Order No. 1

Rockwell International

Semiconductor Products Division

MODEM PRODUCTS DATA BOOK

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Order No. 1
February, 1987

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DEFINITION OF DOCUMENT TYPES

Document Type	Product Status	Definition
Product Preview	Formative or Development	The document type contains the general features and/or specifications for a product in definition or development. The features and/or specifications may change in any manner without notice.
Product Summary	Development or Production	This document type contains the general features and/or specifications of a product in development or in production. Additional information is usually available in a separate document, not contained in this book, such as a Designer's Guide.
Data Sheet (Preliminary)	Sampling or Pre-Production	This document type contains preliminary or design-to characteristic data for a product in pre-production. Additional and/or refined characteristic data will be released in subsequent revisions to the document.
Data Sheet	Production	This document type contains final specification information resulting from measured characteristics. This document type is subject to revision if characteristics are further refined during production.
Product Description	Production	This document type contains final specification information resulting from measured characteristics along with additional application aid information. This document type is subject to revision if characteristics are further refined during production.
Application Note	Development or Production	This document type contains application aids in the use of the subject product. Schematics included in an application note are intended to convey system design concepts only.

NOTICE

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PART NO./DATA BOOK PAGE INDEX

Modem Products
Setting Standards in Connectivity

Rockwell International's OEM modem products offer a highly reliable, cost effective solution for your modem needs. Rockwell has been a driving force behind data communications technology for over 30 years. In the early 1950's we introduced our first modem product. We later pioneered the development of many digital signal processing techniques such as automatic adaptive equalization, digital filtering carrier recovery, phase lock loop and quadrature amplitude modulation. In addition to advanced signal processing technology, Rockwell engineers have developed sophisticated analog filtering techniques.

Today, Rockwell is a generation ahead of our competition with the first fully integrated VLSI modems. Whether communicating at 1200, 2400, 4800, 9600 or 14400 bps, we provide products for any dial-up or leased line modem requirement. High speed network control and multiplexers, personal computer and terminals, standalone and custom modems, facsimile and desktop publishing equipment are samples of end user equipment using Rockwell modems.

With the confidence borne of many years experience in the business, Rockwell offers a full five year warranty on all its standard modem modules and components. This guarantee to our customers reinforces Rockwell's commitment to quality and reliability.

Rockwell is the world's largest supplier of original equipment manufacturer (OEM) modems. We are uniquely positioned to provide the highest quality and performance at competitive prices. With extensive pre-and post-sale support from experienced application engineers, doing business with Rockwell combines the advantages of a large, stable supplier with the responsiveness and innovation of a small entrepreneurial firm.

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PRODUCT INDEX

SECTION 1
1200, 2400 bps DATA MODEMS

1200, 2400 bps DATA MODEMS
Experience Makes a Difference

Rockwell's line of 1200 and 2400 bit-per-second (bps) modem products can easily be incorporated into products requiring high performance, quality and reliability while maintaining a competitive cost advantage. Whether the modem application is internal to a personal computer, or for installation in remote monitoring equipment, Rockwell has a product with the features, form factor and price to meet your requirement.

With the medium speed modem market moving so quickly, time to market is critical. For designers not wishing to develop a custom product, Rockwell offers a Bell 212A and 103 compatible, two-chip set modem with an RS-232-C interface. It also includes the standard "AT" command set in firmware. With minimal external components, such as the FCC-required phone line protection circuitry, a complete modem can be developed within a few weeks. For product designs requiring more flexibility and control, Rockwell offers a standard microprocessor bus (8088 compatible) interface along with user accessible, dual port scratch pad RAM. Together, they allow you to treat the Rockwell modem as a microprocessor peripheral device thus speeding design time. Also, the scratch pad RAM allows the modem to be easily controlled and configured for a wide variety of applications in markets worldwide.

Rockwell also maximizes the design option to develop a single host board and, by plugging in different Rockwell device sets or modules, have a variety of full- or half-duplex, 1200 or 2400 bps modems. Rockwell pioneered this concept with Euro-sized modules incorporating DIN connectors. Now, the next generation form factor is available — a module only seven inches square with dual-in-line pins. This DIP module can be handled as any DIP-type integrated circuit during board assembly and wave soldering. Its small size is ideal for extremely dense designs, such as "1/2 card" modems for personal computers. What's more, all medium speed DIP module products are pin compatible and have the same external dimensions. System designers thereby have a smooth, economical upgrade path from the current R1212 and R2424 products to the new RC1212 and RC2424 families.

Model	Data Speed (bps)	PSTN/ Leased Line	2/4-Wire Half/Full-Duplex	Sync/Async	Compliance
R212AT	1200, 0-300	P	2WFD	Async	Bell 212A, 103 "AT" Command Set
R212DP	1200, 0-300	P	2WFD	Async	Bell 212A, 103
R1212	1200, 600, 0-300	P/L	2WFD	Sync, Async	CCITT V.22 A/B; Bell 212A, 103
R2424	2400, 1200, 600, 0-300	P/L	2WFD	Sync, Async	CCITT V.22 bis, V.22 A/B; Bell 212A, 103
R201/26DP	2400, 1200	P/L	2WHD, 4WFD	Sync	CCITT V.26, V.26 bis; Bell 201B/C
RC1212	1200, 600, 0-300	P/L	2WFD	Sync, Async	CCITT V.22 A/B, V.21; V.23; Bell 212A, 103
RC2424	2400, 1200, 600, 0-300	P/L	2WFD	Sync, Async	CCITT V.22 bis, V.22 A/B, V.21, V.23; Bell 212A, 103

Rockwell

R212DP
Modem Device Set
Bell 212A Compatible

INTRODUCTION

The R212DP/DS Data Pump device set is a high performance 1200/300 bps modem. Using state-of-the-art VLSI technology, the R212DP provides the entire modulation/demodulation process, high and low band filtering, and complete auto dialing function in only two devices.

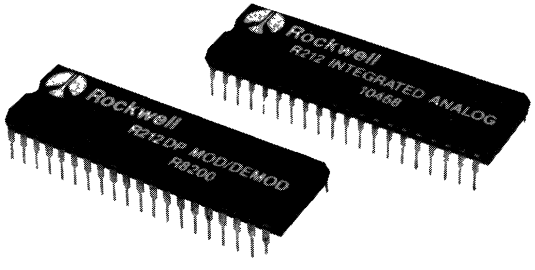
The R212DP is ideal for data transmission over the 2-wire dial-up network. Bell 212A and 103 compatible, the R212DP can handle virtually all applications for full-duplex 1200 bps and 0 to 300 bps asynchronous data transmission over the public switched telephone network (PSTN).

The RS-232-C compatible interface integrates easily into a personal computer, box modem, terminal or any other communications product. The added feature of an integral asynchronous serial auto dialer capable of dialing with DTMF tones or pulses from its 40-byte character buffer offers the user added flexibility in creating a 1200 bps modem customized for specific packaging and functional requirements.

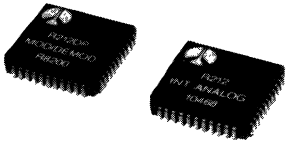
An R212DP/EB Evaluation Board is also available to aid modem system design and evaluation. Included on the printed circuit board are the R212DP/DS modem device set, RS-232-C connector, power connector, an RJ-11 phone jack, six LED indicators, and four configuration switches. The evaluation board comes with an in-depth R212DP Device Set Designer's Guide (Order No. 678) and a wall-mount power supply. All that is required to use the R212DP/EB is an RS-232-C cable connected to a terminal or computer, and a phone cord.

FEATURES

- 2 Device Implementation
  - — R8200 Modulator/Demodulator
  - — 10468 Integrated Analog
- Bell 212A and 103 Compatible (2-Wire Full-Duplex)
  - — Asynchronous
    - 1200 bps DPSK (+1%, −2.5%)
    - 0–300 bps FSK
    - Auto Fallback, Answer Mode
- DTE Interface
  - — Functionally: RS-232-C Compatible
  - — Electrically: TTL
- Auto/Manual Answer
- Auto/Manual Dial
  - — DTMF or Pulses
  - — 0–9 # *, T P CR (ASCII)
  - — 40-Byte Character Buffer
- 10-Bit Character Length
- Break Generation/Detection
- Send/Receive Space Disconnect
- Automatic Adaptive Equalizer
- Analog Loopback
  - — 0 to 300 bps, 1200 bps
- Packaging Options
  - — 40-pin Plastic DIP
  - — 44-pin PLCC

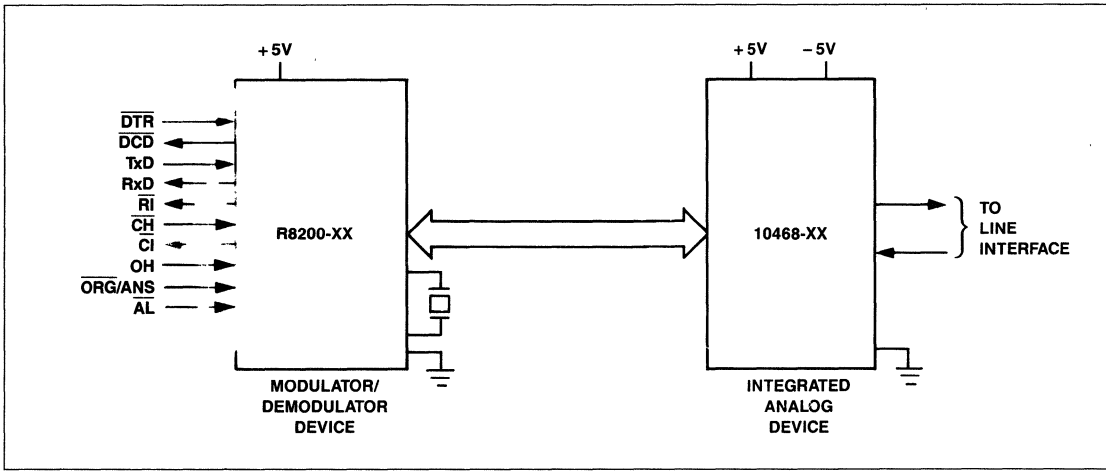


40-PIN DIP



44-PIN PLCC

R212DP/DS Modem Device Set



R212DP/DS Modem Device Set Interface Diagram

SPECIFICATIONS

Power Consumption

+5 Vdc ±5% <300 mA
−5 Vdc ±5% <40 mA
600 mW (typical)

Environmental

Temperature: Operating 0°C to 70°C
Storage −55°C to +150°C
Relative Humidity: Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

R212AT Modem Device Set "AT" Command Set Bell 212A Compatible

INTRODUCTION

The R212AT/DS ("AT" Command Set Compatible) device set is a high performance 1200/300 bps modem. Using state-of-the-art VLSI technology, the R212AT provides the entire modulation/demodulation process, high and low band filtering, and an enhanced "AT" Command Set in only two devices.

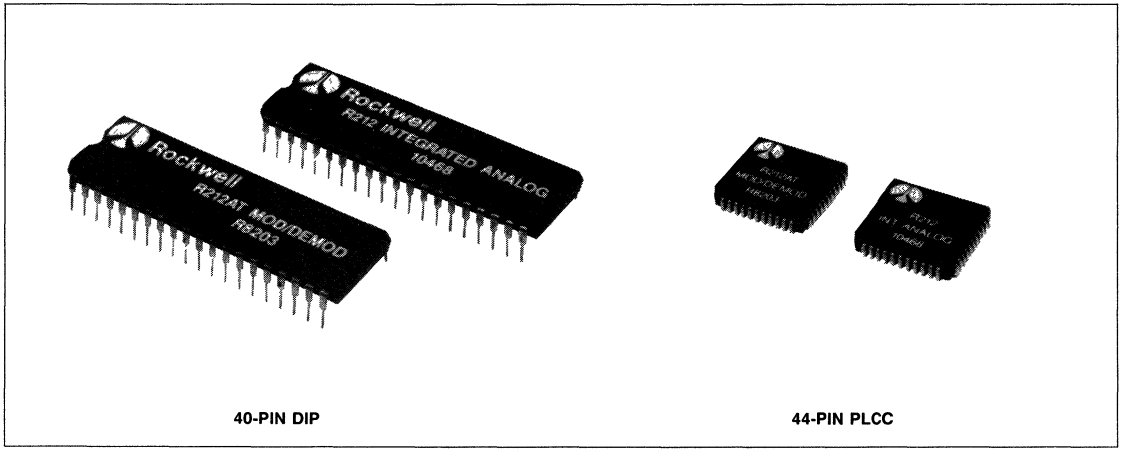
The R212AT is ideal for data transmission over the 2-wire dial-up network. Bell 212A and 103 compatible, the R212AT can handle virtually all applications for full-duplex 1200 bps and 0 to 300 bps asynchronous data transmission over the public switched telephone network (PSTN).

The RS-232-C compatible interface integrates easily into a personal computer, box modem, terminal or any other communications product. The added features of the enhanced "AT" Command Set offer the user added flexibility in creating a 1200 bps modem customized for specific packaging and functional requirements. The R212AT can be readily used with industry standard communication software packages.

An R212AT/EB Evaluation Board is also available to aid modem system design and evaluation. Included on the printed circuit board are the R212AT/DS modem device set, RS-232-C connector, power connector, two RJ-11 phone jacks, 11 LED indicators, four configuration switches, and a speaker with volume control. The evaluation board comes with a detailed R212AT Device Set Designer's Guide (Order No. 686), and a wall-mount power supply. All that is required to use the R212AT/EB is an RS-232-C cable connected to a terminal or computer, and a phone cord.

FEATURES

- 2 Device Implementation
  - — R8203 Modulator/Demodulator
  - — 10468 Integrated Analog
- Bell 212A and 103 Compatible (2-Wire Full-Duplex)
  - — 1200 bps DPSK (+1%, −2.5%) asynchronous
  - — 0–300 bps FSK asynchronous
  - — Auto Fallback, Answer Mode
- Auto/Manual Answer
- Auto/Manual Dial
- "AT" Command Set (see reverse side)
- DTE Interface
  - — Functionally: RS-232-C Compatible
  - — Electrically: TTL
- Data Format
  - — 7 Data Bits; 1 or 2 Stop Bits; Even, Odd, or Fixed Parity
  - — 8 Data Bits; 1 or 2 Stop Bits; No Parity
- Automatic Adaptive Equalizer
- Packaging Options
  - — 40-pin Plastic DIP
  - — 44-pin PLCC



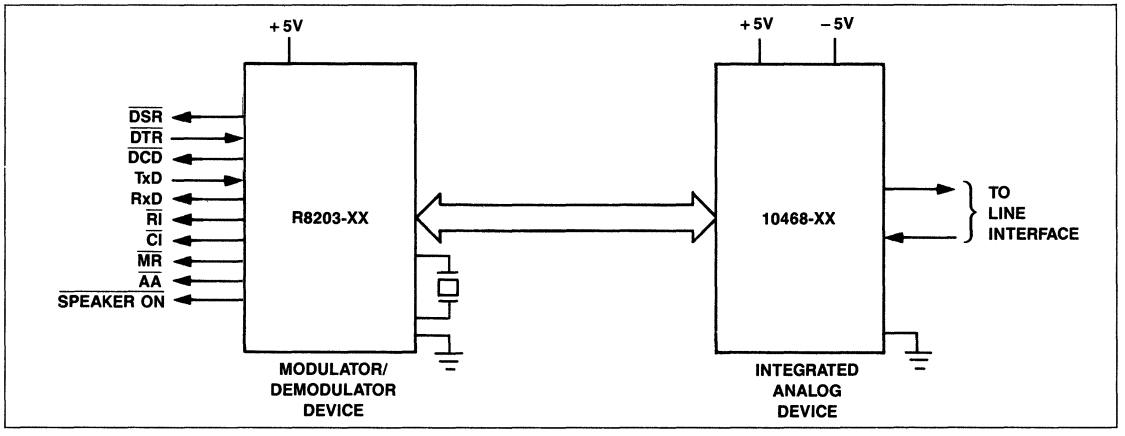
40-PIN DIP

44-PIN PLCC

R212AT/DS Modem Device Set

R212AT "AT" Command Set

Command	Function	Command	Function	Command	Function
AT	Attention Code	Sr=n	Set Register	H	On/Off Hook
A/	Repeat Last Command	V	Verbal/Numeric Result Code	I	Returns Product Code
A	Answer			M	Speaker On/Off
D	Dial	,	Pause	O	On Line
R	Reverse Dial	;	Return to Command State After Dialing	Q	Quiet On/Off
T	Tone Dial			Z	Reset
P	Pulse Dial	E	Echo On/Off	+++	Escape Code
Sr?	Read Register				



R212AT/DS Modem Device Set Interface Diagram

SPECIFICATIONS

Power Consumption

+5 Vdc ±5% <300 mA
-5 Vdc ±5% <40 mA
600 mW (typical)

Environmental

Temperature: Operating 0°C to 70°C
Storage -55°C to +150°C
Relative Humidity: Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

1

R1212
1200 bps Full-Duplex Modem

INTRODUCTION

The Rockwell R1212 is a high performance full-duplex 1200 bps modem. Using state-of-the-art VLSI and signal processing technology, the R1212 provides enhanced performance and reliability. The modem is assembled as a small module with a DIN connector (R1212M amd R1212DC) or a new, smaller module (seven square inches) with a dual-in-line pin (DIP) interface.

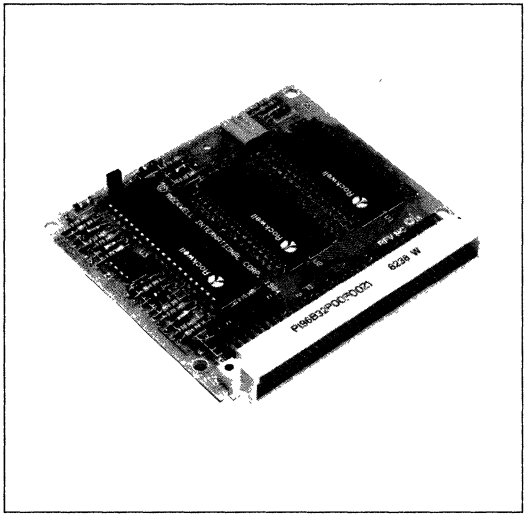
Being CCITT V.22 A, B compatible, as well as Bell 212A and 103 compatible, the R1212 fits most applications for full-duplex 1200 bps (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network, and over point-to-point leased lines.

The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other communications product that demands the utmost in reliability and performance.

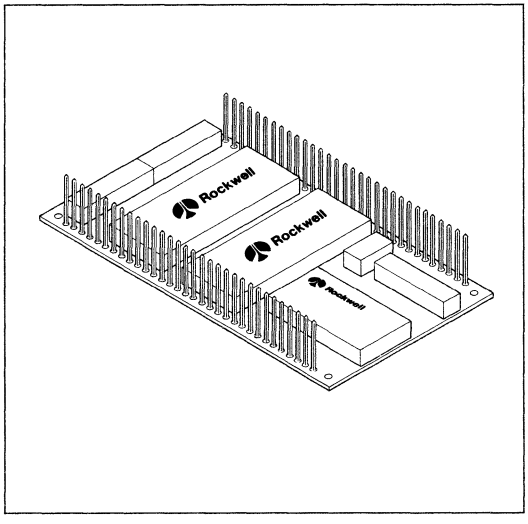
The R1212/DM, with its small form factor and DIP connection, can be automatically installed and soldered onto a host module. Its small size is ideal for internal "1/2-card" PC modem applications. Moreover, the R1212/DM is pin and firmware compatible with the R2424/DM and pin compatible with Rockwell's next generation of medium speed modems, the RC2424 and RC1212.

FEATURES

- CCITT V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 1200 bps, 600 bps ±0.01%
- Asynchronous: 1200 bps, 600 bps +1%, −2.5%, 0–300 bps
  - — Character Length 8, 9, 10, or 11 bits
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL Compatible
- 2-wire Full-Duplex Operation
- Adaptive and Fixed Compromise Equalization
- Test Configurations:
  - — Local Analog Loopback
  - — Remote Digital Loopback
  - — Self Test
- Auto/Manual Answer
- Auto/Manual Dial—DTMF Tone or Pulse Dial
- Power Consumption: 2.3 Watts Typical
- Power Requirements: +5 Vdc, ±12 Vdc
- Three Functional Configurations:
  - — R1212DC (Direct Connect): DIN connector module with FCC approved DAA Part 68 Interface
  - — R1212M: DIN connector module without DAA
  - — R1212/DM: DIP connection module without DAA



R1212M Modem



R1212/DM Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

The transmitter and signaling frequencies supported in the R1212 are listed in Table 1.

Table 1. Transmitter Carrier and Signaling Frequencies Specifications

Mode	Frequency (Hz ±0.01%)
V.22 low channel, Originate Mode	1200
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

TONE GENERATION

The specifications for tone generation are as follows:

1. **Answer Tones:** The R1212 generates echo disabling tones for both the CCITT and Bell configurations, as follows:
   a. CCITT: 2100 Hz ±15 Hz.
   b. Bell: 2225 Hz ±10 Hz.
2. **Guard Tones:** If GTS (see Interface Memory Definitions) is low, an 1800 Hz guard tone frequency is selected; if GTS is high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommendation, the level of transmitted power for the 1800 Hz guard tone is 6 ±1 dB below the level of the data power in the main channel. The total power transmitted to the line is the same whether or not a guard tone is enabled. If a 553.846 Hz guard is used, its transmitted power is 3 ±1 dB below the level of the main channel power, and again the overall power transmitted to the line will remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97 dB and 1.76 dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.
3. **DTMF Tones:** The R1212 generates dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits (see Interface Memory Definitions)must be set to a 1. When in this mode, the specific DTMF tones generated are decided by loading the dial digit register with the appropriate digit as shown in Table 2.

Table 2. Dial Digits/Tone Pairs

Hex	Dial Digits	Tone Pairs	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	★	941	1209
0B	Spare (B)	697	1633
0C	Spare (C)	770	1633
0D	Spare (D)	852	1633
0E	#	941	1477
0F	Spare (F)	941	1633
10	1300 Hz Calling Tone		

TONE DETECTION

The R1212 detects tones in the 340 ±5 Hz to 640 ±5 Hz band.
Detection Level. −10 dBm to −43 dBm
Response Time: 17 ±2 ms

SIGNALING AND DATA RATES

The signaling and data rates for the R1212 are defined in Table 3.

Table 3. Signaling and Data Rates

Operating Mode	Signaling Rate (Baud)	Data Rate
V.22		
(Alternative A)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
(Alternative B)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0 01% Synchronous
Mode ii		1200 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character
Mode iv		600 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character
Bell 212A;	600 0 to 300	1200 bps ±0.01%, Synchronous/Asynchronous 0 to 300 bps Asynchronous

DATA ENCODING

The specifications for data encoding are as follows:

1. *1200 bps (V.22 and Bell 212A).* The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
2. *600 bps (V.22).* Each bit is encoded as a phase change relative to the phase preceding signal elements.

EQUALIZERS

The R1212 provides equalization functions that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.22 and Bell 212A configurations.

Fixed Compromise Equalizer—A fixed compromise equalizer is provided in the transmitter.

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ±150 microseconds over the frequency range 900 to 1500 Hz (low channel) and 2100 to 2700 Hz (high channel).

SCRAMBLER/DESCRAMBLER

The R1212 incorporates a self-synchronizing scrambler-/descrambler. In accordance with the CCITT V.22 and the Bell 212A recommendations.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R1212 can adapt to received frequency errors of up to ±7 Hz with less than a 0.2 dBm degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R1212 satisfies all specified performance requirements for the received line signals from −10 dBm to −48 dBm. The received line signal is measured at the receiver analog input RXA.

TRANSMIT LEVEL

The R1212M output control circuitry contains a variable gain buffer which reduces the modem output level. The R1212M can be strapped via the host interface memory to accomplish this.

PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R1212M transmit level is +6 dBm to allow a Data Access Arrangement (DAA) to be used. The DAA then determines the permissive or programmable configuration.

The R1212DC transmit level is strapped in the permissive mode so that the maximum output level is −10 dBm ±1.0 dBm.

AUTOMATIC RECONFIGURATION

The R1212 is capable of automatically configuring itself to the compatibility of a remote modem. The R1212 can be in either the answer or originate mode for this to occur. The R1212 adaptation compatibilities are limited to V.22 A/B (1200 bps), Bell 212, and Bell 103. If the R1212 is to originate in a specific configuration, the MODE bits (see Interface Memory Definitions) must be set.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, DAA signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The column titled "Type" refers to designations found in the Hardware Circuits Interface Characteristics (Tables 5 and 6). The six groups of hardware circuits are described in the following paragraphs.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives pin 13C to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 13C, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 13C low for at least 3 μs. When an external low input is applied to pin 13C, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 13C is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The R1212 POR sequence leaves the modem configured as follows:

- 1200 bps
- Asynchronous
- 10-bit Character Length
- Constant Carrier
- Serial Mode
- Answer Mode
- Auto Answer Disabled
- RAM Access Code = 00

This configuration is suitable for performing high speed data transfer over the public switched telephone network using the serial data port. Individual features are discussed in subsequent paragraphs.

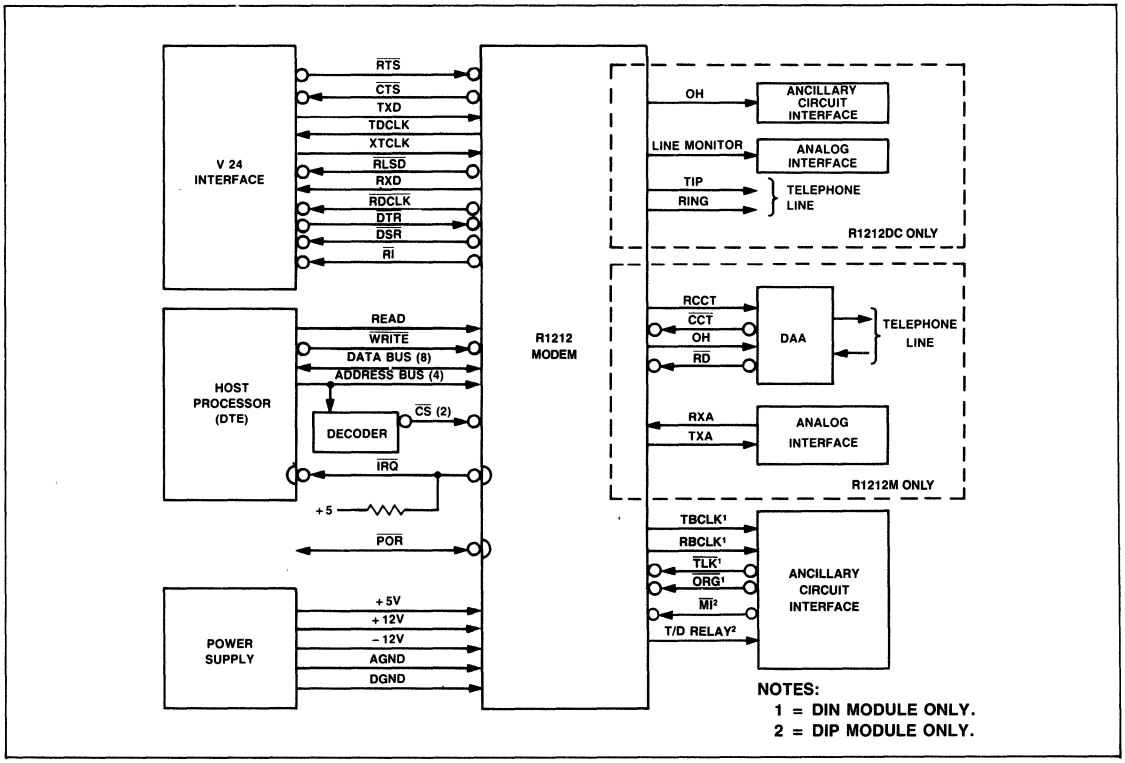


Figure 1. R1212 Modem Functional Interconnect Diagram

Table 4. Hardware Circuits

Name	Type	DIN Pin No.	DIP Pin No.	Description
A. OVERHEAD SIGNALS				
Ground (A)	AGND	31C, 32C	21, 26, 39	Analog Ground Return
Ground (D)	DGND	3C, 8C, 5A, 10A	20, 40, 51, 60	Digital Ground Return
+5 volts	PWR	19C, 23C, 26C, 30C	1, 19, 61	+5 volt supply
+12 volts	PWR	15A	22	+12 volt supply
−12 volts	PWR	12A	25	−12 volt supply
$\overline{POR}$	I/OB	13C	13	Power-on-Reset
B. MICROPROCESSOR INTERFACE SIGNALS				
D7	I/OA	1C	52	↕ Data Bus (8-Lines)
D6	I/OA	1A	53	
D5	I/OA	2C	54	
D4	I/OA	2A	55	
D3	I/OA	3A	56	
D2	I/OA	4C	57	
D1	I/OA	4A	58	
D0	I/OA	5C	59	
RS3	IA	6C	45	↕ Register Select (4-Lines)
RS2	IA	6A	44	
RS1	IA	7C	43	
RS0	IA	7A	42	
$\overline{CS0}$	IA	10C	48	Chip Select Receiver (Baud Rate Device)
$\overline{CS1}$	IA	9C	41	Chip Select Transmitter (Sample Rate Device)
$\overline{READ}$	IA	12C	47	Read Enable
$\overline{WRITE}$	IA	11A	49	Write Enable
$\overline{IRQ}$	OB	11C	50	Interrupt Request

Name	Type	DIN Pin No.	DIP Pin No.	Description
C. V.24 INTERFACE SIGNALS				
XTCLK	IB	22A	3	External Transmit Clock
TDCLK	OC	23A	7	Transmit Data Clock
$\overline{RDCLK}$	OC	21A	8	Receive Data Clock
$\overline{RTS}$	IB	25A	4	Request-to-Send
$\overline{CTS}$	OC	25C	5	Clear-to-Send
TXD	IB	24C	6	Transmit Data
RXD	OC	22C	9	Receive Data
$\overline{RLSD}$	OC	24A	10	Received Line Signal Detector
$\overline{DTR}$	IB	21C	12	Data Terminal Ready
$\overline{DSR}$	OC	20A	11	Data Set Ready
$\overline{RI}$	OC	18A	2	Ring Indicator
D. ANALOG SIGNALS				
RXA (M)	IB	32A	23	Receive Analog Input
TXA (M)	OC	31A	24	Transmit Analog Output
TIP/RING (DC) LINE	AE	RJ11 Jacks	—	Phone Line Interface
MONITOR (DC)	AD	30A	—	Analog Line Monitor
E. DAA INTERFACE SIGNALS				
$\overline{RD}$ (M)	IB	27A	35	Ring Detect
RCCT (M)	OC	28A	—	Request Coupler Cut Through
$\overline{CCT}$ (M)	IB	29C	—	Coupler Cut Through
OH	OC	29A	36	Off-Hook Relay Status
T/D Relay	OC	—	37	Talk/Data Relay
$\overline{MI}$	IC	—	38	Manual Input
F. ANCILLARY INTERFACE SIGNALS				
TBCLK	OC	27C	—	Transmit Baud Clock
RBCLK	OC	26A	—	Receive Baud Clock
$\overline{TLK}$	IC	28C	—	Talk (TLK = Data)
$\overline{ORG}$	IB	16C	—	Originate (ORG = Answer)
(M) R1212M Only, (DC) R1212DC Only, — = not applicable				

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Ouput Type							
			IA	IB	IC	OA	OB	OC	I/O A	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min.				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min.[2]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±2.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1 6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max −10 min.	−240 max −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes: 1. I load = −100 μA 2. I load = 1 6 mA 3. I load = −40 μA 4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc 5 I load = 0.36 mA

Table 6. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604Ω ±1% with an output level of +6 dBm. To obtain a 0 dBm output, a 600Ω load to ground is needed.
RXA	AB	The receiver input impedance is 23.7 KΩ ±1%. The receive level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled).
LINE MONITOR	AD	The line monitor output impedance is 15 KΩ ±5%.
TIP/RING	AE	The impedance of TIP with respect to RING is 600 Ω.

V.24 INTERFACE

Eleven hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, +5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Data Terminal Ready ($\overline{DTR}$)

$\overline{DTR}$ prepares the modem to be connected to the communications channel, and maintains the connection established by the DTE (manual answering) or internal (automatic answering) means. $\overline{DTR}$ OFF places the modem in the disconnect state.

Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) ON indicates that the modem is in the data transfer state. $\overline{DSR}$ OFF is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except $\overline{RI}$. $\overline{DSR}$ will switch to the OFF state when in test state. The ON condition of $\overline{DSR}$ indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem has generated an answer tone or detected answer tone.
4. After ring indicate ($\overline{RI}$) goes ON, $\overline{DSR}$ waits at least two seconds before turning ON to allow the telephone company equipment to be engaged.

$\overline{DSR}$ will go OFF 50 ms after $\overline{DTR}$ goes OFF, or 50 ms plus a maximum of 4 seconds when the SSD bit is enabled.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. In constant carrier mode, $\overline{RTS}$ can be wired to $\overline{DTR}$. In controlled carrier operation, independent operation of $\overline{RTS}$ turns the carrier ON and OFF. The responses to $\overline{RTS}$ are shown in Table 7 (assume the modem is in data mode).

Table 7. $\overline{RTS}$ Responses

Leased or Dial Line[1]	$\overline{RTS}$ OFF	$\overline{RTS}$ ON
Controlled Carrier	$\overline{CTS}$ OFF Carrier OFF	Carrier ON 210 to 275 ms Scrambled 1 s Transmitted $\overline{CTS}$ ON
Constant Carrier	$\overline{CTS}$ OFF Carrier ON Scrambled 1 s Transmitted	$\overline{CTS}$ ON Carrier ON Data Transmitted

Note:
1. After handshake is complete.

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON or OFF condition of $\overline{RTS}$ are shown in Table 8.

Table 8. $\overline{CTS}$ Response Times

$\overline{CTS}$ Transition	Constant Carrier	Controlled Carrier
OFF to ON	<2 ms	210 to 275 ms
ON to OFF	<20 ms*	<20 ms*

Note: *Programmable

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency*. Selected data rate of 1200 Hz or 600 Hz (±0.01%).

2. *Duty Cycle*. 50 ±1%.

TDCLK is provided to the user in both asynchronous and synchronous communications. TDCLK is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing (TDCLK is not valid in FSK). TDCLK is necessary for synchronous communication. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{\text{RDCLK}}$)

The modem provides a Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±.035% (relative) frequency error in the associated transmit timing source.

$\overline{\text{RDCLK}}$ is provided to the user in both asynchronous and synchronous communications. $\overline{\text{RDCLK}}$ is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing ($\overline{\text{RDCLK}}$ is not valid in FSK). $\overline{\text{RDCLK}}$ is necessary for synchronous communication.

Received Line Signal Detector ($\overline{\text{RLSD}}$)

The $\overline{\text{RLSD}}$ thresholds for both high and low channels are:

$\overline{\text{RLSD}}$ ON ≥ −43 dBm
$\overline{\text{RLSD}}$ OFF ≤ −48 dBm

$\overline{\text{RLSD}}$ will not respond to guard tones or answer tones.

When $\overline{\text{RLSD}}$ is active, it indicates to the terminal equipment that valid data is available on RXD.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Ring Indicator ($\overline{\text{RI}}$)

The modem provides a Ring Indicator ($\overline{\text{RI}}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the ON segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The high condition of the $\overline{\text{RI}}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received. The operation of $\overline{\text{RI}}$ is not disabled by an OFF condition on $\overline{\text{DTR}}$.

$\overline{\text{RI}}$ will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across TIP and RING), with the response times given in Table 13.

This OFF-to-ON (ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent ON (OFF) transition of $\overline{\text{RI}}$.

Table 9. $\overline{\text{RI}}$ Response Time

$\overline{\text{RI}}$ Transition	Response Time
OFF-to-ON*	110 ±50 ms (50% duty cycle)
ON-to-OFF	450 ±50 ms
Note: *The OFF-to-ON time is duty cycle dependent: 890 ms (15%) ≥ time ≥ 50 ms (100%)	

MICROPROCESSOR INTERFACE

Seventeen hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{CS0}$ and $\overline{CS1}$) and Register Selects (RS0-RS1)

The signal processor to be accessed is selected by grounding one of two unique chip select lines, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ line high or the $\overline{WRITE}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to + 5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

DAA INTERFACE

The R1212M provides a Data Access Arrangement (DAA) interface that is directly hardware and software compatible with the RDAA. Manual/automatic originate and answer are then controlled via the appropriate R1212M hardware ancillary circuits or software control bits. The modem provides the only interface with the microprocessor (MPU) bus, i.e., no RDAA interface signals must be directly controlled from the MPU bus.

Ring Detect ($\overline{RD}$)

$\overline{RD}$ indicates to the modem by an ON (low) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the $\overline{RD}$ input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40 Vrms, 15 to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on $\overline{RI}$.

Request Coupler Cut Through (RCCT)

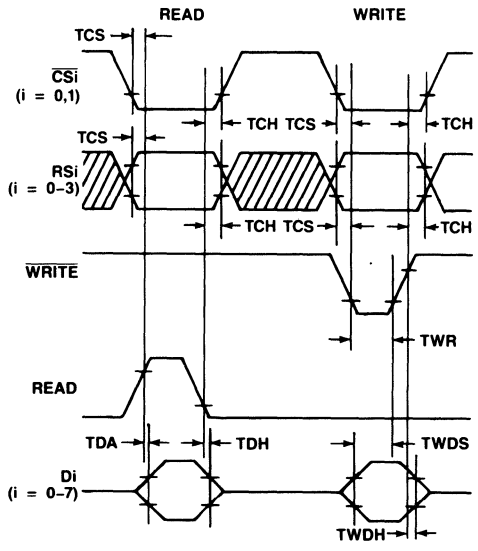
RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When RCCT goes OFF (low), the cut-through buffers are disabled and $\overline{CCT}$ should go OFF (high). RCCT should be OFF during dialing but ON for tone address signaling.

Coupler Cut Through ($\overline{CCT}$)

An ON (low) signal to the $\overline{CCT}$ lead indicates to the modem that the data transmission path through the DAA is connected. This input can always be grounded if the two second billing delay squelch is desired. If $\overline{CCT}$ is user controlled, the billing delay squelch can only be 2 seconds or greater.

Off-Hook Relay Status (OH)

The modem provides an OH output which indicates the state of the OH relay. A high condition on OH implies the OH relay is closed and the modem is connected to the telephone line (off-hook). A low condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.



Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
$\overline{CSi}$, RSi hold time after Read or $\overline{Write}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram

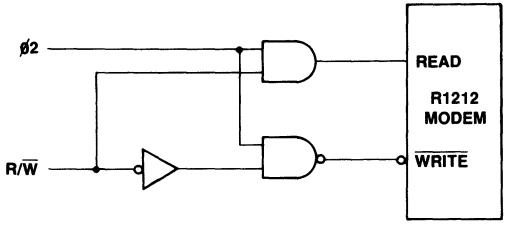


Figure 3. R/$\overline{W}$ to READ $\overline{WRITE}$ Conversion Logic

ANALOG SIGNALS (R1212M)

Two connections are devoted to analog audio signals: TXA and RXA.

Transmit Analog (TXA)

The TXA output is suitable for driving a data access arrangement for connection to either leased lines or the public switched telephone network. The transmitter output impedance is 604 ohms ±1% with an output level of +6 dBm ±1 dBm. To obtain a 0 dBm output, a 600 ohm load to ground is needed.

Receive Analog (RXA)

RXA is an input to the receiver from a data access arrangement. The input impedance is 23.7K ohms ±1%. The received level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled).

ANALOG SIGNALS (R1212DC)

Three analog signals are output by the R1212DC: LINE MONITOR, TIP and RING.

Analog Line Monitor (LINE MONITOR)

The LINE MONITOR output is suitable for a speaker interface. It provides an output for all dialing signals, call progress signals, and the carrier signals. The output impedance is 15K ohms ±1%. The signals which appear on LINE MONITOR are approximately the same level as the signals would appear on the network (assuming a 1 dB loss attributed to the audio transformer).

Phone Line Interface (TIP and RING)

TIP and RING are the DAA analog outputs to the public switched telephone network. These outputs use two RJ11 jacks in parallel as the interface to the network (see Table 10 and Figure 4). The R1212DC, which contains the DAA TIP and RING interface, has been FCC Part 68 approved. The user need not apply for further Part 68 approval. The impedance of TIP with respect to RING is 600 ohms.

Table 10. R1212DC Network Interface

Connector Type	Pin Number	Name	Function
RJ11 Jack	3	RING	One Side of TELCO Line
	4	TIP	One Side of TELCO Line

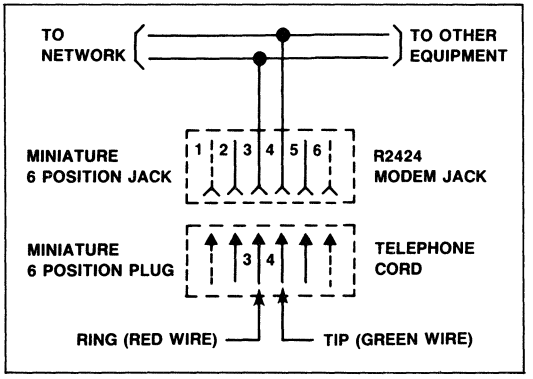


Figure 4. RJ11 Telephone Jack

ANCILLARY CIRCUITS

Transmit Baud Clock (TBCLK) and Received Baud Clock (RBCLK)

TBCLK and RBCLK are provided to the user at the baud rate (600 Hz).

Talk ($\overline{TLK}$) (DIN Module Only)

$\overline{TLK}$ is an input which manually places the modem on-hook (relay open, $\overline{TLK}$ = 0) or off-hook (relay closed, $\overline{TLK}$ = 1). The on-hook condition is referred to as TALK mode and the off-hook condition is referred to as DATA mode. $\overline{TLK}$ is used with $\overline{ORG}$ to manually originate or answer a call. $\overline{TLK}$ should be 0 at power-on or reset to prevent the modem from inadvertently entering the data mode.

Originate ($\overline{ORG}$)

$\overline{ORG}$ is an input which manually places the modem in the originate mode ($\overline{ORG}$ = 0) or the answer mode ($\overline{ORG}$ = 1). To manually originate a call, $\overline{ORG}$ = 0 and $\overline{TLK}$ = 0. Dial the number using the telephone. When the other modem answers and sends answer tone switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook.

To manually answer a call $\overline{ORG}$ = 1 and $\overline{TLK}$ = 0. When the phone rings switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook.

Off-Hook Relay Status (OH)

The modem provides an OH output which indicates the state of the OH relay. A high condition on OH implies the OH relay is closed and the modem is connected to the telephone line (off-hook). A low condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

T/D Relay. (DIP Module Only)

The T/D Relay signal may be used as a second relay control when the parallel control mode of operation is selected (BUS bits 0 and 1 = 1). If the serial control mode is selected (BUS bits 0 and 1 = 0) the T/D relay follows the status of the OH output signal which is controlled by the $\overline{MI}$ signal. In the parallel control mode the OH output signal is controlled by the status of the DATA bit, while independent control of the T/D relay is provided by the $\overline{MI}$ signal. During pulse dialing the OH signal reflects the pulse signals being dialed. It is therefore possible to use the T/D Relay signal to control the off-hook relay and use the OH signal to perform pulse dialing on a separate, independent relay.

Manual Input ($\overline{MI}$) (DIP Module Only)

$\overline{MI}$ is an input which manually places the modem on-hook (relay open, $\overline{MI}$ = 0) or off-hook (relay closed, $\overline{MI}$ = 1). The on-hook condition is referred to as TALK mode and the off-hook condition is referred to as DATA mode. $\overline{MI}$ is used with $\overline{ORG}$ to manually originate or answer a call. $\overline{MI}$ should be 0 at power-on or reset to prevent the modem from inadvertently entering the data mode.

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load-/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on two special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into two areas. These areas are partitioned into receiver and transmitter devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 32 addressable registers in the modem receiver (CS0) and transmitter (CS1) interface memory are shown in Figures 5 and 6, respectively. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Figures 7 and 8 show the registers according to the overall function they perform in the receiver and transmitter, respectively. Figures 9 and 10 show the power-on configuration for the R1212 modem receiver and transmitter devices, respectively.

Table 11 defines the individual bits in the interface memory. In the Table 11 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R							
E	IRQ	ENSI	NEWS	—	NEWC	—	—	—
D	BUS	CRQ	—	—	—	LCD	RSD	—
C	—	—	—	CHAR		—	—	—
B	—	—	—	—	—	—	—	AL
A	ERDL	RDL	DL	ST	MODE			
9	—	—	SPEED		—	—	—	—
8	TONE	ATD	—	—	—	—	TM	RLSD
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (YRAMRM)							
4	RAM Data YRL (YRAMRL)							
3	RAM Data XRM (XRAMRM)							
2	RAM Data XRL (XRAMRL)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—

Note
(—) Indicates reserved for modem use only.

Figure 5. Receiver ($\overline{CS0}$) Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T							
E	IRQ	ENSI	NEWS	—	NEWC	DDEI	—	DDRE
D	BUS	CRQ	DATA	AAE	DTR	—	—	SSD
C	DSRA	TXCLK		CHAR		—	—	DLSF[1]
B	TX LEVEL			GTE	GTS	3DB	DTMF	AL
A	ERDL	RDL	DL	ST	MODE			
9	NAT[1]	—	ORG	LL	RTS	CC	EF	NTS
8	DLO	CTS	DSR	RI	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (YRAMTM)							
4	RAM Data YTL (YRAMTL)							
3	RAM Data XTM (XRAMTM)							
2	RAM Data XTL (XRAMTL)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register							

Notes
1. Not valid before R5312-16
(—) Indicates reserved for modem use only.

Figure 6. Transmitter ($\overline{CS1}$) Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	DIAGNOSTIC CONTROL							
E	HANDSHAKE							
D	CONFIGURATION							
C	CONFIGURATION							
B	CONFIGURATION							
A	CONFIGURATION							
9	STATUS							
8	STATUS							
7	RESERVED							
6	RESERVED							
5	DIAGNOSTIC							
4	DIAGNOSTIC							
3	DIAGNOSTIC							
2	DIAGNOSTIC							
1	RESERVED							
0	RESERVED							
Register / Bit	7	6	5	4	3	2	1	0

Figure 7. Receiver ($\overline{CS0}$) Interface Memory Functions

Register \ Bit	7	6	5	4	3	2	1	0
F	DIAGNOSTIC CONTROL							
E	HANDSHAKE							
D	CONFIGURATION							
C	CONFIGURATION							
B	CONFIGURATION							
A	CONFIGURATION							
9	CONFIGURATION							
8	STATUS							
7	RESERVED							
6	RESERVED							
5	DIAGNOSTIC							
4	DIAGNOSTIC							
3	DIAGNOSTIC							
2	DIAGNOSTIC							
1	RESERVED							
0	DIAL DIGIT REGISTER							
Register / Bit	7	6	5	4	3	2	1	0

Figure 8. Transmitter ($\overline{CS1}$) Interface Memory Functions

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	—	—	—
D	BUS 0	CRQ 0	—	—	—	LCD 1	RSD 0	—
C	—	—	—	CHAR 1	0	—	—	—
B	—	—	—	—	—	—	—	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	0	MODE 0	1	1
9	—	—	SPEED 0	0	—	—	—	—
8	TONE 0	ATD 0	—	—	—	—	TM 0	RLSD 0
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (Random)							
4	RAM Data YRL (Random)							
3	RAM Data XRM (Random)							
2	RAM Data XRL (Random)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—
Register \ Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 9. R1212 Receiver ($\overline{CS0}$) Interface Memory Power On Configuration

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	DDEI 0	—	DDRE 0
D	BUS 0	CRQ 0	DATA 0	AAE 0	DTR 0	—	—	SSD 0
C	DSRA 0	TX CLK 0	0	CHAR 1	0	—	—	DLSF 0
B	TX LEVEL 0	0	0	GTE 0	GTS 0	3DB 0	DTMF 0	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	0	MODE 0	1	1
9	NAT 0	—	ORG 0	LL 0	RTS 0	CC 0	EF 0	NTS 0
8	DLO 0	CTS 0	DSR 0	RI 0	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (Random)							
4	RAM Data YTL (Random)							
3	RAM Data XTM (Random)							
2	RAM Data XTL (Random)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register (Write-Only Register)							
Register \ Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 10. R1212 Transmitter ($\overline{CS1}$) Interface Memory Power On Configuration

Table 11. Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
AAE	Auto Answer Enable	1:D:4	When configuration bit AAE is a 1, the modem will automatically answer when a ringing signal is present on the line. When AAE is set to a 1, the modem will answer after one ring and go into data mode. The modem goes off-hook 1 second after the on-to-off transition of the ring. The $\overline{ORG}$ pin or ORG bit need not to be set to the answer polarity. If it is desired to answer after more than one ring, then the user must use the alternative answer method described under the DATA bit. The $\overline{DTR}$ pin or the DTR bit must also be set before the modem will auto answer. Writing a 0 into the AAE bit will cause the modem to go on-hook. This will occur only when the modem auto answers using the AAE bit
AL	Analog Loopback	(0,1):B:0	When configuration bits AL are a 1, the modem is in local analog loopback (V.54 Loop 3). In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface. An attenuator is introduced into the loop such that the signal level coupled into the receive path is attenuated 14 ±1 dBm. The modem may be placed into analog loopback in either the idle mode or the data mode. However, in the data mode, setting the AL bits to a 1 will terminate the connection. Analog loopback will only function in the high speed modes (1200, or 600 bps). The DTE may be tested when the modem is in analog loopback. Also, all parts of the modem except the line interface are checked. If no DTE is connected, the modem integrity may be verified by use of the self test function. When entering analog loopback, set AL in the receiver to a 1 before setting AL in the transmitter to a 1. When exiting analog loopback, reset AL in the transmitter to a 0 before resetting AL in the receiver to a 0.
ATD	Answer Tone Detected	0:8:6	When status bit ATD is a 1, it signifies that the modem receiver detected the answer tone. The bit is 1 set 75 ms after the answer tone is first detected, and is cleared to a 0 when the modem goes on-hook. The user may clear ATD manually after CTS is active.
BUS	Bus Select	(0,1):D:7	When configuration bits BUS are a 1, the modem is in the parallel control mode; and when 0, the modem is in the serial control mode. BUS can be in either state to configure the modem. *Serial Control Mode* The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. The control signals used in serial control mode are $\overline{DTR}$, $\overline{RTS}$, $\overline{TLK}$, and $\overline{ORG}$. Outputs such as $\overline{RLSD}$ and $\overline{DSR}$ are reflected both in the interface memory and the V.24 interface. Once the bus bits have been set to a 0, the state of the DTR, RTS, DATA, and ORG bits are ignored. *Parallel Control Mode* The modem has the capability of modem control via the microprocessor bus. Data transfer is maintained over the serial V.24 channel. The control bits used in parallel control are DTR, RTS, ORG, and DATA The modem automatically defaults to the serial mode at power-on. If the parallel control mode is to be used, it is recommended that the $\overline{TLK}$ pin be tied to ground. A floating $\overline{TLK}$ pin will assume a logic 1 which will immediately put the modem into the data mode before the BUS bits are set. In either mode, the modem is configured by the host processor via the microprocessor bus

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
CC	Controlled Carrier	1:9:2	When configuration bit CC is a 1, the modem operates in controlled carrier; when 0, the modem operates in constant carrier. Controlled carrier allows the modem transmitter to be controlled by the $\overline{RTS}$ pin or the RTS bit. Its effect may be seen in the RTS and CTS descriptions.
CHAR	Character Length Select	(0,1):C:(3,4)	These character length bits select either 8, 9, 10, or 11 bit characters (includes data, stop, and start bits) as shown below: **Configuration Word** 4 3 — **Configuration** 0 0 — 8 bits 0 1 — 9 bits 1 0 — 10 bits 1 1 — 11 bits It is possible to change character length during the data mode. Errors in the data will be expected between the changeover and the resynchronization (which occurs on the next start bit after the change is implemented).
CRQ	Call Request	(0,1):D:6	When configuration bit CRQ in chip 1 (the transmitter) is a 1, it places the transmitter in auto dial mode. The data then placed in the Dial Digit Register is treated as digits to be dialed. The format for the data should be a hex representation of the number to be dialed (if a 9 is to be dialed then an 09_{16} should be loaded in DDR). CRQ in chip 1 should be a 1 for the duration of the data mode. If CRQ in chip 1 is changed to a 0, the modem will go on-hook. Also, see DDRE bit. When configuration bit CRQ in chip 0 (the receiver) is a 1, the receiver goes into tone detect mode. Any energy above threshold and in the 345 to 635 Hz bandwidth is reflected by the TONE bit. CRQ in chip 0 must be reset to a 0 (after the last digit was dialed and tone detection completed) before the answer tone is sent by the answering modem (after ringback is detected). CRQ in chip 0 need not be used during auto dialing, but may be used to provide call progress information as part of an intelligent auto dialing routine An example flowchart is given in Figure 11. FF (hex) should be loaded into the Dial Digit Register after the last digit is dialed and tone detection is completed. This action also puts the modem in data mode and starts a 30 second abort timer. If the handshake has not been completed in 30 seconds the modem will go on-hook.
CTS	Clear-to-Send	1:8:6	When status bit CTS is a 1, it indicates to the terminal equipment that the modem will transmit any data which are present at TXD. CTS response times from an ON or OFF condition of RTS are shown below: **CTS Transition** — **Constant Carrier** — **Controlled Carrier** OFF to ON — ≤2 ms — 210 to 275 ms ON to OFF — ≤20 ms* — ≤20 ms* *Programmable
DATA	Talk/Data	1:D:5	When control bit DATA is a 1, the modem is in the data state (off-hook); and when 0, the modem is in the talk state (on-hook). This bit allows the modem to go off-hook after a programmable number of rings by counting the required number of RI bit transitions and then setting the DATA bit (assuming ORG = 0).
DDEI	Dial Digit Empty Interrupt	1:E:2	When handshake bit DDEI is a 1, an interrupt will occur when the Dial Digit Register (1:0) is empty (DDRE = 1). This is independent of the state of the ENSI bit. The interrupt will set the IRQ bit and also assert the $\overline{IRQ}$ signal. Loading the Dial Digit Register with a new digit will clear the interrupt condition.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DDR	Dial Digit Register	1 0:(0–7)	DDR is used to load the digits to be dialed. Example: If a 4 is to be dialed, an 04 (hex) should be loaded. This action also causes the interrupt to be cleared. The modem automatically accounts for the interdigit delay. Note. DDR is a write-only register.
DDRE	Dial Digit Register Empty	1·E:0	When handshake bit DDRE is a 1, it indicates that the dial digit register is empty and can be loaded with a new digit to be dialed. If the DDEI bit is set, the IRQ bit will be set when the DDRE bit is set. Also, the $\overline{IRQ}$ signal will be generated. After the DDR is loaded, DDRE goes to a 0 and the interrupts are automatically cleared.
DL	Digital Loopback (Manual)	(0,1):A·5	When configuration bits DL are set to a 1, the modem is manually placed in digital loopback. DL should only be set during the data mode. The DSR and CTS bits will be reset to a 0. The local modem can then be tested from the remote modem end by looping a remotely generated test pattern. At the remote modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be reset to a 0. The local modem will then return to the normal data mode with control reverting to the DTEs, DTR. DL does not function in 300 bps.
DLO	Dial Line Occupied	1:8:7	When status bit DLO is a 1, it indicates that the modem is in the auto dial state, i.e., CRQ in the transmitter is a 1 and the modem is off-hook and ready to dial.
DLSF	Disable Low Speed Fallback	1:C:0	When configuration bit DLSF is a 1, the modem will not automatically fallback to the 300 bps operating mode if it is configured for another data rate. This bit is valid in originate mode only.
DSR	Data Set Ready	1:8:5	The ON condition of the status bit DSR indicates that the modem is in the data transfer state. The OFF condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits — except RI. DSR will switch to the OFF state when in test state. The ON condition of DSR indicates the following: The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing. The modem has generated an answer tone or detected answer tone. After ring indicate goes ON, DSR waits at least two seconds before turning ON to allow the telephone company equipment to be engaged. DSR will go OFF 50 msec after DTR goes OFF, or 50 msec plus a maximum of 4 sec when the SSD bit is enabled.
DSRA	Data Set Ready in Analog Loopback	1:C:7	When configuration bit DSRA is a 1, it causes DSR to be ON during analog loopback.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DTMF	Touch Tones/Pulse Dialing	1:B:1	When configuration bit DTMF is a 1, it tells the modem to auto dial using tones; and when 0, the modem will dial using pulses. The timing for the pulses and tones are as follows (power-on timing): Pulses — Relay open 64 ms Relay closed 36 ms Interdigit delay 750 ms Tones — Tone duration 95 ms Interdigit delay 70 ms The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. The output power level of the DTMF tones is as follows: ±15 dBm ±1 measured at TXA for the R1212M −1 dBm ±1 measured at TIP/RING for the R1212DC
DTR	Data Terminal Ready	1:D:3	Control bit DTR must be a 1 for the modem to enter the data state, either manually or automatically. DTR must also be a 1 in order for the modem to automatically answer an incoming call. During the data mode, DTR must remain at a 1, otherwise the connection will be terminated if DTR resets to a 0 for greater than 50 ms.
EF	Enable Filters	1:9:1	Setting CRQ in the transmitter to a 1 disables the high and low band filters used in data mode so that call progress tone detection can be done. Setting CRQ in the receiver to a 1 inserts a passband filter in the receive path which passes energy in the 345 Hz to 635 Hz bandwidth. The high and low band filters must be enabled and the passband filter disabled for the answer tone and carrier to be detected. This occurs automatically during the auto dial process when EF is set to a 0. In this case, the high and low band filters are disabled when CRQ in the transmitter is set to a 1. If tone detection is required, CRQ in the receiver should be set to a 1. After dialing and call progress tone detection, CRQ in the receiver is set to a 0 and FF is loaded into the dial digit register. (Loading FF enables the high and low band filters). At this time, the answer tone can be detected. To re-enable the high and low band filters disabled by setting CRQ in the transmitter, set EF to a 1. After CRQ in the transmitter and receiver is set to a 1 and tone detection is completed, it may be necessary to detect the answer tone before loading FF into the dial digit register (see the section on sending 1300 Hz calling tone). At that point, EF can be set to a 1 and CRQ in the receiver set to a 0 so the answer tone can be detected (using the ATD bit) and the 1300 Hz calling tone can still be sent. Once the answer tone is detected, FF should be loaded into the dial digit register and the EF bit set to a 0.
ENSI	Enable New Status Interrupt	(0,1):E:6	When handshake bit ENSI is a 1, it causes an interrupt to occur when the status bits in registers (0:[8,9]) and (1:8) are changed by the modem. (NEWS = 1). The IRQ bit will be set to a 1 and the $\overline{IRQ}$ signal will be generated. The interrupt is cleared by writing a 0 into the NEWS bit.
ERDL	Enable Response to Remote Digital Loopback	(0,1):A:7	When configuration bits ERDL are a 1, it enables the modem to respond to another modem's remote digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS, DSR and RLSD bits to a 0 and turns the $\overline{CTS}$, $\overline{DSR}$ and $\overline{RLSD}$ signals to a logic 1. The TM bit is set to inform the user of the test status. When the ERDL bits are a 0, no response will be generated.
GTE	Guard Tone Enable	1:B:4	When configuration bit GTE is a 1, it causes the specified guard tone to be transmitted (CCITT configurations only), according the state of the GTS bit. Note: The guard tone will only be transmitted by the answering modem.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
GTS	Guard Tone Select	1:B:3	When configuration bit GTS is a 0, it selects the 1800 Hz tone; when GTE is a 1 it selects the 550 Hz tone. The selected guard tone will be transmitted only when GTE is enabled.
IRQ	Interrupt	(0,1):E:7	When status bit IRQ is a 1, it indicates that an interrupt has been generated. The $\overline{IRQ}$ hardware signal is generated following the setting of the IRQ bit. $\overline{IRQ}$ is cleared when either the NEWS bit is reset to a 0 or the DDR is loaded with a number.
LCD	Loss of Carrier Disconnect	0:D:2	When configuration bit LCD is a 1, the modem terminates a call when a loss of received carrier energy is detected after 400 ms. After the first 40 ms of loss of carrier, RLSD goes off. 360 ms later, if no carrier is detected, CTS goes off, and the modem goes on-hook. If energy above threshold is detected during the 360 ms period, RLSD will be set to a 1 again. If further loss of energy occurs, the 400 ms time frame is restarted. If LCD is set to a 0, RLSD will be set to a 1 when energy is above threshold, but will not force the modem on-hook when energy falls below threshold. In this case, it is necessary to re-enable LCD in order to put the modem on-hook. LCD is not automatically disabled in leased line operation. The user must write a 0 into LCD bits for this to occur.
LL	Leased Line	1:9:4	When configuration bit LL is a 1, the modem is in leased line operation; when 0, the modem is in switched line operation. When LL is set to a 1, the modem immediately goes off-hook and into data mode.
MODE	Mode Select	(0,1):A:(0,3)	These bits select the compatibility at which the modem is to operate, as shown below: **Configuration Word** / **Configuration** 3 2 1 0 0 0 1 0 — Bell 212A 1200 Sync. 0 0 1 1 — Bell 212A 1200 Async. 0 1 0 0 — Bell 212A 0 to 300 Async. 1 0 0 0 — V.22A 1200 Sync. 1 0 0 1 — V.22B 1200 Async. 1 0 1 0 — V.22A 600 Sync. 1 0 1 1 — V.22B 600 Async. NOTE: The Mode bits in both chips should be set exclusively of all other bits, followed immediately by the setting of the NEWC bits. This will ensure proper modem configuration. *Automatic Reconfiguration* The modem is capable of automatically falling back during the handshake to the compatibility of a remote modem. The modem can be in either the answer or originate mode for this to occur. The compatibilities that the modem are limited to adapt to are V.22 A/B (1200 bps), Bell 212 and Bell 103. If the R1212 is to originate in a specific configuration, the MODE bits must be set. When the answer modem is configured for Bell 300 asynchronous and is called by a 1200 bps modem, the handshake will be completed at 1200 bps.
NAT	No Answer Tone	1:9:7	When configuration bit NAT is a 1, the modem will not transmit the 2100 Hz CCITT answer tone. This bit is only valid for CCITT configurations. With this bit enabled in answer mode, when the modem goes off-hook it will remain silent for 75 ms and then transmit unscrambled ones.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
NEWC	New Configuration	(0,1):E:3	When the NEWC bit is a 1, it tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC to a 0. NEWC must be set to a 1 after a new configuration has been written into the following registers: (0:[A–D]) and (1:[9–D]). The remaining registers do not require the use of NEWC to tell the modem that new data was written into them.
NEWS	New Status	(0,1):E:5	When handshake bit NEWS is a 1, it tells the user that there has been a change of status in the status registers. The user must write a 0 into NEWS to reset it. This action also causes the interrupt to be cleared.
NTS	No Transmitter Scrambler	1:9:0	When configuration bit NTS is a 1, when the modem is off-hook it will transmit all data in an unscrambled form. This bit should be disabled if the normal modem handshake is desired.
ORG	Originate/Answer	1:9:5	When configuration bit ORG is a 1, the modem is in originate mode; and when a 0 the modem is in answer mode. (This is only valid in manual originate/answer and analog loopback). If ORG is a 1 in analog loopback, the modem will transmit in the high band and receive in the low band. If ORG is a 0 in analog loopback, the modem will transmit in the low band and receive in the high band.
(None)	RAM Access R	0:F:0–7	Contains the RAM access code used in reading RAM locations in chip 0 (receiver device).
(None)	RAM Access T	1:F:0–7	Contains the RAM access code used in reading RAM locations in chip 1 (transmitter device).
XRAMRL	RAM Data XRL	0:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 0.
XRAMRM	RAM Data XRM	0:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 0.
XRAMTL	RAM Data XTL	1:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1.
XRAMTM	RAM Data XTM	1:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.
YRAMRL	RAM Data YRL	0:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 0.
YRAMRM	RAM Data YRM	0:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 0.
YRAMTL	RAM Data YTL	1:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1.
YRAMTM	RAM Data YTM	1:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RDL	Remote Digital Loopback	(0,1):A:6	When configuration bits RDL are a 1, it causes the modem to initiate a request for the remote modem to go into digital loopback. RXD is clamped to a mark and the CTS bit and $\overline{CTS}$ signal will be reset until the loop is established. The TM bit is not set in this case, since the local modem initiated the request. RDL does not function in 300 bps.
RI	Ring Indicator	1:8:4	When status bit RI is a 1, it indicates that a ringing signal is being detected. The RI bit follows the ringing signal with a 1 during the on time and a zero during the off time coincident with the $\overline{RI}$ signal. The following are the RI bit response times: **RI Bit Transition** — **Response** OFF-to-ON* — 110 ±50 ms (50% duty cycle) ON-to-OFF — 450 ±50 ms *The OFF-to-ON time is duty cycle dependent. 890 ms (15%) ≥ time ≥ 50 ms (100%) This OFF-to-ON (or ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent transition of the RI bit.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RLSD	Received Line Signal Detector	0:8:0	When status bit RLSD is a 1, it indicates that the carrier has successfully been received. RLSD will not respond to the guard tones or answer tones. RLSD response times are given below: **Constant Carrier** / **Controlled Carrier** $\overline{\text{RLSD}}$[1] OFF-to-ON: 105 to 205 ms / 105 to 205 ms ON-to-OFF: 10 to 24 ms / 10 to 24 ms **Note:** 1. After handshake has occurred.
RSD	Receive Space Disconnect	0:D:1	When configuration bit RSD is a 1, the modem goes on-hook after receiving approximately 1.6 seconds of continuous spaces.
RTS	Request-to-Send	1:9:3	When control bit RTS is a 1, the modem transmits any data on TXD when CTS becomes active. In constant carrier mode, RTS should be set the same time as DTR and then left ON. In controlled carrier operation, independent operation of RTS turns the carrier ON and OFF. The responses to RTS are shown (assume the modem is in data mode). **Leased or Dial Line[1]** / **RTS Off** / **RTS On** Controlled Carrier: CTS OFF, Carrier OFF / Carrier ON, 210 to 275 ms Scrambled 1's Transmitted, CTS ON Constant Carrier: CTS OFF, Carrier ON, Scrambled 1's Transmitted / CTS ON, Carrier ON, Data Transmitted **Note:** 1. After handshake is complete. For ease of use in constant carrier mode, RTS should be turned ON the same time as DTR.
SPEED	Speed Indication	0:9:(4,5)	The SPEED status bits reflect the speed at which the modem is operating. The SPEED bit representations are shown. **4** **5** **Speed** 0 0 0–300 0 1 600 1 0 1200 **Note:** The SPEED bits are not active in analog loopback and leased line mode.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
SSD	Send Space Disconnect	1:D:0	When configuration bit SSD is a 1, it causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR goes from active to inactive state.
ST	Self Test	(0,1):A:4	When configuration bit ST is a 1, self test is activated. ST must be a 0 to end the test. It is possible to perform self test in analog loopback with or without a DTE connected. During any self test, TXD and RTS are ignored. Self test does not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver. Error detection is accomplished by monitoring the self test error counter in the RAM. If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic register when the RAM access code 00 is loaded in the diagnostic control register (0:F). *Self Test End-to-End (Data Mode)* Upon activation of self test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler. *Self Test with Loop 3* Loop 3 is applied to the modem as defined in Recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test, In this test DTR is ignored. *Self Test with Loop 2 (Data Mode)* The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test. ST does not function in 300 bps.
3DB	3 dB Loss to Receive Signal	1:B:2	When configuration bit 3DB is a 1, it attenuates the received signal 3 dB. This is only used if the modem will see 0 dBm or greater line signal at the receiver input. Insertion of the 3 dB loss will then prevent saturation.
TM	Test Mode	0:8:1	When status bit TM is a 1, it indicates that the modem has completed the handshake and is in one of the following test modes: AL or RDL.
TONE	Tone Detect	0:8:7	TONE follows the energy detected in the 340 to 640 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle of the TONE bit. TONE is active only when CRQ in chip 0 is a 1. Detection Range: −10 to −43 dBm Response Time: 17 ±2 ms
TXCLK	Transmit Clock Select	1:C:(5,6)	TXCLK allows the user to designate the origin of the transmitter data clock, as shown below: **Configuration Word** **Transmit Clock** — **6** **5** Internal — 0 0 External — 1 0 Slave — 1 1 If external clock is chosen the user clock must be input at XTCLK. The clock characteristics must be the same as TDCLK. The external clock will be reflected by TDCLK. If slave clock is chosen the transmitter is slaved to the receive clock. This is also reflected by TDCLK.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TX LEVEL	Transmit Level	1:B:(5–7)	TX LEVEL allows the user to change the transmit level at TIP and RING (assuming the DAA has 10 dBm attenuation in the transmit path).

Configuration Word 7	6	5	Transmit Level (±1.0 dBm) (at TIP and RING)
0	0	0	–10 dBm
0	0	1	–12 dBm
0	1	0	–14 dBm
0	1	1	–16 dBm
1	0	0	–18 dBm
1	0	1	–20 dBm
1	1	0	–22 dBm
1	1	1	–24 dBm

Internal Modem Timing

In a microprocessor environment it is necessary to know how long various functions last or what the response times of certain functions are. Since the modem is a part of the microprocessor environment its timing and response times are necessary. Table 12 provides the timing relationships between interface memory bits and modem functions.

Table 12. Internal Modem Timing

Parameter	Time Interval
NEWC bit checked	
Transmitter	Once per sample[1]
Receiver	Once per baud[2]
NEWC bit set by host until modem action	
Transmitter	≤ One baud time
Receiver	One baud time
Control, Configuration bits read	
Transmitter	Only after NEWC is set
Receiver	ST, RSD—every sample, all others after NEWC set
Status bits updated	
Transmitter	Once per sample
Receiver	Once per baud
Status change reflected by NEWS, IRQ	
Transmitter	MIN < one sample time MAX one sample time
Receiver	MIN one sample time MAX one baud time
Memory status reflected to modem pin	
Transmitter	33.33 μs
Receiver	33.33 μs

1. Sample Time = 7200 Hz 2. Baud Time = 600 Hz

AUTO DIAL SEQUENCE

The following flow chart defines the auto dial sequence via the microprocessor interface memory.

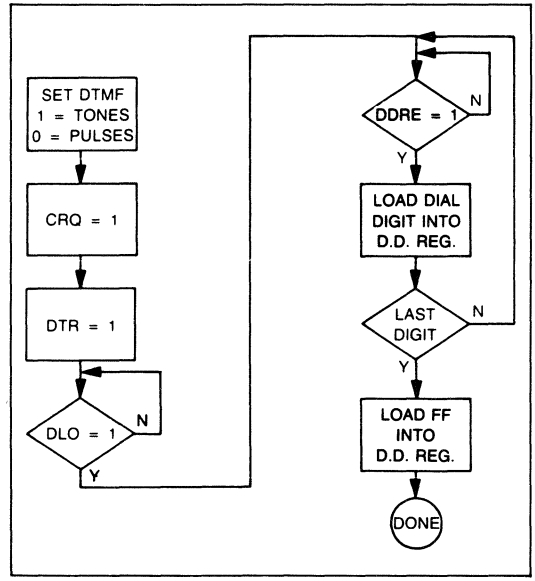


Figure 11. Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

SIGNAL PROCESSOR RAM ACCESS

RAM AND DATA ORGANIZATION

Each signal processor contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16-bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

Interface Memory Locations

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit normally transfers a word from RAM to interface memory once each clock cycle of the SP device. In the transmitter, a word is transferred from SP RAM to the interface memory every sample time. In the receiver, a word is transferred from RAM to the interface memory every sample time as well. Each RAM word transferred to the interface memory is 32-bits long. These bits are written by the SP logic unit into interface memory registers 5, 4, 3, and 2. Registers 3 and 2 contain the most significant byte and least significant byte, respectively, of the XRAM data. Registers 5 and 4 contain the most and least significant bytes of YRAM data, respectively.

RAM Access Codes

The SP logic unit determines the SP RAM address to read from, or write to, by the code stored in the RAM Access bits of interface memory register F (RAM Access R in the receiver 0:F and RAM Access T in the transmitter 1:F).

Only the transmitter (chip 1) allows data to be transferred from interface memory to SP RAM. When set to a 1, bit 1:F:7 signals the SP logic unit to disable transfer of SP RAM data to the interface memory, and instead, to transfer data from interface memory to SP RAM. When writing into SP RAM, 32 bits of data in the XRAM and YRAM registers will be written into the appropriate SP RAM location as specified by the RAM access code (82-86) in register 1:F (Table 13). Once the data is written into the RAM access register 1:F, the XRAM registers 1:2 and 1:3 or the YRAM registers 1:4 and 1:5, set the NEWC bit 1:E:3 to a 1. This action causes the information to be transferred from interface memory into SP RAM. Bit 7 of register 1:F is cleared to a 0 by the modem after the RAM is read. New data can be written into the SP RAM after the NEWC bit is reset to a 0 by the SP.

Note:

Any transmitter RAM Write operation must always be preceded by a RAM read from the desired location. This is to guarantee that the correct information is written into the 16 unchanged bits, since all transmitter RAM operations are 32 bit transfers with typically only 16 of the bits used.

Both the transmitter and receiver (chips 1 and 0, respectively) allow data to be transferred from SP RAM into the interface memory. A 0 in transmitter bit 1:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the RAM access code in register 1:F. A 0 in receiver bit 0:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the access code in register 0:F. To read the SP RAM in chip 1 (transmitter), load into 1:F the RAM access code which identifies the 32 bits of data to transfer to the XRAM and YRAM registers. Next, set the NEWC bit 1:E:3 to a 1. After transferring the data from RAM to the XRAM or YRAM registers, the NEWC bit is reset to a 0 by the SP. Chip 0 (receiver), on the other hand, will provide the XRAM and YRAM data one sample time following the loading of the RAM access code into register 0:F, and will continue to provide the same data at one sample time intervals until a new RAM access code is loaded.

When reading from or writing into RAM, no bits are provided for handshaking or interrupt functions. The NEWC bit can be used as a mechanism to provide sample and baud intervals. Since the NEWC bit is checked, once per baud in chip 0 and once per sample in chip 1, the user can set the NEWC bit and wait for it to be cleared. Depending on which chip the NEWC bit was set, the time interval from the setting to the clearing of the NEWC bit will be either one sample or one baud time. This, however, will not guarantee that the action of reading and writing the XRAM and YRAM will occur in the middle of an actual sample or baud time.

Table 13. RAM Access Codes

Node	Function	RAM Access Code		Chip	Reg. No.
		RAM Read	RAM Write		
1	Demodulator Output	56	–	0	2, 3, 4, 5
2	Low Pass Filter Output	40	–	0	2, 3, 4, 5
3	Input Signal to Equalizer Taps	41–4D	–	0	2, 3, 4, 5
4	AGC Gain Word	14	–	0	2, 3
5	Equalizer Tap Coefficients	01–0D	–	0	2, 3, 4, 5
6	Equalizer Output	53	–	0	2, 3, 4, 5
7	Rotated Equalizer Output (Received Point Eye Pattern)	11	–	0	2, 3, 4, 5
8	Decision Points (Ideal Eye Pattern)	51	–	0	2, 3, 4, 5
9	Rotated Error	52	–	0	2, 3, 4, 5
10	Rotation Angle	12	–	0	4, 5
11	Phase Error	10	–	0	2, 3
12	Self Test Error Counter	00	–	0	2, 3
	DTMF Tone Duration	02	82	1	4, 5
	DTMF Interdigit Delay	03	83	1	2, 3
	Pulse Interdigit Delay	03	83	1	4, 5
	Pulse Relay Make Time	04	84	1	2, 3
	Pulse Relay Break Time	04	84	1	4, 5
	Handshake Abort Counter	05	85	1	4, 5
	Handshake Abort Timer	06	86	1	2, 3
	CTS Off-Time	07	87	1	2, 3

NOTE: 1. All the chip 1 access codes are not valid before R5312-13.
2. Access codes are hexadecimal.
3. Only chip 1 RAM can be written.
4. CTS Off-Time is not valid before R5312-16.

ERROR RATES

Bit error rate (BER) is a measure of the throughput of data on the communication channel. It is the ratio of the number of received bits in error to the number of transmitted bits. This number increases with decreasing signal-to-noise ratio (SNR). The type of line disturbance and the modem configuration affect the BER.

Tables 14 through 16 summarize the BERs for various conditions. Figure 12 shows the BER measurement setup.

Table 14. BER Summary

R1212		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
1200 bps	1×10^{-5}	8.2 dB	7.9 dB
600 bps	1×10^{-5}	5.0 dB	5.0 dB
300 bps	1×10^{-5}	9.2 dB	7.0 dB

Test Condition: Signal Level = −30 dBm,
Sync for 1200 bps, 600 bps,
Async for 300 bps,
With 3002 Unconditioned Line.

Table 15. BER Summary

R1212		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
1200 bps	1×10^{-5}	8.3 dB	8.1 dB
600 bps	1×10^{-5}	5.0 dB	5.0 dB
300 bps	1×10^{-5}	10.4 dB	7.2 dB

Test Condition: Signal Level = −43 dBm,
Sync for 1200 bps, 600 bps,
Async for 300 bps,
With 3002 Unconditioned Line.

Table 16. BER Summary

R1212		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
1200 bps	1×10^{-5}	7.7 dB	7.9 dB
600 bps	1×10^{-5}	4.6 dB	4.5 dB
300 bps	1×10^{-5}	9.3 dB	6.2 dB

Test Condition: Signal Level = −40 dBm,
Sync for 1200 bps, 600 bps,
Async for 300 bps,
Back-To-Back.

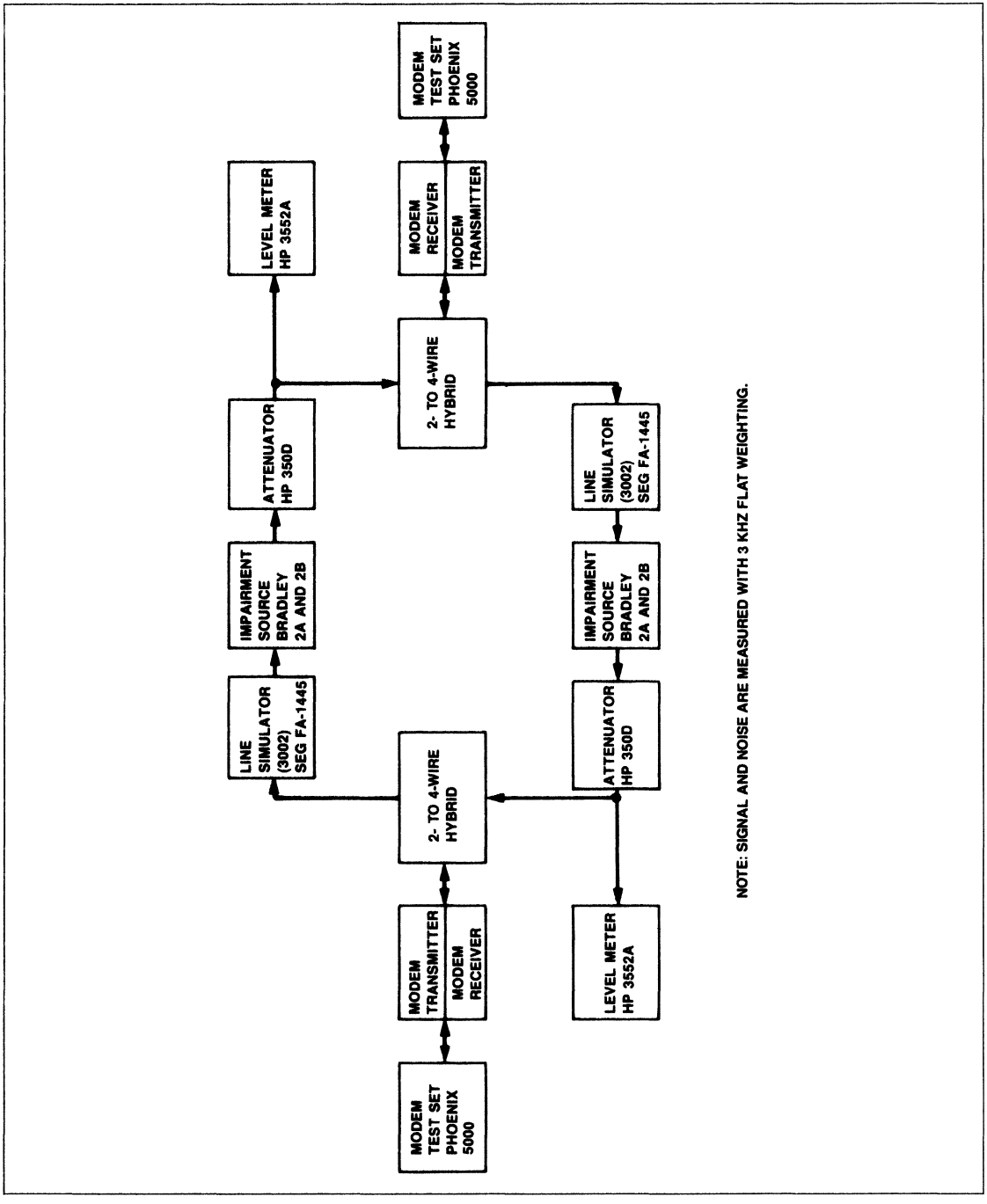


Figure 12. 2-Wire Full-Duplex Bit Error Rate Performance Test Setup (Bidirectional)

Table 17. Modem Power Requirements

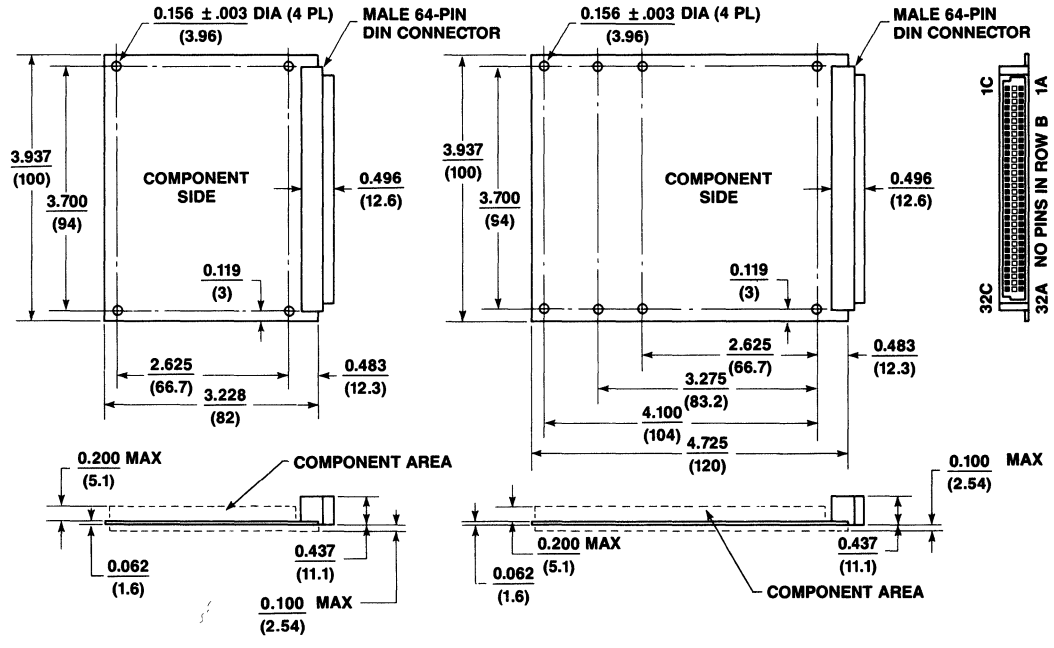
Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	390 mA	<455 mA
+12 Vdc	±5%	25 mA	< 30 mA
−12 Vdc	±5%	4 mA	< 5 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Table 18. Modem Environmental Restrictions

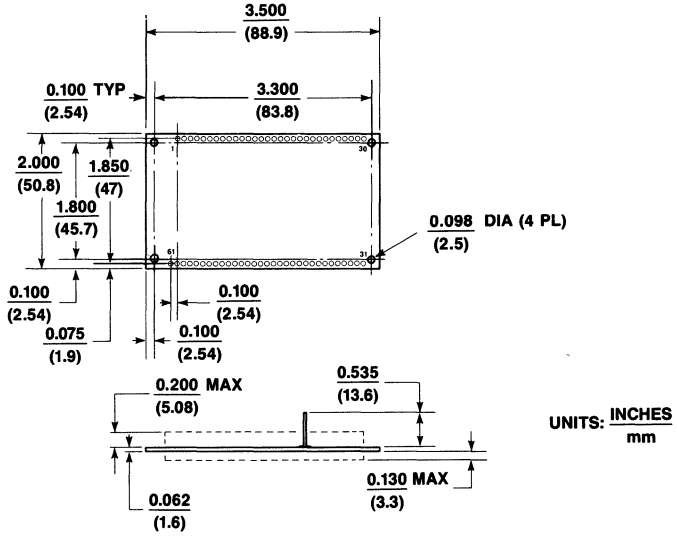
Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 19. Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated.
Board Structure:	The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
PCB Dimensions:	
DC Version	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Height	0.75 in. (19 mm)
M Version	
Width	3.937 in. (100 mm)
Length	3.328 in. (82 mm)
Height	0.40 in. (10.2 mm)
Weight (max):	0.45 lbs. (0.20 kg.)
Lead Extrusion (max.):	0.100 in. (2.54 mm)
DIP Connector Version	
Board Structure	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions	
Width	2.0 in. (50.8 mm)
Length	3.5 in. (88.9 mm)
Height	0.2 in. (5.08 mm) above, 0.13 in. (3.30 mm) below
Weight (max.)	2.6 oz. (73g)
Pin Length (max.)	0.53 in. (13.5 mm) above



DIN CONNECTOR VERSION



DIP CONNECTOR VERSION

Figure 13. Modem Printed Circuit Board Dimensions

R1212 MODEM INSTALLATION AND MAINTENANCE

This section contains installation instructions and maintenance procedures for the Rockwell R1212DC Modem. It also contains a special notice from the Canadian Department of Communications (DOC) for Canadian operation and from the Federal Communications Commission (FCC) for United States operation.

GENERAL DESCRIPTION

The Rockwell R1212DC modem is designed to be used with the United States or Canadian Telephone Switched Networks in 2-wire full-duplex dial-up operation. The modem requires protective circuitry registered with the Federal Communications Commission (FCC) Part 68 which allows direct connection to the U.S. switched telephone network. This circuitry also complies with the Canadian Department of Communications (DOC) Terminal Attachment Program (TAP) which similarly defines their switched telephone network requirements.

The R1212DC features automatic dial and answer capabilities along with surge suppression and hazardous voltage and longitudinal balance protection. Its maximum output signal level at the telephone interface is set at -10 dBm ± 1 dBm (permissive mode of operation).

Two standard telephone jack connectors (RJ11s) are mounted side by side on one edge of the board and are wired in parallel. One is for connection to the telephone line network and the other for the telephone headset connection.

INSTALLATION AND SIGNAL ROUTING INSTRUCTIONS

PHYSICAL MOUNTING

The modem module may be physically incorporated into the customer's end product by utilizing the four corner 0.156" diameter mounting holes (for the self-hooking plastic type standoffs or for bolting it down to some rigid structure) or by installing the module into card guides.

ELECTRICAL INTERFACING INSTRUCTIONS

The electrical interfacing is accomplished via the DIN (Euro) connector (for external power inputs and digital logic signals) and the telco connectors (for the telephone network connection). Note that the telephone interface connectors are physically separated from the modem interface control connector and extreme care must be taken in routing the telephone interface leads from the modem to the telephone network (line connector jack in the wall).

FCC RULES PART 68 REQUIREMENTS

The FCC Rules Part 68 requires that the telephone interface leads shall:

1. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use the same connector as leads or metallic paths connecting to power connections.

   Note

   Power connections are defined as the connections between commercial power and any transformer, power supply rectifier, converter or other circuitry associated with the modem. The connections of the interface pins (including the $+12$ Vdc, -12 Vdc and $+5$ Vdc) are not considered power connections.

2. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use adjacent pins on the same connector as metallic paths that lead to unregistered equipment, when specification details provided to the FCC do not show that the interface voltages are less than nonhazardous voltage source limits in Part 68.

   Note

   All the DIN connector interface voltages to the modem have been established as non-hazardous.

ROUTING OF TELEPHONE INTERFACE LINES

In routing the telephone interface leads from the modem telephone connector jacks to the telephone line network connection, the following precautions should be strongly considered for safety.

1. The telephone interface routing path should be as direct and as short as possible.
2. Any cable used in establishing this path should contain no signal leads other than the modem telephone interface leads.
3. Any connector used in establishing this path shall contain not commercial power source signal leads, and adjacent pins to the TIP and RING (T and R) pins in any such connector shall not be utilized by any signals other than those shown in this document.

MAINTENANCE PROCEDURE

Under the FCC Rules, no customer is authorized to repair modems. In the event of a Rockwell modem malfunctioning, return it for repair to an authorized ROCKWELL INTERNATIONAL distributor (if in Canada) or send it directly to the Semiconductor Products Division, Rockwell International Corporation, El Paso, Texas 79906.

SPECIAL INSTRUCTION TO USERS

If the Rockwell modem has been registered with the Federal Communications Commission (FCC), you must observe the following to comply with the FCC regulations:

A. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.

B. It is prohibited to connect the modem to pay telephones or party lines.

C. You are required to notify the local telephone company of the connection or disconnection of the modem, the FCC registration number, the ringer equivalence number, the particular line to which the connection is made and the telephone number to be associated with the jack.

Note

If the proper jacks are not available, you must order the proper type of jacks to be installed by the telephone company (VSOC RJ11 for permissive mode of operation).

D. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only if it can be determined that the telephone line and not the modem is the source of trouble. If the Rockwell modem needs repair, return it to the ROCKWELL INTERNATIONAL CORPORATION. This applies to the modem whether it is in or out of warranty. Do not attempt to repair the unit as this is a violation of the FCC rules and may cause danger to persons or to the telephone network.

TELEPHONE COMPANY RIGHTS AND RESPONSIBILITIES

A. The Rockwell modem contains protective circuitry to prevent harmful voltages to be transmitted to the telephone network. If such harmful voltages do occur, then the telephone company may temporarily discontinue service to you. In this case, the telephone company should:

1. Promptly notify you of the discontinuance.
2. Afford you the opportunity to correct the situation which caused the discontinuance.
3. Inform you of your right to bring a complaint to the FCC concerning the discontinuance.

B. The telephone company may make changes in its facilities and services which may affect the operation of your equipment. It is, however, the telephone company's responsibility to give you adequate notice in writing to allow you to maintain uninterrupted service.

LABELING REQUIREMENTS

A. The FCC requires that the following label be prominently displayed on the outside surface of the customer's end product and that the size of the label should be such that all the required information is legible without magnification.

Sample label below:

Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.

FCC Registration Number: AMQ9SQ-14211-DM-E

Ringer Equivalence: 0.9B

Note

The Rockwell modem module has the FCC registration number and ringer equivalence number permanently affixed to the solder side of the PCB and any unit containing this modem shall use this information for the label requirements.

SPECIAL NOTICE FROM THE CANADIAN DEPARTMENT OF COMMUNICATIONS

The Canadian Department of Communications label identifies certified equipment. This certification means that the equipment meets certain telecommunications network protective, operational and safety requirements. The Department does not guarantee the equipment will operate to the user's satisfaction.

Before installing this equipment, users should insure that it is permissible to be connected to the facilities of the local telecommunications company. The equipment must also be installed using an approved method of connection. In some cases, the company's inside wiring associated with a single line individual service may be extended by means of a certified jack-plug-cord ensemble (telephone extension cord). The customer should be aware that the compliance with the above conditions may not prevent degradation of service in some situations. Existing telecommunications company requirements do not permit their equipment to be connected to customer-provided jacks except where specified by individual telecommunications company tariffs.

The Department of Communications requires the Certificate Holders to identify the method of network connection in the user literature provided with the certified terminal equipment.

Repairs to certified equipment should be made by an authorized Canadian maintenance facility designated by the supplier. Any repairs or alterations made by the user to this equipment, or equipment malfunctions may give the telecommunications company cause to request the user to disconnect the equipment.

Users should ensure for their own protection that the electrical ground connections of the power utility, telephone lines and internal metallic water pipe system, if present, are connected together. This precaution may be particularly important in rural areas.

CAUTION

Users should not attempt to make such connections themselves, but should contact the appropriate electric inspection authority, or electrician, as appropriate.

Rockwell

R2424
2400 bps Full-Duplex Modem

INTRODUCTION

The Rockwell R2424 is a high performance full-duplex 2400 bps modem. Using state-of-the-art VLSI and signal processing technology, the R2424 provides enhanced performance and reliability. The modem is assembled as a small module with a DIN connector (R2424M and R2424DC) or a new, smaller module (seven square inches) with a dual-in-line pin (DIP) interface.

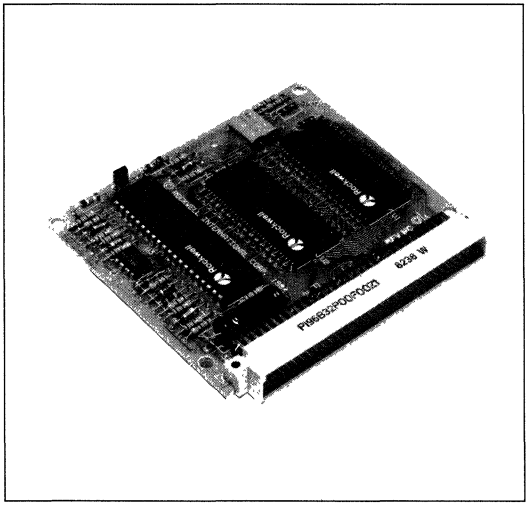
Being CCITT V.22 bis, V.22 A, B compatible, as well as Bell 212A and 103 compatible, the R2424 fits most applications for full-duplex 2400 and 1200 bps fallback (synchronous and asynchronous) and 0 to 300 bps asynchronous data transmission over the general switched telephone network, and over point-to-point leased lines.

The direct-connect, auto dial/answer features are specifically designed for remote and central site computer applications. The bus interface allows easy integration into a personal computer, box modem, microcomputer, terminal or any other communications product.

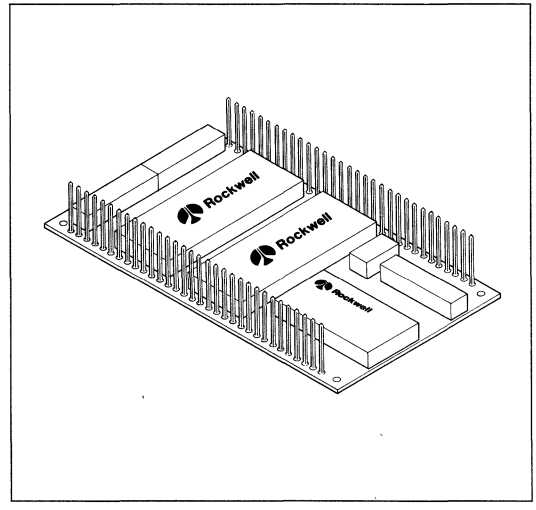
The R2424/DM, with its small form factor and DIP connection, can be automatically installed and soldered onto a host module. Its small size is ideal for internal "1/2-card" PC modem applications. Moreover, the R2424/DM is pin and firmware compatible with the R1212/DM and pin compatible with Rockwell's next generation of medium speed modems, the RC2424 and RC1212.

FEATURES

- CCITT V.22 bis, V.22 A, B Compatible
- Bell 212A and 103 Compatible
- Synchronous: 2400 bps, 1200 bps, 600 bps ±0.01%
- Asynchronous: 2400 bps, 1200 bps, 600 bps +1%, −2.5%, 0–300 bps
  - — Character Length 8, 9, 10, or 11 bits
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL Compatible
- 2-wire Full-Duplex Operation
- Adaptive and Fixed Compromize Equalization
- Test Configurations:
  - — Local Analog Loopback
  - — Remote Digital Loopback
  - — Self Test
- Auto/Manual Answer
- Auto/Manual Dial—DTMF Tone or Pulse Dial
- Power Consumption: 2.3 Watts Typical
- Power Requirements: +5 Vdc, ±12 Vdc
- Three Module Configurations:
  - — R2424DC (Direct Connect): DIN connector module with FCC approved DAA Part 68 Interface
  - — R2424M: DIN connector module without DAA
  - — R2424/DM: DIP connection module without DAA
- Two Functional Versions
  - — R2424/US All data rates specified except 600 bps
  - — R2424/INT All data rates specified except 0–300 bps



R2424M Modem



R2424/DM Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

The transmitter and signaling frequencies supported in the R2424 are listed in Table 1.

Table 1. Transmitter Carrier and Signaling Frequencies Specifications

Mode	Frequency (Hz ±0.01%)
V.22 bis low channel, Originate Mode	1200
V.22 low channel, Originate Mode	1200
V.22 bis high channel, Answer Mode	2400
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

TONE GENERATION

The specifications for tone generation are as follows:

1. **Answer Tones:** The R2424 generates echo disabling tones for both the CCITT and Bell configurations, as follows:
   a. CCITT: 2100 Hz ±15 Hz.
   b. Bell: 2225 Hz ±10 Hz.
2. **Guard Tones:** If GTS (see Interface Memory Definitions) is low, an 1800 Hz guard tone frequency is selected; if GTS is high, a 553.846 Hz tone is employed. In accordance with the CCITT V.22 Recommendation, the level of transmitted power for the 1800 Hz guard tone is 6 ±1 dB below the level of the data power in the main channel. The total power transmitted to the line is the same whether or not a guard tone is enabled. If a 553.846 Hz guard is used, its transmitted power is 3 ±1 dB below the level of the main channel power, and again the overall power transmitted to the line will remain constant whether or not a guard tone is enabled. The device accomplishes this by reducing the main channel transmit path gain by .97 dB and 1.76 dB for the cases of the 1800 Hz and 553.846 Hz guard tones respectively.
3. **DTMF Tones:** The R2424 generates dual tone multi-frequency tones. When the transmission of DTMF tones are required, the CRQ and DTMF bits (see Interface Memory Definitions)must be set to a 1. When in this mode, the specific DTMF tones generated are decided by loading the dial digit register with the appropriate digit as shown in Table 2.

Table 2. Dial Digits/Tone Pairs

Hex	Dial Digits	Tone Pairs	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	★	941	1209
0B	Spare (B)	697	1633
0C	Spare (C)	770	1633
0D	Spare (D)	852	1633
0E	#	941	1477
0F	Spare (F)	941	1633
10	1300 Hz Calling Tone		

TONE DETECTION

The R2424 detects tones in the 340 ±5 Hz to 640 ±5 Hz band.
Detection Level: −10 dBm to −43 dBm
Response Time: 17 ±2 ms

SIGNALING AND DATA RATES

The signaling and data rates for the R2424 are defined in Table 3.

Table 3. Signaling and Data Rates

Operating Mode	Signaling Rate (Baud)	Data Rate
V.22 bis	600	Synchronous/Asynchronous, 2400 bps ±0.01%
V.22 bis	600	Synchronous/Asynchronous, 1200 bps ±0.01%
V.22:		
(Alternative A)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0.01% Synchronous
(Alternative B)		
Mode i	600	1200 bps ±0.01% Synchronous
Mode iii	600	600 bps ±0 01% Synchronous
Mode ii		1200 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character
Mode iv		600 bps Asynchronous, 8, 9, 10 or 11 Bits Per Character
Bell 212A;	600	1200 bps ±0.01%, Synchronous/Asynchronous
	0 to 300	0 to 300 bps Asynchronous

DATA ENCODING

The specifications for data encoding are as follows:

1. *2400 bps (V.22 bis).* The transmitted data is divided into groups of four consecutive bits (quad bits) forming a 16-point signal structure.
2. *1200 bps (V.22 and Bell 212A).* The transmitted data is divided into groups of two consecutive bits (dibits) forming a four-point signal structure.
3. *600 bps (V.22).* Each bit is encoded as a phase change relative to the phase preceding signal elements.

EQUALIZERS

The R2424 provides equalization functions that improve performance when operating over low quality lines.

Automatic Adaptive Equalizer—An automatic adaptive equalizer is provided in the receiver circuit for V.22 bis, V.22 and Bell 212A configurations.

Fixed Compromise Equalizer—A fixed compromise equalizer is provided in the transmitter.

TRANSMITTED DATA SPECTRUM

After making allowance for the nominal specified compromise equalizer characteristic, the transmitted line signal has a frequency spectrum shaped by the square root of a 75 percent raised cosine filter. Similarly, the group delay of the transmitter output is within ±150 microseconds over the frequency range 900 to 1500 Hz (low channel) and 2100 to 2700 Hz (high channel).

SCRAMBLER/DESCRAMBLER

The R2424 incorporates a self-synchronizing scrambler-/descrambler. In accordance with the CCITT V.22 bis, V.22 and the Bell 212A recommendations.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R2424 can adapt to received frequency errors of up to ±7 Hz with less than a 0.2 dBm degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R2424 satisfies all specified performance requirements for the received line signals from −10 dBm to −48 dBm. The received line signal is measured at the receiver analog input RXA.

TRANSMIT LEVEL

The R2424M output control circuitry contains a variable gain buffer which reduces the modem output level. The R2424M can be strapped via the host interface memory to accomplish this.

PERMISSIVE/PROGRAMMABLE CONFIGURATIONS

The R2424M transmit level is +6 dBm to allow a Data Access Arrangement (DAA) to be used. The DAA then determines the permissive or programmable configuration.

The R2424DC transmit level is strapped in the permissive mode so that the maximum output level is −10 dBm ±1.0 dBm.

AUTOMATIC RECONFIGURATION

The R2424 is capable of automatically configuring itself to the compatibility of a remote modem. The R2424 can be in either the answer or originate mode for this to occur. The R2424 adaptation compatibilities are limited to V.22 bis, V.22 A/B (1200 bps), Bell 212, and Bell 103. If the R2424 is to originate in a specific configuration, the MODE bits (see Interface Memory Definitions)must be set.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, DAA signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The column titled "Type" refers to designations found in the Hardware Circuits Interface Characteristics (Tables 5 and 6). The six groups of hardware circuits are described in the following paragraphs.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives pin 13C to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 13C, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 13C low for at least 3 μs. When an external low input is applied to pin 13C, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 13C is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The R2424 POR sequence leaves the modem configured as follows:

- 2400 bps
- Asynchronous
- 10-bit Character Length
- Constant Carrier
- Serial Mode
- Answer Mode
- Auto Answer Disabled
- RAM Access Code = 00

This configuration is suitable for performing high speed data transfer over the public switched telephone network using the serial data port. Individual features are discussed in subsequent paragraphs.

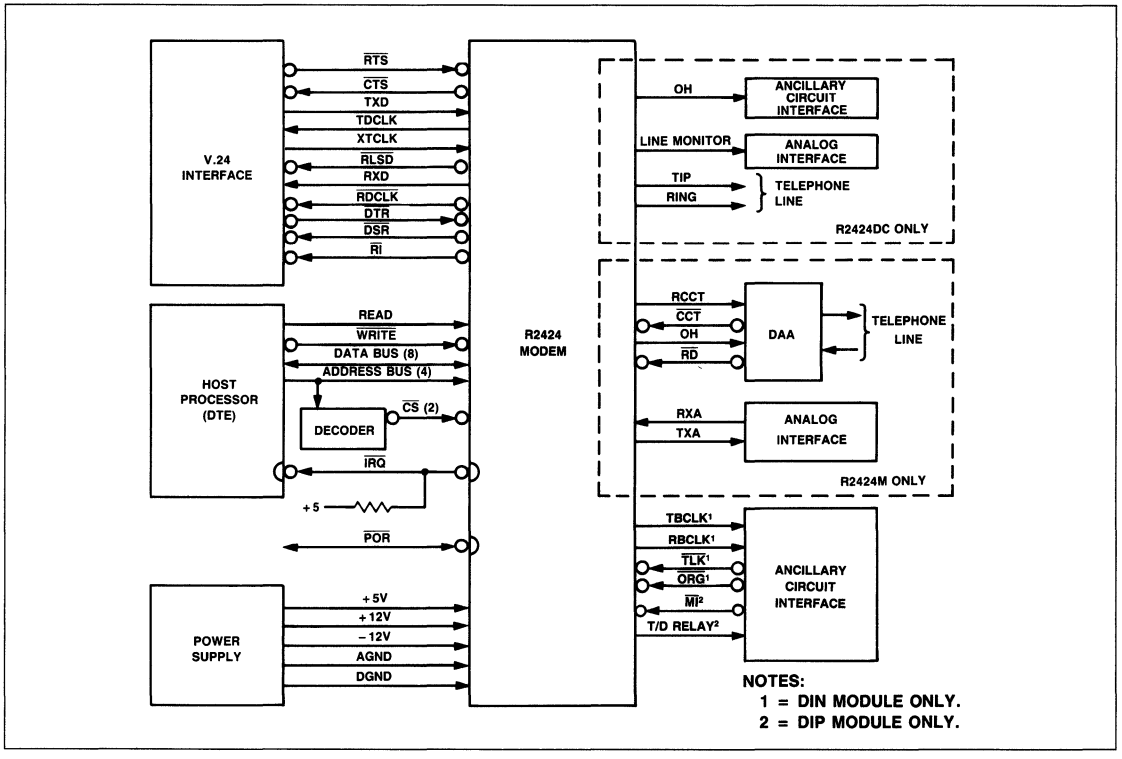


Figure 1. R2424 Modem Functional Interconnect Diagram

Table 4. Hardware Circuits

Name	Type	DIN Pin No.	DIP Pin No.	Description
A. OVERHEAD SIGNALS				
Ground (A)	AGND	31C, 32C	21, 26, 39	Analog Ground Return
Ground (D)	DGND	3C, 8C, 5A, 10A	20, 40, 51, 60	Digital Ground Return
+5 volts	PWR	19C, 23C, 26C, 30C	1, 19, 61	+5 volt supply
+12 volts	PWR	15A	22	+12 volt supply
−12 volts	PWR	12A	25	−12 volt supply
$\overline{POR}$	I/OB	13C	13	Power-on-Reset
B. MICROPROCESSOR INTERFACE SIGNALS				
D7	I/OA	1C	52	Data Bus (8-Lines)
D6	I/OA	1A	53	
D5	I/OA	2C	54	
D4	I/OA	2A	55	
D3	I/OA	3A	56	
D2	I/OA	4C	57	
D1	I/OA	4A	58	
D0	I/OA	5C	59	
RS3	IA	6C	45	Register Select (4-Lines)
RS2	IA	6A	44	
RS1	IA	7C	43	
$\overline{RS0}$	IA	7A	42	
$\overline{CS0}$	IA	10C	48	Chip Select Receiver (Baud Rate Device)
$\overline{CS1}$	IA	9C	41	Chip Select Transmitter (Sample Rate Device)
$\overline{READ}$	IA	12C	47	Read Enable
$\overline{WRITE}$	IA	11A	49	Write Enable
$\overline{IRQ}$	OB	11C	50	Interrupt Request

Name	Type	DIN Pin No.	DIP Pin No.	Description
C. V.24 INTERFACE SIGNALS				
XTCLK	IB	22A	3	External Transmit Clock
TDCLK	OC	23A	7	Transmit Data Clock
$\overline{RDCLK}$	OC	21A	8	Receive Data Clock
$\overline{RTS}$	IB	25A	4	Request-to-Send
$\overline{CTS}$	OC	25C	5	Clear-to-Send
TXD	IB	24C	6	Transmit Data
RXD	OC	22C	9	Receive Data
$\overline{RLSD}$	OC	24A	10	Received Line Signal Detector
$\overline{DTR}$	IB	21C	12	Data Terminal Ready
$\overline{DSR}$	OC	20A	11	Data Set Ready
$\overline{RI}$	OC	18A	2	Ring Indicator
D. ANALOG SIGNALS				
RXA (M)	IB	32A	23	Receive Analog Input
TXA (M)	OC	31A	24	Transmit Analog Output
TIP/RING (DC) LINE	AE	RJ11 Jacks	—	Phone Line Interface
MONITOR (DC)	AD	30A	—	Analog Line Monitor
E. DAA INTERFACE SIGNALS				
$\overline{RD}$ (M)	IB	27A	35	Ring Detect
RCCT (M)	OC	28A	—	Request Coupler Cut Through
$\overline{CCT}$ (M)	IB	29C	—	Coupler Cut Through
OH	OC	29A	36	Off-Hook Relay Status
T/D Relay	OC	—	37	Talk/Data Relay
$\overline{MI}$	IC	—	38	Manual Input
F. ANCILLARY INTERFACE SIGNALS				
TBCLK	OC	27C	—	Transmit Baud Clock
RBCLK	OC	26A	—	Receive Baud Clock
$\overline{TLK}$	IC	28C	—	Talk (TLK = Data)
$\overline{ORG}$	IB	16C	—	Originate (ORG = Answer)
(M) R2424M Only, (DC) R2424DC Only, — = not applicable				

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Ouput Type IA	IB	IC	OA	OB	OC	I/O A	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min.				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min.[2]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±2.5 max [4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive Circuit Type	pF	TTL	TTL w/Pull-up	TTL w/Pull-up	100 TTL	100 Open-Drain	100 Open-Drain w/Pull-up	100 3 State Transceiver	100 Open-Drain w/Pull-up

Notes: 1. I load = −100 μA 2. I load = 1.6 mA 3. I load = −40 μA 4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5 25 Vdc 5. I load = 0.36 mA

Table 6. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604Ω ±1% with an output level of +6 dBm. To obtain a 0 dBm output, a 600Ω load to ground is needed.
RXA	AB	The receiver input impedance is 23.7 KΩ ±1%. The receive level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled).
LINE MONITOR	AD	The line monitor output impedance is 15 KΩ ±5%.
TIP/RING	AE	The impedance of TIP with respect to RING is 600 Ω.

V.24 INTERFACE

Eleven hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, +5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Data Terminal Ready ($\overline{DTR}$)

$\overline{DTR}$ prepares the modem to be connected to the communications channel, and maintains the connection established by the DTE (manual answering) or internal (automatic answering) means. $\overline{DTR}$ OFF places the modem in the disconnect state.

Data Set Ready ($\overline{DSR}$)

Data Set Ready ($\overline{DSR}$) ON indicates that the modem is in the data transfer state. $\overline{DSR}$ OFF is an indication that the DTE is to disregard all signals appearing on the interchange circuits—except $\overline{RI}$. $\overline{DSR}$ will switch to the OFF state when in test state. The ON condition of $\overline{DSR}$ indicates the following:

1. The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line.
2. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing.
3. The modem has generated an answer tone or detected answer tone.
4. After ring indicate ($\overline{RI}$) goes ON, $\overline{DSR}$ waits at least two seconds before turning ON to allow the telephone company equipment to be engaged.

$\overline{DSR}$ will go OFF 50 ms after $\overline{DTR}$ goes OFF, or 50 ms plus a maximum of 4 seconds when the SSD bit is enabled.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. In constant carrier mode, $\overline{RTS}$ can be wired to $\overline{DTR}$. In controlled carrier operation, independent operation of $\overline{RTS}$ turns the carrier ON and OFF. The responses to $\overline{RTS}$ are shown in Table 7 (assume the modem is in data mode).

Table 7. $\overline{RTS}$ Responses

Leased or Dial Line[1]	$\overline{RTS}$ OFF	$\overline{RTS}$ ON
Controlled Carrier	$\overline{CTS}$ OFF Carrier OFF	Carrier ON 210 to 275 ms Scrambled 1s Transmitted $\overline{CTS}$ ON
Constant Carrier	$\overline{CTS}$ OFF Carrier ON Scrambled 1s Transmitted	$\overline{CTS}$ ON Carrier ON Data Transmitted
Note: 1. After handshake is complete.		

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON or OFF condition of $\overline{RTS}$ are shown in Table 8.

Table 8. $\overline{CTS}$ Response Times

$\overline{CTS}$ Transition	Constant Carrier	Controlled Carrier
OFF to ON ON to OFF	<2 ms <20 ms*	210 to 275 ms <20 ms*
Note: *Programmable		

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 2400 Hz, 1200 Hz or 600 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

TDCLK is provided to the user in both asynchronous and synchronous communications. TDCLK is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing (TDCLK is not valid in FSK). TDCLK is necessary for synchronous communication. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{\text{RDCLK}}$)

The modem provides a Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±.035% (relative) frequency error in the associated transmit timing source.

$\overline{\text{RDCLK}}$ is provided to the user in both asynchronous and synchronous communications. $\overline{\text{RDCLK}}$ is not necessary in asynchronous communication but it can be used to supply a clock for UART/USART timing ($\overline{\text{RDCLK}}$ is not valid in FSK). RDCLK is necessary for synchronous communication.

Received Line Signal Detector ($\overline{\text{RLSD}}$)

The $\overline{\text{RLSD}}$ thresholds for both high and low channels are:

$\overline{\text{RLSD}}$ ON ≥ −43 dBm
$\overline{\text{RLSD}}$ OFF ≤ −48 dBm

$\overline{\text{RLSD}}$ will not respond to guard tones or answer tones.

When $\overline{\text{RLSD}}$ is active, it indicates to the terminal equipment that valid data is available on RXD.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Ring Indicator ($\overline{\text{RI}}$)

The modem provides a Ring Indicator ($\overline{\text{RI}}$) output; its low state indicates the presence of a ring signal on the line. The low condition appears approximately coincident with the ON segment of the ring cycle (during rings) on the communication channel. (The ring signal cycle is typically two seconds ON, four seconds OFF.) The high condition of the $\overline{\text{RI}}$ output is maintained during the OFF segment of the ring cycle (between rings) and at all other times when ringing is not being received. The operation of $\overline{\text{RI}}$ is not disabled by an OFF condition on $\overline{\text{DTR}}$.

$\overline{\text{RI}}$ will respond to ring signals in the frequency range of 15.3 Hz to 68 Hz with voltage amplitude levels of 40 to 150 Vrms (applied across TIP and RING), with the response times given in Table 13.

This OFF-to-ON (ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent ON (OFF) transition of $\overline{\text{RI}}$.

Table 9. $\overline{\text{RI}}$ Response Time

$\overline{\text{RI}}$ Transition	Response Time
OFF-to-ON*	110 ±50 ms (50% duty cycle)
ON-to-OFF	450 ±50 ms
Note: *The OFF-to-ON time is duty cycle dependent: 890 ms (15%) ≥ time ≥ 50 ms (100%)	

MICROPROCESSOR INTERFACE

Seventeen hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{CS0}$ and $\overline{CS1}$) and Register Selects (RS0-RS1)

The signal processor to be accessed is selected by grounding one of two unique chip select lines, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable ($\overline{READ}$) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ line high or the $\overline{WRITE}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to + 5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

DAA INTERFACE

The R2424M provides a Data Access Arrangement (DAA) interface that is directly hardware and software compatible with the RDAA. Manual/automatic originate and answer are then controlled via the appropriate R2424M hardware ancillary circuits or software control bits. The modem provides the only interface with the microprocessor (MPU) bus, i.e., no RDAA interface signals must be directly controlled from the MPU bus.

Ring Detect ($\overline{RD}$)

$\overline{RD}$ indicates to the modem by an ON (low) condition that a ringing signal is present. The signal (a 4N35 optoisolator compatible output) into the $\overline{RD}$ input should not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40 Vrms, 15 to 68 Hz, appearing across TIP and RING with respect to ground. The ring is then reflected on $\overline{RI}$.

Request Coupler Cut Through (RCCT)

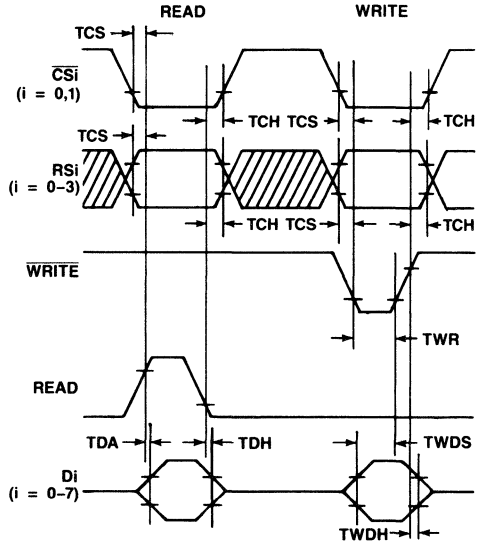
RCCT is used to request that a data transmission path through the DAA be connected to the telephone line. When RCCT goes OFF (low), the cut-through buffers are disabled and $\overline{CCT}$ should go OFF (high). RCCT should be OFF during dialing but ON for tone address signaling.

Coupler Cut Through ($\overline{CCT}$)

An ON (low) signal to the $\overline{CCT}$ lead indicates to the modem that the data transmission path through the DAA is connected. This input can always be grounded if the two second billing delay squelch is desired. If $\overline{CCT}$ is user controlled, the billing delay squelch can only be 2 seconds or greater.

Off-Hook Relay Status (OH)

The modem provides an OH output which indicates the state of the OH relay. A high condition on OH implies the OH relay is closed and the modem is connected to the telephone line (off-hook). A low condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.



Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
$\overline{CSi}$, RSi hold time after Read or $\overline{Write}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram

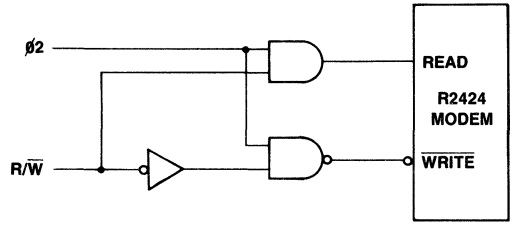


Figure 3. R/$\overline{W}$ to READ $\overline{WRITE}$ Conversion Logic

ANALOG SIGNALS (R2424M)

Two connections are devoted to analog audio signals: TXA and RXA.

Transmit Analog (TXA)

The TXA output is suitable for driving a data access arrangement for connection to either leased lines or the public switched telephone network. The transmitter output impedance is 604 ohms ±1% with an output level of +6 dBm ±1 dBm. To obtain a 0 dBm output, a 600 ohm load to ground is needed.

Receive Analog (RXA)

RXA is an input to the receiver from a data access arrangement. The input impedance is 23.7K ohms ±1%. The received level at RXA must be no greater than −9 dBm (or −6 dBm with the 3DB bit enabled).

ANALOG SIGNALS (R2424DC)

Three analog signals are output by the R2424DC: LINE MONITOR, TIP and RING.

Analog Line Monitor (LINE MONITOR)

The LINE MONITOR output is suitable for a speaker interface. It provides an output for all dialing signals, call progress signals, and the carrier signals. The output impedance is 15K ohms ±1%. The signals which appear on LINE MONITOR are approximately the same level as the signals would appear on the network (assuming a 1 dB loss attributed to the audio transformer).

Phone Line Interface (TIP and RING)

TIP and RING are the DAA analog outputs to the public switched telephone network. These outputs use two RJ11 jacks in parallel as the interface to the network (see Table 10 and Figure 4). The R2424DC, which contains the DAA TIP and RING interface, has been FCC Part 68 approved. The user need not apply for further Part 68 approval. The impedance of TIP with respect to RING is 600 ohms.

Table 10. R2424DC Network Interface

Connector Type	Pin Number	Name	Function
RJ11 Jack	3	RING	One Side of TELCO Line
	4	TIP	One Side of TELCO Line

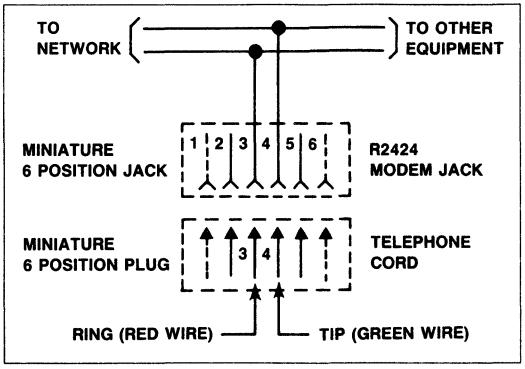


Figure 4. RJ11 Telephone Jack

ANCILLARY CIRCUITS

Transmit Baud Clock (TBCLK) and Received Baud Clock (RBCLK)

TBCLK and RBCLK are provided to the user at the baud rate (600 Hz).

Talk ($\overline{TLK}$) (DIN Module Only)

$\overline{TLK}$ is an input which manually places the modem on-hook (relay open, $\overline{TLK}$ = 0) or off-hook (relay closed, $\overline{TLK}$ = 1). The on-hook condition is referred to as TALK mode and the off-hook condition is referred to as DATA mode. $\overline{TLK}$ is used with $\overline{ORG}$ to manually originate or answer a call. $\overline{TLK}$ should be 0 at power-on or reset to prevent the modem from inadvertently entering the data mode.

Originate ($\overline{ORG}$)

$\overline{ORG}$ is an input which manually places the modem in the originate mode ($\overline{ORG}$ = 0) or the answer mode ($\overline{ORG}$ = 1). To manually originate a call, $\overline{ORG}$ = 0 and $\overline{TLK}$ = 0. Dial the number using the telephone. When the other modem answers and sends answer tone switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook.

To manually answer a call $\overline{ORG}$ = 1 and $\overline{TLK}$ = 0. When the phone rings switch the $\overline{TLK}$ input from 0 to 1 placing the modem off-hook.

Off-Hook Relay Status (OH)

The modem provides an OH output which indicates the state of the OH relay. A high condition on OH implies the OH relay is closed and the modem is connected to the telephone line (off-hook). A low condition on OH implies the OH relay is open (i.e., the modem is on-hook). The delay between the low-to-high or high-to-low transition of OH and the subsequent close-to-open or open-to-close transition of the OH relay is 8 ms maximum.

T/D Relay. (DIP Module Only)

The T/D Relay signal may be used as a second relay control when the parallel control mode of operation is selected (BUS bits 0 and 1 = 1). If the serial control mode is selected (BUS bits 0 and 1 = 0) the T/D relay follows the status of the OH output signal which is controlled by the $\overline{MI}$ signal. In the parallel control mode the OH output signal is controlled by the status of the DATA bit, while independent control of the T/D relay is provided by the $\overline{MI}$ signal. During pulse dialing the OH signal reflects the pulse signals being dialed. It is therefore possible to use the T/D Relay signal to control the off-hook relay and use the OH signal to perform pulse dialing on a separate, independent relay.

Manual Input ($\overline{MI}$) (DIP Module Only)

$\overline{MI}$ is an input which manually places the modem on-hook (relay open, $\overline{MI}$ = 0) or off-hook (relay closed, $\overline{MI}$ = 1). The on-hook condition is referred to as TALK mode and the off-hook condition is referred to as DATA mode. $\overline{MI}$ is used with $\overline{ORG}$ to manually originate or answer a call. $\overline{MI}$ should be 0 at power-on or reset to prevent the modem from inadvertently entering the data mode.

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load-/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on two special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into two areas. These areas are partitioned into receiver and transmitter devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 32 addressable registers in the modem receiver (CS0) and transmitter (CS1) interface memory are shown in Figures 5 and 6, respectively. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Figures 7 and 8 show the registers according to the overall function they perform in the receiver and transmitter, respectively. Figures 9 through 12 show the power on configurations of the interface memory bits for the R2424/US and the R2424/INT versions.

Table 11 defines the individual bits in the interface memory. In the Table 11 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R							
E	IRQ	ENSI	NEWS	—	NEWC	—	—	—
D	BUS	CRQ	—	—	—	LCD	RSD	—
C	—	—	—	CHAR		—	—	—
B	—	—	—	—	—	—	—	AL
A	ERDL	RDL	DL	ST	MODE			
9	—	—	SPEED		—	—	—	—
8	TONE	ATD	—	—	—	—	TM	RLSD
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (YRAMRM)							
4	RAM Data YRL (YRAMRL)							
3	RAM Data XRM (XRAMRM)							
2	RAM Data XRL (XRAMRL)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—

Note
(—) Indicates reserved for modem use only.

Figure 5. Receiver ($\overline{CS0}$) Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T							
E	IRQ	ENSI	NEWS	—	NEWC	DDEI	—	DDRE
D	BUS	CRQ	DATA	AAE	DTR	—	—	SSD
C	DSRA	TXCLK		CHAR		—	—	DLSF[1]
B	TX LEVEL			GTE	GTS	3DB	DTMF	AL
A	ERDL	RDL	DL	ST	MODE			
9	NAT[1]	RTRN	ORG	LL	RTS	CC	EF	NTS
8	DLO	CTS	DSR	RI	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (YRAMTM)							
4	RAM Data YTL (YRAMTL)							
3	RAM Data XTM (XRAMTM)							
2	RAM Data XTL (XRAMTL)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register							

Notes
1. Not valid before R5310-22
(—) Indicates reserved for modem use only.

Figure 6. Transmitter ($\overline{CS1}$) Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	DIAGNOSTIC CONTROL							
E	HANDSHAKE							
D	CONFIGURATION							
C	CONFIGURATION							
B	CONFIGURATION							
A	CONFIGURATION							
9	STATUS							
8	STATUS							
7	RESERVED							
6	RESERVED							
5	DIAGNOSTIC							
4	DIAGNOSTIC							
3	DIAGNOSTIC							
2	DIAGNOSTIC							
1	RESERVED							
0	RESERVED							
Register / Bit	7	6	5	4	3	2	1	0

Figure 7. Receiver ($\overline{CS0}$) Interface Memory Functions

Register \ Bit	7	6	5	4	3	2	1	0
F	DIAGNOSTIC CONTROL							
E	HANDSHAKE							
D	CONFIGURATION							
C	CONFIGURATION							
B	CONFIGURATION							
A	CONFIGURATION							
9	CONFIGURATION							
8	STATUS							
7	RESERVED							
6	RESERVED							
5	DIAGNOSTIC							
4	DIAGNOSTIC							
3	DIAGNOSTIC							
2	DIAGNOSTIC							
1	RESERVED							
0	DIAL DIGIT REGISTER							
Register / Bit	7	6	5	4	3	2	1	0

Figure 8. Transmitter ($\overline{CS1}$) Interface Memory Functions

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	—	—	—
D	BUS 0	CRQ 0	—	—	—	LCD 1	RSD 0	—
C	—	—	—	CHAR 1	0	—	—	—
B	—	—	—	—	—	—	—	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	0	MODE 0	0	1
9	—	—	SPEED 0	0	—	—	—	—
8	TONE 0	ATD 0	—	—	—	—	TM 0	RLSD 0
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (Random)							
4	RAM Data YRL (Random)							
3	RAM Data XRM (Random)							
2	RAM Data XRL (Random)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 9. R2424/US Receiver ($\overline{CS0}$) Interface Memory Power On Configuration

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	DDEI 0	—	DDRE 0
D	BUS 0	CRQ 0	DATA 0	AAE 0	DTR 0	—	—	SSD 0
C	DSRA 0	TX CLK 0	0	CHAR 1	0	—	—	DLSF 0
B	TX LEVEL 0	0	0	GTE 0	GTS 0	3DB 0	DTMF 0	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	MODE 1	1	0	1
9	NAT 0	RTRN 0	ORG 0	LL 0	RTS 0	CC 0	EF 0	NTS 0
8	DLO 0	CTS 0	DSR 0	RI 0	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (Random)							
4	RAM Data YTL (Random)							
3	RAM Data XTM (Random)							
2	RAM Data XTL (Random)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register (Write-Only Register)							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 10. R2424/US Transmitter ($\overline{CS1}$) Interface Memory Power On Configuration

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access R 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	—	—	—
D	BUS 0	CRQ 0	—	—	—	LCD 1	RSD 0	—
C	—	—	—	CHAR 1	0	—	—	—
B	—	—	—	—	—	—	—	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	1	MODE 1	0	1
9	—	—	SPEED 0	0	—	—	—	—
8	TONE 0	ATD 0	—	—	—	—	TM 0	RLSD 0
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YRM (Random)							
4	RAM Data YRL (Random)							
3	RAM Data XRM (Random)							
2	RAM Data XRL (Random)							
1	—	—	—	—	—	—	—	—
0	—	—	—	—	—	—	—	—
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 11. R2424/INT Receiver ($\overline{CS0}$) Interface Memory Power On Configuration

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM Access T 0	0	0	0	0	0	0	0
E	IRQ 0	ENSI 0	NEWS 0	—	NEWC 0	DDEI 0	—	DDRE 0
D	BUS 0	CRQ 0	DATA 0	AAE 0	DTR 0	—	—	SSD 0
C	DSRA 0	TX CLK 0	0	CHAR 1	0	—	—	DLSF 0
B	TX LEVEL 0	0	0	GTE 0	GTS 0	3DB 0	DTMF 0	AL 0
A	ERDL 0	RDL 0	DL 0	ST 0	MODE 1	1	0	1
9	NAT 0	RTRN 0	ORG 0	LL 0	RTS 0	CC 0	EF 0	NTS 0
8	DLO 0	CTS 0	DSR 0	RI 0	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM Data YTM (Random)							
4	RAM Data YTL (Random)							
3	RAM Data XTM (Random)							
2	RAM Data XTL (Random)							
1	—	—	—	—	—	—	—	—
0	Dial Digit Register (Write-Only Register)							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 12. R2424/INT Transmitter ($\overline{CS1}$) Interface Memory Power On Configuration

Table 11. Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
AAE	Auto Answer Enable	1:D:4	When configuration bit AAE is a 1, the modem will automatically answer when a ringing signal is present on the line. When AAE is set to a 1, the modem will answer after one ring and go into data mode The modem goes off-hook 1 second after the on-to-off transition of the ring The $\overline{ORG}$ pin or ORG bit need not to be set to the answer polarity. If it is desired to answer after more than one ring, then the user must use the alternative answer method described under the DATA bit. The $\overline{DTR}$ pin or the DTR bit must also be set before the modem will auto answer. Writing a 0 into the AAE bit will cause the modem to go on-hook. This will occur only when the modem auto answers using the AAE bit.
AL	Analog Loopback	(0,1):B:0	When configuration bits AL are a 1, the modem is in local analog loopback (V.54 Loop 3). In this loop, the transmitter's analog output is coupled to the receiver's analog input at a point near the modem's telephone line interface An attenuator is introduced into the loop such that the signal level coupled into the receive path is attenuated 14 ±1 dBm. The modem may be placed into analog loopback in either the idle mode or the data mode However, in the data mode, setting the AL bits to a 1 will terminate the connection Analog loopback will only function in the high speed modes (2400, 1200, or 600 bps). The DTE may be tested when the modem is in analog loopback. Also, all parts of the modem except the line interface are checked If no DTE is connected, the modem integrity may be verified by use of the self test function. When entering analog loopback, set AL in the receiver to a 1 before setting AL in the transmitter to a 1 When exiting analog loopback, reset AL in the transmitter to a 0 before resetting AL in the receiver to a 0.
ATD	Answer Tone Detected	0:8:6	When status bit ATD is a 1, it signifies that the modem receiver detected the answer tone. The bit is 1 set 75 ms after the answer tone is first detected, and is cleared to a 0 when the modem goes on-hook The user may clear ATD manually after CTS is active.
BUS	Bus Select	(0,1):D:7	When configuration bits BUS are a 1, the modem is in the parallel control mode; and when 0, the modem is in the serial control mode BUS can be in either state to configure the modem. *Serial Control Mode* The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. The control signals used in serial control mode are $\overline{DTR}$, $\overline{RTS}$, $\overline{TLK}$, and $\overline{ORG}$. Outputs such as $\overline{RLSD}$ and $\overline{DSR}$ are reflected both in the interface memory and the V.24 interface. Once the bus bits have been set to a 0, the state of the DTR, RTS, DATA, and ORG bits are ignored. *Parallel Control Mode* The modem has the capability of modem control via the microprocessor bus Data transfer is maintained over the serial V.24 channel The control bits used in parallel control are DTR, RTS, ORG, and DATA. The modem automatically defaults to the serial mode at power-on. If the parallel control mode is to be used, it is recommended that the $\overline{TLK}$ pin be tied to ground A floating $\overline{TLK}$ pin will assume a logic 1 which will immediately put the modem into the data mode before the BUS bits are set In either mode, the modem is configured by the host processor via the microprocessor bus

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
CC	Controlled Carrier	1:9:2	When configuration bit CC is a 1, the modem operates in controlled carrier; when 0, the modem operates in constant carrier. Controlled carrier allows the modem transmitter to be controlled by the $\overline{RTS}$ pin or the RTS bit. Its effect may be seen in the RTS and CTS descriptions.
CHAR	Character Length Select	(0,1):C:(3,4)	These character length bits select either 8, 9, 10, or 11 bit characters (includes data, stop, and start bits) as shown below: **Configuration Word** (4 3) → **Configuration** 0 0 → 8 bits 0 1 → 9 bits 1 0 → 10 bits 1 1 → 11 bits It is possible to change character length during the data mode. Errors in the data will be expected between the changeover and the resynchronization (which occurs on the next start bit after the change is implemented).
CRQ	Call Request	(0,1):D:6	When configuration bit CRQ in chip 1 (the transmitter) is a 1, it places the transmitter in auto dial mode. The data then placed in the Dial Digit Register is treated as digits to be dialed. The format for the data should be a hex representation of the number to be dialed (if a 9 is to be dialed then an 09_{16} should be loaded in DDR) CRQ in chip 1 should be a 1 for the duration of the data mode. If CRQ in chip 1 is changed to a 0, the modem will go on-hook. Also, see DDRE bit. When configuration bit CRQ in chip 0 (the receiver) is a 1, the receiver goes into tone detect mode. Any energy above threshold and in the 345 to 635 Hz bandwidth is reflected by the TONE bit. CRQ in chip 0 must be reset to a 0 (after the last digit was dialed and tone detection completed) before the answer tone is sent by the answering modem (after ringback is detected). CRQ in chip 0 need not be used during auto dialing, but may be used to provide call progress information as part of an intelligent auto dialing routine. An example flowchart is given in Figure 13. FF (hex) should be loaded into the Dial Digit Register after the last digit is dialed and tone detection is completed. This action also puts the modem in data mode and starts a 30 second abort timer. If the handshake has not been completed in 30 seconds the modem will go on-hook.
CTS	Clear-to-Send	1:8:6	When status bit CTS is a 1, it indicates to the terminal equipment that the modem will transmit any data which are present at TXD. CTS response times from an ON or OFF condition of RTS are shown below: **CTS Transition** / **Constant Carrier** / **Controlled Carrier** OFF to ON: ≤2 ms / 210 to 275 ms ON to OFF: ≤20 ms* / ≤20 ms* *Programmable
DATA	Talk/Data	1:D:5	When control bit DATA is a 1, the modem is in the data state (off-hook); and when 0, the modem is in the talk state (on-hook). This bit allows the modem to go off-hook after a programmable number of rings by counting the required number of RI bit transitions and then setting the DATA bit (assuming ORG = 0).
DDEI	Dial Digit Empty Interrupt	1:E:2	When handshake bit DDEI is a 1, an interrupt will occur when the Dial Digit Register (1:0) is empty (DDRE = 1). This is independent of the state of the ENSI bit. The interrupt will set the IRQ bit and also assert the $\overline{IRQ}$ signal. Loading the Dial Digit Register with a new digit will clear the interrupt condition.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DDR	Dial Digit Register	1:0:(0–7)	DDR is used to load the digits to be dialed. Example: If a 4 is to be dialed, an 04 (hex) should be loaded. This action also causes the interrupt to be cleared. The modem automatically accounts for the interdigit delay. Note: DDR is a write-only register
DDRE	Dial Digit Register Empty	1:E:0	When handshake bit DDRE is a 1, it indicates that the dial digit register is empty and can be loaded with a new digit to be dialed. If the DDEI bit is set, the IRQ bit will be set when the DDRE bit is set. Also, the $\overline{IRQ}$ signal will be generated. After the DDR is loaded, DDRE goes to a 0 and the interrupts are automatically cleared.
DL	Digital Loopback (Manual)	(0,1):A:5	When configuration bits DL are set to a 1, the modem is manually placed in digital loopback. DL should only be set during the data mode. The DSR and CTS bits will be reset to a 0. The local modem can then be tested from the remote modem end by looping a remotely generated test pattern. At the remote modem, all interface circuits behave normally as in the data mode. At the conclusion of the test, DL must be reset to a 0. The local modem will then return to the normal data mode with control reverting to the DTEs, DTR. DL does not function in 300 bps.
DLO	Dial Line Occupied	1:8:7	When status bit DLO is a 1, it indicates that the modem is in the auto dial state, i.e., CRQ in the transmitter is a 1 and the modem is off-hook and ready to dial.
DLSF	Disable Low Speed Fallback	1:C:0	When configuration bit DLSF is a 1, the modem will not automatically fallback to the 300 bps operating mode if it is configured for another data rate. This bit is valid in originate mode only.
DSR	Data Set Ready	1:8:5	The ON condition of the status bit DSR indicates that the modem is in the data transfer state. The OFF condition of DSR is an indication that the DTE is to disregard all signals appearing on the interchange circuits — except RI DSR will switch to the OFF state when in test state. The ON condition of DSR indicates the following: The modem is not in the talk state, i.e., an associated telephone handset is not in control of the line. The modem is not in the process of automatically establishing a call via pulse or DTMF dialing. The modem has generated an answer tone or detected answer tone. After ring indicate goes ON, DSR waits at least two seconds before turning ON to allow the telephone company equipment to be engaged DSR will go OFF 50 msec after DTR goes OFF, or 50 msec plus a maximum of 4 sec when the SSD bit is enabled.
DSRA	Data Set Ready in Analog Loopback	1:C:7	When configuration bit DSRA is a 1, it causes DSR to be ON during analog loopback.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
DTMF	Touch Tones/Pulse Dialing	1:B:1	When configuration bit DTMF is a 1, it tells the modem to auto dial using tones; and when 0, the modem will dial using pulses. The timing for the pulses and tones are as follows (power-on timing): Pulses — Relay open 64 ms Relay closed 36 ms Interdigit delay 750 ms Tones — Tone duration 95 ms Interdigit delay 70 ms The DTMF bit can be changed during the dialing process to allow either tone or pulse dialing of consecutive digits. The output power level of the DTMF tones is as follows: ±15 dBm ±1 measured at TXA for the R2424M −1 dBm ±1 measured at TIP/RING for the R2424DC
DTR	Data Terminal Ready	1:D:3	Control bit DTR must be a 1 for the modem to enter the data state, either manually or automatically. DTR must also be a 1 in order for the modem to automatically answer an incoming call. During the data mode, DTR must remain at a 1, otherwise the connection will be terminated if DTR resets to a 0 for greater than 50 ms.
EF	Enable Filters	1:9:1	Setting CRQ in the transmitter to a 1 disables the high and low band filters used in data mode so that call progress tone detection can be done. Setting CRQ in the receiver to a 1 inserts a passband filter in the receive path which passes energy in the 345 Hz to 635 Hz bandwidth. The high and low band filters must be enabled and the passband filter disabled for the answer tone and carrier to be detected. This occurs automatically during the auto dial process when EF is set to a 0. In this case, the high and low band filters are disabled when CRQ in the transmitter is set to a 1. If tone detection is required, CRQ in the receiver should be set to a 1. After dialing and call progress tone detection, CRQ in the receiver is set to a 0 and FF is loaded into the dial digit register. (Loading FF enables the high and low band filters). At this time, the answer tone can be detected. To re-enable the high and low band filters disabled by setting CRQ in the transmitter, set EF to a 1. After CRQ in the transmitter and receiver is set to a 1 and tone detection is completed, it may be necessary to detect the answer tone before loading FF into the dial digit register (see the section on sending 1300 Hz calling tone). At that point, EF can be set to a 1 and CRQ in the receiver set to a 0 so the answer tone can be detected (using the ATD bit) and the 1300 Hz calling tone can still be sent. Once the answer tone is detected, FF should be loaded into the dial digit register and the EF bit set to a 0.
ENSI	Enable New Status Interrupt	(0,1):E:6	When handshake bit ENSI is a 1, it causes an interrupt to occur when the status bits in registers (0:[8,9]) and (1:8) are changed by the modem. (NEWS = 1). The IRQ bit will be set to a 1 and the $\overline{IRQ}$ signal will be generated. The interrupt is cleared by writing a 0 into the NEWS bit.
ERDL	Enable Response to Remote Digital Loopback	(0,1):A:7	When configuration bits ERDL are a 1, it enables the modem to respond to another modem's remote digital loopback request, thus going into loopback. When this occurs, the modem clamps RXD to a mark; resets the CTS, DSR and RLSD bits to a 0 and turns the $\overline{CTS}$, $\overline{DSR}$ and $\overline{RLSD}$ signals to a logic 1. The TM bit is set to inform the user of the test status. When the ERDL bits are a 0, no response will be generated.
GTE	Guard Tone Enable	1:B:4	When configuration bit GTE is a 1, it causes the specified guard tone to be transmitted (CCITT configurations only), according the state of the GTS bit. Note: The guard tone will only be transmitted by the answering modem.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
GTS	Guard Tone Select	1:B:3	When configuration bit GTS is a 0, it selects the 1800 Hz tone; when GTE is a 1 it selects the 550 Hz tone. The selected guard tone will be transmitted only when GTE is enabled.
IRQ	Interrupt	(0,1):E:7	When status bit IRQ is a 1, it indicates that an interrupt has been generated. The $\overline{IRQ}$ hardware signal is generated following the setting of the IRQ bit. $\overline{IRQ}$ is cleared when either the NEWS bit is reset to a 0 or the DDR is loaded with a number.
LCD	Loss of Carrier Disconnect	0:D:2	When configuration bit LCD is a 1, the modem terminates a call when a loss of received carrier energy is detected after 400 ms. After the first 40 ms of loss of carrier, RLSD goes off. 360 ms later, if no carrier is detected, CTS goes off, and the modem goes on-hook. If energy above threshold is detected during the 360 ms period, RLSD will be set to a 1 again. If further loss of energy occurs, the 400 ms time frame is restarted. If LCD is set to a 0, RLSD will be set to a 1 when energy is above threshold, but will not force the modem on-hook when energy falls below threshold. In this case, it is necessary to re-enable LCD in order to put the modem on-hook. LCD is not automatically disabled in leased line operation. The user must write a 0 into LCD bits for this to occur.
LL	Leased Line	1:9:4	When configuration bit LL is a 1, the modem is in leased line operation; when 0, the modem is in switched line operation. When LL is set to a 1, the modem immediately goes off-hook and into data mode.
MODE	Mode Select	(0,1):A:(0,3)	These bits select the compatibility at which the modem is to operate, as shown below: **Configuration Word** **3 2 1 0 — Configuration** 0 0 0 0 — Bell 2400 — 2400 Sync. 0 0 0 1 — Bell 2400 — 2400 Async. 0 0 1 0 — Bell 212A — 1200 Sync. 0 0 1 1 — Bell 212A — 1200 Async. 0 1 0 0 — Bell 212A — 0 to 300 Async. 1 0 0 0 — V.22A — 1200 Sync. 1 0 0 1 — V.22B — 1200 Async. 1 0 1 0 — V.22A — 600 Sync. 1 0 1 1 — V.22B — 600 Async. 1 1 0 0 — V.22 bis — 2400 Sync. 1 1 0 1 — V.22 bis — 2400 Async. 1 1 1 0 — V.22 bis — 1200 Sync. 1 1 1 1 — V.22 bis — 1200 Async. NOTE: The Mode bits in both chips should be set exclusively of all other bits, followed immediately by the setting of the NEWC bits. This will ensure proper modem configuration. *Automatic Reconfiguration* The modem is capable of automatically falling back during the handshake to the compatibility of a remote modem. The modem can be in either the answer or originate mode for this to occur. The compatibilities that the modem are limited to adapt to are V.22 bis, V.22 A/B (1200 bps), Bell 212 and Bell 103. If the R2424 is to originate in a specific configuration, the MODE bits must be set. When the answer modem is configured for Bell 300 asynchronous and is called by a 1200 bps modem, the handshake will be completed at 1200 bps.
NAT	No Answer Tone	1:9:7	When configuration bit NAT is a 1, the modem will not transmit the 2100 Hz CCITT answer tone. This bit is only valid for CCITT configurations. With this bit enabled in answer mode, when the modem goes off-hook it will remain silent for 75 ms and then transmit unscrambled ones.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
NEWC	New Configuration	(0,1):E:3	When the NEWC bit is a 1, it tells the modem that a new configuration has been written into the configuration registers. The modem will then read the configuration registers and then reset NEWC to a 0. NEWC must be set to a 1 after a new configuration has been written into the following registers: (0:[A–D]) and (1:[9–D]). The remaining registers do not require the use of NEWC to tell the modem that new data was written into them.
NEWS	New Status	(0,1):E:5	When handshake bit NEWS is a 1, it tells the user that there has been a change of status in the status registers. The user must write a 0 into NEWS to reset it. This action also causes the interrupt to be cleared.
NTS	No Transmitter Scrambler	1:9:0	When configuration bit NTS is a 1, when the modem is off-hook it will transmit all data in an unscrambled form. This bit should be disabled if the normal modem handshake is desired.
ORG	Originate/Answer	1:9:5	When configuration bit ORG is a 1, the modem is in originate mode; and when a 0 the modem is in answer mode. (This is only valid in manual originate/answer and analog loopback). If ORG is a 1 in analog loopback, the modem will transmit in the high band and receive in the low band. If ORG is a 0 in analog loopback, the modem will transmit in the low band and receive in the high band.
(None)	RAM Access R	0:F:0–7	Contains the RAM access code used in reading RAM locations in chip 0 (receiver device).
(None)	RAM Access T	1:F:0–7	Contains the RAM access code used in reading RAM locations in chip 1 (transmitter device).
XRAMRL	RAM Data XRL	0:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 0.
XRAMRM	RAM Data XRM	0:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 0.
XRAMTL	RAM Data XTL	1:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1.
XRAMTM	RAM Data XTM	1:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.
YRAMRL	RAM Data YRL	0:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 0.
YRAMRM	RAM Data YRM	0:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 0.
YRAMTL	RAM Data YTL	1:4:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1.
YRAMTM	RAM Data YTM	1:5:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RDL	Remote Digital Loopback	(0,1):A:6	When configuration bits RDL are a 1, it causes the modem to initiate a request for the remote modem to go into digital loopback. RXD is clamped to a mark and the CTS bit and $\overline{CTS}$ signal will be reset until the loop is established. The TM bit is not set in this case, since the local modem initiated the request. RDL does not function in 300 bps.
RI	Ring Indicator	1:8:4	When status bit RI is a 1, it indicates that a ringing signal is being detected. The RI bit follows the ringing signal with a 1 during the on time and a zero during the off time coincident with the $\overline{RI}$ signal. The following are the RI bit response times: **RI Bit Transition** — **Response** OFF-to-ON* — 110 ±50 ms (50% duty cycle) ON-to-OFF — 450 ±50 ms *The OFF-to-ON time is duty cycle dependent: 890 ms (15%) ≥ time ≥ 50 ms (100%) This OFF-to-ON (or ON-to-OFF) response time is defined as the time interval between the sudden connection (removal) of the ring signal across TIP and RING and the subsequent transition of the RI bit.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RLSD	Received Line Signal Detector	0:8:0	When status bit RLSD is a 1, it indicates that the carrier has successfully been received. RLSD will not respond to the guard tones or answer tones RLSD response times are given below: **$\overline{\text{RLSD}}$[1]** — **Constant Carrier** — **Controlled Carrier** OFF-to-ON — 40 to 65 ms — 40 to 65 ms ON-to-OFF — 40 to 65 ms — 40 to 65 ms **Note:** 1. After handshake has occurred.
RSD	Receive Space Disconnect	0:D:1	When configuration bit RSD is a 1, the modem goes on-hook after receiving approximately 1.6 seconds of continuous spaces.
RTRN	Retrain (2400 bps only)	1:9:6	When configuration bit RTRN is a 1, the modem sends the training sequence. It resets when the training sequence from the remote modem has successfully been received. If the sequence has not been successfully received from the remote modem, CTS will remain OFF. In order to put the modem back in the data mode, it is necessary to write a 0 into the RTRN bit, then repeat the retrain sequence.
RTS	Request-to-Send	1:9 3	When control bit RTS is a 1, the modem transmits any data on TXD when CTS becomes active. In constant carrier mode, RTS should be set the same time as DTR and then left ON. In controlled carrier operation, independent operation of RTS turns the carrier ON and OFF. The responses to RTS are shown (assume the modem is in data mode). **Leased or Dial Line[1]** — **RTS Off** — **RTS On** Controlled Carrier — CTS OFF Carrier OFF — Carrier ON 210 to 275 ms Scrambled 1's Transmitted CTS ON Constant Carrier — CTS OFF Carrier ON Scrambled 1's Transmitted — CTS ON Carrier ON Data Transmitted **Note:** 1. After handshake is complete. For ease of use in constant carrier mode, RTS should be turned ON the same time as DTR.
SPEED	Speed Indication	0:9:(4,5)	The SPEED status bits reflect the speed at which the modem is operating. The SPEED bit representations are shown **4 5 — Speed** 0 0 — 0–300 0 1 — 600 1 0 — 1200 1 1 — 2400 **Note:** The SPEED bits are not active in analog loopback and leased line mode.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
SSD	Send Space Disconnect	1:D:0	When configuration bit SSD is a 1, it causes the modem to transmit approximately 4 seconds of spaces before disconnecting, when DTR goes from active to inactive state.
ST	Self Test	(0,1):A:4	When configuration bit ST is a 1, self test is activated. ST must be a 0 to end the test. It is possible to perform self test in analog loopback with or without a DTE connected During any self test, TXD and RTS are ignored. Self test does not test asynchronous-to-synchronous converter circuits in either the transmitter or receiver. Error detection is accomplished by monitoring the self test error counter in the RAM. If the counter increments during the self test, an error was made. The counter contents are available in the diagnostic register when the RAM access code 00 is loaded in the diagnostic control register (0:F). *Self Test End-to-End (Data Mode)* Upon activation of self test an internally generated data pattern of alternate binary ones and zeros (reversals) at the selected bit rate are applied to the scrambler. An error detector, capable of identifying errors in a stream of reversals are connected to the output of the descrambler. *Self Test with Loop 3* Loop 3 is applied to the modem as defined in Recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test, In this test DTR is ignored. *Self Test with Loop 2 (Data Mode)* The modem is conditioned to instigate a loop 2 at the remote modem as specified in recommendation V.54. Self test is activated and DCE operation is as in the end-to-end test ST does not function in 300 bps.
3DB	3 dB Loss to Receive Signal	1:B.2	When configuration bit 3DB is a 1, it attenuates the received signal 3 dB. This is only used if the modem will see 0 dBm or greater line signal at the receiver input. Insertion of the 3 dB loss will then prevent saturation.
TM	Test Mode	0:8:1	When status bit TM is a 1, it indicates that the modem has completed the handshake and is in one of the following test modes: AL or RDL.
TONE	Tone Detect	0:8:7	TONE follows the energy detected in the 340 to 640 Hz frequency band. The user must determine which tone is present on the line by determining the duty cycle of the TONE bit. TONE is active only when CRQ in chip 0 is a 1. Detection Range: -10 to -43 dBm Response Time: 17 ±2 ms
TXCLK	Transmit Clock Select	1:C:(5,6)	TXCLK allows the user to designate the origin of the transmitter data clock, as shown below **Configuration Word** **Transmit Clock** — **6** **5** Internal — 0 0 External — 1 0 Slave — 1 1 If external clock is chosen the user clock must be input at XTCLK. The clock characteristics must be the same as TDCLK. The external clock will be reflected by TDCLK. If slave clock is chosen the transmitter is slaved to the receive clock. This is also reflected by TDCLK.

Table 11. Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TX LEVEL	Transmit Level	1·B:(5–7)	TX LEVEL allows the user to change the transmit level at TIP and RING (assuming the DAA has 10 dBm attenuation in the transmit path).

Configuration Word 7	6	5	Transmit Level (±1.0 dBm) (at TIP and RING)
0	0	0	–10 dBm
0	0	1	–12 dBm
0	1	0	–14 dBm
0	1	1	–16 dBm
1	0	0	–18 dBm
1	0	1	–20 dBm
1	1	0	–22 dBm
1	1	1	–24 dBm

Internal Modem Timing

In a microprocessor environment it is necessary to know how long various functions last or what the response times of certain functions are. Since the modem is a part of the microprocessor environment its timing and response times are necessary. Table 12 provides the timing relationships between interface memory bits and modem functions.

Table 12. Internal Modem Timing

Parameter	Time Interval
NEWC bit checked	
Transmitter	Once per sample[1]
Receiver	Once per baud[2]
NEWC bit set by host until modem action	
Transmitter	≤ One baud time
Receiver	One baud time
Control, Configuration bits read	
Transmitter	Only after NEWC is set
Receiver	ST, RSD—every sample, all others after NEWC set
Status bits updated	
Transmitter	Once per sample
Receiver	Once per baud
Status change reflected by NEWS, IRQ	
Transmitter	MIN < one sample time MAX one sample time
Receiver	MIN one sample time MAX one baud time
Memory status reflected to modem pin	
Transmitter	33.33 μs
Receiver	33.33 μs

1. Sample Time = 7200 Hz 2. Baud Time = 600 Hz

AUTO DIAL SEQUENCE

The following flow chart defines the auto dial sequence via the microprocessor interface memory.

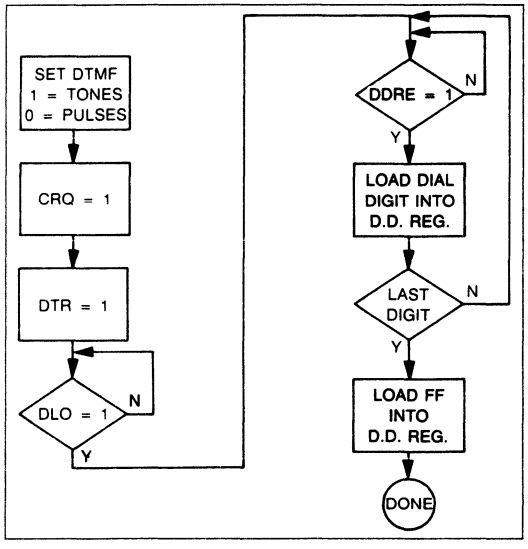


Figure 13. Auto Dial Sequence Flow Diagram

Note: The modem timing for the auto dialer accounts for inter-digit delay for pulses and tones.

SIGNAL PROCESSOR RAM ACCESS

RAM AND DATA ORGANIZATION

Each signal processor contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16-bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

Interface Memory Locations

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit normally transfers a word from RAM to interface memory once each clock cycle of the SP device. In the transmitter, a word is transferred from SP RAM to the interface memory every sample time. In the receiver, a word is transferred from RAM to the interface memory every sample time as well. Each RAM word transferred to the interface memory is 32-bits long. These bits are written by the SP logic unit into interface memory registers 5, 4, 3, and 2. Registers 3 and 2 contain the most significant byte and least significant byte, respectively, of the XRAM data. Registers 5 and 4 contain the most and least significant bytes of YRAM data, respectively.

RAM Access Codes

The SP logic unit determines the SP RAM address to read from, or write to, by the code stored in the RAM Access bits of interface memory register F (RAM Access R in the receiver 0:F and RAM Access T in the transmitter 1:F).

Only the transmitter (chip 1) allows data to be transferred from interface memory to SP RAM. When set to a 1, bit 1:F:7 signals the SP logic unit to disable transfer of SP RAM data to the interface memory, and instead, to transfer data from interface memory to SP RAM. When writing into SP RAM, 32 bits of data in the XRAM and YRAM registers will be written into the appropriate SP RAM location as specified by the RAM access code (82-86) in register 1:F (Table 13). Once the data is written into the RAM access register 1:F, the XRAM registers 1:2 and 1:3 or the YRAM registers 1:4 and 1:5, set the NEWC bit 1:E:3 to a 1. This action causes the information to be transferred from interface memory into SP RAM. Bit 7 of register 1:F is cleared to a 0 by the modem after the RAM is read. New data can be written into the SP RAM after the NEWC bit is reset to a 0 by the SP.

Note:

Any transmitter RAM Write operation must always be preceded by a RAM read from the desired location. This is to guarantee that the correct information is written into the 16 unchanged bits, since all transmitter RAM operations are 32 bit transfers with typically only 16 of the bits used.

Both the transmitter and receiver (chips 1 and 0, respectively) allow data to be transferred from SP RAM into the interface memory. A 0 in transmitter bit 1:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the RAM access code in register 1:F. A 0 in receiver bit 0:F:7 enables the SP to transfer 32 bits of data from SP RAM to the XRAM and YRAM registers (16 bits each) in the interface memory as specified by the access code in register 0:F. To read the SP RAM in chip 1 (transmitter), load into 1:F the RAM access code which identifies the 32 bits of data to transfer to the XRAM and YRAM registers. Next, set the NEWC bit 1:E:3 to a 1. After transferring the data from RAM to the XRAM or YRAM registers, the NEWC bit is reset to a 0 by the SP. Chip 0 (receiver), on the other hand, will provide the XRAM and YRAM data one sample time following the loading of the RAM access code into register 0:F, and will continue to provide the same data at one sample time intervals until a new RAM access code is loaded.

When reading from or writing into RAM, no bits are provided for handshaking or interrupt functions. The NEWC bit can be used as a mechanism to provide sample and baud intervals. Since the NEWC bit is checked, once per baud in chip 0 and once per sample in chip 1, the user can set the NEWC bit and wait for it to be cleared. Depending on which chip the NEWC bit was set, the time interval from the setting to the clearing of the NEWC bit will be either one sample or one baud time. This, however, will not guarantee that the action of reading and writing the XRAM and YRAM will occur in the middle of an actual sample or baud time.

Table 13. RAM Access Codes

Node	Function	RAM Access Code		Chip	Reg. No.
		RAM Read	RAM Write		
1	Demodulator Output	56	–	0	2, 3, 4, 5
2	Low Pass Filter Output	40	–	0	2, 3, 4, 5
3	Input Signal to Equalizer Taps	41–4D	–	0	2, 3, 4, 5
4	AGC Gain Word	14	–	0	2, 3
5	Equalizer Tap Coefficients	01–0D	–	0	2, 3, 4, 5
6	Equalizer Output	53	–	0	2, 3, 4, 5
7	Rotated Equalizer Output (Received Point Eye Pattern)	11	–	0	2, 3, 4, 5
8	Decision Points (Ideal Eye Pattern)	51	–	0	2, 3, 4, 5
9	Rotated Error	52	–	0	2, 3, 4, 5
10	Rotation Angle	12	–	0	4, 5
11	Phase Error	10	–	0	2, 3
12	Self Test Error Counter	00	–	0	2, 3
	DTMF Tone Duration	02	82	1	4, 5
	DTMF Interdigit Delay	03	83	1	2, 3
	Pulse Interdigit Delay	03	83	1	4, 5
	Pulse Relay Make Time	04	84	1	2, 3
	Pulse Relay Break Time	04	84	1	4, 5
	Handshake Abort Counter	05	85	1	4, 5
	Handshake Abort Timer	06	86	1	2, 3
	CTS Off-Time	07	87	1	2, 3

NOTE: 1. All the chip 1 access codes are not valid before R5310-18.
2. Access codes are hexadecimal.
3. Only chip 1 RAM can be written
4. CTS Off-Time is not valid before R5310-22.

ERROR RATES

Bit error rate (BER) is a measure of the throughput of data on the communication channel. It is the ratio of the number of received bits in error to the number of transmitted bits. This number increases with decreasing signal-to-noise ratio (SNR). The type of line disturbance and the modem configuration affect the BER.

Tables 14 through 16 summarize the BERs for various conditions. Figure 14 shows the BER measurement setup.

Table 14. BER Summary

R2424		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
2400 bps	1×10^{-5}	16.6 dB	16.2 dB
1200 bps	1×10^{-5}	8.2 dB	7.9 dB
600 bps	1×10^{-5}	5.0 dB	5.0 dB
300 bps	1×10^{-5}	9.2 dB	7.0 dB

Test Condition: Signal Level = –30 dBm,
Sync for 2400 bps, 1200 bps, 600 bps,
Async for 300 bps,
With 3002 Unconditioned Line.

Table 15. BER Summary

R2424		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
2400 bps	1×10^{-5}	19.0 dB	17.3 dB
1200 bps	1×10^{-5}	8.3 dB	8.1 dB
600 bps	1×10^{-5}	5.0 dB	5.0 dB
300 bps	1×10^{-5}	10.4 dB	7.2 dB

Test Condition: Signal Level = – 43 dBm,
Sync for 2400 bps, 1200 bps, 600 bps,
Async for 300 bps,
With 3002 Unconditioned Line.

Table 16. BER Summary

R2424		Signal to Noise Ratio	
Data Rate	Bit Error Rate	Originate Mode	Answer Mode
2400 bps	1×10^{-5}	17.0 dB	16.6 dB
1200 bps	1×10^{-5}	7.7 dB	7.9 dB
600 bps	1×10^{-5}	4.6 dB	4.5 dB
300 bps	1×10^{-5}	9.3 dB	6.2 dB

Test Condition: Signal Level = –40 dBm,
Sync for 2400 bps, 1200 bps, 600 bps,
Async for 300 bps,
Back-To-Back.

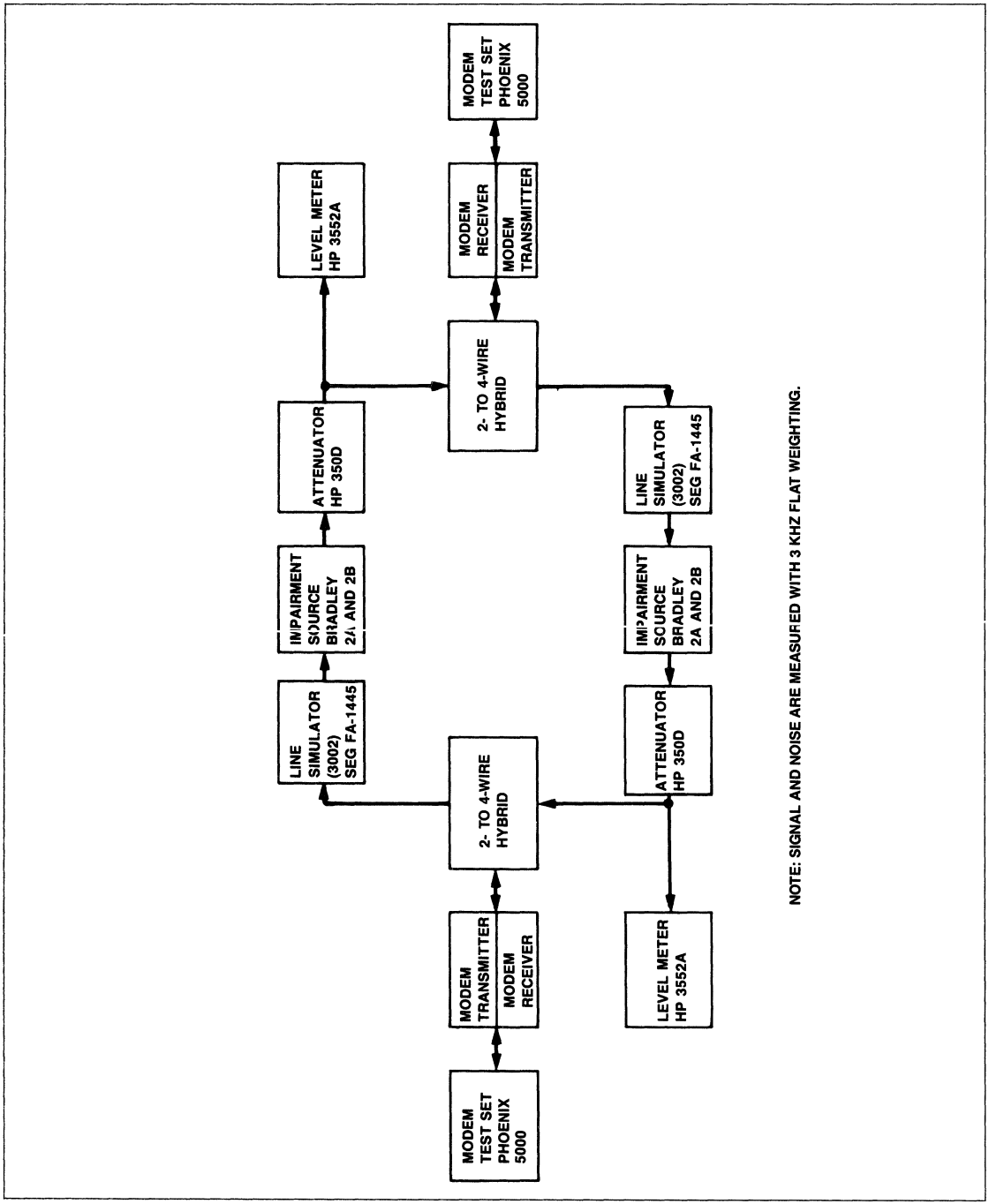


Figure 14. 2-Wire Full-Duplex Bit Error Rate Performance Test Setup (Bidirectional)

Table 17. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	390 mA	<455 mA
+12 Vdc	±5%	25 mA	< 30 mA
−12 Vdc	±5%	4 mA	< 5 mA

Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Table 18. Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 19. Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	
Board Structure.	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
PCB Dimensions:	
DC Version	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Height	0.75 in. (19 mm)
M Version	
Width	3.937 in. (100 mm)
Length	3.328 in. (82 mm)
Height	0.40 in. (10.2 mm)
Weight (max):	0.45 lbs. (0.20 kg.)
Lead Extrusion (max.):	0.100 in. (2.54 mm)
DIP Connector Version	
Board Structure	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions	
Width	2.0 in. (50.8 mm)
Length	3.5 in. (88.9 mm)
Height	0.2 in. (5.08 mm) above, 0.13 in. (3.30 mm) below
Weight (max.)	2.6 oz. (73g)
Pin Length (max.)	0.53 in. (13.5 mm) above

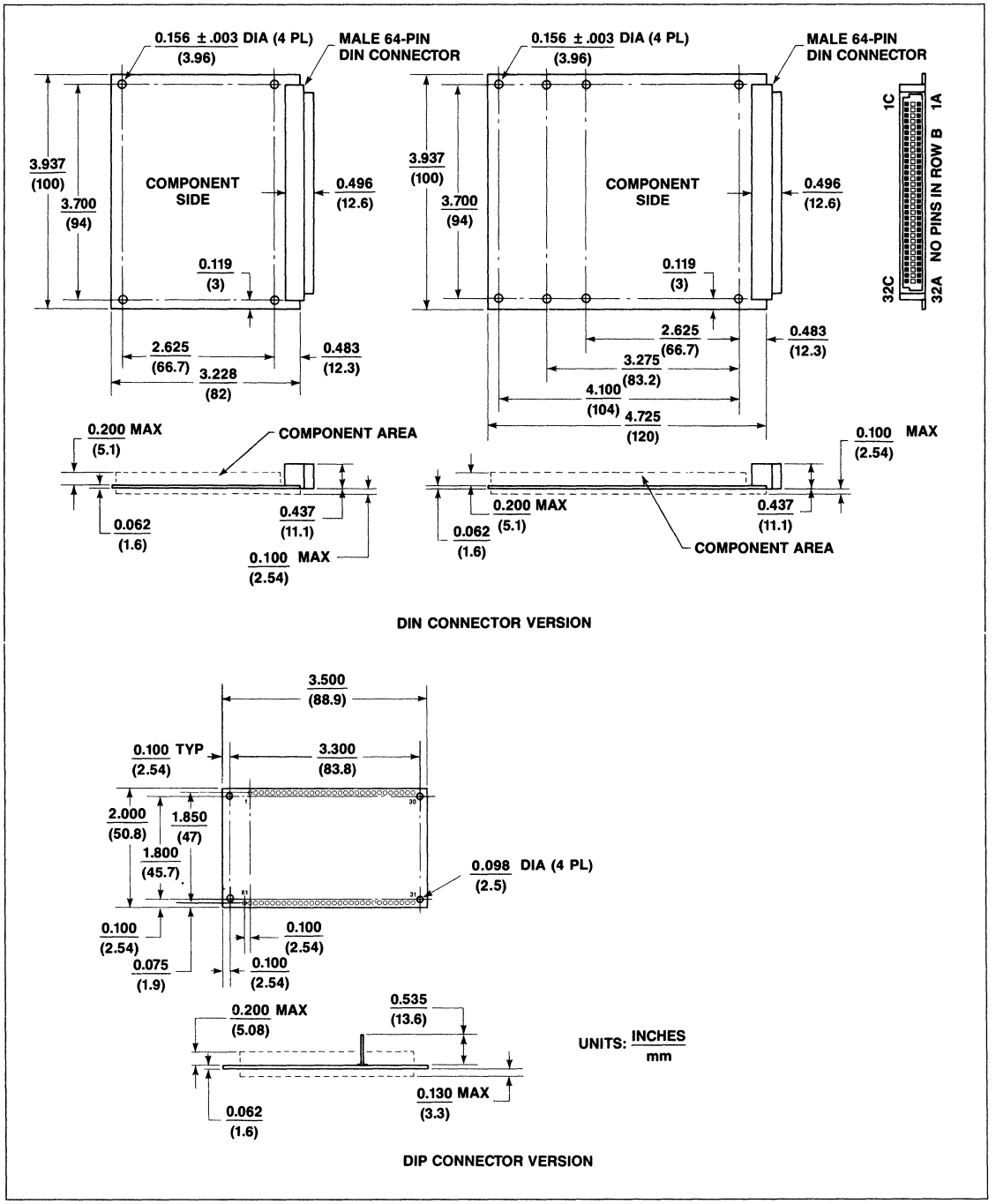


Figure 15. R2424 Modem Dimensions and Pin Locations

R2424 MODEM INSTALLATION AND MAINTENANCE

This section contains installation instructions and maintenance procedures for the Rockwell R2424DC Modem. It also contains a special notice from the Canadian Department of Communications (DOC) for Canadian operation and from the Federal Communications Commission (FCC) for United States operation.

GENERAL DESCRIPTION

The Rockwell R2424DC modem is designed to be used with the United States or Canadian Telephone Switched Networks in 2-wire full-duplex dial-up operation. The modem requires protective circuitry registered with the Federal Communications Commission (FCC) Part 68 which allows direct connection to the U.S. switched telephone network. This circuitry also complies with the Canadian Department of Communications (DOC) Terminal Attachment Program (TAP) which similarly defines their switched telephone network requirements.

The R2424DC features automatic dial and answer capabilities along with surge suppression and hazardous voltage and longitudinal balance protection. Its maximum output signal level at the telephone interface is set at -10 dBm ± 1 dBm (permissive mode of operation).

Two standard telephone jack connectors (RJ11s) are mounted side by side on one edge of the board and are wired in parallel. One is for connection to the telephone line network and the other for the telephone headset connection.

INSTALLATION AND SIGNAL ROUTING INSTRUCTIONS

PHYSICAL MOUNTING

The modem module may be physically incorporated into the customer's end product by utilizing the four corner 0.156" diameter mounting holes (for the self-hooking plastic type standoffs or for bolting it down to some rigid structure) or by installing the module into card guides.

ELECTRICAL INTERFACING INSTRUCTIONS

The electrical interfacing is accomplished via the DIN (Euro) connector (for external power inputs and digital logic signals) and the telco connectors (for the telephone network connection). Note that the telephone interface connectors are physically separated from the modem interface control connector and extreme care must be taken in routing the telephone interface leads from the modem to the telephone network (line connector jack in the wall).

FCC RULES PART 68 REQUIREMENTS

The FCC Rules Part 68 requires that the telephone interface leads shall:

1. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use the same connector as leads or metallic paths connecting to power connections.

   Note

   Power connections are defined as the connections between commercial power and any transformer, power supply rectifier, converter or other circuitry associated with the modem. The connections of the interface pins (including the $+12$ Vdc, -12 Vdc and $+5$ Vdc) are not considered power connections.

2. Be reasonably physically separated and restrained from; not routed in the same cable as; nor use adjacent pins on the same connector as metallic paths that lead to unregistered equipment, when specification details provided to the FCC do not show that the interface voltages are less than nonhazardous voltage source limits in Part 68.

   Note

   All the DIN connector interface voltages to the modem have been established as non-hazardous.

ROUTING OF TELEPHONE INTERFACE LINES

In routing the telephone interface leads from the modem telephone connector jacks to the telephone line network connection, the following precautions should be strongly considered for safety.

1. The telephone interface routing path should be as direct and as short as possible.
2. Any cable used in establishing this path should contain no signal leads other than the modem telephone interface leads.
3. Any connector used in establishing this path shall contain not commercial power source signal leads, and adjacent pins to the TIP and RING (T and R) pins in any such connector shall not be utilized by any signals other than those shown in this document.

MAINTENANCE PROCEDURE

Under the FCC Rules, no customer is authorized to repair modems. In the event of a Rockwell modem malfunctioning, return it for repair to an authorized ROCKWELL INTERNATIONAL distributor (if in Canada) or send it directly to the Semiconductor Products Division, Rockwell International Corporation, El Paso, Texas 79906.

SPECIAL INSTRUCTION TO USERS

If the Rockwell modem has been registered with the Federal Communications Commission (FCC), you must observe the following to comply with the FCC regulations:

A. All direct connections to the telephone lines shall be made through standard plugs and telephone company provided jacks.

B. It is prohibited to connect the modem to pay telephones or party lines.

C. You are required to notify the local telephone company of the connection or disconnection of the modem, the FCC registration number, the ringer equivalence number, the particular line to which the connection is made and the telephone number to be associated with the jack.

Note

If the proper jacks are not available, you must order the proper type of jacks to be installed by the telephone company (VSOC RJ11 for permissive mode of operation).

D. You should disconnect the modem from the telephone line if it appears to be malfunctioning. Reconnect it only if it can be determined that the telephone line and not the modem is the source of trouble. If the Rockwell modem needs repair, return it to the ROCKWELL INTERNATIONAL CORPORATION. This applies to the modem whether it is in or out of warranty. Do not attempt to repair the unit as this is a violation of the FCC rules and may cause danger to persons or to the telephone network.

TELEPHONE COMPANY RIGHTS AND RESPONSIBILITIES

A. The Rockwell modem contains protective circuitry to prevent harmful voltages to be transmitted to the telephone network. If such harmful voltages do occur, then the telephone company may temporarily discontinue service to you. In this case, the telephone company should:

1. Promptly notify you of the discontinuance.
2. Afford you the opportunity to correct the situation which caused the discontinuance.
3. Inform you of your right to bring a complaint to the FCC concerning the discontinuance.

B. The telephone company may make changes in its facilities and services which may affect the operation of your equipment. It is, however, the telephone company's responsibility to give you adequate notice in writing to allow you to maintain uninterrupted service.

LABELING REQUIREMENTS

A. The FCC requires that the following label be prominently displayed on the outside surface of the customer's end product and that the size of the label should be such that all the required information is legible without magnification.

Sample label below:

Unit contains Registered Protective Circuitry which complies with Part 68 of FCC Rules.

FCC Registration Number: AMQ9SQ-14211-DM-E

Ringer Equivalence: 0.9B

Note

The Rockwell modem module has the FCC registration number and ringer equivalence number permanently affixed to the solder side of the PCB and any unit containing this modem shall use this information for the label requirements.

SPECIAL NOTICE FROM THE CANADIAN DEPARTMENT OF COMMUNICATIONS

The Canadian Department of Communications label identifies certified equipment. This certification means that the equipment meets certain telecommunications network protective, operational and safety requirements. The Department does not guarantee the equipment will operate to the user's satisfaction.

Before installing this equipment, users should insure that it is permissible to be connected to the facilities of the local telecommunications company. The equipment must also be installed using an approved method of connection. In some cases, the company's inside wiring associated with a single line individual service may be extended by means of a certified jack-plug-cord ensemble (telephone extension cord). The customer should be aware that the compliance with the above conditions may not prevent degradation of service in some situations. Existing telecommunications company requirements do not permit their equipment to be connected to customer-provided jacks except where specified by individual telecommunications company tariffs.

The Department of Communications requires the Certificate Holders to identify the method of network connection in the user literature provided with the certified terminal equipment.

Repairs to certified equipment should be made by an authorized Canadian maintenance facility designated by the supplier. Any repairs or alterations made by the user to this equipment, or equipment malfunctions may give the telecommunications company cause to request the user to disconnect the equipment.

Users should ensure for their own protection that the electrical ground connections of the power utility, telephone lines and internal metallic water pipe system, if present, are connected together. This precaution may be particularly important in rural areas.

CAUTION

Users should not attempt to make such connections themselves, but should contact the appropriate electric inspection authority, or electrician, as appropriate.

1

R201/26DP
2400/1200 bps Data Pump Modem

INTRODUCTION

The Rockwell R201/26DP is a synchronous, 2400/1200 bits per second (bps) modem. It is designed for half duplex operation over the public switched telephone network or (PSTN) full duplex operation over unconditioned leased lines.

The modem satisfies the telecommunications requirements specified in CCITT Recommendation V.26 bis Alternate A or B, and Bell Specification 201B/C.

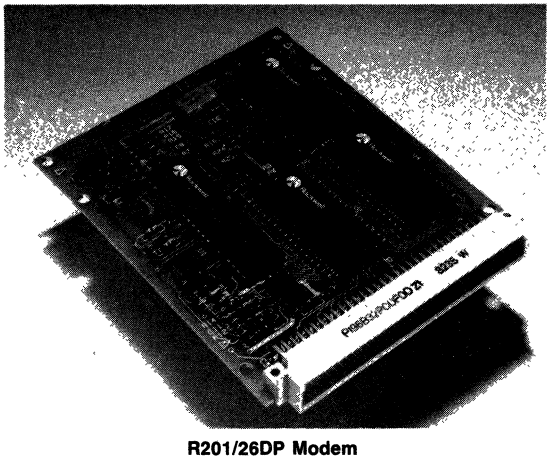
The R201/26DP is optimized for point-to-point applications and is suitable for network applications where the optimum in data transfer is needed. Its small size and low power consumption offer the user flexibility in creating a 2400/1200 bps modem customized for specific packaging and functional requirements.

Data can be transferred between the host computer either serially over the CCITT V.24 (RS-232-C) interface or in parallel over an 8-bit microprocessor bus.

The R201/26DP is a member of Rockwell's family of plug compatible integral modems.

FEATURES

- Configurations:
  — CCITT V.26, V.26 bis
  — Bell 201B/C
- Full-duplex (4-wire) over Leased Lines
- Half-duplex (2-wire) over PSTN
- Ideal for point-to-point applications
- Synchronous Operation:
  — 2400 bps (with fall-back) ±.01%
  — 1200 bps ±.01%
- Dual Tone Multi-Frequency (DTMF) Generation
- Programmable Tone Generation
- Call Progress Tone Detection
- Programmable Output Level: −1 dBm to −15 dBm
- Equalization
  — Automatic Adaptive
  — Compromise Cable and Link (Selectable)
- DTE Interface:
  — Microprocessor Bus
  — CCITT V.24 (RS-232-C Compatible)
- Local and Remote Test Configurations
- Selectable Scrambler/Descrambler (V.27 bis)
- Dynamic Range: 0 dBm to −43 dBm
- Diagnostic Capability
  — Provides Telephone Line Quality Monitoring Statistics
- Small Size: 100 mm × 120 mm (3.94 in. × 4.73 in.)
- Low Power Consumption: 3W (Typical)
- TTL and CMOS Compatible



R201/26DP Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER AND SIGNALING FREQUENCIES

The transmitter carrier and signaling frequencies of the R201/26DP are listed in Table 1.

Table 1. Transmitter Carrier and Signaling Frequency Specifications

Function	Frequency (Hz ±0.01%)
Carrier frequency	1800
CCITT Echo Suppression and Answering Tone Frequencies	2100
BELL Echo Suppression and Answering Tone Frequencies	2025

DTMF GENERATION

The R201/26DP is capable of generating Dual Tone Multifrequency (DTMF) signals. The duration of the DTMF signal is 95 ms and the interdigit delay is 70 ms. The amplitude of the lower frequency is −5.8 dBM and of the higher frequency is −3.8 dBM.

Table 2 lists the Dial Digit Register (DDR) codes necessary for DTMF dialing and the corresponding tone pairs.

Table 2. Dial Digits/Tone Pairs

Dial Digit Register (DDR) Hexadecimal Code	Dial Digit	Tone Pair (Hz)	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	#	941	1477

TONE GENERATION

Under control of the host processor, the R201/26DP can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

TONE DETECTION

The R201/26DP features a Tone Detector receiver configuration. The tone detector responds to energy in the 345 ± 10 Hz to 650 ± 10 Hz frequency range. The presence of a tone is indicated by the zero state of a status bit. The tone detector response time is 10 ±5 ms.

SIGNALING AND DATA RATES

The data signaling and modulation rates for normal and fallback operation are listed in Table 3.

Table 3. Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate: Normal Operation Data Rate:	1200 Baud 2400 bps
Signaling Rate: Fallback Operation Data Rate:	1200 Baud 1200 bps

DATA ENCODING

At either 2400 bps or 1200 bps the R201/26DP operates at 1200 baud.

At 2400 bps the data stream is encoded into dibits. Two different methods of coding are used in accordance with CCITT Recommendation V.26 A/B. The V.26B method is compatible with Bell 201 B/C modems.

At 1200 bps the data stream is encoded into single bits in accordance with CCITT Recommendation V.26 bis.

EQUALIZERS

The modem provides equalization functiuons that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

The transmitted spectrum occupies the bandwidth between 800 Hz and 2800 Hz and is shaped by a square root of 90% raised cosine filter.

SCRAMBLER/DESCRAMBLER

The R201/26DP incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT Recommendation V.27 bis and V.27 ter. The scrambler/descrambler is optionally enabled by interface memory bits.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R201/26DP can adapt to received frequency errors of up to ± 10 Hz with less than 0.5 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

The R48DP/208 provides a data derived Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a squarewave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. $\overline{\text{RDCLK}}$ duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is accurate to ±1.0 dB and is programmable from −1.0 dBm to −15.0 dBm in 2 dB steps.

TRANSMIT TIMING

The R201/26DP provides a Transmit Data Clock (TDCLK) output with the following characteristics:
1. *Frequency.* Selected data rate of 2400 or 1200 Hz (±0.01%).
2. *Duty Cycle.* 50% ±1%

Input data presented on TXD is sampled by the R201/26DP at the low to high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The R201/26DP is capable of tracking an external transmit clock signal on input XTCLK. This input signal must equal the desired data rate ±0.01% with a duty cycle of 50% ±20%.

TRAIN ON DATA

When train on data is enabled, the receiver trains on data in less than 3.5 seconds.

TURN-ON SEQUENCE

A total of 13 selectable turn-on sequences can be generated by the R201/26DP. These are listed in Table 4. The Turn-on Sequence data are written to the Turn On Sequence select field in chip 0.

Table 4. Turn-On Sequences

Turn On Sequence Number	Compatibility	CTS Response Time (ms)	Comments
0000	V.26 bis	0	
0001	V.26 bis	6.67	
0010	V.26 bis	8.33	
0011	V.26 bis	30.0	
0100	V.26 bis	30.0	Scrambler inserted
0101	V.26, V.26 bis	90.0	
0110	V.26, V.26 bis	90.0	Scrambler inserted
0111	Bell 201C	148.3	
1000	Bell 201C	148.3	Scrambler inserted
1001	V.26 bis	220.0	
1010	V.26 bis	220.0	Scrambler inserted
1011	V.26 bis	800.0	
1100	V.26 bis	800.0	Scrambler inserted

***NOTE:** The scrambler bits, DDIS and SDIS must also be set to insert or disable the scrambler.

TURN-OFF SEQUENCE

The R201/26DP turn-off sequence consists of a maximum of 6 ms of remaining data and scrambled ones at 1200 baud.

CLAMPING

The Received Data (RXD) signal is clamped to a constant mark (one) whenever the Received Line Signal Detector ($\overline{RLSD}$) is off.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of Request-To-Send ($\overline{RTS}$) and the off-to-on transition of $\overline{CTS}$ is determined by the modem configuration and its associated turn-on sequence.

These times are listed in Table 4. If training is not enabled $\overline{RTS}$/$\overline{CTS}$ delay is less than 2 baud times.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

The off-to-on (on-to-off) response time of the $\overline{RLSD}$ signal and the $\overline{CDET}$ bit is defined as the time period between the sudden connection (removal) of the received line signal to (from) the modem's receiver, and the subsequent on (off) transition of carrier detect. Table 5 shows the carrier detect response times.

Table 5. Carrier Detect Response Times

Carrier Detect Transition	Response Time (ms)
Off-to-on	14±1
On-to-off	8±3

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided for carrier detect and are selected by writing to the Receiver Threshold (RTH) bits in the interface memory. Table 6 shows the relationship betweeen the setting of the RTH bits and the carrier detect thresholds.

Table 6. Carrier Detect Levels

RTH	$\overline{RLSD}$ On	$\overline{RLSD}$ Off
00	> −43 dBm	< −48 dbm
01	> −33 dBm	< −30 dbm
10	> −26 dBm	< −31 dbm
11	> −16 dBm	< −21 dbm

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R201/26DP is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device shown in the Functional Interconnect Diagram (Figure 1) illustrates this capability.

PARALLEL MODE

The R201/26DP has the capability of transferring channel data up to eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R201/26DP is configured by the host processor via the microprocessor bus.

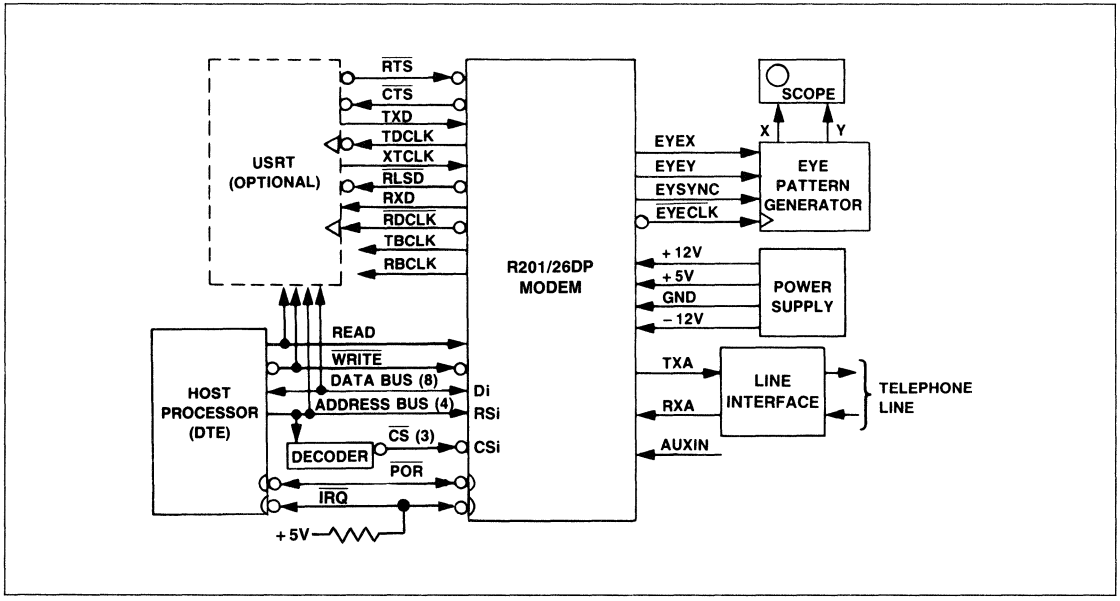


Figure 1. R201/26DP Functional Interconnect Diagram

FULL/HALF DUPLEX MODES

The R201/26DP receiver can be configured for either full duplex operation over four-wire leased lines or for half duplex operation over the switched telephone network. Full duplex or half duplex operation is selected by writing the appropriate configuration code into the receiver configuration register. When configured for half duplex operation, the receiver is squelched and unsquelched by setting and resetting of a control bit. When the receiver is squelched, $\overline{RLSD}$ is turned off and RXD is clamped to the marking state. When the receiver is unsquelched, it searches for a 20 ms period of silence before entering the training state. This prevents line echoes from interfering with the proper reception of training sequence.

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in Table 7. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. Figure 2 shows the Microprocessor Interface Timing Diagram. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors. Table 8 lists the timing parameters of the microprocessor interface.

Table 7. R201/26DP Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground (A)	AGND	31C,32C	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	Digital Ground Return
+5 volts	PWR	19C,23C,26C,30C	+5 volt supply
+12 volts	PWR	15A	+12 volt supply
-12 volts	PWR	12A	-12 volt supply
$\overline{POR}$	I/OB	13C	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	1C	Data Bus (8 Bits)
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	Register Select (4 Bits)
RS2	IA	6A	
RS1	IA	7C	
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	12C	Read Enable
$\overline{WRITE}$	IA	11A	Write Enable
$\overline{IRQ}$	OB	11C	Interrupt Request

Table 7. R201/26DP Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
C. V.24 INTERFACE:			
$\overline{RDCLK}$	OC	21A	Receive Data Clock
TDCLK	OC	23A	Transmit Data Clock
XTCLK	IB	22A	External Transmit Clock
$\overline{RTS}$	IB	25A	Request-to-Send
$\overline{CTS}$	OC	25C	Clear-to-Send
TXD	IB	24C	Transmitter Data
RXD	OC	22C	Receiver Data
$\overline{RLSD}$	OC	24A	Received Line Signal Detector
D. ANCILLARY CIRCUITS:			
RBCLK	OC	26A	Receiver Baud Clock
TBCLK	OC	27C	Transmitter Baud Clock
E. ANALOG SIGNALS:			
TXA	AA	31A	Transmitter Analog Output
RXA	AB	32A	Receiver Analog Input
AUXIN	AC	30A	Auxiliary Analog Input
F. DIAGNOSTIC:			
EYEX	OC	15C	Eye Pattern Data—X Axis
EYEY	OC	14A	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	Eye Pattern Clock
EYESYNC	OA	13A	Eye Pattern Synchronizing Signal

EYE PATTERN GENERATION

The four hardware diagnostic circuits, identified in Table 7, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the $\overline{EYECLK}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

MICROPROCESSOR TIMING

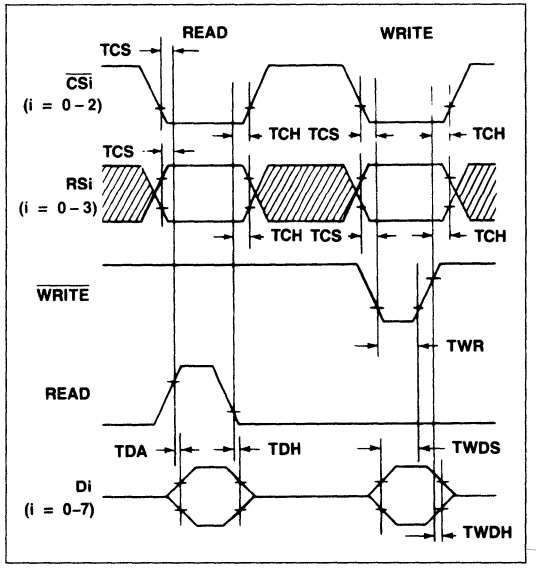


Figure 2. Microprocessor Interface Timing Diagram

Table 8. Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
$\overline{CSi}$, RSi hold time after Read or $\overline{Write}$	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

HARDWARE CIRCUIT CHARACTERISTICS

Digital Interface Characteristics

Table 9 lists the parameters associated with the digital interface provided by the R201/26DP.

Table 9. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type							
			IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes

1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I Load = 0.36 mA

Analog Interface Characteristics

Table 10 lists the parameters associated with the analog interface provided by the R201/26 DP.

Table 10. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is 604 ohms ±1%.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is the TLVL setting +0.6 dB − 1.4 dB. If unused, this input must be grounded near the modem connector. If used, it must be driven from a low impedance source.

SOFTWARE CIRCUITS

The R201/26DP comprises three signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 1 update at half the modem sample rate (2400 bps). Registers in chip 0 and 2 update at the baud rate (1200 bps).

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0−2), the register by Z(0−F), and the bit by Q(0−7, 0=LSB).

Status Control Bits

The operation of the R201/26DP is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory tables (tables 12-14). Bits designated by a dash (—) are reserved for modem use only and must not be changed by the host. Table 15 describes the function of each bit in the interface memory.

RAM Data Access

The R201/26DP provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers in chip 1 allow user access to RAM locations via the X word registers (1:3 and 1:2) and the Y word registers (1:1 and 1:0). Comparable registers in chip 2 provide access to chip 2 RAM locations. The access code stored in RAM ACCESS XS (1:5) selects the source of data for RAM DATA XSM and RAM DATA XSL (1:3 and 1:2). Similarly, the access code stored in RAM ACCESS YS (1:4) selects the source of data for RAM DATA YSM and RAM DATA YSL (1:1 and 1:0). Chip 2 registers are associated in the same way.

Reading of RAM data is performed by storing the necessary access codes in 1:5 and 1:4 (or 2:5 and 2:4), reading 1:0 (or 2:0) to reset the associated data available bit (1:E:0 or 2:E:0), then waiting for the data available bit to return to a one. Data is now valid and may be read from 1:3 through 1:0 (or 2:3 through 2:0). The contents of registers 2:3 and 2:1 are also available serially on outputs EYEX and EYEY, respectively, unless the IFIX bit (1:6:7) is set to a one. When IFIX is a one, EYEX and EYEY remain fixed on the rotated equalizer output.

AUTO DIAL SEQUENCE

The flowchart shown in Figure 3 defines the auto dial sequence via the microprocessor interface memory.

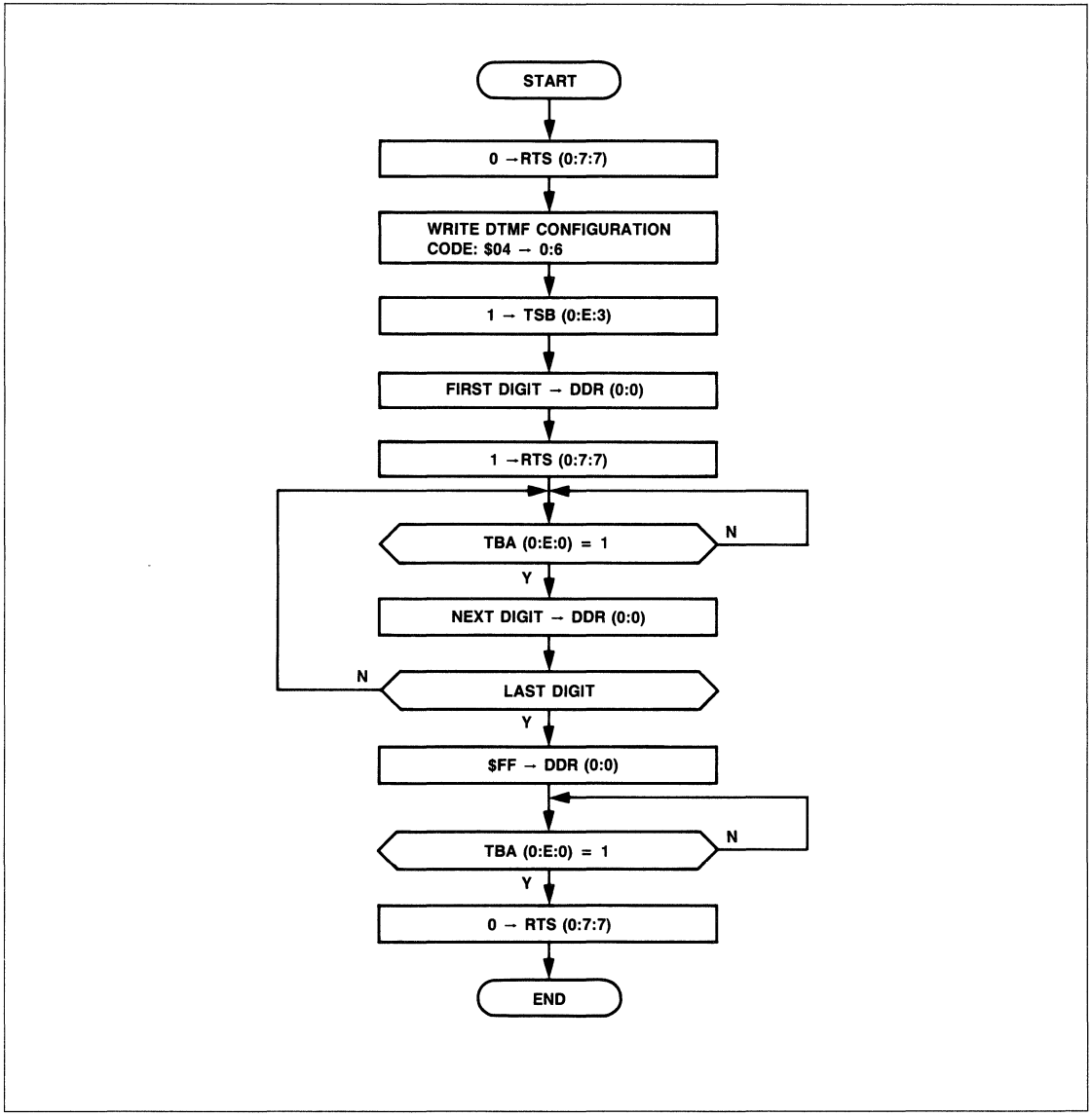


Figure 3. Auto Dialing Sequence Flowchart

RAM Access Codes

The RAM access codes defined in Table 11 allow the host processor to read diagnostic information within the modem.

Table 11. RAM Access Codes

No.	Function	Chip	X Access	Y Access	Register
1	Received Signal Samples	1	C0	Not Used	2,3
2	Demodulator Output	1	C2	42	0,1,2,3
3	Low Pass Filter Output	1	D4	54	0,1,2,3
4	Average Energy	1	DC	Not Used	2,3
5	AGC Gain Word	1	81	Not Used	2,3
6	Equalizer Input	2	C0	40	0,1,2,3
7	Equalizer Tap Coefficients	2	81 – 90	01 – 10	0,1,2,3
8	Unrotated Equalizer Output	2	E1	61	0,1,2,3
9	Rotated Equalizer Output (Received Points)	2	A2	22	0,1,2,3
10	Decision Points (Ideal Data Points)	2	E2	62	0,1,2,3
11	Error	2	E3	63	0,1,2,3
12	Rotation Angle	2	Not Used	00	0,1
13	Frequency Correction	2	AA	Not Used	2,3
14	EQM	2	A7	Not Used	2,3
15	Dual Point	2	AE	2E	0,1,2,3

NOTE

In the interface memory tables that follow, those columns marked by a dash (—) indicate reserved and are for modem use *only*.

Table 12. Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS XT							
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	DWTR	TPDM	XCEN	DTMF
6	TTONE	—	TV26	TBPS	TURN-ON SEQUENCE SELECT			
5	—	—	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			—	LCEN
3	FREQM							
2	FREQL							
1	RAM DATA XTM							
0	RAM DATA XTL/TRANSMITTER DATA/DDR							
Register / Bit	7	6	5	4	3	2	1	0

Table 13. Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Bit / Register	7	6	5	4	3	2	1	0
F	RTSD	SQH	SQHT	—	—	—	—	—
E	RSIA	—	—	—	RSB	RSIE	—	RSDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	$\overline{CDET}$
A	TODF	—	—	—	—	—	—	—
9	—	FED	—	—	—	$\overline{TONE}$	—	—
8	—	—	—	—	—	—	—	—
7	RTH		DDIS	RPDM	WSRD	WBRD	T2	RTDIS
6	IFIX	TOD	RV26	—	TDET	HD2W	RLRT	RBPS
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL/RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

Table 14. Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

Table 15. R201/26DP Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
A3L	Amplitude 3-Link Select	0:5:1	A3L is used in conjunction with LAEN. When A3L is a one the Japanese 3 link equalizer is selected and when A3L is a zero the U.S. Survey Long link equalizer is selected
$\overline{\text{CDET}}$	Carrier Detector	1:B:0	When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
CEQ	Cable Equalizer Field	0:5:4,5	The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following tables list the possible cable equalizer selection codes and responses.
DDIS	Descrambler Disable	1:7:5	When control bit DDIS is a one, and at device reset the receiver descrambler circuit is removed from the data path.
DTMF	Dual Tone Multi-frequency Select	0:7:0	When this bit is set to a one, the DTMF mode is selected. To initiate DTMF tone generation, the TSB bit must be set to a one for each tone pair desired. Although the R201/26DP will perform a 95 ms timeout on the tone pair, it does not notify the host that the tone is completed. Thus the host must perform its own 95 ms timeout to know when to start the next tone pair. DTMF is reset to zero by device reset.

CEQ — Cable Length (0.4 mm diameter)

CEQ	Cable Length (0.4 mm diameter)
0	0.0
1	1.8 km
2	3.6 km
3	7.2 km

Cable Equalizer Nominal Gain

CEQ CODE 1

Frequency (Hz)	Gain Relative to 1700 Hz (dB)	
	Transmitter	Receiver
700	−0.99	−0.94
1500	−0.20	−0.24
2000	+0.15	+0.31
3000	+1.43	+1.49

CEQ CODE 2

Frequency (Hz)	Gain Relative to 1700 Hz (dB)	
	Transmitter	Receiver
700	−2.39	−2.67
1500	−0.65	−0.74
2000	+0.87	+1.02
3000	+3.06	+3.17

CEQ CODE 3

Frequency (Hz)	Gain Relative to 1700 Hz (dB)	
	Transmitter	Receiver
700	−3.93	−3.98
1500	−1.22	−1.20
2000	+1.90	+1.81
3000	+4.58	+4.38

Unless a problem with training or high bit error rate is encountered, most applications operate successfully with no cable equalizer selected.

Table 15. R201/26DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>DWTR</td><td>Diagnostics Write to RAM</td><td>0:7:3</td><td>To write data into the internal memory of the Transmitter Interface Memory Chip 0, the DWTR bit is used. Note that setting DWTR to a one takes the modem out of data mode (important because RAM DATA XTL and TRANSMITTER DATA share the same address). DWTR is reset to zero by device reset.

The proper operational sequence for DWTR is given below:

1. Set DWTR bit to one.
2. Load RAM ACCESS CODE (see Table 11) into RAM ACCESS XT Register.
3. Load new data into RAM DATA XTM and RAM DATA XTL Registers.
4. Set TBA bit to zero to actually write data.
5. Wait for TBA bit to return to a one to insure that the new data is loaded correctly.
6. Repeat steps 2, 3, 4, and 5 until finished loading data.
7. Set DWTR bit to a zero.</td></tr>
<tr><td>D3L</td><td>Delay 3-Link Select</td><td>0:5:0</td><td>D3L is used in conjunction with LDEN. When D3L is a one the Japanese 3 link equalizer is selected and when D3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
<tr><td>$\overline{\text{FED}}$</td><td>Fast Energy Detector</td><td>1:9:6</td><td>When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband.</td></tr>
<tr><td>(None)</td><td>FREQL/FREQM</td><td>0:2:0–7,
0:3:0–7</td><td>The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below:

FREQM Register (0:3)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{15}</td><td>2^{14}</td><td>2^{13}</td><td>2^{12}</td><td>2^{11}</td><td>2^{10}</td><td>2^{9}</td><td>2^{8}</td></tr></table>
FREQL Register (0:2)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{7}</td><td>2^{6}</td><td>2^{5}</td><td>2^{4}</td><td>2^{3}</td><td>2^{2}</td><td>2^{1}</td><td>2^{0}</td></tr></table>
The frequency number (N) determines the frequency (F) as follows:
F = (0.146486) (N) Hz ±0.01%

Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below:

<table><tr><th>Frequency (Hz)</th><th>FREQM</th><th>FREQL</th></tr><tr><td>462</td><td>0C</td><td>52</td></tr><tr><td>1100</td><td>1D</td><td>55</td></tr><tr><td>1650</td><td>2C</td><td>00</td></tr><tr><td>1850</td><td>31</td><td>55</td></tr><tr><td>2100</td><td>38</td><td>00</td></tr></table></td></tr>
<tr><td>HD2W</td><td>Half Duplex (Two Wire)</td><td>1:6:2</td><td>When control bit HD2W is a zero and at device reset, full duplex (4-wire) operation is enabled. When it is a one, half duplex (2-wire) operation is enabled.</td></tr>
<tr><td>IFIX</td><td>Eye Fix</td><td>1:6:7</td><td>When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB. IFIX is reset to 0 by device reset.</td></tr>
</table>

Table 15. R201/26DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>LAEN</td><td>Link Amplitude Equalizer Enable</td><td>0:5:3</td><td>The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table:

<table>
<tr><th>LAEN</th><th>A3L</th><th>Curve Matched</th></tr>
<tr><td>0</td><td>X</td><td>No Equalizer</td></tr>
<tr><td>1</td><td>0</td><td>U.S. Survey Long</td></tr>
<tr><td>1</td><td>1</td><td>Japanese 3-Link</td></tr>
</table>
The link amplitude equalizer responses are given in the following table.

Link Amplitude Equalizer
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr>
<tr><td>1000</td><td>-0.27</td><td>-0.13</td></tr>
<tr><td>1400</td><td>-0.16</td><td>-0.08</td></tr>
<tr><td>2000</td><td>-0.33</td><td>+0.16</td></tr>
<tr><td>2400</td><td>-1.54</td><td>+0.73</td></tr>
<tr><td>2800</td><td>-5.98</td><td>-2.61</td></tr>
<tr><td>3000</td><td>-8.65</td><td>+3.43</td></tr>
</table></td></tr>
<tr><td>LCEN</td><td>Loop Clock Enable</td><td>0:4:0</td><td>When control bit LCEN is a one, the transmitter clock tracks the receiver clock. LCEN is reset to 0 by device reset.</td></tr>
<tr><td>LDEN</td><td>Link Delay Equalizer Enable</td><td>0:5:2</td><td>The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table:

<table>
<tr><th>LDEN</th><th>D3L</th><th>Curve Matched</th></tr>
<tr><td>0</td><td>X</td><td>No Equalizer</td></tr>
<tr><td>1</td><td>0</td><td>U.S. Survey Long</td></tr>
<tr><td>1</td><td>1</td><td>Japanese 3-Link</td></tr>
</table>
The link delay equalizer responses are given in the following table.

Link Delay Equalizer
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Delay Relative to 1700 Hz (Microseconds)</th></tr>
<tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr>
<tr><td>800</td><td>-498.1</td><td>-653.1</td></tr>
<tr><td>1200</td><td>-188.3</td><td>-398.5</td></tr>
<tr><td>1600</td><td>-15.1</td><td>-30.0</td></tr>
<tr><td>1700</td><td>+0.0</td><td>+0.0</td></tr>
<tr><td>2000</td><td>-39.8</td><td>+11.7</td></tr>
<tr><td>2400</td><td>-423.1</td><td>-117.1</td></tr>
<tr><td>2800</td><td>-672.4</td><td>-546.3</td></tr>
</table></td></tr>
<tr><td>L3ACT</td><td>Local Analog Loopback Activate</td><td>0:4:7</td><td>When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3. L3ACT is reset to 0 by device reset.</td></tr>
<tr><td>L4ACT</td><td>Remote Analog Loopback Activate</td><td>0:4:6</td><td>When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4. L4ACT is reset to 0 by device reset.</td></tr>
<tr><td>L4HG</td><td>Loop 4 High Gain</td><td>0:4:5</td><td>When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB. L4HG is reset to 0 by device reset.</td></tr>
</table>

Table 15. R201/26DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
MHLD	Mark Hold	0:7:4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones). MHLD is reset to 0 by device reset.
(None)	RAM Access XB	2:5:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word X (2:3 and 2:2).
(None)	RAM Access XS	1:5:0–7	Contains the RAM access code used in reading chip 1 RAM locations via word X (1:3 and 1:2).
(None)	RAM Access XT	0:F:0–7	Contains the RAM access code used in reading chip 0 RAM locations via word (0:1 and 0:0).
(None)	RAM Access YB	2:4:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word Y (2:1 and 2:0).
(None)	RAM Access YS	1:4:0–7	Contains the RAM access code used in reading chip 1 RAM locations via word Y (1:1 and 1:0).
(None)	RAM Data XBL	2:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XBM	2:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XSL	1:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 1.
(None)	RAM Data XSM	1:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 1.
(None)	RAM Data XTL	0:0:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 0.
(None)	RAM Data XTM	0:1:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 0.
(None)	RAM Data YBL	2:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YBM	2:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YSL	1:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus. See 'Receiver Data.'
(None)	RAM Data YSM	1:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 1.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
RBPS	Receiver Data Rate (bps)	1:6:0	When control bit RBPS is a one and at device reset, the receiver data rate is set to 2400 bps. When control bit RBPS is a zero, the receiver data rate is set to 1200 bps.
(None)	Receiver Configuration	1:6:0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB). The bits included in this field and their initial values are RBPS (1: 2400 bps), RLRT (0: RLSD Response Time = 6 ms), RV26 (0: V.26 Alternate B), HD2W (0: Full Duplex, 4-Wire), and TDET (0: Tone Detector Off).
(None)	Receiver Data	1:0:0–7	The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data. When using receiver parallel data mode, the registers 1:3 through 1:0 can not be used for reading the chip 1 RAM.
RLRT	RLSD Response Time	1:6:1	When control bit RLRT is a zero and at device reset, the RLSD Response Time is set to 6 ms. When control bit RLRT is a one, the RLSD Response Time is set to 14 ms.

Table 15. R201/26DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RPDM	Receiver Parallel Data Mode	1:7:4	When control bit RPDM is a one, the receiver supplies channel data to the receiver data register (1:0) as well as to the hardware serial data output. (See Receiver Data). RPDM is reset to 0 by device reset.
RSB	Receiver Setup Bit	1:E:3	When the host processor changes the receiver configuration field or writes a one in the SQH or SQHT control bits, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective. Worst case setup time is 2 baud times.
RSDA	Receiver Sample Data Available	1:E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0. RSDA goes to a zero when the host processor reads data from register 1:0.
RSIA	Receive Sample Interrupt Active	1:E:7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is a one.
RTDIS	Receiver Training Disable	1:7:0	When control bit RTDIS is a one, the receiver is prevented from recognizing a training sequence and entering the training state. RTDIS is reset to 0 by device reset.
RTH	Receiver Threshold Field	1:7:6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH** / **RLSD On** / **RLSD Off** 00 / > −43 dBm / < −48 dBm 01 / > −33 dBm / < −38 dBm 10 / > −26 dBm / < −31 dBm 11 / > −16 dBm / < −21 dBm The RTH bits are reset to 00 by device reset.
RTS	Request-to-Send	0:7:7	When control bit RTS is set to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are ORed by the modem. RTS is reset to 0 by device reset.
RTSD	Request-to-Send/ Disable Receiver	1:F:7	When control bit RTSD is a zero and at device reset, the receiving circuits are enabled. When control bit RTSD is a one, the receiving functions are put in an idle mode. This function is intended to be used for half duplex (2-wire) modem operation and gives the user the ability to turn off the receiver when transmitting.
RV26	Receiver V.26 Alt. A/Alt. B Select	1:6:5	When control bit RV26 is a zero and at device reset, V.26 Alternate B is selected. When control bit RV26 is a one, V.26 Alternate A is selected.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, and at device reset, the transmitter scrambler circuit is removed from the data path. This bit must match the selection in the turn-on sequence selection field (see table 4) i.e. the scrambler must be either enabled or disabled in both.
SQH	Receiver Squelch	1:F:6	When control bit SQH is set to a one, the receiver is squelched, $\overline{RLSD}$ is turned off and RXD is clamped to all marks. SQH only affects the receiver operation when a half duplex receiver configuration has been selected. (see RSB.)
SQHT	Receiver Squelch Time	1:F:5	This bit controls the duration of the squelch clamping (see SQH). If SQHT is a zero, the squelch lasts for 100 ms, but if it is a one, the squelching lasts for 148 ms. SQHT is reset to zero by device reset.
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one.
TBPS	Transmitter Data Rate (bps)	0:6:4	When control bit TBPS is a one and at device reset, the transmitter data rate is set to 2400 bps. When control bit TBPS is a zero, the transmitter data rate is set to 1200 bps.
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.

Table 15. R201/26DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TIE	Transmitter Interrupt Enable	0:E:2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.
TDET	Tone Detector Enable	1:6:3	When control bit TDET is a one, the tone detector is disabled. TDET is reset to zero by device reset.
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL** — **Transmitter Analog Output*** 000 — −1 dBm ±1 dB 001 — −3 dBm ±1 dB 010 — −5 dBm ±1 dB 011 — −7 dBm ±1 dB 100 — −9 dBm ±1 dB 101 — −11 dBm ±1 dB 110 — −13 dBm ±1 dB 111 — −15 dBm ±1 dB *Each step above is a 2 ±0.2 dB change The TLVL bits are reset to 000 by device reset.
TOD	Train-on Data	1:6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on data. TOD is reset to 0 by device reset.
TODF	Train-On Data Flag	1:A:7	Indicates Train On Data in process.
$\overline{TONE}$	Tone Detect	1:9:2	$\overline{TONE}$ indicates with a zero the presence of energy in the 345–650 ±10 Hz frequency range. For call progress purposes, the user may determine which tone is present by determining the duty cycle of the $\overline{TONE}$ bit.
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0) rather than the serial hardware data input. TPDM is reset to 0 by device reset.
(None)	Transmitter Configuration	0:6:0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB) The bits included in this field and their initial values are DTMF (0: DTMF Generation = Off), TTONE (0: Transmit Tone = Off), TV26 (0: V.26 Alternate B), TBPS (1: Transmitter Data Rate = 2400 bps, and Turn-on Sequence Selector (2: see Table 4).
(None)	RAM DATA XTL/ Transmitter Data/DDR	0:0:0–7	The host processor conveys output data to the transmitter in the parallel mode by writing a data byte to the transmitter data register. When the transmitter is configured for DTMF dialing, this register becomes the Dial Digit Register (DDR). Refer to figure 3 for the proper Auto Dialing Procedure.
TSB	Transmitter Setup Bit	0:E:3	When the host processor changes the transmitter configuration field (DTMF, TTONE, TV26, TBPS, or the Turn-on sequence selector field), the host must write a one in this control bit. TSB resets to zero when the change becomes effective. Worst case setup time is 2 baud + turnoff sequence + training (if applicable).
TTDIS	Transmitter Train Disable	0:7:6	When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times. TTDIS is reset to 0 by device reset.

Table 15. R201/26DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TTONE	Transmit (Single) Tone Output Select	0:6:7	When this bit is set to a one, the single tone output mode is selected. To initiate a tone, the TSB bit must be set to a one for each tone desired. The R201/26DP does not perform a timeout on the tone; thus the host must perform its own timeout to know when to start the next tone. TTONE is reset to zero by device reset. The proper operational sequence to generate a tone is given below: 1. Set the TTONE bit. 2. Load the desired value into FREQM/FREQL (see FREQL/FREQM) 3. Set the TSB bit. 4. Wait for desired timeout. 5. Repeat steps 2, 3, and 4 until all desired tones have been generated. 6. Reset the TTONE bit.
(None)	Turn-on Sequence Selector Field	0:6:3–0	Selects the turn-on sequence timing and whether or not the scrambler is in the circuit. See 'SDIS' and Table 4. This field is set to 0010 (Turn-on sequence number 2) by device reset.
TV26	Transmitter V.26 Alt. A/Alt. B Select	1:6:5	When control bit TV26 is a zero and at device reset, V.26 Alternate B is selected. When control bit TV26 is a one, V.26 Alternate A is selected.
T2	T/2 Equalizer Select	1:7:1	When control bit T2 is a one, an adaptive equalizer with two taps per baud is used. When T2 is a zero, the equalizer has one tap per baud. The total number of taps remains the same for both cases. T2 is reset to 0 by device reset.
WBRD	Write to Baud Rate Device (Receiver #2)	1:7:2	When control bit WBRD is a one, data is written into receiver device 2. WBRD is reset to zero by device reset.
WSRD	Write to Sample Rate Device (Receiver #1)	1:7:3	When control bit WSRD is a one, data is written into receiver device 1. WSRD is reset to zero by device reset.
XCEN	External Clock Enable	0:7:1	When control bit XCEN is a one, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A. XCEN is reset to 0 by device reset.

POWER-ON INITIALIZATION

When power is applied to the R201/26DP, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the $\overline{POR}$ cycle is generated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.26B/Bell 201B/C, short train, full-duplex, T, no echo protector tone, serial data mode, internal clock, transmitter output level set to -1 dBm ± 1 dB, receiver threshold set to -43 dBm, eye pattern selectable, train-on data disabled, the tone generator is off, $\overline{RLSD}$ response time set to 6 ms, the tone detector is off, no extended squelch, and squelch clamping set to 100 ms.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or more applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after $\overline{POR}$ is removed.

PERFORMANCE

Functioning as either a Bell 201 or a V.26/V.26 bis type modem, the R201/26DP provides the user with excellent, reliable performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT recommendation V.56. Bit error rates are measured at a received line signal level of -20 dBm as illustrated in Figures 4 & 5. Figure 6 shows the BER test equipment set up.

TYPICAL PHASE JITTER

At 2400 bps (V.26 Alternate A or B), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler not inserted, equalizer not inserted).

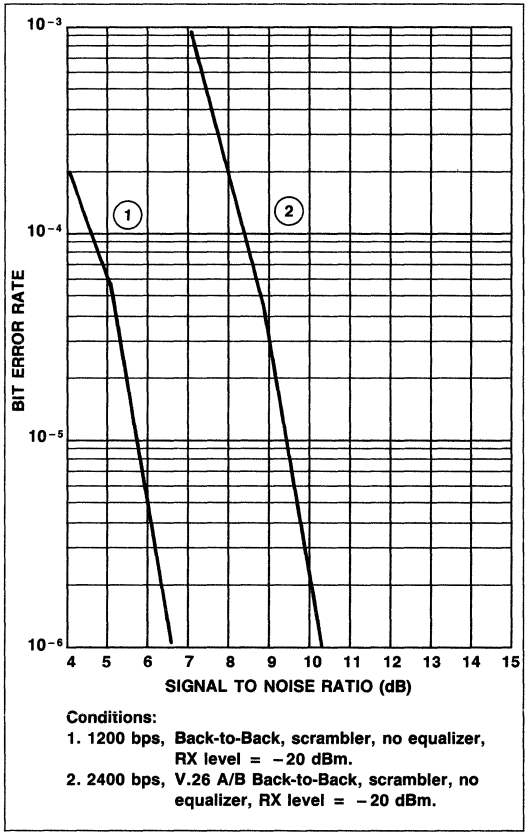


Figure 4. Typical BER Performance Back-to-Back.

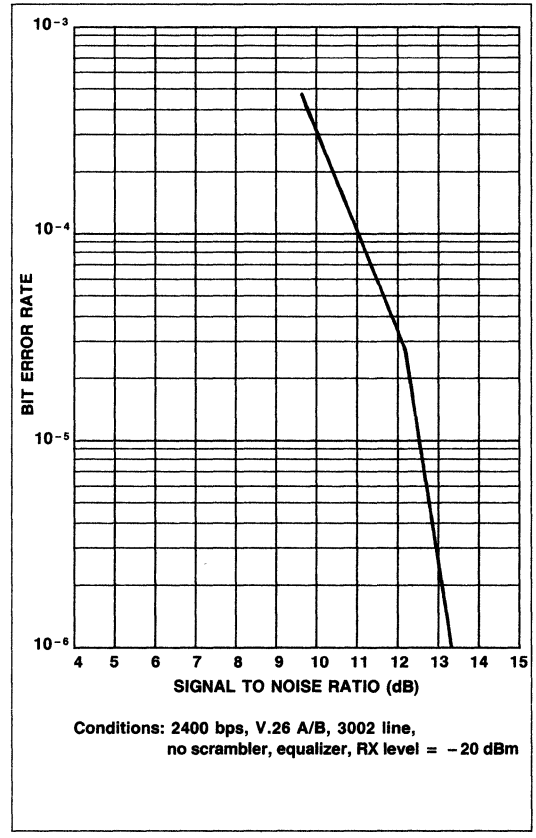


Figure 5. Typical BER Performance 3002 Unconditioned Line.

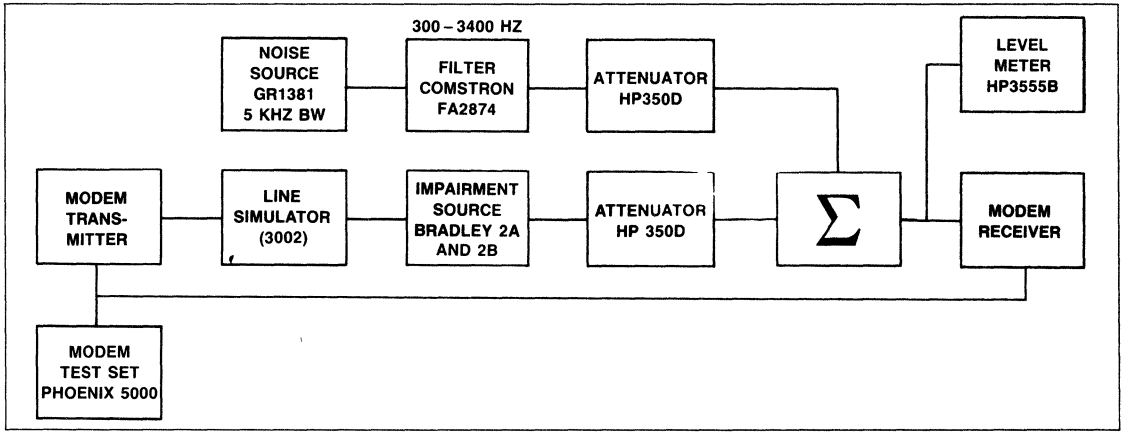


Figure 6. BER Performance Test Set-up

GENERAL SPECIFICATIONS

Table 10. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	550 mA	<700 mA
+12 Vdc	±5%	5 mA	< 10 mA
-12 Vdc	±5%	25 mA	< 50 mA

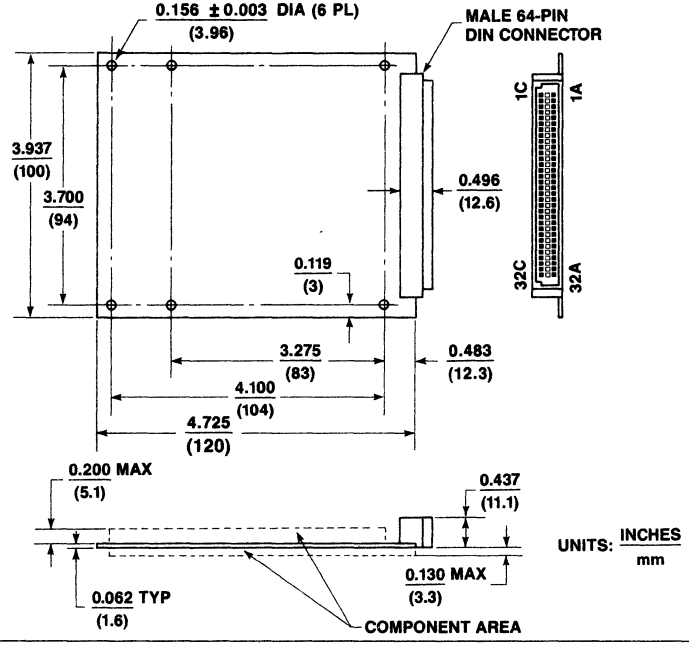
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	-40°C to +80°C (-40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	-200 feet to +10,000 feet

Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Height	0.40 in. (10.2 mm)
Weight (max):	3.6 oz. (100 g)
Lead Extrusion (max.):	0.100 in. (2.54 mm)



R201/26DP Board Dimensions and Pin Locations

Rockwell

RC1212
1200 bps Full-Duplex Modem Family

INTRODUCTION

The RC1212 is Rockwell's new 1200 bps, full-duplex OEM modem family. The RC1212 operates over the public switched telephone network, as well as on point-to-point leased lines. The RC1212 is available in a dual-in-line (DIP) module (RC1212/DM and RC1212/DME), or as a two-device set (RC1212/DS).

The basic RC1212 modem meets the requirements specified in CCITT V.22 A/B, and V.21, as well as Bell 212A and Bell 103. The RC1212/DME includes a V.23/Bell 202 device to provide asynchronous, full-duplex operation at 1200 bps with backwards channel up to 150 bps.

The RC1212/DM and RC1212/DME modem modules contain additional circuitry to interface the modem to a Data Access Arrangement (DAA). The DIP module (about seven square inches) can be handled by automated manufacturing equipment for installation and soldering onto a host board.

A high performance modem engine, the RC1212/DS is the functional and performance equivalent of Rockwell's R1212 device set with the following enhancements: 2-device solution, fully CMOS, V.21 mode, and data transfer over the microprocessor bus interface.

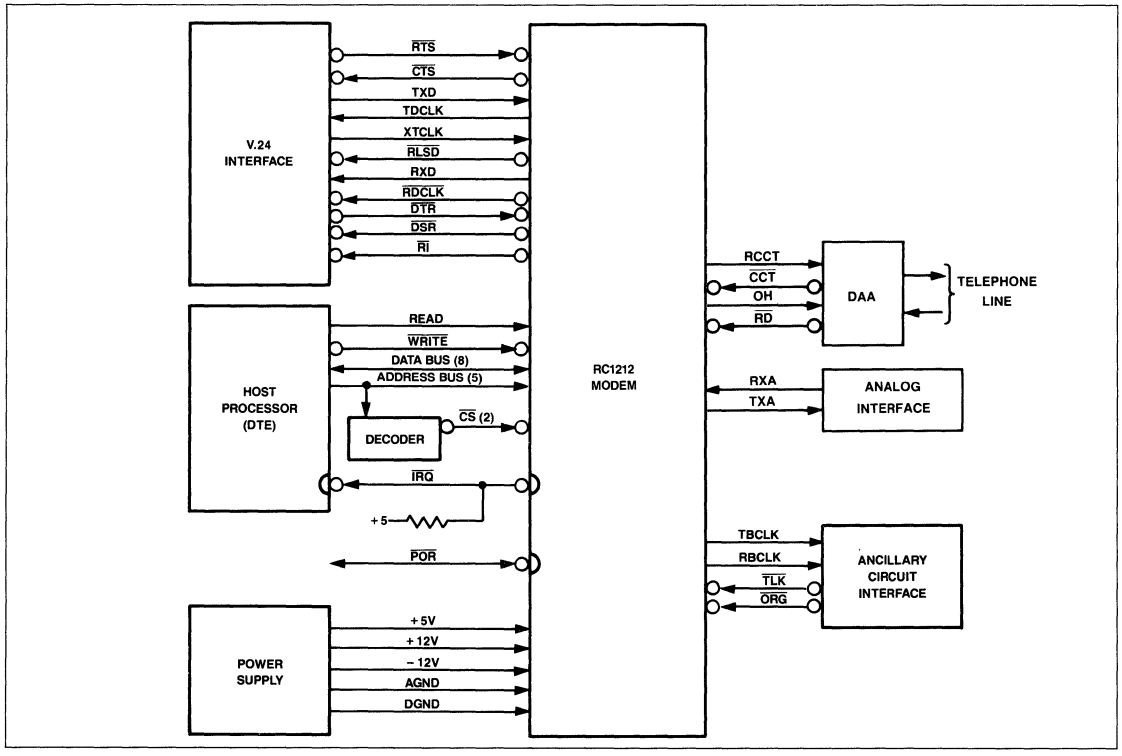
Data may be transferred to and from the modem either serially or in parallel over the microprocessor bus interface. These options, combined with a user accessible, dual port scratch pad RAM (via the microprocessor bus), provide the designer maximum flexibility in customizing the RC1212 for a wide variety of functional requirements.

COMPATIBILITY

Product	Pin and Firmware Compatible with	Pin Compatible with
RC1212/DS	RC2424/DS	
RC1212/DM	RC1212/DME, RC2424/DM and RC2424/DME	R1212/DM and R2424/DM
RC1212/DME	RC1212/DM, RC2424/DME and RC2424/DM	R1212/DM and R2424/DM

FEATURES

- Compatibilities
  - — All Models: CCITT V.22A/B and V.21 and Bell 212A and 103
  - — RC2424/DME: Above Modes Plus CCITT V.23 and Bell 202
- Synchronous: 1200 bps, 600 bps
- Asynchronous: 1200 bps, 600 bps (+1%, +2.3%, −2.5%); 0-300 bps
- Character Length: 8, 9, 10, or 11 bits
- Dynamic Receive Range: 0 dBm to −48 dBm
- Facilitates Auto Speed Recognition
- Fallback Capability
- Programmable Call Progress Tone Detection
- DTE Interface
  - — Functional: Microprocessor Bus (Data/Configuration/Control) and CCITT V.24 (RS-232-C) (Data/Control)
  - — Electrical: TTL and CMOS compatible
- Equalization
  - — Auto Adaptive (Receive)
  - — Fixed Compromise (Transmit)
- Auto/Manual Answer
- Programmable Pulse and DTMF Tone Generation
- Selectable Guard Tone Generation (1800 Hz or 550 Hz)
- Test Modes
  - — Local Analog Loopback
  - — Remote Digital Loopback
  - — Digital Loopback
  - — Self Test
- Low Power Consumption
  - — RC1212/DS and RC1212/DM: 400 mW (Typical)
  - — RC1212/DME: 500 mW (Typical)
- Packaging
  - — RC1212/DS 2-Device Set:
    Digital Signal Processor (DSP): 64-pin QUIP, 68-pin PLCC
    Analog Filter: 40-pin DIP, 44-pin PLCC
  - — RC1212/DM and RC1212/DME Modules
    50.8 mm × 88.9 mm (2.0 in. × 3.5 in.)



RC1212 Modem Functional Interconnect Diagram

Rockwell

RC2424
2400 bps Full-Duplex Modem Family

INTRODUCTION

The RC2424 is Rockwell's new 2400 bps, full-duplex OEM modem family. The RC2424 operates over the public switched telephone network, as well as on point-to-point leased lines. The RC2424 is available in a dual-in-line (DIP) module (RC2424/DM and RC2424/DME), or as a two-device set (RC2424/DS).

The basic RC2424 modem meets the requirements specified in CCITT V.22 bis, V.22 A/B, and V.21, as well as Bell 212A and Bell 103. The RC2424/DME includes a V.23/Bell 202 device to provide asynchronous, full-duplex operation at 1200 bps with backwards channel up to 150 bps.

The RC2424/DM and RC2424/DME modem modules contain additional circuitry to interface the modem to a Data Access Arrangement (DAA). The DIP module (about seven square inches) can be handled by automated manufacturing equipment for installation and soldering onto a host board.

A high performance modem engine, the RC2424/DS is the functional and performance equivalent of Rockwell's R2424 device set with the following enhancements: 2-device solution, fully CMOS, V.21 mode, and data transfer over the microprocessor bus interface.

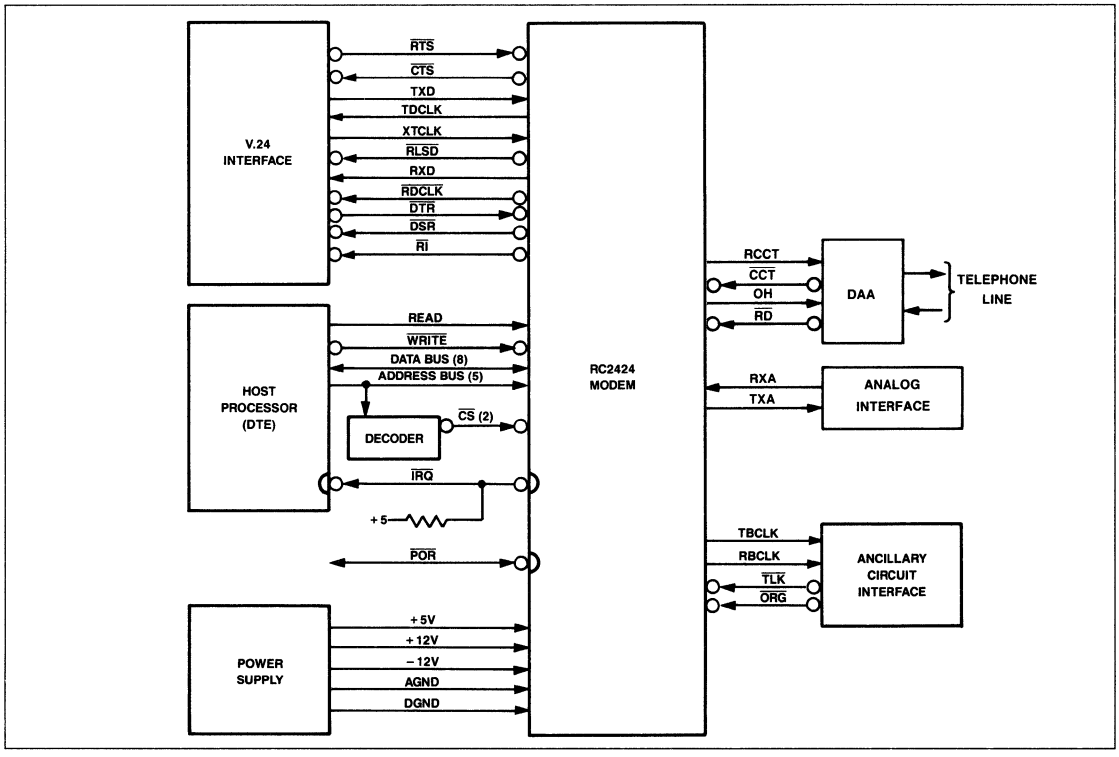
Data may be transferred to and from the modem either serially or in parallel over the microprocessor bus interface. These options, combined with a user accessible, dual port scratch pad RAM (via the microprocessor bus), provide the designer maximum flexibility in customizing the RC2424 for a wide variety of functional requirements.

COMPATIBILITY

Product	Pin and Firmware Compatible with	Pin Compatible with
RC2424/DS	RC1212/DS	
RC2424/DM	RC2424/DME, RC1212/DM and RC1212/DME	R2424/DM and R1212/DM
RC2424/DME	RC2424/DM, RC1212/DME and RC1212/DM	R2424/DM and R1212/DM

FEATURES

- Compatibilities
  - — All Models: CCITT V.22 bis, V.22A/B and V.21 and Bell 212A and 103
  - — RC2424/DME: Above Modes Plus CCITT V.23 and Bell 202
- Synchronous: 2400 bps, 1200 bps, 600 bps
- Asynchronous: 2400 bps, 1200 bps, 600 bps (+1%, +2.3%, −2.5%); 0-300 bps
- Character Length: 8, 9, 10, or 11 bits
- Dynamic Receive Range: 0 dBm to −48 dBm
- Facilitates Auto Speed Recognition
- Fallback Capability
- Programmable Call Progress Tone Detection
- DTE Interface
  - — Functional: Microprocessor Bus (Data/Configuration/Control) and CCITT V.24 (RS-232-C) (Data/Control)
  - — Electrical: TTL and CMOS compatible
- Equalization
  - — Auto Adaptive (Receive)
  - — Fixed Compromise (Transmit)
- Auto/Manual Answer
- Programmable Pulse and DTMF Tone Generation
- Selectable Guard Tone Generation (1800 Hz or 550 Hz)
- Test Modes
  - — Local Analog Loopback
  - — Remote Digital Loopback
  - — Digital Loopback
  - — Self Test
- Low Power Consumption
  - — RC2424/DS and RC2424/DM: 400 mW (Typical)
  - — RC2424/DME: 500 mW (Typical)
- Packaging
  - — RC2424/DS 2-Device Set:
    Digital Signal Processor (DSP): 64-pin QUIP, 68-pin PLCC
    Analog Filter: 40-pin DIP, 44-pin PLCC
  - — RC2424/DM and RC2424/DME Modules
    50.8 mm × 88.9 mm (2.0 in. × 3.5 in.)



RC2424 Modem Functional Interconnect Diagram

RDAA
ROCKWELL DATA ACCESS ARRANGEMENT MODULE

SECTION 1 — INTRODUCTION

This document is an aide to customers installing, operating and troubleshooting the Rockwell Data Access Arrangement (RDAA) Module designed and manufactured by Rockwell International.

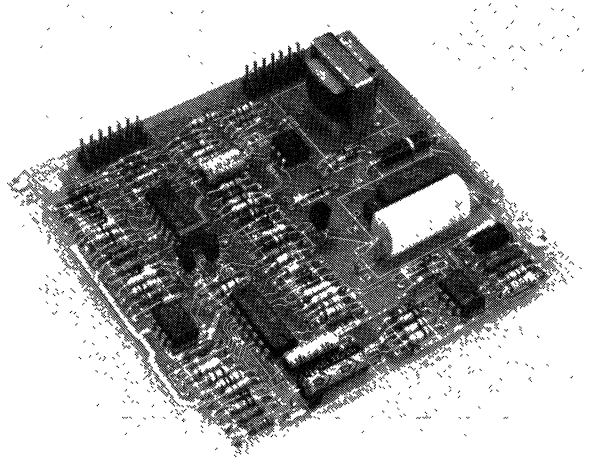
THE RDAA MODULE

The RDAA Module enables the modem user to make direct connections of their modems to the domestic switched telephone network. The RDAA is completely registered with the Federal Communications Commission under Rules Part 68. Therefore, *no* user re-registration of OEM data communication equipment is necessary when used with the RDAA. This means a definite cost-savings for the OEM equipment designer.

In addition to establishing your desired data transmission path, the RDAA also features an automatic answering function, line surge and hazardous voltage protection, switch hook status indication, ringing indication and automatic signal level control. Automatic dialing can be performed by pulsing the OH relay or by transmitting tone pairs.

FEATURES

- Pre-registered (under FCC Rules, Part 68) for direct connection to dial telephone network
- Integral Data Access Arrangement (DAA)
- Automatic dialing—pulse or tone
- Establishes data transmission path
- Automatic answering function
- Surge and hazardous voltage protection
- Switch hook status indication
- Ringing indication
- Automatic line signal output limiting
- Programmable or Permissive (strap selectable) connection arrangements
- Small size (approximately 3.95″ by 3.94″) (100 mm. by 100 mm.)



RDAA Module

The RDAA is easily incorporated into the users end product by either using the provided mounting holes, and/or using the card-guides without card-edge connector. The small size of the RDAA makes it ideal for piggyback type mounting.

The Rockwell RDAA printed circuit board is 3.94 inches (100 mm.) in width and 3.94 inches (100 mm.) in depth.

SELECTABLE CONFIGURATIONS

As a prerequisite, telephone companies require that the signal level received at their local central office not exceed −12 dBm. Several different connection arrangements have been established (as documented in the FCC Rules, Part 68) to meet this requirement.

By jumper selection (Figure 1) the RDAA can be configured to operate in either the Programmable (PG) or Permissive (PM) connection arrangement. This is accomplished by placing the jumper in either the W2 or W1 locations for the desired mode. W1 jumper in, W2 jumper out for the permissive mode. W2 jumper in, W1 jumper out for the programmable mode.

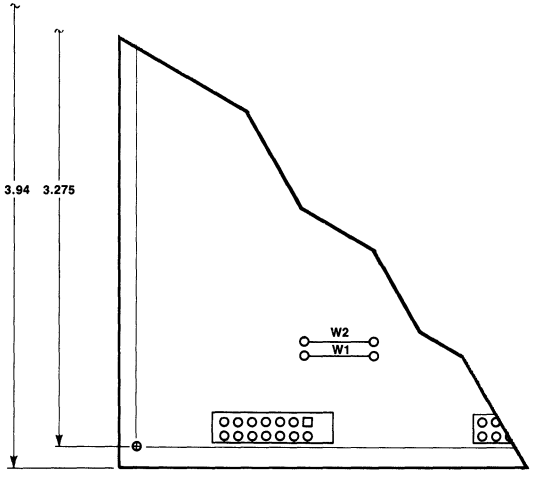


Figure 1. RDAA Module Jumper Selection Location

When using the Programmable connection arrangement, the maximum signal level allowed to be transmitted across T and R is set by a resistor installed by the telephone company in their wall jack (RJ45S or RJ41S) at the customer location. The resistor interacts with the RDAA through the leads PR and PC to program the maximum output level in one dB steps between −12 dBm and 0 dBm. Selection of the resistor from thirteen possible values is based on loop loss measurements performed by the telephone jack installer. The Programmable arrangement provides for the transmission of the maximum allowable amount of power. Therefore, this arrangement offers optimum performance over long loops.

When the Permissive connection arrangement is employed, the maximum signal output level across T and R is fixed at −9 dBm. The Permissive jacks (RJ11C) used for line connections are the same jacks used for standard voice installations. Therefore, this arrangement provides for greater mobility of user equipment.

RDAA DIMENSIONS

The dimensions for the RDAA Module are given in Figure 2.

MATING CONNECTORS

The mating connectors of the RDAA are as follows:

1. Two row (14 pins) ribbon type connectors .1″ spacing between pins.

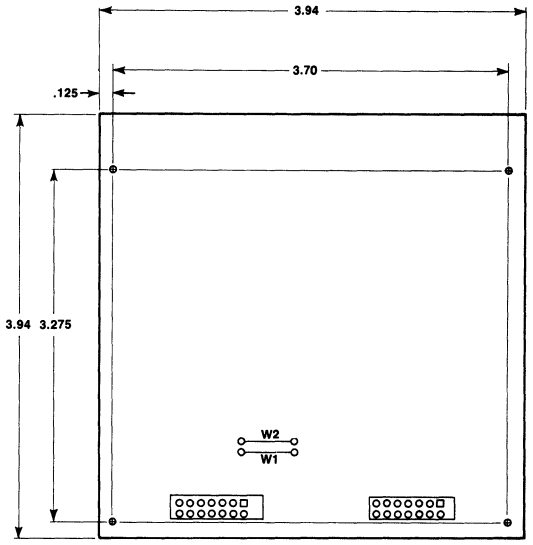


Figure 2. RDAA Module Dimensions

SECTION 2 — INTERFACE DESCRIPTION

INTERFACE CIRCUIT DESCRIPTION

The following paragraphs describe in detail the RDAA interface circuits shown in the block diagram (Figure 3) and the interface circuits listing (Table 2-1).

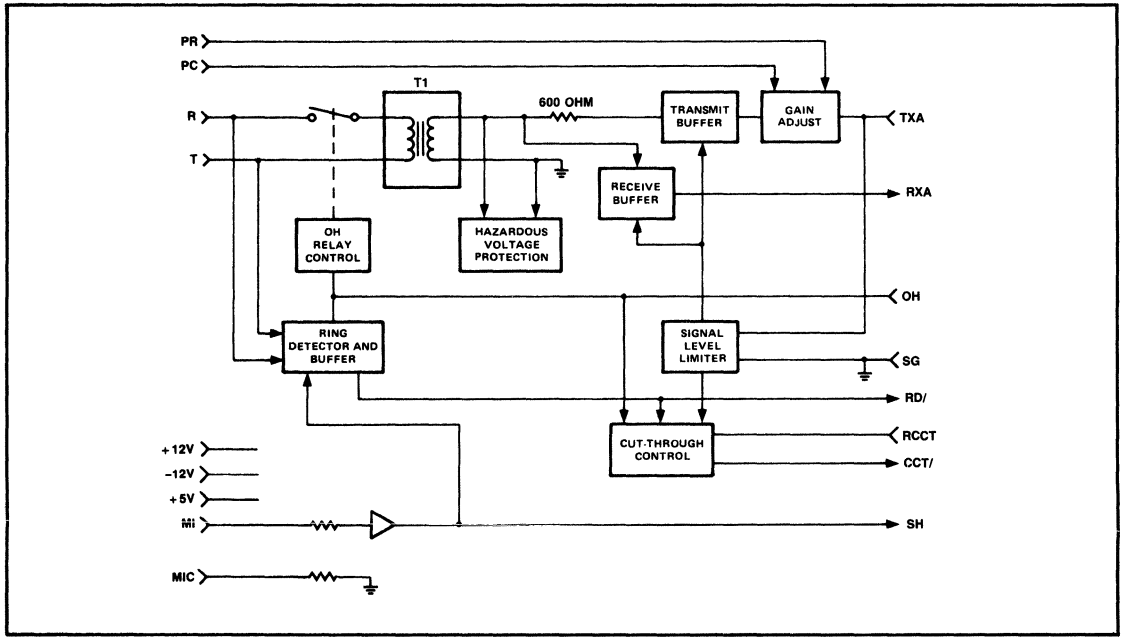


Figure 3. RDAA Functional Block Diagram

Table 2-1. RDAA Interface Circuits

Lead Designation	Signal Direction To: User	RDAA	Both	Function
R, T			X	Transmission leads for data signals.
MI, MIC			X	Leads to telephone set switch hook.
PR, PC			X	Leads to programming resistor.
+5V, +12V, −12V		X		DC power required.
SG			X	Signal ground required.
RD/	X			Ringing signal present indication.
RCCT		X		To request data transmission path cut through.
OH		X		To control Off-Hook relay.
SH	X			Status of telephone set switch hook.
CCT/	X			Transmission path cut through indication.
TXA		X		Lead to modem output.
RXA	X			Lead to modem input.

SG

The SG (Signal Ground) is the common reference for all modem interface signals.

RD/

RD/ (Ring Detect) indicates to the user by an ON (Low) condition that a ringing signal is present. The RD/ signal will not respond to momentary bursts of ringing less than 125 ms in duration, or to less than 40V rms, 15 to 68 Hz appearing across Tip and Ring with respect to ground. RD/ is also used to disable the transmission path. The electrical characteristics of the RD/ signal are shown in Table 2-2.

Table 2-2. Output Signals RD/ SH and CCT/ Characteristics

Output Logic State	Output Levels
LOW	0.0 to 0.4V while sinking < 1.6 ma
HIGH	2 4 to 5.0V while sourcing $< 40\ \mu A$

RCCT

RCCT (Request Coupler Cut-Through) is used to request that a data transmission path through the RDAA be connected to the telephone line. When RCCT goes OFF (Low), the cut-through buffers are disabled and CCT will go OFF (High) within 1 millisecond. RCCT must be OFF (Low) during dial pulsing but ON (High) for tone address signaling. The electrical characteristics of the RCCT signal are shown in Table 2-3.

Table 2-3. Input Signals RCCT and OH Characteristics

Input Logic State	Input Levels
OFF or LOW	0.0 to 0.8V, load current ≤ 0.36 ma
ON or HIGH	RCCT = 2.0 to 5.0V, load current $\leq 20\ \mu a$
	OH = 2.0V, load current $\leq 100\ \mu a$
	5.0V, load current $\leq 250\ \mu a$

OH

OH controls the OFF-HOOK relay. Applying an ON (High) signal to OH closes the OH relay and establishes a DC path between T and R. Maximum delay between the ON signal to OH and the close of the OH relay is 10 ms. When originating a call, an ON (High) signal is used to request dial tone. After detecting dial tone, OH can be pulsed to generate the dial pulses corresponding to the number of the called station (see Section 4.2). On incoming calls, an ON (High) signal to the OH lead initiates the answering sequence (see Section 4.1). The characteristics of the OH signal is shown in Table 2-3.

NOTE

WARNING. If OH is asserted to a logic high before the incoming call ring signal is completed, the OH reed relay switch contacts may suffer degradation.

SH

An ON (High) signal on the SH lead indicates to the user that the associated telephone (if used) is in the talk mode i.e., a contact closure exists between MI and MIC. The characteristics of the SH signal are shown in Table 2-2.

CCT/

CCT/ is the Coupler Cut Through. An ON (Low) signal to the CCT/ lead indicates to the user that the data transmission path through the RDAA is connected. The ON (Low) state does not indicate the status of the telephone line or connection. The characteristics of the CCT/ signal are shown in Table 2-2.

TXA

TXA (Transmit Analog) is the lead from modem transmitter output. This lead should be tied to GND when the modem is in the receive only mode.

RXA

RXA (Receive Analog) is the lead to modem receiver input. This lead may be left open when the modem is in the transmit-only mode.

POWER REQUIREMENTS

The following power must be provided at the RDAA interface.

A. +12 VDC $\pm$5% @ 15 ma with a maximum ripple of 50 mv peak-to-peak

B. +5 VDC $\pm$5% @ 20 ma with a maximum ripple of 100 mv peak-to-peak

C. -12 VDC $\pm$ 5% @ 15 ma with a maximum ripple of 50 mv peak-to-peak.

HAZARDOUS VOLTAGE PROTECTION

Lightning induced surge voltages and other hazardous voltages are limited to 10.0 volts peak between the secondary leads of the coupling transformer T1. The isolation between the relay contacts and coils provides the protection of the telephone line from hazardous voltages appearing on any control lead.

RING DETECTOR AND TIMER

When the Ring Detector detects the presence of a ringing signal ranging from 15.3 to 68 Hz with voltage levels of 40 to 150 VRMS across Tip and Ring (T and R) leads, after a delay of 125 ms to 500 ms, it will send an RD/ (Ring Detect) signal to the user's data terminal equipment (DTE). If the DTE is conditioned for answering, the DTE will return an ON signal on OH and RCCT. The OH signal closes the OH relay and starts a timer. The timer is used to provide a quiet interval of more than two seconds between the closing of OH relay and the connection of data transmission path. This allows the telephone company to properly engage their billing equipment. After this delay the CCT/ interface lead goes ON (Low) and data transmission may begin.

RD/ will go OFF (High) in less than 400 MSEC after the ringing signal is stopped. The ring detector is disabled when OH is ON (High) or SH is ON (High).

SIGNAL LEVEL LIMITER AND GAIN CONTROL CIRCUITRY

The limiter monitors the signal level applied to the RDAA input lead TXA and is unaffected by the level of receive signal. When the applied signal amplitude becomes greater than +7 dBm for a period of 1.3 to 3 seconds, the transmission path is disconnected via the transmit and receive buffers, and the output signal CCT/ will go OFF (High).

NOTE

The off-hook relay is not affected by the limiting function, therefore, so triggering the limiting function need not result in call termination.

Reducing the input signal amplitude to less than +7 dBm will reset the limiter in less than 4 milliseconds, restore the data transmission path, and cause the signal CCT to go ON (Low).

In order not to activate the limiter during normal operation, care must be taken to ensure that the maximum signal amplitude into the RDAA input TXA never exceeds +6 dBm. If the modem output has a tolerance of ± 1 dB, then it is recommended to set the modem output to +5 dBm (± 1 dB), so that the maximum signal amplitude into TXA is 6 dBm.

The output control circuitry contains a variable gain buffer which reduces the RDAA output to the maximum allowed level across T and R. When the RDAA is jumpered to operate in the Programmable mode, the resistor in the telephone company wall jack sets the output level to one of thirteen possible values. If the RDAA is jumpered to operate in the Permissive mode, then an internal resistor will set the output to a fixed value. The relationship between the RDAA input amplitude (in dBm) across TXA and GND and the nominal RDAA output level across T and R is given below:

A. For Programmable mode: output level across T and R = (input amplitude at TXA −7 dB + (Programmed level set by wall jack resistor).

B. For Permissive mode: output level across T and R = (input amplitude at TXA) −16 dB.

IMPEDANCE SPECIFICATIONS

On-Hook DC:	The DC resistance between T and R, and between either T or R and signal ground are greater than 10 megohms for DC voltages up to 100 volts.
On-Hook AC:	The on-hook AC impedance measured between T and R is less than 40K ohms (15.3 Hz minimum).
Off-Hook DC:	Less than 100 ohms.
Off-Hook AC:	600 ohms nominal when measured between T and R.
TXA and GND:	2 megohms typical (operational amplifier voltage follower input impedance).
RXA and GND:	75 ohms typical (operational amplifier voltage follower output impedance).

INSERTION LOSS

There is no insertion loss for the RDAA. The RDAA contains a receive buffer which compensates for transformer insertion loss. For this reason, additional receive buffering is not necessary.

SECTION 3 — INSTALLATION/CHECKOUT

RDAA CONNECTION TO TELEPHONE LINE

Connection of the telephone line interface pins of the RDAA to the network shall be made via standard jacks and plugs as shown in Figure 4. Cable color codes are also shown in Figure 4. A number of telephone line cord manufacturers produce the standard plugs and cables (Meyer Wire Co., Hamden, CT; Virginia Plastics, Roanoke, VA, etc.)

TELEPHONE SET AND JACK ORDERING INFORMATION

If it is desirable to have manual call origination or alternate voice capability, an exclusion key telephone set may be ordered from a local telephone company. The telephone line may be transferred to the telephone set by lifting both the handset and the exclusion key, if the telephone is configured as Data Set Controls Line. This operation is for manual origination or alternate voice transfer (refer to paragraph 4.4 for manual origination procedure). A call may be terminated by replacing the handset in its cradle and taking OH low if OH is not already low.

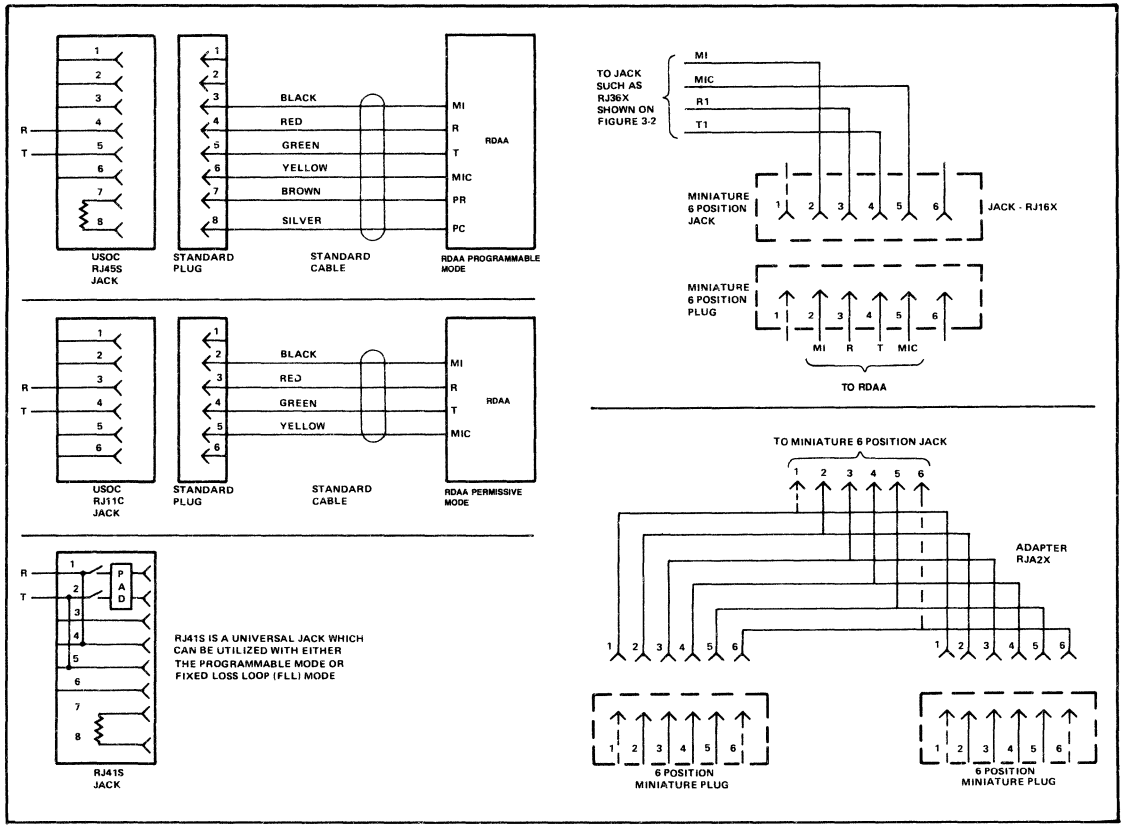


Figure 4. Standard Jacks, Plugs and Cable Color Codes

The ringer of the telephone set may be disconnected by the telephone company to prevent the bell from ringing.

The telephone company provides an exclusion key telephone under the Universal Service Order Code (USOC) RTC. This telephone set has the following customer options:

A. A1 - Telephone set controls line
B. A2 - Data set controls line
C. B3 - Aural monitoring not provided
D. B4 - Aural monitoring provided (See Note 1)
E. C5 - Touch tone dial
F. C6 - Rotary dial
G. D7 - Switch hook indication
H. D8 - Voice mode indication only (See Note 2)

NOTES

1. The aural monitoring feature allows the telephone handset to be used for listening to line signals without interfering with data transmission.
2. In this option the make contact of the exclusion key and a make contact on the switchhook are connected in series and to the mode indication leads MI and MIC of the data jack. Therefore, the SH signal of the RDAA goes ON only when the exclusion key is lifted.

When ordering this telephone, specify the USOC number RTC and the following options:

A. A2 - Data set controls line
B. B3 - Aural monitoring not provided
   or
   B4 - Aural monitoring provided
C. C5 - Touch tone dial telephone (503C)
   or
   C6 - Rotary dial telephone (2503C)
D. D8 - Voice mode indication only

Another telephone set provided by the telephone company is the Model 502 with exclusion key. To order this telephone set, specify the following:

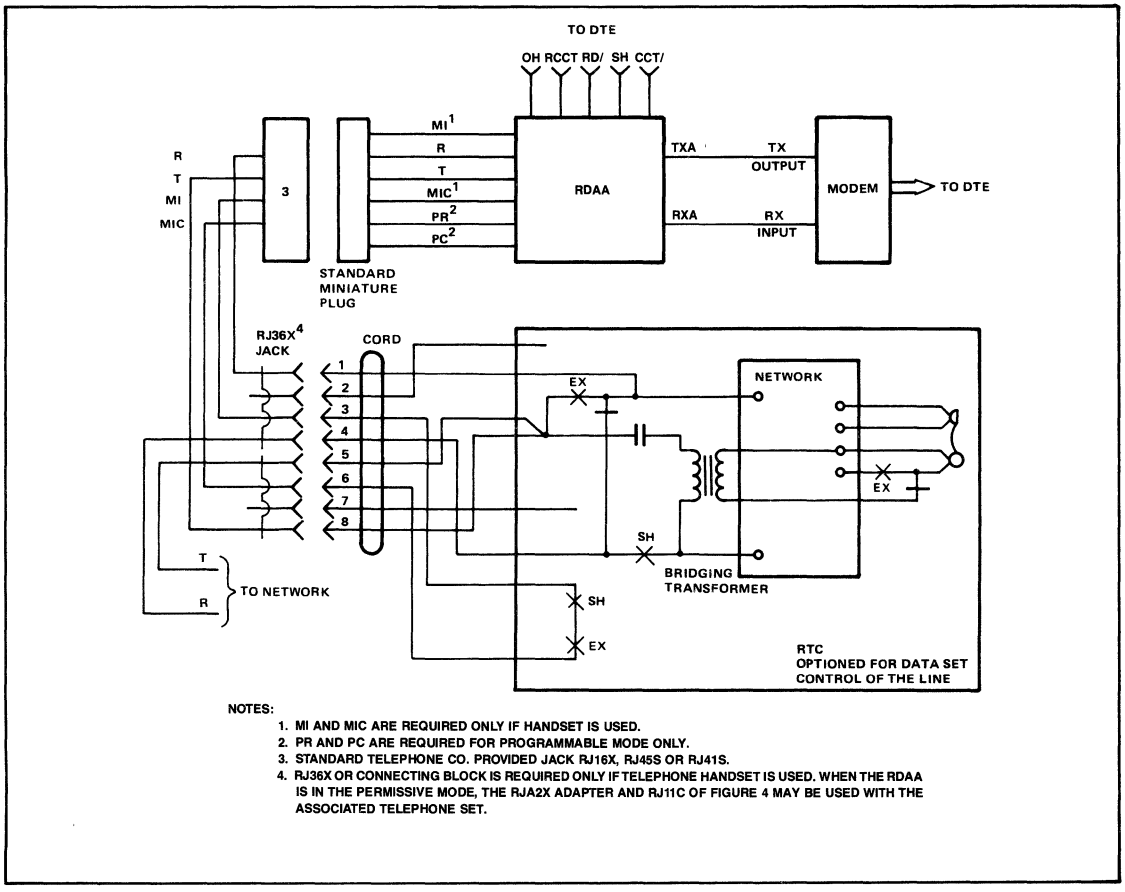
A. Modem 502 with exclusion key
B. Data set controls line

A summary of the information for ordering telephone and jacks is given in Table 3-1. Examples of typical installation are given in Figure 3-2.

Table 3-1. Telephones and Jacks Ordering Information

Output Configuration	Optional Telephone Set	FCC Reg. No.	Ringer Equivalent	Telephone Jack USOC No.	Telephone Set USOC No.
Programmable	With Telephone Set	AMQ9SQ 67943 DP-E	.8B	[1]RJ36X and [2,3]RJ45S	RTC or 502 with exclusion key
	Without Telephone Set	AMQ9SQ 67943 DP-E	.8B	[2,3]RJ45S	N.A.
Permissive	With Telephone Set	AMQ9SQ 67943 DP-E	.8B	[1]RJ36X and RJ16X or [4]RJA2X and RJ11C	RTC or 502 with exclusion key
	Without Telephone Set	AMQ9SQ 67943 DP-E	.8B	RJ11C	N.A.

Notes:
1. RJ36X is an 8 position miniature jack into which the telephone plugs. Rather than using an RJ36X jack, the telephone company may use a connecting block to connect the telephone set and data jack to the telephone line.
2. RJ41S is a universal data jack. It may be used for either Programmable or Fixed-Loss Loop mode The RJ45S jack is preferred, because it costs less
3. For multiple connections, the RJ45M jack should be ordered. The letter M indicates multiple single line jack for up to 8 lines. Specify the number of lines required when ordering.
4. RJA2X is the adapter shown in Figure 3-1. The use of the RJ36X and RJ16X jacks is recommended.



NOTES:

1. MI AND MIC ARE REQUIRED ONLY IF HANDSET IS USED.
2. PR AND PC ARE REQUIRED FOR PROGRAMMABLE MODE ONLY.
3. STANDARD TELEPHONE CO. PROVIDED JACK RJ16X, RJ45S OR RJ41S.
4. RJ36X OR CONNECTING BLOCK IS REQUIRED ONLY IF TELEPHONE HANDSET IS USED. WHEN THE RDAA IS IN THE PERMISSIVE MODE, THE RJA2X ADAPTER AND RJ11C OF FIGURE 4 MAY BE USED WITH THE ASSOCIATED TELEPHONE SET.

Figure 5. Transmit and Receive (Half Duplex) and (Full Duplex)

MODEM INTERFACE

There are 4 possible two-wire modes of operation configurations: receive-only, transmit-only, and receive and transmit (half duplex) and full-duplex (using two different frequencies simultaneously) as described below:

A. For the half-duplex and full-duplex configurations, the interface connection circuitry could be as shown in Figure 5.

B. For the receive-only configuration, the connection circuitry is the same as that shown in Figure 5, except that the RDAA input lead TXA is grounded rather than connected to the modem transmitter output.

C. For the transmit-only configuration, the RDAA lead RXA is left open rather than connected to the modem receiver as shown in Figure 5.

For a 4-wire full-duplex configuration, 2 RDAA modules and 2 telephone lines are required. The connection circuitry consists of one 2-wire receive-only connection, and one 2-wire transmit-only connection.

MODULE MOUNTING AND SECURING

The RDAA may be physically incorporated into the OEM's end product by using the four corner (0.156 inch diameter) mounting holes and self-locking plastic standoffs, or by bolting the RDAA module to a rigid structure. The RDAA module may also be mounted using card guides without card edge connector.

A number of manufacturers such as Richlock Corporation, Chicago, IL., produce plastic standoffs (Part Number CBS-3N).

ELECTRICAL INTERFACE

Electrical connection to the RDAA module is made through ribbon type connectors. The connector(s) interface pins (Figure 2) are contained on the component side of the board. There are two test points brought out to the interface connector of the board. Therefore care must be taken to prevent shorting test points with any of the other interface signals.

The RDAA telephone line interface connector pins are physically separated from the RDAA DTE interface connector pins, as shown in Figure 2 and described in Table 3-2.

Table 3-2. RDAA Telephone and Modem Interface

Type Interface Circuit	RDAA Connectors/ Pin No.	Interface Circuit/Signal
DTE Interface Connections	P2-1	CCT/
	P2-2	RXA
	P2-3	TXA
	P2-4	OH
	P2-5	RCCT
	P2-6	RD/
	P2-7	−12V
	P2-8	SH
	P2-9	GND
	P2-10	TP2 EXCESSIVE POWER DETECT
	P2-11	+12V
	P2-12	+5V
	P2-13	N/U
	P2-14	TP1 BILLING DELAY TIME
Telephone Line Interface Connections	P1-4	PC
	P1-3	PR
	P1-1	MIC
	P1-2	MI
	P1-(5-8) & (11-12)	(Not Used)
	P1-9, 10	R
	P1-13, 14	T

Care must be taken in routing the telephone interface pins to the telephone jack. The FCC (Rules, Part 68) requires that the telephone interface leads shall be separated from the leads or metallic paths connecting to power connections.

NOTE

Power connections are those connections between commercial power and any transformer, power supply rectifier, converter, or other circuitry associated with the RDAA. The connection of the interface pins (including the ±12V and +5V) shown in Figure 2 are not power connections.

The telephone interface leads shall not be routed in the same cable (or use the same connector) as leads or metallic paths connecting to commercial power.

FCC (Rules, Part 68) also requires that the telephone leads T and R be separated from metallic paths to leads connecting to non-registered equipment, when specification details provided to FCC do not show that the interface voltages are less than non-hazardous voltage source limits in Part 68. T and R shall not be routed in the same cable (or use adjacent pins on the same connector) as metallic paths to leads which are not considered non-hazardous. All DTE interface connector signals shown in Table 3-2 have been established as non-hazardous.

Therefore, in routing the telephone interface leads from the RDAA P1 connector to the telephone jack, the following precautions must be strictly adhered to. The telephone jack interface routing path should be as direct as possible. Any cable used in establishing this path should contain no signal leads other than possibly the (previously established as non-hazardous) DTE interface signals shown in Table 3-2. Any connector used in establishing this path should contain no commercial power source signal leads, and adjacent pins to the T and R (Tip and Ring) pins in any such connector should not be utilized by any signals other than possibly those shown in Table 3-2. Also the DTE interface routing path should be made as short as possible.

INSTALLATION PROCEDURE

A. Check the telephone line interface cable(s) plug(s) and jack(s) (Figure 4). If the USOC RJ41S jack is used for the Programmable mode, ensure that the jumper W2 is installed and W1 jumper is removed for the programmable mode of operation.

B. Make sure the telephone company installer has measured the loop loss correctly and has selected the proper programming resistor in the RJ45S or RJ41S jack.

NOTE

You have the right to know the method used by the installer for measuring loop loss and selecting the programming resistor.

C. Check the power supplies to see if they meet the proper requirements specified in paragraph 2.2.

D Insert the telephone cable plug into the jack, and make the DTE interface connection. Then switch on the power supplies.

OPERATIONAL CHECKOUT PROCEDURE

The following procedures check out the RDAA in association with a modem, a data terminal, a telephone set and an automatic dialer. The telephone set is required only in the manual origination mode (refer to paragraph 4.4) or if alternate voice communication is desired. The automatic dialer is required only in the automatic dial mode (refer to paragraph 4.3).

AUTOMATIC ANSWER MODE

A. Set the modem transmitted output level to +5 dBm.

B. Call the local modem from a remote station.

C. Follow the instructions given in Figure 6.

D. Transmit data from the local terminal to the remote terminal and monitor the CCT/ signal. It should stay low.

E. Terminate the call sequence and verify the received data.

AUTOMATIC ORIGINATE MODE

A. Set the modem transmitted output level to +5 dBm.

B. Follow the procedure of Figure 8 for touch tone origination or Figure 7 for pulse dial origination.

C. Transmit data from the local terminal and monitor the CCT/ signal. It should stay low.

D. Terminate the call sequence and verify the received data.

MANUAL OPERATION MODE

A. Set the modem transmitted output level to +5 dBm.

B. Follow the instructions given in paragraph 4.4.

C. Transmit data from the local terminal. CCT should stay low.

D. Terminate the call sequence and verify the received data.

SPECIAL INSTRUCTIONS TO USER

Your Rockwell Data Access Arrangement has been registered with the Federal Communications Commission (FCC). To comply with the FCC regulations you are requested to observe the following:

A. All direct connections to the telephone lines shall be made through standard plugs and jacks as specified in Figure 4 and Table 3-1.

B. It is prohibited to connect the RDAA to pay telephones or party lines.

C. You are required to notify the local telephone company of the connection or disconnection of the RDAA, the make, the modem number, the FCC registration number, the ringer equivalence number (refer to Table 3-1) and the particular line to which the connection is made. If the proper jacks are not available, you must order the type of jacks to be used from the telephone company. (Refer to Table 3-1 for the proper jacks and telephones.)

D. You should disconnect the RDAA from the telephone line if it appears to be malfunctioning. If the RDAA needs repair, return it to Rockwell International. This applies to equipment both in and out of warranty. Do not attempt to repair the unit as this will violate the FCC rules.

E. The RDAA contains protective circuitry to prevent harmful voltages being transmitted to the telephone network. If however, such harmful voltages do occur, then the telephone company has the right to temporarily discontinue your service. In this case, the telephone company shall:

1. Promptly notify you of the discontinuance.
2. Afford you the opportunity to correct the situation that caused the discontinuance.
3 Inform you of your right to bring a complaint to the FCC concerning the discontinuance.

F. The telephone company also has the right to make changes in their facilities and services which may affect the operation of your equipment. However, you shall be given notice in writing by the telephone company adequate to allow you to maintain uninterrupted service.

G. Labeling Requirements:

1. The FCC requires that the following label be prominently displayed on an outside surface of the OEM's end product:

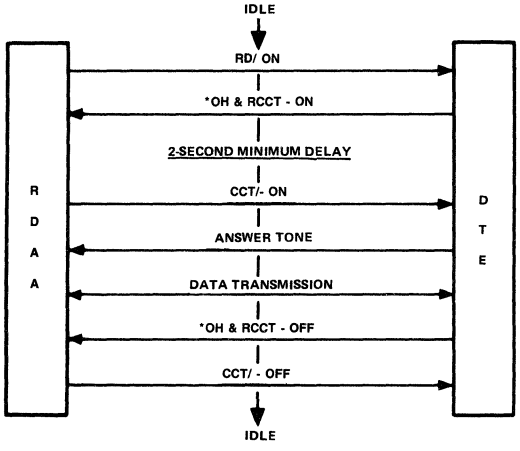
Unit contains Registered Protective Circuitry which complies with Part 68 FCC Rules FCC Registration Number: Ringer Equivalence: .8B

2. The size of the label should be such that all the required information is legible without magnification.

SECTION 4 — OPERATING INSTRUCTIONS

AUTOMATIC ANSWER

The connection of the data transmission path for automatic answer is as described in paragraph 2.4. To disconnect the data transmission path, just turn off OH and/or DA, as shown in Figure 6.



*DA MAY BE ON PERMANENTLY FOR AUTOMATIC ANSWER.

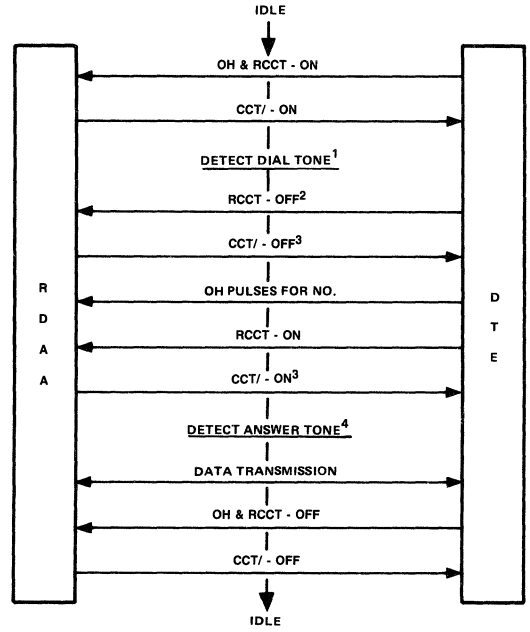
Figure 6. Automatic Answering Sequence

AUTOMATIC DIAL

DIAL PULSE ORIGINATION

The DTE must provide the logic to turn ON the OH and DA leads, detect dial tone (or time for 3 seconds to ensure dial tone present), then turn OFF the DA lead and generate the dial pulses corresponding to the called number (Figure 7). The 2-second delay period between OH and DA going ON and the response of CCT going ON will not be invoked in the origination mode. The DTE should monitor for call progress indication (dial tone, busy tone, answer tone, and call intercept).

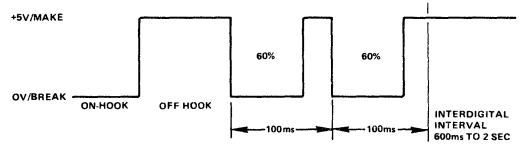
Requirements for proper call establishment exist on the pulse repetition rate (8 to 11 pulses per second), off duty cycle (60 percent nominal), interdigital delay timing (600 ms to 2 seconds) and chatter and spurious makes and breaks. The RDAA off-hook relay is a Reed relay designed to long life. Bell System requirements for pulse and touch-tone dialing are described in their Communications reference "Electrical Characteristics of Bell System Network Facilities at the Interface with Voiceband Ancillary and Data Equipment" (PUB 47001).



NOTES.
1. DIAL TONE DETECTION IS NOT PROVIDED WITHIN THE RDAA. ALTERNATIVELY, DTE MAY START FROM IDLE, TURN ON OH, THEN TIME FOR 3 SECONDS TO ENSURE DIAL TONE PRESENT AND PULSE OH FOR NUMBER.
2. DA MUST BE OFF DURING DIAL PULSING. DA MAY BE ON AT ALL OTHER TIMES.
3. THE DA TO CCT RESPONSE TIME IS LESS THAN 1 MS.
4. ANSWER TONE DETECTION CIRCUITRY IS NOT PROVIDED WITHIN THE RDAA.

Figure 7. Dial Pulse Origination Sequence

The following is an example for pulse dialing the digit #2 through the OH lead.

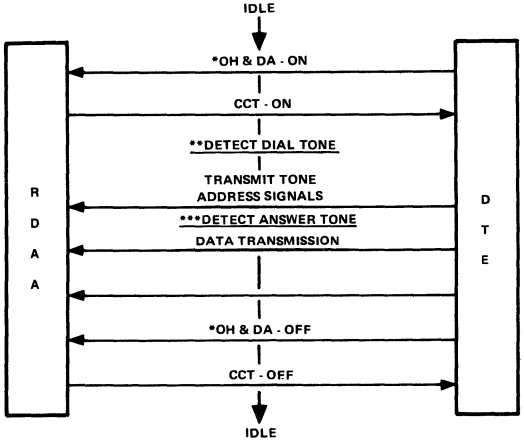


The OH lead can be pulsed directly via microprocessor port, or a commercially available "binary to dial pulse" LSI device such as the Rockwell CRC 8000, the General Instrument AY-5-9151 series, or the Motorola MC 14408. These devices can accept 4-bit binary digital inputs, buffer these digits, and output the OH dial pulses upon command. Also available from numerous semiconductor manufacturers (National, Mostek, General Instrument, Motorola, etc.) are LSI devices capable of interfacing directly to a key board and producing suitable dial pulses.

TOUCH-TONE ORIGINATION

The user's terminal must provide the logic to turn ON the OH and RCCT signals, detect the dial tone (or time for 3 seconds to ensure dial tone present) and transmit the tone-address signals via the TXA lead (Figure 8). The 2-second delay period between OH and RCCT going ON and CCT/ going ON is not invoked in the origination mode. The DTE should monitor for call progress indications (dial tone, busy tone, answer tone, and call intercept).

It should be noted that tone address signaling method is significantly more complicated in terms of hardware requirements than simple pulse dialing. The necessary tone pair generators must be added by the user. A number of semiconductor manufacturers produce monolithic LSI tone generators (AMI, Mostek, Motorola, National, General Instrument, Intersil, etc.). These tone pair generators are designed to interface with keyboards or digital ports and may require varying degrees of additional low pass filtering to reduce harmonic distortion. Touch-tone dialing is significantly faster than pulse dialing, but it may not be available in some locations.



*DA MAY BE PERMANENTLY ON

**ALTERNATIVELY, USER MAY TIME FOR 3 SECONDS TO ENSURE DIAL TONE PRESENT

***ANSWER TONE DETECTION CIRCUITRY IS NOT PROVIDED WITHIN THE RDAA

Figure 8. Touch-Tone Origination Sequence

Bell System requirements exist on minimum and maximum tone pair transmit power for proper call address signaling. When the RDAA is in the programmable mode, the gain of the RDAA transmit leg is set by a programming resistor in the telephone jack (over thirteen possible values). This makes establishment of the tone pair signal level to be input to the RDAA (at TXA) which meets the Bell System requirements difficult. It is therefore necessary to operate the RDAA in the Permissive mode for touch-tone origination. In this event the proper input power level (per frequency pair) to the RDAA (at TXA) would be +15 dBM (nominal). This level is well above the RDAA automatic limiter threshold. But the RDAA limiter activates (cuts off transmission path) only if threshold power level is continuously exceeded for about one second minimum, and quickly resets itself if the power level drops below threshold. If the tone pair duration time is restricted to significantly under one second (the minimum duration requirement is only 50 milliseconds) and the minimum interdigital time requirement (45 milliseconds) is observed, the limiter will not be activated. These requirements are easily met if the tone pair generation is under logic control. If the generation is controlled via keyboard input, the limiter will be activated if a key is depressed and held for more than a second, but will recover during the interval between key closures. However, the possibility exists that transients occurring at limiter activation and resetting may endanger proper call origination.

AUTOMATIC CALLING UNIT

Automatic dialing capability may also be added to a data transmission system simply by purchasing or leasing a separate box termed an "Automatic Calling Unit" (ACU). Such units are available from a variety of manufacturers. ACU's are available utilizing pulse or tone dialing. Connections of ACU to the data transmission system may be different for different ACUs. The standard protocol involved in interfacing between the user's data terminal equipment and an ACU is documented in CCITT Recommendation V.25 and also in EIA Standard RS-366. "Interface Between Data Terminal Equipment and Automatic Calling Equipment for Data Communication." It should be re-emphasized that a separate ACU is not necessarily required for automatic dial capability. The RDAA and some external hardware and/or software (as previously described) can suffice.

MANUAL ORIGINATION

For manual origination a telephone set with an exclusion key must be ordered from the local telephone company (refer to Table 3-1). After lifting both the handset and the exclusion key, a call may be originated or answered in the same manner as normal telephone service. When the handset and the exclusion key are lifted (MI is shorted to MIC), the signal SH is turned ON. If the user's data terminal is ready, it may respond with OH and RCCT. The RDAA will then turn ON the CCT/ signal. When answer tone is heard, the operator replaces the handset in its cradle. the SH signal will go Low and the data transmission path is connected. When data transmission is completed, the terminal turns OFF the OH signal and returns to the idle state.

SECTION 5 — FAULT ISOLATION

CUSTOMER REPAIR LIMITATIONS

Under the FCC Rules, no customer is authorized to repair an RDAA module. In the event of an RDAA malfunction, return the faulty RDAA to Rockwell International. It is recommended that the following fault isolation instructions provided in this section be performed prior to returning a suspected RDAA module. A periodic check of the DC power supplies is also recommended.

FAULT ISOLATION

The fault isolation flow chart (Figure 9) has been prepared specifically as an aid to the user for locating possible network and/or RDAA module malfunctions.

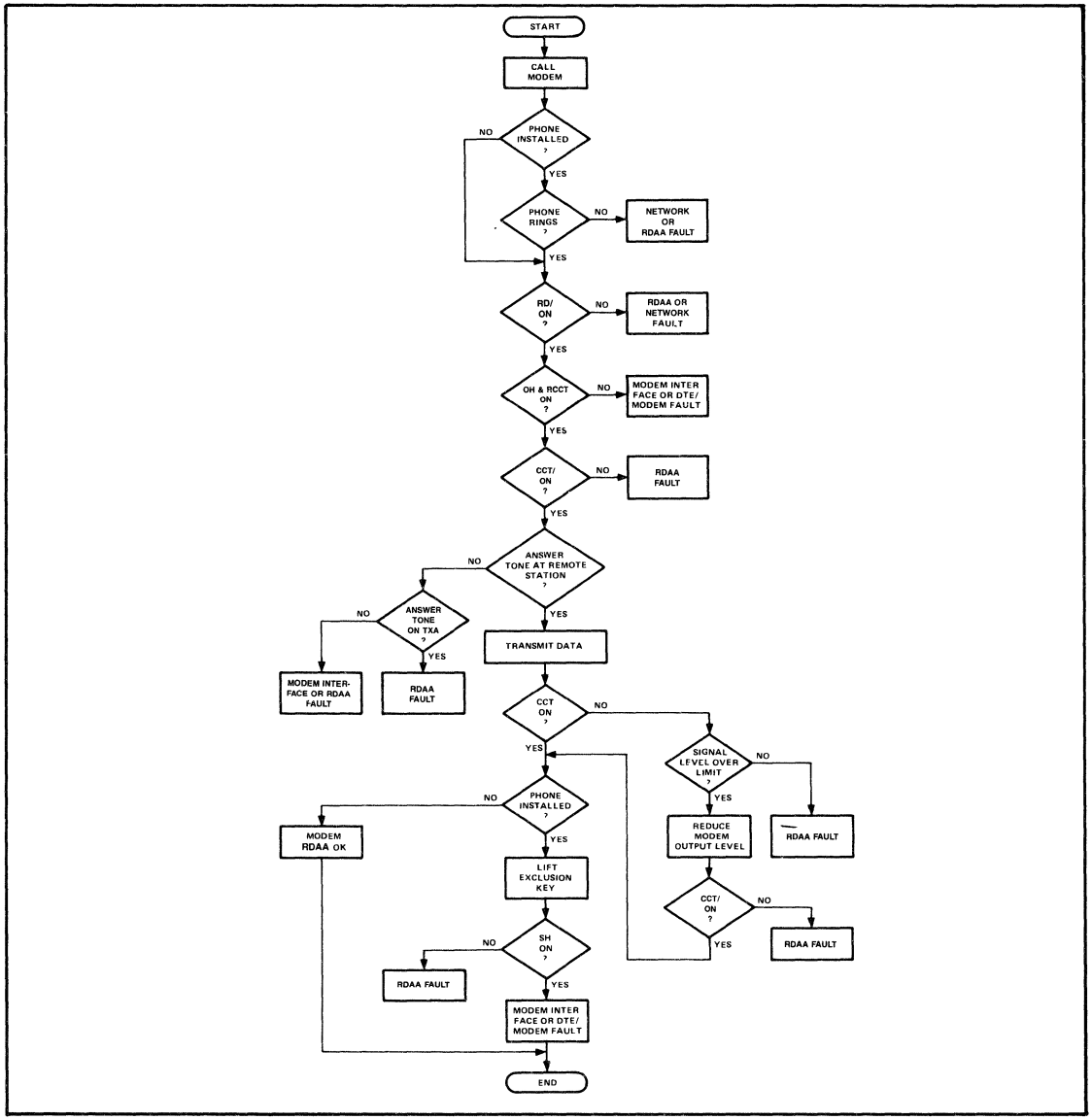


Figure 9. RDAA Fault Isolation Flow Chart

SECTION 2
4800, 9600, 14400 bps DATA MODEMS

2

4800, 9600, 14400 bps DATA MODEMS
Leading the Industry with High Performance and Quality

Rockwell's broad line of 4800, 9600 and 14400 bit-per-second (bps) modem products can easily be incorporated into standalone or system level products at a minimal cost while offering the end user high performance, quality and reliability. This line of modems uses the latest technology to provide customers with the smallest, most integrated designs available on the market.

Our high and ultra-high speed modems are designed to meet the Bell standard as well as the rigid CCITT recommendations. Whether operating at 4800 bps or 14400 bps, and transmitting data across the street or across the world, customers can be assured that Rockwell modems have been designed, built and tested to ensure operation over world-wide phone lines.

Rockwell offers these products in the Euro-size DIN connector modules. Additionally, a Euro-card module that utilizes surface mount technology (SMT) and dual in-line pins is available. This DIP module can be handled like any DIP type integrated circuit during board assembly and wave soldering. Its small size is ideal for integration into personal computers and work-stations as well as the traditional standalone or rack mount applications.

Model	Data Speed (bps)	PSTN/ Leased Line	2/4-Wire Half/Full-Duplex	Sync/Async	Compliance
R208/201	4800, 2400, 1200	P/L	2WHD, 4WFD	Sync	Bell 201B/C, 208A/B CCITT V.27 bis/ter, V.26, V26 bis
R48DP/208	4800, 2400	P/L	2WHD, 4WFD	Sync	Bell 208A/B CCITT V.27 bis/ter
R48DP	4800, 2400	P/L	2WHD, 4WFD	Sync	CCITT V.27 bis/ter
R96DP	9600, 7200, 4800, 2400	P/L	2WHD, 4WFD	Sync	CCITT V.29, V.27 bis/ter
R96FT	9600, 7200, 4800, 2400	P/L	2WHD, 4WFD	Sync	CCITT V.29, V.27 bis/ter, V.21 Channel 2, Proprietary Fast Train
R96FT/SC	9600, 7200, 4800, 2400, 75	P/L	2WHD, 4WFD	Sync	CCITT V.29, V.27 bis/ter, V.21 Channel 2, Proprietary Fast Train, Secondary Channel
R144DP	14400, 12000, 9600, 7200, 4800	P/L	2WHD, 4WFD	Sync	CCITT V.33, V.29
R9696DP	9600, 4800, 2400, 1200, 300	P/L	2WFD	Sync/Async	CCITT V.32, V.22 bis, V.22, V.21; Bell 212A, 103
R1496MM	14400, 12000, 9600, 4800, 2400, 1200, 300	P/L	2WFD, 4WFD	Sync/Async	CCITT V.33, V.32, V.29;

Rockwell

R208/201
Bell 208A/B and Bell 201C Modem

INTRODUCTION

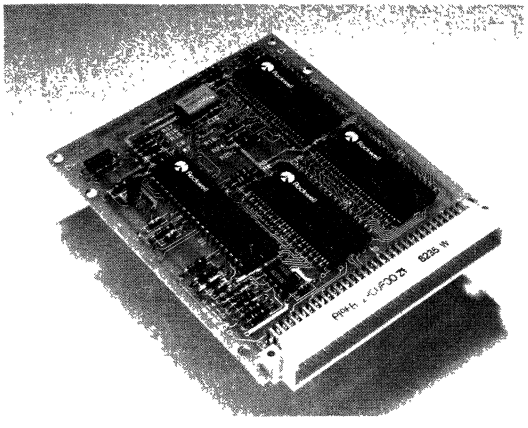
The Rockwell R208/201 is a synchronous 4800 and 2400 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) as well as leased lines through the appropriate line termination.

The modem satisfies the telecommunications requirements specified in Bell 208A/B, Bell 201C, CCITT V.27, and CCITT V.26. The R208/201 can operate at speeds of 4800 and 2400 bps. Employing advanced signal processing techniques, the R208/201 can transmit and receive data even under extremely poor line conditions.

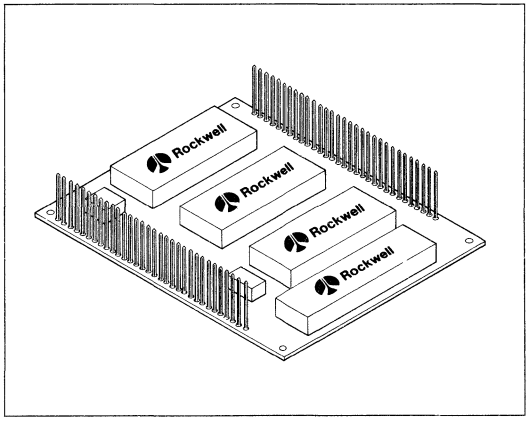
User programmable features allow the R208/201 to be tailored to support a wide variety of functional requirements. The modem's small size, low power consumption, and serial/parallel host interface simplify system design and allow installation in a compact enclosure. The modem module is available with a DIN connector for connection to a mating connector or with dual-in-line pins (DIP) for direct plug-in installation onto a host module.

FEATURES

- Compatible with
  - — Bell 208A/B, Bell 201C
  - — CCITT V.27 and V.26
- Automatic Configuration during Synchronizing Sequence
- 2-Wire Half-Duplex, 4-Wire Full-Duplex
- Programmable Tone Generation
- Programmable DTMF Tone Dialer
- Dynamic Range: – 43 dBm to 0 dBm
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C)(Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Diagnostic Capability
- Programmable Transmit Output Level
- Loopbacks
  - — Local and Remote Analog
  - — Remote Digital
- Small Size
  - — DIN Connector Version:
    100 mm × 120 mm (3.94 in. × 4.73 in.)
  - — DIP Connector Version:
    82 mm × 100 mm (3.23 in. × 3.94 in.)
- Power Consumption: 3 W (Typical)



R208/201 DIN Connector Version



R208/201 DIP Connector Version

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

The supported transmitter carrier frequencies are listed in Table 1.

Table 1. Transmitter Carrier Frequencies

Function	Frequency (Hz ±0.01%)
Bell 208A/B and Bell 201C	1800
CCITT V.27 and V.26	1800

TONE GENERATION

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. DTMF tone transmission capability is provided to allow the modem to operate as a programmable DTMF tone dialer.

SIGNALING AND DATA RATES

The supported signaling and data rates are listed in Table 2.

Table 2. Signaling/Data Rates

Specification	Baud Rate (Symbols/sec.)	Bits Per Baud	Data Rate (bps)(±0.01%)	Symbol Points
Bell 208A/B	1600	3	4800	8
CCITT V.27	1600	3	4800	8
Bell 201C	1200	2	2400	4
CCITT V.26	1200	2	2400	4
CCITT V.26	1200	1	1200	2

DATA ENCODING

The modem data encoding conforms to Bell 208A/B, Bell 201C, CCITT V.27, and CCITT V.26.

EQUALIZERS

The modem provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DdescRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with V.27 bis/ter.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The modem receiver circuit can adapt to received frequency error of up to ± 10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The modem receiver circuit satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

TRANSMIT LEVEL

The transmitter output level is accurate to ± 1.0 dB and is programmable from −1.0 dBm to −15.0 dBm in 2 dB steps.

TRAIN ON DATA

When train on data is enabled, the receiver typically trains on data in less than 3.5 seconds.

TURN-ON SEQUENCE

Selectable turn-on sequences can be generated as defined in Table 3.

Table 3. Turn-On Sequences

Specification	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled*
Bell 208A/B Long	150	355
Bell 208A/B Short	50	255
Bell 201C 26.4 ms Sync. Seq.	26.4	231.4
Bell 201C 148.3 ms Sync. Seq.	148.3	353.3
Bell 201C 220 ms Sync. Seq.	220	425
V.27 4800 Long	708	913
V.27 4800 Short	50	255
V.27 2400 Long	943	1148
V.27 2400 Short	67	272
V.26A 2400 90 ms Sync. Seq.	90	295
V.26 1200 90 ms Sync. Seq.	90	295

* For short echo protector tone, subtract 155 ms from $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ turn-on time.

TURN-OFF SEQUENCE

For Bell 208A/B and CCITT V.27, the turn-off sequence consists of approximately 7 ms and 10 ms, respectively, of remaining data and scrambled ones. For Bell 201C and CCITT V.26, the turn-off sequence consists of approximately 6 ms of remaining data and scrambled ones.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, diagnostic signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The six groups of hardware circuits are described in the following paragraphs. Table 5 lists the digital interface characteristics.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{\text{POR}}$) causes the modem to assume a valid operational state. The modem drives pin 13C to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 13C, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 13C low for at least 3 μs. When an external low input is applied to pin 13C, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 13C is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The modem POR sequence leaves the modem configured as follows:

- Bell 208 Short
- Serial channel data
- T/2 equalizer
- Standard echo protector tone
- −43 dBm threshold
- Cable and link equalizers disabled
- Train-On-Data disabled

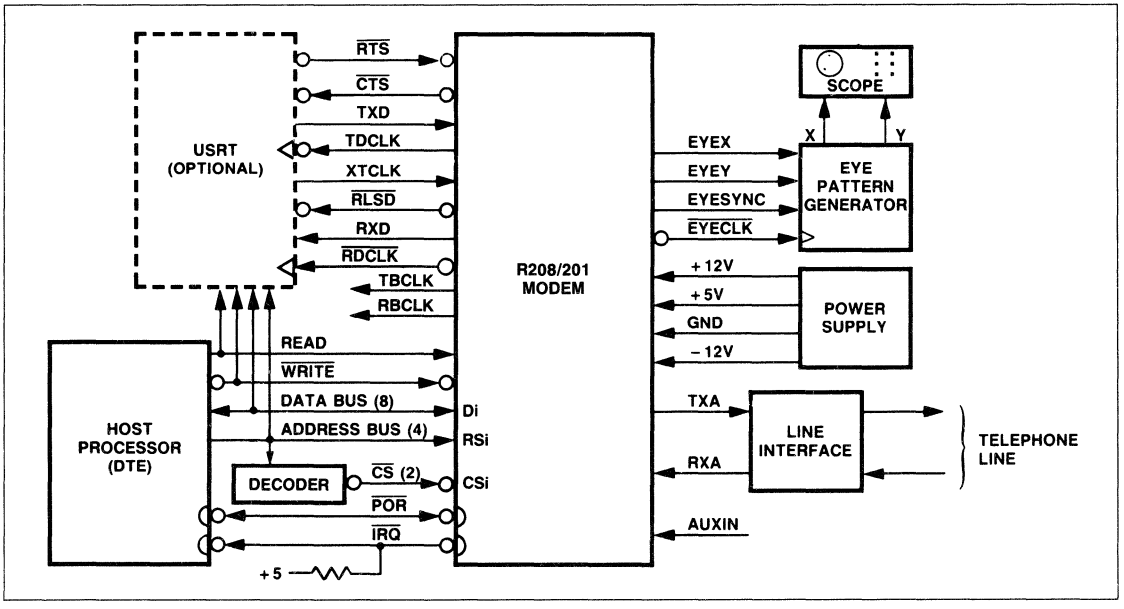


Figure 1. R208/201 Functional Interconnect Diagram

Table 4. R208/201 Hardware Circuits

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Description
A. OVERHEAD:				
Ground (A)	AGND	31C,32C	30,31	Analog Ground Return
Ground (D)	DGND	3C,8C, 5A,10A	29,37,53	Digital Ground Return
+5 volts	PWR	19C,23C, 26C,30C	1,45,61	+5 volt supply
+12 volts	PWR	15A	32	+12 volt supply
−12 volts	PWR	12A	36	−12 volt supply
$\overline{POR}$	I/OB	13C	2	Power-on-reset
B. MICROPROCESSOR INTERFACE:				
D7	I/OA	1C	3	Data Bus (8 Bits)
D6	I/OA	1A	4	
D5	I/OA	2C	5	
D4	I/OA	2A	6	
D3	I/OA	3A	7	
D2	I/OA	4C	8	
D1	I/OA	4A	9	
D0	I/OA	5C	10	
RS3	IA	6C	16	Register Select (4 Bits)
RS2	IA	6A	17	
RS1	IA	7C	18	
RS0	IA	7A	19	
$\overline{CS0}$	IA	10C	20	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	21	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	13	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	12C	14	Read Enable
$\overline{WRITE}$	IA	11A	12	Write Enable
$\overline{IRQ}$	OB	11C	11	Interrupt Request

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Description
C. V.24 INTERFACE:				
$\overline{RDCLK}$	OC	21A	23	Receive Data Clock
TDCLK	OC	23A	46	Transmit Data Clock
XTCLK	IB	22A	51	External Transmit Clock
$\overline{RTS}$	IB	25A	50	Request-to-Send
$\overline{CTS}$	OC	25C	49	Clear-to-Send
TXD	IB	24C	48	Transmitter Data
$\overline{RXD}$	OC	22C	26	Receiver Data
$\overline{RLSD}$	OC	24A	27	Received Line Signal Detector
D. ANCILLARY CIRCUITS:				
RBCLK	OC	26A	22	Receiver Baud Clock
TBCLK	OC	27C	47	Transmitter Baud Clock
E. ANALOG SIGNALS:				
TXA	AA	31A	34	Transmitter Analog Output
RXA	AB	32A	33	Receiver Analog Input
AUXIN	AC	30A	—	Auxiliary Analog Input
F. DIAGNOSTIC:				
EYEX	OC	15C	56	Eye Pattern Data—X Axis
EYEY	OC	14A	55	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	57	Eye Pattern Clock
EYESYNC	OA	13A	58	Eye Pattern Synchronizing Signal

Notes:
1. Refer to Table 5 for digital circuit interface characteristics and Table 7 for analog circuit interface characteristics.
2. Pins not used on the DIP Version: 15, 24, 25, 28, 35, 38, 39, 40, 41, 42, 43, 44, 52, 54, 59, 60

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes
1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I Load = 0.36 mA

This configuration is suitable for performing high speed data transfer using the serial data port. Individual features are discussed in subsequent paragraphs.

V.24 INTERFACE

Eight hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, +5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within standalone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The responses to $\overline{RTS}$ are shown in Table 6.

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON condition of $\overline{RTS}$ are shown in Table 6.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in data state is a maximum of 2 band times for all configurations.

Table 6. $\overline{RTS}$-$\overline{CTS}$ Response Times

Specification	$\overline{RTS}$-$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled*
Bell 208A/B Long	150	355
Bell 208A/B Short	50	255
Bell 201C 26.4 ms Sync Seq	26.4	231.4
Bell 201C 148.3 ms Sync Seq	148.3	353.3
Bell 201C 220 ms Sync. Seq.	220	425
V.27 4800 Long	708	913
V.27 4800 Short	50	255
V.27 2400 Long	943	1148
V.27 2400 Short	67	272
V.26A 2400 90 ms Sync. Seq.	90	295
V.26 1200 90 ms Sync. Seq	90	295

* For short echo protector tone, subtract 155 ms from $\overline{RTS}$-$\overline{CTS}$ turn-on time.

Received Line Signal Detector ($\overline{RLSD}$)

For Bell 208A/B and CCITT V.27, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ±10 ms. For Bell 201C, RLSD turns on in 10 ±5 ms after the detection of energy above threshold. The RLSD on-to-off response time for Bell 208A/B, CCITT V.27 and Bell 201C is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on the threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:

1. Greater than −43 dBm (RLSD on)
   Less than −49 dBm (RLSD off)
2. Greater than −33 dBm (RLSD on)
   Less than −38 dBm (RLSD off)
3. Greater than −26 dBm (RLSD on)
   Less than −31 dBm (RLSD off)
4. Greater than −16 dBm (RLSD on)
   Less than −21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency*. Selected data rate of 4800 or 2400 Hz (±0.01%).
2. *Duty Cycle*. 50 ±1%.

TDCLK is provided to the user in synchronous communications for USRT timing. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{RDCLK}$)

The modem provides a Receive Data Clock ($\overline{RDCLK}$) output in the form of a 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. $\overline{RDCLK}$ is provided to the user in synchronous communications for USRT timing. The timing recovery circuit is capable of tracking a ±.01% frequency error in the associated transmit timing source.

MICROPROCESSOR INTERFACE

Eight hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{CS0}$-$\overline{CS2}$) and Register Selects (RS0-RS3)

The signal processor to be accessed is selected by grounding one of three unique chip select lines, $\overline{CS2}$, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable (READ) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ line high or the $\overline{WRITE}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

ANALOG SIGNALS

The analog signal characteristics are described in Table 7.

Table 7. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is 604 ohms ±1%.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is the TLVL setting +0.6 dB −1.4 dB.

Transmitter Analog (TXA)

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the public switched telephone network. The output structure of TXA is a low impedance amplifier in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

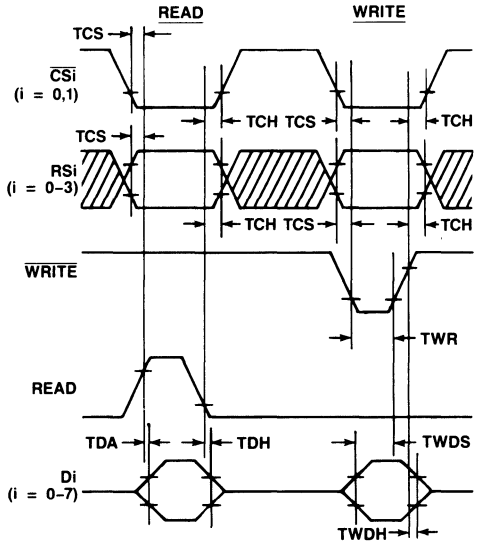
Receiver Analog (RXA)

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source. A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may take the form of back-to-back zener diodes across the transformer or a varistor across the transformer.

Auxiliary Input (AUXIN)

AUXIN provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit at a rate of 9600 samples-per-second. Any signal above 4800 Hz on the AUXIN line will be aliased back into the passband as noise. The input impedance of AUXIN is 1K ohm. The gain from AUXIN to TXA is the same as the selected transmit level +0.6 dB −1.4 dB. AUXIN must be grounded if not used.



Characteristic	Symbol	Min	Max	Units
$\overline{CS}_i$, RS_i setup time prior to Read or $\overline{Write}$	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
$\overline{CS}_i$, RS_i hold time after Read or $\overline{Write}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram

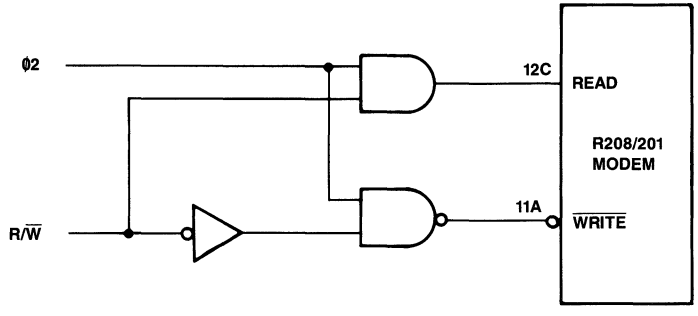


Figure 3. R/W to READ WRITE Conversion Logic

DIAGNOSTIC SIGNALS
EYEX, EYEY, $\overline{\text{EYECLK}}$, and EYESYNC

Four card edge connections provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances as well as defects in the modulation/demodulation process.

The outputs EYEX and EYEY provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. Since this data is in serial digital form it must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two D/A converters. A clock for use by the serial-to-parallel converters is furnished by signal $\overline{\text{EYECLK}}$. A strobe for loading the D/A converters is furnished by signal EYESYNC. Timing of these signals is illustrated in Figure 4. The EYEX and EYEY outputs furnish 9-bit serial words. Since most serial to parallel conversion logic is designed for 8-bit words, an extra storage flip-flop is required for 9-bit resolution. However, the ninth bit is not generally needed for eyepattern generation, and eight-bit hardware can be used if data is copied on the rising edge of $\overline{\text{EYECLK}}$ rather than the falling edge.

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Two clock signals called TBCLK and RBCLK are provided at the modem connector. These signals have no counterpart in the V.24 or RS-232 recommendations since they mark the baud interval for the transmitter and receiver rather than the data rate. The baud clocks can be useful in identifying the order of data bits in a baud (e.g., for multiplexing data, etc.). Both signals are high active, meaning the baud boundaries occur on falling edges. The first bit in each baud begins with the falling edge of the corresponding baud clock.

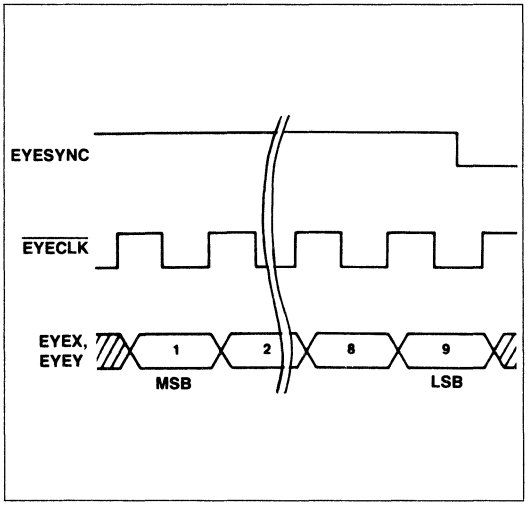


Figure 4. Eye Pattern Timing

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on three special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into areas. These areas are partitioned into transmitter, baud rate, and sample rate devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 48 addressable registers in the modem are shown in Figure 5. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Table 8 defines the individual bits in the interface memory. In the Table 8 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS T							
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	—	—	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	RAM DATA YTM							
0	RAM DATA YTL, TRANSMITTER DATA, DDR							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	SQH	—	—	—	—	—	—	—
E	RSIA	—	—	—	RSB	RSIE	—	RSDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	USMD	$\overline{TONE}$	—	—
8	—	—	—	—	—	$\overline{P2DET}$	—	—
7	RTH		DDIS	RPDM	SWRT	BWRT	T2	RTDIS
6	IFIX	TOD	RECEIVER CONFIGURATION					
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL, RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 5. Interface Memory Map

Table 8. R208/201 Interface Memory Definitions

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>A3L</td><td>Amplitude 3-Link Select</td><td>0:5:1</td><td>A3L is used in conjunction with LAEN. When A3L is a one the Japanese 3 link equalizer is selected and when A3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
<tr><td>BWRT</td><td>Baud Write</td><td>1:7:2</td><td>When control bit BWRT is a one, the RAM write operation is enabled for Chip 2.</td></tr>
<tr><td>CEQ</td><td>Cable Equalizer Field</td><td>0:5:(4.5)</td><td>The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following tables list the possible cable equalizer selection codes and responses.

CEQ — Cable Length (0.4 mm diameter)
0 — 0.0
1 — 1.8 km
2 — 3.6 km
3 — 7.2 km

Cable Equalizer Nominal Gain

CEQ CODE 1
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr><tr><th>Transmitter</th><th>Receiver</th></tr><tr><td>700</td><td>−0.99</td><td>−0.94</td></tr><tr><td>1500</td><td>−0.20</td><td>−0.24</td></tr><tr><td>2000</td><td>+0.15</td><td>+0.31</td></tr><tr><td>3000</td><td>+1.43</td><td>+1.49</td></tr></table>
CEQ CODE 2
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr><tr><th>Transmitter</th><th>Receiver</th></tr><tr><td>700</td><td>−2.39</td><td>−2.67</td></tr><tr><td>1500</td><td>−0.65</td><td>−0.74</td></tr><tr><td>2000</td><td>+0.87</td><td>+1.02</td></tr><tr><td>3000</td><td>+3.06</td><td>+3.17</td></tr></table>
CEQ CODE 3
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr><tr><th>Transmitter</th><th>Receiver</th></tr><tr><td>700</td><td>−3.93</td><td>−3.98</td></tr><tr><td>1500</td><td>−1.22</td><td>−1.20</td></tr><tr><td>2000</td><td>+1.90</td><td>+1.81</td></tr><tr><td>3000</td><td>+4.58</td><td>+4.38</td></tr></table>
Unless a problem with training or high bit error rate is encountered, most applications operate successfully with no cable equalizer selected.</td></tr>
<tr><td>$\overline{\text{CDET}}$</td><td>Carrier Detector</td><td>1:B:0</td><td>When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$. If the $\overline{\text{FED}}$ bit goes to a zero and no P2 sequence is detected, the $\overline{\text{CDET}}$ bit goes to zero within 5 to 25 ms indicating that the receiver has entered the data state without a training sequence.</td></tr>
<tr><td>DDIS</td><td>Descramble Disable</td><td>1:7:5</td><td>When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.</td></tr>
<tr><td>DDR</td><td>Dial Digit Register</td><td>0:0:0–7</td><td>DDR is used to tell the modem which DTMF digit to transmit (see Transmitter Data).</td></tr>
<tr><td>D3L</td><td>Delay 3-Link Select</td><td>0:5:0</td><td>D3L is used in conjunction with LDEN. When D3L is a one the Japanese 3 link equalizer is selected and when D3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
</table>

Table 8. R208/201 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
EPT	Echo Protector Tone	0·7 3	When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission.
$\overline{\text{FED}}$	Fast Energy Detector	1 9 6	When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband, and the receiver is searching for the training sequence.
(None)	FREQL/FREQM	0·2:0–7, 0·3 0–7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below: *FREQM Register (0:3)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01% Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below: FREQM / FREQL / Frequency (Hz) 0C / 52 / 462 1D / 55 / 1100 2C / 00 / 1650 31 / 55 / 1850 38 / 00 / 2100
IFIX	Eye Fix	1:6:7	When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB.
LAEN	Link Amplitude Equalizer Enable	0:5:3	The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table: LAEN / A3L / Curve Matched 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link The link amplitude equalizer responses are given in the following table. **Link Amplitude Equalizer** Frequency (Hz) / Gain Relative to 1700 Hz (dB): U.S. Survey Long / Japanese 3-Link 1000 / −0.27 / −0.13 1400 / −0.16 / −0 08 2000 / +0.33 / +0 16 2400 / +1.54 / +0.73 2800 / +5.98 / +2.61 3000 / +8.65 / +3.43

Table 8. R208/201 Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>LCEN</td><td>Loop Clock Enable</td><td>0:4:0</td><td>When control bit LCEN is a one, the transmitter clock tracks the receiver clock</td></tr>
<tr><td>LDEN</td><td>Link Delay Equalizer Enable</td><td>0:5:2</td><td>The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table:

LDEN D3L Curve Matched
0 X No Equalizer
1 0 U.S. Survey Long
1 1 Japanese 3-Link

The link delay equalizer responses are given in the following table.

Link Delay Equalizer
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Delay Relative to 1700 Hz (Microseconds)</th></tr><tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr><tr><td>800</td><td>-498.1</td><td>-653.1</td></tr><tr><td>1200</td><td>-188.3</td><td>-398.5</td></tr><tr><td>1600</td><td>-15.1</td><td>-30.0</td></tr><tr><td>1700</td><td>+0.0</td><td>+0.0</td></tr><tr><td>2000</td><td>-39.8</td><td>+11.7</td></tr><tr><td>2400</td><td>-423.1</td><td>-117.1</td></tr><tr><td>2800</td><td>-672.4</td><td>-546.3</td></tr></table></td></tr>
<tr><td>L2ACT</td><td>Remote Digital Loopback Activate</td><td>0:4:1</td><td>When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2.</td></tr>
<tr><td>L3ACT</td><td>Local Analog Loopback Activate</td><td>0:4:7</td><td>When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.</td></tr>
<tr><td>L4ACT</td><td>Remote Analog Loopback Activate</td><td>0:4:6</td><td>When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4.</td></tr>
<tr><td>L4HG</td><td>Loop 4 High Gain</td><td>0:4:5</td><td>When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.</td></tr>
<tr><td>MHLD</td><td>Mark Hold</td><td>0:7:4</td><td>When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).</td></tr>
<tr><td>$\overline{\text{PNDET}}$</td><td>Period N Detector</td><td>1:B:6</td><td>When status bit $\overline{\text{PNDET}}$ is a zero, it indicates a PN sequence has been detected. This bit sets to a one at the end of the PN sequence.</td></tr>
<tr><td>$\overline{\text{P2DET}}$</td><td>Period Two Detector</td><td>1:8:2</td><td>When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a P2 sequence has been detected. This bit sets to a one at the start of the PN sequence.</td></tr>
<tr><td>(None)</td><td>RAM Access T</td><td>0:F:0–7</td><td>Contains the RAM access code used in reading or writing chip 0 RAM locations via word Y (0:1 and 0:0).</td></tr>
<tr><td>(None)</td><td>RAM Access XB</td><td>2:5:0–7</td><td>Contains the RAM access code used in reading or writing chip 2 RAM locations via word X (2:3 and 2:2).</td></tr>
<tr><td>(None)</td><td>RAM Access XS</td><td>1:5:0–7</td><td>Contains the RAM access code used in reading or writing chip 1 RAM locations via word X (1:3 and 1:2).</td></tr>
<tr><td>(None)</td><td>RAM Access YB</td><td>2:4:0–7</td><td>Contains the RAM access code used in reading or writing chip 2 RAM locations via word Y (2:1 and 2:0).</td></tr>
</table>

Table 8. R208/201 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Access YS	1 4 0–7	Contains the RAM access code used in reading or writing chip 1 RAM locations via word Y (1 1 and 1·0)
(None)	RAM Data XBL	2 2·0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 2
(None)	RAM Data XBM	2 3 0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 2
(None)	RAM Data XSL	1·2 0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 1
(None)	RAM Data XSM	1:3.0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 1
(None)	RAM Data YBL	2 0 0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2
(None)	RAM Data YBM	2:1.0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YSL	1.0.0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus. See 'Receiver Data '
(None)	RAM Data YSM	1·1.0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1.
(None)	RAM Data YTL	0:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 0. It is shared by parallel data mode and DTMF dialing (see Transmitter Data)
(None)	RAM Data YTM	0:1:0–7	Most significant byte of 16-byte word Y used in reading or writing locations in chip 0
RBDA	Receiver Baud Data Available	2·E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2·0.
RBIA	Receiver Baud Interrupt Active	2·E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low In idle mode the interrupts from chip 2 occur at half the baud rate. During diagnostic access in data mode, the interrupts occur at the baud rate.
RBIE	Receiver Baud Interrupt Enable	2:E.2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
(None)	Receiver Configuration	1·6.0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB). *Receiver Configuration Control Codes* Control codes for the modem receiver configuration are: **Configuration Code (Hex) — Receiver Configuration** 18 — Bell 208/201 Auto. Configuration* 16 — Bell 208A/B HDX 12 — Bell 208A/B FDX 34 — Bell 201C HDX 26.4 ms Sync. Seq. 30 — Bell 201C FDX 26.4 ms Sync. Seq 35 — Bell 201C HDX 148.3 ms Sync. Seq. 31 — Bell 201C FDX 148 3 ms Sync Seq 14 — Bell 201C HDX 220 ms Sync Seq. 10 — Bell 201C FDX 220 ms Sync. Seq 26 — V 27 4800 HDX Long 22 — V.27 4800 FDX Long 25 — V.27 2400 HDX Long 21 — V.27 2400 FDX Long 06 — V.27 4800 HDX Short 02 — V.27 4800 FDX Short 05 — V.27 2400 HDX Short 01 — V.27 2400 FDX Short 15 — V.26A 2400 FDX 90 ms Sync. Seq. 11 — V 26 1200 FDX 90 ms Sync Seq 08 — Tone Detector *When this configuration is selected, the receiver will detect a Bell 208 or 201C handshake and configure itself accordingly.

Table 8. R208/201 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	Receiver Data	1:0:0–7	The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data. When using receiver parallel data mode, the registers 1:3 through 1·0 can not be used for reading the chip 1 RAM.
RPDM	Receiver Parallel Data Mode	1·7:4	When control bit RPDM is a one, the receiver supplies channel data to the receiver data register (1:0) as well as to the hardware serial data output. (See Receiver Data)
RSB	Receiver Setup Bit	1:E:3	When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective. Worst case setup time is 2 baud times.
RSDA	Receiver Sample Data Available	1:E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0. RSDA goes to a zero when the host processor reads data from register 1:0.
RSIA	Receiver Sample Interrupt Active	1:E:7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is a one.
RTDIS	Receiver Training Disable	1:7:0	When control bit RTDIS is a one, the receiver is prevented from recognizing a training sequence and entering the training state.
RTH	Receiver Threshold Field	1:7:6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH** / **RLSD On** / **RLSD Off** 0 / > –43 dBm / < –48 dBm 1 / > –33 dBm / < –38 dBm 2 / > –26 dBm / < –31 dBm 3 / > –16 dBm / < –21 dBm
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are ORed by the modem.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector tone is 30 ms long rather than 185 ms
SQH	Receiver Squelch	1:F:7	When control bit SQH is set to a one, the receiver is squelched, $\overline{RLSD}$ is turned off and RXD is clamped to all marks. SQH only affects the receiver operation when a half duplex receiver configuration has been selected.
SWRT	Sample Write	1:7:3	When control bit SWRT is a one, the RAM write operation is enabled for chip 1.
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one. During a RAM access in chip 0, when TBA is a one the host can perform either a RAM read or write depending on the state of bit 0:6:3 (see Transmitter Configuration).
TIA	Transmitter Interrupt Active	0:E·7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero
TIE	Transmitter Interrupt Enable	0:E·2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.

Table 8. R208/201 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TLVL	Transmitter Level Field	0 4 2–4	The transmitter analog output level is determined by eight TLVL codes, as follows TLVL / Transmitter Analog Output* / TLVL / Transmitter Analog Output* 0 / −1 dBm ±1 dB / 4 / −9 dBm ±1 dB 1 / −3 dBm ±1 dB / 5 / −11 dBm ±1 dB 2 / −5 dBm ±1 dB / 6 / −13 dBm ±1 dB 3 / −7 dBm ±1 dB / 7 / −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB
TOD	Train-on-Data	1·6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state A BER of approximately 10^{-3} for 0 5 seconds initiates train-on-date.
$\overline{\text{TONE}}$	Tone Detect	1·9·2	$\overline{\text{TONE}}$ indicates with a zero the presence of energy in the 345–650 ± 10 Hz frequency range. For call progress purposes, the user may determine which tone is present by determining the duty cycle of the $\overline{\text{TONE}}$ bit.
TPDM	Transmitter Parallel Data Mode	0·7·2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0). When TPDM is a zero channel data from the serial hardware input TXD is accepted and the chip 0 RAM access is enabled.
(None)	Transmitter Configuration*	0·6:0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB) *Transmitter Configuration Control Codes* Control codes for the modem transmitter configurations are: **Configuration Code (Hex)*** / **Configuration** 32 / Bell 208A/B Long 12 / Bell 208A/B Short 30 / Bell 201C 26.4 ms Sync Seq. 31 / Bell 201C 148.3 ms Sync Seq. 10 / Bell 201C 220 ms Sync. Seq 22 / V.27 4800 Long 02 / V.27 4800 Short 21 / V.27 2400 Long 01 / V.27 2400 Short 15 / V.26 2400 90 ms Sync Seq 11 / V.26 1200 90 ms Sync. Seq. 80 / Tone Transmit 08 / DTMF Tone Transmit ***Note:** Bit 3 of the transmitter configuration register is used in the RAM access operation for chip 0 When 0:6.3 is a one, a RAM write operation will occur when TPDM is a zero, and when 0:6.3 is a zero, a RAM read operation will occur when TPDM is a zero **Configuration Definitions** Definitions of the eight Transmitter Configurations are: 1. *Bell 208.* When any of the Bell 208 configurations are selected, the modem operates as specified in the Bell 208A/B Standard. 2. *Bell 201C.* When any of Bell 201C configurations are selected, the modem operates as specified in the Bell 201C Standard. 3. *V.27.* When any of the V.27 configurations are selected, the modem operates as specified in CCITT Recommendation V.27 ter. 4 *V.26.* When any of the V.26 configurations are selected, the modem operates as specified in CCITT Recommendation V.26. 5 *Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by two registers in the host interface memory space containing the frequency code. The most significant bits are specified in the FREQM register (0·3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0 146486 Hz ±0 01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0 01%. 6. *DTMF Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a Dual Tone Multi-Frequency (DTMF) tone specified by the code loaded in the Dial Digit Register (DDR, 0·0). The twelve codes, their associated dial digits and tone pairs are as follows:

Table 8. R208/201 Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>Dial Digit Register (DDR) Hexadecimal Code</th><th>Dial Digit</th><th colspan="2">Tone Pair (Hz)</th></tr>
<tr><td>00</td><td>0</td><td>941</td><td>1336</td></tr>
<tr><td>01</td><td>1</td><td>697</td><td>1209</td></tr>
<tr><td>02</td><td>2</td><td>697</td><td>1336</td></tr>
<tr><td>03</td><td>3</td><td>697</td><td>1477</td></tr>
<tr><td>04</td><td>4</td><td>770</td><td>1209</td></tr>
<tr><td>05</td><td>5</td><td>770</td><td>1336</td></tr>
<tr><td>06</td><td>6</td><td>770</td><td>1477</td></tr>
<tr><td>07</td><td>7</td><td>852</td><td>1209</td></tr>
<tr><td>08</td><td>8</td><td>852</td><td>1336</td></tr>
<tr><td>09</td><td>9</td><td>852</td><td>1477</td></tr>
<tr><td>0A</td><td>★</td><td>941</td><td>1209</td></tr>
<tr><td>0B</td><td>#</td><td>941</td><td>1477</td></tr>
</table>
Figure 6 shows the utilization of the DTMF Tone Transmit configuration in an auto dialing application.
</td></tr>
<tr><td>(None)</td><td>Transmitter; DDR; RAM Data YTL</td><td>0:0:0–7</td><td>
1. The host processor transmits data in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

NOTE
Data is transmitted bit zero first.

<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Bell 208A/B V.27 4800</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>Bell 201C, V26, V.27 2400</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table>
2. Register 0:0 is used to transmit DTMF digits when the transmitter is configured in the DTMF tone transmit mode.

3. Register 0:0 is a RAM data register used for reading or writing the least significant byte of the 16-bit Y word in Chip 0 when TPDM is a zero and no tone or DTMF tone transmission is occurring.
</td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>T2</td><td>T/2 Equalizer Select</td><td>1:7:1</td><td>When control bit T2 is a one, an adaptive equalizer with two taps per baud is used When T2 is a zero, the equalizer has one tap per baud. The total number of taps remains the same for both cases.</td></tr>
<tr><td>USMD</td><td>Unscrambled Mark Detection</td><td>1:9:3</td><td>When status bit USMD is a one, unscrambled mark as defined by Bell 201C has been detected. The response time is 5 ms.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a zero, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A. The clock appearing at the XTCLK input will appear at the TDCLK output.</td></tr>
</table>

SIGNAL PROCESSOR RAM ACCESS

RAM and Data Organization

Each signal processor contains 128 words of random access memory (RAM). Each word is 32 bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16 bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. In the sample rate and baud rate devices the entire contents of XRAM and YRAM may be read from or written into by the host processor via the microprocessor interface. Access to the YRAM is possible only in the transmitter device.

Interface Memory

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit determines the RAM address to read from or write into by the code stored in the RAM ACCESS bits of interface memory registers. The SP logic unit normally transfers a word from RAM to interface memory once each cycle of the device code. Each RAM word transferred to the interface memory is 32 bits long (16 bits in the transmitter). These bits are written by the SP logic unit into interface memory registers 3, 2, 1, and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data, respectively. As previously described for parallel data mode, the data available bits set to a one when register 0 of the respective signal processor is written into by the device and resets to a zero when register 0 is read from by the host. Since the parallel data mode transmitter and receiver data register shares register 0 with the YRAM data, chip 0 and 1 RAM access are disabled in parallel data mode. However, chip 2 RAM access remains active in receiver parallel data mode.

The transmitter, sample rate device and the baud rate device allow data to be transferred from interface memory to RAM. When set to a one, bit SWRT (1:7:3) signals the chip 1 SP logic unit to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. Bit BWRT (1:7:2) performs the same function for chip 2 RAM. When writing into the RAM, 32 bits are transferred. The 16 bits written into XRAM come from registers 3 and 2, with register 3 being the more significant byte. The 16 bits written into YRAM come from registers 1 and 0, with register 1 being the more significant byte. When only 16 bits of data are to be written, FF (a dummy RAM location) must be stored in RAM ACCESS XS or RAM ACCESS YS to prevent writing the insignificant 16 bits of registers 1:3 through 1:0 into a valid RAM location. When the host processor writes into register 1:0 the RSDA bit (1:E:0) is reset to zero. When the SP logic unit reads data from register 1:0, the RSDA bit (1:E:0) is set to a one. In a similar manner, bit RBDA (2:E:0) resets to zero when the host processor writes into register 2:0 and sets to a one when the SP logic unit reads data from register 2:0.

When reading from RAM, or writing into RAM, the bits in registers 0:E, 1:E, 2:E can be used for handshaking or interrupt functions as in parallel data mode. When not in parallel data mode, the bits in register 1:E perform the handshake and interrupt functions for RAM access. In both serial and parallel data modes, the bits in register 2:E perform handshake and interrupt functions for RAM access. When set to one, bit RBIE (2:E:2) enables RBDA to drive the IRQ connector signal to zero volts when RBDA is a one. Bit RBIA (2:E:7) identifies chip 2, the baud rate device, as a source of IRQ interrupt. Bit RBIA is a one when both RBIE and RBDA are set to one. In the event that other system elements may cause IRQ to be driven low, the host must determine if modem chip 2 is causing an interrupt by reading RBIA.

Table 9 provides the available RAM access functions, codes, and registers.

Auto Dial Sequence

The Figure 6 flowchart defines the auto dial sequence via the microprocessor interface memory. The modem timing for the auto dialer accounts for DTMF tone duration and interdigit delay. The default tone duration is 95 ms and the default interdigit delay is 71 ms. The default amplitudes for the high and low frequencies are – 4 dBm and – 6 dBm, respectively. The above four parameters can be changed by performing a RAM write.

Table 9. RAM Access Codes

No.	Function	Chip	X Access Code (Hex)	Y Access Code (Hex)	Register
1	DTMF Low Frequency Amplitude[1]	0	—	88	0,1
2	DTMF High Frequency Amplitude[1]	0	—	08	0,1
3	Interdigit Delay[1]	0	—	89	0,1
4	DTMF Tone Duration[1]	0	—	09	0,1
5	Received Signal Samples	1	C0	Not Used	2,3
6	Demodulator Output	1	C2	42	0,1,2,3
7	Low Pass Filter Output	1	D4	54	0,1,2,3
8	Average Energy	1	DC	Not Used	2,3
9	AGC Gain Word	1	81	Not Used	2,3
10	Equalizer Input	2	C0	40	0,1,2,3
11	Equalizer Tap Coefficients	2	81 – A0	01 – 20	0,1,2,3
12	Unrotated Equalizer Output	2	E1	61	0,1,2,3
13	Rotated Equalizer Output (Received Points)	2	A2	22	0,1,2,3
14	Decision Points Ideal Points	2	62	0,1,2,3	
15	Error	2	E3	63	0,1,2,3
16	Rotation Angle	2	Not Used	00	0,1
17	Frequency Correction	2	AA	Not Used	2,3
18	EQM	2	A7	Not Used	2,3
19	Dual Point	2	AE	2E	0,1,2,3

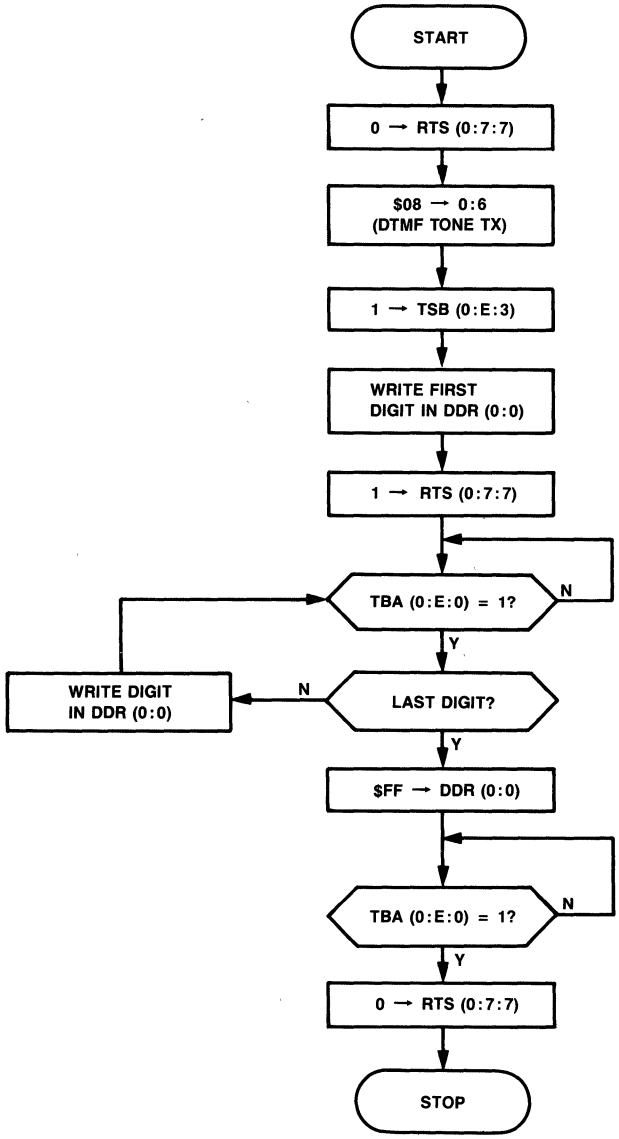


Figure 6. R208/201 Auto Dial Sequence

PERFORMANCE

TYPICAL BIT ERROR RATES

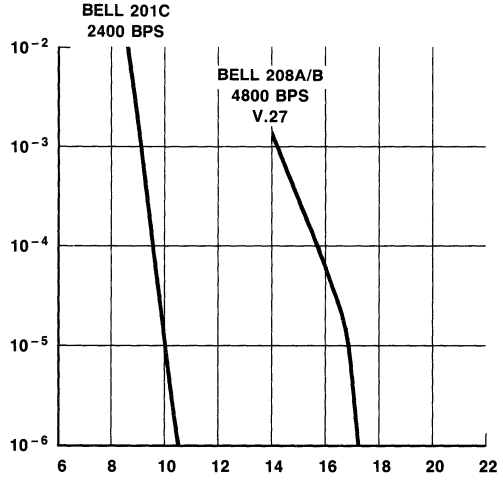
The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

Typical BER performance is shown in Figure 7. Figure 8 shows a typical test setup to measure BER.

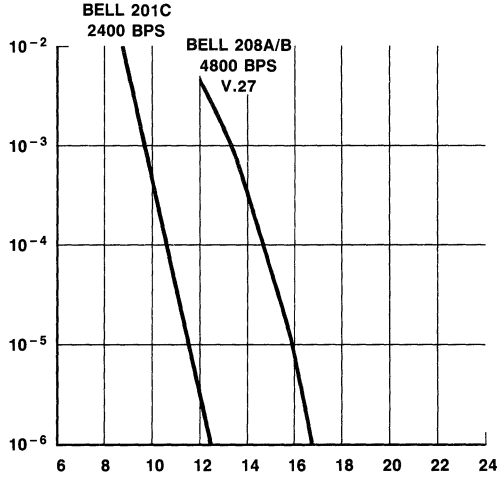
TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.



a) TYPICAL BIT ERROR RATE
(BACK TO BACK, T/2 EQUALIZER, −20 dBm)



b) TYPICAL BIT ERROR RATE
(UNCONDITIONED 3002 LINE, T/2 EQUALIZER, −20 dBm)

Figure 7. R208/201 BER versus SNR

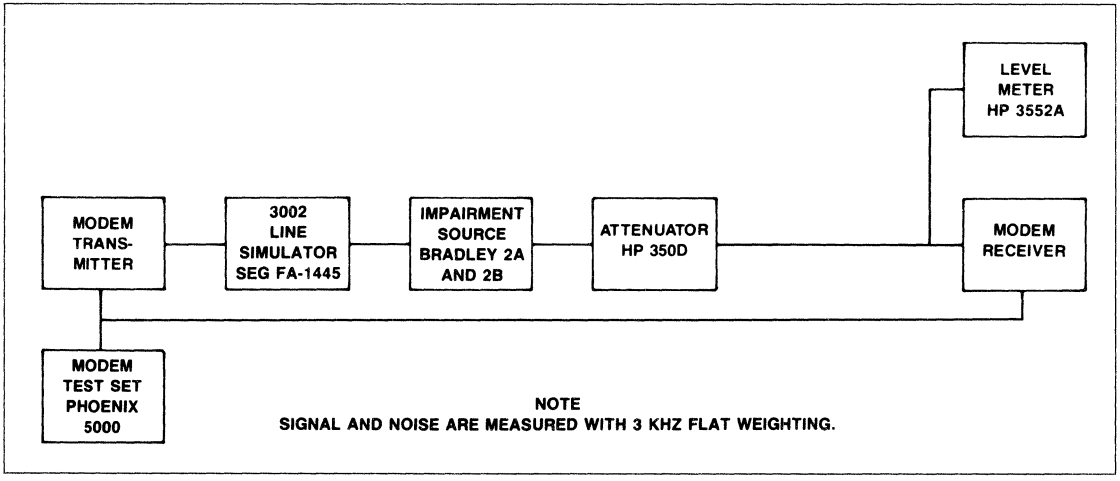


Figure 8. BER Performance Test Set-up

GENERAL SPECIFICATIONS

Table 10. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	550 mA	<700 mA
+12 Vdc	±5%	5 mA	< 10 mA
-12 Vdc	±5%	25 mA	< 50 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Table 11. Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	-40°C to +80°C (-40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	-200 feet to +10,000 feet

Table 12. Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.94 in. (100 mm)
Length	4.725 in. (120 mm)
Connector Height	0.437 in. (11.1 mm)
Component Height	
Top (max.)	0.200 in. (5.1 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max):	3.6 oz. (100 g)
Lead Extrusion (max.):	0.100 in. (2.54 mm)
DIP Connector Version	
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.228 in. (82 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0.200 in. (5.1 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.53 in. (13.5 mm)

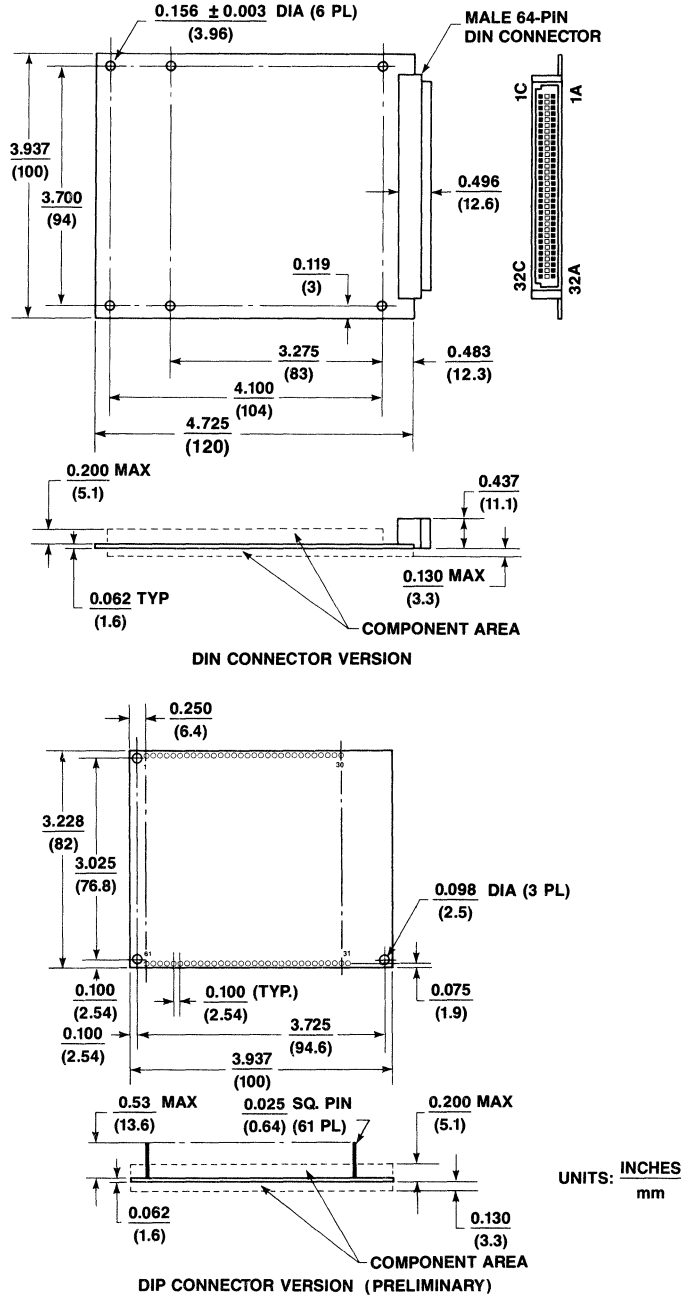


Figure 9. R208/201 Modem Dimensions and Pin Locations

Rockwell

R48DP/208
4800 bps Data Pump Modem

INTRODUCTION

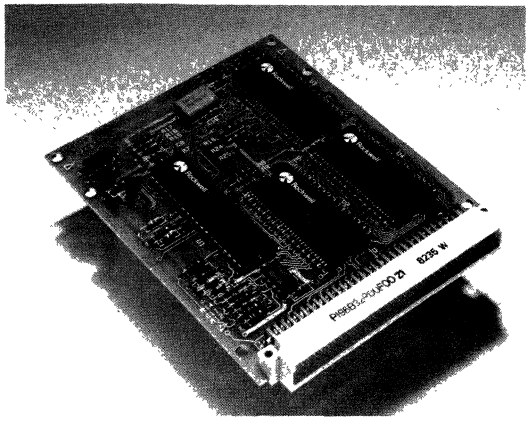
The Rockwell R48DP/208 is a synchronous 4800 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) as well as leased lines through the appropriate line termination.

The modem satisfies the telecommunications requirements specified in CCITT Recommendation V.27 bis/ter and Bell 208A/B. The R48DP/208 can operate at speeds of 4800 and 2400 bps. Employing advanced signal processing techniques, the R48DP/208 can transmit and receive data even under extremely poor line conditions.

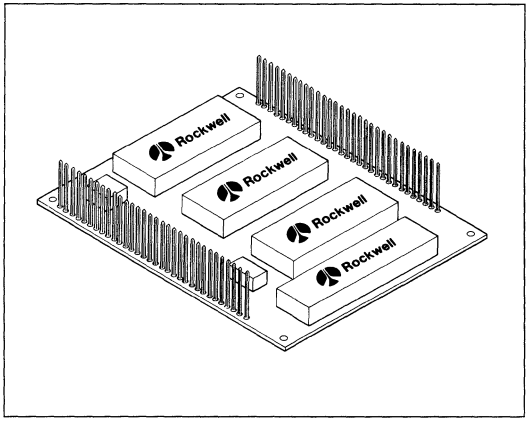
The R48DP/208 is designed for use in point-to-point environments. User programmable features allow the modem operation to be tailored to support a wide variety of functional requirements. The modem's small size, low power consumption, and serial/parallel host interface simplify system design and allow installation in a compact enclosure. The modem module is available with a DIN connector for connection to a mating connector or with dual-in-line pins (DIP) for direct plug-in installation onto a host module.

FEATURES

- CCITT V.27 bis/ter and Bell 208A/B Compatible
- Point-to-Point Applications
- 2-Wire Half-Duplex, 4-Wire Full-Duplex
- Programmable Tone Generation
- Programmable DTMF Tone Dialer
- Dynamic Range: – 43 dBm to 0 dBm
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C)(Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Diagnostic Capability
- Programmable Transmit Output Level
- Loopbacks
  - — Local and Remote Analog
  - — Remote Digital
- Small Size
  - — DIN Connector Version:
    100 mm × 120 mm (3.94 in. × 4.73 in.)
  - — DIP Connector Version:
    82 mm × 100 mm (3.23 in. × 3.94 in.)
- Power Consumption: 3 W (Typical)



R48DP/208 DIN Connector Version



R48DP/208 DIP Connector Version

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

The supported transmitter carrier frequencies are listed in Table 1.

Table 1. Transmitter Carrier Frequencies

Function	Frequency (Hz ±0.01%)
V.27 bis/ter and Bell 208 Carrier	1800

TONE GENERATION

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. DTMF tone transmission capability is provided to allow the modem to operate as a programmable DTMF tone dialer.

SIGNALING AND DATA RATES

The supported signaling and data rates are listed in Table 2.

Table 2. Signaling/Data Rates

Specification	Baud Rate (Symbols/sec.)	Bits Per Baud	Data Rate (bps)(±0.01%)	Symbol Points
V.27	1600	3	4800	8
Bell 208	1600	3	4800	4
V.27	1200	2	2400	4

DATA ENCODING

The data encoding conforms to CCITT Recommendation V.27 bis/ter and Bell 208A/B.

EQUALIZERS

The modem provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96DP incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 bis/ter or Bell 208A/B depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit can adapt to received frequency error of up to ±10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

TRANSMIT LEVEL

The transmitter output level is accurate to ±1.0 dB and is programmable from −1.0 dBm to −15.0 dBm in 2 dB steps.

TRAIN ON DATA

When train on data is enabled, the receiver typically trains on data in less than 3.5 seconds.

TURN-ON SEQUENCE

Selectable turn-on sequences can be generated as defined in Table 3.

Table 3. Turn-On Sequences

Specification	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled*
Bell 208 4800 bps long	150 ms	355 ms
Bell 208 4800 bps short	50 ms	255 ms
V.27 4800 bps long	708 ms	913 ms
V.27 4800 bps short	50 ms	255 ms
V.27 2400 bps long	943 ms	1148 ms
V.27 2400 bps short	67 ms	272 ms

* For short echo protector tone, subtract 155 ms from $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ turn-on time.

TURN-OFF SEQUENCE

For V.27 ter and Bell 208, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, diagnostic signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The six groups of hardware circuits are described in the following paragraphs. Table 5 lists the digital interface characteristics.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{\text{POR}}$) causes the modem to assume a valid operational state. The modem drives pin 13C to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 13C, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 13C low for at least 3 μs. When an external low input is applied to pin 13C, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 13C is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The modem POR sequence leaves the modem configured as follows:

- Bell 208 4800 bps Short Train
- Serial channel data
- T/2 equalizer
- Standard echo protector tone
- −43 dBm threshold
- Cable and link equalizers disabled
- Train-On-Data disabled

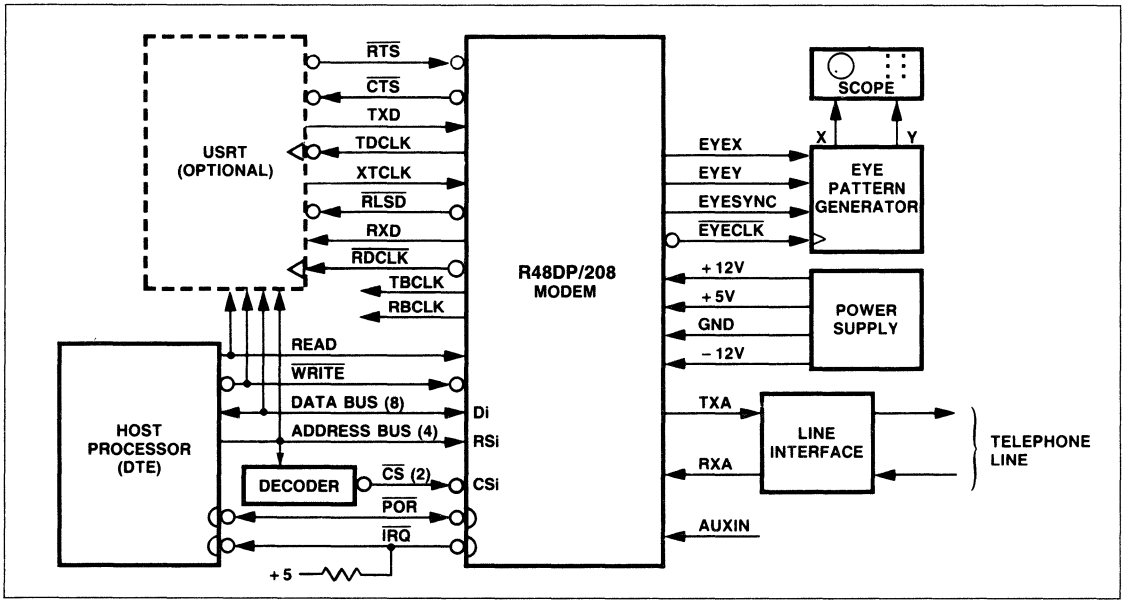


Figure 1. R48DP/208 Functional Interconnect Diagram

Table 4. R48DP/208 Hardware Circuits

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Description
A. OVERHEAD:				
Ground (A)	AGND	31C,32C	30,31	Analog Ground Return
Ground (D)	DGND	3C,8C, 5A,10A	29,37,53	Digital Ground Return
+5 volts	PWR	19C,23C, 26C,30C	1,45,61	+5 volt supply
+12 volts	PWR	15A	32	+12 volt supply
−12 volts	PWR	12A	36	−12 volt supply
$\overline{POR}$	I/OB	13C	2	Power-on-reset
B. MICROPROCESSOR INTERFACE:				
D7	I/OA	1C	3	Data Bus (8 Bits)
D6	I/OA	1A	4	
D5	I/OA	2C	5	
D4	I/OA	2A	6	
D3	I/OA	3A	7	
D2	I/OA	4C	8	
D1	I/OA	4A	9	
D0	I/OA	5C	10	
RS3	IA	6C	16	Register Select (4 Bits)
RS2	IA	6A	17	
RS1	IA	7C	18	
RS0	IA	7A	19	
$\overline{CS0}$	IA	10C	20	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	21	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	13	Chip Select Receiver Baud Rate Device
READ	IA	12C	14	Read Enable
$\overline{WRITE}$	IA	11A	12	Write Enable
$\overline{IRQ}$	OB	11C	11	Interrupt Request
C. V.24 INTERFACE:				
$\overline{RDCLK}$	OC	21A	23	Receive Data Clock
TDCLK	OC	23A	46	Transmit Data Clock
XTCLK	IB	22A	51	External Transmit Clock
$\overline{RTS}$	IB	25A	50	Request-to-Send
$\overline{CTS}$	OC	25C	49	Clear-to-Send
TXD	IB	24C	48	Transmitter Data
RXD	OC	22C	26	Receiver Data
$\overline{RLSD}$	OC	24A	27	Received Line Signal Detector
D. ANCILLARY CIRCUITS:				
RBCLK	OC	26A	22	Receiver Baud Clock
TBCLK	OC	27C	47	Transmitter Baud Clock
E. ANALOG SIGNALS:				
TXA	AA	31A	34	Transmitter Analog Output
RXA	AB	32A	33	Receiver Analog Input
AUXIN	AC	30A	—	Auxiliary Analog Input
F. DIAGNOSTIC:				
EYEX	OC	15C	56	Eye Pattern Data—X Axis
EYEY	OC	14A	55	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	57	Eye Pattern Clock
EYESYNC	OA	13A	58	Eye Pattern Synchronizing Signal

Notes:
1. Refer to Table 5 for digital circuit interface characteristics and Table 7 for analog circuit interface characteristics.
2. Pins not used on the DIP Version: 15, 24, 25, 28, 35, 38, 39, 40, 41, 42, 43, 44, 52, 54, 59, 60

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min [3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2 5 Max.						±2.5 Max [4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes
1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5 25 Vdc
5. I Load = 0 36 mA

This configuration is suitable for performing high speed data transfer using the serial data port. Individual features are discussed in subsequent paragraphs.

V.24 INTERFACE

Eight hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, + 5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The responses to $\overline{RTS}$ are shown in Table 6.

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON condition of $\overline{RTS}$ are shown in Table 6.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in data state is a maximum of 2 band times for all configurations.

Table 6. $\overline{RTS}$-$\overline{CTS}$ Response Times

Specification	$\overline{RTS}$-$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled*
Bell 208 4800 bps long	150 ms	355 ms
Bell 208 4800 bps short	50 ms	255 ms
V.27 4800 bps long	708 ms	913 ms
V.27 4800 bps short	50 ms	255 ms
V.27 2400 bps long	943 ms	1148 ms
V.27 2400 bps short	67 ms	272 ms

* For short echo protector tone, subtract 155 ms from $\overline{RTS}$-$\overline{CTS}$ turn-on time.

Received Line Signal Detector ($\overline{RLSD}$)

For V.27 bis/ter or Bell 208, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ±10 ms. The RLSD on-to-off response time for V.27 is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on the threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:

1. Greater than – 43 dBm (RLSD on)
   Less than – 49 dBm (RLSD off)
2. Greater than – 33 dBm (RLSD on)
   Less than – 38 dBm (RLSD off)
3. Greater than – 26 dBm (RLSD on)
   Less than – 31 dBm (RLSD off)
4. Greater than – 16 dBm (RLSD on)
   Less than – 21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than – 43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with an unmodulated 2400 Hz tone applied to the receiver's audio input (RXA).

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 4800 or 2400 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

TDCLK is provided to the user in synchronous communications for USRT timing. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{RDCLK}$)

The modem provides a Receive Data Clock ($\overline{RDCLK}$) output in the form of a 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. $\overline{RDCLK}$ is provided to the user in synchronous communications for USRT timing. The timing recovery circuit is capable of tracking a ± .01% frequency error in the associated transmit timing source.

MICROPROCESSOR INTERFACE

Eight hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{CS0}$-$\overline{CS2}$) and Register Selects (RS0-RS3)

The signal processor to be accessed is selected by grounding one of three unique chip select lines, $\overline{CS2}$, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable (READ) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ line high or the $\overline{WRITE}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

ANALOG SIGNALS

The analog signal characteristics are described in Table 7.

Table 7. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is 604 ohms ±1%.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is the TLVL setting +0.6 dB −1.4 dB.

Transmitter Analog (TXA)

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the public switched telephone network. The output structure of TXA is a low impedance amplifier in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

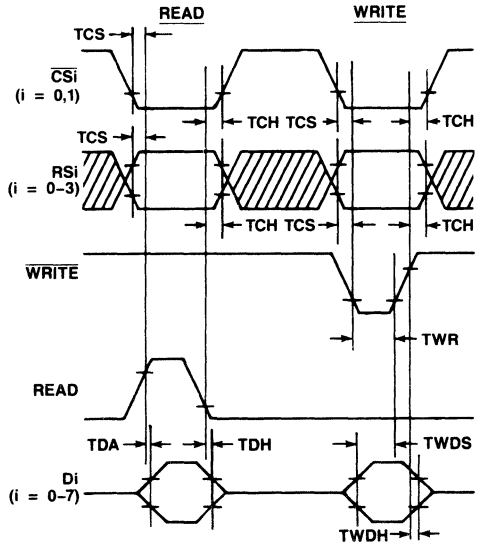
Receiver Analog (RXA)

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source. A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may take the form of back-to-back zener diodes across the transformer or a varistor across the transformer.

Auxiliary Input (AUXIN)

AUXIN provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit at a rate of 9600 samples-per-second. Any signal above 4800 Hz on the AUXIN line will be aliased back into the passband as noise. One application for AUXIN is to inject dual-tone multifrequency (DTMF) touch-tone signals for dialing, however, the source of these tones must be well filtered to eliminate components above 4800 Hz. The input impedance of AUXIN is 1K ohm. The gain from AUXIN to TXA is the same as the selected transmit level +0.6 dB −1.4 dB.



Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
$\overline{CSi}$, RSi hold time after Read or $\overline{Write}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram

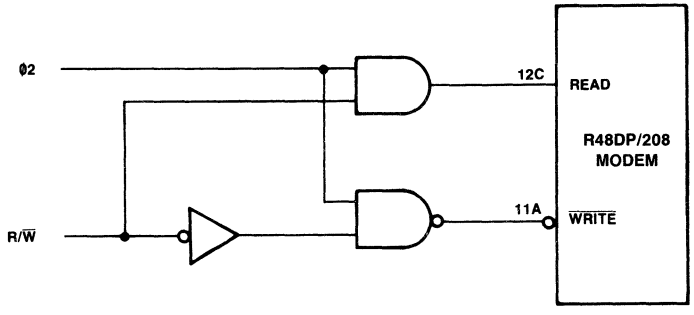


Figure 3. R/$\overline{W}$ to READ $\overline{WRITE}$ Conversion Logic

DIAGNOSTIC SIGNALS
EYEX, EYEY, EYECLK, and EYESYNC

Four card edge connections provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances as well as defects in the modulation/demodulation process.

The outputs EYEX and EYEY provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. Since this data is in serial digital form it must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two D/A converters. A clock for use by the serial-to-parallel converters is furnished by signal EYECLK. A strobe for loading the D/A converters is furnished by signal EYESYNC. Timing of these signals is illustrated in Figure 4. The EYEX and EYEY outputs furnish 9-bit serial words. Since most serial to parallel conversion logic is designed for 8-bit words, an extra storage flip-flop is required for 9-bit resolution. However, the ninth bit is not generally needed for eyepattern generation, and eight-bit hardware can be used if data is copied on the rising edge of EYECLK rather than the falling edge.

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Two clock signals called TBCLK and RBCLK are provided at the modem connector. These signals have no counterpart in the V.24 or RS-232 recommendations since they mark the baud interval for the transmitter and receiver rather than the data rate. The baud clocks can be useful in identifying the order of data bits in a baud (e.g., for multiplexing data, etc.). Both signals are high active, meaning the baud boundaries occur on falling edges. The first bit in each baud begins with the falling edge of the corresponding baud clock.

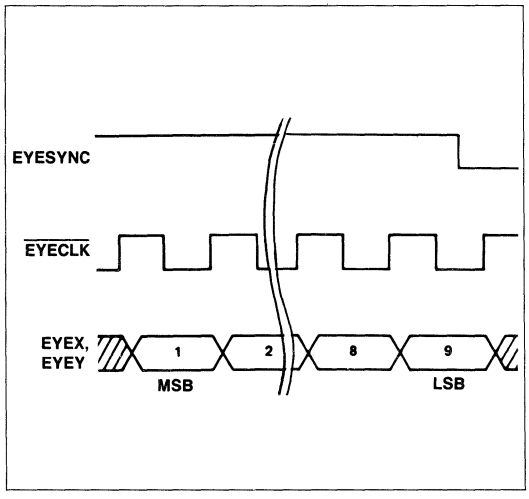


Figure 4. Eye Pattern Timing

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on three special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into areas. These areas are partitioned into transmitter, baud rate, and sample rate devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 48 addressable registers in the modem are shown in Figure 5. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Table 8 defines the individual bits in the interface memory. In the Table 8 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS T							
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	—	—	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	RAM DATA YTM							
0	RAM DATA YTL; TRANSMITTER DATA, DDR							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	SQH	—	—	—	—	—	—	—
E	RSIA	—	—	—	RSB	RSIE	—	RSDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	—	$\overline{TONE}$	—	—
8	—	—	—	—	—	$\overline{P2DET}$	—	—
7	RTH		DDIS	RPDM	SWRT	BWRT	T2	RTDIS
6	IFIX	TOD	RECEIVER CONFIGURATION					
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL, RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 5. Interface Memory Map

Table 8. R48DP/208 Interface Memory Definitions

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>A3L</td><td>Amplitude 3-Link Select</td><td>0:5:1</td><td>A3L is used in conjunction with LAEN. When A3L is a one the Japanese 3 link equalizer is selected and when A3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
<tr><td>BWRT</td><td>Baud Write</td><td>1:7:2</td><td>When control bit BWRT is a one, the RAM write operation is enabled for Chip 2</td></tr>
<tr><td>CEQ</td><td>Cable Equalizer Field</td><td>0:5:4,5</td><td>The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following tables list the possible cable equalizer selection codes and responses.

<table>
<tr><th>CEQ</th><th>Cable Length (0.4 mm diameter)</th></tr>
<tr><td>0</td><td>0.0</td></tr>
<tr><td>1</td><td>1.8 km</td></tr>
<tr><td>2</td><td>3.6 km</td></tr>
<tr><td>3</td><td>7.2 km</td></tr>
</table>

Cable Equalizer Nominal Gain

CEQ CODE 1
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>Transmitter</th><th>Receiver</th></tr>
<tr><td>700</td><td>−0.99</td><td>−0.94</td></tr>
<tr><td>1500</td><td>−0.20</td><td>−0.24</td></tr>
<tr><td>2000</td><td>+0.15</td><td>+0.31</td></tr>
<tr><td>3000</td><td>+1.43</td><td>+1.49</td></tr>
</table>

CEQ CODE 2
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>Transmitter</th><th>Receiver</th></tr>
<tr><td>700</td><td>−2.39</td><td>−2.67</td></tr>
<tr><td>1500</td><td>−0.65</td><td>−0.74</td></tr>
<tr><td>2000</td><td>+0.87</td><td>+1.02</td></tr>
<tr><td>3000</td><td>+3.06</td><td>+3.17</td></tr>
</table>

CEQ CODE 3
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>Transmitter</th><th>Receiver</th></tr>
<tr><td>700</td><td>−3.93</td><td>−3.98</td></tr>
<tr><td>1500</td><td>−1.22</td><td>−1.20</td></tr>
<tr><td>2000</td><td>+1.90</td><td>+1.81</td></tr>
<tr><td>3000</td><td>+4.58</td><td>+4.38</td></tr>
</table>

Unless a problem with training or high bit error rate is encountered, most applications operate successfully with no cable equalizer selected.</td></tr>
<tr><td>$\overline{\text{CDET}}$</td><td>Carrier Detector</td><td>1:B:0</td><td>When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$ If the $\overline{\text{FED}}$ bit goes to a zero and no P2 sequence is detected, the $\overline{\text{CDET}}$ bit goes to zero within 5 to 25 ms indicating that the receiver has entered the data state without a training sequence.</td></tr>
<tr><td>DDIS</td><td>Descramble Disable</td><td>1:7:5</td><td>When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.</td></tr>
<tr><td>DDR</td><td>Dial Digit Register</td><td>0:0:0–7</td><td>DDR is used to tell the modem which DTMF digit to transmit (see Transmitter Data).</td></tr>
<tr><td>D3L</td><td>Delay 3-Link Select</td><td>0:5:0</td><td>D3L is used in conjunction with LDEN. When D3L is a one the Japanese 3 link equalizer is selected and when D3L is a zero the U.S Survey Long link equalizer is selected.</td></tr>
</table>

Table 8. R48DP/208 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
EPT	Echo Protector Tone	0:7.3	When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission.
$\overline{\text{FED}}$	Fast Energy Detector	1.9.6	When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband, and the receiver is searching for the training sequence.
(None)	FREQL/FREQM	0 2:0–7, 0.3 0–7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below:
IFIX	Eye Fix	1 6:7	When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB.
LAEN	Link Amplitude Equalizer Enable	0:5·3	The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table:

FREQM Register (0:3)

Bit:	7	6	5	4	3	2	1	0
Data Word:	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}

FREQL Register (0:2)

Bit:	7	6	5	4	3	2	1	0
Data Word:	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

The frequency number (N) determines the frequency (F) as follows:
F = (0 146486) (N) Hz ±0.01%

Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below:

FREQM	FREQL	Frequency (Hz)
0C	52	462
1D	55	1100
2C	00	1650
31	55	1850
38	00	2100

LAEN	A3L	Curve Matched
0	X	No Equalizer
1	0	U.S. Survey Long
1	1	Japanese 3-Link

The link amplitude equalizer responses are given in the following table.

Link Amplitude Equalizer

Frequency (Hz)	Gain Relative to 1700 Hz (dB)	
	U.S. Survey Long	Japanese 3-Link
1000	−0.27	−0.13
1400	−0.16	−0.08
2000	+0.33	+0.16
2400	+1 54	+0.73
2800	+5.98	+2.61
3000	+8.65	+3 43

Table 8. R48DP/208 Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>LCEN</td><td>Loop Clock Enable</td><td>0:4:0</td><td>When control bit LCEN is a one, the transmitter clock tracks the receiver clock.</td></tr>
<tr><td>LDEN</td><td>Link Delay Equalizer Enable</td><td>0:5:2</td><td>The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table:

<table>
<tr><th>LDEN</th><th>D3L</th><th>Curve Matched</th></tr>
<tr><td>0</td><td>X</td><td>No Equalizer</td></tr>
<tr><td>1</td><td>0</td><td>U.S. Survey Long</td></tr>
<tr><td>1</td><td>1</td><td>Japanese 3-Link</td></tr>
</table>
The link delay equalizer responses are given in the following table.

Link Delay Equalizer
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Delay Relative to 1700 Hz (Microseconds)</th></tr>
<tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr>
<tr><td>800</td><td>-498.1</td><td>-653.1</td></tr>
<tr><td>1200</td><td>-188.3</td><td>-398.5</td></tr>
<tr><td>1600</td><td>-15.1</td><td>-30.0</td></tr>
<tr><td>1700</td><td>+0.0</td><td>+0.0</td></tr>
<tr><td>2000</td><td>-39.8</td><td>+11.7</td></tr>
<tr><td>2400</td><td>-423.1</td><td>-117.1</td></tr>
<tr><td>2800</td><td>-672.4</td><td>-546.3</td></tr>
</table></td></tr>
<tr><td>L2ACT</td><td>Remote Digital Loopback Activate</td><td>0:4:1</td><td>When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2.</td></tr>
<tr><td>L3ACT</td><td>Local Analog Loopback Activate</td><td>0:4:7</td><td>When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.</td></tr>
<tr><td>L4ACT</td><td>Remote Analog Loopback Activate</td><td>0:4:6</td><td>When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4.</td></tr>
<tr><td>L4HG</td><td>Loop 4 High Gain</td><td>0:4:5</td><td>When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.</td></tr>
<tr><td>MHLD</td><td>Mark Hold</td><td>0:7:4</td><td>When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).</td></tr>
<tr><td>$\overline{\text{PNDET}}$</td><td>Period N Detector</td><td>1:B:6</td><td>When status bit $\overline{\text{PNDET}}$ is a zero, it indicates a PN sequence has been detected. This bit sets to a one at the end of the PN sequence.</td></tr>
<tr><td>$\overline{\text{P2DET}}$</td><td>Period Two Detector</td><td>1:8:2</td><td>When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a P2 sequence has been detected. This bit sets to a one at the start of the PN sequence.</td></tr>
<tr><td>(None)</td><td>RAM Access T</td><td>0:F:0–7</td><td>Contains the RAM access code used in reading or writing chip 0 RAM locations via word Y (0:1 and 0:0).</td></tr>
<tr><td>(None)</td><td>RAM Access XB</td><td>2:5:0–7</td><td>Contains the RAM access code used in reading or writing chip 2 RAM locations via word X (2:3 and 2:2).</td></tr>
<tr><td>(None)</td><td>RAM Access XS</td><td>1:5:0–7</td><td>Contains the RAM access code used in reading or writing chip 1 RAM locations via word X (1:3 and 1:2).</td></tr>
<tr><td>(None)</td><td>RAM Access YB</td><td>2:4:0–7</td><td>Contains the RAM access code used in reading or writing chip 2 RAM locations via word Y (2:1 and 2:0).</td></tr>
</table>

Table 8. R48DP/208 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Access YS	1·4·0–7	Contains the RAM access code used in reading or writing chip 1 RAM locations via word Y (1·1 and 1 0).
(None)	RAM Data XBL	2 2·0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 2.
(None)	RAM Data XBM	2·3:0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 2
(None)	RAM Data XSL	1·2·0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 1.
(None)	RAM Data XSM	1:3:0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 1
(None)	RAM Data YBL	2:0 0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YBM	2:1.0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YSL	1:0·0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus. See 'Receiver Data.'
(None)	RAM Data YSM	1:1·0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1.
(None)	RAM Data YTL	0:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 0 It is shared by parallel data mode and DTMF dialing (see Transmitter Data).
(None)	RAM Data YTM	0:1 0–7	Most significant byte of 16-byte word Y used in reading or writing locations in chip 0.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low. In idle mode the interrupts from chip 2 occur at half the baud rate During diagnostic access in data mode, the interrupts occur at the baud rate.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
(None)	Receiver Configuration	1:6·0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB). *Receiver Configuration Control Codes* Control codes for the modem receiver configuration are: **Configuration Code (Hex) — Receiver Configuration** 16 — Bell 208A/B HDX 12 — Bell 208A/B FDX 26 — V 27 4800 HDX Long 22 — V.27 4800 FDX Long 25 — V.27 2400 HDX Long 21 — V.27 2400 FDX Long 06 — V 27 4800 HDX Short 05 — V.27 2400 HDX Short 02 — V 27 4800 FDX Short 01 — V.27 2400 FDX Short 08 — Tone Detector

Table 8. R48DP/208 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	Receiver Data	1:0:0–7	The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data When using receiver parallel data mode, the registers 1:3 through 1:0 can not be used for reading the chip 1 RAM.
RPDM	Receiver Parallel Data Mode	1:7:4	When control bit RPDM is a one, the receiver supplies channel data to the receiver data register (1:0) as well as to the hardware serial data output (See Receiver Data)
RSB	Receiver Setup Bit	1:E:3	When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective. Worst case setup time is 2 baud times
RSDA	Receiver Sample Data Available	1:E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0. RSDA goes to a zero when the host processor reads data from register 1:0.
RSIA	Receiver Sample Interrupt Active	1:E:7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is a one.
RTDIS	Receiver Training Disable	1:7:0	When control bit RTDIS is a one, the receiver is prevented from recognizing a training sequence and entering the training state.
RTH	Receiver Threshold Field	1:7:6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH** / **RLSD On** / **RLSD Off** 0 / > –43 dBm / < –48 dBm 1 / > –33 dBm / < –38 dBm 2 / > –26 dBm / < –31 dBm 3 / > –16 dBm / < –21 dBm
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are ORed by the modem.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector tone is 30 ms long rather than 185 ms.
SQH	Receiver Squelch	1:F:7	When control bit SQH is set to a one, the receiver is squelched, $\overline{RLSD}$ is turned off and RXD is clamped to all marks. SQH only affects the receiver operation when a half duplex receiver configuration has been selected.
SWRT	Sample Write	1:7:3	When control bit SWRT is a one, the RAM write operation is enabled for chip 1.
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one. During a RAM access in chip 0, when TBA is a one the host can perform either a RAM read or write depending on the state of bit 0:6·3 (see Transmitter Configuration).
TIA	Transmitter Interrupt Active	0.E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero
TIE	Transmitter Interrupt Enable	0:E·2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.

Table 8. R48DP/208 Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL** — **Transmitter Analog Output*** 0 — −1 dBm ±1 dB 1 — −3 dBm ±1 dB 2 — −5 dBm ±1 dB 3 — −7 dBm ±1 dB 4 — −9 dBm ±1 dB 5 — −11 dBm ±1 dB 6 — −13 dBm ±1 dB 7 — −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-on-Data	1:6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-date.
$\overline{\text{TONE}}$	Tone Detect	1:9:2	$\overline{\text{TONE}}$ indicates with a zero the presence of energy in the 345–650 ±10 Hz frequency range. For call progress purposes, the user may determine which tone is present by determining the duty cycle of the $\overline{\text{TONE}}$ bit.
TPDM	Transmitter Parallel Data Mode	0:7 2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0). When TPDM is a zero channel data from the serial hardware input TXD is accepted and the chip 0 RAM access is enabled.
(None)	Transmitter Configuration*	0:6:0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space (See TSB.) *Transmitter Configuration Control Codes* Control codes for the modem transmitter configurations are: **Configuration Code (Hex)*** — **Transmitter Configuration** 32 — Bell 208A/B Long 12 — Bell 208A/B Short 22 — V.27 4800 Long 21 — V.27 2400 Long 02 — V.27 4800 Short 01 — V.27 2400 Short 80 — Tone Transmit 04 — DTMF Tone Transmit ***Note:** Bit 3 of the transmitter configuration register is used in the RAM access operation for chip 0. When 0.6:3 is a one, a RAM write operation will occur when TPDM is a zero, and when 0:6:3 is a zero, a RAM read operation will occur when TPDM is a zero **Configuration Definitions** Definitions of the eight Transmitter Configurations are: 1 *Bell 208.* When a Bell 208 configuration has been selected, the modem operates as specified in Bell 208A/B. 2. *V.27.* When a V.27 configuration has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 3. *Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by two registers in the host interface memory space containing the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0.2). The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%. 4. *DTMF Tone Transmit.* In this configuration when the hex value of a DTMF digit is stored in register 0 0, a DTMF tone will be transmitted if RTS is enabled.

Table 8. R48DP/208 Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter; DDR; RAM Data YTL</td><td>0:0:0–7</td><td>1. The host processor transmits data in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

NOTE

Data is transmitted bit zero first.

<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>Bell 208 4800 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table>

2. Register 0:0 is used to transmit DTMF digits when the transmitter is configured in the DTMF tone transmit mode.

3. Register 0:0 is a RAM data register used for reading or writing the least significant byte of the 16-bit Y word in Chip 0 when TPDM is a zero and no tone or DTMF tone transmission is occurring.</td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective. Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>T2</td><td>T/2 Equalizer Select</td><td>1:7:1</td><td>When control bit T2 is a one, an adaptive equalizer with two taps per baud is used. When T2 is a zero, the equalizer has one tap per baud. The total number of taps remains the same for both cases.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a zero, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A. The clock appearing at the XTCLK input will appear at the TDCLK output.</td></tr>
</table>

SIGNAL PROCESSOR RAM ACCESS

RAM and Data Organization

Each signal processor contains 128 words of random access memory (RAM). Each word is 32 bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16 bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. In the sample rate and baud rate devices the entire contents of XRAM and YRAM may be read from or written into by the host processor via the microprocessor interface. Access to the YRAM is possible only in the transmitter device.

Interface Memory

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit determines the RAM address to read from or write into by the code stored in the RAM ACCESS bits of interface memory registers. The SP logic unit normally transfers a word from RAM to interface memory once each cycle of the device code. Each RAM word transferred to the interface memory is 32 bits long (16 bits in the transmitter). These bits are written by the SP logic unit into interface memory registers 3, 2, 1, and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data, respectively. As previously described for parallel data mode, the data available bits set to a one when register 0 of the respective signal processor is written into by the device and resets to a zero when register 0 is read from by the host. Since the parallel data mode transmitter and receiver data register shares register 0 with the YRAM data, chip 0 and 1 RAM access are disabled in parallel data mode. However, chip 2 RAM access remains active in receiver parallel data mode.

The transmitter, sample rate device and the baud rate device allow data to be transferred from interface memory to RAM. When set to a one, bit SWRT (1:7:3) signals the chip 1 SP logic unit to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. Bit BWRT (1:7:2) performs the same function for chip 2 RAM. When writing into the RAM, 32 bits are transferred. The 16 bits written into XRAM come from registers 3 and 2, with register 3 being the more significant byte. The 16 bits written into YRAM come from registers 1 and 0, with register 1 being the more significant byte. When only 16 bits of data are to be written, FF (a dummy RAM location) must be stored in RAM ACCESS XS or RAM ACCESS YS to prevent writing the insignificant 16 bits of registers 1:3 through 1:0 into a valid RAM location. When the host processor writes into register 1:0 the RSDA bit (1:E:0) is reset to zero. When the SP logic unit reads data from register 1:0, the RSDA bit (1:E:0) is set to a one. In a similar manner, bit RBDA (2:E:0) resets to zero when the host processor writes into register 2:0 and sets to a one when the SP logic unit reads data from register 2:0.

When reading from RAM, or writing into RAM, the bits in registers 0:E, 1:E, 2:E can be used for handshaking or interrupt functions as in parallel data mode. When not in parallel data mode, the bits in register 1:E perform the handshake and interrupt functions for RAM access. In both serial and parallel data modes, the bits in register 2:E perform handshake and interrupt functions for RAM access. When set to one, bit RBIE (2:E:2) enables RBDA to drive the IRQ connector signal to zero volts when RBDA is a one. Bit RBIA (2:E:7) identifies chip 2, the baud rate device, as a source of IRQ interrupt. Bit RBIA is a one when both RBIE and RBDA are set to one. In the event that other system elements may cause IRQ to be driven low, the host must determine if modem chip 2 is causing an interrupt by reading RBIA.

Table 9 provides the available RAM access functions, codes, and registers.

Auto Dial Sequence

The Figure 6 flowchart defines the auto dial sequence via the microprocessor interface memory. The modem timing for the auto dialer accounts for DTMF tone duration and interdigit delay. The default tone duration is 95 ms and the default interdigit delay is 71 ms. The default amplitudes for the high and low frequencies are – 4 dBm and – 6 dBm, respectively. The above four parameters can be changed by performing a RAM write.

Table 9. RAM Access Codes

No.	Function	Chip	X Access Code (Hex)	Y Access Code (Hex)	Register
1	DTMF Low Frequency Amplitude	0	—	88	0,1
2	DTMF High Frequency Amplitude	0	—	08	0,1
3	Interdigit Delay	0	—	89	0,1
4	DTMF Tone Duration	0	—	09	0,1
5	Received Signal Samples	1	C0	Not Used	2,3
6	Demodulator Output	1	C2	42	0,1,2,3
7	Low Pass Filter Output	1	D4	54	0,1,2,3
8	Average Energy	1	DC	Not Used	2,3
9	AGC Gain Word	1	81	Not Used	2,3
10	Equalizer Input	2	C0	40	0,1,2,3
11	Equalizer Tap Coefficients	2	81 – A0	01 – 20	0,1,2,3
12	Unrotated Equalizer Output	2	E1	61	0,1,2,3
13	Rotated Equalizer Output (Received Points)	2	A2	22	0,1,2,3
14	Decision Points Ideal Points	2	62	0,1,2,3	
15	Error	2	E3	63	0,1,2,3
16	Rotation Angle	2	Not Used	00	0,1
17	Frequency Correction	2	AA	Not Used	2,3
18	EQM	2	A7	Not Used	2,3
19	Dual Point	2	AE	2E	0,1,2,3

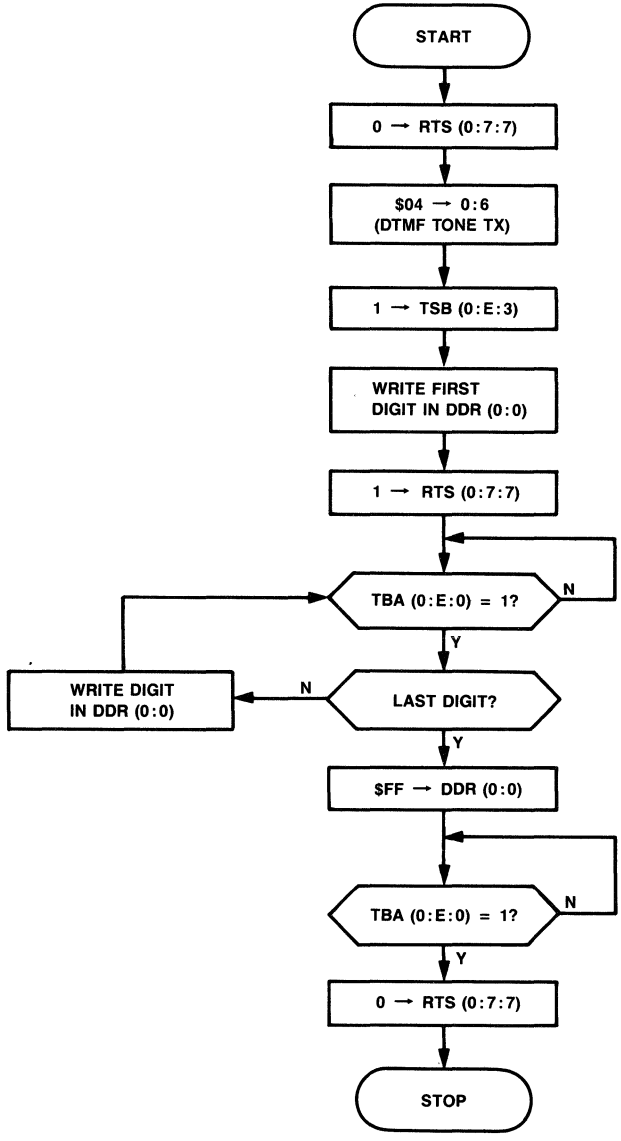


Figure 6. R48DP/208 Auto Dial Sequence

PERFORMANCE

TYPICAL BIT ERROR RATES

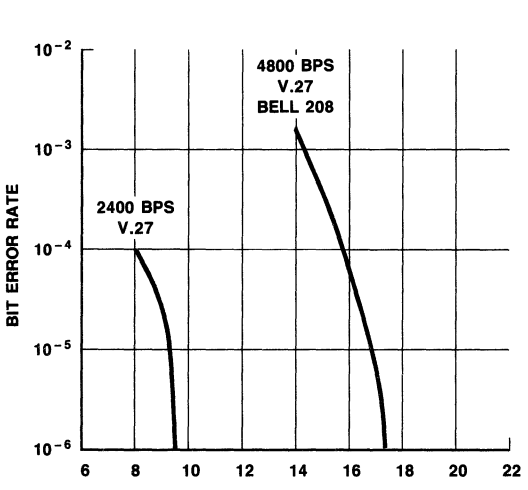
The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

Typical BER performance is shown in Figure 7. Figure 8 shows a typical test setup to measure BER.

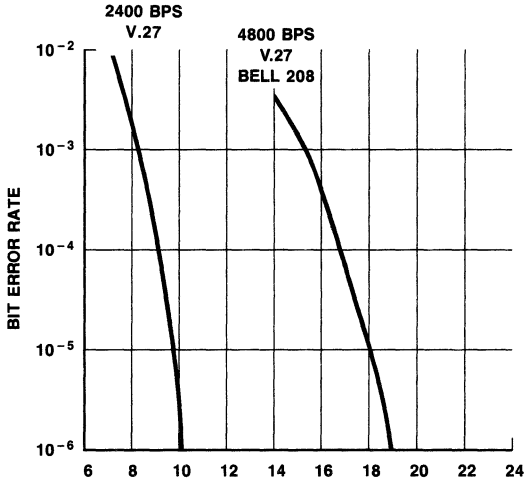
TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.



a) TYPICAL BIT ERROR RATE
(BACK TO BACK, T/2 EQUALIZER, −20 dBm)



b) TYPICAL BIT ERROR RATE
(UNCONDITIONED 3002 LINE, T/2 EQUALIZER, −20 dBm)

Figure 7. R48DP/208 BER versus SNR

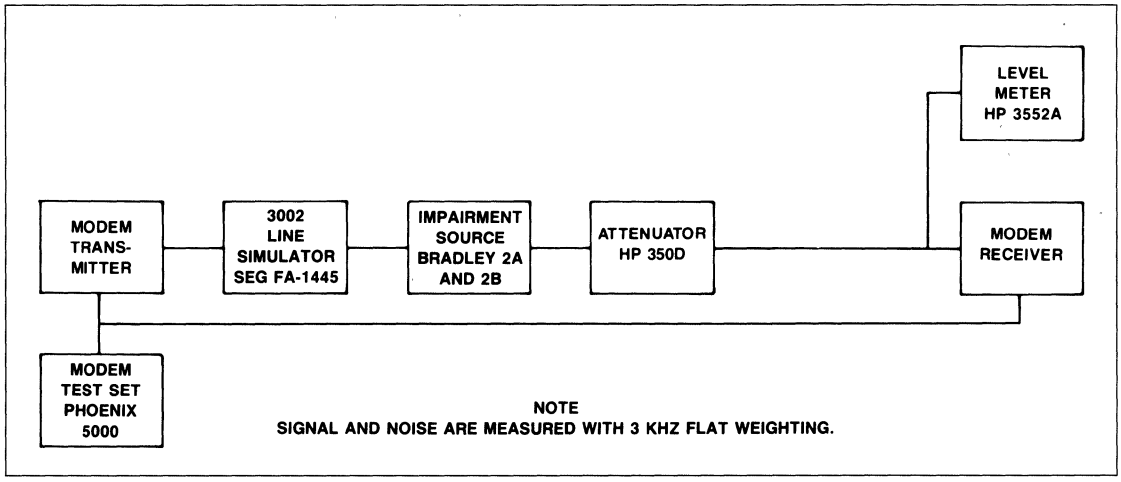


Figure 8. BER Performance Test Set-up

GENERAL SPECIFICATIONS

Table 10. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	550 mA	<700 mA
+12 Vdc	±5%	5 mA	< 10 mA
−12 Vdc	±5%	25 mA	< 50 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Table 11. Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	−200 feet to +10,000 feet

Table 12. Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	
Board Structure·	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Connector Height	0.437 in. (11.1 mm)
Component Height	
Top (max.)	0 200 in. (5.1 mm)
Bottom (max)	0.130 in (3.3 mm)
Weight (max):	3 6 oz. (100 g)
Lead Extrusion (max.)·	0 100 in. (2.54 mm)
DIP Connector Version	
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3 228 in. (82 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0 200 in. (5.1 mm)
Bottom (max)	0 130 in. (3.3 mm)
Weight (max.):	3 6 oz. (100 g)
Pin Length (max.)	0.53 in (13.5 mm)

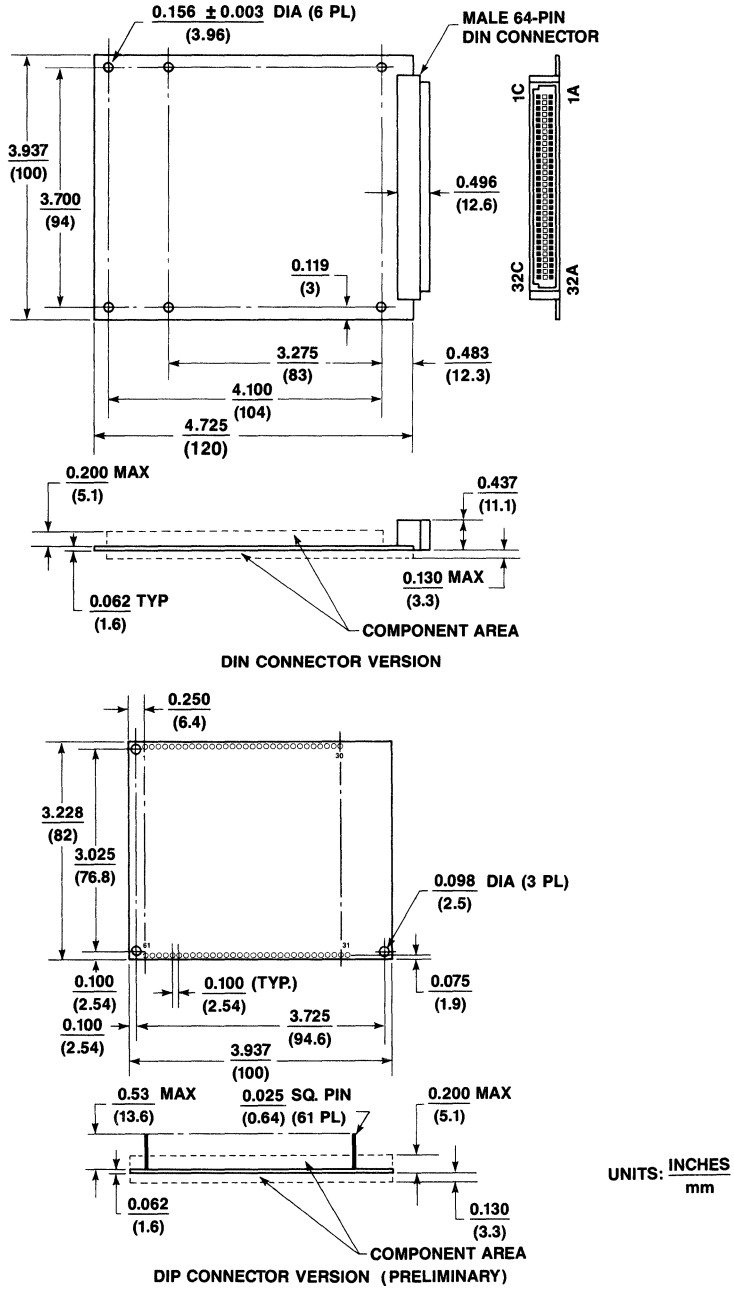


Figure 9. R48DP/208 Modem Dimensions and Pin Locations

Rockwell

R48DP
4800 bps Data Pump Modem

INTRODUCTION

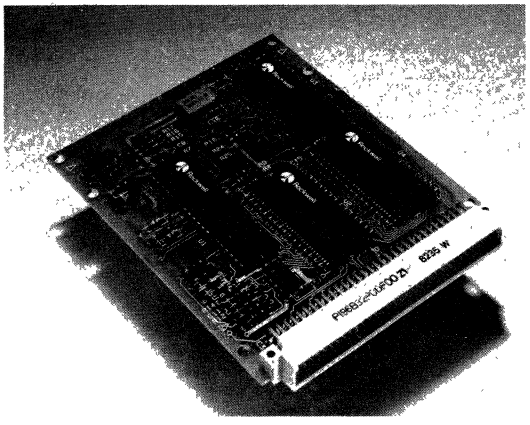
The Rockwell R48DP is a synchronous 4800 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) as well as leased lines through the appropriate line termination.

The modem satisfies the telecommunications requirements specified in CCITT Recommendation V.27 bis/ter. The R48DP can operate at speeds of 4800 and 2400 bps. Employing advanced signal processing techniques, the R48DP can transmit and receive data even under extremely poor line conditions.

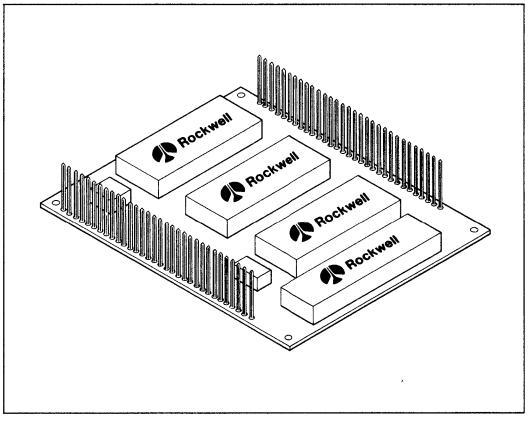
The R48DP is designed for use in point-to-point environments. User programmable features allow the modem operation to be tailored to support a wide variety of functional requirements. The modem's small size, low power consumption, and serial/parallel host interface simplify system design and allow installation in a compact enclosure. The modem module is available with a DIN connector for connection to a mating connector or with dual-in-line pins (DIP) for direct plug-in installation onto a host module.

FEATURES

- CCITT V.27 bis/ter Compatible
- Point-to-Point Applications
- 2-Wire Half-Duplex, 4-Wire Full-Duplex
- Programmable Tone Generation
- Dynamic Range: – 43 dBm to 0 dBm
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C)(Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Diagnostic Capability
- Programmable Transmit Output Level
- Loopbacks
  - — Local and Remote Analog
  - — Remote Digital
- Small Size
  - — DIN Connector Version: 100 mm x 120 mm (3.94 in. x 4.73 in.)
  - — DIP Connector Version: 82 mm x 100 mm (3.23 in. x 3.94 in.)
- Power Consumption: 3 W (Typical)



R48DP DIN Connector Version



R48DP DIP Connector Version

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

The supported transmitter carrier frequencies are listed in Table 1.

Table 1. Transmitter Carrier Frequencies

Function	Frequency (Hz ±0.01%)
V.27 bis/ter Carrier	1800

TONE GENERATION

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

The supported signaling and data rates are listed in Table 2.

Table 2. Signaling/Data Rates

Specification	Baud Rate (Symbols/sec.)	Bits Per Baud	Data Rate (bps)(±0.01%)	Symbol Points
V.27	1600	3	4800	8
V.27	1200	2	2400	4

DATA ENCODING

The data encoding conforms to CCITT Recommendation V.27 bis/ter.

EQUALIZERS

The modem provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with V.27 bis/ter.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit can adapt to received frequency error of up to ± 10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to – 43 dBm. The received line signal level is measured at the receiver analog input (RXA).

TRANSMIT LEVEL

The transmitter output level is accurate to ± 1.0 dB and is programmable from – 1.0 dBm to – 15.0 dBm in 2 dB steps.

TRAIN ON DATA

When train on data is enabled, the receiver typically trains on data in less than 3.5 seconds.

TURN-ON SEQUENCE

Selectable turn-on sequences can be generated as defined in Table 3.

Table 3. Turn-On Sequences

Specification	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector* Tone Enabled
V.27 4800 bps long	708 ms	913 ms
V.27 4800 bps short	50 ms	255 ms
V.27 2400 bps long	943 ms	1148 ms
V.27 2400 bps short	67 ms	272 ms

* For short echo protector tone, subtract 155 ms from $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ turn-on time.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, diagnostic signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The six groups of hardware circuits are described in the following paragraphs. Table 5 lists the digital interface characteristics.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{\text{POR}}$) causes the modem to assume a valid operational state. The modem drives pin 13C to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 13C, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 13C low for at least 3 μs. When an external low input is applied to pin 13C, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 13C is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The modem POR sequence leaves the modem configured as follows:

- V.27, 4800 bps Short Train
- Serial channel data
- T/2 equalizer
- Standard echo protector tone
- −43 dBm threshold
- Cable and link equalizers disabled
- Train-On-Data disabled

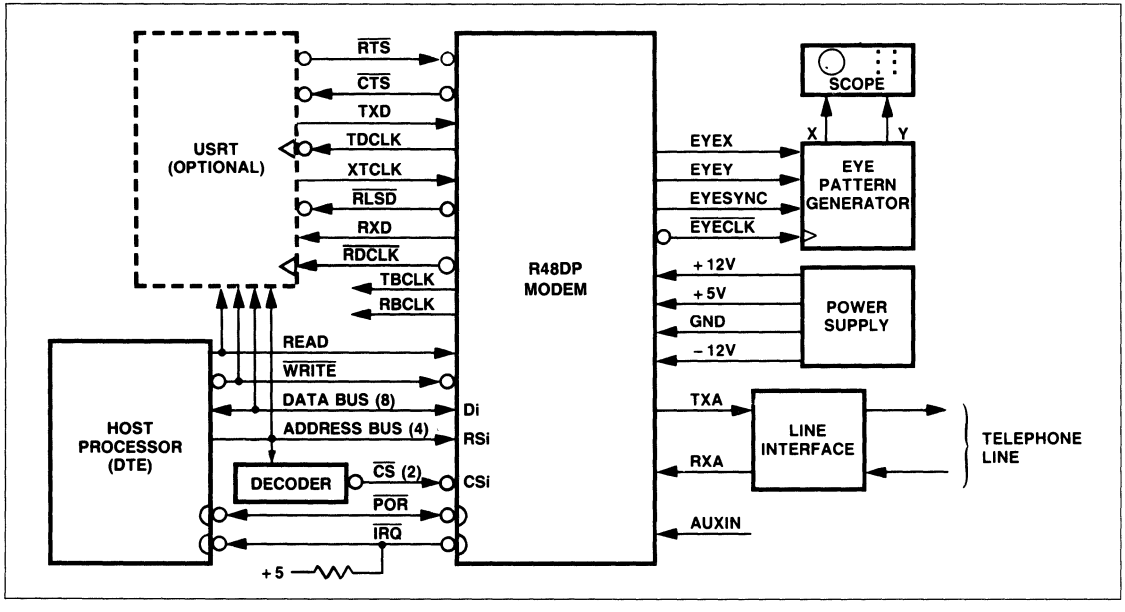


Figure 1. R48DP Functional Interconnect Diagram

Table 4. R48DP Hardware Circuits

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Description
A. OVERHEAD:				
Ground (A)	AGND	31C,32C	30,31	Analog Ground Return
Ground (D)	DGND	3C,8C, 5A,10A	29,37,53	Digital Ground Return
+5 volts	PWR	19C,23C, 26C,30C	1,45,61	+5 volt supply
+12 volts	PWR	15A	32	+12 volt supply
−12 volts	PWR	12A	36	−12 volt supply
$\overline{POR}$	I/OB	13C	2	Power-on-reset
B. MICROPROCESSOR INTERFACE:				
D7	I/OA	1C	3	Data Bus (8 Bits)
D6	I/OA	1A	4	
D5	I/OA	2C	5	
D4	I/OA	2A	6	
D3	I/OA	3A	7	
D2	I/OA	4C	8	
D1	I/OA	4A	9	
D0	I/OA	5C	10	
RS3	IA	6C	16	Register Select (4 Bits)
RS2	IA	6A	17	
RS1	IA	7C	18	
RS0	IA	7A	19	
$\overline{CS0}$	IA	10C	20	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	21	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	13	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	12C	14	Read Enable
$\overline{WRITE}$	IA	11A	12	Write Enable
$\overline{IRQ}$	OB	11C	11	Interrupt Request

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Description
C. V.24 INTERFACE:				
$\overline{RDCLK}$	OC	21A	23	Receive Data Clock
TDCLK	OC	23A	46	Transmit Data Clock
XTCLK	IB	22A	51	External Transmit Clock
$\overline{RTS}$	IB	25A	50	Request-to-Send
$\overline{CTS}$	OC	25C	49	Clear-to-Send
TXD	IB	24C	48	Transmitter Data
RXD	OC	22C	26	Receiver Data
$\overline{RLSD}$	OC	24A	27	Received Line Signal Detector
D. ANCILLARY CIRCUITS:				
RBCLK	OC	26A	22	Receiver Baud Clock
TBCLK	OC	27C	47	Transmitter Baud Clock
E. ANALOG SIGNALS:				
TXA	AA	31A	34	Transmitter Analog Output
RXA	AB	32A	33	Receiver Analog Input
AUXIN	AC	30A	—	Auxiliary Analog Input
F. DIAGNOSTIC:				
EYEX	OC	15C	56	Eye Pattern Data—X Axis
EYEY	OC	14A	55	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	57	Eye Pattern Clock
EYESYNC	OA	13A	58	Eye Pattern Synchronizing Signal

Notes:
1. Refer to Table 5 for digital circuit interface characteristics and Table 7 for analog circuit interface characteristics.
2. Pins not used on the DIP Version: 15, 24, 25, 28, 35, 38, 39, 40, 41, 42, 43, 44, 52, 54, 59, 60

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes
1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I Load = 0.36 mA

This configuration is suitable for performing high speed data transfer using the serial data port. Individual features are discussed in subsequent paragraphs.

V.24 INTERFACE

Eight hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, +5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The responses to $\overline{RTS}$ are shown in Table 6.

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON condition of $\overline{RTS}$ are shown in Table 6.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in data state is a maximum of 2 band times for all configurations.

Table 6. $\overline{RTS}$-$\overline{CTS}$ Response Times

Specification	$\overline{RTS}$-$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector* Tone Enabled
V.27 4800 bps long	708 ms	913 ms
V.27 4800 bps short	50 ms	255 ms
V.27 2400 bps long	943 ms	1148 ms
V.27 2400 bps short	67 ms	272 ms

* For short echo protector tone, subtract 155 ms from $\overline{RTS}$-$\overline{CTS}$ turn-on time

Received Line Signal Detector ($\overline{RLSD}$)

For V.27 bis/ter RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ±10 ms. The RLSD on-to-off response time for V.27 is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on the threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:

1. Greater than −43 dBm (RLSD on)
   Less than −49 dBm (RLSD off)
2. Greater than −33 dBm (RLSD on)
   Less than −38 dBm (RLSD off)
3. Greater than −26 dBm (RLSD on)
   Less than −31 dBm (RLSD off)
4. Greater than −16 dBm (RLSD on)
   Less than −21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with an unmodulated 2400 Hz tone applied to the receiver's audio input (RXA).

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 4800 or 2400 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

TDCLK is provided to the user in synchronous communications for USRT timing. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{RDCLK}$)

The modem provides a Receive Data Clock ($\overline{RDCLK}$) output in the form of a 50 ±1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. $\overline{RDCLK}$ is provided to the user in synchronous communications for USRT timing. The timing recovery circuit is capable of tracking a ±.01% frequency error in the associated transmit timing source.

MICROPROCESSOR INTERFACE

Eight hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{CS0}$-$\overline{CS2}$) and Register Selects (RS0-RS3)

The signal processor to be accessed is selected by grounding one of three unique chip select lines, $\overline{CS2}$, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable (READ) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ line high or the $\overline{WRITE}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

ANALOG SIGNALS

The analog signal characteristics are described in Table 7.

Table 7. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is 604 ohms ±1%.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is the TLVL setting +0.6 dB −1.4 dB.

Transmitter Analog (TXA)

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the public switched telephone network. The output structure of TXA is a low impedance amplifier in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

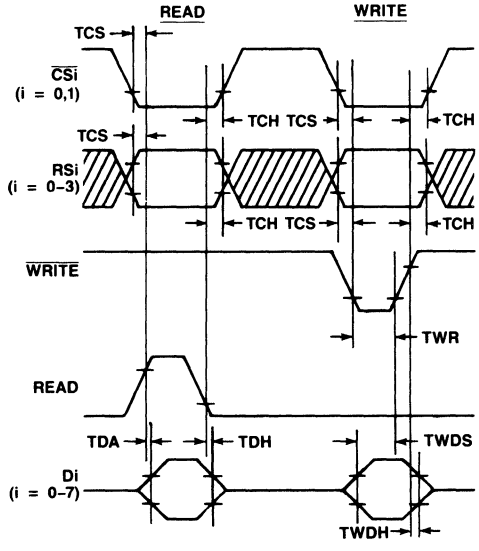
Receiver Analog (RXA)

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source. A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may take the form of back-to-back zener diodes across the transformer or a varistor across the transformer.

Auxiliary Input (AUXIN)

AUXIN provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit at a rate of 9600 samples-per-second. Any signal above 4800 Hz on the AUXIN line will be aliased back into the passband as noise. One application for AUXIN is to inject dual-tone multifrequency (DTMF) touch-tone signals for dialing, however, the source of these tones must be well filtered to eliminate components above 4800 Hz. The input impedance of AUXIN is 1K ohm. The gain from AUXIN to TXA is the same as the selected transmit level +0.6 dB −1.4 dB.



Characteristic	Symbol	Min	Max	Units
CSi, RSi setup time prior to Read or Write	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
CSi, RSi hold time after Read or Write	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram

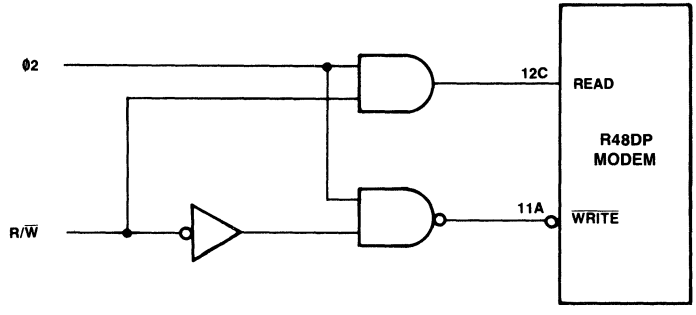


Figure 3. R/W to READ WRITE Conversion Logic

DIAGNOSTIC SIGNALS
EYEX, EYEY, $\overline{\text{EYECLK}}$, and EYESYNC

Four card edge connections provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances as well as defects in the modulation/demodulation process.

The outputs EYEX and EYEY provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. Since this data is in serial digital form it must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two D/A converters. A clock for use by the serial-to-parallel converters is furnished by signal $\overline{\text{EYECLK}}$. A strobe for loading the D/A converters is furnished by signal EYESYNC. Timing of these signals is illustrated in Figure 4. The EYEX and EYEY outputs furnish 9-bit serial words. Since most serial to parallel conversion logic is designed for 8-bit words, an extra storage flip-flop is required for 9-bit resolution. However, the ninth bit is not generally needed for eyepattern generation, and eight-bit hardware can be used if data is copied on the rising edge of $\overline{\text{EYECLK}}$ rather than the falling edge.

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Two clock signals called TBCLK and RBCLK are provided at the modem connector. These signals have no counterpart in the V.24 or RS-232 recommendations since they mark the baud interval for the transmitter and receiver rather than the data rate. The baud clocks can be useful in identifying the order of data bits in a baud (e.g., for multiplexing data, etc.). Both signals are high active, meaning the baud boundaries occur on falling edges. The first bit in each baud begins with the falling edge of the corresponding baud clock.

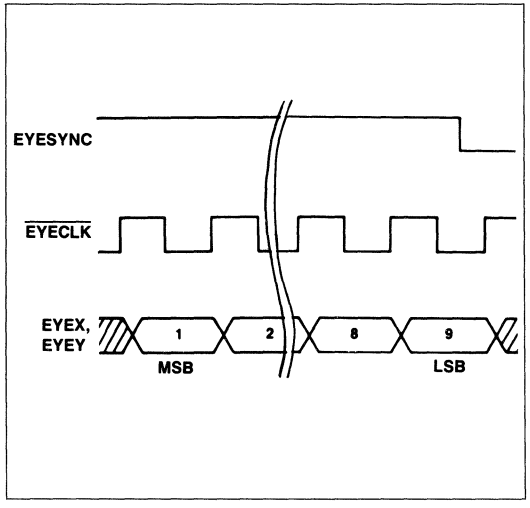


Figure 4. Eye Pattern Timing

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on three special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into areas. These areas are partitioned into transmitter, baud rate, and sample rate devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 48 addressable registers in the modem are shown in Figure 5. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Table 8 defines the individual bits in the interface memory. In the Table 8 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	X	X	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	—	—	—	—	—	—	—	—
0	TRANSMITTER DATA, DDR							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RSIA	—	—	—	RSB	RSIE	—	RSDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	—	—	—	—
8	—	—	—	—	—	$\overline{P2DET}$	—	—
7	RTH		DDIS	RPDM	SWRT	BWRT	T2	RTDIS
6	IFIX	TOD	RECEIVER CONFIGURATION					
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL, RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 5. Interface Memory Map

Table 8. R48DP Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
A3L	Amplitude 3-Link Select	0:5:1	A3L is used in conjunction with LAEN. When A3L is a one the Japanese 3 link equalizer is selected and when A3L is a zero the U.S. Survey Long link equalizer is selected.
BWRT	Baud Write	1:7:2	When control bit BWRT is a one, the RAM write operation is enabled for Chip 2.
CEQ	Cable Equalizer Field	0:5:4,5	The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following tables list the possible cable equalizer selection codes and responses.
$\overline{\text{CDET}}$	Carrier Detector	1:B:0	When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$. If the $\overline{\text{FED}}$ bit goes to a zero and no P2 sequence is detected, the $\overline{\text{CDET}}$ bit goes to zero within 5 to 25 ms indicating that the receiver has entered the data state without a training sequence.
DDIS	Descramble Disable	1:7:5	When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.
DDR	Dial Digit Register	0:0:0–7	DDR is used to tell the modem which DTMF digit to transmit (see Transmitter Data).
D3L	Delay 3-Link Select	0:5:0	D3L is used in conjunction with LDEN. When D3L is a one the Japanese 3 link equalizer is selected and when D3L is a zero the U.S Survey Long link equalizer is selected

CEQ	Cable Length (0.4 mm diameter)
0	0.0
1	1.8 km
2	3.6 km
3	7.2 km

Cable Equalizer Nominal Gain

CEQ CODE 1

Frequency (Hz)	Gain Relative to 1700 Hz (dB)	
	Transmitter	Receiver
700	−0.99	−0.94
1500	−0.20	−0.24
2000	+0.15	+0.31
3000	+1.43	+1.49

CEQ CODE 2

Frequency (Hz)	Gain Relative to 1700 Hz (dB)	
	Transmitter	Receiver
700	−2.39	−2.67
1500	−0.65	−0.74
2000	+0.87	+1.02
3000	+3.06	+3.17

CEQ CODE 3

Frequency (Hz)	Gain Relative to 1700 Hz (dB)	
	Transmitter	Receiver
700	−3.93	−3.98
1500	−1.22	−1.20
2000	+1.90	+1.81
3000	+4.58	+4.38

Unless a problem with training or high bit error rate is encountered, most applications operate successfully with no cable equalizer selected.

Table 8. R48DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>EPT</td><td>Echo Protector Tone</td><td>0:7:3</td><td>When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission</td></tr>
<tr><td>$\overline{\text{FED}}$</td><td>Fast Energy Detector</td><td>1:9:6</td><td>When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband, and the receiver is searching for the training sequence.</td></tr>
<tr><td>(None)</td><td>FREQL/FREQM</td><td>0:2:0–7,
0:3:0–7</td><td>The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below:

FREQM Register (0:3)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{15}</td><td>2^{14}</td><td>2^{13}</td><td>2^{12}</td><td>2^{11}</td><td>2^{10}</td><td>2^{9}</td><td>2^{8}</td></tr></table>
FREQL Register (0:2)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{7}</td><td>2^{6}</td><td>2^{5}</td><td>2^{4}</td><td>2^{3}</td><td>2^{2}</td><td>2^{1}</td><td>2^{0}</td></tr></table>
The frequency number (N) determines the frequency (F) as follows:
F = (0.146486) (N) Hz ±0.01%

Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below:
<table><tr><th>FREQM</th><th>FREQL</th><th>Frequency (Hz)</th></tr><tr><td>0C</td><td>52</td><td>462</td></tr><tr><td>1D</td><td>55</td><td>1100</td></tr><tr><td>2C</td><td>00</td><td>1650</td></tr><tr><td>31</td><td>55</td><td>1850</td></tr><tr><td>38</td><td>00</td><td>2100</td></tr></table></td></tr>
<tr><td>IFIX</td><td>Eye Fix</td><td>1:6:7</td><td>When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB.</td></tr>
<tr><td>LAEN</td><td>Link Amplitude Equalizer Enable</td><td>0:5:3</td><td>The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table:
<table><tr><th>LAEN</th><th>A3L</th><th>Curve Matched</th></tr><tr><td>0</td><td>X</td><td>No Equalizer</td></tr><tr><td>1</td><td>0</td><td>U.S. Survey Long</td></tr><tr><td>1</td><td>1</td><td>Japanese 3-Link</td></tr></table>
The link amplitude equalizer responses are given in the following table.

Link Amplitude Equalizer
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr><tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr><tr><td>1000</td><td>−0.27</td><td>−0.13</td></tr><tr><td>1400</td><td>−0.16</td><td>−0.08</td></tr><tr><td>2000</td><td>+0.33</td><td>+0.16</td></tr><tr><td>2400</td><td>+1.54</td><td>+0.73</td></tr><tr><td>2800</td><td>+5.98</td><td>+2.61</td></tr><tr><td>3000</td><td>+8.65</td><td>+3.43</td></tr></table></td></tr>
</table>

Table 8. R48DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>LCEN</td><td>Loop Clock Enable</td><td>0:4:0</td><td>When control bit LCEN is a one, the transmitter clock tracks the receiver clock.</td></tr>
<tr><td>LDEN</td><td>Link Delay Equalizer Enable</td><td>0:5:2</td><td>The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table:

<table>
<tr><th>LDEN</th><th>D3L</th><th>Curve Matched</th></tr>
<tr><td>0</td><td>X</td><td>No Equalizer</td></tr>
<tr><td>1</td><td>0</td><td>U.S. Survey Long</td></tr>
<tr><td>1</td><td>1</td><td>Japanese 3-Link</td></tr>
</table>
The link delay equalizer responses are given in the following table.

Link Delay Equalizer
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Delay Relative to 1700 Hz (Microseconds)</th></tr>
<tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr>
<tr><td>800</td><td>−498.1</td><td>−653.1</td></tr>
<tr><td>1200</td><td>−188.3</td><td>−398.5</td></tr>
<tr><td>1600</td><td>−15.1</td><td>−30.0</td></tr>
<tr><td>1700</td><td>+0.0</td><td>+0.0</td></tr>
<tr><td>2000</td><td>−39.8</td><td>+11.7</td></tr>
<tr><td>2400</td><td>−423.1</td><td>−117.1</td></tr>
<tr><td>2800</td><td>−672.4</td><td>−546.3</td></tr>
</table></td></tr>
<tr><td>L2ACT</td><td>Remote Digital Loopback Activate</td><td>0:4:1</td><td>When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2.</td></tr>
<tr><td>L3ACT</td><td>Local Analog Loopback Activate</td><td>0:4:7</td><td>When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.</td></tr>
<tr><td>L4ACT</td><td>Remote Analog Loopback Activate</td><td>0:4:6</td><td>When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4.</td></tr>
<tr><td>L4HG</td><td>Loop 4 High Gain</td><td>0:4:5</td><td>When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.</td></tr>
<tr><td>MHLD</td><td>Mark Hold</td><td>0:7:4</td><td>When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).</td></tr>
<tr><td>$\overline{\text{PNDET}}$</td><td>Period N Detector</td><td>1:B:6</td><td>When status bit $\overline{\text{PNDET}}$ is a zero, it indicates a PN sequence has been detected. This bit sets to a one at the end of the PN sequence.</td></tr>
<tr><td>$\overline{\text{P2DET}}$</td><td>Period Two Detector</td><td>1:8:2</td><td>When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a P2 sequence has been detected. This bit sets to a one at the start of the PN sequence.</td></tr>
<tr><td>(None)</td><td>RAM Access XB</td><td>2:5:0–7</td><td>Contains the RAM access code used in reading or writing chip 2 RAM locations via word X (2:3 and 2:2).</td></tr>
<tr><td>(None)</td><td>RAM Access XS</td><td>1:5:0–7</td><td>Contains the RAM access code used in reading or writing chip 1 RAM locations via word X (1:3 and 1:2).</td></tr>
<tr><td>(None)</td><td>RAM Access YB</td><td>2:4:0–7</td><td>Contains the RAM access code used in reading or writing chip 2 RAM locations via word Y (2:1 and 2:0).</td></tr>
</table>

Table 8. R48DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Access YS	1 4 0–7	Contains the RAM access code used in reading or writing chip 1 RAM locations via word Y (1 1 and 1·0)
(None)	RAM Data XBL	2 2 0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 2
(None)	RAM Data XBM	2:3·0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 2.
(None)	RAM Data XSL	1:2:0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 1.
(None)	RAM Data XSM	1 3:0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 1
(None)	RAM Data YBL	2:0 0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YBM	2:1 0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YSL	1·0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus See 'Receiver Data '
(None)	RAM Data YSM	1 1:0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1
RBDA	Receiver Baud Data Available	2 E:0	Status bit RBDA goes to a one when the receiver writes data into register 2·0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2·E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low. In idle mode the interrupts from chip 2 occur at half the baud rate During diagnostic access in data mode, the interrupts occur at the baud rate.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
(None)	Receiver Configuration	1·6:0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB) *Receiver Configuration Control Codes* Control codes for the modem receiver configuration are· **Configuration Code (Hex) — Receiver Configuration** 22 — V.27 4800 Long 21 — V 27 2400 Long 02 — V.27 4800 Short 01 — V.27 2400 Short

Table 8. R48DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	Receiver Data	1:0:0–7	The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data When using receiver parallel data mode, the registers 1:3 through 1:0 can not be used for reading the chip 1 RAM.
RPDM	Receiver Parallel Data Mode	1·7:4	When control bit RPDM is a one, the receiver supplies channel data to the receiver data register (1:0) as well as to the hardware serial data output. (See Receiver Data)
RSB	Receiver Setup Bit	1:E:3	When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective. Worst case setup time is 2 baud times.
RSDA	Receiver Sample Data Available	1:E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0 RSDA goes to a zero when the host processor reads data from register 1:0.
RSIA	Receiver Sample Interrupt Active	1:E:7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is a one.
RTDIS	Receiver Training Disable	1:7:0	When control bit RTDIS is a one, the receiver is prevented from recognizing a training sequence and entering the training state.
RTH	Receiver Threshold Field	1:7·6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH** / **RLSD On** / **RLSD Off** 0 / > –43 dBm / < –48 dBm 1 / > –33 dBm / < –38 dBm 2 / > –26 dBm / < –31 dBm 3 / > –16 dBm / < –21 dBm
RTS	Request-to-Send	0:7:7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input. These inputs are ORed by the modem.
SDIS	Scrambler Disable	0:7:5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7:0	When control bit SEPT is a one, the echo protector tone is 30 ms long rather than 185 ms.
SWRT	Sample Write	1·7:3	When control bit SWRT is a one, the RAM write operation is enabled for chip 1.
TBA	Transmitter Buffer Available	0:E:0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one. During a RAM access in chip 0, when TBA is a one the host can perform either a RAM read or write depending on the state of bit 0:6:3 (see Transmitter Configuration).
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.
TIE	Transmitter Interrupt Enable	0:E:2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.

Table 8. R48DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TLVL	Transmitter Level Field	0·4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL** — **Transmitter Analog Output*** 0 — −1 dBm ±1 dB 1 — −3 dBm ±1 dB 2 — −5 dBm ±1 dB 3 — −7 dBm ±1 dB 4 — −9 dBm ±1 dB 5 — −11 dBm ±1 dB 6 — −13 dBm ±1 dB 7 — −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-on-Data	1:6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-date.
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0·0) When TPDM is a zero channel data from the serial hardware input TXD is accepted.
(None)	Transmtter Configuration*	0:6·0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB.) *Transmitter Configuration Control Codes* Control codes for the modem transmitter configurations are: **Configuration Code (Hex)** — **Transmitter Configuration** 22 — V.27 4800 Long 21 — V.27 2400 Long 02 — V.27 4800 Short 01 — V.27 2400 Short 80 — Tone Transmit **Configuration Definitions** Definitions of the eight Transmitter Configurations are: 1. V.27. When a V.27 configuration has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 2. Tone Transmit. In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by two registers in the host interface memory space containing the frequency code The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%.

Table 8. R48DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter, DDR</td><td>0:0:0–7</td><td>The host processor transmits data in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

NOTE

Data is transmitted bit zero first.

<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table>
</td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective. Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>T2</td><td>T/2 Equalizer Select</td><td>1:7:1</td><td>When control bit T2 is a one, an adaptive equalizer with two taps per baud is used. When T2 is a zero, the equalizer has one tap per baud. The total number of taps remains the same for both cases.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a zero, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A. The clock appearing at the XTCLK input will appear at the TDCLK output.</td></tr>
</table>

SIGNAL PROCESSOR RAM ACCESS

RAM and Data Organization

Each signal processor contains 128 words of random access memory (RAM). Each word is 32 bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16 bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. In the sample rate and baud rate devices the entire contents of XRAM and YRAM may be read from or written into by the host processor via the microprocessor interface. No access to the RAM is possible in the transmitter device.

Interface Memory

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit determines the RAM address to read from or write into by the code stored in the RAM ACCESS bits of interface memory registers. The SP logic unit normally transfers a word from RAM to interface memory once each cycle of the device code. Each RAM word transferred to the interface memory is 32 bits long. These bits are written by the SP logic unit into interface memory registers 3, 2, 1, and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data, respectively. As previously described for parallel data mode, the data available bits set to a one when register 0 of the respective signal processor is written into by the device and resets to a zero when register 0 is read from by the host. Since the parallel data mode receiver data register shares register 0 with the YRAM data, chip 1 RAM access are disabled in parallel data mode. However, chip 2 RAM access remains active in receiver parallel data mode.

The sample rate device and the baud rate device allow data to be transferred from interface memory to RAM. When set to a one, bit SWRT (1:7:3) signals the chip 1 SP logic unit to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. Bit BWRT (1:7:2) performs the same function for chip 2 RAM. When writing into the RAM, 32 bits are transferred. The 16 bits written into XRAM come from registers 3 and 2, with register 3 being the more significant byte. The 16 bits written into YRAM come from registers 1 and 0, with register 1 being the more significant byte. When only 16 bits of data are to be written, FF (a dummy RAM location) must be stored in RAM ACCESS XS or RAM ACCESS YS to prevent writing the insignificant 16 bits of registers 1:3 through 1:0 into a valid RAM location. When the host processor writes into register 1:0 the RSDA bit (1:E:0) is reset to zero. When the SP logic unit reads data from register 1:0, the RSDA bit (1:E:0) is set to a one. In a similar manner, bit RBDA (2:E:0) resets to zero when the host processor writes into register 2:0 and sets to a one when the SP logic unit reads data from register 2:0.

When reading from RAM, or writing into RAM, the bits in registers 1:E and 2:E can be used for handshaking or interrupt functions as in parallel data mode. When not in parallel data mode, the bits in register 1:E perform the handshake and interrupt functions for RAM access. In both serial and parallel data modes, the bits in register 2:E perform handshake and interrupt functions for RAM access. When set to one, bit RBIE (2:E:2) enables RBDA to drive the IRQ connector signal to zero volts when RBDA is a one. Bit RBIA (2:E:7) identifies chip 2, the baud rate device, as a source of IRQ interrupt. Bit RBIA is a one when both RBIE and RBDA are set to one. In the event that other system elements may cause IRQ to be driven low, the host must determine if modem chip 2 is causing an interrupt by reading RBIA.

Table 9 provides the available RAM access functions, codes, and registers.

Table 9. RAM Access Codes

No.	Function	Chip	X Access Code (Hex)	Y Access Code (Hex)	Register
1	Received Signal Samples	1	C0	Not Used	2,3
2	Demodulator Output	1	C2	42	0,1,2,3
3	Low Pass Filter Output	1	D4	54	0,1,2,3
4	Average Energy	1	DC	Not Used	2,3
5	AGC Gain Word	1	81	Not Used	2,3
6	Equalizer Input	2	C0	40	0,1,2,3
7	Equalizer Tap Coefficients	2	81 – A0	01 – 20	0,1,2,3
8	Unrotated Equalizer Output	2	E1	61	0,1,2,3
9	Rotated Equalizer Output (Received Points)	2	A2	22	0,1,2,3
10	Decision Points Ideal Points	2	62	0,1,2,3	
11	Error	2	E3	63	0,1,2,3
12	Rotation Angle	2	Not Used	00	0,1
13	Frequency Correction	2	AA	Not Used	2,3
14	EQM	2	A7	Not Used	2,3
15	Dual Point	2	AE	2E	0,1,2,3

PERFORMANCE

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

Typical BER performance is shown in Figure 6. Figure 7 shows a typical test setup to measure BER.

TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

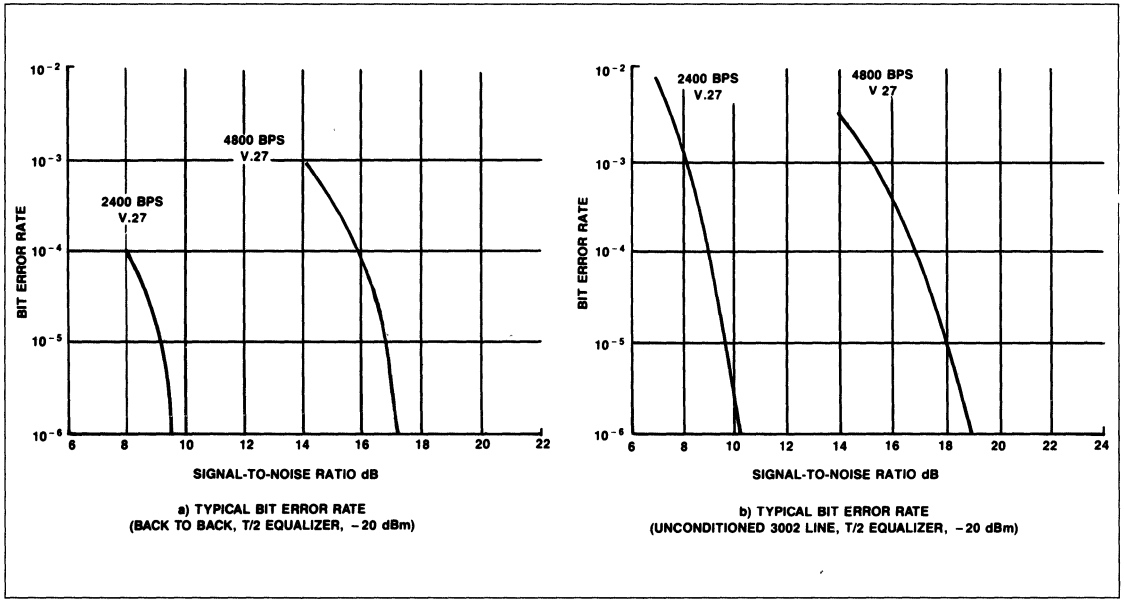


Figure 6. R48DP BER versus SNR

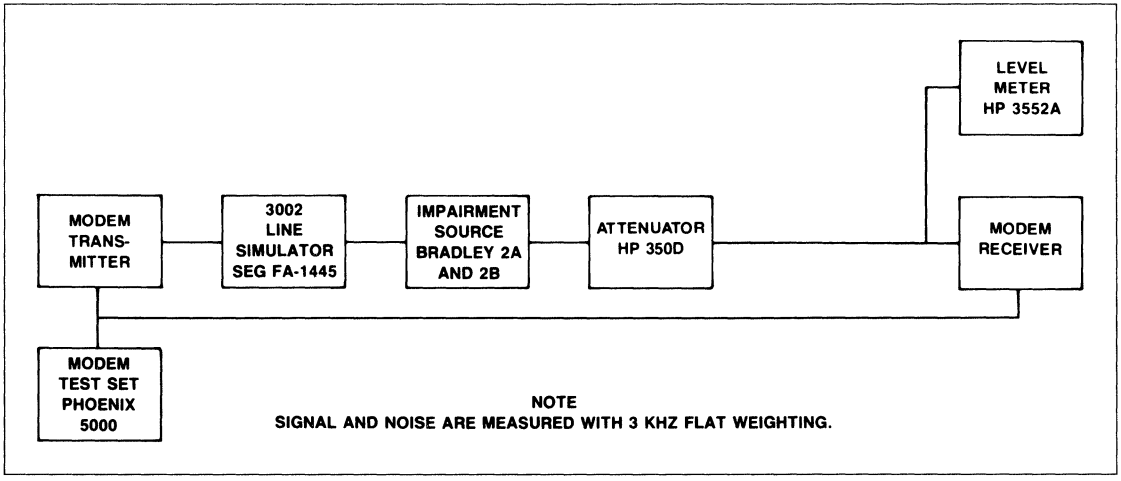


Figure 7. BER Performance Test Set-up

GENERAL SPECIFICATIONS

Table 10. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	550 mA	<700 mA
+12 Vdc	±5%	5 mA	< 10 mA
-12 Vdc	±5%	25 mA	< 50 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Table 11. Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	-40°C to +80°C (-40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	-200 feet to +10,000 feet

Table 12. Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Connector Height	0.437 in. (11.1 mm)
Component Height	
Top (max.)	0.200 in. (5.1 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max):	3.6 oz. (100 g)
Lead Extrusion (max.):	0.100 in (2.54 mm)
DIP Connector Version	
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.228 in. (82 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0.200 in. (5.1 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.53 in. (13.5 mm)

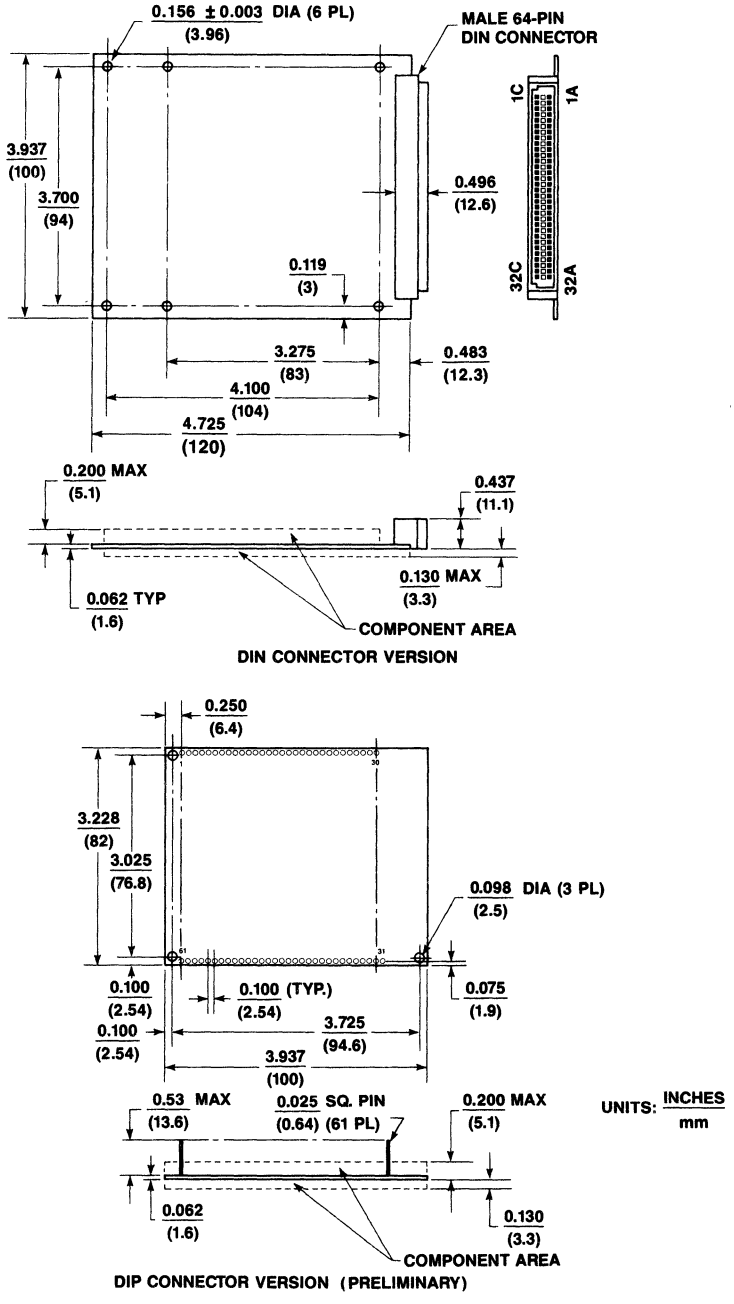


Figure 8. R48DP Modem Dimensions and Pin Locations

Rockwell

R96DP
9600 bps Data Pump Modem

INTRODUCTION

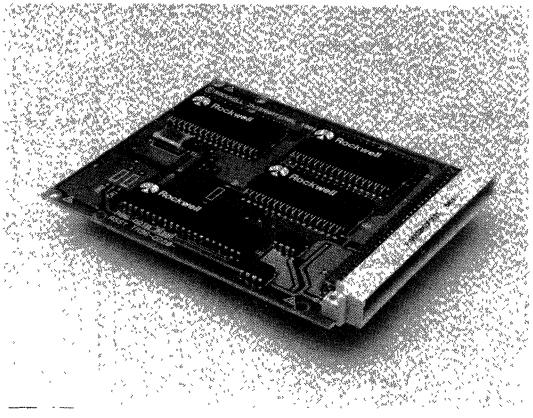
The Rockwell R96DP is a synchronous 9600 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) as well as leased lines through the appropriate line termination.

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29 and V.27 bis/ter. The R96DP can operate at speeds of 9600, 7200, 4800, and 2400 bps. Employing advanced signal processing techniques, the R96DP can transmit and receive data even under extremely poor line conditions.

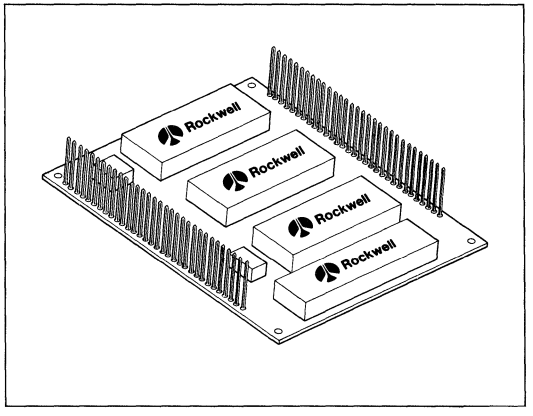
The R96DP is designed for use in point-to-point environments. User programmable features allow the modem operation to be tailored to support a wide variety of functional requirements. The modem's small size, low power consumption, and serial/parallel host interface simplify system design and allow installation in a compact enclosure. The modem module is available with a DIN connector for connection to a mating connector or with dual-in-line pins (DIP) for direct plug-in installation onto a host module.

FEATURES

- CCITT V.29, V.27 bis/ter Compatible
- Point-to-Point Applications
- 2-Wire Half-Duplex, 4-Wire Full-Duplex
- Programmable Tone Generation
- Programmable DTMF Tone Dialer
- Dynamic Range: – 43 dBm to 0 dBm
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C)(Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Diagnostic Capability
- Programmable Transmit Output Level
- Loopbacks
  - — Local and Remote Analog
  - — Remote Digital
- Small Size
  - — DIN Connector Version: 100 mm x 120 mm (3.94 in. x 4.73 in.)
  - — DIP Connector Version: 82 mm x 100 mm (3.23 in. x 3.94 in.)
- Power Consumption: 3 W (Typical)



R96DP DIN Connector Version



R96DP DIP Connector Version

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

The transmitter carrier frequencies supported by the R96DP are listed in Table 1.

Table 1. Transmitter Carrier Frequencies

Function	Frequency (Hz ±0.01%)
V 27 bis/ter Carrier	1800
V 29 Carrier	1700

TONE GENERATION

Under control of the host processor, the R96DP can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated. DTMF tone transmission capability is provided to allow the modem to operate as a programmable DTMF tone dialer.

SIGNALING AND DATA RATES

The signaling and data rates supported by the R96DP are listed in Table 2.

Table 2. Signaling/Data Rates

Specification	Baud Rate (Symbols/sec.)	Bits Per Baud	Data Rate (bps)(±0.01%)	Symbol Points
V.29	2400	4	9600	16
V.29	2400	3	7200	8
V.29	2400	2	4800	4
V.27	1600	3	4800	8
V.27	1200	2	2400	4

DATA ENCODING

The R96DP data encoding conforms to CCITT recommendations V.29 and V.27 bis/ter.

EQUALIZERS

The R96DP provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent
2. *1600 Baud.* Square root of 50 percent
3. *2400 Baud.* Square root of 20 percent

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96DP incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 bis/ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96DP can adapt to received frequency error of up to ± 10 Hz with less than 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from 0 dBm to – 43 dBm. The received line signal level is measured at the receiver analog input (RXA).

TRANSMIT LEVEL

The transmitter output level is accurate to ± 1.0 dB and is programmable from – 1.0 dBm to – 15.0 dBm in 2 dB steps.

TRAIN ON DATA

When train on data is enabled, the receiver typically trains on data in less than 15 seconds for V.29 and 3.5 seconds for V.27.

TURN-ON SEQUENCE

Selectable turn-on sequences can be generated as defined in Table 3.

Table 3. Turn-On Sequences

Specification	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector* Tone Enabled
V.29 (All data rates)	253 ms	438 ms
V.27 4800 bps long	708 ms	913 ms
V.27 4800 bps short	50 ms	255 ms
V.27 2400 bps long	943 ms	1148 ms
V.27 2400 bps short	67 ms	272 ms

* For short echo protector tone, subtract 155 ms from $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ turn-on time.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) whenever the Received Line Signal Detector (RLSD) is off.

MODEM OPERATION

Because the modem is implemented in firmware executed by a specialized computer (the signal processor), operation can best be understood by dividing this section into hardware circuits and software circuits. Hardware circuits include all pins on the modem connector. Software circuits include configuration, control (soft strapping), status, and RAM access routines.

HARDWARE CIRCUITS

The functional interconnect diagram (Figure 1) shows the modem connected into a system. In this diagram, any point that is active when exhibiting the relatively more negative voltage of a two voltage system (e.g., 0 Vdc for TTL or −12 Vdc for RS-232-C) is called low active and is represented by association with a small circle at the signal point. The particular voltage levels used to represent the binary states do not change the logic symbol. Two types of I/O points that may cause confusion are edge-triggered inputs and open-collector (open-source or open-drain) outputs. These signal points include the additional notation of a small triangle or a small half-circle (see signal IRQ), respectively. Active low signals are named with an overscore (e.g., $\overline{\text{POR}}$). In deciding whether a clock output is high active or low active, the convention followed is to assume that the clocking (activating) edge appropriate to the host hardware is a transition from the clocks active to its inactive state (i.e., a trailing edge trigger). A clock intended to activate logic on its rising edge is called low active while a clock intended to activate logic on its falling edge is called high active. When a clock input is associated with a small circle, the input activates on a falling edge. If no circle is shown, the input activates on a rising edge.

The interconnect signals on Figure 1 are organized into six groups of modem operation: overhead signals, V.24 interface signals, microprocessor interface signals, diagnostic signals, analog signals, and ancillary signals. Table 4 lists these groups along with their corresponding connector pin numbers. The six groups of hardware circuits are described in the following paragraphs. Table 5 lists the digital interface characteristics.

POWER-ON RESET

Basic modem operation can be understood most easily by beginning with the modem configured to default conditions. When the modem is initially energized a signal called Power-On-Reset ($\overline{\text{POR}}$) causes the modem to assume a valid operational state. The modem drives pin 13C to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 13C, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 13C low for at least 3 μs. When an external low input is applied to pin 13C, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 13C is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The R96DP POR sequence leaves the modem configured as follows:

- 9600 bps
- Serial channel data
- T/2 equalizer
- Standard echo protector tone
- −43 dBm threshold
- Cable and link equalizers disabled
- Train-On-Data disabled

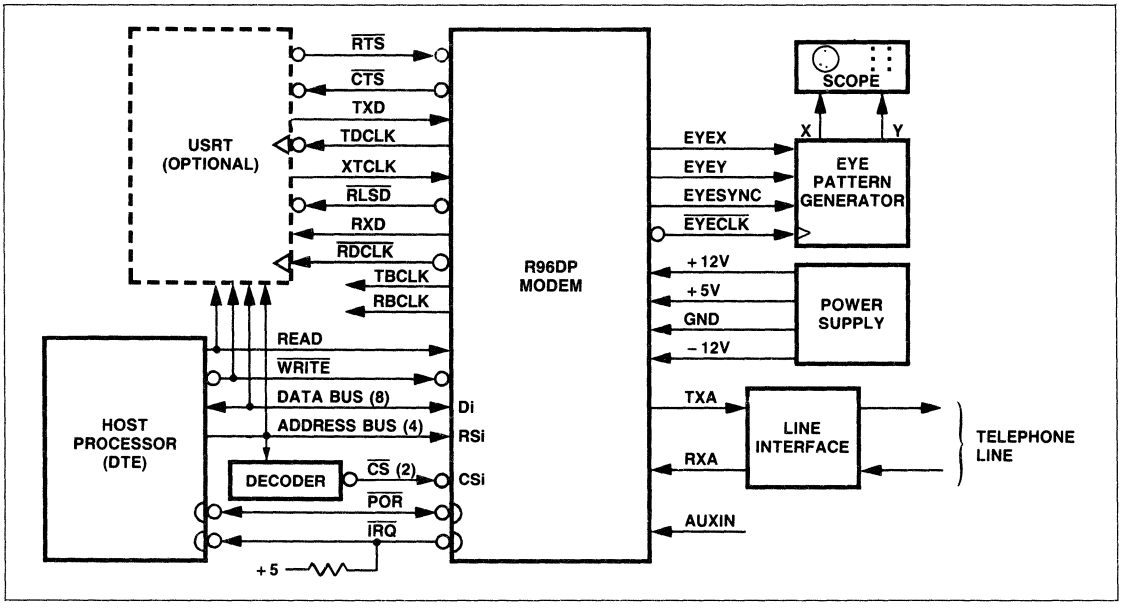


Figure 1. R96DP Functional Interconnect Diagram

DIAGNOSTIC SIGNALS
EYEX, EYEY, EYECLK, and EYESYNC

Four card edge connections provide the timing and data necessary to create an oscilloscope quadrature eye pattern. The eye pattern is simply a display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances as well as defects in the modulation/demodulation process.

The outputs EYEX and EYEY provide two serial bit streams containing data for display on the oscilloscope X axis and Y axis, respectively. Since this data is in serial digital form it must first be converted to parallel digital form by two serial-to-parallel converters and then to analog form by two D/A converters. A clock for use by the serial-to-parallel converters is furnished by signal EYECLK. A strobe for loading the D/A converters is furnished by signal EYESYNC. Timing of these signals is illustrated in Figure 4. The EYEX and EYEY outputs furnish 9-bit serial words. Since most serial to parallel conversion logic is designed for 8-bit words, an extra storage flip-flop is required for 9-bit resolution. However, the ninth bit is not generally needed for eyepattern generation, and eight-bit hardware can be used if data is copied on the rising edge of EYECLK rather than the falling edge.

ANCILLARY SIGNALS

Transmitter Baud Clock (TBCLK) and Receiver Baud Clock (RBCLK)

Two clock signals called TBCLK and RBCLK are provided at the modem connector. These signals have no counterpart in the V.24 or RS-232 recommendations since they mark the baud interval for the transmitter and receiver rather than the data rate. The baud clocks can be useful in identifying the order of data bits in a baud (e.g., for multiplexing data, etc.). Both signals are high active, meaning the baud boundaries occur on falling edges. The first bit in each baud begins with the falling edge of the corresponding baud clock.

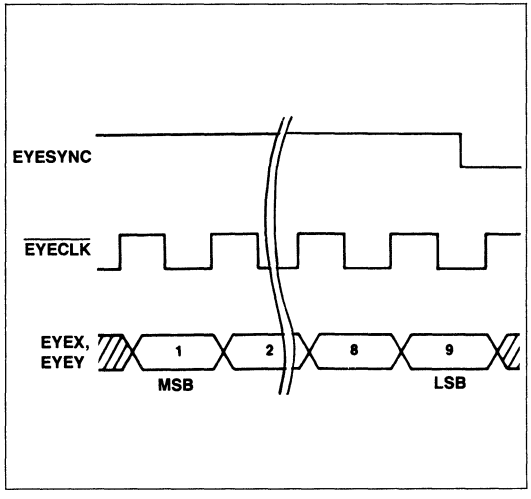


Figure 4. Eye Pattern Timing

SOFTWARE CIRCUITS

Operation of the microprocessor interface circuits was described in the hardware section from the standpoint of timing and load/drive characteristics. In this section, operation of the microprocessor interface is described from a software standpoint.

The modem is implemented in firmware running on three special purpose signal processors. These signal processors share the computing load by performing tasks that are divided into areas. These areas are partitioned into transmitter, baud rate, and sample rate devices.

INTERFACE MEMORY

Each signal processor can communicate with the host processor by means of a specialized, dual-port, scratch-pad memory called interface memory. A set of sixteen 8-bit registers, labeled register 0 through register F, can be read from or written into by either the host processor or signal processor. The host communicates via the microprocessor interface lines shared between the two signal processors. The signal processor communicates via its internal I/O bus. Information transfer from SP RAM to interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. Two of the 16 addressable interface memory registers (i.e., register 0 and register E) have unique hardware connections to the interrupt logic. It is possible to enable a bit in register E to cause an interrupt each time it sets. This interrupt can then be cleared by a read or write cycle from the host processor to register 0. This operation is discussed in detail later in this section.

Memory maps of the 48 addressable registers in the modem are shown in Figure 5. These registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Table 8 defines the individual bits in the interface memory. In the Table 8 descriptions, bits in the interface memory are referred to using the format Y:Z:Q. The chip number is specified by Y (0 or 1), the register number by Z (0 through F), and the bit number by Q (0 through 7, with 0 = LSB).

Table 4. R96DP Hardware Circuits

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Description
A. OVERHEAD:				
Ground (A)	AGND	31C,32C	30,31	Analog Ground Return
Ground (D)	DGND	3C,8C, 5A,10A	29,37,53	Digital Ground Return
+5 volts	PWR	19C,23C, 26C,30C	1,45,61	+5 volt supply
+12 volts	PWR	15A	32	+12 volt supply
−12 volts	PWR	12A	36	−12 volt supply
$\overline{POR}$	I/OB	13C	2	Power-on-reset
B. MICROPROCESSOR INTERFACE:				
D7	I/OA	1C	3	Data Bus (8 Bits)
D6	I/OA	1A	4	
D5	I/OA	2C	5	
D4	I/OA	2A	6	
D3	I/OA	3A	7	
D2	I/OA	4C	8	
D1	I/OA	4A	9	
D0	I/OA	5C	10	
RS3	IA	6C	16	Register Select (4 Bits)
RS2	IA	6A	17	
RS1	IA	7C	18	
RS0	IA	7A	19	
$\overline{CS0}$	IA	10C	20	Chip Select Transmitter Device
$\overline{CS1}$	IA	9C	21	Chip Select Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	13	Chip Select Receiver Baud Rate Device
$\overline{READ}$	IA	12C	14	Read Enable
$\overline{WRITE}$	IA	11A	12	Write Enable
$\overline{IRQ}$	OB	11C	11	Interrupt Request

Name	Type[1]	DIN Pin No.	DIP[2] Pin No.	Description
C. V.24 INTERFACE:				
$\overline{RDCLK}$	OC	21A	23	Receive Data Clock
TDCLK	OC	23A	46	Transmit Data Clock
XTCLK	IB	22A	51	External Transmit Clock
$\overline{RTS}$	IB	25A	50	Request-to-Send
$\overline{CTS}$	OC	25C	49	Clear-to-Send
TXD	IB	24C	48	Transmitter Data
RXD	OC	22C	26	Receiver Data
$\overline{RLSD}$	OC	24A	27	Received Line Signal Detector
D. ANCILLARY CIRCUITS:				
RBCLK	OC	26A	22	Receiver Baud Clock
TBCLK	OC	27C	47	Transmitter Baud Clock
E. ANALOG SIGNALS:				
TXA	AA	31A	34	Transmitter Analog Output
RXA	AB	32A	33	Receiver Analog Input
AUXIN	AC	30A	—	Auxiliary Analog Input
F. DIAGNOSTIC:				
EYEX	OC	15C	56	Eye Pattern Data—X Axis
EYEY	OC	14A	55	Eye Pattern Data—Y Axis
$\overline{EYECLK}$	OA	14C	57	Eye Pattern Clock
EYESYNC	OA	13A	58	Eye Pattern Synchronizing Signal

Notes:
1. Refer to Table 5 for digital circuit interface characteristics and Table 7 for analog circuit interface characteristics.
2. Pins not used on the DIP Version: 15, 24, 25, 28, 35, 38, 39, 40, 41, 42, 43, 44, 52, 54, 59, 60

Table 5. Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.				2.0 Min.	5.25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max.	0.8 Max.	0.8 Max.				0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.						±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.				
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.		
I_L	Output Current, Leakage	μA					±10 Max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.		−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	3-State Transceiver	Open-Drain w/Pull-up

Notes
1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I Load = 0.36 mA

This configuration is suitable for performing high speed data transfer using the serial data port. Individual features are discussed in subsequent paragraphs.

V.24 INTERFACE

Eight hardware circuits provide timing, data, and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0V, + 5V). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within standalone modem enclosures or equipment cabinets. For driving longer cables, the voltage levels and connector arrangement recommended by EIA standard RS-232-C are preferred.

The sequence of events leading to successful data transfer from transmitter to receiver is:

1. The transmitter is activated and a training sequence is sent.
2. The receiver detects channel energy above the prescribed threshold level and synchronizes its operation to the transmitter.
3. Data transfer proceeds to the end of the message.
4. The transmitter turns off after insuring that all data has had time to be recovered at the receiver output.

Transmitted Data (TXD)

The modem obtains serial data from the local DTE on this input.

Received Data (RXD)

The modem presents received data to the local DTE on this output.

Request To Send ($\overline{RTS}$)

$\overline{RTS}$ ON allows the modem to transmit data on TXD when $\overline{CTS}$ becomes active. The responses to $\overline{RTS}$ are shown in Table 6.

Clear To Send ($\overline{CTS}$)

$\overline{CTS}$ ON indicates to the terminal equipment that the modem will transmit any data which are present on TXD. $\overline{CTS}$ response times from an ON condition of $\overline{RTS}$ are shown in Table 6.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in data state is a maximum of 2 band times for all configurations.

Table 6. $\overline{RTS}$-$\overline{CTS}$ Response Times

Specification	$\overline{RTS}$-$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector* Tone Enabled
V.29 (All data rates)	253 ms	438 ms
V.27 4800 bps long	708 ms	913 ms
V.27 4800 bps short	50 ms	255 ms
V.27 2400 bps long	943 ms	1148 ms
V.27 2400 bps short	67 ms	272 ms

* For short echo protector tone, subtract 155 ms from $\overline{RTS}$-$\overline{CTS}$ turn-on time.

Received Line Signal Detector ($\overline{RLSD}$)

For V.27 bis/ter or V.29, RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 15 ± 10 ms. The RLSD on-to-off response time for V.27 is 10 ± 5 ms and for V.29 is 30 ± 9 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on the threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Four threshold options are provided:

1. Greater than – 43 dBm (RLSD on)
   Less than – 49 dBm (RLSD off)
2. Greater than – 33 dBm (RLSD on)
   Less than – 38 dBm (RLSD off)
3. Greater than – 26 dBm (RLSD on)
   Less than – 31 dBm (RLSD off)
4. Greater than – 16 dBm (RLSD on)
   Less than – 21 dBm (RLSD off)

NOTE

Performance may be at a reduced level when the received signal is less than – 43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold level and hysteresis action are measured with an unmodulated 2400 Hz tone applied to the receiver's audio input (RXA).

Transmit Data Clock (TDCLK)

The modem provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, or 2400 Hz (± 0.01%).
2. *Duty Cycle.* 50 ± 1%.

TDCLK is provided to the user in synchronous communications for USRT timing. In this case Transmit Data (TXD) must be stable during the one μs periods immediately preceding and following the rising edge of TDCLK.

External Transmit Clock (XTCLK)

In synchronous communication where the user needs to supply the transmit data clock, the input XTCLK can be used. The clock supplied at XTCLK must exhibit the same characteristics of TDCLK. The XTCLK input is then reflected at TDCLK.

Receive Data Clock ($\overline{RDCLK}$)

The modem provides a Receive Data Clock ($\overline{RDCLK}$) output in the form of a 50 ± 1% duty cycle squarewave. The low-to-high transitions of this output coincide with the center of received data bits. $\overline{RDCLK}$ is provided to the user in synchronous communications for USRT timing. The timing recovery circuit is capable of tracking a ± .01% frequency error in the associated transmit timing source.

MICROPROCESSOR INTERFACE

Eight hardware circuits provide address, data, control, and interrupt signals for implementing a parallel interface compatible with an 8080 microprocessor. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of soft strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in a later section devoted to software circuits. This section describes the operation of the interface from a hardware standpoint.

Chip Select ($\overline{CS0}$-$\overline{CS2}$) and Register Selects (RS0-RS3)

The signal processor to be accessed is selected by grounding one of three unique chip select lines, $\overline{CS2}$, $\overline{CS1}$ or $\overline{CS0}$. The selected chip decodes the four address lines, RS3 through RS0, to select one of sixteen internal registers. The most significant address bit (2^3) is RS3 while the least significant address bit (2^0) is RS0. Once the address bits have been decoded, the selected register can be read from or written into via an 8-bit parallel data bus, D7 through D0. The most significant data bit (2^7) is D7 while the least significant data bit (2^0) is D0.

Read Enable (READ) and Write Enable ($\overline{WRITE}$)

Reading or writing is activated by pulsing either the READ line high or the $\overline{WRITE}$ line low. During a read cycle, data from the selected register is gated onto the data bus by means of three-state drivers. These drivers force the data lines high for a one bit or low for a zero bit. When not being read, the three-state drivers assume their off, high-impedance, state. During a write cycle, data from the data bus is copied into the selected register, with high and low bus levels representing one bits and zero bits, respectively. The timing required for correct read/write cycles is illustrated in Figure 2. Logic necessary to convert the single R/$\overline{W}$ output from a 65XX series microprocessor to the separate READ and $\overline{WRITE}$ signals required by the modem is shown in Figure 3.

Interrupt Request ($\overline{IRQ}$)

The final signal on the microprocessor interface is Interrupt Request ($\overline{IRQ}$). This signal may be connected to the host microprocessor interrupt request input in order to interrupt host program execution for modem service. The use of $\overline{IRQ}$ is optional and the method of software implementation is described in a subsequent section, Software Circuits. The $\overline{IRQ}$ output structure is an open-drain field-effect-transistor (FET). This form of output allows $\overline{IRQ}$ to be connected in parallel to other sources of interrupt. Any of these sources can drive the host interrupt input low, and the interrupt servicing process continues until all interrupts have been cleared and all $\overline{IRQ}$ sources have returned to their high impedance state. Because of the open-drain structure of $\overline{IRQ}$, an external pull-up resistor to +5 volts is required at some point on the $\overline{IRQ}$ line. The resistor value should be small enough to pull the $\overline{IRQ}$ line high when all $\overline{IRQ}$ drivers are off (i.e., it must overcome the leakage currents). The resistor value should be large enough to limit the driver sink current to a level acceptable to each driver. For the case where only the modem $\overline{IRQ}$ driver is used, a resistor value of 5.6K ohms ±20%, 0.25 watt, is sufficient.

ANALOG SIGNALS

The analog signal characteristics are described in Table 7.

Table 7. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is 604 ohms ±1%.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is the TLVL setting +0.6 dB −1.4 dB.

Transmitter Analog (TXA)

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the public switched telephone network. The output structure of TXA is a low impedance amplifier in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

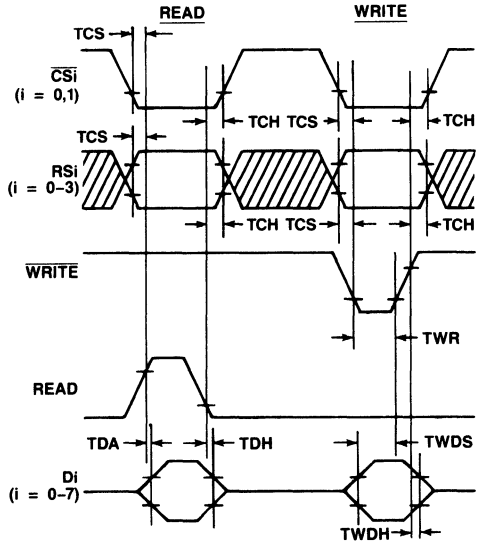
Receiver Analog (RXA)

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source. A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may take the form of back-to-back zener diodes across the transformer or a varistor across the transformer.

Auxiliary Input (AUXIN)

AUXIN provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit at a rate of 9600 samples-per-second. Any signal above 4800 Hz on the AUXIN line will be aliased back into the passband as noise. One application for AUXIN is to inject dual-tone multifrequency (DTMF) touch-tone signals for dialing, however, the source of these tones must be well filtered to eliminate components above 4800 Hz. The input impedance of AUXIN is 1K ohm. The gain from AUXIN to TXA is the same as the selected transmit level +0.6 dB −1.4 dB.



Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	ns
Data access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
$\overline{CSi}$, RSi hold time after Read or $\overline{Write}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Figure 2. Microprocessor Interface Timing Diagram

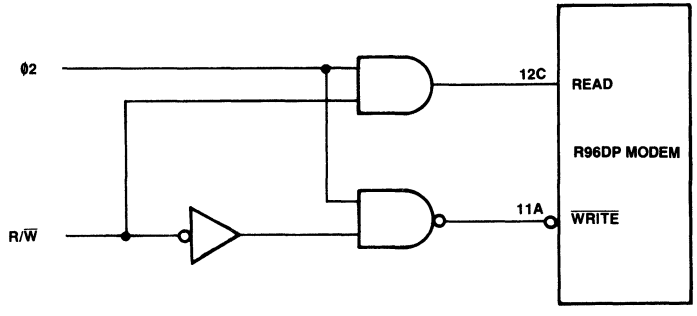


Figure 3. R/$\overline{W}$ to READ $\overline{WRITE}$ Conversion Logic

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS T							
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	—	—	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	RAM DATA YTM							
0	RAM DATA YTL, TRANSMITTER DATA, DDR							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RSIA	—	—	—	RSB	RSIE	—	RSDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	—	—	—	—
8	—	—	—	—	—	$\overline{P2DET}$	—	—
7	RTH		DDIS	RPDM	SWRT	BWRT	T2	RTDIS
6	IFIX	TOD	RECEIVER CONFIGURATION					
5	RAM ACCESS XS							
4	RAM ACCESS YS							
3	RAM DATA XSM							
2	RAM DATA XSL							
1	RAM DATA YSM							
0	RAM DATA YSL; RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS XB							
4	RAM ACCESS YB							
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

(—) Indicates reserved for modem use only.

Figure 5. Interface Memory Map

Table 8. R96DP Interface Memory Definitions

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>A3L</td><td>Amplitude 3-Link Select</td><td>0:5·1</td><td>A3L is used in conjunction with LAEN When A3L is a one the Japanese 3 link equalizer is selected and when A3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
<tr><td>BWRT</td><td>Baud Write</td><td>1:7:2</td><td>When control bit BWRT is a one, the RAM write operation is enabled for Chip 2</td></tr>
<tr><td>CEQ</td><td>Cable Equalizer Field</td><td>0:5·4,5</td><td>The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following tables list the possible cable equalizer selection codes and responses
<table>
<tr><th>CEQ</th><th>Cable Length (0.4 mm diameter)</th></tr>
<tr><td>0</td><td>0.0</td></tr>
<tr><td>1</td><td>1.8 km</td></tr>
<tr><td>2</td><td>3.6 km</td></tr>
<tr><td>3</td><td>7.2 km</td></tr>
</table>
Cable Equalizer Nominal Gain
CEQ CODE 1
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>Transmitter</th><th>Receiver</th></tr>
<tr><td>700</td><td>−0.99</td><td>−0.94</td></tr>
<tr><td>1500</td><td>−0.20</td><td>−0.24</td></tr>
<tr><td>2000</td><td>+0.15</td><td>+0.31</td></tr>
<tr><td>3000</td><td>+1.43</td><td>+1.49</td></tr>
</table>
CEQ CODE 2
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>Transmitter</th><th>Receiver</th></tr>
<tr><td>700</td><td>−2.39</td><td>−2.67</td></tr>
<tr><td>1500</td><td>−0.65</td><td>−0.74</td></tr>
<tr><td>2000</td><td>+0.87</td><td>+1.02</td></tr>
<tr><td>3000</td><td>+3.06</td><td>+3.17</td></tr>
</table>
CEQ CODE 3
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr>
<tr><th>Transmitter</th><th>Receiver</th></tr>
<tr><td>700</td><td>−3.93</td><td>−3.98</td></tr>
<tr><td>1500</td><td>−1.22</td><td>−1.20</td></tr>
<tr><td>2000</td><td>+1.90</td><td>+1.81</td></tr>
<tr><td>3000</td><td>+4.58</td><td>+4.38</td></tr>
</table>
Unless a problem with training or high bit error rate is encountered, most applications operate successfully with no cable equalizer selected.</td></tr>
<tr><td>$\overline{\text{CDET}}$</td><td>Carrier Detector</td><td>1:B·0</td><td>When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$. If the $\overline{\text{FED}}$ bit goes to a zero and no P2 sequence is detected, the $\overline{\text{CDET}}$ bit goes to zero within 5 to 25 ms indicating that the receiver has entered the data state without a training sequence.</td></tr>
<tr><td>DDIS</td><td>Descramble Disable</td><td>1:7:5</td><td>When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.</td></tr>
<tr><td>DDR</td><td>Dial Digit Register</td><td>0·0 0–7</td><td>DDR is used to tell the modem which DTMF digit to transmit (see Transmitter Data)</td></tr>
<tr><td>D3L</td><td>Delay 3-Link Select</td><td>0:5:0</td><td>D3L is used in conjunction with LDEN When D3L is a one the Japanese 3 link equalizer is selected and when D3L is a zero the U.S. Survey Long link equalizer is selected.</td></tr>
</table>

Table 8. R96DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>EPT</td><td>Echo Protector Tone</td><td>0:7:3</td><td>When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission. This option is available in the V.27 and V.29 Configurations, although it is not specified in the CCITT V.29 recommendation.</td></tr>
<tr><td>$\overline{\text{FED}}$</td><td>Fast Energy Detector</td><td>1:9:6</td><td>When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband, and the receiver is searching for the training sequence</td></tr>
<tr><td>(None)</td><td>FREQL/FREQM</td><td>0:2:0–7,
0:3:0–7</td><td>The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below:

FREQM Register (0:3)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{15}</td><td>2^{14}</td><td>2^{13}</td><td>2^{12}</td><td>2^{11}</td><td>2^{10}</td><td>2^{9}</td><td>2^{8}</td></tr></table>
FREQL Register (0:2)
<table><tr><th>Bit:</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr><tr><td>Data Word:</td><td>2^{7}</td><td>2^{6}</td><td>2^{5}</td><td>2^{4}</td><td>2^{3}</td><td>2^{2}</td><td>2^{1}</td><td>2^{0}</td></tr></table>
The frequency number (N) determines the frequency (F) as follows:
F = (0.146486) (N) Hz ±0.01%

Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below:
<table><tr><th>FREQM</th><th>FREQL</th><th>Frequency (Hz)</th></tr><tr><td>0C</td><td>52</td><td>462</td></tr><tr><td>1D</td><td>55</td><td>1100</td></tr><tr><td>2C</td><td>00</td><td>1650</td></tr><tr><td>31</td><td>55</td><td>1850</td></tr><tr><td>38</td><td>00</td><td>2100</td></tr></table></td></tr>
<tr><td>IFIX</td><td>Eye Fix</td><td>1:6:7</td><td>When control bit IFIX is a one, the serial data on EYEX and EYEY reflect the rotated equalizer output and do not follow the data selected by RAM ACCESS XB and RAM ACCESS YB.</td></tr>
<tr><td>LAEN</td><td>Link Amplitude Equalizer Enable</td><td>0:5:3</td><td>The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table:
<table><tr><th>LAEN</th><th>A3L</th><th>Curve Matched</th></tr><tr><td>0</td><td>X</td><td>No Equalizer</td></tr><tr><td>1</td><td>0</td><td>U.S. Survey Long</td></tr><tr><td>1</td><td>1</td><td>Japanese 3-Link</td></tr></table>
The link amplitude equalizer responses are given in the following table.

Link Amplitude Equalizer
<table><tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Gain Relative to 1700 Hz (dB)</th></tr><tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr><tr><td>1000</td><td>−0.27</td><td>−0.13</td></tr><tr><td>1400</td><td>−0.16</td><td>−0.08</td></tr><tr><td>2000</td><td>+0.33</td><td>+0.16</td></tr><tr><td>2400</td><td>+1.54</td><td>+0.73</td></tr><tr><td>2800</td><td>+5.98</td><td>+2.61</td></tr><tr><td>3000</td><td>+8.65</td><td>+3.43</td></tr></table></td></tr>
</table>

Table 8. R96DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>LCEN</td><td>Loop Clock Enable</td><td>0:4 0</td><td>When control bit LCEN is a one, the transmitter clock tracks the receiver clock.</td></tr>
<tr><td>LDEN</td><td>Link Delay Equalizer Enable</td><td>0·5·2</td><td>The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table:

<table>
<tr><th>LDEN</th><th>D3L</th><th>Curve Matched</th></tr>
<tr><td>0</td><td>X</td><td>No Equalizer</td></tr>
<tr><td>1</td><td>0</td><td>U.S Survey Long</td></tr>
<tr><td>1</td><td>1</td><td>Japanese 3-Link</td></tr>
</table>
The link delay equalizer responses are given in the following table.

Link Delay Equalizer
<table>
<tr><th rowspan="2">Frequency (Hz)</th><th colspan="2">Delay Relative to 1700 Hz (Microseconds)</th></tr>
<tr><th>U.S. Survey Long</th><th>Japanese 3-Link</th></tr>
<tr><td>800</td><td>-498.1</td><td>-653.1</td></tr>
<tr><td>1200</td><td>-188.3</td><td>-398.5</td></tr>
<tr><td>1600</td><td>-15.1</td><td>-30.0</td></tr>
<tr><td>1700</td><td>+0.0</td><td>+0.0</td></tr>
<tr><td>2000</td><td>-39.8</td><td>+11.7</td></tr>
<tr><td>2400</td><td>-423.1</td><td>-117.1</td></tr>
<tr><td>2800</td><td>-672.4</td><td>-546.3</td></tr>
</table></td></tr>
<tr><td>L2ACT</td><td>Remote Digital Loopback Activate</td><td>0·4:1</td><td>When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT recommendation V.54 loop 2</td></tr>
<tr><td>L3ACT</td><td>Local Analog Loopback Activate</td><td>0·4:7</td><td>When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT recommendation V.54 loop 3.</td></tr>
<tr><td>L4ACT</td><td>Remote Analog Loopback Activate</td><td>0:4:6</td><td>When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to recommendation V.54 loop 4.</td></tr>
<tr><td>L4HG</td><td>Loop 4 High Gain</td><td>0:4·5</td><td>When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.</td></tr>
<tr><td>MHLD</td><td>Mark Hold</td><td>0:7·4</td><td>When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).</td></tr>
<tr><td>$\overline{\text{PNDET}}$</td><td>Period N Detector</td><td>1·B:6</td><td>When status bit $\overline{\text{PNDET}}$ is a zero, it indicates a PN sequence has been detected. This bit sets to a one at the end of the PN sequence.</td></tr>
<tr><td>$\overline{\text{P2DET}}$</td><td>Period Two Detector</td><td>1:8:2</td><td>When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a P2 sequence has been detected. This bit sets to a one at the start of the PN sequence.</td></tr>
<tr><td>(None)</td><td>RAM Access T</td><td>0.F·0–7</td><td>Contains the RAM access code used in reading or writing chip 0 RAM locations via word Y (0·1 and 0 0)</td></tr>
<tr><td>(None)</td><td>RAM Access XB</td><td>2:5·0–7</td><td>Contains the RAM access code used in reading or writing chip 2 RAM locations via word X (2:3 and 2.2).</td></tr>
<tr><td>(None)</td><td>RAM Access XS</td><td>1:5·0–7</td><td>Contains the RAM access code used in reading or writing chip 1 RAM locations via word X (1·3 and 1:2)</td></tr>
<tr><td>(None)</td><td>RAM Access YB</td><td>2 4.0–7</td><td>Contains the RAM access code used in reading or writing chip 2 RAM locations via word Y (2:1 and 2:0)</td></tr>
</table>

Table 8. R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	RAM Access YS	1:4:0–7	Contains the RAM access code used in reading or writing chip 1 RAM locations via word Y (1:1 and 1:0).
(None)	RAM Data XBL	2:2:0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 2.
(None)	RAM Data XBM	2:3:0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 2.
(None)	RAM Data XSL	1:2:0–7	Least significant byte of 16-bit word X used in reading or writing RAM locations in chip 1.
(None)	RAM Data XSM	1:3:0–7	Most significant byte of 16-bit word X used in reading or writing RAM locations in chip 1.
(None)	RAM Data YBL	2:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YBM	2:1:0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 2.
(None)	RAM Data YSL	1:0:0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1. Shared by parallel data mode for presenting channel data to the host microprocessor bus. See 'Receiver Data.'
(None)	RAM Data YSM	1:1:0–7	Most significant byte of 16-bit word Y used in reading or writing RAM locations in chip 1.
(None)	RAM Data YTL	0.0.0–7	Least significant byte of 16-bit word Y used in reading or writing RAM locations in chip 0. It is shared by parallel data mode and DTMF dialing (see Transmitter Data)
(None)	RAM Data YTM	0:1:0–7	Most significant byte of 16-byte word Y used in reading or writing locations in chip 0.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{IRQ}$ low. In idle mode the interrupts from chip 2 occur at half the baud rate. During diagnostic access in data mode, the interrupts occur at the baud rate.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RBDA is a one
(None)	Receiver Configuration	1:6:0–5	The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB). *Receiver Configuration Control Codes* Control codes for the modem receiver configuration are: **Configuration Code (Hex) — Receiver Configuration** 14 — V.29 9600 12 — V.29 7200 11 — V.29 4800 22 — V.27 4800 Long 21 — V.27 2400 Long 02 — V.27 4800 Short 01 — V.27 2400 Short

Table 8. R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
(None)	Receiver Data	1·0:0–7	The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data When using receiver parallel data mode, the registers 1 3 through 1:0 can not be used for reading the chip 1 RAM
RPDM	Receiver Parallel Data Mode	1 7 4	When control bit RPDM is a one, the receiver supplies channel data to the receiver data register (1·0) as well as to the hardware serial data output (See Receiver Data)
RSB	Receiver Setup Bit	1 E:3	When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective. Worst case setup time is 2 baud times
RSDA	Receiver Sample Data Available	1·E:0	Status bit RSDA goes to a one when the receiver writes data to register 1:0 RSDA goes to a zero when the host processor reads data from register 1 0.
RSIA	Receiver Sample Interrupt Active	1:E 7	This status bit is a one whenever the receiver sample rate device is driving $\overline{IRQ}$ to zero.
RSIE	Receiver Sample Interrupt Enable	1:E:2	When the host processor writes a one in the RSIE control bit, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit RSDA is a one
RTDIS	Receiver Training Disable	1·7:0	When control bit RTDIS is a one, the receiver is prevented from recognizing a training sequence and entering the training state.
RTH	Receiver Threshold Field	1·7:6,7	The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB): **RTH** / **RLSD On** / **RLSD Off** 0 / > –43 dBm / < –48 dBm 1 / > –33 dBm / < –38 dBm 2 / > –26 dBm / < –31 dBm 3 / > –16 dBm / < –21 dBm
RTS	Request-to-Send	0·7.7	When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input These inputs are ORed by the modem.
SDIS	Scrambler Disable	0:7·5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0:7·0	When control bit SEPT is a one, the echo protector tone is 30 ms long rather than 185 ms.
SWRT	Sample Write	1·7:3	When control bit SWRT is a one, the RAM write operation is enabled for chip 1.
TBA	Transmitter Buffer Available	0:E 0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0.0, this bit sets to a one During a RAM access in chip 0, when TBA is a one the host can perform either a RAM read or write depending on the state of bit 0:6·3 (see Transmitter Configuration).
TIA	Transmitter Interrupt Active	0:E·7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero
TIE	Transmitter Interrupt Enable	0:E·2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one

Table 8. R96DP Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL** — **Transmitter Analog Output*** 0 — −1 dBm ±1 dB 1 — −3 dBm ±1 dB 2 — −5 dBm ±1 dB 3 — −7 dBm ±1 dB 4 — −9 dBm ±1 dB 5 — −11 dBm ±1 dB 6 — −13 dBm ±1 dB 7 — −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-on-Data	1.6:6	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-date.
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0). When TPDM is a zero channel data from the serial hardware input TXD is accepted and the chip 0 RAM access is enabled.
(None)	Transmitter Configuration*	0:6:0–7	The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB.) *Transmitter Configuration Control Codes* Control codes for the modem transmitter configurations are: **Configuration Code (Hex)*** — **Transmitter Configuration** 14 — V.29 9600 12 — V.29 7200 11 — V.29 4800 22 — V.27 4800 Long 21 — V.27 2400 Long 02 — V.27 4800 Short 01 — V.27 2400 Short 80 — Tone Transmit 04 — DTMF Tone Transmit ***Note:** Beginning with the R5304-22 device, bit 3 of the transmitter configuration register is used in the RAM access operation for chip 0 When 0:6:3 is a one, a RAM write operation will occur when TPDM is a zero, and when 0:6:3 is a zero, a RAM read operation will occur when TPDM is a zero. **Configuration Definitions** Definitions of the eight Transmitter Configurations are: 1. V.29. When a V.29 configuration has been selected, the modem operates as specified in the CCITT Recommendation V.29. 2. V.27. When a V.27 configuration has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 3. Tone Transmit. In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by two registers in the host interface memory space containing the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%. 4. DTMF Tone Transmit. In this configuration when the hex value of a DTMF digit is stored in register 0:0, a DTMF tone will be transmitted if RTS is enabled.

Table 8. R96DP Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter; DDR, RAM Data YTL</td><td>0 0 0–7</td><td>1 The host processor transmits data in the parallel mode by writing a data byte to the transmitter data register The data is divided on baud boundaries, as follows

NOTE

Data is transmitted bit zero first

<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.29 9600 bps</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V 29 7200 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V 29 4800 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="4">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
</table>

2. Register 0 0 is used to transmit DTMF digits when the transmitter is configured in the DTMF tone transmit mode.

3. Register 0.0 is a RAM data register used for reading or writing the least significant byte of the 16-bit Y word in Chip 0 when TPDM is a zero and no tone or DTMF tone transmission is occurring.</td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0 E:3</td><td>When the host processor changes the transmitter configuration, the host must write a one in this control bit TSB goes to a zero when the change becomes effective. Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7 6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>T2</td><td>T/2 Equalizer Select</td><td>1:7:1</td><td>When control bit T2 is a one, an adaptive equalizer with two taps per baud is used When T2 is a zero, the equalizer has one tap per baud. The total number of taps remains the same for both cases.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0·7:1</td><td>When control bit XCEN is a zero, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A. The clock appearing at the XTCLK input will appear at the TDCLK output</td></tr>
</table>

SIGNAL PROCESSOR RAM ACCESS

RAM and Data Organization

Each signal processor contains 128 words of random access memory (RAM). Each word is 32 bits wide. Because the signal processor is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16 bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. In the sample rate and baud rate devices the entire contents of XRAM and YRAM may be read from or written into by the host processor via the microprocessor interface. Access to the YRAM is possible only in the transmitter device.

Interface Memory

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. Information transfer between RAM and interface memory is accomplished by the signal processor logic unit moving data between the SP main bus and the SP I/O bus. The SP logic unit determines the RAM address to read from or write into by the code stored in the RAM ACCESS bits of interface memory registers. The SP logic unit normally transfers a word from RAM to interface memory once each cycle of the device code. Each RAM word transferred to the interface memory is 32 bits long (16 bits in the transmitter). These bits are written by the SP logic unit into interface memory registers 3, 2, 1, and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data, respectively. As previously described for parallel data mode, the data available bits set to a one when register 0 of the respective signal processor is written into by the device and resets to a zero when register 0 is read from by the host. Since the parallel data mode transmitter and receiver data register shares register 0 with the YRAM data, chip 0 and 1 RAM access are disabled in parallel data mode. However, chip 2 RAM access remains active in receiver parallel data mode.

The transmitter, sample rate device and the baud rate device allow data to be transferred from interface memory to RAM. When set to a one, bit SWRT (1:7:3) signals the chip 1 SP logic unit to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. Bit BWRT (1:7:2) performs the same function for chip 2 RAM. When writing into the RAM, 32 bits are transferred. The 16 bits written into XRAM come from registers 3 and 2, with register 3 being the more significant byte. The 16 bits written into YRAM come from registers 1 and 0, with register 1 being the more significant byte. When only 16 bits of data are to be written, FF (a dummy RAM location) must be stored in RAM ACCESS XS or RAM ACCESS YS to prevent writing the insignificant 16 bits of registers 1:3 through 1:0 into a valid RAM location. When the host processor writes into register 1:0 the RSDA bit (1:E:0) is reset to zero. When the SP logic unit reads data from register 1:0, the RSDA bit (1:E:0) is set to a one. In a similar manner, bit RBDA (2:E:0) resets to zero when the host processor writes into register 2:0 and sets to a one when the SP logic unit reads data from register 2:0.

When reading from RAM, or writing into RAM, the bits in registers 0:E, 1:E, 2:E can be used for handshaking or interrupt functions as in parallel data mode. When not in parallel data mode, the bits in register 1:E perform the handshake and interrupt functions for RAM access. In both serial and parallel data modes, the bits in register 2:E perform handshake and interrupt functions for RAM access. When set to one, bit RBIE (2:E:2) enables RBDA to drive the IRQ connector signal to zero volts when RBDA is a one. Bit RBIA (2:E:7) identifies chip 2, the baud rate device, as a source of IRQ interrupt. Bit RBIA is a one when both RBIE and RBDA are set to one. In the event that other system elements may cause IRQ to be driven low, the host must determine if modem chip 2 is causing an interrupt by reading RBIA.

Table 9 provides the available RAM access functions, codes, and registers.

Auto Dial Sequence

The Figure 6 flowchart defines the auto dial sequence via the microprocessor interface memory. The modem timing for the auto dialer accounts for DTMF tone duration and interdigit delay. The default tone duration is 95 ms and the default interdigit delay is 71 ms. The default amplitudes for the high and low frequencies are – 4 dBm and – 6 dBm, respectively. The above four parameters can be changed by performing a RAM write.

Table 9. RAM Access Codes

No.	Function	Chip	X Access Code (Hex)	Y Access Code (Hex)	Register
1	DTMF Low Frequency Amplitude[1]	0	—	88	0,1
2	DTMF High Frequency Amplitude[1]	0	—	08	0,1
3	Interdigit Delay[1]	0	—	89	0,1
4	DTMF Tone Duration[1]	0	—	09	0,1
5	Received Signal Samples	1	C0	Not Used	2,3
6	Demodulator Output	1	C2	42	0,1,2,3
7	Low Pass Filter Output	1	D4	54	0,1,2,3
8	Average Energy	1	DC	Not Used	2,3
9	AGC Gain Word	1	81	Not Used	2,3
10	Equalizer Input	2	C0	40	0,1,2,3
11	Equalizer Tap Coefficients	2	81 – A0	01 – 20	0,1,2,3
12	Unrotated Equalizer Output	2	E1	61	0,1,2,3
13	Rotated Equalizer Output (Received Points)	2	A2	22	0,1,2,3
14	Decision Points Ideal Points	2	62	0,1,2,3	
15	Error	2	E3	63	0,1,2,3
16	Rotation Angle	2	Not Used	00	0,1
17	Frequency Correction	2	AA	Not Used	2,3
18	EQM	2	A7	Not Used	2,3
19	Dual Point	2	AE	2E	0,1,2,3

Note: 1. Added in transmitter device R5304-22.

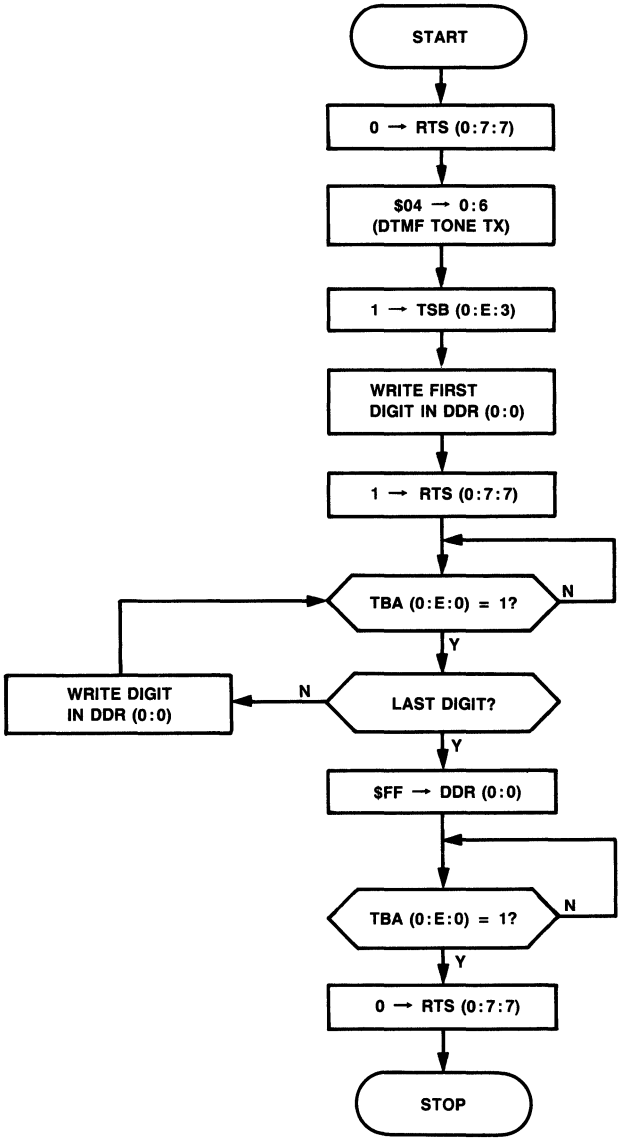


Figure 6. R96DP Auto Dial Sequence

PERFORMANCE

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56, except with regard to the placement of the filter used to bandlimit the white noise source. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

Typical BER performance is shown in Figure 7. Figure 8 shows a typical test setup to measure BER.

TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

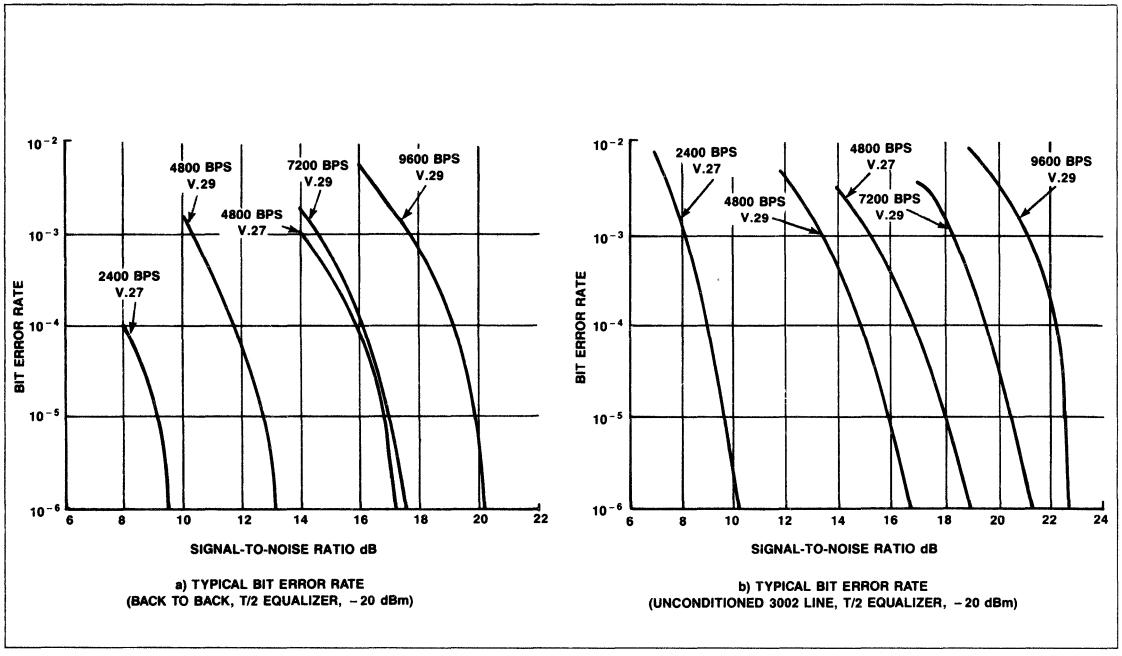


Figure 7. R96DP BER versus SNR

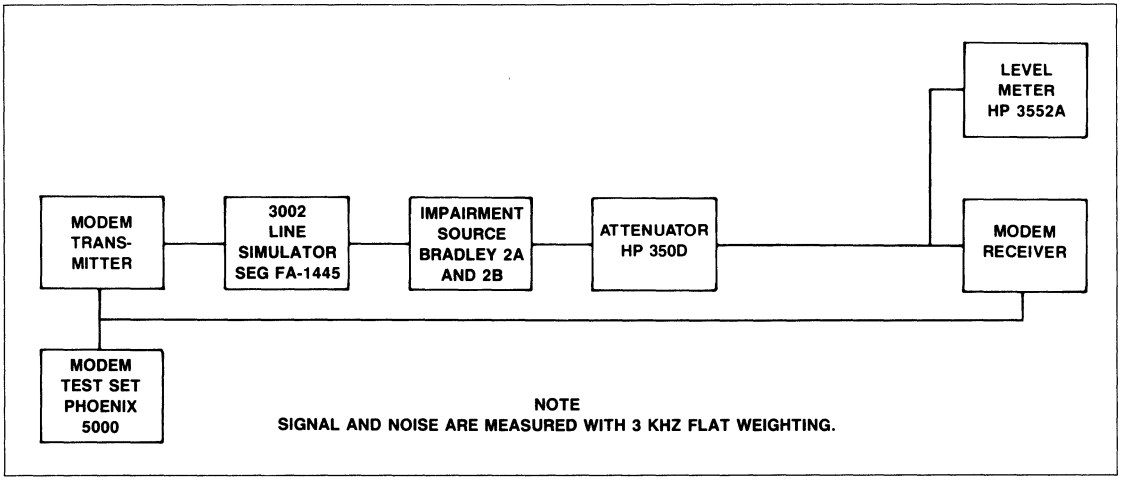


Figure 8. BER Performance Test Set-up

GENERAL SPECIFICATIONS

Table 10. Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	550 mA	<700 mA
+12 Vdc	±5%	5 mA	< 10 mA
-12 Vdc	±5%	25 mA	< 50 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.			

Table 11. Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	-40°C to +80°C (-40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.
Altitude	-200 feet to +10,000 feet

Table 12. Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.937 in. (100 mm)
Length	4.725 in. (120 mm)
Connector Height	0.437 in. (11.1 mm)
Component Height	
Top (max.)	0.200 in. (5.1 mm)
Bottom (max.)	0.130 in. (3.3 mm)
Weight (max):	3.6 oz. (100 g)
Lead Extrusion (max.):	0.100 in. (2.54 mm)
DIP Connector Version	
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.228 in. (82 mm)
Length	3.937 in. (100 mm)
Component Height	
Top (max.)	0 200 in. (5.1 mm)
Bottom (max.)	0 130 in. (3.3 mm)
Weight (max.):	3.6 oz. (100 g)
Pin Length (max.)	0.53 in. (13.5 mm)

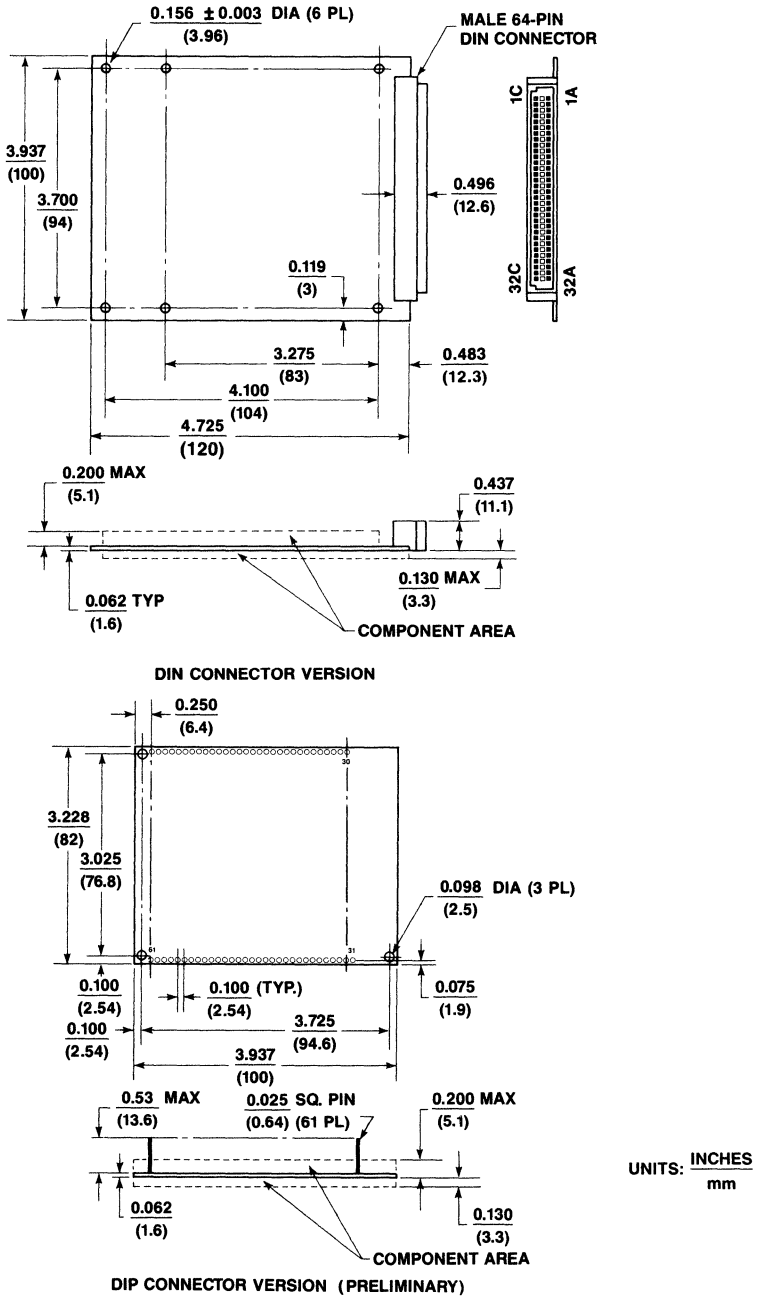


Figure 9. R96DP Modem Dimensions and Pin Locations

Rockwell

R96FT
9600 bps Fast Train Modem

INTRODUCTION

The Rockwell R96FT is a synchronous serial 9600 bps modem designed for multipoint and networking applications. The R96FT allows full-duplex operation over 4-wire dedicated unconditioned lines, or half-duplex operation over the public switched telephone network (PSTN).

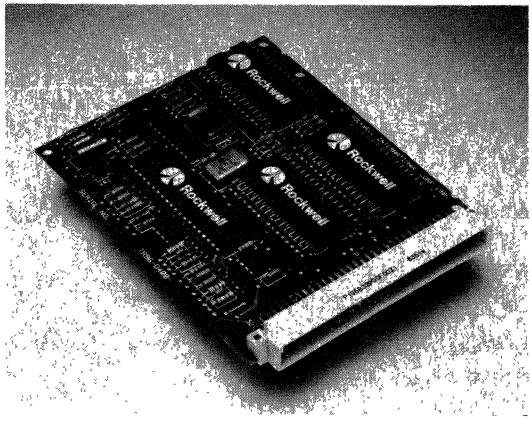
Proprietary fast train configurations provide training times of 23 ms for V.29FT/9600/7200/4800, 22 ms for V.27FT/4800, and 30 ms for V.27FT/2400. A 2400/4800 bps Gearshift configuration provides a training time of 10 ms. For applications requiring operation with international standards, fallback configurations compatible with CCITT recommendations V.29 and V.27 bis/ter are provided. A 300 bps FSK configuration, compatible with CCITT V.21 Channel 2, is also provided.

The small size and low power consumption of the R96FT offer the user flexibility in formulating a 9600 bps modem design customized for specific packaging and functional requirements.

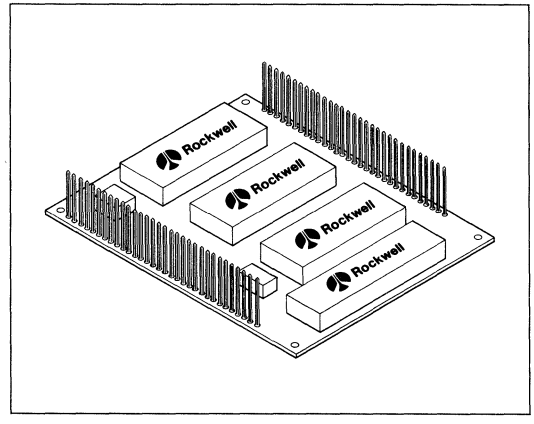
This data sheet corresponds to assembly number TR96-D400-061 and subsequent revisions.

FEATURES

- Proprietary Fast Train
- 2400/4800 bps Gearshift
- CCITT V.29, V.27 bis/ter and V.21 Channel 2 Compatible
- Train on Data
- 2-Wire Half Duplex, 4-Wire Full Duplex
- Programmable Tone Generation
- Dynamic Range −43 dBm to −5 dBm
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Loopbacks
  - — Local Analog
  - — Remote Analog and Digital
- Small Size
  - — DIP Connector Version: 120 mm x 100 mm (4.73 in. x 3.94 in.)
  - — DIN Connector Version: 82 mm x 100 mm (3.23 in. x 3.94)
- Low Power Consumption: 3W (typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R96FT DIN Connector Version



R96FT DIP Connector Version

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

Function	Frequency (Hz ±0.01%)
V.27 bis/ter Carrier	1800
V.27FT Carrier	1800
2400/4800 bps Gearshift	1800
V.29 Carrier	1700
V.29FT Carrier	1700/1800*
V.21 Channel 2:	
Mark	1650
Space	1850
*Selectable carrier frequency	

TONE GENERATION

Under control of the host processor, the R96FT can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

Parameter	Specification
Signaling Rate: Data Rate:	2400 baud 9600 bps 7200 bps 4800 bps
Signaling Rate: Data Rate:	1600 baud 4800 bps
Signaling Rate: Data Rate: Gearshift Data Rate:	1200 baud 2400 bps 2400/4800 bps
Signaling Rate: Data Rate:	300 baud 300 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 bis/ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 bis/ter.

For the Gearshift configuration, the signaling rate is 1200 baud. The 2400 bps data stream is encoded into dibits forming a 4-point structure, and the 4800 bps data stream is encoded into quadbits forming a 16-point structure. The first 32 bauds of data are transmitted at 2400 bps and the remaining message is transmitted at 4800 bps.

At 300 baud, the 300 bps data stream is encoded per CCITT V.21 Channel 2 into a mark frequency of 1650 Hz and a space frequency of 1850 Hz.

EQUALIZERS

The R96FT provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive T equalizer is provided in the receiver circuit.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96FT incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 bis/ter or V.29 depending on the selected configuration.

The scrambler/descrambler facilities for Gearshift can be selected to be in accordance with either V.27 bis/ter or V.29. The scrambler/descrambler selection is made by writing the appropriate configuration codes into the transmitter and receiver.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96FT can adapt to received frequency error of up to ±10 Hz with less than 0.2 dB degradation in BER performance.

During fast train polling, frequency offset must be less than ±2 Hz for successful training.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from –5 dBm to –43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

The R96FT provides a data derived Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a squarewave. The low-to-high transitions of this output coincide with the centers of received data bits. For the Gearshift configuration, the first 32 bauds of data are at 2400 bps followed by 4800 bps data for the remaining message. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. $\overline{\text{RDCLK}}$ duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is accurate to ±1.0 dB and is programmable from –1.0 dBm to –15.0 dBm in 2 dB steps.

TRANSMIT TIMING

The R96FT provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400 or 300 Hz (±0.01%). For the Gearshift Configuration, TDCLK is a 2400 Hz clock for the first 32 bauds of data, and a 4800 Hz clock for the remaining message.
2. *Duty Cycle.* 50% ±1%

Input data presented on TXD is sampled by the R96FT at the low-to-high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The transmitter data clock (TDCLK) can be phase locked to a signal on input XTCLK. This input signal must equal the desired data rate ±0.01% with a duty cycle of 50% ±20%.

TRAIN ON DATA

When train on data is enabled (by setting a bit in the interface memory), the modem monitors the EQM signal. If EQM indicates a loss of equalization (i.e., BER approximately 10^{-3} for 0.5 seconds) the modem attempts to retrain on the data stream. The time for retrain is typically 3 to 15 seconds.

TURN-ON SEQUENCE

A total of 20 selectable turn-on sequences can be generated as defined in the following table:

No.	V.29 (bps)	V.27 bis/ter (bps)	Gearshift (bps)	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Response Time (milliseconds)	Comments
1	FT/9600			23	
2	FT/7200			24	Proprietary
3	FT/4800			23	Fast Train
4		FT/4800		22	
5		FT/2400		30	
6	9600			253	
7	7200			253	
8	4800			253	
9		4800 long		708	
10		2400 long		943	
11		4800 short		50	
12		2400 short		67	
13			2400/4800	10	
14	9600			438	Preceded[1]
15	7200			438	by Echo
16	4800			438	Protector
17		4800 long		913	Tone for
18		2400 long		1148	lines using
19		4800 short		255	echo
20		2400 short		272	suppressors.

1. For short echo protector tone, subtract 155 ms from values of $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ response time.
2. V.21 (300 bps FSK) $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ response time is <35 ms.

TURN-OFF SEQUENCE

For V.27 bis/ter, V.27FT and 2400/4800 bps Gearshift configurations, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy (V.27 bis/ter only). For V.29 and V.29FT, the turn-off sequence consists of approximately 8 ms of remaining data and scrambled ones.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) when the Received Line Signal Detector ($\overline{\text{RLSD}}$) is off.

RESPONSE TIMES OF CLEAR TO SEND ($\overline{\text{CTS}}$)

The time between the off-to-on transition of Request To Send ($\overline{\text{RTS}}$) and the off-to-on transition of Clear to Send ($\overline{\text{CTS}}$) is dictated by the length of the training sequence and the echo protector tone, if used. These times are given in the Turn-On Sequences table. If training is not enabled, $\overline{\text{RTS}}$/$\overline{\text{CTS}}$ delay is less than 2 baud times.

The time between the on-to-off transition of $\overline{\text{RTS}}$ and the on-to-off transition of $\overline{\text{CTS}}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVE LINE SIGNAL DETECTOR ($\overline{\text{RLSD}}$)

Response

For Fast Train and Gearshift configurations, the receiver enters the training state upon detecting a significant increase in the received signal power. If the received line signal power is greater than the selected threshold level at the end of the training state, the receiver enters the data state and $\overline{\text{RLSD}}$ is activated. If the received line signal power is less than the selected threshold level at the end of the training state, the receiver returns to the idle state and $\overline{\text{RLSD}}$ is not activated.

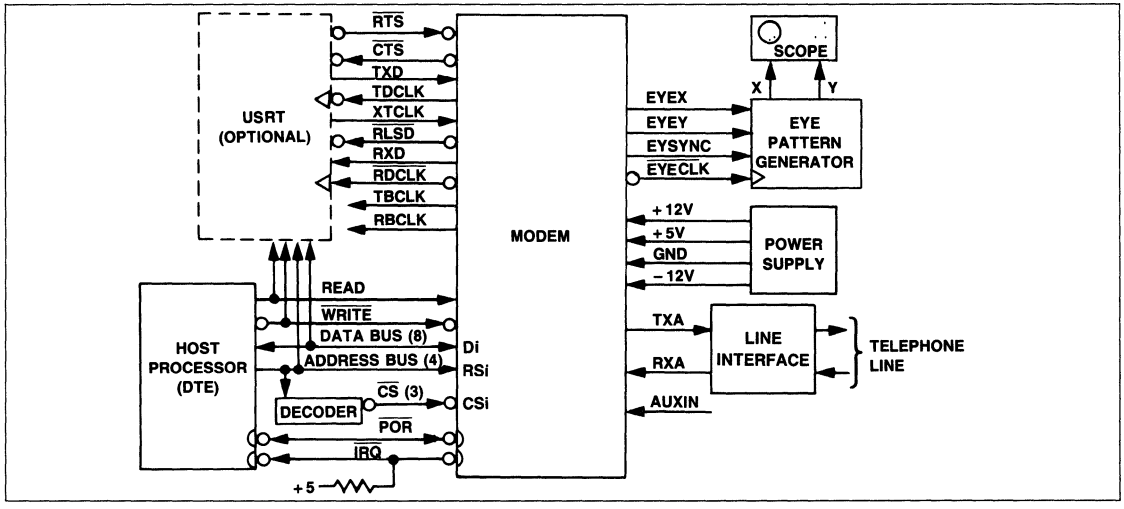
Also, in Fast Train and Gearshift configurations, the receiver initiates the turn-off delay upon detecting a significant decrease in the received signal power. If the received signal power is less than the selected threshold at the end of the turn-off delay, the receiver enters the idle state and $\overline{\text{RLSD}}$ is deactivated. If the received signal power is greater than the selected threshold at the end of the turn-off delay, the receiver returns to the data state and $\overline{\text{RLSD}}$ is left active.

For CCITT configurations, the receiver enters the training detection state when the received line signal power crosses the selected threshold level. $\overline{\text{RLSD}}$ is activated at the end of the training sequence. For V.21 Channel 2, a separate received line signal detector ($\overline{\text{FRLSD}}$) is provided. $\overline{\text{FRLSD}}$ is activated when energy above −43 dBm is present at the receiver's audio input (RXA). The $\overline{\text{FRLSD}}$ off-to-on response time is 15 ±5 ms and the on-to-off response time is 25 ±5 ms.

The $\overline{\text{RLSD}}$ on-to-off response times are:

Configuration	$\overline{\text{RLSD}}$ On-To-Off Response Time (ms)
V.29 Fast Train	6.5 ±1
V.27 Fast Train	8 ±1
Gearshift	6 ±1
V.29	30 ±9
V.27 bis/ter	10 ±5

$\overline{\text{RLSD}}$ response times are measured with a signal at least 3 dB above the actual $\overline{\text{RLSD}}$ on threshold or at least 5 dB below the actual $\overline{\text{RLSD}}$ off threshold.



R96FT Functional Interconnect Diagram

Threshold Options

Four threshold options are provided:

1. Greater than −43 dBm ($\overline{RLSD}$ on)
   Less than −48 dBm ($\overline{RLSD}$ off)
2. Greater than −33 dBm ($\overline{RLSD}$ on)
   Less than −38 dBm ($\overline{RLSD}$ off)
3. Greater than −26 dBm ($\overline{RLSD}$ on)
   Less than −31 dBm ($\overline{RLSD}$ off)
4. Greater than −16 dBm ($\overline{RLSD}$ on)
   Less than −21 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

For CCITT configurations, a minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R96FT is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R96FT has the capability of transferring channel data (up to eight bits at a time) via the microprocessor bus.

MODE SELECTION

For the transmitter, a control bit determines whether the source of transmitted data is the V.24 interface (serial mode) or the parallel transmitter data register (parallel mode). The transmitter automatically defaults to the serial mode at power-on.

The receiver simultaneously outputs received data via the V.24 interface and the parallel receiver data register.

In either parallel or serial mode, the R96FT is configured by the host processor via the microprocessor bus.

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R96FT Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

Eye Pattern Generation

The four hardware diagnostic circuits, identified in the following table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the

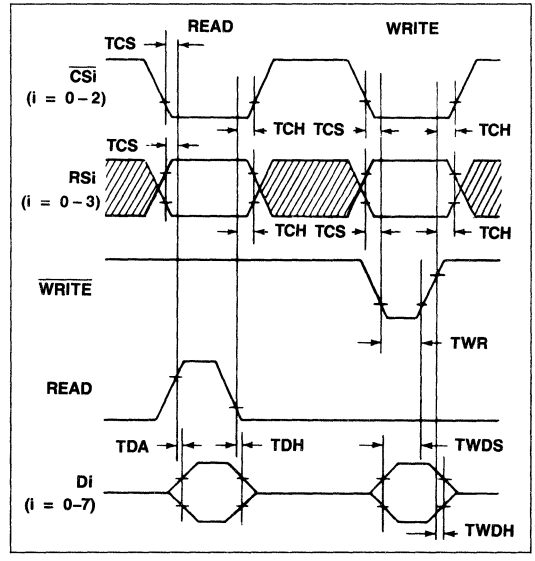
rising edge of the $\overline{\text{EYECLK}}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

R96FT Hardware Circuits

Name	Type	DIN Pin No.	DIP Pin No.	Description
A. OVERHEAD:				
Ground (A)	AGND	31C,32C	30,31	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	29,37,53	Digital Ground Return
+5 volts	PWR	19C,23C, 26C,30C	1,45,61	+5 Vdc Supply
+12 volts	PWR	15A	32	+12 Vdc Supply
−12 volts	PWR	12A	36	−12 Vdc Supply
$\overline{\text{POR}}$	I/OB	13C	2	Power-on-reset
B. MICROPROCESSOR INTERFACE:				
D7	I/OA	1C	3	Data Bus (8 Bits)
D6	I/OA	1A	4	
D5	I/OA	2C	5	
D4	I/OA	2A	6	
D3	I/OA	3A	7	
D2	I/OA	4C	8	
D1	I/OA	4A	9	
D0	I/OA	5C	10	
RS3	IA	6C	16	Register Select (4 Bits)
RS2	IA	6A	17	
RS1	IA	7C	18	
RS0	IA	7A	19	
$\overline{\text{CS0}}$	IA	10C	20	Chip Select—Transmitter Device
$\overline{\text{CS1}}$	IA	9C	21	Chip Select—Receiver Sample Rate Device
$\overline{\text{CS2}}$	IA	9A	13	Chip Select—Receiver Baud Rate Device
$\overline{\text{READ}}$	IA	12C	14	Read Enable
$\overline{\text{WRITE}}$	IA	11A	12	Write Enable
$\overline{\text{IRQ}}$	OB	11C	11	Interrupt Request
C. V.24 INTERFACE:				
$\overline{\text{RDCLK}}$	OC	21A	23	Receive Data Clock
TDCLK	OC	23A	46	Transmit Data Clock
XTCLK	IB	22A	51	External Transmit Clock
$\overline{\text{RTS}}$	IB	25A	50	Request to Send
$\overline{\text{CTS}}$	OC	25C	49	Clear to Send
TXD	IB	24C	48	Transmitter Data
$\overline{\text{RXD}}$	OC	22C	26	Receiver Data
$\overline{\text{RLSD}}$	OC	24A	27	Received Line Signal Detector
D. ANCILLARY CIRCUITS:				
RBCLK	OC	26A	22	Receiver Baud Clock
TBCLK	OC	27C	47	Transmitter Baud Clock
FRXD	OD	16A	60	FSK Receiver Data (inverted data)
$\overline{\text{FRLSD}}$	OD	17C	44	FSK Received Line Signal Detector
E. ANALOG SIGNALS:				
TXA	AA	31A	34	Transmitter Analog Output
RXA	AB	32A	33	Receiver Analog Input
AUXIN	AC	30A	—	Auxiliary Analog Input
F. DIAGNOSTIC:				
EYEX	OC	15C	56	Eye Pattern Data—X Axis
EYEY	OC	14A	55	Eye Pattern Data—Y Axis
$\overline{\text{EYECLK}}$	OA	14C	57	Eye Pattern Clock
EYESYNC	OA	13A	58	Eye Pattern Synchronizing Signal

NOTE: Pins not used on the DIP Version: 15, 24, 25, 28, 35, 38–43, 52, 54 and 59.

Microprocessor Timing



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{\text{CSi}}$, RSi setup time prior to Read or $\overline{\text{Write}}$	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
$\overline{\text{CSi}}$, RSi hold time after Read or $\overline{\text{Write}}$	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

Digital Interface Characteristics

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type								
			IA	IB	IC	OA	OB	OC	OD	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min	2.0 Min.					2 0 Min.	5.25 Max 2.0 Min.
V_{IL}	Input Voltage, Low	V	0 8 Max.	0.8 Max	0.8 Max.					0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2.2 Min [6]	2 4 Min.[1]	2.4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max [2]	0 4 Max [2]	0.4 Max.[2]	0.6 Max.[7]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2 5 Max.							±2 5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.					
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.			
I_L	Output Current, Leakage	μA					±10 Max.				
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min.			−240 Max. −10 Min.			−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20					10	40
C_D	Capacitive Drive	pF				100	100	100		100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	TTL	3-State Transceiver	Open-Drain w/Pull-up

Notes 1. I Load = −100 μA 3. I Load = −40 μA 5. I Load = 0.36 mA 7. I Load = 2.0 mA
2. I Load = 1.6 mA 4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc 6. I Load = −400 μA

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604 ohms ± 1%.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is TLVL setting +0.6 dB −1.4 dB. If unused, this input must be grounded near the modem connector. If used, it must be driven from a low impedance source.

SOFTWARE CIRCUITS

The R96FT comprises three signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 1 update at half the modem sample rate (4800 bps). Registers in chip 0 and 2 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0–2), the register by Z(0–F), and the bit by Q(0–7, 0 = LSB).

Status Control Bits

The operation of the R96FT is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a dash (—) are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R96FT provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers in chip 2 allow user access to RAM locations via the X word registers (2:3 and 2:2) and the Y word register (2:1 and 2:0). The access code stored in RAM ACCESS X (2:5) selects the source of data for RAM DATA XM and RAM DATA XL (2:3 and 2:2). Similarly, the access code stored in RAM ACCESS Y (2:4) selects the source of data for RAM DATA YM and RAM DATA YL (2:1 and 2:0).

Reading of diagnostic RAM data is performed by storing the necessary access codes in 2:5 and 2:4, reading 2:0 to reset the associated data available bit (2:E:0), then waiting for the data available bit to return to a one. Data is now valid and may be read from 2:3 through 2:0.

An additional diagnostic is supplied by the sample rate processor (chip 1). Registers 1:2 and 1:3 supply a 16 bit AGC Gain Word. These two diagnostic data registers are updated at the sample rate during the data state and may be read by the host processor asynchronously.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

Baud Rate Processor (Chip 2) RAM Access Codes

No.	Function	X Access	Y Access	Register
1	Equalizer Input	C0	40	0,1,2,3
2	Equalizer Tap Coefficients	81–A0	01-20	0,1,2,3
3	Unrotated Equalizer Output	E1	61	0,1,2,3
4	Rotated Equalizer Output	E2	62	0,1,2,3
5	Decision Points (Ideal Data Points)	E8	68	0,1,2,3
6	Error Vector	E5	65	0,1,2,3
7	Rotation Angle	A7	Not Used	2,3
8	Frequency Correction	A5	Not Used	2,3
9	Eye Quality Monitor (EQM)	AC	Not Used	2,3

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	FSKT	ASCR	—	—	TCF	DDEE	—	—
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	—	—	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	—	—	—	—	—	—	—	—
0	TRANSMITTER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RIA	—	—	—	RSB	RIE	—	RDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	—	$\overline{CDET}$	—	—
8	—	—	—	—	$\overline{P2DET}$	—	—	—
7	RTH		DDIS	—	—	RCF	RDIS	—
6	TOD	RECEIVER CONFIGURATION						
5	—	—	—	—	—	—	—	—
4	—	—	—	—	—	—	—	—
3	AGC GAIN WORD (MSB)							
2	AGC GAIN WORD (LSB)							
1	—	—	—	—	—	—	—	—
0	RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS X							
4	RAM ACCESS Y							
3	RAM DATA XM							
2	RAM DATA XL							
1	RAM DATA YM							
0	RAM DATA YL							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

R96FT Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
ASCR	Append Scrambled Ones	0:9:6	When control bit ASCR is a one, one baud of scrambled marks is included in the V.29FT and V.27FT training sequences. The RTS-CTS delay is thus extended by one baud period when ASCR is a one.
A3L	Amplitude 3-Link Select	0:5:1	See LAEN.
$\overline{\text{CDET}}$	Carrier Detector	1:9:2	When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
CEQ	Cable Equalizer Field	0:5:(4,5)	The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following table lists the possible cable equalizer selection codes: **CEQ** — **Cable Length (0.4 mm diameter)** 0 — 0.0 1 — 1.8 km 2 — 3.6 km 3 — 7.2 km
DDEE	Digital Delay Equalizer Enable	0:9:2	When control bit DDEE is a one, a fourth order digital delay equalizer is inserted in the transmit path.
DDIS	Descramble Disable	1:7:5	When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.
D3L	Delay 3-Link Select	0:5:0	See LDEN.
EPT	Echo Protector Tone	0:7:3	When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission. This option is available in the V.27 and V.29 configurations, although it is not specified in the CCITT V.29 Recommendation.
$\overline{\text{FED}}$	Fast Energy Detector	1:9:6	When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband.
(None)	FREQL/FREQM	0:2:0–7, 0:3:0–7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below: *FREQM Register (0:3)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01% Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below: **Frequency (Hz)** — **FREQM** — **FREQL** 462 — 0C — 52 1100 — 1D — 55 1650 — 2C — 00 1850 — 31 — 55 2100 — 38 — 00
FSKT	FSK Transmitter Configuration	0:9:7	The V.21 Channel 2 (300 bps synchronous FSK) transmitter configuration is selected by setting the FSKT control bit to a one (see TSB). While set to a one, this control bit overrides the configuration selected by the control code in register 0:6. The FSK data may be transmitted in parallel mode or in serial mode (see TPDM).

R96FT Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
LAEN	Link Amplitude Equalizer Enable	0:5:3	The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table: **LAEN** / **A3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
LCEN	Loop Clock Enable	0:4:0	When control bit LCEN is a one, the transmitter clock tracks the receiver clock.
LDEN	Link Delay Equalizer Enable	0:5:2	The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table: **LDEN** / **D3L** / **Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
L2ACT	Remote Digital Loopback Activate	0:4:1	When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT Recommendation V.54 loop 2.
L3ACT	Local Analog Loopback Activate	0:4:7	When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT Recommendation V.54 loop 3.
L4ACT	Remote Analog Loopback Activate	0:4:6	When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to CCITT Recommendation V.54 loop 4.
L4HG	Loop 4 High Gain	0:4:5	When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.
MHLD	Mark Hold	0:7:4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).
$\overline{\text{P2DET}}$	Period 2 Detector	1:8:3	When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a period 2 sequence has been detected. This bit sets to a one at the start of the period N sequence. This bit is only significant for CCITT V.29 and V.27 bis/ter configurations.
(None)	RAM Access X	2:5.0–7	Contains the RAM access code used in reading chip 2 RAM locations via word X (2:3 and 2:2).
(None)	RAM Access Y	2:4:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word Y (2:1 and 2:0).
(None)	RAM Data XL	2:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XM	2:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data YL	2:0.0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YM	2:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 2.
RBDA	Receiver Baud Data Available	2:E:0	Status bit RBDA goes to a one when the receiver writes data into register 2:0. The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E:7	This status bit is a one whenever the receiver baud rate device is driving $\overline{\text{IRQ}}$ low.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{\text{IRQ}}$ line of the hardware interface is driven to zero when status bit RBDA is a one.
RCF	Receiver Carrier Frequency	1:7:2	Control bit RCF selects the demodulator carrier frequency for V.29FT configurations as follows: **RCF** / **Demodulator Carrier Frequency** 0 / 1700 Hz 1 / 1800 Hz

R96FT Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Receiver Configuration</td><td>1:6:0–6</td><td>The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB).
Note: The receiver must be disabled prior to changing configurations See RDIS.
Receiver Configuration Control Codes
Control codes for the modem receiver configuration are:
<table>
<tr><th colspan="2">Configuration</th><th rowspan="2">Configuration Code (Hex)</th></tr>
<tr><th>V29</th><th>V27 bis/ter</th></tr>
<tr><td>FT/9600
FT/7200
FT/4800</td><td>

FT/4800
FT/2400</td><td>1C
1A
19
0A
09</td></tr>
<tr><td>9600
7200
4800</td><td>

4800 long
2400 long
4800 short
2400 short</td><td>14
12
11
22
21
02
01</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.29 descrambler
2400/4800 bps Gearshift/V.27 bis/ter descrambler</td><td>61[1]
41[1]</td></tr>
<tr><td colspan="2">V.21 Channel 2</td><td>See Note 2</td></tr>
</table>
1. The Receiver Configuration code automatically changes from a hex 61 (or hex 41) to a hex 64 (or hex 44) when the receiver transitions from the 2400 bps data state to the 4800 bps data state.
2. The FSK receiver is active at all times. Two ancillary hardware circuits, $\overline{\text{FRLSD}}$ and $\overline{\text{FRXD}}$, are supplied for FSK message reception. $\overline{\text{FRLSD}}$ is described under the Received Line Signal Detector section. $\overline{\text{FRXD}}$ provides inverted FSK received data. Timing extraction must be performed on the $\overline{\text{FRXD}}$ signal externally as no FSK receiver data clock is provided by the R96FT.</td></tr>
<tr><td>(None)</td><td>Receiver Data</td><td>1:0:0–7</td><td>The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data.</td></tr>
<tr><td>RDA</td><td>Receiver Data Available</td><td>1:E:0</td><td>Status bit RDA goes to a one when the receiver writes data to register 1:0. RDA goes to a zero when the host processor reads data from register 1:0.</td></tr>
<tr><td>RDIS</td><td>Receiver Disable</td><td>1:7:1</td><td>When control bit RDIS is a one, the receiver is disabled, $\overline{\text{RLSD}}$ is turned off and RXD is clamped to all marks. This bit can be used to squelch the receiver during half duplex transmissions over two wires. This bit must be set to a one prior to changing the receiver configuration.</td></tr>
<tr><td>RIA</td><td>Receiver Interrupt Active</td><td>1:E:7</td><td>This status bit is a one whenever the receiver sample rate device is driving $\overline{\text{IRQ}}$ to zero.</td></tr>
<tr><td>RIE</td><td>Receiver Interrupt Enable</td><td>1:E:2</td><td>When the host processor writes a one in the RIE control bit, the $\overline{\text{IRQ}}$ line of the hardware interface is driven to zero when status bit RDA is a one.</td></tr>
<tr><td>RSB</td><td>Receiver Setup Bit</td><td>1:E:3</td><td>When the host processor changes the receiver configuration or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective.</td></tr>
<tr><td>RTH</td><td>Receiver Threshold Field</td><td>1:7:6,7</td><td>The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB):
<table>
<tr><th>RTH</th><th>RLSD On</th><th>RLSD Off</th></tr>
<tr><td>0</td><td>> –43 dBm</td><td>< –48 dBm</td></tr>
<tr><td>1</td><td>> –33 dBm</td><td>< –38 dBm</td></tr>
<tr><td>2</td><td>> –26 dBm</td><td>< –31 dBm</td></tr>
<tr><td>3</td><td>> –16 dBm</td><td>< –21 dBm</td></tr>
</table></td></tr>
<tr><td>RTS</td><td>Request-to-Send</td><td>0:7:7</td><td>When control bit RTS goes to a one, the modem begins a transmit sequence. It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware RTS control input These inputs are OR'ed by the modem.</td></tr>
</table>

R96FT Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>SDIS</td><td>Scrambler Disable</td><td>0:7:5</td><td>When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.</td></tr>
<tr><td>SEPT</td><td>Short Echo Protector Tone</td><td>0:7:0</td><td>When control bit SEPT is a one, the echo protector disable tone is 30 ms long rather than 185 ms. (See TSB.)</td></tr>
<tr><td>TBA</td><td>Transmitter Buffer Available</td><td>0:E:0</td><td>This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one.</td></tr>
<tr><td>TCF</td><td>Transmitter Carrier Frequency</td><td>0:9:3</td><td>Control bit TCF selects the modulator carrier frequency for V.29FT configurations as follows:
TCF — Modulator Carrier Frequency
0 — 1700 Hz
1 — 1800 Hz</td></tr>
<tr><td>TIA</td><td>Transmitter Interrupt Active</td><td>0:E:7</td><td>This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.</td></tr>
<tr><td>TIE</td><td>Transmitter Interrupt Enable</td><td>0:E:2</td><td>When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.</td></tr>
<tr><td>TLVL</td><td>Transmitter Level Field</td><td>0:4:2–4</td><td>The transmitter analog output level is determined by eight TLVL codes, as follows:
TLVL — Transmitter Analog Output*
0 — −1 dBm ±1 dB
1 — −3 dBm ±1 dB
2 — −5 dBm ±1 dB
3 — −7 dBm ±1 dB
4 — −9 dBm ±1 dB
5 — −11 dBm ±1 dB
6 — −13 dBm ±1 dB
7 — −15 dBm ±1 dB
*Each step above is a 2 dB change ±0.2 dB.</td></tr>
<tr><td>TOD</td><td>Train-On-Data</td><td>1:6:7</td><td>When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-data.</td></tr>
<tr><td>TPDM</td><td>Transmitter Parallel Data Mode</td><td>0:7:2</td><td>When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0) rather than the serial hardware data input.</td></tr>
<tr><td>(None)</td><td>Transmitter Configuration</td><td>0:6:0–7</td><td>The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB.)
Transmitter Configuration Control Codes
Control codes for the modem transmitter configurations are:
<table>
<tr><th colspan="2">Configuration</th><th rowspan="2">Configuration Code (Hex)</th></tr>
<tr><th>V29</th><th>V27 bis/ter</th></tr>
<tr><td>FT/9600</td><td></td><td>1C</td></tr>
<tr><td>FT/7200</td><td></td><td>1A</td></tr>
<tr><td>FT/4800</td><td></td><td>19</td></tr>
<tr><td></td><td>FT/4800</td><td>0A</td></tr>
<tr><td></td><td>FT/2400</td><td>09</td></tr>
<tr><td>9600</td><td></td><td>14</td></tr>
<tr><td>7200</td><td></td><td>12</td></tr>
<tr><td>4800</td><td></td><td>11</td></tr>
<tr><td></td><td>4800 long</td><td>22</td></tr>
<tr><td></td><td>2400 long</td><td>21</td></tr>
<tr><td></td><td>4800 short</td><td>02</td></tr>
<tr><td></td><td>2400 short</td><td>01</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.29 Scrambler</td><td>61</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.27 bis/ter Scrambler</td><td>41</td></tr>
<tr><td colspan="2">V.21 Channel 2</td><td>See FSKT</td></tr>
<tr><td colspan="2">Tone transmit</td><td>80</td></tr>
</table></td></tr>
</table>

R96FT Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter Data</td><td>0:0:0–7</td><td>The host processor conveys output data to the transmitter in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

Note: Data is transmitted bit zero first

<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.29 9600 bps</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.29 7200 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.29 4800 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="3">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>2400 bps Gearshift</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td colspan="2">Baud 0</td></tr>
<tr><td>4800 bps Gearshift</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
</table>
</td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the SEPT bit or the FSKT bit, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective. Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7:6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a one, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A.</td></tr>
</table>

POWER-ON INITIALIZATION

When power is applied to the R96FT, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is generated.

At POR time the modem defaults to the following configuration: fast train, V.29, 9600 bps, no echo protector tone, 1700 Hz carrier frequency, scrambled ones segment disabled, serial data mode, internal clock, cable equalizers disabled, transmitter digital delay equalizer disabled, link amplitude equalizer disabled, link delay equalizer disabled, transmitter output level set to -1 dBm ± 1 dB, interrupts disabled, receiver threshold set to -43 dBm, and train-on-data enabled.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or more applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after $\overline{POR}$ is removed.

PERFORMANCE

Whether functioning in V.27, V.29 or the proprietary fast train configurations, the R96FT provides the user with high performance.

POLLING SUCCESS

In the 9600 bps fast train configuration the modem approaches a 98% success rate over unconditioned 3002 lines for a signal-to-noise ratio of 26 dB, with a received signal level of -20 dBm.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of -20 dBm as illustrated.

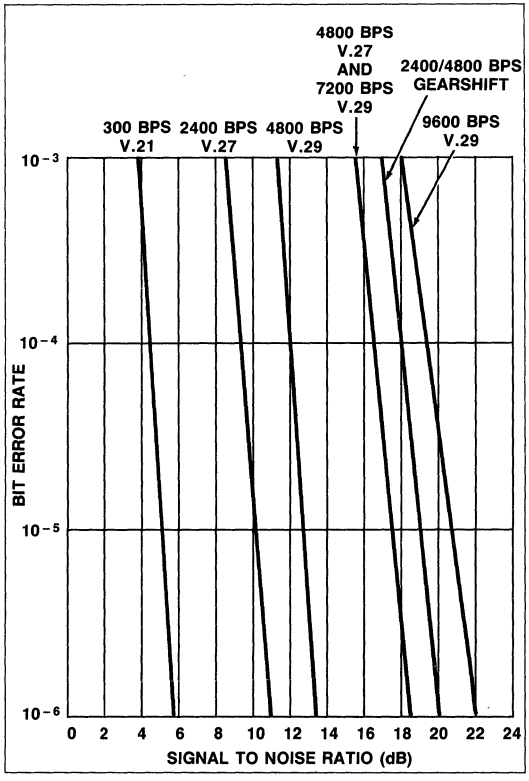
PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz, or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

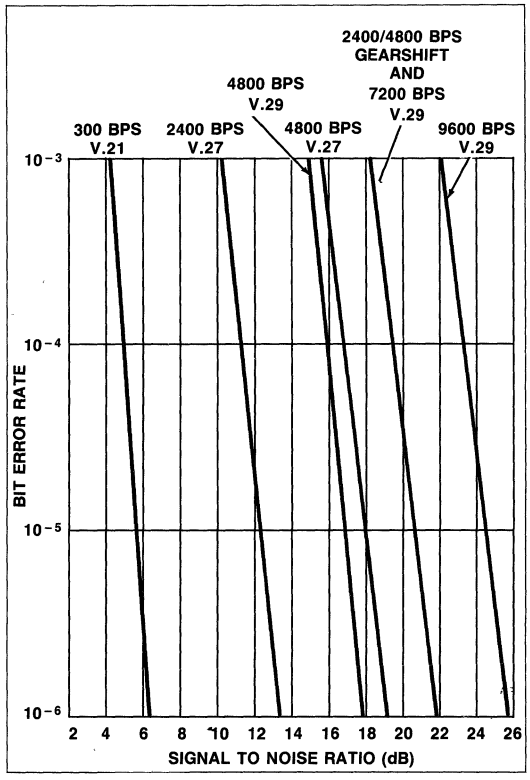
At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

An example of the BER performance capabilities is given in the following diagrams:

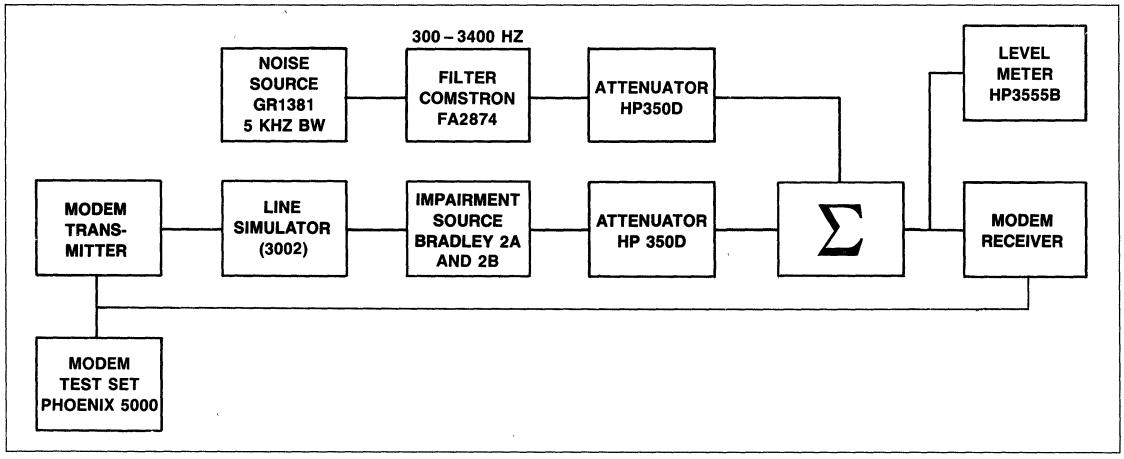


Typical BER Performance
Back-to-Back, –20 dBm Receive Signal Level



Typical BER Performance
3002 Unconditioned Line, –20 dBm Receive Signal Level

The BER performance test set-up is shown in the following diagram:



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	550 mA	<700 mA
+12 Vdc	±5%	20 mA	< 30 mA
−12 Vdc	±5%	50 mA	< 80 mA

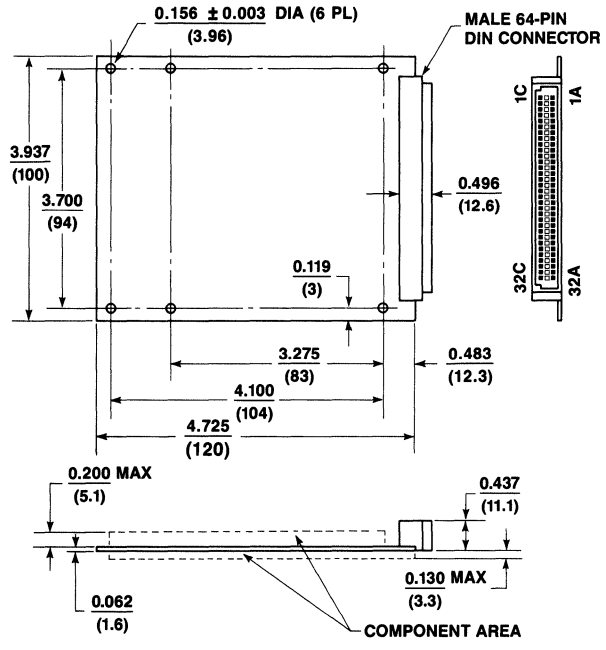
Note: All voltages must have ripple ≤0 1 volts peak-to-peak.

Modem Environmental Restrictions

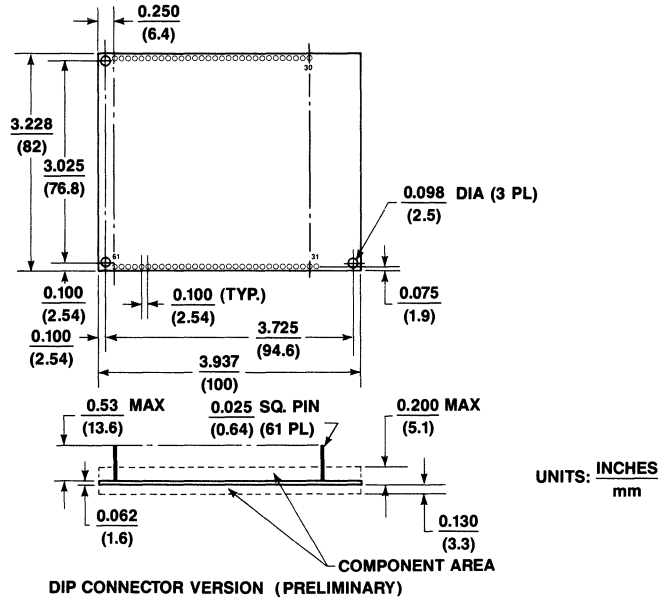
Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity.	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less
Altitude	−200 feet to +10,000 feet

Modem Mechanical Considerations

Parameter	Specification
DIN Connector Version	
Board Structure:	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male, or 6 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating connector: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
Dimensions:	
Width	3.937 in (100 mm)
Length	4.725 in. (120 mm)
Height	0.40 in. (10.2 mm)
Weight (max):	3.6 oz (100 g)
Lead Extrusion (max):	0.100 in. (2 54 mm)
DIP Connector Version	
Board Structure:	Single PC board with a row of 30 pins and a row of 31 pins in a dual in-line pin configuration.
Dimensions:	
Width	3.937 in (100 mm)
Length	3.228 in (82 mm)
Height	0 2 in. (5.08 mm) above, 0.13 in. (3.30 mm) below
Weight (max.):	3 6 oz (100 g)
Pin Length (max.)	0.53 in (13 5 mm)



DIN CONNECTOR VERSION



DIP CONNECTOR VERSION (PRELIMINARY)

R96FT Modem Dimensions and Pin Locations

Rockwell

R96FT/SC
9600 bps Fast Train Modem with Forward Secondary Channel

INTRODUCTION

The Rockwell R96FT/SC is a synchronous serial 9600 bps modem containing a 75 bps asynchronous FSK forward channel. This modem is designed for multipoint and networking applications. The R96FT/SC allows full-duplex operation over 4-wire dedicated unconditioned lines, or half-duplex operation over the general switched telephone network.

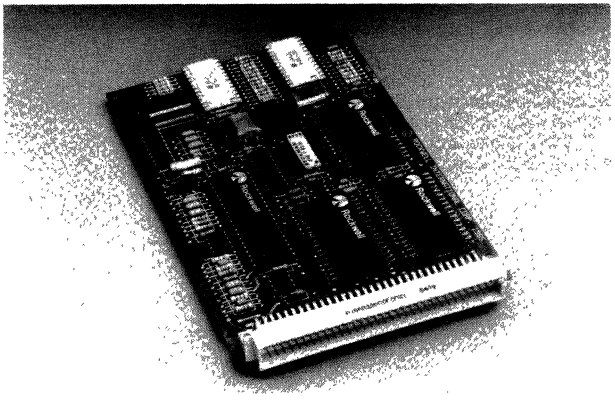
Proprietary fast train configurations provide training times of 23 ms for V.29FT/9600/7200/4800, 22 ms for V.27FT/4800, and 30 ms for V.27FT/2400. A 2400/4800 bps Gearshift configuration provides a training time of 10 ms. For applications requiring operation with international standards, fallback configurations compatible with CCITT Recommendations V.29 and V.27 bis/ter are provided. A 300 bps FSK configuration, compatible with CCITT V.21 Channel 2, is also provided.

The small size and low power consumption of the R96FT/SC offer the user flexibility in formulating a 9600 bps modem design customized for specific packaging and functional requirements.

This data sheet corresponds to assembly number TR96-D500-021.

FEATURES

- Proprietary Fast Train
- 75 bps Forward Channel
- 2400/4800 bps Gearshift
- User Compatibility:
  - — CCITT V.29, V.27 bis/ter and V.21 Channel 2
- Train on Data
- Full-Duplex (4-Wire)
- Half-Duplex (2-Wire)
- Programmable Tone Generation
- Dynamic Range –43 dBm to –5 dBm
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
  - — Compromise Link (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Loopbacks
  - — Local Analog (V.54 Loop 3)
  - — Remote Analog (Locally Activated)
  - — Remote Digital (Locally Activated V.54 Loop 2)
- Small Size
  - — 100 mm x 160 mm (3.94 in. x 6.3 in.)
- Low Power Consumption
  - — 4 watts, typical
- Programmable Transmit Output Levels for Primary Channel and Forward Channel
- TTL and CMOS Compatible



R96FT/SC Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER CARRIER FREQUENCIES

Function	Frequency (Hz ±0.01%)
V.27 bis/ter Carrier	1800
V 27 FT Carrier	1800
2400/4800 bps Gearshift	1800
V.29 Carrier	1700
V.29 FT Carrier	1700*
V 21 Channel 2:	
Mark	1650
Space	1850

*1800 when used in conjunction with 75 bps Forward Channel.

TONE GENERATION

Under control of the host processor, the R96FT/SC can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

SIGNALING AND DATA RATES

Parameter	Specification (±0.01%)
Signaling Rate: Data Rate:	2400 baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate Data Rate:	1600 baud 4800 bps
Signaling Rate: Data Rate: Gearshift Data Rate:	1200 baud 2400 bps 2400/4800 bps
Signaling Rate: Data Rate:	300 baud 300 bps
Signaling Rate: Data Rate:	75 baud 75 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 bis/ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 bis/ter.

For the Gearshift Configuration, the signaling rate is 1200 baud. The 2400 bps data stream is encoded into dibits forming a 4-point structure, and the 4800 bps data stream is encoded into quadbits forming a 16-point structure. The first 32 bauds of data are transmitted at 2400 bps and the remaining message is transmitted at 4800 bps.

At 300 baud, the 300 bps data stream is encoded per CCITT V.21 channel 2 into a mark frequency of 1650 Hz and a space frequency of 1850 Hz.

At 75 baud, the 75 bps data stream is encoded to a mark frequency of 356 Hz and a space frequency of 300 Hz.

EQUALIZERS

The R96FT/SC provides equalization functions that improve performance when operating over low quality lines.

Cable Equalizers — Selectable compromise cable equalizers in the receiver and transmitter are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Equalizers — Selectable compromise link equalizers in the receiver optimize performance over channels exhibiting severe amplitude and delay distortion. Two standards are provided: U.S. survey long and Japanese 3-link.

Automatic Adaptive Equalizer — An automatic adaptive T equalizer is provided in the receiver circuit.

TRANSMITTED DATA SPECTRUM

If the cable equalizer is not enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

NOTE

When used with the 75 bps Forward Channel the 2400 Baud filter is narrower.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96FT/SC incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 bis/ter or V.29 depending on the selected configuration.

The scrambler/descrambler facilities for Gearshift can be selected to be in accordance with either V.27 bis/ter or V.29. The scrambler/descrambler selection is made by writing the appropriate configuration codes into the transmitter and receiver.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R96FT/SC can adapt to received frequency error of up to ±10 Hz with less than 0.2 dB degradation in BER performance.

During fast train polling, frequency offset must be less than ±2 Hz for successful training.

RECEIVE LEVEL

The receiver circuit of the modem satisfies all specified performance requirements for received line signal levels from –5 dBm to –43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING (Synchronous Configurations)

The R96FT/SC provides a data derived Receive Data Clock ($\overline{\text{RDCLK}}$) output in the form of a squarewave. The low-to-high transitions of this output coincide with the centers of received data bits. For the Gearshift Configuration, the first 32 bauds of data are at 2400 bps followed by 4800 bps data for the remaining message. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. $\overline{\text{RDCLK}}$ duty cycle is 50% ±1%.

TRANSMIT LEVEL

The main channel output level is accurate to ±1.0 dB and is programmable from –1.0 dBm to –15.0 dBm in 2 dB steps.

The forward channel transmit level is set relative to the main channel as –6 dB, –10 dB, –14 dB, or –18 dB.

TRANSMIT TIMING (Synchronous Configurations)

The R96FT/SC provides a Transmit Data Clock (TDCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400 or 300 Hz (±0.01%). For the Gearshift Configuration, TDCLK is a 2400 Hz clock for the first 32 bauds of data, and a 4800 Hz clock for the remaining message.
2. *Duty Cycle.* 50% ±1%

Input data presented on TXD is sampled by the R96FT/SC at the low-to-high transition of TDCLK. Data on TXD must be stable for at least one microsecond prior to the rising edge of TDCLK and remain stable for at least one microsecond after the rising edge of TDCLK.

EXTERNAL TRANSMIT CLOCK

The transmitter data clock (TDCLK) can be phase locked to a signal on input XTCLK. This input signal must equal the desired data rate ±0.01% with a duty cycle of 50% ±20%.

TRAIN ON DATA

When train on data is enabled (by setting a bit in the interface memory), the modem monitors the EQM signal. If EQM indicates a loss of equalization (i.e., BER approximately 10^{-3} for 0.5 seconds) the modem attempts to retrain on the data stream. The time for retrain is typically 3 to 15 seconds.

TURN-ON SEQUENCE

A total of 20 selectable turn-on sequences can be generated as defined in the following table:

No.	V.29 (bps)	V.27 bis/ter (bps)	Gearshift (bps)	RTS-CTS Response Time (milliseconds)	Comments
1	FT/9600			23	
2	FT/7200			24	Proprietary
3	FT/4800			23	Fast Train
4		FT/4800		22	
5		FT/2400		30	
6	9600			253	
7	7200			253	
8	4800			253	
9		4800 long		708	
10		2400 long		943	
11		4800 short		50	
12		2400 short		67	
13			2400/4800	10	
14	9600			438	Preceded[1]
15	7200			438	by Echo
16	4800			438	Protector
17		4800 long		913	Tone for
18		2400 long		1148	lines using
19		4800 short		255	echo
20		2400 short		272	suppressors.

1 For short echo protector tone, subtract 155 ms from values of RTS-CTS response time.
2. V.21 (300 bps FSK) RTS-CTS response time is <35 ms
3. 75 bps forward channel SCRTS-SCCTS response time is <500 ms.

TURN-OFF SEQUENCE

For V.27bis/ter, V.27FT and 2400/4800 bps Gearshift configurations, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy (V.27 bis/ter only). For V.29 and V.29FT, the turn-off sequence consists of approximately 8 ms of remaining data and scrambled ones.

CLAMPING

Received Data (RXD) is clamped to a constant mark (one) when the Received Line Signal Detector (RLSD) is off.

RESPONSE TIMES OF CLEAR TO SEND (CTS)

The time between the off-to-on transition of Request To Send (RTS) and the off-to-on transition of Clear to Send (CTS) is dictated by the length of the training sequence and the echo protector tone, if used. These times are given in the Turn-On Sequences table. If training is not enabled, RTS/CTS delay is less than 2 baud times.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RESPONSE TIMES OF FORWARD CHANNEL CLEAR TO SEND (SCCTS)

SCRTS/SCCTS response times vary according to the transmit level set by the SCTLVL field.

SCTLVL (0:9:0-1)	TX Level Relative to Primary	SCCTS Response Time (ms)
0	-6 dB	378
1	-10 dB	238
2	-14 dB	150
3	-18 dB	95

RECEIVE LINE SIGNAL DETECTOR (RLSD)

Response

For Fast Train and Gearshift configurations, the receiver enters the training state upon detecting a significant increase in the received signal power. If the received line signal power is greater than the selected threshold level at the end of the training state, the receiver enters the data state and RLSD is activated. If the received line signal power is less than the selected threshold level at the end of the training state, the receiver returns to the idle state and RLSD is not activated.

Also, in Fast Train and Gearshift configurations, the receiver initiates the turn-off delay upon detecting a significant decrease in the received signal power. If the received signal power is less than the selected threshold at the end of the turn-off delay, the receiver enters the idle state and RLSD is deactivated. If the received signal power is greater than the selected threshold at the end of the turn-off delay, the receiver returns to the data state and RLSD is left active.

For CCITT configurations, the receiver enters the training detection state when the received line signal power crosses the selected threshold level. RLSD is activated at the end of the training sequence. For V.21 Channel 2, a separate received line signal detector (FRLSD) is provided. FRLSD is activated when energy above -43 dBm is present at the receiver's audio input (RXA). The FRLSD off-to-on response time is 15 ±5 ms and the on-to-off response time is 25 ±5 ms.

The RLSD on-to-off response times are:

Configuration	Response Time (ms)
V 29 Fast Train	6.5 ±1
V.27 Fast Train	8 ±1
Gearshift	6 ±1
V.29	30 ±9
V.27 bis/ter	10 ±5

RLSD response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

Threshold Options

Four threshold options are provided:

1. Greater than −43 dBm ($\overline{RLSD}$ on)
   Less than −48 dBm ($\overline{RLSD}$ off)
2. Greater than −33 dBm ($\overline{RLSD}$ on)
   Less than −38 dBm ($\overline{RLSD}$ off)
3. Greater than −26 dBm ($\overline{RLSD}$ on)
   Less than −31 dBm ($\overline{RLSD}$ off)
4. Greater than −16 dBm ($\overline{RLSD}$ on)
   Less than −21 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

For CCITT configurations, a minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

FORWARD CHANNEL SIGNAL DETECTOR ($\overline{SCRLSD}$)

Response

Signal Level	$\overline{SCRLSD}$ Turn-On (ms)	$\overline{SCRLSD}$ Turn-Off (ms)
−7 dBm	140 ± 10	800 ± 10
−48 dBm	340 ± 10	550 ± 10

Threshold

The $\overline{SCRLSD}$ Turn-On threshold is −54 dBm. The $\overline{SCRLSD}$ Turn-Off threshold is −58 dBm.

MODES OF OPERATION

The R96FT/SC is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

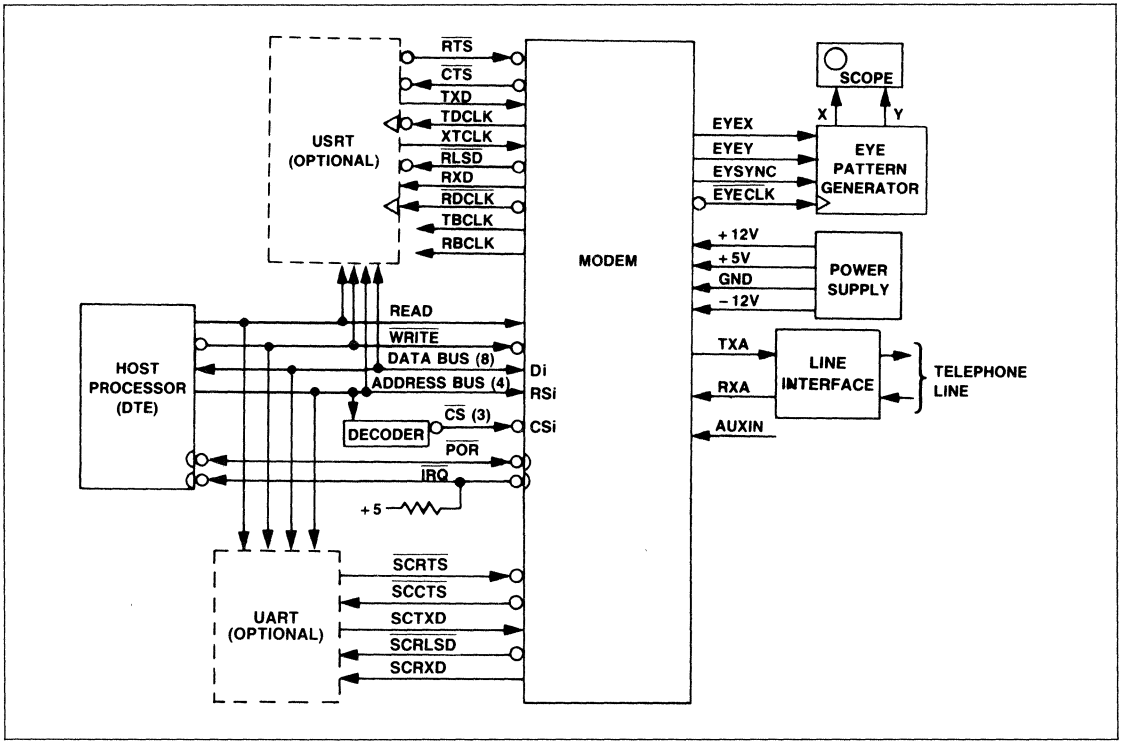
The R96FT/SC has the capability of transferring channel data (up to eight bits at a time) via the microprocessor bus.

MODE SELECTION

For the transmitter, a control bit determines whether the source of transmitted data is the V.24 interface (serial mode) or the parallel transmitter data register (parallel mode). The transmitter automatically defaults to the serial mode at power-on.

The receiver simultaneously outputs received data via the V.24 interface and the parallel receiver data register.

In either parallel or serial mode the R96FT/SC is configured by the host processor via the microprocessor bus.



R96FT/SC Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 64-pin DIN connector. Software circuits are assigned to specific bits in a 48-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R96FT/SC Hardware Circuits table. In the table, the column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R96FT/SC Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground (A)	AGND	31C,32C	Analog Ground Return
Ground (D)	DGND	3C,8C,5A,10A	Digital Ground Return
+5 volts	PWR	19C,23C,26C,30C	+5 Vdc supply
+12 volts	PWR	15A	+12 Vdc supply
−12 volts	PWR	12A	−12 Vdc supply
POR	I/OB	13C	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	1C	Data Bus (8 Bits)
D6	I/OA	1A	
D5	I/OA	2C	
D4	I/OA	2A	
D3	I/OA	3A	
D2	I/OA	4C	
D1	I/OA	4A	
D0	I/OA	5C	
RS3	IA	6C	Register Select (4 Bits)
RS2	IA	6A	
RS1	IA	7C	
RS0	IA	7A	
$\overline{CS0}$	IA	10C	Chip Select—Transmitter Device
$\overline{CS1}$	IA	9C	Chip Select—Receiver Sample Rate Device
$\overline{CS2}$	IA	9A	Chip Select—Receiver Baud Rate Device
READ	IA	12C	Read Enable
WRITE	IA	11A	Write Enable
IRQ	OB	11C	Interrupt Request
C. V.24 INTERFACE:			
RDCLK	OC	21A	Receive Data Clock
TDCLK	OC	23A	Transmit Data Clock
XTCLK	IB	22A	External Transmit Clock
RTS	IB	25A	Request to Send
CTS	OC	25C	Clear to Send
TXD	IB	24C	Transmitter Data
RXD	OC	22C	Receiver Data
RLSD	OC	24A	Received Line Signal Detector
SCRTS	IB	21C	Forward Channel RTS
SCCTS	OC	20A	Forward Channel CTS
SCTXD	IB	19A	Forward Channel TXD
SCRLSD	OD	20C	Forward Channel RLSD
SCRXD	OD	18A	Forward Channel RXD
D. ANCILLARY CIRCUITS:			
RBCLK	OC	26A	Receiver Baud Clock
TBCLK	OC	27C	Transmitter Baud Clock
FRXD	OD	16A	FSK Receiver Data (inverted data)
FRLSD	OD	17C	FSK Received Line Signal Detector
E. ANALOG SIGNALS:			
TXA	AA	31A	Transmitter Analog Output
RXA	AB	32A	Receiver Analog Input
AUXIN	AC	30A	Auxiliary Analog Input

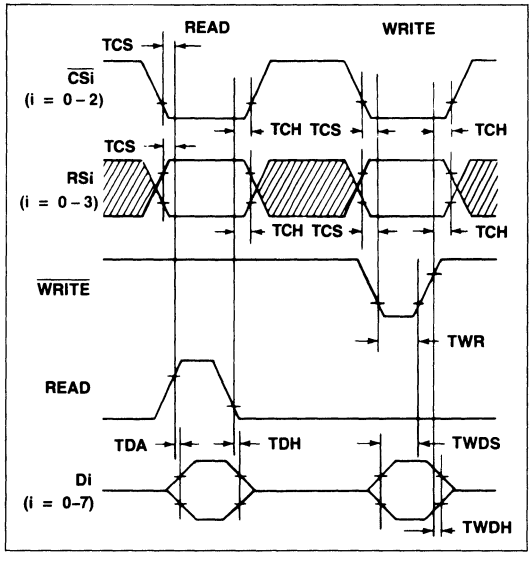
R96FT/SC Hardware Circuits (Continued)

Name	Type	Pin No.	Description
F. DIAGNOSTIC:			
EYEX	OC	15C	Eye Pattern Data—X Axis
EYEY	OC	14A	Eye Pattern Data—Y Axis
EYECLK	OA	14C	Eye Pattern Clock
EYESYNC	OA	13A	Eye Pattern Synchronizing Signal

Eye Pattern Generation

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the EYECLK output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

Microprocessor Timing



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CSi}$, RSi setup time prior to Read or Write	TCS	30	—	nsec
Data access time after Read	TDA	—	140	nsec
Data hold time after Read	TDH	10	50	nsec
$\overline{CSi}$, RSi hold time after Read or Write	TCH	10	—	nsec
Write data setup time	TWDS	75	—	nsec
Write data hold time	TWDH	10	—	nsec
Write strobe pulse width	TWR	75	—	nsec

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type								
			IA	IB	IC	OA	OB	OC	OD	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 Min.	2.0 Min.	2.0 Min.					2.0 Min.	5 25 Max. 2.0 Min.
V_{IL}	Input Voltage, Low	V	0.8 Max	0.8 Max.	0.8 Max.					0.8 Max.	0.8 Max.
V_{OH}	Output Voltage, High	V				2.4 Min.[1]			2 2 Min. [6]	2.4 Min.[1]	2 4 Min.[3]
V_{OL}	Output Voltage, Low	V				0.4 Max.[2]	0.4 Max [2]	0.4 Max.[2]	0.6 Max.[7]	0.4 Max.[2]	0.4 Max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 Max.							±2.5 Max.[4]	
I_{OH}	Output Current, High	mA				−0.1 Max.					
I_{OL}	Output Current, Low	mA				1.6 Max.	1.6 Max.	1.6 Max.			
I_L	Output Current, Leakage	μA					±10 Max.				
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 Max. −10 Min.	−240 Max. −10 Min			−240 Max. −10 Min.			−260 Max. −100 Min.
C_L	Capacitive Load	pF	5	5	20					10	40
C_D	Capacitive Drive	pF				100	100	100		100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open-Drain w/Pull-up	TTL	3-State Transceiver	Open-Drain w/Pull-up

Notes 1. I Load = −100 μA
2. I Load = 1.6 mA
3. I Load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I Load = 0.36 mA
6. I Load = −400 μA
7 I Load = 2.0 mA

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output impedance is 604 ohms ±1%
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is TLVL setting +0.6 dB −1.4 dB. If unused, this input must be grounded near the modem connector. If used, it must be driven from a low impedance source.

SOFTWARE CIRCUITS

The R96FT/SC comprises three signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 1 update at half the modem sample rate (4800 bps). Registers in chip 0 and 2 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0–2), the register by Z(0–F), and the bit by Q(0–7, 0 = LSB).

Status Control Bits

The operation of the R96FT/SC is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a dash (—) are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R96FT/SC provides the user with access to much of the data stored in the modem's memories. This data is useful for performing certain diagnostic functions.

Two RAM access registers in chip 2 allow user access to RAM locations via the X word registers (2:3 and 2:2) and the Y word register (2:1 and 2:0). The access code stored in RAM ACCESS X (2:5) selects the source of data for RAM DATA XM and RAM DATA XL (2:3 and 2:2). Similarly, the access code stored in RAM ACCESS Y (2:4) selects the source of data for RAM DATA YM and RAM DATA YL (2:1 and 2:0).

Reading of diagnostic RAM data is performed by storing the necessary access codes in 2:5 and 2:4, reading 2:0 to reset the associated data available bit (2:E:0), then waiting for the data available bit to return to a one. Data is now valid and may be read from 2:3 through 2:0.

An additional diagnostic is supplied by the sample rate processor (chip 1). Registers 1:2 and 1:3 supply a 16 bit AGC Gain Word. These two diagnostic data registers are updated at the sample rate during the data state and may be read by the host processor asynchronously.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

Baud Rate Processor (Chip 2) RAM Access Codes

No.	Function	X Access	Y Access	Register
1	Equalizer Input	C0	40	0,1,2,3
2	Equalizer Tap Coefficients	81–A0	01-20	0,1,2,3
3	Unrotated Equalizer Output	E1	61	0,1,2,3
4	Rotated Equalizer Output	E2	62	0,1,2,3
5	Decision Points (Ideal Data Points)	E8	68	0,1,2,3
6	Error Vector	E5	65	0,1,2,3
7	Rotation Angle	A7	Not Used	2,3
8	Frequency Correction	A5	Not Used	2,3
9	Eye Quality Monitor (EQM)	AC	Not Used	2,3

Transmitter Interface Memory Chip 0 ($\overline{CS0}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	TIA	—	—	—	TSB	TIE	—	TBA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	FSKT	ASCR	PCF	SCRTS	CF	DDEE	SCTLVL	
8	—	—	—	—	—	—	—	—
7	RTS	TTDIS	SDIS	MHLD	EPT	TPDM	XCEN	SEPT
6	TRANSMITTER CONFIGURATION							
5	—	—	CEQ		LAEN	LDEN	A3L	D3L
4	L3ACT	L4ACT	L4HG	TLVL			L2ACT	LCEN
3	FREQM							
2	FREQL							
1	—	—	—	—	—	—	—	—
0	TRANSMITTER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

Receiver Interface Memory Chip 1 ($\overline{CS1}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RIA	—	—	—	RSB	RIE	—	RDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	$\overline{FED}$	—	—	—	$\overline{CDET}$	—	—
8	—	—	—	—	$\overline{P2DET}$	—	—	—
7	RTH		DDIS	—	—	SCEN	RDIS	—
6	TOD	RECEIVER CONFIGURATION						
5	—	—	—	—	—	—	—	—
4	—	—	—	—	—	—	—	—
3	AGC GAIN WORD (MSB)							
2	AGC GAIN WORD (LSB)							
1	—	—	—	—	—	—	—	—
0	RECEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only

Receiver Interface Memory Chip 2 ($\overline{CS2}$)

Bit / Register	7	6	5	4	3	2	1	0
F	—	—	—	—	—	—	—	—
E	RBIA	—	—	—	—	RBIE	—	RBDA
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RAM ACCESS X							
4	RAM ACCESS Y							
3	RAM DATA XM							
2	RAM DATA XL							
1	RAM DATA YM							
0	RAM DATA YL							
Register / Bit	7	6	5	4	3	2	1	0

NOTE
(—) indicates reserved for modem use only.

R96FT/SC Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
ASCR	Append Scrambled Ones	0:9:6	When control bit ASCR is a one, one baud of scrambled marks is included in the V.29FT and V.27FT training sequences. The $\overline{\text{RTS}}$-$\overline{\text{CTS}}$ delay is thus extended by one baud period when ASCR is a one.
A3L	Amplitude 3-Link Select	0:5:1	See LAEN.
$\overline{\text{CDET}}$	Carrier Detector	1:9:2	When zero, status bit $\overline{\text{CDET}}$ indicates that passband energy is being detected, and that a training sequence is not in process. $\overline{\text{CDET}}$ goes to a zero at the start of the data state, and returns to a one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
CEQ	Cable Equalizer Field	0:5:(4,5)	The CEQ Control field simultaneously controls amplitude compromise equalizers in both the transmit and receive paths. The following table lists the possible cable equalizer selection codes: **CEQ** — **Cable Length (0.4 mm diameter)** 0 — 0.0 1 — 1.8 km 2 — 3.6 km 3 — 7.2 km
CF	Carrier Frequency	0:9:3	When control bit CF is a one, the transmitter carrier frequency for V.29FT changes from 1700 Hz to 1800 Hz.
DDEE	Digital Delay Equalizer Enable	0:9:2	When control bit DDEE is a one, a fourth order digital delay equalizer is inserted in the transmit path.
DDIS	Descramble Disable	1:7:5	When control bit DDIS is a one, the receiver descrambler circuit is removed from the data path.
D3L	Delay 3-Link Select	0:5:0	See LDEN.
EPT	Echo Protector Tone	0:7:3	When control bit EPT is a one, an unmodulated carrier is transmitted for 185 ms (optionally 30 ms) followed by 20 ms of no transmitted energy at the start of transmission. This option is available in the V.27 and V.29 Configurations, although it is not specified in the CCITT V.29 recommendation.
$\overline{\text{FED}}$	Fast Energy Detector	1:9:6	When status bit $\overline{\text{FED}}$ is a zero, it indicates that energy above the receiver threshold is present in the passband.
(None)	FREQL/FREQM	0:2:0–7, 0:3:0–7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below: *FREQM Register (0:3)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* **Bit:** 7 6 5 4 3 2 1 0 **Data Word:** 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01% Hexadecimal frequency numbers (FREQL, FREQM) for commonly generated tones are given below: **Frequency (Hz)** — **FREQM** — **FREQL** 462 — 0C — 52 1100 — 1D — 55 1650 — 2C — 00 1850 — 31 — 55 2100 — 38 — 00

R96FT/SC Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
FSKT	FSK Transmitter Configuration	0 9·7	The V.21 Channel 2 (300 bps synchronous FSK) transmitter configuration is selected by setting the FSKT control bit to a one (see TSB). While set to a one, this control bit overrides the configuration selected by the control code in register 0:6. The FSK data may be transmitted in parallel mode or in serial mode (see TPDM).
LAEN	Link Amplitude Equalizer Enable	0·5:3	The link amplitude equalizer enable and select bits control an amplitude compromise equalizer in the receive path according to the following table: **LAEN / A3L / Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
LCEN	Loop Clock Enable	0:4:0	When control bit LCEN is a one, the transmitter clock tracks the receiver clock.
LDEN	Link Delay Equalizer Enable	0:5·2	The link delay equalizer enable and select bits control a delay compromise equalizer in the receive path according to the following table: **LDEN / D3L / Curve Matched** 0 / X / No Equalizer 1 / 0 / U.S. Survey Long 1 / 1 / Japanese 3-Link
L2ACT	Remote Digital Loopback Activate	0.4:1	When control bit L2ACT is a one, the receiver digital output is connected to the transmitter digital input in accordance with CCITT Recommendation V.54 loop 2.
L3ACT	Local Analog Loopback Activate	0:4:7	When control bit L3ACT is a one, the transmitter analog output is coupled to the receiver analog input through an attenuator in accordance with CCITT Recommendation V.54 loop 3.
L4ACT	Remote Analog Loopback Activate	0.4:6	When control bit L4ACT is a one, the receiver analog input is connected to the transmitter analog output through a variable gain amplifier in a manner similar to CCITT Recommendation V.54 loop 4.
L4HG	Loop 4 High Gain	0:4·5	When control bit L4HG is a one, the loop 4 variable gain amplifier is set for +16 dB, and when at zero the gain is zero dB.
MHLD	Mark Hold	0:7·4	When control bit MHLD is a one, the transmitter input data stream is forced to all marks (ones).
PCF	Primary Channel Filter	0·9:5	When control bit PCF is a one, the 2400 baud primary channel transmitter filter is set to a narrower bandwidth than normal.
$\overline{\text{P2DET}}$	Period 2 Detector	1:8:3	When status bit $\overline{\text{P2DET}}$ is a zero, it indicates that a period 2 sequence has been detected. This bit sets to a one at the start of the period N sequence. This bit is only significant for CCITT V.29 and V.27 bis/ter configurations.
(None)	RAM Access X	2:5:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word X (2:3 and 2:2).
(None)	RAM Access Y	2.4:0–7	Contains the RAM access code used in reading chip 2 RAM locations via word Y (2:1 and 2:0).
(None)	RAM Data XL	2:2:0–7	Least significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data XM	2:3:0–7	Most significant byte of 16-bit word X used in reading RAM locations in chip 2.
(None)	RAM Data YL	2:0:0–7	Least significant byte of 16-bit word Y used in reading RAM locations in chip 2.
(None)	RAM Data YM	2:1:0–7	Most significant byte of 16-bit word Y used in reading RAM locations in chip 2
RBDA	Receiver Baud Data Available	2:E·0	Status bit RBDA goes to a one when the receiver writes data into register 2:0 The bit goes to a zero when the host processor reads data from register 2:0.
RBIA	Receiver Baud Interrupt Active	2:E·7	This status bit is a one whenever the receiver baud rate device is driving $\overline{\text{IRQ}}$ low.
RBIE	Receiver Baud Interrupt Enable	2:E:2	When the host processor writes a one in the RBIE control bit, the $\overline{\text{IRQ}}$ line of the hardware interface is driven to zero when status bit RBDA is a one.

R96FT/SC Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Receiver Configuration</td><td>1 6 0–6</td><td>The host processor configures the receiver by writing a control code into the receiver configuration field in the interface memory space (see RSB)

Note: The receiver must be disabled prior to changing configurations See RDIS.

Receiver Configuration Control Codes

Control codes for the modem receiver configuration are:
<table>
<tr><th colspan="2">Configuration</th><th rowspan="2">Configuration Code (Hex)</th></tr>
<tr><th>V29</th><th>V27 bis/ter</th></tr>
<tr><td>FT/9600
FT/7200
FT/4800</td><td>

FT/4800
FT/2400</td><td>1C
1A
19
0A
09</td></tr>
<tr><td>9600
7200
4800</td><td>

4800 long
2400 long
4800 short
2400 short</td><td>14
12
11
22
21
02
01</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.29 descrambler
2400/4800 bps Gearshift/V.27 bis/ter descrambler</td><td>61[1]
41[1]</td></tr>
<tr><td colspan="2">V 21 Channel 2</td><td>See Note 2</td></tr>
</table>
1. The Receiver Configuration code automatically changes from a hex 61 (or hex 41) to a hex 64 (or hex 44) when the receiver transitions from the 2400 bps data state to the 4800 bps data state.
2. The FSK receiver is active at all times. Two ancillary hardware circuits, $\overline{\text{FRLSD}}$ and $\overline{\text{FRXD}}$, are supplied for FSK message reception. $\overline{\text{FRLSD}}$ is described under the Received Line Signal Detector section. $\overline{\text{FRXD}}$ provides inverted FSK received data. Timing extraction must be performed on the $\overline{\text{FRXD}}$ signal externally as no FSK receiver data clock is provided by the R96FT/SC.</td></tr>
<tr><td>(None)</td><td>Receiver Data</td><td>1:0:0–7</td><td>The host processor obtains channel data from the receiver in the parallel data mode by reading a data byte from the receiver data register. The data is divided on baud boundaries as is the transmitter data.</td></tr>
<tr><td>RDA</td><td>Receiver Data Available</td><td>1:E 0</td><td>Status bit RDA goes to a one when the receiver writes data to register 1:0. RDA goes to a zero when the host processor reads data from register 1:0.</td></tr>
<tr><td>RDIS</td><td>Receiver Disable</td><td>1·7:1</td><td>When control bit RDIS is a one, the receiver is disabled, $\overline{\text{RLSD}}$ is turned off and RXD is clamped to all marks. This bit can be used to squelch the receiver during half duplex transmissions over two wires. This bit must be set to a one prior to changing the receiver configuration.</td></tr>
<tr><td>RIA</td><td>Receiver Interrupt Active</td><td>1:E:7</td><td>This status bit is a one whenever the receiver sample rate device is driving $\overline{\text{IRQ}}$ to zero.</td></tr>
<tr><td>RIE</td><td>Receiver Interrupt Enable</td><td>1:E:2</td><td>When the host processor writes a one in the RIE control bit, the $\overline{\text{IRQ}}$ line of the hardware interface is driven to zero when status bit RDA is a one.</td></tr>
<tr><td>RSB</td><td>Receiver Setup Bit</td><td>1:E:3</td><td>When the host processor changes the receiver configuration, the FSKR bit or the RTH field, the host processor must write a one in the RSB control bit. RSB goes to zero when the changes become effective.</td></tr>
<tr><td>RTH</td><td>Receiver Threshold Field</td><td>1:7:6,7</td><td>The receiver energy detector threshold is set by the RTH field according to the following codes (see RSB):
<table>
<tr><th>RTH</th><th>$\overline{\text{RLSD}}$ On</th><th>$\overline{\text{RLSD}}$ Off</th></tr>
<tr><td>0</td><td>> –43 dBm</td><td>< –48 dBm</td></tr>
<tr><td>1</td><td>> –33 dBm</td><td>< –38 dBm</td></tr>
<tr><td>2</td><td>> –26 dBm</td><td>< –31 dBm</td></tr>
<tr><td>3</td><td>> –16 dBm</td><td>< –21 dBm</td></tr>
</table></td></tr>
</table>

R96FT/SC Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
RTS	Request-to-Send	0 7 7	When control bit RTS goes to a one, the modem begins a transmit sequence It continues to transmit until RTS is reset to zero, and the turn-off sequence has been completed. This input bit parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem.
SCEN	Forward Channel Enable	1·7:2	When control bit SCEN is a one, the forward channel demodulator is enabled and the primary channel receiver carrier frequency is changed from 1700 to 1800 Hz in V.29 FT configurations.
SCRTS	Forward Channel Request-to-Send	0:9·4	When control bit SCRTS is a one, the modem begins a forward channel transmit sequence. Transmission continues until SCRTS is a zero. SCRTS in the interface memory is ORed with signal $\overline{SCRTS}$ on the card connector.
SCTLVL	Forward Channel Transmit Level	0:9:0-1	The forward channel transmit level is set relative to the main channel transmit level by the following SCTLVL codes: **SCTLVL Code** / **Forward Channel Transmit Level Relative to Primary Channel** 0 / −6 dB 1 / −10 dB 2 / −14 dB 3 / −18 dB
SDIS	Scrambler Disable	0:7·5	When control bit SDIS is a one, the transmitter scrambler circuit is removed from the data path.
SEPT	Short Echo Protector Tone	0 7:0	When control bit SEPT is a one, the echo protector disable tone is 30 ms long rather than 185 ms. (See TSB.)
TBA	Transmitter Buffer Available	0 E·0	This status bit resets to zero when the host processor writes data to transmitter data register 0:0. When the transmitter empties register 0:0, this bit sets to a one.
TIA	Transmitter Interrupt Active	0:E:7	This status bit is a one whenever the transmitter is driving $\overline{IRQ}$ to a zero.
TIE	Transmitter Interrupt Enable	0:E:2	When the host processor writes a one in control bit TIE, the $\overline{IRQ}$ line of the hardware interface is driven to zero when status bit TBA is at a one.
TLVL	Transmitter Level Field	0:4:2–4	The transmitter analog output level is determined by eight TLVL codes, as follows: **TLVL** / **Transmitter Analog Output*** 0 / −1 dBm ±1 dB 1 / −3 dBm ±1 dB 2 / −5 dBm ±1 dB 3 / −7 dBm ±1 dB 4 / −9 dBm ±1 dB 5 / −11 dBm ±1 dB 6 / −13 dBm ±1 dB 7 / −15 dBm ±1 dB *Each step above is a 2 dB change ±0.2 dB.
TOD	Train-On-Data	1:6:7	When control bit TOD is a one, it enables the train-on-data algorithm to converge the equalizer if the signal quality degrades sufficiently. When TOD is a one, the modem still recognizes a training sequence and enters the force train state. A BER of approximately 10^{-3} for 0.5 seconds initiates train-on-data
TPDM	Transmitter Parallel Data Mode	0:7:2	When control bit TPDM is a one, the transmitter accepts data for transmission from the transmitter data register (0:0) rather than the serial hardware data input

R96FT/SC Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>Transmitter Configuration</td><td>0:6:0–7</td><td>The host processor configures the transmitter by writing a control byte into the transmitter configuration register in its interface memory space. (See TSB.)

Transmitter Configuration Control Codes

Control codes for the modem transmitter configurations are:
<table>
<tr><th colspan="2">Configuration</th><th rowspan="2">Configuration Code (Hex)</th></tr>
<tr><th>V29</th><th>V27 bis/ter</th></tr>
<tr><td>FT/9600
FT/7200
FT/4800</td><td>

FT/4800
FT/2400</td><td>1C
1A
19
0A
09</td></tr>
<tr><td>9600
7200
4800</td><td>

4800 long
2400 long
4800 short
2400 short</td><td>14
12
11
22
21
02
01</td></tr>
<tr><td colspan="2">2400/4800 bps Gearshift/V.29 Scrambler
2400/4800 bps Gearshift/V.27 bis/ter Scrambler</td><td>61
41</td></tr>
<tr><td colspan="2">V.21 Channel 2</td><td>See FSKT</td></tr>
<tr><td colspan="2">Tone transmit</td><td>80</td></tr>
</table></td></tr>
<tr><td>(None)</td><td>Transmitter Data</td><td>0:0:0–7</td><td>The host processor conveys output data to the transmitter in the parallel mode by writing a data byte to the transmitter data register. The data is divided on baud boundaries, as follows:

Note: Data is transmitted bit zero first.
<table>
<tr><th rowspan="2">Configuration</th><th colspan="8">Bits</th></tr>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>V.29 9600 bps</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
<tr><td>V.29 7200 bps</td><td colspan="2">Not Used</td><td colspan="2">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.29 4800 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td>Baud 0</td></tr>
<tr><td>V.27 4800 bps</td><td colspan="2">Not Used</td><td colspan="2">Baud 1</td><td colspan="3">Baud 0</td></tr>
<tr><td>V.27 2400 bps</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td>Baud 0</td></tr>
<tr><td>2400 bps Gearshift</td><td colspan="2">Baud 3</td><td colspan="2">Baud 2</td><td colspan="2">Baud 1</td><td>Baud 0</td></tr>
<tr><td>4800 bps Gearshift</td><td colspan="4">Baud 1</td><td colspan="4">Baud 0</td></tr>
</table></td></tr>
<tr><td>TSB</td><td>Transmitter Setup Bit</td><td>0:E:3</td><td>When the host processor changes the transmitter configuration, the SEPT bit or the FSKT bit, the host must write a one in this control bit. TSB goes to a zero when the change becomes effective. Worst case setup time is 2 baud + turnoff sequence + training (if applicable).</td></tr>
<tr><td>TTDIS</td><td>Transmitter Train Disable</td><td>0:7·6</td><td>When control bit TTDIS is a one, the transmitter does not generate a training sequence at the start of transmission. With training disabled, RTS/CTS delay is less than two baud times.</td></tr>
<tr><td>XCEN</td><td>External Clock Enable</td><td>0:7:1</td><td>When control bit XCEN is a one, the transmitter timing is established by the external clock supplied at the hardware input XTCLK, pin 22A.</td></tr>
</table>

The following is a list of the configurations that may be used with the forward channel and the states of the various control bits.

	Transmitter Control		Receiver Control
Configuration	PCF 0:9:5	CF 0:9:3	SCEN 1:7:2
FT/V.29/9600	1	1	1
FT/V.29/7200	1	1	1
FT/V.29/4800	1	1	1
FT/V.27/4800	0	X	1
FT/V.27/2400	0	X	1
*V.27/4800	0	X	1
*V.27/2400	0	X	1
V.21 FSK	X	X	1

*Both V.27 long and short train may be used. X = Don't care.

Note that CCITT V.29 and Gearshift configurations cannot be used with the forward channel.

POWER-ON INITIALIZATION

When power is applied to the R96FT/SC, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is generated.

At POR time the modem defaults to the following configuration: fast train, V.29, 9600 bps, no echo protector tone, 1700 Hz carrier frequency, scrambled ones segment disabled, serial data mode, internal clock, cable equalizers disabled, transmitter digital delay equalizer disabled, link amplitude equalizer disabled, link delay equalizer disabled, transmitter output level set to −1 dBm ±1 dB, interrupts disabled, receiver threshold set to −43 dBm, and train-on-data enabled.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or more applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after $\overline{POR}$ is removed.

PERFORMANCE

Whether functioning in V.27, V.29 or the proprietary fast train configurations, the R96FT/SC provides the user with high performance.

POLLING SUCCESS

In the 9600 bps fast train configuration the modem approaches a 98% success rate over unconditioned 3002 lines for a signal-to-noise ratio of 26 dB, with a received signal level of −20 dBm. When used in conjunction with the 75 bps forward channel, 9600 bps main channel polling performance degrades by approximately 2 dB.

BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

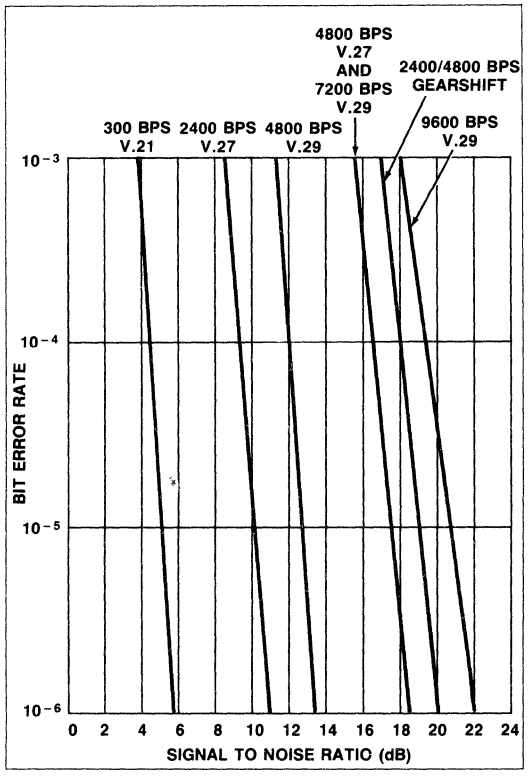
PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz, or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

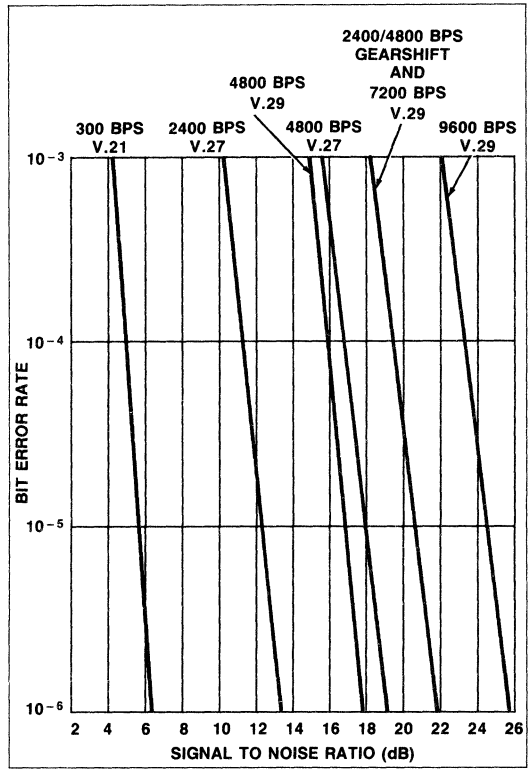
At 4800 bps (V.27 bis/ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

An example of the BER performance capabilities is given in the following diagrams:

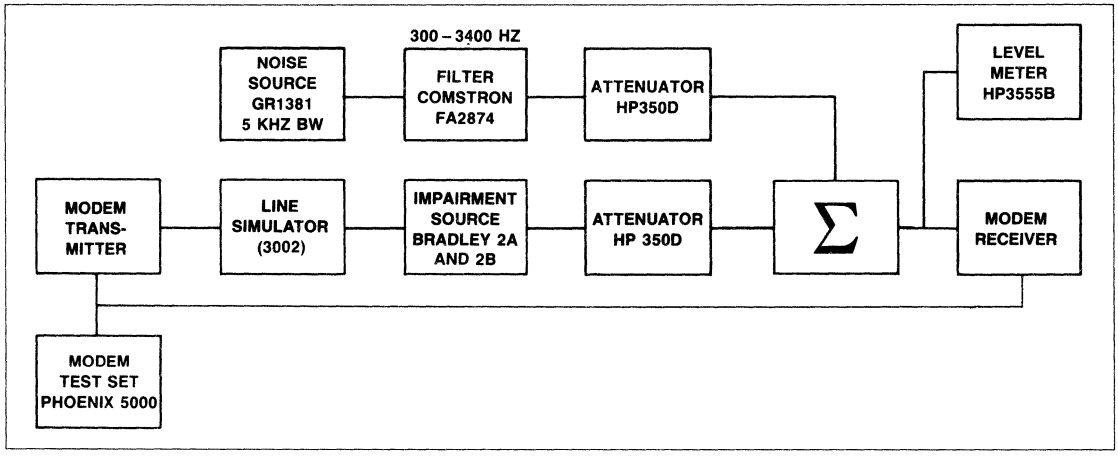


Typical BER Performance
Back-to-Back, – 20 dBm Receive Signal Level



Typical BER Performance
3002 Unconditioned Line, – 20 dBm Receive Signal Level

The BER performance test set-up is shown in the following diagram:



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Modem Power Requirements

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	650 mA	<820 mA
+12 Vdc	±5%	50 mA	< 80 mA
−12 Vdc	±5%	60 mA	< 90 mA

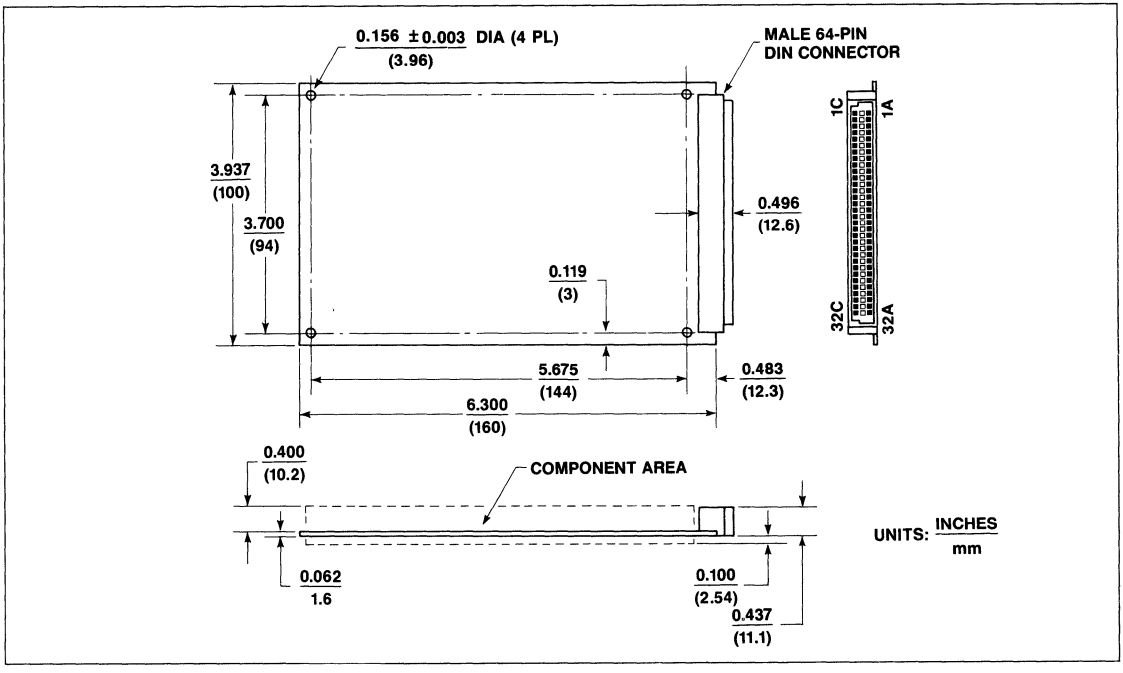
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Modem Environmental Restrictions

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity:	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less
Altitude	−200 feet to +10,000 feet

Modem Mechanical Considerations

Parameter	Specification
Board Structure·	Single PC board with a 3-row 64-pin right angle male DIN connector with rows A and C populated. The modem can also be ordered with the following DIN connector: 64-pin DIN right angle female, 64-pin DIN vertical male or 64-pin DIN vertical female.
Mating Connector:	Female 3-row 64-pin DIN receptacle with rows A and C populated. Typical mating receptacle: Winchester 96S-6043-0531-1, Burndy R196B32R00A00Z1, or equivalent.
PCB Dimensions:	
Width	3.937 in. (100 mm)
Length	6.300 in. (160 mm)
Height	0.40 in. (10.2 mm)
Weight (max):	5.5 oz (156 g)
Lead Extrusion (max.)	0.100 in. (2.54 mm)



R96FT/SC Modem Dimensions and Pin Locations

Rockwell

R144DP
V.33 Ultra High Speed Modem

INTRODUCTION

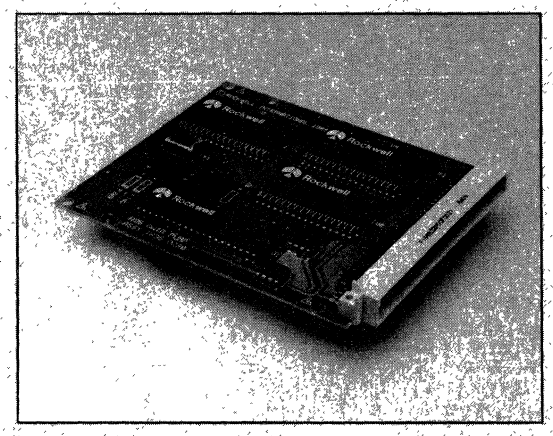
The Rockwell R144DP is a synchronous CCITT V.33 modem. It is designed to operate over unconditioned or conditioned lines, through the appropriate line termination. It is packaged in a small module with a DIN connector, or a smaller module with dual-in-line pin (DIP) connection.

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.33 and V.29. The R144DP can operate at speeds of 14400, 12000, 9600, 7200, and 4800 bps.

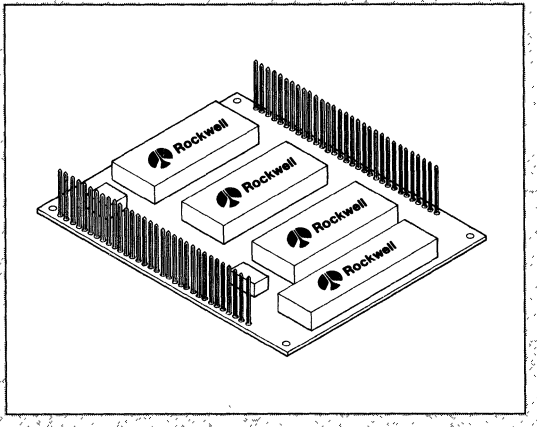
The R144DP is designed for use in ultra high speed data applications. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, serial/parallel host interface simplify system development and reduce system production cost. The DIN connector version can be mated to a matching DIN receptacle on the host module, whereas the DIP connector version can be directly installed onto the host module.

FEATURES

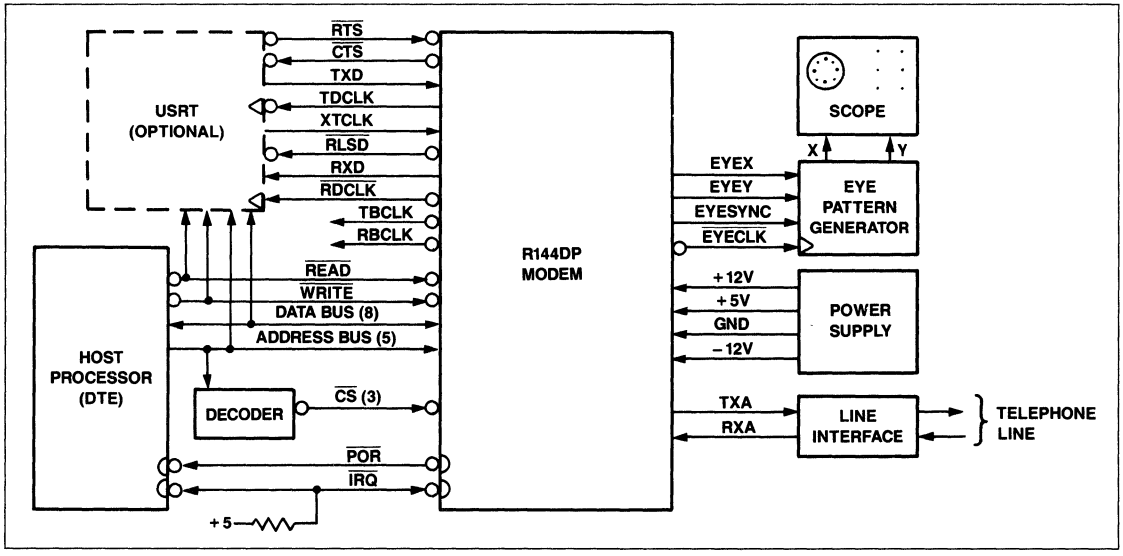
- Compatibilities
  - — CCITT: V.33 and V.29 Synchronous
- 4-Wire Full-Duplex
- Trellis Coded Modulation (TCM)
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Dynamic Range: – 43 dBm to 0 dBm
- Automatic Adaptive Equalizer
- Diagnostic Capability
- Loopback
  - — Local and Remote Analog
  - — Remote Digital
- Small Size
  - — 100 mm × 120 mm (3.94 in. × 4.73 in.) with DIN Connector
  - — 82 mm × 100 mm (3.23 in. × 3.94 in.) with DIP Connection
- Power Consumption: 2 W (Typical)



R144DP DIN Connector Version



R144DP DIP Connector Version



R144DP Functional Interconnect Diagram

SPECIFICATIONS

Power Requirements

+5 Vdc ±5% <650 mA
+12 Vdc ±5% < 10 mA
-12 Vdc ±5% < 70 mA

Environmental

Temperature: Operating 0°C to 60°C
Storage -40°C to 80°C
Relative Humidity: Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Rockwell

R9696DP
V.32 Ultra High Speed Modem

INTRODUCTION

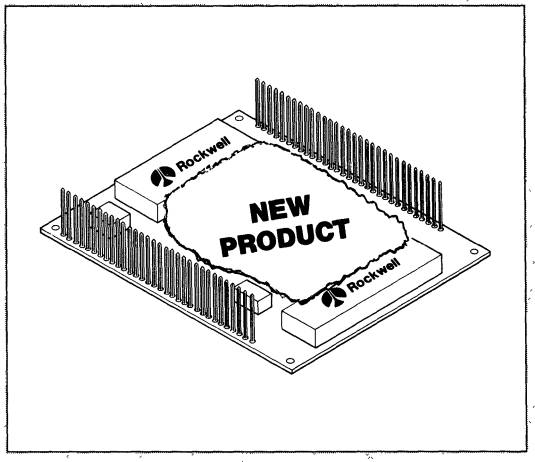
The Rockwell R9696DP is a 2-wire full-duplex, synchronous/asynchronous CCITT V.32 and V.22 bis modem. It is designed to operate over the public switched telephone network, as well as leased lines, through the appropriate line termination. It is packaged in a small module with dual-in-line (DIP) connection for direct installation onto a host module.

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.32, V.22 bis, V.22 and V.21, as well as Bell 212A. The R9696DP can operate at speeds of 9600, 4800, 2400 and 300 bps.

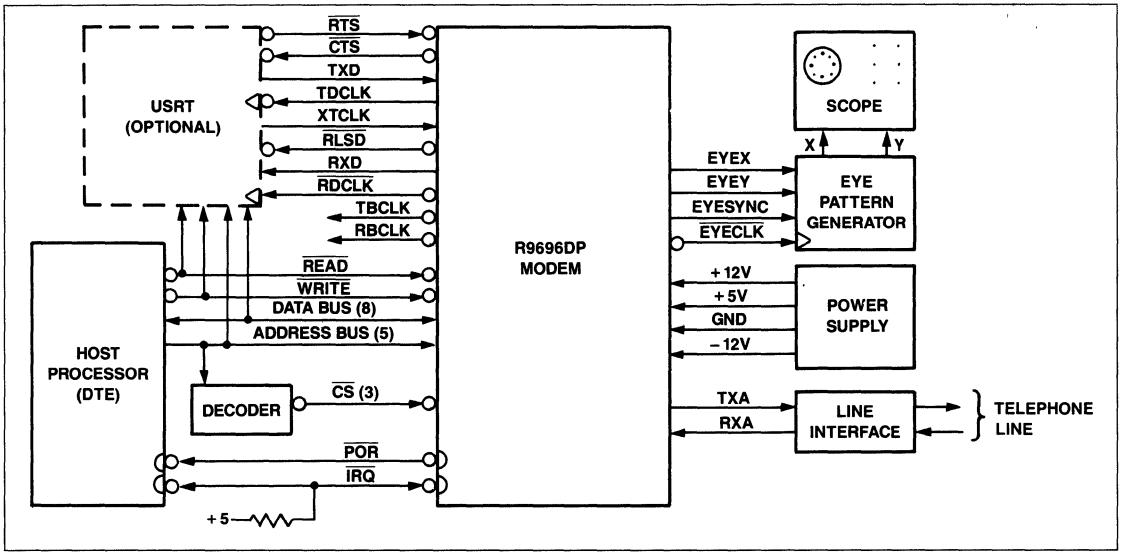
The R9696DP is designed for use in ultra high speed data applications. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, serial/parallel host interface, and DIP connection simplify system development and reduce system production cost.

FEATURES

- Compatibilities
  - — CCITT: V.32, V.22 bis, V.22, and V.21
  - — Bell: Bell 212A
- Synchronous/Asynchronous
- 2-Wire Full-Duplex
- Trellis Coded Modulation (TCM)
- Near and Far End Echo Cancellation
- Automatic Handshake Recognition
- Auto-Dial and Auto-Answer
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Dynamic Range: – 43 dBm to 0 dBm
- Automatic Adaptive Equalizer
- Diagnostic Capability
- Loopback
  - — Local and Remote Analog
  - — Remote Digital
- Small Size
  - — 82 mm × 100 mm (3.23 in. × 3.94 in.) with DIP Connection
- Power Consumption: 2 W (Typical)



R9696DP Modem



R9696DP Functional Interconnect Diagram

SPECIFICATIONS

Power Requirements

+5 Vdc ±5% <650 mA
+12 Vdc ±5% < 10 mA
-12 Vdc ±5% < 70 mA

Environmental

Temperature: Operating 0°C to 60°C
Storage -40°C to 80°C
Relative Humidity: Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

R1496MM
V.33, V.32 Ultra High Speed Modem

INTRODUCTION

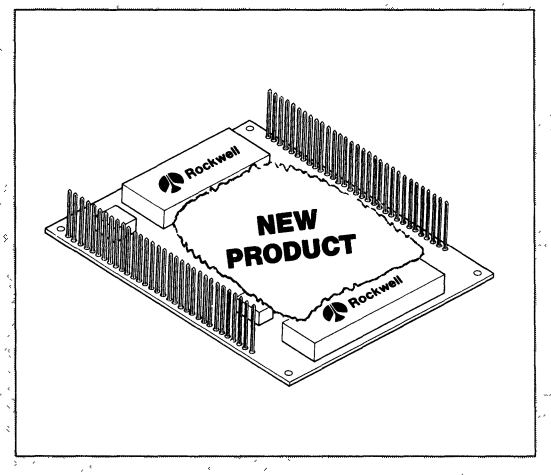
The Rockwell R1496MM is a 2-wire full-duplex, synchronous/asynchronous CCITT V.33 and V.32 modem. It is designed to operate in a leased line environment where fallback to operation over the public switched telephone network is desired. It is packaged in a small module with dual-in-line (DIP) connection for direct installation onto a host module.

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.33, V.32 and V.29. The R1496MM can operate at speeds of 14400, 12000, 9600, 7200, 4800 and 2400 bps.

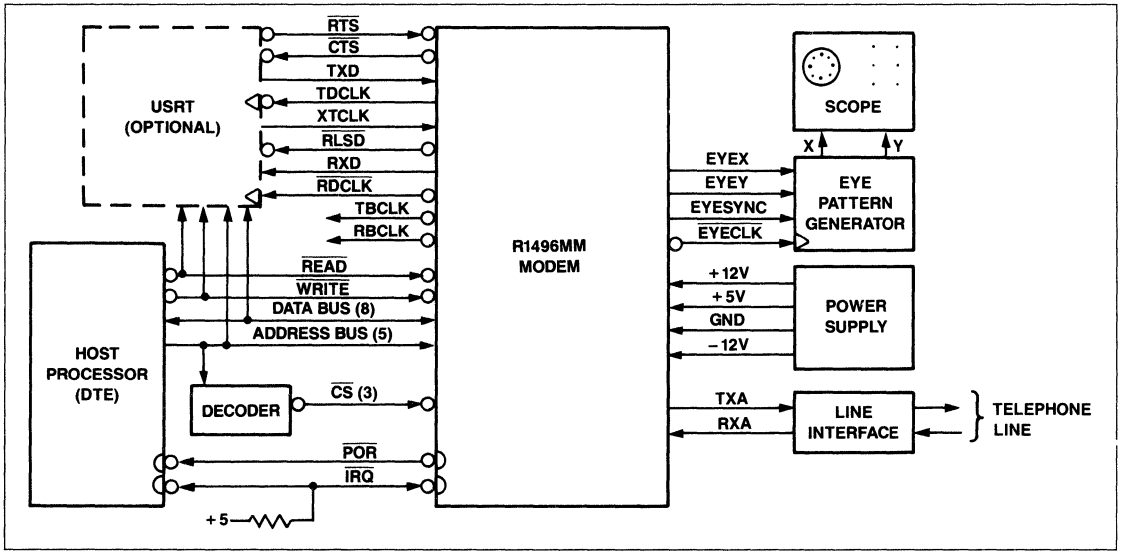
The R1496MM is designed for use in ultra high speed data applications. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, serial/parallel host interface, and DIP connection simplify system development and reduce system production cost.

FEATURES

- Compatibilities
  - — CCITT: V.33, V.32, V.29
- Synchronous/Asynchronous
- 2-Wire Half-Duplex, 2-Wire/4-Wire Full-Duplex
- Trellis Coded Modulation (TCM)
- Near and Far End Echo Cancellation
- Automatic Handshake Recognition
- Auto-Dial and Auto-Answer
- DTE Interface
  - — Functional: CCITT V.24 (RS-232-C) (Data/Control) and Microprocessor Bus (Data/Configuration/Control)
  - — Electrical: TTL and CMOS Compatible
- Dynamic Range: – 43 dBm to 0 dBm
- Automatic Adaptive Equalizer
- Diagnostic Capability
- Loopback
  - — Local and Remote Analog
  - — Remote Digital
- Small Size
  - — 82 mm × 100 mm (3.23 in. × 3.94 in.) with DIP Connection
- Power Consumption: 2 W (Typical)



R1496MM Modem



R1496MM Functional Interconnect Diagram

SPECIFICATIONS

Power Requirements

+5 Vdc ±5% <650 mA
+12 Vdc ±5% < 10 mA
-12 Vdc ±5% < 70 mA

Environmental

Temperature: Operating 0°C to 60°C
Storage -40°C to 80°C
Relative Humidity: Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

SECTION 3
IMAGING MODEMS

IMAGING MODEMS
Leading the World in Facsimile Modems

Rockwell is the world leader in the production and sale of highly integrated 9600 bps Group 3 facsimile modems. We are a major supplier to Japanese facsimile manufacturers and have been a key factor in "driving" signal processor (SP) and integrated analog (IA) technology.

Rockwell's R96F — a half-duplex, dial-up, 9600 bps, synchronous modem — is the industry standard for facsimile image transmission. Its compact size, unexcelled performance and proven reliability record have made it the choice of every major facsimile manufacturer since its introduction in 1984. The R96F is designed for use in Group 3 facsimile machines and is also compatible with Group 2 machines.

In response to market demands for smaller facsimile machines, Rockwell has introduced a line of single-package, 64-pin QUIP, facsimile modems. The R24 MONOFAX, operating at 2400 bps, and the R48 MONOFAX, operating at 4800 bps, are the world's first single-package modems designed for the emerging personal facsimile market.

In addition, Rockwell offers single device modems for other imaging applications. The R48PCJ, a V.27 ter modem with both long and short training options, is designed for applications in personal computer communication, teletex and intelligent workstations. The R24BKJ, a V.26 bis modem, is designed for applications in banking terminals and intelligent workstations.

Continuing our digital communications leadership role, Rockwell has introduced a 14.4 Kbps half-duplex modem for general switched telephone line operation. This high performance, ultra high speed product introduction further establishes Rockwell as a leader in setting standards for the facsimile modem industry.

Model	Data Speed (bps)	PSTN/ Leased Line	2/4-Wire Half/Full-Duplex	Sync/Async	Compliance
R24MFX	2400, 300	P/L	2WHD	Sync	CCITT V.27 ter Fallback, V.21 Channel 2,
R24BKJ	2400	P/L	2WHD	Sync	CCITT V.26 bis, Bell 201C
R48MFX	4800, 2400, 300	P/L	2WHD	Sync	CCITT V.27 ter, V.21 Channel 2, T.4, T.30
R48PCJ	4800, 2400, 300	P/L	2WHD	Sync	CCITT V.27 ter Short Train, V.21 Channel 2, T.4, T.30
R96PCJ	9600, 7200, 4800, 2400 300	P/L	2WHD	Sync	CCITT V.29, V.27 ter Short Train, V.21 Channel 2, T.4, T.30
R96F	9600, 7200, 4800, 2400 300	P/L	2WHD	Sync	CCITT V.29, V.27 ter, V.21 Channel 2, T.3, T.4, T.30
R96MD	9600, 7200, 4800, 2400 300	P/L	2WHD	Sync	CCITT V.29, V.27 ter, V.21 Channel 2, T.3, T.4, T.30
R144HD	14400, 12000, 9600, 7200, 4800, 2400, 300	P/L	2WHD	Sync	CCITT V.33, V.29, V.27 ter, V.21 Channel 2, T.3, T.4, T.30
R96MFX	9600, 7200, 4800, 2400 300	P/L	2WHD	Sync	CCITT V.29, V.27 ter, V.21 Channel 2, T.4, T.30

Rockwell

R24MFX
2400 bps MONOFAX™ Modem

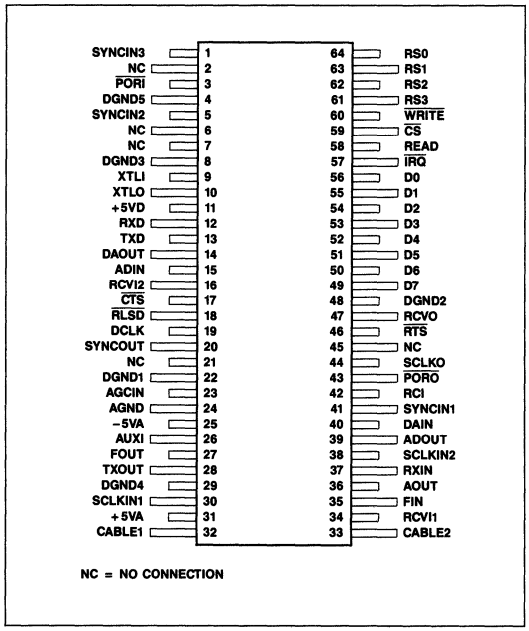
INTRODUCTION

The R24MFX MONOFAX 24 is a synchronous, serial/parallel, 2400 bps modem in a single 64-pin quad in-line package (QUIP). The modem is designed for operation over the public switched telephone network with appropriate line terminations, such as a data access arrangement, provided externally.

The R24MFX satisfies the telecommunications requirements specified in CCITT Recommendation V.27 ter fallback (2400 bps), T.4 and the binary signaling capabilities of Recommendation T.30.

The R24MFX is optimized for use in compact Group 3 facsimile machines. Its small size and low power consumption offer the user flexibility in creating a 2400 bps modem customized for specific packaging and functional requirements.

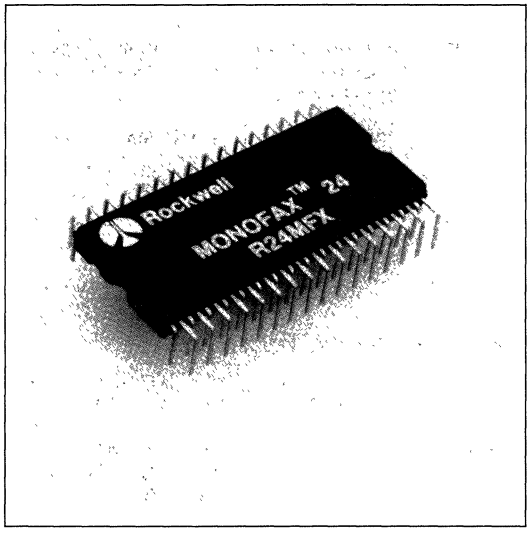
™MONOFAX is a trademark of Rockwell International



R24MFX Pin Assignments

FEATURES

- Single 64-Pin QUIP
- CCITT V.27 ter Fallback, T.30, V.21 Channel 2, T.4
- Group 3 Facsimile Transmission/Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Dynamic Range: −43 dBm to 0 dBm
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R24MFX 2400 bps MONOFAX Modem

TECHNICAL CHARACTERISTICS

TONE GENERATION

Under control of the host processor, the R24MFX can generate single or dual frequency voice band tones up to 3600 Hz with a resolution of 0.11 Hz and an accuracy of 0.01%. The transmit level and frequency of each tone is independently programmable.

TONE DETECTION

Single frequency tones are detected by a programmable filter. The presence of energy at the selected frequency is indicated by a bit in the interface memory.

SIGNALING AND DATA RATES

Signaling/Date Rates

Configuration	Parameter	Specification (±0.01%)
V.27	Signaling Rate Data Rate	1200 Baud 2400 bps
V.21	Signaling Rate Data Rate	300 Baud 300 bps

DATA ENCODING

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

At 300 baud, the data stream is 300 bps FSK per CCITT V.21 channel 2.

COMPROMISE CABLE EQUALIZERS

In addition to the adaptive equalizer, the R24MFX provides selectable compromise cable equalizers to optimize performance over three different lengths of non-loaded cable of 0.4 mm diameter (1.8 km, 3.6 km, and 7.2 km).

Cable Equalizer Nominal Gain

Frequency (Hz)	Gain (dB) Relative to 1700 Hz		
	1.8 km	3.6 km	7.2 km
700	−0.99	−2.39	−3.93
1500	−0.20	−0.65	−1.22
2000	+0.15	+0.87	+1.90
3000	+1.43	+3.06	+4.58

TRANSMITTED DATA SPECTRUM

When operating at 1200 baud, the transmitter spectrum is shaped by a square root of 90% raised cosine filer.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically meet the requirements of foreign telephone regulatory agencies.

SCRAMBLER/DESCRAMBLER

The R24MFX incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT V.27 ter.

RECEIVE LEVEL

The receiver circuit of the R24MFX satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. An external input buffer and filter must be supplied between the receiver analog input (RXA) and the R24MFX RXIN pin. The received line signal level is measured at RXA.

RECEIVE TIMING

In the receive state, the R24MFX provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is programmable. An external output buffer and filter must be supplied between the R24MFX TXOUT pin and the transmitter analog output (TXA). The default level at TXA is +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R24MFX provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency:* Selected data rate of 2400 or 300 Hz (±0.01%).
2. *Duty Cycle:* 50% ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

Three turn-on sequences are generated by the R24MFX, as defined in the following table:

Turn-On Sequences

No.	Bit Rate.	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Time (ms)	Comments
1	300 bps	<14	No Training Sequence
2	2400 bps[2]	943	No Echo Protector Tone
3	2400 bps[2]	1148	Preceded[1] By Echo Protector Tone

Notes:
1. Turn-on sequence 3 is used on lines with protection against talker echo.
2. V.27 ter long training sequence only.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud, followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{\text{RTS}}$ goes false.

CLAMPING

The following clamps are provided with the R24MFX:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{\text{RLSD}}$ is off.
2. *Received Line Signal Detector ($\overline{\text{RLSD}}$).* $\overline{\text{RLSD}}$ is clamped off (squelched) whenever $\overline{\text{RTS}}$ is on.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{\text{CTS}}$)

The time between the off-to-on transition of $\overline{\text{RTS}}$ and the off-to-on transition of $\overline{\text{CTS}}$ is dictated by the length of the training sequence. Response time is 943 ms for V.27 ter at 2400 bps. In V.21 $\overline{\text{CTS}}$ turns on in 14 ms or less.

The time between the on-to-off transition of $\overline{\text{RTS}}$ and the on-to-off transition of $\overline{\text{CTS}}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{\text{RLSD}}$)

$\overline{\text{RLSD}}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{\text{RLSD}}$ off-to-on response time is 674 ±10 ms. The $\overline{\text{RLSD}}$ on-to-off response time is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{\text{RLSD}}$ on threshold or at least 5 dB below the actual $\overline{\text{RLSD}}$ off threshold.

The $\overline{\text{RLSD}}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Receiver threshold is programmable over the range 0 dBm to −50 dBm, however, performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to RXA.

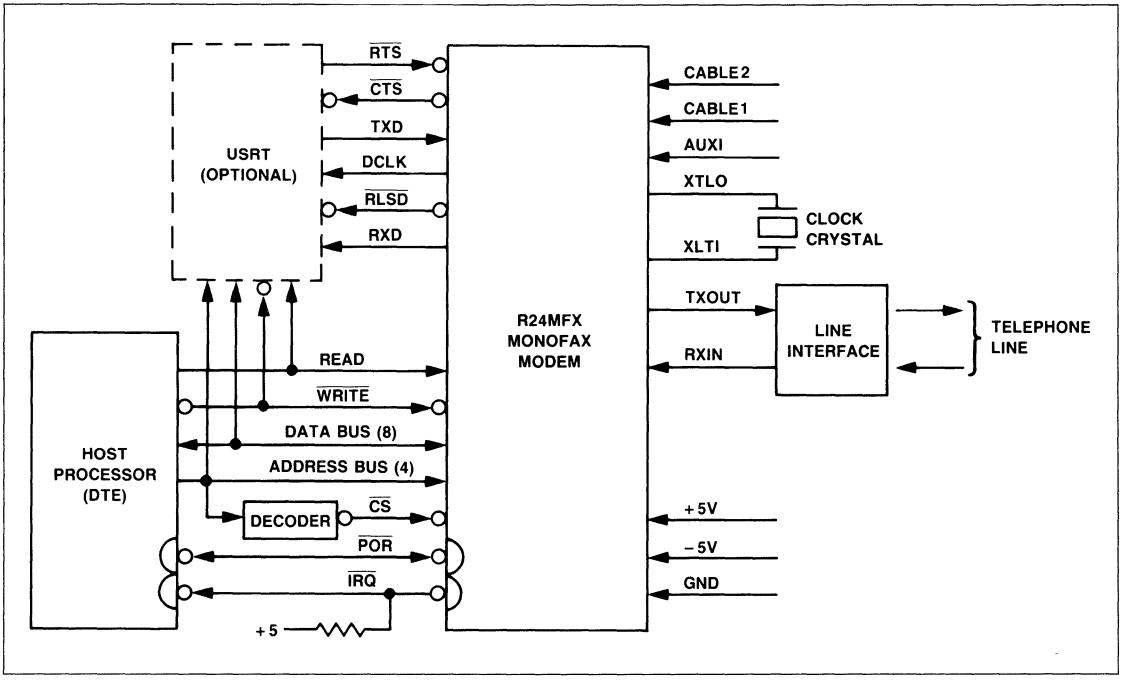
POWER

Voltage	Tolerance	Current (Max) @ 25°C	Current (Max) @ 60°C
+5 Vdc	±5%	250 mA @ 5.0 Vdc	225 mA @ 5.0 Vdc
−5 Vdc	±5%	25 mA @ −5.0 Vdc	25 mA @ −5.0 Vdc

Note: All voltages must have ripple ≤0.1 volts peak-to-peak. If a switching supply is chosen, user may select any frequency between 20 kHz and 150 kHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak

ENVIRONMENTAL

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in suitable antistatic container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.



R24MFX Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins on the 64-pin QUIP. Software circuits are assigned to specific bits in a 16-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R24MFX Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital and Analog Interface Characteristics tables.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

R24MFX Hardware Circuits

Name	Type	Pin No.	Description
A. POWER:			
AGND	GND	24	Connect to Analog Ground
DGND1	GND	22	Connect to AGND Ground
DGND2	GND	48	Connect to Digital Ground
DGND3	GND	8	Connect to Digital Ground
DGND4	GND	29	Connect to Digital Ground
DGND5	GND	4	Connect to Digital Ground
+5 VA	PWR	31	Connect to Analog +5V Power
+5 VD	PWR	11	Connect to Digital +5V Power
−5 VA	PWR	25	Connect to Analog −5V Power
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	49	Data Bus (8 Bits)
D6	I/OA	50	
D5	I/OA	51	
D4	I/OA	52	
D3	I/OA	53	
D2	I/OA	54	
D1	I/OA	55	
D0	I/OA	56	
RS3	IA	61	Register Select (4 Bits) Select Reg. 0−F
RS2	IA	62	
RS1	IA	63	
RS0	IA	64	
$\overline{CS}$	IA	59	Chip Select
READ	IA	58	Read Strobe
$\overline{WRITE}$	IA	60	Write Strobe
$\overline{IRQ}$	OB	57	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	19	Data Clock
$\overline{RTS}$	IB	46	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	13	Transmitter Data Signal
RXD	OC	12	Receiver Data Signal
RLSD	OC	18	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABLE1	IC	32	Cable Select 1
CABLE2	IC	33	Cable Select 2

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXOUT	AA	28	Connect to Output Op Amp
RXIN	AB	37	Connect to Input Op Amp
AUXI	AC	26	Auxiliary Analog Input
F. OVERHEAD			
$\overline{PORO}$	I/OB	43	Power-On-Reset Output
$\overline{PORI}$	I/OB	3	Power-On-Reset Input
XTLO	R*	10	Connect to Crystal Circuit
XTLI	R*	9	Connect to Crystal Circuit
RCVO	R*	47	Receive Mode Output
RCVI1	R*	34	Connect to RCVO
RCVI2	R*	16	Connect to RCVO
SCLKO	R*	44	Switched Capacitor Clock Output
SCLKIN1	R*	30	Connect to SCLKO
SCLKIN2	R*	38	Connect to SCLKO
AOUT	R*	36	Smoothing Filter Output
AGCIN	R*	23	AGC Input
DAOUT	R*	14	DAC/AGC Data Out
DAIN	R*	40	Connect to DAOUT
ADOUT	R*	39	ADC Output
ADIN	R*	15	Connect to ADOUT
FOUT	R*	27	Smoothing Filter Output
FIN	R*	35	Connect to FOUT
SYNCOUT	R*	20	Sample Clock Output
SYNCIN1	R*	41	Connect to SYNCOUT
SYNCIN2	R*	5	Connect to SYNCOUT
SYNCIN3	R*	1	Connect to SYNCOUT
RCI	R*	42	RC Junction for POR Time Constant
G. RESERVED			
	R*	2	Do Not Connect
	R*	6	Do Not Connect
	R*	7	Do Not Connect
	R*	21	Do Not Connect
	R*	45	Do Not Connect

*R = Required overhead connection; no connection to host equipment.

Digital Interface Characteristics

Symbol	Parameter	Units	Type: Input IA	Input IB	Input IC	Output OA	Output OB	Output OC	Input/Output I/OA	Input/Output I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	2.0 min. 0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

Analog Interface Characteristics

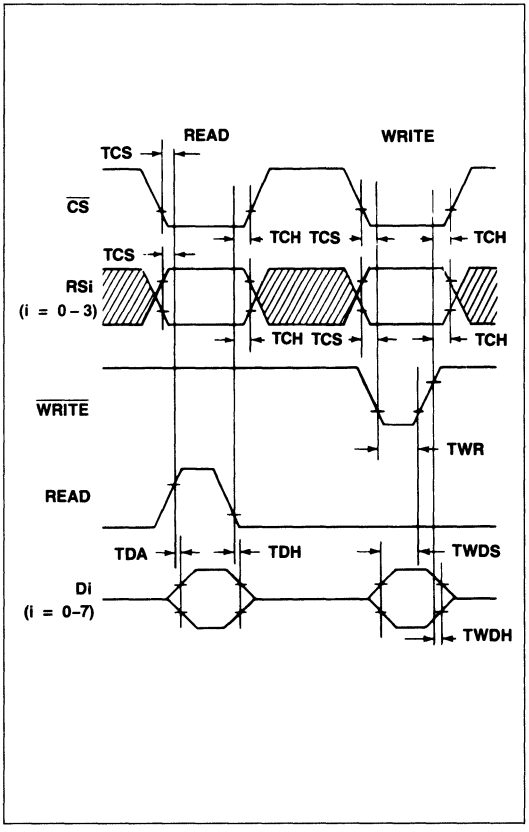
Analog Interface Characteristics

Name	Type	Characteristics
TXOUT	AA	The transmitter output can supply a maximum of ±3.03 volts into a load resistance of 10k Ω minimum. In order to match to 600 Ω, an external smoothing filter with a transfer function of 15726.43/(S+11542.44) and 604 Ω series resistor are required.
RXIN	AB	The receiver input impedance is greater than 1M Ω. An external antialiasing filter with a transfer function of 19533.88/(S+11542.44) is required.
AUXI	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 3600 Hz will cause aliasing errors. The input impedance is 1M Ω, and the gain to transmitter output (TXA) is +5.6 dB ±1 dB.

Note: Absolute maximum voltage ratings for analog inputs are: $(-5\ VA - 0.3) \leq V_{IN} \leq (+5\ VA + 0.3)$

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to READ or $\overline{WRITE}$	TCS	30	—	ns
Data Access time after READ	TDA	—	140	ns
Data hold time after READ	TDH	10	50	ns
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
$\overline{WRITE}$ strobe pulse width	TWR	75	—	ns



Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABLE1	CABLE2	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs. Signals TXOUT and RXIN require buffering and filtering to be suitable for driving and receiving the communication channel. Signal AUXI provides access to the transmitter for summing host audio signals with the modem analog output.

The filters required for anti-aliasing on the receiver input and smoothing on the transmitter output have a single pole located at 11,542 radians. Although this pole is located within the modem passband, internal filters compensate for its presence and, therefore, the pole location must not be changed. Some variation from recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10k Ω.

Notice that when reference is made to signals TXA, RXA, and AUXIN, these signals are not electrically identical to TXOUT, RXIN, and AUXI. The schematic of the recommended modem interface circuit illustrates the differences.

Overhead

Except for the power-on-reset signal $\overline{\text{PORO}}$, the overhead signals are intended for internal use only. The various required connections are illustrated in the recommended modem interface circuit schematic. No host connections should be made to overhead signals other than $\overline{\text{PORO}}$.

SOFTWARE CIRCUITS

The R24MFX contains 16 memory mapped registers to which an external (host) microprocessor has access. The host may read data out of or write data into these registers. Refer to the R24MFX Host Processor Interface figure.

When information in these registers is being discussed, the format Z:Q is used. The register is specified by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a one (1) and "off" when reset to a zero (0).

Status/Control Bits

The operation of the R24MFX is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus.

All status and control bits are defined in the R24MFX Interface Memory Map table. Bits designated by ' — ' are reserved for modem use only and must not be changed by the host.

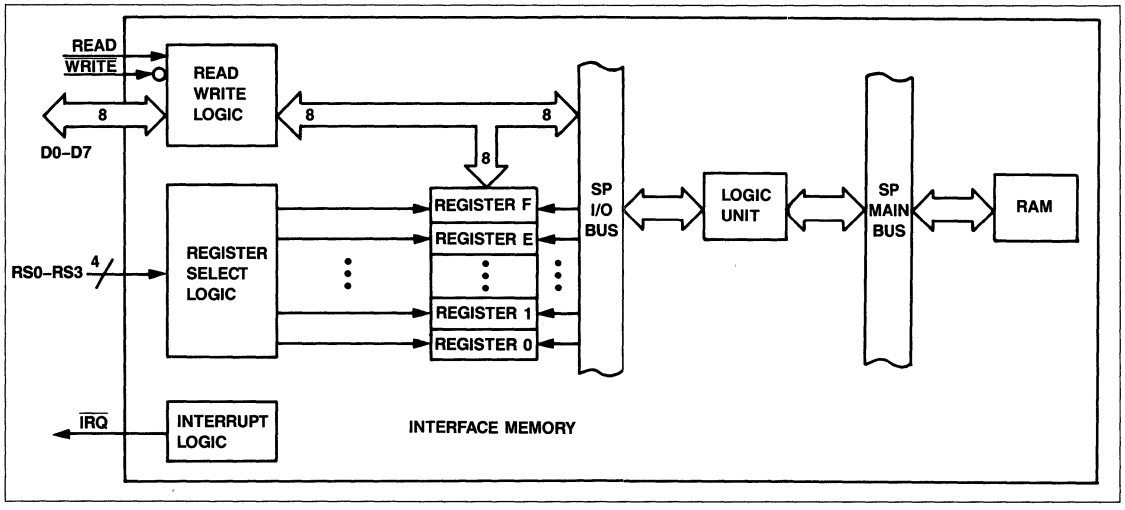
Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Configuration Control

Three configurations are available in the R24MFX modem: V.27, V.21, and Tone. These three configurations are selected by writing an 8-bit binary code into the configuration field (CONF) of the interface memory. The configuration field consists of bits 7 through 0 of register D. The code for these bits is: 0 = V.21, 4 = V.27, and 8 = Tone. All other codes represent invalid states.

When the modem is initialized by power-on-reset, the configuration defaults to V.27. When the host wants to change configuration, the new code is written to the configuration field and the SETUP bit (E:3) is set to a one. Once the new configuration takes effect, the SETUP bit is reset to zero by the modem.

The information in the interface memory is serviced by the modem at either 1200 times per second or 7200 times per second depending on configuration. In V.21, the rate is 7200 times per second. In both V.27 and Tone configuration, the rate is 1200 times per second.



R24MFX Host Processor Interface

R24MFX Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAMA							
E	IA	CDIE	CDREQ	—	SETUP	DDIE	—	DDREQ
D	CONF							
C	RTSP	EPT	TPDM	TDIS	EQSV	EQFZ	—	RAMW
B	RX	FED		GHIT	—	—	—	—
A	TDET	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	CDET	—	PN	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RXCD							
4	TXCD							
3	DDXM							
2	DDXL							
1	DDYM							
0	DDYL							
Register \ Bit	7	6	5	4	3	2	1	0

Channel Data Transfer

Data sent to or received from the data channel may be transferred between the modem and host processor in either serial or parallel form. The receiver operates in both serial and parallel mode simultaneously and requires no mode control bit selection. The transmitter operates in either serial or parallel mode as selected by mode control bit C:5 (TPDM).

To enable the transmitter parallel mode, TPDM must be set to a 1. The modem automatically defaults to the serial mode (TPDM = 0) at power-on. In either transmitter serial or parallel mode, the R24MFX is configured by the host processor via the microprocessor bus.

Serial Mode—The serial mode uses a standard V.24 (RS-232-C) hardware interface (optional USRT) to transfer channel data. Transmitter data can be sent serially only when TPDM is set to a zero.

Parallel Mode—Parallel data is transferred via two registers in the interface memory. Register 5 (RXCD) is used for receiver channel data, and Register 4 (TXCD) is used for transmitter channel data. Register 5 is continuously written every eight bit times when in the receive state. Register 4 is used as the source of channel transmitter data only when bit C:5 (TPDM) is set to a one by the host. Otherwise the transmitter reads data from the V.24 interface. Both $\overline{RTS}$ and RTSP remain enabled, however, regardless of the state of TPDM.

When performing parallel data transfer of channel data, the host and modem can synchronize their operations by handshaking bits in register E. Bit E:5 (CDREQ) is the channel data request bit. This bit is set to a one by the modem when receiver data is available in RXCD or when transmitter data is required in TXCD. Once the host has finished reading RXCD or writing TXCD, the host processor must reset CDREQ by writing a zero to that bit location.

When set to a one by the host, Bit E:6 (CDIE) enables the CDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) is a one.

If the host does not respond to the channel data request within eight bit times, the RXCD register is over written or the TXCD register is sent again.

Refer to Channel Data Parallel Mode Control flow chart for recommended software sequence.

R24MFX Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
CDET	Carrier Detector	8:5	The one state of CDET indicates passband energy is being detected, and a training sequence is not present. CDET goes to one at the start of the data state, and returns to zero at the end of the received signal. CDET activates one baud time before $\overline{\text{RLSD}}$ and deactivates one baud time after $\overline{\text{RLSD}}$.
CDIE	Channel Data Interrupt Enable	E:6	When set to a one, CDIE enables an $\overline{\text{IRQ}}$ interrupt to be generated when the channel data request bit (CDREQ) is a one.
CDREQ	Channel Data Request	E:5	Parallel data mode handshaking bit. Set to a one when the modem receiver writes data to RXCD, or the modem transmitter reads data from TXCD. CDREQ must be reset to zero by the host processor when data service is complete.
CONF	Configuration	D:0-7	The 8-bit field CONF controls the configuration of the modem according to the following table: **Hex Code** — **Configuration** 0 — V.21 4 — V.27 8 — Tone All else — Invalid **Configuration Definitions** *V.21*—The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 Channel 2 modulation system. *Tone*—The modem sends single or dual frequency tones in response to the $\overline{\text{RTS}}$ or RTSP signals. Tone frequencies and amplitudes are controlled by RAM locations written by the host. When not transmitting tones the Tone configuration allows detection of single frequency tones by the TDET bit. The tone detector frequency can be changed by the host by altering the contents of several RAM locations. *V.27*—The modem operates as specified in CCITT Recommendation V.27 for a 2400 bps data rate.
DDIE	Diagnostic Data Interrupt Enable	E:2	When set to a one, DDIE enables an IRQ interrupt to be generated when the diagnostic data request bit (DDREQ) is a one.
DDREQ	Diagnostic Data Request	E:0	DDREQ goes to a one when the modem reads from or writes to DDYL. DDREQ goes to a zero when the host processor reads from or writes to DDYL. Used for diagnostic data handshaking bit.
DDXL	Diagnostic Data X Least	2:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDXM	Diagnostic Data X Most	3:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDYL	Diagnostic Data Y Least	0:0-7	Least significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
DDYM	Diagnostic Data Y Most	1:0-7	Most significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
EPT	Echo Protector Tone	C:6	When EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence.
EQFZ	Equalizer Freeze	C:2	When EQFZ is a one, the adaptive equalizer taps stop updating and remain frozen.
EQSV	Equalizer Save	C:3	When EQSV is a one, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state.
FED	Fast Energy Detector	B:5,6	FED consists of a 2-bit field that indicates the level of received signal according to the following code. **Code** — **Energy Level** 0 — None 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold While receiving a signal, FED normally alternates between Codes 2 and 3.

R24MFX Interace Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
GHIT	Gain Hit	B:4	The gain hit bit goes to one when the receiver detects a sudden increase in passband energy faster than the AGC circuit can correct. GHIT returns to zero when the AGC output returns to normal.
IA	Interrupt Active	E:7	IA is a one when the modem is driving the interrupt request line ($\overline{IRQ}$) to a low TTL level.
PN	Period N	8:3	PN sets to a one at the start of the received PN sequence PN resets to zero at the start of the receiver data state. PN does not operate when EQFZ (C:2), EQSV (C:3) or TDIS (C:4) is set to one
RAMA	RAM Access	F:0-7	The RAMA register is written by the host when reading or writing diagnostic data. The RAMA code determines the RAM location with which the diagnostic read or write is performed.
RAMW	RAM Write	C:0	RAMW is set to a one by the host processor when performing diagnostic writes to the modem RAM. RAMW is set to a zero by the host when reading RAM diagnostic data.
RTSP	Request to Send Parallel	C:7	The one state of RTSP begins a transmit sequence. The modem continues to transmit until RTSP is turned off and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem.
RXCD	Receiver Channel Data	5:0-7	RXCD is written to by the modem every eight bit times. This byte of channel data can be read by the host when the receiver sets the channel data request bit (CDREQ).
RX	Receive State	B:7	RX is a one when the modem is in the receive state (i.e., not transmitting)
SETUP	Setup	E:3	The host processor must set the SETUP bit to a one when reconfiguring the modem, i.e., when changing CONF (D:0-7).
TDET	Tone Detected	A:7	The one state of TDET indicates reception of a tone. The filter can be retuned by means of the diagnostic write routine.
TDIS	Training Disable	C:4	If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one when $\overline{RTS}$ or RTSP go active, the generation of a training sequence is prevented at the start of transmission.
TPDM	Transmitter Parallel Data Mode	C:5	When control bit TPDM is a one, the transmitter accepts data for transmission from the TXCD register rather than the serial hardware data input.
TXCD	Transmitter Channel Data	4:0-7	The host processor conveys output data to the transmitter in parallel data mode by writing a data byte to the TXCD register when the channel data request bit (CDREQ) goes to a one Data is transmitted as single bits in V.21 or as dibits in V.27 starting with bit 0 or dibit 0,1.

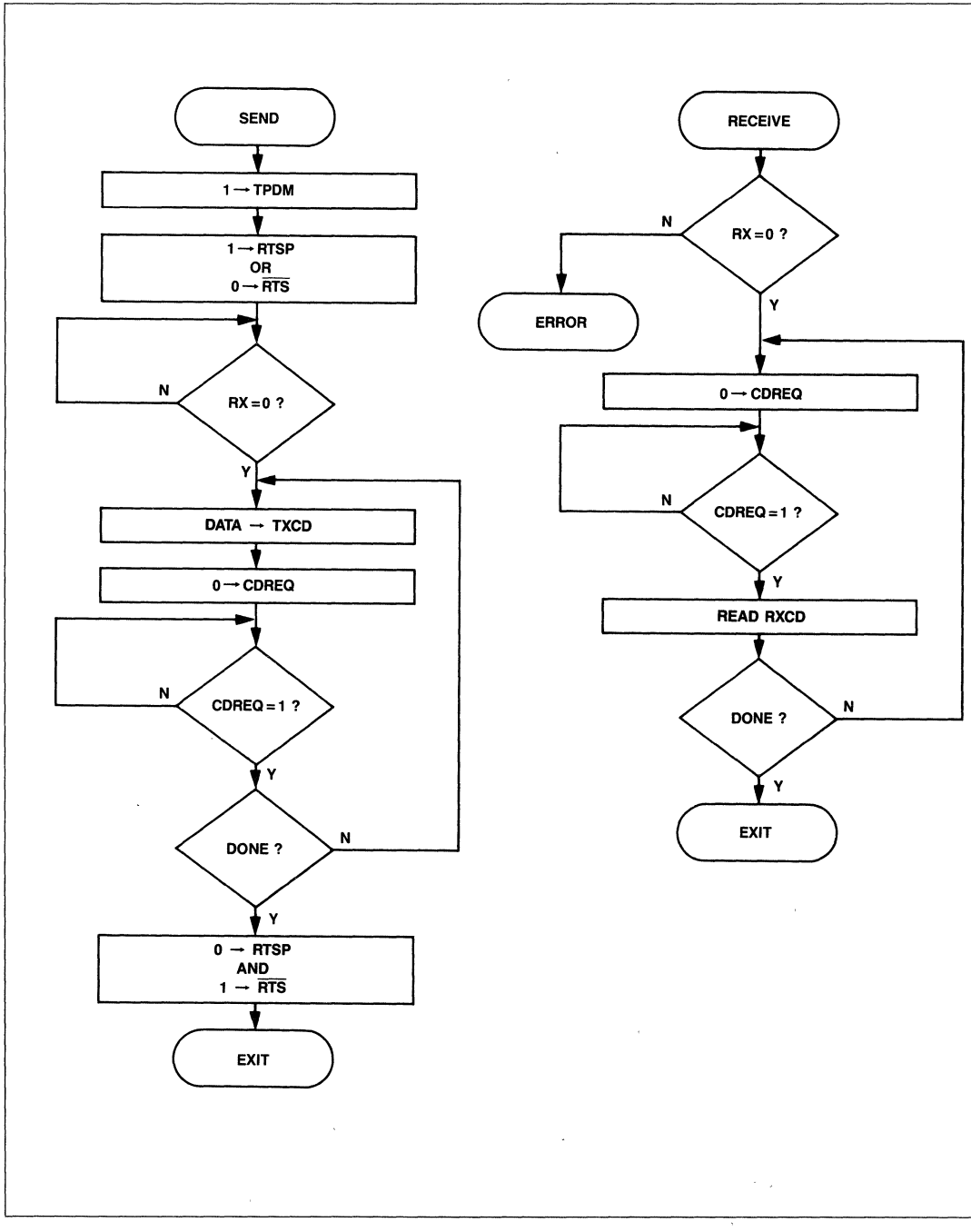
Diagnostic Data Transfer

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register F (RAMA). The R24MFX RAM Access Codes table lists 27 access codes for storage in register F and the corresponding diagnostic functions. The R24MFX Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long. These bits are written into interface memory registers 3, 2, 1 and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit C:0 (RAMW) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the more significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAMA bits of register F. When bit F:7 is set to one, the XRAM is selected. When F:7 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the diagnostic data request bit E:0 (DDREQ) is reset to zero. When the modem reads or writes register 0, DDREQ is set to a one. When set to a one by the host, bit E:2 (DDIE) enables the DDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) goes to a one.



Channel Data Parallel Mode Control

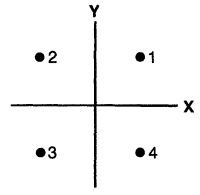
R24MFX RAM Access Codes

Node	Function	RAMA	Reg. No.
1	AGC Gain Word	B1	2,3
2	Average Power	F2	2,3
3	Receiver Sensitivity	F1	2,3
4	Receiver Hysteresis	84	2,3
5	Equalizer Input	5B	0,1,2,3
6	Equalizer Tap Coefficients	1B-2A	0,1,2,3
7	Unrotated Equalizer Output	6B	0,1,2,3
8	Rotated Equalizer Output	0A	0,1,2,3
9	Decision Points	6C	0,1,2,3
10	Error Vector	6D	0,1,2,3
11	Rotation Angle	87	2,3
12	Frequency Correction	8B	2,3
13	EQM	B0	2,3
14	Alpha (α)	36	0,1
15	Beta One (β_1)	37	0,1
16	Beta Two (β_2)	38	0,1
17	Alpha Prime (α')	39	0,1
18	Beta One Prime (β_1')	3A	0,1
19	Beta Two Prime (β_2')	3B	0,1
20	Alpha Double Prime (α'')	B6	2,3
21	Beta Double Prime (β'')	B7	2,3
22	Output Level	43	0,1
23	Tone 1 Frequency	8E	2,3
24	Tone 1 Level	44	0,1
25	Tone 2 Frequency	8F	2,3
26	Tone 2 Level	45	0,1
27	Checksum	02	0,1

R24MFX Diagnostic Data Scaling

Node	Parameter/Scaling
1	**AGC Gain Word** (16-bit unsigned). AGC Gain in dB = 50 − [(AGC Gain Word/64) × 0.098] Range: $(16C0)_{16}$ to $(7FFF)_{16}$, For −43 dBm Threshold
2.	**Average Power** (16-bit unsigned) Post-AGC Average Power in dBm = 10 Log (Average Power Word/2185) Typical Value = $(0889)_{16}$, corresponding to 0 dBm Pre-AGC Power in dBm = (Post-AGC Average Power–AGC Gain)
3	**Receiver Sensitivity** (16-bit twos complement) On-Number = 655.36 (52.38 + P_{ON}) where: P_{ON} = Turn-on threshold in dB Convert On-Number to hexadecimal and store at access code F1
4	**Receiver Hysteresis** (16-bit twos complement) Off-Number = [65.4 $(10^A)]^2/2$ where: A = (P_{OFF} − P_{ON} − 0.5)/20 P_{ON} = Turn-on threshold in dB P_{OFF} = Turn-off threshold in dB Convert Off-Number to hexadecimal and store at access code 84.

R24MFX Diagnostic Data Scaling

Node	Parameter/Scaling
5,7–9	**All base-band signal point nodes** (i.e., Equalizer Input, Unrotated Equalizer Output, Rotated Equalizer Output, and Decision Points) are 32-bit, complex, twos complement numbers. Point 1: X = 1600, Y = 1600 Point 2: X = EA00, Y = 1600 Point 3: X = EA00, EA00 Point 4: X = 1600, EA00 
6	**Equalizer Tap Coefficients** (32-bit, complex, twos complement) Complex numbers with X = real part, Y = imaginary part X and Y range: 0000 to $(FFFF)_{16}$ representing ± full scale in hexadecimal twos complement.
10	**Error Vector** (32-bit, complex, twos complement) Complex number with X = real part, Y = imaginary part. X and Y range: $(8000)_{16}$ to $(7FFF)_{16}$
11	**Rotation Angle** (16-bit, signed, twos complement) Rotation Angle in deg. = (Rot. Angle Word/65,536) × 360
12	**Frequency Correction** (16-bit signed twos complement) Frequency correction in Hz = (Freq. Correction Word/65,536) × Baud Rate Range: $(FC00)_{16}$ to $(400)_{16}$ representing ± 18.75 Hz
13	**EQM** (16-bit, unsigned) Filtered squared magnitude of error vector. Proportionality to BER determined by particular application
14–21	**Filter Tuning Parameters** (16-bit unsigned) Alpha, Beta One, Beta Two, Alpha Prime, Beta One Prime, Beta Two Prime, Alpha Double Prime, and Beta Double Prime are set according to instructions in application note 668. Use a sample rate of 7200 samples per second for all calculations.
22	**Output Level** (16-bit unsigned) Output Number = 27573.6 $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store at access code 43
24 and 26	**Tone 1 and Tone 2 Levels** Calculate the power of each tone independently by using the equation for Output Number given at node 22. Convert these numbers to hexadecimal then store at access codes 44 and 45. Total power transmitted in tone mode is the result of both tone 1 power and tone 2 power.
23 and 25	**Tone 1 and 2 Frequency** (16-bit unsigned) N = 9.1022 (Frequency in Hz) Convert N to hexadecimal then store at access code 8E or 8F.
27	**Checksum** (16-bit unsigned) ROM checksum number determined by revision level.

POWER-ON INITIALIZATION

When power is applied to the R24MFX, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below approximately 3 Vdc for more than 30 msec, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.27/2400 bps, serial mode, training enabled, echo protector tone enabled, interrupts disabled, RAM access code 0A, transmitter output level set for +5 dBm at TXA, receiver turn-on threshold set for -43.5 dBm, receiver turn-off threshold set for -47.0 dBm, tone 1 and tone 2 set for 0 Hz and 0 volts output, and tone detector parameters zeroed.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

Whether functioning as a V.27 ter or V.21 type modem, the R24MFX provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that illustrated in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of -20 dBm.

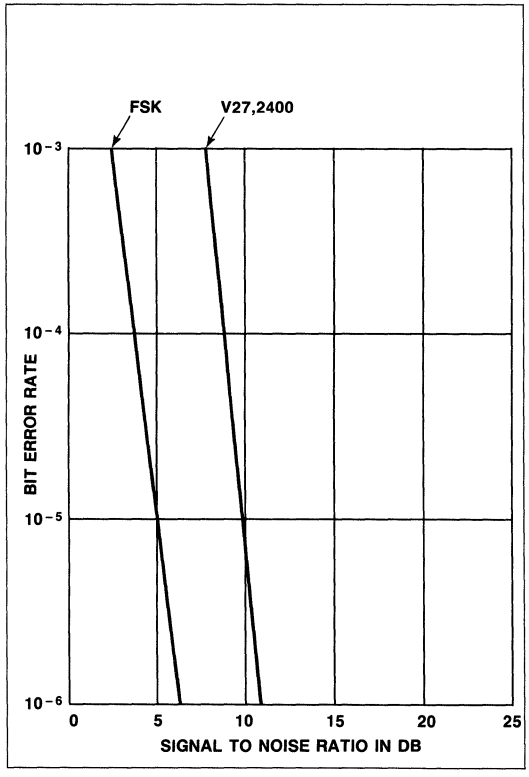
RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R24MFX can adapt to received frequency error of ±10 Hz with less than 0.2 dB degradation in BER performance.

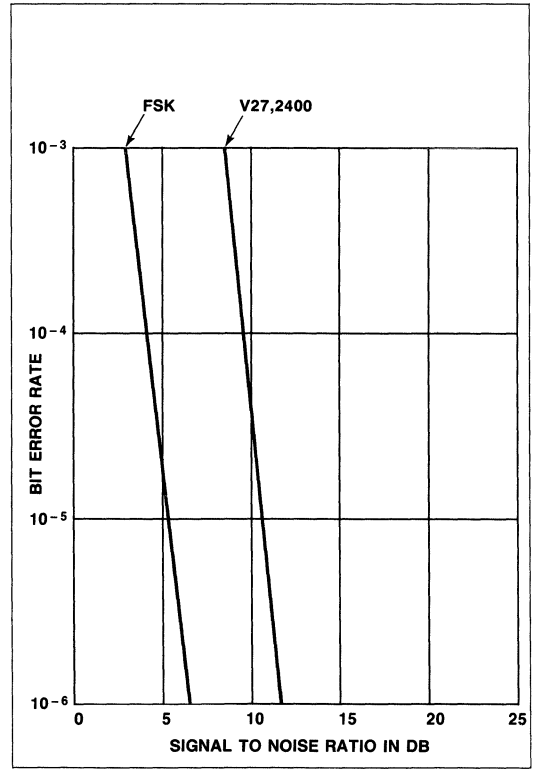
TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

An example of the BER performance capabilities is given in the following diagrams:

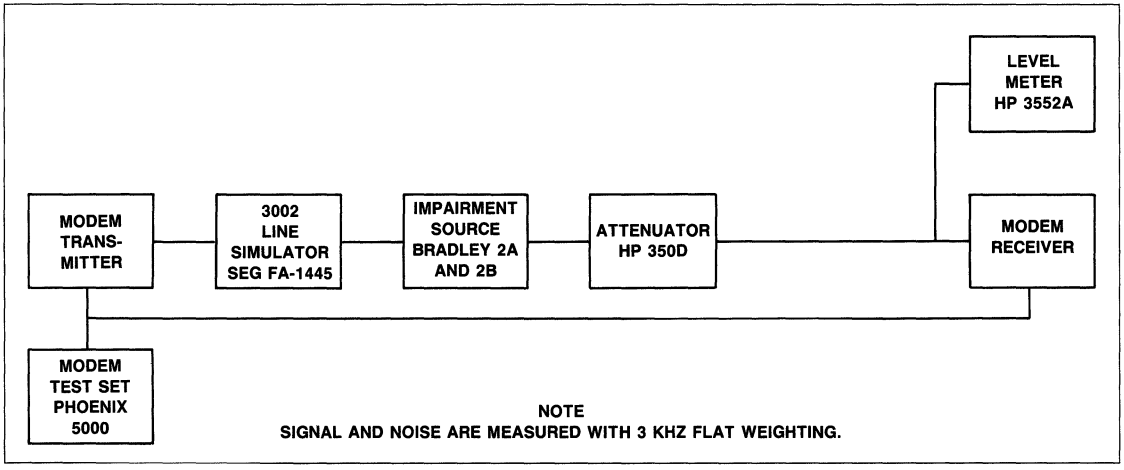


Typical Bit Error Rate (Back-to-Back, Level -20 dBm)



Typical Bit Error Rate (Unconditioned 3002 Line, Level -20 dBm)

The BER performance test set-up is show in the following diagram:



BER Performance Test Set-up

APPLICATION

Recommended Modem Interface Circuit

The R24MFX is supplied as a 64-pin QUIP device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit and parts list illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R2 and R3 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3k Ω series resistor should be used on each input (Pins 32 and 33) for isolation.

Resistors R4 and R9 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dB the 1% resistor values shown are correct for more than 99.8% of the units.

Typical Modem Interface Parts List

Component	Manufacturer's Part Number	Manufacturer
C3,C5,C7,C9	592CX7R104M050B	Sprague
C2	N511BY100JW	San Fernando/ Wescap
C1	C114C330J2G5CA	Kemet
C11	SA405C274MAA	AVX
Y1	333R14-002	Uniden
Z1	LM1458N	National
R5,R6	CML 1/10 T86.6K ohm ±1%	Dale Electronics
R4	5MA434.0K ±1%	Corning Electronics
R11	5043CX3R000J	Mepco Electra
R10	5043CX2M700J	Mepco Electra
R1	5043CX47K00J	Mepco Electra
R7	5043CX3K00J	Mepco Electra
R2,R3	5043CX1K00J	Mepco Electra
C10	ECEBEF100	Panasonic
C8	SMC50T1R0M5X12	United Chem-Con
C4,C6	C124C102J5G5CA	Kemet
CR1	IN751D	I.T.T.
R9	CRB¼XF47K5	R-Ohm
R8	ER025QKF2370	Matsushita Electric
R14	Determined by $\overline{IRQ}$ characteristics	

PC Board Layout Considerations

1. The R24MFX and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board (PCB).
2. All power traces should be at least 0.1 inch width.
3. If power source is located more than approximately 5 inches from the R24MFX, a decoupling capacitor of 10 microfarad or greater should be placed in parallel with C11 near pins 11 and 48.
4. All circuitry connected to pins 9 and 10 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the R24MFX package. Pin 24 should tie directly, by a unique path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and all analog ground points shown in the recommended circuit diagram.
7. Pins 4, 8, 29, and 48 should tie together at the R24MFX package. Pin 48 should tie directly, by a unique path, to the common ground point for analog and digital ground.
8. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 48 and all digital ground points shown in the recommended circuit diagram plus the crystal-can ground.
9. The R24MFX package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
10. As a general rule, digital signals should be routed on the component side of the PCB while analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
11. Routing of R24MFX signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to the table of noise characteristics for a list of pins in each category.

Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	Low	High
1	6	3	26	23
2	7	4	28	27
5	9	8	32	35
14	10	11	33	36
15	12	16		37
20	13	22		
21	17	24		
30	18	25		
38	19	29		
39	45	31		
40	46	34		
41	49	42		
44	50	43		
	51	47		
	52	48		
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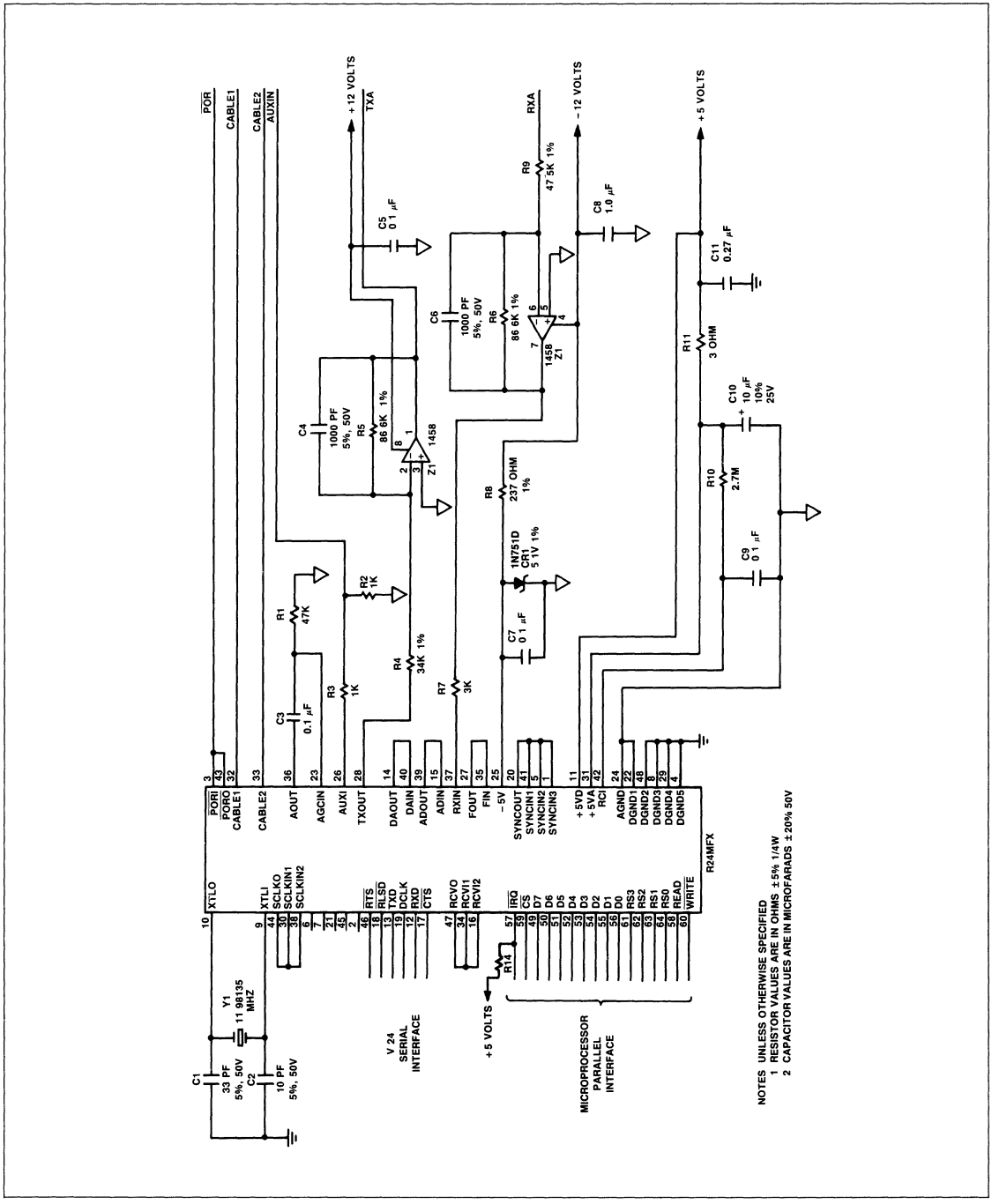
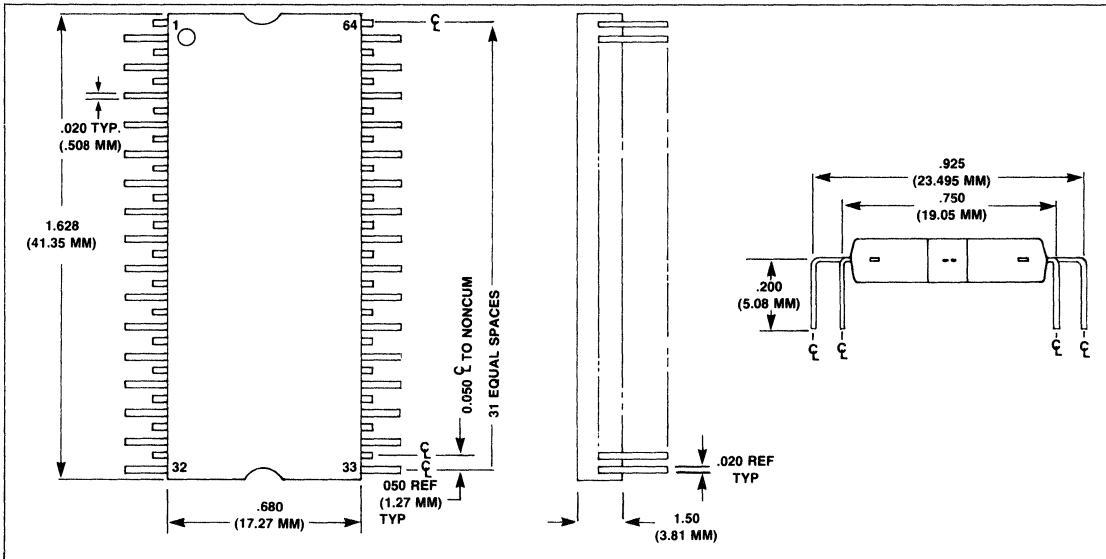


Recommended Modem Interface Circuit

PACKAGE DIMENSIONS



64-Pin QUIP

Rockwell

R24BKJ
2400 bps V.26 bis, Bell 201B/C Modem

INTRODUCTION

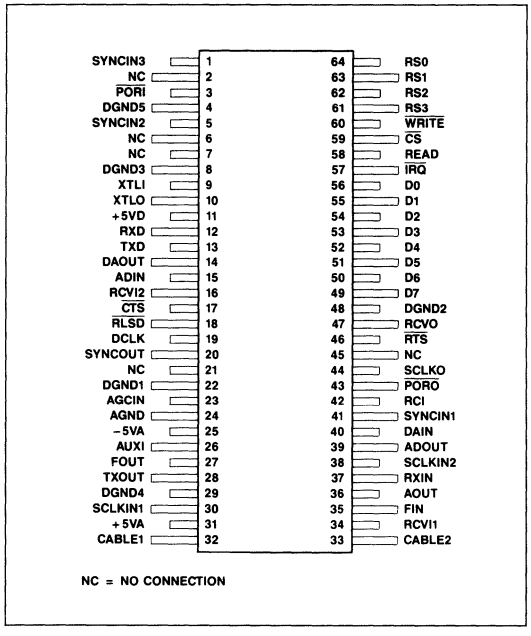
The R24BKJ is a synchronous, serial/parallel, 2400 bps modem in a single 64-pin quad in-line package (QUIP). The modem is designed for operation over the public switched telephone network with appropriate line terminations, such as a data access arrangement, provided externally.

The R24BKJ satisfies the telecommunications requirements specified in CCITT Recommendation V.26 bis Alternate A or B and Bell 201B/C.

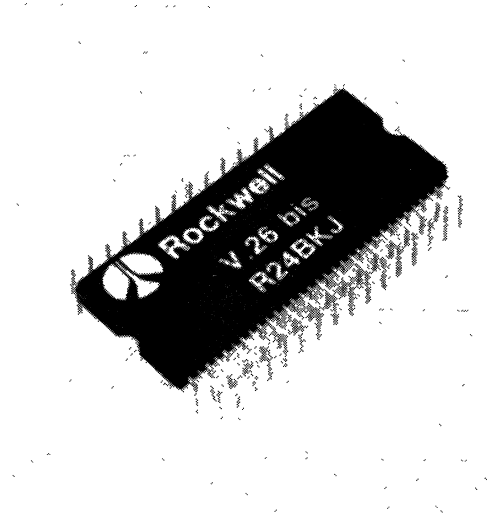
The R24BKJ is optimized for use in compact original equipment manufacturer (OEM) systems. Its small size and low power consumption offer the user flexibility in creating a 2400 bps modem customized for specific packaging and functional requirements.

FEATURES

- Single 64-Pin QUIP
- CCITT V.26 bis Alternate A or B
- Bell 201B/C
- Half-Duplex (2-Wire)
- Programmable RTS/CTS Delay
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Dynamic Range: – 43 dBm to 0 dBm
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R24BKJ Pin Assignments



R24BKJ 2400 bps V.26 bis/Bell 201B/C Modem

TECHNICAL CHARACTERISTICS

TONE GENERATION

Under control of the host processor, the R24BKJ can generate single or dual frequency voice band tones up to 3600 Hz with a resolution of 0.11 Hz and an accuracy of 0.01%. The transmit level and frequency of each tone is independently programmable.

TONE DETECTION

Single frequency tones are detected by a programmable filter. The presence of energy at the selected frequency is indicated by a bit in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate	1200 Baud
Data Rate	2400 bps

DATA ENCODING

The 2400 bps data stream is encoded into dibits per CCITT V.26 bis Alternate A or B and Bell 201B/C.

COMPROMISE CABLE EQUALIZERS

In addition to the adaptive equalizer, the R24BKJ provides selectable compromise cable equalizers to optimize performance over three different lengths of non-loaded cable of 0.4 mm diameter (1.8 km, 3.6 km, and 7.2 km).

Cable Equalizer Nominal Gain

Frequency (Hz)	Gain (dB) Relative to 1700 Hz		
	1.8 km	3.6 km	7.2 km
700	−0.99	−2.39	−3.93
1500	−0.20	−0.65	−1.22
2000	+0.15	+0.87	+1.90
3000	+1.43	+3.06	+4.58

TRANSMITTED DATA SPECTRUM

The transmitter spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically meet the requirements of foreign telephone regulatory agencies.

SCRAMBLER/DESCRAMBLER

The R24BKJ incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT V.27 ter. The scrambler can be disabled by setting a bit in interface memory.

RECEIVE LEVEL

The receiver circuit of the R24BKJ satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. An external input buffer and filter must be supplied between the receiver analog input (RXA) and the R24BKJ RXIN pin. The received line signal level is measured at RXA.

RECEIVE TIMING

In the receive state, the R24BKJ provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is programmable. An external output buffer and filter must be supplied between the R24BKJ TXOUT pin and the transmitter analog output (TXA). The default level at TXA, when sending pseudorandom data, is +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R24BKJ provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency:* Data rate of 2400 Hz (±0.01%).
2. *Duty Cycle:* 50% ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

SYNCHRONIZING SEQUENCE

The synchronizing sequence of the R24BKJ consists of two segments: a fixed segment of unscrambled ones, and an open segment which may be either unscrambled or scrambled ones, depending on the configuration selected. Both segments are programmable by allowing the synchronizing sequence to be varied for specific applications.

TURN-OFF SEQUENCE

The turn-off sequence consists of approximately 10 ms of remaining data and scrambled or unscrambled ones at 1200 baud.

CLAMPING

The following clamps are provided with the R24BKJ:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{\text{RLSD}}$ is off.
2. *Received Line Signal Detector ($\overline{\text{RLSD}}$).* $\overline{\text{RLSD}}$ is clamped off (squelched) whenever $\overline{\text{RTS}}$ is on.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the length of the synchronizing signal. The response time is programmable. The choice of response times depends upon the system application: a) limited protection against line echoes; b) protection given against line echoes.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

$\overline{RLSD}$ turns on whenever energy is detected on the line. The $\overline{RLSD}$ off-to-on response time is 10 ±5 ms.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD. The on-to-off response time is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

Receiver threshold is programmable over the range 0 dBm to −50 dBm, however, performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to RXA.

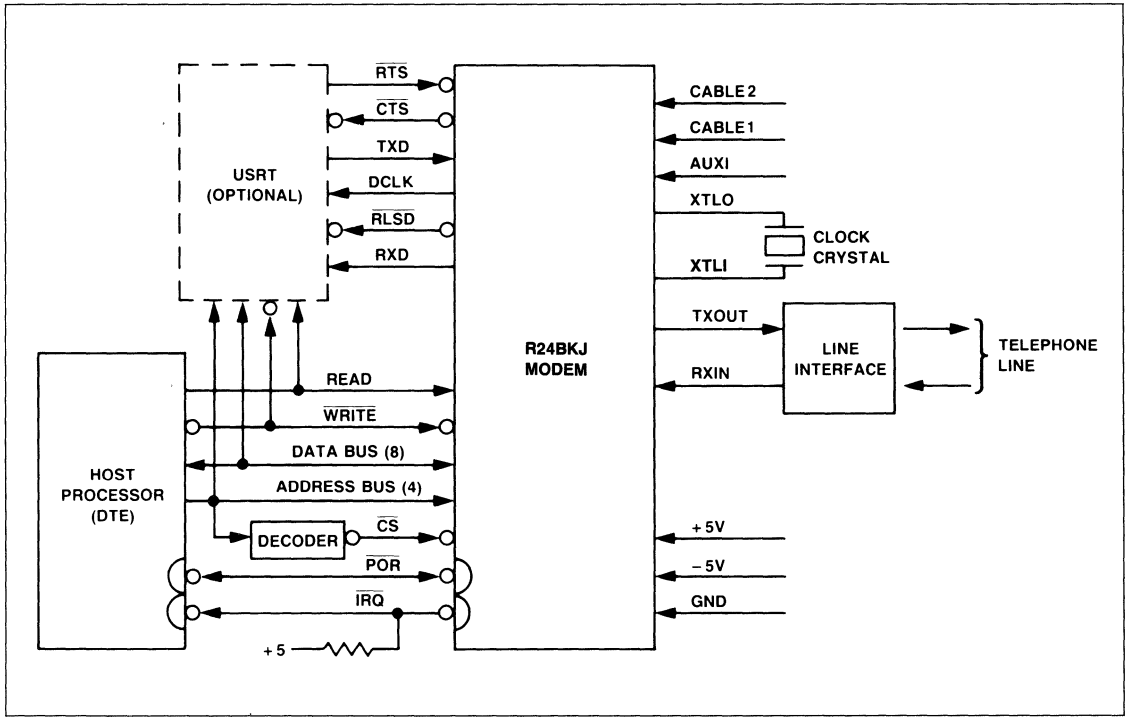
POWER

Voltage	Tolerance	Current (Max) @ 25°C	Current (Max) @ 60°C
+5 Vdc	±5%	250 mA @ 5.0 Vdc	225 mA @ 5.0 Vdc
−5 Vdc	±5%	25 mA @ −5.0 Vdc	25 mA @ −5.0 Vdc

Note: All voltages must have ripple ≤0.1 volts peak-to-peak. If a switching supply is chosen, user may select any frequency between 20 kHz and 150 kHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak.

ENVIRONMENTAL

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in suitable antistatic container).
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.



R24BKJ Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins on the 64-pin QUIP. Software circuits are assigned to specific bits in a 16-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R24BKJ Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital and Analog Interface Characteristics tables.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

R24BKJ Hardware Circuits

Name	Type	Pin No.	Description
A. POWER:			
AGND	GND	24	Connect to Analog Ground
DGND1	GND	22	Connect to AGND Ground
DGND2	GND	48	Connect to Digital Ground
DGND3	GND	8	Connect to Digital Ground
DGND4	GND	29	Connect to Digital Ground
DGND5	GND	4	Connect to Digital Ground
+5 VA	PWR	31	Connect to Analog +5V Power
+5 VD	PWR	11	Connect to Digital +5V Power
−5 VA	PWR	25	Connect to Analog −5V Power
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	49	Data Bus (8 Bits)
D6	I/OA	50	
D5	I/OA	51	
D4	I/OA	52	
D3	I/OA	53	
D2	I/OA	54	
D1	I/OA	55	
D0	I/OA	56	
RS3	IA	61	Register Select (4 Bits) Select Reg. 0−F
RS2	IA	62	
RS1	IA	63	
RS0	IA	64	
$\overline{CS}$	IA	59	Chip Select
READ	IA	58	Read Strobe
$\overline{WRITE}$	IA	60	Write Strobe
$\overline{IRQ}$	OB	57	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	19	Data Clock
$\overline{RTS}$	IB	46	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	13	Transmitter Data Signal
RXD	OC	12	Receiver Data Signal
$\overline{RLSD}$	OC	18	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABLE1	IC	32	Cable Select 1
CABLE2	IC	33	Cable Select 2

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXOUT	AA	28	Connect to Output Op Amp
RXIN	AB	37	Connect to Input Op Amp
AUXI	AC	26	Auxiliary Analog Input
F. OVERHEAD			
$\overline{PORO}$	I/OB	43	Power-On-Reset Output
$\overline{PORI}$	I/OB	3	Power-On-Reset Input
XTLO	R*	10	Connect to Crystal Circuit
XTLI	R*	9	Connect to Crystal Circuit
RCVO	R*	47	Receive Mode Output
RCVI1	R*	34	Connect to RCVO
RCVI2	R*	16	Connect to RCVO
SCLKO	R*	44	Switched Capacitor Clock Output
SCLKIN1	R*	30	Connect to SCLKO
SCLKIN2	R*	38	Connect to SCLKO
AOUT	R*	36	Smoothing Filter Output
AGCIN	R*	23	AGC Input
DAOUT	R*	14	DAC/AGC Data Out
DAIN	R*	40	Connect to DAOUT
ADOUT	R*	39	ADC Output
ADIN	R*	15	Connect to ADOUT
FOUT	R*	27	Smoothing Filter Output
FIN	R*	35	Connect to FOUT
SYNCOUT	R*	20	Sample Clock Output
SYNCIN1	R*	41	Connect to SYNCOUT
SYNCIN2	R*	5	Connect to SYNCOUT
SYNCIN3	R*	1	Connect to SYNCOUT
RCI	R*	42	RC Junction for POR Time Constant
G. RESERVED			
	R*	2	Do Not Connect
	R*	6	Do Not Connect
	R*	7	Do Not Connect
	R*	21	Do Not Connect
	R*	45	Do Not Connect

*R = Required overhead connection; no connection to host equipment.

Digital Interface Characteristics

Symbol	Parameter	Units	Type							
			Input			Output			Input/Output	
			IA	IB	IC	OA	OB	OC	I/OA	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

Analog Interface Characteristics

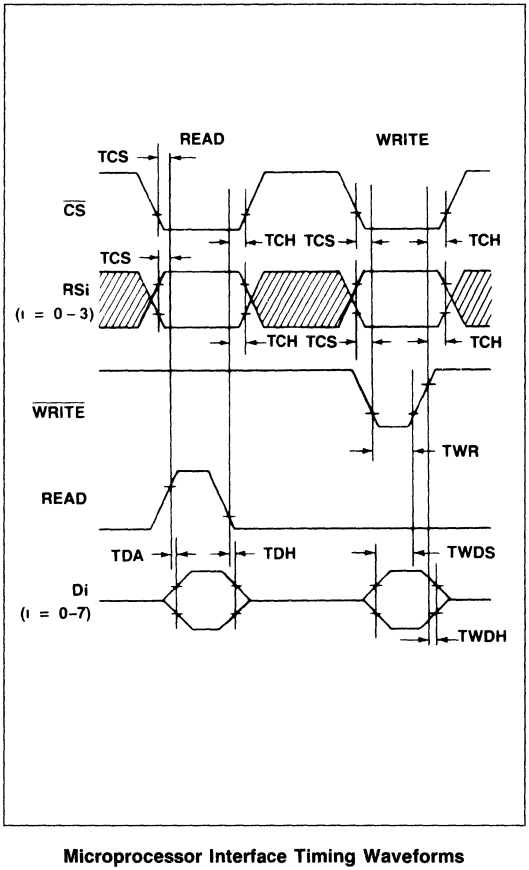
Analog Interface Characteristics

Name	Type	Characteristics
TXOUT	AA	The transmitter output can supply a maximum of ±3.03 volts into a load resistance of 10k Ω minimum. In order to match to 600 Ω, an external smoothing filter with a transfer function of 15726.43/(S + 11542.44) and 604 Ω series resistor are required.
RXIN	AB	The receiver input impedance is greater than 1M Ω. An external antialiasing filter with a transfer function of 19533.88/(S + 11542.44) is required.
AUXI	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 3600 Hz will cause aliasing errors. The input impedance is 1M Ω, and the gain to transmitter output (TXA) is +5.6 dB ±1 dB.

Note: Absolute maximum voltage ratings for analog inputs are: $(-5\ VA - 0.3) \leq V_{IN} \leq (+5\ VA + 0.3)$

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to READ or $\overline{WRITE}$	TCS	30	—	ns
Data Access time after READ	TDA	—	140	ns
Data hold time after READ	TDH	10	50	ns
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
$\overline{WRITE}$ strobe pulse width	TWR	75	—	ns



Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABLE2	CABLE1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs. Signals TXOUT and RXIN require buffering and filtering to be suitable for driving and receiving the communication channel. Signal AUXI provides access to the transmitter for summing host audio signals with the modem analog output.

The filters required for anti-aliasing on the receiver input and smoothing on the transmitter output have a single pole located at 11,542 radians. Although this pole is located within the modem passband, internal filters compensate for its presence and, therefore, the pole location must not be changed. Some variation from recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10k Ω.

Notice that when reference is made to signals TXA, RXA, and AUXIN, these signals are not electrically identical to TXOUT, RXIN, and AUXI. The schematic of the recommended modem interface circuit illustrates the differences.

Overhead

Except for the power-on-reset signal $\overline{\text{PORO}}$, the overhead signals are intended for internal use only. The various required connections are illustrated in the recommended modem interface circuit schematic. No host connections should be made to overhead signals other than $\overline{\text{PORO}}$.

SOFTWARE CIRCUITS

The R24BKJ contains 16 memory mapped registers to which an external (host) microprocessor has access. The host may read data out of or write data into these registers. Refer to the R24BKJ Host Processor Interface figure.

When information in these registers is being discussed, the format Z:Q is used. The register is specified by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a one (1) and "off" when reset to a zero (0).

Status/Control Bits

The operation of the R24BKJ is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus.

All status and control bits are defined in the R24BKJ Interface Memory Map table. Bits designated by ' — ' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Configuration Control

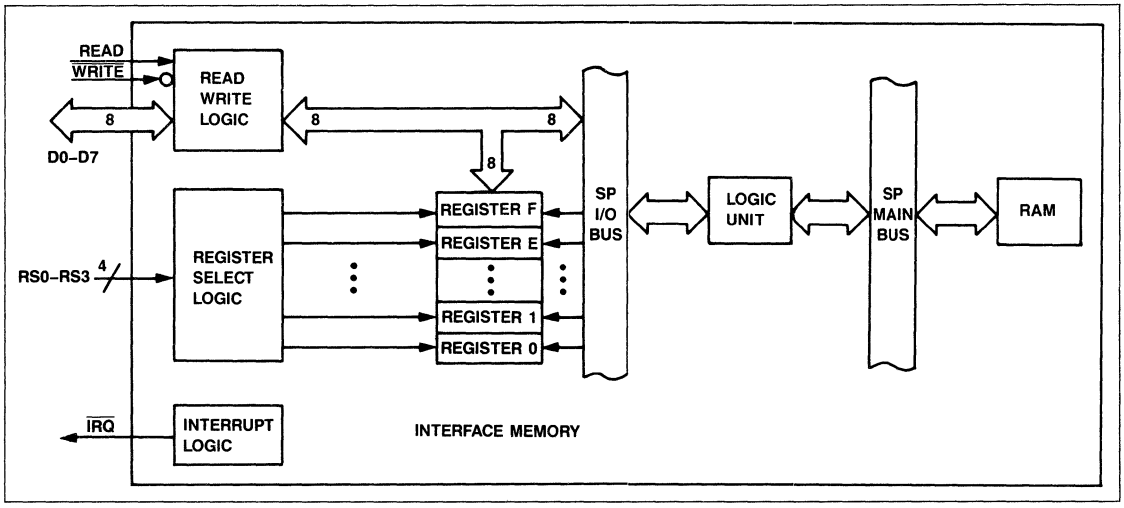
Five configurations are available in the R24BKJ modem. The configuration is selected by writing an 8-bit binary code into the configuration field (CONF) of the interface memory. The configuration field consists of bits 7 through 0 of register D. The code for these bits is shown in the following table. All other codes represent invalid states.

Configuration Codes

CONF Code	Configuration	Scrambler/ Descrambler
04*	V.26B	disabled
44	V.26A	disabled
84	V.26B	enabled
C4	V 26A	enabled
0C	Tone	Not applicable
*Default value at POR with 220 ms synchronizing sequence		

When the modem is initialized by power-on-reset, the configuration defaults to V.26B with scrambler disabled and 220 ms synchronizing signal. When the host wants to change configuration, the new code is written to the configuration field and the SETUP bit (E:3) is set to a one. Once the new configuration takes effect, the SETUP bit is reset to zero by the modem.

The information in the interface memory is serviced by the modem at 1200 times per second.



R24BKJ Host Processor Interface

R24BKJ Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAMA							
E	IA	CDIE	CDREQ	—	SETUP	DDIE	—	DDREQ
D	CONF							
C	RTSP	—	TPDM	1	—	EQFZ	—	RAMW
B	RX	FED		GHIT	—	—	—	—
A	TDET	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	CDET	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RXCD							
4	TXCD							
3	DDXM							
2	DDXL							
1	DDYM							
0	DDYL							
Register \ Bit	7	6	5	4	3	2	1	0

Channel Data Transfer

Data sent to or received from the data channel may be transferred between the modem and host processor in either serial or parallel form. The receiver operates in both serial and parallel mode simultaneously and requires no mode control bit selection. The transmitter operates in either serial or parallel mode as selected by mode control bit C:5 (TPDM).

To enable the transmitter parallel mode, TPDM must be set to a 1. The modem automatically defaults to the serial mode (TPDM = 0) at power-on. In either transmitter serial or parallel mode, the R24BKJ is configured by the host processor via the microprocessor bus.

Serial Mode—The serial mode uses a standard V.24 (RS-232-C) hardware interface (optional USRT) to transfer channel data. Transmitter data can be sent serially only when TPDM is set to a zero.

Parallel Mode—Parallel data is transferred via two registers in the interface memory. Register 5 (RXCD) is used for receiver channel data, and Register 4 (TXCD) is used for transmitter channel data. Register 5 is continuously written every eight bit times when in the receive state. Register 4 is used as the source of channel transmitter data only when bit C:5 (TPDM) is set to a one by the host. Otherwise the transmitter reads data from the V.24 interface. Both $\overline{RTS}$ and RTSP remain enabled, however, regardless of the state of TPDM.

When performing parallel data transfer of channel data, the host and modem can synchronize their operations by handshaking bits in register E. Bit E:5 (CDREQ) is the channel data request bit. This bit is set to a one by the modem when receiver data is available in RXCD or when transmitter data is required in TXCD. Once the host has finished reading RXCD or writing TXCD, the host processor must reset CDREQ by writing a zero to that bit location.

When set to a one by the host, Bit E:6 (CDIE) enables the CDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) is a one.

If the host does not respond to the channel data request within eight bit times, the RXCD register is over written or the TXCD register is sent again.

Refer to Channel Data Parallel Mode Control flow chart for recommended software sequence.

R24BKJ Interface Memory Definitions

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>CDET</td><td>Carrier Detector</td><td>8:5</td><td>The one state of CDET indicates passband energy is being detected, and a training sequence is not present. CDET goes to one at the start of the data state, and returns to zero at the end of the received signal. CDET activates one baud time before $\overline{\text{RLSD}}$ and deactivates one baud time after $\overline{\text{RLSD}}$.</td></tr>
<tr><td>CDIE</td><td>Channel Data Interrupt Enable</td><td>E:6</td><td>When set to a one, CDIE enables an $\overline{\text{IRQ}}$ interrupt to be generated when the channel data request bit (CDREQ) is a one.</td></tr>
<tr><td>CDREQ</td><td>Channel Data Request</td><td>E:5</td><td>Parallel data mode handshaking bit. Set to a one when the modem receiver writes data to RXCD, or the modem transmitter reads data from TXCD. CDREQ must be reset to zero by the host processor when data service is complete.</td></tr>
<tr><td>CONF</td><td>Configuration</td><td>D:0-7</td><td>The 8-bit field CONF controls the configuration of the modem according to the following table:
<table><tr><th>Hex Code</th><th>Configuration</th></tr><tr><td>04*</td><td>V.26B, Bell 201B/C, Scrambler/descrambler disabled</td></tr><tr><td>44</td><td>V.26A, Scrambler/descrambler disabled</td></tr><tr><td>84</td><td>V.26B, Bell 201B/C, Scrambler/descrambler enabled</td></tr><tr><td>C4</td><td>V.26A, Scrambler/descrambler enabled</td></tr><tr><td>0C</td><td>Tone</td></tr><tr><td colspan="2">*Default value at POR with 220 ms turn-on sequence.</td></tr></table>
Configuration Definitions
V.26/Bell 201—The modem operates as specified in CCITT Recommendation V.26 bis Alternate A or B, and Bell 201B/C, at a 2400 bps data rate.
Tone—The modem sends single or dual frequency tones in response to the $\overline{\text{RTS}}$ or RTSP signals. Tone frequencies and amplitudes are controlled by RAM locations written by the host. When not transmitting tones the Tone configuration allows detection of single frequency tones by the TDET bit. The tone detector frequency can be changed by the host by altering the contents of several RAM locations.</td></tr>
<tr><td>DDIE</td><td>Diagnostic Data Interrupt Enable</td><td>E:2</td><td>When set to a one, DDIE enables an IRQ interrupt to be generated when the diagnostic data request bit (DDREQ) is a one.</td></tr>
<tr><td>DDREQ</td><td>Diagnostic Data Request</td><td>E:0</td><td>DDREQ goes to a one when the modem reads from or writes to DDYL. DDREQ goes to a zero when the host processor reads from or writes to DDYL. Used for diagnostic data handshaking bit.</td></tr>
<tr><td>DDXL</td><td>Diagnostic Data X Least</td><td>2:0-7</td><td>Least significant byte of 16-bit word used in reading XRAM locations.</td></tr>
<tr><td>DDXM</td><td>Diagnostic Data X Most</td><td>3:0-7</td><td>Least significant byte of 16-bit word used in reading XRAM locations.</td></tr>
<tr><td>DDYL</td><td>Diagnostic Data Y Least</td><td>0:0-7</td><td>Least significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.</td></tr>
<tr><td>DDYM</td><td>Diagnostic Data Y Most</td><td>1:0-7</td><td>Most significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.</td></tr>
<tr><td>EQFZ</td><td>Equalizer Freeze</td><td>C:2</td><td>When EQFZ is a one, the adaptive equalizer taps stop updating and remain frozen.</td></tr>
<tr><td>FED</td><td>Fast Energy Detector</td><td>B:5,6</td><td>FED consists of a 2-bit field that indicates the level of received signal according to the following code.
<table><tr><th>Code</th><th>Energy Level</th></tr><tr><td>0</td><td>None</td></tr><tr><td>1</td><td>Invalid</td></tr><tr><td>2</td><td>Above Turn-off Threshold</td></tr><tr><td>3</td><td>Above Turn-on Threshold</td></tr></table>While receiving a signal, FED normally alternates between Codes 2 and 3.</td></tr>
</table>

R24BKJ Interace Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
GHIT	Gain Hit	B:4	The gain hit bit goes to one when the receiver detects a sudden increase in passband energy faster than the AGC circuit can correct. GHIT returns to zero when the AGC output returns to normal.
IA	Interrupt Active	E:7	IA is a one when the modem is driving the interrupt request line ($\overline{IRQ}$) to a low TTL level.
RAMA	RAM Access	F:0-7	The RAMA register is written by the host when reading or writing diagnostic data. The RAMA code determines the RAM location with which the diagnostic read or write is performed
RAMW	RAM Write	C:0	RAMW is set to a one by the host processor when performing diagnostic writes to the modem RAM. RAMW is set to a zero by the host when reading RAM diagnostic data.
RTSP	Request to Send Parallel	C:7	The one state of RTSP begins a transmit sequence. The modem continues to transmit until RTSP is turned off and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem.
RXCD	Receiver Channel Data	5:0-7	RXCD is written to by the modem every eight bit times. This byte of channel data can be read by the host when the receiver sets the channel data request bit (CDREQ).
RX	Receive State	B:7	RX is a one when the modem is in the receive state (i.e., not transmitting).
SETUP	Setup	E:3	The host processor must set the SETUP bit to a one when reconfiguring the modem, i.e., when changing CONF (D:0-7).
TDET	Tone Detected	A:7	The one state of TDET indicates reception of a tone. The filter can be retuned by means of the diagnostic write routine.
TPDM	Transmitter Parallel Data Mode	C:5	When control bit TPDM is a one, the transmitter accepts data for transmission from the TXCD register rather than the serial hardware data input.
TXCD	Transmitter Channel Data	4:0-7	The host processor conveys output data to the transmitter in parallel data mode by writing a data byte to the TXCD register when the channel data request bit (CDREQ) goes to a one. Data is transmitted as single bits in V.21 or as dibits in V.27 starting with bit 0 or dibit 0,1.

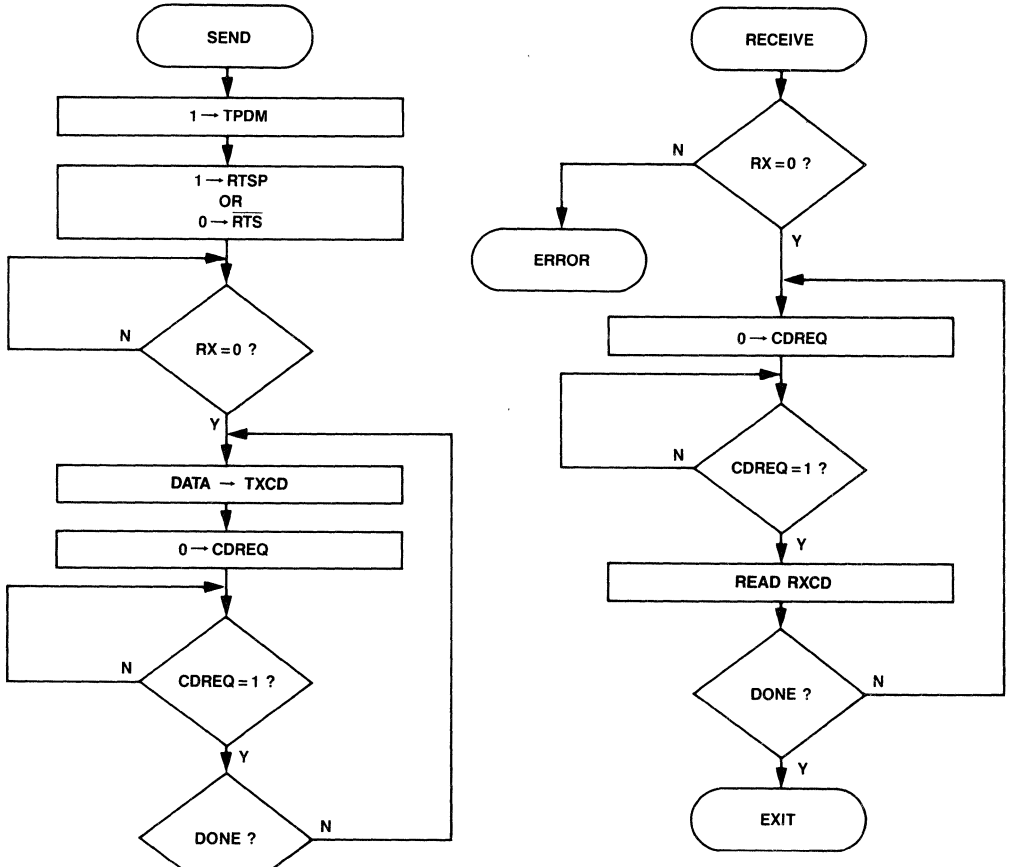
Diagnostic Data Transfer

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register F (RAMA). The R24BKJ RAM Access Codes table lists 27 access codes for storage in register F and the corresponding diagnostic functions. The R24BKJ Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long. These bits are written into interface memory registers 3, 2, 1 and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit C:0 (RAMW) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the more significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAMA bits of register F. When bit F:7 is set to one, the XRAM is selected. When F:7 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the diagnostic data request bit E:0 (DDREQ) is reset to zero. When the modem reads or writes register 0, DDREQ is set to a one. When set to a one by the host, bit E:2 (DDIE) enables the DDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) goes to a one.



Channel Data Parallel Mode Control

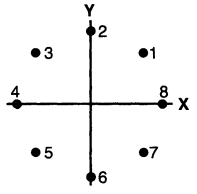
R24BKJ RAM Access Codes

Node	Function	RAMA	Reg. No.
1	AGC Gain Word	B1	2,3
2	Average Power	F2	2,3
3	Receiver Sensitivity	F1	2,3
4	Receiver Hysteresis	84	2,3
5	Equalizer Input	5B	0,1,2,3
6	Equalizer Tap Coefficients	1B-2A	0,1,2,3
7	Unrotated Equalizer Output	6B	0,1,2,3
8	Rotated Equalizer Output	0A	0,1,2,3
9	Decision Points	6C	0,1,2,3
10	Error Vector	6D	0,1,2,3
11	Rotation Angle	87	2,3
12	Frequency Correction	8B	2,3
13	EQM	B0	2,3
14	Alpha (α)	36	0,1
15	Beta One (β_1)	37	0,1
16	Beta Two (β_2)	38	0,1
17	Alpha Prime (α')	39	0,1
18	Beta One Prime (β_1')	3A	0,1
19	Beta Two Prime (β_2')	3B	0,1
20	Alpha Double Prime (α'')	B6	2,3
21	Beta Double Prime (β'')	B7	2,3
22	Output Level	43	0,1
23	Tone 1 Frequency	8E	2,3
24	Tone 1 Level	44	0,1
25	Tone 2 Frequency	8F	2,3
26	Tone 2 Level	45	0,1
27	Checksum	02	0,1
28	Fixed Synchronizing Segment	11	2,3
29	Open Synchronizing Segment	11	0,1

R24BKJ Diagnostic Data Scaling

Node	Parameter/Scaling
1	**AGC Gain Word** (16-bit unsigned). AGC Gain in dB = 50 – [(AGC Gain Word/64) × 0.098] Range: $(16C0)_{16}$ to $(7FFF)_{16}$, For –43 dBm Threshold
2.	**Average Power** (16-bit unsigned) Post-AGC Average Power in dBm = 10 Log (Average Power Word/2185) Typical Value = $(0889)_{16}$, corresponding to 0 dBm Pre-AGC Power in dBm = (Post-AGC Average Power–AGC Gain)
3	**Receiver Sensitivity** (16-bit twos complement) On-Number = 655.36 (52.38 + P_{ON}) where: P_{ON} = Turn-on threshold in dB Convert On-Number to hexadecimal and store at access code F1
4	**Receiver Hysteresis** (16-bit twos complement) Off-Number = $[65.4\ (10^A)]^2/2$ where: A = (P_{OFF} – P_{ON} – 0.5)/20 P_{ON} = Turn-on threshold in dB P_{OFF} = Turn-off threshold in dB Convert Off-Number to hexadecimal and store at access code 84

R24BKJ Diagnostic Data Scaling

Node	Parameter/Scaling
5,7–9	**All base-band signal point nodes** (i.e., Equalizer Input, Unrotated Equalizer Output, Rotated Equalizer Output, and Decision Points) are 32-bit, complex, twos complement numbers. Point 1: X 1600, Y 1600 Point 2: X 0000, Y 1F1C Point 3: X EA00, Y 1600 Point 4: X E0E4, Y 0000 Point 5: X EA00, Y EA00 Point 6: X 0000, Y E0E4 Point 7: X 1600, Y EA00 Point 8: X 1F1C, Y 0000 
6	**Equalizer Tap Coefficients** (32-bit, complex, twos complement) Complex numbers with X = real part, Y = imaginary part X and Y range: 0000 to $(FFFF)_{16}$ representing ± full scale in hexadecimal twos complement.
10	**Error Vector** (32-bit, complex, twos complement) Complex number with X = real part, Y = imaginary part. X and Y range: $(8000)_{16}$ to $(7FFF)_{16}$
11	**Rotation Angle** (16-bit, signed, twos complement) Rotation Angle in deg. = (Rot. Angle Word/65,536) × 360
12	**Frequency Correction** (16-bit signed twos complement) Frequency correction in Hz = (Freq. Correction Word/65,536) × Baud Rate Range: $(FC00)_{16}$ to $(400)_{16}$ representing ± 18.75 Hz
13	**EQM** (16-bit, unsigned) Filtered squared magnitude of error vector. Proportionality to BER determined by particular application.
14–21	**Filter Tuning Parameters** (16-bit unsigned) Alpha, Beta One, Beta Two, Alpha Prime, Beta One Prime, Beta Two Prime, Alpha Double Prime, and Beta Double Prime are set according to instructions in application note 668. Use a sample rate of 7200 samples per second for all calculations.
22	**Output Level** (16-bit unsigned) Output Number = 27573.6 $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store at access code 43
24 and 26	**Tone 1 and Tone 2 Levels** Calculate the power of each tone independently by using the equation for Output Number given at node 22. Convert these numbers to hexadecimal then store at access codes 44 and 45. Total power transmitted in tone mode is the result of both tone 1 power and tone 2 power.
23 and 25	**Tone 1 and 2 Frequency** (16-bit unsigned) N = 9.1022 (Frequency in Hz) Convert N to hexadecimal then store at access code 8E or 8F.
27	**Checksum** (16-bit unsigned) ROM checksum number determined by revision level.
28,29	**Fixed and Open Synchronizing Segments** (16-bit unsigned) Synchronizing Sequence = [Fixed + (Open + 1)] baud times (± 1 baud time) $7FFF_{16} \geq$ Fixed, Open baud times ≥ 0 (baud time = 1/1200 = 0.833 ms) Fixed = unscrambled ones Open = unscrambled or scrambled ones

3

POWER-ON INITIALIZATION

When power is applied to the R24BKJ, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below approximately 3 Vdc for more than 30 msec, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.26B, scrambler disabled, serial mode, 90 ms synchronizing signal, interrupt disabled, RAM access code 0A, transmitter output level set for +5 dBm at TXA, receiver turn-on threshold set for –43.5 dBm, receiver turn-off threshold set for –47.0 dBm, tone 1 and tone 2 set for 0 Hz and 0 volts output, and tone detector parameters zeroed.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

The R24BKJ provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that illustrated in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm.

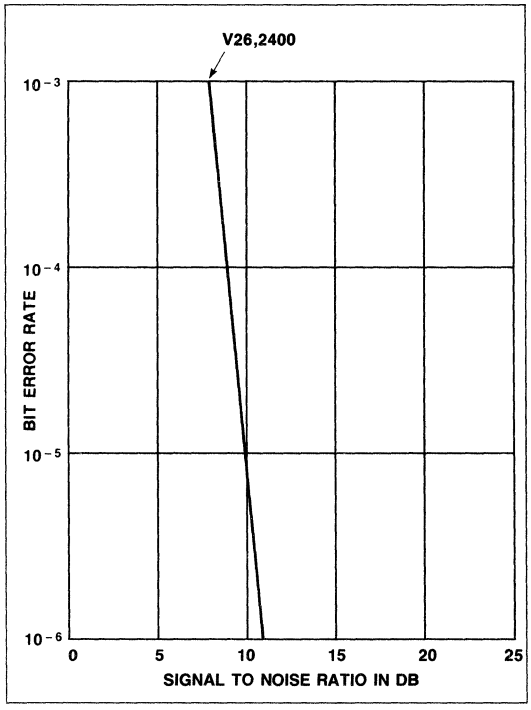
RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R24BKJ can adapt to received frequency error of ±10 Hz with less than 0.2 dB degradation in BER performance.

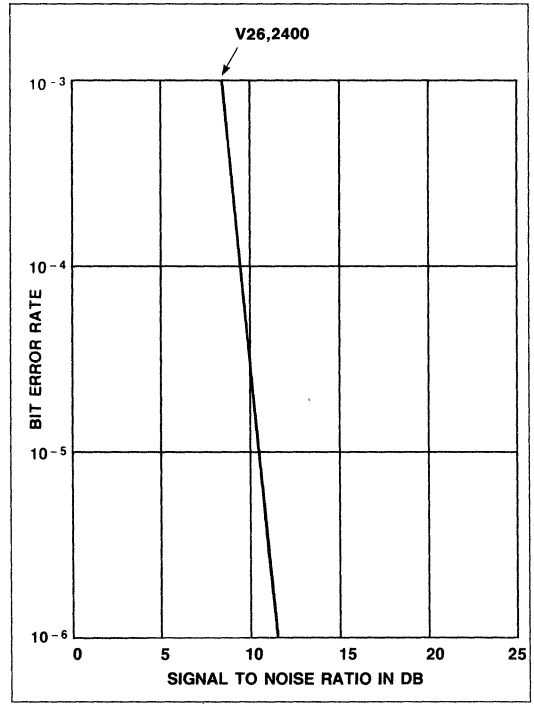
TYPICAL PHASE JITTER

The modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

An example of the BER performance capabilities is given in the following diagrams:

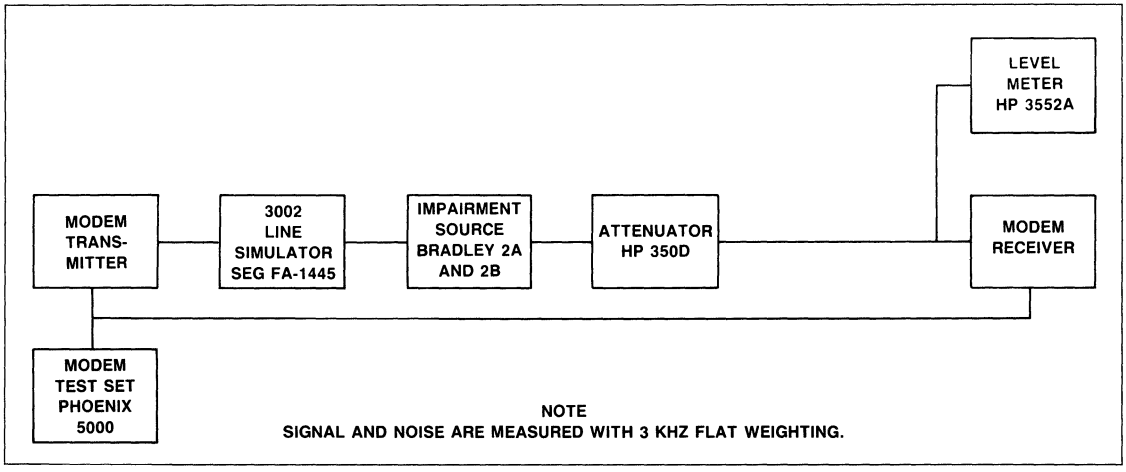


Typical Bit Error Rate (Back-to-Back, Level –20 dBm)



Typical Bit Error Rate (Unconditioned 3002 Line, Level –20 dBm)

The BER performance test set-up is show in the following diagram:



BER Performance Test Set-up

APPLICATION

Recommended Modem Interface Circuit

The R24BKJ is supplied as a 64-pin QUIP device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit and parts list illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R2 and R3 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3k Ω series resistor should be used on each input (Pins 32 and 33) for isolation.

Resistors R4 and R9 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dB the 1% resistor values shown are correct for more than 99.8% of the units.

Typical Modem Interface Parts List

Component	Manufacturer's Part Number	Manufacturer
C3,C5,C7,C9	592CX7R104M050B	Sprague
C2	N511BY100JW	San Fernando/ Wescap
C1	C114C330J2G5CA	Kemet
C11	SA405C274MAA	AVX
Y1	333R14-002	Uniden
Z1	LM1458N	National
R5,R6	CML 1/10 T86.6K ohm ±1%	Dale Electronics
R4	5MA434.0K ±1%	Corning Electronics
R11	5043CX3R000J	Mepco Electra
R10	5043CX2M700J	Mepco Electra
R1	5043CX47K00J	Mepco Electra
R7	5043CX3K00J	Mepco Electra
R2,R3	5043CX1K00J	Mepco Electra
C10	ECEBEF100	Panasonic
C8	SMC50T1R0M5X12	United Chem-Con
C4,C6	C124C102J5G5CA	Kemet
CR1	IN751D	I.T.T.
R9	CRB¼XF47K5	R-Ohm
R8	ER025QKF2370	Matsushita Electric
R14	Determined by $\overline{IRQ}$ characteristics	

PC Board Layout Considerations

1. The R24BKJ and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board (PCB).
2. All power traces should be at least 0.1 inch width.
3. If power source is located more than approximately 5 inches from the R24BKJ, a decoupling capacitor of 10 microfarad or greater should be placed in parallel with C11 near pins 11 and 48.
4. All circuitry connected to pins 9 and 10 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the R24BKJ package. Pin 24 should tie directly, by a unique path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and all analog ground points shown in the recommended circuit diagram.
7. Pins 4, 8, 29, and 48 should tie together at the R24BKJ package. Pin 48 should tie directly, by a unique path, to the common ground point for analog and digital ground.
8. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 48 and all digital ground points shown in the recommended circuit diagram plus the crystal-can ground.
9. The R24BKJ package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
10. As a general rule, digital signals should be routed on the component side of the PCB while analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
11. Routing of R24BKJ signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to the table of noise characteristics for a list of pins in each category.

Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	Low	High
1	6	3	26	23
2	7	4	28	27
5	9	8	32	35
14	10	11	33	36
15	12	16		37
20	13	22		
21	17	24		
30	18	25		
38	19	29		
39	45	31		
40	46	34		
41	49	42		
44	50	43		
	51	47		
	52	48		
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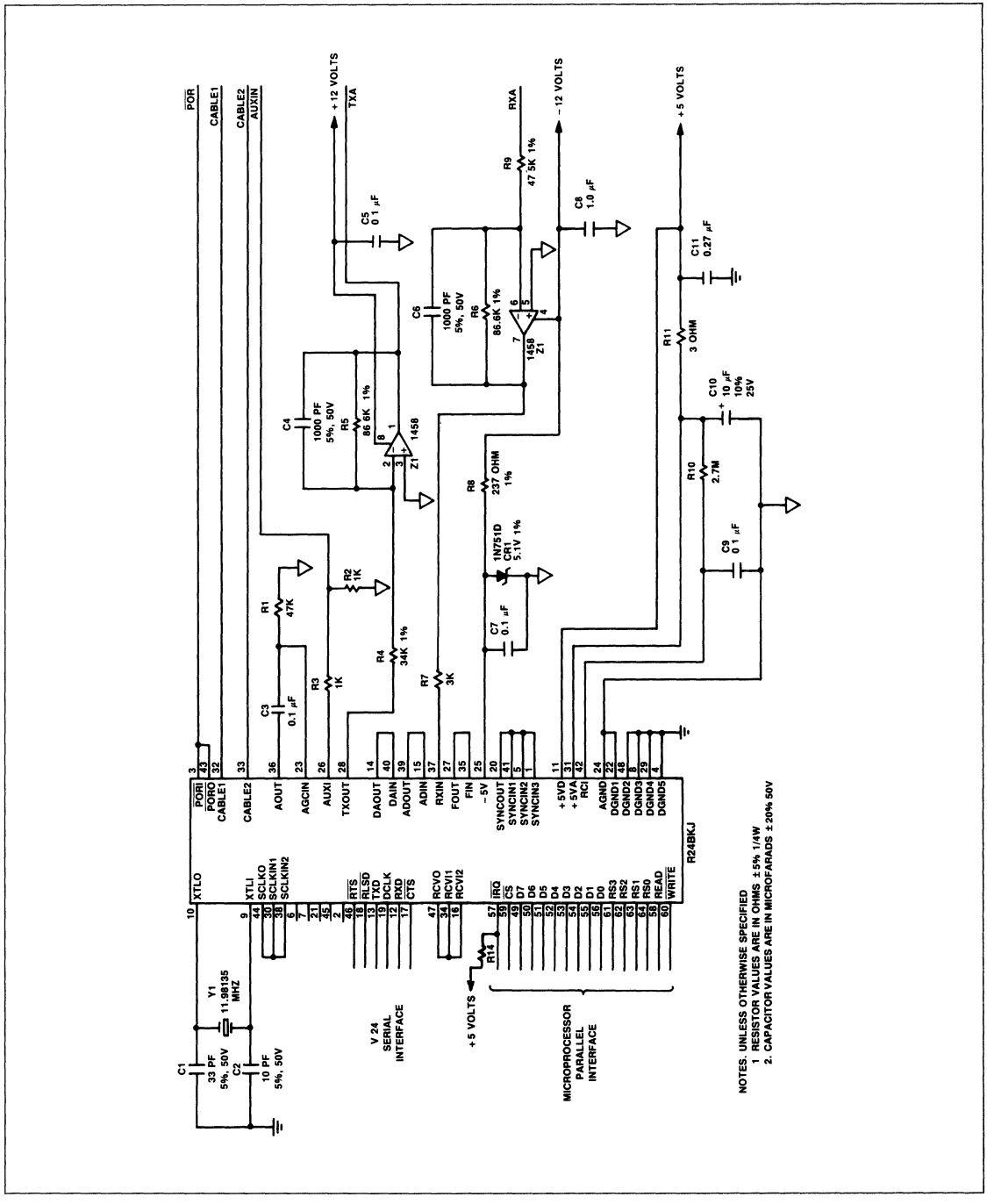
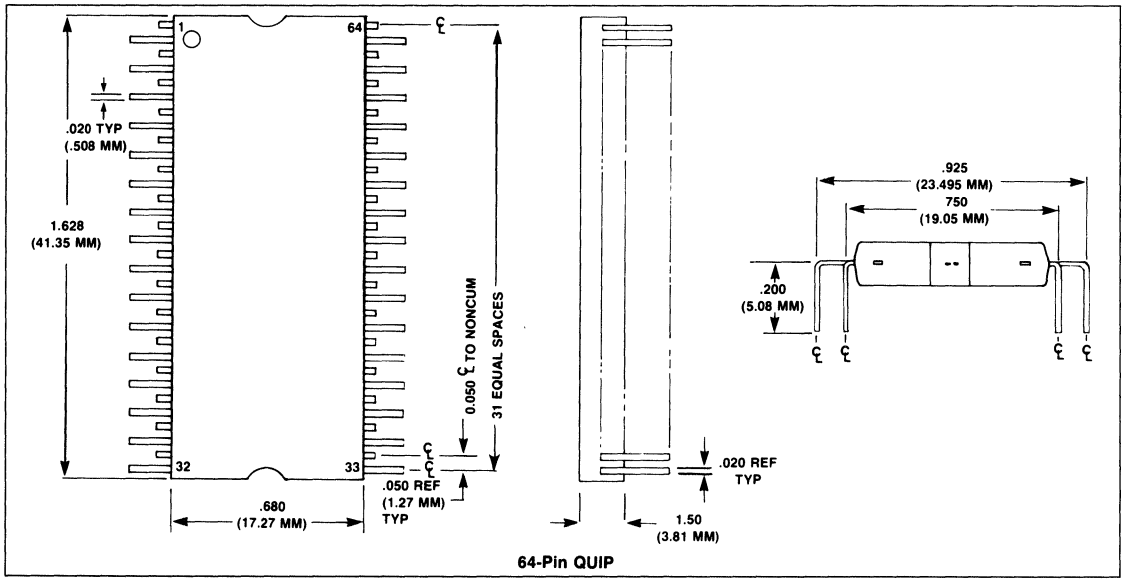


Recommended Modem Interface Circuit

PACKAGE DIMENSIONS



64-Pin QUIP

Rockwell

R48MFX
4800 bps MONOFAX™ Modem

INTRODUCTION

The R48MFX MONOFAX 48 is a synchronous, serial/parallel, 4800 bps modem in a single 64-pin quad in-line package (QUIP). The modem is designed for operation over the public switched telephone network with appropriate line terminations, such as a data access arrangement, provided externally.

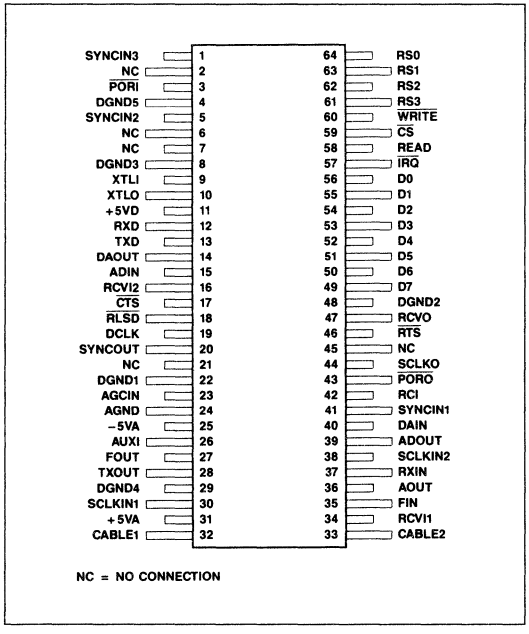
The R48MFX satisfies the telecommunications requirements specified in CCITT Recommendation V.27 ter, T.4 and the binary signaling capabilities of Recommendation T.30.

The R48MFX is optimized for use in compact Group 3 facsimile machines. Its small size and low power consumption offer the user flexibility in creating a 4800 bps modem customized for specific packaging and functional requirements.

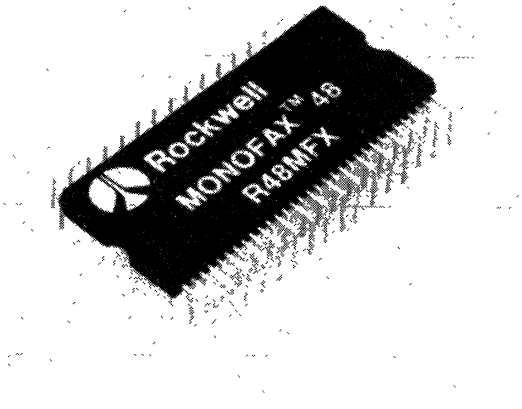
™MONOFAX is a trademark of Rockwell International

FEATURES

- Single 64-Pin QUIP
- CCITT V.27 ter, T.30, V.21 Channel 2, T.4
- Group 3 Facsimile Transmission/Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Dynamic Range: −43 dBm to 0 dBm
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R48MFX Pin Assignments



R48MFX 4800 bps MONOFAX Modem

TECHNICAL CHARACTERISTICS

TONE GENERATION

Under control of the host processor, the R48MFX can generate single or dual frequency voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. The transmit level and frequency of each tone is independently programmable.

TONE DETECTION

Single frequency tones are detected by a programmable filter. The presence of energy at the selected frequency is indicated by a bit in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Configuration	Parameter	Specification (±0.01%)
V.27	Signaling Rate	1600 Baud
	Data Rate	4800 bps
	Signaling Rate	1200 Baud
	Data Rate	2400 bps
V.21	Signaling Rate	300 Baud
	Data Rate	300 bps

DATA ENCODING

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

At 300 baud, the data stream is 300 bps FSK per CCITT V.21 channel 2.

COMPROMISE CABLE EQUALIZERS

In addition to the adaptive equalizer, the R48MFX provides selectable compromise cable equalizers to optimize performance over three different lengths of non-loaded cable of 0.4 mm diameter (1.8 km, 3.6 km, and 7.2 km).

Cable Equalizer Nominal Gain

Frequency (Hz)	Gain (dB) Relative to 1700 Hz		
	1.8 km	3.6 km	7.2 km
700	−0.99	−2.39	−3.93
1500	−0.20	−0.65	−1.22
2000	+0.15	+0.87	+1.90
3000	+1.43	+3 06	+4.58

TRANSMITTED DATA SPECTRUM

When operating at 1600 baud, the transmitter spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitter spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically meet the requirements of foreign telephone regulatory agencies.

SCRAMBLER/DESCRAMBLER

The R48MFX incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT V.27 ter. The scrambler can be disabled by setting a bit in interface memory.

RECEIVE LEVEL

The receiver circuit of the R48MFX satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. An external input buffer and filter must be supplied between the receiver analog input (RXA) and the R48MFX RXIN pin. The received line signal level is measured at RXA.

RECEIVE TIMING

In the receive state, the R48MFX provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is programmable. An external output buffer and filter must be supplied between the R48MFX TXOUT pin and the transmitter analog output (TXA). The default level at TXA is +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R48MFX provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency:* Selected data rate of 4800, 2400 or 300 Hz (±0.01%).
2. *Duty Cycle:* 50% ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

Seven turn-on sequences are generated by the R48MFX, as defined in the following table:

Turn-On Sequences[1]

No.	Bit Rate (bps)	$\overline{RTS}$ On-$\overline{CTS}$ On Time[1] (ms)	Comments
1	300	<14	No Training Sequence, No Echo Tone
2	2400	943	Long Train, No Echo Tone
3	2400	1148	Long Train, with Echo Tone[2]
4	2400	<10	Training Disabled
5	4800	708	Long Train, No Echo Tone
6	4800	913	Long Train, with Echo Tone[2]
7	4800	<10	Training Disabled

Notes:

1. Assumes the receiver is in idle; if not, add receiver turn-off time.
2. For use on lines with protection against talker echo.

TURN-OFF SEQUENCE

Five turn-off sequences are generated by the R48MFX:

Turn-Off Sequences

No.	Bit Rate (bps)	$\overline{RTS}$ Off-Energy Off Time (ms)	Silence Time (ms)
1	300	<7	0
2	2400 serial	7.5	20
3	2400 parallel	7.5-10	20
4	4800 serial	5.4	20
5	4800 parallel	5.4-6.7	20

CLAMPING

The following clamps are provided with the R48MFX:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector (RLSD).* $\overline{RLSD}$ is clamped off (squelched) whenever $\overline{RTS}$ is on.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the bit rate, the length of the training sequence, and the presence of the echo tone. The Turn-On Sequences table on page 2 lists the $\overline{CTS}$ response times.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

$\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RLSD}$ off-to-on response time is 801 bauds (V.27) or <10 ms (300 bps). The $\overline{RLSD}$ on-to-off response time is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Receiver threshold is programmable over the range 0 dBm to −50 dBm, however, performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to RXA.

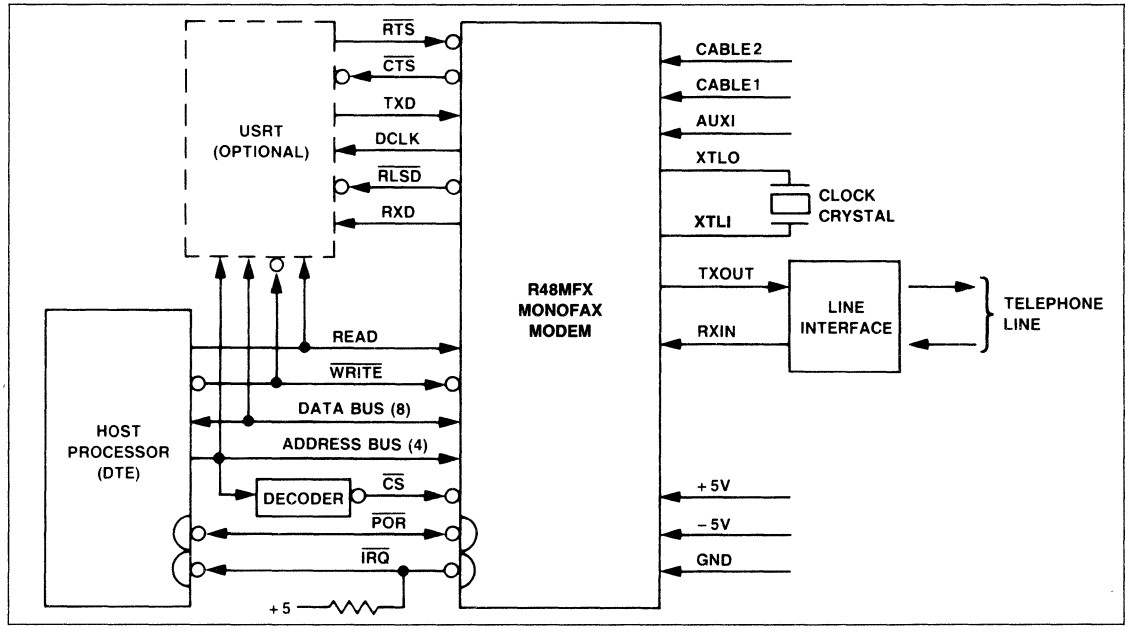
POWER

Voltage	Tolerance	Current (Max) @ 25°C	Current (Max) @ 60°C
+5 Vdc	±5%	250 mA @ 5.0 Vdc	225 mA @ 5.0 Vdc
−5 Vdc	±5%	25 mA @ −5.0 Vdc	25 mA @ −5.0 Vdc

Note: All voltages must have ripple ≤0.1 volts peak-to-peak. If a switching supply is chosen, user may select any frequency between 20 kHz and 150 kHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak.

ENVIRONMENTAL

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in suitable antistatic container).
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.



R48MFX Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins on the 64-pin QUIP. Software circuits are assigned to specific bits in a 16-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R48MFX Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital and Analog Interface Characteristics tables.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

R48MFX Hardware Circuits

Name	Type	Pin No.	Description
A. POWER:			
AGND	GND	24	Connect to Analog Ground
DGND1	GND	22	Connect to AGND Ground
DGND2	GND	48	Connect to Digital Ground
DGND3	GND	8	Connect to Digital Ground
DGND4	GND	29	Connect to Digital Ground
DGND5	GND	4	Connect to Digital Ground
+5 VA	PWR	31	Connect to Analog +5V Power
+5 VD	PWR	11	Connect to Digital +5V Power
−5 VA	PWR	25	Connect to Analog −5V Power
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	49	Data Bus (8 Bits)
D6	I/OA	50	
D5	I/OA	51	
D4	I/OA	52	
D3	I/OA	53	
D2	I/OA	54	
D1	I/OA	55	
D0	I/OA	56	
RS3	IA	61	Register Select (4 Bits) Select Reg. 0−F
RS2	IA	62	
RS1	IA	63	
RS0	IA	64	
$\overline{CS}$	IA	59	Chip Select
$\overline{READ}$	IA	58	Read Strobe
$\overline{WRITE}$	IA	60	Write Strobe
$\overline{IRQ}$	OB	57	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	19	Data Clock
$\overline{RTS}$	IB	46	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	13	Transmitter Data Signal
RXD	OC	12	Receiver Data Signal
$\overline{RLSD}$	OC	18	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABLE1	IC	32	Cable Select 1
CABLE2	IC	33	Cable Select 2

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXOUT	AA	28	Connect to Output Op Amp
RXIN	AB	37	Connect to Input Op Amp
AUXI	AC	26	Auxiliary Analog Input
F. OVERHEAD			
$\overline{PORO}$	I/OB	43	Power-On-Reset Output
$\overline{PORI}$	I/OB	3	Power-On-Reset Input
XTLO	R*	10	Connect to Crystal Circuit
XTLI	R*	9	Connect to Crystal Circuit
RCVO	R*	47	Receive Mode Output
RCVI1	R*	34	Connect to RCVO
RCVI2	R*	16	Connect to RCVO
SCLKO	R*	44	Switched Capacitor Clock Output
SCLKIN1	R*	30	Connect to SCLKO
SCLKIN2	R*	38	Connect to SCLKO
AOUT	R*	36	Smoothing Filter Output
AGCIN	R*	23	AGC Input
DAOUT	R*	14	DAC/AGC Data Out
DAIN	R*	40	Connect to DAOUT
ADOUT	R*	39	ADC Output
ADIN	R*	15	Connect to ADOUT
FOUT	R*	27	Smoothing Filter Output
FIN	R*	35	Connect to FOUT
SYNCOUT	R*	20	Sample Clock Output
SYNCIN1	R*	41	Connect to SYNCOUT
SYNCIN2	R*	5	Connect to SYNCOUT
SYNCIN3	R*	1	Connect to SYNCOUT
RCI	R*	42	RC Junction for POR Time Constant
G. RESERVED			
	R*	2	Do Not Connect
	R*	6	Do Not Connect
	R*	7	Do Not Connect
	R*	21	Do Not Connect
	R*	45	Do Not Connect

*R = Required overhead connection; no connection to host equipment.

Digital Interface Characteristics

Symbol	Parameter	Units	Type							
			Input			Output			Input/Output	
			IA	IB	IC	OA	OB	OC	I/OA	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min.[1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1 6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

Analog Interface Characteristics

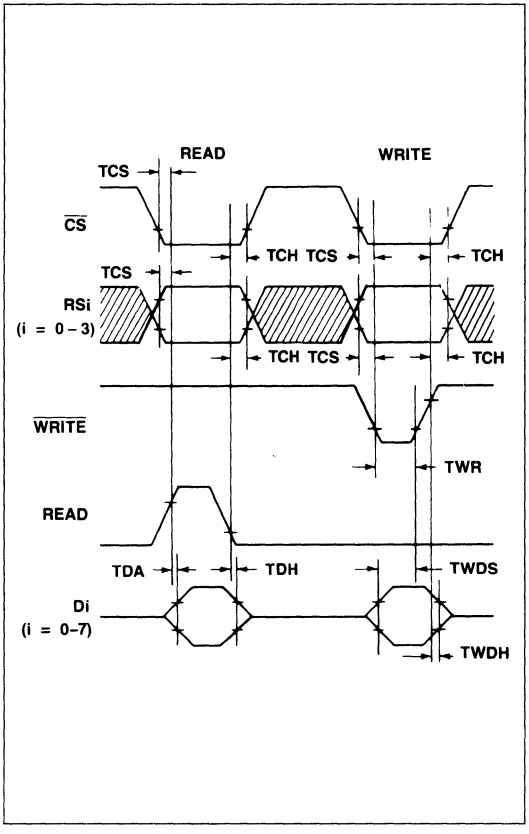
Analog Interface Characteristics

Name	Type	Characteristics
TXOUT	AA	The transmitter output can supply a maximum of ±3.03 volts into a load resistance of 10k Ω minimum. In order to match to 600 Ω, an external smoothing filter with a transfer function of 15726.43/(S+11542.44) and 604 Ω series resistor are required.
RXIN	AB	The receiver input impedance is greater than 1M Ω. An external antialiasing filter with a transfer function of 19533.88/(S+11542.44) is required.
AUXI	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1M Ω, and the gain to transmitter output (TXA) is +5.6 dB ±1 dB.

Note: Absolute maximum voltage ratings for analog inputs are: (−5 VA − 0.3) ≤ V_{IN} ≤ (+5 VA + 0.3)

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to READ or $\overline{WRITE}$	TCS	30	—	ns
Data Access time after READ	TDA	—	140	ns
Data hold time after READ	TDH	10	50	ns
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
$\overline{WRITE}$ strobe pulse width	TWR	75	—	ns



Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABLE2	CABLE1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs. Signals TXOUT and RXIN require buffering and filtering to be suitable for driving and receiving the communication channel. Signal AUXI provides access to the transmitter for summing host audio signals with the modem analog output.

The filters required for anti-aliasing on the receiver input and smoothing on the transmitter output have a single pole located at 11,542 radians. Although this pole is located within the modem passband, internal filters compensate for its presence and, therefore, the pole location must not be changed. Some variation from recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10k Ω.

Notice that when reference is made to signals TXA, RXA, and AUXIN, these signals are not electrically identical to TXOUT, RXIN, and AUXI. The schematic of the recommended modem interface circuit illustrates the differences.

Overhead

Except for the power-on-reset signal $\overline{\text{PORO}}$, the overhead signals are intended for internal use only. The various required connections are illustrated in the recommended modem interface circuit schematic. No host connections should be made to overhead signals other than $\overline{\text{PORO}}$.

SOFTWARE CIRCUITS

The R48MFX contains 16 memory mapped registers to which an external (host) microprocessor has access. The host may read data out of or write data into these registers. Refer to the R48MFX Host Processor Interface figure.

When information in these registers is being discussed, the format Z:Q is used. The register is specified by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a one (1) and "off" when reset to a zero (0).

Status/Control Bits

The operation of the R48MFX is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus.

All status and control bits are defined in the R48MFX Interface Memory Map table. Bits designated by ' — ' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Configuration Control

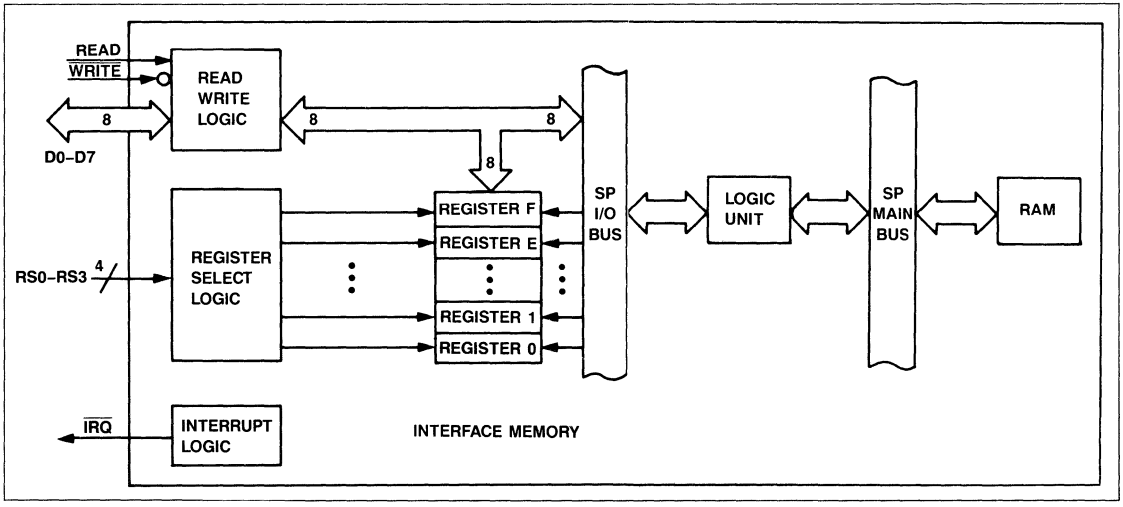
Four configurations are available in the R48MFX modem: V.27 4800/2400 bps long train, V.21, and Tone. The configuration is selected by writing an 8-bit binary code into the configuration field (CONF) of the interface memory. The configuration field consists of bits 7 through 0 of register D. The code for these bits is shown in the following table. All other codes represent invalid states.

Configuration Codes

CONF Code	Configuration
00	V.21
04	V.27, 2400 Long Train
06*	V.27, 4800 Long Train
08	Tone Mode
* Default value at POR.	

When the modem is initialized by power-on-reset, the configuration defaults to V.27 4800 bps. When the host wants to change configuration, the new code is written to the configuration field and the SETUP bit (E:3) is set to a one. Once the new configuration takes effect, the SETUP bit is reset to zero by the modem.

The information in the interface memory is serviced by the modem at the baud rate (V.27 and V.21), 9600 times per second (tone generator), or 1600 times per second (tone detector).



R48MFX Host Processor Interface

R48MFX Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAMA							
E	IA	CDIE	CDREQ	—	SETUP	DDIE	—	DDREQ
D	CONF							
C	RTSP	EPT	TPDM	TDIS	EQSV	EQFZ	SDIS	RAMW
B	RX	FED		GHIT	—	—	—	—
A	TDET	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	CDET	—	PN	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RXCD							
4	TXCD							
3	DDXM							
2	DDXL							
1	DDYM							
0	DDYL							
Register / Bit	7	6	5	4	3	2	1	0

Channel Data Transfer

Data sent to or received from the data channel may be transferred between the modem and host processor in either serial or parallel form. The receiver operates in both serial and parallel mode simultaneously and requires no mode control bit selection. The transmitter operates in either serial or parallel mode as selected by mode control bit C:5 (TPDM).

To enable the transmitter parallel mode, TPDM must be set to a 1. The modem automatically defaults to the serial mode (TPDM = 0) at power-on. In either transmitter serial or parallel mode, the R48MFX is configured by the host processor via the microprocessor bus.

Serial Mode—The serial mode uses a standard V.24 (RS-232-C) hardware interface (optional USRT) to transfer channel data. Transmitter data can be sent serially only when TPDM is set to a zero.

Parallel Mode—Parallel data is transferred via two registers in the interface memory. Register 5 (RXCD) is used for receiver channel data, and Register 4 (TXCD) is used for transmitter channel data. Register 5 is continuously written every eight bit times when in the receive state. Register 4 is used as the source of channel transmitter data only when bit C:5 (TPDM) is set to a one by the host. Otherwise the transmitter reads data from the V.24 interface. Both $\overline{RTS}$ and RTSP remain enabled, however, regardless of the state of TPDM.

When performing parallel data transfer of channel data, the host and modem can synchronize their operations by handshaking bits in register E. Bit E:5 (CDREQ) is the channel data request bit. This bit is set to a one by the modem when receiver data is available in RXCD or when transmitter data is required in TXCD. Once the host has finished reading RXCD or writing TXCD, the host processor must reset CDREQ by writing a zero to that bit location.

When set to a one by the host, Bit E:6 (CDIE) enables the CDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) is a one.

If the host does not respond to the channel data request within eight bit times, the RXCD register is over written or the TXCD register is sent again.

Refer to Channel Data Parallel Mode Control flow chart for recommended software sequence.

R48MFX Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
CDET	Carrier Detector	8:5	The one state of CDET indicates passband energy is being detected, and a training sequence is not present. CDET goes to one at the start of the data state, and returns to zero at the end of the received signal. CDET activates one baud time before $\overline{\text{RLSD}}$ and deactivates one baud time after $\overline{\text{RLSD}}$.
CDIE	Channel Data Interrupt Enable	E:6	When set to a one, CDIE enables an $\overline{\text{IRQ}}$ interrupt to be generated when the channel data request bit (CDREQ) is a one.
CDREQ	Channel Data Request	E:5	Parallel data mode handshaking bit. Set to a one when the modem receiver writes data to RXCD, or the modem transmitter reads data from TXCD. CDREQ must be reset to zero by the host processor when data service is complete.
CONF	Configuration	D:0-7	The 8-bit field CONF controls the configuration of the modem according to the following table: **Hex Code** — **Configuration** 00 — V.21 04 — V.27, 2400 Long Train 06 — V.27, 4800 Long Train (Default) 08 — Tone All else — Invalid **Configuration Definitions** *V.21*—The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 Channel 2 modulation system. *Tone*—The modem sends single or dual frequency tones in response to the $\overline{\text{RTS}}$ or RTSP signals. Tone frequencies and amplitudes are controlled by RAM locations written by the host. When not transmitting tones the Tone configuration allows detection of single frequency tones by the TDET bit. The tone detector frequency can be changed by the host by altering the contents of several RAM locations. *V.27*—The modem is compatible with CCITT Recommendation V.27 ter.
DDIE	Diagnostic Data Interrupt Enable	E:2	When set to a one, DDIE enables an IRQ interrupt to be generated when the diagnostic data request bit (DDREQ) is a one.
DDREQ	Diagnostic Data Request	E:0	DDREQ goes to a one when the modem reads from or writes to DDYL. DDREQ goes to a zero when the host processor reads from or writes to DDYL. Used for diagnostic data handshaking bit.
DDXL	Diagnostic Data X Least	2:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDXM	Diagnostic Data X Most	3:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDYL	Diagnostic Data Y Least	0:0-7	Least significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
DDYM	Diagnostic Data Y Most	1:0-7	Most significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
EPT	Echo Protector Tone	C:6	When EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. EPT is not active if TDIS is on.
EQFZ	Equalizer Freeze	C:2	When EQFZ is a one, the adaptive equalizer taps stop updating and remain frozen.
EQSV	Equalizer Save	C:3	When EQSV is a one, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training.
FED	Fast Energy Detector	B:5,6	FED consists of a 2-bit field that indicates the level of received signal according to the following code. **Code** — **Energy Level** 0 — None 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold While receiving a signal, FED normally alternates between Codes 2 and 3.

R48MFX Interace Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
GHIT	Gain Hit	B:4	The gain hit bit goes to one when the receiver detects a sudden increase in passband energy faster than the AGC circuit can correct. GHIT returns to zero when the AGC output returns to normal.
IA	Interrupt Active	E.7	IA is a one when the modem is driving the interrupt request line ($\overline{IRQ}$) to a low TTL level.
PN	Period N	8:3	PN sets to a one at the start of the received PN sequence. PN resets to zero at the start of the received scrambled ones. PN does not operate when TDIS is set to a one.
RAMA	RAM Access	F:0-7	The RAMA register is written by the host when reading or writing diagnostic data. The RAMA code determines the RAM location with which the diagnostic read or write is performed.
RAMW	RAM Write	C:0	RAMW is set to a one by the host processor when performing diagnostic writes to the modem RAM. RAMW is set to a zero by the host when reading RAM diagnostic data.
RTSP	Request to Send Parallel	C:7	The one state of RTSP begins a transmit sequence. The modem continues to transmit until RTSP is turned off and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem.
RXCD	Receiver Channel Data	5.0-7	RXCD is written to by the modem every eight bit times. This byte of channel data can be read by the host when the receiver sets the channel data request bit (CDREQ).
RX	Receive State	B:7	RX is a one when the modem is in the receive state (i.e., not transmitting).
SDIS	Scrambler Disable	C:1	When SDIS is a one, the scrambler/descrambler is disabled. When SDIS is a zero, the scrambler/descrambler is enabled (default)
SETUP	Setup	E:3	The host processor must set the SETUP bit to a one when reconfiguring the modem, i.e., when changing CONF (D:0-7).
TDET	Tone Detected	A:7	The one state of TDET indicates reception of a tone. The filter can be retuned by means of the diagnostic write routine.
TDIS	Training Disable	C:4	If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one when $\overline{RTS}$ or RTSP go active, the generation of a training sequence is prevented at the start of transmission.
TPDM	Transmitter Parallel Data Mode	C:5	When control bit TPDM is a one, the transmitter accepts data for transmission from the TXCD register rather than the serial hardware data input.
TXCD	Transmitter Channel Data	4:0-7	The host processor conveys output data to the transmitter in parallel data mode by writing a data byte to the TXCD register when the channel data request bit (CDREQ) goes to a one. Data is transmitted as single bits in V.21 or as dibits in V.27 starting with bit 0 or dibit 0,1.

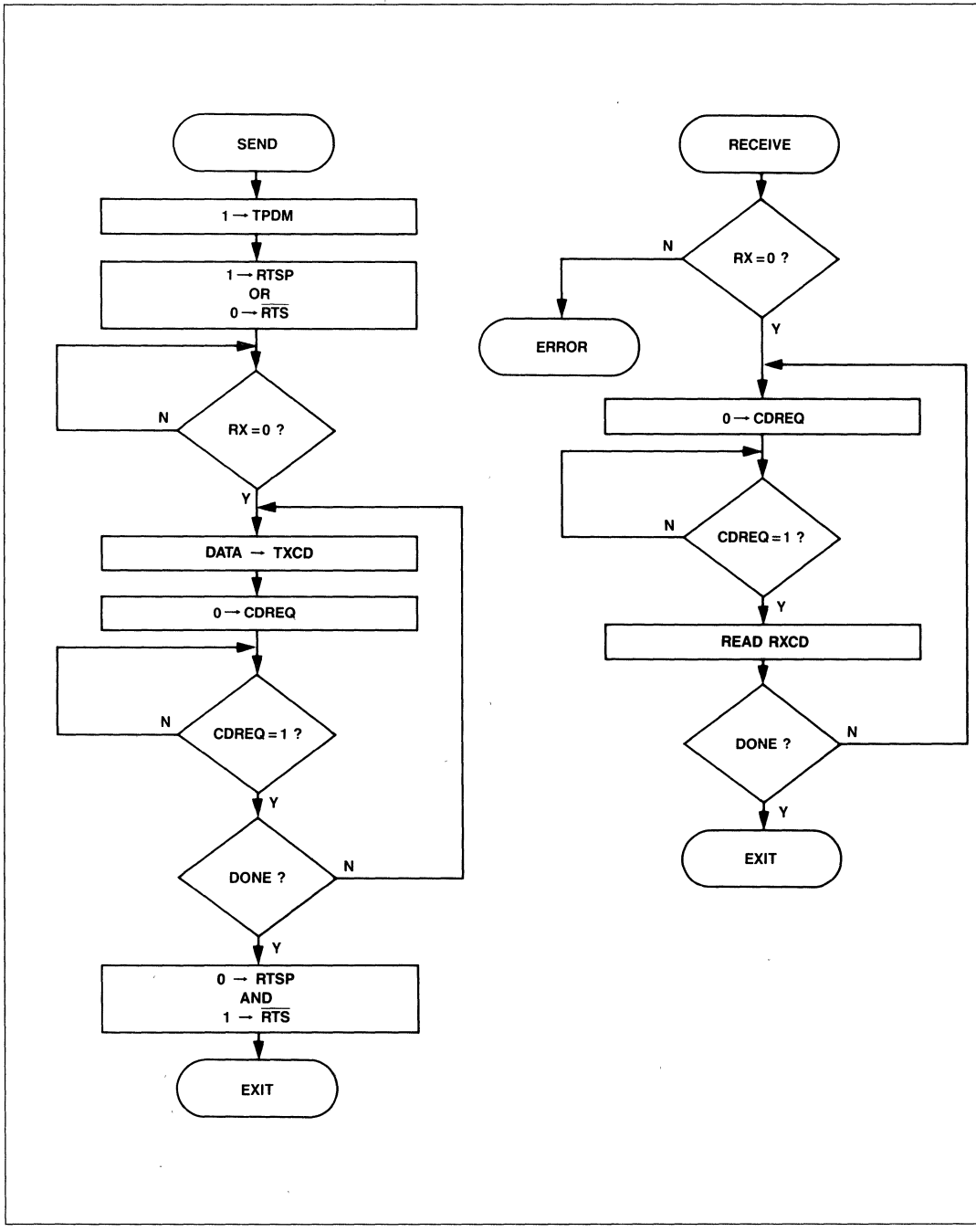
Diagnostic Data Transfer

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register F (RAMA). The R48MFX RAM Access Codes table lists 27 access codes for storage in register F and the corresponding diagnostic functions. The R48MFX Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long. These bits are written into interface memory registers 3, 2, 1 and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit C:0 (RAMW) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the more significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAMA bits of register F. When bit F:7 is set to one, the XRAM is selected. When F:7 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the diagnostic data request bit E:0 (DDREQ) is reset to zero. When the modem reads or writes register 0, DDREQ is set to a one. When set to a one by the host, bit E:2 (DDIE) enables the DDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) goes to a one.



Channel Data Parallel Mode Control

R48MFX RAM Access Codes

Node	Function	RAMA	Reg. No.
1	AGC Gain Word	87	2,3
2	Average Power	91	2,3
3	Receiver Sensitivity	47	0,1
4	Receiver Hysteresis	84	2,3
5	Equalizer Input	63	0,1,2,3
6	Equalizer Tap Coefficients	23-32	0,1,2,3
7	Unrotated Equalizer Output	73	0,1,2,3
8	Rotated Equalizer Output	0A	0,1,2,3
9	Decision Points	74	0,1,2,3
10	Error Vector	75	0,1,2,3
11	Rotation Angle	B3	2,3
12	Frequency Correction	8B	2,3
13	EQM	89	2,3
14	Alpha (α)	38	0,1
15	Beta One (β_1)	39	0,1
16	Beta Two (β_2)	3A	0,1
17	Alpha Prime (α')	3B	0,1
18	Beta One Prime (β_1')	3C	0,1
19	Beta Two Prime (β_2')	3D	0,1
20	Alpha Double Prime (α'')	B8	2,3
21	Beta Double Prime (β'')	B9	2,3
22	Output Level	43	0,1
23	Tone 1 Frequency	8E	2,3
24	Tone 1 Level	44	0,1
25	Tone 2 Frequency	8F	2,3
26	Tone 2 Level	45	0,1
27	Checksum	02	0,1

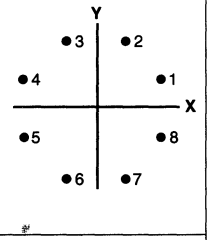
R48MFX Diagnostic Data Scaling

Node	Parameter/Scaling
1	**AGC Gain Word** (16-bit unsigned). AGC Gain in dB = 50 − [(AGC Gain Word/64) × 0.098] Range: $(16C0)_{16}$ to $(7FFF)_{16}$, For −43 dBm Threshold
2.	**Average Power** (16-bit unsigned) Post-AGC Average Power in dBm = 10 Log (Average Power Word/2185) Typical Value = $(0889)_{16}$, corresponding to 0 dBm Pre-AGC Power in dBm = (Post-AGC Average Power–AGC Gain)
3	**Receiver Sensitivity** (16-bit twos complement) On-Number = 655.36 (52.38 + P_{ON}) where: P_{ON} = Turn-on threshold in dB Convert On-Number to hexadecimal and store at access code 47
4	**Receiver Hysteresis** (16-bit twos complement) Off-Number = $[65.4\ (10^A)]^2/2$ where: A = (P_{OFF} − P_{ON} − 0.5)/20 P_{ON} = Turn-on threshold in dB P_{OFF} = Turn-off threshold in dB Convert Off-Number to hexadecimal and store at access code 84.

R48MFX Diagnostic Data Scaling (Cont'd)

Node	Parameter/Scaling
5,7–9	**All base-band signal point nodes** (i.e., Equalizer Input, Unrotated Equalizer Output, Rotated Equalizer Output, and Decision Points) are 32-bit, complex, twos complement numbers.
6	**Equalizer Tap Coefficients** (32-bit, complex, twos complement) Complex numbers with X = real part, Y = imaginary part X and Y range: 0000 to $(FFFF)_{16}$ representing ± full scale in hexadecimal twos complement.
10	**Error Vector** (32-bit, complex, twos complement) Complex number with X = real part, Y = imaginary part. X and Y range: $(8000)_{16}$ to $(7FFF)_{16}$
11	**Rotation Angle** (16-bit, signed, twos complement) Rotation Angle in deg. = (Rot. Angle Word/65,536) × 360
12	**Frequency Correction** (16-bit signed twos complement) Frequency correction in Hz = (Freq. Correction Word/65,536) × Baud Rate Range: $(FC00)_{16}$ to $(400)_{16}$ representing ± 18.75 Hz
13	**EQM** (16-bit, unsigned) Filtered squared magnitude of error vector. Proportionality to BER determined by particular application.
14–21	**Filter Tuning Parameters** (16-bit unsigned) Alpha, Beta One, Beta Two, Alpha Prime, Beta One Prime, Beta Two Prime, Alpha Double Prime, and Beta Double Prime are set according to instructions in application note 668.
22	**Output Level** (16-bit unsigned) Output Number = 27573.6 $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store at access code 43
24 and 26	**Tone 1 and Tone 2 Levels** Calculate the power of each tone independently by using the equation for Output Number given at node 22. Convert these numbers to hexadecimal then store at access codes 44 and 45. Total power transmitted in tone mode is the result of both tone 1 power and tone 2 power.
23 and 25	**Tone 1 and 2 Frequency** (16-bit unsigned) N = 6.8267 (Frequency in Hz) Convert N to hexadecimal then store at access code 8E or 8F.
27	**Checksum** (16-bit unsigned) ROM checksum number determined by revision level.

Point	Value (Hex) X	Value (Hex) Y
1	1D00	0C00
2	0C00	1D00
3	F400	1D00
4	E300	0C00
5	E300	F400
6	F400	E300
7	0C00	E300
8	1D00	F400



3

POWER-ON INITIALIZATION

When power is applied to the R48MFX, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below approximately 3 Vdc for more than 30 msec, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.27/4800 bps, serial mode, training enabled, echo protector tone enabled, interrupts disabled, RAM access code 0A, transmitter output level set for +5 dBm at TXA, receiver turn-on threshold set for –43.5 dBm, receiver turn-off threshold set for –47.0 dBm, tone 1 and tone 2 set for 0 Hz and 0 volts output, and tone detector parameters zeroed.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

Whether functioning as a V.27 ter or V.21 type modem, the R48MFX provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that illustrated in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm.

RECEIVED SIGNAL FREQUENCY TOLERANCE

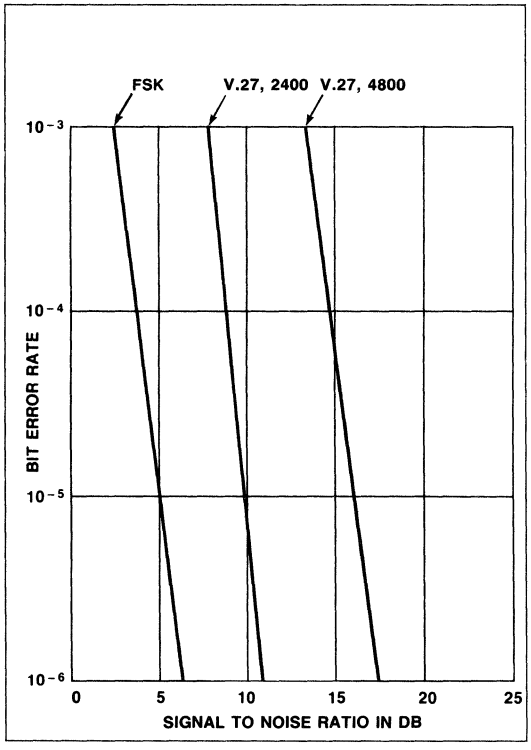
The receiver circuit of the R48MFX can adapt to received frequency error of ±10 Hz with less than 0.2 dB degradation in BER performance.

TYPICAL PHASE JITTER

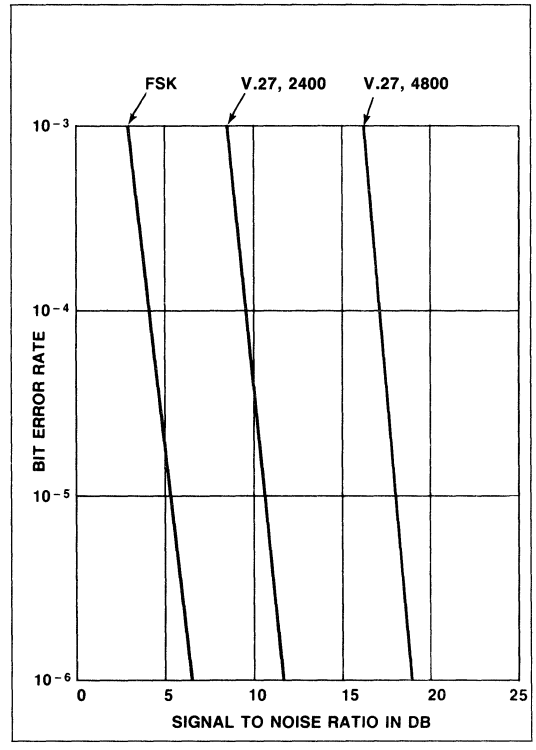
At 4800 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 2400 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

An example of the BER performance capabilities is given in the following diagrams:

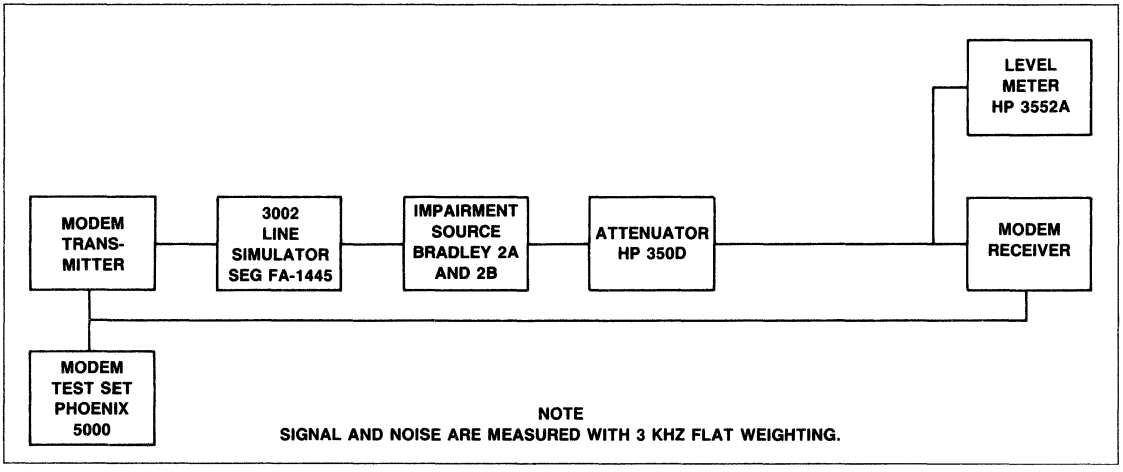


Typical Bit Error Rate (Back-to-Back, Level –20 dBm)



Typical Bit Error Rate (Unconditioned 3002 Line, Level –20 dBm)

The BER performance test set-up is show in the following diagram:



BER Performance Test Set-up

APPLICATION

Recommended Modem Interface Circuit

The R48MFX is supplied as a 64-pin QUIP device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit and parts list illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R2 and R3 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3k Ω series resistor should be used on each input (Pins 32 and 33) for isolation.

Resistors R4 and R9 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dB the 1% resistor values shown are correct for more than 99.8% of the units.

Typical Modem Interface Parts List

Component	Manufacturer's Part Number	Manufacturer
C3,C5,C7,C9	592CX7R104M050B	Sprague
C11	SA405C274MAA	AVX
Y1	333R14-002	Uniden
Z1	LM1458N	National
R5,R6	CML 1/10 T86.6K ohm ±1%	Dale Electronics
R4	5MA434.0K ±1%	Corning Electronics
R11	5043CX3R000J	Mepco Electra
R10	5043CX2M700J	Mepco Electra
R1	5043CX47K00J	Mepco Electra
R7	5043CX3K00J	Mepco Electra
R2,R3	5043CX1K00J	Mepco Electra
C10	ECEBEF100	Panasonic
C8	SMC50T1R0M5X12	United Chem-Con
C4,C6	C124C102J5G5CA	Kemet
CR1	IN751D	I.T.T.
R9	CRB¼XF47K5	R-Ohm
R8	ER025QKF2370	Matsushita Electric
R14	Determined by $\overline{IRQ}$ characteristics	

PC Board Layout Considerations

1. The R48MFX and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board (PCB).
2. All power traces should be at least 0.1 inch width.
3. If power source is located more than approximately 5 inches from the R48MFX, a decoupling capacitor of 10 microfarad or greater should be placed in parallel with C11 near pins 11 and 48.
4. All circuitry connected to pins 9 and 10 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the R48MFX package. Pin 24 should tie directly, by a unique path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and all analog ground points shown in the recommended circuit diagram.
7. Pins 4, 8, 29, and 48 should tie together at the R48MFX package. Pin 48 should tie directly, by a unique path, to the common ground point for analog and digital ground.
8. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 48 and all digital ground points shown in the recommended circuit diagram plus the crystal-can ground.
9. The R48MFX package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
10. As a general rule, digital signals should be routed on the component side of the PCB while analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
11. Routing of R48MFX signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to the table of noise characteristics for a list of pins in each category.

Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	Low	High
1	6	3	26	23
2	7	4	28	27
5	9	8	32	35
14	10	11	33	36
15	12	16		37
20	13	22		
21	17	24		
30	18	25		
38	19	29		
39	45	31		
40	46	34		
41	49	42		
44	50	43		
	51	47		
	52	48		
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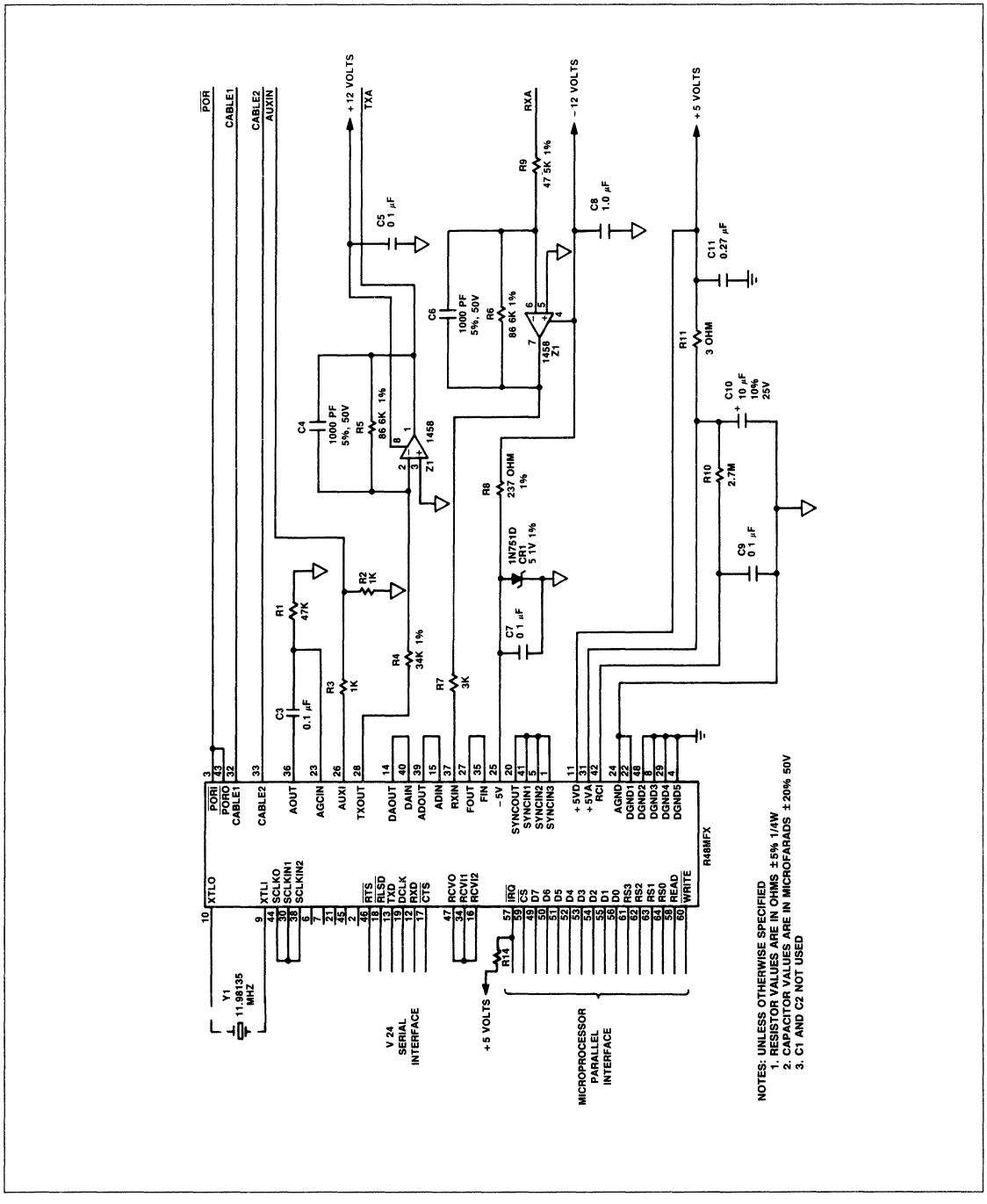
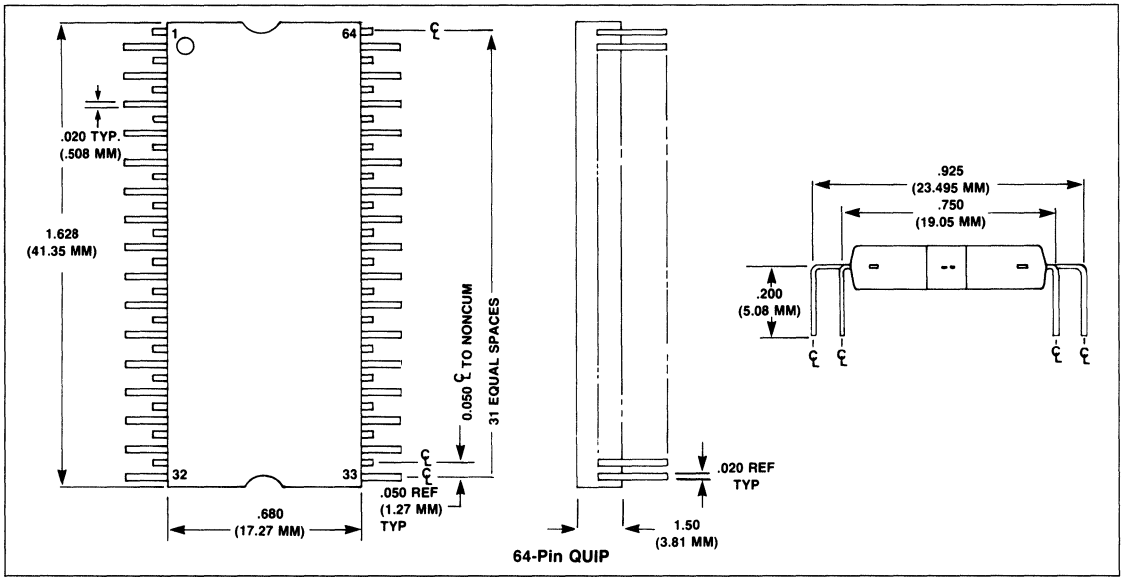


Recommended Modem Interface Circuit

PACKAGE DIMENSIONS



64-Pin QUIP

Rockwell

R48PCJ
4800 bps PC Communication Modem

INTRODUCTION

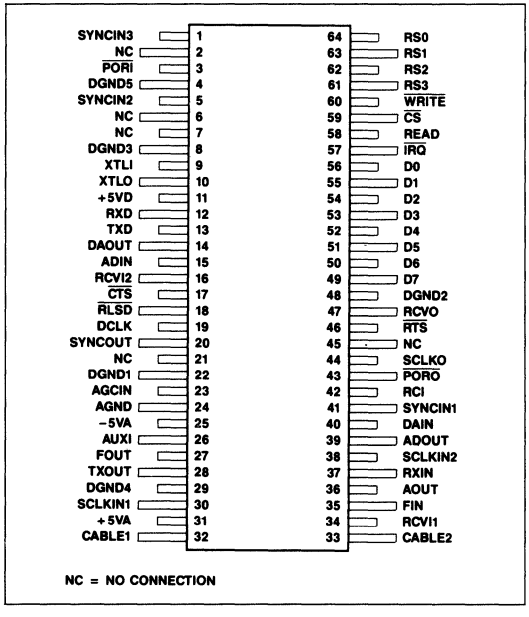
The Rockwell R48PCJ is a synchronous 4800 bits per second (bps) modem in a single 64-pin quad in-line package (QUIP). It is designed for operation over the public switched telephone network through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.27 ter, T.4 and the binary signaling capabilities of T.30. The R48PCJ can operate at speeds of 4800, 2400 and 300 bps, and includes the V.27 ter short training sequence option. Employing advanced signal processing techniques, the R48PCJ can transmit and receive data even under extremely poor line conditions.

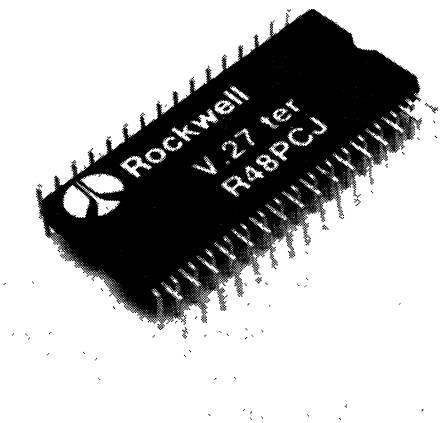
User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The R48PCJ is optimized for incorporation into an original equipment manufacturer (OEM) developed system. The modem's single device package, low power consumption, and serial/parallel host interface simplify system design and allow direct installation on the host module.

FEATURES

- Single 64-Pin QUIP
- CCITT V.27 ter, T.30, V.21 Channel 2, T.4
- Group 3 Facsimile Transmission/Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation
- Programmable Tone Detection
- Dynamic Range: – 43 dBm to 0 dBm
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R48PCJ Pin Assignments



R48PCJ 4800 bps Modem

TECHNICAL CHARACTERISTICS

TONE GENERATION

Under control of the host processor, the R48PCJ can generate single or dual frequency voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. The transmit level and frequency of each tone is independently programmable.

TONE DETECTION

Single frequency tones are detected by a programmable filter. The presence of energy at the selected frequency is indicated by a bit in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Configuration	Parameter	Specification (±0.01%)
V.27	Signaling Rate	1600 Baud
	Data Rate	4800 bps
	Signaling Rate	1200 Baud
	Data Rate	2400 bps
V.21	Signaling Rate	300 Baud
	Data Rate	300 bps

DATA ENCODING

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

At 300 baud, the data stream is 300 bps FSK per CCITT V.21 channel 2.

COMPROMISE CABLE EQUALIZERS

In addition to the adaptive equalizer, the R48PCJ provides selectable compromise cable equalizers to optimize performance over three different lengths of non-loaded cable of 0.4 mm diameter (1.8 km, 3.6 km, and 7.2 km).

Cable Equalizer Nominal Gain

Frequency (Hz)	Gain (dB) Relative to 1700 Hz		
	1.8 km	3.6 km	7.2 km
700	−0.99	−2.39	−3.93
1500	−0.20	−0.65	−1.22
2000	+0.15	+0.87	+1.90
3000	+1.43	+3.06	+4.58

TRANSMITTED DATA SPECTRUM

When operating at 1600 baud, the transmitter spectrum is shaped by a square root of 50% raised cosine filter.

When operating at 1200 baud, the transmitter spectrum is shaped by a square root of 90% raised cosine filter.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically meet the requirements of foreign telephone regulatory agencies.

SCRAMBLER/DESCRAMBLER

The R48PCJ incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with CCITT V.27 ter. The scrambler can be disabled by setting a bit in interface memory.

RECEIVE LEVEL

The receiver circuit of the R48PCJ satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. An external input buffer and filter must be supplied between the receiver analog input (RXA) and the R48PCJ RXIN pin. The received line signal level is measured at RXA.

RECEIVE TIMING

In the receive state, the R48PCJ provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the centers of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is programmable. An external output buffer and filter must be supplied between the R48PCJ TXOUT pin and the transmitter analog output (TXA). The default level at TXA is +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R48PCJ provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency:* Selected data rate of 4800, 2400 or 300 Hz (±0.01%).
2. *Duty Cycle:* 50% ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

Eleven turn-on sequences are generated by the R48PCJ, as defined in the following table:

Turn-On Sequences

No.	Bit Rate (bps)	$\overline{RTS}$ On-$\overline{CTS}$ On Time[1] (ms)	Comments
1	300	<14	No Training Sequence, No Echo Tone
2	2400	66	Short Train, No Echo Tone
3	2400	271	Short Train, with Echo Tone[2]
4	2400	943	Long Train, No Echo Tone
5	2400	1148	Long Train, with Echo Tone[2]
6	2400	<10	Training Disabled
7	4800	50	Short Train, No Echo Tone
8	4800	255	Short Train, with Echo Tone[2]
9	4800	708	Long Train, No Echo Tone
10	4800	913	Long Train, with Echo Tone[2]
11	4800	<10	Training Disabled

Notes:

1. Assumes the receiver is in idle; if not, add receiver turn-off time.
2. For use on lines with protection against talker echo.

TURN-OFF SEQUENCE

Five turn-off sequences are generated by the R48PCJ:

Turn-Off Sequences

No.	Bit Rate (bps)	RTS Off-Energy Off Time (ms)	Silence Time (ms)
1	300	<7	0
2	2400 serial	7.5	20
3	2400 parallel	7 5-10	20
4	4800 serial	5 4	20
5	4800 parallel	5.4-6.7	20

CLAMPING

The following clamps are provided with the R48PCJ:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever RLSD is off.
2. *Received Line Signal Detector (RLSD).* RLSD is clamped off (squelched) whenever RTS is on.

RESPONSE TIMES OF CLEAR-TO-SEND (CTS)

The time between the off-to-on transition of RTS and the off-to-on transition of CTS is dictated by the bit rate, the length of the training sequence, and the presence of the echo tone. The Turn-On Sequences table on page 2 lists the CTS response times.

The time between the on-to-off transition of RTS and the on-to-off transition of CTS in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR (RLSD)

RLSD turns on at the end of the training sequence. If training is not detected at the receiver, the RLSD off-to-on response time is 801 bauds (V.27 long train), 481 bauds (V.27 short train), or <10 ms (300 bps). The RLSD on-to-off response time is 10 ±5 ms. Response times are measured with a signal at least 3 dB above the actual RLSD on threshold or at least 5 dB below the actual RLSD off threshold.

The RLSD on-to-off response time ensures that all valid data bits have appeared on RXD.

Receiver threshold is programmable over the range 0 dBm to −50 dBm, however, performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to RXA.

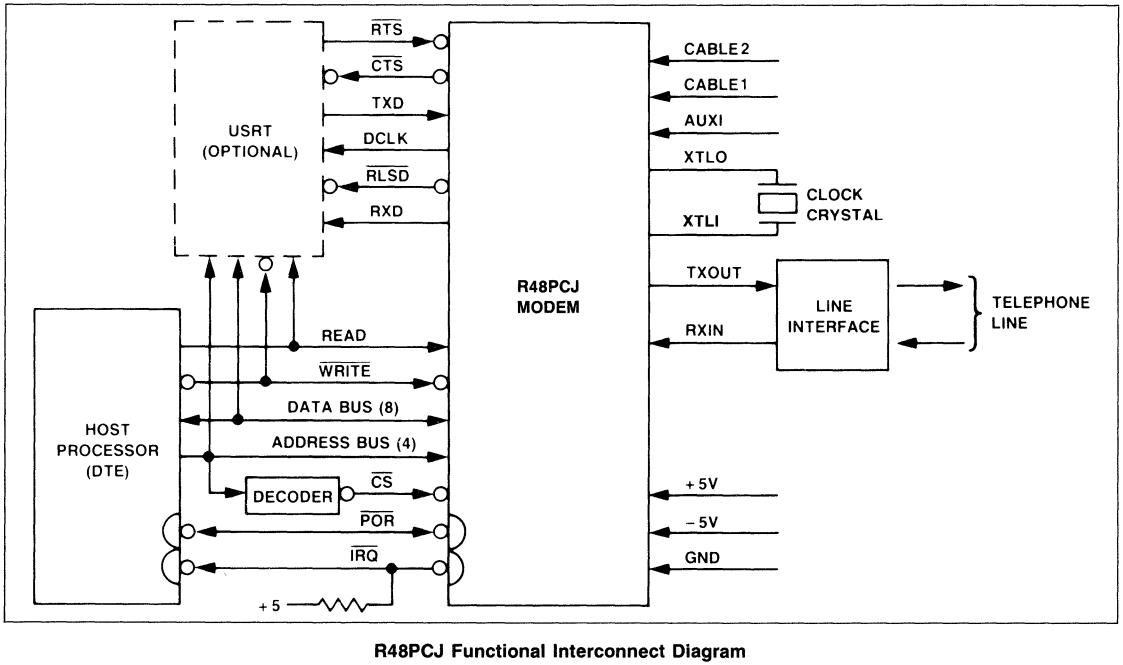
POWER

Voltage	Tolerance	Current (Max) @ 25°C	Current (Max) @ 60°C
+5 Vdc	±5%	270 mA @ 5.0 Vdc	245 mA @ 5.0 Vdc
−5 Vdc	±5%	25 mA @ −5.0 Vdc	25 mA @ −5.0 Vdc

Note: All voltages must have ripple ≤0.1 volts peak-to-peak. If a switching supply is chosen, user may select any frequency between 20 kHz and 150 kHz so long as no component of the switching frequency is present outside of the power supply with an amplitude greater than 500 microvolts peak.

ENVIRONMENTAL

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−55°C to +150°C (−67°F to +302°F) (Stored in suitable antistatic container).
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less



R48PCJ Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins on the 64-pin QUIP. Software circuits are assigned to specific bits in a 16-byte interface memory.

• HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R48PCJ Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital and Analog Interface Characteristics tables.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0-RS3), data (D0-D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

R48PCJ Hardware Circuits

Name	Type	Pin No.	Description
A. POWER:			
AGND	GND	24	Connect to Analog Ground
DGND1	GND	22	Connect to AGND Ground
DGND2	GND	48	Connect to Digital Ground
DGND3	GND	8	Connect to Digital Ground
DGND4	GND	29	Connect to Digital Ground
DGND5	GND	4	Connect to Digital Ground
+5 VA	PWR	31	Connect to Analog +5V Power
+5 VD	PWR	11	Connect to Digital +5V Power
−5 VA	PWR	25	Connect to Analog −5V Power
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	49	Data Bus (8 Bits)
D6	I/OA	50	
D5	I/OA	51	
D4	I/OA	52	
D3	I/OA	53	
D2	I/OA	54	
D1	I/OA	55	
D0	I/OA	56	
RS3	IA	61	Register Select (4 Bits) Select Reg. 0−F
RS2	IA	62	
RS1	IA	63	
RS0	IA	64	
$\overline{CS}$	IA	59	Chip Select
$\overline{READ}$	IA	58	Read Strobe
$\overline{WRITE}$	IA	60	Write Strobe
$\overline{IRQ}$	OB	57	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	19	Data Clock
$\overline{RTS}$	IB	46	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	13	Transmitter Data Signal
RXD	OC	12	Receiver Data Signal
$\overline{RLSD}$	OC	18	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABLE1	IC	32	Cable Select 1
CABLE2	IC	33	Cable Select 2

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXOUT	AA	28	Connect to Output Op Amp
RXIN	AB	37	Connect to Input Op Amp
AUXI	AC	26	Auxiliary Analog Input
F. OVERHEAD			
$\overline{PORO}$	I/OB	43	Power-On-Reset Output
$\overline{PORI}$	I/OB	3	Power-On-Reset Input
XTLO	R*	10	Connect to Crystal Circuit
XTLI	R*	9	Connect to Crystal Circuit
RCVO	R*	47	Receive Mode Output
RCVI1	R*	34	Connect to RCVO
RCVI2	R*	16	Connect to RCVO
SCLKO	R*	44	Switched Capacitor Clock Output
SCLKIN1	R*	30	Connect to SCLKO
SCLKIN2	R*	38	Connect to SCLKO
AOUT	R*	36	Smoothing Filter Output
AGCIN	R*	23	AGC Input
DAOUT	R*	14	DAC/AGC Data Out
DAIN	R*	40	Connect to DAOUT
ADOUT	R*	39	ADC Output
ADIN	R*	15	Connect to ADOUT
FOUT	R*	27	Smoothing Filter Output
FIN	R*	35	Connect to FOUT
SYNCOUT	R*	20	Sample Clock Output
SYNCIN1	R*	41	Connect to SYNCOUT
SYNCIN2	R*	5	Connect to SYNCOUT
SYNCIN3	R*	1	Connect to SYNCOUT
RCI	R*	42	RC Junction for POR Time Constant
G. RESERVED			
	R*	2	Do Not Connect
	R*	6	Do Not Connect
	R*	7	Do Not Connect
	R*	21	Do Not Connect
	R*	45	Do Not Connect

*R = Required overhead connection; no connection to host equipment

Digital Interface Characteristics

Symbol	Parameter	Units	Type: Input IA	Input IB	Input IC	Output OA	Output OB	Output OC	Input/Output I/OA	Input/Output I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0 4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max.						±12.5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

Analog Interface Characteristics

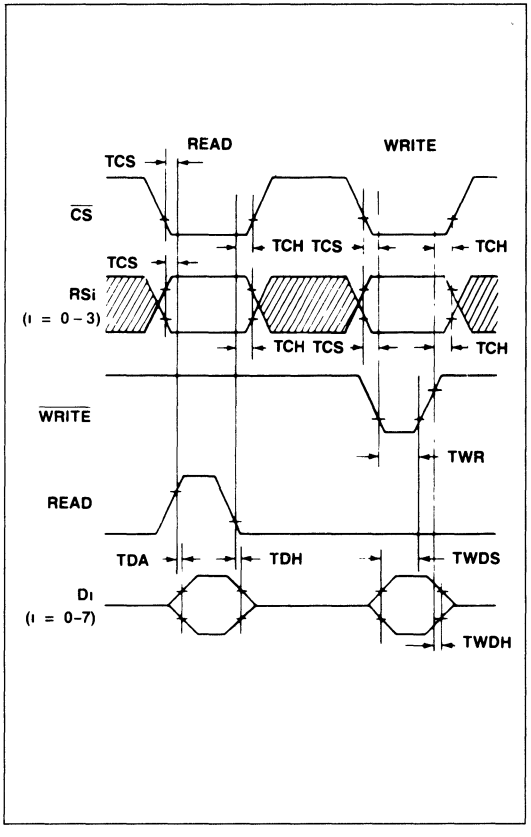
Analog Interface Characteristics

Name	Type	Characteristics
TXOUT	AA	The transmitter output can supply a maximum of ±3.03 volts into a load resistance of 10k Ω minimum. In order to match to 600 Ω, an external smoothing filter with a transfer function of 15726.43/(S + 11542.44) and 604 Ω series resistor are required.
RXIN	AB	The receiver input impedance is greater than 1M Ω. An external antialiasing filter with a transfer function of 19533.88/(S + 11542.44) is required.
AUXI	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1M Ω, and the gain to transmitter output (TXA) is +5.6 dB ±1 dB.

Note: Absolute maximum voltage ratings for analog inputs are: (−5 VA − 0.3) ≤ V_{IN} ≤ (+5 VA + 0.3)

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to READ or $\overline{WRITE}$	TCS	30	—	ns
Data Access time after READ	TDA	—	140	ns
Data hold time after READ	TDH	10	50	ns
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
$\overline{WRITE}$ strobe pulse width	TWR	75	—	ns



Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABLE2	CABLE1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs. Signals TXOUT and RXIN require buffering and filtering to be suitable for driving and receiving the communication channel. Signal AUXI provides access to the transmitter for summing host audio signals with the modem analog output.

The filters required for anti-aliasing on the receiver input and smoothing on the transmitter output have a single pole located at 11,542 radians. Although this pole is located within the modem passband, internal filters compensate for its presence and, therefore, the pole location must not be changed. Some variation from recommended resistor and capacitor values is permitted as long as the pole is not moved, overall gain is preserved, and the device is not required to drive a load of less than 10k Ω.

Notice that when reference is made to signals TXA, RXA, and AUXIN, these signals are not electrically identical to TXOUT, RXIN, and AUXI. The schematic of the recommended modem interface circuit illustrates the differences.

Overhead

Except for the power-on-reset signal $\overline{\text{PORO}}$, the overhead signals are intended for internal use only. The various required connections are illustrated in the recommended modem interface circuit schematic. No host connections should be made to overhead signals other than $\overline{\text{PORO}}$.

SOFTWARE CIRCUITS

The R48PCJ contains 16 memory mapped registers to which an external (host) microprocessor has access. The host may read data out of or write data into these registers. Refer to the R48PCJ Host Processor Interface figure.

When information in these registers is being discussed, the format Z:Q is used. The register is specified by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a one (1) and "off" when reset to a zero (0).

Status/Control Bits

The operation of the R48PCJ is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus.

All status and control bits are defined in the R48PCJ Interface Memory Map table. Bits designated by ' — ' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

Configuration Control

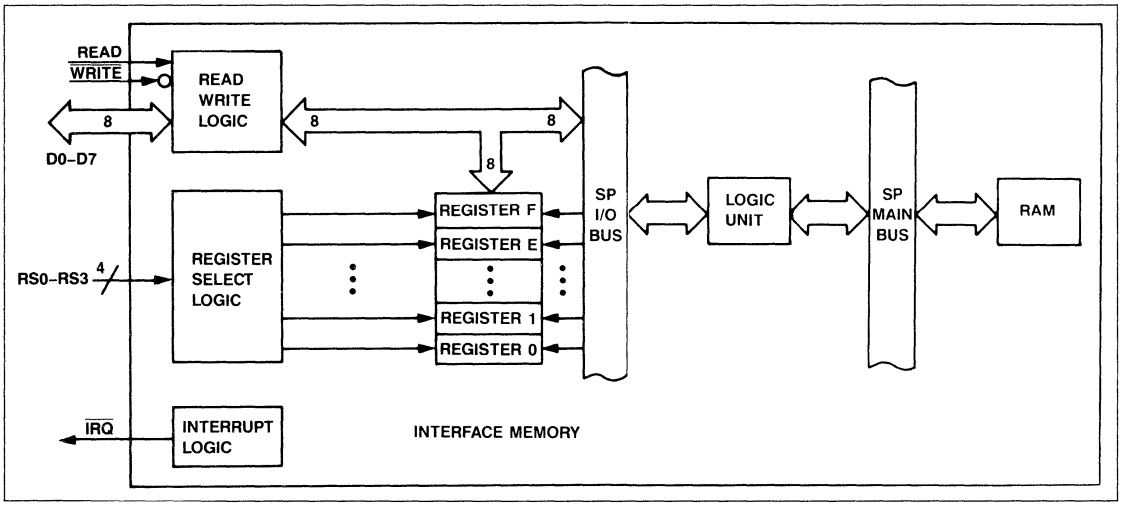
Six configurations are available in the R48PCJ modem: V.27 4800/2400 bps long/short train (four variations), V.21, and Tone. The configuration is selected by writing an 8-bit binary code into the configuration field (CONF) of the interface memory. The configuration field consists of bits 7 through 0 of register D. The code for these bits is shown in the following table. All other codes represent invalid states.

Configuration Codes

CONF Code	Configuration
00	V.21
04	V.27, 2400 Long Train
05	V.27, 2400 Short Train
06*	V.27, 4800 Long Train
07	V.27, 4800 Short Train
08	Tone Mode
* Default value at POR.	

When the modem is initialized by power-on-reset, the configuration defaults to V.27 4800 bps long train. When the host wants to change configuration, the new code is written to the configuration field and the SETUP bit (E:3) is set to a one. Once the new configuration takes effect, the SETUP bit is reset to zero by the modem.

The information in the interface memory is serviced by the modem at the baud rate (V.27 and V.21), 9600 times per second (tone generator), or 1600 times per second (tone detector).



R48PCJ Host Processor Interface

R48PCJ Interface Memory Map

Register \ Bit	7	6	5	4	3	2	1	0
F	RAMA							
E	IA	CDIE	CDREQ	—	SETUP	DDIE	—	DDREQ
D	CONF							
C	RTSP	EPT	TPDM	TDIS	EQSV	EQFZ	SDIS	RAMW
B	RX	FED		GHIT	—	—	—	—
A	TDET	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	CDET	—	PN	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RXCD							
4	TXCD							
3	DDXM							
2	DDXL							
1	DDYM							
0	DDYL							
Register \ Bit	7	6	5	4	3	2	1	0

Channel Data Transfer

Data sent to or received from the data channel may be transferred between the modem and host processor in either serial or parallel form. The receiver operates in both serial and parallel mode simultaneously and requires no mode control bit selection. The transmitter operates in either serial or parallel mode as selected by mode control bit C:5 (TPDM).

To enable the transmitter parallel mode, TPDM must be set to a 1. The modem automatically defaults to the serial mode (TPDM = 0) at power-on. In either transmitter serial or parallel mode, the R48PCJ is configured by the host processor via the microprocessor bus.

Serial Mode—The serial mode uses a standard V.24 (RS-232-C) hardware interface (optional USRT) to transfer channel data. Transmitter data can be sent serially only when TPDM is set to a zero.

Parallel Mode—Parallel data is transferred via two registers in the interface memory. Register 5 (RXCD) is used for receiver channel data, and Register 4 (TXCD) is used for transmitter channel data. Register 5 is continuously written every eight bit times when in the receive state. Register 4 is used as the source of channel transmitter data only when bit C:5 (TPDM) is set to a one by the host. Otherwise the transmitter reads data from the V.24 interface. Both $\overline{\text{RTS}}$ and RTSP remain enabled, however, regardless of the state of TPDM.

When performing parallel data transfer of channel data, the host and modem can synchronize their operations by handshaking bits in register E. Bit E:5 (CDREQ) is the channel data request bit. This bit is set to a one by the modem when receiver data is available in RXCD or when transmitter data is required in TXCD. Once the host has finished reading RXCD or writing TXCD, the host processor must reset CDREQ by writing a zero to that bit location.

When set to a one by the host, Bit E:6 (CDIE) enables the CDREQ bit to cause an $\overline{\text{IRQ}}$ interrupt when set. While the $\overline{\text{IRQ}}$ line is driven to a TTL low level by the modem, bit E:7 (IA) is a one.

If the host does not respond to the channel data request within eight bit times, the RXCD register is over written or the TXCD register is sent again.

Refer to Channel Data Parallel Mode Control flow chart for recommended software sequence.

R48PCJ Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
CDET	Carrier Detector	8:5	The one state of CDET indicates passband energy is being detected, and a training sequence is not present. CDET goes to one at the start of the data state, and returns to zero at the end of the received signal. CDET activates one baud time before $\overline{\text{RLSD}}$ and deactivates one baud time after $\overline{\text{RLSD}}$.
CDIE	Channel Data Interrupt Enable	E:6	When set to a one, CDIE enables an $\overline{\text{IRQ}}$ interrupt to be generated when the channel data request bit (CDREQ) is a one.
CDREQ	Channel Data Request	E:5	Parallel data mode handshaking bit. Set to a one when the modem receiver writes data to RXCD, or the modem transmitter reads data from TXCD. CDREQ must be reset to zero by the host processor when data service is complete.
CONF	Configuration	D:0-7	The 8-bit field CONF controls the configuration of the modem according to the following table: **Hex Code** — **Configuration** 00 — V.21 04 — V.27, 2400 Long Train 05 — V.27, 2400 Short Train 06 — V.27, 4800 Long Train (Default) 07 — V.27, 4800 Short Train 08 — Tone All else — Invalid **Configuration Definitions** *V.21*—The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 Channel 2 modulation system. *Tone*—The modem sends single or dual frequency tones in response to the $\overline{\text{RTS}}$ or RTSP signals. Tone frequencies and amplitudes are controlled by RAM locations written by the host. When not transmitting tones the Tone configuration allows detection of single frequency tones by the TDET bit. The tone detector frequency can be changed by the host by altering the contents of several RAM locations. *V.27*—The modem is compatible with CCITT Recommendation V.27 ter.
DDIE	Diagnostic Data Interrupt Enable	E:2	When set to a one, DDIE enables an IRQ interrupt to be generated when the diagnostic data request bit (DDREQ) is a one.
DDREQ	Diagnostic Data Request	E:0	DDREQ goes to a one when the modem reads from or writes to DDYL. DDREQ goes to a zero when the host processor reads from or writes to DDYL. Used for diagnostic data handshaking bit.
DDXL	Diagnostic Data X Least	2:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDXM	Diagnostic Data X Most	3:0-7	Least significant byte of 16-bit word used in reading XRAM locations.
DDYL	Diagnostic Data Y Least	0:0-7	Least significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
DDYM	Diagnostic Data Y Most	1:0-7	Most significant byte of 16-bit word used in reading YRAM locations or writing XRAM and YRAM locations.
EPT	Echo Protector Tone	C:6	When EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. EPT is not active if TDIS is on.
EQFZ	Equalizer Freeze	C:2	When EQFZ is a one, the adaptive equalizer taps stop updating and remain frozen.
EQSV	Equalizer Save	C:3	When EQSV is a one, the adaptive equalizer taps are not zeroed when reconfiguring the modem or when entering the training state. Adaptive equalizer taps are also not updated during training.
FED	Fast Energy Detector	B:5,6	FED consists of a 2-bit field that indicates the level of received signal according to the following code. **Code** — **Energy Level** 0 — None 1 — Invalid 2 — Above Turn-off Threshold 3 — Above Turn-on Threshold While receiving a signal, FED normally alternates between Codes 2 and 3.

R48PCJ Interace Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
GHIT	Gain Hit	B:4	The gain hit bit goes to one when the receiver detects a sudden increase in passband energy faster than the AGC circuit can correct GHIT returns to zero when the AGC output returns to normal
IA	Interrupt Active	E 7	IA is a one when the modem is driving the interrupt request line ($\overline{IRQ}$) to a low TTL level.
PN	Period N	8:3	PN sets to a one at the start of the received PN sequence PN resets to zero at the start of the received scrambled ones PN does not operate when TDIS is set to a one.
RAMA	RAM Access	F:0-7	The RAMA register is written by the host when reading or writing diagnostic data The RAMA code determines the RAM location with which the diagnostic read or write is performed.
RAMW	RAM Write	C:0	RAMW is set to a one by the host processor when performing diagnostic writes to the modem RAM. RAMW is set to a zero by the host when reading RAM diagnostic data.
RTSP	Request to Send Parallel	C:7	The one state of RTSP begins a transmit sequence. The modem continues to transmit until RTSP is turned off and the turn-off sequence has been completed. RTSP parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are ORed by the modem.
RXCD	Receiver Channel Data	5:0-7	RXCD is written to by the modem every eight bit times. This byte of channel data can be read by the host when the receiver sets the channel data request bit (CDREQ)
RX	Receive State	B:7	RX is a one when the modem is in the receive state (i.e., not transmitting).
SDIS	Scrambler Disable	C:1	When SDIS is a one, the scrambler/descrambler is disabled When SDIS is a zero, the scrambler/descrambler is enabled (default).
SETUP	Setup	E:3	The host processor must set the SETUP bit to a one when reconfiguring the modem, i.e., when changing CONF (D:0-7).
TDET	Tone Detected	A:7	The one state of TDET indicates reception of a tone. The filter can be retuned by means of the diagnostic write routine.
TDIS	Training Disable	C:4	If TDIS is a one in the receive state, the modem is prevented from entering the training phase If TDIS is a one when $\overline{RTS}$ or RTSP go active, the generation of a training sequence is prevented at the start of transmission.
TPDM	Transmitter Parallel Data Mode	C:5	When control bit TPDM is a one, the transmitter accepts data for transmission from the TXCD register rather than the serial hardware data input.
TXCD	Transmitter Channel Data	4:0-7	The host processor conveys output data to the transmitter in parallel data mode by writing a data byte to the TXCD register when the channel data request bit (CDREQ) goes to a one. Data is transmitted as single bits in V.21 or as dibits in V.27 starting with bit 0 or dibit 0,1

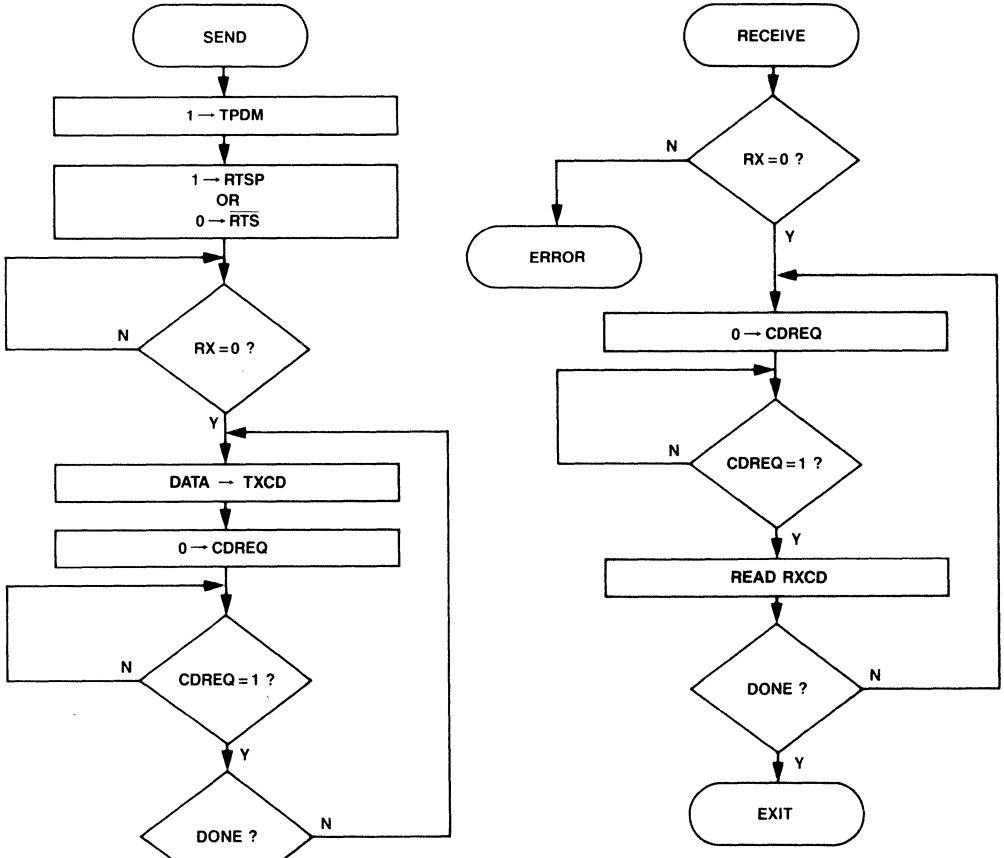
Diagnostic Data Transfer

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register F (RAMA). The R48PCJ RAM Access Codes table lists 27 access codes for storage in register F and the corresponding diagnostic functions. The R48PCJ Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long. These bits are written into interface memory registers 3, 2, 1 and 0 in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit C:0 (RAMW) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the more significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAMA bits of register F. When bit F:7 is set to one, the XRAM is selected. When F:7 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the diagnostic data request bit E:0 (DDREQ) is reset to zero. When the modem reads or writes register 0, DDREQ is set to a one. When set to a one by the host, bit E:2 (DDIE) enables the DDREQ bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit E:7 (IA) goes to a one.



Channel Data Parallel Mode Control

R48PCJ RAM Access Codes

Node	Function	RAMA	Reg. No.
1	AGC Gain Word	87	2,3
2	Average Power	91	2,3
3	Receiver Sensitivity	47	0,1
4	Receiver Hysteresis	84	2,3
5	Equalizer Input	63	0,1,2,3
6	Equalizer Tap Coefficients	23-32	0,1,2,3
7	Unrotated Equalizer Output	73	0,1,2,3
8	Rotated Equalizer Output	0A	0,1,2,3
9	Decision Points	74	0,1,2,3
10	Error Vector	75	0,1,2,3
11	Rotation Angle	B3	2,3
12	Frequency Correction	8B	2,3
13	EQM	89	2,3
14	Alpha (α)	38	0,1
15	Beta One (β_1)	39	0,1
16	Beta Two (β_2)	3A	0,1
17	Alpha Prime (α')	3B	0,1
18	Beta One Prime (β_1')	3C	0,1
19	Beta Two Prime (β_2')	3D	0,1
20	Alpha Double Prime (α'')	B8	2,3
21	Beta Double Prime (β'')	B9	2,3
22	Output Level	43	0,1
23	Tone 1 Frequency	8E	2,3
24	Tone 1 Level	44	0,1
25	Tone 2 Frequency	8F	2,3
26	Tone 2 Level	45	0,1
27	Checksum	02	0,1

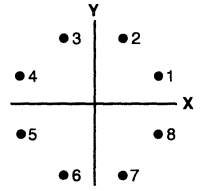
R48PCJ Diagnostic Data Scaling

Node	Parameter/Scaling
1	**AGC Gain Word** (16-bit unsigned). AGC Gain in dB = 50 – [(AGC Gain Word/64) × 0.098] Range: $(16C0)_{16}$ to $(7FFF)_{16}$, For –43 dBm Threshold
2.	**Average Power** (16-bit unsigned) Post-AGC Average Power in dBm = 10 Log (Average Power Word/2185) Typical Value = $(0889)_{16}$, corresponding to 0 dBm Pre-AGC Power in dBm = (Post-AGC Average Power–AGC Gain)
3	**Receiver Sensitivity** (16-bit twos complement) On-Number = 655.36 (52.38 + P_{ON}) where: P_{ON} = Turn-on threshold in dB Convert On-Number to hexadecimal and store at access code 47
4	**Receiver Hysteresis** (16-bit twos complement) Off-Number = $[65.4\ (10^A)]^2/2$ where: A = (P_{OFF} – P_{ON} – 0.5)/20 P_{ON} = Turn-on threshold in dB P_{OFF} = Turn-off threshold in dB Convert Off-Number to hexadecimal and store at access code 84.

R48PCJ Diagnostic Data Scaling (Cont'd)

Node	Parameter/Scaling
5,7–9	**All base-band signal point nodes** (i.e., Equalizer Input, Unrotated Equalizer Output, Rotated Equalizer Output, and Decision Points) are 32-bit, complex, twos complement numbers.
6	**Equalizer Tap Coefficients** (32-bit, complex, twos complement) Complex numbers with X = real part, Y = imaginary part X and Y range: 0000 to $(FFFF)_{16}$ representing ± full scale in hexadecimal twos complement.
10	**Error Vector** (32-bit, complex, twos complement) Complex number with X = real part, Y = imaginary part. X and Y range: $(8000)_{16}$ to $(7FFF)_{16}$
11	**Rotation Angle** (16-bit, signed, twos complement) Rotation Angle in deg. = (Rot. Angle Word/65,536) × 360
12	**Frequency Correction** (16-bit signed twos complement) Frequency correction in Hz = (Freq. Correction Word/65,536) × Baud Rate Range: $(FC00)_{16}$ to $(400)_{16}$ representing ± 18.75 Hz
13	**EQM** (16-bit, unsigned) Filtered squared magnitude of error vector. Proportionality to BER determined by particular application.
14–21	**Filter Tuning Parameters** (16-bit unsigned) Alpha, Beta One, Beta Two, Alpha Prime, Beta One Prime, Beta Two Prime, Alpha Double Prime, and Beta Double Prime are set according to instructions in application note 668.
22	**Output Level** (16-bit unsigned) Output Number = 27573.6 $[10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store at access code 43
24 and 26	**Tone 1 and Tone 2 Levels** Calculate the power of each tone independently by using the equation for Output Number given at node 22. Convert these numbers to hexadecimal then store at access codes 44 and 45. Total power transmitted in tone mode is the result of both tone 1 power and tone 2 power.
23 and 25	**Tone 1 and 2 Frequency** (16-bit unsigned) N = 6.8267 (Frequency in Hz) Convert N to hexadecimal then store at access code 8E or 8F.
27	**Checksum** (16-bit unsigned) ROM checksum number determined by revision level.

Point	Value (Hex) X	Value (Hex) Y
1	1D00	0C00
2	0C00	1D00
3	F400	1D00
4	E300	0C00
5	E300	F400
6	F400	E300
7	0C00	E300
8	1D00	F400



3

POWER-ON INITIALIZATION

When power is applied to the R48PCJ, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below approximately 3 Vdc for more than 30 msec, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.27/4800 bps, serial mode, training enabled, echo protector tone enabled, interrupts disabled, RAM access code 0A, transmitter output level set for +5 dBm at TXA, receiver turn-on threshold set for –43.5 dBm, receiver turn-off threshold set for –47.0 dBm, tone 1 and tone 2 set for 0 Hz and 0 volts output, and tone detector parameters zeroed.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

Whether functioning as a V.27 ter or V.21 type modem, the R48PCJ provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that illustrated in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm.

RECEIVED SIGNAL FREQUENCY TOLERANCE

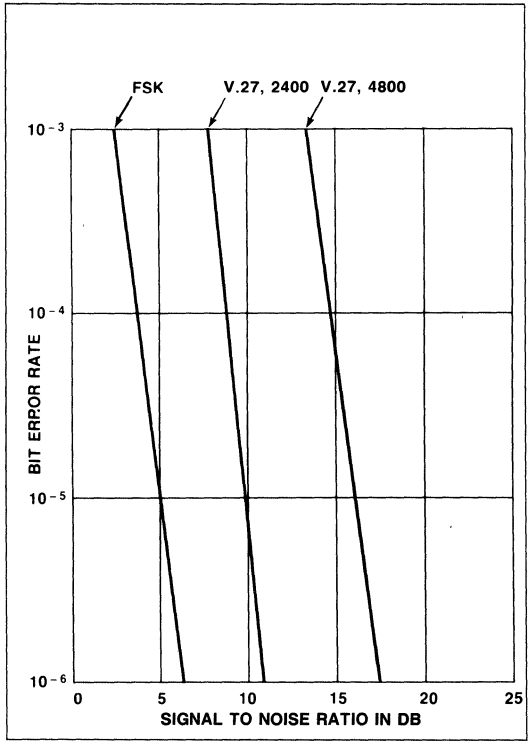
The receiver circuit of the R48PCJ can adapt to received frequency error of ±10 Hz with less than 0.2 dB degradation in BER performance.

TYPICAL PHASE JITTER

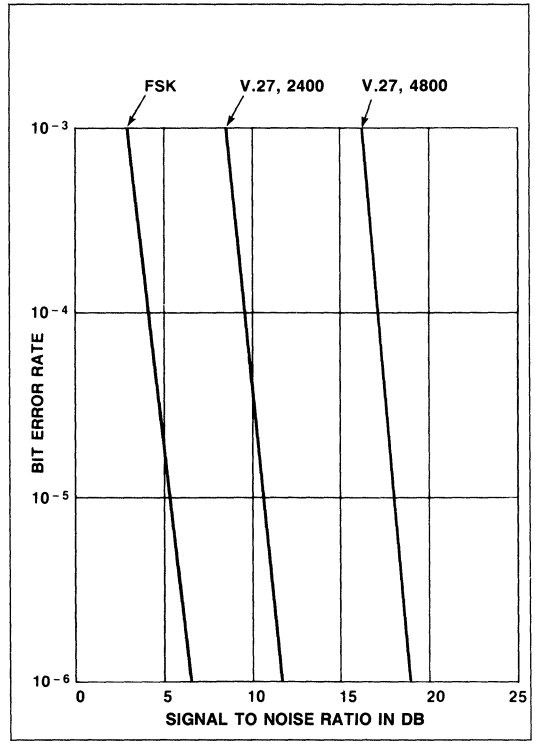
At 4800 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 2400 bps, the modem exhibits a BER of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

An example of the BER performance capabilities is given in the following diagrams:

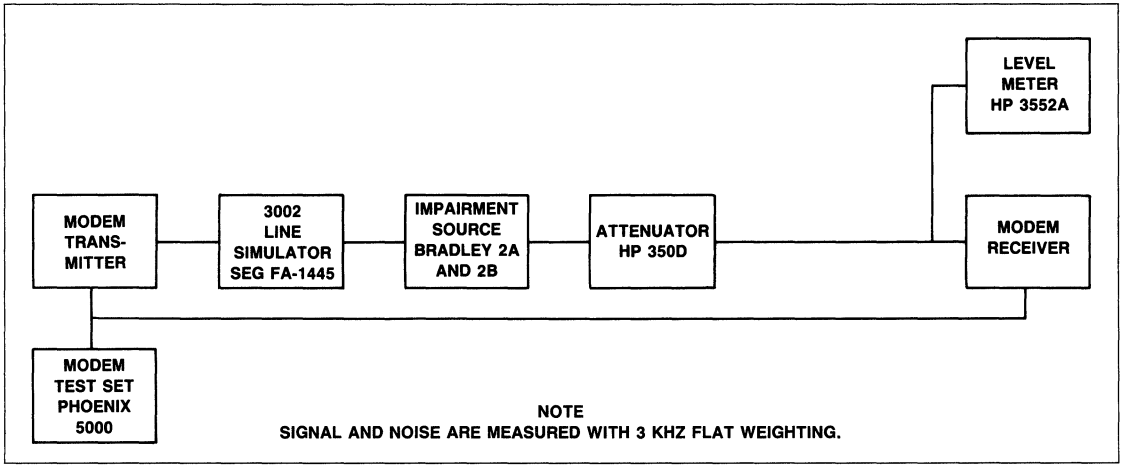


Typical Bit Error Rate (Back-to-Back, Level –20 dBm)



Typical Bit Error Rate (Unconditioned 3002 Line, Level –20 dBm)

The BER performance test set-up is show in the following diagram:



BER Performance Test Set-up

APPLICATION

Recommended Modem Interface Circuit

The R48PCJ is supplied as a 64-pin QUIP device to be designed into original equipment manufacturer (OEM) circuit boards. The recommended modem interface circuit and parts list illustrate the connections and components required to connect the modem to the OEM electronics.

If the auxiliary analog input (pin 26) is not used, resistors R2 and R3 can be eliminated and pin 26 must be connected to analog ground (pin 24). When the cable equalizer controls CABLE1 and CABLE2 are connected to long leads that are subject to picking up noise spikes, a 3k Ω series resistor should be used on each input (Pins 32 and 33) for isolation.

Resistors R4 and R9 can be used to trim the transmit level and receive threshold to the accuracy required by the OEM equipment. For a tolerance of ±1 dB the 1% resistor values shown are correct for more than 99.8% of the units.

Typical Modem Interface Parts List

Component	Manufacturer's Part Number	Manufacturer
C3,C5,C7,C9	592CX7R104M050B	Sprague
C11	SA405C274MAA	AVX
Y1	333R14-002	Uniden
Z1	LM1458N	National
R5,R6	CML 1/10 T86.6K ohm ±1%	Dale Electronics
R4	5MA434.0K ±1%	Corning Electronics
R11	5043CX3R000J	Mepco Electra
R10	5043CX2M700J	Mepco Electra
R1	5043CX47K00J	Mepco Electra
R7	5043CX3K00J	Mepco Electra
R2,R3	5043CX1K00J	Mepco Electra
C10	ECEBEF100	Panasonic
C8	SMC50T1R0M5X12	United Chem-Con
C4,C6	C124C102J5G5CA	Kemet
CR1	IN751D	I.T.T.
R9	CRB¼XF47K5	R-Ohm
R8	ER025QKF2370	Matsushita Electric
R14	Determined by $\overline{IRQ}$ characteristics	

PC Board Layout Considerations

1. The R48PCJ and all supporting analog circuitry, including the data access arrangement if required, should be located on the same area of printed circuit board (PCB).
2. All power traces should be at least 0.1 inch width.
3. If power source is located more than approximately 5 inches from the R48PCJ, a decoupling capacitor of 10 microfarad or greater should be placed in parallel with C11 near pins 11 and 48.
4. All circuitry connected to pins 9 and 10 should be kept short to prevent stray capacitance from affecting the oscillator.
5. Pin 22 should be tied directly to pin 24 at the R48PCJ package. Pin 24 should tie directly, by a unique path, to the common ground point for analog and digital ground.
6. An analog ground plane should be supplied beneath all analog components. The analog ground plane should connect to pin 24 and all analog ground points shown in the recommended circuit diagram.
7. Pins 4, 8, 29, and 48 should tie together at the R48PCJ package. Pin 48 should tie directly, by a unique path, to the common ground point for analog and digital ground.
8. A digital ground plane should be supplied to cover the remaining allocated area. The digital ground plane should connect to pin 48 and all digital ground points shown in the recommended circuit diagram plus the crystal-can ground.
9. The R48PCJ package should be oriented relative to the two ground planes so that the end containing pin 1 is toward the digital ground plane and the end containing pin 32 is toward the analog ground plane.
10. As a general rule, digital signals should be routed on the component side of the PCB while analog signals are routed on the solder side. The sides may be reversed to match a particular OEM requirement.
11. Routing of R48PCJ signals should provide maximum isolation between noise sources and sensitive inputs. When layout requirements necessitate routing these signals together, they should be separated by neutral signals. Refer to the table of noise characteristics for a list of pins in each category.

Pin Noise Characteristics

Noise Source			Noise Sensitive	
High	Low	Neutral	Low	High
1	6	3	26	23
2	7	4	28	27
5	9	8	32	35
14	10	11	33	36
15	12	16		37
20	13	22		
21	17	24		
30	18	25		
38	19	29		
39	45	31		
40	46	34		
41	49	42		
44	50	43		
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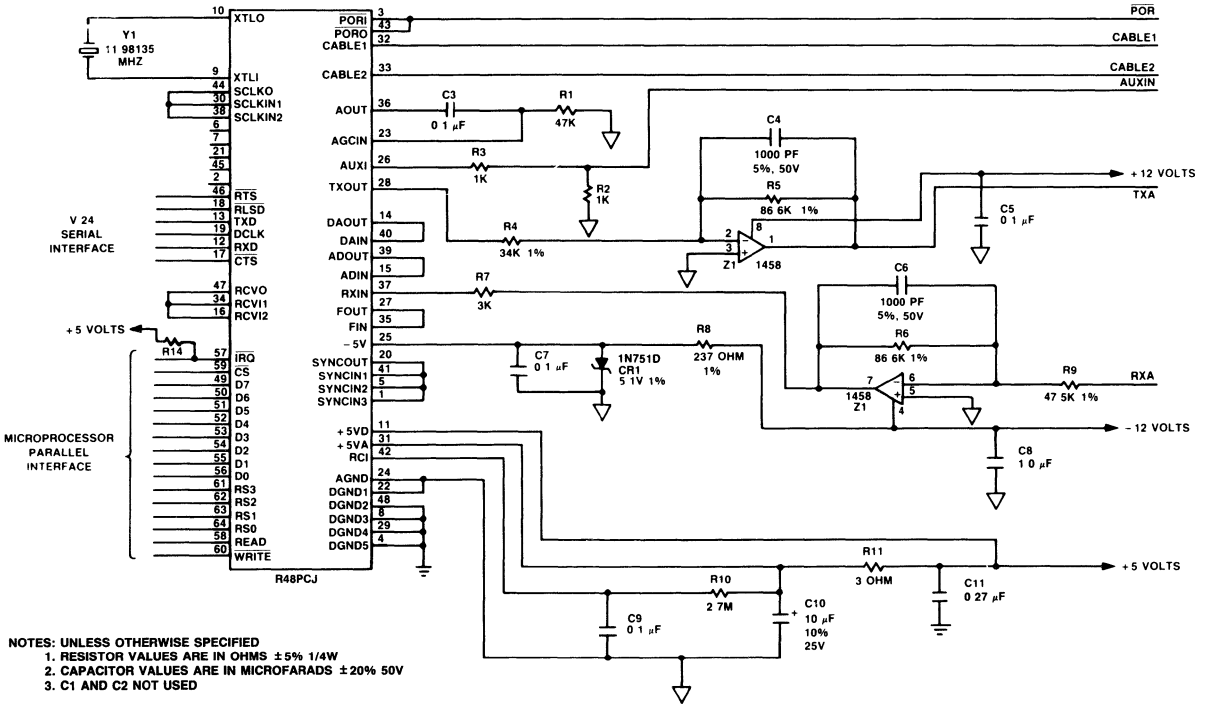
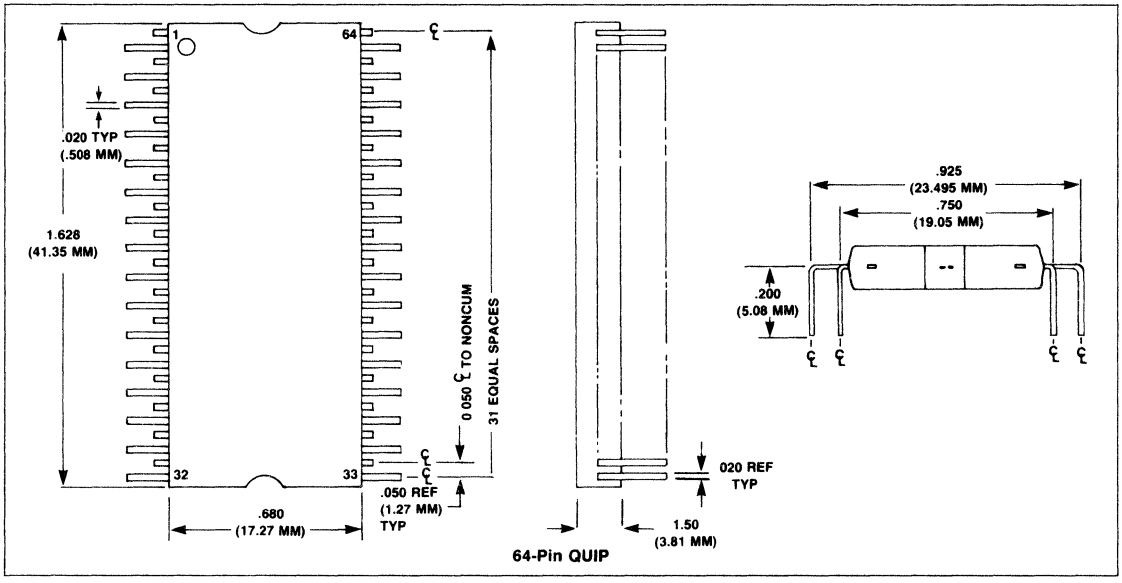


NOTES: UNLESS OTHERWISE SPECIFIED

1. **RESISTOR VALUES ARE IN OHMS ±5% 1/4W**
2. **CAPACITOR VALUES ARE IN MICROFARADS ±20% 50V**
3. **C1 AND C2 NOT USED**

Recommended Modem Interface Circuit

PACKAGE DIMENSIONS



64-Pin QUIP

Rockwell

R24/48MEB
Modem Evaluation Board

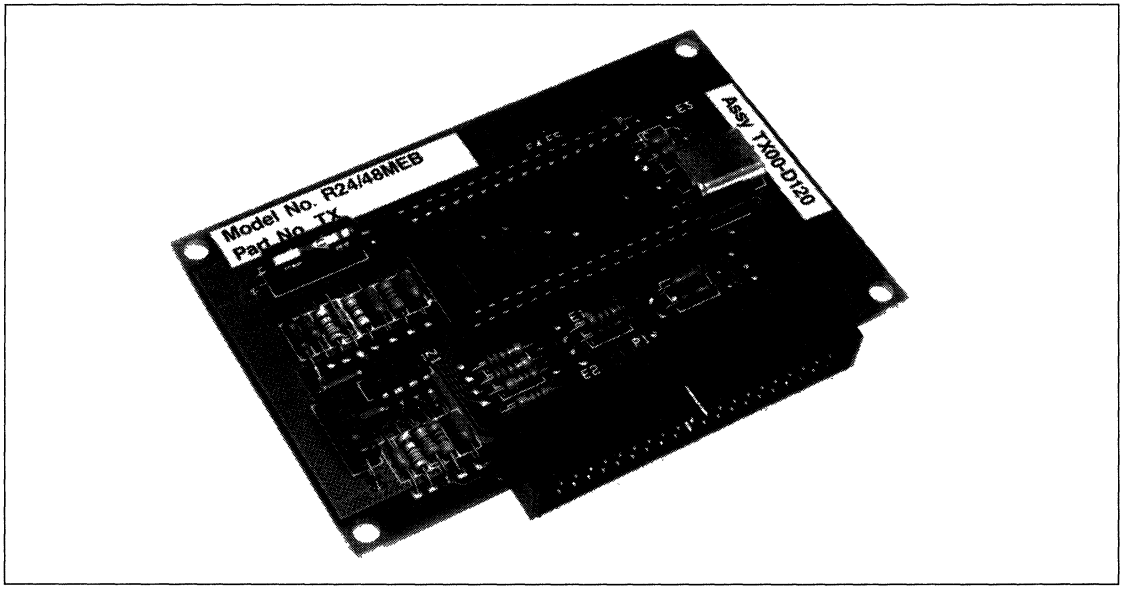
INTRODUCTION

The Rockwell R24/48MEB Modem Evaluation Board (MEB) aids the original equipment manufacturer (OEM) during the evaluation and design in phases of product development. Modems supported by the R24/48MEB include the R24MFX, R24BKJ, R48MFX, and R48PCJ. The Modem Evaluation Board contains a socket (U1) for mounting the 64-pin quad in-line package (QUIP) of the selected modem, plus support circuitry to configure a complete data pump. For operation over the public switched telephone network (PSTN), an appropriate line termination, such as a data access arrangement (DAA), must be provided externally.

The R24/48MEB physical and electrical interface is compatible with the Rockwell R96FAX modem. For users of the R96FAX, this feature provides a rapid means of preparing to evaluate a 64-pin QUIP modem. Equipment previously developed for use with the R96FAX can be converted for use with the R24/48MEB by changing only the software.

FEATURES

- Convenient evaluation method for
  - R24MFX
  - R24BKJ
  - R48MFX
  - R48PCJ
- Exercises all modem functions
- Easily integrated into a prototype system
- Cost effective for low volume production applications
- Standard 40-pin flat ribbon connector
- Backward compatible with R96FAX hardware
- Low power consumption: 1.5W (typical)
- Small size: 100 mm × 65 mm (3.94 in. × 2.56 in.).



R24/48MEB Modem Evaluation Board

TECHNICAL SPECIFICATION

For a description of the R24/48MEB characteristics with a 64-pin QUIP modem installed in socket U1, refer to the corresponding modem data sheet.

Modem Number	Data Sheet Order Number
R24MFX	MD17
R24BKJ	MD20
R48MFX	MD19
R48PCJ	MD21

CIRCUIT DESCRIPTION

INTERFACE CIRCUITS

The circuitry and design rules used to create the R24/48MEB follow the recommended modem interface and PC board layout considerations published in the associated 64-pin QUIP modem data sheet. The circuit card can be used as a guide in host PC board design.

Refer to the R24/48MEB schematic diagram (Figure 2) during the following description. The modem being evaluated is inserted in the 64-pin QUIP socket (U1). Various overhead connections between QUIP pins are completed by circuits on the evaluation board. Some of these overhead signals are connected to test points (E3, E4, E5) or connector pins (P1-11, P1-12, P1-22, P1-24) for use in Rockwell production test. These signals are not intended for use by the host equipment.

Modem signals that form the user interface on connector P1 (Table 1) are divided into five categories: Power, Microprocessor Interface, V.24 Interface, Cable Equalizer, and Analog Signals. The column titled "Type" refers to designations found in the digital and analog interface characteristics tables (Tables 2 and 3). The five categories are defined in the following paragraphs.

Power

Power signals include ± 12 volts, +5 volts, ground and $\overline{POR}$. The ± 12 volt supplies provide power for analog circuits and should be free from switching transients normally associated with digital circuits. The +5 volt source provides power for digital circuits and can be driven by the host logic supply.

The common reference point for all signals, both digital and analog, is modem ground (pins 14 and 39). These pins provide the power supply return points for all voltages and should be used as reference for transmitter and receiver signals. To minimize noise problems, circuits that interface to the modem should maintain their ground references as close as possible to the same potential as modem pins 14 and 39. Digital signals and analog signals should be referenced to modem ground via separate connections to prevent digital noise from appearing on analog signals due to a common ground impedance.

In order to reduce the effect of noise coupled through direct current (DC) power lines, decoupling capacitors are recommended on all power inputs. Each supply input should be decoupled to signal ground (pins 14 and 39) by a parallel set of capacitors. A large value capacitor of 10 microfarads or greater should be paralleled by a low inductance small value capacitor of 0.1 microfarads.

Because the modem uses switched capacitor filters, the noise floor can be degraded as the result of high frequency noise aliased into the passband by beating with the switched capacitor clock. For this reason, use of linear power supplies, rather than switching power supplies, is recommended where low level reception (i.e., around −40 dBm) is anticipated. If switching power supplies are used, extra care must be taken to keep switching noise out of the modem. The following techniques have proven helpful in designing systems using switching supplies.

1. In addition to the decoupling capacitors on all modem power inputs, the power supply output leads should be wrapped around a toroidal core to increase series inductance. This technique blocks the conducted high frequency noise from the switching supply.

Table 1. R24/48MEB Connector Interface Signals

Name	Type	Pin No.	Description
A. POWER:			
Ground	GND	14, 39	Power Supply Return
+5 volts	PWR	3, 4	+5 volt supply
+12 volts	PWR	26	+12 volt supply
−12 volts	PWR	37	−12 volt supply
$\overline{POR}$	I/OB	36	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	7	Data Bus (8 Bits)
D6	I/OA	5	
D5	I/OA	9	
D4	I/OA	31	
D3	I/OA	15	
D2	I/OA	28	
D1	I/OA	23	
D0	I/OA	29	
RS3	IA	30	Register Select (4 Bits)
RS2	IA	8	
RS1	IA	27	
RS0	IA	10	
$\overline{CS}$	IA	6	Chip Select
$\overline{READ}$	IA	1	Read Enable
$\overline{WRITE}$	IA	2	Write Enable
$\overline{IRQ}$	OB	32	Interrupt Request
C. V.24 INTERFACE:			
$\overline{DCLK}$	OC	13	Data Clock
$\overline{RTS}$	IB	19	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	20	Transmitter Data
RXD	OC	21	Receiver Data
$\overline{RLSD}$	OC	16	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IC	33	Cable Select 1
CABS2	IC	34	Cable Select 2
E. ANALOG SIGNALS:			
TXA	AA	38	Transmitter Analog Output
RXA	AB	40	Receiver Analog Input
AUXIN	AC	35	Auxiliary Analog Input

Table 2. Digital Interface Characteristics

Symbol	Parameter	Units	Type							
			Input			Output			Input/Output	
			IA	IB	IC	OA	OB	OC	I/OA	I/OB
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min	2.0 min				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min.[1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max						±12.5 max[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

Table 3. Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 47.5K ohms ±1%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above half the sample rate will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −0.4 dB ±1 dB.

2. A ground plane should be inserted between the modem and the power supply. This technique reduces radiated EMI pickup by modem circuits.

3. Shield analog signals in coaxial wire. Signals TXA (pin 38), RXA (pin 40), and AUXIN (pin 35) should be shielded. Signal AUXIN should be tied to ground (pin 39) if not used.

By following these procedures, satisfactory performance over the full dynamic range should be realized even when switching power supplies must be used.

When the modem is initially energized a signal called Power-On Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives pin 36 to ground during the beginning of the POR sequence. Approximately 10 milliseconds after the low to high transition of pin 36, the modem is ready for normal use. The POR sequence is reinitialized anytime the +5 volt supply drops below +3.0 volts for more than 30 milliseconds, or an external device drives pin 36 low for at least 3 microseconds.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0–RS3), data (D0–D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. The microprocessor interface timing waveforms are shown in Figure 1 and the microprocessor interface timing requirements are listed in Table 4. With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the referenced data sheet of each 64-pin QUIP modem.

V.24 Interface

Six hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels. These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

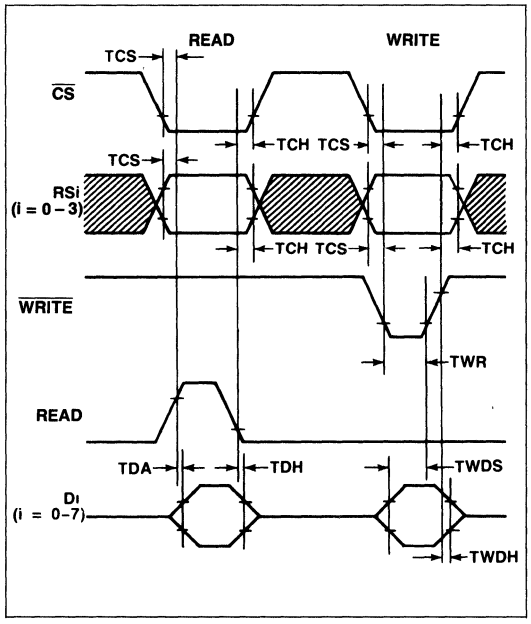


Figure 1. Microprocessor Interface Timing Waveforms

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion. The low (0) and high (1) states of signals CABS1 and CABS2 that are necessary to select each of the cable equalizer options are defined in Table 5.

Analog Signals

Three connector pins are devoted to analog audio signals: TXA, RXA, and AUXIN. The TXA (transmitter analog) line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the public switched telephone network. The output structure of TXA is a low impedance amplifier. In order to match this output to a standard telephone load of 600 ohms, a series resistor is required. A value of 604 ohms ±1% is recommended.

The RXA (receiver analog) line is an input to the receiver from an audio transformer or data access arrangement. The input impedance is 47.5K ohms ±1%. The RXA input must be shunted by an external resistor in order to match a 600 ohms source. The 604 ohms ±1% resistor recommended for the transmitter is also suitable for the receiver.

Table 4. Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$, RSi setup time prior to Read or $\overline{WRITE}$	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
$\overline{CS}$, RSi hold time after READ or $\overline{WRITE}$	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
$\overline{WRITE}$ strobe pulse width	TWR	75	—	NS

Table 5. Cable Equalizer Selection

CABLE1	CABLE2	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

The last analog connection is the input AUXIN. This line provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit. Any signal above half the sample rate on the AUXIN line will be aliased back into the passband as noise.

MEB SUPPORT CIRCUITS

The modem evaluation board with a 64-pin QUIP modem installed forms a complete data pump ready for interfacing to a host microprocessor (Figure 3). The host electronics must provide data and timing on the microprocessor interface pins to allow normal modem configuration and option selection plus status monitoring. Additional circuitry is recommended to allow generation of an eye pattern for diagnostic purposes (Figure 6). A commercially available modem test set (e.g., Phoenix 5000) can be connected directly to the V.24 serial interface (using TTL levels) or can be buffered with DS1488 and DS1489 type drivers and receivers for operation with standard RS-232 levels.

Schematic diagrams are provided for the RS-232 buffer circuit (Figure 4) and the microprocessor bus interface with eye pattern output (Figure 5). Note that the data clock signal must drive both the transmitter clock and the receiver clock and is therefore buffered to reduce the load on the R24/48MEB pin 13. Also note that an SN74121 is used to shorten the write pulse in order to meet data hold time requirements for the NE5018 devices. The 100 ohm resistors in series with modem signals are required only when driving several feet of cable where excessive ringing may require damping. The address decode logic places the modem registers between locations 9000 and 900F hexadecimal. The eye pattern DAC's are at locations 9071 and 9072.

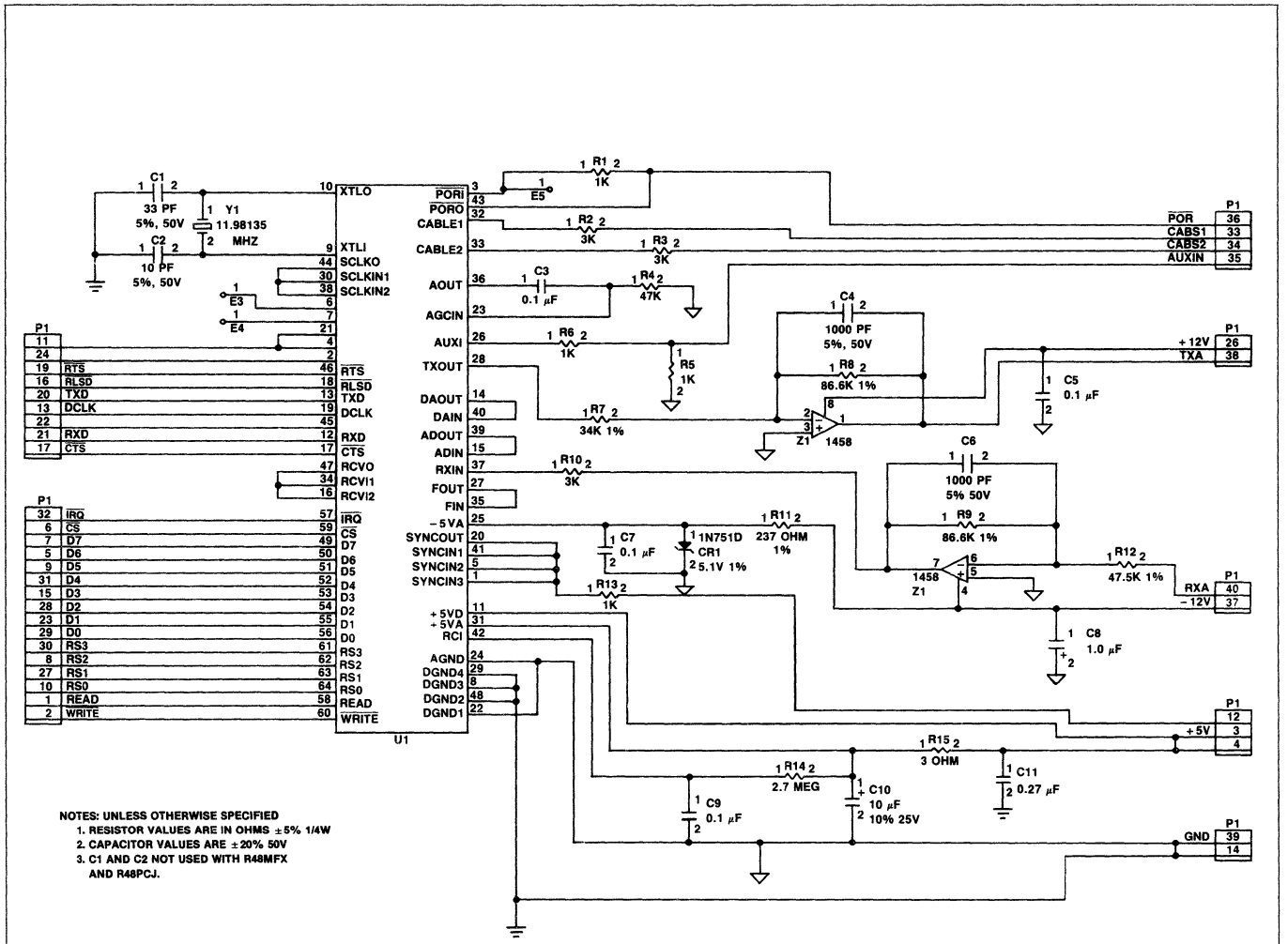


Figure 2. R24/48MEB Schematic Diagram

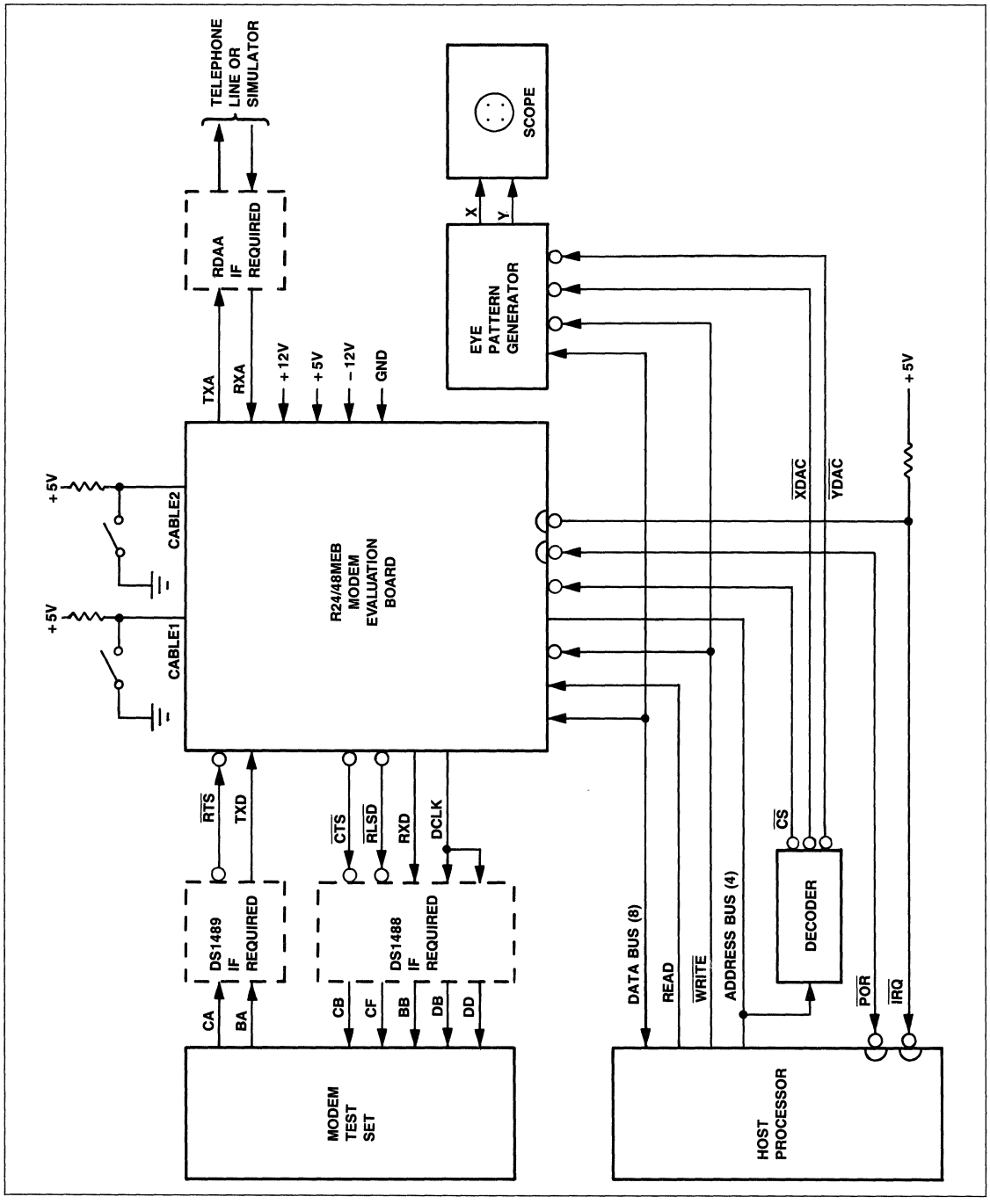


Figure 3. R24/48MEB Functional Interconnect Diagram

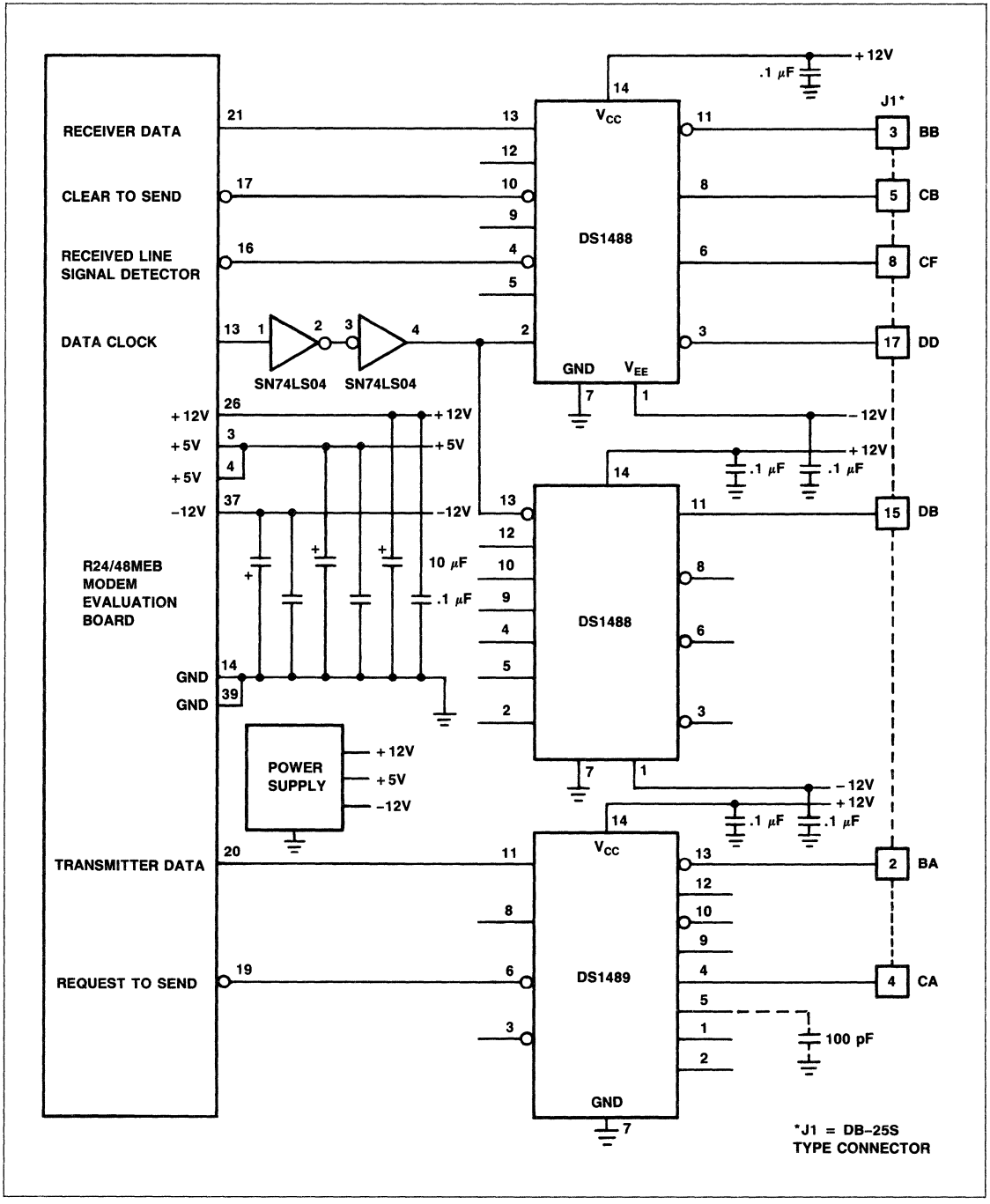


Figure 4. RS-232 Buffer Circuit

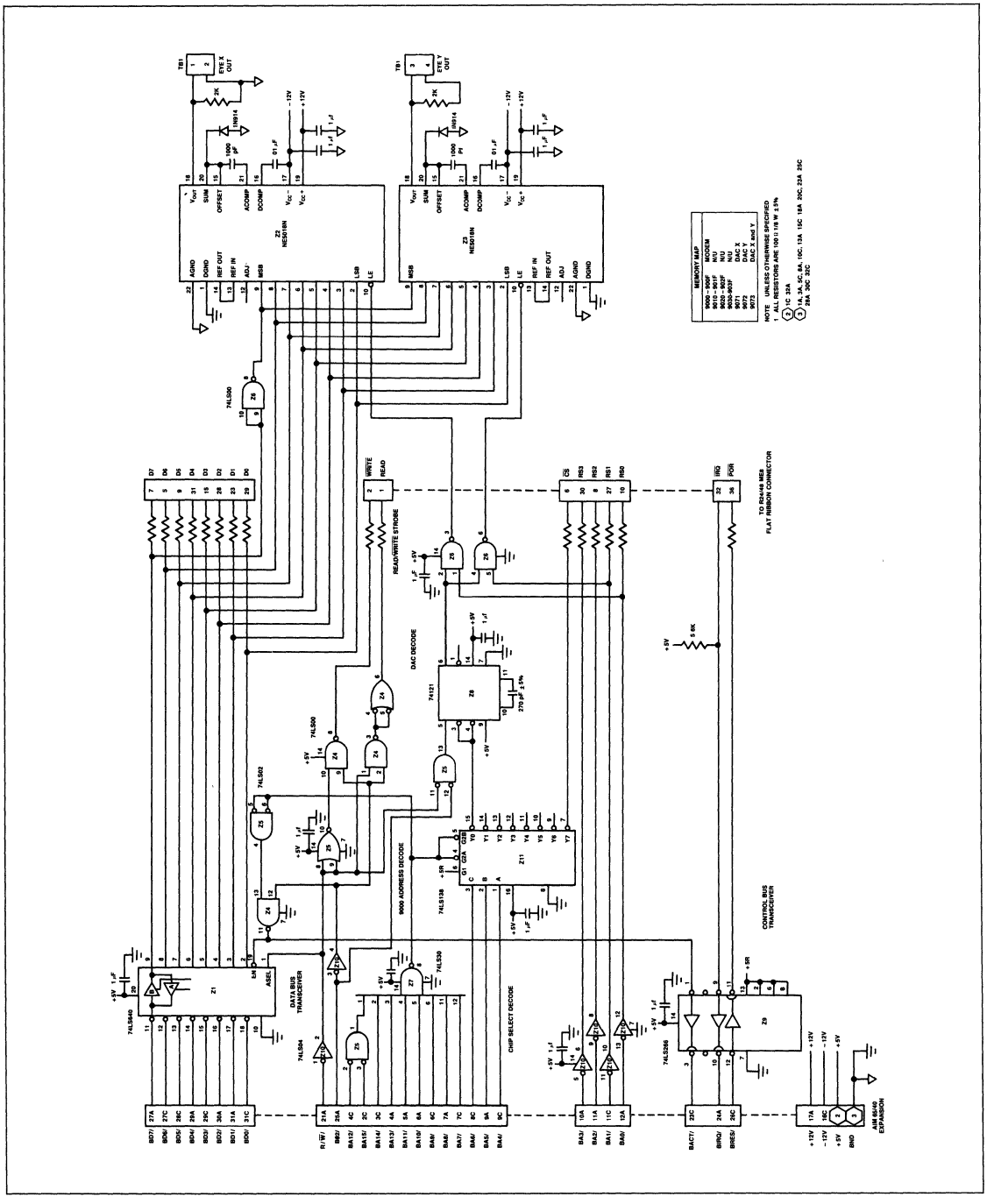


Figure 5. R24/48MEB Microprocessor Bus Interface with Eye Pattern Output

MODEM EVALUATION

EYE PATTERN

The eye pattern is an oscilloscope display of the received baseband constellation. By monitoring this constellation, an observer can often identify common line disturbances as well as defects in the modulation/demodulation process.

In quadrature amplitude modulation (QAM), two multilevel amplitude modulated (AM) carriers are transmitted simultaneously. Interference between these two modulated carriers is minimized by using carriers of identical frequency with a constant 90° relative phase angle. After demodulation, the multilevel baseband signals can be displayed on an oscilloscope with the set of levels received on one carrier displayed on the X axis and the set of levels received on the other carrier displayed on the Y axis. Since these signals consist of discrete levels sent at high data rates, the resulting oscilloscope pattern appears to be a fixed set of points.

Figures 6a through 6d illustrate four examples of an eye pattern. Figure 6a shows the location of four ideal points corresponding to a signal structure using 0 and ±1 for the three amplitude levels. One such signal structure is CCITT Recommendation V.27 at 2400 bits per second. The dashed lines superimposed on the eye pattern represent decision boundaries used by the receiver in deciding which ideal point corresponds to the actual received point. Although the transmitter sends ideal points, line impairments cause the received points to be misaligned. Figure 6b shows the effect of random noise. The received points cluster around the ideal location, but are randomly offset from the ideal point by the noise causing undesired signal modulation. The random offsets are a result of the random nature of the noise. If the line impairment is not random but periodic or is a function of the received signal itself (e.g., harmonic distortion) then the distribution of points around the ideal location is not random. Figure 6c illustrates the tangential smearing resulting from phase jitter and Figure 6d shows the effect of amplitude distortion (either gain jitter or harmonic distortion). The magnitude of the spreading is directly proportional to the severity of the impairment, and represents the quality of the signal or the likelihood of errors in the received data.

Consult the Eye Pattern Generation Flowchart (Figure 7) for an example of eye pattern generation using the address structure indicated in the eye pattern output schematic.

BIT ERROR RATE

Bit Error Rate (BER) is a measure of the steady-state transfer of data on the communication channel. It is the ratio of the number of received bits in error to the number of transmitted bits. This number increases with decreasing signal-to-noise ratio (SNR). The type of line disturbance and the modem configuration also affect the BER.

The BER Performance Test Set-up (Figure 8) illustrates a method of measuring BER in accordance with CCITT Recommendation V.56. The band-limited noise level should be adjusted by the noise attenuator to give the desired signal to noise ratio for the selected received signal level. The modem transmitter is then caused to send a 511-bit pseudo random test pattern. The signal attenuator is set for a received signal level of −20 dBm to simulate leased line operation or −30 dBm to simulate switched network operation. In leased line testing the line simulator should be 3002-C1 or 3002-C2 conditioned.

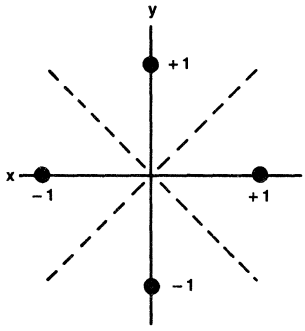
Once the receiver has trained (as indicated by a stable eye pattern) the BER test can begin. A large enough number of bits should be sent to cause at least 10 bit errors to be recorded. BER is calculated by dividing the number of bits in error by the number of bits sent.

The impairment source can be adjusted to provide phase-jitter or frequency offset, etc. The BER tests can be repeated in the presence of these line impairments to determine the amount by which performance has degraded. All BER tests should be conducted under steady-state conditions; i.e., after the adaptive equalizer has stabilized.

Transient response can be measured by using very short polling messages and comparing the number of attempts to send a message with the number of error free messages received for a specific signal to noise ratio and line condition. This type of testing is called block-error-rate (BLER) and can be performed using the same test set-up as bit-error-rate.

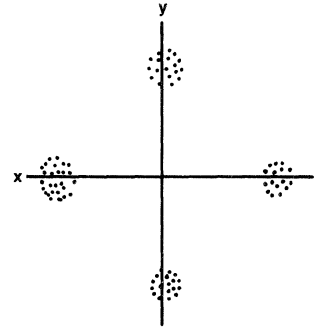
Data throughput for a specific application is determined by a combination of bit-error-rate and block-error-rate. Depending on system architecture, line conditions, error control method used, etc., an optimum message length can be chosen to maximize throughput. As messages become shorter, block-error-rate becomes the limiting factor. As messages become longer, bit-error-rate becomes the limiting factor.

a) IDEAL EYE PATTERN



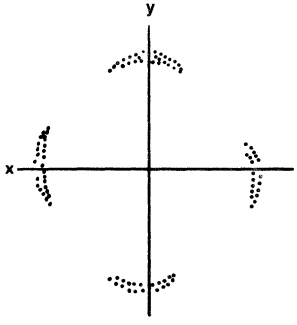
- DASHED LINES REPRESENT DECISION BOUNDARIES

b) WHITE NOISE



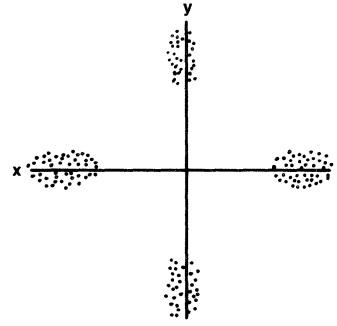
- SMEARING AROUND EACH IDEAL LOCATION

c) PHASE JITTER



- CONTINUOUSLY PERIODIC PHASE SMEARING
- LITTLE OR NO AMPLITUDE SMEARING

d) HARMONIC DISTORTION



- NON-PERIODIC AMPLITUDE SMEARING
- LITTLE PHASE EFFECT
- GAIN-JITTER (AM) EFFECT IS SIMILAR AND IS PERIODIC

*DEGREE OF THE SPREADING OF THE EYE PATTERN IS PROPORTIONAL TO THE SEVERITY OF THE LINE DISTURBANCE

Figure 6. Four Point Eye Patterns

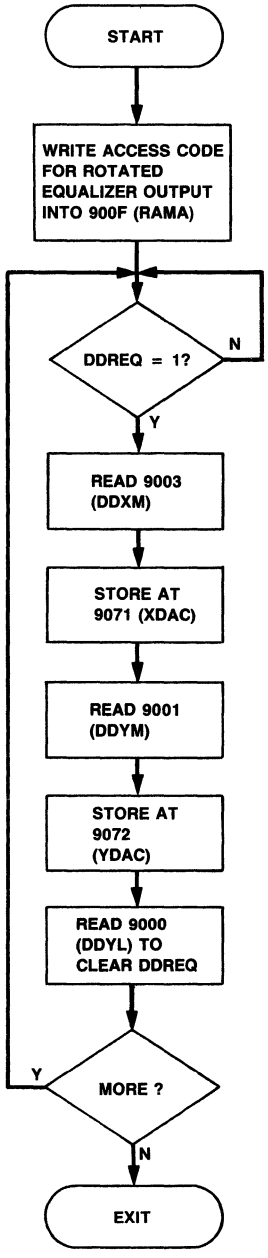


Figure 7. Eye Pattern Generation Flowchart

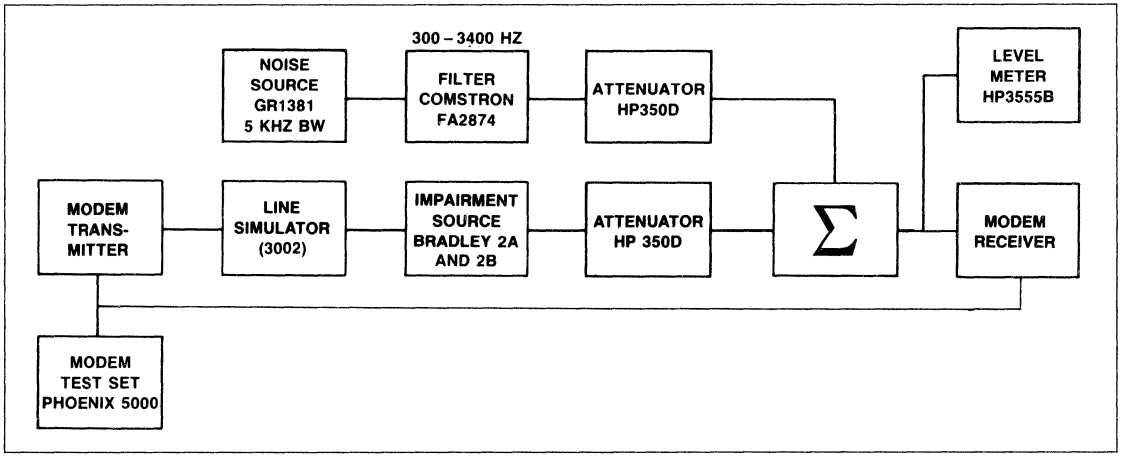


Figure 8. BER Performance Test Set-up

GENERAL SPECIFICATIONS

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	200 mA	<300 mA
+12 Vdc	±5%	5 mA	<10 mA
−12 Vdc	±5%	30 mA	<50 mA

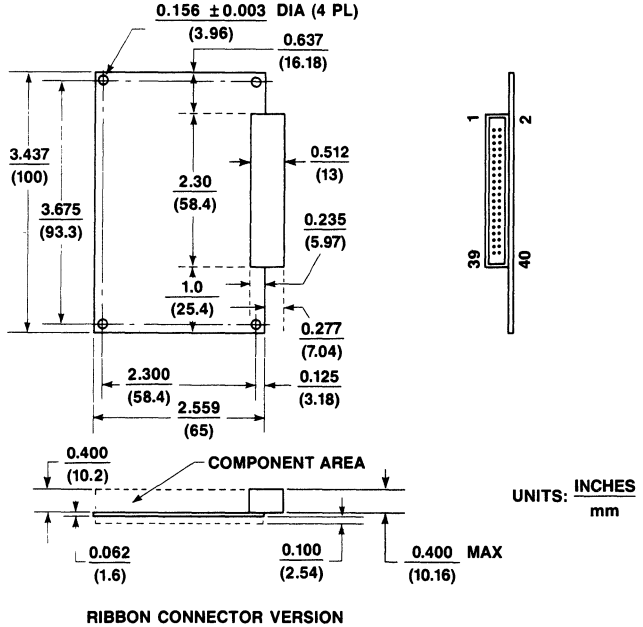
Note: All voltages must have ripple ≤0.1 volts peak-to-peak

Environmental

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 40 pins. Burndy FRS 40BS8P or equivalent mating connector.
Dimensions	
Width	3.937 in. (100 mm)
Length	2.559 in. (65 mm)
Height	0.40 in. (10.2 mm)
Weight (max.)	2.6 oz. (73 g)
Lead Extrusion (max.)	0.100 in. (2.54 mm)



R24/48MEB Dimensions and Pin Locations

Rockwell

R96PCJ
9600 bps PC Communication Modem

INTRODUCTION

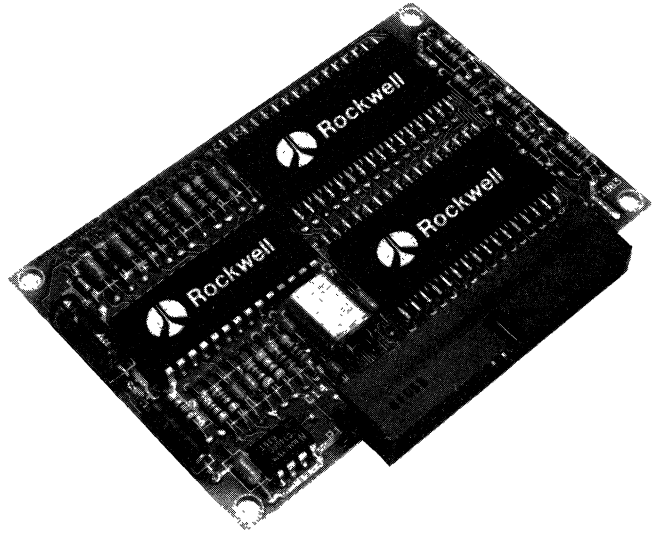
The Rockwell R96PCJ is a synchronous 9600 bits per second (bps) modem designed for operation over the public switched telephone network through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29, V.27 ter, V.21, T.4 and the binary signaling capabilities of T.30. The R96PCJ can operate at speeds of 9600, 7200, 4800, 2400 and 300 bps, and includes the V.27 ter short training sequence option. Employing advanced signal processing techniques, the R96PCJ can transmit and receive data even under extremely poor line conditions.

User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, and serial/parallel host interface simplify system design and allow installation in a small enclosure.

FEATURES

- Ultimate User Compatibility:
  — CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4
- Half-Duplex (2-Wire)
- Programmable Tone Generation and Detection
- Dynamic Range: −47 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
  — Automatic Adaptive
  — Compromise Cable (Selectable)
  — Compromise Link Amplitude (Selectable)
- DTE Interface:
  — Microprocessor Bus
  — CCITT V.24 (RS-232-C Compatible)
- Small Size: 100 mm × 65 mm (3.94 in. × 2.56 in.)
- Low Power Consumption: 2W (typical)
- Transmit Output Level: +5 dBm ±1 dB
- TTL and CMOS Compatible



R96PCJ Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

T.30 Tonal Signaling Frequencies

Function	Frequency (Hz ±0.01 Hz)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100

Carrier Frequencies

Function	Frequency (Hz ±0.01 Hz)
V 27 ter Carrier	1800
V.29 Carrier	1700

TONE GENERATION

Under control of the host processor, the R96PCJ can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

TONE DETECTION

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory of the R96PCJ.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate: Data Rate:	2400 baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate: Date Rate·	1600 baud 4800 bps
Signaling Rate: Data Rate	1200 baud 2400 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

EQUALIZERS

The R96PCJ provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Amplitude Equalizer — The selectable compromise amplitude equalizer may be inserted into the transmit and/or receive paths under control of the transmit amplitude equalizer enable and the receive amplitude equalizer enable bits in the interface memory. The amplitude select bit controls which of two amplitude equalizers is selected.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If neither the link amplitude nor cable equalizer is enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R96PCJ incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

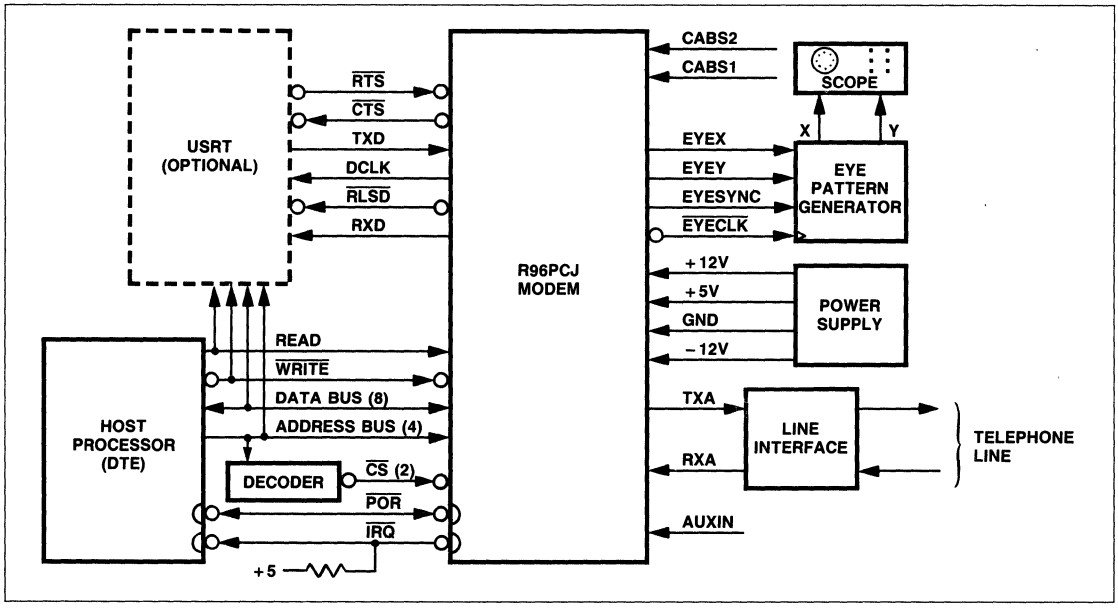
The receiver circuit of the R96PCJ can adapt to received frequency error of up to ±10 Hz with less than a 0.2 dB degradation in BER performance.

RECEIVE LEVEL

The receiver circuit of the R96PCJ satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the R96PCJ provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.



R96PCJ Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 40-pin ribbon connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R96PCJ Hardware Circuits table; the table column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R96PCJ Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground	GND	14, 39	Power Supply Return
+5 volts	PWR	3, 4	+5 Vdc Supply
+12 volts	PWR	26	+12 Vdc Supply
-12 volts	PWR	37	-12 Vdc Supply
$\overline{POR}$	I/OA	36	Power-on-reset

R96PCJ Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	7	Data Bus (8 Bits)
D6	I/OA	5	
D5	I/OA	9	
D4	I/OA	31	
D3	I/OA	15	
D2	I/OA	28	
D1	I/OA	23	
D0	I/OA	29	
RS3	IA	30	Register Select (4 Bits) Select Reg. 0 - F
RS2	IA	8	
RS1	IA	27	
RS0	IA	10	
$\overline{CS0}$	IA	6	Chip Select Sample Rate Device
$\overline{CS1}$	IA	18	Chip Select Baud Rate Device
$\overline{READ}$	IA	1	Read Enable
$\overline{WRITE}$	IA	2	Write Enable
$\overline{IRQ}$	OB	32	Interrupt Request
C. V.24 INTERFACE:			
$\overline{DCLK}$	OC	13	Data Clock
$\overline{RTS}$	IB	19	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	20	Transmitter Data
$\overline{RXD}$	OC	21	Receiver Data
$\overline{RLSD}$	OC	16	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IC	33	Cable Select 1
CABS2	IC	34	Cable Select 2

TRANSMIT LEVEL

The transmitter output level is fixed at +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the R96PCJ provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz (±0.01%).
2. *Duty Cycle.* 50 ±1%.

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

A total of 14 selectable turn-on sequences can be generated as defined in the following table:

Turn-On Sequences

No.	V.29	V.27 ter	$\overline{CTS}$ [2] Response Time (milliseconds)	Comments
1	9600 bps		253	
2	7200 bps		253	
3	4800 bps		253	
4		4800 bps long	708	
5		2400 bps long	943	
6		4800 bps short	50	
7		2400 bps short	67	
8	9600 bps		438	Preceded by [1]
9	7200 bps		438	Echo Protector
10	4800 bps		438	Tone for lines
11		4800 bps long	913	using echo
12		2400 bps long	1148	suppressors
13		4800 bps short	255	
14		2400 bps short	272	

1 Turn-on sequences 8 through 14 are used on lines with protection against talker echo.
2 V.21 (300 bps FSK) $\overline{RTS}$-$\overline{CTS}$ delay is 14 ms or less.

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{RTS}$ goes false.

CLAMPING

The following clamps are provided with the R96PCJ:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector (RLSD).* $\overline{RLSD}$ is clamped off (squelched) during the time when $\overline{RTS}$ is on.
3. *Extended Squelch.* Optionally, $\overline{RLSD}$ remains clamped off for 130 ms after the turn-off sequence.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the length of the training sequence. Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps. In V.21 $\overline{CTS}$ turns on in 14 ms or less.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

For either V.27 ter or V.29, $\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RLSD}$ off-to-on response time is 15 ±10 ms. The $\overline{RLSD}$ on-to-off response time for V.27 is 10 ±5 ms and for V.29 is 30 ±9 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided:

1. Greater than −43 dBm ($\overline{RLSD}$ on)
   Less than −48 dBm ($\overline{RLSD}$ off)
2. Greater than −47 dBm ($\overline{RLSD}$ on)
   Less than −52 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R96PCJ is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the R96PCJ Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R96PCJ has the capability of transferring channel data eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R96PCJ is configured by the host processor via the microprocessor bus.

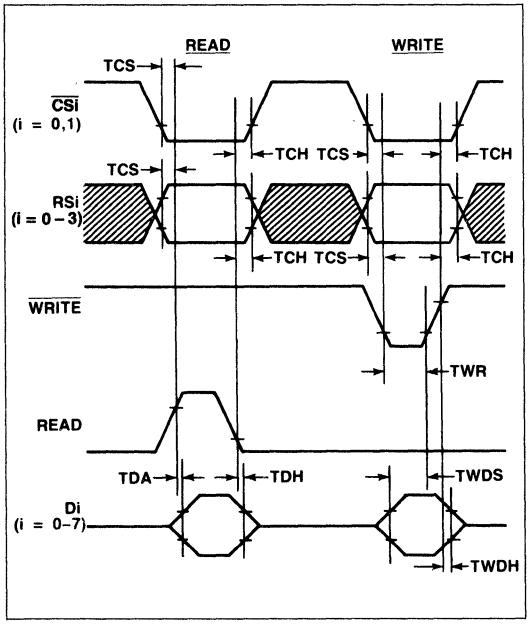
R96PCJ Hardware Circuits (Cont.)

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXA	AA	38	Transmitter Analog Output
RXA	AB	40	Receiver Analog Input
AUXIN	AC	35	Auxiliary Analog Input
F. DIAGNOSTIC:			
EYEX	OC	24	Eye Pattern Data — X Axis
EYEY	OC	25	Eye Pattern Data — Y Axis
EYECLK	OA	11	Eye Pattern Clock
EYESYNC	OA	12	Eye Pattern Synchronizing Signal

Eye Pattern Generation

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words obtained from registers 1:3 and 1:1 (see RAM Data Access) are shifted out most significant bit first clocked by the rising edge of the EYECLK output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

Microprocessor Timing



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
CSi, RSi setup time prior to Read or Write	TCS	30	—	ns
Data Access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
CSi, RSi hold time after Read or Write	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Cable Equalizer Selection

Cable Equalizer Selection

CABS 2	CABS 1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Digital Interface Characteristics

The digital interface characteristics are listed in the table on the following page.

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −0.4 dB ±1 dB.

SOFTWARE CIRCUITS

The R96PCJ comprises two signal processor chips. Each chip contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data from or write data to these registers. The registers are referred to as interface memory. Registers in chip 0 update at the modem sample rate (9600 bps). Registers in chip 1 update at the selected baud rate.

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type							
			IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 min.	2 0 min	2 0 min				2 0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max	0 8 max.				0 8 max.	0.8 max
V_{OH}	Output Voltage, High	V				2.4 min.[1]			2.4 min [1]	2 4 min [3]
V_{OL}	Output Voltage, Low	V				0.4 max.[2]	0.4 max.[2]	0 4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max						±12 5 max.[4]	
I_{OH}	Output Current, High	mA				−0.1 max.				
I_{OL}	Output Current, Low	mA				1 6 max	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max −10 min.	−240 max. −10 min.			−240 max. −10 min.		−260 max. −100 min.
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Status/Control Bits

The operation of the R96PCJ is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Bits designated by an 'X' are "Don't Care" inputs that can be set to either 1 or 0. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by an '—' are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R96PCJ provides the user with access to much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

Two RAM access registers are provided in the interface memory to allow user access to various RAM locations within the modem. The access code stored in 0:F selects the source of data for the RAM data registers in chip 0 (0:0 through 0:3). Similarly, the access code stored in 1:F selects the source of data for registers 1:0 through 1:3. Reading is performed by storing the desired access code in register 0:F (or 1:F), performing a read of 0:0 (or 1:0) to reset 0:E:0 (or 1:E:0), then waiting for 0:E:0 (or 1:E:0) to return to a one. The data may now be read from 0:3 through 0:0 (or 1:3–1:0).

Data in registers 1:3 and 1:1 are presented serially on EYEX and EYEY, respectively.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

R96PCJ RAM Access Codes

Node	Function	Access	Chip	Reg. No.
1	Received Signal Samples	40	0	2,3
2	Demodulator Output	42	0	0,1,2,3
3	Low Pass Filter Output	54	0	0,1,2,3
4	Average Energy	5C	0	2,3
5	AGC Gain Word	01	0	2,3
6	Equalizer Input	40	1	0,1,2,3
7	Equalizer Tap Coefficients	01-20	1	0,1,2,3
8	Unrotated Equalizer Output	61	1	0,1,2,3
9	Rotated Equalizer Output (Received Point—Eye Pattern)	22	1	0,1,2,3
10	Decision Points (Ideal)	62	1	0,1,2,3
11	Error Vector	63	1	0,1,2,3
12	Rotation Angle	00	1	0,1
13	Frequency Correction	A8	1	2,3
14	EQM	AB	1	,2,3

R96PCJ Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	—	—	—	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	X	X	EPT	SQEXT	T2	LRTH
4	CONFIGURATION							
3	RAM DATA XSM; FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL; TRANSCEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

X = User available (not used by modem)
— = Reserved (modem use only)

R96PCJ Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	—	—	—	—	IE1	—	MDA1
D	X	TLE	RLE	J3L	X	X	X	—
C	X	X	X	X	X	X	X	X
B	FR3	FR2	FR1	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{FED}$	—	—	—	—	—	—
4	—	—	—	—	—	$\overline{P2DET}$	—	—
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

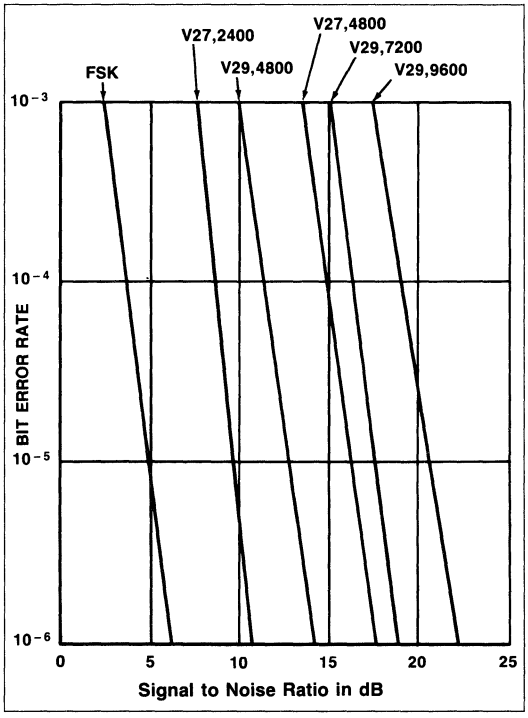
X = User available (not used by modem).
— = Reserved (modem use only).

R96PCJ Interface Memory Definitions

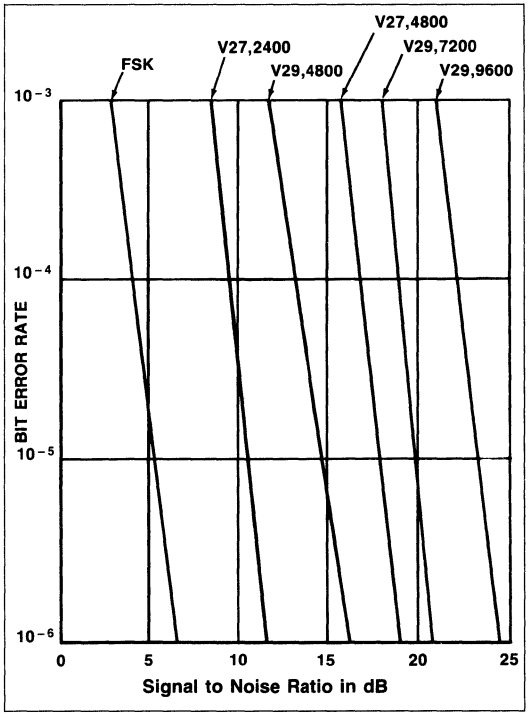
Mnemonic	Name	Memory Location	Description
$\overline{\text{CDET}}$	Carrier Detector	1:7 0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present. $\overline{\text{CDET}}$ goes to zero at the start of the data state, and returns to one at the end of the received signal $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
(None)	Configuration	0:4:0–7	The host processor configures the R96PCJ by writing a control code into the configuration register in the interface memory space. (See SETUP.) ***Configuration Control Codes*** Control codes for the four available R96PCJ configurations are: **Configuration** — **Configuration Code (HEX)** V.29 9600 — 14 V.29 7200 — 12 V.29 4800 — 11 V.27 4800 Long — 0A V.27 2400 Long — 09 V.27 4800 Short — 4A V.27 2400 Short — 49 Tone Transmit — 80 FSK — 20 ***Configuration Definitions*** Definitions for the four available R96PCJ configurations are: 1. *V.29.* When any of the V.29 configurations has been selected, the modem operates as specified in CCITT Recommendation V.29. 2. *V.27.* When any of the V.27 configurations has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 3. *FSK.* The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system. 4. *Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%.
EPT	Echo Protector Tone	0.5:3	If EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. This option is available in both the V.27 and V.29 configurations, although it is not specified in the CCITT V.29 Recommendation.
$\overline{\text{FED}}$	Fast Energy Detector	1:5.6	The zero state of $\overline{\text{FED}}$ indicates energy is present above the receiver threshold in the passband.
(None)	FREQL/FREQM	0:2:0-7, 0:3:0-7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below. *FREQM Register (0:3)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0}

R96PCJ Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
			The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01%. Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given below: **Frequency (Hz) / FREQM / FREQL** 462 / 0C / 52 1100 / 1D / 55 1650 / 2C / 00 1850 / 31 / 55 2100 / 38 / 00
FR1 – FR3	Frequency 1,2,3	1:B:5,6,7	The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for FSK. The default frequencies for FR1, FR2 and FR3 are: **Bit / Frequency (Hz)** FR1 / 2100 FR2 / 1100 FR3 / 462
IA1	Interrupt Active (One)	1:E:7	IA1 is a one when Chip 1 is driving $\overline{IRQ}$ to zero volts.
IA0	Interrupt Active (Zero)	0:E:7	IA0 is a one when Chip 0 is driving $\overline{IRQ}$ to zero volts.
IE0	Interrupt Enable (Zero)	0:E:2	The one state of IE0 causes the $\overline{IRQ}$ output to be low when the DA0 bit is a one.
IE1	Interrupt Enable (One)	1:E:2	The one state of IE1 causes the $\overline{IRQ}$ output to be low when the DA1 bit is a one.
J3L	Japanese 3 Link	1:D:4	The one state of J3L selects this standard for link amplitude equalizer. The zero state of J3L selects U.S. survey long.
LRTH	Lower Receive Threshold	0:5:0	The one state of LRTH lowers the receiver turn-on threshold from −43 dBm to −47 dBm. (See SETUP.)
MDA0	Modem Data Available (Zero)	0:E:0	MDA0 goes to one when the modem reads or writes register 0:0. MDA0 goes to zero when the host processor reads or writes register 0:0. MDA0 is used for parallel mode as well as for diagnostic data retrieval.
MDA1	Modem Data Available (One)	1:E:0	MDA1 goes to one when the modem writes register 1:0. MDA1 goes to zero when the host processor reads register 1:0.
PDM	Parallel Data Mode	0:F:7	The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.
$\overline{PNDET}$	Period 'N' Detector	1:7:6	The zero state of $\overline{PNDET}$ indicates a PN sequence has been detected. $\overline{PNDET}$ sets to a one at the end of the PN sequence.
$\overline{P2DET}$	Period '2' Detector	1:4:2	The zero state of $\overline{P2DET}$ indicates a P2 sequence has been detected. $\overline{P2DET}$ sets to a one at the start of the PN sequence.
(None)	RAM Access B	1:F:0–7	Contains the RAM access code used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Access S	0:F:0–6	Contains the RAM access code used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XBL	1:2:0–7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device)
(None)	RAM Data XBM	1:3:0–7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).

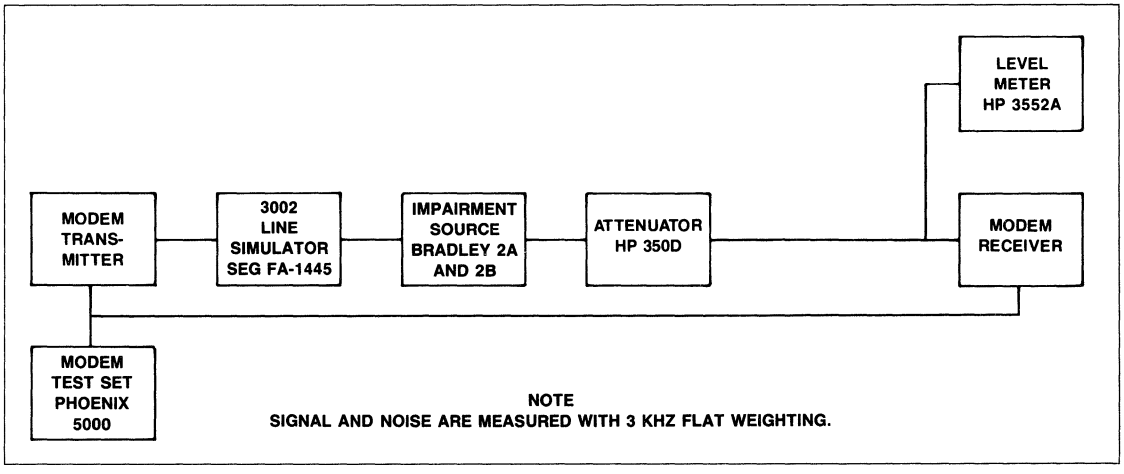


Typical Bit Error Rate
(Back to Back, T Equalizer, Level −20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, T Equalizer, Level −20 dBm)

The BER performance test set-up is shown in the following diagram:



BER Performance Test Set-up

R96PCJ Interface Memory Definitions (continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>RAM Data XSL</td><td>0:2:0–7</td><td>Least significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).</td></tr>
<tr><td>(None)</td><td>RAM Data XSM</td><td>0:3:0–7</td><td>Most significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).</td></tr>
<tr><td>(None)</td><td>RAM Data YBL</td><td>1:0:0–7</td><td>Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device). (See DA1.)</td></tr>
<tr><td>(None)</td><td>RAM Data YBM</td><td>1:1:0–7</td><td>Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device).</td></tr>
<tr><td>(None)</td><td>RAM Data YSL</td><td>0:0:0–7</td><td>Least significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device). Shared by parallel data mode for presenting channel data to the host microprocessor bus. (See Transceiver Data and DA0.)</td></tr>
<tr><td>(None)</td><td>RAM Data YSM</td><td>0:1:0–7</td><td>Most significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device).</td></tr>
<tr><td>RLE</td><td>Receiver Link Equalizer</td><td>1:D:5</td><td>The one state of RLE enables the link amplitude equalizer in the receiver.</td></tr>
<tr><td>RTS</td><td>Request-to-Send</td><td>0:5:7</td><td>The one state of RTS begins a transmit sequence. The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed. RTS parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are "ORed" by the modem.</td></tr>
<tr><td>SETUP</td><td>Setup</td><td>0:E:3</td><td>The one state of SETUP causes the modem to reconfigure to the control word in the configuration register, and to assume the options specified for equalizer (0:5:1) and threshold (0:5:0). SETUP returns to zero when acted on by the modem. The time required for the SETUP bit to cause a change depends on the current state of the modem. The following table lists worst case delays.
<table>
<tr><th>Current State</th><th>V.21</th><th>High Speed Receiver</th><th>High Speed Transmitter</th></tr>
<tr><td>DELAY</td><td>14 ms</td><td>2 BAUD</td><td>2 BAUD + TURNOFF Sequence + Training (if applicable) + SQUELCH (if applicable)</td></tr>
</table>
</td></tr>
<tr><td>SQEXT</td><td>Squelch Extend</td><td>0:5:2</td><td>The one state of SQEXT inhibits reception of signals for 130 ms after the turn-off sequence.</td></tr>
<tr><td>TDIS</td><td>Training Disable</td><td>0:5:6</td><td>If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one prior to $\overline{RTS}$ going on, the generation of a training sequence is prevented at the start of transmission.</td></tr>
<tr><td>TLE</td><td>Transmitter Link Equalizer</td><td>1:D:6</td><td>The one state of TLE enables the link amplitude equalizer in the transmitter.</td></tr>
<tr><td>(None)</td><td>Transceiver Data</td><td>0:0·0–7</td><td>In receive parallel data mode, the modem presents eight bits of channel data in register 0:0 for reading by the host microprocessor. After the eight bits have been accumulated in register 0:C they are transferred to 0:0 and bit 0:E:0 goes to a one. When the host reads 0:0, bit 0:E:0 resets to a zero. The first bit of received data is not necessarily located in bit 0:0:0. The host must frame the received data by searching for message sync characters. Bit 0:E:0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations.

In transmit parallel data mode, the host stores data at location 0:0. This action causes bit 0:E:0 to reset to a 0. When the modem transfers the data from 0:0 to 0:2 bit 0:E:0 sets to a 1. The data is serially transmitted from register 0:2 least significant bit first. Received data is shifted into register 0:C from MSB toward LSB.</td></tr>
<tr><td>T2</td><td>T/2 Equalizer Select</td><td>0:5:1</td><td>If T2 is a one, an adaptive equalizer with two taps per baud is used. If T2 is a zero, an adaptive equalizer with one tap per baud is used. The number of taps remains the same for both cases. (See SETUP.)</td></tr>
</table>

POWER-ON INITIALIZATION

When power is applied to the R96PCJ, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low-to-high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 ms, the $\overline{POR}$ cycle is repeated.

At $\overline{POR}$ time the modem defaults to the following configuration: V.29/9600 bps, T/2 equalizer, serial mode, training enabled, echo protector tone on, no extended squelch, higher receive threshold, interrupts disabled, no link equalizer, and RAM access codes 00.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μs or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 ms after the low active pulse is removed from $\overline{POR}$.

PERFORMANCE

Whether functioning as a V.27 ter or V.29 type modem, the R96PCJ provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm as illustrated.

TYPICAL PHASE JITTER

At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

An example of the BER performance capabilities is given in the following diagrams:

GENERAL SPECIFICATIONS

Power

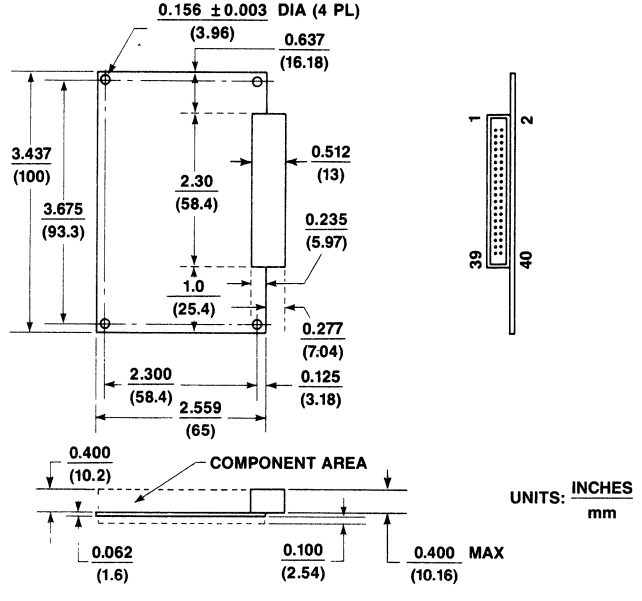
Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	400 mA	<500 mA
+12 Vdc	±5%	5 mA	<10 mA
−12 Vdc	±5%	30 mA	<50 mA
Note: All voltages must have ripple ≤0.1 volts peak-to-peak			

Environmental

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 40 pins. Burndy FRS 40BS8P or equivalent mating connector.
Dimensions	
Width	3.937 in. (100 mm)
Length	2.559 in. (65 mm)
Height	0.40 in. (10.2 mm)
Weight (max)	2.6 oz. (73 g)
Lead Extrusion (max)	0.100 in. (2.54 mm)



RIBBON CONNECTOR VERSION

R96PCJ Dimensions and Pin Locations

Rockwell

R96F
9600 bps Facsimile Modem

INTRODUCTION

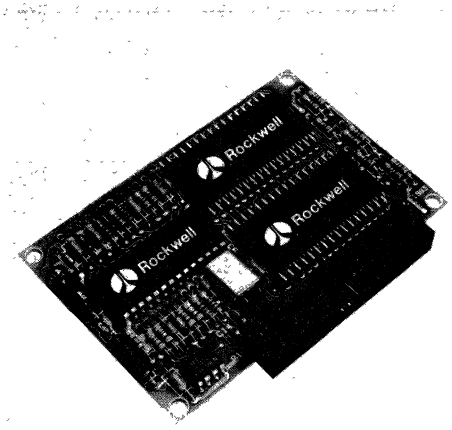
The Rockwell R96F is a synchronous 9600 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29, V.27 ter, T.30, T.4 and T.3. The R96F can operate at speeds of 9600, 7200, 4800, 2400 and 300 bps. Employing advanced signal processing techniques, the R96F can transmit and receive data even under extremely poor line conditions.

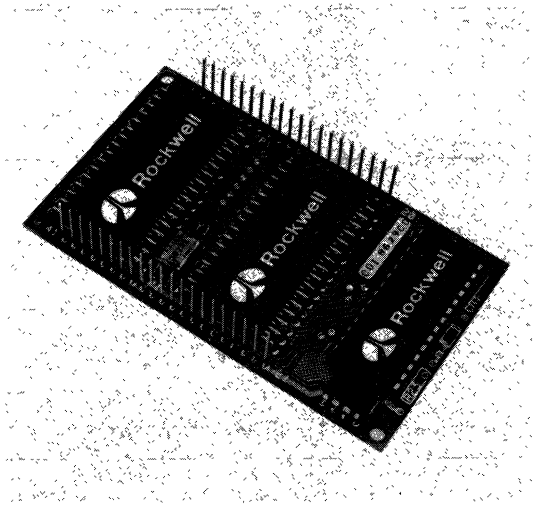
The R96F is designed for use in Group 3 facsimile machines and is also compatible with Group 2 machines. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, serial/parallel host interface, simplify system design. Two module versions are available: one with a ribbon connector for cable connection to a host, and one with dual in-line pins for direct connection onto a host module.

FEATURES

- Compatibility:
  - — CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4, T.3
- Group 3 and Group 2 Facsimile
- Half-Duplex (2-Wire)
- Tone Detection
- Programmable Tone Generation and Detection
- Dynamic Range: −47 dBm to 0 dBm
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
  - — Compromise Link Amplitude (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Small Size:
  - — Ribbon cable connector version
    100 mm × 65 mm (3.94 in. × 2.56 in.)
  - — Dual in-line pin (DIP) connector version
    88.9 mm × 50.8 mm (3.5 in. × 2.0 in.)
- Low Power Consumption: 2 W (Typical)
- Transmit Output Level: +5 dBm ±1 dB
- TTL and CMOS Compatible



R96F Ribbon Connector Version



R96F DIP Connector Version

TECHNICAL SPECIFICATIONS

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

T.30 Tonal Signaling Frequencies

Function	Frequency (Hz ±0.01%)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group 2 Identification (C12)	1850
Group 2 Command (GC2)	2100
Group 2 Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462

Carrier Frequencies

Function	Frequency (Hz ±0.01%)
T.3 Carrier (Group 2)	2100
V.27 ter Carrier	1800
V.29 Carrier	1700

TONE GENERATION

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

TONE DETECTION

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory of the modem.

SIGNALING AND DATA RATES

Signaling/Data Rates

Parameter	Specification (±0.01%)
Signaling Rate: Data Rate:	2400 baud 9600 bps, 7200 bps, 4800 bps
Signaling Rate: Date Rate:	1600 baud 4800 bps
Signaling Rate: Data Rate:	1200 baud 2400 bps

DATA ENCODING

At 2400 baud, the data stream is encoded per CCITT V.29. At 9600 bps, the data stream is divided in groups of four-bits (quadbits) forming a 16-point structure. At 7200 bps, the data stream is divided into three bits (tribits) forming an 8-point structure. At 4800 bps, the data stream is divided into two bits (dibits) forming a 4-point structure.

At 1600 baud, the 4800 bps data stream is encoded into tribits per CCITT V.27 ter.

At 1200 baud, the 2400 bps data stream is encoded into dibits per CCITT V.27 ter.

EQUALIZERS

The modem provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Amplitude Equalizer — The selectable compromise amplitude equalizer may be inserted into the transmit and/or receive paths under control of the transmit amplitude equalizer enable and the receive amplitude equalizer enable bits in the interface memory. The amplitude select bit controls which of two amplitude equalizers is selected.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

If neither the link amplitude nor cable equalizer is enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The modem receiver circuit can adapt to received frequency error of up to ±10 Hz with less than a 0.2 dB degradation in BER performance. Group 2 carrier recovery capture range is 2100 ±30 Hz. The Group 2 receiver operates properly when the carrier is varied by ±16 Hz at a 0.1 Hz per second rate.

RECEIVE LEVEL

The modem receiver circuit satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the modem provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level is fixed at +5 dBm ±1 dB. When driving a 600 ohm load the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load.

TRANSMIT TIMING

In the transmit state, the modem provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz (±0.01%). In Group 2, DCLK tracks an external 10368 Hz clock. If the external clock input (XCLK) is grounded, the Group 2 DCLK is 10372.7 Hz ±0.01%.
2. *Duty Cycle.* 50 ±1%

Transmit Data (TXD) must be stable during the 1 microsecond period immediately preceding and the 1 microsecond period immediately following the rising edge of DCLK.

TURN-ON SEQUENCE

A total of ten selectable turn-on sequences can be generated by the modem, as defined in the following table:

Turn-On Sequences

Specification	$\overline{\text{RTS}}$-$\overline{\text{CTS}}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.29	253 ms	438 ms
V.27 4800 bps	708 ms	913 ms
V.27 2400 bps	943 ms	1148 ms
V.21 300 bps	≤14 ms	≤14 ms
Group 2	≤400 μs	≤400 μs

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{\text{RTS}}$ goes false. In Group 2 the transmitter turns off within 200 μs after $\overline{\text{RTS}}$ goes false.

CLAMPING

The following clamps are provided with the modem:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{\text{RLSD}}$ is off.
2. *Received Line Signal Detector (RLSD).* $\overline{\text{RLSD}}$ is clamped off (squelched) during the time when $\overline{\text{RTS}}$ is on.
3. *Extended Squelch.* Optionally, $\overline{\text{RLSD}}$ remains clamped off for 130 ms after the turn-off sequence.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{\text{CTS}}$)

The time between the off-to-on transition of $\overline{\text{RTS}}$ and the off-to-on transition of $\overline{\text{CTS}}$ is dictated by the length of the training sequence. Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps. In V.21 $\overline{\text{CTS}}$ turns on in 14 ms or less. In Group 2 $\overline{\text{CTS}}$ turns on in 400 μs or less.

The time between the on-to-off transition of $\overline{\text{RTS}}$ and the on-to-off transition of $\overline{\text{CTS}}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{\text{RLSD}}$)

For either V.27 ter or V.29, $\overline{\text{RLSD}}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{\text{RLSD}}$ off-to-on response time is 15 ±10 ms. The $\overline{\text{RLSD}}$ on-to-off response time for V.27 is 10 ±5 ms and for V.29 is 30 ±9 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{\text{RLSD}}$ on threshold or at least 5 dB below the actual $\overline{\text{RLSD}}$ off threshold.

The $\overline{\text{RLSD}}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided:

1. Greater than −43 dBm ($\overline{\text{RLSD}}$ on)
   Less than −48 dBm ($\overline{\text{RLSD}}$ off)
2. Greater than −47 dBm ($\overline{\text{RLSD}}$ on)
   Less than −52 dBm ($\overline{\text{RLSD}}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The modem operates in either a serial or a parallel mode.

SERIAL MODE

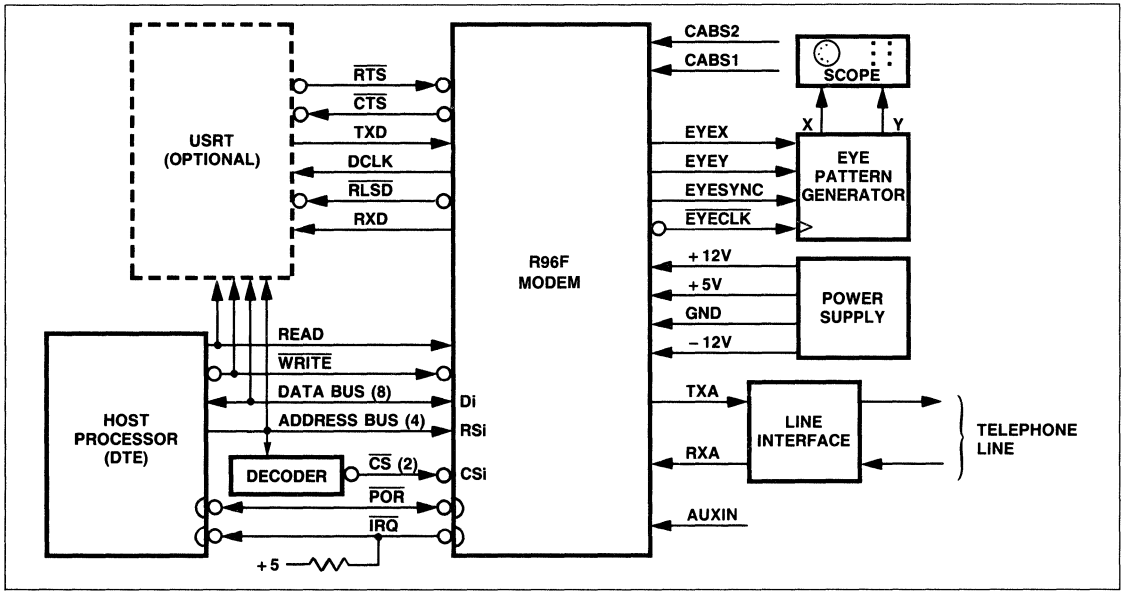
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Modem Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The modem can transfer channel data eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the modem is configured by the host processor via the microprocessor bus.



Modem Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 40-pin ribbon connector or in a 41-pin dual in-line pin connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the Modem Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital or Analog Interface Characteristics.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0–RS3), data (D0–D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

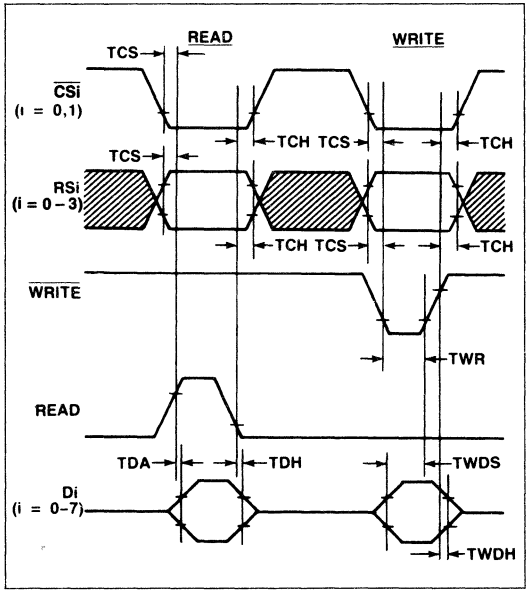
To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Modem Hardware Circuits (Cont.)

Name	Type	RC Pin No.	DIP Pin No.	Description
E. ANALOG SIGNALS:				
TXA	AA	38	23	Transmitter Analog Output
RXA	AB	40	22	Receiver Analog Input
AUXIN	AC	35	20	Auxiliary Analog Input
F. DIAGNOSTIC:				
EYEX	OC	24	35	Eye Pattern Data — X Axis
EYEY	OC	25	40	Eye Pattern Data — Y Axis
$\overline{\text{EYECLK}}$	OA	11	36	Eye Pattern Clock
EYESYNC	OA	12	37	Eye Pattern Synchronizing Signal
RC = Ribbon connector DIP = Dual in-line pins				

Diagnostic

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the $\overline{\text{EYECLK}}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{\text{CSi}}$, RSi setup time prior to Read or $\overline{\text{Write}}$	TCS	30	—	ns
Data Access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
CSi, RSi hold time after Read or $\overline{\text{Write}}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 60K ohms ±23%.
AUXIN	AC	The auxiliary analog input allows access to the transmitter for the purpose of interfacing with user provided equipment. Because this is a sampled data input, any signal above 4800 Hz will cause aliasing errors. The input impedance is 1K ohms, and the gain to transmitter output is −0.4 dB ±1 dB.

SOFTWARE CIRCUITS

The modem includes two signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 0 update at the modem sample rate (9600 bps). Registers in chip 1 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Status/Control Bits

Modem operation is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a '—' are reserved for modem use only and must not be changed by the host.

Cable Equalizer Selection

CABS2	CABS1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Three analog signals provide the interface point for telephone company audio circuits and host audio inputs: TXA, RXA, and AUXIN.

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the PSTN. The output structure of TXA is a low impedance amplifier in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source. A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may be back-to-back zener diodes across the transformer or a varistor across the transformer.

AUXIN provides a means of inserting audio signals into the modem output stage. Because this input is summed with the transmitter output prior to the transmitter low pass filter and compromise equalizers, the AUXIN signal is sampled by a compensated sample-and-hold circuit at a rate of 9600 samples-per-second. Any signal above 4800 Hz on the AUXIN line will be aliased back into the passband as noise. One application for AUXIN is to inject dual-tone multifrequency (DTMF) touch-tone signals for dialing, however, the source of these tones must be well filtered to eliminate components above 4800 Hz. The input impedance of AUXIN is 1K ohm. The gain from AUXIN to TXA is −0.4 dB ±1 dB.

Overhead

Except for the power-on-reset signal $\overline{POR}$, the overhead signals are dc power or ground points. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives the $\overline{POR}$ pin to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of the $\overline{POR}$ pin, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives the $\overline{POR}$ pin low for at least 3 μs. When an external low input is applied to the $\overline{POR}$ pin, the modem is ready for normal use approximately 10 ms after the low input is removed. The $\overline{POR}$ pin is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The POR sequence leaves the modem configures as follows:

- V.29/9600 bps
- T/2 equalizer
- Serial mode
- Training enabled
- Echo protector tone enabled
- No extended squelch
- Higher receive threshold
- Interrupts disabled
- No link equalizer
- RAM access codes 00

This configuration is suitable for performing high speed data transfer on the PSTN with the serial data port selected as the input and output point for data terminal equipment (DTE).

Modem Hardware Circuits

Name	Type	RC Pin No.	DIP Pin No.	Description
A. OVERHEAD:				
Ground	GND	14, 39	17,18, 41*	Power Supply Return
+5 volts	PWR	3, 4	33,34	+5 volt supply
+12 volts	PWR	26	21	+12 volt supply
−12 volts	PWR	37	19	−12 volt supply
$\overline{POR}$	I/OB	36	39	Power-on-reset
B. MICROPROCESSOR INTERFACE:				
D7	I/OA	7	9	Data Bus (8 Bits)
D6	I/OA	5	8	
D5	I/OA	9	2	
D4	I/OA	31	3	
D3	I/OA	15	4	
D2	I/OA	28	5	
D1	I/OA	23	6	
D0	I/OA	29	7	
RS3	IA	30	13	Register Select (4 Bits) Select Reg. 0 − F
RS2	IA	8	14	
RS1	IA	27	15	
RS0	IA	10	16	
$\overline{CS0}$	IA	6	11	Chip Select Sample Rate Device
$\overline{CS1}$	IA	18	38	Chip Select Baud Rate Device
READ	IA	1	10	Read Enable
$\overline{WRITE}$	IA	2	12	Write Enable
$\overline{IRQ}$	OB	32	1	Interrupt Request
C. V.24 INTERFACE:				
DCLK	OC	13	30	Data Clock
XCLK	IB	22	31	External Clock for Group 2
$\overline{RTS}$	IB	19	32	Request-to-Send
$\overline{CTS}$	OC	17	28	Clear-to-Send
TXD	IB	20	27	Transmitter Data
RXD	OC	21	26	Receiver Data
$\overline{RLSD}$	OC	16	29	Received Line Signal Detector
D. CABLE EQUALIZER:				
CABS1	IC	33	24	Cable Select 1
CABS2	IC	34	25	Cable Select 2

*Pin 41 added for connector keying, not for use as a ground.

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	IC	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 min	2.0 min	2.0 min				2 0 min	5.25 max 2 0 min
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.	0 8 max				0.8 max	0 8 max.
V_{OH}	Output Voltage, High	V				2.4 min [1]			2 4 min. [1]	2 4 min.[3]
V_{OL}	Output Voltage, Low	V				0.4 max [2]	0.4 max [2]	0.4 max [2]	0 4 max.[2]	0 4 max.[5]
I_{IN}	Input Current, Leakage	μA	± 2.5 max.						± 12 5 max.[4]	
I_{OH}	Output Current, High	mA				− 0.1 max				
I_{OL}	Output Current, Low	mA				1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA					± 10 max			
I_{PU}	Pull-up Current (Short Circuit)	μA		− 240 max. − 10 min.	− 240 max. − 10 min.			− 240 max − 10 min.		− 260 max. − 100 min
C_L	Capacitive Load	pF	5	5	20				10	40
C_D	Capacitive Drive	pF				100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = − 100 μA 5 I load = 0.36 mA
2. I load = 1.6 mA
3. I load = − 40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc

3

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

RAM Data Access

The user can access much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

Two RAM access registers are provided in the interface memory to allow user access to various RAM locations within the modem. The access code stored in 0:F selects the source of data for the RAM data registers in chip 0 (0:0 through 0:3). Similarly, the access code stored in 1:F selects the source of data for registers 1:0 through 1:3. Reading is performed by storing the desired access code in register 0:F (or 1:F), performing a read of 0:0 (or 1:0) to reset 0:E:0 (or 1:E:0), then waiting for 0:E:0 (or 1:E:0) to return to a one. The data may now be read from 0:3 through 0:0 (or 1:3–1:0).

Chip one also provides the capability to write data into RAM. When bit RAMW is set to a one, reading is suspended and a write cycle takes place once each time bit DA1 (1·E:0) is reset to zero.

Writing is performed by storing the desired access code in register 1:F, waiting for bit DA1 (1:E:0) to be a 1, setting bit RAMW (1:D:0) to a 1, then storing sixteen bits of data in registers 1:1 and 1:0. The eight bits in 1:1 are most significant. Writing to 1:0 resets bit 1:E:0 to a 0 and starts the write cycle, which ends by 1:E:0 returning to a 1. Bit RAMW (1:D:0) must remain set until the end of the cycle.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem. The access code stored in chip 1 (1:F) also selects the source of data for the serial outputs EYEX and EYEY. Diagnostic data is scaled as shown in the Diagnostic Data Scaling table.

RAM Access Codes

Node	Function	Access	Chip	Reg. No.
1	Received Signal Samples	40	0	2,3
2	Demodulator Output	42	0	0,1,2,3
3	Low Pass Filter Output	54	0	0,1,2,3
4	Average Power	5C	0	2,3
5	AGC Gain	01	0	2,3
6	Equalizer Input	40	1	0,1,2,3
7	Equalizer Tap Coefficients	01-20	1	0,1,2,3
8	Unrotated Equalizer Output	61	1	0,1,2,3
9	Rotated Equalizer Output (Received Point—Eye Pattern)	22	1	0,1,2,3
10	Decision Points (Ideal)	62	1	0,1,2,3
11	Error Vector	63	1	0,1,2,3
12	Rotation Angle	00	1	0,1
13	Frequency Correction	A8	1	2,3
14	Eye Quality Monitor (EQM)	AB	1	,2,3
15	G2 Baseband Signal	C8	1	2,3
16	G2 AGC Gain	AD	1	2,3
17	G2 AGC Slew Rate	AA	1	2,3
18	G2 PLL Frequency Correction	C2	1	2,3
19	G2 PLL Slew Rate	F0	1	,2,3
20	G2 Black/White Threshold	2A	1	0,1
21	G2 Phase Limit*	F2	1	2,3

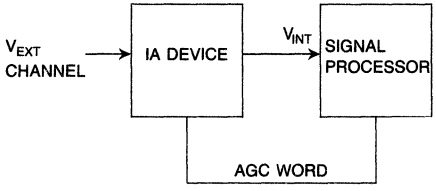
*Added in R5301-20

Diagnostic Data Scaling

Node 1

Parameter/Scaling

Received Signal Samples = A/D Sample Word (signed 16 bits, twos complement)



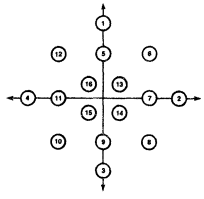
$$V_{INT} = \frac{(\text{A/D Sample Word})_{16}}{40_{16}} \times \frac{3}{256} \text{ Volts}$$

$$V_{EXT} = V_{INT} \div LOG_{10}^{-1}\left[\frac{\text{AGC Gain (dB)}}{20}\right]$$

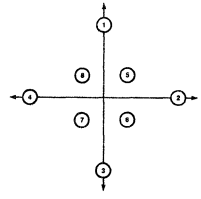
Nodes 2, 3, 6, 8, 9, 10

All Baseband Signal Nodes (32 bits, complex, twos complement)

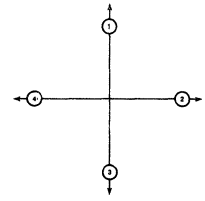
Point	Configuration			
	V.29/9600 x , y	**V.29/7200** x , y	**V.29/4800 & V.27/2400** x , y	**V.27/4800** x , y
1	0000, 2800	0000, 2400	0000, 1C00	0000, 1C00
2	2800, 0000	2400, 0000	1C00, 0000	1400, 1400
3	0000, D800	0000, DC00	0000, E400	1C00, 0000
4	D800, 0000	DC00, 0000	E400, 0000	1400, EC00
5	0000, 1800	0C00, 0C00		0000, E400
6	1800, 1800	0C00, F400		EC00, EC00
7	1800, 0000	F400, F400		E400, 0000
8	1800, E800	F400, 0C00		EC00, 1400
9	0000, E800			
10	E800, E800			
11	E800, 0000			
12	E800, 1800			
13	0800, 0800			
14	0800, F800			
15	F800, F800			
16	F800, 0800			



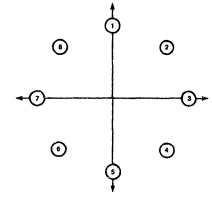
V.29/9600 BPS



V.29/7200 BPS



V.29/4800 BPS and V.27/2400 BPS



V.27/4800 BPS

Node 4

Average Power (16 bits, unsigned)

Typical value: 0889_{16} (corresponding to 0 dBm)

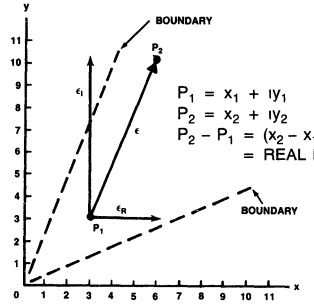
$$\text{Post-AGC Average Power in dBm} = 10 \text{ Log } \frac{(\text{Average Power Word})_{16}}{889_{16}}$$

Pre-AGC Average Power in dBm = Post-AGC Avg. Power in dBm – AGC gain in dB

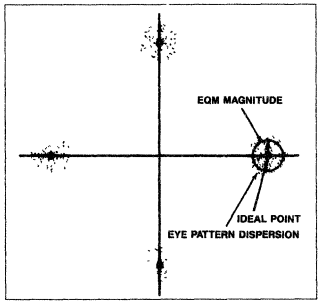
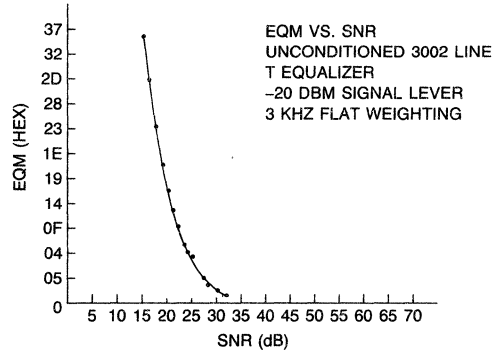
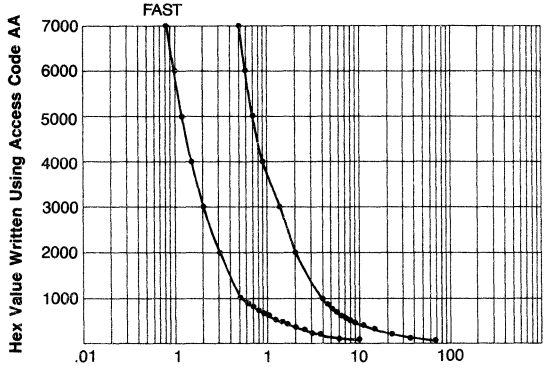
Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
5	**AGC Gain (16 bits, unsigned)** Range $0FC0_{16}$ to $7FFF_{16}$ for LRTH = 0 (– 43 dBm Threshold) 0640_{16} to $7FFF_{16}$ for LRTH = 1 (– 47 dBm Threshold) $\text{AGC Gain in dB} = 50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0\ 098$
7	**Equalizer Taps (32 bits, complex, twos complement)** Node 7 is not a single point but is actually a set of RAM locations containing adaptive equalizer tap coefficients In V.29 configuration, access codes 01 through 20 hexadecimal represent 32 complex taps. In V.27 configuration, access codes 01 through 10 hexadecimal represent 16 complex taps, since the equalizer for V 27 is only half as long as the equalizer for V.29 The equalizer tap access codes can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. Since the equalizer tap coefficients are complex numbers they require two write operations per tap, one for the real part and one for the imaginary part. When writing the real part, the access codes 01 through 20 must be changed to 81 through A0. When writing the imaginary part, or when reading the complex number, the access codes 01 through 20 are correct. Registers 1:1 and 1:0 hold the most and least significant bytes, respectively, of the 16 bits during a write operation.
11	**Error Vector (32 bits, complex, twos complement)** Represents the difference between the received point (P2) and the nearest ideal point (P1). **Error Vector Maximum Values** $P_1 = x_1 + iy_1$ $P_2 = x_2 + iy_2$ $P_2 - P_1 = (x_2 - x_1) + i(y_2 - y_1)$ = REAL ERROR + IMAGINARY ERROR
12	**Rotation Angle (16 bits, twos complement)** Represents instantaneous correction for phase and frequency errors. $\text{Rotation Angle in degrees} = \frac{(\text{Rot. Angle Word})_{16}}{10000_{16}} \times 180$

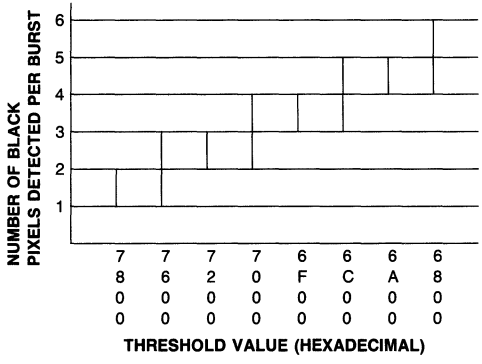
Configuration	Bit Rate (BPS)	Registers 3 and 2 Real Error	Registers 1 and 0 Imag. Error	Magnitude $\sqrt{Re^2 + Im^2}$
V.29	9600	$<0C00_{16}$	$<0C00_{16}$	$<0E66_{16}$
V.29	7200	$<2400_{16}$	$<2400_{16}$	$<1AD4_{16}$
V.29	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	2400	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$



Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
13	**Frequency Correction (16 bits, twos complement)** Represents component of rotation angle caused by frequency error. Range: $FC00_{16}$ to 0400_{16} representing ±37.5 Hz Freq. Correction in Hz = $\frac{(\text{Freq. Correction Word})_{16}}{10000_{16}} \times$ Baud Rate in Hz
14	**Eye Quality Monitor, EQM (16 bits, unsigned)** Equals the filtered squared magnitude of the error vector. Proportionality to bit error rate is determined by particular application. Stabilizes in approximately 700 baud times from $\overline{\text{RLSD}}$ going active.  **Relationship of EQM to Eye Pattern**  **Typical Eye-Quality Versus Signal-to-Noise Ratio for V.29/9600**
15	***Group 2 Baseband Signal (16 bits, unsigned)** Range: 0000_{16} to 0600_{16} represents black 1000_{16} to 2100_{16} represents white
16	***Group 2 AGC Gain (16 bits, unsigned)** (AGC Gain in dB = $50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0.098$
17	***Group 2 AGC Slew Rate** Can be adjusted by the host. Range: 0000_{16} to $7FFF_{16}$  **Seconds to Stabilize AGC for -55 DBM to 0 DBM Step**

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
18	***Group 2 PLL Frequency Correction (16 bits, twos complement)** Range: $FC6A_{16}$ to 0346_{16} representing ±140 Hz Frequency correction in Hz = Frequency correction number (0 167)
19	***Group 2 PLL Slew Rate** Represents gain of first order term in phase locked loop. Range: 0010_{16} to 7000_{16} for stable operation Directly proportional to PLL slew rate
20	***Group 2 Black/White Threshold (16 bits, unsigned)** Default value: $(7800)_{16}$  **NOTE:** **1. 100 WHITE PIXELS SENT FOLLOWED BY 4 BLACK PIXELS SENT.** **2. RESULTS OBTAINED AT 0 DBM, NO COMPROMISE EQUALIZERS IN BACK TO BACK CONNECTION.**
21	***Group 2 Phase Limit (16 bits, twos complement)** When phase error exceeds this limit, PLL updating is suspended. Default: 5000_{16} representing ±67.5 degrees Phase limit = $180° - \left[\frac{(\text{Phase Limit})_{16}}{7FFF_{16}} \times 180° \right]$. Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits, etc.
	*See Rockwell Application Note, R96F Modem Recommended Receive Sequence for Group 2 Facsimile (Order No. 655, Rev. 3).

Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	—	—	—	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	—	—	EPT	SQEXT	T2	LRTH
4	CONFIGURATION							
3	RAM DATA XSM; FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL; TRANSCEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only).

Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	—	—	—	—	IE1	—	MDA1
D	—	TLE	RLE	J3L	—	—	FRT*	RAMW
C	—	—	—	—	—	—	—	G2FGC
B	FR3	FR2	FR1	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{FED}$	—	—	—	—	—	—
4	—	—	—	—	—	$\overline{P2DET}$	—	—
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only).
* = Added in 5301-20.

Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
$\overline{\text{CDET}}$	Carrier Detector	1:7:0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present. $\overline{\text{CDET}}$ goes to zero at the start of the data state, and returns to one at the end of the received signal $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
(None)	Configuration	0:4 0–7	The host processor configures the modem by writing a control code into the configuration register in the interface memory space (See SETUP) ***Configuration Control Codes*** Control codes for the five available modem configurations are: **Configuration** — **Configuration Code (HEX)** V.29 9600 — 14 V.29 7200 — 12 V.29 4800 — 11 V 27 4800 — 0A V.27 2400 — 09 FSK — 20 Group 2 — 40 Tone Transmit — 80 ***Configuration Definitions*** Definitions for the five available modem configurations are: 1. *V.29.* When any of the V.29 configurations has been selected, the modem operates as specified in CCITT Recommendation V.29. 2. *V.27.* When any of the V.27 configurations has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 3. *FSK.* The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system. 4. *Group 2.* The modem operates as a CCITT T.3 compatible AM modem. This configuration permits transmission to and reception from Group 2 facsimile apparatus. A carrier frequency of 2100 Hz is used. A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black. When in the receive state, the modem recovers the carrier of the remote transmitting modem to perform a coherent demodulation of the incoming signal This technique allows a baseband of 3400 Hz to be recovered. The recovered baseband signal is available on the microprocessor bus. The baseband signal is converted to black or white by comparing the received signal level with a preset threshold number. This number may be changed by the user Receiver data is presented to the RXD output at a rate of 10368 samples per second. The user should strobe the data on the rising edge of the data clock (DCLK). A logical 1 level (high voltage) represents white. A logical 0 level (low voltage) represents black. 5. *Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2) The least significant bit represents 0.146486 Hz ± 0.01%. The frequency generated is: f = 0 146486 (256 FREQM + FREQL) Hz ± 0.01%.
EPT	Echo Protector Tone	0:5·3	If EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. This option is available in both the V.27 and V.29 configurations, although it is not specified in the CCITT V.29 Recommendation.
$\overline{\text{FED}}$	Fast Energy Detector	1.5·6	The zero state of $\overline{\text{FED}}$ indicates energy is present above the receiver threshold in the passband $\overline{\text{FED}}$ is not used for Group 2 facsimile.

3

Interface Memory Definitions (continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>(None)</td><td>FREQL/FREQM</td><td>0:2:0-7,
0:3:0-7</td><td>The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below.

FREQM Register (0:3)

<table>
<tr><td>Bit:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Data Word:</td><td>2^{15}</td><td>2^{14}</td><td>2^{13}</td><td>2^{12}</td><td>2^{11}</td><td>2^{10}</td><td>2^{9}</td><td>2^{8}</td></tr>
</table>

FREQL Register (0:2)

<table>
<tr><td>Bit:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Data Word:</td><td>2^{7}</td><td>2^{6}</td><td>2^{5}</td><td>2^{4}</td><td>2^{3}</td><td>2^{2}</td><td>2^{1}</td><td>2^{0}</td></tr>
</table>

The frequency number (N) determines the frequency (F) as follows:
F = (0.146486) (N) Hz ±0.01%.

Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given below:

<table>
<tr><th>Frequency (Hz)</th><th>FREQM</th><th>FREQL</th></tr>
<tr><td>462</td><td>0C</td><td>52</td></tr>
<tr><td>1100</td><td>1D</td><td>55</td></tr>
<tr><td>1650</td><td>2C</td><td>00</td></tr>
<tr><td>1850</td><td>31</td><td>55</td></tr>
<tr><td>2100</td><td>38</td><td>00</td></tr>
</table>
</td></tr>
<tr><td>FRT</td><td>Freeze Taps</td><td></td><td>When FRT is a one, adaptive equalization taps are prevented from changing.</td></tr>
<tr><td>FR1 – FR3</td><td>Frequency 1,2,3</td><td>1:B:5,6,7</td><td>The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for FSK. The default frequencies for FR1, FR2 and FR3 are:

<table>
<tr><th>Bit</th><th>Frequency (Hz)</th></tr>
<tr><td>FR1</td><td>2100</td></tr>
<tr><td>FR2</td><td>1100</td></tr>
<tr><td>FR3</td><td>462</td></tr>
</table>
</td></tr>
<tr><td>G2FGC</td><td>Group 2 Fast Gain Control</td><td>1:C:0</td><td>The one state of G2FGC selects a fast AGC rate (8.6 times standard) in Group 2 Facsimile.</td></tr>
<tr><td>IA1</td><td>Interrupt Active (One)</td><td>1:E:7</td><td>IA1 is a one when Chip 1 is driving $\overline{IRQ}$ to zero volts.</td></tr>
<tr><td>IA0</td><td>Interrupt Active (Zero)</td><td>0:E:7</td><td>IA0 is a one when Chip 0 is driving $\overline{IRQ}$ to zero volts.</td></tr>
<tr><td>IE0</td><td>Interrupt Enable (Zero)</td><td>0:E:2</td><td>The one state of IE0 causes the $\overline{IRQ}$ output to be low when the DA0 bit is a one.</td></tr>
<tr><td>IE1</td><td>Interrupt Enable (One)</td><td>1:E:2</td><td>The one state of IE1 causes the $\overline{IRQ}$ output to be low when the DA1 bit is a one.</td></tr>
<tr><td>J3L</td><td>Japanese 3 Link</td><td>1:D:4</td><td>The one state of J3L selects this standard for link amplitude equalizer. The zero state of J3L selects U.S. survey long.</td></tr>
<tr><td>LRTH</td><td>Lower Receive Threshold</td><td>0:5:0</td><td>The one state of LRTH lowers the receiver turn-on threshold from –43 dBm to –47 dBm. (See SETUP)</td></tr>
<tr><td>MDA0</td><td>Modem Data Available (Zero)</td><td>0:E:0</td><td>MDA0 goes to one when the modem reads or writes register 0:0. MDA0 goes to zero when the host processor reads or writes register 0:0. MDA0 is used for parallel mode as well as for diagnostic data retrieval.</td></tr>
<tr><td>MDA1</td><td>Modem Data Available (One)</td><td>1:E:0</td><td>MDA1 goes to one when the modem writes register 1:0. MDA1 goes to zero when the host processor reads register 1:0.</td></tr>
<tr><td>PDM</td><td>Parallel Data Mode</td><td>0:F:7</td><td>The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.</td></tr>
</table>

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
$\overline{\text{PNDET}}$	Period 'N' Detector	1:7:6	The zero state of $\overline{\text{PNDET}}$ indicates a PN sequence has been detected. $\overline{\text{PNDET}}$ sets to a one at the end of the PN sequence.
$\overline{\text{P2DET}}$	Period '2' Detector	1:4:2	The zero state of $\overline{\text{P2DET}}$ indicates a P2 sequence has been detected. $\overline{\text{P2DET}}$ sets to a one at the start of the PN sequence.
(None)	RAM Access B	1:F:0 – 7	Contains the RAM access code used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Access S	0:F:0 – 6	Contains the RAM access code used in reading RAM locations in Chip 0 (sample rate device)
(None)	RAM Data XBL	1:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XBM	1:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XSL	0:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XSM	0:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data YBL	1:0:0 – 7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device). See DA1.
(None)	RAM Data YBM	1:1:0 – 7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Data YSL	0:0:0 – 7	Least significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device). Shared by parallel data mode for presenting channel data to the host microprocessor bus. See Transceiver Data and DA0.
(None)	RAM Data YSM	0:1:0 – 7	Most significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device).
RAMW	RAM Write Chip 1 (baud rate device)	1:D:0	RAMW is set to a one by the host processor when performing diagnostic writes to the baud rate device (Chip 1) RAMW is set to a zero by the host when reading RAM diagnostic data from Chip 1.
RLE	Receiver Link Equalizer	1:D:5	The one state of RLE enables the link amplitude equalizer in the receiver.
RTS	Request-to-Send	0:5:7	The one state of RTS begins a transmit sequence. The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed RTS parallels the operation of the hardware $\overline{\text{RTS}}$ control input. These inputs are "ORed" by the modem.
SETUP	Setup	0:E:3	The one state of SETUP causes the modem to reconfigure to the control word in the configuration register, and to assume the options specified for equalizer (0:5:1) and threshold (0:5:0). SETUP returns to zero when acted on by the modem. The time required for the SETUP bit to cause a change depends on the current state of the modem. The following table lists worst case delays.
SQEXT	Squelch Extend	0:5:2	The one state of SQEXT inhibits reception of signals for 130 ms after the turn-off sequence.
TDIS	Training Disable	0:5:6	If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one prior to $\overline{\text{RTS}}$ going on, the generation of a training sequence is prevented at the start of transmission.
TLE	Transmitter Link Equalizer	1:D:6	The one state of TLE enables the link amplitude equalizer in the transmitter.

Current State	V.21	G2	High Speed Receiver	High Speed Transmitter
DELAY	14 ms	400 μs	2 BAUD	2 BAUD + TURNOFF Sequence + Training (if applicable) + SQUELCH (if applicable)

Interface Memory Definitions (continued)

Mnemonic	Name	Memory Location	Description
(None)	Transceiver Data	0:0:0–7	In receive parallel data mode, the modem presents eight bits of channel data in register 0:0 for reading by the host microprocessor. After the eight bits have been accumulated in register 0:C they are transferred to 0:0 and bit 0:E:0 goes to a one. When the host reads 0:0, bit 0:E:0 resets to a zero. The first bit of received data is not necessarily located in bit 0:0:0. The host must frame the received data by searching for message sync characters. Bit 0:E:0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations. In transmit parallel data mode the host stores data at location 0:0. This action causes bit 0:E:0 to reset to a 0. When the modem transfers the data from 0:0 to 0:2 bit 0:E:0 sets to a 1. The data is serially transmitted from register 0:2 least significant bit first. Received data is shifted into register 0:C from MSB toward LSB.
T2	T/2 Equalizer Select	0:5:1	If T2 is a one, an adaptive equalizer with two taps per baud is used. If T2 is a zero, an adaptive equalizer with one tap per baud is used. The number of taps remains the same for both cases. (See SETUP)

PERFORMANCE

Whether functioning in V.27 ter or V.29 configuration, the modem provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of –20 dBm as illustrated.

TYPICAL PHASE JITTER

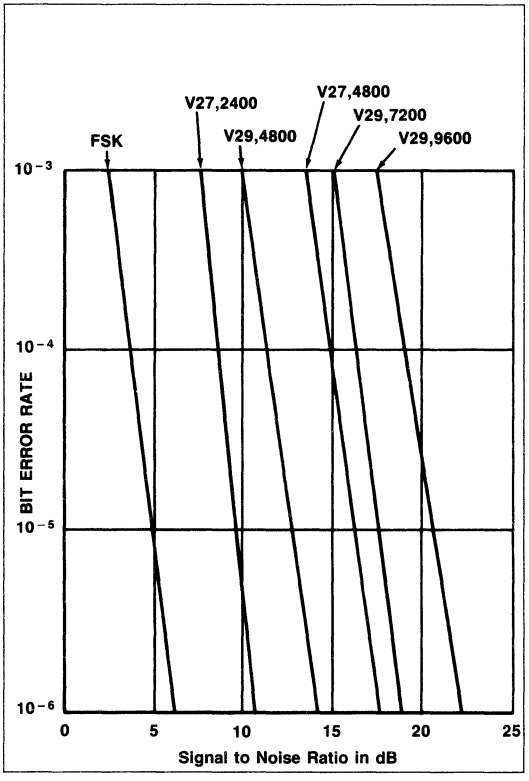
At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

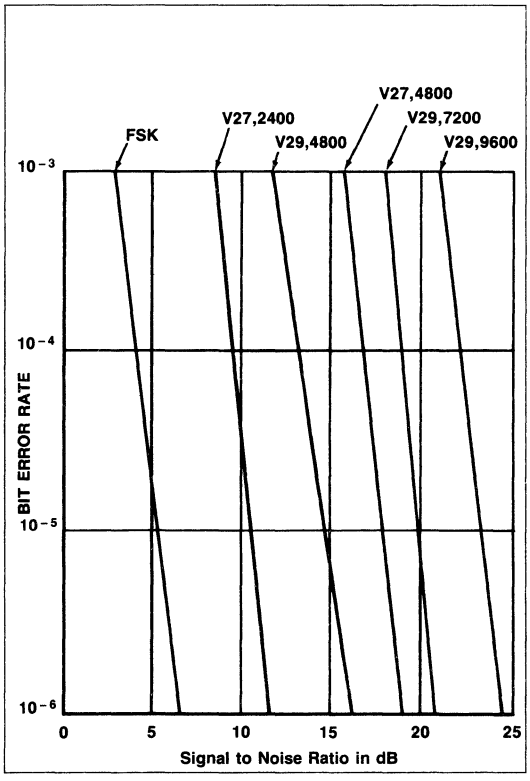
At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

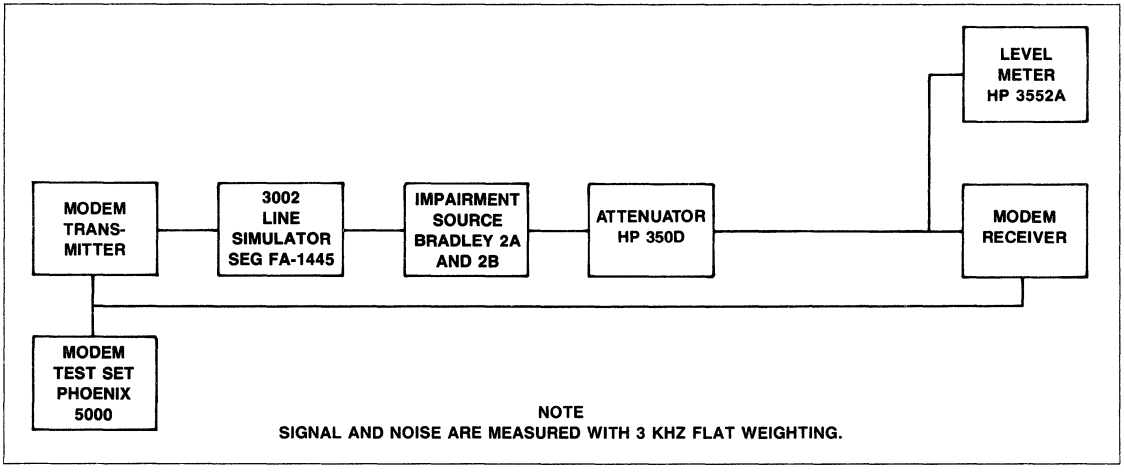
An example of the BER performance capabilities is given in the following diagrams:



Typical Bit Error Rate
(Back-to-Back, T Equalizer, Level −20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, T Equalizer Level −20 dBm)



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	400 mA	<500 mA
+12 Vdc	±5%	5 mA	< 10 mA
−12 Vdc	±5%	30 mA	< 50 mA

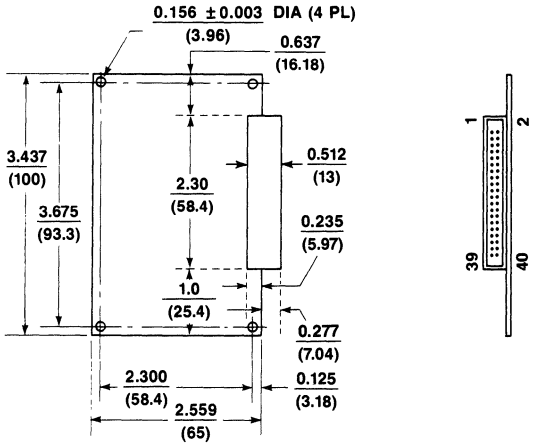
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Environmental

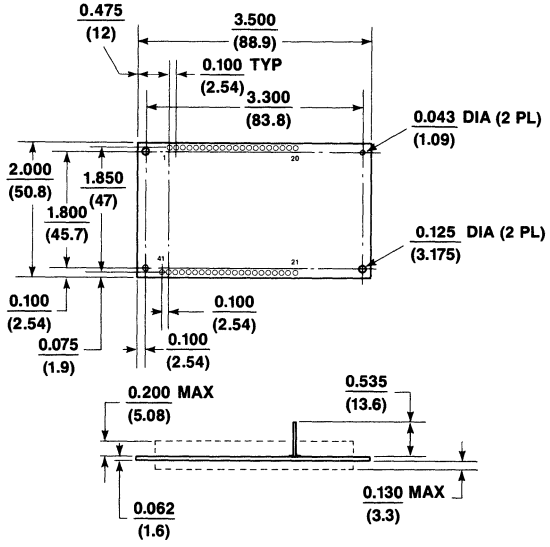
Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical

Parameter	Specification
DIP Connector Version	
Board Structure	Single PC board with a row of 20 pins and a row of 21 pins in a dual in-line pin configuration. Match with Berg 65780 or equivalent.
Dimensions	
Width	2.0 in. (50.8 mm)
Length	3.5 in. (88.9 mm)
Component Height	0.2 in. (5.08 mm) above, 0.13 in. (3.30 mm) below.
Weight (max.)	2.6 oz. (73 g)
Pins	
Length (max.)	0.535 in. (13.6 mm) above.
Thickness	0.025 in. (0.64 mm) square
Ribbon Connector Version	
Board Structure	Single PC board with single right angle header with 40 pins. Burndy FRS 40BS8P or equivalent mating connector.
Dimensions	
Width	3.94 in. (100 mm)
Length	2.56 in. (65 mm)
Height	0.40 in. (10.2 mm)
Weight (max.)	2.6 oz. (73 g)
Lead Extrusion (max.)	0.100 in. (2.54 mm)



RIBBON CONNECTOR VERSION



DIP CONNECTOR VERSION

R96F Dimensions and Pin Locations

R96MD
9600 bps Facsimile Modem

INTRODUCTION

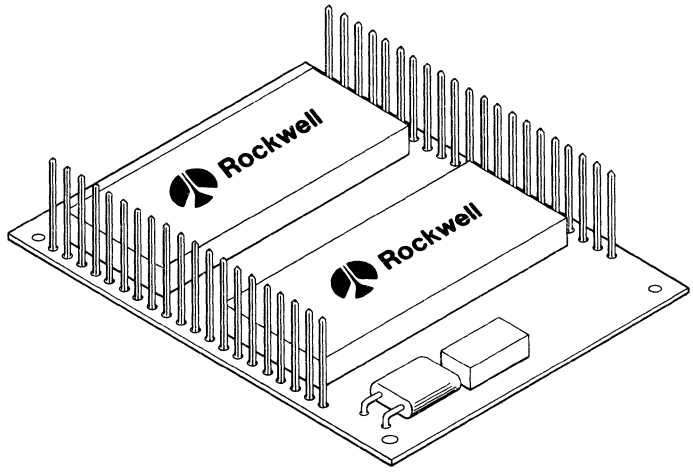
The Rockwell R96MD is a synchronous 9600 bits per second (bps) modem. It is designed for operation over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29, V.27 ter, T.30, T.4 and T.3. The R96MD can operate at speeds of 9600, 7200, 4800, 2400 and 300 bps. Employing advanced signal processing techniques, the R96MD can transmit and receive data even under extremely poor line conditions.

The R96MD is designed for use in Group 3 facsimile machines and is also compatible with Group 2 machines. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, serial/parallel host interface, and dual in-line pin (DIP) interface simplify system design and allow direct installation on the host module.

FEATURES

- Compatible with:
  - — CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4, T.3
- Group 3 and Group 2 Facsimile
- Half-Duplex (2-Wire)
- Programmable Tone Detection
- Programmable Dual/Single Tone Generation
- Dynamic Range: −47 dBm to 0 dBm
- Programmable Transmit Levels
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Small Size: 50.8 mm × 65.4 mm (2.0 in. × 2.575 in.)
- Low Power Consumption: 2 W (Typical)
- Transmit Output Level: +5 dBm ±1 dB
- TTL and CMOS Compatible



R96MD Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

T.30 Tonal Signaling Frequencies

Function	Frequency (Hz ±0.01%)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group 2 Identification (C12)	1850
Group 2 Command (GC2)	2100
Group 2 Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462

Carrier Frequencies

Function	Frequency (Hz ±0.01%)
T.3 Carrier (Group 2)	2100
V.27 ter Carrier	1800
V.29 Carrier	1700

TONE GENERATION

Under control of the host processor, the modem can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

TONE DETECTION

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Specification	Baud Rate (Symbols/Sec.)	Bits Per Baud	Data Rate (BPS) (±0.01%)	Symbol Points
V 29	2400	4	9600	16
V 29	2400	3	7200	8
V.27	1600	3	4800	8
V.27	1200	2	2400	4

DATA ENCODING

The modem data encoding conforms to CCITT recommendations V.29 and V.27 ter.

EQUALIZERS

The modem provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for V.27 and V.29 configurations. The equalizer can be configured as either a T or a T/2 equalizer.

TRANSMITTED DATA SPECTRUM

The transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The modem incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter or V.29 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the modem can adapt to received frequency error of up to ±10 Hz with less than a 0.2 dB degradation in BER performance. Group 2 carrier recovery capture range is 2100 ±30 Hz. The Group 2 receiver operates properly when the carrier is varied by ±16 Hz at a 0.1 Hz per second rate.

RECEIVE LEVEL

The modem receiver circuit satisfies all specified performance requirements for received line signal levels from 0 dBm to −43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the modem provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level defaults to +5 dBm ±1 dB at power on. When using the default transmit level and driving a 600 ohm load, the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load. The output level can be programmed over a 10 dB range by performing a RAM write operation.

TRANSMIT TIMING

In the transmit state, the modem provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 9600, 7200, 4800, 2400, or 300 Hz (±0.01%). In Group 2, DCLK tracks an external 10368 Hz clock. If the external clock input (XCLK) is grounded the Group 2 DCLK is 10372.7 Hz ±0.01%.
2. *Duty Cycle.* 50 ±1%

Transmit Data (TXD) must be stable during the 1 microsecond period immediately preceding and the 1 microsecond period immediately following the rising edge of DCLK.

TURN-ON SEQUENCE

A total of ten selectable turn-on sequences can be generated by the modem, as defined in the following table:

Turn-On Sequences

Specification	$\overline{RTS}$-$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.29 V.27 4800 bps V.27 2400 bps	253 ms 708 ms 943 ms	438 ms 913 ms 1148 ms
V.21 300 bps Group 2	≤14 ms ≤400 μs	≤14 ms ≤400 μs

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled ones followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{RTS}$ goes false. In Group 2 the transmitter turns off within 200 μs after $\overline{RTS}$ goes false.

CLAMPING

The following clamps are provided with the modem:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector (RLSD).* $\overline{RLSD}$ is clamped off (squelched) during the time when $\overline{RTS}$ is on.
3. *Extended Squelch.* Optionally, $\overline{RLSD}$ remains clamped off for 130 ms after the turn-off sequence.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the length of the training sequence. Response time is 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps. In V.21 $\overline{CTS}$ turns on in 14 ms or less. In Group 2 $\overline{CTS}$ turns on in 400 μs or less.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

For either V.27 ter or V.29, $\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RLSD}$ off-to-on response time is 15 ±10 ms. The $\overline{RLSD}$ on-to-off response time for V.27 is 10 ±5 ms and for V.29 is 30 ±9 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD.

Two threshold options are provided:

1. Greater than −43 dBm ($\overline{RLSD}$ on)
   Less than −48 dBm ($\overline{RLSD}$ off)
2. Greater than −47 dBm ($\overline{RLSD}$ on)
   Less than −52 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The modem operates in either a serial or a parallel mode.

SERIAL MODE

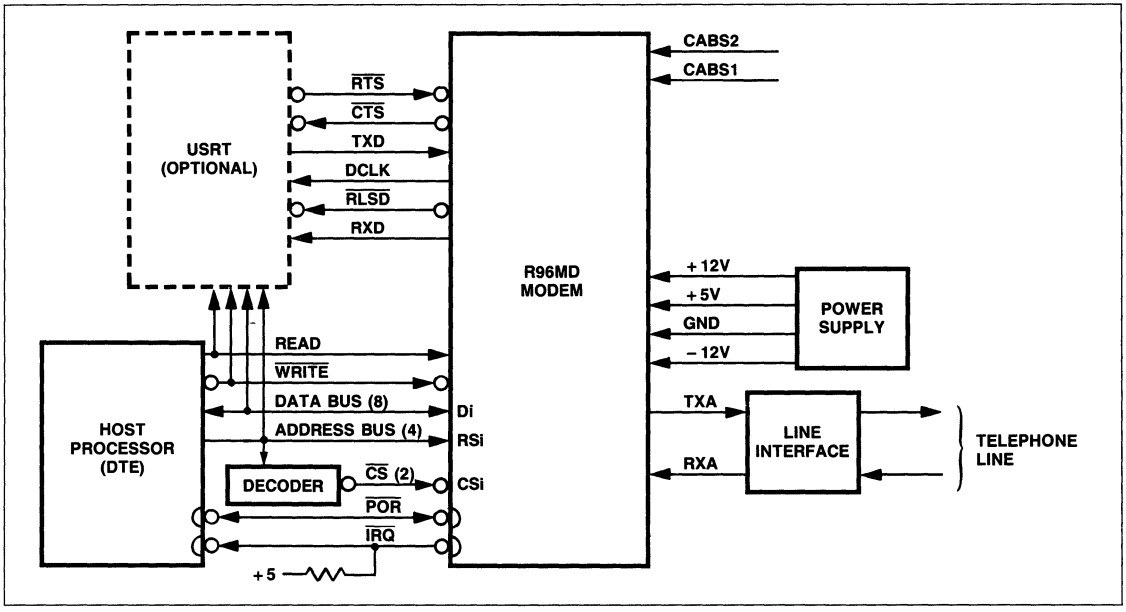
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the Modem Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The modem can transfer channel data eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the modem is configured by the host processor via the microprocessor bus.



Modem Functional Interconnect Diagram

INTERFACE CHARACTERISTICS

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in a 40-pin dual in-line pin (DIP) connector. Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the Modem Hardware Circuits table; the table column titled 'Type' refers to designations found in the Digital or Analog Interface Characteristics.

Microprocessor Interface

Sixteen hardware circuits provide address (RS0–RS3), data (D0–D7), control ($\overline{CS}$, READ and $\overline{WRITE}$) and interrupt ($\overline{IRQ}$) signals for implementing a parallel interface compatible with an 8080 microprocessor. (Refer to the Microprocessor Interface Timing Waveforms figure and Microprocessor Interface Timing Requirements table.) With the addition of a few external logic gates, the interface can be made compatible with a wide variety of microprocessors such as 6500, 6800, or 68000.

The microprocessor interface allows a host microprocessor to change modem configuration, read or write channel data as well as diagnostic data, and supervise modem operation by means of software strappable control bits and modem status bits. The significance of the control and status bits and methods of data interchange are discussed in the Software Circuits section.

V.24 Interface

Seven hardware circuits provide timing, data and control signals for implementing a serial interface compatible with CCITT Recommendation V.24. These signals interface directly with circuits using TTL logic levels (0, +5 volt). These TTL levels are suitable for driving the short wire lengths or printed circuitry normally found within stand-alone modem enclosures or equipment cabinets.

In applications where the modem is operated in parallel data mode only (i.e., where the V.24 signals are unused), all V.24 pins may remain unterminated.

Cable Equalizers

Modems may be connected by direct wiring, such as leased telephone cable or through the public switched telephone network, by means of a data access arrangement. In either case, the modem analog signal is carried by copper wire cabling for at least some part of its route. The cable characteristics shape the passband response so that the lower frequencies of the passband (300 Hz to 1700 Hz) are attenuated less than the higher frequencies (1700 Hz to 3300 Hz). The longer the cable the more pronounced the effect.

To minimize the impact of this undesired passband shaping, a compromise equalizer with more attenuation at lower frequencies than at higher frequencies can be placed in series with the analog signal. The modem includes three such equalizers designed to compensate for cable distortion.

Cable Equalizer Selection

CABS2	CABS1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Analog Signals

Two analog signals, TXA and RXA, provide the interface point for telephone company audio circuits.

The TXA line is an output suitable for driving an audio transformer or data access arrangement for connection to either leased lines or the PSTN. The output structure of TXA is a low impedance amplifier in series with an internal 604 ohm ±1% resistor to match a standard telephone load of 600 ohms.

RXA is an input to the receiver from an audio transformer or data access arrangement. The input impedance is nominally 60K ohms but a factory select resistor allows a variance of 23%. The RXA input must be shunted by an external resistor in order to match a 600 ohm source. A 604 ohm ±1% resistor is satisfactory.

Some form of transient protection for TXA and RXA is recommended when operating directly into a transformer. This protection may be back-to-back zener diodes across the transformer or a varistor across the transformer.

Overhead

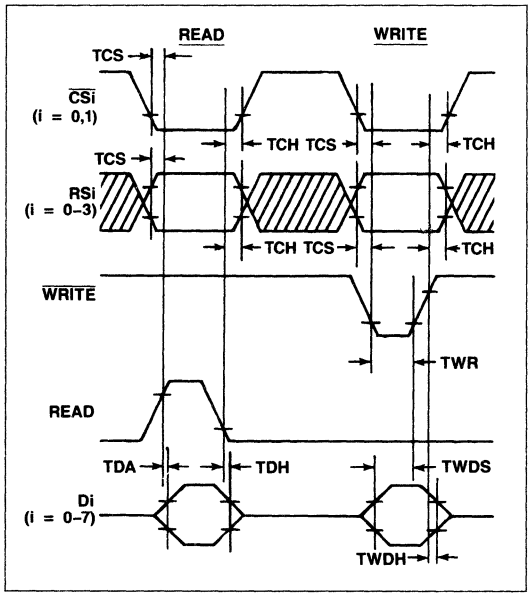
Except for the power-on-reset signal $\overline{POR}$, the overhead signals are dc power or ground points. When the modem is initially energized a signal called Power-On-Reset ($\overline{POR}$) causes the modem to assume a valid operational state. The modem drives pin 39 to ground during the beginning of the POR sequence. Approximately 10 ms after the low to high transition of pin 39, the modem is ready for normal use. The POR sequence is reinitiated anytime the +5V supply drops below +3.5V for more than 30 ms, or an external device drives pin 39 low for at least 3 μs. When an external low input is applied to pin 39, the modem is ready for normal use approximately 10 ms after the low input is removed. Pin 39 is not driven low by the modem when the POR sequence is initiated externally. In all cases, the POR sequence requires 50 ms to 350 ms to complete. The POR sequence leaves the modem configures as follows:

- V.29/9600 bps
- T/2 equalizer
- Serial mode
- Training enabled
- Echo protector tone enabled
- No extended squelch
- Higher receive threshold
- Interrupts disabled
- RAM Access S=00
- RAM Access B=22

This configuration is suitable for performing high speed data transfer on the PSTN with the serial data port selected as the input and output point for data terminal equipment (DTE).

Modem Hardware Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground	GND	17,18	Power Supply Return
+5 volts	PWR	33,34	+5 volt supply
+12 volts	PWR	21	+12 volt supply
−12 volts	PWR	19	−12 volt supply
$\overline{POR}$	I/OB	39	Power-on-reset
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	9	Data Bus (8 Bits)
D6	I/OA	8	
D5	I/OA	2	
D4	I/OA	3	
D3	I/OA	4	
D2	I/OA	5	
D1	I/OA	6	
D0	I/OA	7	
RS3	IA	13	Register Select (4 Bits) Select Reg. 0−F
RS2	IA	14	
RS1	IA	15	
RS0	IA	16	
$\overline{CS0}$	IA	11	Chip Select Sample Rate Device
$\overline{CS1}$	IA	38	Chip Select Baud Rate Device
$\overline{READ}$	IA	10	Read Enable
$\overline{WRITE}$	IA	12	Write Enable
$\overline{IRQ}$	OB	1	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	30	Data Clock
XCLK	IB	31	External Clock for Group 2
$\overline{RTS}$	IB	32	Request-to-Send
$\overline{CTS}$	OC	28	Clear-to-Send
TXD	IB	27	Transmitter Data
RXD	OC	26	Receiver Data
$\overline{RLSD}$	OC	29	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IB	24	Cable Select 1
CABS2	IB	25	Cable Select 2
E. ANALOG SIGNALS			
TXA	AA	23	Transmitter Analog Output
RXA	AB	22	Receiver Analog Input
Pin 35 is removed for keying connector.			



Microprocessor Interface Timing Diagram

Microprocessor Interface Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{CS}$i, RSi setup time prior to Read or $\overline{Write}$	TCS	30	—	ns
Data Access time after Read	TDA	—	140	ns
Data hold time after Read	TDH	10	50	ns
CSi, RSi hold time after Read or $\overline{Write}$	TCH	10	—	ns
Write data setup time	TWDS	75	—	ns
Write data hold time	TWDH	10	—	ns
Write strobe pulse width	TWR	75	—	ns

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 46.4K ohms ±23%.

3

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type						
			IA	IB	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 min	2 0 min.				2 0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V			2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V			0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2 5 max.					±12.5 max.[4]	
I_{OH}	Output Current, High	mA			−0.1 max.				
I_{OL}	Output Current, Low	mA			1.6 max.	1 6 max	1.6 max		
I_L	Output Current, Leakage	μA				±10 max.			
I_{PU}	Pull-up Current (Short Circuit)	μA		−240 max. −10 min.			−240 max. −10 min.		−260 max −100 min.
C_L	Capacitive Load	pF	5	5				10	40
C_D	Capacitive Drive	pF			100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1 6 mA
3. I load = −40 μA
4. V_{IN} = 0 4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

SOFTWARE CIRCUITS

The modem includes two signal processor chips. Each of these chips contains 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Registers in chip 0 update at the modem sample rate (9600 bps). Registers in chip 1 update at the selected baud rate except in Group 2 and FSK configurations when they update at the sample rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Status/Control Bits

Modem operation is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a '—' are reserved for modem use only and must not be changed by the host.

Any one of the registers may be read or written on any host read or write cycle, but all eight bits of that register are affected. In order to read a single bit or a group of bits in a register, the host processor must mask out unwanted data. When writing a single bit or group of bits in a register the host processor must perform a read-modify-write operation. That is, the entire register is read, the necessary bits are set or reset in the accumulator of the host, then the original unmodified bits and the modified bits are written back into the register of the interface memory.

RAM Data Access

The user can access much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register 0:F (RAM ACCESS S) or 1:F (RAM ACCESS B). The RAM Access Codes table lists access codes for storage in registers 0:F or 1:F and the corresponding diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long.

These bits are written into interface memory registers 0:3, 0:2, 0:1 and 0:0, or 1:3, 1:2, 1:1 and 1:0, in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit 0:5:5 (RAMWS) or bit 1:D:0 (RAMWB) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM in chip 0 or in chip 1, respectively. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the most significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAM Access B bits of register 1:F for chip 1, or by means of 0:5:4 (RAE) and 0:F (RAM Access S) for chip 0. When bit 1:F:7 or 0:5:4 is set to one, the XRAM is selected. When 1:F:7 or 0:5:4 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the modem data available bit 0:E:0 or 1:E:0 (MDAi) is reset to zero. When the modem reads or writes register 0, MDAi is set to a one. When set to a one by the host, bit 0:E:2 or 1:E:1 (IEi) enables the MDAi bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit 0:E:7 or 1:E:7 (IAi) goes to a one.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem. This information is scaled as shown in the Diagnostic Data Scaling table.

RAM Access Codes

Node	Function	Access	RAE	Chip	Read Reg. No.
1	Received Signal Samples	40	X	0	2,3
2	Demodulator Output	42	X	0	0,1,2,3
3	Low Pass Filter Output	54	X	0	0,1,2,3
4	Average Power	5C	X	0	2,3
5	AGC Gain	3C	X	0	2,3
6	Tone 1 Frequency	71	1	0	2,3
7	Tone 1 Level	72	1	0	2,3
8	Tone 2 Frequency	71	0	0	0,1
9	Tone 2 Level	72	0	0	0,1
10	Output Level	4C	0	0	0,1
11	Equalizer Input	40	N.A.	1	0,1,2,3
12	Equalizer Tap Coefficients	01-20	N.A.	1	0,1,2,3
13	Unrotated Equalizer Output	61	N.A.	1	0,1,2,3
14	Rotated Equalizer Output (Received Point—Eye Pattern)	22	N.A.	1	0,1,2,3
15	Decision Points (Ideal)	62	N.A.	1	0,1,2,3
16	Error Vector	63	N.A.	1	0,1,2,3
17	Rotation Angle	00	N.A.	1	0,1
18	Frequency Correction	A8	N.A.	1	2,3
19	Eye Quality Monitor (EQM)	AB	N.A.	1	2,3
20	G2 Baseband Signal	C8	N.A.	1	2,3
21	G2 AGC Gain	AD	N.A.	1	2,3
22	G2 AGC Slew Rate	AA	N.A.	1	2,3
23	G2 PLL Frequency Correction	C2	N.A.	1	2,3
24	G2 PLL Slew Rate	F0	N.A.	1	2,3
25	G2 Black/White Threshold	2A	N.A.	1	0,1
26	G2 Phase Limit	F2	N.A.	1	2,3
27	Checksum	2D	N.A.	1	2,3

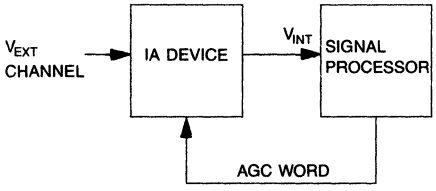
RAE = X is don't care since this location should only be read from, and *not* written to, by the host. N.A. is not applicable since RAE is not used in chip one.

Diagnostic Data Scaling

Node 1

Parameter/Scaling

Received Signal Samples = A/D Sample Word (signed 16 bits, twos complement)



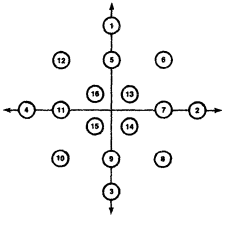
$$V_{INT} = \frac{(\text{A/D Sample Word})_{16}}{(40)_{16}} \times \frac{3}{256} \text{ Volts}$$

$$V_{EXT} = V_{INT} \div LOG_{10}^{-1}\left[\frac{\text{AGC Gain (dB)}}{20}\right]$$

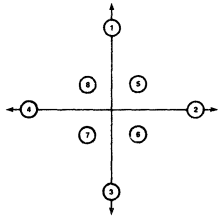
Nodes 2, 3, 11, 13, 14, 15

All Baseband Signal Nodes (32 bits, complex, twos complement)

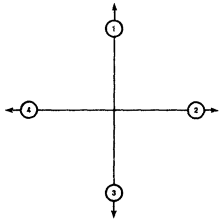
Point	Configuration			
	V.29/9600 x , y	V.29/7200 x , y	V.29/4800 & V.27/2400 x , y	V.27/4800 x , y
1	0000, 2800	0000, 2400	0000, 1F00	0000, 1F00
2	2800, 0000	2400, 0000	1F00, 0000	1600, 1600
3	0000, D800	0000, DC00	0000, E100	1F00, 0000
4	D800, 0000	DC00, 0000	E100, 0000	1600, EA00
5	0000, 1800	0C00, 0C00		0000, E100
6	1800, 1800	0C00, F400		EA00, EA00
7	1800, 0000	F400, F400		E100, 0000
8	1800, E800	F400, 0C00		EA00, 1600
9	0000, E800			
10	E800, E800			
11	E800, 0000			
12	E800, 1800			
13	0800, 0800			
14	0800, F800			
15	F800, F800			
16	F800, 0800			



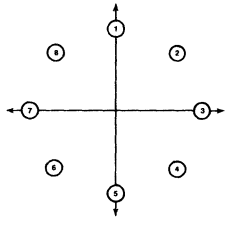
V.29/9600 BPS



V.29/7200 BPS



V.29/4800 BPS and V.27/2400 BPS



V.27/4800 BPS

Node 4

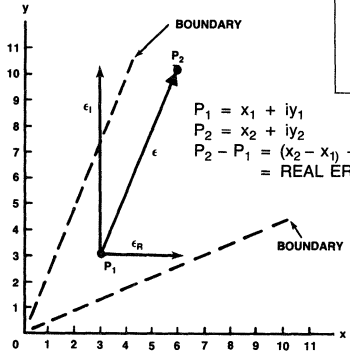
Average Power (16 bits, unsigned)

Typical value: 0889_{16} (corresponding to 0 dBm)

$$\text{Post-AGC Average Power in dBm} = 10 \text{ Log} \frac{(\text{Average Power Word})_{16}}{889_{16}}$$

Pre-AGC Average Power in dBm = Post-AGC Avg. Power in dBm – AGC gain in dB

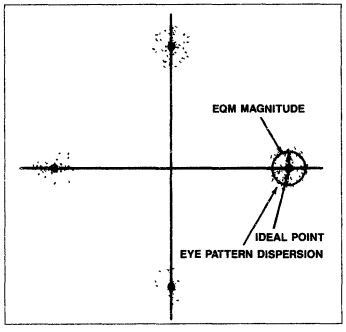
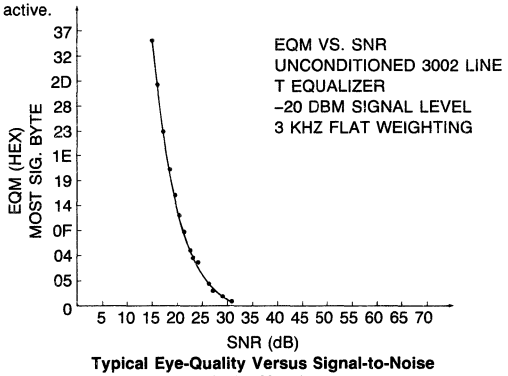
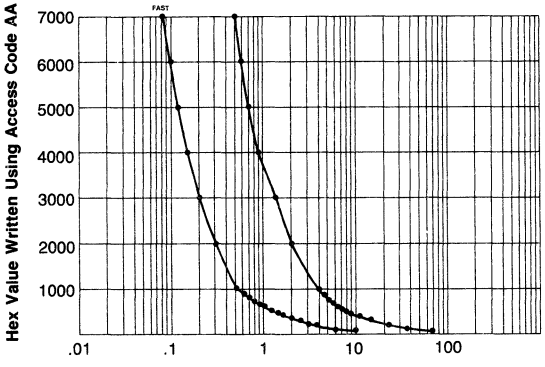
Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
5	**AGC Gain (16 bits, unsigned)** Range: $0FC0_{16}$ to $7FFF_{16}$ for LRTH = 0 (– 43 dBm Threshold) 0640_{16} to $7FFF_{16}$ for LRTH = 1 (– 47 dBm Threshold) $\text{AGC Gain in dB} = 50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0.098$
6, 8	**Tone 1 and 2 Frequency (16 bits, unsigned)** N = 6.8267 (Frequency in Hz) Convert N to hexadecimal then store in RAM.
7, 9	**Tone 1 and Tone 2 Level** Calculate the power of each tone independently by using the equation for Output Number given at node 10. Convert these numbers to hexadecimal then store in RAM. Total power transmitted in tone configuration is the result of both tone 1 power and tone 2 power.
10	**Output Level (16 bits, unsigned)** Output Number = $27573.6\ [10^{(Po/20)}]$ Po = output power in dBm with series 600 ohm resistor into 600 ohm load. Convert Output Number to hexadecimal and store in RAM.
12	**Equalizer Taps (32 bits, complex, twos complement)** Node 12 is not a single point but is actually a set of RAM locations containing adaptive equalizer tap coefficients. In V.29 configuration, access codes 01 through 20 hexadecimal represent 32 complex taps. In V.27 configuration, access codes 01 through 10 hexadecimal represent 16 complex taps, since the equalizer for V.27 is only half as long as the equalizer for V.29. The equalizer tap access codes can be useful for restoring modem operation after loss of equalization without requesting a training sequence from the transmitter. Since the equalizer tap coefficients are complex numbers they require two write operations per tap, one for the real part and one for the imaginary part. When writing the real part, the access codes 01 through 20 must be changed to 81 through A0. When writing the imaginary part, or when reading the complex number, the access codes 01 through 20 are correct. Registers 1:1 and 1:0 hold the most and least significant bytes, respectively, of the 16 bits during a write operation.
16	**Error Vector (32 bits, complex, twos complement)** Represents the difference between the received point (P2) and the nearest ideal point (P1).  $P_1 = x_1 + iy_1$ $P_2 = x_2 + iy_2$ $P_2 - P_1 = (x_2 - x_1) + i(y_2 - y_1)$ = REAL ERROR + IMAGINARY ERROR

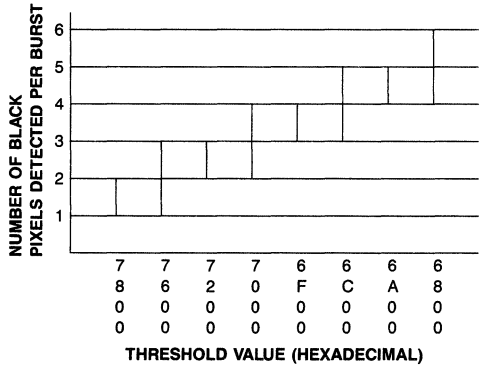
Error Vector Maximum Values

Configuration	Bit Rate (BPS)	Registers 3 and 2 Real Error	Registers 1 and 0 Imag. Error	Magnitude $\sqrt{Re^2 + Im^2}$
V.29	9600	$<0C00_{16}$	$<0C00_{16}$	$<0E66_{16}$
V.29	7200	$<2400_{16}$	$<2400_{16}$	$<1AD4_{16}$
V.29	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	2400	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
17	**Rotation Angle (16 bits, twos complement)** Represents instantaneous correction for phase and frequency errors. Rotation Angle in degrees = $\frac{(\text{Rot Angle Word})_{16}}{10000_{16}} \times 180$
18	**Frequency Correction (16 bits, twos complement)** Represents component of rotation angle caused by frequency error. Range: $FC00_{16}$ to 0400_{16} representing ±37.5 Hz Freq. Correction in Hz = $\frac{(\text{Freq. Correction Word})_{16}}{10000_{16}}$ × Baud Rate in Hz
19	**Eye Quality Monitor, EQM (16 bits, unsigned)** Equals the filtered squared magnitude of the error vector. Proportionality to bit error rate is determined by particular application. Stabilizes in approximately 700 baud times from $\overline{\text{RLSD}}$ going active.  **Relationship of EQM to Eye Pattern**  **Typical Eye-Quality Versus Signal-to-Noise Ratio for V.29/9600**
20	***Group 2 Baseband Signal (16 bits, unsigned)** Range: 0000_{16} to 0600_{16} represents black 1000_{16} to 2100_{16} represents white
21	***Group 2 AGC Gain (16 bits, unsigned)** AGC Gain in dB = $50 - \frac{(\text{AGC Gain Word})_{16}}{40_{16}} \times 0.098$
22	***Group 2 AGC Slew Rate** Can be adjusted by the host. Range: 0000_{16} to $7FFF_{16}$  **Seconds to Stabilize AGC for -55 DBM to 0 DBM Step**

Diagnostic Data Scaling (continued)

Node	Parameter/Scaling
23	***Group 2 PLL Frequency Correction (16 bits, twos complement)** Range: $FC6A_{16}$ to 0346_{16} representing ± 140 Hz Frequency correction in Hz = Frequency correction number (0.167)
24	***Group 2 PLL Slew Rate** Represents gain of first order term in phase locked loop. Range: 0010_{16} to 7000_{16} for stable operation Directly proportional to PLL slew rate
25	***Group 2 Black/White Threshold (16 bits, unsigned)** Default value: $(7800)_{16}$  **NOTE:** **1. 100 WHITE PIXELS SENT FOLLOWED BY 4 BLACK PIXELS SENT.** **2. RESULTS OBTAINED AT 0 DBM, NO COMPROMISE EQUALIZERS IN BACK TO BACK CONNECTION.**
26	***Group 2 Phase Limit (16 bits, twos complement)** When phase error exceeds this limit, PLL updating is suspended. Default: 5000_{16} representing ± 67.5 degrees $\text{Phase limit} = 180° - \left[\frac{(\text{Phase Limit})_{16}}{(7FFF)_{16}} \times 180° \right]$ Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits.
27	**Checksum (16-bit unsigned)** ROM checksum number determined by revision level.
	*See Rockwell Application Note, R96F Modem Recommended Receive Sequence for Group 2 Facsimile (Order No. 655, Rev. 3).

Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	—	—	—	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	RAMWS	RAE	EPT	SQEXT	T2	LRTH
4	CONFIGURATION							
3	RAM DATA XSM; FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL; TRANSCEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only).

Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	—	—	—	—	IE1	—	MDA1
D	—	—	—	—	—	—	FRT	RAMWB
C	—	—	—	—	—	—	—	G2FGC
B	FR3	FR2	FR1	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{FED}$	—	—	—	—	—	—
4	—	—	—	—	—	$\overline{P2DET}$	—	—
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only).

Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
$\overline{\text{CDET}}$	Carrier Detector	1:7:0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present. $\overline{\text{CDET}}$ goes to zero at the start of the data state, and returns to one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$.
(None)	Configuration	0:4:0–7	The host processor configures the modem by writing a control code into the configuration register in the interface memory space. (See SETUP) ***Configuration Control Codes*** Control codes for the eight available modem configurations are: **Configuration** — **Configuration Code (HEX)** V.29 9600* — 14 V.29 7200 — 12 V.27 4800 — 0A V.27 2400 — 09 FSK — 20 Group 2 — 40 Tone Transmit — 80 DTMF Transmit — 81 *Default at POR. ***Configuration Definitions*** 1. *V.29.* When a V.29 configuration has been selected, the modem operates as specified in CCITT Recommendation V.29. 2. *V.27.* When a V.27 configuration has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 3. *FSK.* The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system. 4. *Group 2.* The modem operates as a CCITT T.3 compatible AM modem. This configuration permits transmission to and reception from Group 2 facsimile apparatus. A carrier frequency of 2100 Hz is used. A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black. When in the receive state, the modem recovers the carrier of the remote transmitting modem to perform a coherent demodulation of the incoming signal. This technique allows a baseband of 3400 Hz to be recovered. The recovered baseband signal is available on the microprocessor bus. The baseband signal is converted to black or white by comparing the received signal level with a preset threshold number. This number may be changed by the user. Receiver data is presented to the RXD output at a rate of 10368 samples per second. The user should strobe the data on the rising edge of the data clock (DCLK). A logical 1 level (high voltage) represents white. A logical 0 level (low voltage) represents black. 5. *Tone Transmit.* In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%. 6. *DTMF Transmit.* In this configuration, activating RTS causes the modem to transmit two tones at frequencies and output levels specified by the user. By using the RAM Data Access routines, the user can program the tones and levels.

Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
EPT	Echo Protector Tone	0:5:3	If EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. This option is available in both the V.27 and V.29 configurations, although it is not specified in the CCITT V.29 recommendation.
$\overline{FED}$	Fast Energy Detector	1:5:6	The zero state of $\overline{FED}$ indicates energy is present above the receiver threshold in the passband. $\overline{FED}$ is not used for Group 2 Facsimile.
(None)	FREQL/FREQM	0:2:0-7, 0:3:0-7	The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below. *FREQM Register (0:3)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{15} 2^{14} 2^{13} 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} *FREQL Register (0:2)* Bit: 7 6 5 4 3 2 1 0 Data Word: 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0} The frequency number (N) determines the frequency (F) as follows: F = (0.146486) (N) Hz ±0.01%. Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given below: **Frequency (Hz) / FREQM / FREQL** 462 / 0C / 52 1100 / 1D / 55 1650 / 2C / 00 1850 / 31 / 55 2100 / 38 / 00
FRT	Freeze Taps		When FRT is a one, adaptive equalization taps are prevented from changing.
FR1 – FR3	Frequency 1,2,3	1:B:5,6,7	The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for FSK. The default frequencies for FR1, FR2 and FR3 are: **Bit / Frequency (Hz)** FR1 2100 FR2 1100 FR3 462
G2FGC	Group 2 Fast Gain Control	1:C:0	The one state of G2FGC selects a fast AGC rate (8.6 times standard) in Group 2 Facsimile.
IA1	Interrupt Active (One)	1:E:7	IA1 is a one when Chip 1 is driving $\overline{IRQ}$ to zero volts.
IA0	Interrupt Active (Zero)	0:E:7	IA0 is a one when Chip 0 is driving $\overline{IRQ}$ to zero volts.
IE0	Interrupt Enable (Zero)	0:E:2	The one state of IE0 causes the $\overline{IRQ}$ output to be low when the DA0 bit is a one.
IE1	Interrupt Enable (One)	1:E:2	The one state of IE1 causes the $\overline{IRQ}$ output to be low when the DA1 bit is a one.
LRTH	Lower Receive Threshold	0:5:0	The one state of LRTH lowers the receiver turn-on threshold from –43 dBm to –47 dBm. (See SETUP)
MDA0	Modem Data Available (Zero)	0:E:0	MDA0 goes to one when the modem reads or writes register 0:0. MDA0 goes to zero when the host processor reads or writes register 0:0. MDA0 is used for parallel mode as well as for diagnostic data retrieval.

Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
MDA1	Modem Data Available (One)	1:E:0	MDA1 goes to one when the modem writes register 1:0. MDA1 goes to zero when the host processor reads register 1:0.
PDM	Parallel Data Mode	0:F:7	The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.
$\overline{\text{PNDET}}$	Period 'N' Detector	1:7:6	The zero state of $\overline{\text{PNDET}}$ indicates a PN sequence has been detected. $\overline{\text{PNDET}}$ sets to a one at the end of the PN sequence.
$\overline{\text{P2DET}}$	Period '2' Detector	1:4:2	The zero state of $\overline{\text{P2DET}}$ indicates a P2 sequence has been detected. $\overline{\text{P2DET}}$ sets to a one at the start of the PN sequence.
(None)	RAM Access B	1:F:0 – 7	Contains the RAM access code used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Access S	0:F:0 – 6	Contains the RAM access code used in reading or writing RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XBL	1:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XBM	1:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XSL	0:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XSM	0:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data YBL	1:0:0 – 7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device). See DA1.
(None)	RAM Data YBM	1:1:0 – 7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Data YSL	0:0:0 – 7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 0 (sample rate device). Shared by parallel data mode for presenting channel data to the host microprocessor bus. See Transceiver Data and DA0.
(None)	RAM Data YSM	0:1:0 – 7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 0 (sample rate device).
RAE	RAM Address Extension	0:5:4	This bit is an extension of RAM Access S when RAMWS is a one. During a RAM write to Chip 0, when RAE is a 1 the XRAM is selected and when RAE is a 0 the YRAM is selected.
RAMWB	RAM Write Chip 1 (baud rate device)	1:D:0	RAMWB is set to a one by the host processor when performing diagnostic writes to the baud rate device (Chip 1). RAMWB is set to a zero by the host when reading RAM diagnostic data from Chip 1.
RAMWS	RAM Write Chip 0 (sample rate device)	0:5:5	RAMWS is set to a one by the host processor when performing diagnostic writes to the sample rate device (Chip 0). RAMWS is set to a zero by the host when reading RAM diagnostic data from Chip 0.
RTS	Request-to-Send	0:5:7	The one state of RTS begins a transmit sequence. The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed. RTS parallels the operation of the hardware $\overline{\text{RTS}}$ control input. These inputs are "ORed" by the modem.
SETUP	Setup	0:E:3	The one state of SETUP causes the modem to reconfigure to the control word in the configuration register, and to assume the options specified for equalizer (0:5:1) and threshold (0:5:0). SETUP returns to zero when acted on by the modem. The time required for the SETUP bit to cause a change depends on the current state of the modem. The following table lists worst case delays.

Current State	V.21	G2	High Speed Receiver	High Speed Transmitter
DELAY	14 ms	400 μs	2 BAUD	2 BAUD + TURNOFF Sequence + Training (if applicable) + SQUELCH (if applicable)

Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
SQEXT	Squelch Extend	0:5:2	The one state of SQEXT inhibits reception of signals for 130 ms after the turn-off sequence.
TDIS	Training Disable	0:5:6	If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one prior to $\overline{RTS}$ going on, the generation of a training sequence is prevented at the start of transmission.
(None)	Transceiver Data	0:0 0–7	In receive parallel data mode, the modem presents eight bits of channel data in register 0:0 for reading by the host microprocessor. After the eight bits have been accumulated in register 0:C they are transferred to 0:0 and bit 0:E:0 goes to a one. When the host reads 0:0, bit 0:E:0 resets to a zero. The first bit of received data is not necessarily located in bit 0:0:0. The host must frame the received data by searching for message sync characters. Bit 0:E:0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations. In transmit parallel data mode the host stores data at location 0:0. This action causes bit 0:E:0 to reset to a 0. When the modem transfers the data from 0:0 to 0:2 bit 0.E:0 sets to a 1. The data is serially transmitted from register 0:2 least significant bit first. Received data is shifted into register 0:C from MSB toward LSB.
T2	T/2 Equalizer Select	0:5:1	If T2 is a one, an adaptive equalizer with two taps per baud is used. If T2 is a zero, an adaptive equalizer with one tap per baud is used. The number of taps remains the same for both cases. (See SETUP)

PERFORMANCE

Whether functioning in V.27 ter or V.29 configuration, the modem provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of −20 dBm as illustrated.

TYPICAL PHASE JITTER

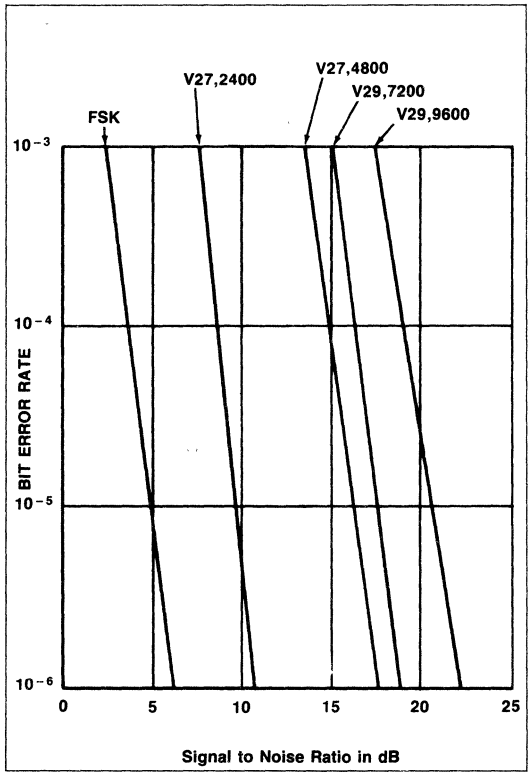
At 2400 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 12.5 dB in the presence of 15° peak-to-peak phase jitter at 150 Hz or with a signal-to-noise ratio of 15 dB in the presence of 30° peak-to-peak phase jitter at 120 Hz (scrambler inserted).

At 4800 bps (V.27 ter), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 19 dB in the presence of 15° peak-to-peak phase jitter at 60 Hz.

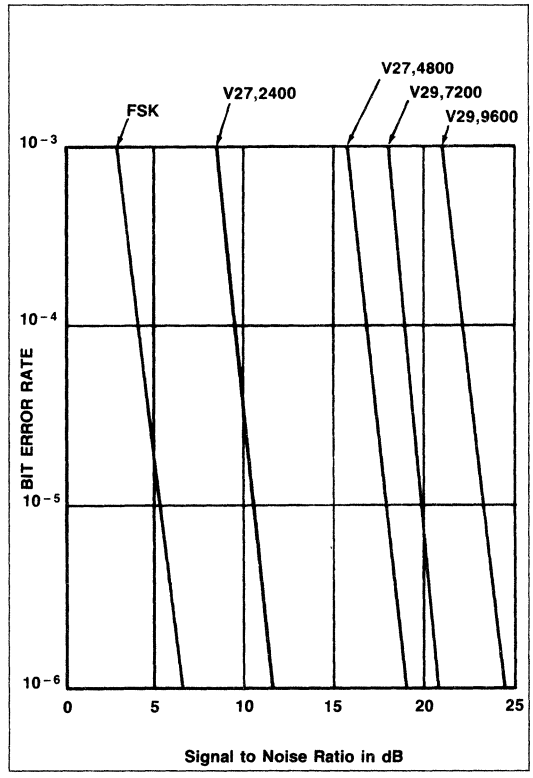
At 7200 bps (V.29), the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 25 dB in the presence of 12° peak-to-peak phase jitter at 300 Hz.

At 9600 bps, the modem exhibits a bit error rate of 10^{-6} or less with a signal-to-noise ratio of 23 dB in the presence of 10° peak-to-peak phase jitter at 60 Hz. The modem exhibits a bit error rate of 10^{-5} or less with a signal-to-noise ratio of 23 dB in the presence of 20° peak-to-peak phase jitter at 30 Hz.

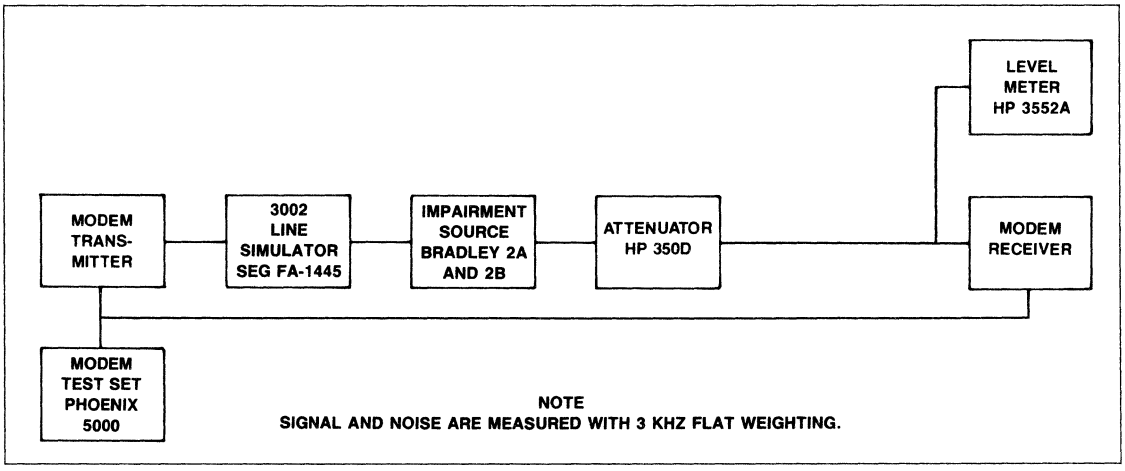
An example of the BER performance capabilities is given in the following diagrams:



Typical Bit Error Rate
(Back-to-Back, T Equalizer, Level −20 dBm)



Typical Bit Error Rate
(Unconditioned 3002 Line, T Equalizer Level −20 dBm)



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	350 mA	<500 mA
+12 Vdc	±5%	5 mA	< 10 mA
−12 Vdc	±5%	30 mA	< 50 mA

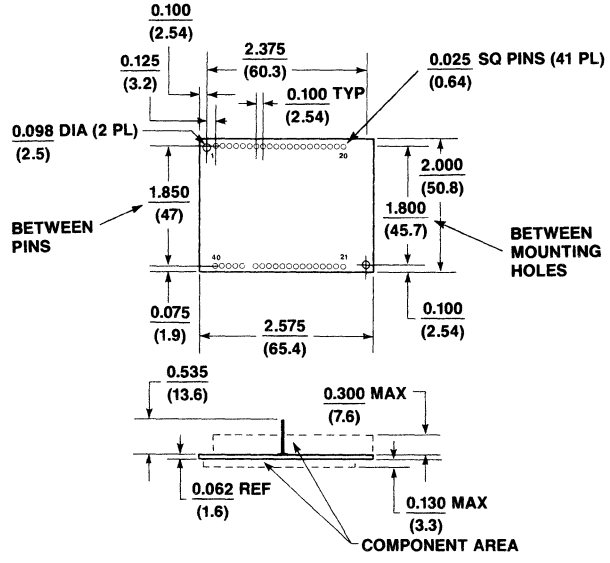
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less

Mechanical

Parameter	Specification
Board Structure	Single PC board with a row of 20 pins and a row of 20 pins in a dual-in-line pin configuration. Mates with Berg 65780 or equivalent.
Dimensions	
Width	2.0 in. (50.8 mm)
Length	2.575 in. (65.4 mm)
Component Height	0.30 in. (7.6 mm) above, 0.13 in. (3 30 mm) below
Weight (max.)	2.6 oz. (73 g)
Pins	
Length (max.)	0.650 in. (16.5 mm) above (tin), 0.535 in. (13.6 mm) above (gold)
Thickness	0.025 in (0.64 mm) square



R96MD Dimensions and Pin Locations

Rockwell

R144HD
14400 bps Half-Duplex Modem

INTRODUCTION

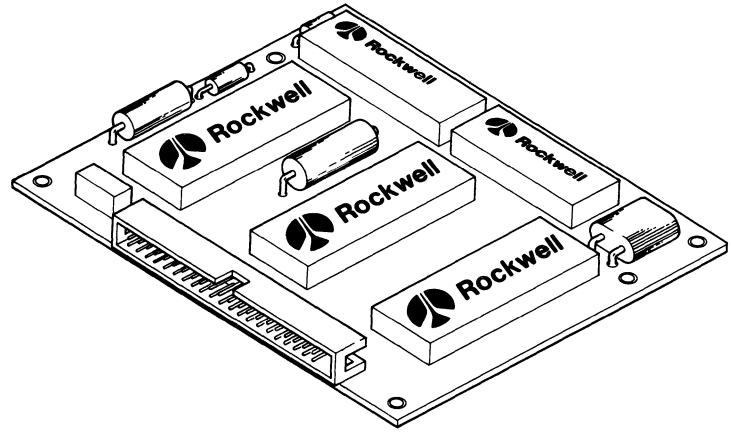
The Rockwell R144HD is a synchronous 14400 bits per second (bps) half-duplex modem. It is designed for operation over the public switched telephone network (PSTN) through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.33, V.29, V.27 ter, T.30, T.4 and T.3. The R144HD can operate at speeds of 14400, 12000, 9600, 7200, 4800, 2400 and 300 bps.

The R144HD is designed for use in Group 3 facsimile machines and is also compatible with Group 2 machines. User programmable features allow the modem operation to be tailored to support a wide range of functional requirements. The modem's small size, low power consumption, serial/parallel host interface, and standard connector simplify system design and allow installation in a compact enclosure.

FEATURES

- Compatibility:
  - — CCITT V.33, V.29, V.27 ter, T.30, V.21 Channel 2, T.4, T.3
  - — Trellis Coded Modulation (TCM) at 14400, 12000, 9600 and 7200 bps
- Group 3 and Group 2 Facsimile
- Half-Duplex (2-Wire)
- Programmable Tone Detection
- Programmable Dual/Single Tone Generation.
- DTMF Tone Generation
- Dynamic Range: −43 dBm to −6 dBm
- Diagnostic Capability
- Equalization:
  - — Automatic Adaptive
  - — Compromise Cable and Link (Selectable)
- DTE Interface:
  - — Microprocessor Bus
  - — CCITT V.24 (RS-232-C Compatible)
- Transmit Output Level: +5 dBm ±1 dBm
- Small Size: 100 mm × 82 mm (3.94 in. × 3.23 in.)
- Low Power Consumption: 2.5W (Typical)
- TTL and CMOS Compatible



R144HD Modem

TECHNICAL SPECIFICATIONS

TRANSMITTER TONAL SIGNALING AND CARRIER FREQUENCIES

T.30 Tonal Signaling Frequencies

Function	Frequency (Hz ±0.01%)
Calling Tone (CNG)	1100
Answer Tone (CED)	2100
Group 2 Identification (C12)	1850
Group 2 Command (GC2)	2100
Group 2 Confirmation (CFR2, MCF2)	1650
Line Conditioning Signal (LCS)	1100
End of Message (EOM)	1100
Procedure Interrupt (PIS)	462
MF1 Confirmation (CFR)	1080
MF1 Procedure Interrupt (PIS)	462

Carrier Frequencies

Function	Frequency (Hz ±0.01%)
T.3 (Group 2)	2100
V.27 ter, V.33, TCM96, TCM72	1800
V.29, (V 33, TCM96, TCM72)[1]	1700
1. Selectable option	

TONE GENERATION

Under control of the host processor, the R144HD can generate voice band tones up to 4800 Hz with a resolution of 0.15 Hz and an accuracy of 0.01%. Tones over 3000 Hz are attenuated.

TONE DETECTION

In the 300 bps FSK receive configuration, the presence of tones at preset frequencies is indicated by bits in the interface memory.

SIGNALING AND DATA RATES

Signaling/Data Rates

Specification	Baud Rate (Symbols/Sec.)	Bits Per Baud	Data Rate (BPS) (±0.01%)	Symbol Points
V.33	2400	6	14400	128
V.33	2400	5	12000	64
TCM96	2400	4	9600	32
TCM72	2400	3	7200	16
V.29	2400	4	9600	16
V.29	2400	3	7200	8
V.29	2400	2	4800	4
V.27	1600	3	4800	8
V 27	1200	2	2400	4

DATA ENCODING

The R144HD data encoding conforms to CCITT recommendations V.33, V.32 (TCM96, TCM72), V.29, and V.27 ter.

EQUALIZERS

The R144HD provides the following equalization functions which can be used to improve performance when operating over poor lines:

Cable Equalizers — Selectable compromise cable equalizers are provided to optimize performance over different lengths of non-loaded cable of 0.4 mm diameter.

Link Amplitude Equalizer — The selectable compromise amplitude equalizer may be inserted into the transmit and/or receive paths under control of the transmit amplitude equalizer enable and the receive amplitude equalizer enable bits in the interface memory. The amplitude select bit controls which of two amplitude equalizers is selected.

Automatic Adaptive Equalizer — An automatic adaptive equalizer is provided in the receiver circuit for high speed data configurations.

TRANSMITTED DATA SPECTRUM

If neither the link amplitude nor cable equalizer is enabled, the transmitter spectrum is shaped by the following raised cosine filter functions:

1. *1200 Baud.* Square root of 90 percent.
2. *1600 Baud.* Square root of 50 percent.
3. *2400 Baud.* Square root of 20 percent.

The out-of-band transmitter power limitations meet those specified by Part 68 of the FCC's Rules, and typically exceed the requirements of foreign telephone regulatory bodies.

SCRAMBLER/DESCRAMBLER

The R144HD incorporates a self-synchronizing scrambler/descrambler. This facility is in accordance with either V.27 ter, V.29, or V.33 depending on the selected configuration.

RECEIVED SIGNAL FREQUENCY TOLERANCE

The receiver circuit of the R144HD can adapt to received frequency error of up to ±10 Hz with less than a 0.2 dB degradation in BER performance. Group 2 carrier recovery capture range is 2100 ±30 Hz. The Group 2 receiver operates properly when the carrier is varied by ±16 Hz at a 0.1 Hz per second rate.

RECEIVE LEVEL

The receiver circuit of the R144HD satisfies all specified performance requirements for received line signal levels from –6 dBm to –43 dBm. The received line signal level is measured at the receiver analog input (RXA).

RECEIVE TIMING

In the receive state, the R144HD provides a Data Clock (DCLK) output in the form of a square wave. The low to high transitions of this output coincide with the center of received data bits. The timing recovery circuit is capable of tracking a ±0.01% frequency error in the associated transmit timing source. DCLK duty cycle is 50% ±1%.

TRANSMIT LEVEL

The transmitter output level defaults to +5 dBm ±1 dB at power on. When using the default transmit level and driving a 600 ohm load, the TXA output requires a 600 ohm series resistor to provide −1 dBm ±1 dB to the load. The output level can be programmed by performing a RAM write operation.

TRANSMIT TIMING

In the transmit state, the R144HD provides a Data Clock (DCLK) output with the following characteristics:

1. *Frequency.* Selected data rate of 14400, 12000, 9600, 7200, 4800, 2400, or 300 Hz (±0.01%). In Group 2, DCLK tracks an external 10368 Hz clock. If the external clock input (XCLK) is grounded the Group 2 DCLK is 10372.7 Hz ±0.01%.
2. *Duty Cycle.* 50 ±1%

Transmit Data (TXD) must be stable during the 1 microsecond periods immediately preceding and following the rising edge of DCLK.

TURN-ON SEQUENCE

The selectable turn-on sequences of the R144HD are defined in the following table:

Turn-On Sequences

Specification	$\overline{RTS}$-$\overline{CTS}$ Turn-On Time	
	Echo Protector Tone Disabled	Echo Protector Tone Enabled
V.33	1393 ms	1598 ms
TCM96	1393 ms	1598 ms
TCM72	1393 ms	1598 ms
V.29	253 ms	438 ms
V.27 4800 bps	708 ms	913 ms
V.27 2400 bps	943 ms	1148 ms
V.27 4800 Short	50	255
V.27 2400 Short	67	272
V.21 300 bps	≤14 ms	≤14 ms
Group 2	≤400 μs	≤400 μs

TURN-OFF SEQUENCE

For V.27 ter, the turn-off sequence consists of approximately 10 ms of remaining data and scrambled ones at 1200 baud or approximately 7 ms of data and scrambled ones at 1600 baud followed by a 20 ms period of no transmitted energy. For V.33, TCM96, and V.29, the turn-off sequence consists of approximately 5 ms of remaining data and scrambled 1's followed by a 20 ms period of no transmitted energy. In V.21 the transmitter turns off within 7 ms after $\overline{RTS}$ goes false. In Group 2 the transmitter turns off within 200 μseconds after $\overline{RTS}$ goes false.

CLAMPING

The following clamps are provided with the R144HD:

1. *Received Data (RXD).* RXD is clamped to a constant mark (1) whenever $\overline{RLSD}$ is off.
2. *Received Line Signal Detector (RLSD).* $\overline{RLSD}$ is clamped off (squelched) during the time when $\overline{RTS}$ is on.
3. *Extended Squelch.* Optionally, $\overline{RLSD}$ remains clamped off for 130 ms after the turn-off sequence.

RESPONSE TIMES OF CLEAR-TO-SEND ($\overline{CTS}$)

The time between the off-to-on transition of $\overline{RTS}$ and the off-to-on transition of $\overline{CTS}$ is dictated by the length of the training sequence. Response time is 1393 ms for V.33 and TCM96, 253 ms for V.29, 708 ms for V.27 ter at 4800 bps, and 943 ms for V.27 ter at 2400 bps. In V.21 $\overline{CTS}$ turns on in 14 ms or less. In Group 2 $\overline{CTS}$ turns on in 400 μs or less.

The time between the on-to-off transition of $\overline{RTS}$ and the on-to-off transition of $\overline{CTS}$ in the data state is a maximum of 2 baud times for all configurations.

RECEIVED LINE SIGNAL DETECTOR ($\overline{RLSD}$)

For V.33, TCM96, V.29 or V.27 ter, $\overline{RLSD}$ turns on at the end of the training sequence. If training is not detected at the receiver, the $\overline{RLSD}$ off-to-on response time is 15 ±10 ms. The $\overline{RLSD}$ on-to-off response time for V.27 is 10 ±5 ms, V.29 is 30 ±9 ms, and V.33 and TCM96 is 40 ±10 ms. Response times are measured with a signal at least 3 dB above the actual $\overline{RLSD}$ on threshold or at least 5 dB below the actual $\overline{RLSD}$ off threshold.

The $\overline{RLSD}$ on-to-off response time ensures that all valid data bits have appeared on RXD. The threshold levels are:

Greater than −43 dBm ($\overline{RLSD}$ on)
Less than −48 dBm ($\overline{RLSD}$ off)

NOTE

Performance may be at a reduced level when the received signal is less than −43 dBm.

A minimum hysteresis action of 2 dB exists between the actual off-to-on and on-to-off transition levels. The threshold levels and hysteresis action are measured with an unmodulated 2100 Hz tone applied to the receiver's audio input (RXA).

MODES OF OPERATION

The R144HD is capable of being operated in either a serial or a parallel mode of operation.

SERIAL MODE

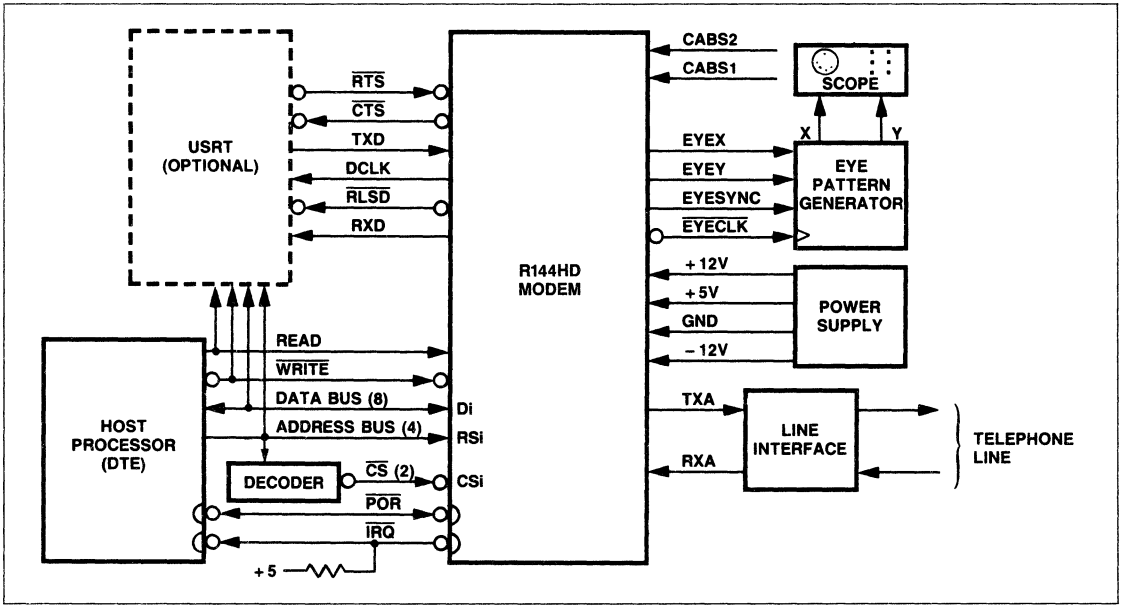
The serial mode uses standard V.24 (RS-232-C compatible) signals to transfer channel data. An optional USRT device (shown in the R144HD Functional Interconnect Diagram) illustrates this capability.

PARALLEL MODE

The R144HD has the capability of transferring channel data eight bits at a time via the microprocessor bus.

MODE SELECTION

Selection of either the serial or parallel mode of operation is by means of a control bit. To enable the parallel mode, the control bit must be set to a 1. The modem automatically defaults to the serial mode at power-on. In either mode the R144HD is configured by the host processor via the microprocessor bus.



R144HD Functional Interconnect Diagram

INTERFACE CRITERIA

The modem interface comprises both hardware and software circuits. Hardware circuits are assigned to specific pins in two rows. One row contains 20 pins (1–20) and the other row contains 21 pins (21–41). Software circuits are assigned to specific bits in a 32-byte interface memory.

HARDWARE CIRCUITS

Signal names and descriptions of the hardware circuits, including the microprocessor interface, are listed in the R144HD Hardware Circuits table; the table column titled 'Type' refers to designations found in the Hardware Circuit Characteristics. The microprocessor interface is designed to be directly compatible with an 8080 microprocessor. With the addition of a few external logic gates, it can be made compatible with 6500, 6800, or 68000 microprocessors.

R144HD Hardware Supervisory Circuits

Name	Type	Pin No.	Description
A. OVERHEAD:			
Ground	GND	14, 39	Power Supply Return
+5 volts	PWR	3, 4	+5 volt supply
+12 volts	PWR	26	+12 volt supply
−12 volts	PWR	37	−12 volt supply
$\overline{POR}$	I/OB	36	Power-on-reset

R144HD Hardware Circuits (Continued)

Name	Type	Pin No.	Description
B. MICROPROCESSOR INTERFACE:			
D7	I/OA	7	Data Bus (8 Bits)
D6	I/OA	5	
D5	I/OA	9	
D4	I/OA	31	
D3	I/OA	15	
D2	I/OA	28	
D1	I/OA	23	
D0	I/OA	29	
RS3	IA	30	Register Select (4 Bits)
RS2	IA	8	Select Reg. 0 – F
RS1	IA	27	
RS0	IA	10	
$\overline{CS0}$	IA	6	Chip Select Sample Rate Device
$\overline{CS1}$	IA	18	Chip Select Baud Rate Device
$\overline{READ}$	IA	1	Read Enable
$\overline{WRITE}$	IA	2	Write Enable
$\overline{IRQ}$	OB	32	Interrupt Request
C. V.24 INTERFACE:			
DCLK	OC	13	Data Clock
XCLK	IB	22	External Clock for Group II
$\overline{RTS}$	IB	19	Request-to-Send
$\overline{CTS}$	OC	17	Clear-to-Send
TXD	IB	20	Transmitter Data
RXD	OC	21	Receiver Data
$\overline{RLSD}$	OC	16	Received Line Signal Detector
D. CABLE EQUALIZER:			
CABS1	IB	33	Cable Select 1
CABS2	IB	34	Cable Select 2

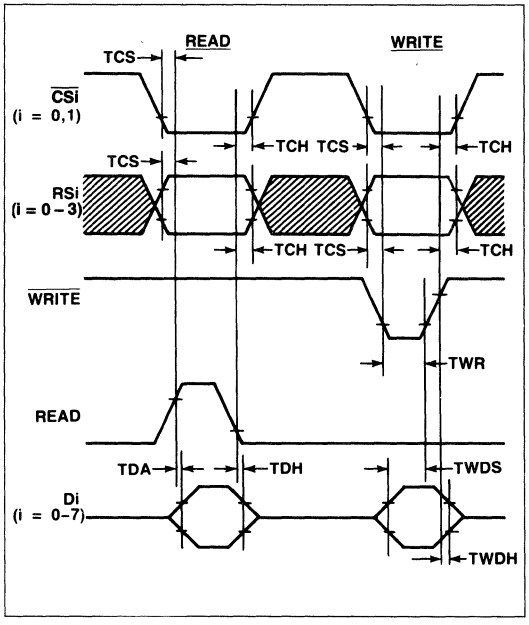
R144HD Hardware Circuits (Continued)

Name	Type	Pin No.	Description
E. ANALOG SIGNALS:			
TXA	AA	38	Transmitter Analog Output
RXA	AB	40	Receiver Analog Input
F. DIAGNOSTIC:			
EYEX	OC	24	Eye Pattern Data — X Axis
EYEY	OC	25	Eye Pattern Data — Y Axis
$\overline{\text{EYECLK}}$	OA	11	Eye Pattern Clock
EYESYNC	OA	12	Eye Pattern Synchronizing Signal

Eye Pattern Generation

The four hardware diagnostic circuits, identified in the preceding table, allow the user to generate and display an eye pattern. Circuits EYEX and EYEY serially present eye pattern data for the horizontal and vertical display inputs respectively. The 8-bit data words are shifted out most significant bit first, clocked by the rising edge of the $\overline{\text{EYECLK}}$ output. The EYESYNC output is provided for word synchronization. The falling edge of EYESYNC may be used to transfer the 8-bit word from the shift register to a holding register. Digital to analog conversion can then be performed for driving the X and Y inputs of an oscilloscope.

Microprocessor Timing



Microprocessor Interface Timing Diagram

Critical Timing Requirements

Characteristic	Symbol	Min	Max	Units
$\overline{\text{CSi}}$, RSi setup time prior to Read or $\overline{\text{Write}}$	TCS	30	—	NS
Data Access time after Read	TDA	—	140	NS
Data hold time after Read	TDH	10	50	NS
CSi, RSi hold time after Read or $\overline{\text{Write}}$	TCH	10	—	NS
Write data setup time	TWDS	75	—	NS
Write data hold time	TWDH	10	—	NS
Write strobe pulse width	TWR	75	—	NS

Cable Equalizer Selection

Cable Equalizer Selection

CABS 2	CABS 1	Length of 0.4mm Diameter Cable
0	0	0.0
0	1	1.8 km
1	0	3.6 km
1	1	7.2 km

Digital Interface Characteristics

The digital interface characteristics are listed in the table on the following page.

Analog Interface Characteristics

Analog Interface Characteristics

Name	Type	Characteristics
TXA	AA	The transmitter output is a low impedance operational amplifier output. In order to match to 600 ohms, an external 604 ohm series resistor is required.
RXA	AB	The receiver input impedance is 60K ohms ±23%.

SOFTWARE CIRCUITS

The R144HD comprises three signal processor chips. Two of these chips contain 16 registers to which an external (host) microprocessor has access. Although these registers are within the modem, they may be addressed as part of the host processor's memory space. The host may read data out of or write data into these registers. The registers are referred to as interface memory. Register in chip 0 update at the modem sample rate (9600 bps). Registers in chip 1 update at the selected baud rate.

When information in these registers is being discussed, the format Y:Z:Q is used. The chip is specified by Y(0 or 1), the register by Z(0-F), and the bit by Q(0-7, 0 = LSB). A bit is considered to be "on" when set to a 1.

Digital Interface Characteristics

Symbol	Parameter	Units	Input/Output Type IA	IB	OA	OB	OC	I/O A	I/O B
V_{IH}	Input Voltage, High	V	2.0 min.	2.0 min.				2.0 min.	5.25 max. 2.0 min.
V_{IL}	Input Voltage, Low	V	0.8 max.	0.8 max.				0.8 max.	0.8 max.
V_{OH}	Output Voltage, High	V			2.4 min.[1]			2.4 min. [1]	2.4 min.[3]
V_{OL}	Output Voltage, Low	V			0.4 max.[2]	0.4 max.[2]	0.4 max [2]	0.4 max.[2]	0.4 max.[5]
I_{IN}	Input Current, Leakage	μA	±2.5 max					±12.5 max.[4]	
I_{OH}	Output Current, High	mA			−0.1 max				
I_{OL}	Output Current, Low	mA			1.6 max.	1.6 max.	1.6 max.		
I_L	Output Current, Leakage	μA				±10 max.			
I_{PU}	Pull-up Current	μA		−240 max.			−240 max.		−260 max.
	(Short Circuit)			−10 min.			−10 min.		−100 min.
C_L	Capacitive Load	pF	5	5				10	40
C_D	Capacitive Drive	pF			100	100	100	100	100
	Circuit Type		TTL	TTL w/Pull-up	TTL	Open-Drain	Open Drain w/Pull-up	3 State Transceiver	Open-Drain w/Pull-up

Notes
1. I load = −100 μA
2. I load = 1.6 mA
3. I load = −40 μA
4. V_{IN} = 0.4 to 2.4 Vdc, V_{CC} = 5.25 Vdc
5. I load = 0.36 mA

3

Status/Control Bits

The operation of the R144HD is affected by a number of software control inputs. These inputs are written into registers within the interface memory via the host microprocessor bus. Modem operation is monitored by various software flags that are read from interface memory via the host microprocessor bus. All status and control bits are defined in the Interface Memory table. Bits designated by a '—' are reserved for modem use only and must not be changed by the host.

RAM Data Access

The R144HD provides the user with access to much of the data stored in the modem's memories. This data is a useful tool in performing certain diagnostic functions.

The modem contains 128 words of random access memory (RAM). Each word is 32-bits wide. Because the modem is optimized for performing complex arithmetic, the RAM words are frequently used for storing complex numbers. Therefore, each word is organized into a real part (16 bits) and an imaginary part (16-bits) that can be accessed independently. The portion of the word that normally holds the real value is referred to as XRAM. The portion that normally holds the imaginary value is referred to as YRAM. The entire contents of XRAM and YRAM may be read by the host processor via the microprocessor interface.

The interface memory acts as an intermediary during these host to signal processor RAM data exchanges. The RAM address to be read from or written to is determined by the contents of register 0:F (RAM ACCESS S) or 1:F (RAM ACCESS B). The R144HD RAM Access Codes table lists access codes for storage in registers 0:F or 1:F and the corresponding diagnostic functions. The R144HD Diagnostic Data Scaling table provides scaling information for these diagnostic functions. Each RAM word transferred to the interface memory is 32 bits long.

These bits are written into interface memory registers 0:3, 0:2, 0:1 and 0:0, or 1:3, 1:2, 1:1 and 1:0, in that order. Registers 3 and 2 contain the most and least significant bytes of XRAM data, respectively, while registers 1 and 0 contain the most and least significant bytes of YRAM data respectively.

When set to a one, bit 0:5:5 (RAMWS) or bit 1:D:0 (RAMWB) causes the modem to suspend transfer of RAM data to the interface memory, and instead, to transfer data from interface memory to RAM in chip 0 or in chip 1, respectively. When writing into the RAM, only 16 bits are transferred, not 32 bits as for a read operation. The 16 bits written in XRAM or YRAM come from registers 1 and 0, with register 1 being the most significant byte. Selection of XRAM or YRAM for the destination is by means of the code stored in the RAM Access B bits of register 1:F for chip 1, or by means of 0:5:4 (RAE) for chip 0. When bit 1:F:7 or 0:5:4 is set to one, the XRAM is selected. When 1:F:7 or 0:5:4 equals zero, YRAM is selected.

When the host processor reads or writes register 0, the modem data available bit 0:E:0 or 1:E:0 (MDAi) is reset to zero. When the modem reads or writes register 0, MDAi is set to a one. When set to a one by the host, bit 0:E:2 or 1:E:1 (IEi) enables the MDAi bit to cause an $\overline{IRQ}$ interrupt when set. While the $\overline{IRQ}$ line is driven to a TTL low level by the modem, bit 0:E:7 or 1:E:7 (IAi) goes to a one.

The default access codes are 22 for 1:F and 00 for 0:F.

Data in registers 1:3 and 1:1 are presented serially on EYEX and EYEY, respectively.

RAM Access Codes

The RAM access codes defined in the following table allow the host processor to read diagnostic information within the modem.

RAM Access Codes

Node	Function	Access	RAE	Chip	Read Reg. No.
1	Received Signal Samples	40	X	0	2,3
2	Demodulator Output	52	X	0	0,1,2,3
3	Low Pass Filter Output	54	X	0	0,1,2,3
4	Average Energy	5C	X	0	2,3
5	AGC Gain Word	3C	X	0	2,3
6	Tone 1 Frequency	7D	1	0	2,3
7	Tone 1 Level	7E	1	0	2,3
8	Tone 2 Frequency	7D	0	0	0,1
9	Tone 2 Level	7E	0	0	0,1
10	Output Level	4C	0	0	0,1
11	Receiver Sensitivity			0	
12	Receiver Hysteresis			0	
13	Checksum	3F		0,1	0,1
14	TX Level Attenuation	3E	1	0	2,3
15	Equalizer Input	40		1	0,1,2,3
16	Equalizer Tap Coefficients	01-20		1	0,1,2,3
17	Unrotated Equalizer Output	61		1	0,1,2,3

Ram Access Codes (Continued)

Node	Function	Access	RAE	Chip	Read Reg. No.
18	Rotated Equalizer Output (Received Point—Eye Pattern)	22		1	0,1,2,3
19	Decision Points (Ideal)	62		1	0,1,2,3
20	Error Vector	63		1	0,1,2,3
21	Rotation Angle	00		1	0,1
22	Frequency Correction	A8		1	2,3
23	EQM	AB		1	2,3
24	Group II Base Band Signal	C8		1	2,3
25	G2 AGC Gain Word	AD		1	2,3
26	G2 AGC Slew Rate	AA		1	2,3
27	G2 PLL Frequency Correction	C2		1	2,3
28	G2 PLL Slew Rate	F0		1	2,3
29	G2 Black/White Threshold	2A		1	0,1
30	G2 Phase Limit	F2		1	2,3

RAE = X is don't care since this location should only be read from, and *not* written to, by the host.

R144HD Interface Memory Chip 0 ($\overline{CS0}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	PDM	RAM ACCESS S						
E	IA0	—	—	—	SETUP	IE0	—	MDA0
D	—	—	—	—	—	—	—	—
C	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	—	—
5	RTS	TDIS	RAMWS	RAE	EPT	SQEXT	—	—
4	CONFIGURATION							
3	RAM DATA XSM; FREQM							
2	RAM DATA XSL; FREQL							
1	RAM DATA YSM							
0	RAM DATA YSL; TRANSCEIVER DATA							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only).

R144HD Interface Memory Chip 1 ($\overline{CS1}$)

Register \ Bit	7	6	5	4	3	2	1	0
F	RAM ACCESS B							
E	IA1	—	—	—	—	IE1	—	MDA1
D	—	TLE	RLE	J3L	—	—	FRT	RAMWB
C	—	—	—	—	—	—	—	G2FGC
B	FR3	FR2	FR1	—	—	—	—	—
A	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	—	—
7	—	$\overline{PNDET}$	—	—	—	—	—	$\overline{CDET}$
6	—	—	—	—	—	—	—	—
5	—	$\overline{FED}$	—	—	—	—	—	—
4	—	—	—	—	—	$\overline{P2DET}$	—	—
3	RAM DATA XBM							
2	RAM DATA XBL							
1	RAM DATA YBM							
0	RAM DATA YBL							
Register / Bit	7	6	5	4	3	2	1	0

— = Reserved (modem use only).

R144HD Interface Memory Definitions

Mnemonic	Name	Memory Location	Description
$\overline{\text{CDET}}$	Carrier Detector	1·7 0	The zero state of $\overline{\text{CDET}}$ indicates passband energy is being detected, and a training sequence is not present $\overline{\text{CDET}}$ goes to zero at the start of the data state, and returns to one at the end of the received signal. $\overline{\text{CDET}}$ activates up to 1 baud time before $\overline{\text{RLSD}}$ and deactivates within 2 baud times after $\overline{\text{RLSD}}$
(None)	Configuration	0·4:0–7	The host processor configures the R144HD by writing a control code into the configuration register in the interface memory space. (See SETUP) ***Configuration Control Codes*** Control codes for the R144HD configurations are: **Configuration** — **Configuration Code (HEX)** V.33 14400[1] — 31 V.33 12000 — 32 TCM96 9600 — 34 TCM72 7200 — 38 V.33 14400 (1700 Hz)[2] — 71 V.33 12000 (1700 Hz)[2] — 72 TCM96 9600 (1700 Hz)[2] — 74 TCM72 7200 (1700 Hz)[2] — 78 V.29 9600 — 14 V 29 7200 — 12 V.29 4800 Long — 11 V.27 4800 Long — 0A V.27 2400 — 09 V.27 4800 Short — 8A V.27 2400 Short — 89 FSK — 20 Group 2 and MF1 — 40 Single Tone Transmit — 80 Dual Tone Transmit — 81 DTMF Transmit — 82 [1] Default at POR. [2] The 1700 Hz carrier frequency is non-standard ***Configuration Definitions*** 1. *V.33.* When a V.33 configuration has been selected, the modem operates as specified in CCITT Recommendation V.33. 2 *TCM96 and TCM72.* When configuration TCM96 or TCM72 is selected, the training sequence is defined by V 33 and the modulation trellis coded is defined by V.32 (32 or 16 point constellation) 3. *V.29.* When a V.29 configuration has been selected, the modem operates as specified in CCITT Recommendation V.29. 4. *V.27.* When a V.27 configuration has been selected, the modem operates as specified in CCITT Recommendation V.27 ter. 5. *FSK.* The modem operates as a CCITT T.30 compatible 300 bps FSK modem having characteristics of the CCITT V.21 channel 2 modulation system. 6. *Group 2.* The modem operates as a CCITT T.3 compatible AM modem. This permits transmission to and reception from Group 2 facsimile apparatus. A carrier frequency of 2100 Hz is used. A black signal is transmitted as no carrier. The phase of the carrier representing white is reversed after each transition through black. When in the receive state, the R144HD recovers the carrier of the remote transmitting modem to perform a coherent demodulation of the incoming signal. This allows a baseband of 3400 Hz to be recovered. The recovered baseband signal is available on the microprocessor bus. The baseband signal is converted to black or white by comparing the received signal level with a preset threshold number. This number may be changed by the user.

R144HD Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td></td><td></td><td></td><td>Receiver data is presented to the RXD output at a rate of 10368 samples per second. The user should strobe the data on the rising edge of the data clock (DCLK). A logical 1 level (high voltage) represents white. A logical 0 level (low voltage) represents black.

7. Single Tone Transmit. In this configuration, activating signal RTS causes the modem to transmit a tone at a single frequency specified by the user. Two registers in the host interface memory space contain the frequency code. The most significant bits are specified in the FREQM register (0:3). The least significant bits are specified in the FREQL register (0:2). The least significant bit represents 0.146486 Hz ±0.01%. The frequency generated is: f = 0.146486 (256 FREQM + FREQL) Hz ±0.01%.

8. Dual Tone Transmit. In this configuration, activating RTS causes the modem to transmit two tones at frequencies and output levels specified by the user. By using the RAM Data Access routines, the user can program the tones and levels.

9. DTMF Transmit. In this configuration, when the hex value of a DTMF digit is stored in register 0:0, a DTMF tone will be transmitted if RTS is enabled.</td></tr>
<tr><td>EPT</td><td>Echo Protector Tone</td><td>0:5:3</td><td>If EPT is a one, an unmodulated carrier is transmitted for 185 ms followed by 20 ms of no transmitted energy at the beginning of the training sequence. This option is available in both the V.27 and V.29 configurations, although it is not specified in the CCITT V.29 recommendation.</td></tr>
<tr><td>$\overline{FED}$</td><td>Fast Energy Detector</td><td>1:5:6</td><td>The zero state of $\overline{FED}$ indicates energy is present above the receiver threshold in the passband. $\overline{FED}$ is not used for Group 2 Facsimile.</td></tr>
<tr><td>(None)</td><td>FREQL/FREQM</td><td>0:2:0-7,
0:3:0-7</td><td>The host processor conveys tone generation data to the transmitter by writing a 16-bit data word to the FREQL and FREQM registers in the interface memory space, as shown below.

FREQM Register (0:3)
<table><tr><td>Bit:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Data Word:</td><td>2^{15}</td><td>2^{14}</td><td>2^{13}</td><td>2^{12}</td><td>2^{11}</td><td>2^{10}</td><td>2^{9}</td><td>2^{8}</td></tr></table>
FREQL Register (0:2)
<table><tr><td>Bit:</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr><tr><td>Data Word:</td><td>2^{7}</td><td>2^{6}</td><td>2^{5}</td><td>2^{4}</td><td>2^{3}</td><td>2^{2}</td><td>2^{1}</td><td>2^{0}</td></tr></table>
The frequency number (N) determines the frequency (F) as follows:
F = (0.146486) (N) Hz ±0.01%.

Hexadecimal frequency numbers (FREQM, FREQL) for commonly generated tones are given below:
<table><tr><th>Frequency (Hz)</th><th>FREQM</th><th>FREQL</th></tr><tr><td>462</td><td>0C</td><td>52</td></tr><tr><td>1100</td><td>1D</td><td>55</td></tr><tr><td>1650</td><td>2C</td><td>00</td></tr><tr><td>1850</td><td>31</td><td>55</td></tr><tr><td>2100</td><td>38</td><td>00</td></tr></table></td></tr>
<tr><td>FRT</td><td>Freeze Taps</td><td></td><td>When FRT is a one, adaptive equalization taps are prevented from changing.</td></tr>
<tr><td>FR1 – FR3</td><td>Frequency 1,2,3</td><td>1:B:5,6,7</td><td>The one state of FR1, FR2 or FR3 indicates reception of the respective tonal frequency when the modem is configured for FSK. The default frequencies for FR1, FR2 and FR3 are:
<table><tr><th>Bit</th><th>Frequency (Hz)</th></tr><tr><td>FR1</td><td>2100</td></tr><tr><td>FR2</td><td>1100</td></tr><tr><td>FR3</td><td>462</td></tr></table></td></tr>
<tr><td>G2FGC</td><td>Group 2 Fast Gain Control</td><td>1:C:0</td><td>The one state of G2FGC selects a fast AGC rate (8.6 times standard) in Group 2 Facsimile.</td></tr>
<tr><td>IA1</td><td>Interrupt Active (One)</td><td>1:E:7</td><td>IA1 is a one when Chip 1 is driving $\overline{IRQ}$ to zero volts.</td></tr>
<tr><td>IA0</td><td>Interrupt Active (Zero)</td><td>0:E:7</td><td>IA0 is a one when Chip 0 is driving $\overline{IRQ}$ to zero volts.</td></tr>
</table>

R144HD Interface Memory Definitions (Continued)

Mnemonic	Name	Memory Location	Description
IE0	Interrupt Enable (Zero)	0:E:2	The one state of IE0 causes the $\overline{IRQ}$ output to be low when the DA0 bit is a one
IE1	Interrupt Enable (One)	1.E:2	The one state of IE1 causes the $\overline{IRQ}$ output to be low when the DA1 bit is a one.
J3L	Japanese 3 Link	1.D:4	The one state of J3L selects this standard for link amplitude equalizer. The zero state of J3L selects U.S. survey long.
MDA0	Modem Data Available (Zero)	0.E:0	MDA0 goes to one when the modem reads or writes register 0:0. MDA0 goes to zero when the host processor reads or writes register 0:0. MDA0 is used for parallel mode as well as for diagnostic data retrieval.
MDA1	Modem Data Available (One)	1:E:0	MDA1 goes to one when the modem writes register 1:0. MDA1 goes to zero when the host processor reads register 1·0.
PDM	Parallel Data Mode	0:F:7	The one state of PDM places the modem in the parallel mode and inhibits the reading of Chip 0 diagnostic data.
$\overline{PNDET}$	Period 'N' Detector	1:7:6	The zero state of $\overline{PNDET}$ indicates a PN sequence has been detected. $\overline{PNDET}$ sets to a one at the end of the PN sequence.
$\overline{P2DET}$	Period '2' Detector	1:4·2	The zero state of $\overline{P2DET}$ indicates a P2 sequence has been detected. $\overline{P2DET}$ sets to a one at the start of the PN sequence.
(None)	RAM Access B	1:F:0 – 7	Contains the RAM access code used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Access S	0:F:0 – 6	Contains the RAM access code used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XBL	1:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device)
(None)	RAM Data XBM	1:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 1 (baud rate device).
(None)	RAM Data XSL	0:2:0 – 7	Least significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data XSM	0:3:0 – 7	Most significant byte of 16-bit word x used in reading RAM locations in Chip 0 (sample rate device).
(None)	RAM Data YBL	1:0:0 – 7	Least significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device). See DA1.
(None)	RAM Data YBM	1.1:0 – 7	Most significant byte of 16-bit word y used in reading or writing RAM locations in Chip 1 (baud rate device).
(None)	RAM Data YSL	0:0:0 – 7	Least significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device). Shared by parallel data mode for presenting channel data to the host microprocessor bus. See Transceiver Data and DA0.
(None)	RAM Data YSM	0:1:0 – 7	Most significant byte of 16-bit word y used in reading RAM locations in Chip 0 (sample rate device).
RAE	RAM Address Extension	0:5:4	This bit is an extension of RAM Access S when RAMWS is a one. When RAE is a one, the XRAM in Chip 0 is selected for a RAM write operate, and when a zero the YRAM is selected.
RAMWB	RAM Write Chip 1 (baud rate device)	1:D:0	RAMWB is set to a one by the host processor when performing diagnostic writes to the baud rate device (Chip 1). RAMWB is set to a zero by the host when reading RAM diagnostic data from Chip 1.
RAMWS	RAM Write Chip 0 (sample rate device)	0:5.5	RAMWS is set to a one by the host processor when performing diagnostic writes to the sample rate device (Chip 0). RAMWS is set to a zero by the host when reading RAM diagnostic data from Chip 0.
RLE	Receiver Link Equalizer	1:D·5	The one state of RLE enables the link amplitude equalizer in the receiver.
RTS	Request-to-Send	0:5·7	The one state of RTS begins a transmit sequence. The modem will continue to transmit until RTS is turned off, and the turn-off sequence has been completed. RTS parallels the operation of the hardware $\overline{RTS}$ control input. These inputs are "ORed" by the modem.

R144HD Interface Memory Definitions (Continued)

<table>
<tr><th>Mnemonic</th><th>Name</th><th>Memory Location</th><th>Description</th></tr>
<tr><td>SETUP</td><td>Setup</td><td>0:E:3</td><td>The one state of SETUP causes the modem to reconfigure to the control word in the configuration register, and to assume the options specified for the equalizer (0:5:1). SETUP returns to zero when acted on by the modem. The time required for the SETUP bit to cause a change depends on the current state of the modem. The following table lists worst case delays.
<table>
<tr><th>Current State</th><th>V.21</th><th>G11</th><th>High Speed Receiver</th><th>High Speed Transmitter</th></tr>
<tr><td>DELAY</td><td>14 ms</td><td>400 μs</td><td>2 BAUD</td><td>2 BAUD + TURNOFF Sequence + Training (if applicable) + SQUELCH (if applicable)</td></tr>
</table></td></tr>
<tr><td>SQEXT</td><td>Squelch Extend</td><td>0:5:2</td><td>The one state of SQEXT inhibits reception of signals for 130 ms after the turn-off sequence.</td></tr>
<tr><td>TDIS</td><td>Training Disable</td><td>0:5:6</td><td>If TDIS is a one in the receive state, the modem is prevented from entering the training phase. If TDIS is a one prior to $\overline{RTS}$ going on, the generation of a training sequence is prevented at the start of transmission.</td></tr>
<tr><td>TLE</td><td>Transmitter Link Equalizer</td><td>1:D:6</td><td>The one state of TLE enables the link amplitude equalizer in the transmitter.</td></tr>
<tr><td>(None)</td><td>Transceiver Data</td><td>0:0:0–7</td><td>In receive parallel data mode, the modem presents eight bits of channel data in register 0:0 for reading by the host microprocessor. After the eight bits have been accumulated in register 0:C they are transferred to 0:0 and bit 0:E:0 goes to a one. When the host reads 0:0, bit 0:E:0 resets to a zero. The first bit of received data is not necessarily located in bit 0:0:0. The host must frame the received data by searching for message sync characters. Bit 0:E:0 sets at one eighth the bit rate in parallel data mode rather than at the sample rate (9600 Hz) as it does when reading RAM locations.

In transmit parallel data mode the host stores data at location 0:0. This action causes bit 0:E:0 to reset to a 0. When the modem transfers the data from 0:0 to 0:2 bit 0:E:0 sets to a 1. The data is serially transmitted from register 0:2 least significant bit first. Received data is shifted into register 0:C from MSB toward LSB.</td></tr>
</table>

AUTO DIAL SEQUENCE

The modem features a Dual Tone Multifrequency transmitter configuration. The duration of the DTMF signal is 95 ms and the interdigit delay is 70 ms.

The table below lists the Dial Digit Register (DDR) codes necessary for DTMF dialing and the corresponding tone pairs.

Dial Digits/Tone Pairs

Dial Digit Register (DDR) Hexadecimal Code	Dial Digit	Tone Pair (Hz)	
00	0	941	1336
01	1	697	1209
02	2	697	1336
03	3	697	1477
04	4	770	1209
05	5	770	1336
06	6	770	1477
07	7	852	1209
08	8	852	1336
09	9	852	1477
0A	*	941	1209
0B	#	941	1477

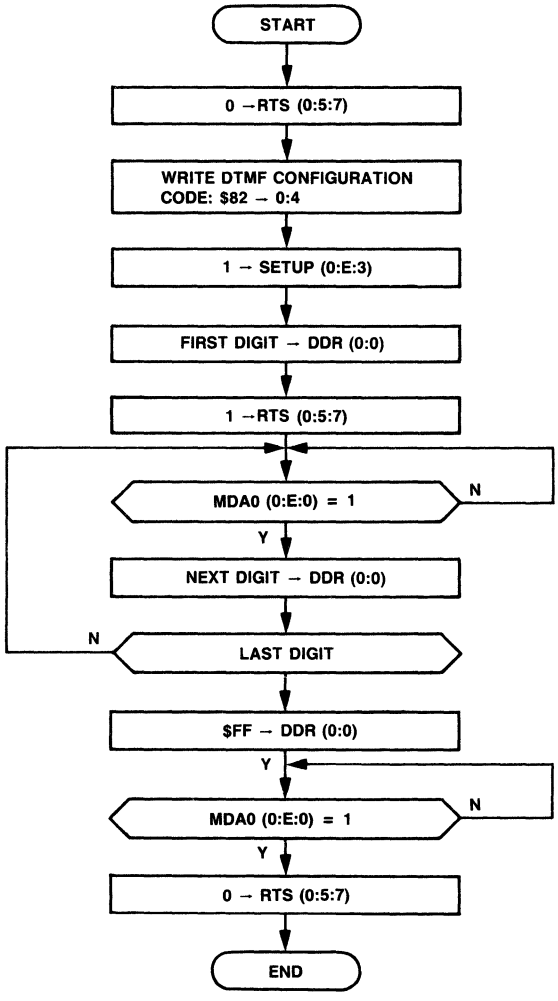
POWER-ON INITIALIZATION

When power is applied to the modem, a period of 50 to 350 ms is required for power supply settling. The power-on-reset signal ($\overline{POR}$) remains low during this period. Approximately 10 ms after the low to high transition of $\overline{POR}$, the modem is ready to be configured, and $\overline{RTS}$ may be activated. If the 5 Vdc power supply drops below 3.5 Vdc for more than 30 msec, the POR cycle is repeated.

At POR time the modem defaults to the following configuration: V.33/14400 bps, serial mode, training enabled, no echo protector tone on, no extended squelch, interrupts disabled, no link equalizer, RAM Access B code 22.

$\overline{POR}$ can be connected to a user supplied power-on-reset signal in a wire-or configuration. A low active pulse of 3 μsec or longer applied to the $\overline{POR}$ pin causes the modem to reset. The modem is ready to be configured 10 msec after the low active pulse is removed from $\overline{POR}$.

The following flowchart defines the auto dial sequence via the microprocessor interface memory.



Auto Dialing Sequence Flowchart

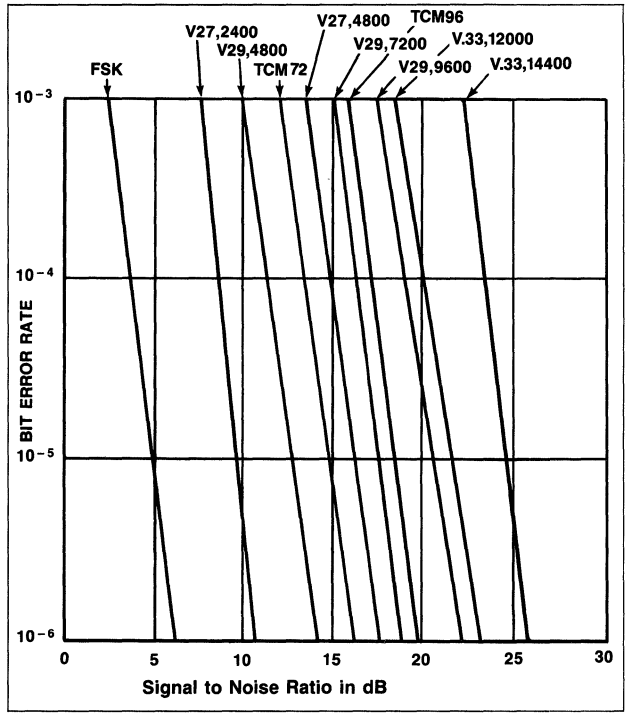
PERFORMANCE

Whether functioning as a V.27 ter, V.29, TCM96, TCM72, or V.33 type modem, the R144HD provides the user with unexcelled high performance.

TYPICAL BIT ERROR RATES

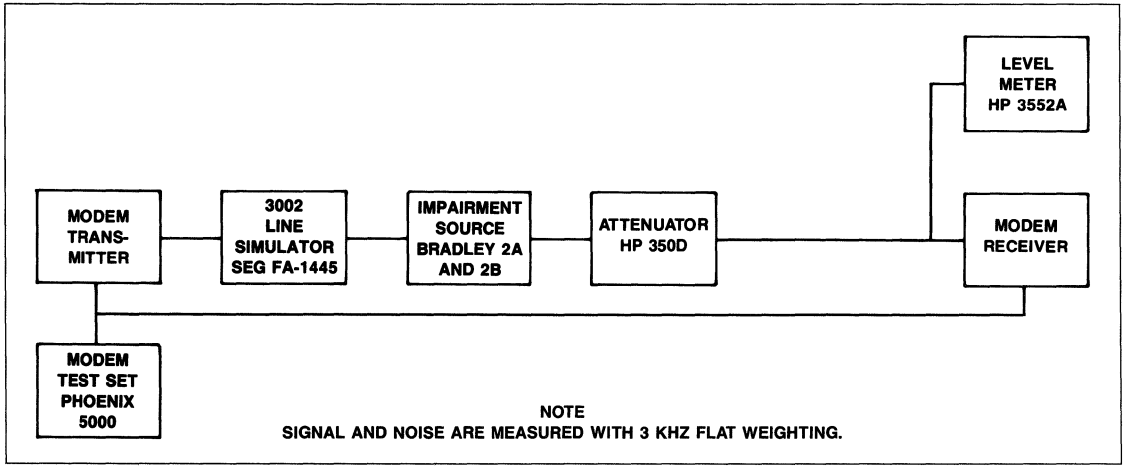
The Bit Error Rate (BER) performance of the modem is specified for a test configuration conforming to that specified in CCITT Recommendation V.56. Bit error rates are measured at a received line signal level of – 20 dBm as illustrated.

An example of the BER performance capabilities is given in the following diagram.



Typical Bit Error Rate
(Back-to-Back, Level – 20 dBm)

The BER performance test set-up is shown in the following diagram:



BER Performance Test Set-up

GENERAL SPECIFICATIONS

Power

Voltage	Tolerance	Current (Typical) @ 25°C	Current (Max) @ 0°C
+5 Vdc	±5%	500 mA	<600 mA
+12 Vdc	±5%	5 mA	< 10 mA
−12 Vdc	±5%	5 mA	< 10 mA

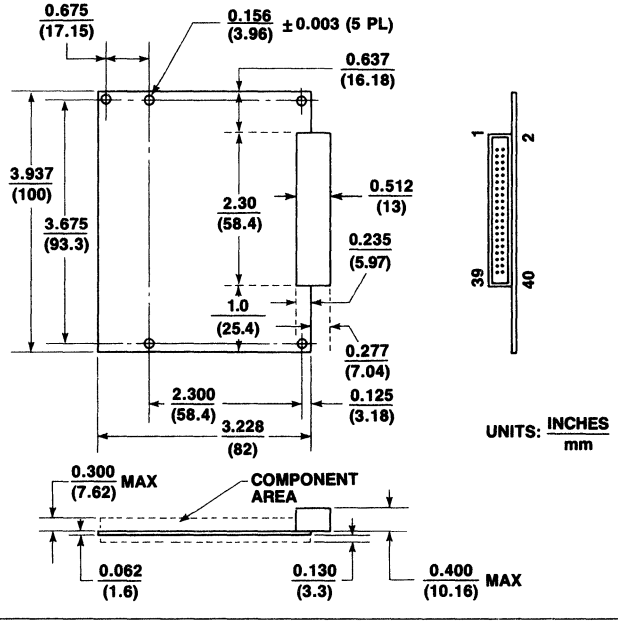
Note: All voltages must have ripple ≤0.1 volts peak-to-peak.

Environmental

Parameter	Specification
Temperature	
Operating	0°C to +60°C (32°F to 140°F)
Storage	−40°C to +80°C (−40°F to 176°F) (Stored in heat sealed antistatic bag and shipping container)
Relative Humidity	Up to 90% noncondensing, or a wet bulb temperature up to 35°C, whichever is less.

Mechanical

Parameter	Specification
Board Structure	Single PC board with single right angle header with 40 pins. Burndy FRS 40BS8P or equivalent mating connector.
Dimensions	
Width	3.937 in. (100 mm)
Length	3.228 in. (82 mm)
Component Height (max)	0.300 in. (7.62 mm) above, 0.130 in. (3.3 mm) below
Connector Height	0.400 in. (10.16 mm)
Weight (max)	3.6 oz. (100 g)



R144HD Dimensions and Pin Locations

Rockwell

R96MFX
9600 bps MONOFAX™ Modem

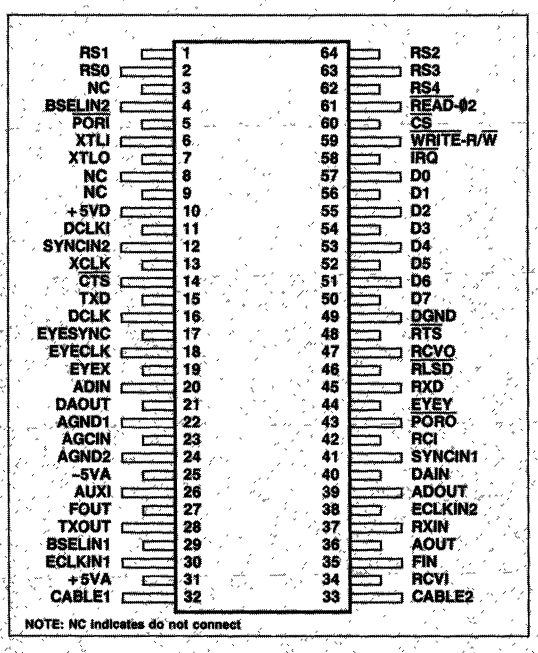
INTRODUCTION

The Rockwell R96 MONOFAX™ is a synchronous 9600 bits per second (bps) half-duplex modem in a single 64-pin quad-in-line package (QUIP). It is designed for operation over the public switched telephone network through line terminations provided by a data access arrangement (DAA).

The modem satisfies the telecommunications requirements specified in CCITT recommendations V.29, V.27 ter, V.21 and T.4, and the binary signaling requirements of T.30. The R96MFX can operate at speeds of 9600, 7200, 4800, 2400 and 300 bps.

The R96FAX is designed for use in Group 3 facsimile machines. The modem's small size and low power consumption allow the design of compact system enclosures for use in both office and home environments.

MONOFAX is a trademark of Rockwell International

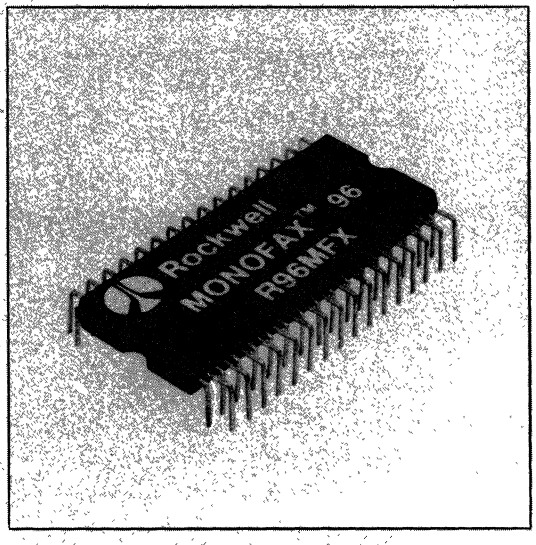


NOTE: NC indicates do not connect

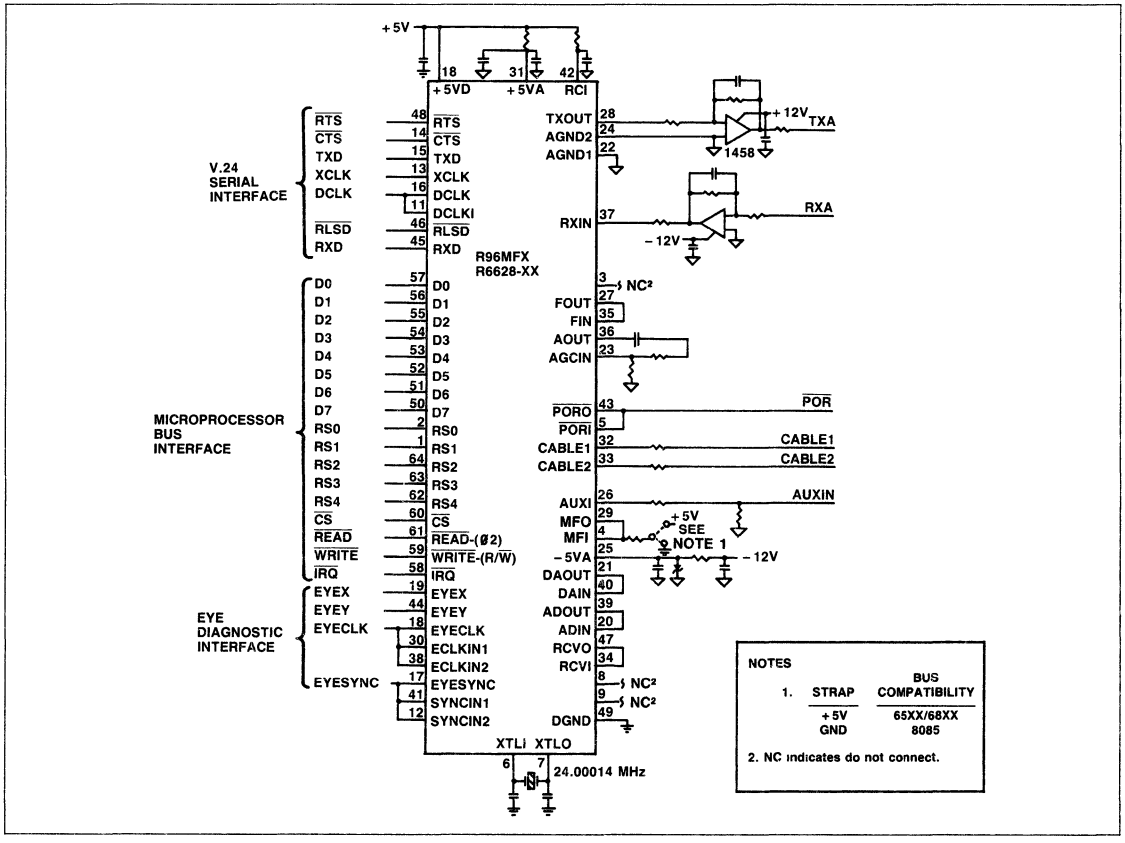
R96MFX Pin Assignments

FEATURES

- Single 64-Pin QUIP
- CCITT V.29, V.27 ter, T.30, V.21 Channel 2, T.4
- Group 3 Facsimile Transmission/Reception
- Half-Duplex (2-Wire)
- Programmable Dual Tone Generation and Detection
- Programmable Tone Detection
- Programmable Turn-on and Turn-off Threshold
- Diagnostic Capability
  - — Provides Telephone Line Quality Monitoring Statistics
- Equalization
  - — Automatic Adaptive
  - — Compromise Cable (Selectable)
- DTE Interface: Two Alternate Ports
  - — Selectable Microprocessor Bus (6500 or 8085 Compatible)
  - — CCITT V.24 (RS-232-C Compatible)
- Low Power Consumption: 1W (Typical)
  - — +5 Vdc ±5% <250 mA
  - — −5 Vdc ±5% <25 mA
- Programmable Transmit Output Level
- TTL and CMOS Compatible



R96MFX 9600 bps MONOFAX Modem



R96MFX Schematic Diagram

SECTION 4
CUSTOM AND PRIVATE LABEL MODEMS

CUSTOM AND PRIVATE LABEL MODEMS
Customizing Products for OEM Requirements

Combining communications expertise with custom design capabilities and vertically integrated manufacturing capabilities, Rockwell offers fully customized or private label products to meet your communications requirements. Rockwell has an experience base of over ten years as a supplier of custom modems for major computer and data communications companies worldwide.

Continued advancements in VLSI modem and digital communications technology enable us to design and produce custom modems in a full range of speeds and compatibilities. In addition to Bell and CCITT compliance, custom modems can be designed specifically for your proprietary hardware or software compatibility requirements, including popular error correction protocols. Stand-alone, custom board, rack mount and PC card configurations are available to meet your form factor requirements.

For rapid market entry with minimum investment, Rockwell offers OEMs and resellers a growing line of private label modems. Full turn-key solutions, these stand-alone modems require only the addition of your company logo. Rockwell can also supply custom front panels and a selection of enclosure colors. PC card private label modems are also available. The chart below presents the current models of the private label modem product line.

Model	Data Speed (bps)	PSTN/ Leased Line	2/4-Wire Half/Full-Duplex	Sync/Async	Compliance	Error Correction
RG224	2400, 1200 300	P	2WFD	Sync, Async	CCITT V.22 bis, V.22A/B; Bell 212, 103	
RG224EC	2400, 1200 300	P	2WFD	Sync, Async	CCITT V.22 bis, V.22A/B; Bell 212, 103	MNP Class 3
RGV22BEC	2400, 1200 300	P	2WFD	Sync, Async	CCITT V.22 bis, V.22A/B; Bell 212, 103	MNP Class 3
RG208	4800, 2400	P/L	2WHD, 4WFD	Sync	Bell 208A/B; CCITT V.27 bis/ter	
RGV29FT	9600, 7200, 4800, 2400	P/L	2WHD, 4WFD	Sync	CCITT V.29, V.27 bis/ter	

Rockwell

RG224EC and RGV22BEC 2400 bps Modems

DESCRIPTION

The RG224EC and RGV22BEC are advanced error correcting 2400/1200/300 bps modems for private labeling by OEMs and resellers. With Rockwell VLSI and digital signal processing technology, these modems offer high quality, low cost and a versatile array of features.

These Bell-compatible modems operate at 2400 bps, 1200 bps or 300 bps full-duplex, over the dial-up telephone network. Over shorter hauls, the RG224 works in half-duplex and fallback (synchronous and asynchronous) modes.

The RG224EC and RGV22BEC are packed with user convenience features. In answer mode, the modem automatically adapts to match the speed of the incoming signal. For outgoing calls, pulse or tone dialing can be selected, and communication software is no problem with "AT" command set compatibility. Rockwell's unique automatic adaptive equalization technique compensates for noise on the telephone line or weak incoming signals, delivering accurate and reliable data. A non-volatile memory stores up to ten frequently called numbers and command strings. The RG224 also features auto answer, a call progress speaker with volume control, and the ability to monitor another data transmission.

VIRTUALLY ERROR-FREE TRANSMISSION

Error detection is crucial at 2400 bps because so much data can be garbled by a single distortion in the line. Simple protocols are not equipped to handle the errors and delays inherent in the long-distance dial-up network.

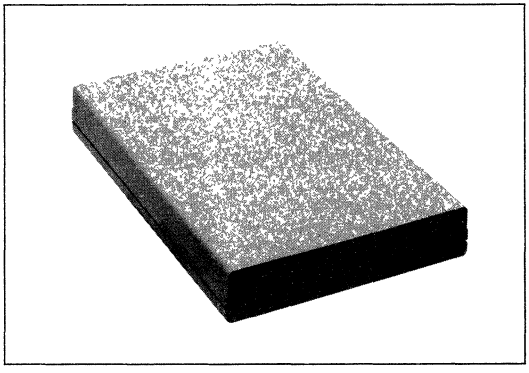
The RG224EC corrects errors by employing Microcom's class 3 MNP protocol, which resides in firmware in the modem itself and is transparent to the user except for a few simple commands. The RGV22BEC further tailors this error correcting software to the country of operation. This protocol is bit-synchronous, which is 20% more efficient than asynchronous transmission. It has error detection based upon a 16-bit Cyclic Redundancy Check (CRC), error correction, and automatic retransmission. These error correction techniques create a reliable link of virtually error-free data transfer at both 2400 and 1200 bps when communicating with another MNP type modem.

INTERNATIONAL COMPATIBILITY

For global markets, the RG224EC and RGV22BEC are compatible with CCITT V.22A/B and V.22 bis standards. The RGV22BEC offers all the features of the RG224EC plus a telco interface and dialing protocol developed for specific country operation. Contact the Rockwell factory for information on available international versions.

CUSTOMIZING THE PRODUCT

The RG224EC and RGV22BEC are available with customized logos and enclosure colors. The standard enclosure color is bone, with other colors available on special order. Rockwell will silkscreen your own custom artwork or logo on the available on the front panel. For a true scale front drawing, request RG224EC brochure (Document No. D-4).



RG224EC Modem

CUSTOMIZED DOCUMENTATION AND PACKAGING

The corrugated cardboard shipping box is blank, ready to slip on your sleeve. The text will be supplied to you on an industry compatible 5-1/4" diskette in Microsoft Word format. It can be directly output to an HP LaserJet printer, or easily converted for output to a different printer. Photostats of all artwork used in the manual complete the documentation kit. With this kit, you can easily paste up a manual for printing, or you can have it edited to your specific needs.

FOR ADDITIONAL INFORMATION

For a color brochure on the RG224EC, request Document No. D-4. Additional 2400 bps private label modems are available, including a version without error correction, the RG224, and an internal PC halfcard. Contact the Rockwell factory for details.

TECHNICAL SPECIFICATIONS

Compliance: Bell 212A and 103
CCITT V.22A/B and V.22 bis

Data Format: Synchronous or asynchronous binary serial.
Synchronous: 2400 or 1200 bps.
Asynchronous: 2400, 1200 or 300 bps.
Character lengths: 8, 9, 10 or 11 bits.

Operation: Full or half duplex over 2-wire dial-up or leased lines.

Modulation: QAM for V.22 bis; DPSK for V.22 and Bell 212A
FSK for 0-300 bps.

Carrier Frequency:

Specification	Frequency
V.22 bis low channel, Originate Mode	1200
V.22 low channel, Originate Mode	1200
V.22 bis high channel, Answer Mode	2400
V.22 high channel, Answer Mode	2400
Bell 212A high channel Answer Mode	2400
Bell 212A low channel Originate Mode	1200
Bell 103/113 Originating Mark	1270
Bell 103/113 Originating Space	1070
Bell 103/113 Answer Mark	2225
Bell 103/113 Answer Space	2025

Equalization: Automatic adaptive and fixed compromise.

Transit Level: −10 dBm ±1 dB

Dial modes: Pulse or tone auto dialing. Non-volatile directory stores 10 numbers with 40 digits each.

Sensitive: 0 to −43 dBm

Answer Modes: Manual or automatic, with automatic conversion to speed of incoming data.

Telephone Interface: Connection to two-wire DDD network via USOC RJ11, RJ12 and RJ13 jack.

DTE Interface: EIA RS-232-C, CCITT V.24/V.28

Error Correction: Microcom Network Protocol (MNP) level 3

Command Compatibility: Hayes "AT" command set compatible

Software Compatibility: Crosstalk XVI and Smartcom II.

Test Modes: Local analog loopback, remote digital loopback.

Certification: FCC Parts 68 and 15 Class B. UL/CSA approved.

Electrical: 120 VAC (104 VAC-128 VAC), 60 Hz, 0.2A external wallmount transformer

Environmental: Operating: −10°C to 50°C
Storage: −20°C to 80°C
Relative Humidity: 10% to 90%, noncondensing, or a wet bulb temperature of 35°C, whichever is less

Dimensions: Width 6.25 in. (15.88 cm)
Height 1.375 in. (3.49 cm)
Depth 10.50 in. (26.67 cm)

Weight: 3.75 lbs. (8.25 kg)

Warranty: Two-year, limited

Specification is subject to change without notice and shall not be regarded as a warranty

RG208
4800 bps Private Label Modem

DESCRIPTION

The RG208 4800 bps synchronous modem is designed for private labeling by OEMs and resellers. It incorporates advanced features such as auto-dial, four-wire dial backup and truly uncomplicated set-up. In addition, the RG208 is compatible with existing 208A/B modems as well as the CCITT V.27 bis/ter standard. The front panel liquid crystal display and touch sensitive keys make configuration easy, with menus, call progress and system status displays. Optimum data transfer over poor or changing lines is assured with Rockwell's Auto Adaptive Equalization.

JUST ADD YOUR LOGO

Add your logo to the area within the embossed border on the left side of the front panel. Or, simply send us the camera-ready art and we will do the rest.

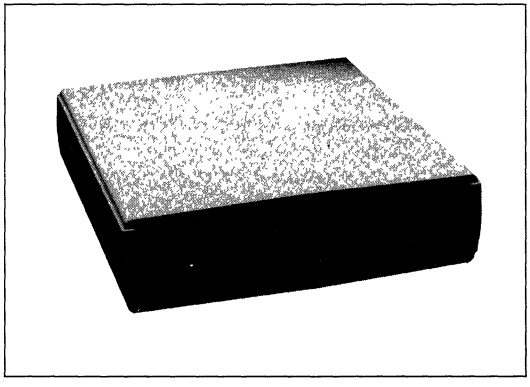
You may customize the front panel with your choice of color and graphic designs. Rockwell will be happy to quote the additional cost for a custom front panel.

PERSONALIZED DOCUMENTATION

The RG208 user manual is stored on an industry compatible 5-1/4 in. diskette in Microsoft Word format. Edit the file to add your company name, model number and any application-specific instructions. Print the file directly on an HP LaserJet printer. Photostats of all artwork and photographs used in the manuals complete the documentation kit.

FEATURES

- Self-contained modem with your customized logo
- 4800 or 2400 bps operation
- Bell 208A/B and CCITT V.27 bis/ter compatible
- Compatible with industry standard 208A/B modems
- Full-duplex, synchronous operation over four-wire leased lines
- Full duplex over four-wire dial backup (dual, two-wire dual lines)
- Half-duplex operation over two-wire, dial-up or leased lines
- Auto/manual dial and answer
- LCD front panel displays user commands and system status for ease of use
- Easily configured via front panel touch-sensitive keys: no internal switches and registers to set
- Pulse or tone auto-dialing with automatic redial capability
- Call progress monitored on LCD display or internal speaker
- Non-volatile directory of 20 telephone numbers (35 digits each)
- Two year limited warranty; extended warranty plans are available



RG208 Modem

RG208 PACKAGING

The RG208 is shipped to you in a blank corrugated cardboard box ready to slip into your branded sleeve. The modem, three cables (an RJ11C, RF45S and a standard telephone cable) and the power supply are packed in foam protectors and covered with a top tray that holds your customized documentation.

FOR MORE INFORMATION

Request the RG208 brochure (Literature Order No. D-6).

TECHNICAL SPECIFICATIONS

Compliance: Bell 208 A/B and V.27 bis/ter

Data Rates: 4800 and 2400 bps

Data Format: Synchronous binary serial

Operation: Four-wire leased line, full duplex
Two-wire leased line, half-duplex
Two-wire dial-up line, half-duplex or pseudo full-duplex
Four-wire dial backup, full-duplex (two 2-wire dial-up lines, half-duplex)

Modulation: Eight-phase DPSK

Carrier Frequency: 1800 ±1 Hz

Line Requirement: Unconditioned

Equalization: Automatic adaptive; selectable cable length equalization

Transmit Clock: Internal or External

Transmit Level: 0 to −14 dBm (Selectable in −2 dBm steps)

Receiver Threshold: −43 dBm, −33 dBm, −26 dBm, −16 dBm (Selectable)

RTS/CTS Delay: Bell 208: 50 ms or 150 ms (Selectable)
V.27: 50 ms, 67 ms, 708 ms, or 943 ms (Selectabl)

Telephone Interface: Leased Line: RJ14C
Dial-up Lines: RJ11C and RF45S

DTE Interface: EIA RS-232-C, CCITT V.24/V.28

Liquid Crystal Display: Two-line, 40-character LCD and four key system for menu driven operation and configuration from front panel. Configuration stored in nonvolatile memory. Displays call progress, error messages, line quality, signal strength, CD, RTS, CTS, DSR and test results

Auto-dial: Automatic tone or pulse dialing; telephone directory stores 20 numbers with 35 digits each

Answer Modes: Manual or automatic

Terminal Mode: May be controlled by terminal commands in SDLC eight-bit ASCII data format

Test Modes: Local and remote analog loopback, digital loopback, and self-test

Certification: FCC parts 68 and 15 Class A. UL/CSA certified

Electrical: 120 VAC (104 VAC-128 VAC), 60 Hz, 0.25 A external wallmount transformer

Environmental: Operating Temperature: 5°C to 40°C
Storage Temperature: −20°C to 70°C
Relative Humidity: 10% to 90%, noncondensing, or a wet bulb temperature of 35°C, whichever is less

Dimensions: Width: 8.5 in. (21.6 cm)
Height: 2.6 in. (6.7 cm)
Depth: 9.3 in. (23.6 cm)

Weight: 4.6 lbs. (10.1 kg)

Warranty: Two-year, limited

Specification is subject to change without notice and shall not be regarded as a warranty.

Rockwell

RGV29FT
9600 bps Private Label Modem

INTRODUCTION

The RGV29FT is a 9600 bps synchronous modem with fast training capability for leased line network applications. Designed for private labeling by OEMs and resellers, the RGV29FT also includes a four-wire dial line mode which may be used to back-up a four-wire leased circuit. The auto-dial/auto-answer features and convenient configuration from the front panel ensure easy operation for even the first-time user. The front panel liquid crystal display displays configuration menus, modem status, line quality, signal strength and the telephone numbers stored in the programmable telephone number directory.

The RGV29FT is compatible with CCITT V.22 and V.27 bis/ter standards. The security option provides a choice of password and dialback security modes.

READY FOR PRIVATE LABELING

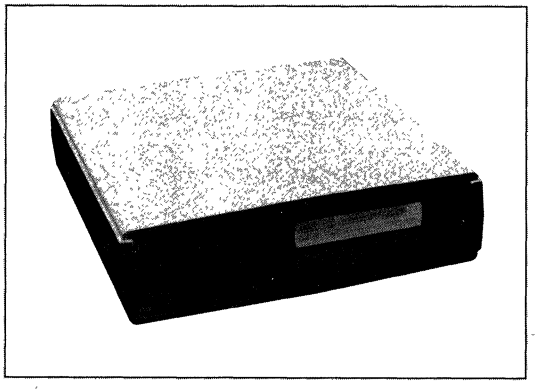
The front panel includes an embossed area ready to accept your company logo or may be customized to your design. Cost of custom front panel colors and graphic designs are available by quotation. The RGV29FT is shipped in a blank corrugated cardboard box ready for insertion in your branded outer sleeve.

CUSTOMIZE YOUR DOCUMENTATION

The user manual is supplied on an IBM PC-compatible 5 1/4 in. diskette in Microsoft Word format, ready for addition of your company name, model number. It is formatted for printout on an HP LaserJet printer. Photostats of artwork used in the manual complete your documentation kit.

FOR MORE INFORMATION

Request RGV29FT brochure (Literature Order No. D-9).



RGV29FT Modem

TECHNICAL SPECIFICATIONS

Compliance: CCITT V.29 and V.27 bis/ter

Data Rates: V.29: 9600, 7200, and 4800 bps
V.27: bis/ter: 4800 and 2400 bps

Data Format: Synchronous binary serial

Operation: Four-wire leased line, full duplex
Two-wire leased line, half-duplex
Two-wire dial-up line, half-duplex or pseudo full-duplex
Four-wire dial backup, full-duplex (two 2-wire half-duplex dial-up lines)

Modulation: V.29: Quadrature Amplitude Modulation (QAM)

Carrier Frequency: 1700 ±1 Hz or 1800 ±1 Hz

Line Requirement: Unconditioned

Equalization: Automatic adaptive; selectable cable length equalization

Transmit Clock: Internal or External

Transmit Level: 0 to −14 dBm (Selectable in −2 dBm steps)

Receiver Threshold: −43 dBm, −33 dBm, −26 dBm, −16 dBm (Selectable)

RTS/CTS Delay: Fast Train:
23 ms (V.29 9600, 7200, 4800 bps)
22 ms (V.27 4800 bps)
30 ms (V.27 2400 bps)
CCITT V.29: 253 ms

Telephone Interface: Leased Line: RJ14C
Dial-up lines: RJ11C and RJ45S

DTE Interface: EIA RS-232-C, CCITT V.24/V.28

Liquid Crystal Display: Two-line, 40-character LCD and four key system for menu driven operation and configuration from front panel. Configuration stored in non-volatile memory. Displays call progress, error messages, line quality, signal strength, CD, RTS, CTS, DSR and test results

Auto-dial: Automatic tone or pulse dialing; telephone directory stores 20 numbers with 35 digits each

Answer Modes: Manual or automatic

Security Mode Option: Password or dialback

Test Modes: Local and remote analog loopback, digital loopback, and self-test Certification: FCC parts 68 and 15 Class A. Designed for UL and CSA certification

Electrical: 120 VAC (104 VAC-128 VAC), 60 Hz, 0.25 A external wallmount transformer

Environmental: Operating Temperatures: 5°C to 40°C
Storage Temperature: −20°C to 70°C
Relative Humidity: 10% to 90%, noncondensing, or a wet bulb temperature of 35°C, whichever is less

Dimensions: Width: 8.5 in. (21.6 cm)
Height: 2.6 in. (6.7 cm)
Depth: 9.3 in. (23.6 cm)

Weight: 4.6 lbs. (10.1 kg)

Warranty: Two-year, limited

Specification is subject to change without notice and shall not be regarded as a warranty.

SECTION 5
APPLICATION NOTES

Rockwell

An R6500/11 — R2424 Intelligent Modem Design

by Ron Collins and Joseph W. Hance
Product Applications Engineers
Semiconductor Products Division, Newport Beach, California

INTRODUCTION

The combination of single chip microcomputers and standard modems makes possible the implementation of sophisticated and flexible telecommunications systems. The intelligent modem has become the standard for personal microcomputers and provides access to many outside resources over standard telephone lines.

This application note describes the hardware and software design of a 300/1200/2400 bit-per-second (bps) modem based on the Rockwell R2424 single board modem and the R6500/11 single-chip microcomputer. The system design minimizes the number of devices used and provides the user adequate room for special features. The software implements the industry standard "AT" command set so that compatibility with commercial software packages is provided. This particular design is that of a stand-alone "Box Modem" but only minimal changes are needed in the configuration for a personal computer bus compatible modem.

HARDWARE DESIGN

The hardware used in this design (see the schematic in Figure 1) consists of an R6500/11 microcomputer (Z1), an R2424DC modem module (Z3), and a 16L8 type PAL (Z2). A complete parts list is tabulated in Table 1.

The R6500/11 controls the system and implements the high level command protocol. It has an internal UART which provides communications between the host computer and the modem. The R2424DC module is addressed as a peripheral on the abbreviated bus of the R6500/11. All modem configuration, dial, status, and commands are transmitted over the data bus. The serial interface to the R2424DC carries only the data transmitted or received over the telephone line.

Table 1. R6500/11—R2424 Intelligent Modem Parts List

Item	Part	Qty	Description
1	P1	1	RS-232C Connector, Female, DB-25
2	R1	1	4.7K Resistor, 5%
3	R2	1	3K Resistor, 5%
4	R3	1	3K Resistor, 5%
5	Y1	1	1.8432 MHz Crystal
6	Z1	1	R6500/11 Single-chip Microcomputer
7	Z2	1	PAL 16L8
8	Z3	1	R2424DC Modem Board
9	Z4	1	MC1488
10	Z5	1	MC1488
11	Z6	1	MC1489

The PAL* generates the proper bus control signals needed to interface the R2424DC to the R6500/11's bus. It also allows the R6500/11 to switch the serial data between the host and the line to accommodate the command and on-line modes. The 1488's (Z4, Z5) and the 1489 (Z6) provide a standard RS-232-C interface for the host computer. These devices would not be necessary in the design of a plug-in personal computer modem. Figure 2 shows the logic equivalent of the 16L8 PAL and Figure 3 shows the PALASM equations used to program the PAL.

SOFTWARE DESIGN

The Functional State diagram for the software is shown in Figure 4. An assembly listing of the program is included at the end of this application note. Notes are liberally included in the listing to assist the understanding of program operation. (Figure 7).

Note: In the discussion of the software and operation of this design, it is assumed the reader knows and understands the common "AT" commands. If not, refer to any of a number of source materials devoted to this subject.

There are five main sections to this program. In order of occurrance in the listing, they are:

Part 1: Baud rate and protocol determination	($F800–$F998)
Part 2: Reading in the command string	($F999–$F9E8)
Part 3: Processing the command string	($F9E9–$FA1B)
Part 4: Command definitions	($FB1E–$FEBA)
Part 5: Interrupt Service Routine	($FF57–$FF79)

Most of the software operates in the Command Mode, responding to inputs from the host system. The Command Mode section includes Parts 1–5, with the exception of the <CR> (Carriage Return) command in Part 4. The remaining sections of Figure 4 lie within the definition of the <CR> command. Figure 5 shows the flow chart of the Command Mode section.

After initialization, the software loops in Part 1, waiting for an attention code ("AT" or "A/") or for the phone to ring. Any system designed to run the "AT" command set must be able to operate at either 300 or 1200 (or, in this case, 2400) baud, using 7 or 8 bits per word, with even, odd or no parity, switching from one mode to another automatically. The method used to do this is outlined on page 0004 of the software listing, Figure 7. Figure 6 diagrams the bit patterns of the characters "A", "T" and "/" and shows how the relationship of bits 8 and 9 of each character determine the characteristics of the serial protocol.

**PAL and PALASM are registered trademarks of Monolithic Memories, Inc.*

In Part 2 the serial communications protocol as been established. ASCII command characters are read in one at a time and stored in a buffer (INBUFF), excepting <SPACE> and non-<CR> control characters, until a <CR> character is entered. Should more than 40 characters be received, a flag (BUFFLG) is set, indicating an error condition.

When the program recognizes a <CR> character it stops accepting commands and goes directly to command execution (Part 3). It processes each command in sequence until an "A", "O", "Z" or <CR> command. "A" and "O" forces an attempt to go on-line (examine RSLD/ for carrier signal and go on-line if present, otherwise it will go back to Command Mode.) "Z" performs a soft reset and returns to Command Mode. <CR> is the usual end to each command string. This is where error conditions are reported, on-line data are handled, and a return to Command Mode from Data Mode is made upon recognition of a valid escape code sequence.

This intelligent modem will recognize that it is being called only while it is waiting for an attention code (at label L1). If the PA0 flag goes high at this point, indicating the phone is "ringing", the program branches to RING then jumps to RINGNG, where a determination is made whether to answer the phone or not. If not ringing, it goes back to waiting for "AT" or "A/". If it is ringing, it then bypasses Part 2 and Part 3 and attempts to go to the Data Mode (depending on presence of a carrier signal) by executing the "A" (Answer) command.

When this modem is called, an assumption is made as to the proper baud rate and serial protocol, that the values determined by the most recent attention code are still valid. Should a call be received before the first attention code was entered, it defaults to 1200 baud, 8 bits, no parity. The call is not answered in this case, since S0 was not set to a non-zero value, however, the "RING" message is sent out to the host system at this rate.

Part 4 comprises the coding of each "AT" command. All but AAA, OOO, ZZZ and CR end in an RTS instruction, returning control back to the command string processor at NXTCMD. AAA and OOO transfer control directly to CR in an attempt to go on-line. CR always returns to Part 1 of the program, and ZZZ always jumps to the Power-On-Reset address at RESET.

Part 5 is divided into two parts: signal processing and delay timing (execution of one or the other is determined by the value of the INTFLG flag). The signal processing takes place while waiting for an attention code, echoing (if enabled) the incoming bits back to the host system, and is described on page 0004 of Figure 7. Delay timing is selected just before Part 2 (or if a call is answered). The delay routine is designed to allow a variable number of precise time delays, where the actual time interval is determined by the routine needing the delay. For example, the "," (comma) command tells the modem to do nothing for S8 number of seconds, so one time interval would be 1 second. The Carrier Detect Response time interval is 1/10 second and the Escape Code Guard time interval is 20 ms, each requiring different values for CNTR-B and DELAYT.

General notes on the software:

Liberal use was made of the available RAM for 1-bit flags and variables, primarily because no premium is placed on RAM space in this design. These could be compressed into byte-sized entities should more space be required.

No attempt was made to provide status information via the S13, S14, S15 or S17 pseudo-registers. These could be added if necessary.

The S10 (Loss of Carrier) and S11 (Touch-Tone) delay times are limited to 400 ms and 70 ms, respectively, due to the design of the R2424 Modem.

The "H2" command does nothing additional to the "H1" command since the R2424 Modem does not have an auxiliary relay.

This program implements the concepts of modularity and structured programming as much as was practical for assembly-level code. This allows easy customization and tailoring for a particular application. There are deviations from this guideline, however, so modifications should be made with this in mind.

Expansion might include detection of Dial tone, Ringing and Busy signals using the TONE bit of RCV8. For example, if a Busy signal is detected, the program could automatically re-dial after a suitable delay time.

Unlike some commercial intelligent modems, no default switches or status LEDs were implemented in this design, nor was an actual speaker circuit included (though a control line for one, SPKR-ON/, is provided) in the interests of simplicity.

Finally, this design has not been thoroughly tested to meet the "AT" specifications. This application note is presented only as a guide on how to control a R2424 Modem with a R6500/11 single-chip microcomputer.

SERIAL INTERFACE

The modem system supports the following data rates and asynchronous serial protocols:

Baud: 300, 1200 or 2400
No. of data bits: 7 or 8
No. of stop bits: 1 or 2
Parity: Odd, even or none

The baud rate is determined by the width of the start bit.

The number of data bits, the number of stop bits and parity type are determined by examining bit 8 and, sometimes, bit 9 in two consecutive data words comprising an "AT" or "A/" command. Figure 6 shows the serial stream waveforms for the "AT" or "A/" commands along with the message bits positions. Table 2 lists the six selectable protocol configurations.

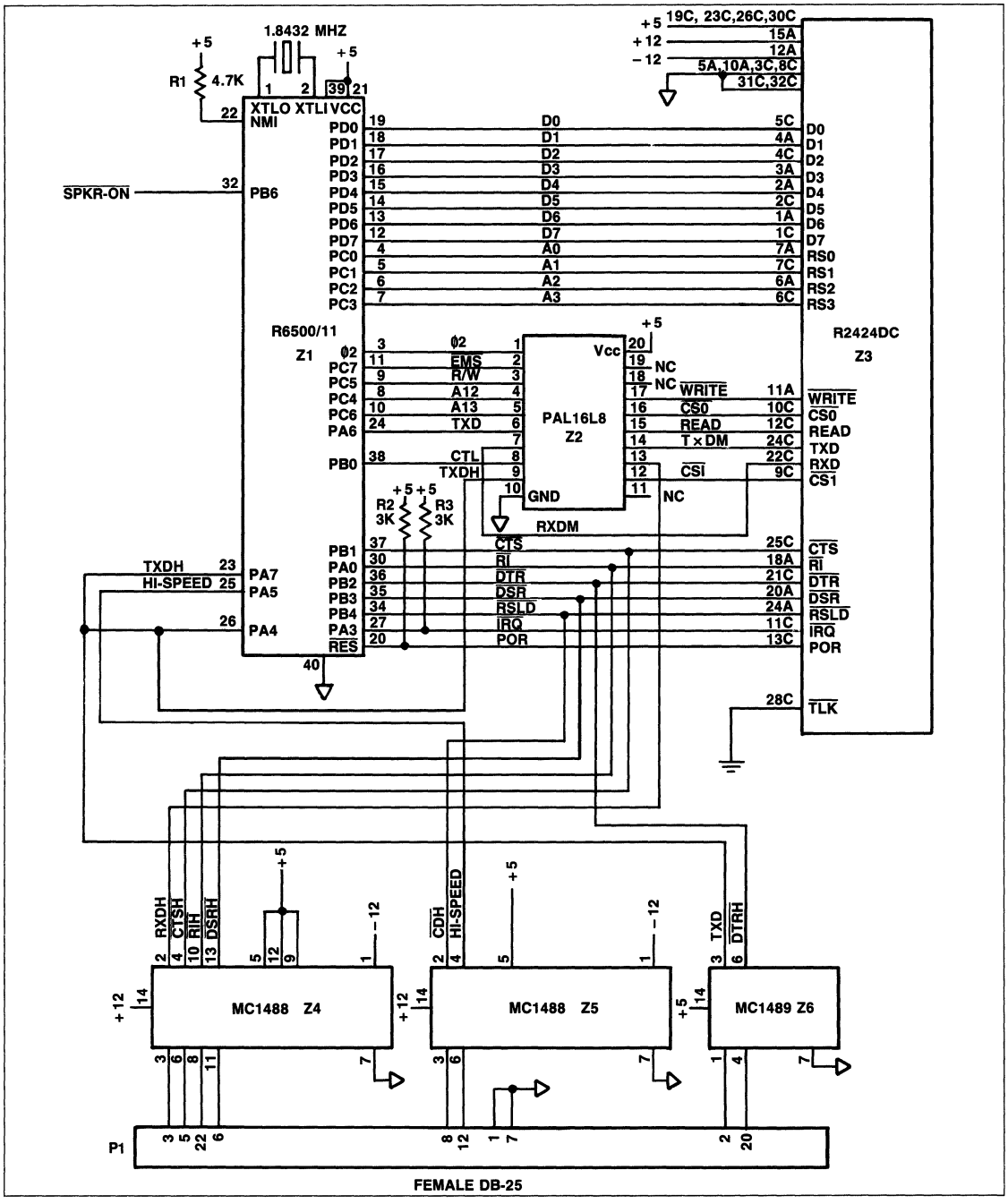


Figure 1. R6500/11-R2424 Intelligent Modem Schematic

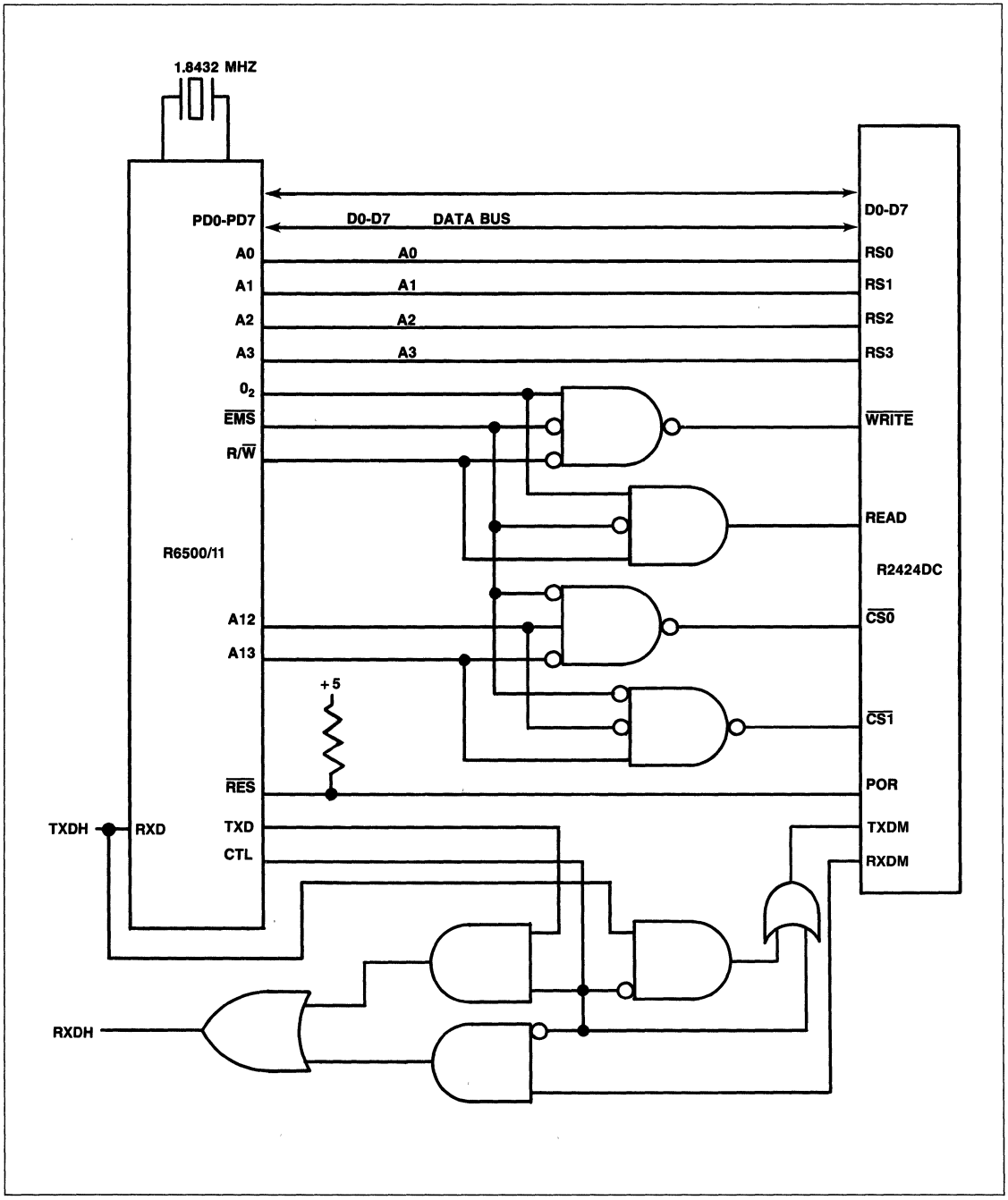


Figure 2. Logic for 16L8 PAL (Z2)

```
PAL16L8
MODEM
MODEM CONTROL CIRCUIT
JW HANCE
P2 EMS RW A12 A13 TXD RXDM CTL TXDH GND NC
/CS1 RXDH TXDM READ /CSO /WRITE NC NC VCC
IF (VCC) WRITE = P2 * /EMS * /RW
IF (VCC) /READ = /P2 + EMS + /RW
IF (VCC) CS0 = /EMS * A12 * /A13
IF (VCC) CS1 = /EMS * /A12 * A13
IF (VCC) /RXDH = /TXD * CTL + /TXD * /RXDM + /CTL * /RXDM
IF (VCC) /TXDM = /CTL * /TXDH
*END*
```

Figure 3. PAL16L8 (Z2) PALASM Equations

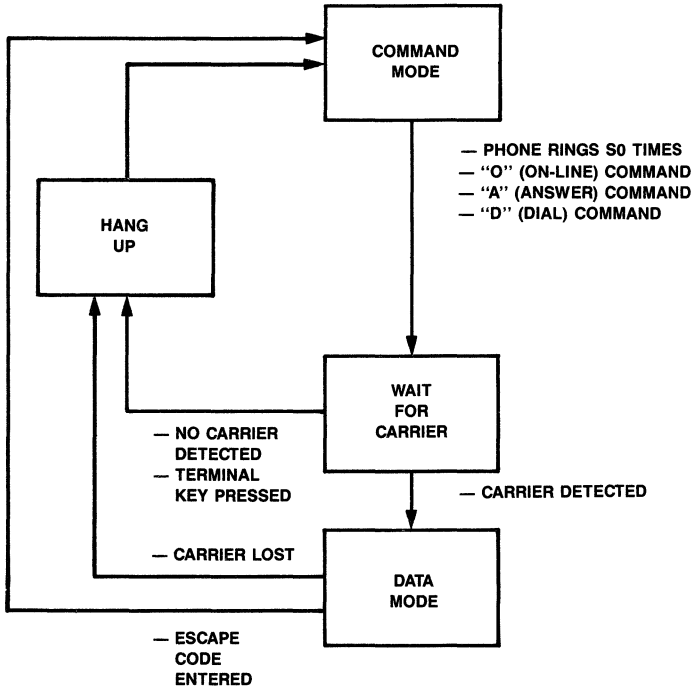


Figure 4. Modem Software Functional State Diagram

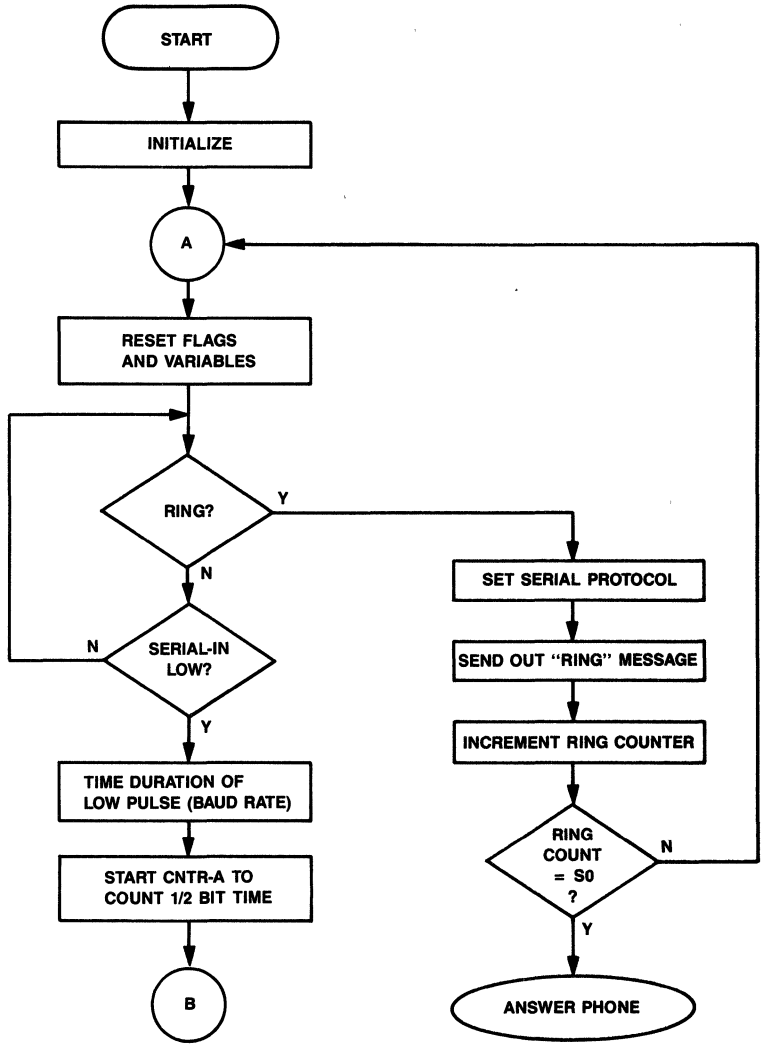


Figure 5. Command Mode Flowchart

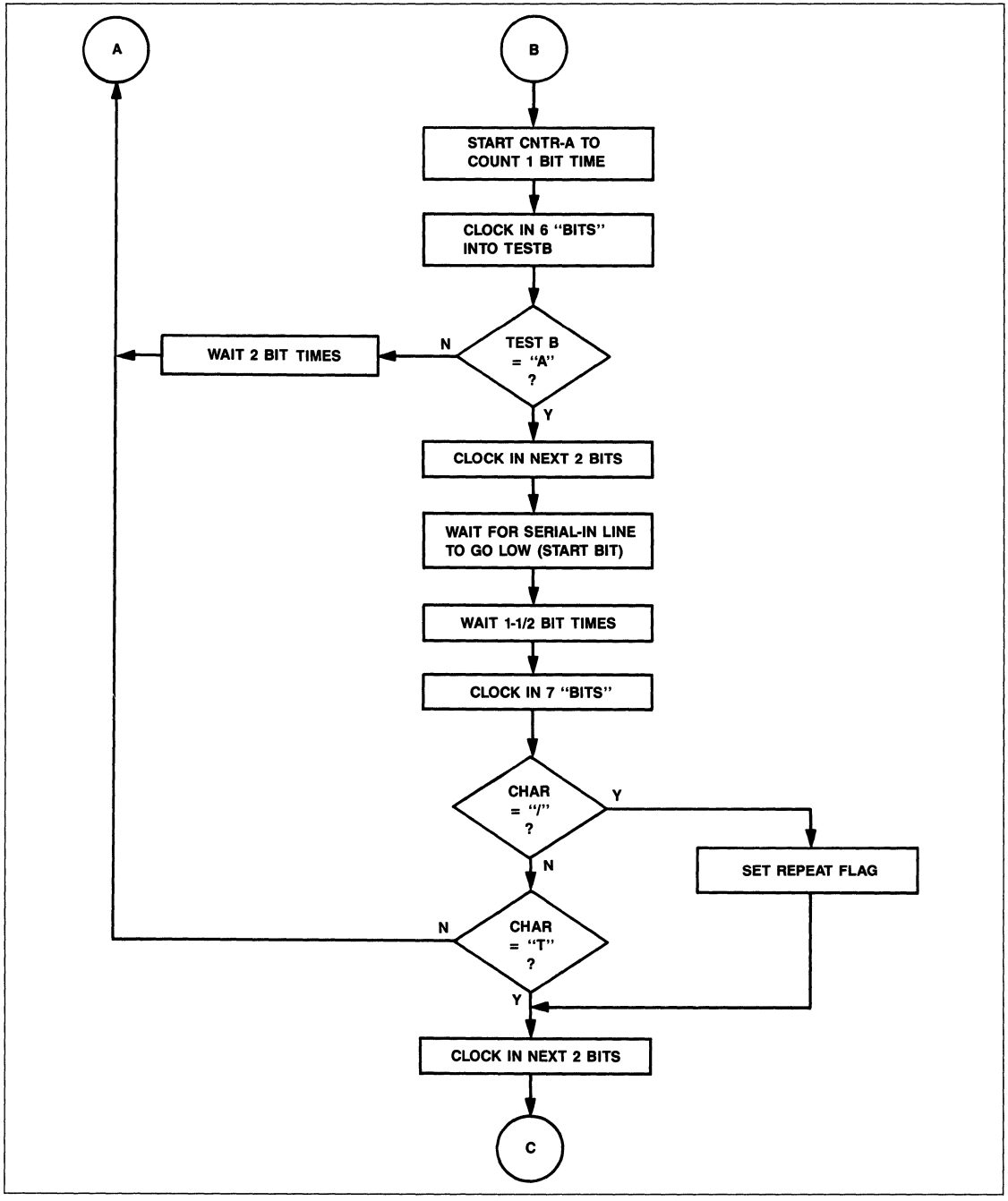


Figure 5. Command Mode Flowchart (Continued)

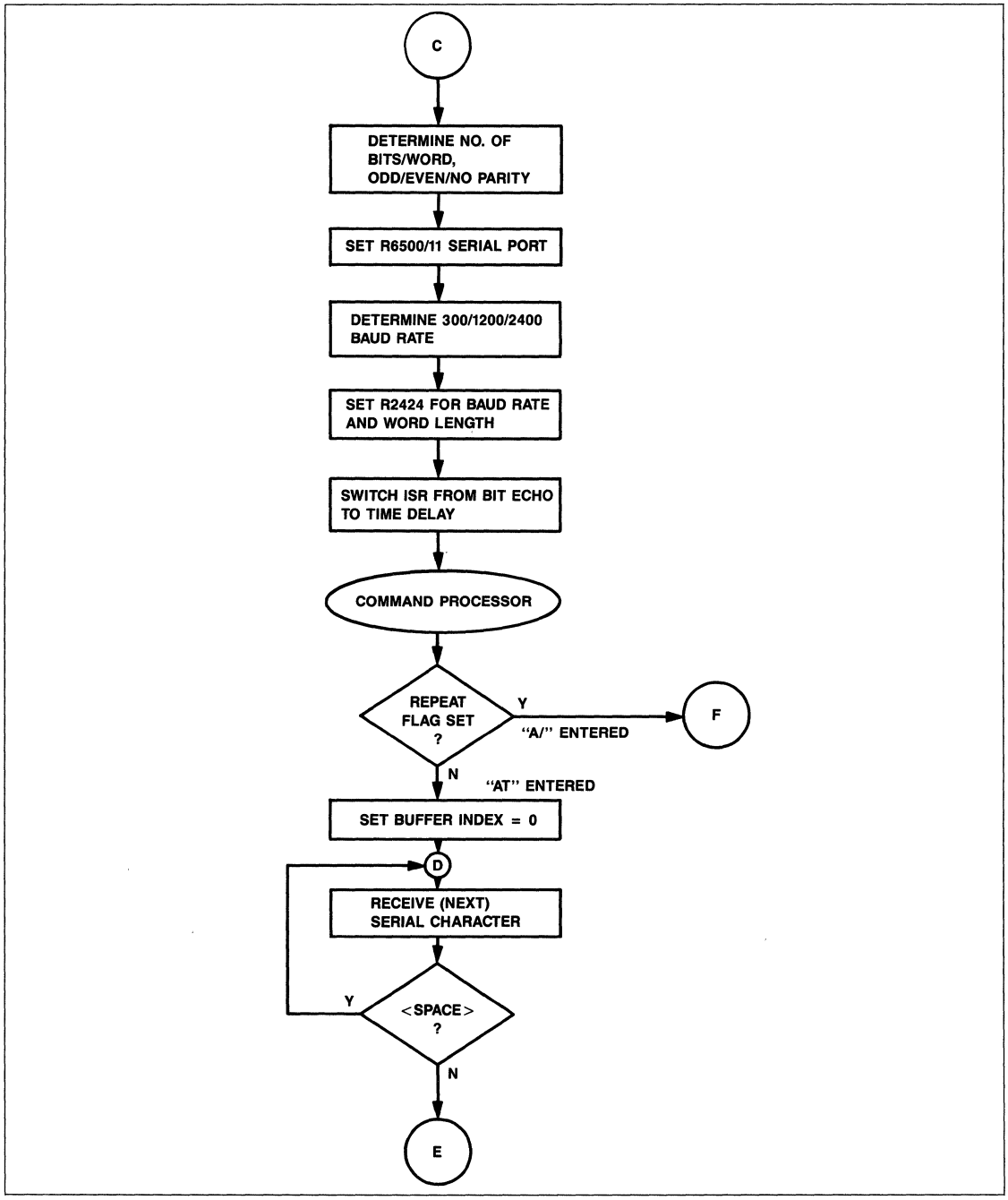


Figure 5. Command Mode Flowchart (Continued)

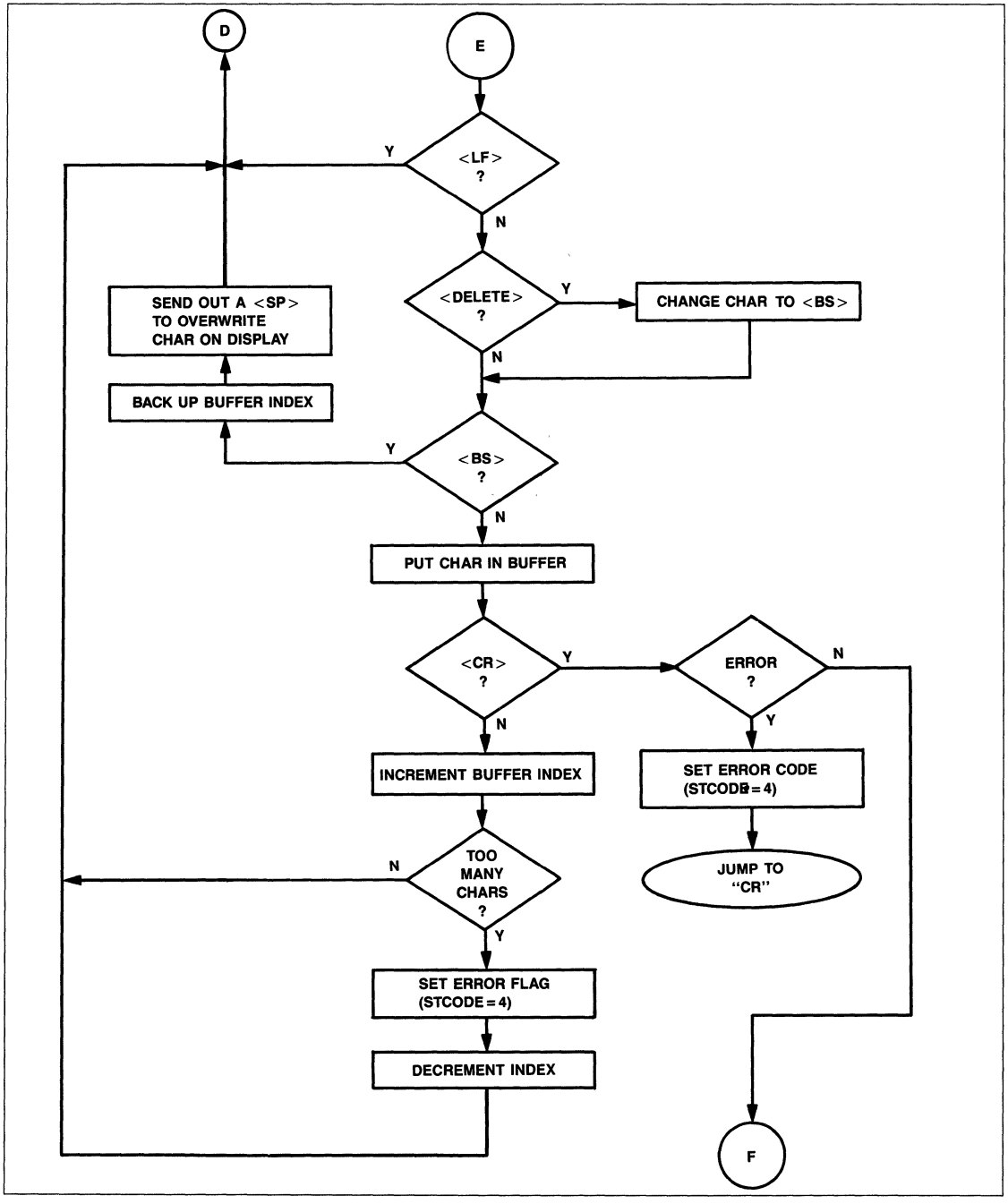


Figure 5. Command Mode Flowchart (Continued)

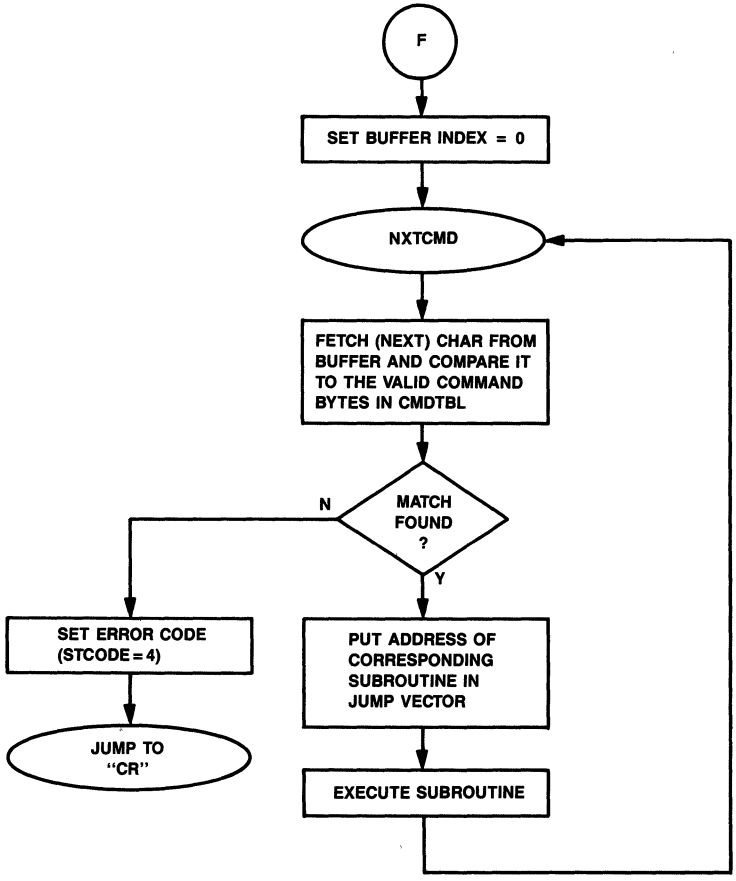


Figure 5. Command Mode Flowchart (Continued)

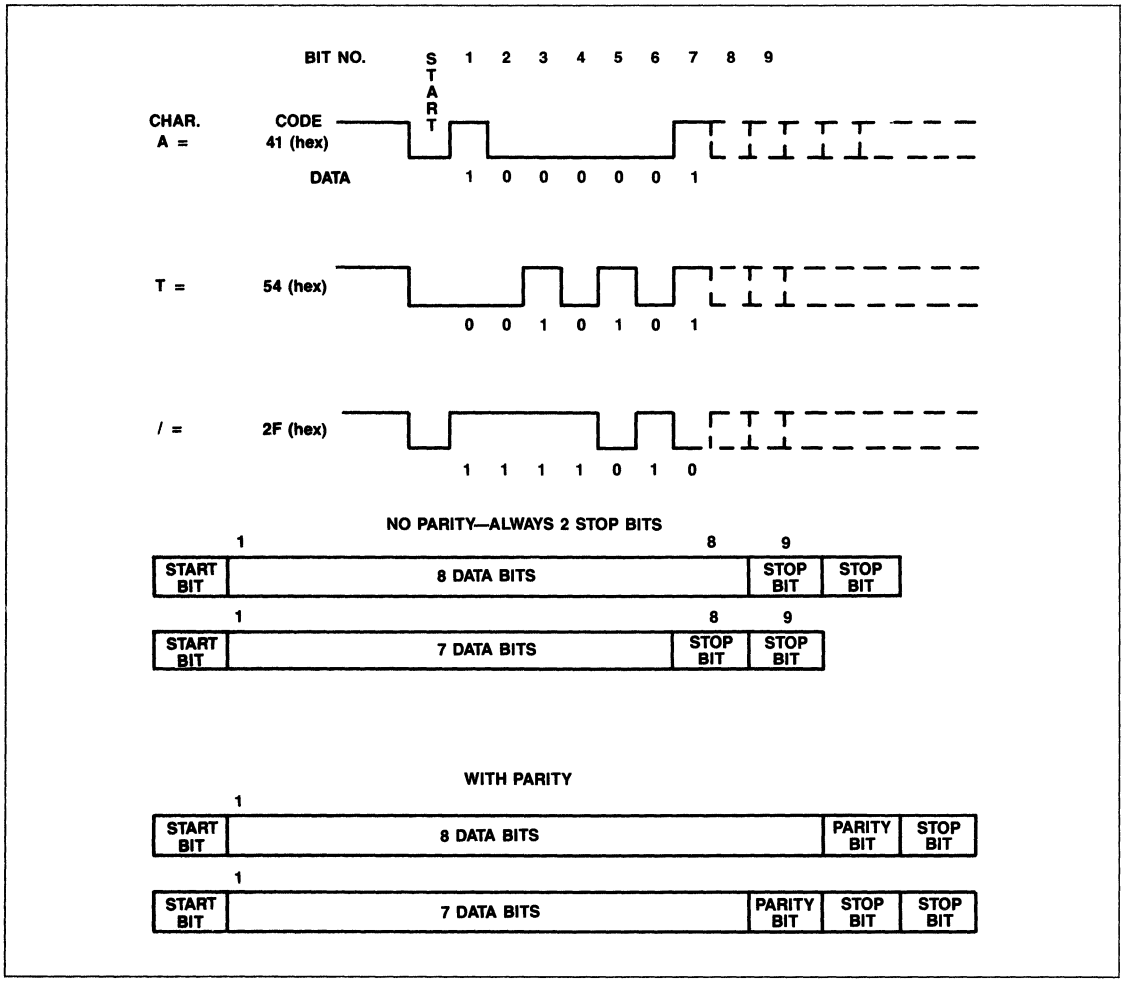


Figure 6. Serial Protocol Formats Data Length

Table 2. Selectable Serial Protocol Configurations

Command Word No.	Command ASCII Char. (Bits 1–7)	Command Word Bit 8	Command Word Bit 9	Message Protocol
1 2	A T or /	1 0	— —	Odd parity, 7 data bits, 2 stop bits
1 2	A T or /	0 1	— —	Even parity, 7 data bits, 2 stop bits
1 2	A T or /	1 1	— —	No parity, 7 data bits, 2 stop bits
1 2	A T or /	0 0	1 0	Odd parity, 8 data bits, 1 stop bit
1 2	A T or /	0 0	0 1	Even parity, 8 data bits, 1 stop bit
1 2	A T or /	0 0	1 1	No parity, 8 data bits, 2 stop bits

```
                                                        PAGE 0001

0001                ; THIS IS A PROGRAM FOR AN R6500/11 ACTING AS AN INTERFACE
0002                ;  BETWEEN A HOST COMPUTER WITH A SERIAL PORT AND AN R2424
0003                ;  MODEM.  IT IS DESIGNED TO RUN THE "AT" COMMAND SET.
0004
0005                ; =========================================================
0006
0007
0008                      .OPT   LLEN=132
0009                      .OPT   IVB
0010
0011 0000                 *=$0000
0012
0013 0000           PA    *=*+1
0014 0001           PB    *=*+1
0015
0016 0002                 *=$11
0017
0018 0011           IFR   *=*+1
0019 0012           IER   *=*+2
0020 0014           MCR   *=*+1
0021 0015           SCCR  *=*+1
0022 0016           SCSR  *=*+1
0023 0017           STDR  *=*+1
0024 0017           SRDR  =     STDR
0025 0018           CNTACL *=*+1
0026 0019           CNTAH *=*+1
0027 001A           CNTAL *=*+1
0028
0029 001B                 *=*+1
0030 001C           CNTBCL *=*+1
0031 001D           CNTBHC *=*+1
0032 001E           CNTBHL *=*+1
0033
0034 001F                 *     = $40             ; RAM VARIABLES
0035
0036 0040           DEFPRO *=*+1                  ; DEFAULT SERIAL PROTOCOL FOR AUTO-ANSWER COMMUNICATIONS
0037 0041           BAUD   *=*+1                  ; INDICATOR OF PRESENT TERMINAL BAUD RATE ( 3/12/24 )
0038 0042           BDRATL *=*+1                  ; LOW PART OF BAUD RATE, AS DETERMINED BY CNTR-A
0039 0043           BDRATH *=*+1                  ; HIGH PART OF BAUD RATE
0040 0044           DELAYC *=*+1                  ; IRQ COUNTER: COUNTS NUMBER OF TIMES IRQ ROUTINE IS CALLED
0041 0045           DELAYT *=*+1                  ; SET TO THE # OF TIMES THE IRQ ROUTINE IS TO BE CALLED
0042 0046           DELAYS *=*+1                  ; SET TO THE NUMBER OF SECONDS TO WAIT FOR
0043 0047           TESTB  *=*+1                  ; CONTAINS THE 7 SAMPLE BITS FROM THE SERIAL-IN LINE
0044 0048           ABIT8  *=*+1                  ; WHEN THE 7 BITS CLOCKED INTO "TESTB" MATCH THE "A" CHAR,
0045 0049           ABIT9  *=*+1                  ;   THE NEXT 2 BITS ARE CLOCKED IN AND STORED HERE.
0046 004A           TBIT8  *=*+1                  ; WHEN THE 7 SAMPLE BITS IN "TESTB" MATCH THE "T" CHAR, THE
0047 004B           TBIT9  *=*+1                  ;  NEXT 2 BITS ARE STORED IN "TBIT8" AND "TBIT9".
0048 004C           INBUFF *=*+40                 ; CONTAINS THE COMMAND STRING AS ENTERED FROM THE HOST SYS.
0049 0074           REPFLG *=*+1                  ; WHEN "A/" IS ENTERED AS COMMAND, THIS FLAG IS SET.
0050 0075           BUFFLG *=*+1                  ; THIS FLAG IS SET WHEN TOO MANY COMMAND CHARS ARE ENTERED
0051 0076           DILFLG *=*+1                  ; IS SET TO INDICATE ANY FOLLOWING NUMBERS ARE DIAL DIGITS
0052 0077           REVFLG *=*+1                  ; NORMAL ($00) OR REVERSE ($80) DIAL
0053 0078           IRQFLG *=*+1                  ; $00 ==> IRQ IS SERIAL-IN TIMER: $80 ==> IRQ IS DELAY TIMER
0054 0079           ECHOFG *=*+1                  ; $00 ==> DO NOT ECHO COMMAND CHARS: $80 ==> ECHO CHARS
```

Figure 7. Software Assembly Listing

```
0055 007A          DUPLEX *=*+1          ; ECHO CHARS WHILE IN DATA MODE (ON-LINE) : 0=NO, $80=YES
0056 007B          RSLTFG *=*+1          ; $00 ==> SEND OUT RESULT PROMPT: $80 ==> DON'T SEND IT OUT.
0057 007C          SPKRFG *=*+1          ; USED TO CONTROL THE EXTERNAL SPEAKER
0058 007D          STCODE *=*+1          ; RESULT (STATUS) CODE ( 0-4,5 )
0059 007E          VCODE  *=*+1          ; SEND RESULT PROMPT IN NUMERIC ( $00 ) OR VERBAL ( $80 ) FORM
0060 007F          XCODE  *=*+1          ; ALLOW EXTENDED RESULT CODES ?  ( $00 = NO / $80 = YES )
0061 0080          WAITFG *=*+1          ; "WAIT-FOR-CARRIER ?" FLAG  (0 = NO / $80 = YES )


                                                    PAGE 0002

0062 0081          WAITC  *=*+1          ; INDICATES "WAIT-FOR-CARRIER" TIME INTERVAL HAS ELAPSED
0063 0082          ESCCNT *=*+1          ; ESCAPE CODE COUNTER
0064 0083          SSETFG *=*+1          ; INDICATES S-REG POINTER HAS BEEN SET TO SOME VALUE
0065 0084          SREGP  *=*+2          ; CONTAINS THE INDIRECT POINTER TO ONE OF THE S-REGISTERS
0066
0067                                     ;  THE FOLLOWING 17 BYTES CONTAIN THE VALUES FOR THE S-REGISTERS
0068
0069 0086          S0     *=*+1          ; RING TO ANSWER ON
0070 0087          S1     *=*+1          ; COUNTS THE NUMBER OF RINGS
0071 0088          S2     *=*+1          ; ESCAPE CODE CHARACTER
0072 0089          S3     *=*+1          ; CARRIAGE RETURN CHAR
0073 008A          S4     *=*+1          ; LINE FEED CHAR
0074 008B          S5     *=*+1          ; BACKSPACE CHAR
0075 008C          S6     *=*+1          ; WAIT-TIME FOR DIAL TONE
0076 008D          S7     *=*+1          ; WAIT-TIME FOR CARRIER (AFTER DIALING OR ANSWERING )
0077 008E          S8     *=*+1          ; PAUSE-TIME ( USED BY "COMMA" COMMAND )
0078 008F          S9     *=*+1          ; CARRIER-DETECT RESPONSE TIME
0079 0090          S10    *=*+1          ; DELAY-TIME BETWEEN LOSS OF CARRIER AND "HANG UP"
0080 0091          S11    *=*+1          ; DURATION AND SPACING OF TOUCH TONES
0081 0092          S12    *=*+1          ; ESCAPE CODE GUARD-TIME
0082 0093          S13    *=*+1          ; UART STATUS REGISTER
0083 0094          S14    *=*+1          ; OPTION REGISTER
0084 0095          S15    *=*+1          ; FLAG REGISTER
0085 0096          S16    *=*+1          ; 1=ENTER SELF-TEST / 0=STOP SELF-TEST
0086 0097          S17    *=*+1          ; GENERAL SYSTEM STATUS
0087
0088 0098          NUM    *=*+3          ; WORK AREA FOR ASCII-TO-HEX AND HEX-TO-ASCII CONVERSION
0089 009B          CMDVEC *=*+2          ; INDIRECT POINTER TO THE NEXT COMMAND TO BE EXECUTED
0090 009D          TEMP   *=*+1          ; TEMPORARY STORAGE BYTE

                                                    PAGE 0003

0092 1000          RCV    =      $1000   ; BASE ADDRESS FOR RECEIVER REGISTERS
0093
0094 009E                 *=     RCV+2
0095 1002          RCV2   *=*+6
0096 1008          RCV8   *=*+1
0097 1009          RCV9   *=*+1
0098 100A          RCVA   *=*+1
0099 100B          RCVB   *=*+1
0100 100C          RCVC   *=*+1
0101 100D          RCVD   *=*+1
0102 100E          RCVE   *=*+1
```

```
0103 100F                RCVF   *=*+1
0104
0105 2000                XMT    =$2000                ; BASE ADDRESS FOR THE TRANSMITTER REGISTERS
0106
0107 1010                       *=     XMT
0108 2000                XMT0   *=*+2
0109 2002                XMT2   *=*+6
0110 2008                XMT8   *=*+1
0111 2009                XMT9   *=*+1
0112 200A                XMTA   *=*+1
0113 200B                XMTB   *=*+1
0114 200C                XMTC   *=*+1
0115 200D                XMTD   *=*+1
0116 200E                XMTE   *=*+1
0117 200F                XMTF   *=*+1
0118
0119 0010                DLYHIB =      $10             ; DELAY-TIME FACTOR
0120 E09C                DLYTIM =      $E09C           ; ( DLYTIM * DLYHIB @ 920KHZ = 1 SEC. )
0121 6760                TENTHD =      $6760           ; ( TENTHD * DLYHIB @ 920KHZ = 1/10 SEC. )
0122 0001                ESCDLY =      1
0123 479C                ESCTIM =      $479C           ; 1 COUNT FOR "ESCAPE" CODE GUARD TIME ( 20MS )
0124
0125 00BF                BAUD3  =      $00BF           ; CNTR-A VALUE FOR SERIAL-I/O BAUD RATE OF 300 BAUD ( @ 920KHz
0126 002F                BAUD12 =      $002F           ;  VALUE FOR 1200 BAUD
0127 0017                BAUD24 =      $0017           ;  VALUE FOR 2400 BAUD
0128
0129 0021                NUMCMD =      33              ; NUMBER OF COMMANDS IN "CMDTBL"
```



```
0131 2010                       *=$F800
0132
0133 F800  A2 FF         RESET LDX    #$FF            ; INITIALIZE THE R6500/11
0134 F802  9A                   TXS
0135 F803  D8                   CLD
0136 F804  78                   SEI
0137 F805  A9 A0                LDA    #$A0           ; SET UP MODE REGISTER FOR ABBREVIATED BUS
0138 F807  85 14                STA    MCR
0139
0140 F809  20 BE FA             JSR    INITSW         ; INITIALIZE VARIABLES, ETC.
0141
0142 F80C  87 01                SMB    0,PB           ; CTL = 0  ( TRANSMIT TO MODEM )
0143 F80E  17 01                RMB    1,PB           ; CTS/ = 0
0144 F810  27 01                RMB    2,PB           ; DTR/ = 0  ( ACTIVE )
0145 F812  D7 01                SMB    5,PB           ; HISPEED = 1 ( HIGH SPEED )
0146 F814  E7 01                SMB    6,PB           ; DISABLE SPEAKER
0147
```

```
0148                    ; ******************************************************************
0149                    ;
0150                    ;       FIRST CHARS ACROSS SHOULD BE "AT" OR ""A/".  ASSUME AN "A"
0151                    ;  IS THE FIRST CHAR:  BY TIMING THE DURATION OF THE FIRST LOW
0152                    ;  PULSE (START BIT), THE BAUD RATE IS DETERMINED.  USING THIS AS
0153                    ;  THE WIDTH OF ONE BIT, 7 SAMPLES ARE MADE OF THE SERIAL INPUT LINE
0154                    ;  AT ONE-BIT INTERVALS, WITH EACH "BIT" SHIFTED INTO A TEST BUFFER
0155                    ;  ( "TESTB" ).  AFTER 7 SAMPLES, THE TEST BUFFER IS RIGHT-JUSTIFIED
0156                    ;  (SHIFTED RIGHT ONE MORE TIME) AND COMPARED TO THE ASCII "A" CHAR.
0157                    ;  IF A MATCH IS NOT MADE, WE WAIT 2 MORE "BITS", TIME THE NEXT LOW PULSE
0158                    ;    AND CLOCK IN 7 MORE BITS.
0159                    ;  IF A MATCH IS FOUND, AN "A" CHAR IS ASSUMED TO HAVE BEEN READ IN
0160                    ;  AND THE NEXT TWO BITS ARE SAVED FOR FUTURE DETERMINATION OF
0161                    ;  TRANSMISSION PROTOCOL (PARITY, BITS/CHAR).  THE NEXT CHAR IS
0162                    ;  CLOCKED IN AND COMPARED TO "T" AND "/".  IF A MATCH IS FOUND THEN
0163                    ;  THE PROTOCOL IS DETERMINED AND THE COMMAND BYTES FOR THE MODEM
0164                    ;  ( IF ANY ) ARE READ IN AND PROCESSED.
0165                    ;       IF A MATCH IS NOT FOUND FOR "AT" OR "A/" THEN WE START OVER AGAIN
0166                    ;  LOOKING FOR AN "A" CHAR.
0167                    ;       MEANWHILE, IF CHARACTER ECHOING HAS BEEN ENABLED ( AND BY DEFAULT
0168                    ;  IT IS ), TIMER B IS GENERATING INTERRUPTS AT A FREQUENCY SLIGHTLY
0169                    ;  GREATER THAN TWICE THE 2400 BAUD ( MAXIMUM ALLOWABLE BAUD RATE ) FREQUENCY.
0170                    ;  THE INTERRUPT ROUTINE SAMPLES THE LEVEL OF THE SERIAL INPUT LINE AND SETS
0171                    ;  THE SERIAL OUTPUT LINE TO MATCH.  THIS HAS THE EFFECT OF BLINDLY ECHOING
0172                    ;  INCOMING CHARACTERS BACK TO THE HOST COMPUTER.  THIS WILL BE DONE UNTIL
0173                    ;  "AT" OR "A/" HAS BEEN RECOGNIZED, AT WHICH POINT THE IRQ IS DISABLED
0174                    ;  AND CHARACTERS ARE ECHOED BACK AS CHARACTERS, NOT AS BITS.
0175
0176 F816  A9 00       RESTRT LDA   #00               ; DISABLE RECEIVER AND TRANSMITTER
0177 F818  85 15            STA   SCCR
0178 F81A  85 74            STA   REPFLG              ; CLEAR OUT WORKING VARIABLES
0179 F81C  85 48            STA   ABIT8
0180 F81E  85 49            STA   ABIT9
0181 F820  85 4A            STA   TBIT8
0182 F822  85 4B            STA   TBIT9
0183 F824  85 47            STA   TESTB
0184 F826  85 76            STA   DILFLG              ; PREVENT NUMBERS FROM DIALING UNTIL "DIAL" COMMAND
0185 F828  85 80            STA   WAITFG
0186 F82A  85 75            STA   BUFFLG
0187 F82C  85 7D            STA   STCODE              ; ASSUME "OK" -- STCODE WILL BE RESET IF A PROBLEM ARISES
0188 F82E  AD 0D 10         LDA   RCVD                ; SET "LCD" BIT
0189 F831  09 04            ORA   #$04
0190 F833  8D 0D 10         STA   RCVD
0191 F836  20 D7 FD         JSR   NEWCR               ; UPDATE RECEIVER REGISTER
```

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```
0192 F839  07 10            RMB   0,IFR-1             ; CLEAR "RING" FLAG BIT FROM FLAG REGISTER
0193 F83B  A9 03            LDA   #03                 ; CNTR A = PULSE WIDTH TIMER
0194 F83D  05 14            ORA   MCR
0195 F83F  85 14            STA   MCR
0196 F841  7F 79 0C         BBR   7,ECHOFG,NOIRQ      ; NO ECHO IF FLAG TURNED OFF
0197 F844  A9 B0            LDA   #$B0                ; START TIMER B TO PERIODICALLY SAMPLE
0198 F846  85 1C            STA   CNTBCL              ;  THE SERIAL INPUT LINE AND ECHO BACK
```

```
0199 F848  A9 00          LDA   #00             ;  THE SAME LOGIC LEVEL ON THE OUTPUT
0200 F84A  85 1E          STA   CNTBHL          ;  LINE.
0201 F84C  D7 12          SMB   5,IER
0202 F84E  77 7B          RMB   7,IRQFLG
0203 F850  A9 FF    NOIRQ LDA   #$FF
0204 F852  A8             TAY
0205 F853  85 18          STA   CNTACL          ; READY CNTR A FOR PULSE-WIDTH MEASUREMENT
0206 F855  84 1A          STY   CNTAL
0207 F857  8F 11 50 L1    BBS   0,IFR,RING      ; IF PHONE IS RINGING, GO SEE IF IT'S TIME TO ANSWER IT
0208 F85A  FF 00 FA       BBS   7,PA,L1         ; WAIT FOR RECEIVE LINE TO GO LOW
0209 F85D  67 00          RMB   6,PA            ; SET SERIAL-OUT LINE LOW TO MATCH
0210 F85F  7F 00 FD L2    BBR   7,PA,L2         ; NOW WAIT FOR IT TO GO BACK HIGH ( THIS SHOULD
0211                                            ;   BE THE START BIT OF "A" )
0212 F862  58             CLI                   ; ALLOW TIMER-B IRQ
0213 F863  A5 19          LDA   CNTAH           ; GET PULSE WIDTH COUNT
0214 F865  49 FF          EOR   #$FF            ; INVERT IT
0215 F867  85 43          STA   BDRATH          ; AND SAVE IT
0216 F869  A8             TAY
0217 F86A  A5 18          LDA   CNTACL
0218 F86C  49 FF          EOR   #$FF
0219 F86E  AA             TAX
0220 F86F  A9 FC          LDA   #$FC            ; SET CNTR A = TIME INTERVAL COUNTER
0221 F871  25 14          AND   MCR
0222 F873  85 14          STA   MCR
0223 F875  86 42          STX   BDRATL          ; SAVE LOW BYT OF COUNT
0224 F877  86 18          STX   CNTACL          ; SET LOW BYTE OF BAUD TIMER
0225 F879  98             TYA                   ; SET UP COUNTER FOR 1/2 BIT WIDTH, TO
0226 F87A  4A             LSR   A               ;  POSITION SERIAL LINE SAMPLES APPROX.
0227 F87B  85 1A          STA   CNTAL           ;  IN MIDDLE OF BIT.
0228 F87D  4F 11 FD L3    BBR   4,IFR,L3        ; WAIT FOR TIMER
0229 F880  84 1A          STY   CNTAL           ;  NOW START TIMER A WITH FULL DELAY  ( ALSO CLEARS FLAG )
0230 F882  A5 00          LDA   PA              ; GET VALUE OF SERIAL BIT (SHOULD BE HIGH)
0231 F884  0A             ASL   A               ; ROTATE RECEIVE BIT VALUE INTO CARRY BIT
0232 F885  66 47          ROR   TESTB           ;  AND ROTATE IT INTO TEST BYTE
0233 F887  A2 06          LDX   #06             ; CLOCK IN 6 MORE SERIAL BITS
0234 F889  4F 11 FD L4    BBR   4,IFR,L4        ; WAIT FOR ONE BIT TIME
0235 F88C  A5 18          LDA   CNTACL          ; CLEAR FLAG
0236 F88E  A5 00          LDA   PA              ; GET SERIAL BIT
0237 F890  0A             ASL   A               ; AND ROTATE IT INTO TESTB
0238 F891  66 47          ROR   TESTB
0239 F893  CA             DEX                   ; CLOCKED IN 6 BITS YET ?
0240 F894  D0 F3          BNE   L4              ; NO ==> GET NEXT BIT
0241 F896  A5 47          LDA   TESTB           ; YES==> IS CHAR AN "A" ?
0242 F898  4A             LSR   A               ;  ( RIGHT-JUSTIFY TEST CHAR )
0243 F899  C9 41          CMP   #'A'
0244 F89B  F0 10          BEQ   FOUNDA          ; YES==> CHECK NEXT CHAR FOR "T" OR "/"
0245 F89D  98             TYA                   ; NO ==> WAIT 2 BIT TIMES
0246 F89E  0A             ASL   A               ;  THEN JUMP TO "RESTART"
0247 F89F  85 1A          STA   CNTAL           ;  TO READ IN ANOTHER TEST CHAR
0248 F8A1  4F 11 FD L4A   BBR   4,IFR,L4A       ; WAIT FOR TIMER
0249 F8A4  7F 00 FD L5    BBR   7,PA,L5         ; THEN MAKE SURE INPUT LINE IS HIGH
0250 F8A7  4C 16 F8 GO2RES JMP  RESTRT          ; ... AND READ IN ANOTHER 7 BITS
0251
0252 F8AA  4C 1C FA RING  JMP   RINGNG          ; CHECK RING COUNT.  IF PHONE HAS RUNG ENOUGH TIMES
```

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```
0253                                                    ;  ( AS DETERMINED BY S-REG 0 ) THEN ANSWER IT.
0254                                                    ;  OTHERWISE, GO BACK TO "RESTART"
0255
0256                    ; FOUND AN "A" CHAR.  NOW SAVE NEXT TWO BITS FOR PROTOCOL CHECK,
0257                    ;   THEN CHECK FOR "T" OR "/" CHARS.
0258
0259 F8AD  4F 11 FD    FOUNDA BBR    4,IFR,FOUNDA        ; WAIT ONE BIT TIME
0260 F8B0  A5 18               LDA    CNTACL              ; CLEAR FLAG
0261 F8B2  A5 00               LDA    PA                  ; GET BIT
0262 F8B4  0A                  ASL    A
0263 F8B5  66 48               ROR    ABIT8               ; SAVE IT AS BIT 8 OF "A" ( FOR FORMAT CHECKING LATER )
0264 F8B7  4F 11 FD    L6      BBR    4,IFR,L6            ; GET BIT 9  ( WAIT ONE MORE BIT TIME )
0265 F8BA  A5 18               LDA    CNTACL              ; CLEAR FLAG
0266 F8BC  A5 00               LDA    PA
0267 F8BE  0A                  ASL    A
0268 F8BF  66 49               ROR    ABIT9               ; AND SAVE "A" BIT 9
0269 F8C1  7F 00 FD    L7      BBR    7,PA,L7             ; WAIT FOR RECEIVE LINE TO GO HIGH
0270 F8C4  FF 00 FD    L8      BBS    7,PA,L8             ; NOW WAIT FOR IT TO GO LOW ( START BIT )
0271 F8C7  86 47               STX    TESTB               ; RESET "TESTB" FOR "T" AND "/" CHECK
0272 F8C9  98                  TYA                        ; DELAY APPROX. 1/2 BIT TIME
0273 F8CA  4A                  LSR    A                   ;  ( DIVIDE MSB OF DELAY TIME BY 2 )
0274 F8CB  85 1A               STA    CNTAL               ; START TIMER
0275 F8CD  4F 11 FD    L9      BBR    4,IFR,L9            ; WAIT FOR TIMER
0276 F8D0  84 1A               STY    CNTAL               ; RESTART TIMER  ( AND CLEAR FLAG )
0277 F8D2  A2 07               LDX    #07                 ; CLOCK IN 7 BITS ONLY ( OF CHAR FOLLOWING "A" )
0278 F8D4  4F 11 FD    L10     BBR    4,IFR,L10           ; WAIT FOR TIMER
0279 F8D7  A5 1B               LDA    CNTACL              ; CLEAR FLAG
0280 F8D9  A5 00               LDA    PA                  ; GET BIT
0281 F8DB  0A                  ASL    A
0282 F8DC  66 47               ROR    TESTB               ;  AND SHIFT IT IN "TESTB"
0283 F8DE  CA                  DEX                        ; 7 BITS YET ?
0284 F8DF  D0 F3               BNE    L10                 ; NO ==> GET NEXT BIT
0285 F8E1  A5 47               LDA    TESTB               ; YES==> SEE IF THIS CHAR MATCHES "T" OR "/"
0286 F8E3  4A                  LSR    A                   ; ( RIGHT-JUSTIFY CHAR )
0287 F8E4  C9 2F               CMP    #'/'                ; "/" ?
0288 F8E6  F0 07               BEQ    FOUNDS              ; YES==> "A/" CHARS RECEIVED --> FIGURE OUT PROTOCOL
0289 F8E8  C9 54               CMP    #'T'                ; NO ==> "T" ?
0290 F8EA  F0 05               BEQ    FOUNDT              ; YES==> "AT" CHARS RECEIVED --> FIGURE OUT PROTOCOL
0291 F8EC  4C 16 F8            JMP    RESTRT              ; NO ==> START OVER .....
0292
0293 F8EF  F7 74       FOUNDS SMB    7,REPFLG            ; INDICATE REPEAT OF LAST COMMAND STRING
0294
0295 F8F1  4F 11 FD    FOUNDT BBR    4,IFR,FOUNDT        ; WAIT ONE BIT TIME
0296 F8F4  A5 18               LDA    CNTACL              ; CLEAR FLAG
0297 F8F6  A5 00               LDA    PA                  ; SAVE BIT 8
0298 F8F8  0A                  ASL    A
0299 F8F9  66 4A               ROR    TBIT8
0300 F8FB  4F 11 FD    L12     BBR    4,IFR,L12           ; WAIT ONE LAST BIT TIME
0301 F8FE  A5 1B               LDA    CNTACL              ; CLEAR BIT-WIDTH FLAG
0302 F900  A5 00               LDA    PA
0303 F902  0A                  ASL    A                   ; SAVE BIT 9
0304 F903  66 4B               ROR    TBIT9
0305
```

```
0306                    ; BAUD RATE DETERMINED.  NOW FIGURE OUT TRANSMISSION PROTOCOL
0307                    ;   ( NUMBER BITS/CHAR, ODD/EVEN/NO PARITY )
0308
0309 F905  24 49              BIT   ABIT9           ; IS BIT 9 OF "A" = 0 ?
0310 F907  10 14              BPL   EVEN8           ; YES==> PROTOCOL IS 8 BITS/CHAR, EVEN PARITY
0311 F909  24 4B              BIT   TBIT9           ; NO ==> IS BIT 9 OF "T" = 0 ?
0312 F90B  10 16              BPL   ODD8            ; YES==> PROTOCOL IS 8 BITS/CHAR, ODD PARITY
0313 F90D  A5 48              LDA   ABIT8           ; NO ==> ARE EIGHTH BITS OF "A" AND "T"
```



```
0314 F90F  45 4A              EOR   TBIT8           ;        THE SAME ?
0315 F911  F0 1C              BEQ   NOPAR           ; YES==> NO PARITY USED
0316 F913  24 48              BIT   ABIT8           ; NO ==> BIT 8 OF "A" = 0 ?
0317 F915  10 12              BPL   EVEN7           ; YES==> 7 BITS, EVEN PARITY, 2 STOP BITS
0318 F917  A9 C6        ODD7  LDA   #$C6            ; NO ==> 7 BITS, ODD PARITY,  2 STOP BITS
0319 F919  A0 10              LDY   #$10            ; SET VALUE FOR "RCVC"  ( 10 BITS/WORD )
0320 F91B  D0 20              BNE   LABEL1          ; ( BRANCH ALWAYS )
0321 F91D  A9 C3        EVEN8 LDA   #$C3
0322 F91F  A0 18              LDY   #$18            ; SET VALUE FOR "RCVC"  ( 11 BITS/WORD )
0323 F921  D0 1A              BNE   LABEL1          ; ( BRA )
0324 F923  A9 C2        ODD8  LDA   #$C2
0325 F925  A0 18              LDY   #$18            ; SET VALUE FOR "RCVC"  ( 11 BITS/WORD )
0326 F927  D0 14              BNE   LABEL1          ; ( BRA )
0327 F929  A9 C7        EVEN7 LDA   #$C7
0328 F92B  A0 10              LDY   #$10            ; SET VALUE FOR "RCVC"  ( 10 BITS/WORD )
0329 F92D  D0 0E              BNE   LABEL1          ; ( BRA )
0330 F92F  24 48        NOPAR BIT   ABIT8           ; IS BIT 8 OF "A" = 1 ?
0331 F931  30 06              BMI   NOPAR7          ; YES==> 7 BITS, NO PARITY
0332 F933  A9 C0        NOPAR8 LDA  #$C0            ; NO ==> 8 BITS, NO PARITY
0333 F935  A0 10              LDY   #$10            ; SET VALUE FOR "RCVC"  ( 10 BITS/WORD )
0334 F937  D0 04              BNE   LABEL1          ; ( BRA )
0335 F939  A9 C4        NOPAR7 LDA  #$C4
0336 F93B  A0 08              LDY   #$08            ; SET VALUE FOR "RCVC"  ( 9 BITS/WORD )
0337
0338 F93D  85 15        LABEL1 STA  SCCR            ; SET UP SERIAL COMMAND REGISTER FOR
0339 F93F  85 40              STA   DEFPRD          ;   BAUD RATE AND PROTOCOL  [ SAVE PRESENT PROTOCOL ]
0340 F941  A2 04              LDX   #04             ; DIVIDE BIT-WIDTH TIME BY 16
0341 F943  46 43        ROTATE LSR  BDRATH          ;  TO GET BAUD RATE VALUE
0342 F945  66 42              ROR   BDRATL
0343 F947  CA                 DEX
0344 F948  D0 F9              BNE   ROTATE
0345 F94A  A5 42              LDA   BDRATL          ; SET UP BAUD RATE TIMER
0346 F94C  85 1B              STA   CNTACL
0347 F94E  A5 43              LDA   BDRATH
0348 F950  85 1A              STA   CNTAL
0349 F952  57 12              RMB   5,IER           ; DISABLE IRQS
0350 F954  A5 42              LDA   BDRATL          ; DETERMINE WHAT BAUD RATE WE'RE RUNNING AT
0351 F956  C9 B5              CMP   #BAUD3-10       ; IS IT GREATER THAN 300 ?
0352 F958  90 08              BCC   GT300           ; YES==> BRANCH
0353 F95A  A2 03        B03   LDX   #03             ; NO ==> BAUD = 300
0354 F95C  57 01              RMB   5,PB            ; SET "HISPEED" TO 0 ( LOW SPEED )
0355 F95E  A9 04              LDA   #$04            ; SET R2424 "MODE" CODE  ( BELL 212A ASYNC )
0356 F960  D0 12              BNE   BD2             ; ( BRANCH ALWAYS )
```

```
0357 F962  C9 25      GT300  CMP   #BAUD12-10      ; IS BAUD GREATER THAN 1200 ?
0358 F964  90 08             BCC   B24             ; YES==> MUST BE 2400
0359 F966  A2 0C      B12    LDX   #12             ; NO ==> MUST BE 1200
0360 F968  D7 01             SMB   5,PB            ; SET "HISPEED" TO 1 (HIGH SPEED )
0361 F96A  A9 03             LDA   #$03            ; SET R2424 "MODE" CODE  ( BELL 212A ASYNC )
0362 F96C  D0 06             BNE   BD2             ; ( BRA )
0363 F96E  A2 18      B24    LDX   #24             ; 2400 BAUD
0364 F970  D7 01             SMB   5,PB
0365 F972  A9 0D             LDA   #$0D            ; SET R2424 "MODE" CODE  ( V.22 BIS ASYNC )
0366 F974  85 9D      BD2    STA   TEMP            ; SAVE "MODE" CODE IN TEMPORARY LOCATION
0367 F976  AD 0A 10          LDA   RCVA            ; CHANGE "MODE" IN R2424 MODEM REGISTERS
0368 F979  29 F0             AND   #$F0            ;  - CLEAR OUT PREVIOUS MODE
0369 F97B  05 9D             ORA   TEMP            ;  - SET NEW MODE
0370 F97D  8D 0A 10          STA   RCVA            ;  - AND PROGRAM RECEIVER
0371 F980  AD 0A 20          LDA   XMTA            ; CHANGE TRANSMITTER BAUD RATE ...
0372 F983  29 F0             AND   #$F0            ;  - CLEAR OUT PREVIOUS MODE
0373 F985  05 9D             ORA   TEMP            ;  - SET NEW MODE
0374 F987  8D 0A 20          STA   XMTA            ;  - AND PROGRAM TRANSMITTER
```

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```
0375 F98A  8C 0C 10          STY   RCVC            ;   AND SET MODEM
0376 F98D  8C 0C 20          STY   XMTC
0377 F990  20 CB FD          JSR   NEWCXR          ; UPDATE R2424 REGISTERS WITH NEW VALUES
0378 F993  86 41             STX   BAUD            ; SAVE BAUD CODE
0379
0380 F995  F7 7B             SMB   7,IRQFLG        ; SET ISR TO PROCESS DELAY TIME FOR WAIT-FOR-CARRIER
0381 F997  D7 16             SMB   5,SCSR          ; SET "DATA REG EMPTY" FLAG FOR 'LAST BIT OUT'
```

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```
0383                ; BAUD RATE DETERMINED.  NOW IN COMMAND MODE.  READ COMMAND
0384                ;  CHARACTERS INTO BUFFER ( INBUFF ).  TERMINATE ON <CR>.
0385
0386 F999  FF 74 4B          BBS   7,REPFLG,REPEAT ; BRANCH IF "A/" RECEIVED
0387 F99C  A2 00      SETPTR LDX   #00             ; "AT" RECEIVED --> SET BUFFER INDEX TO 0
0388 F99E  A5 16      WAITIN LDA   SCSR            ; CHECK RECEIVER STATUS
0389 F9A0  29 0F             AND   #$0F
0390 F9A2  F0 FA             BEQ   WAITIN          ; NO BITS SET ==> NO RECEIVED CHAR, TRY AGAIN
0391
0392 F9A4  A5 17      GETCHR LDA   SRDR            ; GET CHAR FROM RECEIVER BUFFER
0393 F9A6  7F 79 03          BBR   7,ECHOFG,CTLCOD  ; BRANCH IF ECHO DISABLED
0394 F9A9  20 51 FF          JSR   CHROUT          ; ECHO CHAR BACK TO HOST COMPUTER
0395 F9AC  C5 89      CTLCOD CMP   S3              ; IS CHAR A <CR> ?
0396 F9AE  F0 1D             BEQ   GOTCHR          ; YES==> SAVE IT AND PROCEED TO "ALLIN"
0397 F9B0  C9 20             CMP   #$20            ; IS INCHAR A <SP> ?
0398 F9B2  F0 EA             BEQ   WAITIN          ; YES==> IGNORE IT
0399 F9B4  90 E8             BCC   WAITIN          ; CHAR IS LESS THAN $20 ( CONTROL CODE ) --> IGNORE IT
0400 F9B6  C9 7F             CMP   #$7F            ; IS IT A "DELETE" CHAR ?   <-- REMOVE THESE FOUR LINES IF THE
0401 F9B8  D0 05             BNE   BS              ; NO ==> CHECK FOR <BS>       <-- <DELETE> KEY ON THE PARTICULAR
0402 F9BA  A5 8B             LDA   S5              ; YES==> CHANGE IT TO <BS>    <-- TERMINAL USED WITH THIS DESIGN
0403 F9BC  20 51 FF          JSR   CHROUT          ; SEND OUT <BACKSPACE>    <-- BACKSPACES THE CURSOR.
```

```
0404 F9BF  C5 8B     BS     CMP   S5              ; IS IT A <BACK-SPACE> ?
0405 F9C1  D0 0A            BNE   GOTCHR          ; NO ==> ACCEPT CHAR
0406 F9C3  CA        DELETE DEX                   ; YES==> OVERWRITE PREVIOUS CHAR IN BUFFER
0407 F9C4  10 D8            BPL   WAITIN          ; BRANCH IF BUFF POINTER NOT LESS THAN 0
0408 F9C6  A9 20            LDA   #$20            ; OUTPUT A <SP>
0409 F9C8  20 51 FF         JSR   CHROUT
0410 F9CB  30 CF            BMI   SETPTR          ; LIMIT LOWEST VALUE OF POINTER TO 0  ( BRA )
0411
0412 F9CD  95 4C     GOTCHR STA   INBUFF,X        ;  SAVE CHAR IN BUFFER
0413 F9CF  C5 89            CMP   S3              ; IS IT A <CR> ?
0414 F9D1  F0 0A            BEQ   ALLIN           ; YES==> ALL CHARS RECEIVED
0415 F9D3  E8               INX                   ; NO ==> INC POINTER AND GET NEXT CHAR
0416 F9D4  E0 29            CPX   #41             ; IS BUFFER FULL ?
0417 F9D6  D0 C6            BNE   WAITIN          ; NO ==> GET NEXT CHAR
0418 F9D8  F7 75            SMB   7,BUFFL6        ; YES==> SET FLAG TO INDICATE ERROR
0419 F9DA  CA               DEX                   ; KEEP READING UNTIL <CR>
0420 F9DB  D0 C1            BNE   WAITIN          ; ( BRA )
0421
0422 F9DD  7F 75 07  ALLIN  BBR   7,BUFFL6,REPEAT  ; BRANCH IF 40 OR LESS CHARS READ IN
0423 F9E0  A9 04            LDA   #04             ; TOO MANY CHARS ENTERED --> ERROR
0424 F9E2  85 7D            STA   STCODE          ; SET STATUS CODE TO INDICATE ERROR
0425 F9E4  4C E0 FD         JMP   CR              ; AND TERMINATE COMMAND STRING
0426
0427 F9E7  A2 00     REPEAT LDX   #00             ; SET COMMAND STRING POINTER TO ZERO
```



```
0429                ; ALL COMMANDS AND PARAMETERS HAVE BEEN RECEIVED.  NOW EXECUTE
0430                ;  EACH COMMAND, IN ORDER, UNTIL <CR> OR UNRECOGNIZED COMMAND (ERROR)
0431
0432 F9E9  20 F5 F9 NXTCMD JSR   FNDCMD          ; FIND CORRESPONDING SUBROUTINE ADDRESS AND
0433                                              ;  SET UP JUMP VECTOR
0434 F9EC  20 F2 F9         JSR   DOCMD           ; EXECUTE COMMAND.
0435 F9EF  4C E9 F9         JMP   NXTCMD          ; FETCH NEXT COMMAND
0436 F9F2  6C 9B 00  DOCMD  JMP   (CMDVEC)        ; JMP TO COMMAND ROUTINE.


0438                ;           EACH COMMAND ROUTINE ASSUMES THE X-REG POINTS
0439                ;            TO THE CHAR IN "INBUFF" FOLLOWING THE COMMAND
0440                ;            CHAR, AND LEAVES X-REG POINTING TO THE NEXT
0441                ;            COMMAND CHAR.  THE Y-REG IS FREE FOR USE AS
0442                ;            A GENERAL SCRATCH-PAD REGISTER.
0443
0444 F9F5  A0 00     FNDCMD LDY   #00              ; SET UP TABLE INDEX
0445 F9F7  B5 4C            LDA   INBUFF,X        ; FETCH COMMAND BYTE
0446 F9F9  C5 89            CMP   S3              ; IS IT A <CR> ?
0447 F9FB  F0 0E            BEQ   GOCR            ; YES==> TERMINATE COMMAND STRING
0448 F9FD  D9 47 FA  LOOP2  CMP   CMDTBL,Y        ; NO ==> A MATCH FOUND ?
0449 FA00  F0 0B            BEQ   FOUND           ; YES==> GET VECTOR
0450 FA02  C8               INY                   ; NO ==> TRY NEXT TABLE ENTRY
0451 FA03  C0 21            CPY   #NUMCMD         ; END OF TABLE ?
0452 FA05  D0 F6            BNE   LOOP2           ; NO ==> GO AGAIN
0453 FA07  A9 04            LDA   #04             ; YES==> ERROR ...
0454 FA09  85 7D            STA   STCODE
```

```
0455 FA0B   A0 21       GOCR  LDY   #NUMCMD           ; SET POINTER TO <CR> COMMAND
0456
0457 FA0D   98          FOUND TYA                     ; COMMAND FOUND.  GET ASSOCIATED VECTOR
0458 FA0E   0A                ASL   A                 ; MULT INDEX BY 2
0459 FA0F   A8                TAY
0460 FA10   B9 69 FA          LDA   VECTBL,Y          ; GET VECTOR
0461 FA13   85 9B             STA   CMDVEC            ; AND SET UP COMMAND JUMP
0462 FA15   B9 6A FA          LDA   VECTBL+1,Y
0463 FA18   85 9C             STA   CMDVEC+1
0464 FA1A   E8                INX                     ; INC INBUFF INDEX TO POINT TO FIRST
0465 FA1B   60                RTS                     ;  BYTE FOLLOWING COMMAND BYTE
```



```
0467                ;         PHONE IS RINGING.  ANSWER IT ?
0468
0469 FA1C   57 12   RINGNG RMB   5,IER              ; DISABLE IRQ
0470 FA1E   07 10          RMB   0,IFR-1            ; RESET PA0 ( "PHONE IS RINGING" ) FLAG
0471 FA20   A9 A0          LDA   #$A0               ; SET MCR FOR SERIAL I/O
0472 FA22   85 14          STA   MCR
0473 FA24   A5 40          LDA   DEFPRO             ; SET SERIAL PROTOCOL TO MOST RECENT VALUE
0474 FA26   85 15          STA   SCCR
0475 FA28   A5 42          LDA   BDRATL             ; SET SERIAL CLOCK TO MOST RECENT VALUE
0476 FA2A   85 18          STA   CNTACL
0477 FA2C   A5 43          LDA   BDRATH
0478 FA2E   85 1A          STA   CNTAL
0479 FA30   A9 02          LDA   #$02               ; SET "STCODE" TO "RING" RESPONSE
0480 FA32   85 7D          STA   STCODE
0481 FA34   20 E8 FE       JSR   RESPNS             ; AND OUTPUT APPROPRIATE MESSAGE
0482 FA37   E6 87          INC   S1                 ; ADD 1 TO RING COUNTER
0483 FA39   A4 87          LDY   S1                 ; NOW CHECK FOR RING COUNT
0484 FA3B   C4 86          CPY   S0                 ; IS THE RING COUNT UP TO THE SET LIMIT YET ?
0485 FA3D   F0 03          BEQ   ANSWER             ; YES==> GO ANSWER THE PHONE !
0486 FA3F   4C 16 F8       JMP   RESTRT             ; NO==> START OVER READING IN CHARS FROM HOST SYSTEM
0487
0488 FA42   F7 78   ANSWER SMB   7,IRQFLG           ; CHANGE ISR TO PROCESS DELAY TIME FOR WAIT-FOR-CARRIER
0489 FA44   20 0D FC       JSR   AAA                ; NOW GO ANSWER PHONE  ( "JSR" WILL PUT 2 RETURN
0490                                                ;   ADDRESS BYTES ON THE STACK.  THESE WILL BE
0491                                                ;   DISCARDED AT THE END OF THE <CR> COMMAND
0492                                                ;   -- AT LABLE "NOWAIT" -- FOLLOWED BY
0493                                                ;   A "JMP RESTRT" )
```



```
0496                ;                    ----- THE ORDER OF THESE TWO TABLES MUST MATCH ----
0497 FA47   2C      CMDTBL .BYT   ','
0498 FA48   30             .BYT   '0123456789*#'
0499 FA54   3B             .BYT   $3B,'=?'
0500 FA57   41             .BYT   'ACDEFH'
0501 FA5D   49             .BYT   'IMOPQR'
0502 FA63   53             .BYT   'STVXZ'
0503 FA68   00             .BYT   $00               ; MARKER FOR <CR> COMMAND
```

```
0504
0505 FA69  1E FB      VECTBL .WOR   COMMA
0506 FA6B  3C FB             .WOR   DIGIT,DIGIT,DIGIT,DIGIT,DIGIT,DIGIT
0507 FA77  3C FB             .WOR   DIGIT,DIGIT,DIGIT,DIGIT,DIGIT,DIGIT
0508 FA83  5B FB             .WOR   SEMIC,EQUAL,QUESTN
0509 FA89  0D FC             .WOR   AAA,CCC,DDD,EEE,FFF,HHH
0510 FA95  BB FC             .WOR   III,MMM,OOO,PPP,QQQ,RRR
0511 FAA1  3A FD             .WOR   SSS,TTT,VVV,XXX,ZZZ
0512 FAAB  E0 FD             .WOR   CR                  ; ---------> MUST BE LAST ENTRY IN TABLE
0513
0514
0515                  ;  INITIAL VALUES FOR S-REGISTERS, IN ORDER FROM 0 TO 16
0516
0517 FAAD  00         STBL    .BYT   0,0,43,13,10
0518 FAB2  08                 .BYT   8,2,30,02
0519 FAB6  06                 .BYT   6,7,70,50
0520 FABA  FF                 .BYT   $FF,$FF,$FF
0521 FABD  00                 .BYT   0
```



```
0523                  ;   THIS ROUTINE INITIALIZES PROGRAM VARIABLES AND
0524                  ;    CPU REGISTERS.
0525
0526 FABE  A9 00      INITSW LDA    #$00                 ; DISABLE ALL IRQS
0527 FAC0  85 11             STA    IFR
0528 FAC2  85 12             STA    IER
0529 FAC4  8D 0D 20          STA    XMTD                 ; SET UP R2424 TO DEFAULT VALUES
0530 FAC7  8D 0B 20          STA    XMTB
0531 FACA  A9 04             LDA    #$04
0532 FACC  8D 0D 10          STA    RCVD
0533 FACF  A9 03             LDA    #$03
0534 FAD1  8D 0A 10          STA    RCVA
0535 FAD4  8D 0A 20          STA    XMTA
0536 FAD7  A9 08             LDA    #$08
0537 FAD9  8D 0C 10          STA    RCVC
0538 FADC  8D 0C 20          STA    XMTC
0539 FADF  8D 0E 10          STA    RCVE
0540 FAE2  8D 0E 20          STA    XMTE
0541
0542 FAE5  A9 00             LDA    #00
0543 FAE7  85 83             STA    SSETFG               ; SET FLAG TO INDICATE S-REG HAS NOT BEEN SET
0544 FAE9  85 87             STA    S1                   ; SET RING COUNT TO 0
0545 FAEB  85 7F             STA    XCODE                ; STANDARD "CARRIER" RESPONSE
0546 FAED  85 76             STA    DILFLG               ; DISABLE DIALING
0547 FAEF  85 7B             STA    RSLTFG               ; ENABLE RESULT RESPONSE
0548 FAF1  A9 80             LDA    #$80                 ; ENABLE ECHO
0549 FAF3  85 79             STA    ECHOFG
0550 FAF5  85 7A             STA    DUPLEX               ; FULL DUPLEX
0551 FAF7  85 7E             STA    VCODE                ; SET UP FOR VERBAL RESPONSE
0552 FAF9  85 7C             STA    SPKRFG               ; SET SPEAKER FOR "M1" COMMAND OPERATION
0553 FAFB  A9 2F             LDA    #<BAUD12             ; SET DEFAULT BAUD RATE TO 1200 BAUD
0554 FAFD  85 42             STA    BDRATL
0555 FAFF  A9 00             LDA    #>BAUD12
0556 FB01  85 43             STA    BDRATH
```

```
0557 FB03   A9 C0          LDA   #$C0          ; SET DEFAULT SERIAL PROTOCOL TO 8 BITS, NO PARITY
0558 FB05   85 40          STA   DEFPRO
0559 FB07   A9 86          LDA   #<S0          ; BASE POINTER FOR S-REGISTERS
0560 FB09   85 84          STA   SREGP
0561 FB0B   A9 00          LDA   #>S0          ; SET UP HIGH-BYTE OF S-REG POINTER
0562 FB0D   85 85          STA   SREGP+1
0563 FB0F   A0 11          LDY   #17           ; INITIALIZE S-REGS
0564 FB11   B9 AD FA  SLOOP LDA   STBL,Y
0565 FB14   91 84          STA   (SREGP),Y
0566 FB16   88             DEY
0567 FB17   10 F8          BPL   SLOOP
0568 FB19   A5 89          LDA   S3
0569 FB1B   85 4C          STA   INBUFF        ; INITIALIZE COMMAND STRING TO [NULL]
0570 FB1D   60             RTS
0571                       .FILE MDM10B
```



```
0573                ; THE FOLLOWING ARE ALL THE COMMAND ROUTINES TO EXECUTE THE
0574                ;  "AT" COMMANDS....
0575
0576
0577                ; "," COMMAND   --- WAIT FOR ONE PAUSE TIME
0578
0579 FB1E   86 9D   COMMA  STX   TEMP          ; SAVE INBUFF POINTER
0580 FB20   A6 8E          LDX   S8            ; GET VALUE OF S-REG 8 ( DELAY TIME )
0581 FB22   F0 15          BEQ   NODLAY        ; IF ZERO THEN NO DELAY
0582 FB24   A9 9C          LDA   #<DLYTIM
0583 FB26   85 1C          STA   CNTBCL        ; START TIMER-B
0584 FB28   A9 E0          LDA   #>DLYTIM
0585 FB2A   85 1E          STA   CNTBHL
0586 FB2C   A0 10   ONESEC LDY   #DLYHIB
0587 FB2E   5F 11 FD WAITB BBR   5,IFR,WAITB   ; IS TIMER B DONE YET ?
0588 FB31   A5 1C          LDA   CNTBCL        ; YES ==> CLEAR TIMER FLAG
0589 FB33   88             DEY                 ; DONE COUNTING YET ?
0590 FB34   D0 F8          BNE   WAITB         ; NO ==> KEEP GOING
0591 FB36   CA             DEX                 ; ANY MORE 1-SEC DELAYS ?
0592 FB37   D0 F3          BNE   ONESEC        ; YES==> ONE MORE TIME ....
0593 FB39   A6 9D   NODLAY LDX   TEMP          ; RESTORE INBUFF POINTER
0594 FB3B   60             RTS
0595
0596                ;*********************************************************************
0597
0598
0599                ; DIAL A NUMBER
0600
0601 FB3C   7F 76 15 DIGIT BBR   7,DILFLG,DIGERR ; IF NUMBER IS NOT TO BE DIALED --> ERROR
0602 FB3F   A9 01          LDA   #$01          ; WAIT UNTIL DIAL BUFFER EMPTY
0603 FB41   2C 0E 20 WAITRE BIT   XMTE
0604 FB44   F0 FB          BEQ   WAITRE
0605 FB46   B5 4B          LDA   INBUFF-1,X    ; GET ASCII NUMBER FROM BUFFER.  IN THIS CASE, THE
0606                                           ;  COMMAND BYTE IS THE PARAMETER.  SINCE THE X-REG
0607                                           ;  HAS ALREADY BEEN UPDATED TO POINT TO THE BYTE
0608                                           ;  FOLLOWING THIS DIGIT/COMMAND, THE BASE OF THE
0609                                           ;  COMMAND BUFFER HAS TO BE SHIFTED DOWN ONE BYTE
```

```
0610                                                    ;  TO COMPENSATE.
0611 FB4B  C9 23          CMP   #'#'                    ; IS THE DIAL DIGIT A "#" ?
0612 FB4A  D0 02          BNE   DIG2                    ; NO ==> BRANCH
0613 FB4C  A9 0E          LDA   #$0E                    ; YES==> EXCHANGE CHAR FOR R2424'S "#" NUMBER
0614 FB4E  29 0F    DIG2  AND   #$0F                    ; MAKE IT ABSOLUTE
0615 FB50  8D 00 20       STA   XMTO                    ;  AND DIAL ...
0616 FB53  60       QDIGIT RTS
0617
0618 FB54  A9 04    DIGERR LDA  #04                     ;   "ERROR "
0619 FB56  85 7D          STA   STCODE
0620 FB58  4C E0 FD       JMP   CR                      ; TERMINATE COMMAND STRING PROCESSING
0621
0622               ;*************************************************************************
0623
0624
0625               ; SEMICOLON COMMAND   ---   DONE DIALING - RETURN TO COMMAND MODE
0626
0627 FB5B  7F 76 11 SEMIC  BBR   7,DILFLG,SEMERR      ; BRANCH IF ";" ENTERED WHILE NOT DIALING (ERROR)
0628 FB5E  06 76          ASL   DILFLG                ; TURN OFF DIAL FLAG ( $80 --> $00 )
0629 FB60  A9 01          LDA   #01                   ; WAIT UNTIL DIAL REGISTER IS EMPTY
0630 FB62  2C 0E 20 SEMI2 BIT   XMTE                  ; EMPTY YET ?
0631 FB65  F0 FB          BEQ   SEMI2                 ; NO ==> KEEP WAITING
0632 FB67  A9 FF          LDA   #$FF                  ; YES==> FINISH DIALING
0633 FB69  8D 00 20       STA   XMTO
```



```
0634 FB6C  77 80          RMB   7,WAITFG              ; PREVENT <CR> COMMAND FROM GOING ON-LINE (REMAIN IN
0635 FB6E  60             RTS                         ;   COMMAND MODE)
0636
0637 FB6F  A9 04    SEMERR LDA  #$04                  ; SET STCODE FOR ERROR
0638 FB71  85 7D          STA   STCODE
0639 FB73  4C E0 FD       JMP   CR                    ;  ... AND TERMINATE COMMAND STRING EXECUTION
0640
0641               ;*************************************************************************
0642
0643               ;  "=" COMMAND   ---   SET S-REGISTER TO A VALUE
0644
0645 FB76  7F 83 DB EQUAL  BBR   7,SSETFG,DIGERR      ; IF FLAG IS CLEAR --> "ERROR"
0646 FB79  A9 00          LDA   #00                   ; CLEAR OUT TEMP BUFFER
0647 FB7B  85 9B          STA   NUM
0648 FB7D  85 99          STA   NUM+1
0649 FB7F  85 9A          STA   NUM+2
0650 FB81  20 8E FD       JSR   GETNUM                ; GET FIRST CHAR FROM BUFFER
0651 FB84  B0 36          BCS   EQ4                   ; IF IT IS NOT A NUMBER, THEN ASSUME ZERO
0652 FB86  85 98          STA   NUM                   ; SAVE NUMBER IN TEMP BUFF
0653 FB88  20 8E FD       JSR   GETNUM                ; IS THERE ANOTHER NUMBER ?
0654 FB8B  B0 15          BCS   EQ2                   ; NO ==> ONES DIGIT ONLY --> BRANCH
0655 FB8D  A4 9B          LDY   NUM                   ; YES==> MOVE ONES DIGIT OVER
0656 FB8F  84 99          STY   NUM+1                 ;        AND INSERT TENS DIGIT
0657 FB91  85 9B          STA   NUM
0658 FB93  20 8E FD       JSR   GETNUM                ; IS THERE A THIRD NUMBER ( HUNDREDS DIGIT ) ?
0659 FB96  B0 0A          BCS   EQ2                   ; NO ==> ALL NUMBERS FETCHED --> BRANCH
0660 FB98  A4 99          LDY   NUM+1                 ; YES==> MOVE ONES AND TENS DIGITS
```

```
0661 FB9A  84 9A        STY   NUM+2          ;        OVER AND INSERT HUNDREDS
0662 FB9C  A4 98        LDY   NUM            ;        DIGIT IN FRONT
0663 FB9E  84 99        STY   NUM+1
0664 FBA0  85 98        STA   NUM
0665 FBA2  A5 99  EQ2   LDA   NUM+1          ; GET TENS DIGIT
0666 FBA4  F0 07        BEQ   EQ3            ; IGNORE IT IF IT'S ZERO
0667 FBA6  20 EC FB     JSR   MULT10         ; IF > 0 , MULTIPLY BY 10
0668 FBA9  65 98        ADC   NUM            ; ADD IN ONES DIGIT
0669 FBAB  85 98        STA   NUM            ; AND SAVE TENS+ONES
0670 FBAD  A5 9A  EQ3   LDA   NUM+2          ; GET HUNDREDS DIGIT; IS IT = 0 ?
0671 FBAF  F0 0B        BEQ   EQ4            ; YES==> FINISHED CONVERTING TO HEX
0672 FBB1  20 EC FB     JSR   MULT10         ; NO ==> MULTIPLY HUNDREDS DIGIT BY 10
0673 FBB4  20 EC FB     JSR   MULT10         ;  AND BY 10  AGAIN  ( * 100  )
0674 FBB7  18           CLC
0675 FBB8  65 98        ADC   NUM            ;  ADD IN TENS+ONES DIGIT
0676 FBBA  85 98        STA   NUM
0677 FBBC  A5 98  EQ4   LDA   NUM
0678 FBBE  A0 00        LDY   #00
0679 FBC0  91 84        STA   (SREGP),Y      ; SAVE TOTAL HEX VALUE
0680 FBC2  A5 96        LDA   S16            ; GO TO SELF-TEST ?
0681 FBC4  D0 12        BNE   SLFTST         ; NO => STOP SELF TEST
0682 FBC6  A9 EF  NOSLFT LDA  #$EF           ; NO SELF TEST -- RETURN TO NORMAL OPERATING MODE
0683 FBC8  2D 0A 10     AND   RCVA           ;  DISABLE SELF-TEST BITS IN R2424
0684 FBCB  8D 0A 10     STA   RCVA
0685 FBCE  A9 EF        LDA   #$EF
0686 FBD0  2D 0A 20     AND   XMTA
0687 FBD3  8D 0A 20     STA   XMTA
0688 FBD6  D0 10        BNE   QEQ            ; ( BRANCH ALWAYS )
0689
0690 FBD8  A9 10  SLFTST LDA  #$10           ; START SELF-TEST
0691 FBDA  0D 0A 10     ORA   RCVA           ;  SET SELF-TEST BITS IN R2424
0692 FBDD  8D 0A 10     STA   RCVA
0693 FBE0  A9 10        LDA   #$10
0694 FBE2  0D 0A 20     ORA   XMTA
```



```
0695 FBE5  8D 0A 20     STA   XMTA
0696 FBE8  20 CB FD  QEQ  JSR  NEWCXR        ; UPDATE R2424 SCRATCH-PAD REGISTERS
0697 FBEB  60           RTS
0698
0699 FBEC  85 9D  MULT10 STA  TEMP           ; SAVE VALUE IN TEMP STORAGE
0700 FBEE  0A           ASL   A              ; MULTIPLY BY 2   ( * 2 )
0701 FBEF  0A           ASL   A              ;  AND BY 2 AGAIN ( * 4 )
0702 FBF0  65 9D        ADC   TEMP           ; THEN ADD IN ORIGINAL VALUE  ( CARRY FLAG ALWAYS CLEAR )
0703 FBF2  0A           ASL   A              ; MULTIPLY BY 2 AGAIN ( * 10 )
0704 FBF3  60           RTS
0705
0706               ;*********************************************************************************
0707
0708               ; "?" COMMAND  ---  SEND BACK CONTENTS OF S-REGISTER
0709
0710 FBF4  20 40 FF  QUESTN JSR  CRLF        ; PREFACE OUTPUT WITH <CR/LF>
0711 FBF7  A0 00        LDY   #00
```

```
0712 FBF9  B1 84          LDA   (SREGP),Y        ; GET VALUE OF S-REG
0713 FBFB  20 9F FD       JSR   HX2ASC           ; AND CONVERT IT TO ASCII
0714 FBFE  A0 02          LDY   #02              ; SEND OUT 3 CHARS
0715 FC00  B9 98 00  QUES3 LDA  NUM,Y           ; GET CHAR FROM "NUM" BUFFER
0716 FC03  20 51 FF       JSR   CHROUT
0717 FC06  88             DEY                    ; LAST CHAR ?
0718 FC07  10 F7          BPL   QUES3            ; NO ==> SEND OUT NEXT ONE
0719 FC09  20 40 FF       JSR   CRLF             ; YES==> SEND OUT <CR/LF>
0720 FC0C  60             RTS
0721
0722               ;*************************************************************************
0723
0724               ; "A" COMMAND  ---  SET MODEM TO ANSWER AN INCOMING CALL
0725
0726 FC0D  20 95 FC  AAA  JSR   H1AND2           ; PICK UP PHONE ( GO OFF-HOOK )
0727 FC10  A9 10          LDA   #$10             ; SET R2424 TO ANSWER MODE
0728 FC12  0D 0D 20       ORA   XMTD
0729 FC15  8D 0D 20       STA   XMTD
0730 FC18  A9 DF          LDA   #$DF             ; SET "ORG" BIT TO 0
0731 FC1A  2D 09 20       AND   XMT9
0732 FC1D  8D 09 20       STA   XMT9
0733 FC20  20 CE FD       JSR   NEWCX            ; UPDATE R2424 STATUS
0734 FC23  F7 80          SMB   7,WAITFG         ; SET FLAG TO INDICATE WE ARE TO WAIT FOR CARRIER
0735 FC25  4C EE FD       JMP   CR2              ;  AND GO DIRECTLY TO CARRIER-DETECT
0736                                             ;  -- DO NOT ACCEPT ANY MORE COMMANDS
0737
0738               ;*************************************************************************
0739
0740               ; "C" COMMAND  --- TOGGLE TRANSMITTER
0741
0742
0743 FC28  20 8E FD  CCC   JSR   GETNUM           ; GET PARAMETER, IF ANY
0744 FC2B  B0 0B          BCS   CCZERO           ; BRANCH IF NO PARAMETER ( ASSUME ZERO )
0745 FC2D  F0 09          BEQ   CCZERO           ; BRANCH IF PARAMETER = 0
0746 FC2F  A9 04     CCONE LDA  #04              ; PARAMETER =1 --> TURN ON "CC" BIT
0747 FC31  0D 09 20       ORA   XMT9             ;  IN MODEM REGISTER
0748 FC34  D0 07          BNE   QCCC
0749 FC36  D0 05          BNE   QCCC             ; ( BRANCH ALWAYS )
0750 FC38  A9 FB     CCZERO LDA  #$FB            ; PARAMETER =0 --> TURN OFF "CC" BIT
0751 FC3A  2D 09 20       AND   XMT9
0752 FC3D  8D 09 20  QCCC STA   XMT9
0753 FC40  20 CE FD       JSR   NEWCX            ; UPDATE MODEM REGISTERS
0754 FC43  60             RTS
0755
```



```
0756               ;*************************************************************************
0757
0758               ; "D" COMMAND  ---  DIAL A NUMBER
0759
0760 FC44  A9 20     DDD  LDA   #$20             ; PUT MODEM IN ORIGINATE MODE
0761 FC46  0D 09 20       ORA   XMT9             ; AND SET TO DIAL
0762 FC49  8D 09 20       STA   XMT9
```

```
0763 FC4C  AD 0D 20          LDA   XMTD
0764 FC4F  29 EF             AND   #$EF
0765 FC51  09 48             ORA   #$48
0766 FC53  8D 0D 20          STA   XMTD              ; SET CRQ=1 AND DTR=1
0767 FC56  20 CE FD          JSR   NEWCX             ; UPDATE TRANSMITTER REGISTERS
0768 FC59  2C 08 20    WAITDL BIT  XMTB
0769 FC5C  10 FB             BPL   WAITDL            ; WAIT UNTIL DLO=1
0770 FC5E  A5 8E             LDA   S8                ; DELAY "S6" NUMBER OF SECONDS.  USE "COMMA"
0771 FC60  48                PHA                     ;  COMMAND FOR DELAY ROUTINE.  TO DO THIS, WE HAVE TO
0772 FC61  A5 8C             LDA   S6                ;  SAVE THE ORIGINAL VALUE OF "S8" ( IN THIS CASE ON
0773 FC63  85 8E             STA   S8                ;  THE STACK ) AND THEN SUBSTITUTE THE VALUE FOR "S6"
0774 FC65  20 1E FB          JSR   COMMA             ;  INTO "S8".  THIS WILL DELAY "S6" SECONDS.  AFTER
0775 FC68  68                PLA                     ;  THE DELAY IS FINISHED, WE POP THE ORIGINAL "S8"
0776 FC69  85 8E             STA   S8                ;  VALUE OFF THE STACK AND RETURN IT TO "S8".
0777 FC6B  F7 76             SMB   7,DILFLG          ; SET "DIAL FLAG" TO DIAL SUBSEQUENT NUMBERS
0778 FC6D  F7 80             SMB   7,WAITFG          ; ENABLE WAIT-FOR-CARRIER DELAY
0779 FC6F  77 77             RMB   7,REVFLG          ; SET FOR NORMAL DIALING
0780 FC71  60                RTS
0781
0782                   ;*************************************************************************
0783
0784                   ; "E" COMMAND  ---  TOGGLE ECHOING CHARS BACK TO HOST SYSTEM
0785
0786 FC72  20 8E FD    EEE   JSR   GETNUM              ; GET PARAMETER, IF ANY
0787 FC75  B0 06             BCS   EZERO             ; BRANCH IF NO PARAMETER ( ASSUME ZERO )
0788 FC77  F0 04             BEQ   EZERO             ; BRANCH IF PARAMETER = 0
0789 FC79  F7 79       EONE  SMB   7,ECHOFG          ; SET ECHO FLAG
0790 FC7B  D0 02             BNE   QECHO             ; ( BRA )
0791 FC7D  77 79       EZERO RMB   7,ECHOFG          ; CLEAR ECHO FLAG ( NO ECHO )
0792 FC7F  60          QECHO RTS
0793
0794                   ;*************************************************************************
0795
0796                   ; "F" COMMAND  ---  SET HALF/FULL DUPLEX
0797
0798 FC80  20 8E FD    FFF   JSR   GETNUM              ; GET PARAMETER, IF ANY
0799 FC83  B0 06             BCS   FZERO             ; IF NONE, ASSUME ZERO
0800 FC85  F0 04             BEQ   FZERO             ; BRANCH IF = 0
0801 FC87  F7 7A       FONE  SMB   7,DUPLEX          ; SET FOR FULL DUPLEX
0802 FC89  D0 02             BNE   QFFF              ; ( BRANCH ALWAYS )
0803 FC8B  77 7A       FZERO RMB   7,DUPLEX          ; SET FOR HALF DUPLEX
0804 FC8D  60          QFFF  RTS
0805
0806                   ;*************************************************************************
0807
0808                   ; "H" COMMAND  ---  ON/OFF HOOK
0809
0810 FC8E  20 8E FD    HHH   JSR   GETNUM              ; GET PARAMETER, IF ANY
0811 FC91  B0 14             BCS   HHZERO            ; IF NO PARAMETER, ASSUME ZERO
0812 FC93  F0 12             BEQ   HHZERO            ; BRANCH IF PARAMETER = 0
0813 FC95  AD 0D 20    H1AND2 LDA   XMTD              ; PARAMETER MUST BE 1 OR 2 (ON THE R2424, THEY
0814                                                  ;  FUNCTION THE SAME)
0815 FC98  09 40             ORA   #$40
0816 FC9A  8D 0D 20          STA   XMTD              ; SET XMIT CRQ = 1
```

```
0817 FC9D  AD 0D 10          LDA   RCVD
0818 FCA0  09 40             ORA   #$40
0819 FCA2  8D 0D 10          STA   RCVD              ; SET RCV CRQ = 1
0820 FCA5  D0 10             BNE   HHSET             ; ( BRANCH ALWAYS )
0821 FCA7  AD 0D 20    HHZERO LDA   XMTD             ; GO OFF-LINE  ( HANG UP )
0822 FCAA  29 AF             AND   #$AF
0823 FCAC  8D 0D 20          STA   XMTD              ; SET XMIT CRQ = 0
0824 FCAF  AD 0D 10          LDA   RCVD
0825 FCB2  29 BF             AND   #$BF
0826 FCB4  8D 0D 10          STA   RCVD              ; SET RCV CRQ = 0
0827 FCB7  20 CB FD    HHSET JSR   NEWCXR            ; UPDATE MODEM'S INTERNAL REGISTERS
0828 FCBA  60          QHHH  RTS
0829
0830
0831                   ;*************************************************************************
0832
0833                   ; "I" COMMAND  ---  RESPOND WITH CHECKSUM OR PRODUCT CODE
0834
0835 FCBB  20 40 FF    III   JSR   CRLF              ; MOVE DOWN TO NEXT LINE
0836 FCBE  20 8E FD          JSR   GETNUM            ; GET PARAMETER, IF ANY
0837 FCC1  B0 06             BCS   IIZERO            ; BRANCH IF NO PARAMETER ( ASSUME ZERO )
0838 FCC3  F0 04             BEQ   IIZERO            ; BRANCH IF PARAMTER = 0
0839 FCC5  A0 2D       IIONE LDY   #CHKSUM-MSG       ; SEND OUT CHECKSUM
0840 FCC7  D0 02             BNE   QII
0841 FCC9  A0 31       IIZERO LDY   #PCODE-MSG       ; SEND OUT PRODUCT CODE
0842 FCCB  20 33 FF    QII   JSR   MSGOUT
0843 FCCE  60                RTS
0844
0845
0846                   ;*************************************************************************
0847
0848                   ; "M" COMMAND  ---  ENABLE/DISABLE SPEAKER
0849
0850 FCCF  77 7C       MMM   RMB   7,SPKRFG          ; DISABLE SPEAKER FLAG
0851 FCD1  20 8E FD          JSR   GETNUM            ; GET PARAMETER, IF ANY
0852 FCD4  B0 0D             BCS   MMZERO            ; IF NONE, ASSUME ZERO
0853 FCD6  F0 0B             BEQ   MMZERO            ;  BRANCH IF = 0
0854 FCD8  C9 01             CMP   #01               ; IS IT ONE ?
0855 FCDA  D0 02             BNE   MMTWO             ; NO ==> LEAVE SPEAKER FLAG DISABLED
0856 FCDC  F7 7C       MMONE SMB   7,SPKRFG          ; YES==> ENABLE FLAG TO TURN SPEAKER OFF AT CARRIER TONE
0857 FCDE  67 01       MMTWO RMB   6,PB              ;  TURN ON SPEAKER
0858 FCE0  4C E5 FC          JMP   QMMM
0859 FCE3  E7 01       MMZERO SMB   6,PB             ; DISABLE SPEAKER
0860 FCE5  60          QMMM  RTS
0861
0862
0863                   ;*************************************************************************
0864
0865
0866                   ; "O" COMMAND  ---  GO ON-LINE
0867
0868 FCE6  20 95 FC    OOO   JSR   H1AND2            ; PICK UP PHONE  ( GO OFF-HOOK )
0869 FCE9  F7 80             SMB   7,WAITFG          ; ENABLE CARRIER TEST
0870 FCEB  4C F6 FD          JMP   CARTIM            ;  AND GO DIRECTLY TO CARRIER-DETECT ...
```

```
0871
0872                    ;*****************************************************************************
0873
0874                    ;  "P" COMMAND   ---   PULSE DIAL
0875
0876 FCEE   AD 0B 20    PPP     LDA     XMTB            ; SET PULSE/TONE BIT TO 0
0877 FCF1   29 FD               AND     #$FD
```



```
0878 FCF3   8D 0B 20            STA     XMTB
0879 FCF6   20 CE FD            JSR     NEWCX           ; UPDATE TRANSMITTER REGISTERS
0880 FCF9   60                  RTS
0881
0882                    ;*****************************************************************************
0883
0884                    ;  "Q" COMMAND   ---   TOGGLE SENDING RESULT CODE/MESSAGE
0885
0886 FCFA   20 BE FD    QQQ     JSR     GETNUM          ; GET PARAMETER, IF ANY
0887 FCFD   B0 06               BCS     QQZERO          ; BRANCH IF NO PARAMETER ( ASSUME ZERO )
0888 FCFF   F0 04               BEQ     QQZERO          ; BRANCH IF PARAMETER = 0
0889 FD01   F7 7B       QQONE   SMB     7,RSLTFG        ; SET FLAG  ( ENABLE PROMPTS )
0890 FD03   D0 02               BNE     QQ              ; ( BRA )
0891 FD05   77 7B       QQZERO  RMB     7,RSLTFG        ; CLEAR FLAG  ( DISABLE PROMPTS )
0892 FD07   60          QQ      RTS
0893
0894                    ;*****************************************************************************
0895
0896                    ; "R" COMMAND   ---   SET DIAL FOR REVERSE MODE
0897                    ;               ( TO DIAL AN ORIGINATE-ONLY MODEM )
0898
0899 FD08   7F 76 28    RRR     BBR     7,DILFLG,RERROR ; BRANCH IF "R" ENTERED WHILE NOT DIALING (ERROR)
0900 FD0B   A5 41               LDA     BAUD            ; ARE WE RUNNING AT 2400 BAUD ?
0901 FD0D   C9 18               CMP     #24
0902 FD0F   F0 21               BEQ     QRRR            ; YES==> "REVERSE" MODE NOT EASILY DONE AT 2400 SINCE
0903                                                    ;         "ANSWER" TONE GOES AWAY AFTER 3 SECONDS.
0904 FD11   77 76               RMB     7,DILFLG        ; NO ==> 300/1200 --> DISABLE FURTHER DIALING
0905 FD13   F7 77               SMB     7,REVFLG        ; SET FLAG TO INDICATE REVERSE DIALING
0906 FD15   A9 20               LDA     #$20            ; SET "ORG" BIT TO 1
0907 FD17   0D 09 20            ORA     XMT9
0908 FD1A   8D 09 20            STA     XMT9
0909 FD1D   A9 BF               LDA     #$BF            ; SET RECEIVER'S "CRQ" BIT TO 0
0910 FD1F   2D 0D 10            AND     RCVD
0911 FD22   8D 0D 10            STA     RCVD
0912 FD25   A9 BF               LDA     #$BF            ; SET TRANSMITTER'S "CRQ" BIT TO 0
0913 FD27   2D 0D 20            AND     XMTD
0914 FD2A   09 20               ORA     #$20            ;   AND "DATA" BIT TO 1
0915 FD2C   8D 0D 20            STA     XMTD
0916 FD2F   20 CB FD            JSR     NEWCXR          ; UPDATE REGISTERS
0917 FD32   60          QRRR    RTS                     ;  AND RETURN .....
0918
0919 FD33   A9 04       RERROR  LDA     #$04            ; SET STCODE FOR ERROR
0920 FD35   85 7D               STA     STCODE
0921 FD37   4C E0 FD            JMP     CR              ;    AND TERMINATE COMMAND STRING EXECUTION
```

```
0922
0923                    ;*************************************************************************
0924
0925                    ; "S" COMMAND   ---   IDENTIFY S-REGISTER FOR FUTURE ACCESS
0926
0927 FD3A   A9 86       SSS     LDA     #<S0            ; START WITH BASE ADDRESS
0928 FD3C   85 84               STA     SREGP
0929 FD3E   20 8E FD            JSR     GETNUM          ; GET NUMBER OF S-REGISTER
0930 FD41   B0 14               BCS     QSSS            ; BRANCH IF NO PARAMETER FOUND
0931 FD43   F0 12               BEQ     QSSS            ; BRANCH IF PARAMETER = 0 ( ALREADY SET UP )
0932 FD45   85 98               STA     NUM             ;  SAVE VALUE
0933 FD47   20 8E FD            JSR     GETNUM          ; GET ONES DIGIT, IF ANY
0934 FD4A   B0 04               BCS     SS2             ; BRANCH IF ONLY ONE DIGIT
0935 FD4C   69 0A               ADC     #10             ; TENS DIGIT COULD ONLY BE A "1"
0936 FD4E   85 98               STA     NUM
0937 FD50   A5 98       SS2     LDA     NUM
0938 FD52   18                  CLC
```



```
0939 FD53   65 84               ADC     SREGP           ; ADD IN BASE ADDRESS
0940 FD55   85 84               STA     SREGP           ;  AND STORE IN POINTER
0941 FD57   F7 83       QSSS    SMB     7,SSETF6        ; SET FLAG TO INDICATE AN S-REG HAS BEEN SET
0942 FD59   60                  RTS
0943
0944                    ;*************************************************************************
0945
0946                    ; "T" COMMAND   ---   TOUCH-TONE DIAL
0947
0948 FD5A   AD 0B 20    TTT     LDA     XMTB            ; SET PULSE/TONE BIT TO 1
0949 FD5D   09 02               ORA     #$02
0950 FD5F   8D 0B 20            STA     XMTB
0951 FD62   20 CE FD            JSR     NEWCX           ; UPDATE TRANSMITTER REGISTERS
0952 FD65   60                  RTS
0953
0954                    ;*************************************************************************
0955
0956                    ; "V" COMMAND   ---   SET VERBAL/NUMERIC RESPONSE
0957
0958 FD66   20 8E FD    VVV     JSR     GETNUM          ; GET PARAMETER, IF ANY
0959 FD69   B0 06               BCS     VZERO           ; IF NONE, ASSUME ZERO
0960 FD6B   F0 04               BEQ     VZERO           ; BRANCH IF = 0
0961 FD6D   F7 7E       VONE    SMB     7,VCODE         ; SET FOR VERBAL RESPONSE
0962 FD6F   D0 02               BNE     QVVV            ; ( BRANCH ALWAYS )
0963 FD71   77 7E       VZERO   RMB     7,VCODE         ; SET FOR NUMERIC RESPONSE
0964 FD73   60          QVVV    RTS
0965
0966                    ;*************************************************************************
0967
0968                    ; "X" COMMAND   ---   ENABLE/DISABLE EXTENDED RESPONSE CODES
0969
0970 FD74   20 8E FD    XXX     JSR     GETNUM          ; GET PARAMETER, IF ANY
0971 FD77   B0 06               BCS     XZERO           ; ASSUME ZERO, IF NONE
0972 FD79   F0 04               BEQ     XZERO           ; BRANCH IF = 0
```

```
0973 FD7B  F7 7F     XONE   SMB   7,XCODE          ; SET FOR EXTENDED CODES
0974 FD7D  D0 02            BNE   QXXX
0975 FD7F  77 7F     XZERO  RMB   7,XCODE          ; SET FOR NORMAL CODES
0976 FD81  60        QXXX   RTS
0977
0978               ;*************************************************************************
0979
0980               ;  "Z" COMMAND   ---   SOFTWARE RESET
0981
0982 FD82  20 E8 FE  ZZZ    JSR   RESPNS          ; SEND OUT RESPONSE, IF ENABLED
0983 FD85  20 40 FF         JSR   CRLF
0984 FD88  7F 16 FD  ZZWAIT BBR   7,SCSR,ZZWAIT   ; WAIT UNTIL ALL CHARS HAVE BEEN SENT OUT
0985 FD8B  4C 00 F8         JMP   RESET           ; THEN RESTART
```



```
0987               ; CHECK THE NEXT CHAR IN "INBUFF".  IF IT IS AN ASCII NUMBER (0-9),
0988               ;    FETCH IT, MASK OFF MSN, INCREMENT COMMAND STRING POINTER  ( REG-X ),
0989               ;    CLEAR CARRY AND RETURN.
0990               ;  IF CHAR IS NOT A NUMBER, SET CARRY AND RETURN.
0991
0992 FD8E  B5 4C     GETNUM LDA   INBUFF,X         ; GET CHAR FROM BUFFER
0993 FD90  C9 30            CMP   #'0'             ; IS IT LESS THAN '0' ?
0994 FD92  90 09            BCC   NOTNUM          ; YES==> QUIT
0995 FD94  C9 3A            CMP   #'9'+1          ; NO ==> IS IT GREATER THAN '9' ?
0996 FD96  B0 06            BCS   QGETN           ; YES==> QUIT
0997 FD98  E8               INX                   ; NO ==> INCREMENT INBUFF POINTER
0998 FD99  29 0F            AND   #$0F            ; MASK OFF TOP-MOST 4 BITS
0999 FD9B  90 01            BCC   QGETN           ; AND RETURN
1000 FD9D  38        NOTNUM SEC                   ; INDICATE CHAR IS NOT AN ASCII NUMBER
1001 FD9E  60        QGETN  RTS                   ; AND RETURN
1002               ;*************************************************************************
1003               ;  ROUTINE TO CONVERT FROM HEX BYTE TO 3-DIGIT ASCII DECIMAL
1004               ;    ( PAGE 154 '6502 SOFTWARE DESIGN' ) .
1005
1006 FD9F  A0 00     HX2ASC LDY   #00
1007 FDA1  C9 64     HX2    CMP   #100             ; FIND NUMBER OF HUNDREDS
1008 FDA3  90 05            BCC   GOTHUN
1009 FDA5  E9 64            SBC   #100
1010 FDA7  C8               INY
1011 FDA8  D0 F7            BNE   HX2
1012 FDAA  20 C4 FD  GOTHUN JSR   HCONV            ; CONVERT TO ASCII
1013 FDAD  84 9A            STY   NUM+2           ; AND SAVE IT
1014 FDAF  A0 00            LDY   #00
1015 FDB1  C9 0A     HX3    CMP   #10              ; FIND NUMBER OF TENS
1016 FDB3  90 05            BCC   GOTTEN
1017 FDB5  E9 0A            SBC   #10
1018 FDB7  C8               INY
1019 FDB8  D0 F7            BNE   HX3
1020 FDBA  20 C4 FD  GOTTEN JSR   HCONV            ; CONVERT TO ASCII
1021 FDBD  84 99            STY   NUM+1           ; SAVE TENS DIGIT
1022 FDBF  09 30            ORA   #$30
1023 FDC1  85 98            STA   NUM             ; SAVE ONES DIGIT
1024 FDC3  60               RTS
1025
```

```
1026 FDC4  48          HCONV  PHA
1027 FDC5  98                 TYA
1028 FDC6  09 30              ORA   #$30              ; CONVERT ABSOLUTE NUMBER TO ASCII
1029 FDC8  A8                 TAY
1030 FDC9  68                 PLA
1031 FDCA  60                 RTS
1032               ;*********************************************************************
1033
1034 FDCB  20 D7 FD    NEWCXR JSR   NEWCR               ; UPDATE BOTH RECEIVER AND TRANSMITTER REGS
1035
1036 FDCE  A9 08       NEWCX  LDA   #$08                ; UPDATE MODEM'S TRANSMITTER REGISTERS
1037 FDD0  0D 0E 20           ORA   XMTE
1038 FDD3  8D 0E 20           STA   XMTE
1039 FDD6  60                 RTS
1040
1041 FDD7  A9 08       NEWCR  LDA   #$08                ; UPDATE MODEM'S RECEIVER REGISTERS
1042 FDD9  0D 0E 10           ORA   RCVE
1043 FDDC  8D 0E 10           STA   RCVE
1044 FDDF  60                 RTS
```



```
1046               ;*********************************************************************
1047               ; "<CR>" COMMAND   ---   CARRIAGE RETURN:  SEND OUT RESPONSE MESSAGE
1048               ;                          OR GO INTO DATA MODE IF REQUESTED AND
1049               ;                          IF CARRIER SIGNAL ACTIVE.
1050
1051 FDE0  A5 7D       CR     LDA   STCODE              ; CHECK STATUS OF PREVIOUS COMMANDS
1052 FDE2  D0 31              BNE   HOP                 ; BRANCH IF NOT "OK"
1053 FDE4  7F 80 2E           BBR   7,WAITF6,HOP        ; BRANCH IF WE ARE NOT TO WAIT FOR A CARRIER SIGNAL
1054 FDE7  A9 01              LDA   #$01                ; WAIT UNTIL DIAL REGISTER IS EMPTY
1055 FDE9  2C 0E 20    WAITDB BIT   XMTE                ; EMPTY YET ?
1056 FDEC  F0 FB              BEQ   WAITDB              ; NO ==> CHECK AGAIN ...
1057 FDEE  FF 77 05    CR2    BBS   7,REVFLG,CARTIM     ; YES==> CHECK FOR "REVERSE" DIAL --> BRANCH IF
1058                                                     ;        WE ARE REVERSE DIALING ( DON'T CLOSE OUT DIALING JUST YET)
1059 FDF1  A9 FF              LDA   #$FF                ;  MUST BE 2400 OR NORMAL 300/1200 BAUD DIAL.
1060 FDF3  8D 00 20           STA   XMTO                ;   --> CLOSE DIAL MODE AND GO TO DATA MODE.
1061
1062                                                     ;    IF WE WERE AT 300 BAUD AND DIALING "REVERSE"
1063                                                     ;  MODE THEN WE WOULD HAVE TO WAIT FOR A CARRIER
1064                                                     ;  SIGNAL BEFORE REVERSING THE MODEM TO "ANSWER"
1065                                                     ;  MODE.  THEN WE WRITE AN $FF TO "XMTO" TO CLOSE
1066                                                     ;  OUT THE DIAL SEQUENCE.
1067
1068 FDF6  20 D3 FE    CARTIM JSR   STRTB3              ; START CNTR-B FOR SECONDS-LONG TIME INTERVAL
1069 FDF9  A5 8D              LDA   S7                  ; SET UP SECONDS COUNTER ( SET BY "COMMA" COMMAND )
1070 FDFB  85 46              STA   DELAYS
1071 FDFD  4F 01 18    WCARIR BBR   4,PB,GOTCAR         ; BRANCH IF CARRIER DETECTED
1072 FE00  8F 16 03           BBS   0,SCSR,NOCARR       ; BRANCH (EXIT) IF A KEY HAS BEEN TYPED
1073 FE03  7F 81 F7           BBR   7,WAITC,WCARIR      ; BRANCH IF WAIT TIME HAS NOT EXPIRED
1074 FE06  57 12       NOCARR RMB   5,IER               ; DISABLE TIMER B IRQ
```

```
1075 FE08  A5 1C           LDA   CNTBCL          ;  AND CLEAR CNTB FLAG
1076 FE0A  77 80           RMB   7,WAITFG        ; TURN OFF WAIT FLAG
1077 FE0C  87 01           SMB   0,PB            ; DIRECT ALL OUTPUT TO HOST SYSTEM
1078 FE0E  A9 03           LDA   #$03            ; INDICATE "NO CARRIER"
1079 FE10  85 7D           STA   STCODE
1080 FE12  20 A7 FC        JSR   HHZERO          ; HANG UP THE PHONE ....
1081 FE15  4C AF FE  HOP   JMP   NOWAIT          ;  AND RETURN TO "RESTRT"
1082
1083 FE18  57 12     GOTCAR RMB   5,IER          ; GOT A CARRIER --> DISABLE TIMER B IRQ
1084 FE1A  A9 FF           LDA   #$FF            ; FINISH UP DIALING (IN CASE OF REVERSE DIAL)
1085 FE1C  8D 00 20        STA   XMTO
1086 FE1F  A9 01           LDA   #$01            ; INDICATE CARRIER DETECTED
1087 FE21  85 7D           STA   STCODE
1088 FE23  7F 7C 02        BBR   7,SPKRFG,GOTCR1 ; LEAVE SPEAKER ALONE IF FLAG IS NOT SET
1089 FE26  E7 01           SMB   6,PB            ; CARRIER DETECTED --> TURN SPEAKER OFF
1090 FE28  20 E8 FE  GOTCR1 JSR   RESPNS          ;  AND OUTPUT " CONNECT" MESSAGE, IF ENABLED
1091 FE2B  07 01           RMB   0,PB            ; THEN DIRECT ALL OUTPUT TO MODEM
1092 FE2D  A9 00     GOTCR2 LDA   #00             ; RESET ESCAPE CODE COUNTER
1093 FE2F  85 82           STA   ESCCNT
1094 FE31  20 BB FE  GOTCR3 JSR   STRTB1          ; START TIMER-B FOR GUARD-TIME COUNTER
1095 FE34  4F 01 11  INCHAR BBR   4,PB,INCHR2     ; BRANCH IF CARRIER STILL DETECTED
1096 FE37  20 C9 FE        JSR   STRTB2          ; CARRIER LOST --> WAIT FOR S10 TENTHS-OF-SECONDS
1097 FE3A  A5 90           LDA   S10             ;   FOR CARRIER TO RETURN -- OTHERWISE INDICATE
1098 FE3C  85 46           STA   DELAYS          ;   LOSS OF CARRIER AND RETURN TO COMMAND MODE
1099 FE3E  FF 81 C5  CARCK2 BBS   7,WAITC,NOCARR  ; BRANCH IF THE TIME-OUT FLAG GOES TRUE
1100 FE41  CF 01 FA        BBS   4,PB,CARCK2     ; BRANCH IF CARRIER STILL LOST
1101 FE44  A5 16           LDA   SCSR            ; CARRIER DETECTED AGAIN BEFORE TIME-OUT-->CLEAR SERIAL FLAGS
1102 FE46  57 12           RMB   5,IER           ; DISABLE IRQ
1103 FE48  A5 16     INCHR2 LDA   SCSR            ; WAIT FOR RECEIVED CHAR FROM HOST COMPUTER
1104 FE4A  29 0F           AND   #$0F            ; CHAR RECEIVED ?
1105 FE4C  F0 E6           BEQ   INCHAR          ; NO ==> CHECK AGAIN
1106 FE4E  4A        CHKCHR LSR   A               ; YES==> CHECK FOR PROPER RECEPTION
```



```
1107 FE4F  B0 06           BCS   CHKOK           ; BRANCH IF CHAR OK
1108 FE51  A9 04           LDA   #04             ; CHAR NOT OK --> ERROR ....
1109 FE53  85 7D           STA   STCODE
1110 FE55  D0 58           BNE   NOWAIT          ; INDICATE ERROR AND START OVER  ( BRA )
1111
1112 FE57  A5 17     CHKOK LDA   SRDR            ; CHAR OK --> FETCH IT
1113 FE59  20 51 FF        JSR   CHROUT          ;  AND SEND IT TO MODEM
1114 FE5C  FF 7A 0A        BBS   7,DUPLEX,ESCCHK ; BRANCH IF CHAR IS NOT TO BE ECHOED BACK
1115 FE5F  87 01           SMB   0,PB            ; ECHO --> DIRECT OUTPUT TO HOST COMPUTER
1116 FE61  20 51 FF        JSR   CHROUT          ; ECHO CHAR BACK
1117 FE64  6F 16 FD  WAITDP BBR   6,SCSR,WAITDP  ; WAIT UNTIL CHAR IS SENT OUT
1118 FE67  07 01           RMB   0,PB            ;  AND REDIRECT OUTPUT BACK TO MODEM
1119
1120                 ;  NOW CHECK FOR POSSIBLE ESCAPE CODE SEQUENCE ....
1121
1122 FE69  C5 88     ESCCHK CMP   S2             ; WAS CHAR AN "ESCAPE" CHAR ?
1123 FE6B  D0 C4           BNE   GOTCR3          ; NO ==> GET NEXT CHAR
1124 FE6D  A5 82           LDA   ESCCNT          ; YES==> IS IT THE FIRST "ESCAPE" CHAR ?
1125 FE6F  F0 06           BEQ   ESCHK2          ; YES==> CHECK FOR ELAPSED TIME SINCE PREV CHAR
```

```
1126 FE71  24 81           BIT   WAITC          ; HAS GUARD TIME ELAPSED ?
1127 FE73  30 B8           BMI   GOTCR2         ; YES==> WAITED TOO LONG; ESCAPE NO LONGER VALID
1128 FE75  10 03           BPL   ESCHK3         ; NO ==> ADD 1 TO ESCAPE COUNT ( BRANCH ALWAYS )
1129 FE77  7F 81 B7  ESCHK2 BBR   7,WAITC,GOTCR3 ; BRANCH IF GUARD TIME HAS NOT ELAPSED
1130 FE7A  E6 82     ESCHK3 INC   ESCCNT        ; INCREMENT ESCAPE CODE COUNTER
1131 FE7C  A5 82            LDA   ESCCNT        ; IS THIS THE THIRD SEQUENTIAL "ESCAPE" CODE ?
1132 FE7E  C9 03            CMP   #03
1133 FE80  D0 AF            BNE   GOTCR3        ; NO ==> GET NEXT CHAR
1134 FE82  20 BB FE         JSR   STRTB1        ; YES==> RESTART GUARD-TIMER
1135 FE85  4F 01 13  LSTCHK BBR   4,PB,LSTCK2   ; NOW WAIT FOR 1 GUARD-TIME INTERVAL FOR A CHARACTER
1136                                            ; ( BRANCH IF CARRIER IS OK )
1137 FE88  20 C9 FE         JSR   STRTB2        ; CARRIER LOST --> WAIT FOR S10 TENTHS-OF-SECONDS
1138 FE8B  A5 90            LDA   S10           ;   FOR CARRIER TO RETURN -- OTHERWISE INDICATE
1139 FE8D  85 46            STA   DELAYS        ;   LOSS OF CARRIER AND RETURN TO COMMAND MODE
1140 FE8F  FF 81 AC  CARCK3 BBS   7,WAITC,CARCK2 ; BRANCH IF THE TIME-OUT FLAG GOES TRUE
1141 FE92  CF 01 FA         BBS   4,PB,CARCK3   ; BRANCH IF CARRIER STILL LOST
1142 FE95  A5 16            LDA   SCSR          ; CARRIER DETECTED AGAIN BEFORE TIME-OUT-->CLEAR SERIAL FLAGS
1143 FE97  57 12            RMB   5,IER         ; DISABLE IRQ
1144 FE99  D0 92            BNE   GOTCR2        ; LOSS OF CARRIER ABORTS ESCAPE SEQUENCE --> BRANCH ALWAYS
1145
1146 FE9B  A5 16     LSTCK2 LDA   SCSR
1147 FE9D  29 0F            AND   #$0F          ; IF A CHARACTER HAS BEEN ENTERED BEFORE
1148 FE9F  D0 8C            BNE   GOTCR2        ; THE GUARD-TIME INTERVAL HAS ELAPSED, THEN THE ESCAPE
1149 FEA1  7F 81 E1         BBR   7,WAITC,LSTCHK ; SEQUENCE IS ABORTED AND CHAR IS HANDLED IN THE
1150                                            ;  USUAL FASHION ( AT "CHKCHR" ).  IF TIMER HAS
1151                                            ;  ELAPSED THEN ESCAPE SEQUENCE IS COMPLETED WITH A
1152                                            ;  RETURN TO COMMAND MODE.
1153
1154 FEA4  57 12     ESCAPE RMB   5,IER         ; STOP TIMER B IRQ
1155 FEA6  6F 16 FD  ESC2   BBR   6,SCSR,ESC2   ; WAIT UNTIL ALL CHARS ARE TRANSMITTED OUT
1156 FEA9  87 01            SMB   0,PB          ; THEN DIRECT OUTPUT TO HOST COMPUTER
1157
1158
1159 FEAB  A9 00            LDA   #00           ; RESET RESULT CODE TO "OK"
1160 FEAD  85 7D            STA   STCODE
1161 FEAF  68        NOWAIT PLA                 ; GET RID OF RETURN ADDRESS FROM "JSR DOCMD"
1162 FEB0  68               PLA                 ;  ( OR "JSR AAA" AT LABLE "ANSWER" )
1163 FEB1  20 E8 FE         JSR   RESPNS        ; SEND OUT RESPONSE, IF ENABLED
1164 FEB4  A9 00            LDA   #00           ; RESET RING COUNTER TO ZERO
1165 FEB6  85 87            STA   S1
1166 FEB8  4C 16 F8         JMP   RESTRT        ; AND START ALL OVER AGAIN
1167
```

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```
1168                ; ********************************************************************************
1169
1170                ;    1/50 SEC (20MS) DELAY
1171
1172 FEBB  A5 92    STRTB1 LDA   S12            ; SET DELAY COUNTER FOR NUMBER OF 20MS GUARD-TIME INTERVALS
1173 FEBD  85 46           STA   DELAYS
1174 FEBF  57 12           RMB   5,IER          ; DISABLE IRQ
1175 FEC1  A9 01           LDA   #ESCDLY        ; SET UP DELAY PARAMETERS
1176 FEC3  A2 9C           LDX   #<ESCTIM
```

```
1177 FEC5  A0 47          LDY   #>ESCTIM
1178 FEC7  D0 12          BNE   STRTIM          ;  ... AND START TIMER ...
1179
1180                ;   1/10 SEC DELAY
1181
1182 FEC9  57 12    STRTB2 RMB   5,IER         ; DISABLE IRQ
1183 FECB  A9 10           LDA   #DLYHIB        ; SET UP DELAY PARAMETERS FOR 1/10 SEC
1184 FECD  A2 60           LDX   #<TENTHD
1185 FECF  A0 67           LDY   #>TENTHD
1186 FED1  D0 08           BNE   STRTIM          ;  ... AND START TIMER ...  ( BRA )
1187
1188                ;   1 SECOND DELAY
1189
1190 FED3  57 12    STRTB3 RMB   5,IER         ; DISABLE IRQ
1191 FED5  A9 10           LDA   #DLYHIB        ; SET UP DELAY PARAMETERS FOR 1 SEC. DELAY
1192 FED7  A2 9C           LDX   #<DLYTIM
1193 FED9  A0 E0           LDY   #>DLYTIM
1194 FEDB  86 1C    STRTIM STX   CNTBCL        ; LOAD COUNTER-B
1195 FEDD  84 1E           STY   CNTBHL
1196 FEDF  85 44           STA   DELAYC         ; SET IRQ COUNTER
1197 FEE1  85 45           STA   DELAYT
1198 FEE3  77 81           RMB   7,WAITC        ; SET TIME-OUT FLAG FALSE
1199 FEE5  D7 12           SMB   5,IER          ; ENABLE CNTR-B IRQ
1200 FEE7  60              RTS
```

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```
1202 FEE8  20 40 FF RESPNS JSR   CRLF
1203 FEEB  FF 7B 1E        BBS   7,RSLTFG,QRSP  ; BRANCH IF STATUS RESPONSE IS DISABLED
1204 FEEE  A5 7D           LDA   STCODE         ; GET CODE VALUE
1205 FEF0  C9 01           CMP   #$01           ; IF "CARRIER" RESPONSE, CHECK FOR EXTENDED CODE
1206 FEF2  D0 0D           BNE   RSP2           ; NOT "CARRIER" --> BRANCH ...
1207 FEF4  7F 7F 0A        BBR   7,XCODE,RSP2   ; BRANCH IF EXTENDED CODE SET IS NOT TO BE USED
1208 FEF7  A4 41           LDY   BAUD           ; IS SYSTEM RUNNING AT 1200 BAUD ?
1209 FEF9  C0 03           CPY   #$03           ;
1210 FEFB  F0 04           BEQ   RSP2           ; NO ==> BRANCH ...
1211 FEFD  A9 05           LDA   #$05           ; YES==> INDICATE 1200/2400 BAUD CARRIER
1212 FEFF  85 7D           STA   STCODE         ;  AND SAVE IT
1213 FF01  FF 7E 09 RSP2   BBS   7,VCODE,VERBAL ; BRANCH IF RESPONSE IS TO BE VERBAL
1214 FF04  09 30    NUMERC ORA   #$30           ; CONVERT RESPONSE CODE TO ASCII
1215 FF06  20 51 FF        JSR   CHROUT         ;  AND SEND IT OUT
1216 FF09  20 40 FF        JSR   CRLF           ;  FOLLOWED BY <CR/LF>
1217 FF0C  60       QRSP   RTS                  ; RETURN
1218
1219 FF0D  A4 7D    VERBAL LDY   STCODE         ; DETERMINE WHICH MESSAGE TO SEND OUT
1220 FF0F  F0 20           BEQ   RSPOK          ; 0 ==> "OK"
1221 FF11  88              DEY
1222 FF12  F0 19           BEQ   RSPCAR         ; 1 ==> "CARRIER"
1223 FF14  88              DEY
1224 FF15  F0 12           BEQ   RSPRNG         ; 2 ==> "RING"
1225 FF17  88              DEY
1226 FF18  F0 0B           BEQ   RSPNC          ; 3 ==> "NO CARRIER"
1227 FF1A  88              DEY
1228 FF1B  F0 04           BEQ   RSPERR         ; 4 ==> "ERROR"
```

5

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1229
1230 FF1D  A0 1C     RSPC12 LDY   #CON12M-MSG      ; 5 ==> "CONNECT 1200/2400"
1231 FF1F  D0 12            BNE   MSGOUT
1232 FF21  A0 17     RSPERR LDY   #ERRMSG-MSG
1233 FF23  D0 0E            BNE   MSGOUT
1234 FF25  A0 0D     RSPNC  LDY   #NOCARM-MSG
1235 FF27  D0 0A            BNE   MSGOUT
1236 FF29  A0 09     RSPRNG LDY   #RNGMSG-MSG
1237 FF2B  D0 06            BNE   MSGOUT
1238 FF2D  A0 02     RSPCAR LDY   #CARMSG-MSG
1239 FF2F  D0 02            BNE   MSGOUT
1240 FF31  A0 00     RSPOK  LDY   #OKMSG-MSG
1241
1242 FF33  B9 7A FF  MSGOUT LDA   MSG,Y           ; GET CHAR FROM MESSAGE TABLE
1243 FF36  48               PHA                   ; SAVE CHARACTER
1244 FF37  C8               INY                   ; POINT TO NEXT CHAR
1245 FF38  29 7F            AND   #$7F            ; MASK OFF MSB
1246 FF3A  20 51 FF         JSR   CHROUT          ; AND SEND OUT CHAR
1247 FF3D  68               PLA                   ; RESTORE SIGN BIT
1248 FF3E  10 F3            BPL   MSGOUT          ; BRANCH IF MORE CHARS TO BE SENT
1249 FF40  A5 89     CRLF   LDA   S3              ; ( S3 CONTAINS CURRENT <CR> )
1250 FF42  20 51 FF         JSR   CHROUT          ; SEND OUT <CR>
1251 FF45  7F 7E 05         BBR   7,VCODE,WAITLF  ; BYPASS <LF> IF NUMERIC RESPONSE SELECTED
1252 FF48  A5 8A            LDA   S4              ; ( S4 CONTAINS CURRENT <LF> )
1253 FF4A  20 51 FF         JSR   CHROUT          ; OUTPUT <LF>
1254 FF4D  7F 16 FD  WAITLF BBR   7,SCSR,WAITLF   ; WAIT UNTIL <LF> IS FINISHED
1255 FF50  60               RTS                   ;  THEN RETURN
1256
1257 FF51  6F 16 FD  CHROUT BBR   6,SCSR,CHROUT   ; WAIT TILL TRANSMITTER BUFFER IS EMPTY
1258 FF54  85 17            STA   STDR            ;  THEN SEND OUT CHAR
1259 FF56  60               RTS
```



```
1261
1262                ; INTERRUPT SERVICE ROUTINE
1263
1264 FF57  48       ISR    PHA
1265 FF58  A5 1C            LDA   CNTBCL          ; CLEAR TIMER B FLAG
1266 FF5A  FF 78 0D         BBS   7,IRQFLG,CARIER ; BRANCH IF IRQ IS FOR WAIT-FOR-CARRIER DELAY
1267 FF5D  A5 00            LDA   PA              ;  ECHO SERIAL IN TO SERIAL OUT
1268 FF5F  0A               ASL   A
1269 FF60  90 04            BCC   SET0
1270 FF62  E7 00     SET1   SMB   6,PA
1271 FF64  B0 12            BCS   QISR            ;  (BRANCH ALWAYS)
1272 FF66  67 00     SET0   RMB   6,PA
1273 FF68  90 0E            BCC   QISR            ;  (BRANCH ALWAYS)
1274
1275 FF6A  C6 44     CARIER DEC   DELAYC          ; IS TIMER COUNTER = 0 ?
1276 FF6C  D0 0A            BNE   QISR            ; NO ==> RETURN
1277 FF6E  A5 45            LDA   DELAYT          ; YES==> RESET IT
```

```
1278 FF70  85 44            STA   DELAYC
1279 FF72  C6 46            DEC   DELAYS          ; IS SECONDS COUNTER = 0 ?
1280 FF74  D0 02            BNE   QISR            ; NO ==> RETURN
1281 FF76  F7 81            SMB   7,WAITC         ; YES==> SET TIME-OUT FLAG
1282 FF78  68          QISR  PLA
1283 FF79  40          NMIRTN RTI


1285 FF7A              MSG   =     *
1286
1287 FF7A  4F          OKMSG  .SBY   'OK'
1288 FF7C  43          CARMSG .SBY   'CONNECT'
1289 FF83  52          RNGMSG .SBY   'RING'
1290 FF87  4E          NOCARM .SBY   'NO CARRIER'
1291 FF91  45          ERRMSG .SBY   'ERROR'
1292 FF96  43          CON12M .SBY   'CONNECT 1200/2400'
1293
1294 FFA7  2A          CHKSUM .SBY   '****'
1295 FFAB  36          PCODE  .SBY   '6500'
1296
1297 FFAF                     *=$FFFA
1298
1299 FFFA  79 FF              .WOR   NMIRTN
1300 FFFC  00 F8              .WOR   RESET
1301 FFFE  57 FF              .WOR   ISR
1302
1303                          .END   MDM10A

ERRORS = 0000 <0000>
```

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SYMBOL TABLE

```
AAA     FC0D     0489  0509 #0726
ABIT8   0048    #0044  0179  0263  0313  0316  0330
ABIT9   0049    #0045  0180  0268  0309
ALLIN   F9DD     0414 #0422
ANSWER  FA42     0485 #0488
BAUD    0041    #0037  0378  0900  1208
BAUD12  002F    #0126  0357  0553  0555
BAUD24  0017    #0127
BAUD3   00BF    #0125  0351
BDRATH  0043    #0039  0215  0341  0347  0477  0556
BDRATL  0042    #0038  0223  0342  0345  0350  0475  0554
BD2     F974     0356  0362 #0366
BS      F9BF     0401 #0404
BUFFLG  0075    #0050  0186  0418  0422
B03     F95A    #0353
B12     F966    #0359
B24     F96E     0358 #0363
CARCK2  FE3E    #1099  1100  1140
CARCK3  FE8F    #1140  1141
CARIER  FF6A     1266 #1275
CARMSG  FF7C     1238 #1288
```

```
CARTIM FDF6    0870  1057 #1068
CCC    FC28    0509 #0743
CCONE  FC2F   #0746
CCZERO FC38    0744  0745 #0750
CHKCHR FE4E   #1106
CHKOK  FE57    1107 #1112
CHKSUM FFA7    0839 #1294
CHROUT FF51    0394  0403  0409  0716  1113  1116  1215  1246  1250  1253
              #1257  1257
CMDTBL FA47    0448 #0497
CMDVEC 009B   #0089  0436  0461  0463
CNTACL 001B   #0025  0205  0217  0224  0235  0260  0265  0279  0296  0301
               0346  0476
CNTAH  0019   #0026  0213
CNTAL  001A   #0027  0206  0227  0229  0247  0274  0276  0348  0478
CNTBCL 001C   #0030  0198  0583  0588  1075  1194  1265
CNTBHC 001D   #0031
CNTBHL 001E   #0032  0200  0585  1195
COMMA  FB1E    0505 #0579  0774
CON12M FF96    1230 #1292
CR     FDE0    0425  0512  0620  0639  0921 #1051
CRLF   FF40    0710  0719  0835  0983  1202  1216 #1249
CR2    FDEE    0735 #1057
CTLCOD F9AC    0393 #0395
DDD    FC44    0509 #0760
DEFPRO 0040   #0036  0339  0473  0558
DELAYC 0044   #0040  1196  1275  1278
DELAYS 0046   #0042  1070  1098  1139  1173  1279
DELAYT 0045   #0041  1197  1277
DELETE F9C3   #0406
DIGERR FB54    0601 #0618  0645
DIGIT  FB3C    0506  0507 #0601
DIG2   FB4E    0612 #0614
DILFLG 0076   #0051  0184  0546  0601  0627  0628  0777  0899  0904
DLYHIB 0010   #0119  0586  1183  1191
DLYTIM E09C   #0120  0582  0584  1192  1193
DOCMD  F9F2    0434 #0436
DUPLEX 007A   #0055  0550  0801  0803  1114
ECHOFG 0079   #0054  0196  0393  0549  0789  0791
```


SYMBOL TABLE

```
EEE    FC72    0509 #0786
EONE   FC79   #0789
EQUAL  FB76    0508 #0645
EQ2    FBA2    0654  0659 #0665
EQ3    FBAD    0666 #0670
EQ4    FBBC    0651  0671 #0677
ERRMSG FF91    1232 #1291
ESCAPE FEA4   #1154
ESCCHK FE69    1114 #1122
ESCCNT 0082   #0063  1093  1124  1130  1131
ESCDLY 0001   #0122  1175
```

```
ESCHK2 FE77    1125 #1129
ESCHK3 FE7A    1128 #1130
ESCTIM 479C   #0123  1176  1177
ESC2   FEA6   #1155  1155
EVEN7  F929    0317 #0327
EVEN8  F91D    0310 #0321
EZERO  FC7D    0787  0788 #0791
FFF    FC80    0509 #0798
FNDCMD F9F5    0432 #0444
FONE   FC87   #0801
FOUND  FA0D    0449 #0457
FOUNDA F8AD    0244 #0259  0259
FOUNDS F8EF    0288 #0293
FOUNDT F8F1    0290 #0295  0295
FZERO  FC8B    0799  0800 #0803
GETCHR F9A4   #0392
GETNUM FD8E    0650  0653  0658  0743  0786  0798  0810  0836  0851  0886
               0929  0933  0958  0970 #0992
GOCR   FA0B    0447 #0455
GOTCAR FE18    1071 #1083
GOTCHR F9CD    0396  0405 #0412
GOTCR1 FE28    1088 #1090
GOTCR2 FE2D   #1092  1127  1144  1148
GOTCR3 FE31   #1094  1123  1129  1133
GOTHUN FDAA    1008 #1012
GOTTEN FDBA    1016 #1020
GO2RES F8A7   #0250
GT300  F962    0352 #0357
HCONV  FDC4    1012  1020 #1026
HHH    FC8E    0509 #0810
HHSET  FCB7    0820 #0827
HHZERO FCA7    0811  0812 #0821  1080
HOP    FE15    1052  1053 #1081
HX2    FDA1   #1007  1011
HX2ASC FD9F    0713 #1006
HX3    FDB1   #1015  1019
H1AND2 FC95    0726 #0813  0868
IER    0012   #0019  0201  0349  0469  0528  1074  1083  1102  1143  1154
               1174  1182  1190  1199
IFR    0011   #0018  0192  0207  0228  0234  0248  0259  0264  0275  0278
               0295  0300  0470  0527  0587
III    FCBB    0510 #0835
IIONE  FCC5   #0839
IIZERO FCC9    0837  0838 #0841
INBUFF 004C   #0048  0412  0445  0569  0605  0992
INCHAR FE34   #1095  1105
INCHR2 FE48    1095 #1103
INITSW FABE    0140 #0526
IRQFLG 0078   #0053  0202  0380  0488  1266
```

5

SYMBOL TABLE

```
ISR     FF57    #1264  1301
LABEL1  F93D     0320  0323  0326  0329  0334 #0338
LOOP2   F9FD    #0448  0452
LSTCHK  FE85    #1135  1149
LSTCK2  FE9B     1135 #1146
L1      F857    #0207  0208
L10     F8D4    #0278  0278  0284
L12     F8FB    #0300  0300
L2      F85F    #0210  0210
L3      F87D    #0228  0228
L4      F889    #0234  0234  0240
L4A     F8A1    #0248  0248
L5      F8A4    #0249  0249
L6      F8B7    #0264  0264
L7      F8C1    #0269  0269
L8      F8C4    #0270  0270
L9      F8CD    #0275  0275
MCR     0014    #0020  0138  0194  0195  0221  0222  0472
MMM     FCCF     0510 #0850
MMONE   FCDC    #0856
MMTWO   FCDE     0855 #0857
MMZERO  FCE3     0852  0853 #0859
MSG     FF7A     0839  0841  1230  1232  1234  1236  1238  1240  1242 #1285
MSGOUT  FF33     0842  1231  1233  1235  1237  1239 #1242  1248
MULT10  FBEC     0667  0672  0673 #0699
NEWCR   FDD7     0191  1034 #1041
NEWCX   FDCE     0733  0753  0767  0879  0951 #1036
NEWCXR  FDCB     0377  0696  0827  0916 #1034
NMIRTN  FF79    #1283  1299
NOCARM  FF87     1234 #1290
NOCARR  FE06     1072 #1074  1099
NODLAY  FB39     0581 #0593
NOIRQ   F850     0196 #0203
NOPAR   F92F     0315 #0330
NOPAR7  F939     0331 #0335
NOPARB  F933    #0332
NOSLFT  FBC6    #0682
NOTNUM  FD9D     0994 #1000
NOWAIT  FEAF     1081  1110 #1161
NUM     0098    #0088  0647  0648  0649  0652  0655  0656  0657  0660  0661
                 0662  0663  0664  0665  0668  0669  0670  0675  0676  0677
                 0715  0932  0936  0937  1013  1021  1023
NUMCMD  0021    #0129  0451  0455
NUMERC  FF04    #1214
NXTCMD  F9E9    #0432  0435
ODD7    F917    #0318
ODD8    F923     0312 #0324
OKMSG   FF7A     1240 #1287
ONESEC  FB2C    #0586  0592
ODD     FCE6     0510 #0868
PA      0000    #0013  0208  0209  0210  0230  0236  0249  0261  0266  0269
                 0270  0280  0297  0302  1267  1270  1272
PB      0001    #0014  0142  0143  0144  0145  0146  0354  0360  0364  0857
                 0859  1071  1077  1089  1091  1095  1100  1115  1118  1135
```

```
                1141  1156
PCODE   FFAB    0841 #1295
PPP     FCEE    0510 #0876
QCCC    FC3D    0748  0749 #0752
QDIGIT  FB53   #0616
QECHO   FC7F    0790 #0792
```



```
SYMBOL TABLE

QEQ     FBE8    0688 #0696
QFFF    FC8D    0802 #0804
QGETN   FD9E    0996  0999 #1001
QHHH    FCBA   #0828
QII     FCCB    0840 #0842
QISR    FF78    1271  1273  1276  1280 #1282
QMMM    FCE5    0858 #0860
QQ      FD07    0890 #0892
QQDNE   FD01   #0889
QQQ     FCFA    0510 #0886
QQZERO  FD05    0887  0888 #0891
QRRR    FD32    0902 #0917
QRSP    FF0C    1203 #1217
QSSS    FD57    0930  0931 #0941
QUESTN  FBF4    0508 #0710
QUES3   FC00   #0715  0718
QVVV    FD73    0962 #0964
QXXX    FD81    0974 #0976
RCV     1000   #0092  0094
RCVA    100A   #0098  0367  0370  0534  0683  0684  0691  0692
RCVB    100B   #0099
RCVC    100C   #0100  0375  0537
RCVD    100D   #0101  0188  0190  0532  0817  0819  0824  0826  0910  0911
RCVE    100E   #0102  0539  1042  1043
RCVF    100F   #0103
RCV2    1002   #0095
RCV8    1008   #0096
RCV9    1009   #0097
REPEAT  F9E7    0386  0422 #0427
REPFLG  0074   #0049  0178  0293  0386
RERROR  FD33    0899 #0919
RESET   F800   #0133  0985  1300
RESPNS  FEE8    0481  0982  1090  1163 #1202
RESTRT  F816   #0176  0250  0291  0486  1166
REVFLG  0077   #0052  0779  0905  1057
RING    F8AA    0207 #0252
RINGNG  FA1C    0252 #0469
RNGMSG  FF83    1236 #1289
ROTATE  F943   #0341  0344
RRR     FD08    0510 #0899
RSLTFG  007B   #0056  0547  0889  0891  1203
RSPCAR  FF2D    1222 #1238
RSPC12  FF1D   #1230
RSPERR  FF21    1228 #1232
```

```
RSPNC  FF25    1226 #1234
RSPOK  FF31    1220 #1240
RSPRNG FF29    1224 #1236
RSP2   FF01    1206  1207  1210 #1213
SCCR   0015   #0021  0177  0338  0474
SCSR   0016   #0022  0381  0388  0984  1072  1101  1103  1117  1142  1146
               1155  1254  1257
SEMERR FB6F    0627 #0637
SEMIC  FB5B    0508 #0627
SEMI2  FB62   #0630  0631
SETPTR F99C   #0387  0410
SET0   FF66    1269 #1272
SET1   FF62   #1270
SLFTST FBDB    0681 #0690
SLOOP  FB11   #0564  0567
SPKRFG 007C   #0057  0552  0850  0856  1088
```



```
SYMBOL TABLE

SRDR   0017   #0024  0392  1112
SREGP  0084   #0065  0560  0562  0565  0679  0712  0928  0939  0940
SSETFG 0083   #0064  0543  0645  0941
SSS    FD3A    0511 #0927
SS2    FD50    0934 #0937
STBL   FAAD   #0517  0564
STCODE 007D   #0058  0187  0424  0454  0480  0619  0638  0920  1051  1079
               1087  1109  1160  1204  1212  1219
STDR   0017   #0023  0024  1258
STRTB1 FEBB    1094  1134 #1172
STRTB2 FEC9    1096  1137 #1182
STRTB3 FED3    1068 #1190
STRTIM FEDB    1178  1186 #1194
S0     0086   #0069  0484  0559  0561  0927
S1     0087   #0070  0482  0483  0544  1165
S10    0090   #0079  1097  1138
S11    0091   #0080
S12    0092   #0081  1172
S13    0093   #0082
S14    0094   #0083
S15    0095   #0084
S16    0096   #0085  0680
S17    0097   #0086
S2     0088   #0071  1122
S3     0089   #0072  0395  0413  0446  0568  1249
S4     008A   #0073  1252
S5     008B   #0074  0402  0404
S6     008C   #0075  0772
S7     008D   #0076  1069
S8     008E   #0077  0580  0770  0773  0776
S9     008F   #0078
TBIT8  004A   #0046  0181  0299  0314
TBIT9  004B   #0047  0182  0304  0311
TEMP   009D   #0090  0366  0369  0373  0579  0593  0699  0702
```

```
TENTHD 6760    #0121  1184  1185
TESTB  0047    #0043  0183  0232  0238  0241  0271  0282  0285
TTT    FD5A     0511 #0948
VCODE  007E    #0059  0551  0961  0963  1213  1251
VECTBL FA69     0460  0462 #0505
VERBAL FF0D     1213 #1219
VONE   FD6D    #0961
VVV    FD66     0511 #0958
VZERO  FD71     0959  0960 #0963
WAITB  FB2E    #0587  0587  0590
WAITC  0081    #0062  1073  1099  1126  1129  1140  1149  1198  1281
WAITDB FDE9    #1055  1056
WAITDL FC59    #0768  0769
WAITDP FE64    #1117  1117
WAITFG 00B0    #0061  0185  0634  0734  0778  0869  1053  1076
WAITIN F99E    #0388  0390  0398  0399  0407  0417  0420
WAITLF FF4D     1251 #1254  1254
WAITRE FB41    #0603  0604
WCARIR FDFD    #1071  1073
XCODE  007F    #0060  0545  0973  0975  1207
XMT    2000    #0105  0107
XMTA   200A    #0112  0371  0374  0535  0686  0687  0694  0695
XMTB   200B    #0113  0530  0876  0878  0948  0950
XMTC   200C    #0114  0376  0538
XMTD   200D    #0115  0529  0728  0729  0763  0766  0813  0816  0821  0823
                0913  0915
```



```
SYMBOL TABLE

XMTE   200E    #0116  0540  0603  0630  1037  1038  1055
XMTF   200F    #0117
XMT0   2000    #0108  0615  0633  1060  1085
XMT2   2002    #0109
XMT8   2008    #0110  0768
XMT9   2009    #0111  0731  0732  0747  0751  0752  0761  0762  0907  0908
XONE   FD7B    #0973
XXX    FD74     0511 #0970
XZERO  FD7F     0971  0972 #0975
ZZWAIT FD88    #0984  0984
ZZZ    FD82     0511 #0982
.NARG  ****

END OF ASSEMBLY
```

Rockwell

Interfacing Rockwell Signal Processor-Based Modems To An Apple IIe Computer

by Carlos A. Laiz, Product Applications Engineer
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INTRODUCTION

This application note describes the electrical design of a module that interfaces an Apple IIe* computer to a Rockwell Signal Processor (SP)-based modem. The design incorporates an USART (8251A) for asynchronous/synchronous serial data transfer and control, and two digital-to-analog converters (DACs) for quadrature eye pattern generation. Memory mapped input/output (I/O) allows easy access to the modem interface memory for parallel control and data transfer. The interface module connects directly to the following modems with minor software differences required to switch between them:

- R1212M or R1212DC
- R2424M or R2424DC
- R48DP
- R96DP
- R96FT

Two assembly listings of sample software subroutines for R1212/R2424 automatic dialing and R48DP/R96DP eye pattern generation are also included.

HARDWARE DESIGN

The interface module schematic (Figure 1) shows the routing of signals between an Apple IIe peripheral slot, the USART, and the modem. The modem can physically be located outside the Apple IIe and connected by a short 64-conductor ribbon cable to a 64-pin DIN connector (with the same pin assignments) installed on the interface module.

The major devices on the interface module are the 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) and two NE5018 DACs. The USART (U1) allows the microprocessor to transfer data and control to the modem via the serial interface. This USART supports both asynchronous and synchronous data transfer modes. The two DACs, U8 and U9, generate the analog voltages to drive the eye pattern X-OUT and Y-OUT signals, respectively.

Address lines A0–A3 are directly connected to the modem register select inputs RS0-RS3. The Apple's partially decoded $\overline{\text{I/O SELECT}}$ (pin 1 in the Apple peripheral connector) is used to gate R/$\overline{\text{W}}$ to produce two separate READ and $\overline{\text{WRITE}}$ signals with the proper timing as required by the modem and the USART. $\overline{\text{I/O SELECT}}$ is active during $\phi 0$ clock when the microprocessor references page $Cn, where n is a peripheral slot number (1–7) in the Apple.

The data lines are buffered by U2 and routed to multiple destinations (U1, U8, U9 and the interfacing modem). U2 is enabled by $\overline{\text{I/O SELECT}}$ and the data direction is controlled by READ.

Address lines A4–A6 are decoded (U3) into eight chip select signals ($\overline{\$Cn0R}$–$\overline{\$Cn3R}$ and $\overline{\$Cn4X}$–$\overline{\$Cn7X}$). Addresses $\overline{\$Cn0R}$–$\overline{\$Cn3R}$ correspond to the modem chip select inputs ($\overline{CS0}$–$\overline{CS3}$). Writing to address $\overline{\$Cn4X}$ triggers U4 to generate a low level pulse (4 μs min.) causing the modem to initiate a Power On Reset (POR) cycle. Addresses $\overline{\$Cn5X}$ and $\overline{\$Cn6X}$ are used to write eye pattern data into the X-DAC and Y-DAC, respectively.

The USART's input line Control/$\overline{\text{Data}}$ (C/$\overline{\text{D}}$) is controlled by the address line A7. Address $\overline{\$Cn7X}$ (A7 = 0) is used to write to the transmitter register or to read the receiver register in the USART. Address $\overline{\$CnFX}$ (A7 = 1) is used to write to the USART Control register or to read its status register. The USART is supplied with $\phi 1$ clock directly from the Apple bus.

The I/O addresses and their functions are summarized in Table 1.

Table 1. Interface Module Memory Map

Address	Device Addressed/Function Performed
$\overline{\$Cn0R}$	Chip Select 0 (CS0)
$\overline{\$Cn1R}$	Chip Select 1 (CS1)
$\overline{\$Cn2R}$	Chip Select 2 (CS2)
$\overline{\$Cn3R}$	Chip Select 3 (CS3)
$\overline{\$Cn4X}$	POR (Power-On-Reset)
$\overline{\$Cn5X}$	X-DAC Latch Enable (XLE)
$\overline{\$Cn6X}$	Y-DAC Latch Enable (YLE)
$\overline{\$Cn7X}$	USART Chip Select (C/$\overline{\text{D}}$ = A7 = ϕ)
$\overline{\$CnFX}$	USART Chip Select (C/$\overline{\text{D}}$ = A7 = 1)

Notes:
n = Apple IIe peripheral slot number (1–7)
R = Modem register number (0–F)
X = Irrelevant

*Apple and Apple IIe are registered trademarks of Apple Computer, Inc

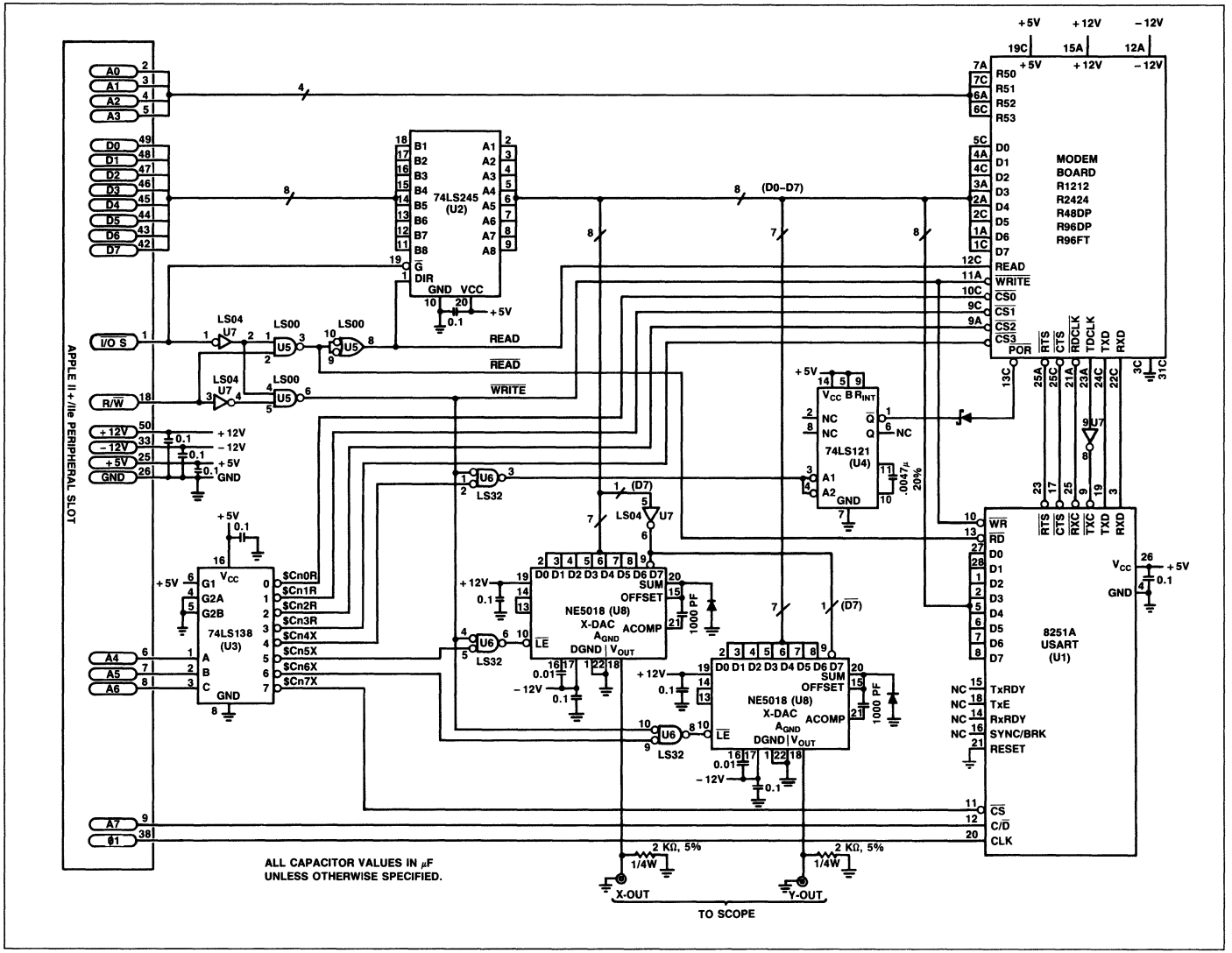

Figure 1. Apple IIe to Rockwell SP Modem Interface Schematic

SOFTWARE CONSIDERATIONS

Application software can easily control the modem, the USART and the two DACs via the addresses decoded on the interface module (Table 1). The location of bits and registers as well as diagnostic access codes vary between modems. Refer to the appropriate data sheet for specific bit and register locations and access codes.

Two example software subroutines are included in this application note for interfacing to an SP-based modem. These routines are written in 6502 assembly language.

The Automatic Dialer subroutine for the R1212/R2424 (Figure 2) implements the same function described and flowcharted in the R1212 and R2424 data sheets. The subroutine, as shown, starts at address $6000 but can be easily relocated. As written, it assumes that the interface module is installed in Apple IIe peripheral slot 4. The number to be dialed should be stored at $6100 and terminated with an $FF character.

The Eye Pattern Generator subroutine for the R48DP/R96DP (Figure 3) generates a continuous eye pattern in loop 3 (local analog loopback) by reading a signal point once per baud. The subroutine starts at $0300 and can also be easily relocated. Execution is halted and control returned to the calling routine when a key is pressed. The comments in the listing describe the detail operation.

```
                        1000        ORG $6000
                        1008 *
                        1016 ********************************************
                        1024 *     R1212/R2424 AUTOMATIC DIALER ROUTINE     *
                        1032 ********************************************
                        1040 *
                        1048 ********************************************
                        1056 * THE NUMBER TO BE DIALED SHOULD BE STORED AT  *
                        1064 * $6100. THIS PROGRAM ASSUMES THAT THE        *
                        1072 * INTERFACE BOARD IS IN SLOT 4. IT MAY BE     *
                        1080 * EXECUTED AS A SUBROUTINE FROM BASIC WITH A  *
                        1088 * "CALL 24576" OR A "JSR $6100" FROM ASSEMBLY. *
                        1096 ********************************************
                        1104 *
6000  AD 1B C4  1112        LDA $C41B
6003- 29 FD     1120        AND ##$FD       ;SET PULSE DIALING
6005- 8D 1B C4  1128        STA $C41B
6008- AD 1D C4  1136        LDA $C41D
6008  09 08     1144        ORA ##$08       ;SET ORO=1, BUS=1, DIR=1
600D  8D 1D C4  1152        STA $C41D
6010- AD 1E C4  1160        LDA $C41E
6013- 09 08     1168        ORA ##$08       ;SET NEWC (TRANSMITTER)
6015- 8D 1E C4  1176        STA $C41E
6018- A9 1B C4  1184 DLO    LDA #C41B
601B- 29 80     1192        AND ##80
601D- F0 F9     1200        BEQ DLO         ;DLO-- 1?
601F- A2 00     1208        LDX #$00        ;INITIALIZE DIGIT COUNTER
6021 - AD 1E C4  1216 DDRF  LDA $C41E
6024  29 01     1224        AND ##01        ;DDRE=1 ?
6026  F0 F9     1232        BEQ DDRL
6028- BD 00 61  1240        LDA $6100,X     ;GET DIGIT FROM BUFFER AT $6100
602B  8D 10 C4  1248        STA $C410       ;STORE DIGIT IN DDR
602E- E8        1256        INX
602F  E0 FF     1264        CMP ##FF        ;LAST DIGIT ?
6031  D0 EE     1272        BNE DDRF        ;IF NO, DIAL NEXT DIGIT
6033- 60        1280        RTS             ;ELSE, RETURN FROM SUBROUTINE


SYMBOL TABLE

DLO    6018     DDRF   6021
```

Figure 2. R2424 Automatic Dialer Routine

```
                        1000        ORG $300
                        1008 *
                        1016 ************************************************
                        1024 *   R48DP/R96DP EYE PATTERN GENERATION ROUTINE    *
                        1032 ************************************************
                        1040 *                                              *
                        1048 * THIS ROUTINE GENERATES A CONTINUOUS EYE PATTERN *
                        1056 * READING A SIGNAL POINT ONCE PER BAUD.          *
                        1064 * EXECUTION IS HALTED AND CONTROL IS RETURNED TO  *
                        1072 * THE CALLING PROGRAM WHEN A KEY IS PRESSED.     *
                        1080 *                                              *
                        1088 ************************************************
                        1096 *
0300- AD 10 C0          1104        LDA $C010       ;CLEAR KBRD.
0303- 8D 40 C4          1112        STA $C440       ;POR
0306- A9 A2             1120        LDA ##A2
0308- 8D 25 C4          1128        STA $C425       ;WRITE RAM ACCESS XB
030B- A9 22             1136        LDA ##$22
030D- 8D 24 C4          1144        STA $C424       ;WRITE RAM ACCESS YB
0310- AD 04 C4          1152        LDA $C404
0313- 09 80             1160        ORA ##80
0315- 8D 04 C4          1168        STA $C404       ;SET 13ACT ANALOG LOOPBACK
0318- AD 07 C4          1176        LDA $C407
031B- 09 80             1184        ORA ##80
031D- 8D 07 C4          1192        STA $C407       ;RTS ON
0320- AD 2E C4          1200 RBDA   LDA $C42E       ;READ RBDA
0323- 29 01             1208        AND ##$01
0325- F0 F9             1216        BEQ RBDA        ;WAIT UNTIL RBDA=1
0327- AD 23 C4          1224        LDA $C423       ;READ RAM DATA XBM
032A- 8D 50 C4          1232        STA $C450       ;WRITE TO X-DAC
032D- AD 21 C4          1240        LDA $C421       ;READ RAM DATA YBM
0330- 8D 60 C4          1248        STA $C460       ;WRITE TO Y-DAC
0333- AD 20 C4          1256        LDA $C420       ;READ REG. 2:0 TO CLEAR RBDA
0336- AD 00 C0          1264        LDA $C000       ;KEYBOARD ACTIVE ?
0339- 29 80             1272        AND ##80
033B- F0 E3             1280        BEQ RBDA        ;IF YES, CLEAR DACS AND RETURN
033D- A9 00             1288        LDA ##00
033F- 8D 50 C4          1296        STA $C450
0342- 8D 60 C4          1304        STA $C460
0345- 60                1312        RTS
```

Figure 3. Eye Pattern Generator Routine

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Rockwell

2400/1200/300 bps International Modem Design

by Malcolm B. Waters, Product Applications Engineer
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INTRODUCTION

This application note presents a design for a 2400/1200/300 bps international modem which meets CCITT recommendations V.21, V.22, V.22 bis and V.23. The design is based on the Rockwell R2424 2400/bps full duplex modem which provides the 2400 bps V.22 bis and 1200 bps V.22 modes, and the Am7910 FSK modem which provides 1200 bps half duplex V.23 and 300 bps full duplex V.21 modes. The modes supported are listed in Table 1.

The hardware design, along with software described in this application note, demonstrates a complete functional unit for asynchronous operation. The application note software supports five operating modes:

Originate 2400 bps in V.22 bis
Originate 1200 bps in V.22
Originate 1200 bps in V.23
Originate 300 bps in V.21
Universal Auto Answer

The modem design includes the complete interface to an IBM PC (or compatible) host computer. The application hardware was built on a full-size prototyping card which can be installed into any spare PC expansion slot. The Am7910 modem and other peripheral and TTL devices are installed on one third of the prototyping card. A Rockwell R2424M, a small (4 in. x 3.5 in.) self-contained modem module, is mounted over one third of the prototyping card. A Rockwell Data Access Arrangement (RDAA) module (3.94 in. x 3.94 in.) is mounted over the middle third of the prototyping card. Figure 1 shows the basic layout of the major hardware components.

The Rockwell R2424 modem is also available as a device set (R2424DS). By using modem devices and an integral DAA in a production design, this application note design can be incorporated onto a single full-size IBM PC printed circuit board.

HARDWARE DESIGN

The major components of the international modem are:

R2424M 2400/1200 Full Duplex Modem module
Am7910 1200/300 FSK Modem
Z8530 Serial Communications Controller (SCC)
82C55 Programmable Peripheral Interface (PPI)
Rockwell Data Access Arrangement (RDAA) module

A functional block diagram showing major data and control signal flow is shown in Figure 2. In addition to supplying the 2400 bps (V.22 bis) and 1200 (V.22) full duplex modes, the R2424 modem provides the primary control interface with the telephone line. The Am7910 modem supplies 1200 bps half duplex (V.23) and 300 bps full duplex (V.21) functions. The R2424 is controlled directly from the host computer data bus, whereas the Am7910 has control pins which are driven from the 82C55 PPI. Control signals select which modem is in operation and route the data along specific paths. A schematic detailing all signal routing and connections is shown in Figure 3.

Host Interface

The IBM PC address, data and control bus signals are buffered by devices U1-U4. The modem uses I/O address space 200H-23FH. Table 2 allocates the addresses used by the various devices in the application design. Decoder U5 generates four chip select signals ($\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$) from address lines A0-A9. The U13a output enables U5 when a valid address (200H-23FH) occurs.

The I/O Read ($\overline{IOR}$) and I/O Write ($\overline{IOW}$) lines are gated with a valid I/O address to generate read and write inputs to the R2424 modem, the Z8530 SCC (U6) and the 82C55 PPI (U7) as the chip select lines are not selected at a unique address range. An inverter (U14c) is included in the read line to make it active high for the R2424.

Table 1. International Modem Modes

Recommendation	Rate	Full Duplex/ Half Duplex	Originate/ Answer	Modulation Scheme	Modem
V.22 bis	2400 bps	Full Duplex	Originate	PSK	R2424
V.22 bis	2400 bps	Full Duplex	Answer	PSK	R2424
V.22	1200 bps	Full Duplex	Originate	PSK	R2424
V 22	1200 bps	Full Duplex	Answer	PSK	R2424
V.23	1200 bps	Half Duplex	Mode 2	FSK	Am7910
V.23	1200 bps	Half Duplex	Mode 2 with Equalizer	FSK	Am7910
V.21	300 bps	Full Duplex	Originate	FSK	Am7910
V.21	300 bps	Full Duplex	Answer	FSK	Am7910

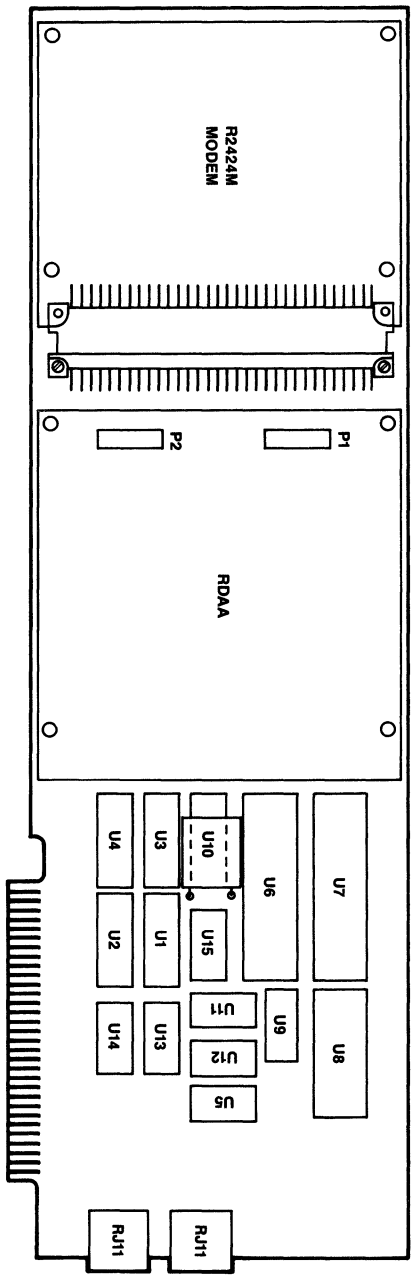

Figure 1. International Modem Prototype Layout

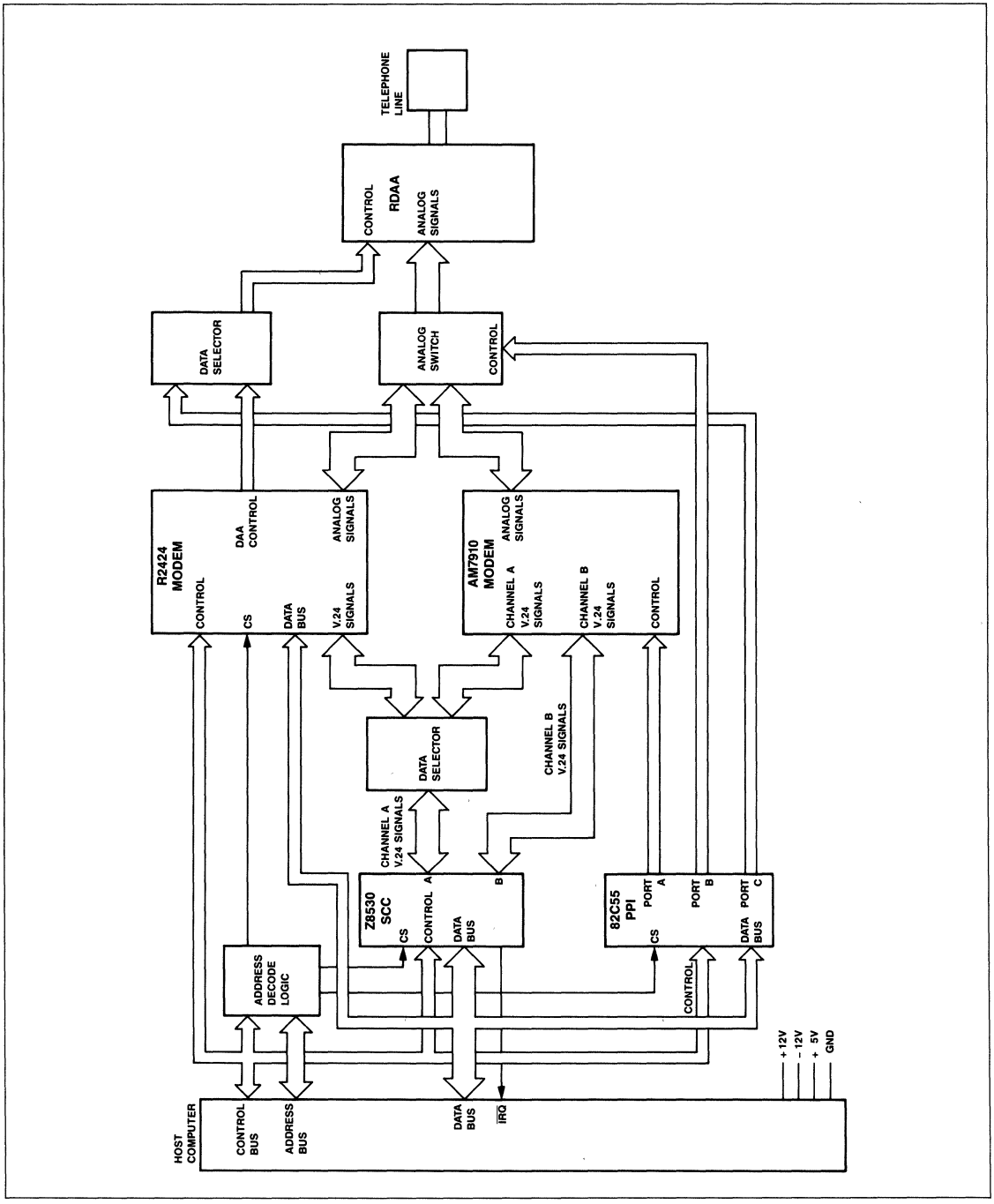

Figure 2. International Modem Hardware Block Diagram

Table 2. International Modem I/O Addresses

Address (Hex)	Register Description
200	R2424 Receiver Reserved
201	R2424 Receiver Reserved
202	R2424 Receiver Diagnostic 1
203	R2424 Receiver Diagnostic 2
204	R2424 Receiver Diagnostic 3
205	R2424 Receiver Diagnostic 4
206	R2424 Receiver Reserved
207	R2424 Receiver Reserved
208	R2424 Receiver Status 1
209	R2424 Receiver Status 2
20A	R2424 Receiver Configuration 1
20B	R2424 Receiver Configuration 2
20C	R2424 Receiver Configuration 3
20D	R2424 Receiver Configuration 4
20E	R2424 Receiver Handshake
20F	R2424 Receiver Diagnostic Control
210	R2424 Transmitter Dial Digit Register
211	R2424 Transmitter Reserved
212	R2424 Transmitter Diagnostic 1
213	R2424 Transmitter Diagnostic 2
214	R2424 Transmitter Diagnostic 3
215	R2424 Transmitter Diagnostic 4
216	R2424 Transmitter Reserved
217	R2424 Transmitter Reserved
218	R2424 Transmitter Status 1
219	R2424 Transmitter Configuration 1
21A	R2424 Transmitter Configuration 2
21B	R2424 Transmitter Configuration 3
21C	R2424 Transmitter Configuration 4
21D	R2424 Transmitter Configuration 5
21E	R2424 Transmitter Handshake
21F	R2424 Transmitter Diagnostic Control
220	Z8530 Channel B Command
221	Z8530 Channel B Data
222	Z8530 Channel A Command
223	Z8530 Channel A Data
224–	Not Used
22F	Not Used
230	82C55 Port A
231	82C55 Port B
232	82C55 Port C
233	82C55 Control Register
234–	Not Used
23F	Not Used

All data between the host computer and the modem is transferred over the bidirectional data bus (D0-D7). The data bus carries data to be transmitted to the modem (TXD) and to be received from the modem (RXD) via the Z8530 SCC, as well as control/status signals to/from the R2424 modem, the Z8530 SCC and the 82C55 PPI. U13b, U13c and U13d enable data bus buffer U3 when an I/O read or I/O write occurs in a valid address range. The direction of the data bus buffer is controlled by the host computer I/O read line ($\overline{IOR}$) gated with the valid I/O address signal appearing at U13d/11.

Z8530 SCC

The Z8530 SCC (U6) transfers the data from the modems to the data bus and converts the data from parallel to serial and serial to parallel between the host computer and the modem devices and provides asynchronous formatting and unformatting. The SCC has two I/O channels (A and B). Channel A is used for all full duplex modes; channel B is used in a V.23 half duplex mode where a secondary channel is used.

Outgoing data (TXD) written from the host computer is serialized and formatted by the Z8530 SCC (U6). It is then output on the TXDA or TXDB pin in serial form.

Incoming data (RXD) from the modem is input to the SCC on the RXDA or RXDB pin and is read via the data bus from the SCC data register. The data is then routed to the PC display (application note software), or it may be routed to a different destination (user-provided software).

The SCC A/$\overline{B}$ input selects channel A or B. The SCC $\overline{C}$/D input determines if control or data information is being accessed. The $\overline{WR}$ and $\overline{RD}$ inputs determine if data is being written to or read from the SCC, respectively. The $\overline{CE}$ input is low at address 220-223 to enable the SCC.

R2424 Modem

The R2424 is mapped into the PC I/O addresses 200H-21FH. The R2424 receiver is enabled by $\overline{CS0}$ (200H-20FH) and the transmitter is enabled by $\overline{CS1}$ (210H-21FH). This enables access to the 32 locations required by the receiver and transmitter interface memories. Host computer address lines A0-A3 are routed to R2424 register select inputs R0-R3, respectively, to access the required interface memory location.

For more information on the R2424 refer to the R2424 Data Sheet (Order No. MD11) and Section 4 (R1212/R2424 Modem Functional Characteristics) in the Modem Interface Guide (Order No. 685), both available from Rockwell International.

Am7910 Modem

Operation of the Am7910 modem is controlled by five configuration inputs (MC0-MC4). Table 3 lists the available modes and identifies the modes used in this application note. The Am7910 configuration signals are controlled by PPI (U7) ports PA0-PA4 since there is no direct host computer bus interface.

The V.24 control signals are routed from the Z8530 SCC (U6). The primary channel (used for all full duplex modes) is routed to the SCC channel A and the Am7910 secondary channel (used for the 1200 half duplex mode) is routed to the SCC channel B.

The clock for the Am7910 is provided by the SCC output TRxCA.

V.24 Interface

TTL V.24 signals are routed to/from the R2424/Am7910 modems as selected by U9 and U10. The $\overline{RLSD}$, $\overline{CTS}$ and RXD outputs from either the R2424 or the Am7910 are switched through U9 to Z8530 SCC (U6) channel A inputs $\overline{DCDA}$, $\overline{CTSA}$ and RXDA, respectively. PPI PA5 output high selects Am7910 signals; PPI PA5 output low selects R2424 signals.

The TXD input to both the R2424 and the Am7910 is routed directly from the SCC TXDA output. The $\overline{RTS}$ input to the R2424 and/or the Am7910 is routed from the SCC $\overline{RTSA}$ output through U10. The $\overline{RTS}$ input to the R2424 is enabled through U10 by PPI PA6 output low. The $\overline{RTS}$ input to the Am7910 is enabled through U10 by PPI PA7 output low.

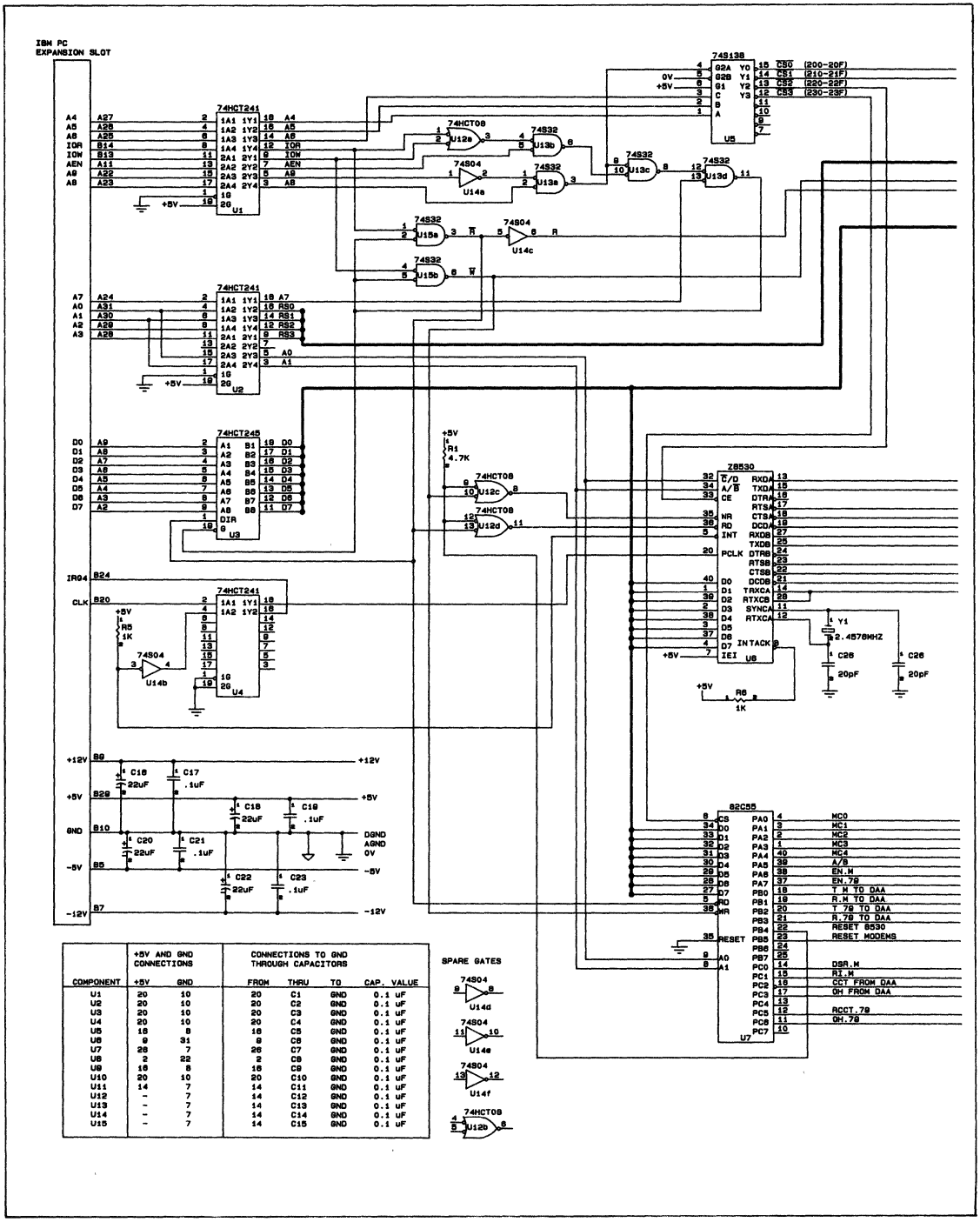

Figure 3. International Modem Schematic

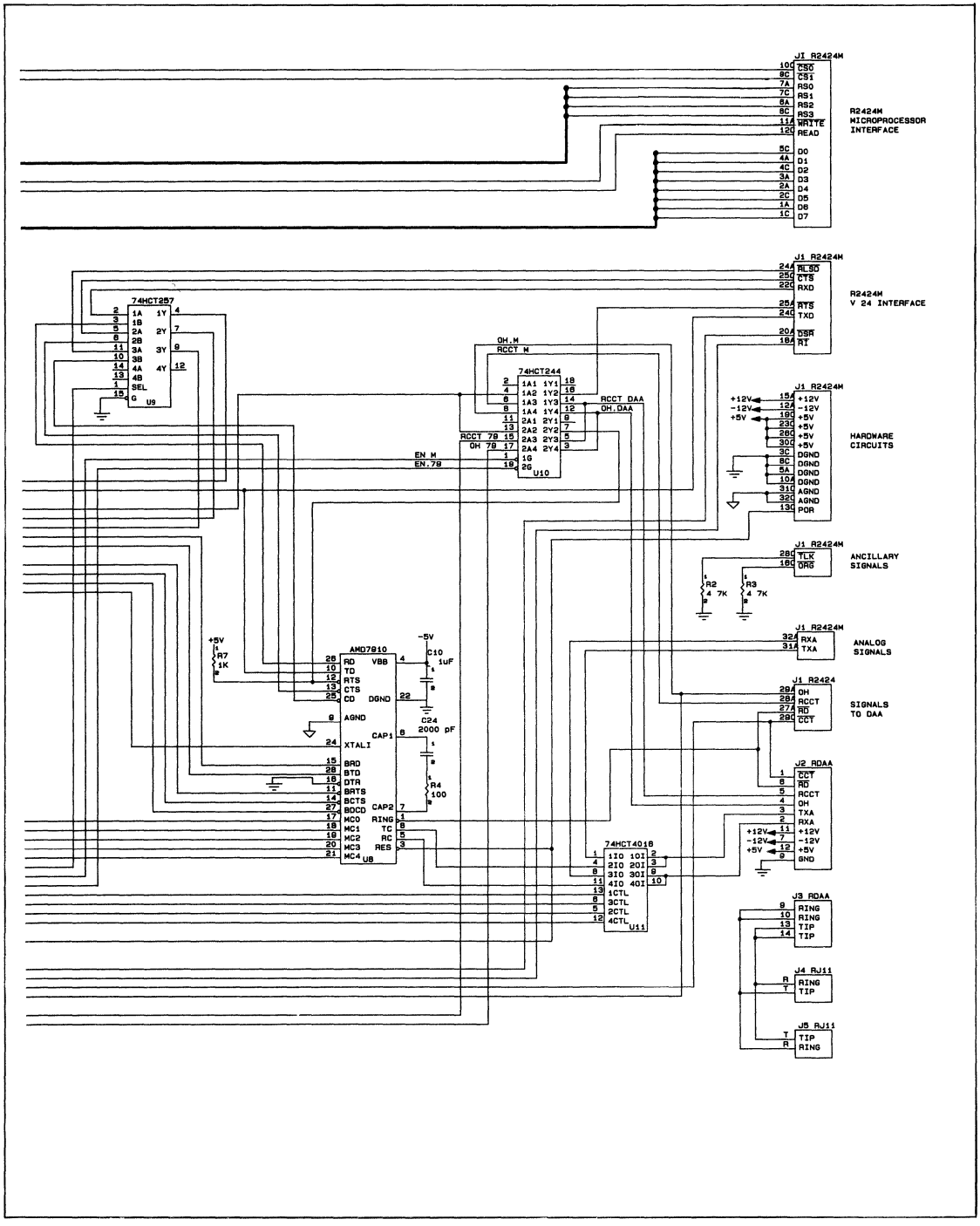

Figure 3. International Modem Schematic (Continued)

Table 3. Am7910 Mode Selection

MC4	MC3	MC2	MC1	MC0	Mode
0	0	0	0	0	Bell 103 Originate 300 bps Full Duplex
0	0	0	0	1	Bell 103 Answer 300 bps Full Duplex
0	0	0	1	0	Bell 202 1200 bps Half Duplex
0	0	0	1	1	Bell 202 with Equalizer 1200 bps Full Duplex
0	0	1	0	0	V.21 Originate 300 bps Full Duplex*
0	0	1	0	1	V.21 Answer 300 bps Full Duplex*
0	0	1	1	0	V.23 Mode 2 1200 bps Half Duplex*
0	0	1	1	1	V.23 Mode 2 with Equalizer 1200 bps Half Duplex
0	1	0	0	0	V.23 Mode 1 600 bps Half Duplex
1	0	0	0	0	Bell 103 Originate Loopback
1	0	0	0	1	Bell 103 Answer Loopback
1	0	0	1	0	Bell 202 Main Loopback
1	0	0	1	1	Bell 202 with Equalizer Loopback
1	0	1	0	0	V.21 Originate Loopback
1	0	1	0	1	V.21 Answer Loopback
1	0	1	1	0	V.23 Mode 2 Main Loopback
1	0	1	1	1	V.23 Mode 2 with Equalizer Loopback
1	1	0	0	0	V.23 Mode 1 Main Loopback
1	1	0	0	1	V.23 Back Loopback

* Modes implemented in application note software.

82C55 PPI

The 82C55 PPI handles control signals between the host computer and the Am7910 modem and various TTL switches, data selectors/multiplexers and buffers. The functions of the bits in the PPI registers are listed in Table 4.

Port A signals control the Am7910 configuration and the U10 switch. Port B output signals control U11 to select the routing of TXA and RXA between the RDAA and either the R2424 or the Am7910. Port B output signals also control the resetting of the modems and the PPI. Port C inputs monitor $\overline{RTS}$ and $\overline{CTS}$ from the R2424 and OH and $\overline{CCT}$ signals from the R2424. The Port C outputs issue OH and $\overline{CCT}$ to the RDAA via U10.

RDAA Interface

Routing selection of TXA to the RDAA and RXA from the RDAA is controlled by U11. TXA is routed from the R2424 (TXA) or the Am7910 (TC) and RXA is routed to the R2424 (RXA) or the Am7910 (RC). OH and RCCT originate from the R2424 (OH and RCCT) or from the 82C55 PPI (OH.79 on PC6 and RCCT.79 on PC7) as selected by U10. $\overline{RD}$ is routed from the RDAA to the R2424 ($\overline{RD}$) and Am7910 ($\overline{RING}$) in parallel. CCT is routed to the R2424 ($\overline{CCT}$) and to the PPI (CCT on PC2).

MODEM OPERATION

Originate Mode

Modem operation is divided into two parts: originate and answer. In the originate mode, the R2424 always does the dialing, regardless of the final configuration. If a V.22 or V.22 bis connection is desired, the default hardware setup (initialized by application software) permits the R2424 to stay on line after dialing and connect with the remote modem. If a V.21 or V.23 connection is desired, then the R2424 dials the call. After dialing, a set of control signals (OH and $\overline{CCT}$) is generated to keep the DAA connected to the phone line. Meanwhile, the R2424 is disconnected and the Am7910 is configured for the desired mode. When the remote modem answers the Am7910 has control of the line and is set up to be in originate mode. The connection places the modem in data mode in either V.21 or V.23.

Answer Mode

In the answer mode, the modem must be capable of answering an incoming call from a modem of unknown configuration. The R2424 always answers the call, regardless of the final configuration. Because the default setup condition exists, the R2424 sends out the CCITT answertone and waits for the response from the remote modem. The software determines the configuration of the remote modem within one second of Data Set Ready becoming active in the R2424. It does this by first examining the SPEED bits.

If the SPEED bits are set to 11 (binary), then the modem is connected in V.22 bis mode at 2400 bps. If the SPEED bits are set to 10, then the modem is connected in V.22 mode at 1200 bps. If the SPEED bits are set to 00 then the calling modem is a V.21 or V.23 type. The RLSD bit of the R2424 is then examined. If it is set to 1, then the calling modem is a V.23 modem, otherwise it is a V.21 modem. At this time the Am7910 is already in data mode, although not connected to the line. (The ringing signal supplied by the DAA is shared by the R2424 and the Am7910, so both go off hook in answer mode.) When the software determines that a V.21 or V.23 connection is in progress, it holds the line by generating a set of control signals for the DAA. The R2424 is switched out and the Am7910 is switched in to the line, already in data mode. The remote modem received 2100 Hz answertone from the R2424. Now the Am7910 completes the handshake and the modems enter the data mode.

OPERATING PROCEDURE

The procedure to operate the modem using the application note software is described in this section. It is assumed that the user has entered, edited and stored the FORTH screens listed in Figure 15. It also assumes that the FORTH command level has been invoked.

Table 4. 82C55 Port Functions

Port	Bit	Function	7910	R2424
Port A—8 Outputs (0-7)				
PA0	0	7910 Configuration Pin MC0	X	
PA1	1	7910 Configuration Pin MC1	X	
PA2	2	7910 Configuration Pin MC2	X	
PA3	3	7910 Configuration Pin MC3	X	
PA4	4	7910 Configuration Pin MC4	X	
PA5	5	RXD, $\overline{CTS}$, $\overline{DCD}$ Modem Select 1 = 7910 0 = 2424	X	X
PA6	6	$\overline{DTR}$, $\overline{RTS}$, RCCT, OH Disable to R2424 1 = Disable 0 = Enable	X	X
PA7	7	$\overline{DTR}$, $\overline{RTS}$, RCCT, OH Disable to 7910 1 = Disable 0 = Enable	X	X
Port B—8 Outputs (0-7)				
PB0	0	R2424 TXA to DAA 1 = Enable 0 = Disable	X	X
PB1	1	R2424 RXA to DAA 1 = Enable 0 = Disable	X	X
PB2	2	7910 TC to DAA 1 = Enable 0 = Disable	X	X
PB3	3	7910 RC to DAA 1 = Enable 0 = Disable	X	X
PB4	4	Reset Z8530 (Pulse) 1 = Normal 0 = Reset		
PB5	5	Reset Modems (Pulse) 1 = Normal 0 = Reset	X	X
PB6	6	Not Used		X
PB7	7	Not Used		X
Port C—4 Inputs (0-3), 4 Outputs (4-7)				
PC0	0	Read R2424 $\overline{DSR}$		X
PC1	1	Read R2424 $\overline{RI}$		X
PC2	2	Read Status of $\overline{CCT}$ from DAA		X
PC3	3	Read Status of OH from DAA		
PC4	4	Not Used		
PC5	5	Set RCCT on DAA for 7910 1 = Set 0 = Off	X	
PC6	6	Set OH on DAA for 7910 1 = Off-Hook 0 = On-Hook	X	
PC7	7	Not Used		

Type 70 LOAD and press RETURN.

When loading is complete, the software initializes and configures all devices for the default settings. A menu screen is then displayed on the terminal. This menu is function key driven and prompts the user for a choice of five keys to press for different options. Four originate modes are presented and one universal auto answer mode. The four originate modes allow the modem to connect at 300 bps in V.21 mode, 1200 bps in V.22, 2400 bps in V.22 bis and 1200 bps in V.23. The universal auto answer mode connects at the speed and configuration of the calling modem (initially unknown).

The displayed menu is:

INTERNATIONAL MODEM

F1 V.21 ORIGINATE
F2 V.22 ORIGINATE 1200
F3 V.22 ORIGINATE 2400
F4 V.23 ORIGINATE
F5 UNIVERSAL AUTO ANSWER

When the menu screen is displayed, the modem is in idle mode and the program is waiting for a function to be requested. To initiate a mode, press the corresponding function key.

Originate Mode

If an originate key is pressed, the user is prompted to enter the phone number to call. Upon number entry, the call is placed (always by the R2424). If a V.22 or V.22 bis configuration was selected then the R2424 stays connected to the line after placing the call. Otherwise, the Am7910 is switched in to complete the handshake with the remote modem. Once the modem is in data mode the program enters the dumb terminal routine.

After an originate mode is selected, the system will display one of the following messages depending on the selected mode:

V.21 300 BPS MODE
V.22 1200 BPS MODE
V.22 2400 BPS MODE
V.23 1200 BPS MODE*

followed by

ENTER PHONE NUMBER

Enter the telephone number to call and press ENTER.

Upon carrier detection and line connection the system will display:

CARRIER DETECTED . . . ON LINE
TERMINAL ON LINE

To terminate the mode anytime during the operation, press CTRL BREAK. After connection is established, pressing ' (single quote) will also terminate the mode. After terminating the mode, press RETURN to return to FORTH command entry level. Now type MENU and press RETURN to disconnect the modem from the line and to display the mode menu.

*V23 call origination results in a half duplex data mode connection. This application note software configures the originate modem for transmitting by asserting $\overline{RTS}$. In order to receive data, $\overline{RTS}$ must be made inactive.

Auto Answer Mode

In the universal auto answer mode, the program waits for the phone to ring. It then answers the call with the R2424 which sends out a 2100 Hz answertone. The R2424 decides the speed and configuration of the calling modem from the response from the calling modem. Depending on the response, the line is left connected to the R2424 or switched to the Am7910. When the handshake is complete, the program enters the dumb terminal routine.

When the universal auto answer mode is selected, the system will display:

```
UNIVERSAL AUTO ANSWER MODE
WAITING TO BE CALLED
```

Place the call from the remote modem. Upon ring detection and Data Set Ready assertion, the system will display:

```
RING DETECTED
DATA SET READY ON
```

followed by one of the following messages when the corresponding connection is made:

```
CONNECTED TO V.21 MODEM AT 300 BPS
CONNECTED TO V.22 MODEM AT 1200 BPS
CONNECTED TO V.22 MODEM AT 2400 BPS
CONNECTED TO V.23 MODEM AT 1200 BPS*
```

then

```
TERMINAL ON LINE . . .
```

To terminate the mode anytime during the operation, press CTRL BREAK. After connection is established, pressing ' (single quote) will also terminate the mode. After terminating the mode, press RETURN to return to FORTH command entry level. Now type MENU and press RETURN to disconnect the modem from the line (if not terminated by the remote modem) and to display the mode menu.

*Answering a call from a V.23 modem results in a half duplex data mode connection. This application note software configures the modem for receiving by keeping $\overline{RTS}$ inactive. In order to transmit data after the remote modem has finished transmitting, $\overline{RTS}$ must be made active.

Dumb Terminal

The dumb terminal routine is used once the modem has completed a connection. Data entered on the PC keyboard is sent to the modem to be transmitted to the remote modem. Incoming data is displayed on the terminal. In order to capture all received data at 2400 bps, it is necessary to interrupt the PC so that the data can be stored in a buffer. (This is because the scrolling actions of the screen take too much time and data would be lost if a polling method were used.) The dumb terminal routine interacts with the USART function in the Z8530 SCC device (U6) on the modem board. There are two main actions running continuously. Keyboard data, if available, is written to the data port of channel A of the Z8530. Then it is sent to the modem via the TXD line. The received data buffer in memory is checked to see if there are any characters waiting in the queue to be displayed. If there are, it displays them.

When the modem receives a character, it is passed to the RXD line of the Z8530. This causes an interrupt to be generated.

The interrupt handling routine services the interrupt by transferring the received data byte from the data port to the next location in the buffer in memory. Housekeeping is done on the buffer pointers and the loop then repeats itself.

SOFTWARE

Structure

The overall operation of the software is flowcharted in Figure 4. Figures 5 through 8 show subsections of the main routines, such as basic default settings for the devices. The command flow to control the modem in each of its configurations is shown in Figures 9 through 13.

If an originate connection is selected from the menu, then the flowcharts of Figure 11 and Figure 12 show the actions which are performed to set up the modem, make the call and enter the data state. The algorithm for the universal auto answer mode is given in Figure 13. This allows the modem to connect with an unknown calling modem which may be one of four different standards; V.21, V.22, V.22 bis or V.23. The modem automatically reconfigures itself and connects to the remote modem.

Programming

The application note software is programmed in FORTH. The FORTH screens are listed in Figure 15. Any FORTH system implementing the FORTH '83 standard for execution on the IBM PC should be compatible. The compiled screens presented here add the extra customized FORTH primitives to the Kernel dictionary. Operation of the modem is governed by routines using these words to control the hardware circuits from software. The software can be user-customized for a particular application. Alternatively, the listing is complete as supplied. There is an interrupt driven dumb terminal program included, which is capable of handling 2400 bps full duplex communications.

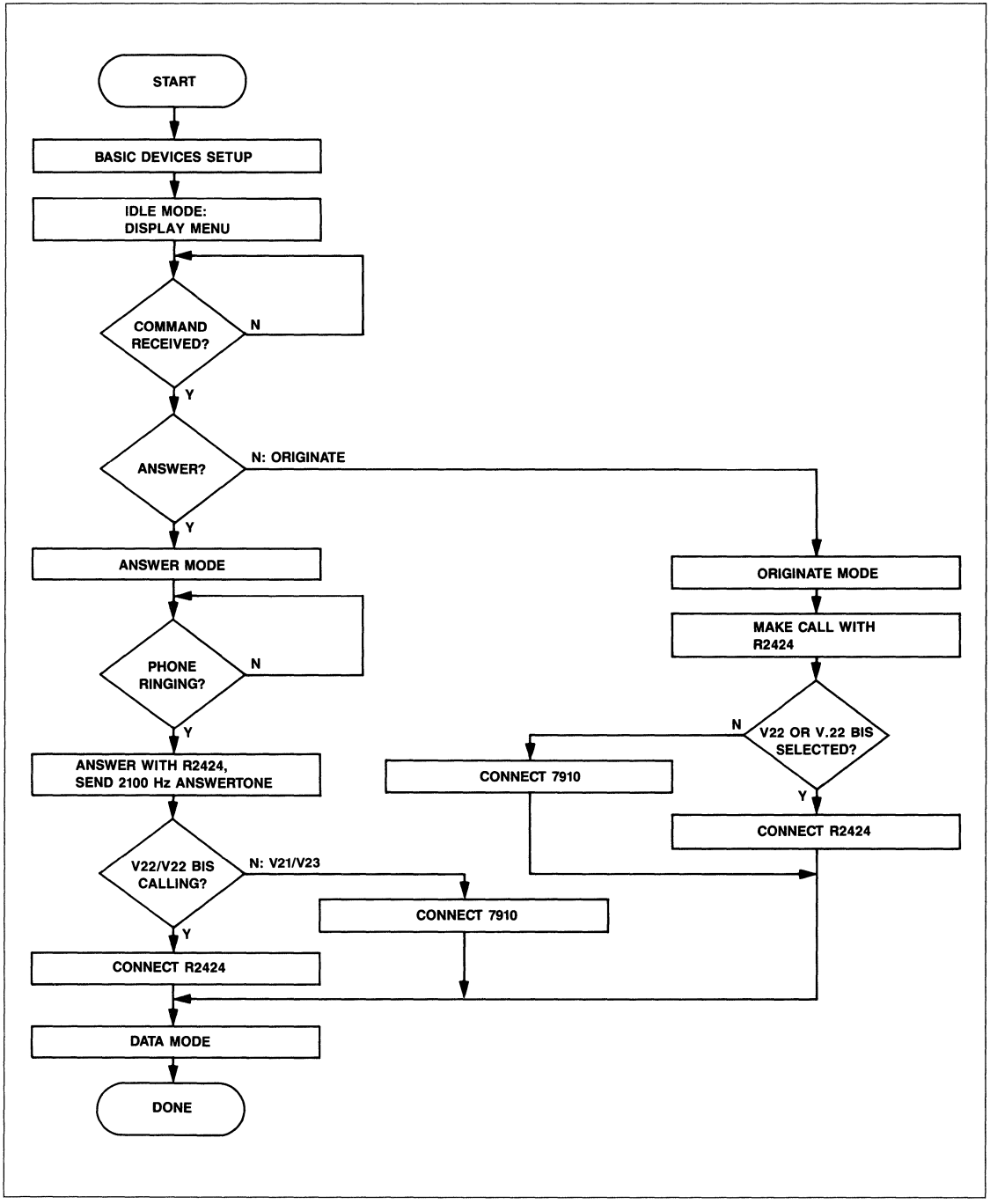

Figure 4. Flowchart — International Modem Software Overview

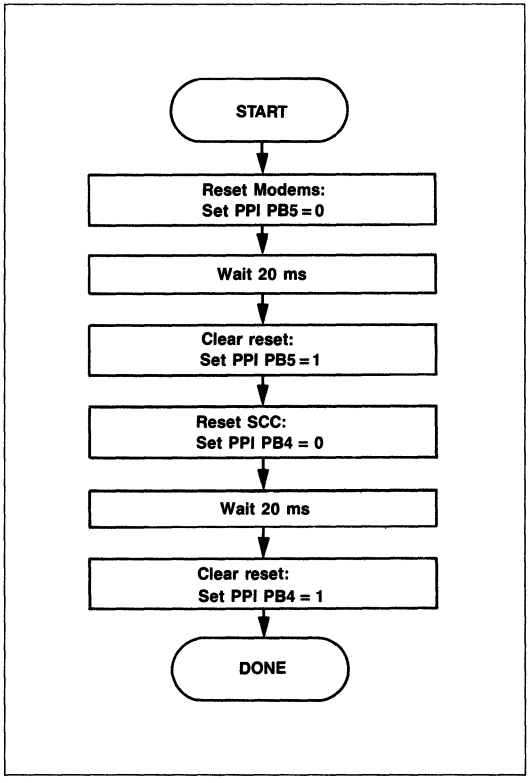

Figure 5. Flowchart — Reset Devices

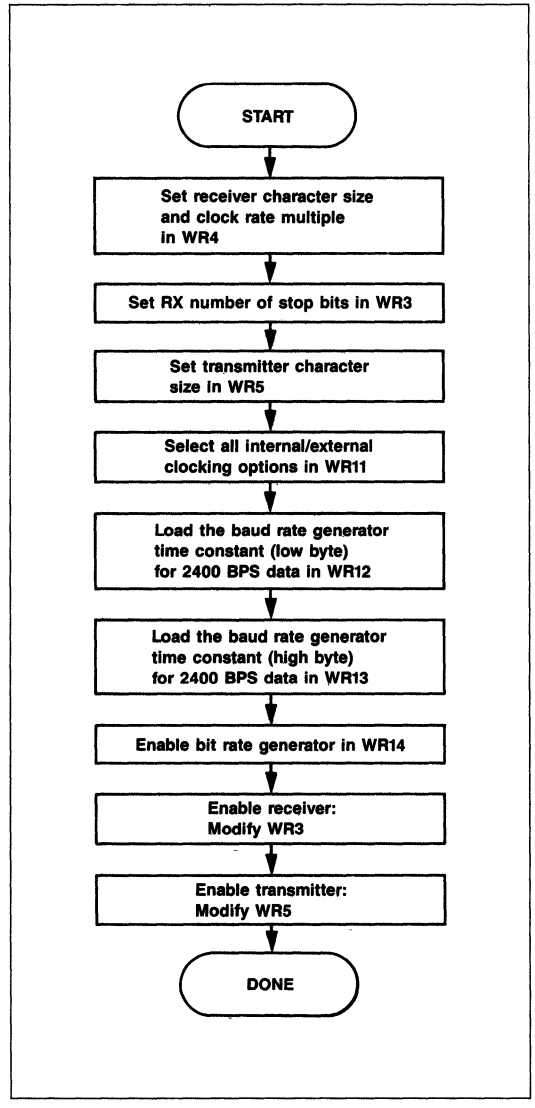

Figure 6. Flowchart — Basic Devices Setup: 8530

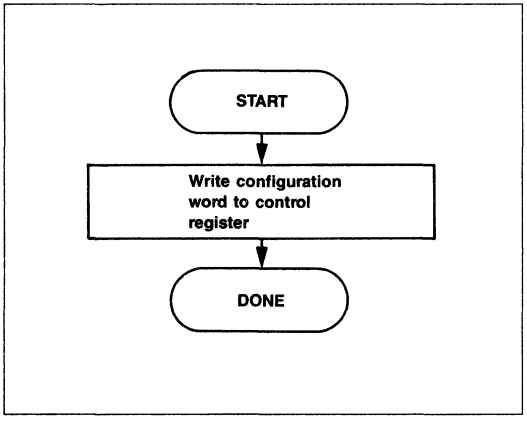

Figure 7. Flowchart — Basic Devices Setup: 82C55

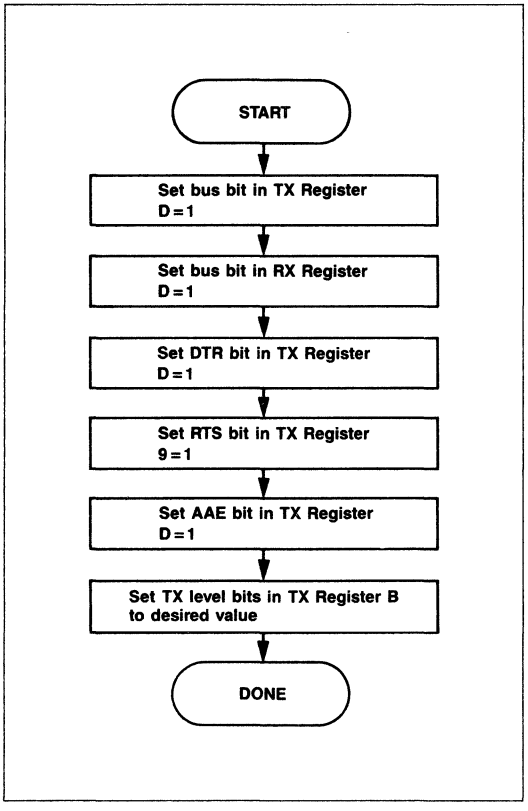

Figure 8. Flowchart — Basic Devices Setup: R2424

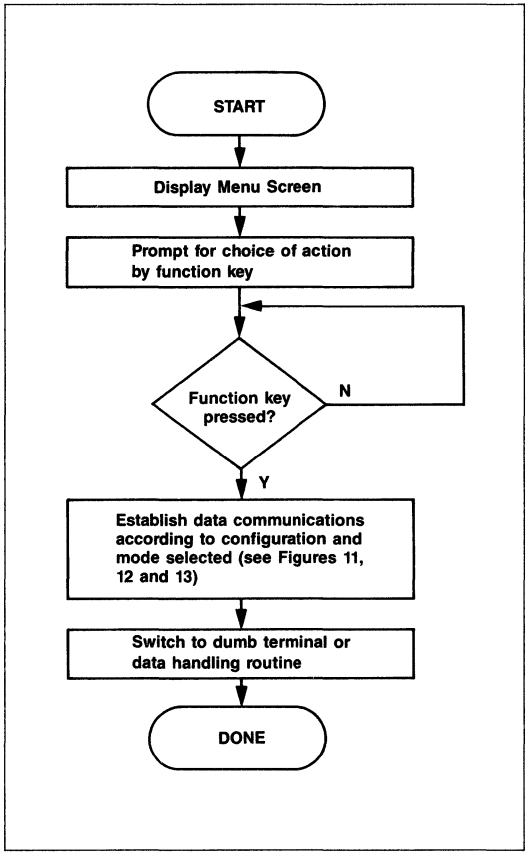

Figure 9. Flowchart — Main Operation

5

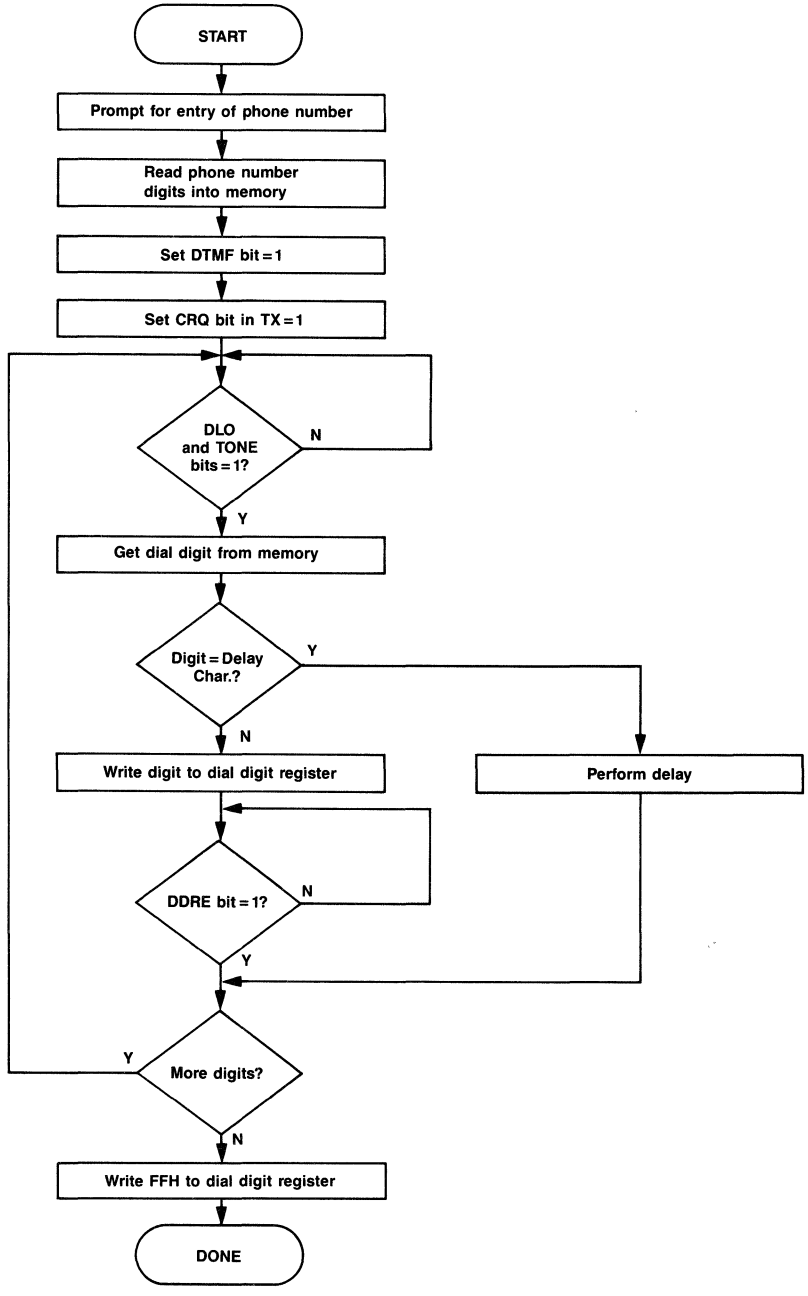

Figure 10. Flowchart — Auto Dial

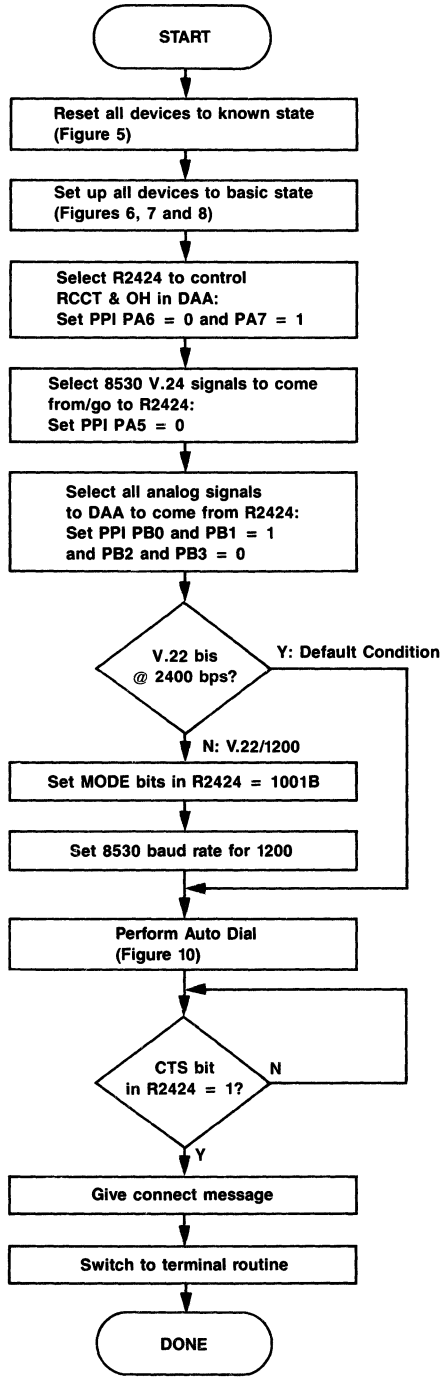

Figure 11. Flowchart — V.22 or V.22 bis Call Origination

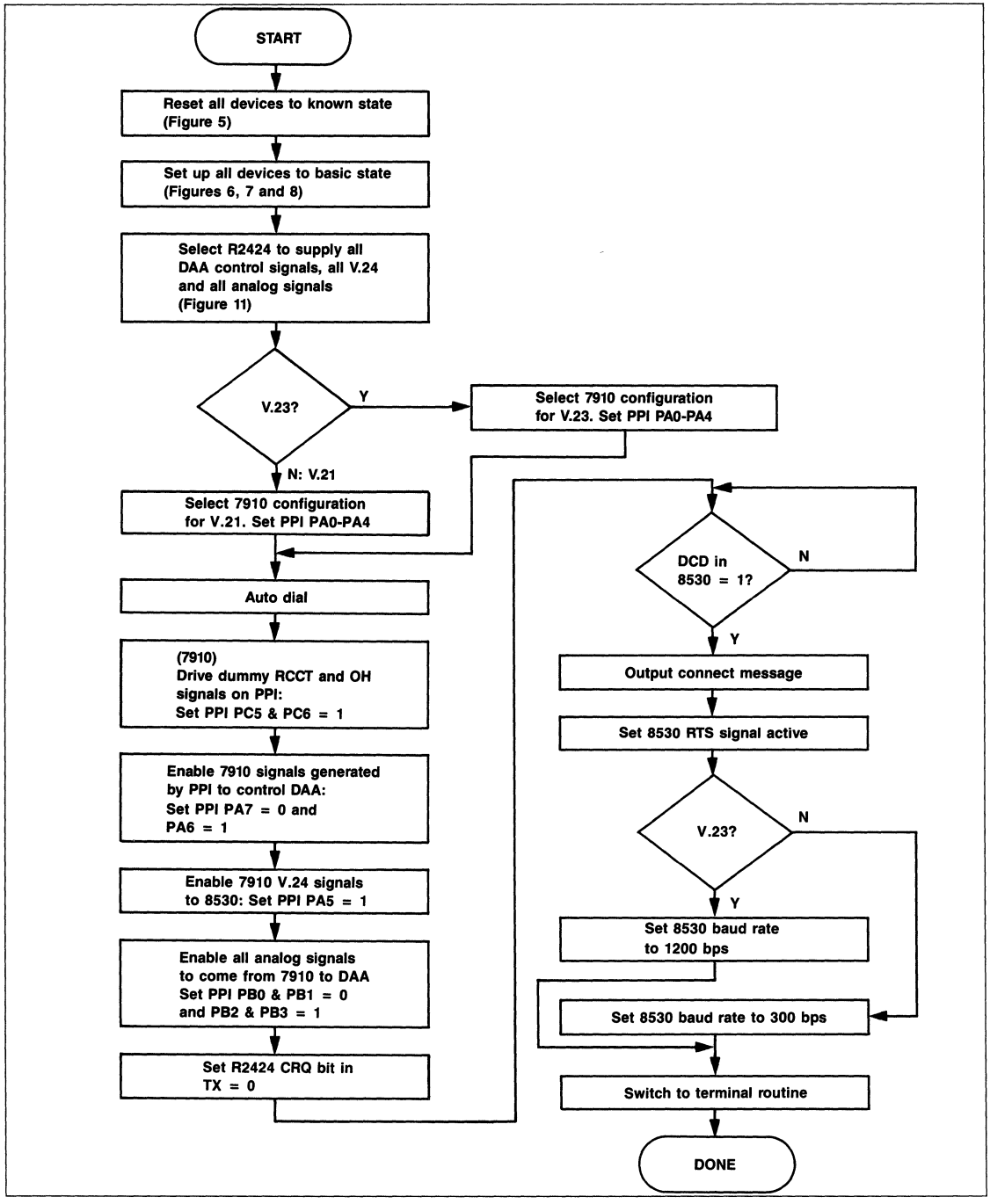

Figure 12. Flowchart — V.21 or V.23 Call Origination

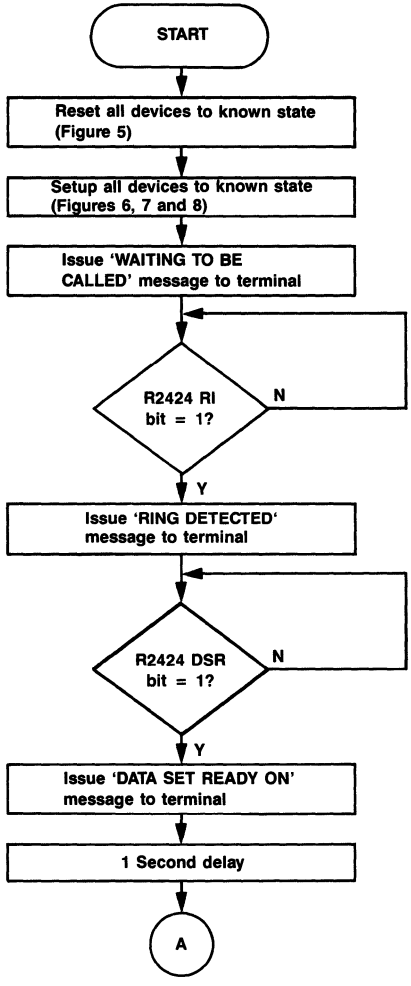

Figure 13. Flowchart — Universal Auto Answer Mode

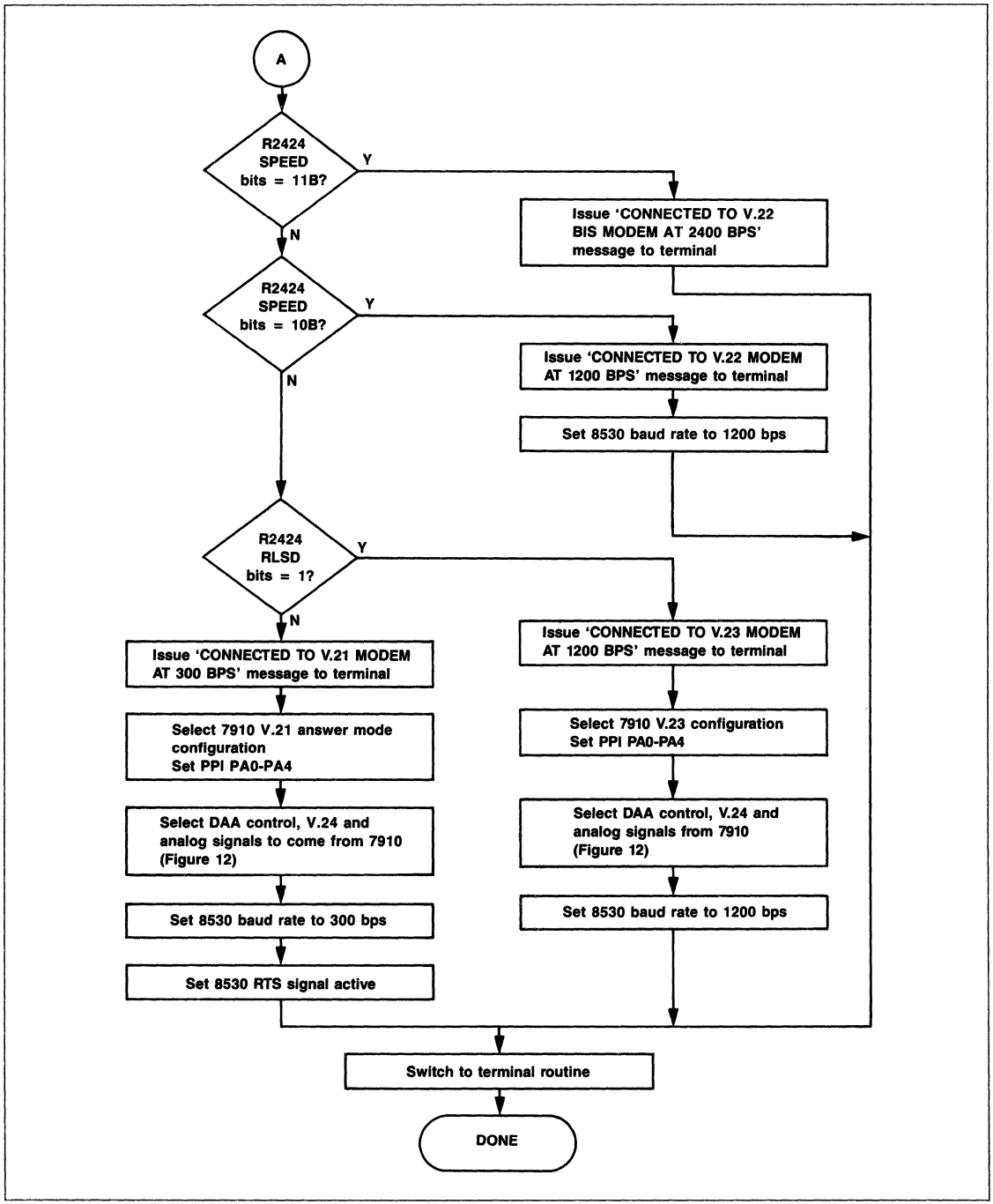

Figure 13. Flowchart — Universal Auto Answer Mode (Continued)

```
Screen # 69
  0
  1
  2
  3
  4
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15


Screen # 70
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 FORTH DEFINITIONS HEX
  2
  3  -1 CONSTANT COM1?
  4   0 CONSTANT COM2?
  5
  6 COM1? .IF
  7   0223 CONSTANT ASC_PORT
  8   0010 CONSTANT INT_MASK        ( IRQ4 )
  9   000C CONSTANT INT_#
 10 .THEN  COM2? .IF
 11   0223 CONSTANT ASC_BASE
 12   0008 CONSTANT INT_MASK        ( IRQ3 )
 13   000B CONSTANT INT_#
 14 .THEN
 15 -->


Screen # 71
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 DECIMAL
  2
  3 2VARIABLE LINKS
  4 VARIABLE X VARIABLE V
  5
  6 : FIX-VOC-LINKS
  7         VOC-LINK DUP  X !   @ V !
  8         BEGIN   V @
  9         WHILE   V @ HERE U<
 10                 IF    V @ X @ !  V @ X !  X @ @ V !
 11                 ELSE  V @ @ V !  THEN
 12         REPEAT ;
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens

```
Screen # 72
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 : BEGIN-MOD    1 ?DEPTH HERE LINKS !
  2         LATEST NAME> LINKS 4+ !
  3         LIMIT 500 - SWAP - DP ! ;
  4
  5 : END-MOD  LINKS @ DP ! ;
  6
  7 : FORGET-MOD    LINKS 4+ @
  8         SHR4
  9         LINKS @ 32 0 SKIP DROP
 10         N>LINK W!  FIX-VOC-LINKS ;
 11
 12
 13
 14
 15 -->
Screen # 73
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 DECIMAL  17000 BEGIN-MOD  ASM86  END-MOD
  3
  4 HEX
  5
  6 2000 CONSTANT ASC_BUF_SIZE
  7
  8 CREATE  ASC_BUF  ASC_BUF_SIZE ALLOT
  9         ASC_BUF  ASC_BUF_SIZE ERASE
 10
 11 VARIABLE ASC_IN
 12 VARIABLE ASC_OUT
 13
 14
 15 -->
Screen # 74
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 0 INT_# 4 * 2CONSTANT INT-VEC
  3
  4 2VARIABLE PREV_ASC_VEC
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 75
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 : INCR_PTR       ROT
  3                  2 PICK @ +
  4                  2DUP <=
  5                  IF   SWAP -
  6                  ELSE SWAP DROP
  7                  THEN SWAP ! ;
  8
  9 : +ASC_IN        ASC_IN  ASC_BUF_SIZE INCR_PTR ;
 10 : +ASC_OUT       ASC_OUT ASC_BUF_SIZE INCR_PTR ;
 11
 12
 13
 14
 15 -->
Screen # 76
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 : ?ASC           ASC_IN @  ASC_OUT @  <> ;
  3
  4 : @ASC           BEGIN ?ASC
  5                  UNTIL ASC_OUT @ ASC_BUF + C@  1 +ASC_OUT ;
  6
  7 : #ASC           ASC_OUT @ ASC_IN @ 2DUP U>
  8                  IF    ASC_BUF_SIZE +   THEN  - NEGATE ;
  9
 10
 11
 12
 13
 14
 15 -->
Screen # 77
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2 CREATE ASC_INT   ASSEMBLER
  3                  STI
  4                  AX PUSH  BX PUSH
  5                  DX PUSH  DS PUSH
  6                  AX, CS MOV  DS, AX MOV
  7                  DX, # ASC_PORT MOV
  8                  AL, DX IN
  9                  CLI
 10                  BX, ASC_IN 2+ MOV
 11                  ASC_BUF [BX], AL MOV
 12
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 78
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2                  BX INC
  3                  BX, # ASC_BUF_SIZE CMP
  4                  1$ JNZ
  5                  BX, BX XOR
  6          1$:     ASC_IN 2+ , BX MOV
  7                  STI
  8                  AL, # 20 MOV
  9                  # 20 , AL OUT
 10                  DS POP  DX POP
 11                  BX POP  AX POP
 12                  IRET
 13 FORTH
 14
 15 -->
Screen # 79
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2 : ASC-TRAP       PREV_ASC_VEC 2@ OR 0=
  3                  IF   INT-VEC @L
  4                       INT-VEC 2+ @L
  5                       PREV_ASC_VEC 2!
  6                  THEN
  7                  ?CS:  INT-VEC 2+ !L
  8                  ASC_INT INT-VEC !L  ;
  9
 10
 11
 12
 13
 14
 15 -->
Screen # 80
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 : ASC-RELEASE    PREV_ASC_VEC 2@
  3                  INT-VEC 2+ !L
  4                  INT-VEC !L ;
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 81
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2 : ASC-ENB
  3                  21 PC@
  4                  INT_MASK NOT  AND
  5                  21 PC!
  6
  7                  ASC_IN OFF ASC_OUT OFF
  8                  ASC_BUF ASC_BUF_SIZE ERASE ;
  9
 10
 11
 12
 13
 14
 15 -->
Screen # 82
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2
  3 : ASC-DSB        21 PC@
  4                  INT_MASK OR
  5                  21 PC! ;
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->
Screen # 83
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 : ASC-ON         ASC-TRAP   ASC-ENB ;
  3
  4 : ASC-OFF        ASC-DSB  ASC-RELEASE ;
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->
```

5

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 84
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1 HEX
  2
  3 : ASC_TX_WAIT   BEGIN  ASC_PORT 1 -  PC@  40 AND
  4                 UNTIL ;
  5
  6 : !ASC          ASC_TX_WAIT   ASC_PORT PC! ;
  7
  8
  9
 10
 11
 12
 13
 14
 15 -->

Screen # 85
  0 ( V21/V23 MODEM  INTERRUPT HANDLER                    27/1/86 MBW )
  1
  2 HEX HERE 0FFF0 U>
  3
  4 .IF     CR
  5         CR
  6         CR
  7         CR
  8
  9         FORGET COM1?  ." ERROR....MUST BE LOADED BELOW FFF0 "
 10
 11 .THEN   DECIMAL  FORGET-MOD
 12 -->
 13
 14
 15

Screen # 86
  0 ( V21/V23 MODEM  DUMB TERMINAL                        27/1/86 MBW )
  1 FORTH DEFINITIONS DECIMAL
  2 HEX
  3 ( --- )
  4 : TALK       CR ." TERMINAL ON LINE . . . ." CR CR ASC-ON
  5         BEGIN   ?ASC
  6                 IF    @ASC  7F AND EMIT
  7                 THEN
  8                 ?TERMINAL
  9                 IF    KEY  DUP 27 =
 10                       IF   DROP CLS QUIT
 11                       ELSE !ASC
 12                       THEN
 13                THEN
 14         AGAIN ;
 15 DECIMAL -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 87
  0 ( V21/V23 MODEM   TIMERS                                  27/1/86 MBW )
  1 DECIMAL
  2 : ALL ;
  3 : MS
  4   0 DO 22 0 DO LOOP LOOP ;
  5 : SEC
  6   1000 * MS ;
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->
Screen # 88
  0 ( V21/V23 MODEM   INITIALISATION                          27/1/86 MBW )
  1 HEX
  2 : INIT.8255   81 233 PC! ; ( 2 1/2 OUTPUT PORTS 1/2 INPUT )
  3 : RESET.MODEMS   231 PC@ DUP DF AND ( SET PB5 TO 0 )
  4                  231 PC!
  5                  20 MS
  6                  20 OR 231 PC!       ( SET PB5 TO 1 )
  7                  50 MS ;
  8 : RESET.8530   231 PC@ DUP EF AND ( SET PB4 TO 0 )
  9                231 PC!
 10                20 MS
 11                10 OR 231 PC!
 12                20 MS ;
 13 : INIT   INIT.8255 RESET.MODEMS RESET.8530 ; ( EVERYTHING )
 14 DECIMAL
 15 -->
Screen # 89
  0 ( V21/V23 MODEM   ENABLES/DISABLES                        27/1/86 MBW )
  1 HEX
  2 : EN.RCCT/OH.M   230 PC@ BF AND              ( MAKE PA6=0 )
  3                      80 OR  230 PC!          ( MAKE PA7=1 ) ;
  4 : EN.RCCT/OH.79  230 PC@ 7F AND              ( MAKE PA7=0 )
  5                      40 OR  230 PC!          ( MAKE PA6=1 ) ;
  6 : EN.V24.79      230 PC@ 20 OR  230 PC!      ( MAKE PA5=1 ) ;
  7 : EN.V24.M       230 PC@ DF AND 230 PC!      ( MAKE PA5=0 ) ;
  8 : EN.ANALOG.M    231 PC@ 03 OR               ( PB0/ PB1=1 )
  9                  F3 AND 231 PC!              ( PB2/ PB3=0 ) ;
 10 : EN.ANALOG.79   231 PC@ 0C OR               ( PB0/ PB1=0 )
 11                  FC AND 231 PC!              ( PB2/ PB3=1 ) ;
 12 : ENABLE.INT.8530   1 222 PC! 10 222 PC!     ( SET INT ON RX )
 13                     9 222 PC! 0A 222 PC! ;   ( MIE          )
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 90
  0 ( V21/V23 MODEM   ENABLES/DISABLES                    27/1/86 MBW )
  1 HEX
  2 : EN.M    EN.RCCT/OH.M  EN.V24.M  EN.ANALOG.M
  3           ( ENABLE ALL R2424 SIGNALS ) ;
  4
  5 : EN.79   EN.RCCT/OH.79 EN.V24.79 EN.ANALOG.79
  6           ( ENABLE ALL 7910 SIGNALS ) ;
  7
  8
  9
 10 : NEWC.R    20E PC@ 08 OR 20E PC!
 11             BEGIN 20E PC@ 8 = NOT UNTIL ;
 12 : NEWC.T    21E PC@ 08 OR 21E PC!
 13             BEGIN 21E PC@ 8 = NOT UNTIL ;
 14 DECIMAL
 15 -->

Screen # 91
  0 ( V21/V23 MODEM   R2424 BIT SETTING  1 OF 2           27/1/86 MBW )
  1 HEX
  2 : NOW    ( FLAG REGISTER MASK -- )
  3   SWAP DUP 2SWAP SWAP ROT ROT
  4         ROT 0 = IF
  5                       FF SWAP - SWAP DUP PC@
  6                       ROT AND SWAP PC!
  7                 ELSE
  8                       SWAP DUP PC@ ROT
  9                       OR SWAP PC!
 10                 THEN
 11
 12
 13
 14
 15 -->

Screen # 92
  0 ( V21/V23 MODEM   R2424 BIT SETTING  2 OF 2           27/1/86 MBW )
  1   DUP 20A >= IF
  2             DUP 20D <= IF
  3                         NEWC.R ELSE
  4                                 DUP 219 >= IF
  5                                           DUP 21D <= IF
  6                                                       NEWC.T
  7                                                     THEN
  8                                           THEN
  9                       THEN
 10             THEN  DROP  ;
 11
 12
 13
 14
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 93
  0 ( V21/V23 MODEM   R2424 BIT CHECKING                    27/1/86 MBW )
  1 HEX
  2 : IS    ( REGISTER MASK -- BIT VALUE )
  3
  4   SWAP PC@ AND IF 1 ELSE 0 THEN ;
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->
Screen # 94
  0 ( V21/V23 MODEM   R2424 RECEIVER BIT MASKS               27/1/86 MBW )
  1 HEX
  2 : BUS.R     20D  80 ;
  3 : CRQ.R     20D  40 ;
  4 : LCD       20D  04 ;
  5 : AL.R      20B  01 ;
  6 : ERDL.R    20A  80 ;
  7 : RDL.R     20A  40 ;
  8 : DL.R      20A  20 ;
  9 : ST.R      20A  20 ;
 10 : TONE      208  80 ;
 11 : ATD       208  40 ;
 12 : TM        208  02 ;
 13 : RLSD      208  01 ;
 14 DECIMAL
 15 -->
Screen # 95
  0 ( V21/V23 MODEM   R2424 TRANSMITTER BIT MASKS            27/1/86 MBW )
  1 HEX
  2 : DDRE      21E  01 ;
  3 : BUS.T     21D  80 ;
  4 : CRQ.T     21D  40 ;
  5 : DATA      21D  20 ;
  6 : AAE       21D  10 ;
  7 : DTR       21D  08 ;
  8 : DSRA      21C  80 ;
  9 : GTE       21B  10 ;
 10 : GTS       21B  08 ;
 11 : 3DB       21B  04 ;
 12 : DTMF      21B  02 ;
 13 : AL.T      21B  01 ;
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 96
  0 ( V21/V23 MODEM   R2424 TRANSMITTER BIT MASKS      27/1/86 MBW )
  1 HEX
  2 : ERDL.T    21A  80 ;
  3 : RDL.T     21A  40 ;
  4 : DL.T      21A  20 ;
  5 : ST.T      21A  10 ;
  6 : RTRN      219  40 ;
  7 : ORG       219  20 ;
  8 : LL        219  10 ;
  9 : RTS       219  08 ;
 10 : CC        219  04 ;
 11 : EF        219  02 ;
 12 : DLO       218  80 ;
 13 : CTS       218  40 ;
 14 DECIMAL
 15 -->

Screen # 97
  0 ( V21/V23 MODEM   R2424 TRANSMITTER BIT MASKS      27/1/86 MBW )
  1 HEX
  2 : DSR       218  20 ;
  3 : RI        218  10 ;
  4
  5
  6
  7
  8
  9
 10
 11
 12
 13 DECIMAL
 14 -->
 15

Screen # 98
  0 ( V21/V23 MODEM   R2424 MULTIPLE BITS              27/1/86 MBW )
  1 HEX
  2 : V.22/1200    20A PC@ F9 AND 09 OR 20A PC! ( SET RX MODE BITS )
  3                NEWC.R
  4                21A PC@ F9 AND 09 OR 21A PC! ( SET TX MODE BITS )
  5                NEWC.T ;
  6 : V.22/2400    20A PC@ FD AND 0D OR 20A PC!
  7                NEWC.R
  8                21A PC@ FD AND 0D OR 21A PC!
  9                NEWC.T ;
 10 : SPEED?       209 PC@ 10 / DUP 4 / 4 * - ; ( -- VALUE OF BITS )
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 99
  0 ( V21/V23 MODEM   R2424 TRANSMIT LEVEL                27/1/86 MBW )
  1 HEX
  2 : 0DB     21B PC@ 0F AND 00 OR 21B PC! NEWC.T ;
  3 : -2DB    21B PC@ 3F AND 20 OR 21B PC! NEWC.T ;
  4 : -4DB    21B PC@ 5F AND 40 OR 21B PC! NEWC.T ;
  5 : -6DB    21B PC@ 7F AND 60 OR 21B PC! NEWC.T ;
  6 : -8DB    21B PC@ 9F AND 80 OR 21B PC! NEWC.T ;
  7 : -10DB   21B PC@ BF AND A0 OR 21B PC! NEWC.T ;
  8 : -12DB   21B PC@ DF AND C0 OR 21B PC! NEWC.T ;
  9 : -14DB   21B PC@ FF AND E0 OR 21B PC! NEWC.T ;
 10
 11
 12
 13
 14 DECIMAL
 15 -->
Screen # 100
  0 ( V21/V23 MODEM  8530 SETUP                            27/1/86 MBW )
  1 ( THIS DEFAULT SETTING CONFIGURES THE 8530 FOR 8 BIT DATA,      )
  2 ( 1 STOPBIT,  ENABLES THE TRANSMITTER & RECEIVER, SETS DTR, RTS)
  3 ( SETS THE CLOCKS, XTAL I/P,AND THE BIT RATE GENERATOR FOR 2400)
  4 HEX
  5 : DEFAULT.8530      ENABLE.INT.8530
  6   4 222 PC! 44 222 PC! ( SET RX 8 BITS X16 CLOCK )
  7   3 222 PC! C0 222 PC! ( 1 STOPBIT               )
  8   5 222 PC! 60 222 PC! ( SET TX 8 BITS           )
  9   B 222 PC! D4 222 PC! ( CLOCK OPTIONS           )
 10   C 222 PC! 1E 222 PC! ( BAUD RATE GEN LOW FOR 2400 )
 11   D 222 PC! 00 222 PC! ( BAUD RATE GEN HI FOR ALL   )
 12   E 222 PC! 01 222 PC! ( ENABLE BIT RATE GEN     )
 13   3 222 PC! C1 222 PC! ( ENABLE RX               )
 14   5 222 PC! 68 222 PC! ( ENABLE TX               ) ;
 15 DECIMAL -->
Screen # 101
  0 ( V21/V23 MODEM  CHANGE 8530 PARAMETERS                27/1/86 MBW )
  1 HEX
  2 : RX.ENABLE          3 222 PC!  C1 222 PC! ;
  3 : RX.DISABLE         3 222 PC!  C0 222 PC! ;
  4 : RTS.8530.ON        5 222 PC!  EA 222 PC! ;
  5 : RTS.8530.OFF       5 222 PC!  E8 222 PC! ;
  6 : 300BPS.8530        C 222 PC!  FE 222 PC! ;
  7 : 1200BPS.8530       C 222 PC!  3E 222 PC! ;
  8 : 2400BPS.8530       C 222 PC!  1E 222 PC! ;
  9 : DTR/RTS.8530.OFF   5 222 PC!  68 222 PC! ;
 10 : DTR.8530.ON        5 222 PC!  E8 222 PC! ;
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 102
  0 ( V21/V23 MODEM  DAA CONTROL  MASKS                    27/1/86 MBW )
  1 HEX
  2 : CCT       232  04 ;    (     -- FLAG )
  3 : OH        232  08 ;    (     -- FLAG )
  4 : RCCT.79   232  20 ;    ( FLAG   --   )
  5 : OH.79     232  40 ;    ( FLAG   --   )
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->
Screen # 103
  0 ( V21/V23 MODEM   R2424 BASIC MODEM SETUP               27/1/86 MBW )
  1 HEX
  2 : DEFAULT.2424
  3   INIT
  4   EN.M
  5   V.22/2400
  6   1 BUS.R NOW 1 BUS.T NOW
  7   1 DTR NOW
  8   1 RTS NOW
  9   1 AAE NOW
 10   0DB          ( NO ATTENUATION BEFORE DAA )
 11   DEFAULT.8530 ;
 12
 13
 14 DECIMAL
 15 -->
Screen # 104
  0 ( V21/V23 MODEM   8530 STATUS                           27/1/86 MBW )
  1 HEX
  2 : RXREADY?   BEGIN 222 PC@ 1 AND 1 = UNTIL ;
  3 : TXREADY?   BEGIN 222 PC@ 4 AND 4 = UNTIL ;
  4 : DCD.8530?  BEGIN 222 PC@ 08 AND 08 = UNTIL ;
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 105
  0 ( V21/V23 MODEM   PHONE NUMBER ENTERING              27/1/86 MBW )
  1 HEX
  2 0 VARIABLE PHONE.NUMBER 20 ALLOT
  3 : PHONE.NUMBER.PROMPT
  4   ." ENTER PHONE NUMBER "  ;
  5
  6 : READY.TO.DIAL?
  7   BEGIN DDRE IS UNTIL ;
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->

Screen # 106
  0 ( V21/V23 MODEM   DIALER                             27/1/86 MBW )
  1 HEX
  2 : DIAL  PHONE.NUMBER.PROMPT
  3   PHONE.NUMBER 20 EXPECT CR
  4       1 DTMF NOW 1 CRQ.T NOW ." DIALING # " 1 SEC  PHONE.NUMBER
  5   BEGIN DUP 1+ SWAP C@ DUP DUP 0=
  6   IF
  7     DROP DROP 1
  8                ELSE DUP 44 = IF
  9                                  2 SEC DROP DROP 0
 10                                        ELSE READY.TO.DIAL?
 11                                        0F AND 210 PC! EMIT 0
 12                                THEN
 13  THEN
 14  UNTIL DROP READY.TO.DIAL? FF 210 PC! -14DB  CLS ;
 15 DECIMAL -->

Screen # 107
  0 ( V21/V23 MODEM   7910 CONFIGURATION                 27/1/86 MBW )
  1 HEX
  2 : V21.ANS.7910   230 PC@ E0 AND 05 OR 230 PC! ;
  3 : V21.ORG.7910   230 PC@ E0 AND 04 OR 230 PC! ;
  4 : V23.7910       230 PC@ E0 AND 06 OR 230 PC! ;
  5 : V23.EQU.7910   230 PC@ E0 AND 07 OR 230 PC! ;
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 108
  0 ( V21/V23 MODEM   7910 CONNECT V.21                27/1/86 MBW )
  1 HEX
  2 : CONNECT.V21.ORG
  3   CLS ." V.21 300BPS MODE "  CR
  4   DEFAULT.2424
  5   V21.ORG.7910
  6   DIAL
  7   1 RCCT.79 NOW 1 OH.79 NOW EN.79
  8   0 CRQ.T NOW
  9   DTR.8530.ON
 10   DCD.8530? ." CARRIER DETECTED  . . . ON LINE "  CR CR
 11   RTS.8530.ON
 12   300BPS.8530 TALK     ;
 13
 14 DECIMAL
 15 -->

Screen # 109
  0 ( V21/V23 MODEM   7910 CONNECT V.23                27/1/86 MBW )
  1 HEX
  2 : CONNECT.V23.ORG
  3   CLS ." V.23 1200BPS MODE "  CR
  4   DEFAULT.2424
  5   V23.7910
  6   DIAL
  7   1 RCCT.79 NOW 1 OH.79 NOW EN.79
  8   0 CRQ.T NOW
  9   DTR.8530.ON
 10   DCD.8530? ." CARRIER DETECTED  . . . ON LINE "  CR CR
 11   RTS.8530.ON   1200BPS.8530
 12   TALK     ;
 13
 14 DECIMAL
 15 -->

Screen # 110
  0 ( V21/V23 MODEM   2424 CONNECT V.22                27/1/86 MBW )
  1 HEX
  2 : CONNECT.V22.ORG
  3   CLS ." V.22 1200BPS MODE "  CR
  4   DEFAULT.2424  V.22/1200 1200BPS.8530
  5   DIAL
  6   BEGIN CTS IS 1 = UNTIL  ." CARRIER DETECTED  . . . ON LINE "
  7   CR CR TALK     ;
  8 : CONNECT.V22.2400
  9   CLS ." V.22 2400BPS MODE "  CR
 10   DEFAULT.2424
 11   DIAL
 12   BEGIN CTS IS 1 = UNTIL  ." CARRIER DETECTED  . . . ON LINE "
 13   CR CR TALK     ;
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 111
  0 ( V21/V23 MODEM   V.22 ANSWER MODE CONNECTIONS     27/1/86 MBW )
  1 HEX
  2 : V22BIS.CONNECTION
  3   ." CONNECTED TO V.22 BIS MODEM AT 2400 BPS " CR CR
  4   TALK     ;
  5
  6 : V22.CONNECTION
  7   ." CONNECTED TO V.22 MODEM AT 1200 BPS "  CR CR
  8   1200BPS.8530
  9   TALK     ;
 10
 11
 12
 13
 14 DECIMAL
 15 -->
Screen # 112
  0 ( V21/V23 MODEM  V.21/V.23 ANSWER MODE CONNECTIONS 27/1/86 MBW )
  1 HEX
  2 : V21.CONNECTION
  3   ." CONNECTED TO V.21 MODEM AT 300BPS " CR CR
  4   V21.ANS.7910
  5   1 RCCT.79 NOW 1 OH.79 NOW EN.79
  6   DTR.8530.ON RTS.8530.ON
  7   300BPS.8530
  8   TALK     ;
  9 : V23.CONNECTION
 10   ." CONNECTED TO V.23 MODEM AT 1200BPS "  CR CR
 11   V23.7910
 12   1 RCCT.79 NOW 1 OH.79 NOW EN.79
 13   DTR.8530.ON
 14   1200BPS.8530
 15   TALK     ;  DECIMAL -->
Screen # 113
  0 ( V21/V23 MODEM   AUTO ANSWER MODE  1 OF 2         27/1/86 MBW )
  1 HEX
  2 : AUTO.ANSWER
  3   DEFAULT.2424
  4   CLS ." UNIVERSAL ANSWER MODE " CR
  5       ." WAITING TO BE CALLED " CR
  6   BEGIN RI IS UNTIL
  7       ." RING DETECTED . . .  " CR
  8   BEGIN DSR  IS UNTIL
  9       ." DATA SET READY  ON   " CR
 10   1 SEC
 11
 12
 13
 14 DECIMAL
 15 -->
```

Figure 14. International Modem FORTH Screens (Continued)

```
Screen # 114
  0 ( V21/V23 MODEM   AUTO ANSWER MODE  2 OF 2          27/1/86 MBW )
  1 HEX
  2   SPEED? DUP 3 = IF V22BIS.CONNECTION ELSE
  3          DUP 2 = IF V22.CONNECTION    ELSE
  4   THEN THEN DROP
  5   RLSD IS IF V23.CONNECTION ELSE V21.CONNECTION THEN ;
  6
  7
  8
  9
 10
 11
 12
 13
 14 DECIMAL
 15 -->


Screen # 115
  0 ( V21/V23 MODEM   MENU SCREEN                        27/1/86 MBW )
  1 HEX
  2 : MENU INIT  BEGIN
  3   CLS  A 3  GOTOXY  ." ROCKWELL INTERNATIONAL'S   " CR
  4   CR   A SPACES     ." INTERNATIONAL MODEM ....   " CR
  5   CR CR A  SPACES   ." F1  V.21 ORIGINATE         " CR
  6         A  SPACES   ." F2  V.22 ORIGINATE 1200    " CR
  7         A  SPACES   ." F3  V.22 ORIGINATE 2400    " CR
  8         A  SPACES   ." F4  V.23 ORIGINATE         " CR
  9         A  SPACES   ." F5  AUTO ANSWER/CONFIGURE  " CR
 10 PCKEY DROP DUP 3B = IF CONNECT.V21.ORG  ELSE
 11            DUP 3C = IF CONNECT.V22.ORG  ELSE
 12            DUP 3D = IF CONNECT.V22.2400 ELSE
 13            DUP 3E = IF CONNECT.V23.ORG  ELSE
 14            DUP 3F = IF AUTO.ANSWER
 15 THEN THEN THEN THEN THEN SWAP DROP UNTIL ; MENU DECIMAL -->


Screen # 116
  0
  1
  2
  3
  4
  5
  6
  7
  8
  9
 10
 11
 12
 13
 14
 15
```

Figure 14. International Modem FORTH Screens (Continued)

Rockwell

Quality of Received Data for Signal Processor-Based Modems

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INTRODUCTION

This application note provides the modem design engineer with detailed information on the generation and interpretation of diagnostic data featured in Rockwell's signal processor (SP)-based modems.

Rockwell's plug-compatible SP-based modems can generate a variety of diagnostic data. This data is extremely useful in the evaluation of modem performance and line conditions. A microprocessor interface can readily access diagnostic data and other useful signals via the SP interface memory.

The diagnostic capabilities of specific Rockwell modems are summarized in Table 1.

ACCESSING DIAGNOSTIC DATA

Diagnostic data can be readily accessed via the microprocessor interface. The host processor must store the access code corresponding to the desired data in the RAM access register (See Table 2). The signal processor then stores the desired data in diagnostic data registers. The data available flag (R48DP, R96DP, R96FT and R96FAX only) in the respective interface memory sets when the signal processor writes data into diagnostic register zero and resets when the host reads data from register zero and is used to handshake with the diagnostic data registers. Diagnostic data is generated in 16-bit double precision form, although for most applications only the most significant byte of data is necessary. The RAM access codes for the SP-based modems are shown in Table 2. Functional block diagrams that relate the RAM access codes to specific functions are shown in Figures 1 through 4. Refer to the applicable modem data sheet for specific details regarding an individual modem.

EYE PATTERN

A quadrature eye pattern is an extremely useful diagnostic tool. The visual display of an eye pattern can be monitored to identify common line disturbances, as well as defects in the modulation/demodulation processes.

The ideal eye patterns or signal constellations for the various encoding methods are illustrated in Figures 5 through 10. By performing digital-to-analog (D/A) conversion of the received signal point data (refer Table 2, Node 9), an eye pattern can be displayed on an oscilloscope. Two methods of eye pattern generation are available:

1. The microprocessor can read the received signal points and then write this data into two memory mapped D/A converters. Figure 11 shows a typical microprocessor interface eye pattern generator. A typical parallel eye pattern algorithm is shown in Figure 12.
2. High speed modems (4800 bps and above) can generate diagnostic data serially through hardware pins in the modem connector.

5

Table 1. Summary of Diagnostic Capabilities for SP-Based Modems

Modem	Eye Pattern		EQM Value	Error Vector	Phase Error	Access to SP RAM Space[2]
	Serial	Parallel MPU Bus				
R1212M		X	1	X	X	X
R1212DC		X	1	X	X	X
R2424M		X	1	X	X	X
R2424DC		X	1	X	X	X
R48DP	X	X	X	X		X
R96DP	X	X	X	X		X
R96FT	X	X	X	X		X
R96FAX	X	X	X	X		X

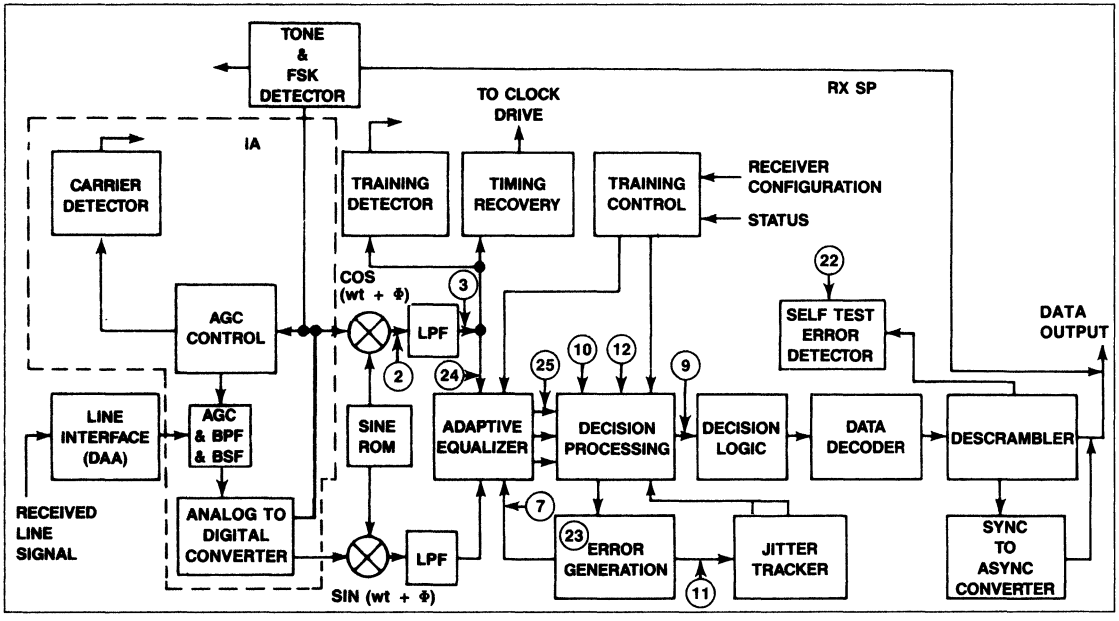
Notes:
1. EQM may be computed by the host processor from the error vector data.
2. See RAM access codes (Table 2) and block diagrams (Figures 1–4).

Table 2. RAM Access Codes

Node No.	Function	R1212M/DC R2424M/DC			R48DP/R96DP				R96FT				R96FAX		
		Access Codes	Chip No.	Reg. No.	RAM Access X	RAM Access Y	Chip No.	Reg. No.	RAM Access X	RAM Access Y	Chip No.	Reg. No.	RAM Access	Chip No.	Reg. No.
1	Received Signal Samples (and Output)				C0	—	1	2,3	DC	—	1	2,3	C0	0	2,3
2	Demodulator Output	56	0	2,3,4,5	C2	42	1	0,1,2,3	C0	40	1	0,1,2,3	42	0	0,1,2,3
3	Low Pass Filter Output	40	0	2,3,4,5	D4	54	1	0,1,2,3	DD	5D	1	0,1,2,3	54	0	0,1,2,3
4	Average Energy				—	04	1	0,1	—	32	1	0,1	DC	0	2,3
5	AGC Gain Word				81	—	1	2,3		2E	1	2,3	81	0	2,3
6	Equalizer Input				C0	40	2	0,1,2,3	C0	40	2	0,1,2,3	40	1	0,1,2,3
7	Equalizer Taps	01-0D	0	2,3,4,5	81-A0	01-20	2	0,1,2,3	81-A0	01-20	2	0,1,2,3	01-20	1	0,1,2,3
8	Unrotated Equalizer Output				E1	61	2	0,1,2,3	E1	61	2	0,1,2,3	61	1	0,1,2,3
9	Rotated Equalizer Output (Received Point Eye Pattern)	11	0	2,3,4,5	A2	22	2	0,1,2,3	E2	62	2	0,1,2,3	22	1	0,1,2,3
10	Decision Points (Ideal Eye Pattern Points)	51	0	2,3,4,5	E2	62	2	0,1,2,3	E8	68	2	0,1,2,3	62	1	0,1,2,3
11	Error Vector (Rotated Error)	52	0	2,3,4,5	E3	63	2	0,1,2,3	E5	65	2	0,1,2,3	63	1	0,1,2,3
12	Rotation Angle	12	0	4,5	—	00	2	0,1	A7	—	2	2,3	00	1	0,1
13	Frequency Correction				AA	—	2	2,3					A8	1	2,3
14	EQM	*			A7	—	2	2,3	AC	—	2	2,3	AB	1	2,3
15	Dual Point				AE	2E	2	0,1,2,3					—		
16	Group II Baseband Signal												C8	1	2,3
17	Group II AGC Gain Word												AD	1	2,3
18	Group II AGC Slew Rate												AA	1	2,3
19	Group II PLL Frequency Correction												C2	1	2,3
20	Group II PLL Slew Rate												F0	1	2,3
21	Group II Black/White Level												2A	1	0,1
22	Self Test Error Counter	00	0	2,3,4,5											
23	Phase Error	10	0	2,3											
24	Input Signal to Equalizer Taps	41-4D	0	2,3,4,5											
25	Equalizer Output	53	0	2,3,4,5											

Note: * EQM value may be computed by the host processor from error vector data, node 11.

Receiver/Equalizer Section



Transmitter Section

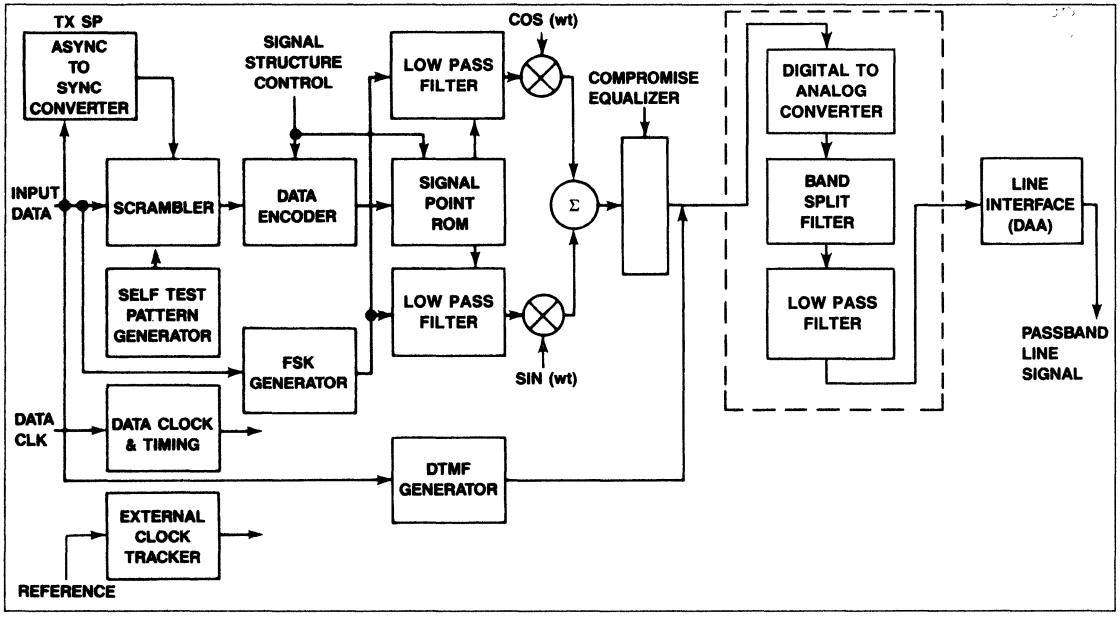


Figure 1. R1212/R2424 Processing Flow Diagram

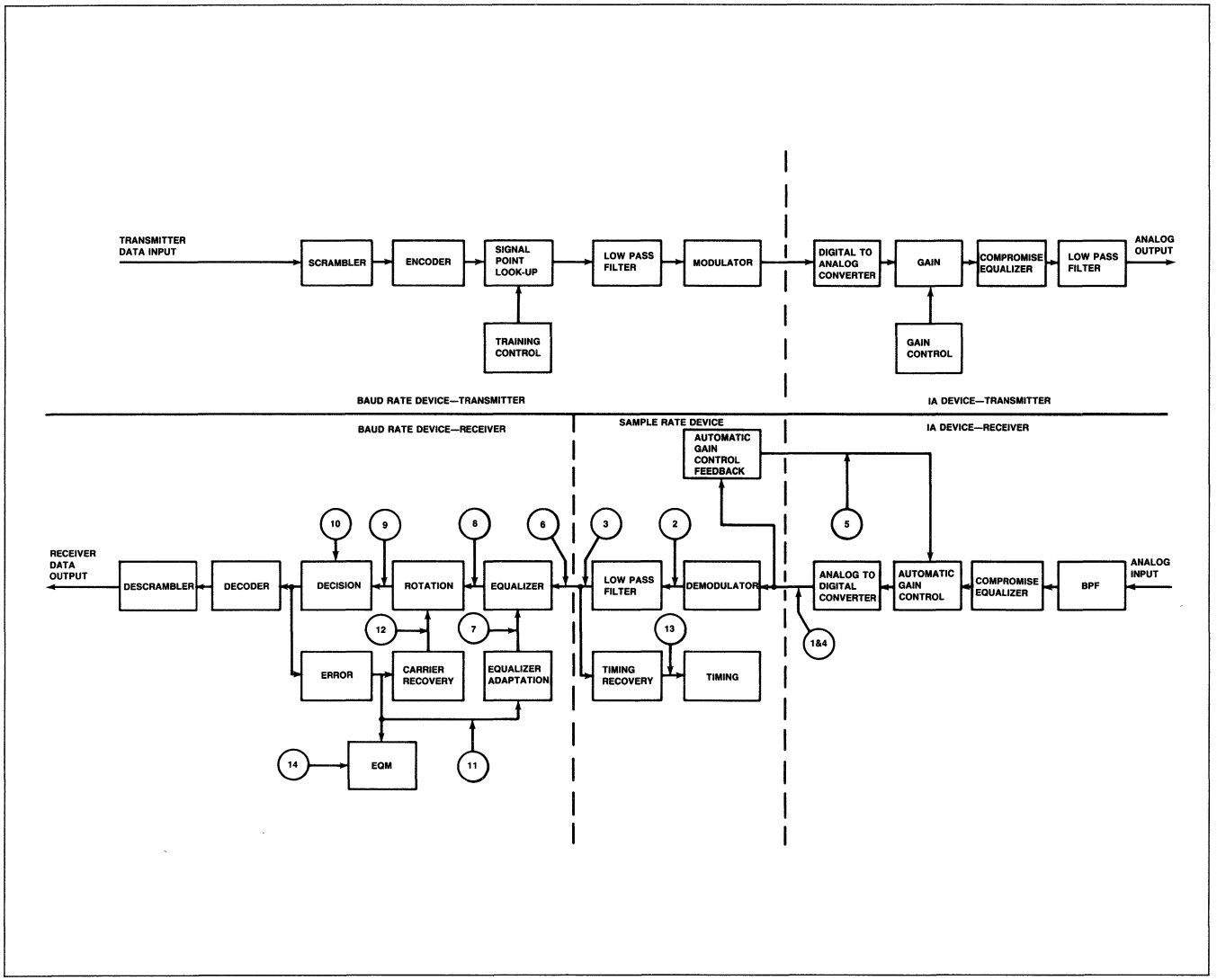


Figure 2. R48DP/R96DP/R96FT/R96FAX (Group 3) Processing Flow Diagram

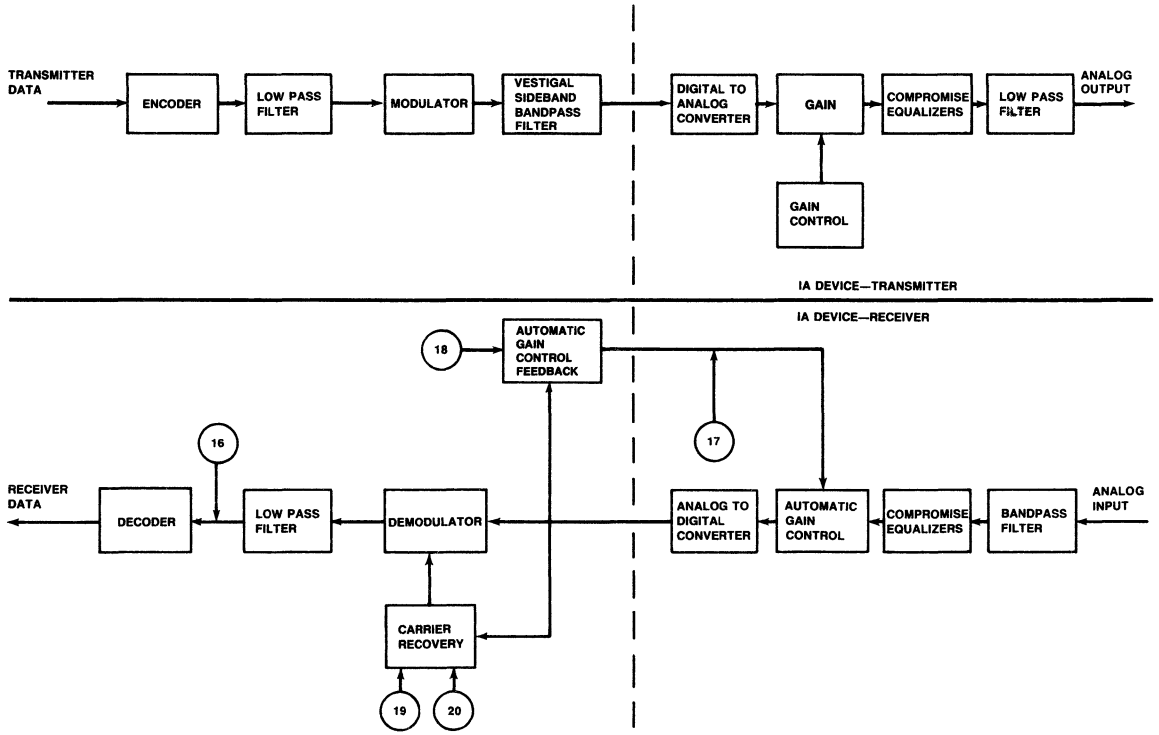


Figure 3. R96FAX (Group 2) Processing Flow Diagram

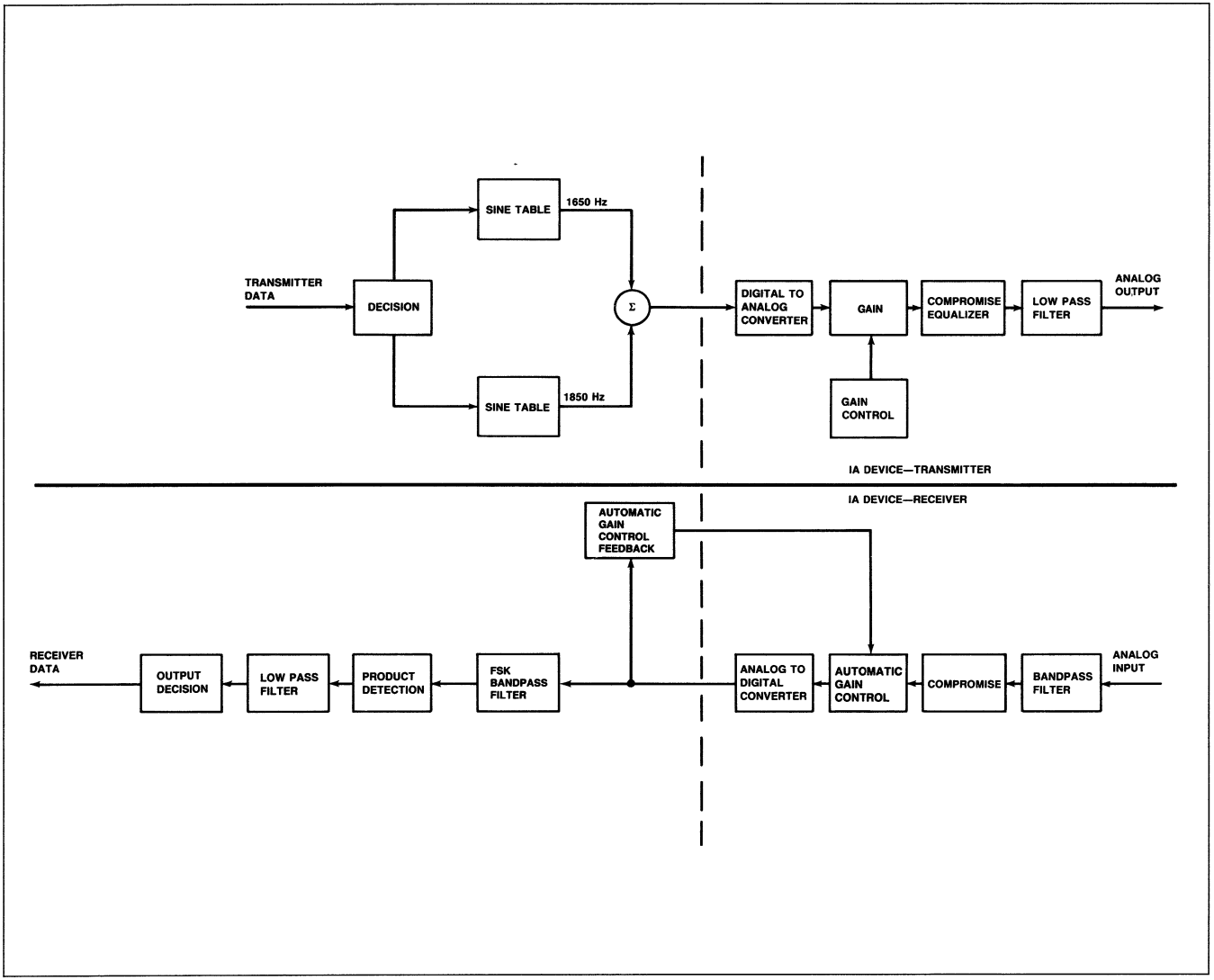
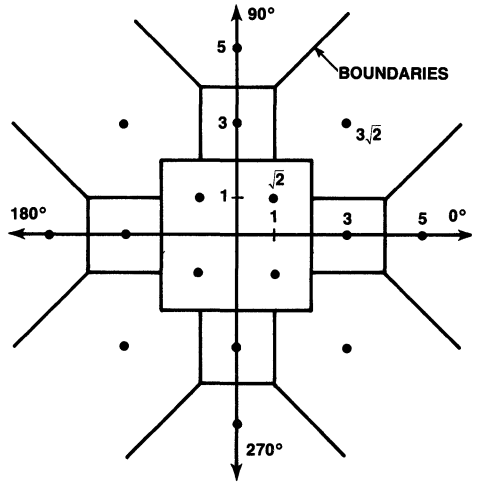
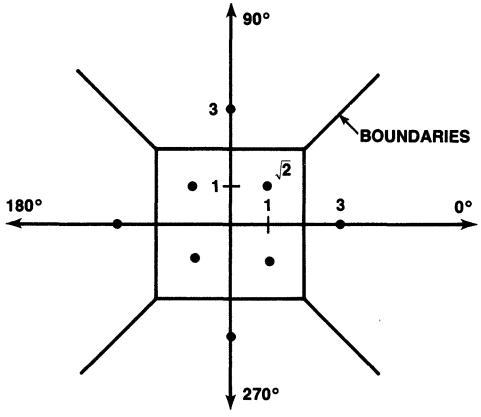


Figure 4. R96FAX FSK Processing Flow Diagram



Q2	Q3	Q4	PHASE CHANGE	ABSOLUTE PHASE	Q1	RELATIVE AMPLITUDE
0	0	1	0°	0°, 90°, 180°, 270°	0	3
0	0	0	45°			
0	1	0	90°		1	5
0	1	1	135°			
1	1	1	180°	45°, 135°, 225°, 315°	0	√2
1	1	0	225°			
1	0	0	270°		1	3√2
1	0	1	315°			

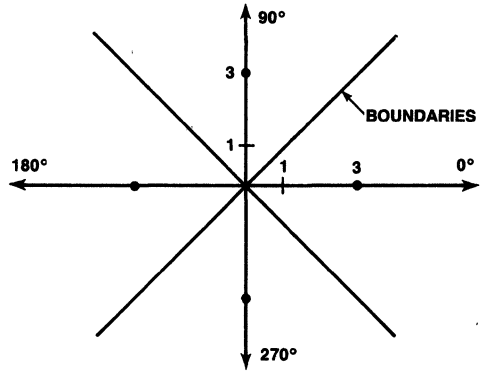
Figure 5. Ideal Eye Pattern—V.29/9600 bps



TRIBIT ENCODING:

IN V.29/7200 BPS FALLBACK MODE, DATA IS ENCODED IN GROUPS OF 3 BITS OR TRIBITS. THE ENCODING IS AS FOR V.29/9600 BPS ABOVE EXCEPT THAT: THE FIRST DATA BIT IN TIME DETERMINES Q2 OF THE MODULATOR QUADBIT. THE SECOND AND THIRD BITS IN TIME DETERMINE Q3 AND Q4, RESPECTIVELY. Q1 = 0 FOR ALL EIGHT SIGNAL ELEMENTS.

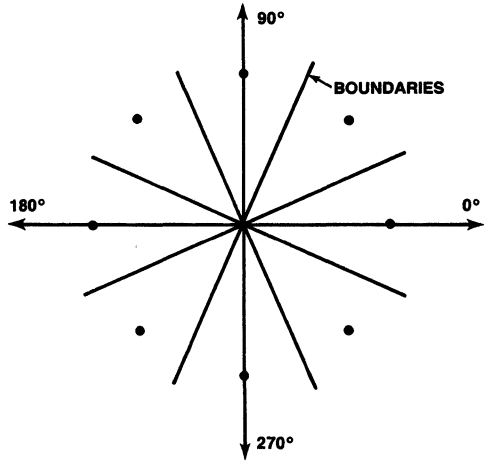
Figure 6. Ideal Eye Pattern—V.29/7200 bps



DIBIT ENCODING:

DATA BITS	PHASE CHANGE	RELATIVE AMPLITUDE
00	0°	CONSTANT
01	90°	
11	180°	
10	270°	

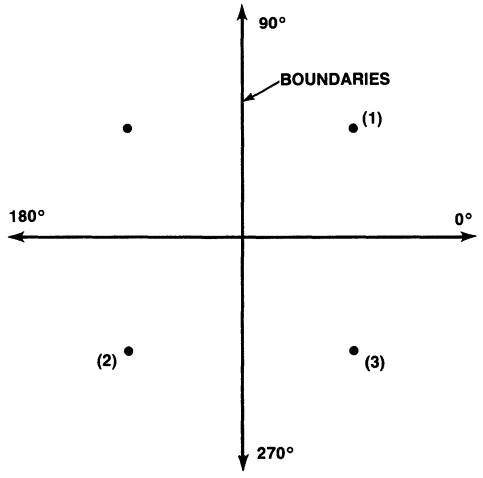
Figure 7. Ideal Eye Pattern—V.29/4800 bps and V.27/BIS/TER/2400 bps



TRIBIT ENCODING:

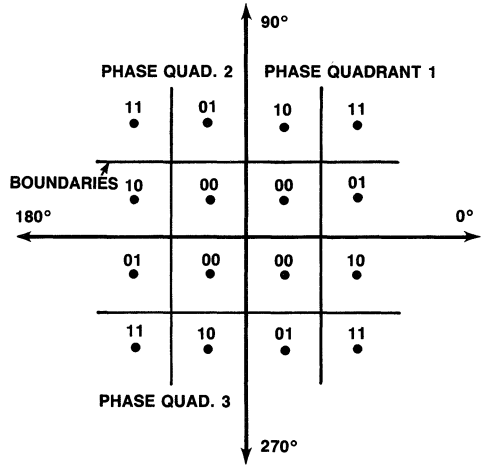
TRIBIT VALUE	PHASE CHANGE	RELATIVE AMPLITUDE
0 0 1	0°	CONSTANT
0 0 0	45°	
0 1 0	90°	
0 1 1	135°	
1 1 1	180°	
1 1 0	225°	
1 0 0	270°	
1 0 1	315°	

Figure 8. V.27 BIS/TER/4800 bps



DIBIT VALUES (1200)	BIT VALUES (600 BPS)	PHASE CHANGE
00	0	+90°
01	—	0°
11	1	+270°
10	—	+180°

Figure 9. V.22 A/B 1200 bps/600 bps



DATA IS ENCODED IN QUADBITS. THE FIRST TWO BITS OR DIBIT SELECT ONE OF FOUR QUADRANTS. THE SECOND DIBIT SELECTS ONE OF FOUR POINTS IN THAT QUADRANT, AS SHOWN BELOW.

FIRST TWO BITS IN QUADBIT [2400 BIT(S)] OR DIBIT VALUES [1200 BIT(S)]	PHASE QUADRANT CHANGE	
00	1 → 2 2 → 3 3 → 4 4 → 1	90°
01	1 → 1 2 → 2 3 → 3 4 → 4	0°
11	1 → 4 2 → 1 3 → 2 4 → 3	270°
100	1 → 3 2 → 4 3 → 1 4 → 2	180°

Figure 10. V.22 BIS/4800 bps

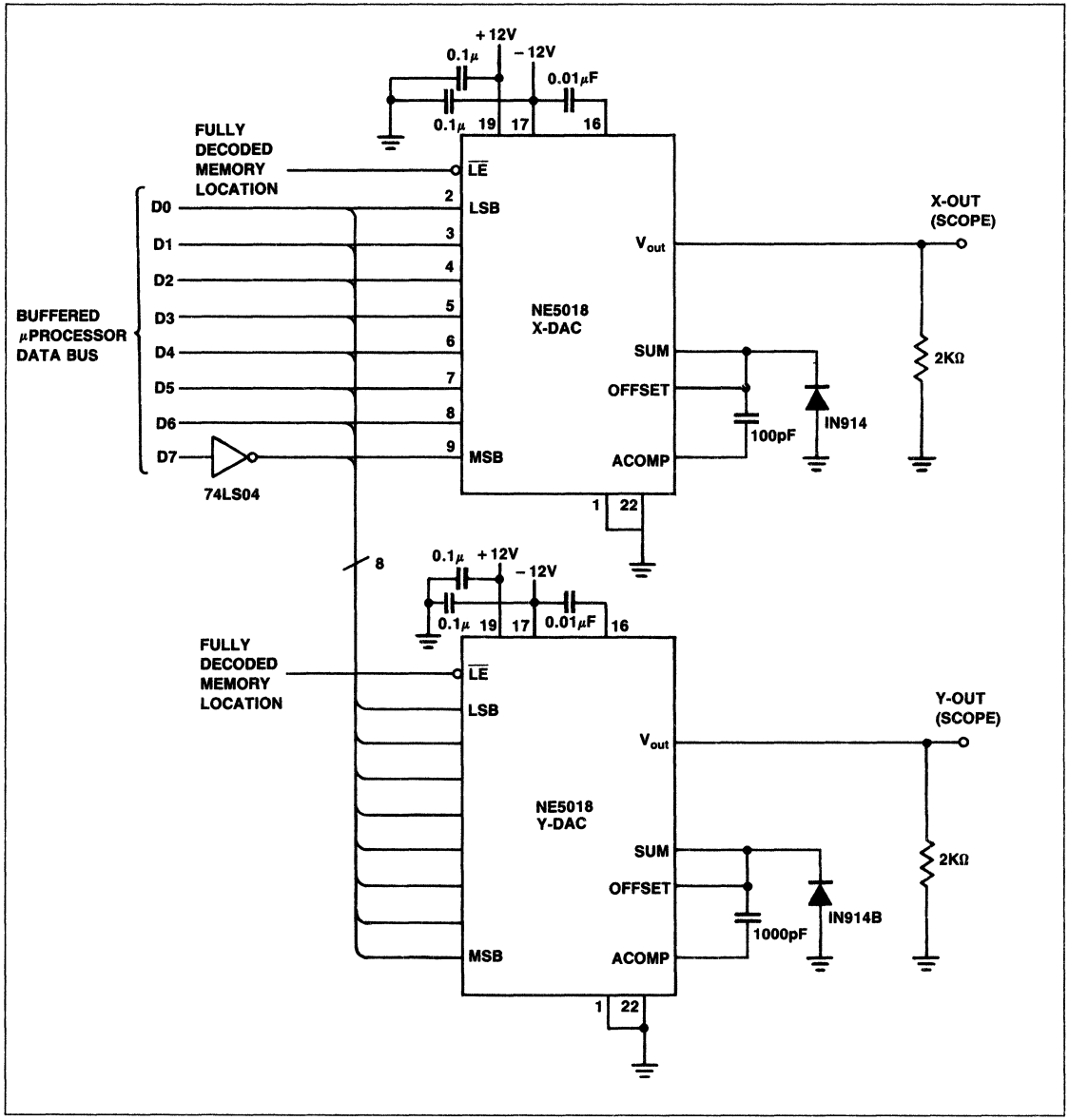


Figure 11. Typical Microprocessor Bus Eye Pattern Generator

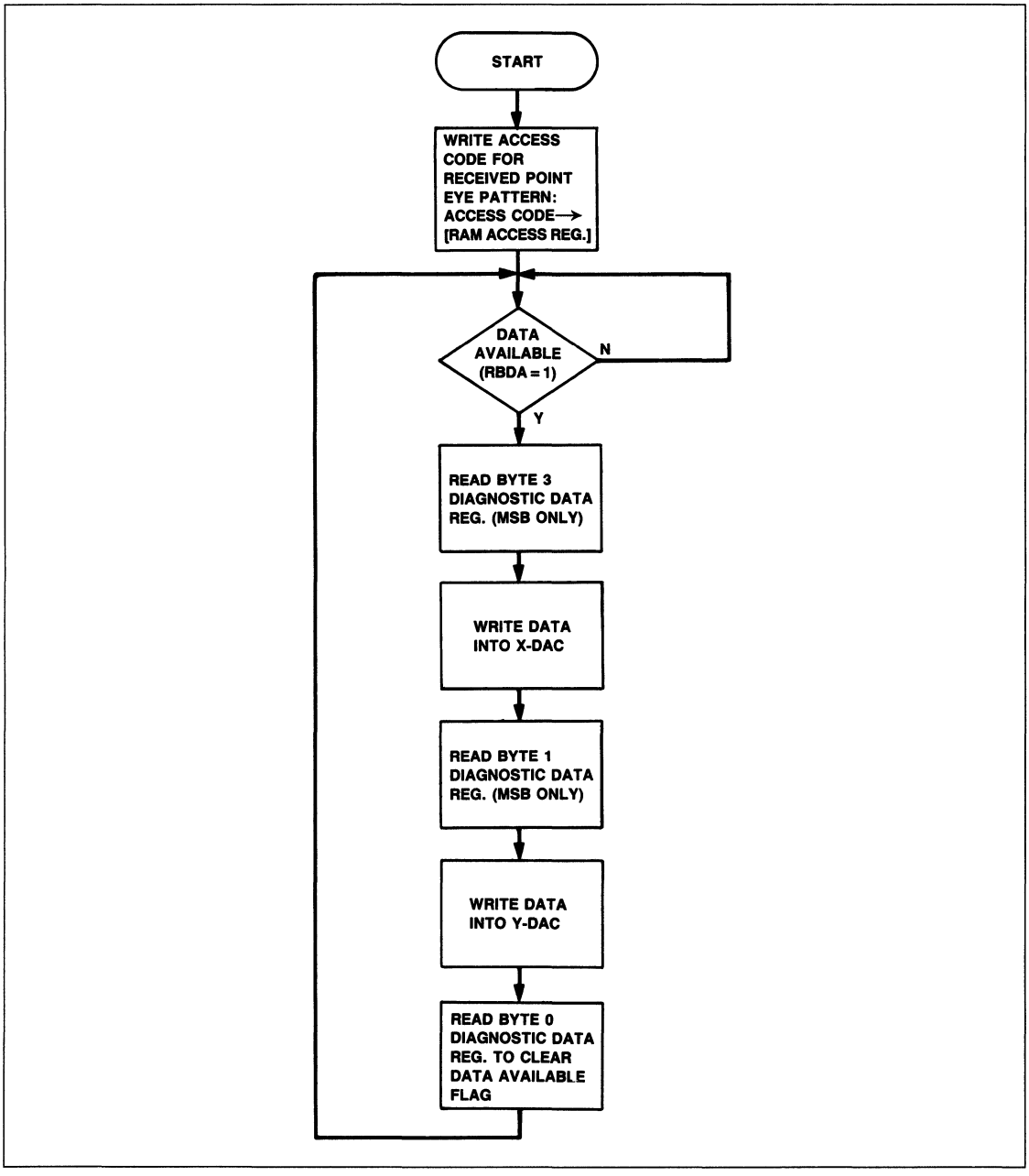


Figure 12. Typical Microprocessor Eye Pattern Generation Loop (R96DP/R48DP)

The hardware necessary to generate a serial eye pattern along with the relevant timing signals are shown in Figures 13 and 14.

The eye pattern consists of dots or received signal points. Each point represents the location of a received signal element in the

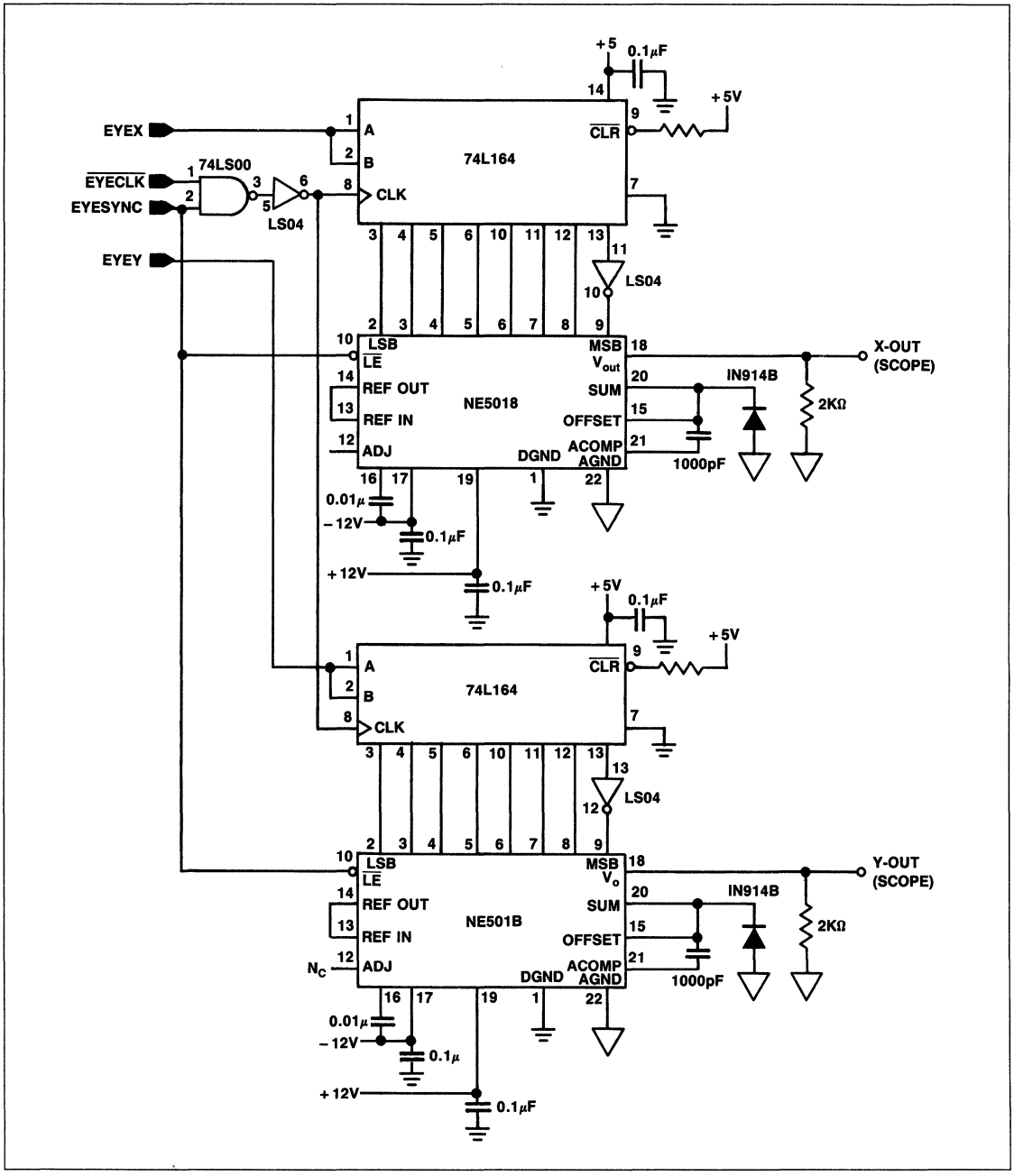


Figure 13. Serial Eye Pattern Generator

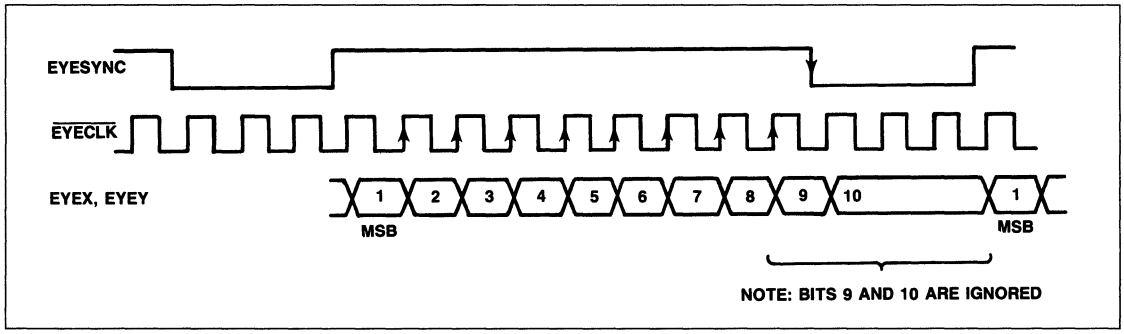


Figure 14. Serial Eye Pattern Signal Timing

baseband signal plane. In polar coordinates each point represents a magnitude and differential phase shift. Eye pattern data is updated at the baud rate so the oscilloscope display appears to be a continuous signal constellation.

For a DPSK (Differential Phase Shift Keyed) modem, the phase shift from one signal element to the next is decoded to recover data. For a QAM (Quadrature Amplitude Modulation) modem, both amplitude and differential phase shift are decoded to recover data.

Assume a V.22/1200 bps configuration (R1212 modem), and that initially a dot is displayed at point 1 of Figure 9. If the first dibit received is 10, the point displayed will be point 2, corresponding to a 180° shift in phase. If the second dibit is a 00 (90°), point 3 will be displayed. In this fashion a continuous stream of random data produces the display of Figure 9.

TYPICAL LINE DISTURBANCES

Actual received signal points are distorted by one or more types of line disturbances such as noise, phase or amplitude hits, phase or amplitude jitter, harmonic distortion and drop-outs.

White noise produces a smearing of each signal constellation point around its ideal location (see Figure 15A).

Phase jitter produces periodic phase smearing with little or no amplitude effect (see Figure 15B).

Harmonic distortion produces a non-periodic amplitude smearing with little phase effect (see Figure 15C).

Amplitude jitter produces an effect similar to harmonic distortion, but in this case the disturbance is periodic.

An amplitude (or phase) hit is associated with an instantaneous high error in the amplitude (or phase) signal component.

The degree of smearing in the eye pattern is proportional to the severity of the particular disturbance. These disturbances may occur in combination producing more complex smearing of the eye pattern.

A point falling within the signal space delimited by boundaries is decoded by the modem as if it were located at the ideal point within that space. When a line disturbance causes the signal point to cross a decision boundary, the received signal point is incorrectly decoded.

ERROR VECTOR AND EQM VALUES

Transient phenomena are difficult to observe in a quadrature eye pattern. Also, the proper interpretation of the eye pattern is a function of the observer's training and requires constant attention. Rockwell's signal processor modems generate error vector and Eye Quality Monitor (EQM) data that are more suitable for microprocessor manipulation and interpretation.

The error vector is defined as the angle and magnitude difference between an actual received signal point and its ideal location in the baseband signal plane (refer to Figure 16). Error vectors are represented as complex numbers whose real and imaginary components may be read out of the modem's diagnostic registers once per baud. An EQM value may be obtained by processing the error vector data to obtain a positive hexadecimal value whose magnitude is an indicator of the quality of the received signal or probability of error of received signal points. In the case of high speed modems (R48DP, R96DP, R96FT, and R96FAX), the error vector is processed by the SP devices and the EQM value is available through the diagnostic data registers. For medium speed modems (R1212 and R2424), the EQM value may be computed by the host processor using the error vector data. An algorithm for computing EQM values is given below.

It is desirable to have a quantity whose magnitude is proportional to the time average of the error vector magnitude. The error vector magnitude may be approximated by its squared magnitude eliminating the computation of a square root:

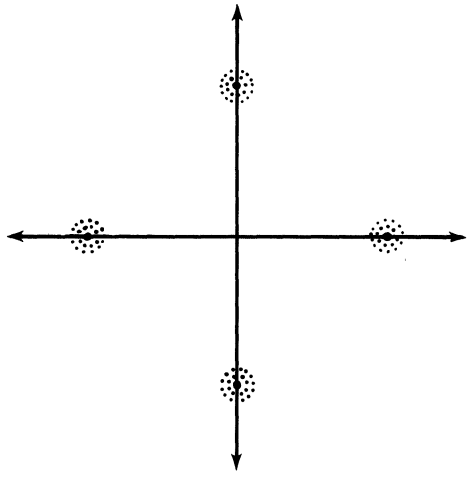
$$\text{Re (ERROR)}^2 + \text{Im (ERROR)}^2 \qquad \text{(Eq. 1)}$$

The squared magnitude may then be averaged by a digital filter of transfer function (see Figure 17):

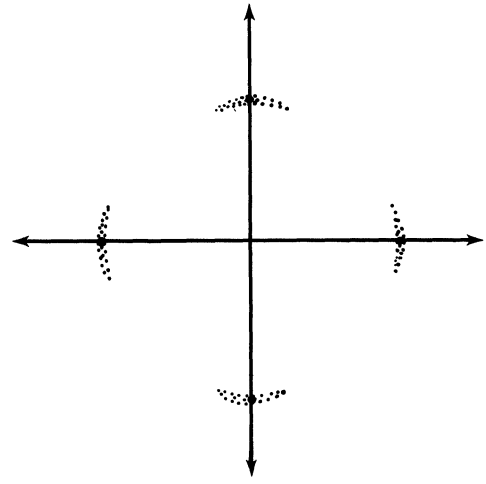
$$H(Z) = \frac{\alpha}{1 - \beta Z^{-1}} \qquad \text{(Eq. 2)}$$

The coefficients α and β may be computed by a Z-domain approximation to an RC network of transfer function (see Figure 18):

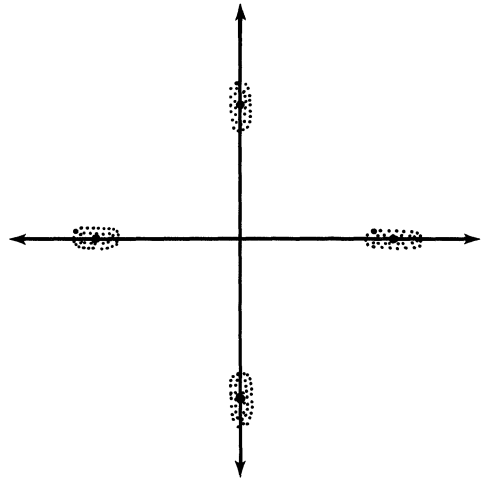
$$H(s) = \frac{1}{1 + S\tau}, \tau = RC \qquad \text{(Eq. 3)}$$



A. WHITE NOISE



B. PHASE JITTER



C. HARMONIC DISTORTION
(NON-PERIODIC) AMPLITUDE
JITTER (PERIODIC)

Figure 15. Typical Line Disturbances

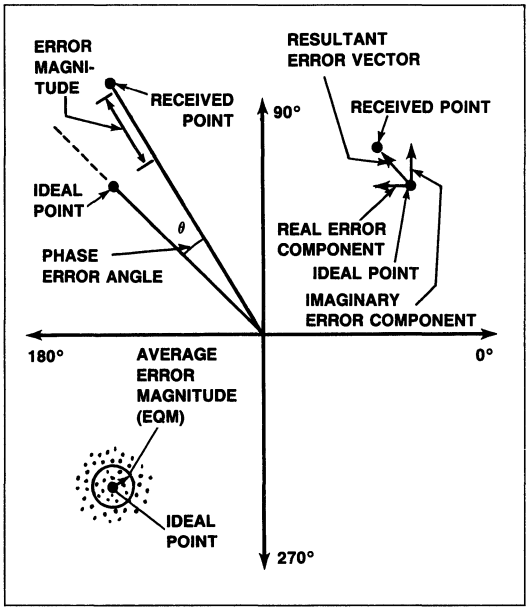


Figure 16. Error Vector Phase Error/EQM

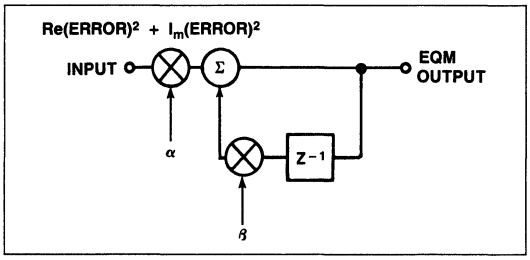


Figure 17. Digital Energy Averaging Filter

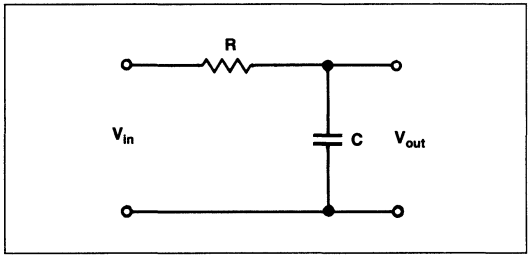


Figure 18. Equivalent Analog RC-Network

Substituting variables (first backward difference approximation) $S = 1 - Z^{-1}/T$ yields α and β (τ = RC, T = sampling period 1/T = 7200 Hz for R1212/R2424):

$$\alpha = \frac{1}{1 + \tau/T} = \frac{1}{1 + 7200\tau} \qquad \text{(Eq. 4)}$$

$$\beta = \frac{\tau/T}{1 + \tau/T} = \frac{1}{1 + \frac{1}{7200\tau}} \qquad \text{(Eq. 5)}$$

Re-writing the transfer function H(Z) (Equation 1) as a difference equation:

$$y(n) = \alpha u(n) + \beta y(n-1) \qquad \text{(Eq. 6)}$$

Letting the input sequence u(n) = Re $(\text{ERROR}(n))^2$ + Im $(\text{ERROR}(n))^2$ and the output y(n) = EQM(n) we obtain:

$$\text{EQM}(n) = \alpha\left[\text{Re}(\text{ERROR}(n))^2 + \text{Im}(\text{ERROR}(n))^2\right] + \beta\text{EQM}(n-1) \qquad \text{(Eq. 7)}$$

where: EQM(n) = Current EQM value.
EQM(n − 1) = EQM value delayed by one sample period.
Re (ERROR (n)) = Real component of the error vector.
Re (ERROR (n)) = Imaginary component of the error vector.

If we choose τ = 0.1 seconds and 1/T = 7200 Hz then, α = 0.001386962 and β = 0.998613037. Note that $\alpha + \beta = 1$ and $\alpha \ll \beta < 1$.

The EQM value is the filtered squared magnitude of the error vector. These values represent the probability of error and can be used to implement a discrete Data Signal Quality Detector circuit (circuit 110 of CCITT recommendation V.24 or circuit CG of RS-232-C recommendation) by comparing the EQM value against an experimentally obtained criteria (refer to Figures 19 and 20).

Bit Error Rate (BER) curves as a function of the signal-to-noise ratio (SNR) are used to establish a criteria for determining the acceptance of EQM values. Figure 20 is a typical BER curve showing the meaning of a given EQM value in terms of BER and SNR. From an EQM value, the host processor can determine an approximate BER value. If the BER is found to be unacceptable, the host may cause the modem to fall-back to a lower speed to improve BER.

It should be noted that the meaning of EQM varies with the type of line disturbance present on the line and with the various configurations. A given magnitude of EQM in V.29/9600 does not represent the same BER as in V.29/4800. The former configuration has 16 signal points that are more closely spaced than the four signal points in the latter, resulting in a greater probability of error for a given level of noise or jitter. Also, the type of disturbance has a significant bearing on the EQM value. For example, white noise produces an evenly distributed smearing of the eye pattern with about equal magnitude and phase error while phase jitter produces phase error with little error in magnitude.

Recalling that EQM is an average of the squared magnitude of the error vector, it can be seen that the correspondence of EQM to SNR (and hence BER) is dependent upon the signal structure of the modulation being used and the type of line disturbance present.

5

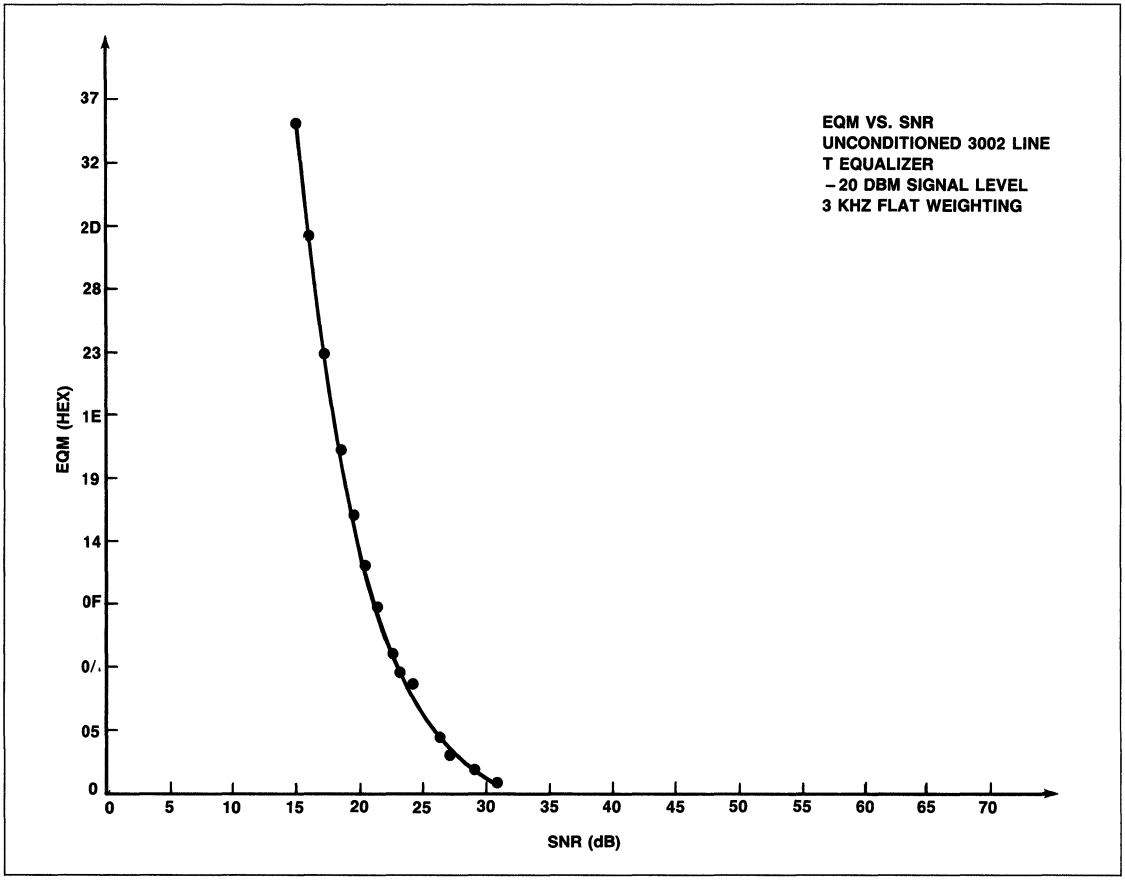


Figure 19. Typical Eye-Quality Versus Signal-To-Noise Ratio for V.29/9600 (R96FAX)

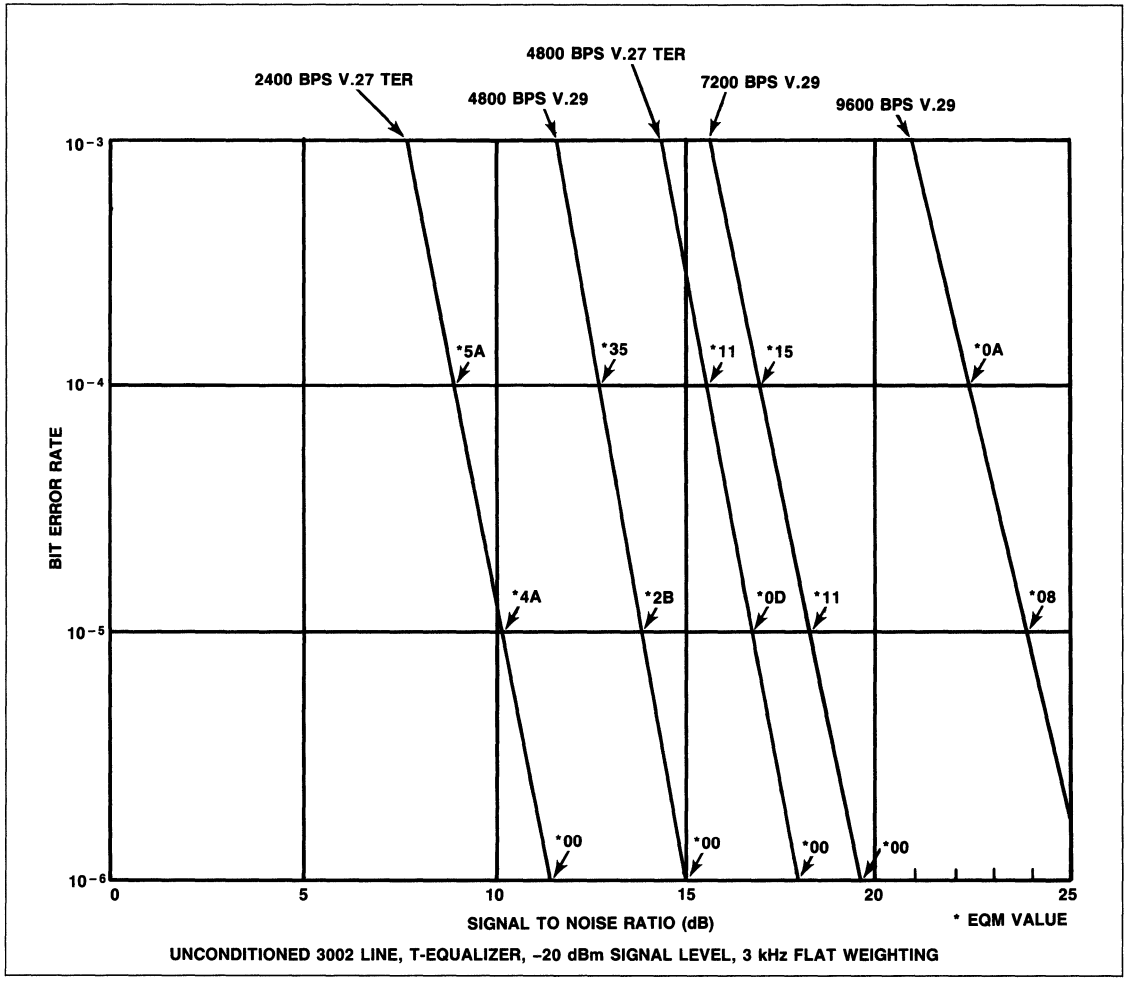


Figure 20. Typical Bit Error Rate Versus SNR and EQM

SCALING OF SP SIGNALS (R48DP, R96DP, R96FT, AND R96FAX)

The following list of formulas can be used to obtain diagnostic data in engineering units. Typical values or ranges for the data are also given.

CONVERSION FORMULAS, RANGES AND TYPICAL VALUES FOR R48DP, R96DP AND R96FAX MODEMS

1. **AGC Gain Word (16 bits unsigned)—Node 5**

   Range:
   $0F00_{16}$ – $7FFF_{16}$ for LRTH = 0 (–43 dBm Threshold)
   0640_{16} – $7FFF_{16}$ for LRTH = 1 (–47 dBm Threshold)

$$\text{AGC Gain in dB} = 50 - \frac{\text{AGC Gain Word}}{(100)_8} \times 0.097 \text{ dB}$$

2. **Average Power Word (16 bits)—Node 4**

   Typical value: $4211_8 = 0889_{16}$ (corresponding to 0 dBm)

$$\text{Post-AGC Average Power in dBm} = 10 \text{ Log} \left(\frac{\text{Average Power Word}}{(889)_{16}} \right) \text{dBm}$$

$$\text{Pre-AGC Average Power in dBm} = \text{(Post AGC Avg. Power in dBm – AGC gain in dB) dBm}$$

3. **A/D Sample Word (16 bits two's complement)—Node 1**

   (Refer to Figure 21 for the location of V_{INT} and V_{EXT} signals)

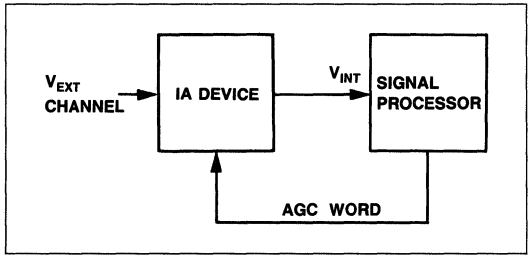


Figure 21. External and Internal Voltages

$$V_{INT} = \frac{\text{Signed, two's complement 16-bit A/D Word}}{(100)_8} \times \frac{3}{256} \text{Volts}$$

$$V_{EXT} = V_{INT} \div LOG_{10}^{-1} \left[\frac{\text{AGC Gain (dB)}}{20}\right]$$

4. **Rotation Angle Word (16 bits two's complement)—Node 12**

   Range: $-180° — +180°$

   Rotation Angle in degrees $= \frac{\text{Rot. Angle Word}}{2^{16}} \times 180°$

5. **Frequency Correction Word (16 bits two's complement)—Node 13** (Deviation from carrier in Hz)

   Range: $FC01_{16} - 0400_{16}$ (± 37.5Hz)

   Freq. Correction in Hz $= \left(\frac{\text{Freq. Correction word}}{2^{16}}\right)$ $\times$ (Baud Rate in Hz) Hz

6. **Error Vector Real (16 bits two's complement) and Imaginary (16 bits two's complement) Words**

   (Refer to Table 3.)

7. **Scaled Signal Points (16 bits two's complement) (V.29 to V.27)**

   (Refer to Figure 22 and Table 4.)

Table 3. Error Vector Maximum Values

Configuration	Bit Rate (BPS)	Real Error	Imag. Error	Magnitude $\sqrt{Re^2 + Im^2}$
V.29	9600	$<C00_{16}$	$<C00_{16}$	$<E66_{16}$
V.29	7200	$<2400_{16}$	$<2400_{16}$	$<1AD4_{16}$
V.29	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	4800	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$
V.27	2400	$<1C00_{16}$	$<1C00_{16}$	$<1C00_{16}$

Table 4. R48DP/R96DP/R96FAX Scaled Signal Points (Hex)

Point	Modem			
	V.29/9600 x , y	V.29/7200 x , y	V.29/4800 & V.27/2400 x , y	V.27/4800 x , y
1	0000, 2800	0000, 2400	0000, 1F00	0000, 1F00
2	2800, 0000	2400, 0000	1F00, 0000	1600, 1600
3	0000, D800	0000, DC00	0000, E100	1F00, 0000
4	D800, 0000	DC00, 0000	E100, 0000	1600, EA00
5	0000, 1800	0C00, 0C00		0000, E100
6	1800, 1800	0C00, F400		EA00, EA00
7	1800, 0000	F400, F400		E100, 0000
8	1800, E800	F400, 0C00		EA00, 1600
9	0000, E800			
10	E800, E800			
11	E800, 0000			
12	E800, 1800			
13	0800, 0800			
14	0800, F800			
15	F800, F800			
16	F800, 0800			

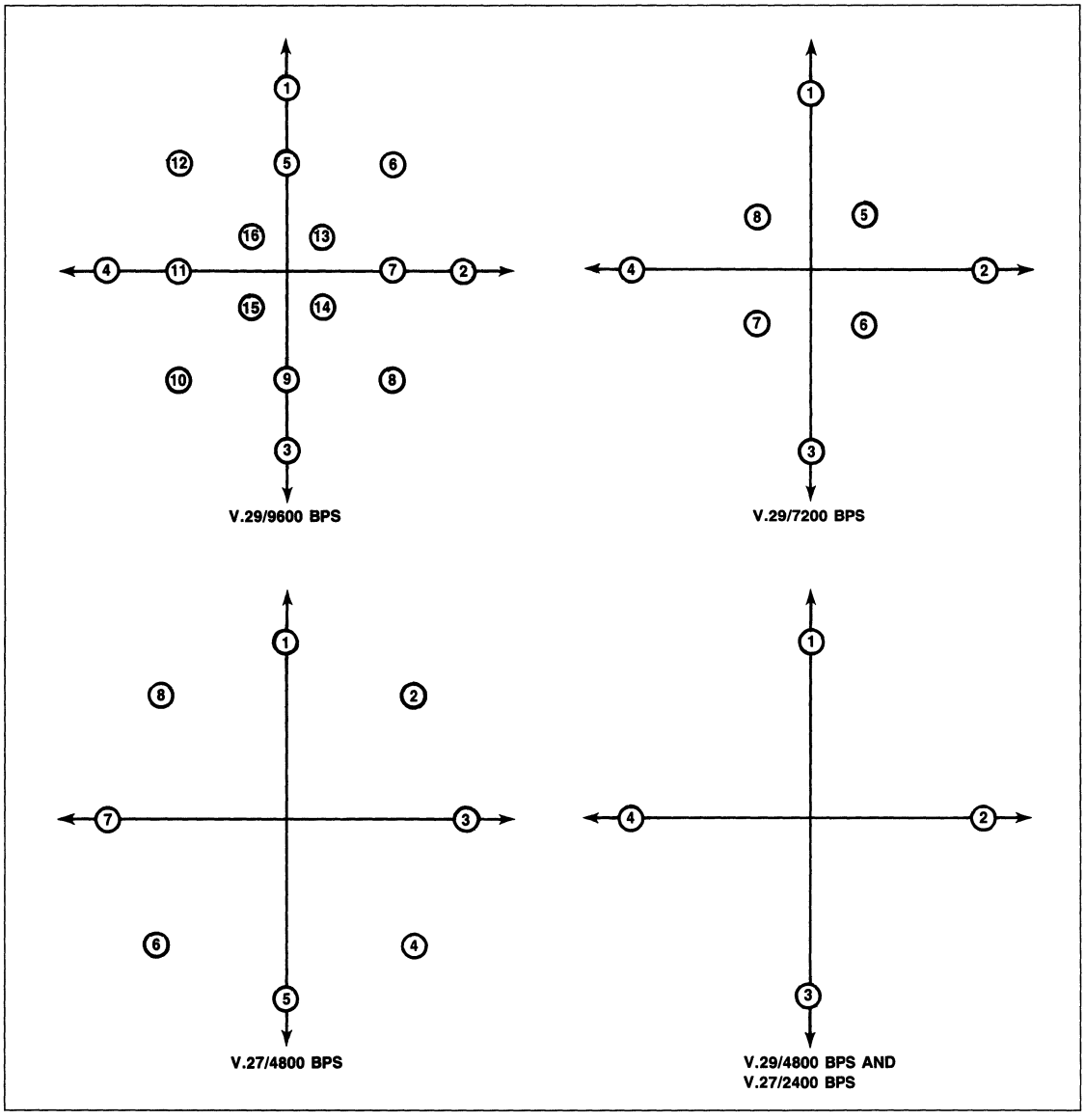


Figure 22. Scaled Signal Points

SCALING OF SP SIGNALS (R1212 AND R2424)

1. **Rotation Angle (16 bits unsigned)—Node 12**
   Range: 0° — 360°

$$\text{Rotated Angle} = \left[\left(\frac{\text{16 Bit Rotated Angle Word}}{2}\right) \bullet 7FFF_{16}\right] \times 5B_{16}$$

2. **Phase Error (16 bits two's complement)—Node 22**

$$\text{Phase Error}^\circ = \frac{\text{16 Bit Phase Error Word}}{K}$$

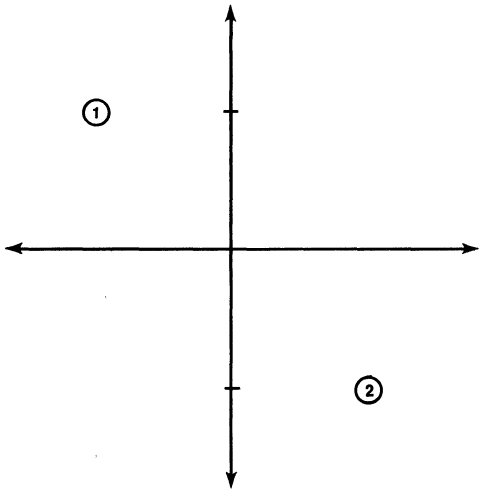
Where: $-45^\circ \leq$ Phase Error $\leq 45^\circ$

$K = 28_{16}$ for 2400 bps
$K = 14_{16}$ for 1200 bps

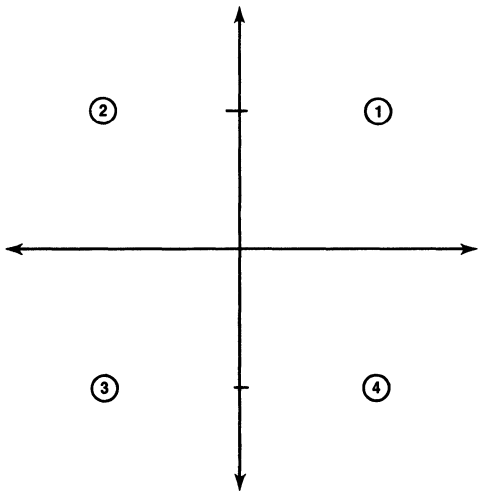
3. **Scaled Signal Points (16 bit two's complement)**
   (Refer to Figure 23 and Table 5.)

Table 5. R1212 and R2424 Scaled Signal Points (Hex)

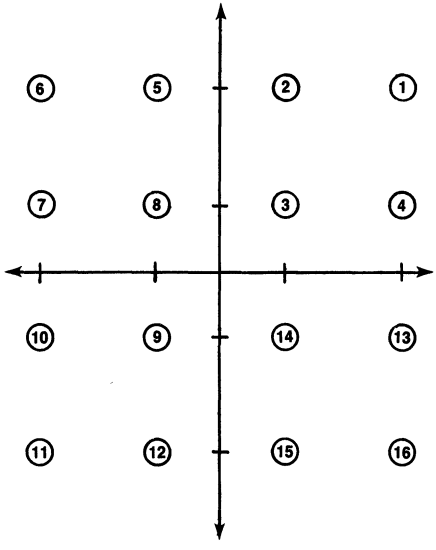
Point	Modem		
	V.22 bis/2400 bps x , y	V.22 A/B, Bell 212A/1200 bps x , y	V.22 A/B 600 bps x , y
1	1800, 1800	1100, 1100	EF00, 1100
2	800, 1800	EF00, 1100	1100, EF00
3	800, 800	EF00, EF00	
4	1800, 800	1100, EF00	
5	F800, 1800		
6	E800, 1800		
7	E800, 800		
8	F800, 800		
9	F800, F800		
10	E800, F800		
11	E800, E800		
12	F800, E800		
13	1800, F800		
14	800, F800		
15	800, E800		
16	1800, E800		



V.22 A/B 600 BPS



V.11 A/B AND BELL 212A 1200 BPS



V.22 bis 2400 BPS

5

Figure 23. Scaled Signal Points

Rockwell

R2424 and R1212 Modems Auto Dial and Tone Detection

by Jeffrey T. Higgins and Malcolm B. Waters, Product Applications Engineers
Semiconductor Products Division, Newport Beach, California

INTRODUCTION

The R2424 and R1212 modems provide auto dial and tone detection capabilities. These functions aid the designer in creating an intelligent modem subsystem. The auto dialer can be designed to dial both normally and in reverse fashion. Tone detection, a subset of an intelligent auto dialer, can provide call progress monitoring of ringback, busy, and answer tones. This application note presents examples of auto dial and tone detection routines and the problems they overcome.

R2424/R1212 AUTO DIALER

The auto dialer flowchart (Figure 1) shows the typical command flow to cause the modem to dial and then enter the tone detection state. The sequence shown assumes that the modem is in serial control (BUS bits = 0) and that the NEWC bits are set at the appropriate time.

To auto dial the $\overline{\text{DTR}}$ signal must be active. In a constant carrier application where $\overline{\text{RTS}}$ must be on before the end of the handshake, it is recommended that $\overline{\text{RTS}}$ be activated the first time $\overline{\text{DTR}}$ is active and then left on permanently. ($\overline{\text{RTS}}$ may also be hardwired to DTR for constant carrier applications.)

During the time the modem is initialized for auto dialing and the telephone number is being entered, both CRQ bits should be 0. After touch tone or pulse dialing is selected using the DTMF bit and the telephone number is entered, both CRQ bits should be set to a one.

Note:

The CRQ bit in the transmitter enables the auto dialer. The CRQ bit in the receiver enables tone detection when CRQ in the transmitter is enabled. If no tone detection is wanted, CRQ in the receiver does not have to be set.

Following a short delay to allow the relay to close, the DLO and TONE bit are checked. The DLO bit when active tells the user that the relay is closed. If the CRQ bit in the receiver is enabled, the TONE bit at this time will be a one signifying that dial tone is being detected. If both bits are active the actual dialing can begin.

First, the dial digit register is checked to see if it is empty. If it is, the first dial digit is taken from memory and examined. If it is a character that represents a delay then a delay occurs and the second dial digit is taken from memory. If it was not a delay character then it is loaded into the dial digit register. The modem will take the digit and dial it according to the state of the DTMF bit. (The DTMF bit can be changed during the dialing process to allow both tone and pulse dialing of consecutive digits.) The modem also accounts for interdigit delay. After the digit is dialed and the interdigit delay time has elapsed the DDRE bit will be a one signifying that the next digit can be loaded. The interdigit delay can be lengthened by not loading the dial digit register immediately after the DDRE bit is active. This process is continued until the last digit is dialed.

At this point the user can put the modem into data mode by loading $FF into the dial digit register (assuming the CRQ bit in the receiver is 0) or the tone detection routine can begin. If tone detection is desired, $FF should not be loaded at this time. The loading of $FF tells the modem to go into the data mode and start the 30 second abort timer. Once this action is taken the dialing process and tone detection is ended. CRQ in the transmitter must be a one during data mode or the modem will go on-hook. When $FF is loaded, CRQ in the receiver must be a zero.

ANSWER TONE DETECTION—NO RINGBACK

If tone detection is attempted, the software which determines the call progress status must be able to compensate for the many inconsistencies in the dial-up network. One of the problems is no ringback.

Since the tone detector in the modem has a passband from 345 to 635 Hz it is unable to detect answer tone if no ringback occurs. Figure 2 is a flowchart of a routine which switches back and forth between data mode and tone detection mode to catch answer tone if no ringback occurs. Figure 4 shows the worst case example of no ringback and the timing of the software routine which tries to keep the modem from missing the answer tone.

After the last digit is dialed, a 4.5 second watchdog timer is started. During this time the TONE bit is being monitored for call progress tones. If the TONE bit becomes active then the routine of Figure 3 is implemented. If the timer times out and no tone was detected the routine continues and looks for answer tone. (If the answer sequence started immediately after the last digit was dialed then approximately 500 milliseconds of answer tone would remain. This is enough time for the originating modem to detect answer tone.) CRQ in the receiver is reset to zero and $FF is loaded into the dial digit register. This action puts both the transmitter and receiver in data mode. The receiver can now detect answer tone. A 750 ms watchdog timer is started. The DSR bit is monitored during this time. If DSR becomes active then answer tone was detected and the modem will continue with the handshake. If the timer times out and DSR is not active the program can exit and abort the call (depending on how many tries are desired for tone detection) or it can go back into tone detection looking for call progress tones.

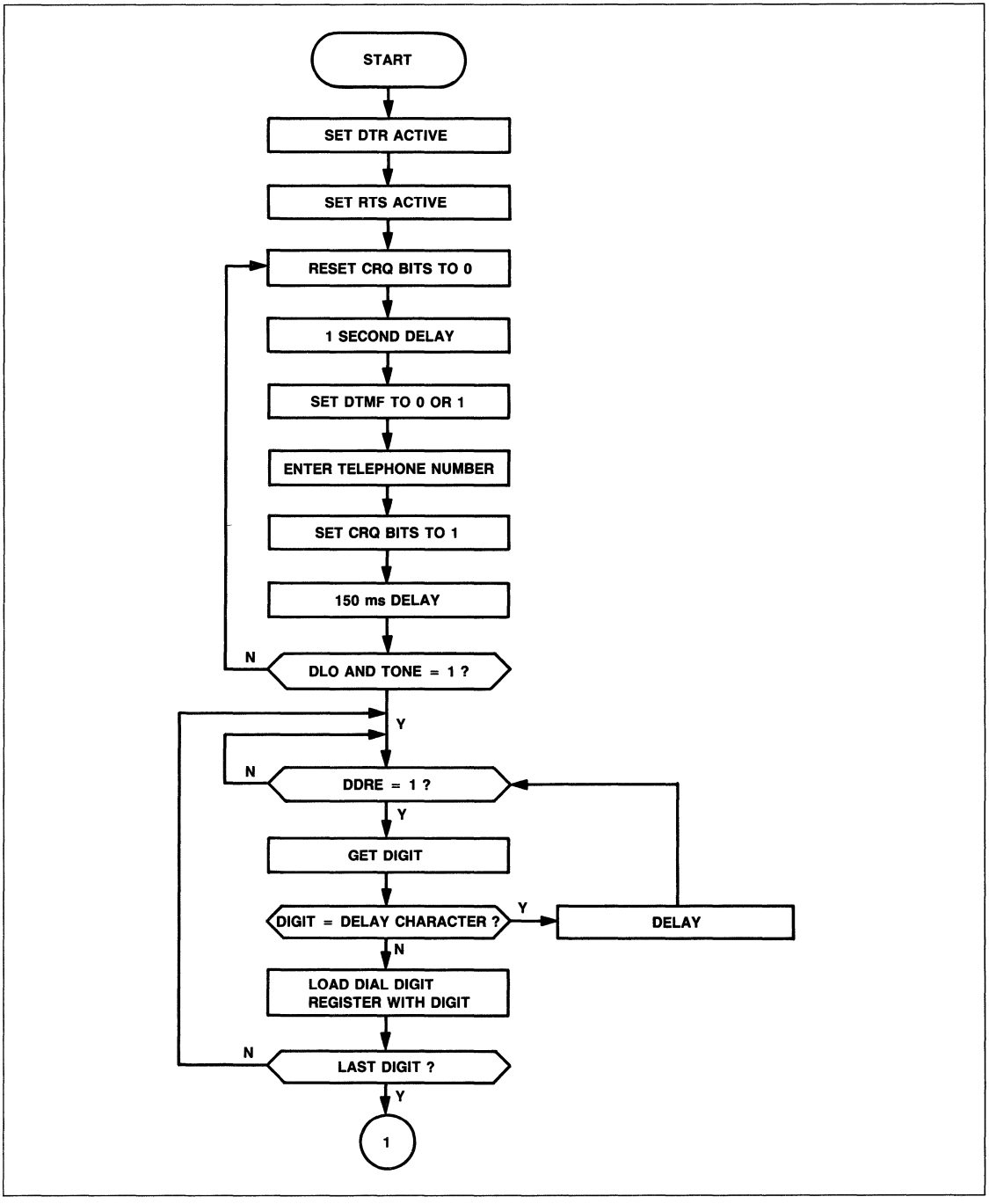


Figure 1. R1212 and R2424 Auto Dial Routine

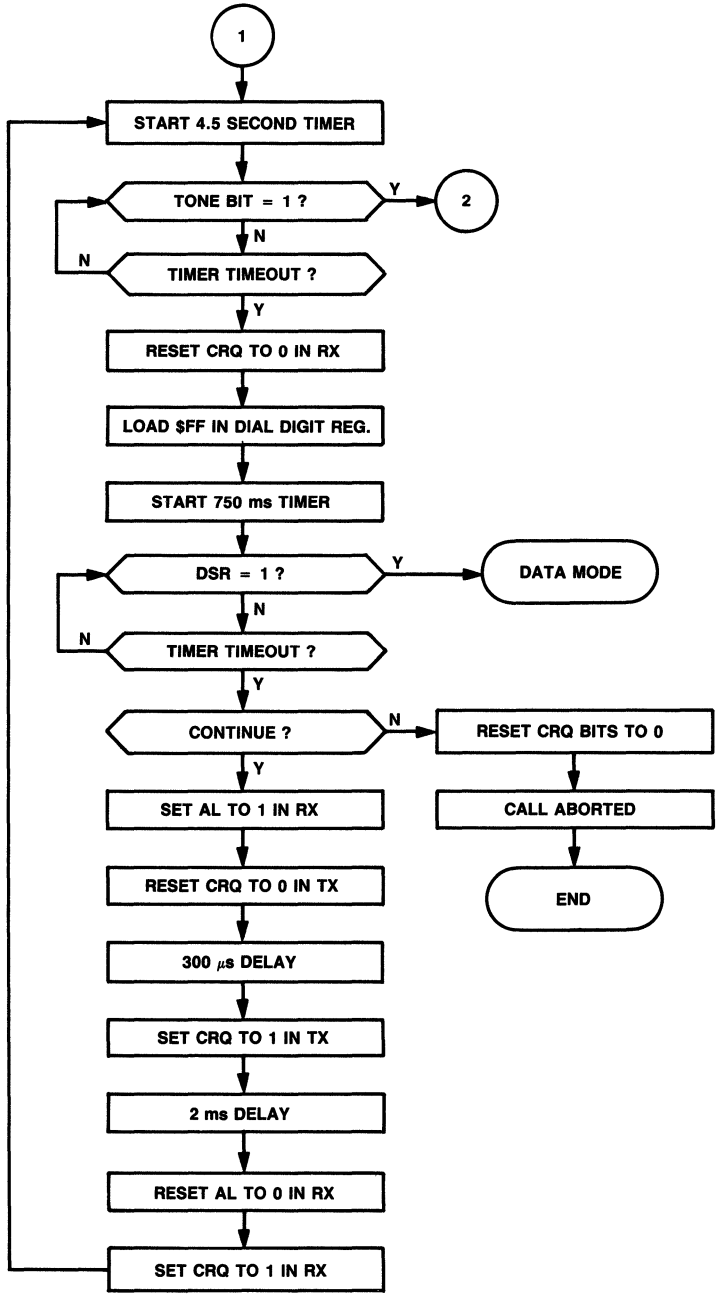


Figure 2. Answer Tone Detection When No Ringback Occurs

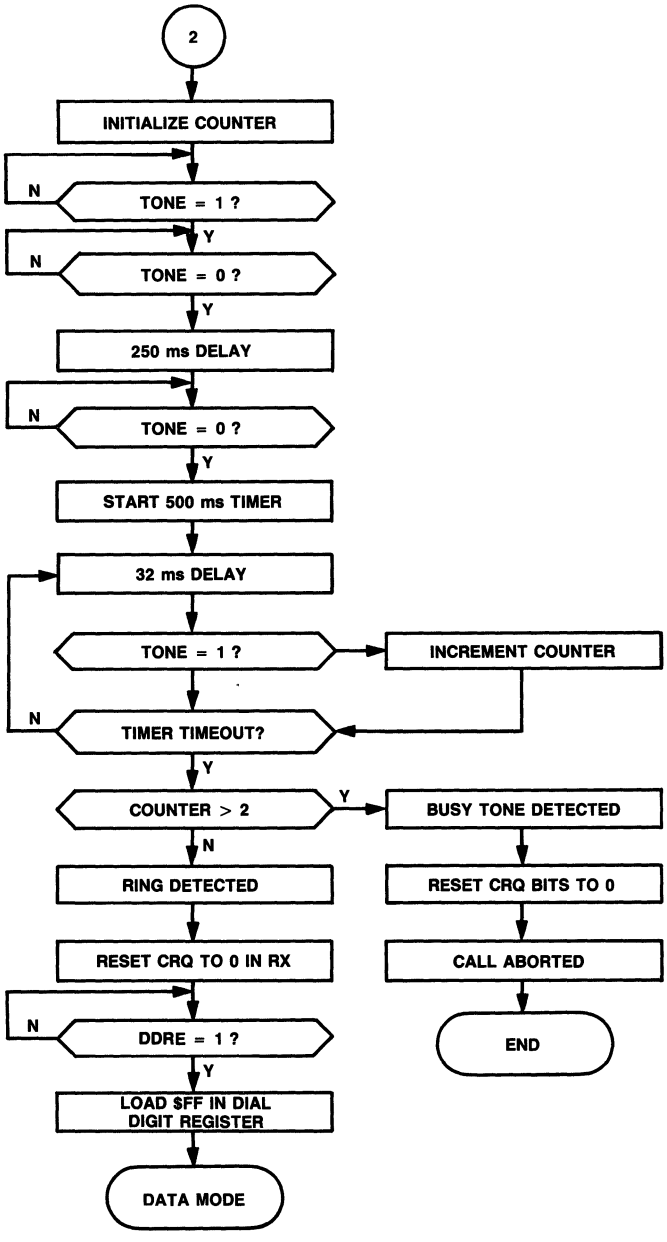


Figure 3. Call Progress Detection of Ringback and Busy Tones

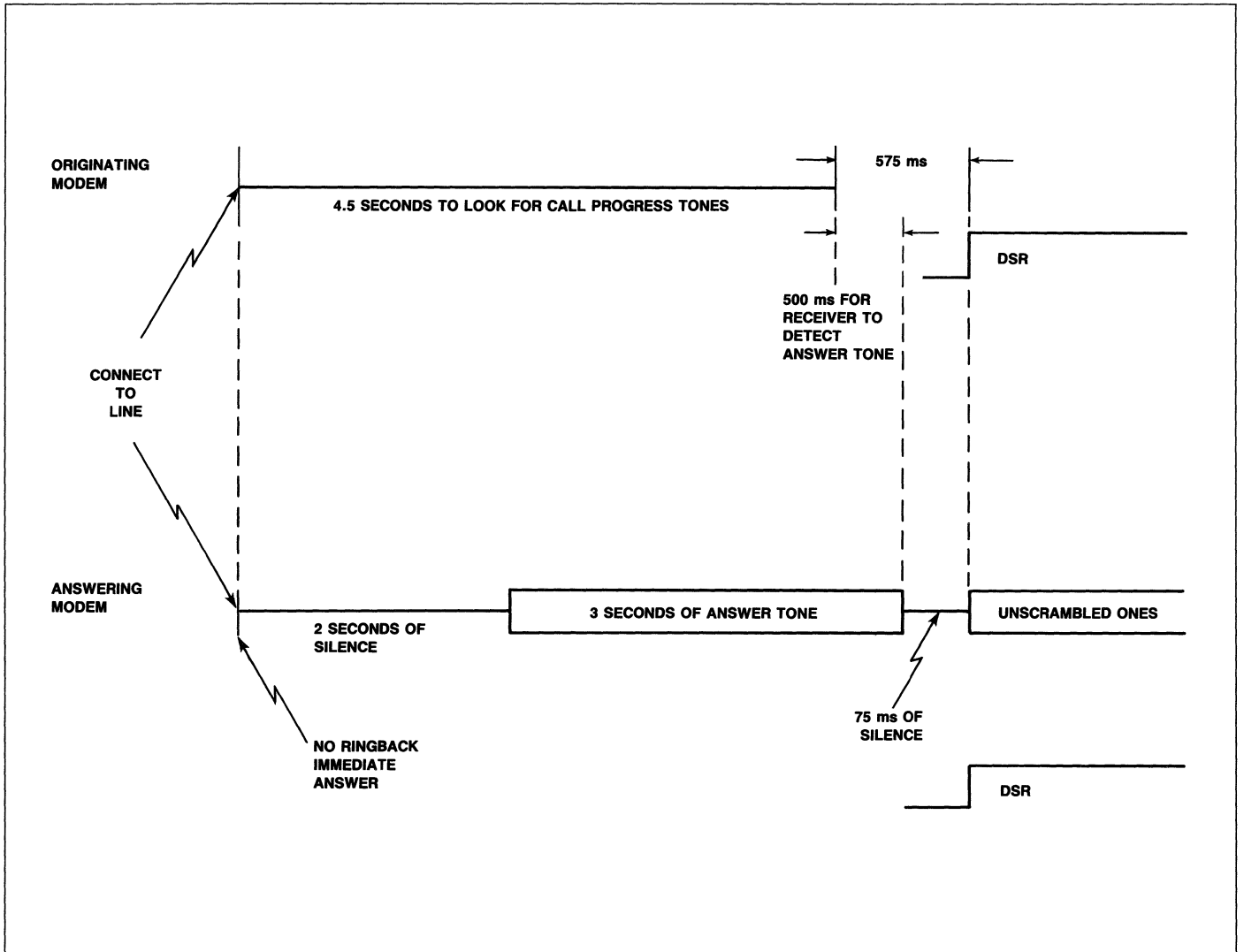


Figure 4. Worst Case Tone Detection Example: No Ringback, Immediate Answer

If it is desired to go back into the tone detect mode, the following sequence must be followed. Set the AL bit in the receiver to a one. Reset CRQ in the transmitter to a zero and after 2 sample times (approximately 300 microseconds) set CRQ in the transmitter to a one. This action resets the transmitter, without opening the relay. One baud time later (approximately 2 ms) reset AL in the receiver to a zero. (Although setting and resetting the AL bit in the receiver does not seem to make sense, it does help to ensure internal flags are properly set so the modem does not lock-up by switching back and forth between data and tone detect mode. After AL in the receiver is reset, set CRQ in the receiver to a one. At this point the modem is back in tone detect mode and the routine begins again.

If after a number of passes through the routine no call progress or answer tones have been detected, the call can be aborted by resetting both CRQ bits to a zero.

CALL PROGRESS DETECTION

If the TONE bit becomes active during the 4.5 second period of Figure 2, the call progress tone detection routine of Figure 3 should be implemented. This routine monitors the duty cycle of the TONE bit and reports what tone is being detected.

The difficulty with any tone detection routine is the fact that the tones provided by the telephone network are not always according to specification. Figure 5 shows both ideal and nonideal tone detection situations. It is the nonideal tones that create the timing problems in the tone detection routine, and those situations must be dealt with. The routine of Figure 3 provides a possible solution to catch the nonideal call progress tones.

The call progress detection routine makes its decisions after the on-to-off period of any tone. After a 250 ms delay the TONE bit is monitored for 500 ms. During this time samples of the TONE bit are taken every 32 ms (see Figure 6). If the TONE bit is active when sampled, a counter is incremented. If the counter was incremented more than two times it is assumed that a busy tone was detected. CRQ should then be reset in both the transmitter and receiver to zero. This puts the modem back on-hook and the call is aborted. If the counter was incremented two times or less a ring was detected and the modem must go into data mode. This is accomplished by resetting CRQ in the receiver to zero and loading $FF into the dial digit register.

Note:

It is assumed that the answering modem will answer after one ring. Therefore, the tone detection routine must decide the call progress status before the remote modem answers.

R2424/R1212 REVERSE AUTO DIALER

The R2424 and R1212 can be used to call an originate-only modem. This application provides a higher level of security in dial-up environments. With the increasing problem of data security in dial-up computer systems it is necessary to prevent unauthorized users from connecting to the network. Reverse auto dialing helps solve the problem.

The central site modem would be set up to monitor a ringing signal, but would be configured for originate mode. The remote modem would dial, switch to the answer mode and send the answering sequence. The central site would answer the call and detect answer tone as though it had originated the call. The handshake would then proceed as normal.

If an authorized modem which was not configured to send answertone after dialing, tried to connect, the central site modem would not respond after answering, because it would be expecting answer tone.

The reverse auto dialer flowchart (Figure 7) shows the command flow to cause the modem to dial and then enter the answer state and send answer tone. The sequence shown assumes that the modem is in parallel control (BUS bits = 1) and that the NEWC bits are set at the appropriate time.

The routine initializes the modem and prepares it for dialing. The ORG bit is set to a zero (manual answer) but is ignored during the dialing process. The dialing is identical to Figure 1 except that CRQ in the receiver is not set to a one. No tone detection can be done with the reverse dialing because CRQ in the transmitter is disabled after the last digit is dialed. After CRQ in the transmitter is reset to a zero the DATA bit is immediately set to a one. Since the ORG bit was set previously, the result is the OH relay stays closed, the modem switches from originate to answer configuration, and the answer sequence is transmitted according to the specification of the modem configuration.

The modem will send the answering sequence for 30 seconds or until the other modem responds.

R2424/R1212 REVERSE AUTO ANSWER

The R2424 and R1212 provides the capability to auto answer in the originate configuration. This feature complements the reverse auto dialing described previously.

The flowchart of Figure 8 shows the method to perform the reverse auto answering. The sequence shown assumes that the modem is in parallel control (BUS bits = 1) and that the NEWC bits are set at the appropriate time.

The ORG bit is set to a one, configuring the modem to originate. On detection of the ring using the RI bit, the DATA bit is set to a 1. This sequence causes the modem to answer, but remain in the originate mode looking for the answer sequence.

A more comprehensive description of R1212/R2424 modem operation is contained in Section 4 of the Modem Interface Guide (Order No. 685)

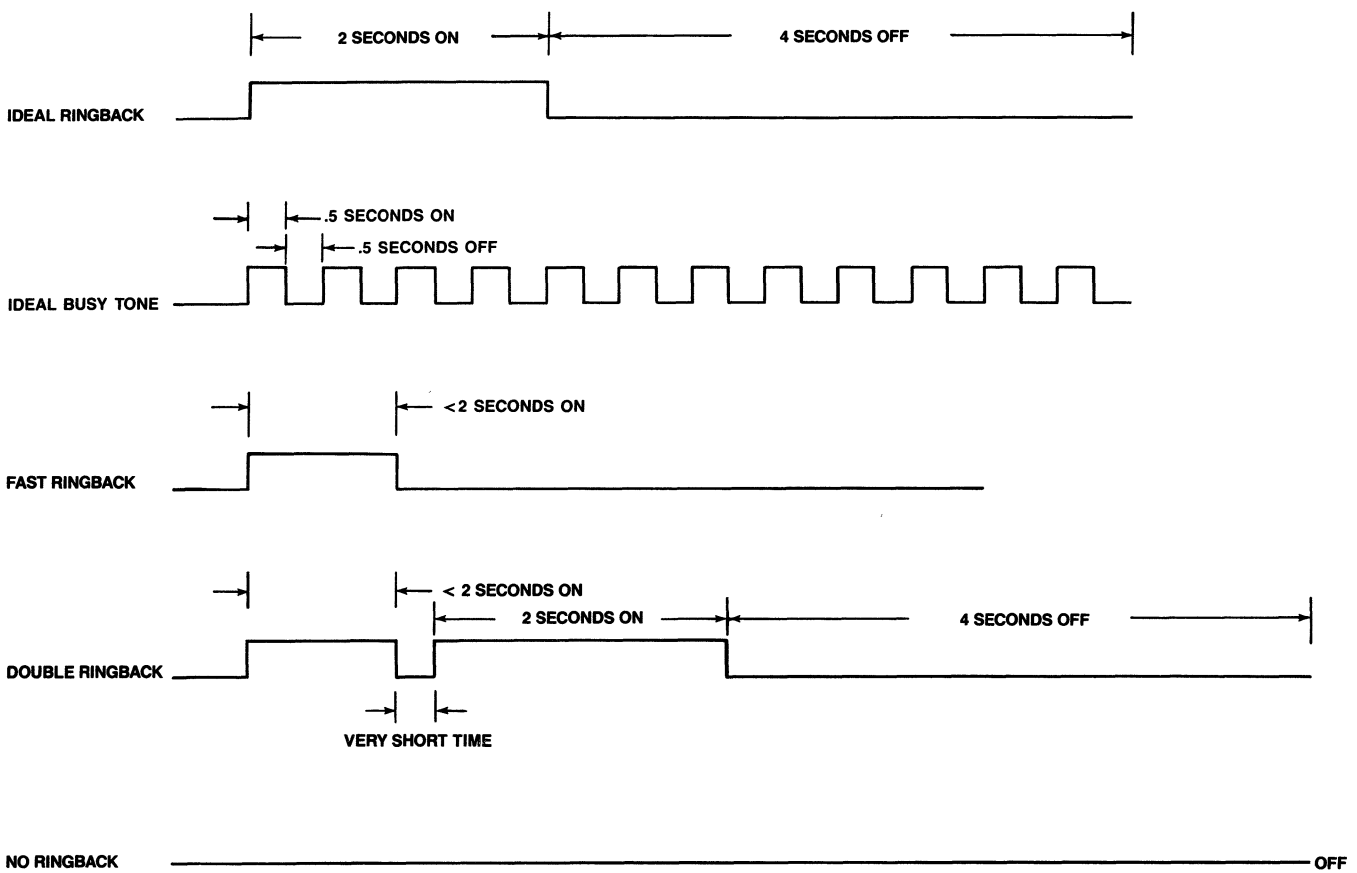


Figure 5. Call Progress Tones Timing Problems

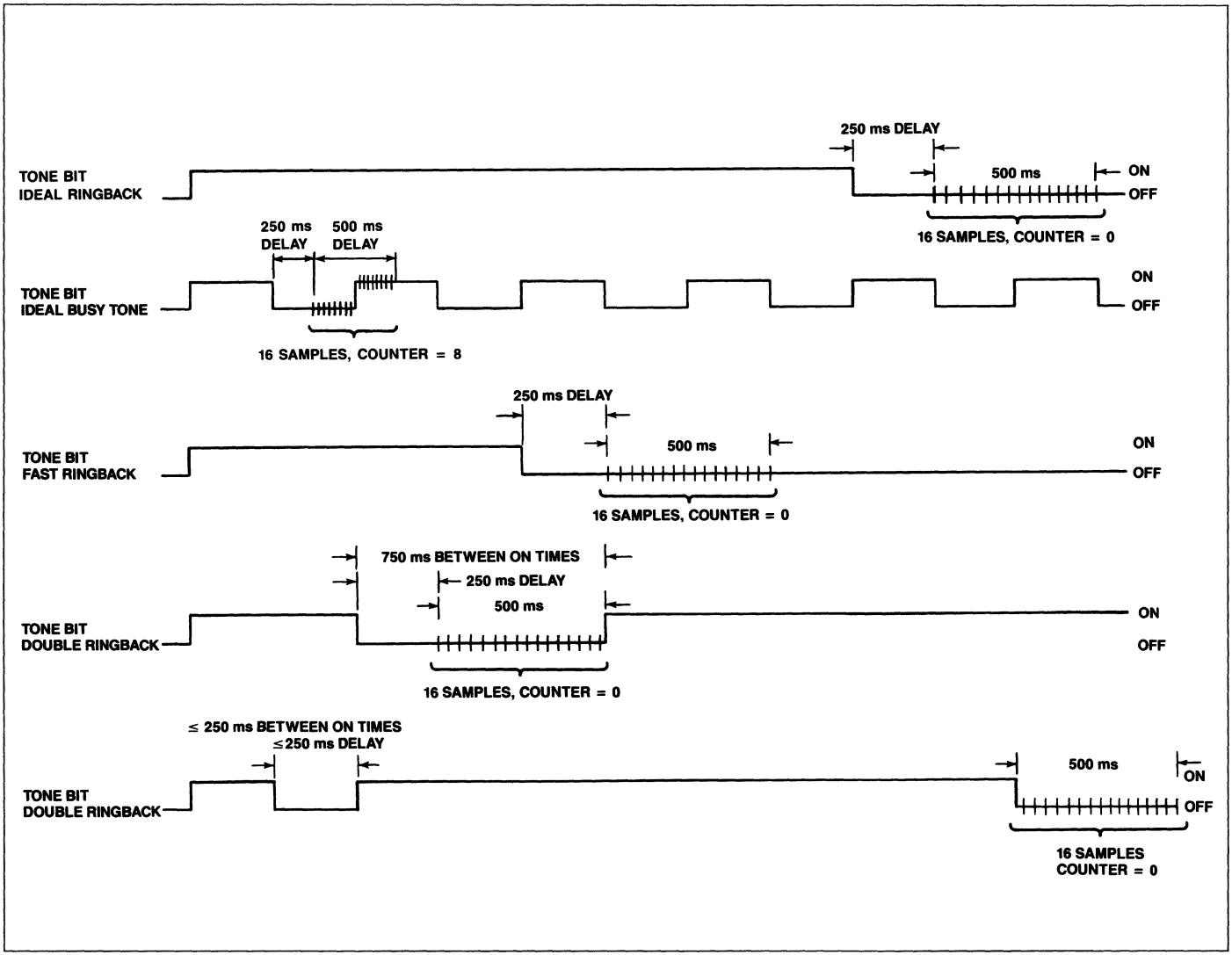


Figure 6. Timing for Call Progress Tone Detection Routine

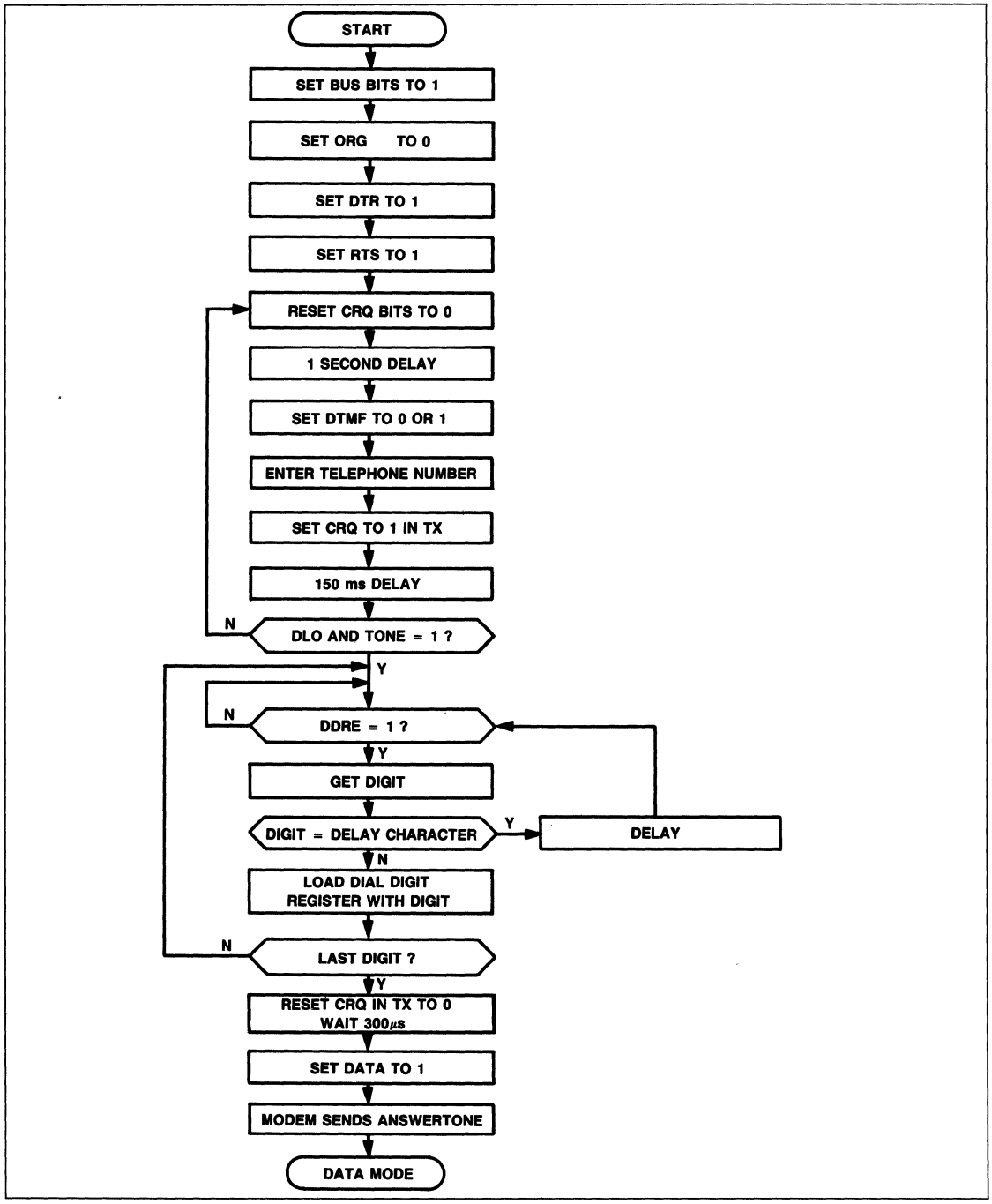


Figure 7. R1212 and R2424 Reverse Auto-Dial Routine

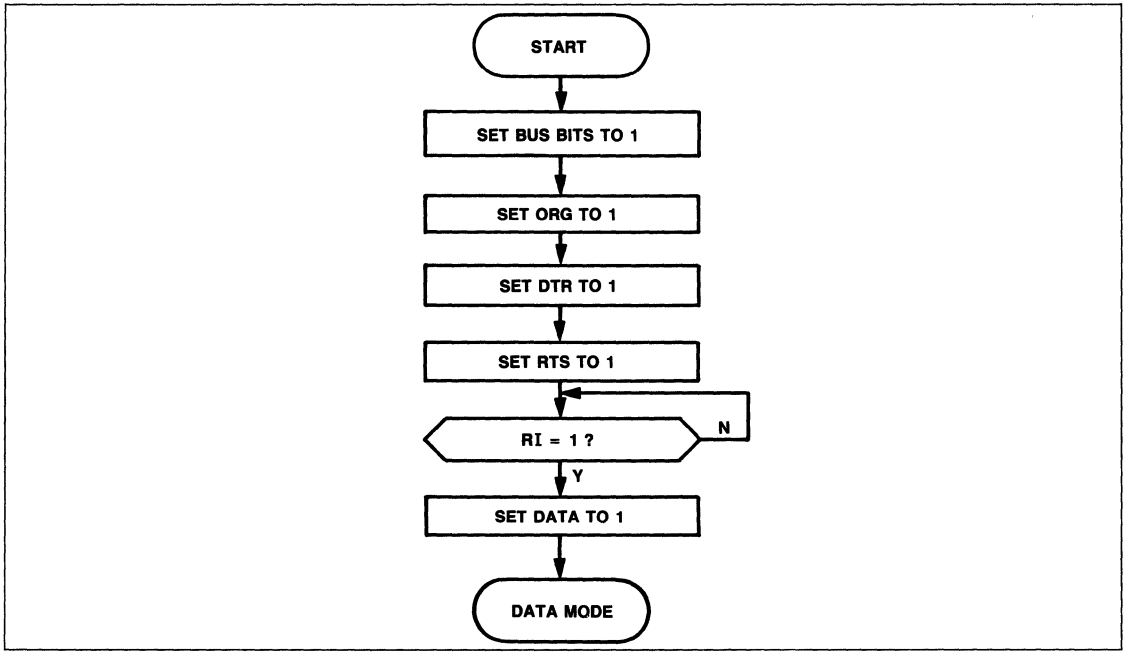


Figure 8. R1212 and R2424 Reverse Auto Answer

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Rockwell

8088 Microprocessor to R1212/R2424 Modem Interface

INTRODUCTION

This application note details the connections and circuitry needed to interface a Rockwell R1212 1200 BPS or R2424 2400 BPS Full-Duplex Modem to an 8088 microprocessor-based system. Also included is an assembly language level computer program that performs an auto dialer function.

8088 INTERFACE

The basic interface signals between an R1212/R2424 and an 8088-based system are summarized in Figure 1. A schematic detailing the components and connections necessary to interface an R1212/R2424 modem to an expansion slot in an IBM PC (or equivalent) personal computer is shown in Figure 2. This particular circuit was used with a COMPAQ Personal Computer but should be able to be used with an IBM PC or other compatible computer with little or no modification.

The R1212/R2424 modem is mapped into the memory space allocated for the prototype board in the IBM PC input/output map. The chip select logic places the modem in the following address space:

Chip Select Line	Address Range
$\overline{CS0}$	$300-$30F
$\overline{CS1}$	$310-$31F

The INS8250 UART provides the asynchronous communications between the R1212/R2424 modem and the 8-bit microprocessor data bus.

AUTO DIALER SOFTWARE

The 8088 assembly language instructions (and assembled hmachine code that performs an auto dialer function is listed starting on page 3.

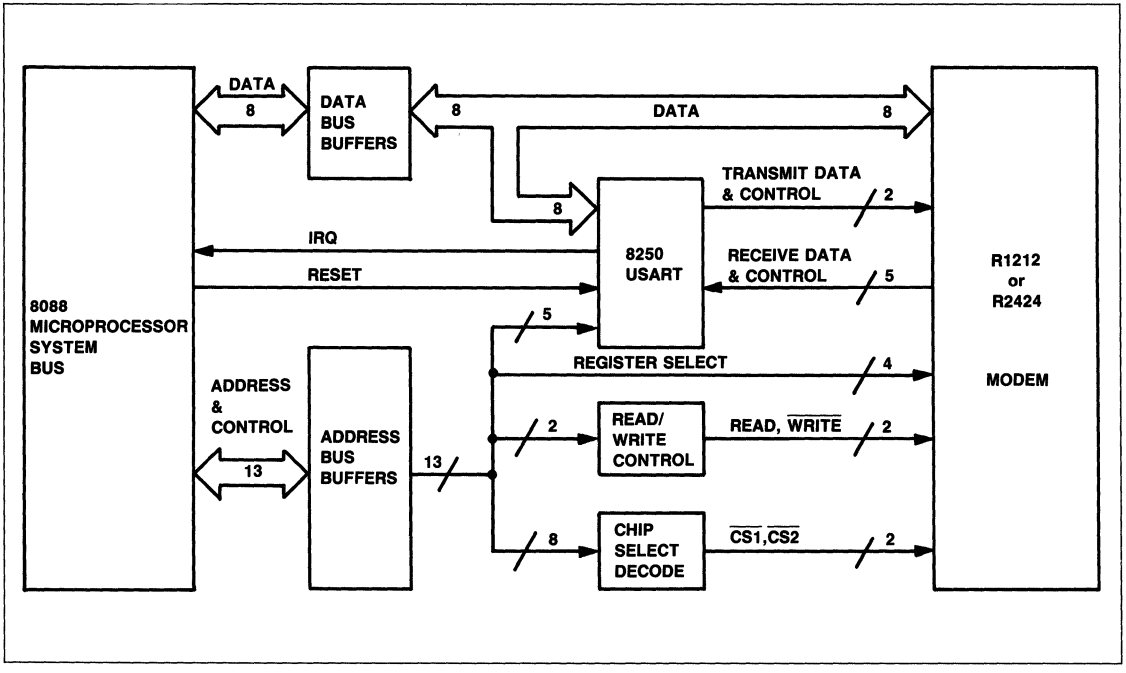


Figure 1. IBM PC to R1212/R2424 Modem Interface

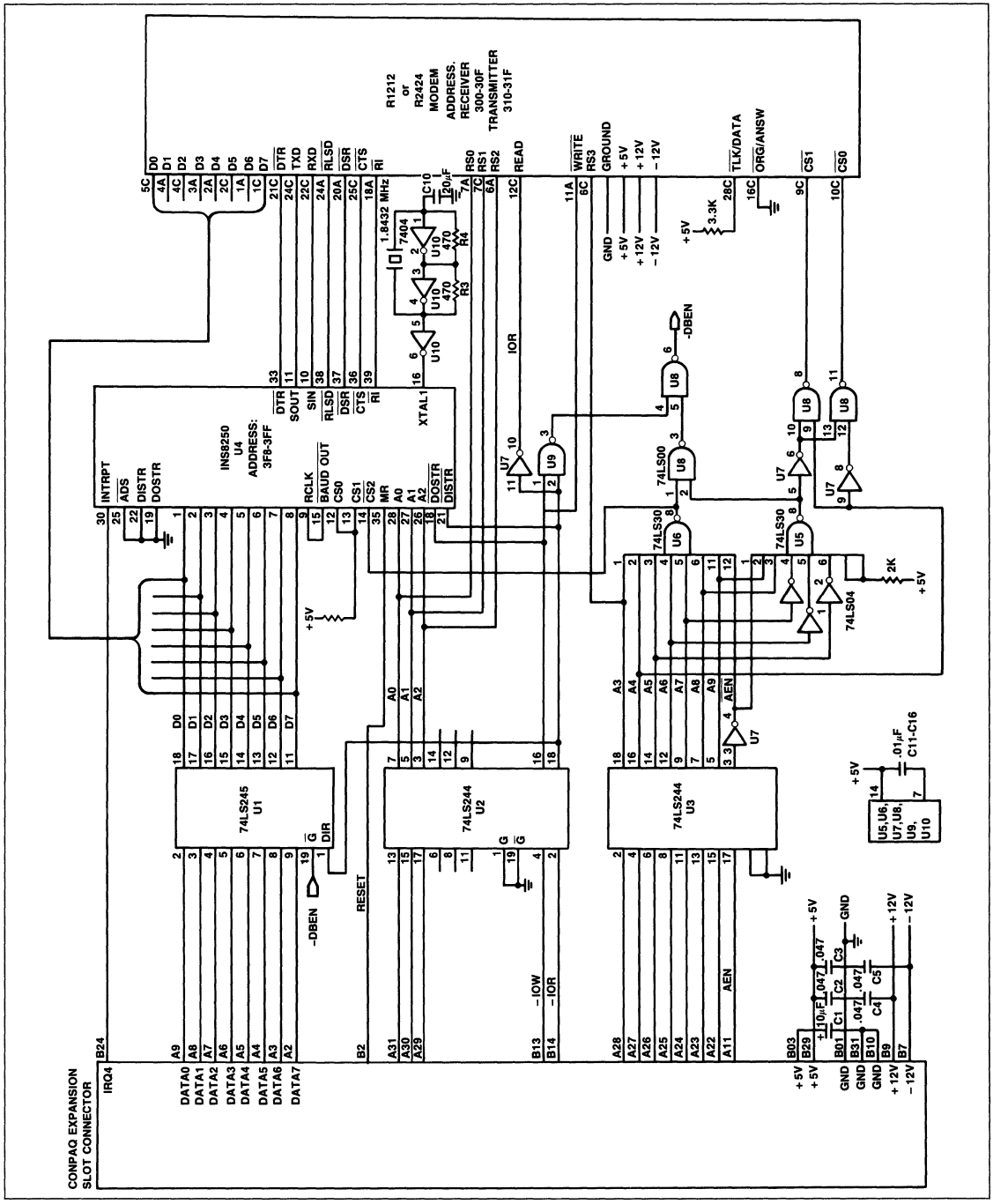


Figure 2. IBM PC to R1212/R2424 Modem Schematic

8088 AUTO DIALER ASSEMBLY LISTING

```
                                TITLE   8088 AUTO DIALER (DIAL1.ASM)
                                COMMENT*

                                        Rockwell Applications Lab 5/15/84

                                        This is written as an example of an auto-dialer in 8088
                                        Assembly Language.  It was written using the Microsoft
                                        Macro Assembler which runs under the IBM Disk Operating
                                        System.

                                        The hardware used places the interface memory Bank 0
                                        and Bank 1 at locations 300-30F and 310-31F respectively.
                                        This is the space allocated for the Prototype Card in the
                                        IBM I/O Address Map.
                                *
                                ;
                                ;Macro pseudo-op for use in setting req bits in the interface memory
                                ;
                                ;The address and bit to be set/reset is sent to the Macro.
                                ;The Macro then gets the appropriate byte from the R1224.
                                ;This byte is ORed with the bit to be set to change only that
                                ;bit.  The byte is then sent back to the R1224.
                                ;
                                SET     MACRO   ADDR,BIT
                                        MOV     DX,ADDR
                                        IN      AL,DX
                                        OR      AL,BIT
                                        OUT     DX,AL
                                        ENDM
                                ;
                                ;
0000                            STACK   SEGMENT STACK
0000  0100 [                            DB      256     DUP (?)
            ??
                ]

0100                            STACK   ENDS
                                ;
0000                            DATA    SEGMENT
0000  14 15 [                   BUF     DB      20,21 DUP(0)    ;Set up a buffer for the phone number
            00
                ]

0016  20 45 4E 54 45 52         MSG     DB      ' ENTER PHONE NUMBER:$ '
      20 50 48 4F 4E 45
      20 4E 55 4D 42 45
      52 3A 24 20
002C  20 20 44 49 41 4C         MES1    DB      '  DIALING $ '
      49 4E 47 20 24 20
003B                            DATA    ENDS
                                ;
0000                            CODE    SEGMENT
0000                            START   PROC    FAR
                                ;
                                ;Standard Program Prologue
                                ;
                                        ASSUME  CS:CODE,DS:DATA,SS:STACK
0000  1E                                PUSH    DS
0001  B8 0000                          MOV     AX,0
0004  50                                PUSH    AX
0005  B8  ---- R                       MOV     BX,DATA ;Get data segment base address
0008  8E DB                             MOV     DS,BX
000A  E8 000E R                         CALL    MAIN
000D  CB                                RET
000E                            START   ENDP
```

8088 AUTO DIALER ASSEMBLY LISTING (Continued)

```
                                ;
000E                            MAIN    PROC NEAR
                                ;
                                ;Dial set-up
                                ;
                                        SET     31DH,00H        ;Assure that DTR is a 0
000E  BA 031D                   +       MOV     DX,31DH
0011  EC                        +       IN      AL,DX
0012  0C 00                     +       OR      AL,00H
0014  EE                        +       OUT     DX,AL
                                        SET     31EH,08H        ;Set NEWC
0015  BA 031E                   +       MOV     DX,31EH
0018  EC                        +       IN      AL,DX
0019  0C 08                     +       OR      AL,08H
001B  EE                        +       OUT     DX,AL
                                ;
                                        SET     30DH,80H        ;Set the BUS bit, receiver
001C  BA 030D                   +       MOV     DX,30DH
001F  EC                        +       IN      AL,DX
0020  0C 80                     +       OR      AL,80H
0022  EE                        +       OUT     DX,AL
                                ;
                                        SET     31DH,80H        ;Set the BUS bit, transmitter
0023  BA 031D                   +       MOV     DX,31DH
0026  EC                        +       IN      AL,DX
0027  0C 80                     +       OR      AL,80H
0029  EE                        +       OUT     DX,AL
                                ;
                                        SET     31BH,02H        ;Set DTMF for tone dialing
002A  BA 031B                   +       MOV     DX,31BH
002D  EC                        +       IN      AL,DX
002E  0C 02                     +       OR      AL,02H
0030  EE                        +       OUT     DX,AL
                                ;
                                        SET     30DH,40H        ;Set CRQ bit, receiver
0031  BA 030D                   +       MOV     DX,30DH
0034  EC                        +       IN      AL,DX
0035  0C 40                     +       OR      AL,40H
0037  EE                        +       OUT     DX,AL
                                ;
                                        SET     31DH,40H        ;Set CRQ bit, transmitter
003B  BA 031D                   +       MOV     DX,31DH
003B  EC                        +       IN      AL,DX
003C  0C 40                     +       OR      AL,40H
003E  EE                        +       OUT     DX,AL
                                ;
                                ;Wait at least 50 msec between reset and set of DTR
                                ;
003F  B3 FF                             MOV     BL,0FFH
0041  FE CB                     TIME1:  DEC     BL
0043  80 FB 00                         CMP     BL,00H
0046  75 F9                             JNZ     TIME1
                                ;
                                        SET     31DH,08H        ;Set DTR
0048  BA 031D                   +       MOV     DX,31DH
004B  EC                        +       IN      AL,DX
004C  0C 08                     +       OR      AL,08H
004E  EE                        +       OUT     DX,AL
                                ;
                                        SET     30EH,08H        ;Set NEWC, Receiver
004F  BA 030E                   +       MOV     DX,30EH
0052  EC                        +       IN      AL,DX
0053  0C 08                     +       OR      AL,08H
0055  EE                        +       OUT     DX,AL
                                        SET     31EH,08H        ;Set NEWC bit, Transmitter
0056  BA 031E                   +       MOV     DX,31EH
0059  EC                        +       IN      AL,DX
005A  0C 08                     +       OR      AL,08H
005C  EE                        +       OUT     DX,AL
                                ;
                                ;Check that we are off-hook and ready to dial
                                ;
005D  BA 0318                   WAIT:   MOV     DX,318H
0060  EC                               IN      AL,DX
0061  24 80                            AND     AL,80H
0063  3C 80                            CMP     AL,80H          ;Check to see if DLO is set
0065  75 F6                            JNZ     WAIT            ;If not, wait for it
```

8088 AUTO DIALER ASSEMBLY LISTING (Continued)

```
                                ;Wait for dial-tone on the line
                                ;
0067  BA 0308                           MOV     DX,308H
006A  EC                                IN      AL,DX
006B  24 80                             AND     AL,80H
006D  3C 80                             CMP     AL,80H
006F  75 EC                             JNZ     WAIT
                                ;
0071  B4 09                             MOV     AH,9
0073  BA 0016 R                         MOV     DX,OFFSET MSG   ;Print prompt for phone # input
0076  CD 21                             INT     21H
                                ;
                                ; Read the number and display it.
                                ;
0078  B4 0A                             MOV     AH,0AH
007A  BA 0000 R                         MOV     DX,OFFSET BUF   ;Buffered Keyboard Input
007D  CD 21                             INT     21H
                                ;
007F  B2 0A                             MOV     DL,0AH          ;Line feed
0081  B4 02                             MOV     AH,02           ;Display function
0083  CD 21                             INT     21H             ;DOS call
                                ;
0085  B4 09                             MOV     AH,9
0087  BA 002C R                         MOV     DX,OFFSET MES1  ;Print DIALING message
008A  CD 21                             INT     21H
                                ;
                                ; Loop and redisplay telephone number as it is dialed
                                ;
008C  BE 0000                           MOV     SI,0
008F  B9 0000                           MOV     CX,0
0092  8A 0E 0001 R                      MOV     CL,BUF+1        ;Get number of digits read
0096  8A 94 0002 R              PAD:    MOV     DL,BUF[SI+2]
                                ;DL now contains the dial digit
009A  52                                PUSH    DX      ;Preserve the dial digit on the stack
                                ;
                                ;Check to see that the dial digit register is empty
                                ;
009B  BA 031E                   FULL1:  MOV     DX,31EH
009E  EC                                IN      AL,DX
009F  24 01                             AND     AL,01H
00A1  3C 01                             CMP     AL,01H
00A3  75 F6                             JNZ     FULL1
                                ;
                                ;Get the dial digit off the stack
                                ;
00A5  5A                                POP     DX
                                ;
                                ;Check to see if it's a carriage return
                                ;
00A6  80 FA 0D                          CMP     DL,0DH
00A9  74 10                             JZ      DONE            ;If it is, end the dialing sequence
                                ;
                                ;Feedback for dialing
                                ;
00AB  B4 02                             MOV     AH,2            ;Print the digits as they are dialed
00AD  CD 21                             INT     21H
                                ;
                                ;Send the dial digit to the R1224
                                ;
00AF  80 E2 0F                          AND     DL,0FH
00B2  8A C2                             MOV     AL,DL           ;Dial Digit must be in AL to be sent
00B4  BA 0310                           MOV     DX,310H         ;to the I/O port
00B7  EE                                OUT     DX,AL           ;Send it
00B8  46                                INC     SI              ;Point to the next digit
00B9  E2 DB                             LOOP    PAD
                                ;
                                ;Go here to end the dial sequence by putting FF
                                ;into the dial digit register
                                ;
                                ;Assure DDRE empty again
                                ;
00BB  BA 031E                   DONE:   MOV     DX,31EH
00BE  EC                                IN      AL,DX
00BF  24 01                             AND     AL,01H
00C1  3C 01                             CMP     AL,01H
00C3  75 F6                             JNZ     DONE
                                ;
00C5  BA 0310                           MOV     DX,310H
00C8  B0 FF                             MOV     AL,0FFH
00CA  EE                                OUT     DX,AL
                                ;
00CB  C3                                RET
00CC                            MAIN    ENDP
00CC                            CODE    ENDS
                                END     START
```

Rockwell

High Speed Modems
Filter Characteristics

INTRODUCTION

The R96F, R96DP, R48DP, and R96FT modems include integrated analog devices using switched capacitor filters to perform the functions of receiver input bandpass filtering, transmitter output lowpass filtering, and compromise equalization. Differences in performance result from half-duplex (HDX) or full-duplex (FDX) versions of the integrated analog device.

R96 FILTERS

The following tables illustrate the response of the receiver input bandpass and transmitter output low pass filters without compromise equalization.

A. Receiver Input Bandpass Filter

Parameter	Value
Test signal range	0 dBm to −45 dBm
Passband	400 Hz – 3000 Hz
Passband ripple	0.5 dB max.
Loss below 60 Hz	40 dB min.
Loss above 6000 Hz	40 dB min.
Passband gain	0.0 dB ±1.0 dB
Delay distortion 400 Hz – 1800 Hz	Less than 1000 usec
Delay distortion 1800 Hz – 3000 Hz	Less than 150 usec

B. Transmitter Output Lowpass Filter

Parameter	Value
Test signal	0 dBm to −16 dBm
Passband	400 – 3000 Hz
Passband Gain	−1 dB ±1 dB
Passband ripple	0.5 dB max.
Loss at 3600 Hz	5.5 dB min.
Loss at 7800 Hz	32 dB min.
Loss at 11400 Hz	33.5 dB min.
Loss at 12000 Hz	41 dB min.
Loss above 17400 Hz	45 dB min.
Delay distortion 400 – 3000 Hz	Less than 300 usec

The following tables illustrate the change in filter response caused by enabling each of the compromise equalizers independently.

A. Receiver

1. Link Amplitude Equalizer HDX and FDX.

Frequency Hz	Gain dB Relative to 1700 Hz	
	US Long	Japanese 3 Link
1000	−0.27	−0.13
1400	−0.16	−0.08
2000	+0.33	+0.16
2400	+1.54	+0.73
2800	+5.98	+2.61
3000	+8.65	+3.43

2. Link Delay Equalizer FDX Only.

Frequency Hz	Delay Microseconds Relative to 1700 Hz	
	US Long	Japanese 3 Link
800	−498.1	−653.1
1200	−188.3	−398.5
1600	− 15.1	− 30.0
1700	+ 0.0	+ 0.0
2000	− 39.8	+ 11.7
2400	−423.1	−117.1
2800	−672.4	−546.3

3. Cable amplitude HDX and FDX.

a. CODE 1

Frequency Hz	Gain dB Relative to 1700 Hz	
	HDX	FDX
700	−0.99	−0.94
1500	−0.20	−0.24
2000	+0.15	+0.31
3000	+1.43	+1.49

5

b. CODE 2

Frequency Hz	Gain dB Relative to 1700 Hz	
	HDX	FDX
700	−2.39	−2.67
1500	−0.65	−0.74
2000	+0.87	+1.02
3000	+3.06	+3.17

c. CODE 3

Frequency Hz	Gain dB Relative to 1700 Hz	
	HDX	FDX
700	−3.93	−3.98
1500	−1.22	−1.20
2000	+1.90	+1.81
3000	+4.58	+4.38

B. Transmitter

1. Link Amplitude Equalizer HDX Only.

Frequency Hz	Gain dB Relative to 1700 Hz	
	US Long	Japanese 3 Link
1000	−0.27	−0.13
1400	−0.16	−0.08
2000	+0.33	+0.16
2400	+1.54	+0.73
2800	+5.98	+2.61
3000	+8.65	+3.43

2. Cable Amplitude HDX and FDX.

a. CODE 1

Frequency Hz	Gain dB Relative to 1700 Hz
700	−0.99
1500	−0.20
2000	+0.15
3000	+1.43

b. CODE 2

Frequency Hz	Gain dB Relative to 1700 Hz
700	−2.39
1500	−0.65
2000	+0.87
3000	+3.06

c. CODE 3

Frequency Hz	Gain dB Relative to 1700 Hz
700	−3.93
1500	−1.22
2000	+1.90
3000	+4.58

Rockwell

R96F Modem
Tone Detector Filter Tuning

INTRODUCTION

The Rockwell R96F modem includes three independent tone detectors (F1, F2 and F3). These tone detectors are operational when the modem is configured for V.21 FSK, and are centered, upon power-up, to 2100 Hz (F1), 1100 Hz (F2), and 462 Hz (F3). This application note presents a method of tuning these detectors to any desired frequency in the 300 Hz – 3 kHz band.

COMPUTATION OF TONE DETECTOR COEFFICIENTS

Each tone detector consists of two second-order filters in cascade, an energy averaging filter, and a threshold comparator. A diagram of the tone detector is shown in Figure 1.

Filter 1 has a transfer function:

$$H_1(Z) = \frac{2\alpha}{1 - 2\beta_1 Z^{-1} - 2\beta_2 Z^{-2}} \qquad \text{(Eq. 1)}$$

Filter 2 has a transfer function:

$$H_2(Z) = \frac{2\alpha'}{1 - 2\beta_1' Z^{-1} - 2\beta_2' Z^{-2}} \qquad \text{(Eq. 2)}$$

The energy averaging filter has a transfer function:

$$H_3(Z) = \frac{\alpha''}{1 - \beta'' Z^{-1}} \qquad \text{(Eq. 3)}$$

The output of the energy averager is fed to a threshold comparator which sets, or resets, the appropriate bit (F1, F2 and F3) in the signal processor (SP) scratchpad memory if the energy output is equal to or greater than 1/8, or less than 1/8, respectively.

Filters 1 and 2 have a typical frequency response as shown in Figure 2. When cascaded, they form a bandpass filter with a narrow bandwidth as shown in Figure 3.

Given the transfer functions $H_1(Z)$ and $H_2(Z)$, an analytical method is required to compute their coefficients for any desired frequency in the 300 Hz – 3 kHz band. First, consider $H_1(Z)$. This transfer function can be rewritten as:

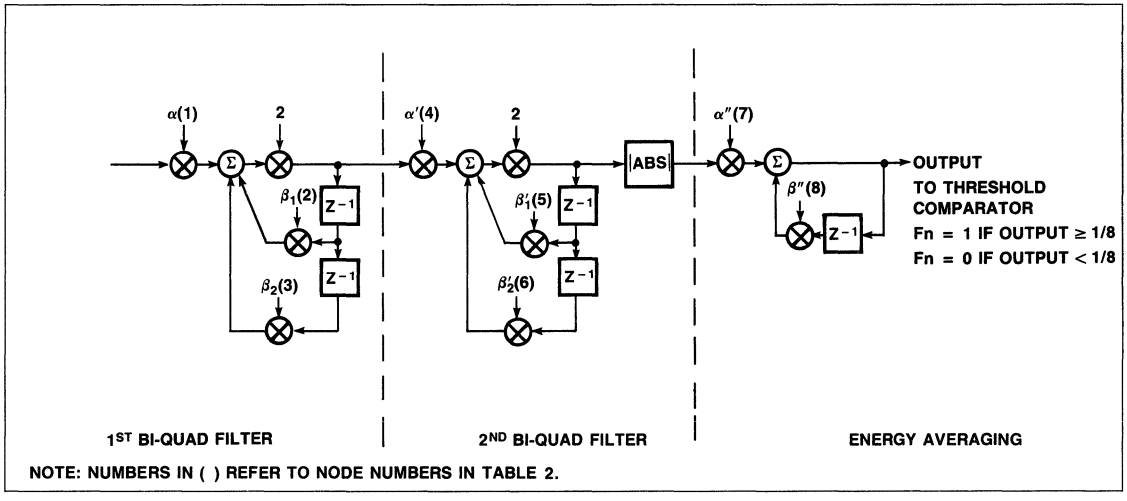
$$H_1(Z) = \frac{2\alpha Z^2}{Z^2 - 2\beta_1 Z - 2\beta_2} \qquad \text{(Eq. 4)}$$

which has a conjugate pair of poles:

$$P_1 = \beta_1 + j\sqrt{\beta_1^2 + 2\beta_2}$$

and

$$P_2 = \beta_1 - j\sqrt{\beta_1^2 + 2\beta_2}$$



NOTE: NUMBERS IN ( ) REFER TO NODE NUMBERS IN TABLE 2.

Figure 1. R96F Tone Detector Diagram

These poles lie on a circle of radius 0.994030884 on the Z-plane. The radius of the tone detector circle was chosen so that each filter has a high Q without being unstable (i.e., poles must lie inside the unit circle for stability). Figure 4 shows a Z-plane pole-zero diagram for an arbitrary conjugate pole pair on the tone detector circle. The angle $\theta = 360° \times f_O/f_S$, where f_O is the desired center frequency and f_S is the sampling rate (f_S = 9600 Hz). The following equations are derived from the angle and magnitude of the position vector pointing to a pole pair located at the desired angle:

$$\cos^{-1}\left(\frac{\beta_1}{r}\right) = \theta = 360° \times \frac{f_O}{f_S} \quad \text{(Eq. 5)}$$

$$\sqrt{\beta_1^2 + \left(-\beta_1^2 - 2\beta_2\right)} = r = 0.994030884 \quad \text{(Eq. 6)}$$

solving for β_1 and β_2:

$$\beta_1 = r \cos\left(360° \frac{f_O}{f_S}\right) \quad \text{(Eq. 7)}$$

$$\beta_2 = -\frac{r^2}{2} \quad \text{(Eq. 8)}$$

In deriving these equations, only $H_1(Z)$ was considered. However, the tone detector consists of two identical filters in cascade. Referring to Figure 5, shifting filter 1 and filter 2 above and below the desired center frequency, a response with the desired bandwidth is achieved. Furthermore, since α controls the amplitude response, one may set $\alpha = \alpha'$ to uniformly raise or lower the overall cascade response.

From Equation 8, we see that $\beta_2 = \beta'_2 = -r^2/2 = -0.494048699$. Rewriting Equation 7 in terms of the offsets f_A and f'_A we obtain:

$$\beta_1 = r \cos\left[360° \left(f_O - f_A\right)/f_S\right] \quad \text{(Eq. 9)}$$

$$\beta'_1 = r \cos\left[360° \left(f_O + f'_A\right)/f_S\right] \quad \text{(Eq. 10)}$$

The frequency offset is approximately 72% of B/2 (half the bandwidth):

$$f'_A \cong 0.72\left(\frac{B}{2}\right) \quad \text{(Eq. 11)}$$

The value of f_A should be equal to f'_A. However, f_A may be chosen 1% smaller than f'_A to compensate for the fact that the overall cascade response is not perfectly symmetrical (see Figure 5).

The values for the coefficients α and α' that set $|H(f_O)| = 0$ dB in equations 1 and 2 were measured and plotted versus center frequency f_O as shown in Figure 6. Three equations corresponding to three linear approximations result:

$$\alpha = \alpha' = \frac{(104/319)f_O - 78.62}{32767} \qquad 300 \le f_O \le 1100 \text{ Hz} \quad \text{(Eq. 12a)}$$

$$\alpha = \alpha' = \frac{(44/275)f_O + 104}{32767} \qquad 1100 \le f_O \le 1650 \text{ Hz} \quad \text{(Eq. 12b)}$$

$$\alpha = \alpha' = \frac{(4/45)f_O + 221}{32767} \qquad 1650 \le f_O \le 3000 \text{ Hz} \quad \text{(Eq. 12c)}$$

Energy Averaging Filter

The coefficients of the energy averaging filter are determined by a Z-domain approximation to an RC circuit of transfer function: $H(S) = 1/1 + S\tau$.

$$\alpha'' = \frac{1}{1 + 9600\tau} \quad \text{(Eq. 13)}$$

$$\beta'' = \frac{1}{1 + \frac{1}{9600\tau}} \quad \text{(Eq. 14)}$$

Upon power-up, α'' and β'' are set for τ = 0.1 seconds. Unless different tone detector response times are required, these coefficients need not be changed.

Table 1 contains the computed values of the filter coefficients, including those of default frequencies 462 Hz, 1100 Hz, and 2100 Hz. The value 32767 (Hex 7FFF) is full scale in the SP's machine units (i.e., 32767 = unity). Coefficients may range from −1 to +1 (or FFFF to 7FFF in machine units).

WRITING NEW COEFFICIENTS INTO THE SIGNAL PROCESSOR (SP) RAM

The RAM ACCESS B register (1:F) allows the host processor to specify an access code for RAM data registers. The access code specifies the RAM location being written. Table 2 contains the RAM access codes for all filter coefficients.

The proper procedure for writing new coefficients into the SP RAM is as follows:

1. Store the desired access code into register 1:F.
2. Wait for bit DA1 (1:E:0) to be a 1.
3. Set bit RAMW (1:D:0) to a 1.
4. Write the two halves of the 16-bit coefficient into registers 1:1 and 1:0. (Register 1:1 is the MSB.)

Writing to Register 1:0 resets DA1 (1:E:0) to a 0 and starts the write cycle, which ends by DA1 returning to a 1. Bit RAMW (1:D:0) must remain set until the end of the cycle.

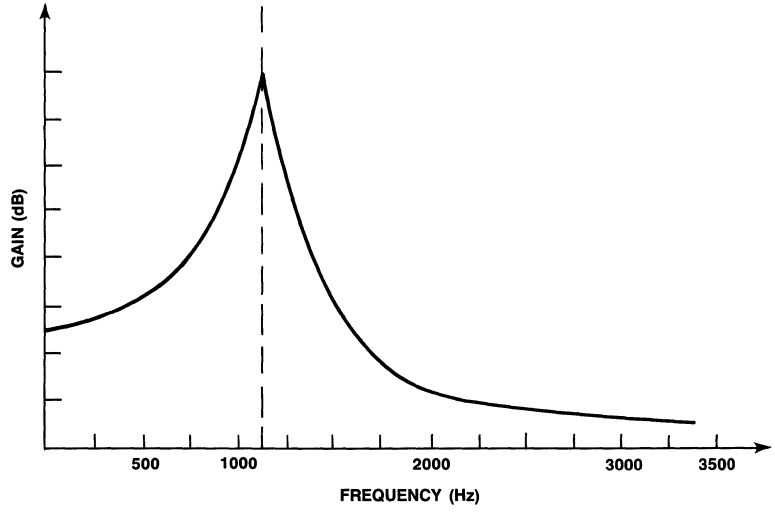


Figure 2. Typical Single Filter Response

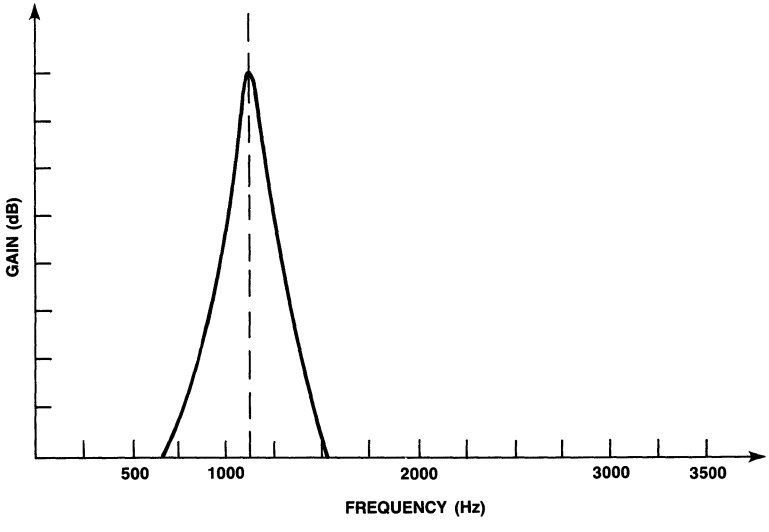


Figure 3. Typical Cascade Filter Response

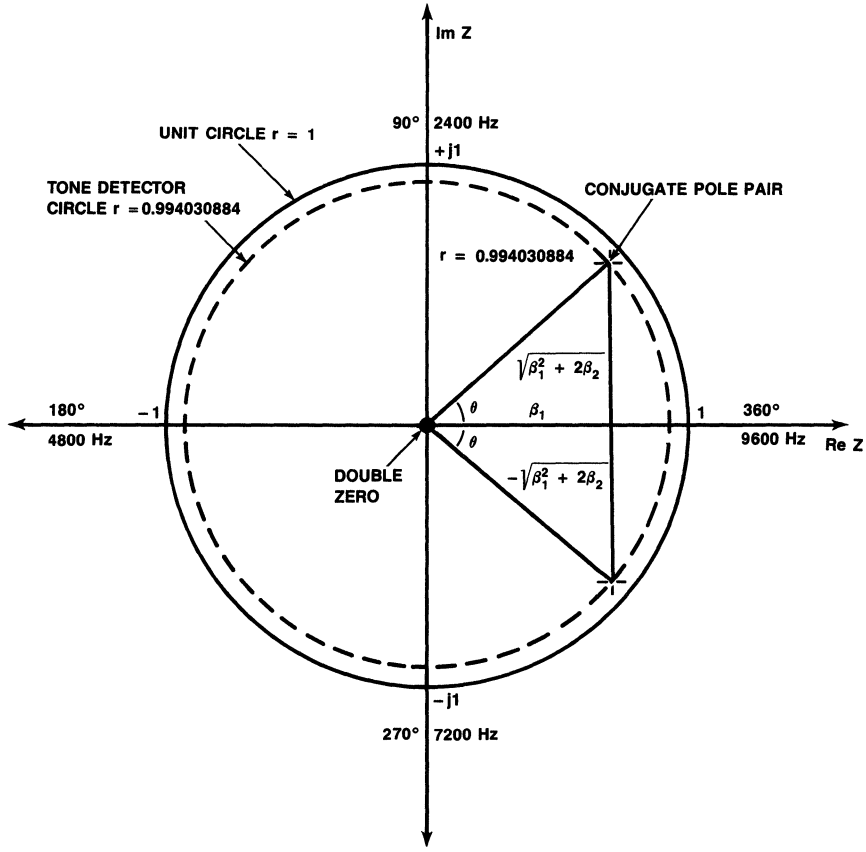


Figure 4. Z-Plane Pole-Zero Diagram

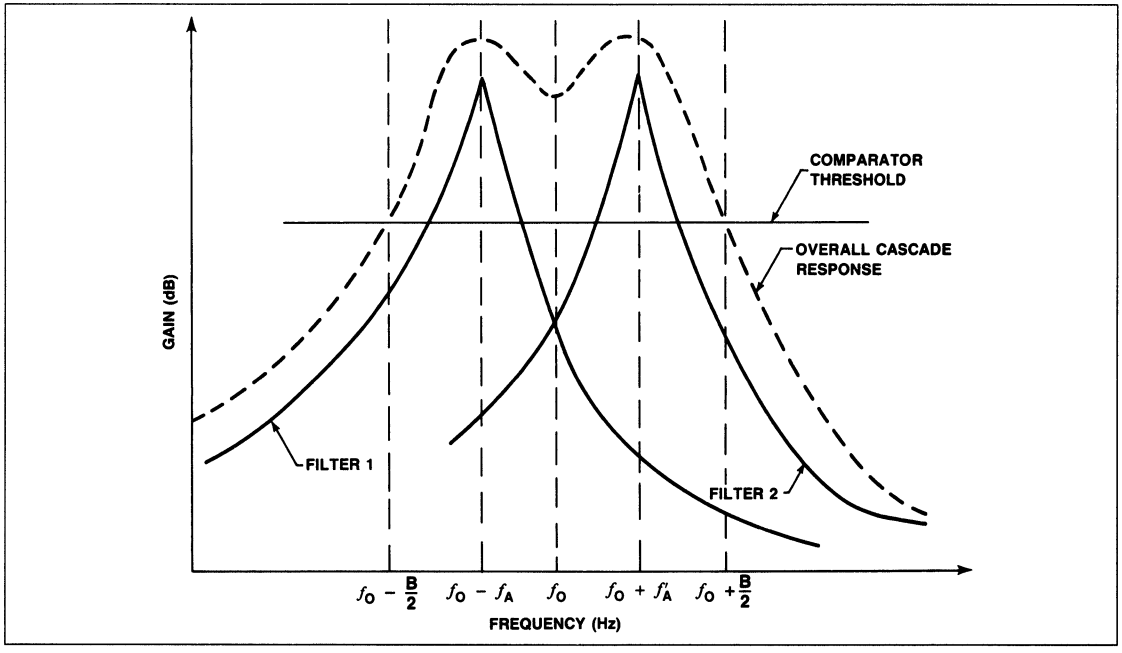


Figure 5. Graphical Representation of Bandwidth (B) and Offset Frequencies (f_A and f'_A)

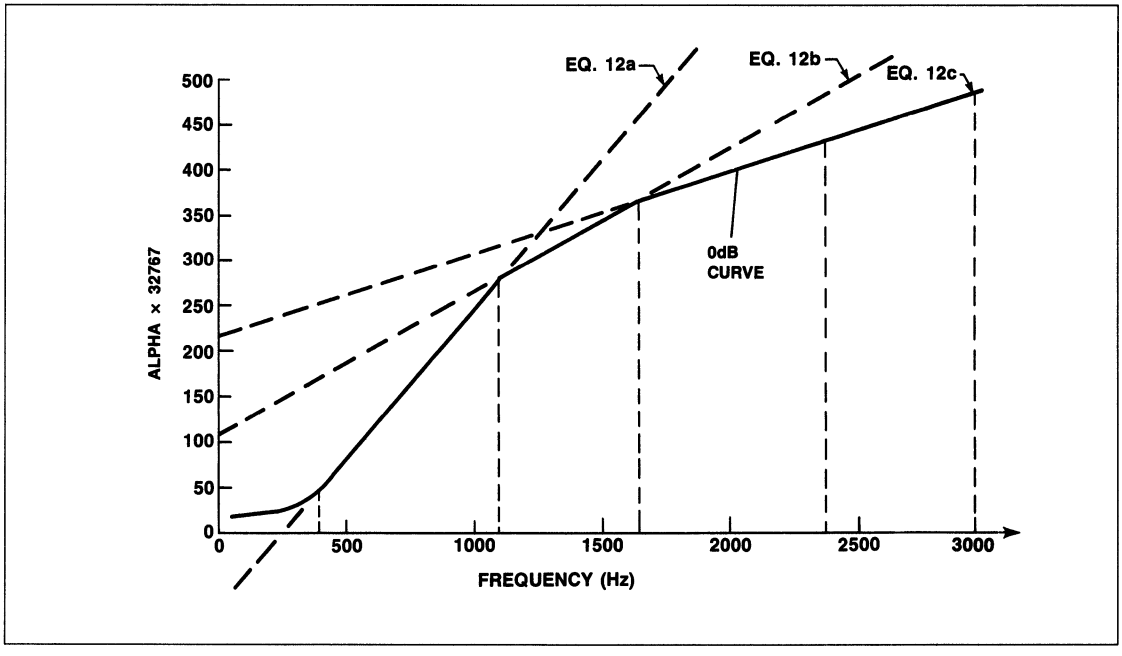


Figure 6. α versus Center Frequency for $|H(f_O)|$ = 0dB

Table 1. Calculated Coefficient Values

Frequency Detected	Coefficient Name	Coefficient Value	
		Hex	Decimal
2100 Hz ±25 Hz	$\alpha = \alpha'$	0198	408/32767
	β_1	1A4A	6730/32767
$f_A \cong 18$ Hz	β_1'	175A	5978/32767
	$\beta_2 = \beta_2'$	C0C5	−16187/32767
1850 Hz ±24 Hz	$\alpha = \alpha'$	0180	384/32767
	β_1	2E37	11831/32767
$f_A \cong 18$ Hz	β_1'	2B69	11113/32767
	$\beta_2 = \beta_2'$	C0C4	−16188/32767
1650 Hz ±23 Hz	$\alpha = \alpha'$	0170	368/32767
	β_1	3D48	15688/32767
$f_A \cong 18$ Hz	β_1'	3AA6	15014/32767
	$\beta_2 = \beta_2'$	C0C4	−16188/32767
1100 Hz ±30 Hz	$\alpha = \alpha'$	0118	280/32767
	β_1	60B2	24754/32767
$f_A \cong 19$ Hz	β_1'	5E9C	24220/32767
	$\beta_2 = \beta_2'$	C0C4	−16188/32767
462 Hz ±14 Hz	$\alpha = \alpha'$	0048	72/32767
	β_1	79F3	31219/32767
$f_A \cong 10$ Hz	β_1'	7974	31092/32767
	$\beta_2 = \beta_2'$	C083	−16253/32767

Table 2. Filter Coefficients Access Codes

Node No. (n)	Name	Access Code (Hex)		
		F1	F2	F3
1	α	2E	34	3A
2	β_1	2F	35	3B
3	β_2	30	36	3C
4	α'	2B	31	37
5	β_1'	2C	32	38
6	β_2'	2D	33	39
7	α''	B7	B9	BB
8	β''	B8	BA	BC

Rockwell

R96F Modem Recommended Receive Sequence for Group 2 Facsimile

INTRODUCTION

The R96F includes a transmit and receive configuration that is compatible with the transmission scheme of Group 2 facsimile equipment. In order to achieve the best results with Group 2 reception, the following procedure is recommended. The step numbers are keyed to points in Figure 1. Refer to Data Sheet MD06 and Application Note Order No. 654 for details on how to configure the modem and write modem data to chip one.

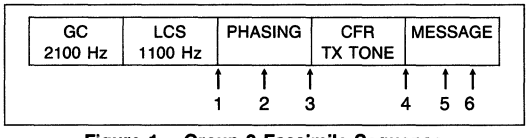


Figure 1. Group 2 Facsimile Sequence

METHOD

1. Enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Write hex 0038 using access code C2. This action sets the Group 2 phase-locked-loop for a frequency correction of 9 Hz, causing the phase term to drift rapidly to overcome any tendency to slow phase recovery.
   b. Write hex 4000 using access code F1 and hex 7FFF using access code 71. This action allows the Group 2 phase-locked-loop to accept the greatest number of samples for carrier recovery during phasing.
   c. Write hex 2000 using access code AA. This action sets the AGC slew rate for very fast acquisition.
   d. Select fast AGC state by setting control bit G2FGC (1:C:0) to a one.
2. After phasing is detected, wait approximately 2 seconds for the AGC circuit to settle. Then:
   a. Write hex 0000 using access code AA. This action stops AGC tracking in order to preserve the present AGC setting.
   b. Select slow AGC state by resetting control bit G2FGC (1:C:0) to a zero. This action changes the Group 2 phase-locked-loop characteristics to match reduced AGC response.
   c. Read and save the 16-bit value from registers 1:3 and 1:2 using access code C2. This value represents the frequency error term from the Group 2 phase-locked-loop.
   d. Verify that phasing signal is still being received. This action guarantees that AGC value was frozen during phasing signal.
   e. If step d above determines that phasing signal is present, allow transmission of CFR. If phasing signal is not present, suppress CFR.
3. Exit Group 2 configuration.
4. At completion of CFR transmission, re-enter Group 2 configuration and wait 5 milliseconds to complete initialization. Then:
   a. Repeat step 1.b.
   b. Repeat step 2.a.
   c. Add hex 0038 to the value saved in step 2.c above and write the sum using access code C2. This action forces a 9 Hz error as in step 1.a.
5. Wait for start of Group 2 message transmission. Then:
   a. Write hex 0400 using access code AA. This action restores the AGC slew rate to the default value.
   b. After 2 lines, write the value saved in step 2.c using access code C2. This action removes the 9 Hz forced frequency error without waiting for the phase-locked-loop to complete the correction. This step is optional as the correction will eventually be completed, but, depending on the percentage of white in the document being sent, the correction may take from 4 to 16 lines (100 ms of white required).
6. After approximately 6 to 10 seconds of message reception, perform either step a or step b below:
   a. Write hex 6100 using access code F1 and hex 0600 using access code 71. This action places narrow limits on the received signal used for carrier recovery during message reception and reduces the chance of errors being caused by repeated patterns in the message.
   b. Synchronize the modem's Group 2 phase-locked-loop to the facsimile machine's blanking signal as follows:
      1. Freeze the phase-locked-loop during data by:
         a. Writing hex 7FFF using access code F1
         b. Writing hex 0000 using access code 71
      2. Enable the phase-locked-loop during the white margins by:
         a. Writing hex 4000 using access code F1
         b. Writing hex 7FFF using access code 71
   c. The sequence of writing in step 6.b is important and must be performed as described. Option 6.b requires more action by the host procesor, but it eliminates the possibility of data patterns affecting carrier recovery.

5

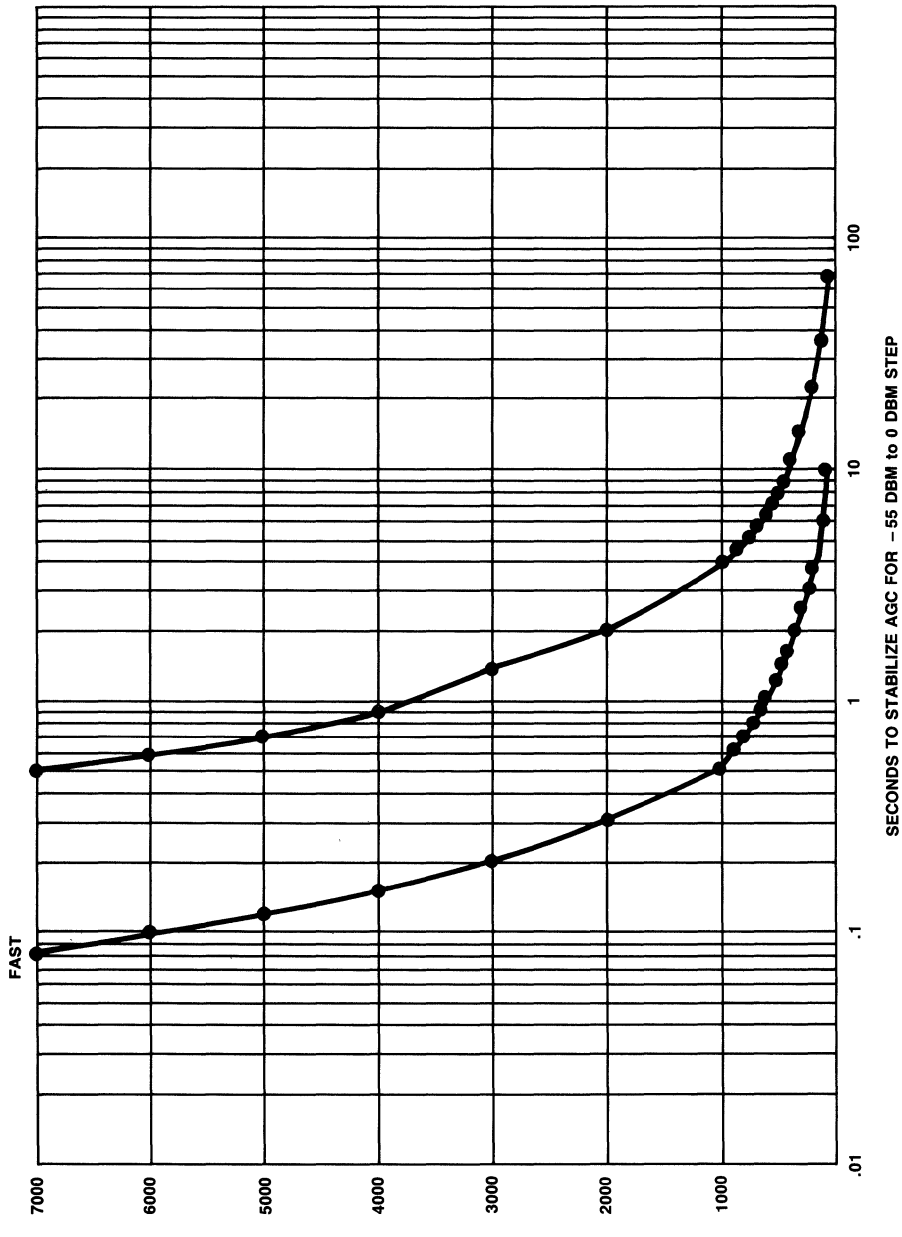


Figure 2. AGC Slew Rate

PARAMETER SCALING

1. Access code C2 represents frequency error; i.e., the deviation of received carrier from 2100 Hz. LSB = 0.167 Hz.; Range = ±140 Hz.

2. Access code F0 represents the Group 2 phase-locked-loop slew rate for the first order term. The number is directly proportional to slew rate. The range of stable operating values is 0010 to 7000 in hexidecimal.

3. Access code AA represents the AGC slew rate.
   Range = 0000 to 7FFF in hexidecimal.
   Scaling: see Figure 2.

4. Access codes F1 and 71 represent limits on acceptable zero crossings for use by the carrier recovery loop. The carrier recovery loop uses several nonlinear controls in attempting to lock the zero crossings of the local carrier to those of the transmitter. Since Group 2 facsimile uses VSB transmission, it is necessary to either reconstruct the upper sideband or exclude those zero crossings that represent frequencies other than 2100 Hz. The R96F excludes unwanted zero crossings by testing the effective slope of the waveform as it crosses zero. In Figure 3, points A and B represent samples taken about a zero crossing over sample period T, where T = 1/10,368 seconds.

   The magnitude of |A| + |B| is directly proportional to the slope of line segment AB and is therefore an indicator of frequency. If H represents the value stored at F1 and L represents the value at 71, then 1 − [|A| + |B|] + H must be less than positive full scale or the frequency is excluded for being too low. Also 1 − [|A| + |B|] + H + L must be greater than positive full scale or the frequency is excluded for being too high.

   The average value for 1 − [|A| + |B|] with an all white transmission and back-to-back connection is hex 19A1 ±0543.

5. An access code added to baud rate chip 5301-20 allows host control of the limits placed on phase error correction. This access code is F2 in chip 1. When the phase error exceeds the limit set by F2, PLL updating is suspended. The default value of 5000 corresponds to a limit of ±67.5 degrees. A zero in F2 causes the PLL to update for any phase error. By setting F2 to zero, it may be unnecessary to force a frequency offset in the receive sequence. For systems using step 6.a in the receive sequence, reception of messages containing a large amount of black may be improved by setting F2 to zero. F2 scaling is:

$$\text{Phase limit} = 180° - \left[\left(\frac{\text{F2 value}}{\text{7FFF}}\right) \times 180°\right]$$

   Once phasing is acquired, the limits may be narrowed to improve immunity to phase hits, etc.

BLACK/WHITE THRESHOLD

The R96F receives a Group 2 baseband signal that contains density (gray scale) information in the amplitude modulation. In order for this information to be used on a Group 3 facsimile machine the R96F converts the gray scale to black/white baseband form. The threshold at which the black/white decision is made determines the density of the received page.

Access code 2A represents the Group 2 black/white threshold. This location defaults to hex 7800 at POR time. The number may be increased or decreased by the host to achieve a page weighted more toward white or toward black, respectively.

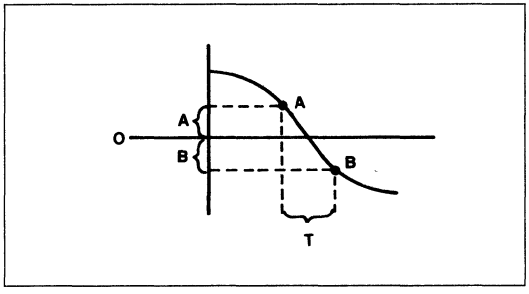


Figure 3. Samples of Zero Crossing

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DTMF Dialing Using the R24MFX, R24BKJ, R48MFX, or R48PCJ Modem

INTRODUCTION

The R24MFX, R24BKJ, R48MFX, and R48PCJ modems include tunable oscillators that can be used to perform dual-tone multi-frequency (DTMF) dialing. The frequency and amplitude of each oscillator output is under host control. A programmable tone detector can also be used in call establishment to recognize an answer tone.

This application note describes the method of oscillator and filter tuning by the host processor and provides an example of an auto-dialer routine that may be programmed into the host.

DTMF REQUIREMENTS

EIA Standard RS-496, paragraph 4.3.2, specifies requirements that ensure proper DTMF signaling through the public switched telephone network (PSTN). These tones consist of two sinusoidal signals, one from a high group of three frequencies and one from a low group of four frequencies, that represent each of the standard pushbutton telephone characters shown in Table 1.

Table 1. DTMF Signals

High Frequency / Low Frequency	1209 Hz	1336 Hz	1477 Hz
697 Hz	1	2	3
770 Hz	4	5	6
852 Hz	7	8	9
941 Hz	*	0	#

Signal power is defined for the combined tones as well as for the individual tones. Both maximum and minimum power requirements are functions of loop current. By combining the various requirements of RS-496, compromise power levels can be determined that meet the power specification for all U.S. lines (when driving the PSTN from a 600 ohm resistive source). The high frequency tone should be at a higher power level than the low frequency tone by approximately 2 dB. The maximum combined power, averaged over the pulse duration, should not exceed +1 dBm. The minimum steady state power of the high frequency tone should not be less than −8 dBm. When connecting the modem circuit to the PSTN by means of a data access arrangement (DAA) set for permissive mode, the DAA gain is −9 dB. The modem circuit must, therefore, drive the DAA input with +1 dBm of steady state high frequency power and −1 dBm of steady state low frequency power in order to meet all of the listed conditions.

The required duration of the DTMF pulse is 50 ms minimum. By experience, a pulse duration of approximately 95 ms is more reliable. The required interval between DTMF pulses is 45 ms minimum and 3 seconds maximum. Again by experience, an interdigit delay of approximately 70 ms is preferred.

The remaining requirements of RS-496, relative to DTMF dialing, are not influenced by the host processor. These requirements are all met by the modem's oscillators.

SETTING OSCILLATOR PARAMETERS

The oscillator frequency and output power are set by the host computer using the microprocessor bus and diagnostic data routine. For a description of the microprocessor bus and other interface considerations, refer to the R24/48MEB modem evaluation board data sheet and the relevant modem data sheet listed in Table 2.

Table 2. Data Sheet Order Numbers

Title	Order Number
R24/48MEB Data Sheet	MD22
R24MFX Data Sheet	MD17
R24BKJ Data Sheet	MD20
R48MFX Data Sheet	MD19
R48PCJ Data Sheet	MD21

When setting the frequency of tone 1, the host must write a 16-bit hexadecimal number into RAM using RAMA code 8E. When setting the frequency of tone 2, a 16-bit hexadecimal number must be written into RAM using RAMA code 8F. The power levels of tone 1 and tone 2 are set by writing 16-bit hexadecimal numbers into RAM using RAMA codes 44 and 45, respectively. The hexadecimal numbers written into these RAM locations are scaled as follows:

R24MFX AND R24BKJ

Frequency number = 9.1022 (desired frequency in Hz).

R48MFX AND R48PCJ

Frequency number = 6.8267 (desired frequency in Hz).

R24MFX, R24BKJ, R48MFX, AND R48PCJ

Power number = 27573.6 $[10^{(P_O/20)}]$

Where P_o = output power in dBm with a series 600 ohm resistor into a 600 ohm load.

These decimal numbers must be converted to hexadecimal form then stored in RAM by following the RAM data write routine illustrated by Figure 1.

Hexadecimal numbers for DTMF generation on the R24MFX and R48MFX are listed in Table 3. These numbers are also suitable for use with the R24BKJ and R48PCJ. Numbers used for setting the frequency of tone 1 and tone 2 are larger in the 2400 bps products than in the 2400/4800 bps products. This variation is due to the sample rate difference between these modems. Power levels are selected to give the desired output power for each tone while compensating for modem filter characteristics.

Table 3. DTMF Parameters

Digit	RAMA	R24XXX	R48XXX
0	8E	2174	1918
	8F	2F80	23A0
	44	6184	6184
	45	7A80	7A80
1	8E	18C8	1296
	8F	2AFC	203D
	44	61E8	61E8
	45	7AFC	7AFC
2	8E	18C8	1296
	8F	2F80	23A0
	44	61E8	61E8
	45	7A80	7A80
3	8E	18C8	1296
	8F	3483	2763
	44	61E8	61E8
	45	79E3	79E3
4	8E	1B60	1488
	8F	2AFC	203D
	44	6250	6250
	45	7AFC	7AFC
5	8E	1B60	1488
	8F	2F80	23A0
	44	6250	6250
	45	7A80	7A80
6	8E	1B60	1488
	8F	3483	2763
	44	6250	6250
	45	79E3	79E3
7	8E	1E4A	16B8
	8F	2AFC	203D
	44	621A	621A
	45	7AFC	7AFC
8	8E	1E4A	16B8
	8F	2F80	23A0
	44	621A	621A
	45	7A80	7A80
9	8E	1E4A	16B8
	8F	3483	2763
	44	621A	621A
	45	79E3	79E3

DETECTING ANSWER TONE

The modem tone detect bit, TDET (A:7), can be used to detect the presence of answer tone when connection to the remote modem is successful. Bit TDET goes active (one) when energy is detected by the associated tone detect filter. This filter is illustrated in Figure 2.

A set of eight coefficients determines the filter response. Table 2 lists the RAM access codes and filter coefficient values to be written using the RAM Data Write routine of Figure 1. These values tune the filter to detect 2100 Hz ± 25 Hz.

Once TDET turns on, the calling modem knows the call has been answered. At the end of the answer tone, TDET returns to zero and data transmission can begin.

COMPLETE CALLING SEQUENCE

A complete calling sequence consists of several steps including modem configuration, telephone number selection, DTMF transmission, and answer tone detection. A sample flow chart for implementing an auto-dialer in host software is illustrated in Figure 3.

The auto-dialer routine may be entered at one of two points; either AUTO DIAL or REDIAL. When entering at AUTO DIAL, the host prompts the user to enter a phone number, which is then stored in the phone number buffer. When entering at REDIAL, the routine dials the number previously stored in the phone number buffer and does not issue a user prompt.

Interrupts not required during dialing are disabled to prevent errors in real time delays. Interrupt status is saved to allow restoring these interrupts when dialing is complete. The current modem configuration is saved prior to selecting the tone configuration, then restored at the completion of the auto-dialer routine to allow data transfer.

The commands for off-hook and request coupler cut through are typical of signals required by data access arrangements that may be connected to the modem for switched network operation.

Since the number to be dialed varies in length depending on the requirements of various PBX equipment, domestic telephone companies, and foreign PTTs, the number buffer must allow for numbers of different length. The method used in Figure 3 to determine the end of valid bytes in the buffer is zero recognition. After the last digit is entered, the carriage return must place a hexadecimal 00 (nul character) in the buffer. All other bytes must be non-zero ASCII characters. Only numeric characters (ASCII 30 through 39) are printed and dialed. Non-numeric characters are tested for comma and nul. Comma causes a 2-second pause in dialing to allow for known delays in the telephone network or PBX. Nul ends the dialing portion of the routine and begins the answer tone detection portion. All other characters are ignored.

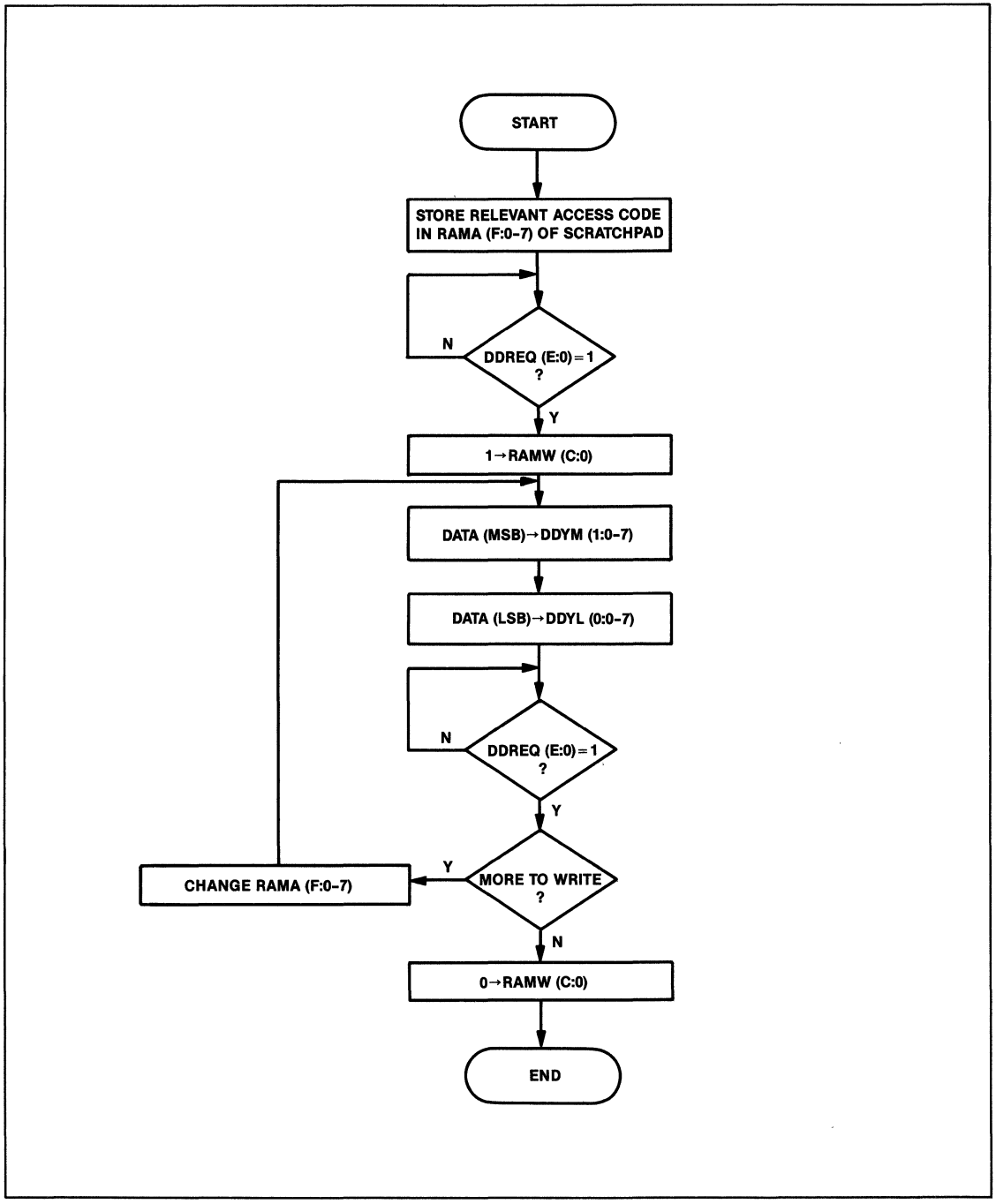

Figure 1. RAM Data Write Routine

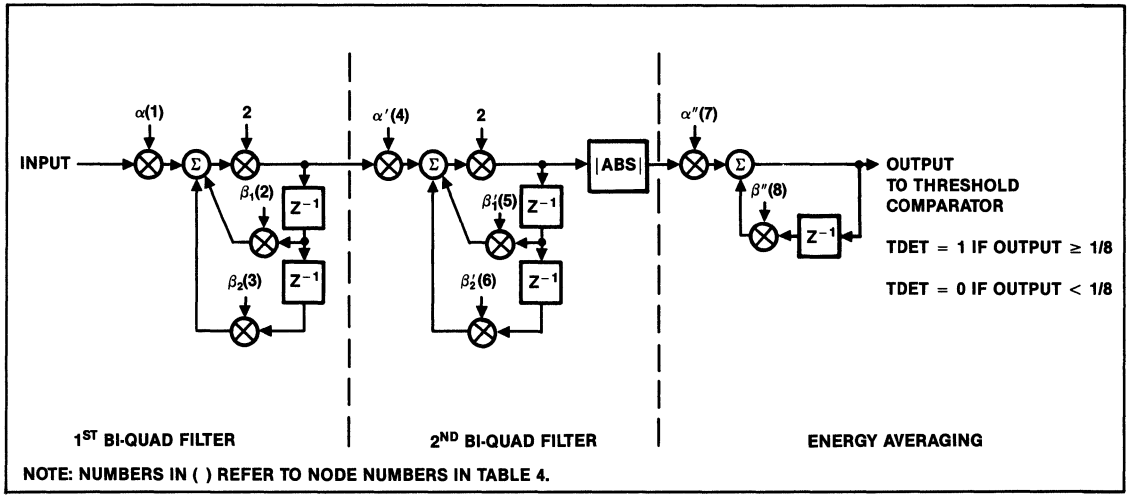

Figure 2. Tone Detector Diagram

Table 4. Tone Detector Coefficients for 2100 Hz

Node	Coefficient Name	R24XX RAMA	R24XX Coefficient Value	R48XX RAMA	R48XX Coefficient Value
1	α	36	0198	38	0198
2	β_1	37	E0F4	39	1A4A
3	β_2	38	C0C5	3A	C0C5
4	α'	39	0198	3B	0198
5	β'_1	3A	DD33	3C	175A
6	β'_2	3B	C0C5	3D	C0C5
7	α''	B6	002D	B8	002D
8	β''	B7	7FD1	B9	7FD1

The answer tone detection logic allows 30 seconds for 2100 Hz recognition. If answer tone is not recognized within this time limit, the call is aborted. If answer tone is recognized, the routine jumps to the data handling software.

ADDED FEATURES

The application of modem tone generation and detection to DTMF dialing and answer tone recognition can be extended to include additional features. For example, the tone detector can monitor call progress for dial tone, busy signal or ringback tone. The detector filter must be returned to detect different frequencies used in call progress signaling. Table 5 lists tones for various lines in the Bell network. These call progress signals vary according to the telephone networks of each country. For details on tuning the tone detector for other frequencies, refer to Application Note Order No. 668. That note refers to the R96F filters but is also applicable to R24XXX and R48XXX modems for coefficient calculation. When applying Application Note 668 to R24XXX modems, the sample rate used should be 7200 samples per second rather than 9600 samples per second.

In OEM equipment that combines the features of a modem with those of a telephone handset, the tone generators may be used to generate a caller reassurance tone (or even music) while the caller is kept on hold. To generate a single tone, set one of the oscillators to zero frequency or zero amplitude while the other oscillator is keyed on by the RTSP bit. This technique is also applicable for generating a 2100 Hz answer tone when the modem is used to automatically answer a call. The parameters for 2100 Hz answer tone generation are listed in Table 6.

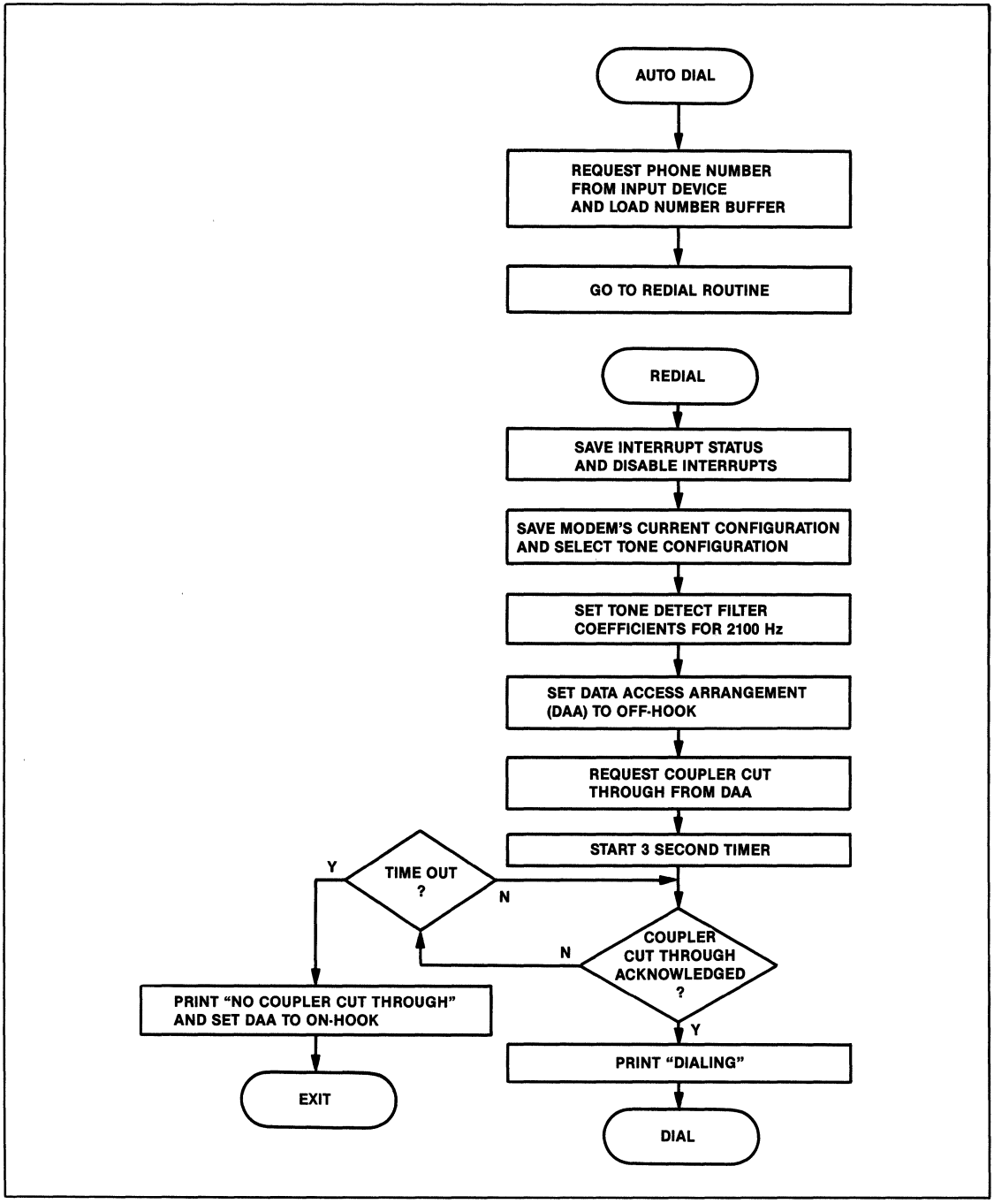

Figure 3. Autodialer Flow Chart

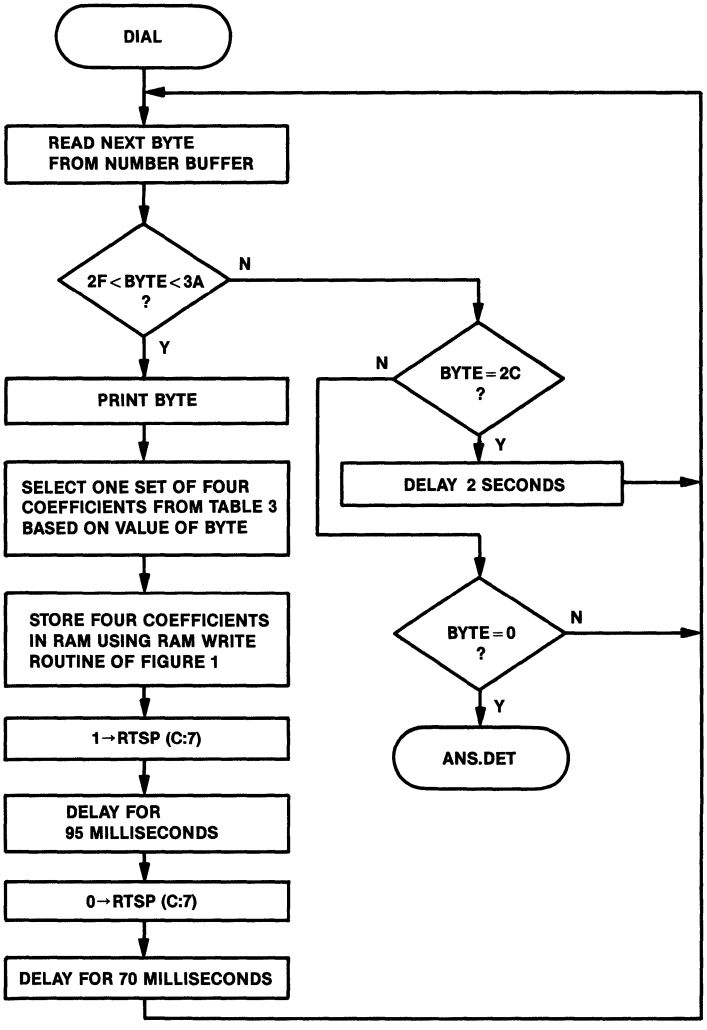

Figure 3. Autodialer Flow Chart (Cont'd)

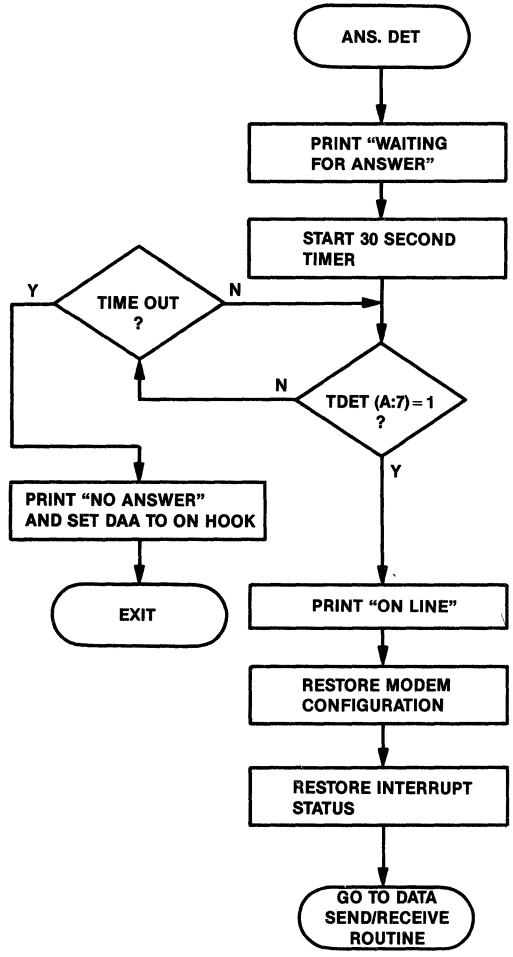

Figure 3. Autodialer Flow Chart (Cont'd)

Table 5. Call Progress Signals

Tone	Frequency (Hz)*	Interruption Rates	Use
Precision Dial Tone	350 +440	Continuous	Dialing may commence
Old Dial Tones	600 +120 or 133, and other combinations	Continuous	Dialing may commence
Precision Busy	480 +620	0.5 Sec On 0.5 Sec. Off	Called line busy
Old Busy	600 +120	0.5 Sec On 0.5 Sec. Off	Called line busy
Precision Reorder Old Reorder	480 +620 600 +120	0 3 Sec. On } Local 0.2 Sec. Off } Reorder 0.2 Sec. On } Toll 0.3 Sec Off } Reorder 0.25 Sec. On } Toll 0.25 Sec. Off } Local	All local switching paths busy, all trunks busy, all paths or trunks busy
Precision Audible Ringing	440 +480	2 Sec. On 4 Sec. Off	To calling customer
Old Audible Ringing	420 +40, and other combinations	2 Sec. On 4 Sec. Off	To calling customer
Call Waiting	440	0 3 Sec. On	Call waiting service; an incoming call is waiting
Precision Receiver Off-Hook (ROH)	1400 +2060 +2450 +2600	On and Off 5 Times per Sec.	To cause off-hook customers to go on-hook
Precision High Tone Old High Tone	480 480, 400 or 540	Continuous	To cause off-hook customers to go on-hook
Recorder Connector Tone	1400	On 0 5 Sec. Every 15 Seconds	To indicate call is being recorded by distant customer

*A "+" sign indicates either superposition (precision tones) or modulation (old tones).

Table 6. 2100 Hz Answer Tone Parameters

Frequency	RAMA	R24XXX	R48XXX
2100 Hz	8E	4AAA	3800
	8F	0000	0000
	44	5FFF	5FFF
	45	5FFF	5FFF

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