APPLICATIONS

Power Transistors

Power Transistor Applications

This Manual is intended as a guide to the designers of power transistor circuits. It includes a brief introduction to solid-state physics and general information on electrical ratings, packaging and mounting techniques, and thermal factors for power transistor devices. Detailed discussions are provided on the theory of operation, basic design concepts, operating parameters, structures, geometries, and capabilities of power transistors. Specific design criteria and procedures are supplied for circuits that use power transistors in the amplification, rectification, conversion, control, and switching of electrical power. Design examples are given, and practical circuits are shown and analyzed.

This Manual is a comprehensive, authoritative, up-to-date text on the design of power transistor circuits. It will be found extremely useful by circuit and systems designers, educators, students, hobbyists, and others.

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Basic Design Considerations

Solid-state devices are small but versatile units that can perform a great variety of control functions in electronic equipment. Like other electron devices, they have the ability to control almost instantly the movement of charges of electricity. They are used as rectifiers, detectors, amplifiers, oscillators, electronic switches, mixers, and modulators.

In addition, solid-state devices have many important advantages over other types of electron devices. They are very small and light in weight. They have no filaments or heaters, and therefore require no heating power or warm-up time. They consume very little power. They are solid in construction, extremely rugged, free from microphonics, and can be made impervious to many severe environmental conditions.

SEMICONDUCTOR MATERIALS

Unlike some electron devices, which depend on the flow of electric charges through a vacuum or a gas, solid-state devices make use of the flow of current in a solid. In general, all materials may be classified into three major categories—conductors, semiconductors, and insulators—depending upon their ability to conduct an electric current. As the name indicates, a semiconductor material has poorer conductivity than a conductor, but better conductivity than an insulator.

The material most often used in semiconductor devices is silicon. Germanium has higher electrical conductivity (less resistance to current flow) than silicon, and has been used in the past in many low- and medium-power diodes and transistors. Silicon is more suitable for higher power devices than germanium. One reason is that it can be used at much higher temperatures. In general, silicon is preferred over germanium because silicon processing techniques yield more economical devices. As a result, silicon has superseded germanium in almost every type of application, including the small-signal area.

Resistivity

The ability of a material to conduct current (conductivity) is directly proportional to the number of free (loosely held) electrons in the material. Good conductors, such as silver, copper, and aluminum, have large numbers of free electrons; their resistivities are of the order of a few millionths of an ohm-centimeter. Insulators such as glass, rubber, and mica, which have very few loosely held electrons, have resistivities as high as several million ohm-centimeters.

Semiconductor materials lie in the range between these two extremes, as shown in Fig. 1. Pure germanium has a resistivity of 60 ohm-
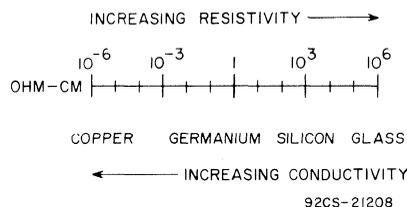
Fig. 1 - *Resistivity of typical conductor, semiconductor, and insulator.*

centimeters. Pure silicon has a considerably higher resistivity, in the order of 60,000 ohm-centimeters. As used in solid-state devices, however, these materials contain carefully controlled amounts of certain impurities which reduce their resistivity from a low of less than one to greater than 50 ohm-centimeters at room temperature (this resistivity decreases rapidly as the temperature rises).

Impurities

Carefully prepared semiconductor materials have a crystal structure. In this type of structure, which is called a lattice, the outer or valence electrons of individual atoms are tightly bound to the electrons of adjacent atoms in electron-pair bonds, as shown in Fig. 2. Because such a structure has no loosely held

ELECTRON-PAIR BONDS   ATOMS

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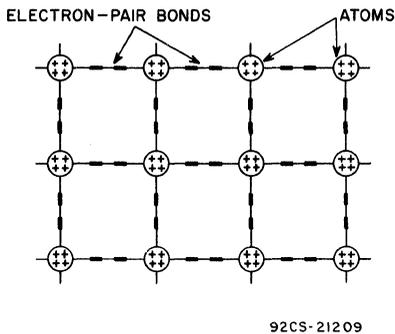
Fig. 2 - Crystal lattice structure.

electrons, semiconductor materials are normally poor conductors. One way to separate the electron-pair bonds and provide free electrons for electrical conduction would be to apply high temperature or strong electric fields to the material.

Another way to alter the lattice structure and thereby obtain free electrons, however, is to add small amounts of other elements having a different atomic structure. By the addition of almost infinitesimal amounts of such other elements, called **impurities**, the basic electrical properties of pure semiconductor materials can be modified and controlled. The ratio of impurity to the semiconductor material is usually extremely small, in the order of one part in ten million.

When the impurity elements are added to the semiconductor material, impurity atoms take the place of semiconductor atoms in the lattice structure.

When the impurity atom has one more valence electron than the semiconductor atom, this extra electron cannot form an electron-pair bond because no adjacent valence electron is available. The excess electron is then held very loosely by the atom, as shown in Fig. 3, and requires only slight excitation to break away. Consequently, the presence of such excess electrons makes the material a better conductor, i.e., its resistance to current flow is reduced.

ELECTRON-PAIR BONDS   SEMICONDUCTOR ATOMS

IMPURITY ATOM   EXCESS ELECTRON

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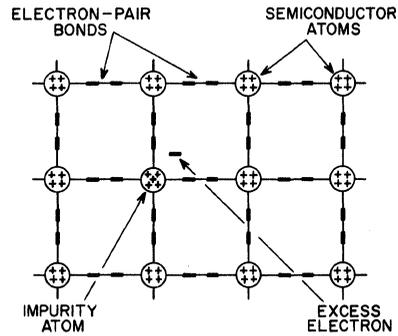
Fig. 3 - Lattice structure of n-type material.

Impurity elements which are added to silicon crystals to provide excess electrons include phosphorus, arsenic, and antimony. When these elements are introduced, the resulting material is called **n-type** because the excess free electrons have a negative charge. (It should be noted, however, that the negative charge of the electrons is balanced by an equivalent positive charge in the center of the impurity atoms. Therefore, the net electrical charge of the semiconductor material is not changed.)

A different effect is produced when an impurity atom having one less valence electron than the semiconductor atom is substituted in the lattice structure. As a result, a vacancy or **hole** exists in the lattice, as shown in Fig. 4. An

ELECTRON-PAIR BONDS   SEMICONDUCTOR ATOMS

IMPURITY ATOM   VACANCY (HOLE)

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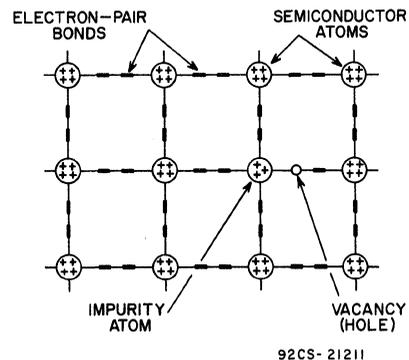
Fig. 4 - Lattice structure of p-type material.

electron from an adjacent electron-pair bond may then absorb enough energy to break its bond and move through the lattice to fill the hole. As in the case of excess electrons, the presence of holes encourages the flow of electrons in the semiconductor material;

consequently, the conductivity is increased and the resistivity is reduced.

The vacancy or hole in the crystal structure is considered to have a positive electrical charge because it represents the absence of an electron. (Again, however, the net charge of the crystal is unchanged.) Semiconductor material which contains these holes or positive charges is called **p-type** material. P-type materials are formed by the addition of boron, aluminum, gallium, or indium.

Although the difference in the chemical composition of n-type and p-type materials is slight, the differences in the electrical characteristics of the two types are substantial, and are very important in the operation of semiconductor devices.

JUNCTIONS

When n-type and p-type materials are joined together, as shown in Fig. 5, an unusual but
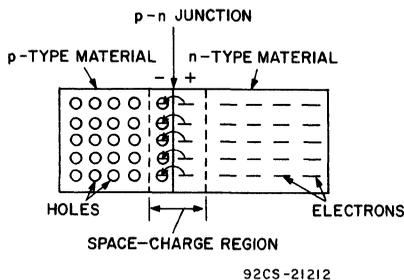
Fig. 5 - Interaction of holes and electrons at p-n junction.

very important phenomenon occurs at the interface where the two materials meet (called the **p-n junction**). An interaction takes place between the two types of material at the junction as a result of the holes in one material and the excess electrons in the other.

When a p-n junction is formed, some of the free electrons from the n-type material diffuse across the junction and recombine with holes in the lattice structure of the p-type material; similarly, some of the holes in the p-type material diffuse across the junction and recombine with free electrons in the lattice structure of the n-type material. This interaction or diffusion is brought into equilibrium by a small space-charge region (sometimes called the **transition region** or **depletion layer**). The p-type material thus acquires a slight negative charge and the n-type material acquires a slight positive charge.

Thermal energy causes charge carriers (electrons and holes) to diffuse from one side of the p-n junction to the other side; this flow of charge carriers is called **diffusion current**. As a result of the diffusion process, however, a potential gradient builds up across the space-charge region. This potential gradient can be represented, as shown in Fig. 6, by an imaginary battery connected across the p-n junction. (The battery symbol is used merely to illustrate internal effects; the potential it represents is not directly measurable.) The
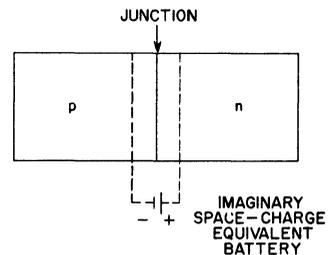
Fig. 6 - Potential gradient across space-charge region.

potential gradient causes a flow of charge carriers, referred to as **drift current**, in the opposite direction to the diffusion current. Under equilibrium conditions, the diffusion current is exactly balanced by the drift current so that the net current across the p-n junction is zero. In other words, when no external current or voltage is applied to the p-n junction, the potential gradient forms an **energy barrier** that prevents further diffusion of charge carriers across the junction. In effect, electrons from the n-type material that tend to diffuse across the junction are repelled by the slight negative charge induced in the p-type material by the potential gradient, and holes from the p-type material are repelled by the slight positive charge induced in the n-type material. The potential gradient (or energy barrier, as it is sometimes called), therefore, prevents total interaction between the two types of materials, and thus preserves the differences in their characteristics.

Current Flow

When an external battery is connected across a p-n junction, the amount of current flow is determined by the polarity of the

applied voltage and its effect on the space-charge region. In Fig. 7(a), the positive terminal of the battery is connected to the n-type material and the negative terminal to the p-type material. In this arrangement, the free electrons in the n-type material are attracted toward the positive terminal of the battery and away from the junction. At the same time, holes from the p-type material are attracted toward the negative terminal of the battery and away from the junction. As a result, the space-charge region at the junction becomes effectively wider, and the potential gradient increases until it approaches the potential of the external battery. Current flow is then extremely small because no voltage difference (electric field) exists across either the p-type or the n-type region. Under these conditions, the p-n junction is said to be **reverse-biased**.

In Fig. 7(b), the positive terminal of the external battery is connected to the p-type material and the negative terminal to the n-type material. In this arrangement, electrons in the p-type material near the positive terminal of the battery break their electron-pair bonds and enter the battery, creating new holes. At the same time, electrons from the negative terminal of the battery enter the n-type material and diffuse toward the junction. As a result, the space-charge region becomes effectively narrower, and the energy barrier decreases to

ELECTRON FLOW

(a) REVERSE BIAS

ELECTRON FLOW

(b) FORWARD BIAS

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Fig. 7 - Electron current flow in biased p-n junctions.

an insignificant value. Excess electrons from the n-type material can then penetrate the space-charge region, flow across the junction, and move by way of the holes in the p-type material toward the positive terminal of the battery. This electron flow continues as long as the external voltage is applied. Under these conditions, the junction is said to be **forward-biased**.

The generalized voltage-current characteristic for a p-n junction in Fig. 8 shows both the reverse-bias and forward-bias regions. In the

CURRENT(mA)

FORWARD CURRENT

REVERSE BIAS

FORWARD BIAS

REVERSE CURRENT

CURRENT (μA)

92CS-21215

Fig. 8 - Voltage-current characteristic for a p-n junction.

forward-bias region, current rises rapidly as the voltage is increased and is relatively high. Current in the reverse-bias region is usually much lower. Excessive voltage (bias) in either direction is avoided in normal applications because excessive currents and the resulting high temperatures may permanently damage the solid-state device.

TRANSISTOR STRUCTURES

Fig. 7 shows that a p-n junction biased in the reverse direction is equivalent to a high-resistance element (low current for a given applied voltage), while a junction biased in the forward direction is equivalent to a low-resistance element (high current for a given applied voltage). Because the power developed by a given current is greater in a high-resistance element than in a low-resistance element ($P = I^2 R$), power gain can be obtained in a structure containing two such resistance elements if the current flow is not materially reduced. A device containing two p-n junctions biased in opposite directions can operate in this fashion. The resulting device is called a transistor.

Such a two-junction device is shown in Figs. 9 and 10. The thick end layers are made of the same type of material (n-type in this case), and are separated by a very thin layer of the opposite type of material (p-type in the device shown). The three regions of the device are called the **emitter**, the **base**, and the **collector**, as shown in Fig. 10. By means of the external batteries, the left-hand (n-p) junction is biased in the forward direction to provide a low-resistance input circuit, and the right-hand (p-n) junction is biased in the reverse direction to provide a high-resistance output circuit.
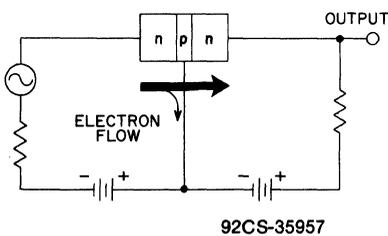
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Fig. 9 - N-P-N structure biased for power gain.
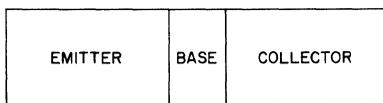
Fig. 10 - Functional diagram of transistor structure.

Electrons flow easily from the left-hand n-type region to the center p-type region as a result of the forward biasing. Most of these electrons diffuse through the thin p-type region, however, and are attracted by the positive potential of the external battery across the right-hand junction. In practical devices, approximately 95 to 99.5 per cent of the electron current reaches the right-hand n-type region. This high percentage of current penetration provides power gain in the high-resistance output circuit and is the basis for transistor amplification capability.

The operation of p-n-p devices is similar to that shown for the n-p-n device, except that the bias-voltage polarities are reversed, and electron-current flow is in the opposite direction. (In general, discussions of semiconductor theory assume that the "holes" in semiconductor material constitute the main charge carriers in p-n-p devices, and discuss "hole currents" for these devices and "electron currents" for n-p-n devices. The direction of hole current flow is considered to be the same as that of conventional current flow, which is assumed to travel through a circuit in a direction from the positive terminal of the external battery back to its negative terminal. This direction is opposite from that of electron flow, which travels from a negative to a positive terminal.)

Different symbols are used for n-p-n and p-n-p transistors to show the difference in the direction of current flow in the two types of devices. In the n-p-n transistor shown in Fig. 11(a), electrons flow from the emitter to the collector. In the p-n-p transistor shown in Fig. 11(b), electrons flow from the collector to the emitter. In other words, the direction of electron current is always opposite to that of the arrow on the emitter lead. The arrow indicates the direction of "conventional current flow" in the circuit.
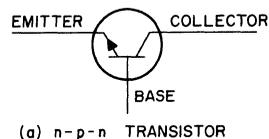
(a) n-p-n TRANSISTOR
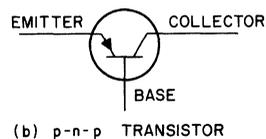
(b) p-n-p TRANSISTOR

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Fig. 11 - Schematic symbols for transistors.

The transistor can be used for a wide variety of control functions, including amplification, oscillation, switching, and frequency conversion. Power-transistor characteristics and ratings are discussed in the following pages.

The ultimate aim of all transistor fabrication techniques is the construction of two parallel p-n junctions with controlled spacing between the junctions and controlled impurity levels on both sides of each junction. A variety of structures and geometries have been developed in the course of transistor evolution.

In power transistors, structure refers to the junction depth, the concentration and profile of the impurities (doping), and the spacings of the various layers of the device. Geometry refers to the topography of the transistor. These factors and the method of assembly of the semiconductor pellet into the over-all transistor package have an important bearing on the types of applications in which a power transistor can be used to optimum advantage. The proper choices of trade-offs among these factors determine the gain, frequency, voltage, current, and dissipation capabilities of power transistors.

Various structures have been developed to provide different electrical, thermal, or cost properties, with each having certain advantages or compromises to offer. Table I lists the principal structures available for silicon power transistors, together with some of the advantages and disadvantages of each type. A brief description of each type of structure follows.

Table I—Types of Structures for Silicon Power Transistors

Structure	Advantages	Disadvantages
Hometaxial-base	Electrically rugged, low cost, good voltage rating	Low speed, low upper-voltage limit (150-200 V)
Double-diffused mesa	High speed	High saturation resistance
Double-diffused planar	Uniformity of device characteristics, high speed, low leakage	High saturation resistance
Triple-diffused	High speed, low saturation resistance	Moderate cost, moderate leakage
Triple-diffused planar	Very low leakage, high speed, low saturation resistance	Higher cost
Double-diffused epitaxial mesa	High speed, low saturation resistance	Moderate cost, moderate leakage, less rugged
Double-diffused epitaxial planar	High speed, low leakage, low saturation resistance	High cost, less rugged
Epitaxial-base mesa	High current-carrying capability, moderate speed, low saturation resistance	Low voltage, moderate leakage
Multiple-epitaxial-base mesa	Good current-handling capability, moderate speed, low saturation resistance, electronically rugged, high voltage	Moderate cost
Double-diffused multiple-epitaxial mesa	High speed, electronically rugged, low saturation resistance, high collector-junction voltage ratings	Moderate cost, moderate leakage
Darlington (double-epitaxial, single-diffused)	Moderate speed, high gain, high input impedance	High saturation resistance

Hometaxial-Base Transistors

Hometaxial-base transistors start with a wafer of moderately-high-resistivity silicon on which are deposited several thin layers of impurities. Then, under controlled temperature and ambient conditions, the impurities are driven deep into both sides of the silicon wafer. Early in the diffusion, the process is interrupted briefly, and a "mesa" or raised portion is selectively etched to define the emitter geometry. The process is complete when the deep diffused junctions are separated by a moderately wide (about 1 mil) base region. Fig. 12 shows a typical cross section of a completed single-diffused hometaxial transistor.

Double-Diffused Transistors

Double-diffused transistors start with a relatively high-resistivity silicon wafer on which a base dopant impurity is deposited. This dopant is then diffused to a shallow depth. Then, an oxide (S_iO_2) is selectively etched to define regions where an emitter impurity is to be deposited and diffused. The oxide acts as an effective mask against the diffusion of most of the usual impurity elements, such as boron or phosphorus. The emitter diffuses more rapidly than the base and, therefore, provides a means to narrow the base width until the desired electrical properties are obtained. The more rapid emitter diffusion results from a much higher

Fig. 12 - Hometaxial-base (single-diffused) transistor structure.

The chief advantages of the hometaxial-base transistors are good voltage ratings and excellent electronic ruggedness that permit these transistors to withstand repeated high-energy power pulses. Both advantages result from the very deep graded junctions and the wide base region. The graded junction provides a benefit of either higher voltage ratings with good saturation resistances, or much lower saturation resistances at a given voltage. The electronic ruggedness arises from the moderately wide, undiffused (homogeneous) base region which allows injected charge carriers to fan out and thereby reduce charge-carrier density at the collector junction where heating effects predominate. Another advantage is that the manufacturing cost per unit of power-handling capability is relatively low, primarily as a result of large-batch processing.

Hometaxial-base transistors have a relatively low switching-speed limit because of the moderately wide base spacing, and a low upper voltage limit of about 150 to 200 volts because of punch-through limitations.

impurity level, which enhances the diffusion coefficient as compared to that of the base diffusion. Fig. 13 shows a cross section of a typical double-diffused transistor.
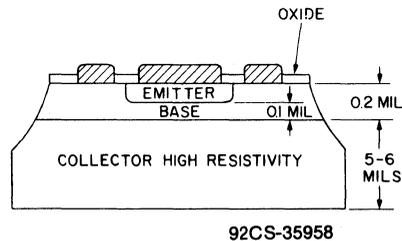
Fig. 13 - Double-diffused transistor structure.

The double-diffused structure differs from other designs in that the high-resistivity side of the collector-base junction is on the collector side; therefore, the collector voltage can be designed almost independent of the base width. The advantage of the double-diffused transistor is that very narrow non-homogeneous

or graded base widths are employed; the frequency responses of these devices, therefore, are orders of magnitude greater than those of earlier types of transistors. Double-diffused transistors, however, have a very high collector saturation resistance and relatively fragile junctions because of the thick high-resistivity collector and narrow graded base width.

Double-Diffused Planar Transistors

The double-diffused planar transistor is essentially identical to the double-diffused type with one modification in the manufacturing process. As shown in Fig. 14 the

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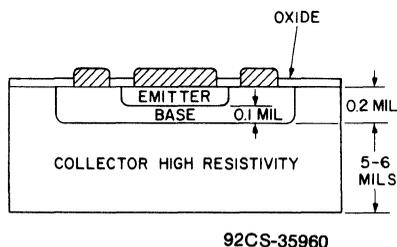
Fig. 14 - Double-diffused planar transistor structure.

collector-base junction terminates under a protective oxide layer at the surface of the silicon wafer instead of at the side. This requires one additional masking step for the base impurity. An oxide similar to the emitter masking step is also used for this mask.

The double-diffused planar transistor features drastically reduced collector leakage currents and better uniformity of device characteristics. The double-diffused planar structure allows the transistor to come very close to the low theoretical limit for silicon junction leakage current.

The disadvantages are similar to those of the double-diffused transistor, in that the double-diffused planar type has a very high collector saturation resistance and relatively fragile junctions. The double-diffused planar transistor has a collector voltage 10 to 20 per cent lower than that of mesa types with the same junction design.

Triple-Diffused Transistors

The triple-diffused structure is essentially identical to the double-diffused design except that a third diffusion is performed. The third diffusion, on the opposite side of the silicon wafer, eliminates the major disadvantage of

the double-diffused design—high saturation resistance. In the triple-diffused transistor the wafer of silicon is coated with a dopant, followed by a controlled diffusion. Fig. 15 shows a typical cross section of a triple-diffused transistor.
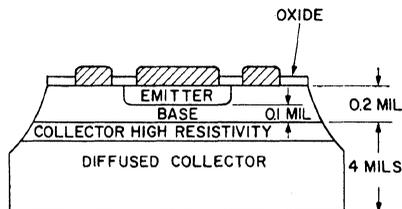
Fig. 15 - Triple-diffused transistor structure.

The principal advantage of the triple-diffused structure is that it has low saturation resistance which is of crucial importance in power transistor applications. The saturated switching speeds of this type of transistor are faster than those of the double-diffused design. Both advantages are a result of the thinning down of the high-resistivity section while the bulk of the collector is heavily doped and highly conductive. This technique, however, results in relatively fragile junctions.

Triple-Diffused Planar Transistors

The triple-diffused planar transistor, which is similar in structure to the triple-diffused transistor, incorporates a planar collector, as shown in Fig. 16. Critical cross sections of
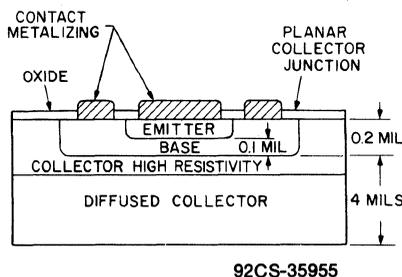
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Fig. 16 - Triple-diffused planar transistor structure.

different stages of the manufacturing processes are shown in Fig. 17.

The principal advantages of the triple-diffused planar transistor are very low leakage

STARTING WAFER — LIGHTLY DOPED n TYPE

DEEP n+ DIFFUSION

COLLECTOR DIFFUSION
n+
n
n+

REMOVE (LAP & POLISH)

LAP BACK
n
n+

SHALLOW BASE DIFFUSE

BASE DIFFUSION
p+
n
n+

EMITTER DIFFUSE — OXIDE MASK

EMITTER DIFFUSION
n+
p+
n
n+
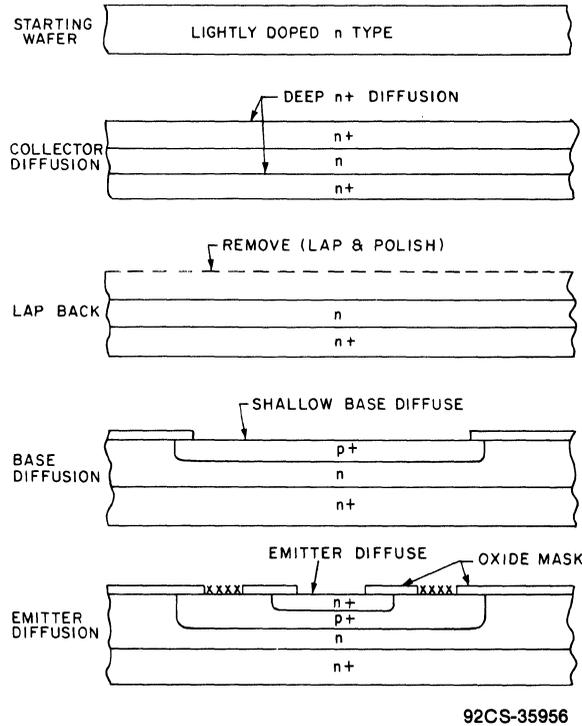
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Fig. 17 - Processing steps in the manu-facture of a triple-diffused planar transistor.

current, high-speed operation, and low sat-uration resistance. The main disadvantage is that the cost of manufacturing is higher than that of non-planar devices.

Double-Diffused Epitaxial Transistors

The double-diffused epitaxial structure is similar in appearance to the triple-diffused design, except that the diffused collector region is replaced by a heavily doped homogeneous layer referred to as the epitaxial substrate. Because of the difference in doping between the double-diffused epitaxial and triple-dif-fused structures, some improvements in switching speeds and saturation resistance can be realized. The double-diffused structure, however, has a somewhat poorer reverse "energy profile", so that its capability to withstand inductive or capacitive energy pulses is reduced.

Fig. 18 shows a cross section of a typical double-diffused epitaxial transistor, and Fig. 19 shows a planar version of the same kind of transistor.

OXIDE

EMITTER
BASE   0.1 MIL   0.2 MIL
COLLECTOR HIGH RESISTIVITY
HEAVILY DOPED SUBSTRATE   4 MILS
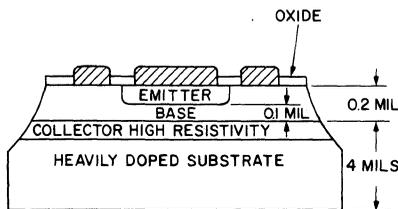
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Fig. 18 - Double-diffused epitaxial tran-sistor structure.

CONTACT METALIZING   PLANAR COLLECTOR JUNCTION   EPITAXIAL LAYER

OXIDE

EMITTER
BASE   0.1 MIL   0.2 MIL
COLLECTOR HIGH RESISTIVITY
HEAVILY DOPED SUBSTRATE   8 MILS
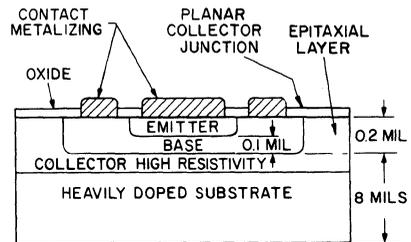
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Fig. 19 - Double-diffused epitaxial planar transistor structure.

Epitaxial-Base Transistors

The epitaxial-base structure uses epitaxial layers in the actual formation of the base-collector junction. A single diffusion of the emitter completes this relatively simple design. A layer of impurity (opposite to the substrate impurity) is epitaxially grown on the highly doped substrate. An oxide masking and emitter diffusion into this epitaxial layer completes the construction. Fig. 20 shows a typical cross section of an epitaxial-base power transistor.

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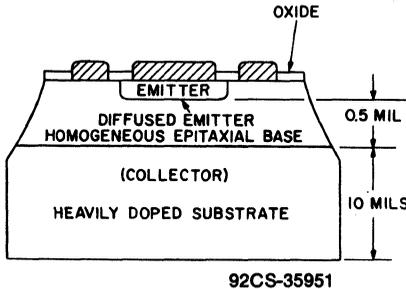
Fig. 20 - Epitaxial-base transistor structure.

The principal advantage of the epitaxial-base structure, compared to the double-diffused designs, is that it is electronically more rugged (able to withstand energy pulses) as a result of the wider and homogeneous base region. In comparison to the hometaxial structure, the epitaxial-base type has significantly higher frequency response and the ability to carry higher currents for an equivalent emitter area.

The disadvantage of the epitaxial-base design is that it is limited by low voltage ratings imposed by the constraint of the abrupt base-collector junction formed between the heavily doped collector substrate and the epitaxially deposited base layer. The low voltage rating also results from the thin base width necessary for adequate current gain which reduces voltage limits because of punch-through effects. The epitaxial-base transistor also suffers from moderate collector leakage-current levels resulting from the abrupt step junctions and mesa construction.

Multiple-Epitaxial-Base Transistors

The multiple-epitaxial-base structure is similar to the epitaxial-base transistor, but has the added feature of a high-resistivity epitaxial layer for the active collector region. The multiple epitaxial-base transistor is fabricated from a heavily doped silicon wafer on which alternate layers of p-n or n-p high-resistivity silicon are epitaxially grown to create a $\pi - \nu$ or a $\nu - \pi$ base-collector junction. An emitter area is then diffused into the structure. Fig. 21 shows the various stages in

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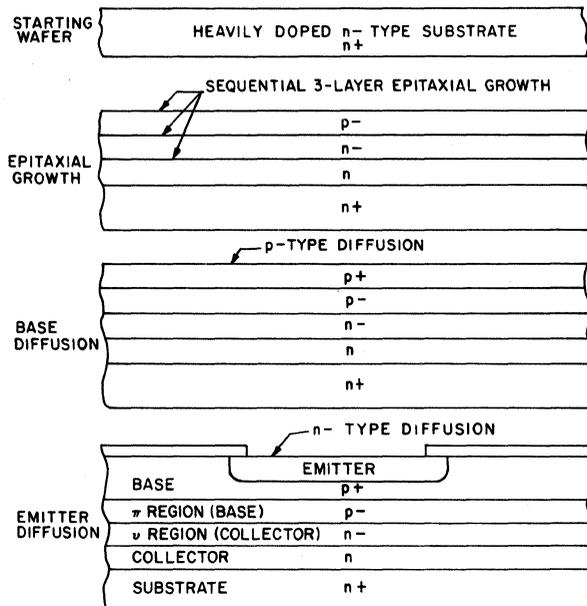
Fig. 21 - Processing steps in the manufacture of a multiple-epitaxial-base transistor.
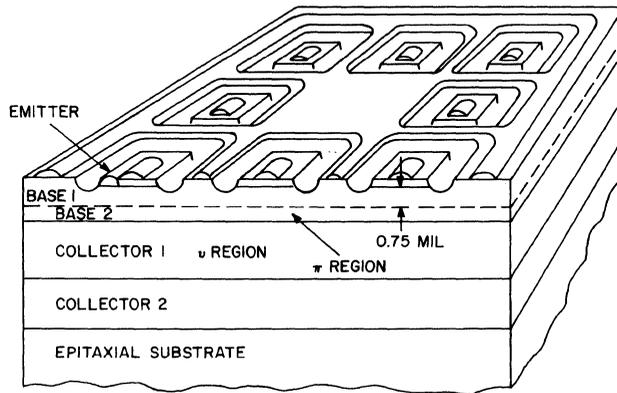
Fig. 22 - Multiple-epitaxial-base transistor
structure.

the manufacture of the multiple-epitaxial-base transistor structure, and Fig. 22 shows a typical cross section of this type of device.

The principal advantage of the multiple-epitaxial-base structure is that it has high voltage ratings with good current carrying abilities and excellent power-handling capabilities at high voltages (second breakdown). The higher voltage ratings result because the transistor uses both the base and the collector regions to support the applied collector voltage. The good current-handling characteristic results from the fact that lower collector resistivity can be used for equivalent voltage ratings, as compared to double-diffused epitaxial designs. The lower collector resistivity also minimizes high-current fall-off effects that result from base widening. The excellent second breakdown characteristic results from the moderately wide base width and partial homogeneous base doping, which allows more charge-carrier fan-out (diffusion) and reduced current densities at the collector junction where heating effects predominate.

The principal disadvantage is that the cost of manufacturing the multiple epitaxial-base transistor is relatively high.

Multiple-Epitaxial
Double-Diffused Transistors

The multiple epitaxial double-diffused structure is almost identical to the double-diffused epitaxial design, with the exception that multiple epitaxial layers are used in the collector region, instead of a single collector layer. The top collector layer is a thin, high-resistivity layer followed by one or more thin,

but more heavily doped, layers. These more heavily doped layers are grown sequentially in an epitaxial reactor system onto a thick, heavily doped silicon substrate wafer. Fig. 23 shows the various stages in manufacture of the multiple epitaxial double-diffused structure, and Fig. 24 shows a typical cross section of the completed transistor.

The advantages of the multiple epitaxial double-diffused structure include those of the double-diffused epitaxial design (high speed and low saturation), as well as the significant advantages of higher collector-junction voltage
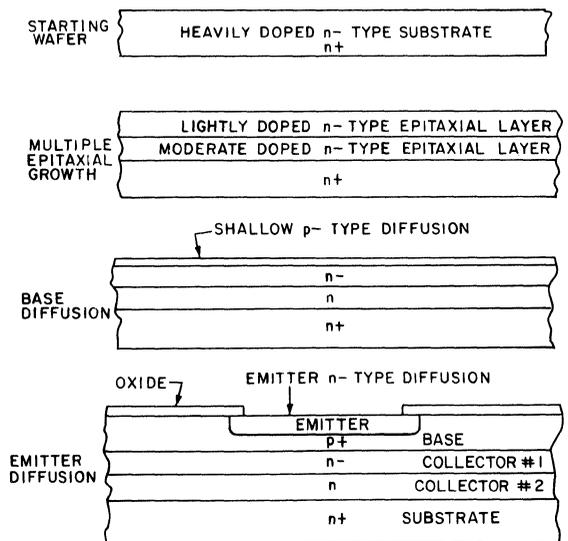
Fig. 23 - Processing steps in the manu-
facture of a multiple-epitaxial
double-diffused transistor.

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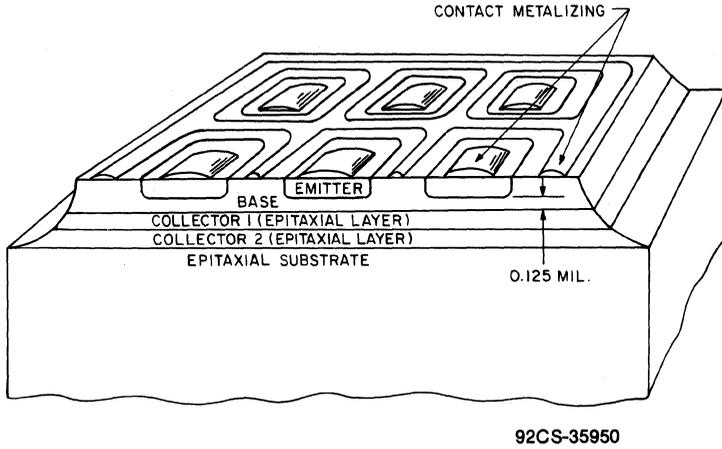
Fig. 24 - Multiple-epitaxial double-diffused transistor structure.

ratings, and increased electrical ruggedness. The electrical ruggedness (supplied by the additional collector layers) becomes even more of a factor during power switching with inductive loads in the 100-to-200-volt range where significant inductive energies (reverse second breakdown) may have to be handled by the transistor.

The disadvantages of the multiple epitaxial double-diffused transistor are the moderate-to-high cost per unit and the moderate leakage in the structure.

GEOMETRIES

The topography of a transistor is referred to as its geometry. This transistor geometry, in conjunction with its structure, establishes most of the fundamental transistor electrical, ther-

mal, and economic properties. Proper geometric design of a transistor allows for many compromises, which may result in a variety of advantages and disadvantages from different structures.

The basic premise for most geometric designs for power transistors is to increase current handling per unit area of device. This condition results in lower-cost designs or, as in high-frequency transistors, higher-speed operation as a result of the smaller device areas.

Power transistor geometries have evolved from the very early inefficient "ring-dot" configurations to the present-day sophisticated "overlay" concepts. Fig. 25 shows some typical geometry milestones in this evolutionary cycle.

The early geometries were characterized by simple shapes, large dimensional tolerances,

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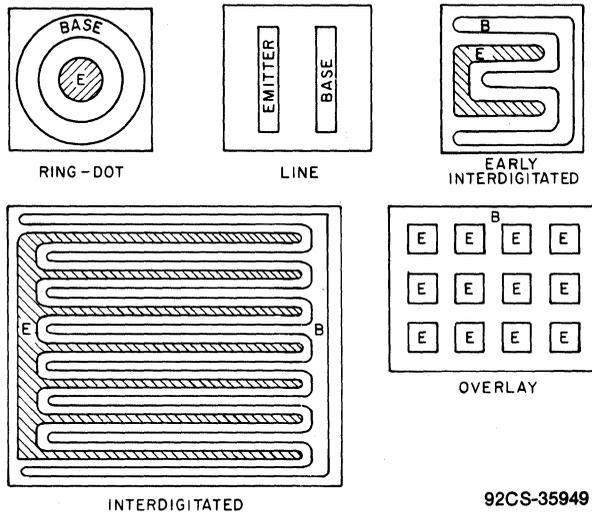
Fig. 25 - Typical geometries in the development of transistors.

and poor utilization of active regions. As the state of the art in fine-line mask making and wafer printing improved, the geometries became more involved, with much finer dimensions.

Certain device structures have constraints on how fine the emitter geometry can be made. Refinement of emitters is governed by the space needed for emitter and collector mesas and by the thickness of oxide masks needed for deep diffusion, as well as by other factors.

SPECIAL PROCESSING TECHNIQUES

Silicon power transistors are now taking on new dimensions in performance. New processing techniques including ion implanted, diffused junctions, polysilicon field shields, glass passivation, moated planar junctions, aluminum-titanium-nickel metallization, and high lifetime wafer processing are some of the advanced technologies that are responsible.

Neutron Doping

The voltage and current performance of a high-voltage transistor is critically dependent on the crystal resistivity in the n-type collector region of the device.

Conventional n-type float-zone crystal-growing techniques tend to produce large variations in doping levels due to the low distribution coefficient of the n-type dopant (phosphorous) and the varying thermal equilibrium conditions at the growth interface.

Phosphorous doping by thermal neutron transmutation is a doping technique in which a flux of thermal neutrons is irradiated on a high-resistivity, undoped single crystal to fractionally transmutate silicon into phosphorous.

The crystal is subsequently annealed to remove radiation-induced defects in the lattice. The technique is cost-effective at low doping levels below $\sim 1 \times 10^{14}/cm^3 (\rho > 50 \ \Omega \ cm)$ producing wafers in production quantities with resistivity variations less than 10 per cent.

Ion Implantation

Control of base and collector doping profiles is also an important aspect of transistor processing. The use of ion implantation to achieve precise doping levels for the base and collector diffusion sources has eliminated critical high-temperature chemical-deposition processes, resulting in better yields and tighter parameter distributions. A schematic of a basic ion implant machine is shown in Fig. 26.
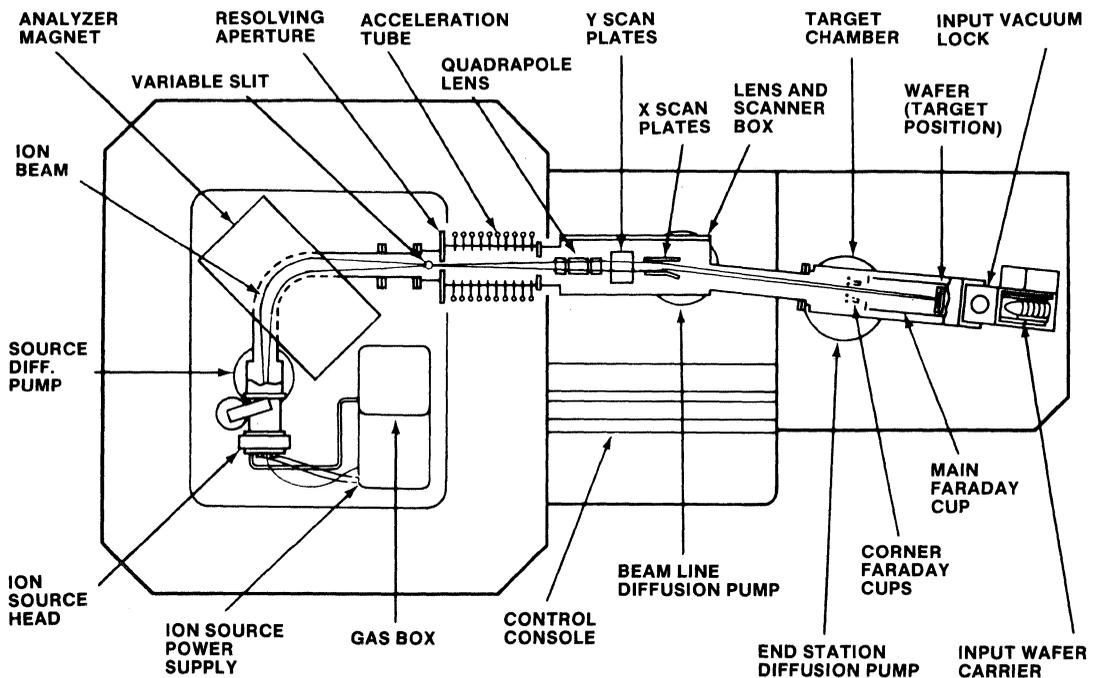
92CM-35946

Fig. 26 - Basic ion implantation machine.

The machine provides simple electronic control of the incident beam of doping ions. Mass analysis is used to assure extreme purity of the ion beam. Doping accuracy is better than one per cent compared to about 10 per cent for typical chemical processes. Recently, high current machines have become commercially available, providing sufficient capability for most power device doping.

With the ion-implantation technique, atomic species are ionized, accelerated to high velocities under vacuum by the application of electrostatic fields, and directed against the surface of a target material where they penetrate and come to rest in a shallow layer below the surface.

Diffusion Process

The diffusion process developed for production of high-voltage transistors contains only two diffusion steps as shown in Fig. 27. The ion-implanted base and collector regions are diffused simultaneously from both sides of the wafer. This high-temperature (1300° C) process forms the basic high-voltage diode structure. The ion-implanted emitter, base-contact, and collector-contact regions are then diffused in a second short diffusion step at a moderate temperature (1200° C) producing the complete n-p-n transistor structure. Standard photolithographic and silicon dioxide masking techniques are used to restrict the diffusion to the desired regions.

Surface Electric-Field Control

Once the requirements are met for voltage breakdown capability in bulk silicon, special consideration of the termination of the junction with the silicon surface must be taken because the peak surface electric field that initiates avalanche breakdown is generally significantly lower than the corresponding bulk electric field. Several common methods of reducing surface fields are shown in Fig. 28. While no method is completely successful in eliminating the surface effect, each method is capable of surface breakdown voltage within 90-95 per cent of the bulk capability. For reasons described, the **planar depletion moat** was chosen as the best structure for a passivated high-voltage transistor.

The reverse-bevel technique, shown in Fig. 28(a), is used by most manufacturers of high-voltage transistors. Surface fields are reduced because the field is spread over a larger surface area due to the approximately 30° bevel. One drawback of the technique is that it requires a mechanical grinding step to produce an accurate taper, and mechanical processes are generally expensive in comparison with other semiconductor processes. Hard-glass passivation of the junction is not practical due to the position of the junction, and devices of this type are generally non-passivated. The reverse-bevel technique, however, is proven and has withstood the test of time both in volume production and in device application.

The **planar depletion moat** structure shown in Fig. 28(d) is an excellent method of high-voltage junction termination both from the standpoint of pellet area utilization and the ease of hard-glass passivation. The junction is located in a plane parallel to the top surface of the pellet several mils from the mesa-etch
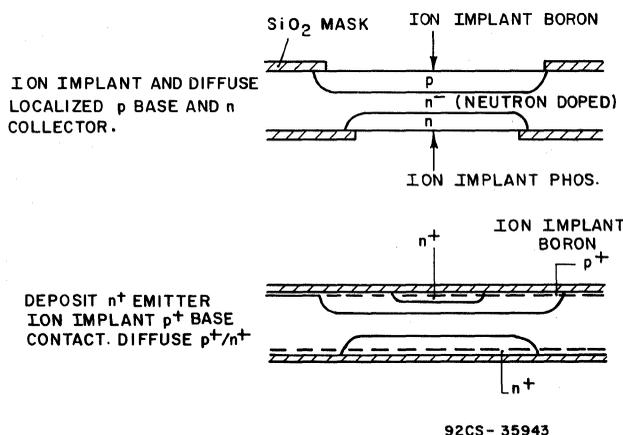
Fig. 27 - Simplified diffusion process.

REVERSE BIAS DEPLETION REGION

(a) POSITIVE BEVEL

E_S - SURFACE ELECTRIC FIELD

(b) PLANAR GUARD BANDS

(c) MESA π-υ

(d) PLANAR DEPLETION MOAT

RESTRICTED COLLECTOR

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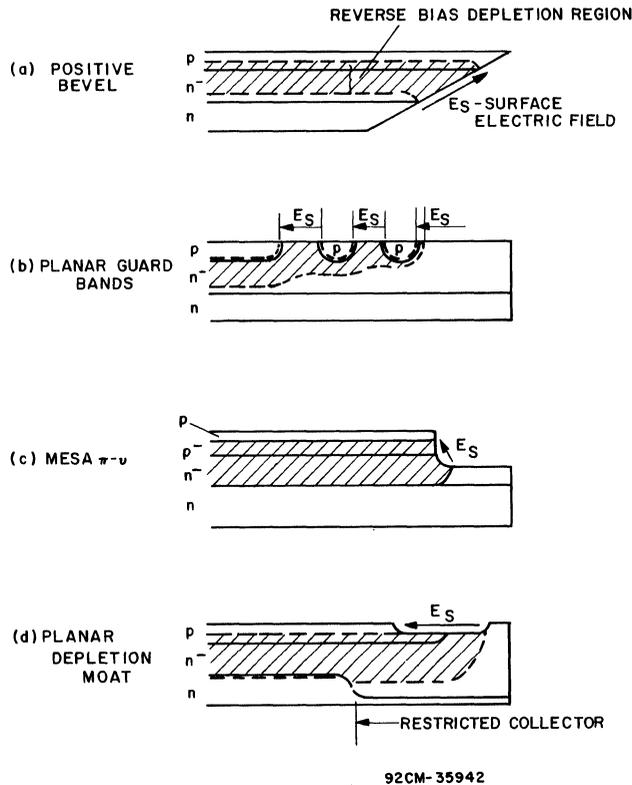
Fig. 28 - Common methods of reducing surface electric fields.

discontinuity. This arrangement minimizes the adverse effects of certain variables in the passivation process such as photoresist adherence, mechanical stresses in the passivation layers, and glass coverage. Near-theoretical breakdown can be achieved with proper etch-depth control.

Glass Passivation

The operating voltage of a solid-state device is generally limited by the surface breakdown voltage and the stability of the surface when the device is subjected to high voltage and high temperature. Bulk silicon can withstand an electric field in the order of 500 volts per mil before breakdown occurs; the surrounding medium and its interface, however, have much lower breakdown potentials. Even when arcing or breakdown of the surface does not occur, high electric fields can cause ionization of atoms or molecules on the surface and migration of ions along the surface.

Ion migration is actually a leakage current that, although of negligible magnitude, results in an accumulation of negative and positive static charges on the pellet surface. These static charges induce opposite-polarity mobile charges beneath the surface within the pellet body. It is the flow of these induced mobile charges within the body of the pellet, rather than the flow of charge on the pellet surface, that actually constitutes the leakage current which is detrimental to a device operated at high voltages and high temperatures. Glass passivation is used to assure maximum surface breakdown voltage and maximum surface stability. The glass protects the surface of the silicon pellet from breakdown or arcing and forms a barrier that prevents migration of ions to the silicon surface. Fig. 29 shows a cross section of a typical glass-passivated transistor pellet.

Sipos/Glass Passivation

In any high-voltage device, fringing electric fields external to the pellet are important in determining performance and reliability. Mobile ionic contaminants on the surface can play havoc with the electrical characteristics causing high leakage, unstable voltage break-
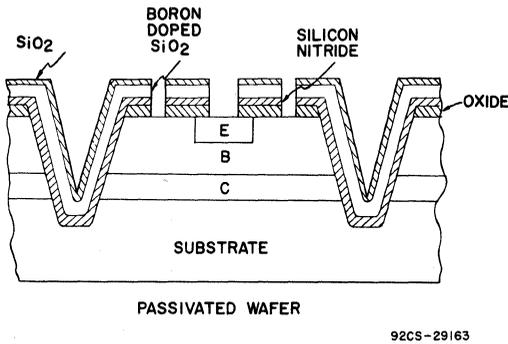
Fig. 29 - Glass-passivated transistor pellet.

down and, in severe cases, complete destruction of the device. This condition is especially true in a non-hermetic environment. To desensitize the junction from external effects, the silicon surface can be passivated with insulating or semi-insulating materials which bond well with the silicon and do not contain mobile contaminants which can be thermally activated at the device's operating temperature.

Passivation of the junction serves another important economic purpose. Because the passivated system hermetically seals the device in chip form, the hard-glass-passivated device can be tested, categorized, and inventoried at the pellet stage, reducing inventory carrying costs and enabling more effective response to varying market conditions.

A multilayer passivation system called SOGO was developed to meet the performance and reliability requirements of high-voltage devices. The basic components of the SOGO system are shown in Fig. 30. The primary passivation layer is a thin film of semi-insulating polycrystalline oxygen doped silicon (Sipos) which is formed by Low Pressure Chemical Vapor Deposition (LPCVD) through the reaction of nitrous oxide (N_2O) and silane (SiH_4).

The use of LPCVD primary passivant is also advantageous from the manufacturing standpoint. High throughput, excellent uniformity and reproducibility are realized with the LPCVD system.
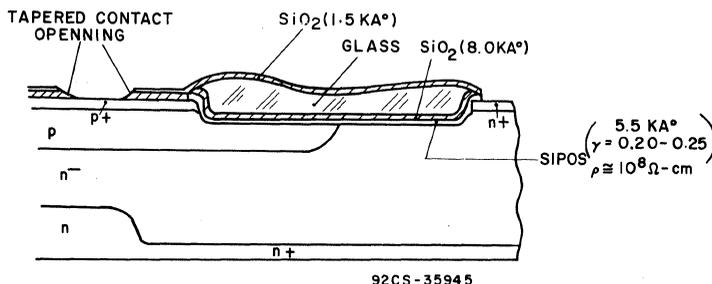
Tri-Metal Metallization

The wide collector region and high lifetime result in large amounts of stored charge which tend to restrict switching performance of high-voltage devices. In order to achieve fast switching and minimize turn-off tails (which lead to high power dissipation in turn-off), RCA high-voltage, high-current transistors use a finely subdivided discrete emitter structure and employ a high-conductivity, solderable Al/Ti/Ni metallization system, shown in Fig. 31, on the emitter-base side of the device with metal-over-oxide capability to access the discrete emitters. In this metal system, a thick layer of aluminum is used to bond to the silicon and silicon dioxide and provide high lateral conductivity, minimizing voltage drops in the base and emitter metal which would tend to create current non-uniformities at high current injection levels. The titanium layer serves as a buffer region preventing the formation of brittle aluminum/nickel intermetallics during the metal alloying process. Solder contact is readily made to the nickel layer. On the collector side of the device a layer of nickel is deposited over a titanium layer to provide a high-conductivity surface for solder mounting to a heat sink. The metal layers are deposited in an electron-gun vacuum evaporator and metal definition is accomplished using photolithographic techniques. A single-step metal etch is employed for ease of manufacturing. This metal system combines the advantages of high conductivity, fine-line geometry, and metal over oxide capability of the aluminum metal system, with the advantages of a rugged nickel-lead solder mounting and clip bonding assembly process.

Fig. 30 - Sipos-Oxide-Glass-Oxide (SOGO) passivation system.

NICKEL
TITANIUM
ALUMNUM

TITANIUM
NICKEL

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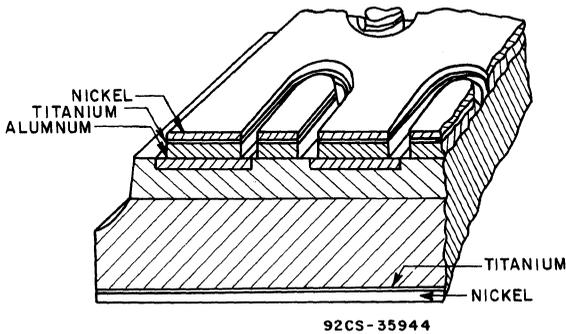
Fig. 31 - Cross section of transistor pellet employing high-conductivity metallization system.

RCA SwitchMax Power Transistors

Many of the special processing techniques described in the previous paragraphs are employed to advantage in the RCA "SwitchMax" series of power-switching transistors. These transistors employ a multiple-layer epitaxial, double-diffused collector structure that is specially designed for high-current, high-speed switching. They are fully characterized for switching applications in off-the-line switching power supplies, converters, and pulse-width-modulated switching regulators.

The RCA SwitchMax transistors feature high voltage capability, fast switching speeds, and high safe-operating-area (SOA) ratings; they are 100 per cent tested for the parameters essential to the design of power-switching circuits. Table II lists the RCA SwitchMax series together with important switching characteristics and voltage and current ratings. As indicated in the table, switching parameters are tested at elevated temperatures ($T_C \geq 100°$ C), as well as at room temperature, to provide limit values necessary for worst-case design.

The fine-geometry emitter, together with minimum base and collector sheet resistivities compatible with voltage-breakdown requirements, assures excellent high-current and fast-switching capability. The low collector resistivity and carefully controlled layer thicknesses minimize the fall-off in gain at high currents that results from base-widening effects. A controlled-lifetime process used in the production of the SwitchMax pellets results in higher gain for a given base width and assures stable current gain during operation at elevated temperatures.

The ruggedness of the SwitchMax transistors is enhanced by careful design of the emitter periphery to assure low current density, use of wide base widths so that collector current is spread over more of the pellet area, a special emitter-pad design that provides "dynamic" emitter ballasting during switching, and graded n-type layers for collector ballasting.

The SwitchMax transistors employ the **high-conductivity trimetal metallization** system, previously shown in Fig. 31, that permits a designer to solder-mount pellets and chips for ruggedness and still retain a high-conductivity, fine-geometry metallization pattern. Potential weaknesses in the system are detected by infrared analyses, which enable establishment of optimum patterns to assure uniform base-current distribution over the entire transistor active area. The SwitchMax transistors employ a **unique, proprietary glass-passivation system** (similar to that shown earlier in Fig. 30) that assures low surface leakage, increased voltage capability, and improved high-temperature performance.

SwitchMax Transistor Classification Chart

Table II — SwitchMax Transistor Classification Chart

I_C(sat)		1A	4A	5A	5A	6A	8A	10A	.15A	25A
V_{CEV}	260 V	—	—	—	—	—	—	—	—	2N6686
	280 V	—	—	—	—	—	—	—	—	2N6687
	300 V	—	—	—	—	—	—	—	—	2N6688*
	450 V	2N6771△	—	2N6671■	—	—	—	2N6674■	2N6676■	—
		BUW40△	—	2N6738△	—	—	—		2N6774	—
		—	—	BUW41△	—	—	—	—		—
	550 V	2N6772△	—	2N6672	—	—	—	—	2N6677	—
		BUW40A△	—	2N6739△	—	—	—	—	2N6775	—
		—	—	BUW41A△	—	—	—	—	—	—
	650 V	2N6773△	—	2N6673■	—	—	—	2N6675■	2N6678■	—
		BUW40B△	—	2N6740△	—	—	—		2N6776	—
		—	—	BUW41B△	—	—	—	—	—	—
	800 V	—	BUX31	—	2N6751	BUX32	BUX33	—	—	—
		—	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—	—
	850 V	—	—	—	2N6752	—	—	—	—	—
	900 V	—	BUX31A	—	2N6753	BUX32A	BUX33A	—	—	—
		—	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—	—
	1000 V	—	BUX31B	—	2N6754	BUX32B	BUX33B	—	—	—
		—	—	—	—	—	—	—	—	—
		—	—	—	—	—	—	—	—	—
Characteristics	**Temp., T_C**	**Limits**								
I_{CEV} (max) at $V_{CE}=V_{CEV}$	25°C	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.05 mA
	100°C	—	1 mA	—	1 mA	1 mA	1 mA	2 mA	1 mA	—
	125°C	1 mA	—	1 mA	—	—	—	—	—	0.5 mA
V_{CE}(sat)(max) at I_C (sat)	25°C	1 V	1 V	1 V	1 V	1 V	1 V	1 V	1 V	1.5 V
	100°C	—	1.5 V	—	1.5 V	1.5 V	1.5 V	2 V	2 V	—
	125°C	2 V	—	2 V	—	—	—	—	—	1.5 V
t_r (max) at I_C (sat)	25°C	0.2 µs	0.45 µs	0.5 µs	0.45 µs	0.45 µs	0.45 µs	0.6 µs	0.6 µs	0.35 µs
	100°C	—	0.6 µs	—	0.6 µs	0.6 µs	0.6 µs	1 µs	1 µs	—
	125°C	0.5 µs	—	0.8 µs	—	—	—	—	—	0.6 µs
t_s (max) at I_C (sat)	25°C	2.5 µs	3 µs	2.5 µs	3 µs	3 µs	3 µs	2.5 µs	2.5 µs	0.8 µs
	100°C	—	4 µs	—	4 µs	4 µs	4 µs	4 µs	4 µs	—
	125°C	4.5 µs	—	4 µs	—	—	—	—	—	2.5 µs
t_f (max) at I_C (sat)	25°C	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.5 µs	0.5 µs	0.5 µs
	100°C	—	0.7 µs	—	0.7 µs	0.7 µs	0.7 µs	1 µs	1 µs	—
	125°C	1.3 µs	—	0.8 µs	—	—	—	—	—	0.8 µs
t_c (max) at I_C (sat)	25°C	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.5 µs	0.5 µs	0.5 µs
	100°C	—	0.8 µs	—	0.8 µs	0.8 µs	0.8 µs	0.8 µs	0.8 µs	—
	125°C	1.3 µs	—	0.8 µs	—	—	—	—	—	0.8 µs

All SwitchMax transistors are supplied in JEDEC TO-204MA/TO-3 packages, except as noted below: *I_C (sat) = 20 A.
△Supplied in JEDEC TO-220AB plastic package. ■MIL Approved:
MIL-S-19500/536 — 2N6671, 2N6673
MIL-S-19500/537 — 2N6674, 2N6675
MIL-S-19500/538 — 2N6676, 2N6678

Packaging, Handling, and Mounting

RCA power transistors are supplied in both hermetic packages (metal and/or ceramic) and plastic packages. The photographs in Fig. 32 show the packages that are used for these devices.

The volume and area of the package are important in determining the power dissipation capability of a power transistor; chip mounting and encapsulation are also factors. The maximum allowable power dissipation in the device is limited by its junction temperature, which depends upon the ability of the thermal circuit to conduct heat away from the chip. The predominant mode of heat transfer is conduction through the silicon chip and through the case; the effects of internal free convection and radiation and lead conduction are small and may be neglected. The **thermal resistance** from pellet to case depends upon the pellet dimensions and the package configuration.

When the device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance. Thermal considerations require that there be a free flow of air around the device and that the power dissipation be maintained below that which would cause the junction temperature to rise above the maximum rating. When the device is mounted on a heat sink, however, care must be taken to assure that all portions of the thermal circuit are considered.

Fig. 33 shows the thermal equivalent circuit for a heat-sink-mounted device. This figure shows that the junction-to-ambient thermal circuit includes three series thermal-resistance components, i.e., junction-to-case, $R_{\theta JC}$; case-to-heat-sink, $R_{\theta CS}$; and heat-sink-to-ambient, $R_{\theta SA}$. The junction-to-case thermal resistance of the various device types is given in the individual technical bulletins on specific types. The heat-sink-to-ambient thermal resistance can be determined from the technical data

provided by the heat-sink manufacturer, or from published heat-sink nomographs. The case-to-heat-sink thermal resistance depends on several factors, which include the condition of the heat-sink surface, the type of material and thickness of the insulator, the type of thermal compound, the mounting torque, and the diameter of the mounting hole in the heat-sink.

T_J = junction temperature
T_C = case temperature
T_S = heat-sink temperature
T_A = ambient temperature
$R_{\theta JC}$ = junction-to-case thermal resistance
$R_{\theta CS}$ = case-to-heat-sink thermal resistance
$R_{\theta SA}$ = heat-sink-to-ambient thermal resistance

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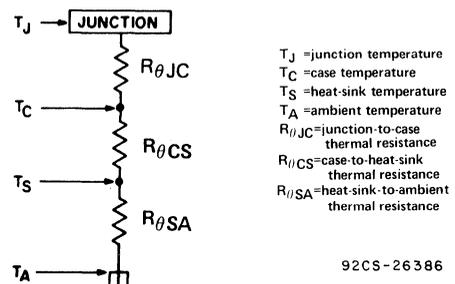
Fig. 33 - Thermal equivalent circuit for a solid-state device mounted on a heat sink.

HERMETIC PACKAGES

The selection of a particular method for mounting and connection of power transistors in equipment depends on the type of package involved; on the equipment available for mounting and interconnection; on the connection method used (soldered, welded, crimped, etc.); on the size, shape, and weight of the equipment package; on the degree of reliability and maintainability (ease of replacement) required; and, of course, on cost considerations.

In the following discussion, the information given applies to the package rather than the device unless otherwise specified. In other words, the discussion of handling and mounting of the TO-5 package is understood to cover mounting of the transistors.

JEDEC TO-3/
TO-204MA

2N6032, 2N6033
Modified TO-3
(0.060-In. Dia. Pins)

TO-39/TO-5
with Heat Radiator

TO-39/TO-5
with Flange

JEDEC
TO-39/TO-
205MD

JEDEC TO-66/
TO-213MA

TO-66 with Heat Radiator

VERSAWATT
JEDEC TO-220AA

VERSAWATT
JEDEC TO-220AB

RADIAL
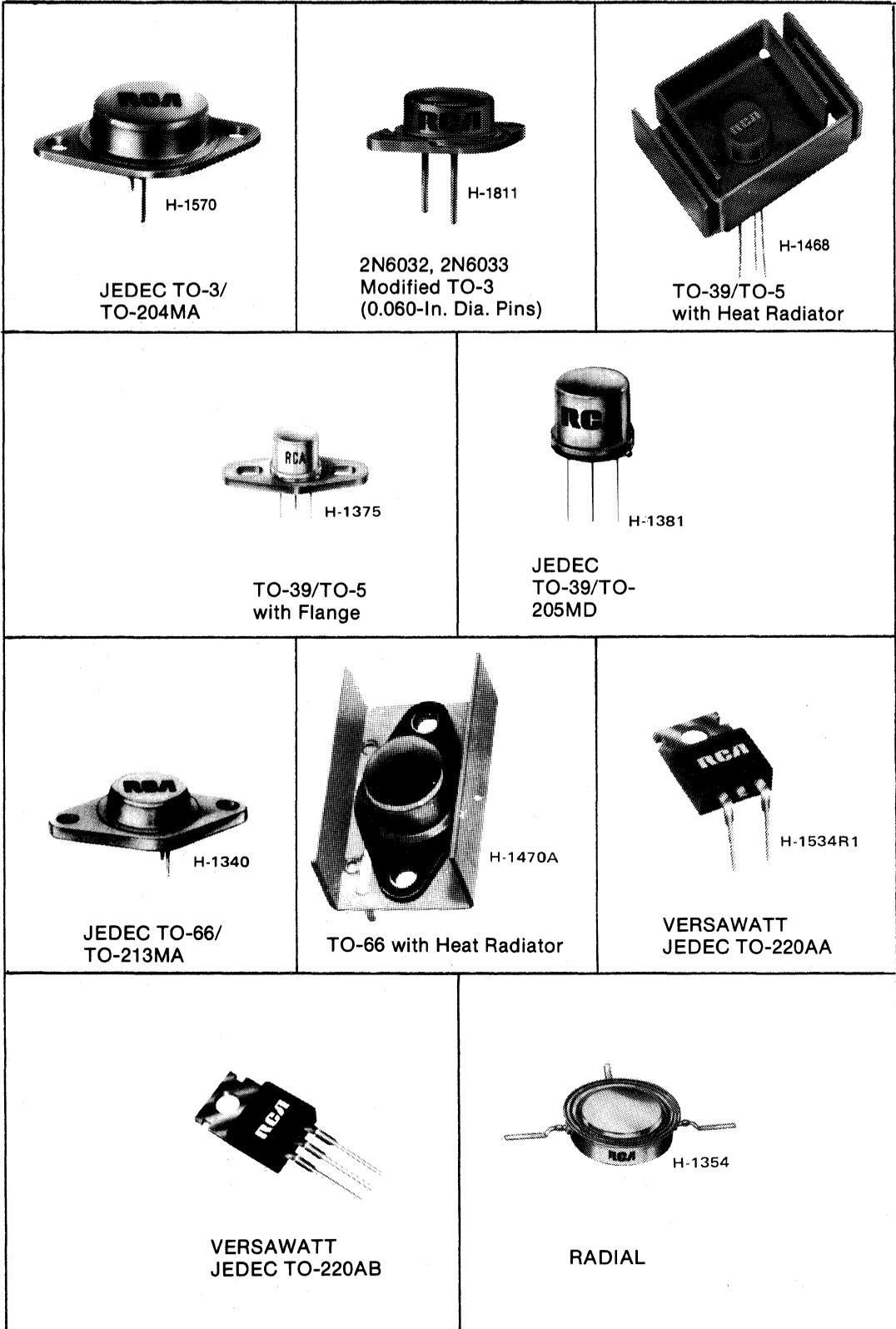
Fig. 32 - RCA power transistor packages.

Packages with Flexible Leads

Some power transistor packages have flexible leads; these leads are usually soldered to the circuit elements. In all soldering operations, some slack or an expansion elbow should be provided in each lead to prevent excessive tension on the leads. Excessive heat should be avoided during the soldering operation to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of long-nosed pliers.

Although flexible leads can be bent into almost any configuration to fit any mounting requirement, they are not intended to take repeated bending. In particular, repeated bending at the point at which the lead enters the case should be avoided. The leads are not especially brittle at this point, but the sharp edge of the case produces an excessively small radius of curvature in a bend made at the case. Repeated bending with a small radius of curvature at a fixed point will cause fatigue and breakage in almost any material. For this reason, right-angle bends should be made at least 0.020 inch from the case. This practice will avoid sharp bends and maintain sufficient electrical isolation between lead connections and header. A safe bend can be assured if the lead is gripped with pliers close to the case and then bent the requisite amount with the fingers, as shown in Fig. 34. When the leads of a

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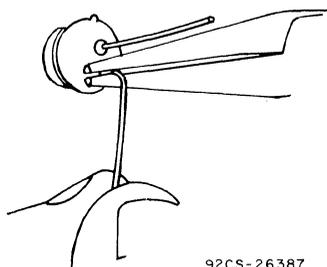
Fig. 34 - Method of bending leads on a flexible-lead package.

number of devices are to be bent into a particular configuration, it may be advantageous to use a lead-bending fixture to assure that all leads are bent to the same shape and in the correct place the first time, so that there is no need for the repeated bending.

Transistors should be mounted on heat sinks when they are operated at high power levels. An efficient heat-sink method for transistors in JEDEC TO-39 packages is to provide intimate contact between the heat sink and at least one-half of the base of the device opposite the leads. TO-39 packages can be mounted to the heat sink mechanically, with glue or an epoxy adhesive. Transistors should not be soldered to the heat sink.

Packages with Mounting Flanges

The mounting flanges of packages such as the JEDEC-type TO-3 or TO-66 often serve as the collector terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Under no circumstances, however, should the mounting flange be soldered directly to the heat sink or chassis because the heat of the soldering operation could permanently damage the device.

Such devices can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seats provided care is taken to conduct excessive heat away from the seals; otherwise, the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must provide sufficient thermal conduction to the ambient environment to assure that the temperature of the device mounting flange does not rise above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

Fig. 35 shows methods of mounting flanged packages. Zinc-oxide-filled silicone grease should be used between the device and the heat sink to eliminate surface voids and to help conduct heat across the interface. Although glue or epoxy adhesive provides good bonding, a significant amount of thermal resistance may exist at the interface. To minimize this interface resistance, an adhesive material with low thermal resistance, such as Hysol* Epoxy Patch Material No. 6C or Wakefield* Delta Bond No. 152, or their equivalent, should be used.

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*Products of Hysol Corporation, Olean, New York, and Wakefield Engineering, Inc., Wakefield, Massachusetts, respectively.

TO-204MA/TO-3

2 SCREWS, 6-32

DF377A
MICA INSULATOR

HEAT SINK
(CHASSIS)

DF378F
2 NYLON INSULATING
BUSHINGS
I. D. = 0.156 in. (4.00 mm)
SHOULDER DIA. = 0.250 in.
(6.40 mm) MAX.,
SHOULDER THICKNESS
= 0.050 in. (1.27 mm) MAX.

2 METAL WASHERS

2 LOCK WASHERS

2 HEX. NUTS

2 SOLDER LUGS

2 HEX. NUTS
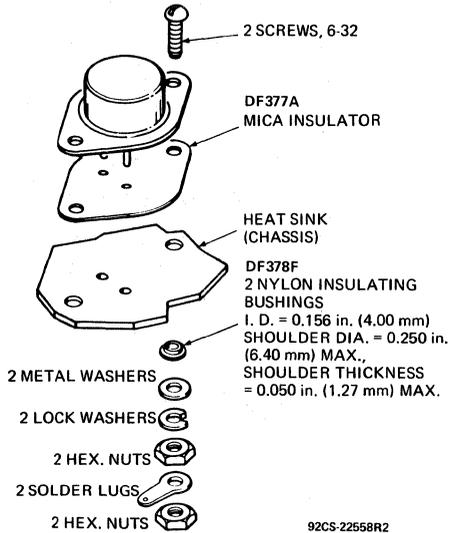
92CS-22558R2

NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING
FLANGE IS 12 in.-lbs. (0.14 kgf m).

MODIFIED TO-3

2 SCREWS, 6-32

DF238A
MICA INSULATOR

HEAT SINK

DF378F
2 NYLON INSULATING
BUSHINGS
I.D. = 0.156 (4.00)
SHOULDER DIA. = 0.250
(6.40) MAX.,
SHOULDER THICKNESS
= 0.050 (1.27) MAX.

2 METAL WASHERS

2 LOCK WASHERS

2 HEX. NUTS

1 SOLDER LUG

2 HEX. NUTS
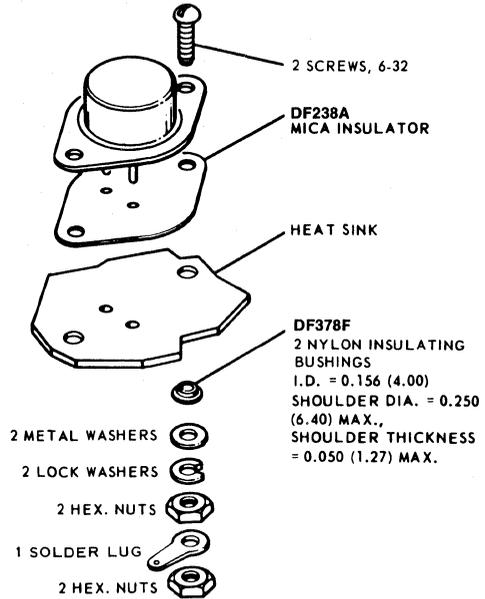
92CS-22556R1

TO-204MA/TO-3
With 200-mil diameter pin
isolation

2 SCREWS, 4-40

DF435A
MICA INSULATOR

HEAT SINK
(CHASSIS)

DF436A
2 NYLON INSULATING
BUSHINGS
I.D.=0.120 in. (3.05 mm)
SHOULDER DIA.=0.310 in.
(7.87 mm) MAX.,
SHOULDER THICKNESS
=0.064 in. (1.63 mm) MAX.

2 METAL WASHERS

2 LOCK WASHERS

2 HEX. NUTS

2 SOLDER LUGS

2 HEX. NUTS
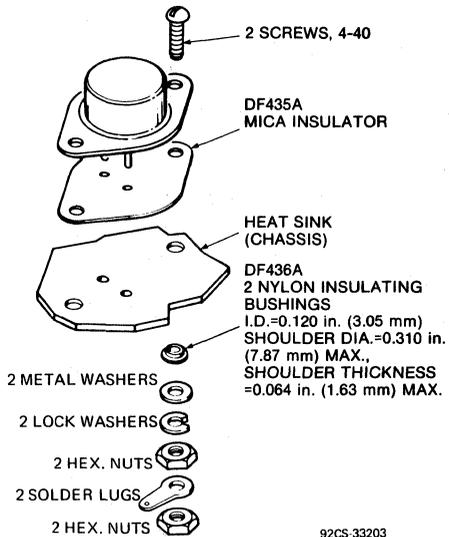
92CS-33203

NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING
FLANGE IS 8 in.-lbs. (0.09 kgf m).

TO-205MA/TO-5
TO-205MD/TO-39
With Flange

2 SCREWS, 4-40

DF063A
MICA INSULATOR

HEAT SINK

DF378G
2 NYLON INSULATING BUSHINGS
I.D. = 0.130 (3.30)
SHOULDER DIA. = 0.218 (5.54)
SHOULDER THICKNESS =
0.050 (1.27) MAX.

2 METAL WASHERS

2 LOCK WASHERS

2 HEX. NUTS
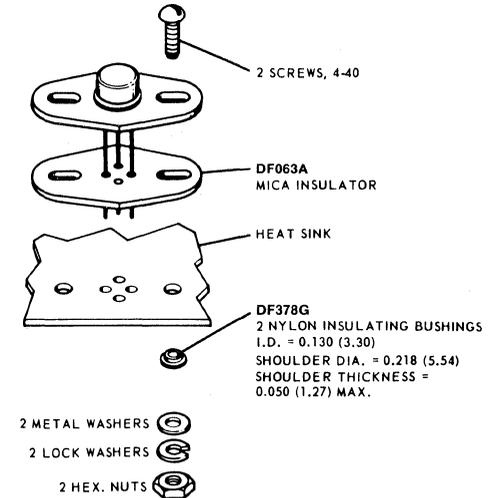
Note: Maximum torque applied
to mounting flange is
8 in.-lb. (0.09 kgfm).

92CS-22567E

*Fig. 35 - Methods of mounting flanged-
packaged types.*

TO-213MA/TO-66

2 SCREWS, 6-32

DF031A
MICA INSULATOR

HEAT SINK

DF378F
2 NYLON INSULATING BUSHINGS
I.D. = 0.156 (4.00)
SHOULDER DIA. =
0.250 (6.40) M AX.
SHOULDER THICKNESS =
0.050 (1.27) MAX.

2 METAL WASHERS

2 LOCK WASHERS

2 HEX. NUTS

1 SOLDER LUG

2 HEX. NUTS
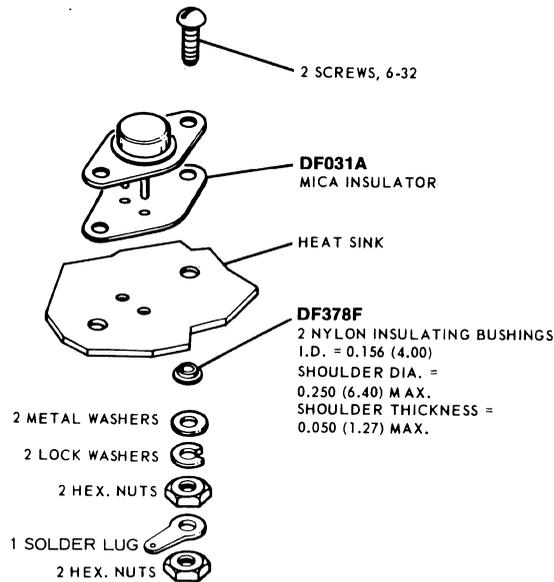
**Note: Maximum torque applied to mounting flange is
12 in.-lb. (0.14 kgfm)**

92CS-22560R5

TO-220AB

SCREW, 6-32

NR231A
RECTANGULAR METAL
WASHER

DF103B
MICA INSULATOR
HOLE DIA. = 0.145-0.141 in.
(3.68-3.58 mm)

HEAT SINK
(CHASSIS)

DF378F

INSULATING SHOULDER WASHER
I.D. = 0.156 in. (4.00 mm)
SHOULDER DIA. =
0.250 in. 6.35 (mm) MAX.

METAL WASHER

LOCK WASHER

HEX NUT

SOLDER LUG

HEX NUT
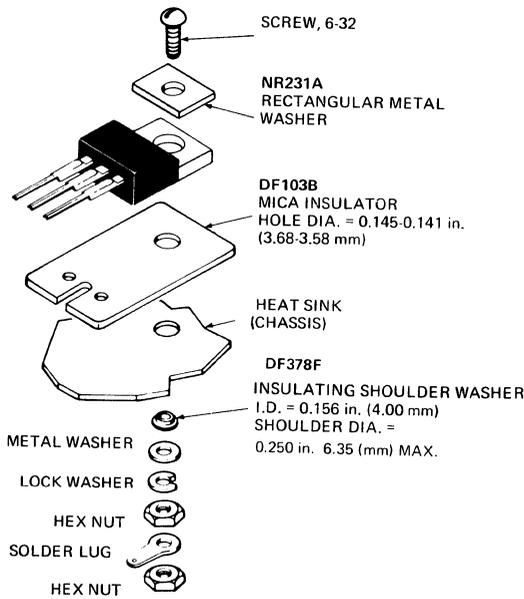
92CS-34689

NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING
FLANGE IS 8 in.-lb. (0.09 kgf·m)

TO-220AA

SCREW, 6-32

NR231A
RECTANGULAR METAL
WASHER

DF103B
MICA INSULATOR
HOLE DIA. = 0.145-0.141
(3.68-3.58)

HEAT SINK

DF378F
INSULATING BUSHING
I.D. = 0.156 (4.00)
SHOULDER DIA. =
0.250 (6.40) MAX.
SHOULDER THICKNESS =
0.050 (1.27) MAX.

METAL WASHER

LOCK WASHER

HEX. NUT

SOLDER LUG

HEX. NUT
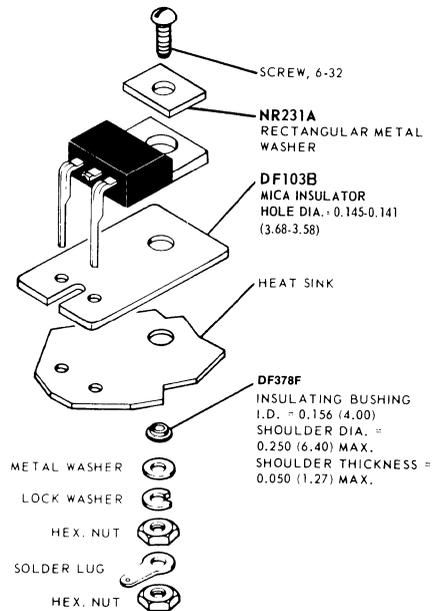
92CS-22564R2

*Fig. 35 - Methods of mounting flanged-
packaged types (cont'd).*

MOLDED-PLASTIC PACKAGES

RCA power transistors in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations.

The most common type of molded-plastic package is the RCA VERSAWATT (JEDEC TO-220) package for medium-power applications, specifically designed for ease of use in many applications. Each basic type offers several different lead options, and the user can select the configuration best suited to his particular application.

Fig. 36 shows the options currently available for devices in RCA VERSAWATT packages.

H-1535R1

(a)

(b)

H-1534R1

(c)
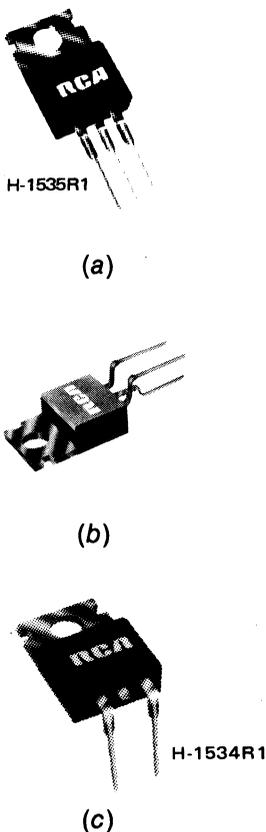
Fig. 36 - RCA VERSAWATT transistor packages: (a) JEDEC No. TO-220AB in-line lead version; (b) configuration designed for mounting on printed-circuit boards; (c) JEDEC No. TO-220AA version, which may be used as replacement for JEDEC No. TO-66 metal packages in JEDEC TO-66 sockets.

The JEDEC Type TO-220AB in-line-lead version, shown in Fig. 36(a), represents the basic style. This configuration features leads that can be formed to meet a variety of specific mounting requirements. Figs. 36(b) and 37 show a package configuration that allows a VERSAWATT package to be mounted on a printed-circuit board with a 0.100-inch grid and a minimum lead spacing of 0.200 inch. Fig. 36(c) shows a JEDEC Type TO-220AA version of the VERSAWATT package. The dimensions of this type of transistor package are such that it can replace the JEDEC TO-66 transistor package in a commercial socket or printed-circuit board without retooling. The TO-220AA VERSAWATT package can also be obtained with an integral heat sink.
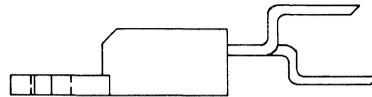
Fig. 37 - Method of configuring VERSA-WATT transistor leads for connection to printed-circuit boards and to provide relief in mounting arrangements in which forces are imposed on the package leads.

Lead-Forming Techniques

The RCA VERSAWATT plastic package is both rugged and versatile within the confines of commonly accepted standards for such devices. Although these versatile packages lend themselves to numerous arrangements, provision of a wide variety of lead configurations to conform to the specific requirements of many different mounting arrangements is highly impractical. However, the leads of the VERSAWATT in-line package can be formed to a custom shape, provided that they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping.

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The use of a properly designed

INCORRECT

LEAD IS NOT RESTRAINED BETWEEN
BENDING POINT AND PLASTIC CASE.

(a)

CORRECT

(b)

92CS-26385
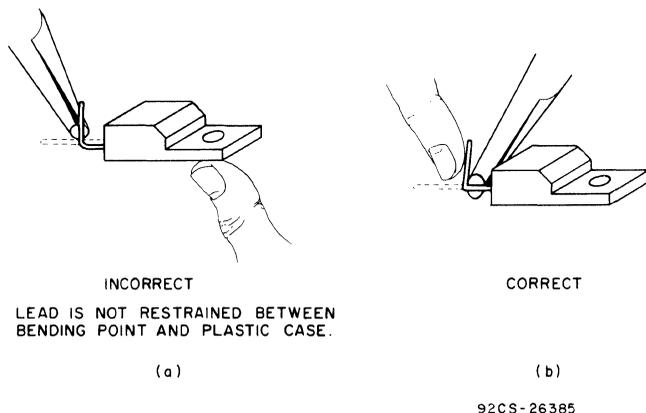
*Fig. 38 - Use of long-nosed pliers for lead
bending: (a) incorrect method;
(b) correct method.*

fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case. Fig. 38 illustrates the use of long-nosed pliers for lead bending. Fig. 38(a) shows a technique that should be avoided; Fig. 38(b) shows the correct method.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least ⅛ inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT in-line package are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should

be devised. Fig. 38 illustrates an acceptable lead-forming method that provides this relief.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed; the maximum soldering temperature, however, must not exceed 235°C and must be applied for not more than 10 seconds at a distance greater than ⅛ inch from the plastic case. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

Mounting Considerations

Fig. 39 shows recommended mounting arrangements and suggested hardware for VERSAWATT devices. The rectangular washer (NR231A) shown in Fig. 39(a), (c) and (d) was designed to minimize distortion of the mounting flange when the device is fastened to a heat sink. Excessive distortion of the flange could cause damage to the device. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8-inch-pounds is recommended. The tool used to drive the mounting screw should never come in contact with the plastic

SCREW, 6-32

NR231A
RECTANGULAR METAL
WASHER

DF103B
MICA INSULATOR
HOLE DIA. = 0.145-0.141 in.
(3.68-3.58 mm)

HEAT SINK
(CHASSIS)

DF378F

INSULATING SHOULDER WASHER
I.D. = 0.156 in. (4.00 mm)
SHOULDER DIA. =
0.250 in. 6.35 (mm) MAX.

METAL WASHER

LOCK WASHER

HEX NUT

SOLDER LUG

HEX NUT

92CS-34689

NOTE: MAXIMUM TORQUE APPLIED TO MOUNTING
FLANGE IS 8 in. lb. (0.09 kgf m)

SCREW, 4-40

DF137A
INTEGRAL
INSULATING WASHER

DF103C
MICA INSULATOR
(HOLE FOR 4-40 SCREW)

HEAT SINK

METAL WASHER

LOCK WASHER

HEX. NUT

SOLDER LUG

HEX. NUT

92CS-21279R2

SCREW, 6-32

NR231A
RECTANGULAR METAL
WASHER

DF103B
MICA INSULATOR
HOLE DIA. = 0.145-0.141
(3.68-3.58)

HEAT SINK

DF378F
INSULATING BUSHING
I.D. = 0.156 (4.00)
SHOULDER DIA. =
0.250 (6.40) MAX.
SHOULDER THICKNESS =
0.050 (1.27) MAX.

METAL WASHER

LOCK WASHER

HEX. NUT

SOLDER LUG

HEX. NUT

92CS-22564R2

NR231A
RECTANGULAR METAL
WASHER

HEAT
SINK

SCREW, 6-32

PRINTED
CIRCUIT
BOARD

92CS-21281R1

Fig. 39 - Recommended mounting arrangements and suggested hardware for use with VERSAWATT devices.

body during driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body, as shown in Fig. 40. The material used for such a spacer or spacer-isolating bushing should be carefully selected to avoid cold-flow and consequent reduction in mounting force. Suggested materials for these bushings are diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The flange should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the device to become excessive.

SCREW 4-40

SHOULDER BUSHING

HEADER

INSULATOR

HEAT SINK
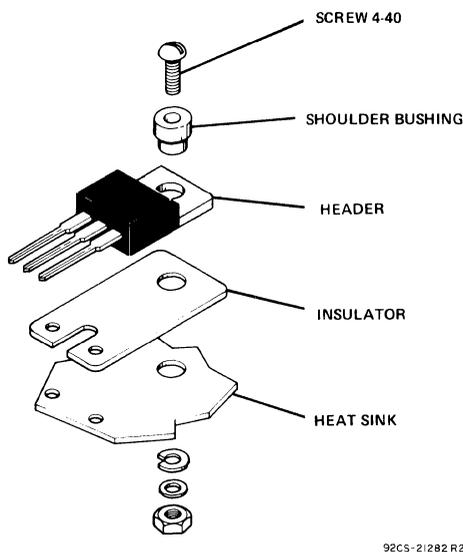
92CS-21282 R2

Fig. 40 - Mounting arrangement in which an isolating bushing is used to raise the head of the mounting screw above the plastic body of the VERSAWATT package.

TO-220AA packages can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket No. PT-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. CD74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:
1. Use appropriate hardware.
2. Always fasten the devices to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings made of materials that do not have hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

Many solvents are available for degreasing and removal of flux from device and printed-circuit board after the device has been mounted. The usual practice is to submerge the board in a solvent bath for a specified time. From a reliability standpoint, however, it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), not adversely affect the life of the device. This consideration applies to all non-hermetic and molded-plastic devices.

It is, of course, impractical to evaluate the effect on long-term device life of all cleaning solvents, which are marketed under a variety of brand names with numerous additives. Chlorinated solvents, gasoline, and other hydrocarbons cause the inner encapsulant to swell and damage the transistor. Alcohols are acceptable solvents and are recommended for flux removal whenever possible. Several examples of suitable alcohols are listed below:
1. methanol
2. ethanol
3. isopropanol
4. blends of the above

When considerations such as solvent flammability are of concern, selected freon-alcohol blends are usable when exposure is limited. Solvents such as those listed below should be safe when used for normal flux removal

operations, but care should be taken to assure their suitability in the cleaning procedure:
1. Freon TE
2. Freon TE-35
3. Freon TP-35 (Freon PC)

These solvents may be used for a maximum of 4 hours at 25° C or for a maximum of 1 hour at 50° C.

Care must also be used in the selection of fluxes in the soldering of leads. Rosin or activated-rosin fluxes are recommended; organic fluxes are not.

SPECIAL HANDLING CONSIDERATIONS

The generation of static charge in dry weather is harmful to all transistors, and can cause permanent damage or catastrophic failure in the case of high-speed devices. The most obvious precaution against such damage is humidity control in storage and operating areas. In addition, it is desirable that transistors be stored and transported in metal trays rather than in polystyrene foam "snow". During testing and installation, both the equipment and the operator should be grounded, and all power should be turned off when the device is inserted into the socket. Grounded plates may also be used for stockpiling of transistors prior to or after testing, or for use in testing ovens or on operating life racks. Further protection against static charges can be provided by use of partially conducting floor planes and non-insulating footwear for all personnel.

Environmental temperature also affects performance. Variations of as little as 5 per cent can cause changes of as much as 50 per cent in the saturation current of a transistor. Some test operators can cause marked changes in measurements of saturation current because the heat of their hands affects the transistors they work on. Precautions against temperature effects include air-conditioning systems, use of finger cots in handling of transistors (or use of pliers or "plug-in boards" to eliminate handling), and accurate monitoring and control of temperature near the devices. Prior to testing, it is also desirable to allow sufficient time (about 5 minutes) for a transistor to stabilize if it has been subjected to temperature much higher or lower than normal room temperature (25° C).

Although transient rf fields are not usually of sufficient magnitude to cause permanent damage to transistors, they can interfere with accurate measurement of characteristics at very low signal levels or at high frequencies. For this reason, it is desirable to check for such radiation periodically and to eliminate its causes. In addition, sensitive measurements should be made in shielded screen rooms if possible. Care must also be taken to avoid the exposure of transistors to other ac or magnetic fields.

Many transistor characteristics are sensitive to variations in temperature, and may change enough at high operating temperatures to affect circuit performance. Fig. 41 illustrates the effect of increasing temperature on the common-emitter forward current-transfer ratio (beta), the dc collector-cutoff current, and the input and output impedances. To avoid undesired changes in circuit operation, it is recommended that transistors be located away from heat sources in equipment, and also that provisions be made for adequate heat dissipation and, if necessary, for temperature compensation.


92CS-25741
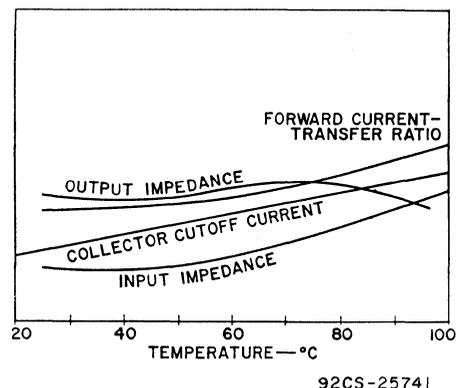
Fig. 41 - Variation of transistor characteristics with temperature.

Ratings and Characteristics

Ratings are established for solid-state devices to help circuit and equipment designers use the performance and service capabilities of each type to maximum advantage. They define the limiting conditions within which a device must be maintained to assure satisfactory and reliable operation in equipment applications. A designer must thoroughly understand the constraints imposed by the device ratings if he is to achieve effective, economical, and reliable equipment designs. Reliability and performance considerations dictate that he select devices for which no ratings will be exceeded by any operating conditions of his application, including equipment malfunction. He should also realize, however, that selection of devices that have overly conservative ratings may significantly add to the cost of his equipment.

BASIS FOR DEVICE RATINGS

Three systems of ratings (the absolute maximum system, the design center system, and the design maximum system) are currently in use in the electronics industry. The ratings given in the RCA technical data for solid-state devices are based on the **absolute maximum system**. A definition for this system of ratings has been formulated by the **Joint Electron Devices Engineering Council (JEDEC)** and standardized by the **National Electrical Manufacturers Association (NEMA)** and the **Electronic Industries Association (EIA)**, as follows:

"**Absolute-maximum ratings** are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

"The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

"The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst possible operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics."

The rating values specified in the technical data for RCA solid-state devices are determined on the basis of extensive operating and life tests and comparison measurements of critical device parameters. These tests and measurements define the limiting capabilities of a specific device type in relation to the rating factors being considered. The test and measurement conditions simulate, as closely as possible, the worst-case conditions that the device is likely to encounter in actual equipment applications.

Rating tests are expensive, time-consuming, and often destructive. Obviously, therefore, all individual solid-state devices of a given type designation cannot be subjected to these tests. The validity of the ratings is assured, however, by use of stringent processing and fabrication controls and extensive quality checks at each stage in the manufacturing process to assure product uniformity among all devices of a specific type designation and by testing of a statistically significant number of samples.

Ratings are given for those stress factors that careful study and experience indicate may lead to severe degradation in performance characteristics or eventual failure of a device unless they are constrained within certain limits.

All solid-state devices undergo irreversible changes if their temperature is increased

beyond some critical limit. A number of ratings are given for power transistors, therefore, to assure that this critical temperature limit will not be exceeded on even a very small part of the silicon chip. The ratings for power transistors normally specify the maximum voltages, maximum current, maximum and minimum operating and storage temperatures, and maximum power dissipation that the transistor can safely withstand.

In power transistors, the main design consideration is power-handling capability. This capability is determined by the maximum junction temperature a transistor can withstand and how quickly the heat can be conducted away from the junction.

In general, the basic physical theory that defines the behavior of any bipolar transistor in relation to charge-carrier interactions, current gain, frequency capabilities, voltage breakdown, and current and temperature ratings is not significantly different for power types. Power transistors, however, must be capable of large current densities and are required to sustain large voltage fields. For power types, therefore, the basic transistor theory must be expanded to include the effect that these conditions have on the physical behavior of the devices. In addition, the physical capabilities of power transistors must be defined in terms of factors, such as second-breakdown energy levels, safe operating area, and thermal-cycling stresses, that are not usually considered for small-signal types.

VOLTAGE RATINGS

Maximum voltage ratings are normally given for both the collector and the emitter junctions of a transistor. A V_{BEO} rating, which indicates the maximum base-to-emitter voltage with the collector open, is usually specified. The collector-junction voltage capability is usually given with respect to the emitter, which is used as the common terminal in most transistor circuits. This capability may be expressed in several ways. A V_{CEO} rating specifies the maximum collector-to-emitter voltage with the base open; a V_{CER} rating for this voltage implies that the base is returned to the emitter through a specified resistor; a V_{CES} rating gives the maximum voltage when the base is shorted to the emitter; and a V_{CEV} rating indicates the maximum voltage when the base is reverse-biased with respect to the emitter by a specified voltage. A V_{CEX} rating

may also be given to indicate the maximum collector-emitter voltage when a resistor and voltage are both connected between base and emitter.

If a maximum voltage rating is exceeded, the transistor may "break down" and pass current in the reverse direction. The breakdown across the junction is usually not uniform, and the current may be localized in one or more small areas. The small area becomes overheated unless the current is limited to a low value, and the transistor may then be destroyed.

The collector-to-base or emitter-to-base breakdown (avalanche) voltage is a function of the resistivity or impurity doping concentration at the junction of the transistor and of the characteristics of the circuit in which the transistor is used. When there is a breakdown at the junction, a sudden rise in current (an "avalanche") occurs. In an abruptly changing junction, called a step junction, the avalanche voltage is inversely proportional to the impurity concentration. In a slowly changing junction, called a graded junction, the avalanche voltage is dependent upon the rate of change of the impurity concentration (grade constant) at the physical junction. Fig. 42 shows the two types of junction breakdowns. The basic transistor voltage-breakdown mechanisms and their relationship to external circuits are the basis for the various types of voltage ratings used by transistor manufacturers.
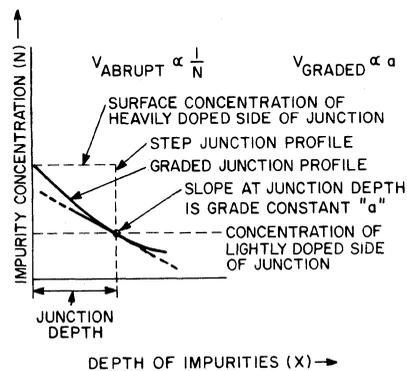
Fig. 42 - *Step-junction and graded-junction breakdown.*

CURRENT, TEMPERATURE, AND DISSIPATION RATINGS

The physical mechanisms related to basic transistor action are temperature-sensitive. If the bias is not temperature-compensated, the transistor may develop a regenerative condition, known as **thermal runaway**, in which the thermally generated carrier concentration approaches the impurity carrier concentration. [Experimental data for silicon show that, at temperatures up to 700°K, the thermally generated carrier concentration n_i is determined as follows: $n_i = 3.87 \times 10^{16} \times T \times (3/2)$ exp $(-1.21/2kT)$.] When this condition becomes extreme, transistor action ceases, the collector-to-emitter voltage V_{CE} collapses to a low value, and the current increases and is limited only by the external circuit.

If there is no current limiting, the increased current can melt the silicon and produce a collector-to-emitter short. This condition can occur as a result of a large-area average temperature effect, or in a small area that produces hot spots or localized thermal runaway. In either case, if the intrinsic temperature of a semiconductor is defined as the temperature at which the thermally generated carrier concentration is equal to the doped impurity concentration, the absolute maximum temperature for transistor action can be established.

The intrinsic temperature of a semiconductor is a function of the impurity concentration, and the limiting intrinsic temperature for a transistor is determined by the most lightly doped region. It must be emphasized, however, that the intrinsic temperature acts only as an upper limit for transistor action. The maximum operating junction temperature and the maximum current rating are established by additional factors such as the efficiency of heat removal, the yield point and melting point of the solder used in fabrication, and the temperature at which permanent changes in the junction properties occur.

The **maximum current rating** of a transistor indicates the highest current at which, in the manufacturer's judgment, the device is useful. This current limit may be established by setting an arbitrary minimum current gain or may be determined by the fusing current of an internal connecting wire. A current that exceeds the rating, therefore, may result in a low current gain or in the destruction of the transistor.

The basic materials in a silicon transistor allow transistor action at temperatures greater than 300°C. Practical transistors, however, are limited to lower temperatures by mounting systems and surface contamination. If the **maximum rated storage** or **operating temperature** is exceeded, irreversible changes in leakage current and in current-gain characteristics of the transistor result.

Junction-Temperature Ratings

The temperature of solid-state devices must be closely controlled not only during operation, but also during storage. For this reason, ratings data for these devices usually include maximum and minimum **storage temperatures**, as well as **maximum operating temperatures**.

The maximum allowable power dissipation in a solid-state device is limited by the temperature of the semiconductor pellet (i.e., the junction temperature). An important factor that assures that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device. For this reason, solid-state power devices should be mounted on a good thermal base (usually copper), and means should be provided for the efficient transfer of heat from this base to the surrounding environment.

When a solid-state device is mounted in free air, without a heat sink, the steady-state thermal circuit is defined by the **junction-to-free-air thermal resistance** given in the published data on the device. Thermal considerations require that there be a free flow of air around the device and that the power dissipation be maintained below that which would cause the **junction temperature** to rise above the maximum rating. When the device is mounted on a heat sink, however, care must be taken to assure that all portions of the thermal circuit are considered.

Solid-state power devices may also be adversely affected by temperature variations that result from changes in power dissipation during operation or in the temperature of the ambient environment. Such temperature variations produce cyclic mechanical stresses at the interface of the semiconductor pellet and the copper base to which the pellet is attached because of the different thermal-expansion coefficients of these materials. These thermally induced cyclic stresses may eventually lead to a wearout type of failure refered to as **thermal fatigue**.

In this section the thermal impedances that comprise the basic thermal circuit of a solid-state device are defined, the use and advantages of external heat sinks are described, and the effects of cyclic thermal stresses are analyzed. The basic principles explained are generally applicable to all solid-state power devices regardless of the particular type of device identified in specific examples.

Basic Thermal System

When current flows through a solid-state device, power is dissipated in the semiconductor pellet that is equal to the product of the voltage across the junction and the current through it. As a result, the temperature of the pellet increases. The amount of the increase in temperature depends on the power level and how fast the heat can flow away from the junction through the device structure to the case and the ambient atmosphere. The rate of heat removal depends primarily upon the thermal resistance and capacitance of the materials involved. The temperature of the pellet rises until the rate of heat generated by the power dissipation is equal to the rate of heat flow away from the junction; i.e., until thermal equilibrium has been established.

Thermal resistance can be compared to electrical resistance. Just as electrical resistance is the extent to which a material resists the

flow of electricity, thermal resistance is the extent to which a material resists the flow of heat. A material that has a low thermal resistance is said to be a good thermal conductor. In general, materials which are good electrical conductors are good thermal conductors, and vice versa.

Power-Dissipation Ratings

Power is dissipated in the semiconductor material of a solid-state device in the form of heat, which if excessive can cause irreversible changes in the crystal structure or melting of the pellet. This dissipation is equal to the difference between the input power applied to the device and the power delivered to the load circuit. Because of the sensitivity of semiconductor materials to variations in thermal conditions, maximum dissipation ratings are usually given for specific temperature conditions.

In many instances, dissipation ratings for solid-state devices are specified for ambient, case, or mounting-flange temperatures up to 25°C. Such ratings must be reduced linearly for operation of the devices at higher temperatures. Fig. 43 shows a typical power-transistor derating chart that can be used to determine maximum permissible dissipation values at specific temperatures above 25°C. (This chart cannot be assumed to apply to transistor types
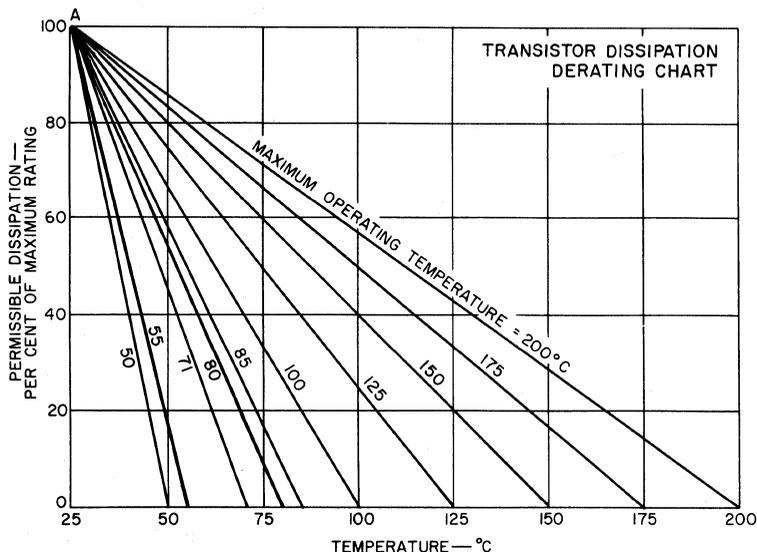

Fig. 43 - Chart showing maximum permissible percentage of maximum rated dissipation as a function of temperature.

other than the particular transistors for which it was prepared.) The chart shows the permissible percentage of the maximum dissipation ratings as a function of ambient or case temperature. Individual curves are shown for specific operating temperatures. If the maximum operating temperature of a particular transistor type is some other value, a new curve can be drawn from point A to the desired temperature value on the abscissa, as indicated by the dashed-line curves on the chart.

EFFECT OF EXTERNAL HEAT SINKS

The maximum allowable power dissipation in a solid-state device is limited by the temperature of the semiconductor pellet (i.e., the junction temperature). An important factor that assures that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device. For this reason, solid-state power devices should be mounted on a good thermal base (usually copper), and means should be provided for the efficient transfer of heat from this base to the surrounding environment.

Most practical heat sinks used in modern, compact equipment are the result of experiments with heat transfer through convection, radiation, and conduction in a given application. Although there are no set design formulas that provide exact heat-sink specifications for a given application, there are a number of simple rules that reduce the time required to evolve the best design for the job. These simple rules are as follows:

1. The surface area of the heat sink should be as large as possible to provide the greatest possible heat transfer. The area of the surface is dictated by case-temperature requirements and the environment in which the device is to be placed.

2. The heat-sink surface should have an emissivity value near unity for optimum heat transfer by radiation. A value approaching unity can be obtained if the heat-sink surface is painted flat black.

3. The thermal conductivity of the heat-sink material should be such that excessive thermal gradients are not established across the heat sink.

Although these rules are followed in conventional heat-sink systems, the size and cost of such systems often become restrictive in compact, mass-produced power-control and power-switching applications. The use of mass-produced prepunched parts, direct soldering, and batch-soldering techniques eliminates many of the difficulties associated with heat sinks by making possible the use of a variety of simple, efficient, readily fabricated heat-sink configurations that can be easily incorporated into the mechanical design of equipment.

For most efficient heat sinking, intimate contact should exist between the heat sink and at least one-half of the package base. The package can be mounted on the heat sink mechanically, with glue or epoxy adhesive, or by soldering. (Soldering is not recommended for transistors.) If mechanical mounting is employed, silicone grease should be used between the device and the heat sink to eliminate surface voids, prevent insulation buildup due to oxidation, and help conduct heat across the interface. Although glue or epoxy adhesive provides good bonding, a significant amount of resistance may exist at the interface resistance; an adhesive material with low thermal resistance, such as Hysol Epoxy Patch Material No. 6C or Wakefield Delta Bond No. 152, or their equivalent, should be used.

Types of Heat Sinks

Heat sinks are produced in various sizes, shapes, colors, and materials; the manufacturer should be contacted for exact design data. It is convenient for discussion purposes to group heat sinks into three categories as shown below:

1. **Flat vertical-finned types** are normally aluminum extrusions with or without an anodized black finish. They are unexcelled for natural convection cooling and provide reasonable thermal resistance at moderate air-flow rates for forced convection.

2. **Cylindrical or radial vertical-finned types** are normally cast aluminum with an anodized black finish. They are used when maximum cooling in minimum lateral displacement is required, using natural convection.

3. **Cylindrical horizontal-finned types** are normally fabricated from sheet-metal rings and have a painted black matte finish. They are used in confined spaces for maximum cooling in minimum displaced volume.

It is also common practice to use the existing mechanical structure or chassis as a

heat sink. The design equations and curves for such heat sinks based upon convection and radiation are shown in Figs. 44, 45, and 46.

A useful nomograph which considers heat removal by both convection and radiation is given in Fig. 47. This nomograph applies for natural bright finish on the copper or aluminum.

$$R_{\theta C} = \frac{2300}{A} \times \left(\frac{L}{T_s - T_a}\right)^{0.25}$$

$$R_{\theta C} = \frac{\theta_C'}{A} \; °C/WATT$$

WHERE $R_{\theta C}$ = CONVECTION THERMAL RESISTANCE °C/WATT

A = AREA IN cm^2, TOTAL EXPOSED SURFACE

L = HEIGHT IN cm
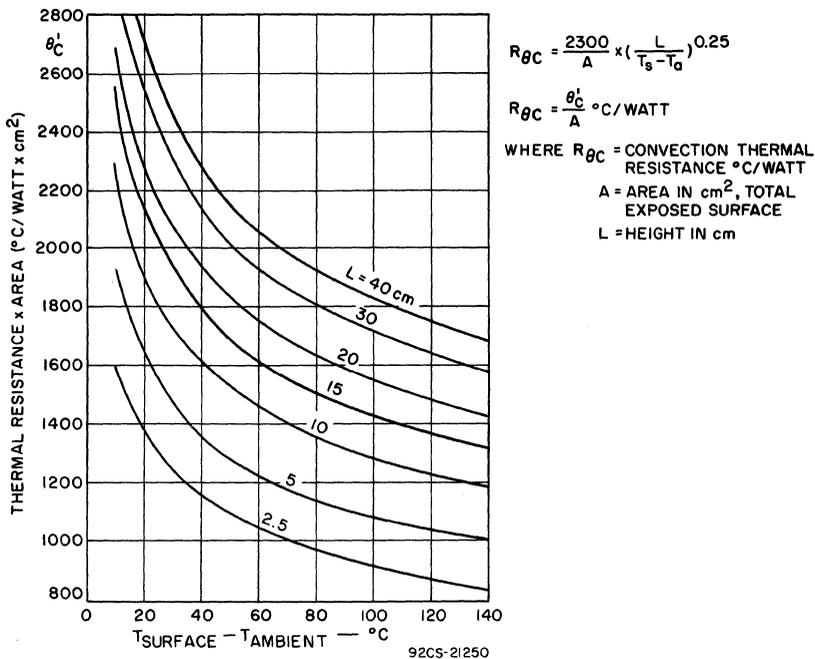
Fig. 44 - Convection thermal resistance as a function of temperature drop from the surface of the heat sink to free air for heat sinks of various heights. (Reprinted from Control Engineering, October 1956.)

$$R_{\theta R} = \frac{1793 \times 10^8}{A e \left(T_s^2 + T_a^2\right)\left(T_s + T_a\right)}$$

$$= \frac{R_{\theta R}'}{Ae} \; °C/WATT$$

WHERE A = TOTAL EXPOSED AREA, cm^2

e = EMISSIVITY

T_s = SURFACE TEMP, °C

T_a = AMBIENT TEMP, °C

$R_{\theta R}$ = RADIATION THERMAL RESISTANCE
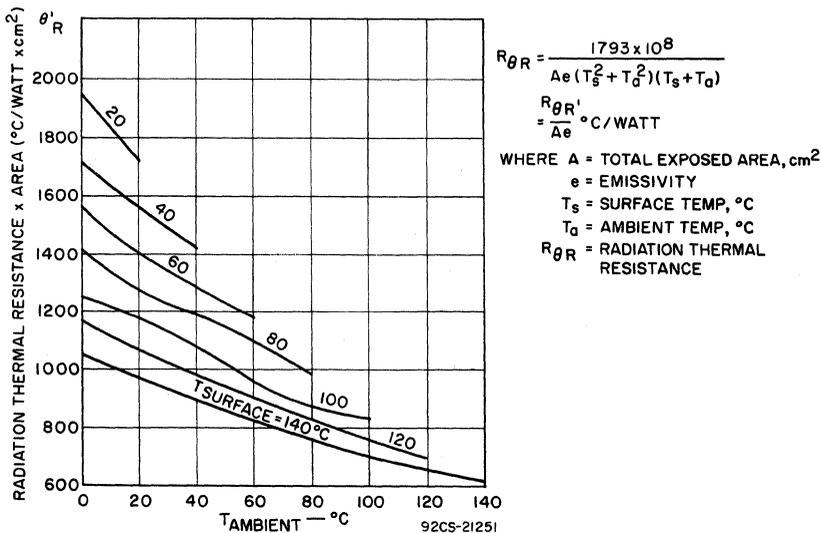
Fig. 45 - Radiation thermal resistance as a function of ambient temperature for various heat-sink surface temperatures. (Reprinted from Control Engineering, October 1956.)
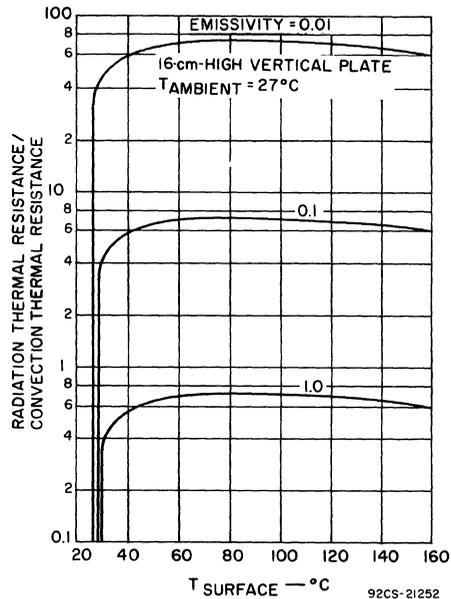
Fig. 46 - Ratio of radiation thermal resistance to convection thermal resistance as a function of heat-sink surface temperature for various surface emissivities. (Reprinted from Control Engineering, October 1967.)
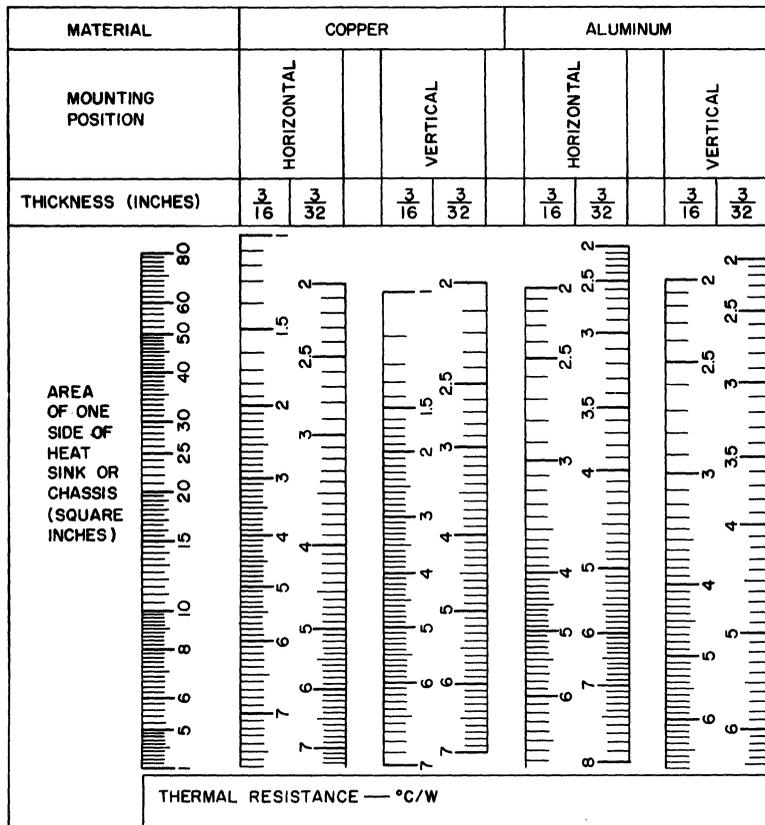
Fig. 47 - Thermal resistance as a function of heat-sink dimensions. (Nomograph reprinted from Electronic Design, August 16, 1961.)

Heat-Sink Performance

The performance that may be expected from a commercial heat sink is normally specified by the manufacturer, and the information supplied in the design curves shown in Figs. 44, 45, and 46 provides the basis for the design of flat vertical plates for use as heat sinks. In all cases, it must be remembered that the heat is dissipated from the heat sink by both convection and radiation. Although surface area is important in the design of vertical-plate heat sinks, other factors such as surface and ambient temperature, conductivity, emissivity, thickness, shape, and orientation must also be considered. An excessive temperature gradient can be avoided and the conduction thermal resistance in the heat sink can be minimized by use of a high-conductivity material, such as copper or aluminum, for the heat sink. Radiation losses are increased by an increase in surface emissivity. Best results are obtained when the heat sink has a black matte finish for which the emissivity is at least 0.9. When free-air convection is used for heat removal, a vertically mounted heat sink provides a thermal resistance that is approximately 30 per cent lower than that obtained with horizontal mounting.

In restricted areas, it may be necessary to use forced-convection cooling to reduce the effective thermal resistance of the heat sink. On the basis of the improved reliability of cooling fans, it can be shown that the over-all reliability of a system may actually be improved by use of forced-convection cooling because the number of components required is reduced.

Economic factors are also important in the selection of heat sinks. It is often more economical to use one heat sink with several properly placed transistors than to use individual heat sinks. It can be shown that the cooling efficiency increases and the unit cost decreases under such conditions.

Heat-Sink Insulators

As pointed out previously, when power transistors are to be mounted on heat sinks, some form of electrical isolation must be provided between the case and the heat sink. Unfortunately, however, good electrical insulators usually are also good thermal insulators. It is difficult, therefore, to provide electrical insulation without introduction of significant thermal resistance between case and heat sink. The best materials for this application are mica, beryllium oxide (Beryllia), and anodized aluminum. A comparison of the properties of these three materials for case-to-heat-sink isolation of the TO-3 package is shown in Table III. If the area of the seating plane, the thickness of the material, and the thermal conductivity are known, the case-to-heat-sink thermal resistance θ_{C-S} can be readily calculated by use of the following equation:

$$\theta_{cond} = d/4.186\ KA\ °C \text{ per watt}$$

where d is the length of the thermal path in centimeters, K is the thermal conductivity in cal/(sec) (cm) (°C), and A is the area perpendicular to the thermal path t in square centimeters. The number 4.186 is a conversion factor used to obtain the result in °C per watt.

In all cases, this calculation should be experimentally verified. Irregularities in the bottom of the transistor seating plane or on the face of the heat sink or insulating washer may result in contact over only a very small area unless a filling compound is used. Although silicone grease has been used for years, recently newer compounds with zinc oxide fillers (e.g., Dow Corning #340 or Wakefield #120) have been found to be even more effective.

For small general-purpose transistors, such as the 2N2102, which use a JEDEC TO-5 package, a good method for thermal isolation of the collector from a metal chassis or

Table III - Comparison of Insulating Washers Used for Electrical Isolation of Transistor

TO-3 Case from Heat Sink			
Material	Thickness (inches)	θ_{C-S} (°C/W)	Capacitance (pF)
Mica	0.002	0.4	90
Anodized Aluminum	0.016	0.35	110
Beryllia	0.063	0.25	15

printed-circuit board is by means of a beryllium-oxide washer. The use of a zinc-oxide-filled silicone compound between the washer and the chassis, together with a moderate amount of pressure from the top of the transistor, helps to decrease thermal resistance. Fin-type heat sinks, which are commercially available, are also suitable, especially when transistors are mounted in Teflon sockets which provide no thermal conduction to the chassis or printed-circuit board. Fig. 48 illustrates both types of mounting.

(a)

(b)

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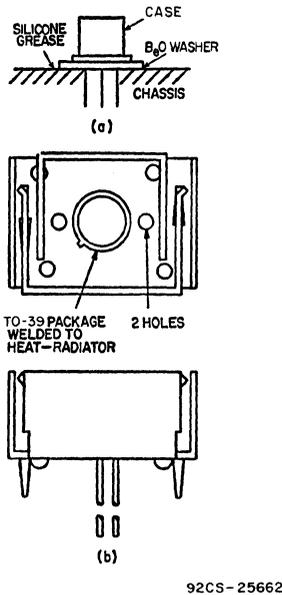
Fig. 48 - Suggested mounting arrangements for transistors having a JEDEC TO-5 package: (a) without heat sink; (b) with fin-type heat sink.

SECOND BREAKDOWN

A bipolar transistor operated at high power densities is subject to a failure mode termed "second breakdown" in which the emitter-collector voltage suddenly drops, usually 10 to 25 volts. Unless the power is rapidly removed, the transistor is destroyed or materially degraded by overheating. Second breakdown (S/b) is a thermal hot-spot formation within the transistor pellet. It has two phases of development. First is the constriction phase where, because of thermal regeneration, the current tends to concentrate in a small area. The second phase is the destruction phase. In this second phase, local temperatures and

temperature gradients increase until they cause permanent device damage.

The constriction or regeneration phase of second breakdown may be initiated in any number of ways. One section of the emitter-base junction need only be higher in temperature than the others. Such a hot spot might be caused by resistive debiasing, divergent heat flow to the device heat sink, an inhomogeneity in the thermal path, or other irregularities or imperfections within the device. Once a slightly hotter emitter-base region is present, positive thermal feedback begins: the hot region injects more and therefore gets hotter. If the available power is limited or the effective thermal resistance of the hot spot is sufficiently low, the peak temperature remains below a critical temperature, and stable operation continues. When the peak temperature reaches a value such that local base-collector leakage currents reach base current magnitude, the device regenerates into second breakdown, often very rapidly.

Second breakdown may occur when the device operates with a forward-biased emitter-base junction or during the application of reverse bias. In the forward-biased form of second breakdown, shown in Fig. 49, the current $I_{S/b}$ above which the device switches into second breakdown is specified as part of the "safe-operating area" rating system developed by RCA for power transistors. (This system is explained later in this section.) Emitter

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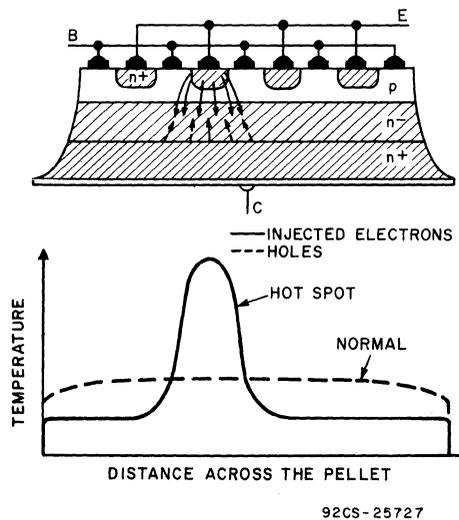
Fig. 49 - Forward-biased second breakdown.

and base resistive ballasting effectively increase forward-biased $I_{s/b}$ of a device. Emitter ballasting equalizes currents by inserting in each emitter region a voltage drop proportional to base current in the various base regions thus equalizing drive conditions within the device and maintaining uniformity. Thermal coupling between emitter regions may also be used to improve the forward biased $I_{s/b}$ performance of a transistor. This design approach tends to hold all regions of the emitter-base junction at the same temperature and same forward bias, thus maintaining uniform current flow.

Second breakdown is also observed when a transistor operating with an inductive load is turned off. Fig. 50 shows this form of second breakdown. When the emitter-base junction is



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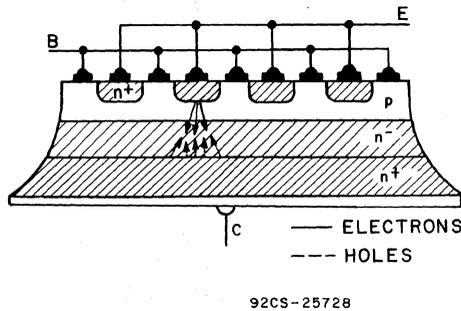
Fig. 50 - Reverse-biased second break-down.

reverse biased, the edges of the emitters are quickly turned-off by the voltage drop caused by the reverse flow of the base current through the base resistance under the emitter. Collector current tends to be rapidly reduced; however, the inductive load responds to the decrease in collector current by driving the collector-emitter voltage to a value at which breakdown can occur in the collector-base space charge region $V_{(BR)CEX}$. The multiplied current resulting from the breakdown is focused towards the emitter centers, keeping the centers on for a longer time. When all center sections of the emitters behave alike, the power is dissipated uniformly by all emitters. If, however, a hot spot exists or develops, the energy stored in the load inductance is dumped into this region. The central region of this emitter rapidly rises in temperature, reaching a value where the hot spot sustains itself and second breakdown occurs. Emitter ballasting is not effective in protecting against reverse-biased second breakdown because the hogging portion of the

emitter is fed internally from a current source, and this current source is insensitive to the relatively small differences in emitter potential: Ballasting against reverse-biased second breakdown is best done in the collector by the addition of a resistive layer which decreases the internal collector-emitter voltage in the affected region. The maximum energy that may be stored in the load inductance before second breakdown ($E_{s/b}$) is specified for most RCA power transistors intended for switching applications.

HIGH-VOLTAGE SURFACE EFFECTS

As the voltage ratings of a power transistor are increased, it becomes more difficult to achieve theoretical bulk breakdown values. Furthermore, both the breakdown voltage and junction leakage currents may vary under operating conditions. The problem is usually due to surface phenomena.

High-voltage transistors require large depletion widths in the base-collector junction. This requirement suggests that at least one side of the junction must be lightly doped. Fig. 51 shows what happens in a normal "mesa-type" device. The external fringing electrical fields terminate on the silicon and modify the depletion regions at the surface. If these fringing fields are large and configured as shown, a local high field condition is established at the surface and premature breakdown occurs. High-intensity fringing fields exist well outside the junction and contribute to the movement of ions external or internal to the applied passivation layers, leading to instabilities.

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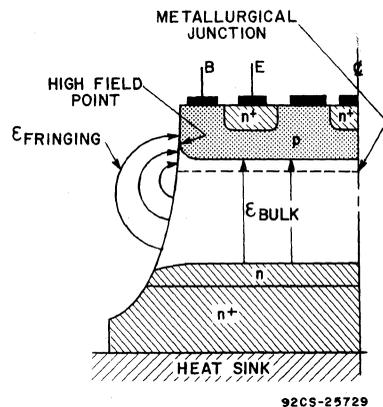
Fig. 51 - Electric field distribution in high-voltage "mesa" n-p-n transistor.

The state-of-the-art "cures" for these problems are: junction contouring to reduce the magnitude and the shape of the fringing fields; empirical determination of the proper surface etch and the optimum organic encapsulant; or glassing of the junctions to contain the fringing fields. The latter two solutions do not usually yield breakdown voltages equal to the bulk values, but they do lessen the surface instability.

To achieve breakdown voltages approaching the bulk values it is necessary that the fringing field be properly shaped, and once properly shaped it must be kept in this condition. Field electrodes are being investigated to accomplish this objective.

THERMAL-CYCLING RATINGS

A power transistor is often used in applications where the power in the device is cycled; the transistor is heated and cooled many times. Because the transistor is constructed of materials that have different thermal expansion coefficients, stress is placed on the chip, the metallurgical bond, and the heat spreader. If the stress is severe enough and sufficient cycles are encountered, the device fails. Usually the chip separates from the heat spreader or one of the contact connections opens. The stress is proportional to the size of the pellet, the temperature variation, elasticity of the connecting members, and the differences in thermal-expansion coefficients. Anything which concentrates the stress, such as voids in the mounting system, aggravates the condition.

The rate of degradation of a metallurgical bond under stressed conditions is also proportional to the average and peak temperature excursions of the bond. The failure-rate dependency of thermal fatigue and other

phenomena can be as much as double for every 10° C increase in average and peak temperature. The most economical way to buy reliability in power transistor application is, therefore, to reduce these temperatures by careful consideration of heat flow during equipment design.

Several techniques are used to improve thermal-cycling capability within power transistors. One method is to mount the chip on a metal such as molybdenum, whose thermal expansion coefficient is similar to silicon, and to braze this metal to the package. In this way stresses are evenly distributed, as in a graded glass seal. Another method, applicable on units using the lead solder mounting technique, uses a controlled solder process in which the thickness and composition of the lead solder are carefully controlled at all times.

An equipment manufacturer should make certain that power-transistor circuits included in his systems are designed so that cyclic thermal stresses are mild enough to assure that no transistor fatigue failures will occur during the required operating life of his equipment.

RCA has developed a **thermal-cycling rating system** that relates the total power dissipation P_T and the change in case temperature ΔT_C to the total number of thermal cycles N that the transistor is rated to withstand.

Fig. 52 shows a typical **thermal-cycling rating chart** for a power transistor. This chart is provided in the form of a log-log presentation in which total transistor dissipation is denoted by the ordinate and the thermal-cycling capability (number of cycles to failure) is indicated by the abscissa. Rating curves are shown for various magnitudes of changes in


92CS-18051
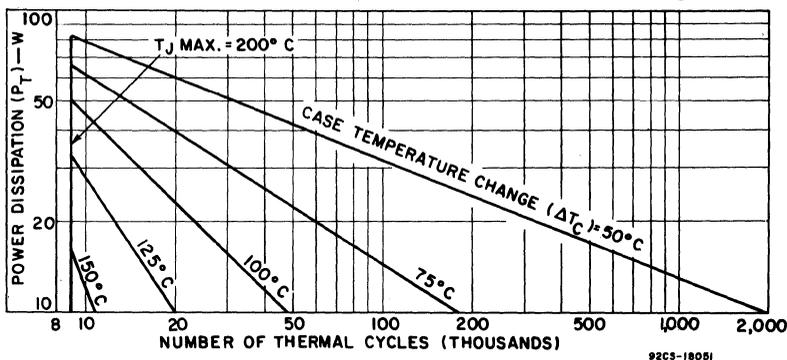
Fig. 52 - Thermal-cycling rating chart for an RCA hermetic power transistor.

case temperature. Use of the thermal-cycling rating charts makes it possible for a circuit designer to avoid transistor thermal-fatigue failures during the operating life of his equipment. In general, power dissipation is a fixed system requirement. The design can also readily determine the number of thermal cycles that a power transistor will be subjected to during the minimum required life of the equipment. For these conditions, the charts indicate the maximum allowable change in case temperature. If the rating point does not lie exactly on one of the rating curves, the allowable change in case temperature can be approximated by linear interpolation. The designer can then determine the minimum size of the heat sink required to restrict the change in case temperature within this maximum value.

RCA thermal-cycling ratings allow a circuit designer to use power transistors with assurance that thermal-fatigue failures of these devices will not occur during the minimum required life of his equipment. These ratings provide valid indications of the thermal-cycling capability of power transistors for all types of operating conditions.

SAFE-OPERATING-AREA RATINGS

During normal circuit operation, power transistors are often required to sustain high current and high voltage simultaneously. The capability of a transistor to withstand such conditions is normally shown by use of a safe-operating-area rating curve. This type of rating curve defines, for both steady-state and pulsed operation, the voltage-current boundaries that result from the combined limitations imposed by voltage and current ratings, the maximum allowable dissipation, and the second-breakdown ($I_{S/b}$) capabilities of the transistor.

If the safe-operating area of a power transistor is limited within any portion of the voltage-current characteristics by thermal factors (thermal impedance, maximum junction temperatures, or operating case temperature), this limiting is defined by a constant-power hyperbola ($I = KV^{-1}$) which can be represented on the log-log voltage-current curve by a straight line that has a slope of –1.

The energy level at which second breakdown occurs in a power transistor increases as the time duration of the applied voltage and current decreases. The power-handling capa-

bility of the transistor also increases with a decrease in pulse duration because thermal mass of the power-transistor chip and associated mounting hardware imparts an inherent thermal delay to a rise in junction temperature.

Fig. 53 shows a forward-bias safe-area rating chart for a typical silicon power transistor, the RCA-2N3585. The boundaries defined by the curves in the safe-area chart indicate, for both continuous-wave and non-repetitive-pulse operation, the maximum current ratings, the maximum collector-to-emitter forward-bias avalanche breakdown-voltage rating [$V\alpha M = 1$, which is usually approximated by $V_{CEO}(sus)$], and the thermal and second-breakdown ratings of the transistors.

As shown in Fig. 53, the thermal (dissipation) limiting of the 2N3585 ceases when the collector-to-emitter voltage rises above 100 volts during dc operation. Beyond this point, the safe operating area of the transistor is limited by the second-breakdown ratings. During pulsed operation, the thermal limiting extends to higher values of collector-to-emitter voltage before the second-breakdown region is reached, and as the pulse duration decreases, the thermal-limited region increases.
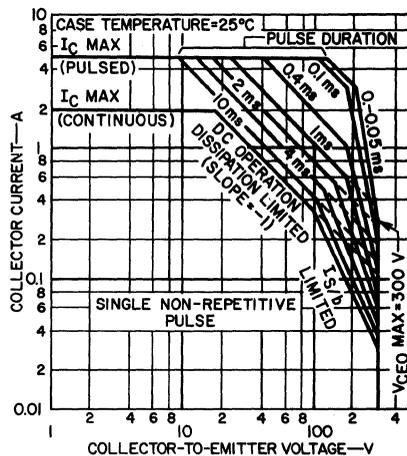
92CS-25733

Fig. 53 - Safe-area rating chart for the RCA-2N3585 silicon power transistor.

If a transistor is to be operated at a pulse duration that differs from those shown on the safe-area chart, the boundaries provided by the safe-area curve for the next higher pulse duration must be used, or the transistor manufacturer should be consulted. Moreover,

as indicated in Fig. 53, safe-area ratings are normally given for single nonrepetitive pulse operation at a case temperature of 25° C and must be derated for operation at higher case temperatures and under repetitive-pulse or continuous-wave conditions.

Fig. 54 shows temperature derating curves for the 2N3585 safe-area chart of Fig. 53. These curves show that thermal ratings are affected far more by increases in case temperature than are second-breakdown ratings. The thermal (dissipation-limited) derating curve decreases linearly to zero at the maximum junction temperature of the transistor [T_J(max)= 200° C]. The second-breakdown ($I_{S/b}$-limited) temperature derating curve, however, is less severe because the increase in the formation of the high current concentrations that cause second breakdown is less than the increase in dissipation factors as the temperature increases.

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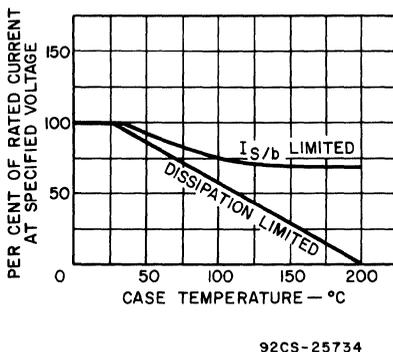
Fig. 54 - Safe-area temperature-derating curves for the RCA-2N3585 silicon power transistor.

Because the thermal and second-breakdown deratings are different, it may be necessary to use both curves to determine the proper derating factor for a voltage-current point that occurs near the breakpoint of the thermal-limited and second-breakdown-limited regions on the safe-area curve. For this condition, a derating factor is read from each derating curve. For one of the readings, however, either the thermal-limited section of the safe-area curve must be extrapolated upward in voltage or the second-breakdown-limited section must be extrapolated downward in voltage, depending upon which side of the voltage breakpoint the voltage-current point is located. The smaller of the collector-current values obtained from the thermal and second-breakdown deratings must be used as the safe rating.

For pulsed operation, the derating factor shown in Fig. 54 must be applied to the appropriate curve on the safe-area rating chart. For the derating, the effective case temperature T_C(eff) may be approximated by the average junction temperature T_J(av). The average junction temperature is determined as follows:

$$T_J(av) = T_C + P_{AV} (\theta_{J-C})$$

This approach results in a conservative rating for the pulsed capability of the transistor. A more accurate determination can be made by computation of actual instantaneous junction temperatures. (For more detailed information on safe-area ratings and temperature derating the reader should refer to the **RCA Power Circuits Designer's Handbook**, Technical Series SP-52.

BASIC TRANSISTOR CHARACTERISTICS

The term "characteristic" is used to identify the distinguishing electrical features and values of a transistor. These values may be shown in curve form or they may be tabulated. When the characteristics values are given in curve form, the curves may be used for the determination of transistor performance and the calculation of additional transistor parameters.

Characteristics values are obtained from electrical measurements of transistors in various circuits under certain definite conditions of current and voltage. **Static characteristics** are obtained with dc potentials applied to the transistor electrodes. **Dynamic characteristics** are obtained with an ac voltage on one electrode under various conditions of dc potentials on all the electrodes. The dynamic characteristics, therefore, are indicative of the performance capabilities of the transistor under actual working conditions.

Current-Voltage Relationships

The currents in a transistor are directly related to the movement of minority carriers in the base region that results from the application of voltages of the proper polarities to the emitter-base and collector-base junctions. A definite mutual relationship exists between the transistor currents and the voltages applied to the transistor terminals. Graphical representations of the variations in transistor currents with the applied voltages provide an excellent indication of the operation of a

transistor under different biasing conditions. Transistor manufacturers usually provide curves of current-voltage characteristics to define the operating characteristics of their devices. Such curves are provided for either common-emitter or common-base transistor connections. Fig. 55 shows the bias-voltage polarities and the current components for both common-emitter and common-base connections of a p-n-p transistor. For an n-p-n transistor, the polarities of the voltages and the directions of the currents are reversed.

(a)

(b)

92CS-25697RI
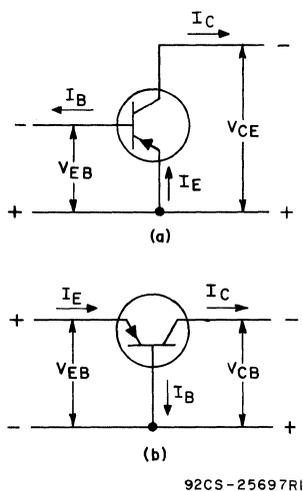
Fig. 55 - Transistor bias-voltage polarities and current components for (a) the common-emitter connection and (b) the common-base connection.

The common-emitter connection, shown in Fig. 55(a), is the more widely used in practical applications. In this connection, the emitter is the common point between the input (base) and output (collector) circuits, and large current gains are realized by use of a small base current to control a much larger emitter-to-collector current. The common-base connection, shown in Fig. 55(b), differs from the common-emitter connection in that the voltages applied to the transistor are referred to the base rather than to the emitter.

Published data for transistors include both electrode characteristic curves and transfer characteristic curves. These curves present the same information, but in two different forms

to provide more useful data. Because transistors are used most often in the common-emitter configuration, characteristic curves are usually shown for the collector or output electrode. The **collector-characteristic curve** is obtained by varying collector-to-emitter voltage and measuring collector current for different values of base current. The **transfer-characteristic curve** is obtained by varying the base-to-emitter (bias) voltage or current at a specified or constant collector voltage, and measuring collector current.

Current-Gain Parameters

Power gain in transistor circuits is usually obtained by use of a small control signal to produce larger signal variations in the output current. The gain parameter most often specified is the current gain (β) from the base to the collector. The power gain of a transistor operated in a common-emitter configuration is equal to the square of the current gain β times the ratio of the load resistance r_L to the input resistance r_{in}, as indicated in Fig. 56.
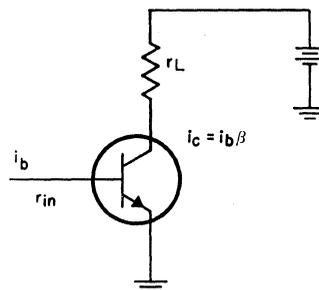
INPUT CURRENT $= i_b$
INPUT VOLTAGE $= i_b \, r_{in}$
OUTPUT CURRENT $= i_c = i_b\beta$
OUTPUT VOLTAGE $= i_c r_L = i_b\beta r_L$
INPUT POWER $= i_b{}^2 \, r_{in}$
OUTPUT POWER $= i_c{}^2 \, r_L = i_b{}^2 \, \beta^2 \, r_L$
POWER GAIN $=$ power output/power input
$= i_b{}^2\beta^2 r_L/i_b{}^2 r_{in}$
$= \beta^2 r_L/r_{in}$

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Fig. 56 - Test circuit and simplified power-gain calculation for a transistor operated in a common-emitter configuration.

Although the input resistance r_{in} affects the power gain, as shown by the equations given in Fig. 56, this parameter is not usually specified directly in the published data on transistors because of the large number of

components of which it is comprised. In general, the input impedance is expressed as a maximum base-to-emitter voltage V_{BE} under specified input-current conditions.

A measure of the current gain of a transistor is its **forward current-transfer ratio**, i.e., the ratio of the current in the output electrode to the current in the input electrode. Because of the different ways in which transistors may be connected in circuits, the forward current-transfer ratio is specified for a particular circuit configuration.

The current gain (or current transfer ratio) of a transistor is expressed by many symbols; the following are some of the most common, together with their particular shades of meaning:

1. beta (β)—general term for current gain from base to collector (i.e., common-emitter current gain)

2. alpha (α)—general term for current gain from emitter to collector (i.e., common-base current gain)

3. h_{fe}—ac gain from base to collector (i.e., ac beta)

4. h_{FE}—dc gain from base to collector. (i.e., dc beta)

Common-base current gain, α, is the ratio of collector current to emitter current (i.e., $\alpha = I_C / I_E$). Although α is slightly less than unity, circuit gain is realized as a result of the large differences of input (emitter-base) and output (collector-base) impedances. The input impedance is small because the emitter-base junction is forward-biased, and the output impedance is large because the collector-base junction is reverse-biased.

Common-emitter current gain, β, is the ratio of collector current to base current (i.e., $\beta = I_C / I_B$). Useful values of β are normally greater than ten.

Transconductance

Extrinsic transconductance may be defined as the quotient of a small change in collector current divided by the small change in emitter-to-base voltage producing it, under the condition that other voltages remain unchanged. Thus, if an emitter-to-base voltage change of 0.1 volt causes a collector-current change of 3 milliamperes (0.003 ampere) with other voltages constant, the transconductance is 0.003 divided by 0.1, or 0.03 mho. (A "mho" is the unit of conductance, and was named by spelling "ohm" backward.) For convenience, a millionth of a mho, or a micromho (μmho), is used to express transconductance. Thus, in the example, 0.03 mho is 30,000 micromhos.

Cutoff Frequencies

For all transistors, there is a frequency f at which the output signal cannot properly follow the input signal because of time delays in the transport of the charge carriers. The three principal cut-off frequencies, shown in Fig. 57, may be defined as follows:

1. The **base cut-off frequency** $f_{\alpha b}$ is that frequency at which alpha (α) is down 3 dB from the low-frequency value.

2. The **emitter cut-off frequency** $f_{\alpha e}$ is that frequency at which beta (β) is down 3 dB from the low-frequency value.

3. The frequency f_T is that frequency at which beta theoretically decreases to unity (i.e., 0-dB gain) with a theoretical 6-dB-per-octave fall off. This term, which is a useful figure of merit for transistors, is referred to as the **gain-bandwidth product**.

The gain-bandwidth product f_T is the term that is generally used to indicate the high-frequency capability of a transistor. Other parameters that critically affect high-frequency


$$\beta = \frac{\alpha}{(1-\alpha) + j\omega/\omega_{ab}}$$
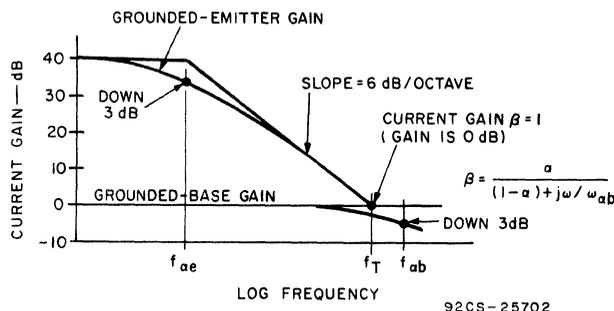
Fig. 57 - Cut-off frequencies.

performance are the capacitance or resistance which shunts the load and the input impedance, the effect of which is shown by the equations given in Fig. 56.

The base and emitter cut-off frequencies and the gain-bandwidth product of a transistor provide an approximate indication of the useful frequency range of the device, and help to determine the most suitable circuit configuration for a particular application.

The specification of all the characteristics which affect high-frequency performance is so complex that often a manufacturer does not specify all the parameters, but instead specifies transistor performance in a specific amplifier circuit. This information is very useful when the transistor is operated under conditions very similar to those of the test circuit, but is difficult to apply when the transistor is used in a widely different application. Some manufacturers also specify transistor performance characteristics as a function of frequency, which alleviates these problems.

Cutoff Currents

Cutoff currents are small steady-state reverse currents which flow when a transistor is biased into non-conduction. They consist of **leakage currents**, which are related to the surface characteristics of the semiconductor material, and **saturation currents**, which are related to the impurity concentration in the material and which increase with increasing temperatures. Collector-cutoff current is the steady-state current which flows in the reverse-biased collector-to-base circuit when the emitter-to-base circuit is open. Emitter-cutoff current is the current which flows in the reverse-biased emitter-to-base circuit when the collector-to-base circuit is open.

In the common-base configuration, the collector reverse (leakage) current, I_{CBO}, is measured with the emitter circuit open. The presence of the second junction, however, still affects the level of the current because the emitter acquires a small negative bias when it is open-circuited. This bias reduces the hole gradient at the collector and causes the reverse current to decrease. This current, therefore, is much smaller with the emitter open than it is when the emitter-base junction is short-circuited.

The reverse current increases with collector voltage, and may lead to avalanche breakdown at high voltages.

The common-emitter reverse collector current I_{CEO}, measured with zero input current ($I_B=0$ in this case), is very much larger than the reverse collector current I_{CBO} in the common-base connection. When the base current is zero, the emitter current adjusts itself so that the losses in the hole-injection and diffusion mechanisms are exactly balanced by the supply of excess electrons left in the vicinity of the collector by hole extraction. For this condition, the collector current is equal to the emitter current.

The common-emitter reverse collector current I_{CEO} increases with collector voltage, unlike the common-base reverse collector current I_{CBO}. This behavior is another consequence of the variation in the effective base width with collector voltage. The narrower the effective base region, the more efficient is the transfer of current from emitter to collector. The more efficient base transport with the higher collector voltage permits a higher emitter current to flow before the losses are again balanced by the supply of electrons from the vicinity of the collector.

Breakdown Voltages

Transistor breakdown voltages define the voltage values between two specified electrodes at which the crystal structure changes and current begins to rise rapidly. The voltage then remains relatively constant over a wide range of electrode currents. Breakdown voltages may be measured with the third electrode open, shorted, or biased in either the forward or the reverse direction. For example, Fig. 58 shows a series of collector-characteristic curves for different base-bias conditions. It can be seen that the collector-to-emitter breakdown voltage increases as the base-to-emitter bias decreases from the normal forward values through zero to reverse values. The symbols shown on the abscissa are sometimes used to designate collector-to-emitter breakdown voltages with the base open $V_{(BR)CEO}$, with external base-to-emitter resistance $V_{(BR)CER}$, with the base shorted to the emitter $V_{(BR)CES}$, and with a reverse base-to-emitter voltage $V_{(BR)CEV}$.

As the resistance in the base-to-emitter circuit decreases, the collector characteristic develops two breakdown points, as shown in Fig. 58. After the initial breakdown, the collector-to-emitter voltage decreases with increasing collector current until another breakdown occurs at a lower voltage. This
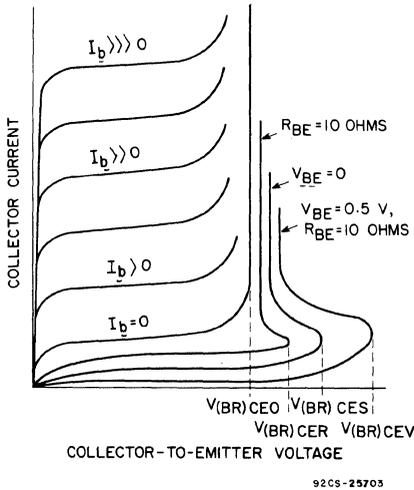
Fig. 58 - Typical collector-characteristic curves showing locations of various breakdown voltages.

minimum collector-to-emitter breakdown voltage is called the **sustaining voltage**.

Punch-Through Voltage

Punch-through (or reach-through) voltage defines the voltage value at which the depletion region in the collector region passes completely through the base region and makes contact at some point with the emitter region. This "reach-through" phenomenon results in a relatively low-resistance path between the emitter and the collector, and causes a sharp increase in current. Punch-through voltage does not result in permanent damage to a transistor, provided there is sufficient impedance in the power-supply source to limit transistor dissipation to safe values.

Saturation Voltage

The curves at the left of Fig. 58 show typical collector characteristics under normal forward-bias conditions. For a given base input current, the collector-to-emitter saturation voltage is the minimum voltage required to maintain the transistor in full conduction (i.e., in the saturation region). Under saturation conditions, a further increase in forward bias produces no corresponding increase in collector current. Saturation voltages are very important in switching applications, and are usually specified for several conditions of electrode currents and ambient temperatures.

Effect of Temperature on Transistor Characteristics

The characteristics of transistors vary with changes in temperature. In view of the fact that most circuits operate over a wide range of environments, a good circuit design should compensate for such changes so that operation is not adversely affected by the temperature dependence of the transistors.

Current Gain—The effect of temperature on the gain of a silicon transistor is dependent upon the level of the collector current, as shown in Fig. 59. At the lower current levels, the current-gain parameter h_{FE} increases with temperature. At higher currents, however, h_{FE} may increase or decrease with a rise in temperature because it is a complex function of many components.
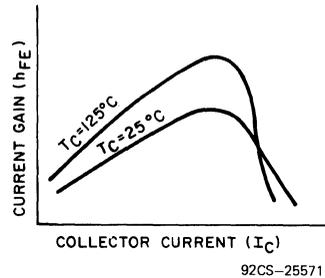
Fig. 59 - Current gain as a function of collector current at different temperatures.

Base-to-Emitter Voltage—Fig. 60 shows the effect of changes in temperature on the base-to-emitter voltage (V_{BE}) of silicon transistors. As indicated, the base-to-emitter voltage diminishes with a rise in temperature for low values of collector current, but tends to increase with a rise in temperature for higher values of collector current.
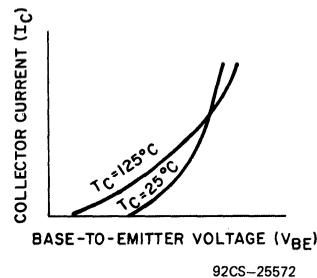
Fig. 60 - Collector current as a function of base-to-emitter voltage at different temperatures.

Collector-to-Emitter Saturation Voltage—

The collector-to-emitter saturation voltage (V_{CE}(sat)) is affected primarily by collector resistivity (ρ_c) and the amount by which the natural gain of the device (h_{FE}) exceeds the gain with which the circuit drives the device into saturation. This latter gain is known as the forced gain (h_{FEf}).

At lower collector currents, the natural h_{FE} of a transistor increases with temperature, and the IR drop in the transistor is small. The collector-to-emitter saturation voltage, therefore, diminishes with increasing temperature if the circuit continues to maintain the same forced gain. At higher collector currents, however, the IR drop increases, and gain may decrease. This decrease in gain causes the collector-to-emitter saturation voltage to increase and possibly to exceed the room-temperature (25°C) value. Fig. 61 shows the effect of temperature on the collector-to-emitter saturation voltage.
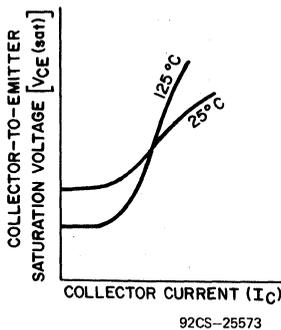
Fig. 61 - Collector current as a function of collector-to-emitter saturation voltage at different temperatures.

Collector Leakage Currents—Reverse collector current I_R is a resultant of three components, as shown by the following equation:

$$I_R = I_D + I_G + I_S$$

Fig. 62 shows the variations of these components with temperature.

Leakage currents are important because they affect biasing in amplifier applications and represent the off condition for transistors used in switching applications. The symbol I_R used in the preceding discussion represents any of several different leakage currents commonly specified by transistor manufacturers. The most basic specification is I_{CBO}, which indicates the leakage from collector to
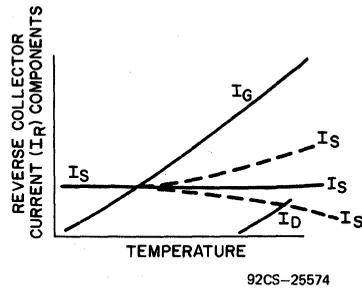
Fig. 62 - Reverse collector current as a function of temperature.

base with the emitter open. This leakage is simply the reverse current of the collector-to-base diode.

In addition to the I_{CBO} value, I_{CEV}, I_{CEO}, and I_{CER} specifications are often given for transistors. I_{CEV} is the leakage from the collector to emitter with the base-emitter junction reverse-biased. I_{CER} is the leakage current from the collector to the emitter with the base and emitter connected by a specified resistance, I_{CEO} is the leakage current from collector to emitter with the base open. I_{CEV} differs from I_{CBO} only very slightly and in most transistors the two parameters can be considered equal. (This equality is not maintained in symmetrical transistors.) I_{CEO} is simply the product of I_{CBO} at the voltage specified and the h_{FE} of the transistor at a base current equal to I_{CBO}. I_{CEO} is of course the largest leakage current normally specified. I_{CER} is intermediate in value between I_{CEV} and I_{CEO}.

POWER TRANSISTORS IN SWITCHING SERVICE

An important application of power transistors is power switching. Large amounts of power, at high currents and voltages, can be switched with small losses by use of a power transistor that is alternatively driven from cutoff to saturation by means of a base control signal. The two most important considerations in such switching applications are the speed at which the transistor can change states between saturation and cutoff and the power dissipation.

Transistor switching applications are usually characterized by large-signal nonlinear operation of the devices. The switching transistor is generally required to operate in either of two states: on or off. In transistor switching circuits, the common-emitter configuration is by far the most widely used.

Typical output characteristics for an n-p-n transistor in the common-emitter configuration are shown in Fig. 63. These characteristics are divided into three regions of operation, i.e., cutoff region, active region, and saturation region.

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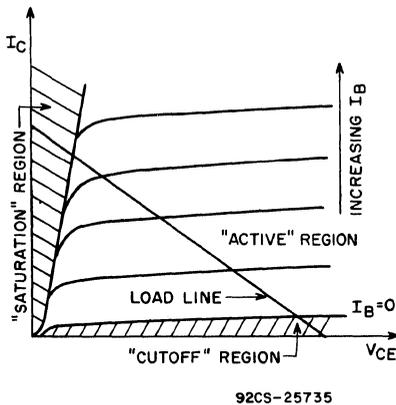
Fig. 63 - Typical collector characteristic of an n-p-n transistor showing three principal regions involved in switching.

In the cutoff region, both the emitter-base and collector-base junctions are reverse-biased. Under these conditions, the collector current is very small, and is comparable in magnitude to the leakage current I_{CEO}, I_{CEV}, or I_{CBO}, depending on the type of base-emitter biasing used.

Fig. 64 is a sketch of the minority-carrier concentration in an n-p-n transistor. For the cutoff condition, the concentration is zero at both junctions because both junctions are reverse-biased, as shown by curve 1 in Fig. 64.

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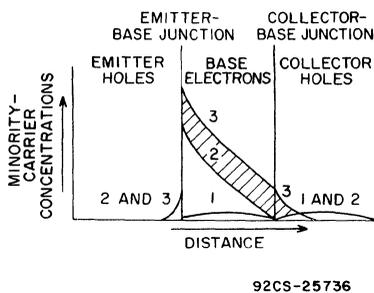
Fig. 64 - Minority-carrier concentrations in an n-p-n transistor: (1) in cutoff region, (2) in active region at edge of saturation region, (3) in saturation region.

In the active region, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased. Switching from the cutoff region to the active region is accomplished along a load line, as indicated in Fig. 63. The speed of transition through the active region is a function of the frequency-response characteristics of the device. The minority-carrier concentration for the active region is shown by curve 2 in Fig. 64.

The remaining region of operation is the saturation region. In this region, the emitter-base and collector-base junctions are both forward-biased. Because the forward voltage drop across the emitter-base junction under this condition [$V_{BE}(sat)$] is greater than that across the collector-base junction, there is a net collector-to-emitter voltage referred to as $V_{CE}(sat)$. It is evident that any series-resistance effects of the emitter and collector also enter into determining $V_{CE}(sat)$. Because the collector is now forward-biased, additional carriers are injected into the base, and some into the collector. This minority-carrier concentration is shown by curve 3 in Fig. 64.

A basic saturated-transistor switching circuit is shown in Fig. 65. The voltage and current

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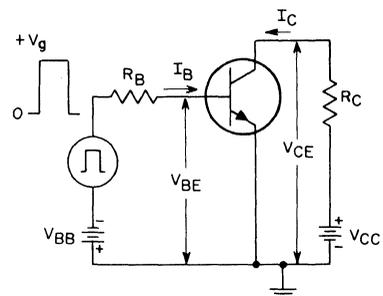
Fig. 65 - Basic saturated transistor switching circuit.

waveforms for this circuit under typical base-drive conditions are shown in Fig. 66. Prior to the application of the positive-going input pulse, the emitter-base junction is reverse-biased by a voltage $-V_{BE}(off) = V_{BB}$. Because the transistor is in the cutoff region, the base current I_B is the reverse leakage current I_{BEV}, which is negligible compared with I_{B1}, and the collector current I_C is the reverse leakage current I_{CEV}, which is negligible compared with V_{CC}/R_C.

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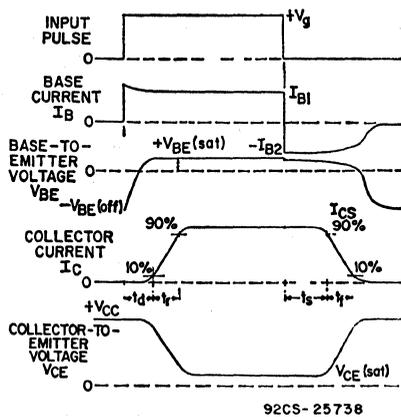
Fig. 66 - Voltage and current waveforms for saturated switching circuit shown in Fig. 65.

When the positive-going input pulse V_g is applied, the base current I_B immediately goes positive. The collector current, however, does not begin to increase until some time later. This delay in the flow of collector current (t_d) results because the emitter and collector capacitances do not allow the emitter-base junction to become forward-biased instantaneously. These capacitances must be charged from their original negative potential [$-V_{BE}$(off)] to a forward bias sufficient to cause the transistor to conduct appreciably. After the emitter-base junction is sufficiently forward-biased, there is an additional delay caused by the time required for minority carriers which are injected into the base to diffuse across the base and be collected at the collector. This delay is usually negligible compared with the delay introduced by the capacitive component. The collector and emitter capacitances vary with the collector-base and emitter-base junction voltages, and increase as the voltage V_{BE} goes positive. An accurate determination of total delay time, therefore, requries knowledge of the nonlinear characteristics of these capacitances.

When the collector current I_C begins to increase, the transistor has made the transition from the cutoff region into the active region. The collector current takes a finite time to reach its final value. This time, called rise time (t_r), is determined by the gain-bandwidth product (f_T), the collector-to-emitter capacitance (C_C), and the static forward current-transfer ratio (h_{FE}) of the transistor. At high collector currents and/or low collector volt-

ages, the effect of this capacitance on rise time is negligible, and the rise time of collector current is inversely proportional to f_T. At low currents and/or high voltages, the effect of gain-bandwidth product is negligible, and the rise time of collector current is directly proportional to the product $R_C C_C$. At intermediate currents and voltages, the rise time is proportional to the sum $(\frac{1}{2}\pi f_T) + R_C C_C$. Under any of the above conditions, the collector current responds exponentially to a step of base current. If a turn-on base current (I_{B1}) is applied to the device, and the product $I_{B1} h_{FE}$ is less than V_{CC}/R_C, the collector current rises exponentially until it reaches the steady-state value $I_{B1} h_{FE}$. If $I_{B1} h_{FE}$ is greater than V_{CC}/R_C, the collector current rises toward the value $I_{B1} h_{FE}$. The transistor becomes saturated when I_C reaches the value $I_{CS}(\approx V_{CC}/R_C)$. At this point, I_C is effectively clamped at the value V_{CC}/R_C.

The rise time, therefore, depends on an exponential function of the ratio $I_{CS}/I_{B1}{:}h_{FE}$. Because the values of h_{FE}, f_T, and C_C are not constant, but vary with collector voltage and current as the transistor is switching, the rise time as well as the delay time is dependent on nonlinear transistor characteristics.

After the collector current of the transistor has reached a steady-state value I_{CS}, the minority-charge distribution is that shown by curve 3 in Fig. 66. When the transistor is turned off by returning the input pulse to zero, the collector current does not change immediately. This delay is caused by the excess charge in the base and collector regions, which tends to maintain the collector current at the I_{CS} value until this charge decays to an amount equal to that in the active region at the edge of saturation (curve 2 in Fig. 66). The time required for this charge to decay is called the storage time (t_S). The rate of charge decay is determined by the minority-carrier lifetime in the base and collector regions, on the amount of reverse "turn-off" base current (I_{B2}), and on the overdrive "turn-on" current (I_{B1}) which determined how deeply the transistor was driven into saturation. (In non-saturated switching, there is no excess charge in the base region, so that storage time is negligible.)

When the stored charge (Q_S) has decayed to the point where it is equal to that at the edge of saturation, the transistor again enters the active region and the collector current begins

to decrease. This fall-time portion of the collector-current characteristic is similar to the rise-time portion because the transistor is again in the active region. The fall time, however, depends on I_{B2}, whereas the rise time was dependent on I_{B1}. Fall time, like rise time, also depends on f_T and C_C.

The approximate values of I_{B1}, I_{B2}, and I_{CS} for the circuit shown in Fig. 65 are given by:

$$I_{B1} = \frac{V_G - V_{BB} - V_{BE}(sat)}{R_B}$$

$$I_{B2} = \frac{V_{BB} + V_{BE}(sat)}{R_B}$$

$$I_{CS} = \frac{V_{CC} - V_{CE}(sat)}{R_C}$$

Switching Characteristics

The electrical characteristics for a switching transistor, in general, differ from that for a linear-amplifier type of transistor in several respects. The static forward current-transfer ratio h_{FE} and the saturation voltages $V_{CE}(sat)$ and $V_{BE}(sat)$ are of fundamental importance in a switching transistor. The static forward current-transfer ratio determines the maximum amount of current amplification that can be achieved in any given circuit, saturated or non-saturated. The saturation voltages are necessary for the proper dc design of saturated circuits. Consequently, h_{FE} is always specified for a switching transistor, generally at two or more values of collector current. $V_{CE}(sat)$ and $V_{BE}(sat)$ are specified at one or more current levels for saturated transistor applications. Control of these three characteristics determines the performance of a given transistor type over a broad range of operating conditions. For non-saturated applications, $V_{CE}(sat)$ and $V_{BE}(sat)$ need not be specified. For such applications, it is important to specify V_{BE} at specific values of collector current and collector-to-emitter voltage in the active region.

Because the collector and emitter capacitances and the gain-bandwidth product influence switching time, these characteristics are specified for most switching transistors. The collector-base and emitter-base junction capacitances are usually measured at some value of reverse bias and are designated C_{ob} and C_{ib}, respectively. The gain-bandwidth product (f_T) of the transistor is the frequency at which the small-signal forward current-transfer ratio (h_{fe}) is unity. Because this characteristic falls off at 6 dB per octave above the corner frequency, f_T is usually controlled by specifying the h_{fe} at a fixed frequency anywhere from $1/2$ to $1/10$ f_T. Because C_{ob}, C_{ib}, and f_T vary nonlinearly over the operating range, these characteristics are generally more useful as figures of merit than as controls for determining switching speeds. When the switching speeds in a particular application are of major importance, it is preferable to specify the required switching speeds in the desired switching circuit rather than C_{ob}, C_{ib}, and f_T.

The storage time (t_S) of a transistor is dependent on the stored charge (Q_S) and on the driving current employed to switch the transistor between cutoff and saturation. Consequently, either the stored charge or the storage time under heavy overdrive conditions should be specified. Most recent transistor specifications require that storage time be specified.

Because of the dependence of the switching times on current and voltage levels, these times are determined by the voltages and currents employed in circuit operation.

Dissipation, Current, and Voltage Ratings

Up to this point, no mention has been made of dissipation, current, and voltage ratings for a switching transistor. The maximum continuous ratings for dissipation and current are determined in the same manner as for any other transistor. In a switching application, however, the peak dissipation and current may be permitted to exceed these continuous ratings depending on the pulse duration, on the duty factor, and on the thermal time constant of the transistor.

Voltage ratings for switching transistors are more complicated. In the basic switching circuit shown in Fig. 65, three breakdown voltages must be considered. When the transistor is turned off, the emitter-base junction is reverse-biased by the voltage $V_{BE}(off)$, (i.e., V_{BB}), the collector-base junction by $V_{CC} + V_{BB}$, and the emitter-to-collector junction by $+V_{CC}$. To assure that none of the voltage ratings for the transistor is exceeded under "off" conditions, the following requirements must be met:

The minimum emitter-to-base breakdown voltage $V_{(BR)EBO}$ must be greater than $V_{BE}(off)$.

The minimum collector-to-base breakdown voltage $V_{(BR)CBO}$ must be greater than $V_{CC} + V_{BE}(off)$.

The minimum collector-to-emitter breakdown voltage $V_{(BR)CERL}$ must be greater than V_{CC}.

$V_{(BR)EBO}$ and $V_{(BR)CBO}$ are always specified for a switching transistor. The collector-to-emitter breakdown voltage $V_{(BR)CEO}$ is usually specified under open-base conditions. The breakdown voltage $V_{(BR)CERL}$ (the subscript "RL" indicates a resistive load in the collector circuit) is generally higher than $V_{(BR)CEO}$. The requirement that $V_{(BR)CEO}$ be greater than V_{CC} is overly pessimistic. The requirement that $V_{(BR)CERL}$ be greater than V_{CC} should be used wherever applicable.

Coupled with the breakdown voltages are the collector-to-emitter and base-to-emitter transistor leakage currents. These leakage currents (I_{CEV} and I_{BEV}) are particularly important considerations at high operating temperatures. The subscript "V" in these symbols indicates that these leakage currents are specified at a given emitter-to-base voltage (either forward or reverse). In the basic circuit of Fig. 65, these currents are determined by the following conditions:

$$I_{CEV} \Big\} \quad V_{CE} = V_{CC}$$
$$I_{BEV} \Big\} \quad V_{BE} = V_{BE}(off) = -V_{BB}$$

In a switching transistor, these leakage currents are usually controlled not only at room temperature, but also at some higher operating temperature near the upper operational limit of the transistor.

Inductive Switching

Most inductive switching circuits can be represented by the basic equivalent circuit shown in Fig. 67. This type of circuit requires a rapid transfer of energy from the switched inductance to the switching mechanism, which may be a relay, a transistor, a commutating diode, or some other device. Often an accurate calculation of the energy to be dissipated in the switching device is required, particularly if that device is a transistor. If the supply voltage is low compared to the sustaining breakdown

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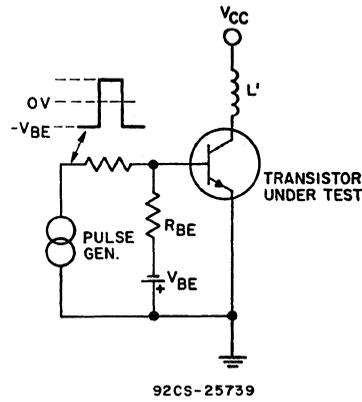
Fig. 67 - Basic equivalent circuit for inductive switching circuit.

voltage of the transistor and if the series resistance of the inductor can be ignored, then the energy to be dissipated is $\frac{1}{2} LI^2$. This type of rating for a transistor is called "reverse-bias second breakdown." The energy capability of a transistor varies with the load inductance and base-emitter reverse bias. A typical set of ratings which now appears in RCA published data is shown in Fig. 68.

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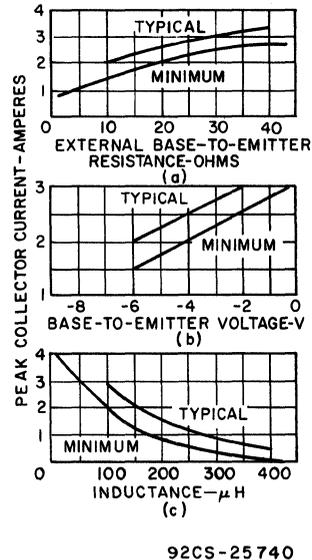
Fig. 68 - Typical reverse-bias second-breakdown ($E_{S/b}$] rating curves.

Linear Regulators for DC Power Supplies

All linear voltage regulators can be classified as either **series** or **shunt** types, as determined by the arrangement of the pass element with respect to the load. In a series regulator, as the name implies, the pass transistor is connected in series with the load. Regulation is accomplished by variation of the current through the series pass transistor in response to a change in the line voltage or circuit loading. In this way, the voltage drop across the pass transistor is varied and that delivered to the load circuit is maintained essentially constant. In the shunt regulator, the pass transistor is connected in parallel with the load circuit, and a voltage-dropping resistor is connected in series with this parallel network. If the load current tends to fluctuate, the current through the pass transistor is increased or decreased as required to maintain an essentially constant current through the dropping resistor.

BASIC POWER-SUPPLY ELEMENTS

A dc power supply converts the power from the ac line into a direct current and steady voltage of a desired value. The ac input voltage is first rectified to provide a pulsating dc and is then filtered to produce a smooth voltage. Finally, the voltage may be regulated to assure that a constant output level is maintained despite fluctuations in the power-line voltage or circuit loading. The rectification, filtering, and regulation steps in a dc power supply are illustrated in Fig. 69.

Rectifier Circuits

The optimum type of rectifier circuit for a particular application depends upon the dc voltage and current requirements, the maximum amount of ripple (undesirable fluctuations in the dc output caused by an ac component) that can be tolerated in the circuit, and the type of power available. Single-phase circuits are used to provide the relatively low dc power required for radio and television receivers, public-address systems, and similar types of electronic equipment. Polyphase rectifier circuits are used to provide the dc power in high-power industrial applications.

Polyphase circuits more fully take advantage of the capabilities of the rectifier and power transformer and, in addition, provide a dc output with a small percentage of ripple. Polyphase rectifiers circuits, therefore, require
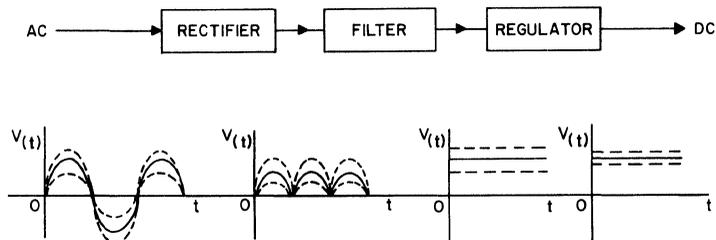
Fig. 69 - Block diagram of a regulated dc power supply. The waveforms show the effects of rectification, filtering, and regulation. (Dashed lines indicate voltage fluctuations as a result of input variations)

less filtering of the dc output voltage than is required for the dc output from single-phase rectifier circuits.

Rectifier Voltage and Current Ratios

Table IV lists voltage and current ratios for the basic rectifier circuits shown in Figs. 70 through 72 and in Figs. 78 through 81. For most effective use of the rectifiers and power transformers, operation of the rectifier circuits into inductive loads, except for the single-phase half-wave type, is generally recom-

mended. Current ratios given for inductive loads are applicable only when a filter choke (inductance) is used between the output of the rectifier and any capacitor in the filter circuit. The values shown neglect the voltage drops in the power transformer, the silicon rectifiers, and the filter components that occur when load current is drawn. When a specific type of rectifier has been selected for a specific circuit, the information given in Table IV can be used to determine the parameters and characteristics of the circuit.
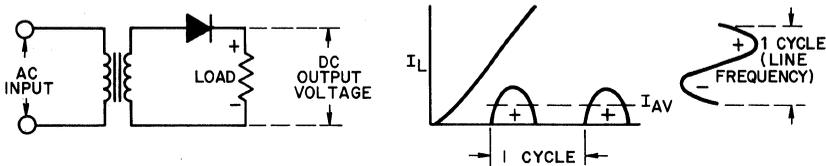
Fig. 70 - Single-phase half-wave rectifier and load-current waveform.
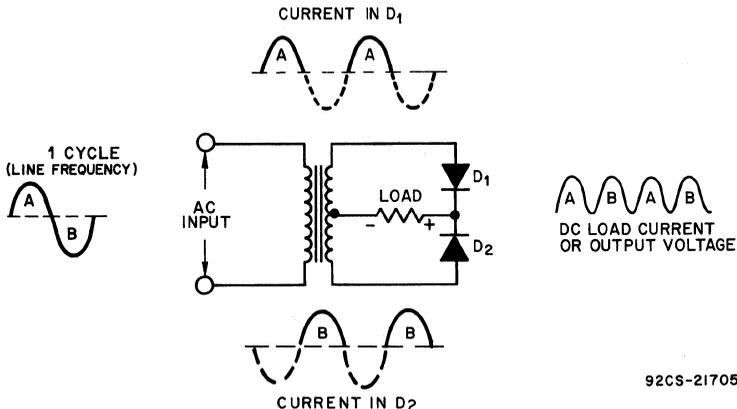
Fig. 71 - Single-phase full-wave rectifier circuit with center-tapped transformer.
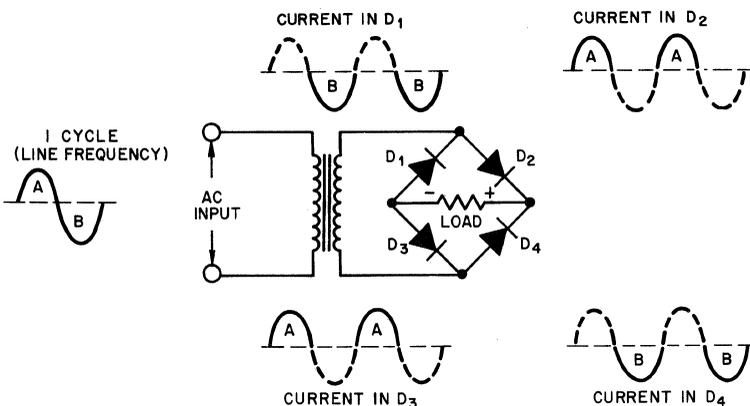
Fig. 72 - Full-wave bridge rectifier without center-tapped power transformer.

CURRENT IN D_1

1 CYCLE
(LINE FREQUENCY)

AC INPUT

CURRENT IN D_2

92CS-21707
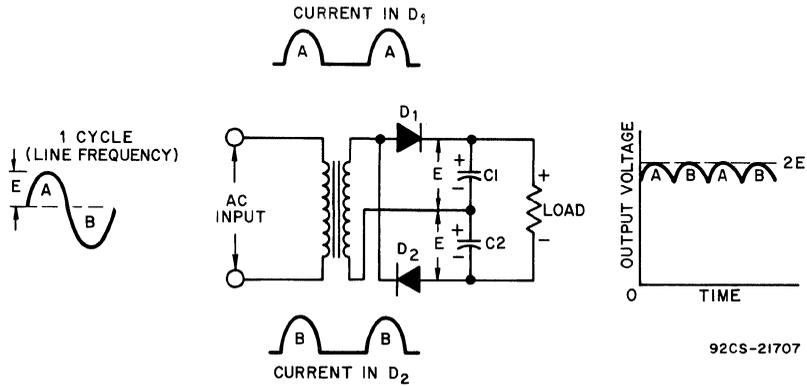
Fig. 73 - Full-wave voltage-doubler circuit.

VOLTAGE AT POINT A

AC INPUT

1 CYCLE
(LINE FREQUENCY)
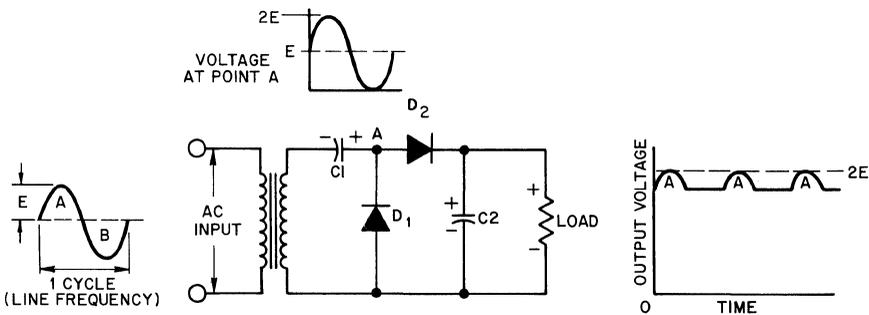
Fig. 74 - Half-wave voltage-doubler circuit.

E_{OUT}

APPLIED AC
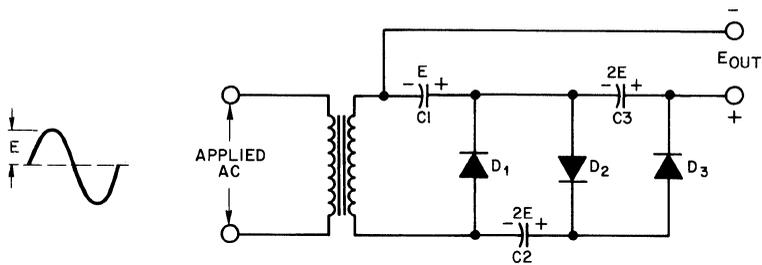
Fig. 75 - Half-wave voltage-tripler circuit.

FIRST SECTION

mTH SECTION

APPLIED AC

$n = 2m$
$E_{OUT} = 2mE$

E_{OUT}
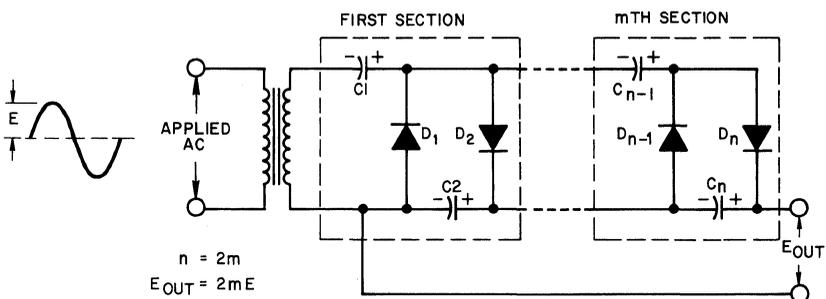
Fig. 76 - Half-wave "n" multiplier rectifier circuit.

$$m = \frac{n+1}{2}$$

$$V_{OUT} = DC + mV_1 + (n-1)(V_2)$$

(a)

$$n = 2m$$

$$V_{OUT} = m(V_1 + V_2)$$

(b)

V_1 = POSITIVE PORTION OF PULSE VOLTAGE ACROSS HIGH-VOLTAGE WINDING

V_2 = NEGATIVE PORTION OF PULSE VOLTAGE ACROSS HIGH-VOLTAGE WINDING
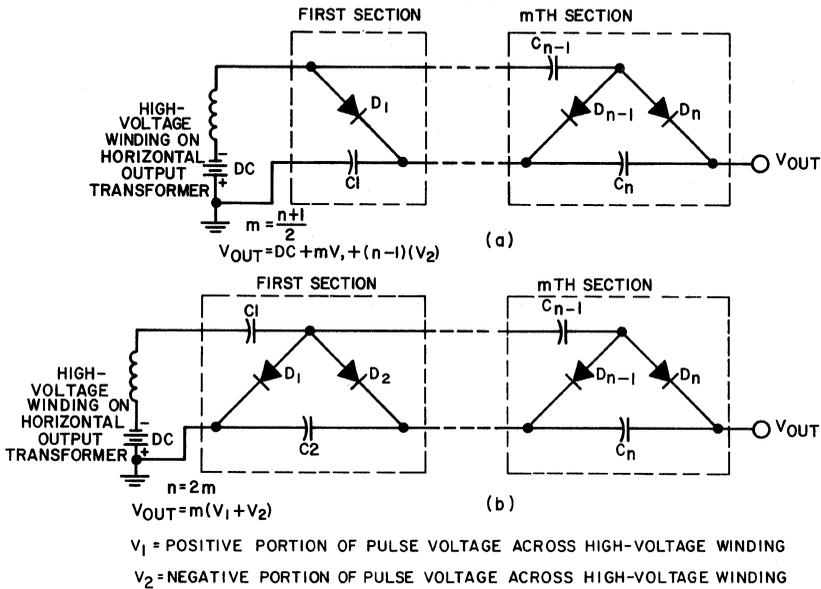
Fig. 77 - Basic multiplier circuits: (a) with odd number of diodes; (b) with even number of diodes.
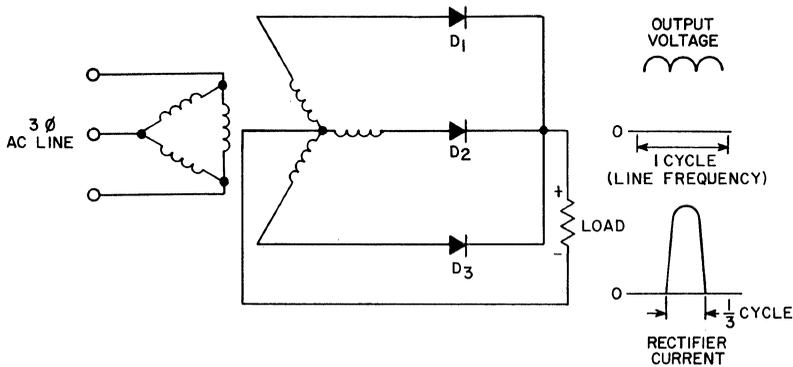
Fig. 78 - Three-phase half-wave delta-wye circuit.
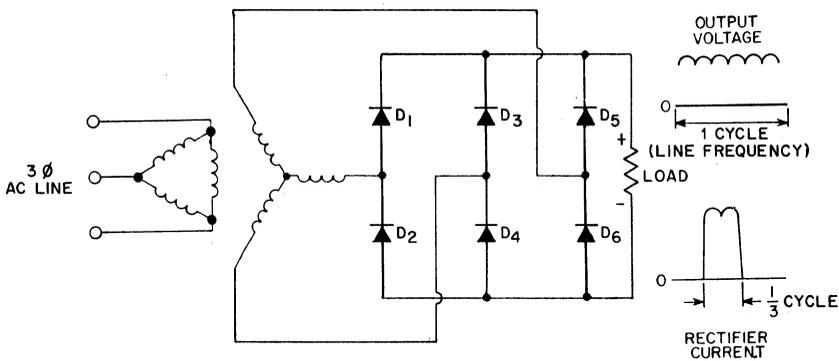
Fig. 79 - Three-phase, full-wave, delta-wye bridge rectifier.
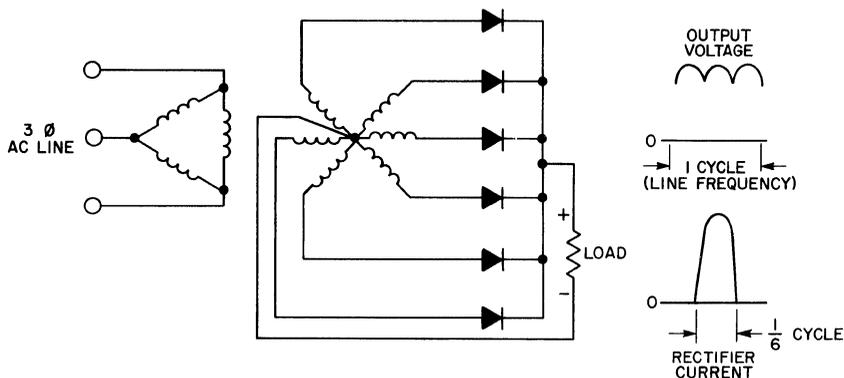
Fig. 80 - Three-phase, delta-star (six-phase), half-wave rectifier.
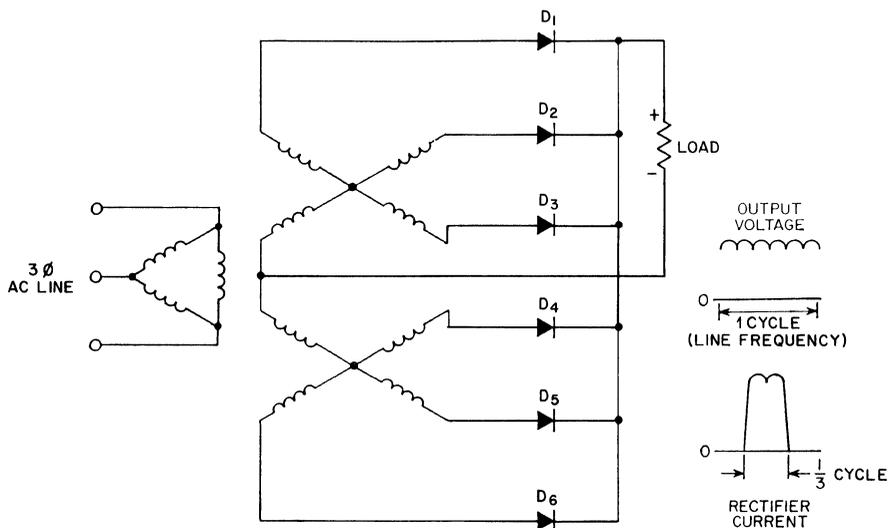
Fig. 81 - Three-phase, half-wave, double-wye and interphase transformer circuit.

Filter Networks

In general, the output-voltage waveform of a dc power supply should be as flat as possible (i.e., should approach a pure dc). The objective, therefore, is a voltage waveform that has a peak-to-average ratio of unity. The output of a basic rectifier circuit, however, is a series of positive or negative pulses rather than a pure dc voltage. The rectifier output may be considered as a steady dc voltage with an alternating voltage superimposed on it. For most applications, this alternating voltage (ripple) must be removed (filtered out), or the equipment in which the power supply is used will not operate properly.

Figs. 82 through 86 illustrate the various types of filter networks and the resulting degree of ripple content appearing at the output.

Table IV—Normalized Characteristics for Rectifier Circuits With Resistance and Choke-Input-Filtered Loads*

E	= Transformer Secondary Voltage (rms)
E_{av}	= Average DC Output Voltage
E_m	= Peak Transformer Secondary Voltage
E_{bmi}	= Peak Inverse Anode Voltage
E_r	= Major Ripple Voltage (rms)
F	= Supply Frequency
t_r	= Major Ripple Frequency
I_{av}	= Average DC Output Current
I_b	= Average Anode Current
I_p	= Anode Current (rms)
I_{pm}	= Peak Anode Current
P_{ap}	= Transformer Primary Volt-Amperes
P_{as}	= Transformer Secondary Volt-Amperes
P_{dc}	= DC Power = (E_{av} x I_{av})

Item	1-Phase Half-Wave (Fig. 70)	1-Phase Full-Wave (Fig. 71)	1-Phase Full-Wave Bridge (Fig. 72)	3-Phase Half-Wave Delta-Wye (Fig. 78)	3-Phase Full-Wave Delta-Wye (Fig. 79)	3-Phase Half-Wave Delta-Star (Fig. 80)	3-Phase Half-Wave Double-Wye with Bal. Coil (Fig. 81)
Voltage Ratios							
E_m/E_{av}	3.14	1.57	1.57	1.21	1.05	1.05	1.05
E/E_{av}	2.22	1.11	1.11	0.854	0.74	—	0.854
E_{bmi}/E	1.41	2.83	1.41	2.45	2.83	2.83	2.45
E_{bmi}/E_{av}	3.14	3.14	1.57	2.09	2.09	2.42	2.09
E_r/E_{av}	1.11	0.471	0.471	0.177	0.040	—	0.04
Frequency Ratio							
■f_r/f	1	2	2	3	6	6	6
Current Ratios							
■I_b/I_{av}	1	0.5	0.5	0.333	0.167	0.167	0.167
Resistive Load							
I_p/I_{av}	1.57	0.785	0.785	0.587	0.409	0.409	0.294
I_{pm}/I_{av}	3.14	1.57	1.57	1.21	1.05	1.05	0.525
I_{pm}/I_b	3.14	3.14	3.14	3.63	6.3	6.30	3.14
Inductive Load°							
I_p/I_{av}	*	0.707	0.707	0.577	0.408	0.408	0.289
I_{pm}/I_{av}	*	1.00	1.00	1.00	1.00	1.00	0.5

Notes:

*Conditions assume sine-wave voltage supply; zero voltage drop across rectifiers when conducting; no losses in transformer or choke; output load is a pure resistance.

° The use of a large filter-input choke is assumed.

* Single-phase, half-wave, choke-input-filtered load has no practical significance; only a minute pulsating dc current will flow.

■These ratios also apply for the case of capacitor-input filtered load.
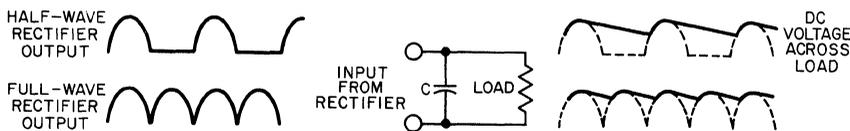
Fig. 82 - Single capacitor filter.
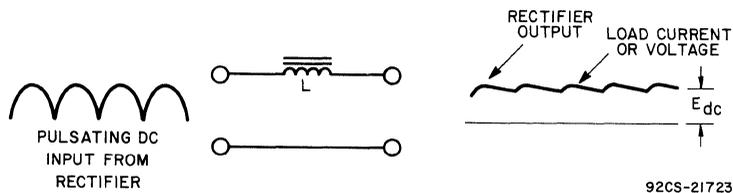
Fig. 83 - Simple inductance filter.
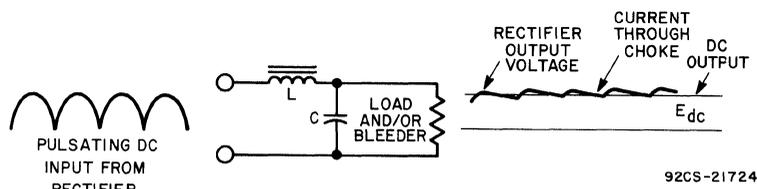
Fig. 84 - Choke-input filter.
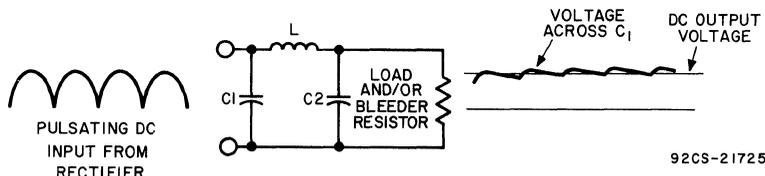
Fig. 85 - Capacitor-input LC filter.
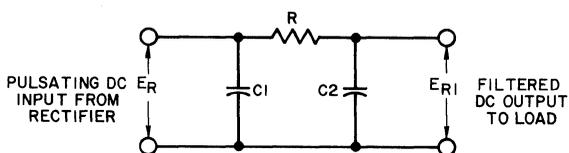
Fig. 86 - Resistance-capacitance filter.

SERIES REGULATORS

Series-regulated power supplies are classified as voltage-regulating types, voltage-regulating current-limiting types, current-regulating types, or voltage-regulating current-regulating types. Fig. 87 shows the response characteristics for each type of series-regulated power supply.

Linear series regulators provide an excellent means for prevention of large variations in power-supply load current or output voltage. Fast response time provided by the linear control circuit makes possible close control of the output voltage. However, because the series pass transistor is equivalent to a variable resistance in series with the load, the transistor must dissipate a large amount of power at low output voltages. Another disadvantage of the series regulator is that the total fault current passes through the regulating transistor if the load becomes short-circuited. As a result,

overload and short-circuit protection in the form of current-limiting or drive-reduction networks that operate rapidly must be used to protect the transistor.
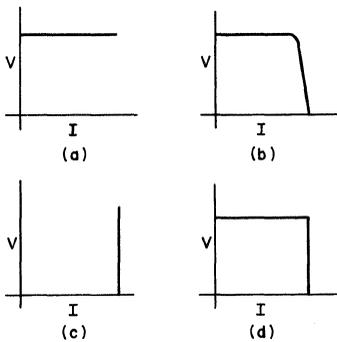
Fig. 87 - Typical response characteristics for series-regulated power supplies: (a) voltage-regulating types; (b) voltage-regulating current-limiting types; (c) current-regulating types; (d) voltage-regulating current-regulating types.

Basic Circuit Configurations

Fig. 88 shows a basic configuration for a linear series regulator which is representative of the type used in **voltage-regulating power supplies**. In this type of regulator, the series pass transistor is usually operated as an emitter-follower, and the control (error) signal used to initiate the regulating action is applied to the base. The base control is developed by a dc amplifier. This amplifier, which is included in the feedback loop from the load circuit to the pass transistor, senses any change in the output voltage by comparison of this voltage with a known reference voltage. If an error exists, the error voltage is amplified and applied to the base of the pass transistor. The conduction of the pass transistor is then increased or decreased in response to the error signal input as required to maintain the output voltage at the desired value.
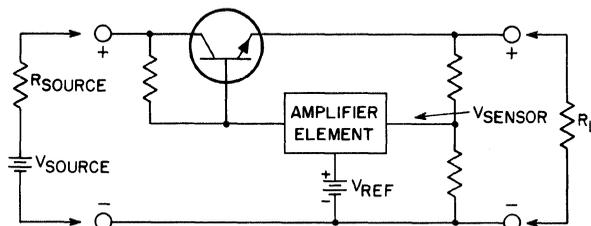
Voltage-regulating power supplies are required to maintain a constant output voltage, independent of the load current, as shown in Fig. 87(a). The supply, therefore, usually has a very low output impedance. For this reason, voltage-regulating supplies must often be made current-limiting to protect the regulator from very high current drawn at the output terminal, such as may be caused by a short circuit. In **voltage-regulating current-limiting power supplies**, the load current is prevented from rising above some predetermined design value by reduction of the power-supply output voltage when this current limit is reached, as shown in Fig. 87(b).

Fig. 89 shows the basic configuration for a linear regulator circuit used in **current-regulating power supplies**. This regulator senses the voltage across a resistor in series with the load, rather than the voltage across the load circuit as in the linear voltage regulator. Because the voltage across the series resistor is directly proportional to the load current, a detected error signal can be used to cancel any tendency for a change in load current from the desired value. Ideally, the linear current regulator has an infinite output impedance and output characteristics as shown in Fig. 87(a).

The regulator circuit used with **voltage-regulating current-regulating power supplies** is essentially a combination of the other types of linear regulators. As shown in Fig. 87(d), the output response characteristics of this type of regulated supply exhibit a crossover point at which the supply switches from voltage regulation to current regulation.

Fig. 90 shows a block diagram of a voltage-regulating current-regulating power supply. The input ac power is rectified and filtered and is then applied to the regulating circuit. When preregulators are used, as is normally the case, switching types are preferred. The efficiency of the switching regulator is extremely high, and a fast response time to load or line

Fig. 88 - Basic series voltage regulator.
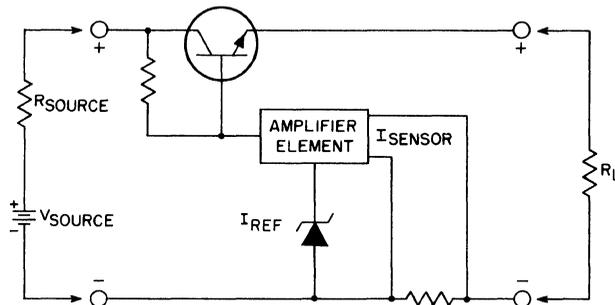
*Fig. 89 - Basic series regulator modified
for current sensing.*
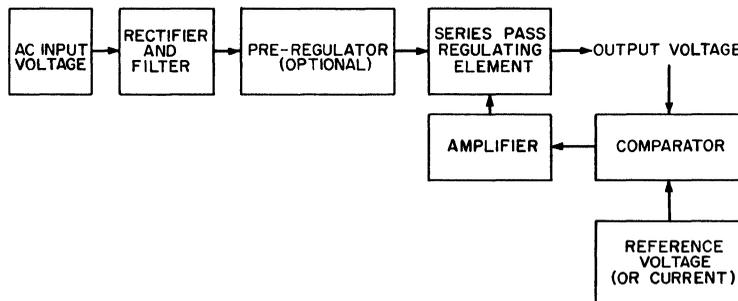
*Fig. 90 - Block diagram of series voltage-
regulating current-regulating dc
power supply.*

variations is not required at this point in the circuit. (The operation and characteristics of switching regulators are discussed later in the section on **Switching Regulators**.)

The output from the preregulator is transferred to the series pass element which provides the fast response time for the entire regulating circuit. At this point in the circuit, a sample of the output voltage is compared with a reference voltage and the resulting error signal, which is proportional to the difference between these voltages, is amplified and delivered to the base of the pass transistor to correct the output voltage.

In this type of system, the resulting output voltage is highly dependent upon the accuracy of the reference supply. Such a voltage source may be a temperature-compensated zener diode in series with a very constant source of current so that the diode incremental resistance has no effect on the output voltage. The sensitivity of the regulator is an inverse function of the gain of the drive amplifier. The smaller the variation to be sensed, the higher the required gain of the amplifier. A higher gain, however, results in less stability.

Performance Parameters

Most voltage-regulated power supplies are required to provide voltage regulation for wide variations in load current. It is important, therefore, to specify the output impedance of the supply, $\Delta V_{out}/\Delta I_{out}$, over a large band of frequencies. This parameter indicates the ability of the power supply to maintain a constant output voltage during rapid changes in load. The output impedance of a typical voltage-regulated supply is normally less than 0.1 ohm at all frequencies below 2 kHz. Above this frequency, the impedance increases and may be as much as several ohms.

A power supply must continue to supply a constant voltage (or current) regardless of variations in line voltage. An index of its ability to maintain a constant output voltage or current during input variation is called the **line regulation** of the supply, which is defined as 100 (V_o'/V_o), or as the change in output voltage ΔV_o, for a specified change in input voltage, expressed in per cent. Typical values of line regulation are less than 0.01 per cent.

Another important power-supply parameter is **load regulation**, which specifies the amount

that the regulated output quantity (voltage or current) changes for a given change in the unregulated quantity. Load regulation is mainly a function of the stability of the reference source and the gain of the feedback network.

A power-supply parameter referred to as **recovery time** denotes the time required for the regulated quantity (voltage or current) to return to the specified limits when a step change in load is applied, as shown in Fig. 91.
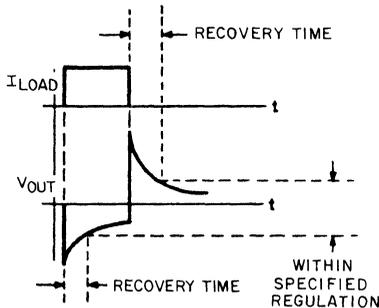
Fig. 91 - *Typical recovery-time character-istics for regulated dc power supplies.*

Recovery time is a function of the frequency response of the feedback network of the power supply. For voltage-regulated supplies, the "roll-off" of the feedback network increases the output impedance at high frequencies, and the impedance becomes inductive. As a result, the high-frequency harmonics of the step change in the load current induce a spike of voltage at the output.

The amount of change in the output voltage of the regulated power supply from an initial value over a specified period of time is referred to as **drift**. This parameter is measured after an initial warm-up period with a constant input voltage and load applied and the ambient temperature held constant.

Transistor Requirements

In linear series regulators, the transistor parameters that affect circuit design and performance are collector dissipation, maximum collector current $I_C(max)$, leakage current (I_{CER} in most cases), current gains h_{FE} and h_{fe}, collector-to-emitter saturation voltage V_{CE} (sat), collector-to-emitter breakdown voltage $V_{CEO}(sus)$, and second breakdown.

The collector-dissipation rating limits the amount of power which the series transistor can safely dissipate when the power supply is

short-circuited. The maximum collector current $I_C(max)$ limits the total current which the regulator can handle. A low value of leakage current is required to maintain the stability of the circuit and, possibly, to prevent thermal runaway. This requirement makes silicon transistors especially suitable for use as the regulator pass element because leakage current is generally much lower in silicon transistors than in germanium types. The current-gain parameters h_{FE} and h_{fe} determine the amount of drive current needed at various collector current levels. The ac forward-current transfer ratio h_{fe} also determines the output impedance of the supply. A high h_{fe} results in a low output impedance. The saturation voltage $V_{CE}(sat)$ is one factor that determines the required input voltage to the regulator for a specified output voltage and current. The collector-to-emitter breakdown voltage V_{CEO} (sus) limits the maximum output voltage of the power supply. Second-breakdown considerations in circuit applications of transistors were discussed previously in the section on **Power Transistor Ratings and Characteristics**.

Current-Limiting Techniques

One of the problems encountered in the design of series transistor voltage regulators is protection of the series control element from excess dissipation because of current overloads and short circuits.

In some series voltage-regulator circuits, overloading results in permanent damage to the series control transistor. For example, when the output terminals of the regulator circuit shown in Fig. 92 are shorted, the full input voltage and available current are applied to the series control transistor. This power usually is many times greater than the dissipation ratings of the series transistor.
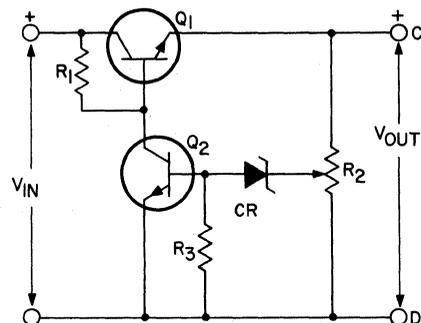
Fig. 92 - *Series voltage regulator without current limiting.*

A series fuse is sometimes used in an attempt to protect the series transistor from this excessive dissipation. A series fuse cannot usually provide the necessary protection under all overload conditions, however, because the thermal time constant of the fuse is normally much greater than that of the transistor.

Protection for all overload conditions may be accomplished by use of a circuit which limits the current to a safe value, as determined from the dissipation rating of the series regulator transistor. An effective current-limiting circuit must respond fast enough to protect the series transistor and yet permit the circuit to return to normal regulator operation as soon as the overload condition is removed. It is desirable to achieve current-overload protection with minimum degradation of regulator performance.

One method of achieving limiting is to use a resistor in series with the regulator transistor. The large resistance normally required, however, dissipates a large amount of power and degrades the regulator performance.

The current-limiting section (dashed line) of the regulator circuit shown in Fig. 93(a) is designed to appear as a large series resistance during current overload and as a negligible resistance during normal operating conditions. The value of resistance R_5 is designed so that, during normal regulator operation, transistor Q_4 operates in the saturated condition. For the overload condition, R_4 is adjusted so that the maximum allowable value of overload current through this resistor produces a voltage drop large enough to cause silicon rectifier CR_1 to conduct. Conduction of CR_1 reduces the bias to Q_4, so that the transistor appears as an increasing series resistance in the regulator circuit.
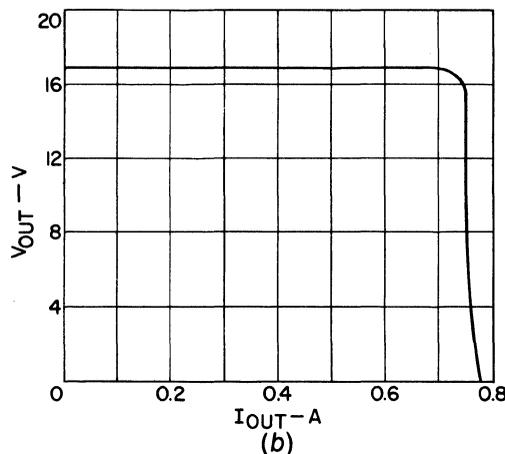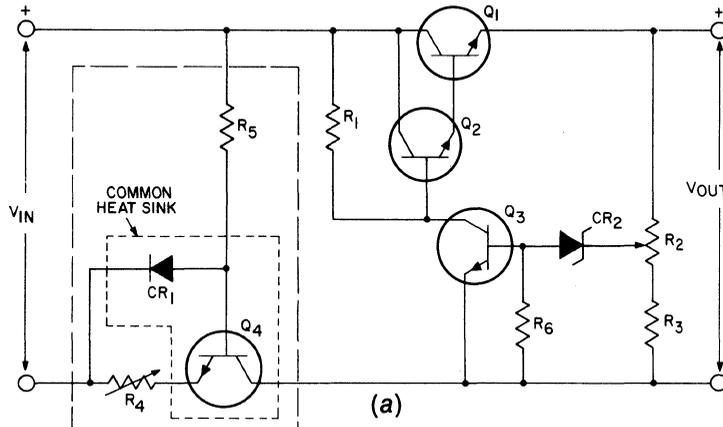
Fig. 93 - Series voltage regulator with transistor current-limiting circuit (inside dashed lines) added: (a) schematic diagram; (b) response characteristics.

Under short-circuit conditions, the entire value of input voltage V_{in} appears across Q_4 simultaneously with the limiting value of current. Transistor Q_4 must be capable of withstanding the resulting dissipation. When the current limit is reached, the junction temperature of Q_4 rises to a value considerably above the ambient temperature. This increase in junction temperature causes the value of short-circuit current to rise slightly because of the inherent variation of the base-to-emitter voltage V_{BE} with temperature in transistors. This effect is minimized by mounting silicon rectifier CR_1 and transistor Q_4 on a common heat sink so that their respective junction temperatures may reach the same value (the values of their respective V_{BE} and forward-voltage-drop temperature coefficients are comparable).

Performance characteristics for the transistor series voltage regulator of Fig. 93(a) are shown in Fig. 93(b).

Although the series-regulator circuit shown in Fig. 93(a) provides adjustable current limiting with simple circuitry and minimum power loss during normal operation, it has the disadvantage of requiring a second series transistor capable of withstanding short-circuit output current and total input voltage simultaneously.

(a)

(b)
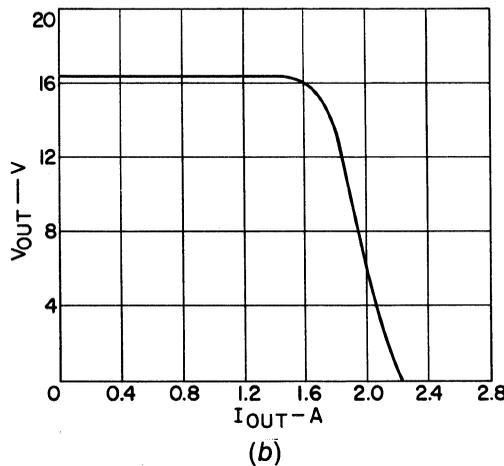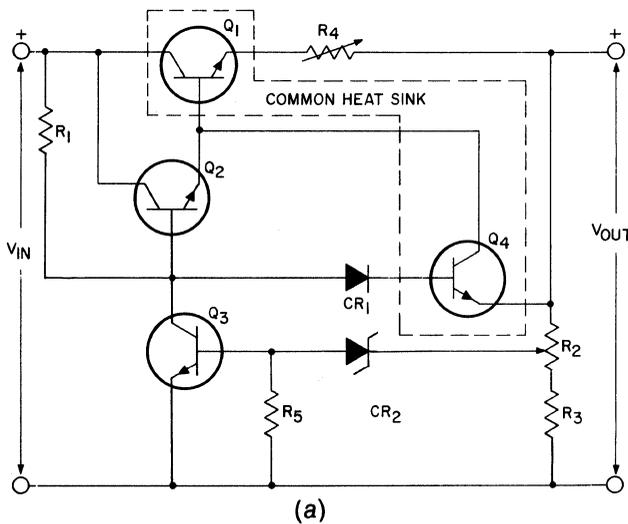
Fig. 94 - Series voltage regulator using pass transistor as part of current-limiting circuit: (a) schematic diagram; (b) response characteristics (for R_4=0).

In many high-current high-voltage regulator circuits, it is necessary to use parallel or series connections of pass transistors so that the voltage, current, and power ratings of the series control element are not exceeded. The method shown in Fig. 93(a) may not be practical in this application because of the additional series transistor required. The circuit shown in Fig. 94(a) eliminates the need for an additional series transistor by use of the series regulator transistor as the current-limiting element. This method is very effective when a Darlington connection is used for the series control transistor. A desirable feature of this circuit in high-current regulators is that it functions well even when the value of resistor R_4 is reduced to zero.

In the circuit shown in Fig. 94(a), current limiting is achieved by the combined action of the components shown inside the dashed lines. The voltage developed across R_4 and the base-to-emitter voltages of Q_1 and Q_2 are proportional to the circuit output current. During current overload, these voltages add up to a value great enough to cause CR_1 and Q_4 to conduct. As CR_1 and Q_4 begin to conduct, Q_4 shunts a portion of the bias available to the series regulator transistor.

This action, in turn, increases the series resistance of Q_1. The value of current in the circuit, under current-limiting conditions, is adjusted by varying the value of resistance R_4.

Higher current ranges may be obtained by increasing the number of rectifiers represented by CR_1. Temperature drift is minimized by mounting transistors Q_1 and Q_4 on a common heat sink. Performance characteristics for this circuit (for $R_4 = 0$) are shown in Fig. 94(b).

The circuit shown in Fig. 95(a) is a variation of that shown in Fig. 94(a). Current limiting is adjusted by varying R_4 and by changing the number of silicon rectifiers represented by CR_1. Temperature drift is minimized by mounting the series control transistor Q_1 and silicon rectifier CR_1 on a common heat sink. Performance characteristics for this circuit are shown in Fig. 95(b). The circuits shown in Figs. 94 and 95 are both applicable to high-current high-voltage regulators because additional series power transistors are not required.

Fig. 96(a) shows another current-limiting circuit in which the regulator series control transistor is used as the current-limiting element. The series element must be capable of withstanding input voltage and short-circuit current simultaneously. The value of short-

(a)

(b)
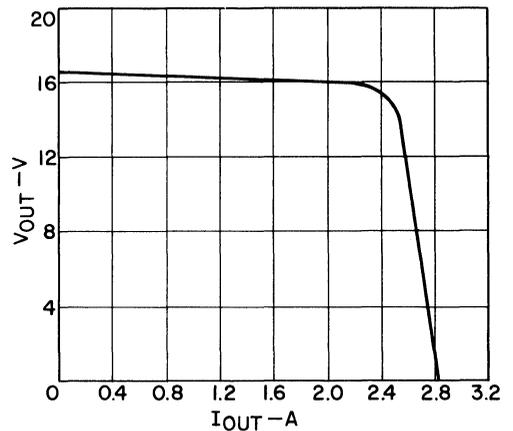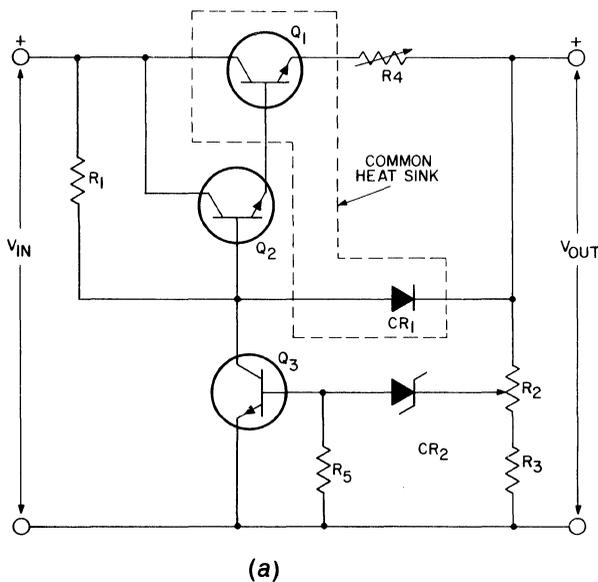
Fig. 95 - Series voltage regulator which uses additional transistor-diode network and series pass transistor to accomplish current-limiting function: (a) schematic diagram; (b) response characteristics.
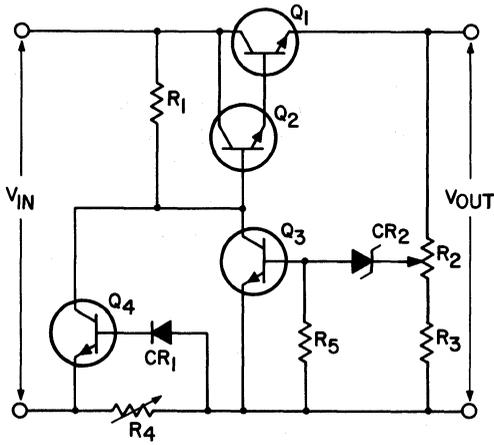
(a)
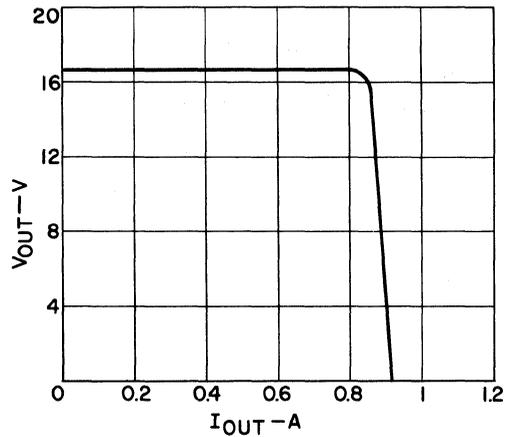
(b)

Fig. 96 - *Current-limiting series voltage regulator in which series pass transistor must be capable of withstanding input voltage and short-circuit current simultaneously: (a) schematic diagram; (b) response characteristics.*

circuit current is selected by adjusting the value of resistor R_4. Performance characteristics of this circuit are shown in Fig. 96(b). The circuit functions equally well with resistor R_4 located in the positive output lead.

Foldback Current Limiting

Foldback current limiting is a form of protection against excessive current. If the load impedance is reduced to a value that would draw more than the predetermined maximum current, the foldback circuit reduces output voltage and thus reduces the current. Further reduction of load impedance causes further decrease of output voltage and current; therefore a regulated power supply that includes a foldback current-limiting circuit has the voltage-current characteristic shown in Fig. 97. The foldback process is reversible; if the load impedance is increased while the circuit is in the limiting mode, the output voltage and current increase. When the current reaches the threshold level, the regulator is re-activated, and the power supply returns to normal operation.

For additional information on the Design of Current Regulated Supplies, refer to **RCA Solid State Power Circuits Handbook**, SP-52 Series.
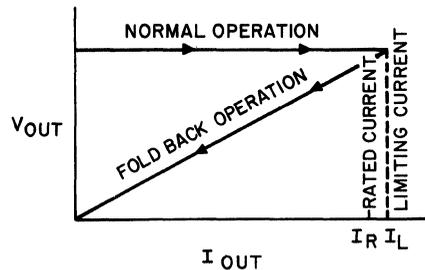
Fig. 97 - *Output characteristic of a regulated power supply with foldback current-limiting protection for pass transistor.*

A foldback current-limiting circuit is shown in Fig. 98. At low output current, transistor Q_5 is cut off; the value of resistor R_5 is selected so that Q_5 has zero bias when the output current reaches its rated value, I_R. When the load current I_{OUT} reaches the limiting value, I_X, Q_5 begins to conduct; current flows through resistor R_2, transistor Q_4 turns on, and the base-to-emitter voltage of transistor Q_3 is reduced. Therefore, the base-to-emitter voltage of transistor Q_2 decreases, and the output voltage of the power supply decreases. This decrease in the output voltage V_{OUT} reduces the output current, so that Q_5 continues to conduct at the same emitter current. If the load impedance is reduced further, Q_5 is
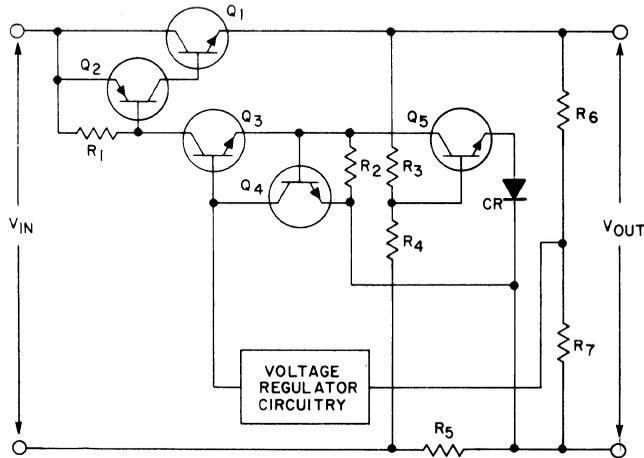
*Fig. 98 - Foldback-current-limiting cir-
cuitry in a series voltage regulator*
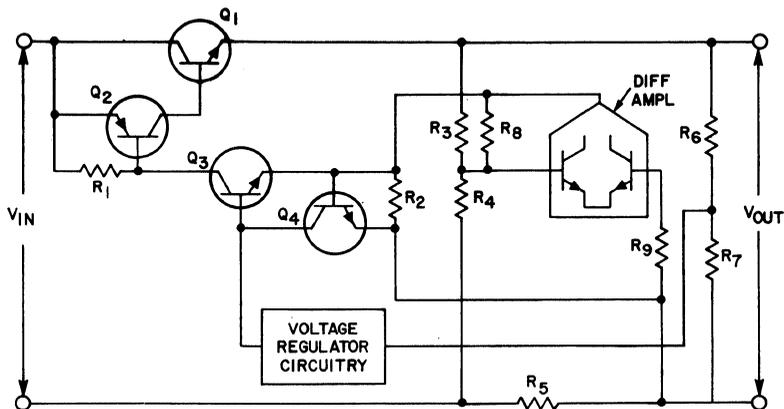
*Fig. 99 - Foldback-current-limiting circuit
with a differential amplifier for
greater sensitivity.*

driven even harder, and the output voltage and current decrease even further.

Improved foldback-circuit performance can be achieved by use of a differential amplifier instead of single-ended amplifier Q_5. With the improved circuit, illustrated in Fig. 99.

FOLDBACK—LIMITED REGULATED SUPPLY

Fig. 100 shows a series regulated power supply with foldback current limiting. This supply can deliver currents of up to 3 amperes at 20 volts. The circuit uses integrated circuits for the regulation and protection functions; the voltage regulator is an RCA-CA3085A and the foldback limiter uses an RCA-CA3030 operational amplifier as a linear differential amplifier.

Circuit Description

Specifications for the 60-watt, 20-volt supply shown in Fig. 100 are listed on page 69. The circuit uses an external pass transistor and driver to extend the current capability of the RCA-CA3085A integrated circuit voltage regulator; the overload protection provided

by a foldback current-limiting circuit permits operation of the transistor at a dissipation level close to its limit. This foldback circuit achieves high efficiency by use of an RCA-CA3030 integrated circuit operational amplifier.

The over-all operation of the circuit can be understood with the aid of the schematic diagram shown in Fig. 100. Transformer T1 and its rectifiers supply the raw dc power that is regulated by pass transistor Q_1; this pass transistor is driven by driver Q_2, which is driven by the CA3085A voltage regulator. Transformer T2, with its rectifiers and shunt regulator Q_4, provides positive and negative supplies for the operational amplifier CA3030. This operational amplifier drives the current-limiting control Q_3. Output voltage is sensed at resistance string ($R_6 + R_{13}$), and load current is sensed by R_S.

Voltage Regulation

The power-supply output voltage is sampled by the voltage divider ($R_6 + R_{13}$), and a portion is fed to terminal No. 6 (the inverting input) of the CA3085A. (This portion is less than the 3.3-volt breakdown voltage of the type 1N5225 zener diode; the zener is present only to protect the integrated circuit from accidental overvoltages.) If the output voltage decreases, the base-to-emitter voltage of Q_2 increases, as explained in the next paragraph. Therefore the pass transistor Q_1 is driven harder, and as a result the output voltage increases to its original value (minus the error dictated by the system gain).

The process by which a voltage decrease at
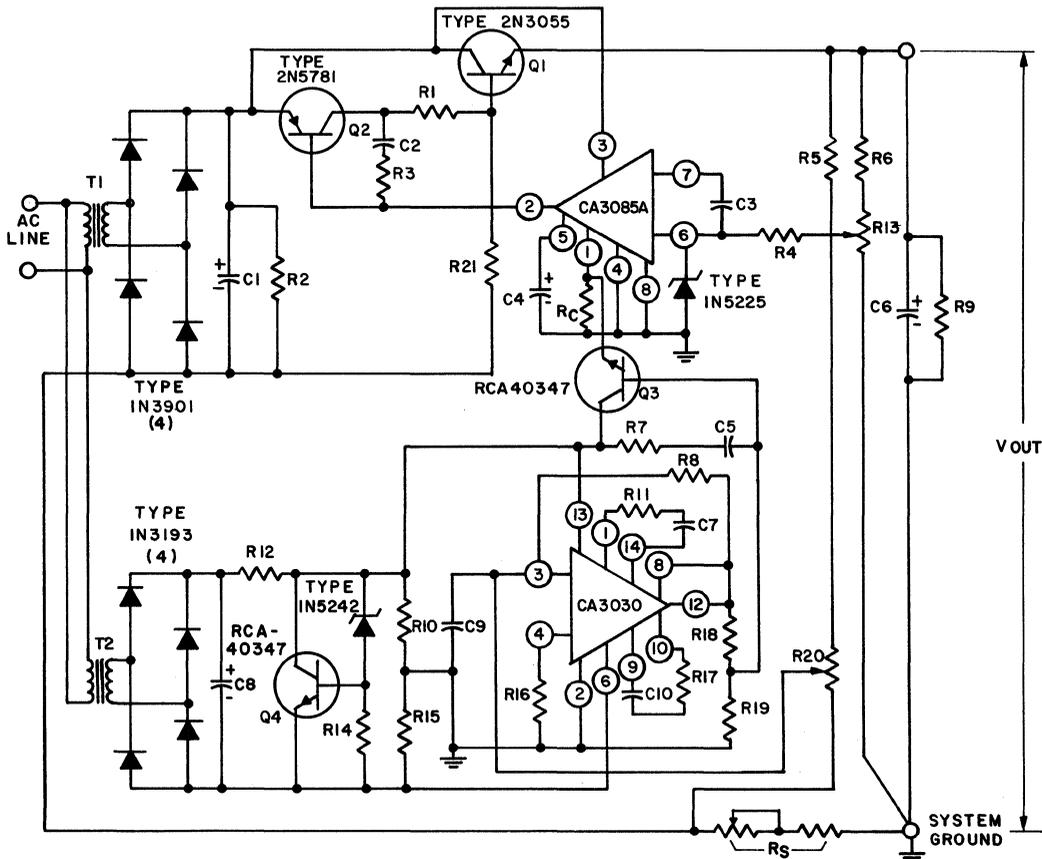
Fig. 100 - Schematic diagram of a dc power supply that uses integrated circuits in the voltage regulator and foldback-current-limiting circuitry.

Parts List for Schematic Diagram of Fig. 100

T_1=Signal Transformer Co.,
Part No. 24-4 or equivalent

T_2=Signal Transformer Co.,
Part No. 12.8-0.25 or equivalent

C_1=5900 μF, 75 V, Sprague Type
36D592F075BC or equivalent

C_2=0.005 μF, ceramic disc,
Sprague TGD50 or equivalent

C_3, C_7, C_{10}=50 pF, ceramic disc,
Sprague 30GA-Q50 or equivalent

C_4=2 μF, 25 V, electrolytic, Sprague
500D G025BA7 or equivalent

C_5=0.01 μF, ceramic disc, Sprague
TG510 or equivalent

C_6=500 μF, 50 V, Cornell-Dubilier
No. BR500-50 or equivalent

C_8=250 μF, 25 V, Cornell-Dubilier
BR 250-25 or equivalent

C_9=0.47 μF, film type, Sprague
Type 220P or equivalent

R_1=5 ohms, 1 watt, IRC type
BWH or equivalent

R_2=1000 ohms, 5 watts, Ohmite
type 200-5 ¼ or equivalent

R_3=1200 ohms, ½ watt, carbon,
IRC Type RC ½ or equivalent

R_4=100 ohms, ½ watt, carbon,
IRC Type RC ½ or equivalent

R_5=430 ohms, 2 watt, wire wound
IRC Type BWH or equivalent

R_6=9100 ohms, 2 watts, wire wound,
IRC Type BWH or equivalent

R_7=470 ohms, ½ watt, carbon,
IRC type ½ or equivalent

R_8=5100 ohms, ½ watt, carbon,
IRC type RC ½ or equivalent

R_9,R_{14}=1000 ohms 2 watts, wire
wound, IRC type BWH or
equivalent

R_{10},R_{15}=250 ohms, 2 watts, 1% wire
wound, IRC type AS-2 or
equivalent

R_{11},R_{17}=1000 ohms, ½ watt, carbon,
IRC type RC ½ or equivalent

R_{12}=82 ohms, 2 watts, IRC type
BWH or equivalent

R_{13}=1000 ohms, potentiometer,
Clarostat Series U39 or equivalent

R_{16}=1200 ohms, 2 watts, wire
wound, IRC type BWH or
equivalent

R_{38}=510 ohms, ½ watt, carbon,
IRC type RC ½ or equivalent

R_{19}=10,000 ohms, ½ watt, carbon,
IRC type RC ½ or equivalent

R_{20}=300 ohms, potentiometer,
Clarostat Series U39 or equivalent

R_{21}=510 ohms, 3 watts, wire wound,
Ohmite type 200-3 or equivalent

R_C=240 ohms, 1%, wire wound,
IRC type AS-2 or equivalent

R_S=(See text for fixed portion);
1 ohm, 25 watts, Ohmite type H or
equivalent

Miscellaneous

(1 Req'd)—Heat Sink, Delta
Division Wakefield Engineering
NC-423 or equivalent

(3 Req'd)—Heat Sink, Thermalloy
#2207 PR-10 or equivalent

(1 Req'd)—8-pin socket Cinch
#8-1CS or equivalent

(1 Req'd)—14-pin DIL socket, T.I.,
#ICO14ST-7528 or equivalent

(2 Req'd)—TO-5 socket ELCO
#05-3304 or equivalent

Vector Board #838AWE-1 or
equivalent

Vector Receptacle R644 or
equivalent

Chassis—As required

Cabinet—As required

Dow Corning DC340 filled grease

60-Watt, 20-Volt Power-Supply Specifications

V_{input}	105-130 V, Single Phase, 55-420 cps	Transients: No load to full load: 100 mV, recovery within 50 μs	
V_{output}	20 V ±0.5 V	Full load to no load: 100 mV, recovery within 50 μs	
I_{load}(max)	3 A		
Ambient Temperature	0 to +55°C	Drift	20 mV in 8 hours of operation at constant ambient temperature
Voltage spikes	None at turn-on or turn-off		
Regulation	Line: ±0.25% Load: ±0.25%	Short Circuit and Overcurrent Protection	Foldback technique
Ripple	33 mV pp; 9.5 mV rms		

terminal No. 6 of the CA3085A produces an increase of Q_2 base-to-emitter voltage can be understood with the aid of Fig. 101, which shows some of the internal circuitry of the CA3085A. The drop of voltage at terminal No. 6 causes a higher base-to-emitter voltage at the Darlington combination Q_{13}-Q_{14}. Therefore the collector current of Q_{14} increases, and thus increases the voltage drop across the 500-ohm resistor, which is the base-to-emitter voltage of Q_2.

Fig. 102 - Foldback current-limiting characteristic.

The foldback current-limiting circuit shown in Fig. 103 uses the CA3030 integrated circuit as a differential amplifier. A signal from the voltage divider R_{R1} and R_{R2}*, which is across V_O and the E_{BB} return, is applied to the inverting input (terminal No. 3) of the CA3030. The non-inverting input is tied to system ground through R_{16}. Thus the base-to-base signal that actuates the CA3030 is the difference between $V_{RS}(=I_O R_S)$ and V_{RR2}. The CA3030 output, which is the voltage at terminal No. 12, varies linearly with the actuating voltage, as shown in Fig. 104. When the load current is zero*, V_{RS} is zero; therefore $(V_{RS}-V_{RR2})$ is negative, terminal 12 is negative with respect to ground, and Q_3 is back-biased (i.e., cut off). Therefore Q_3 does not interfere with the normal voltage-regulated operation of the supply. As the load current increases, V_{RS} increases and the voltage at terminal 12 increases.

Fig. 101 - CA3085A control of the power transistors.

Foldback Current-Limiting Circuit

The purpose of the current-limiting circuit is to prevent the power supply from passing a load current that could damage the pass transistor if a very low impedance (or a short circuit) is placed across the output terminals. Fig. 102 shows the effect of this circuit. The supply voltage remains constant until the load current reaches the threshold for activation of the limiting circuit; any further decrease of load impedance causes output voltage V_O and load current I_O to decrease, so that the V_O-I_O characteristic folds back to limit the power dissipation in the pass transistor. Activation of the foldback limiting circuit disables the voltage-regulation circuit.

*R_{R1} actually consists of R_5 and the upper portion of R_{20} in the schematic diagram of Fig. 100. R_{R2} is the lower portion of R_{20}.

The value of resistor R_S is adjusted so that when the load current reaches the foldback-activation value (about 3 amperes in the power supply shown), the voltage at terminal No. 12 of the CA3030 becomes positive. At about 0.7 volt, transistor Q_3 begins to conduct; current flows through the current-limiting resistor R_C, with the result that terminal No. 1 of the CA3085A control circuit is driven positive. Q_{15} of Fig. 101 turns on, and the base-to-emitter voltage of Q_{13}-Q_{14} is therefore reduced; the base-to-emitter voltage of Q_2 is reduced, and the output voltage of the power supply decreases. This decrease of V_O tends to reduce the load current; however, V_{RR2} also
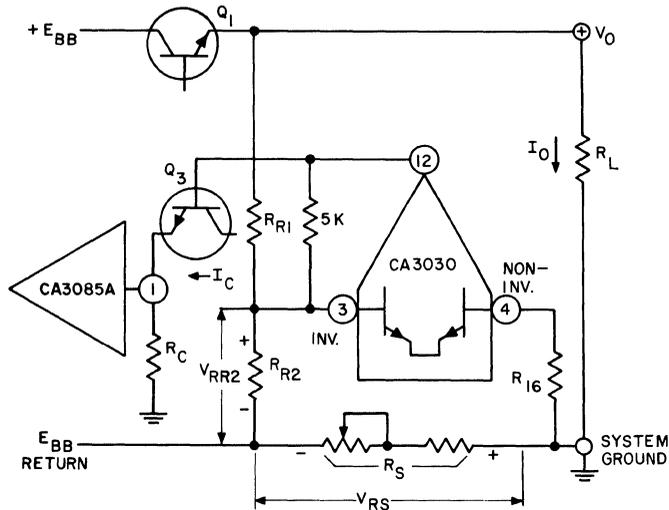
Fig. 103 - Foldback current-limiting circuit.

decreases with V_O, so that $(V_{RS}-V_{RR2})$ remains fixed and Q_3 continues to conduct at the same emitter current. If the load impedance is reduced, Q_3 will be driven even harder, and therefore the output voltage and the load current will decrease even further. Fig. 102 shows the foldback as R_L decreases.

This process is reversible. If the load impedance R_L is increased, I_O and V_O will increase. When I_O reaches the foldback-activation level, Q_3 will cut off again and the power supply will return to regulated operation.

The CA3030 must be operated as a linear voltage amplifier in the foldback circuit, so that the gain is as shown in Fig. 104. If the
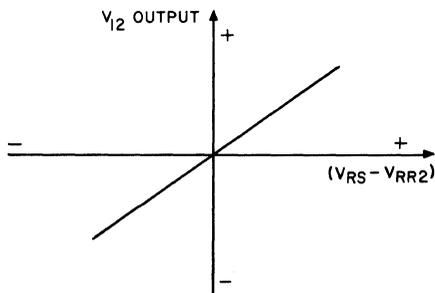
Fig. 104 - Output voltage from the CA3030 operational amplifier as a function of actuating voltage.

CA3030 is misadjusted, a Schmitt trigger action can occur. Such operation may be desirable in latching-type current protection, e.g., in circuits that switch off at overload. Such circuits, however, introduce other prob-

lems such as lack of automatic turn-on, hysteresis effects on varying loads during the shutdown process, and capacitive and non-linear loads.

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*The currents in the 1-kilohm bleeder resistor and the 10-kilohm sensing string are neglected in this discussion.

FOLDBACK-LIMITED SUPPLY

Hybrid-Circuit Regulator

The RCA line of power hybrid circuits includes a series voltage regulator, shown in Fig. 105, designed for use as the regulating element in foldback-current-limited, regulated dc power supplies. The hybrid-circuit regulator includes an RCA-CA3085A integrated-circuit voltage-regulator chip for voltage regulation, stability, and temperature compensation. This integrated circuit supplies a regulated signal to a two-stage high-current booster circuit that consists of a p-n-p driver chip Q_2 and an n-p-n hometaxial-base transistor chip Q_4 (RCA-2N3055 type) used as the series pass transistor. This two-stage output circuit makes possible a load-current capability of 4 amperes without the use of external booster devices. With the use of two external booster transistors, the hybrid circuit can provide regulation at load currents up to 12 amperes. For load currents greater than 12 amperes, the regulator circuit is used as a Darlington driver.

The internal circuitry of the hybrid regulator also includes a foldback-current-limiting circuit, a crowbar trigger circuit, and three
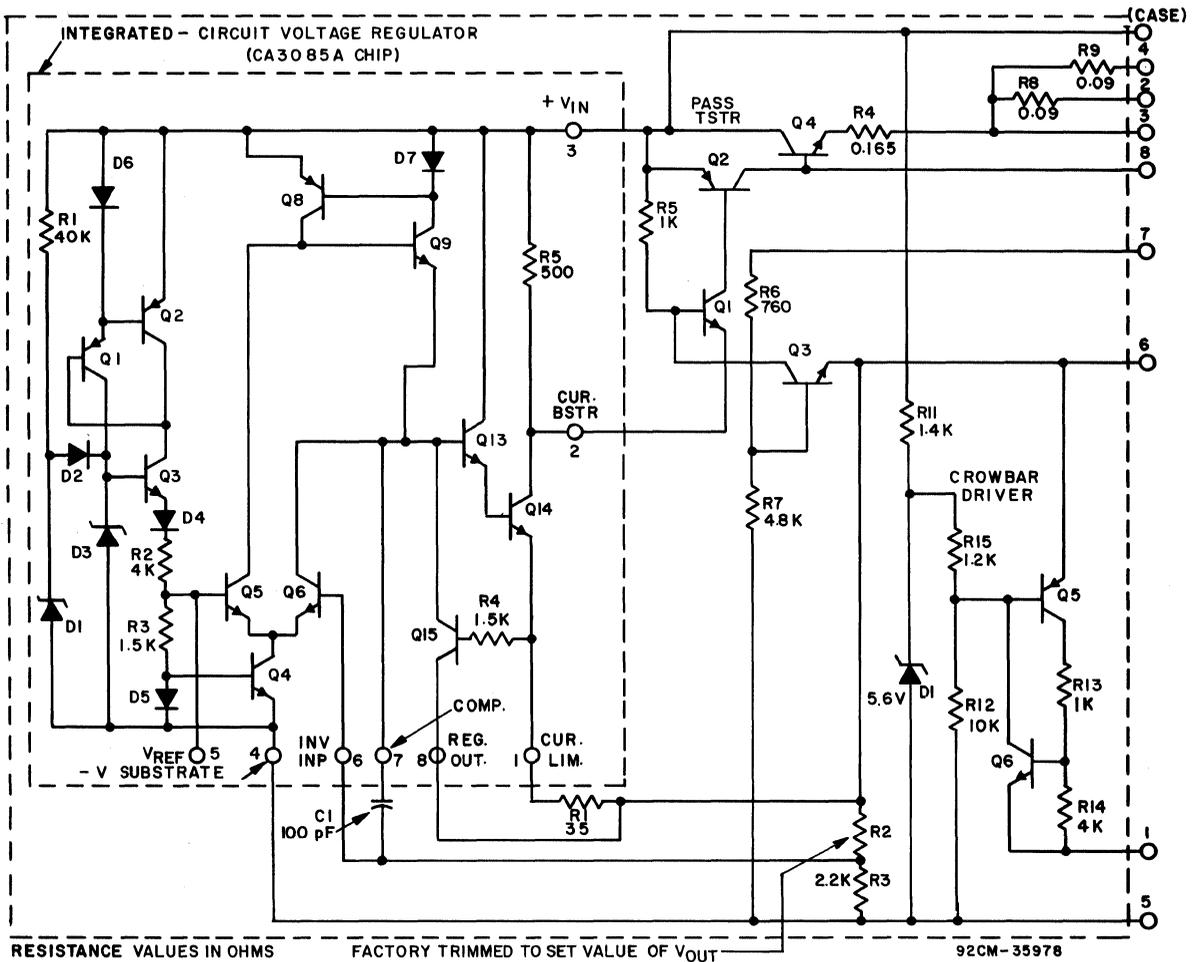
Fig. 105 - RCA high-current hybrid-circuit series voltage regulator.

ballast resistors. The ballast resistors are provided to assure current sharing between the internal pass transistor and two external pass transistors when regulation is required at current levels between 4 and 12 amperes.

Because the CA3085A chip is rated for a maximum supply voltage of 40 volts and a feedback voltage to the inverting input (terminal 6) of 1.8 volts, the output-voltage capability of the hybrid-circuit regulator is limited to a range from 2 to 32 volts. Standard-design regulator circuits that provide a regulated output of 5, 8, or 12 volts are available. For each type, the output voltage is regulated to within ±1 per cent for typical line-voltage, load-current, and temperature variations.

The values of the voltage-divider resistors

R_2 and R_3 establish the level of the output voltage. The junction of these resistors is directly coupled to the inverting input of the CA3085A voltage-regulator chip. The values of the resistors are selected to divide the output voltage so that, for the rated output, the voltage applied to the CA3085A inverting input is approximately 1.6 volts. Any change in output voltage produces a corresponding change at the inverting input of the CA3085A and this circuit then develops an output to cancel the change in output voltage. For example, an increase in load resistance causes the output voltage to rise. The resultant increase in the voltage at the inverting input of the CA3085A is applied to the base of transistor Q_6 on the CA3085A chip, and the collector current of this transistor increases. The base

current of transistor Q_{13} then decreases because it is derived from a constant-current source. This action, in turn, causes the base and collector currents of transistor Q_{14} to decrease so that the drive for the p-n-p driver transistor Q_2 and the n-p-n pass transistor Q_4 is reduced. The load current then decreases to return the output voltage to its original value.

HIGH-OUTPUT-CURRENT VOLTAGE REGULATOR WITH FOLDBACK CURRENT LIMITING

Fig. 106 illustrates the use of the hybrid-circuit series voltage regulator in a foldback-current-limited, regulated dc power supply. This supply provides an output of 5 volts regulated to within ± 1 per cent. The two external 2N3055 hometaxial-base transistors Q_{B1} and Q_{B2} are used as booster pass transistors to increase the load-current capability of the basic regulator circuit to 10 amperes.

The values of the three ballast resistors (R_4, R_8, and R_9) in the hybrid circuit are selected so that (1) the voltage drop across each resistor at the rated current is approximately 450 millivolts and (2) the current through each

external pass transistor is 1.5 times that through the internal pass transistor. These resistors, therefore, force the required current sharing between the internal and external pass transistors.

The foldback-current-limiting circuit consists of transistors Q_1 and Q_3 and resistors R_1, R_5, R_6, and R_7 in the hybrid circuit (shown in Fig. 105). Transistor Q_3 senses the voltages across the branches of the bridge circuit formed by resistors R_6 and R_7 on one side and the base-emitter junction of the series pass transistor Q_4, resistor R_4, and the load resistance on the other side. Because the base-to-emitter voltage of transistor Q_4 increases with the collector current, inclusion of the base-emitter junction of this transistor in the bridge increases circuit sensitivity.

During normal operation, transistor Q_1 is operated in the saturation region, and transistor Q_3 is cut off. When an overload occurs, transistor Q_3 is driven into conduction, and the collector current of this transistor flows through resistor R_5 to decrease the base-to-emitter voltage of transistor Q_1. This effect reduces the base drive to the p-n-p driver

92CM-35979

*SPRAGUE 36 D
CORNELL FAH, OR EQUIV.
T_1=SIGNAL TRANSFORMER CO.
No. 36-6, OR EQUIV.

Fig. 106 - Foldback-current-limited regulated dc power supply that uses an RCA high-current power hybrid circuit as the series voltage regulator.

transistor Q_2 and subsequently the voltage drop across the load resistor. The voltage-feedback condition reaches a stable point on the load-resistance characteristic because the loop gain is less than unity. Transistor Q_1 effectively protects transistors Q_2 and Q_4 and the main pass transistor Q_{14} on the CA3055 integrated-circuit chip (shown in Fig. 105), but it does not protect transistor Q_{13}. Protection of this latter transistor is provided by transistor Q_{15}, which turns on when the current through resistor R_1 reaches 20 milliamperes.

The crowbar trigger circuit in the hybrid circuit provides a trigger input to the external 2N682 crowbar SCR in response to an overvoltage that ranges from 105 to 125 per cent of the rated output value. This overvoltage may result from short-duration transient currents generated by either the load, the supply, or a pass transistor that becomes short-circuited. Resistor R_{11} and zener diode D_1 provide a stable reference voltage that is reduced in value by the voltage divider formed by resistors R_{12} and R_{15}. The voltage at the junction of these resistors is compared to the output voltage by transistor Q_5. When an overvoltage occurs, transistor Q_5 turns on and provides the base drive to turn on the transistor Q_6. This action is regenerative, and the collector currents of transistors Q_5 and Q_6 are limited only by resistor R_{13}, which limits the base current of transistor Q_6. Resistor R_{14} provides a leakage path for the collector-base junction of transistor Q_6. The output of the trigger circuit is connected to the gate of the SCR. The SCR is triggered on by the gate current supplied by this circuit to provide a low-impedance path to shunt excessive currents generated by the overvoltage condition away from the load circuit.

In high-current voltage regulators employing constant-current limiting, it is possible to develop excessive dissipation in the series-pass transistor when a short-circuit develops across the output terminals. This situation can be avoided by the use of the "foldback" current-limiting circuitry as shown in Fig. 107. In this circuit, terminal 8 of the RCA CA3085A senses the output voltage, and terminal 1 is tied to a tap on a voltage-divider network connected between the emitter of the pass-transistor (Q_3) and ground. The current-foldback trip-point is established by the value of resistor R_{SC}.

The protective tripping action is accomplished by forward-biasing Q_{15} in the CA-3085A. Conditions for tripping-circuit operation are defined by the following expressions:

$$V_{BE(Q_{15})} = \text{(voltage at terminal 1)} - \text{(output voltage)}$$

$$= \left[(V_O + I_L R_{SC}) \, \frac{R_1}{R_1 + R_2} \right] - V_O$$

If $\dfrac{R_1}{R_1 + R_2} = K$. then

$$V_{BE(Q_{15})} = (V_O + I_L R_{SC}) K - V_O = K V_O + K I_L R_{SC} - V_O$$

and therefore

$$R_{SC} = \frac{V_O + V_{BE(Q_{15})} - K V_O}{K I_L}$$

Fig. 107 - *High-output-current voltage regulator with "foldback" current limiting.*

Under load short-circuit conditions, terminal 8 is forced to ground potential and current flows from the emitter of Q_{14} in the CA3085A establishing terminal 1 at one V_{BE}-drop [$\cong 0.7$ V] above ground and Q_{15} in a partially conducting state. The current through Q_{14} necessary to establish this one-V_{BE} condition is the sum of currents flowing to ground through R_1 and [$R_2 + R_{SC}$]. Normally R_{SC} is much smaller than R_2 and can be ignored: therefore, the equivalent resistance R_{eq} to ground is the parallel combination of R_1 and

R_2. The Q_{14} current is then given by:

$$IQ_{14} = \frac{V_{BE}(Q_{15})}{R_{eq}} = \frac{V_{BE}(Q_{15})}{\frac{R_1 R_2}{R_1 + R_2}} = \frac{0.7\,[1.3 + 0.46]}{1.3\times 0.46} = 2.06$$
milliamperes

This current provides a voltage between terminals 2 and 3 as follows:

$$V_{2-3} = IQ_{14} \times 250\ \text{ohms} = 2.06 \times 10^{-3} \times 250 = 0.515$$
volt.

The effective resistance between terminals 2 and 3 is 250 ohms because the external 500-ohm resistor R_3 is in parallel with the internal 500-ohm resistor R_5. It should be understood that the V_{2-3} potential of 0.515 volt is insufficient to maintain the external p-n-p transistor Q_2 in conduction, and, therefore, Q_3 has no base drive. Thus the output current is reduced to zero by the protective circuitry. Fig. 108 shows the foldback characteristic typical of the circuit of Fig. 107.

An alternative method of providing "foldback" current-limiting is shown in Fig. 109. The operation of this circuit is similar to that of Fig. 107, except that the foldback-control transistor Q_2 is external to the CA3085A to permit added flexibility in protection-circuit design.

Under low load conditions Q_2 is effectively reverse-biased by a small amount, depending upon the values of R_3 and R_4. As the load current increases the voltage drop across R_{trip} increases, thereby raising the voltage at the base of Q_1 and Q_2 starts to conduct. As Q_2
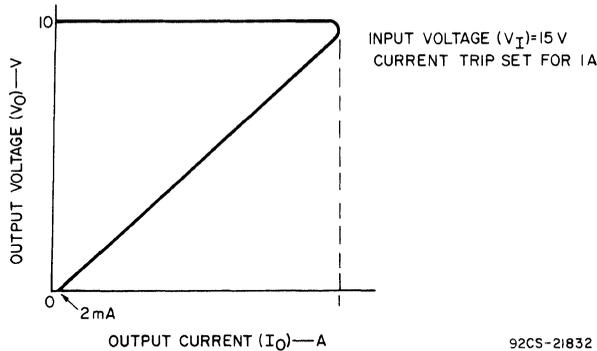
Fig. 108 - Typical "foldback" current-limiting characteristic for circuit of Fig. 107.
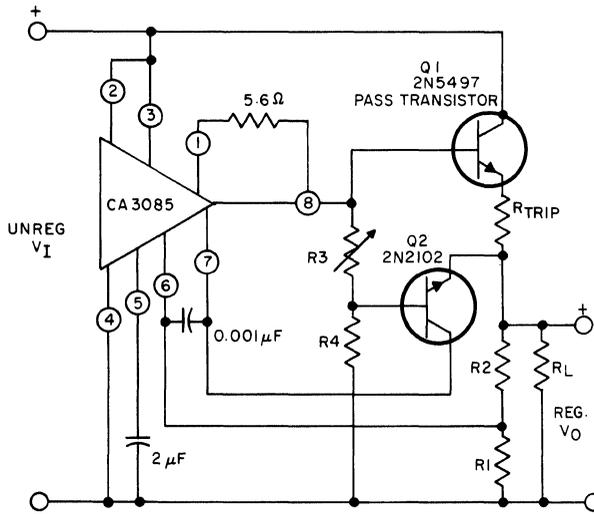
Fig. 109 - High-output-current voltage regulator using auxiliary transistor to provide "foldback" current limiting.

becomes increasingly conductive it diverts base current from transistors Q_{13} and Q_{14} in the CA3085, and thus reduces base drive to the external pass-transistor Q_1 with a consequent reduction in the output voltage. The point at which current-limiting occurs, I_{trip}, is calculated as follows:

$V_{BE(Q_1)}$=voltage at terminal 8 $-V_O$(assuming a low value for R_{trip})

$V_{BE(Q_2)}$=voltage at terminal 8$\left(\dfrac{R_4}{R_3+R_4}\right)$-$V_O$

$$=\left[V_O+I_LR_{trip}+V_{BE(Q_1)}\right]\left[\dfrac{R_4}{R_3+R_4}\right]-V_O$$

if $K=\dfrac{R_4}{R_3+R_4}$, then the trip current is given by:

$$I_{trip}=\dfrac{V_{BE(Q_2)}-K[V_O+V_{BE(Q_1)}]+V_O}{KR_{trip}}$$

In the circuit in Fig. 107 the load current goes to zero when a short circuit occurs. In the circuit of Fig. 109 the load current is significantly reduced but does not go to zero. The value for I_{SC} is computed as follows:

$$V_{BE(Q_2)}+\left[\dfrac{V_{BE(Q_2)}}{R_2}+I_B(Q_2)\right]R_1=V_{BE(Q_1)}+I_{SC}R_{trip}$$

$$I_{SC}=\dfrac{V_{BE(Q_2)}+\left[\dfrac{V_{BE(Q_2)}}{R_2}+I_B(Q_2)\right]R_1-V_{BE(Q_1)}}{R_{trip}}$$

Fig. 110 shows that the transfer characteristic of the load current is essentially linear between the "trip-point" and the "short-circuit" point.

SHUNT REGULATORS

Although shunt regulators are not as efficient as series regulators for most applications, they have the advantage of greater simplicity. The shunt regulator includes a shunt element and a reference-voltage element.
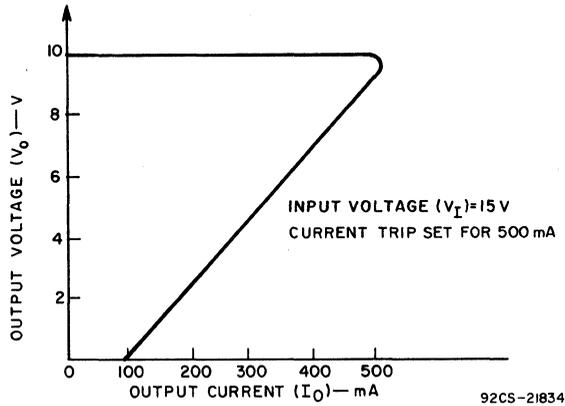
Fig. 110 - *Typical foldback current-limiting characteristic for circuit of Fig. 109.*

The output voltage remains constant because the shunt-element current changes as the load current or input voltage changes. This current change is reflected in a change of voltage across the resistance R_1 in series with the load. A typical shunt regulator is shown in Fig. 111.
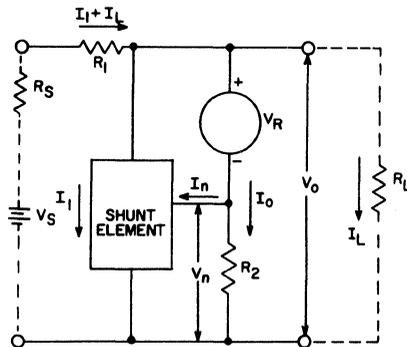
Fig. 111 - *Basic configuration for a typical shunt regulator.*

The shunt element contains one or more transistors connected in the common-emitter configuration in parallel with the load.

For a detailed discussion of the Design and Equations for Shunt Regulators, refer to **RCA Solid State Circuits Handbook**, SP52-Series

Switching Regulator Power Supplies

A switching regulator is used to maintain the output voltage V_O constant during variations in loading. Essentially, the regulator is an inductance-capacitance (LC) filter in series with a switch and a power source. By variation in the length of time the switch is on during each cycle, the amount of energy delivered to the filter can be controlled. The output voltage V_O is a function of this energy.

BASIC REGULATOR OPERATION

As shown in Fig. 112, Q1 is used in the switching mode; therefore, large power levels may be controlled with low loss. Because the output voltage of a switching regulator is not perfectly regulated, this circuit is often used as a preregulator.

Typical operating waveforms for a switching regulator are shown in Fig. 113. The period T is constant; the transistor "on" time t, however, is variable. A differential amplifier compares the output voltage to a reference voltage, and that difference determines the "on" time t. The output voltage V_O is proportional to t for a given load. When Q1 is on, current increases linearly in the L part of the LC filter. When Q1 is off, the energy in L is transferred to C and the load. The commutating diode limits the voltage across Q1 to the supply voltage. When Q1 again turns on, the capacitance of the diode must be discharged. This discharge causes an initial spike in the collector current of Q1.
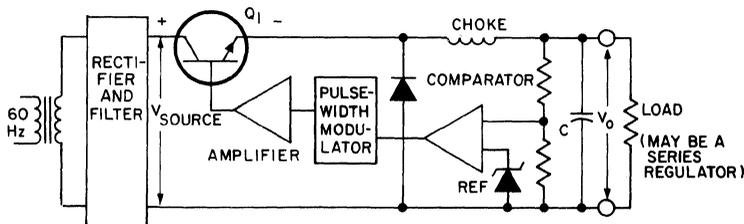
92CS-25584

Fig. 112 - Switching regulator.
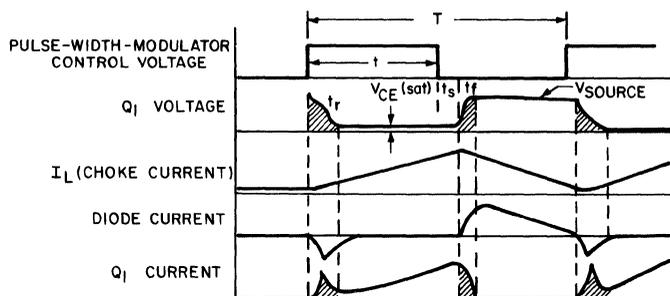
92CS-25585

Fig. 113 - Typical operating waveforms for a switching regulator.

Some important characteristics of the switching-regulator performance are as follows:

1. The maximum operating frequency may be limited by the switching time of the transistor Q1.

2. The collector-to-emitter saturation voltage $V_{CE}(sat)$ and switching-time losses cause device dissipation and power loss. The power dissipation P_t in Q1 is determined as follows:

$$P_t = V_{CE}(sat) \; I_C \; \frac{t}{T}$$

$$+ \; \frac{E_{SW} \; (rise \; and \; fall)}{T}$$

where t is the transistor "on" time. T is the period, I_C is the collector current in amperes, and E_{SW} is the energy absorbed by the output transistor during switching. The collector-to-emitter saturation voltage $V_{CE}(sat)$ and the transistor rise and fall times should be small to ensure low device dissipation.

3. The maximum output voltage is limited by the amount of voltage that Q1 can withstand without breaking down. Because the full source voltage appears across Q1 when it is off and the diode is on, the collector-to-emitter breakdown voltage V_{CEX} should be greater than the source voltage.

DESIGN OF A PRACTICAL SWITCHING—REGULATOR POWER SUPPLY

Power supplies that use switching regulation usually are smaller and lighter and operate more efficiently than conventional supplies. These improvements result from elimination of the need for a 60-Hz power transformer and heat sinks for the transistors.

A complete switching-regulator power supply is described in detail in the sections below (see Fig. 114). A block diagram of this circuit showing voltage waveforms at various points is given in Fig. 115. This supply produces 250 watts at 5 volts with an efficiency of 70 per cent. It uses two switching transistors in a push-pull arrangement with variable pulse width; the switching rate is 20 kHz. The complete supply weighs only 10 pounds and occupies only 470 cubic inches.

Power-Supply Elements

The switching-regulator power supply includes the six major elements shown in the schematic diagram of Fig. 114: (1) the main
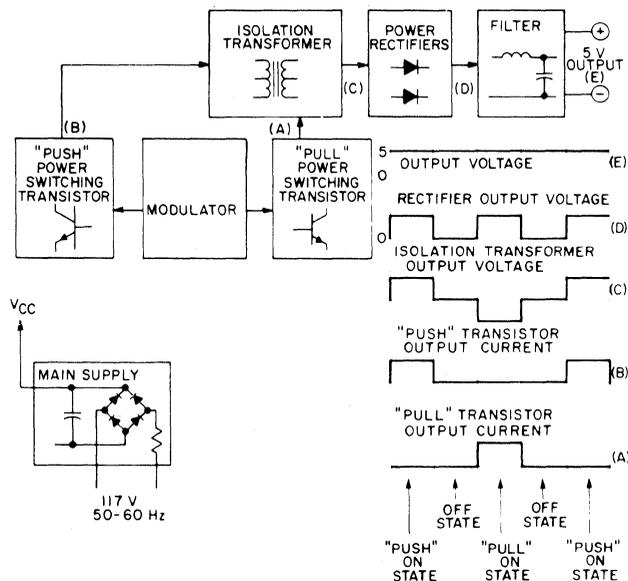
Fig. 115 - Block diagram of switching-regulator power supply, showing voltage waveforms at various points.
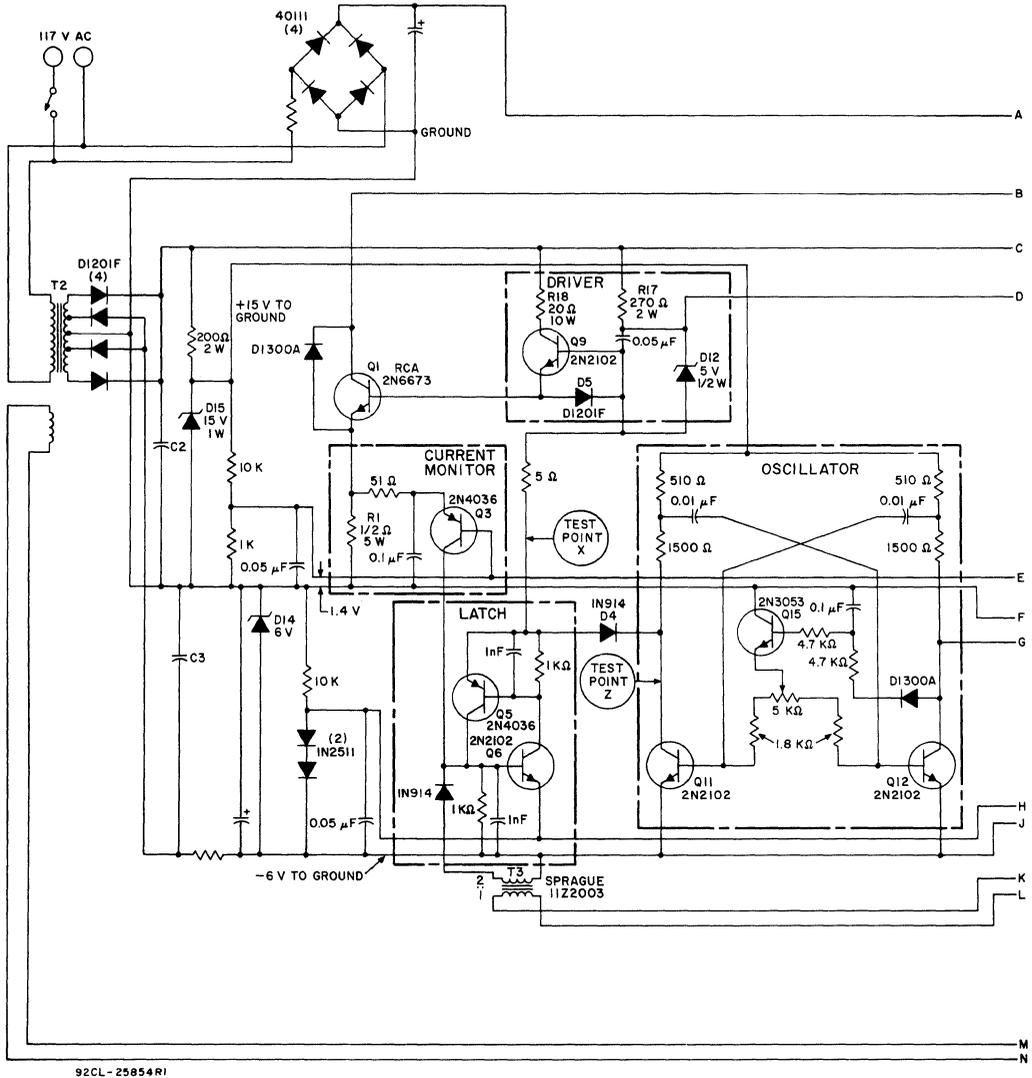
Fig. 114 - Diagram of switching-regulator power supply.

power supply, (2) the power-switching transistors, (3) the isolation transformer, (4) the modulator circuits, (5) the power rectifiers, and (6) the filter. The important parameters of these elements are discussed below.

Main Power Supply

The **main power supply** provides the power that ultimately becomes the output power. It rectifies and filters the line voltage without use of a 60-Hz transformer. For a switching-regulator type of power supply, the main supply may be designed for high ripple without

increased regulator losses (such as would occur in a conventional series regulator). Therefore, smaller capacitors and lower-cost rectifiers can be used. Some resistance must be added in series with the power line to prevent damage to the rectifiers during turn-on. The voltage delivered by the main power supply varies with line-voltage and load variations. The peak output voltage of the main supply at the maximum line conditions (with transients) determines both the collector-voltage rating required for the power-switching transistors and the turns ratio of the isolation transformer.
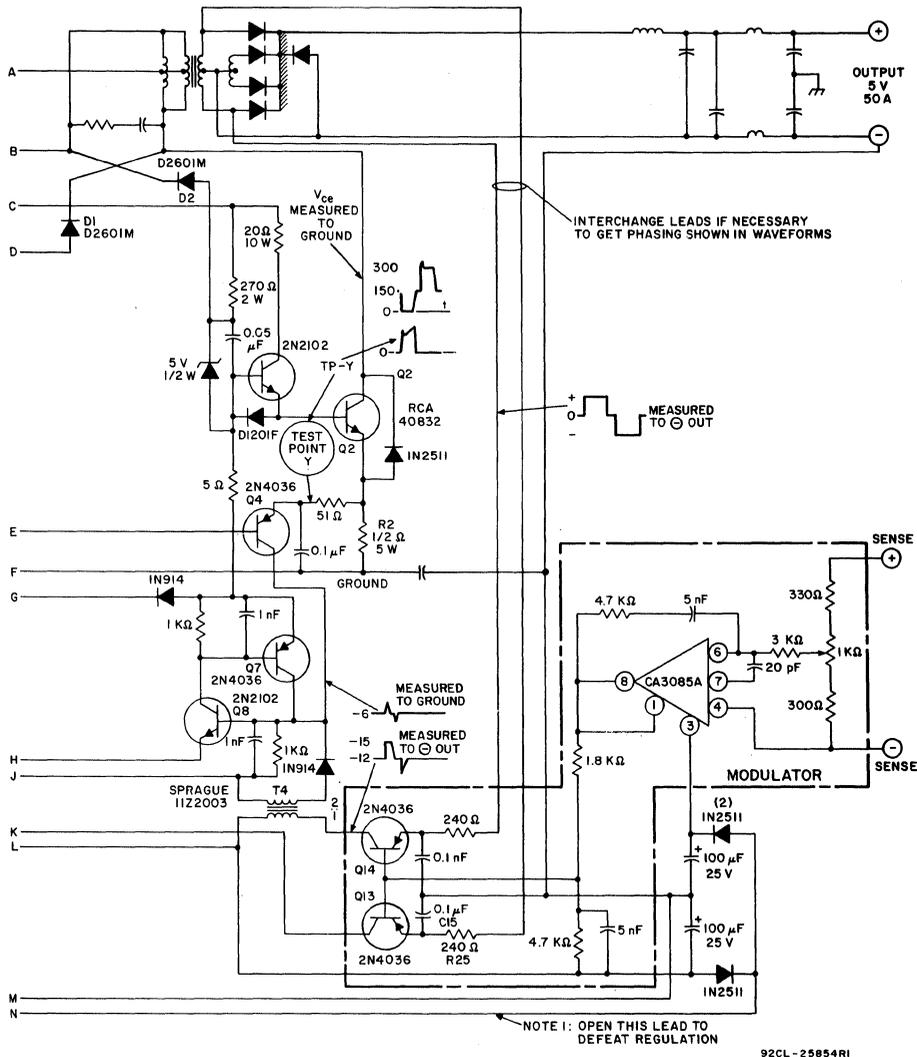
Fig. 114 - Diagram of switching-regulator power supply (cont'd).

Power-Switching Transistors

The performance capabilities of the power supply are determined by **the switching transistors**, because they are the parts least able to withstand overloads such as those caused by load faults or misuse. Therefore, the switching transistors must have the following characteristics (see Table VI for typical examples). Listed in order of importance:

1. High forward-bias second-breakdown capability. The transistor must carry high currents at high voltages shown in the switching load line of Fig. 116.

2. Ability to withstand the required collector voltage specified in Table V while in the cut-off condition. A leakage current specification I_{CEV} establishes this capability.

3. Short rise and fall times (t_r and t_f) for low power dissipation in the transistors and thus high efficiency of the power supply.

4. Reasonably low $V_{CE}(sat)$ for low dissipation and economical transistor heat sinks.
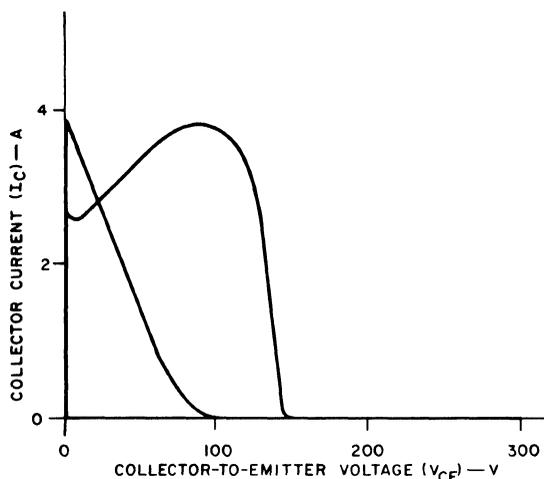
Fig. 116 - Typical load line for a switching transistor in the pulse-width modulated switching-regulator type power supply of Fig. 114.

I_{CER}, forward-bias second-breakdown voltage, and switching times (see Table VI). The forward-current transfer ratio h_{FE} determines the amount of drive current needed. The collector-to-emitter saturation voltage V_{CE}(sat) is important because it determines part of the power loss in the circuit and the dissipation of the transistor during the ON period. The amount of leakage current is important because the transistor essentially conducts this amount of current during the OFF period and thus increases dissipation. If this leakage current is large enough, the transistor can enter into a condition of thermal runaway. Silicon transistors, with their inherently lower leakage-current value, do not often exhibit this problem.

The transistor safe-area rating determines the maximum power that can be handled by the transistor and by the supply. This parameter and its implications are explained in detail in the section on Safe-Area Ratings.

Table V - Relationship Between Line Voltage and the Required Collector Voltage Rating for the Switching Transistors

Rms Line Voltage (V)	Peak Line Voltage (V)	Nominal Collector Voltage (V)	Safe (15% Added) Collector Voltage Rating (V)
90	127.3	254.5	292
95	134.3	268.7	309
100	141.4	282.8	325
105	148.5	296.9	341
110	155.5	311.1	357
115	162.6	325.2	374
120	169.7	339.4	390
125	176.7	353.5	406
130	183.8	367.6	422
135	190.0	381.8	439
140	198.0	395.9	455
145	205.0	410.1	471
150	212.1	424.2	487

(Operating Range — indicated between 341 and 439)
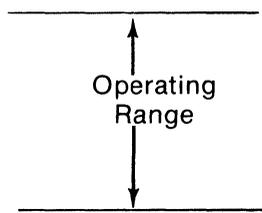
5. Stable leakage current (I_{CEV}). The magnitude of the leakage is not important (even 20 milliamperes at 500 volts contributes less than 5 watts to the average dissipation per transistor), but it should be stable.

Transistor Parameters

The transistor parameters affecting the performance of a switching regulator are the current gain h_{FE}, the collector-to-emitter saturation voltage V_{CE}(sat), the leakage current

The switching times, t_r (rise time) and t_f (fall time), are of prime consideration in selection of a transistor to be used as the switch. For good regulation over a wide range of input voltage and output current, the duty cycle must be variable from at least 10 to 90 per cent (i.e., the pulse width could be a minimum of one-tenth of the period $1/10f$). For low switching losses, the rise and fall times should each be less than 10 per cent of the minimum pulse width.

Table VI - Recommended Specifications for Switching Transistors

Parameter	Measurement Conditions		Value
	General	For Transistors Used in Design Example	
I_{CEV}	V_{CE} from Table V $V_{BE} \leq V_{EE}$[1]	$V_{CE} = 450$ V $V_{BE} = 1.5$ V	5 mA max.
I_{EBO}	$V_{EB} = V_{EE}$[1]	$V_{EB} = 6$ V	5 mA max.
$I_{S/b}$	$I_C = I_C$(max.)	$I_C = 4$ A	(must pass test)
	$V_{CE} = V_{CC}$ (max.) $t \geq 50\ \mu s$	$V_{CE} = 200$ V $t = 100\ \mu s$	
V_{CE}(sat)	$I_C = I_C$(max.) I_B as provided by driver circuit	$I_C = 4$ A $I_B = 0.8$ A	< 3 V
V_{BE}(sat)	"	"	< 2 V[2]
t_r	$I_C = I_C$(max.) I_{B1} and I_{B2} as provided by driver circuits	conditions[3]	$< 1\ \mu s$
t_f	"	"	$< 1\ \mu s$

[1]V_{EE} is negative voltage source applied to the base.

[2]Importance depends upon drive-circuit design. For the design shown, V_{BE}(sat) is not critical.

[3]Because of the great variations in parameters and waveforms, some standard test condition is used for control. The manufacturers standard conditions are usually adequate control.

Switching Arrangement

The transistor switching arrangement usually takes on one of two forms as illustrated in Fig. 117. If isolated supplies appear in the drive circuits of Q1 and Q2, performance of the two circuits is basically the same. However, if no isolated supplies are used, then the circuit of Fig. 117(b) has the disadvantage that the V_{CE} of Q2 cannot be reduced below the V_{BE} of Q2. This condition results because the base of Q2 cannot be tied to a point more positive than the plus voltage of the power supply.

The circuit of Fig. 117(a) can avoid this problem if the collector of the driver unit is connected to the positive side of the supply. The disadvantage is that current in the driver does not flow through the load; the power associated with this current, therefore, is lost.

The circuit of Fig. 117(b) is usually preferred when the power that results from a high V_{CE}(sat) can be tolerated.
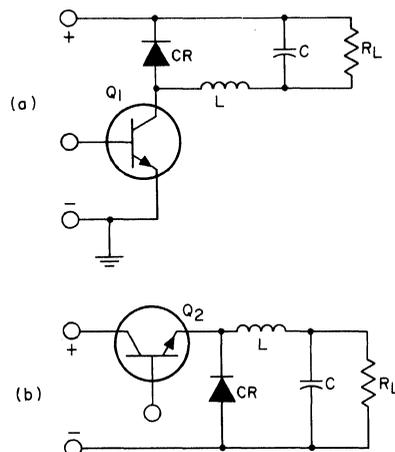
Fig. 117 - Basic transistor switching arrangements: (a) filter elements and load impedance in collector circuit of switching transistor; (b) filter elements and load impedance in emitter circuit of switching transistor.
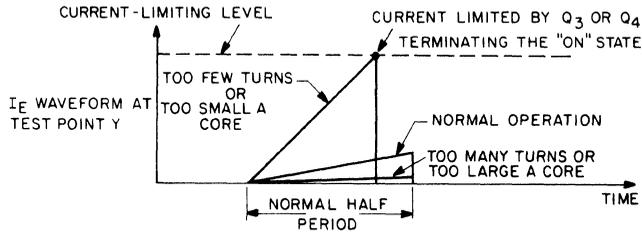
Fig. 118 - Waveform of emitter current in power-switching transistor showing effects of core size and number of primary turns, with regulation defeated (see note on Fig. 114).

Fig. 118 shows the emitter-current waveform of a power-switching transistor, monitored at point Y of Fig. 114 for different numbers of primary turns. If the emitter current is excessive, the circuit reduces the duty cycle to protect the power-switching transistor. Fig. 119 shows the waveforms for unbalanced dc drive. These unbalanced currents result from unequal duty cycles, caused by oscillator unbalance or by unbalance or faults in the modulator. Because such unbalances occur in normal operation, the protective circuits must be included in the design.

must have a short rise time to provide fast transistor turn-on and low dissipation. The reverse drive must have short rise time and a magnitude equal to or greater than the forward base drive.

The oscillator frequency should be stable to minimize rectifier losses, and should be greater than 20 kHz to eliminate sound. All of the circuits should be insensitive to component-value variations, component drift, and random or stray interference. The circuits also sense excessive emitter current in the power-switching transistors, and compensate by adjustment of
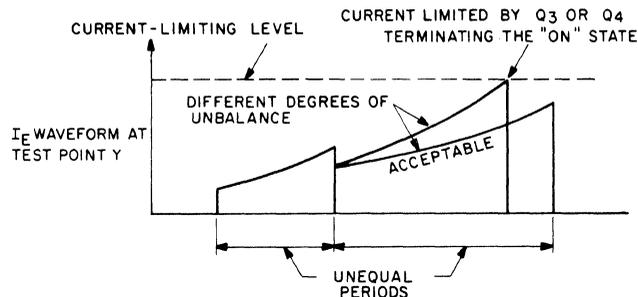
Fig. 119 - Waveform of emitter current in power-switching transistor showing effect of unbalanced direct current, with regulation defeated and load current of 25 amperes.

Modulator Circuits

The **modulator circuit (oscillator, drivers, modulators, and latches)**, which is indicated in the circuit diagram, delivers the base drive to the power-switching transistors. The forward drive must be sufficient to keep the transistors saturated under all conditions, and

the duty cycle, as noted above.

These circuits eliminate common-mode conduction in the power-switching transistors. This conduction occurs in a driven inverter when the transistor that has been "off" is turned "on"; the other transistor continues to conduct because of its storage time. For

several microseconds both transistors conduct, and the current is not limited by the collector circuit. The transistor that has just been switched on has high current and voltage simultaneously, and therefore high dissipation perhaps 50 per cent of the rated power-supply output). This power dissipation is wasteful and may even damage the transistor.

Power Rectifiers

Most of the losses in the power supply occur in the power rectifiers. For example, in a 5-volt, 50-ampere supply utilizing four 1N3909 rectifier diodes, each of the diodes carries a nominal peak current of 25 amperes at 50-percent duty cycle. The forward power loss in the rectifier can be calculated from the current and voltage values. The voltage drop is not specified for 25-ampere operation, but the rectifier has a maximum voltage drop of 1.4 volts at a current of 30 amperes. Because this 30-ampere data is close to 25-ampere operation (and unbalance could cause the current to exceed 25 amperes), the maximum forward-drop rectifier losses can be estimated from the 30-ampere specifications: ½ x 1.4 V x 30 A x 4= 84 watts at maximum rated output.

Reverse recovery losses in the diodes add to the total dissipation; these losses, which are significant at 20 kHz, depend on the rectifiers used, the leakage inductances in the wiring and the isolation transformer, the transistor switching times, and the operating frequency. Because of the many variables (and unknowns) involved, the rectifier losses should be determined by measurement of circuit efficiency or heat-sink temperature. A total rectifier loss of 45 per cent of the rated output power of the regulator is to be expected.

Isolation Transformer

The isolation transformer is a ferrite-core transformer that operates at 20 kHz. Its design formulas are the same as those for conventional 60-Hz transformers, but the results are significantly different. The number of turns is never greater than 200, and may be as low as one. These turns always fit in the large "windows" in the ferrite core. Leakage inductance is reduced in the primary turns by sectioning the primary winding. Leakage in the secondary is less important because the secondary is loaded by a filter choke. The copper losses can easily be made negligible, and the copper wire costs are small. The size of the transformer core is determined by the need

to dissipate the heat generated in the core material; the Indiana General Co.* recommends that dissipation be kept below 0.25 W/in. The 20-kHz ferrite core is much smaller than a 60-Hz core (3 in.^{3} vs. 140 in.^{3}), and is much lighter (1 lb. vs. 33 lbs.).

The design of a 20-kHz power transformer involves three basic problems: core material selection, windings to keep peak flux below saturation, and compensation for unbalanced direct currents.

If a core has too much loss, it will overheat. If it has too many turns, the flux density will be below saturation, but the copper losses will be greater than necessary. The number of turns is kept low to avoid unnecessary copper losses, but must be great enough to keep the peak flux in the core below saturation.

The core will saturate if its cross section is too small, if there are not enough turns in the primary winding, or if the primary direct current is unbalanced. Core saturation causes the power-switching transistors to draw excessive currents.

Filter Considerations

A fundamental part of every switching regulator is the filter. Fig. 120 shows the various types of filters that can be used. Selection of the optimum filter for a power supply is based on the load requirements of the particular circuit and consideration of the basic disadvantages of the various types of filters.
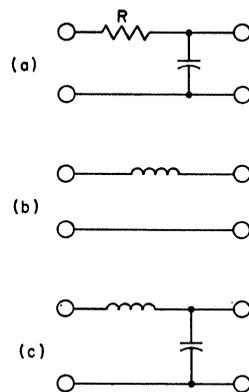
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Fig. 120 - Typical filter circuits for use between pass element and load in a switching regulator: (a) capacitive filter; (b) inductive filter; (c) inductive-capacitive filter.

A capacitive filter, shown in Fig. 120(a), has two primary disadvantages: (1) because large peak currents exist, R must be made large enough to limit peak transistor current to a safe value; and (2) the resistance in this circuit introduces loss.

*Indiana General Ferramic Components,
 Indiana General Corp. Keasbey, N.J.

An inductive filter, shown in Fig. 120(b), has three disadvantages: (1) The inductance may produce a destructive voltage spike when the transistor turns off. This problem, however, can be solved effectively by the addition of a commutating diode, as shown in Fig. 121.
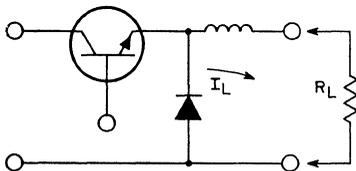
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Fig. 121 - Use of inductance and commutating diode as filter network between pass transistor and load in switching voltage regulator.

This diode commutates the current flowing through the inductor I_L when the transistor switches off. (2) An abrupt change in the load resistance R_L produces an abrupt change in output voltage because the current through the load I_L cannot change instantaneously. (3) A third disadvantage of the inductive filter becomes evident during light loads. The energy stored in an inductor is given by

$$E = \tfrac{1}{2}LI^2$$

As a result, the capability of the inductor to store energy varies with the square of the load current. Under light load conditions, the inductor must be much larger to provide a relatively constant current flow when the transistor is off than is required for a heavy load.

Most of the problems associated with either a capacitive filter or an inductive filter can be solved by use of a combination of the two as shown in Fig. 120(c). Because the energy stored in an inductor varies directly as current squared, whereas the energy output at constant voltage varies directly with current, it is not usually practical to design the inductor for continuous current at low current outputs.

The addition of a capacitor eliminates the need for a continuous flow of current through the inductor. With the addition of a commutating diode, this filter has the following advantages: (1) no "lossy" elements are required (2) The inductive element need not be oversized for light loads because the capacitance maintains the proper output voltage V_{out} if the inductive current becomes discontinuous. (3) High peak currents through the transistor are eliminated by the use of the inductive element.

In summary, the switching-regulator filter can take on various forms depending upon the load requirements. However, if a wide range of voltage and current is required, an LC filter is used in combination with a commutating diode.

A practical rule of thumb is to design the inductor to be large enough to dominate the performance during maximum-load conditions. The filter capacitor is chosen to be large enough to dominate performance at mid-range current values and the full range of output voltages.

A primary advantage of the transistor switching regulator is that the switching frequency can be made considerably higher than the line frequency. As a result, the filter can be made relatively small and light in weight.

The means by which the switching regulator removes the line-frequency ripple component is illustrated in Fig. 122. The on time increases under the valley points of the unregulated supply and decreases under the peaks. The net result is to remove the 60-Hz component of ripple and introduce only ripple at the switching frequency which is relatively high frequency and easily filtered out.

The inductor carries a current equal to the dc output. It can have small size and low
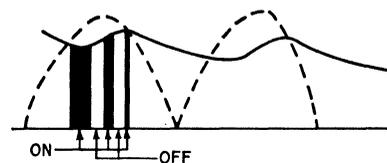
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Fig. 122 - Effect of high-frequency switching of the switching regulator on power-supply ripple component.

resistance because it has a low inductance (3 to 8 microhenries). The inductance value used is a compromise between the need for a high value to limit peak currents and thus permit good transistor utilization, and the need for a low value to permit fast response to sudden current demands. The minimum value of inductance is determined by the peak collector current allowed, as follows:

$$L_{min} = \frac{t_{off}(max)\ E_{out}}{n_T I_c(peak) - I_{load}}$$

where n_T is the turns ratio of the isolation transformer.

The filter capacitors for this application must be selected for 20-kHz operation. Ceramic and paper types are recommended, but tantalum or high-quality aluminum electrolytics can be used for large values of capacitance. The capacitance must be sufficient to prevent the output voltage from decreasing excessively when the load is suddenly increased and the inductor supplies less than the load current. The minimum capacitance is given by

$$C_{min} = \frac{I_{load}[t_{dis}+2t_{off}(max)]}{2(\Delta V)\ allowed}$$

where

$$t_{dis} = \frac{L\ I_{load}}{\dfrac{V_{CC}(min)}{n_T} - V_o - 1.0}$$

and $t_{off}(max)$ is 12.5 microseconds for this design.

Fig. 123 shows how the inductor controls the ratio of peak collector current to average
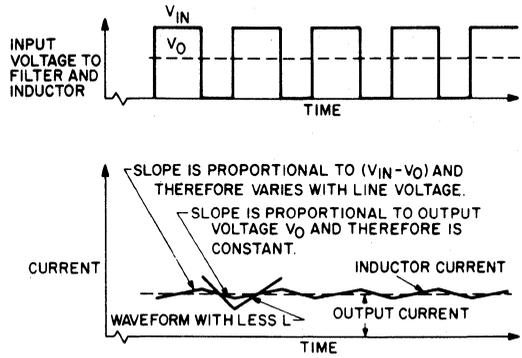
Fig. 123 - Waveforms for filter inductor under steady-state operation at 60-per-cent duty cycle.

collector current in the power-switching transistors under steady-state operation. Smaller inductors cause higher peak currents, which require larger transistors and result in poor utilization of the transistor capabilities. The minimum value of inductance is determined by the peak collector current allowed, as follows:

$$L_{min}= \frac{t_{off}(max)\ E_{out}}{n_T\ I_c(peak) - I_{load}}$$

where n_T is the turns ratio of the isolation transformer. However, as shown in Fig. 124, the inductor also establishes the maximum rate of rise of current to the capacitor, and thus determines the ability of the power supply to respond to sudden demands for load current. For quick response, a low value of inductance is desirable.

Power-Supply Performance

The power supply shown in Fig. 114 can deliver a load curent of 50 amperes at 5 volts.
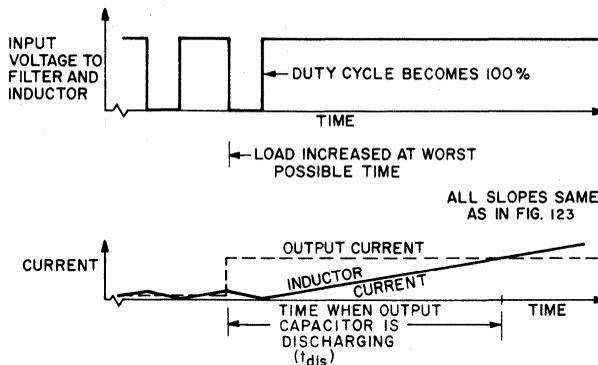
Fig. 124 - Waveforms for filter inductor under sudden increase of load current.

All of the pulse-width modulation circuits, drivers, and latches are duplicated for each power-switching transistor. This duplication uses more than the minimum number of components, but it provides wide design margins and reliable operation.

Voltage regulation and overload regulation are accomplished by reducing the duty cycle of the power-switching transistors. The duty cycle is reduced by triggering the latches on, either from pulse transformers T_3 and T_4 to regulate the output voltage, or from transistors Q_3 and Q_4 to prevent excessive emitter currents in the power-switching transistors. The excessive currents could be caused by overloads at the output or by transformer core saturation resulting from unbalanced duty cycles.

Input-to-output isolation is maintained through the main isolation transformer (T_1), the 60-Hz transformer (T_2), and the pulse transformers (T_3 and T_4). This circuit isolation is indicated in Fig. 114.

This power supply is capable of operating into any load impedance, including short circuits, without damage. It can operate at duty cycles from less than 10 per cent to 100 per cent. With a duty cycle of 100 per cent, the supply operates as a straight inverter at the full capacity of the transistors, transformers, and rectifiers.

The base drive for the power-switching transistors is direct-coupled, and is supplied by an unregulated low-voltage power supply that operates from a 60-Hz transformer. Direct coupling of the base drive provides positive control over transistor bias. The reverse base drive is supplied by the two-transistor latch circuits Q_5 and Q_6 or Q_7 and Q_8, or by the oscillator transistors (Q_{11} and Q_{12}) if the duty cycle is 100 per cent. The reverse base voltage is obtained from a 6-volt regulated supply.

The frequency is controlled by the astable transistor oscillator that operates from 15-volt and –6-volt regulated sources. A potentiometer for equalization of the duty cycle is shown, but is not normally required. Transistor Q_{15} insures that the oscillator does not "hang up."

Common-mode conduction is reduced by cross-coupled diodes D_1 and D_2. These diodes conduct when the V_{CE} of the power-switching transistor is less than 5 volts (breakdown of the zener diode), and prevent conduction of the opposite power-switching transistor. These diodes are of critical importance because the storage time of the power-switching transistors is several microseconds at light load conditions ($I_{B_1} > 0.5$ amperes and $I_C < 0.5$ amperes).

A major consideration in the design of this power supply is the protection of the switching transistors and the load circuit from damage caused by transients or faults in the modulator. The faults most likely to occur are lock-up in the oscillator, transient turn-on of the latching transistors caused by dv/dt at point X in Fig. 114, and magnetic pickup in the pulse transformers. The circuit is designed so that any of these faults will cause the power-switching transistors to turn off; this design protects the transistors and keeps the output voltage low. The over-current protection circuit is made independent of the proper functioning of the output regulator or its associated circuits, and is dc-coupled to minimize the possibility of failure. Finally, if the low-voltage supplies fail, the output voltage merely falls to zero without any harmful surges.

STEP-DOWN SWITCHING REGULATOR

A transistor switching regulator can be used as a dc step-down transformer. This circuit is a very efficient means of obtaining a low dc voltage directly from a high-voltage ac line without the need for a step-down transformer. Fig. 125 shows a typical step-down transistor switching regulator. This regulator utilizes the dc voltage obtained from a rectified 117-volt line to provide a constant 60-volt supply. Fig. 126 shows the performance characteristics for this circuit.

20-KHZ SWITCHING-REGULATOR CIRCUIT

The following paragraphs describe a 20-kHz switching-regulator circuit that operates from a 28-volt supply and has a regulated output between 4 and 16 volts dc. The circuit features overload protection which limits the current to about 11 amperes.

The control element of the switching regulator is a 2N6650, a p-n-p Darlington power transistor used as a switch and driven directly from a CA3085A integrated-circuit positive voltage regulator shown in Fig. 127. The regulator does not operate at a fixed clock frequency, but is free running.

The regulator circuit is basically a step-down switching regulator. When the pass unit, Q3 (2N6650) is switched on, current is charged into L1; when Q3 switches off, the

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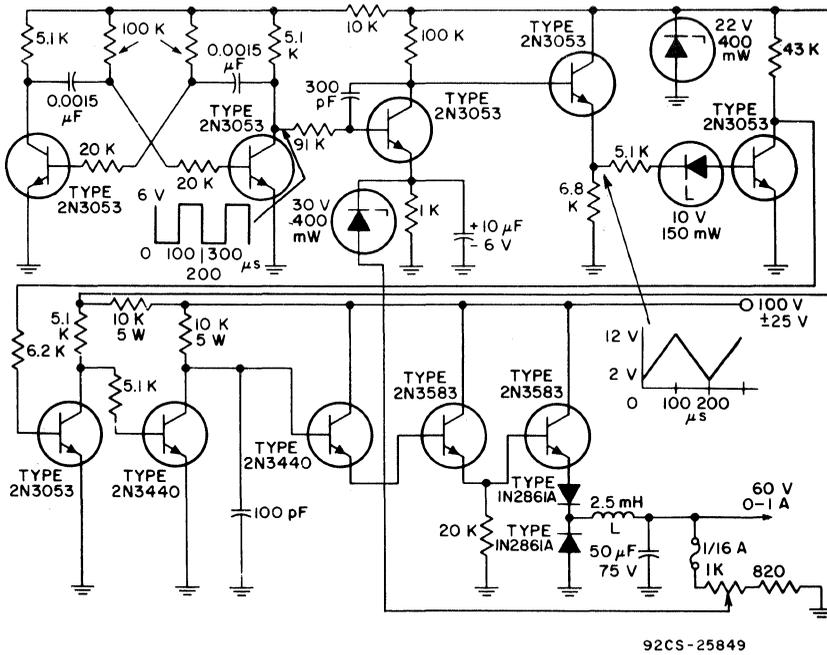
Fig. 125 - Typical step-down transistor switching regulator.
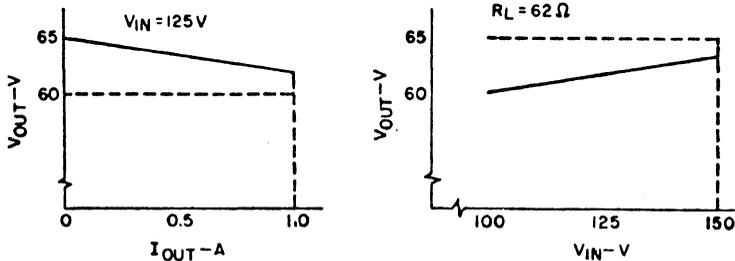
Fig. 126 - Performance characteristics of step-down switching regulator shown in Fig. 125.

current through L1 continues to flow by way of the commutating diode, D1.

The dc output voltage is determined by the ratio of R10 to R11, just as in a linear series regulator. Switching action is accomplished by comparing a ripple voltage to a hysteresis voltage. The circuit switches on and off, triggered by the ripple of the output voltage. The voltage at pin 6 of the CA3085A (Fig. 128) is determined by R10 and R11 of Fig. 127, and is proportional to the output voltage plus the ripple voltage at point A, V_A, fed in by capacitor C5. This voltage is compared with the voltage at pin 5. The voltage at pin 5 consists of the built-in reference voltage of the

CA3085A plus a variable component proportional to the voltage at point, B, V_B, fed through R8.

The impedance of C5 at the operating frequency (10-kHz minimum) must be low compared to the input impedance at pin 6. As shown in Fig. 129, the Darlington, Q3, is switched on when the output voltage becomes too low, i.e., when the voltage at pin 6 becomes less than the voltage at pin 5; when this condition is reversed Q3 is switched off.

Diodes D2 and D3 are added for the protection of the very sensitive input at pin 6. Resistors R7 and R12 and capacitor C3 control the drive current and improve the
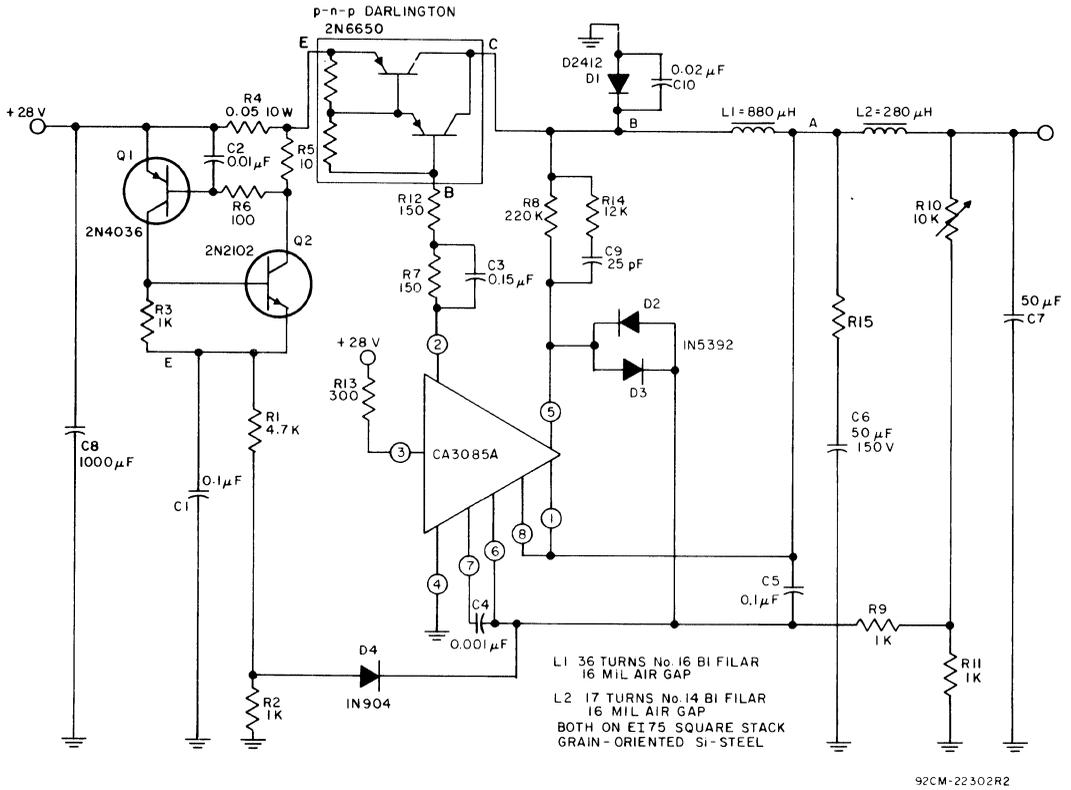
Fig. 127 - The switching-regulator circuit.
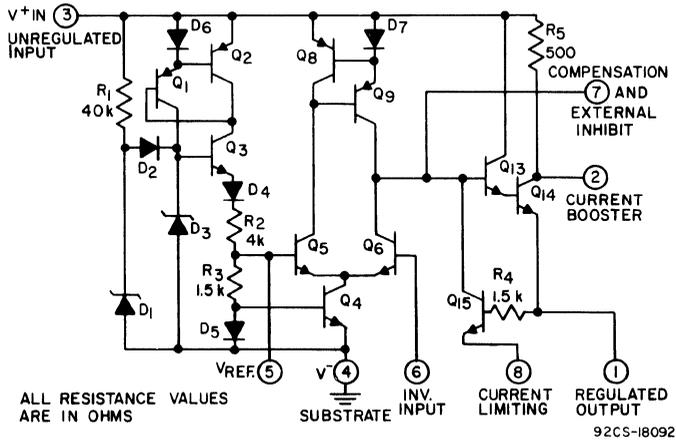
Fig. 128 - The CA3085A.

switching performance of the Darlington, Q3.

L2 and C7 provide additional filtering and isolate point A from the load. Isolation is necessary from loads, capacitive loads, for example, which could drastically affect the ripple voltage at point A. Therefore, at the frequencies involved, L2 must have an impedance which is high compared to R15. L2, together with C7, serves also as a filter to reduce the output ripple.
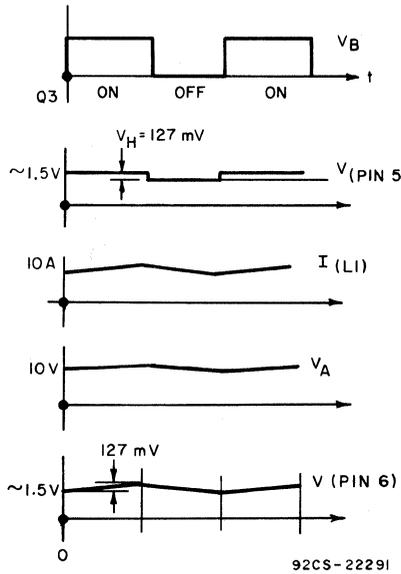
Fig. 129 - *Waveforms for normal operation of the Darlington, Q3.*

C10 is a small capacitor placed in parallel with D1 to buffer the surge voltage at point B when Q3 is switched on. C10 reduced the high-frequency ringing (approximate 3 MHz) at point A caused by L1 and its distributed winding capacitance. The combination of C9 and R14 speeds the switching of the CA3085A without changing the hysteresis voltage, V_H.

Transistors Q1 and Q2 and their associated circuitry provide overload protection. Normally, Q1 and Q2 are off, C1 is discharged, and the voltage at point E, V_E, is zero. In case of overload, the current through R4 produces a voltage sufficient to turn Q1 on. As a result, Q2 turns on, and C1 charges mainly through Q2 and R5. A voltage proportional to that at point E is fed through diode D4 into pin 6 of the CA3085A; this results in Q3 being turned off, even while C1 is still charging. The voltage drop across R5 caused by this charging current holds Q1 on, however, until C1 is fully charged. When C1 becomes fully charged, Q1 and Q2 are turned off, and C1 discharges slowly through R1 and R2. When V_E becomes low enough, Q3 is switched on again. Since the basic frequency-determining mechanism of the switching regulator is not disturbed (an overload or short circuit is separated or insulated from the inner circuit by the impedance of L2), a few cycles of normal operation occur until the current through R4

has built up again. Fig. 130 shows the voltage at point E, V_E, the current through inductance L1, I_{L1}, and the voltage at point B, V_B, under overload conditions.
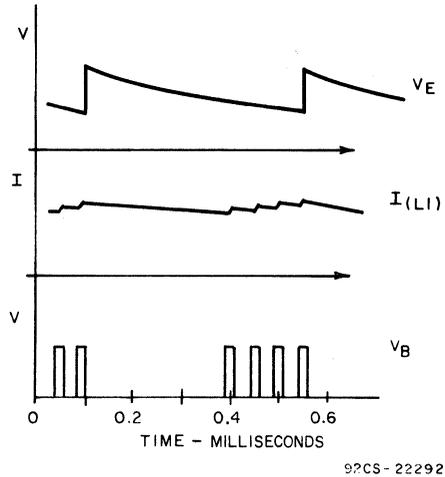
Fig. 130 - *Circuit waveforms under over-load conditions.*

Performance

The regulator was designed mainly for use in equipment requiring supply-voltages of 5 and 12 volts (computers, battery chargers, etc.). With the values of R10 and R11 shown, the voltage can be regulated between 4 and 16 volts. With other values of R10 and R11, the output voltage can be varied over a wider range, approximately 2 to 22 volts. The output voltage varies less than 0.11 volt between 10 per cent and full load. After one hour of operation, it dropped 30 millivolts.

The efficiency varies with output voltage as shown in Fig. 131. At 5-volts output efficiency is 66 to 72 per cent and at 12 volts output, 76 to 83 per cent between 20 per cent and full load.

As shown in Fig. 132, the operating frequency varies from 12 to 28 kHz for outputs between 5 and 12 volts; at outputs above 30 watts the frequency is above the audible range.

The circuit is relatively insensitive to input voltage ripple. For an input voltage ripple of 4 volts (60-Hz bridge rectified), the output ripple is 0.1-volt peak-to-peak (60 millivolts, 120 Hz, plus 40 millivolts, at approximately 20 kHz). As shown in Fig. 133, the efficiency is not affected by variations of the input voltage. The frequency changes considerably and peaks
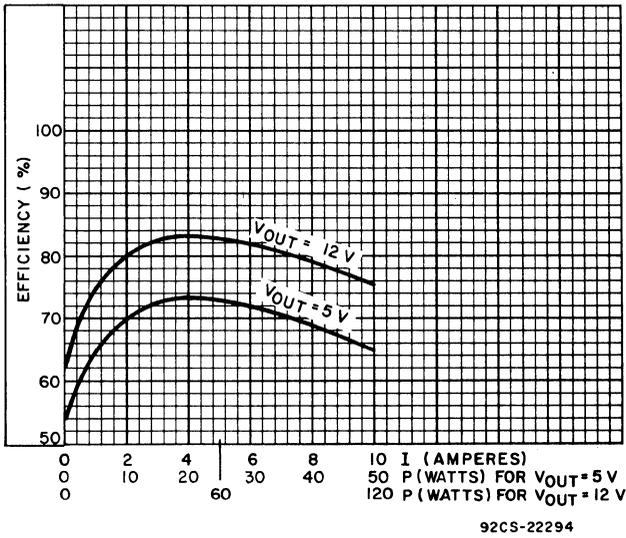
Fig. 131 - Efficiency as a function of output.

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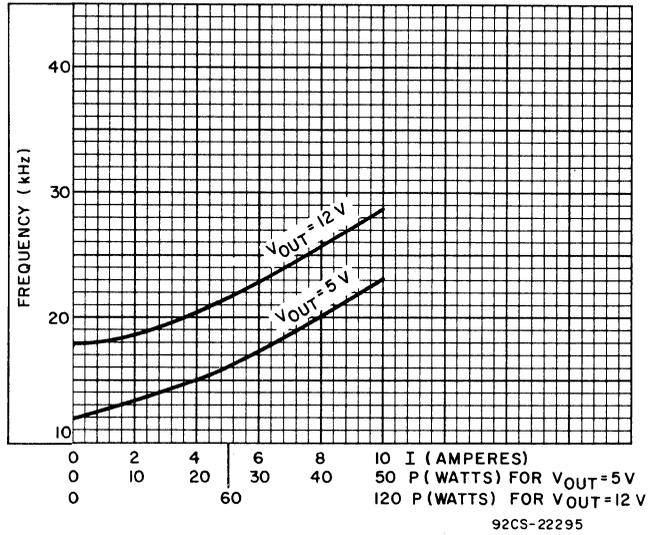
Fig. 132 - Operating frequency as a function of output.

92CS-22295
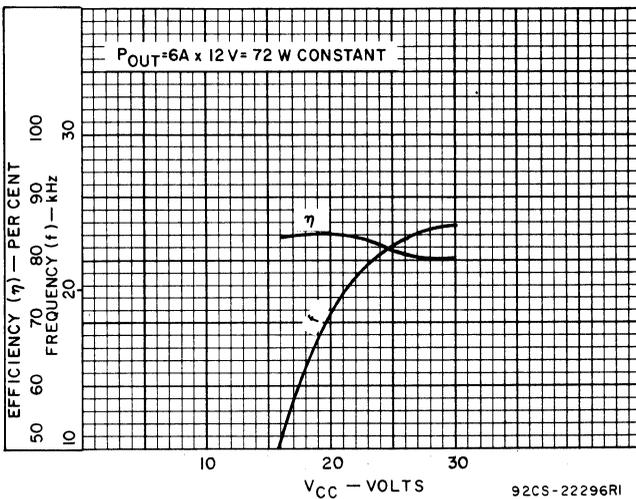
Fig. 133 - Efficiency and operating frequency as a function of input voltage.

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when V_{CC} is approximately $2V_{out}$.

At 25°C ambient, the operating temperature of Q3 and D1 was 78°C at maximum load; Q3 and D1 were mounted on a common heat sink rated at 2.3°C/W. Under short-circuit operation, the diode, D1, reached 88°C, while Q3 ran cooler, 58°C. As mentioned earlier, under short-circuit or overload conditions, the circuit is self-protecting.

Fig. 134 shows efficiency and frequency versus output voltage; Fig. 135 shows the regulation characteristic for a V_{out} of 12 volts.

The free-running switching regulator described in the previous paragraphs provides a simple circuit which combines good regulation with high efficiency and relatively low output ripple. The equations for designing the regulator are straightforward, and the design procedure, although approximate, works exceedingly well.
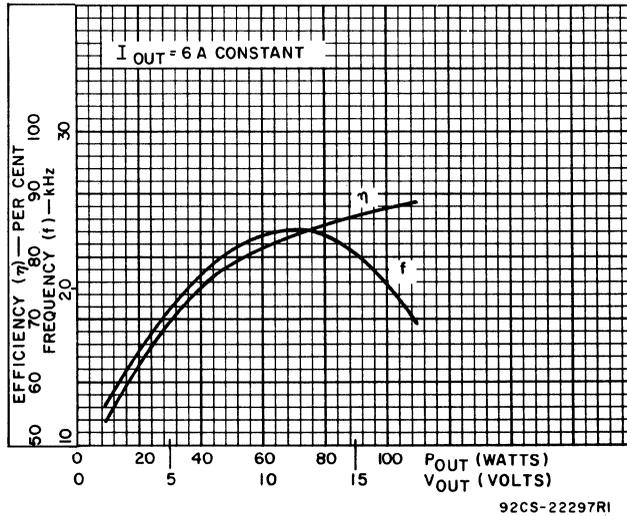
Fig. 134 - Efficiency and operating frequency as a function of output voltage.
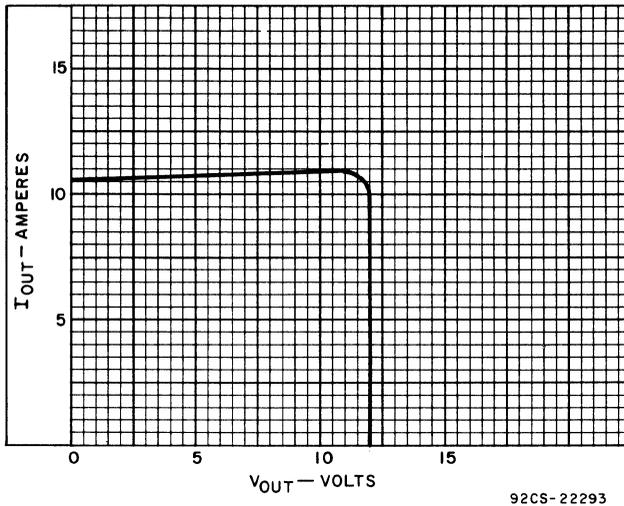
Fig. 135 - Regulation characteristic for an output voltage of 12 volts.

Table VII - Comparison of Power Supplies

	Conventional Series-Regulated Supply	Pulse-Width Modulated Regulator	Units
Output Current at 5 volts	25	50	A
Power Losses (Max.)	300	100	W
Size	1600	470	in.^{3}
Weight	50	10	lb.
Recovery Time	50	500	μs
Regulation (Half load to full load)	> 0.25	0.5	%
Line Regulation	> 0.25	0.5	%

PULSE-WIDTH MODULATED (SWITCHING-REGULATOR) SUPPLIES

In a switching-regulator type of power supply, the output voltage is regulated by a technique referred to as "pulse-width modulation", in which pulses of variable duty cycle are averaged with an inductor-capacitor filter. Regulation is accomplished by the variation of the duty cycle. The pulses constitute a two-state signal (power on and power off) that is supplied to the filter. However, to permit use of a smaller isolation transformer, the "power-on" state is operated in a push-pull mode that is then rectified by full-wave power rectifiers. The time ratios of the push, pull, and off conditions are controlled by a modulator circuit.

The on-state voltage is unregulated and is always greater than the required output voltage from the filter. It is supplied by a low-impedance source that consists of a transformer with closely coupled windings, the main supply, and a saturated transistor. The on-state voltage is decreased to the specified output value by an inductor that forms part of the filter. Thus the filter, which converts the ac signals to a dc output, is a "choke-input" type.

The switching-regulator supply operates at a frequency above the audio range to permit use of a small isolation transformer, and also to prevent sound generation.

The pulse-width-modulated converter, see chapter on Power Conversion, is finding increasingly widespread use in high-current low-voltage regulated power supplies. Such supplies use switching regulators, rather than the more common dissipating regulators, to eliminate the need for a 60-Hz power transformer and heat sinks for the transistors. As a result, pulse-width-modulated (i.e., switching-regulator) supplies offer the following important advantages over conventional power supplies:

1. Smaller size - volume is reduced by a factor of four. This size reduction does not cause any cooling problems because pulse-width-modulated supplies dissipate very little power.

2. Higher efficiency - power dissipation in the regulator is virtually eliminated; only the power rectifiers require cooling. The reduction in heat dissipation for a 250-watt supply can be 200 to 300 watts, which represents a substantial economic saving.

3. Reduced weight - weight is reduced by a factor of five. Portability is improved, mounting is simpler, and chassis cost is decreased.

Table VII compares the basic features of a conventional (series-regulated) power supply and a pulse-width-modulated (switching-regulator) power supply.

A switching-regulator circuit using the CA3085A is shown in Fig. 136. The values of L and C (1.5 millihenries and 50 microfarads, respectively) are commercially available com-

ponents having values approximately equal to the computed values in the previous design example.

$$R_{LIMIT} = \frac{0.7}{1.2\, I_L(MAX)} \qquad V_O = V_{REF.}\left(\frac{R1+R2}{R1}\right)$$

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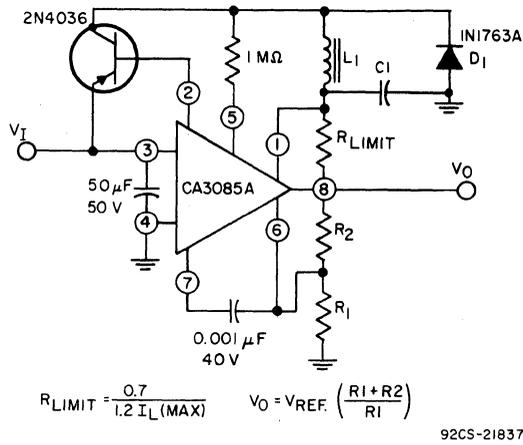
Fig. 136 - Typical switching regulator circuit.

Power Conversion

In many applications, the optimum value of voltage is not available from the primary power source. In such instances, dc-to-dc converters or dc-to-ac inverters may be used, with or without regulation, to provide the optimum voltage for a given circuit design.

An **inverter** is a power-conversion device used to transform dc power to ac power. If the ac output is rectified and filtered to provide dc again, the over-all circuit is referred to as a **converter**. The purpose of the converter is then to change the magnitude of the available dc voltage.

BASIC CIRCUIT ELEMENTS

Power-conversion circuits, both inverters and converters, consist basically of some type of "chopper". Fig. 137(a) shows a simple chopper circuit. In this circuit, a switch S is connected between the load and a dc voltage source E. If the switch is alternately closed and opened, the output voltage across the load will be as shown in Fig. 137(b). If the on-off intervals are equal, the average voltage across the load is equal to E/2. The average voltage across the load can be varied by varying the ratio of the on-to-off time of the switch, by periodically varying the repetition rate, or by a combination of these factors. If a filter is

added between the switch and the load, the fluctuations in the output can be suppressed, and the circuit becomes a true dc-to-dc stepdown transformer (or converter).

In practice, the switch shown in Fig. 137 may be replaced by a power transistor, in which case the switch is opened or closed by application of the appropriate polarity signal to the transistor base. The chopping or switching function in the inverter circuit is usually performed by high-speed transistors connected in series with the primary winding of the output transformer.

The design of the transformer is an important consideration because this component determines the size and frequency of the converter (or inverter), influences the amount of regulation required after the conversion or inversion is completed, and provides the transformation ratio necessary to assure that the desired value of output voltage is delivered to the load circuit.

Inverters may be used to drive any equipment which requires an ac supply, such as motors, ac radios, television receivers, or fluorescent lighting. In addition, an inverter can be used to drive electromechanical transducers in ultrasonic equipment, such as ultrasonic cleaners and sonar detection devices. Similarly, converters may be used to provide the operating voltages for equipment that requires a dc supply.

Transistor inverters can be made very light in weight and small in size. They are also highly efficient circuits and, unlike their mechanical counterparts, have no moving components.

Fig. 137 - *Simple chopper circuit and output-voltage waveform.*

TYPES OF INVERTERS AND CONVERTERS

Several types of transistor circuits may be used to convert a steady-state dc voltage into either an ac voltage (inversion) or another dc

voltage (conversion). The simplest converter circuit is the blocking-oscillator, or ringing-choke, power converter which consists of one transistor and one transformer. More complex circuits use two transistors and one or two transformers.

In the ringing-choke type of dc-to-dc converter, a blocking oscillator (chopper circuit) is transformer-coupled to a half-wave rectifier type of output circuit. The rectifier converts the pulsating oscillator output into a fixed-value dc output voltage.

When the oscillator transistor conducts (as a result of either a forward bias or external drive), energy is transferred to the collector inductance presented by the primary winding of the transformer. The voltage induced across the transformer is fed back (from a separate feedback winding) to the transistor base through a resistor. This voltage increases the conduction of the transistor until it is driven into saturation. A rectifier diode in series with the secondary winding of the transformer is oriented so that no power is delivered to the load circuit during this portion of the oscillator cycle.

Fig. 138(a) shows the basic configuration for a practical ringing-choke converter, which is basically a one-transistor, one-transformer circuit. Fig. 138(b) shows the waveforms obtained during an operating cycle.

During the "on" or conduction period of the transistor (t_{on}), energy is drawn from the battery and stored in the inductance of the transformer. When the transistor switches off, this energy is delivered to the load. At the start of t_{on}, the transistor is driven into saturation, and a substantially constant voltage, waveform A in Fig. 138(b), is impressed across the primary by the battery. This primary voltage produces a linearly increasing current in the collector-primary circuit, waveform B. This increasing current induces substantially constant voltages in the base windings, shown by waveform C, and in the secondary winding.

The resulting base current is substantially constant and has a maximum value determined by the base-winding voltage, the external base resistance R_B, and the input conductance of the transistor. Because the polarity of the secondary voltage does not permit the rectifier diode to conduct, the secondary is open-circuited. Therefore, during the conduction period of the transistor t_{on}, the load is supplied only by energy stored in the output capacitor

Fig. 138 - Ringing-choke converter circuit: (a) Schematic diagram; (b) Typical operating waveforms in a ringing-choke converter-(A) primary voltage; (B) primary current; (C) base-to-emitter voltage; (D) secondary current; (E) magnetic flux in transformer core.

C_{OUT}.

The collector-primary current increases until it reaches a maximum value I_P which is determined by the maximum base current and base voltage supplied to the transistor. At this instant, the transistor starts to move out of its saturated condition with the result that the collector-primary current and the voltage across the transformer windings rapidly decrease, and "switch-off" occurs.

After the transistor has switched off, the circuit starts to "ring", i.e., the energy stored in the transformer inductance starts to discharge into the stray capacitance of the circuit,

with the result that the voltages across the primary, base, and secondary windings reverse polarity. These reverse voltages rapidly increase until the voltage across the secondary winding exceeds the voltage across the output capacitor. At this instant the diode rectifier starts to conduct and to transfer the energy stored in the inductance of the transformer to the output capacitor and load. Because the output capacitor tends to hold the secondary voltage substantially constant, the secondary current decreases at a substantially constant rate, as shown by waveform D in Fig. 138(b). When this current reaches zero, the transistor switches on again, and the cycle of operation repeats.

The operating efficiency of the ringing-choke inverter is low, and the circuit, therefore, is used primarily in low-power applications. In addition, because power is delivered to the output circuit for only a small fraction of the oscillator cycle (i.e., when the transistor is not conducting), the circuit has a relatively high ripple factor which substantially increases output filtering requirements. This converter, however, provides definite advantages to the system designer in terms of design simplicity and compactness.

Transistor power inverter/converters are generally required to drive either a resistive or an inductive load. Each load affects the transistor somewhat differently with respect to over-all switching power losses. There are essentially four clases of inverter/converter circuits commonly used:

1. Forward inverter
2. Flyback inverter
3. Push-pull switching inverter
4. Half-bridge or full-bridge inverter

Flyback and push-pull inverters are discussed below as illustrations of resistive and inductive loading.

Flyback Inverter

Fig. 139(a) shows a typical flyback converter circuit which uses a single transistor as the switching device. The transistor is driven with a positive rectangular input pulse of controllable width and constant period. In this circuit, when the base control or drive pulse turns on the transistor, a current I_P builds up in the primary winding (which serves as a choke) of transformer T1, as shown in Fig. 139(b). The secondary winding of the transformer is phased so that the diode D1 blocks the flow of secondary current at this time. The primary or collector current I_P rises linearly, provided the winding series resistance is low, to a final value determined by the primary winding L1, the supply voltage V_{CC}, and the turn-on duration t_{on} of the transistor. The transistor is considered to be inductively loaded. Energy is

$$Pd(sw) = \frac{1}{2} I_p \, V_{sat} \left(\frac{t_{ON}}{T}\right) \left[1 + \frac{t_f}{t_{ON}} \frac{V_{CE\,(max)}}{V_{CE\,(sat)}}\right]$$

(b)   92CS-28704R1
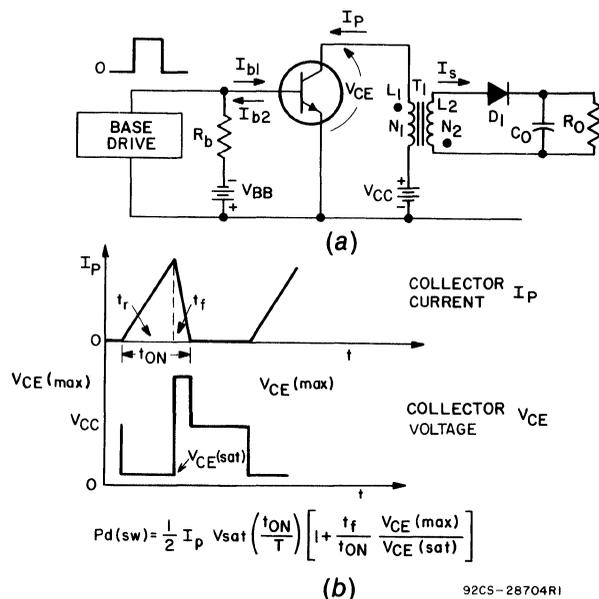
Fig. 139 - Flyback inverter circuit and waveforms.

stored in the primary winding during the on-time of the transistor. The maximum amount of energy stored must be sufficient to support the secondary load requirements. This energy is released into the secondary side after the transistor is turned off, and secondary current flows through the diode D1 into the filter capacitor C_O and the load. In this circuit, however, the transistor is subjected to certain electrical stresses during the switching process which, if not clearly understood and controlled, can result in serious device degradation or failure.

Push-Pull Transformer-Coupled Inverters and Converters

The **push-pull switching inverter** is probably the most widely used type of power-conversion circuit. For inverter applications, the circuit provides a square-wave ac output. When the inverter is used to provide dc-to-dc conversion, the square-wave voltage is usually applied to a full-wave bridge rectifier and filter. Fig. 140 shows the basic configuration for a push-pull switching converter. The single saturable transformer controls circuit switching and provides the desired voltage transformation for the square-wave output delivered to the bridge rectifier. The rectifier and filter convert the square-wave voltage into a smooth, fixed-amplitude dc output voltage.

When the voltage V_{CC} is applied to the converter circuit, current tends to flow through both switching transistors Q_1 and Q_2. It is very unlikely, however, that a perfect balance can be achieved between corresponding active and passive components of the two transistor sections; therefore, the initial flow of current through one of the transistors is slightly larger than that through the other transistor. If transistor Q_1 is assumed to conduct more heavily initially, the rise in current through its collector inductance causes a voltage to be induced in the feedback windings of transformer T_1 which supply the base drive to transistors Q_1 and Q_2. The base-drive voltages are in the proper polarity to increase the current through Q_1 and to decrease the current through Q_2. As a result of regenerative action, the conduction of Q_1 is rapidly increased, and Q_2 is quickly driven to cutoff.

The increased current through Q_1 causes the core of the collector inductance to saturate. The inductance no longer impedes the rise in current, and the transistor current increases sharply into the saturation region. For this condition, the magnetic field about the collector inductance is constant, and no voltage is induced in the feedback windings of transformer T_1. With the cutoff base voltage removed, current is allowed to flow through transistor Q_2. The increase in current through the collector inductance of this transistor causes voltages to be induced in the feedback windings in the polarity that increases the current through Q_2 and decreases the current through Q_1. This effect is aided by the collapsing magnetic field about the collector inductance of Q_1 that results from the decrease in current through this transistor. The feedback voltages produced by this collapsing field quickly drive Q_1 beyond cutoff and further increase the conduction of Q_2 until the core of the collector inductance for this transistor saturates to initiate a new cycle of operation. The square wave of voltage produced by the
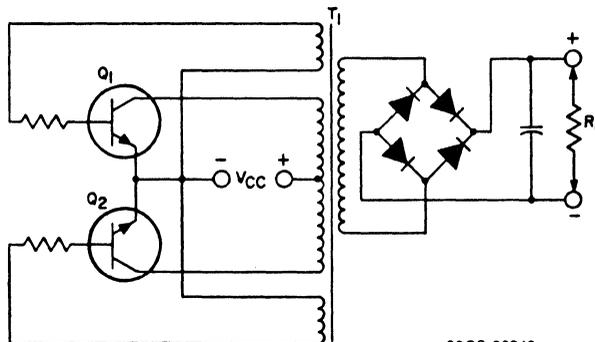
92CS-36243

Fig. 140 - Basic circuit configuration of a single-transformer push-pull switching converter.

switching action of transistors Q_1 and Q_2 is coupled by transformer T_1 to the bridge rectifier and filter, which develop a smooth, constant-amplitude dc voltage across the load resistance R_L. The small ripple produced by the square wave greatly simplifies filter requirements.

Push-pull transformer-coupled converters with full-wave rectification provide power to the load continuously and are, therefore, well suited for low-impedance, high-power applications. The push-pull configuration provides high efficiency and good regulation. In driven inverters such as that shown in Fig. 141(a), the output power transistor is switched by a multivibrator drive which is usually controlled by logic circuitry. Controlled-drive push-pull inverters are useful for precision systems requiring carefully controlled frequency or pulse-width control. Careful control of the input-drive pulse width, as in pulse-width-modulated switching systems, eliminates common-mode conduction between the transistors. Good load regulation can also be achieved.

As the switching-drive circuit in Fig. 141(a) alternately saturates and cuts off each transistor switch, an alternating voltage is generated across the winding of transformer T1
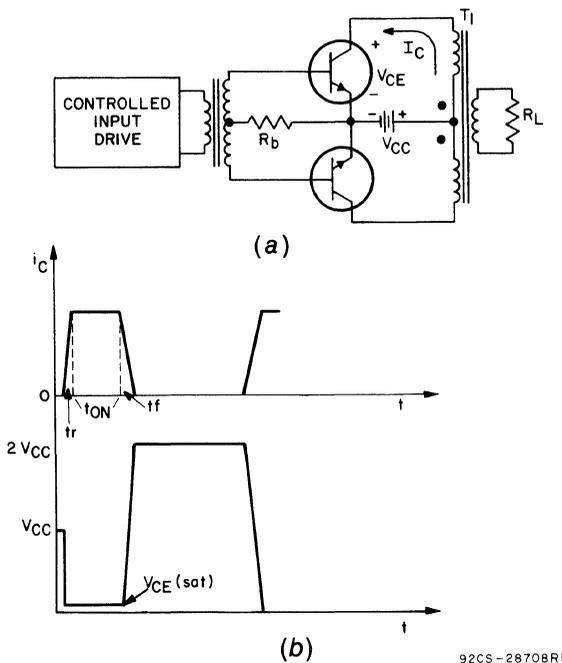
and delivered to the output circuit. A voltage equal to the dc supply voltage V_{CC} less the $V_{CE}(sat)$ of the conducting transistor is directly impressed across one-half the primary winding of T1. The voltage impressed across the non-conducting transistor is approximately twice the amplitude of V_{CC}. Although the voltages across the primary and secondary windings are always a square wave, no matter what load is used, the current waveform in the primary is not a square wave if other than a resistive load is used.

Fig. 142 shows a **four-transistor, single-transformer bridge configuration** that is often used in inverter or converter applications. In this type of circuit, the primary winding of the output transformer is simpler and the breakdown-voltage requirements of the transistors are reduced to one-half those of the transistors in the push-pull converter shown in Fig. 140.

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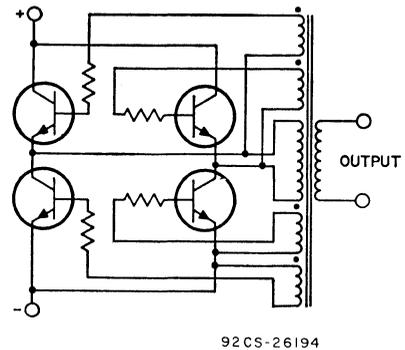
Fig. 142 - Basic circuit configuration of a four-transistor, single-transformer bridge inverter.

Fig. 143 shows the schematic diagram for a **two-transistor, two-transformer converter**. In this circuit, a small saturable transformer provides the base drive for the switching transistors, and a nonsaturable output transformer provides the coupling and desired voltage transformation of the output delivered to the load circuit. With the exception that it uses a separate saturable transformer, rather than feedback windings on the output transformer, to provide base drive for the transistors, this converter is very similar in its operation to the basic push-pull converter shown in Fig. 140. The saturable-transformer technique may also be applied in the design of a bridge converter, as shown in Fig. 144.

(a)

(b) 92CS-28708RI

Fig. 141 - Driven inverter circuit and waveforms.
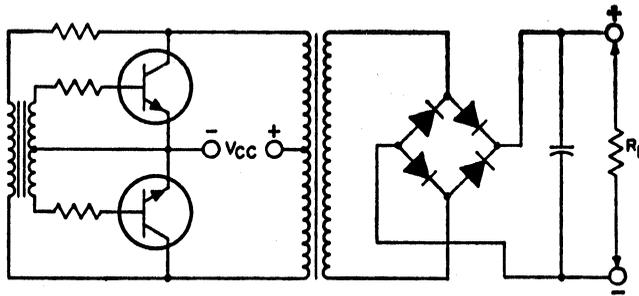
92CS-36242

Fig. 143 - Basic circuit configuration of a two-transformer push-pull switching converter.
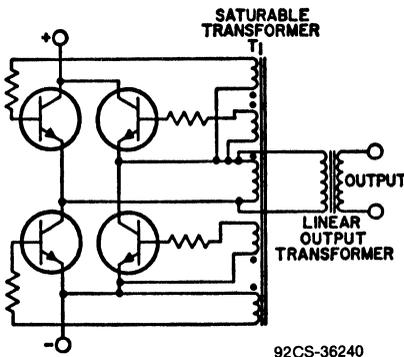
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Fig. 144 - Basic configuration of a four-transistor bridge inverter that uses a saturable output transformer.

DESIGN OF PRACTICAL TRANSISTOR INVERTERS

The design of practical inverter (or converter) circuits involves, essentially, selection of the proper transistors and design of the transformers to be used. The particular requirements for the transistors and transformers to be used are specified by the individual circuit design. The following paragraphs discuss the design of three basic inverter circuits: the simple one-transistor, one-transformer (ringing-choke) type and two push-pull switching converters (a two-transistor, one-transformer type and a two-transistor, two-transformer type). The operation of each circuit is described. For design equations and sample designs, refer to **RCA Solid State Power Circuits Handbook**, SP-52 Series.

Two-Transistor, One-Transformer Converter

Fig. 145 shows a push-pull, transformer-coupled, dc-to-dc converter that uses one transformer and two transistors. Fig. 146 shows the waveforms obtained from this
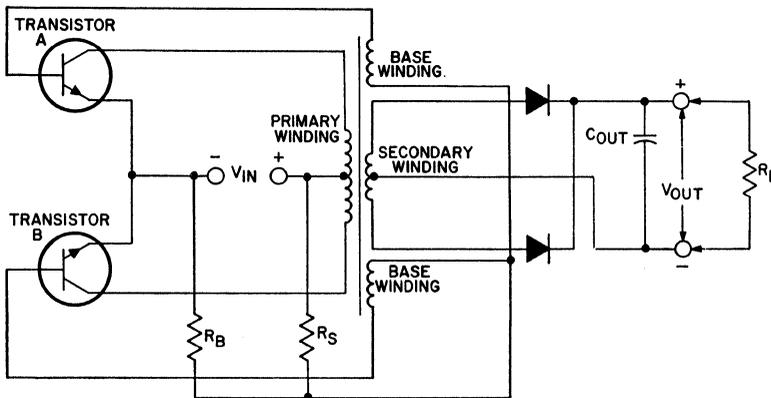
92CS-26181

Fig. 145 - Two-transistor, one-transformer push-pull switching converter.

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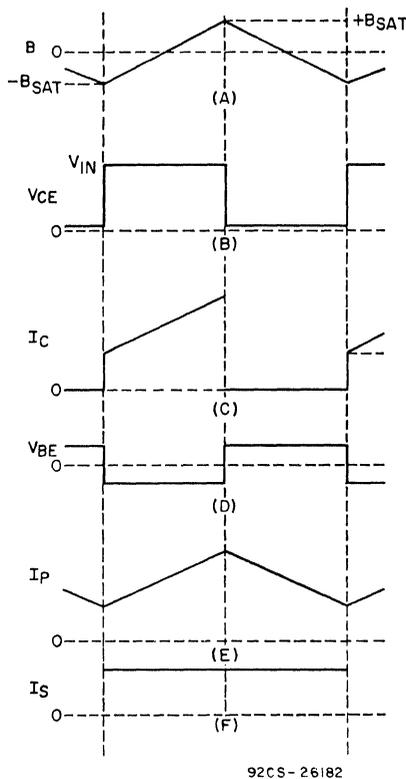
Fig. 146 - Typical operating waveforms for a two-transistor, one-transformer switching converter: (A) flux density in transformer core; (B) collector voltage of one transistor; (C) collector current of one transistor; (D) base voltage of one transistor; (E) primary current; (F) secondary current.

circuit during one complete operating cycle.

During a complete cycle, the flux density in the transformer core varies between the saturation value in one direction and the saturation value in the opposite direction, as shown by waveform A in Fig. 146. At the start of the conduction period for one transistor, the flux density in the core is at either its maximum negative value ($-B_{sat}$) or its maximum positive value ($+B_{sat}$).

For example, transistor A switches "on" at $-B_{sat}$. During conduction of transistor A, the flux density changes from its initial level of $-B_{sat}$ and becomes positive as energy is simultaneously stored in the inductance of the transformer and supplied to the load by the

battery. When the flux density reaches $+B_{sat}$, transistor A is switched off and transistor B is switched on. The transformer assures that energy is supplied to the load at a constant rate during the entire period that transistor A conducts. This energy-transformation cycle is repeated when transistor B conducts.

Initially, sufficient bias is applied to saturate transistor A. As a result, a substantially constant voltage, waveform B in Fig. 146, is impressed across the upper half of the primary winding by the dc source V_{in}. This bias voltage can be a temporary bias, a small fixed bias, or even a small forward bias developed across the bias winding as a result of leakage and saturation current flowing in the transformer primary. The constant primary voltage causes a dc component and a linearly increasing component of current, waveform C in Fig. 146, to flow through transistor A. As in the ringing-choke converter, the linearly increasing primary current induces substantially constant voltages, waveform D in Fig. 146, in the base winding and secondary winding. The induced voltage in the base winding limits the maximum value of the base current and, therefore, of the collector current.

In the push-pull transformer-coupled converter, the transition to switch-off is initiated when the transformer begins to saturate. As long as the transistor is not saturated, the product of the transformer inductance and the time rate of change of the collector current remains constant. When the transformer core saturates, however, the inductance decreases rapidly toward zero, with the result that the time rate of change of the collector current increases towards infinity. When the collector current reaches its maximum value, transistor A moves out of saturation and the winding voltages decrease and then reverse and thereby cause transistor A to switch off. The reversal of the winding voltages switches transistor B on, and the switching operation is repeated.

One-Transistor, One-Transformer Converter

Fig. 147(a) shows the basic configuration for a practical circuit of a ringing-choke converter, which is basically a one-transistor, one-transformer circuit. Fig. 147(b) shows the waveforms obtained during an operating cycle.

During the "on" or conduction period of the transistor (t_{on}), energy is drawn from the battery and stored in the inductance of the transformer. When the transistor switches off,
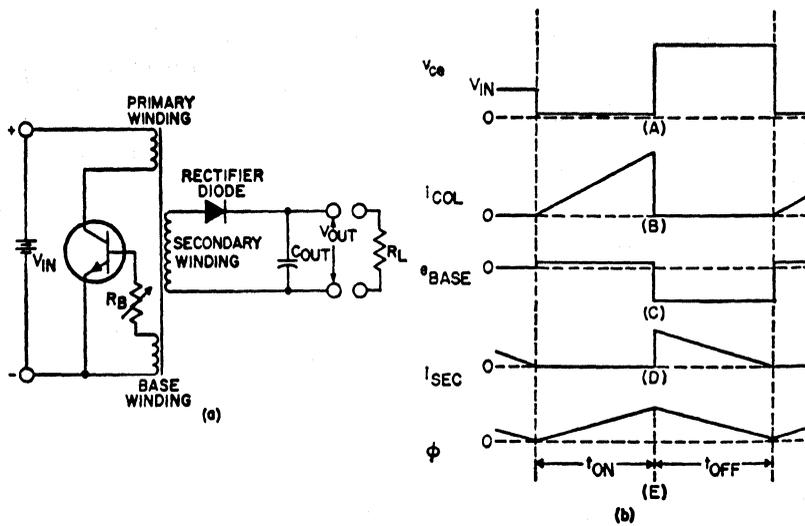
Fig. 147 - Ringing-choke converter cir-
cuit: (a) Schematic diagram;
(b) Typical operating wave-
forms in a ringing-choke con-
verter-(A) primary voltage; (B)
primary current; (C) base-to-
emitter voltage; (D) secondary
current; (E) magnetic flux in
transformer core.

this energy is delivered to the load. At the start of t_{on}, the transistor is driven into saturation, and a substantially constant voltage, waveform A in Fig. 147(b), is impressed across the primary by the battery. This primary voltage produces a linearly increasing current in the collector-primary circuit, waveform B. This increasing current induces substantially constant voltages in the base windings, shown by waveform C, and in the secondary winding.

The resulting base current is substantially constant and has a maximum value determined by the base-winding voltage, the external base resistance R_B, and the input conductance of the transistor. Because the polarity of the secondary voltage does not permit the rectifier diode to conduct, the secondary is open-circuited. Therefore, during the conduction period of the transistor t_{on}, the load is supplied only by energy stored in the output capacitor C_{out}.

The collector-primary current increases until it reaches a maximum value I_P which is determined by the maximum base current and base voltage supplied to the transistor. At this

instant, the transistor starts to move out of its saturated condition with the result that the collector-primary current and the voltage across the transformer windings rapidly decrease, and "switch-off" occurs.

After the transistor has switched off, the circuit starts to "ring", i.e., the energy stored in the transformer inductance starts to discharge into the stray capacitance of the circuit, with the result that the voltages across the primary, base, and secondary windings reverse polarity. These reverse voltages rapidly increase until the voltage across the secondary winding exceeds the voltage across the output capacitor. At this instant the diode rectifier starts to conduct and to transfer the energy stored in the inductance of the transformer to the output capacitor and load. Because the output capacitor tends to hold the secondary voltage substantially constant, the secondary current decreases at a substantially constant rate, as shown by waveform D in Fig. 147(b). When this current reaches zero the transistor switches on again, and the cycle of operation repeats.

Two-Transistor, Two-Transformer Inverters

There are three basic disadvantages associated with the two-transistor, one-transformer inverter. First, the peak collector current is independent of the load. This current, therefore, depends on the available base voltage, the gain of the transistor, and the input characteristic of the transistor. Second, because of the dependence of the peak current on transistor characteristics, the circuit performance depends on the particular transistor used because there is a wide spread in transistor characteristics. Third, the transformer, which is relatively large must use expensive square-loop material and must have a high value of flux density at saturation. These disadvantages can be overcome by the use of two transformers in various circuit arrangements, such as that shown in Fig. 148.

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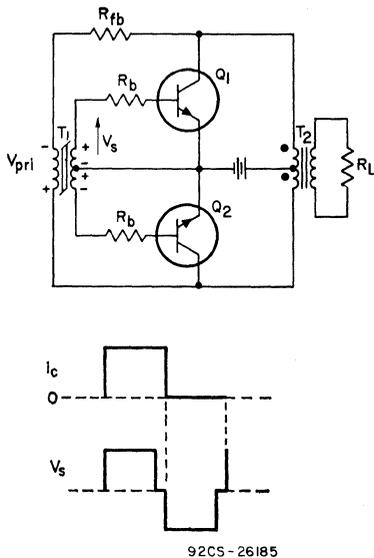
Fig. 148 - Two-transistor, two-transformer push-pull switching inverter.

In this type of circuit, a saturable base-drive transformer T_1 controls the inverter switching operation at base-circuit power levels. The linearly operating output transformer transfers the output power to the load. Because the output transformer T_2 is not allowed to saturate, the peak collector current of each transistor is determined principally by the value of the load impedance. This feature provides high circuit efficiency. The operation of the inverter circuit is described as follows.

It is assumed that, because of a small unbalance in the circuit, one of the transistors, Q_1 for example, initially conducts more heavily than the other. The resulting increase in the voltage across the primary of output transformer T_2 is applied to the primary of base-drive transformer T_1 in series with the feedback resistor R_{fb}. The secondary windings of transformer T_1 are arranged so that transistor Q_1 is driven to saturation. As transformer T_1 saturates, the rapidly increasing primary current causes a greater voltage drop across feedback resistor R_{fb}. This increased voltage reduces the voltage applied to the primary of transformer T_1; thus, the drive input and ultimately the collector current of transistor Q_1 are decreased.

In the circuit arrangement shown in Fig. 148, the base is driven hard compared to the expected peak collector current (forced beta of ten, for example). If the storage time of the transistor used is much longer than one-tenth of the total period of oscillation T, the transistors begin to have an appreciable effect on the frequency of operation. In Fig. 148, the storage time could conceivably be quite long because there is no turn-off bias (the drive voltage only decreases to zero) for Q_1 until the collector current of Q_1 begins to decrease.

Two methods of overcoming this problem by decreasing the storage time are shown in Fig. 149. In Fig. 149(a) a capacitor is placed in parallel with each base resistor R_B. When V_s is positive, the capacitor charges with the polarity shown. When V_s decreases to zero, this capacitor provides turn-off current for the transistor. In Fig. 149(b), a feedback winding from the output transformer is placed in series with each base. The base-to-emitter voltage V_{BE} is then expressed as follows:

$$V_{BE} = V_s - V_{rb} - V_T$$

If V_s decreases to zero and the collector current does not begin to decrease, then the base-to-emitter voltage is expressed simply by

$$V_{BE} = V_{rb} - V_T$$

A turn-off bias is thus provided to decrease the collector current.

The energy stored in the output transformer by its magnetizing current is sufficient to assure a smooth changeover from one transistor to the other. The release of this stored energy allows the inverter-circuit switching to be accomplished without any possibility of a
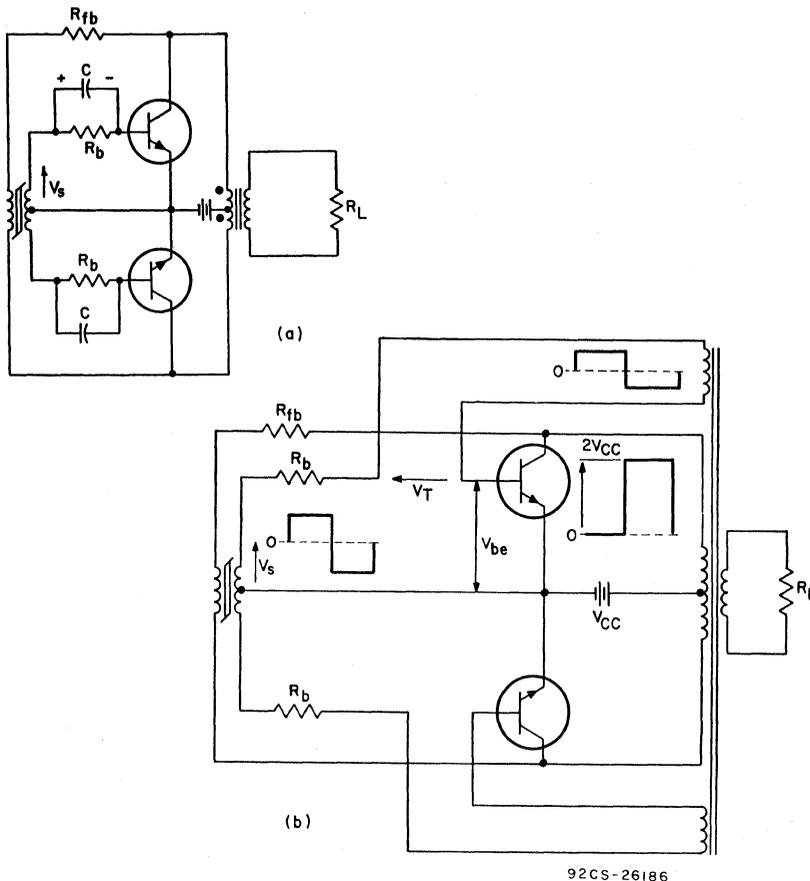
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Fig. 149 - Two-transistor, two-transformer push-pull switching inverters in which transistor-storage times are reduced: (a) Capacitor in parallel with each base resistor assures sharp turn-off of associated transistor; (b) Feedback winding from output transformer in series with base of each transistor assures sharp cutoff characteristics.

"hang-up" in the crossover region during the short period when neither transistor is conducting.

The operation of the high-speed converter is relatively insensitive to small system variations that may cause slight overloading of the circuit. Under such conditions, the base power decreases; however, this loss is so small that it does not noticeably affect circuit performance. At the same time, the amount of energy stored in the output transformer also increases. Although this increase results in a greater transient dissipation, the inverter switching is still effected smoothly.

A practical design of the high-speed converter should include some means of initially biasing the transistors into conduction to assure that the circuit will always start. Such starting circuits, as described later, can be added readily to the converter, and are much more reliable than one which depends on circuit imbalance to shock the converter into oscillation.

Four-Transistor Bridge Inverters

Fig. 150 shows a four-transistor, single-transformer bridge configuration that is often used in inverter or converter applications. In this type of circuit, the primary winding of the output transformer is simpler and the breakdown-voltage requirements of the transistors are reduced to one-half those of the transistors in the push-pull converter shown in Fig. 145.

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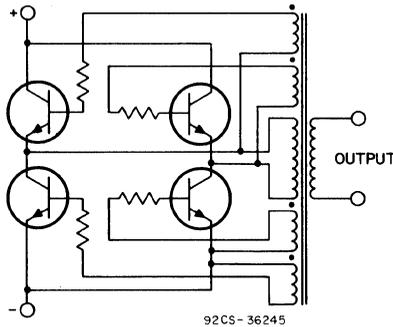
Fig. 150 - Basic circuit configuration of a four-transistor, single-transformer bridge inverter.

The separate saturable-transformer technique may also be applied in the design of a bridge converter, as shown in Fig. 151.

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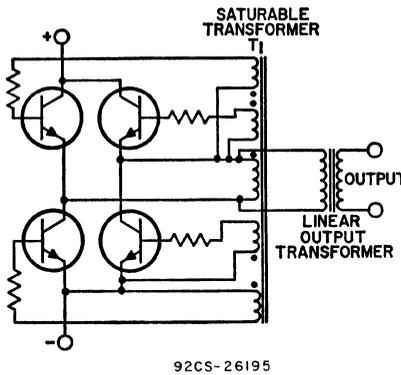
Fig. 151 - Basic configuration of a four-transistor bridge inverter that uses a saturable output transformer.

Three-phase bridge inverters for induction motors are usually used to convert dc, 60-Hz, or 400-Hz input to a much higher frequency, possibly as high as 10 kHz. Increasing frequency reduces the motor size and increases the horsepower-to-weight ratio, desirable features in military, aviation, and portable

industrial power-tool markets. Fig. 152 shows a typical three-phase bridge circuit with base driving signals and transformer primary currents.
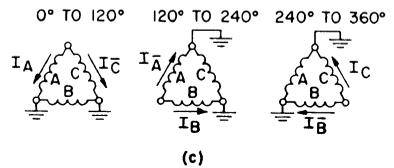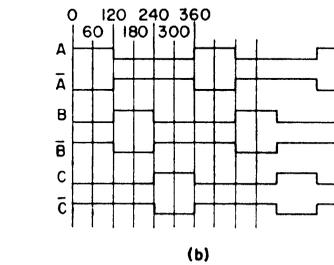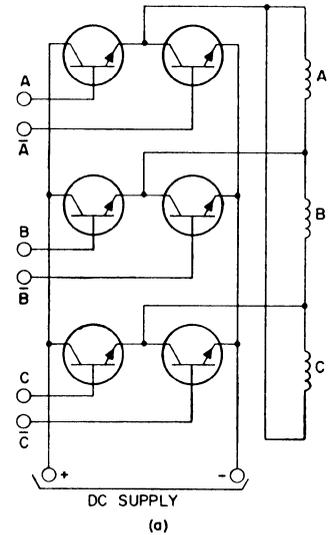
Fig. 152 - Three-phase bridge inverter: (a) circuit configuration; (b) base driving signals; (c) transformer primary current switching.

DESIGN OF OFF-THE-LINE INVERTER AND CONVERTER CIRCUITS

Power transistors have been used successfully in the past to generate and control large amounts of ac or dc power at low frequencies such as 60 and 400 cycles. At these low frequencies, however, most power sources are

bulky because large amounts of magnetic materials are required in transformers and inductors, particularly if kilowatts of power output are required.

The current trend in power inverter/converter designs is to use higher-frequency switching techniques and direct operation from the available utility lines (i.e., 110/220 V). The use of higher operating frequencies reduces not only the magnetic materials required but also the size of the filter capacitors. Direct off-line operation and the use of power transistors with high voltage breakdowns and peak-current-handling capabilities, combined with high-frequency switching techniques, have resulted in a new generation of power sources which are substantially smaller and have good efficiency and reliability.

General Design Considerations

The designer of a power inverter/converter usually must satisfy certain specification requirements, such as ac or dc power output, ac or dc input voltage, output frequency and waveform (inverter), load characteristics (including starting load, phase angle, duty cycle, and desired regulation), efficiency, maximum size and weight, minimum and maximum operating temperature (or other environmental requirements), and cost effectiveness.

The circuit designer's first task is to select a switching transistor capable of performing the intended function most economically and efficiently. Information supplied by manufacturers is usually very general, and the circuit engineer has the problem of relating this information to his particular design requirements. His selection of the switching transistor may be further complicated by a limited knowledge of the relative merits of transistors as switching devices. The designer may be inclined to select devices which are compatible with his experience, although not necessarily cost-effective. Selection of the proper switching device can be simplified if the relative merits of transistor switching capabilities are better understood.

Selection of the Switching Device

The selection of a switching transistor depends primarily on the power output level required. Table VIII lists the characteristics of the 2N6678 SwitchMax power transistor.

A switching device for off-line, high-frequency, switch-mode inverter circuits must possess the following characteristics:

(a) High-voltage breakdown capability to withstand the maximum peak inverse voltage and transient voltages encountered.

Table VIII - Device Characteristics

Characteristic	Transistor 2N6678
Max. Voltage	V_{CEO}=400 V
Peak Current	I_C=15 A
Switching Characteristics	t_r=0.6 μs t_f=0.5 μs
Forward Voltage Drop	V_{CE}(sat)=1 V @ I_C=15 A

(b) High peak current capability to support the output load current demand.

(c) Fast switching speed characteristics (i.e., sufficiently low turn-on and turn-off times) to minimize transient switching power dissipation.

Transistors are available which possess all of these unique features. The RCA-2N6678 transistor is a representative device for high-frequency power-switching applications.

Fig. 153 shows that the RCA-2N6678 can provide peak collector currents of 15 amperes with current gain of 8 up to approximately 22 kHz. The peak current of the transistor is limited by both gain and dissipation at high frequencies. Because the maximum V_{CEO} of the RCA-2N6678 is 400 volts, the transistor is limited to 110-V, off-line application in both single-ended (flyback) and push-pull circuits.
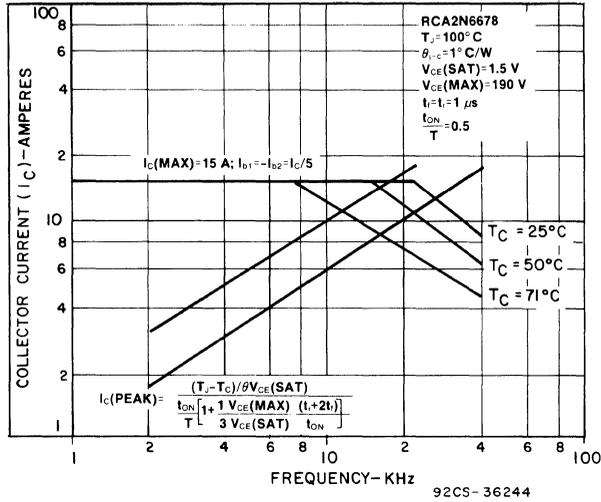
Fig. 153 - I_C as a function of frequency in the push-pull arrangement.

230-WATT, 40-KHZ, OFF-LINE FORWARD CONVERTER

The performance of the 2N6673 SwitchMax power transistor is demonstrated in the following 230-watt, 15-volt, 15-ampere off-line converter operating at 40 kHz from a 120-volt, 60-cycle line; a block diagram of the circuit is shown in Fig. 154. The 2N6673 is designed, characterized, and tested for the parameters critical to this type of converter
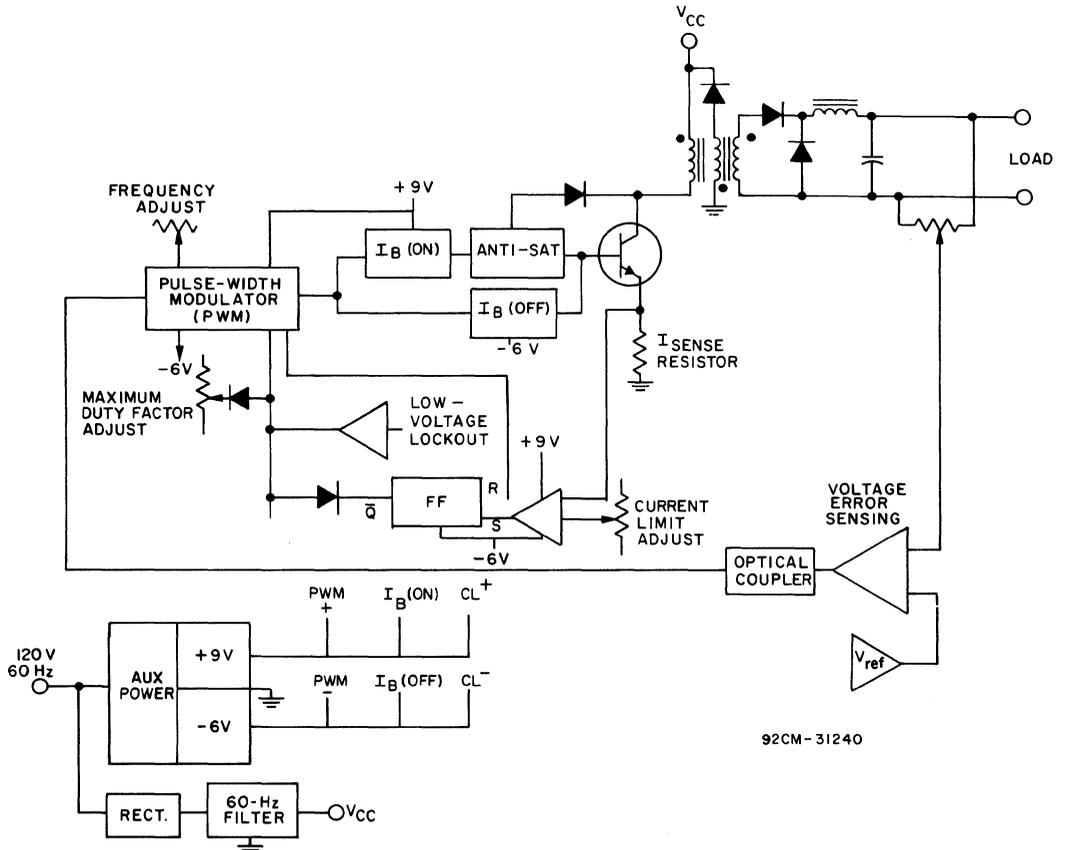
Fig. 154 - Block diagram of 230-watt single-ended converter.

design which is capable of providing 230 watts output, 15.5 amperes at 15 volts, from a low line of 100 volts rms to a high line of 135 volts. At high line, the power-switching device dissipates only 17 watts (4 watts saturation plus 13 watts switching). Table IX shows the performance to be expected from this converter. The primary purpose of this circuit is to demonstrate switching-device/circuit-format compatibility and capability and not to propose the design of a converter complete to commercial standards.

Table IX - Converter Performance

Regulation

Regulation is 0.2% from no load at $V_{high\ line}$=135 V(rms) to 230-watt load at $V_{low\ line}$=100 V(rms).

Overall Efficiency

Overall efficiency, including blower and auxiliary power is 70% at low line (100 V(rms)) to 67.24% at high line (135 V(rms)).

Efficiency of Converter System Alone

Efficiency of converter system alone is 78% or

$$\frac{234\ \text{watts out}}{299\ \text{watts in}}.$$

Ripple

40-kHz ripple is 20 mV or better, Fig. 7(b), 60/120-Hz ripple is unmeasurable at 50 mV/division, Fig. 7(d).

HF Switching Noise

HF switching noise is approximately 1.2 volts peak-to-peak, the exact value is obscured by rfi received on load-box leads and shielding problems in the measurement.

Transient Response

Transient response at no load to full load: V_{dip}=2 volts maximum; 90% recovery in 5 milliseconds or less.

The advantages of the forward converter design are its electrical simplicity and parts economy. These advantages are manifest by:
1. The simple power transformer.
2. The single power-switching device required.
3. Single-ended operation which, with the tertiary demagnetizing winding, avoids the core saturation problems caused by the unmatched switching characteristics

or winding dissymmetries that occur in some push-pull configurations.
4. The faster response to step changes in load made possible by the availability of higher than normal switching frequencies.

The following considerations must be observed to assure reliable forward-converter operation; these considerations are given below in the form of comparisons with a push-pull type of converter.
1. The transformer core must have 1.5 to 2 times the cross section of a push-pull core because of the unsymmetrical flux operation.
2. Because of the reduced duty factor allowed for the forward converter (0.5 maximum), the output choke must be correspondingly large or the switching frequency must be increased.
3. The power-switching devices and high-frequency rectifiers must be able to handle up to twice the peak current that devices in a push-pull design of the same power would be required to handle.
4. Because of the transformer and choke considerations mentioned above, it is desirable to increase the operating frequency of the forward converter beyond that which would be used with a push-pull converter. This increase mandates proportionately increased switching losses in the power switch, thus requiring faster switches or larger heat sinks and/or more sophisticated drive techniques. The SwitchMax transistor has demonstrated its special amenability to the higher temperatures and enhanced base-drive characteristics required for successful performance in forward converter systems.

The design of the subject converter proceeded from the operational switching ratings of the 2N6673 transistor:
1. V_{CE}(sat)=2 V max.
   V_{BE}(sat)=1.6 V max.
   @ I_C=5 A/I_B=1 A
   T_j=125° C

2. t_s=4 μs max.
   t_c=0.8 μs max.
   @ I_C=5 A, I_{B1}=I_{B2}=1 A
   V_{clamp}=450 V
   Load=25 Ω + 170 μH
   T_j=125° C

3. V_{CEX}(clamped)=450 V

Within the constraints of the forward converter configuration, an available conversion power of 234 watts was determined based on the application of these ratings in the following relationship:

Maximum Conversion Power= V_{CC}(low line)x I_C(max) x D(max) x Efficiency

where V_{CC}=130 V, I_C(max)=5 A, D(max)= Maximum Duty Factor=0.4, and Efficiency= 90%.

D(max) was chosen as 0.4 rather than 0.5 to allow for a 2.5 μs dead-space guardband at 40 kHz. The 15-volt output voltage permits use of the breadboarded circuit as a utility bench supply so that experience with the circuit can be gained.

The turn-off time losses in a switching circuit are approximated by the following relationships:

1. For the resistive load case:

$$P_F(R)= \frac{t_f x I_C(peak) x V_{CE}(peak) x f}{6}$$

2. For the clamped inductive load case:

$$P_F(I)=t_c x I_C(peak) x V_{CE}(peak) x f x 0.4$$

Assuming an operating frequency f of 40 kHz and a worst-case junction temperature of 125° C, calculations based on data-sheet values of t_s, t_c and a high line V_{CC} of 200 volts yields a $P_F(R)$ of 12 watts and a $P_F(I)$ of 29 watts. If a reasonable value of system thermal resistance, junction-to-air, of 3.3° C/W is also assumed, the maximum allowable ambient temperature t(amb.), for the resistive condition is T(amb.)= T_j(max)–P_F(R)·R_{JCSA}=125–12x3.3=85.4° C. For the inductive case the same initial expression would yield 125–29x3.3 for a T(amb.) allowable of 29.3° C.

Of course, the high line V_{CC} and full load will not exist for more than a few seconds, and the steady-state P_F(I) at high line will be closer to 26 watts. allowing a maximum ambient temperature of 39° C.

Now that the forward converter design has been shown to be thermally practical from the device standpoint, storage time must be considered. As indicated previously the t_c condition represents a worst-case data-bulletin limit obtained with a forced gain of 5 (I_C=5 A, I_{B1}=I_{B2}=1 A). Furthermore, this condition implies a worst-case t_s (storage time) of 4 microseconds at 125° C. At f=40 kHz, the **total** allowable on time (t_p) is only 12.5 microseconds, so that 4 microseconds of t_s would be intolerable. Therefore, either a proportional drive or an antisaturation clamp technique must be used to reduce the storage time. The design under discussion employs an antisaturation drive; a technique that reduces t_s to about 1 microsecond, a tolerable value. An added benefit of this choice of anti-saturation drive is an improved fall time, both t_f and t_c being improved by a factor of 1.5 to 2. Reinforcement for the antisaturation drive decision comes with the recognition that t_s is at its lengthiest for light loads at low line voltage, and that base drive proportioning in some form is essential to the existence of a manageable storage time.

Circuitry

The schematic diagram of the power output circuit is shown in Fig. 155; discussion begins with the output terminals.

As previously stated, the terminal voltage is 15 volts. The energy-storage/filter system is conventional, except that the filter choke value of approximately 120 microhenries is greater than one might consider adequate for this sort of circuit. It must be recognized that in a half-wave circuit the maximum duty factor, D, must not exceed 0.5. The secondary voltage, V_S, must, therefore, be 2.2 to 4 times the output voltage, whereas, in a full-wave circuit, V_S would be 1.1 to approximately 2.2 times the output voltage.

During the on time, DT, the current, I_C, in the energy-storage choke will consist of two parts, the pedestal current, I_p, and the ramping current, i_R, as shown in Fig. 156. During the on time, DT, this current is supplied from the rectifier and appears to the power switch as:

$$(I_p+i_R) x \frac{N_S}{N_p}=i_C \text{ (collector current)}$$

if primary magnetizing currents and losses are neglected. i_R can be found from the basic relationship $E=L\frac{di}{dt}$; $E=(V_S–V_O)$, di=i_R and dt=DT where D=$\frac{VO}{VS}$.

The power output of the circuit and its efficiency will be largely dependent on the value of the ramp current, i_R. Referred to the primary side of the transformer, the peak ramp current should be less than 1 ampere at

Fig. 155 - Power-output circuit for 230- watt forward converter.
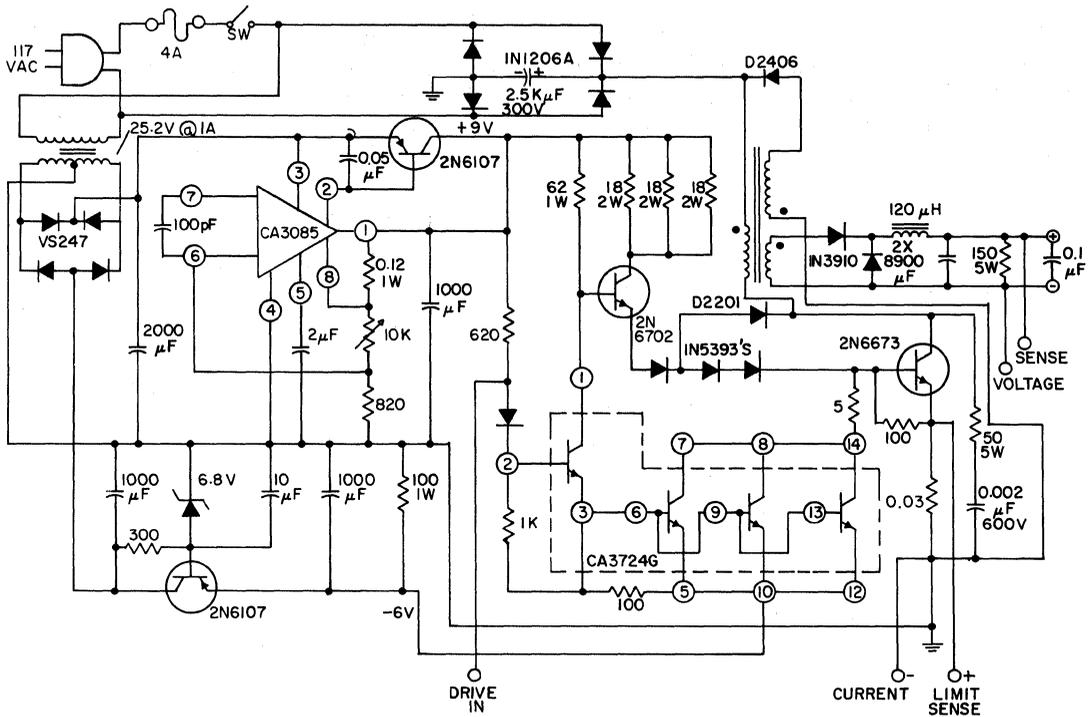
Transformer Specifications
Core - Siemens N27 Material, Type E55, Part No.
  B66251-A0000-R027
Cross Section - 0.53 in^2=354 mm^2
B_{Max}=2500 Gauss
f=40 kHz
N_1 (Primary) - 28 turns No. 18
N_2 (Demag.) - 28 turns No. 18 bifilar with N_1
N_3 (Secondary) - 8 turns 1.375 inch by 0.010 inch
  Cu strap
L_1=L_2=82 mH, L_3=500 μH, L_1 leakage (L_2L_3 short)=16
  μH

Notes: N_3 wound closest to the core, no bobbin; N_1
and N_2 wound bifilar.
Energy Storage Choke
Core Material - Same as transformer
Air Gap Across E Core - 0.090 inch
Total Air Gap in Magnetic Path - 0.180 inch
Cross Section - 0.53 inch=354 mm^2
Winding - 26 turns of No. 10 wire L @ 10 kHz, zero
  bias=120 μH

Fig. 156 - Components of the current I_L in the energy-storage choke during the on time.

high line voltage. The following equation
shows a relationship to determine the necessary
choke value.

$$L=\cfrac{(V_{CC}(\text{high line})x\cfrac{N_S}{N_P}V_O)x\cfrac{V_O}{V_{CC}(\text{high line})}x\cfrac{1}{f}}{i_R}$$

$$L=\cfrac{(200x\cfrac{8}{28}-15)x\cfrac{15}{200}x25}{1.0}=79 \mu H$$

However, the condition under which cir-
culating current must be maintained with
minimum load must also be examined. The
choke value required is given by the equation:

$$L=\cfrac{V_O(1-D)\cfrac{1}{f}}{2 I_O (\text{min})}$$

Using a minimum load current of 0.5 amperes and a DT of 0.25 (corresponding to a high line voltage), a value for L of approximately 140 microhenries is determined. Therefore, a choke with an L(min) of 140 microhenries at an I_{DC} of 1 ampere or an L(min) of 80 microhenries at an I_{DC} of 15 amperes is required.

The output capacitor value was not optimized; the key to capacitor choice is low equivalent series impedance rather than absolute capacitance. The rectifiers in Fig. 155 are 1N3910 fast-recovery DO-5 stud units.

The secondary of the transformer was strap wound. While not necessary for the current level indicated above, the strap provided a neat, flat foundation on which to position the bifilar primary and tertiary windings so that the best coupling and lowest possible leakage inductance could be realized.

Leakage inductance, Ll with secondary and tertiary shorted, was measured at 16 microhenries. The energy stored in Ll at the end of each on period cannot be commutated to the secondary. It must, therefore, be dissipated as heat either in the transistor (where it becomes reverse-bias second-breakdown energy, $E_{S/b}$)

or in an auxiliary circuit called a "snubber".

The snubber in this circuit consists of a 0.002 microfarad capacitor and a 50-ohm 5-watt resistor connected across the 2N6673 switch. This circuit will hold the worst-case collector spike voltage to less than 450 volts and the turn-on current spikes to less than 6 amperes.

The base drive arrangements of the forward-converter circuit are intended to provide 1 ampere of available I_{B1} drive by way of the

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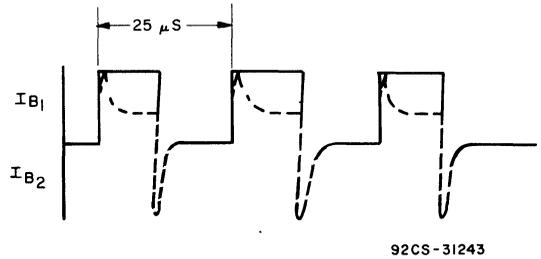
Fig. 157 - Base drive current applied to antisaturation network (solid line) and actual I_{B1} and I_{B2} in the 2N6673 base (dashed line).

(a)

(b)

(c)

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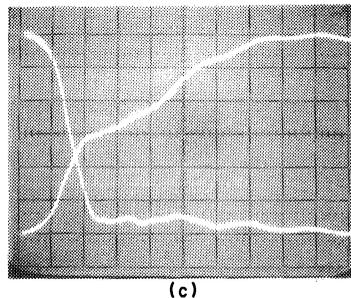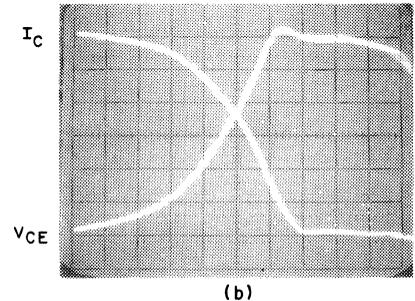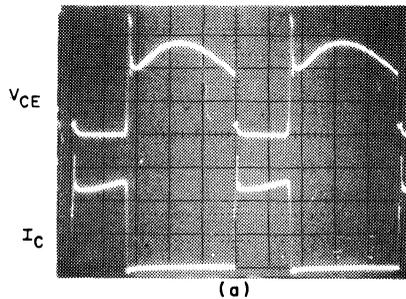
Fig. 158 - Turn-off switching behavior:

(a) Collector-voltage, collector current waveform at $I_{Load}=15.5 A$, $V_{Load}=15 V$ $V_{line}=120 V$ (rms) $V_{CE}=100 V/div.$, $I_C=2 A/div.$ t (horizontal scale)=5 μs/div.

(b) Fall time of power-switching transistor at $I_{Load}=15.5 A$, $V_{Load}=15 V$ $V_{line}=120 V$ (rms) $V_{CE}=360 V$, $I_C=5 A$ t (horizontal scale)=50 ns/div.

(c) Fall time of power-switching transistor at $I_{Load}=3 A$, $V_{Load}=15 V$ $V_{line}=120 V$ (rms) $V_{CE}=210 V$, $I_C=3 A$ peak t (horizontal scale)=50 ns/div.

2N6702, a high-speed, 7-ampere, medium-voltage switch. The combination of the D2201 fast-recovery clamp diode and the 1N5393 level-shift diodes cause the 2N6673 transistor to operate approximately 2 volts out of saturation, which greatly reduces the storage time by shunting the excess base current into the collector circuit as shown in Fig. 157. The device is turned off by a –6-volt V_{BB2}, further assuring minimal switching-loss heat generation. Turn-off switch behavior is shown in Fig. 158.

The designs of the +9-volt and –6-volt auxiliary supplies are straightforward and need no explanation.

Oscillator and Pulse-Width Modulator

The schematic diagram of the oscillator and pulse-width modulator circuit is shown in Fig. 159. The foundation of the control system is an oscillator/pulse-width-modulator integrated circuit. The oscillator-logic/comparator system powered by the +9 and –6-volt auxiliary supplies operates conventionally. The current-limiter and shut-down facilities provided on the chip are not used. The error amplifier operating only as a voltage follower is driven from the collector of the 2N6702 photocoupler, which provides the phase inversion and dc isolation from load-to-line.

Voltage Sensing—The CA723 integrated circuit voltage regulator shown in Fig. 159 provides four functions of the voltage error-sensing system:
1. Reference-voltage supply for error amplifier
2. Error amplification (non-inverting)
3. LED drive to photocoupler
4. LED current limiting (with the addition of one zener)

The output stage of the CA723 is arranged as a current limiter to prevent over powering of the LED in the photocoupler.

Because the power converter operates from a 15-volt supply, the voltage reference, error amplifier, and photocoupler can be self-powered from the 15-volt output bus. With a
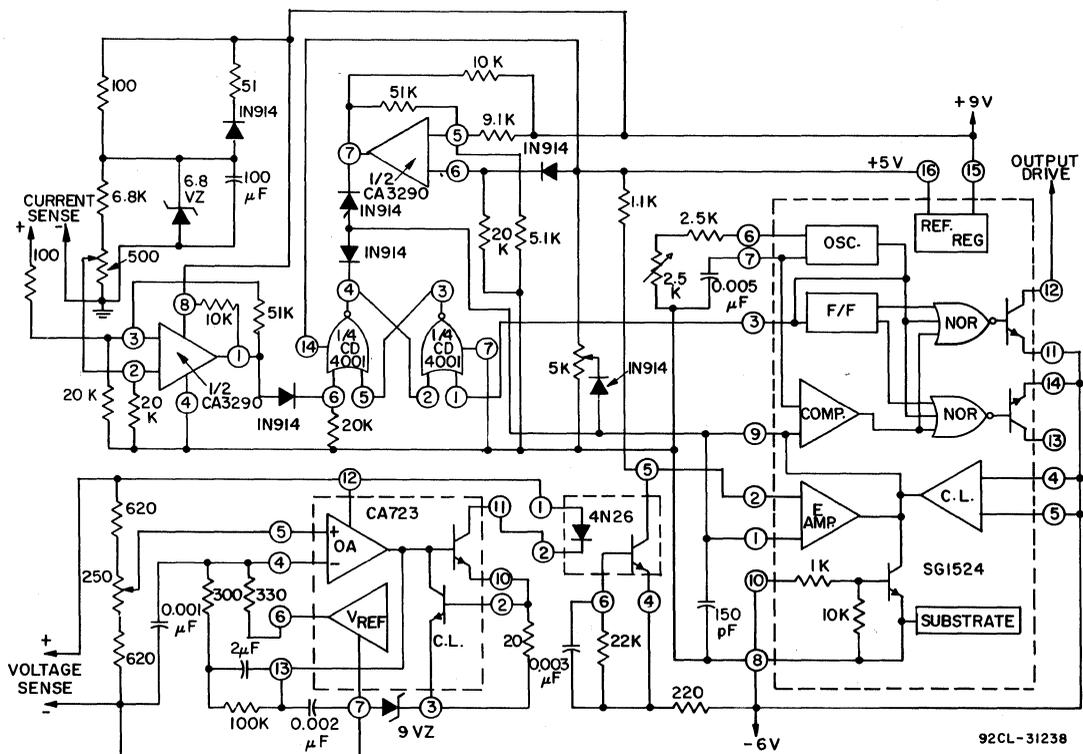
Fig. 159 - Schematic diagram of oscillator and pulse-width modulator circuit.

lower-voltage supply, the necessary operating voltage can be obtained with the aid of an extra rectifier-capacitor combination, directly from the secondary of the high-frequency transformer.

Auxiliary Functions—In addition to the following seven basic voltage-regulating functions:

1. Reference-Voltage Source
2. Error Amplifier
3. Photocoupler Isolator
4. Voltage Follower
5. Ramp Generator
6. Comparator
7. Logic Output

the power converter also provides the following:

8. Minimum Duty Factor Control to assure complete discharge of snubber network.
9. Maximum Duty Factor Control
10. "Soft-Start" and Low Line-Voltage Lockout
11. Pulse-by-Pulse Current Limiting

Functions 8 through 11 are discussed in more detail below.

Minimum Duty Factor—The minimum duty factor, D(min) is established by the emitter resistor in the 4N26 photocoupler; this resistor clamps the minimum voltage to the pulse-width modulator. For the snubber to operate effectively, the time at each operating point (switch on or switch off) must be sufficiently long so that the capacitor reaches equilibrium. Therefore, a minimum on time, DT, must be established for each cycle of at least t_{rise} plus five times the snubber RC product. In the circuit being considered, RC=50 x 0.002 x 10^{-6}=0.1 μs. Hence, a 1-microsecond minimum on time is adequate. The emitter resistor selected, 220 ohms, yields a minimum DT of approximately 2.5 microseconds, which provides ample margin.

Maximum Duty Factor—The maximum duty factor control must limit D(max) to less than 0.5, allowing for delays and storage in the remainder of the system, to assure that the transformer is demagnetized during the off time.

The maximum duty factor is set by adjusting the tap on a 5-kilohm potentiometer so that the maximum voltage that can appear at the comparator rail (terminal 9 on the pulse-width modulator) is limited. In the circuit being discussed, the potentiometer is set for a maximum on-pulse width of 10 microseconds

at no load with sensing disconnected for 40-kHz operation.

"Soft-Start" and Low Line-Voltage Lockout—Safe operation of pulse-width modulator supplies requires that the drive circuits and main load power be sequenced on and off in the proper order as the power supply, connected across the power mains, is turned on or off. If this condition is not complied with, severe stresses will be placed on the switching transistor, and device failure may result. An effective way to provide proper sequencing is to use a "soft start" (defined in statement 2, below), and a low-voltage lockout circuit. The objectives of the lockout circuit are to:

1. Apply drive to the power devices only after:
   a. The oscillator is running at the proper frequency, 40 kHz.
   b. Voltages for the base drive system are at full operating values.
   c. The initial line-surge phase of the 60-Hz rectifier filter is complete.
2. Apply base drive in a "soft-start" fashion; i.e., start with minimum pulse width, but full base current, then slowly increase the pulse width to its full controlled value of 10 microseconds.
3. In the event of low line voltage, shut off the base drive pulse before deterioration of the base drive current occurs. Low base current causes partial switching of the power device and operation outside the safe operating area.
4. Upon restoration of proper line voltage, restore the supply to operation in the soft-start mode.

Pulse-by-Pulse Current Limiting—Pulse-by-pulse current limiting in the primary rather than dc-load side-current limiting was chosen as the limiting technique in the forward converter circuit for several reasons.

1. Current surges into the output capacitors at start-up are eliminated.
2. There is no problem with load-to-line isolation.
3. Damage control is simplified. Shorted rectifiers, shorted transformer or choke turns, transformer saturation, and excess load conditions can be sensed. The circuit can operate in an impaired condition without producing additional damage, thus simplifying service procedures.

A 0.03-ohm resistor is in series with the emitter of the 2N6673. The emitter-current

sensing voltage produced is applied to terminal 3, the non-inverting input of the second half of the CA3290 dual comparator. An adjustable reference voltage is applied to terminal 2. When the voltage at terminal 3 exceeds the reference on terminal 2, the output at terminal 1 goes high and triggers the CD4001 flip-flop which, in turn, crowbars the comparator rail (terminal 9) of the pulse-width modulator IC, and the drive pulse is terminated. At the start of the next half cycle, the flip-flop is reset by the clock pulse from terminal 3 of the pulse-width-modulator IC.

Note that the snap action of the comparator is assured by the positive feedback obtained through the 51-kilohm resistor connected between terminals 1 and 3 of the CA3290. This feedback eliminates any ambiguities in sensing.

Summary

This converter could be redesigned to handle 400 watts or more by using a second output unit (driver, output device and transformer) operating from the now unused phase of the SG1524 pulse-width modulator, or by substituting a 2N6675 in the output, making slight changes in the base drive resistance and using a larger output rectifier.

Again, as previously stated, this does not describe a finished commercial item. Rather it serves as a demonstration of switching-device/circuit-format capability. Only the full-time power-supply designer can envision all of the environments and contingencies that will be the ultimate determinants of the design of a finished product.

340-WATT, 20-KHZ FLYBACK CONVERTER

The power-switching capability of the RCA-2N6676 SwitchMax power transistor is demonstrated in the following high-power flyback converter. The circuit provides 340 watts of output power at 20 kHz when operated from a 110-volt ac power line. The resultant overall efficiency was determined to range from 82 to 86 percent for inputs of 150 to 190 volts dc to the converter stage.

Converter Circuit Description

The converter circuit, shown in Fig. 160 in block diagram form, is powered by a direct input from a 110-volt ac power line; this input is rectified by a full-wave bridge to provide a dc output. This dc source, which is filtered by a capacitor, serves as the power supply for the RCA-2N6676 power switch. The circuit also contains a driver stage which provides sufficient gain to allow interfacing between suitable low-power pulse-width-controlled modulator logic circuitry and the input of the high-level transistor switch. The reverse-bias $(-I_{b2})$ current amplifier provides reverse-bias current essential for rapid turn-off of the power switch. Overvoltage and overcurrent protection circuitry is also provided. The driver stage, reverse-bias amplifier, and protection circuit are discussed in this section together with the flyback output stage. The pulse-width control function, indicated by dashed lines in Fig. 160, is not discussed; adequate material is available to show the implementation of necessary logic-function designs.
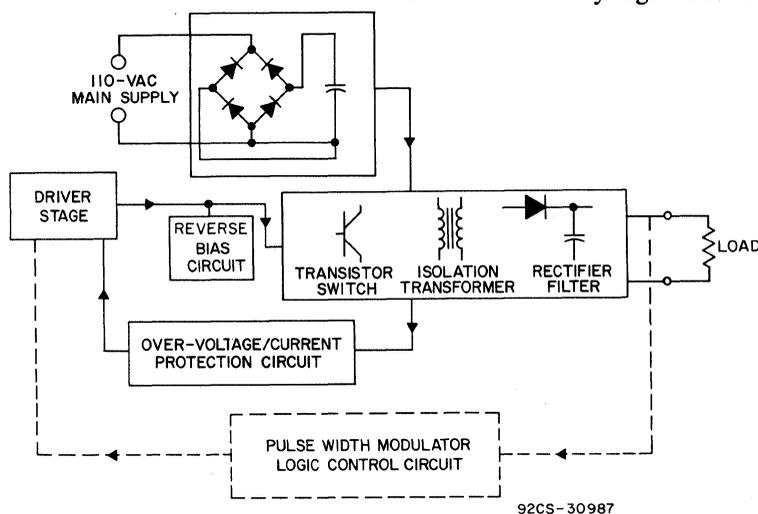
Fig. 160 - Block diagram of the converter circuit.

Output Stage

The flyback-type converter is generally not considered a high-power generator for three main reasons:

1. It requires approximately twice the peak current of a square-wave type.
2. It requires a larger output transformer as a result of the large magnitude of the dc current flowing and the need for a large air gap to avoid core saturation.
3. It requires, at low output voltage (5 to 12 volts), very large and expensive capacitors to obtain good ripple-voltage reduction.

However, the flyback converter does have several attractive features which make it worthy of consideration for applications requiring a high-power output:

1. Simplicity and low cost.
2. Provision for isolation of the secondary load from the main-line input voltage.
3. Suitability for multiple output supplies.
4. Suitability for medium-to-high levels of secondary voltages.

Fig. 161(a) shows a typical basic flyback-converter circuit that uses a single transistor as the switching device. The transistor is driven with a positive rectangular input pulse of controllable width and constant period. In this circuit, when the base control or drive pulse turns the transistor on, a current (I_p) builds up in the primary winding (which serves as a choke) of transformer T_1, as shown in Fig. 161(b). The secondary winding of the transformer is phased so that diode D_1 blocks the flow of secondary current at this time. The primary or collector current I_p rises linearly, provided the winding series resistance is low, to a final value determined by the primary winding inductance, L_p, the supply voltage, V_{CC}, and the turn-on duration, t_{on}, of the transistor. The transistor is considered to be inductively loaded. Energy is stored in the primary winding during the on time of the transistor; the maximum amount of energy stored must be sufficient to support the secondary load requirements. This energy is released into the secondary side after the transistor is turned off; the secondary current flows through diode D_1 into filter capacitor C_0 and the load R_0.

In the practical flyback circuit shown in Fig. 162, the output circuit employs an RCA-2N6676 power transistor (Q_4) as the power switch. The 110-volt ac power-line voltage is rectified and applied to the collector of the
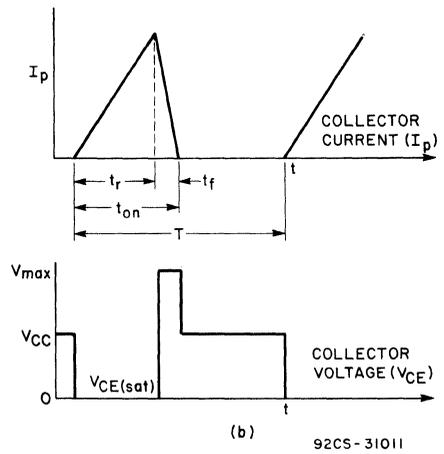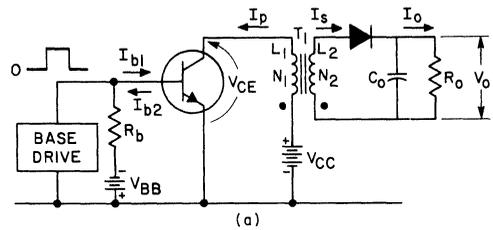
Fig. 161 - Basic flyback converter circuit and primary circuit waveforms.

power transistor through the primary winding of transformer T_1. The primary inductance L_p of the transformer is determined by the maximum allowable peak collector current, $I_c(pk)$, the minimum dc input voltage (low ac line voltage), and the maximum width of the turn-on pulse at low line voltage. Generally the secondary load requirements together with the rectifier and transformer losses dictate the final value of the peak collector current. The peak collector current in the design shown was determined by the following conditions:

Operating Junction Temperature (T_j)	100°C
Operating Case Temperature (T_c)	50°C
$V_{CE}(sat)$ at T_j=100°C	2 Volts
Operating Frequency (f)	20 kHz
Duty Cycle	50%
Inductive Turn-Off Time (t_c)	0.8 μs
Maximum Collector Voltage, $V_{CE}(sus)$	450 V
Thermal Resistance, θ_{JC}	1°C/W
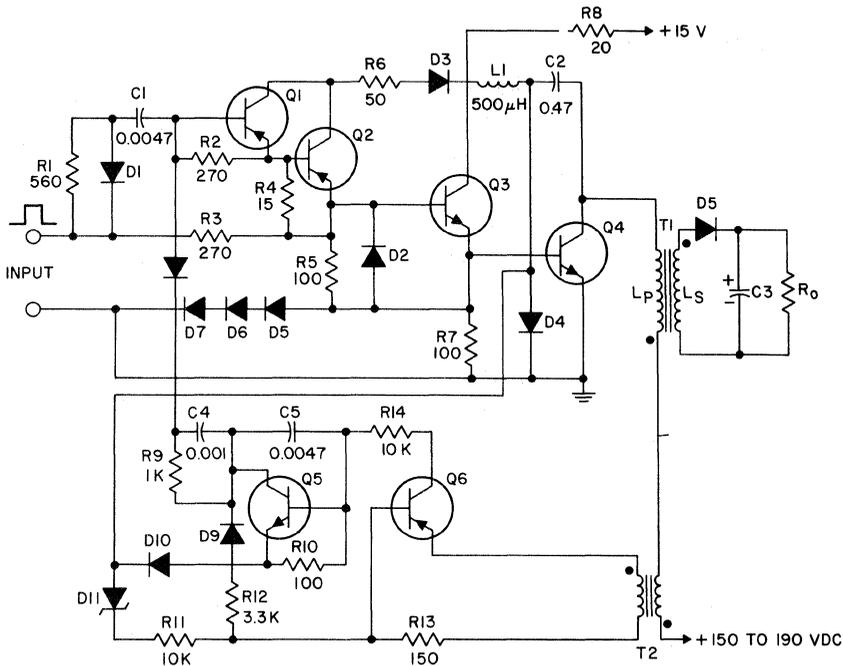
Q1,Q6 = 2N5416 ; DI = IN914
Q2 = 2N6213 ; D2,D3,D4 = A28D
Q3 = 2N3878 OR 2N5038 ; D5,D6,D7= INI206
Q4 = 2N6676 D8 ⎫
Q5 = 2N3439 D9 ⎬ = IN4937
          DIO ⎭
DII= 400 V ZENER

T_1 = CORE : SIEMENS E CORE SET (N27)
AIR GAP : 0.04 INCH
PRIMARY : 29 TURNS,30/36 LITZ
SECONDARY : IO TURNS, 30/36 LITZ
(SANDWICHED LAYERS I PRI./2 SEC./I PRI.)

T_2 = CORE FORM : 3/8 INCH OD, LENGTH 1.5 INCHES
PRIMARY : L_P = 2μH, WIRE SIZE No. 20
SECONDARY : L_S = 2μH WIRE SIZE No. 20

92CL-30996

Fig. 162 - Practical flyback converter circuit.

FLYBACK CONVERTER
RCA 2N6676
T_J =100°C; θ_{JC} = 1°C/W, t_c = 0.8 μs
DUTY CYCLE = 0.5
$V_{CE(sat)}$ = 2 V AT 100°C
$V_{CE(max)}$ = 450 V

$$I_{C(pk)} = \frac{(T_J - T_C)/\theta_{JC}}{\frac{1}{2}\left(\frac{t_{on}}{T}\right)V_{CE(sat)}\left[1+\left(\frac{t_c}{t_{on}}\right)\frac{V_{CE(max)}}{V_{CE(sat)}}\right]}$$

92CS-31010
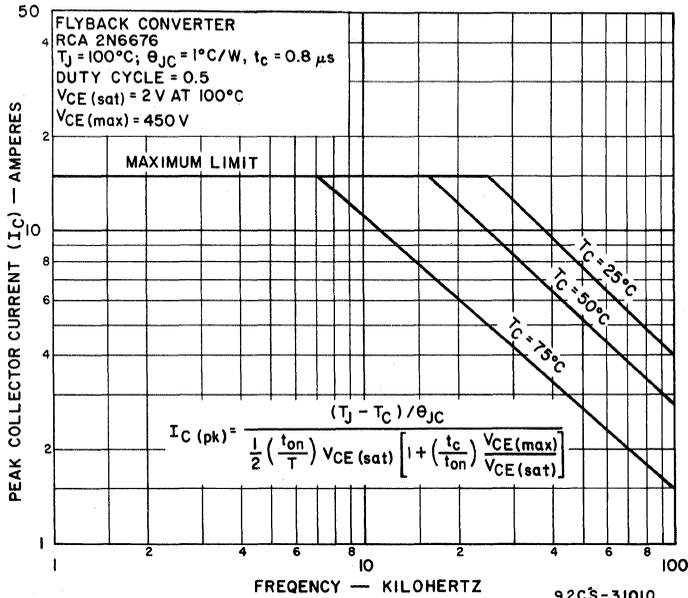
Fig. 163 - Peak collector current of the RCA-2N6676 as a function of frequency for three different case temperatures.

Fig. 163 shows a plot of the peak collector current of the RCA-2N6676 as a function of frequency for three different case temperatures. At a case temperature of 50°C, the peak collector current must be limited to 12 amperes. The flyback converter shown in Fig. 162 was designed to operate with a 20-kHz pulse-width modulated input drive signal and to provide a dc output of 48 volts with more than 300 watts of continuous output power.

An equally important part of the flyback converter is the output transformer, T_1. The switching converter works by cyclically storing energy in the primary winding, L_p, and then dumping this stored energy into the load, which is connected to the secondary side of the transformer. The design of the output transformer is important not only because it affects the amount of output power and efficiency of the converter, but also because it determines the operating frequency range.

Switching Characteristics

The turn-on time of the RCA-2N6676 transistor for a given peak collector current is a function of the duration of the base turn-on drive current. Although the turn-off time is related to the amplitude of the negative base-current drive, particularly with regard to storage-time reduction, the actual turn-off time in the flyback circuit is determined by the characteristics of the 2N6676 transistor and the output transformer. However, the application of sufficient reverse base current minimizes the effects of the transistor turn-off time on the overall turn-off characteristics of the circuit. Fig. 164 shows the base current

and voltage waveforms during maximum output-load conditions. The base-current turn-on pulse has a peak value of 0.75 amperes. A peak reverse base current of 1 ampere is obtained with a negative base-to-emitter voltage of 12 volts.

The base-to-emitter junction can be operated into the avalanche region during the reverse-bias condition. The result is an enhancement in turn-off time with no immediate observable degradation in junction characteristics. This result is attributed to the low level of reverse-bias energy present during the reverse base current conduction time, (approximately 1.5 microseconds); the reverse-bias energy in the base-to-emitter junction is approximately 18 microjoules.

Performance

Typical collector current and voltage waveforms for the 2N6676 transistor are shown in Fig. 165(a); transformer secondary current and voltage waveforms at maximum output

I_C(PRIMARY)
5 A/div   0-

V_C(PRIMARY)
100 V/div

0-

10 μs/div
(a)   92CS-30991

I (SECONDARY)
10 A/div

0-

V (SECONDARY)
50 V/div

0-

10 μs/div
(b)   92CS-30990
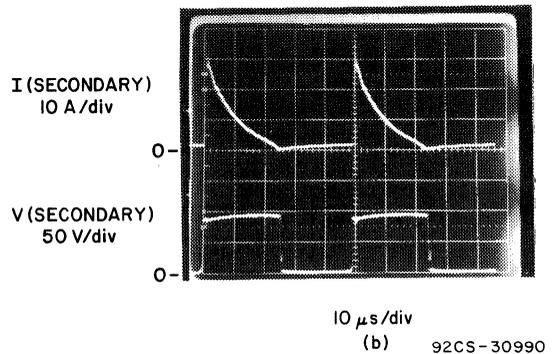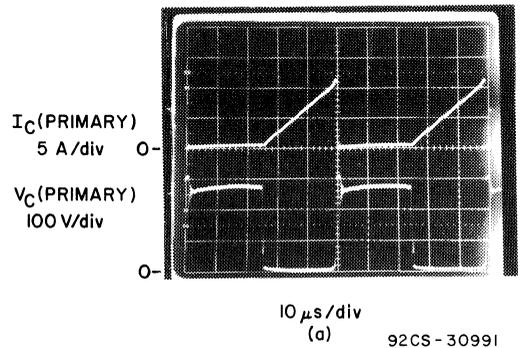
Fig. 165 - (a) Collector current and voltage (primary) for the RCA-2N6676 and (b) transformer secondary current and voltage at V_{CC}=150 V_{dc}, t=50 μs, t_{on}=25 μs, V_O=48 V_{dc}, I_O=7.2 A.

0-
I(base)
0.5 A/div

V (base) 0-
5 V/div

10 μs/div
92CS-30988

Fig. 164 - Base characteristics for the RCA-2N6676 at V_{CC}=+150 V_{dc}, t=50 μs, t_{on}(collector)=25 μs.

I_C(PRIMARY)
5 A/div

V_C(PRIMARY)
100V/div

10 μs/div
(a)

92CS-30992

I (SECONDARY)

V (SECONDARY)

10 μs/div
(b)

92CS-30993
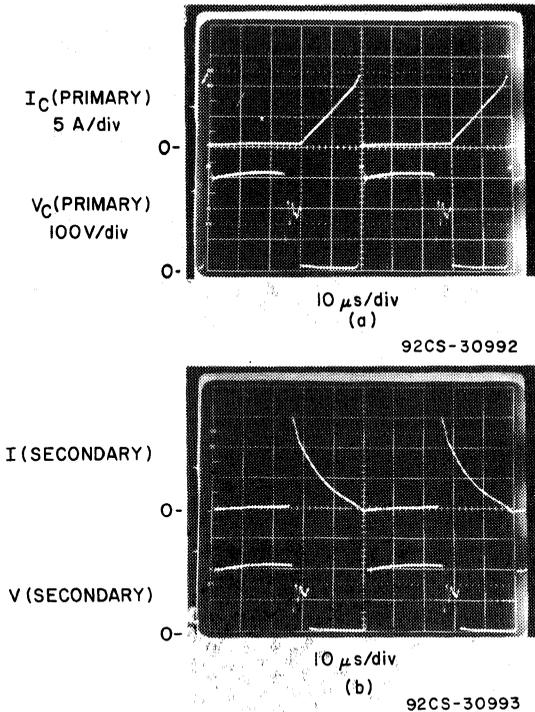
Fig. 166 - (a) Collector current and voltage for the RCA-2N6676, and (b) transformer secondary current and voltage at V_{CC}=190 V_{dc}, t=50 μs, t_{on}=19 μs, V_O=48 V_{dc}, I_O=7.2 A.

I_C(PRIMARY)
2 A/div
(a)

V_C(PRIMARY)
50 V/div

100 ns/div

92CS-30994
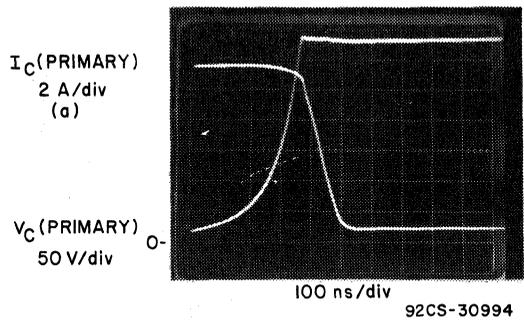
Fig. 167 - Turn-off characteristics for the RCA-2N6676 at V_{CC}=190 V_{dc}, t=50 μs, t_{on}=19 μs, V_O=48 V_{dc}, I_O=7.2 A.

power are shown in Fig. 165(b). The maximum output power of 345 watts was measured with a dc input of 150 volts and a turn-on pulse width of 25 microseconds at a frequency of 20 kHz.

Fig. 166 shows the performance of the flyback circuit at high line voltage, a V_{CC} of 190 volts. In order to limit the peak collector current to 10.8 amperes, the turn-on pulse width was reduced to 19 microseconds. The peak secondary current and voltage waveforms shown in Fig. 166 are identical to those shown in Fig. 165, indicating that this flyback converter design provides constant output power.
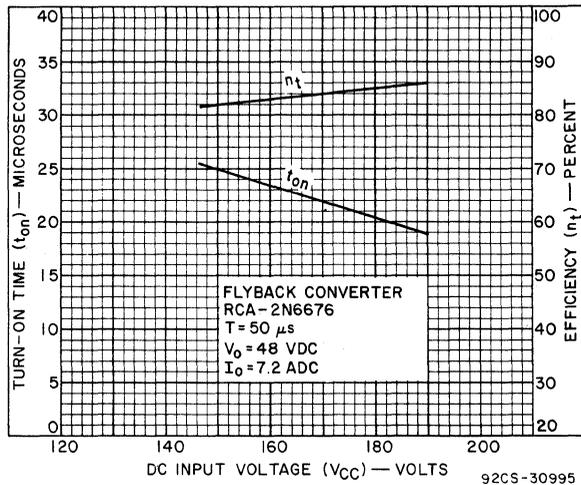
Fig. 168 - Overall efficiency of the RCA-2N6676 flyback converter stage (upper curve); efficiency with reduction of turn-on pulse width and increasing line voltage (lower curve).

Fig. 167 shows the turn-off characteristics of the 2N6676 transistor output stage at high line voltage, 190 volts, and reduced turn-on pulse width. The turn-off time interval, approximately 400 nanoseconds, was also reduced, indicating a reduction in turn-off dissipation in the transistor. The upper curve in Fig. 168 shows the overall efficiency of the RCA-2N6676 flyback converter stage; the efficiency ranges from 82 to 85.5 percent. The reduction of the turn-on pulse width with increasing line voltage results in high operating efficiency, as shown in the lower curve of Fig. 168.

Driver Stage

The driver stage of the converter, Q3, shown in Fig. 162, utilizes an RCA-2N5038 or 2N3878 transistor in an emitter-follower circuit configuration. The driver stage is operated from a separate 15-volt dc supply which is obtained from a line to a low-voltage transformer. The driver stage provides sufficient current gain to allow interfacing between suitable low-power pulse-width-controlled modulator logic circuitry and the input of the high-level transistor power switch. The driver stage serves as an impedance matching transformer as well as a current amplifier. In order to provide 750 milliamperes of base drive to the output power switch, the driver stage requires approximately 30 milliamperes of input base current.

Reverse-Bias Amplifier

The reverse-bias current, $-I_{b2}$, for power switch Q4 is provided by a current amplifier consisting of transistors Q_1 (RCA-2N5416) and Q_2 (RCA-2N6213). Because the reverse-bias circuit is somewhat uncommon, its operation is discussed in detail. The source of energy used to turn off power switch Q_4 is stored in capacitor C_2. During collector-current turn-off, the voltage developed across capacitor C_2 is equal to the clamped flyback voltage across Q_4; this voltage is limited to 400 volts. The voltage at the diode (D_4) end of C_2 becomes a negative value equal to the peak inverse or flyback voltage when the output transistor Q_4 turns on. This negative voltage cannot be used directly as a source for $-I_{b2}$ since the peak flyback voltage (which is converted to zero volts at the D_4 end of C_2) occurs as I_c just starts to fall. To be effective, this negative voltage must be present during

the entire I_c fall time (as it would be in a purely resistive circuit). Inductor L_1 is used in series with R_6, C_2, and the $-I_{b2}$ switching transistors Q_1 and Q_2 to maintain the required negative potential.

The reverse-bias current switch Q_1, Q_2 is turned on by the charge on C_1 at the end of the input, or oscillator, pulse, at which time the voltage at C_2 is -400 volts. The functions of L_1 are:

1. To reduce the source voltage at R_6 during conduction of $-I_{b2}$, thereby reducing dissipation in R_6.
2. To reduce the influence of the flyback voltage, which would tend to nullify $-I_{b2}$ at this time since the voltage at C_2 is zero.
3. To provide a ramping negative voltage across R_6, which, in turn, creates an increasing $-I_{b2}$ during the fall time of the collector current of Q_4 (a condition that tends to eliminate tailing). The end result is an output device, Q_4, that experiences minimum dissipation because of a fast turn-off time.

As an added benefit of this circuit, capacitor C_2 provides snubbing action. This benefit occurs because the charge that is dissipated by the reverse-bias current circuit must be replaced by the sustaining voltage, $V_{CE}(sus)$, of the output device, Q_4. The reverse-bias current drain represents the resistance part of the RC network connected across the collector and emitter of output transistor Q_4. The network acts as an inhibitor, at about 400 volts, on the operating range of the inverter.

Protection Circuitry

The protection circuit for the converter consists of transistors Q_5 and Q_6 and operates under the following conditions: short circuit, open circuit, 50-percent duty cycle exceeded, and high line voltage. Open-circuit and high line voltage conditions are detected simply by monitoring the flyback peak voltage across the output transistor, since both of these conditions manifest themselves as an excessive voltage across the device, a voltage that would ultimately destroy the device. The clamping action of C_2 is not a rigid clamping action and, as a result, the peak V_{CEX} varies somewhat with line voltage and loading conditions. The maximum safe V_{CEX} was chosen as 400 volts.

The selection of R_6 and L_1 determines both the value of $-I_{b2}$ and the voltage level at which C_2 effectively clamps. When the V_{CEX} of the

output device exceeds 400 volts, as it would during high line-voltage or open-circuit conditions, Q_6 turns on by conduction of the 400-volt zener diode D_{11}. Since the voltage at the diode end of C_2 becomes negative when Q_4 turns on, the level being determined by the peak positive voltage across the output transistor, Fig. 165, the zener diode will fire the protection circuit on the next conduction cycle after the peak voltage exceeds 400 volts. Even during a sudden open-circuit condition, this voltage cannot change instantaneously (because of the presence of C_2) and will take several cycles to rise above 400 volts. When Q_6 turns on, the base of Q_5 is effectively tied to the line voltage through R_{14}, while its emitter is at -400 volts. This arrangement provides about 40 milliamperes of base drive to Q_5, and turns it on. Part of the collector current of Q_5 is fed back to Q_6. This current maintains both Q_5 and Q_6 in a latched-on condition until the line voltage is switched off.

Short circuit and over-50-percent duty-cycle conditions are detected by inserting a small air-core transformer, T_2, in series with the primary winding of the output transformer. Observation of the primary current waveform, Fig. 165(a), shows that, under normal conditions, the collector current of Q_4 ramps up gradually from a zero current level. Under conditions of over 50-percent duty cycle, abnormally high current demands, or a short circuit, the waveform changes. All of the above conditions cause the same change in varying degrees, that is, a step up from the zero current level before the ramp starts. This step occurs, because, in all of the above conditions, the secondary current continues to flow even after the start of the next cycle.

The connection of the current-sensing transformer to Q_5 provides for a starting pulse to the Q_5,Q_6 switch whenever there is an appreciable step in current in the positive direction. There is always a very large step in the negative direction as a result of the fall time of the collector current in the output transistor, Q_4. This negative step is bypassed around Q_6 by D_9.

A 450-WATT, 40-KHZ, 240-VAC TO 5-VDC, FORWARD CONVERTER

The principles and virtues of the forward-converter circuit are well known, and this type of circuit has been advocated for some time. Until recently, however, a main drawback to

its use in high-power and high-frequency power supplies has been the lack of high-voltage power transistors with fast enough rise and fall times. Development of RCA's SwitchMax transistor family makes possible the design of a single forward converter of 450 watts output that can operate from nominal mains of 240 volts ac and a 40-kHz switching frequency.

A block diagram of such a converter is shown in Fig. 169.

Performance Considerations

Some of the advantages and disadvantages of the forward-converter circuit are:

Advantages:
1. Superficially a simple circuit.
2. No transformer balance problem.
3. Problem of unequal storage time (t_s) eliminated.
4. "Switch-through" problem avoided.

Disadvantages:
1. Transistor repetitive peak voltages may exceed 750 volts at high line, limiting choice of devices having suitable switching speeds.
2. Short duty factor ($<.5$) mandates a higher value energy-storage choke than that needed for a push-pull circuit.
3. Transformer requires a bifilar tertiary winding for commutation of magnetizing energy.
4. Primary leakage inductance of the transformer cannot be commutated so must be snubbed.
5. Because a single forward converter is a half-wave system, the peak current on the transistor is twice what it would be in a full-wave circuit of similar power.
6. Total duty factor (D) of power switch must not exceed 50%.

Fundamental to all switching supplies is the requirement of load-to-line isolation. The method by which this isolation is accomplished affects the subsequent design of the base drive system and whether it will be transformer or direct coupled.

The low saturation resistance of the type 2N6751 (V_{CE}(sat) typically less than 0.5 V at I_C=5 A, I_B=1 A) permits the effective use of the Baker (antisaturation) clamp technique to reduce the storage time of the power switch. A two-diode-drop level shift is sufficient to put the transistor into the active region, thus reducing the worst-case, high-temperature
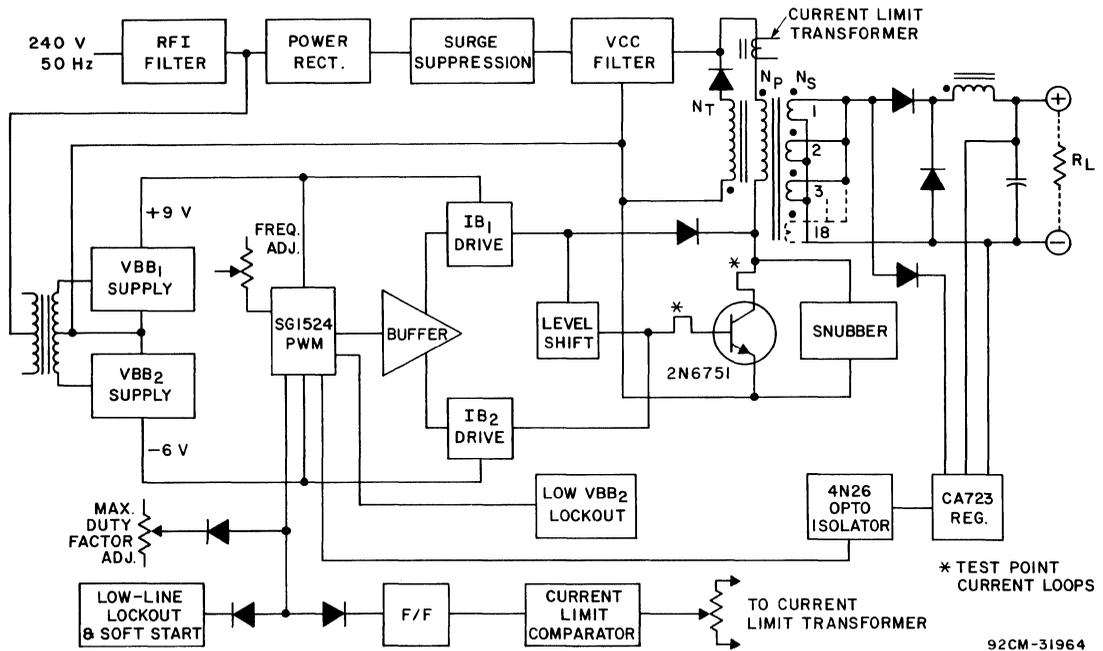
Fig. 169 - Block diagram of the converter.

storage time to less than 1.5 microseconds and lowering the fall time to 50 to 70% of its saturated switching-speed value.

Dead Time

Since the forward converter is a single-ended design, the simultaneous conduction problem that can occur with push-pull, half-bridge or bridge circuit formats does not exist. **However**, the total duty factor must **not** exceed 50%. Violation of this constraint will result in eventual transformer saturation and system failure. The need for the provision of a brief and controlled storage time becomes apparent. This storage time, together with a setting of the maximum duty factor control on the pulse-width modulator for D=0.4, provides a worst-case on time, including a 1.5-microsecond t_s, of about 11.5 microseconds with a 1-microsecond safety margin.

Transformer Limitations

One of the limitations of the forward converter is the portion of the on time (DT) consumed by the current rise time in the switching transistor and dominated by the referred leakage inductance of the transformer secondary. This limitation restricts the energy per cycle that can be transferred to the load side of the system at low line. The inductance of concern is that measured across the primary with the secondary shorted and the tertiary winding **open** (L_e). The power transfer is the product of the energy per cycle (W_c) times frequency (f).

$$W_c = \int_0^{DT} V_{CC}\, i_C\, dt$$

where:

$$D = \text{duty factor, } T = \frac{1}{f}$$

$$i_C = I_C(\text{max}) \left(1 - \varepsilon^{\frac{-t}{\tau}} \right)$$

$$\tau = \frac{L_e}{R_L} = \begin{array}{l}\text{secondary leakage induc-}\\ \text{tance referred to primary}\\ \text{at } V_{CC}(\text{low line})/I_C(\text{max}).\end{array}$$

Combining the above yields:

$$P_{transfer} = f \times V_{CC}(\text{min})$$

$$\times I_C(\text{max}) \int_0^{DT} \left(1 - e^{\frac{-R_L t}{L_e}} \right) dt$$

If $DT > 3\tau$ (which it must be for efficient operation) the equation integrates to $P_{transfer} = 1/T \times V_{CC}(\text{min}) \times I_C(\text{max})$

$$\times (DT - \frac{L_e}{R_L}).$$

Inserting into the simplified equation the values of V_{CC}(low line)=240 volts

I_C(max)=5 A

D x T=11.5 μs

$R_L=V_C/I_C$=48 ohms

L_e typical=40 μH

The value of $P_{transfer}$ would be:

$$P_{transfer}=1/25 \times 240 \times 5 \times (11.5-40/48)=512 \text{ watts}$$

The value of L_e in the final transformer design was 16 microhenries. Reevaluating the equation with this value yields $P_{transfer}$=536 watts, a substantial improvement. The reader can anticipate the effect on power transfer of increasing the operating frequency to 80 kHz, for example.

Snubbing and Turn-Off Dissipation

To restrain voltage overshoots on the power switching device at turn-off, it is necessary to add capacitance between the collector and emitter to absorb the energy of the uncommutated leakage inductance of the primary (L_{p1}).

Current Limiting

To protect the power switching transistor from the load faults that may occur at the output of a power supply, collector current limiting is essential. To be effective, the delay time through the entire current control loop must be minimal and the base drive must keep its integrity to pulse widths narrower than those necessary for normal voltage regulation.

Antisaturation clamping relieves the worst part of the forward-loop delay problem by holding the power-device storage time (t_s) to less than 1.5 microseconds.

Overcurrent may be sensed by using a current-sensing toroid on the primary lead of the power transformer. This technique has several benefits:

1. The toroid is so located that it senses only the referred secondary currents and ignores the excess base-current contribution.
2. The comparator circuit is isolated from the high voltages and high currents that may occur with a power-switching failure.

As previously mentioned, the forward-converter circuit places very high repetitive peak voltages (in excess of 700 volts) on the switching transistor, clamp diode, snubber, capacitor, and transformer windings. Should power requirements be such as to require the paralleling of forward-converter circuits, a half-bridge circuit might be more economical and produce lower stresses with a wider choice of transistors.

900-WATT, OFF-THE-LINE, HALF-BRIDGE CONVERTER

The performance of two RCA-2N6678 'SwitchMax' high-speed power transistors (15 A, 450 V (V_{CEX})) is demonstrated in the following 900-watt, half-bridge converter.

The circuit switches at a 20-kilohertz rate and with minimal alterations can operate from either 120 or 240 volts. It was built using conventional circuitry but in a non-compact modular format so that it would be easily accessible for instrumentation connections and component or design alteration. The power switches used are the RCA-2N6678 'SwitchMax' 15-ampere [I_{CE}(sat)], 450-volt (V_{CEX}) high-speed transistors.

Because the purpose of this effort was not to develop an optimum design but to permit experimentation with and analysis of high-speed transistor switching operation, a 10-volt/100-ampere output capability was selected rather than the more common 5-volt/200-ampere range. This choice permitted the use of simple magnetic components and fast-recovery rectifiers, rather than Schottky devices, without the hazard of rectifier damage in the event of lost regulation. It also permitted easier dummy-load manipulation.

The half-bridge circuit was chosen because of the following advantages:

1. Requires a simple transformer primary having a single winding.
2. System leakage inductance is commutable, allowing minimum snubber design and lower dissipation.
3. Adaptable to either 120- or 240-volt operation.
4. Permits easy maintenance of B-H symmetry in transformer core without exotic circuits or excessive air gaps.
5. Modulation and drive circuits are easily protected from the consequences of a power stage failure.
6. Needs only two 2N6678 'SwitchMax' transistors for almost a kilowatt of output.

The disadvantages encountered with the selection of the half-bridge circuit include:

1. Difficulties in making voltage versus current measurements because the primary section has no identifiable ground plane.
2. Difficulty in providing solid turn-off drive

power at short duty factors.

3. Tendency to cross-switch at high power levels because of large displacement currents in the device mica-heat sink region and sharp L di/dt voltages.

These disadvantages, however, were found to be manageable.

System Configuration

A block diagram of a half-bridge converter is shown in Fig. 170. The system is made up of three major building blocks:

I. **Power Block**. This block encompasses the 60-Hz power rectifiers, filters, power switching devices, commutating diodes and snubbers, 20-kilohertz 8-to-1 step-down transformer, rectifier, and filter elements.

II. **Oscillator-Modulator Block**. This block comprises the oscillator for the pulse-width modulator, modulator IC, soft-start, low-line lock-out comparator, pulse-by-pulse current limiter, and the predriver IC's.

III. **Base Driver Block**. This block provides on and off drive to the power switches.

System Performance

The over-all performance of the 900-watt half-bridge rectifier system is given in Table X. The line and load regulation figures though

Table X - Performance of 900-Watt Converter System

Output Voltage (nominal)—V_O=10 volts
Output Current (nominal)—I_O=90 amperes

Line Regulation at V_O=10 V, I_O=50 A, V_{LINE}=120 rms:
    −0.7% at V_{LINE}=105 V rms
    +0.5% at V_{LINE}=135 V rms

Load Regulation at V_O=10 V, I_O=50 A, V_{LINE}=110 V rms:
    +1% at 10 A to −0.6% at 80 A
    Current limit at 90 A

Hum (see Fig. 171) at 120 Hz=100 mV peak to peak
Ripple (See Fig. 172) at 20 kHz=50 mV peak to peak
RF Noise (see Fig. 172) at 5 MHz=0.5 V peak to peak
Efficiency=69 to 73% (conventional watt-meter readings)

92CM-31080
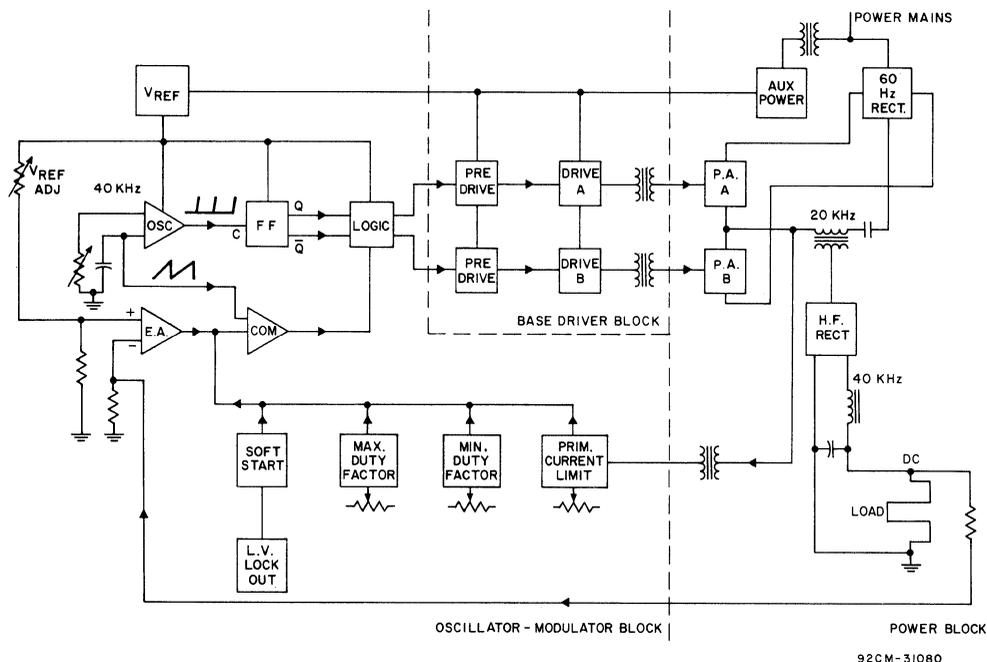
Fig. 170 - Block diagram of half-bridge driven converter. Note the three major sections: Power Block, Oscillator-Modulator Block, and Base Driver Block.

satisfactory are not outstanding and could be improved by a higher dc open-loop gain. Such improvement, however, is not likely in the present configuration.

The hum performance, less than 100 millivolts on a 10-volt output, is respectable (see Fig. 171) and is comparable to the accepted industry standard of 50 millivolts on a 5-volt output. Some additional design effort on the error amplifier and a less conservative roll-off characteristic could bring about a two to one improvement.

I_L = 90 A
t = 5 ms/DIV.
V = 0.1 V AC/DIV.

92CS-31072
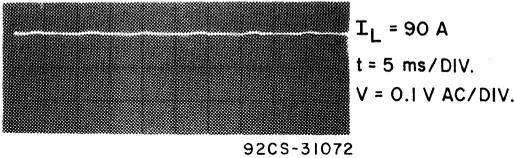
Fig. 171 - Hum performance of 900-watt converter system.

As shown in Fig. 172, the ripple at 20 kilohertz is also low, less than 50 millivolts peak to peak on a 10-volt output. High-frequency ripple is almost entirely dependent on the quality of the final filter capacitor (C13 in Fig. 173).

I_L = 90 A
t = 10 μs/DIV.
V = 0.1 V AC/DIV.

92CS-31073
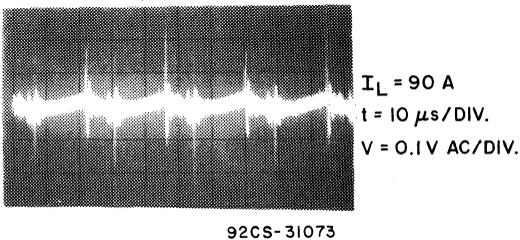
Fig. 172 - Ripple performance of 900-watt converter system. Note rf noise during rectifier transitions.

The elimination of rf noise presents a major problem. The noise, see Fig. 172, is caused by the transition of the high-current rectifiers and is extremely difficult to filter or shield. The appearance of this noise in a magnified oscilloscope display is that of several different high-frequency damped oscillations excited by the same voltage or current shock. This problem is further complicated by the confusion of grounding systems between the isotransformer, and associated instrumentation, as well as the radio-frequency inter-

ference radiating from the long leads of the breadboard system.

The efficiency of the supply, depending on load and based on conventional wattmeter readings, is 69 to 73 per cent. A 100-watt discrepancy, however, was noted between the wattmeter measurements and the total of the subsystem calculated losses. A summary of the calculated losses at the 900-watt level with 120-volt line is given in Table XI. The total power loss is 251 watts and the calculated efficiency, therefore, is a more reasonable 78 per cent. Determination of true efficiency would require the use of a 300-volt dc supply in place of the 60-Hz mains, rectifier, and ac wattmeter.

Table XI - Power Losses Calculated by Subsystem

Subsystem	Power Loss (W)
Auxiliary Supply Pass Regulator	20
Base Driver System	25
Power Switches	50
Output Rectifier	100
High-Frequency Transformer	10
60-Hz Rectifier	10
Snubbers	10
Output Chokes	6
60-Hz Bleeder Resistors	20
Total	251
Calculated efficiency=251/(251+900)=78%	

Power Block Operation Analysis

The schematic diagram and parts list for the power-block portion of the 900-watt half-wave bridge converter are given in Fig. 173. For discussion purposes, this block is divided into ten sections:

A. 60-Hz Rectifier and Filter
B. High-Frequency Power Transformer
C. Coupling Capacitor
D. Commutating Diodes
E. Snubber Network
F. Power Switches
G. Base-Input Networks
H. Output Rectifiers and LC Filter
I. Current-Sense Transformer
J. Auxiliary Power Supply

A. **60-Hz Rectifier and Filter.** This section, which could also operate on 50 Hz, is conventional. It provides the option of switch-

C1,C2	=4500 pF, 250 V, electrolytic
C3	=1100 μF, 25 V, electrolytic
C4	=100 pF, ceramic
C5	=2 μF, 25 V, electrolytic
C6	=10 μF, 25 V, electrolytic
C7	=0.05 μF, 100 V, ceramic or paper
C8	=4 capacitors in parallel, each 2 μF, 200 V, paper
C9,C10	=3 capacitors in parallel, each 0.001 pF, 600 V, Mylar or metal film
C11,C12	=0.68 μF, 200 V, Mylar or metal film
C13	=6 capacitors in parallel, each 1600 μF, 50 V, low ESR electrolytics (Sangamo 301JP162 U050B or equivalent)
C14,C15	=0.01 μF, 1 kV, ceramic
C17,C18	=0.005 μF, 1 kV, ceramic
C19,C20	=0.5 μF, 600 V, paper or Mylar
D1,D2 **D3,D4**	=20 A/300 V, DO5 rectifier, 1N1195A or equivalent
D5,D6	=6 A/50 V, DO4 rectifier, 1N1341B or equivalent
D7,D8	=18 A/600 V, fast-recovery rectifier, D2412M or equivalent
D9,D10	=1 A, fast-recovery diode, 1N4933 or equivalent
D11 through D18	=fast-recovery diode, 1N3910 or equivalent
F1,F2	=8 A/250 V fuse

IC1	=CA3085, voltage rectifier
L1	=9 μH, 2 18-μH inductors in parallel
Q11	=2N6649, p-n-p Darlington, TO-3
Q12,Q13	=2N6678, power transistor
R1	=2.5 ohms (cold); 0.045 ohms (hot) Rodan surge guard SG-7
R2	=0.12 ohms, 2 W
R3	=10 kilohms, potentiometer
R4	=820 ohms, 1/2 W
R5,R6	=3500 ohms, 10 W, wire wound
R7,R8	=50 ohms, 12 W, made up of 6 300-ohm 2-W resistors in parallel
R9,R10	=4 ohms, 3 W, made up of 3 12-ohm 1-W resistors in parallel
R11,R12	=1.5 ohms, 10 W, non-inductive
R13,R19	=10 ohms, 2 W
R14,R15	=10 ohms, 1 W
R16	=1 ohm, 1/2 W
R17,R18	=20 ohms, 1/2 W
T1	=115 V, 28 V, 2 A, center tapped (Signal Transformer 241-7-28 or equivalent)
T4	=Cores — pair IR8113 "E", Indiana Secondaries — 4 each 3-1/2 turns of 0.020" x 0.75" copper strap Primary — wound on secondaries, 28 turns 6 strands of #21 enameled wire
T5	=1000 turns #32 wire on a pair of linear ferrite E cores about 3/8" x 3/8"; cross section non-critical. See text.

Fig. 173 - Schematic diagram and parts list for Power Block portion of 900-watt converter.

ing from a bridge for 230-volt operation to a doubler for 115-volt operation. The capacitors and rectifiers are oversize to provide the extended range of operating conditions desired for this study. Minimal surge limiting is provided by a surge-limiting resistor having a negative temperature coefficient. A commercial power supply would require a sturdier arrangement plus an RFI filter.

B. **High-Frequency Power Transformer**. The high-frequency power transformer T4 uses a pair of Indiana General IR8113 E cores. The secondaries have four windings, each 3½ turns of copper strap 0.75 inch wide by 0.020 inch thick. The 3½ turns allow the common point for all windings to terminate on the same side of the bobbin for ease of connection to the negative bus. The primary is 28 turns of 6 strands of No. 21 enameled wire twisted two turns per inch and wound on top of the secondary. Three-mil Mylar drafting film provides the interlayer insulation. Each secondary winding has a 0.01-μF/10-ohm damper network across it at the rectifiers to reduce self-resonance ringing. A five-mil insulated copper-foil Faraday shield between the primary and secondary windings is grounded to the output common and chassis to reduce coupling between windings. The double secondary made of 0.75-inch strap was required by the core dimension to provide the copper cross section needed to keep I^2R losses below nine watts.

C. **Coupling Capacitor**. The power transformer coupling capacitor C8 is designed to preserve the B-H symmetry in the half-bridge circuit. However closely components are matched to preserve drive symmetry to the switching transistors, differences in heat sinking, the switching temperature coefficient, transient load changes, or unsymmetrical rectification can cause offset of the transformer-core B-H curve. As a result, the transformer may draw abnormal current on one half of its cycle and, in turn, charge the coupling capacitor to a higher voltage than normal. When the cycle reverses, the higher capacitor voltage adds to the $V_{CC}/2$ being applied to the other switch, thus providing extra voltage across the transformer winding in such a direction as to recenter the B-H characteristic.

Selection of the proper value for this capacitor requires some analysis. The lower limit of the capacitor value can be determined by recognizing a series resonant circuit formed

by the capacitor and the referred value of the filter choke $L=(N_P/N_S)^2 L_F$. The resonant frequency must be less than half of the switching frequency and for charging to be linear it should be less than one fourth of it. The circuit of Fig. 173 uses a filter inductance of 9 microhenries (two 18 microhenry chokes in parallel) and a switching frequency of 20 kilohertz. Allowing for a high dc current and temperature, the effective value of the inductance is estimated as 6 microhenries. With this value for L_F and a resonant frequency of 5 kilohertz, a value for the coupling capacitor C can be determined as follows:

$$f = \frac{1}{2\pi \sqrt{LC}} \qquad L = (N_p/N_S)^2 L_F$$

$$C = \frac{1}{4\pi^2 f^2 (N_p/N_S)^2 L_F}$$

$$C = \frac{1}{4\pi^2 \times 25 \times 10^6 \times 8^2 \times 6 \times 10^{-6}}$$

$$= 2.6 \, \mu F$$

This value of 2.6 μF is a reasonable one.

The charging voltages on the coupling capacitor should be considered next. With an average current of 10 amperes for 20 microseconds, the capacitor would charge to a value given by:

$$V = \frac{I}{C} \times dt$$

$$V = \frac{10 \times 20 \times 10^{-6}}{2.6 \times 10^{-6}}$$

$$= 77 \text{ volts}$$

This value of 77 volts is excessive and would interfere with regulation at low line voltages. A more reasonable value would be 30 volts or 10 per cent of the nominal V_{CC} (20 per cent of $V_{CC}/2$). With this value for V

$$C = I \frac{dt}{dv} = \frac{10 \times 20 \times 10^{-6}}{30}$$

$$= 6.67 \, \mu F$$

Based on this calculation, a value of 8 μF was selected for the coupling capacitor C8. Although a voltage rating of 50 volts would be adequate theoretically, 200-volt units were used for safety purposes. To minimize heating, four 2-μF 200-volt paper capacitors in parallel were used. The effect of this capacitor is illustrated in Fig. 174, which shows the droop
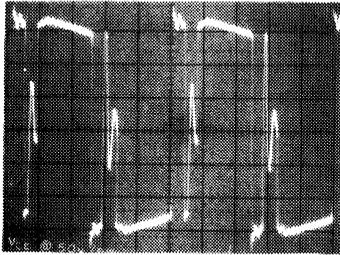
$I_L = 90$ A

$t = 10\ \mu s/DIV.$

$V_{CE} = 50$ V/DIV.

92CS-31071

*Fig. 174 - Waveform of transformer pri-
mary voltage. Note tilt in wave-
form caused by compensating
effect of coupling capacitor.*

in transformer voltage at high ampere-second products.

D. **Commutating Diodes**. The commutating diodes (D7 and D8) are standard, fast-recovery, 12-ampere, 450-volt rectifiers D2412M connected as close as possible to their companion transistor switches (Q12 and Q13). In a half-bridge circuit, the commutating diodes do more than steer leakage inductance energy back to the main supply. In the event of a sudden off-load, or a backfeed, the drastic increase in transformer flux can drive the collector of the conducting transistor negative with respect to its emitter, forcing the device into "inverse conduction". The commutating diode then bypasses the switch until the collector again goes positive, thus preventing a high-stress situation.

E. **Snubber Network**. The snubber network limits the $L_1 di/dt$ voltage excursion produced by the interruption of the current flow in the transformer and absorbs the energy in the leakage inductance. In contrast, the commutating diode does not absorb the inductive

energy, but transfers it back to the main power source. A feature of the half-bridge circuit is that most of the leakage and wiring inductance can be commutated. This feature allows the use of smaller, lower-dissipation snubbers than would be needed for forward or push-pull inverters of comparable power. Instead of absorbing the entire $L_1 I_p^2/2$ energy, the snubber needs only enough capacitance to hold the V_{CE} down to its limit value until the turn-on delay of the commutating diode is overcome. This turn-on delay is in the order of 50 to 100 nanoseconds depending on the diodes and wiring. The interplay between snubbers and commutating diodes can be clarified by a study of the simplified circuit of Fig. 175 and the corresponding waveforms in Fig. 176.

For additional information on Snubber Network Systems Design, refer to RCA Application Note AN-6743 "A 900-Watt Off-the-Line Half-Bridge Converter."

F. **Power Switching**. The power switching devices, 2N6678, are from the RCA "Switch-Max" power transistor family. They have been specially designed for high inductive-switching-locus capability (clamped $E_{S/b}$) up to 450 volts at 15 amperes and with a load inductance of 50 microhenries. They also provide excellent switching-speed performance at high temperature as well as at room ambient. All devices in this family are tested for these parameters at both 100° C and at 25° C. The circuit designer, therefore, can safely use these transistors to the full extent of their capabilities with assurance that no critical limit will be exceeded. As a result, maximum efficiency and cost effectiveness can be achieved in switching-circuit designs.
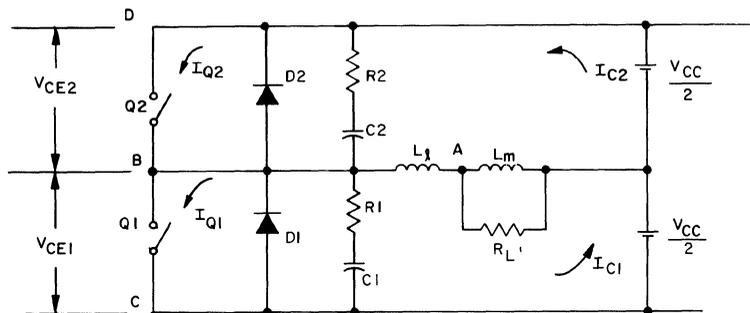
92CS-31061

*Fig. 175 - Simplified diagram of snubber
network system.*
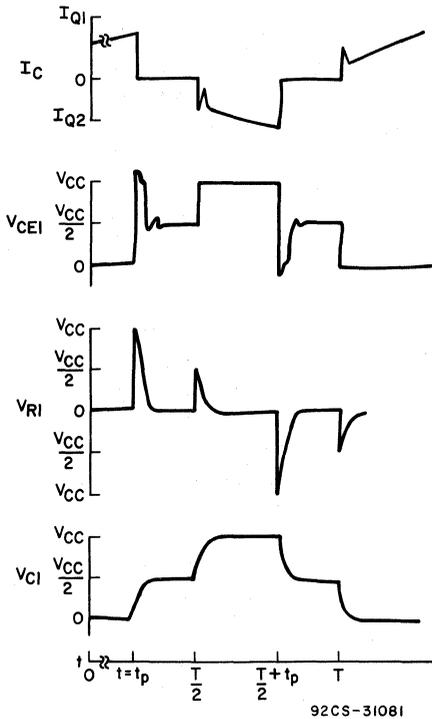
Fig. 176 - Waveforms in snubber net-work.

G. **Base-Input Network.** The base-input network conforms to standard practice with a 1.5-ohm current-limiting resistor and 0.68-μF speed-up capacitor to sharpen the base-current rise time and enhance the I_{B2}, V_{BB2} turn-off drive. A 4-ohm resistor is connected from base to emitter of each switching device to minimize the cross-switching problem previously mentioned.

H. **Output-Rectifiers and LC Filter.** The output rectifiers (D11-D18) are conventional 1N3910 fast-recovery types wired and mounted on heat sinks with their companion chokes. The chokes use Indiana General SR15002-1-245 pregapped E cores wound with 9 turns each of 0.75-by-0.020-inch copper strap giving a nominal inductance of 20 microhenries per choke. The strap ends were left long to facilitate low-ohmic connections to the recti-fiers and filter capacitors. The double filter chokes were used because the standard pre-gapped cores available were rated at only 50 amperes at the inductance selected. The chokes were designed for a minimum load current of 10 amperes.

The filter capacitor bank C13 consisted of six Sangamo 1600-pF/50-V tubular single-ended electrolytics (Cat.#301JP162U050B). This capacitor bank effectively keeps the 20-kilohertz ripple to less than 50 millivolts at all loads from 10 to 90 amperes. Calculations show that a capacitance of only 8000 μF is needed for good ripple control but a total of 9600 μF was used to be conservative. For stability tests, an additional 30,000 μF of capacitance was added to approximate worst-case loading.

I. **Current-Sensing Transformer.** The cur-rent-sensing transformer is placed on the primary side of the power transformer so that it will be responsive to core saturation as well as provide fast response to load faults. The secondary of the current-sensing transformer (T5) is 1000 turns of No. 32 wire on a pair of ferrite E cores having a ⅜″ by ⅜″ center leg. The primary is one turn of the wire to the power transformer wrapped over the sec-ondary. Terminated with 1100 ohms, T5 produces a faithful waveshape of about 1 volt/ampere.

J. **Auxiliary Power Supply.** This supply powers the pulse-width modulator and base drive circuits. It is a basic transformer, rectifier, series-pass regulator system. The only critical component is the high-quality transformer (T1) needed for the line-voltage range over which the inverter must work, 95 to 135 volts RMS. Economy transformers tend to overheat at high line conditions and cause regulation problems at low line.

Oscillator-Modulator Block
Operation Analysis

The circuit diagram of the complete Oscil-lator-Modulator Block is given in Fig. 177. This block uses the pulse-width modulator integrated circuit type 1524 combining on one chip a reference voltage source, a clock oscillator and ramp generator, a toggling flip-flop, separate A and B output buffers, an error operational amplifier, and a comparator. The shut-down clamp and the current-limit shut-down portions are not used in this application. Additional components provide the following functions.

1. Maximum Duty Factor Control—prevents common-mode conduction.
2. Minimum Duty Factor Control—prevents double pulsing in case of a sudden off-load, line surge, or back feed, and assures proper snubbing action.
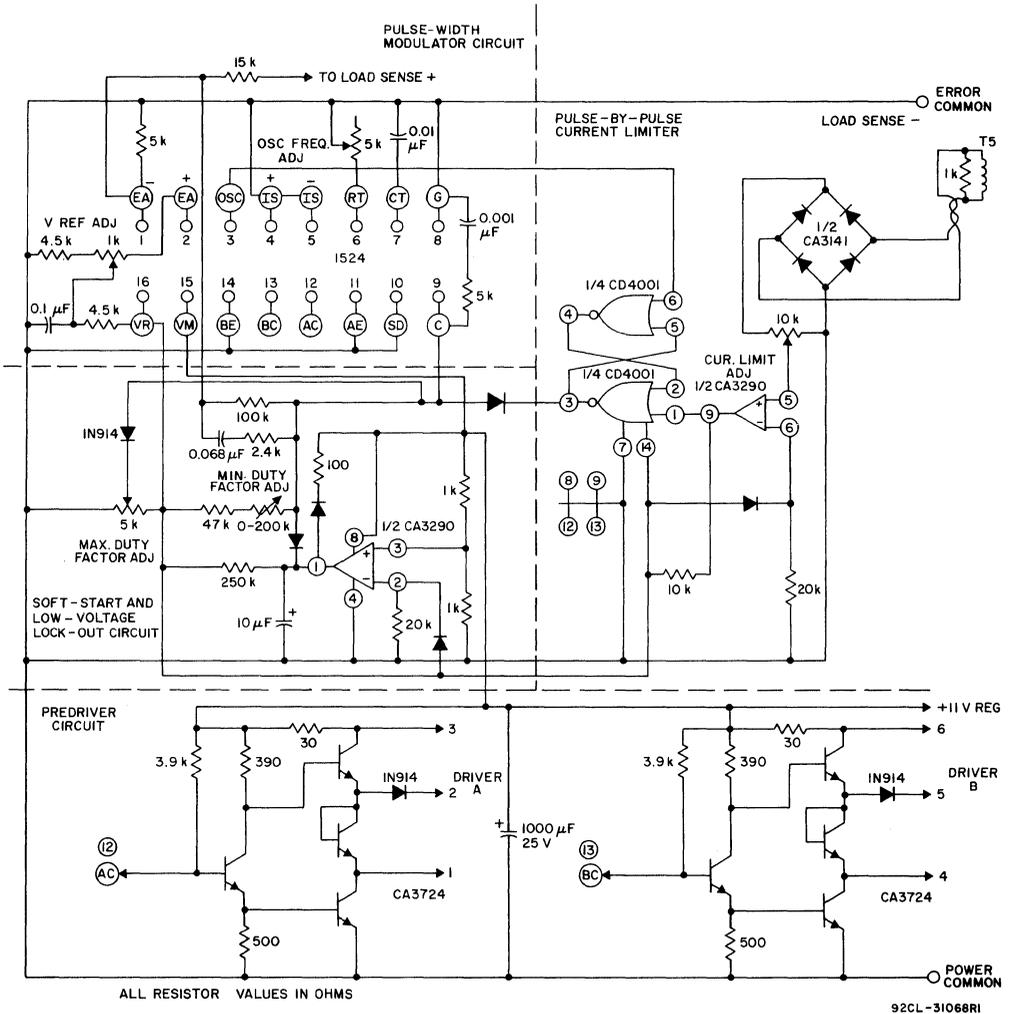
*Fig. 177 - Schematic diagram of Oscil-
lator-Modulator Block.*

3. Soft Start—with a fast reset, limits surge
   currents.
4. Low-Line Lock-Out—truncates the duty
   factor whenever the power line voltage
   drops below 100 volts RMS and shuts
   down the supply entirely at 85 volts.
5. Pulse-by-Pulse Current Limiter—term-
   inates the drive pulse in the event of
   overload or core saturation.

Pulse-Width Modulator Circuit. The opera-
tion of the pulse-width modulator circuit is
conventional except for the following:
1. Because the current-limiting and shut-
   down facilities are not used, terminals 4,
   5, and 10 are tied to common pin 8.
2. To maintain a minimum duty factor, a
   positive current is forced into the error

amplifier-comparator control rail from
the voltage reference source through the
47-kilohm and 200-kilohm adjustable
resistor. This current prevents the high-
impedance error amplifier from driving
the control rail all the way to zero and
provides a minimum 2.5-microsecond
width for the adjustable pulse to assure
that if there is a sudden off-load, back
feed, or power-line surge, the switching
devices continue to alternate their switch-
ing action until the output voltage regulates
downward, thus preventing the problem
called "double pulsing."

**Soft-Start and Low-Voltage-Lock-Out Cir-
cuit.** For the safe operation of the pulse-
width modulator supply-voltage circuits, the

drive circuits and the main power load must be sequenced on and off in the proper order as the power supply is turned on or off across the power mains. If not, severe stresses are placed on the switching transistors and can lead to device failure.

An effective way to provide these capabilities is to use a "soft-start" circuit having a fast reset and a low-voltage lockout provision. "Soft start" refers to the application of the base drive pulse to the switching transistors. It starts with a minimum pulse width but with full current and then slowly increases pulse width to its full controlled value. Such a circuit is shown in Fig. 178. This circuit

Fig. 178 - Soft-start low-voltage lock-out circuit.

assures that base-drive power is applied to the power switches only after the auxiliary power is up to its full regulated value (in this case 11 volts) and then, in a soft-start fashion, it minimizes start-up current surges. Conversely when power is removed from the system, either accidentally, deliberately, or because of brown-out conditions, the low-voltage lock-out truncates the duty factor over the range of 100 to 75 volts without lowering the base-drive current. Upon recovery of the main voltage, the soft-start circuit again takes control.

The soft-start low-voltage lock-out circuit operates as follows.

1. Upon application of power, the voltage at the 11-volt auxiliary regulator output increases and applies power to the 1524 pulse-width modulator circuit, producing a reference voltage of 5.2 volts at its pin 16. (See Fig. 177). This reference voltage is applied through a 1N914 coupling diode to the negative input, pin 2, of the CA3290 comparator and through a 250-kilohm resistor to the 10-microfarad soft-start capacitor. This capacitor is held low, thus holding the control bus, pin 9 of the 1524, low also.

2. The regulator auxiliary supply voltage connects through a voltage divider to the positive input, pin 3, of the CA3290 comparator.

3. When the voltage on comparator pin 3 exceeds that on pin 2, the output, pin 1, goes high and the 10-microfarad capacitor charges through the 250-kilohm resistor and allows the voltage on pin 9 of the 1524, to rise to that value called for by the error amplifier or the maximum duty factor control.

4. If the auxiliary voltage falls below its limit, the comparator goes low, draining the 10-microfarad capacitor and pulling down the control bus voltage, truncating the duty factor pulse, and finally shutting off the drive voltage. This circuit also has the effect of "degaussing" the power transformer during system turn-off.

5. When the equipment is switched off under normal conditions, the 100-ohm resistor and the diode quickly discharge the capacitor to reset it for the next turn-on.

Pulse-by-Pulse Current Limiter

The major hazards in the life of a power converter are core saturation and overload, both of which are heralded by excessive collector currents. Because the user cannot be expected to count every ampere of load on the output terminals, a current sensor placed in the primary side of the power transformer can recognize core saturation as well as provide fast response to load faults. Fig. 179 gives the schematic for the current-sensing technique used in this converter. The current-sensing transformer (T_5) was described as part of the Power Block. Its output waveform is shown in Fig. 180.

Base-Driver Block Operation Analysis

The Base-Driver Block provides the on and off drive to the power switches. It gets its input from the Oscillator-Modulator Block. A schematic of the drive system is given in Fig. 181. The pre-driver portion of the oscillator-modulator block is a conventional circuit and is also included in Fig. 181.

Fig. 179 - Pulse-by-pulse current-limiter circuit.

Fig. 180 - Waveform of current-sense transformer output voltage.

PERFORMANCE CONSIDERATIONS

Feedback Loop

Rigorous design requires that open-loop gain and phase-shift calculations be made to ascertain that the open-loop gain is reduced to unity (0 dB) before the 360-degree total phase shift is reached. The total open-loop gain is made up of five increments, as shown in Fig. 182. These increments are:

G_S = gain of the sensing circuit

G_A = gain of the error amplifier

G_P = gain of the pulse-width modulator and the power switch combination

G_T = gain of the high-frequency power transformer

G_F = gain of the filter network

The summing of $G_S+G_A+G_P+G_T+G_F$ and their related phase shifts shows the system to be stable but not optimized for best hum suppression.

The mechanics of phase-gain calculations

and the techniques of equipment measurements are well-documented in the current literature. Experience with this converter and similar projects indicates that the best reasonable calculations give only crude estimates and actual measurements of operating gain and the phase relations are essential for optimal design.

Power Losses in Power-Switching Transistors

The most essential element of power loss is the power dissipation during the fall time of the driver pulse. This dissipation ranges from $(V_{CE}(max) \times I_C \times t_f \times F)/6$ for the pure resistive and oversnubbed case to $V_{CE}(max) \times I_C(max) \times t_c \times f \times 0.4$ for the clamped inductive case. These dissipations span almost a three-to-one range. In operating equipment, both equations and anything in between are correct at one time or another. The reason is that if a simple RC snubber network is made from calculations based on the previously discussed criteria, it will be made for the highest collector current for which the equipment is designed. For lower currents, consequently, the equipment is oversnubbed. In other words, a voltage-current locus that is inductive at 13 or 15 amperes will be resistive at 3 to 4 amperes, if snubbing is properly in place. This transition from capacitive-to-resistive-to-inductive turn-off locus with change in output load is shown in Fig. 183.
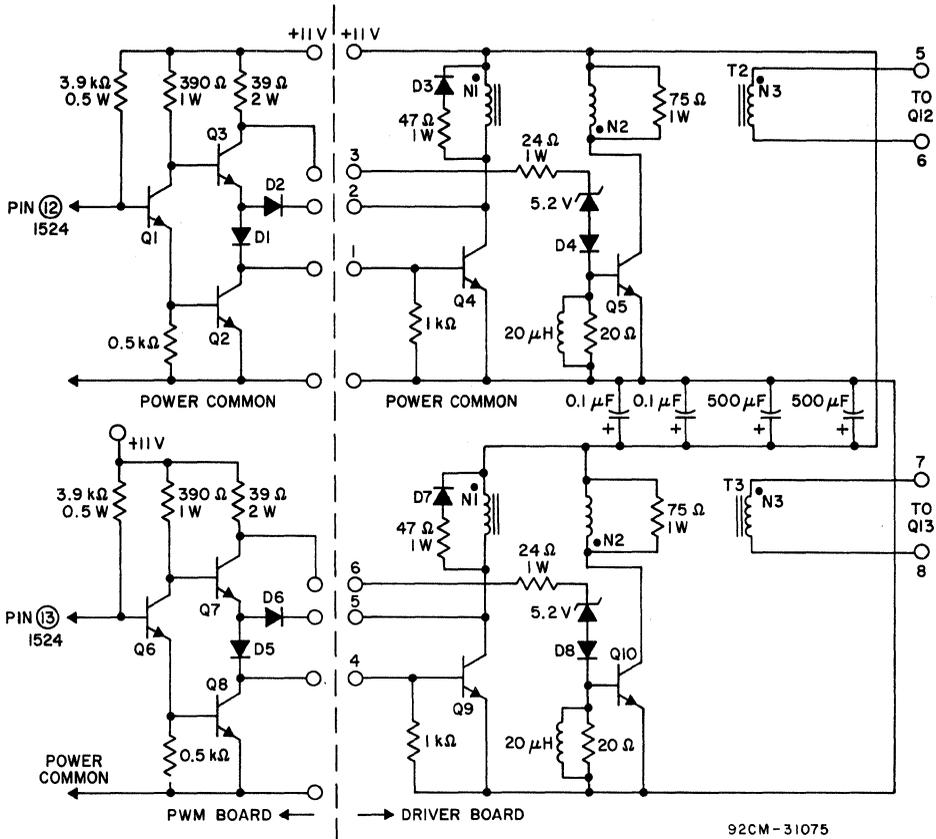
Fig. 181 - Schematic of Base-Driver
Block. Includes predriver stage
on pulse-width-modulator of
Oscillator-Modulator Block.
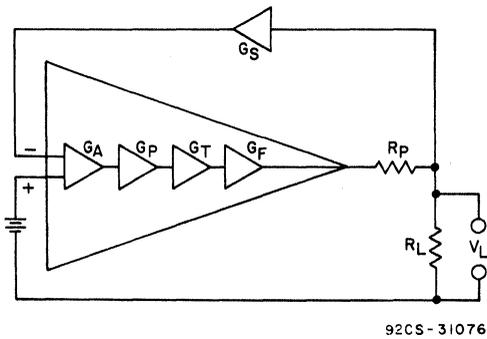
$V_L = A (V_R - V_L G_s) - I_L R_P$

$= A V_R - A V_L G_s - I_L R_P$

$$\frac{V_L}{V_R} = \frac{A - \dfrac{I_L R_P}{V_R}}{1 + A G_s}$$

where A = Vector system forward gain

$= G_A + G_P + G_T + G_F$

G_s = Vector gain of feedback network
R_P = Parasitic resistance of rectifier's wiring
V_R = Reference voltage

Fig. 182 - Feedback components in con-
verter.
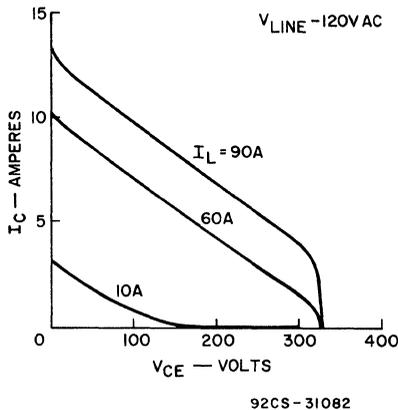
Fig. 183 - Collector current-voltage switching locus with change in output load.

Thermal Considerations

Because the converter was not intended as a commercial design the heatsinking is far from optimum. On each power transistor, a standard 1.8° C per watt heatsink is used to which its companion commutating diode is also mounted. At full load they reach a case temperature of about 60 to 70° C. The base-drive transistors are each mounted on small heatsinks of about three square inches on their circuit card. The eight output rectifiers are mounted on two 1.8° C per watt heatsinks (four on each) which get quite warm in operation. No forced ventilation is used.

The snubber network resistors reach about 70° C in operation. This dissipation burden, however, can be better distributed by partial snubbing at the transformer instead of doing the entire job at the transistor terminals. The heatsinking of the snubber networks was improved by soldering the leads of the six parallel 2-watt resistors to punched 10-mil copper straps connected at their tops to the cathode of their respective commutating diodes.

The auxiliary-supply pass transistor and rectifier diodes mount on a fifth 1.8° C per watt heat sink and are only comfortably warm.

Overload and Short-Circuit Protection

Overload and short-circuit protection are provided by the combined functions of soft start, low-line lock-out, pulse-by-pulse current limiting, and the capacitor-coupled transformer. With the system described, no failures were experienced as the result of turn-on at full load, stepped-load charge, load pull, shorted filter chokes, or turn-off with full load. A direct short was not tried.

1-KW, 20-KHZ, OFF-LINE DRIVEN CONVERTER

Driven converters offer certain advantages over free-running converter systems which depend on the magnetic properties of a transformer to control switching. The main advantages are: 1) stable operating frequency independent of load (the degree of stability is dependent on the clock circuit chosen); 2) a simplified transformer design because feedback windings are not required; and 3), lower cost of the ferrite material employed (the cost of linear ferrite cores is often less than half that of square-loop cores of comparable size). One major disadvantage of this converter-circuit approach, however, is a tendency for common-mode conduction. Common-mode conduction refers to a mode of circuit operation during which both devices of a push-pull pair conduct simultaneously. During this period, the net flux density within the transformer core is virtually nulled out, presenting, for all practical purposes, short-circuit load conditions to the transistors. Although the high currents which prevail during this mode tend to turn off the transistor which has completed its normal conduction period, the opposite device starting its on period experiences high voltage and high current at the same time. This could lead to second breakdown. Therefore, considerable care must be taken when designing the drive circuitry to prevent or at least minimize common-mode conduction during light- or no-load conditions.

The inverter employed for this application uses a small high-frequency output transformer to isolate the load from the ac line and from the system ground of the converter itself. Because of the high operating frequency of the inverter, low ripple dc can be obtained by using low-valued capacitor-filter components. To achieve the same low level of ripple, a linear power supply would require the use of a regulator circuit and a series pass transistor (or transistors) with high energy-handling capability.

Since the transistors in an inverter are operated in the switching mode, their required energy-handling capability is considerably less than those employed in a linear power supply of comparable power output.

The following paragraphs describe a 1-kilowatt driven converter that operates from a 117-volt ac line. The converter is designed to provide a dc output of 100 volts and deliver 1 kilowatt of continuous output power to the load with an overall system efficiency exceeding 85 percent. This performance is achieved through the use of type 40854 transistors selected from the 2N6250 power-transistor family.

The following discussion is limited to a review of the design and construction of the converter circuit only. In a complete system, overload sensing and some form of latching circuit must be added to protect the transistors and other vital components from an overload or short circuit at the output terminals.

CIRCUIT DESCRIPTION

The converter consists of four major sections as illustrated by the block diagram shown in Fig. 184. A complete schematic diagram of the converter circuit is shown in Fig. 185. All circuits are operated from a single high-voltage source and are stable over ac line-voltage variations between 105 and 130 volts. The oscillator, buffer, and driver circuits easily fit on a single 4½-inch by 5½-inch
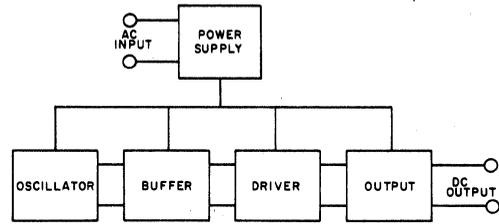
Fig. 184 - The four major converter sections.

circuit board. Additional filtering of the supply voltage for these stages keeps the ripple voltage below 500 millivolts during normal load conditions. Because all circuitry operates from a high dc potential, and because the speed-up capacitors employed in the base drive circuits for wave shaping charge up to this potential, diodes must be connected from base to ground of every transistor (with the exception of output transistors Q_7 and Q_8) to clamp the bases and prevent base-emitter junction breakdown during each transistor's respective off period. The effect of the clamping diode can be seen in the bottom waveform of Fig. 186.

PARTS LIST FOR THE CONVERTER CIRCUIT

PART No.	MFG TYPE No.	DATA SHEET FILE No.	DESCRIPTION
$Q_{1,2,3,4}$	RCA 2N3440	64	300V, 1A, 10W, TO-5
$Q_{5,6}$	RCA 2N6176	508	350V, 1A, 20W, TO-5 Plastic
$Q_{7,8}$	RCA 40854	498 (prototype File 523)	450V, 30A, 175W, TO-3
$D_{1,2,3,4,9,10,11,12,19,20}$	RCA 1N3195	41	600V, 750 mA, DO-26
$D_{5,6,13,14,15,16}$	RCA TA7894	*	600V, 1A, DO-26, fast recovery rectifier
$D_{7,8}$	TRW 1N4740	*	10V, 1W, zener diode
$D_{17,18}$	RCA TA7900	*	600V, 3A, modified DO-4, fast recovery rectifier
$D_{21,22,23,24}$	RCA TA7985	*	300V, 40A, DO-5, fast recovery rectifier
$D_{25,26,27,28}$	RCA 1N1195A	6	300V, 20A, DO-5

* – developmental data sheet

Fig. 185 - Complete schematic diagram of the converter circuit.

TOP: COLLECTOR
VOLTAGE OF Q₁ (V- 50V/DIV,
H-10μs/DIV), BOTTOM= BASE
VOLTAGE OF Q₄ (V-IV/DIV,
H-10 μs/DIV)
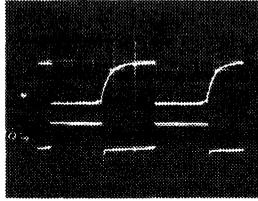
Fig. 186 - The effect of the clamping diodes and the wave shaping resulting from the presence of the buffer stage.

Oscillator

The clock signal is provided by a simple two-transistor (Q_1 and Q_2) multivibrator. The desired frequency of 20 kHz is stable to within ± 2-percent drift with dc supply voltage varying between 125 and 175 volts. Trimmer resistors R_2 and R_3 are used to adjust the oscillator frequency and duty cycle. Resistor R_3 is included to eliminate the need for matching circuit components.

Buffer

A buffer stage (Q_3, Q_4) between the oscillator and driver circuits provides the isolation required by the oscillator for stable operation independent of the load. The wave shaping resulting from this stage is evident in the waveforms shown in Fig. 186. The top waveform is the collector voltage of Q_1 (or Q_2). The bottom waveform is the voltage present at the base of the respective drive transistor Q_6 (or Q_5).

Driver

Common-mode conduction in the push-pull driver stage is minimized by delaying the base drive to transistors Q_5 and Q_6. The desired delay is obtained through the use of cross-coupling diodes D_5 and D_6. These diodes prevent the base drive from reaching the non-conducting driver while the other is still in the conducting state. The base drive is held back until the V_{CE} of the conducting driver, during its transition to the off state, exceeds the breakdown voltage of the zener diode (D_7 or D_8) connected to the base of the non-conducting driver. This technique provides a delay that varies proportionately with the storage time of the devices in the sockets, and thus eliminates the need for matching transistors.

Output

The severity of common-mode conduction in the output stage is several orders of magnitude greater than that encountered in the driver stage if no steps are taken to delay the base drive. During the time when common-mode conduction occurs, the current flowing through each device is limited only by the transistor's gain and the impedance of the collector-emitter circuit. As these currents and their conduction times increase, the possibility of the occurrence of secondary breakdown also increases. Even if the safe-operating-area of the transistors is not exceeded, the resulting high volt-ampere pulses can substantially increase the power dissipation and affect the overall efficiency of the system.

The waveforms shown in Fig. 187 illustrate
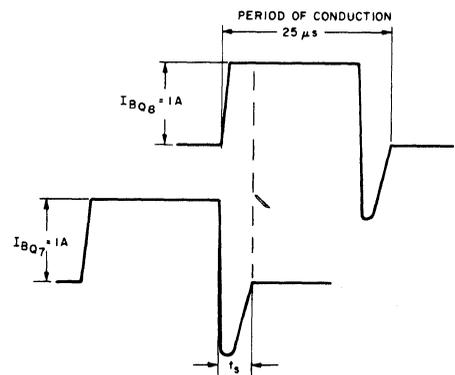
Fig. 187 - Form of base current to output transistors Q7 and Q8 without delay circuit.

what the base current to output transistors Q_7 and Q_8 would look like if no delay circuit were employed. If this drawing represented the actual operating condition of the output stage, common-mode conduction would occur during the storage time interval t_s. The amount of storage time is dependent on how hard the transistor is driven into saturation. Fig. 188 shows the reverse base-current waveform of one of the output devices under different load conditions with constant forward base drive. Comparison of the two waveforms shows almost a two to one increase in storage time when the converter is switched from a normal load state (1 kilowatt output) to an unloaded state.

A number of methods for obtaining the proper variable delay are available to the designer. The circuit approach shown in Fig.

RESERSE BASE
CURRENT WAVEFORM OF Q7
TOP = WITH 1KW LOAD
BOTTOM : WITH NO LOAD
V - I AMP/ DIV
H - 0.5 μs / DIV
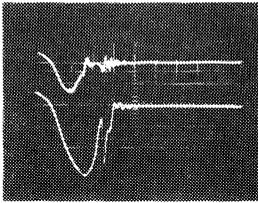
*Fig. 188 - The reverse base-current wave-
form of one of the output
devices under different load
conditions with constant for-
ward base drive.*

185 has been chosen because it is economical; it requires a minimum of parts. The same design philosophy used in the driver stage has been applied to the output stage. Cross-coupling diodes D_{13} and D_{14} are used to shunt drive current through the conducting transistor during the needed delay period. When the conducting transistor turns off, its collector-to-emitter voltage rises to twice the supply voltage. As soon as this voltage increases beyond the base threshold voltage, the conducting shunt diode becomes back biased, turns off, and permits current flow to the base of the non-conducting output transistor. The base threshold voltage is determined by the series base diodes (D_{17}, D_{18}), the transistor base-emitter diode, and the voltage dropped across the emitter resistor (R_{15}, R_{16}). The end result is a base current pulse whose width varies according to the delay dictated by the load and the switching characteristics of the output transistors being used. For any given load and supply voltage, higher peak collector currents are required to maintain a constant average current if the forward drive portion of the base pulse width becomes narrower.

Therefore, it is highly desirable to keep the needed delay to a minimum. Diodes D_{15} and D_{16} minimize delay by providing a low-impedance base return to ground during the reverse-bias portion of each cycle. This low-impedance return reduces transistor-switching storage time.

Although the emitter resistors account for only a small part of the base threshold voltage (voltage drop results from collector-to-emitter leakage current), the degeneration they provide contributes to the reliability of the output stage by suppressing transient current spikes and enhancing the thermal stability of the device.

Transformer Design Considerations

A description of the transformers employed in the converter is given in Table XII. Because of the high operating frequency, ferrite was chosen as the core material for both transformers to minimize core losses. Each transformer is designed for non-saturated operation at core temperatures up to 100°C and supply voltages as high as 185 volts. The primaries of both transformers are bifilar wound to assure symmetrical coupling to the secondaries. The number of primary turns was determined through the use of the following formula:

$$N_p = \frac{2 \, V_{cc} \times 10^8}{4 \, f \, A_c \, B}$$

where V_{cc} is dc supply voltage, f is frequency, A_c is core cross-sectional area, and B is flux density.

Utilization of No. 12 wire (based on 800 to 1000 cir. mils/amp. rms) for the output transformer was found to be impractical. Not only was it extremely difficult to wind, but several layers were required to obtain the

Table XII - Ferrite Transformer Description

Transformer	Primary	Secondary	Remarks
T_1	300 turns C.T. bifilar AWG No. 30	10 turns C.T. bifilar AWG No. 22	Ferroxcube pot core, No. 36/22, 3B7
T_2	60 turns C.T. bifilar AWG No. 18	20 turns bifilar AWG No. 16	Allen Bradley C core, (4 pieces) No. U2625C133A, WO-3, paralleled sets of primary and secondary windings

needed number of turns called for in the design. The parasitic winding capacitance and leakage inductance resulting from this poor physical design caused severe ringing and large voltage turn-off spikes at the collectors of Q_7 and Q_8. The ringing and voltage spikes were reduced considerably by paralleling duplicate pairs of the primary and the secondary windings from each set of C cores. This arrangement permitted the use of smaller-gauge wire to reduce the total number of layers and to get the windings closer to the core for better coupling. As a result, the transformer efficiency was improved, and a corresponding decrease in its operating temperature was obtained.

Performance Characteristics

The output performance characteristics of the converter are shown in Fig. 189. Fig.

189(a) shows the converter efficiency versus dc output power at the nominal ac line voltage. Fig. 189(b) shows the dc output power as a function of the ac input line voltage. The efficiency is computed by the use of the following formula:

$$\eta = \frac{\text{DC output power}}{\text{AC input power}} \times 100\% \text{ eff.}$$

The losses in efficiency are primarily attributed to power consumption within the semiconductor components. The bulk of this dissipation is due to switching and saturation voltage losses. Since saturated switching techniques are employed, the dominant dissipation factor results from the switching losses. To optimize efficiency, the designer should therefore select devices that offer the best switching characteristics without sacrificing so much safe-operating-area capability that the system becomes unreliable. Because this trade-off exists, the care that should be exercised in device selection cannot be over-emphasized.

Fig. 190 shows typical output collector

Fig. 189 - Output performance characteristics of the converter: (a) efficiency as a function of dc output power at the nominal ac line voltage; (b) dc output power as a function of the ac input line voltage.
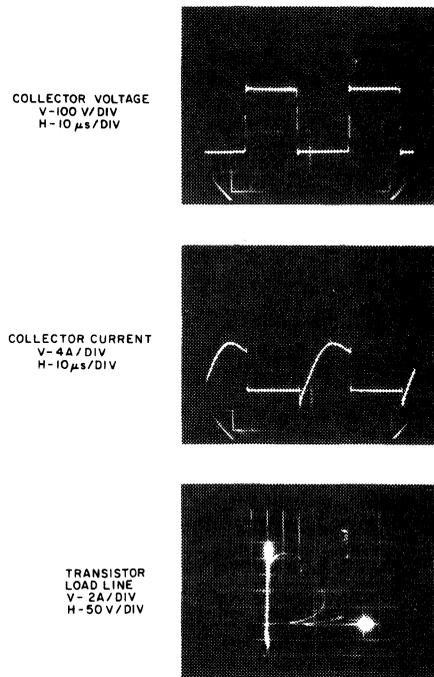

Fig. 190 - Typical output collector voltage, collector current, and load-line waveforms for a 1-kilowatt load at the nominal ac line voltage.

voltage, collector current, and load-line waveforms for a 1-kilowatt load at the nominal ac line voltage. By using these waveforms together with the published safe-operating-area curves and temperature-derating curves found in the transistor data sheet, the designer can determine if the transistor will operate safely and reliably in the circuit.

The bottom waveform in Fig. 191 shows a magnified view of the intensified portion of the fall-time region of the collector-voltage waveform shown in Fig. 190. The inflection seen in Fig. 191 results when simultaneous conduction of both halves of the output-diode bridge reflects an instantaneous short back to the primary side of T_2 and causes a momentary collapse of the collector voltage. This condition occurs during the diode reverse-recovery time and persists until all stored charge is depleted from the junction and the diode ceases conduction. The condition becomes readily apparent in a comparison of the two waveforms in Fig. 191 where the top waveform is the output diode current of one half of the bridge.

TOP: CURRENT
THROUGH DIODE D21
(V-4 AMP/DIV, H-0.5μs/DIV)
BOTTOM: COLLECTOR VOLTAGE
OF Q8 (V-100V/DIV, H-0.5μs/DIV
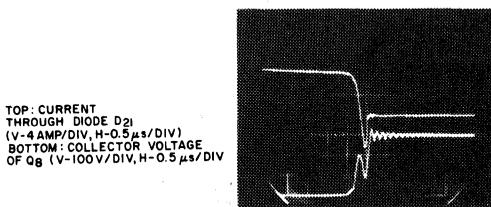
Fig. 191 - Waveforms showing current through diode D21 and collector voltage of Q8.

Efficiency/Cost Considerations

Some improvement in converter efficiency can be obtained by using two diodes instead of four for full-wave rectification of the output. This change can be readily accomplished by doubling the present number of secondary turns on T_2 and including a center tap for the ground return point. The elimination of a diode drop in the system described previously would represent a saving of 10 to 15 watts of power dissipation when the converter is delivering 1000 watts into a 10-ohm load. Since the forward diode voltage increases with current, the power dissipated by the rectifiers increases as the load-current demand increases. Although the number of secondary turns is doubled, dissipation within the transformer remains essentially unchanged because each

half of the secondary conducts for only 50 percent of the time. The size constraints imposed on a system may make it impossible for a designer to use this approach even though it could offer increased reliability and, possibly, lower system cost. Implementation of this change in the present design would require the use of a larger core and a redesign of the transformer.

Another point to be considered when attempting to optimize efficiency is wire lead length. Because the residual inductance of the leads has an adverse effect on transistor switching speeds, lead lengths should be kept as short as possible. The turn-on times of transistors Q_7 and Q_8 were improved by approximately 0.3 microsecond when the converter breadboard circuit was reassembled into the final form.

2-KILOWATT STEPPED SINE-WAVE INVERTER

The following pages describe the use of the 2N5578 power transistor in a 2-kilowatt, 60-Hz, 117-volt, stepped sine-wave inverter. Additional information is provided to permit conversion of the inverter to 50-Hz, 220-volt operation.

General Circuit Description and Operation

The inverter is frequency regulated, has a peak and average power capability equivalent to a 117-volt rms sine wave, operates from a 24-to-28-volt dc power source, and yields a maximum efficiency of 87 percent. The 2N5578 employed in the inverter is a high-current transistor that is ideally suited to switch up to 60 amperes in a common-emitter inverter configuration. In the following application 3.5 kilowatts of peak power are converted from a 24-to-28-volt dc bus at a frequency of 180 Hz.

The classical method for obtaining a 60-Hz, 117-volt power source from a dc bus is to use a single 60-Hz square-wave inverter. The disadvantages of this method are the large size and considerable weight of the resultant system and the fact that the waveform factor of a square wave does not have the same peak-to-rms voltage ratio as that of a conventional sine wave, a condition required for proper operation of various equipment and appliances. All of these disadvantages are overcome with the stepped approach.

The basic operation of the inverter can be described with the aid of the simplified circuit schematic diagram shown in Fig. 192. Power is taken from a dc supply and inverted into an ac-power square wave by a high-power transistor inverter employing six 2N5578 power transistors. The inverter operates at a frequency of 180 Hz while the output is stepped into a 60-Hz signal. The secondary winding of the inverter transformer is composed of two series-connected windings with different turns ratios, and two SCR's (silicon controlled rectifiers) attached in a bidirectional conduction configuration to the ends of each winding. The other side of each SCR is connected in common with one side of the load, R_L, while the opposite side of R_L is returned to the off-center tap of the secondary winding.

With the inverter in operation, the switching of the SCR's causes a stepped sine wave with the peak-to-average power ratio of a 117-volt ac rms sine wave to appear across R_L. Waveform A of Fig. 192 exists across the secondary winding while waveform B is present across R_L.

Circuit Description

As shown in the block diagram of Fig. 193, the inverter comprises six functions:

1. Low-Power Voltage Regulator: Provides a constant voltage of 10 volts to the low-power circuits for supply voltage variations from 24 to 28 volts dc.
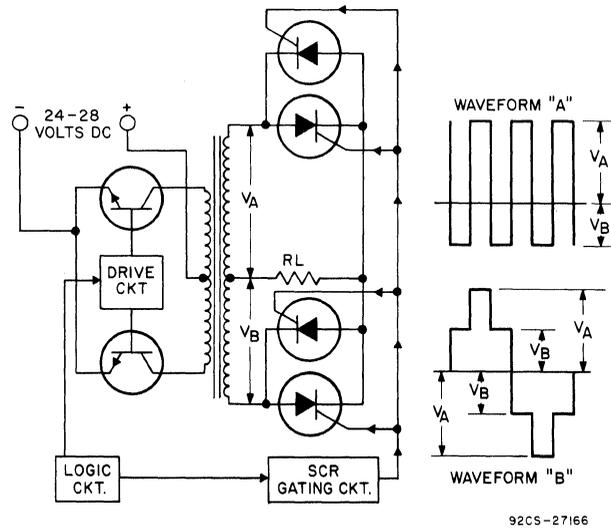
Fig. 192 - Basic circuit schematic diagram.
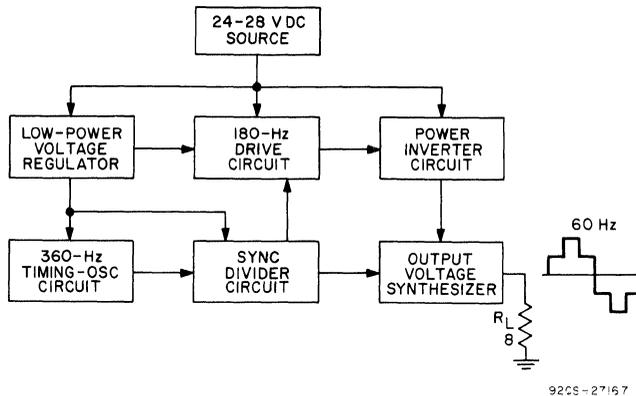
Fig. 193 - Block diagram of a 3.9-kilowatt-peak, 60-Hz, synthesized sine-wave inverter.

2. 360-Hz Timing Oscillator: Determines the timing reference for the sync divider and drive circuits.
3. Sync Divider: Divides the 360-Hz time-reference signal by two and six to create a 180-Hz drive signal and a 60-Hz SCR gating signal and synchronizes the 60-Hz gating signal with the 180-Hz drive signal.
4. 180-Hz Driver: Amplifies the drive current so that it will be capable of meeting the drive requirements of the power-inverter stage.
5. Power Inverter: Delivers a maximum of 150 amperes into a pair of bifilar-wound primary windings alternately at a rate of 180-Hz. This circuit is composed of a 2-kilowatt power transformer and six 2N5578 power transistors.
6. Output-Voltage Synthesizer: Amplifies the SCR gating signals and drives the SCR's at a 60-Hz rate to simulate the average

power and peak voltage of a 117-volt sine wave.

Detailed Circuit Operation

A detailed schematic diagram of the inverter is shown in Fig. 194. When power is applied to the circuit, the low-power regulator section starts to regulate its output to 10 volts. As the voltage builds up, the 360-Hz reference oscillator begins to generate timing pulses that are fed into the CMOS CD4017AE integrated-circuit ring counter. Seven outputs of the CD4017AE are utilized: six for a dividing function and one for reset. Eight diodes are used in the divider circuit to create two frequencies: 180 Hz and 60 Hz. This type of circuit is employed because of its simplicity and its ability to assure synchronization of the 180-Hz inverter drive signal with the 60-Hz SCR gating signals. Synchronization plays an important part in the voltage synthesizer

Q1, Q2 = 2N3054
Q3, 4, 10, 11 = 2N2102
Q8, 9 = 2N5320
Q5, 6 = 2N3772
UJT = 2N4892
Q7 = 2N3055

SCR'S = S6220M
D1, 2, 13, 14 = 1N3191
D3, D4 = 1N1186A
D5 THROUGH D12 = 1N914
T1, T2, T3 = SPECIAL

(C_T = 0.18 µF) FOR 60 Hz, 117 V OPERATION
(C_T = 0.22 µF) FOR 50 Hz, 220V OPERATION

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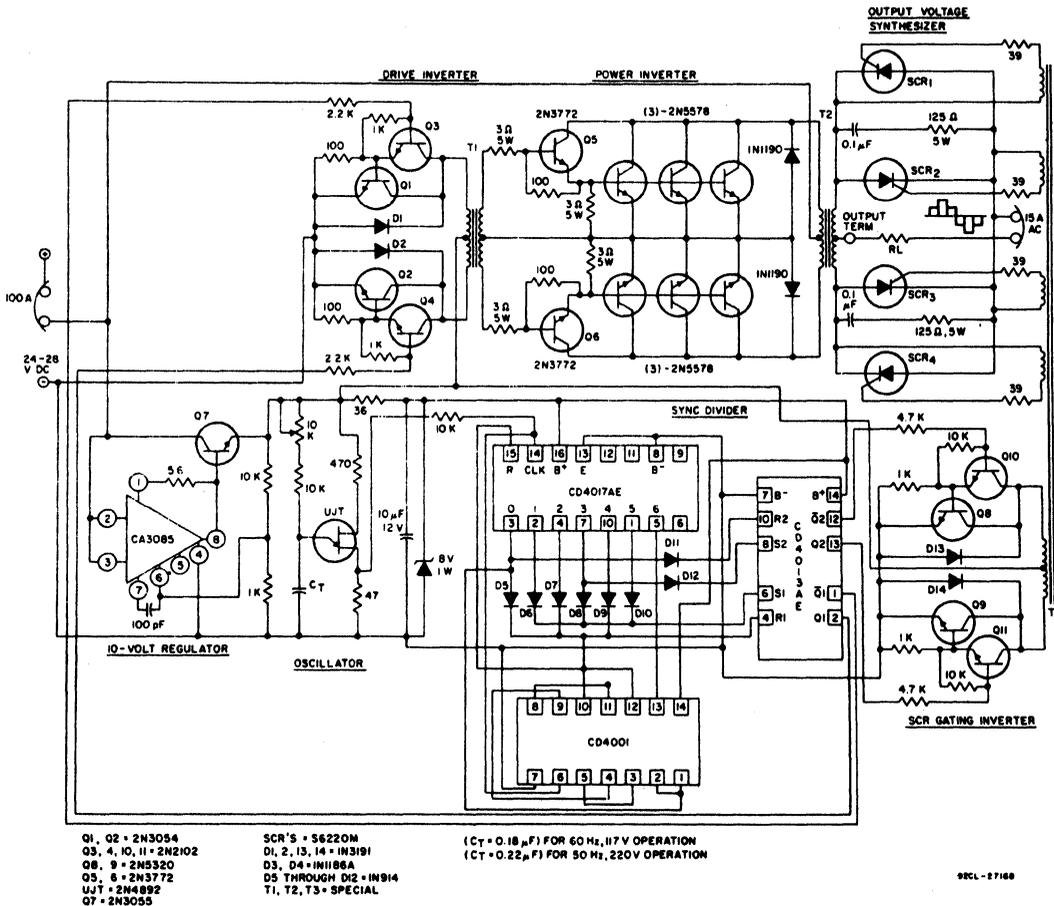
Fig. 194 - 2-kilowatt, stepped sine-wave inverter.

circuit in the simulation of the sine wave voltage across the load.

The 180-Hz and 60-Hz signals are fed into the CMOS CD4013AE dual-data flip-flop. The dual-data flip-flop provides two 60-Hz square-wave signals which are 180 degrees out of phase and which drive the push-pull SCR gating inverter. The other output of the dual-data flip-flop also has two 180-Hz square-wave signals which are 180° out of phase and drive the push-pull inverter drive circuit. The inverter drive circuit supplies 1.5 amperes of base drive to the 2N3772 power transistors in the power inverter.

Each 2N3772 transistor drives three matched 2N5578's in parallel. The 2N5578's operate the inverter output transformer T_2 in push-pull at 180 Hz. As the transformer is switched, the primary current can reach 150 amperes, depending on the load demand. One secondary winding of the transformer is connected to the other in series, as shown in Fig. 194. One winding produces 164 volts while the other produces 84 volts, as shown in Fig. 195.

Fig. 195 illustrates the voltage phase relationship between the primary and secondary windings of the inverter power transformer T_2
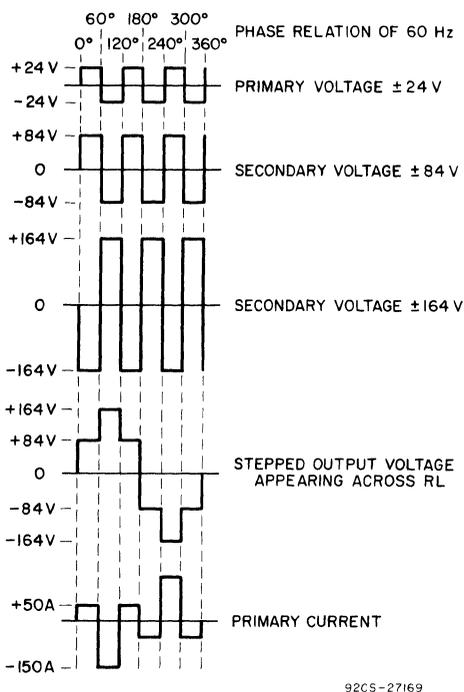
and shows the phasing between the secondary voltages and the 60-Hz synthesized sine-wave output voltage.

The voltage synthesizing circuit is a bi-directional full-wave-rectifier bridge circuit in which the SCR's are triggered alternately at 60 Hz to produce a positive or negative voltage swing across the load, R_L. The positive side of the stepped sine wave is produced when SCR's 2 and 3 are triggered together; the negative side is produced when SCR's 1 and 4 are triggered, see Fig. 194.

Circuit Design Considerations

The design of a high-power inverter of the type under discussion is based upon the voltage and power capabilities of the dc source. The 2N5578 was selected on the basis of its high-current switching capability. Careful attention must be given to the published maximum electrical characteristics for each power-transistor type: the maximum allowable case temperature, $V_{CE}(sat)$, H_{FE}, I_C, and V_{BE}. In addition, the minimum load resistance allowed must be determined so that the maximum power limitations of the transistors are not exceeded.

The following procedure is used to determine the required secondary voltage levels for the power transformer. These voltage levels are calculated to simulate the peak voltage and average power of a 117-volt rms sine wave in the output of the inverter circuit.

Step 1. Transistor Voltage Limit
The first step in calculating the safe limit of voltage stress for the 2N3772 and 2N5578 is to establish a typical source that is readily available, such as a battery source of 24 to 28 volts. This source is then used to subject the switching devices to a theoretical maximum of 56 volts, two times the high-line supply voltage resulting from auto transformer action. If a 50-percent margin is allowed for inductive spikes, the V_{CEX} voltage rating of 90 volts is not exceeded.

Step 2 Peak Output Voltage (maximum)
The peak-voltage value (125 volts ac) of a high-line sine wave is next calculated because that is the voltage value at which maximum power must be switched by the power transistors.
Peak-Voltage Value=(Effective Value) x (1.414)
or (125) x (1.414)=177 volts peak

Fig. 195 - Synchronized voltage wave-forms of T_2 and stepped output.

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Step 3. **Inverter Output Power (maximum)**

The maximum power that can be handled by the power inverter is now determined by multiplying the maximum collector current (I_C) of 150 amperes (50 amperes per 2N5578) by the supply voltage (V_{CC}) of 28 volts minus the switch voltage drop ($V_{CE}(sat)$) of 2 volts.

Max. $W = I_C$ max. x $[V_{CC}-V_{CE}(sat)]$

or $(28-2)$ x $150 = 3,900$ watts

The power transformer is a non-saturating, driven type that has an estimated efficiency of approximately 96 percent. For practical purposes, the remainder of the calculations can be rounded out to ±3 percent.

Step 4. **Minimum Load Resistance**

When the maximum power and peak voltage have been determined, the worst-case load resistance R_L can be calculated:

$$\frac{\text{Min. Load}}{\text{Resistance}} = \frac{(\text{Max. Peak Output Voltage})^2}{(\text{Max. Inverter Output Power})}$$

or $R_L = E^2/P = \dfrac{177^2}{3900} = 8$ ohms

Step 5. **Output Power**

The average power that a 117-volt rms sine wave delivers into an 8-ohm load resistance can now be determined.

$$\text{Average Power} = \frac{(117 \text{ V rms})^2}{R_L}$$

or $\dfrac{(117)^2}{8} = 1,700$ watts

Step 6. **Peak Output Voltage (nominal)**

At a nominal input voltage of 26 volts minus 2 volts for $V_{CE}(sat)$, a nominal voltage of 24 volts appears across one-half of the primary winding of the power transformer. When this voltage is present, a secondary voltage value must be available that will yield a peak-voltage value for a synthesized sine wave equivalent to that of a 117-volt rms sine wave. The calculation of the peak synthesized sine wave voltage is accomplished as described in Step 2, except that the calculation makes use of the nominal 117-volt rms value.

Peak Voltage Value=(Effective Value) x (1.414)

or (117) x (1.414)=164 volts peak

Step 7. **Step Voltage**

In synthesizing a 117-volt rms sine wave for peak voltage and equivalent power, a minimum of three voltage pulses are added consecutively every 60 degrees to produce 180 degrees of a 60-Hz stepped sine wave. The values of the two voltage pulses A and C indicated in Fig. 196 are equal and, at this point in the calculations, unknown. Pulse B, which is the peak voltage for the stepped sine wave, is known, and is equal to 164 volts. The voltage values for pulses A and C can be determined since A, B and C are the same width and must be related as a square function to provide the same peak-to-average power ratio as a sine wave.

Then $\dfrac{A^2}{3} + \dfrac{C^2}{3} + \dfrac{B^2}{3} = 117^2$

and since A=C, $\dfrac{2A^2 + 164^2}{3} = 117^2$

A=C=84 volts

Fig. 196 illustrates only the positive side of the stepped sine wave. The negative side is of equal amplitude but negative in direction.

VOLTAGE PULSE ACCUMULATION

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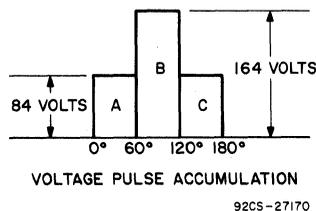
Fig. 196 - Voltage-pulse accumulation.

Step 8. **Stepped Wave Power**

A check on the previous calculations can be made now that the step voltage levels are known.

$$\text{Average Power} = \frac{\dfrac{(\text{Pulses A+C})^2}{\text{Min. } R_L} + \dfrac{(\text{Pulse B})^2}{\text{Min. } R_L}}{3}$$

or

$$\text{Average Power} = \frac{\dfrac{2 \text{ x } (84)^2}{8} + \dfrac{(164)^2}{8}}{3} = 1,700 \text{ W}$$

The information obtained in the check procedure indicates that the peak voltage and power of the sine wave synthesized in the inverter is equivalent to a 117-volt ac sine wave. However, although the peak voltage and power are equivalent, the total harmonic distortion for this type of stepped sine wave is approximately 24 percent. To obtain a sine

Table XIII - Transformer Design Data*

180-Hz or 150-Hz Drive Transformer (T$_1$)	
Core Material	=EI 75 grain-oriented silicon steel
Core Size	=square stack
Primary	=68 turns, bifilar wound, No. 23 Ga wire @ 10 V
Secondary	=41 turns, bifilar wound, No. 21 Ga wire @ 6 V
180-Hz Power Transformer (T$_2$)	
Core Material	=225 grain-oriented silicon steel
Core Size	=2.25 inch x 4.5 inch stack
Primary	=5 turns, bifilar wound, .032" thick x 3" wide, Cu @ 24 V
No. 1 Secondary	=34 turns, No. 14 Ga wire @ 164 V
No. 2 Secondary	=17.5 turns, No. 10 Ga wire @ 84 V
150-Hz Power Transformer (T$_2$)	
Core Material	=EI 225 grain-oriented silicon steel
Core Size	=2.25 inch x 4.5 inch stack
Primary	=6 turns, bifilar wound, .032" thick x 3" wide, Cu @ 24 V
No. 1 Secondary	=78 turns, No. 14 Ga wire @ 311 V
No. 2 Secondary	=39 turns, No. 14 Ga wire @ 156 V
60-Hz or 50-Hz SCR Gating Transformer (T$_3$)	
Core Material	=EI 625 grain-oriented silicon steel
Core Size	=square stack
Primary	=180 turns, bifilar wound, No. 28 Ga wire @ 10 V
Secondary	=108 turns, 4 separate windings, No. 31 Ga wire @ 6 V each

*This table includes transformer design data for 60-Hz/117-V and 50-Hz/220-V operation.

wave with a lower distortion content, more than three voltage pulses per polarity change must be provided.

When the two secondary voltage levels have been determined, the inverter power transformer and drive and SCR gating transformers can be designed according to standard transformer design procedures. The data needed to design the transformers used in the subject inverter is shown in Table XIII.

Two additional factors which must be considered when designing this inverter are the drive current and drive voltage needed for the Darlington-connected configuration. As illustrated in the detailed schematic diagram of Fig. 194, the three 2N5578's are driven by a 2N3772 transistor. A minimum gain of 10 was selected for the 2N3772 transistor and the 2N5578's. The total forced gain condition of the Darlington configuration is, then, 100. For 150 amperes of collector current, a base drive current of 1.5 amperes is needed. The typical worst-case V$_{BE}$ for this Darlington configuration is approximately 3 volts. The drive transformer was designed to supply 6 volts of drive for the input. Therefore, a 2-ohm, 3-watt resistor is used in series with the base of each 2N3772 to provide base-current limiting of 1.5 amperes.

Current Sharing—Current sharing of the 2N5578's is achieved by V$_{BE}$ matching as opposed to the less efficient emitter-ballast resistor method. The matching procedure involved the selection of three transistors with V$_{BE}$'s within 100 millivolts at 50 amperes. Tests indicate that this margin can spread to about 200 millivolts at a case temperature of 75° C. Since the V$_{BE}$ will be exactly the same when the circuit is in operation, the 200-millivolt spread must be related to a collector-current spread. The data-sheet transfer characteristic of Fig. 197(a) indicates a collector-current variation of about 4 amperes. This means that a worst-case match at 150 amperes can yield collector currents of 52, 50, and 48 amperes. Therefore, the value of maximum collector current should be increased by 4 percent in the calculations for power dissipation for each device.

Power Dissipation in the 2N5578—The calculated value of power dissipation is used to determine an adequate heat-sink size for a 100° C maximum case temperature. The junction temperature, which is of main concern, is limited to 175° C for the 2N5578. If an efficiency of 85 percent is achieved at 2 kilowatts, a maximum dissipation of 50 watts per transistor could be expected. The maxi-
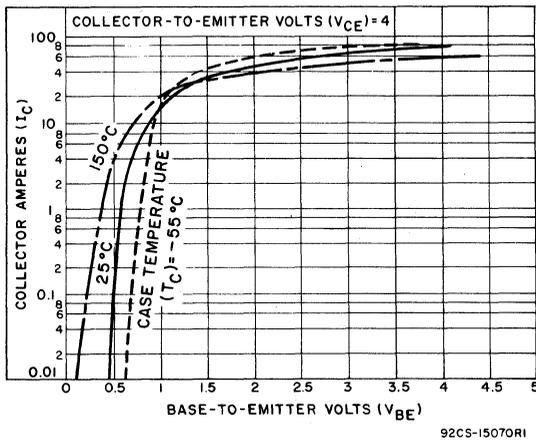
Fig. 197(a) - *Typical transfer characteristics for type 2N5578.*
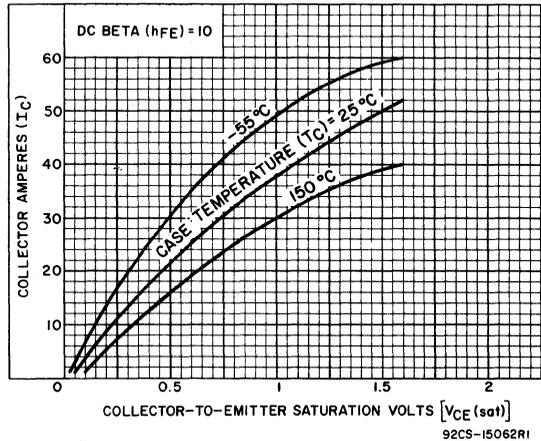
Fig. 197(b) - *Typical saturation voltage characteristics for type 2N5578.*

mum junction temperature is then:
$T_j=T_c+R_{\theta JC} P_d=100+0.5\times50=125°C$. This value is acceptable.

Actual dissipation can be calculated with the aid of the primary current waveform of Fig. 195. The dissipation of each transistor during pulses A and C is:

$P_d = V_{CE}(sat) \times I_C = 0.45$ V $\times 17$ A
$\qquad = 7.65$ watts

However, the dissipation during pulse B is much higher since the current and saturation voltage are greater:

$P_{d(peak)} = 2.0$ V $\times 52$ A $= 104$ watts.

The saturation voltages are determined from the characteristic curve, which is shown in Fig. 197(b). The average power dissipation in each transistor is:

$P_{d(avg)} = ½ \times 7.65 + 1/6 \times (104-7.65)$
$\qquad = 20$ watts and
$T_{j(avg)} \quad = 100 + 0.5 \times 20 = 110°C.$

Clearly, the peak junction temperature during pulse B must be determined to assure that the $175°C$ temperature is not exceeded. The width of pulse B is ½ x 1/180 Hz=2.8 milliseconds
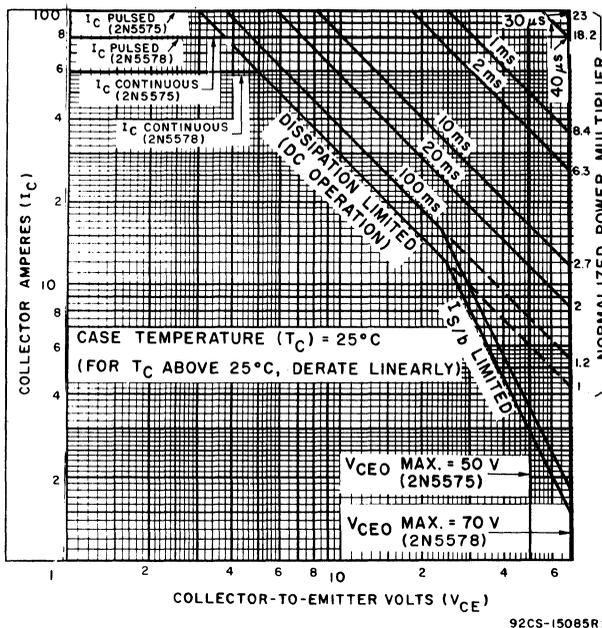
Fig. 197(c) - *Collector-to-emitter voltage as a function of collector current.*

and, from the maximum operating area of Fig. 197(c), the transient thermal resistance is approximately:

$$R_{\theta JC}(TR) = \frac{175-25°C}{50\,A \times 30\,V} = \frac{150}{1500} \overline{\overline{=}} 0.1°C/watt$$

The peak junction temperature at the end of pulse B is then:

$$T_{j(peak)} = T_{j(avg)} + P_{d(peak)} \times R_{\theta JC}(TR)$$
$$= 110 + 104 \times 0.1 = 120.4°C$$

Since the load is primarily resistive, switching losses can be calculated in the traditional way:

$$P_{SW}(off) = \frac{52\,A \times 28\,V}{6} \times 5\,\mu s \times 180\,Hz$$
$$= 0.22\,W$$

It is assumed that losses for turn-on power and "shoot-through" (both sides on momentarily) are of the same magnitude; the result is a total switching loss of 1 watt.

Heat Sink

Since the total average power dissipation is now known, the minimum heat sink size can be determined from:

$$T_c = T_a + P_d \times R_{\theta HS} \text{ or } R_{\theta HS} = \frac{T_c - T_a}{P_d}$$

Assuming T_a max.$=60°C$ and three devices per heat sink:

$$R_{\theta HS} = \frac{100-60}{3 \times 21} = 0.64°C/watt$$

A 0.5°C/watt heat sink was selected.

Performance

A curve of efficiency as a function of output power is shown in Fig. 198. The curve indicates that the high efficiency of a switching inverter can be realized with a simulated sine wave output. The low distortion (less than 1 percent) of a class B amplifier, which is normally used to produce a sine wave, has been sacrificed for efficiency. Ideally, a class B amplifier exhibits a peak efficiency of 78.5 percent, but this efficiency is never realized, and values of 40 to 50 percent are typical. In contrast, the stepped sine wave inverter discussed in the preceding paragraphs exceeds 75 percent efficiency above 500 watts, has an 80 percent efficiency between 650 and 2000 watts, and a peak efficiency of 87 percent at 1300 watts.

The high efficiency contributes to the low
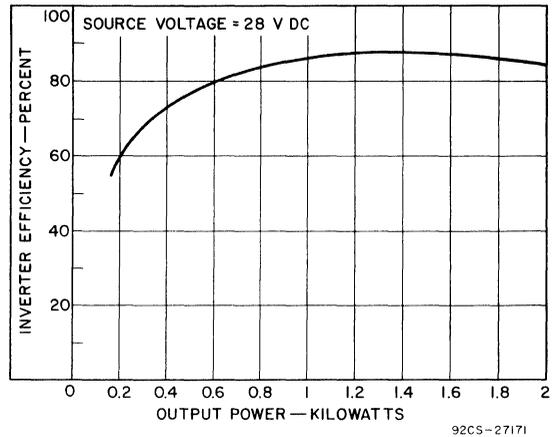
Fig. 198 - *Inverter efficiency as a function of output power.*

case temperature of the power transistors, approximately 60°C during operation.

Fig. 199, a regulation curve for the inverter, indicates a load regulation of about 7 percent. This value corresponds to an output resistance of 0.45 ohm up to 1500 watts output; resistance increases to 1 ohm at 2 kilowatts.
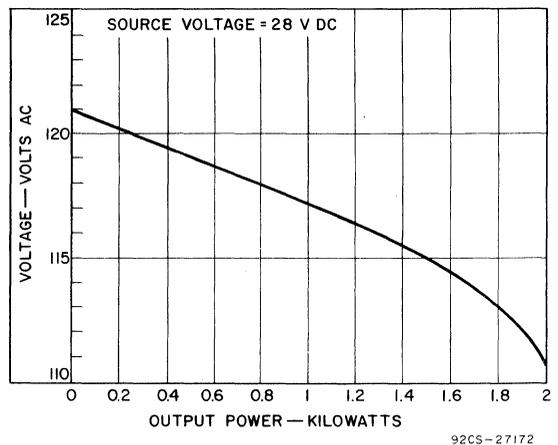
Fig. 199 - *Output-voltage regulation as a function of output power.*

The efficiency stated above and the power curves shown were generated with a resistive load. Tests with inductive loads indicated that phase shifts up to 60° are allowable before malfunction (common-mode conduction) occurs. Such malfunction results in circuit-breaker trip-out without noticeable damage to the supply.
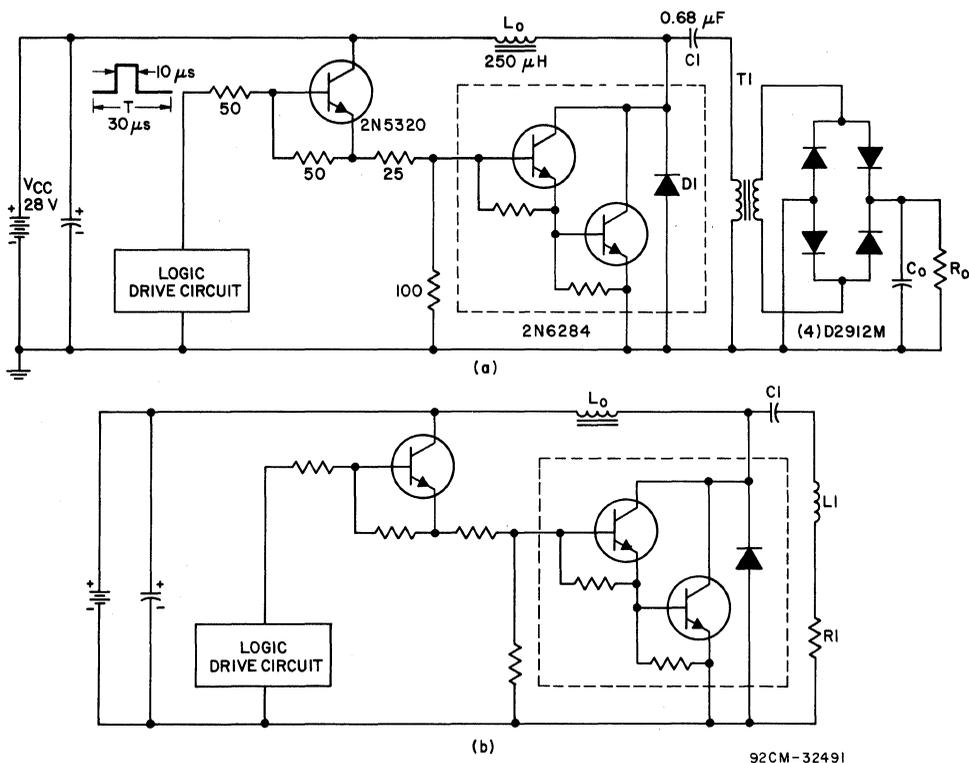
Fig. 200 - Resonant sine-wave inverter circuit.

20-AMPERE SINE-WAVE-INVERTER

Circuit Description

Single-Transistor Inverter—Fig. 200(a) shows the circuit diagram of the single Darlington-transistor sine-wave inverter. The circuit consists of a 28-volt dc power supply, a two-stage power amplifier, a charging choke (L_0) and a series-resonant load circuit, which is formed by capacitor C_1 and transformer T_1. (Transformer and charging choke data are given on succeeding pages of this section.) The power amplifier utilizes a type 2N5320 transistor as the current source for base drive of the output transistor. The output stage utilizes the type 2N6284 (n-p-n) power Darlington transistor as the power switch; this switch is connected in shunt with the output-load circuit. The series-resonant output-load circuit is formed by capacitor C_1, the primary leakage inductance of T_1, and the transformed value of the secondary-load resistance. The secondary-load circuit consists of a full-wave bridge rectifier, which uses four RCA D2412M diodes, and an output filter capacitor C_0, paralleled with load resistor R_0.

Fig. 200(b) illustrates the basic form of the series-resonant circuit as viewed from the collector-emitter terminals of the 2N6284 transistor; Fig. 201 shows typical circuit waveforms. The operation of the circuit is as follows. Initially, capacitor C_1 is charged to a voltage equal to the dc input voltage, V_{CC}. The base of the type 2N5320 transistor is driven by a square-wave pulse whose width is 10 microseconds and whose repetition rate is 30 microseconds. In the type of inverter under discussion, the pulse width is maintained constant during operation; the pulse repetition rate is usually varied, however, to achieve good load regulation. Although the power-Darlington transistor has high gain, a driver stage using the 2N5320 transistor was employed to assure minimum loading on the IC logic circuitry that provides the input-drive signal.

The inverter is turned on by a 10-volt, 10-microsecond pulse, as shown in Fig. 201(b), and both the 2N5320 and 2N6284 transistors are driven into voltage saturation. During this interval, the 2N6284 transistor acts as a closed switch, essentially shorting capacitor C_1 to

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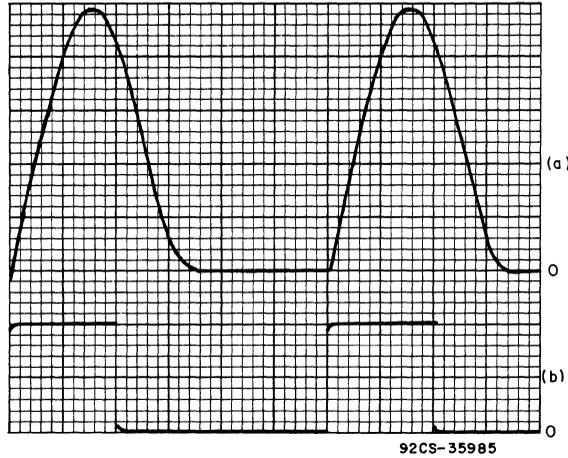
Fig. 201 - Inverter turn-on waveforms:
(a) Collector current $I_C=5$
A/div.; (b) Input base drive
voltage $V_B=5$ V/div. ($t=5$
$\mu s/div.$)

ground. Capacitor C_1 discharges its energy through inductor L_1 and resistor R_1. The series combination of C_1, L_1, and R_1 forms a series resonant circuit whose natural resonant frequency is approximately 50 kHz. A sinusoidal load current ($I_C(pk)$) having a maximum amplitude of 25 amperes flows in the output circuit, as shown in Fig. 201(b). The internal diode, D_1, of the power-Darlington transistor assures closure of the collector-emitter circuit and provides a path for any reverse-current conduction. The extent to which reverse current will flow through the diode depends upon the circuit loading and the repetition rate of the driving signal. In the implementation of the circuit of Fig. 200, the loading and repetition rate were adjusted to achieve maximum output power with good efficiency; this adjustment minimizes reverse-current flow.

Figs. 202(a) and 202(b) show the relationship between the collector current and the collector-emitter voltage of the Darlington power transistor. At the end of the 10-microsecond input-pulse interval, the drive signal is turned off for 20 microseconds. Since both the transistor and diode are then non-conducting, the combination approximates an open switch. Output capacitor C_1 is recharged by the dc input voltage, V_{CC}, through choke L_0. The resultant voltage across the transistor increases in magnitude to a peak value substantially greater than V_{CC}, as shown in Fig. 202(b). Because collector-current conduction is de-

layed until after complete collector-voltage saturation, and because the collector voltage is reapplied at the time of zero collector-current conduction, no significant transition losses occur. The main power losses occur during the on-state conduction period, and are contributed to by the associated circuit losses in the output transformer and rectifier diodes. No reverse-bias base current drive is required during turn-off.
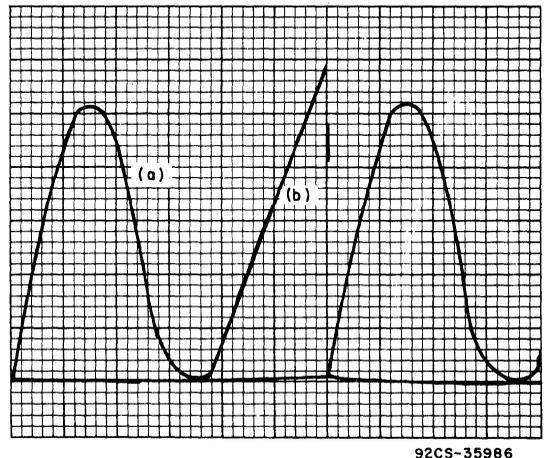
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Fig. 202 - Relationship between collector
current and collector-emitter
voltage of Darlington power
transistor: (a) Collector current
$I_C=5$ A/div.; (b) collector-to-
emitter voltage $V_{CE}=20$ V/div.
($t=5$ $\mu s/div.$)
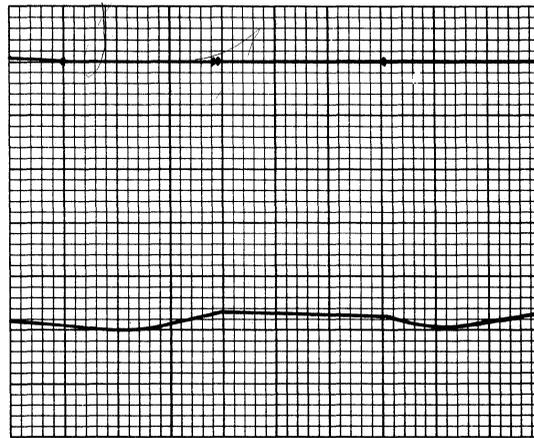
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Fig. 203 - DC output-voltage waveform
(t=5 μs/div.).

Fig. 203 shows the waveform of the dc output voltage of the circuit of Fig. 200. The level of output is 48 volts across a 12-ohm load resistor for a dc output power of 192 watts. DC input power is 218.4 watts, so that circuit efficiency is 87 percent. Overall circuit performance data is presented in Table XIV. Fig. 204 shows the performance of the circuit with changing load. The repetition rate may be adjusted, as shown in Fig. 204, to provide a constant output voltage of 48 volts.

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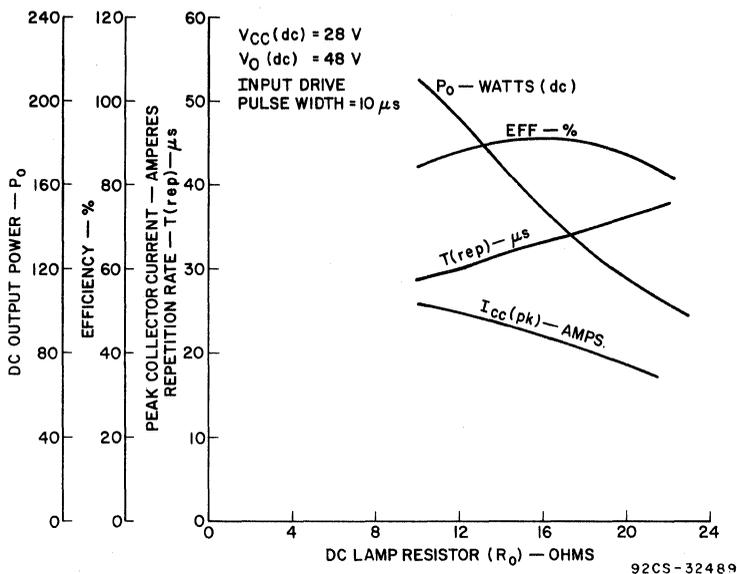
Fig. 204 - Performance of the sine-wave
inverter with changing loads.

Table XIV - Typical Performance Data

Characteristic	Value	Units
DC Supply Voltage (V_S)	28	V
DC Input Current (I_{DC})	8	A
Peak Collector Current (I_{pk})	25	A
DC Output Voltage (V_O)	48	V
DC Output Load (R_O)	12	Ω
DC Output Power (P_O)	192	W
DC Input Power (P_S)	218.4	W
Efficiency (η_p)	87	%
Output Resonant Freq. (T_O)	50	kHz
Input Pulse Width (T_P)	10	μs
Pulse Repetition Rate T(rep.)	30	μs
Transformer and Charging-Choke Data		
Transformer T_1		
Primary Inductance (Lp)	110 μH	
Number Turns (Np)	24 T	
Wire Size:	56/30 Litz (Twisted Pair)	
Secondary Inductance (Ls)	375 μH	
Number Turns (Ns)	43	
Wire Size:	56/30 Litz (Twisted Pair)	
Core:	Indiana General IR8207	
Air Gap	30 mils	
Note: ½ Np wound on separate coil form ½ Np wound on same form with Ns		
Charging Choke Inductance (Lo)	250 μH	
Number Turns (N)	36 T	
Wire Size:	56/30 Litz (Twisted Pair)	
Core:	Indiana General IR8207	
Air Gap:	30 mils	

Overload Protection

Semiconductors are used today in many applications in power and control circuits. Their great advantage is in their capability to handle considerable power within a very small size. Unfortunately, because of their small mass, they are less able to withstand high-current overloads and overvoltages. Currents of many thousands of amperes may be caused by electrical faults (e.g., short circuits) in the circuit. The following pages describe the possibilities of protecting a semiconductor by fusing—when and how a fuse can be used and how much protection is afforded. Cases for which fuse protection is not possible, or for which only partial protection is feasible, are also discussed. Fuse selection methods are described.

FUSE BASICS

A fuse is a component that protects the semiconductor devices in a circuit against a failure of one or more of them as a result of a current overload. The fuse is connected in series with either the device to be protected or the load to be controlled.

The protection requirements of a fuse can be summarized as follows:

A fuse must withstand the normal steady-state current, and interrupt overload current safely without permanently changing semiconductor performance.

Therefore, a fuse must limit the amount of current allowed to pass through the semiconductor, limit the thermal energy to which a device is subjected (I^2t), and not produce an arc voltage greater than the semiconductor rating.

The protection can be either complete or for short-circuit only. In the first case, the fuse capability must be less than that of the semiconductor it is to protect over the overload time range. This type of protection is illustrated in Fig. 205.
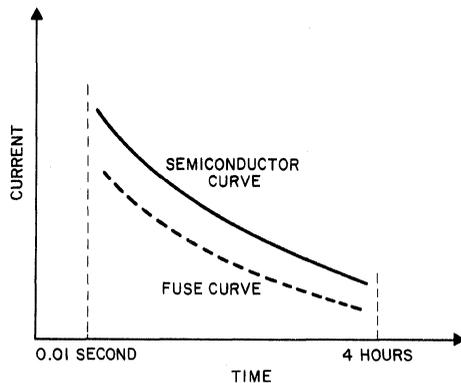
Fig. 205 - Complete protection of semiconductor by fuse.

The second case is the most common: a circuit breaker provides protection during long-duration overload, and the fuse works only for short-duration overloads. This type of protection is shown in Fig. 206. The following pages examine only the second type of protection.
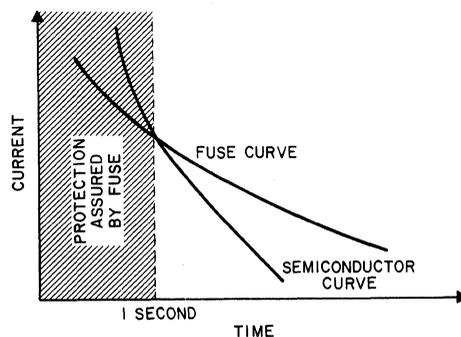
Fig. 206 - Semiconductor protected by fuse for short-circuit only.

Definitions

As shown in Fig. 207, a cartridge fuse consists of the fusing element (generally pure silver), the filling material, the body, and the

terminals. Fig. 208 shows how the fuse is connected into the circuit; Fig. 209 shows the condition of the waveforms when a fuse interrupts an overload current.
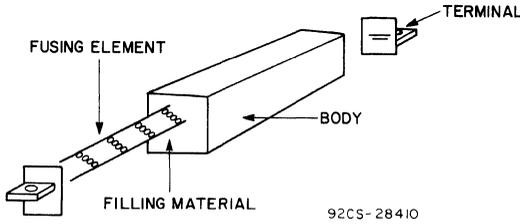
Fig. 207 - Cartridge fuse parts.
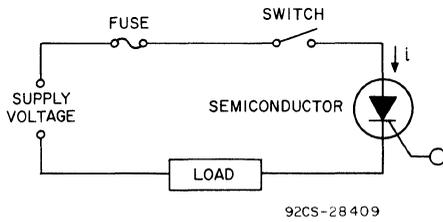
Fig. 208 - A fused circuit.
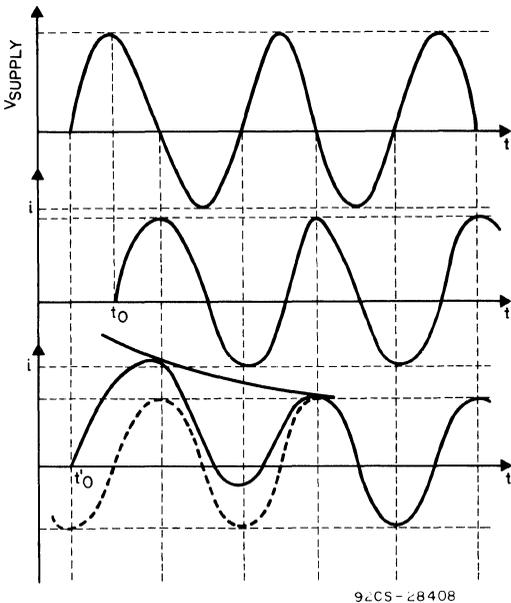
Fig. 209 - Current waveform for unfused circuit.

The shape of the current waveform depends on the time at which the overload occurs. Assume first that the overload occurs at the time that the switch (Fig. 208) is closed. If the

switch is closed at t_o, the time of maximum supply voltage, the current waveform will be symmetrical, Fig. 209. If the switch is closed at another time, particularly at t'_o, the current waveform will be asymmetrical. This asymmetry is caused by the load parameter, $\cos\phi$ (generally, during fuse manufacture, $\cos\phi$ is chosen at 0.1). When an overload current is interrupted by a fuse, the short-circuit current shape is triangular, as shown in Fig. 210. Of course, this shape is fixed by the properties of the fuse.
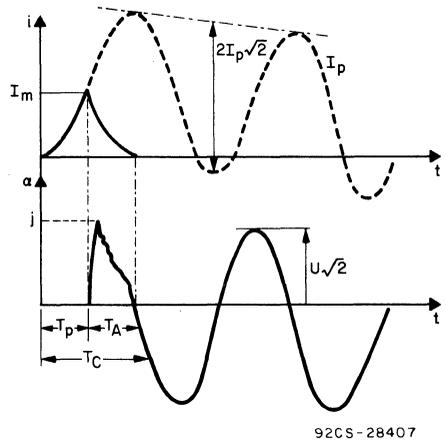
Fig. 210 - Voltage and current waveforms during action of a fuse.

Fuse Terminology

Voltage Rating, V_N:
  Sinusoidal or continuous voltage value for which the cartridge fuse is built.
Current Rating, I_N:
  Current from which characteristics are drawn. The fuse can withstand this current without damage.
Expected Current, I_p:
  AC: Effective value of the ac current component.
  DC: Continuous-current component value. This current would flow in the circuit if the cartridge fuse impedance were negligible.
Melting Time, T_p:
  Time from the moment of overload until the fuse is melted. (Fig. 210)
Arcing Time, T_A:
  Duration of arc. (Fig. 210)
Clearing Time, T_c:
  $T_p + T_A$ (Fig. 210)
Peak Current, I_m:

Maximum instantaneous current value reached in the protected circuit. (Fig. 210)

Melting Energy, I^2t:

$$\int_0^{T_p} i^2 dt$$

Arcing Energy, I^2t:

$$\int_{T_p}^{T_c} i^2 dt$$

Clearing Energy, I^2t:

$$\int_0^{T_c} i^2 dt = \int_0^{T_p} i^2 dt + \int_{T_p}^{T_A} i^2 dt$$

Arc Voltage:
Maximum voltage across the cartridge fuse during its working time.

Working Voltage:
Effective voltage value across the fuse after the current stops. It is less than or equal to the maximum rated voltage, V_N.

Breaking Capacity:
Maximum current that can be passed by the fuse.

Fuse Characteristics

The following fuse characteristics typically supplied by the manufacturer are shown in Fig. 211.

Time/current characteristics
Maximum value of total operating energy
Actual total operating time
Voltage drop
Arc voltage
Cutoff characteristics

An example of how these characteristics are used is given below.

Fuse Position

There is no well-established theoretical method for determining the correct location of a fuse in a circuit; only practical examples can be given: rectifier circuits, inverters, dimmers—all in the small- or medium-power range. More detailed methods concerning the protection of high-power circuits through the use of several semiconductors in parallel can be found in the literature. Three types of protection are discussed in the following paragraphs:

- External
- Internal
- Total

Fig. 212 summarizes these types of protection. When only external protection is required, the fuse is connected at the output of the circuit, just before the load. When internal or total protection is required, fuses are placed either at the circuit input or internal to it.
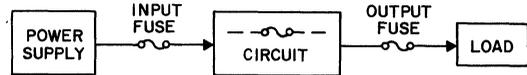
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Fig. 212 - Fuse placement.

EXTERNAL PROTECTION

The characteristic curve of the protection system must cover the same time range as the device curve. When the circuit is protected by a fuse only, fuse and device curves cover the same time range, Fig. 205. When a circuit is protected by a circuit breaker and a fuse with a short time characteristic, the current-time capacity of the fuse must be less than that of the semiconductor, Fig. 206.

INTERNAL PROTECTION

Bridge Rectifier

When internal protection is to be provided, the fuses can be connected in series with the semiconductors or the phase lines. For example, Fig. 213 illustrates the case of the protection of a Greatz bridge. The in-line fuse rating is equal to the fuse rating in the bridge multiplied by $\sqrt{2}$. Fig. 214 gives voltages and currents at different locations of several rectifier bridges. This information aids in calculating fuse ratings.
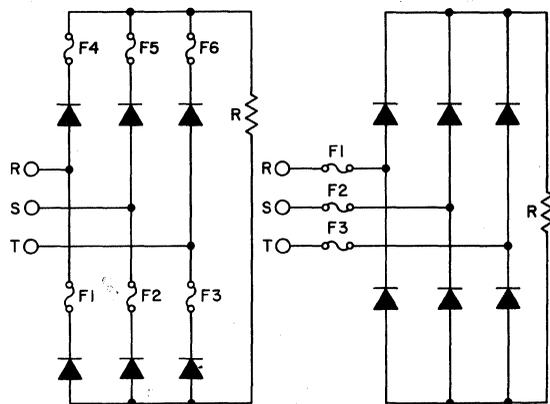
92CS - 28405

Fig. 213 - Three-phase-bridge fuse protection.

(a) TIME/CURRENT CHARACTERISTICS

92CS-28426

(b) MAXIMUM VALUE OF TOTAL ENERGY

92CS-28427

(c) ACTUAL TOTAL OPERATING TIME

92CS-28428

(d) VOLTAGE DROP

92CS-28429

(e) ARC VOLTAGE

92CS-28422

(f) CUTOFF CHARACTERISTICS

92CS-28423
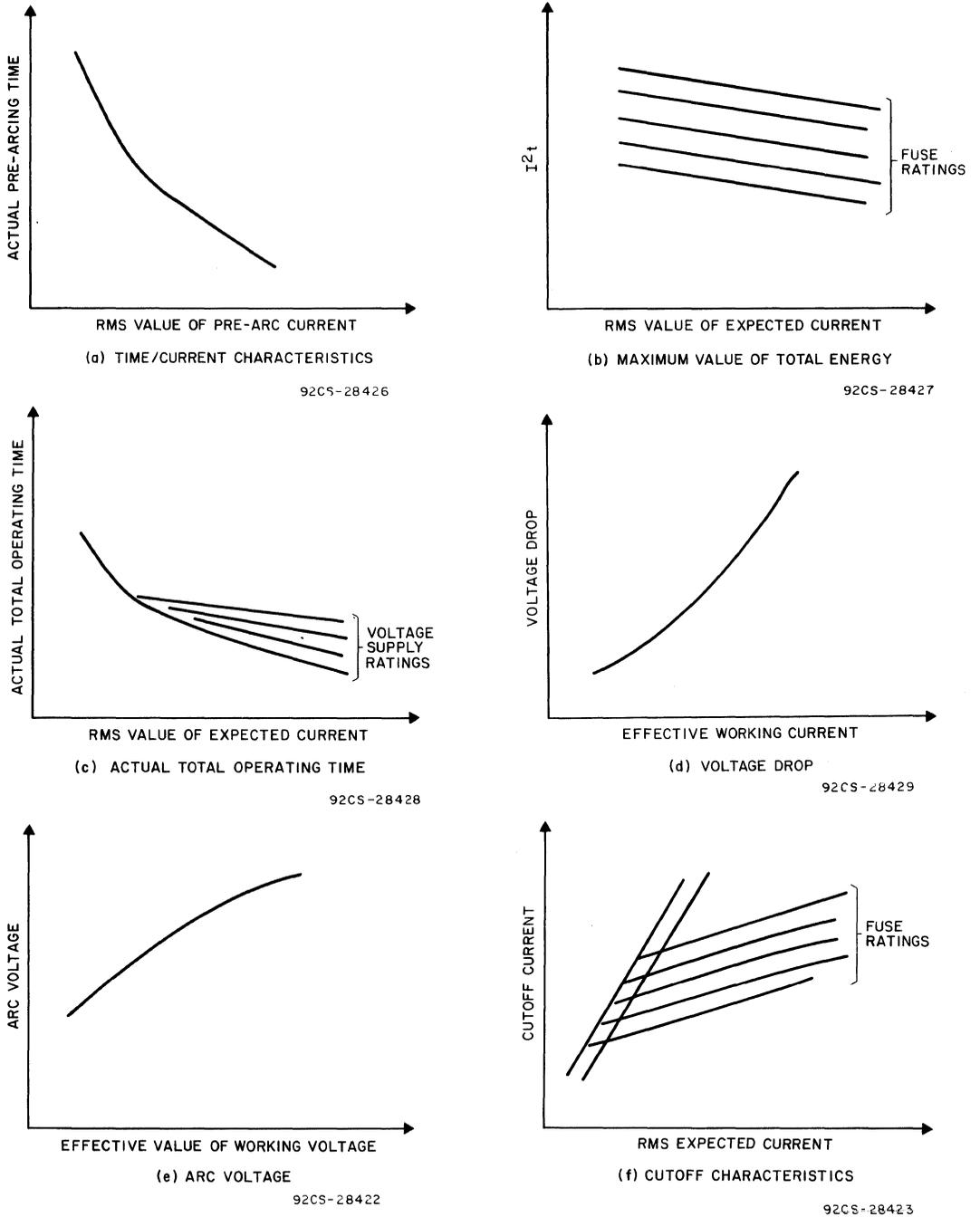
*Fig. 211 - Fuse characteristics typically
supplied by the manufacturer.*

In inverter circuits, it is recommended that the fuse be placed in series with each device.

Fuse Choice

Fuse choice consists of four steps:
- Type of fuse
- Working voltage
- Fuse rating
- Fuse arc voltage

The type of fuse, slow or fast, depends on the type of semiconductor to be protected; a

SINGLE PHASE HALF WAVE	SINGLE PHASE FULL WAVE	SINGLE PHASE BRIDGE	THREE PHASE HALF WAVE	THREE PHASE FULL WAVE	DOUBLE START CONNECTION WITH INTERPHASE TRANSFORMER	HEX –BRIDGE
$I_{CRMS} = \frac{\pi}{2} I_{CAV}$	$I_{CRMS} = \frac{\pi}{2\sqrt{2}} I_{CAV}$ $I_{DAV} = \frac{1}{2} I_{CAV}$ $I_{DRMS} = \frac{\pi}{4} I_{CAV}$	$I_{CRMS} = \frac{\pi}{2\sqrt{2}} I_{CAV}$ $I_{DAV} = \frac{1}{2} I_{CAV}$ $I_{DRMS} = \frac{\pi}{4} I_{CAV}$ $I_{RMS} = \frac{\pi}{2\sqrt{2}} I_{CAV}$	$I_{CRMS} = \frac{\pi}{3} I_{CAV}$ $I_{DAV} = \frac{1}{3} I_{CAV}$ $I_{DRMS} = \frac{\pi}{3\sqrt{3}} I_{CAV}$	$I_{CRMS} = \sim I_{CAV}$ $I_{DAV} = \frac{I_{CAV}}{3}$ $I_{DRMS} = \frac{I_{CAV}}{\sqrt{3}}$ $I_{RMS} = \sqrt{\frac{2}{3}} I_{CAV}$	$I_{CRMS} = \sim I_{CAV}$ $I_{DAV} = \frac{I_{CAV}}{2\times3}$ $I_{DRMS} = \frac{I_{CAV}}{2\sqrt{2}}$	$I_{CRMS} = \sim I_{CAV}$ $I_{DAV} = \frac{I_{CAV}}{6}$ $I_{DRMS} = \frac{I_{CAV}}{\sqrt{6}}$
$V_C = \frac{\pi}{2} V_{CAV}$ $V_{PK} = \pi V_{CAV}$ $V_{RMS} = \frac{\pi}{\sqrt{2}} V_{CAV}$	$V_{CRMS} = \frac{\pi}{2\sqrt{2}} V_{CAV}$ $V_{PK} = \frac{\pi}{2} V_{CAV}$ $V_{RMS} = \frac{\pi}{2\sqrt{2}} V_{CAV}$	$V_{CRMS} = \frac{\pi}{2\sqrt{2}} V_{CAV}$ $V_{PK} = \frac{\pi}{2} V_{CAV}$ $V_{RMS} = \frac{\pi}{2\sqrt{2}} V_{CAV}$	$V_{CRMS} = \frac{\pi}{3} V_{CAV}$ $V_{PK} = \frac{2\pi}{3} V_{CAV}$ $V_{RMS} = \frac{2\pi}{3\sqrt{2}} V_{CAV}$	$V_{CRMS} = V_{CAV}$ $V_{PK} = \frac{\pi}{3} V_{CAV}$ $V_{RMS} = \frac{\pi}{3\sqrt{2}} V_{CAV}$	$V_{CRMS} = V_{CAV}$ $V_{PK} = \frac{2\pi}{3} V_{CAV}$ $V_{RMS} = \frac{2\pi}{3\sqrt{2}} V_{CAV}$	$V_{CRMS} = V_{CAV}$ $V_{PK} = \frac{2\pi}{3} V_{CAV}$ $V_{RMS} = \frac{\pi}{\sqrt{6}} V_{CAV}$

C = CONTINUOUS STD
D = DIODE

TRANSFORMER VOLTAGE DROP AND DIODE FORWARD-VOLTAGE-DROP NEGLECTED.

92CL-28454

Fig. 214 - Voltages and currents at various locations of several rectifier bridges.

fuse must operate before semiconductor degradations occur.

The working voltage of the fuse must be in agreement with the supply voltage. Often, to decrease fuse energy dissipation, a higher working voltage than needed is chosen.

The current rating of a fuse must be at least the value of the rms current flowing through the device. But most of the time that value is not large enough and, occasionally, some fuses may fail under the normal steady-state conditions for the device being protected. The fuse manufacturers specify a correction factor, F, which allows the user to calculate the fuse rating as follows:

Fuse Rating=F · I_RMS

The factor F depends on the following parameters:
- Permanent current: AC current with T < 100 milliseconds DC current without interruption or with interruption limited to within 10 milliseconds
- Temperature
- Forced cooling
- Effect of the current variation on the fuse life
- Current waveshape
- Random current overload expected

The fuse arc voltage is an important parameter; the speed of the fuse and the arc voltage are interdependent. The faster the fuse, the higher the arc voltage. Because this arc voltage is applied between the semiconductor main terminals, it should be smaller than the maximum voltage rating of the semiconductor. The extent to which the arc voltage limits the use of fuses in semiconductor protection is covered in the following paragraphs.

Fig. 215 describes the arc voltage as a function of rms supply voltage. The arc voltage is never more than 2.2 V_N, the sinusoidal or continuous voltage value for which the fuse is designed. In the worst case then, one must select a fuse so that 2.2 V_N does not exceed the maximum rated voltage of the device to be protected.

For additional information on Fuses, refer to RCA Application Note, AN-6452, "A New Practical Fuse-Thyristor Coordination Method."
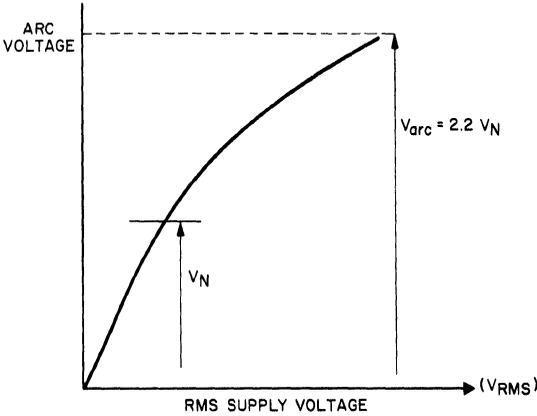
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*Fig. 215 - Arc voltage as a function of V$_{RMS}$
supply curve.*

Audio Power Amplifiers

The quality of an audio power amplifier is measured by its ability to provide high-fidelity reproduction of audio program material over the full range of audible frequencies. The amplifier is required to increase the power level of the input to a satisfactory output level with little distortion, and the sensitivity of its response to the input signals must remain essentially constant throughout the audio-frequency spectrum. Moreover, the input-impedance characteristics of the amplifier must be such that the unit does not load excessively and thus adversely affect the characteristics of the input-signal source.

Silicon power transistors offer many advantages when used in the power-output and driver stages of high-power audio amplifiers. These devices may be used, either as discrete components or as building-block elements in power hybrid circuits, over a wide range of ambient temperatures to develop up to hundreds of watts of audio-frequency power to drive a loudspeaker system. The following paragraphs describe the basic factors that must be considered and the important concepts and techniques employed in the design of transistor audio power amplifiers.

CLASSES OF OPERATION

A circuit designer may select any one of three classes of operation for transistors used in linear-amplifier applications. This selection is made on the basis of a combination of such factors as required power output, dissipation capability, efficiency, gain, and distortion characteristics.

The three basic classes of operation (class A, class B, and class C) for linear transistor amplifiers are defined by the operating point of the transistor. In class A operation, the active element conducts for the entire input cycle. In class B operation, the active element conducts for 180 degrees of an input cycle and is cut off during the remainder of the time. In

class C operation, the active element conducts for some amount less than 180 degrees of an input cycle. The following paragraphs discuss the distinguishing features of class A and class B operation. In general, because of the high harmonic distortion introduced as a result of the short conduction angle, class C operation is used primarily in rf-amplifier applications in which it is practical to use tuned output circuits to eliminate the harmonic components. For this reason, class C operation is not discussed further.

Class A Operation

Class A amplifiers are used for linear service at low power levels. When power amplifiers are used in this class of operation, the amplifier output is usually transformer-coupled to the load circuit, as shown in Fig. 216. At low power levels, the class A amplifier can also be coupled to the load by resistor, capacitor, or direct coupling techniques.
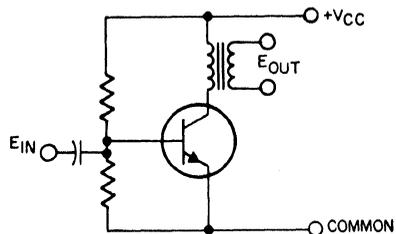
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Fig.216 - Basic class A, transformer-coupled amplifier.

There is some distortion in a class A stage because of the nonlinearity of the active device and circuit components. The maximum efficiency of a class A amplifier is 50 per cent; in practice, however, this efficiency is not realized. The class A transistor amplifier is usually biased so that the quiescent collector current is midway between the maximum and minimum values of the output-current swing.

Collector current, therefore, flows at all times and imposes a constant drain on the power supply. The consistent drain is a distinct disadvantage when higher power levels are required or operation from a battery is desired.

Class B Operation

Class B power amplifiers are usually used in pairs in a push-pull circuit because conduction is not maintained over the complete cycle. A circuit of this type is shown in Fig. 217. If conduction in each device occurs during

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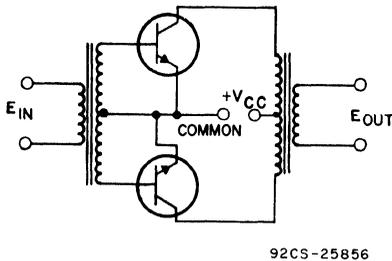
Fig.217 - Basic class B, push-pull trans-former-coupled amplifier.

approximately 180 degrees of a cycle and the driving wave is split in phase, the class B stage can be used as a linear power amplifier. The maximum efficiency of the class B stage at full power output is 78.5 per cent when two transistors are used. In a class B amplifier, the maximum power dissipation is 0.203 times the maximum power output and occurs at 42 per cent of the maximum output.

Transistors are not usually used in true class B operation because of an inherent nonlinear-ity, called **cross-over distortion**, that produces a high degree of distortion at low power levels. The distortion results from the nonlinearities in the transistor characteristics at very low current levels. For this reason, most power stages operate in a biased condition somewhat between class A and class B.

This intermediate class is defined as **class AB**. Class AB transistor amplifiers operate with a small forward bias on the transistor to minimize the nonlinearity. The quiescent current level, however, is still low enough so that class AB amplifiers provide good effic-iency. This advantage makes class AB ampli-fiers an almost universal choice for high-power linear amplification, especially in battery-operated equipment.

DRIVE REQUIREMENTS

In class A amplifiers, the output stage is usually connected in a common-emitter con-figuration. The relatively low input impedance that generally characterizes this type of configuration may result in a severe mismatch with the output impedance of the driver transistor. Usually, at low power levels, RC coupling is used and the loss is accepted. It may be advantageous in some circuits, how-ever, to use an emitter-follower between the driver and the output stage to obtain an improved impedance match.

Class AB amplifiers have many types of output connections. One form is the **trans-former-coupled output stage** illustrated in Fig. 218. Again, the common-emitter circuit is

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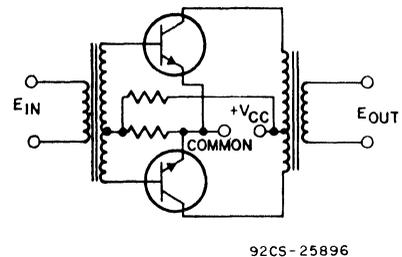
Fig.218 - Basic class AB, push-pull, trans-former-coupled amplifier.

usually employed because it provides the highest power gain. The load circuit is never matched to the output impedance of the transistor, but rather is fixed by the available voltage swing and the required power output. The transformer is designed to reflect the proper impedance to the output transistors so that the desired power output can be achieved with a specific supply voltage.

The use of transformer coupling from the driver to the input of the power transistor assures that the phase split required for push-pull operation of the output stages and any necessary impedance transformation can be readily achieved. Output transformer coupling provides an easy method for matching several values of load impedance, including those encountered in sound-distribution systems. For paging service, servo motor drive, or other applications requiring a limited band-width, the transformer-coupled output stage is very useful. However, there are disadvantages to the use of transformer coupling. One disadvantage is the phase shift encountered at

low- and high-frequency extremes, which may lead to unstable operation. In addition, the output transistors must be capable of handling twice the supply voltage because of the transformer requirements.

Another type of transistor output circuit is the **series-connected output stage**. With this type of circuit, the transistors are connected in series across the supply and the load circuit is coupled to the midpoint through a capacitor. There must be a 180-degree phase shift between the driving signals for the upper and lower transistors. A transformer can be used in this application provided that the secondary consists of two separate windings, as shown in Fig. 219. Other forms of phase splitting can be
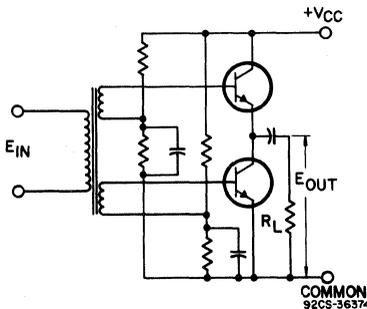
Fig.219 - Class AB, push-pull amplifier with series output connection.

used; all have problems such as insufficient swing or poor impedance matching. Capacitor output coupling also has disadvantages. A low-frequency phase shift is usually associated with the capacitor, and it is difficult to obtain a capacitor that is large enough to produce an acceptable low-frequency output. These disadvantages can be alleviated by use of a split supply and by connection of the load between the transistor midpoint and the supply mid-

point with the return path through the power-supply capacitors. The power-supply capacitors must be large enough to prevent excessive ripple.

Complementary amplifiers are produced when p-n-p and n-p-n transistors are used in series. A capacitor can be used to couple the amplifier output when a single supply is used, or direct coupling can be employed when a split power supply is used, as shown in Fig. 220. Because no phase inversion is needed in the driving circuit for this output configuration, there are definite advantages in the simplicity of the design. One disadvantage of this type of amplifier is that the driver must be a class A stage which may have a high dissipation. This dissipation can be reduced, however, by use of a Darlington compound connection for the output stage. This compound connection reduces the driving-stage requirement. A method of overcoming this disadvantage completely is to use a quasi-complementary configuration. In this configuration, the output transistors are a pair of p-n-p or n-p-n transistors driven by a complementary pair. In this manner the n-p-n/ p-n-p drivers provide the necessary phase inversion. The driving transistors are connected directly to the bases of the output transistors, as illustrated in Fig. 221.

Adequate drive may be a problem with the transistor pair shown in the upper part of the quasi-complementary amplifier unless suitable techniques are used to assure that this pair saturates. Care must also be taken when split supplies are used to assure that any ripple on the lower supply is not introduced into the predriving stages by this technique. The advantage of a split supply is that it makes possible direct connection to the load and thus
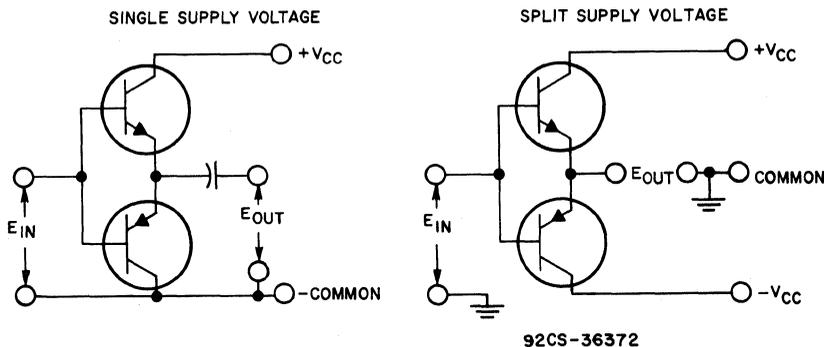
Fig.220 - Circuit arrangements for operation of complementary output stages (a) from single dc supply; (b) from symmetrical dual (positive and negative) supplies.
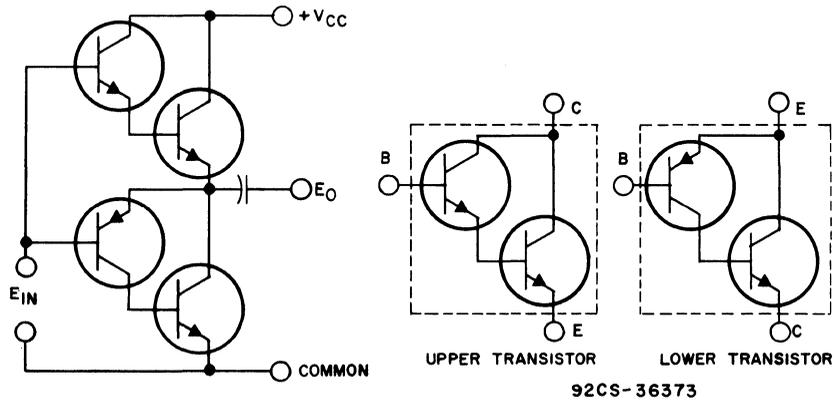
Fig.221 - Compound output stage in which output transistors are driven by complementary driver transistors: (a) over-all circuit; (b) upper transistor pair; (c) lower transistor pair.

improves low-frequency response.

To this point, **phase inversion** has been mentioned but not discussed. Phase inversion may be accomplished in many ways. The simplest electronic phase inverter is the single-stage configuration. This configuration can be used at low power levels or with high-gain devices when the limited drive capability is not a drawback. At higher power levels, some impedance transformation and gain may be required to supply the drive needed. There are several complex phase-splitting circuits; a few of them are shown in Fig. 222.

EFFECT OF OPERATING CONDITIONS ON CIRCUIT DESIGN

Some additional design problems involve the consideration of thermal stability, high line voltage, line-voltage transients, excessive drive, ambient temperature, load impedance,
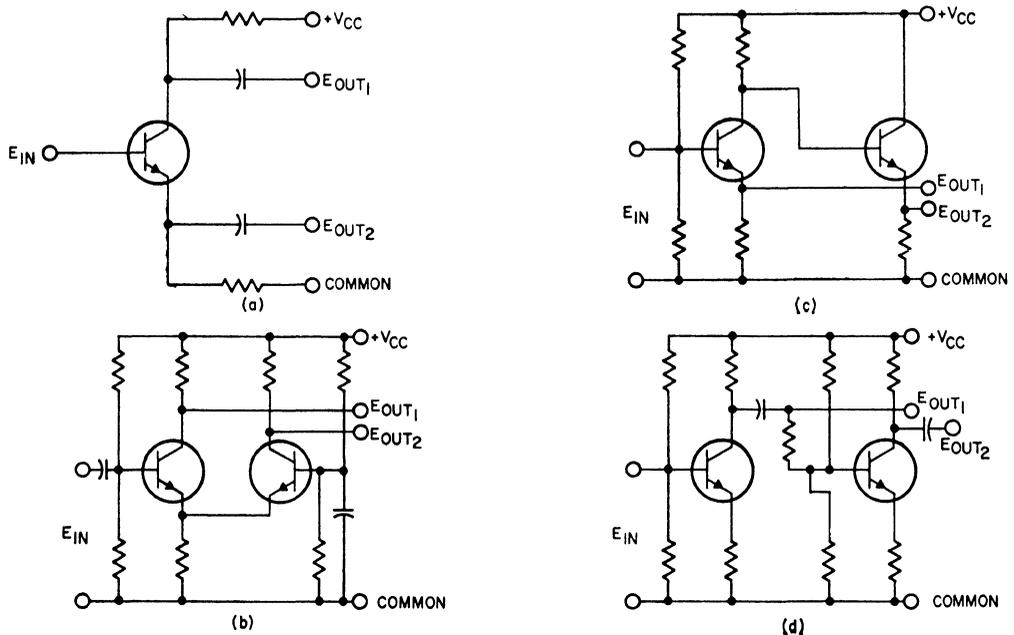
Fig.222 - Basic phase-inverter circuits: (a) single-stage phase-splitter type; (b) two-stage emitter-coupled type; (c) two-stage low-impedance type; (d) two-stage similar-amplifier type.

and other factors that may subject the transistors to abnormal high-stress conditions. A prime consideration is the maximum power dissipation at high supply voltage. Thermal stability is another problem that is often difficult to control. The problem is complex because the base-to-emitter voltage V_{BE} of a transistor decreases with an increase in junction temperature at a constant level of collector current. Therefore, if the V_{BE} of the transistor is held constant, the collector current I_C increases as the junction temperature rises. This process is regenerative because the dissipation increases with an increase in the value of I_C. One solution is to place a resistor in series with the emitter lead. This approach is not the best solution to the problem, however, because the use of the resistor increases circuit losses. A decrease in the loss may be obtained if the resistor is bypassed. Another approach is to use a thermistor or similar device which, when properly connected, reduces the base drive at high temperatures. This approach improves the stability without increasing the circuit loss.

The collector-to-base leakage current I_{CBO} can also be a problem because a fraction of this current is multiplied by the transistor h_{fe} and appears as a component of the collector-to-emitter current. In general, the value of I_{CBO} is in the order of microamperes in silicon devices and milliamperes in germanium devices. This leakage current is composed of two components. One component is caused by surface leakage and is unpredictable in its variations with temperature. It increases with voltage and may even decrease with increasing temperature. The other component is a function of the device material and geometry. This component approximately doubles with every $7°C$ temperature rise in silicon devices, and approximately doubles for every $10°C$ temperature increase in germanium devices. This component may also be voltage-dependent.

The total leakage is of interest to the circuit designer because it can be the mechanism for thermal-runaway problems. An increase in this leakage increases the total base current and thus causes an increase in collector current and dissipation. The increase in collector current and dissipation causes a rise in temperature which may produce a regenerative cycle that leads to thermal runaway. If an external resistor is connected between the base and emitter, some of this leakage current is shunted from the base, and the thermal-stability problem is reduced.

Another potential source of trouble in amplifiers is the feedback loop. Feedback is used to reduce distortion and extend the frequency range of the amplifier. The feedback loop usually encloses several if not all of the amplifier stages and can cause several problems. When transformer coupling is used, phase shifts may occur at the high- or low-frequency extremes; a positive voltage may then be fed back and cause oscillation. High-signal-level transients may cause the value of the transformer inductances and other components to change and become unstable so that they initiate oscillation. A similar condition can occur at low frequencies when capacitor-coupled transformerless designs are used.

Excessive drive levels at high frequencies can cause dissipation problems. An excessive drive level forces the output stages to saturate before the peak of the input signal is reached. This additional drive lengthens the storage time which, at high frequencies, may approach the period of the drive signal. Under this condition, two results occur: First, feedback does not increase after the point where the output stage saturates. This condition permits the drive signal to increase. Second, one transistor may not turn off until the second has been turned on. In series-type output stages, the second transistor is turned on with the full supply voltage present. This condition can lead to forward-bias second-breakdown problems.

Another potential source of difficulty with amplifiers occurs when the output is open- or short-circuited. Transformer-coupled output stages are particularly susceptible to operational problems with no load. Without a load, the transistors operate into a purely inductive load line and the probability of reverse-bias second breakdown must be considered. In series-type output stages, the major problem arises under short-circuit load conditions. As a result of the short circuit, feedback is removed and an open-loop gain condition exists together with the excessive-drive-condition problems previously mentioned. It is advisable to use some form of fast-acting overload protection for the power transistor; a fuse is usually not fast enough in this application.

Some frequency exists at which the gain of any transistor begins to decrease. This decrease in gain can be corrected over the required frequency range by use of feedback or a higher-frequency device. Roll-off of the frequency response of the preamplifier stages at some point prior to the limiting value of the frequency characteristics of the transistor is necessary. This technique assures that the drive is limited to a safe value by the input stage so that even the drivers are not affected by the high dissipation mentioned previously.

Several other factors that should be considered in the design of amplifiers for audio-frequency service include the frequency response desired, gain, optimum load, noise, and power output needed.

BASIC CIRCUIT CONFIGURATIONS

The selection of the basic circuit configuration for an audio power amplifier is dictated by the particular requirements of the intended application. The selection of the basic circuit configuration that provides the desired performance most efficiently and economically is based primarily upon the following factors: power output to be supplied, required sensitivity and frequency-response characteristics, maximum allowable distortion, and capabilities of available devices.

Class A Transformer-Coupled Amplifiers

Fig. 223 shows a three-stage class A transformer-coupled audio amplifier that uses dc feedback (coupled by R_1, R_2, R_3, R_4, and C_1) from the emitter of the output transistor to the base of the input transistor to obtain a stable operating point. An output capability of 5 watts with a total harmonic distortion of 3 per cent is typical for this type of circuit. In general, this output level is the upper limit for class A amplifiers because the power dissipated by the output transistor in such circuits is more than twice the output power. For this reason, it is economically impractical to use class A audio amplifiers to develop higher levels of output power. A circuit such as the one shown in Fig. 223 usually requires no over-all feedback unless extremely low distortion is required. Local feedback in each stage is adequate; amplifiers of this type, therefore, are usually very stable.

Class AB Push-Pull Transformer-Coupled Amplifiers

At power-output levels above 5 watts, the operating efficiency of the circuit becomes an important factor in the design of audio power amplifiers. The circuit designer may then consider a class AB push-pull amplifier for use as the audio-output stage.

Fig. 224 shows a class AB push-pull transformer-coupled audio-output stage. Re-
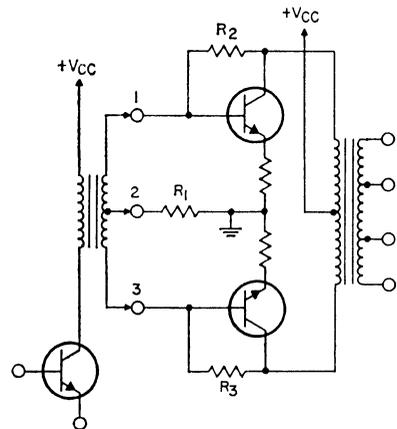
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Fig.224 - Class AB, push-pull, transformer-coupled audio output stage.

sistors R_1, R_2, and R_3 form a voltage divider that provides the small amount of transistor forward bias required for class AB operation. The transformer type of output coupling used in the circuit is advantageous in that a suitable output transformer can be selected to match the audio system to any desired load impedance. This feature assures maximum transfer of the audio-output power to the load circuit, which is especially important in sound-distribution systems that use high-impedance transmission lines to reduce losses. A

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Fig.223 - Three-stage transformer-coupled, class A amplifier.

major disadvantage of transformer output coupling is that it tends to limit the amplifier frequency response, particularly at the low-frequency end. Variations in transformer impedance with frequency may produce significant phase shifts in the signal at both frequency extremes of the amplifier response. Such phase shifts are potential causes of amplifier instability if they occur within the feedback loop. Open-circuit stability is always a problem in designs that use output transformers because the gain increases sharply when the load is removed. If too much over-all feedback is employed, the amplifier may oscillate. The local feedback caused by the bias arrangement of R_2 and R_3 helps to eliminate this problem.

Push-pull output stages, which use identical output transistors, require some form of phase inversion in the driver stage. In the circuit shown in Fig. 224, a center-tapped driver transformer is used for this purpose. The requirements of this transformer depend upon the power levels involved, the bandwidth required, and the distortion that can be tolerated. This transformer also introduces phase-shift problems that tend to cause instabilities in the circuit when high levels of feedback are employed. Phase-shift problems are substantially reduced when the output stage is designed to operate at low drive requirements. The reduced drive requirements can be achieved by use of the Darlington circuit shown in Fig. 225. Resistors R_1 and R_2
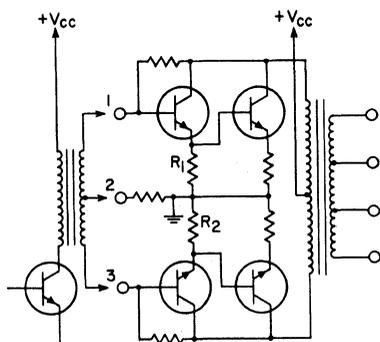
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Fig. 225 - Class AB, push-pull, transformer-coupled audio output stage in which Darlington pairs are used to reduce drive requirements of output transistors.

shunt the leakage of the driver and also permit the output transistors to turn off more rapidly. Impedance levels between the class A driver and the output stage can be easily matched by the use of an appropriate transformer turns ratio.

An alternative method of phase inversion is to use a transistor in a phase-splitter circuit, such as those shown in Fig. 222 and described later in the discussion on **Phase Inverters**. Unlike the center-tapped transformer method, impedance matching may be a problem because the collector of the driver, which has a relatively high impedance, operates into the low input impedance of the output stage. One solution is to reduce the output impedance of the driver stage by the use of smaller resistors. The resultant increase in collector current, however, also increases the dissipation. Moreover, very large coupling capacitors are necessary for the achievement of good low-frequency performance. The nonlinear impedance exhibited by the input of the output transistor causes a dc voltage to be produced across the capacitor under high signal levels. An alternate solution is to use a Darlington pair to increase the input impedance of the output stage.

Class AB Series-Output Amplifiers

For applications in which low distortion and wide frequency response are major requirements, a transformerless approach is usually employed in the design of audio power amplifiers. With this approach, the common type of circuit configuration used is the series-output amplifier.

The class-AB-operated n-p-n transistors used in the series-output circuits shown in Fig. 226 require some form of phase inversion of the drive signal for push-pull operation. A common approach is to use a driver transformer that has split secondary windings, as shown in Fig. 227. The split secondary windings are required because of the mode in which each of the series output transistors operates.

If ground were used as the drive reference for both secondary windings of the circuit shown in Fig. 227, transistor Q_1 would operate as an emitter-follower and would provide gain of somewhat less than unity. Transistor Q_2, however, is connected in a common-emitter configuration which can provide substantial voltage gain. For equal output-voltage swings in both directions, the drive input to transistor Q_1 is applied directly across the base and
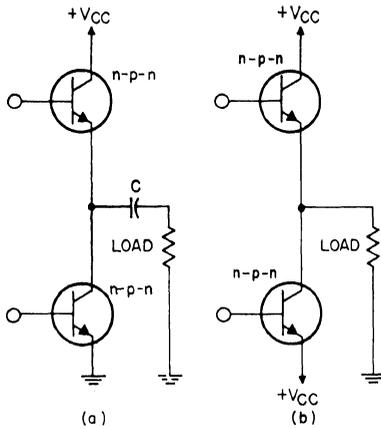
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Fig.226 - Circuit arrangements for operation of series output circuit from (a) a single dc supply and (b) symmetrical dual supplies.

emitter terminals. Transistor Q_1 is then effectively operated in a common-emitter configuration (although there is no phase reversal from input to output) and has a voltage gain equal to that of transistor Q_2.
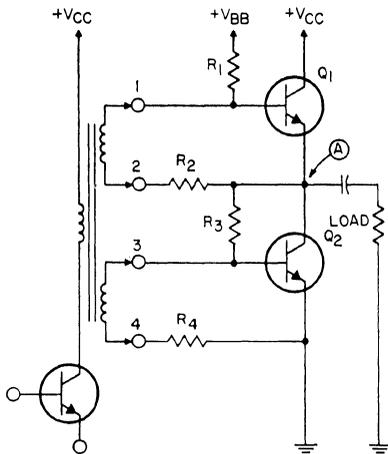
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Fig.227 - Circuit using a driver transformer that has split secondary windings to provide phase inversion for push-pull operation of a series-output circuit.

The disadvantages of a driver transformer discussed previously also apply to the circuit shown in Fig. 227. In addition, coupling through interwinding capacitances can adversely affect the performance of the circuit. Such coupling is particularly serious because

at both ends of the upper secondary (terminals 1 and 2) the ac voltage with respect to ground is approximately equal to the output voltage. During signal conditions, when output transistor Q_1 is turned on, this coupling provides an unwanted drive to Q_1. The forward transistor bias required to maintain class AB circuit operation is provided by the resistive voltage divider R_1, R_2, R_3, and R_4. These resistors also assure that the output point between the two transistors (point A) is maintained at one-half the dc supply voltage V_{CC}.

As in the case of the transformer-coupled output, phase inversion can be accomplished by use of an additional transistor. Fig. 228 shows a circuit in which the transistor phase inverter is used, together with a Darlington output stage to minimize loading on the phase inverter. It should be noted that capacitor C provides a drive reference back to the emitter of the upper output transistor. In effect, this arrangement duplicates the drive conditions of the split-winding transformer approach. A disadvantage of this circuit is the high-quiescent dissipation of the phase inverter Q_1 which is necessary to obtain adequate drive at full power output.
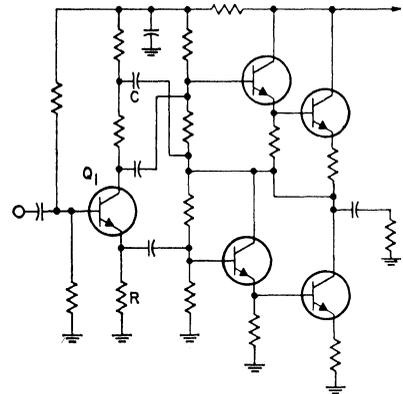
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Fig.228 - Push-pull series-output amplifier in which driver and output transistors are connected as Darlington pairs and drive-signal phase inversion is provided by phase-splitter stage Q_1.

An unbypassed emitter resistor R is necessary because a signal is derived from this point to drive the lower output transistor. When transistor Q_1 is driven into saturation, the minimum collector-to-ground voltage that

can be obtained is limited primarily by the peak emitter voltage under these conditions. To obtain the necessary voltage swing at this collector (a voltage swing that is also approximately equal to the output voltage swing), it is necessary to use a quiescent collector-to-emitter voltage higher than that required in a stage that uses a bypassed emitter resistor.

Complementary-Symmetry Amplifiers

When a complementary pair of output transistors (n-p-n and p-n-p) is used, it is possible to design a series-output type of audio power amplifier which does not require push-pull drive. Because phase inversion is unnecessary with this type of configuration, the drive circuit for the amplifier is simplified substantially. Fig. 229 shows a basic complementary type of series-output circuit together with a simple class A driver stage. The voltage drop across resistor R provides the small amount of forward bias required for class AB operation of the complementary pair of output transistors.
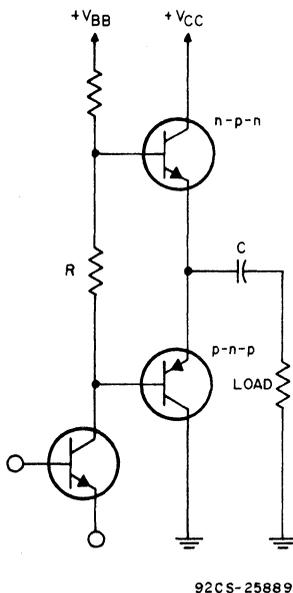
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Fig.229 - Basic complementary type of series-output circuit with class A driver.

In practice, a diode is employed in place of resistor R. The purpose of the diode is to maintain the quiescent current at a reasonable value with variations in junction temperatures. It is usually thermally connected to one of the output transistors and tracks with the V_{BE} of the output transistors.

The complementary circuit is by far the most thermally stable output circuit. It places the output transistors in a V_{CES} mode because both transistors are operated with a low impedance between base and emitter. Therefore, the I_{CBO} leakage is the only component of concern in the stability criteria. At power-output levels from 3 to 20 watts, a complementary-symmetry amplifier offers advantages in terms of circuit simplicity. At higher power levels, however, the class A driver transistor is required to dissipate considerable heat, the quiescent power-supply current drain becomes significant, and excessively large filter capacitors are required to maintain a low hum level. This dissipation can be reduced, however, by use of a Darlington compound connection for the output stage. This compound connection reduces the driving-stage requirement.

There are two basic methods of overcoming this disadvantage entirely. The first is to use a quasi-complementary configuration; the second is to employ the compound true complementary-symmetry amplifier circuit shown in Fig. 230. Both methods replace the class A driver with a complementary driver stage. The circuit of Fig. 230 also employs a complementary grounded-base predriver stage which reduces static current drain even further. With this circuit it is practical to obtain power levels of over 100 watts with paralleled output transistors. For higher power levels, the quasi-complementary circuit is generally used because of the unavailability of higher power complementary devices.

Quasi-Complementary-Symmetry Amplifiers

In the quasi-complementary amplifier shown in Fig. 231, the driver transistors provide the necessary phase inversion. A simple but descriptive way to analyze the operation of a quasi-complementary amplifier is to consider the result of connecting a p-n-p transistor to a high-power n-p-n output transistor, as shown in Fig. 232. The collector current of the p-n-p transistor becomes the base current of the n-p-n transistor. The n-p-n transistor, which is operated as an emitter-follower, provides additional current gain without inversion. If the emitter of the n-p-n transistor is considered as the "effective" collector of the composite circuit, it becomes apparent that the circuit is equivalent to a high-gain, high-power p-n-p transistor.
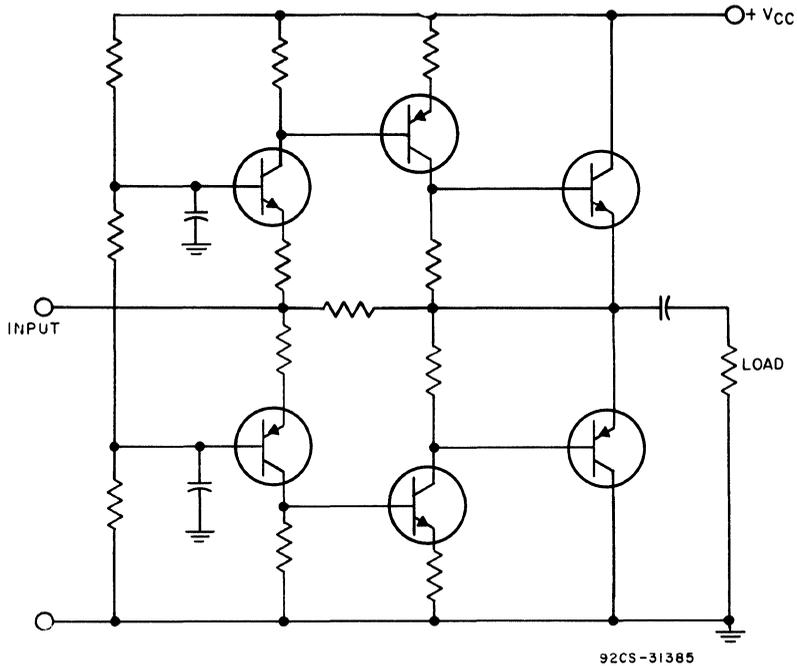
Fig.230 - Basic complementary type of
series-output circuit with comple-
mentary type driver and predriver.

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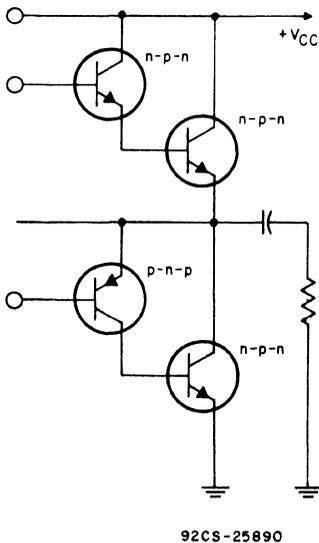
Fig.231 - Basic quasi-complementary type
of series-output circuit.

The output characteristics of the p-n-p
circuit shown in Fig. 232 and of a high-gain,
high-power n-p-n circuit formed by the
connection of the same type of n-p-n output
transistor and an n-p-n driver transistor in a
Darlington configuration, such as shown in
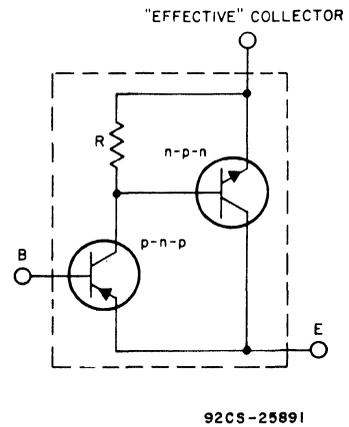
Fig.232 - Connection of p-n-p driver tran-
sistor to n-p-n output transistor.

Fig. 233, are compared in Fig. 234.

The saturation characteristics of the over-
all circuit in both cases are the combination of
the base-to-emitter voltage V_{BE} of the output
transistor and the collector saturation voltage
of the driver transistor. Moreover, in both
cases the current gain is the product of the
individual betas of the transistors used. A
quasi-complementary amplifier, therefore, is
effectively the same as a simple complementary
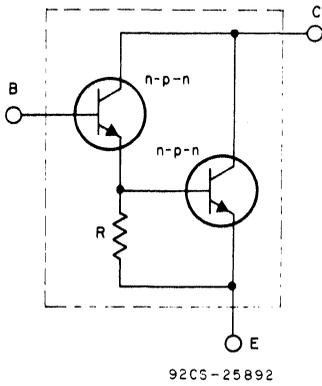
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Fig.233 - Darlington connection of n-p-n driver transistor to n-p-n output transistor.
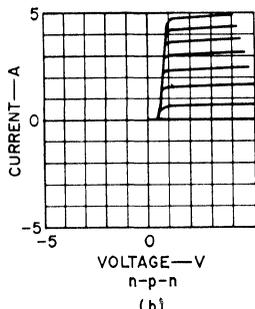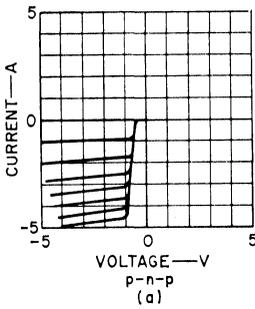
Fig.234 - Output characteristics for (a) p-n-p/n-p-n driver-output transistor pair shown in Fig. 232 and for (b) Darlington pair of n-p-n transistors shown in Fig. 233.

output circuit such as that shown in Fig. 229, and is formed by the use of high-gain, high-power n-p-n and p-n-p equivalent transistors. In both cases, the resistor R between the emitter and base of the output transistor places the device in a V_{CER} mode. This mode is not as stable as that of the complementary amplifier, but present no problem for silicon transistors.

A typical quasi-complementary amplifier is shown in Fig. 235. Capacitor C performs two functions essential to the successful operation of the circuit. First, it acts as a bypass to decouple any power-supply ripple from the driver and predriver stages. Second, it is connected as a "boot-strap" capacitor to provide the drive necessary to pull the upper Darlington pair of transistors into saturation. This latter function results from the fact that the stored voltage of the capacitor, with reference to the output point A, provides a higher voltage than the normal collector-supply voltage to drive transistor Q2. This higher voltage is necessary during the signal conditions that exist when the upper transistors are being turned on because the emitter voltage of transistor Q_2 then approaches the normal supply voltage. An increase in the base voltage to a point above this level is required to drive the transistor into saturation. Resistor R_1 provides the necessary dc feedback to maintain point A at approximately one-half the nominal supply voltage. Over-all ac feedback from output to input is coupled by resistor R_2 to reduce distortion and to improve low-frequency performance.
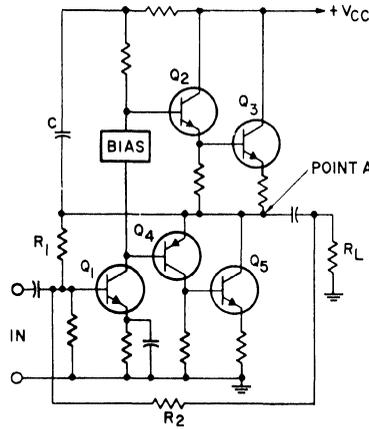
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Fig.235 - Quasi-complementary audio power amplifier that operates from a single dc supply.

Series-output circuits can be employed with separate positive and negative supplies; no series output capacitor is then required. The elimination of this capacitor may result in an economic advantage, even though an additional power supply is used, because of the size

of the series output capacitor necessary in the single-supply case to obtain good low-frequency performance (e.g., a 2000-microfarad capacitor is required to provide a 3-dB point at 20 Hz for a 4-ohm load impedance). Split supplies, however, pose certain problems which do not exist in the single-supply case. The output of the amplifier must be maintained at zero potential under quiescent conditions for all environmental conditions and device parameter variations. Also, the input ground reference can no longer be at the same point as that indicated in Fig. 235, because this point is at the negative supply potential in a split-supply system.

If the ground-point reference for the input signal were a common point between the split supplies, any ripple present on the negative supply would effectively drive the amplifier through transistor Q_1, with the result that this stage would operate as a common-base amplifier with its base grounded through the effective impedance of the input signal source. To avoid this condition, the amplifier must include an additional p-n-p transistor as shown in Fig. 236. This transistor (Q_6) reduces the drive effects of the negative supply ripple because of the high collector impedance (1 megohm or more) that it presents to the base of transistor Q_1, and effectively isolates the input source impedance from transistor Q_1. In

practice, transistor Q_1 may be replaced by a Darlington pair to reduce the loading effects on the p-n-p predriver.

Negative dc feedback is applied from the output to the input stage by R_1, R_2, and C_1 so that the output is maintained at about zero potential. Actually, the output is maintained at approximately the forward-biased base-emitter voltage of transistor Q_6, which may be objectionable in a few cases, but which can be eliminated by a method discussed later. Capacitor C_1 effectively bypasses the negative dc feedback at all signal frequencies. Resistor R_3 provides ac feedback to reduce distortion in the amplifier.

True Complementary Symmetry Amplifiers

The true complementary symmetry amplifier shown in Fig. 237 has better thermal stability than other dc-coupled circuits, because transistors Q2 and Q5 are driven from the same low-impedance source. Forward bias for both transistors is provided by Q3, and is adjustable.

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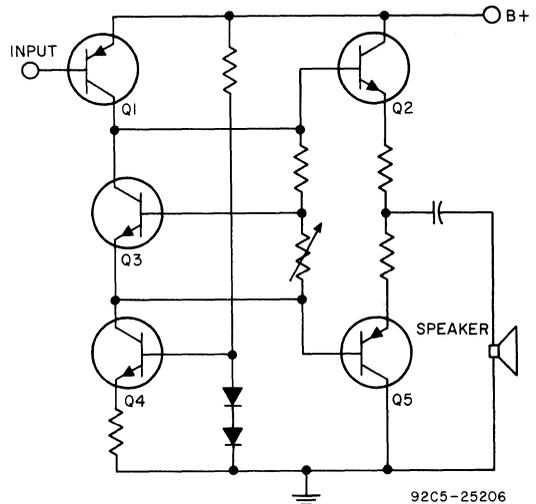
Fig.237 - True-complementary-symmetry amplifier.

Conjugate Complementary-Symmetry Amplifiers

Fig. 238 compares a transformer-coupled class AB amplifier to a **conjugate complementary amplifier**. The elimination of the transformer in the conjugate complementary amplifier, in the quasi-complementary amplifier and the true complementary amplifier shown in Fig. 237 permits a lighter-weight, less costly construction and eliminates the

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Fig.236 - Quasi-complementary audio power amplifier that operates from symmetrical dual dc power supplies. The p-n-p transistor input stage is required to prevent ripple component from driving amplifier.

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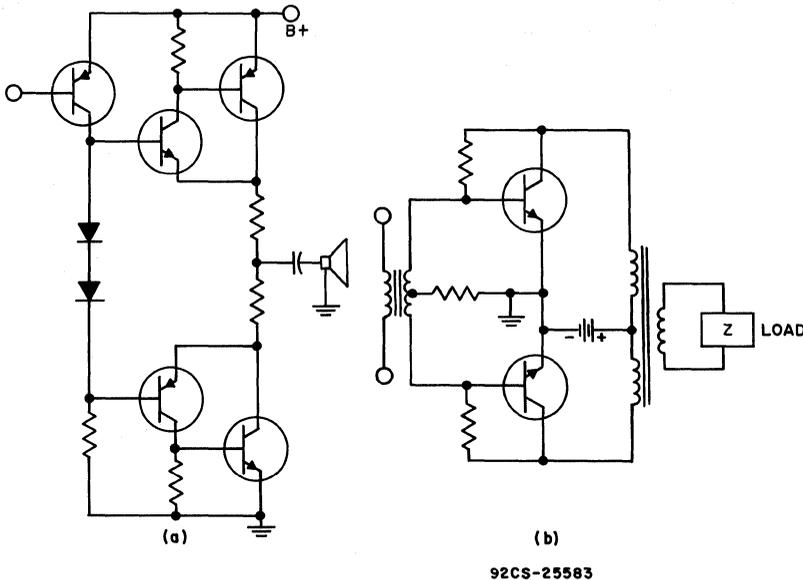
*Fig.238 - (a) Conjugate-complementary-
symmetry and (b) transformer-
coupled amplifiers.*

phase shifts and stability problems normally associated with transformers. The main advantage of a transformer-coupled circuit is easier matching of transistor volt-ampere capability to various load impedances.

Bridge Amplifiers

Fig. 239 shows the block diagram of an audio-amplifier configuration that, for a given dc supply voltage, transistor voltage-breakdown capability, and load, can provide four times the power output obtainable from a conventional push-pull audio-output stage. Alternatively, given power-output and load requirements may be achieved from this circuit

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*Fig.239 - Block diagram of bridge type of
audio-amplifier circuit.*

configuration with half the supply voltage and transistor voltage-breakdown capabilities required of conventional circuits. This performance is possible because the load can swing the full supply voltage on each half-cycle. The load is direct-coupled between the center point of two series-connected push-pull stages. This bridge type of arrangement eliminates the need for expensive coupling capacitors or transformers. These features are very attractive in applications for which the supply voltage is fixed, such as automotive or aircraft supplies.

The bridge-amplifier configuration consists essentially of two complementary-symmetry amplifiers with the load direct-coupled between the two center points. Each amplifier section is driven by a class A driver stage that uses a transistor Darlington pair. The amplifiers must be driven 180 degrees out of phase. This dual-phase drive is provided by a differential-amplifier type of input stage, which also provides the advantage of a high input impedance.

Fig. 240 shows the basic configuration of an experimental breadboard circuit designed to evaluate the bridge-amplifier approach to audio-amplifier design. The major difference between this type of circuit and the conventional complementary-symmetry circuit, besides the increased output power, is the higher current requirements of the class A driver
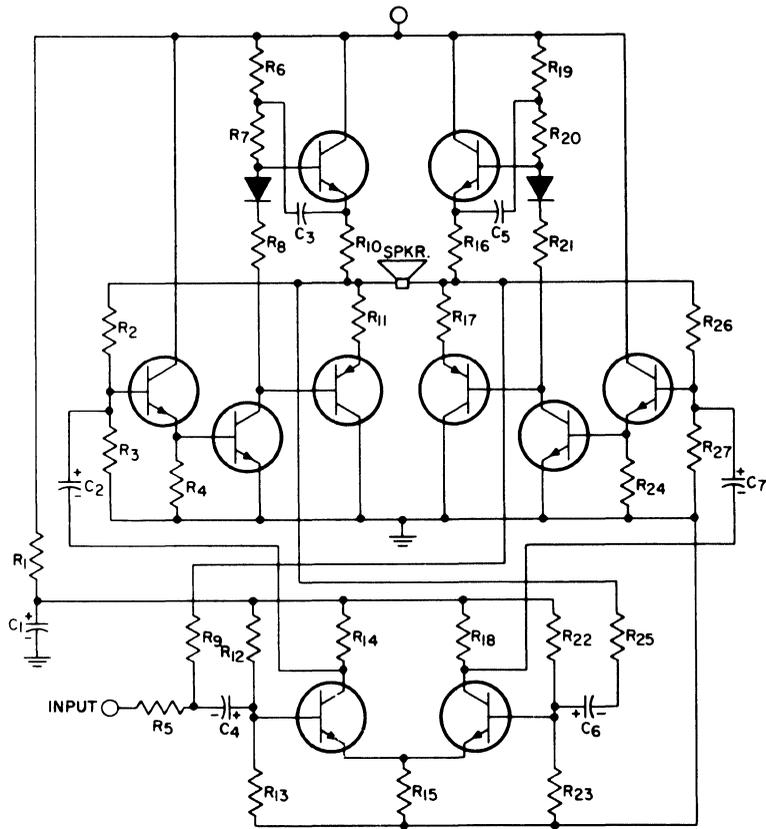
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*Fig.240 - Basic circuit configuration for a
bridge type of audio amplifier.*

stages. This current is twice the value normally required because the peak value of the output current is doubled. The feedback network from each complementary-symmetry output section back to the base of the corresponding class A driver stage, which establishes the center-point voltage in the output stage, also provides a minimum of 22 dB of ac feedback.

One problem encountered in the bridge amplifier is the achievement of a zero center-point (offset) voltage. The load circuit conducts a direct current proportional to the difference (offset) between the voltages at the two output stages. The dc dissipation in the load circuit is, of course, proportional to the square of the offset voltage. In this breadboard circuit, two potentiometers are used to balance the center-point voltage of the two output-stage sections.

The differential-amplifier input stage operates at ten times the required value of peak input current to assure linear operation. Balanced feedback is taken from each side of

the load and coupled back to the separate bases of the differential-amplifier transistors. Fig. 241 shows curves of total harmonic distortion as a function of power output for operation of the bridge amplifier with 0 dB, 20 dB, and 28 dB of balanced feedback. Figs. 242 and 243 show total harmonic distortion and relative response as functions of frequency for the bridge amplifier operated with 20 dB of balanced feedback.

Phase Inverters

Phase inversion may be accomplished in many ways. The simplest electronic phase inverter is the single-stage configuration. This configuration can be used at low power levels or with high-gain devices when the limited drive capability is not a drawback. At higher power levels, some impedance transformation and gain may be required to supply the drive needed. There are several complex phase-
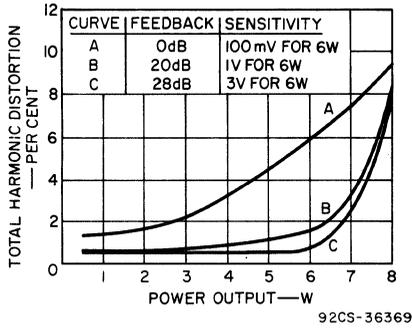
Fig.241 - Total harmonic distortion (at 1 kHz) of the bridge audio amplifier as a function of power output for different values of balanced loop feedback. (Distortion performance is comparable to that of a single-ended amplifier that provides one-quarter of the power output for the same dc supply voltage).
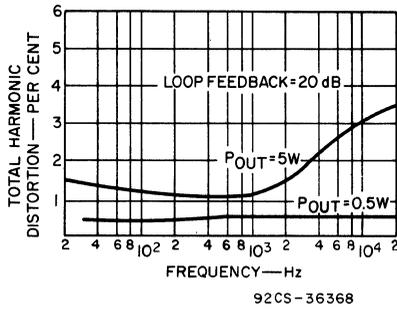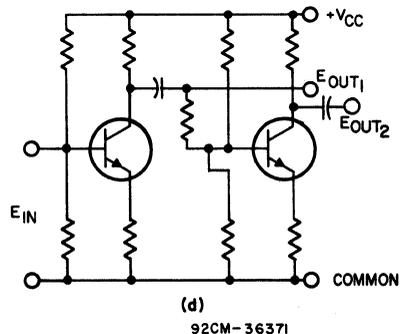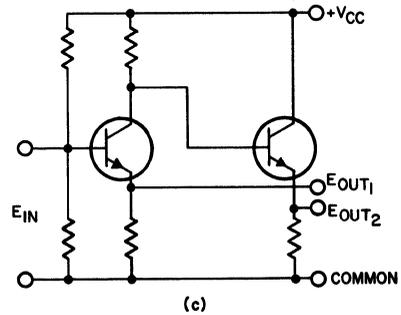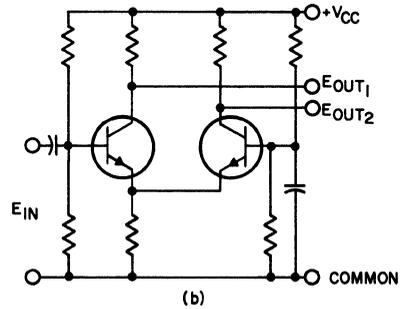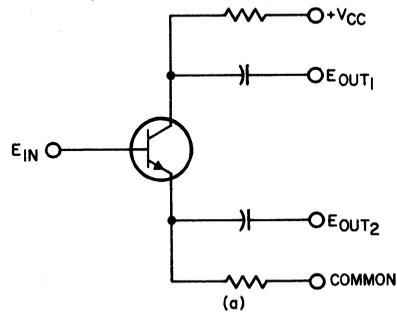
Fig.242 - Total harmonic distortion of the bridge audio amplifier as a function of frequency.
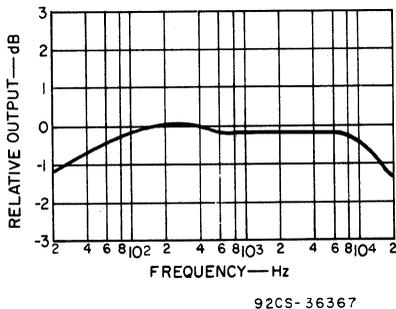
Fig.243 - Relative response of the bridge audio amplifier.

Fig.244 - Basic phase-inverter circuits: (a) single-stage phase-splitter type; (b) two-stage emitter-coupled type; (c) two-stage low-impedance type; (d) two-stage similar-amplifier type.

splitting circuits; a few of them are shown in Fig. 244.

POWER OUTPUT IN CLASS B AUDIO AMPLIFIERS

For all cases of practical interest, the power output (P_o) of an audio amplifier is given by the following equation:

$$P_o = I(rms) \times E(rms) = (I_p E_p)/2$$
$$= (I_p^2 R_L)/2 = E_p^2/2R_L$$

where I_p and E_p are the peak load current and voltage, respectively, and R_L is the load impedance presented to the transistor. Fig. 245 shows the relationship among these various factors in graphic form. Obviously, the peak load current is the peak transistor current, and the transistor breakdown-voltage rating must be at least twice the peak load voltage. The vertical lines that denote 4-ohm, 8-ohm, and 16-ohm resistances are particularly useful for transformerless designs in which the transistor operates directly into the loudspeaker.

Rating Methods

The **Institute of High Fidelity** (IHF) and the **Electronic Industries Association** (EIA) have attempted to standardize power-output ratings to establish a common reference of comparison and to provide a solid definition of the capabilities of audio power amplifiers. Obviously, an audio power amplifier using an unregulated supply can deliver more output power under transient conditions than under steady-state conditions. The rating methods which have been standardized for this type of operation are the **IHF Dynamic Output Rating (IHF-A-201)** and the **EIA Music Power Rating (EIA RS-234-A)**.

Both of these measurement methods allow the use of regulated supply voltage to simulate transient conditions. Because the regulated supply has no source impedance or ripple, the results do not completely represent the transient conditions, as will be explained later.

Measurement Techniques

The EIA standard is used primarily by manufacturers of packaged equipment, such
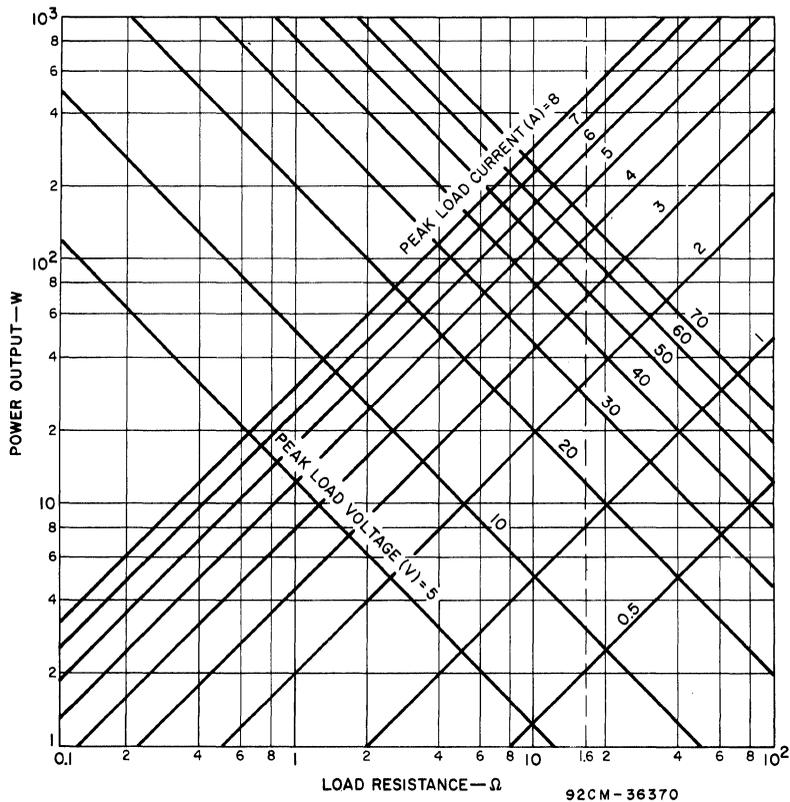
Fig.245 - Peak transistor currents and load voltages for various output powers and load resistances.

as portable phonographs, packaged stereo hi-fi consoles, and packaged home-entertainment consoles. The **EIA music power output** is defined as the power obtained at a total harmonic distortion of 5 per cent or less, measured after the "sudden application of a signal during a time interval so short that supply voltages have not changed from their no-signal values." The supply voltages are bypassed voltages. These definitions mean that the internal supply may be replaced with a regulated supply equal in voltage to the no-signal voltage of the internal supply. For a stereo amplifier, the music power rating is the sum of both channels, or twice the single-channel rating.

The IHF standard provides two methods to measure dynamic output. One is the **constant-supply method**. This method assumes that under music conditions the amplifier supply voltages undergo only insignificant changes. Unlike the EIA method, this measurement is made at a reference distortion. The constant-supply method is used by most high-fidelity component manufacturers. The reference distortion chosen is normally less than one per cent, or considerably lower than the EIA value of 5 per cent used by packaged-equipment manufacturers.

A second IHF method is called the **"transient distortion" test**. This method requires a complex setup including a low-distortion modulator with a prescribed output rise time and other equipment. The modulator output is required to have a rise time of 10 to 20 milliseconds to simulate the envelope rise time of music and speech. This measurement is made using the internal supply of the amplifier and, consequently, includes distortion caused by voltage decay, power-supply transients, and ripple. This method tends to be more realistic, and to yield lower power-output ratings than the constant-supply method. Actually, both IHF methods should be used, and the lowest power rating obtained at reference distortion with both channels operating, both in and out of phase, should be used as the power rating. (There is some question concerning unanimity among high-fidelity manufacturers on actually performing both IHF tests.)

Because music is not a continuous sine wave, and has average power levels much below peak power levels, it would appear that the music power or dynamic power ratings are true indications of a power amplifier's ability to reproduce music program material. The problem is that all three methods described have a common flaw. Even the transient-distortion method fails to account for the ability of the audio amplifier to reproduce power peaks while it is already delivering some average power. The amplifier is almost never delivering zero output when it is called on to deliver a transient. For every transient that occurs after an extremely quiet passage or zero signal, there are hundreds that are imposed on top of some low but non-zero average power level.

This condition can best be clarified by consideration of the power supply. Many amplifiers have regulated supplies for the front-end or low-level stages, but almost none provides a regulated supply for the power-output stages because regulation requires extra transistors or other devices; it becomes costly, especially at high power levels. The power supply for the output stages of power amplifiers is commonly a nonregulated rectifier supply having a capacitive input filter. The output voltage of such a supply is a function of the output current and, consequently, of the power output of the amplifier.

Effect of Power-Supply Regulation

Power-supply regulation is dependent on the amount of effective internal series resistance present in the power supply. The effective series resistance includes such things as the dc resistance of the transformer windings, the amount and type of iron used in the transformer, the amount of surge resistance present, the resistance of the rectifiers, and the amount of filtering. The internal series resistance causes the supply voltage to drop as current is drawn from the supply

Fig. 246 shows a typical regulation curve for a rectifier power supply that has a capacitive input filter. The voltage is a linear function of the average supply current over most of the useful range of the supply. However, a rapid change in slope occurs in the regions of both very small and very large currents. In class B amplifiers, the no-signal supply current normally occurs beyond the low-current knee, and the current required for the amplifier at the clipping level occurs before the high-current knee. The slope between these points is nearly linear and may be used as an approximation
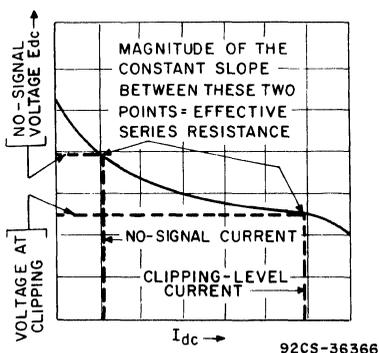
Fig.246 - Regulation curve for capacitive rectifier power supply.

of the equivalent series resistance of the supply.

The amount of power lost depends on the quality of the power supply used in the amplifier. Accordingly, rating amplifier power output with a superb **external** power supply (that is, not using the built-in amplifier power supply) provides false music power outputs. Under actual usage, the output is lower.

It should be emphasized that, while there is a discrepancy between the actual power measured under the EIA Music Power or the IHF Dynamic Power methods, these methods are not without merit. The IHF dynamic power rating, in conjunction with the continuous power rating, produces an excellent indication of how the amplifier will perform. The EIA music power rating, which is measured at a total harmonic distortion of 5 per cent with a regulated power supply, provides a less adequate indication of amplifier performance because there is no indication of how the amplifier power-supply voltage reacts to power output.

Some important factors considered by packaged-equipment manufacturers, the primary users of the EIA music power ratings, are mostly economic in nature and affect many aspects of the amplifier performance. Because there is no continuous power output rating required, two amplifiers may receive the same EIA music power rating but have different continuous power ratings. The ratio of music power to continuous power is, of course, a function of the regulation and effective series resistance of the supply.

One reason for the difference between ratings used by the console or the packaged-equipment manufacturer and those used by the hi-fi

component manufacturer is that the latter does not always know just what will be required of the amplifier. The console manufacturer always designs an amplifier as part of a system, and consequently knows the speaker impedances and the power required for adequate sound output. The console manufacturer may use high-efficiency speakers requiring only a fraction of the power needed to drive many component-type acoustic-suspension systems. The difference may be such that the console may produce the same sound pressure level with an amplifier having one-tenth of the power output. High ratios of music-power to continuous-power capability are common in these consoles. A typical ratio of IHF music power to continuous power may be 1.2 to 1 in component amplifiers, whereas a typical ratio of EIA music power to continuous power in a console system may be 2 to 1. Console manufacturers use the EIA music power rating to economic advantage as a result of the reduced regulation requirement of the power supply. A high ratio of music power to continuous power means higher effective series resistance in the power supply. This resistance, in turn, means less continuous dissipation on the output transistors, smaller heat sinks, and a lower-cost power supply.

Ratio of Music Power to Continuous Power

Some advantages of high values of the ratio R_S/R_L and correspondingly high ratios of music power output to transistor dissipation are as follows:

1. Reduced heat sink or transistor cost: Because the volt-ampere capacity of the transistor is determined by the music power output, it is not likely that reduced thermal-resistance requirements will produce significant cost reductions. Alternatively, the heat-sink requirements may be reduced.

2. Reduced power supply costs: Transformer and/or filter-capacitor specifications may be relaxed.

3. Reduced speaker cost: Continuous power-handling capability may be relaxed.

These cost reductions may be passed along to the consumer in the form of more music power per dollar.

The question arises as to how high the ratio R_S/R_L and the corresponding ratio of music power output to continuous power output may be before the capability of the amplifier to reproduce program material is impaired.

The objective is to provide the listener with a close approximation of an original live performance. Achievement of this objective requires the subjective equivalents of sound pressure levels that approach those of a concert hall. Although the peak sound pressure level of a live performance is about 100 dB, the average listener prefers to operate an audio system at a peak sound pressure level of about 80 dB. The amplifier, however, should also accommodate listeners who desire higher-than-average levels, perhaps to peaks of 100 dB.

A sound pressure level of 100 dB corresponds to about 0.4 watt of acoustic power for an average room of about 3,000 cubic feet.

If speaker efficiencies are considered to be in the order of 1 per cent, a stereophonic amplifier must be capable of delivering about 20 watts per channel. Higher power outputs are required for lower-efficiency speakers. The peak-to-average level for most program material is between 20 and 23 dB. A system capable of providing a continuous level of 77 dB and peaks of 100 dB would satisfy the power requirements of nearly all listeners. For this performance to be attained, the power-supply voltage cannot drop below the voltage required for 100 dB of acoustic power while delivering the average current required for 77 dB. Moreover, because sustained passages that are as much as 10 dB above the average may occur, the power-supply voltage cannot drop below the value required for 100 dB of acoustic power while delivering 87 dB of acoustic power (87 dB of acoustic power corresponds to about 1 watt per channel). This performance means that for 8-ohm loads, with output-circuit losses neglected, the power-supply voltage must not decrease to a value less than 36 volts, while delivering the average current required for 1 watt per channel (0.225 ampere dc).

It should be noted that the power-output capability for peaks while the amplifier is delivering a total of 2 watts is not the music power rating of the amplifier because the power-supply voltage is below its no-signal value by an amount depending on its effective series resistance.

THERMAL-STABILITY REQUIREMENTS

One serious problem that confronts the design engineer is the achievement of a circuit which is thermally stable at all temperatures to which the amplifier might be exposed. As previously discussed, thermal runaway may be a problem because the V_{BE} of all transistors decreases at low current. It should be noted, however, that at high current levels the base-to-emitter voltage of silicon transistors increases with a rise in junction temperature. This characteristic is the result of the increase in the base resistance that is produced by the rise in temperature. The increase in base resistance helps to stabilize the transistor against thermal runaway. In high-power amplifiers, the emitter resistors employed usually have a value of about 1 ohm or less. The size of the capacitor required to bypass the emitter adequately at all frequencies of interest makes this approach economically impractical. A more practical solution is to increase the value of the emitter resistor and shunt it with a diode. With this technique, sufficient degeneration is provided to improve the circuit stability; at low currents, however, the maximum voltage drop across the emitter resistor is limited to the forward voltage drop of the diode.

The quasi-complementary amplifier shown in Fig. 247 incorporates the stabilization
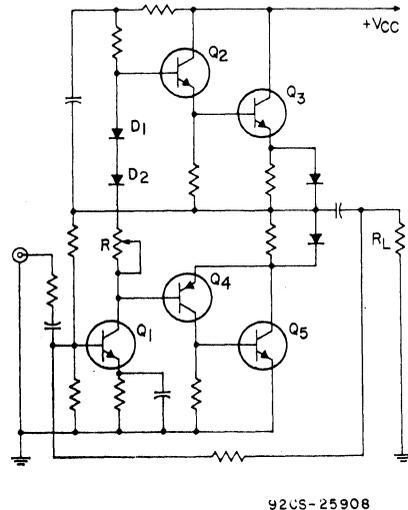
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Fig.247 - Quasi-complementary amplifier that incorporates two stabilization networks.

techniques described. A resistor-diode network is used in the emitter of transistor Q_3, and another such network is used in the collector of transistor Q_5, with the emitter of transistor Q_4 returned to the collector of transistor Q_5. Previous discussion regarding the p-n-p driver and n-p-n output combination (Q_4 and Q_5) showed that the collector of the output device becomes the "effective" emitter of the high-gain, high-power p-n-p equivalent, and vice versa. For maximum operating-point stability, therefore, the diode-resistor network should be in the "effective" emitter of the p-n-p equivalent. Quasi-complementary circuits employing the stabilization resistor in the emitter of the lower output transistor do not improve the operating-point stability of the over-all circuit.

The circuit shown in Fig. 247 is biased for class AB operation by the voltage obtained from the forward drop of two diodes, CR_1 and CR_2, plus the voltage drop across potentiometer R, which affords a means for a slight adjustment in the value of the quiescent current. The current necessary to provide this voltage reference is the collector current of driver transistor Q_1. The diodes may be thermally connected to the heat sink of the output transistors so that thermal feedback is provided for further improvement of thermal stability. Because the forward voltage of the reference diodes decreases with increasing temperature, these diodes compensate for the decreasing V_{BE} of the output transistors by reducing the external bias applied. In this way, the quiescent current of the output stage can be held relatively constant over a wide range of operating temperatures.

EFFECTS OF
LARGE PHASE SHIFTS

The amplifier frequency-response characteristic is an important factor with respect to the ability of the amplifier to withstand unusually severe electrical stress conditions. For example, under certain conditions of input-signal amplitude and frequency, the amplifier may break into high-frequency oscillations which can lead to destruction of the output transistors, the drivers, or both. This problem becomes quite acute in transformer-coupled amplifiers because the characteristics of transformers depart from the ideal at both low and high frequencies. The departure occurs at low frequencies because the inductive

reactance of the transformer decreases, and at high frequencies because the effects of leakage inductance and transformer winding capacitance become appreciable. At both frequency extremes, the effect is to introduce a phase shift between input and output voltage.

Negative feedback is used almost universally in audio amplifiers; the voltage coupled back to the input through the feedback loop may cause the amplifier to be potentially unstable at some frequencies, especially if the additional phase shift is sufficient to make the feedback positive. Similar effects can occur in transformerless amplifiers because reactive elements (such as coupling and bypass capacitors, transistor junction capacitance, stray wiring capacitance, and inductance of the loudspeaker voice coil) are always present. The values of some of the reactive elements (e.g., transistor junction capacitance and transformer inductance as the core nears saturation) are functions of the signal level; coupling through wiring capacitance and unavoidable ground loops may also vary with the signal level. As a result, an amplifier that is stable under normal listening levels may break into oscillations when subjected to high-level signal transients.

A large phase shift is not only a potential cause of amplifier instability, but also results in additional transistor power dissipation and increases the susceptibility of the transistor to forward-bias second-breakdown failures. The effects of large-signal phase shifts at low frequencies are illustrated in Fig. 248, which shows the load-line characteristics of a transistor in a class AB push-pull circuit for signal frequencies of 1000 Hz and 10 Hz. The phase
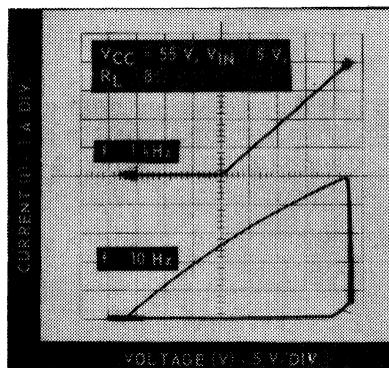
92CS-36365

Fig.248 - Effect of large signal phase shift on the load-line characteristics of a transistor at low frequencies.

shift is caused primarily by the output capacitor. In both cases, the amplifier is driven very strongly into saturation by a 5-volt input signal. The increased dissipation at 10 Hz, compared to that obtained at 1000 Hz, results from simultaneous high-current high-voltage operation. The transistor is required to handle safely a current of 0.75 ampere at a collector voltage of 40 volts for an equivalent pulse duration of about 10 milliseconds; it must be free from second-breakdown failures under these conditions.

EFFECT OF EXCESSIVE DRIVE

Simultaneous high-current high-voltage operation may also occur in class B amplifiers at high frequencies when the amplifier is overdriven to the point that the output signals are clipped. For example, if the input signal applied to the series-output push-pull circuit shown in Fig. 249(a) is large enough to drive the transistors into both saturation and cutoff, transistor A is driven into saturation, and transistor B is cut off during a portion of the input cycle. Fig. 249(b) shows the collector-current waveform for transistor A under these conditions.

(a)
(b)
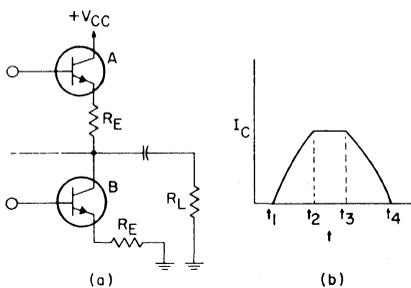
92CS-25910

Fig.249 - (a) class B series-output stage, (b) collector-current waveform under overdrive (clipping) conditions.

During the interval of time from t_2 to t_3, transistor A operates in the saturation region and the output voltage is clipped. The effective negative feedback is then reduced because the output voltage does not follow the sinusoidal input signal. Transistor A, therefore, is driven even further into saturation by the unattenuated input signal. When transistor B starts to conduct, transistor A cannot be turned off immediately because the excessive drive results

in a large storage time. As a result, transistor B is required to support almost the full supply voltage (less only the saturation voltage of transistor A and the voltage drop across the emitter resistors, if used) as its current is increased by the drive signal. For this condition to occur, a large input signal is required at a frequency high enough so that the storage time is greater than one-quarter cycle.

Because of the charging current through the output coupling capacitor, transistor A in Fig. 249(a) is also subject to forward-bias second-breakdown failure if the dc supply voltage and a large input signal are applied simultaneously.

All of these conditions point to the need for a good "safe area" of operation. Fig. 250 shows the safe area for the RCA-2N3055. In all cases, the load lines fall within the area guaranteed safe for this transistor.
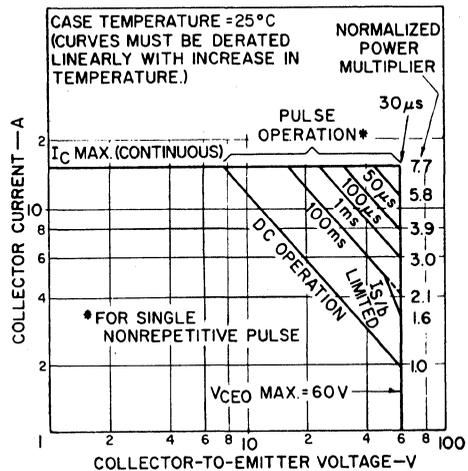
92CS-25911

Fig.250 - Safe-area-of-operation rating chart for the RCA-2N3055 homo-taxial-base transistor.

Short-Circuit Protection

Another important consideration in the design of high-power audio amplifiers is the ability of the circuit to withstand short-circuit conditions. As previously discussed, overdrive conditions may result in disastrously high currents and excessive dissipation in both driver and output stages. Obviously, some form of short-circuit protection is necessary. One such technique is shown in Fig. 251. A current-sampling resistor R is placed in the ground leg of the load. If any condition (including a short) exists such that higher-
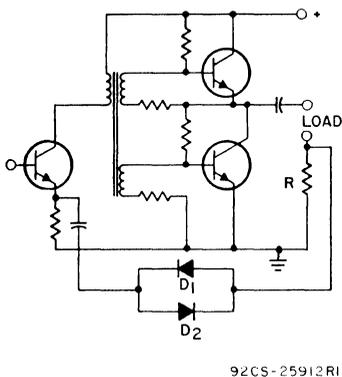
92CS-25912RI

Fig.251 - Push-pull power amplifier with short-circuit protection.

than-normal load current flows, diodes CR₁ and CR₂ conduct on alternate half-cycles and thus provide a high negative feedback which effectively reduces the drive of the amplifiers. This feedback should not exceed the stability margin of the amplifier. This technique in no way affects the normal operation of the amplifier.

A second approach to current limiting is illustrated by the circuit shown in Fig. 252. In this circuit, a diode biasing network is used to establish a fixed current limit on the driver and output transistors. Under sustained short-circuit conditions, however, the output transistors are required to support this current

limit and one-half the dc supply voltage.

The circuit shown in Fig. 253 illustrates a dissipation-limiting technique that provides
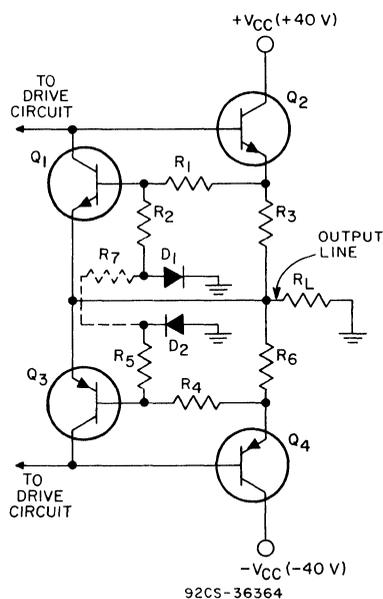
92CS-36364

Fig.253 - Quasi-complementary audio output in which diode-resistor biasing network is used to prevent complementary transistors Q_1 and Q_2 from being forward-biased by the output voltage swing.
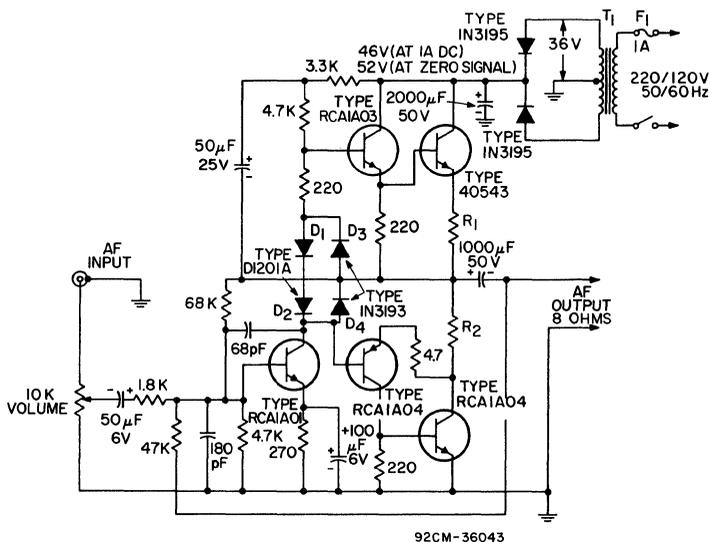
92CM-36043

Fig.252 - 25-watt (rms) quasi-complementary audio amplifier using current-limiting diodes (D_3 and D_4).

positive protection under all loading conditions. The limiting action of this circuit is shown in Fig. 254. This safe-area limiting technique permits use of low-dissipation driver and output transistors and of smaller heat sinks in the output stages. The use of smaller heat sinks is possible because the worst-case dissipation is normal 4-ohm operation instead of short-circuit conditions. With this technique, highly inductive or capacitive loads are no

92CS-36363

Fig.254 - Load lines for the circuit of Fig. 253. Load lines showing effect of the inclusion of high-resistance diode-resistor network in the forward-biasing path of Q_1 are shown dotted.

longer a problem, and thermal cut-outs are unnecessary. In addition, the technique is inexpensive.

V_{BE} MULTIPLIER BIASING CIRCUIT FOR POWER AMPLIFIER OUTPUT STAGES

The following paragraphs describe a biasing circuit for the output stage of a power amplifier. The biasing circuit is called a V_{BE} multiplier; its purpose is to provide proper bias for the output transistors of the amplifier under all operating conditions. The amount of forward bias provided determines the quiescent operating point of the output stage. The criteria for determining the proper quiescent collector current of the output transistors are the output-signal distortion level to be achieved and the need to minimize quiescent current because of dissipation in the output transistors. Fig. 255 shows the circuit of a typical complementary output stage for an audio amplifier. In this circuit, transistor Q3 serves as the biasing element for transistors Q4 and Q5.

Since all transistors are temperature sensitive, the bias circuit should change bias voltage in such a manner that the quiescent collector

92CS-24053

Fig.255 - Complementary output stage for an audio amplifier.

current of the output transistors remains constant. Typical temperature dependence of a silicon power transistor is shown in Fig. 256. The figure shows that the bias voltage must decrease approximately 2 mV/°C if the collector current is to be constant. Failure to provide thermal compensation will result in a current change of:

$$\frac{\Delta I_c}{\Delta T} \simeq 10\%/°C$$

A further examination of Fig. 256 shows that an error of 20 millivolts (3 per cent) in the bias voltage will result in a change in the collector current by a factor of 2.

Transistor Q3 in Fig. 255 varies the biasing voltage for the output transistors so that quiescent current does not change with temperature change. This constant-current condition is achieved by mounting Q3, Q4, and Q5 on the same heat sink so that a change in the junction temperature of the output transistors will change the heat-sink temperature proportionally and, therefore, the junction temperature of Q3. If, for example, temperature increases, the collector current of Q3 would tend to increase, but constant-current source Q6 keeps the collector current of Q3 constant. Under this condition, the V_{BE} of Q3 will decrease and V_{bias} will decrease proportionally. The net result will be the stabilization of the quiescent collector current of Q4 and Q5.

AUDIO AMPLIFIER CIRCUITS USING ALL DISCRETE DEVICES

A broad selection of power levels can be obtained from amplifiers using only discrete solid state devices. The following chart lists the type of circuit configuration and recommended output devices for power output levels ranging from 3 to 300 watts. A circuit diagram and performance data are shown for representative amplifiers. For information on the other audio amplifier circuits listed in the chart, refer to RCA "Audio Amplifier Manual," APA-551 and the individual data sheets for the output devices.

25-Watt True-Complementary-Symmetry Audio Amplifier with Darlington Output Transistors

Fig. 257 shows a complementary amplifier rated at 25 watts output with an 8-ohm load, using Darlington transistors in the output stage. The amplifier also will supply 25 watts output with a 4-ohm load and 14-watts with a 16-ohm load. Thermal stability is provided by mounting the biasing transistor on the output heat-sink. Dissipation-limiting overload protection is incorporated in this circuit. A 70°C thermal cut-out should be used in the primary of the power supply.

Typical performance data are shown in Table XVI. Fig. 258 shows distortion as a function of power output.
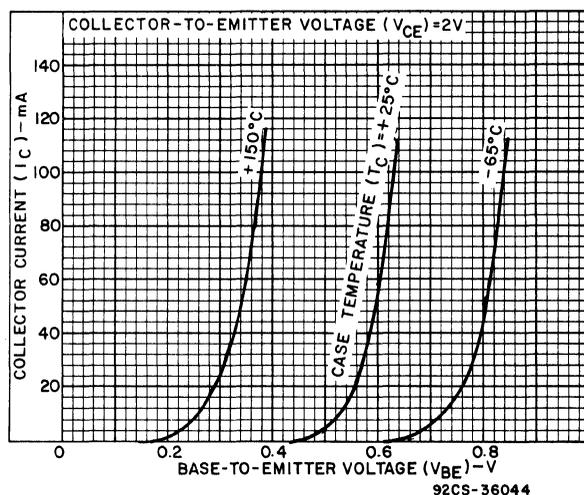
Fig.256 - Temperature dependence of a silicon power transistor.

Table XV - Selection Chart for Discrete Preamplifier
Power Output Stage Amplifiers

Power Output (W)	Load Res. (Ω)	Supply Voltage (V)	Type of Circuit	Output Transistors NPN	Output Transistors PNP
3 12	8 4	20	True-Comp.	RCP703A	RCP702A
12 6.5	8 16	36	True-Comp.	RCA1C10	RCA1C11
45	4			RCA1C05	RCA1C06
25	8	52	True-Comp.	BD243A or RCA1C05	BD244A or RCA1C06
16	16			RCA1C05	RCA1C06
25	4	40		2N6387 or BDX33A	2N6667 or BDX34A
25	8	52	True-Comp. Darlington	2N6388 or BDX33B	2N6668 or BDX34B
14	16	52		2N6388 or BDX33B	2N6668 or BDX34B
40	4	46		BD501A or RCA1C07	BD500A or RCA1C08
40	8	64	True-Comp.	BD501B or RCA1C07	BD500B or RCA1C08
22	16	64		BD501B or RCA1C07	BD500B or RCA1C08
40	4	46	Quasi-Comp.	2-2N6101 or 2-RCA1C09	—
40	8	64			
25	16	64			
100	4			2-RCA1B06	—
70	8	90	Quasi-Comp.	2-BD550 or 2-RCA1B06	—
40	16			2-BD550 or 2-RCA1B06	—
100	4	84		2-RCA1B01	—
70	4	60		2-BD450	—
70	8	84	Quasi-Comp.	2-BD451 or 2-RCA1B01	—
38	16	84		2-BD451 or 2-RCA1B01	
180	4	130		4-RCA1B04	—
120	4	90		4-BD550	—
120	8	130	Quasi-Comp.	4-BD550A or 4-RCA1B04	—
70	16	130		4-BD550A or 4-RCA1B04	
300	4	160		6-RCA1B05	—
200	4	110		6-BD550A	—
200	8	160	Quasi-Comp.	6-BD550B or 6-RCA1B05	—
120	16	160		6-BD550B or 6-RCA1B05	—
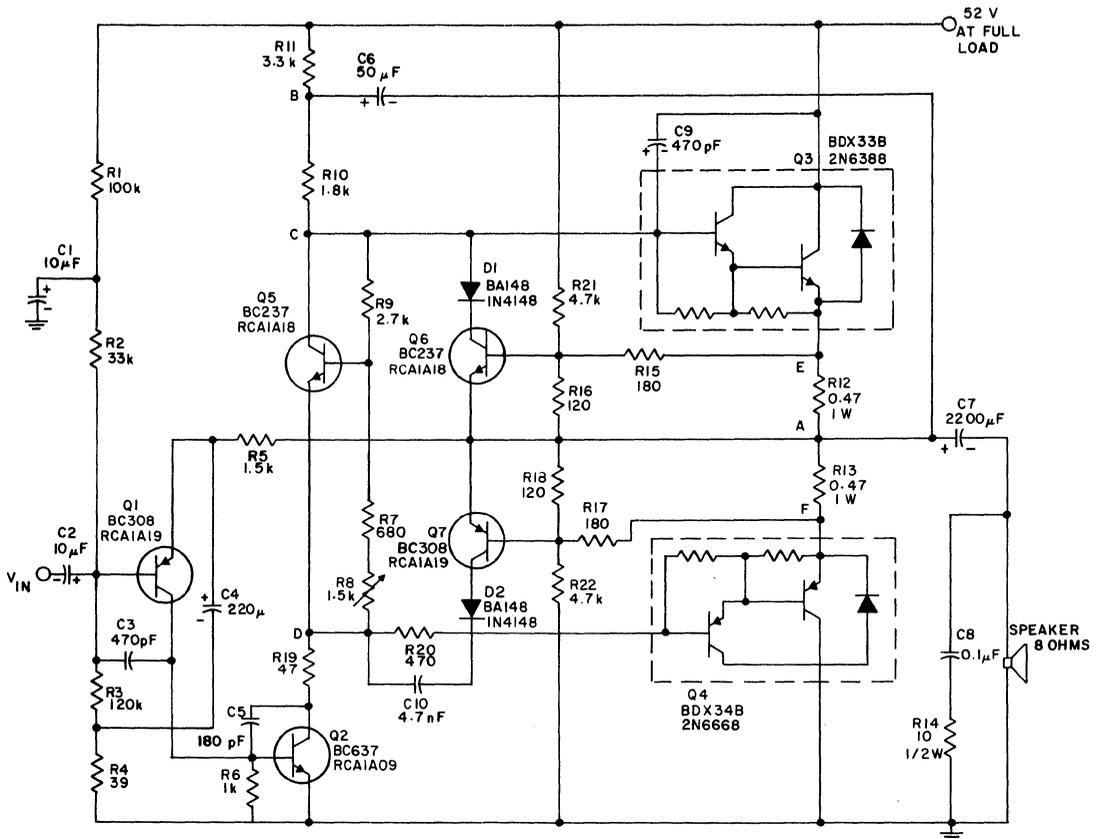
Fig.257 - *25-watt true-complementary-symmetry amplifier featuring Darlington output transistors.*
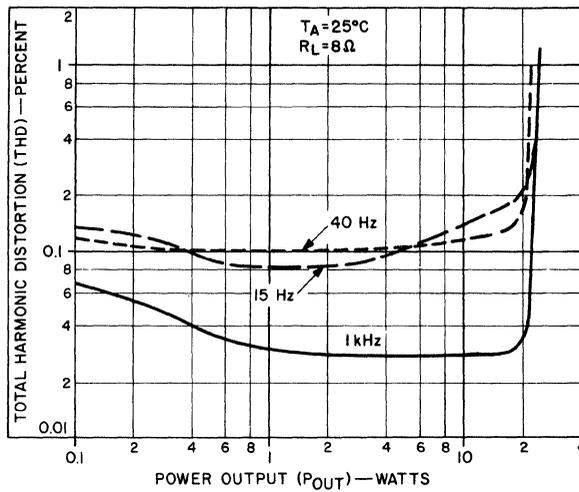
Fig.258 - *Typical total harmonic distortion as a function of power output.*

Table XVI - Typical Performance Data for 25-Watt Audio Amplifier

Measured at V_{CC}=52 V, T_A=25° C, and frequency of 1 kHz unless otherwise specified.

Power:

Rated power (8 Ω load) . . . . 25 W

Typical power (4 Ω load) . . . . 25 W*

Typical power (16 Ω load) . . . . 14 W

Total Harmonic Distortion . . . . See Fig. 258

Sensitivity:

For 25-W output . . . . 360 mV

*With 40-V supply voltage and BDX33A, BDX34A substituted for BDX33B, BDX34B.

40-Watt True-Complementary-Symmetry Audio Amplifier

Fig. 259 shows a complementary amplifier using epitaxial base output transistors rated at 40 watts output with an 8-ohm load. A power supply intended to supply two identical amplifiers is shown in Fig. 260. The amplifiers

also will supply 40 watts output with a 4-ohm load and 22 watts with 16-ohm load. This amplifier provides outstanding stability of the output transistors through the use of a unique turn-off drive circuit, which consists of a resistor and capacitor connected between the bases of the discrete output devices. This
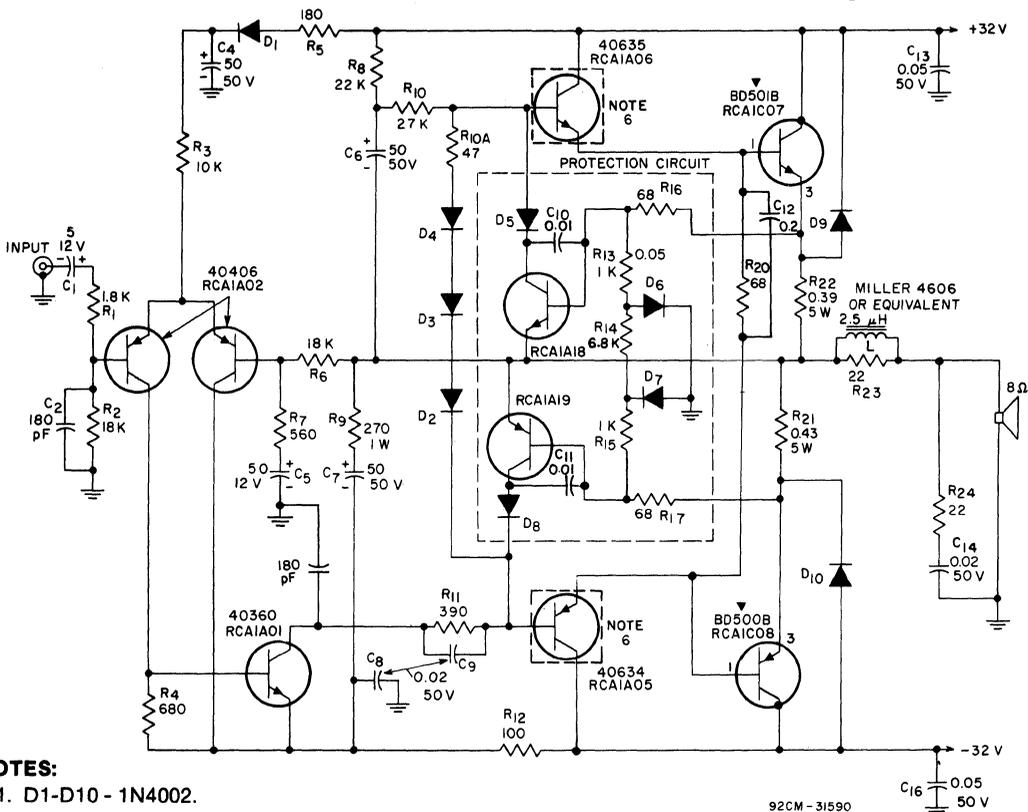
NOTES:

1. D1-D10 - 1N4002.
2. Resistors are ½-watt, ±10%, unless otherwise specified; values are in ohms.
3. Non-inductive resistors.
4. Capacitances are in μF unless otherwise specified.

5. Provide heat sink of approx. 1.2° C/W per output device with a contact thermal resistance of 1.3° C/W max. and T_A=40° C max.
6. TO-39 case devices with heat radiator attached.

92CM-31590

Fig.259 - 40-watt amplifier featuring true-complementary-symmetry output using load-line limiting.
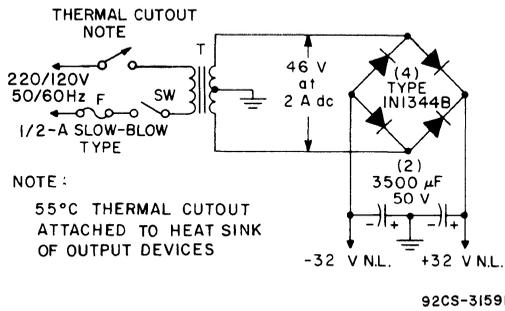
Fig.260 - Power supply for 40-watt amplifier.

technique allows the output transistors to operate with equal power-bandwidth performance. The circuit also incorporates dissipation-limiting overload protection.

Typical performance data are shown in Table XVII. Fig. 261 shows distortion as a function of frequency and Fig. 262 shows the frequency response.

70-Watt Quasi-Complementary-Symmetry Audio Amplifier

Fig. 263 shows a complementary amplifier using hometaxial-base output transistors, rated at 70 watts output with an 8-ohm load. A
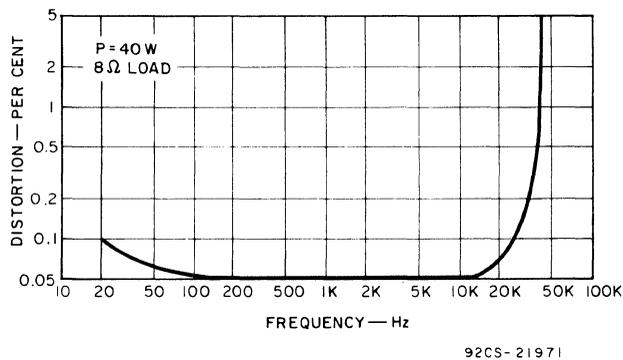
Fig.261 - Typical total harmonic distortion as a function of frequency.

Table XVII - Typical Performance Data for 40-Watt Audio Amplifier

Measured at V_{CC}=64 V, T_A=25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:
    Rated power (8 Ω load, at rated distortion) . . . . 40 W
    Typical power (4 Ω load) . . . . 75 W*
    Typical power (16 Ω load) . . . . 22 W
Total Harmonic Distortion:
    Rated distortion 1%
    Typical at 20 W 0.05%
IM Distortion:
    10 dB below continuous power output at 60 Hz and 7 kHz (4:1) 0.1%
IHF Power Bandwidth:
    3 dB below rated continuous power at rated distortion . . . . 80 kHz
Sensitivity:
    At continuous power-output rating . . . . .600 mV
Hum and Noise:
    Below continuous power output:
        Input shorted . . . . 80 dB
        Input open . . . . 75 dB
Input Resistance . . . . .20 KΩ

*Typical power (4 Ω load) with 46-volt split power supply and BD500A, BD501A output . . . . 40 W
 Typical power (4 Ω load) with 40-volt split power supply and BD500, BD501 output . . . . 25 W
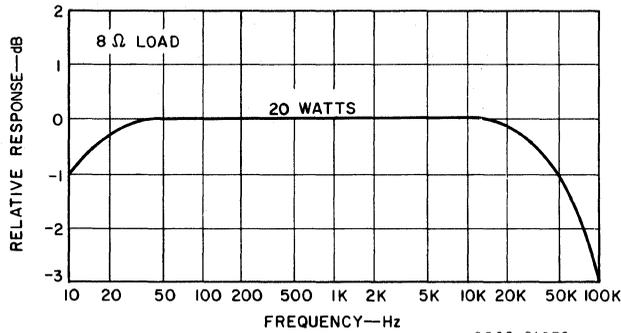
Fig.262 - *Typical frequency response.*

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Fig.263 - *70-watt amplifier circuit featuring quasi-complementary-symmetry output employing hometaxial-base construction output transistors.*

92CM-31596
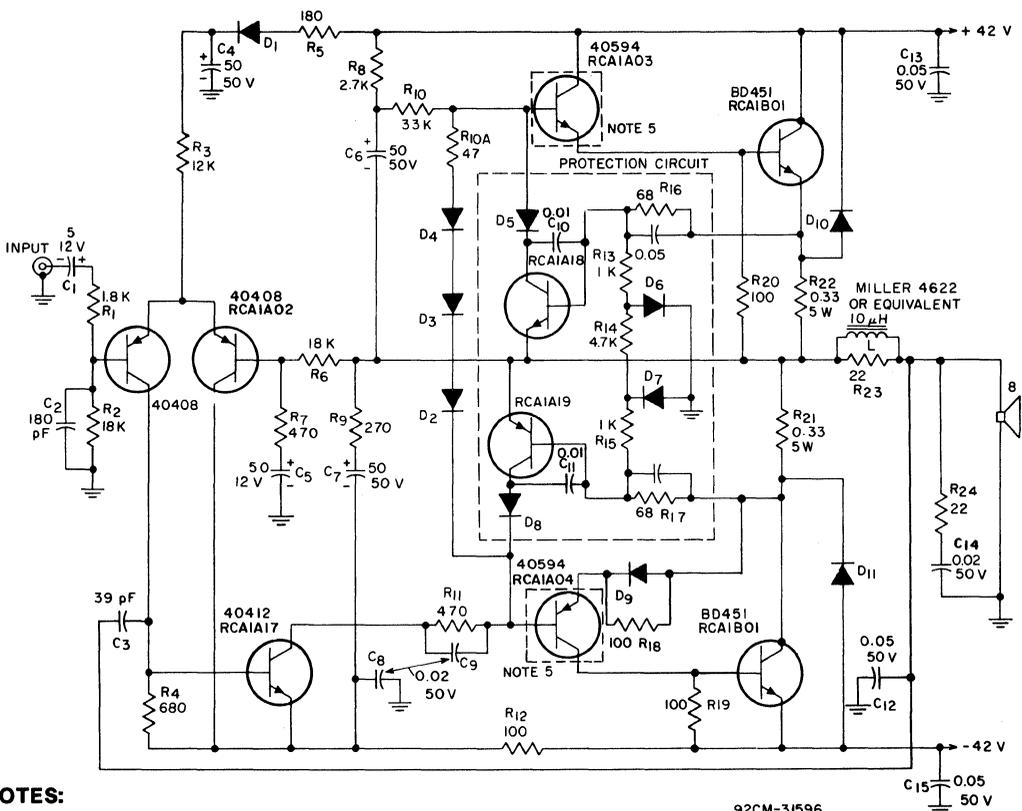
NOTES:
1. D1-D11 - 1N4002.
2. Resistors are ½-watt, ±10%, unless otherwise specified; values are in ohms.
3. Non-inductive resistors.
4. Capacitances are in μF unless otherwise specified.
5. Mount each device on TO-39 heat sink.
▼6. Provide heat sink of approx. 1.2° C/W per output device with a contact thermal resistance of 0.5° C/W max. and T_A=45° C max.

power supply intended to supply two identical amplifiers is shown in Fig. 264. The amplifier also will supply 100 watts with a 4-ohm load and 38 watts with a 16-ohm load. The circuit is unusually rugged in regard to overloads, but also incorporates dissipation-limiting overload protection.

Typical performance data are shown in Table XVIII. Fig. 265 shows distortion as a function of power output, and Fig. 266 shows the response curve.
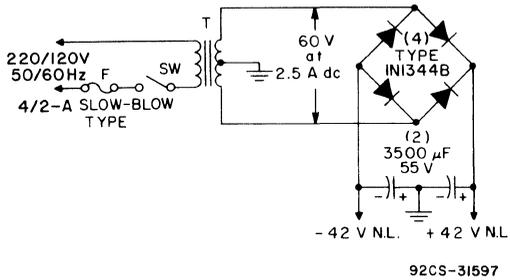
Fig.264 - Power supply for 70-watt amplifier.

120-Watt Quasi-Complementary-Symmetry Audio Amplifier

Fig. 267 shows an amplifier using two pairs of complementary output transistors in parallel rated at 120 watts output with an 8-ohm load. A power supply intended to supply two identical amplifiers is shown in Fig. 268. The amplifier also will supply 180 watts with a 4-ohm load and 70 watts with a 16-ohm load. Thermal stability is enhanced by mounting the biasing transistor on the output heat sink. The circuit incorporates dissipation-limiting overload protection.
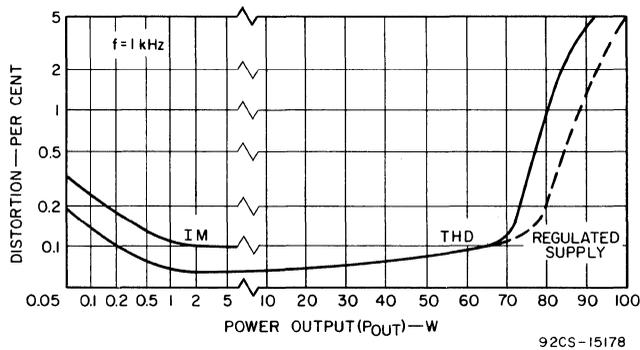
Fig.265 - Typical intermodulation and total harmonic distortion as a function of power output at 1 kHz.

Table XVIII - Typical Performance Data for 70-Watt Audio Amplifier

Measured at V_{CC}=84 V, T_A=25° C, and a frequency of 1 kHz unless otherwise specified.

Power:
Rated power (8 Ω load, at rated distortion) .... 70 W
Typical power (4 Ω load) .... 100 W*
Typical power (16 Ω load) .... 38 W
Music power (8 Ω load, at 5% THD with regulated supply) .... 100 W
Dynamic power (8 Ω load, at 1% THD with regulated supply) .... 88 W
Total Harmonic Distortion:
Rated distortion 1%
IM Distortion:
10 dB below continuous power output at 60 Hz and 7 kHz (4:1) 0.1%
Sensitivity:
At continuous power-output rating .... 700 mV
Hum and Noise:
Below continuous power output:
Input shorted .... 85 dB
Input open .... 80 dB
Input Resistance .... 20 KΩ

*With 2-RCA1B01 in output stage.
With 60-volt split power supply and 2-BD450 substituted for 2-BD451 .... 70 W
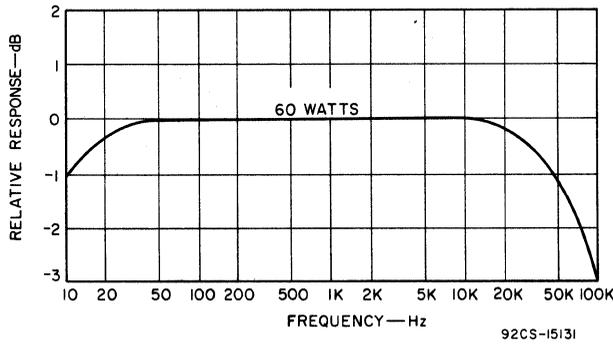
Fig.266 - *Typical response as a function*
of frequency at 60-watt output.
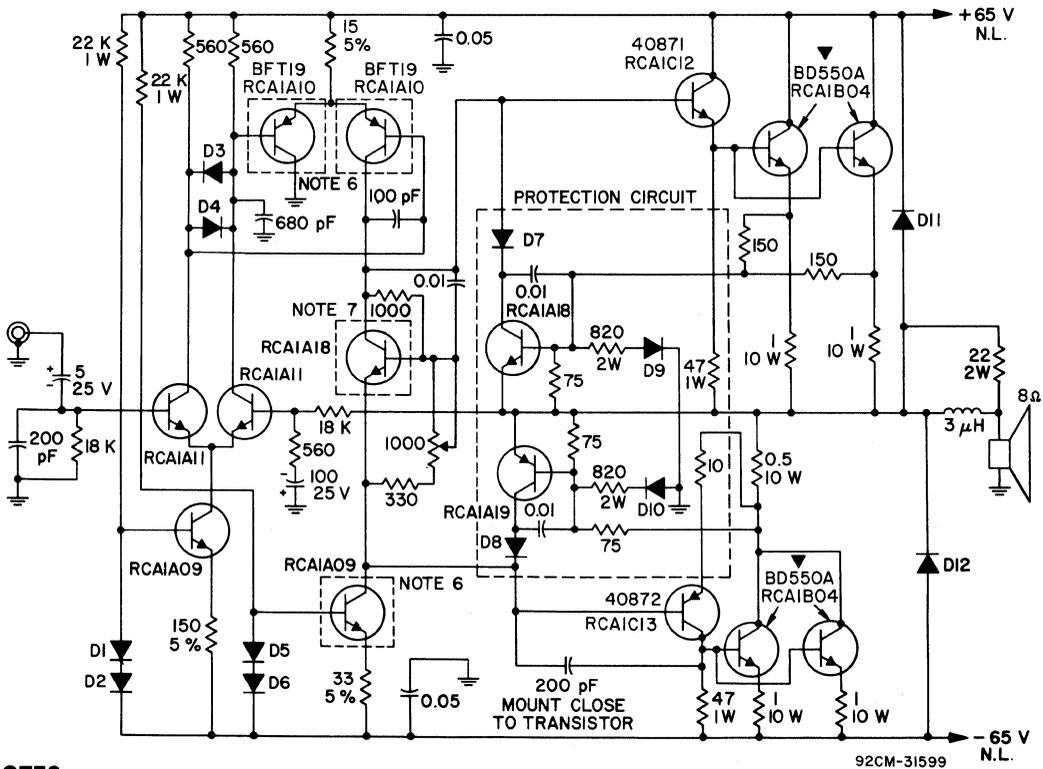
NOTES:

1. D1-D8 - 1N5391; D9, D10 - 1N4148, D11-D12 -1N5393.
2. Resistors are ½-watt, ±10%, unless otherwise specified; values are in ohms.
3. Non-inductive resistors.
4. Capacitances are in µF unless otherwise specified.

▼5. Provide heat sink of approx. 1° C/W per output device with a contact thermal resistance of 0.5° C/W max. and T_A=45° C max.
6. Mount each device on TO-39 heat sink.
7. Attach TO-39 heat sink cap to device and mount on same heat sink with the output devices.

Fig.267 - *120-watt amplifier circuit featuring quasi-complementary-*
symmetry output circuit with parallel output transistors.

Typical performance data are shown in Table XIX. Fig. 269 shows distortion as a function of power output, and Fig. 270 as a function of frequency.

Table XIX - Typical Performance Data for 120-Watt Audio Amplifier

Measured at V_{CC}=130 V, T_A=25° C, and a frequency of 1 kHz, unless otherwise specified.

Power:
  Rated power (8 Ω load, at rated distortion) .... 120 W
  Typical power (4 Ω load) .... 180 W*
  Typical power (16 Ω load) .... 70 W
Total Harmonic Distortion:
  Rated Distortion 0.5%
IM Distortion:
  10 dB below continuous power output at 60 Hz and 7 kHz (4:1) 0.2%
Sensitivity:
  At continuous power output rating .... 900 mV
Input Resistance .... 18 KΩ
IHF Power Bandwidth:
  3 dB below rated continuous power at rated distortion .... 5 Hz to 50 kHz
Hum and Noise:
  Below continuous power output:
    Input shorted .... 104 dB
    Input open .... 88 dB
    With 2 KΩ resistance on 20-ft. cable on input .... 104 dB

*With 4-RCA1B04 in output stage.
  With a 90-V split power supply and 4-BD550 substituted for 4-BD550A .... 120 W
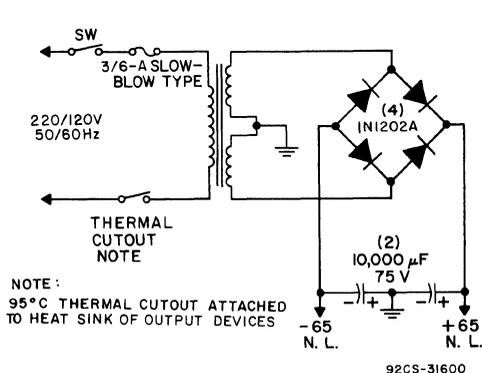
Fig.268 -
Power supply for 120-watt ampli-
fier.

92CS-22028

Fig.269 - Typical total harmonic distortion
as a function of power output for
single channel (8 Ω) and both
channels driven at 1 kHz.

AUDIO AMPLIFIER CIRCUITS WITH IC PREAMPLIFIERS AND DISCRETE POWER OUTPUT STAGES

Many modern high-fidelity amplifiers use integrated circuits as preamplifiers and pre-drivers with power transistors in the driver and output stages. Integrated circuits usually offer some performance and cost advantages over discrete transistors for the low-power stages. Table XX is a selection chart for amplifiers in this classification with power output capability from a few watts to several hundred watts. A circuit diagram and performance data are shown for representative amplifiers. For information on the other audio amplifiers listed in the chart, refer to RCA "Audio Amplifier Manual," APA-551, also the individual data sheets for the output devices.
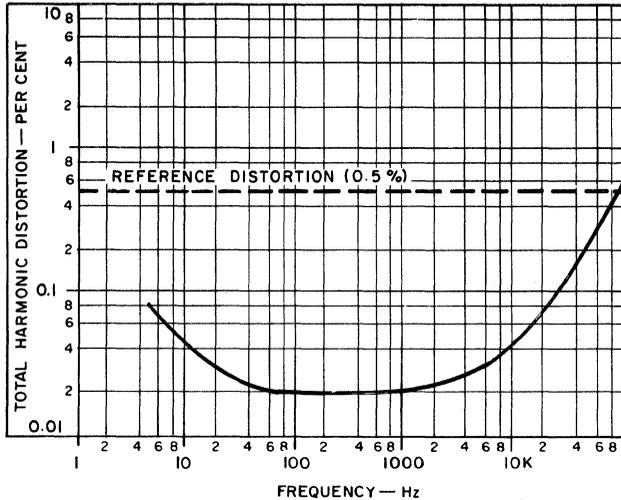
Fig.270 -
Typical total harmonic distortion
as a function of frequency for
60-watt output.

Table XX - Selection Chart for IC Preamplifiers with Discrete Power Output Stage Amplifiers

Power Output (W)	Load Res. (Ω)	Supply Voltage (V)	IC Type No.	Type of Output Circuit	Output Transistors	
					NPN	**PNP**
4	8	12	CA3020	Single Class A	—	2N6107
9 12 6	4 8 16	36	CA3094A	True-Comp.	2N6290 or BD241	2N6109 or BD242
10	4	14.4	CA3094	Bridge	2-2N6288	2-2N6111
25 15 8	4 8 16	40	CA3094B	True-Comp. Darlington	2N6388 or BDX33A	2N6668 or BDX34A
30 60	8 4	60	CA3100	True-Comp. Darlington	2N6385	2N6650
40 20	8 16	14.4	2-CA2002	Push-Pull	2-2N6486	—
20	8	50	CA3140B	True-Comp. Darlington	BDX33B or RCA1C15	BDX34B or RCA1C16
50 100 150 100	8 4	72 108 120 90	CA3140A	True-Comp.	RCA8638 2-MJ15003 3-MJ15003 4-BD550 or 4-RCA8638D	RCA9116 2-MJ15004 3-MJ15004 —
100 60 300	8 16 4	114 114 120	CA3100	Quasi-Comp.	4-BD550A or 4-RCA1B04 4-BD550A or 4-RCA1B04 18-BD550A or 18-RCA1B05	— — —
300 160	8 16	172 172	CA3100	Quasi-Comp.	18-BD550B or 18-RCA1B05 18-BD550B or 18-RCA1B05	— —
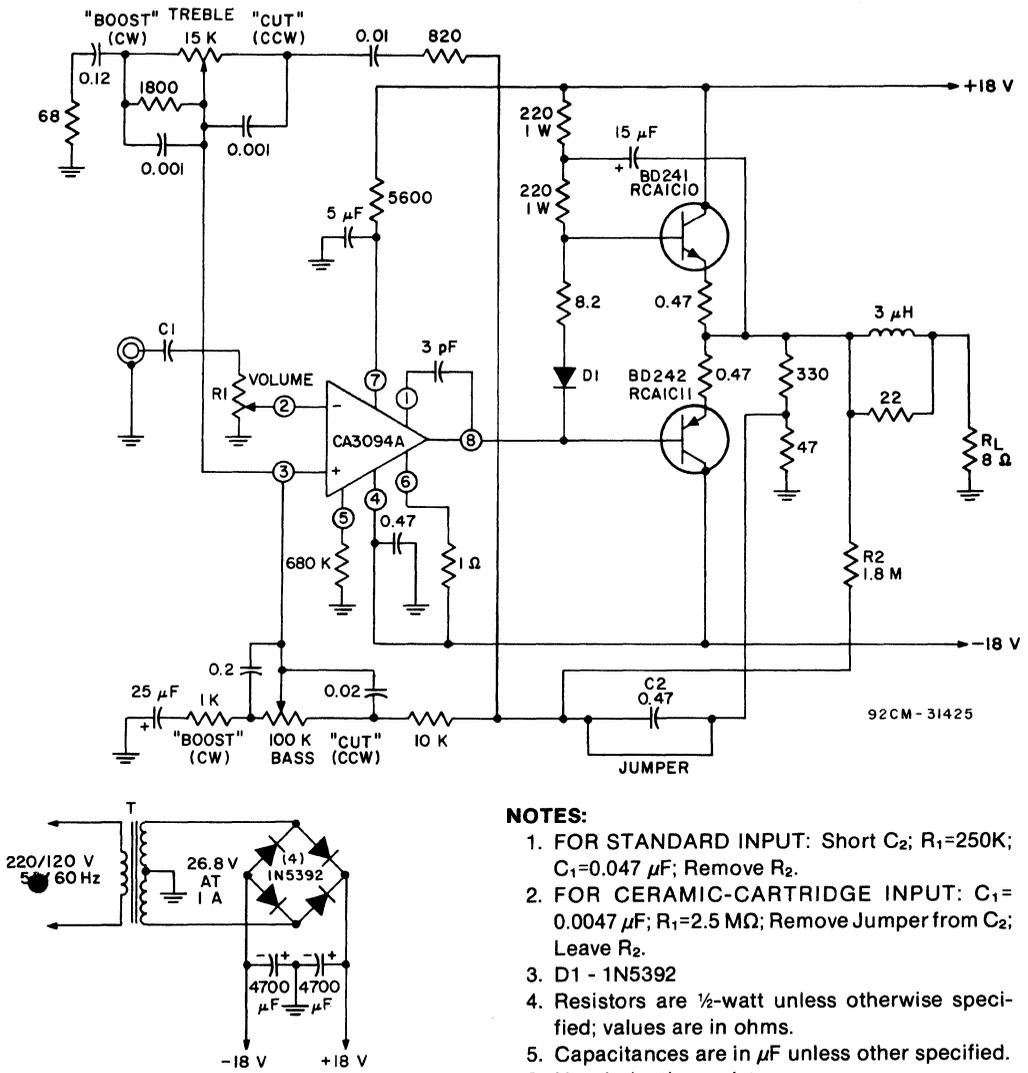
NOTES:
1. FOR STANDARD INPUT: Short C_2; R_1=250K; C_1=0.047 μF; Remove R_2.
2. FOR CERAMIC-CARTRIDGE INPUT: C_1= 0.0047 μF; R_1=2.5 MΩ; Remove Jumper from C_2; Leave R_2.
3. D1 - 1N5392
4. Resistors are ½-watt unless otherwise specified; values are in ohms.
5. Capacitances are in μF unless other specified.
6. Non-inductive resistors.

Fig.271 - 12-watt amplifier circuit featuring an integrated-circuit driver and a true-complementary-symmetry output stage.

12-Watt True-Complementary-Symmetry Audio Power Amplifier

The CA3094-series IC power amplifiers have a configuration and characteristics well suited for driving complementary discrete power-output transistors. The circuit of Fig. 271 shows an amplifier of this type that can supply 12 watts output to an 8-ohm load from a 36-V split power supply with very low harmonic and intermodulation distortion. Fig. 272 shows IMD as a function of power output.

The large amount of loop gain and the flexibility of feedback arrangements with the CA3094 make it possible to incorporate the tone controls into a feedback network that is closed around the entire amplifier system. Fig. 273 shows voltage gain as a function of frequency with tone controls adjusted for "flat" response and for responses at the extremes of tone-control rotation. The use of tone controls in the feedback network results in excellent signal-to-noise ratio.

Diode D1 may be mounted on the output-transistor heat sink for improved thermal stability. Typical performance data are shown
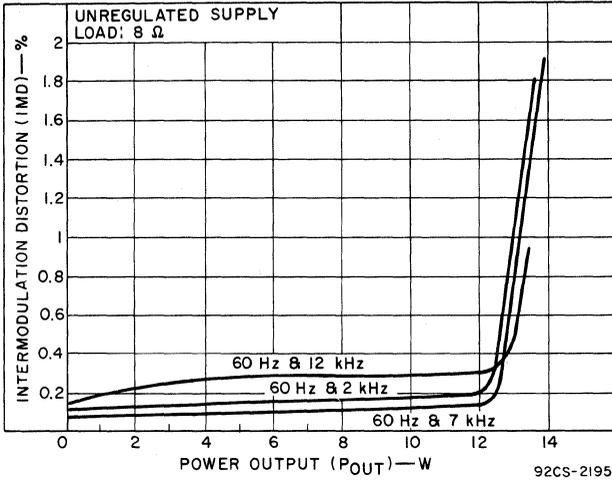
Fig.272 -
Intermodulation distortion as a
function of power output.

Fig.273 -
Voltage gain as a function of
frequency.
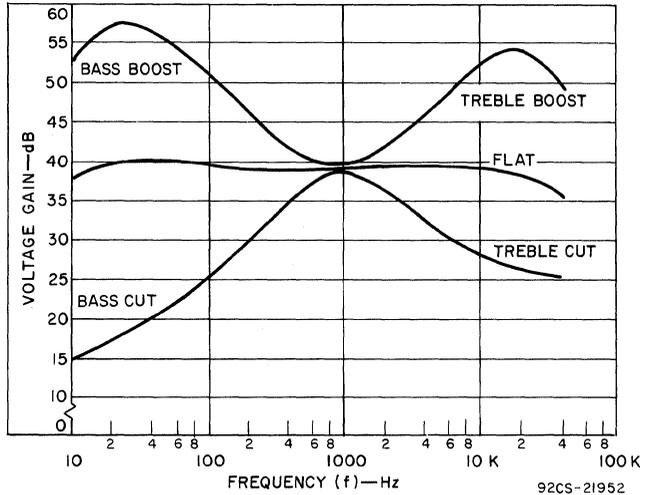
Table XXI - Typical Performance Data for 12-Watt Audio Amplifier Circuit

Measured at V_{CC}=36 V, T_A=25°C, and a frequency of 1 kHz, unless otherwise specified.

Power:
   Rated power (8 Ω load, at rated distortion) .... 12 W
   Typical power (4 Ω load) .... 9 W
   Typical power (16 Ω load) .... 6 W
   Music power (8 Ω load, at 5% THD with regulated supply) .... 15 W
Total Harmonic Distortion:
   Rated distortion 1%
   Typical at 1 W 0.05%
IM Distortion:
   10 dB below continuous power output at 60 Hz and 2 kHz (4:1) 0.2%
Sensitivity:
   At continuous power-output rating (tone controls flat) .... 100 mV
Hum and Noise:
   Below continuous power output:
     Input open .... 83 dB
Input Resistance .... 250 KΩ
Voltage Gain .... 40 dB
Tone Control Range .... See Fig. 273

NOTES:
1. D1-D2 - 1N3754; D3-D6 - 1N4148
2. Z1-Z2 - 1N4744.
3. Resistors are ½-watt, ±10%, unless otherwise specified; values are in ohms.
4. Capacitances are in μF unless otherwise specified.
5. Non-inductive resistors.
6. Heat sink per output transistor 1.3° C/W max. thermal resistance.

Fig.274 - 20-watt audio-amplifier circuit featuring full-complementary-symmetry with Darlington output transistors.

in Table XXI, for operation with 4-ohm, 8-ohm, and 16-ohm loads.

20-Watt True-Complementary-Symmetry Audio Amplifier

Fig. 274 shows a circuit with the CA3140B IC driving an amplifier with complementary Darlington transistors in the output stage. The CA3140B-series BiMOS IC's have a configuration and characteristics nearly ideal for driving complementary discrete power amplifier transistors.

The circuit of Fig. 274 is capable of supplying 20 watts output to an 8-ohm load with very low distortion using a 50-volt split power supply. Typical performance data are shown in Table XXII. Total harmonic distortion as a function of power output is shown in Fig. 275 and as a function of frequency in Fig. 276. Intermodulation distortion is shown in Fig. 277 and frequency response in Fig. 278.

Table XXII - Typical Performance Data for 20-Watt Audio Amplifier

Measured at V_{CC}=50 V, T_A=25° C, and a frequency of 1 kHz, unless otherwise specified.

Rated Power:
   8-Ohm Load . . . . 20 W
Total Harmonic Distortion:
   (THD) . . . . See Figs. 275 and 276
Intermodulation Distortion:
   (IMD) . . . . See Fig. 277
Sensitivity . . . . 0.85 V for 10 W
Input Impedance . . . . 10 KΩ
Hum and Noise:
  Below rated power output
     Open input . . . . 94 dB
     Shorted input . . . . 97 dB
Phase Shift . . . . +1.5° at 20 Hz
                                             –6° at 20 kHz
Slew Rate . . . . .30 V/μs
Rise Time . . . . 1.3 μs
Damping Factor 220
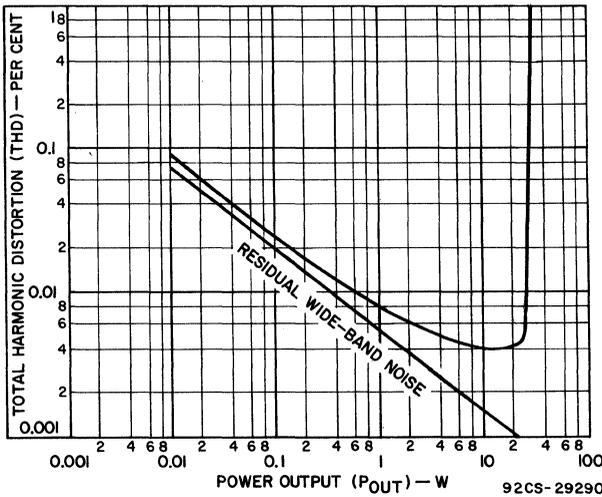
Fig.275 -

Typical total harmonic distortion as a function of power at 1 kHz, both channels driven.

Fig.276 -

Typical total harmonic distortion as a function of frequency for 20-watt output.
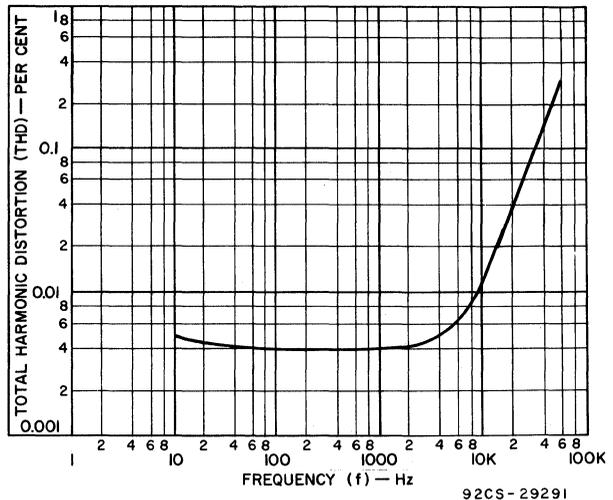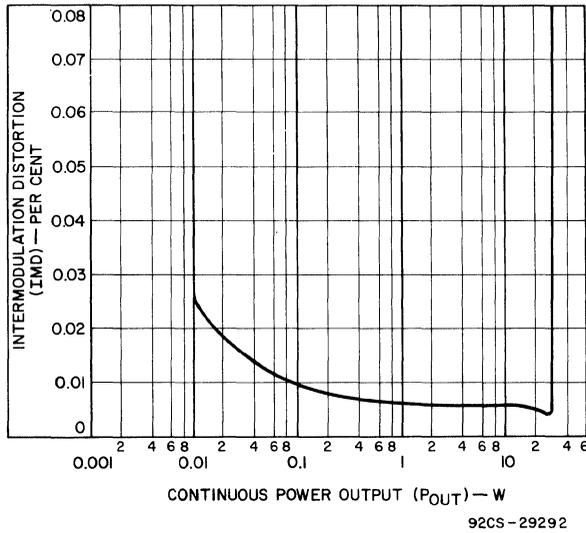
Fig.277 - Typical intermodulation distortion as a function of power at 60 Hz and 7 kHz, 4:1.
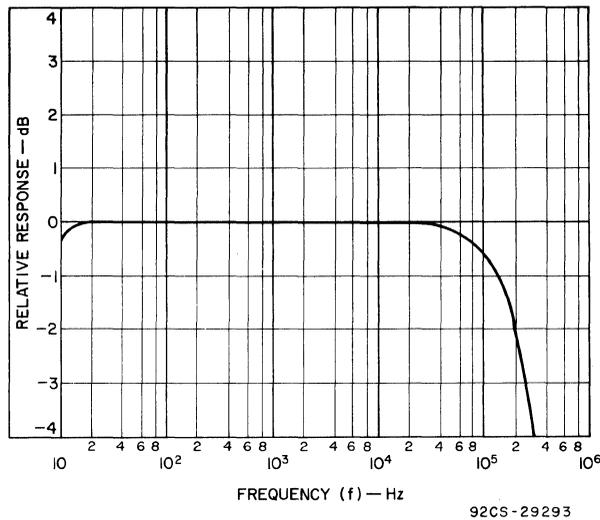
Fig.278 - Typical frequency response.

100-Watt True-Complementary-Symmetry Audio Amplifier

Figs. 279 and 280 show a circuit with the CA3140A IC driving an amplifier with two pairs of epitaxial transistors in parallel in a true-complementary-symmetry output stage. The amplifier is capable of supplying 100 watts output to an 8-ohm load, using a 108-V split power supply. Typical performance of this amplifier is shown in Table XXIII including operation with both 4-ohm and 16-ohm loads. The harmonic distortion as a function of power output is shown in Fig. 281 and as a function of frequency in Fig. 282. Additional features include thermal overload and reactive overload protection, and instant turn-on with no undesirable transients.

With a single pair of output transistors of the same type, or with the substitution of the RCA8638 and RCA9116 in the output stage, the amplifier is capable of 50 watts power output using a 72-V split power supply. With

Table XXIII - Typical Performance Data for 100-Watt Audio Amplifier

Measured at V_{CC}=108 V, T_A=25°C, and a frequency of 1 kHz unless otherwise specified.

Rated Power (8 Ω load at rated distortion) .... 100 W
Typical Power (4 Ω load) .... 150 W*
Typical Power (16 Ω load) .... 75 W
Total Harmonic Distortion:
  (THD) .... See Figs. 281 and 282
Sensitivity .... 1 V for 100 W
Input Impedance.. 10 KΩ
Slew Rate ....28 V/μs
Rise Time .... 1.1 μs
Damping Factor 140

*With 68-V split power supply, 100 W.
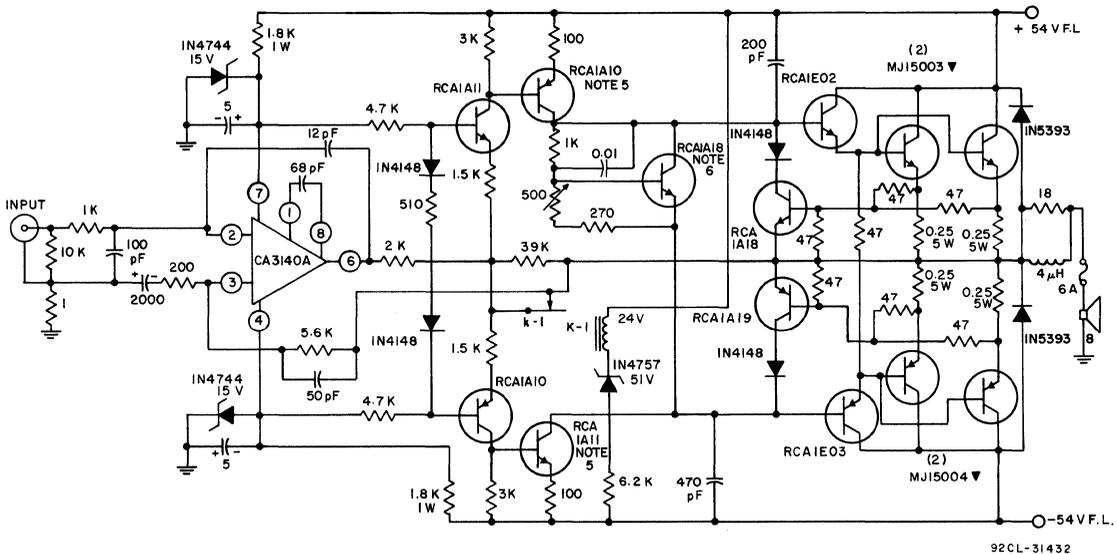
NOTES:
1. Resistors are ½-watt, ±5%, unless otherwise specified; values are in ohms.
2. Non-inductive resistors.
3. Capacitances are in μF unless otherwise specified.
4. K-1 relay, single-pole, single-throw, normally closed, with 24 V, 3 mA coil.
5. Mount each on heat sink, 5 sq. in. min. area.
6. Mount on same heat sink with the output devices.
▼ 7. Provide heat sink of approx. 1°C/W per output device with a contact thermal resistance of 0.5°C/W max. and T_A=45°C max.

Fig.279 - 100-watt audio amplifier with parallel output transistors.

three pairs in parallel, it is capable of 150 watts output using a 120-V split power supply, in both cases with an 8-ohm load.

100-Watt Quasi-Complementary-Symmetry Audio Power Amplifier

The circuit shown in Figs. 283 and 284 uses the CA3100 IC as a preamplifier and dual-Darlington-driven parallel output transistors to deliver 100 watts power output to an 8-ohm

load from a 114-V split power supply. With the exception of the CA3100, this amplifier is entirely push-pull for improved high-frequency distortion and slew rate. Additional features include thermal overload and reactive overload protection, and instant turn-on with no undesirable transients.

Typical performance data for this amplifier are shown in Table XXIV. The harmonic distortion is shown in Fig. 285, and the response curve in Fig. 286.
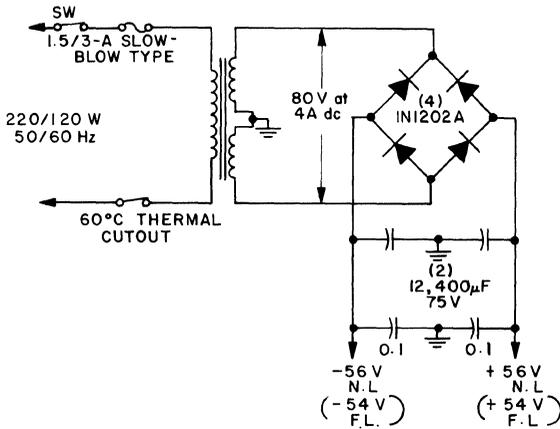
Fig.280 - *Power supply for 100-watt amplifier.*

92CS-31446

Fig.281 -

Typical total harmonic distortion as a function of power output for 100-watt true-complementary amplifier shown in Fig. 279.
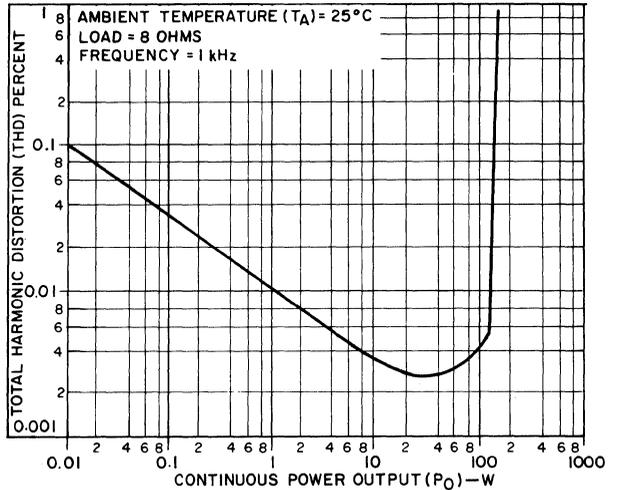
92CS-31433
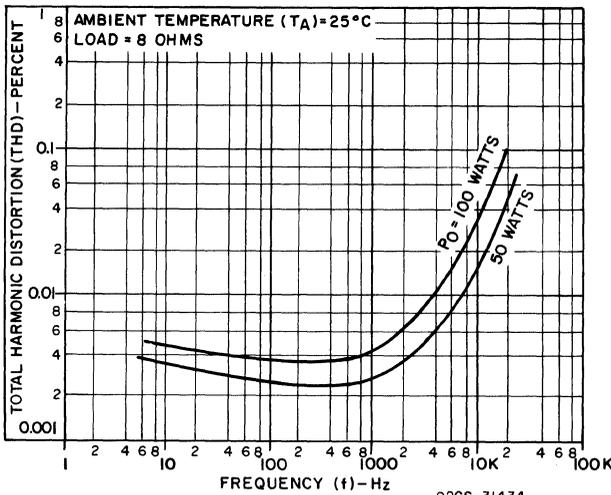
Fig.282 -

Typical total harmonic distortion as a function of frequency for 100-watt true-complementary amplifier shown in Fig. 279.
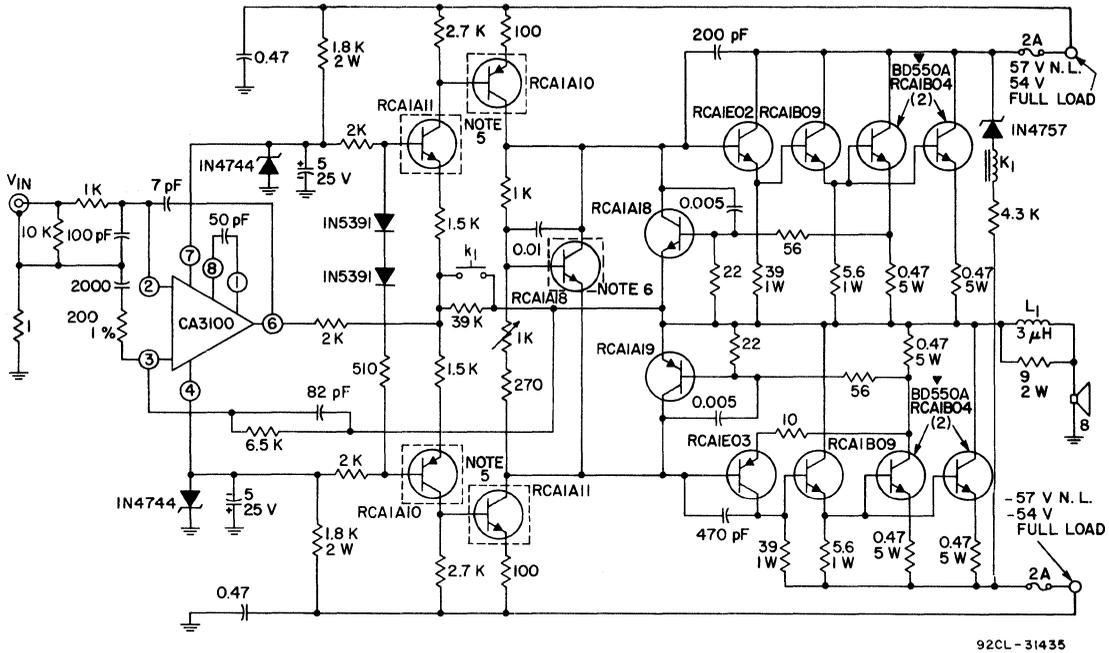
92CS-31434

92CL-31435

NOTES:

1. Resistors are ½-watt, ±5%, unless otherwise specified; values are in ohms.
2. Non-inductive resistors.
3. Capacitances are in μF unless otherwise specified.
4. K-1 relay, single-pole, single-throw, normally closed, with 24 V, 3 mA coil.

5. Mount on common heat sink, 25 sq. in. min. area.
6. Mount on same heat sink with the output devices.
▼7. Provide heat sink of approx. 1° C/W per output device with a contact thermal resistance of 0.5° C/W max. and T_A=45° C max.

Fig.283 - 100-watt audio power amplifier featuring parallel output transistors.

92CS-31436
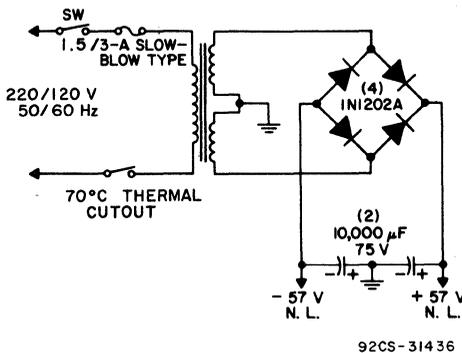
Fig.284 - Power supply for 100-watt audio amplifier.

Twenty-Five-Watt (RMS) True Complementary-Symmetry Audio Amplifier

The twenty-five-watt (rms) complementary-symmetry audio amplifier shown in block form in Fig. 287 uses the BDX33 and BDX34 in conjunction with five TO-92 transistors, two diodes, and a 52-volt (with eight-ohm load) or 40-volt (with four-ohm load) single power supply. The high-frequency performance of this amplifier will satisfy the most critical listener. Table XXV lists typical performance data.

The quiescent current in the class AB output stages (Q3 and Q4) of the amplifier, Fig. 291, has been fixed at 30 milliamperes, which places it above the knee of the h_{fe} characteristics of the BDX33 and BDX34 output devices. The bias that establishes this idling current is provided by the BC237 biasing transistor and can be adjusted by resistor R8. Because the biasing transistor is mounted on the heatsink with the output devices, excellent stabilization of the quiescent current with temperature increase is provided.

It is important to note that, as a result of the high unit-gain frequency of the BDX33 and

Table XXIV - Typical Performance Data for 100-Watt Audio Amplifier

Measured at V_{CC}=114 V, T_A=25° C, and a frequency of 1 kHz, unless otherwise specified.

Power:
 Rated power (8 Ω load) . . . . 100 W
 Typical power (4 Ω load) . . . . 100 W*
 Typical power (16 Ω load) . . . . 60 W
Total Harmonic Distortion:
 Rated Distortion . . . . See Fig. 206
IM Distortion . . . . < 0.05%
Sensitivity . . . . 0.9 V for 100 W
Input Impedance. . . . . 10 KΩ
Hum and Noise:
 Below rated power output
  Open input . . . . 100 dB
  Shorted input . . . . 106 dB
Phase Shift . . . . +1° at 20 Hz
                                                                                    −7° at 20 kHz
Slew Rate . . . . 46 V/μs
Rise Time . . . . 1.7 μs
Damping Factor 130

*With a 90-V split power supply and 4-BD550 substituted for 4-BD550A.
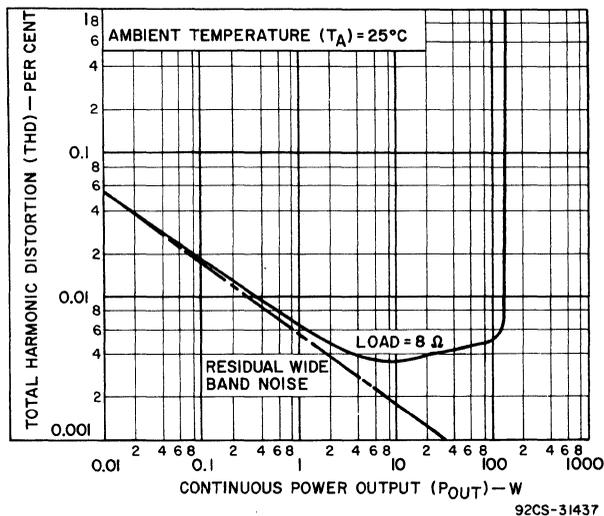
Fig.285 - Typical harmonic distortion as a function of power output for 100-watt amplifier shown in Fig. 283.

BDX34 Darlingtons, the high-frequency operation of the amplifier remains in the highly efficient class B mode, and dissipation and temperature are kept low.

The quiescent current in the driver stage (which must be at least equal to the maximum peak base current required by the n-p-n Darlington) is established by resistors R10 and R11, Fig. 291. The driver current is equal to the difference between the supply voltage and the center voltage divided by the sum of the series resistances (R10 + R11), and is approximately 5 milliamperes.

For proper operation of the circuit, the
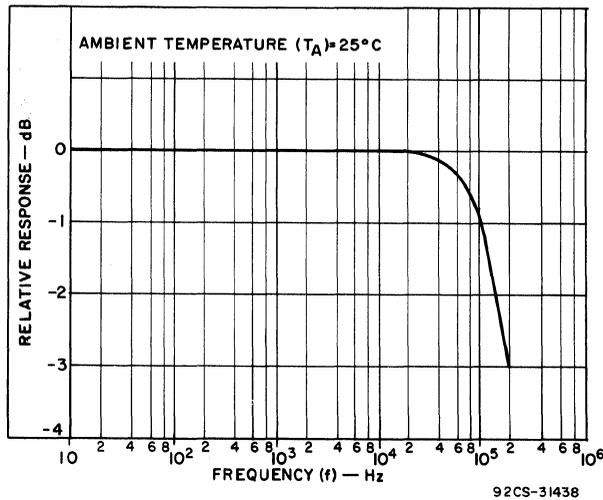
Fig.286 - *Typical frequency response for 100-watt amplifier shown in Fig. 283.*
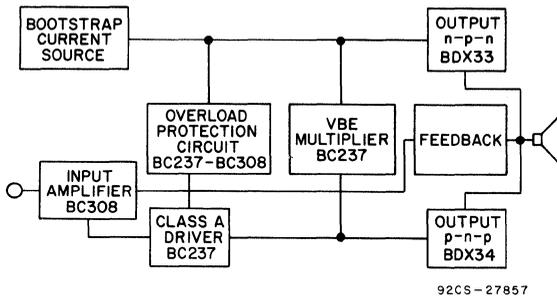
Fig.287 - *Block diagram of the 25-watt, full complementary-symmetry, audio amplifier.*

Table XXV - Typical Performance Data

All measurements made at an ac line voltage of 220 volts, T_A=25° C.		
Power Output	**Load**	
	8-Ohm	**4-Ohm**
At 1000 Hz for harmonic distortion=1%	26 W	28 W
At 1000 Hz for harmonic distortion < 0.1%	24 W	26 W
Total harmonic distortion as a function of power output at 1000 Hz	Figs. 288 and 289	
Total harmonic distortion as a function of power output at 40 Hz	Figs. 288 and 289	
Total harmonic distortion as a function of power output at 15 kHz	Figs. 288 and 289	
Frequency Response At an output of 15 W: 1 dB down 3 dB down	40 Hz to 60 kHz 20 Hz to 80 kHz	50 Hz to 50 kHz 25 Hz to 70 kHz
Sensitivity For power output of 30 W Electrical Stability	360 mV	260 mV
20 kHz square wave 1 kHz square wave 100 Hz square wave	Fig. 290(a) Fig. 290(b) Fig. 290(c)	
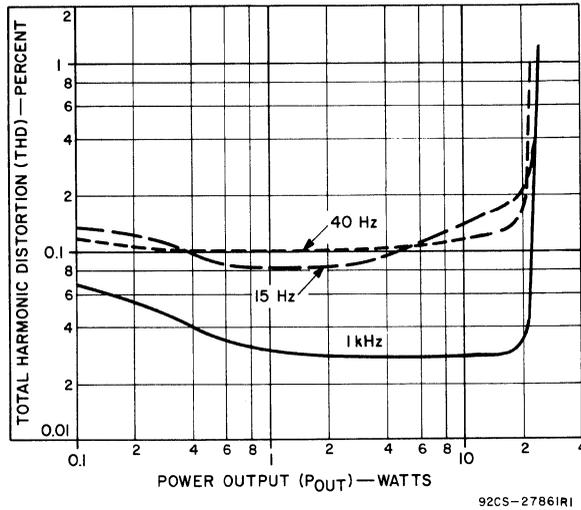
Fig.288 - Total harmonic distortion as a function of power output for the 25-watt amplifier with an eight-ohm load.
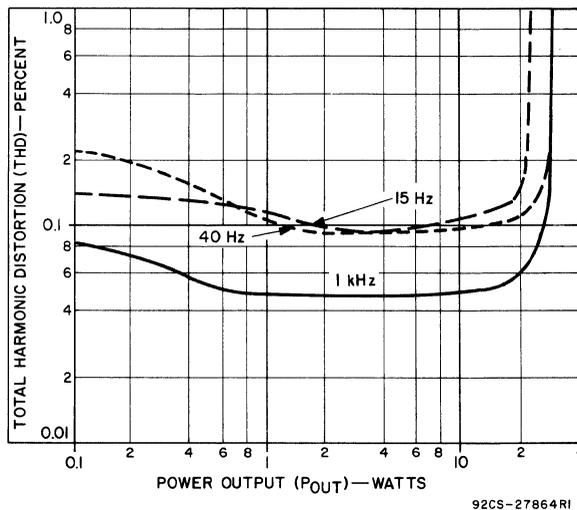
Fig.289 - Total harmonic distortion as a function of power output for the 25-watt amplifier with a four-ohm load.

current I_l flowing through resistor R10 must remain essentially constant during any excursion of the ac output voltage, Fig. 291. For this reason, a 50-microfarad bootstrap capacitor, C6, is connected between the bias resistors and point A. As the voltage across C6 does not change during ac output-voltage excursions, the change in voltage at point B is the same as at point A. The change in voltage at point C is essentially the same as that at

point A; it differs only by the small change in the base-to-emitter voltage of Q3. Therefore, the voltage at points B and C changes by essentially the same amount, and the voltage across resistor R10 remains constant, as does the current I_l.

DC and ac voltages are fed back to the emitter of Q1 to keep the center voltage constant and to assure symmetrical levels of clipping.
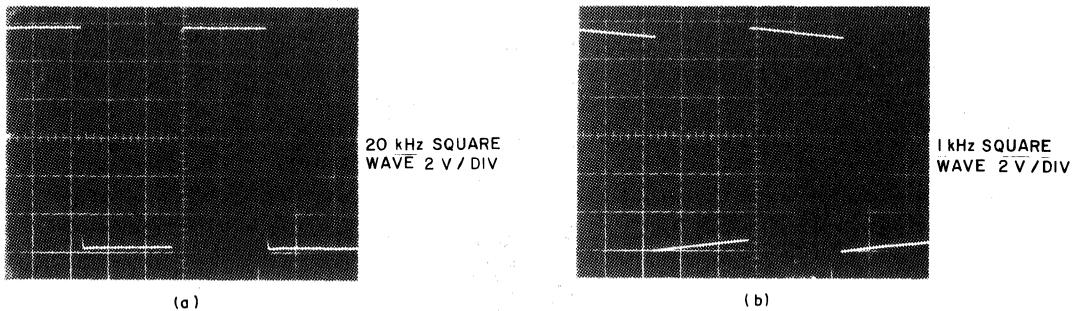
Fig.290 - *Oscilloscope curves demonstrating amplifier stability: (a) 20-kHz square wave, (b) 1-kHz square wave. Scale on all photos is 2 volts per division.*
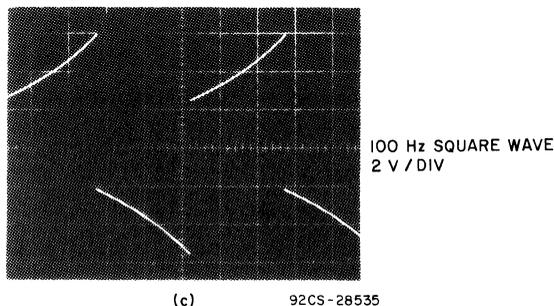
Fig.290 - *Oscilloscope curves demonstrating amplifier stability: (c) 100-Hz square wave. Scale on all photos is 2 volts per division.*

40-Watt Automotive Audio-Power Booster

In recent years, there has been a growing demand for higher power-output capability in automotive tape and audio systems. One of the factors limiting output capability is the 12-volt automotive-system voltage. The following text and illustrations describe the combination of a dc-to-dc regulated up-converter and a simple and economical output amplifier that will deliver 40 watts into a 4-ohm load.

Power Converter

The converter, shown schematically in Fig. 292, is externally excited by an RCA CD4047 integrated-circuit multivibrator operating in the astable mode. The period of the multivibrator is determined by the selection of the values of R and C through the use of the formula: period=4.4 RC. Using the values of R_1 and C_1 indicated in Fig. 292, the period for the circuit shown is 48.4 microseconds, or roughly 20 kilohertz. The Q and $\overline{Q}$ outputs are used to sink base drive for Q_1 and Q_2, which provide primary current for base-drive trans-

former T_1. Because Q_1 and Q_2 are Darlington transistors, they are able to provide a direct interface with the transformer with minimal loading and high current gain; R_2 limits primary current to 400 milliamperes.

T_1 is a 4-to-1 step-down transformer whose secondary is coupled to the bases of inverter-output transistors Q_3 and Q_4. The center tap of the base-drive transformer secondary is coupled to the common emitter leads of these transistors through the bias network consisting of D_1, D_2, R_3, C_2. This network eliminates common-mode conduction in Q_3 and Q_4, thereby increasing the efficiency and improving the thermal stability of the converter. Note that the bias network does not provide forward bias for starting, but just the opposite, and that transistors Q_3 and Q_4 are operated in a class C manner, with negative bias. When the base-drive signals are near the zero-voltage cross-over point, the negative voltage developed across C_2 is the predominant base signal, and the transistor that was on, and is in the process of turning off, experiences a back bias with an energy content sufficient to
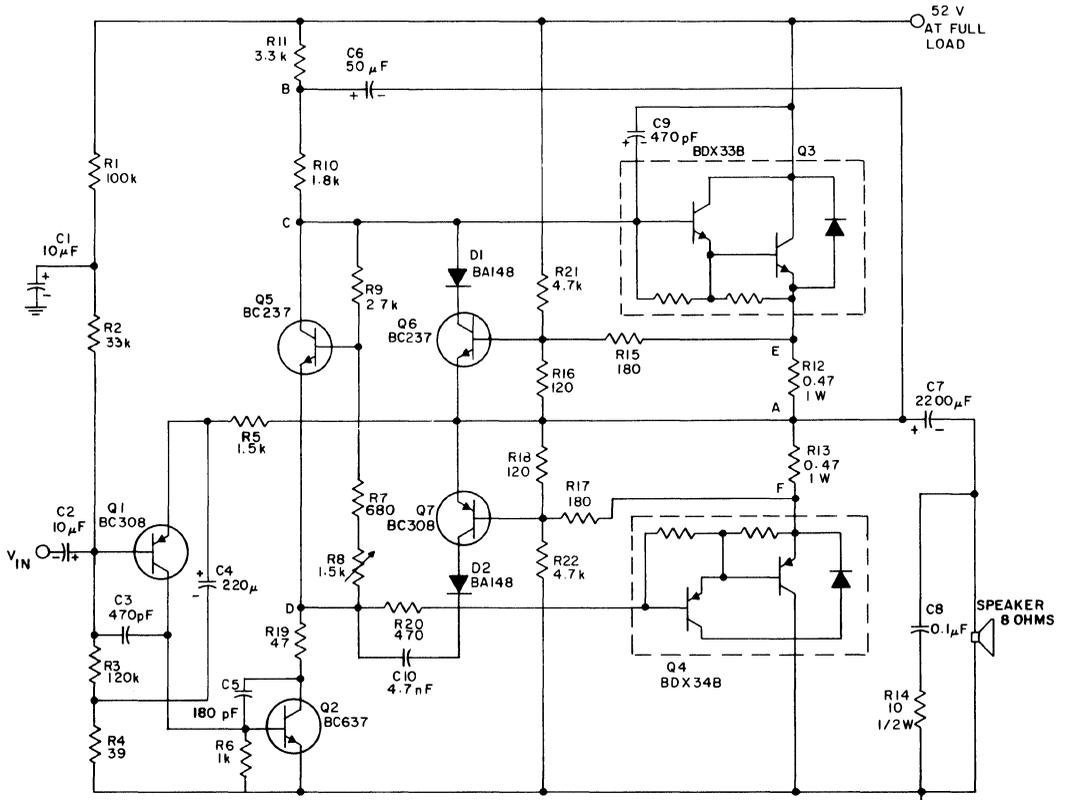
Fig.291 - Schematic diagram of the 25-watt amplifier. Values are given for 8-ohm load.

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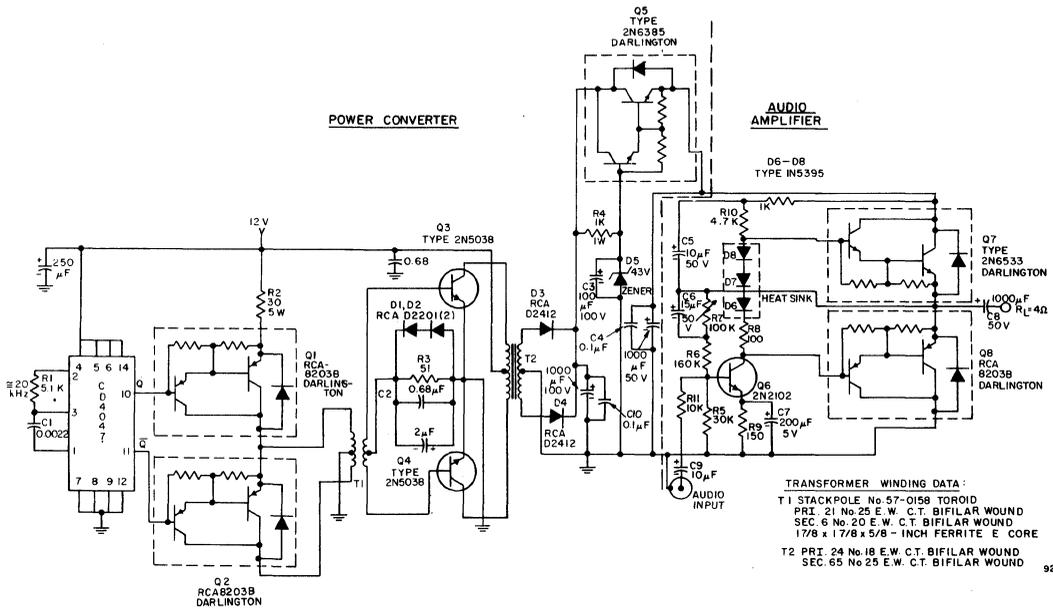
Fig.292 - Schematic diagram of the 40-watt amplifier.

92CL-31873

compensate for a worst-case stored-charge condition, thereby reducing switching dissipation.

T_2, a step-up transformer with a turns ratio of 1 to 5.5, provides an unregulated output voltage of 66 volts across filter-capacitor C_{10} via high-speed rectifier-diodes D_3 and D_4. Since, in the automotive environment, the battery voltage varies depending on loading and engine rpm, a series voltage regulator is provided, with a base control voltage determined by zener-diode D_5, to maintain a constant audio-amplifier operating voltage. A Darlington transistor regulator was selected because of its high current gain and minimal base-drive requirements. Resistor R_4 provides bleeder current through the high side of the unregulated supply; C_3 is placed across D_5 to provide zener stability during peak current loading. As a result of the placement of C_3 in the base circuit of Q_5, a capacitor multiplier circuit is formed that reflects an emitter output capacitance of βC_3, thereby further increasing output-voltage stability.

The output voltage of the converter, which is of greater magnitude than the available system voltage, is now applied to the audio-power-amplifier section of the circuit.

The audio amplifier, also shown schematically in Fig. 292, consists of three transistors that provide an ac gain of approximately sixteen. The output devices labeled Q_7 and Q_8 are Darlington transistors configured in a complementary push-pull output arrangement and using a common power supply. A quiescent voltage equal to one-half the supply voltage exists at the common-emitter junction point, and is maintained by the values of R_5, R_6, and R_7, which provide dc feedback. Resistor R_7 is variable and makes possible a fine adjustment of this feedback voltage.

When a complementary pair of output transistors is used (n-p-n and p-n-p), it is possible to design a series-output type of audio amplifier for which the drive circuitry is substantially simplified relative to other amplifier designs; the series-output does not require push-pull drive because phase inversion is unnecessary. The drive in the series-output circuit of Fig. 292 is developed across R_8 and provides the small amount of forward bias required for class AB operation of the complementary pair of output transistors.

Diodes D_6, D_7, and D_8 are also part of the drive circuit; their purpose is to maintain the quiescent current at a reasonable value with variations in junction temperature. To assure thermal tracking, the diodes are mounted on the output heatsink and track with the V_{BE} of the output transistors, thereby providing thermal stability. Transistor Q_6, operated class A, is dc stabilized by R_9; its high ac gain is assured by bypassing the 150-ohm resistor with a 200-microfarad capacitor. In the past, for output power greater than 20 watts, a quasicomplementary output stage was used; this stage used more costly phase-inverter drivers. These phase-inverter drivers were necessary due to the power dissipation in class A operation of the base-driver stage. The design described in Fig. 292 overcomes the need for the phase-inverter drivers due to the high beta of the Darlington transistors. Consequently, the loading of Q6, the base driver, is greatly reduced to the point that a TO-5 package provides ample output base-drive requirements. This design enhances the thermal stability of the base-driver stage over previous designs using class A stages.

The input resistance of the amplifier is determined by R_{11}, and the gain is set by the ratio of R_6 to R_{11}. Capacitor C_5 provides two functions essential to circuit operation. First, it acts as a bypass to decouple power-supply ripple. Second, it is connected as a "bootstrap" capacitor to provide the drive necessary to pull the upper Darlington transistor into saturation. This latter function results from the fact that the stored voltage of the capacitor, with reference to the common output point, provides a higher voltage than the normal collector-supply voltage required to drive transistor Q_7. This higher voltage is necessary during the signal conditions that exist when the upper transistor is being turned on because the emitter voltage of transistor Q_7 then approaches the normal supply voltage. An increase in the base voltage to a point above this level is required to drive Q_7 into saturation. C_9 provides ac coupling for the audio signal while blocking dc that could upset the biasing of transistor Q_6.

The frequency response for the circuit described is well within hi-fi specifications; the circuit provides a response from 40 hertz to 28 kilohertz within a 3-dB tolerance (Fig. 293). The percentage of total harmonic distortion is less than 1 percent over 75 percent of its rated power output, (Fig. 294).
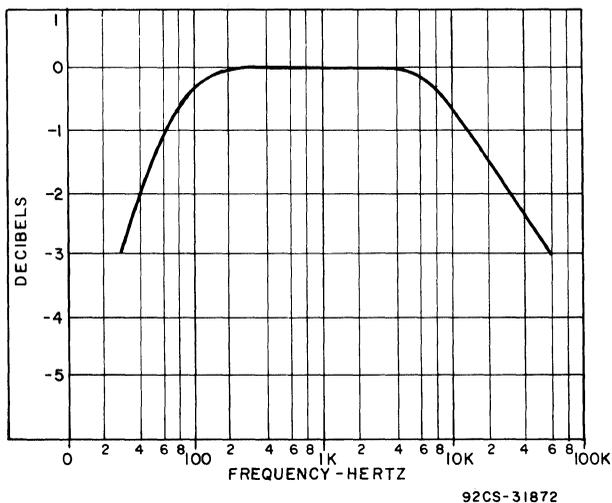
*Fig.293 - Frequency response of the 40-
watt amplifier with a 4-ohm load.*
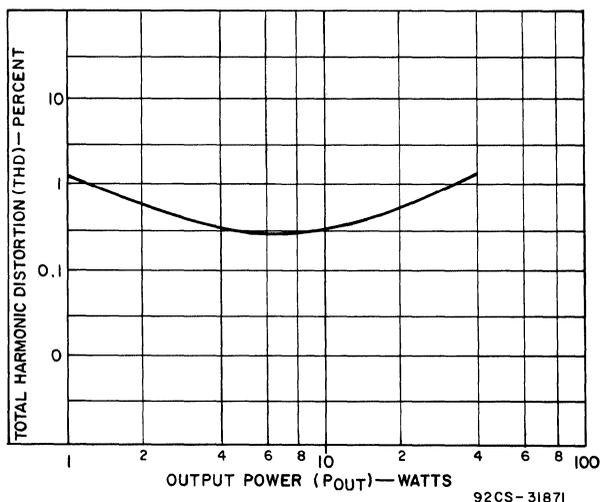
*Fig.294 - Total harmonic distortion at 1
kilohertz with a 4-ohm load.*

One-Hundred-Watt True-Complementary-Symmetry Audio Amplifier

The BD750 and BD751 series of power transistors are complementary p-n-p and n-p-n series, respectively, selected from the ballasted epitaxial-base silicon transistor families, RCA8638 and RCA9116. They feature high-dissipation capability, low saturation voltage, maximum safe-operating area, a gain-bandwidth product (f_T) higher than 4 MHz, and high gain at high current levels. The transistors are especially suitable for use in the output stage of true-complementary high-power audio amplifiers.

Table XXVI shows the peak load voltages and currents ($\hat{V}_L$ and $\hat{I}$, respectively) required for the various output power levels by the output stage of a 100-watt power amplifier with an 8 or 4-ohm load. The table also shows the supply voltage for a typical design and the required V_{CER} capability of the output transistors.

Table XXVI - Characteristics of 80 and 100-Watt Audio Amplifiers

| | Output Power | | | | |
	80 W		100 W		Units
Load impedance: R_L	4	8	4	8	Ω
R_E	0.27	0.68	0 27	0.68	Ω
Peak load current - $\hat{I}$	6.4	4.5	7.1	5	A
Peak load voltage - $\hat{V}_L$	25.3	35.8	28.3	40	V
Typical design supply voltage - V_S	70	94	78	104	V
Output device min. V_{CER} required	90	120	100	130	V
Output device max. dissipation under unclipped sine-wave conditions - P_T	29	26	36	32	W
ϕ at clipping for rated output power - ϕ_M	29	28	29	27	°
Protection circuit (limitation line): R_1	180	470	180	470	Ω
(refers to Fig. 295) R_2	3.9	8.2	3.9	8.2	$K\Omega$
R_3	56	75	50	68	Ω
Short circuited output conditions: I_C (peak)	3.5	2.5	3.7	2.65	A
(f=20 Hz, duty cycle 50%) V_{CE} (peak)	34	45	37.7	50	V
P (max)	119	113	140	133	W
Suggested types: n-p-n	BD751	BD751A	BD751B	BD751C	
p-n-p	BD750	BD750A	BD750B	BD750C	
Suggested types: $I_{s/b}$ capability (DC) $\{$ V_{CE}	35	45	40	50	V
I_C	5.71	4.44	6.25	5	A
P_T	200	200	250	250	W
$R_{\theta\,(j-c)}$	0.875	0.875	0.7	0.7	°C/W
$\Delta T_{(j-c)}$ (max)	73	69	68	65	°C
$\Delta T_{(c-h)}$ (max)	24	23	28	27	°C
T_h (max)	103	108	104	108	°C
T_{cutout} (max)	95	95	95	95	°C
Heatsink thermal resistance per output device $R_{\theta\,ha}$ (B) (T_A (max)=45°C)	1.5	1.7	1.2	1.4	°C/W
Max. working case temperature under unclipped sine-wave conditions at T_A= 45°C - T_C (max)	100	100	103	103	°C

The circuit diagram shown in Fig. 295 consists of an integrated circuit input stage and a power stage composed of discrete transistors; it can be treated as two cascaded gain blocks with one common feedback loop. The discrete gain block has its own local feedback provided by R_{17}, R_{10} and C_8. The integrated circuit for the input stage, A_1, is the CA3100, which offers a high unity-gain crossover frequency, wide power bandwidth, a high slew rate, low noise, and low offset. A parts list, parts layout, and printed-circuit board template for the amplifier are provided in the Appendix.

The input stage of the discrete section is a common base stage (Q_{12}, Q_{13}), which serves as a voltage translator and is operated in the class A mode. The next stage (Q_1, Q_2) is also class A operated; its main purpose is voltage amplification. The top and bottom portions of this stage are connected to the V_{BE} multiplier (Q_3), which provides the bias for the output section (driver Q_8, Q_9 and output Q_{10} and Q_{11}). The quiescent current can be adjusted by means of R_{22}; in the practical amplifier under discussion, it was fixed at 200 milliamperes. The driver and output stages are the emitter-follower stages that achieve needed current gain.

A load-line-limiting circuit (Q_6, Q_4 and Q_7, Q_5) is connected across the inputs of the driver stage. As explained above, this load-line
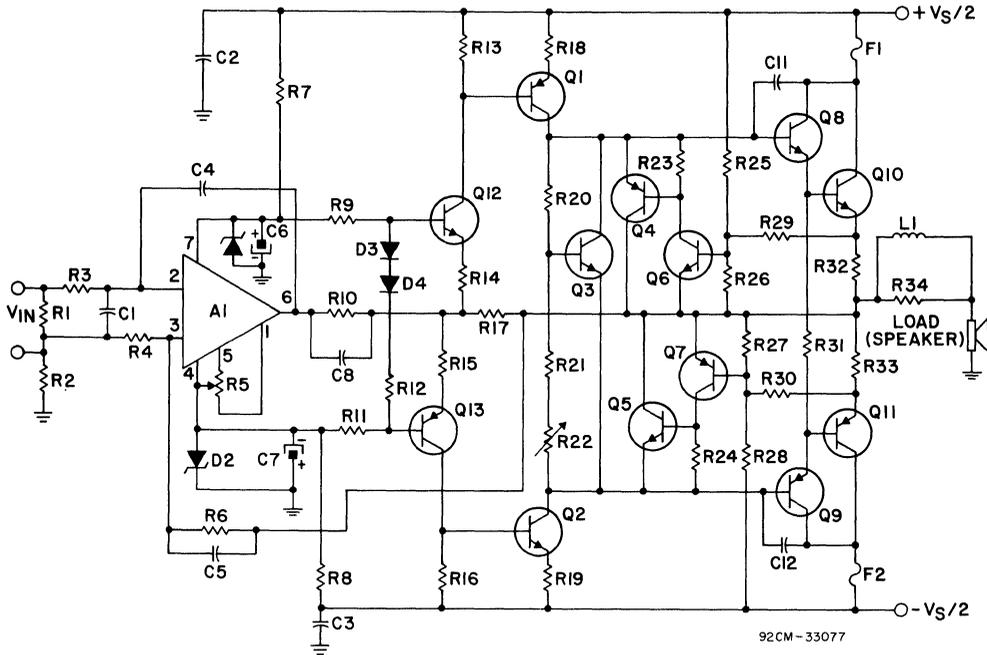
Fig.295 - Circuit of a dc-coupled 100-watt audio amplifier.
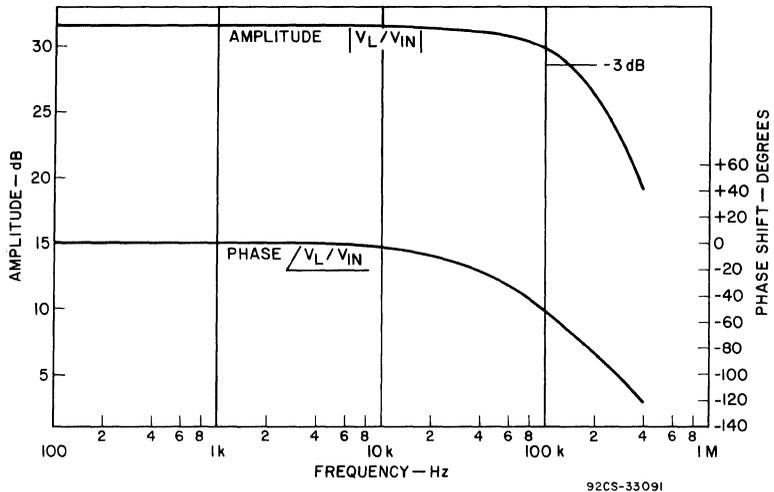
Fig.296 - Typical frequency response of the complete amplifier of Fig. 295.

limiting is necessary to protect the amplifier against excessive dissipation and possible destruction under overload or short-circuited output conditions. In the practical amplifier, two transistors are used for each half of the circuit.

With the component values given in the Appendix, the cut-off frequency at –3 dB of the open-loop response of the discrete section of the 100-watt amplifier is approximately 1 kHz. Fig. 296 gives the typical frequency response of the complete amplifier shown in Fig. 295. Typical performance data for 100-watt audio amplifiers with 4 and 8-ohm loads is provided in Table XXVII and Figs. 296, 297, 298 and 299.

Table XXVII - Typical Performance Data for 100-Watt, 4 and 8-Ohm Audio Amplifiers

Rated Power	100 W	100 W
Load Impedance	4 Ω	8 Ω
Sensitivity	530 mV	750 mV
Input Impedance	10 KΩ	10 KΩ
Slew Rate	25 V/μs	25 V/μs
Frequency Response ············..················	See Fig. 296	
Square-wave Response ····························	See Fig. 297	
Total Harmonic Distortion ······················	See Figs. 298 and 299	

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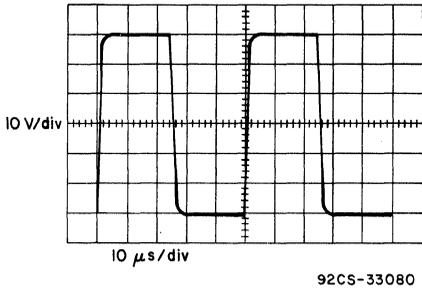
Fig.297 - 20-kHz square-wave output waveform.

92CS-33076

Fig.298 -

Total harmonic distortion as a function of frequency.

92CS-33075
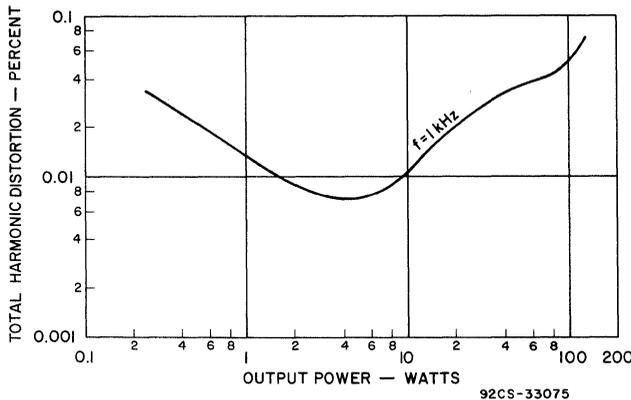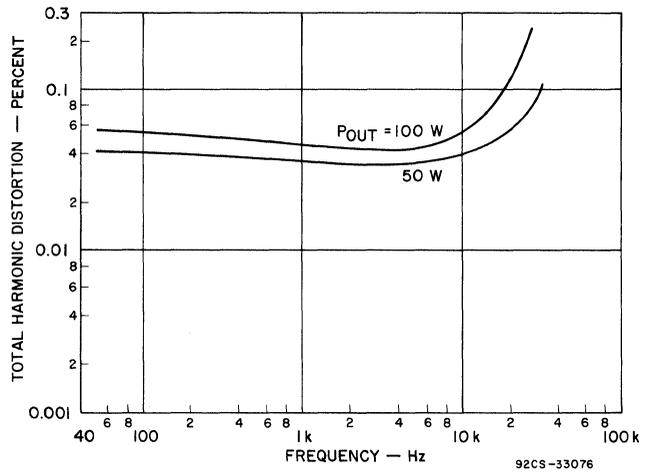
Fig.299 -

Total harmonic distortion as a function of output power.
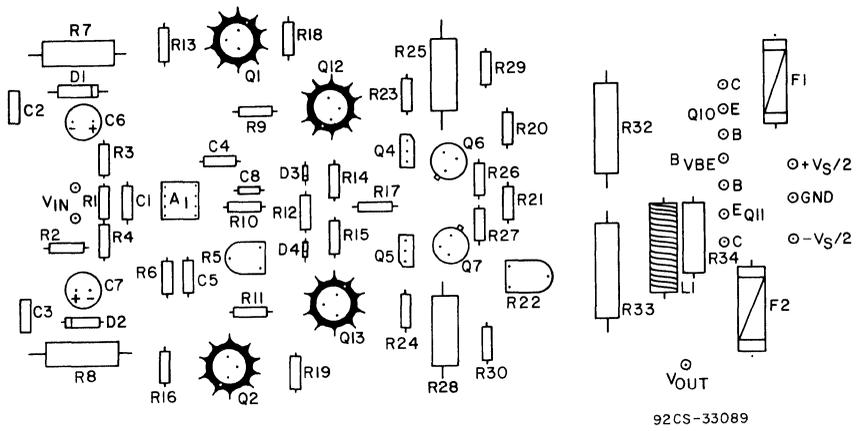
Fig.300 - Components side of PC board.
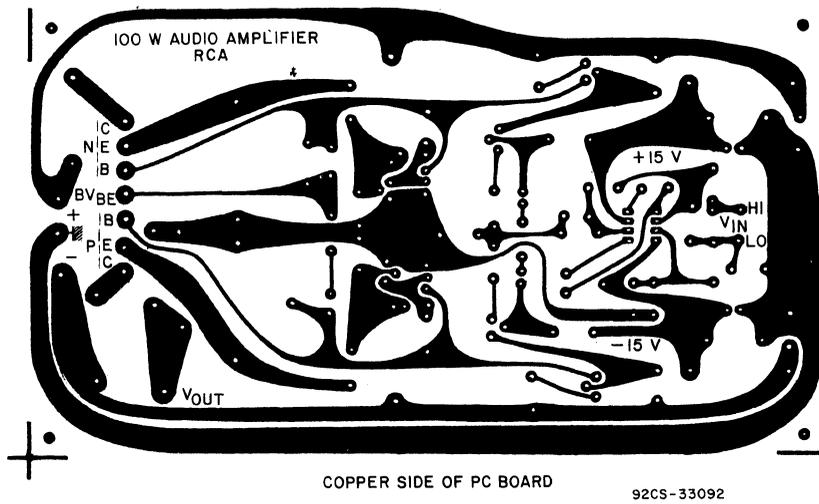
Fig.301 - Copper side of PC board.

Parts List for Amplifier of Fig. 295 with 4 or 8-Ohm Load

Components	4 Ohms	8 Ohms	Components	4 Ohms	8 Ohms
R1 (Note 1)	10 K	10 K	C1	100 pF	100 pF
R2	1	1	C2	0.47 μF, 50 V	0.47 μF, 50 V
R3	1 K	1 K	C3	0.47 μF, 50 V	0.47 μF, 50 V
R4	220	220	C4	12 pF	12 pF
R5 (Note 2)	Pot, 10 K	Pot, 10 K	C5	100 pF	100 pF
R6	8.2 K	8.2 K	C6	22 μF, 25 V	22 μF, 25 V
R7	1 K, 1 W	1.8 K, 1 W	C7	22 μF, 25 V	22 μF, 25 V
R8	1 K, 1 W	1.8 K, 1 W	C8	10 nF	10 nF
R9	1.8 K	1.8 K	C11 (Note 7)	3.9 nF	3.9 nF
R10	2.2 K	2.2 K	C12 (Note 7)	3.9 nF	3.9 nF
R11	1.8 K	1.8 K			
R12	220	220	D1	Zener, 15 V	Zener, 15 V
R13	4.7 K	1.8 K	D2	Zener, 15 V	Zener, 15 V
R14	820	820	D3	1N4148	1N4148
R15	820	820	D4	1N4148	1N4148
R16	4.7 K	1.8 K			
R17	39 K	39 K	Q1 (Note 4)	RCA1A10	RCA1A10
R18	47	47	Q2 (Note 4)	RCA1A11	RCA1A11
R19	47	47	Q3 (Note 5)	RCA1A18	RCA1A18
R20	390	1 K	Q4	RCP700A	RCP700A
R21	56	56	Q5	RCP701A	RCP701A
R22 (Note 3)	Pot, 1 K	Pot, 1 K	Q6	RCA1A18	RCA1A18
R23	100	100	Q7	RCA1A19	RCA1A19
R24	100	100	Q8 (Note 6)	RCA1C03	2N6474
R25	3.9 K, 1 W	8.2 K, 1 W	Q9 (Note 6)	RCA1C04	2N6476
R26	50	68	Q10 (Note 6)	BD751B	BD751C
R27	50	68	Q11 (Note 6)	BD750B	BD750C
R28	3.9 K, 1 W	8.2 K, 1 W	Q12 (Note 4)	RCA1A11	RCA1A11
R29	180	470	Q13 (Note 4)	RCA1A10	RCA1A10
R30	180	470			
R31 (Note 7)	100	100	A1	CA3100	CA3100
R32	0.27, 7 W	0.68, 7 W			
R33	0.27, 7 W	0.68, 7 W	F1	4 A	3 A
R34	4.7, 1 W	10, 1 W	F2	4 A	3 A
			L1	2 μH	4 μH
			V_s	78 V	104 V

Notes for Parts List:
1. All resistors are non-inductive.
2. Adjust for an output of zero volts with zero volts at the input.
3. Adjust for a quiescent current of 200 mA.
4. Mount each device on heatsink of 30 cm^2 minimum area.
5. Mount on same heatsink as driver and output devices Q_8, Q_9, Q_{10} and Q_{11}.
6. Provide heatsinking as described in text.
7. These components cannot be found on the components layout of Fig. 300. They are to be mounted directly on the driver-device sockets that are fixed on the heatsink.

TV Deflection Systems

For reproduction of a transmitted picture in a television receiver, the face of a cathode-ray tube is scanned with an electron beam while the intensity of the beam is varied to control the emitted light at the phosphor screen. The scanning is synchronized with a scanned image at the TV transmitter, and the black-through-white picture areas of the scanned image are converted into an electrical signal that controls the intensity of the electron beam in the picture tube at the receiver.

SCANNING FUNDAMENTALS

The scanning procedure used in the United States employs horizontal linear scanning in an odd-line interlaced pattern. The standard scanning pattern for television systems includes a total of 525 horizontal scanning lines in a rectangular frame having an aspect ratio of 4 to 3. The frames are repeated at a rate of 30 per second, with two fields interlaced in each frame. The first field in each frame consists of all odd-number scanning lines, and the second field in each frame consists of all even-number scanning lines. The field repetition rate is thus 60 per second, and the vertical scanning rate is 60 Hz. (For color systems, the vertical scanning rate is 59.94 Hz.)

The picture on the face of a television picture tube is formed by rapid movement of a single spot of light in both horizontal and vertical directions. This spot of light is produced when the electron beam strikes the fluorescent screen; the brightness of the spot varies in proportion to the amplitude of the video signal. The electron beam moves under the influence of two magnetic fields. One field causes the beam to move (scan) horizontally across the face of the picture tube; the other field causes the beam to move from top to bottom.

Fig. 302 illustrates the basic scanning principle. This diagram assumes that the beam starts at the upper left corner of the
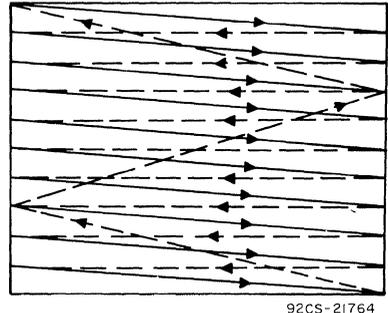
92CS-21764

Fig. 302 - Non-interlaced scanning.

picture area, sweeps rapidly across and simultaneously moves **downward** at a very small slope to the opposite edge of the screen. The beam then jumps back, or retraces, much more rapidly to the left edge, and starts across again at a point lower down as shown.

The two magnetic fields which cause the beam to sweep across the face of the picture tube are so related that the beam scans 262½ times across the face of the picture tube horizontally for every time it scans once across the tube vertically. Each complete picture is "scanned" twice in a time interval of 1/30th second. Therefore, the rate at which a complete picture is scanned, or at the frame rate, is 30 frames per second. Persistence of vision makes it practical to portray motion very well with this frame rate.

A picture or "raster" of 262½ lines presents two problems which make it unsatisfactory for commercial television use. First, a line structure of 262½ lines is relatively coarse and can be readily seen at normal viewing distances and, of course, imposes a severe limitation on vertical resolution. Second, although the eye with its persistence of vision averages a succession of still pictures into apparent smooth motion, it does not filter out the periodic brightness changes as the complete frames are presented and cut off at a 30 frames-per-second rate.

The vertical resolution is improved and the flicker effect is eliminated if the scanning pattern is changed from the simple one first discussed to a pattern called **interlaced scanning**.

In interlaced scanning, as shown in Fig. 303, the beam skips every even-numbered line in scanning the entire picture, then jumps back and sweeps over the even-numbered lines. In other words, on its first trip, the beam scans all the odd-numbered lines (1,3,5,7 . . .), on the second trip, the beam scans even-numbered lines (2,4,6,8 . . .). All this action occurs in the time of one frame (1/30 second).

— 1ST FIELD – – –2ND FIELD
92CS-21765
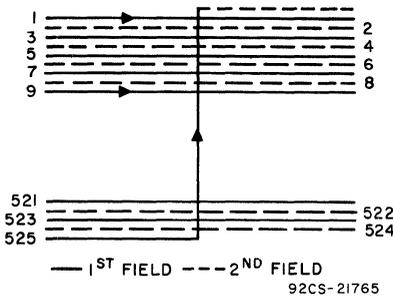
Fig. 303 - Interlaced scanning.

Although the eye has received two distinct light impressions for each frame, each spot on the screen has actually been scanned only once. The effect on the eye is the same as though 60 complete pictures per second were transmitted instead of 30, and the eye is quite insensitive to this flicker rate.

It would have been possible to select a frame rate of 24, which has been used for movies, and a flicker rate of 48 would probably be tolerable. However, a frame rate which is an integral multiple or submultiple of the 60-Hz line frequency minimizes the effect of any picture distortion produced by factors such as poor power-supply filtering, wiring pickup, and heater-cathode leakage in the picture tube. Such effects produce a stationary distortion pattern for a 60-Hz flicker rate. If another frame frequency were used, a continuously moving distortion pattern would result. Experiments have shown that a moving distortion pattern is much more annoying than a stationary one.

Although the complete television picture is made up of 525 lines, not all these lines are actually used in forming the picture on the face of the picture tube. If the lines on the picture tube were counted, only about 480 "active" lines would be visible. The missing lines are blanked out during the retrace period. The reasons for this blanking will become obvious during the discussion on synchronization, later in this section.

Two complete fields are scanned vertically in one 30-Hz frame, the vertical scanning rate, therefore, is 2 x 30, or 60 Hz. For each 30-Hz frame, there must be 525 horizontal lines, so the horizontal scanning rate is 30 x 525 or 15,750 Hz.

Composite Video Signal

The standard television signal has four major components: (1) the picture information which is generated during active scanning time, (2) picture blanking pulses, (3) picture synchronizing pulses, and (4) an average dc component.

Picture Information—Picture information, which is the basic part of the signal, is a series of waves and pulses generated during the active line scanning of the camera tube. For a monochrome picture, as the electron beam traverses the face of the camera tube, its amplitude is modulated in accordance with the brightness of the scene it is scanning. Fig. 304 shows a very simple scene being scanned, and the electrical brightness signal from the camera that corresponds to one scanning line.

SCANNING LINE

SIMPLE PICTURE SCENE

ELECTRICAL SIGNAL CORRESPONDING
TO SCANNING LINE

92CS-21766
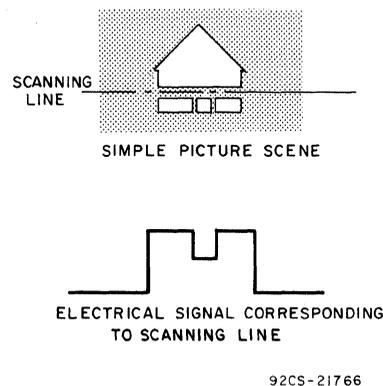
Fig. 304 - Video signal for one scanning line.

For color pictures, the three color-difference signals are added to the monochrome, or Y, signal, as explained later in the discussion of **Color Synchronization**.

Blanking Signals—During retrace periods, the camera pickup tube may generate spurious signals. Also, during this period, retrace lines in either the camera tube or in the picture-tube in the receiver can detract from the appearance of the picture. Blanking pulses are applied to the scanning beams in both the pickup camera and in the receiver picture tube to eliminate retrace lines and the unwanted information from the picture during retrace.

A standard blanking signal has been agreed upon by the television industry. The blanking signal is actually part of the signal produced by the synchronizing circuit. It is a pulse somewhat longer than the synchronizing pulse, but of smaller amplitude. The magnitude of this pulse is held at the proper value to cut off the scanning beam during retrace. This level is called the **black level**, because during the time the signal from the transmitter is at that level the beam does not produce any light on the face of the picture tube. Fig. 305 shows how the picture information is combined with the blanking pulses and synchronizing pulses to form the composite video signal. It should be noted that the undesired signals have been pushed down below the black level.
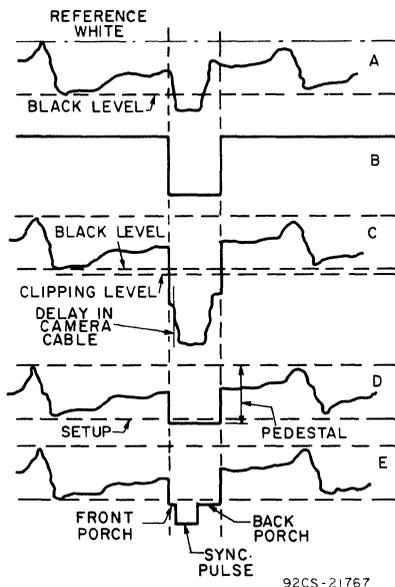
Fig. 305 - *Steps in synthesis of picture signal.*

Actually, there are two blanking signals, because the beam must move both vertically and horizontally. The **horizontal blanking pulses** are transmitted at the end of each line at

intervals of 1/15,750 second (1/15,374 second for color broadcasts) and blank the beam during the retrace period between lines. **Vertical blanking pulses** are transmitted at the end of each field, at the bottom of the picture, at intervals of 1/60 second (1/59.94 second for color), and blank the beam during the time required for its return to the top of the picture.

Synchronizing Signals—The attainment of a viewable picture on the face of the picture tube requires that the scanning beams in the camera and the receiver be in exact synchronism at all times. This synchronization is provided in the form of electrical pulses during the retrace interval between successive lines of the picture and between successive pictures. These pulses are generated at the transmitting end in the equipment which controls the scanning beam of the camera pickup tube and becomes a part of the composite signal which is transmitted. Synchronizing signals should (1) provide positive synchronization of both horizontal and vertical sweep circuits, (2) be separable by simple electrical circuits to recover the vertical and horizontal components of the composite synchronizing signal, and (3) be able to combine simply with the picture.

Because proper synchronization is absolutely essential to obtain a usable picture, the synchronizing signals are made to be the strongest ones that the transmitter can produce. The level of the picture signal itself is not allowed to exceed 75 percent of the full transmitter power (black level); the full power of the transmitter, however, is used to transmit the sync pulses. The task of separating the sync pulses from the rest of the signal at the receiver, therefore, is simplified. Fig. 306 shows the waveform of a radiated picture signal, together with a horizontal sync pulse.
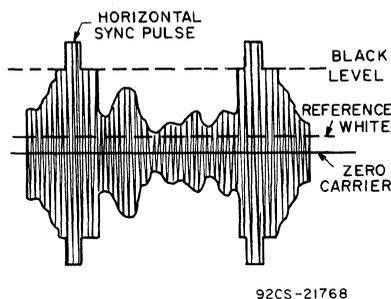
Fig. 306 - *Waveform of radiated picture signal.*
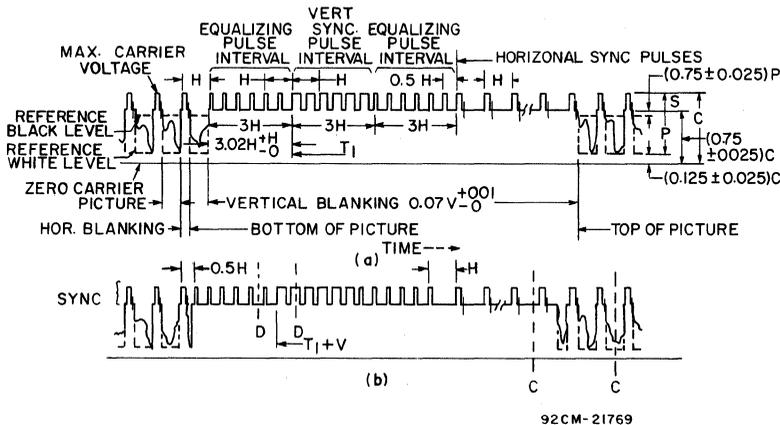
Fig. 307 - Standard FCC video wave-forms.

The reference white line indicated on the sketch is relatively close to zero carrier level (12.5 percent), the synchronizing pulses, however, are in the "blacker than black" region that represents maximum carrier power. Fig. 307 shows how the synchronizing signal waveform is added to the picture signal.

The horizontal and vertical synchronizing pulses have the same amplitude, but different waveshapes and time durations. Frequency discrimination techniques, therefore, can then be used to separate them in the receiver.

The vertical synchronizing pulses are rectangular in shape, but are of much greater duration than the horizontal pulses. The difference in the time duration of the two types of pulses provides a means of frequency discrimination. Each vertical synchronizing pulse has six slots (serrations) in it, so that it appears to be a series of six wide pulses at the horizontal frequency. The width of the slots in the vertical sync pulses is approximately equal to the width of the horizontal sync pulses. Although the slots do not assist in vertical synchronization, they do provide uninterrupted synchronizing information to the horizontal oscillator during the vertical sync interval. The slots are spaced one horizontal line apart so that the receiver can use this pulse information to keep the horizontal oscillator in synchronization.

One of the most difficult problems in synchronization is that of maintaining accurate interlacing. Variations in either the timing or the amplitude of the vertical scanning of alternate fields will cause a vertical displacement of the interlaced fields. The result is a

nonuniform spacing of the scanning lines. This effect, which is usually called "pairing," reduces the vertical resolution and makes the line structure of the picture visible at normal viewing distance. Because the two interlaced fields are displaced by half a line with an equivalent frame rate of 30 Hz, there is an inherent 30-Hz component in the synchronizing signal. If even a minute portion of this 30-Hz component gets into the vertical oscillator, it will inevitably cause pairing.

The pairing problem is minimized and continuous horizontal synchronization throughout the vertical sync and blanking intervals is assured by addition of another series of pulses, called "equalizing pulses," just before and just after the vertical sync pulses. The repetition frequency of the equalizing pulses and of the slots in the vertical sync pulse is twice the horizontal rate. Therefore, the pulses are spaced half a horizontal line apart. The horizontal oscillator will "trigger" on every odd pulse in the first field and on every even pulse in the second field and, therefore, provides interlace as shown previously in Fig. 303.

Color Synchronization—For color receivers, an additional synchronizing signal is required. The demodulators must be supplied with locally generated continuous-wave 3.58-MHz signals, which are precisely locked in frequency and in phase with the color subcarrier signals applied to the modulators at the transmitter, in order to function properly and demodulate the proper colors. The 3.58-MHz local oscillator in the receiver is synchronized in frequency and in phase by a

synchronizing signal sent out by the trans-
mitter. This **color-sync signal** consists of a
short burst of 3.58-MHz signal transmitted
during the horizontal-blanking interval and
following the horizontal-sync interval, as
shown in Fig. 308. The phase of this **burst
signal** is the reference phase for the system. It

is chosen to coincide with the phase of the
$-E_{(B-Y)}$ color-difference signal, as shown in
Fig. 309. Fig. 310 shows how the burst signal
is used in a color television receiver.
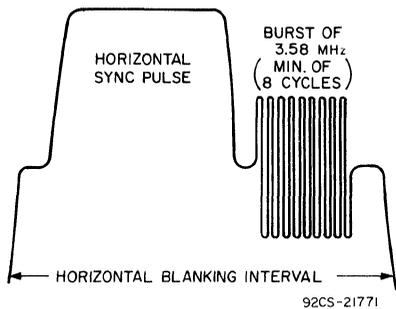
Fig. 308 - *A synchronizing signal, con-
sisting of about 8 cycles of the
subcarrier signal at the refer-
ence phase, is transmitted in
short bursts following every
horizontal sync pulse.*
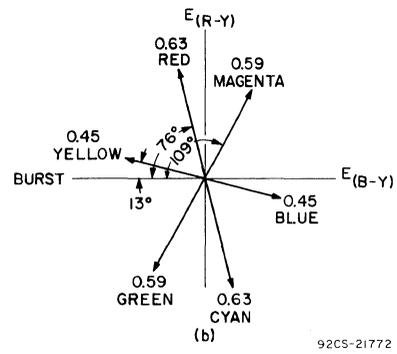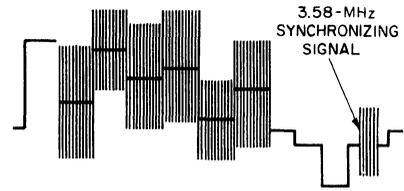
Fig. 309 - *Addition of burst to color
signal.*
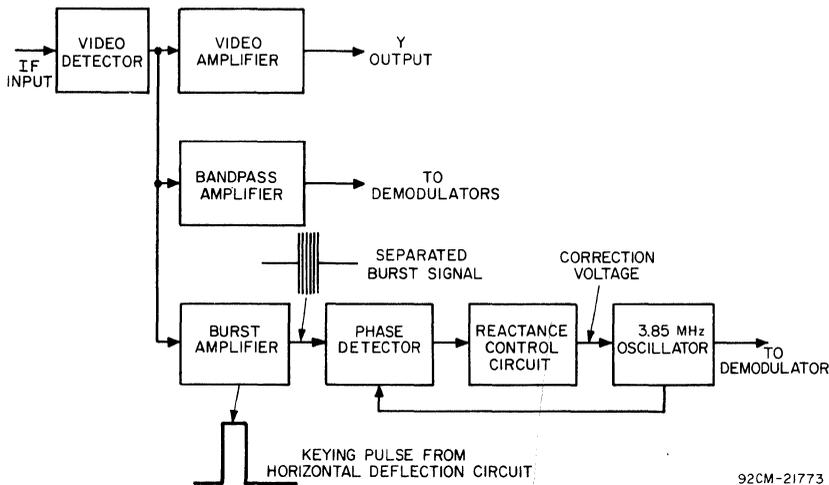
Fig. 310 - *The color subcarrier synchronizing system. (This system resembles
horizontal AFC system. The oscillator signal is compared with the
burst signal and an error in phase produces a dc correction voltage
that forces the oscillator to operate at the correct phase.)*

The composite video signal, which includes the burst signal as well as the chrominance signal, is applied to a burst amplifier, which is tuned to 3.58 MHz. In the absence of a keying pulse, this amplifier is cut off, or non-conducting. A keying pulse, delayed by an appropriate amount to be coincident with the burst signal, is derived from the horizontal deflection circuit and drives the burst amplifier into conduction. The burst amplifier, therefore, amplifies the burst signal, but is cut off for most of the composite video signal. After separation in this way, the amplified burst signal is applied to a phase detector in which it is compared with another 3.58-MHz signal obtained from the local subcarrier oscillator. Any error in frequency or instantaneous phase of the locally generated subcarrier produces a dc output from the phase detector. This correction voltage is used to correct the phase of the subcarrier oscillator through a reactance control circuit.

DC Component—Most sound systems, even the best high fidelity systems, use ac coupling and do not reproduce frequencies below 15 to 20 Hz. This limitation does not impose any special problem because the human eye is incapable of responding to frequencies below 15 to 20 Hz. The eye, however, can perceive both absolute intensities of light and very slow variations in intensity. As the frequency of the variations increases, the eye soon loses its ability to follow the changes and tends to respond to the average of the variations. This phenomenon, which is called **persistency of vision**, makes it possible for the eye to see a rapid succession of still pictures as apparent smooth, uninterrupted motion.

Because the eye can recognize slow changes in light intensity, a television system must be able to transmit these slow changes to the receiver and to the screen of the picture tube. The system must either pass the entire TV spectrum, including the dc component, through each stage, or the signal must contain

information which makes it possible to restore the dc component in the receiver.

The loss of the dc component results in a signal which tends to adjust itself about its own ac axis. Fig. 311(a) shows the video signal when the dc component is present. Fig. 311(b) shows the effect on this signal when the dc component is lost.
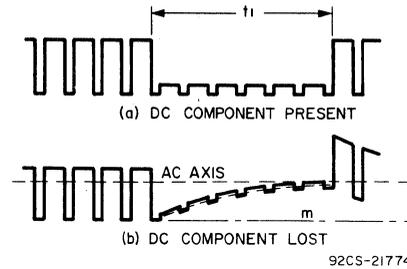
Fig. 311 - DC component of video signal.

Addition of the dc component by means of a dc restorer will restore the signal to its original form, shown in Fig. 311(a). As shown in Fig. 311(b), when the dc component is lost, the peak-to-peak excursions of the signal are considerably increased and require a greater amplitude excursion from the amplifiers through which the signal must pass. Therefore, it is sometimes desirable to reinsert the dc component at earlier points in the system, in addition to restoring it at the picture tube. DC restoration also tends to reduce hum, switching surges, and some spurious signals.

Sync Pulses

In addition to picture information, the composite video signal from the video detector of a television receiver contains timing pulses to assure that the picture is produced on the faceplate of the picture tube at the right instant and in the right location. These pulses, which are called sync pulses, control the horizontal and vertical scanning generators of the receiver.

Fig. 312 shows a portion of the detected
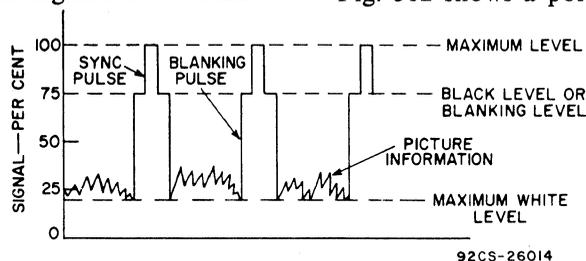
Fig. 312 - Detected video signal.

video signal. When the picture is bright, the amplitude of the signal is low. Successively deeper grays are represented by higher amplitudes until, at the "blanking level" shown in the diagram, the amplitude represents a complete absence of light. This "black level" is held constant at a value equal to 75 per cent of the maximum amplitude of the signal during transmission. The remaining 25 per cent of the signal amplitude is used for synchronization information. Portions of the signal in this region (above the black level) cannot produce light.

In the transmission of a television picture, the camera becomes inactive at the conclusion of each horizontal line and no picture information is transmitted while the scanning beam is retracing to the beginning of the next line. The scanning beam of the receiver is maintained at the black level during this retrace interval by means of the blanking pulse shown in Fig. 312. Immediately after the beginning of the blanking period, the signal amplitude rises further above the black level to provide a horizontal-synchronization pulse that initiates the action of the horizontal scanning generator. When the bottom line of the picture is reached, a similar vertical-synchronization pulse initiates the action of the vertical scanning generator to move the scanning spot back to the top of the pattern.

Sync Separation

The sync pulses in the composite video signal are separated from the picture information in a **sync-separator stage**, as shown in Figs. 313 and 314. This stage is biased sufficiently beyond cutoff so that current flows and an output signal is produced only at the peak positive swing of the input signal. In the diode circuit of Fig. 313, negative bias for the diode is developed by R and C as a result of the flow of diode current on the positive extreme of signal input. The bias automatically
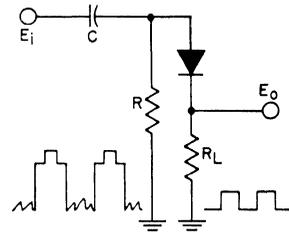
Fig. 313 - Diode sync-separator circuit.
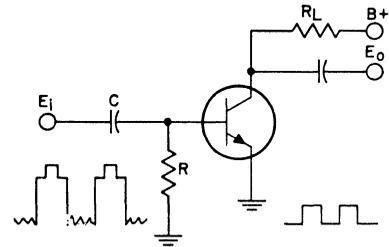
Fig. 314 - Transistor sync-separator circuit.

adjusts itself so that the peak positive swing of the input signal drives the anode of the diode positive and allows the flow of current only for the sync pulse. In the circuit shown in Fig. 314, the base-emitter junction of the transistor functions in the same manner as the diode in Fig. 313, but in addition the pulses are amplified.

After the synchronizing signals are separated from the composite video signal, it is necessary to filter out the horizontal and vertical sync signals so that each can be applied to its respective deflection generator. This filtering is accomplished by RC circuits designed to filter out all but the desired synchronizing signals. Although the horizontal, vertical, and equalizing pulses are all rectangular pulses of the same amplitude, they differ in frequency and pulse width, as shown in Fig. 315. The
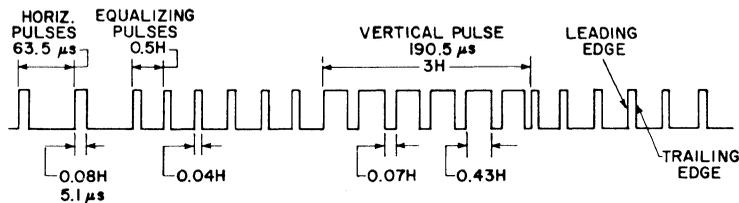
Fig. 315 - Waveform of TV synchronizing pulses (H=horizontal line period of 1/15,750 seconds, or 63.5 μs).

horizontal sync pulses have a repetition rate of 15,750 per second (one for each horizontal line) and a pulse width of 5.1 microseconds. (For color systems, the repetition rate of the horizontal sync pulses is 15,734 per second.) The equalizing pulses have a width approximately half the horizontal pulse width, and a repetition rate of 31,500 per second; they occur at half-line intervals, with six pulses immmediately preceding and six following the vertical synchronizing pulse. The vertical pulse is repeated at a rate of 60 per second (one for each field), and has a width of approximately 190 microseconds. The serrations in the vertical pulse occur at half-line intervals, dividing the complete pulse into six individual pulses that provide horizontal synchronization during the vertical retrace. (Although the picture is blanked out during the vertical retrace time, it is necessary to keep the horizontal scanning generator synchronized.)

All the pulses described are produced at the transmitter by the synchronizing-pulse generator; their waveshapes and spacings are held within very close tolerances to provide the required synchronization of receiver and transmitter scanning.

The horizontal sync signals are separated from the total sync in a differentiating circuit that has a short time constant compared to the width of the horizontal pulses. When the total sync signal is applied to the differentiating circuit shown in Fig. 316, the capacitor charges completely very soon after the leading edge of each pulse, and remains charged for a period of time equal to practically the entire pulse width. When the applied voltage is removed at the time corresponding to the trailing edge of each pulse, the capacitor discharges completely within a very short time. As a result, a positive peak of voltage is obtained for each leading edge and a negative peak for the trailing edge of every pulse. One polarity is produced by the charging current for the leading edge of the applied pulse, and the opposite polarity is obtained from the discharge current corresponding to the trailing edge of the pulse.

As mentioned above, the serrations in the vertical pulse are inserted to provide the differentiated output needed to synchronize the horizontal scanning generator during the time of vertical synchronization. During the vertical blanking period, many more voltage peaks are available than are necessary for horizontal synchronization (only one pulse is used for each horizontal line period). The check marks above the differentiated output in Fig. 316 indicate the voltage peaks used to synchronize the horizontal deflection generator for one field. Because the sync system is made sensitive only to positive pulses occurring at approximately the right horizontal timing, the negative sync pulses and alternate differentiated positive pulses produced by the equalizing pulses and the serrated vertical information have no effect on horizontal timing. It can be seen that although the total sync signal (including vertical synchronizing information) is applied to the circuit of Fig. 316, only horizontal synchronization information appears at the output.

The vertical sync signal is separated from
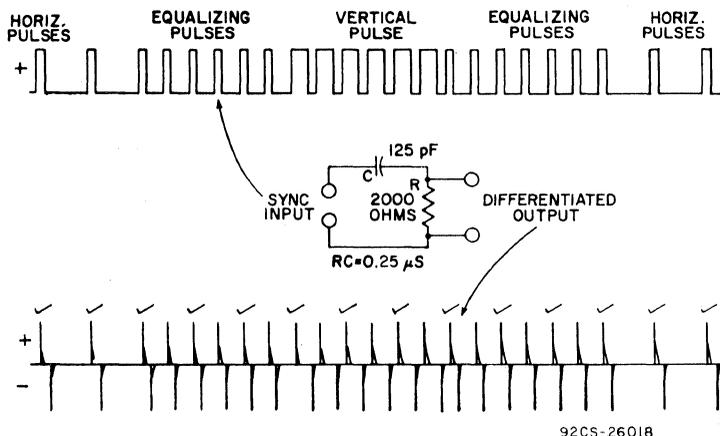
Fig. 316 - Separation of the horizontal sync signals from the total sync by a differentiating circuit.

the total sync in an integrating circuit which has a time constant that is long compared with the duration of the 5-microsecond horizontal pulses, but short compared with the 190-microsecond vertical pulse width. Fig. 317 shows the general circuit configuration used, together with the input and output signals for both odd and even fields. The period between

92CS-26019
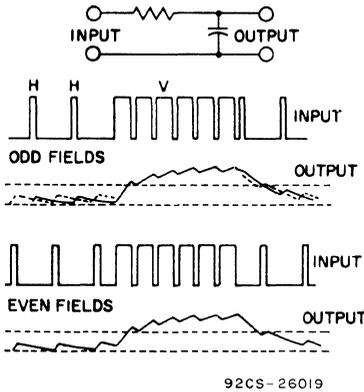
Fig. 317 - Separation of vertical sync signals from the total sync for odd and even fields with no equalizing pulses. (Dashed line indicates triggering level for vertical scanning generator.)

horizontal pulses, when no voltage is applied to the RC circuit, is so much longer than the horizontal pulse width that the capacitor has time to discharge almost down to zero. When the vertical pulse is applied, however, the integrated voltage across the capacitor builds up to the value required for triggering the vertical scanning generator. This integrated voltage across the capacitor reaches its maximum amplitude at the end of the vertical pulse, and then declines practically to zero, producing a pulse of the triangular waveshape shown for the complete vertical synchronizing pulse. Although the total sync signal (including horizontal information) is applied to the circuit of Fig. 314, therefore, only vertical synchronization information appears at the output.

The vertical synchronizing pulses are repeated in the total sync signal at the field frequency of 60 per second (59.94 per second in color systems). Therefore, the integrated output voltage across the capacitor of the RC circuit of Fig. 317 can be coupled to the vertical scanning generator to provide vertical synchronization. The six equalizing pulses immediately preceding and following the

vertical pulse improve the accuracy of the vertical synchronization for better interlacing. The equalizing pulses that precede the vertical pulses make the average value of applied voltage more nearly the same for even and odd fields, so that the integrated voltage across the capacitor adjusts to practically equal values for the two fields before the vertical pulse begins. The equalizing pulses that follow the vertical pulse minimize any difference in the trailing edge of the vertical synchronizing signal for even and odd fields.

HORIZONTAL-DEFLECTION CIRCUITS

Fig. 318 shows the functional relationship among the various circuit elements of a horizontal-deflection circuit that uses a power transistor to generate the sawtooth of current through the deflection yoke and to develop the beam accelerating voltage for the picture tube. The high-voltage transformer shown across the output stage may be used as a slight step-up or step-down transformer for the picture-tube high-voltage supply, the yoke, the damper diode, the capacitor, or any combination of these elements.

92CS-26023
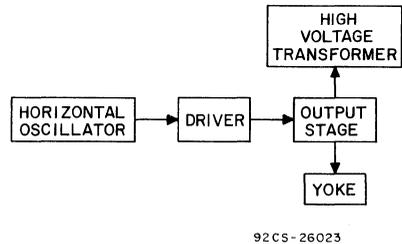
Fig. 318 - Block diagram of a transistor horizontal-deflection system.

In the following paragraphs, the design factors and technical considerations used in the development of a typical horizontal-deflection-system circuit are explained. This system is assumed to provide the deflection energy and high voltage required for a 19-inch, 20-kilovolt, 114-degree monochrome receiver from a power supply having a 12-microsecond retrace time. Basic circuit configurations for practical horizontal-deflection systems for both monochrome and color television receivers are then shown and analyzed.

Voltage Considerations—For an idealized horizontal-deflection circuit, the peak voltage E_{max} across the transistor is given by

$$E_{max} = \left(1.79 + 1.57 \frac{T_t}{T_R}\right) E_{dc}$$

where T_t is the scanning or trace time, T_R is the retrace time, and E_{dc} is the supply voltage. If third-harmonic tuning is employed, the peak voltage is reduced by approximately 20 per cent.

The highest anticipated value of E_{max} is determined by use of the value of E_{dc} obtained at high ac line voltage and at the lowest horizontal-oscillator frequency, i.e., the longest trace time. (For these conditions, of course, the receiver is out of sync.) The tolerances on the inductors and capacitors alter the trace time only slightly and usually may be ignored if a 10-per-cent tolerance is used for the tuning capacitor.

When a capacitor is used in series with the yoke for linearity correction, the peak-to-peak yoke current and the flyback voltage are both increased by about 10 per cent. In a first-order approximation, this effect may be ignored if the system is designed without S-shaping. If shaping is employed, however, the supply voltage must be reduced by 5 to 10 per cent to restore the scan conditions originally observed.

An abnormality that must be considered is high-voltage arcing. Fig. 319 shows the normal

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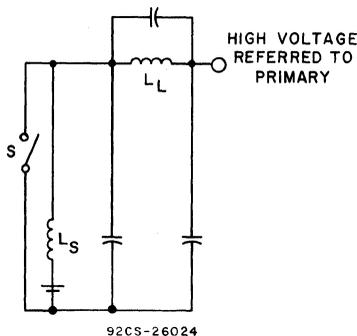
Fig. 319 - Equivalent output circuit for third-harmonic tuning (referred to primary side.)

transistor load for third-harmonic tuning of the flyback transformer in which the leakage inductance, secondary-winding capacitances, and anode stray capacitances are reflected to the primary. In a properly designed system, the leakage inductance is about one-half the shunt inductance (yoke plus flyback primary inductance).

When a high-voltage arc occurs, the secondary is momentarily shorted, placing the leakage inductance in parallel with the shunt inductance. As a result, the peak collector current is increased by a factor of about three, and the retrace time is decreased by a factor of about two (if the transistor is still operating as an ideal switch).

Because the flyback voltage would then be increased by a factor of 2.5, avalanche breakdown occurs at a high current level, second breakdown is initiated, and the transistor is destroyed. Since occasional high-voltage arcing is unavoidable in the picture-tube gun, the output transistor must be protected.

If a diode and capacitor are connected in series and placed across the transistor, the flyback pulse is clamped at a level equal to the normal peak value when a high-voltage arc occurs. When the arcing is sustained long enough for an appreciable increase in the capacitor voltage, the increased drain (caused by the very high peak collector current) opens a fuse in the B-supply, and the transistor is adequately protected. A bleeder resistor is placed across the capacitor to protect against intermittent arcs. This circuit also protects against several other types of high-voltage short circuits.

Another method used to reduce the effect of high-voltage arcing is to make the leakage inductance of the secondary very high compared to the shunt inductance by designing the secondary to resonate at the fundamental frequency (15 kHz). In addition to protection during high-voltage arcs, this method reduces peak collector current (caused by higher primary inductance) and also facilitates manufacture of the flyback transformer.

There are several disadvantages, however. Because the flyback primary current is very high and circulates at all times (as opposed to the case of third-harmonic tuning), very high primary and secondary losses occur. In addition, the magnetic field of the transformer is quite high and causes interference problems in the rest of the receiver. It also becomes difficult to enclose the transformer in a cage without causing an excessive shorted-turn problem because the cage is magnetically coupled.

A third and rather significant disadvantage is the high peak-to-peak secondary voltage developed for a given value of dc high voltage. In third-harmonic tuning, the secondary

voltage waveform exhibits a narrow spike for approximately 10 per cent of the cycle and a low constant voltage for the remainder of the cycle. As a result, the peak-inverse rating on the high-voltage rectifier is approximately 1.1 times the dc high voltage developed. In the "fundamental-tuned" arrangement, the secondary voltage is nearly a sine wave and results in a peak-inverse rating on the high-voltage rectifier approximately twice that of the third-harmonic-tuned system.

Choice of Retrace Time—The choice of a slightly longer retrace time offers the following significant advantages for circuit design:

1. As retrace time is lengthened, the product of peak voltage and peak curent is reduced directly.
2. The peak stored energy, as well as the voltage-current product, is reduced because more primary inductance can be used in the flyback transformer.
3. The retrace losses are reduced with the square of the retrace time.
4. Losses in the yoke and flyback that result from skin effect are reduced.
5. The core losses in the flyback transformer are reduced because of the greater inductance.
6. The supply voltage may be increased because of the lower flyback pulse.
7. The flyback transformer secondary becomes easier to wind.

High-Voltage Power—High voltage is obtained by means of a tertiary winding on the flyback transformer which through auto-transformer action steps up the yoke pulse to a high value. In monochrome receivers, the energy typically extracted is seldom greater than 0.3 millijoule for 5 watts of beam power and results in a typical circuit Q of approximately 60, if other degenerative losses are neglected. When an LC network is damped to a Q of 60, the voltage and current waveshapes for the first π radians show very little change (except for phase relationship) over the infinite-Q condition. Therefore, the losses, which are determined by the voltage and current waveshapes, do not increase when beam current flows; i.e., 5 watts of beam power reflects only an added demand of 5 watts in the power supply.

A further point of interest in transistor deflection circuits is the excellent high-voltage regulation encountered. This improvement is the result of the high efficiency of these circuits, which keeps the extracted energy to a minimum and results in a fairly high circuit Q. As noted, the anode-voltage amplitude does not change much as energy is extracted and thus accounts for good high-voltage regulation.

Deflection Energy Requirement—The peak deflection energy required by the yoke for complete scanning of picture tubes varies directly with the high voltage, the 5/2 power of the deflection angle (approximately), and the neck diameter (where all geometries of the yoke are adjusted in direct proportion). The peak energy required for minimum scanning of a 114-degree picture tube having a $1\frac{1}{8}$-inch neck diameter and an anode voltage of 20 kilovolts is 2.4 millijoules (scan from center to either side).

When full scan is obtained at low line voltage and at an anode voltage that corresponds to low line, the peak stored energy equals ε. When the line voltage is increased, the peak energy increases in proportion to the square of the voltage. If the low line voltage is 105 volts and high line is 135 volts, the increase in energy is a factor of 1.65.

If the receiver is adjusted out of sync by 2 microseconds (or a 480-cycle pullout range), the energy, which is proportional to the square of the trace time in a fixed circuit, increases by a factor of 1.08. If the yoke is shunted by a practical flyback transformer, the inductance is reduced by a factor of approximately 1.3 and, therefore, the peak stored energy in the system is increased by a factor of 1.3. When all three items are considered, the transistor must handle 2.3 times the peak stored energy normally expected.

Transistor Drive Considerations—Transformer drive is usually employed for the output transistor. When this type of drive is used, the collector load may be placed in series with either the collector or the emitter because, in either case, the transformer secondary appears from base to emitter. If the load is in series with the emitter (emitter loading), the collector is directly at the supply-voltage potential. If a positive-supply is used, the transistor case is at chassis potential. The damper diode is constructed with its anode at case potential so that it is also at chassis potential.

This method has a disadvantage in that a high potential is placed between the primary and secondary windings of the driver trans-

former. Because the driver transformer is very tightly coupled, insulation breakdown must be carefully considered.

While the output stage is cut off, the driver stage should be conducting; the transformer secondary can then provide any current demanded. (The current, however, is limited by the leakage inductance.) When the driver stage is cut off, the energy stored in the transformer flows in the secondary in the form of a constant current. If this mode of drive is employed, and if the base-to-emitter voltage of one transistor varies from that of another, the turn-on current still starts at the same value but decays at a different rate. If all charge is removed from the base of the output transistor during turn-off, no more transformer current is required and the transistor stays at a reverse-bias mode.

No impedance should be placed in the base. Transistor interchangeability is thus improved because the voltage level remains low enough to prevent breakdown of the base-emitter function during the turn-off period. The primary and secondary windings of the driver transformer must be very tightly coupled to obtain a large spike of current during the turn-off period (for a fast turn-off time).

The circuit shown in Fig. 320 is used to develop the all-important waveshaping. The

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Fig. 320 - Waveforming circuit.

560-ohm resistor in combination with the 0.05-microfarad capacitor increases the amplitude and rise time of the turn-off base current for the first few microseconds. The D1201F diode, together with the 2700-ohm resistor and 10-microfarad capacitor, serves as a clamp circuit which assures that the output transistor is always reverse-biased during the entire turn-off period, even in the presence of high I_{CBO} at several hundred volts and elevated

temperatures. With this circuit, the 560-ohm, 0.05-microfarad combination can be optimized for the best turn-off time without regard for the remainder of the off signal.

The turn-off pulse developed by this circuit is 3 amperes for approximately 2 microseconds, followed by a constant voltage of approximately ½ volt for 18 microseconds. The on-pulse then initiates at 650 milliamperes and, 45 microseconds later, decreases to 500 milliamperes.

Deflection Circuit for Monochrome Receiver—The following paragraphs describe a practical horizontal-deflection system for a 19-inch black-and-white (monochrome) television receiver. The deflection system operates from a regulated dc supply of 100 volts.

The power-supply voltage of 100 volts is decoupled to 85 volts for raster regulation with brightness. A retrace time of 14 microseconds is selected to present the maximum usable picture, although a value of 17 microseconds could have been used with no sacrifice in performance as compared to present-day receivers.

The picture tube used, the 19DQP4, has minimum usable screen dimensions of 15⅛ inches horizontally and 12 inches vertically. These dimensions establish the front mask size for the cabinet and fix the aspect ratio of 1.26. The diagonal deflection angle of the 19DQP4 is 114 degrees, and the neck diameter is a nominal 1⅛ inches. The zero-beam accelerating potential is 20 kilovolts. The horizontal circuit should be capable of providing an average beam current of 400 microamperes with virtually no change in raster height or width at any brightness setting between zero and full current. An over-scan of 4 per cent is desired.

Energy requirements for horizontal deflection show that the peak stored energy in the yoke must be 2.4 millijoules to fulfill the requirements for the 19DQP4. If a trace time of 49.5 microseconds and a power-supply voltage of 85 volts are used, and if it is assumed that the use of "S" shaping (by use of a capacitor in series with the yoke) has the effect of increasing the scan by 5 to 10 per cent, the yoke inductance must be 1 millihenry and the peak-to-peak yoke current must be 4.4 amperes.

Driver and output circuit—The horizontal-drive-and-output circuit for the receiver is shown in Fig. 321. The output circuit (Q_5) is

Fig. 321 - Horizontal driver and output circuit for a black-and-white television receiver.

basically a self-oscillator which requires the 27,000-ohm resistor to initiate oscillation. Drive current is obtained through the 33-ohm resistor in parallel with the picture-tube heater and through diode D_5, and is applied from the feedback winding of the transformer T_1 through the 50-microfarad capacitor in parallel with the 10-ohm resistor to the base of the output transistor Q_5. If this drive circuit is correctly designed, transistor Q_5 does not come out of saturation during normal operation. When retrace is to be initiated, the driver transistor Q_6 is driven heavily into saturation. The drive current is then shunted to ground, and the base of transistor Q_5 is simultaneously reverse-biased by means of the charge stored on the 50-microfarad capacitor. If the resistor shunting this capacitor is large compared to 2 ohms, most of the drive current flows through the capacitor. When transistor Q_6 is saturated, therefore, a capacitor current of opposite polarity results through Q_6 and D_1. As a result, the turn-off drive to transistor Q_5 is always a reverse-bias voltage equal to the forward drop across diode D_1. If the value of the parallel resistor is made extremely large, the circuit may not start.

When the output transistor Q_5 is turned off, the collector voltage comes out of saturation and goes through the normal flyback pulse. During this time, the feedback drive (already shunted to ground) decreases and, as the collector voltage passes the supply voltage, a

heavy reverse drive current results. However, the driver diode D_5 blocks this reverse current flow. D_5 also permits the starting current (through the 27,000-ohm resistor) to flow through the base of Q_5.

The damper current flows through the collector-base diode of Q_5 in series with D_4 to ground. Diode D_4 is a silicon type that has a low forward drop at 2 amperes and a minimum breakdown requirement of only 1 volt. It must be capable of dissipating 300 milliwatts. D_4 is called a damper diode, even though it only partially fulfills this function. The 50-microfarad coupling capacitor must have a low series resistance to obtain proper turn-off.

The 100-volt supply voltage is reduced 15 per cent at zero beam current by means of the 75-ohm decoupling resistor. When the beam current is increased to 400 microamperes, the demand for extra power of 7 or 8 watts causes the decoupled voltage to drop. As a result, the high voltage and the scanning current decrease linearly with the decoupled voltage. The high voltage also decreases because of the lack of perfect high-voltage regulation. If the circuit is designed correctly, the high voltage decreases with the square of decoupled voltage so that the scanning-energy requirement approximately tracks the scanning energy provided. This decoupled voltage is also fed back to the vertical circuit in the size-determining portion of the circuit so that the vertical scan energy also tracks the high voltage as a function of

picture-tube average brightness setting.

A separate winding on the flyback transformer T_1 provides gating for the agc circuit. A signal taken from the driver diode D_5 provides a timing reference for the horizontal phase circuit (afc). A positive voltage of approximately 500 volts is available from the clamp circuit provided by diode D_7 to supply bias to grid No. 2 or grid No. 4 of the picture tube. (The current drain should be kept below 1 milliampere.)

Picture-tube heater power is also derived from the horizontal-driver circuit. When the receiver is first turned on, the base drive current to transistor Q_5 is larger than normal because of the thermally non-linear characteristic of the heater. This method of providing heater power should prove to be satisfactory for long picture-tube life. However, excessive heater-to-cathode capacitance may cause a video modulation in the form of a vertical line similar to a drive line in tube deflection. No such problem has been experienced with the approach shown. A more conservative control of heater power may be obtained by means of a separate winding or by incorporation of the heater with the agc winding.

The video-blanking circuit must be gated from the flyback transformer T_1. A 100,000-ohm resistor is fed from the collector of the output transistor Q_5 for this function. This resistor provides blanking whenever the collector voltage is more positive than 25 volts.

The picture-tube heater has a dc voltage across it, together with a large ac voltage. After adequate decoupling, this dc voltage provides a convenient source of negative potential to power the agc and sync-separator circuits.

Various forms of arcing protection are provided in the horizontal output circuit.

A voltage-clamp circuit is provided by the clamp diode D_7 in conjunction with the 8-microfarad capacitor. Sufficient current drain must be provided across the capacitor to discharge it between arcs. The capacitor must be large enough to absorb most of the energy stored by the picture-tube capacitance. The purpose of this clamp circuit is to assure that the transistor does not go into voltage breakdown during high-voltage arcs.

The 75-ohm decoupling resistor provides raster regulation, as mentioned previously, and also limits the maximum power that may be delivered to the entire horizontal-scanning

circuit to 30 watts.

If the output transistor Q_5 is pulled out of saturation at a high collector-current level as a result of high-voltage arcing, the feedback drive circuit turns off Q_5 and thus controls the transistor load line. The transistor turns off fairly fast under this condition because it is in an unsaturated state. If the driver transistor Q_6 is turned on or off when Q_5 is reverse-biased, no change in state occurs because the drive is basically self-oscillating and transistor Q_6 functions merely as a gate. If drive is available, Q_6 may exclude it. If drive is being applied, Q_6 may turn it off. However, Q_6 may not provide drive if Q_5 is not saturated.

Although drive is available at the beginning of trace time, it should be excluded by Q_6 until about 5 microseconds prior to normal need. As a result, Q_6 should receive a drive pulse that saturates it for approximately 30 microseconds, and turns it off for the remaining 34 microseconds.

The clamp diode D_7 must not fail. If it does, destruction of Q_6 is almost assured.

Horizontal oscillator—Fig. 322 shows a simplified diagram of a multivibrator-type of horizontal-oscillator circuit. It should be noted that a gated dc feedback signal is provided from the power supply. If the 100-volt supply becomes excessively high as a result of a fault, the horizontal-oscillator frequency is raised to such a point that the flyback voltage remains within specifications.

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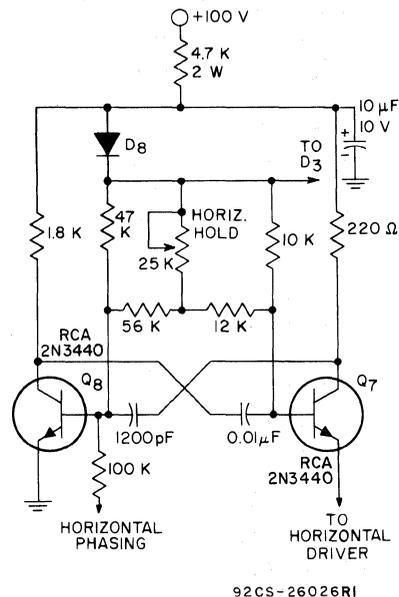
Fig. 322 - Horizontal oscillator circuit.

Horizontal phasing (afc)—The horizontal phasing used is novel. Gating is obtained from a 1-milliampere sync pulse that is only 2 microseconds wide (and can be much narrower if desired). Nearly any desired average control current up to several milliamperes can be provided. When the picture is correctly phased, the circuit is open to receive a sync pulse for only 4 microseconds, and thus is relatively immune to noise. Because the circuit functions on the leading edge of the sync pulse, rather than on the entire area of the differentiated pulse, the effects of the vertical equalizing pulses and the serrations in the vertical pulse are greatly minimized. As a result, the top of the picture exhibits proper synchronization at essentially all settings of the hold control (as is not the case with normal afc).

The horizontal-phasing circuit is shown in Fig. 323. A control current of only 20


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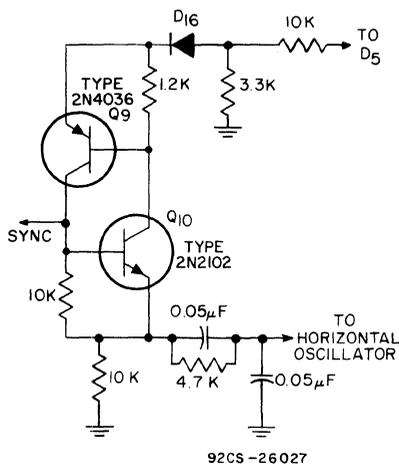
Fig. 323 - Horizontal-phasing (afc) circuit.

microamperes is required for the low-level oscillator. Transistors Q_9 and Q_{10} are connected in a latching configuration that resembles a thyristor. (A thyristor could be used if it were fast enough and sensitive enough.) A replica of the flyback pulse is applied to the emitter of transistor Q_9 from diode D_5 through the voltage divider consisting of the 10,000-ohm and 3300-ohm resistors. During trace time, this voltage is slightly negative, and any signal appearing on the base of transistor Q_{10} is ineffective. When the flyback voltage appears across transistor Q_9, however, the gate is open to receive a sync pulse. When the pulse fires transistor Q_{10}, the combination of transistors

Q_9 and Q_{10} becomes regenerative; the transistors then become heavily saturated and pass any amount of current the voltage divider will permit. Transistors Q_9 and Q_{10} remain in saturation until the voltage reverses and resets the latch. Control current of the opposite polarity may be obtained from the emitter of transistor Q_9, if desired. Diode D_{16} serves to block reverse current.

Deflection Circuit for Color Receiver—Fig. 324 shows a schematic of a transistorized horizontal-deflection circuit for a color TV receiver. The horizontal output transistor, Q_4 is a high-voltage silicon transistor. The normal collector-to-emitter pulse voltage across Q_4 includes an ample safety factor that allows for any increased pulse that may result from out-of-sync operation, line surges, and other abnormal conditions.

A unique feature of the horizontal-deflection circuit is the low-voltage supply of approximately 23 volts that is derived from it. This feature makes it possible to eliminate the power transformer in the power supply. The low-voltage power is used to operate all but the high-voltage receiver stages, such as the video-output stage, the audio-output stage, and the horizontal oscillator and driver. The vertical oscillator is supplied from the same point which supplies the horizontal output in such a way that the actual voltage is a function of beam current; this connection compensates for the tendency for picture height to change with brightness settings.

The transistorized deflection circuit achieves commercially acceptable high-voltage regulation without the use of the high-voltage shunt regulator used with tube-type deflection circuits. With a flyback transformer of normal design and a low-voltage power supply with about 3-per-cent regulation, high-voltage regulation from zero beam to full load of 750 microamperes is about 3 kilovolts, and is accompanied by a considerable increase in picture width. Improvement of this behavior with brightness changes is achieved by utilizing the accompanying changes of direct current to the deflection circuit in two ways. First, the air gap of the transformer is reduced to permit core saturation to decrease the system inductance as the high-voltage load is increased. When this method is used, regulation is improved to about half that of the normal transformers with no circuit instabilities, but picture-width change is still greater than
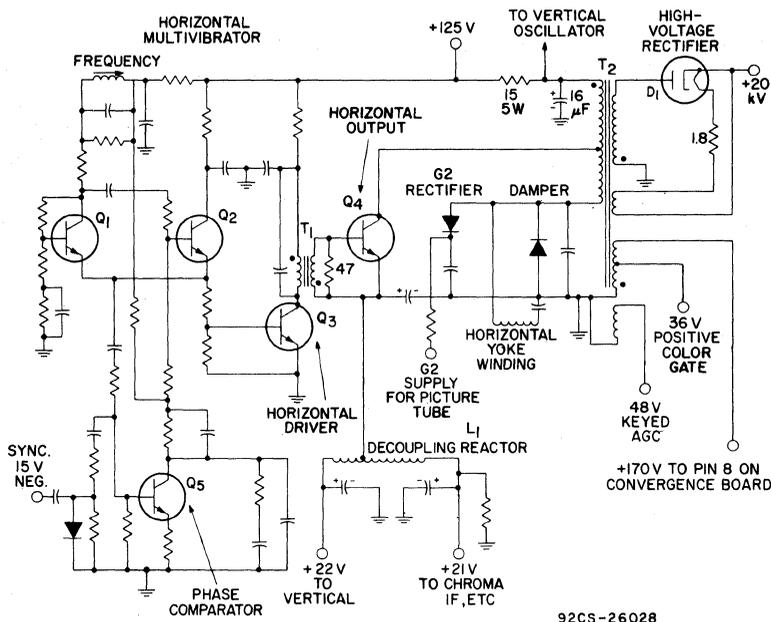
Fig. 324 - Horizontal-deflection system for a color television receiver.

desired. Second, series resistance is added to the B supply to decrease power input at full load and thereby reduce the change in picture width (at some sacrifice in high-voltage regulation). The net result of both changes is a regulation of about 2.8 kilovolts for the high voltage, with very little variation in picture size.

A secondary benefit of the inherently good regulation of the transistor deflection system is a reduction in the size of the flyback transformer. The size reduction is accomplished by a reduction in the area of the "window" in the flyback core.

Auxiliary Deflection-System Functions

Although the major function of the horizontal-deflection system is to deflect the electron beam horizontally across the face of the picture tube, it normally also provides a number of auxiliary functions. These functions may include items such as follows:

1. Generation of the high voltage for the picture tube
2. Focus supply voltage for the picture tube
3. High-voltage regulation
4. Scan-linearity correction
5. Convergence waveforms
6. Retrace blanking

7. Gating pulse for automatic gain control (agc)
8. Timing reference for automatic frequency control (afc)
9. Bias voltage for grid No. 2 of the picture tube
10. Low-voltage supplies for the other sections of the receiver

The voltages for these functions are normally obtained by connection of a transformer in shunt with the yoke. This transformer is called the high-voltage or "flyback" transformer. This transformer is always a **step-up transformer** for the high-voltage rectifier and is usually a **step-down transformer** for the various other voltages obtained from it. In addition, it may be used as a slight step-up or step-down transformer for the yoke, the damper diode, the capacitor, or any combination of these components. Fig. 324 shows a deflection circuit that includes a high-voltage transformer together with a number of auxiliary functions.

VERTICAL DEFLECTION CIRCUITS

The vertical-deflection circuit in a television receiver is essentially a class A audio amplifier with a complex load line, severe low-frequency requirements (much lower than 60 Hz), and a need for controlled linearity. The equivalent low-frequency response for a 10-per-cent deviation from linearity is 1 Hz. A simple
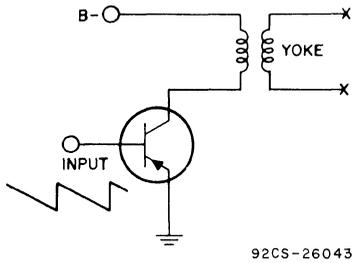
Fig. 325 - Simple vertical-deflection circuit.

circuit configuration is shown in Fig. 325.

The required performance can be obtained in a vertical-deflection circuit in any of three ways. The amplifier may be designed to provide a flat response down to 1 Hz. This design, however, requires an extremely large output transformer and immense capacitors. Another arrangement is to design the amplifier for fairly good low-frequency response and predistort the generated signal.

The third method is to provide extra gain so that feedback techniques can be used to provide linearity. If loop feedback of 20 or 30 dB is used, transistor gain variations and non-linearities become fairly insignificant. The feedback automatically provides the necessary "predistortion" to correct low-frequency limitations. In addition, the coupling of miscellaneous signals (such as power-supply hum or horizontal-deflection signals) in the amplifying loop is suppressed.

The inductance of the output transformer must be fairly low for maximum efficiency. When a circuit is designed for maximum efficiency, the transistor dissipation must be at least three times the yoke power. When interchangeability, line-voltage variations, and bias instability are considered, the dissipation may reach high levels (e.g., 14 watts in a 25-inch color receiver); as a result, expensive bias techniques and extruded-aluminum heat sinks must be used.

Use of a toroid yoke having an L/R time constant of 3.2 milliseconds reduces the maximum dissipation to 3 or 4 watts and allows the plated steel chassis to be used as the heat sink for the transistor. The output transformer may also be reduced in size.

The higher Q of the toroid yoke normally results in a long retrace time or a very high flyback voltage.

Basic Design Approach

In some commercial television receivers, the Miller-integrator concept is employed in the generation of the linear ramp of current required in the vertical-deflection yoke. Fig. 326 shows the basic configuration of a Miller-
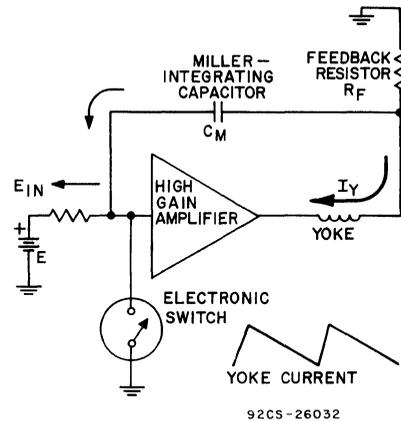

Fig. 326 - Basic Miller Sweep Circuit.

integrator type of vertical-deflection circuit. In this circuit, a high-gain amplification system is used to develop the drive current for the yoke winding, and the integrating capacitor is connected in shunt with the yoke and the amplifier system. In effect, the Miller circuit multiplies the capacitor charging current by a factor equal to the gain of the amplifier without feedback. This technique results in an extremely linear output current waveform. In addition, variations in supply voltage, amplifier gain, and other factors that drastically affect the output of conventional vertical-deflection circuits have but slight adverse effects in the Miller circuit because of the large degenerative feedback.

At the beginning of the vertical-trace interval, the integrating capacitor C_M is charged from a voltage source E. The resulting voltage across the capacitor causes the amplifier to supply current to the yoke winding and to the feedback resistor R_F, which is directly coupled to the integrating capacitor. The feedback action of the integrating capacitor tends to maintain a constant input to the amplifier so that the voltage across the capacitor builds up (integrates) at a constant rate. Because the voltage across the feedback resistor, which is essentially the same as the voltage across the integrating capacitor, is directly proportional to the yoke current, the
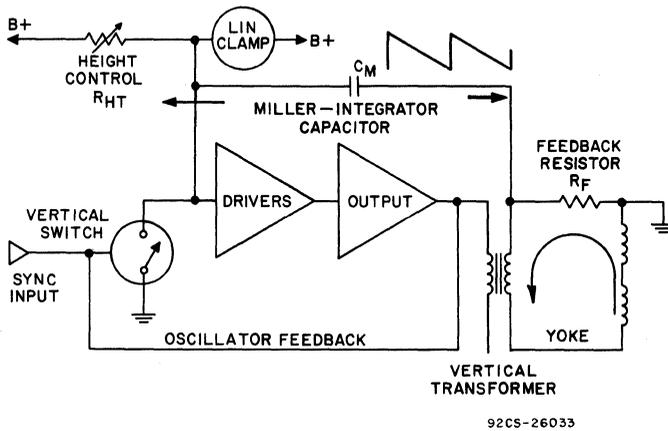
Fig. 327 - Basic configuration of a Miller-integrator vertical-deflection system that uses a conventional transformer-coupled output stage.

yoke current increases at a constant rate, and a linear scan results. The sweep rate is determined by an electronic switch which discharges the integrating capacitor at the end of each scan period.

The amplifiers used in the vertical-deflection system are similar to those used in any high-gain audio-amplifier system. Either conventional transformer-coupled types or transformerless true-complementary-symmetry or quasi-complementary-symmetry types may be used. The following paragraphs describe the use of different types of output amplifiers and their associated circuitry in vertical-system applications.

Vertical-Deflection Circuit that Uses a Conventional Output Stage

Fig. 327 shows the basic functional relationship among the various stages of a Miller-integrator vertical-deflection circuit used in some commercial color-television receivers. The vertical-switch circuit controls the trace and retrace times and, therefore, the over-all operating frequency of the circuit. The switching action of the vertical switch is made self-sustaining by use of positive feedback from the output stage. Vertical synchronizing pulses applied to the switch from the sync separator determine the exact instant at which the switch is triggered on and, in this way, synchronize the switching action with the transmitted scanning interval. The Miller high-gain amplification system includes predriver and driver stages in addition to a conventional transformer-coupled output

power-amplifier stage. The Miller-integrator capacitor is connected between the yoke winding and the input to the predriver so that is shunts the gain stages. The linearity-clamp circuit provides the initial charging current for this capacitor.

Vertical Switch—The vertical switch discharges the Miller-integrator capacitor at the end of the vertical scanning interval and, in this way, causes beam retrace and prepares the circuit for a subsequent scanning interval. Fig. 328 shows the schematic diagram and operating waveforms for the vertical-switch circuit. The operation of the circuit is made self-sustaining by two feedback signals.

One feedback signal is applied to the base of the vertical-switch transistor from a secondary winding on the vertical-output transformer through resistors R_3 and R_4. This feedback signal is referred to as the triggering or turn-on pulse. The vertical synchronizing pulses from the sync separator are integrated by resistors R_1 and R_2 and capacitor C_2 and added to the triggering pulse.

Another feedback signal from a different secondary winding on the vertical-output transformer is applied to the base of the switch transistor through the vertical-hold potentiometer R_H. The addition of this waveform to the turn-on waveform causes the voltage at the base of the switch transistor to pass very quickly through the transistor turn-on voltage. As a result, the turn-on action of the vertical switch is very stable and relatively immune to noise voltages. The vertical-hold potentiometer provides some control over the shape of the
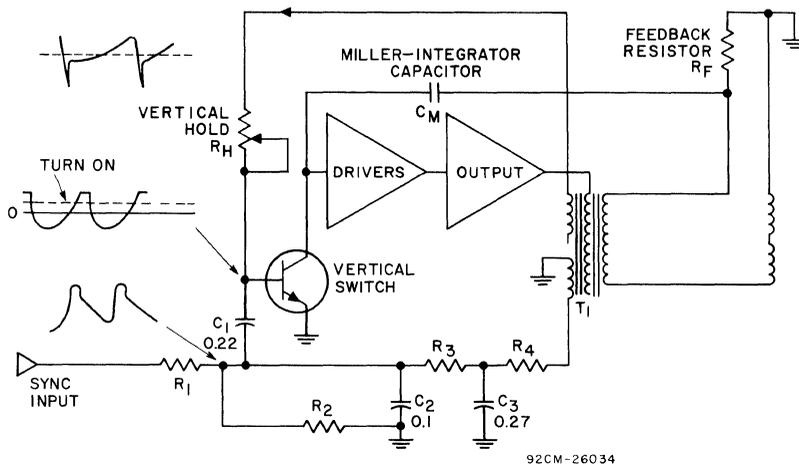
Fig. 328 - Vertical-switch circuit.

latter feedback waveform and, therefore, offers limited control over the exact point at which the switch turns on.

Driver Stages—Two common-emitter stages (predriver and driver) provide the amplification required to increase the amplitude of the vertical-switch output sufficiently to drive the vertical-output stage. Fig. 329 shows a simplified circuit diagram of the driver stage.

The vertical predriver employs an n-p-n transistor Q_3 that is directly coupled to the p-n-p transistor Q_2 used in the driver stage. The emitter-supply voltage for the driver is obtained from the voltage-divider network formed by resistors R_5 and R_6. The collector load of the driver consists of the parallel combination of the 680-ohm resistor R_4 and

the base-emitter junction of the output-stage transistor Q_1. The service switch S_1 included in the emitter circuit of the driver can be used to cut off the vertical scanning during set-up adjustments of the picture tube if desired. When this switch is closed, the emitter of the driver is shorted to ground, and no vertical-deflection signals are developed.

The predriver input waveform is supplied by the charging action of the Miller-integrator capacitor C_M, which is charged through the height-control potentiometer R_{HT}. The height-control supply voltage is made relatively immune to temperature-caused variations by the thermistor R_T. This supply also receives some dynamic regulation from a voltage supplied from the horizontal-deflection system.
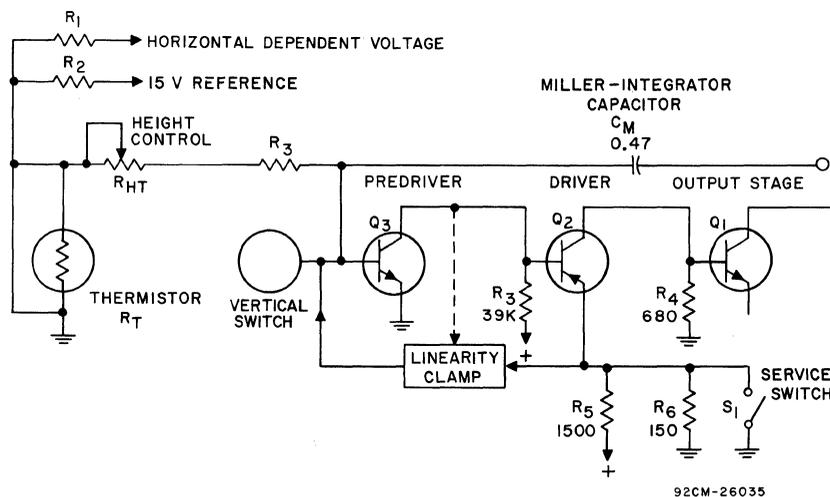

*Fig. 329 - Vertical predriver and driver stages.*
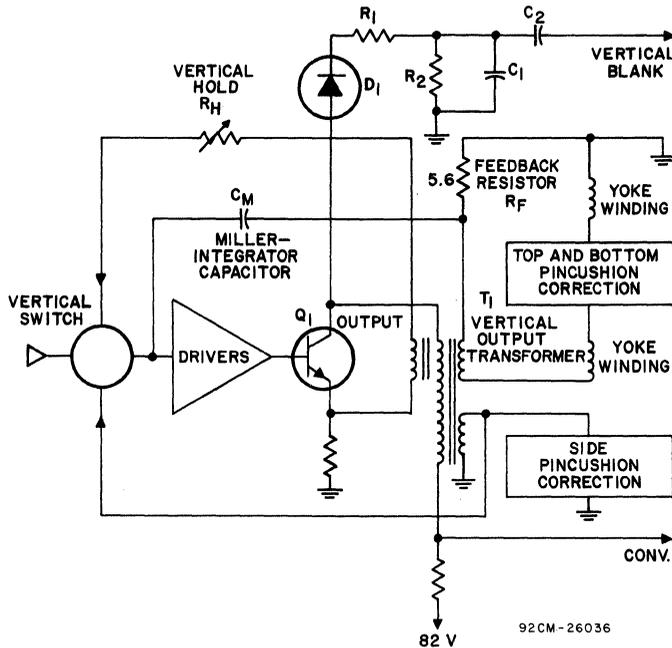
Fig. 330 - Transformer-coupled vertical output circuit.

The addition of this regulating voltage helps to maintain a constant vertical height with respect to horizontal-scan and high-voltage variations.

Vertical Output Stage—Fig. 330 shows the circuit details for the output stage of the vertical system. This stage, which is directly driven by the driver circuit, uses a transistor operated in a common-emitter amplifier configuration to develop the power necessary to produce the required vertical deflection of the picture-tube beams. The collector-load circuit consists of the vertical-output transformer T_1 and the vertical convergence circuitry. The secondary of the vertical-output transformer is loaded by the vertical yoke windings, two feedback paths, and the pincushion-correction circuitry. The Miller-integrator capacitor C_M is coupled to the 5.6-ohm feedback resistor R_F, which is connected in series with the output-transformer secondary and the windings of the vertical-deflection yoke. Two feedback waveforms are provided from the output stage (from separate secondary windings on the output transformer) to the vertical switch to assure stable, self-sustaining switch operation.

The diode D_1 and the filter network formed by resistor R_2 and capacitor C_1 form a protective clamp circuit for the output tran-

sistor. Positive-going retrace pulses cause the diode D_1 to conduct and capacitor C_1 charges rapidly through the short-time-constant path provided by diode D_1 and resistor R_2. After the retrace pulse is removed, the capacitor attempts to discharge through the resistor R_2. Because of the long-time-constant path provided by this resistor, the capacitor is only allowed to discharge an amount sufficient to assure a voltage differential across the diode when the retrace pulses occur. This action effectively clamps the collector output of transistor Q_1 to the voltage across capacitor C_1. The pulses that appear across this capacitor during the conduction of the diode are coupled by capacitor C_2 to the television-receiver video-amplifier circuit for use in vertical-retrace blanking.

Linearity Clamp—A circuit referred to as the linearity clamp is included in the vertical-deflection system to assure that sufficient initial-scan charging current is provided for the Miller-integrator capacitor. Fig. 331 illustrates the action of this circuit.

When the Miller-integrator capacitor C_M is discharged by the vertical switch at the end of a vertical-scan interval, the capacitor discharges into the base circuit of the predriver stage, and the predriver transistor is cut off. The positive voltage that then appears at the
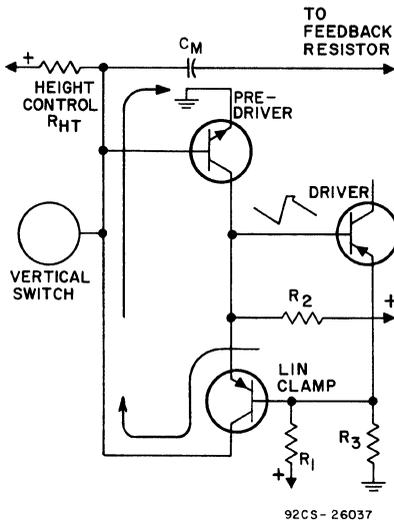
Fig. 331 - Linearity clamp.

collector of the predriver transistor forward-biases the p-n-p linearity-clamp transistor, and current flows through this transistor, resistor R_2, and the vertical switch. After approximately 700 microseconds, the vertical switch turns off, and the current through the linearity clamp is used to provide rapid initial charging of the Miller-integrator capacitor C_M. As the initial charge quickly builds up on the capacitor, the predriver and driver stages start to conduct, and the base-emitter junction of the linearity-clamp transistor is reverse-biased by the voltage drop across the base-emitter junction of the driver transistor. This action cuts off the linearity-clamp circuit and initiates another vertical-scan interval. The Miller-integrator capacitor continues to charge through the height-control potentiometer R_{HT} for the duration of the scan interval.

Vertical-Deflection Circuit Using a Complementary-Symmetry Output Stage

The introduction of complementary pairs of power transistors has led to the development of class B transformerless output stages that are both economical and efficient. In vertical-output applications, such circuits may be capacitively coupled to the yoke because of this arrangement, the output transformer, together with the problems of non-linearity, low-frequency phase shift, and excessive retrace pulse amplitudes associated with the transformer, can be eliminated. Regardless of the type of output stage used, the generation

of a linear sawtooth by use of the Miller-integrator circuit has become widespread.

Fig. 332 shows a block diagram of a vertical-deflection system of this type that uses a true-complementary-symmetry output stage. The vertical switch controls the free-running frequency of the vertical system. The high-gain amplifier consists of a direct-coupled predriver and driver, in addition to the true-complementary-symmetry output stage. The output stage is capacitively coupled to the convergence circuitry and the vertical-deflection yoke.
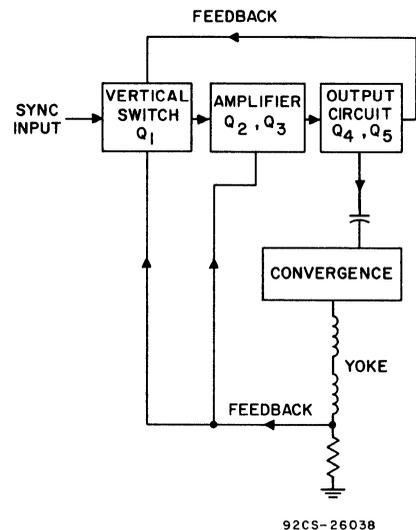

Fig. 332 - Block diagram of a vertical-deflection system that uses a true-complementary-symmetry output stage.

Vertical-Switch and Predriver Circuit—Fig. 333 shows the circuit configuration of the predriver circuit and its interconnection with the vertical-switch circuit. An increase in the positive voltage at the junction of resistors R_{12} and R_{13} will increase the raster height because the major source of the voltage to R_{13} is obtained from the +15-volt regulated supply through resistors R_{11} and R_{12}. As the resistance of R_{12} is decreased, raster height increases. If the set-up switch S_1 is closed to the service position, the supply to R_{13} is diminished practically to zero, and the raster collapses.

Because the output-stage transistor Q_5 is cut off while the top half of the raster is scanned, the voltage at the collector of this transistor is zero until vertical scan reaches the
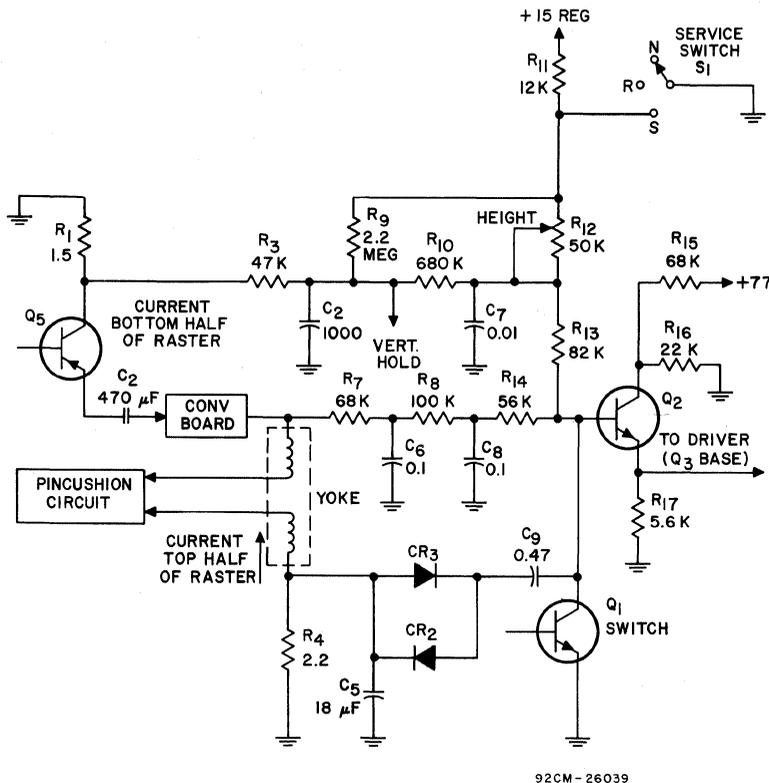
*Fig. 333 - The vertical predriver with its inputs.*

center. During the bottom half of scan, the collector current of output transistor Q_6 increases linearly, so that the voltage fed back to R_{13} tends to "stretch" the lower part of the raster, to overcome some tendency towards bottom compression. Feedback to the vertical-switch transistor also is derived from resistor R_1.

The remaining input to resistor R_{13} is obtained from the horizontal system. As high-voltage return current to the brightness limiter increases or decreases, the voltage at the junction of R_5 and R_6 also varies. An increase in picture-tube current, therefore, reduces slightly the voltage to the height control and causes a slight decrease in vertical deflection. This action causes scanning height to track scanning width.

A feedback signal is fed to capacitor C_9 from the junction of the system feedback resistor R_4 and the yoke. If the effect of capacitor C_5 is ignored, the voltage at this point reaches its maximum positive value at the beginning of scan, passes through zero, and reaches its maximum negative value just before vertical retrace. Therefore, the feedback

to the predriver transistor Q_2 is degenerative, because voltage at the base of Q_2 tends to rise throughout the scanning interval. Capacitor C_5 is used to filter out any horizontal-deflection voltage which may be present.

The transistor vertical-switch circuit shown in Fig. 334 performs three functions. It controls the free-running frequency of the vertical-deflection system, allows synchronization with the received signal, and determines the duration of vertical retrace. The overall vertical system may be considered as a free-running oscillator. The base of switch transistor Q_1 is returned to the supply voltage (height-control B+) through resistor R_7, the hold control, and a 680-kilohm resistor R_8. If no sync pulses are present at the moment after the end of retrace, capacitor C_6 begins to charge, and the base of Q_1 begins to swing positive. When Q_1 begins conducting (about 17 milliseconds later), predriver and driver transistors Q_2 and Q_3 shown in Figs. 333 and 335 respectively, conduct less, and the output transistor Q_4 which was cut off during the lower half of vertical scan, resumes conduction. Because the voltage across the yoke inductance leads
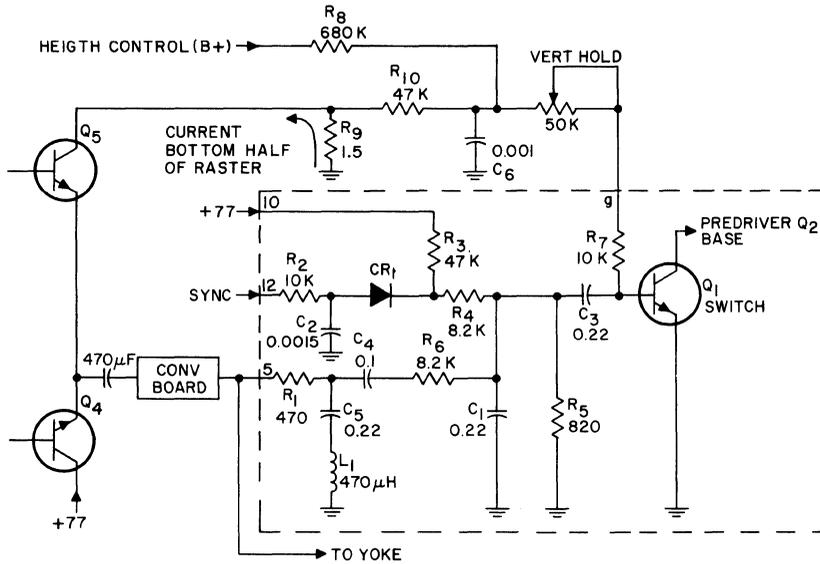
Fig. 334 - Vertical-switch circuit.
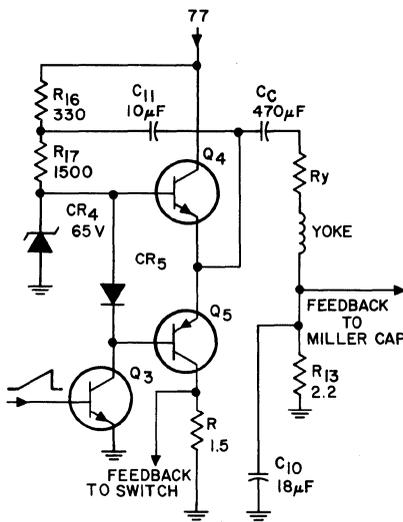
Fig. 335 - Vertical driver, output, and simplified yoke circuit.

the current through it, a sharp positive pulse appears at the input to resistor R_1, and this pulse, coupled to the base of Q_1, drives Q_1 into saturation. This transition of Q_1 from cutoff to saturation is very rapid.

Capacitor C_5 and inductor L_1, connected from the junction of resistor R_1 and capacitor C_4 to ground, are series resonant at the horizontal-scan frequency, and shunt to ground any 15.734-kHz energy which may be present. The presence of horizontal ripple at the vertical switch tends to synchronize the vertical scan with the horizontal scan and causes a degradation of interlace. Resistor R_6 and capacitor C_1 shape the feedback pulse so that the transition of Q_1 from cutoff to saturation is as rapid as possible.

When Q_1 saturates, Q_4 reaches maximum conduction, and the yoke current rises to maximum in the direction which produces maximum upward deflection. During retrace, the base current of transistor Q_1 charges capacitor C negatively. The duration of the scanning is determined by the length of time required for the base of Q_1 to become forward-biased once more.

A second feedback circuit improves the frequency stability of the oscillator circuit. During the top half of scan, output transistor Q_5 is cut off, and the voltage at the junction of resistors R_9 and R_{10} is essentially zero. Therefore, the voltage rise at the base of switch transistor Q_1 is exponential. But, as scan nears the bottom of the raster, transistor Q_4 conducts, and causes a positive voltage to be developed across resistor R_9. This voltage sharpens the voltage rise at the base of Q_1, so that its transition from cutoff to saturation is more rapid. Similarly, the sharp drop in voltage across R_9 (from maximum to zero during the first half of retrace) enhances the cutoff characteristics of the Q_1 circuit.

The composite sync signal is introduced into the vertical system at terminal 12. Resistor R_2 and capacitor C_2 integrate the input so that the horizontal sync pulses are reduced in amplitude to about 8 volts and the vertical pulses about twice this amplitude. Since diode CR_1 has about 12 volts of positive bias on its cathode, only the vertical sync pulse can pass to the switch transistor. If the free-running frequency of the vertical system is slightly less than the vertical-sync rate, Q_1 is at the threshold of conduction when each sync pulse arrives, so that the vertical system is synchronized at the vertical-sync pulse rate.

Vertical Driver and Output Stage—Fig. 335 shows the schematic diagram of the vertical-system driver and of the output stage with the yoke circuit simplified. The circuit configuration is very similar to that of a high-quality audio power amplifier. The yoke itself is analogous to the speaker voice coil, C_C is the coupling capacitor, and R_y is the equivalent of the total resistance of the yoke and convergence circuit. The value of capacitor C_C is selected to provide maximum energy transfer at the vertical scanning frequency. Feedback to the Miller capacitor is developed across resistor R_{13}, and capacitor C_{10} is a filter.

During retrace, transistor Q_3 is cut off, and its collector voltage rises towards the supply voltage; however, the 65-volt zener diode CR_4 limits the maximum base bias of transistor Q_4 and, in this way, limits the yoke retrace current. During the scanning interval, the bases of transistors Q_4 and Q_5 are driven progressively less positive at a linear rate. Conduction is through Q_4 during most of the retrace time and as scan passes from the top of the raster to center. The voltage across capacitor C_C at vertical scan center has reached maxim   (90° out of phase with the current),

and during the lower half of scan, capacitor C_C discharges back through the yoke and transistor Q_4. This current increases at a linear rate, because the forward bias on the base of transistor Q_4 is increasing at a linear rate.

The diode connected between the bases of transistors Q_4 and Q_5 improves the switching characteristics of the transistors at mid-scan. Q_5 has zero bias as long as Q_4 is conducting. Therefore, only slight voltage swings are necessary to cut off Q_4 and turn on Q_5 at the center of the raster. If the diode were shorted or bypassed, reverse bias would exist between base and emitter of Q_5 while Q_4 was conducting, and consequently there would be appreciably more disturbance in the circuit during transition time.

Vertical-Deflection Circuit Using a Quasi-Complementary-Symmetry Output Stage

A disadvantage of the true-complementary-symmetry vertical-output circuit is the higher cost of p-n-p power transistors in comparison to n-p-n power transistors.

Fig. 336 shows the complete circuit diagram for a vertical-deflection system that uses a quasi-complementary-symmetry output stage to drive a low-impedance toroidal yoke (L=950 microhenries, R=1.5 ohms). This system is basically the same as the true-complementary-symmetry output stage, with the exception of some minor modifications necessary to supply the higher deflection current required for the toroidal yoke.

Transistors Q_3 and Q_5 are functionally equivalent to the n-p-n output device in the true-complementary-symmetry circuit; transistors Q_4 and Q_6 are equivalent to the p-n-p device.
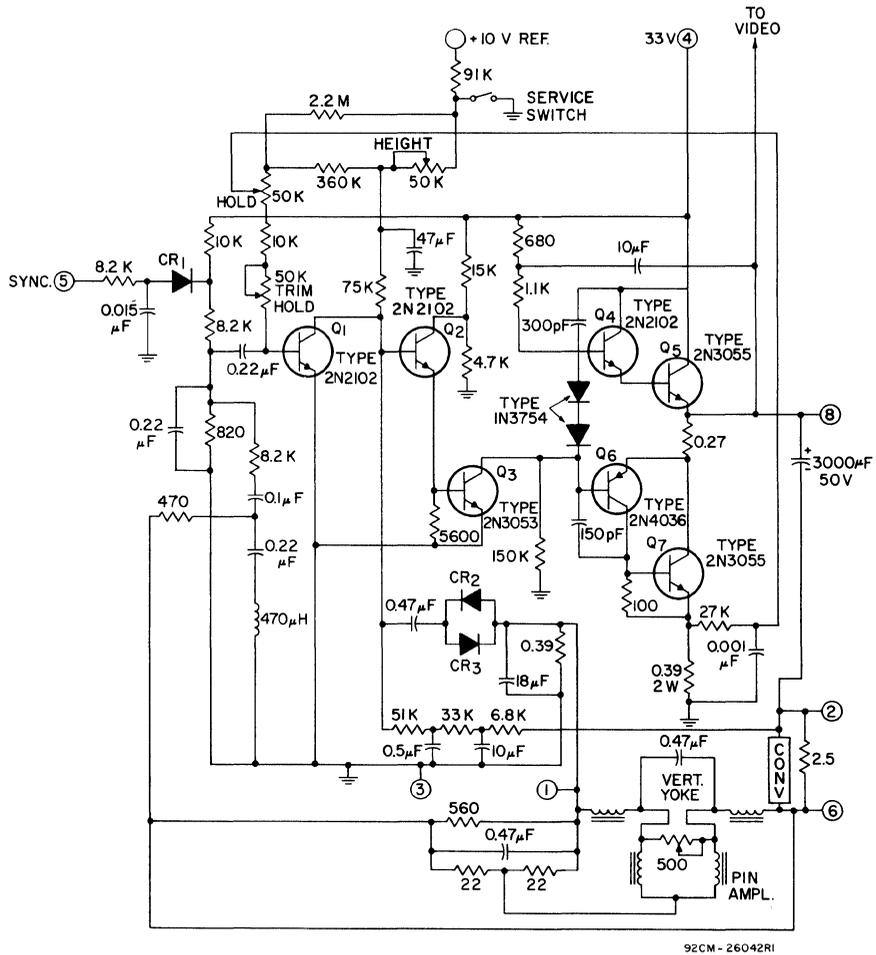
Fig. 336 - Complete transistor vertical-deflection system that uses a quasi-comple-mentary-symmetry output stage.

Ultrasonic Power Sources

Ultrasonics is a term applied to a field of engineering in which high-frequency acoustical energy is used to effect an ultimate improvement in a product or process. The improvement may take place in cleaning, soldering, welding, drilling, defoaming, and degassing, or in control, measurement, detection, and medical diagnostics.

The frequency range used in ultrasonics is typically between 15 kHz and 10 Mhz. A few applications employ lower frequencies to achieve maximum particle displacement; at these lower frequencies, however, the power level must be kept low to avoid painful discomfort to those working in the vicinity. In testing applications, higher frequencies are required because the smaller the wavelength, the smaller the flaw that can be detected.

The power level used in ultrasonic engineering depends upon the application. Large-scale industrial-cleaning operations may require many kilowatts, while measuring and testing applications may require only a few microwatts. Table XXVIII lists some of the general industrial applications of ultrasonics, together with a brief description of the various applications and the typical power level and frequency required for each.

CHARACTERISTICS OF
ULTRASONIC TRANSDUCERS

Many devices can be used to produce ultrasonic energy; these devices are called transducers. All transducers can be classified in one of three groups: mechanical, magnetostrictive, or electrostrictive. Mechanical transducers are applied for the most part to the production of acoustic and ultrasonic oscillations in air or other gaseous media. Mechanical transducers used as sources of ultrasonic waves in air include whistles, gas-jet generators, and sirens. The power sources used in these devices usually incorporate a type of pressurized gas or fluid. The gas and liquid trans-

ducers convert a steady mechanical force into a vibratory mechanical force.

In solids, however, the same effect is not possible. In this case a source of electrical energy at the required operating frequency is converted into a vibrating mechanical force. This conversion is accomplished through the use of special materials which have magnetostrictive or electrostrictive properties.

Magnetostriction is the name applied to the change in length of a magnetic material under the influence of an external magnetic field. Whether a magnetic material (such as iron, nickel, cobalt, or a magnetic alloy) lengthens or shortens depends on a property of the material and is not dependent on the direction of the magnetic field. Fig. 337 shows the strain

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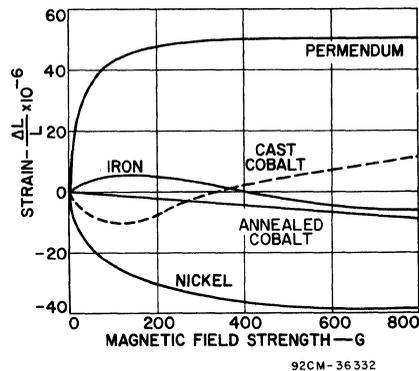
Fig. 337 - Strain as a function of magnetic field strength for several magnetostrictive materials.

(change in length per unit length) as a function of magnetic field strength for several magnetostrictive materials. The figure shows that nickel gets shorter as the magnetic field is increased, while Permendum gets longer. Fig. 338 shows how a bar of material that has a positive strain coefficient (lengthens with increased magnetic field) would react to an alternating magnetic field with no static biasing

Table XXVIII - Ultrasonic Applications

| Application	Description	Power Range (Watts)	Frequency Range (kHz)
Ultrasonic cleaning and degreasing	Cavitated cleaning solution scrubs parts immersed in solution.	50 to 25,000 (Typically 100 watts per gallon of solution).	20 to 40
Drilling, cutting, and polishing of hard and brittle materials.	Abrasive slurry between vibrating tool and work piece cuts into material.	50 to 2,000	16 to 30
Soldering and brazing.	Ultrasonically vibrating solder removes oxide film eliminating the need for flux.	0.5 to 250	16 to 30
Welding metals and plastics.	Vibrating tool generates high temperature at interface of the two materials.	10 to 1,000	16 to 30
Emulsification, dispersion, and homogenization.	Mixing and homogenizing of liquids, slurries and creams.	100 to 2,000	16 to 1,000
Control and measurement, alarm systems, counting.	Interruption or deflection of beam, damping of transducer.	0.1 to 50	16 to 45
Flaw detection.	Determination of size and location of flaws in solids by the pulse echo technique.	0.5 to 20	1,000 to 10,000
Medical: surgery and diagnostics.	Ultrasonic surgical knife cuts through tissue. Locating tumors and other flaws using the pulse-echo technique.	1 to 1,000	100 to 10,000
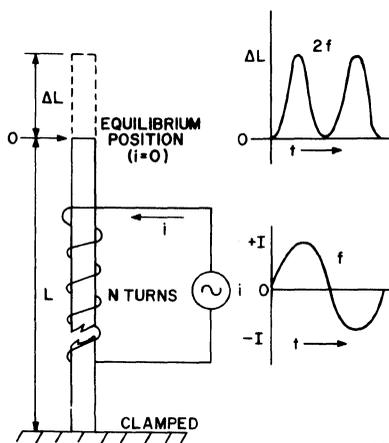
Fig. 338 - *Reaction of a bar of material that has a positive strain coefficient to an alternating magnetic field when no static biasing field is used. Waveforms show change in length of bar (top) and alternating current (bottom) used to produce the magnetic field.*

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field. The figure shows that the bar vibrates at twice the generator frequency and that the amplitude is ΔL peak to peak.

Fig. 339 shows the effect of adding a static biasing magnetic field. This bias could also be supplied by a permanent magnet. The dc bias field yields an initial displacement ΔL. Under these conditions, the bar oscillates about its equilibrium position at the frequency of the generator with a peak-to-peak amplitude of $2\Delta L$.
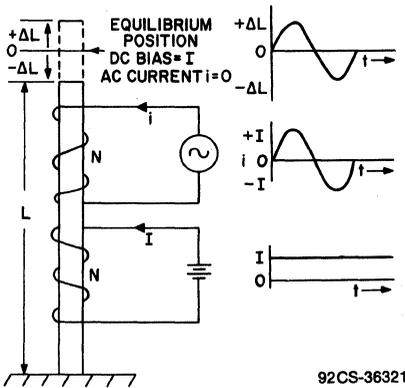
Fig. 339 - Reaction of bar of material that has a positive strain coefficient to an alternating magnetic field when static biasing is employed. Waveforms show change in length of bar (top), alternating current used to produce alternating field (center), and direct current (bottom) used to produce the bias field.

The **piezoelectric effect** is a phenomenon that occurs in certain crystals; the crystals are deformed when subjected to an electric field. The converse is also true; i.e., if the crystal (quartz, Rochelle salt, barium titanate) is strained, an electric charge appears at its edges.

The piezoelectric effect in the first mode is used in the generation of high-frequency sound waves. This effect is accomplished by application of an alternating voltage of the desired frequency to the crystal. Fig. 340 shows an example of this method.

In the design of equipment that uses electromechanical transducers, a useful equivalent circuit for the transducer must be available. Fig. 341(a) shows the equivalent of a magnetostrictive transducer in which Z_A, Z_B, and N depend upon the magnetic and physical
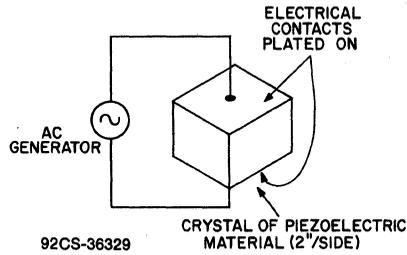

Fig. 340 - Application of an alternating voltage to a piezoelectric crystal to produce high-frequency sound waves.
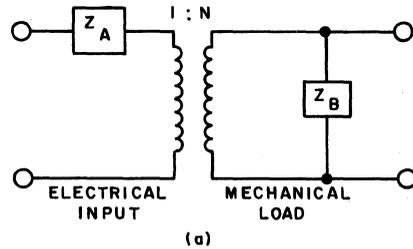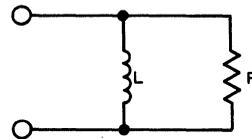
Fig. 341 - (a) Actual equivalent circuit and (b) simplified approximation of a magnetostrictive transducer.

properties of the core material. Fig. 341(b) is an approximate equivalent circuit for the transducer. The reactive component of the input impedance is attributed primarily to the inductance of the winding. This inductance is a function of the number of turns and the transducer core material. The resistance R represents the mechanical load. To obtain mechanical energy, it is necessary to provide electrical power to this resistance. Because magnetostrictive transducers usually operate with a static bias field, a dc component of current must be supplied to the transducer. Fig. 342 shows a typical circuit.

In the circuit, the choke is used to prevent the high-frequency signal from shorting through the low-impedance dc supply. The capacitor C is required to prevent dc from flowing through the generator. In addition, the value of C can be chosen so that the inductive reactance of the transducer is
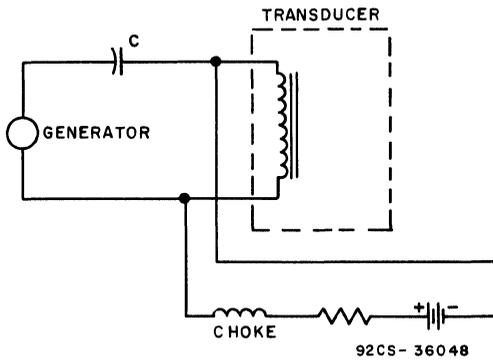
Fig. 342 - Circuit showing application of electrical power to a magneto-strictive transducer.

cancelled (series resonance).

Fig. 343(a) is the equivalent circuit for a piezoelectric crystal; Z_A, Z_B, and N are functions of the electrical and physical properties of the crystal. Fig. 343(b) shows the approximate equivalent circuit used to represent a piezoelectric transducer for the purpose of making calculations. The capacitance is usually tuned out by use of either a parallel or series inductor in the matching circuit between the generator and transducer.
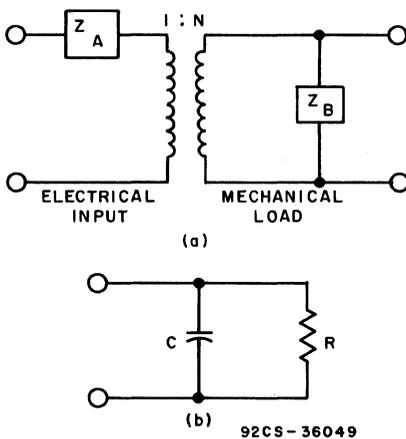

Fig. 343 - (a) Actual equivalent circuit and (b) simplified approximation of a piezoelectric crystal.

ULTRASONIC GENERATORS

The majority of ultrasonic applications employ a continuously oscillating power source. In fact the only application listed in Table XXVIII that does not make use of a continuous wave is flaw detection by the pulse-echo technique. For this reason, the

following discussion of ultrasonic power sources is limited to the continuous-wave type. Table XXVIII shows that most of the frequencies and power levels required are such that transistors can be used in the power generators. Therefore, the power sources discussed below are of the solid-state type.

The waveform delivered to the transducer can be of the square or sinusoidal type. As a result, there are four basic methods of power generation:

1. A low-power square-wave inverter followed by a class B push-pull power amplifier,
2. A square-wave power inverter that drives the load directly,
3. A low-power sine-wave oscillator followed by a class B push-pull amplifier,
4. A self-oscillating power amplifier that drives the load directly.

The detailed explanation of circuit operation and design procedures for each of these circuits is given in other parts of this Handbook.

If the transducer used can operate with a square-wave power source, then an inverter should be used because it affords very high efficiency. However, if the electromechanical transducer is required to deliver sinusoidal power to its load (cleaning solution, abrasive slurry, and the like), sinusoidal electrical power must be delivered to the resistor representing the load in the equivalent circuit of the transducer.

Inverter Circuits

Fig. 344 shows one method of obtaining a voltage sine wave across R_L. In this circuit, the
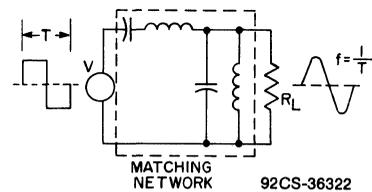

Fig. 344 - Use of a transducer and resonant matching network to convert a square-wave input to a sinusoidal output. Reactive component of transducer is used as the shunt inductor or capacitor of the matching network depending upon whether a magnetostrictive or electrostrictive type of transducer is used.

generator supplies a square-wave voltage; the matching network filters out the harmonics so that only the fundamental component remains. The matching network includes the reactive component of the transducer as a shunt inductor or capacitor, depending upon whether the transducer is of the magnetostrictive or electrostrictive type. In other words, the reactive component of the transducer is used as part of the filter. With this type of network, a transistorized inverter can be used to drive the transducer. The Q of the series tuned matching circuit should be at least 5.

The simplicity of this type of system is shown in Fig. 345. In the push-pull inverter with a series tuned load, each transistor provides current half of the time. The current flows only during the time that the transistor collector-to-emitter voltage is near zero [V_{CE}(sat)]. During the half-cycle when the voltage across the transistor is equal to $2V_{CC}$, there is no current flow. During both half-cycles, the dissipation in the device is very low. Theoretically, then, the efficiency could be very high. A thorough analysis and detailed design procedure for inverters is given in the section on **Power Conversion**.

Class C Oscillators

One disadvantage of the inverter approach is that the fundamental frequency is determined by the feedback network. Any time there is a change in the reactance of the load, its resonant frequency changes and the operating frequency of the inverter must be adjusted to the new resonant frequency. If the frequency is not adjusted, the power delivered to the load

decreases and the power dissipated in the transistor increases. With most practical transducers, the reactive component is continually changing.

One method used to overcome this problem is to let the load determine the frequency by use of a tuned-load class C oscillator, such as that shown in Fig. 346. With this arrangement, the operating frequency is always the resonant frequency of the load.
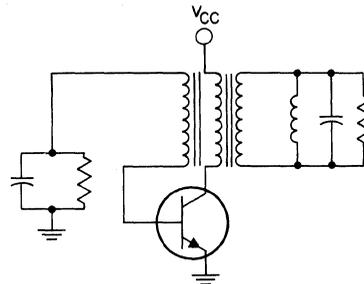
Fig. 346 - Class C oscillator that operates into a tuned load circuit.

Fig. 347 shows that the class C oscillator provides a pulse of current to the load. The load is parallel tuned; the voltage across the load, therefore, is sinusoidal. The period (T)
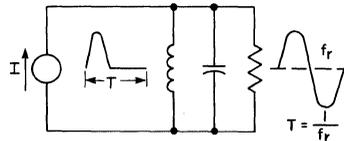
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Fig. 347 - Simplified equivalent circuit for the class C oscillator shown in Fig. 346.
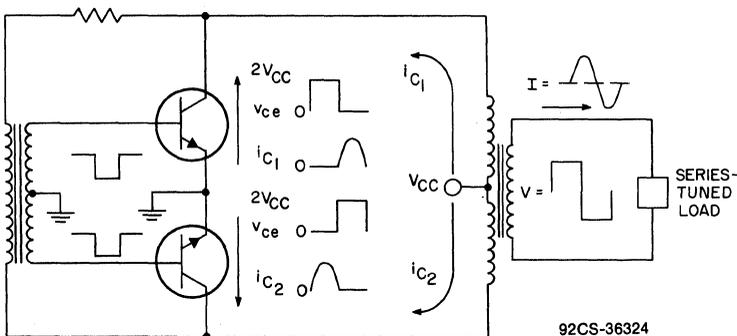
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Fig. 345 - Use of a push-pull switching inverter to drive a transducer that forms part of a series-tuned load circuit.

of the current pulse is equal to the reciprocal of the resonant frequency f_r of the load. Therefore, if f_r changes, there is a corresponding change in T. Fig. 348 shows the collector voltage and collector current for the class C oscillator.
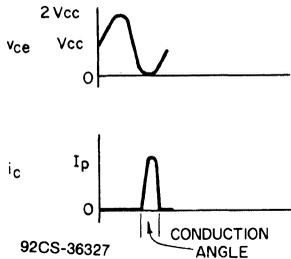
Fig. 348 - Collector voltage and current waveforms for the class C oscillator shown in Fig. 346.

The magnitude of the collector-current pulse is determined by the load power. The current peak occurs at $V_{CE}(sat)$, which is approximately zero. As the conduction time of i_c is made smaller, the efficiency increases; however, i_c must also increase to maintain the same power output. In the limit, an infinite pulse of zero width would yield 100-per-cent efficiency. However, this limit would require an infinite circuit Q. It can easily be shown that, for a fixed V_{CC} the power output is proportional to the area under the current pulse shown in Fig. 348, where the area is determined by the magnitude and conduction angle of the current pulse. The maximum value if i_c is limited by the maximum current rating of the transistor used. The maximum power output [for a given V_{CC} and $I_C(max)$], therefore, is proportional to the conduction angle. However, because the efficiency is inversely proportional to the conduction angle, it is obvious that some sort of compromise must be made. The following examples should help to determine the best compromise:

Example No. 1—In class C oscillators, the maximum collector voltage rises to a value equal to twice the supply voltage [i.e., $V_{CE}(max)= 2V_{CC}$], as indicated in Fig. 349. This condition occurs when the transistor is reverse-biased. The $V_{CEV}(sus)$ rating of the transistor used, therefore, should be equal to, or greater than, $2V_{CC}$. The relationship between dc input power P_s, power delivered to the load P_L, transistor dissipation P_d, and circuit efficiency η can be
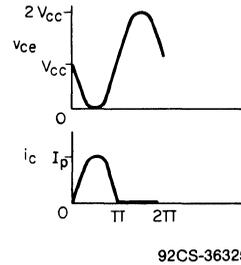
Fig. 349 - Collector voltage and current waveforms for an oscillator circuit that has a conduction angle of 180 degrees.

calculated for a typical transistor operated in a circuit of this type. The parameters assumed for the transistor are as follows:

$V_{CEV}(sus) = 100$ volts
$I_C(max) = 20$ amperes
$T_d(max) = 200° C$
TR_{J-C} (includes heat sink) $= 3° C/W$
$T_A = 80° C$ (ambient)

For these parameters, P_d should not exceed $(200 - 80)/3$, or 40 watts. For $V_{CC}=100/2=50$ volts, $I_p=I_C(max)=20$ amperes, and the conduction angle $\theta=\pi$ (maximum power output), the quantities P_s, P_L, P_d, and η are calculated as follows:

$$P_s = \frac{1}{2\pi}\int_0^{2\pi} V_{CC}\, i_c\, d\theta$$

$$= \frac{V_{CC}}{2\pi}\int_0^{\pi} I_p \sin\theta\, d\theta$$

$$= \left[\frac{V_{CC}\, I_p}{2\pi}(-\cos\theta)\right]_0^{\pi}$$

$$= \frac{V_{CC}\, I_p}{2\pi}(1+1)$$

$$= \frac{V_{CC}\, I_p}{\pi} = 0.317\, V_{CC}\, I_p = 320 \text{ watts}$$

$$P_L = \frac{1}{2\pi}\int_0^{\pi} V_{CC} \sin\theta\, I_p \sin\theta\, d\theta$$

$$= \frac{V_{CC}\, I_p}{2\pi}\int_0^{\pi} \sin^2\theta\, d\theta = \frac{V_{CC}\, I_p}{4}$$

$$= 0.25\, V_{CC}\, I_p = 250 \text{ watts}$$

$$P_d = P_s - P_L = 0.067\, V_{CC}\, I_p = 70 \text{ watts}$$

$$\eta = P_L/P_s = 78\%$$

The calculated value for the transistor dissipation (P_d=70 watts) exceeds the maxi-

mum allowable value (40 watts). This condition indicates the value calculated for the maximum power output (P_L=250 watts) cannot be obtained because of thermal limitations.

Example No. 2—If the conditions V_{CC}=50 volts and $\theta=\pi$ are maintained, then the efficiency η is still 78 per cent. The peak current I_p, therefore, must be reduced so that the transistor dissipation P_d does not exceed 40 watts. (The same heat sink and thermal temperature used in example No. 1 are assumed.) The new value of I_p is calculated as follows:

P_d=0.067 V_{CC} I_p=40 watts

I_p=40/(0.067 x 50)=11.9 amperes

The power delivered to the load P_L then becomes

P_L=(0.25)(50)(11.5)=149 watts

Although the transistor current is only slightly more than one-half the maximum current rating, the dissipation is equal to the maximum allowable value under the given conditions. In other words, the junction temperature is at its maximum rating.

Example No. 3—If the conduction angle is decreased to 1/3 of the cycle (i.e., $\theta=2\pi/3$= 120°), the transistor dissipation is substantially reduced. Fig. 350 shows the collector current and voltage waveforms for this condition. If
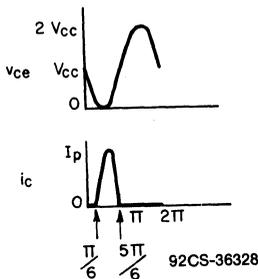
Fig. 350 - Collector voltage and current waveforms for an oscillator circuit that has a conduction angle of 120 degrees.

all other conditions are assumed to be the same as for example No. 1, the dc input power, load power, transistor dissipation, and efficiency are calculated as follows:

$$P_s = \frac{1}{2\pi} \int_{\pi/6}^{5\pi/6} V_{CC} \, I_p \sin \frac{3}{2} \, \theta \, d\theta$$

$$= \left[\frac{V_{CC} \, I_p}{2\pi} \left(-\frac{2}{3} \cos \frac{3}{2} \theta \right) \right]_{\pi/6}^{5\pi/6}$$

$$= \frac{-V_{CC} \, I_p}{3\pi} \left[\cos \frac{3}{2} \left(\frac{5\pi}{6} \right) - \cos \frac{3}{2} \left(\frac{\pi}{6} \right) \right]$$

$$= \frac{V_{CC} \, I_p}{3\pi} \, (2) \left(-\frac{1}{\sqrt{2}} \right)$$

$$= 0.15 \, V_{CC} \, I_p = 150 \text{ watts}$$

$$P_L = \frac{1}{2\pi} \int_{\pi/6}^{5\pi/6} V_{CC} \sin \theta \, I_p \sin \frac{3}{2} \, \theta \, d\theta$$

$$= \frac{V_{CC} \, I_p}{2\pi} \int_{\pi/6}^{5\pi/6} \sin \theta \sin \frac{3}{2} \, \theta \, d\theta$$

$$= \frac{V_{CC} \, I_p}{2\pi} \left[\frac{\sin \left(\frac{3}{2} - 1 \right)}{2 \left(\frac{3}{2} - 1 \right)} - \frac{\sin \left(\frac{3}{2} + 1 \right)}{2 \left(\frac{3}{2} + 1 \right)} \right]_{\pi/6}^{5\pi/6} = \frac{V_{CC} \, I_p}{2\pi}$$

$$\frac{V_{CC} \, I_p}{2\pi} \left[\sin \frac{1}{2} \, \theta - \frac{\sin \frac{5}{2} \theta}{5} \right]_{\pi/6}^{5\pi/6}$$

$$= \frac{V_{CC} \, I_p}{2\pi} \, (0.966{-}0.05{-}0.26{+}0.193)$$

$$= \frac{0.85}{2\pi} \, V_{CC} \, I_p = 0.135 \, V_{CC} \, I_p$$

$$= 35 \text{ watts}$$

$$P_d = P_s - P_L = 0.015 \, V_{CC} \, I_p$$

$$= 15 \text{ watts}$$

$$\eta = P_L / P_s = 90 \text{ per cent}$$

For a conduction angle of one-third of a cycle, therefore, the transistor is not limited by power dissipation under the conditions stated. The transistor can operate at full voltage and current ratings. If the heat sink used in examples Nos. 1 and 2 is employed, the junction temperature is maintained well below the rated level.

Example No. 4—The design of a practical class C oscillator which has a conduction

angle θ of 120° and an over-all circuit efficiency η of about 80 per cent is illustrated by the following example:

The design conditions are as follows:

V_{CC}=50 volts; P_L=125 watts
R_L=1000 ohms in parallel with a 0.005-microfarad capacitor
f=25 kHz
TR_{HS}=2° C/W
T_A=80° C
θ=2π/3

For these conditions, the following values are calculated:

P_L=(0.135) (V_{CC}) (I_p)
125=(0.135) (50) (I_p)
I_p=18.5 amperes
P_d=(0.015) (50) (18.5)=14 watts

The Q of the load circuits, which is equivalent $R_L/2\pi fL$ for a parallel tuned network, is 2.5. The value of the load-circuit inductance L, therefore, may be calculated as follows:

L=1000/(2π) (25) (10^3) (2.5)
=2.5 millihenries

The load-circuit capacitance then is determined as follows:

2πf=1/(LC)$^{1/2}$
C=0.01 microfarad

Because the load resistance R_L is shunted by a capacitance of 0.005 microfarad, the actual value of the capacitor used in the output tuned circuit is 0.015 — 0.005, or 0.01 microfarad.

The transistor requirements are as follows:

V_{CEV}(sus) $\geq$ 2 V_{CC}=100 volts
I_C(max) $\geq$ 18.5 amperes
P_d(max) $\geq$ 14 watts at T_C=108° C
[80° C ambient + (14) (2° C/W)]

Therefore, the thermal resistance from junction to case $\theta_{J-C} \leq$ 7° C/watt.

Information on the selection of core size and material is given in the section on **Power Conversion**. For this design, a toroid of linear material (Arnold Engineering No. A438381-2 or equivalent) is used. Use of 100 turns of No. 24 wire for the secondary winding provides 2.7 millihenries of open-circuit inductance. This secondary provides the inductance of the matching network.

The power output P_L is equal to 125 watts, and the load resistance R_L is equal to 1000 ohms. The peak voltage across the load, therefore, is 500 volts. The transformer turns ratio then becomes

N=500/50=10:1

Ten turns of No. 22 wire, therefore, are required for the primary. Fig. 351 shows the schematic diagram of the completed circuit, and Fig. 352 shows the circuit waveforms.
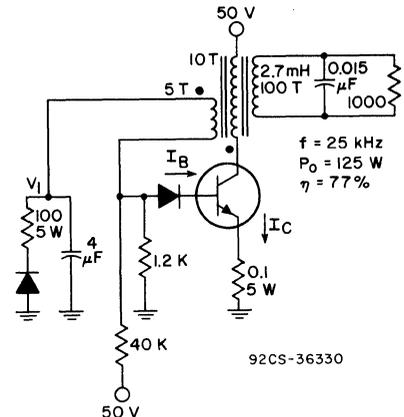
Fig. 351 - 125-watt, 25-kHz, class C oscillator.
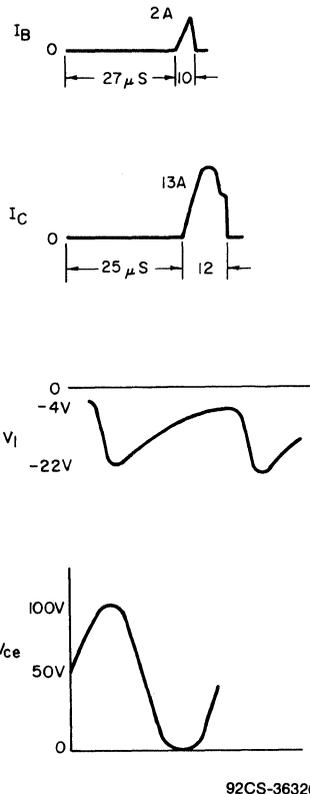
Fig. 352 - Current and voltage waveforms for the class C oscillator shown in Fig. 351.

ULTRASONIC POWER AMPLIFIERS

In general, the power amplifiers used to drive ultrasonic transducers are the same as those used to drive the loudspeakers in audio-amplifier applications. The basic design considerations and circuit configurations described in the section on **Audio Power Amplifiers** are applicable, therefore, to the design of power amplifiers for ultrasonic applications. The frequency range of the basic amplifier configurations can be readily extended into the range of 10 kHz to 100 kHz normally used in ultrasonic systems by selection of higher-frequency power transistors, use of smaller inductive and capacitive coupling components, and a proper choice of values for feedback elements.

Automotive Applications

This chapter discusses the application of semiconductor power devices to automotive systems. Automotive systems are broadly defined to include all surface vehicles employing internal combustion engines. Power devices perform a wide variety of functions in such systems, and many more functions are being considered.

Table XXIX is a listing of systems showing the function performed by the power device, the voltage and current requirements imposed on the device, and typical devices employed.

GENERAL DEVICE REQUIREMENTS

The performance requirements of power devices in automotive systems are almost always dictated by worst-case conditions. Although they occur infrequently, these conditions must be accommodated in order to permit the vehicle to function adequately under all reasonably encountered circumstances. Some requirements are imposed so that minimum system performance levels are achieved, others are imposed to assure survival of the power device under transient and fault conditions to which the device may be exposed.

The following are the most common worst-case or extreme conditions which must be considered individually and to varying degrees in combination:

1. **Ambient temperature range.**
   −40° C (−30° C for selected systems); +85° C (passenger compartment systems); +100° C (engine compartment systems)—for some specialized engine compartment systems this may reach +125° C.
2. **Continuous high system voltage.**
   For the nominal 14-volt automotive system an extreme voltage of 24 volts is usually the maximum voltage which occurs during "jump" or booster starting of a vehicle with a dead battery. The jump start source is from two 12-volt batteries in series, or from a 24-volt service vehicle

electrical system. The power device must survive the conditions imposed when the system voltage goes to 24 volts for short periods. With the nominal 14-volt system, the power device must function properly at 17 to 18 volts for extended periods, in the event the voltage regulator fails in the full-field or over-charge mode.
3. **Reverse battery.**
   The power device must also survive conditions experienced when the battery is inadvertently connected to the system with reverse polarity for short periods.
4. **Low system voltage.**
   Minimum performance levels are usually required at voltages as low as 5 to 10 volts, depending on the system.
5. **Transient voltage (forward polarity).**
   Forward voltage transients of 75 to 150 V with exponentially time-decaying waveforms having time constants of many 10's of milliseconds are experienced in automotive electrical systems if the battery is disconnected while the engine is running. This condition is referred to as "load dump" because it occurs when the stabilizing effect of the battery (the load) is removed. When load dump occurs, it is important that the power device have the voltage- and/or energy-handling capability to survive the transient voltage conditions imposed by the particular system.
6. **Transient voltage (reverse polarity).**
   A transient voltage of reverse polarity, also referred to as a negative transient, is generated in an automotive system when a circuit in series with an inductor is opened under load (see Figs. 353 and 354), while current is flowing, thus interrupting the current. This voltage is also called a field decay transient which is normally limited to the specific circuit being opened, and will not generate a transient on the system bus to which the

Table XXIX

| System		Function	Device Requirements (Approx.)		RCA Device			
			Voltage V	Current A	Type	Polarity	Class	Package
Automotive Voltage Regulator		Controls Current to Alternator Field Winding	40-150	5	2N6107	p-n-p	Transistor	TO-220
					2N6668	p-n-p	Darlington	TO-220
					2N6669	n-p-n	Transistor	TO-220
					2N6533	n-p-n	Darlington	TO-220
					RCA8766	n-p-n	Darlington	TO-3
Automotive Engine Ignition (Inductive-Discharge)		Output Device: Switches Current in Ignition Spark Coil	400	5	2N6513	n-p-n	Transistor	TO-3
					RCA8766B	n-p-n	Darlington	TO-3
		Driver: Supplies Base Drive to Output Device	80	1	2N6385	n-p-n	Darlington	TO-3
					2N6292	n-p-n	Transistor	TO-220
Automotive Engine Ignition (Capacitive-Discharge)		Inverter: Charges Capacitor	60	5	2N3055	n-p-n	Transistor	TO-3
Automotive Radio		Class A Audio Amplifier	35	1	2N3054	n-p-n	Transistor	TO-66
		Class B True-Comp. Audio Amplifier	40	1.5	2N6288	n-p-n	Transistor	TO-220
					2N6111	p-n-p	Transistor	TO-220
Automotive Tape Player		Motor Drive	40	1	2N5296	n-p-n	Transistor	TO-220
					2N6288	n-p-n	Transistor	TO-220
Anti-Skid Adaptive Braking		Solenoid Driver	80	3-5	2N5496	n-p-n	Transistor	TO-220
					2N6388	n-p-n	Darlington	TO-220
					2N3055	n-p-n	Transistor	TO-3
Air Conditioner Blower		Motor Control	80	20	2N6385	n-p-n	Darlington	TO-3
					2N3772	n-p-n	Transistor	TO-3
					2N5303	n-p-n	Transistor	TO-3
Instrument Cluster		Series Regulator Lamp Driver	60-80	1-3	2N6668	p-n-p	Darlington	TO-220
					2N6292	n-p-n	Transistor	TO-220
					2N6478	n-p-n	Transistor	TO-220
					2N6388	n-p-n	Darlington	TO-220
Engine Governor		Solenoid Driver	80	1	2N6388	n-p-n	Darlington	TO-220
	Feedback Carburetor	Solenoid Driver or Stepped Motor Drive	80	1	2N6388	n-p-n	Darlington	TO-220
					2N6668	p-n-p	Darlington	TO-220
					2N6292	n-p-n	Transistor	TO-220
	Fuel Injection	Solenoid Driver	80	5	2N6101	n-p-n	Transistor	TO-220
					2N6388	n-p-n	Darlington	TO-220
					2N5886	n-p-n	Transistor	TO-3
Electronic Engine Controls	Fuel Pump	Motor Drive	80	15	2N6286	p-n-p	Darlington	TO-3
	Fuel Metering	Servo Motor Drive or Solenoid Driver	80	10	2N6383	n-p-n	Darlington	TO-3
					2N6386	p-n-p	Darlington	TO-3
	Exhaust Gas Recirculation	Servo Motor Drive or Solenoid Driver	80	10	2N6388	n-p-n	Darlington	TO-3
					2N6668	p-n-p	Darlington	TO-3
	Cold-Start Control	Solenoid Driver	80	5	2N6388	n-p-n	Darlington	TO-220
					2N6668	p-n-p	Darlington	TO-220
	Transmission Control	Solenoid Driver	80	5	2N6388	n-p-n	Darlington	TO-220
					2N6668	p-n-p	Darlington	TO-220
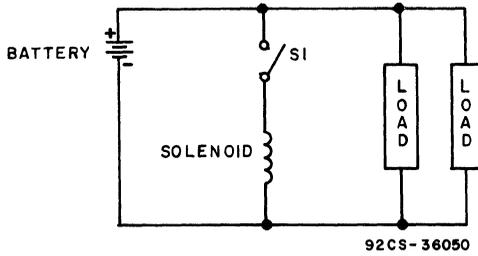
Fig. 353 - Negative transient condition.
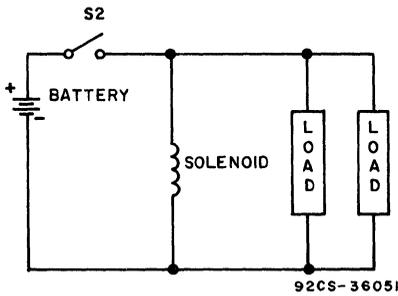
Fig. 354 - Negative transient condition.
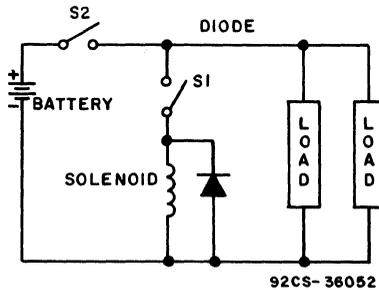
Fig. 355 - Diode suppression of negative transient.

battery is still connected. However, if the current interruption is caused by disconnecting the battery from the system bus, the resulting transient will appear on the entire system, unless provision is made to limit the voltage as the inductor is discharged.

The negative transient is typically an exponentially decaying waveform having a voltage of 75 to 100 volts peak, and a time constant of several milliseconds. Loads which can generate the negative transient are solenoids, the field winding of the alternator, and motors. In systems where negative transients can be generated, the power device must be capable of surviving the conditions generated by these transients.

In most circuits when a solid-state power device is employed to switch the current to the inductive load, a diode is connected across the inductive load (Fig. 355) in such a way that the diode is not disconnected from the load during switching. This diode limits the voltage appearing across the inductor to the diode voltage drop while the inductor is being discharged. Under these conditions negative transients will not be impressed on the system bus.

It is recommended that all inductive loads including solenoids and motors be provided with a shunting diode of sufficient current rating to absorb all negative transients.

7. **Mechanical.**
The mechanical shock and vibration conditions experienced do not significantly affect device performance. However, the method used to mount the devices in the system can introduce conditions detrimental to that performance. If excessive forces are employed in securing the devices to the mounting structure, permanent deformation can occur, with resultant internal damage to the devices. On the other hand, if device headers are only loosely secured to mounting structures that also serve as heat-removal elements, excessive heating of the device can occur.

8. **Thermal cycling.**
The device must be of such a design that it will continue to function in a suitable manner after repeated thermal cycles to the extreme temperatures typically experienced in service. The number of cycles to be imposed should be consistent with the service life of the system.

Transistor Requirements

The type of transistor selected for use in automotive electrical systems is dictated by the following considerations:

A. The **collector-to-emitter saturation voltage**, $V_{CE}(sat)$, at given I_C and I_b, and the **base-to-emitter voltage**, V_{BE}, at given I_C and V_{CE}. These specifications, which the transistor must meet in terms of the indicated conditions and limits are determined by on-state performance requirements imposed by the system at the lowest battery voltage and at the lowest ambient temperatures. In some instances, the

V_{CE}(sat) conditions and limits must also be specified at the highest junction temperatures consistent with acceptable performance. Production testing is usually performed at room temperature, with test conditions and/or limits appropriately guardbanded to assure that performance at the temperature extremes is maintained within the specification limits. Tests at the temperature extremes are usually performed on a sampling basis.

B. The **leakage specification** for the transistor is determined from the maximum permissible off-state current at the highest junction temperature, at a high collector-to-emitter voltage, and with a specific base-to-emitter termination. A typical base-to-emitter configuration, shown in Fig. 356, includes:

1. Base-to-emitter resistor, R_{BE}.
2. Current sinking transistor, with the collector of Q_1 connected to the base of Q_0, and emitter of Q_1 connected to emitter of Q_0. See Fig. 356 which may be used with or without series resistor R_1.


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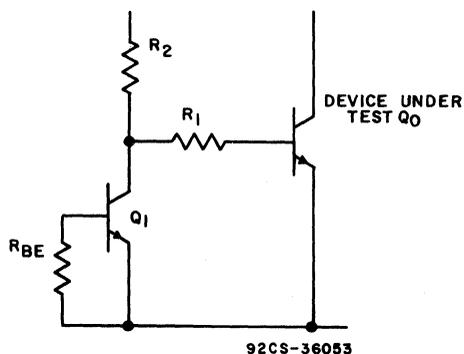
Fig. 356 - Typical transistor circuit configuration.

In this circuit the device under test experiences a small forward bias which is the V_{CE}(sat) voltage of device Q_1.

To verify performance at the required elevated temperature the test may be set up as follows:

1. **As a leakage test**: For a maximum limit of I_C leakage at a specified collector-to-emitter voltage (V_{CE}) and forward-bias voltage (V_{BE}) or,
2. **As a forward-bias voltage (V_{BE}) test**: For a minimum V_{BE} at specified I_C (corresponding to maximum permis-

sible leakage) and V_{CE}. If a device exhibits a V_{BE} value below the minimum limit, the device is rejected.

C. The **sustaining voltage and breakdown voltage** requirements of a transistor are usually governed by the voltage the device will experience in the system under load-dump conditions. For output transistors in ignition service these voltages are dependent on the clamp circuit which limits the peak collector voltage during turn-off.

D. The **energy-handling (safe-operating-area or SOA)** capability of the device may be dictated by conditions experienced under high battery operation and conditions experienced during load dump. In the case of output transistors for ignition service, the worst-case condition occurs under high battery operation with an open-circuit ignition-coil secondary (disconnected spark plug). In testing these transistors, a "use test" inductive discharge circuit simulating the above worst-case system condition is specified to insure SOA capability.

AUTOMOTIVE IGNITION SYSTEMS

Under worst-case conditions, about 22 kilovolts are required to ignite the combustible mixture in the cylinder of an automobile engine. In addition, a minimum energy of about 20 millijoules must be available in the spark to assure propagation of a stable flame front originating at the spark. The exact values of voltage and energy required under all operating conditions depend on many factors, including those described in the following paragraphs.

Condition of spark plugs—Fouled plugs reduce both the voltage and the energy available for ignition. The plug gap also affects both the voltage and the energy required. As the plug gap is increased, the required voltage increases, but the required energy decreases.

Cylinder pressure—The cylinder pressure depends on both the compression at the point of ignition and the air-fuel mixture. The minimum breakover voltage in any gas is a function of the product of gas pressure and electrode spacing (Paschen's Law). In automobile engines, the minimum voltage increases as this product increases. Therefore, higher pressures also require higher voltages. How-

ever, the energy required decreases as the pressure increases, and increases as the fuel-air mixture deviates from the optimum ratio. Worst-case conditions occur when the engine is started, at idle speeds, and during acceleration from a low speed because carburetion is poor and the fuel-air mixture is lean. The combination of a lower cylinder pressure and a dilute fuel-air mixture under these conditions results in a high energy requirement.

Spark plug polarity—The center electrode of the spark plug is hotter than the outside electrode because of the thermal resistance of the ceramic sleeve that supports it. If the center electrode is made negative, the effect of thermionic emission from this electrode can reduce the required ignition voltage by 20 to 50 per cent.

Spark plug voltage waveshape—The spark plug voltage waveshape is shown qualitatively in Fig. 357. The voltage starts to rise at point A and reaches ignition at point B. The region from B' to C represents the sustaining voltage for ionization across the spark plug. When there is insufficient energy left to maintain the discharge (at point C), current flow ceases and the remaining energy is dissipated by ringing. The final small spike at point D occurs when the ignition coil again starts to pass current.
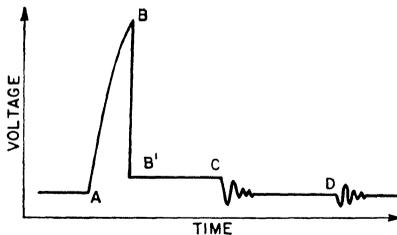
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*Fig. 357 - Ignition-voltage waveshape.*

The two most important characteristics of the voltage waveshape are its rise time (from A to B) and the spark duration (from B' to C). A rise time that is too long results in excessive energy dissipation with fouled plugs; a rise time that is too short can lead to loss by radiation through the ignition harness of the high-frequency components of the voltage. The minimum rise time should be about 10 microseconds; a 50-microsecond rise time is acceptable. Conventional systems have a typical rise time of about 100 microseconds. It should be noted that, at an engine speed of

5000 revolutions per minute, one revolution takes 12 milliseconds. Engine timing accuracy is usually no better than 2 degrees, which corresponds to 67 microseconds. The error caused by the rise time is therefore comparable to normal timing errors. At normal cruising speeds (about 2000 revolutions per minute), the 2-degree timing error corresponds to about 165 microseconds, and rise-time effects are negligible.

Energy storage—The energy delivered to the spark plug can be stored in either an inductor or a capacitor. Although the inductive storage method is the more common approach, both are used. Both are discussed below. One requirement common to both methods is that, after the storage element is discharged by ignition, it must be recharged before the next spark plug is fired. For an eight-cylinder engine that has a dwell angle of 30 degrees, the time τ between ignition pulses (in milliseconds) is equal to 15,000 divided by the engine r/min., and the time t_{on} during which the points are closed is equal to $10,000/r/min$. When the engine r/min. is 5000, t_{on} is 2 milliseconds. Therefore, the charging time constant for either an inductive or a capacitive storage system should be small compared to 2 milliseconds.

Inductive-Discharge Automotive Systems

Fig. 358 shows the basic circuit for an inductive-discharge system. The total primary-circuit resistance (ballast plus coil) is represented by R_p; the primary inductance of the coil is represented by L_p. Switch S respresents the points in a conventional system. The step-up turns ratio of the transformer is N. When the points close, current increases exponentially with a time constant t_L equal to L_p/R_p.
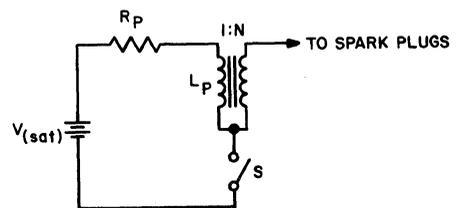
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Fig. 358 - Basic inductive-discharge ignition circuit (Kettering system).
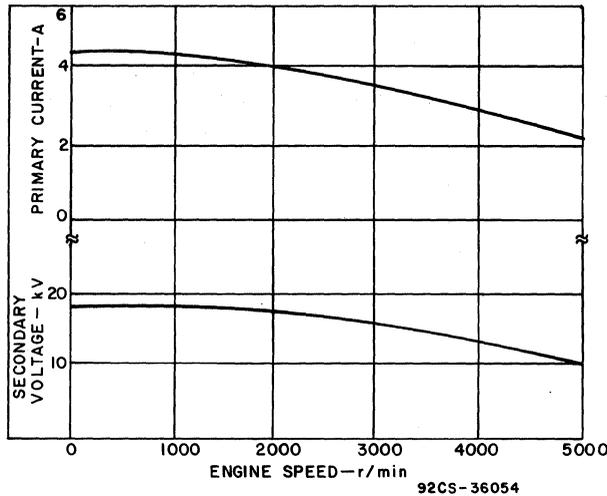
Fig. 359 - *Performance of conventional inductive-discharge ignition system.*

The maximum primary current I_p is equal to V_{BAT}/R_p, and the energy e_L stored in the coil is equal to $L_pI_p^2/2$. When the points open, a voltage V_p is generated across the primary terminals; this voltage is equal to $-L_p(dI_p/dt)$, where I_p is the primary current as a function of time t. The secondary voltage V_S, which is delivered to the spark plugs through the distributor, is equal to NV_p.

The maximum current is limited to about 4 amperes by possible burnout of the points. The total energy stored in the coil must be about 50 millijoules to provide for energy losses by radiation, fouled plugs, and the like. For a battery voltage of 12 volts and a primary-circuit resistance of 3 ohms, L_p must have a value of about 6 millihenries. The time constant t_L is then about 2 milliseconds; the coil current does not reach its maximum value at high engine speeds. Fig. 359 shows primary current and secondary voltage as a function of engine speed for a typical non-transistorized ignition circuit. The degradation in secondary voltage follows the primary current. The available energy decreases even more rapidly because it is proportional to the square of the current. This problem can be even more severe than indicated because some conventional ignition coils have inductances as high as 12 millihenries, and the time constant is correspondingly longer.

Capacitive-Discharge Systems

Capacitive-discharge (CD) ignition systems

have been in use since the introduction of silicon controlled rectifiers (SCR's). The early recognition and application of the benefits of the SCR CD ignition in limited areas of the small-engine market (one-cylinder, two- and four-cycle engines, and marine engines) has since expanded to nearly 100 per cent penetration of that market. Typical applications are chain saws, lawn mowers, snowmobiles, motorcycles, mini-bikes, fence chargers and auxiliary power sources relying on the maintenance-free, high performance CD ignition system. For further discussion of CD systems refer to the **RCA Solid-State Devices Manual**, SC-16.

The emission standards and service restrictions imposed on the automotive industry have made electronic ignition systems all but mandatory. An improvement in nearly any part of the engine will help to meet the emission requirements, and even if the contribution of the electronic ignition to the total improvement of the performance of the automobile is considered small, it is significant. Those areas in which the present system is deficient and in which the electronic system is superior are explained below.

The points (contacts) in the standard ignition system produce ignition timing errors in three ways, as shown in Fig. 360: 1) wear of the rubbing block, 2) variations in the cam profile, and 3) shaft eccentricity. Cam and shaft eccentricity change the timing of each cylinder relative to the others. The elimination of these

(a) POINTS

1. RUBBING BLOCK
2. CAM
3. SHAFT

AIR GAP
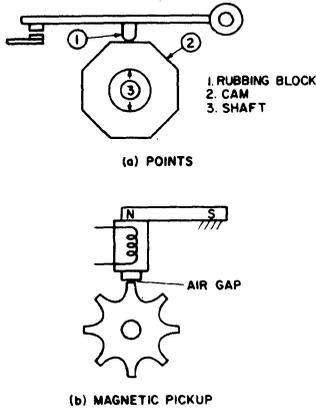
(b) MAGNETIC PICKUP

Fig. 360 - (a) Standard ignition timing system, (b) magnetic pickup timing system.

points of wear in the ignition-point system is also helpful in meeting the emissions tests for 50,000 miles without engine service. These three problems are solved by using a magnetic pickup, Fig. 360, instead of points. But a magnetic pickup produces only a small signal, which necessitates amplification and, hence, an electronic system.

In summary, the automotive industry is using electronic ignition to obtain performance not previously required—more accurate spark timing and the elimination of the need for periodic adjustment of the timing.

Legal restrictions prohibit the description of circuits in use by particular manufacturers; however, a general discussion of the four principal characteristics of inductive ignition systems is appropriate. These characteristics include dwell, battery-voltage compensation, high-voltage limiting, and obtaining output-transistor base drive.

Dwell—Dwell is the portion of the operating cycle in which the ignition coil is being charged, and is expressed in either per cent (as in this discussion), in degrees of crankshaft rotation (100% dwell=90° for 8 cylinders; 100% dwell=120° for 6 cylinders, etc.), or in milliseconds (the amount varies with r/min.). Breaker points produce constantpercentage dwells independent of r/min., as shown in curve 3 of Fig. 361(a). This is not the optimum dwell; it is excessive at low r/min. and wastes current as shown in Fig. 361(b). At high r/min., Fig. 361(c), the dwell is more correct. Fig. 361(d) shows spark energy as a function of r/min. for a constant-per cent dwell system. The minimum dwell is shown in curve 1 of Fig. 361(a). This dwell would minimize the battery current consumption. A magnetic pickup does not allow the use of a simple circuit to compensate for acceleration. One solution adds extra dwell; this approach produces curve 2 of Fig. 361(a).

These functions are important because a magnetic pickup can only produce a 50%

(a) comparison of dwell percentages *vs.* r/min.

① IDEAL DWELL-NO ACCELERATION
② DWELL REQUIRED FOR 4000 RPM/S ACCELERATION WITH NO ACCELERATION CORRECTION
③ POINTS SYSTEM

(e) two practical dwell curves.

(b) engine idling at 500 r/min.

PEAK CURRENT AT IDLE

(c) engine at 5000 r/min (same scale as Fig. 2b).

(d) spark energy as a function of r/min for a constant-percent dwell system.
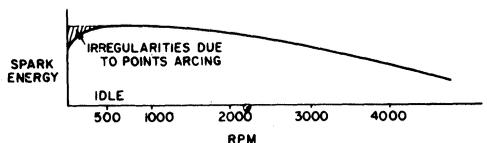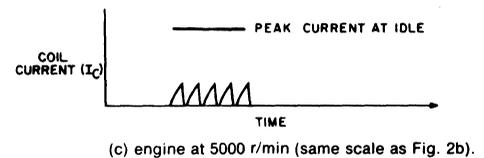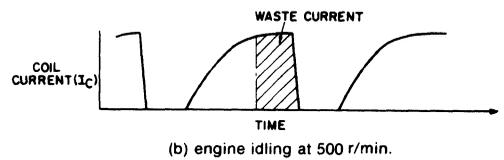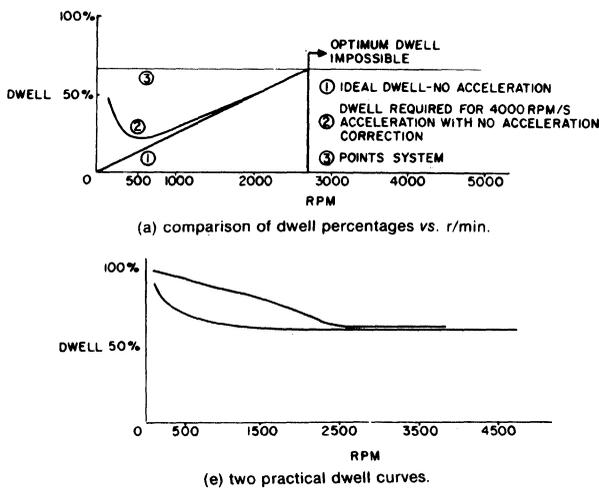
Fig. 361 - Ignition system dwell waveforms.
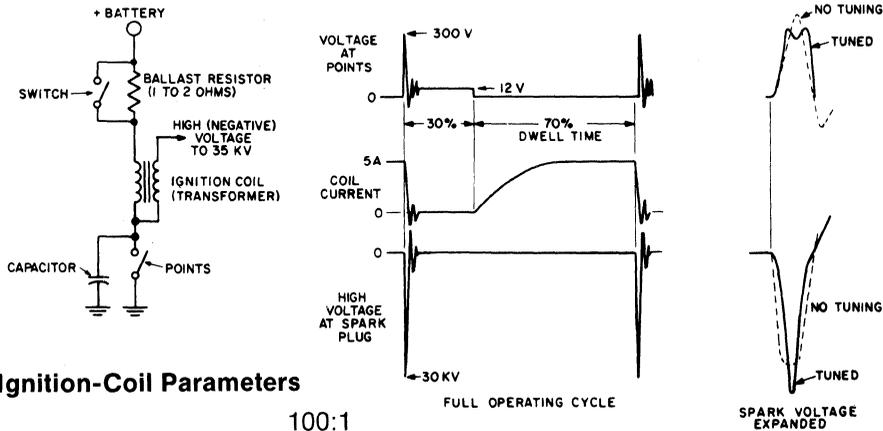
Typical Ignition-Coil Parameters

Turns Ratio	100:1
Secondary	25,000 turns #41
Primary	250 turns #22
Primary Inductance	6 to 10 mH
Primary Resistance	about 1.5 ohms
Secondary Inductance	40 H
Secondary Resistance	10 kilohms

Fig. 362 - *Operation of a basic ignition circuit. A low engine speed and a disconnected spark plug are assumed for clarity. The high voltage is generated when the points located in the distributor open. The capacitor reduces arcing by decreasing the rate of voltage rise at the points. It also "third-harmonic" tunes the coil and raises the peak output voltage. The switch shown may be built into the ignition switch, the starter, or the starter relay.*

dwell unless electronic circuits are added. The resultant dwell function will be a compromise with circuit economics. Two simple, practical, dwell curves are shown in Fig. 361(e).

Battery-voltage compensation—Some method must be used to compensate for battery-voltage variation. Just when the best spark is needed—during starting—a low battery voltage exists. When starting, the plugs and the air are cold, the cylinder pressure is up, and the fuel mixture is poorly controlled, so a good spark is needed. The battery voltage drops as much as 60% because of the high current drain in the starter motor. Conventionally, this loss in battery voltage is compensated for by shorting a ballast resistor in the ignition, as shown in Fig. 362. However, when used with an electronic ignition, this method causes excessive transistor currents when the battery is fully charged, or worse if a booster battery (24 V) is applied by a service truck. The latter is a worst-case condition for the transistor; the collector currents can approach 20 A.

An electronic ignition system can be made to compensate for battery-voltage variations if the output transistor is made to operate as a current limiter. However, not only is it difficult to cool a transistor operating in the active-region in the hostile environment under the engine hood, but such operation limits the number of suitable mounting locations. Also important is the fact that a system so operated produces less spark energy than the point system when the battery is fresh, and this might adversely affect starting capability when the engine is hot.

High-voltage limiting—High-voltage limiting is concerned with the method used to protect the output transistor from excessively high voltages. All of the systems being used or considered by the automotive manufacturers use the standard 100-to-1 turns-ratio coil, and require the transistor to operate at approximately 300 V. Either a disconnected spark plug or a cold start with a good battery can raise the transistor's voltage to 800 or 1,000 V. There are four ways to eliminate the need for a 1,000-V transistor. The coil current can be limited by the output transistor, as described
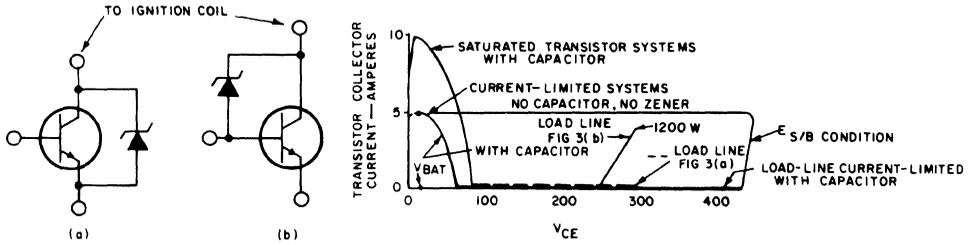
Fig. 363 - Methods of eliminating the need for a 1,000-V transistor in the transistor ignition system.

above, in which case a 400- or 500-V transistor would be adequate. The second way is to use a zener clamp from the transistor's collector to its emitter to absorb the energy, as shown in Fig. 363(a), however, the required 10-W zener is expensive. The third way to protect the transistor is to use the transistor to amplify the zener output. The zener is a 0.5-W unit placed across the transistor's collector and base, as shown in Fig. 363(b). The transistor must dissipate high peak powers (900 W) in short pulses. The fourth way is to use a 300-V transistor that can absorb the energy in a voltage-breakdown mode. This approach would be the most expensive with the present state of the art.

An example of the worst-case load lines are shown in Fig. 363(c). Current limiting requires high power-dissipation capability, particularly when the engine stalls. When no capacitor is used, a severe second-breakdown condition exists. In saturated transistor-switch systems with collector-emitter zeners, the transistor requirements are minimized. Despite the high pulse-power loads needed for the collector-base zener approach, this system is the least expensive.

Each of the methods discussed requires different output transistor capabilities.

Obtaining base drive—The final difference among inductive, electronic-ignition systems is the source of base drive for the power transistor. Cost-effective, high-voltage power transistors require more than one ampere of base drive for the starting condition (a battery voltage of 6 V and a collector current of 3 to 5 A); two methods exist for obtaining this current. In the first, a Darlington transistor is used, as shown in Fig. 364(a), which means that the base drive of the output transistor passes through the coil. This arrangement minimizes the current requirement but in-

creases $V_{CE}(sat)$, and a lower resistance, more expensive coil is needed. In the second approach, as shown in Fig. 364(b), the base drive comes from the battery through a separate power resistor. This yields a better $V_{CE}(sat)$, but requires up to 3 A more battery current, a 50-W resistor, and extra wiring.


Fig. 364 - Methods of obtaining base-drive.

A typical circuit for the power stage of an automotive ignition system is shown in Fig. 365. The saturation voltage $V_{CE}(sat)$ of the

Fig. 365 - *Typical automotive ignition circuit.*

92CS-36055

output device Q_0 is governed by the relationship: $V_{CE}(sat) \leq V_S$ low $- I_C(R_L + R_2)$ at specified I_C and $T_{ambient}$. (This relation assumes I_b has negligible effect on the voltage drop across R_2) where

V_S = supply voltage

V_S low = lowest value of system voltage at which performance is expected (starting or cranking mode)

I_C = minimum allowable coil current which provides adequate energy for the ignition spark

R_2 = low-value sensing resistor often used to monitor and control coil current

R_L = internal resistance of the primary winding of the ignition coil. The value of R_L depends on the ambient temperature because most coil windings are of copper. Therefore, the appropriate value of R_L should be used corresponding to the specified ambient temperature.

T_A = Typically $-30°$ C for the low-temperature extreme, $+100°$ C to $125°$ C for the high-temperature extreme

I_b = base current to Q_0

It is usually necessary to specify the $V_{CE}(sat)$ requirements at the two temperature extremes.

The relationship for the base driving current (I_b) required, and the related components and device parameters are derived from the following expression:

$$V_S = V_{CE}(sat)(Q_1) + V_{BE}(Q_0) + R_2 (I_c + I_b) + R_1 \left(I_b + \frac{V_{BE}(Q_0) + R_2(I_c + I_b)}{R_3} \right)$$

This expression assumes that the contribution of the driving current to Q_1 through R_4 can be neglected for purposes of determining the voltage distribution in the main Q_0 drive circuit. The expression can be solved to determine a value for R_1 based on the other parameters under worst-case, low-system voltage and worst-case low ambient temperature conditions as follows:

$$R_1 = \frac{V_S \text{ low} - V_{CE}(sat)(Q_1) - V_{BE}(Q_0) - R_2(I_c + I_b)}{I_b + \dfrac{R_2}{R_3}(I_c + I_b) + \dfrac{V_{BE}(Q_0)}{R_3}}$$

or it may be solved to determine the I_b drive to Q_0 available or supplied under similar worst-case conditions, as follows:

$$I_b = \frac{V_S \text{ low} - V_{CE}(sat)(Q_1) - I_c\left(R_2 + \dfrac{R_1 R_2}{R_3}\right)}{R_1 + R_2 + \dfrac{R_1 R_2}{R_3}} - \frac{V_{BE}(Q_0)\left(1 + \dfrac{R_1}{R_3}\right)}{R_1 + R_2 + \dfrac{R_1 \times R_2}{R_3}}$$

Where,

$V_{CE}(sat)(Q_1)$ = maximum voltage drop across the driver transistor at low ambient temperature extremes

and,

$V_{BE}(Q_0)$ = base-to-emitter voltage drop across Q_0 with Q_0 current equal to I_c

Fig. 366 - Alternate ignition circuit.

Fig. 367 - Ignition circuit with collector-coupled drive transistor.

with,

$V_{CE} = V_{CE}(sat)(Q_0)$ and T_A = low ambient-temperature extreme.

The equation for I_b shows the tradeoff between I_b and V_{BE} such that any combination of values of V_{BE} and I_b which result in a value of device base current equal to or less than that given by the equation for I_b will provide acceptable performance.

The maximum power dissipation in R_1 will be approximately:

$$\text{Max. } P_{R1} = \frac{[V_S \text{ high} - V_{BE}(Q_0) - V_{CE}(sat)(Q_1)]^2}{R_1} D_{max}$$

when,

V_S high is the worst-case high system voltage

and,

D_{max} is maximum duty factor-typically .80 to .90 which occurs at high engine speed.

In an alternate circuit configuration, shown in Fig. 366, the n-p-n drive transistor Q_1 is replaced by a p-n-p device. This circuit offers the possibility of providing acceptable performance at lower system voltages than can be provided by the circuit of Fig. 365 because the stacking of V_{BE} voltage drops in the drive

chain has been reduced. (Note the logic level, output vs. input, has been inverted in this circuit.)

Another popular drive circuit, shown in Fig. 367, employs a collector-coupled drive transistor as opposed to the emitter-follower drive shown in Fig. 365. The basic drive circuit relationship in this configuration is:

$$V_S = I_b(R_1+R_4+R_2)+I_cR_2+V_{BE}(Q_0)$$

and,

$$R_1 = \frac{V_S \text{ low}-V_{BE}(Q_0)-I_cR_2}{I_b} -R_4-R_2$$

and I_b (available or supplied with given circuit values) is:

$$I_b = \frac{V_S \text{ low}-I_cR_2}{R_1+R_2+R_4} - V_{BE}(Q_0)\ \frac{1}{R_1+R_2+R_4}$$

R_4 must be large enough to allow the zener clamp circuit to turn Q_0 on in the high-voltage clamp condition without exceeding the current capability of the zener circuit.

$$\text{then } R_2 \text{ Min} \cong \frac{V_{BE}(Q_0) - V_{CE}(\text{sat})(Q_1)}{I_{ZZ}}$$

where I_{ZZ} is the maximum permissible zener current which may be diverted through R_4. (A portion of the total zener current must be used to supply drive to turn Q_0 on during clamp conditions.) A value of 5 ohms for R_2 is usually suitable.

The maximum current which Q_1 must handle is:

$$I_{Q1}(\text{max}) \cong \frac{V_S \text{ high}}{R_1}$$

Where V_S is the highest voltage which will provide acceptable system performance.

The maximum power dissipation in R_1 is:

$$P_{R1}(\text{max}) \cong \frac{(V_S \text{ high})^2}{R_1}$$

Suitable component parameters for a transistor ignition system are given below:

R_1=34 Ω (Fig. 365); 60 Ω (Fig. 366)
R_3=75 Ω
R_2=0.05 Ω
R_L=0.5 Ω at 25° C (0.411 Ω at –30° C)
R_4=5 Ω (Fig. 366)
I_c=5 A
V_S low=5.5 V
V_S high=18 V
$V_{CE}(\text{sat})(Q_1) \le 0.5$ V

$V_{CE}(\text{sat}) \le 3$ V at T_A=–30° C
I_c=5 A
I_b=0.05 A
$V_{BE} \le 2$ V at T_A=–30° C
I_c=5 A
V_{CE}=3 V
and $I_b \le 0.136-V_{BE}\times0.043$ (Fig. 365)
$I_b \le 0.08-V_{BE}\times0.015$ (Fig. 366)

An Automotive Breakerless Ignition System Using a Power Darlington and an Integrated Circuit Control

A breakerless system consists of a distributor with a contactless pick-up, an electronic control unit, and an ignition coil. Operation of the circuit shown in Fig. 368 is based on the accurate amplitude-modulation of a resonant-circuit oscillator in which the inductor acts as the sensor. When the conductive material of a toothed, metallic trigger wheel in the distributor enters the field of the sensor (L), eddy current losses in the non-magnetic wheel-tooth reduce the Q of the resonant circuit and decrease the amplitude of oscillations to a specific level at which discrete transistor Q_a interrupts the coil current. When the oscillator amplitude has decreased below the switching level, a variable-feedback system in the integrated circuit maintains a minimum amplitude of oscillation. This lower amplitude level eliminates timing variations which would occur if the oscillator had to be restarted by random noise. Therefore, either transition may be used to control event timing. The system performance is comparatively independent of dQ/dt; i.e., pulse amplitude and noise immunity are maintained over a wide range of rotor (engine) speeds. In a typical automotive application, capacitor C2 parallel-resonates the circuit at a frequency between 200 and 400 kHz.

An output circuit produces a switching signal ϕ at terminal 4 and its complement $\overline{\phi}$ at terminals 6 and 7; signal ϕ is high in response to a high oscillator state. When ϕ is high, the Darlington transistor is driven by base current supplied via resistors R_1 and R_g, so that current flows through the primary winding of the ignition coil. The peak coil current is limited by a "current-setting" transistor Q_a, in response to the voltage-drop developed across current-sampling resistor, R_h.

A spark is generated when ϕ goes low and $\overline{\phi}$ high. Switching is initiated by a low signal at terminal 4; the signal turns transistors Q_b and
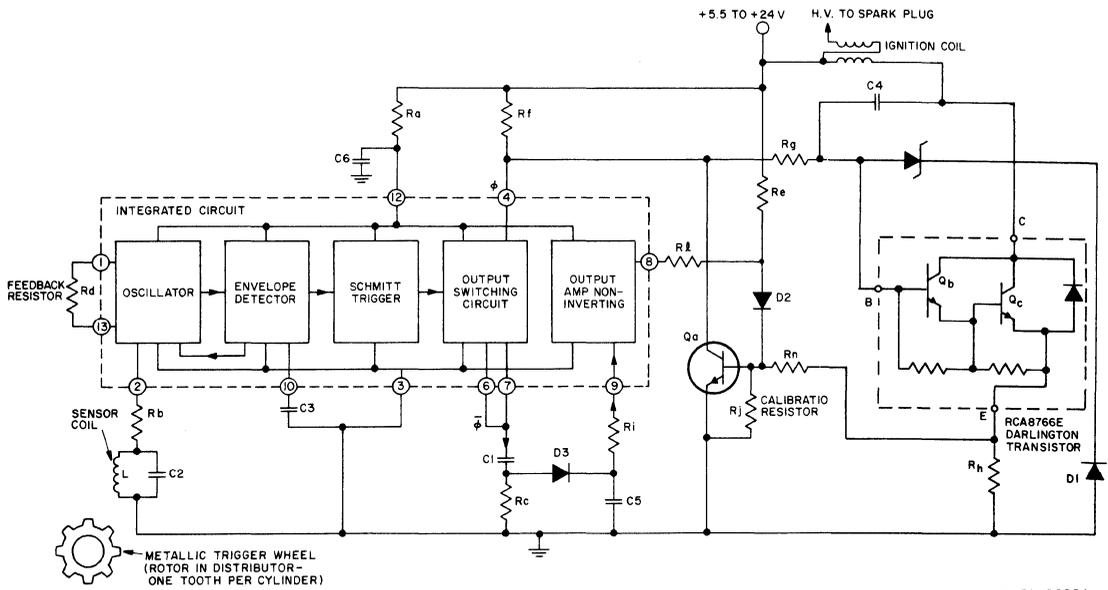
Fig. 368 - *Block diagram of the breakerless ignition system.*
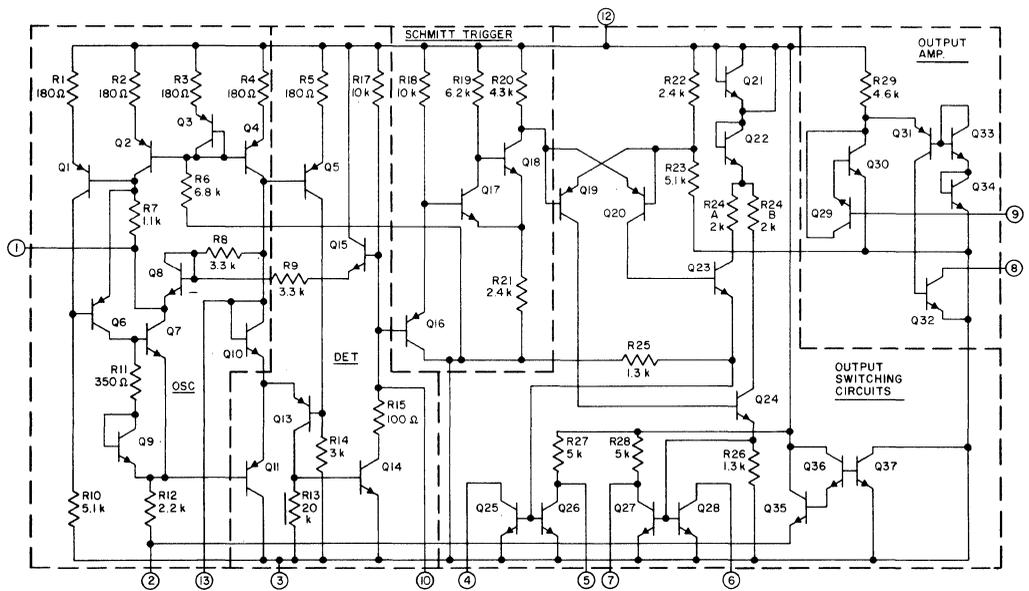
Fig. 369 - *Schematic diagram of the integrated circuit.*

Q_c off. When the current flowing through the coil primary is interrupted, its stored energy is transferred to the secondary circuit where it produces a high voltage that fires a spark plug. Diode D1 protects Q_b and Q_c against excessive negative voltages and the application of reverse battery voltage. Although noise produced by the spark is suppressed to meet the applicable standards, an additional circuit consisting of C_1, R_c, D_3, C_5, R_1, and the output amplifier in the integrated circuit assures that noise will not affect the switching.

Description of the Integrated Circuit

The block diagram of the integrated circuit is shown in Fig. 368. Fig. 369 shows the schematic diagram. The 0.063 × 0.075-inch chip, is contained in a 14-lead dual-in-line plastic package.

The basic oscillator is of the tuned collector type, with emitter feedback. It comprises transistors Q6, Q7, Q11, associated current-sources, and external integrated circuit. Transistors Q13 and Q14 constitute an active envelope detector. The auxiliary feedback circuitry mentioned above consists of diode-connected Q8, R9, and R8: it is actuated when the output of the detector goes high as the oscillator amplitude decreases. In the low-amplitude state when diode-connected Q8 is turned on, additional feedback is provided to the oscillator through resistor R8.

The Schmitt trigger circuit utilizes transistors Q16, Q17, Q18 and resistors R19, R20, and R21. It is isolated from the envelope detector by transistor Q16 and current-limiting resistor R18. The two threshold voltages are developed across resistor R21; the high threshold voltage is developed when Q18 is driven to saturation.

Transistors Q19 and Q20 develop signals with 180° phase difference; transistor Q20 controls the ϕ-signal at terminal 4, and Q19 controls the $\overline{\phi}$-signal at terminals 6 and 7. Transistors Q29, Q30, and Q32, the active transistors in the output amplifier, provide the noise immunity feature described above.

Since terminal 2 leads into the distributor, it it is imperative that protection against spurious transients which might otherwise damage the integrated circuit be provided. A degree of transient attenuation is supplied by resistor R_b, Fig. 368. Additional protection is provided on-chip by transistors Q35, Q36, and Q37.

High-Reliability Power Transistors

Power transistors classified as high-reliability types have come to be primarily associated with military and aerospace applications. In many ways, this association is misleading because the commercial equipment market is probably the largest user of high-reliability products, but not necessarily by that label. Military and aerospace agencies, however, have been largely responsible for establishment of comprehensive published reliability specifications and standards which have been accepted by the solid-state industry. MIL standards dominate the procedures used to specifiy high-reliability solid-state devices and represent a common reference point frequently used by commercial users to define their requirements.

Military and aerospace requirements for high-reliability solid-state devices are extremely large and diverse, not only in terms of performance, operating conditions, and reliability, but also in terms of logistics and procurement. As a result of these requirements, the military services have jointly developed specifications and standards under which most military end-use solid-state devices are procured. To simplify procurement, logistics, and the development of reliability data, MIL specs are not issued for the full spectrum of devices manufactured; rather, they are restricted to those devices for which significant need is demonstrated and are specified so that the device can have as wide applicability as possible. Although the limits for operating conditions may exceed those required for some applications, they simplify procurement and assure a supply of devices for the majority of military equipment.

SPECIFICATIONS AND STANDARDS

There are two major military specifications used for the procurement of standard solid-state devices by the military. These specifications are MIL-S-19500, which covers devices such as discrete transistors, thyristors, and diodes, and MIL-M-38510, which covers microcircuits, both hybrid and monolithic.

MIL-S-19500 is the specification for the familiar "JAN" devices. Detailed electrical specifications are prepared as needed by the three military services and coordinated by the Defense Electronic Supply Center. At present, approximately six hundred detailed electrical specifications are included in the MIL-S-19500 system.

JAN AND JANTX
POWER TRANSISTORS

Table XXX shows the wide product line of JAN and JANTX military-specification solid-state power transistors available from RCA for high-reliability applications in military, aerospace, and critical industrial usage. These power transistors are processed in accordance with the MIL-S-19500 general specifications. MIL-STD-750 test methods are used as required by the individual military detail specification. This table lists the individual MIL-S-19500 specification number for each family of devices.

Four levels of product assurance requirements, JAN, JANTX, JANTXV, and JANS are defined in Military Specification MIL-S-19500. Devices designated as JAN types receive electrical testing only. JANTX devices receive 100 percent screening such as bake, temperature cycling, acceleration, hermetic seal, high-temperature reverse bias, and power burn-in. JANTXV types receive JANTX testing but with criterial visual inspection prior to sealing the` package. JANS level types receive JANTXV testing plus manufacturing certification, process controls and wafer lot acceptance with electrical testing using larger sample sizes with tighter acceptance criteria.

The Defense Electronics Supply Center (DESC) maintains a Qualified Products List

(QPL-19500) of all device types and the manufacturers qualified to supply these devices in accordance with MIL-S-19500. This list is updated periodically and is available to designers and manufacturers of military equipment.

DESC military standard MIL-STD-701 of standard semiconductor devices lists the preferred JANTXV, JANTX, and JAN types for military equipment designers and manufacturers.

NASA military standard MIL-STD-975 of standard semiconductor devices lists the preferred JANS and JANTXV types for flight and mission-essential ground-support equipment.

MIL-STD-750 is the military standard specification of test methods for discrete solid state devices.

RCA NON-JAN TYPE POWER TRANSISTORS

Many power transistors are not covered by military specifications, either because they are too new or are not used in sufficient quantities. Many of these devices offer the most recent technological advances or have special performance characteristics which offer advantages to the designer of high-reliability equipment. RCA cooperates with the users of such devices in establishment of high-reliability specifications patterned after MIL standards, which allow these designs to be approved for use in military and aerospace systems, as well as commercial equipment. If the use warrants, these specifications may be submitted by RCA, or the user, to the cognizant military specification agency as candidates for MIL approval as a standard type.

Table XXX - RCA JAN and JANTX Solid-State Power Devices

Parent Type	Military Specification Type	MIL-S-19500/* Specification
POWER TRANSISTORS		
Hometaxial-Base Types		
2N1479	JAN2N1479	207
2N1480	JAN2N1480	207
2N1481	JAN2N1481	207
2N1482	JAN2N1482	207
2N1487	JAN2N1487	208
2N1488	JAN2N1488	208
2N1489	JAN2N1489	208
2N1490	JAN2N1490	208
2N3055	JAN2N3055, JANTX2N3055	407
2N3441	JAN2N3441, JANTX2N3441	369
2N3442	JAN2N3442, JANTX2N3442	370
2N3771	JAN2N3771, JANTX2N3771	413
2N3772	JAN2N3772, JANTX2N3772	413
Epitaxial-Base Types		
2N5302	JAN2N5302, JANTX2N5302	456
2N5303	JAN2N5303, JANTX2N5303	456
High-Current Darlington Types		
2N6283	JAN2N6283, JANTX2N2683	504
2N6284	JAN2N6284, JANTX2N6284	504
2N6383	JAN2N6383, JANTX2N6383	523
2N6384	JAN2N6384, JANTX2N6384	523
2N6385	JAN2N6385, JANTX2N6385	523
2N6648	JAN2N6648, JANTX2N6648	527
2N6649	JAN2N6649, JANTX2N6649	527
2N6650	JAN2N6650, JANTX2N6650	527

Table XXX (Cont'd)

Parent Type	Military Specification Type	MIL-S-19500/* Specification
POWER TRANSISTORS		
High-Voltage Types		
2N3439	JAN2N3439, JANTX2N3439	368
2N3440	JAN2N3440, JANTX2N3440	368
2N3584	JAN2N3584, JANTX2N3584	384
2N3585	JAN2N3585, JANTX2N3585	384
2N5415S	JAN2N5415S, JANTX2N5415S	485
2N5416S	JAN2N5416S, JANTX2N5416S	485
2N6211	JAN2N6211, JANTX2N6211	461
2N6212	JAN2N6212, JANTX2N6212	461
2N6213	JAN2N6213, JANTX2N6213	461
2N6306	JAN2N6306, JANTX2N6306	498
2N6308	JAN2N6308, JANTX2N6308	498
2N6546	JAN2N6546, JANTX2N6546	525
2N6671	JAN2N6671, JANTX2N6671	536
2N6673	JAN2N6673, JANTX2N6673	536
2N6674	JAN2N6674, JANTX2N6674	537
2N6675	JAN2N6675, JANTX2N6675	537
2N6676	JAN2N6676, JANTX2N6676	538
2N6678	JAN2N6678, JANTX2N6678	538
High-Speed Types		
2N3879	JAN2N3879, JANTX2N3879	526
2N5038	JAN2N5038, JANTX2N5038	439
2N5039	JAN2N5039, JANTX2N5039	439
2N5671	JAN2N5671, JANTX2N5671	488
2N5672	JAN2N5672, JANTX2N5672	488
2N6032	JAN2N6032, JANTX2N6032	528
2N6033	JAN2N6033, JANTX2N6033	528

*MIL-S-19500 specifications can be obtained from the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, Pa. 19120.

Most procurements of solid-state devices for military systems are made by the equipment contractor from the MIL-STD parts list as awards are received for electronic equipment. Some military and aerospace programs, because of their size, duration, or special requirements (Minuteman and Apollo are two examples), require that special specifications and process methods, or even special production lines, be established and tailored to the particular functional, reliability, and economic needs of the program. RCA Solid State Division has frequently used the resources of its laboratories, production facilities, and expert technical staff to contribute to the success of such programs.

All RCA high-reliability solid-state power devices are processed in accordance with the provisions of MIL-S-19500. These provisions include the following items:

1. A clearly defined procedure for the conversion of a customer specification

into an RCA internal specification with built-in safeguards to assure the customer that the delivered parts meet or exceed his specification requirements.

2. A formalized personnel training and testing program which assures that each operation is performed correctly.

3. A complete inspection of incoming materials, utilities, and work in process using on-site facilities such as scanning-electron-microscope and X-ray equipment.

4. Maintenance of cleanliness in work areas.

5. Rigorous control over changes in design materials, and processes with documentation kept in active files for a minimum of three years.

6. Tool and test equipment maintenance and calibration in strict accordance with MIL-C-45662, "Calibration System Requirements."

7. A quality-assurance program in accordance with MIL-Q-9858, "Quality Program Requirements."

For detailed information on the **Lot Sampling** plans used for RCA high-reliability solid-state power devices, as defined by MIL-S-19500 and MIL-STD-105D, refer to **RCA Power Devices DATABOOK**, SSD-220 Series.

In addition to JAN and JANTX types, high-reliability selections of all RCA power transistors can be obtained on a custom basis. Such power transistors are subjected to high-reliability preconditioning and screening in accordance with the Group A, B, and C Sampling Tests as specified in MIL-STD-750 or special customer requirements. These power transistors can be supplied to four basic reliability levels shown in Fig. 370. Level 3 devices are equivalent to JANTX devices. For RCA Level 4 devices, the preconditioning consists of burn-in only. Fig. 371 shows the processing requirements specified by MIL-S-19500 for JAN and JANTX solid-state power devices.
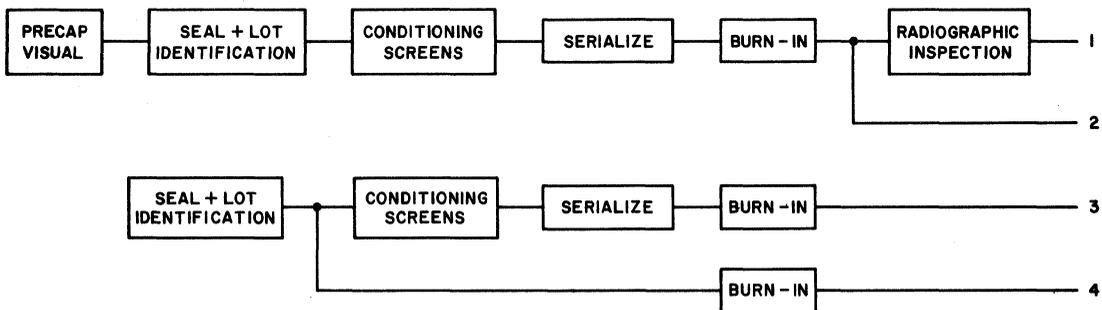
92CM-22891

Fig. 370 - Process-flow chart for four reliability levels of RCA high-reliability power transistors.

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┌─────────────────────────┐   ┌─────────────────────┐
│ Production Process      │   │ Precap              │
│ 1  Raw Material         │   │ Visual              │
│ 2  Factory Processing   │   │ For JANTXV          │
│                         │   │ Types               │
└─────────────────────────┘   └─────────────────────┘
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| Production Process 1 Raw Material 2 Factory Processing | Precap Visual For JANTXV Types |

Inspection Lots Formed at Final Assembly Operation (Sealing)

Lots Proposed for JAN Types (Non-TX)

Inspection Tests to Verify LTPD Group A[1] Group B[2] Group C[3]

Review of Group A, B, And C Data For Accept or Reject

Lots Proposed For JANTX And JANTXV Types

Preparation For Delivery JAN

100 Percent Process Conditioning[4]
1 High Temp Storage
2 Thermal Shock
3 Acceleration
4 Hermetic Seal Tests
5 Reverse Bias

100 Percent Power Conditioning[4]
1 Measurement of Specified Parameters
2 Burn-In
3 Measurement of Specified Parameters To Determine Delta And Other Rejects
4 Lot Rejection Criteria Based on Rejects From Burn-In Test

Inspection Tests To Verify LTPD Group A[1] Group B[2] Group C[3]

Review of Group A, B and C Data For Lot Accept Or Reject

1   Group A Electrical Performance Tests Performed On a Lot Sample Basis
2   Group B Environmental, Mechanical and Lift Tests (Storage and Operating) Performed on a Lot Sample Basis
3   Group C Environmental and Life Tests Performed on a Time Period Basis
4   Tests shall be Performed in the Order as Shown

Preparation for Delivery JANTX And JANTXV

92CM-25057

Fig. 371 - Order of procedure diagram for JAN and JANTX solid-state power devices.

Radiation-Hardened
Power Transistors

Solid-state devices intended for use in applications such as space satellites or military-weapons systems must be able to survive various types of radiation without significant changes in performance characteristics. The damaging types of radiation most likely to be encountered include neutron bombardment, gamma rays, flash x-rays, and electromagnetic pulses (EMP).

TYPES OF RADIATION

Neutron radiation can be particularly harmful to discrete or monolithic bipolar transistors. Fast-neutron bombardment can cause displacement of atoms from the silicon crystal lattice of a transistor; these atoms trap out charge carriers and increase the recombination rate of charge-carrier pairs. As a result, the lifetime of minority carriers in the transistor base region is shortened (causing a decrease in current gain), the collector series resistance rises (causing higher collector saturation voltage), and transistor leakage currents increase. Current gain is affected most rapidly and most critically, and is the chief cause of failure in devices exposed to neutron radiation.

Because neutron displacement damage results primarily in a shortening of minority-carrier life-time, its effect is minimal on MOS transistors (both discrete and monolithic) because they are majority-carrier types.

Gamma rays produce large numbers of hole-electron pairs in solid-state devices. When these charge-carrier pairs recombine, they generate a current (called a "photocurrent") which may be large enough at high gamma dose rates to turn on a transistor. The photocurrent then experiences a step-function increase as a result of the transistor gain. The increased current (or secondary photocurrent), which may exceed device ratings, lasts for a period equal to the gamma-ray exposure time plus the turn-off time of the transistor.

Photocurrents produced by gamma-ray ionization can cause latch-up, circuit ringing, or junction breakdown in all types of transistors.

Flash x-rays and electromagnetic pulses produced by a nuclear explosion can cause permanent physical damage to any type of solid-state device. Flash x-rays generate a thermomechanical shock that propagates through the dense material (molybdenum, gold, or copper) used for lead connections and for bonding the pellet to the header. At high energy levels (above 10 kev), the shock wave can be strong enough to fracture the pellet.

Electromagnetic-pulse (EMP) radiation can induce extremely high voltage pulses in the cables used to interconnect electrical equipment. If these voltage pulses exceed the junction-breakdown capability of a solid-state device, they can cause junction avalanching and result in device destruction.

The effects of flash x-rays and EMP radiation cannot be overcome by any changes in device design and processing, but must be treated as system-design problems. The chief weapons used to prevent x-ray or EMP damage are the traditional methods used to combat any RFI: shielding and line-filtering.

RADIATION-HARDENING TECHNIQUES

RCA offers a variety of bipolar silicon power transistors in which special design and processing techniques are used to assure continued functional performance after exposure to specified dosages of neutron and gamma radiation.

Neutron-Radiation Compensation—In RCA radiation-resistant power transistors, the base width is made as narrow as possible (consistent with other design objectives) to achieve a minimum base transit time so that a maximum number of minority carriers can complete the journey through the base. The

narrower base width thus compensates for the major cause of failure in transistors exposed to neutron radiation, the reduction in minority-carrier lifetime and the corresponding decrease in transistor current gain. The voltage-supporting region in the collector is also made as narrow as feasible and is heavily doped. In this way, the series-resistance path is made as low as possible to compensate for the rise in collector series resistance and the resulting higher saturation voltage caused by exposure of the transistor to neutron radiation.

The problem of increased leakage currents is solved by use of epitaxial-planar transistors. The initial leakage in these transistors is so small that even the higher levels caused by neutron bombardment are unlikely to cause failure.

Because the narrower base width and reduced collector resistivity used to improve transistor radiation resistance are contra-dictory to the design requirement for high-voltage, high-energy transistors, designers should adjust circuits to require the minimum possible emitter-to-collector voltage-break-down capability. In addition, ratings for transistors should be specified in accordance with the way in which the devices are to be used (i.e., V_{CER} or V_{CEV}, and never V_{CEO}). The circuit design should also provide high-energy protection for the transistor.

Gamma-Radiation Compensation—The gamma dose rate at which the onset of secondary photocurrent occurs depends strongly on the geometry of the transistor emitter. The secondary photocurrent is ini-tiated when a portion of the emitter-base junction becomes forward-biased because of the voltage drop across the lateral base resistance under the emitter. In RCA radiation-resistant transistors, the distance from the base contact to the farthest point of the base under the emitter is reduced to the minimum possible value to achieve a substantial increase in the gamma threshold level at which the secondary photocurrent starts. Table XXXI shows RCA's radiation-hardened power tran-sistors.

Table XXXI - RCA Radiation-Hardened Power Transistors

Parent Type	Military Specification Type	MIL-S-19500/ Specification
Epitaxial-Base Types		
2N6248		—
High-Speed Types		
2N3879	JAN2N3879, JANTX2N3879	526
2N5038	JAN2N5038, JANTX2N5038	439
2N5320		—
2N5322		—
2N5672	JAN2N5672, JANTX2N5672	488
2N6480		—
High-Voltage Types		
2N6673		536
2N6688		—

Appendix A
Power Transistor Product Matrix
Hometaxial-Base (Single-Diffused) N-P-N Types

$I_C$max. = 1.5 A $f_T$typ. = 1.5 MHz TO-205MA/TO-5	$I_C$max. = 3 A $f_T$typ. = 0.8 MHz TO-213MA/TO-66	$I_C$max. = 3 A $f_T$typ. = 0.8 MHz TO-220	$I_C$max. = 4 A $f_T$typ. = 1 MHz TO-213MA/TO-66	$I_C$max. = 4 A $f_T$typ. = 1 MHz TO-220	$I_C$max. = 7 A $f_T$typ. = 1 MHz TO-220
2N1482 Family	2N3441 Family	2N6478 Family	2N3054 Family	2N5298 Family	2N5496 Family
2N1479 V_{CEO} = 40 V h_{FE} = 20-60 @ 0.2 A P_T = 5 W	2N6263 V_{CEO} = 120 V h_{FE} = 20-100 @ 0.5 A P_T = 20 W	RCA3441 V_{CEO} = 120 V h_{FE} = 20-150 @ 0.5 A P_T = 36 W	BDX24 40250 V_{CEO} = 40 V h_{FE} = 25-100 @ 1.5 A P_T = 29 W	2N5296 V_{CEO} = 40 V h_{FE} = 30-120 @ 1 A P_T = 36 W	2N5490 V_{CEO} = 40 V h_{FE} = 20-100 @ 2 A P_T = 50 W
2N1482 V_{CEO} = 55 V h_{FE} = 35-100 @ 0.2 A P_T = 5 W	2N3441 V_{CEO} = 140 V h_{FE} = 25-100 @ 0.5 A P_T = 25 W	2N6477 V_{CEO} = 120 V h_{FE} = 25-150 @ 1 A P_T = 50 W	2N3054 V_{CEO} = 55 V h_{FE} = 25-150 @ 0.5 A P_T = 25 W	2N5298 V_{CEO} = 60 V h_{FE} = 20-80 @ 1.5 A P_T = 36 W	2N5492 V_{CEO} = 55 V h_{FE} = 20-100 @ 2.5 A P_T = 50 W
40348 V_{CEO} = 65 V h_{FE} = 30-125 @ 0.3 A P_T = 8.75 W	2N6264 V_{CEO} = 150 V h_{FE} = 20-60 @ 1 A P_T = 50 W	2N6478 V_{CEO} = 140 V h_{FE} = 25-150 @ 1 A P_T = 50 W	2N6261 V_{CEO} = 80 V h_{FE} = 25-100 @ 1.5 A P_T = 50 W	2N5294 V_{CEO} = 70 V h_{FE} = 30-120 @ 0.5 A P_T = 36 W	2N5496 V_{CEO} = 70 V h_{FE} = 20-100 @ 3.5 A P_T = 50 W

$I_C$max. = 10 A $f_T$typ. = 0.4 MHz TO-204MA/TO-3	$I_C$max. = 15 A $f_T$typ. = 1.5 MHz TO-204MA/TO-3	$I_C$max. = 16 A $f_T$typ. = 0.7 MHz TO-204MA/TO-3	$I_C$max. = 16 A $f_T$typ. = 1.5 MHz TO-220	$I_C$max. = 30 A $f_T$typ. = 1.5 MHz TO-204MA/TO-3
2N3442 Family	2N3055 Family	2N3773 Family	2N6103 Family	2N3772 Family
2N4347 V_{CEO} = 120 V h_{FE} = 15-60 @ 2 A P_T = 100 W	2N6371 V_{CEO} = 40 V h_{FE} = 15-60 @ 8 A P_T = 117 W	2N4348 V_{CEO} = 120 V h_{FE} = 15-60 @ 5 A P_T = 120 W	2N6103 V_{CEO} = 40 V h_{FE} = 15-60 @ 8 A P_T = 75 W	2N3771 V_{CEO} = 40 V h_{FE} = 15-60 @ 15 A P_T = 150 W
2N3442 V_{CEO} = 140 V h_{FE} = 20-70 @ 3 A P_T = 117 W	BD182 2N3055 V_{CEO} = 60 V h_{FE} = 20-70 @ 4 A P_T = 115 W	BDY37 2N3773 V_{CEO} = 140 V h_{FE} = 15-60 @ 8 A P_T = 150 W	2N6099 V_{CEO} = 60 V h_{FE} = 20-80 @ 4 A P_T = 75 W	2N3772 V_{CEO} = 60 V h_{FE} = 15-60 @ 10 A P_T = 150 W
2N6262 V_{CEO} = 150 V h_{FE} = 20-70 @ 3 A P_T = 150 W	2N6254 V_{CEO} = 80 V h_{FE} = 20-70 @ 5 A P_T = 150 W	2N6259 V_{CEO} = 150 V h_{FE} = 15-60 @ 8 A P_T = 250 W	2N6101 V_{CEO} = 70 V h_{FE} = 20-80 @ 5 A P_T = 75 W	RCS258 V_{CEO} = 60 V h_{FE} = 15-60 @ 10 A P_T = 250 W

Power Transistor Product Matrix (Cont'd)
Epitaxial-Base N-P-N and P-N-P Types

$I_C$max. = -3.5 A $f_T$typ. = 20 MHz TO-205MA/TO-5	$I_C$max. = 6 A $f_T$typ. = 8 MHz TO-213MA/TO-66	$I_C$max. = -6 A $f_T$typ. = 10 MHz TO-213MA/TO-66	$I_C$max. = 7 A $f_T$typ. = 8 MHz TO-220	$I_C$max. = -7 A $f_T$typ. = 10 MHz TO-220	$I_C$max. = 15 A $f_T$typ. = 6 MHz TO-204MA/TO-3	$I_C$max. = 15 A $f_T$typ. = 8 MHz TO-204MA/TO-3
2N5783 Family P-N-P	2N6374 Family N-P-N	2N5954 Family P-N-P	2N6292 Family N-P-N	2N6107 Family P-N-P	2N3716 Family N-P-N	2N6472 Family N-P-N
2N5783 V_{CEO} = -40 V h_{FE} = 20-100 @ -1.6 A P_T = 10 W	2N6374 V_{CEO} = 40 V h_{FE} = 20-100 @ 3 A P_T = 40 W	2N5956 V_{CEO} = -40 V h_{FE} = 20-100 @ -3 A P_T = 40 W	2N6292 V_{CEO} = 70 V h_{FE} = 30-150 @ 2 A P_T = 40 W	2N6111 V_{CEO} = -30 V h_{FE} = 30-150 @ -3 A P_T = 40 W	2N6569 V_{CEO} = 40 V h_{FE} = 15-120 @ 4 A P_T = 100 W	2N6470 V_{CEO} = 40 V h_{FE} = 20-150 @ 5 A P_T = 125 W
2N5782 V_{CEO} = -50 V h_{FE} = 20-100 @ -1.2 A P_T = 10 W	2N6372 V_{CEO} = 80 V h_{FE} = 20-100 @ 2 A P_T = 40 W	2N5954 V_{CEO} = -80 V h_{FE} = 20-100 @ -2 A P_T = 40 W	2N6473 V_{CEO} = 100 V h_{FE} = 15-150 @ 1.5 A P_T = 40 W	2N6107 V_{CEO} = -70 V h_{FE} = 30-150 @ -2 A P_T = 40 W	2N3055 V_{CEO} = 60 V h_{FE} = 20-70 @ 4 A P_T = 115 W	2N6471 V_{CEO} = 60 V h_{FE} = 20-150 @ 5 A P_T = 125 W
2N5781 V_{CEO} = -65 V h_{FE} = 20-100 @ -1 A P_T = 10 W	2N6465 V_{CEO} = 80 V h_{FE} = 15-150 @ 1.5 A P_T = 40 W	2N6467 V_{CEO} = -100 V h_{FE} = 15-150 @ -1.5 A P_T = 40 W	2N6474 V_{CEO} = 120 V h_{FE} = 15-150 @ 1.5 A P_T = 40 W	2N6475 V_{CEO} = -100 V h_{FE} = 15-150 @ -1.5 A P_T = 40 W	2N3716 V_{CEO} = 80 V h_{FE} = 30 @ 3 A P_T = 150 W	2N6472 V_{CEO} = 80 V h_{FE} = 20-150 @ 5 A P_T = 125 W
	2N6466 V_{CEO} = 120 V h_{FE} = 15-150 @ 1.5 A P_T = 40 W	2N6468 V_{CEO} = -120 V h_{FE} = 15-150 @ -1.5 A P_T = 40 W		2N6476 V_{CEO} = -120 V h_{FE} = 15-150 @ -1.5 A P_T = 40 W	2N5878 V_{CEO} = 80 V h_{FE} = 20-100 @ 4 A P_T = 150 W	

$I_C$max. = -15 A $f_T$typ. = 16 MHz TO-204MA/TO-3	$I_C$max. = 15 A $f_T$typ. = 8 MHz TO-220	$I_C$max. = -15 A $f_T$typ. = 8 MHz TO-220	$I_C$max. = 20 A $f_T$typ. = 4 MHz TO-204MA/TO-3	$I_C$max. = -20 A $f_T$typ. = 4 MHz TO-204MA/TO-3	$I_C$max. = 30 A $f_T$typ. = 8 MHz TO-204MA/TO-3
2N6247 Family P-N-P	2N6488 Family N-P-N	2N6491 Family P-N-P	RCA8638 Family N-P-N	RCA9116 Family P-N-P	2N5303 Family N-P-N
2N6594 V_{CEO} = -40 V h_{FE} = 15-200 @ -4 A P_T = 100 W	2N6486 V_{CEO} = 40 V h_{FE} = 20-150 @ 5 A P_T = 75 W	2N6489 V_{CEO} = -40 V h_{FE} = 20-150 @ -5 A P_T = 75 W	RCA8638E V_{CEO} = 100 V h_{FE} = 10-100 @ 7.5 A P_T = 200 W	RCA9116E V_{CEO} = -100 V h_{FE} = 10-100 @ -7.5 A P_T = 200 W	2N5301 V_{CEO} = 40 V h_{FE} = 15-60 @ 15 A P_T = 200 W
2N5875 V_{CEO} = -60 V h_{FE} = 20-100 @ -4 A P_T = 150 W	2N6487 V_{CEO} = 60 V h_{FE} = 20-150 @ 5 A P_T = 75 W	2N6490 V_{CEO} = -60 V h_{FE} = 20-150 @ -5 A P_T = 75 W	RCA3773 V_{CEO} = 140 V h_{FE} = 15-60 @ 8 A P_T = 150 W	2N6609 V_{CEO} = -140 V h_{FE} = 15-60 @ -8 A P_T = 150 W	2N5302 V_{CEO} = 60 V h_{FE} = 15-60 @ 15 A P_T = 200 W
2N5880 V_{CEO} = -80 V h_{FE} = 20-100 @ -6 A P_T = 160 W	2N6488 V_{CEO} = 80 V h_{FE} = 25-150 @ 5 A P_T = 75 W	2N6491 V_{CEO} = -80 V h_{FE} = 20-150 @ -5 A P_T = 75 W	RCA8638C V_{CEO} = 140 V h_{FE} = 25-150 @ 5 A P_T = 200 W	RCA9116C V_{CEO} = -140 V h_{FE} = 25-150 @ -5 A P_T = 200 W	2N5303 V_{CEO} = 80 V h_{FE} = 15-60 @ 10 A P_T = 200 W
2N6248 V_{CEO} = -100 V h_{FE} = 20-100 @ -5 A P_T = 125 W			MJ15003 V_{CEO} = 140 V h_{FE} = 25-150 @ 5 A P_T = 250 W	MJ15004 V_{CEO} = -140 V h_{FE} = 25-150 @ -5 A P_T = 250 W	

Power Transistor Product Matrix (Cont'd)
High-Voltage, High-Speed-Switching N-P-N Types

SwitchMax Transistor Classification Chart

Ic(sat)		1A	4A	5A	5A	6A	8A	10A	15A	25A
VCEV	260 V	—	—	—	—	—	—	—	—	2N6686
	280 V	—	—	—	—	—	—	—	—	2N6687
	300 V	—	—	—	—	—	—	—	—	2N6688*
		2N6771†	—	2N6671‡	—	—	—	2N6674‡	2N6676‡	—
	450 V	BUW40†	—	2N6738†	—	—	—	—	2N6774	—
		—	—	BUW41†	—	—	—	—	—	—
		2N6772†	—	2N6672	—	—	—	—	2N6677	—
	550 V	BUW40A†	—	2N6739†	—	—	—	—	2N6775	—
		—	—	BUW41A†	—	—	—	—	—	—
		2N6773†	—	2N6673‡	—	—	—	2N6675‡	2N6678‡	—
	650 V	BUW40B†	—	2N6740†	—	—	—	—	2N6776	—
		—	—	BUW41B†	—	—	—	—	—	—
	800 V	—	BUX31	—	2N6751	BUX32	BUX33	—	—	—
	850 V	—	—	—	2N6752	—	—	—	—	—
	900 V	—	BUX31A	—	2N6753	BUX32A	BUX33A	—	—	—
	1000 V	—	BUX31B	—	2N6754	BUX32B	BUX33B	—	—	—
Characteristics	Temp., Tc	Limits								
ICEV (max)	25°C	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.1 mA	0.05 mA
at VCE = VCEV	100°C	—	1 mA	—	1 mA	1 mA	1 mA	2 mA	1 mA	—
	125°C	1 mA	—	1 mA	—	—	—	—	—	0.5 mA
VCE(sat) (max)	25°C	1 V	1 V	1 V	1 V	1 V	1 V	1 V	1 V	1.5 V
at Ic (sat)	100°C	—	1.5 V	—	1.5 V	1.5 V	1.5 V	2 V	2 V	—
	125°C	2 V	—	2 V	—	—	—	—	—	1.5 V
t_f (max)	25°C	0.2 µs	0.45 µs	0.5 µs	0.45 µs	0.45 µs	0.45 µs	0.6 µs	0.6 µs	0.35 µs
at Ic (sat)	100°C	—	0.6 µs	—	0.6 µs	0.6 µs	0.6 µs	1 µs	1 µs	—
	125°C	0.5 µs	—	0.8 µs	—	—	—	—	—	0.6 µs
t_s (max)	25°C	2.5 µs	3 µs	2.5 µs	3 µs	3 µs	3 µs	2.5 µs	2.5 µs	0.8 µs
at Ic (sat)	100°C	—	4 µs	—	4 µs	4 µs	4 µs	4 µs	4 µs	—
	125°C	4.5 µs	—	4 µs	—	—	—	—	—	2.5 µs
t_r (max)	25°C	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.5 µs	0.5 µs	0.5 µs
at Ic (sat)	100°C	—	0.7 µs	—	0.7 µs	0.7 µs	0.7 µs	1 µs	1 µs	—
	125°C	1.3 µs	—	0.8 µs	—	—	—	—	—	0.8 µs
t_c (max)	25°C	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.4 µs	0.5 µs	0.5 µs	0.5 µs
at Io (sat)	100°C	—	0.8 µs	—	0.8 µs	0.8 µs	0.8 µs	0.8 µs	0.8 µs	—
	125°C	1.3 µs	—	0.8 µs	—	—	—	—	—	0.8 µs

All SwitchMax transistors are supplied in JEDEC TO-204MA/TO-3 packages, except as noted below: *Ic(sat) = 20A
†Supplied in JEDEC TO-220AB plastic package.   ‡MIL Approved:
MIL-S-19500/536 — 2N6671, 2N6673
MIL-S-19500/537 — 2N6674, 2N6675
MIL-S-19500/538 — 2N6676, 2N6678

Power Transistor Product Matrix (Cont'd)
High-Speed-Switching N-P-N and P-N-P Types

$I_C$max. = 1 A $f_T$typ. = 100 MHz TO-205MD/TO-39	$I_C$max. = -1 A $f_T$typ. = 100 MHz TO-205MD/TO-39	$I_C$max. = 2 A $f_T$typ. = 75 MHz TO-205MD/TO-39	$I_C$max. = -2 A $f_T$typ. = 75 MHz TO-205MD/TO-39	$I_C$max. = 7 A $f_T$typ. = 100 MHz TO-213MA/TO-66
2N2102 Family N-P-N	2N4036 Family P-N-P	2N5320 Family N-P-N	2N5322 Family P-N-P	2N3879 Family N-P-N
2N3053 V_{CEO} = 40 V h_{FE} = 50-250 @ 0.15 A P_T = 5 W	2N4037 V_{CEO} = -40 V h_{FE} = 50-250 @ -0.15 A P_T = 7 W	2N5321 V_{CEO} = 50 V h_{FE} = 40-250 @ 0.5 A P_T = 10 W	2N5323 V_{CEO} = -50 V h_{FE} = 40-250 @ -0.5 A P_T = 10 W	2N5202 V_{CEO} = 50 V h_{FE} = 10-100 @ 4 A P_T = 35 W
2N2270 V_{CEO} = 45 V h_{FE} = 50-200 @ 0.15 A P_T = 5 W	2N4036 V_{CEO} = -65 V h_{FE} = 40-140 @ -0.15 A P_T = 7 W	2N5320 V_{CEO} = 75 V h_{FE} = 30-130 @ 0.5 A P_T = 10 W	2N5322 V_{CEO} = -75 V h_{FE} = 30-130 @ -0.5 A P_T = 10 W	2N3878 V_{CEO} = 50 V h_{FE} = 20 min. @ 4 A P_T = 35 W
2N2102 V_{CEO} = 65 V h_{FE} = 40-120 @ 0.15 A P_T = 5 W	2N4314 V_{CEO} = -65 V h_{FE} = 50-250 @ -0.15 A P_T = 7 W			2N3879 V_{CEO} = 75 V h_{FE} = 20-80 @ 4 A P_T = 35 W
2N2405 V_{CEO} = 90 V h_{FE} = 60-200 @ 0.15 A P_T = 5 W				2N6500 V_{CEO} = 90 V h_{FE} = 15-60 @ 3 A P_T = 35 W

$I_C$max. = 7 A $f_T$typ. = 100 MHz TO-220	$I_C$max. = 12 A $f_T$typ. = 150 MHz Radial Pkg.	$I_C$max. = 20 A $f_T$typ. = 90 MHz TO-204MA/TO-3	$I_C$max. = 25 A $f_T$typ. = 50 MHz TO-204MA/TO-3	$I_C$max. = 30 A $f_T$typ. = 100 MHz TO-204MA/TO-3	$I_C$max. = 50 A $f_T$typ. = 100 MHz Modified TO-3
2N6704 Family N-P-N	2N6480 Family N-P-N	2N5038 Family N-P-N	2N6688 Family N-P-N	2N5671 Family N-P-N	2N6033 Family N-P-N
BUW64A 2N6702 V_{CEO} = 90 V h_{FE} = 20 min. @ 5 A P_T = 50 W	2N6479 V_{CEO} = 60 V h_{FE} = 20-300 @ 12 A P_T = 87 W	2N5039 V_{CEO} = 75 V h_{FE} = 20-100 @ 10 A P_T = 140 W	2N6686 V_{CEO} = 160 V h_{FE} = 15 min. @ 25 A P_T = 200 W	2N5671 V_{CEO} = 120 V h_{FE} = 20 min. @ 20 A P_T = 140 W	2N6032 V_{CEO} = 90 V h_{FE} = 10-50 @ 50 A P_T = 140 W
BUW64B 2N6703 V_{CEO} = 110 V h_{FE} = 20 min. @ 5 A P_T = 50 W	2N6480 V_{CEO} = 80 V h_{FE} = 20-300 @ 12 A P_T = 87 W	2N5038 V_{CEO} = 90 V h_{FE} = 20-100 @ 12 A P_T = 140 W	2N6687 V_{CEO} = 180 V h_{FE} = 15 min. @ 25 A P_T = 200 W	2N5672 V_{CEO} = 90 V h_{FE} = 20 min. @ 20 A P_T = 140 W	2N6033 V_{CEO} = 120 V h_{FE} = 10-50 @ 40 A P_T = 140 W
BUW64C 2N6704 V_{CEO} = 130 V h_{FE} = 20 min. @ 5 A P_T = 50 W		2N6354 V_{CEO} = 120 V h_{FE} = 10-100 @ 10 A P_T = 140 W	2N6688 V_{CEO} = 200 V h_{FE} = 15 min. @ 25 A P_T = 200 W		

Power Transistor Product Matrix (Cont'd)
High-Voltage N-P-N and P-N-P Types

$I_C$max. = 1A $f_T$typ. = 25 MHz TO-205MD/TO-39	$I_C$max. = -1 A $f_T$typ. = 35 MHz TO-205MD/TO-39	$I_C$max. = 5 A $f_T$typ. = 25 MHz TO-213MA/TO-66	$I_C$max. = -5 A $f_T$typ. = 30 MHz TO-213MA/TO-66	$I_C$max. = 5 A $f_T$typ. = 5 MHz TO-204MA/TO-3	$I_C$max. = 7 A $f_T$typ. = 7 MHz TO-213MA/TO-66
2N3439 Family N-P-N	2N5415 Family P-N-P	2N3585 Family N-P-N	2N6213 Family P-N-P	2N5240 Family N-P-N	2N6079 Family N-P-N
40346 V_{CER} = 175 V h_{FE} = 25 @ 10 mA P_T = 10 W	RCA1A16 V_{CEO} = -100 V h_{FE} = 40-250 @ -10 mA P_T = 10 W	2N3583 V_{CEO} = 175 V h_{FE} = 40-200 @ 0.75 A P_T = 35 W	2N6211 V_{CEO} = -225 V h_{FE} = 10-100 @ -1 A P_T = 35 W	2N5239 V_{CEO} = 225 V h_{FE} = 20-80 @ 2 A P_T = 100 W	2N6078 V_{CEO} = 250 V h_{FE} = 12-70 @ 1.2 A P_T = 45 W
2N3440 V_{CEO} = 250 V h_{FE} = 40-160 @ 20 mA P_T = 10 W	2N5415 V_{CEO} = -200 V h_{FE} = 35-150 @ -50 mA P_T = 10 W	2N3584 V_{CEO} = 250 V h_{FE} = 25-100 @ 1 A P_T = 35 W	2N6213 V_{CEO} = -350 V h_{FE} = 10-100 @ -1 A P_T = 35 W	2N5240 V_{CEO} = 300 V h_{FE} = 20-80 @ 2 A P_T = 100 W	2N6077 V_{CEO} = 275 V h_{FE} = 12-70 @ 2 A P_T = 45 W
2N3439 V_{CEO} = 350 V h_{FE} = 40-160 @ 20 mA P_T = 10 W	2N5416 V_{CEO} = -300 V h_{FE} = 30-120 @ -50 mA P_T = 10 W	2N3585 V_{CEO} = 300 V h_{FE} = 25-100 @ 1 A P_T = 35 W	2N6214 V_{CEO} = -400 V h_{FE} = 10-100 @ -1 A P_T = 35 W	2N5840 V_{CEO} = 350 V h_{FE} = 10-50 @ 2 A P_T = 100 W	2N6079 V_{CEO} = 350 V h_{FE} = 12-50 @ 1.2 A P_T = 45 W

$I_C$max. = 7 A $f_T$typ. = 2 MHz TO-204MA/TO-3	$I_C$max. = 8 A $f_T$typ. = 15 MHz TO-204MA/TO-3	$I_C$max. = 10 A $f_T$typ. = 20 MHz TO-204MA/TO-3
2N6510 Family N-P-N	2N6308 Family N-P-N	RCA8766 Family N-P-N
2N6510 V_{CEO} = 200 V h_{FE} = 10-50 @ 3 A P_T = 120 W	2N6306 V_{CEO} = 250 V h_{FE} = 15-75 @ 3 A P_T = 125 W	RCA8766 V_{CEO} = 350 V h_{FE} = 100 @ 6 A P_T = 150 W
2N6514 V_{CEO} = 300 V h_{FE} = 10-50 @ 5 A P_T = 120 W	2N6307 V_{CEO} = 300 V h_{FE} = 15-75 @ 3 A P_T = 125 W	RCA8766B V_{CEO} = 400 V h_{FE} = 100 @ 6 A P_T = 150 W
2N6513 V_{CEO} = 350 V h_{FE} = 10-50 @ 4 A P_T = 120 W	2N6308 V_{CEO} = 350 V h_{FE} = 12-60 @ 3 A P_T = 125 W	RCA8766D V_{CEO} = 450 V h_{FE} = 100 @ 6 A P_T = 150 W

Power Transistor Product Matrix (Cont'd)
Monolithic Darlington N-P-N and P-N-P Types

$I_C$max. = 2 A $f_T$typ. = 25 MHz TO-220	$I_C$max. = -2 A $f_T$typ. = 25 MHz TO-220	$I_C$max. = 4 A $f_T$typ. = 10 MHz TO-220	$I_C$max. = 4 A $f_T$typ. = 10 MHz TO-220	$I_C$max. = 5 A $f_T$typ. = 10 MHz TO-220	$I_C$max. = -10 A $f_T$typ. = 40 MHz TO-220	$I_C$max. = 10 A $f_T$typ. = 60 MHz TO-220
TIP112 Family N-P-N	TIP117 Family P-N-P	RCA9202C Family N-P-N	RCA9203C Family N-P-N	RCA9201C Family N-P-N	2N6668 Family P-N-P	2N6388 Family N-P-N
TIP110 V_{CEO} = 60 V h_{FE} = 500 @ 2 A P_T = 50 W	TIP115 V_{CEO} = -60 V h_{FE} = 500 @ -2 A P_T = 50 W	RCA9202A V_{CEO} = 300 V h_{FE} = 500 @ 4 A P_T = 65 W	RCA9203A V_{CEO} = 250 V h_{FE} = 100 @ 4 A P_T = 50 W	RCA9201A V_{CEO} = 150 V h_{FE} = 500 @ 5 A P_T = 65 W	2N6666 V_{CEO} = -40 V h_{FE} = 1k-20k @ -3 A P_T = 65 W	2N6386 V_{CEO} = 40 V h_{FE} = 1k-20k @ 3 A P_T = 65 W
TIP111 V_{CEO} = 80 V h_{FE} = 500 @ 2 A P_T = 50 W	TIP116 V_{CEO} = -80 V h_{FE} = 500 @ -2 A P_T = 50 W	RCA9202B V_{CEO} = 350 V h_{FE} = 500 @ 4 A P_T = 65 W	RCA9203B V_{CEO} = 300 V h_{FE} = 100 @ 4 A P_T = 50 W	RCA9201B V_{CEO} = 200 V h_{FE} = 500 @ 5 A P_T = 65 W	2N6667 V_{CEO} = -60 V h_{FE} = 1k-20k @ -5 A P_T = 65 W	2N6387 V_{CEO} = 60 V h_{FE} = 1k-20k @ 5 A P_T = 65 W
TIP112 V_{CEO} = 100 V h_{FE} = 500 @ 2 A P_T = 50 W	TIP117 V_{CEO} = -100 V h_{FE} = 500 @ -2 A P_T = 50 W	RCA9202C V_{CEO} = 400 V h_{FE} = 250 @ 4 A P_T = 65 W	RCA9203C V_{CEO} = 350 V h_{FE} = 100 @ 4 A P_T = 50 W	RCA9201C V_{CEO} = 250 V h_{FE} = 250 @ 5 A P_T = 65 W	2N6668 V_{CEO} = -80 V h_{FE} = 1k-20k @ -5 A P_T = 65 W	2N6388 V_{CEO} = 80 V h_{FE} = 1k-20k @ 5 A P_T = 65 W
						2N6533 V_{CEO} = 120 V h_{FE} = 1k-20k @ 3 A P_T = 65 W

$I_C$max. = 10 A $f_T$typ. = 60 MHz TO-204MA/TO-3	$I_C$max. = -10 A $f_T$typ. = 40 MHz TO-204MA/TO-3	$I_C$max. = 10 A $f_T$typ. = 20 MHz TO-204MA/TO-3	$I_C$max. = 20 A $f_T$typ. = 15 MHz TO-204MA/TO-3	$I_C$max. = -20 A $f_T$typ. = 50 MHz TO-204MA/TO-3	$I_C$max. = 50 A $f_T$typ. = 5 MHz TO-3 (mod)	$I_C$max. = -50 A $f_T$typ. = 5 MHz TO-3 (mod)
2N6385 Family N-P-N	2N6650 Family P-N-P	RCA8766 Family N-P-N	2N6284 Family N-P-N	2N6287 Family P-N-P	RCA9228 Family N-P-N	RCA9229 Family P-N-P
2N6055 V_{CEO} = 60 V h_{FE} = 0.75k-18k @ 4 A P_T = 100 W	2N6648 V_{CEO} = -40 V h_{FE} = 1k-20k @ -5 A P_T = 70 W	RCA8766 V_{CEO} = 350 V h_{FE} = 100 @ 6 A P_T = 150 W	2N6282 V_{CEO} = 60 V h_{FE} = 0.75k-18k @ 10 A P_T = 160 W	2N6285 V_{CEO} = -60 V h_{FE} = 0.75k-18k @ -10 A P_T = 160 W	RCA9228A V_{CEO} = 60 V h_{FE} = 2000 @ 25 A P_T = 300 W	RCA9229A V_{CEO} = -60 V h_{FE} = 2000 @ -25 A P_T = 300 W
2N6383 V_{CEO} = 40 V h_{FE} = 1k-20k @ 5 A P_T = 100 W	2N6649 V_{CEO} = -60 V h_{FE} = 1k-20k @ -5 A P_T = 70 W	RCA8766B V_{CEO} = 400 V h_{FE} = 100 @ 6 A P_T = 150 W	2N6283 V_{CEO} = 80 V h_{FE} = 0.75k-18k @ 10 A P_T = 160 W	2N6286 V_{CEO} = -80 V h_{FE} = 0.75k-18k @ -10 A P_T = 160 W	RCA9228B V_{CEO} = 80 V h_{FE} = 2000 @ 25 A P_T = 300 W	RCA9229B V_{CEO} = -80 V h_{FE} = 2000 @ -25 A P_T = 300 W
2N6385 V_{CEO} = 80 V h_{FE} = 1k-20k @ 5 A P_T = 100 W	2N6650 V_{CEO} = -80 V h_{FE} = 1k-20k @ -5 A P_T = 70 W	RCA8766D V_{CEO} = 450 V h_{FE} = 100 @ 6 A P_T = 150 W	2N6284 V_{CEO} = 100 V h_{FE} = 0.75k-18k @ 10 A P_T = 160 W	2N6287 V_{CEO} = -100 V h_{FE} = 0.75k-18k @ -10 A P_T = 160 W	RCA9228C V_{CEO} = 100 V h_{FE} = 2000 @ 25 A P_T = 300 W	RCA9229C V_{CEO} = -100 V h_{FE} = 2000 @ -25 A P_T = 300 W
2N6578 V_{CEO} = 120 V h_{FE} = 2k-20k @ 4 A P_T = 120 W						

Appendix B

Terms and Symbols

General

AQL	acceptance quality level
CM	cross modulation
IMD	intermodulation distortion
K	post-radiation neutron-damage constant
LTPD	lot tolerance per cent defective
MTBF	mean time between failures
MTTF	mean time to failure
NF	noise factor (or noise figure)
P_D	device dissipation
pps	pulses per second
P_{rr}	pulse repetition rate
prt	pulse recurrence time
PW	pulse width
RMS	root mean square
$R_{\theta JA}$	thermal resistance, junction-to-ambient
$R_{\theta JC}$	thermal resistance, junction-to-case
$R_{\theta JF}$	thermal resistance, junction-to-flange
$R_{\theta JFA}$	thermal resistance, junction-to-free air
$R_{\theta JHS}$	thermal resistance, junction-to-heat sink
T_A	ambient temperature
T_C	case temperature
THD	total harmonic distortion
T_J	operating (junction) temperature
T_L	lead temperature during soldering
t_p	pulse duration
T_{stg}	storage temperature
η	efficiency
θ	conduction angle
ϕ	phase angle
ϕL	lead radius (for bending)
τ	torque
τ_s	device stud torque

Power Transistors

(C)	collector-to-base charge-generation constant (during gamma exposure)
$C_{b'c}$	feedback capacitance
C_c	collector-to-case capacitance
C_{cb}	collector-to-base feedback capacitance
C_{ib}	common-base input capacitance
C_{ob}	common-base output capacitance
C_{obo}	open-circuit common-base output capacitance

$E_{S/b}$	reverse-bias second-breakdown energy
$f_{\alpha b}$	base (alpha) cutoff frequency
$f_{\alpha e}$	emitter (beta) cutoff frequency
h_{FE}	dc forward-current transfer ratio
h_{fe}	common-emitter, small-signal, short-circuit, forward-current transfer ratio
$|h_{fe}|$	magnitude of common-emitter, small-signal, short-circuit, forward-current transfer ratio
f_{hfe}	common-emitter, small-signal, short-circuit forward-current transfer ratio cutoff frequency
f_T	gain-bandwidth product (unity-gain frequency for devices in which gain roll off has a −1 slope)
G_c	conversion gain
G_{pb}	small-signal, common-base power gain
G_{PB}	large-signal, common-base power gain
G_{pe}	small-signal, common-emitter power gain
G_{PE}	large-signal, common-emitter power gain
G_{VE}	wide-band voltage gain
h_{ib}	common-base, small-signal, short-circuit input impedance
h_{ie}	common-emitter, small-signal, short-circuit input impedance
h_{ob}	common-base, small-signal, open circuit output admittance
h_{rb}	common-base, small-signal, open-circuit reverse-voltage transfer ratio
I_B	continuous base current
I_{BEV}	base-cutoff current with specified voltage between collector and emitter
I_{BM}	peak base current
I_C	continuous collector current
I_{CBO}	collector-cutoff current, emitter open
I_{CEO}	collector-cutoff current, base open
I_{CER}	collector-cutoff current with specified resistance between base and emitter
I_{CES}	collector-cutoff current with base-emitter junction short-circuited

Terms and Symbols (Cont'd)

Power Transistors (Cont'd)

I_{CEV}	collector-cutoff current with specified voltage between base and emitter
I_{CEX}	collector-cutoff current with specified circuit between base and emitter
I_{CM}	peak collector current
$I_C(sat)$	collector current at which h_{FE}, $V_{BE}(sat)$, $V_{CE}(sat)$, and switching speeds are measured
I_E	continuous emitter current
I_{EBO}	emitter-cutoff current, collector open
I_{EM}	peak emitter current
$I_{S/b}$	forward-bias, second-breakdown collector current
P_G	power gain
PRT	power rating test
P_T	transistor dissipation at specified temperature
$r_{bb'}$	base spreading resistance
R_{BB}	base bias resistor
$r_{b'}C_c$	collector-to-base time constant
R_{BE}	external base-to-emitter resistance
R_c	collector resistor
$r_{CE}(sat)$	dc collector-to-emitter saturation resistance
$Re\ (h_{ie})$	real part of common-emitter, small-signal, short-circuit input impedance
R_s	collector-to-emitter saturation resistance
t_c	clamped turn-off switching time of an inductive load
t_d	delay time
t_f	fall time
t_{OFF}	turn-off time (storage time + fall time)
t_{ON}	turn-on time (delay time + rise time)
t_r	rise time
t_s	storage time
T_{VI}	clamped inductive turn-off time
V_{BB}	base supply voltage
V_{BE}	base-to-emitter voltage
$V_{BE}(sat)$	base-to-emitter saturation voltage
$V_{(BR)CBO}$	collector-to-base breakdown voltage, emitter open
$V_{(BR)CEO}$	collector-to-emitter breakdown voltage, base open
$V_{(BR)CEV}$	collector-to-emitter breakdown voltage with specified voltage between base and emitter
$V_{(BR)CEX}$	collector-to-emitter breakdown voltage with specified circuit between base and emitter
$V_{(BR)EBO}$	emitter-to-base breakdown voltage, collector open
V_{CB}	collector-to-base voltage
V_{CBO}	collector-to-base voltage, emitter open
V_{CC}	collector supply voltage
V_{CE}	collector-to-emitter voltage
V_{CEO}	collector-to-emitter voltage, base open
$V_{CE}(sat)$	collector-to-emitter saturation voltage
$V_{CEO}(sus)$	collector-to-emitter sustaining voltage, base open
V_{CER}	collector-to-emitter voltage with specified resistance between base and emitter
$V_{CER}(sus)$	collector-to-emitter sustaining voltage with specified resistance between base and emitter
V_{CES}	collector-to-emitter voltage with base-emitter junction short-circuited
V_{CEV}	collector-to-emitter voltage with specified voltage between base and emitter
$V_{CEV}(sus)$	collector-to-emitter sustaining voltage with specified voltage between base and emitter
V_{CEX}	collector-to-emitter voltage with specified circuit between base and emitter
$V_{CEX}(sus)$	collector-to-emitter sustaining voltage with specified circuit between base and emitter
V_{EB}	emitter-to-base voltage
V_{EBO}	emitter-to-base voltage, collector open
V_F	diode forward-voltage drop
V_{RT}	collector-to-emitter reach through (or punch through) voltage
α	common-base current gain (alpha)
β	collector-emitter current gain (beta)
η_C	collector efficiency
τ_l	thermal time constant

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Tennessee
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Knoxville, TN 37919
Tel: (615) 588-2467

Texas
RCA Center
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Town No. Plaza, Suite 121
Dallas, TX 75234
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Virginia
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Tel: (703) 558-4161

Canada

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Quebec
RCA Inc.
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St. Anne-de-Bellevue,
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Ontario
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Ontario M9W 1L3
Tel: (416) 247-5491

Europe

Belgium
RCA S.A.
Mercure Centre, Rue de la
Fusee 100, 1130 Bruxelles
Tel: 02/720.89.80

France
RCA S.A.
2-4 Avenue de L'Europe
78140 Velizy
Tel: (3) 946.56.56

Germany
RCA GmbH
Pfingstrosenstrasse 29,
8000 Munchen 70
West Germany
Tel: 089/7143047-49

RCA GmbH
Justus-von-Liebig-Ring 10
2085 Quickborn
West Germany
Tel: 04106/613-0

RCA GmbH
Zeppelinstrasse 35,
7302 Ostfildern 4 (Kemnat)
West Germany
Tel: 0711/454001-04

Italy
RCA SpA
Piazza San Marco 1
20121 Milano
Tel: (02) 65.97.048-051

Sweden
RCA International LTD
Box 3047, Hagalundsgatan 8
171 03 Solna 3
Tel: 08/83 42 25

U.K.
RCA LTD
Lincoln Way, Windmill Road
Sunbury-on-Thames
Middlesex TW16 7HW
Tel: 093 27 85511

Asia Pacific

Hong Kong
RCA International, Ltd.
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Tsimshatsui, Kowloon
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Taiwan
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7th Floor, 97
Nanking East Road, Section 2
Taipei
Tel: (02) 521-8537

Latin America

Argentina
Ramiro E. Podetti Reps.
Lavalle 357
3rd Floor, Office No. 24
1047 Buenos Aires
Tel: 393-3919

Brazil
RCA Solid State Limitada
Av. Brig Faria Lima 1476
7th Floor, Sao Paulo 01452
Tel: 210-4033

Mexico
RCA S.A. de C.V./
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Postal 17-570, Mexico 16, D.F.
Tel: (905) 399-7228

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CSR Electronics
7272-E2 Arcadia Ci. N.W.
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Suite 110
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Tel: (516) 422-2500

North Carolina
CSR Electronics
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Suite 305
Raleigh, NC 27609
Tel: (919) 787-2137

Ohio
Lyons Corporation
4812 Frederick Road
Suite 101
Dayton, OH 45414
Tel: (513) 278-0714

Lyons Corporation
4615 W. Streetsboro Road
Richfield, OH 44286
Tel: (216) 659-9224

South Carolina
CSR Electronics
1506 Winding Way
So. Carolina
Taylors, SC 29687
Tel: (803) 292-2388

Texas
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Suite 218-6
Austin, TX 78752
Tel: (512) 452-9459

Southern States Marketing
9730 Townpark Drive #105
Houston, TX 77036
Tel: (713) 988-0991

Southern States Marketing
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Tel: (214) 238-7500

Utah
Simpson Assocs.
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