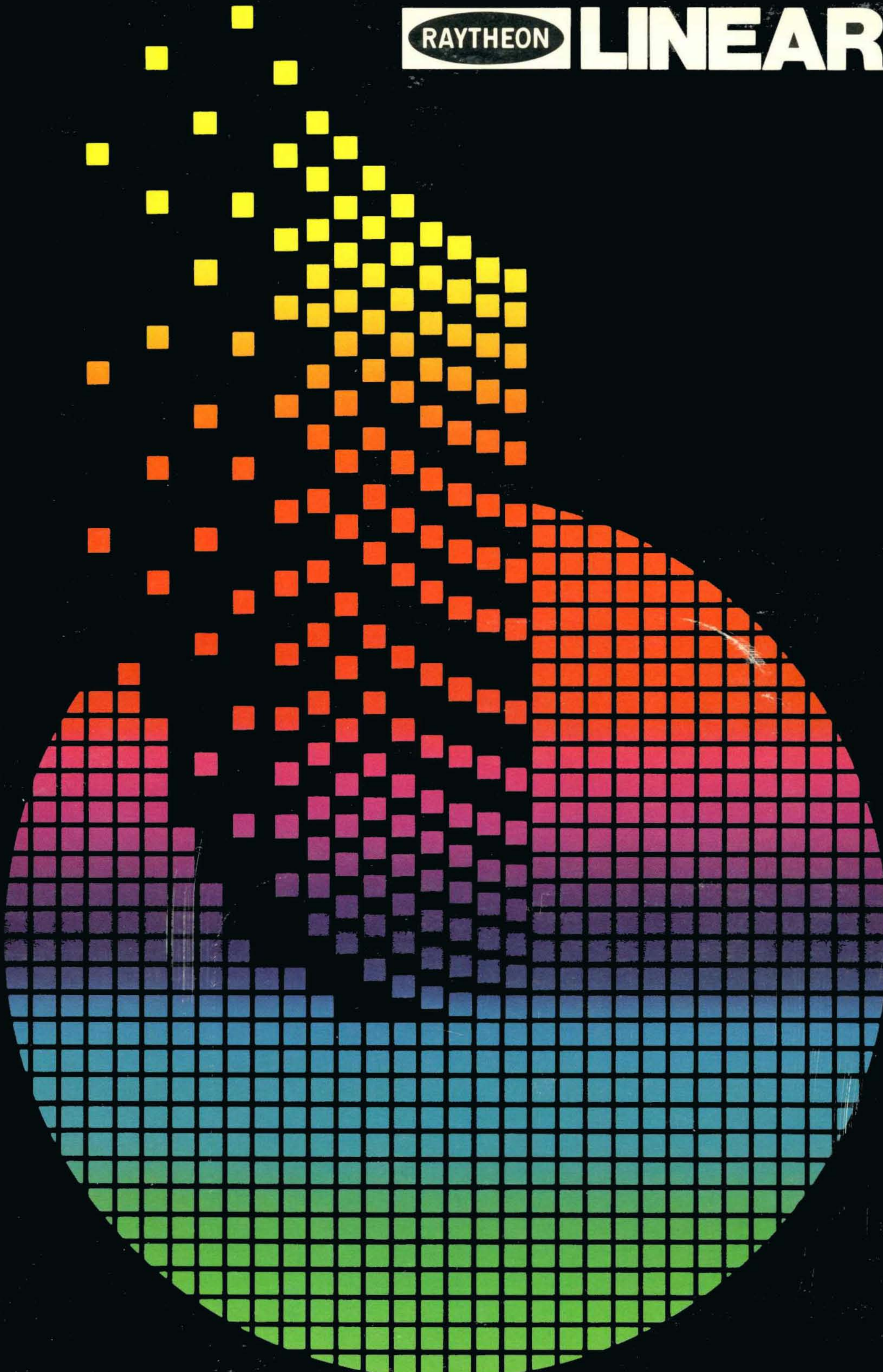
RAYTHEON LINEAR



RAYTHEON LINEAR

LINEAR INTEGRATED CIRCUIT DATA BOOK

RAYTHEON

SEMICONDUCTOR DIVISION

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**Wideband, low noise version

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***Plastic mini-dip

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*Dual replacement
**Wideband, low-noise version

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Dual Operational Amplifier Summary

	SYMBOL	RM/RC747			RM1537/RC1437			RM1558/RC1458			LH2101A/2301A			UNIT
Maximum Ratings Supply Voltage Range	V_{CC}	±3 to ±22/±18*			±3 to ±18			±3 to ±22/±18*			±3 to ±22/±18*			V
Differential Input Voltage	V_{ID}	±30			±5			±30			±30			V
Input Voltage		±15			±10			±15			±15			V
Power Dissipation	P_D	500			500			500			500			mW
Electrical Characteristics	@ 25°C	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Test Conditions	V_{CC}		±15			±15			±15			**		V
Input Offset Voltage	V_{ID}		1.0 2.0*	5.0 6.0*		1.0	5.0 7.5*		1.0 2.0*	5.0 6.0*			2.0 7.5*	mV
Input Offset Current	I_{IO}		30	200		50	200/500*		30	200			10/50*	nA
Input Bias Current	I_{IB}		200	500		0.2/0.4	0.5/1.5*		200	500			75/250*	nA
Input Common Mode Voltage Range	V_{ICR}	±12	±13		±8	±10		±12	±13		±15/±12*			V
Supply Current	I_D		3.3	5.6		5	7.5		3.3	5.6			2.5	mA
Open Loop Voltage Gain	A_{VOL}	50	200		25/15*	45	70	50	200		25/15*			V/mV
Output Voltage Swing	V_{OR}	±12	±14		±12	±14		±12	±14		±12			V
Common Mode Rejection Ratio	CMRR	70	90		70/65*	90		70	90		80/70*			dB
Power Supply Rejection Ratio	PSSR		30	150			150 200*		30	150	80/70* dB		150	µV/V
Unity Gain Bandwidth	BW		0.8						0.8					MHz
Slew Rate	SR		0.5						0.5					V/µs
Channel Separation			-98			-90			-98					dB
Noise Voltage	V_N													nV/(Hz)½
Operating Temperature Range	T_A	-55 0	RM RC	125 70	-55 0	RM RC	125 70	-55 0	RM RC	125 70	-55 -25 0	2101A 2201A 2301A	+125 +85 +70	°C
Package: Hermetic TO-5		TF						TE						
Hermetic Dip		DC			DC			DE			DC			
Plastic Dip		DB			DB			NB						

**Note: Specifications apply ±5 ⩽ V_{CC} ⩽ ±20V and over temperature.
*Commercial temp range device.

	SYMBOL	RM/RC4558			RM/RC4559			RC4739			UNIT
Maximum Ratings Supply Voltage Range	V_{CC}	±4 to ±18			±4 to ±18			±4 to ±18			V
Differential Input Voltage	V_{ID}	±30			±30			±30			V
Input Voltage		±15			±15			±15			V
Power Dissipation	P_D	500			500			500			mW
Electrical Characteristics	@ 25°C	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Test Conditions	V_{CC}		±15			±15			±15		V
Input Offset Voltage	V_{IO}		1.0 2.0*	5.0 6.0*		1.0 2.0*	5.0 6.0*		2.0	6.0	mV
Input Offset Current	I_{IO}		5.0	200		5.0	200		5.0	200	nA
Input Bias Current	I_{IB}		40/200*	500		40/200*	500		40	500	nA
Input Common Mode Voltage Range	V_{ICR}	±12	±14		±12	±14		±12	±14		V
Supply Current	I_D		3.5	5.6		3.5	5.6		3.5	5.6	mA
Open Loop Voltage Gain	A_{VOL}	50/20*	300		50/20*	300		20	300		V/mV
Output Voltage Swing	V_{OR}	±12	±14		±12	±14		±12	±14		V
Common Mode Rejection Ratio	CMRR	70	100		70	100		70	100		dB
Power Supply Rejection Ratio	PSSR		10	150		10	150		10	150	μV/V
Unity Gain Bandwidth	BW	2.5/2.0*	3.0		3	4			3.0		MHz
Slew Rate	SR		0.5		1.5	2.0			1.0		V/μs
Channel Separation			-90			-90			-125		dB
Noise Voltage	V_N		10		2.0†	1.4†			2.5†		nV/(Hz)½
Operating Temperature Range	T_A	-55 0	RM RC	+125 70	-55 0	RM RC	+125 70	0		70	°C
Package: Hermetic TO-5		TE			TE						
Hermetic Dip		DE			DE						
Plastic Dip		NB			NB			DB			

*Commercial temp range device.
†Broad Band noise voltage -20 Hz to 20 kHz (μV_{RMS}).

Quad Operational Amplifier Summary

	SYMBOL	RM4136/RC4136			LM124/LM224/LM324			LM2902			RM3503A/ RV3403A/RC3403A			LM2900/LM3900			RV3301/RC3401			UNIT
Maximum Ratings Supply Voltage Range	V_{CC}		±4 to ±22/±18*			+3 or ±1.5 to +32 or ±16			+3 or ±1.5 to +32 or ±16			+2.5 or ±1.25 to +36 or ±18			+4 or ±2 to +36 or ±18			+4 to +28/+18*		V
Differential Input Voltage	V_{ID}		±30			32			26			36								V
Input Voltage			±15			32			26			36								V
Power Dissipation	P_D		800			900			570			650			570			625		mW
Electrical Characteristics	@25°C	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Test Condition V_{CC}:			±15			+5			+5			±15			+15			±15		V
Input Offset Voltage	V_{IO}		0.5 0.5	4.0 6.0*		2	5 7*		2	7		2	4 5*							mV
Input Offset Current	I_{IO}		5	150 200*		±3 ±3	±30 ±50*		5	50		±30	±50							nA
Input Bias Current	I_{IB}		40	400 500*			150 250*		45	500		150	200		30	200		50	300	nA
Input Common Mode Voltage Range	V_{ICR}	±12	±14			35			35		−15		+13							V
Supply Current	I_D		7	11.3		0.8	2		0.8	2		3	4/5*		6.2	10		6.9	10	mA
Open Loop Voltage Gain	A_{VOL}	50 20*	300		50 25*	100			100		50 25*	100		1.2	2.8		1	2		V/mV
Output Voltage Swing	V_{OR}	±12	±14		0		V^+−1.5	0		V^+−1.5	±13	±14		13.5	14.2		13.5	14.2		V
Common Mode Rejection Ratio	CMRR	70	100		70 65*	85		50	70		80	90								dB
Power Supply Rejection Ratio	PSRR		10 µV/V	150 µV/V	65 dB	100 dB		50 dB	100 dB			20 µV/V	45 µV/V 100 µV/V*		70 dB			55 dB		
Unity Gain Bandwidth	BW		3									2.0			2.5			5.0		MHz
Slew Rate	SR		1.5 1.0*			0.3						1.2			0.5			0.6		V/µs
Output Sink Current	I_{sink}				10	20		10	20		10	20		0.5	1.3		0.5	1.0		mA
Output Source Current	I_{source}				20	40		20	40		20	40		6	18		5.0	10		mA
Channel Separation			−90			−120			−120			−120						−65		dB
Operating Temperature Range		−55 −40 0	RM RC RV	+125 +70 +85	−55 −25 0	LM124 LM224 LM324	+125 +85 +70	−40		+85	−55 −40 0	RM RV RC	+125 +85 +70	−40 0	2900 3900	+85 +70	−40 0	3301 3401	+85 +75	°C
Package: 14 pin Dip	Hermetic		DC			DC						DC								
	Plastic		DB			DB			DB			DB			DB			DB		

*Denote commercial temperature range device

	SYMBOL	RM/RV/RC4156(2)			LM149/249/349 LM148/248/348			HA4741-2/5			RM/RV/RC4157			UNIT
Maximum Ratings Supply Voltage Range	V_{CC}	±4 to ±20			±4 to ±22			±4 to ±20			±4 to ±20			V
Differential Input Voltage	V_{ID}	±30			±44/±36*			±30			±30			V
Input Voltage		±15			±22/±18*			±15			±15			V
Power Dissipation	P_D	880			900			800			880			mW
Electrical Characteristics	**@25°C**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	
Test Condition V_{CC}:			±15			±15			±15			±15		V
Input Offset Voltage	V_{IO}		0.5 1.0	3.0 5.0*		1.0	5.0 6.0*		0.5 1.0	3.0 5.0*		0.5 1.0	3.0 5.0*	mV
Input Offset Current	I_{IO}		15 30	30 50*		4	25 50*		15 30	30 50*		15 30	30 50*	nA
Input Bias Current	I_{IB}		60	200 300*		30	100 200*		60	200 300*		60	200 300*	nA
Input Common Mode Voltage Range	V_{ICR}	±12	±14		±12**			±12			±12			V
Supply Current	I_D		4.5/5	5/7*		2.4	3.6		4.5/5	5/7*		4.5/5	5/7*	mA
Open Loop Voltage Gain	A_{VOL}	50 25*	100		50 25*	160		50 25*	100 50*		50 25*	100		V/mV
Output Voltage Swing	V_{OR}	±12	±14		±12**	±13					±12			V
Common Mode Rejection Ratio	CMRR	80			70**	90		80			80			dB
Power Supply Rejection Ratio	PSRR	80dB			77** dB	96		80** dB			80 dB			
Unity Gain Bandwidth	BW	2.8	3.5			1.0/ 4.0†(1)			3.5		15(1)			MHz
Slew Rate	SR	1.3	1.6			0.5/ 2.0†			1.6		6.5	8		V/μs
Output Sink Current	I_{sink}							5	15					mA
Output Source Current	I_{source}							5	15					mA
Channel Separation			−108			−120			−108			−108		dB
Operating Temperature Range		−55 −40 0	RM RV RC	+125 85 70	−55 −25 0	148 248 348	+125 +85 +70	−55 0	−2 −5	+125 70	−55 −25 0	RM RV RC	+125 +85 +70	°C
Package: 14 pin Dip	Hermetic	DC			DC			DC			DC			
	Plastic	DB			DB			DB			DB			

*Denotes commercial temperature range device
**Applies over temperature
†149/349 ($A_{V_{min}}$ = 5) parameter
‡Denotes industrial temperature range device
(1)Gain-bandwidth product ($A_{V_{min}}$ = 5)
(2)Input noise voltage = 2 μV RMS max (20 Hz to 20 kHz)

Quad Comparators Summary

	SYMBOL	LM139A/LM139			LM239A/LM239/ LM339A/LM339			LM2901			RV3302			UNIT
Maximum Ratings														
Supply Voltage Range	V_{CC}	+4 to +36			+4 to +36			+4 to +36			+4 to +28 or ±14			V
Differential Input Voltage	V_{ID}	+36			+36			+36			+28			V
Input Voltage		+36			+36			+36			+28			V
Power Dissipation	P_D	800			800			570			625			mW
Electrical Characteristics		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Test Condition	V_{CC}		+5			+5			+5			+5		V
Input Offset Voltage	V_{IO}		2/1	5/2*		2/1	5/2*		2	7		3	20	mV
Input Offset Current	I_{IO}		3	25		5	50		5	50		3	100	nA
Input Bias Current	I_{IB}		25	100		25	250		25	250		25	500	nA
Input Common Mode Voltage Range	V_{ICR}	0		+3.5	0		+3.5	0		+3.5	0		+3.5	V
Supply Current	I_{OC}		0.8	2		0.8	2		0.8	2		0.7	1.5	mA
Open Loop Voltage Gain	A_{VOL}		200			200			200		2	30		V/mV
Common Mode Rejection Ratio	CMRR											60		dB
Slew Rate	SR											−200 +50		V/μs
Response Time	T_r		1.3			1.3			1.3			2.0		μs
Output Sink Current	I_{sink}	6	16		6	16		6	16		2	16		mA
Saturation Voltage	V_{sat}		0.2	0.4		0.2	0.4		0.2	0.4		0.25	0.5	V
Output Leak Current	I_{OL}		0.1			0.1			0.1				1.0	nA
Operating Temperature Range	T_A	−55		+125	−25 0	239A 339A	+85 +70	−40		+85	−40		+85	°C
Package: 14 Pin Dip	Hermetic	DC			DC						DC			
	Plastic	DB			DB			DB			DB			

*A version

RAYACT-883 PROGRAM

The Raytheon Acceptance Testing Program called Rayact-883 involves in-process inspections which assure compliance with MIL-STD-883 test methods and MIL-M-38510 Program Plan Requirements.

Table 1 defines the Standard Process Flow for Raytheon Semiconductor's Integrated Circuits. After completion of the in-process inspections and 100% production screens, each lot is subjected to a quality conformance inspection as defined in Table 2. The screening and acceptance testing outlined in Tables 1 and 2 are provided at no extra cost.

In addition to the Standard Process Flow and acceptance testing, Qualification Tests in accordance with MIL-STD-883, Method 5005 are conducted every three months on each product line. Generic Summary Data of Groups A, B, C and D is available upon request.

The level of reliability you desire can be selected from Table 3. These tests are conducted in accordance with Method 5004 of MIL-STD-883.

APPLICABLE DOCUMENTS:

Military: MIL-STD-883
MIL-M-38510
MIL-Q-9858

Raytheon Semiconductor:
Quality/Reliability Assurance Manual

PROCESS MONITORS

Quality control process monitors as shown on Table 1 are designed to verify our compliance with our internal written specifications.

Our monitor reports are used to identify problem areas and process trends.

From the analysis of these reports we are able to continually improve our processes.

DIE SALES

Raytheon devices are available in chip form as well as a variety of packages.

Each die is electrically tested to the applicable wafer probe test specification. In addition the die are 100% visually inspected to meet the requirements of MIL-STD-883 Method 2010 condition B. Die are then checked to assure a 1% AQL by quality control. Refer to Raytheon's dice catalog for complete product and processing information.

FAILURE ANALYSIS GROUP

The failure analysis group is capable of analyzing any material used in the Semiconductor industry. Equipment such as S.E.M., Auger Spectroscopy and Dispersive x-ray are used on a daily basis.

Full metallographic capability is also available for studying various structures.

Table 1—Standard Process Flow Summary for Integrated Circuits

COMMERCIAL		MILITARY	PROCESS FLOW
EPOXY	HERMETIC	HERMETIC	
X	X	X	Purchase raw material
X	X	X	Quality control receiving inspection. Parts are inspected to applicable M&SS and/or drawing.
X	X	X	Mask making
X	X	X	QC mask lot acceptance. Each lot is inspected for mask defects.
X	X	X	Wafer fabrication
X	X	X	QC process monitors including particle counts, DI water, gasses, SEM and diffusion
X	X	X	QC lot acceptance. Samples are selected from each lot.
X	X	X	100% electrical probe test per applicable spec
X	X	X	QC lot acceptance. Samples are selected from each lot
X	X	X	Wafer stores
X	X	X	Scribe and break and plate.
X	X	X	QC monitor
		X	100% die visual MIL-STD-883 Method 2010 condition B
X	X		100% die visual commercial spec
X	X	X	QC lot acceptance
X	X	X	Die attach.
X	X	X	QC monitor
	X	X	Ultrasonic aluminum bond.
	X	X	QC monitor
X			Thermal compression gold bond.
X			QC monitor
		X	Preseal inspection 100X MIL-STD-883 Method 2010 Condition B

Table 1—Standard Process Flow Summary for Integrated Circuits (Cont.)

COMMERCIAL		MILITARY	PROCESS FLOW
EPOXY	HERMETIC	HERMETIC	
		X	Preseal inspection 30X MIL-STD-883 Method 2010 Condition B
X	X		Preseal inspection 30X commercial specification
X	X	X	QC lot acceptance
X	X	X	Seal/mold and cure.
X	X	X	QC monitor
	X	X	Stabilization bake MIL-STD-883 Method 1008 Condition C 150°C for 24 hours
	X	X	Temperature cycle MIL-STD-883 Method 1010 Condition C -65 to +150°C, 10 cycles
	X	X	QC monitor
	X	X	Centrifuge* MIL-STD-883 Method 2001 Condition C, Y1 only
	X	X	QC monitor
	X	X	Tin plate MIL-STD-883 Method 2003
	X	X	QC monitor
X			Solder dip MIL-STD-883 Method 2003
X			QC monitor
		X	Hermeticity MIL-STD-883 Method 1014 Condition A or B and C
		X	QC monitor
X	X	X	Visual mechanical MIL-STD-883 Method 2009
X	X	X	QC monitor
X	X	X	DC and functional per applicable electrical test specification
X	X	X	QA lot acceptance
X	X	X	Unbranded inventory

*Except TK(TO66) packages.

Table 2—Quality Conformance Inspection (Each Lot)

INSPECTION		LTPD/MAX. ACC. NO.	COMMENTS
External		7/2	MIL-STD-883, Method 2009
Hermeticity		7/2	Military Products
Fine Leak			MIL-STD-883, Method 1014, Condition A or B
Gross Leak			MIL-STD-883, Method 1014, Condition C
Electrical			Per Applicable Electrical Test Specification
Static Parameters	+25°C	5/1	
	+125°C	7/1	
	-55°C	7/1	
Dynamic Parameters	+25°C	5/1	
	+125°C	7/1	
	-55°C	7/1	
Package and Ship		Quality Assurance Monitor	

NOTE:
Generic Qualification Data in accordance with MIL-STD-883, Method 5005, can be supplied if negotiated prior to procurement.

Table 3—Optional Screening Reference MIL-STD-883 Method 5004*

SCREEN	CLASS S (A)[14]		CLASS B		CLASS C	
	METHOD	REQMT	METHOD	REQMT	METHOD	REQMT
3.1.1 Internal visual[1]	2010, test condition A	100%	2010, test condition B	100%	2010, test condition B	100%
3.1.2 Stabilization bake (see 3.4.1, 3.4.2) no end point measurements required[16]	1008 24 hrs, min, test condition C min	100%	1008 24 hrs, min, test condition C min	100%	1008 24 hrs, min, test condition C min	100%
3.1.3 Temperature cycling[2]	1010, test condition C	100%	1010, test condition C	100%	1010, test condition C	100%
3.1.4 Constant acceleration (see 3.2 and 3.4.2)[16]	2001, test condition E (min) Y_1 orientation only	100%	2001, test condition E (min) Y_1 orientation only	100%	2001, test condition E (min) Y_1 orientation only	100%
3.1.5 Visual inspection[3]		100%		100%		100%
3.1.6 Seal[4] (a) Fine (b) Gross	1014	100% (5)	1014	100%	1014	100%
3.1.7 Particle impact noise detection (PIND)	2020, test condition A or B	100% (6)		–		–
3.1.8 Serialization		(7)		–		–
3.1.9 Interim (pre-burn-in) electrical parameters (see 3.5.1)[16]	Per applicable device specification	100% (8)	Per applicable device specification	(9)		–
3.1.10 Burn-in test (see 3.4.2)[16]	1015[10] 240 hrs at 125°C min	100%	1015[15] 160 hrs at 125°C min	100%		–
3.1.11 Interim (post-burn-in) electrical[16] parameters (see 3.5.1)	Per applicable device specification	100% (8)		–		–
3.1.12 Reverse bias burn-in[11] (see 3.4.2)[16]	1015; test condition A or C, 72 hrs at 150°C min[10]	100%		–		–
3.1.13 Interim (post-burn-in) electrical[16] parameters (see 3.5.1)	Per applicable device specification	100% (8)	Per applicable device specification	100%		–

*See footnotes at end of table.

Table 3—Optional Screening Reference MIL-STD-883 Method 5004 (Cont.)

SCREEN	CLASS S (A)(14)		CLASS B		CLASS C	
	METHOD	REQMT	METHOD	REQMT	METHOD	REQMT
3.1.14 Seal (a) Fine (b) Gross	1014	100%		–		–
3.1.15 Final electrical test (see 3.5.2)(16)	Per applicable device specification		Per applicable device specification		Per applicable device specification	
(a) Static tests (1) 25°C (subgroup 1, table I, 5005)		100%		100%		100%
(2) Maximum and minimum rated operating temp (subgroups 2, 3, table I, 5005)		100%		100%		–
(b) Dynamic tests and switching tests 25°C (subgroups 4 and 9, table I, 5005)		100%		100%		–
(c) Functional test 25°C (subgroup 7, table I, 5005)		100%		100%		100%
3.1.16 Radiographic (12)	2012 two views	100%		–		–
3.1.17 Qualification or quality conformance inspection test sample selection		(13)		(13)		(13)
3.1.18 External visual	2009	100%	2009	100%	2009	100%

NOTES:

(1) Unless otherwise specified, at the manufacturer's option, test samples for group B, bond strength (method 5005) may be selected randomly immediately following internal visual (method 5004) prior to sealing.
(2) For class B and C devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.
(3) At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages or lids off.
(4) For classes B and C devices, the seal test may be performed in any sequence between 3.1.6 and 3.1.16, but it shall be performed after all shearing and forming operations on the terminals.
(5) Optional when 3.1.14 is performed.
(6) See MIL-M-38510 paragraph 4.6.3. The PIND test may be performed in any sequence after 3.1.4 and prior to 3.1.13.
(7) Class S devices shall be serialized prior to interim electrical parameter measurements.
(8) Electrical parameters shall be read and recorded.
(9) When specified in the applicable device specification, 100 percent of the devices shall be tested for those parameters requiring delta calculations.
(10) For class S devices, test condition F of method 1015 and 3.4.2 herein shall not apply.
(11) The reverse bias burn-in (see 3.1.12) is a requirement only when specified in the applicable device specification and is recommended only for certain MOS, linear or other microcircuits where surface sensitivity may be of concern. When reverse bias burn-in is not required, interim electrical parameter measurements of 3.1.11 are omitted. The order of performing the burn-in (see 3.1.10) and the reverse bias burn-in may be inverted.
(12) The radiographic (see 3.1.16) screen may be performed in any sequence after 3.1.8.
(13) Samples shall be selected for testing in accordance with the specific device class and lot requirements of method 5005.
(14) Class A devices have been deleted from MIL-STD-883 and MIL-M-38510. Pending a decision on additional Class S requirements, class (A) has been included in this data book.
(15) May use 80 hours at 150°C.
(16) Refer MIL-STD-883, Method 5004 for complete details.

Table 4—Group Electrical Tests.(1) Reference MIL-STD-883

SUBGROUP(2)	CLASSES S (A) AND B LTPD(3)	CLASS C LTPD
Subgroup 1 Static tests at 25°C	5	5
Subgroup 2 Static tests at maximum rated operating temperature	7	10
Subgroup 3 Static tests at minimum rated operating temperature	7	10
Subgroup 4 Dynamic tests at 25°C	5	5
Subgroup 5 Dynamic tests at maximum rated operating temperature	7	10
Subgroup 6 Dynamic tests at minimum rated operating temperature	7	10
Subgroup 7 Functional tests at 25°C	5	5
Subgroup 8 Functional tests at maximum and minimum rated operating temperatures	10	15
Subgroup 9 Switching tests at 25°C	7	10
Subgroup 10 Switching tests at maximum rated operating temperature	10	15
Subgroup 11 Switching tests at minimum rated operating temperature	10	15

NOTES:

(1) The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

(2) A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed (see 30.2.5 of Appendix B of MIL-M-38510).

(3) Class A devices have been deleted from MIL-STD-883 and MIL-M-38510. Pending a decision on additional Class S requirements, class (A) has been included in this data book.

Table 5—Group B Tests for Classes B and C. (1) Reference MIL-STD-883 Method 5005

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	CLASSES B AND C LTPD
Subgroup 1			
a. Physical dimensions(2)	2016		2 devices (no failures)
b. Internal water-vapor content(3)	1018	1,000 ppm maximum water content at 100°C	3 devices (no failures)
Subgroup 2			
a. Resistance to solvents	2015		3 devices (no failures)
b. Internal visual and mechanical	2014	Failure criteria from design and construction requirements of applicable procurement document	1 devices (no failures)
c. Bond strength(4)	2011		15
(1) Thermocompression		(1) Test condition C or D	
(2) Ultrasonic or wedge		(2) Test condition C or D	
(3) Flip-chip		(3) Test condition F	
(4) Beam lead		(4) Test condition H	
Subgroup 3			
Solderability(5)	2003	Soldering temperature of 260 ±10°C.	15

NOTES:

(1) Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required.
(2) Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.
(3) This test is required only if the package contains a desiccant.
(4) Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected immediately following internal visual (precap) inspection specified in Method 5004, prior to sealing. Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 10 devices, and for conditions F or H is the number of dice (not bonds) (see Method 2011).
(5) All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.

Table 5a—Group B Tests for Class S (A) Devices. (1) Reference MIL-STD-883 Method 5005

TEST	MIL-STD-883		CLASS S A(10) QUANTITY/(ACCEPT NO.)	
	METHOD	CONDITION	LOT 1	LOT 2 AND SUBSEQUENT
Subgroup 1				
(a) Physical dimensions(2)	2016		2(0)	2(0)
(b) Internal water-vapor content(3)	1018	1,000 ppm maximum water content at 100°C	3(0)	3(0)
Subgroup 2(4)	2015			
(a) Resistance to solvents	2013		3(0)	3(0)
(b) Internal visual and mechanical	and 2014	Failure criteria from design and construction requirements of applicable procurement document	2(0)	2(0)
(c) Bond strength	2011		2(0)(8)	2(0)(8)
(1) Thermocompression		(1) Test condition C or D		
(2) Ultrasonic		(2) Test condition C or D		
(3) Flip-chip		(3) Test condition F		
(4) Beam lead		(4) Test condition H		
(d) Die shear test	2019	Per table I of Method 2019 for the applicable die size	3(0)	3(0)
Subgroup 3				
Solderability(5)	2003	Soldering temperature of 260 ±10°C	LTPD = 15	LTPD = 15
Subgroup 4				
Lead integrity	2004	Test condition B_2, lead fatigue	2(0)	2(0)
Seal	1014	As applicable		
(a) Fine				
(b) Gross				

See footnotes at end of table.

Table 5a—Group B Tests for Class S (A) Devices. (1) Reference MIL-STD-883 Method 5005 (Cont.)

TEST	MIL-STD-883		CLASS S A(10) QUANTITY/(ACCEPT NO.)	
	METHOD	CONDITION	LOT 1	LOT 2 AND SUBSEQUENT
Subgroup 5(6)(7)				
(a) Gate 1				
(1) Electrical parameters		Group A, subgroup 1, 2, 3: Read and record		
(2) Steady state life (accelerated)	1005	Group A, subgroups 4-11: Attributes Condition F, 250°C, 120 continuous hours minimum		
(3) Electrical parameters		Group A, subgroups 1, 2, 3: Read and record	40(8)	10(2)
(b) Gate 2				
(1) Steady state life (accelerated)	1005	Condition F, 250°C, 240 hours minimum including actual gate 1 life test duration		
(2) Seal a. Fine b. Gross	1014	As applicable		
(3) Electrical parameters		Group A, subgroups 1, 2, 3: Read and record Group A, subgroups 4-11: Attributes	40(16)(9)	10(4)(9)
Subgroup 6(4)				
(a) Electrical parameters		Group A, subgroups 1, 2, 3: Read and record		
(b) Temperature cycling	1010	Condition C 100 cycles/min	12(0)	5(0)
(c) Constant acceleration	2001	Test condition E: Y_1 orientation only		
(d) Seal	1014		or	or
(1) Fine				
(2) Gross			20(1)	8(1)
(e) Electrical parameters		Group A, subgroups 1, 2, 3: Read and record		

NOTES:

(1) Electrical reject devices from the same inspection may be used for all subgroups when end-point measurements are not required.
(2) Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.
(3) This test is required only if the package contains a desiccant.
(4) For class S lot quality conformance testing, all samples for subgroup B2 must have been through the complete sequence of subgroup B6 tests.
(5) All devices must have been through the temperature/time exposure in burn-in. The LTPD applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.
(6) The alternate removal-of-bias provisions of 3.3.1 and 3.2.1 of Methods 1005 and 1015 respectively shall not apply for test temperatures above 125°C.
(7) At the manufacturer's option, an alternate life test may be performed in accordance with 3.8.2.
(8) All bonds on both devices shall be pulled or, for condition F or H, all dice shall be tested.
(9) Sample quantity for acceptance purposes is the incoming sample for gate 1 and the accept number applies to the total failures from both gate 1 and gate 2.
(10) Class A devices have been deleted from MIL-STD-883 and MIL-M-38510. Pending a decision on additional Class S requirements, class (A) has been included in this data book.

Table 6—Group C (Die-Related Tests) (for Classes B and C Only). Reference MIL-STD-883 Method 5005

TEST	MIL-STD-883		LTPD
	METHOD	CONDITION	
Subgroup 1			
Steady state life test(1)	1005	Test condition to be specified (1,000 hours at 125°C)	5
End-point electrical parameters		As specified in the applicable device specification	
Subgroup 2			
Temperature cycling	1010	Test condition C	15
Constant acceleration	2001	Test condition E min (for large packages, see 3) Y_1 orientation only	
Seal (a) Fine (b) Gross	1014	As applicable	
Visual examination	(2)		
End-point electrical parameters		As specified in the applicable device specification	

NOTES:
(1) See 40.4 of Appendix B of MIL-M-38510.
(2) Visual examination shall be in accordance with Method 1010 or 1011.

Table 7—Group D (Package Related Tests) (for All classes). Reference MIL-STD-883 Method 5005

TEST	MIL-STD-883		LTPD
	METHOD	CONDITION	
Subgroup 1			
(a) Physical dimensions	2016		15
(b) Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3 devices (no failures)
Subgroup 2(1)			
Lead integrity	2004	Test condition B2 (lead fatigue)	15
Seal	1014	As applicable	
(a) Fine			
(b) Gross			
Subgroup 3(2)			
Thermal shock	1011	Test condition B as a minimum, 15 cycles minimum	15
Temperature cycling	1010	Test condition C, 100 cycles minimum	
Moisture resistance	1004		
Seal	1014	As applicable	
(a) Fine			
(b) Gross			
Visual examination		Per visual criteria of Method 1004	
End-point electrical parameters(4)		As specified in the applicable device specification	
Subgroup 4(2)			
Mechanical shock	2002	Test condition B	15
Vibration variable frequency	2007	Test condition A	
Constant acceleration	2001	Test condition E (see 3), Y_1 orientation only	
Seal	1014	As applicable	
(a) Fine			
(b) Gross			
Visual examination	(3)		
End-point electrical parameters		As specified in the applicable device specification	
Subgroup 5(1)			
Salt atmosphere	1009	Test condition A	15
Seal	1014	As applicable	
(a) Fine			
(b) Gross			
Visual examination		Per visual criteria of Method 1009	

NOTES:

(1) Electrical reject devices from that same inspection lot may be used for samples.
(2) Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical."
(3) Visual examination shall be in accordance with Method 1010 or 1011.
(4) At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

NOTICE

Tables 3, 4, 5, 6 and 7 are referenced from MIL-STD-883. These are for reference only. All required test, screening procedures, classes or sub-group levels, whether in addition to or apart from any military standards must be specified on the purchase order and agreed upon in writing by Raytheon Co.

Introduction

Raytheon's A+ program is designed to provide the Industrial and Commercial marketplace with product reliability. ■ Reliability consistent with application requirements. ■ Reliability that avoids an **overbuy** situation where the user pays for screening beyond the scope of his needs.

Raytheon offers three screening flows under the A+ program. Each having a separate reliability factor and cost saving. When deciding which A+ flow best suits your needs, you should consider the cost savings realized through elimination of outside lab services and the need to tighten incoming inspection. Users who do not presently have their integrated circuits screened should consider the cost of component replacement during system test and in the field. Substantial cost savings can now be realized by specifying Raytheon's A+ program.

The designations A+1 and A+2 are used for epoxy B packaged devices only. A+3 is reserved for ceramic devices. The appropriate screening level may be specified by simply adding the proper A+ suffix to the Raytheon part number, i.e., - - RC4136DB with A+2 screening would be designated RC4136DB2.

Customers who use the epoxy package may wish to obtain a copy of the **Epoxy Encapsulated Linear I.C. Quality Review**, available from your local Raytheon sales office.

Basic Reliability Measures

Raytheon has instituted an internal program to assure that products bearing the Raytheon logo are unsurpassed in reliability when used in the industrial environment. Several tests, including some normally reserved for military products, are applied to our industrial products on a continuing basis in support of this effort. A brief summary of these tests is given below.

1. Monitored Burn-In (all packages)

24 hours at +125°C with zero failures allowed. This RVT (reliability verification test), a Raytheon exclusive, is performed on 20 samples from each manufacturing lot.

2. Standard Burn-In (all packages)

168 hours at +125°C, 1% PDA. This RVT is performed on 45 samples from each EIA data code.

3. Operating Life (all packages)

1000 hours at +125°C, LTPD = 5. This RVT is performed on all new products and periodically on existing product types as an indicator of long-term reliability.

4. Steam Pressure (epoxy packages only)

24 hours at +125°C in steam vapor. This RVT is performed on 25 samples from each EIA data code as to assure package and device integrity.

5. 85/85 (epoxy packages only)

168 hours with bias at +85°C and 85% relative humidity. This RVT is performed on 25 samples from each EIA data code also as an indicator of package and device integrity.

6. Temperature Cycle (epoxy packages only)

100 cycles per method 1010.1, 0°C to 100°C. This RVT is performed on 25 samples from each EIA date code to mechanically stress the wire bond, die bond and package material.

7. Military Flow (ceramic packages and metal-cans)

Only dice lots which pass MIL-STD-883 condition B visual tests are used in these packages and the 883 class B flow is used up to point of electrical test. This provides military type product reliability at commercial prices.

A+ Programs Increase Reliability

Raytheon's A+ programs were designed to provide an even greater reliability assurance than standard process testing. Starting with devices which are processed with the basic reliability measures, various combinations of temperature cycle, burn-in, **Hot Rail** testing and tightened AQL lot acceptance are available as shown in the flow chart. The objectives of these 100% screens are:

1. Temperature Cycle (epoxy packages only)

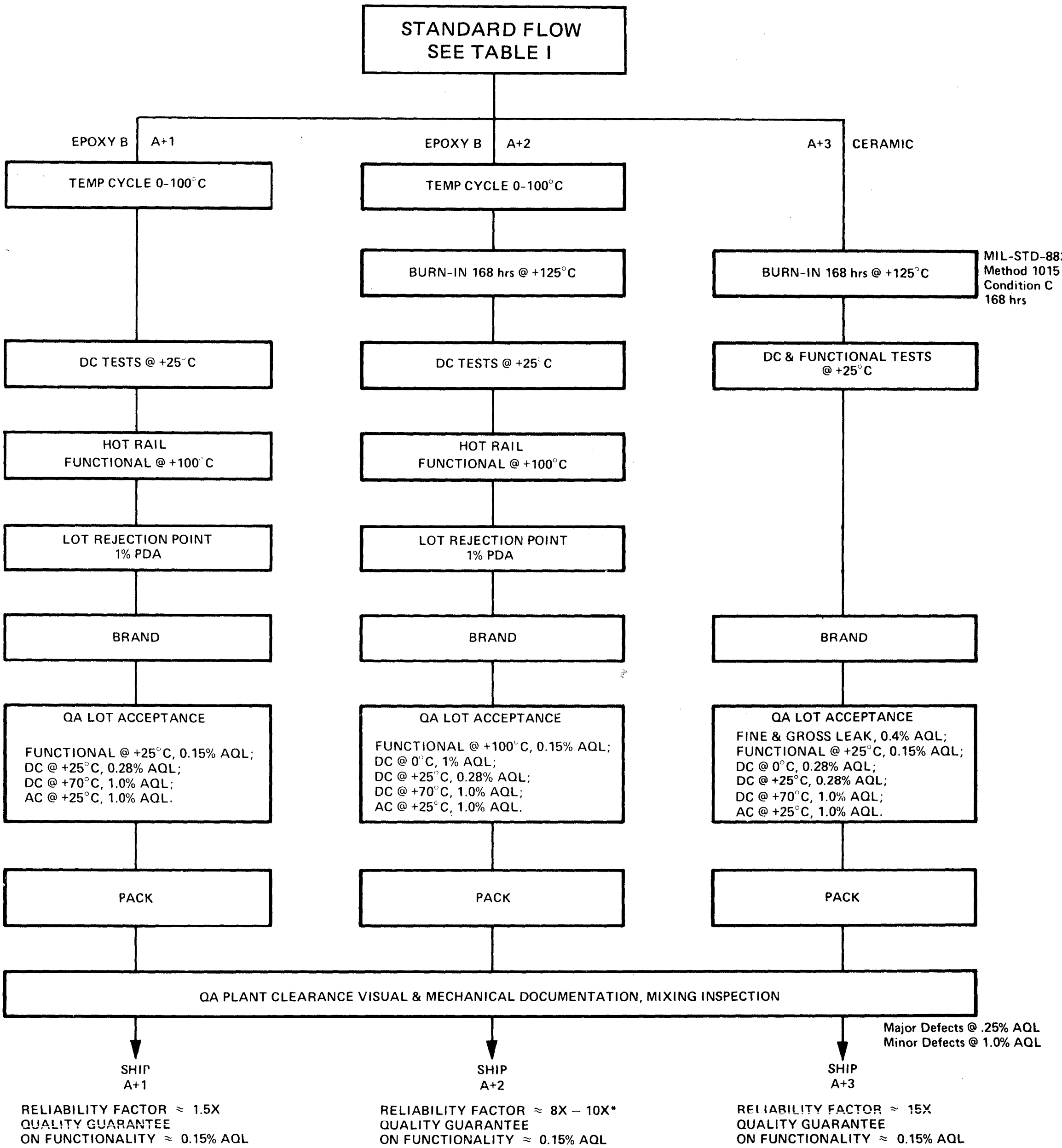
0°C to +100°C per method 1011, condition A. This is the first screening for the A+1 and A+2 flows. (A+3 ceramic and metal-can devices received temperature cycles as part of standard product flow.) The purpose of this screening is to stress wire bonds and die bonds mechanically to prove the integrity of the devices.

2. Burn-In (all packages)

168 hours at +125°C or equivalent up to 200°C. This screening is performed in A+2 and A+3 flows.

3. High Temperature Functional Test (Hot Rail) (epoxy packages only)

+100°C. This screening serves to further prove bond integrity.



* Must be expressed as a range since a normally controlled environment (constant power and temperature) cannot be assured.

OP AMPS

Average Input Offset Current t° Coefficient—Change in input offset current divided by change in ambient temperature producing it.

Average Input Offset Voltage t° Coefficient—Change in input offset voltage divided by change in ambient temperature producing it.

Common-Mode Input Resistance—Resistance looking into both inputs tied together.

Common-Mode Rejection Ratio (CMRR)—Ratio of change of input offset voltage to input common-mode voltage change producing it.

Full Power Bandwidth—Maximum frequency at which full sinewave output might be obtained.

Input Bias Current—Average of the two input currents at zero output voltage. In some cases, input current for either input independently.

Input Capacitance—Capacitance looking into either input terminal with other grounded.

Input Current—Current into an input terminal.

Input Noise Voltage—Square root of mean square narrow-band noise voltage referred to input.

Input Offset Current—Difference in currents into two input terminals with output at zero volts.

Input Offset Voltage—Voltage which must be applied between input terminals to obtain zero output voltage. Input offset voltage may also be defined for case where two equal resistances are inserted in series with input leads.

Input Resistance—Resistance looking into either input terminal with other grounded.

Input Voltage Range—Range of voltages on input terminals for which amplifier operates within specifications. In some cases, input offset specifications apply over input voltage range.

Large-Signal Voltage Gain—Ratio of maximum output voltage swing to change in input voltage required to drive output to this voltage.

Output Resistance—Resistance seen looking into output terminal with output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate influence of drift and thermal feedback.

Settling Time—Time between initiation of input step function and time when output voltage has settled to within specified error band of final output voltage.

Output Short-Circuit Current—Maximum output current available from amplifier with output shorted to ground or to either supply.

Output Voltage Swing—Peak output swing, referred to zero, that can be obtained.

Power Consumption—DC power required to operate amplifier with output at zero and with no load current.

Power Supply Rejection Ratio—Ratio of change in input offset voltage to change in supply voltages producing it.

Rise Time—Time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate—Maximum rate of change of output voltage under large signal condition.

Supply Current—Current required from power supply to operate amplifier with no load and output at zero.

Temperature Stability Of Voltage Gain—Maximum variation of voltage gain over specified temperature range.

Harmonic Distortion—Percentage of harmonic distortion being defined as 100 times ratio of RMS sum of harmonics to fundamental.

% harmonic distortion =

$$\frac{(V_2{}^2 + V_3{}^3 + V_4{}^2 + \ldots)^{1/2}\,(100\%)}{V_I}$$

where V_I is RMS amplitude of fundamental and V_2, V_3, V_4, . . . are RMS amplitudes of individual harmonics.

Transient Response—Closed-loop step-function response of amplifier under small-signal conditions.

Unity Gain Bandwidth—Frequency range from DC to frequency where amplifier open-loop gain rolls off to one.

Voltage Gain—Ratio of output voltage to input voltage under stated conditions for source resistance (R_S) and load resistance (R_L).

Bandwidth—Frequency at which voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Output Impedance—Ratio of output voltage to output current under stated conditions for source resistance (R_S) and load resistance (R_L).

Input Impedance—Ratio of input voltage to input current under stated conditions for source resistance (R_S) and load resistance (R_L).

REGULATORS

Dropout Voltage—Input-output voltage differential at which circuit ceases to regulate against further reductions in input voltage.

Input-Output Voltage Differential—Range of voltage difference between supply voltage and regulated output voltage over which regulator will operate.

Line Regulator—Percentage change in output voltage for a specified change in input voltage.

Load Regulator—Percentage change in output voltage for specified change in load current.

Maximum Power Dissipation—Maximum total device dissipation for which regulator will operate within specifications.

Output Noise Voltage—RMS output noise voltage with constant load and no input ripple.

Output Voltage Range—Range of output voltage over which regulator will operate.

Quiescent Current—Part of input current to regulator that is not delivered to load.

Reference Voltage—Output of reference amplifier measured with respect to negative supply.

Ripple Rejection—Ratio of peak-to-peak input ripple voltage to peak-to-peak output ripple voltage.

Sense Voltage—Voltage between current sense and current limit terminals necessary to cause current limiting.

Short-Circuit Current Limit—Output current of regulator with output shorted to negative supply.

Standby Current Drain—Supply current drawn by regulator with no output load and no reference voltage load.

Temperature Stability—Percentage change in output voltage for thermal variation from room temperature to either temperature extreme.

Long Term Stability—Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

Output Voltage Scale Factor—Output voltage obtained for unit value of resistance between adjustment terminal and ground.

Input Voltage Range—Range of DC input voltages over which regulator will operate within specifications.

Current-Limit Sense Voltage—Voltage across current limit terminals required to cause regulator to current-limit with short-circuited output. This voltage is used to determine value of external current-limit resistor when external booster transistors are used.

COMPARATORS/SENSE AMPLIFIERS

Common-Mode Firing Voltage—CM input voltage that exceeds dynamic range of inputs with strobe enabled resulting in output switching states.

Common-Mode Recovery Time—Time from turn off of CM signal to analog input threshold of earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than input threshold with corresponding proper output.

Equivalent Input Common-Mode Noise Voltage—Change in input offset voltage due to common-mode input noise.

Logic Input High Voltage—Minimum voltage allowed at bit control gate to hold bit off.

Logic Input Low Voltage—Maximum voltage allowed at bit control gate to hold bit on.

Output Sink Current—Maximum negative current that can be delivered by comparator.

Peak Output Current—Maximum current that may flow into output load without causing damage to comparator.

Propagation Delay—Interval between application of an input voltage step and its arrival at either output, measured at 50% of final value.

Response Time—Interval between application of input step function and time when output crosses logic threshold voltage. Input step drives comparator from some initial, saturated input voltage to input level just barely in excess of that required to bring output from saturation to logic threshold voltage overdrive.

Strobe Current—Maximum current drawn by strobe terminals when it is at zero logic level.

Strobe Delay—Time delay measured from strobe to output threshold with signal present exceeding input threshold.

Strobe Release Time—Time required for output to rise to logic threshold voltage after strobe terminal has been driven from zero to one logic level. Appropriate input conditions are assumed.

Strobed Output Level—DC output voltage, independent of input voltage, with voltage on strobe terminal equal to or less than minimum specified amount.

Switching Speed—Time required to turn on least significant bit.

Threshold Uncertainty—With all sense amps sharing same input threshold less uncertainty as "0." This includes unit to unit, power supply and temperature variations.

Threshold Voltage—Typical referred to input voltage which determines whether input is "1" or "0." Signal whose magnitude is greater than threshold level is sensed as logic "1" and signal whose magnitude is less as "0."

Zero Scale Output Current—Output current for all bits turned off.

Supply Current—Current required from positive or negative supply to operate comparator with no output load. Power will vary with input voltage, but is specified as maximum for entire range of input voltage conditions.

Voltage Gain—Ratio of change in output voltage to change in voltage between input terminals producing it.

Differential Input Offset Current—Absolute difference in two input bias currents of one differential input.

Differential Input Overload Recovery Time—Time necessary for device to recover from 2V differential pulse ($t_f = t_r = 20ns$) prior to strobe enable signal.

Offset Voltage—Difference between absolute values of threshold voltage in positive- and negative-going directions.

Input Bias Current—Average of two input currents.

Input Offset Current—Absolute value of difference between two input currents for which output will be driven higher or lower than specified voltages.

Glossary of Terms

Input Offset Voltage—Absolute value of voltage between input terminals required to make output voltage greater or less than specified voltages.

Input Voltage Range—Range of voltage on input terminals (common-mode) over which offset specifications apply.

Positive Output Level—High output voltage level with given load and input drive equal to or greater than specified value.

Power Consumption—Power required to operate comparator with no output load. Power will vary with signal level, but is specified as maximum for entire range of input signal conditions.

Output Leakage Current—Current into output terminal with output voltage within given range and input drive equal to or greater than given value.

Output Resistance—Resistance seen looking into output terminal with DC output level at logic threshold voltage.

Strobed Output Level—DC output voltage, independent of input conditions, with voltage on strobe terminal equal to or less than specified low state.

Strobe ON Voltage—Maximum voltage on either strobe terminal required to force output to specified high state independent of input voltage.

Differential Input Threshold Voltage—DC input voltage which forces logic output to logic threshold voltage ($\sim$1.5V) level.

Input Bias Current—DC current which flows into each input pin with differential input of 0V.

Negative Output Level—Negative DC output voltage with comparator saturated by differential input equal to or greater than specified voltage.

Strobe OFF Voltage—Minimum voltage on strobe terminal that will guarantee that it does not interfere with operation of comparator.

SECTION 1

Operational Amplifiers

CONTENTS

GENERAL DESCRIPTION

The LM101A/LM201A and LM301A are general purpose, high performance operational amplifiers fabricated monolithically on a silicon chip by the planar epitaxial process. The units may be fully compensated with the addition of a 30pF capacitor stabilizing the circuit for all feedback configurations including capacitive loads.

The device may be operated as a comparator with a differential input as high as ±30V. Used as a comparator the output can be clamped at any desired level to make it compatible with logic circuits.

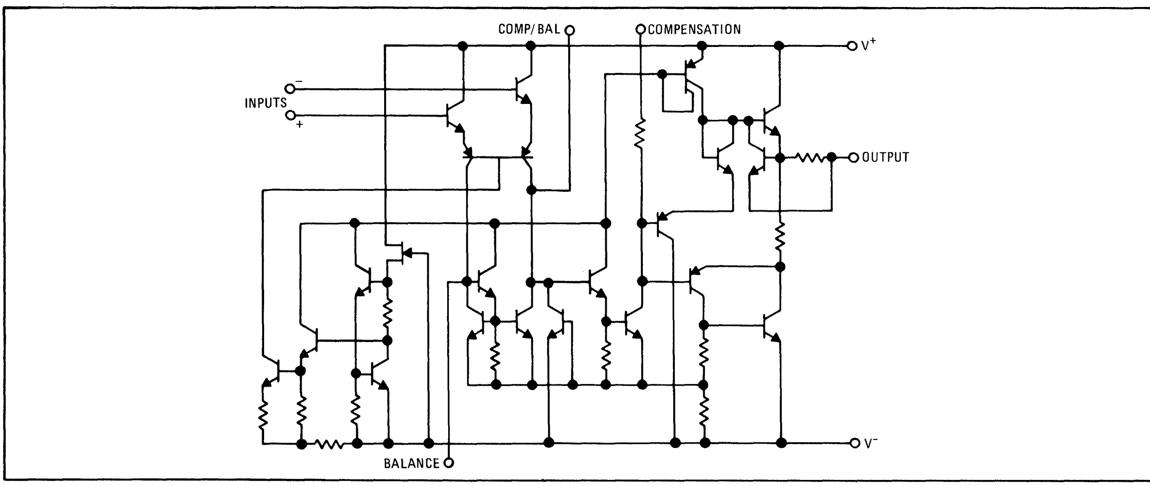
The LM101A operational amplifier will operate over the full military temperature range from −55°C to +125°C. The commercial version, the LM301A operates over a temperature range from 0°C to +70°C..

The LM201A is the same as the LM101A except its performance is guaranteed from −25°C to +85°C.

DESIGN FEATURES

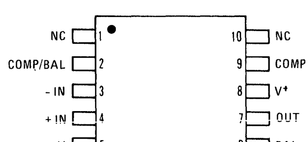
- Offset Voltage 3mV Maximum Over Temperature
- Input Current 100nA Maximum Over Temperature
- Offset Current 20nA Maximum Over Temperature
- Offsets Guaranteed Over Entire Common-Mode Range and Supply Voltage Range
- Frequency Compensation 30pF
- Supply Voltage ±5V to ±20V

SCHEMATIC DIAGRAM



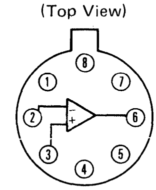
CONNECTION INFORMATION

CQ Flatpak
(Top View)



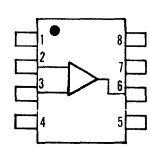
Order Part No.:
LM101AF

TE
Metal Can Package
(Top View)



Order Part Nos.:
LM101AH, LM201AH,
LM301AH

DE and NB
Dual In-line Package
(Top View)



Order Part Nos.:
LM101ADE, LM201ADE,
LM301ADE, LM301AN

PIN	FUNCTION
1	COMP/BAL
2	−INPUT
3	+INPUT
4	V−
5	BAL
6	OUTPUT
7	V+
8	COMP

NOTE: THE LM101A/301A IS AVAILABLE ON SPECIAL ORDER IN THE DC (14-PIN) CERAMIC DIP PACKAGE.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	101A, 201A: ±22V 301A: ±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
LM101A	−55°C to +125°C
LM201A	−25°C to +85°C
LM301A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60s)	300°C

ELECTRICAL CHARACTERISTICS

LM101A, LM201A: $\pm 5V \leqslant V_S \leqslant \pm 20V$; LM301A: $\pm 5 \leqslant V_S \leqslant \pm 15V$ (Note 4)

PARAMETER	CONDITIONS	LM101A, LM201A			LM301A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leqslant 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4		0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$		1.8	3.0		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geqslant 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leqslant 50\ k\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leqslant T_A \leqslant 125°C$		0.01	0.1				nA/°C
	$25°C \leqslant T_A \leqslant 70°C$					0.01	0.3	nA/°C
	$-55°C \leqslant T_A \leqslant 25°C$		0.02	0.2				nA/°C
	$0°C \leqslant T_A \leqslant 25°C$					0.02	0.6	nA/°C
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geqslant 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	LM101A: $V_S = \pm 20V$; LM301A: $V_S = \pm 15V$	±15			±12			V
Common Mode Rejection Ratio	$R_S \leqslant 50\ k\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 50\ k\Omega$	80	96		70	96		dB

NOTES:

1. For operating at elevated temperatures, the device must be derated based on +150°C for LM101A, +100°C for LM201A and LM301A, maximum junction temperature and a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short-circuit is allowed for case temperatures to +125°C and ambient temperatures to +75°C for LM101A, case temperatures to +70°C and ambient temperatures to +55°C for LM301A.
4. Specifications apply for temperature ranges: LM101A: −55°C to +125°C; LM201A: −25°C to +85°C; LM301A: 0°C to +70°C unless otherwise specified.

GENERAL DESCRIPTION

The LM107, LM207, and LM307 high-gain, general purpose operational amplifiers are monolithically constructed and internally compensated. The addition of a 30pF MOS capacitor guarantees unconditional stability eliminating the need for external frequency compensation. Input currents are a factor of ten lower than an industry standard device such as the 709, LM101, and 741.

This series offers all the best features of the LM101. In addition, the devices provide better accuracy and lower noise in high impedance circuitry.

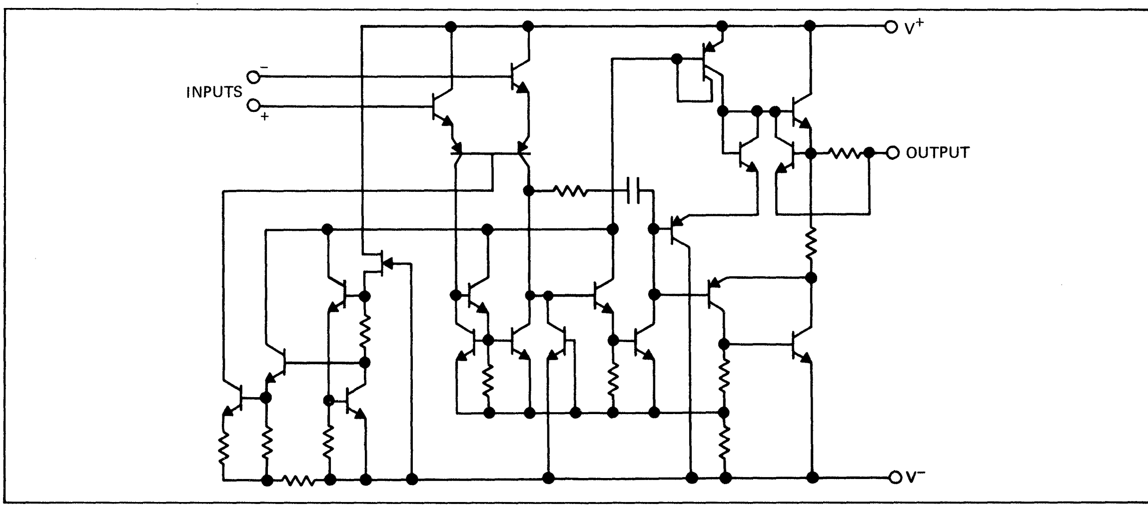
The LM107 operates over a temperature range of −55°C to +125°C. The LM307 operates from 0°C to +70°C.

The LM207 is the same as the LM107 except its performance is guaranteed from −25°C to +85°C.

DESIGN FEATURES

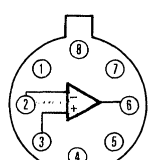
- Offset Voltage 3mV Maximum Over Temperature
- Input Current 100nA Maximum Over Temperature
- Offset Current 20nA Maximum Over Temperature
- Offsets Guaranteed Over Entire Common-Mode Range and Supply Voltage Range
- Internal Frequency Compensation
- Supply Voltage ±5V to ±20V

SCHEMATIC DIAGRAM



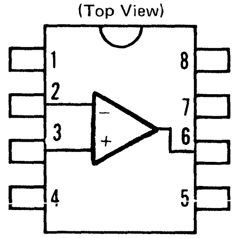
CONNECTION INFORMATION

TE
Metal Can Package
(Top View)



Order Part No.:
LM107H, LM207H, LM307H

DE and NB
Dual In-line Package
(Top View)



Order Part No.:
LM107DE, LM207DE,
LM307DE, LM307N

PIN	FUNCTION
1	NC
2	−INPUT
3	+INPUT
4	V−
5	NC
6	OUTPUT
7	V+
8	NC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	107A, 207A: ±22V; 307A: ±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	
LM107	-55^oC to $+125^oC$
LM207	-25^oC to $+85^oC$
LM307	0^oC to $+70^oC$
Storage Temperature Range	-65^oC to $+150^oC$
Lead Temperature (Soldering, 60s)	300^oC

ELECTRICAL CHARACTERISTICS LM107A, LM207A: $\pm5V \leqslant V_S \leqslant \pm20V$; LM307A: $\pm5 \leqslant V_S \leqslant \pm15V$ (Note 4)

PARAMETER	CONDITIONS	LM107/207 MIN	LM107/207 TYP	LM107/207 MAX	LM307 MIN	LM307 TYP	LM307 MAX	UNITS
Input Offset Voltage	$T_A = 25^oC$, $R_S \leqslant 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25^oC$		1.5	10		3	50	nA
Input Bias Current	$T_A = 25^oC$		30	75		70	250	nA
Input Resistance	$T_A = 25^oC$	1.5	4		0.5	2		MΩ
Supply Current	$T_A = 25^oC$, $V_S = \pm20V$		1.8	3.0		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25^oC$, $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L \geqslant 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leqslant 50\ k\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	$\mu V/^oC$
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25^oC \leqslant T_A \leqslant 125^oC$		0.01	0.1				$nA/^oC$
	$25^oC \leqslant T_A \leqslant 70^oC$					0.01	0.3	$nA/^oC$
	$-55^oC \leqslant T_A \leqslant 25^oC$		0.02	0.2				$nA/^oC$
	$0^oC \leqslant T_A \leqslant 25^oC$					0.02	0.6	$nA/^oC$
Input Bias Current				100			300	nA
Supply Current	$T_A = +125^oC$, $V_S = \pm20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L \geqslant 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm20V$	±15			±12			V
Common Mode Rejection Ratio	$R_S \leqslant 10\ k\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10\ k\Omega$	80	96		70	96		dB

NOTES:
1. For operating at elevated temperatures, the device must be derated based on $+150^oC$ for LM107 or 100^oC for LM207 and LM307, maximum junction temperature and a thermal resistance of $150^oC/W$ junction to ambient or $45^oC/W$ junction to case.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short-circuit is allowed for case temperatures to $+125^oC$ and ambient temperatures to $+75^oC$ for LM107, case temperatures to $+70^oC$ and ambient temperatures to $+55^oC$ for LM307.
4. These specifications apply for $-55^oC < T_A < +125^oC$ LM107, -25^oC to $+85^oC$ LM207, and $0^oC < T_A < +70^oC$ LM307, unless otherwise specified.

GENERAL DESCRIPTION

The LM108A/LM108, LM208A/LM208 and LM308A/LM308 are Super Beta operational amplifiers fabricated on single silicon chips using the planar epitaxial process.

The LM108A/LM108 offer specifications an order of magnitude better than FET amplifiers over a temperature range −55°C to +125°C.

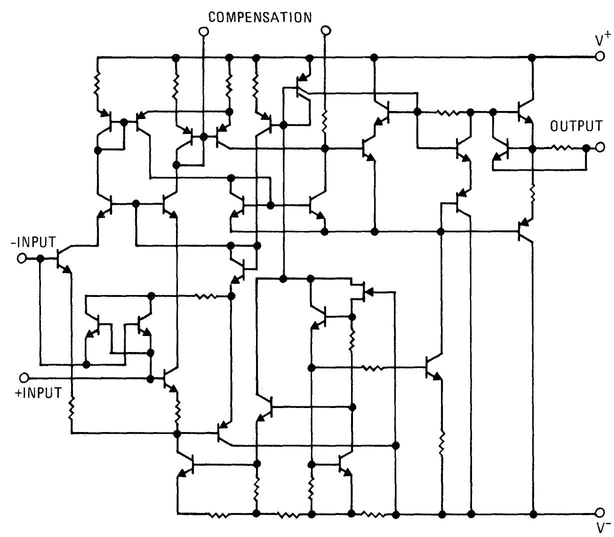
The LM208A/LM208 are identical to the LM108A/LM108 except their performance is guaranteed from −25°C to +85°C.

The LM308A/LM308 provide lower input offset voltage of 0.5mV maximum, and drift characteristics of 5.0μV/°C maximum. These devices can be compensated by the conventional technique used with the LM101/LM101A series.

DESIGN FEATURES

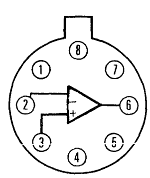
- Offset Voltage Over Temperature Range 0.5mV Maximum
- Input Current Over Temperature Range 3.0nA Maximum
- Offset Current Over Temperature Range 400pA Maximum
- Supply Current Only 400μA
- Guaranteed Drift Characteristics 5.0μV/°C Maximum
- Supply Voltage ±2V to ±20V

SCHEMATIC DIAGRAM



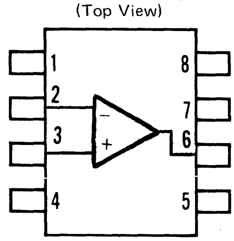
CONNECTION INFORMATION

TE
Metal Can Package
(Top View)



Order Part Nos.:
LM108AH, LM208AH,
LM308AH, LM108H,
LM208H, LM308H

DE and NB
Dual In-line Packages
(Top View)



Order Part Nos.:
LM108ADE, LM208ADE,
LM108DE, LM208DE
LM308DE, LM308ADE
LM308N

PIN	FUNCTION
1	COMP
2	−INPUT
3	+INPUT
4	V−
5	NC
6	OUTPUT
7	V+
8	COMP

NOTE: THE LM108A SERIES IS AVAILABLE ON SPECIAL ORDER IN THE DC (14-PIN) CERAMIC DIP AND CQ (10-PIN) FLATPAK PACKAGES.

RAYTHEON

Precision Operational Amplifiers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .... LM108A/LM108: ±20V
LM208A/LM208: ±20V
LM308A/LM308: ±18V
Power Dissipation (Note 1) 500mW
Differential Input Current (Note 3) .... ±10mA
Input Voltage (Note 2) .... ±15V
Output Short-Circuit Duration .... Indefinite

Operating Temperature Range
LM108A/LM108 .... −55°C to +125°C
LM208A/LM208 .... −25°C to +85°C
LM308A/LM308 .... 0°C to +70°C
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 60s) .... 300°C

ELECTRICAL CHARACTERISTICS (Notes 4 and 5)

PARAMETER	CONDITIONS	LM108A/LM208A			LM308A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A=25°C		0.3	0.5		0.3	0.5	mV
Large Signal Voltage Gain	T_A=25°C, V_S=±15V, V_{out}=±10V, $R_L \geqslant 10k\Omega$	80	300		80	300		V/mV
Input Offset Voltage				1.0			0.73	mV
Average Temperature Coefficient of Input Offset Voltage			1.0	5.0		1.0	5.0	μV/°C
Large Signal Voltage Gain	V_S=±15V, V_{out}=±10V, $R_L \geqslant 10k\Omega$	40			60			V/mV
Common Mode Rejection Ratio		96	110		96	110		dB
Supply Voltage Rejection Ratio		96	110		96	110		dB

PARAMETER	CONDITIONS	LM108/LM208			LM308			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A=25°C		0.7	2.0		2.0	7.5	mV
Input Offset Current	T_A=25°C		0.05	0.2		0.2	1.0	nA
Input Bias Current	T_A=25°C		0.8	2.0		1.5	7.0	nA
Input Resistance	T_A=25°C	30	70		10	40		MΩ
Supply Current	T_A=25°C		0.3	0.6		0.3	0.8	mA
Large Signal Voltage Gain	T_A=25°C, V_S=±15V, V_{out}=±10V, $R_L \geqslant 10k\Omega$	50	300		25	300		V/mV
Input Offset Voltage				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				0.4			1.5	nA
Average Temperature Coeffiecient of Offset Current			0.5	2.5		2.0	10	pA/°C
Input Bias Current				3.0			10	nA
Supply Current	T_A=+125°C		0.15	0.4				mA
Large Signal Voltage Gain	V_S=±15V, V_{out}=+10V, $R_L \geqslant 10k\Omega$	25			15			V/mV
Output Voltage Swing	V_S=±15V, R_L=10kΩ	±13	±14		±13	±14		V
Input Voltage Range	V_S=±15V	±13.5			14			V
Common Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

NOTES:

1. For operating at elevated temperatures, the device must be derated based on +150°C for LM108, +100°C for LM308 maximum junction temperature and a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
4. These specifications apply for ±5V < V_S < ±20V and −55°C < $T_A \leqslant$ +125°C, LM108A/LM108; ±5V < V_S < ±20V and −25°C < T_A < +85°C, LM208A/LM208.
5. These specifications apply for ±5V < V_S < ±15V and 0°C < T_A < +70°C, LM308A/LM308.

GENERAL DESCRIPTION

The LM118, LM218, and LM318 are precision operational amplifiers which offer fast slewing and wide bandwidth. They feature internal frequency compensation and ten times the speed of general purpose amplifiers.

External feedforward compensation may be used for an additional increase in speed. For inverting applications this will increase the slew rate to more than 150V/μs and almost double the bandwidth. (Feedforward is not used for non-inverting or differential applications.)

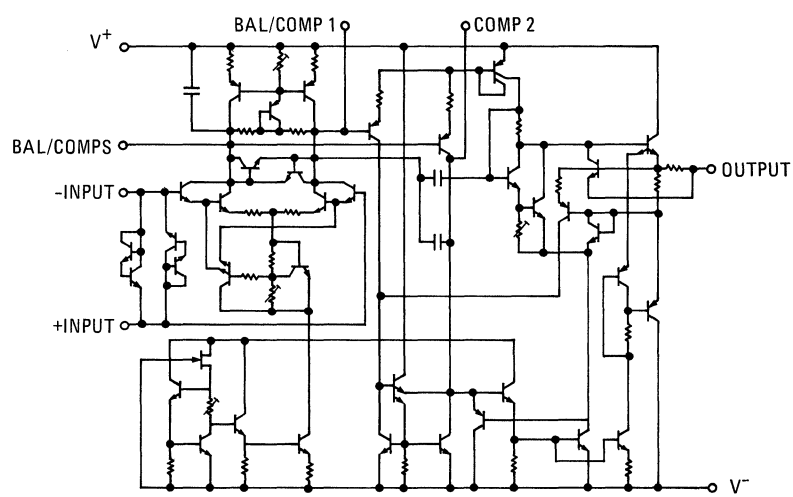
Their high speed and fast settling time make them ideal devices for A/D converters, oscillators, active filters, sample-and-hold circuits, as well as general purpose amplifiers.

The LM118 military version operates over a temperature range of −55°C to +125°C. The LM218 is the same as the LM118 except its performance is guaranteed from −25°C to +85°C. The LM318 operates from 0°C to +70°C.

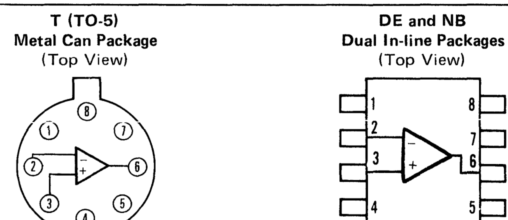
DESIGN FEATURES

- 15MHz Small Signal Bandwidth
- Guaranteed 50V/μs Slew Rate
- Operates from ±5V to ±20V Supply
- Internal Frequency Compensation
- Input and Output Overload Protected
- Pin Compatible With General Purpose Op Amps

SCHEMATIC DIAGRAM



CONNECTION INFORMATION



Order Part Nos.:
LM118H, LM218H, LM318H

Order Part Nos.:
LM118DE, LM218DE,
LM318DE, LM318N

PIN	FUNCTION
1	BAL/COMP 1
2	−INPUT
3	+INPUT
4	V−
5	BAL/COMP 3
6	OUTPUT
7	V+
8	COMP 2

NOTE: THE LM118/318 IS AVAILABLE ON SPECIAL ORDER IN THE DC (14-PIN) CERAMIC DIP AND CQ (10-PIN) FLATPAK PACKAGES.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V	Operating Temperature Range	
Power Dissipation (Note 1)	500mW	LM118	-55°C to +125°C
Differential Input Current (Note 2)	±10mA	LM218	-25°C to +85°C
Input Voltage (Note 3)	±15	LM318	0°C to +70°C
Output Short-Circuit Duration	Indefinite	Storage Temperature Range	-65°C to +150°C
		Lead Temperature (Soldering, 10s)	+300°C

ELECTRICAL CHARACTERISTICS (Note 4)

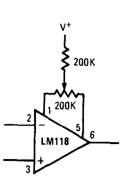
PARAMETER	CONDITIONS	LM118/LM218	LM318	UNITS	
Input Offset Voltage	T_A = 25°C	4	10	mV	Max.
Input Offset Current	T_A = 25°C	50	200	nA	Max.
Input Bias Current	T_A = 25°C	250	500	nA	Max.
Input Resistance	T_A = 25°C	1	0.5	MΩ	Min.
Supply Current	T_A = 25°C	8	10	mA	Max.
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V, V_{OUT} = ±10V, $R_L \geq$ 2k	50	25	V/mV	Min.
Input Offset Voltage		6	15	mV	Max.
Small Signal Bandwidth	T_A = 25°C, V_S = ±15V	15	15	MHz	Typ.
Slew Rate	T_A = 25°C, V_S = ±15V, A_V = 1, R_S = 10kΩ	50	50	V/µs	Min.
Input Offset Current		100	300	nA	Max.
Input Bias Current		500	750	nA	Max.
Supply Current	$T_A = T_{MAX}$	7		mA	Max.
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq$ 2k	25	20	V/mV	Min.
Output Voltage Swing	V_S = ±15V, R_L = 2kΩ	±12	±12	V	Min.
Input Voltage Range	V_S = ±15V	±11.5	±11.5	V	Min.
Common Mode Rejection Ratio		80	70	dB	Min.
Supply Voltage Rejection Ratio		70	65	dB	Min.

NOTES:

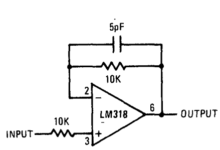
1. The maximum junction temperature of the LM118 is +150°C, LM218 is +100°C and +85°C for the LM318. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.
2. The inputs are shunted with shunt diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
3. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
4. These specifications apply for ±5V $\leq V_S \leq$ ±20V and -55°C $\leq T_A \leq$ +125°C for the LM118; ±5V $\leq V_S \leq$ ±20V and -20°C $\leq T_A \leq$ +85°C for the LM218; ±5V $\leq V_S \leq$ ±20V and 0°C $\leq T_A \leq$ +70°C for the LM318. Also, power supplies must be bypassed with 0.1 µF ceramic disc capacitors.

TYPICAL APPLICATIONS

Offset Balancing

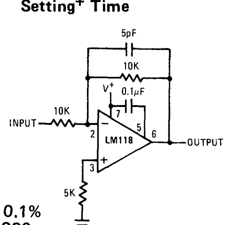


Fast Voltage Follower

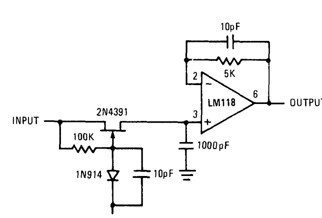


+Slew and setting time to 0.1% for a 10V step change is 800ns.

Compensation for Minimum Setting+ Time

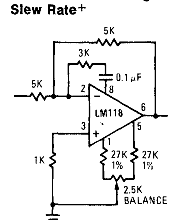


Fast Sample and Hold



+Slew rate typically 150V/µs

Feedforward Compensation for Greater Inverting Slew Rate+



Quad Single-Supply Operational Amplifiers

GENERAL DESCRIPTION

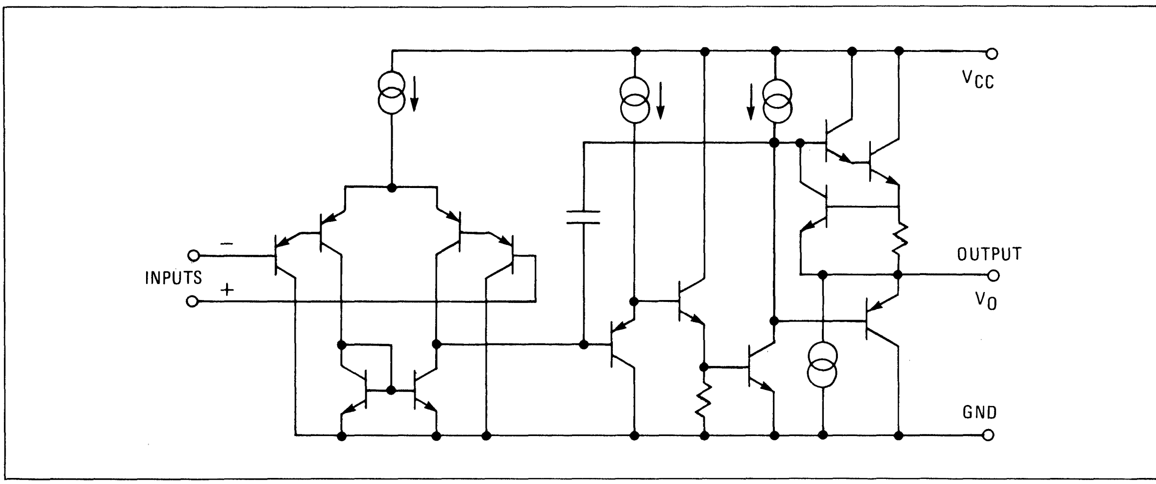
Each of the devices in this series consists of four independent, high-gain, operational amplifiers that are designed for single-supply operation. Operation from split power supplies is also possible and the low power supply drain is independent of the magnitude of the power supply voltage.

Used with a dual supply, the circuit will operate over a wide range of supply voltages. However, a large amount of crossover distortion may occur with loads to ground. An external current-sinking resistor to $-V_{CC}$ will reduce crossover distortion. There is no crossover distortion problem in single supply operation if the load is direct-coupled to ground.

DESIGN FEATURES

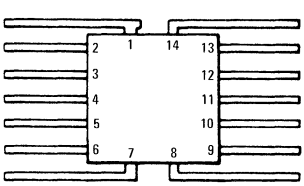
- Large DC Voltage Gain 100 dB
- Compatible with All Forms of Logic
- Temperature Compensated
- Wide Bandwidth at Unity Gain Frequency 1 MHz
- Large Output Voltage Swing: 0 V_{DC} to V^+ −1.5 V_{DC}
- Input Common Mode Voltage Range Includes Ground

SCHEMATIC DIAGRAM (1/4 Shown)



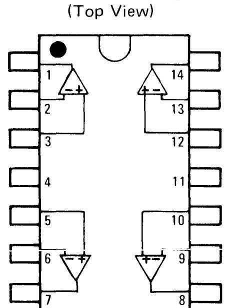
CONNECTION INFORMATION

CJ Flatpak
(Top View)



Order Part No.:
LM124F, LM124AF

DB and DC
Dual In-Line Packages
(Top View)



Order Part Nos.:
LM124J, LM224J, LM324J, LM2902J,
LM224N, LM324N, LM2902N,
LM124AJ, LM224AJ, LM324AJ,
LM224AN, LM324AN

PIN	FUNCTION
1	OUTPUT 1
2	−INPUT 1
3	+INPUT 1
4	V^+
5	+ INPUT 2
6	− INPUT 2
7	OUTPUT 2
8	OUTPUT 3
9	− INPUT 3
10	+ INPUT 3
11	GROUND
12	+ INPUT 4
13	− INPUT 4
14	OUTPUT 4

ABSOLUTE MAXIMUM RATINGS

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	-0.3 V_{DC} to +32 V_{DC}	-0.3 V_{DC} to +32 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	800 mW	
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15$ V_{DC} and $T_A = 25°C$	Continuous	Continuous

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Input Current ($V_{IN} < -0.3$ V_{OL}) (Note 3)	50 mA	
Operating Temperature Range		-40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	-25°C to +85°C	
LM124/LM124A	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

ELECTRICAL CHARACTERISTICS ($V^+ = +5.0$ V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30$ V_{DC}, $T_A = 25°C$	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	V_{DC}
Supply Current	$R_L = \infty$, $V_{CC} = 30V$, (LM2902 $V_{CC} = 26V$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA_{DC}
	$R_L = \infty$ On All Op Amps		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
	Over Full Temperature Range																			
	$T_A = 25°C$																		3	mA_{DC}
Large Signal Voltage Gain	$V^+ = 15$ V_{DC} (For Large V_O Swing) $R_L \geq 2$ kΩ, $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2$ kΩ, $T_A = 25°C$ (LM2902 $R_L \geq 10$ kΩ)										0		V^+-1.5	0		V^+-1.5	0		V^+-1.5	V_{DC}
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)		-120			-120			-120			-120			-120			-120		dB
Output Current Source	$V_{IN^+} = 1$ V_{DC}, $V_{IN^-} = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
Output Current Sink	$V_{IN^-} = 1$ V_{DC}, $V_{IN^+} = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	$V_{IN^-} = 1$ V_{DC}, $V_{IN^+} = 0$ V_{DC}, $T_A = 25°C$, $V_O = 200$ mV_{DC}	12	50		12	50		12	50		12	50		12	50					μA_{DC}
Short Circuit to Ground	$T_A = 25°C$, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}

ELECTRICAL CHARACTERISTICS (CONT)

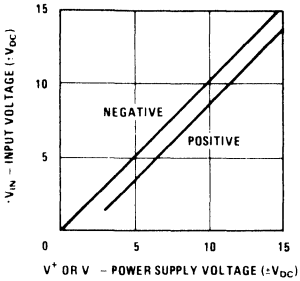
PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	20		7	20		7	30		7			7			7		$\mu V/°C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		$pA_{DC}/°C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \leq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current																				
Source	$V_{IN^+} = +1\ V_{DC}$, $V_{IN^-} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA
Sink	$V_{IN^-} = +1\ V_{DC}$, $V_{IN^+} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA
Differential Input Voltage	(Note 7)			V^+			V^+			V^+			V^+			V^+			V^+	V_{DC}

NOTES:

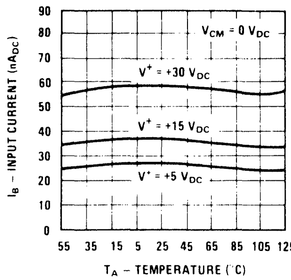
1. For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers — use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC}.
4. These specifications apply for $V^+ = +5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM224/LM224A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2902 specifications are limited to $-40°C \leq T_A \leq +85°C$.
5. $V_O \approx 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full common-mode range (0 V_{DC} to V^+ −1.5 V_{DC}).
6. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
7. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+-1.5V, but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902).
8. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

TYPICAL PERFORMANCE CHARACTERISTICS

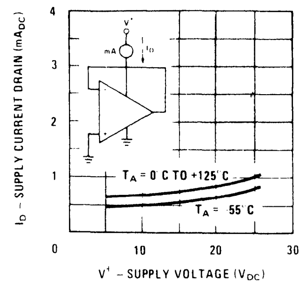
Input Voltage Range



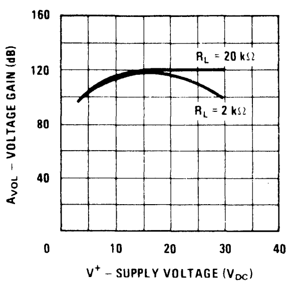
Input Current



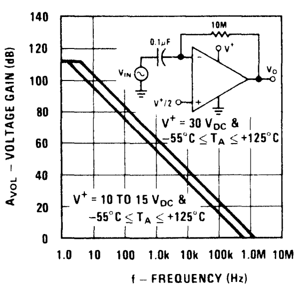
Supply Current



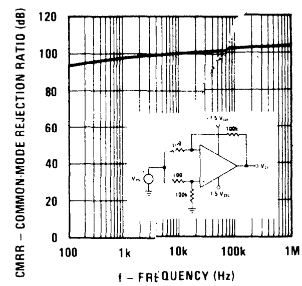
Voltage Gain



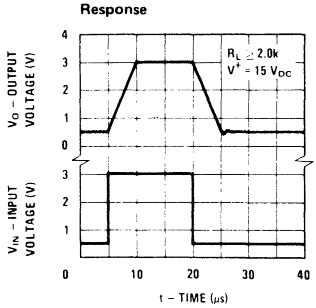
Open Loop Frequency Response



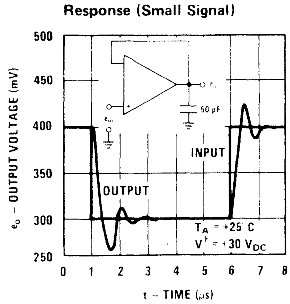
Common Mode Rejection Ratio



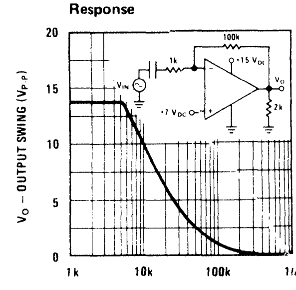
Voltage Follower Pulse Response



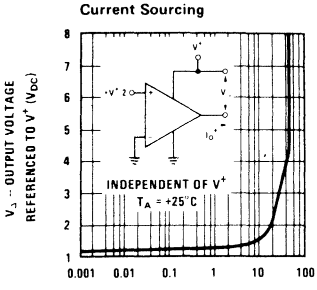
Voltage Follower Pulse Response (Small Signal)



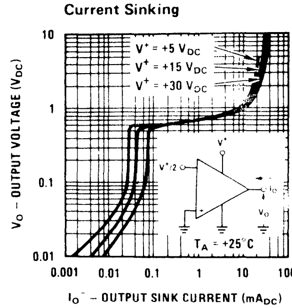
Large Signal Frequency Response



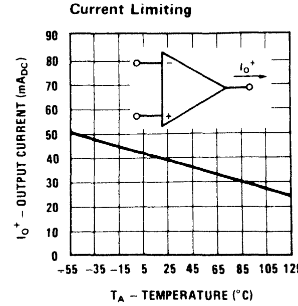
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



148/149 248/249 348/349 Low Power Quad 741 Operational Amplifiers

DESCRIPTION

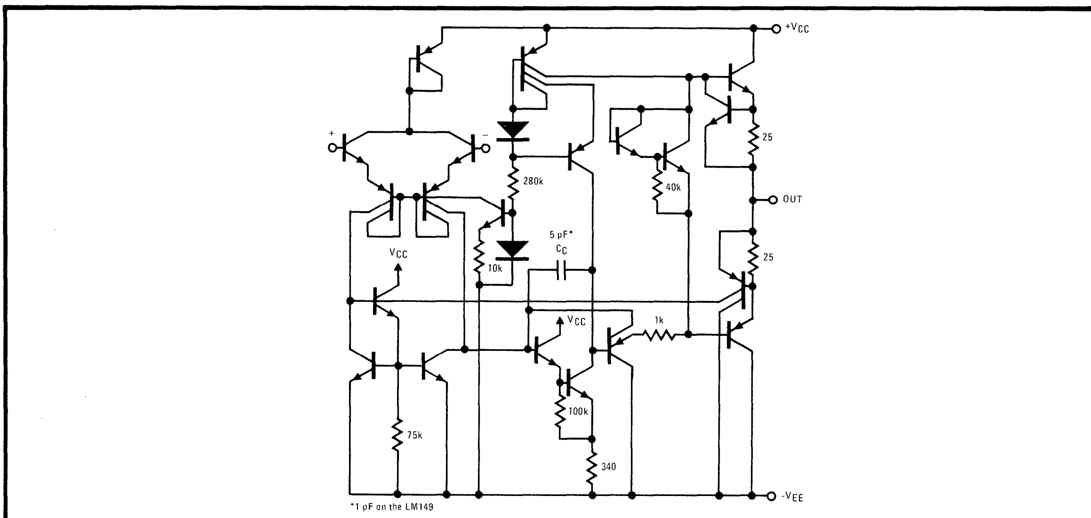
The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 series has the same features as the LM148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

FEATURES

- 741 op amp operating characteristics
- Low supply current drain (0.6 mA/Amplifier)
- Class AB output stage - no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage (1 mV)
- Low input offset current (4 nA)
- Low input bias current (30 nA)
- Gain bandwidth product: LM148 (unity gain) (1.0 MHz)
  LM149 ($A_V \geqslant 5$) (4 MHz)
- High degree of isolation between amplifiers (120 dB)
- Overload protection for inputs and outputs

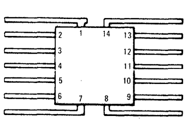
SCHEMATIC DIAGRAM (1/4 Shown)



*1 pF on the LM149

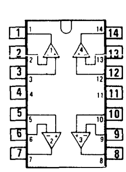
CONNECTION INFORMATION

CJ Flatpak
(Top View)



Order Part Nos.:
LM148F, LM149F,
LM148J, LM248J, LM348J,
LM248N, LM348N,
LM149J, LM249J, LM349J,
LM149N, LM349N

DC and DB Dual In-Line Packages
(Top View)



PIN	FUNCTION
1	OUTPUT A
2	$-V_{IN}$ A
3	$+V_{IN}$ A
4	V+
5	$+V_{IN}$ B
6	$-V_{IN}$ B
7	OUTPUT B
8	OUTPUT C
9	$-V_{IN}$ C
10	$+V_{IN}$ C
11	V-
12	$+V_{IN}$ D
13	$-V_{IN}$ D
14	OUTPUT D

HIGH RELIABILITY OPTIONS

Part Number	Screening
LM148J03	MIL-STD-883 Class B
LM248J03*, LM348J03	Raytheon A+3 screening including Burn-in and tightened AQL
LM248N02*, LM348N02	Raytheon A+2 screening including temp cycles, Burn-in, "Hot Rail" testing and tightened AQL
LM248N01*, LM348N01	Raytheon A+1 screening including temp cycles, "Hot Rail" testing and tightened AQL

*Complete details are shown in the quality section of this catalog.

RAYTHEON

Low Power Quad 741 Operational Amplifiers

148/149 248/249 348/349

ABSOLUTE MAXIMUM RATINGS

		LM148/LM149	LM248/LM249	LM348/LM349
Supply Voltage		±22V	±18V	±18V
Differential Input Voltage		±44V	±36V	±36V
Input Voltage		±22V	±18V	±18V
Output Short Circuit Duration (Note 1)		Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}) (Note 2)				
Molded DIP (N)	P_d	–	–	500 mW
	θ_{jA}	–	–	150°C/W
Cavity DIP (D) (J)	P_d	900 mW	900 mW	900 mW
	θ_{jA}	100°C/W	100°C/W	100°C/W
Flat Pack (CJ)	P_d	675 mW	–	–
	θ_{jA}	185°C/W	–	–
Maximum Junction Temperature (T_{jMAX})		150°C	110°C	100°C
Operating Temperature Range		$-55°C \leqslant T_A \leqslant +125°C$	$-25°C \leqslant T_A \leqslant +85°C$	$0°C \leqslant T_A \leqslant +70°C$
Storage Temperature Range		-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering 60 seconds)		300°C	300°C	300°

ELECTRICAL CHARACTERISTICS (See Note 3)

PARAMETER	CONDITIONS	LM148/149 MIN	LM148/149 TYP	LM148/149 MAX	LM248/249 MIN	LM248/249 TYP	LM248/249 MAX	LM348/349 MIN	LM348/349 TYP	LM348/349 MAX	UNITS
Input Offset Voltage	T_A = 25°C, $R_S \leqslant 10$ kΩ		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	T_A = 25°C		4	25		4	50		4	50	nA
Input Bias Current	T_A = 25°C		30	100		30	200		30	200	nA
Input Resistance	T_A = 25°C	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	T_A = 25°C, V_S = ±15V		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, $R_L \geqslant 2$ kΩ	50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz to 20 kHz		-120			-120			-120		dB
Small Signal Bandwidth	T_A = 25°C, LM148		1.0			1.0			1.0		MHz
	T_A = 25°C, LM149		4.0			4.0			4.0		MHz
Phase Margin	T_A = 25°C, LM148(A_V=1)		60			60			60		degrees
	T_A = 25°C, LM149(A_V=5)		60			60			60		degrees
Slew Rate	T_A = 25°C, LM148(A_V=1)		0.5			0.5			0.5		V/µs
	T_A = 25°C, LM149(A_V=5)		2.0			2.0			2.0		V/µs
Output Short Circuit Current	T_A = 25°C		25			25			25		mA
Input Offset Voltage	$R_S \leqslant 10$ kΩ			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA
Input Bias Current				325			500			400	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L >2 kΩ	25			15			15			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13		±12	±13		±12	±13		V
	R_L = 2 kΩ	±10	±12		±10	±12		±10	±12		V
Input Voltage Range	V_S = ±15V	±12			±12			±12			V
Common Mode Rejection Ratio	$R_S \leqslant 10$ kΩ	70	90		70	90		70	90		dB
Supply Voltage Rejection	$R_S \leqslant 10$ kΩ	77	96		77	96		77	96		dB

Note 1: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: These specifications apply for V_S = ±15V and over the absolute maximum operating temperature range ($T_L \leqslant T_A \leqslant T_H$) unless otherwise noted.

APPLICATION GUIDES

The 148 series are low power quad operational amplifiers that exhibit performance comparable to the popular 741. Substitution can therefore be made with no change in circuit behavior.

The 149 series is similar to the 148 except it is decompensated to yield a wider gain-bandwidth product. Consequently, it must be operated at a minimum closed loop gain of 5.

The input characteristics of these devices allow differential voltages which exceed the supplies. Output phase will be correct as long as one of the inputs are within the operating common mode range. If both exceed the negative limit, the output will latch positive. Current limiting resistors should be used on the inputs in case voltages become excessive.

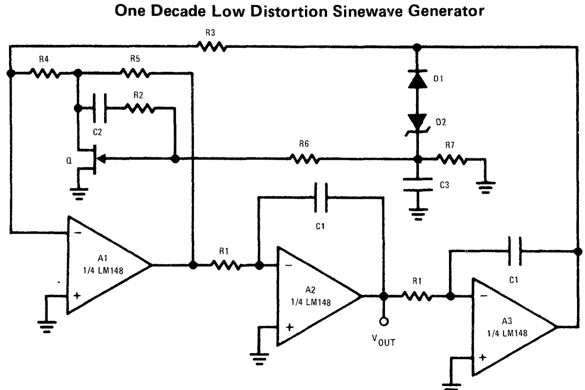
When capacitive loading becomes much greater than 100 pf, a resistor should be placed between the output and feedback connection in order to reduce phase shift.

The 148/149 series is short circuit protected to either ground or the supplies continuously when only one of the four amplifiers are shorted. If multiple shorts occur simultaneously, the unit can be destroyed due to excessive power dissipation.

To assure stability, feedback resistors should be placed close to the input to maximize the feedback pole frequency (function of input to ground capacitance) and to minimize pickup. A good rule of thumb is that the feedback pole frequency should be 6 times the operating 3 dB frequency. If less, a lead capacitor should be placed between the output and input.

TYPICAL APPLICATIONS

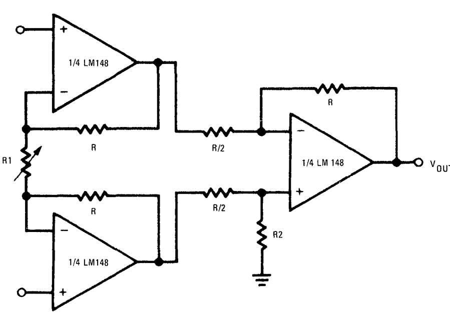
One Decade Low Distortion Sinewave Generator



$$f = \frac{1}{2\pi R1C1} \times \sqrt{K},\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\ r_{DS} \cong \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

f_{MAX} = 5 kHz, THD ⩽ 0.03%
R1 = 100k pot., C1 = 0.0047µF, C2 = 0.01µF, C3 = 0.1µF, R2 = R6 = R7 = 1M, R3 = 5.1k, R4 = 12Ω, R5 = 240Ω, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V
A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Low Cost Instrumentation Amplifier

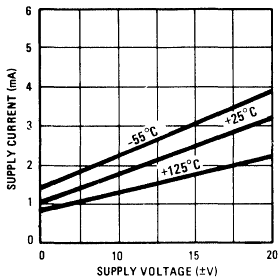


$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right),\ V_S^- - 3V \leqslant V_{IN\ CM} \leqslant V_S^+ - 3V,$$

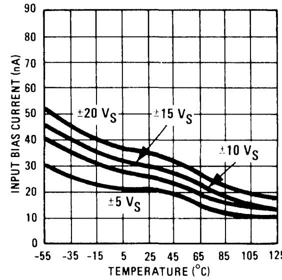
V_S = ±15V

R = R2, trim R2 to boost CMRR

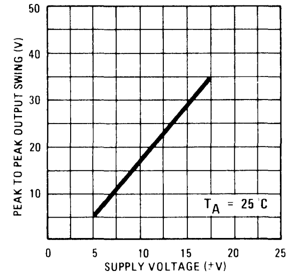
TYPICAL PERFORMANCE DATA



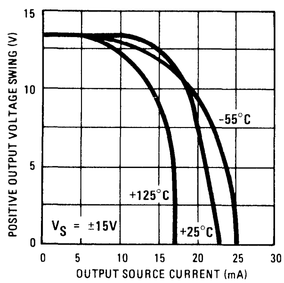
Supply Current vs Supply Voltage



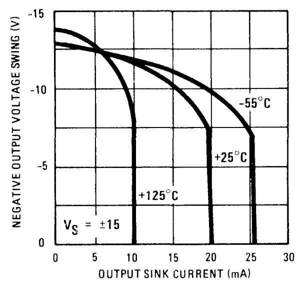
Input Bias Current vs Temperature



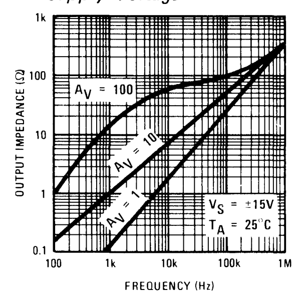
Voltage Swing vs Supply Voltage



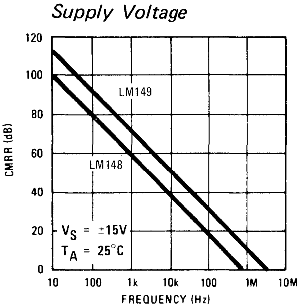
Positive Current Limit vs Supply Voltage



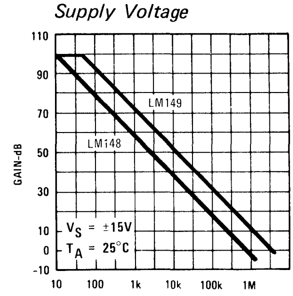
Negative Current Limit vs Supply Voltage



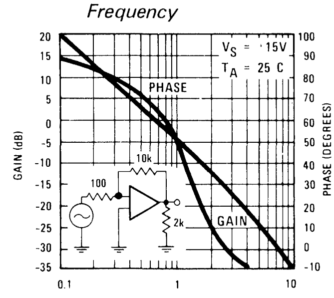
Output Impedance vs Frequency



Common-Mode Rejection Ratio vs Frequency

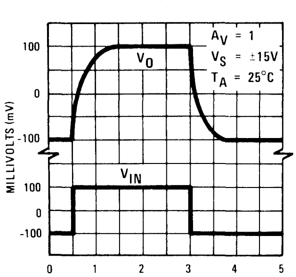


Open Loop Frequency Response

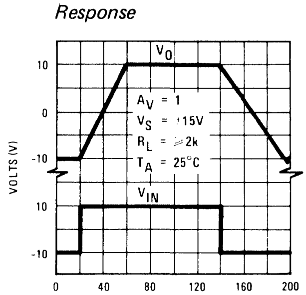


LM148

Phase Margin vs Frequency

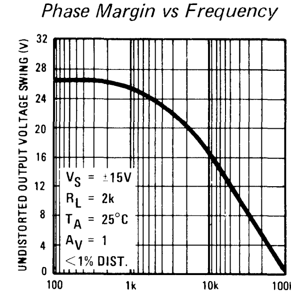


Small Signal Pulse Response



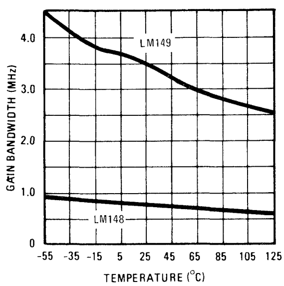
LM148

Large Signal Pulse Response

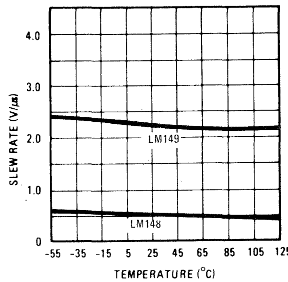


Undistorted Output Voltage Swing vs Frequency

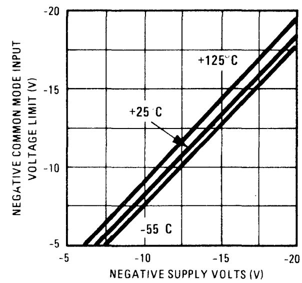
TYPICAL PERFORMANCE DATA (CONT)



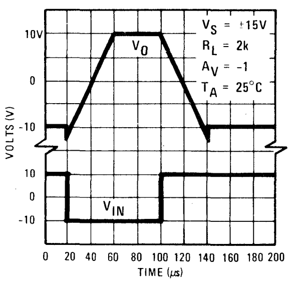
Gain Bandwidth vs Temperature



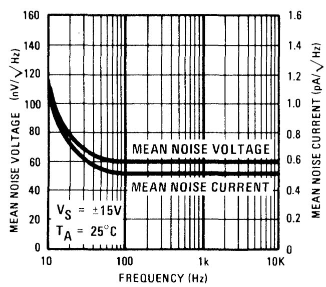
Slew Rate vs Temperature



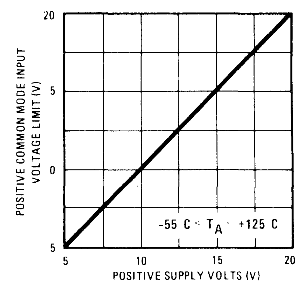
Negative Common-Mode Input Voltage Limit



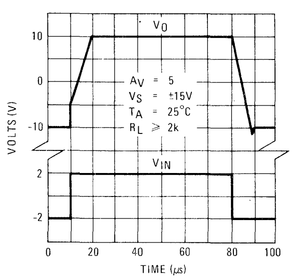
Inverting Large Signal Pulse Response (LM148)



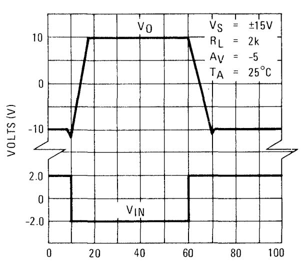
Input Noise Voltage and Noise Current



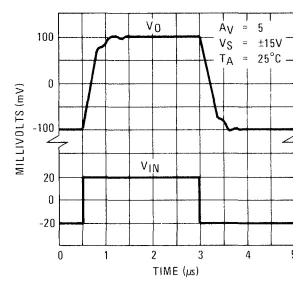
Positive Common-Mode Input Voltage Limit



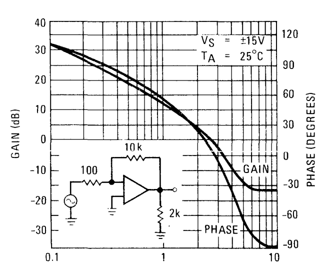
Large Signal Pulse Response (LM149)



Inverting Large Signal Pulse Response (LM149)



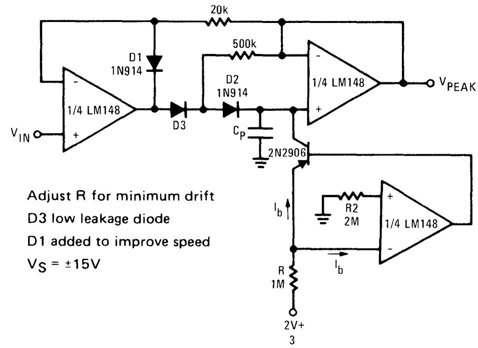
Small Signal Pulse Response (LM149)



Bode Plot LM149

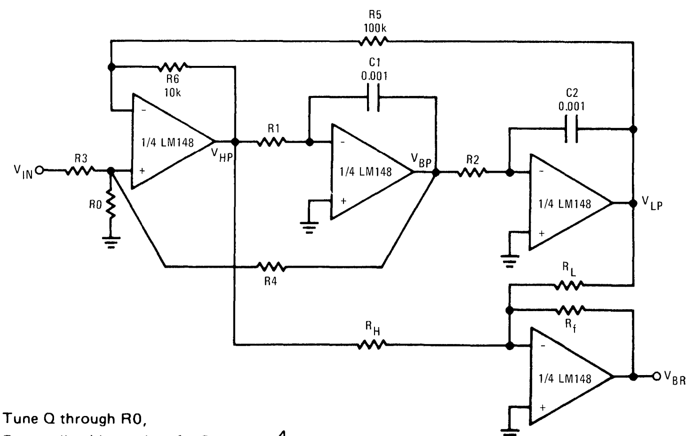
TYPICAL APPLICATIONS–LM148

Low Drift Peak Detector with Bias Current Compensation



Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
$V_S = \pm 15V$

Universal State-Space Filter



Tune Q through R0,
For predictable results: $f_O\, Q \leq 4 \times 10^4$
Use Band Pass output to tune for Q

$$\frac{V(s)}{V_{IN}(s)} = \frac{N(s)}{D(s)}, \quad D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o^{\,2}$$

$$N_{HP}(s) = S^2 H_{OHP}, \quad N_{BP}(s) = \frac{-S\omega_O H_{OBP}}{Q} \qquad N_{LP} = \omega_o^{\,2} H_{OLP}$$

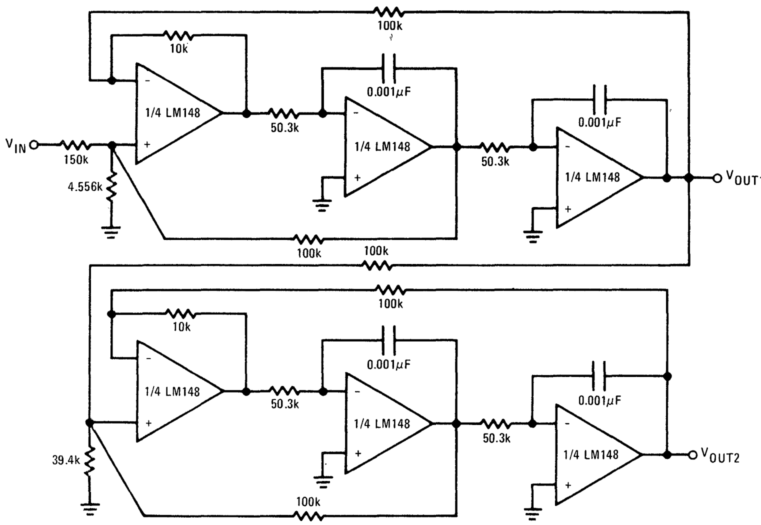
$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\sqrt{\frac{1}{t1\,t2}}, \quad t_i = R_i C_i, \quad Q = \left(\frac{1 + R4/R3 + R4/R0}{1 + R6/R5}\right)\left(\frac{R6}{R5}\,\frac{t_1}{t_2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L t_1 t_2}\right)^{1/2}, \quad H_{OHP} = \frac{1 + R6/R5}{1 + R3/R0 + R3/R4}, \quad H_{OBP} = \frac{1 + R4/R3 + R4/R0}{1 + R3/R0 + R3/R4}$$

$$H_{OLP} = \frac{1 + R5/R6}{1 + R3/R0 + R3/R4}$$

TYPICAL APPLICATIONS LM148 (CONT)

A 1 kHz 4 Pole Butterworth

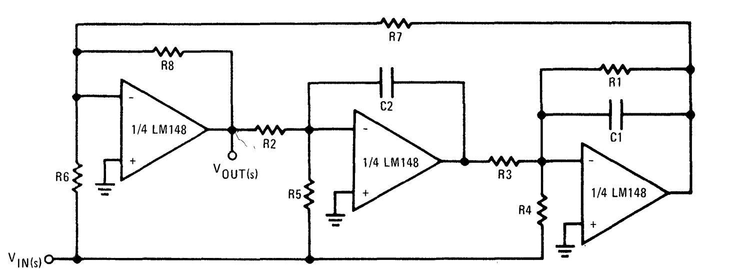


Use general equations, and tune each section separately

$Q_{1stSECTION} = 0.541$, $Q_{2ndSECTION} = 1.306$

The response should have 0 dB peaking

A 3 Amplifier Bi-Quad Notch Filter



$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}}, \quad f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}}, \quad f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

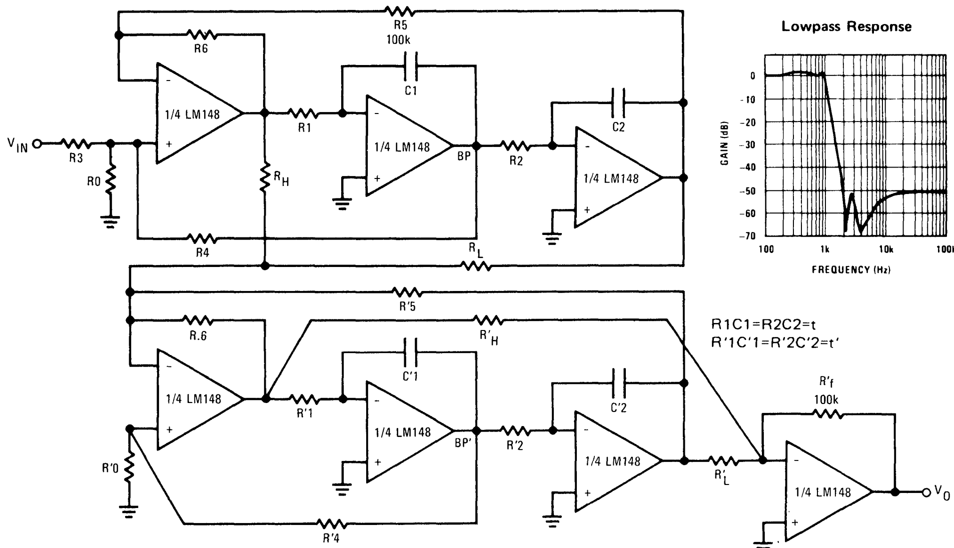
Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: f_{NOTCH} = 3 kHz, Q = 5, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001µF

Better noise performance than the state-space approach

TYPICAL APPLICATIONS LM148 (CONT)

A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)



f_C = 1 kHz, f_S = 2 kHz, f_P = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z ≈ 4.92, Q' = 4.403, normalized to ripple BW

$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t},\ f_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}} \times \frac{1}{t},\ Q = \left(\frac{1 + R4/R3 + R4/R0}{1 + R6/R5}\right) \times \sqrt{\frac{R6}{R5}},\ Q' = \sqrt{\frac{R'6}{R'5}}\ \frac{1 + R'4/R'0}{1 + R'6/R'5 + R'6/R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

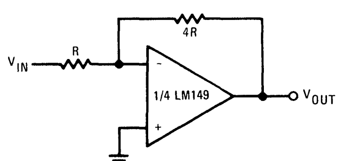
Use the BP outputs to tune Q, Q', tune the 2 sections separately

R1 = R2 = 92.6k, R3 = R4 = R5 = 100k, R6 = 10k, R0 = 107.8k, R_L = 100k, R_H = 155.1k,

R'1 = R'2 = 50.9k, R'4 = R'5 = 100k, R'6 = 10k, R'0 = 5.78k, R'_L = 100k, R'_H = 248.12k, R'f = 100k. All capacitors are 0.001μF.

TYPICAL APPLICATIONS—LM149

Minimum Gain to Insure LM149 Stability



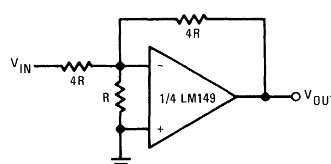
$$A_{CL(S)} = \frac{V_{OUT}}{V_{IN}} = \frac{-4}{\left(1 + \frac{5}{A_{OL(s)}}\right)} \cong -4$$

$$V_O\Big|_{V_{IN}=0} \cong \pm 5\ V_{OS}$$

Power BW = 40 kHz

Small Signal BW = G BW/5

The LM149 as a Unity Gain Inverter



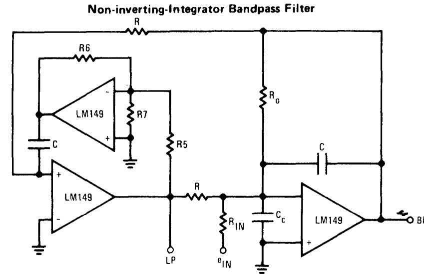
$$A_{CL(s)} = \frac{V_{OUT}}{V_{IN}} = \left(\frac{-1}{1 + \frac{6}{A_{OL(s)}}}\right) \cong -1$$

$$V_O\Big|_{V_{IN}=0} \cong \pm 5\ V_{OS}$$

Small signal BW = G BW/5

TYPICAL APPLICATIONS—LM149 (CONT)

Non-inverting-Integrator Bandpass Filter



For stability purposes: $R7 = R6/4$, $10R6 = R5$, $C_C = 10C$

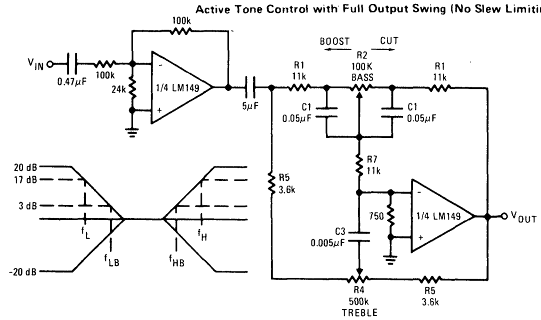
$$f_O = \frac{1}{2\pi}\sqrt{\frac{R5}{R6}} \times \frac{1}{RC}, \quad Q = \frac{R_Q}{R}\sqrt{\frac{R5}{R6}}, \quad Ho_{BP} = \frac{R_Q}{R_{IN}}$$

$(f_{O(MAX)}, Q_{MAX}) = 20$ kHz, 10

Better Q sensitivity with respect to open loop gain variations than the state variable filter.

R7, C_C added for compensation

Active Tone Control with Full Output Swing (No Slew Limiting at 20 kHz)



$V_S = \pm 15V$, $V_{OUT(MAX)} = 9.1\ V_{RMS}$, $f_{MAX} = 20$ kHz, THD $\leq 1\%$

Duplicate the above circuit for stereo

$$f_L = \frac{1}{2\pi R2C1}, \quad f_{LB} = \frac{1}{2\pi R1C1}$$

$$f_H = \frac{1}{2\pi R5C3}, \quad f_{HB} = \frac{1}{2\pi(R1 + 2R7)C3}$$

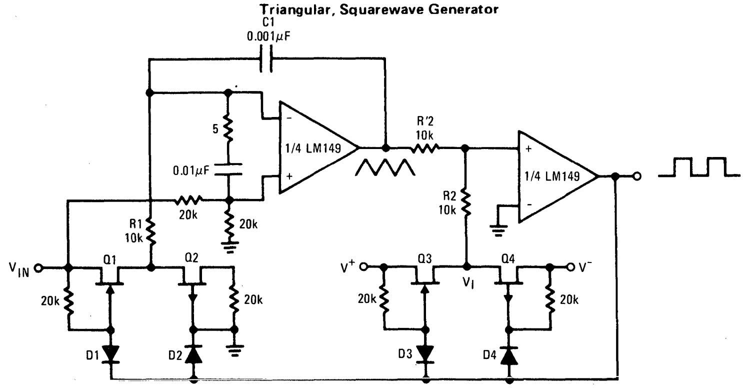
Max Bass Gain $\cong (R1 + R2)/R1$

Max Treble Gain $\cong (R1 + 2R7)/R5$

as shown: $f_L \cong 32$ Hz, $f_{LB} \cong 320$ Hz

$f_H \cong 11$ kHz, $f_{HB} \cong 1.1$ Hz

Triangular, Squarewave Generator



$$f = \frac{K \times V_{IN}}{8V^+C1\,R1}, \quad K = R2/R'2, \quad \frac{2V_I}{K} \leq 25V, \quad V^+ = V^-, \quad V_S = \pm 15V$$

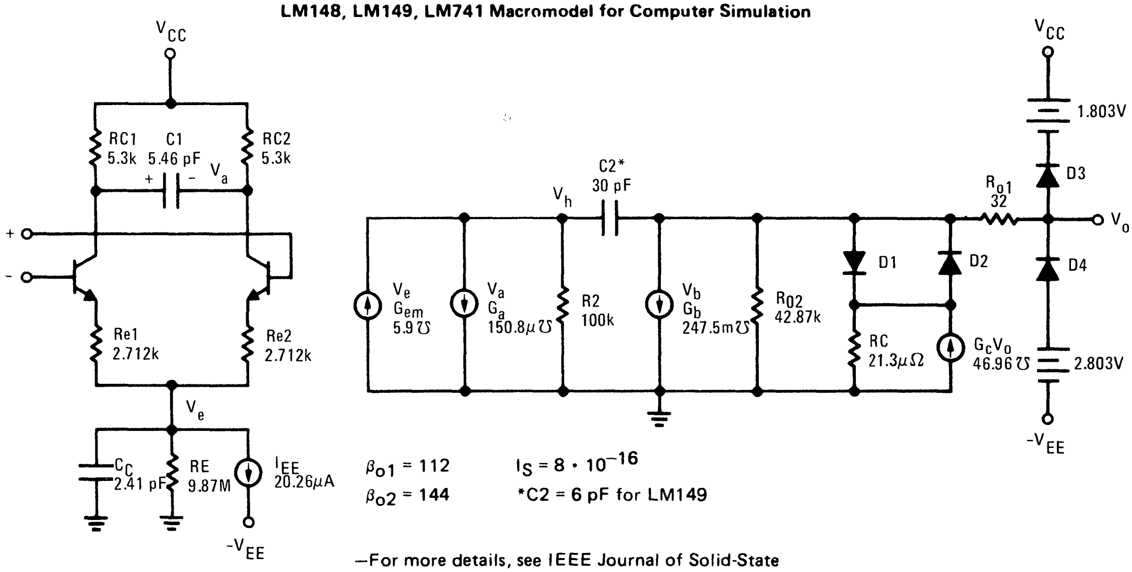
Use LM125 for ±15V supply

The circuit can be used as a low frequency V/F for process control.

Q1, Q3: KE4393, Q2, Q4: P1087E, D1–D4 = 1N914

TYPICAL SIMULATION

LM148, LM149, LM741 Macromodel for Computer Simulation



$\beta_{o1} = 112$ $\quad I_S = 8 \cdot 10^{-16}$

$\beta_{o2} = 144$ $\quad$ *C2 = 6 pF for LM149

—For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974

Monolithic JFET Input Operational Amplifiers

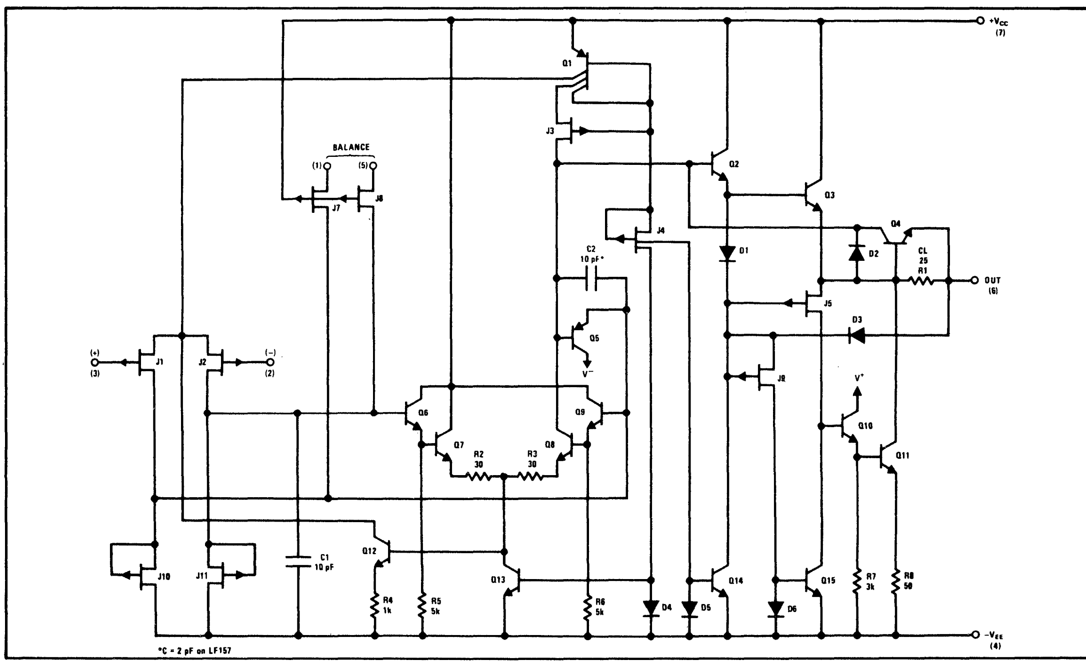
GENERAL DESCRIPTION

The LF155A, 156A and 157A family is composed of JFET input operational amplifiers which by using advanced processing techniques, contain both bipolar transistors and closely matched JFET's on the same chip. The resulting amplifiers feature low input offset voltage and offset voltage drift, low input bias and offset current, and low noise. These devices also feature wide bandwidth, high slew rate and fast settling time making them extremely versatile in such applications as A/D and D/A conversion, sample and hold circuits; analog function circuits, active filters and instrumentation circuits.

DESIGN FEATURES

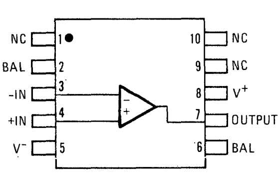
- Low input offset voltage – 1 mV
- Low input offset current – 3 pA
- Low input bias current – 30 pA
- Low input noise voltage – 12 nV/$\sqrt{Hz}$ 156A,157A
  20 nV/$\sqrt{Hz}$ 155A
- Low input noise current – 0.01 pA/$\sqrt{Hz}$
- High DC voltage gain – 200,000 V/V

SCHEMATIC DIAGRAM



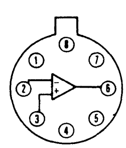
CONNECTION INFORMATION

CQ Flat Package
(Top View)



Order Part Nos.:
LF155AF, LF155F,
LF156AF, LF156F,
LF157AF, LF157F

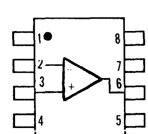
T (TO-99)
Metal Can Package
(Top View)



Note 4: Pin 4 connected to case.

Order Part Nos.:
LF155AH, LF355AH, LF156AH,
LF356AH, LF157AH, LF357AH,
LF155H, LF255H, LF355H, LF156H,
LF256H, LF356H, LF157H, LF257H,
LF357H

DE and NB
Dual In-line Packages
(Top View)



Order Part Nos.:
LF155ADE, LF355ADE, LF156ADE,
LF356ADE, LF157ADE, LF357ADE,
LF155DE, LF255DE, LF355DE, LF156DE,
LF256DE, LF356DE, LF157DE, LF257DE,
LF357DE, LF355AN, LF356AN, LF357AN,
LF355N, LF356N, LF357N

PIN	FUNCTION
1	COMP/BAL
2	–INPUT
3	+INPUT
4	V–
5	BAL
6	OUTPUT
7	V+
8	COMP

ABSOLUTE MAXIMUM RATINGS

	LF155A/6A/7A	LF355A/6A/7A	LF155/6/7	LF255/6/7	LF355/6/7
Supply Voltage	±22V	±22V	±22V	±22V	±18V
Power Dissipation (Note 1) TO-99 (H package)	670 mW	500 mW	670 mW	570 mW	500 mW
Operating Temperature Range	-55 to +125°C	0 to +70°C	-55 to +125°C	-25 to +85°C	0 to +70°C
$T_{j(MAX)}$	150°C	100°C	150°C	110°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	-65 to +150°C	-65 to +150°C	-65 to +150°C	-65 to +150°C	-65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C	300°C

Note: LF157A, 357A, 157, 257, 357 are decompensated for use in circuits with $A_V \geq 5$ only.

DC ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	LF155A/156A/157A MIN	TYP	MAX	LF355A/356A/357A MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ KΩ		1.0	2.0		1.0	2.0	mV
Input Offset Current			3	10		3	10	pA
Input Bias Current			30	50		30	50	pA
Input Resistance			10^6			10^6		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ KΩ V_{OUT} ±10V	50K	200K		50K	200K		V/V
The following specifications apply for -55°C ≤ T_A ≤ +125°C for LF155A/156A/157A; 0°C ≤ T_A ≤ +70°C for LF355A/356A/357A.								
Input Offset Voltage	$R_S \leq 10$ KΩ			2.5			2.3	mV
Input Offset Current				10			1.0	nA
Input Bias Current				25			5	nA
Large Signal Voltage Gain	$R_L \geq 2$ KΩ V_{OUT} ±10V	25K			25K			V/V
Output Voltage Swing	$R_L \geq 10$ KΩ	±12	±13		±12	±13		V
Average Offset Voltage Drift			3	5		3	5	μV/°C
Common Mode Rejection Ratio	$R_S \leq 10$ KΩ ΔV ±5V	85	100		85	100		dB
Power Supply Rejection Ratio	$R_S \leq 10$ KΩ ΔV ±5V	85	100		85	100		dB
Input Voltage Range		±11	+15.1 -12		±11	+15.1 -12		V

AC ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	LF155A/355A MIN	TYP	MAX	LF156A/356A MIN	TYP	MAX	LF157A/357A MIN	TYP	MAX	UNITS
Gain Bandwidth Product			2.5		4.0	4.5		15	20		MHz
Settling Time	To 0.01%		4			1.5			1.5		μs
Slew Rate	LF155A/156A: $A_V = 1$ LF157A: $A_V = 5$	3	5		10	12		40	50		V/μs
Input Capacitance			3			3			3		pF
Input Noise Current	F = 100 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$
	F = 1 kHz		0.01			0.01			0.01		pA/$\sqrt{Hz}$
Input Noise Voltage (R_S = 100Ω)	F = 100 Hz		25			15			15		nV/$\sqrt{Hz}$
	F = 1 kHz		20			12			12		nV/$\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$

PARAMETER	LF155A/355A LF155/255		LF355		LF156A/356A LF156/256		LF356		LF157A/357A LF157/257		LF357		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current	2	4	2	4	5	7	5	10	5	7	5	10	mA

DC ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	·CONDITIONS	LF155/156/157			LF255/256/257			LF355/356/357			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ K\Omega$		3	5		3	5		3	10	mV
Input Offset Current			3	20		3	20		3	50	pA
Input Bias Current			30	100		30	100		30	200	pA
Input Resistance			10^6			10^6			10^6		MΩ
Large Signal Voltage Gain	$R_L \geq 2\ K\Omega$ V_{OUT} ±10V	50K	200K		50K	200K		25K	200K		V/V
The following specifications apply for -55°C ≤ T_A ≤ +125°C for LF155/156/157; -25°C ≤ T_A ≤ +85°C for LF255/256/257; 0°C ≤ T_A ≤ +70°C for LF355/356/357.											
Input Offset Voltage	$R_S \leq 10\ K\Omega$			7			6.5			13	mV
Input Offset Current				20			1			2	nA
Input Bias Current				50			5			8	nA
Large Signal Voltage Gain	$R_L \geq 2\ K\Omega$ V_{OUT} ±10V	25K			25K			15K			V/V
Output Voltage Swing	$R_L \geq 10\ K\Omega$	±12	±13		±12	± 13		± 12	±13		V
Average Offset Voltage Drift			5			5			5		μV/°C
Common Mode Rejection Ratio	$R_S \leq 10\ K\Omega$ ΔV ±5V	85	100		85	100		80	100		dB
Power Supply Rejection Ratio	$R_S \leq 10\ K\Omega$ ΔV ±5V	85	100		85	100		80	100		dB
Input Voltage Range		±11	+15.1 −12		±11	+15.1 -12		±11	+15.1 -12		V

AC ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	LF155/255/355 TYP	LF156/256 MIN	LF156/256/356 TYP	LF157/257 MIN	LF157/257/357 TYP	UNITS
Gain Bandwidth Product		2.5		5.0		20	MHz
Settling Time	To 0.01%	4		1.5		1.5	μs
Slew Rate	LF155/156: A_V=1 LF157: A_V=5	5	7.5	12	30	50	V/μs
Input Capacitance		3		3		3	pF
Input Noise Current	F = 100 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
	F = 1 kHz	0.01		0.01		0.01	
Input Noise Voltage (R_S = 100Ω)	F = 100 Hz	25		15		15	$nV/\sqrt{Hz}$
	F = 1 kHz	20		12		12	

Note 1: The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $\pm15V \leqslant V_S \leqslant \pm20V$, $-55°C \leqslant T_A \leqslant +125°C$ and $T_{HIGH} = -125°C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For LF255/6/7, these specifications apply for $\pm15V \leqslant V_S \leqslant \pm20V$, $-25°C \leqslant T_A$ +85°C and T_{HIGH} = +85°C unless otherwise stated. For LF355A/6A/7A, these specifications apply for $\pm15V \leqslant V_S \leqslant \pm20V$, $0°C \leqslant T_A \leqslant +70°C$ and T_{HIGH} = +70°C, and for the LF355/6/7 these specifications apply for $V_S = \pm15V$ and $0°C \leqslant T_A \leqslant +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

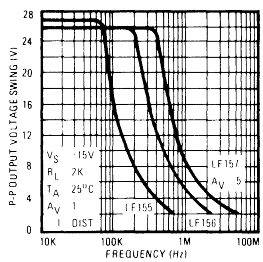
Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d. $T_j = T_A + \theta_{jA} P_d$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

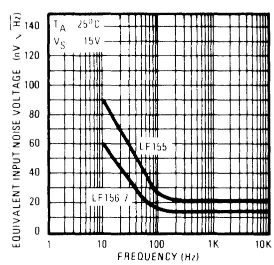
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Setting time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF115/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (see Setting Time Test Circuit).

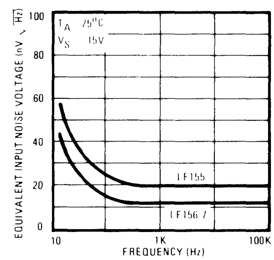
TYPICAL AC PERFORMANCE CHARACTERISTICS



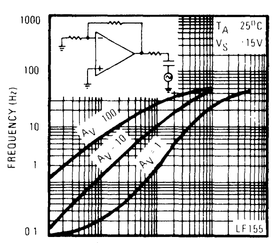
Undistorted Output Voltage Swing



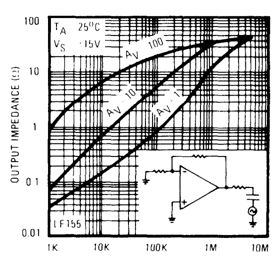
Equivalent Input Noise Voltage



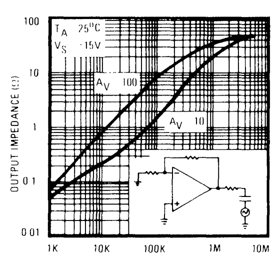
Equivalent Input Noise Voltage (Expanded Scale)



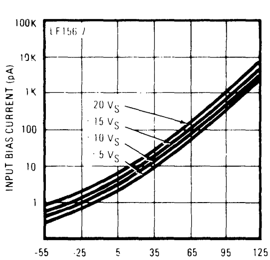
Output Impedance



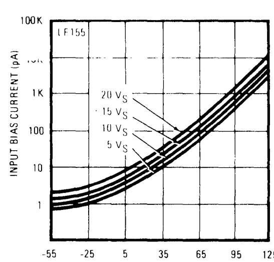
Output Impedance



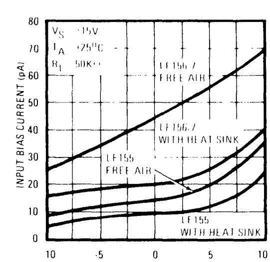
Output Impedance



Input Bias Current

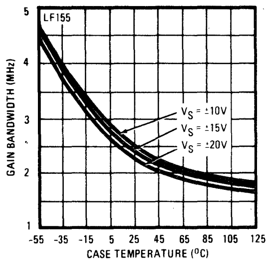


Input Bias Current

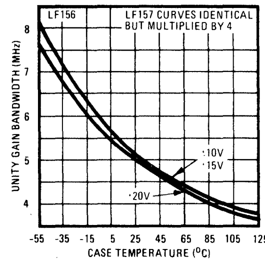


Input Bias Current

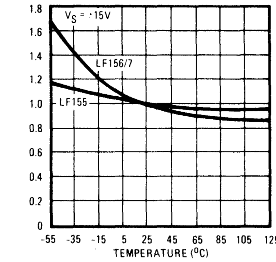
TYPICAL AC PERFORMANCE CHARACTERISTICS (CONT)



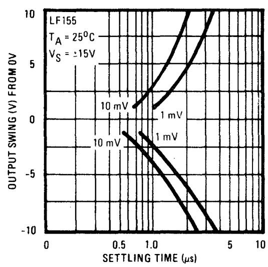
Gain Bandwidth



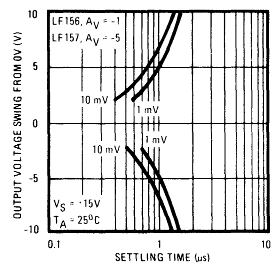
Unity Gain Bandwidth



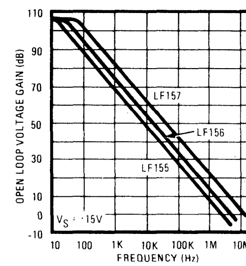
Normalized Slew Rate



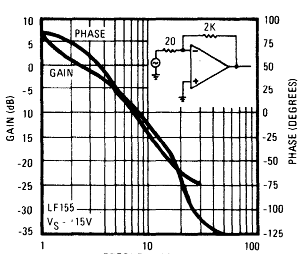
Inverter Setting Time



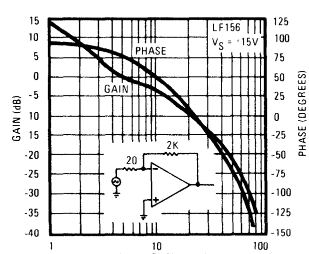
Inverter Setting Time



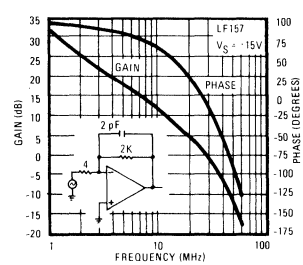
Open Loop Frequency Response



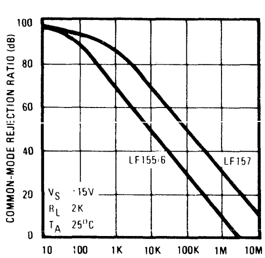
Bode Plot



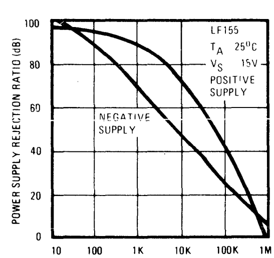
Bode Plot



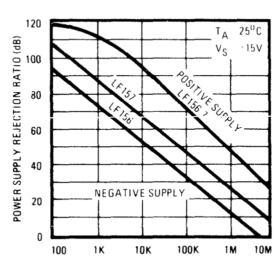
Bode Plot



Common Mode Rejection Ratio

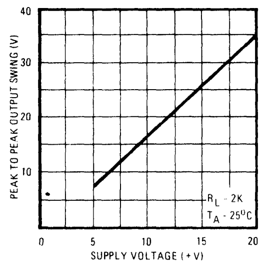


Power Supply Rejection Ratio

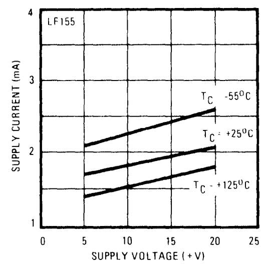


Power Supply Rejection Ratio

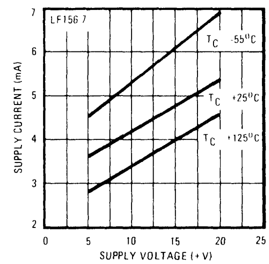
TYPICAL DC PERFORMANCE CHARACTERISTICS



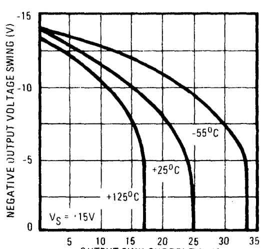
Voltage Swing



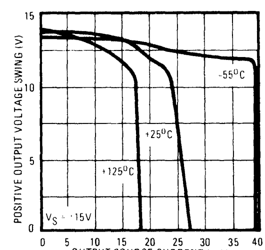
Supply Current



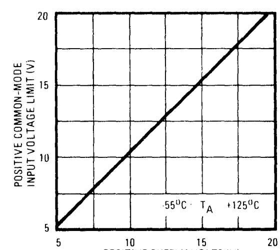
Supply Current



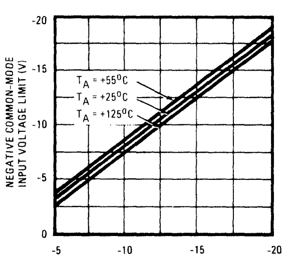
Negative Current Limit



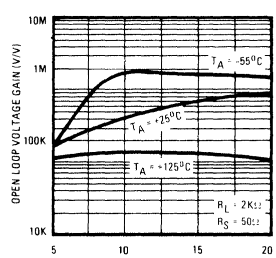
Positive Current Limit



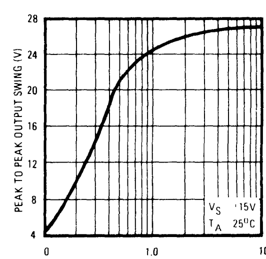
Positive Common-Mode Input Voltage Limit



Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain



Output Voltage Swing

INPUT PROTECTION

This family of op amps has an ion-implanted, P-Channel-JFET input stage. The reverse breakdown voltages are large; therefore there is no need for protective diode-clamps across the inputs. Also, large differential-input voltages can be accommodated without causing large increases in input-bias current. The maximum differential-input-voltage is independent of the supply voltages. These amplifiers have JFET inputs rather than MOSFET inputs, so special handling is not needed. The only word of caution: Do *not* let either input voltage exceed the negative supply voltage. If either input becomes more negative than the negative supply voltage, then excessive currents may flow through the input stage and destroy the unit.

INPUT COMMON-MODE RANGE

An unusual feature of these amplifiers is that the common-mode-input-voltage range for linear operation extends to the positive supply voltage. The common-mode input voltage can even exceed the positive supply voltage by approximately 100 mV. This ability to operate with common-mode voltages of up to, and slightly over, the positive supply voltage holds over the full power-supply range and rated operating temperature range. This capability is very useful in comparator applications where the positive supply voltage can be used as a reference voltage on one of the inputs.

On the negative side, the specified range must be adhered to for proper operation. Exceeding the negative common-mode limit on either input will cause a reversal of phase at the output and will force the amplifier output to the corresponding high or low state (positive or negative saturation). Exceeding the negative common-mode voltage limit on both inputs forces the amplifier output into positive saturation. The amplifier will not "latch" or become damaged by exceeding the negative common-mode limits as long as the peak input current is limited to 30 mA. But there is reversal of phase and this should be carefully considered in designing oscillator circuits, comparators, etc. where common-mode limits might be exceeded.

BROADBANDING

The LF157 family is decompensated to obtain very high slew-rate and gain-bandwidth product. This sacrifices phase-margin and thereby limits the usage to selected applications, but the performance improvement in those particular applications is often substantial. External compensation can be used to optimize overall performance.

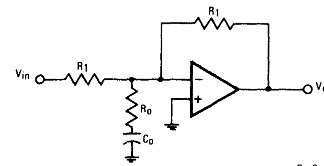
The LF157 series is a LF156 circuit decompensated by a factor of 5, and is therefore 5 times faster than the LF156. But to obtain the same degree of stability, the LF157 op amp must be operated at a minimum closed-loop gain of 5 (maximum feedback factor of 0.2). Stability is determined by the phase shift and magnitude of the loop gain. Instability occurs if the loop gain is greater than unity at a frequency where phase shift of 180°C can occur.

Wideband decompensated amplifiers can be used as low gains if frequency compensation is used. An example of a unity-gain circuit is shown in Figure 1.

At high frequencies, the C_O impedance becomes low and resistor R_O serves to reduce the feedback factor. This circuit has improved AC response with no sacrifice of DC parameters.

INPUT OFFSET VOLTAGE

Conventional FET-input op amps often have an undesirable interaction between adjustment of input offset voltage and drift. With some designs, CMR is also degraded by adjusting input offset voltage. This family of monolithic FET-input op amps has very little interaction of offset adjustment with other parameters. Each mV of offset adjustment typically

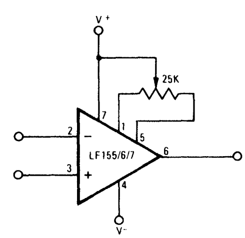


$$\text{Feedback Factor (F)} = 0.5 \frac{R_o C_o s + 1}{(R_o + 0.5R_1) C_o s + 1}$$

Figure 1. LF157 Unity Gain Operation

causes less than $\pm 0.5\mu V/°C$ change in drift. The low initial offset, low drift, and low degree of interaction between offset and drift, all combine to make this amplifier family an ideal choice for any high-gain circuit. For example, the LF356A has a maximum input offset voltage at 25°C of 2 mV and a maximum average temperature of $5\mu V/°C$. Adjusting input offset on the LF356A will typically cause less than $\pm 1\mu V/°C$ of additional drift.

A circuit for adjusting input offset voltage is shown in Figure 2. The range of adjustment will be sufficient to zero any of these amplifiers. For applications requiring very low drift, we recommend using the "A" versions (± 2 mV V_{OS} Max).



- V_{OS} is adjusted with a 2K potentiometer.
- The potentiometer output is connected to the V^+.
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is $\approx 0.5\mu V/°C/mV$ of adjustment.
- Typical overall drift: $5\mu V/0°C \pm (0.5\mu V/°C/mV$ of adj).

Figure 2. Offset Voltage Adjust

INPUT BIAS CURRENT

Low input bias current is the primary advantage of using FET-input op amps. The reduction in bias current is approximately 1000:1 when compared to standard 741-type op amps. This significantly reduces offset and noise when using high-impedance summing networks or when driving the noninverting input with a high-impedance signal source.

Because the input bias currents are junction leakage currents, there will be a doubling of bias current for each 10°C increase in junction temperature. In normal operation, the junction temperature will rise above the ambient temperature by approximately 10°C to 20°C due to the internal power dissipation. In addition, input bias current varies somewhat with common-mode voltage and power supply voltages. The performance curves illustrate typical changes in bias current due to these effects. For applications where input bias currents must be minimized, these secondary effects should be considered.

APPLICATIONS

General-Purpose Instrumentation Amplifier

The three-op-amp instrumentation amplifier circuit shown in Figure 3 provides excellent performance when implemented with op amps from the LF156 family. The circuit will amplify millivolt-level differential signals with very good rejection of common-mode inputs. The FET-input stages of A1 and A2 provide high-input impedance and very low input-bias-currents. CMR vs frequency is usually good due to the excellent AC response. The interaction between input offset adjustment and drift is unusually low, which is very important when using this circuit at high gain.

Circuit operation is straight-forward: The input amplifiers A1 and A2 buffer and amplify the differential-input-voltage V_d, and the common-mode voltage V_{cm} is rejected by the output amplifier A3. To adjust offsets, ground both inputs ($V_d \rightarrow 0$) and set the gain A_d to some high value ($A_d > 100$). Adjust the offset of amplifier A1 for zero at amplifier A3 output ($V_o \rightarrow 0$). Then open up the gain-setting path ($R_g \rightarrow \infty$) and adjust amplifier A3 offset pot for zero at amplifier A3 output ($V_o \rightarrow 0$). Now the gain can be varied over a wide range (1 to 1000 is reasonable) without changing the offset.

To adjust common-mode rejection, connect the two amplifier inputs together (V_d = 0) and drive them with an AC input. A low-frequency sine wave with an amplitude of about ±10V will give the best results. Drive the horizontal input of a scope with the AC signal and observe the output V_o on the vertical channel. Vary the CMR adjust pot for minimum peak-to-peak error voltage at V_o. Differential phase shift between amplifiers A1 and A2 and amplifier nonlinearities will limit the CMR obtainable, but 100 dB to 120 dB at 60 Hz is practical. One advantage of using the 156 family is that the R2 impedance can be larger than usual due to the low input bias currents. Therefore, the CMR adjust pot value can be chosen to provide improved resolution. A value of 100 kΩ is a good choice for R2.

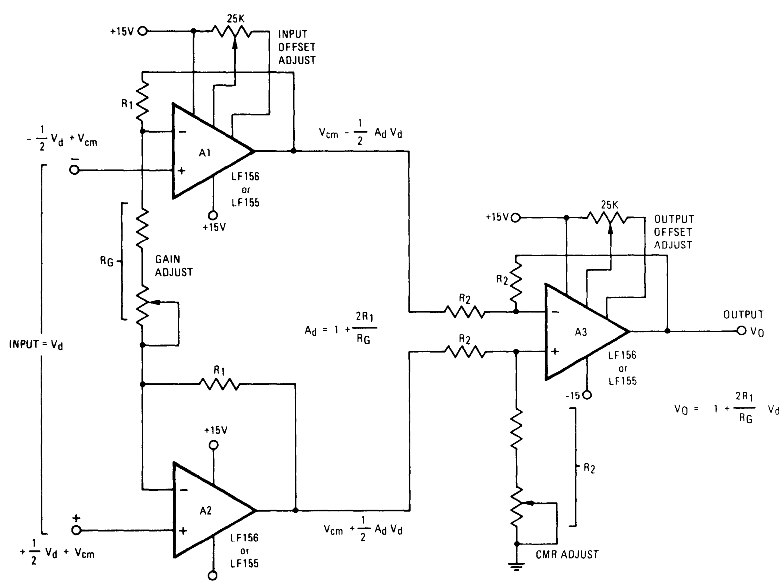


Figure 3. Instrumentation Amplifier

Gain can be varied by changing R_g, and the gain formula is:

$$V_o = \left[1 + \frac{2R_1}{R_g}\right] V_d$$

Minimum gain is unity and the maximum gain is limited by the op-amp open-loop gain. A gain range of 1 to 1000 is readily achieved with excellent performance.

High Q, Bandpass Filter

The LF157 version is recommended for use in active filter circuits. The extra margin of AC response provides much higher performance than can be achieved using standard 741-type op amps.

A bandpass filter using LF157 op amps is shown in Figure 4. This circuit uses positive feedback to achieve high Q. A Q-range of 10 to 50 is practical for this circuit. The transfer function for this circuit is:

$$\frac{V_o(s)}{V_{in}(s)} = \frac{\frac{1}{R_1C_1} K s}{s^2 + \frac{1}{R_1C_1}\left(2 - K\frac{R_1}{R_2}\right) s + \left(\frac{1}{R_1C_1}\right)^2 \left(1 + \frac{R_1}{R_2 + R_3}\right)}$$

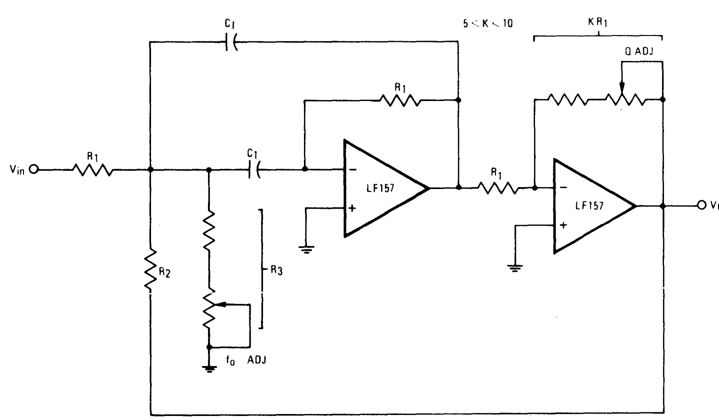
Center frequency f_o is determined primarily by the time constant R_1C_1 and the ratio of R_1 to R_3. Values are chosen such that $R_1 \gg R_3$. A range of 5 to 10 is practical for the gain K.

Center frequency and Q are given by:

$$\omega_o = \frac{1}{R_1C_1}\sqrt{1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}}$$

$$Q = \frac{\omega_o}{\frac{1}{R_1C_1}\left(2 - K\frac{R_1}{R_2}\right)} = \frac{\sqrt{1 + \frac{R_1}{R_2} + \frac{R_1}{R_3}}}{2 - K\frac{R_1}{R_2}}$$

Center frequency can be most easily set by adjusting R_3. The Q can then be independently set by adjusting gain K. Both op amps are operated at loop gains above 5 in this circuit, so the LF157 can be used without encountering stability problems. As with any high-Q bandpass filter, reasonable care must be taken to lead dress, grounding, and power-supply bypassing, to avoid undesired oscillation and noise pick-up.



Monolithic JFET Input Operational Amplifiers

155/155A 156/156A 157/157A

SELECTION GUIDE

Model No.	Temp. Range	V_{OS} (max) at 25°C	V_{OS} (max) Over T	Avg. T_C (max)	I_{OS} (max)	I_b (max)	Slew Rate	I_{CC} (max)
LOW SUPPLY CURRENT								
LF155	-55/125	5 mV	7.0 mV		20 pA	100 pA	5V/μsec	4 mA
LF155A	-55/125	2 mV	2.5 mV	5μV/°C	10 pA	50 pA	3V/μsec (min)	4 mA
LF255	-25/85	5 mV	6.5 mV		20 pA	100 pA	5V/μsec	4 mA
LF355	0/70	10 mV	13.0 mV		50 pA	200 pA	5V/μsec	4 mA
LF355A	0/70	2 mV	2.3 mV	5μV/°C	10 pA	50 pA	3V/μsec (min)	4 mA
WIDE BAND								
LF156	-55/125	5 mV	7.0 mV		20 pA	100 pA	7.5V/μsec (min)	7 mA
LF156A	-55/125	2 mV	2.5 mV	5μV/°C	10 pA	50 pA	10V/μsec (min)	7 mA
LF256	-25/85	5 mV	6.5 mV		20 pA	100 pA	7.5V/μsec (min)	7 mA
LF356	0/70	10 mV	13.0 mV		50 pA	200 pA	12V/μsec	10 mA
LF356A	0/70	2 mV	2.3 mV	5μV/°C	10 pA	50 pA	10V/μsec (min)	7 mA
WIDE BAND DECOMPENSATED ($A_{V_{min}}$ = 5)								
LF157	-55/125	5 mV	7.0 mV		20 pA	100 pA	30V/μsec (min)	7 mA
LF157A	-55/125	2 mV	2.5 mV	5μV/°C	10 pA	50 pA	40V/μsec (min)	7 mA
LF257	-25/85	5 mV	6.5 mV		20 pA	100 pA	30V/μsec (min)	7 mA
LF357	0/70	10 mV	13.0 mV		50 pA	200 pA	50V/μsec	10 mA
LF357A	0/70	2 mV	2.3 mV	5μV/°C	10 pA	50 pA	40V/μsec (min)	7 mA

HIGH RELIABILITY OPTIONS

Part Type	Added Screening	To Order:
All LF15X types	With MIL-STD-883 Class B processing	Add suffix 3 example: LF156DE3
All LF35S DE types ceramic	With A+3 processing including burn-in and tightened AQL*	Add suffix 3 example: LF356DE3
All LF35S N types plastic	With A+2 processing including "Hot Rail" testing, burn-in, temp cycle and tightened AQL*	Add suffix 02 example: LF356N02
	With A+1 processing including "Hot Rail" testing, temp cycle and tightened AQL*	Add suffix 01 example: LF356N01

*Full description contained in the quality section of this catalog.

GENERAL DESCRIPTION

The RM709 and RC709 are monolithic, high gain DC operational amplifiers fabricated on a single silicon chip by the planar process.

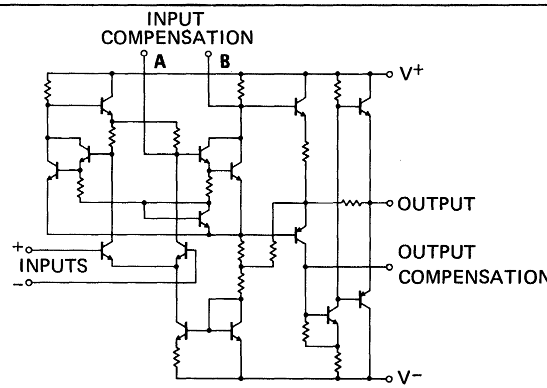
These devices are designed for use in operational amplifier signal processing, low level instrumentation, control systems and for the generation of special linear and non-linear transfer functions.

The RM709 operates over the full military temperature range from −55°C to +125°C. The RC709 is the commercial device intended to operate over a temperature range of 0°C to +70°C.

DESIGN FEATURES

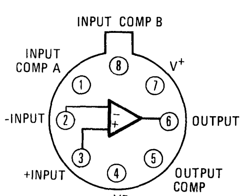
- Low Input Offset Voltage ±1.0mV Maximum
- Low Temperature Drift of Input Offset Voltage ±6μV/°C Maximum
- Low Temperature Drift of Input Offset Current
  (+25°C to +125°C) 0.3nA/°C Maximum
  (−55°C to +25°C) 1.0nA/°C Maximum
- Low Power Consumption 90mW Maximum
- High Performance Open Loop Gain Characteristics 45k Typical

SCHEMATIC DIAGRAM



CONNECTION INFORMATION

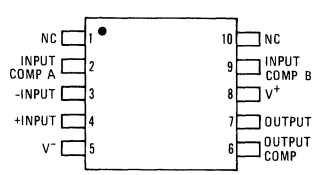
TE (TO-99)
Metal Can Package
(Top View)



NOTE: Pin 4 connected to case.

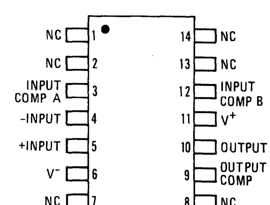
Order Part Nos.:
RM709T, RC709T

CQ
Flat Package
(Top View)



Order Part Nos.:
RM709CQ

DC
Dual In-line Package
(Top View)



NOTE: Pin 7 connected to bottom of package.

Order Part Nos.:
RM709DC, RC709DC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage	±5V
Input Voltage	±10V
Power Dissipation (Note)	
Dual In-line Package	300mW
TO-5 Package	300mW
Flat Package	250mW
Output Short-Circuit Duration ($T_A = 25°C$)	5 sec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
RM709/709A	−55°C to +125°C
RC709	0°C to +70°C
Lead Temperature (Soldering, 60s)	300°C

ELECTRICAL CHARACTERISTICS ($\pm9 \leqslant V_S \leqslant \pm15V$, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	RM709			RC709			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leqslant 10k\Omega$		1.0	3.0		2.0	7.5	mV
Input Offset Current			25	100		100	500	nA
Input Bias Current			180	300		300	1500	nA
Input Resistance		220	400		50	250		kΩ
Output Resistance			150			150		Ω
Supply Current	$V_S = \pm15V$		2.6	4.0			6.6	mA
Power Consumption	$V_S = \pm15V$		80	120		80	200	mW
Transient Response	$R_L = 2k\Omega$, $V_S = \pm15V$, $V_{IN} = 20mV$							
Rise Time	$C_1 = 5nF$, $R_1 = 1.5k$, $C_2 = 200pF$, $R_2 = 50\Omega$		0.3	1.0		0.3	1.0	μs
Overshoot	$C_L \leqslant 100pF$		10	30		10	30	%
Slew Rate	$V_S = \pm15V$, $R_L \geqslant 10k\Omega$, $A_V = 1$	0.15	0.4			0.4		V/μs
Large Signal Voltage Gain	$V_S = \pm15V$, $R_L = 2k$, $V_{OUT} = \pm10V$				15	45		kV/V
The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$ for RM; $0°C \leqslant T_A \leqslant 70°C$ for RC.								
Large Signal Voltage Gain	$V_S = \pm15V$, $R_L \geqslant 2k$, $V_{OUT} = \pm10V$	25	45	70	12			kV/V
Input Offset Voltage	$R_S \leqslant 10k\Omega$			4.0			10	mV
Input Offset Current	$T_A = max$		10	100				nA
	$T_A = min$		50	300			750	nA
Input Bias Current	$T_A = min$		400	1000			2000	nA
Average Temperature of Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ to $T_A = max$		1.8	10				μV/°C
	$R_S = 50\Omega$, $T_A = 25°C$ to $T_A = min$		1.8	10				μV/°C
	$R_S = 10k$, $T_A = 25°C$ to $T_A = max$		2.0	15				μV/°C
	$R_S = 10k$, $T_A = 25°C$ to $T_A = min$		6.0	15				μV/°C
Average Temperature Coefficient of Input Offset Current	$T_A = +25°C$ to max							nA/°C
	$T_A = +25°C$ to min							nA/°C
Input Voltage Range	$V_S = \pm15V$	±8.0	±10		±8.0	±10		V
Output Voltage Swing	$V_S = \pm15V$, $R_L \geqslant 10k\Omega$	±12	±14		±12	±14		V
	$V_S = \pm15V$, $R_L \geqslant 2k\Omega$	±10	±13		±10	±13		V
Input Resistance	$T_A = min$	50	125		35	125		kΩ
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	70	90		65	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$		25	150		25	200	μV/V
Supply Current	$V_S = \pm15V$, $T_A = max$							mA
	$V_S = \pm15V$, $T_A = min$							mA
Power Consumpstion	$V_S = \pm15V$, $T_A = max$							mW
	$V_S = \pm15V$, $T_A = min$							mW

NOTE:
Derate linearly the maximum power dissipation of the dual in-line package at 8.6mW/°C for ambient temperature above +115°C, of the TO-5 package at 5.6mW/°C for ambient temperature above +95°C and of the flat package at 5.4mW/°C for ambient temperature above +103°C. For RC709, rating applies for case temperatures to +70°C.

GENERAL DESCRIPTION

The RM725 and RC725 are high performance, high gain operational amplifiers on a silicon planar epitaxial processed chip.

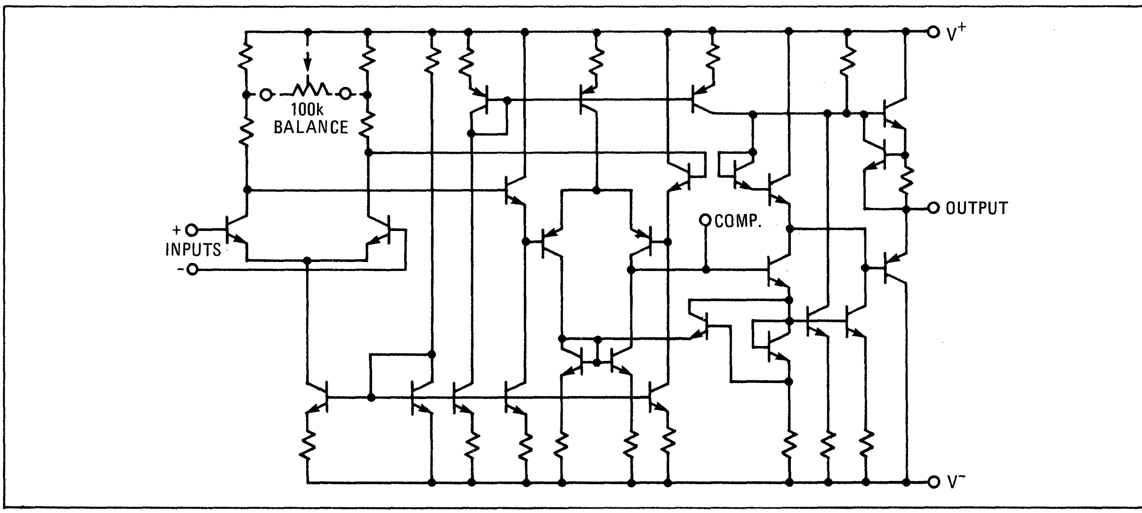
The RM725 military version operates over full temperature range from −55°C to +125°C. The commercial RC725 operates from 0°C to +70°C.

The RM725 and RC725 offer offset null capability, very high voltage gain and low power consumption over a wide power supply voltage range. They are used for all instrumentation applications requiring precise, low level signal amplification, low noise, low drift and accurate closed loop gain.

DESIGN FEATURES

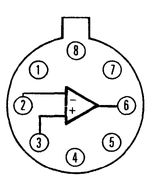
- Low Input Noise Current 0.15pA/√Hz
- High Open Loop Gain 3,000,000
- Low Input Offset Current 2nA
- Low Input Voltage Drift 0.6μV/°C
- High Common-Mode Rejection 120dB
- High Input Voltage Range ±14V
- Wide Power Supply Range ±3V to ±22V
- Offset Null Capability

SCHEMATIC DIAGRAM



CONNECTION INFORMATION

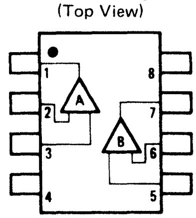
TE (TO-99)
Metal Can Package
(Top View)



Note: Pin 4 connected to case

Order Part Nos.:
RM725T, RC725T

DE and NB Dual
In-line Package
(Top View)



Order Part Nos.:
RM725DE, RC725DE,
RC755NB

PIN	FUNCTION
1	BAL
2	-INPUT
3	+INPUT
4	V-
5	COMP
6	OUTPUT
7	V+
8	BAL

RAYTHEON

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±5V
Input Voltage (Note 2)	±22V
Voltage Between Offset Null and V^+	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
RM725	−55°C to +125°C
RC725	0°C to +70°C
Lead Temperature (Soldering, 60s)	300°C

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM725			RC725			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (without external trim)	$R_S \leqslant 10k\Omega$		0.5	1.0		0.5	2.5	mV
Input Offset Current			2.0	20		2.0	35	nA
Input Bias Current			42	100		42	125	nA
Input Noise Voltage	f_O = 10Hz		15			15		nV/$\sqrt{Hz}$
	f_O = 100Hz		9.0			9.0		
	f_O = 1kHz		8.0			8.0		
Input Noise Current	f_O = 10Hz		1.0			1.0		pA/$\sqrt{Hz}$
	f_O = 100Hz		0.3			0.3		
	f_O = 1kHz		0.15			0.15		
Input Resistance			1.5			1.5		MΩ
Input Voltage Range		±13.5	±14		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geqslant 2k\Omega$ V_{out}=±10V	1,000,000	3,000,000		250,000	3,000,000		
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	110	120		94	120		dB
Power Supply Rejection Ratio	$R_S \leqslant 10k\Omega$		2.0	10		2.0	35	μV/V
Output Voltage Swing	$R_L \geqslant 10k\Omega$	±12	±13.5		±12	±13.5		V
	$R_L \geqslant 2k\Omega$	±10	±13.5		±10	±13.5		
Output Resistance			150			150		Ω
Power Consumption			80	105		80	150	mW
The following specifications apply for −55°C ⩽ T_A ⩽ +125°C for RM725; 0°C ⩽ T_A ⩽ +70°C for RC725.								
Input Offset Voltage (without external trim)	$R_S \leqslant 10k\Omega$			1.5			3.5	mV
Average Input Offset Voltage Drift (without external trim)	$R_S = 50\Omega$		2.0	5.0		2.0		μV/°C
Average Input Offset Voltage Drift (with external trim)	$R_S = 50\Omega$		0.6			0.6		μV/°C
Input Offset Current	T_A=125°C;70°C		1.2	20		1.2	3.5	nA
	T_A=−55°C;0°C		7.5	40		4.0	50	
Average Input Offset Current Drift			35	150		10		pA/°C
Input Bias Current	T_A=125°C;70°C		20	100			125	nA
	T_A=−55°C;0°C		80	200			250	
Large Signal Voltage Gain	T_A=125°C;70°C	1,000,000			125,000			
	T_A=−55°C;0°C	250,000			125,000			
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	100				115		dB
Power Supply Rejection Ratio	$R_S \leqslant 10k\Omega$			20		20		μV/V
Output Voltage Swing	$R_L \geqslant 2k\Omega$	±10			±10			V

NOTES:

1. Rating applies for case temperature to +125°C; derate linearly at 6.5 mW/°C for ambient temperature above +75°C.
2. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

GENERAL DESCRIPTION

The RM741 and RC741 integrated circuits are high performance, high gain internally compensated monolithic operational amplifiers fabricated on a single silicon chip using the planar epitaxial process.

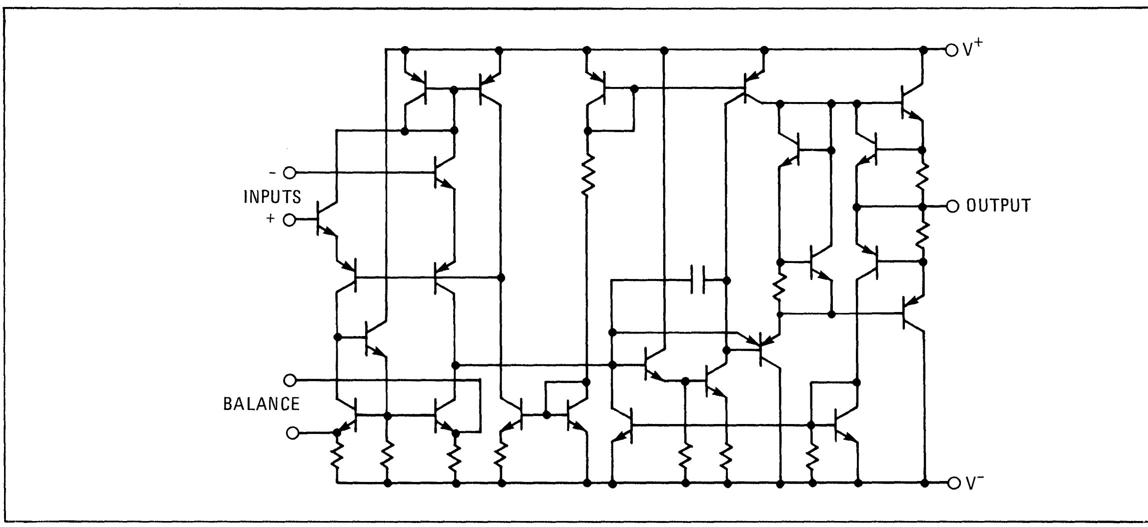
High common-mode voltage range and absence of latch-up tendencies make the RM741 and RC741 ideal for use as a voltage follower. High gain and wide ranges of operating voltages provide superior performance in integrator, summary amplifier and general feedback applications.

Both RM741 and RC741 are pin compatible with the RM709, LM101A and the LM107. The military version, RM741 operates over a temperature range from −55°C to +125°C. The commercial version RC741 operates from 0°C to +70°C.

DESIGN FEATURES

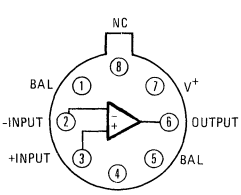
- Supply Voltage ±22V RM741, ±18V RC741
- Offset Voltage Null Capability
- Short-Circuit Protection
- No Frequency Compensation Required
- No Latch-up
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption

SCHEMATIC DIAGRAM



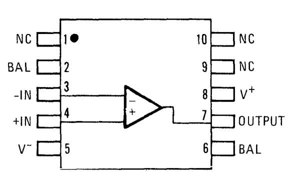
CONNECTION INFORMATION

TE (TO-99)
Metal Can Package
(Top View)



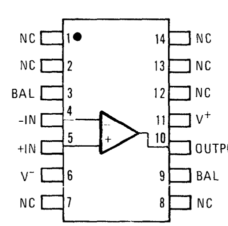
Order Part Nos.:
RM741T, RC741T

CQ
Flat Package
(Top View)



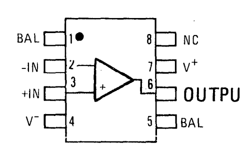
Order Part No.:
RM741CQ

DC
Dual In-line Package
(Top View)



Order Part Nos.:
RM741DC, RC741DC

DE and NB
Dual In-line Package
(Top View)



Order Part No.:
RC741NB, RC741DE,
RV741NB, RV741DE,
RM741DE

RAYTHEON

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . RM741: ±22V
RC741: ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . ±30V
Input Voltage (Note 2) . . . . ±15V
Storage Temperature Range . . . . −65°C to +150°C
Operating Temperature Range
RM741 . . . . −55°C to +125°C
RC741 . . . . 0°C to +70°C
Lead Temperature (Soldering, 60s) . . . . 300°C
Output Short-Circuit Duration (Note 3) . . . . . Indefinite

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM741 MIN	RM741 TYP	RM741 MAX	RC741 MIN	RC741 TYP	RC741 MAX	UNITS
Input Offset Voltage (Note 4)	$R_S \leqslant 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Large-Signal Voltage Gain	$R_L \geqslant 2k\Omega$, $V_{out} = \pm10V$	50,000	200,000		20,000	200,000		
Output Voltage Swing	$R_L \geqslant 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geqslant 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$		30	150		30	150	µV/V
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	V_{in} = 20mV, R_L = 2kΩ, $C_L \leqslant 100pF$							
Risetime			0.3			0.3		µs
Overshoot			5.0			5.0		%
Slew Rate (unity gain)	$R_L \geqslant 2k\Omega$		0.5			0.5		V/µs
The following specifications apply for −55°C ⩽ T_A ⩽ +125°C for RM741; 0°C ⩽ T_A ⩽ +70°C for RC741.								
Input Offset Voltage	$R_S \leqslant 10k\Omega$			6.0			7.5	mV
Input Offset Current	+125°C,+70°C −55°C, 0°C			200			300	nA
Input Bias Current	+125°C,+70°C −55°C, 0°C			500			800	nA
Large-Signal Voltage Gain	$R_L \geqslant 2k\Omega$, $V_{out} = \pm10V$	25,000			15,000			
Output Voltage Swing	$R_L \geqslant 10k$	±12						V
	$R_L \geqslant 2k\Omega$	±10			±10			V
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	70						dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$			150				µV/V
Supply Current	+125°C			2.5				mA
	−55°C			3.3				mA
Power Consumption	+125°C			75				mW
	−55°C			100				mW

NOTES:
1. Rating applies for case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C for RM741.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for RM741.
4. Offset voltage may be nulled by connecting a 10kΩ potentiometer accross the balance pins and connecting the wiper pin to V^-.

GENERAL DESCRIPTION

The RM747 and RC747 integrated circuits are high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial process.

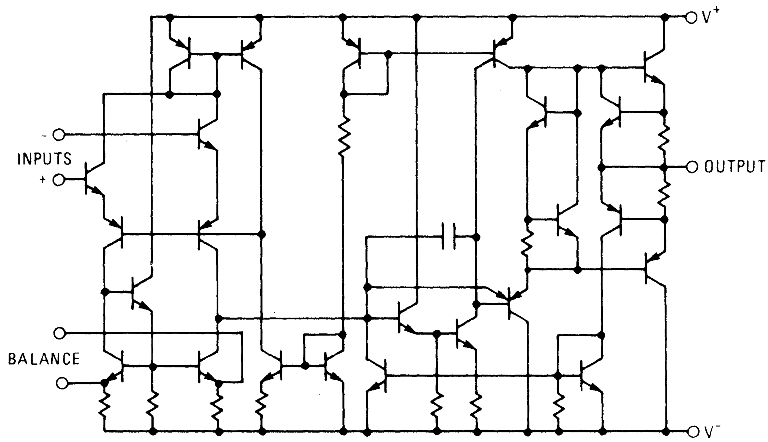
The military version, RM747, operates over a temperature range from −55°C to +125°C. The commercial version, RC747, operates from 0°C to +70°C.

Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of the dual device in all single 741 operational amplifier applications providing high packaging density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

DESIGN FEATURES

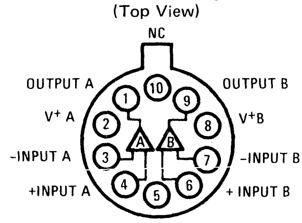
- Short-Circuit Protection
- No Frequency Compensation Required
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- Parameter Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers

SCHEMATIC DIAGRAM (1/2 Shown)



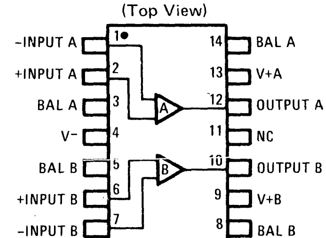
CONNECTION INFORMATION

TF
Metal Can Package
(Top View)



Order Part Nos.:
RM747T, RC747T

DB and DC
Dual In-line Packages
(Top View)



Order Part Nos.:
RM747DC, RC747DC
RC747DB

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	RM747: ±22 V
	RC747: ±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	RM747: −55°C to +125°C
	RC747: 0°C to +70°C
Lead Temperature (Soldering, 60s)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	RM747			RC747			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leqslant 10\ k\Omega$		1.0	5,0		2.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Large-Signal Voltage Gain	$R_L \geqslant 2\ k\Omega$ V_{out} = ±10V	50,000	200,000		50,000	200,000		V/V
Output Voltage Swing	$R_L \geqslant 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geqslant 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leqslant 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10\ k\Omega$		30	150		30	150	μV/V
Power Consumption			100	170		100	170	mW
Transient Response (unity gain)	V_{in} = 20 mV R_L = 2 kΩ $C_L \leqslant 100$ pF							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate (unity gain)	$R_L \geqslant 2\ k\Omega$		0.5			0.5		V/μs
Channel Separation	f = 1 kHz		98			98		dB
The following specifications apply for −55°C ⩽ T_A ⩽ +125°C for RM747; 0°C ⩽ T_A ⩽ +70°C for RC747.								
Input Offset Voltage	$R_S \leqslant 10\ k\Omega$			6.0			7.5	mV
Input Offset Current	+125°C, +70°C -55°C, 0°C			200 500			300 300	nA
Input Bias Current	+125°C, +70°C -55°C, 0°C			500 1500			800 800	nA
Large-Signal Voltage Gain	$R_L \geqslant 2\ k\Omega$ V_{out} = ±10V	25,000			25,000			V/V
Output Voltage Swing	$R_L \geqslant 10k$ $R_L \geqslant 2\ k\Omega$	±12 ±10			±10			V
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	70			70			dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$			150			150	μV/V
Power Consumption	V_S = ±15V							mW
	T_A = +125°C			150			150	
	T_A = −55°C			200			200	
Input Voltage Range		±12			±12			V

NOTES:

1. Rating applies for case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C for RM747.
2. For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for RC747.

GENERAL DESCRIPTION

The RM748 and RC748 integrated circuits are high performance, high gain monolithic operational amplifiers fabricated on a single silicon chip using the planar epitaxial process. Frequency compensation can be tailored externally to cover a broad range of analog applications.

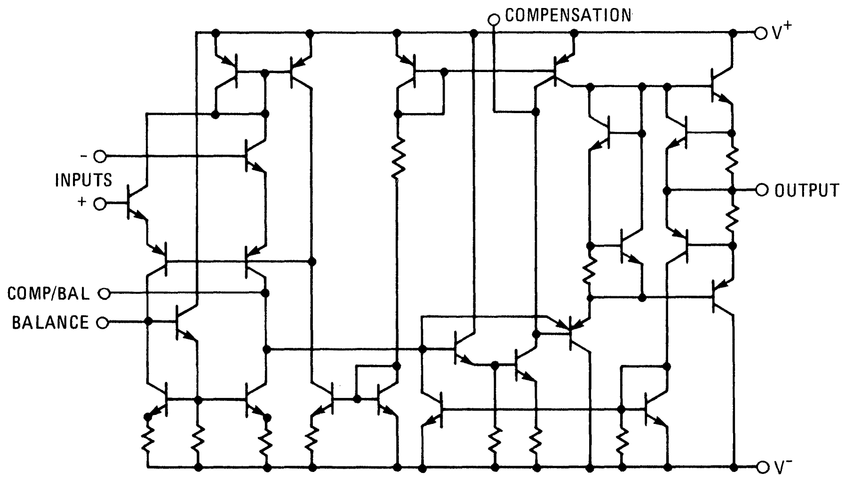
High common-mode voltage range and absence of latch-up tendencies make the RM748 and RC748 ideal for use as a voltage follower. High gain and wide ranges of operating voltages provide superior performance in integrators, summing amplifiers and general feedback applications. Unity gain compensation is achieved by means of a single 30pF capacitor.

Both RM748 and RC748 are pin compatible with the RM709, LM101 and RM4101. The military version, RM748 operates over a temperature range from −55°C to +115°C while the commercial version RC748 operates from 0°C to +70°C.

DESIGN FEATURES

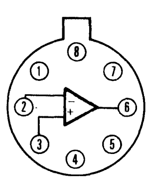
- Offset Voltage Null Capability
- Short-Circuit Protection
- No Latch-up
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption

SCHEMATIC DIAGRAM



CONNECTION INFORMATION

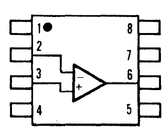
TE (TO-99)
Metal Can Package
(Top View)



Note: Pin 4 connected to case

Order Part Nos.:
RM748T, RC748T

DE and NB
Dual In-line Packages
(Top View)



Order Part Nos.:
RC748NB, RC748DE,
RM748DE

PIN	FUNCTION
1	COMP/BAL
2	-INPUT
3	+INPUT
4	V-
5	BAL
6	OUTPUT
7	V+
8	COMP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage: RM748	±22V
Supply Voltage: RC748	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range: RM748	−55°C to +125°C
Operating Temperature Range: RC748	0°C to +70°C
Lead Temperature (Soldering, 60s)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM748			RC748			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leqslant 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Large-Signal Voltage Gain	$R_L \geqslant 2k\Omega$, V_{out} = ±10V	50,000	200,000		20,000	200,000		
Output Voltage Swing	$R_L \geqslant 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geqslant 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$		30	150		30	150	μV/V
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	V_{in} = 20mV, R_L = 2kΩ, $C_L \leqslant 100pF$							
Risetime			0.3			0.3		μs
Overshoot	(Note 4)		5.0			5.0		%
Slew Rate (unity gain)	$R_L \geqslant 2k\Omega$ (Note 4)		0.5			0.5		V/μs
The following specifications apply for −55°C ≤ T_A ≤ +125°C for RM748 ; 0°C ≤ T_A ≤ +70°C for RC748.								
Input Offset Voltage	$R_S \leqslant 10k\Omega$			6.0			7.5	mV
Input Offset Current	+125°C,+70°C			200			300	nA
	−55°C,+70°C			500			800	
Input Bias Current	+125°C,+70°C						800	nA
	−55°C,+70°C						800	
Large-Signal Voltage Gain	$R_L \geqslant 2k\Omega$, V_{out} = ±10V	25,000			15,000			
Output Voltage Swing	$R_L \geqslant 10k$	±12						V
	$R_L \geqslant 2k$	±10			±10			
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	70						dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$			150				μV/V

NOTES:
1. Rating applies for case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C for RM748.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for RM748.
4. Compensation capacitor: 30pF.

Dual High-Gain Operational Amplifiers

GENERAL DESCRIPTION

The RC1437 and RM1537, previously referred to as the 4709, integrated circuits are monolithic dual high gain operational amplifiers. The device is composed of two 709 operational amplifiers fabricated on a single silicon chip. It has all the outstanding features of the 709.

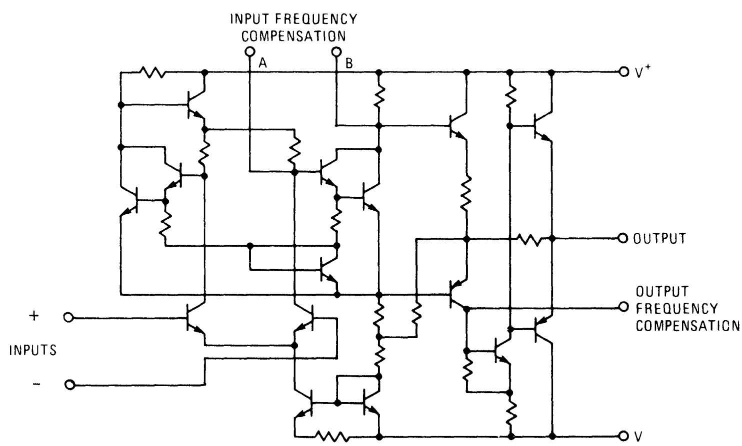
Due to the inherent matching and tracking of parameters, the 1537/1437 has several unique applications: differential in/out amplifiers, non-inverting amplifiers, gain and phase matched channels.

The RM1537 operates over a temperature range of −55°C to +125°C. RC 1437 is the commercial temperature range device for operation from 0°C to +75°C.

DESIGN FEATURES

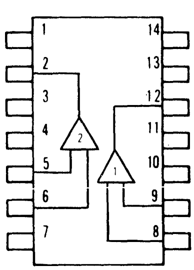
- Gain and Phase Matching Between Amplifiers
- Low Temperature Drift ±3 μV/°C
- Large Output Voltage Swing ±14 V Typical

SCHEMATIC DIAGRAM (1/2 Shown)



CONNECTION INFORMATION

DC and DB
Dual In-line Packages
(Top View)



Order Part Nos.:
RM1537DC, RC1437DC,
RC1437DB

PIN	FUNCTION
1	OUTPUT LAG 2
2	OUTPUT 2
3	INPUT LAG 2
4	INPUT LAG 2
5	-INPUT 2
6	+INPUT 2
7	V^-
8	+INPUT 1
9	-INPUT 1
10	INPUT LAG 1
11	INPUT LAG 1
12	OUTPUT 1
13	OUTPUT LAG 1
14	V^+

Dual High-Gain Operational Amplifiers

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . ±18 V	Operating Temperature Range . RM1537: −55°C to +125°C
Differential Mode Input Voltage . . . . ±5 V	RC1437: 0°C to +75°C
Common Mode Input Voltage . . . . ±V+v	Storage Temperature Range . . . . −65°C to +150°C
Power Dissipation . . . . 500 mW	Lead Temperature (Soldering, 60s) . . . . 300°C
Derate above 75°C . . . . 5.0 mW/°C	Output Short Circuit Duration (25°C). . . . . .5 s

ELECTRICAL CHARACTERISTICS (RM1537: −55°C to +125°C; RC1437: 0°C to +75°C, unless otherwise noted)

PARAMETER	CONDITIONS		RM1537			RC1437			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$50\Omega \leqslant R_S \leqslant 10k\Omega$	$T_A = 25°C$		1.0	5.0		1.0	7.5	mV
	$\pm9V < V^+ < \pm15V$				6.0			10	
Input Offset Current	$\pm9V < V^+ < \pm15V$	RM1537: +25°C to +125°C RC1437: +25°C to +75°C		50	200		50	500	nA
		RM1537: −55°C RC1437: 0°C			500			750	
Input Bias Current	$\pm9V < V^+ < \pm15V$	RM1537: +25°C to +125°C RC1437: +25°C to +75°C		0.2	0.5		0.4	1.5	μA
		RM1537: −55°C RC1437: 0°C			1.5			2.0	
Input Resistance	$\pm9V < V^+ < \pm15V$		150	400		50	150		kΩ
Output Resistance	$\pm9V < V^+ < \pm15V$			150			150		Ω
Power Consumption	$V^+ = \pm15V$, $R_L = \infty$			160	225		160	225	mW
Large Signal Voltage Gain	$V^+ = \pm15V$, $V_O = \pm10V$, $R_L \geqslant 2\ k\Omega$		25	45	70	15	45		KV/V
Output Voltage Swing	$V^+ = \pm15V$	$R_L \geqslant 10\ k\Omega$ $R_L \geqslant 2\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V
Input Common Mode Voltage	$V^+ = \pm15V$		±8	±10		±8	±10		V
Common Mode Rejection Ratio	$R_S \leqslant 10\ k\Omega$, $\pm9V < V^+ < \pm15V$		70	90		65	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10\ k\Omega$, $\pm9V < V^+ < \pm15V$				150			200	$\mu V/V$
Transient Response	$V^+ = \pm15V$, $V_{in} = 20$ mV, $R_L = 2\ k\Omega$, $C_1 = 5$ nF, $R_1 = 1.5\ k\Omega$, $C_2 = 200$ pF, $R_2 = 50\ \Omega$								
Rise Time				0.3	1.0		0.3	1.0	μs
Overshoot					30			30	%
Average Temperature Coefficient of Input Offset Voltage	$\pm9V < V^+ < \pm15V$	$R_S = 50\ \Omega$ $R_S = 10\ k\Omega$		1.5 3.0			1.5 3.0		$\mu V/°C$
Average Temperature Coefficient of Input Offset Current	$\pm9 < V^+ < \pm15V$			0.7			0.7		nA/°C
Channel Separation, f = 10 kHz	$\pm9V < V^+ < \pm15V$			90			90		dB

MATCHING CHARACTERISTICS ($T_A = 25°C$, $\pm9V < V^+ < \pm15V$ unless otherwise noted)

PARAMETER	RM1537			RC1437			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Gain		±1.0			±1.0		dB
Input Bias Current		±100			±150		nA
Input Offset Current		±15			±20		nA
Input Offset Voltage		±0.5			±1.0		mV
Average Temperature Coefficient of Input Offset Voltage		±0.5			±0.5		$\mu V/°C$
Average Temperature Coefficient of Input Offset Current		±0.2			±0.2		nA/°C

1458 1558 Dual 741 General Purpose Operational Amplifiers

GENERAL DESCRIPTION

The RM1558 and RC1458 integrated circuits are high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial process.

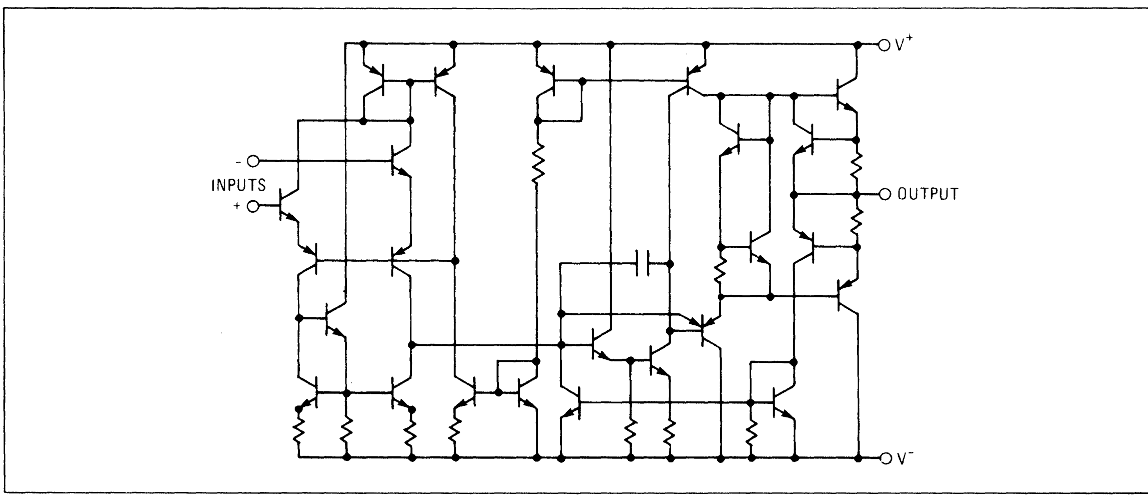
The military version, RM1558, operates over a temperature range from −55°C to +125°C. The commercial version, RC1458, operates from 0°C to +70°C.

Combining all of the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. It is especially well suited for applications where gain and phase matched channels are mandatory.

DESIGN FEATURES

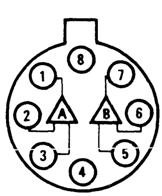
- Short-Circuit Protection
- No Frequency Compensation Required
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- Parameter Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers

SCHEMATIC DIAGRAM (1/2 Shown)



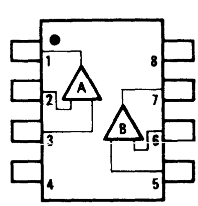
CONNECTION INFORMATION

TE (TO-99)
Metal Can Package
(Top View)



Order Part Nos.:
RM1558T, RC1458T

DE and NB Dual
In-line Package
(Top View)



Order Part No.:
RC1458NB, RC1458DE
RM1558DE

PIN	FUNCTION
1	OUTPUT (A)
2	−INPUT (A)
3	+INPUT (A)
4	V−
5	+INPUT (B)
6	−INPUT (B)
7	OUTPUT (B)
8	V+

Dual 741 General Purpose Operational Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	RM1558: ±22 V RC1458: ±18 V	Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation (Note 1)	500 mW	Operating Temperature Range	RM1558: −55°C to +125°C RC1458: 0°C to +70°C
Differential Input Voltage	±30 V	Lead Temperature (Soldering, 60s)	300°C
Input Voltage (Note 2)	±15 V	Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_A = 25°C unless otherwise noted)

PARAMETER	CONDITIONS	RM1558			RC1458			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			30	200		30	200	nA
Input Bias Current			200	500		200	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$ $V_{out} = \pm 10V$	50,000	200,000		50,000	200,000		V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Power Consumption			100	150		100	170	mW
Transient Response (unity gain)	V_{in} = 20mV $R_L = 2\ k\Omega$ $C_L \leq 100pF$							
Risetime			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate (unity gain)	$R_L \geq 2\ k\Omega$		0.5			0.5		V/μs
Channel Separation	f = 1 kHz		98			98		dB
The following specifications apply for −55°C ≤ T_A ≤ +125°C for RM1558; 0°C ≤ T_A ≤ +70°C for RC1458.								
Input Offset Voltage	$R_L \leq 10\ k\Omega$			6.0			7.5	mV
Input Offset Current	+125°C,+70°C −55°C, 0°C			200 500			300 300	nA
Input Bias Current	+125°C,+70°C −55°C, +70°C			500 1500			800 800	nA
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$ $V_{out} = \pm 10V$	25,000			25,000			
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±12 ±10			±10			V
Power Consumption	V_S = ±15V							
	T_A = +125°C			150			150	mW
	T_A = −55°C			200			200	
Input Voltage Range		±12			±12			V

NOTES:

1. Rating applies for case temperatuers to +125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C for RM1558.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for RC1458.

GENERAL DESCRIPTION

The RM1556/RC1556 are high performance, high gain operational amplifiers. Each amplifier is internally compensated and fabricated on a single silicon chip by the planar epitaxial process.

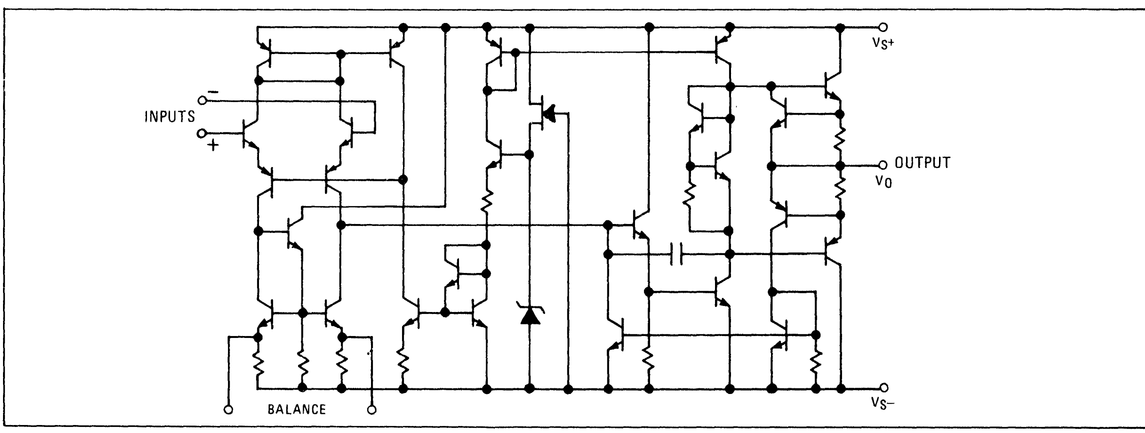
These amplifiers feature high common-mode and differential voltage range, very low input bias current, optimum performance over a wide range of supply voltage, and freedom from "latch-up." They are ideal for use as voltage followers, comparators, integrators, summing and general purpose amplifiers.

The RM types operate over a temperature range of -55°C to +125°C. The RC types operate from 0°C to +70°C.

DESIGN FEATURES

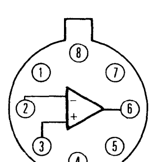
- Input Bias Current 15nA Maximum
- Input Offset Current 2nA Maximum
- Input Offset Voltage 4mV Maximum
- At ±15V Current Drain 1.0mA
- Offset Voltage Nulling (10k pot)
- Slew Rate 2.0V/μs
- Unity Gain Bandwidth 4MHz
- Gain Variation 3dB from ±3V to ±20V
- Open Loop Voltage Gain 106dB

SCHEMATIC DIAGRAM



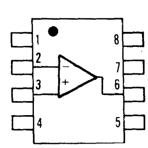
CONNECTION INFORMATION

TE (TO-99)
Metal Can Package
(Top View)



Order Part Nos.:
RM1556T, RC1556T

NB Dual In-line
Plastic Package
(Top View)



Order Part No.:
RC1556NB

PIN	FUNCTION
1	BAL
2	-INPUT
3	+INPUT
4	V^-
5	BAL
6	OUTPUT
7	V^+
8	NC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . RM1556: ±22V
RC1556: ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . ±30V
Input Voltage (Note 2) . . . . ±15V
Storage Temperature Range . . . . −65°C to +150°C
Operating Temperature Range
RM1556 . . . . −55°C to +125°C
RC1556. . . . . 0°C to +70°C
Lead Temperature (Soldering, 60s) . . . . 300°C
Output Short-Circuit Duration (Note 3) . . . . . . Indefinite

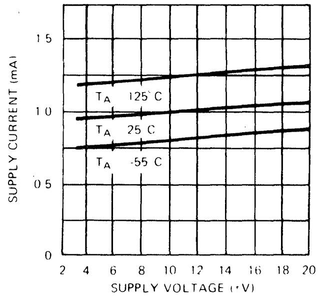
RM1556 AND RC1556 ELECTRICAL CHARACTERISTICS

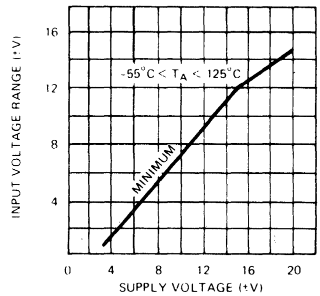
(RM1556: $-55°C \leq T_A \leq 125°C$; RC1556: $0°C \leq T_A \leq 70°C$; $V_S = \pm15V$ unless otherwise specified)

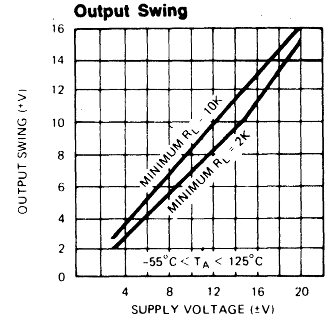
PARAMETER	CONDITIONS	RM1556			RC1556			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		2.0	4.0		5.0	10	mV
Input Offset Current	$T_A = 25°C$		1.0	2.0		5.0	10	nA
Input Bias Current	$T_A = 25°C$		8.0	15		15	30	nA
Input Resistance	$T_A = 25°C$		5.0			3.0		MΩ
Supply Current	$T_A = 25°C$		1.0	1.5		1.3	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$ $V_{OUT} = \pm10V$, $R_L > 2k\Omega$	100	200		70	100		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			6.0			14	mV
Input Offset Current	+25°C to T_H			3.0			14	nA
	T_L to +25°C			5.0			14	
Input Bias Current				30			40	nA
Supply Current				1.9			3.5	mA
Slew Rate (Unity Gain)	$T_A = 25°C$, $R_L \geq 2k\Omega$		2.0			2.0		V/μs
Bandwidth (Unity Gain)	$T_A = 25°C$, $R_L \geq 2k\Omega$		4			4		MHz
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	40			40			V/mV
Output Voltage Swing	$T_A = 25°C$, $R_L \geq 2k\Omega$,	±12	±13		±11	±12		V
Input Voltage Range		±12	±13		±11	±12		V
Input Noise Voltage	$R_S = 10k\Omega$, f = 1.0kHz, AV = 100, BW = 1.0Hz		25			25		$nV/\sqrt{Hz}$
Common-Mode Rejection Ratio	$R_S \leq 50k\Omega$	80	110		70	110		dB
Supply Voltage Rejection Ratio	$R_L \leq 50k\Omega$	80	86		74	83		dB

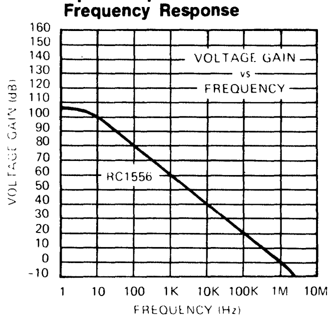
NOTES:
1. For operating at elevated temperatures, the device must be derated based on 150°C for RM1556; 100°C for RC1556 maximum junction temperature and a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit to ground rating applies to +125°C case temperature or +75°C ambient temperature for RM1556.

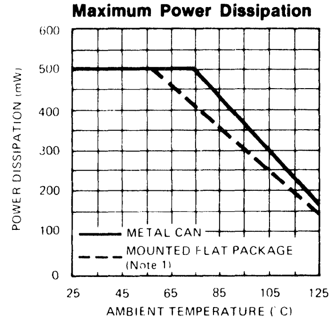
TYPICAL ELECTRICAL DATA

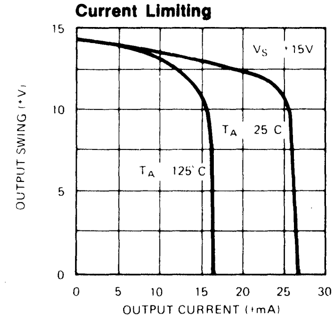
Supply Current


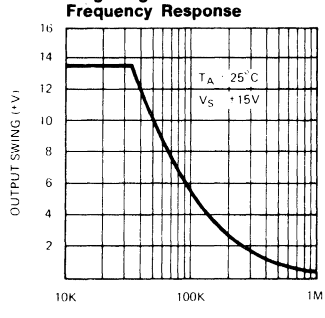
Input Voltage Range


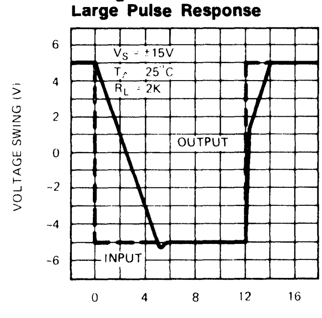
Output Swing


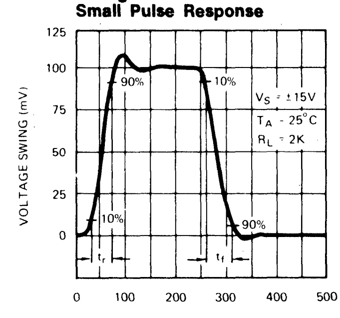
Open Loop Frequency Response


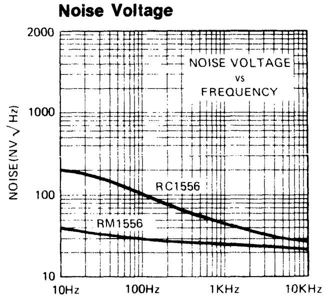
Maximum Power Dissipation


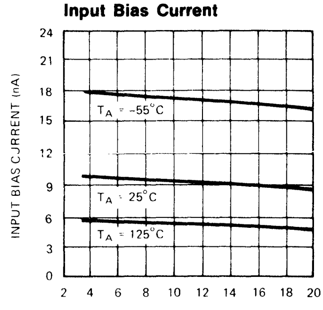
Current Limiting


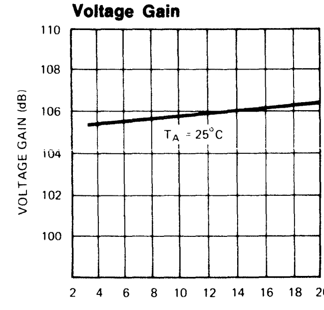
Large Signal Frequency Response


Voltage Follower Large Pulse Response


Voltage Follower Small Pulse Response


Noise Voltage


Input Bias Current


Voltage Gain


Dual High Performance Operational Amplifiers

2101A 2201A 2301A

GENERAL DESCRIPTION

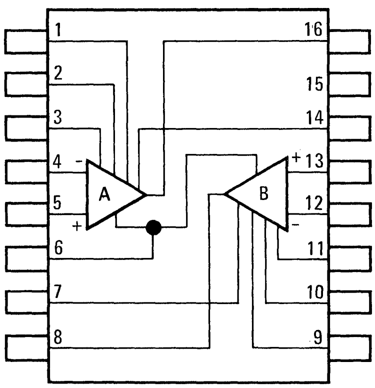
The LH2101A series of dual operational amplifiers are two LM101A type op amps in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost, and smaller size than two singles.

The LH2101A is specified for operation over the −55°C to +125°C military temperature range. The LH2201A is specified for operation over the −25°C to +85°C temperature range. The LH2301A is specified for operation over the 0°C to +70°C temperature range.

DESIGN FEATURES

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

CONNECTION DIAGRAM

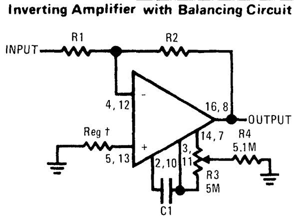


Part Order Nos.: LH2101AD, LH2201AD or LH2301AD

PIN	FUNCTION
1	V^+
2	OUTPUT COMP
3	BAL/COMP
4	INV. INPUT
5	NON-INV. INPUT
6	V^-
7	BALANCE
8	OUTPUT
9	V^+
10	OUTPUT/COMP
11	BAL/COMP
12	INV. INPUT
13	NON-INV. INPUT
14	BALANCE
15	GROUND
16	OUTPUT

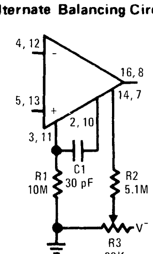
AUXILIARY CIRCUITS

Inverting Amplifier with Balancing Circuit

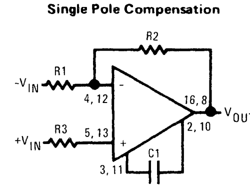


†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

Alternate Balancing Circuit



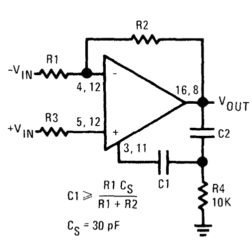
Single Pole Compensation



$C1 \geq \frac{R1\ C_S}{R1 + R2}$

$C_S = 30\ pF$

Two Pole Compensation

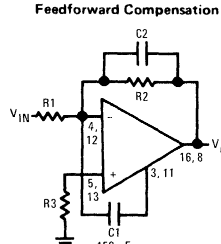


$C1 \geq \frac{R1\ C_S}{R1 + R2}$

$C_S = 30\ pF$

$C2 = 10\ C1$

Feedforward Compensation



$C2 = \frac{1}{2\pi f_0\ R2}$

$f_0 = 3\ MHz$

RAYTHEON

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . ±22V
Power Dissipation (Note 1) . . . . 500 mW
Differential Input Voltage . . . . ±30V
Input Voltage (Note 2) . . . . ±15V
Output Short-Circuit Duration . . . . Continuous
Operating Temperature Range LH2101A . -55°C to 115°C
LH2201A . . -25°C to 85°C
LH2301A . . . 0°C to 70°C
Storage Temperature Range . . . . -65°C to 150°C
Lead Temperature (Soldering, 10 sec) . . . . 300°C

ELECTRICAL CHARACTERISTICS each side (Note 3)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2101A	LH2201A	LH2301A	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50$ kΩ	2.0	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	75	75	250	nA Max
Input Resistance	$T_A = 25°C$	1.5	1.5	0.5	MΩ Min
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$	3.0	3.3	3.0	mA Max
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2$ kΩ	50	50	25	V/mV Min
Input Offset Voltage	$R_S \leq 50$ kΩ	3.0	3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	15	30	μV/°C Max
Input Offset Current		20	20	70	nA Max
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq 25°C$	0.1 0.2	0.1 0.2	0.3 0.6	nA/°C Max nA/°C Max
Input Bias Current		100	100	300	nA Max
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$	2.5	2.5		mA Max
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2$ kΩ	25	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10$ kΩ $R_L = 2$ kΩ	±12 ±10	±12 ±10	±12 ±10	V Min V Min
Input Voltage Range	$V_S = \pm 20V$	±15	±15	±12	V Min
Common Mode Rejection Ratio	$R_S \leq 50$ kΩ	80	80	70	dB Min
Supply Voltage Rejection Ratio	$R_S \leq 50$ kΩ	80	80	70	dB Min

NOTES:
(1) The maximum junction temperature of the LH2101A is 150°C, while that of the LH2201A is 100°C. For operating temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
(2) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
(3) These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LH2201A, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$. For the LH2301A these specifications apply for $0°C \leq T_A \leq 70°C$, ±5V and $\leq V_S \leq$ ±15V. Supply current and input voltage range are specified as $V_S = \pm 15V$ for the LH2301A. $C_1 = 30$ pF unless otherwise specified.

Quad Current Mode Single-Supply Operational Amplifiers

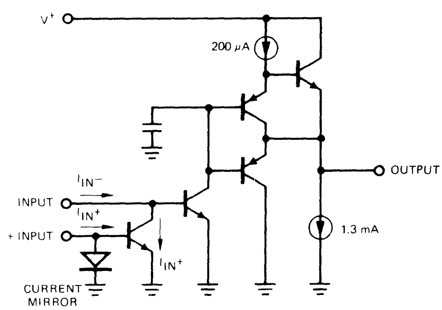
GENERAL DESCRIPTION

The LM2900 and LM3900 consist of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: AC amplifiers, RC active filters; low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

DESIGN FEATURES

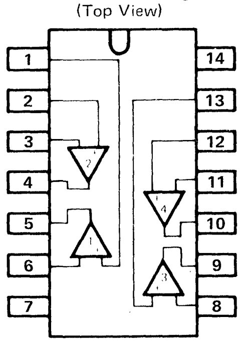
- Wide Single Supply Voltage Range 4V to 36V
- Supply Current Drain Independent of Supply Voltage
- Low Input Biasing Current 30 nA
- High Open-loop Gain 70 dB
- Wide Bandwidth 2.5MHz (Unity Gain)
- Larger Gain-Bandwidth Product in Non-Inverting Mode ($A_V = 100$ @ f = 1 MHz)
- Large Output Voltage Swing, $(V^+-1)V_{p\text{-}p}$
- Internally Frequency Compensated for Unity Gain
- Output Short-Circuit Protection

SCHEMATIC DIAGRAM (1/4 Shown)



CONNECTION INFORMATION

DB
Dual In-line Package
(Top View)



Order Part Nos.:
LM2900N, LM3900N

PIN	FUNCTION
1	+INPUT 1
2	+INPUT 2
3	-INPUT 2
4	OUTPUT 2
5	OUTPUT 1
6	-INPUT 1
7	GROUND
8	-INPUT 3
9	OUTPUT 3
10	OUTPUT 4
11	-INPUT 4
12	+INPUT 4
13	+INPUT 3
14	V^+

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (LM 2900) ... +36V	Output Short Circuit Duration — One Amplifier, T_A = 25°C ... Continuous
(LM 3900) ... +32V	Operating Temperature Range (LM 2900) . −40°C to +85°C
Supply Voltage ... ±18V	Operating Temperature Range (LM 3900) . . 0°C to +70°C
Power Dissipation (T_A = 25°C)(Note 1) ... 570mW	Storage Temperature Range ... −65°C to +150°C
Input Currents, I_{IN}+ or I_{IN}− ... 20mA	Lead Temperature (Soldering, 10 sec) ... 300°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15V, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS	LM 2900/LM 3900			
		MIN	TYP	MAX	UNITS
Open Loop					
Voltage Gain	f = 100 Hz	1200	2800		V/V
Input Resistance	Inverting Input		1		MΩ
Output Resistance			8		kΩ
Unity Gain Bandwidth	Inverting Input (Note 2)		2.5		MHz
Input Bias Current	Inverting Input		30	200	nA
Slew Rate	Positive Output Swing		0.5		V/μs
	Negative Output Swing		20		V/μs
Supply Current	R_L = ∞ On All Amplifiers		6.2	10	mA
Output Voltage Swing R_L = 5.1 k					
V_{OUT} High	I_{IN-} = 0, I_{IN+} = 0	13.5	14.2		V
V_{OUT} Low	I_{IN-} = 10 μA, I_{IN+} = 0		0.09	0.2	V
Output Current Capability					
	Source	6	18		mA
	Sink (Note 3)	0.5	1.3		mA
Power Supply Rejection	f = 100 Hz		70		dB
Mirror Gain	I_{IN+} = 200 μA (Note 4)	0.90	1	1.1	μA/μA
Mirror Current	(Note 5)		10	500	μA
Negative Input Current	(Note 6)		1.0		mA

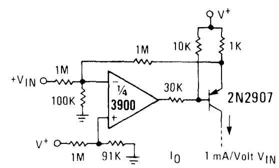
NOTES:

1. For operating at high temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient.
2. When used as a "non-inverting amplifier", the gain-bandwidth product is not limited to 2.5 MHz. The isolation provided by the "current mirror" allows a constant unity voltage gain feedback for the main inverting amplifier. This means that large values of gain can be achieved at high frequencies and the dominant limit is due to the slew rate of the amplifier. For example: a voltage gain of 100 is easily obtained at 1 MHz and an output voltage swing of 160 mVp-p can be achieved prior to slew rate limiting. This operational mode is useful for signal frequencies in the 50 kHz to 1 MHz range as would be encountered in IF or carrier frequency applications.
3. The output current sink capability can be increased for large signal conditions by overdriving the inverting input.
4. This spec indicates the current gain of the current mirror which is used as the non-inverting input.
5. Input V_{BE} match between the non-inverting and the inverting inputs occurs for a mirror-current (non-inverting input current) of approximately 10 μA. This is therefore a typical design center for many of the application circuits.
6. Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately −0.3 V_{DC}. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1 mA. Negative input currents in excess of 4 mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven, negative smaller maximum currents are allowed. Common-mode current biasing can be used to prevent negative input voltages; for example, see the "Differentiator Circuit" in the applications section.

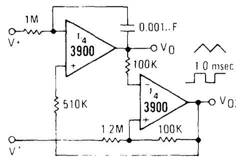
Quad Current Mode Single-Supply Operational Amplifiers

3900 TYPICAL APPLICATIONS ($V^+ = 15V$)

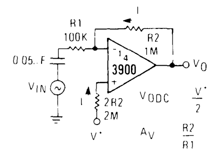
Voltage-Controlled Current Source (Transconductance Amplifier)



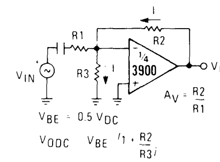
Triangle/Square Generator



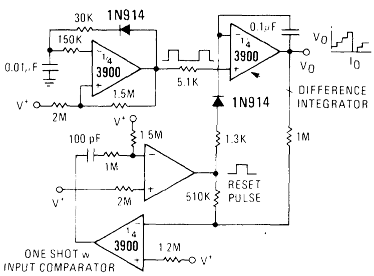
Inverting Amplifier



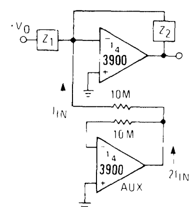
V_{BE} Biasing



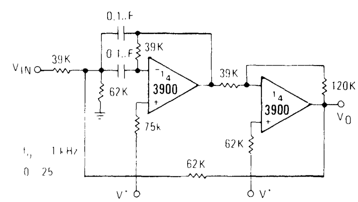
Free-Running Staircase Generator/Pulse Counter



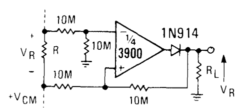
Supplying I_{IN} with Aux. Amp (to Allow High Z Feedback Networks)



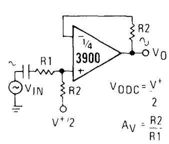
Bandpass Active Filter



Ground Referencing a Differential Input Signal

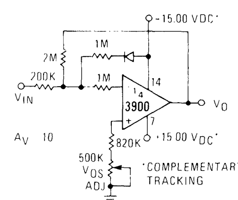


Non-Inverting Amplifier

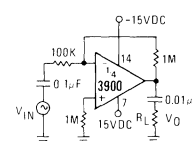


Split Supply ($V^+ = +15V_{DC}$ & $V^- = -15V_{DC}$)

Non-Inverting DC Gain



AC Amplifier



Micropower Operational Amplifier

GENERAL DESCRIPTION

The 3078 and 3078A are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The 3078 and 3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

The 3078A is a premium device having a supply voltage range of $V^{\pm}$ = 0.75V to $V^{\pm}$ = 15V and an operating temperature range of -55°C to +125°C. The 3078 has the same lower supply voltage limit but the upper limit is V^{+} = +6V and V^{-} = -6V. The operating temperature range is from 0°C to +70°C.

DESIGN FEATURES

- Low Standby Power: As Low as 700 nW
- Wide Supply Voltage Range: ±0.75 to ±15V
- High Peak Output Current: 6.5 mA min.
- Adjustable Quiescent Current
- Output Short-circuit Protection

APPLICATIONS

- Portable Electronics
- Medical Electronics
- Instrumentation
- Telemetry

SCHEMATIC DIAGRAM

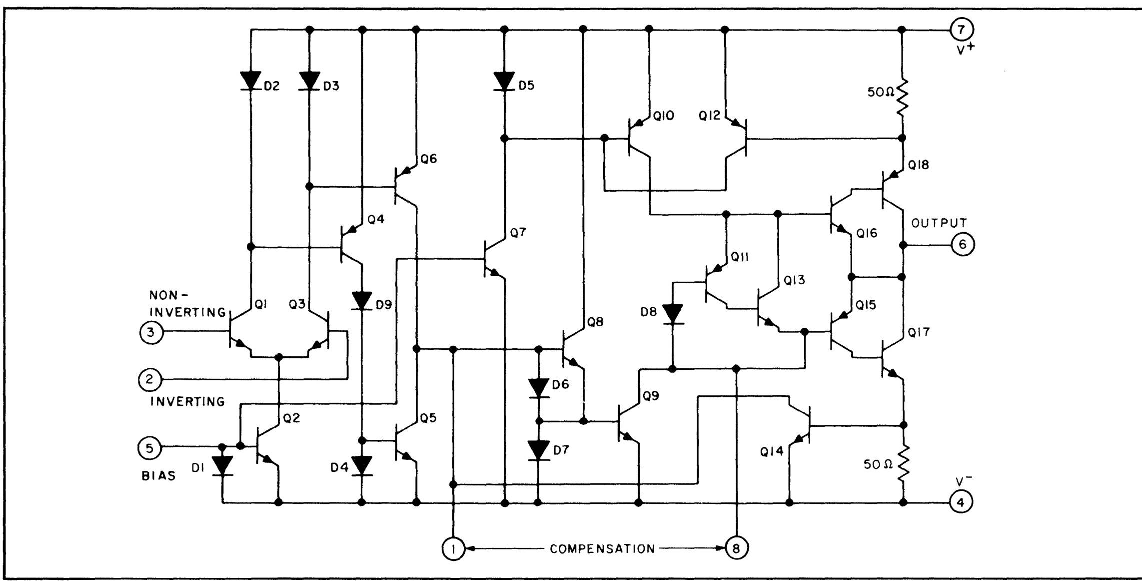
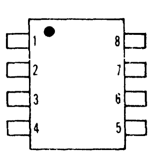


Figure 1. Schematic Diagram.

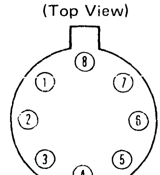
CONNECTION INFORMATION

NB, DE
Dual In-Line Package
(Top View)



Order Part Nos.:
RC3078NB, RC3078DE,
RM3078A DE

TE
Metal Can Package
(Top View)



Order Part Nos.:
RC3078T, RM3078A T

PIN	FUNCTION
1	COMP
2	INV. INPUT
3	NON-INV. INPUT
4	V^-
5	BIAS
6	OUTPUT
7	V^+
8	COMP

Micropower Operational Amplifier

3078
3078A

ABSOLUTE MAXIMUM RATINGS (Absolute Maximum Values at T_A = 25°C)

	3078	3078
DC Supply Voltage (between V^+ and V^- (terminal.	36V	14V
Differential Input Voltage.	±6V	±6V
DC Input Voltage	V^+ to V^-	V^+ to V^-
Input Signal Current	0.1 mA	0.1 mA
Output Short-Circuit Duration*	No Limitation	No Limitation
Device Dissipation	250 mW (up to (125°C)	500 mW (up to 70°C)
Temperature Range:		
Operating	-55 to +125°C	0 to +70°C
Storage	-65 to +150°C	-65 to +150°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)		
from case for 10s max.	+300°C	+300°C

*Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS (For Equipment Design)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			3078A R_{SET} = 5.1 MΩ, I_Q = 20 μA					3078 R_{SET} = 13MΩ, I_Q = 100 μA					UNITS
		V^+ & V^-	R_S KΩ	R_L KΩ	T_A = 25°C			T_A = -55 to 125°C		T_A = 25°C			T_A = 0 to 70°C		
					MIN	TYP	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Input Offset Voltage	V_{IO}		≤10	–	–	0.70	3.5	–	4.5	–	1.3	4.5	–	5	mV
Input Offset Current	I_{IO}		–	–	–	0.50	2.5	–	5.0	–	6	32	–	40	nA
Input Bias Current	I_{IB}		–	–	–	7	12	–	50	–	60	170	–	200	nA
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	92	100	–	90	–	88	92	–	86	–	dB
Total Quiescent Current	I_Q		–	–	–	20	25	–	45	–	100	130	–	150	μA
Device Dissipation	P_D		–	–	–	240	300	–	540	–	1200	1560	–	1800	μW
Maximum Output Voltage	V_{OM}	6	–	≥10	±5.1	±5.3	–	±5	–	±5.1	±5.3	–	±5.0	–	V
Common-Mode Input Voltage Range	V_{ICR}		≤10	–	–	-5.5 to +5.8	–	-5 to +5	–	–	-5.5 to +5.8	–	-5 to +5	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	80	115	–	–	–	80	110	–	–	–	dB
Maximum Output Current	I_{OM}^+ or I_{OM}^-		–	–	–	12	–	6.5	30	–	12	–	6.5	30	mA
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V^+$		≤10	–	76	105	–	–	–	76	93	–	–	–	μV/V
Negative	$\Delta V_{IO}/\Delta V^-$			–	76	105	–	–	–	76	93	–	–	–	
										R_{SET} = 13 MΩ, I_Q = 20 μA					
Input Offset Voltage	V_{IO}		≤10	–	–	1.4	3.5	–	4.5	–	–	–	–	–	mV
Open-Loop Diff. Voltage Gain	A_{OL}		–	≥10	92	100	–	88	–	–	–	–	–	–	dB
Total Quiescent Current	I_Q	15	–	–	–	20	30	–	50	–	–	–	–	–	μA
Device Dissipation	P_D		–	–	–	600	750	–	1350	–	–	–	–	–	μW
Maximum Output Voltage	V_{OM}		–	≥10	13.7	14.1	–	13.5	–	–	–	–	–	–	V
Common-Mode Rejection Ratio	CMRR		≤10	–	80	106	–		–	–	–	–	–	–	dB
Input Bias Current	I_{IB}		–	–	–	7	14	–	55	–	–	–	–	–	nA
Input Offset Current	I_{IO}		–	–	–	0.50	2.7	–	5.5	–	–	–	–	–	nA

ELECTRICAL CHARACTERISTICS (At $T_A = 25^\circ C$)

TYPICAL VALUES				UNITS	CURVES FIG. NO.	CHARACTERISTICS
3078A		3078				
$V^+ = +1.3V$, $V^- = -1.3V$, $R_{SET} = 2M\Omega$, $I_Q = 10\ \mu A$	$V^+ = +0.75V$, $V^- = -0.75V$, $R_{SET} = 10M\Omega$, $I_Q = 1\ \mu A$	$V^+ = +1.3V$, $V^- = -1.3V$, $R_{SET} = 2M\Omega$, $I_Q = 10\ \mu A$	$V^+ = 0.75V$, $V^- = -0.75V$, $R_{SET} = 10M\Omega$, $I_Q = 10\ \mu A$			
0.7	0.9	1.3	1.5	mV	3, 13	V_{IO}
0.3	0.054	1.7	0.5	nA	4, 14	I_{IO}
3.7	0.45	9	1.3	nA	5, 15	I_{IB}
84	65	80	60	dB	6, 11, 12, 16	A_{OL}
10	1	10	1	μA	17	I_Q
26	1.5	26	1.5	μW	–	P_D
1.4	0.3	1.4	0.3	V	9, 10	V_{OPP}
-0.8 to +1.1	-0.2 to +0.5	-0.8 to +1.1	-0.2 to +0.5	V	10	V_{ICR}
100	90	100	90	dB	–	CMRR
12	0.5	12	0.5	mA	8	$I_{OM}^{\pm}$
20	50	20	50	$\mu V/V$	–	$\Delta V_{IO}/\Delta V\pm$

(Typical Values Intended Only for Design Guidance at $T_A = 25^\circ C$ and $V^+ = +6V$, $V^- = -6V$)

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	3078A		3078	UNITS
			$R_{SET} = 5.1M\Omega$, $I_Q = 20\ \mu A$	$R_{SET} = 1M\Omega$, $I_Q = 100\ \mu A$	$R_{SET} = 1M\Omega$, $I_Q = 100\ \mu A$	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10\ K\Omega$	5	6	6	$\mu V/^\circ C$
Input Offset Current Drift	$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10\ K\Omega$	6.3	70	70	$pA/^\circ C$
Open-Loop Bandwidth	BW_{OL}	3 dB pt.	0.3	2	2	kHz
Slew Rate: Unity Gain	SR	See Figures 20, 21	0.027	0.04	0.04	$V/\mu s$
Slew Rate: Comparator	SR	See Figures 20, 21	0.5	1.5	1.5	$V/\mu s$
Transient Response	–	10% to 90% Rise Time	3	2.5	2.5	μs
Input Resistance	R_I		7.4	1.7	0.87	$M\Omega$
Output Resistance	R_O		1	0.8	0.8	$K\Omega$
Equiv. Input Noise Voltage	e_N (10 Hz)	$R_S = 0$	36	–	19	$nV/\sqrt{Hz}$
Equiv. Input Noise Current	i_N (10 Hz)	$R_S = 1M\Omega$	0.4	–	1	$pA/\sqrt{Hz}$

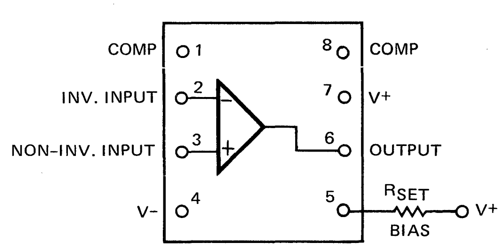


Figure 2. Functional Block Diagram of the 3078 and 3078A.

TYPICAL CHARACTERISTICS

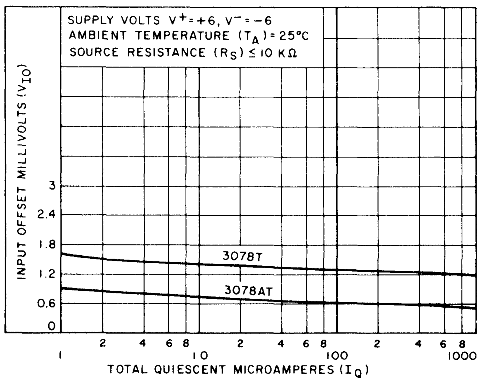


Figure 3. Input Offset Voltage versus Total Quiescent Current

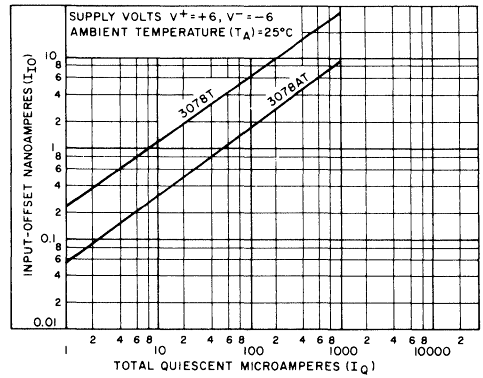


Figure 4. Input Offset Current versus Total Quiescent Current

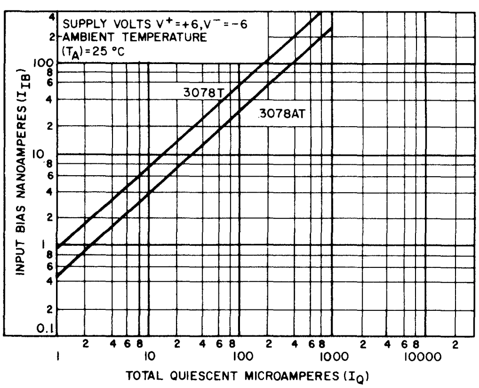


Figure 5. Input Bias Current versus Total Quiescent Current

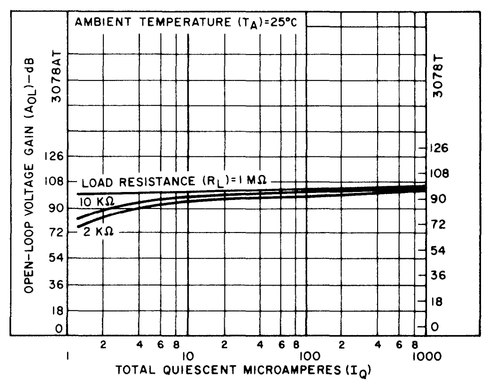


Figure 6. Open-loop Voltage Gain versus Total Quiescent Current

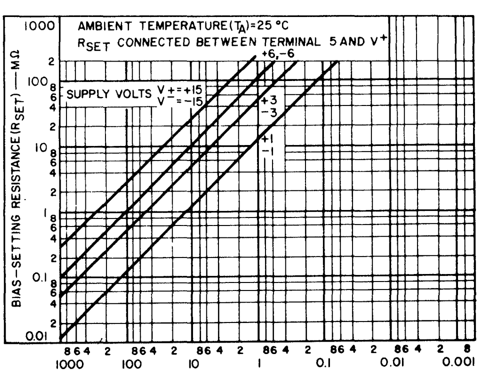


Figure 7. Bias-setting Resistance versus Total Quiescent Current

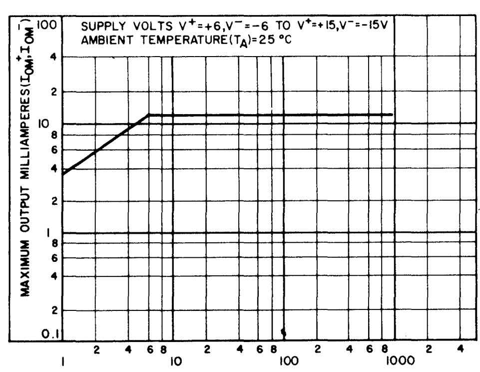


Figure 8. Maximum Output Current versus Total Quiescent Current

TYPICAL CHARACTERISTICS

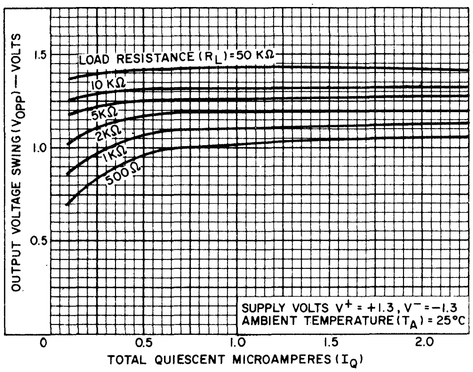


Figure 9. Output Voltage Swing versus Total Quiescent Current

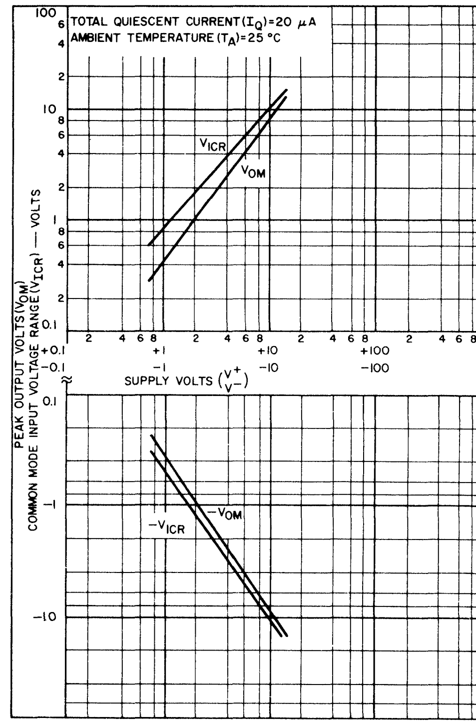


Figure 10. Output and Common-mode Voltage versus Supply Voltage

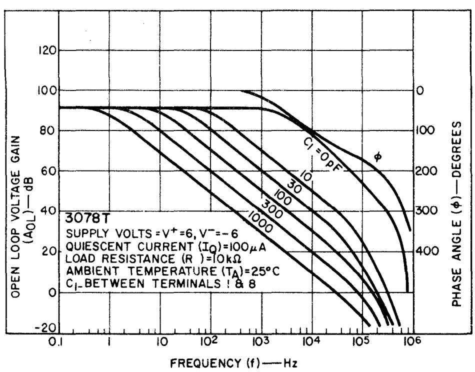


Figure 11. Open-loop Voltage Gain versus Frequency—3078

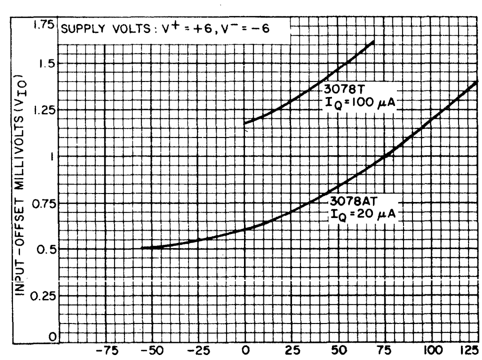


Figure 13. Input Offset Voltage versus Temperature

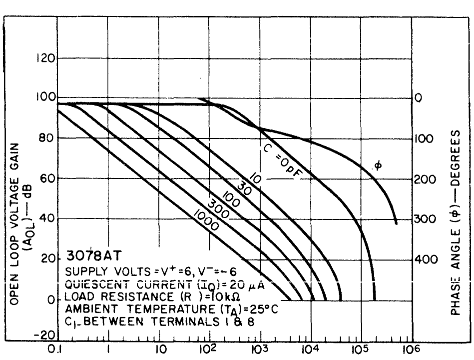


Figure 12. Open-loop Voltage Gain versus Frequency—3078A

Micropower Operational Amplifier

TYPICAL CHARACTERISTICS

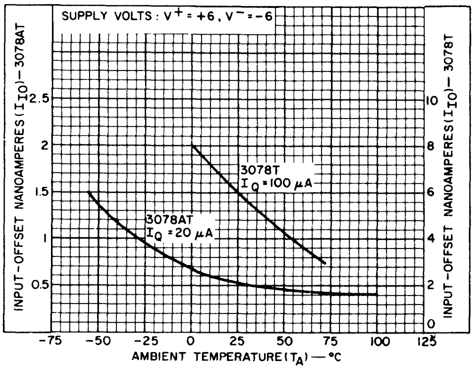


Figure 14. Input Offset Current versus Temperature

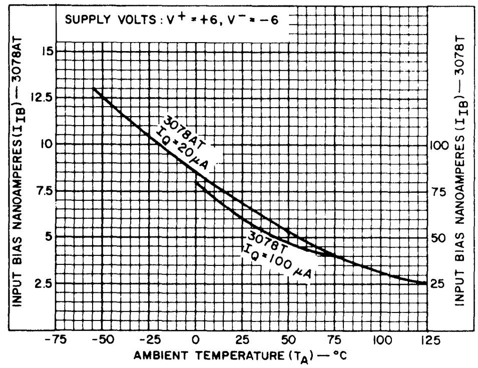


Figure 15. Input Bias Current versus Temperature

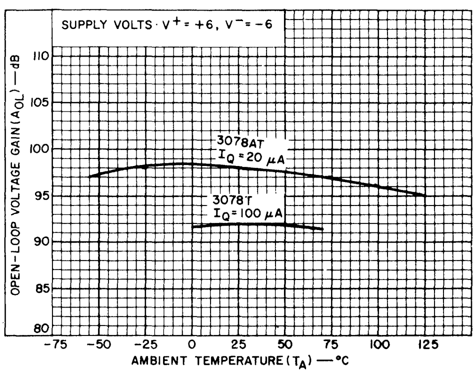


Figure 16. Open-loop Voltage Gain versus Temperature

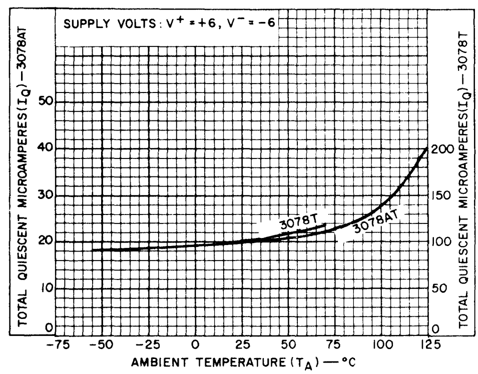


Figure 17. Total Quiescent Current versus Temperature

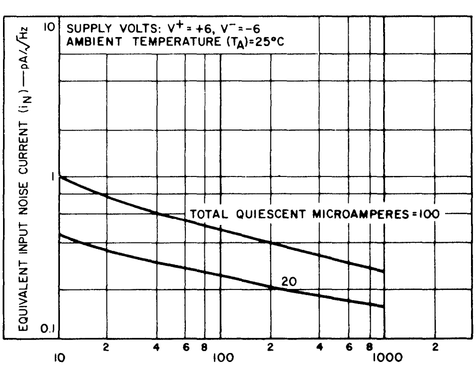


Figure 18. Equivalent Input Noise Voltage versus Frequency

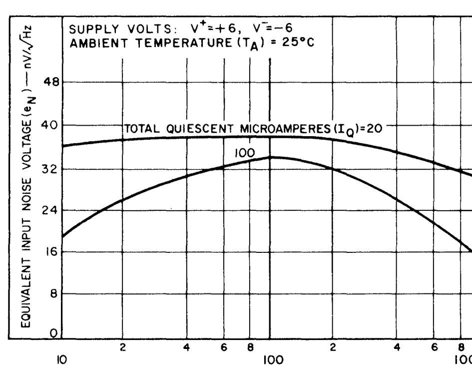


Figure 19. Equivalent Input Noise Current versus Frequency

TYPICAL CHARACTERISTICS

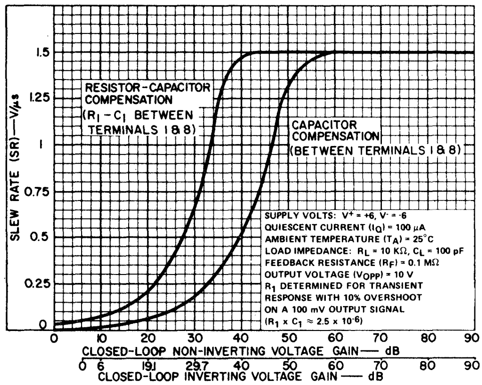


Figure 20. Slew Rate versus Closed-loop Gain—3078

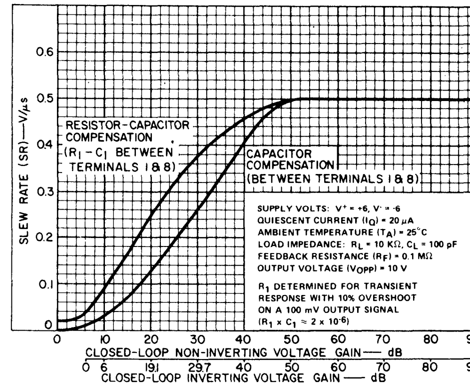


Figure 21. Slew Rate versus Closed-loop Gain—3078A

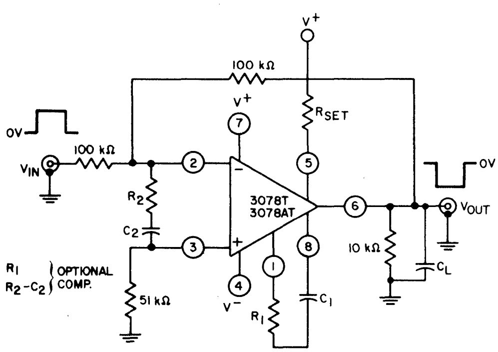


Figure 22. Transient Response and Slew-rate Unity Gain (Inverting) Test Circuit

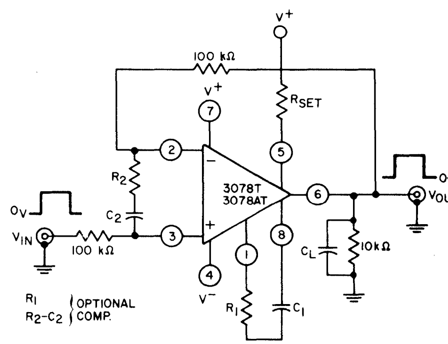


Figure 23. Slew-rate, Unit Gain (Non-Inverting) Test Circuit

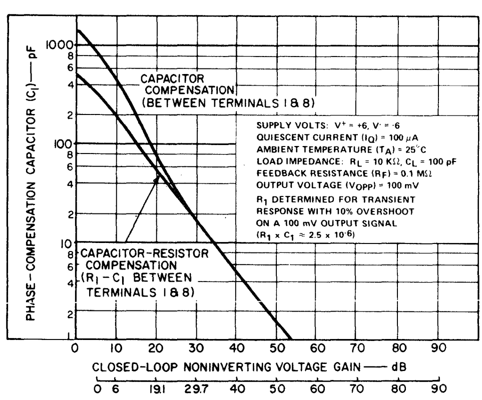


Figure 24. Phase Compensation Capacitance versus Closed-loop Gain—3078

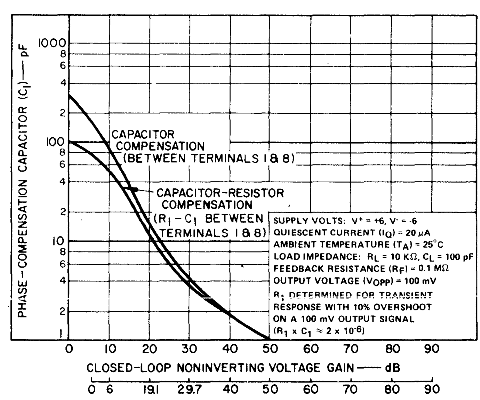


Figure 25. Phase Compensation Capacitance versus Closed-loop Gain—3078A

Micropower Operational Amplifier

Table 1. Unity-gain Slew Rate versus Compensation—3078 and 3078A

SUPPLY VOLTS: $V^+ = 6$, $V^- = -6$; OUTPUT VOLTAGE (V_O) = ±5V; LOAD RESISTANCE (R_L) = 10 KΩ	TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE OF 100 mV; AMBIENT TEMPERATURE (T_A) = 25°C									
	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
COMPENSATION TECHNIQUE	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
3078T—I_Q = 100 μA	KΩ	pF	KΩ	μF	V/μs	KΩ	pF	KΩ	μF	V/μs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor and Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
3078AT—I_Q = 20 μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor and Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

OPERATING CONSIDERATIONS

Compensation Techniques

The 3078AT and 3078T can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figures 24 and 25. These curves represent the compensation necessary at quiescent currents of 20 μA and 100 μA, respectively, for a transient with 10% overshoot. Figures 21 and 22 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 20 μA and 100 μA.

Single Supply Operation

The 3078AT and 3078T can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figures 27 and 28 show the 3078AT or 3078T in inverting and non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300 mV p-p with a 20 KΩ load.

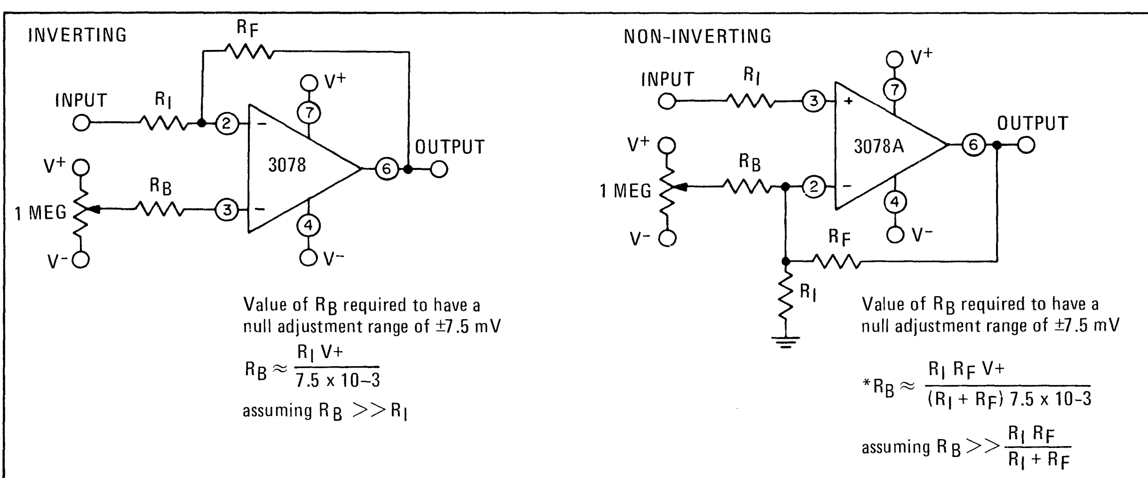


Figure 26. Offset Voltage Null Circuit

SCHEMATIC DIAGRAM

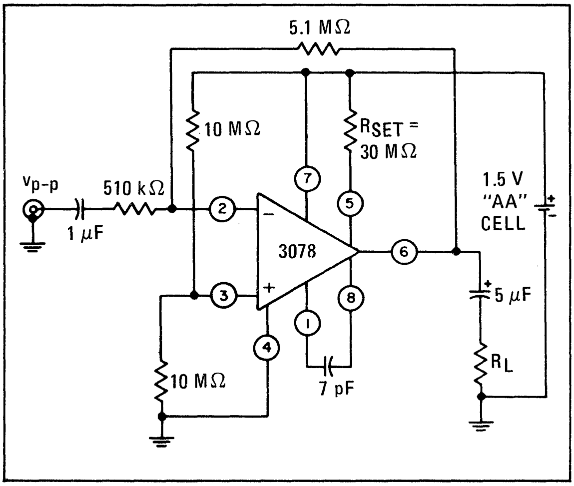


Figure 27. Inverting 20 dB Amplifier Circuit

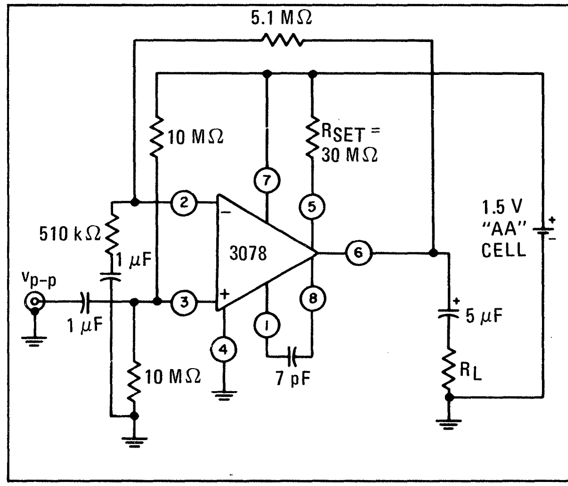


Figure 28. Non-inverting 20 dB Amplifier Circuit

Quad Operational Amplifiers

GENERAL DESCRIPTION

The RV3301 and RC3401 consist of four independent amplifiers, with internal frequency compensation, designed to operate from a single power supply.

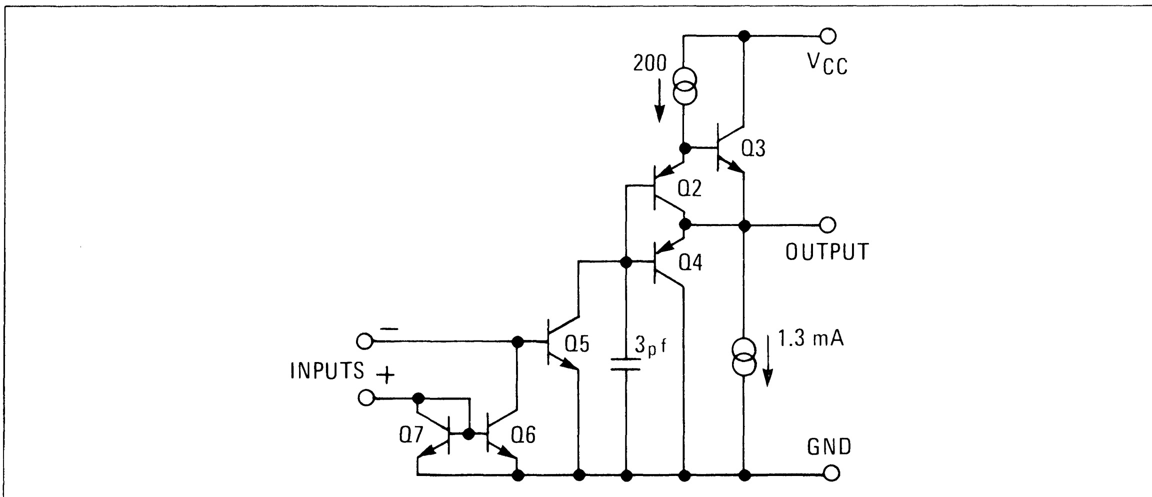
These amplifiers employ a current mirror to achieve the non-inverting inputs.

The current-differencing inputs allow a variety of applications in automotive instrumentation, industrial and consumer circuits for performing active filtering and pulse and waveform generation and processing.

DESIGN FEATURES

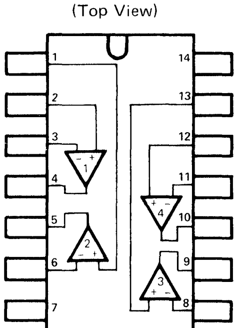
- Wide Supply Voltage Range 4 to 28 V
- Wide Operating Temperature Range −40°C to +85°C
- Wide Bandwidth Unity Gain 4 MHz
- Low Input Bias Current 50 nA

SCHEMATIC DIAGRAM



CONNECTION INFORMATION

DB
Dual In-Line Package
(Top View)



Order Part Nos.:
RV3301DB, RC3401DB

PIN	FUNCTION
1	+INPUT 2
2	+INPUT 1
3	-INPUT 1
4	OUTPUT 1
5	OUTPUT 2
6	-INPUT 2
7	GROUND
8	-INPUT 3
9	OUTPUT 3
10	OUTPUT 4
11	-INPUT 4
12	+INPUT 4
13	+INPUT 3
14	V_{CC}

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	
3301	+28V
3401	+18V
Non Inverting Input Current	5 mA
Sink Current	50 mA
Source Current	50 mA
Power Dissipation (Package Limitation)	625 mW
Derate above T_A = +25°C	5 mW/°C
Operating Temperature Range	3301: -40°C to +85°C
	3401: 0°C to +75°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10s)	300°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15V, R_L = 5.0KΩ, T_A = +25°C unless otherwise noted.)

Characteristic	Conditions	NOTE	3301 MIN	3301 TYP	3301 MAX	3401 MIN	3401 TYP	3401 MAX	UNIT
Open-Loop Voltage Gain		1							V/V
	T_A = +25°C		1000	2000		1000	2000		
	-40°C ≤ T_A ≤ 85°C			1600					
	0°C ≤ T_A ≤ 75°C					800			
Quiescent Power Supply Current (Total for 4 amplifiers)		2							mA
Noninverting inputs open				6.9	10		6.9	10	
Noninverting inputs grounded				7.8	14		7.8	14	
Input Bias Current	R_L = ∞	3							nA
	T_A = +25°C			50	300		50	300	
	-40°C ≤ T_A ≤ +85°C			100					
	0°C ≤ T_A ≤ +75°C							500	
Current Mirror Gain	I_r = 200μA	4	0.80	0.98	1.16				A/A
Current Mirror Gain Drift									%
	-40°C ≤ T_A ≤ +85°C			±2.5					
Output Current		5							mA
Source Capability	(V_{OH} = 0.4V)		3.0	10		5.0	10		
	(V_{OH} = 9.0V)			7.0					
Sink Capability	(V_{OL} = 0.4V)		0.5	0.87		0.5	1.0		
Output Voltage		6							V
High Voltage			13.5	14.2		13.5	14.2		
Low Voltage	(Inverting Input Driven)			0.03	0.1		0.03	0.1	
	(Noninverting Input Driven)			0.6					
Undistorted Output Swing	(0°C < T_A < +75°C)	7				10	13.5		V(p-p)
Input Resistance	(Inverting input only)		0.1	1.0		0.1	1.0		MΩ
Slew Rate	(C_L = 100 pF, R_L = 5.0 k)			0.6			0.6		V/μs
Unity Gain Bandwidth		8		4.0			5.0		MHz
Phase Margin		8		70			70		Degrees
Power Supply Rejection	(f = 100 Hz)	9		55			55		dB
Channel Separation	(f = 1.0 kHz)			65			65		dB

NOTES:
1. Open loop voltage gain is defined as the voltage gain from the inverting input to the output.
2. The quiescent current will increase approximately 0.3 mA for each noninverting input which is grounded. Leaving the noninverting input open causes the apparent input bias current to increase slightly (100 nA) at high temperatures.
3. Input bias current can be defined only for the inverting input. The noninverting input is not a true "differential input"—as with a conventional IC operational amplifier. As such this input does not have a requirement for input bias current.
4. Current mirror gain is defined as the current demanded at the inverting input divided by the current into the noninverting input.
5. Sink current is specified for linear operation. When the device is used as a gate or a comparator (non-linear operation), the sink capability of the device is approximately 5.0 milliamperes.
6. When used as a noninverting amplifier, the minimum output voltage is the V_{BE} of the inverting input transistor.
7. Peak-to-peak restrictions are due to the variations of the quiescent dc output voltage in the standard configuration.
8. Bandwidth and phase margin are defined with respect to the voltage gain from the inverting input to the output.
9. Power supply rejection is specified at closed loop unity gain, and therefore indicates the supply rejection of both the biasing circuitry and the feedback amplifier.

Total Quad Operational Amplifiers

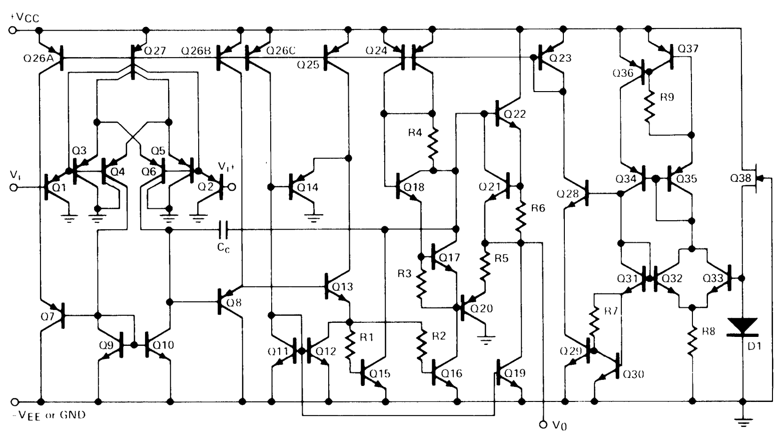
GENERAL DESCRIPTION

The 3403A high performance quad op-amp features improved large signal bandwidth and worst case DC specs equal to or better than the standard 741 type general purpose op-amp. The device uses a newly developed type of ground-sensing differential input stage which provides increased slew rate.

DESIGN FEATURES

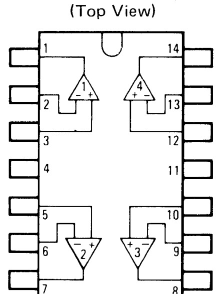
- Class AB Output State; No Crossover Distortion
- Output Voltage Swings to Ground in Single Supply Operations
- High Slew Rate 1.2 V/μs
- Single or Split Supply Operation
- Wide Supply Operation 2.5 V to +36 V or ±1.25 V to ±18 V
- Pin Compatible with LM324 and 3403
- Low Power Consumption 0.8 mA/amplifier

SCHEMATIC DIAGRAM (1/4 Shown)



CONNECTION INFORMATION

DB and DC
Dual In-line Packages
(Top View)



PIN	FUNCTION
1	OUTPUT 1
2	-INPUT 1
3	+INPUT 1
4	V^+
5	+INPUT 2
6	-INPUT 2
7	OUTPUT 2
8	OUTPUT 3
9	-INPUT 3
10	+INPUT 3
11	GROUND
12	+INPUT 4
13	-INPUT 4
14	OUTPUT 4

Order Part Nos.:
RC3403ADB, RC3403ADC, RV3403ADB,
RV3403ADC, RM3503ADC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V^+ . . . . 36 V or ±18 V
Differential Input Voltage . . . . 36 V
Input Voltage . . . . -0.3 V to +36 V
Power Dissipation
"DB" package . . . . 500 MW (molded DIP epoxy "B")
"DC" package . . . . 650 mW (hermetic DIP)

Operating Temperature Range
RM3503A . . . . -55°C to +125°C
RC3403A . . . . 0°C to +70°C
RV3403A . . . . -40°C to +85°C
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering, 60s) . . . . 300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±15V unless otherwise noted)

PARAMETER	CONDITIONS	RM3503A			RC/RV3403A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S = 0$		2	4		2	5	mV
Input Offset Current	I_{in-} or I_{in+}		±30	±50		±30	±50	nA
Input Bias Current	I_{in-} or I_{in+}		-100	-200		-100	-200	nA
Input Common Mode Voltage Range		0		$V^+ - 2$	0		$V^+ - 2$	V
Supply Current	$R_L = \infty$ on all op-amps		3	4		3	5	mA
Large Signal Voltage Gain	$R_L > 2K\Omega$	50	100		25*	100		V/mV
Output Voltage Swing	$R_L = 2K\Omega$	±13	±14		±13	±14		V
Common Mode Rejection Ratio	DC	80	90		80	90		dB
Channel Separation	±1kHz to 20 kHz (in ref)		-120			-120		dB
Output Source Current	V_{IN+} = 1 V V_{IN-} = 0 V	20	40		20	40		mA
Output sink current		10	20		10	20		mA
Small signal bandwidth			2			2		MHz
Slew Rate	$A_V = 1, -10<V_i<+10$		1.2			1.2		V/µs
Distortion (Crossover)	f = 20 kHz, VO = $10V_{pp}$		1			1		%
Power Bandwidth	VO = $10V_{pp}$		40			40		kHz
Power Supply Rejection Ratio			20	45		20	100	µV/V

ELECTRICAL CHARACTERISTICS GUARANTEED OVER TEMPERATURE

Range: RM3503A: -55°C to +125°C
RC3403A: 0°C to +70°C
RV3403A: -40°C to +85°C

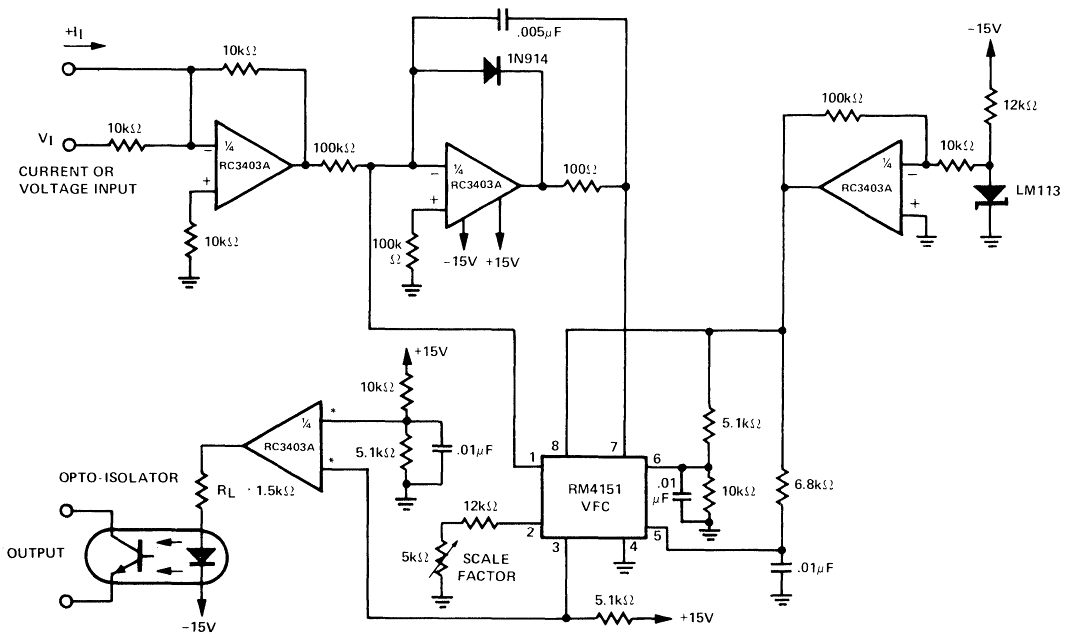
PARAMETER	RM3503A		RC3403A		RV3403A		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	
Input Offset Voltage	–	6.0	–	10.0	–	10.0	mV
Input Offset Current	–	200	–	200	–	200	nA
Input Bias Current	–	-1500	–	-800	–	-1500	nA
Large Signal Voltage Gain	25	–	15	–	15	–	V/mV
Output Voltage Swing	±10	–	±10	–	±10	–	V

LOW VOLTAGE ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{EE} = GND, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS	RM3503A MIN	RM3503A TYP	RM3503A MAX	RC/RV3403A MIN	RC/RV3403A TYP	RC/RV3403A MAX	UNITS
Input Offset Voltage	$R_S = 0\Omega$		2.0	5.0		2.0	10	mV
Input Offset Current	$I_{in-} - I_{in+}$		30	50		30	50	nA
Input Bias Current	$I_{in-} + I_{in+}/2$		-100	-200		-100	-200	nA
Large Signal Voltage Gain	$R_L = 2K\Omega$	20	200		20	200		V/mW
Power Supply Rejection Ratio				50			150	μV/V
Output Voltage Range[1]	$R_L = 10K\Omega$	3.5			3.5			$V_{p\text{-}p}$
Power Supply Current	$R_L = \infty$, all amplifiers		2.5	4.0		2.5	5.0	mA
Channel Separation	1KHz≤f≤.2MHz (input referred)		-120			-120		dB

[1] Output will swing to ground.

3403A TYPICAL APPLICATIONS

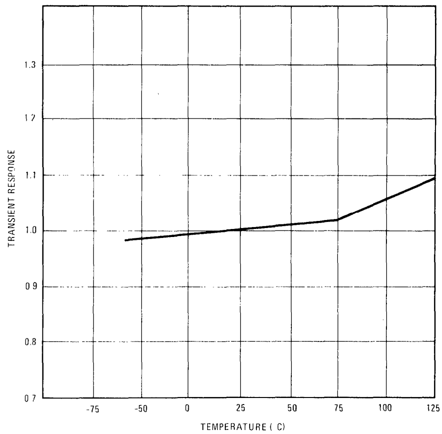


*POLARITY DETERMINED BY DESIRED LED RESPONSE;
I.E., LED ON FOR DATA HIGH, OR LED HIGH FOR DATA LOW.

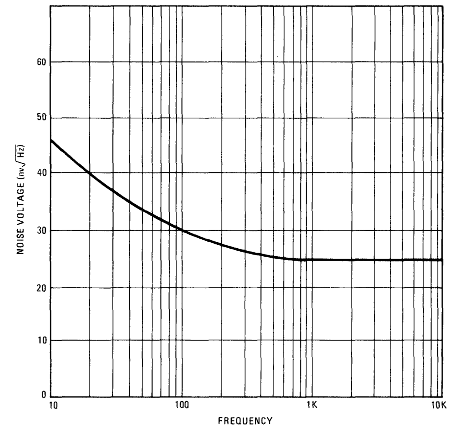
PRECISION POSITIVE-INPUT, ISOLATED OUTPUT VOLTAGE FREQUENCY CONVERTER

TYPICAL ELECTRICAL DATA

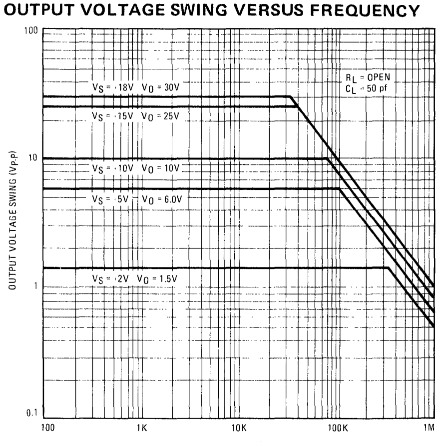
TRANSIENT RESPONSE VERSUS TEMPERATURE



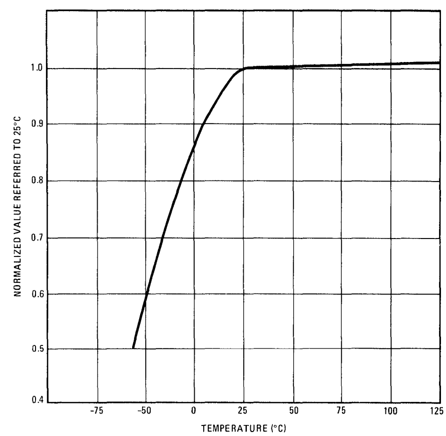
NOISE VERSUS FREQUENCY



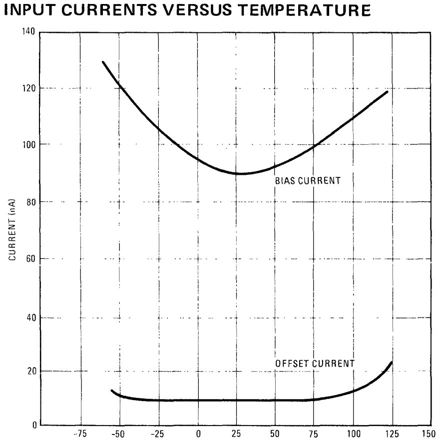
OUTPUT VOLTAGE SWING VERSUS FREQUENCY



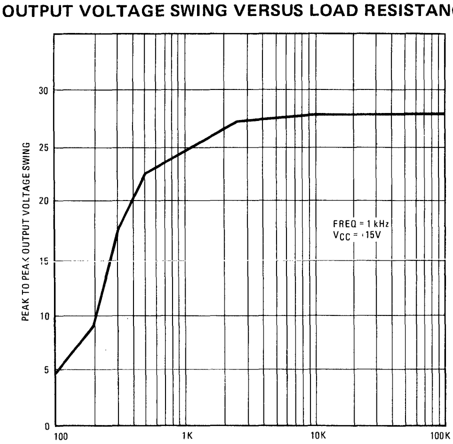
SLEW RATE VERSUS TEMPERATURE



INPUT CURRENTS VERSUS TEMPERATURE



OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



GENERAL DESCRIPTION

The RC4131/RM4131 are high performance, high gain, internally compensated operational amplifiers fabricated on a single silicon chip using the planar epitaxial process.

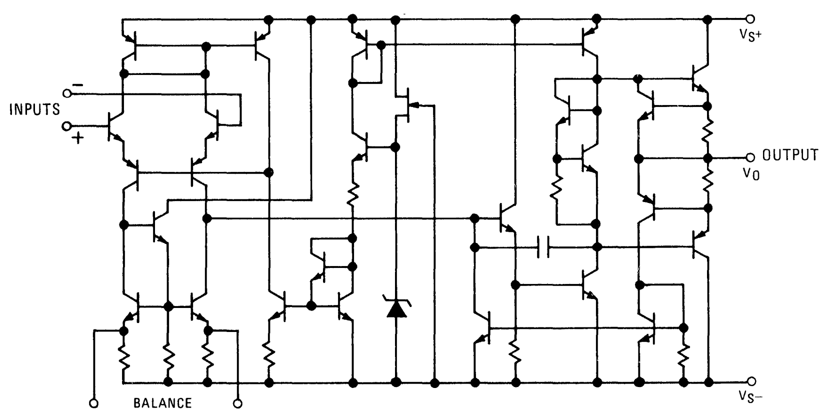
Designed as a pin for pin replacement for the RM709, they are also direct replacements for the 741 and LM107. Relative to these latter units, the RC4131/RM4131 features four times the slew rate, and ½ the power dissipation at ±20V.

High common-mode and differential voltage range, very low input bias current, optimum performance over a very wide range of supply voltage, freedom from "latch-up," and operation over the full military temperature range from −55°C to +125°C make the RM4131 ideal for use as a voltage follower, comparator, integrator, and summing or general purpose feedback amplifier. The RC4131 operates over a temperature range of 0°C to +70°C.

DESIGN FEATURES

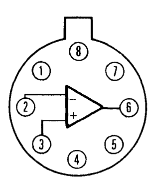
- 50nA Maximum Input Bias Current
- 10nA Maximum Input Offset Current
- 2mV Maximum Input Offset Voltage
- 1.1mA Current Drain at ±20V
- Offset Voltage Nulling (10kΩ pot.)
- 2.0V/μs Slew Rate
- 4MHz Unity Gain Bandwidth
- 3dB Gain. Variation From ±3V to ±20V
- 88dB Minimum Gain ±3V to ±20V, −55°C to +125°C

SCHEMATIC DIAGRAM



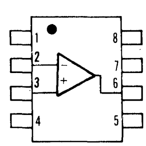
CONNECTION INFORMATION

TE (TO-99)
Metal Can Package
(Top View)



Order Part Nos.:
RM4131T, RC4131T

NB
Dual In-line Package
(Top View)



Order Part Nos.:
RC4131NB

PIN	FUNCTION
1	BAL
2	-INPUT
3	+INPUT
4	V⁻
5	BAL
6	OUTPUT
7	V⁺
8	NC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . RM4131: ±22V
RC4131: ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage . . . . ±30V
Input Voltage (Note 2) . . . . ±15V
Storage Temperature Range . . . . −65°C to +150°C

Operating Temperature Range
RM4131 . . . . −55°C to +125°C
RC4131 . . . . 0°C to +70°C
Lead Temperature (Soldering, 60s) . . . . 300°C
Output Short-Circuit Duration (Note 3) . . . . . . Indefinite

ELECTRICAL CHARACTERISTICS

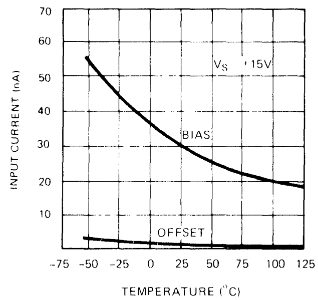
RM4131: $\pm3V < V_S < \pm20V$, $-55°C \leq T_A \leq +125°C$, unless otherwise specified.
RC4131: $\pm3V < V_S < \pm15V$, $0°C \leq T_A \leq +70°C$, unless otherwise specified.

PARAMETER	CONDITIONS	RM4131 MIN	RM4131 TYP	RM4131 MAX	RC4131 MIN	RC4131 TYP	RC4131 MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$, $T_A = +25°C$		0.7	2.0		1.5	5.0	mV
	$R_S \leq 10k\Omega$			3.0			6.0	mV
Input Offset Current	$T_A = +25°C$		1.5	10		3.0	20	nA
				20			30	nA
Input Bias Current	$T_A = +25°C$		30	50		70	150	nA
				100			200	nA
Input Resistance		2.2	3.5		0.7	3.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$ (Note 4), $T_A = +25°C$	50	160		35	160		V/mV
	$R_L \geq 2k\Omega$ (Note 4)	25			25			V/mV
Output Voltage Swing RM4131: $V_S = \pm20V$ RC4131: $V_S = \pm15V$	$R_L \geq 10k\Omega$	±16			±12			V
	$R_L \geq 2k\Omega$	±15			±10			V
Input Voltage Range	RM4131: $V_S = \pm20V$ RC4131: $V_S = \pm15V$	±15			±11			V
Common-Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	100		70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$	80	100		70	100		dB
Supply Current	$R_L = \infty$, $T_A = +25°C$		1.1	1.6		1.3	1.9	mA
	$R_L = \infty$			1.9				mA
Average Temperature Coefficient of Input Offset Voltage			3.0	15		5.0	20	μV/°C
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$		0.01	0.1				nA/°C
	$-55°C \leq T_A \leq 25°C$		0.02	0.2				nA/°C
	$25°C \leq T_A \leq 70°C$					0.01	0.1	nA/°C
	$0°C \leq T_A \leq 25°C$					0.02	0.2	nA/°C
Slew Rate (Unity Gain)	$R_L \geq 2k\Omega$		2.0			2.0		V/μs
Bandwidth (Unity Gain)			4.0			4.0		MHz

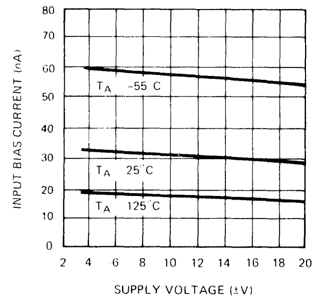
NOTES:
1. Rating applies for case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature of +75°C ambient temperature.
4. RM4131: $V_S = \pm3.0V$, $V_o = \pm1.3V$; $V_S = \pm20V$, $V_o = \pm15V$. RC4131: $V_S = \pm3V$, $V_o = \pm1.3V$; $V_S = \pm15V$, $V_o = \pm10V$.

TYPICAL ELECTRICAL DATA

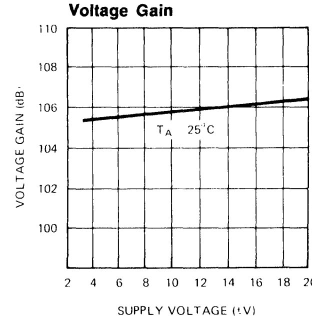
Input Current



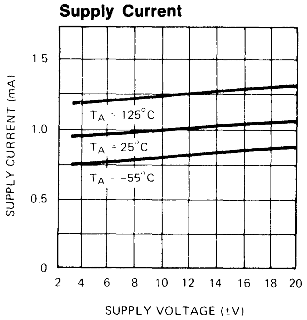
Input Bias Current



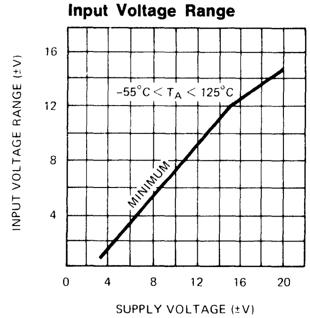
Voltage Gain



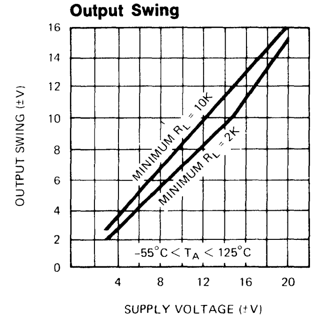
Supply Current



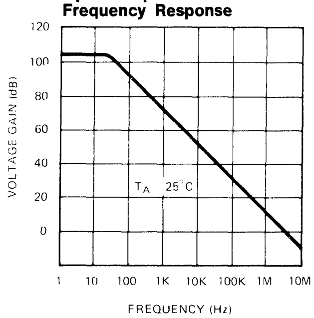
Input Voltage Range



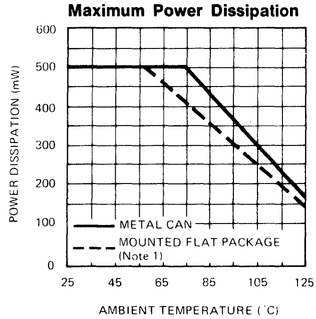
Output Swing



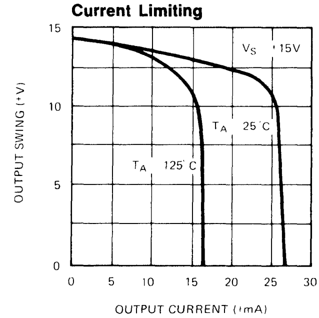
Open Loop Frequency Response



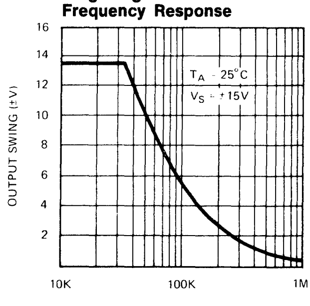
Maximum Power Dissipation



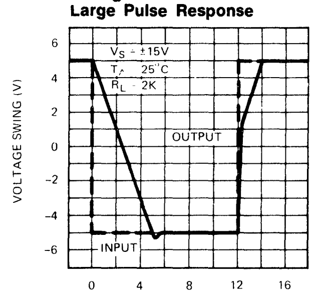
Current Limiting



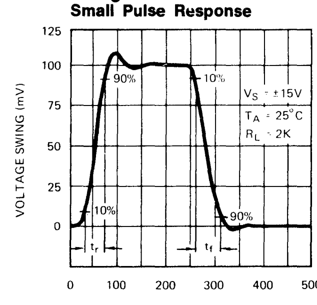
Large Signal Frequency Response



Voltage Follower Large Pulse Response

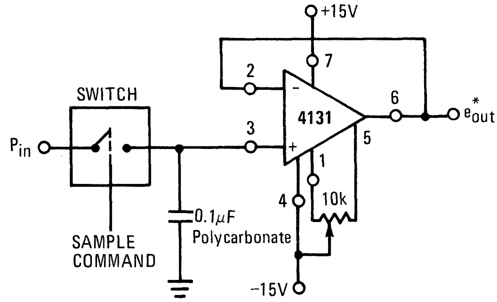


Voltage Follower Small Pulse Response

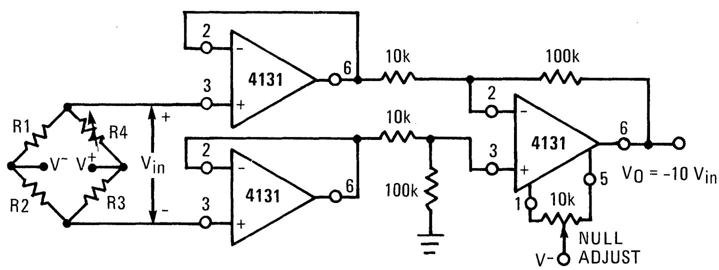


TYPICAL APPLICATIONS

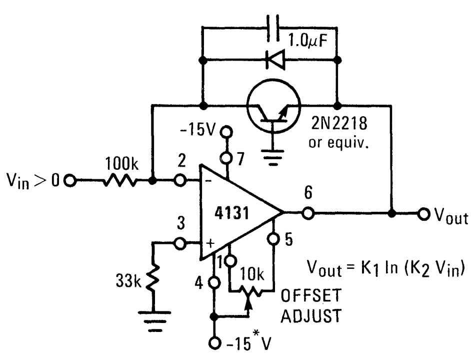
Low Drift Sample and Hold



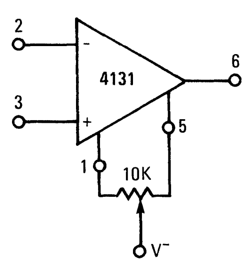
High Impedance Bridge Amplifier



Logarithmic Amplifier



Voltage Offset Null Circuit



Micropower Operational Amplifier 4132

DESIGN FEATURES

- 10 nA Maximum Input Bias Current
- 2 nA Maximum Input Offset Current
- 3 mV Maximum Input Offset Voltage
- 35 μA Maximum Current Drain at ±20V
- 20 MΩ Input Impedance
- ±10V Min Into a 5 KΩ Load
- 3 dB Gain Variation from ±3V to ±20V
- 94 dB Minimum Gain ±3V to ±20V, -55°C to +125°C

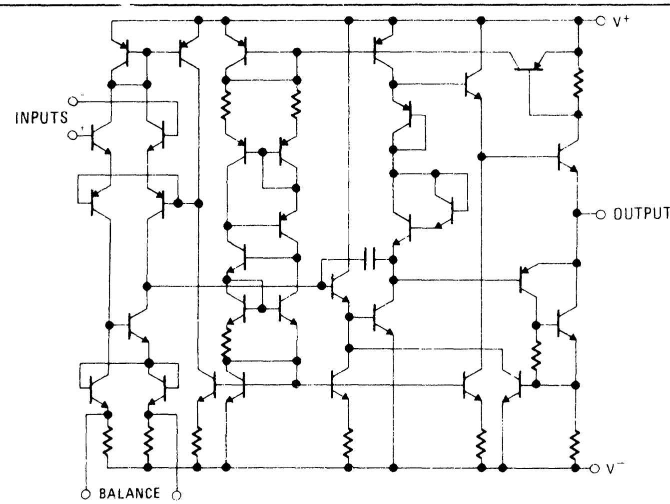
GENERAL DESCRIPTION

The RM4132/RC4132 are high performance, high gain, micropower, internally compensated operational amplifiers fabricated on a single silicon chip using the planar epitaxial process.

Designed for applications where power supply current is at a premium (such as in battery operated equipments), 4132 characteristics are very similar to those of the Raytheon 4131 general purpose operational amplifier.

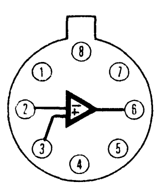
The RM4132 is pin compatible with the 709, 741, and 4131, and features high common mode and differential voltage range, 20 MΩ input impedance, optimum performance over a wide range of supply voltages, freedom from latch-up, and operation over the full military temperature range. The RC4132 operates over the commercial range of 0°C to +70°C.

SCHEMATIC DIAGRAM



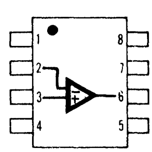
CONNECTION INFORMATION

TE (TO-99)
Metal Can Package
(Top View)



Order Part Nos.:
RM4132T, RC4132T

NB
Dual In-line Package
(Top View)



Order Part Nos.:
RC4132NB, RM4132DE,
RC4132DE

PIN	FUNCTION
1	BAL
2	-INPUT
3	+INPUT
4	V⁻
5	BAL
6	OUTPUT
7	V⁺
8	NC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	RM4132: ±22V RC4132: ±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
RM4132	-55°C to +125°C
RC4132	0°C to +70°C
Lead Temperature (Soldering, 60s)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS

($\pm3V \leqslant V_S \leqslant \pm20V$, RM4132: $-55°C \leqslant T_A \leqslant +125°C$; RC4132: $0°C \leqslant T_A \leqslant +70°C$ Unless otherwise specified)

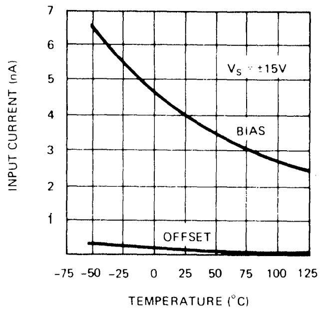
PARAMETER	CONDITIONS		RM4132 MIN	RM4132 TYP	RM4132 MAX	RC4132 MIN	RC4132 TYP	RC4132 MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10\ k\Omega$	25°C		0.7	3.0 4.0		1.5	5.0 6.0	mV
Input Offset Current		25°C		0.3	2.0 4.0		1.0	5.0 7.5	nA
Input Bias Current		25°C		4.0	10 20		10	25 35	nA
Input Resistance		25°C		20			10		MΩ
Large-Signal Voltage Gain	$R_L \geqslant 5\ k\Omega$, Note 4		50	160		50	160		V/mV
Output Voltage Swing	$V_S = \pm15V$	$R_L = 10\ K$	±12	±14		±12	±14		V
		$R_L = 5\ K$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm20V$		±15			±15			V
Common Mode Rejection Ratio	$R_S \leqslant 10\ k\Omega$		80	94		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10\ k\Omega$		80	94		70	90		dB
Supply Current	$T_A = 25°C$				45			50	μA
Average Temperature Coefficient of Input Offset Voltage				3.0	15		3.0	20	uV/°C
Average Temperature Coefficient of Input Offset Current	$25°C \leqslant T_A \leqslant 125°C$			2	20				pA/°C
	$-55°C \leqslant T_A \leqslant 25°C$			4	40				pA/°C
	$25°C \leqslant T_A \leqslant 70°C$						4	40	pA/°C
	$0°C \leqslant T_A \leqslant 25°C$						10	100	pA/°C
Slew Rate (unity gain)	25°C, $R_L = 5\ K$			0.13			0.13		V/μs
Bandwidth (unity gain)	25°C, $R_L = 5\ K$			150			150		kHz

NOTES:

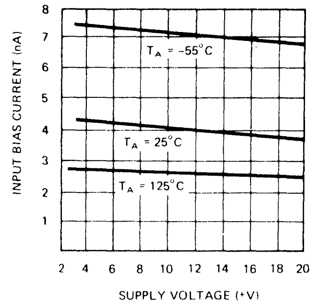
1. Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
4. V_{OUT} = guaranteed minimum output swing.

TYPICAL ELECTRICAL DATA

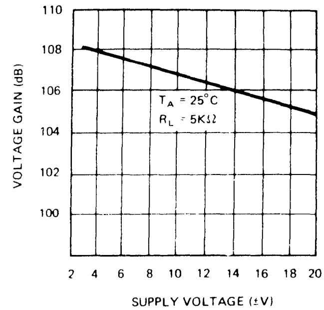
Input Current



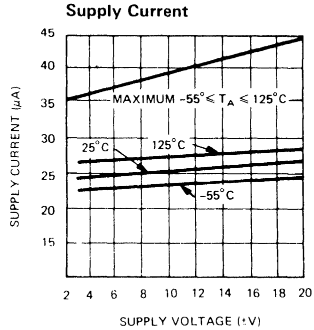
Input Bias Current



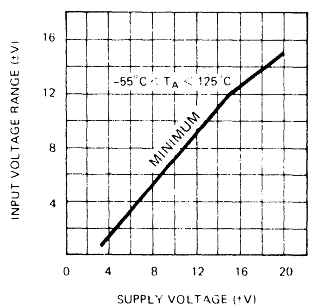
Voltage Gain



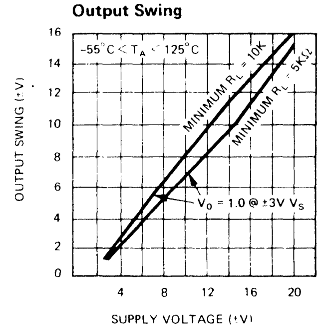
Supply Current



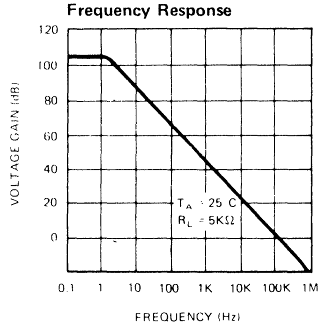
Input Voltage Range



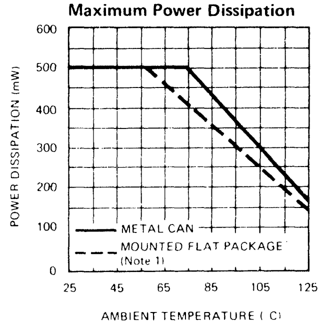
Output Swing



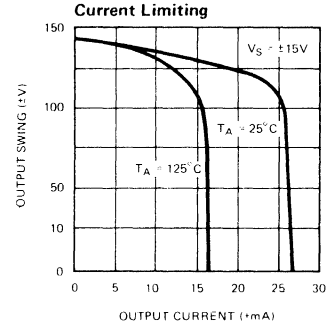
Open Loop
Frequency Response



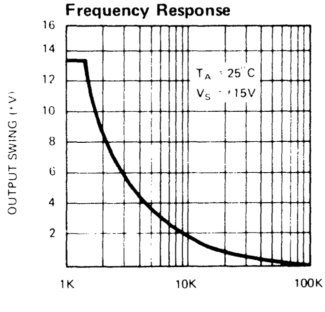
Maximum Power Dissipation



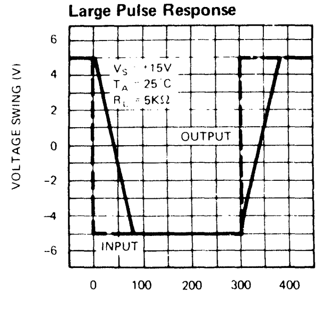
Current Limiting



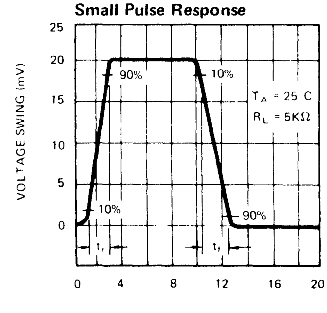
Large Signal
Frequency Response



Voltage Follower
Large Pulse Response

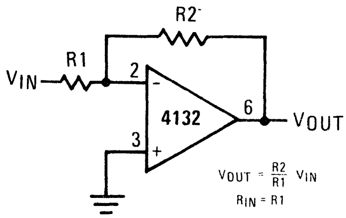


Voltage Follower
Small Pulse Response



TYPICAL APPLICATIONS

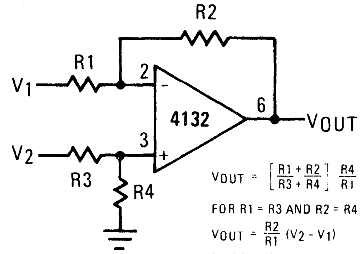
Inverting Amplifier



$V_{OUT} = \frac{R2}{R1} V_{IN}$

$R_{IN} = R1$

Difference Amplifier



$V_{OUT} = \left[\frac{R1 + R2}{R3 + R4}\right] \frac{R4}{R1} V_2 - \frac{R2}{R1} V_1$

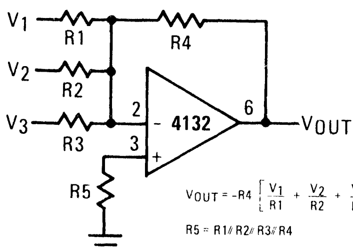
FOR R1 = R3 AND R2 = R4

$V_{OUT} = \frac{R2}{R1} (V_2 - V_1)$

R1//R2 = R3//R4

FOR MINIMUM OFFSET ERROR
DUE TO INPUT BIAS CURRENT

Inverting Summing Amplifier

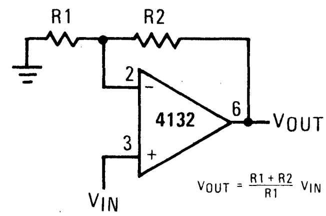


$V_{OUT} = -R4 \left[\frac{V1}{R1} + \frac{V2}{R2} + \frac{V3}{R3}\right]$

R5 = R1// R2// R3// R4

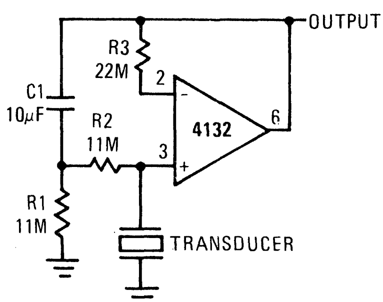
FOR MINIMUM OFFSET ERROR
DUE TO INPUT BIAS CURRENT

Non-Inverting Amplifier

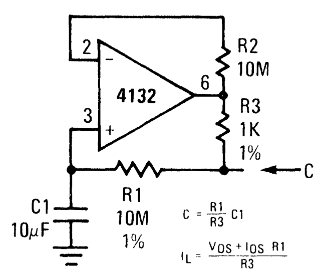


$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$

Amplifier for Piezoelectric Transducers



Capacitance Multiplier

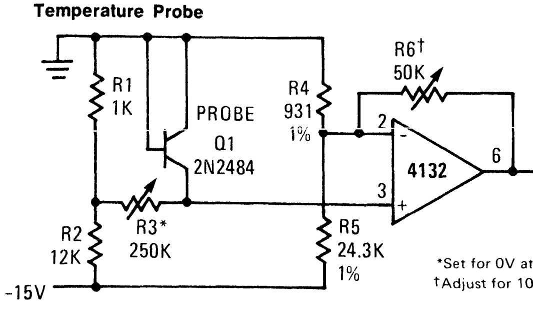


$C = \frac{R1}{R3} C1$

$I_L = \frac{V_{OS} + I_{OS} R1}{R3}$

$R_S = R3$

Temperature Probe



*Set for 0V at 0°C
†Adjust for 100 mV/°C

GENERAL DESCRIPTION

The RM4136 and RC4136 include four independent high gain operational amplifiers internally compensated and constructed on a single silicon chip using the planar epitaxial processes.

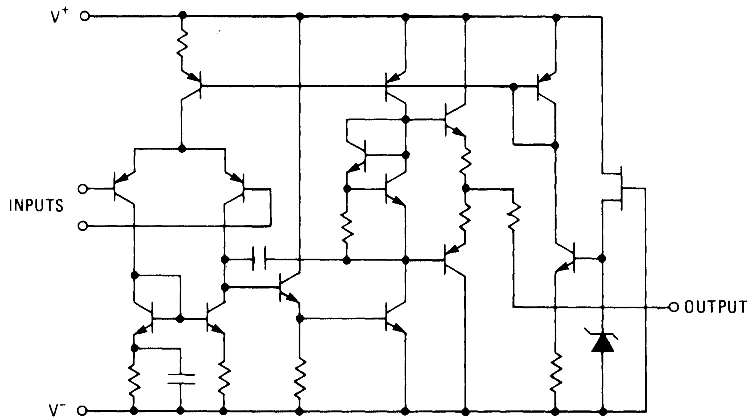
These amplifiers meet or exceed all specifications for 741 type amplifiers. Excellent channel separation allows the use of the 4136 quad amplifier in all 741 operational amplifier applications providing the highest possible packaging density.

The specially designed low noise input transistors allow the 4136 to be used in low noise signal processing applications such as audio preamplifiers and signal conditioners.

DESIGN FEATURES

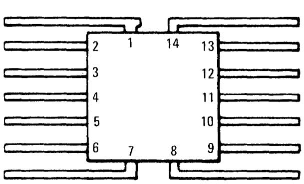
- Unity Gain Bandwidth, 3MHz
- Short-Circuit Protection
- No Frequency Compensation Required
- No Latch-up
- Large Common Mode and Differential Voltage Ranges
- Low Power Consumption
- Parameter Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers

SCHEMATIC DIAGRAM (1/4 Shown)



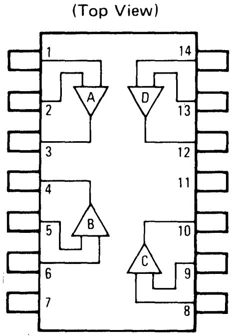
CONNECTION INFORMATION

CJ
Flatpak



Order Part No.:
RM4136CJ

DC and DB
Dual In-line Packages
(Top View)



Order Part Nos.:
RM4136DC, RV4136DB, RV4136DC,
RC4136DB, RC4136DC

PIN	FUNCTION
1	-INPUT (A)
2	+INPUT (A)
3	OUTPUT (A)
4	OUTPUT (B)
5	+INPUT (B)
6	-INPUT (B)
7	$-V_{CC}$
8	-INPUT C
9	+INPUT (C)
10	OUTPUT (C)
11	$+V_{CC}$
12	OUTPUT (D)
13	+INPUT (D)
14	-INPUT (D)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . RM4136: ±22V RV4136, RC4136: ±18V	Storage Temperature Range . . . . −65°C to +150°C
Internal Power Dissipation (Note 1) 800mW	Operating Temperature Range . . RM4136: −55°C to +125°C RC4136: 0°C to +70°C RV4136: −40°C to +85°C
Differential Input Voltage . . . . ±30V	Lead Temperature (Soldering, 60s) . . . . 300°C
Input Voltage (Note 2) . . . . ±15V	Output Short-Circuit Duration (Note 3) . . . . Indefinite

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_A = +25°C unless otherwise noted.)

PARAMETER	CONDITIONS	RM4136			RV4136, RC4136			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10$ kΩ		0.5	4.0		0.5	* 6.0	mV
Input Offset Current			5.0	150		5.0	* 200	nA
Input Bias Current			40	400		40	* 500	nA
Input Resistance		0.3	5.0		0.3	5.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ V_{out} = ±10V	50,000	300,000		* 20,000	300,000		V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		* ±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		* ±10	±13		V
Input Voltage Range		±12	±14		* ±12	±14		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	100		* 70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		10	150		10	* 150	µV/V
Power Consumption	$R_L = \infty$, All Outputs		210	340		210	* 340	mW
Transient Response (unity gain)	V_{in} = 20 mV R_L = 2 kΩ $C_L \leq 100$ pF							
Risetime			0.13			0.13		µs
Overshoot			5.0			5.0		%
Unity Gain Bandwidth			3.0			3.0		MHz
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		1.5			1.0		V/µs
Channel Separation (Gain = 100)	f = 10 kHz R_S = 1 kΩ		90			90		dB
The following specifications apply for −55°C ≤ T_A ≤ +125°C for RM4136; 0°C ≤ T_A ≤ +70°C for RC4136.								
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0			* 7.5	mV
Input Offset Current				* 500			300	nA
Input Bias Current				* 1500			800	nA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ V_{out} = ±10V	25,000			* 15,000			V/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			* ±10			V
Power Consumption	T_A = High		180	300		180	* 300	mW
	T_A = Low		240	400		240	* 400	mW

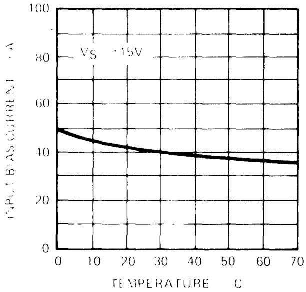
* = RV limits

NOTES:

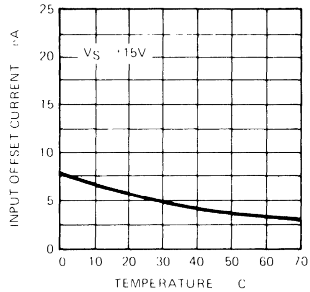
1. Rating applies for case temperature to +25°C; derate linearly at 6.4 mW/°C for ambient temperatures above +25°C.
2. For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground or one amplifier only. I_{CC} = 45mA (typical).

TYPICAL ELECTRICAL DATA

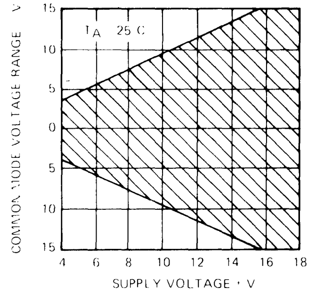
Input Bias Current as a Function of Ambient Temperature



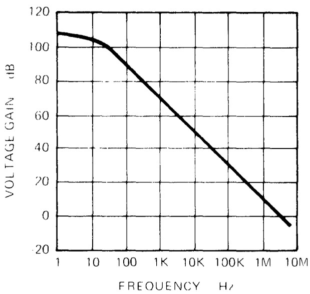
Input Offset Current as a Function of Ambient Temperature



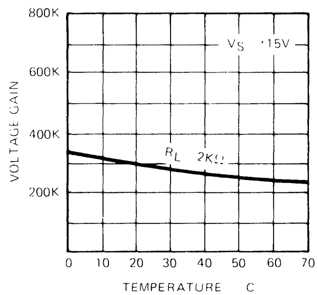
Common Mode Range as a Function of Supply Voltage



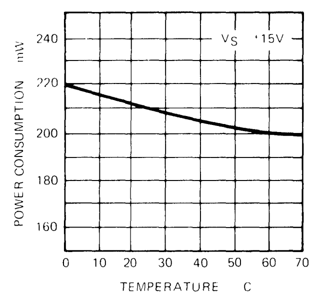
Open Loop Voltage Gain as a Function of Frequency



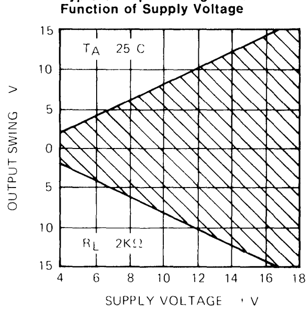
Open Loop Gain as a Function of Temperature



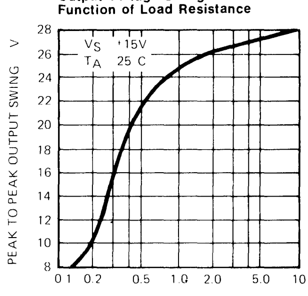
Power Consumption as a Function of Ambient Temperature



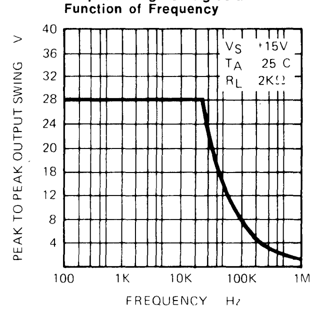
Typical Output Voltage as a Function of Supply Voltage



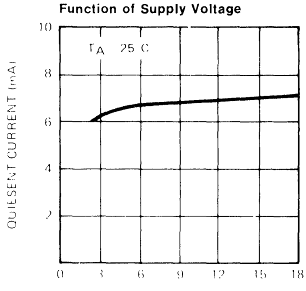
Output Voltage Swing as a Function of Load Resistance



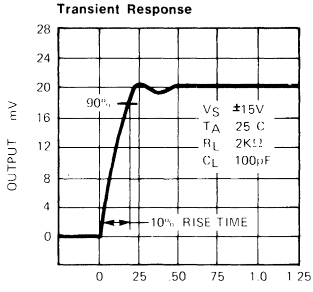
Output Voltage Swing as a Function of Frequency



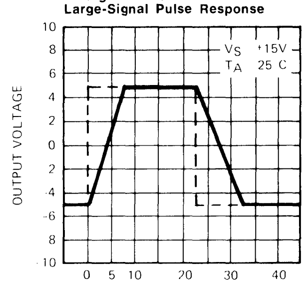
Quiesent Current as a Function of Supply Voltage



Transient Response

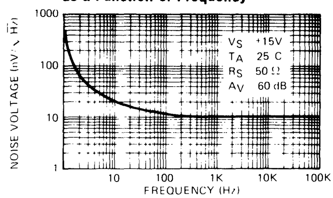


Voltage Follower Large-Signal Pulse Response

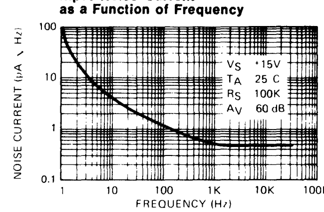


TYPICAL ELECTRICAL DATA

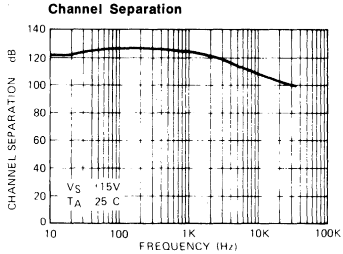
Input Noise Voltage as a Function of Frequency



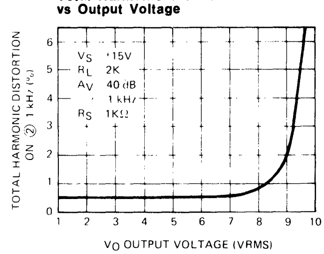
Input Noise Current as a Function of Frequency



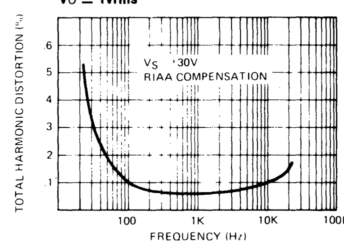
Channel Separation



Total Harmonic Distortion vs Output Voltage



Distortion vs Frequency
Vo = 1vrms



ELECTRICAL CHARACTERISTICS COMPARISON ($V_{CC} = \pm 15V$, $T_A = +25^oC$)

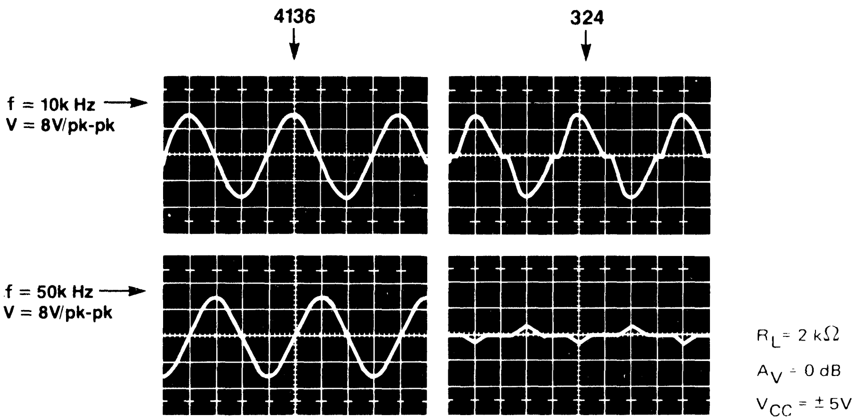
PARAMETER		RC4136 (typ)	RC741 (typ)	LM324 (typ)	UNIT
Input Offset Voltage		0.5	2.0	2	mV
Input Offset Current		5	10	5	nA
Input Bias Current		40	80	55	nA
Input Resistance		5	2		MΩ
Large-Signal Voltage Gain (R_L = 2 kΩ)		300,000	200,000	100,000	V/V
Output Voltage Swing (R_L = 2 kΩ)		±13V	±13V	$\lvert +V_{CC} - 1.2V \rvert$ to $-V_{CC}$	$\overline{V}$
Input Voltage Range		±14V	±13V	$\lvert +V_{CC} - 1.5V \rvert$ to $-V_{CC}$	$\overline{V}$
Common-Mode Rejection Ratio		100	90	85	dB
Supply Voltage Rejection Ratio		10	30	10	μV/V
Transient Response (gain = 1)	Risetime	0.13	0.3		μs
	Overshoot	5	5		%
Unity-Gain Bandwidth		3	0.8	0.8	MHz
Unity-Gain Slew Rate		1.0	0.5	0.5	V/μs
Input Noise Voltage (f_O = 1 kHz)		10	22.5		nV/√Hz
Output Short-Circuit Current		±45	±25		mA

RAYTHEON

4136 vs. 741

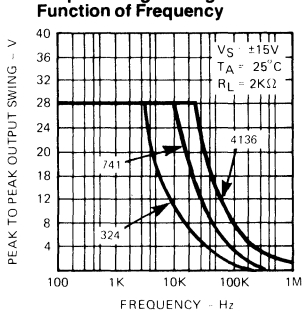
Although the 324 is an excellent device for single-supply applications where ground-sensing is important, it is a poor substitute for four 741's in split-supply circuits.

The simplified input circuit of the 4136 exhibits much lower noise than that of the 324 and exhibits no crossover distortion as compared with the 324 (see illustration). The 324 shows serious crossover distortion and pulse delay in attempting to handle a large-signal input pulse.

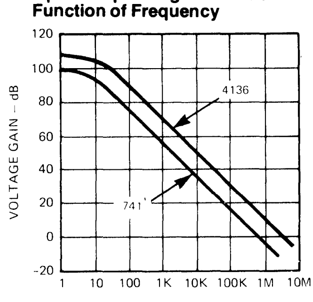


Comparative Cross-over Distortion

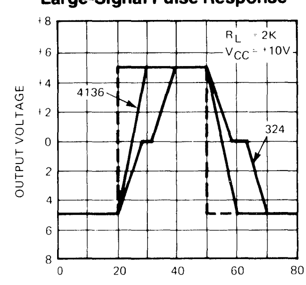
Output Voltage Swing as a Function of Frequency



Open Loop Voltage Gain as a Function of Frequency

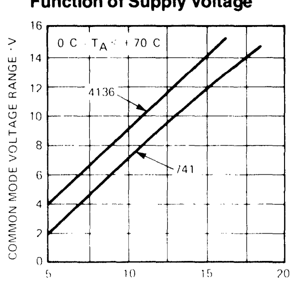


Voltage Follower Large-Signal Pulse Response

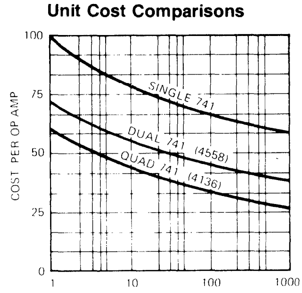


Typical Characteristics Curves Comparison

Input Common Mode Voltage Range as a Function of Supply Voltage

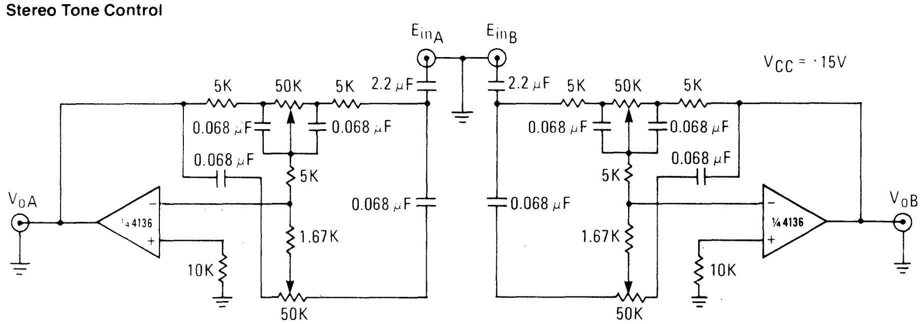


Unit Cost Comparisons

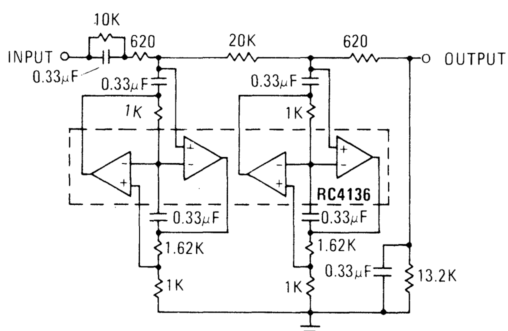


4136 TYPICAL APPLICATIONS

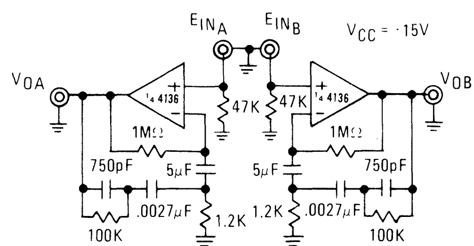
Stereo Tone Control



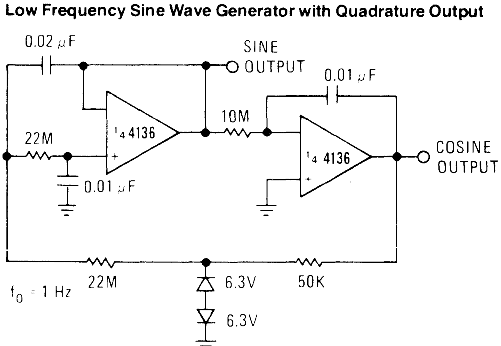
400 Hz Lowpass Butterworth Active Filter



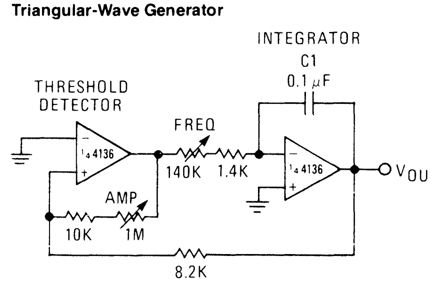
RIAA Preamplifier



Low Frequency Sine Wave Generator with Quadrature Output

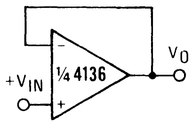


Triangular-Wave Generator

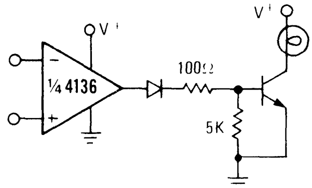


4136 TYPICAL APPLICATIONS

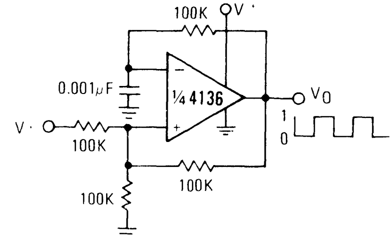
Voltage Follower



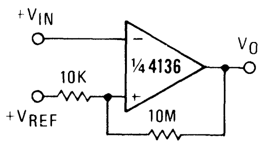
Lamp Driver



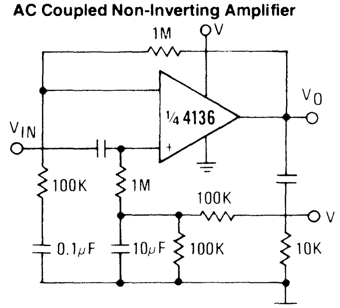
Squarewave Oscillator



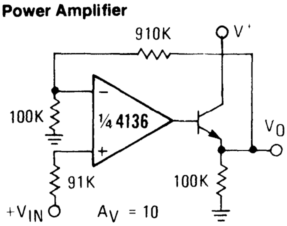
Comparator With Hysteresis



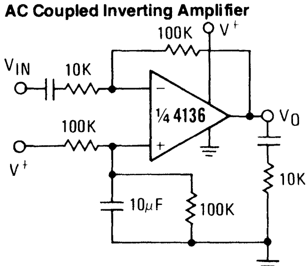
AC Coupled Non-Inverting Amplifier



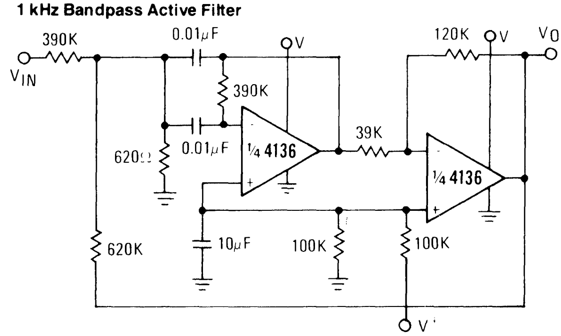
Power Amplifier



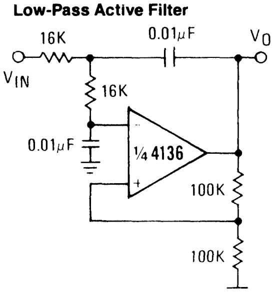
AC Coupled Inverting Amplifier



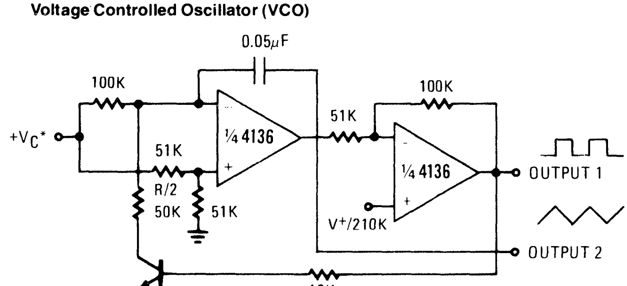
1 kHz Bandpass Active Filter



DC Coupled 1 kHz Low-Pass Active Filter



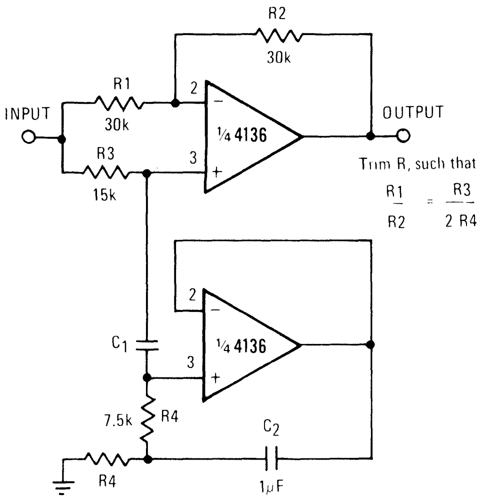
Voltage Controlled Oscillator (VCO)



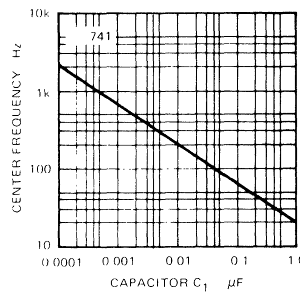
*Wide Control Voltage Range: 0 $V_{DC} < V_C < 2\ (V^+ - 1.5\ V_{DC})$

4136 TYPICAL APPLICATIONS

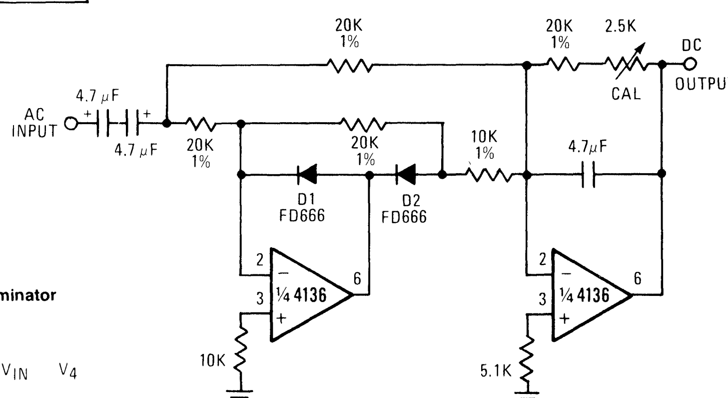
Notch Filter Using the 4136 as a Gyrator



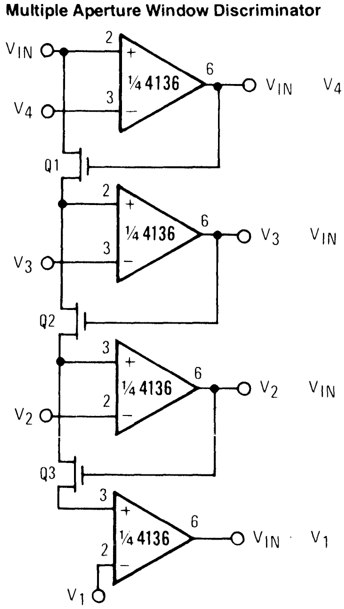
Notch Frequency as a Function of C_1



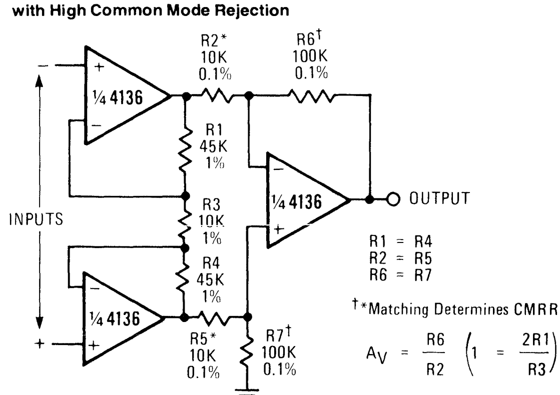
Full-Wave Rectifier and Averaging Filter



Multiple Aperture Window Discriminator



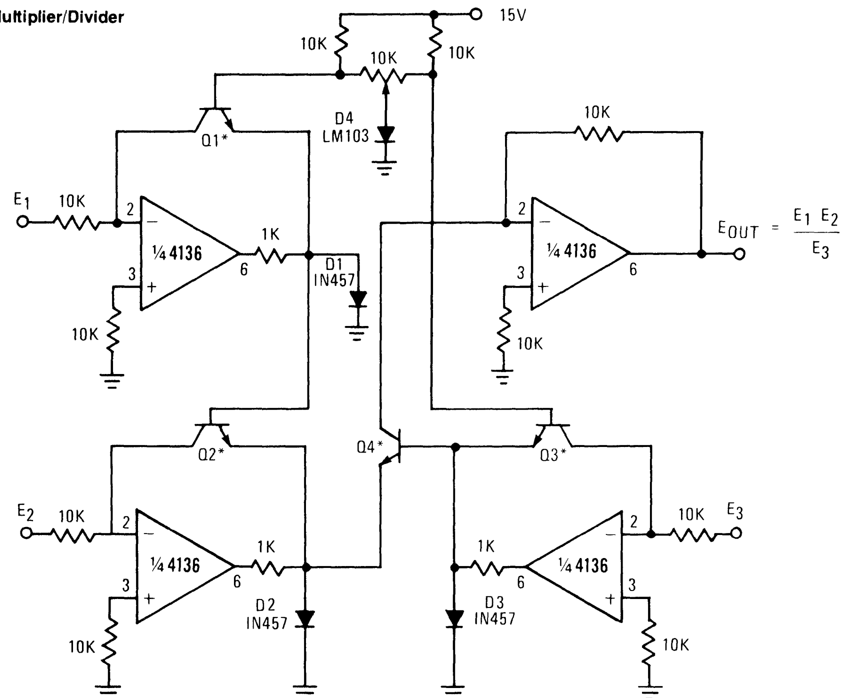
Differential Input Instrumentation Amplifier with High Common Mode Rejection



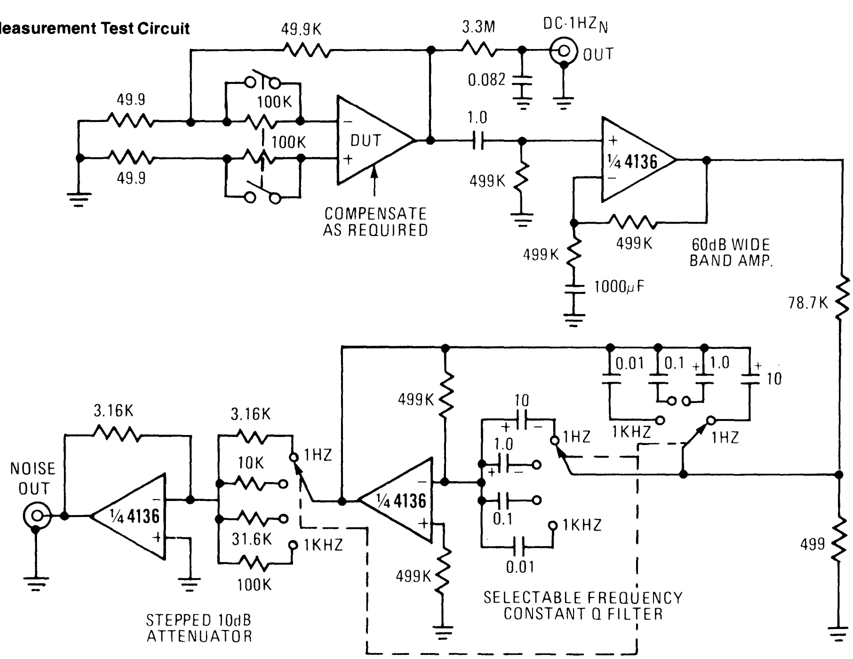
$$A_V = \frac{R6}{R2}\left(1 = \frac{2R1}{R3}\right)$$

4136 TYPICAL APPLICATIONS

Analog Multiplier/Divider



Noise Measurement Test Circuit



Quad High Performance Operational Amplifier

DESCRIPTION

The RM4156/RC4156 is a monolithic integrated circuit, consisting of four independent high performance operational amplifiers constructed with the planar epitaxial process.

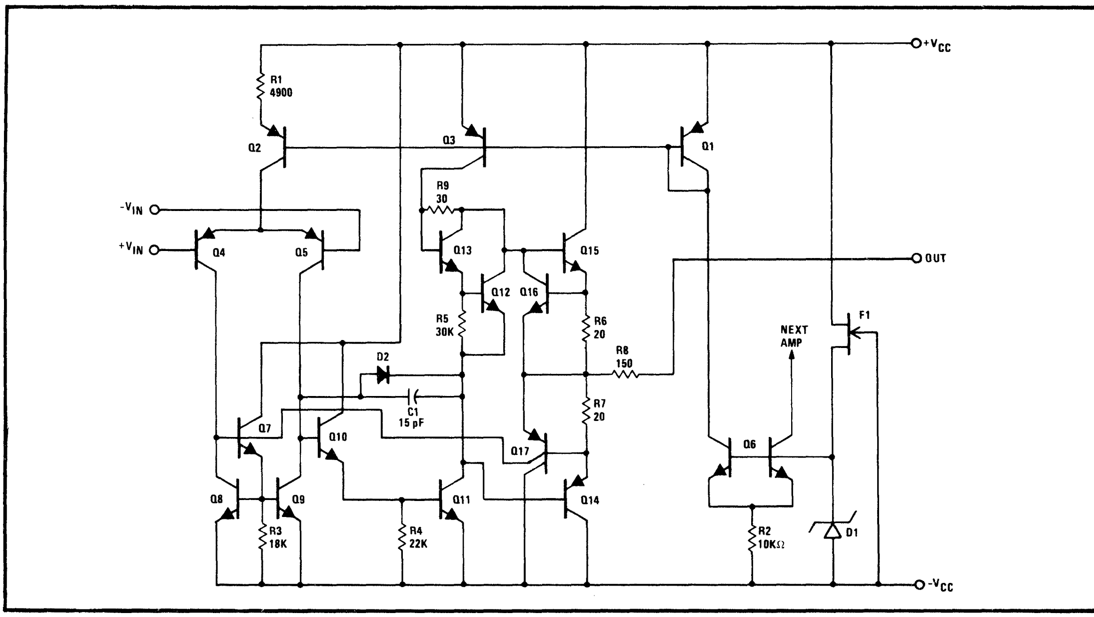
These amplifiers feature guaranteed A.C. performance which far exceeds that of the 741 type amplifiers. Also featured are excellent input characteristics and guaranteed low noise making this device the optimum choice for audio, active filter and instrumentation applications.

FEATURES

	Typical	Guaranteed
• Unity Gain Bandwidth	3.5 MHz	2.8 MHz
• High Slew Rate	1.6V/μS	1.3V/μS
• Low Noise Voltage	1.4μV	$2.0\mu V_{RMS}$

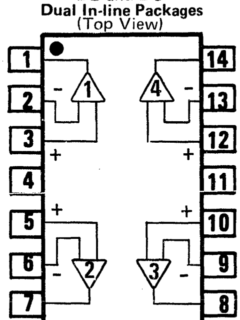
- Indefinite Short Circuit Protection
- No Crossover Distortion
- Low Input Offset and Bias Parameters
- Internal Compensation

SCHEMATIC DIAGRAM (1/4 Shown)



CONNECTION INFORMATION

DB and DC
Dual In-line Packages
(Top View)



PIN	FUNCTION
1	OUTPUT A
2	$-V_{IN}$ A
3	$+V_{IN}$ A
4	V+
5	$+V_{IN}$ B
6	$-V_{IN}$ B
7	OUTPUT B
8	OUTPUT C
9	$-V_{IN}$ C
10	$+V_{IN}$ C
11	V-
12	$+V_{IN}$ D
13	$-V_{IN}$ D
14	OUTPUT D

Order Part Nos.
RM4156DC, RV4156DB,
RV4156DC, RC4156DC,
RC4156DB

ABSOLUTE MAXIMUM RATINGS

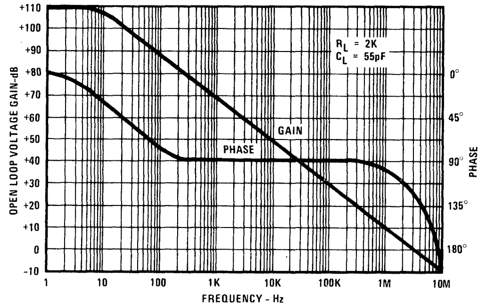
Supply Voltage	±20V	Storage Temperature Range		-65 to +150°C
Internal Power Dissipation (Note 1)	880 mW	Operating Temperature Range	RM4156	-55 to +125°C
Differential Input Voltage	±30V		RV4156	-40 to +85°C
Input Voltage (Note 2)	±15V		RC4156	0 to +70°C
Output Short Circuit Duration (Note 3)	Indefinite	Lead Soldering Temperature (60 sec)		300°C

ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

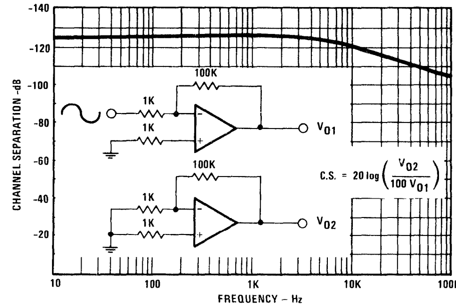
PARAMETER	CONDITIONS	RM4156 MIN	RM4156 TYP	RM4156 MAX	RV4156/RC4156 MIN	RV4156/RC4156 TYP	RV4156/RC4156 MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10\ K\Omega$		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geqslant 2\ K\Omega\ V_{OUT}\ \pm 10V$	50,000	100,000		25,000	100,000		V/V
Output Voltage Swing	$R_L \geqslant 10\ K\Omega$	±12	±14		±12	±14		V
	$R_L \geqslant 2\ K\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Output Resistance			230			230		Ω
Output Short Circuit Current			25			25		mA
Common Mode Rejection Ratio	$R_S \leqslant 10\ K\Omega$	80			80			dB
Power Supply Rejection Ratio	$R_S \leqslant 10\ K\Omega$	80			80			dB
Supply Current (all amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response								
Rise Time			50			75		ns
Overshoot			25%			25%		%
Slew Rate		1.3	1.6		1.3	1.6		V/μs
Unity Gain Bandwidth		2.8	3.5		2.8	3.5		MHz
Phase Margin	$R_L = 2\ K\Omega\ R_C = 50\ pF$		50			50		degrees
Full Power Bandwidth	$V_O = 20V$ p-p	20	25		20	25		kHz
Input Noise Voltage	f = 20 Hz to 20 kHz		1.4	2.0		1.4	2.0	μV RMS
Input Noise Current	f = 20 Hz to 20 kHz		15			15		pA RMS
Channel Separation			-108			-108		dB
The following specifications apply for -55°C ≤ T_A ≤ +125°C for RM4156, -40°C ≤ T_A ≤ +85°C for RV4156, 0°C ≤ T_A ≤ +70°C for RC4156.								
Input Offset Voltage	$R_S \leqslant 10\ K\Omega$			5.0			6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain	$R_L \geqslant 2\ K\Omega\ V_{OUT}\ \pm 10V$	25,000			15,000			V/V
Output Voltage Swing	$R_L \geqslant 2\ K\Omega$	±10			±10			V
Supply Current			10			10		mA
Average Offset Voltage Drift			5			5		μV/°C

Notes:
1. Rating applies for case temperature of +25°C maximum; derate linearity at 6.4 mW/°C for temperatures above +25°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

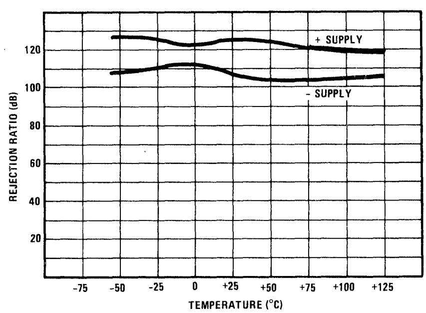
TYPICAL PERFORMANCE DATA



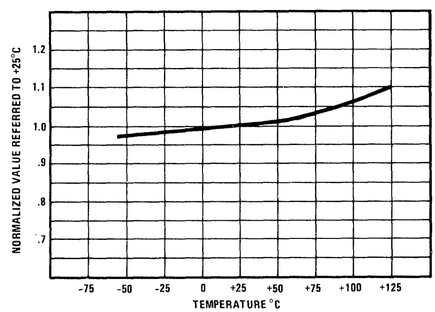
Open Loop Frequency Response



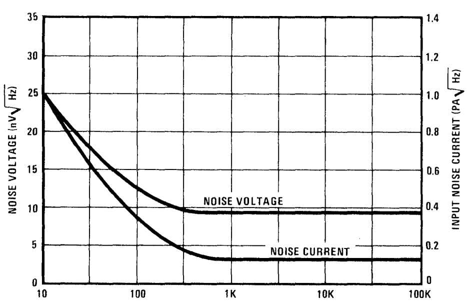
Channel Separation vs. Frequency



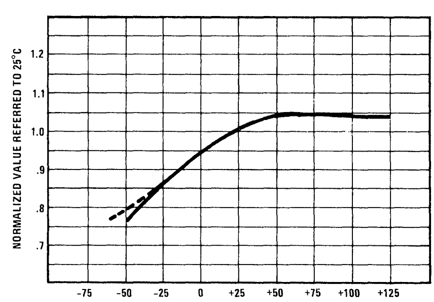
Power Supply Rejection Ratio vs. Temperature



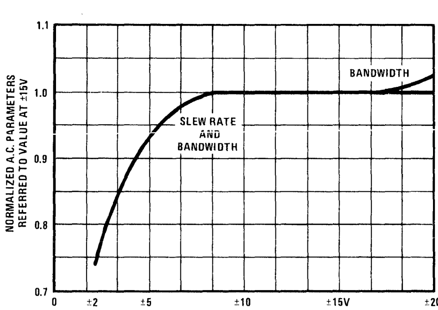
Transient Response vs. Temperature



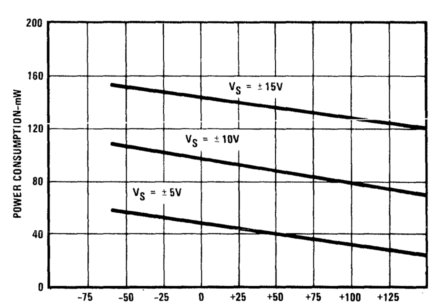
Input Noise vs. Frequency



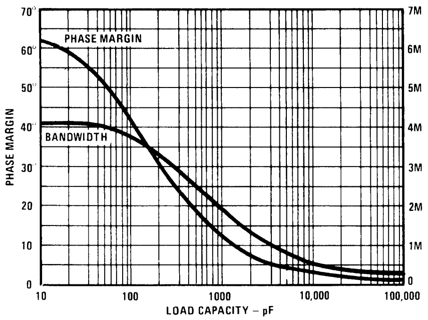
Normalized AC Parameters vs. Temperature



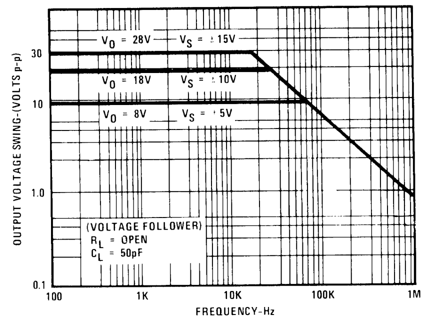
Slew Rate vs. Supply Voltage



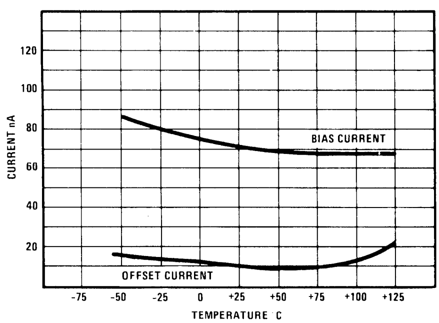
Power Consumption vs. Temperature



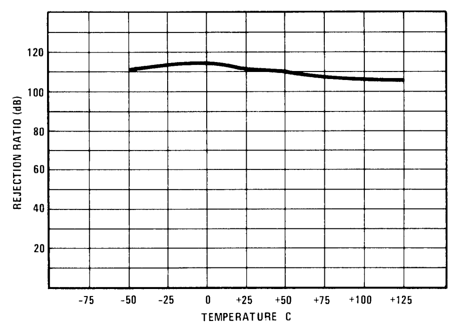
Small Signal Bandwidth and Phase Margin vs. Load Capacitance



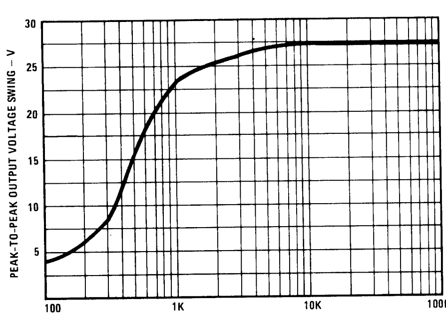
Output Voltage Swing vs. Frequency



Input Currents vs. Temperature



Common Mode Rejection Ratio vs. Temperature



Output Voltage Swing vs. Load Resistance

AVAILABLE TYPES

Part Number	Package	Operating Temperature
RM4156DC	Ceramic	-55 to +125°C
RV4156DB	Plastic	-40 to +85°C
RV4156DC	Ceramic	-40 to +85°C
RC4156DC	Ceramic	0 to +70°C
RC4156DB	Plastic	0 to +70°C

HIGH RELIABILITY OPTIONS

Part Type	Added Screening	Order Part No.
RM4156DC	With MIL-STD-883 Class B processing	RM4156DC3
RV4156DC RC4156DC	With A+3 processing* including burn-in and tightened AQL	RV4156DC3 RC4156DC3
RV4156DB RC4156DB	With A+2 processing* including "Hot Rail" testing, burn-in, temp cycle and tightened AQL	RV4156DB2 RC4156DB2
	With A+1 processing* including "Hot Rail" testing, temp cycle and tightened AQL	RV4156DB1 RC4156DB1

* Full description contained in the A+ bulletin available at your local Raytheon Sales Office.

APPLICATIONS

The 4156 Quad Operational Amplifier can be used in almost any 741 application and will provide superior performance. The higher unity-gain bandwidth and slew rate make it ideal for applications requiring good frequency response, such as. active filter circuits, oscillators and audio amplifiers.

The following applications have been selected to illustrate the advantages of using the Raytheon 4156 Quad Operational Amplifier.

VERSATILE TRIANGLE-AND-SQUARE WAVE GENERATOR

This circuit generates a precise triangle-wave with independently adjustable frequency, offset, and amplitude. A square-wave is also available from a separate output. The circuit exhibits excellent stability in both amplitude and frequency when using the 4156 quad op amp. See Figure 1.

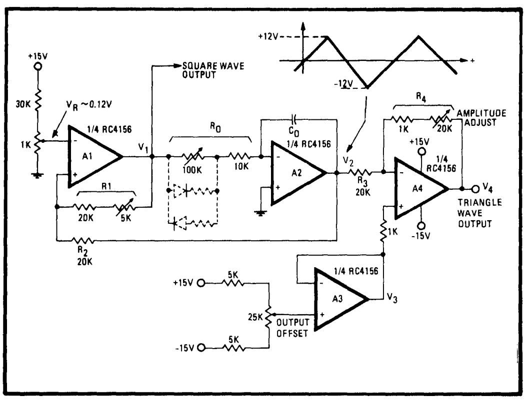


Figure 1. Triangle-and-Square Wave Generator

Amplifier A1 acts as a comparator and will swing between the positive and negative limits, typically +14V and -13.5V. The square-wave from amplifier A1 is converted to a triangle-wave by amplifier A2. Amplitude of V_2 is adjusted by varying R_1. For best operation, it is recommended that R_1 and V_R be set to obtain a triangle-wave at V_2 with ±12V amplitude. This will then allow A3 and A4 to be used for independent adjustment of output-offset and amplitude over a wide range.

The output frequency can be easily calculated. The switching transitions occur at:

$$\frac{R_1}{R_1 + R_2} V_2 + \frac{R_2}{R_1 + R_2} V_{1H} = V_R$$

and

$$\frac{R_1}{R_1 + R_2} V_2 + \frac{R_2}{R_1 + R_2} V_{1L} = V_R$$

where V_{1H} is the positive saturation level and V_{1L} is the negative saturation level. For a ±12V triangle-wave at output of A2, V_R will need to be approximately 0.12V and R_2/R_1 = 1.87.

Amplifiers A3 and A4 are used to independently adjust output offset and amplitude. The output V_4 will be:

$$V_4 = -\frac{R_4}{R_3} V_2 + V_3$$

An asymmetric triangle-wave is needed in some applications. Adding diodes as shown by the dashed lines is a way to vary the positive and negative slopes independently.

Frequency range can be very wide and the circuit will function very well up to about 10 kHz. Transition time for the square-wave at V_1 is less than 21 μsec when using the 4156.

ACTIVE FILTERS

The introduction of low-cost quad op amps has had a strong impact on active filter design. The complex multiple-feedback, single-op-amp filter circuits have been rendered obsolete for most applications. *State-variable* active-filter circuits using three to four op amps per section offer many advantages over the single-op-amp circuits. They are relatively insensitive to the passive-component tolerances and variations. The Q, gain, and natural frequency can be independently adjusted. Hybrid construction is very practical because resistor and capacitor values are relatively low and the filter parameters are determined by resistance ratios rather than by single resistors. A generalized circuit diagram of the 2-pole state-variable active filter is shown in Figure 2. The particular input connections and component-values can be calculated for specific applications. An important feature of the state-variable filter is that it can be inverting or noninverting and can simultaneously provide three outputs: lowpass, bandpass, and highpass. A notch filter can be realized by adding one summing op amp.

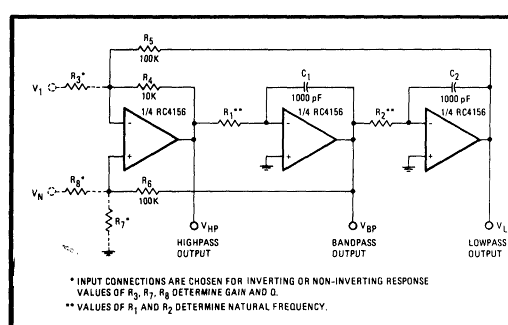


Figure 2. Generalized State-Variable Configuration for Active Filter

The Raytheon 4156 was designed and characterized for use in active filter circuits. Frequency response is fully specified with minimum values for unity-gain bandwidth, slew-rate, and full-power response. Maximum noise is specified. Output swing is excellent with no distortion or clipping. The Raytheon 4156 provides full, undistorted response up to 20 kHz and is ideal for use in high-performance audio and telecommunication equipment.

In the state-variable filter circuit, one amplifier performs a summing function and the other two act as integrators. The choice of passive component values is arbitrary, but must be consistent with the amplifier operating range and input signal characteristics. The values shown for C1, C2, R4, R5 and R6 are arbitrary. Pre-selecting their values will simplify the filter tuning procedures, but other values can be used if necessary.

The generalized transfer function for the state-variable active filter is:

$$T(s) = \frac{a_2 s^2 + a_1 s + a_0}{s^2 + b_1 s + b_0}$$

Filter response is conventionally described in terms of a natural frequency ω_0 in radians/sec, and Q, the quality of the complex pole pair. The filter parameters ω_0 and Q relate to the coefficients in T(s) as:

$$\omega_0 = \sqrt{b_0} \quad \text{and} \quad Q = \frac{\omega_0}{b_1}$$

The input configuration determines the polarity (inverting or noninverting), and the output selection determines the type of filter response (lowpass, bandpass, or highpass).

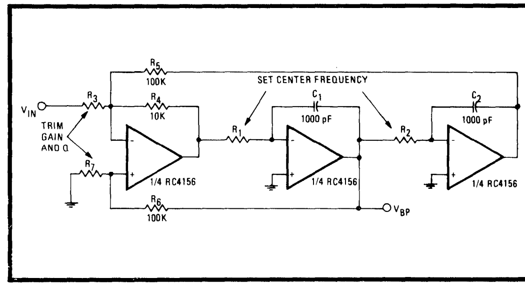


Figure 3. Bandpass Active Filter

Notch and all-pass configurations can be implemented by adding another summing amplifier.

Bandpass filters are of particular importance in audio and telecommunication equipment. A design approach to bandpass filters will be shown as an example of the state-variable configuration.

DESIGN EXAMPLE – BANDPASS FILTER

In this example, the input signal is applied through R_3 to the inverting input of the summing amplifier and the output is taken from the first integrator (V_{BP}). The summing amplifier will maintain equal voltage at the inverting and noninverting inputs, (see equation below).

$$\frac{\dfrac{R_3R_5}{R_3+R_5}}{R_4+\dfrac{R_3R_5}{R_3+R_5}} V_{HP}(s) + \frac{\dfrac{R_3R_4}{R_3+R_4}}{R_5+\dfrac{R_3R_4}{R_3+R_4}} V_{LP}(s) + \frac{\dfrac{R_4R_5}{R_4+R_5}}{R_3+\dfrac{R_4R_5}{R_4+R_5}} V_{in}(s) = \frac{R_7}{R_6+R_7} V_{BP}(s)$$

These equations can be combined to obtain the transfer function:

$$V_{BP}(s) = -\frac{1}{R_1C_1S} V_{HP}(s) \quad \text{and} \quad V_{LP}(s) = -\frac{1}{R_2C_2S} V_{BP}(s)$$

$$\frac{V_{BP}(s)}{V_{in}(s)} = \frac{\dfrac{R_4}{R_3}\dfrac{1}{R_1C_1}s}{s^2 + \dfrac{R_7}{R_6+R_7}\left(1+\dfrac{R_4}{R_5}+\dfrac{R_4}{R_3}\right)\left(\dfrac{1}{R_1C_1}\right)s + \dfrac{R_4}{R_5}\dfrac{1}{R_1C_1R_2C_2}}$$

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Defining $1/R_1C_1$ as ω_1, $1/R_2C_2$ as ω_2, and substituting in the assigned values for R_4, R_5, and R_6, then the transfer function simplifies to:

$$\frac{V_{BP}(s)}{V_{in}(s)} = \frac{\frac{10^4}{R_3}\,\omega_1 s}{s^2 + \left[\frac{1.1 + \frac{10^4}{R_3}}{1 + \frac{10^5}{R_7}}\right]\omega_1 s + \frac{0.1}{\omega_1\omega_2}}$$

This is now in a convenient form to look at the center-frequency ω_0 and filter Q.

$$\omega_0 = \sqrt{0.1\,\omega_1\omega_2} = 10^{-9}\sqrt{0.1\,R_1R_2} \quad \text{and} \quad Q = \left[\frac{1 + \frac{10^5}{R_7}}{1.1 + \frac{10^4}{R_3}}\right]\omega_0$$

The frequency response for various values of Q are shown in Figure 4.

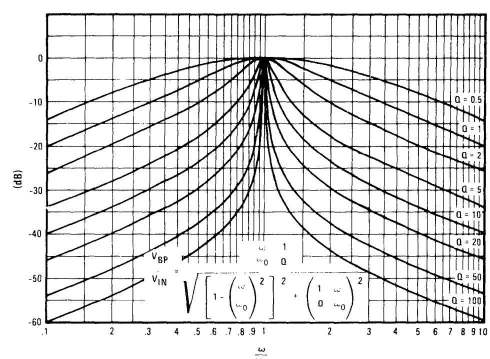


Figure 4. Bandpass Transfer Characteristics Normalized for Unity Gain and Frequency

These equations suggest a tuning sequence where ω_0 is first trimmed via R_1 or R_2, then Q is trimmed by varying R_7 and/or R_3. An important advantage of the state-variable bandpass filter is that Q can be varied without affecting center frequency ω_0.

This analysis has assumed ideal op amps operating within their linear range, which is a valid design approach for a reasonable range of ω_0 and Q. At extremes of ω_0 and at high values of Q, the op amp parameters become significant. A rigorous analysis is very complex, but some factors are particularly important in designing active filters:

1. The passive component values should be chosen such that all op amps are operating within their linear region for the anticipated range of input signals. Slew rate, output current rating, and common-mode input range must be considered. For the integrators, the current through the feedback capacitor (I = C dV/dt) should be included in the output current computations.

2. From the equation for Q, it would seem that infinite Q could be obtained by making R_7 zero. But as R_7 is made small, the Q becomes limited by the op amp gain at the frequency of interest. The effective closed-loop gain is being increased directly as R_7 is made smaller, and the ratio of open-loop gain to closed-loop gain is becoming less. The gain and phase error of the filter at high Q is very dependent on the op-amp open-loop gain at ω_0.

3. The attenuation at extremes of frequency is limited by the op amp gain and unity-gain bandwidth. For integrators, the finite open-loop op-amp gain limits the accuracy at the low-end. The open-loop roll-off of gain limits the filter attenuation at high frequency.

The Raytheon 4156 Quad Operational Amplifier has much better frequency response than a conventional 741 circuit and is ideal for active filter use. Natural frequencies of up to 10 kHz are readily achieved and up to 20 kHz is practical for some configurations. Q can range up to 50 with very good accuracy and up to 500 with reasonable response. The extra gain of the 4156 at high frequencies gives the Raytheon quad op amp an extra margin of performance in active-filter circuits.

Quad High Speed Decompensated Operational Amplifier

DESCRIPTION

The RM4157/RC4157 is a monolithic integrated circuit, consisting of four independent high performance operational amplifiers constructed with the planar epitaxial process.

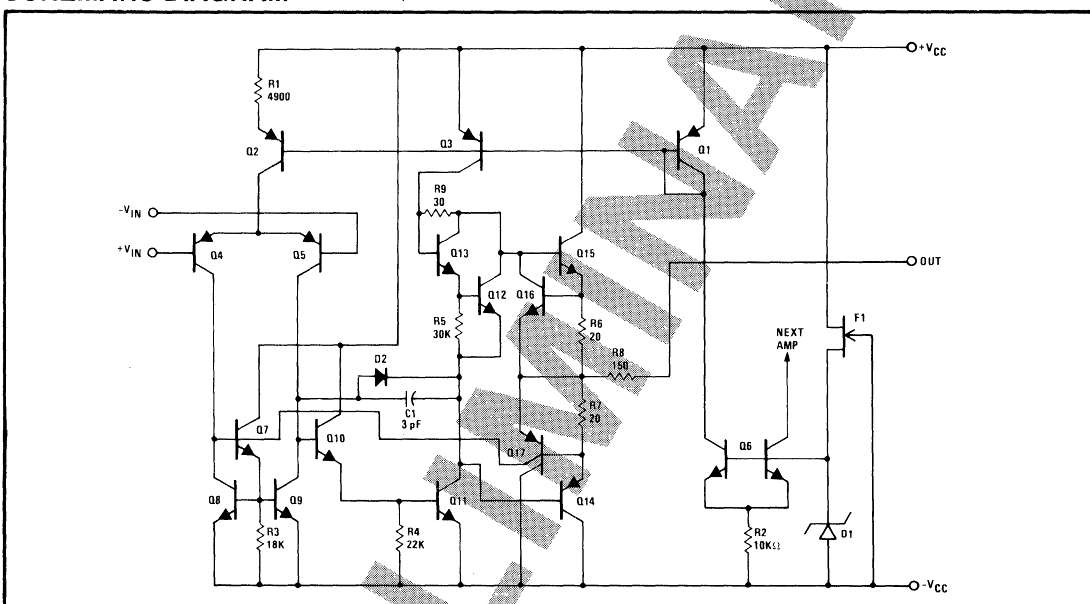
These amplifiers feature guaranteed A.C. performance which far exceeds that of the LM149 type amplifiers. Also featured are excellent input characteristics and guaranteed low noise making this device the optimum choice for audio, active filter and instrumentation applications.

FEATURES

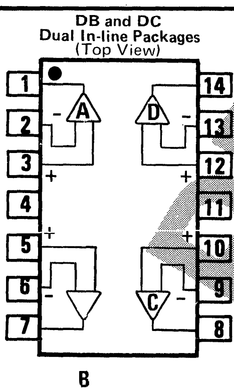
	Typical	Guaranteed
• Gain Bandwidth Product ($A_V \geq 5$)	19 MHz	15 MHz
• High Slew Rate (A_V=5)	8	6.5V/μs
• Low Noise Voltage	1.4μV	2.0μV RMS

- Indefinite Short Circuit Protection
- No Crossover Distortion
- Low Input Offset and Bias Parameters
- Internal Compensation

SCHEMATIC DIAGRAM (1/4 Shown)

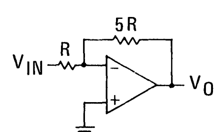


CONNECTION INFORMATION

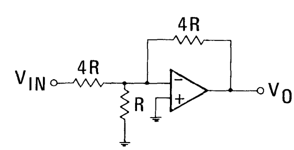


PIN	FUNCTION
1	OUTPUT A
2	$-V_{IN}$ A
3	$+V_{IN}$ A
4	V+
5	$+V_{IN}$ B
6	$-V_{IN}$ B
7	OUTPUT B
8	OUTPUT C
9	$-V_{IN}$ C
10	$+V_{IN}$ C
11	V-
12	$+V_{IN}$ D
13	$-V_{IN}$ D
14	OUTPUT D

Minimum Gain Configurations



Minimum Gain for Stable Operation



Unity Gain Inverter

The 4157 is an uncompensated version of the 4156. The characteristics are the same except the 4157 has wider bandwidths. As a result the part requires a minimum gain of 5.

Order Part Nos.:
RM4157DC, RV4157DB, RV4157DC, RC4157DC, RC4157DB

Quad High Speed Decompensated Operational Amplifier 4157

ABSOLUTE MAXIMUM RATINGS

Quad Wide Band Decompensated (Av_{min} = 5) Operational Amplifier

Supply Voltage	±20V
Internal Power Dissipation (Note 1)	880 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite

Storage Temperature Range		-65 to +150°C
Operating Temperature Range	RM4157	-55 to +125°C
	RV4157	-40 to +85°C
	RC4157	0 to +70°C
Lead Soldering Temperature (60 sec)		300°C

ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	RM4157 MIN	RM4157 TYP	RM4157 MAX	RV4157/RC4157 MIN	RV4157/RC4157 TYP	RV4157/RC4157 MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ K\Omega$		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2\ K\Omega\ V_{OUT}$ ±10V	50,000	100,000		25,000	100,000		V/V
Output Voltage Swing	$R_L \geq 10\ K\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ K\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Output Resistance			230			230		Ω
Output Short Circuit Current			25			25		mA
Common Mode Rejection Ratio	$R_S \leq 10\ K\Omega$	80			80			dB
Power Supply Rejection Ratio	$R_S \leq 10\ K\Omega$	80			80			dB
Supply Current (all amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response								
Rise Time	$A_V = 5$		50			60		ns
Overshoot	$A_V = 5$		25%			25%		%
Slew Rate	$A_V = 5$	6.5	8		6.5	8		V/μs
Gain Bandwidth Product		15	19		15	19		MHz
Phase Margin ($A_V = 5$)	$R_L = 2\ K\Omega\ R_C = 50\ pF$		50			50		degrees
Full Power Bandwidth	V_O = 20V p-p	100	125		100	125		kHz
Input Noise Voltage	f = 20 Hz to 20 kHz		1.4	2.0		1.4	2.0	μV RMS
Input Noise Current	f = 20 Hz to 20 kHz		15			15		pA RMS
Channel Separation			-108			-108		dB
The following specifications apply for -55°C ≤ T_A ≤ +125°C for RM4157, -40°C ≤ T_A ≤ +85°C for RV4157, 0°C ≤ T_A ≤ +70°C for RC4157.								
Input Offset Voltage	$R_S \leq 10\ K\Omega$			5.0			6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain	$R_L \geq 2\ K\Omega\ V_{OUT}$ ±10V	25,000			15,000			V/V
Output Voltage Swing	$R_L \geq 2\ K\Omega$	±10			±10			V
Supply Current			10			10		mA
Average Offset Voltage Drift			5			5		μV/°C

Notes:
1. Rating applies for case temperature of +25°C maximum; derate linearity at 6.4 mW/°C for temperatures above +25°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

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GENERAL DESCRIPTION

The RM4531 and RC4531 are high slew rate operational amplifiers intended for applications requiring slew rates up to 30V/μs while keeping the DC performance of the 741.

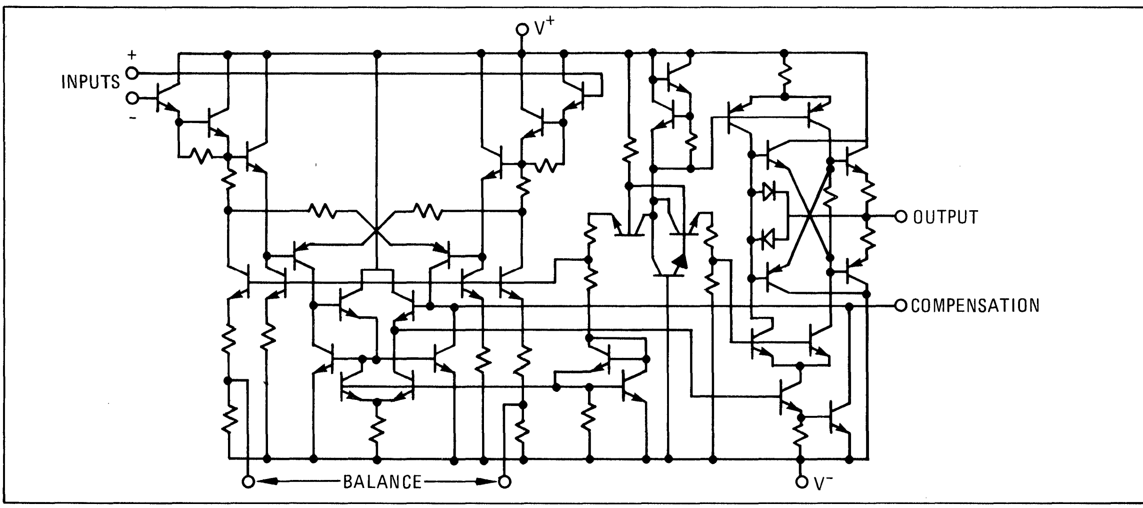
The RM4531 military version operates over a temperature range from −55°C to +125°C. The RC4531 operates from 0°C to +70°C.

High slew rates are achieved through use of an improved input stage which tends to retain small signal characteristics when subjected to large differential input signals. Advanced integrated circuit layout techniques are used to eliminate thermal feedback. The RM4531 and RC4531 feature offset null capability, high gain, and each can be compensated with an external 100pF capacitor connected between the output and compensation terminals.

DESIGN FEATURES

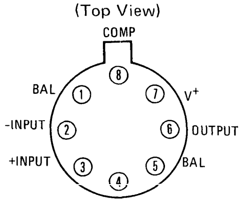
- Slew Rate 35V/μs
- Small Signal Bandwidth 1MHz
- Large Signal Bandwidth 500kHz
- Supply Voltage ±6V to ±18V
- Pin-for-Pin Replacement for 709, LM101A, 741
- Low Drift Offset-Null Circuitry
- Compensated with Single Capacitor

SCHEMATIC DIAGRAM



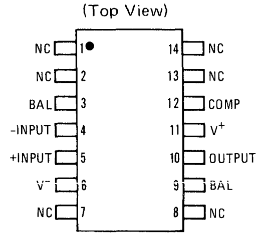
CONNECTION INFORMATION

TE (TO-99)
Metal Can Package
(Top View)



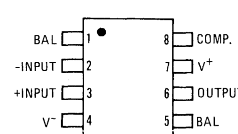
Order Part Nos.:
RM4531T, RC4531T

DC
Dual In-line Package
(Top View)



Order Part Nos.:
RM4531DC, RC4531DC

NB Dual In-line
Plastic Package
(Top View)



Order Part No.:
RC4531NB

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	RM4531: ±22V RC4531: ±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±15V
Input Voltage (Note 2)	−12.5V, +15V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
RM4531	−55°C to +125°C
RC4531	0°C to +70°C
Lead Temperature (Soldering, 60s)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM4531 MIN	RM4531 TYP	RM4531 MAX	RC4531 MIN	RC4531 TYP	RC4531 MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10k\Omega$		2.0	5.0		2.0	6.0	mV
Input Offset Current			30	200		50	200	nA
Input Bias Current			300	500		400	1500	nA
Input Resistance		0.3	20		0.3	20		MΩ
Large-Signal Voltage Gain	$R_S \geqslant 2k\Omega$, V_{out} = ±10V	50,000	100,000		20,000	60,000		V/V
Input Votlage Range (Note 2)		±10			±10			V
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	70	100		70	100		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$		10	150		10	150	μV/V
Output Resistance			75			75		Ω
Supply Current			5.5	7.0		5.5	10	mA
Power Consumption			165	210		165	300	mW
Setting Time, 1%	A_V = +1, V_{IN} = ±10V		1.5			1.5		μs
Setting Time, .01%	A_V = +1, V_{IN} = ±10V		2.5			2.5		μs
Large Signal Overshoot	A_V = +1, V_{IN} = ±10V		2.0			2.0		%
Small Signal Risetime	A_V = +1, V_{IN} = 400mV		300			300		ns
Small Signal Overshoot	A_V = +1, V_{IN} = 400mV		5.0			5.0		%
Slew Rate	A_V = 100		35			35		V/μs
	A_V = 10		35			35		V/μs
	A_V = 1 (non-inv.)		30			30		V/μs
	A_V = 1 (inv.)		35			35		V/μs
The following specifications apply for −55°C ⩽ T_A ⩽ +125°C for RM4531; 0°C ⩽ T_A ⩽ +70°C for RC4531.								
Input Offset Voltage	$R_S \leqslant 10k\Omega$			6.0			7.5	mV
Input Offset Current	$T_A = T_{min}$			500			300	nA
	$T_A = T_{max}$			200			200	nA
Input Bias Current	$T_A = T_{min}$			1.5			2.0	μA
	$T_A = T_{max}$			0.5			1.5	μA
Large-Signal Voltage Gain	$R_L \geqslant 2k\Omega$, V_{out} = ±10V	25,000			15,000			
Output Voltage Swing	$R_L \geqslant 2k\Omega$	±10	±13		±10	±13		V
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	70	90					dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$		10	150				μV/V
Supply Current	$T_A = T_{max}$		4.5	5.5		4.5	5.5	mA

NOTES:
1. Rating applies for case temperatures to +125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C for RM4531.
2. For supply voltages less than ±15V, the absolute maximum positive input voltage is equal to the supply votlage. The absolute maximum negative input voltage decreased by 1 volt for every 1 volt decrease in the negative supply voltage.
3. Short-circuit may be to ground or to either supply Rating applies to +125°C case temperature or +75°C ambient temperature for RM4531.

GENERAL DESCRIPTION

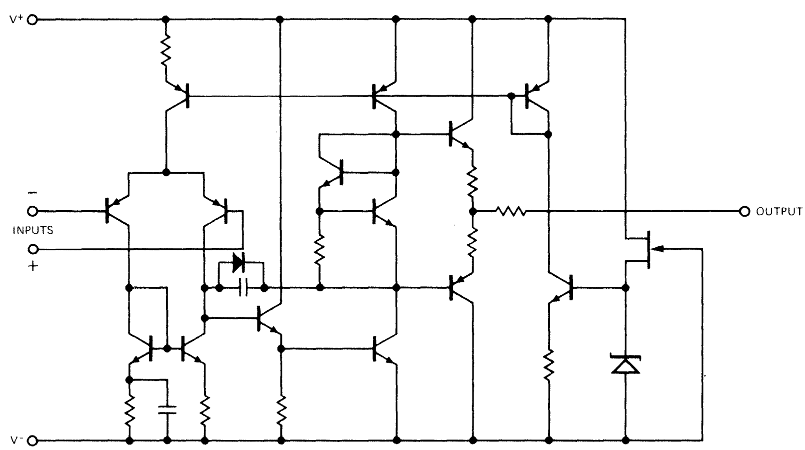
The 4558 integrated circuit is a dual high gain operational amplifier internally compensated and constructed on a single silicon chip using the planar epitaxial process.

Combining the features of the 741 with the close parameter matching and tracking of a dual device on a monolithic chip results in unique performance characteristics. Excellent channel separation allows the use of the dual device in single 741 operational amplifier applications providing the highest possible packaging density. It is especially well suited for applications in differential-in, differential-out as well as in potentiometric amplifiers and where gain and phase matched channels are mandatory.

DESIGN FEATURES

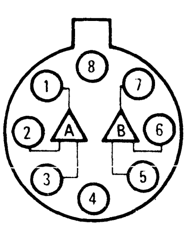
- 2.5 MHz Unity Gain Bandwidth Guaranteed
- Supply Voltage ±22V for RM4558 and ±15V for RC4558
- Short-Circuit Protection
- No Frequency Compensation Required
- No Latch-Up
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- Parameter Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers

SCHEMATIC DIAGRAM (1/2 Shown)



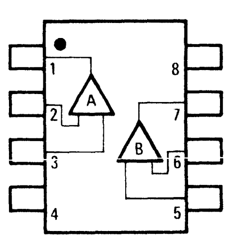
CONNECTION INFORMATION

TE (TO-99)
Metal Can Package
(Top View)



Order Part Nos.:
RC4558T, RM4558T

DE and NB
Dual In-line Packages
(Top View)



Order Part Nos.:
RC4558NB, RV4558NB
RC4558DE, RV4558DE
RM4558DE

PIN	FUNCTION
1	A OUTPUT
2	A -INPUT
3	A +INPUT
4	V^-
5	B +INPUT
6	B -INPUT
7	B OUTPUT
8	V^+

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	RM4558: ±22V
	RC4558: ±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	RM4558: −55°C to +125°C
	RV4558: −40°C to +85°C
	RC4558: 0°C to +70°C
Lead Temperature (Soldering, 60s)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM4558 MIN	RM4558 TYP	RM4558 MAX	RV/RC4558 MIN	RV/RC4558 TYP	RV/RC4558 MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5.0	200		30	200	nA
Input Bias Current			40	500		200	500	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geqslant 2k\Omega$, V_{out} = ±10V	50,000	300,000		20,000	300,000		
Output Voltage Swing	$R_L \geqslant 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geqslant 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	70	100		70	100		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$		10	150		10	150	μV/V
Power Consumption (All Amplifiers)	$R_L = \infty$		100	170		100	170	mW
Transient Response (unity gain)	V_{IN} = 20mV, R_L = 2kΩ, $C_L \leqslant 100pF$							
Risetime			0.3			0.3		μs
Overshoot			15.0			15.0		%
Slew Rate (unity gain)	$R_L \geqslant 2k\Omega$		0.5			0.5		V/μs
Channel Separation (Gain = 100)	f = 10kHz, R_S = 1kΩ		90			90		dB
Unity Gain Bandwidth (Gain = 1)		2.5	3.0		2.0	3.0		MHz
The following specifications apply for −55°C ⩽ T_A ⩽ +125°C for RM4558; 0°C ⩽ T_A ⩽ +70°C for RC4558; −40°C ⩽ T_A ⩽ +85°C for RV4558								
Input Offset Voltage	$R_S \leqslant 10k\Omega$			6.0			7.5	mV
Input Offset Current				500			300/500*	nA
Input Bias Current				1500			800/1500	nA
Large-Signal Voltage Gain	$R_L \geqslant 2k\Omega$, V_{out} = ±10V	25,000			15,000			
Output Voltage Swing	$R_L \geqslant 2k\Omega$	±10			±10			V
Power Consumption	V_S = ±15V							
	T_A = +125°C		90	150		90	150	mW
	T_A = −55°C		120	200		120	200	mW

*RV4558

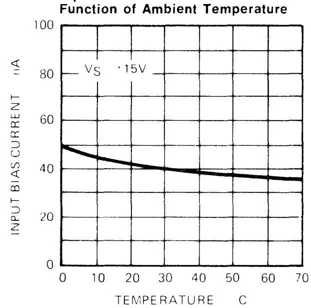
MATCHING CHARACTERISTICS (V_{CC} = ±15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM4558 TYP	RC4558 TYP	UNITS
Voltage Gain	$R_L \geqslant 2k\Omega$	±.5	±1.0	dB
Input Bias Current		±15	±15	nA
Input Offset Current		±7.5	±7.5	nA
Input Offset Voltage	$R_S \geqslant 10k\Omega$	±.1	±.2	mV

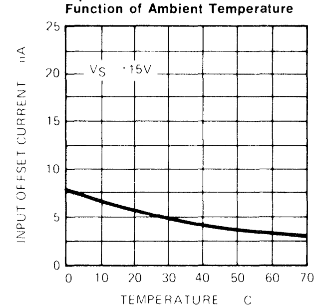
NOTE 1: Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C for RM4558.
NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 3: Short circuit may be to ground on one amp only. Rating applies to +125°C case temperature or +75°C ambient temperature for RC4558 and to +85°C ambient temperature for RV4558.

TYPICAL ELECTRICAL DATA

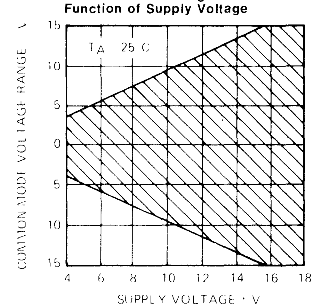
Input Bias Current as a Function of Ambient Temperature



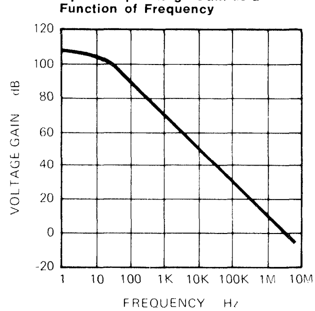
Input Offset Current as a Function of Ambient Temperature



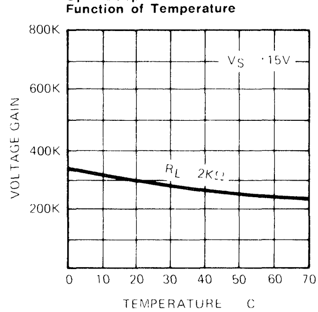
Common Mode Range as a Function of Supply Voltage



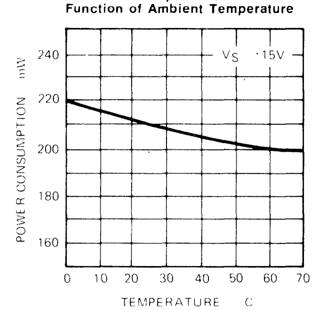
Open Loop Voltage Gain as a Function of Frequency



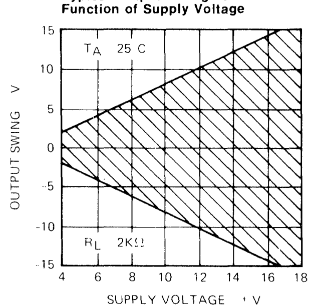
Open Loop Gain as a Function of Temperature



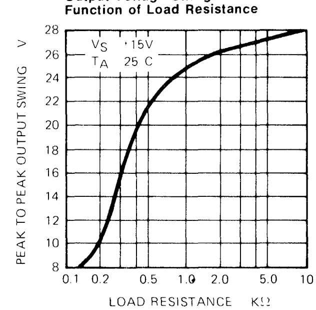
Power Consumption as a Function of Ambient Temperature



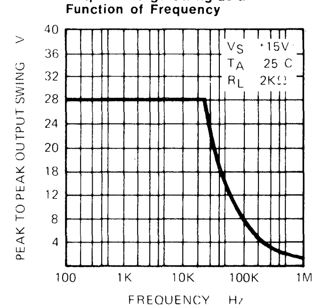
Typical Output Voltage as a Function of Supply Voltage



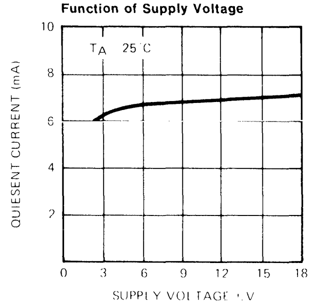
Output Voltage Swing as a Function of Load Resistance



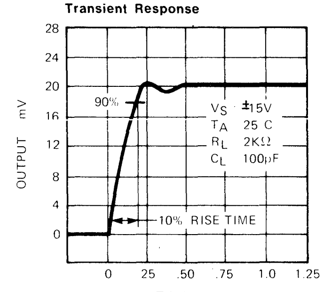
Output Voltage Swing as a Function of Frequency



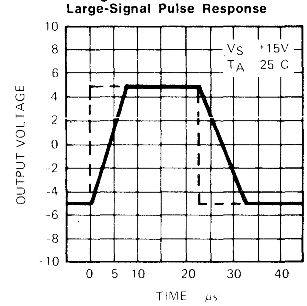
Quiesent Current as a Function of Supply Voltage



Transient Response

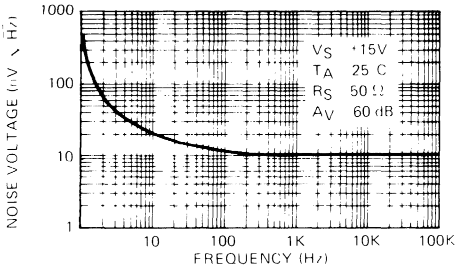


Voltage Follower Large-Signal Pulse Response

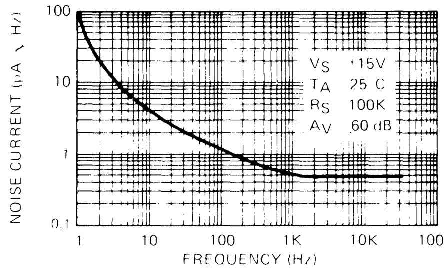


TYPICAL ELECTRICAL DATA

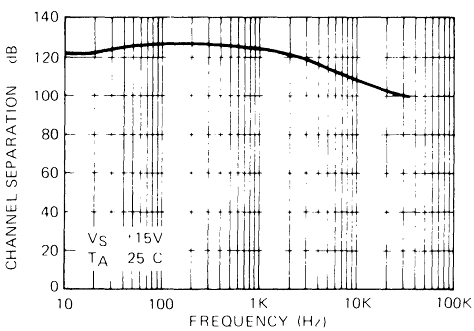
Input Noise Voltage as a Function of Frequency



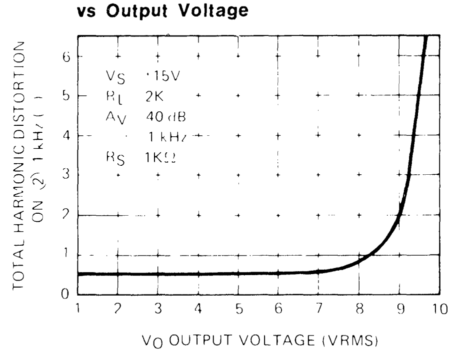
Input Noise Current as a Function of Frequency



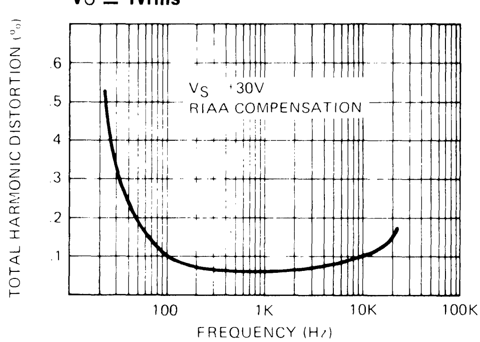
Channel Separation



Total Harmonic Distortion vs Output Voltage



Distortion vs Frequency
Vo = 1vrms



GENERAL DESCRIPTION

The 4559 integrated circuit is a dual high performance operational amplifier internally compensated and constructed on a single silicon chip using the planar epitaxial process.

These amplifiers feature guaranteed AC performance which far exceeds that of the 741-type amplifiers. The specially designed low-noise input transistors allow the 4559 to be used in low-noise signal processing applications such as audio pre amplifiers and signal conditioners.

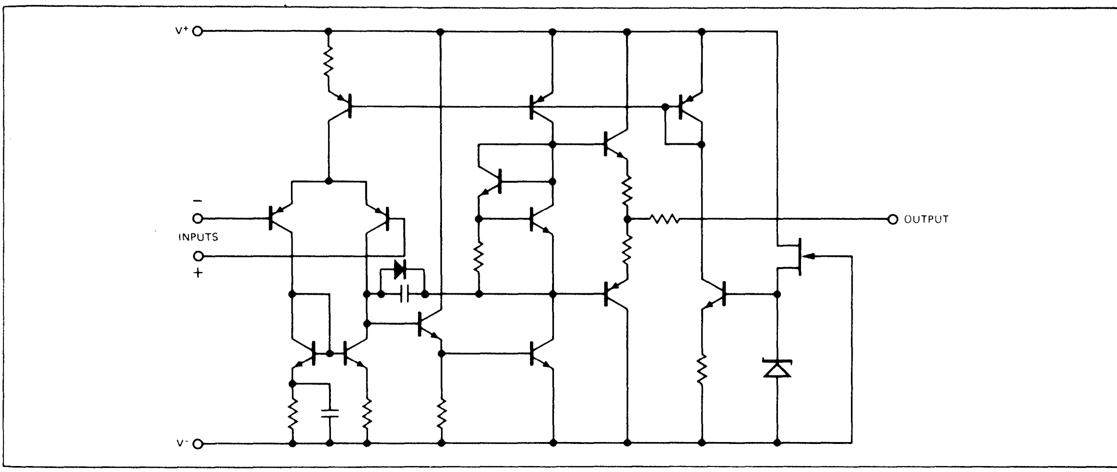
The 4559 also has more output drive than 741-type amplifiers and can be used to drive a 600 ohm load.

FEATURES

	Typical	Guaranteed
• Unity Gain Bandwidth	4.0 MHz	3.0 MHz
• Slew Rate	2.0 V/μsec	1.5 V/μsec
• Low Noise Voltage	1.4 μV_{RMS}	2.0 μV_{RMS}

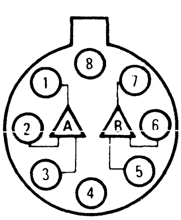
- Supply Voltage ±22V for RM4559 and ±18V for RC4559
- No Frequency Compensation Required
- No Latch Up
- Large Common Mode and Differential Voltage Ranges
- Low Power Consumption
- Parametric Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers

SCHEMATIC DIAGRAM (1/2 Shown)



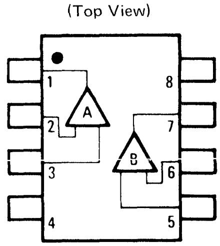
CONNECTION INFORMATION

TE (TO-99)
Metal Can Package
(Top View)



Order Part Nos.:
RC4559T, RM4559T

DE and NB
Dual In-line Packages
(Top View)



Order Part Nos.:
RC4559NB, RV4559NB
RC4559DE, RV4559DE
RM4559DE

PIN	FUNCTION
1	A OUTPUT
2	A -INPUT
3	A +INPUT
4	V^-
5	B +INPUT
6	B -INPUT
7	B OUTPUT
8	V^+

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . RM4559: ±22V
RC4559: ±18V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage. . . . . ±30V
Input Voltage (Note 2). ±15V
Storage Temperature Range. . . . . –65°C to +150°C

Operating Temperature Range
RM4559 . . . . –55°C to +125°C
RV4559 . . . . –40°C to +85°C
RC4559 . . . . 0°C to +70°C
Lead Temperature (Soldering, 60 sec) . . . . 300°C
Output Short-Circuit Duration (Note 3). . . . . . . Indefinite

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±15 V unless otherwise specified.)

PARAMETER	CONDITIONS	RM4559 MIN	RM4559 TYP	RM4559 MAX	RV/RC4559 MIN	RV/RC4559 TYP	RV/RC4559 MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5	100		5	100	nA
Input Bias Current			40	250		40	250	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geqslant 2k\Omega$, V_{out} = ±10V	50,000	300,000		20,000	300,000		V/V
Output Voltage Swing	$R_L \geqslant 3k\Omega$ $R_L \geqslant 600\Omega$	±12 ±9.5	±13 ±10		±12 ±9.5	±13 ±10		V V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leqslant 10k\Omega$	80	100		80	100		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10k\Omega$		10	75		10	75	μV/V
Supply Current	$R_L = \infty$ (All Amplifiers)		3.3	5.6		3.3	5.6	mA
Transient Response (unity gain) Rise Time	V_{IN} = 20mV, R_L = 2kΩ, $C_L \leqslant$ 100pf		80			80		nsec
Overshoot			18			18		%
Slew Rate (unity gain)		1.5	2.0		1.5	2.0		V/μs
Unity Gain Bandwidth		3.0	4.0		3.0	4.0		MHz
Full Power Bandwidth	$V_O = 20\ V_{p-p}$	24	32		24	32		kHz
Input Noise Voltage	f = 20 Hz to 20 kHz		1.4	2.0		1.4	2.0	μV_{RMS}
Input Noise Current	f = 20 Hz to 20 kHz		25			25		pA RMS
Channel Separation	Gain = 100 f = 10 kHz, R_S = 1kΩ		90			90		dB
The following specifications apply for –55°C ≤ T_A ≤ +125°C for RM4559; 0°C ≤ T_A ≤ +70°C for RC4559								
Input Offset Voltage	$R_S \leqslant 10k\Omega$			6.0			7.5	mV
Input Offset Current				300			200	nA
Input Bias Current				500			500	nA
Large-Signal Voltage Gain	$R_L \geqslant 2k\Omega$, V_{out} = ±10V	25,000			15,000			
Output Voltage Swing	$R_L \geqslant 2k\Omega$	±10			±10			V
Supply Current (All Amplifiers)	V_S = ±15 V, $R_L = \infty$ T_A = +125°C T_A = -55°C		3 4	5 6.6		3 4	5 6.6	mA

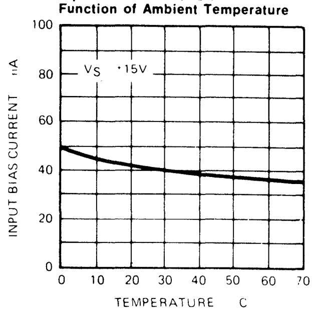
MATCHING CHARACTERISTICS (V_{CC} = ±15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM4559 TYP	RC4559 TYP	UNITS
Voltage Gain	$R_L \geqslant 2k\Omega$	±0.5	±1.0	dB
Input Bias Current		±15	±15	nA
Input Offset Current		±7.5	±7.5	nA
Input Offset Voltage	$R_S \geqslant 10k\Omega$	±0.1	±0.2	mV

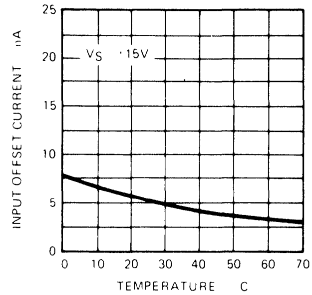
NOTES:
1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C for RM4559.
2. For supply voltages less than -15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one amp only. Rating applies to +125°C case temperature or +75°C ambient temperature for RC4559 and to +85°C ambient temperature for RV4559.

TYPICAL ELECTRICAL DATA

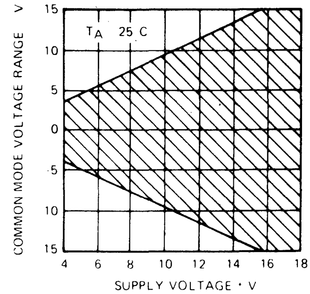
Input Bias Current as a Function of Ambient Temperature



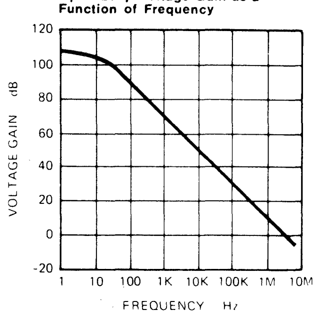
Input Offset Current as a Function of Ambient Temperature



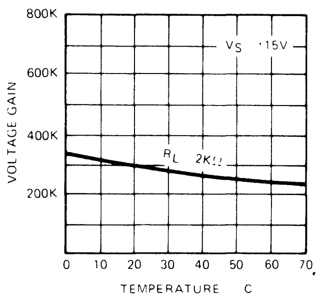
Common Mode Range as a Function of Supply Voltage



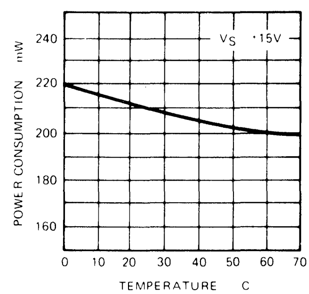
Open Loop Voltage Gain as a Function of Frequency



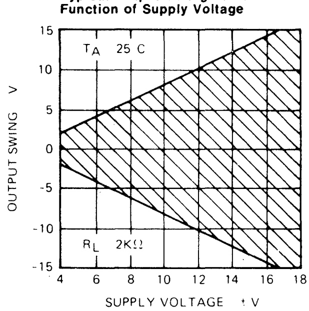
Open Loop Gain as a Function of Temperature



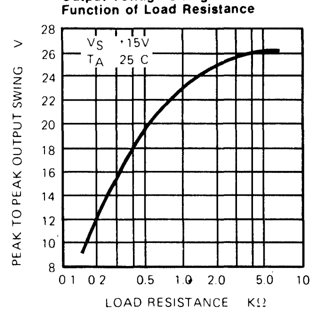
Power Consumption as a Function of Ambient Temperature



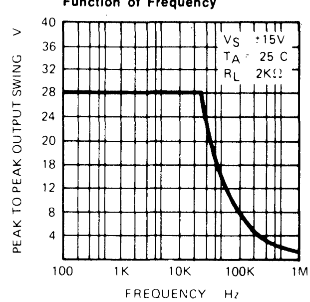
Typical Output Voltage as a Function of Supply Voltage



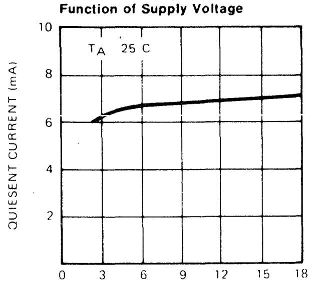
Output Voltage Swing as a Function of Load Resistance



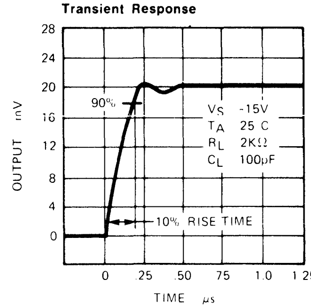
Output Voltage Swing as a Function of Frequency



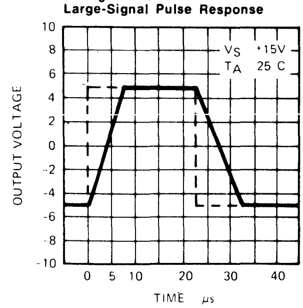
Quiesent Current as a Function of Supply Voltage



Transient Response



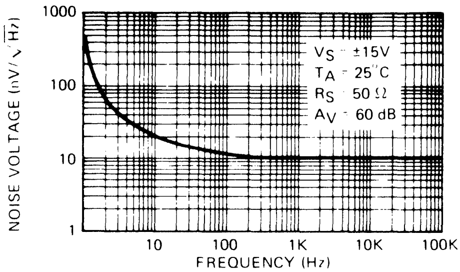
Voltage Follower Large-Signal Pulse Response



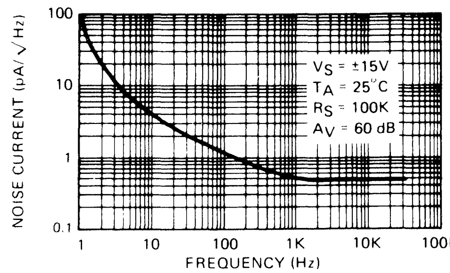
RAYTHEON

TYPICAL ELECTRICAL DATA

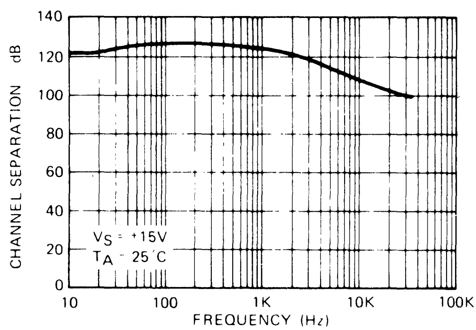
Input Noise Voltage as a Function of Frequency



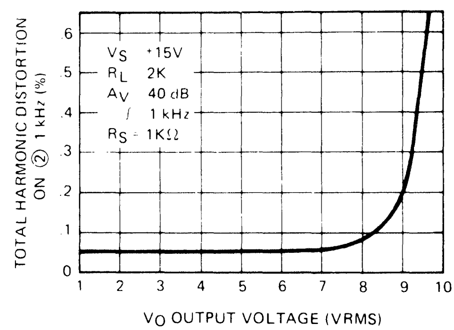
Input Noise Current as a Function of Frequency



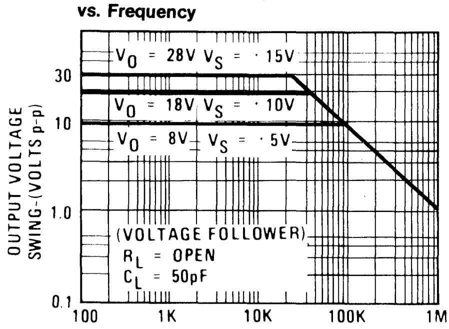
Channel Separation



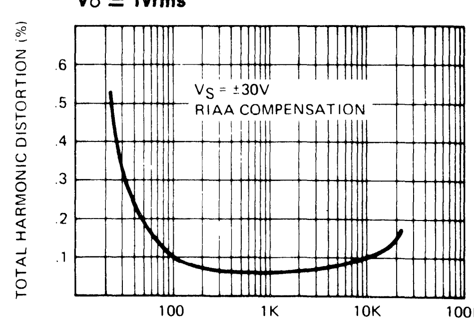
Total Harmonic Distortion vs Output Voltage



Output Voltage Swing vs. Frequency



Distortion vs Frequency Vo = 1vrms



GENERAL DESCRIPTION

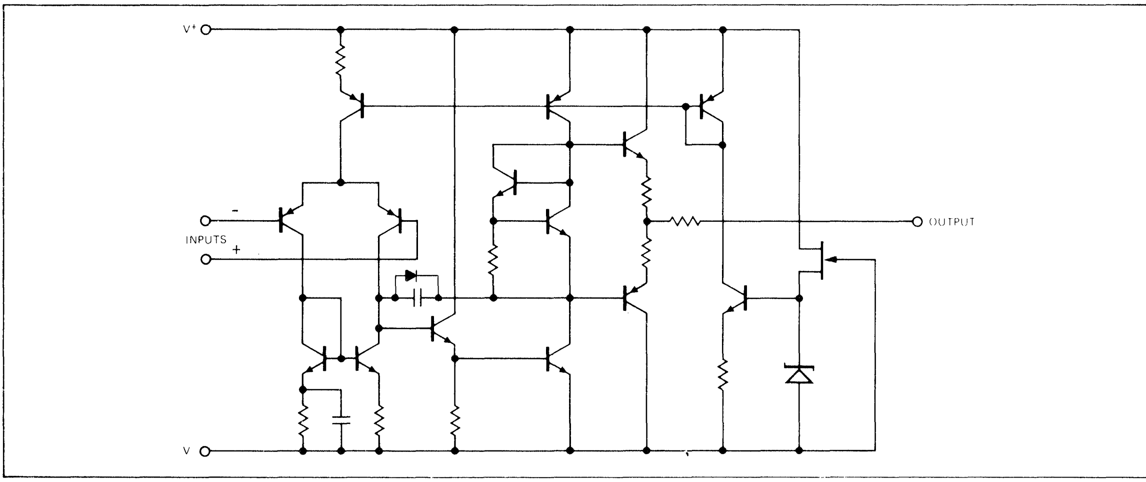
The RC4739 dual low-noise operational amplifier is fabricated on a single silicon chip using the planar epitaxial process. It was designed primarily for preamplifiers in consumer and industrial signal processing equipment. The device is pin compatible with the μA739 and MC1303, however, compensation is internal. This permits a lowered external parts count and simplfied application.

The RC4739 is available in molded dual in-line 14-pin package and operated over the commercial temperature range from 0°C to +70°C.

DESIGN FEATURES

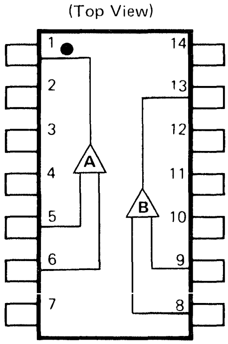
- Internally Compensated Replacement for μA739 and MC1303
- Signal-to-Noise Ratio 76 dB (RIAA 10 mV ref.)
- Channel Separation 125 dB
- Unity Gain Bandwidth 3MHz
- Output Short-Circuit Protected
- 0.1% Distortion at 8.5 V RMS Output into 2 kΩ Load

SCHEMATIC DIAGRAM (1/2 Shown)



CONNECTION INFORMATION

DB
Dual In-line Package
(Top View)



Order Part No.:
RC4739DB

PIN	FUNCTION
1	A OUTPUT
2	NC
3	NC
4	NC
5	+A INPUT
6	-A INPUT
7	V⁻
8	B INPUT
9	+B INPUT
10	NC
11	NC
12	NC
13	B OUTPUT
14	V⁺

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V	Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation (Note 1)	500 mW	Operating Temperature Range	0°C to +70°C
Differential Input Voltage	±30 V	Lead Temperature (Soldering, 60s)	300°C
Input Voltage (Note 2)	±15 V	Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS (V_{CC} = ±15V, T_A = +25°C unless otherwise noted.)

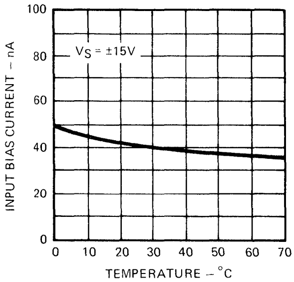
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10\ k\Omega$		2.0	6.0	mV
Input Offset Current			5.0	200	nA
Input Bias Current			40	500	nA
Input Resistance		0.3	5.0		MΩ
Large-Signal Voltage Gain	$R_L \geqslant 2\ k\Omega$ V_{out} = ±10V	20,000	300,000		V/V
Output Voltage Swing	$R_L \geqslant 10\ k\Omega$	±12	±14		V
	$R_L \geqslant 2\ k\Omega$	±10	±13		V
Input Voltage Range		±12	±14		V
Common Mode Rejection Ratio	$R_S \leqslant 10\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leqslant 10\ k\Omega$		10	150	μV/V
Power Consumption			105	170	mW
Transient Response (unity gain) Risetime	V_{in} = 20 mV R_L = 2 kΩ $C_L \leqslant$ 100pF		0.15		μs
Transient Response (unity gain) Overshoot	V_{in} = 20 mV R_L = 2 kΩ $C_L \leqslant$ 100 pF		10		%
Slew Rate (unity gain)	$R_L \geqslant 2\ k\Omega$		1.0		V/μs
Broadband Noise Voltage	B_W = 10-30 KHz R_S = 1 kΩ		2.5		μV_{RMS}
Channel Separation	f = 1.0 kHz A_V = 40 dB R_S = 1 kΩ		125		dB
The following specification apply for 0°C ⩽ T_A ⩽ 70°C unless otherwise specified.					
Input Offset Voltage	$R_S \leqslant 10\ k\Omega$		3.0	7.5	mV
Input Offset Current			7.0	300	nA
Input Bias Current			50	800	nA
Large-Signal Voltage Gain	$R_L \geqslant 2\ k\Omega$ V_{out} = ±10V	15,000	200,000		
Output Voltage Swing	$R_L \geqslant 2\ k\Omega$	±10	±13		V
Power Consumption	V_S = ±15V				
	T_A = 70°C		100	150	mW
	T_A = 0°C		110	220	mW

NOTES:

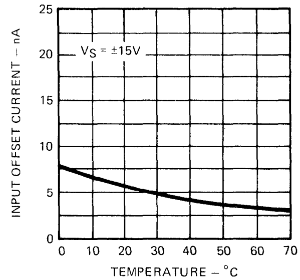
1. Rating applies for ambient temperatures below +70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short-circuit may be to ground, typically 45 mA. Rating applies to +125°C case temperature or +75°C ambient temperature.

TYPICAL ELECTRICAL DATA

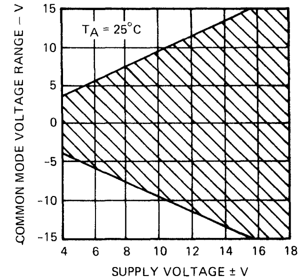
Input Bias Current as a Function of Ambient Temperature



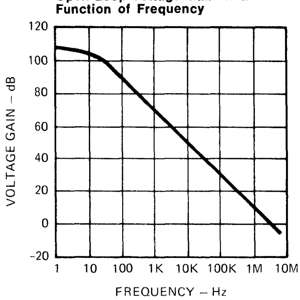
Input Offset Current as a Function of Ambient Temperature



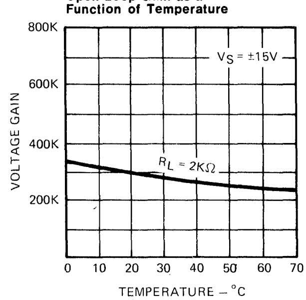
Common Mode Range as a Function of Supply Voltage



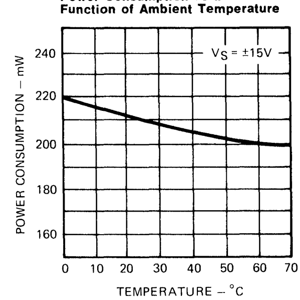
Open Loop Voltage Gain as a Function of Frequency



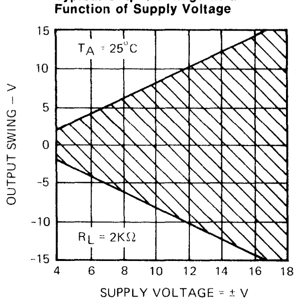
Open Loop Gain as a Function of Temperature



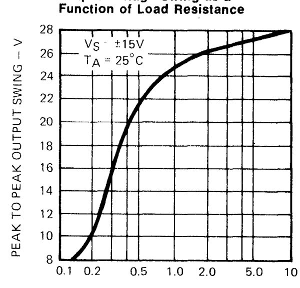
Power Consumption as a Function of Ambient Temperature



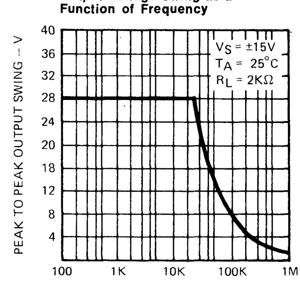
Typical Output Voltage as a Function of Supply Voltage



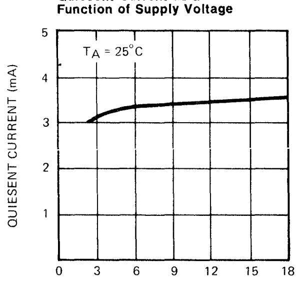
Output Voltage Swing as a Function of Load Resistance



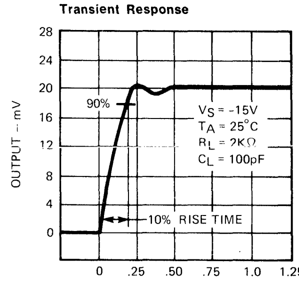
Output Voltage Swing as a Function of Frequency



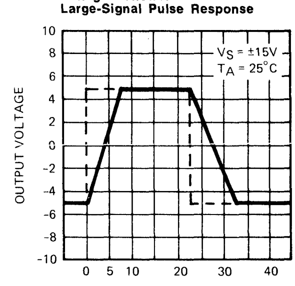
Quiesent Current as a Function of Supply Voltage



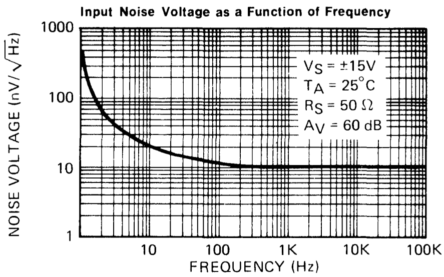
Transient Response

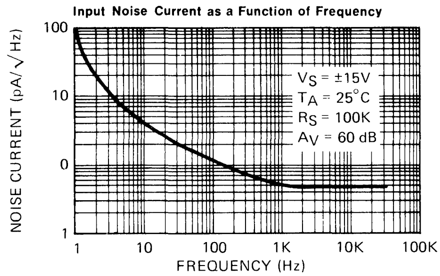


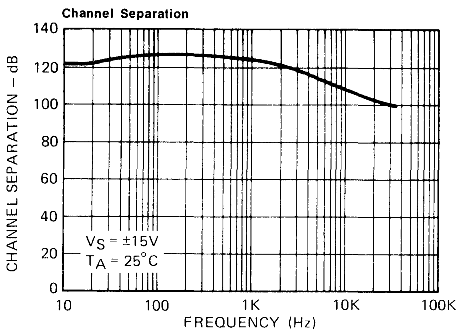
Voltage Follower Large-Signal Pulse Response

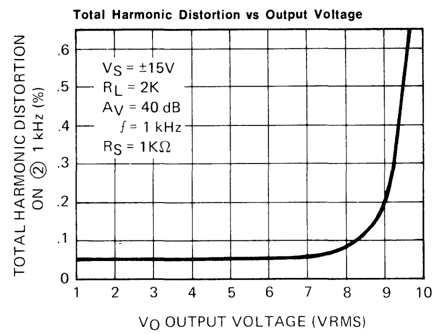


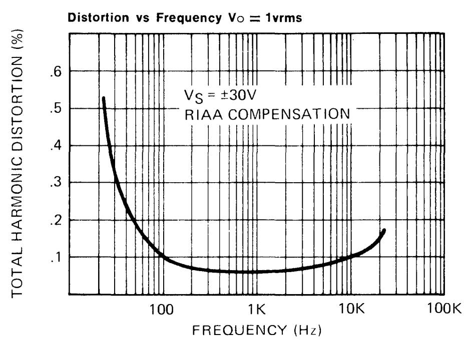
TYPICAL ELECTRICAL DATA





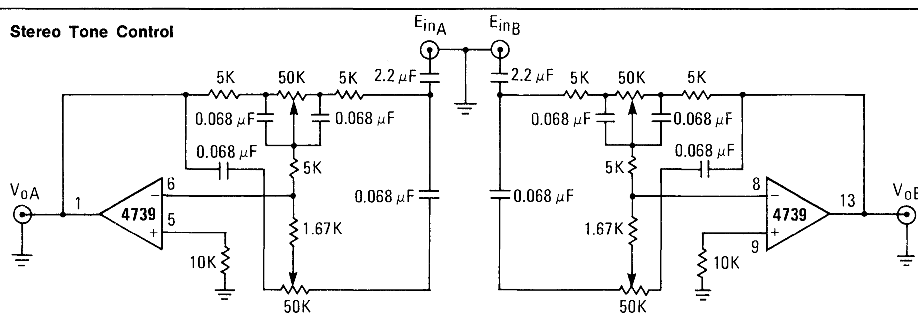






TYPICAL APPLICATIONS

Stereo Tone Control



Quad Operational Amplifier

DESCRIPTION

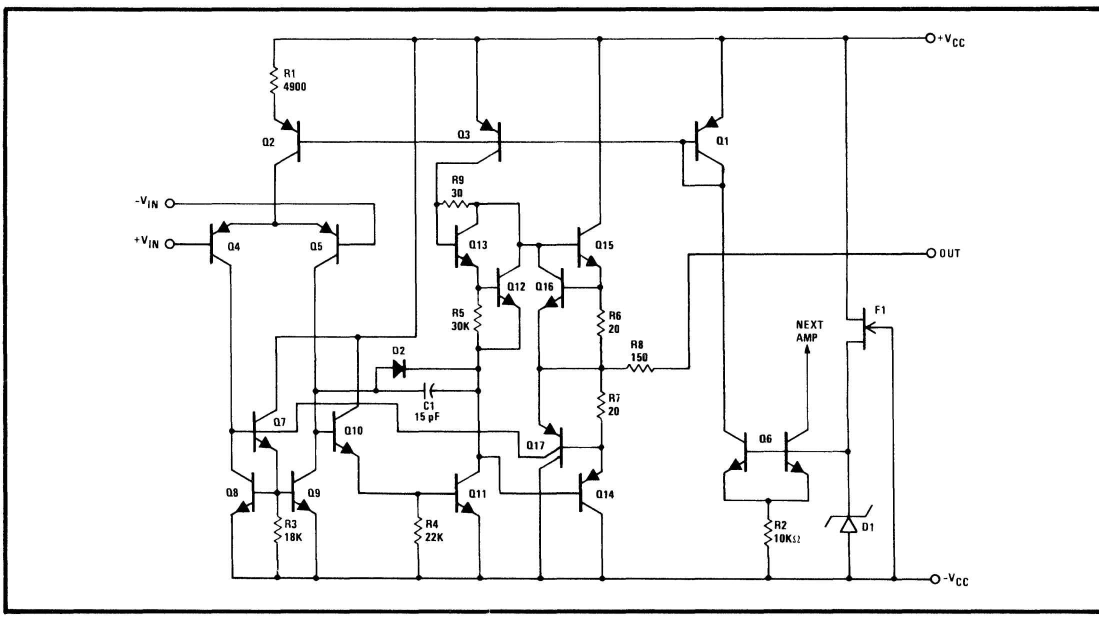
The HA-4741 is a monolithic integrated circuit, consisting of four independent operational amplifiers constructed with the planar epitaxial process.

These amplifiers feature AC and DC performance which exceed that of the 741 type amplifiers. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

FEATURES

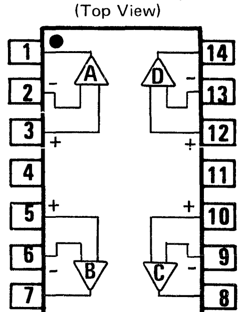
- Unity Gain Bandwidth 3.5 MHz (typical)
- High Slew Rate 1.6V/μS (typical)
- Low Noise Voltage 9nV/$\sqrt{Hz}$ (typical)
- Input Offset Voltage 0.5mV (typical)
- Input Bias Current 60nA (typical)
- Indefinite Short Circuit Protection
- No Crossover Distortion
- Internal Compensation
- Wide Power Supply Range ±2V to ±20V

SCHEMATIC DIAGRAM (1/4 Shown)



CONNECTION INFORMATION

DB and DC
Dual In-line Packages
(Top View)



Order Part Nos.:
HA1-4741-2
HA1-4741-8
HA1-4741-5
HA3-4741-5

PIN	FUNCTION
1	OUTPUT A
2	$-V_{IN}$ A
3	$+V_{IN}$ A
4	V+
5	$+V_{IN}$ B
6	$-V_{IN}$ B
7	OUTPUT B
8	OUTPUT C
9	$-V_{IN}$ C
10	$+V_{IN}$ C
11	V-
12	$+V_{IN}$ D
13	$-V_{IN}$ D
14	OUTPUT D

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . ±20V
Internal Power Dissipation (Note 1) . . . . 880 mW
Differential Input Voltage . . . . ±30V
Input Voltage (Note 2) . . . . ±15V
Output Short Circuit Duration (Note 3) . . . Indefinite

Storage Temperature Range . . . . . -65 to +150°C
Operating Temperature Range
HA-4741-2 . . . . -55 to +125°C
HA-4741-5 . . . . 0 to +70°C
Lead Soldering Temperature (60 sec) . . . . 300°C

ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	HA-4741-2 MIN	HA-4741-2 TYP	HA-4741-2 MAX	HA-4741-5 MIN	HA-4741-5 TYP	HA-4741-5 MAX	UNITS
Input Offset Voltage	$R_S \leqslant 10\ K\Omega$		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geqslant 2\ K\Omega\ V_{OUT} \pm 10V$	50,000	100,000		25,000	50,000		V/V
Input Voltage Range		±12			±12			V
Output Resistance			300			300		Ω
Output Current	$V_{OUT} \pm 10V$	±5	±15		±5	±15		mA
Common Mode Rejection Ratio	$R_S \leqslant 10\ K\Omega\ \Delta V = \pm 5V$	80			80			dB
Supply Current (all amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response								
Rise Time			75			75		ns
Overshoot			25%			25%		%
Slew Rate			1.6			1.6		V/µs
Unity Gain Bandwidth			3.5			3.5		MHz
Full Power Bandwidth	V_O = 20V p-p R_L = 2K		25			25		kHz
Input Noise Voltage	f = 1 kHz		9			9		$nV/\sqrt{Hz}$
Channel Separation			108			108		dB
The following specifications apply for -55°C $\leqslant T_A \leqslant$ +125°C for HA-4741-2, 0°C $\leqslant T_A \leqslant$ +70°C for HA-4741-5.								
Input Offset Voltage	$R_S \leqslant 10\ K\Omega$		4.0	5.0		5.0	6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain	$R_L \geqslant 2\ K\Omega\ V_{OUT} \pm 10V$	25,000			15,000			V/V
Output Voltage Swing	$R_L \geqslant 10\ K\Omega$	±12	±13.7		±12	±13.7		V
	$R_L \geqslant 2\ K\Omega$	±10	±12.5		±10	±12.5		V
Supply Current (all Amplifiers)			10			10		mA
Average Offset Voltage Drift			5			5		µV/°C
Common Mode Rejection Ratio	$R_S \leqslant 10\ K\Omega\ \Delta V \pm 5V$	74			74			dB
Power Supply Rejection Ratio	$R_S \leqslant 10\ K\Omega\ \Delta V \pm 5V$	80			80			dB

Notes:
1. Rating applies for case temperature of +25°C maximum; derate linearity at 6.4 mW/°C for temperatures above +25°C.
2. For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

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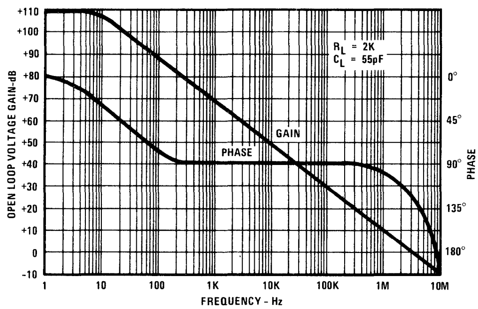
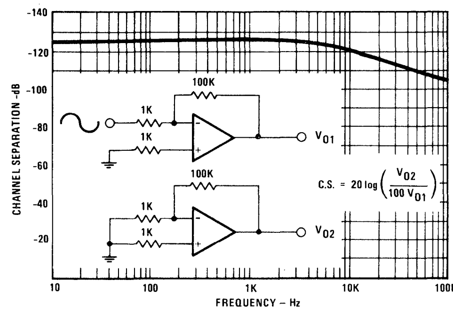
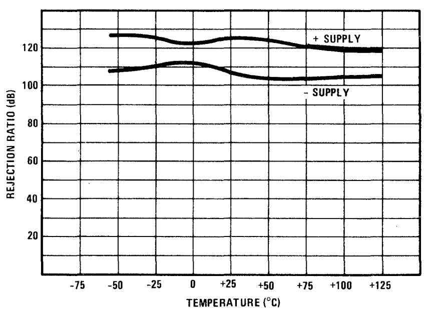
TYPICAL PERFORMANCE DATA



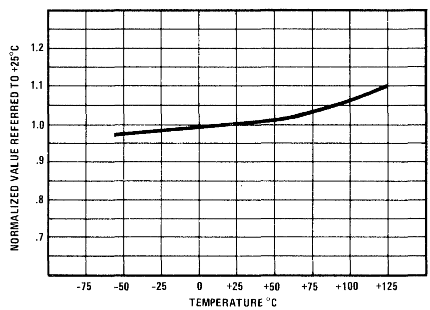
Open Loop Frequency Response



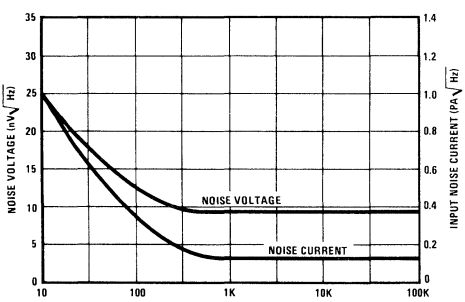
Channel Separation vs. Frequency



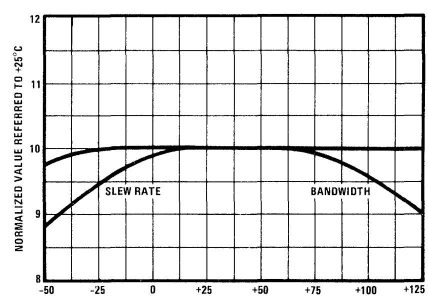
Power Supply Rejection Ratio vs. Temperature



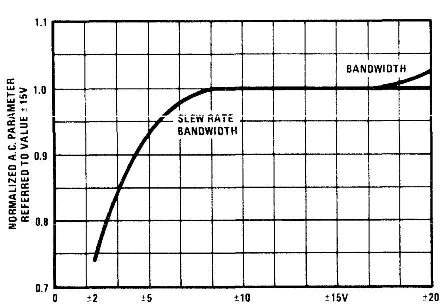
Transient Response vs. Temperature



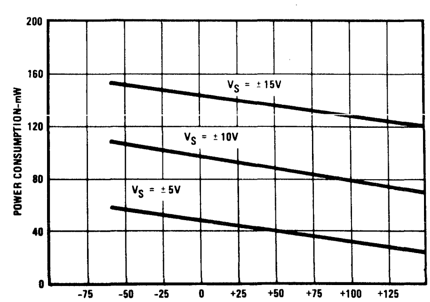
Input Noise vs. Frequency



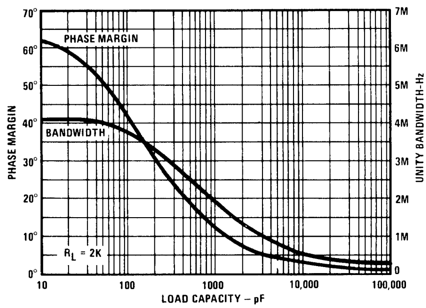
Normalized AC Parameters vs. Temperature



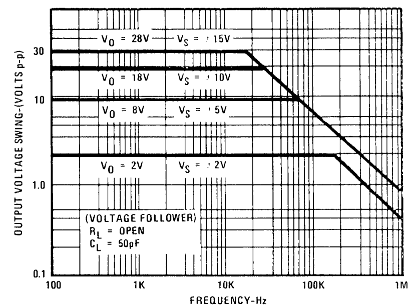
Slew Rate vs. Supply Voltage



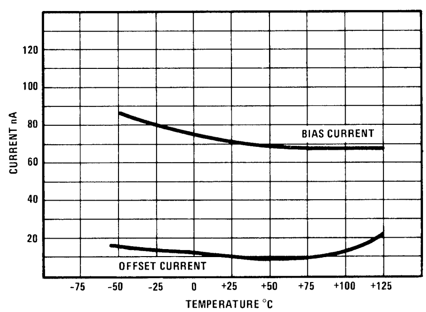
Power Consumption vs. Temperature



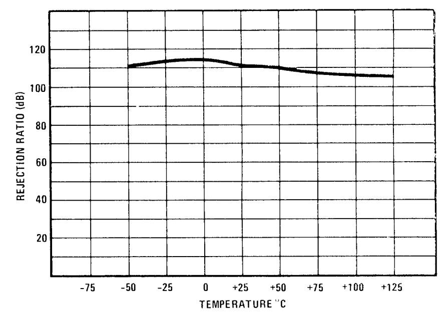
Small Signal Bandwidth and Phase Margin vs. Load Capacitance



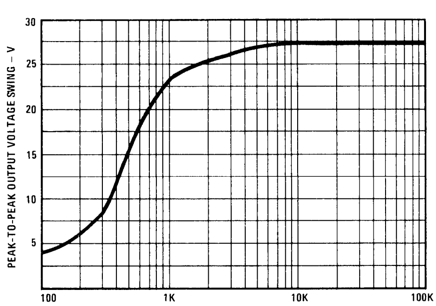
Output Voltage Swing vs. Frequency



Input Currents vs. Temperature



Common Mode Rejection Ratio vs. Temperature



Output Voltage Swing vs. Load Resistance

AVAILABLE TYPES

Part Number	Package	Operating Temperature
HA1-4741-2	Ceramic	-55 to +125°C
HA1-4741-8*	Ceramic	-55 to +125°C
HA1-4741-5	Ceramic	0 to +70°C
HA3-4741-5	Plastic	0 to +70°C

* Processed to MIL-STD-883 Class B

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SECTION 2

Wideband Amplifier

CONTENTS

GENERAL DESCRIPTION

The RM733/RC733 integrated circuit is a monolithic video amplifier with differential inputs and differential outputs. It offers three selectable voltage gains of 10, 100, or 400 and adjustable gain of 10 to 400 using a single resistor. No external frequency compensation is necessary for any gain option. The circuit and process designs are optimized to give a stable gain (±10%), wide bandwidth (DC to 120MHz), high input resistance (250kΩ), and low phase shift that is linear up to 10MHz (2° per MHz).

The RM733/RC733 is designed for use as a read head amplifier for magnetic tape, drum, or disc memories using phase of NRZ encoding. It will also function as a preamplifier for high speed film or plated wire memory systems; as a video or pulse amplifier, pulse height detector, peak detector.

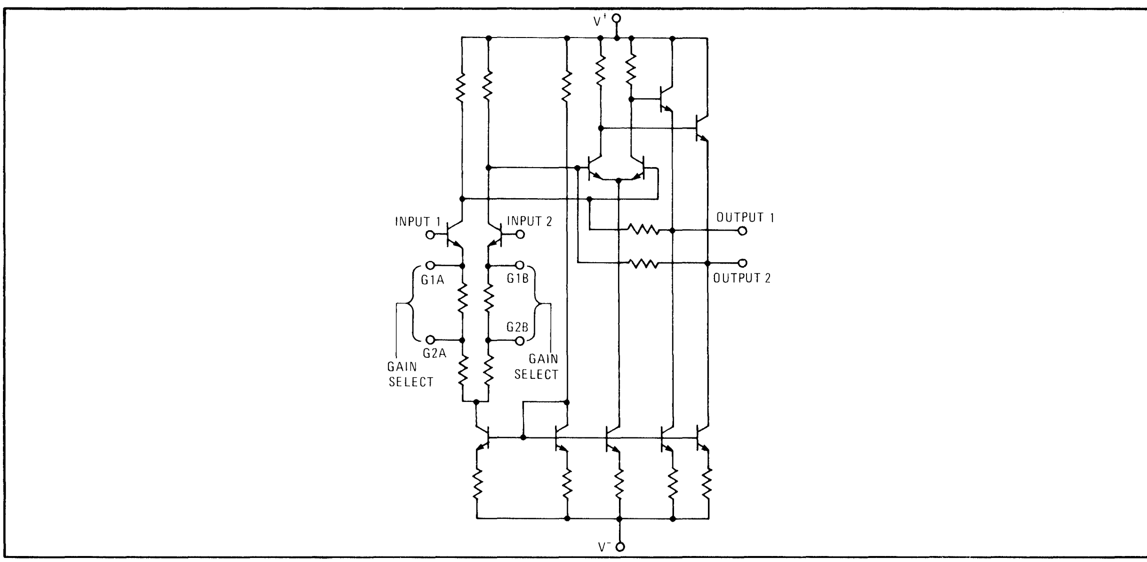
Applications for the RM733/RC733 include bulk computer memory systems, very high speed random access memory systems, communications systems, nuclear event instrumentation, frequency counters, and other systems where the specific design features of the RM733/RC733 are required.

The RM733 video amplifier will operate over the complete military temperature range from −55°C to +125°C while the commercial version, the RC733, operates from 0°C to +70°C.

DESIGN FEATURES

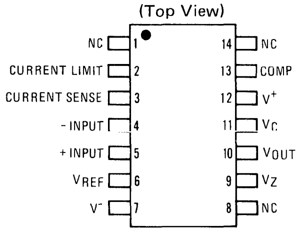
- Wide Bandwidth DC to 120MHz
- Low Linear Phase Shift 2τ/MHz to 10MHz
- Selectable Voltage Gains 10, 100, or 400
- Excellent Pulse Characteristics
- High Input Resistance 250kΩ

SCHEMATIC DIAGRAM



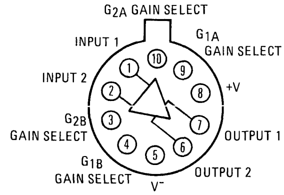
CONNECTION INFORMATION

DB and DC Dual In Line Packages
(Top View)



Order Part Nos.:
RM733DC, RC733DC,
RC733DB

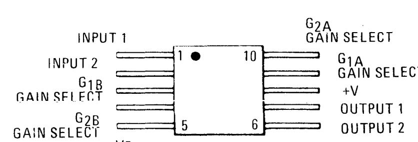
TF Metal Can Package
(Top View)



NOTE: Pin 5 connected to case.

Order Part Nos.:
RM733T
RC733T

CQ Flat Pack Package



Order Part Nos.:
RM733CQ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8.0V
Differential Input Voltage	±5.0V
Common Mode Input Voltage	±6.0V
Input Current	10mA
Internal Power Dissipation Metal Can (Note 1)	500mW
Flat Pack	570mW
Operating Temperature Range	
RM733	-55°C to +125°C
RC733	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60s)	300°C

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	(Note 3)	CONDITIONS	RM733 MIN	RM733 TYP	RM733 MAX	RC733 MIN	RC733 TYP	RC733 MAX	UNITS
Differential Voltage Gain	Gain 1		300	400	500	250	400	600	
	Gain 2		90	100	110	80	100	120	
	Gain 3		9.0	10	11	8.0	10	12	
Bandwidth	Gain 1	$R_S = 50\Omega$		40			40		MHz
	Gain 2			90			90		
	Gain 3			120			120		
Risetime	Gain 1	$R_S = 50\Omega$, $V_{OUT} = 1V_{PP}$		10.5			10.5		ns
	Gain 2			4.5	10		4.5	12	
	Gain 3			2.5			2.5		
Propagation Delay	Gain 1	$R_S = 50\Omega$, $V_{OUT} = 1V_{PP}$		7.5			7.5		ns
	Gain 2			6.0	10		6.0	10	
	Gain 3			3.6			3.6		
Input Resistance	Gain 1			4.0			4.0		kΩ
	Gain 2		20	30		10	30		
	Gain 3			250			250		
Input Capacitance		Gain 2		2.0			2.0		pF
Input Offset Current				0.4	3.0		0.4	5.0	μA
Input Bias Current				9.0	20		9.0	30	μA
Input Noise Voltage		$R_S = 50\Omega$, BW = 1kHz to 10MHz		12			12		μVrms
Input Voltage Range			±1.0			±1.0			V
Common Mode Rejection Ratio	Gain 2	$V_{CM} = \pm1V$, $R \leqslant 100kHz$	60	86		60	86		dB
		$V_{CM} = \pm1V$, f = 5MHz		60			60		
Supply Voltage Rejection Ratio	Gain 2	$\Delta V_S = \pm0.5V$	50	70		50	70		dB
Output Offset Voltage	Gain 1			0.6	1.5		0.6	1.5	V
	Gain 2 Gain 3			0.35	1.0		0.35	1.5	
Output Common Mode Voltage			2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing			3.0	4.0		3.0	4.0		V_{PP}
Output Sink Current			2.5	3.6		2.5	3.6		mA
Output Resistance				20			20		Ω
Power Supply Current				18	24		18	24	mA

NOTES:

1. For RM733 the rating applies for case temperature to +125°C; derate RM733T linearly at 6.5 mW/°C for ambient temperature above 75°C. For RC733T, the rating applies for ambient temperatures to 70°C. For RM733CQ, derate linearly at 7.2 mW/°C for ambient temperature above 75°C.
2. $V_S = \pm6.0V$; $T_A = 25°C$ unless otherwise noted.
3. Gain 1: G1A and G1B connected together; Gain 2: G2A and G2B connected together; Gain 3: Gain select pins open.

ELECTRICAL CHARACTERISTICS

(The following specifications apply for $-55^{\circ}C \leqslant T_A \leqslant 125^{\circ}C$ for the RM733 and $0^{\circ}C \leqslant T_A \leqslant 70^{\circ}C$ for the RC733, $V_S = \pm 6.0V$)

PARAMETER	CONDITIONS	LM733			LM733C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Differential Voltage Gain Gain 1		200		600	250		600	
Gain 2		80		120	80		120	
Gain 3		8.0		12.0	8.0		12.0	
Input Resistance Gain 2		8			8			kΩ
Input Offset Current				5			6	μA
Input Bias Current				40			40	μA
Input Voltage Range		±1			±1			V
Common-Mode Rejection Ratio Gain 2		50			50			dB
Supply Voltage Rejection Ratio Gain 2		50			50			db
Output Offset Voltage Gain 1				1.5			1.5	V
Gain 2 and 3				1.2			1.5	V
Output Voltage Swing		2.5			2.8			V p-p
Output Sink Current		2.2			2.5			mA
Power Supply Current				27			27	mA

SECTION 3

Voltage Regulators

CONTENTS

GENERAL DESCRIPTION

The LM105 series are positive voltage regulators, each constructed on a silicon chip by the planar epitaxial process.

They are similar to the LM100, except for an extra gain stage to improve regulation. In both linear and switching regulator circuits with outputs greater than 4.5V, these devices are direct plug-in replacements for the LM100.

The LM105 military version operates from −55°C to +125°C. The LM305/LM305A are commercial versions which operate from 0°C to +70°C.

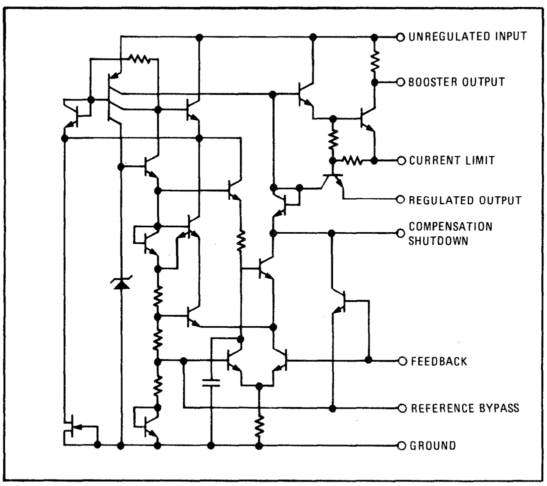
These regulators feature fast response to load and line transients, freedom from oscillations with varying resistive and reactive loads, and reliable starts on any load within ratings.

The LM205 is the same as the LM105 except its performance is guaranteed from −25°C to +85°C.

DESIGN FEATURES

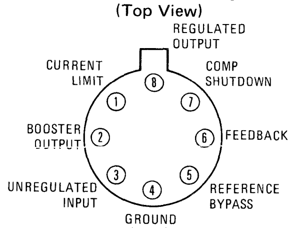
- Output Voltage Adjustable from 4.5V to 40V
- Output Currents in Excess of 10A by Adding External Transistors
- Load Regulation Better Than 0.1%, Full Load With Current Limiting
- DC Line Regulation Guaranteed at 0.03%/V
- Ripple Rejection of 0.01%/V
- 45mA Output Current Without External Pass Transistor

SCHEMATIC DIAGRAM



CONNECTION INFORMATION

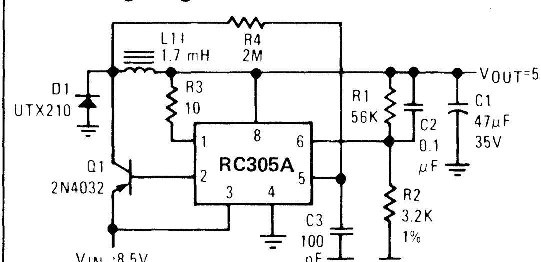
TE Metal Can Package
(Top View)



Order Part Nos.:
LM105H, LM205H,
LM305H, LM305AH

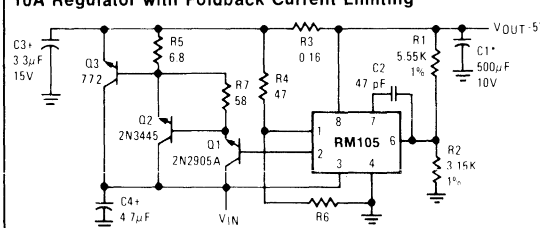
TYPICAL APPLICATIONS

Switching Regulator



†Solid tantalum
‡125 turns = 22 on Arnold Engineering A262123-2 molybdenum permalloy core.

10A Regulator with Foldback Current Limiting



†Solid tantalum
*Electrolytic

ABSOLUTE MAXIMUM RATINGS

Input Voltage LM105, LM205, LM305A:	50V
LM305:	40V
Input-Output Voltage Differential	40V
Power Dissipation (Note 1)	
LM105, LM205, LM305A	800mW
LM305	500mW
Operating Temperature Range	
LM105	$-55^\circ C$ to $+150^\circ C$
LM205	$-25^\circ C$ to $+85^\circ C$
LM305/305A	$0^\circ C$ to $+70^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering, 10s)	$300^\circ C$

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	LM105/205/305A		8.5		50	V
	LM305		8.5		40	
Output Voltage Range	LM105/205/305A		4.5		40	V
	LM305		4.5		30	
Output-Input Voltage Differential			3.0		30	V
Load Regulation (Note 3)	LM105	$0 \leqslant I_O \leqslant 12mA$				%
		$R_{SC} = 10\Omega$, $T_A = 25^\circ C$		0.02	0.05	
		$R_{SC} = 10\Omega$, $T_A = 125^\circ C$		0.03	0.1	
		$R_{SC} = 10\Omega$, $T_A = -55^\circ C$		0.03	0.1	
	LM205	$0 \leqslant I_O \leqslant 12mA$				%
		$R_{SC} = 10\Omega$, $T_A = 25^\circ C$		0.02	0.05	
		$R_{SC} = 10\Omega$, $T_A = 85^\circ C$		0.03	0.1	
		$R_{SC} = 10\Omega$, $T_A = -25^\circ C$		0.03	0.1	
	LM305A	$0 \leqslant I_O \leqslant 45mA$				%
		$R_{SC} = 0\Omega$, $T_A = 25^\circ C$		0.02	0.2	
		$R_{SC} = 0\Omega$, $T_A = 70^\circ C$		0.03	0.4	
		$R_{SC} = 0\Omega$, $T_A = 0^\circ C$		0.03	0.4	
	LM305	$0 \leqslant I_O \leqslant 12mA$				%
		$R_{SC} = 10\Omega$, $T_A = 25^\circ C$		0.02	0.05	
		$R_{SC} = 15\Omega$, $T_A = 70^\circ C$		0.03	0.1	
		$R_{SC} = 10\Omega$, $T_A = 0^\circ C$		0.03	0.1	
Line Regulation		$V_{IN} - V_{OUT} \leqslant 5V$		0.025	0.06	%/V
		$V_{IN} - V_{OUT} > 5V$		0.015	0.03	
Ripple Rejection		$C_{REF} = 10\mu F$, $F = 120Hz$		0.003	0.01	%/V
Temperature Stability	LM105	$-55^\circ C \leqslant T_A \leqslant 125^\circ C$		0.3	1.0	%
	LM205	$-25^\circ C \leqslant T_A \leqslant 85^\circ C$		0.3	1.0	
	LM305/LM305A	$0^\circ C \leqslant T_A \leqslant 70^\circ C$		0.3	1.0	
Current Limit Sense Voltage (Note 4)		$R_{SC} = 10\Omega$, $T_A = 25^\circ C$, $V_{OUT} = 0V$	225	300	375	mV
Feedback Sense Voltage	LM105/205/305		1.63	1.7	1.81	V
	LM305A		1.55	1.7	1.85	
Output Noise Voltage		$10Hz \leqslant f \leqslant 10kHz$				%
		$C_{REF} = 0$		0.005		
		$C_{REF} > 0.1\mu F$		0.002		
Standby Current Drain	LM305	$V_{IN} = 40V$		0.8	2.0	mA
	LM105/205/305A	$V_{IN} = 50V$		0.8	2.0	
Long Term Stability				0.1	1.0	%

NOTES:

1. The maximum junction temperature of the LM105 is 150°C and 85°C for the LM305. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to ambient, or 45°C/W junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval, for the LM105, and averaged over a two second inverval for the LM305.
2. These specifications apply for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.
3. The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.
4. No external pass transistor.

GENERAL DESCRIPTION

The RM723/RC723 integrated circuits are monolithic voltage regulators constructed on a single silicon chip. They consist of a temperature compensated reference amplifier, error amplifier, a power series pass transistor capable of 150mA, and current limiting circuitry.

They feature low standby current drain, low temperature drift and high ripple rejection.

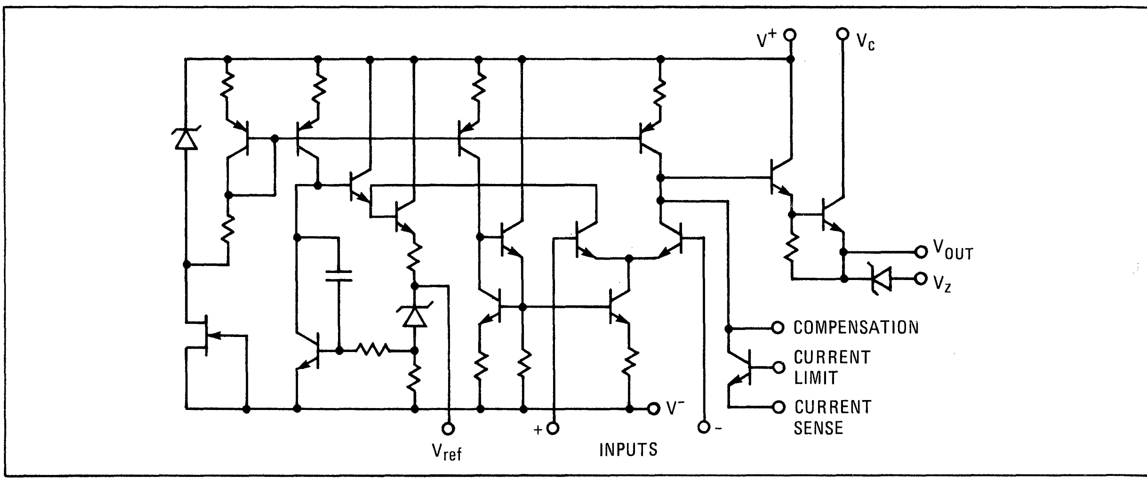
These devices are designed for use as a logic card regulator, small instrument power supply, or, by use of an external pass transistor, as a negative or floating regulator. They may also be used where local voltage supply regulation is required for linear and digital circuits. Provision is made for adjustable current limiting and remote shutdown.

The RM723 operates over the full military temperature range from −55°C to +125°C. The RC723 operates from 0°C to +70°C.

DESIGN FEATURES

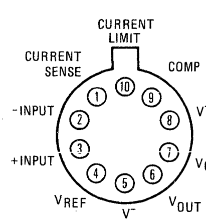
- Positive or Negative Supply Operation
- Series, Shunt, Switching or Floating Operation
- 0.01% Line and Load Regulation
- Output Voltage Adjustable from 2V to 37V
- Output Current to 150mA Without External Pass Transistor

SCHEMATIC DIAGRAM



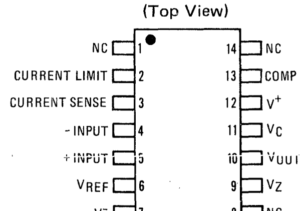
CONNECTION INFORMATION

TF Metal Can Package
(Top View)



Order Part Nos.:
RM723T, RC723T

DC and DB
Dual In-line Package
(Top View)



Order Part Nos.:
RM723DC, RC723DC,
RC723DB

ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V^+ to V^- (50 ms) RM723: 50V
Continuous Voltage from V^+ to V^- 40V
Input-Output Voltage Differential 40V
Maximum Output Current 150mA
Current from V_Z 25mA
Current from V_{REF} 15mA
Internal Power Dissipation-Metal Can (Note 1) . . . 900mW
Internal Power Dissipation—DIP (Note 1) 900mW
Operating Temperature Range
RC723 . . . . 0°C to +70°C
RM723 . . . . −55°C to +125°C
Storage Temperature Range . . . . −65°C to +150°C
Lead Temperature (Soldering, 60s) . . . . 300°C

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	RM723			RC723			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		0.01	0.1		0.01	0.1	% V_{OUT}
	V_{IN} = 12V to V_{IN} = 40V		0.02	0.2		0.1	0.5	
	−55°C ⩽ T_A ⩽ +125°C, V_{IN} = 12V to V_{IN} = 15V			0.3			0.3	
Load Regulation	I_L = 1mA to I_L = 50mA		0.03	0.15		0.03	0.2	% V_{OUT}
	−55°C ⩽ T_A ⩽ +125°C, I_L = 1mA to I_L = 50mA			0.6			0.6	
Ripple Rejection	f = 50Hz to 10kHz, C_{REF} = 0		74			74		dB
	f = 50Hz to 10kHz, C_{REF} = 5μF		86			86		
Average Temperature Coeffieient of Output Voltage	−55°C ⩽ T_A ⩽ +125°C (RM) 0°C ⩽ T_A ⩽ 70°C (RC)		0.002	0.015		0.003	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100Hz to 10kHz, C_{REF} = 0		20			20		μV_{rms}
	BW = 100Hz to 10kHz, C_{REF} = 5μF		2.5			2.5		
Long Term Stability			0.1			0.1		%/1000 hr
Standby Current Drain	I_L = 0, V_{IN} = 30V, V_O = V_{REF}		2.3	3.5		2.3	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input-Output Voltage Differential		3.0		38	3.0		38	V

NOTES:

1. Derate metal can package at 6.8mW/°C and dual in-line package at 7.8mW/°C for operation at ambient temperatures above +25°C.
2. Unless otherwise specified, T_A = 25°C, $V_{IN} = V^+ = V_C$ = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1mA, R_{SC} = 0, C_i = 100pF, C_{REF} = 0, divider impedance as seen by error amplifier ⩽10kΩ.
3. For metal can applications where V_Z is required, an external 6.2 zener should be connected in series with V_{OUT}.

GENERAL DESCRIPTION

The RM4194 and RC4194 are dual polarity tracking regulators designed to provide balanced or unbalanced positive and negative output voltages at currents to 200mA. A single external resistor adjustment can be used to change both outputs between the limits of ±50mV and ±42V.

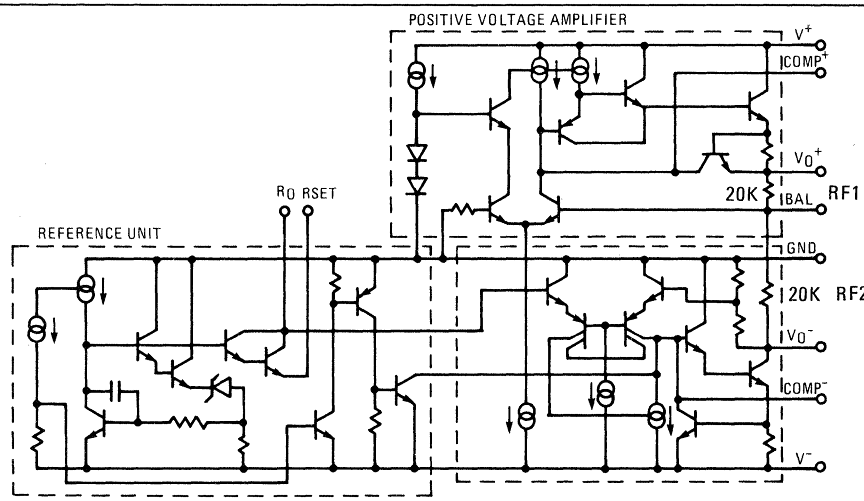
These devices are designed for local "on-card" regulation, eliminating distribution problems associated with single-point regulation. To simplify application the regulators require a minimum number of external parts.

The device is available in two package types to accommodate various power requirements. The TK (TO-66) power package can dissipate up to 3W at T_A = 25°C. The DC 14-pin dual in-line will dissipate up to 1W.

DESIGN FEATURES

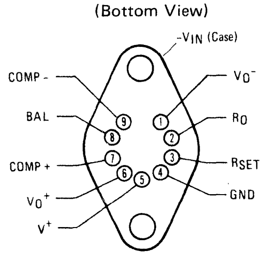
- Simultaneously Adjustable Outputs With One Resistor to ±42V
- Load Current ±200mA with 0.2% Load Regulation
- Internal Thermal Shutdown at T_j = 175°C
- External Balance for $\pm V_0$ Unbalancing
- 3W Power Dissipation

SCHEMATIC DIAGRAM



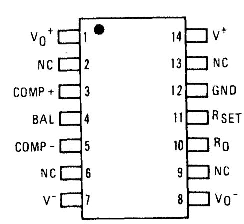
CONNECTION INFORMATION

TK (TO-66) Package
(Bottom View)



Order Part Nos.:
RC4194TK, RM4194TK

DB and DC Dual In-line Package
(Top View)



Order Part Nos.:
RC4194DB, RC4194DC, RM4194DC

ABSOLUTE MAXIMUM RATINGS

Input Voltage ±V to Ground . . . . RM4194: ±45V
RC4194: ±35V
Input-Output Voltage Differential . . . . . . RM4194: ±45V
RC4194: ±35V
Power Dissipation at T_A = 25°C
DC Package 1W
TK Package 3.0W
DB Package 625mW

Load Current
DC Package 150mA
TK Package 250mA
DB Package 100mA
Operation Junction Temperature Range
RM4194 . . . . -55°C to +150°C
RC4194 . . . . .0°C to +125°C
Storage Temperature Range. . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . +300°C

ELECTRICAL CHARACTERISTICS

($\pm 5 \leqslant V_{OUT} \leqslant V_{MAX}$; RM4194: -55°C$\leqslant T_j \leqslant$+125°C; RC4194: 0°C$\leqslant T_j \leqslant$+70°C) (Note 2)

PARAMETER	CONDITIONS	RM4194			RC4194			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	$\Delta V_{IN} = 0.1V_{IN}$		0.04	0.1		0.04	0.1	$\%V_{OUT}$
Load Regulation	4194TK: I_L = 1 to 200mA 4194DC: I_L = 1 to 100mA, T_j = +25°C		0.001	0.002		0.002	0.004	%V°/mA
	RM4194 = t_j = -55°C – +125°C RC4194 = t_j = 0°C – +70°C		0.002	0.004		0.002	0.004	%V°/mA
TC of Output Voltage			0.002	0.015		0.002	0.015	%/°C
TC of Output Voltage			0.002	0.015		0.003	0.015	%/°C
Stand-By Current Drain (Note 1)	$V_{IN} = V_{MAX}$, V_o = 0V		+0.3	+1.0		+0.3	+1.5	mA
	$V_{IN} = V_{MAX}$, V_o = 0V		−1.2	−2.0		−1.2	−3.0	
Input Voltage Range		±9.5		±45	±9.5		±35	V
Output Voltage Scale Factor	R_{set} = 71.5K, T_j = 25°C	2.42	2.5	2.58	2.38	2.5	2.62	KΩ/V
Output Voltage Range	R_{set} = 71.5K	0.05		±42	0.05		±32	V
Output Voltage Tracking				1.0			2.0	%
Ripple Rejection	f = 120Hz, T_j = 25°C		70			70		dB
Input-Output Voltage Differential	I_L = 50mA T_A = +25°C	3.0			3.0			V
Output Short Circuit Current	V_{IN} = ±30V Max.		300			300		mA
Output Noise Voltage	C_L = 4.7µF, V_o = ±15V f = 10Hz to 100KHz		250			250		µV RMS
Internal Thermal Shutdown			175			175		°C

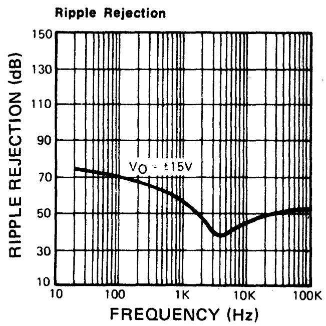
THERMAL CHARACTERISTICS

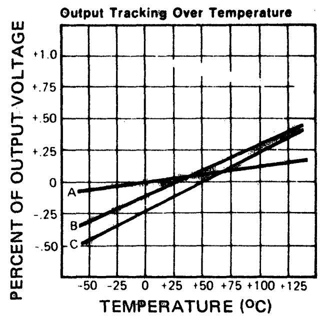
PARAMETER	CONDITIONS	PACKAGE		
		DB	DC	TK (TO-66)
Power Dissipation	T_A = 25°C	625mW	1W	3W
	T_C = 25°C	1.25W	2.2W	17.5W
Thermal Resistance	Junction to Ambient, θ_{J-A}	160°C/W	128°C/W	41.6°C/W
	Junction to Case, θ_{J-C}	80°C/W	55°C/W	7.15°C/W

NOTE:

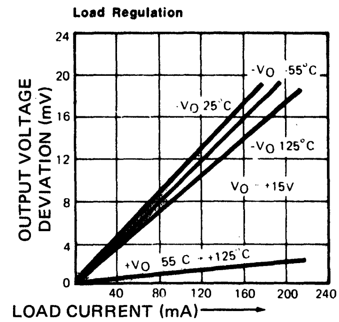
1. $\pm I_{Quiescent}$ will increase by 50µA/V_{OUT} on positive side and 100µA/V_{OUT} on negative side.
2. The specifications above apply for the given junction temperatures since pulse test conditions are used.

TYPICAL ELECTRICAL TEST DATA



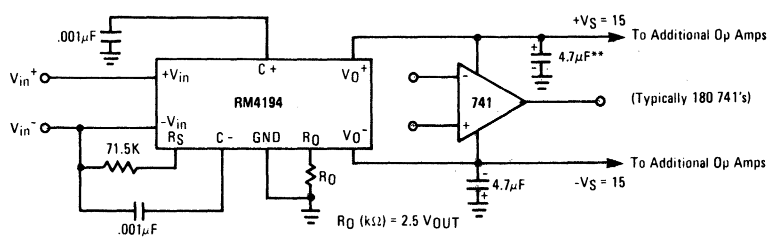


A = % Tracking of outputs vs. temperature
B = T.C. for positive regulator
C = T.C. for negative regulator

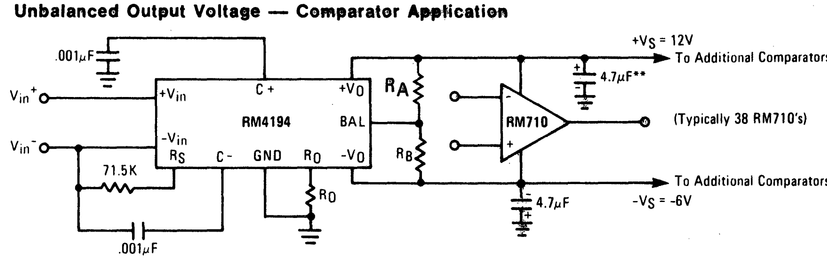


TYPICAL APPLICATIONS

Balanced Output Voltage — Op Amp Application

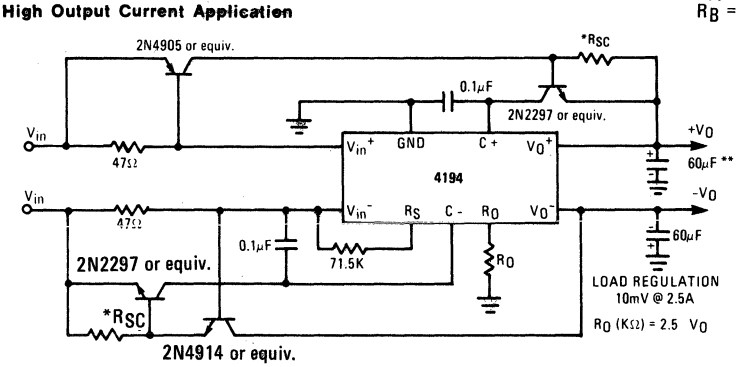


Unbalanced Output Voltage — Comparator Application



R_O (kΩ) = 2.5 ($-V_{OUT}$)
Adjust R_O for $-V_S$ = -6V (15KΩ)
$R_{F1} = R_{F2}$ = 20KΩ (see schematic)
$|+V_{OUT}| = |-V_{OUT}| \dfrac{R_{F1} \parallel R_A}{R_{F2} \parallel R_B}$
$R_A = \infty$ when $|+V_{OUT}| > |-V_{OUT}|$
$R_B = \infty$ when $|-V_{OUT}| > |+V_{OUT}|$
For $+V_S$ = 12 when $-V_S$ = 6V
$R_A = \infty$
R_B = 20KΩ

High Output Current Application



$*R_{SC} = \dfrac{0.7}{I_{SC}}$

Note: Compensation and bypass capacitor connections should be as close as possible to the 4194.

**Optional usage – not as critical as $-V_0$ bypass capacitors.

GENERAL DESCRIPTION

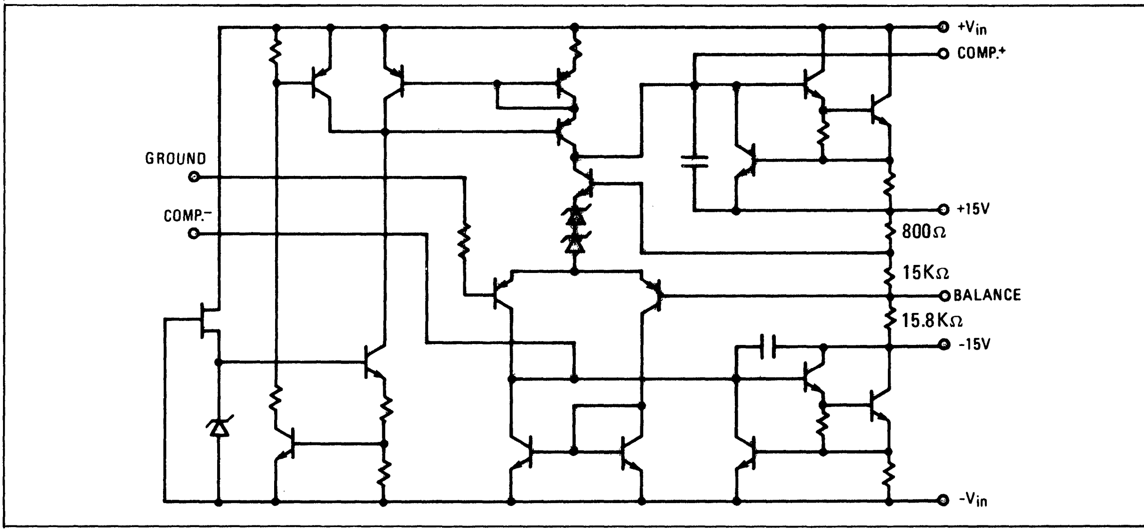
The RM4195 and RC4195 are dual polarity tracking regulators designed to provide balanced positive and negative 15V output voltages at currents to 100mA. These devices are designed for local "on-card" regulation eliminating distribution problems associated with single point regulation. The regulator is intended for ease of application. Only two external components are required for operation (two 10μF bypass capacitors).

The device is available in three package types to accommodate various applications requiring economy, high power dissipation, and reduced component density.

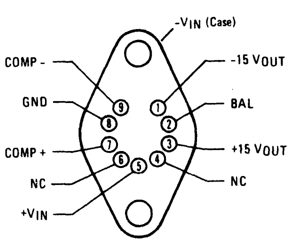
DESIGN FEATURES

- ±15V Operational Amplifier Power at Reduced Cost and Component Density
- Thermal Shutdown at T_j = +175°C in Addition to Short-Circuit Protection
- Output Currents to 100mA
- May be Used as Single Output Regulator with up to +50V Output
- Available in TO-66, TO-99, and 8-Pin Plastic Mini-DIP

SCHEMATIC DIAGRAM

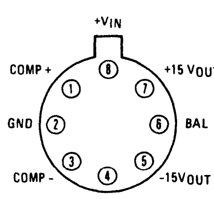


TK (TO-66) Power Package
(Bottom View)



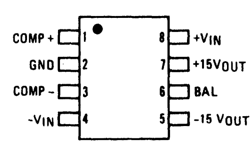
Order Part Nos.:
RC4195TK, RM4195TK

TE Metal Can Package
(Top View)



Order Part Nos.:
RC4195T, RM4195T

NB Dual In-line
(Top View)



Order Part No.:
RC4195NB

Note: The RM/RC4195 is available on special order in the DC (14-pin) ceramic package.

ABSOLUTE MAXIMUM RATINGS

Input Voltage ±V to Ground .... ±30V
Power Dissipation @ T_A = +25°C
 TK Package 2.4W
 T Package 800mW
 NB Package 600mW
Load Current
 TK Package 150mA
 T, and NB Package 100mA

Operating Junction Temperature Range
 RM4195 .... −55°C to +150°C
 RC4195 .... 0°C to +125°C
Storage Temperature Range
 RM4195 .... -65°C to +150°C
 RC4195 .... -65°C to +150°C
Lead Temperature (Soldering, 10s) .... +300°C

ELECTRICAL CHARACTERISTICS (I_L = 1mA, V_{CC} = ±20V, C_L = 10μF unless otherwise specified) (Note 1)

PARAMETER	CONDITIONS	RM4195			RC4195			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	V_{IN} = ±18 to ±30V		2	20		2	20	mV
Load Regulation	I_L = 1 to 100mA		5	30		5	30	mV
Output Voltage Temperature Stability			0.005	0.015		0.005	0.015	%/°C
Standby Current Drain	V_{IN} = ±30V, I_L = 0mA		±1.5	±2.5		±1.5	±3.0	mA
Input Voltage Range		18		30	18		30	V
Output Voltage	T_j = +25°C	14.8	15	15.2	14.5	15	15.5	V
Output Voltage Tracking			±50	±150		±50	±300	mV
Ripple Rejection	f = 120Hz, T_j = +25°C		75			75		dB
Input-Output Voltage Differential	I_L = 50mA	3			3			V
Short-Circuit Current	T_j = +25°C		220			220		mA
Output Noise Voltage	T_j = +25°C f = 100Hz to 10kHz		60			60		μV RMS
Internal Thermal Shutdown			175			175		°C

THERMAL CHARACTERISTICS

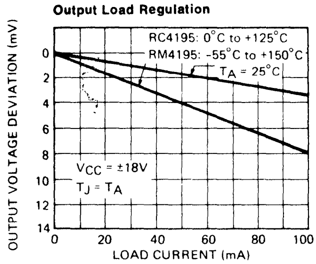
PARAMETER	CONDITIONS	PACKAGE			UNITS
		NB	T (TO-99)	TK (TO-66)	
Power Dissipation	T_A = 25°C	0.6	0.8	2.4	W
	T_C = 25°C		2.1	9	
Thermal Resistance	$\theta_{J\text{-}C}$		70	17	°C/W
	$\theta_{J\text{-}A}$	210	185	62	

NOTE:

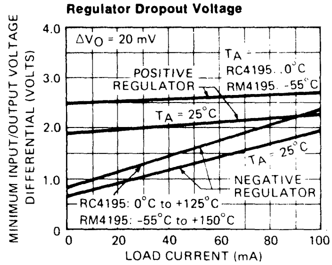
1. The specifications above apply for the given junction temperatures since pulse test conditions are used.

TYPICAL ELECTRICAL TEST DATA

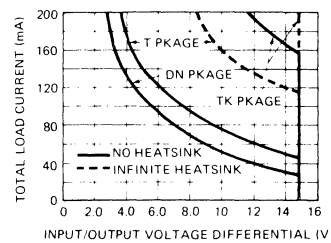
Output Load Regulation



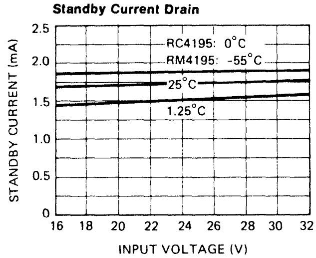
Regulator Dropout Voltage



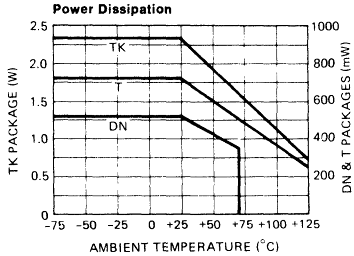
Maximum Current Capability



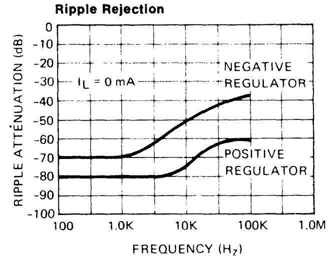
Standby Current Drain



Power Dissipation

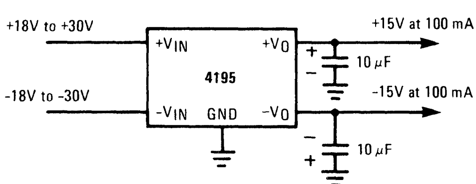


Ripple Rejection

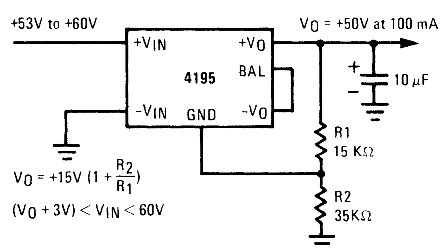


TYPICAL APPLICATIONS

Balanced Output (V_O = ±15V)



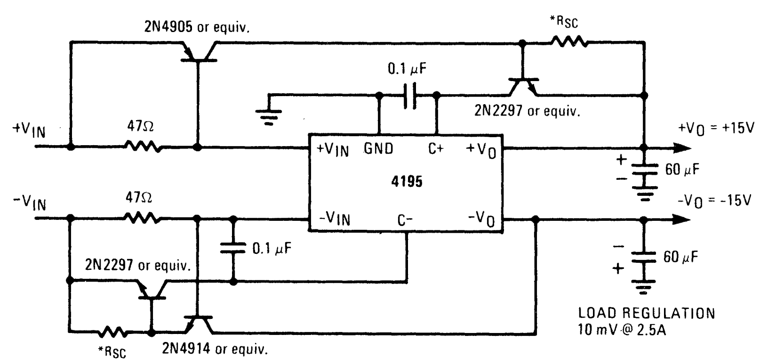
Positive Single Supply (+15V < V_O < +50V)



$V_O = +15V\ (1 + \frac{R_2}{R_1})$

$(V_O + 3V) < V_{IN} < 60V$

High Output Current



$*R_{SC} = \frac{0.7}{I_{SC}}$

COMPENSATION

For most applications, the compensation technique shown in the data sheet is sufficient. The positive regulator section of the 4194 is compensated by a 0.001µf ceramic disc capacitor from the C+ terminal to ground. The negative regulator requires compensation at two points. The first is the C- pin, which should have 0.001µf to the -Vin pin, or case. A ceramic disc is best here also. The second compensation point for the negative side is the -Vout terminal, which ideally should be a 4.7µf solid tantalum capacitor with enough reserve voltage capacity to avoid the momentary shorting and reforming which can occur with tantalum caps. For systems where the cost of a solid tantalum capacitor cannot be justified, it is usually sufficient to use an aluminum capacitor with a 0.03µf ceramic disc in parallel to bypass high frequencies. In addition, if the rectifier filter capacitors have poor high frequency characteristics (like aluminum electrolytics) or if any impedance is in series with the +Vin and -Vin terminals, it is necessary to bypass these two points with 0.01µf ceramic disc capacitors. Just as with monolithic op-amps, some applications may not require these bypass caps, but if in doubt, be sure to include them.

All compensation and bypass caps should have short leads, solid grounds, and be located as close to the RM/RC4194 as possible. Refer to Figure 1 for recommended compensation circuitry.

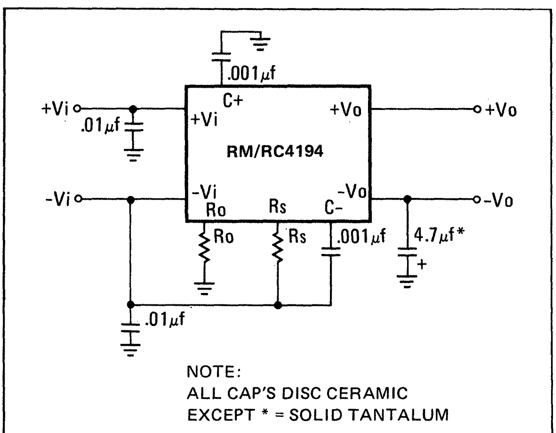


Figure 1. 4194 Recommended Compensation

PROTECTION

In systems using monolithic voltage regulators, a number of conditions can exist which, left uncorrected, will destroy the regulator. Fortunately, regulators can easily be protected against these potentially destructive conditions. Monolithic regulators can be destroyed by any reversal of input or output voltage polarity, or if the input voltage drops below the output voltage in magnitude. These conditions can be caused by inductive loads at the inputs or outputs of the regulator. Other problems are caused by heavy loads at the unregulated inputs to the regulator, which might cause the input voltage to drop below the output voltage at turn-off. If any of the preceding problem conditions are present in your system, it is recommended that you protect the regulator using diodes. These diodes should be high speed types capable of handling large current surges. Figure 2 shows all six of the possible protection diodes. The diodes at the inputs and outputs prevent voltages at those points from becoming reversed. Diodes from outputs to inputs prevent the output voltage from exceeding the input voltage. Chances are that the system under consideration will not require all six diodes, but if in doubt, be sure to include them.

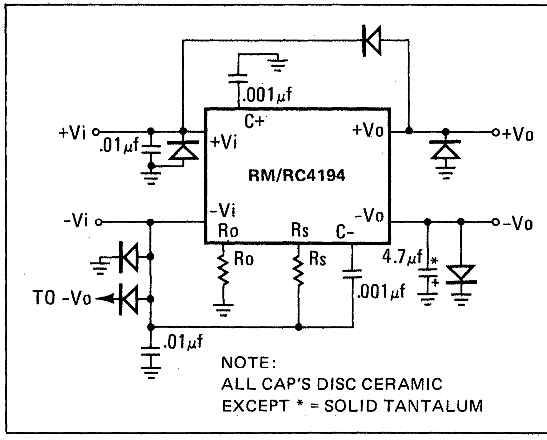


Figure 2. 4194 Regulator Showing all Protective Diodes

BROWNOUT PROTECTION

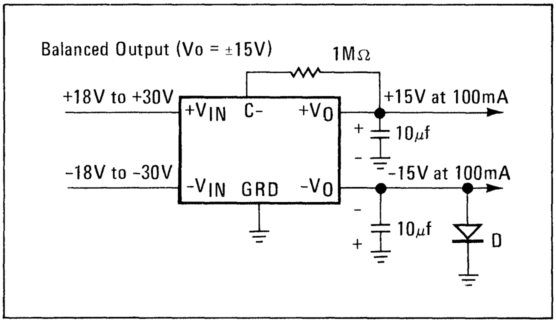
The RM/RC4195 is one of the most easily applied and trouble-free monolithic IC's available. When used within the data sheet ratings (package power dissipation, maximum output current, minimum and maximum input voltages) it provides the most cost-effective source of regulated ±15 volts for powering linear IC's.

Sometimes occasions arise in which the RM/RC4195 ratings must be exceeded. One example is the "brownout." During a brownout, line voltages may be reduced to as low as 75VRMS, causing the input voltage to the RM/RC4195 to drop below the ±18 V DC minimum. When this happens, the negative output voltage can go positive. Refer to the schematic diagram on pg. to see how this happens.

When the positive input voltage drops below +18V, the PNP current source can saturate, causing current, I, to drop to zero. This removes all drive from the negative pass transistor, Q_1. The negative output is then free to be pulled positive by resistors R_1, R_2, and R_3. The total value of $R_1 + R_2 + R_3$ is 30K ohms, so the maximum amount of current available is approximately 5mA.

In general, this is not enough current to damage most IC's which the 4195 might be supplying, but it is a potentially destructive condition. Fortunately, it is easy to protect against. As shown in the typical application circuit below, a diode, D, can be connected to the negative output.

If a small signal silicon diode is used, it will clamp the negative output voltage at about +0.55V. A Schottky barrier or germanium device would clamp the voltage at about +0.3V. Another cure which will keep the negative output negative at all times is the 1Mohm resistor connected between the +15V output and the C- terminal. This resistor will then supply drive to the negative output transistor, Q_1, causing it to saturate to $-V_1$ during the brownout.



HEATSINKING FOR 4194 AND 4195

Voltage Regulators are power devices which are used in a wide range of applications.

When operating these devices near their extremes of load current, ambient temperature and input-output differential, consideration of package dissipation becomes important to avoid thermal shutdown at 175°C. Both the 4194 and 4195 have this feature to prevent damage to the device. It typically starts affecting load regulation approximately 2°C below 175°C. *To avoid shutdown, some form of heatsinking should be used or one of the above operating conditions would need to be derated.

The following is the basic equation for junction temperature:

$$T_j = T_A + P_D\,\theta_{j\text{-}A} \qquad (1)$$

where T_j = junction temperature (°C)
T_A = ambient air temperature (°C)
P_D = power dissipated by device (W)
$\theta_{j\text{-}A}$ = thermal resistance from junction to ambient air (°C/W)

The power dissipated by the voltage regulator can be detailed as follows:

$$P_D = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q \qquad (2)$$

where V_{IN} = input voltage
V_{OUT} = regulated output voltage
I_O = load current
I_Q = quiescent current drain

*In allowing for process deviations, the user should work with a maximum allowable function temperature of 150°C.

Let's look at an application where a user is trying to determine whether the RM4194 in a high temperature environment will need a heatsink.

Given: T_j at thermal shutdown = 150°C
T_A = 125°C
$\theta_{j\text{-}A}$ = 41.6°C/W, TK (TO-66) pkg. (see data sheet)

V_{IN} = 40V
V_{OUT} = 30V
I_Q = 1mA + 75µA/V_{OUT} x 30V = 3.25mA (1)

$$\theta_{j\text{-}A} = \frac{T_j - T_A}{P_D}$$

$$P_D = \frac{T_j - T_A}{\theta_{jA}} = (V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q$$

Solve for I_O,

$$I_O = \frac{T_j - T_A}{\theta_{j\text{-}A}\,(V_{IN} - V_{OUT})} - \frac{V_{IN} \times I_Q}{(V_{IN} - V_{OUT})}$$

$$I_O = \frac{50°C - 125°C}{41.6°C/W \times 10V} - \frac{40 \times 3.25 \times 10^{-3}}{10}$$

$$= 50mA - 13mA \simeq 47mA$$

If this supply current does not provide at least a 10% margin under worst case load conditions, heatsinking should be employed. If reliability is of prime importance, the multiple regulator approach should be considered.

In equation 1, $\theta_{j\text{-}A}$ can be broken into the following components:

$$\theta_{j\text{-}A} = \theta_{j\text{-}c} + \theta_{c\text{-}s} + \theta_{s\text{-}A}$$

where $\theta_{j\text{-}c}$ = junction-to-case thermal resistance
$\theta_{c\text{-}s}$ = case-to-heatsink thermal resistance
$\theta_{s\text{-}A}$ = heatsink-to-ambient thermal resistance

In the above example, let's say that the user's load current is 200mA and he wants to calculate the combined $\theta_{c\text{-}s}$ and $\theta_{s\text{-}A}$ he needs:

Given: I_O = 200mA,

$$\theta_{j\text{-}A} = \frac{T_j - T_A}{(V_{IN} - V_{OUT}) \times I_O + V_{IN} \times I_Q}$$

$$= \frac{50°C - 125°C}{10V \times 200mA + 40 \times 3.25 \times 10^{-3}}$$

$$= 11.75°C/W$$

(1) See note 1 of 4194 data sheet.

Given: θ_{j-c} = 7.15°C/W for the 4194 in the TK package,

$\theta_{c-s} + \theta_{s-A}$ = 11.75°C/W - 7.15°C/W = 4.6°C/W

When using heatsink compound with a metal-to-metal interface, a typical θ_{c-s} = 0.5°C/W for the TK package. The remaining θ_{s-A} of approximately 4°C/W is a large enough thermal resistance to be easily provided by a number of heatsinks currently available. Table 1 is a brief selection guide to heatsink manufacturers.

TABLE 1
Commercial Heatsink Selection Guide

No attempt has been made to provide a complete list of all heatsink manufacturers. This list is only representative.

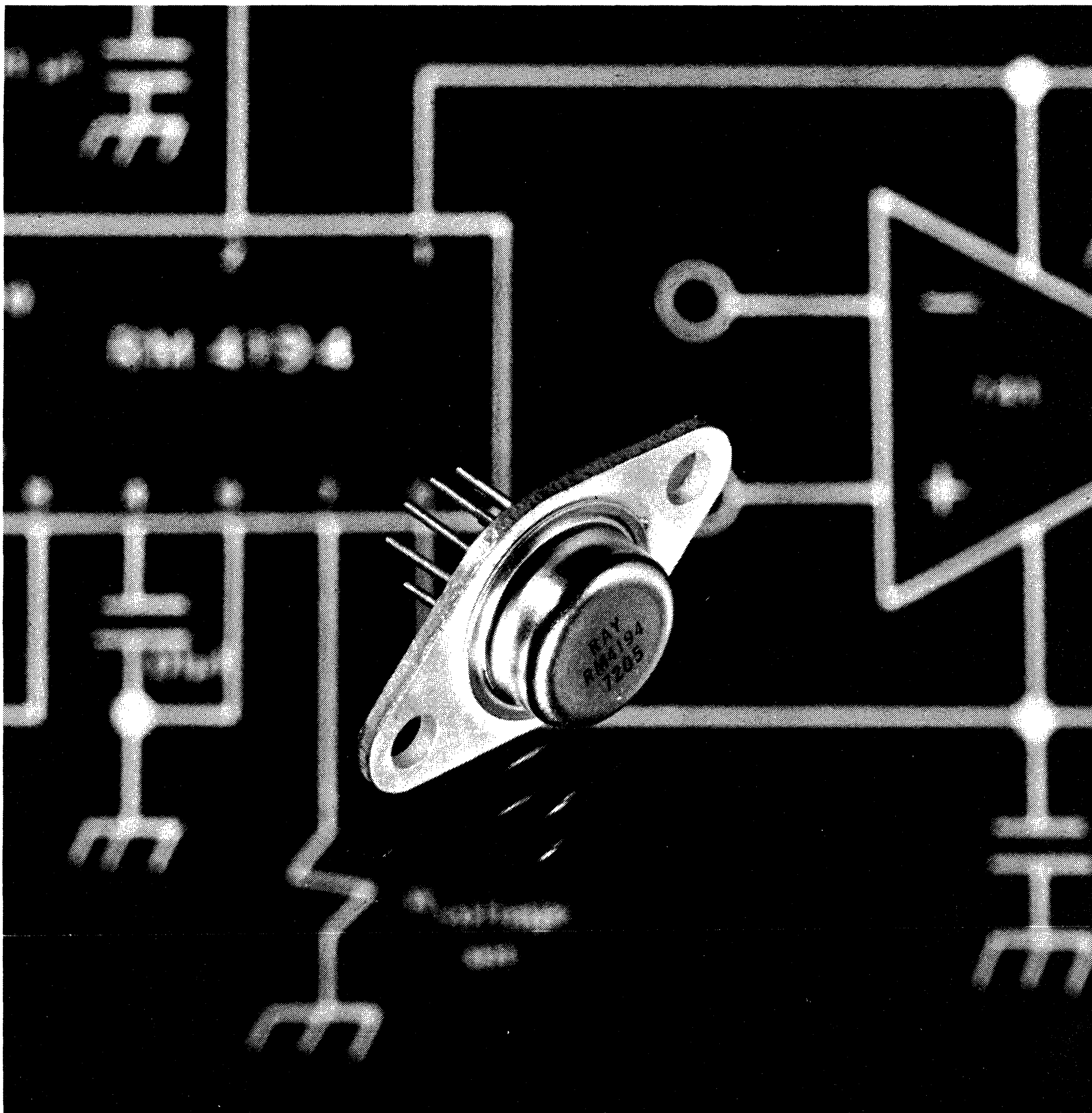
TO-3 AND TO-66	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
0.3-1.0	Thermalloy – 6441, 6443, 6450, 6470, 6560, 6590, 6660, 6690
1.0-3.0	Wakefield – 641 Thermalloy – 6123, 6135, 6169, 6306, 6401, 6403, 6421, 6423, 6427, 6442, 6463, 6500
3.0-5.0	Wakefield – 621, 623 Thermalloy – 6606, 6129, 6141, 6303 IERC – HP Staver – V3-3-2
5.0-7.0	Wakefield – 690 Thermalloy – 6002, 6003, 6004, 6005, 6052, 6053, 6054, 6176, 6301 IERC – LB Staver – V3-5-2
7.0-10.0	Wakefield – 672 Thermalloy – 6001, 6016, 6051, 6105, 6601 IERC – LA, uP Staver – V1-3, V1-5, V3-3, V3-5, V3-7
10.0-25.0	Thermalloy – 6013, 6014, 6015, 6103, 6104, 6105, 6117
TO-99	
12.0-20.0	Wakefield – 260 Thermalloy – 1101, 1103 Staver – V3A-5
20.0-30.0	Wakefield – 209 Thermalloy – 1116, 1121, 1123, 1130, 1131, 1132, 2227, 3005 IERC – LP Staver – F5-5
30.0-50.0	Wakefield – 207 Thermalloy – 2212, 2215, 225, 2228, 2259, 2263, 2264 Staver – F5-5, F6-5
	Wakefield – 204, 205, 208 Thermalloy – 1115, 1129, 2205, 2207, 2209, 2210, 2211, 2226, 2230, 2257, 2260, 2262 Staver – F1-5, F5-5
CASE 199, CASE 313	
10.0-15.0	Thermalloy – 6030, 6032, 6034 Staver – V4-3-192, V-5-1
15.0-20.0	Thermalloy – 6106 Staver – V4-3-128, V6
20.0-30.0	Wakefield – 295 Thermalloy – 6025, 6107

TABLE 1 Commercial Heatsink Selection Guide (Cont.)

DUAL-INLINE-PIN ICS	
θ_{SA}*(°C/W)	Manufacturer/Series or Part Number
20	Thermalloy – 6007
30	Thermalloy – 6010
32	Thermalloy – 6011
34	Thermalloy – 6012
45	IERC – LIC
60	Wakefield – 650, 651

*All values are typical as given by mfgr. or as determined from characteristic curves supplied by manufacturer.

Staver Co., Inc.: 41-51 N. Saxon Ave., Bay Shore, NY 11706
IERC: 135 W. Magnolia Blvd., Burbank, CA 91502
Thermalloy: P.O. Box 34829, 2021 W. Valley View Ln., Dallas, TX
Wakefield Engin Ind: Wakefield, MA 01880


RAY
RM4194
7205

SECTION 4

Voltage References

CONTENTS

RAYTHEON

GENERAL DESCRIPTION

The LM129 and LM329 family are precision multicurrent temperature compensated 6.9V zener references with dynamic impedances a factor of 10 to 100 less than discrete diodes. Constructed in a single silicon chip, the LM129 uses active circuitry to buffer the internal zener allowing the device to operate over a 0.5mA to 15mA range with virtually no change in performance. The LM129 and LM329 are available with selected temperature coefficients of 0.001, 0.002, 0.005 and 0.01%/°C. These new references also have excellent long term stability and low noise.

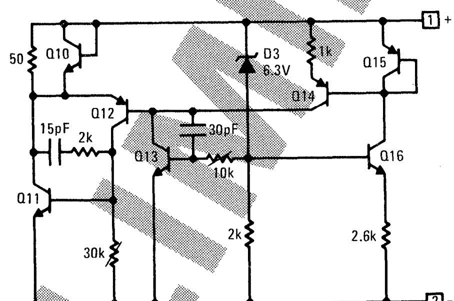
A new subsurface breakdown zener used in the LM129 gives lower noise and better long term stability than conventional IC zeners. Further the zener and temperature compensating transistor are made by a planar process so they are immune to problems that plague ordinary zeners. For example, there is virtually no voltage shifts in zener voltage due to temperature cycling and the device is insensitive to stress on the leads. The LM129 can be used in place of conventional zeners with improved performance. The low dynamic impedance simplifies biasing and the wide operating current allows the replacement of many zener types.

The LM129 is packaged in a 2-lead TO-46 package and is rated for operation over a -55°C to +125°C temperature range. The LM329 for operation over 0–70°C is available in both a hermetic TO-46 package and a TO-92 epoxy package.

DESIGN FEATURES

- 0.6mA to 15mA operating current
- 0.6Ω dynamic impedance at any current
- Available with temperature coefficients of 0.001%/°C
- 7μV wideband noise
- 5% initial tolerance
- 0.002% long term stability
- Low cost

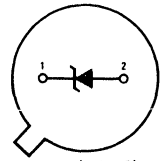
SCHEMATIC DIAGRAMS



Reference

CONNECTION INFORMATION

Metal Can Package
(Bottom View)



TR (TO-46)

Order Part Nos.:
LM129AH, LM129BH,
LM129CH, LM329BH,
LM329CH or LM329DH

ABSOLUTE MAXIMUM RATINGS

Reverse Breakdown Current	30mA
Forward Current	2mA
Operating Temperature Range	
LM129	-55°C to +125°C
LM329	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (Note 1)

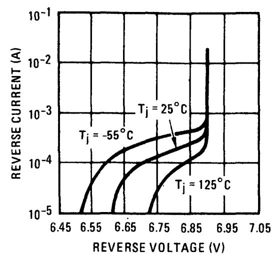
PARAMETER	CONDITIONS	LM129A, B, C			LM329B, C, D			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reverse Breakdown Voltage	$T_A = 25°C$, $0.6mA \leqslant I_R \leqslant 15mA$	6.7	6.9	7.2	6.55	6.9	7.25	V
Reverse Breakdown Change with Current	$T_A = 25°C$, $0.6mA \leqslant I_R \leqslant 15mA$		9	14		9	20	mV
Reverse Dynamic Impedance	$T_A = 25°C$, $I_R = 1mA$		0.6	1		0.8	2	Ω
RMS Noise	$T_A = 25°C$, $10\ Hz \leqslant F \leqslant 10\ kHz$		7	20		7	100	μV
Long Term Stability	$T_A = 45°C \pm 0.1°C$, $I_R = 1mA \pm 0.3\%$		20			20		ppm
Temperature Coefficient	$I_R = 1mA$							
LM129A			6	10				ppm/°C
LM129B, LM329B			15	20		15	20	
LM129C, LM329C			30	50		30	50	
LM329D						50	100	
Change In Reverse Breakdown Temperature Coefficient	$1mA \leqslant I_R \leqslant 15mA$		1			1		ppm/°C
Reverse Breakdown Change with Current	$1mA \leqslant I_R \leqslant 15mA$		12			12		mV
Reverse Dynamic Impedance	$1mA \leqslant I_R \leqslant 15mA$		0.8			1		Ω

NOTE:

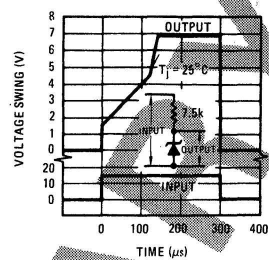
1. These specifications apply for $-55°C \leqslant T_A \leqslant +125°C$ for the LM129 and $0°C \leqslant T_A \leqslant +70°C$ for the LM329 unless otherwise specified.

TYPICAL PERFORMANCE CHARACTERISTICS

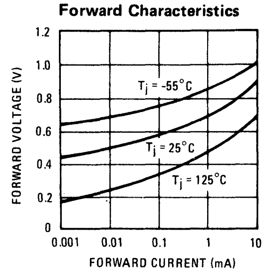
Reverse Characteristics



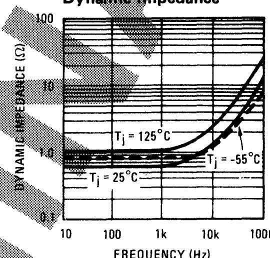
Response Time



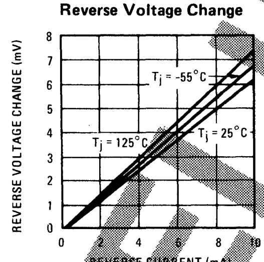
Forward Characteristics



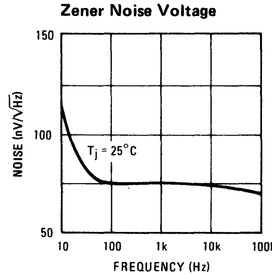
Dynamic Impedance



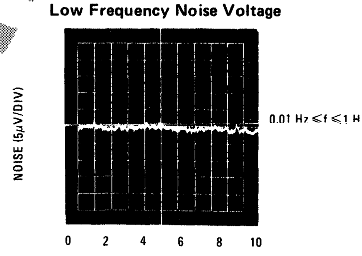
Reverse Voltage Change



Zener Noise Voltage



Low Frequency Noise Voltage



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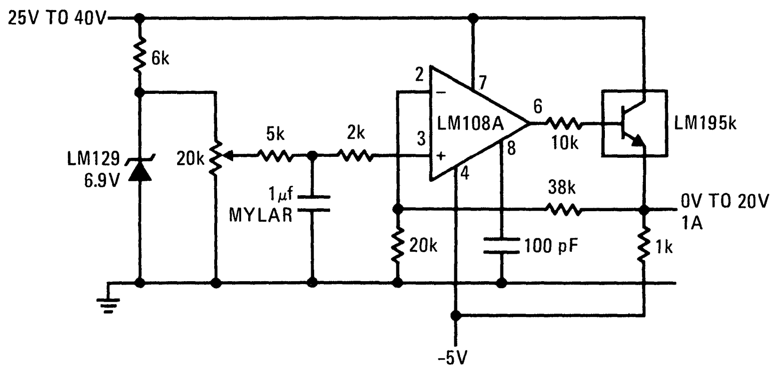
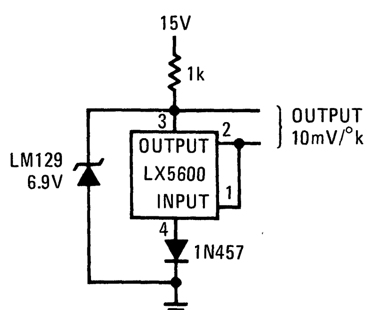
TYPICAL APPLICATIONS

0V to 20V Power Reference

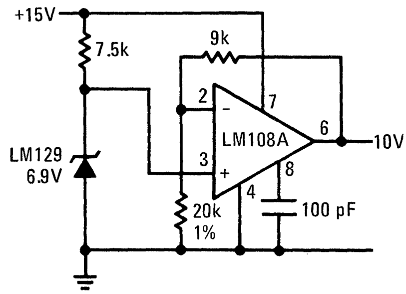


External Reference for Temperature Transducer

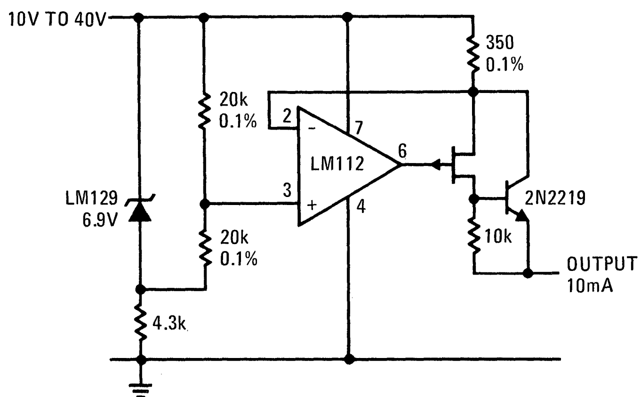


TYPICAL APPLICATIONS (Cont.)

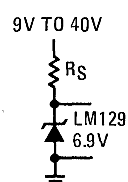
Buffered Reference with Single Supply



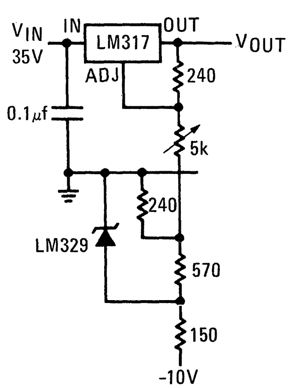
Positive Current Source



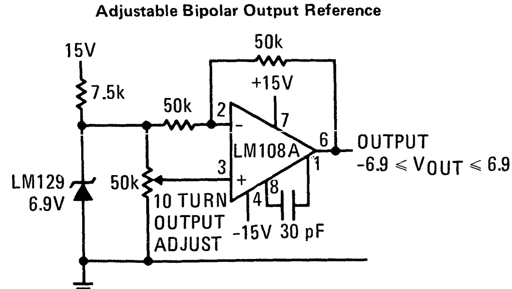
Simple Reference



Low Cost 0-25V Regulator



Adjustable Bipolar Output Reference



GENERAL DESCRIPTION

The LM199/LM399 are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5mA to 10mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

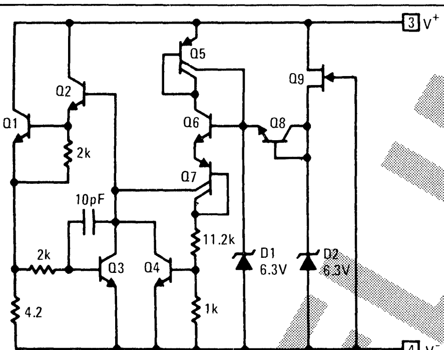
The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from -55°C to +125°C while the LM299 is rated for operation from -25°C to +85°C and the LM399 is rated from 0°C to +70°C.

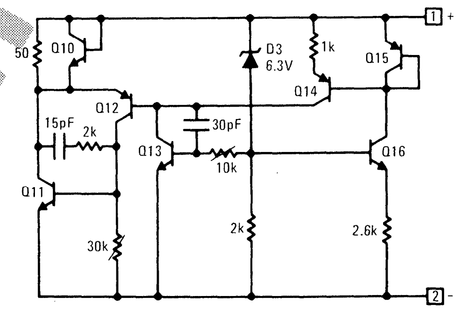
DESIGN FEATURES

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400μA
- Wide operating current — 500μA to 10mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300mW at 25°C
- Long term stability — 20 ppm

SCHEMATIC DIAGRAMS



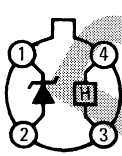
Temperature Stabilizer



Reference

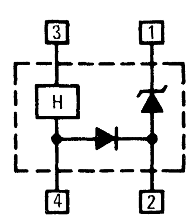
CONNECTION INFORMATION

TT (TO-46)
Metal Can Package
(Top View)



Order Part Nos.:
LM199H, LM299H
or LM399H

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Temperature Stabilizer Voltage 40V
Reverse Breakdown Current 20mA
Forward Current 1mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1) . . . . +40V
-0.1V

Operating Temperature Range
LM199 . . . . -55°C to +125°C
LM299 . . . . -25°C to +85°C
LM399 . . . . 0°C to +70°C
Storage Temperature Range . . . . -55°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS (Note 2)

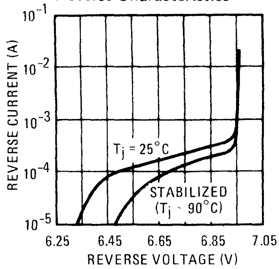
PARAMETER	CONDITIONS		LM199, LM299 MIN	LM199, LM299 TYP	LM199, LM299 MAX	LM399 MIN	LM399 TYP	LM399 MAX	UNITS
Reverse Breakdown Voltage	$0.5mA \leqslant I_R \leqslant 10mA$		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5mA \leqslant I \leqslant 10mA$			6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1mA$			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \leqslant T_A \leqslant 85°C$	LM199		0.00003	0.0001				%/°C
	$85°C \leqslant T_A \leqslant 125°C$	LM199		0.0005	0.0015				
	$-25°C \leqslant T_A \leqslant 85°C$	LM299		0.00003	0.0001				
	$0°C \leqslant T_A \leqslant 70°C$	LM399					0.00003	0.0002	
RMS Noise	$10\ Hz \leqslant f \leqslant 10\ kHz$			7	20		7	50	μV
Long Term Stability	Stabilized, $22°C \leqslant T_A \leqslant 28°C$, 1000 Hours, $I_R = 1mA \pm 0.1\%$			20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$			8.5	14		8.5	15	mA
	$T_A = -55°C$			22	28				mA
Temperature Stabilizer Supply Voltage (Note 3)			9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$			3			3		Seconds
Initial Turn-on Current	$9 \leqslant V_S \leqslant 40$, $T_A = 25°C$			140	200		140	200	mA

NOTES:

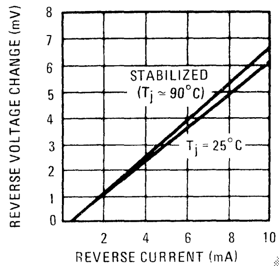
1. The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.
2. These specifications apply for 30V applied to the temperature stabilizer and $-55°C \leqslant T_A \leqslant +125°C$ for the LM199; $-25°C \leqslant T_A \leqslant +85°C$ for the LM299 and $0°C \leqslant T_A \leqslant +70°C$ for the LM399.
3. CAUTION. If the device is operated for more than 60 seconds with heater supply voltage between 2V and 9V the heater temperature control circuitry is not properly biased and the device can rise to approximately +150°C.

TYPICAL PERFORMANCE CHARACTERISTICS

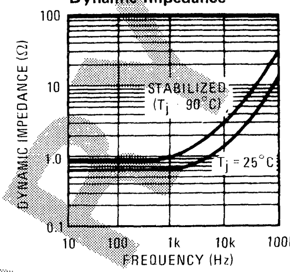
Reverse Characteristics



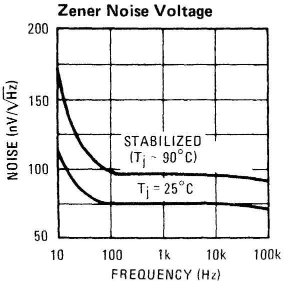
Reverse Voltage Change



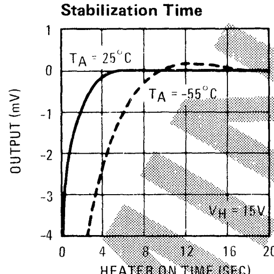
Dynamic Impedance



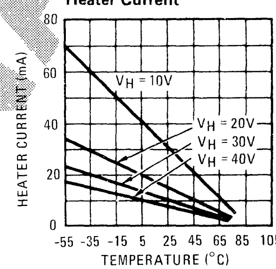
Zener Noise Voltage



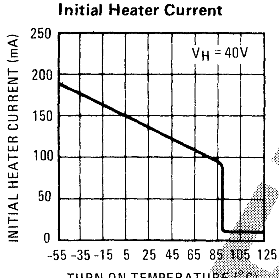
Stabilization Time



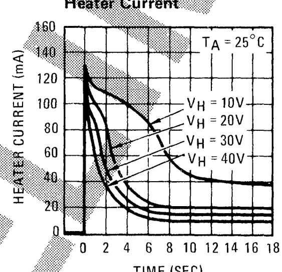
Heater Current



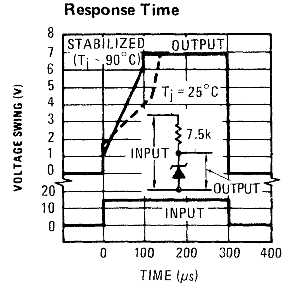
Initial Heater Current



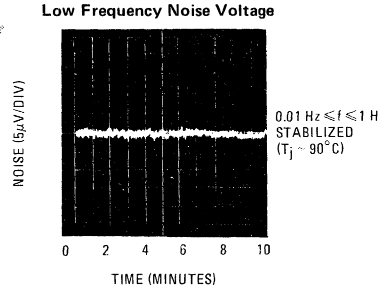
Heater Current



Response Time

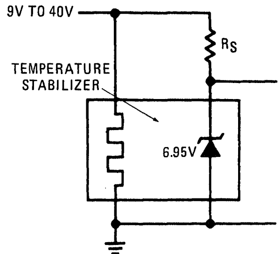


Low Frequency Noise Voltage

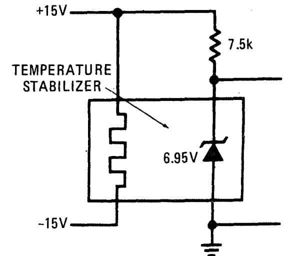


TYPICAL APPLICATIONS

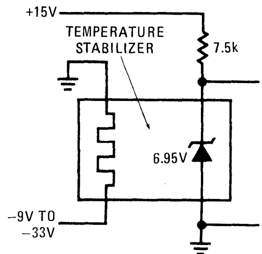
Single Supply Operation



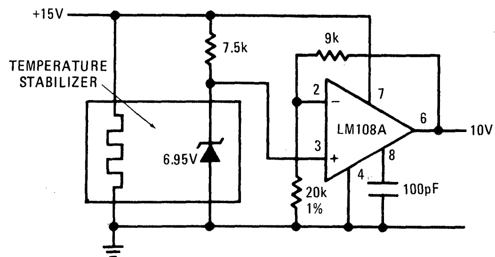
Split Supply Operation



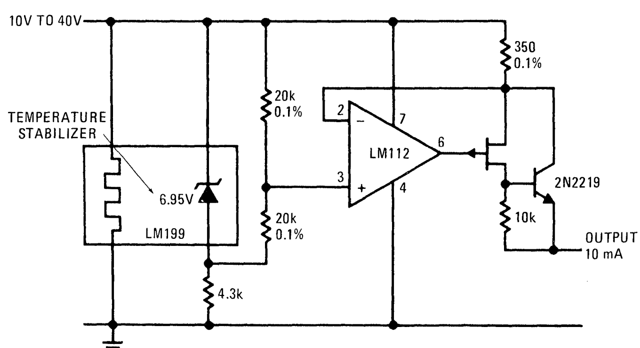
Negative Heater Supply with Positive Reference



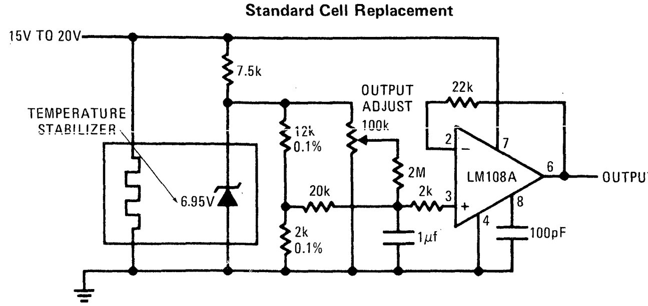
Buffered Reference with Single Supply



Positive Current Source



Standard Cell Replacement



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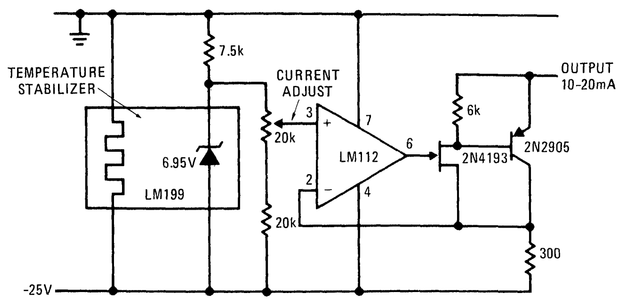
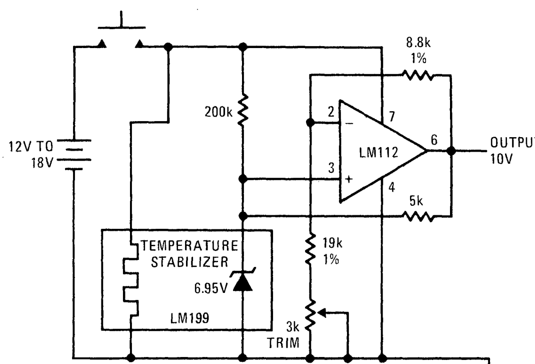
TYPICAL APPLICATIONS (Cont.)

Negative Current Source

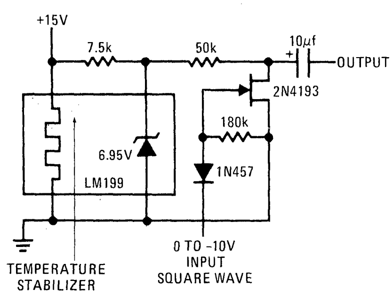


Portable Calibrator*

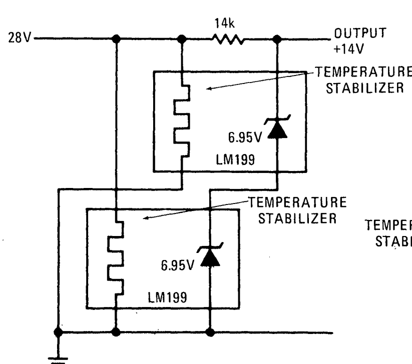


*Warm-up time 10 seconds; intermittant operation does not degrade long term stability.

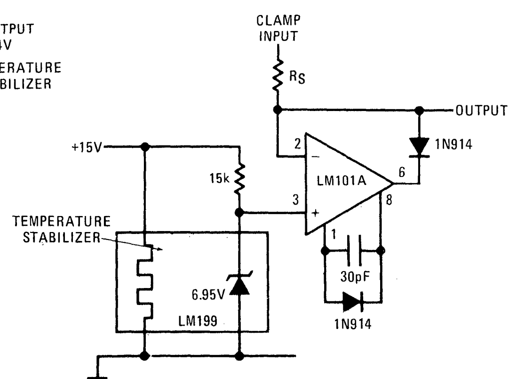
Square Wave Voltage Reference



14V Reference



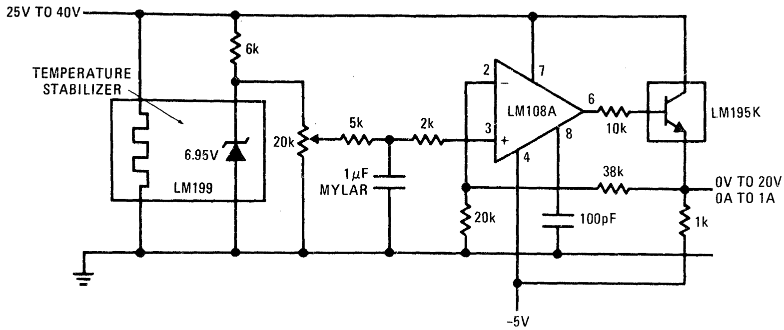
Precision Clamp*



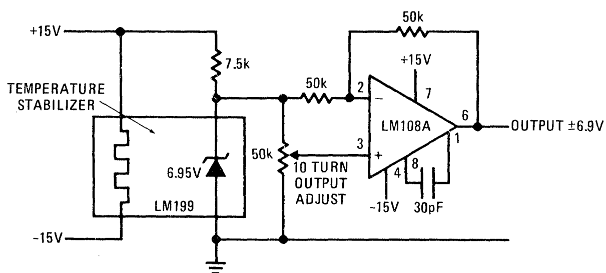
*Clamp will sink 5mA when input goes more positive than reference.

TYPICAL APPLICATIONS (Cont.)

0V to 20V Power Reference



Bipolar Output Reference



RAYTHEON

GENERAL DESCRIPTION

The LM199A/LM299A/LM399A are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5mA to 10mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199A series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199A is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

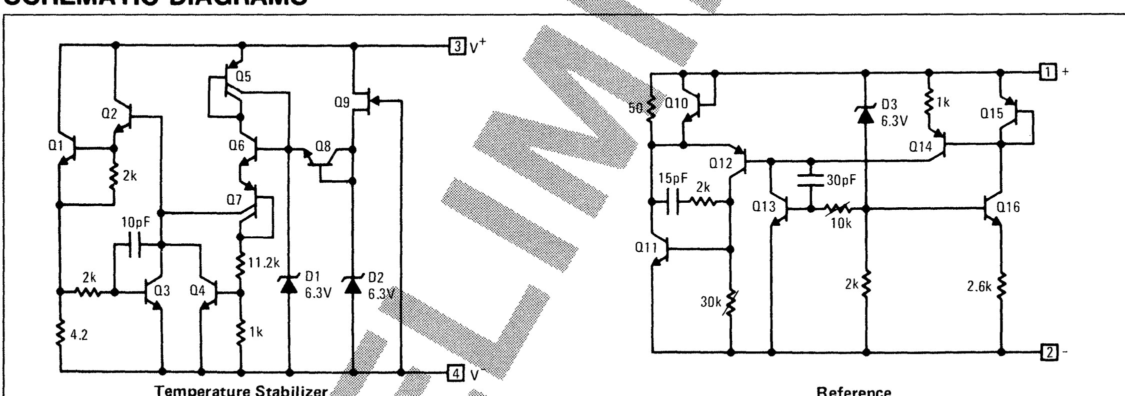
The LM199A can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199A can replace references in existing equipment with a minimum of wiring changes.

The LM199A series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from -55°C to +125°C while the LM299A is rated for operation from -25°C to +85°C and the LM399A is rated from 0°C to +70°C.

DESIGN FEATURES

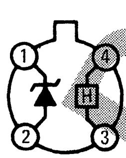
- Guaranteed 0.00005%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400μA
- Wide operating current — 500μA to 10mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300mW at 25°C
- Long term stability — 20 ppm

SCHEMATIC DIAGRAMS



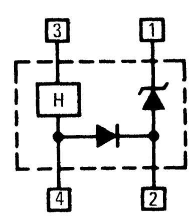
CONNECTION INFORMATION

TT (TO-46) Metal Can Package
(Top View)



Order Part Nos.:
LM199AH, LM299AH
or LM399AH

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Temperature Stabilizer Voltage 40V
Reverse Breakdown Current 20mA
Forward Current 1mA
Reference to Substrate Voltage $V_{(RS)}$ (Note 1) 40V
-0.1V

Operating Temperature Range
- LM199A . . . . -55°C to +125°C
- LM299A . . . . -25°C to +85°C
- LM399A . . . . 0°C to +70°C

Storage Temperature Range . . . . -55°C to +150°C
Lead Temperature (Soldering, 10 seconds) . . . . 300°C

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LM199A/LM299A MIN	LM199A/LM299A TYP	LM199A/LM299A MAX	LM399A MIN	LM399A TYP	LM399A MAX	UNITS
Reverse Breakdown Voltage	$0.5mA \leq I_R \leq 10mA$		6.8	6.95	7.1	6.6	6.95	7.3	V
Reverse Breakdown Voltage Change With Current	$0.5mA \leq I \leq 10mA$			6	9		6	12	mV
Reverse Dynamic Impedance	$I_R = 1mA$			0.5	1		0.5	1.5	Ω
Reverse Breakdown Temperature Coefficient	$-55°C \leq T_A \leq 85°C$	LM199A		0.00002	0.00005				%/°C
	$85°C \leq T_A \leq 125°C$	LM199A		0.0005	0.0010				
	$-25°C \leq T_A \leq 85°C$	LM299A		0.00002	0.00005				
	$0°C \leq T_A \leq 70°C$	LM399A					0.00003	0.0001	
RMS Noise	$10 Hz \leq f \leq 10 kHz$			7	20		7	50	µV
Long Term Stability	Stabilized, $22°C \leq T_A \leq 28°C$, 1000 Hours, $I_R = 1mA \pm 0.1\%$			20			20		ppm
Temperature Stabilizer Supply Current	$T_A = 25°C$, Still Air, $V_S = 30V$			8.5	14		8.5	15	mA
	$T_A = -55°C$			22	28				mA
Temperature Stabilizer Supply Voltage (Note 3)			9		40	9		40	V
Warm-Up Time to 0.05%	$V_S = 30V$, $T_A = 25°C$			3			3		Seconds
Initial Turn-on Current	$9 \leq V_S \leq 40$, $T_A = 25°C$			140	200		140	200	mA

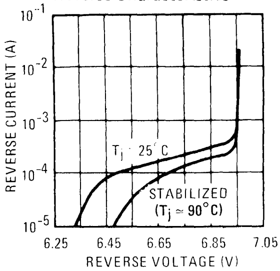
NOTES:
1. The substrate is electrically connected to the negative terminal of the temperature stabilizer. The voltage that can be applied to either terminal of the reference is 40V more positive or 0.1V more negative than the substrate.
2. These specifications apply for 30V applied to the temperature stabilizer and $-55°C \leq T_A \leq +125°C$ for the LM199A; $-25°C \leq T_A \leq +85°C$ for the LM299A and $0°C \leq T_A \leq +70°C$ for the LM399A.
3. CAUTION. If the device is operated for more than 60 seconds with heater supply voltage between 2V and 9V the heater temperature control circuitry is not properly biased and the device can rise to approximately +150°C.

TYPICAL APPLICATIONS

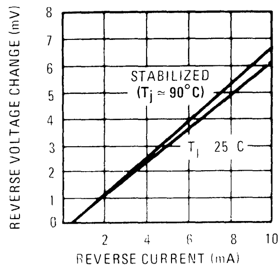
For typical applications, see 199 data sheet beginning on page 4-7.

TYPICAL PERFORMANCE CHARACTERISTICS

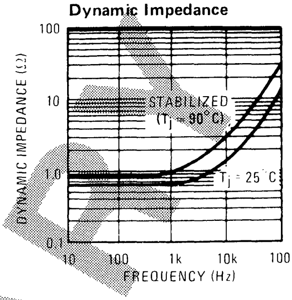
Reverse Characteristics



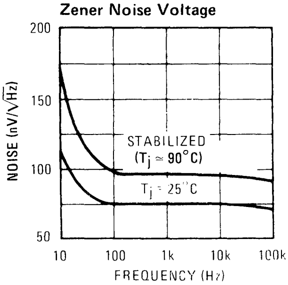
Reverse Voltage Change



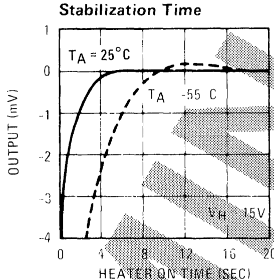
Dynamic Impedance



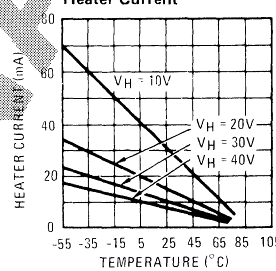
Zener Noise Voltage



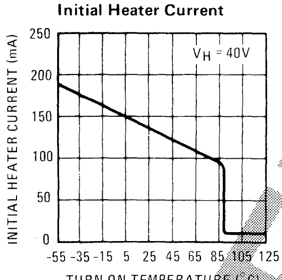
Stabilization Time



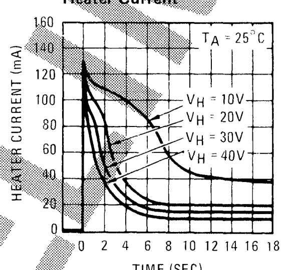
Heater Current



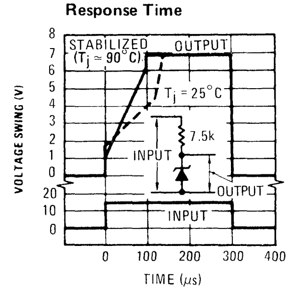
Initial Heater Current



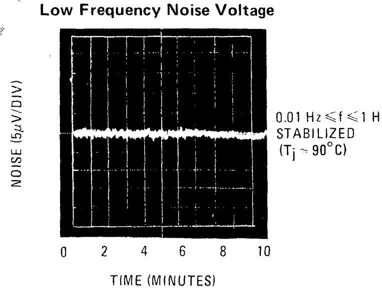
Heater Current

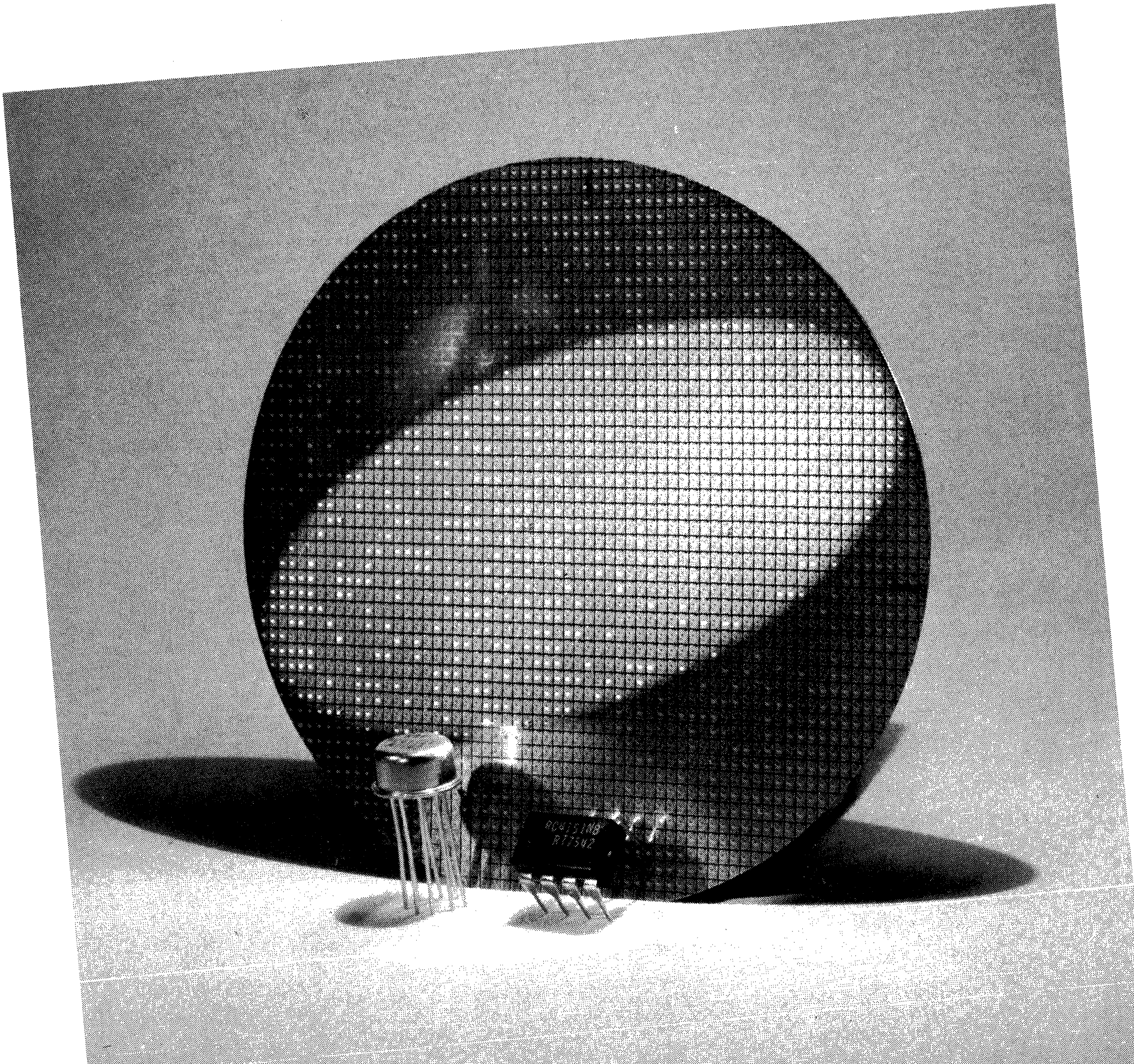


Response Time



Low Frequency Noise Voltage





RAYTHEON

SECTION 5

Comparators

CONTENTS

GENERAL DESCRIPTION

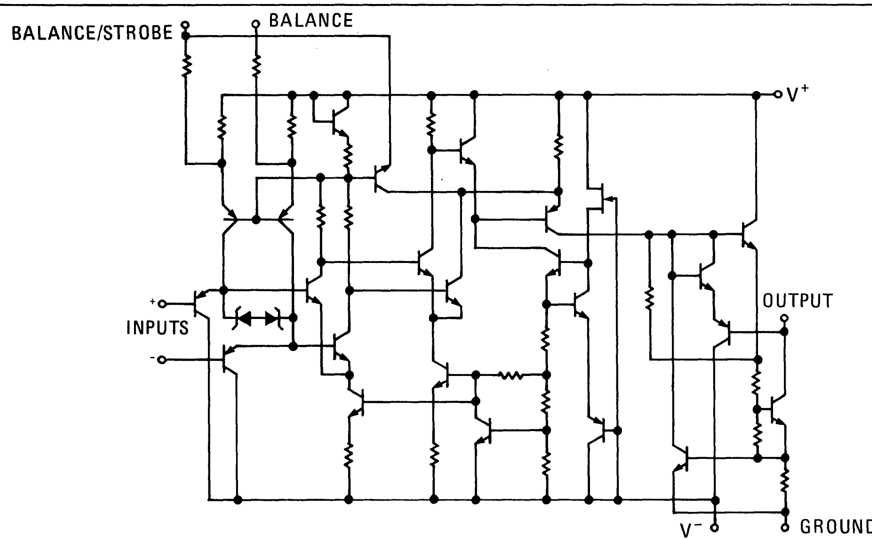
The LM111, LM211, and LM311 are voltage comparators with about one-thousandth the input current of the LM106 and LM107. These comparators are designed to operate from standard ±15V operational amplifier supplies to a single +5V supply used for IC logic. Their outputs are compatible with DTL, RTL, TTL, and MOS devices. Offset balancing is provided, and the outputs can be OR wired.

The LM111 operates over the full military temperature range of −55°C to +125°C. The LM211 is the same as the LM111 except its performance is guaranteed from −25°C to +85°C. The LM311 is the commercial version which operates from 0°C to +70°C.

DESIGN FEATURES

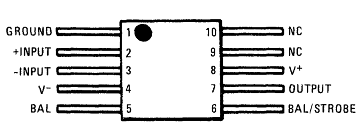
- Input Current 150nA Maximum
- Operates from +5V Supply
- Offset Current 20nA Maximum

SCHEMATIC DIAGRAM



CONNECTION INFORMATION

CQ Flat Pack Package
(Top View)

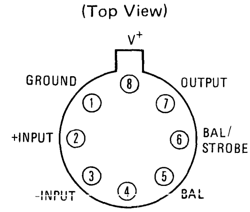


NOTE: Pin 4 connected to case.

Order Part No.:
LM111F

Note: The LM111 and LM311 are available on special order in the DC (14 pin) ceramic package.

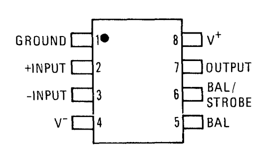
TE Metal Can Package
(Top View)



NOTE: Pin 4 connected to case.

Order Part Nos.:
LM111H, LM211H,
LM311H

DE and NB Dual In-line Package
(Top View)



Order Part Nos.:
LM111DE, LM211DE,
LM311DE, LM311N

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_{84})	36V
Output to Negative Supply (V_{74}) LM111/LM211	50V
LM311	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500mW
Output Short-Circuit Duration	10s
Operating Temperature Range	
LM111	−55°C to +125°C
LM221	−25°C to +85°C
LM311	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10s)	300°C

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LM111/211		LM311		UNITS
		TYP	MAX	TYP	MAX	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leqslant 50k$	0.7	3.0	2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$	4.0	10	6.0	50	nA
Input Bias Current	$T_A = 25°C$	60	100	100	250	nA
Voltage Gain	$T_A = 25°C$	200		200		V/mV
Response Time (Note 5)	$T_A = 25°C$	200		200		ns
Saturation Voltage	$V_{IN} \leqslant -5mV$, $I_{OUT} = 50mA$, $T_A = 25°C$	0.75	1.5	0.75	1.5	V
Strobe On Current	$T_A = 25°C$	3.0		3.0		mA
Output Leakage Current	$V_{IN} \geqslant 5mV$, $V_{OUT} = 35V$, $T_A = 25°C$	0.2	10	0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leqslant 50k$		4.0		10	mV
Input Offset Current (Note 4)			20		70	nA
Input Bias Current			150		300	nA
Input Voltage Range		±14		±14		V
Saturation Voltage	$V^+ \geqslant 4.5V$, $V^- = 0$, $V_{IN} \leqslant -6mV$, $I_{SINK} \leqslant 8mA$	0.23	0.4	0.23	0.4	V
Output Leakage Current	$V_{IN} \geqslant 5mV$, $V_{OUT} = 35V$	0.1	0.5			μA
Positive Supply Current	$T_A = 25°C$	5.1	6.0	5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$	4.1	5.0	4.1	5.0	mA

NOTES:

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage of 30V below the positive supply, whichever is less.
2. The maximum junction temperature of the LM111 is 150°C, while that of the LM311 is +85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat pack, derate based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2 ounce copper conductors. The thermal resistance of the dual-in-line (DE) package is 100°C/W, junction to ambient.
3. These specifications apply for $V_S = \pm 15V$ and $-55°C \leqslant T_A \leqslant +125°C$, unless otherwise stated. With the LM311, however, all temperature specifications are limited to $0°C \leqslant T_A \leqslant +70°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

139 239 339
139A 239A 339A 2901 3302 Quad Single-Supply Comparators

GENERAL DESCRIPTION

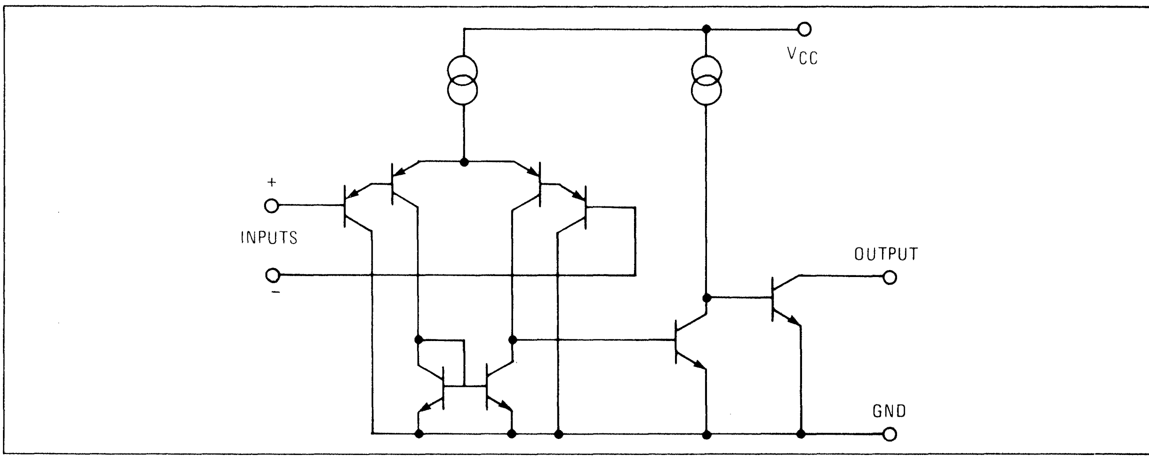
These devices offer higher frequency operation and faster switching than can be had from internally compensated quad op amps. Intended for single-supply applications, the Darlington PNP input stage allows them to compare voltages that include ground. The two-stage common-emitter output circuit provides gain and output sink capacity of 3.2mA at an output level of 400mV. The output collector is left open, permitting the designer to drive devices in the range of 2V to 36V.

They are intended for applications not needing response time less than 1 μs, but demanding excellent op amp input parameters of offset voltage and current, and bias current, to insure accurate comparison with reference voltage.

DESIGN FEATURES

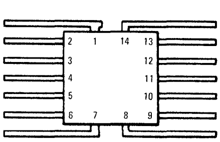
- Input Common Mode Voltage Range Includes Ground
- Wide Single Supply Voltage Range, 2 to 36V
- Output Compatible with TTL, DTL, ECL, MOS and CMOS Logic Systems
- Very Low Supply Current Drain (.8mA) Independent of Supply Voltage

SCHEMATIC DIAGRAM (1/4 shown)



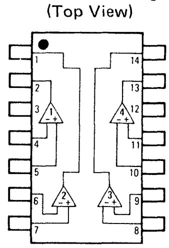
CONNECTION INFORMATION

CJ Flatpak
(Top View)



Order Part Nos.:
LM139F, LM139AF,
LM239F, LM239AF

DC and DB
Dual In-line Packages
(Top View)



Order Part Nos.:
LM139J, LM239J, LM339N, LM339J,
LM2901N, RC3302DB,
LM349AJ, LM239AJ, LM239AJ,
LM339AN

PIN	FUNCTION
1	OUTPUT 2
2	OUTPUT 1
3	V+
4	-INPUT 1
5	+INPUT 1
6	-INPUT 2
7	+INPUT 2
8	-INPUT 3
9	+INPUT 4
10	-INPUT 4
11	+INPUT 4
12	GROUND
13	OUTPUT 4
14	OUTPUT 3

ABSOLUTE MAXIMUM RATINGS

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage	36 V_{DC}	28 V_{DC}
Input Voltage	-0.3 V_{DC} to +36 V_{DC}	-0.3 V_{DC} to +28 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	800 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3$ V_{DC}), (Note 3)	50 mA	50 mA
Operating Temperature Range		-40°C to +85°C
LM339A	0°C to +70°C	
LM239A	-25°C to +85°C	
LM139A	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

ELECTRICAL CHARACTERISTICS ($V^+ = 5\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3	±20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $T_A = 25°C$, (Note 5)		25	100		25	250		25	100		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5	±50		±3	±100	nA_{DC}
Input Common-Mode Voltage Range	$T_A = 25°C$, (Note 6)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators, $T_A = 25°C$		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	1.0		0.8	2	mA_{DC}
	$R_L = \infty$, $V^+ = 30V$, $T_A = 25°C$														1	2.5				
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$ (To Support Large V_O Swing), $T_A = 25°C$	50	200		50	200			200			200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4\ V_{DC}$, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300			300			300			300			300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5\ V_{DC}$, $T_A = 25°C$	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		2.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = 25°C$		250	400		250	400		250	400		250	400			400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$, $T_A = 25°C$		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}
Input Offset Voltage	(Note 9)			4.0			4.0			9.0			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150			±100			±150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range		0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			V^+			V^+			36			36	0		V^+			V_{CC}	V_{DC}

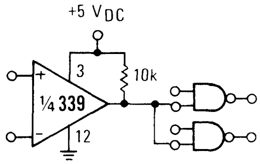
NOTES:

1. For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$.
4. These specifications apply for $V^+ = 5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+-1.5V$, but either or both inputs can go to $+30\ V_{DC}$ without damage.
7. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.
8. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used).
9. At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+-1.5\ V_{DC}$).
10. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

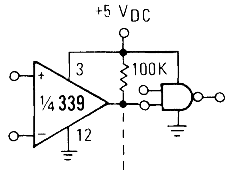
339 TYPICAL APPLICATIONS

Single Supply ($V^+ = 15V_{DC}$)

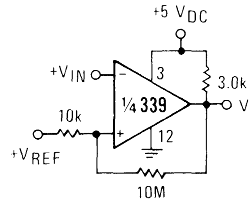
Driving TTL



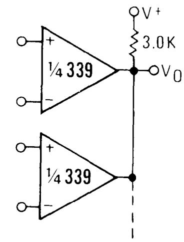
Driving CMOS



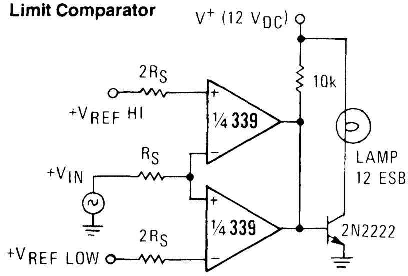
Comparator with Hysteresis



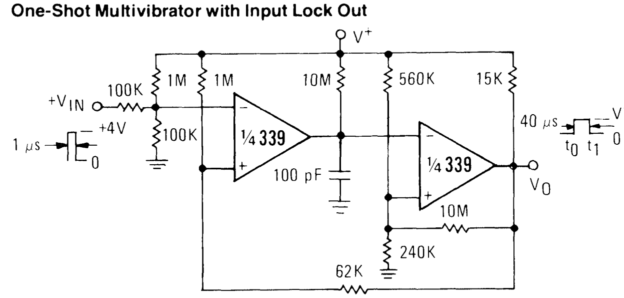
ORing the Outputs



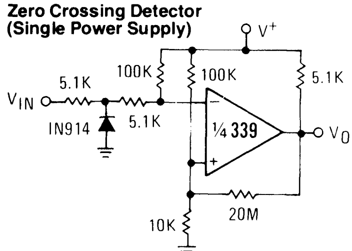
Limit Comparator



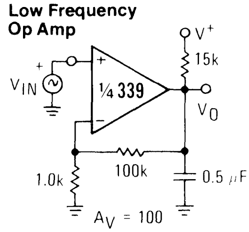
One-Shot Multivibrator with Input Lock Out



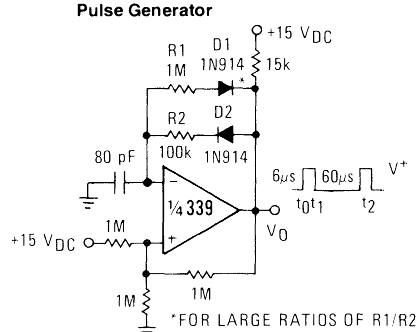
Zero Crossing Detector (Single Power Supply)



Low Frequency Op Amp

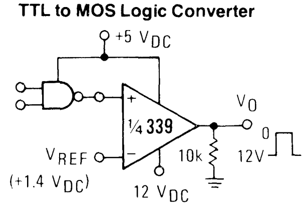


Pulse Generator



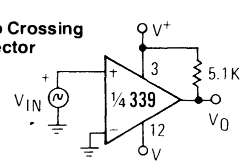
*FOR LARGE RATIOS OF R1/R2, D1 CAN BE OMITTED

TTL to MOS Logic Converter

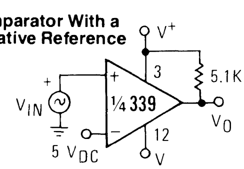


Split Supply ($V^+ = +15V_{DC}$ & $V^- = -15V_{DC}$)

Zero Crossing Detector



Comparator With a Negative Reference



GENERAL DESCRIPTION

The RM710 and RC710 integrated circuits are monolithic, high speed, differential voltage comparators. Manufactured by the planar process, component matching is inherent. Characteristic of the devices is low offset voltage and low drift parameters as well as high accuracy and fast response.

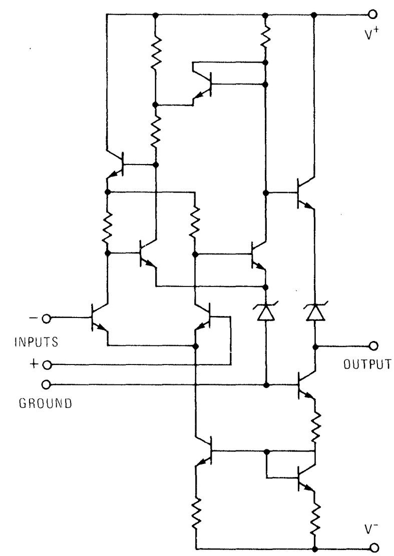
These voltage comparators are specially designed for a variety of applications such as high speed A/D converter, memory sense amplifier, zero crossing detector, amplitude discriminator and variable threshold Schmitt trigger.

The RM710 operates over the full military temperature range from −55°C to +125°C. The RC710, commercial equivalent of the RM710, operates over a temperature from 0°C to +70°C.

DESIGN FEATURES

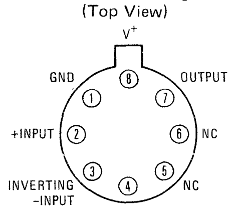
- Low Offset Voltage and Drift Over Entire Temperature Range
- Fast Response Time
- Output Logic Compatible With All Existing Integrated Logic Forms
- Meets or Exceeds All Environmental Requirements of MIL-S-19500, MIL-STD-202, and MIL-STD-750

SCHEMATIC DIAGRAM



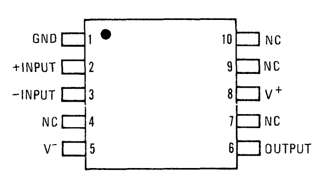
CONNECTION INFORMATION

TE
Metal Can Package
(Top View)



Order Part Nos.:
RM710T, RC710T

CQ
Flat Package
(Top View)



Order Part No.:
RM710Q

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage . . . . +14V
Negative Supply Voltage . . . . -7.0V
Peak Output Current 10.0mA
Differential Input Voltage . . . . ±5.0V
Input Voltage . . . . ±7.0V
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering, 60s) . . . . 300°C

Operating Temperature Range
RM710 . . . . -55°C to +125°C
RC710 . . . . 0°C to +70°C
Internal Power Dissipation (Note 1)
TO-5 . . . . 300mW
Flat Package 200mW

ELECTRICAL CHARACTERISTICS ($V^+ = 12.0V$, $V^- = -6.0V$, $T_A = +25^oC$ unless otherwise specified)

PARAMETER	CONDITIONS	RM710 MIN	RM710 TYP	RM710 MAX	RC710 MIN	RC710 TYP	RC710 MAX	UNITS
Input Offset Voltage (Note 3)	$R_S \leq 200\Omega$		0.6	2.0		1.6	5.0	mV
Input Offset Current (Note 3)			0.75	3.0		1.8	5.0	μA
Input Bias Current			13	20		16	25	μA
Voltage Gain		1250	1700		1000	1500		V/V
Output Resistance			200			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5mV$, $V_{out} = 0$	2.0	2.5		1.6	2.5		mA
Response Time (Note 2)			40	60		40		ns
The following specifications apply for $-55^oC \leq T_A \leq +125^oC$.					**The following specifications apply for $0^\circ C \leq T_A \leq +70^\circ C$.**			
Input Offset Voltage (Note 3)	$R_S \leq 200\Omega$			3.0			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 20\Omega$, T_A = Low to T_A = High, $R_S = 20\Omega$		3.5	10		5.0	20	μV/°C
	$T_A = 25^oC$ to T_A = Low		2.7	10				
Input Offset Current (Note 3)	$T_A = +125^oC$		0.25	3.0				μA
	T_A = Low		1.8	7.0			7.5	
Average Temperature Coefficient of Input Offset Current	$T_A = 25^oC$ to T_A = High		5.0	25		15	50	nA/°C
	$T_A = 25^oC$ to T_A = Low		15	75		24	100	
Input Bias Current	T_A = Low		27	45		25	40	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		70	98		dB
Differential Input Voltage Range		±5.0			±5.0			V
Voltage Gain		1000			800			
Positive Output Level	$\Delta V_{in} \geq 5mV$, $0 \leq I_{out} \leq 5.0mA$	2.5	3.2	4.0	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5mV$	-1.0	-0.5	0	-1.0	-0.5	0	V
Output Sink Current	T_A = Low, $\Delta V_{in} \geq 5mV$, $V_{out} = 0$	0.5	2.3		0.5			mA
	T_A = High, $\Delta V_{in} \geq 5mV$, $V_{out} = 0$	0.5	1.7		0.5			
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0		5.2	9.0	mA
Negative Supply Current			4.6	7.0		4.6	7.0	mA
Power Consumption			90	150		90	150	mW

NOTES:
1. The thermal characteristics are based on a maximum chip temperature of 160°C. Derate maximum power dissipation of TO-5 Can by 6.7mW/°C for $T_A \geq 114^\circ C$, and of Flat Pak by 5.3mW/°C for $T_A \geq 103^\circ C$. The ratings apply for $-55^\circ C \leq T_A \leq +125^\circ C$.
2. The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.
3. The input offset voltage and input offset current are specified for a logic threshold voltage as follows: For RM710 grade 1.8V at -55°C, 1.4V at +25°C and 1.0V at +125°C. For RC710 grade 1.5V at +25°C and 1.2V at +70°C.

GENERAL DESCRIPTION

The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

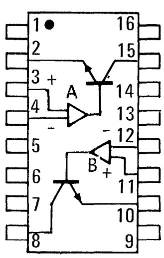
The LH2111 is specified for operation over the -55°C to +125°C military temperature range. The LH2211 is specified for operation over the -25°C to +85°C temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

DESIGN FEATURES

- Wide operating supply range — ±15V to a single +5V
- Low input currents — 6nA
- High sensitivity — 10µV
- Wide differential input range — ±30V
- High output drive — 50mA, 50V

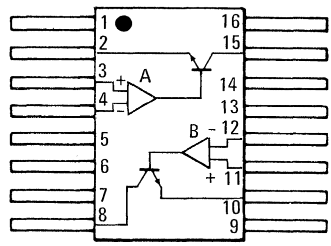
CONNECTION INFORMATION

DD Dual-In-Line Ceramic Package
(Top View)



Order Part Nos.:
LH2111D or LH2211D
or LH2311D

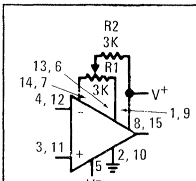
CL Flat Package
(Top View)



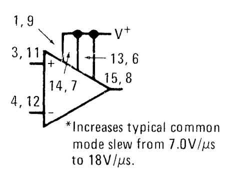
Order Part Nos.:
LH2111F or LH2211F
or LH2311F

PIN	FUNCTION
1	V_A+
2	EMITTER V OUTPUT (A)
3	+INPUT A
4	-INPUT A
5	V-
6	BAL B
7	BAL/STROBE B
8	COLLECTOR V OUTPUT (B)
9	V_B+
10	EMITTER V OUTPUT (B)
11	+INPUT B
12	-INPUT B
13	BAL A
14	BAL/STROBE A
15	COLLECTOR VOUTPUT (A)
16	NC

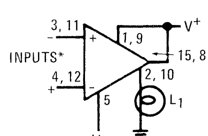
AUXILIARY CIRCUITS



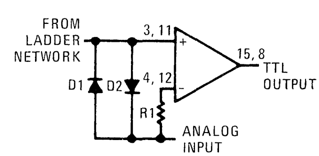
Offset Balancing



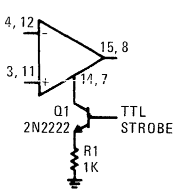
Increasing Input Stage Current*



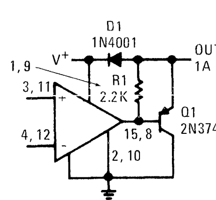
Driving Ground-Referred Load



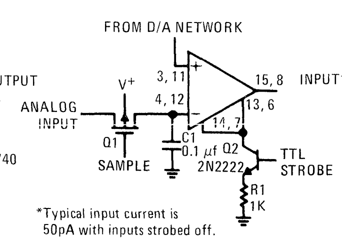
Using Clamp Diodes to Improve Responses



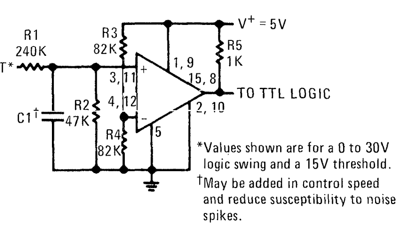
Strobing



Comparator and Solenoid Driver



Strobing off Both Input* and Output Stages



TTL Interface with High Level Logic

RAYTHEON

ABSOLUTE MAXIMUM RATINGS

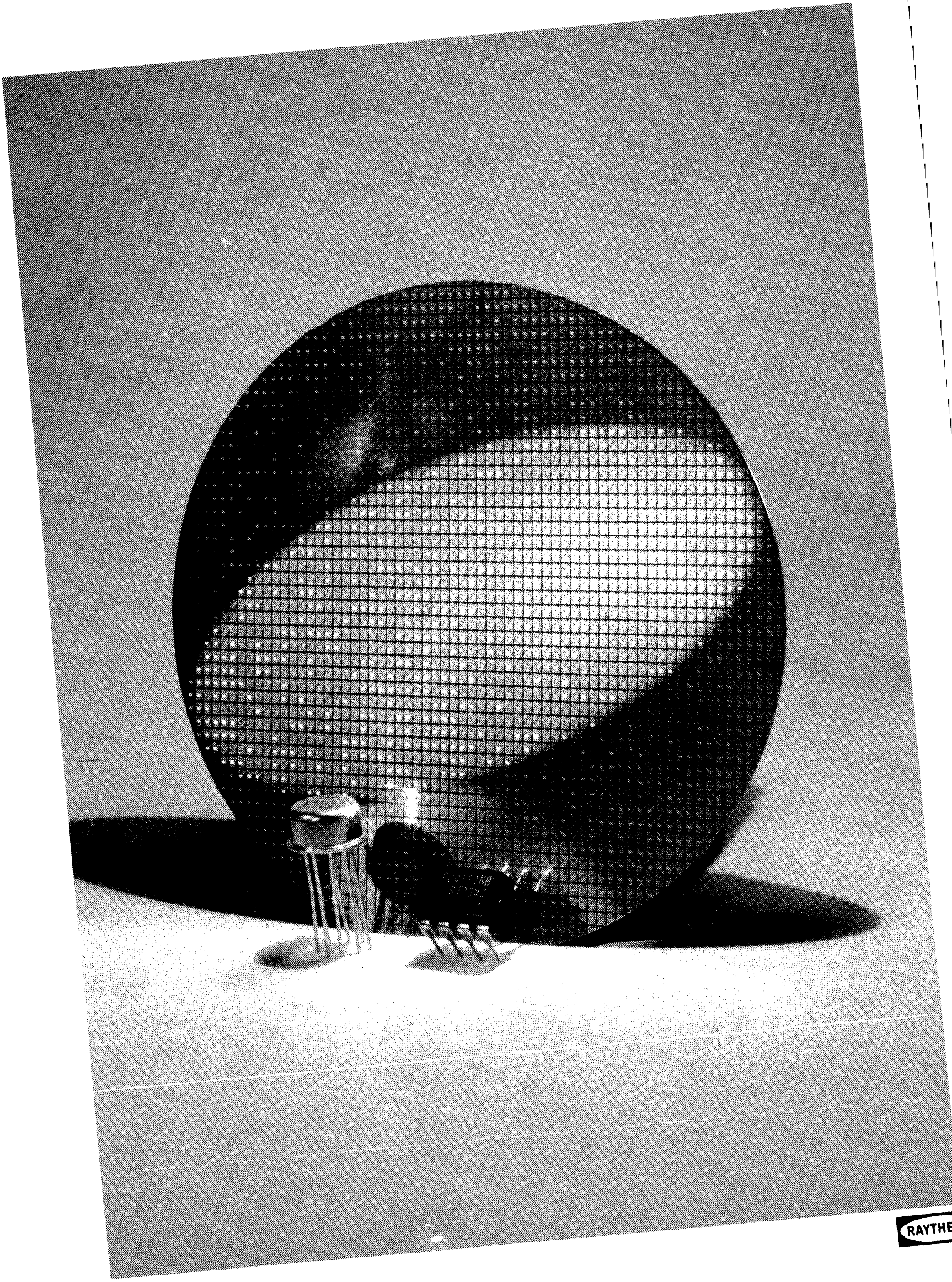
Total Supply Voltage ($V^+ - V^-$)	36V
Output to Negative Supply Voltage ($V_{OUT} - V^-$)	50V
Ground to Negative Supply Voltage (GND - V^-)	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500mW
Output Short Circuit Duration	10 sec
Operating Temperature Range LH2111	-55°C to 125°C
LH2211	-25°C to 85°C
LH2311	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS – each side (Note 3)

PARAMETER	CONDITIONS	LIMITS			UNITS
		LH2111	LH2211	LH2311	
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leqslant 50k$	3.0	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	100	250	nA Max
Voltage Gain	$T_A = 25°C$	200	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	200	ns Typ
Saturation Voltage	$V_{IN} \leqslant -5mV$, $I_{OUT} = 50mA$ $T_A = 25°C$	1.5	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	3.0	mA Typ
Output Leakage Current	$V_{IN} \geqslant 5mV$, $V_{OUT} = 35V$ $T_A = 25°C$	10	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leqslant 50k$	4.0	4.0	10	mV Max
Input Offset Current (Note 4)		20	20	70	nA Max
Input Bias Current		150	150	300	nA Max
Input Voltage Range		±14	±14	±14	V Typ
Saturation Voltage	$V^+ \geqslant 4.5V$, $V^- = 0$ $V_{IN} \leqslant -5mV$, $I_{SINK} \leqslant 8mA$	0.4	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	5.0	mA Max

NOTES:

1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. The maximum junction temperature is 150°C. For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with 0.03-inch-wide, 2-ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
3. These specifications apply for $V_S = \pm 15V$ and $-55°C \leqslant T_A \leqslant 125°C$ for the LH2111, $-25°C \leqslant T_A \leqslant 85°C$ for the LH2211, and $0°C \leqslant T_A \leqslant 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm 10mV$.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified is for a 100mV input step with 5mV overdrive.



SECTION 6

Line Drivers and Receivers

CONTENTS

1488 Quad Line Drivers

DESCRIPTION

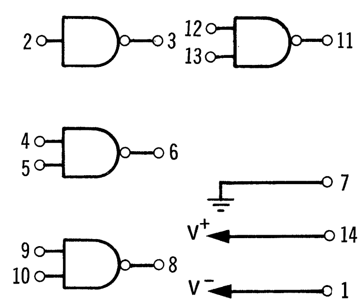
The RC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA standard number RS-232-C. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used.

The RC1488 and its companion circuit, the RC1489/RC1489A quad line receiver, provide a complete interface system between DTL and TTL logic levels and the RS-232-C defined levels.

DESIGN FEATURES

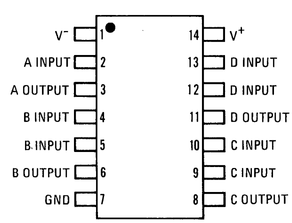
- Current Limited Output 10mA Typical
- Power-off Source Impedance 300 Ohms Minimum
- Simple Slew Rate Control With External Capacitor
- Flexible Operating Supply Range
- Compatible With All DTL and TTL Logic

LOGIC DIAGRAM



CONNECTION INFORMATION

DB and DC Dual In-line Package
(Top View)



Order Part Nos.:
RC1488DB, RC1488DC

Quad Line Drivers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Power Supply Voltage	V^+	+15	V
	V^-	−15	
Input Signal Voltage	V_{in}	$-15 \leqslant V_{in} \leqslant 7.0$	V
Output Signal Voltage	V_O	±15	V
Power Derating (Package Limitation, Ceramic and Plastic Dual In-Line Packages)	P_D	1000	mW
Derate above T_A = +25°C	$1/\theta_{JA}$	6.7	mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V^+ = +9.0 ±1% Vdc, V^- = −9.0 ±1% Vdc, T_A = 0°C to +75°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Forward Input Current	I_F	V_{in} = 0V		1.0	1.6	mA
Reverse Input Current	I_R	V_{in} = +5.0V			10	μA
Output Voltage High	V_{OH}	V_{in}=0.8V, R_L=3.0kΩ, V^+=+9.0V, V^-=−9.0V	+6.0	+7.0		V
		V_{in}=0.8V, R_L=3.0kΩ, V^+=+13.2V, V^-=−13.2V	+9.0	+10.5		
Output Voltage Low	V_{OL}	V_{in}=1.9Vdc, R_L=3.0kΩ, V^+=+9.0V, V^-=−9.0V	−6.0	−7.0		V
		V_{in}=1.9Vdc, R_L=3.0kΩ, V^+=+13.2V, V^- = −13.2V	−9.0	−10.5		
Positive Output Short-Circuit Current	I_{SC+}		+6.0	+10	+12	mA
Negative Output Short-Circuit Current	I_{SC-}		−6.0	−10	−12	mA
Output Resistance	R_O	$V^+ = V^- = 0$, $\lvert V_O \rvert$ = ±2.0V	300			Ω
Positive Supply Current ($R_l = \infty$)	I^+	V_{in} = 1.9Vdc, V^+ = +9.0V		+15	+20	mA
		V_{in} = 0.8Vdc, V^+ = +9.0V		+4.5	+6.0	
		V_{in} = 1.9Vdc, V^+ = +12V		+19	+25	
		V_{in} = 0.8Vdc, V^+ = +12V		+5.5	+7.0	
		V_{in} = 1.9Vdc, V^+ = +15V			+34	
		V_{in} = 0.8Vdc, V^+ = +15V			+12	
Negative Supply Current ($R_L = \infty$)	I^-	V_{in} 1.9Vdc, V^- = −9.0V		−13	−17	mA
		V_{in} = 0.8Vdc, V^- = −9.0V		0	0	
		V_{in} = 1.9Vdc, V^- = −12V		−18	−23	
		V_{in} = 0.8Vdc, V^- = −12V		0	0	
		V_{in} = 1.9Vdc, V^- = −15V			−34	
		V_{in} = 0.8Vdc, V^- = −15V			−2.5	
Power Dissipation	P_D	V^+ = 9.0Vdc, V^- = −9.0V			333	mW
		V^+ = 12Vdc, V^- = −12V			576	

SWITCHING CHARACTERISTICS (V^+ = +9.0 ±1% Vdc, V^- = −9.0 ±1% Vdc, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Porpagation Delay Time	t_{pd+}	Z_L = 3.0k and 15pF		275	350	ns
Fall Time	t_f	Z_L = 3.0k and 15pF		45	75	ns
Propagation Delay Time	t_{pd-}	Z_L = 3.0k and 15pF		110	175	ns
Rise Time	t_r	Z_L - 3.0k and 15pF		55	100	ns

1489
1489A
Quad Line Receivers

GENERAL DESCRIPTION

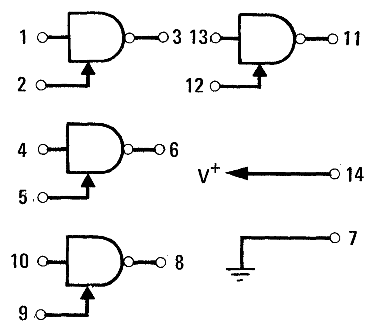
The RC1489 and RC1489A are monolithic quad line receivers designed to interface data terminal equipment in conformance with the specifications of EIA standard number RS-232-C. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used.

The RC1488 quad driver and its companion circuit, the RC1489/RC1489A quad receiver, provide a complete interface system between DTL or TTL logic levels and the RS-232-C defined levels.

DESIGN FEATURES

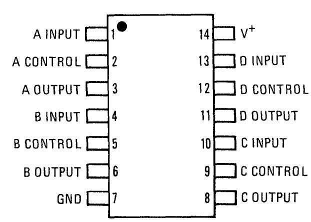
- Input Resistance 3k to 7k
- Input Signal Range ±30V
- Built-in Input Threshold Hysteresis
- Response Control: Logic Threshold Shifting and Input Noise Filtering

LOGIC DIAGRAM



CONNECTION INFORMATION

DB and DC
Dual In-line Package
(Top View)



Order Part Nos.:
RC1489DC, RC1489ADC,
RC1489DB, RC1489ADB

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Power Supply Voltage	V^+	+10	V
Input Signal Range	V_{in}	±30	V
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Packages)	P_D	1000	mW
Derate above T_A = +25°C	$1/\theta_{JA}$	6.7	mW/°C
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS

(Response control pin is open. V^+=+5.0Vdc ±1%, T_A=0°C to +75°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Positive Input Current	I_{IH}	V_{in} = +25V	3.6		8.3	mA
		V_{in} = +3.0V	0.43			
Negative Input Current	I_{IL}	V_{in} = −25V	−3.6		−8.3	mA
		V_{in} = −3.0V	−0.43			
Input Turn-On Threshold Voltage	V_{IH}	T_A = +25°C, $V_{OL} \leqslant$ 0.45V RC1489	1.0		1.5	V
		RC1489A	1.75	1.95	2.25	
Input Turn-Off Threshold Voltage	V_{IL}	T_A = +25°C, $V_{OH} \geqslant$ 2.5V, I_L = −0.5mA RC1489	0.75		1.25	V
		RC1489A	0.75	0.8	1.25	
Output Voltage High	V_{OH}	V_{in} = 0.75V, I_L = −0.5mA	2.6	4.0	5.0	V
		Input Open Circuit, I_L = −0.5mA	2.6	4.0	5.0	
Output Voltage Low	V_{OL}	V_{in} = 3.0V, I_L = 10mA		0.2	0.45	V
Output Short-Cirucuit Current	I_{SC}			3.0		mA
Power Supply Current	I^+	V_{in} = +5.0V		20	26	mA
Power Dissipation	P_D	V_{in} = +5.0V		100	130	mW

SWITCHING CHARACTERISTICS (V^+ = +5.0 Vdc ±1%, T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time	t_{pd+}	R_L = 3.9Ω		25	85	ns
Rise Time	t_r	R_L = 3.9Ω		120	175	ns
Propagation Delay Time	t_{pd-}	R_L = 390Ω		25	50	ns
Fall Time	t_f	R_L = 390Ω		10	20	ns

GENERAL DESCRIPTION

The RM9622 and RC9622 are dual line receivers designed to discriminate a worst-case logic swing of 2V from a ±10V common-mode noise signal or ground shift. To provide a CCSL-compatible threshold voltage and maximum noise immunity, the differential amplifier has a built-in threshold of 1.5V. The offset is obtained by use of current sources and matched resistors, and varies only ±5% (75mV) over the military and commercial temperature ranges.

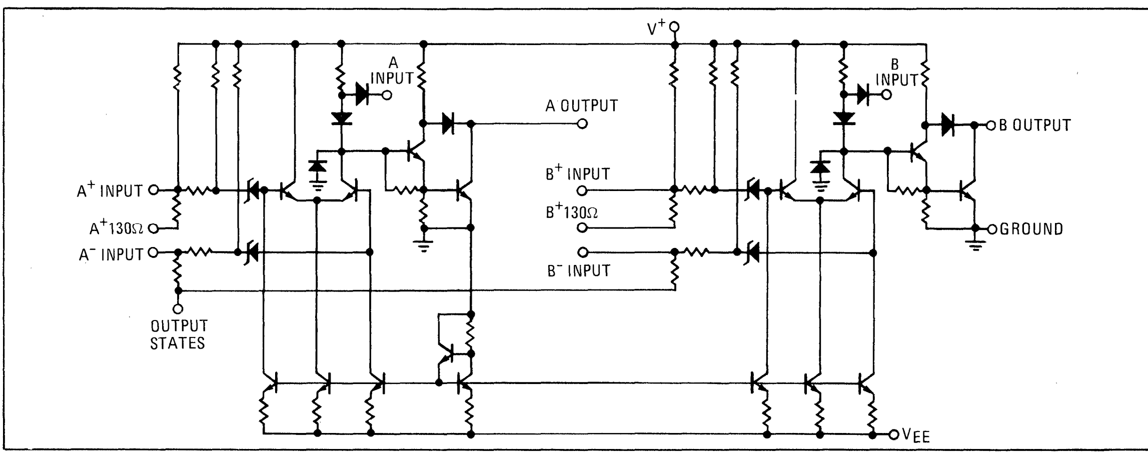
The RM9622 military version operates over a temperature range of −55°C to +125°C. The RC9622 is the commercial type which operates from 0°C to +70°C.

These dual line receivers offer a choice of output states with the inputs open, without affecting circuit performance by use of S3. At the input of each line receiver a 130-ohm terminating resistor is provided. The output is CCSL-compatible. And the output high level can be increased to +12V by connecting to a positive supply through a resistor. The outputs can be wired OR.

DESIGN FEATURES

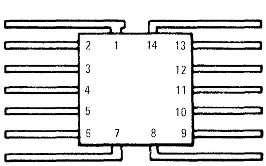
- CCSL-Compatible Threshold Voltage
- Input Terminating Resistors
- Choice of Output State With Inputs Open
- CCSL-Compatible Output
- High Common-Mode
- Wire-OR Capability
- Enable Inputs
- Full Military Temperature Range
- Logic Compatible Supply Voltages

SCHEMATIC DIAGRAM



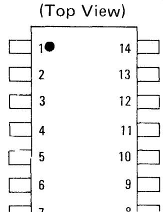
CONNECTION INFORMATION

CJ Flat Pack
(Top View)



Order Part No.:
RM9622CJ

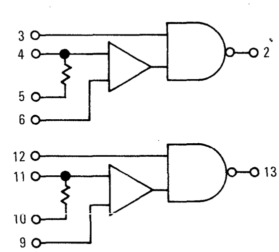
DC Dual In-line Package
(Top View)



Order Part Nos.:
RM9622DC, RC9622DC

PIN	FUNCTION
1	OUTPUT STATES
2	A OUTPUT
3	A INPUT
4	A+
5	A+130Ω
6	A−
7	V+
8	V−
9	B−
10	B+130Ω
11	B+
12	B INPUT
13	B OUTPUT
14	GROUND

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{CC}, Pin Potential to Ground Pin . . . . -0.5V to +7V
Input Voltage . . . . ±15V
Voltage Applied to Outputs for High Output State . . . . -0.5V to +13.2V
V_{EE} Pin Potential to Ground Pin . . . . -0.5V to -12V
Enable Pin Potential to Ground Pin . . . . -0.5V to -15V
Storage Temperature Range . . . . -65°C to +150°C

Operating Temperature Range
RM9622 . . . . -55°C to +125°C
RC9622 . . . . 0°C to +70°C
Internal Power Dissipation (Note 1)
Ceramic Dip 670mW
Flatpak 570mW

ELECTRICAL CHARACTERISTICS (-55°C to +125°C, V_{CC} = 5.0V ±10%, V_{EE} = -10V ±10%)

SYMBOL	CHARACTERISTICS	CONDITIONS & COMMENTS	LIMITS -55°C MIN	-55°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+125°C MIN	+125°C MAX	UNITS
V_{OL}	Output Low Voltage	V_{CC} = 4.5V, V_{EE} = -11V, *V_{DIFF} = 2.0V, I_{OL} = 12.4mA		0.40		0.25	0.40		0.40	V
V_{OH}	Output High Voltage	V_{CC} = 4.5V, V_{EE} = -9.0V, *V_{DIFF} = 1.0V, I_{OH} = -0.2mA	2.8		3.0	3.3		2.9		V
I_{CEX}	Output Leakage Current	V_{CC} = 4.5V, V_{EE} = -11V, *V_{DIFF} = 1.0V, V_{CEX} = 12V		50			100		200	μA
I_{SC}	Output Shorted Current	V_{CC} = 5.0V, V_{EE} = -10V, *V_{DIFF} = 1.0V, V_{SC} = 0V	-1.3	-3.1	-1.4	-2.15	-3.1	-1.3	-3.1	mA
$I_{R(ENABLE)}$	Enable Input Leakage Current	V_{CC} = 4.5V, V_{EE} = -11V, S_3 = 4.5V, V_R = 4.0V					2.0		5.0	μA
$I_{F(ENABLE)}$	Enable Input Forward Current	V_{CC} 5.5V, V_{EE} = -9.0V, S_3 = 0V, V_F = 0V		-1.5		-0.96	-1.5		-1.5	mA
$I_{F(+ INPUT)}$	+ Input Forward Current	V_{CC} = 5.0V, V_{EE} = -10V, -Input = Gnd, V_F = 0V		-2.3		-1.67	-2.1		-2.0	mA
$I_{F(- INPUT)}$	– Input Forward Current	V_{CC}, S_3 = 5.0V, V_{EE} = -10V, + Input = Gnd, V_F = 0V		-2.6		-1.87	-2.4		-2.3	mA
$V_{IL(ENABLE)}$	Input Low Voltage	V_{CC} = 5.0V ±10%, V_{EE} = -10V ±10%		1.3		1.4	1.0		0.7	V
V_{th}	Differential Input Threshold Voltage	V_{CC} = 5.0V ±10%, V_{EE} = -10V ±10%	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V
V_{CM}	Common Mode Voltage	V_{CC} = 5.0V, V_{EE} = -10V, *V_{DIFF} = 1.0V or 2.0V			-10	±12	+10			V
$R_{130\Omega}$	Terminating Resistance	V_{CC} = 5.5V, V_{EE} = -11V			100	130	175			Ω
I_{CC}	5V Supply Current	S_3, + Inputs = 5.5V, -Inputs = 0V				13.7	22.9			mA
I_{EE}	-10V Supply Current	V_{CC} = 5.5V, V_{EE} = -11V, S_3, + Inputs = 5.5V, – Inputs = 0V				-6.5	-11.1			mA
t_{pd+}	Turn-off Time	V_{CC} = 5.0V, V_{EE} = -10V, V_{IN} 0→3.0V, R_L = 3.9kΩ, C_L = 30pF				38	50			ns
t_{pd-}	Turn-on Time	V_{CC} = 5.0V, V_{EE} = -10V, V_{IN} 0→3.0V, R_L = 0.39kΩ, C_L = 30pF				35	50			ns

*V_{DIFF} is a differential input voltage referred from A+ to A- and from B+ to B-.

NOTE:

1. Rating applies to ambient temperature up to 70°C. Above 70°C, derate linearly at 8.3mW/°C for the ceramic DIP and 7.1mW/°C for the Flatpak.

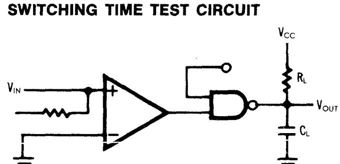
ELECTRICAL CHARACTERISTICS (0°C to +75°C, V_{CC} = 5.0V ±5%, V_{EE} = −10V ±5%)

SYMBOL	CHARACTERISTICS	CONDITIONS & COMMENTS		LIMITS 0°C MIN	0°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+75°C MIN	+75°C MAX	UNITS
V_{OL}	Output Low Voltage	V_{CC} = 4.75V *V_{DIFF} = 2.0V	V_{EE} = −10.5V I_{OL} - 14.1mA		0.45		0.25	0.45		0.45	V
V_{OH}	Output High Voltage	V_{CC} = 4.75V *V_{DIFF} = 1.0V	V_{EE} = −9.5V I_{OH} = −0.2mA	2.9		3.0	3.3		2.9		V
I_{CEX}	Output Leakage Current	V_{CC} = 4.75V *V_{DIFF} = 1.0V	V_{EE} = −10.5V V_{CEX} = 5.25V		80			100		200	µA
I_{SC}	Output Shorted Current	V_{CC} = 5.0V *V_{DIFF} = 1.0V	V_{EE} = −10V V_{SC} = 0V	−1.3	−3.1	−1.4	−2.15	−3.1	−1.3	−3.1	mA
$I_{R(ENABLE)}$	Enable Input Leakage Current	V_{CC} = 4.75V S_3 = 4.75V	V_{EE} = −10.5V V_R = 4.0V					5.0		10	µA
$I_{F(ENABLE)}$	Enable Input Forward Current	V_{CC} 5.25V S_3 = 0V	V_{EE} = −9.5V V_F = 0V		−1.5		−0.96	−1.5		−1.5	mA
$I_{F(+ INPUT)}$	+ Input Forward Current	V_{CC} = 5.0V −Input = Gnd	V_{EE} = −10V V_F = 0V		−2.6		−1.67	−2.4		−2.3	mA
$I_{F(- INPUT)}$	− Input Forward Current	V_{CC}, S_3 = 5.0V + Input = Gnd	V_{EE} = −10V V_F = 0V		−2.9		−1.87	−2.7		−2.6	mA
$V_{IL(ENABLE)}$	Input Low Voltage	V_{CC} = 5.0V ±5%	V_{EE} = −10V ±5%		1.2		1.4	1.0		0.85	V
V_{th}	Differential Input Threshold Voltage	V_{CC} = 5.0V ±5%	V_{EE} = −10V ±5%	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V
V_{CM}	Common Mode Voltage	V_{CC} = 5.0V *V_{DIFF} = 1.0V or 2.0V	V_{EE} = −10V			−7.5	±12	+7.5			V
$R_{130\Omega}$	Terminating Resistance	V_{CC} = 5.25V	V_{EE} = −10.5V			91	130	185			Ω
I_{CC}	5V Supply Current	S_3, + Inputs = 5.25 V, −Inputs = 0V					13.7	22.9			mA
I_{EE}	−10V Supply Current	V_{CC} = 5.25V S_3, + Inputs = 5.25V, −Inputs = 0V	V_{EE} = −10.5V				−6.5	−11.1			mA
t_{pd+}	Turn-off Time	V_{CC} = 5.0V V_{IN}0→3.0V, R_L = 3.9kΩ, C_L = 30pF	V_{EE} = −10V				38	100			ns
t_{pd-}	Turn-on Time	V_{CC} = 5.0V V_{IN}0→3.0V, R_L = 0.39kΩ, C_L = 30pF	V_{EE} = −10V				35	100			ns

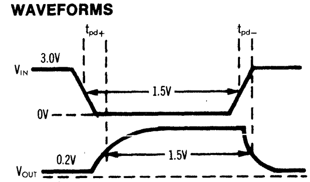
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

TYPICAL APPLICATIONS

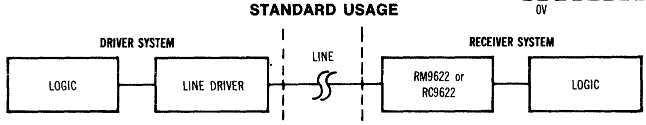
SWITCHING TIME TEST CIRCUIT



WAVEFORMS

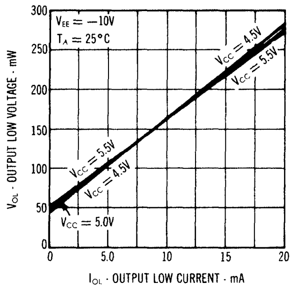


STANDARD USAGE

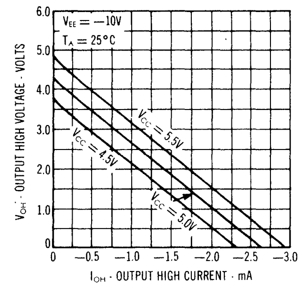


TYPICAL ELECTRICAL DATA

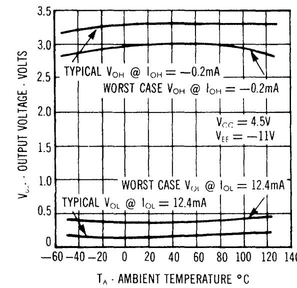
Output Low Voltage versus Output Low Current



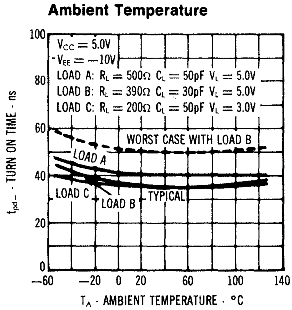
Output High Voltage versus Output High Current



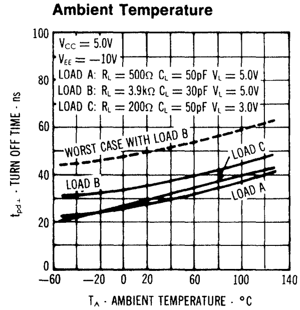
Logic Levels versus Ambient Temperature



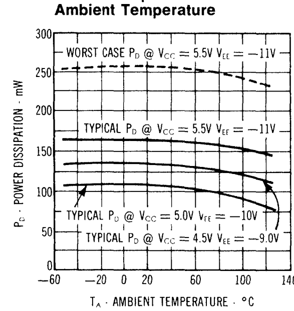
Turn On Time versus Ambient Temperature



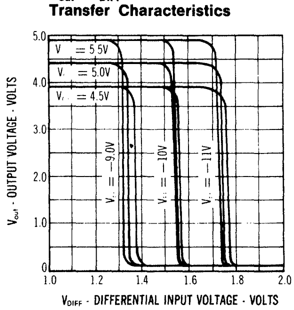
Turn Off Time versus Ambient Temperature



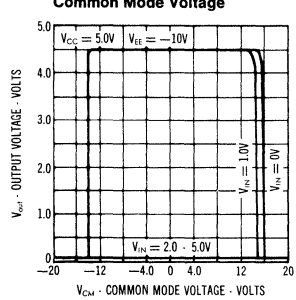
Power Dissipation versus Ambient Temperature



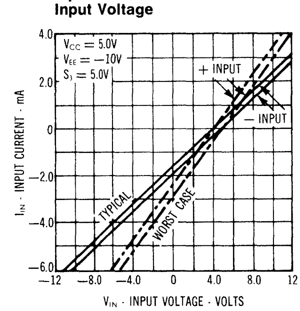
V_{out} - V_{DIFF} Transfer Characteristics



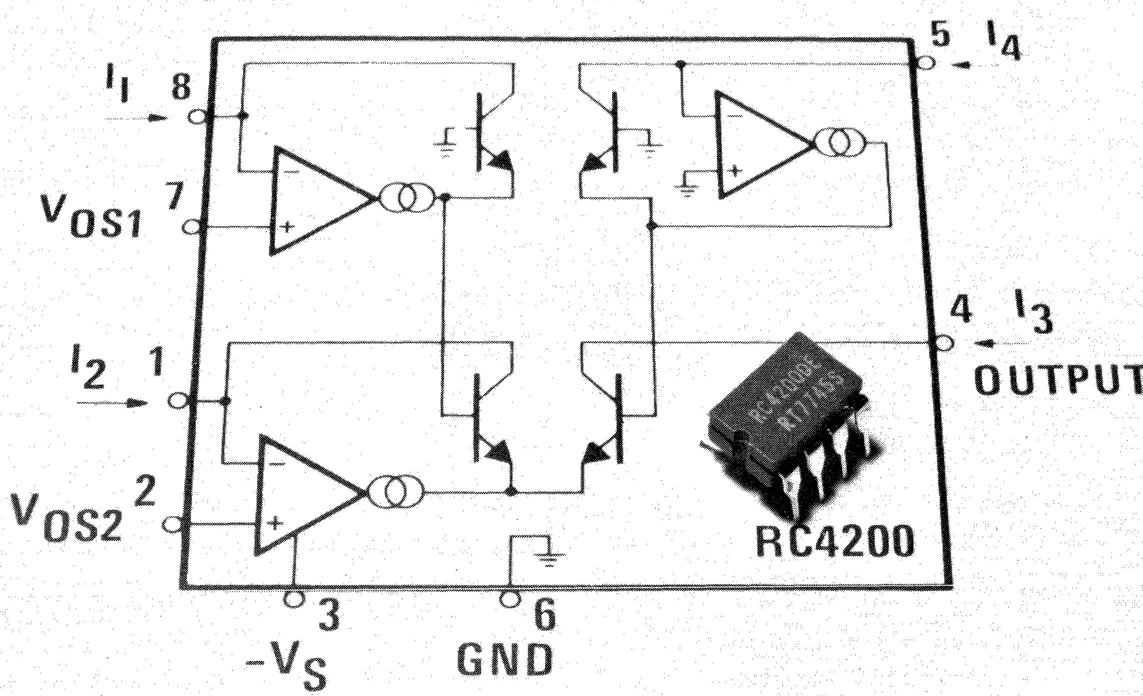
Output Voltage versus Common Mode Voltage



Input Current versus Input Voltage



FUNCTIONAL DIAGRAM OF RC4200 MULTIPLIER



SECTION 7

Special Functions

CONTENTS

GENERAL DESCRIPTION

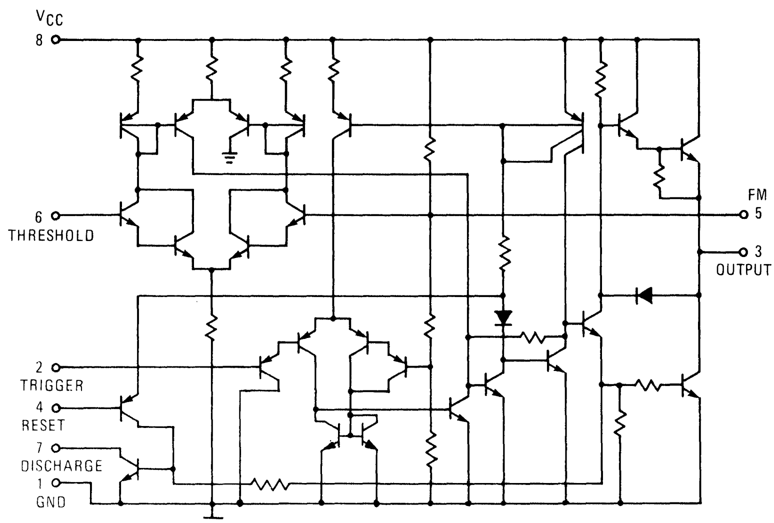
The RC555 and RM555 monolithic timing circuits are highly stable controllers capable of producing accurate time delays or oscillation. In the time delay mode, delay time is precisely controlled by only two external parts: a resistor and a capacitor. For operation as an oscillator, both the free running frequency and the duty cycle are accurately controlled by two external resistors and a capacitor.

Terminals are provided for triggering and resetting. The circuit will trigger and reset on falling waveforms. The output can source or sink up to 200mA or drive TTL circuits.

DESIGN FEATURES

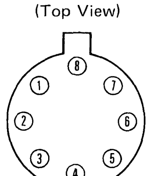
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- Output Drives TTL
- High Current Output Can Source or Sink 200mA
- Temperature Stability of 0.005%/°C
- Normally On and Normally Off Output

SCHEMATIC DIAGRAM



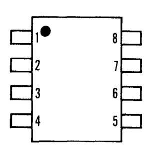
CONNECTION INFORMATION

TE Metal Can Package
(Top View)



Order Part Nos.:
RC555T, RM555T

DE and NB Dual In-line Packages
(Top View)



Order Part Nos.:
RC555NB, RV555NB
RC555DE, RV555DE, RM555DE

PIN	FUNCTION
1	GROUND
2	TRIGGER
3	OUTPUT
4	RESET
5	CONTROL VOLTAGE
6	THRESHOLD
7	DISCHARGE
8	V_{CC}

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+18V	Operating Temperature Range	
Power Dissipation	600mW	RC555	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	RV555	−40°C to +85°C
Lead Temperature (Soldering, 60s)	+300°C	RM555	−55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V to +15V, T_A = 25°C unless otherwise specified)

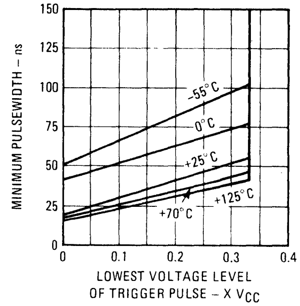
PARAMETER	CONDITIONS	RM555			RV/RC555			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞		10	12		10	15	mA
	Low State, (Note 1)							
Timing Error	R_A, R_B = 1kΩ to 100kΩ							
	C = 0.1μF (Note 2)							
Initial Accuracy			0.5	2		1		%
Drift with Temperature			30	100		50.1		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%/Volt
Threshold Voltage			2/3			2/3		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	(Note 3)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		2	2.2		2	2.5	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					0.25	0.35	
Output Voltage Drop (high)	I_{SOURCE} = 200mA							
	V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

NOTES:

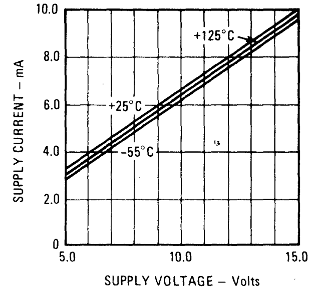
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of R_A + R_B. For 15V operation, the max total R = 20 megohm.

TYPICAL ELECTRICAL DATA

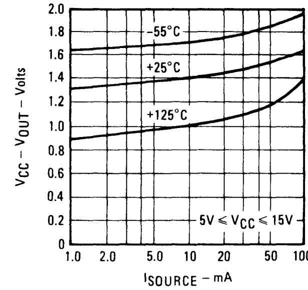
Minimum Pulse Width Required for Triggering



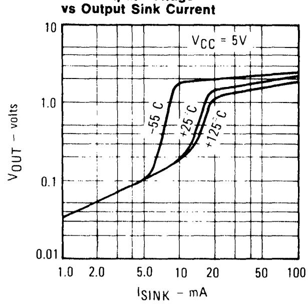
Supply Current vs Supply Voltage



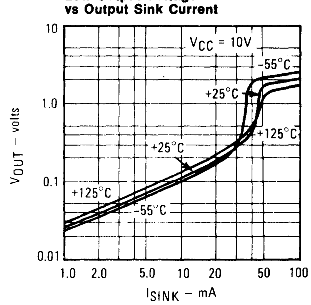
High Output Voltage vs Output Source Current



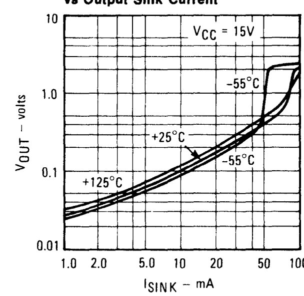
Low Output Voltage vs Output Sink Current



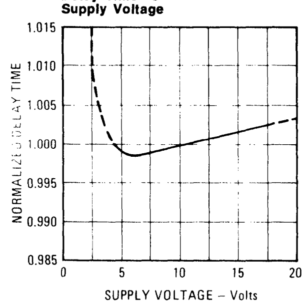
Low Output Voltage vs Output Sink Current



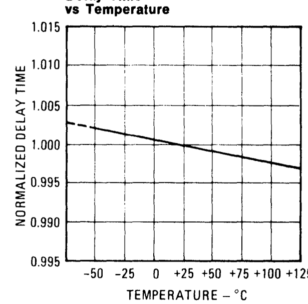
Low Output Voltage vs Output Sink Current



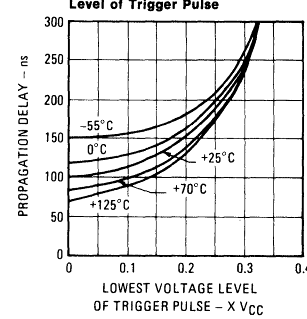
Delay Time vs Supply Voltage



Delay Time vs Temperature



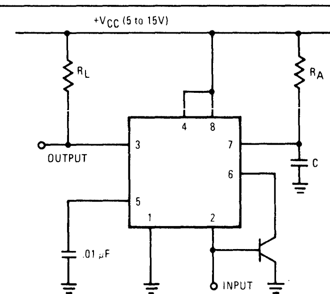
Propagation Delay vs Voltage Level of Trigger Pulse



TYPICAL APPLICATIONS

Missing Pulse Detector

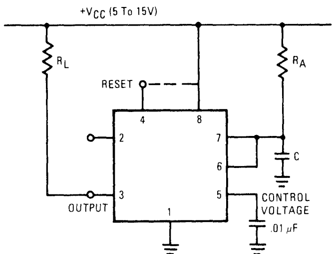
With the RC555/RM555 connected as shown, the timing cycle will be continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows the timing cycle to go to completion and change the output level. For proper operation the time delay should be set slightly longer than the normal time between pulses.



TYPICAL APPLICATIONS (Cont.)

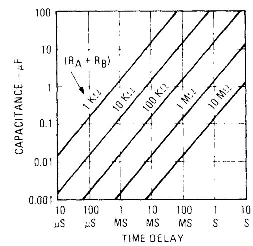
Monostable Operation

In this mode, the timer functions as a one-shot. The external capacitor is initially held discharged by a transistor internal to the timer. Applying a negative trigger pulse to Pin 2 sets the flip-flop, driving the output high and releasing the short-circuit across the external capacitor. The voltage across the capacitor increases with time constant r = R_AC to 2/3 V_{CC}, where the comparator resets the flip-flop and discharges the external capacitor. The output is now in the low state.



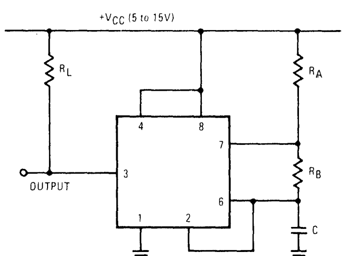
Circuit triggering takes place when the negative-going trigger pulse reaches 1/3V_{CC} and the circuit stays in the output high state until the set time elapses. The time the output remains in the high state is 1.1R_AC and can be determined by the graph. A negative pulse applied to Pin 4 (reset) during the timing cycle will discharge the external capacitor and start the cycle over again beginning on the positive-going edge of the reset pulse. If reset function is not used, Pin 4 should be connected to V_{CC} to avoid false resetting.

Time Delay vs R_A, R_B and C

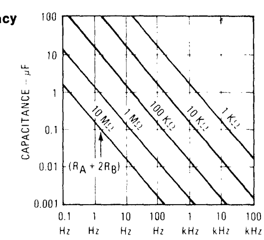


Free Running Operation

With the circuit connected as shown, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle is set by the ratio of these two resistors, and the capacitor charges and discharges between 1/3V_{CC} and 2/3V_{CC}. Charge and discharge times, and therefore frequency, are independent of supply voltage. The free running frequency versus R_A, R_B, and C is shown in the graph.



Free Running Frequency vs R_A, R_B and C



GENERAL DESCRIPTION

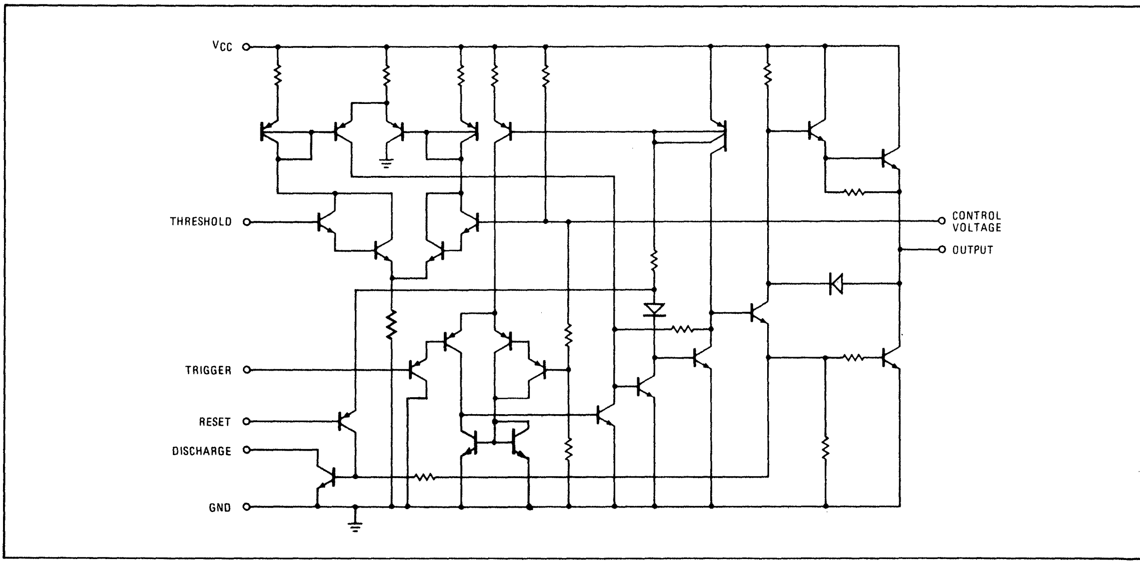
The RC556 and RM556 dual monolithic timing circuits are highly stable controllers capable of producing accurate time delays or oscillation. In the time delay mode, delay time is precisely controlled by only two external parts: a resistor and a capacitor. For operation as an oscillator, both the free running frequency and the duty cycle are accurately controlled by two external resistors and a capacitor.

Terminals are provided for triggering and resetting. The circuit will trigger and reset on falling waveforms. The output can source or sink up to 200mA or drive TTL circuits.

DESIGN FEATURES

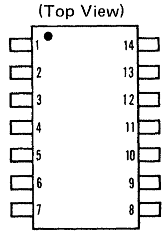
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- Output Drives TTL
- High Current Output Can Source or Sink 200mA
- Temperature Stability of 0.005%/°C
- Normally On and Normally Off Output

SCHEMATIC DIAGRAM (1/2 shown)



CONNECTION INFORMATION

DC and DB
Dual In-line Packages
(Top View)



Order Part Nos.:
RC556DB, RC556DC, RM556DC, RV556DB, RV556DC

PIN	FUNCTION
1	DISCHARGE A
2	THRESHOLD A
3	CONTROL A
4	RESET A
5	OUTPUT A
6	TRIGGER A
7	GROUND
8	TRIGGER B
9	OUTPUT B
10	RESET B
11	CONTROL B
12	THRESHOLD B
13	DISCHARGE B
14	V_{CC}

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +18V	Operating Temperature Range
Power Dissipation 600mW	RC556 . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C	RM556 . . . . . −55°C to +125°C
Lead Temperature (Soldering, 60s) . . . . . +300°C	RV556 . . . . . −40°C to +85°C

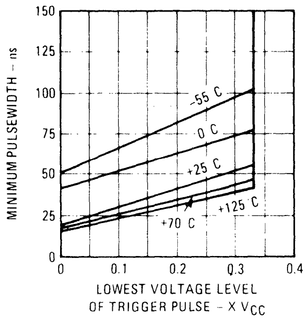
ELECTRICAL CHARACTERISTICS (V_{CC} = +5V to +15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM556			RC556, RV556			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current (Each Side)	V_{CC} = 5V, $R_L = \infty$		3	5		3	6	mA
	V_{CC} = 15V, $R_L = \infty$ Low State, (Note 1)		10	11		10	14	mA
Timing Error (Free Running)	R_A, R_B = 2kΩ to 100kΩ C = 0.1μF (Note 2)							
Initial Accuracy			1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Drift with Supply Voltage			0.15			0.3		%/Volt
Timing Error (Monostable)	R_A, R_B = 2kΩ to 100kΩ C = 0.1μF (Note 2)							
Initial Accuracy			0.5	1.5		0.75		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%/Volt
Threshold Voltage			2/3			2/3		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	(Note 3)		0.03	0.1		0.03	0.1	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100mA		2	2.25		2	2.75	V
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				V
	I_{SINK} = 5mA					0.25	0.35	
Output Voltage Drop (high)	I_{SOURCE} = 200mA V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns
Matching Characteristics Between Each Section								
Initial Timing Accuracy			0.3	0.6		0.5	1	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%/Volt

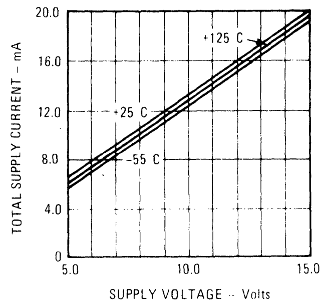
Notes on following page.

TYPICAL ELECTRICAL DATA

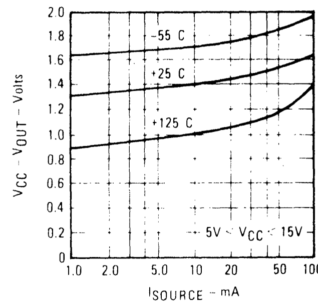
Minimum Pulse Width Required for Triggering



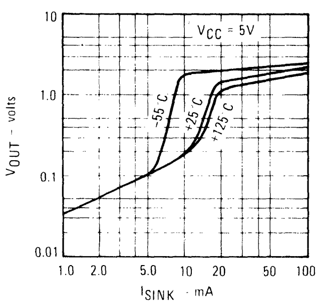
Supply Current vs Supply Voltage



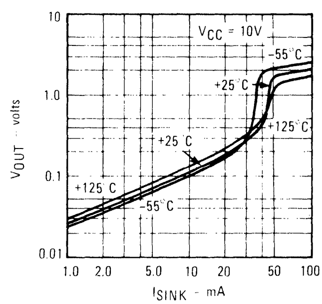
High Output Voltage vs Output Source Current



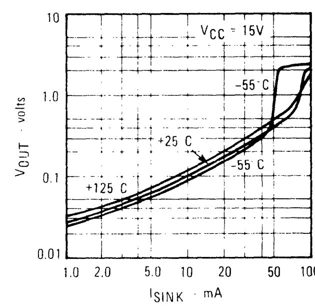
Low Output Voltage vs Output Sink Current



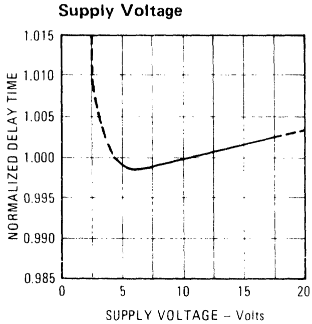
Low Output Voltage vs Output Sink Current



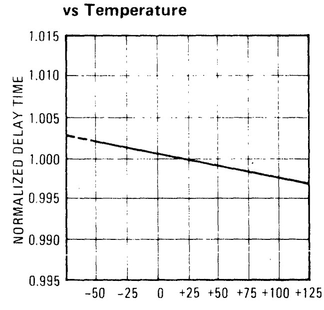
Low Output Voltage vs Output Sink Current



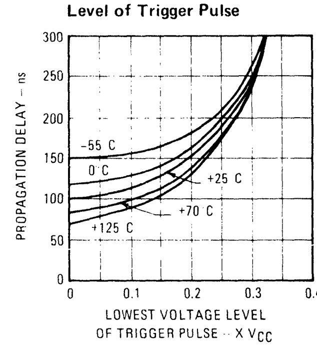
Delay Time vs Supply Voltage



Delay Time vs Temperature



Propagation Delay vs Voltage Level of Trigger Pulse



NOTES

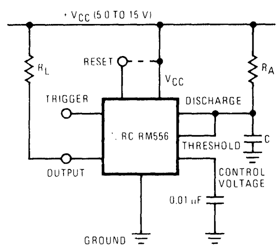
1. Supply current when output high typically 2mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V.
3. This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total R = 20MΩ.

BASIC OPERATIONAL MODES

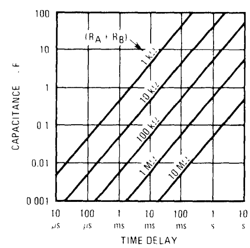
Monostable Operation

In this mode, the timer functions as a one-shot. The external capacitor is initially held discharged by a transistor internal to the timer. Applying a negative trigger pulse to Pin 2 sets the flip-flop, driving the output high and releasing the short-circuit across the external capacitor. The voltage across the capacitor increases with time constant $r = R_AC$ to 2/3 V_{CC}, where the comparator resets the flip-flop and discharges the external capacitor. The output is now in the low state.

Circuit triggering takes place when the negative-going trigger pulse reaches $1/3V_{CC}$ and the circuit stays in the output high state until the set time elapses. The time the output remains in the high state is $1.1R_AC$ and can be determined by the graph. A negative pulse applied to Pin 4 (reset) during the timing cycle will discharge the external capacitor and start the cycle over again beginning on the positive-going edge of the reset pulse. If reset function is not used, Pin 4 should be connected to V_{CC} to avoid false resetting.

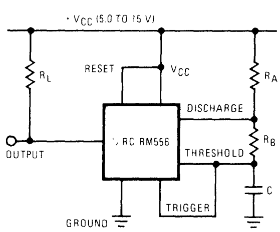


Time Delay vs R_A, R_B and C

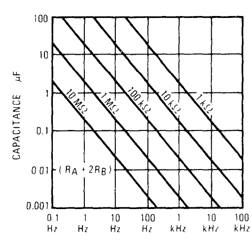


Free Running Operation (Astable)

With the circuit connected as shown, it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle is set by the ratio of these two resistors, and the capacitor charges and discharges between $1/3V_{CC}$ and $2/3V_{CC}$. Charge and discharge times, and therefore frequency, are independent of supply voltage. The free running frequency versus R_A, R_B, and C is shown in the graph.



Free Running Frequency vs R_A, R_B and C



DESCRIPTION

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK, and sweep or tone generation, as well as for phase-locked loop applications.

As shown in Figure 1, the circuit is comprised of four functional blocks: a variable-frequency oscillator which generates the basic periodic waveforms; four current switches actuated by binary keying inputs; and buffer amplifiers for both the triangle and squarewave outputs. The internal switches transfer the oscillator current to any of four external timing resistors to produce four discrete frequencies which are selected according to the binary logic levels at the keying terminals (pins 8 and 9).

The XR-2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage; and the duty cycle of both the triangle and the squarewave outputs can be varied from 0.1% to 99.9% to generate stable pulse and sawtooth waveforms.

FEATURES

- Excellent Temperature Stability (20 ppm/°C)
- Linear Frequency Sweep
- Adjustable Duty Cycle (0.1% to 99.9%)
- Two or Four Level FSK Capability
- Wide Sweep Range (1000:1 Min)
- Logic Compatible Input and Output Levels
- Wide Supply Voltage Range (±4V to ±13V)
- Low Supply Sensitivity (0.15%/V)
- Wide Frequency Range (0.01 Hz to 1 MHz)
- Simultaneous Triangle and Squarewave Outputs

APPLICATIONS

- FSK Generation
- Voltage and Current-to-Frequency Conversion
- Stable Phase-Locked Loop
- Waveform Generation
  Triangle, Sawtooth, Pulse, Squarewave
- FM and Sweep Generation

SCHEMATIC DIAGRAM

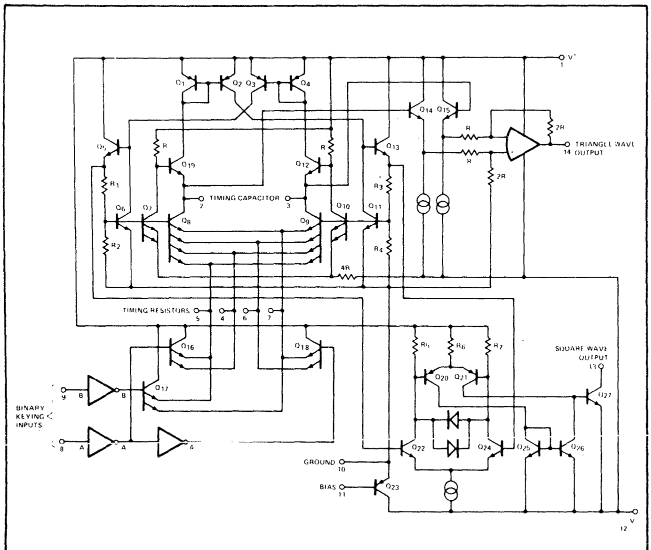
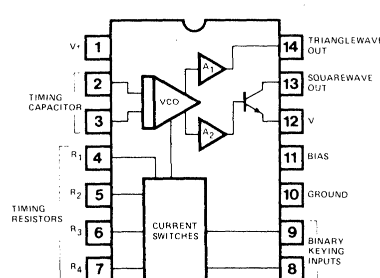


Figure 1. Functional Schematic Diagram

CONNECTION INFORMATION

DC and DB
Dual In-line Packages
(Top View)



Order Part Nos.:
XR-2207M, XR-2207CN
XR-2207CP, XR-2207N
XR-2207P

ELECTRICAL CHARACTERISTICS

Test circuit of Figure 2, $V^+ = V^- = 6V$, $T_A = +25°C = 5000$ pF, $R_1 = R_2 = R_3 = R_4 = 20$ KΩ, $R_L = 4.7$ KΩ, Binary inputs grounded, S_1 and S_2 closed unless otherwise specified.

PARAMETERS	CONDITIONS	XR-2207 MIN.	XR-2207 TYP.	XR-2207 MAX.	XR-2207C MIN.	XR-2207C TYP.	XR-2207C MAX.	UNITS
GENERAL CHARACTERISTICS								
Supply Voltage								
Single Supply	See Typical Electrical Data	8	12	26	8	12	26	V
Split Supplies		±4	±6	±13	±4	±6	±13	V
Supply Current								
Single Supply	Measured at pin 1, S_1 open See Figure 2		5	7		5	8	mA
Split Supplies								
Positive	Measured at pin 1, S_1 open		5	7		5	8	mA
Negative	Measured at pin 12, S_1, S_2 open		4	6		4	7	mA
OSCILLATOR SECTION – FREQUENCY CHARACTERISTICS								
Upper Frequency Limit	C = 500 pF, R_3 = 2 KΩ	0.5	1.0		0.5	1.0		MHz
Lower Practical Frequency	C = 50 μF, R_3 = 2 MΩ		0.01			0.01		Hz
Frequency Accuracy			±1	±3		±1	±5	% of f_o
Frequency Matching			0.5			0.5		% of f_o
Frequency Stability								
Temperature	$0° < T_A < 75°C$		20	50		30		ppm/°C
Power Supply			0.15			0.15		%/V
Sweep Range	R_3 = 1.5 KΩ for f_{H1} R_3 = 2 MΩ for f_L	1000:1	1000:1			1000:1		fH/fL
Sweep Linearity	C = 5000 pF							%
10:1 sweep	f_H = 10 kHz, f_L = 1 kHz		1	2		1.5		
1000:1 Sweep	f_H = 100 kHz, f_L = 100 kHz		5			5		
FM Distortion	±10% FM Deviation		0.1			0.1		%
Recommended Range of Timing Resistors	See Characteristic Curves	1.5		2000	1.5		2000	KΩ
Impedance at Timing Pins	Measured at pins 4, 5, 6, or 7		75			75		Ω
DC Level at Timing Terminals			10			10		mV
BINARY KEYING INPUTS								
Switching Threshold	Measured at pins 8 and 9. Refer to pin 10	1.4	2.2	2.8	1.4	2.2	2.8	V
Input Impedance			5			5		KΩ
OUTPUT CHARACTERISTICS								
Triangle Output	Measured at pin 13							
Amplitude		4	6		4	6		Vpp
Impedance			10			10		Ω
DC Level	Referenced to pin 10 from 10%		+100			+100		mV
Linearity	to 90% of swing		0.1			0.1		%
Squarewave Output	Measured at pin 13, S_5 closed							
Amplitude		11	12		11	12		Vpp
Saturation Voltage	Referenced to pin 12		0.2	0.4		0.2	0.4	V
Rise Time	$C_L \leq 10$ pF		200			200		nsec
Fall Time	$C_L \leq 10$ pF		20			20		nsec

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation (package limitation)	
Ceramic Package	750 mW
Derate above +25°C	6.0 mW/°C
Plastic Package	625 mW
Derate above +25°C	5 mW/°C
Storage Temperature Range	-65°C to +150°C

DESCRIPTION OF CIRCUIT CONTROLS

TIMING CAPACITOR (PINS 2 AND 3)

The oscillator frequency is inversely proportional to the timing capacitor, C. The minimum capacitance value is limited by stray capacitances and the maximum value by physical size and leakage current considerations. Recommended values range from 100 pF to 100 μF. The capacitor should be non-polarized.

TIMING RESISTORS (PINS 4, 5, 6, AND 7)

The timing resistors determine the total timing current, I_T, available to charge the timing capacitor. Values for timing resistors can range from 1.5 KΩ to 2 MΩ; however, for optimum temperature and power supply stability, recommended values are 4 KΩ to 200 KΩ. To avoid parasitic pick up, timing resistor leads should be kept as short as possible. For noisy environments, unused or deactivated timing terminals should be bypassed to ground through 0.1 μF capacitors. Otherwise, they may be left open.

SUPPLY VOLTAGE (PINS 1 AND 12)

The XR-2207 is designed to operate over a power supply range of ±4V to ±13V for split supplies, or 8V to 26V for single supplies. At high supply voltages, the frequency sweep range is reduced. Performance is optimum for ±6V, or 12V single supply operation.

BINARY KEYING INPUTS (PINS 8 AND 9)

The internal impedance at these pins is approximately 5 KΩ. Keying levels are $<$1.4V for "zero" and $>$3V for "one" logic levels referenced to the dc voltage at pin 10.

BIAS FOR SINGLE SUPPLY (PIN 11)

For single supply operations, pin 11 should be externally biased to a potential between $V^+/3$ and $V^+/2$ volts (see Figure 2). The bias current at pin 11 is nominally 5% of the total oscillation timing current I_T.

GROUND (PIN 10)

For split supply operation, this pin serves as circuit ground. For single supply operation, pin 10 should be ac grounded through a 1 μF bypass capacitor. During split supply operation, a ground current of 2 I_T flows out of this terminal, where I_T is the total timing current.

SQUAREWAVE OUTPUT (PIN 13)

The squarewave output at pin 13 is a "open-collector" stage capable of sinking up to 20 mA of load current. R_L serves as a pull-up load resistor for this output. Recommended values for R_L range from 1 KΩ to 100 KΩ.

TRIANGLE OUTPUT (PIN 14)

The output at pin 14 is a triangle wave with a peak swing of approximately one-half of the total supply voltage. Pin 14 has a very low output impedance of 10 Ω and is internally protected against short circuits.

Note: *Triangle waveform linearity is sensitive to parasitic coupling between the square and the triangle-wave outputs (pins 13 and 14). In board layout or circuit wiring care should be taken to minimize stray wiring capacitance between these pins.*

OPERATING INSTRUCTIONS

PRECAUTIONS

The following precautions should be observed when operating the XR-2207 family of integrated circuits:

1. Pulling excessive current from the timing terminals will adversely effect the temperature stability of the circuit. To minimize this disturbance, it is recommended that the *total current* drawn from pins 4, 5, 6, and 7 be limited to ≤6 mA. In addition, permanent damage to the device may occur if the total timing current exceeds 10 mA.
2. Terminals 2, 3, 4, 5, 6, and 7 have very low internal impedance and should, therefore, be protected from accidental shorting to ground or the supply voltages.
3. The keying logic pulse amplitude should not exceed the supply voltage.

RAYTHEON

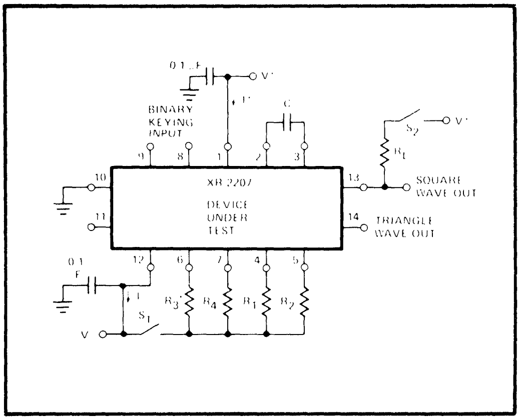


Figure 2. Test Circuit for Split Supply Operation

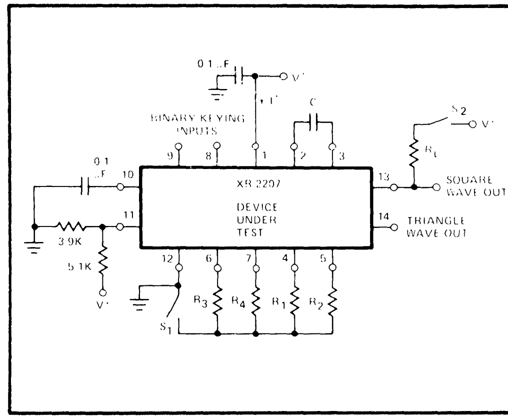
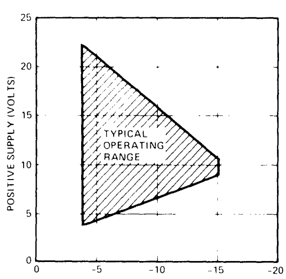
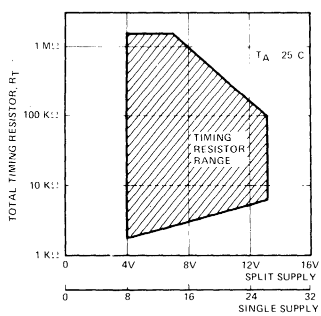


Figure 3. Test Circuit for Single Supply Operation

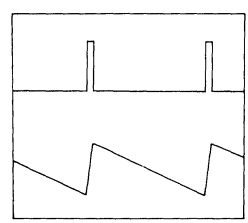
TYPICAL PERFORMANCE DATA



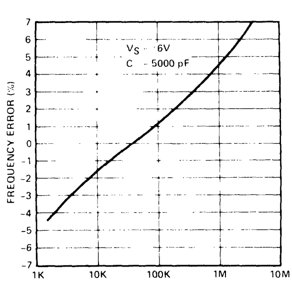
Typical Operating Range for Split Supply Voltage



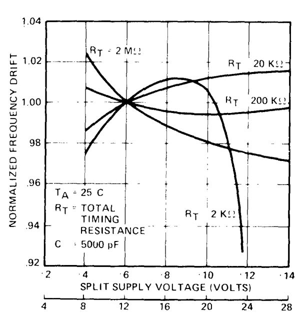
*Recommended Timing Resistor Value vs Power Supply Voltage**



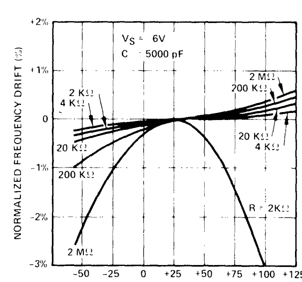
Pulse and Sawtooth Outputs



Frequency Accuracy vs. Timing Resistance



Frequency Drift vs. Supply Voltage



Normalized Frequency Drift with Temperature

***Note:** R_T *= Parallel Combination of Activated Timing Resistors*

SPLIT SUPPLY OPERATION

Figure 2 is the recommended circuit connection for split supply operation. The frequency of operation is determined by the timing capacitor, C, and the activated timing resistors (R_1 through R_4). The timing resistors are activated by the logic signals at the binary keying inputs (pins 8 and 9), as shown in the logic table below. If a single timing resistor is activated, the frequency is 1/RC. Otherwise, the frequency is either $1/(R_1 \parallel R_2)C$ or $1/(R_1 \parallel R_4)C$.

The squarewave output is obtained at pin 13 and has a peak-to-peak voltage swing equal to the supply voltages. This output is an "open-collector" type and requires an external pull-up load resistor (nominally 5 KΩ) to the positive supply. The triangle waveform obtained at pin 14 is centered about ground and has a peak amplitude of $V^+/2$.

The circuit operates with supply voltages ranging from ±4V to ±13V. Minimum drift occurs with ±6 volt supplies. For operation with unequal supply voltages, see page 4.

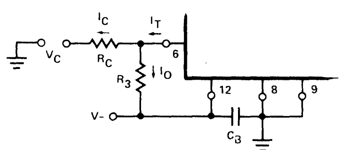


Figure 4. Frequency Sweep Operation

Table 1. Logic Table for Binary Keying Controls

LOGIC LEVEL 8	9	SELECTED TIMING PINS	FRE-QUENCY	DEFINITIONS
0	0	6	f_1	$f_1 = 1/R_3C$, $\Delta f_1 = 1/R_4C$
0	1	6 and 7	$f_1 + \Delta f_1$	$f_2 = 1/R_2C$, $\Delta f_2 = 1/R_1C$
1	0	5	f_2	Logic Levels: 0 = Ground
1	1	4 and 5	$f_2 + \Delta f_2$	1 = > 3 V

Note: *For single-supply operation, logic levels are referenced to voltage at pin 10.*

SINGLE SUPPLY OPERATION

The circuit should be interconnected as shown in Figure 3 for single-supply operation. Pin 12 should be grounded, and pin 11 biased from V^+ through a resistive divider to a value of bias voltage between $V^+/3$ and $V^+/2$. Pin 10 is bypassed to ground through a 0.1 μF capacitor.

For single-supply operation, the dc voltage at pin 10 and the timing terminals (pins 4 through 7) are equal and approximately 0.6V above V_B, the bias voltage at pin 11. The logic levels at the binary keying terminals are referenced to the voltage at pin 10.

ON – OFF KEYING

The XR-2207 can be keyed on and off by simply activating an open circuited timing pin. Under certain conditions, the circuit may exhibit very low frequency (<1 Hz) residual oscillation in the "off" state due to internal bias current. If this effect is undesirable, it can be eliminated by connecting a 10 MΩ resistor from pin 3 to V^+.

FREQUENCY CONTROL (SWEEP AND FM)

The frequency of operation is controlled by varying the total timing current, I_T, drawn from the activated timing pins 4, 5, 6, or 7. The timing current can be modulated by applying a control voltage, V_C, to the activated timing pin through a series resistor R_C as shown in Figure 4.

For split supply operation, a *negative* control voltage, V_C, applied to the circuits of Figure 4 causes the total timing current, I_T, and the frequency, to increase.

As an example, in the circuit of Figure 4, the binary keying inputs are grounded. Therefore, only timing pin 6 is activated.

The frequency of operation is determined by:

$$f = \frac{1}{R_3C_B}\left[1 - \frac{V_CR_3}{R_CV^-}\right] \text{Hz}$$

PULSE AND SAWTOOTH OPERATION

The duty cycle of the output waveforms can be controlled by frequency shift keying at the end of every half cycle of oscillator output. This is accomplished by connecting one or both of the binary keying inputs (pins 8 or 9) to the squarewave output at pin 13. The output waveforms can then be converted to positive or negative pulses and sawtooth waveforms.

Figure 5 is the recommended circuit connection for duty cycle control. Pin 8 is shorted to pin 13 so that the circuit switches between the "0, 0" and the "1, 0" logic states given in Table 1. Timing pin 5 is activated when the output is "high", and pin 6 is activated when the squarewave output goes to a "low" state.

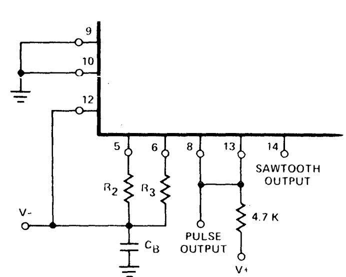


Figure 5. Pulse and Sawtooth Generation

The duty cycle of the output waveforms is given as:

$$\text{Duty Cycle} = \frac{R_2}{R_2 + R_3}$$

and can be varied from 0.1% to 99.9% by proper choice of timing resistors. The frequency of oscillation, f, is given as:

$$f = \frac{2}{C}\left[\frac{1}{R_2 + R_3}\right]$$

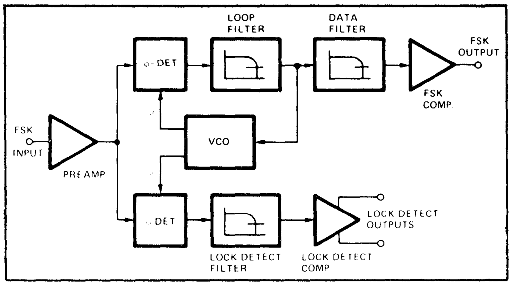
The frequency can be modulated or swept without changing the duty cycle by connecting R_2 and R_3 to a common control voltage V_C instead of to V^-. The sawtooth and the pulse output waveforms are shown in the Typical Electrical Data.

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2207M	Ceramic	-55°C to +125°C
XR-2207CN	Ceramic	0°C to +75°C
XR-2207CP	Plastic	0°C to +75°C
XR-2207N	Ceramic	-40°C to +85°C
XR-2207P	Plastic	-40°C to +85°C

DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth, and output delay.



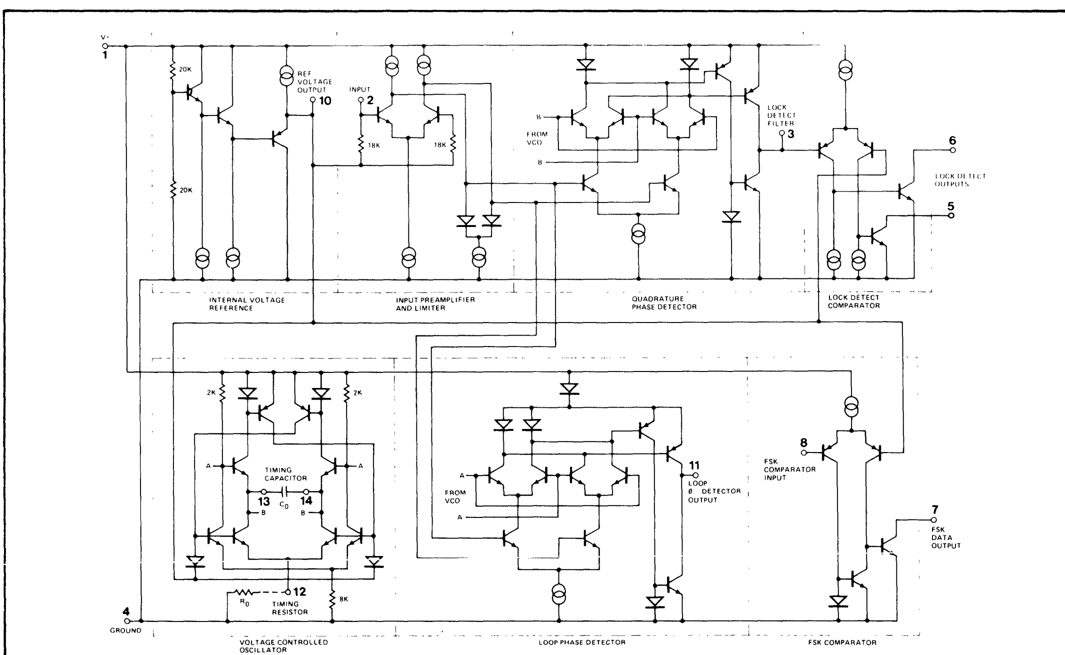
FEATURES

- Wide Frequency Range (0.01 Hz to 300 kHz)
- Wide Supply Voltage Range (4.5V to 20V)
- DTL/TTL/ECL Logic Compatibility
- FSK Demodulation with Carrier-Detection
- Wide Dynamic Range (2 mV to 3V rms)
- Adjustable Tracking Range (±1% to ±80%)
- Excellent Temperature Stability (20 ppm/°C, typical)

APPLICATIONS

- FSK Demodulation
- Data Synchronization
- Tone Decoding
- FM Detection
- Carrier Detection

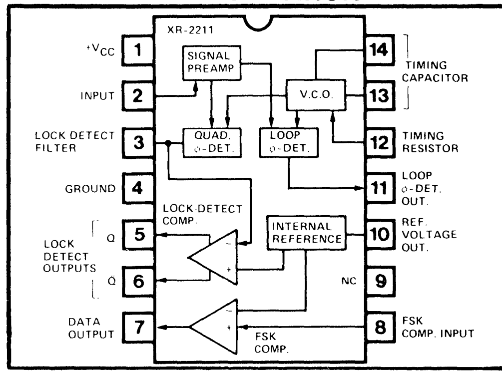
SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Power Supply 20V
Input Signal Level . . . . 3V rms
Power Dissipation
  Ceramic Package . . . . 750 mW
    Derate above T_A = +25°C . . . . 6 mW/°C
  Plastic Package . . . . 625 mW
    Derate above T_A = +25°C . . . . 5 mW/°C

CONNECTION INFORMATION

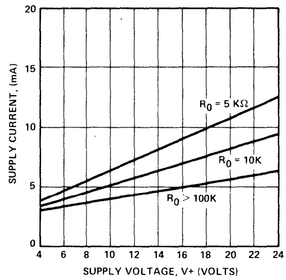


ELECTRICAL CHARACTERISTICS

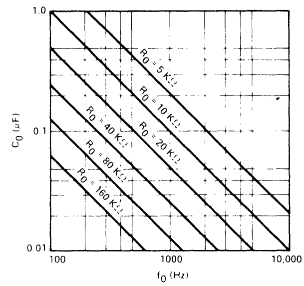
Test Conditions (see Figure 2):
V^+ = +12V, T_A = +25°C, R_0 = 30 KΩ, C_0 = 0.033 μF.

PARAMETER	CONDITIONS	XR-2211/2211M MIN.	XR-2211/2211M TYP.	XR-2211/2211M MAX.	XR-2211C MIN.	XR-2211C TYP.	XR-2211C MAX.	UNITS
GENERAL								
Supply Voltage		4.5		20	4.5		20	V
Supply Current	$R_0 \geq$ 10 KΩ. See Fig. 4.		4	7		5	9	mA
OSCILLATOR								
Frequency Accuracy	Deviation from $f_0 = 1/R_0C_0$		±1	±3		±1		%
Frequency Stability	$R_1 = \infty$							
Temperature Coefficient	See Fig. 8.		±20	±50		±20		ppm/°C
Power Supply Rejection	V^+ = 12 ±1V. See Fig. 7.		0.05	0.5		0.05		%/V
	V^+ = 5 ±0.5V. See Fig. 7.		0.2			0.2		%/V
Upper Frequency Limit	R_0 = 8.2 KΩ, C_0 = 400 pF	100	300			300		kHz
Lowest Practical Operating Frequency	R_0 = 2 MΩ, C_0 = 50 μF			0.01		0.01		Hz
Timing Resistor, R_0	See Fig. 5							
Operating Range		5		2000	5		2000	KΩ
Recommended Range	See Fig. 7 and 8.	15		100	15		100	KΩ
LOOP PHASE DETECTOR								
Peak Output Current	Measured at pin 11.	±150	±200	±300	±100	±200	±300	μA
Output Offset Current			±1			±2		μA
Output Impedance			1			1		MΩ
Maximum Swing	Referenced to pin 10.	±4	±5		±4	±5		V
QUADRATURE PHASE DETECTOR								
Peak Output Current	Measured at pin 3.	100	150			150		μ
Output Impedance			1			1		MΩ
Maximum Swing			11			11		Vpp
INPUT PREAMP								
Input Impedance	Measured at pin 2.		20			20		KΩ
Input Signal Voltage Required to Cause Limiting			2	10		2		mV rms
VOLTAGE COMPARATOR								
Input Impedance	Measured at pins 3 and 8.		2			2		MΩ
Input Bias Current			100			100		nA
Voltage Gain	R_L = 5.1 KΩ	55	70		55	70		dB
Output Voltage Low	I_C = 3 mA		300			300		mV
Output Leakage Current	V_0 = 12V		.01			.01		μA
INTERNAL REFERENCE								
Voltage Level	Measured at pin 10.	4.9	5.3	5.7	4.75	5.3	5.85	V
Output Impedance			100			100		Ω

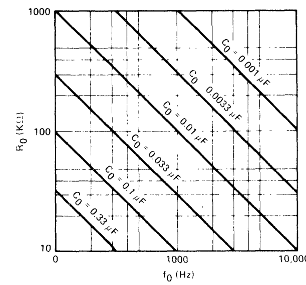
TYPICAL PERFORMANCE DATA



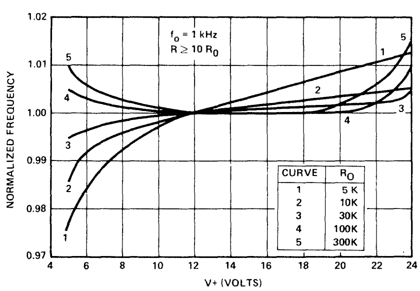
Typical Supply Current vs V^+ (Logic Outputs Open Circuited)



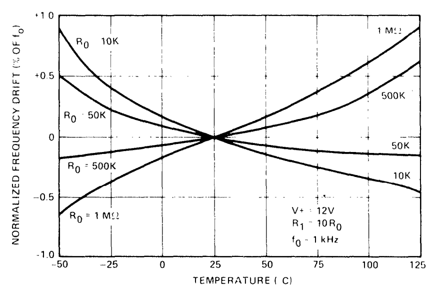
VCO Frequency vs Timing Resistor



VCO Frequency vs Timing Capacitor



Typical f_0 vs Power Supply Characteristics



Typical Center Frequency Drift vs Temperature

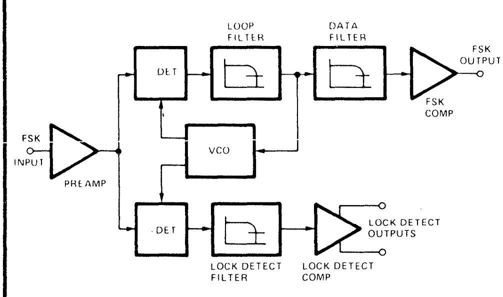


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211.

DESCRIPTION OF CIRCUIT CONTROLS

SIGNAL INPUT (PIN 2)

Signal is ac coupled to this terminal. The internal impedance at pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mV rms to 3V rms.

QUADRATURE PHASE DETECTOR OUTPUT (PIN 3)

This is the high-impedance output of quadrature phase detector, and is internally connected to the input of lock-detect voltage-comparator. In tone-detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 2) to eliminate the chatter at lock-detect outputs. If this tone-detect section is not used, pin 3 can be left open circuited.

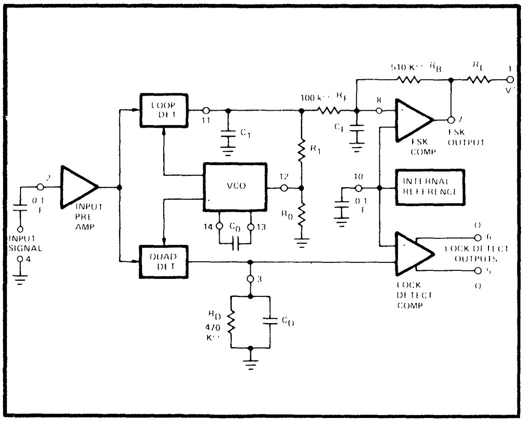


Figure 2. Generalized Circuit Connection for FSK and Tone Detection

LOCK-DETECT OUTPUT, Q (PIN 5)

The output at pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open-collector type output and requires a pull-up resistor, R_L, to V^+ for proper operation. At "low" state, it can sink up to 5 mA of load current.

LOCK-DETECT COMPLEMENT, $\overline{Q}$ (PIN 6)

The output at pin 6 is the logic complement of the lock-detect output at pin 5. This output is also an open-collector type stage which can sink 5 mA of load current at low or "on" state.

FSK DATA OUTPUT (PIN 7)

This output is an open-collector logic stage which requires a pull-up resistor, R_L, to V^+ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or off state for low input frequency; and at "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

FSK COMPARATOR INPUT (PIN 8)

This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (pin 11). This data filter is formed by R_F and C_F of Figure 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available for pin 10.

REFERENCE VOLTAGE, V_R (PIN 10)

This pin is internally biased at the reference voltage level, V_R; $V_R = V^+/2 - 650$ mV. The dc voltage level at this pin forms an internal reference for the voltage levels at pins 3, 8, 11 and 12. Pin 10 must be bypassed to ground with a 0.1 μF capacitor, for proper operation of the circuit.

LOOP PHASE DETECTOR OUTPUT (PIN 11)

This terminal provides a high-impedance output for the loop phase-detector. The PLL loop filter is formed by R_1 and C_1 connected to pin 11 (see Figure 2). With no input signal, or with no phase-error within the PLL, the dc level at pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

VCO CONTROL INPUT (PIN 12)

VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

where C_0 is the timing capacitor across pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ (see Typical Electrical Data).

This terminal is a low-impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from pin 12 must be limited to $\leqslant$3mA for proper operation of the circuit.

VCO TIMING CAPACITOR (PINS 13 AND 14)

VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals. C_0 must be non-polar, and in the range of 200 pF to 10 μF

VCO FREQUENCY ADJUSTMENT

VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at pin 12 (see Figure 3).

VCO FREE-RUNNING FREQUENCY, f_o.

The XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for set-up or adjustment purposes, VCO free-running frequency can be measured at pin 3 (with C_D disconnected), with no input and with pin 2 shorted to pin 10.

DESIGN EQUATIONS

See Figure 2 for Definitions of Components.

1. VCO Center Frequency, f_0:

   $f_0 = 1/R_0C_0$ Hz

2. Internal Reference Voltage, V_R (measured at pin 10)

   $V_R = V^+/2 - 650$ mV

3. Loop Lowpass Filter Time Constant, τ:

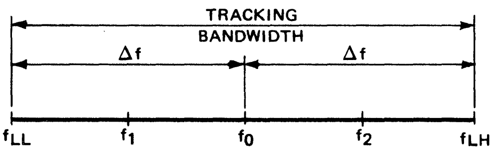
   $\tau = R_1C_1$

4. Loop Damping, ζ:

   $$\zeta = 1/4\sqrt{\frac{C_0}{C_1}}$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:

   $\Delta f/f_0 = R_0/R_1$



6. FSK Data Filter Time Constant, τ_F:

   $\tau_F = R_FC_F$

7. Loop Phase Detector Conversion Gain, K_ϕ: (K_ϕ is the differential dc voltage across pins 10 and 11, per unit of phase error at phase-detector input):

   $K_\phi = -2V_R/\pi$ volts/radian

8. VCO Conversion Gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at pin 11):

   $K_0 = -1/V_RC_0R_1$ Hz/volt

9. Total Loop Gain, K_T:

   $K_T = 2\pi K_\phi K_0 = 4/C_0R_1$ rad/sec/volt

10. Peak Phase-Detector Current, I_A:

    $I_A = V_R$ (volts)/25 mA

APPLICATIONS

FSK DECODING

Figure 3 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 3, the functions of external components are defined as follows: R_0 and C_0 set the PLL center frequency, R_1 sets the system bandwidth, and C_1 sets the loop-filter-time-constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510 KΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table 1.

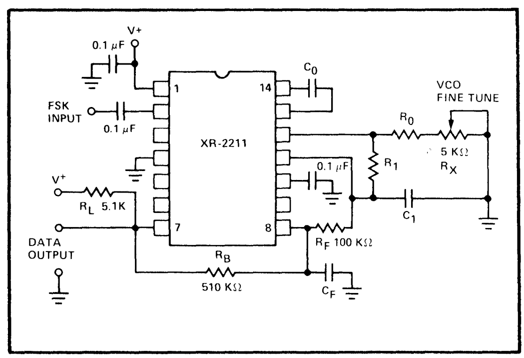


Figure 3. Circuit Connection for FSK Decoding

Design Instructions

The circuit of Figure 3 can be tailored for any FSK decoding application by the choice of five key circuit components; R_0, R_1, C_0, C_1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

1. Calculate PLL center frequency, f_0:

   $$f_0 = \frac{f_1 + f_2}{2}$$

2. Choose value of timing resistor R_0 to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary. The recommended value is $R_0 \cong 20$ KΩ. The final value of R_0 is normally fine-tuned with the series potentiometer, R_X.

3. Calculate value of C_0 from Design Equation No. 1 or from Typical Performance Data:

   $C_0 = 1/R_0f_0$

RAYTHEON

4. Calculate R_1 to give a Δf equal to the mark-space deviation:

   $R_1 = R_0 \; [f_0/f_1 - f_2)]$

5. Calculate C_1 to set loop damping. (See Design Equation No. 4.)

   Normally, $\zeta \approx 1/2$ is recommended.

   Then: $C_1 = C_0/4$ for $\zeta = 1/2$

6. Calculate Data Filter Capacitance, C_F:

   For $R_F = 100\ K\Omega$, $R_B = 510\ K\Omega$, the recommended value of C_F is:

   $C_F \approx 3/\text{Baud Rate})\ \mu F$

Note: *All calculated component values except R_0 can be rounded-off to the nearest standard value, and R_0 can be varied to fine-tune center frequency through a series potentiometer, R_X. (See Figure 3.)*

Design Example:

75 Baud FSK demodulator with mark/space frequencies of 1110/1170 Hz:

Step 1: Calculate f_0: $f_0 = (1110 + 1170)\ (1/2) = 1140$ Hz

Step 2: Choose $R_0 = 20\ K\Omega$ (18 $K\Omega$ fixed resistor in series with 5 $K\Omega$ potentiometer)

Step 3: Calculate C_0 from VCO Frequency vs Timing Capacitor: $C_0 = 0.044\ \mu F$

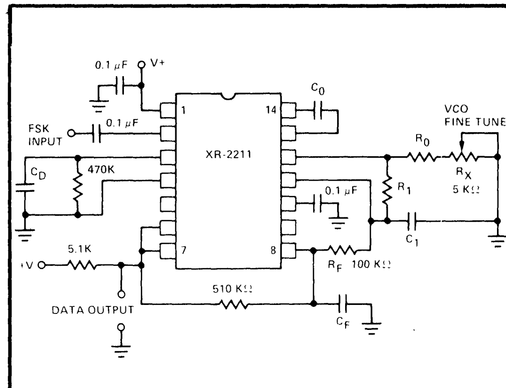
Step 4: Calculate R_1: $R_1 = R_0\ (2240/60) = 380\ K\Omega$

Step 5: Calculate C_1: $C_1 = C_0/4 = 0.011\ \mu F$

Note: *All values except R_0 can be rounded-off to nearest standard value.*

Table 1. Recommended Component Values for Commonly Used FSK Bands (See Circuit of Figure 3)

FSK BAND	COMPONENT VALUES	
300 Baud $f_1 = 1070$ Hz $f_2 = 1270$ Hz	$C_0 = 0.039\ \mu F$ $C_1 = 0.01\ \mu F$ $R_1 = 100\ K\Omega$	$C_F = 0.005\ \mu F$ $R_0 = 18\ K\Omega$
300 Baud $f_1 = 2025$ Hz $f_2 = 2225$ Hz	$C_0 = 0.022\ \mu F$ $C_1 = 0.0047\ \mu F$ $R_1 = 200\ K\Omega$	$C_F = 0.005\ \mu F$ $R_0 = 18\ K\Omega$



Note: Data output is "low" when no carrier is present.

Figure 4. External Connectors for FSK Demodulation with Carrier-Detect Capability

FSK DECODING WITH CARRIER-DETECT

The lock-detect section of the XR-2211 can be used as a carrier-detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 4. The open-collector lock-detect output, pin 6, is shorted to data output (pin 7). Thus, data output will be disabled at "low" state until there is a carrier within the detection band of the PLL and the pin 6 output goes "high" to enable the data output.

The minimum value of the lock-detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta f_c > \Delta f/2$. For $R_D = 470\ K\Omega$, the approximate minimum value of C_D can be determined by:

$$C_D\ (\mu F) \geqslant 16/\text{capture range in Hz.}$$

With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively-large values of C_D will slow the response time of the lock-detect output.

TONE DETECTION

Figure 5 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2}, as shown in Figure 5.

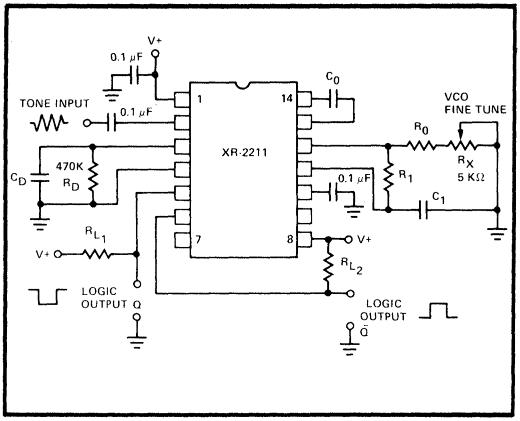


Figure 5. Circuit Connection for Tone Detection

With reference to Figures 2 and 5, the function of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the lowpass-loop filter time constant and the loop damping factor, R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\bar{Q}$ logic outputs.

Design Instructions

The circuit of Figure 5 can be optimized for any tone-detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input tone frequency, f_S, these parameters are calculated as follows:

1. Choose R_0 to be in the range of 15 KΩ to 100 KΩ. This choice is arbitrary.

2. Calculate C_0 to set center frequency, f_0 equal to f_S: $C_0 = 1/R_0f_S$.

3. Calculate R_1 to set bandwidth $\pm\Delta f$; (see Design Equation No. 5):

   $R_1 = R_0(f_0/\Delta f)$

Note: *The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.*

4. Calculate value of C_1 for a given loop damping factor:

   $C_1 = C_0/16\zeta^2$

Normally $\zeta \approx 1/2$ is optimum for most tone-detector applications, giving $C_1 = 0.25\ C_0$.

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

5. Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with R_D = 470 KΩ, C_D must be:

   C_D (μF) $\geqslant$ (16/capture range in Hz)

Increasing C_D slows the logic output response time.

Design Examples:

Tone detector with a detection band of 1 kHz ± 20 Hz:

Step 1: Choose R_0 = 20 KΩ (18 KΩ in series with 5 KΩ potentiometer).

Step 2: Choose C_0 for f_0 = 1 kHz:
$C_0 = 0.05\ \mu$F.

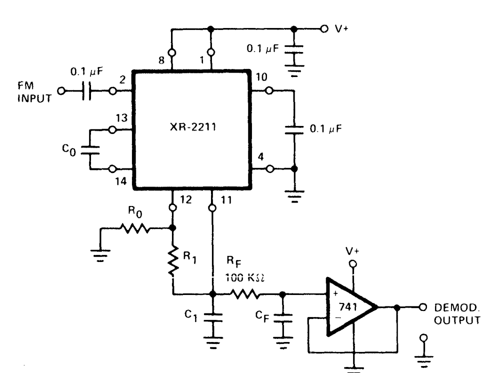
Step 3: Calculate R_1: $R_1 = (R_0)\ (1000/20) = 1$ MΩ.

Step 4: Calculate C_1: for $\zeta = 1/2$, $C_1 = 0.25\ \mu$F,
$C_0 = 0.013\ \mu$F.

Step 5: Calculate C_D: $C_D = 16/38 = 0.42\ \mu$F.

Step 6: Fine-tune center frequency with 5 KΩ potentiometer, R_X.

LINEAR FM DETECTION



Note: See section on Design Equations for Component Values.

Figure 6. Linear FM Detector Using XR-2211 and an External Op Amp

LINEAR FM DETECTION

The XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 6. . The demodulated output is taken from the loop phase detector output (pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 6.

The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$$V_{out} = R_1 V_R / 100 R_0 \text{ Volts/\%deviation}$$

where V_R is the internal reference voltage. ($V_R = V^+/2 - 650$ mV). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see section on Design Equations.

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	-55°C to +125°C
XR-2211N	Ceramic	-40°C to +85°C
XR-2211P	Plastic	-40°C to +85°C
XR-2211CN	Ceramic	0°C to +75°C
XR-2211CP	Plastic	0°C to +75°C

DESCRIPTION

The XR-2567 is a dual monolithic tone decoder of the 567-type that is ideally suited for tone or frequency decoding in multiple-tone communication systems. Each decoder of the XR-2567 can be used independently or both sections can be interconnected for dual operation. The matching and temperature tracking characteristics between decoders on this monolithic chip are superior to those available from two separate tone-decoder packages.

The XR-2567 operates over a frequency range of 0.01 Hz to 500 kHz. Supply voltages can vary from 4.5V to 12V, with internal voltage regulation provided for supplies between 7V and 12V. A functional block diagram of the complete monolithic system is shown below. Each decoder consists of a phase-locked loop (PLL), a quadrature AM detector, a voltage comparator, and a logic compatible output that can sink more than 100 mA of load current.

The center frequency of each decoder is set by an external resistor and capacitor which determine the free-running frequency of each PLL. When an input tone is present within the passband of the circuit, the PLL "locks" on the input signal. The logic output, which is normally "high", then switches to a "low" state during this "lock" condition.

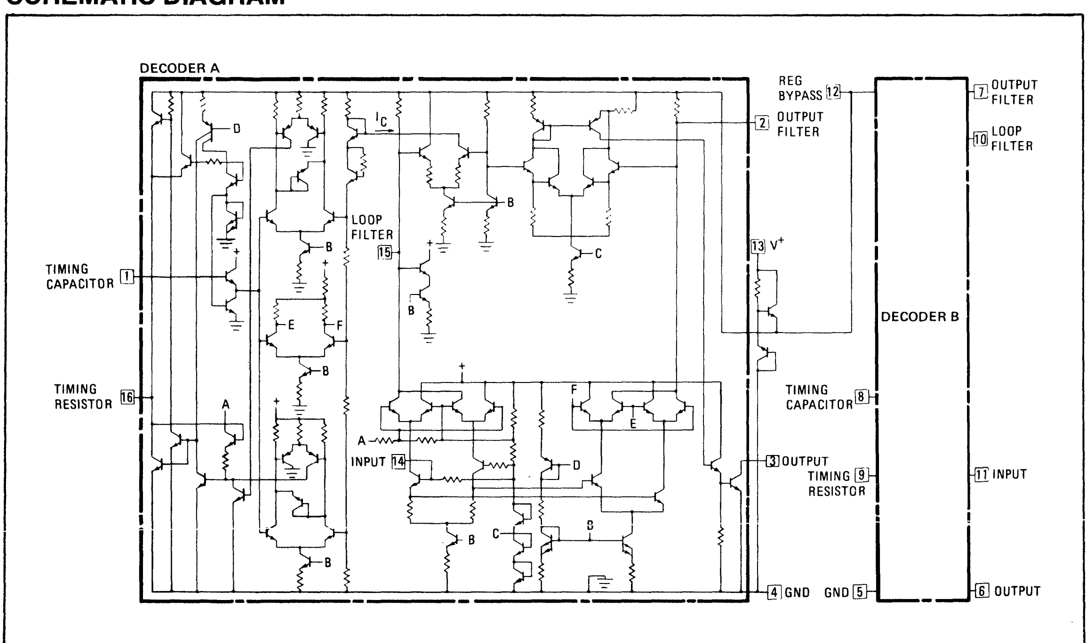
FEATURES

- Replaces two 567-type decoders
- Excellent temperature tracking between decoders
- Bandwidth adjustable from 0 to 14%
- Logic compatible outputs with 100 mA sink capability
- Center frequency matching (1% typical)
- Center frequency adjustable from 0.01 Hz to 500 kHz
- Inherent immunity to false triggering
- Frequency range adjustable over 20:1 range by external resistor

APPLICATIONS

- Touch-Tone® Decoding
- Sequential Tone Decoding
- Dual-Tone Decoding/Encoding
- Communications Paging
- Ultrasonic Remote-Control and Monitoring
- Full-Duplex Carrier-Tone Transceiver
- Wireless Intercom
- Dual Precision Oscillator
- FSK Generation and Detection

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V, T_A = 25°C, unless otherwise specified.

Test circuit of Figure 1, S_1 closed unless otherwise specified.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
GENERAL					
Supply Voltage Range					
Without Regulator	See Figure 1, S_1 closed	4.75		7	Vdc
With Internal Regulator	See Figure 1, S_1 open	6.5		12	Vdc
Supply Current (both decoders)	See Typical Performance Data				
Quiescent XR-2567M	R_L = 20 KΩ		12	16	mA
XR-2567C	R_L = 20 KΩ		14	20	mA
Activated XR-2567M	R_L = 20 KΩ		22	26	mA
XR-2567C	R_L 20 KΩ		24	30	mA
Output Voltage				15	V
Negative Voltage at Input				-10	V
Positive Voltage at Input				V_{CC}+0.5	V
CENTER FREQUENCY*					
Highest Center Frequency		100	500		kHz
Center Frequency Stability					
Temperature T_A = 25°C	See Typical Performance Data		35		ppm/°C
$0 < T_A < +75°C$	See Typical Performance Data		±60		ppm/°C
$-55° < T_A < +125°C$	See Typical Performance Data		±140		ppm/°C
Supply Voltage					
Without Regulator XR-2567M	f_o = 100 kHz		0.5	1.0	%/V
XR-2567C	f_o = 100 kHz		0.7	2.0	%/V
With Internal Regulator XR-2567M	f_o = 100 kHz, V+ = 9V		0.05		%/V
XR-2567C	f_o = 100 kHz, V+ = 9V		0.1		%/V
DETECTION BANDWIDTH*					
Largest Detection Bandwidth XR-2567M	f_o = 100 kHz	12	14	16	% of f_o
XR-2567C	f_o = 100 kHz	10	14	18	% of f_o
Largest Detection Bandwidth Skew					
XR-2567M			1	2	% of f_o
XR-2567C			1	3	% of f_o
Largest Detection Bandwidth Variation					
Temperature	V_{in} = 300 mV rms		± 0.1		%/°C
Supply Voltage	V_{in} = 300 mV rms		± 2		%/V
INPUT*					
Input Resistance			20		kΩ
Smallest Detectable Input Voltage	I_L = 100 mA, $f_i = f_o$		20	25	mV rms
Largest No-Output Input Voltage	I_L = 100 mA, $f_i = f_o$	10	15		mV rms
Greatest Simultaneous Outband Signal to Inband Signal Ratio			+6		dB
Minimum Input Signal to Wideband Noise Ratio	Noise Bw = 140 kHz		-6		dB
OUTPUT*					
Output Saturation Voltage	I_L = 30 mA, V_{in} = 25 mV rms		0.2	0.4	V
	I_L = 100 mA, V_{in} = 25 mV rms		0.6	1.0	V
Output Leakage Current			0.01	25	μA
Fastest ON-OFF Cycling Rate			fo/20		
Output Rise Time	R_L = 50Ω		150		ns
Output Fall Time	R_L = 50Ω		30		ns
MATCHING CHARACTERISTICS					
Center Frequency Matching	f_o = 10 kHz		1		%
Temperature Drift Matching	$0°C < T_A < 75°C$		±20		ppm/°C
	$-55°C < T_A < 125°C$		±50		ppm/°C

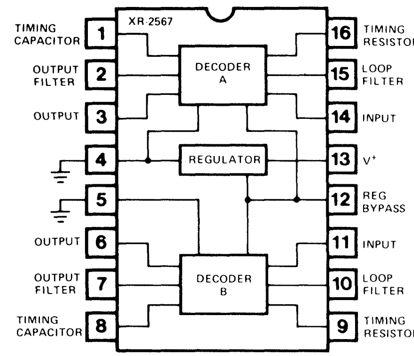
* Each decoder section.

ABSOLUTE MAXIMUM RATINGS

Power Supply	
With Internal Regulator	14V
Without Regulator (Pins 12 and 13 shorted)	10V
Power Dissipation	
Ceramic Package	750 mW
Derate above +25°C	6 mW/°C
Plastic Package	625 mW/°C
Derate above +25°C	5 mW/°C
Temperature	
Operating: 2567M	-55°C to +125°C
2567C	0°C to +75°C
Storage	-65°C to +150°C

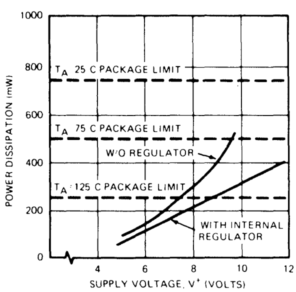
CONNECTION INFORMATION

DD and MB
Dual In-Line Packages
(Top View)

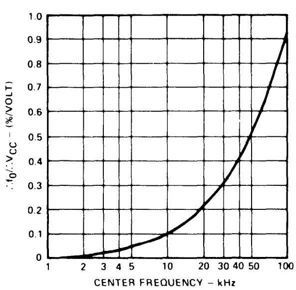


Order Part Nos.:
XR-2567M, XR-2567CN,
XR-2567CD

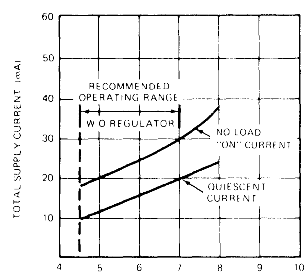
TYPICAL PERFORMANCE DATA



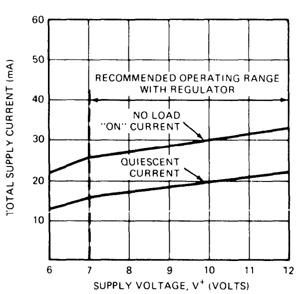
Internal Power Dissipation vs Supply Voltage. Both Units Activated, $R_L = 20\ K$



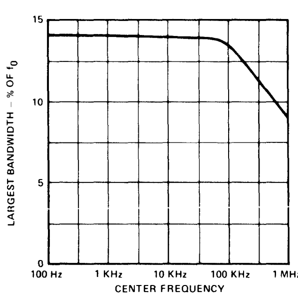
Power Supply Dependence of Center Frequency



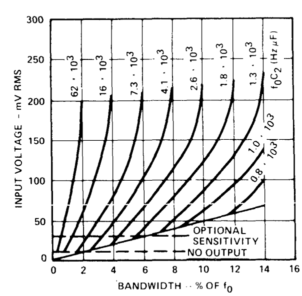
Total Supply Current vs Supply Voltage for Operation Without Internal Regulator (Pins 12 and 13 Shorted)



Total Supply Current vs Supply Voltage for Operation with Internal Regulator (Pins 12 and 13 Not Connected)

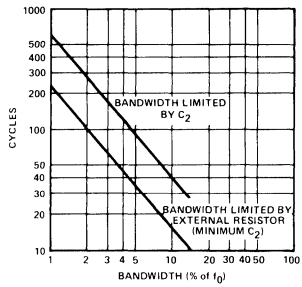


Largest Detection Bandwidth vs Operating Frequency

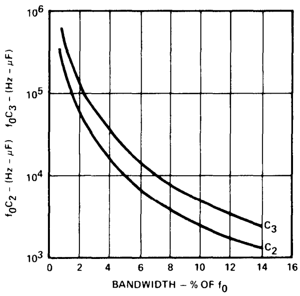


Bandwidth vs Input Signal Amplitude (C_2 in μF)

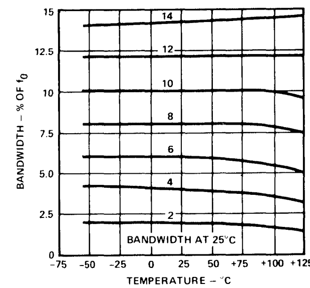
TYPICAL PERFORMANCE DATA (Cont)



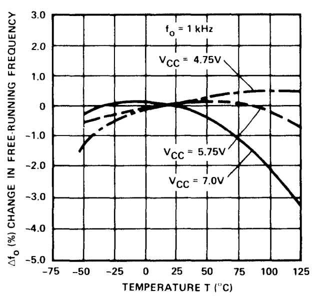
Greatest Number of Cycles Before Output



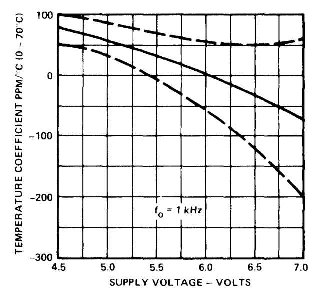
Detection Bandwidth as a Function of C_2 and C_3



Bandwidth Variation With Temperature



Frequency Drift With Temperature



Temperature Coefficient of Center Frequency (Mean and S.D.)

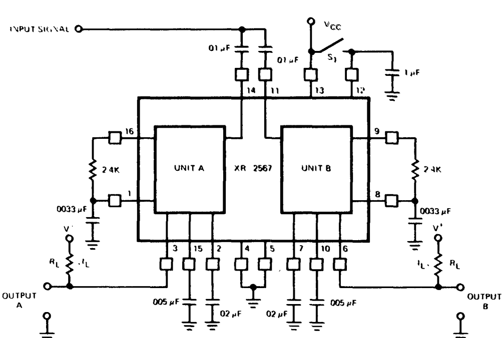
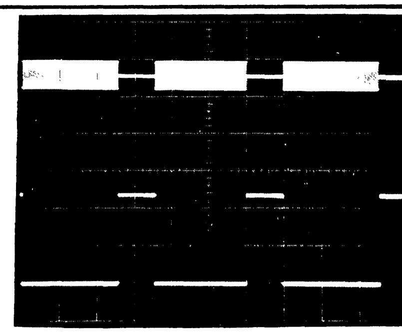


Figure 1. Test Circuit



Response to 100 mV rms tone burst.
R_L = 100 ohms.

Figure 2. XR-2567 Typical Response

DEFINITIONS OF THE XR-2567 PARAMETERS

The center frequency, f_0, is the *free-running frequency* of the current-controlled oscillator of the PLL with no input signal. It is determined by resistor R_1 and capacitor C_1; f_0 can be approximateed by

$$f_0 \approx \frac{1}{R_1C_1} \text{ Hz}$$

where R_1 is in ohms and C_1 is in farads.

The *detection bandwidth* is the frequency range centered about f_0, within which an input signal larger than the threshold voltage (typically 20 mV rms) will cause a "logic zero" state at the output. The detection bandwidth corresponds to the capture range of the PLL and is determined by the lowpass bandwidth filter. The bandwidth of the filter, as a percent of f_0, can be determined by the approximation

$$BW \approx 1070\sqrt{\frac{V_i}{f_0C_2}}$$

where V_i is the input signal in volts, rms, and C_2 is the capacitance in μF at pins 10 or 15.

The *largest detection bandwidth* is the largest frequency range within which an input signal above the threshold voltage will cause a logical zero state at the output. The maximum detection bandwidth corresponds to the lock range of the PLL.

The *detection band skew* is a measure of how accurately the largest detection band is centered about the center frequency f_0. It is defined as $(f_{max} + f_{min} - 2f_0)/f_0$, where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. If necessary, the detection band skew can be reduced to zero by an optional centering adjustment. (See Optional Controls.)

DESCRIPTION OF CIRCUIT CONTROLS

INPUT (PINS 11 AND 14)

The input signal is applied to pins 14 and/or 11 through a coupling capacitor, C_C. These terminals are internally biased at a dc level 2 volts above ground and they have an input impedance level of approximately 20 KΩ.

TIMING RESISTOR R_1 AND CAPACITOR C_1 (PINS 1, 8, 9, and 16)

The center frequency, f_0, of each decoder section is set by a resistor R_1 and a capacitor C_1. R_{1A} is connected between pins 1 and 16 in decoder section A, and R_{1B} between pins 8 and 9 of decoder section B. C_{1A} is connected from pin 1 to ground, and C_{1B} from pin 8 to ground, as shown in Figure 3. R_1 and C_1 should be selected for the desired center frequency by the expression $f_0 \approx 1/R_1C_1$. For optimum temperature stability, R_1 should be selected such that $2\text{ K}\Omega \leqslant R_1 \leqslant 20\text{ K}\Omega$, and the R_1C_1 product should have sufficient stability over the projected operating temperature range.

For decoder section A, the oscillator output can be obtained at either pin 1 or 16. Pin 16 is the oscillator squarewave output which has a magnitude of approximately V_{CC}-1.4V and an average dc level of $V_{CC}/2$. A 1 KΩ load may be driven from this point. The voltage at pin 1 is an exponential triangle waveform with a peak-to-peak amplitude of 1 volt and an average dc level of $V_{CC}/2$. Only high impedance loads should be connected to pin 1 to avoid disturbing the temperature stability or duty cycle of the oscillator. For section B, pin 9 is the squarewave output and pin 8 the exponential triangle waveform output.

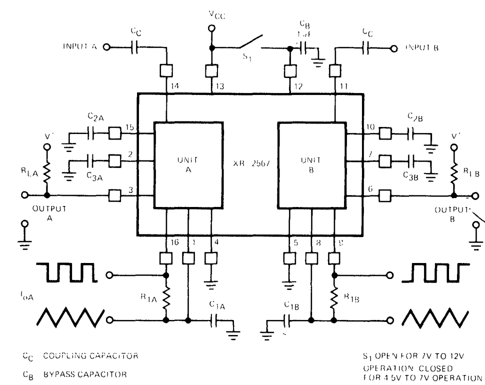


Figure 3. Circuit Connection Diagram

LOOP FILTER, C_2 (PINS 10 and 15)

Capacitors C_{2A} and C_{2B} connected from pins 15 and 10 to ground are the single-pole, lowpass filters for the PLL portion of decoder sections A and B. The filter time constant is given by $T_2 = R_2C_2$, where R_2 (10 KΩ) is the impedance at pins 10 or 15. The selection of C_2 is determined by the detection bandwidth requirements and input signal amplitude as shown in the Curves. One approach is to select an area of operation from the graph and then adjust the input level and value of C_2 accordingly. Or, if the input amplitude variation is known, the required f_0C_2 product can be found to give the desired bandwidth. Constant bandwidth operation requires $V_i > 200$ mV rms. Then, as noted in the Curves, bandwidth will be controlled solely by the f_0C_2 product. (For additional information, see Optional Controls Section, "Speed of Response" and "Bandwidth Reduction".)

Pins 10 and 15 correspond to the PLL phase detector outputs of sections A and B, respectively. The voltage level at these pins is a linear function of frequency over the range of 0.95 to 1.05 f_0, with a slope of approximately 20 mV/% frequency deviation.

OUTPUT FILTER, C_3 (PINS 2 AND 7)

Capacitors C_{3A} and C_{3B} connected from pins 2 and 7 to ground form lowpass post detection filters for sections A and B respectively. The function of the post detection filter is to eliminate spurious outputs caused by out-of-band signals. The time constant of the filter can be expressed as $T_3 = R_3C_3$, where R_3(4.7 K) is the internal impedance at pins 2 or 7.

The precise value of C_3 is not critical for most applications. To eliminate the possibility of false triggering by spurious signals, a minimum value for C_3 is $2C_2$, where C_2 is the loop filter capacitance for the corresponding decoder section. If C_3 is smaller than $2C_2$, then frequencies adjacent to the detection band may switch the output stage "off" and "on" at the beat frequency, or the output may pulse "off" and "on" during the turn-on transient.

If the value of C_3 becomes too large, the turn-on or turn-off time of the output stage will be delayed until the voltage change across C_3 reaches the threshold voltage. In certain applications, this delay may be desirable as a means of suppressing spurious outputs. (For additional information, see Optional Controls Section, "Speed of Response" and "Chatter".)

LOGIC OUTPUT (PINS 3 AND 6)

Output terminals 3 and 6 provide a binary logic output when an input signal tone is present within the detection-band of each respective decoder section. The logic outputs are uncommitted "bare-collector" power transistors capable of switching high current loads. The current level at the output is determined by an external load resistor, R_L, connected from V_{CC} to pins 3 and 6.

When an in-band signal is present, the output transistor at pins 3 or 6 saturates with a collector voltage less than 1 volt (typically 0.6V) at full rated current of 100 mA. If large output voltage swings are needed, R_L can be connected to a supply voltage, V^+ higher than the V_{CC} supply. For safe operation, $V^+ \leqslant 15$ volts.

REGULATOR BYPASS (PIN 12)

This pin corresponds to the output of the voltage regulator section. For circuit operation with a supply voltage greater than 7V, pin 12 should be ac grounded with a bypass capacitor $\geqslant 1\ \mu$F. For circuit operation over a supply voltage range of 4.5 to 7V, the voltage regulator section is not required; pin 12 should be shorted to V_{CC}.

GROUND TERMINALS (PINS 4 AND 5)

To eliminate parasitic interaction, each decoder section has a separate ground terminal. The internal regulator shares a common ground with decoder section A (pin 4).

Independent ground terminals also allow additional flexibility for split supply operation. Pin 4 can be used as V^-, and pin 5 as ground, as shown in Figure 4. When the circuit is operated with split supplies, the positive supply should always be $>$6V, and the dc potential across pins 13 and 14 should not exceed 15 volts.

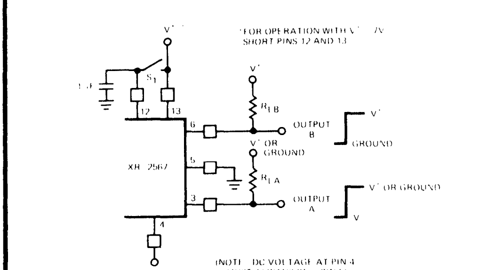


Figure 4. Split-Supply Operation Using Independent Ground Terminals of Units A and B. Unit A Operates Between V^+ and V^-, Unit B Operates Between V^+ and Ground

OPTIONAL CONTROLS

SPEED OF RESPONSE

The minimum lock-up time is inversely related to the loop frequency. As the natural loop frequency is lowered, the turn-on transient becomes greater. Thus, maximum operating speed is obtained when the value of capacitor C_2 is minimum. At the instant an input signal is applied, its phase may drive the oscillator away from the incoming frequency rather than toward it. Under this condition, the lock-up transient is in a worst case situation, and the minimum theoretical lock-up time will not be achievable.

The following expressions yield the values of C_2 and C_3, in microfarads, which allow the maximum operating speeds for various center frequencies. The minimum rate that digital information may be detected without losing information due to turn-on transient or output chatter is about 10 cycles/bit, which corresponds to an information transfer rate of $f_0/10$ Baud.

$$C_2 = \frac{130}{f_0}, \quad C_3 = \frac{260}{f_0}$$

In situations where minimum turn-off time is of less importance than fast turn-on, the optional sensitivity adjustment circuit of Figure 5 can be used to bring the quiescent C3 voltage closer to the threshold voltage. Sensitivity to beat frequencies, noise, and extraneous signals, however, will be increased.

CHATTER

When the value of C_3 is small, the lock transient and ac components at the lock detector output may cause the output stage to move through its threshold more than once, resulting in output chatter.

Although some loads, such as lamps and relays will not respond to chatter, "logic" may interpret chatter as a series of output signals. Chatter can be eliminated by feeding a portion of the output back to the input or by increasing the size of capacitor C_3. Generally, the feedback method is preferred since keeping C_3 small will enable faster operation. Three alternate schemes for chatter prevention are shown in Figure 6. Generally, it is only necessary to assure that the feedback time constant does not get so large that it prevents operation at the highest anticipated speed.

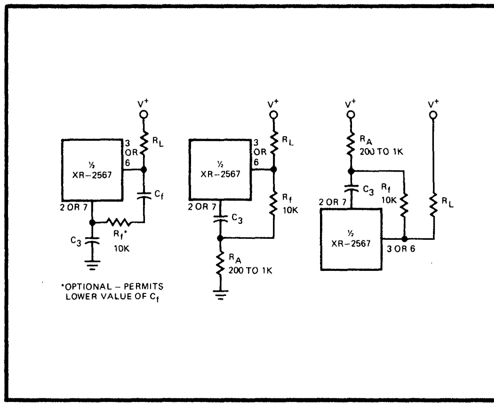


Figure 6. Methods of Reducing Chatter

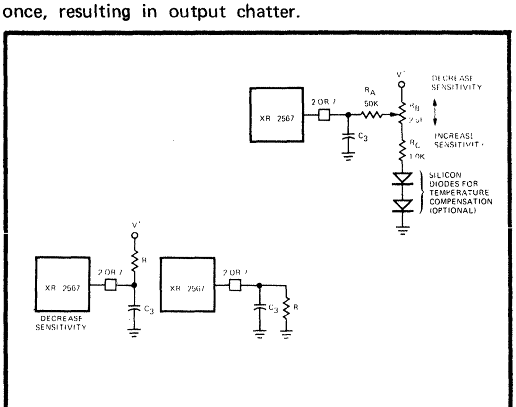


Figure 5. Optional Connections for Sensitivity Control

SKEW ADJUSTMENT

The circuits shown in Figure 7 can be used to change the position of the detection band (capture range) within the largest detection band (or loop range). By moving the detection band to either edge of the lock range, input signal variations will expand the detection band in one direction only. Since R_3 also has a slight effect on the duty cycle, this approach may be useful to obtain a precise duty cycle when the circuit is used as an oscillator.

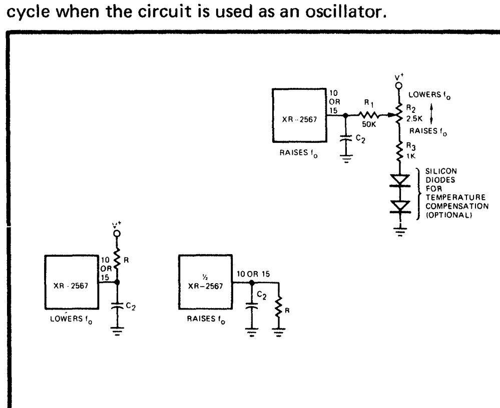


Figure 7. Connections to Reposition Detection Band

OUTPUT LATCHING

After a signal is received, the output of either decoder section can be latched "on" by connecting a 20 KΩ resistor and diode from the "output" terminal to the "output filter" terminal as shown in Figure 8. The output stage can be unlatched by raising the voltage level at the output filter terminal.

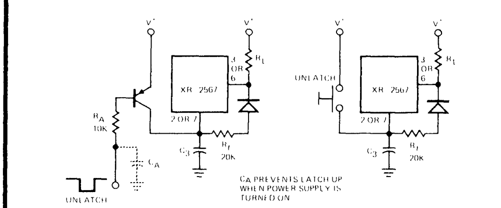
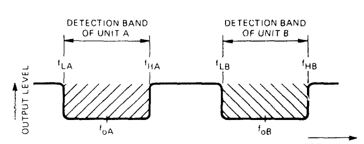


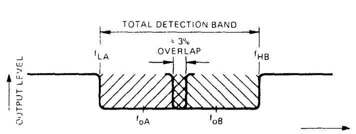
Figure 8. Output Latching

POSITIONING OF DETECTION BANDS

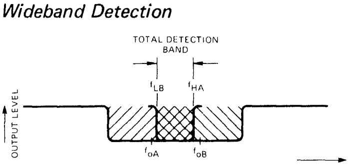
Figure 9 defines the respective band-edge and band-center frequencies for sections A and B of the dual tone decoder. Frequencies f_L and f_H with appropriate subscripts refer to the low and the high band-edge frequencies for decoder section A and B, and f_0 is the center frequency.



(a) Independent Detection of Two Separate Tones



(b) Addition of Detection Bandwidth for Wideband Detection



(c) Subtraction of Bandwidths for Narrow-Band Detection

Figure 9. Positioning of Detection Bands

The two sections can be interconnected to form a single-tone detector with an overall detection bandwidth equal to the sum of the difference of the detection bands for the two individual detector sections. For example, if the individual decoder sections are interconnected as shown in Figure 13, then the total detection bandwidth would be approximately equal to the sum of the respective bandwidths as shown in Figure 9 (b). Similarly, if the decoders are interconnected as shown in Figure 11, then the overall detection band would be equal to the difference, or the overlap, between the respective bandwidths as shown in Figure 9 (c).

BANDWIDTH REDUCTION

The bandwidth of each decoder can be reduced by either increasing the loop filter capacitor C_2 or reducing the loop gain. Increasing C_2 may be an undesirable solution since this will also reduce the damping of the loop and thus slow the circuit response time.

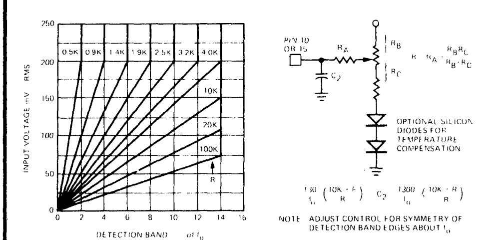


Figure 10. Bandwidth Reduction

Figure 10 shows the proper method of reducing the loop gain for reduced bandwidth. This technique will improve damping and permit faster performance under narrow band operation.

Bandwidth reduction can also be obtained by subtracting over-lapping bandwidths of the two decoder sections (see Figures 9 (c) and 11).

APPLICATIONS

DUAL-TONE DETECTION

In most dual-tone detection systems, the decoder output is required to change state only when both input tones are present simultaneously. This can be implemented by setting the detection bandwidth of each of the XR-2567 decoder sections to cover one of the input tones; and then connecting the respective outputs through a NOR gate, as shown in Figure 11. In this case, the output of the NOR gate will be "high" only when both input tones are present simultaneously.

Figure 12 shows additional circuit configurations which can be used for decoding multiple-tone input signals. In Figure 12 (a), the output of Unit A is connected to the output filter (pin 7) of Unit B through the diode D_1. If no input tone is present within the detection-band of Unit A, then its output (pin 3) is "high", which keeps diode D_1 conducting and "disables" Unit B by keeping its output (pin 6) "high". If an input tone is present within the detection-band of Unit A, pin 3 is low, diode D_1 is reverse biased, and decoder B is no longer disabled. If under these conditions an input signal is present within the detection-band of Unit B, then its output at pin 6 would be "low". Thus, the output at pin 6 is "low" only when input tones within the detection-band of A and B are present simultaneously.

The dual-tone decoder circuit of Figure 12 (b) makes use of the split-ground feature of the XR-2567. The output terminal of Unit A is used as a "switch" in series with the ground terminal (pin 5) of Unit B. If the input tone A is not present, pin 3 is at its high-impedance state, and the ground terminal of Unit B is open-circuited. When the input tone A is present, pin 3 goes to a low-impedance state and Unit B is activated. In this manner, the output of Unit B will be "low" *only* when both tones A and B are present.

In the circuit connection of Figure 12 (b), Unit B does not draw any current until it is activated. Therefore, its power dissipation in a stand-by condition is lower than other dual-tone decoder configurations. However, due to finite series resistance between pin 3 and ground when Unit B is activated, the output current sink capability is limited to $\leqslant$10 mA.

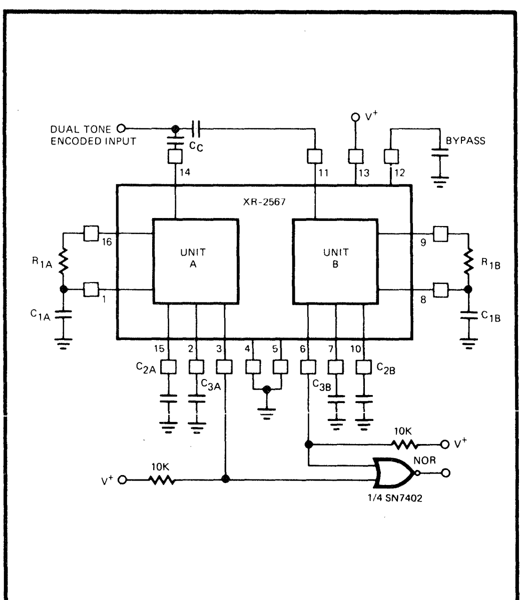


Figure 11. Connections for Decoding Dual-Tone Encoded Input Signals.

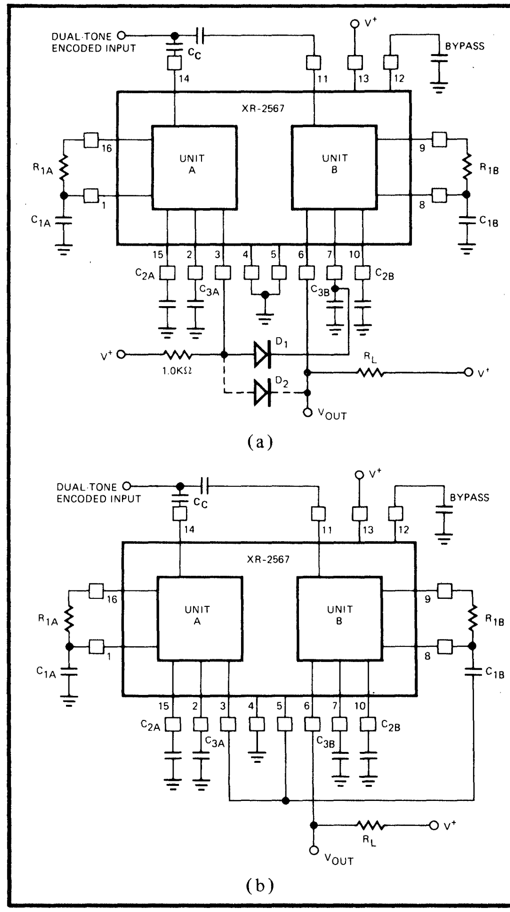


Figure 12. Additional Dual-Tone Decoding Circuits

SEQUENTIAL TONE DECODING

Dual-tone detector circuits can also be used for sequential tone decoding where one tone must be present before the other for the circuit to operate. This can be achieved by making the output filter capacitance, C_3, of one of the sections larger with respect to the other. For example, in the circuits of Figure 12 (a) and 13 (b), if C_{3A} is chosen to be much larger than C_{3B} ($C_{3A} \geqslant C_{3B}$), then Unit A will remain "on" and activate B for a finite time duration after tone A is terminated. Thus, the circuit will be able to detect the two tones only if they are present sequentially, with tone A preceding tone B.

The circuit of Figure 12 (a) can also be modified for sequential tone decoding by addition of a diode, D_2, between pins 3 and 6. Once activated by Unit A, Unit B will stay "on" as long as tone B is present, even though tone A may terminate. Once tone B disappears, the circuit is reset to its original state and would require tone A to be present for activation.

HIGH-SPEED NARROW-BAND TONE DECODER

The circuit of Figure 11 can be used as a narrow-band tone decoder by overlapping the detection bands of Units A and B (see Figure 9 (c)). The output of the NOR gate will be high only when an input signal is present within the overlapping portions of the detection band. To maintain uniform response within the passband, the input signal amplitude should be ⩾80 mV rms. For minimum response time, PLL filter capacitors C_{2A} and C_{2B} should be:

$$C_{2A} = C_{2B} \cong \frac{130}{f_0\,(\mathrm{Hz})}\ \mu F$$

Under this condition, the worst-case output delay is ≈10 to 14 cycles of the input tone.

The practical matching and tracking tolerances of individual units limit the minimum bandwidth to ≈4% of f_0.

WIDEBAND DECODER

Figure 13 is a circuit configuration for increasing the detection bandwidth of the XR-2567 by combining the respective bandwidths of individual decoder sections. If the detection bands of each section are located adjacent to each other as shown in Figure 9 (b), and if the two outputs (pins 3 and 6) are shorted together, then the resulting bandwidth is the sum of individual bandwidths. In this manner, the total detection bandwidth can be increased to 24% of center frequency. To maintain uniform response throughout the passband, the input signal level should be ⩾80 mV rms, and the respective passbands of each section should have ≈3% overlap at center frequency.

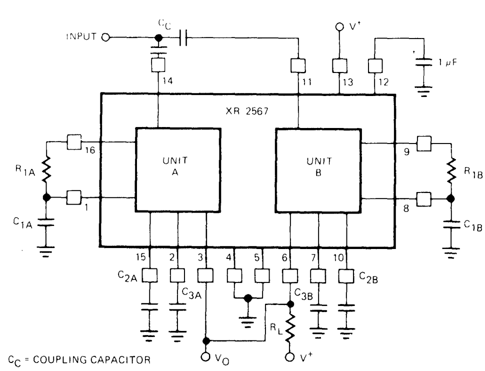


Figure 13. Wide-Band Tone Detection

TONE TRANSCEIVER

The XR-2567 can be used as a full-duplex tone transceiver by using one section of the unit as a tone detector and the remaining section as a tone generator. Since both sections operate independently, the circuit can transmit and receive simultaneously. A recommended circuti connection for transceiver applications is shown in Figure 14. In this case, Unit A is utilized as the receiver and Unit B is used as the transmitter. The transmitter section can be keyed "on" and "off" by applying a pulse to pin 8 through a disconnect diode D_1. The oscillator section of Unit B will be keyed "off' when the keying logic level at pin 8 is at a "low" state.

The output of the transmitter section (Unit B) can also be frequency modulated over a +6% deviation range by applying a modulation signal to pin 10.

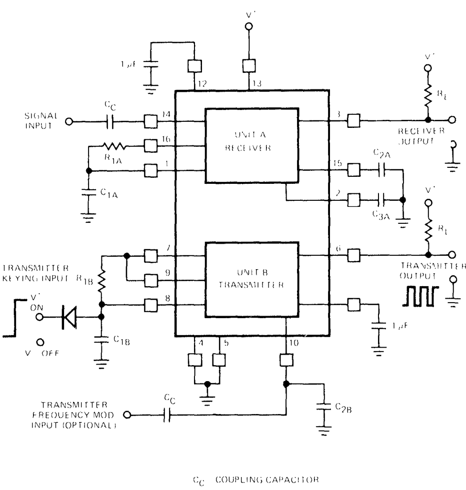


Figure 14. Tone Transceiver

HIGH CURRENT OSCILLATOR

The oscillator output of each section of XR-2567 can be amplified using the high current logic driver sections of the circuit. In this manner, each section of the circuit can switch 100 mA loads, without sacrificing oscillator stability. A recommended circuit connection for this application is shown in Figure 15. The oscillator frequency can be modulated over ±6% of f_0 by applying a control voltage to pins 15 or 10.

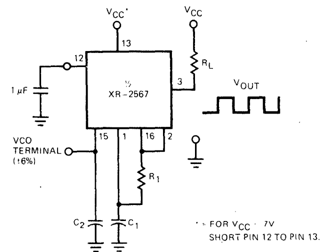


Figure 15. Precision Oscillator with High Current Output Capability

AVAILABLE TYPES

Part Number	Package	Operating Temperature
XR-2567M	Ceramic	-55°C to +125°C
XR-2567CN	Ceramic	0°C to +75°C
XR-2567CP	Plastic	0°C to +75°C

GENERAL DESCRIPTION

The RC4151 and RM4151 provide a simple low-cost method of A/D conversion. They have all the inherent advantages of the voltage-to-frequency conversion technique. The output of RC4151/RM4151 is a series of pulses of constant duration. The frequency of the pulses is proportional to the applied input voltage. These converters are designed for use in a wide range of data conversion and remote sensing applications.

DESIGN FEATURES

- Single Supply Operation (+8V to +22V)
- Pulse Output Compatible With All Logic Forms
- Programmable Scale Factor (K)
- Linearity ±0.05% typical—precision mode
- Temperature stability ±100% ppm/°C typical
- High Noise Rejection
- Inherent Monotonicity
- Easily Transmittable Output
- Simple Full Scale Trim
- Single-Ended Input, Referenced to Ground
- Also Provides Frequency-to-Voltage Conversion

SCHEMATIC DIAGRAM

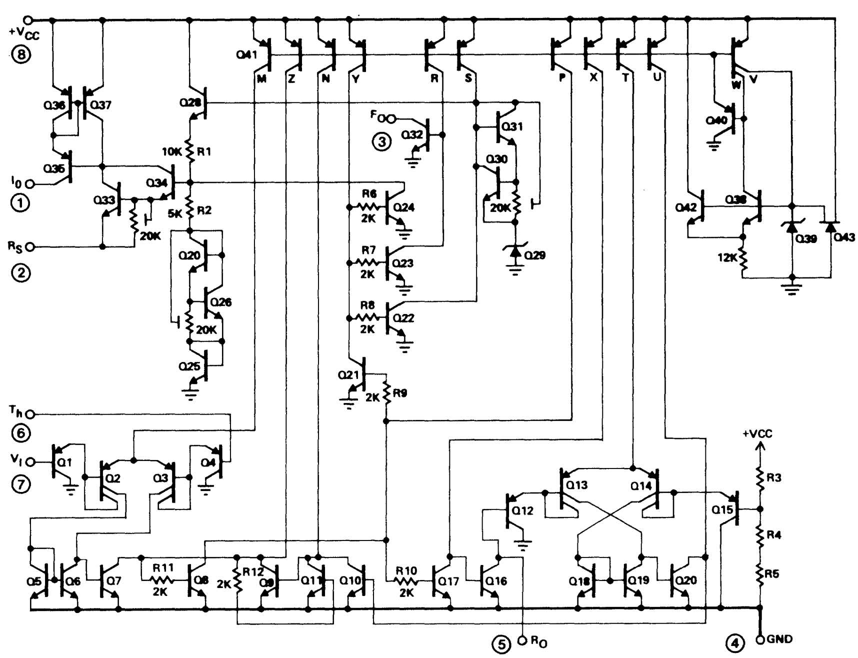
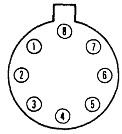


Figure 1

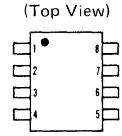
CONNECTION INFORMATION

TE (TO-99) Metal Can
(Top View)



Order Part Nos.: RC4151T, RM4151T
NOTE: PIN 4 CONNECTED TO CASE

DE and NB
Dual In-Line Packages
(Top View)



Order Part Nos.: RC4151NB, RV4151NB
RM4151DE, RV4151DE, RC4151DE

PIN	FUNCTION
1	CURRENT SOURCE
2	SCALE FACTOR
3	LOGIC OUTPUT
4	GROUND
5	ONE-SHOT R, C
6	THRESHOLD
7	INPUT VOLTAGE
8	V_{CC}

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	+22V
Output Sink Current	20mA
Internal Power Dissipation	500mW
Input Voltage	−0.2V to $+V_{CC}$
Output Short Circuit to Ground	Continuous
Storage Temperature Range	
RM4151	−65°C to +150°C
RV4151	−55°C to +125°C
RC4151	−55°C to +125°C
Operating Temperature Range	
RM4151	−55°C to +125°C
RV4151	−40°C to +85°C
RC4151	0°C to +70°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +15V, T_A = +25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	$8V < V_{CC} < 15V$		3.5	6.0	mA
	$15V < V_{CC} < 22V$	2.0	4.5	7.5	mA
Conversion Accuracy Scale Factor	Circuit Figure 3, V_I = 10V R_S = 14.0k	0.90	1.00	1.10	kHz/V
Drift with Temperature	Circuit Figure 3, V_I = 10V	–	±100	–	ppM/°C
Drift with V_{CC}	Circuit Figure 3, V_I = 1.0V $8V < V_{CC} < 18V$	–	0.2	1.0	%/V
Input Comparator Offset Voltage		–	5	10	mV
Offset Current		–	±50	±100	nA
Input Bias Current		–	−100	-300	nA
Common Mode Range (Note 1)		0	0 to V_{CC}−2	V_{CC} −3.0	V
One-Shot Threshold Voltage, Pin 5		0.63	.667	0.70	x V_{CC}
Input Bias Current, Pin 5		–	−100	-500	nA
Reset V_{SAT}	Pin 5, I = 2.2mA	–	0.15	0.50	V
Current Source Output Current (R_S = 14.0kΩ)	Pin 1, Figure 2, V = 0	–	138.7	–	µA
Change with Voltage	Pin 1, V = 0V to V = 10V	–	1.0	2.5	µA
Off Leakage	Pin 1, V = 0V	–	1	50.0	nA
Reference Voltage	Pin 2, Figure 2	1.70	1.9	2.08	V
Logic Output V_{SAT}	Pin 3, I = 3.0mA	–	0.15	0.50	V
V_{SAT}	Pin 3, I = 2.0mA	–	0.10	0.30	V
Off Leakage		–	.1	1.0	µA

Note 1: Input Common Mode Range includes ground.

PRINCIPLE OF OPERATION

Single Supply Mode Voltage-to-Frequency Conversion

In this application the RC4151/RM4151 functions as a stand-alone voltage to frequency converter operating on a single positive power supply. Refer to Figure 2, the simplified block diagram. The RC/RM4151 contains a voltage comparator, a one-shot, and a precision switched current source. The voltage comparator compares a positive input voltage applied at pin 7 to the voltage at pin 6. If the input voltage is higher, the comparator will fire the one-shot. The output of the one-shot is connected to both the logic output and the precision switched current source. During the one-shot period, T, the logic output will go low and the current source will turn on with current I. At the end of the one-shot period the logic output will go high and the current source will shut off. At this time the current source has injected an amount of charge $Q = I_O T$ into the network R_B–C_B. If this charge has not increased the voltage V_B such that $V_B > V_I$, the comparator again fires the one-shot and the current source injects another lump of charge, Q, into the R_B–C_B network. This process continues until $V_B > V_I$. When this condition is achieved the current source remains off and the voltage V_B decays until V_B is again equal to V_I. This completes one cycle. The VFC will now run in a steady state mode. The current source dumps lumps of charge into the capacitor C_B at a rate fast enough to keep $V_B \geqslant V_I$. Since the discharge rate of capacitor C_B is proportional to V_B/R_B, the frequency at which the system runs will be proportional to the input voltage.

The 4151 VFC is easy to use and apply if you understand the operation of it through the block diagram, Figure 2. Many users, though, have expressed the desire to understand the workings of the internal circuitry. Figure 1 shows the schematic of the 4151. The circuit can be divided into five sections: the internal biasing network, input comparator, one-shot, voltage reference, and the output current source.

The internal biasing network is composed of Q39-Q43. The N-channel FET Q43 supplies the initial current for zener diode Q39. The NPN transistor Q38 senses the zener voltage to derive the current reference for the multiple collector current source Q41. This special PNP transistor provides active pull-up for all of the other sections of the 4151.

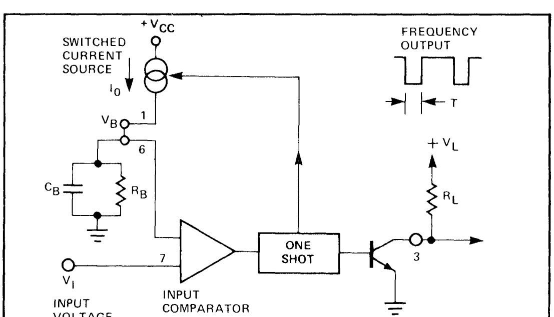


Figure 2. Simplified Block Diagram, Single Supply Mode

The input comparator section is composed of Q1-Q7. Lateral PNP transistors Q1-Q4 form the special ground-sensing input which is necessary for VFC operation at low input voltages. NPN transistors Q5 and Q6 convert the differential signal to drive the second gain stage Q7. If the voltage on input pin 7 is less than that on threshold pin 6, the comparator will be off and the collector of Q7 will be in the high state. As soon as the voltage on pin 7 exceeds the voltage on pin 6, the collector of Q7 will go low and trigger the one-shot.

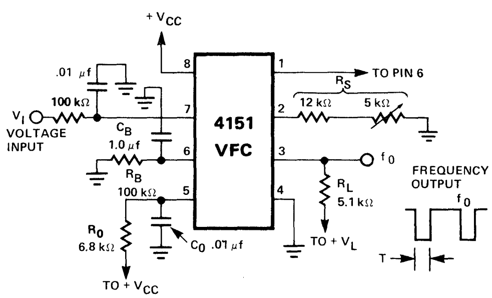
The one-shot is made from a voltage comparator and an R-S latch. Transistors Q12-Q15 and Q18-Q20 form the comparator, while Q8-Q11 and Q16-Q17 make up the R-S latch. One latch output, open-collector reset transistor Q16, is connected to a comparator input and to the terminal, pin 5. Timing resistor R_O is tied externally from pin 5 to $+V_{CC}$ and timing capacitor C_O is tied from pin 5 to ground. The other comparator input is tied to a voltage divider R_3-R_5 which sets the comparator threshold voltage at 0.667 V_{CC}. One-shot operation is initiated when the collector of Q7 goes low and sets the latch. This causes Q16 to turn off, releasing the voltage at pin 5 to charge exponentially towards $+V_{CC}$ through R_O. As soon as this voltage reaches 0.667 V_{CC}, comparator output Q20 will go high causing Q10 to reset the latch. When the latch is reset, Q16 will discharge C_O to ground. The one-shot has now completed its function of creating a pulse of period $T = 1.1\ R_O C_O$ at the latch output, Q21. This pulse is buffered through Q23 to drive the open-collector logic circuit transistor Q32. During the one-shot period the logic output will be in the low state. The one-shot output is also used to switch the reference voltage by Q22 and Q24. The low T.C. reference voltage is derived from the combination of a 5.5V zener diode with resistor and diode level shift networks. A stable 1.89 volts is developed at pin 2, the emitter of Q33.

Connecting the external current-setting resistor R_S = 14.0Ω from pin 2 to ground gives 135μA from the collectors of Q33 and Q34. This current is reflected in the precision current mirror Q35-Q37 and produces the output current I_O at pin 1. When the R-S latch is reset, Q22 and Q24 will hold the reference voltage off, pin 2 will be at 0V, and the current will be off. During the one-shot period T, the latch will be set, the voltage of pin 2 will go to 1.89V, and the output current will be switched on.

TYPICAL APPLICATIONS

Single Supply Voltage-to-Frequency Converter

Figure 3 shows the simplest type of VFC that can be made with the 4151. Input voltage range is from 0 to +10V, and output frequency is from 0 to 10kHz. Full scale frequency can be tuned by adjusting R_S, the output current set resistor. This circuit has the advantage of being simple and low in cost, but it suffers from inaccuracy due to a number of error sources. Linearity error is typically 1%. A frequency offset will also be introduced by the input comparator offset voltage. Also, response time for this circuit is limited by the passive integration network R_B C_B. For the component values shown in Figure 3, response time for a step change input from 0 to +10V will be 135msec. For applications which require fast response time and high accuracy, use the circuits of Figure 4 and 5.



DESIGN EQUATIONS

$f_O = KV_I$ Where $K = 0.486 \frac{R_S}{R_B R_O C_O} \frac{kHz}{V}$

$T = 1.1\, R_O C_O$

Figure 3. Single Supply Voltage-to-Frequency Converter

Precision VFC with Single Supply Voltage

For applications which requrie a VFC which will operate from a single positive supply with positive input voltage, the circuit of Figure 4 will give greatly improved linearity, frequency offset, and response time. Here, an active integrator using one section of the RC3403A quad ground-sensing op-amp has replaced the R_B-C_B network in Figure 3. Linearity error for this circuit is due only to the 4151 current source output conductance. Frequency offset is due only to the op-amp input offset and can be nulled to zero by adjusting R_B. This technique uses the op-amp bias current to develop the null voltage, so an op-amp with stable bias current, like the RC3403A, is required.

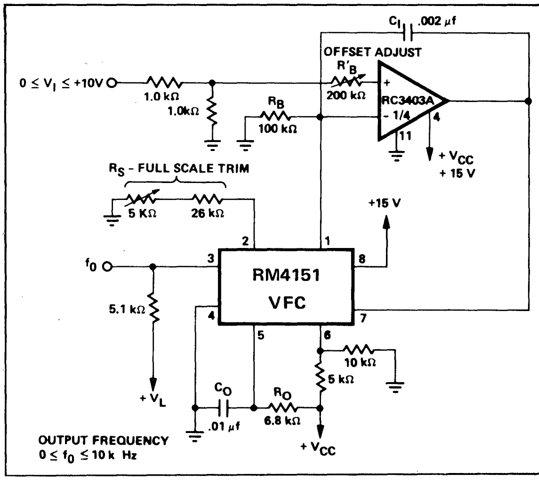


Figure 4. Precision Voltage-to-Frequency Converter Single Supply

Precision Voltage-to-Frequency Converter

In this application (Figure 5) the 4151 VFC is used with an operational amplifier integrator to provide typical linearity of 0.05% over the range of 0 to −10V. Offset is adjustable to zero. Unlike many VFC designs which lose linearity below 10mV, this circuit retains linearity over the full range of input voltage, all the way to 0V.

Trim the full scale adjust pot at V_I = −10V for an output frequency of 10kHz. The offset adjust pot should be set for 10Hz with an input voltage of −10mV.

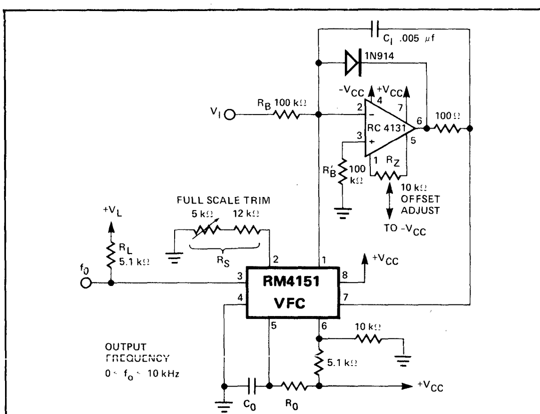


Figure 5. Precision Voltage-to-Frequency Converter

The 4131 operational amplifier integrator improves linearity of this circuit over that of Figure 3 by holding the output of the source, Pin 1, at a constant 0V. Therefore linearity error due to the current source output conductance is eliminated. The diode connected around the op-amp prevents the voltage at 4151 pin 7 from going below 0. Use a low-leakage diode here, since any leakage will degrade the accuracy. This circuit can be operated from a single positive supply if an RC3403A ground-sensing op-amp is used for the integrator. In this case, the diode can be left out. Note that even though the circuit itself will operate from a single supply, the input voltage is necessarily negative. For operation above 10kHz, bypass 4151 pin 6 with 0.01μf.

Comparison of Voltage-to-Frequency Applications Circuits

Table 1 compares the VFC applications circuits for typical linearity, frequency offset, response time for a step input from 0 to 10 volts, sign of input voltage, and whether the circuit will operate from a single positive supply or split supplies.

Table 1

	Figure 3	Figure 4	Figure 5
Linearity	1%	0.2%	0.05%
Frequency Offset	+10Hz	0	0
Response Time	135msec	10μsec	10μsec
Input Voltage	+	+	–
Single Supply	yes	yes	yes
Split Supply	–	–	yes

Frequency-to-Voltage Conversion

The 4151 can be used as a frequency-to-voltage converter. Figure 6 shows the single-supply FVC configuration. With no signal applied, the resistor bias networks tied to pins 6 and 7 hold the input comparator in the off state. A negative going pulse applied to pin 6 (or positive pulse to pin 7) will cause the comparator to fire the one-shot. For proper operation, pulse width must be less than the period of the one-shot, T = 1.1 R_O C_O. For a 5V p-p square-wave input the differentiator network formed by the input coupling capacitor and the resistor bias network will provide pulses which correctly trigger the one-shot. An external voltage comparator such as the 311 or 339 can be used to "square-up" sinusoidal input signals before they are applied to the 4151. Also, the component values for the input signal differentiator and bias network can be altered to accommodate square waves with different amplitudes and frequencies. The passive integrator network R_B C_B filters the current pulses from the pin 1 output. For less output ripple, increase the value of C_B.

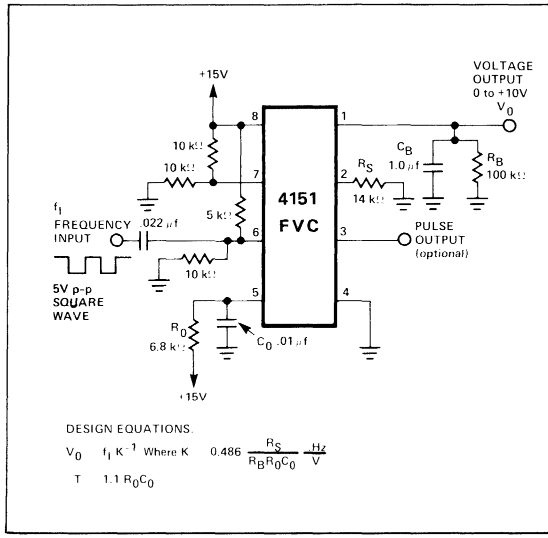


Figure 6. Single Supply Frequency-to-Voltage Converter

For increased accuracy and linearity, use an operational amplifier integrator as shown in Figure 7, the precision FVC configuration. Trim the offset to give –10mV out with 10Hz in and trim the full scale adjust for –10V out with 10kHz in. Input signal conditioning for this circuit is necessary just as for the single supply mode, and scale factor can be programmed by the choice of component values. A tradeoff exists between output ripple and response time, through the choice of integration capacitor C_I. If C_I = 0.1μf the ripple will be about 100mV. Response time constant τ_R = R_B C_I. For R_B = 100kΩ and C_I = 0.1μf, τ_R = 10msec.

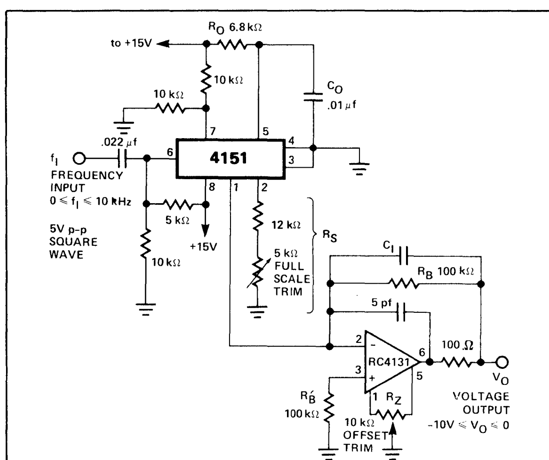


Figure 7. Precision Frequency-to-Voltage Converter

PRECAUTIONS

1. The voltage applied to comparator input pins 6 and 7 should not be allowed to go below ground by more than 0.3 volt.
2. Pins 3 and 5 are open-collector outputs. Shorts between these pins and $+V_{CC}$ can cause overheating and eventual destruction.
3. Reference voltage terminal pin 2 is connected to the emitter of an NPN transistor and is held at approximately 1.9 volts. This terminal should be protected from accidental shorts to ground or supply voltages. Permanent damage may occur if current in pin 2 exceeds 5mA.
4. Avoid stray coupling between 4151 pins 5 and 7, which could cause false triggering. For the circuit of Figure 3, bypass pin 7 to ground with at least 0.01μf. If false triggering is experienced with the precision mode circuits, bypass pin 6 to ground with at least 0.01μf. This is necessary for operation above 10kHz.

PROGRAMMING THE 4151

The 4151 can be programmed to operate with a full scale frequency anywhere from 1.0Hz to 100kHz. In the case of the VFC configuration, nearly any full scale input voltage from 1.0V and up can be tolerated if proper scaling is employed. Here is how to determine component values for any desired full scale frequency.

1. Set $R_S = 14k\Omega$ or use a 12k resistor and 5k pot as shown in the figures. (The only exception to this is Figure 5.)
2. Set $T = 1.1\ R_O C_O = 0.75\left[\frac{1}{fo}\right]$ where fo is the desired full scale frequency. For optimum performance make $6.8k\Omega < R_O < 680k\Omega$ and $0.001\mu f < C_O < 1.0\mu f$.
3. a) For the circuit of Figure 3 make $C_B = 10^{-2}\left[\frac{1}{fo}\right]$ Farads. Smaller values of C_B will give faster response time, but will also increase frequency offset and nonlinearity.

   b) For the active integrator circuits make

   $$C_I = 5 \times 10^{-5}\left[\frac{1}{fo}\right] \text{ Farads.}$$

   The op-amp integrator must have a slew rate of at least $135 \times 10^{-6}\left[\frac{1}{C_I}\right]$ volts per second where the value of C_I is again give in Farads.
4. a) For the circuits of Figure 3 and 4 keep the values of R_B and R_B' as shown and use an input attenuator to give the desired full scale input voltage.

   b) For the precision mode circuit of Figure 5, set $R_B = \frac{V_{IO}}{100\mu A}$ where V_{IO} is the full scale input voltage. Alternately the op-amp inverting input (summing node) can be used as a current input with full scale input current $I_{IO} = -100\mu A$.
5. For the FVCs, pick the value of C_B or C_I to give the optimum tradeoff between response time and output ripple for the particular application.

DESIGN EXAMPLE

I. Design a precision VFC (from Figure 5) with fo = 100kHz and $V_{IO} = -10V$.

1. Set $R_S = 14.0k\Omega$.
2. $T = 0.75\left[\frac{1}{10^{-5}}\right] = 7.5\mu sec$

   Let $R_O = 6.8k\Omega$ and $C_O = 0.001\mu f$.
3. $C_I = 5 \times 10^{-5}\left[\frac{1}{10^{-5}}\right] = 500pf.$

   Op-amp slew rate must be at least

   $SR = 135 \times 10^{-6}\left[\frac{1}{500pf}\right] = 0.27\mu sec$
4. $R_B = \frac{10V}{100\mu A} = 100k\Omega.$

II. Design a precision VFC with fo = 1Hz and $V_{IO} = -10V$.

1. Let $R_S = 14.0k\Omega$.
2. $T = 0.75\left[\frac{1}{1}\right] = 0.75$ sec.

   Let $R_O = 680k\Omega$ and $C_O = 1.0\mu f$.
3. $C_I = 5 \times 10^{-5}\left[\frac{1}{1}\right] F = 50\mu f.$
4. $R_B = 100k\Omega.$

III. Design a single supply FVC to operate with a supply voltage of 9V and full scale input frequency fo = 83.3Hz. The output voltage must reach at least 0.63 of its final value in 200msec. Determine the output ripple.

1. Set $R_S = 14.0k\Omega$.
2. $T = 0.75\left[\frac{1}{83.3}\right] = 9msec$

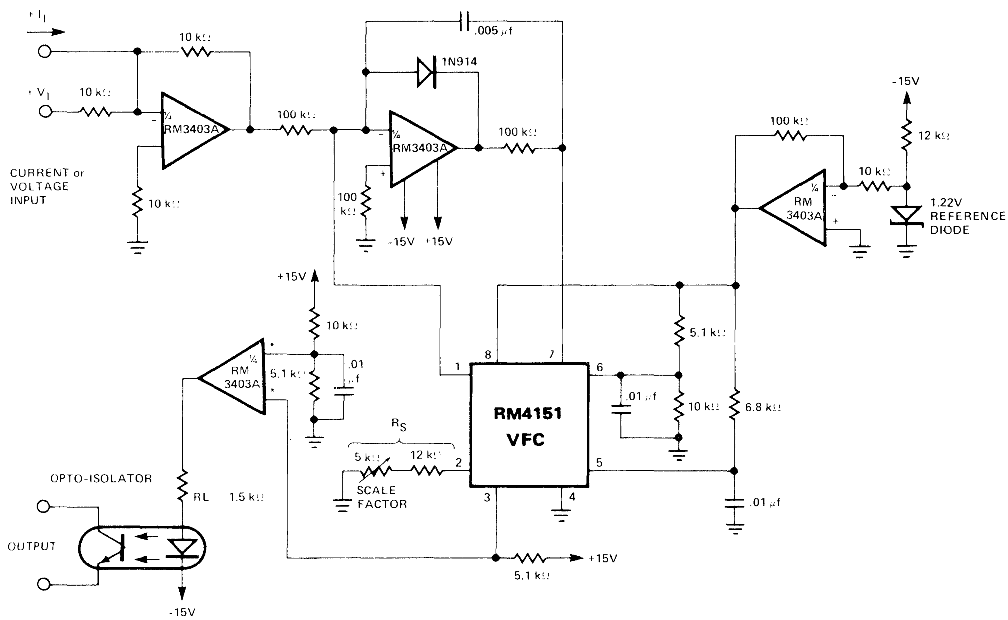
   Let $R_O = 82k\Omega$ and $C_O = 0.1\mu f$.
3. Since this FVC must operate from 8.0V, we shall make the full scale output voltage at pin 6 equal to 5.0V.
4. $R_B = \frac{5V}{100\mu A} = 50k\Omega.$
5. Output response time constant is $\tau_R \leqslant 200msec$

   Therefore $C_B \leqslant \frac{\tau_R}{R_B} = \frac{200 \times 10^{-3}}{50 \times 10^{3}} = 4\mu f.$

   Worst case ripple voltage is:

   $V_R = \frac{9mS \times 135\mu A}{4\mu f} = 304mV.$

IV. Design an opto-isolated VFC with high linearity which accepts a full scale input voltage of +10V. See Figure 8 for the final design. This circuit uses the precision mode VFC configuration for maximum linearity. The RC3403A quad op-amp provides the functions of inverter, integrator, regulator, and LED driver.



* POLARITY DETERMINED BY DESIRED RELATIONSHIP BETWEEN PULSE OUTPUT LEVEL AND LED "ON" STATE.

Figure 8. Opto-Isolated VFC

DESCRIPTION

The Raytheon 4152 consists of a comparator, a one-shot, a precise gated current-source output, an internal voltage reference, and an open-collector output . . . all on a single monolithic IC chip. These elements can be combined via external pin connections to perform a wide variety of circuit functions.

The versatility of this unique IC makes it easy to tailor the circuit operation to your needs. Pulse width, scale factor, and output drive are set by external resistors as shown in Figure 1. Combine the versatile 4152 with an op amp or two, some digital circuits, and the range of cost-effective applications becomes even greater.

The Raytheon 4152 provides a versatile, low-cost means of accurately converting an analog signal to a pulse train of proportional frequency, and vice versa. It can be imaginatively applied to a broad range of signal conditioning applications once the various functional blocks within the IC are understood.

The 4152 is directly interchangeable with the 4151, thereby allowing an upgrading of system accuracy at minimal cost.

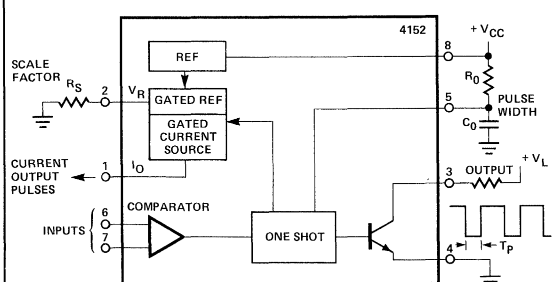


Figure 1. Functional Diagram of Raytheon 4152.

FEATURES

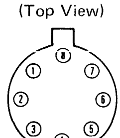
- Single supply operation (+7 V to +18 V)
- Pulse output compatible with all logic forms (DTL/TTL/CMOS)
- Programmable scale factor (K)
- High linearity ±0.05% max
- Temperature stability ±150 ppm/°C max
- Direct replacement for RM/RC4151
- High noise rejection
- Inherent monotonicity
- Easily transmittable output
- Simple full scale trim
- Single-ended input, referenced to ground
- V/F or F/V conversion
- Voltage or current input
- Wide dynamic range

APPLICATIONS

- Precision voltage-to-frequency-converters
- Pulse-width modulators
- Programmable pulse generators
- Frequency-to-voltage converters
- Integrating analog-to-digital converter
- Long-term analog integrator
- Signal conversion –
  - Current-to-frequency
  - Temperature-to-frequency
  - Pressure-to-frequency
  - Capacitance-to-frequency
  - Frequency-to-current
- Signal isolation
  - VFC → opto-isolation → FVC
  - ADC with opto-isolation
- Signal encoding
  - FSK modulation/demodulation
  - Pulse-width modulation
- Frequency scaling
- DC motor speed control

CONNECTION INFORMATION

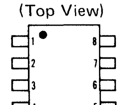
TE (TO-99) Metal Can
(Top View)



Order Part Nos.: RC4152T, RM4152T

NOTE: PIN 4 CONNECTED TO CASE

DE and NB Miniature Dual In-line Packages
(Top View)



Order Part Nos.: RC4152NB, RV4152NB
RM4152DE, RV4152DE, RC4152DE

PIN	FUNCTION
1	CURRENT SOURCE
2	SCALE FACTOR
3	LOGIC OUTPUT
4	GROUND
5	ONE-SHOT R, C
6	THRESHOLD
7	INPUT VOLTAGE
8	V_{CC}

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	+22V
Output Sink Current	20mA
Internal Power Dissipation	500mW
Input Voltage	−0.2V to $+V_{CC}$
Output Short Circuit to Ground	Continuous
Storage Temperature Range	
RM4152	−65°C to +150°C
RV4152	−55°C to +125°C
RC4152	−55°C to +125°C
Operating Temperature Range	
RM4152	−55°C to +125°C
RV4152	−40°C to +85°C
RC4152	0°C to +70°C

ELECTRICAL SPECIFICATIONS Typical performance at V_{CC} = +15 V and T_A = +25°C unless otherwise noted.

CIRCUIT CHARACTERISTICS	MIN	TYP	MAX	UNITS
Input Comparator				
Input Offset Voltage @ 25°C		±2	±10	mV
vs. Temperature		±20		μV/°C
Input Offset Current		±30	±100	nA
Bias Current (Either Input)		-50	-300	nA
Input Voltage Range (Either Input)		0 to V_{CC} -3.0 Volts		V
Comparator Gain		10,000		—
One-Shot Pulse Circuit				
Pulse Width (See Fig. 1)		$1.1\ R_O\ C_O \pm 3\%$		sec
Threshold Voltage (Pin 5)	0.65 V_{CC}	0.67 V_{CC}	0.69 V_{CC}	V
Input Bias Current (Pin 5)		-100	-500	nA
V_{sat} at Pin 5, I = 2.2 mA		0.10	0.5	V
Pulse Width Stability (T_p = 75 μs)				
vs. Temperature		±30	±50	ppm/°C
vs. Supply		±100		ppm/V
Gated Current Source				
Output of Gated Current Source		$V_R/R_S \pm 1\%$		—
vs. Temperature(1)		±50	±100	ppm/°C
vs. Supply		0.10		%/V
Compliance (Change with Voltage)		0.10	0.25	μA/V
Leakage in OFF State		10	50	nA
Rise Time		100		nsec
Fall Time		100		nsec
Reference Voltage				
Voltage V_R (Pin 2)	2.0	2.25	2.5	V
Temperature Coefficient		±50	±100	ppm/°C
Logic Output (Pin 3)				
V_{sat} @ I = 3 mA		0.1	0.5	V
@ I = 10 mA		0.8		V
Power Supply				
Voltage, Operating Range	+7	+15	+18	V
Quiescent Current Drain		2.5	6	mA

(1)Temperature coefficient of output current mirror (pin 1 output) exclusive of reference voltage drift.

Input Comparator

The input comparator section consists of transistors Q1 through Q7 (see Figure 2). A PNP ground-sensing input stage provides capability of operating down to low input voltages, thus the input range on either input is from zero up to $+V_{CC}$-3V(power supply voltage less three volts). This is particularly important for single-supply operation. Input comparator gain is approximately 10,000. The output of the comparator, transistor Q7, switches from OFF to ON when the input voltage applied to pin 7 becomes more positive than the input voltage on pin 6. The output transistor Q7 going into saturation is used to trigger the one-shot.

One important precaution: The voltage applied to the input comparator (pins 6 and 7) must not be more negative than 0.3 V relative to the ground terminal (pin 4) unless there is protective current limiting. Negative input voltages will saturate the input PNP transistors and cause excessive input base current. This input-base current must not be allowed to exceed 25 mA over an extended period of time or the IC could be damaged. If there is a possibility of continuous excessive negative voltage on the input, then a resistor in series with the input should be added to limit the input current.

One-Shot Circuit

Pulse-width of the one-shot is determined by the external components R_o, C_o that are connected to pin 5. The capacitor C_o is normally discharged through the saturated transistor Q16. When the one-shot timing cycle is initiated, capacitor C_o is released by Q16 turning OFF and allowed to charge towards $+V_{CC}$ through R_o. At 2/3 of $+V_{CC}$, transistor Q16 is switched ON and the capacitor C_o is discharged. The pulse width will therefore be determined by the following equation:

$$1 - \epsilon^{-\frac{T_p}{R_o C_o}} = 0.667$$

$$T_p = 1.1\ R_o C_o$$

Pulse width T_p is independent of supply voltage $+V_{CC}$. For best linearity and stability, R_o and C_o should be selected within a range of 5 KΩ to 500 KΩ and 0.001 μF to 1.0 μF.

A latching action by the RS flip-flop comprised of Q9 and Q11 assures that the timing cycle will be completed regardless of input voltage. The flip-flop is set by Q7 going into the ON state. Q9 is normally OFF and Q11 normally ON; so Q7 going low will cause Q11 to switch OFF and Q9 to switch ON. Since Q9 and Q7 collectors are tied together, Q9 will keep the collectors low regardless of Q7 state. At the end of the timing cycle, Q10 is switched ON and this will make Q9 go OFF. If Q7 is OFF, then the flip-flop can reset to the normal state where Q9 is OFF and Q11 ON. The input state overides this reset action. In FVC applications, it is very important to make the input pulses narrower than the output pulse width T_p to assure proper resetting of the Q9-Q11 flip-flop.

The output pulse of the one-shot performs three functions during the timing interval:

1. The open-collector output transistor Q32 is switched into saturation. The output pulse at pin 3 is in the low state during the T_p timing interval.
2. A reference voltage V_R is switched ON at pin 2.
3. The output current source is gated ON. A current pulse of width T_p and amplitude V_R/R_S will come out of pin 1.

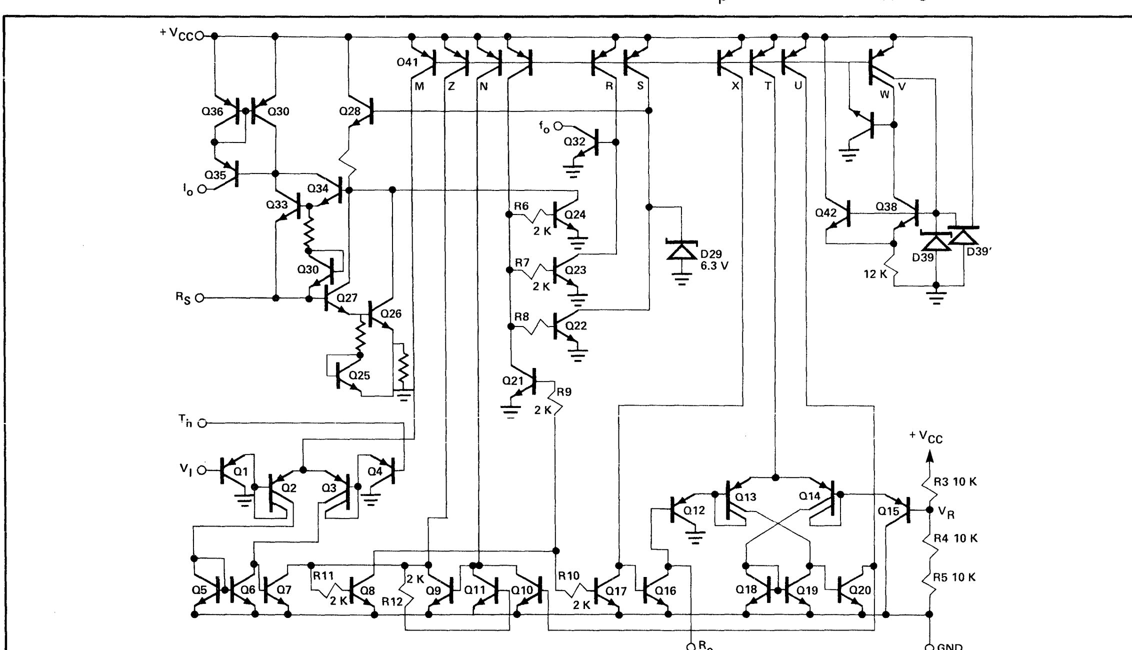


Figure 2. Raytheon 4152 Schematic Diagram

Gated Current Source

During the pulse timing interval T_p, a reference voltage V_R is switched to the ON state at pin 2. External resistor R_S at pin 2 sets up a current V_R/R_S that is reflected in precision current source Q35-Q37. This causes a current pulse of magnitude V_R/R_S from Q35 at pin 1. The output pulse I_O at pin 1 has pulse width T_p and amplitude of V_R/R_S.

Reference

The reference voltage V_R is derived from a very stable, low tempco, buried-zener diode. The zener voltage is level shifted to provide a stable 2.3 V at pin 2 during the timing interval T_p. This internal reference provides excellent power-supply rejection over a wide operating range. Low-cost unregulated power supplies can often be used without degrading accuracy (see characteristic curves).

VOLTAGE-TO-FREQUENCY CONVERSION

Single-Supply VFC Circuit

The simplest type of VFC that can be made with the Raytheon 4152 is shown in Figure 3. The circuit will operate from a single power supply voltage that can vary from +7 V to +18 V. The input voltage V_{IN} is positive and can range from zero up to within 3 V of positive supply.

The input voltage V_{IN} is applied to the input comparator through a low-pass filter (100 KΩ, 0.01 μF). The one-shot will fire repetitively and pump out current pulses of amplitude I_O into the external low-pass filter comprised of R_B, C_B. This sets up a feedback loop and the pulse repetition rate will rise until the average voltage at pin 6 equals the DC input voltage at pin 7. At null, the duty cycle T_p/T must be sufficient to keep integrating capacitor C_B charged up to V_{IN}. Assuming C_B is relatively large, then in the steady-state condition:

SPECIFICATIONS AS SINGLE-SUPPLY VFC (Figure 3) — Typical performance at 25°C when connected as shown in Fig. 3. R_O = 6.8 KΩ, C_O = 0.01 μF, V_{CC} = +15.0 V, R_B = 100 KΩ, C_B = 1.0 μF.

Input	
Input Voltage Range	10 mV to +10 V
Input Overrange	+10% min
Input Impedance	100 KΩ
Output	
Frequency Range	10 Hz to 10 kHz
Frequency Overrange	+10% min
Scale Factor	1 kHz/V ± 10%
Response Time to Step Input	135 msec
Pulse Width	75 μsec ± 10%
Rise and Fall Time	500 nsec
Output Voltage	$+V_{CC}$
HIGH State	3.0 mA @ V_{sat} = 0.15 V
LOW State	10 mA @ V_{sat} = 0.8 V
Accuracy	
Nonlinearity	±1% max
Offset Voltage	±15 mV max
Gain Accuracy	
vs. Temperature	±300 ppm/°C max
vs. Supply	±0.3%/Volt
Offset Stability	
vs. Temperature	±50 μV/°C
vs. Supply	±20 μV/V of ΔV_S
Power Requirement	
Supply Voltage	
Rated Performance	+15 V
Operating Range	+7 V to +18 V
Quiescent Current Drain	+6.0 mA max

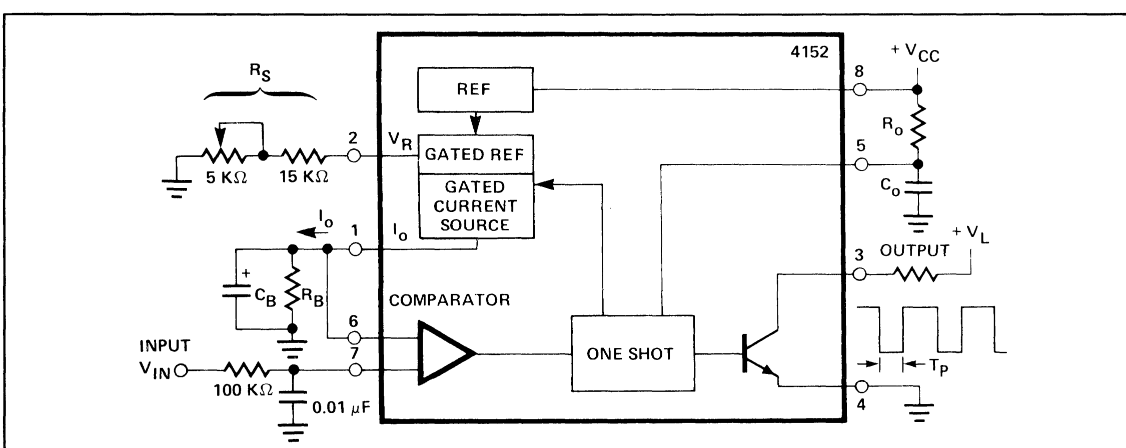


Figure 3. Single-Supply Voltage-to-Frequency Converter

$$\frac{V_{IN}}{R_B} = I_O \frac{T_p}{T}$$

Since I_O is V_R/R_S and T_p is 1.1 R_o C_o, then the output frequency F_O will be:

$$F_O = \frac{1}{T} = \frac{R_S}{1.1\ R_o C_o R_B} \cdot \frac{V_{IN}}{V_R}$$

The external passive components set the scale factor. For best linearity, R_S should be limited to a range of 15 KΩ to 20 KΩ. Reference voltage V_R is nominally 2.3 V. Recommended values for various operating ranges are given in the table below:

Operating Range	R_o	C_o	R_B	C_B
DC to 1 kHz	6.8 KΩ	0.1 μF	100 KΩ	10 μF
DC to 10 kHz	6.8 KΩ	0.01 μF	100 KΩ	1.0 μF
DC to 100 kHz	6.8 KΩ	0.001 μF	100 KΩ	0.1 μF

This simple, single-supply VFC circuit is recommended for applications where the input dynamic range is limited and does not go to zero, and response time is not critical. When scaled for 10 kHz full-scale output, the nonlinearity will be less than 1% over an input range of 10 mV to 10 V. Response time to a step input will be approximately 135 msec.

Linearity, offset, and response time are all improved by adding an external op amp as shown in Figure 4. The active integrator is used to make a precision VFC circuit.

SPECIFICATIONS AS PRECISION, DUAL-SUPPLY VFC (Figure 4) — Typical performance when connected as shown in Fig. 4. R_o = 6.8 KΩ, C_o = 0.01 μF, C_I = 0.005 μF, V_{CC} = ±15 V, R_B = 100 KΩ.

Input	
Input Voltage Range	0 to −10 V
Input Overrange	+10% min
Input Impedance	100 KΩ
Output	
Frequency Range	0 to 10 kHz
Frequency Overrange	+10% min
Scale Factor	1 kHz/V ± 10%
Response Time to Step Input(1)	10 μsec
Pulse Width	75 μsec ± 10%
Rise and Fall Time	500 nsec
Output Voltage	
HIGH State	$+V_{CC}$
LOW State	+0.5 V max at 3 mA
Accuracy	
Nonlinearity	±0.05% max
Offset Voltage	±1 mV, Adj to Zero
Gain Accuracy	
vs. Temperature	±150 ppm/°C max
vs. Supply	±0.02%/V
Offset Stability	
vs. Temperature	±20 μV/°C
vs. Supply	±20 μV/V
Power Requirement	
Supply Voltage	±15 V
Quiescent Current Drain (4152 only)	+6 mA

(1)Two pulses of new frequency plus 10 μsec.

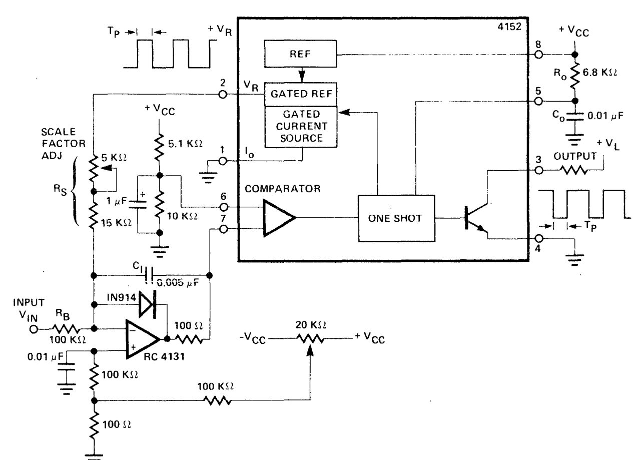


Figure 4. Precision Voltage-to-Frequency Converter

Precision VFC Circuit, Dual-Supply

In the precision VFC circuit of Figure 4, a negative input voltage is summed with positive output current pulses V_R/R_S into an integrator circuit. The integrator output is applied to the 4152 input comparator. This forms a charge-balancing loop and the pulse-repetition frequency will be such that the average value of output current pulses will equal the average value of input current. In the steady-state condition,

$$\frac{V_{IN}}{R_B} = \frac{V_R}{R_S} \frac{T_p}{T}$$

As before, pulse width T_p is 1.1 R_oC_o. The reference voltage V_R is nominally 2.3 V, therefore:

$$F_O = 0.395 \frac{R_S}{R_BR_oC_o} V_{IN}$$

For best linearity, R_S should be limited to a range of 15 KΩ to 20 KΩ. The current pulses will have a magnitude of approximately 134 μA with V_R of 2.3 V and R_S of 17.2 KΩ. A choice of 100 KΩ for R_B provides a high input impedance to V_{IN}. If we choose R_o of 6.8 KΩ, then the table below indicates the VFC scaling for various capacitor values using the circuit of Fig. 4 and R_S of 17.2 KΩ:

C_o	C_I	Scale Factor	Range Input V_{IN}	Range Output F_O
0.1 μF	0.05 μF	0.1 kHz/V	0 to -10 V	0 to 1 kHz
0.01 μF	0.005 μF	1 kHz/V	0 to -10 V	0 to 10 kHz
1000 pF	500 pF	10 kHz/V	0 to -10 V	0 to 100 kHz

Scale factor can be easily trimmed by varying R_S. The offset adjustment shown in Fig. 4 compensates for offset in the op amp. Best linearity is obtained with op amps having greater than 1 V/μsec slew rate, but any op amp can be used.

FREQUENCY-TO-VOLTAGE CONVERSION

Single-Supply FVC Circuit

A basic, single-supply frequency-to-voltage converter can be designed as shown in Figure 5 if the input frequency is in the form of a pulse or square wave. If the input is in the form of a sine wave, then a comparator should be used ahead of this circuit. The incoming pulses shaped by C_{IN} trigger the 4152 input comparator and fire the one-shot. For proper operation, the input pulse width must be less than the one-shot period T_p, which is 1.1 R_oC_o. A differentiator and biasing network on the input (C_I, 5.1 KΩ, and 10 KΩ) is used to shape the trigger input. Pin 7 is biased at 1/2 V_{CC} and Pin 6 is biased at 2/3 V_{CC}, therefore the input comparator is in the OFF state between input pulses. A negative-going pulse applied to Pin 6, or a positive-going pulse to Pin 7, will cause the input comparator to fire the one-shot. The input pulse amplitude must be large enough to trip the comparator, but not so large as to exceed the input voltage ratings. For the component values shown in Fig. 5, the input pulse amplitude should be 5 V peak-to-peak when operating from ±15 V supplies.

Output current pulses of precise amplitude and width are low-pass filtered by R_B, C_B to provide a DC output voltage. Output ripple voltage can be minimized by increasing C_B, but at the expense of increased response time. The DC output voltage will be directly proportional to the input frequency F_{IN}. The average value of the output is given by:

$$V_o = \frac{F_{IN}\ \text{Hz}}{0.395 \dfrac{R_S}{R_BR_oC_o} \dfrac{\text{Hz}}{\text{Volt}}}$$

$$V_o = 2.53 \frac{R_BR_oC_o}{R_S} F_{IN} \text{ Volts}$$

Recommended values for various operating ranges are given below:

Input Operating Range	C_{IN}	R_o	C_o	R_B	C_B	Ripple
0 to 1 kHz	0.02 μF	6.8 KΩ	0.1 μF	100 KΩ	100 μF	1 mV
0 to 10 kHz	0.002 μF	6.8 KΩ	0.01 μF	100 KΩ	10 μF	1 mV
0 to 100 kHz	200 pF	6.8 KΩ	0.001 μF	100 KΩ	1 μF	1 mV

To estimate worst-case ripple voltage, assume that the current pulse I_O of width T_p causes a step change in output voltage across C_B. From i = C dV/dt,

$$\Delta V_o = \frac{I_OT_p}{C_B}, \text{ where } T_p = 1.1\ R_oC_o$$

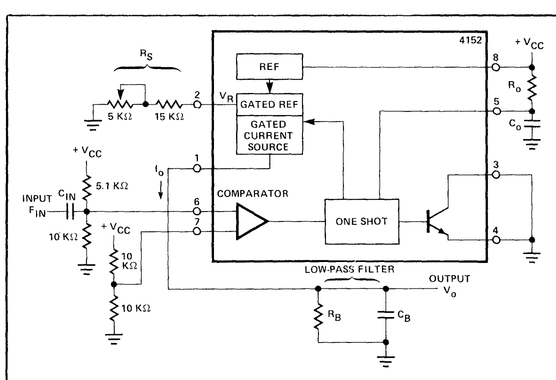


Figure 5. Single Supply Frequency-to-Voltage Converter

For example; if the output pulse width T_p were 9 msec, the pulse amplitude were 2.3 V/17 KΩ = 135 μA, and C_B were chosen to be 10 μF, then the output ripple would be approximately 121 mV peak-to-peak.

Precision Frequency-to-Voltage Circuits

Linearity and offset can be improved by adding one or more op amps to form an active low-pass filter at the output. A circuit using a single op amp filter is shown in Figure 6. The output current pulses of amplitude V_R/R_S are injected into the summing junction of an op amp integrator.

The positive output pulses are averaged by the low-pass filter and the output voltage will be negative. In the steady-state condition,

$$V_{o\,Avg} = \frac{F_{IN}\ \text{Hz}}{0.395 \dfrac{R_S}{R_B R_o C_o} \dfrac{\text{Hz}}{\text{Volt}}}$$

$$V_{o\,Avg} = -2.53 \frac{R_B R_o C_o}{R_S} F_{IN}\ \text{Volts}$$

The worst-case ripple can be estimated as in the single-supply case. As before, there is a design trade-off between ripple voltage and response time.

A two-pole low-pass filter is recommended for applications requiring wide dynamic range and fast response time. The double pole filter shown in Figure 7 is an excellent choice for FVC operation. The filter response can be calculated from the following equations:

$$I_O + \frac{V_O}{R_1} = -C_1 \frac{dV_1}{dt}$$

and

$$\frac{V_1 - V_O}{R_2} = C_2 \frac{dV_O}{dt}$$

These combine into the single differential equation:

$$I_O = -C_1 R_2 C_2 \frac{d^2V_O}{dt^2} - C_1 \frac{dV_O}{dt} - \frac{V_O}{R_1}$$

On the input side; I_O is a pulse train of frequency F_{IN}, pulse-width T_p, and amplitude V_R/R_S. As before, the input amplitude should be 5 V peak-to-peak for the component values shown. When F_{IN} is constant, the output voltage will be:

$$\frac{V_{o\,Avg}}{R_1} = \frac{V_R}{R_S} \frac{T_p}{T}$$

$$V_{o\,Avg} = -1.1 \frac{R_1}{R_S} R_o C_o V_R F_{IN}$$

Response to a step-change in input frequency is determined by the ratio of the two time constants, R_1C_1 and R_2C_2. Step response to input frequency change will be critically damped for $R_1C_1 = 4R_2C_2$. A more optimum relationship is R_1C_1 equal to R_2C_2 which provides a damping factor of 0.5. The capacitors C_1 and C_2, as well as R_oC_o, should be chosen for minimum ripple over the desired range of operation. Scaled for 1 V per kHz and T_p of 6.8 msec, this filter has less than 0.1 V peak-to-peak ripple over the range of 10 Hz to 10 kHz (R_1 = 100 K and C_1 = 0.1 μF). The ripple is less than 0.02 V peak-to-peak above 100 Hz.

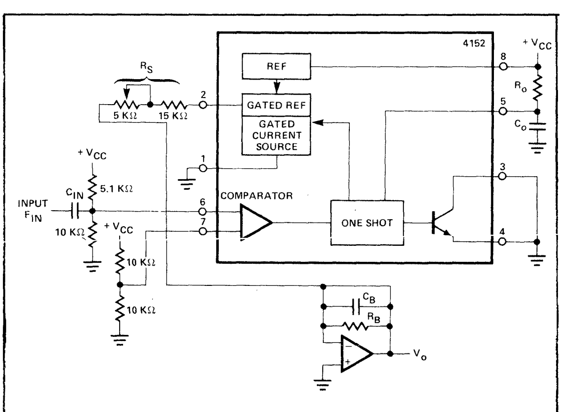


Figure 6. Frequency-to-Voltage Converter with Single-Pole Low-Pass Filter

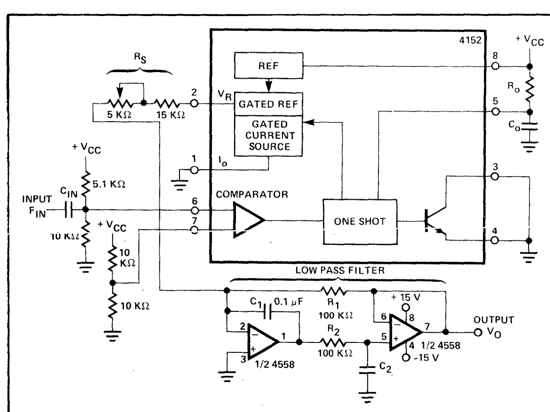
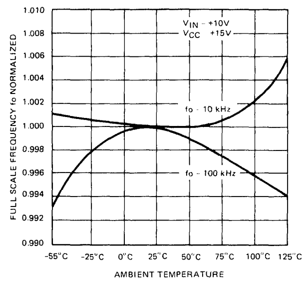


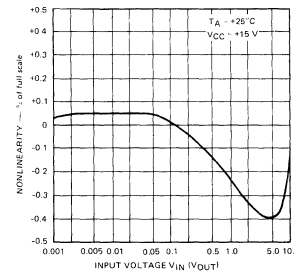
Figure 7. Frequency-to-Voltage Converter with Two-Pole Low-Pass Filter

TYPICAL ELECTRICAL DATA

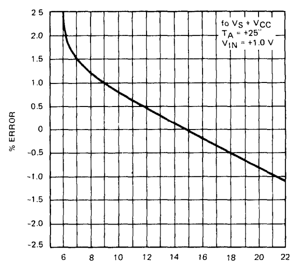
Single Supply VFC



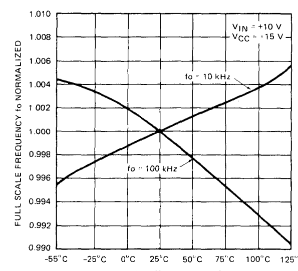
Single Supply VFC



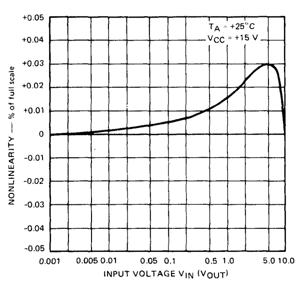
Single Supply VFC



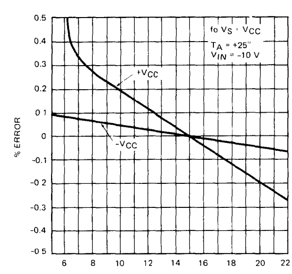
Precision Mode VFC fo vs. Temperature



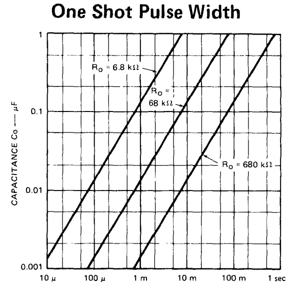
Precision Mode VFC



Precision Mode VFC



One Shot Pulse Width



PRODUCT DESCRIPTION

The Raytheon RC4200 is the industry's first integrated circuit multiplier to have complete compensation for nonlinearity, the primary source of error and distortion. This is also the first IC multiplier to have three on-board operational amplifiers designed specifically for use in multiplier logging circuits. These specially-designed amplifiers are frequency compensated for optimum AC response in a logging circuit; the heart of a multiplier, and can therefore provide superior AC response in comparison to other analog multipliers.

Versatility is unprecedented; this is the first IC multiplier that can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, one-quadrant division or square-rooting, and RMS-to-DC conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very low tempco on accuracy.

The excellent linearity and versatility were achieved through circuit design rather than special grading or tweaking, therefore unit cost is very low. Analog multipliers can now be used in applications where price was previously an inhibiting factor.

The Raytheon RC4200 is ideal for use in low-distortion audio modulation circuits, voltage-controlled active filters, and precision oscillators.

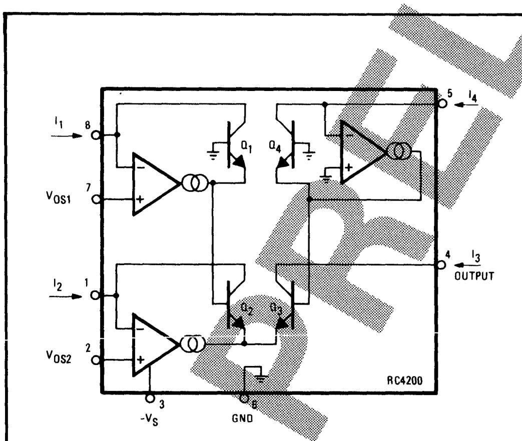


Figure 1. 4200 Multiplier Functional Diagram

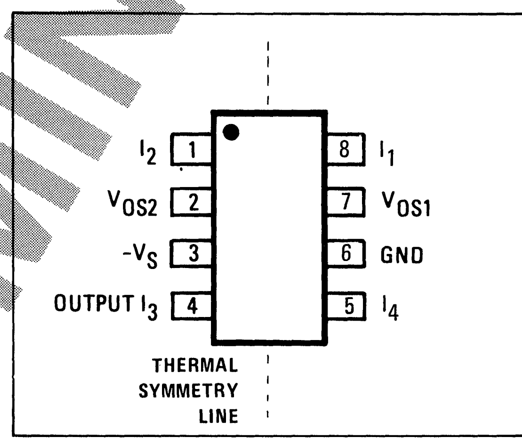
FEATURES

- High accuracy
  - Non-linearity – 0.1% maximum
  - Temperature coefficient – 0.005%/°C maximum
- Multiple functions
  - Multiply, divide, square, square root, RMS-to-DC conversion, AGC, and modulate/demodulate
- Wide bandwidth – 4 MHz

THERMAL SYMMETRY

The scale factor is sensitive to temperature gradients across the chip in the lateral direction. Where possible, the package should be oriented such that sources generating temperature gradients are located physically on the line of thermal symmetry. This will minimize scale-factor error due to thermal gradients.

CONNECTION INFORMATION



FUNCTIONAL DESCRIPTION

The RC4200 multiplier is designed to multiply two input currents (I_1 and I_2) and to divide by a third input current (I_4). The output is also in the form of a current (I_3). A simplified circuit diagram is shown in Figure 1. The nominal relationship between the three inputs and the output is:

$$I_3 = \frac{i_1 i_2}{I_4} \qquad (1)$$

All four currents must be positive and restricted to a range of 1μA to 1mA. The three input currents go into the multiplier chip at op-amp summing junctions which are nominally at zero volts. Therefore, an input voltage can be easily

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Supply Voltage	-22V
Internal Power Dissipation	500 mW
Input Current	-5 mA
Storage Temperature Range	
RM4200/4200A	-65°C to +150°C
RV4200/4200A	-55°C to +125°C
RC4200/4200A	-55°C to +125°C
Operating Temperature Range	
RM4200/4200A	-55°C to +125°C
RV4200/4200A	-40°C to +85°C
RC4200/4200A	0°C to +70°C

ELECTRICAL CHARACTERISTICS (Over operating temperature range, V_S = -15V unless otherwise noted)

PARAMETER	CONDITIONS	RC4200A			RC4200			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input range (I_1, I_2 and I_4)		1.0		1000	1.0		1000	μA
Total error as multiplier	T_A = 25°C							
Untrimmed				±2.0			±3.0	%
With external trim				±0.2			±0.5	%
Vs temperature			±0.005			±0.005		%/°C
Vs supply (-9 to -18V)			±0.1			±0.1		%/V
Nonlinearity	50μA < I < 250μA, T_A = 25°C			±0.1			±0.3	%
Input offset voltage	$I_1 = I_2 = I_4$ = 150μA, T_A = 25°C			±5			±10	mV
Input bias current	$I_1 = I_2 = I_4$ = 150μA, T_A = 25°C			300			500	nA
Average temperature coefficient of input offset voltage	$I_1 = I_2 = I_4$ = 150μA			±50			±100	μV/°C
Output current range (I_3)	(Note 1)	1.0		1000	1.0		1000	μA
Frequency response, -3 dB			4 MHz			4 MHz		MHz
Supply voltage range		-9	-15	-18	-9	-15	-18	V
Quiescent current	$I_1 = I_2 = I_4$ = 150μA, T_A = 25°C			4			4	mA

Note 1: These specifications apply with output (I_3) connected to an op amp summing junction. If desired, the output (I_3) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700 ohms and must be pulled up to a positive supply such that the voltage on pin (3) stays within a range of 0 to +5V.

converted to an input current by a series resistor. Any number of currents may be summed at the inputs. Depending on the application, the output current can be converted to a voltage by an external op amp or used directly. This capability of combining input currents and voltages in various combinations provides great versatility in application.

Inside the multiplier chip, the three op amps make the collector currents of transistors Q1, Q2, and Q4 equal to their respective input currents (I_1, I_2, and I_4). These op amps are designed with current-source outputs and are phase-compensated for optimum frequency response as a multiplier. Power drain of the op amps was minimized to prevent the introduction of undesired thermal gradients on the chip. The three op amps operate on a single-supply voltage (nominally -15V) and total quiescent current drain is less than 4 mA. These special op amps provide significantly improved performance in comparison to 741-type op amps.

The actual multiplication is done within the log-antilog configuration of the Q1-Q4 transistor array. These four transistors, with associated proprietary circuitry, were specially designed to precisely implement the relationship

$$V_{BEN} = \frac{kT}{q} \ln \frac{I_{CN}}{I_{SN}} \quad (2)$$

Previous multiplier designs have suffered from an additional undesired linear term in the above equation; the collector current times the emitter resistance. This $I_C r_E$ term can cause significant linearity error. In four-quadrant multiplier circuits, this added $I_C r_E$ term introduces a parabolic non-linearity even with matched transistors. Raytheon has developed a unique and proprietary means of inherently compensating for this undesired $I_C r_E$ term. Furthermore, this Raytheon-developed circuit technique compensates linearity error over temperature changes. The nonlinearity-versus-temperature is significantly improved over earlier designs.

From equation (2) and by assuming equal transistor junction temperatures, summing base-to-emitter voltage drops around the transistor array yields:

$$\frac{kT}{q}\left[\ln \frac{I_1}{I_{S1}} + \ln \frac{I_2}{I_{S2}} - \ln \frac{I_3}{I_{S3}} - \ln \frac{I_4}{I_{S4}}\right] = 0 \quad (3)$$

This equation reduces to:

$$\frac{I_1 I_2}{I_3 I_4} = \frac{I_{S1} I_{S2}}{I_{S3} I_{S4}} \quad (4)$$

The ratio of reverse saturation currents, $I_{S1} I_{S2} / I_{S3} I_{S4}$, depends on the transistor matching. In a monolithic multiplier this matching is easily achieved and the ratio is very close to unity, typically 1.0 ±1%. The final result is the desired relationship:

$$I_3 = \frac{I_1 I_2}{I_4} \quad (5)$$

The inherent linearity and gain stability combined with low cost and versatility makes this new circuit ideal for a wide range of nonlinear functions.

APPLICATIONS

FOUR-QUADRANT, GENERAL-PURPOSE MULTIPLIER

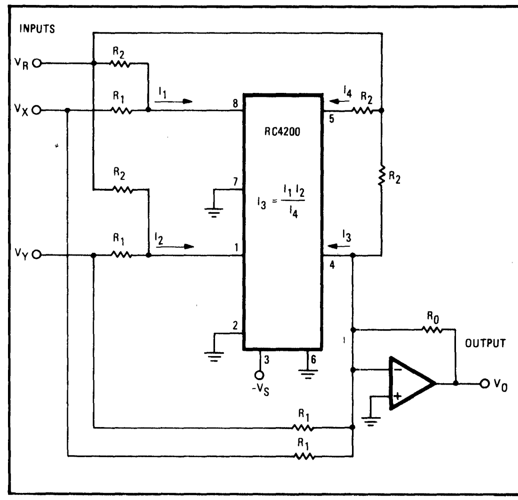


Figure 2. Four-Quadrant General Purpose Multiplier Using the RC4200

The general schematic for a four-quadrant multiplier using the RC4200 IC is shown in Figure 2. A positive reference voltage, V_R, is used to offset the multiplier chip. To stay within the most linear operating range, it is necessary that V_R/R_2 plus V_X/R_1 be limited to a range of 50µA to 250µA. Within the operating range, input and output currents are given by the following equations:

$$I_1 = \frac{V_X}{R_1} + \frac{V_R}{R_2} \qquad I_3 = \frac{V_X}{R_1} + \frac{V_Y}{R_1} + \frac{V_R}{R_2} + \frac{V_0}{R_0}$$

$$I_2 = \frac{V_Y}{R_1} + \frac{V_R}{R_2} \qquad I_4 = \frac{V_R}{R_2}$$

Combining these relationships through the equation $I_3 = I_1 I_2 / I_4$ yields:

$$V_0 = \frac{R_0 R_2}{R_1^2} \frac{V_X V_Y}{V_R}$$

The reference voltage V_R must be positive, but V_X and V_Y can be AC voltages. The positive supply voltage can be used as the reference in many applications where a well-regulated +15V is available. Some typical values for a multiplier scaled at $V_X V_Y/10$ are calculated below:

Given: V_X and V_Y have range of -10V to +10V.

Desired scaling is $V_0 = V_X V_Y / 10$

Reference voltage V_R is +15V

Calculation:

(1) Choose $R_1 = 100K\Omega$

From requirement of +50μA minimum

$$\frac{-10V}{100K} + \frac{15V}{R_2} = 50\mu A$$

Thus, R_2 would also need to be 100KΩ

(2) Calculate R_0 from $\frac{R_0 R_2}{R_1^2} \frac{1}{V_R} = \frac{1}{10}$,

$$R_0 = \frac{R_1^2}{R_2} \frac{V_R}{10}$$

$$R_0 = (100K\Omega) \frac{15}{10}$$

$$R_0 = 150K\Omega$$

Results:

$$V_0 = \frac{V_X V_Y}{10} \text{ with } V_R = +15V$$

$$R_1, R_2 = 100K\Omega$$

$$R_0 = 150K\Omega$$

These values cause a range on I_1 and I_2 of 50μA to 250μA for V_X and V_Y of -10V to +10V.

While the choice of values for R_1, R_2 and R_0 are arbitrary, best results are obtained by operating I_1 and I_2 over a range of approximately 50μA to 250μA.

Accuracy of the four-quadrant multiplier is dependent upon both the RC4200 chip and the external components. AC feedthrough, which is the undesired output when multiplying one AC input by zero on the other input, is dependent on op amp offsets and on the matching of the R_1 and R_2 resistor sets. Gain accuracy depends on the external reference voltage V_R, the resistor ratio $R_0 R_2/R_1^2$, and the multiplier chip. Linearity depends almost entirely upon the multiplier IC. The linear error terms can all be nulled externally by trimming resistor ratios or offsets. A four-quadrant multiplier with provision for external trimming of linear error components is shown in Figure 3. The optimum mix of component tolerances, trimming range, and cost is very application dependent. With moderate-cost components and no external trimming, the RC4200 is more accurate than many of the complete IC multipliers. With precision components and external trimming as shown in Figure 3, the RC4200 is capable of performance comparable to the best hybrid or modular multipliers.

The error analysis is most easily done by separately considering resistor match, offsets, and gain; then superimposing the results.

Resistor Matching

Assuming no op amp offsets and no error due to the multiplier chip, then the output would be the sum of the terms given below:

$$\text{Desired Output} = \frac{R_0 R_{2d}}{R_{1a} R_{1c}} \frac{V_X V_Y}{V_R}$$

$$V_Y \text{ Feedthrough} = \frac{R_0}{R_{1a}} \left(\frac{R_{2d}}{R_{2a}} - \frac{R_{1c}}{R_{1d}} \right) V_Y$$

$$V_X \text{ Feedthrough} = \frac{R_0}{R_{1a}} \left(\frac{R_{2d}}{R_{2b}} - \frac{R_{1a}}{R_{1b}} \right) V_X$$

$$\text{Output Offset} = \frac{R_0}{R_{2a}} \left(\frac{R_{2d}}{R_{2b}} - \frac{R_{2a}}{R_{2c}} \right) V_R^2$$

The AC feedthrough is directly proportional to the matching of the R_2 resistor set and the R_1 resistor set. AC feedthrough on the X or Y input is related to resistor tolerance as:

$$\text{AC Feedthrough} \sim \frac{R_0}{R_1} \times 2 \times \text{Res. Tol.} \times V_{IN}$$

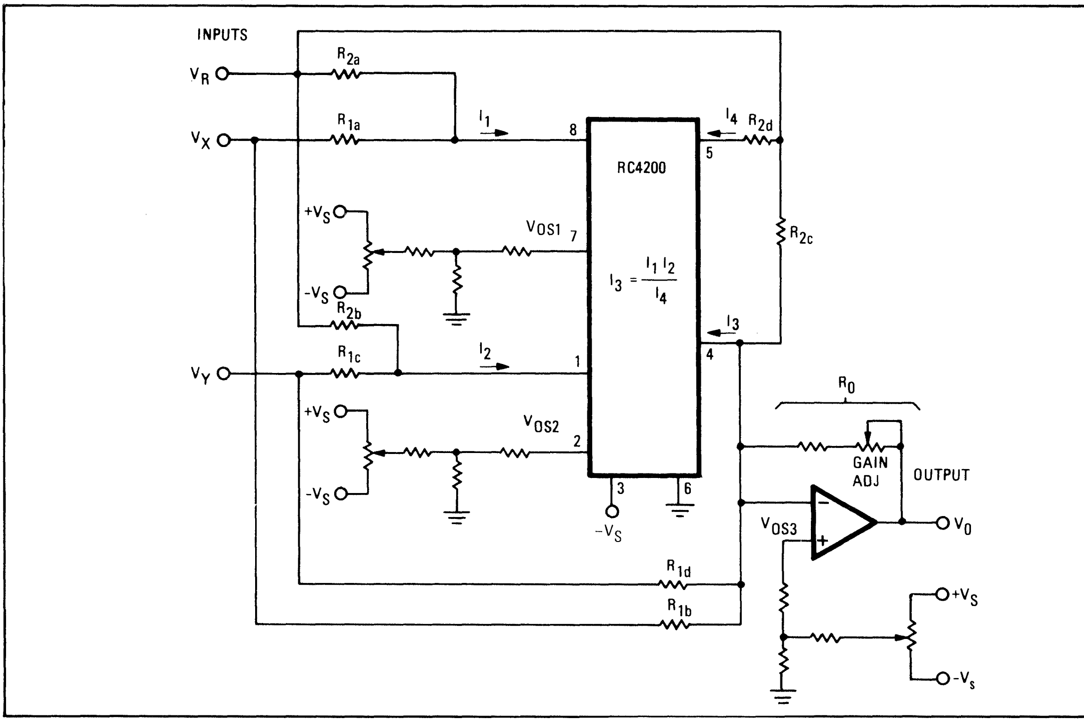


Figure 3. Four-Quadrant, General-Purpose Multiplier with Offset Adjustments

For example, if R_0/R_1 were 1.5 as in the example given previously and the resistors were matched to within 1%, then the maximum AC feedthrough due to resistor mismatch would be 3% of the V_X or V_Y input voltage. This AC feedthrough can be nulled directly by trimming the resistor sets or indirectly by trimming offsets.

Effect of Op Amp Offsets

In a multiplier, the offsets are cross multiplied and can thus cause AC feedthrough. When one input is zero and the other is a large AC signal, then the output will be the offset of the "zero" input times the AC signal. To quantify this effect, consider the circuit as shown in Figure 3. The offsets of each amplifier are due to both input offset voltage for the op amp and the input offset current times the source resistance.

These offsets can be lumped together into a single V_{OS} term. For this analysis, assume that the external resistors are perfectly matched (R_1's and R_2's all matched). The set of equations below must be combined to see their interaction:

$$I_1 = \frac{V_X - V_{OS1}}{R_1} + \frac{V_R - V_{OS1}}{R_2}$$

$$I_2 = \frac{V_Y - V_{OS2}}{R_1} + \frac{V_R - V_{OS2}}{R_2}$$

$$I_3 = \frac{V_X - V_{OS3}}{R_1} + \frac{V_Y - V_{OS3}}{R_1} + \frac{V_R - V_{OS3}}{R_2} + \frac{V_0 - V_{OS3}}{R_0}$$

$$I_4 = \frac{V_R - V_{OS4}}{R_2} \qquad I_3 = \frac{I_1 I_2}{I_4}$$

For simplicity, V_{OS}^2 terms and gain-error factors on error terms can be dropped. The output voltage would then be the sum of the terms given below:

$$\text{Desired Output} = \frac{R_0 R_2}{R_1^2}\frac{V_X V_Y}{V_R}$$

$$V_Y \text{ Feedthrough} = \frac{R_0}{R_1}\frac{1}{V_R}\left[V_{OS4} - \left(\frac{R_2}{R_1} + 1\right) V_{OS1}\right] V_Y$$

$$V_X \text{ Feedthrough} = \frac{R_0}{R_1}\frac{1}{V_R}\left[V_{OS4} - \left(\frac{R_2}{R_1} + 1\right) V_{OS2}\right] V_X$$

Output Offset =

$$\left(\frac{2R_0}{R_1} + \frac{R_0}{R_2} + 1\right) V_{OS3} - \left(\frac{R_0}{R_1} + \frac{R_0}{R_2}\right)(V_{OS1} + V_{OS2})$$

To estimate magnitudes, consider the previous example where R_0 = 150kΩ, R_1 and R_2 were 100kΩ, and V_R = 15V. Then,

$$V_Y \text{ Feedthrough} = \frac{1}{10}(V_{OS4} - 2V_{OS1})\ V_Y$$

$$V_X \text{ Feedthrough} = \frac{1}{10}(V_{OS4} - 2V_{OS2})\ V_X$$

$$\text{Output Offset} = 5.5\ V_{OS3} - 3\ (V_{OS1} + V_{OS2})$$

To carry this example further, let each V_{OS} term have a maximum value of ±10mV. The worst-case combination would then be a feedthrough of $0.003V_Y$ and $0.003V_X$. Output offset could be as high as 115mV, but would generally be less.

The trimming procedure is straight-forward when done in the following recommended sequence:

1. Apply a full-scale AC voltage to V_Y and make V_X zero. Trim V_{OS1} for output null ($V_O = 0$).
2. Apply the same full scale AC voltage to V_X and make V_Y zero. Trim V_{OS2} for output null $V_O = 0$).
3. Apply zero to both inputs ($V_X = 0$ and $V_Y = 0$). Trim V_{OS3} for output null ($V_O = 0$).
4. Adjust scale factor with R_O. Always adjust the input offsets before setting the scale factor.

In most applications, the offset adjustments are used to compensate for the R_1 and R_2 resistor network mismatch as well as the op amp offsets. Thus, the range of offset adjustment is usually chosen to encompass both error terms. For example, the V_Y feedthrough is:

$$\left\{\frac{R_0}{R_1}\left(\frac{R_{2d}}{R_{2b}} - \frac{R_{1a}}{R_{1b}}\right) + \frac{R_0}{R_1}\frac{1}{V_R}\left[V_{OS4} - \left(\frac{R_2}{R_1} + 1\right) V_{OS1}\right]\right\} V_Y$$

Varying V_{OS1} over sufficient range can compensate for both offset and resistor mismatch.

ONE-QUADRANT DIVIDER

Division is very easily implemented with the RC4200 multiplier when the inputs are all positive. The circuit for one-quadrant division is shown in Figure 4. The inputs V_X, V_Z, and V_R must be positive and the input currents I_1, I_2 and I_4 must be restricted in range. Within the rated range, $I_1\ I_2$ will equal $I_3\ I_4$ and therefore:

$$\left(\frac{V_X}{R_1}\right)\left(\frac{V_R}{R_2}\right) = \left(\frac{V_0}{R_0}\right)\left(\frac{V_Z}{R_4}\right)$$

$$V_0 = \frac{R_0 R_4}{R_1 R_2} V_R \frac{V_X}{V_Z}$$

The reference input V_R is generally fixed and the ratio of $R_0\ R_4/R_1\ R_2$ is usually chosen to make V_O = 10V at the maximum value of V_X/V_Z. For example, if V_R = 6.2V and V_X/V_Z maximum is one, then choose $R_0\ R_4/R_1 R_2$ of 10/6.2 which is 1.613. The output would then be:

$$V_0 = 10\frac{V_X}{V_Z},\ \text{where}\ \frac{V_X}{V_Z} \leq 1$$

As with the four-quadrant multiplier circuit, op amp offsets cross-multiply with the inputs. These offsets should be nulled to obtain best accuracy. The output voltage with offsets considered, but neglecting V_{OS}^2 terms, is given by:

$$V_0 = \underbrace{\frac{R_4R_0}{R_1R_2} V_R \frac{V_X}{V_Z}}_{\text{Ideal}} + \underbrace{\frac{R_4R_0}{R_1R_2}\left[\frac{V_RV_X}{V_Z^2} V_{OS4} - \frac{V_X}{V_Z} V_{OS2} - \frac{V_R}{V_Z} V_{OS1}\right] + V_{OS3}}_{\text{Error Terms}}$$

Because the offsets and signals are interactive, the recommended procedure for adjustment is the following:

1. Monitor the offsets at pins (8) and (1) directly and adjust V_{OS1}, V_{OS2} to null them. This removes the V_{OS1} and V_{OS2} error terms.
2. Make $V_X = V_Z$ and sweep over their full dynamic range. The output should be constant; vary the V_{OS4} ADJ pot for a constant output of $R_4 R_0 V_R/R_1 R_2$ plus V_{OS3}.
3. Apply the minimum value of V_X/V_Z and adjust V_{OS3} to obtain the proper V_O.
4. Apply the maximum value of V_X/V_Z and adjust R_0 for proper V_O.

The accuracy will be limited only by the nonlinearity, which for the RC4200 is very small.

SQUARE-ROOTING

The circuit for implementing the square-rooting function is shown in Figure 5. An input voltage V_X multiplied by a reference voltage V_R is made equal to the square of the output voltage. The relationship $I_1 I_2 = I_3 I_4$ becomes:

$$\frac{V_XV_R}{R_1R_2} = \frac{V_0^2}{R_0R_4}$$

The input voltage must be positive. Scaling is determined by the external resistor network and reference voltage V_R. The output voltage is given by:

$$V_0 = \sqrt{\frac{R_0R_4}{R_1R_2} V_R V_X}$$

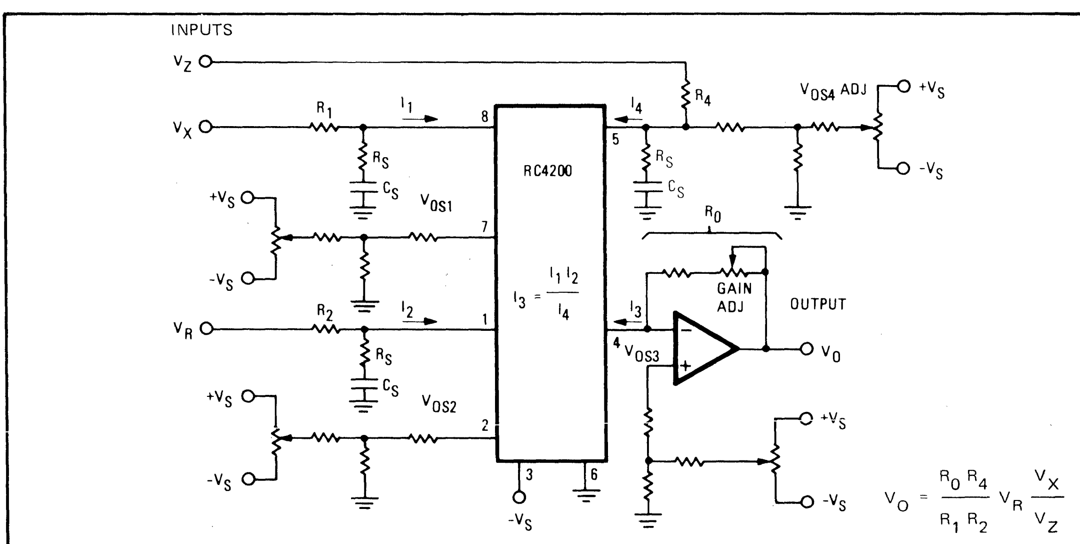


Figure 4. One-Quadrant Divider

RAYTHEON

In most applications, the resistors should be comparable in value and V_R should be in the range of 5V to 15V. A scale factor of 10 is very convenient and provides an output range of 0.3V to 10V for an input range of 10mV to 10V. In equation form:

$$V_O = \sqrt{10V_X}\ , \ 10\text{mV} < V_X < 10\text{V}$$

The offsets can be externally trimmed as needed. The nonlinear nature of the square-rooting function makes the error due to offsets very small for large inputs and very large at low input levels. With offsets included, the output voltage is:

$$V_O = \left[\frac{R_0R_4}{R_1R_2} V_R \left(1 - \frac{V_{OS2}}{V_R}\right) V_X - \frac{R_0R_4}{R_1R_2} V_R V_{OS1} + V_O \left(V_{OS3} + V_{OS4}\right)\right]^{1/2}$$

The term V_{OS2}/V_R affects gain only and is constant, therefore varying R_O can compensate for the V_{OS2} error term. The effect of V_{OS3} and V_{OS4} is additive and only one of these offsets need be adjusted. The V_{OS1} term should be trimmed to zero. The recommended trimming sequence is as follows:

1. Adjust V_{OS3} to zero directly by monitoring pin (4).
2. Apply minimum value of V_X and adjust V_{OS1} for correct V_O.
3. Apply maximum value of V_X and adjust R_O for correct V_O.

The square-rooting circuit can easily be designed for overall accuracy of ±0.2% when using the RC4200A IC multiplier.

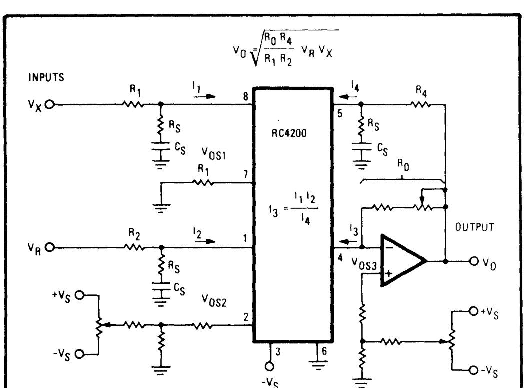


Figure 5. Square-Rooting Circuit

RMS-TO-DC CONVERTER

The root-mean-square value of a complex waveform can be computed directly by squaring, integrating, and then square rooting. The RC4200 is ideally suited to this computation and the entire RMS-to-DC conversion can be implemented with a single device.

A functional diagram is shown in Figure 6. An absolute-value circuit, or precision rectifier, first converts the AC input into a rectified positive voltage. Input currents I_1 and I_2 are made equal and will be $|V_{IN}|/R_1$. The remaining input current, I_4, is made equal to V_O/R_O plus a derivative term, $C_O dV_O/dt$. Combining these relationships according to $I_1 I_2 = I_3 I_4$,

$$\frac{V_{IN}^2}{R_1^2} = \frac{V_O}{R_1} + C_1 \frac{dV_O}{dt} \frac{V_O}{R_1}$$

This equation is equivalent to

$$V_O^2 + \frac{R_O C_O}{2} \frac{d}{dt}\left(V_O^2\right) = V_{IN}^2$$

The output voltage squared is the exponentially-weighted average of the input-voltage squared. Square-rooting both sides of the equation, and considering the polarity constraints inherent in this implementation, gives the desired results:

$$V_O = \sqrt{\overline{\left[V_{IN}(t)\right]^2}}$$

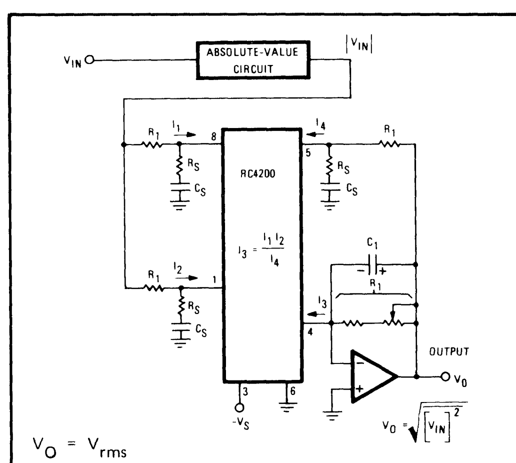


Figure 6. RMS-to-DC Converter

This is the true RMS value of V_{IN} within the frequency range where the averaging time constant $R_1 C_1/2$ is of sufficient magnitude for low-pass filtering. Capacitor C_1 must be large enough in value to adequately average the signal at its minimum frequency.

Various practical considerations limit performance for very small input signals, so this circuit is usually designed for a specific input voltage range. As with the divide and square-root modes of operation, the RC4200 may require a stabilizing $R_S C_S$ at the input summing junctions (pins 8, 1, and 5).

The specific component values and external adjustments needed depends on the particular application.

DESIGN CONSIDERATIONS

FREQUENCY RESPONSE AND STABILITY

The op amps within the RC4200 multiplier are stabilized for optimum performance in the four-quadrant multiplier configuration. At extremes of input current, the stability becomes marginal and external phase compensation may be required. The possibility of undesired oscillations should be considered for input currents of less than 50μA or greater than 500μA. Dividing and square-rooting operations often require a wide dynamic range on the input currents.

Two techniques are very helpful for assuring frequency stability and minimizing noise under a wide range of conditions:

1. Connect a series R_S C_S from input summing junction to ground as shown in Figure 7. This network has the effect of attenuating the feedback at high frequencies and thereby stabilizing the op amp. Loop gain at high frequencies is sacrificed, but this is seldom of concern in dividing or square-rooting applications. Recommended values are 10kΩ for R_S and 0.005μf for C_S.

2. The resistor on the noninverting input can be bypassed as shown in Figure 7. This helps to reduce noise.

The need for these frequency compensating techniques will depend on the application, particularly the input current range and input signal characteristics.

GAIN STABILITY

This type of multiplier is very sensitive to temperature gradients across the transistor quad (Q1 to Q4 and Q2 to Q3). The ambient temperature tends to affect offsets, but temperature gradients will cause a gain error. Several steps can be taken to minimize this effect:

1. Keep the multiplier physically remote from power dissipating components.

2. When using printed-circuit boards, make pad sizes and layout pattern as symmetrical as possible.

3. Heat sinking or epoxy potting can be used if necessary. This will tend to prevent rapid changes in temperature gradient.

Power drain within the multiplier chip itself is relatively low, therefore the gain stability can be very good if the IC is not exposed to temperature gradients.

OFFSET STABILITY

Input offset voltage of the op amps can be easily trimmed if desired. The effects of input bias current drift can be minimized by making the impedance approximately equal on the inverting and noninverting inputs. The equivalent input offset will then depend only on the difference in bias currents rather than the absolute values.

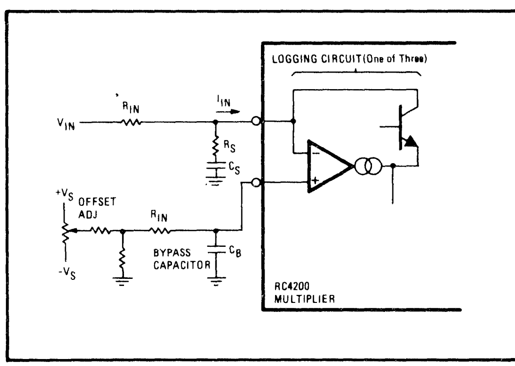


Figure 7. Optional Frequency Stability Components R_S, C_S, and C_B.

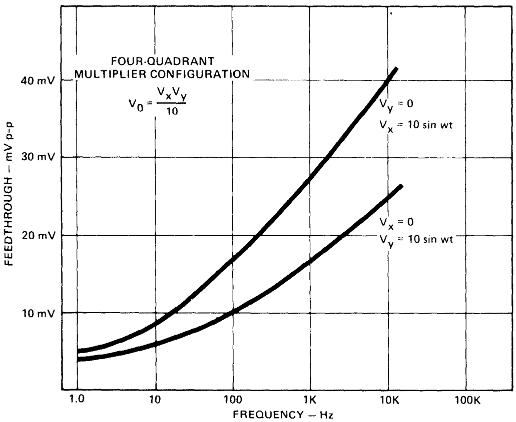


Figure 8. AC Feedthrough vs. Frequency

AVAILABLE TYPES

Part Type	Package	Operating Temperature
RM4200DE	Ceramic	-55 to +125°C
RV4200NB	Plastic	-40 to +85°C
RV4200DE	Ceramic	-40 to +85°C
RC4200DE	Ceramic	0 to +70°C
RC4200NB	Plastic	0 to +70 C
RM4200ADE	Ceramic	-55 to +125°C
RV4200ANB	Plastic	-40 to +85°C
RV4200ADE	Ceramic	-40 to +85°C
RC4200ADE	Ceramic	0 to +70°C
RC4200ANB	Plastic	0 to +70°C

HIGH RELIABILITY OPTIONS

Part Type	Added Screening	Order Part No.
RM4200DE RM4200ADE	With MIL-STD-883 Class B processing	RM4200DE3 RM4200ADE3
RV4200DE RC4200DE RV4200ADE RC4200ADE	With A + 3 processing* including burn-in and tightened AQL	RV4200DE3 RC4200DE3 RV4200ADE3 RC4200ADE3
RV4200NB RC4200NB RV4200ANB RC4200ANB	With A + 2 processing* including "Hot Rail" testing, burn-in, temp cycle and tightened AQL	RV4200NB2 RC4200NB2 RV4200ANB2 RC4200ANB2
RV4200NB RC4200NB RV4200ANB RC4200ANB	With A + 1 processing* including "Hot Rail" testing, temp cycle and tightened AQL	RV4200NB1 RC4200NB1 RV4200ANB1 RC4200ANB1

*Full descriptions contained in the quality section of this catalog.

GENERAL DESCRIPTION

The RC4444 is a monolithic dielectrically isolated crosspoint array arranged into a 4x4x2 matrix. The primary applications are for balanced switching of 600 ohm transmission lines. The ring and tip are selected by selective biasing of the P+ and P– gate.

Designed to replace reed-relays in telephone switchboards, it does not require a constant gate drive to keep the SCR in the "on" condition. It is several orders faster, with no bouncing, and has a much longer operating life than its mechanical counterpart.

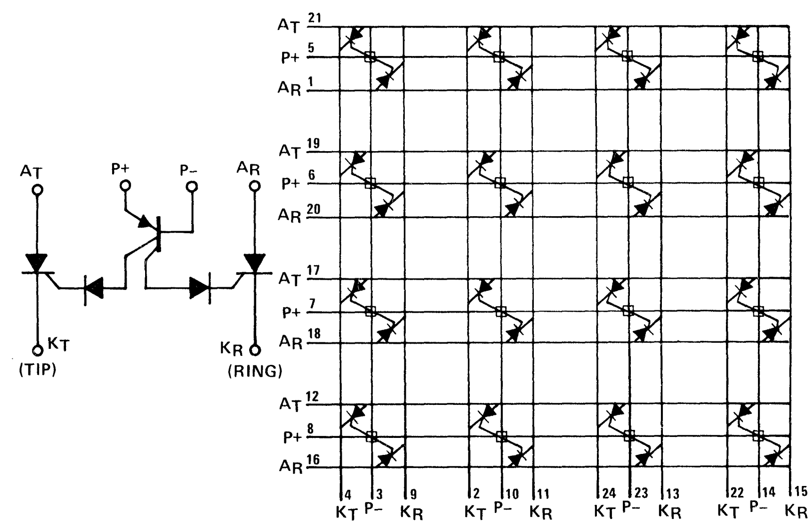
The 16 SCR pairs with the gating system are packaged in a 24 pin dual-in-line package.

The RC4444 is a monolithic pin-for-pin replacement for the MC3416 and MCBH7601.

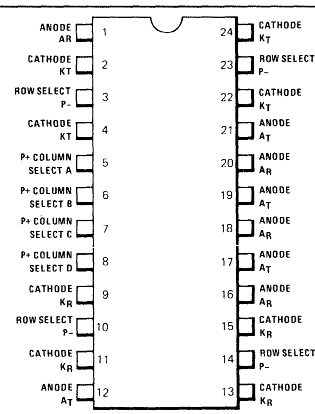
DESIGN FEATURES

- Low Bi-Directional R_{on}
- High R_{off}
- Excellent Matching of Gates
- Low Capacitance
- High Rate Firing
- Predictable Holding Current

SCHEMATIC DIAGRAM



CONNECTION INFORMATION



R and PU
Dual In-Line Packages

Order Part Nos.:
RC4444R, RC4444PU

ABSOLUTE MAXIMUM RATINGS

Operating Voltage (Note 1)	25V	Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation (Note 2)	900mW	Operating Temperautre Range	0°C to +70°C
Operating Current per Crosspoint (Note 2)	100mA	Lead Temperature (Soldering, 60s)	300°C

ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C unless otherwise noted)

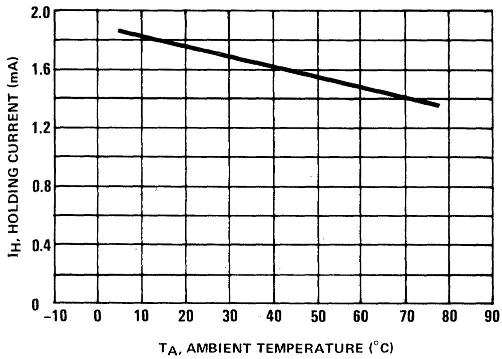
CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Anode-Cathode Breakdown Voltage (I_{AK} = 25μA)	BV_{AK}	25	–	Vdc
Cathode-Anode Breakdown Voltage (I_{KA} = 25μA)	BV_{KA}	25	–	Vdc
Base-Cathode Breakdown Voltage (I_{BK} = 25μA)	BV_{BK}	25	–	Vdc
Cathode-Base Breakdown Voltage (I_{KB} = 25μA)	BV_{KB}	25	–	Vdc
Base-Emitter Breakdown Voltage (I_{BE} = 25μA)	BV_{BE}	25	–	Vdc
Emitter-Cathode Breakdown Voltage (I_{EK} = 25μA)	BV_{EK}	25	–	Vdc
OFF State Resistance (V_{AK} = 10V)	r_{off}	100	–	MΩ
Dynamic ON Resistance	r_{on}			Ω
(Center Current = 10mA)		4.0	12	
(Center Current = 20mA)		2.0	10	
Holding Current (See Figure 10)	I_H	0.9	3.8	mA
Enable Current (V_{BE} = 1.5V)	I_{En}	4.0	–	mA
Anode-Cathode ON Voltage	V_{AK}			V
(I_{AK} = 10mA)		–	1.0	
(I_{AK} = 20mA)		–	1.1	
Gate Sharing Current Ratio @ Cathodes (Under Select Conditions with Anodes Open)	G_{Sh}	0.8	1.25	mA/mA
Inhibit Voltage (V_B = 3.0V)	V_{inh}	–	0.3	V
Inhibit Current (V_B = 3.0V)	I_{inh}	–	0.1	mA
OFF State Capacitance (V_{AK} = 0V)	C_{off}	–	2.0	pF
Turn-ON Time	t_{on}	–	1.0	μs
Minimum Voltage Ramp (Which Could Fire the SCR Under Transient Conditions)	dv/dt	800	–	V/μs

NOTES:

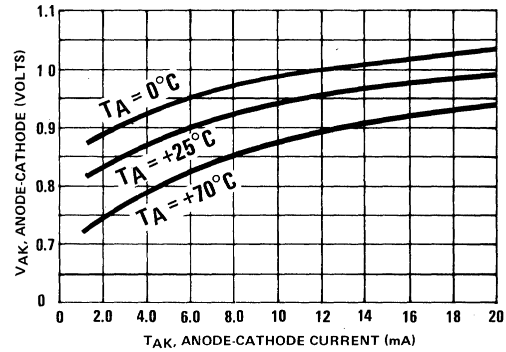
1. Maximum voltage from anode to cathode.
2. Package thermal resistance θ_{JA} typically .055°C/mW. Package power dissipation limited to 900mW.

TYPICAL APPLICATIONS

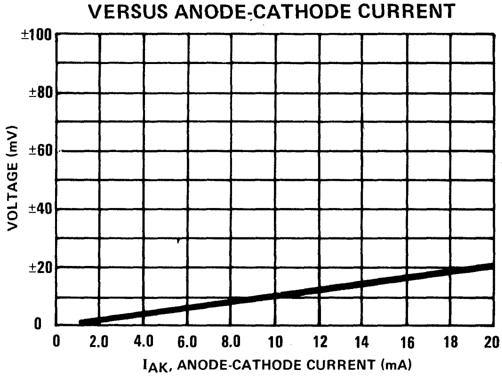
HOLDING CURRENT VERSUS AMBIENT TEMPERAUTRE



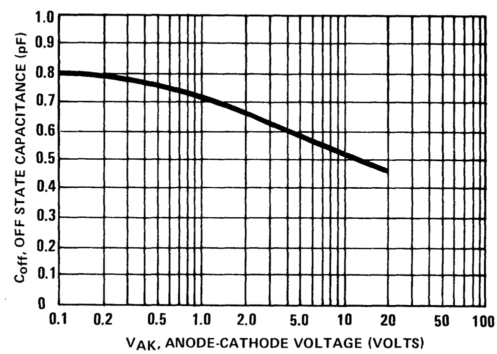
ANODE-CATHODE ON VOLTAGE VERSUS CURRENT AND TEMPERATURE



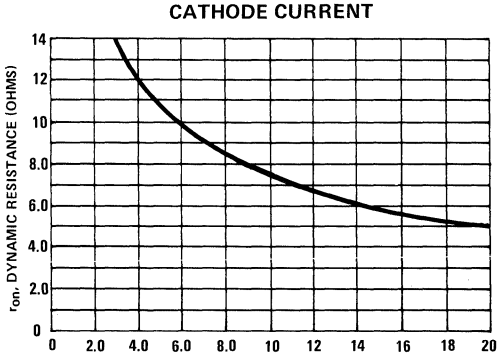
DIFFERENCE IN ANODE-CATHODE ON VOLTAGE (Between Associate Pairs of SCR's) VERSUS ANODE-CATHODE CURRENT



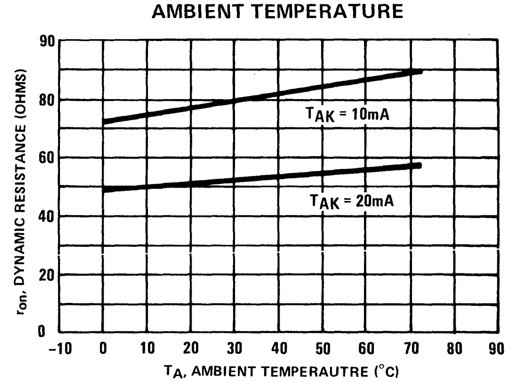
OFF-STATE CAPACITANCE VERSUS ANODE CATHODE VOLTAGE



DYNAMIC ON RESISTANCE VERSUS ANODE-CATHODE CURRENT

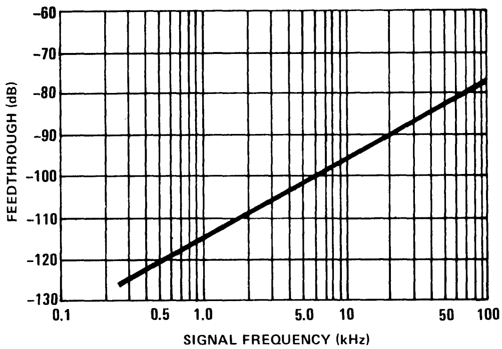


DYNAMIC ON RESISTANCE VERSUS AMBIENT TEMPERATURE

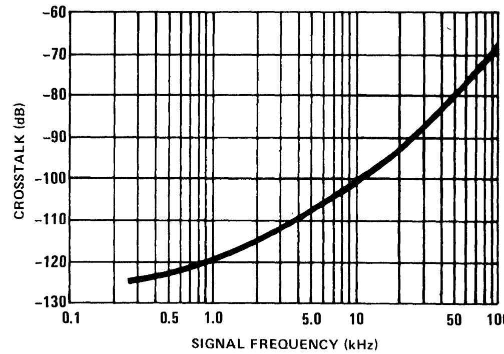


TYPICAL APPLICATIONS

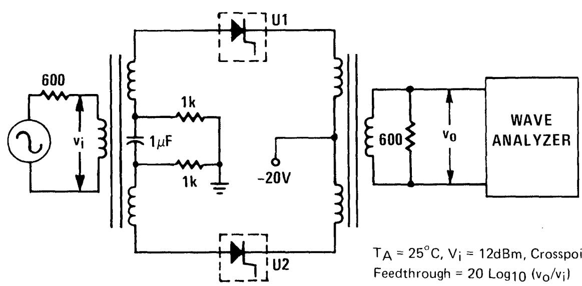
FEEDTHROUGH VERSUS SIGNAL FREQUENCY



CROSSTALK VERSUS SIGNAL FREQUENCY

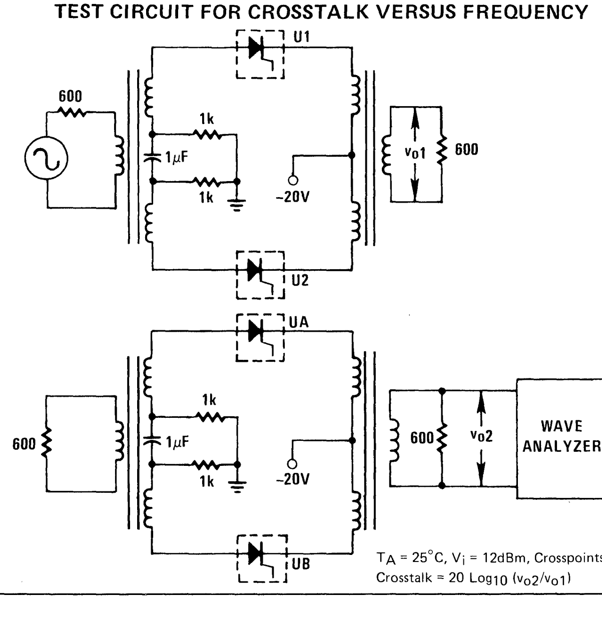


TEST CIRCUIT FOR FEEDTHROUGH VERSUS FREQUENCY

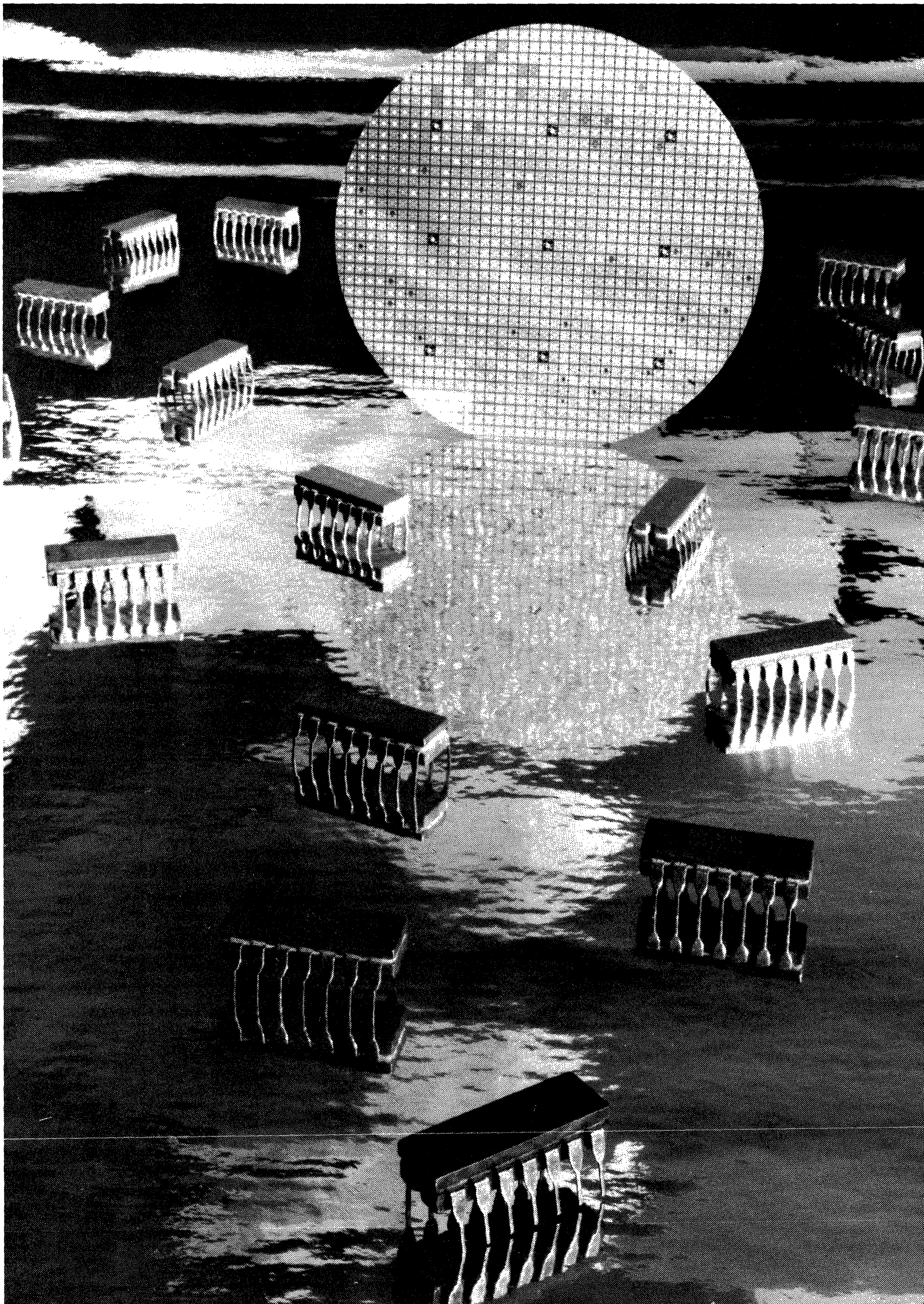


$T_A = 25°C$, $V_i = 12dBm$, Crosspoints Off
Feedthrough = 20 Log_{10} (v_o/v_i)

TEST CIRCUIT FOR CROSSTALK VERSUS FREQUENCY



$T_A = 25°C$, $V_i = 12dBm$, Crosspoints On
Crosstalk = 20 Log_{10} (v_{o2}/v_{o1})

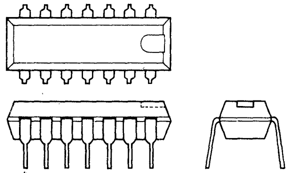
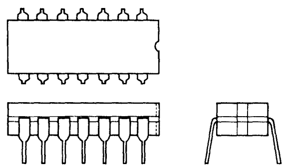
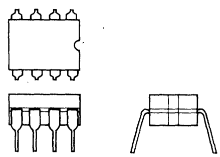
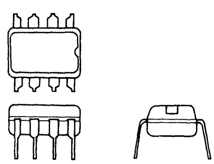
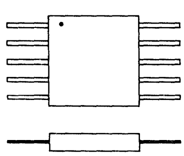
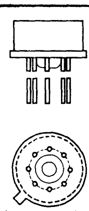


SECTION 8

Packaging Information and Beam Lead Products

CONTENTS

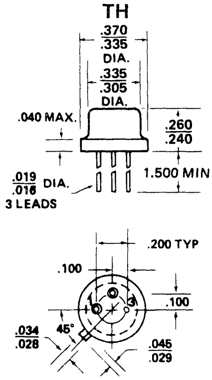
Industry Cross ReferenceGuide

Package	Raytheon	Fairchild	NSC	Signetics	Motorola	TI	RCA
 PLASTIC DIP VARIATIONS	DB MB DN(1)	P	N	A, B	P	N	
 CERAMIC DIP (14 or 16-Lead)	DC DD DF(2) DM(2)	D	D	I	L		D
 CERAMIC MINI DIP	DE	R	J		L	J	
 PLASTIC MINI DIP	NB	T	N	V	P	P	E
 FLATPAK VARIATIONS (10, 14 or 16-Lead)	CJ CL CQ	F	F, W	Q	F	F, S, W	K
 TO-99, TO-100, TO-5	TE TF TH	H	H	T, K, L, DB	G	L	S, V1

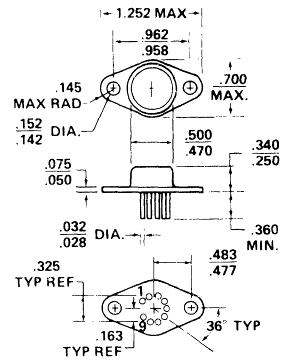
NOTES:

1. 24-pin package.
2. Large cavity.

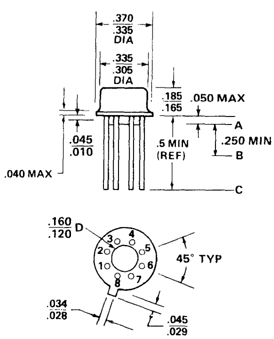
3-LEAD
TO-5 PACKAGE
TH



10-LEAD
TO-66 PACKAGE
TK



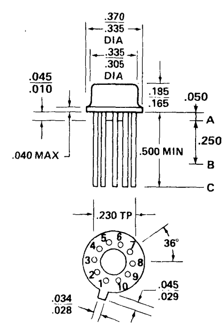
8-LEAD
TO-99 PACKAGE
TE



BETWEEN PT A AND PT B LEAD DIA IS $\frac{.019}{.016}$

BETWEEN B & C $\frac{.021}{.016}$

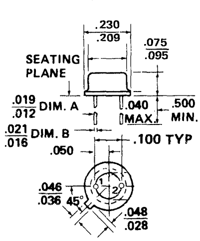
10-LEAD
TO-100 PACKAGE
TF



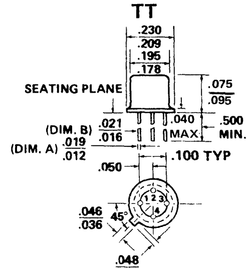
BETWEEN PT A AND PT B LEAD DIA IS $\frac{.019}{.016}$

BETWEEN B & C $\frac{.021}{.016}$

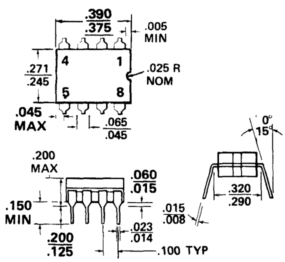
2-LEAD
TO-46 PACKAGE
TR



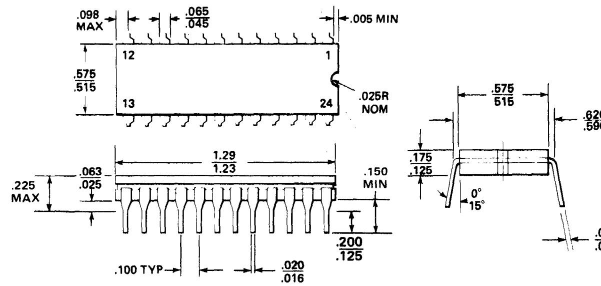
4-LEAD
TO-46 PACKAGE
TT



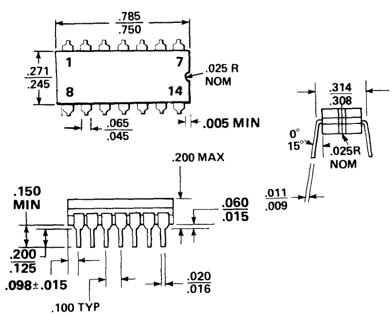
8-LEAD CERAMIC DIP
DE



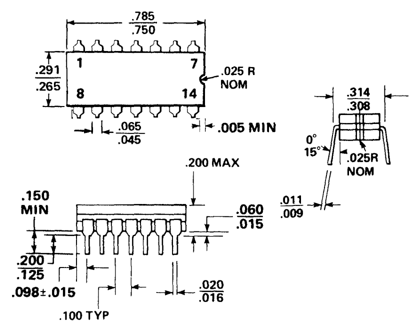
24-LEAD
CERAMIC PACKAGE
R



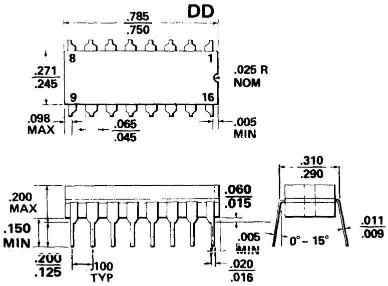
14-LEAD CERAMIC DIP
DC



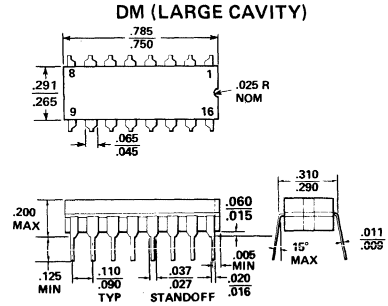
14-LEAD CERAMIC DIP
DF (LARGE CAVITY)



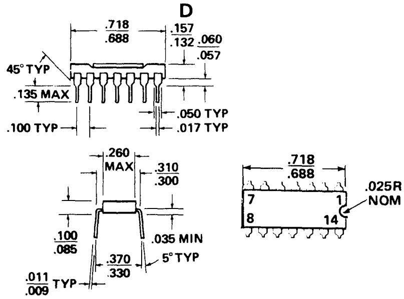
16-LEAD
CERAMIC PACKAGE
DD



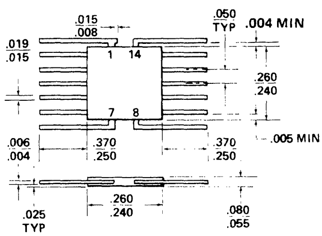
16-LEAD
CERAMIC PACKAGE
DM (LARGE CAVITY)



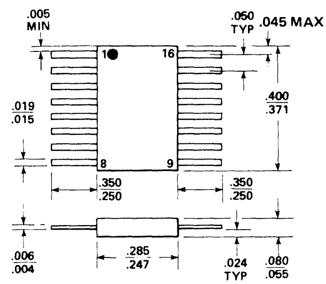
14-LEAD METAL DIP
D



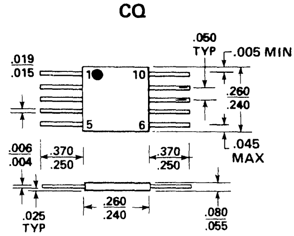
14-LEAD CERAMIC FLAT PACKAGE
CJ



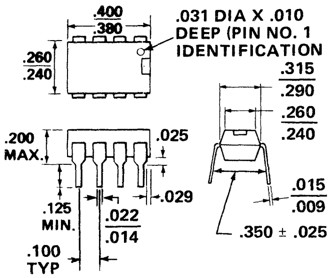
16-LEAD CERAMIC FLAT PACKAGE
CL



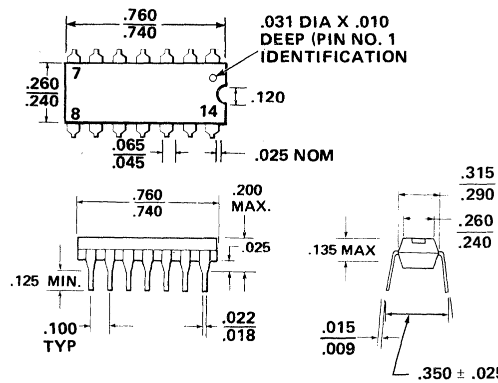
10-LEAD CERAMIC FLAT PACKAGE
CQ



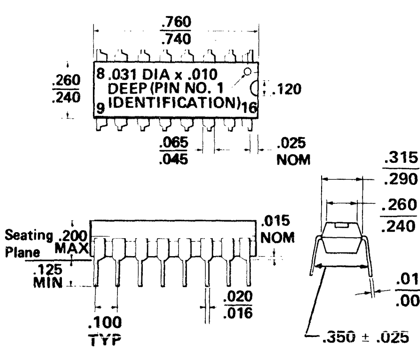
8-LEAD PLASTIC DIP
NB



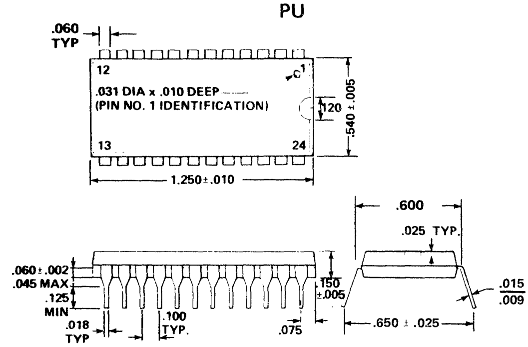
14-PIN PLASTIC DIP
DB/BD



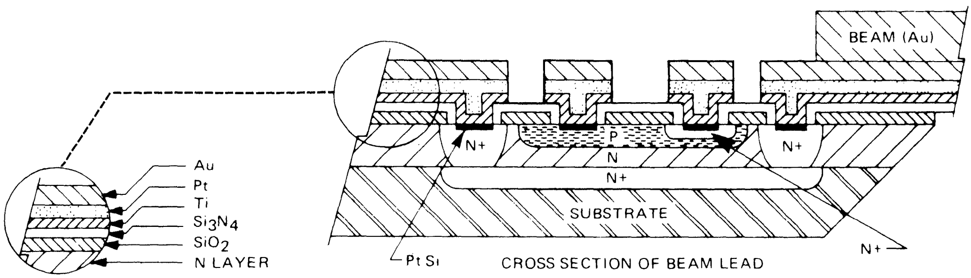
16-LEAD PLASTIC DIP
BM/MB



24-LEAD PLASTIC DIP
PU



Typical Beam Lead Cross Section with Interconnections



CROSS SECTION OF BEAM LEAD DEVICE WITH INTERCONNECTIONS

Ordering Information

Beam Lead Linear IC's may be ordered either as military or commercial grade devices:

RM = −55°C to +125°C operating temperature range, B-level visual.

RC = 0°C to +70°C, C-level visual.

Examples

RM101ABL

Military Specifications — Product Type No. — Beam Lead Device

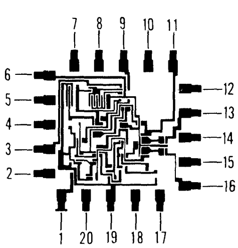
RC104BL

Commercial Specifications — Product Type No. — Beam Lead Device

101A GENERAL PURPOSE OPERATIONAL AMPLIFIER

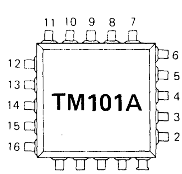
Order Part Nos.: RM101ABL, RC101ABL

Die Size: 58 x 60 mils.



ACTIVE SIDE

Mechanical Outline 16



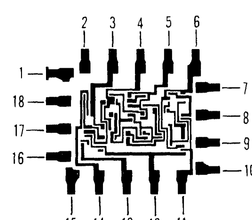
AS BONDED

1. BAL	6. $+V_{CC}$	11. COMP/BAL	16. +INPUT
2. NC	7. NC	12. NC	17. NC
3. OUTPUT	8. NC	13. −INPUT	18. NC
4. NC	9. COMP	14. NC	19. $-V_{CC}$
5. NC	10. NC	15. NC	20. NC

105 POSITIVE VOLTAGE REGULATOR

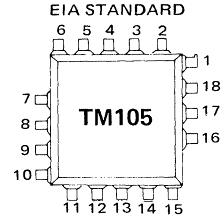
Order Part Nos.: RM105BL, RC105BL

Die Size: 53 x 63 mils.



ACTIVE SIDE

Mechanical Outline 22
EIA STANDARD



AS BONDED

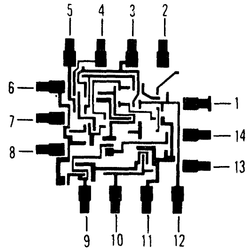
1. NC	5. GND	10. NC	15. NC
2. NC	6. BYPASS	11. FEEDBACK	16. NC
3. BOOSTER OUTPUT	7. NC	12. COMP	17. NC
4. UNREG INPUT	8. NC	13. REG OUTPUT	18. NC
	9. NC	14. CURRENT LIMIT	

709 GENERAL PURPOSE / 709A OPERATIONAL AMPLIFIER

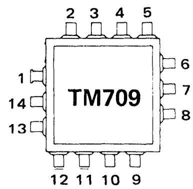
Die Size: 48 x 48

Order Part Nos.: RM709BL, RM709ABL, RC709BL

Mechanical Outline 8



ACTIVE SIDE



AS BONDED

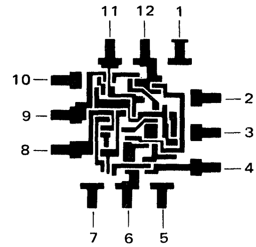
1. NC	5. +INPUT	9. OUTPUT COMP	12. INPUT COMP
2. NC	6. $-V_{CC}$	10. OUTPUT	13. NC
3. INPUT COMP	7. NC	11. $+V_{CC}$	14. NC
4. −INPUT	8. NC		

710 GENERAL PURPOSE COMPARATOR

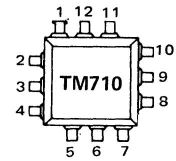
Die Size: 41 x 41 mils.

Order Part Nos.: RM710BL, RM710ABL, RC710BL

Mechanical Outline 5



ACTIVE SIDE



AS BONDED

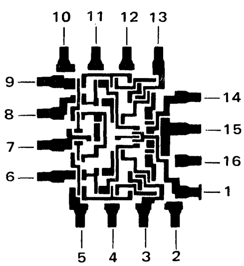
1. NC	4. +INPUT	7. NC	10. NC
2. NC	5. NC	8. $-V_{CC}$	11. $+V_{CC}$
3. NC	6. −INPUT	9. OUTPUT	12. GND

711 DUAL COMPARATOR

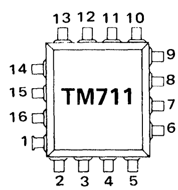
Die Size: 44 x 49 mils.

Order Part Nos.: RM711BL, RC711BL

Mechanical Outline 9



ACTIVE SIDE



AS BONDED

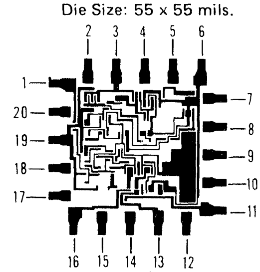
1. GND	5. −INPUT (A)	9. −INPUT (B)	13. STROBE 2
2. NC	6. +INPUT (A)	10. NC	14. OUTPUT
3. STROBE 1	7. $-V_{CC}$	11. NC	15. $+V_{CC}$
4. NC	8. +INPUT (B)	12. NC	16. NC

1741 GENERAL PURPOSE OPERATIONAL AMPLIFIER

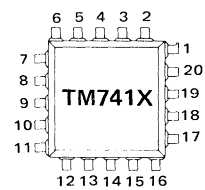
Die Size: 55 x 55 mils.

Order Part Nos.: RM1741BL, RC1741BL

Mechanical Outline 15
EIA STANDARD



ACTIVE SIDE



AS BONDED

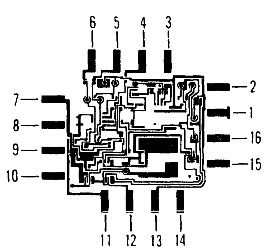
1. BALANCE	6. $+V_{CC}$	11. BALANCE	16. +INPUT
2. NC	7. NC	12. NC	17. NC
3. OUTPUT	8. NC	13. −INPUT	18. NC
4. NC	9. NC	14. NC	19. $-V_{CC}$
5. NC	10. NC	15. NC	20. NC

4132 MICRO POWER OPERATIONAL AMPLIFIER

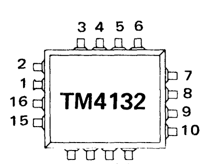
Die Size: 64 x 74 mils.

Order Part Nos.: RM4132BL, RC4132BL

Mechanical Outline 14



ACTIVE SIDE



AS BONDED

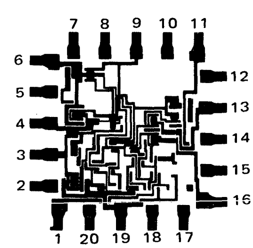
1. NC	5. −INPUT	9. NC	13. V^+
2. NC	6. +INPUT	10. NC	14. NC
3. NC	7. $-V_{CC}$	11. BAL	15. NC
4. BAL	8. NC	12. OUTPUT	16. NC

748 OPERATIONAL AMPLIFIER

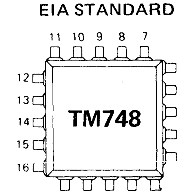
Die Size: 55 x 55

Order Part Nos.: RM748BL, RC748BL

Mechanical Outline 15
EIA STANDARD



ACTIVE SIDE



AS BONDED

1. BAL	6. $+V_{CC}$	11. BAL	16. +INPUT
2. NC	7. NC	12. NC	17. NC
3. OUTPUT	8. NC	13. −INPUT	18. NC
4. COMP	9. COMP	14. NC	19. $-V_{CC}$
5. NC	10. NC	15. NC	20. NC

RAYTHEON

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