ExpressLane PEX 8311AA

PCI Express-to-Generic Local Bus Bridge

Data Book

Version	1.0

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Website	www.plxtech.com
Technical Support	www.plxtech.com/support
Phone	800 759-3735
	408 774-9060
FAX	408 774-2169

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Revision History

Version	Date	Description of Changes
1.0	December, 2009	Initial Production Release, Silicon Revision AA. Security category changed. Terms and abbreviations – Local Bus Mode, Tx ant Rx definitions updated. Chapter 1: commercial temperature range details changed Chapter 2: • Local Bus Mode details changed, Tables 2-4, 2-5 • Reference to AL_BTT24_U buffer removed, Table 2-8 • Miscellaneous signals, CLKIN and CLKOUT details added, Table 2-10 • JTAG interface, TRST# details changed, Table 2-11 • Test signal, IDDQEN# resistor value changed, Table 2-12 • No connect pins description changed, Table 2-13 • References to 9054 removed, Section 2.4 Chapter 7: • Timing diagram numbering corrected • Removal of Reset Operaiton and Direct Data Transfer Mode sections Chapter 8: reference to LCS_PCIBAR0 added, section 8.3.2.2 Chapter 9, changes to: • Direct Master Delayed Read Mode section restructured, Section 9.2.6 • Direct Master Read Ahead Mode details changed, Section 9.2.7 • Internal PCI Bus Master/Target Abort details changed, Section 9.2.9 • Direct Master Write FIFO Programmable Almost Full, Section 9.2.11 • IDMA OPeration details changed, Section 9.2.13 • Direct Slave Writes details changed, Section 9.3.1.2 • Direct Slave Delayed Read Mode PCI details added, Seciton 9.3.4.2 • Slave Transfer Error now M mode only, Section 9.3.9 • Figures 9-9 and 9-10 changed order • Replaced DMA Demand Mode, Channel x – C and J Modes, Section 9.5.13.1 • Replaced DMA Demand Mode, Channel x – M Mode, section 9.5.13.2 • Removal of Fast Terminate Mode Operation section • Removal of Slow Terminate Mode Operation section • Removal of End of Transfer Input section Chapter 12: • Figure 12-1 changed • Endpoint Mode Local Interrupts note changed, Section 12.3 Chapter 14: • Endpoint Mode PCI Express-PM Device Power States recovery time detaios changed, Seciton 14.2.4 Chapter 19: • Register 19-25. Offset 24h PECS_PREBASE Prefetchable Memory Base bits 3:0 • Register 19-48. Offset 52h PECS_MSICTL Message Signaled Interrupts Control bit 0 • Register 19-56. Offset 68h PECS_DEVCTL PCI Express Device Control bit 10 • Register 19-89. Offset 1040h PECS_CHIPREV Chip Silicon Revision bits 15:0 • Register 19-92. Offset 104Ch PECS_TLPCFG1 TLP Controller Configuration 1 bits 13:21 Chapter 23: Recommended Operating Conditions, operating temperature note added, Section 23.5 Chapter 24: • PEX 8311 Package Thermal Resistance values changed, Table 24-2 • Mechanical dimensions image changed, Figure 24-1

Preface

The information contained in this data book is subject to change without notice. This data book will be updated periodically as new information is made available.

Scope

This data book is the primary source of technical documentation describing the features, functions and operations of the PLX Technology PEX 8311 PCI Express-to-Generic Local Bus Bridge.

Intended Audience

This data book provides functional details of PLX Technology's ExpressLane PEX 8311AA PCI Express-to-Generic Local Bus Bridge, for hardware designers and software/firmware engineers.

Supplemental Documentation

This data book assumes that the reader is familiar with the following documents:

- PLX Technology, Inc. (PLX)

  870 W Maude Avenue, Sunnyvale, CA 94085 USA

  Tel: 800 759-3735 (domestic only) or 408 774-9060, Fax: 408 774-2169, www.plxtech.com

  The PLX PEX 8311 Toolbox includes this data book, as well as other PEX 8311 documentation, including the Errata.

- PCI Special Interest Group (PCI-SIG)

  3855 SW 153rd Drive, Beaverton, OR 97006 USA

  Tel: 503 619-0569, Fax: 503 644-6708, www.pcisig.com

    – *PCI Local Bus Specification, Revision 3.0*
    – *PCI Local Bus Specification, Revision 2.2*
    – *PCI Local Bus Specification, Revision 2.1*
    – *PCI to PCI Bridge Architecture Specification, Revision 1.1*
    – *PCI Bus Power Management Interface Specification, Revision 1.1*
    – *PCI Hot Plug Specification, Revision 1.1*
    – *PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0*
    – *PCI Express Base Specification, Revision 1.0a*
    – *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
    – *PCI Express Card Electromechanical Specification, Revision 1.1*

- The Institute of Electrical and Electronics Engineers, Inc. (IEEE)

  445 Hoes Lane, Piscataway, NJ 08854-4141 USA

  Tel: 800 701-4333 (domestic only) or 732 981-0060, Fax: 732 981-9667, www.ieee.org

    – *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990*
    – *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
    – *IEEE Standard 1149.1b-1994, Specifications for Vendor-Specific Extensions*

- I$_2$O Special Interest Group (I$_2$O SIG®)

  www.developer.osdl.org/dev/opendoc/Online/Local/I20/index.html

    – *Intelligent I/O (I$_2$O) Architecture Specification, Revision 1.5*

- Other References

    – *Advanced Configuration and Power Interface (ACPI) Specification, Revision 2.0*

Supplemental Documentation Abbreviations

Note: In this data book, shortened titles are provided to the previously listed documents. The following table defines these abbreviations.

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
PCI r2.2	*PCI Local Bus Specification, Revision 2.2*
PCI r2.1	*PCI Local Bus Specification, Revision 2.1*
PCI-to-PCI Bridge r1.1	*PCI to PCI Bridge Architecture Specification, Revision 1.1*
PCI Power Mgmt. r1.1	*PCI Bus Power Management Interface Specification, Revision 1.1*
PCI Hot Plug r1.1	*PCI Hot Plug Specification, Revision 1.1*
PCI Standard Hot Plug r1.0	*PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0*
PCI Express Base 1.0a	*PCI Express Base Specification, Revision 1.0a*
PCI Express-to-PCI/ PCI-X Bridge r1.0	*PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
PCI Express CEM 1.1	*PCI Express Card Electromechanical Specification, Revision 1.1*
I₂O r1.5	*Intelligent I/O (I₂O) Architecture Specification, Revision 1.5*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*

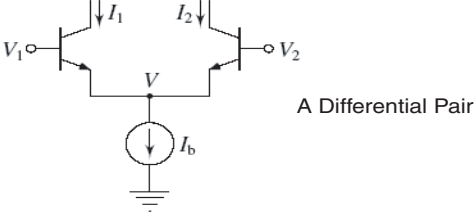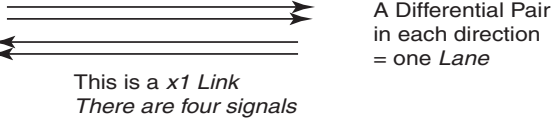## Data Assignment Conventions

Data Width	PEX 8311 Convention
Half byte (4 bits)	Nibble
1 byte (8 bits)	Byte
2 bytes (16 bits)	Word
4 bytes (32 bits)	DWORD/DWord/Dword
8 bytes (64 bits)	QWORD/QWord/Qword

Terms and Abbreviations

The following table provides common terms and abbreviations used in this data book. Terms and abbreviations defined in the *PCI Express r1.0a* are not included in this table.

Terms and Abbreviations	Definition
#	Indicates an Active-Low signal.
ACK	Acknowledge Control Packet. A control packet used by a destination to acknowledge data packet receipt. A signal that acknowledges the signal receipt.
ADB	Allowable Disconnect Boundary.
Asynchronous	Inputs and Outputs can be asynchronous to a clock. Level-sensitive signals.
BAR	Base Address Register.
CA	Completion with Completer Abort status.
CFG	Access initiated by PCI Express Configuration transactions on the primary interface.
Clock cycle	One period of the clock.
Completer	Device addressed by a *Requester*.
CRS	Configuration Retry Status.
CSR	Configuration Status register; Control and Status register; Command and Status register.
DAC	Dual Address cycle. A PCI Express transaction wherein a 64-bit address is transferred across a 32-bit data path in two Clock cycles.
Destination Bus	Target of a transaction that crosses a bridge is said to reside on the destination bus.
DLLP	Data Link Layer Packet (originates at the Data Link Layer); can contain Flow Control (FCx DLLPs) acknowledge packets (ACK and NAK DLLPs); and power management (PMx DLLPs).
DM	Direct Master. A type of transfer that originates from an external Local Bus Master and addresses a device in PCI Express Space.
DMA	Direct Memory Access. Method of transferring data between a device and main memory, without CPU intervention.
Downstream	Transactions that are forwarded from the primary interface to the secondary interface of a bridge are said to be *flowing downstream*.
DS	Direct Slave. A type of transfer that originates from PCI Express Space and addresses a device on the Local Bus.
ECRC	End-to-end Cyclic Redundancy Check (CRC)
EE	Access initiated by the Serial EEPROM Controller during initialization.
Endpoint mode	The primary interface is the PCI Express interface. The secondary interface is the Local Bus interface.
Endpoints	Devices, other than the Root Complex and switches, that are requesters or completers of PCI Express transactions, as follows: • Endpoints can be PCI Express endpoints or Conventional PCI endpoints. • Conventional PCI endpoints can support I/O and Locked transaction semantics. PCI Express endpoints do **not support** I/O nor Locked transaction semantics.
FCP	Flow Control Packet devices on each Link exchange FCPs, which carry *header* and *data payload* credit information for one of three packet types – Posted requests, Non-Posted requests, and Completions.

Terms and Abbreviations	Definition
Host	Computer that provides services to computers that connect to it on a network. Considered in charge of the other devices connected to the bus.
I	CMOS Input.
I/O	CMOS Bi-Directional Input/Output.
JTAG	Joint Test Action Group
Lane	A PCI Express physical data Link consisting of a differential signal pair in each direction.
Layers	PCI Express defines three layers: • *Transaction Layer* – The primary function of the Transaction Layer is TLP assembly and disassembly. The major components of a transaction layer packet (TLP) are *Header*, *Data Payload*, and an optional *Digest* field. • *Data Link Layer* – The primary task of the Data Link Layer is to provide Link management and data integrity, including error detection and correction. This layer defines the data control for PCI Express. • *Physical Layer* – The primary value to users is that this layer appears to the upper layers as PCI. It connects the lower protocols to the upper layers.
LCPU	Local Bus Central Processing Unit (Local Bus Intelligent Device).
LCS	Local Configuration Space.
Local Bus	Interface that provides an interconnect of other components to a PLX device.
Local Bus Modes	The PEX 8311 supports three Local Bus modes – C, J, and M: • **C** – Non-Multiplexed Local Bus interface based on 80960CX Processor Protocol • **J** – Multiplexed Local Bus interface based on 80960JX RISC Processor Protocol • **M** – *Motorola MPC850/MPC860 and IBM PowerPC 801*
Local Bus Master	Local Bus device that initiates transfers.
Local Bus Slave (Target)	Bus device that responses to Local Bus Master-initiated transactions.
Local Configuration Space (**LCS**)	The register set used to configure and control operations on the PEX 8311 Local Bus.
LTSSM	Link Training and Status State Machine.
MM	PCI Express Configuration Space (**PECS**) Register access initiated by PCI Express Memory transactions on the primary or secondary interface, using the address range defined by the **PECS_PCIBASE0** register.
MSI	Message Signaled Interrupt.
MWI	Memory Write and Invalidate.
NAK	Negative Acknowledge.
NMI	Non-Maskable Interrupt – the highest-priority interrupt recognized.
Non-Posted Transaction	Memory Read, I/O Read or Write, or Configuration Read or Write that returns a completion to the master.
NS	No Snoop.
O	CMOS Output.
OD	Open Drain Output.
Originating Bus	Master of a transaction that crosses a bridge is said to reside on the *originating bus*.
Packet Types	There are three packet types: • *TLP*, Transaction Layer Packet • *DLLP*, Data Link Layer Packet • *PLP*, Physical Layer Packet

Terms and Abbreviations	Definition
PCI	Peripheral Component Interconnect. The original 32/64-bit parallel interconnect standard, defined in the *PCI r2.2*. When listed in the signal tables, indicates PCI compliance.
PCI Express Configuration Space (**PECS**)	The register set used to initialize, enumerate, and operate the PEX 8311's PCI Express interface.
PCI Express Requester	Generates a "Request" packet, thereby initiating a transaction on the PCI Express interface.
PCI Express Target	Returns data and/or completions on the PCI Express interface, to the Requester.
PCI Express Transaction	Read, write, read burst, or write burst operation on the PCI Express interface. Includes an Address phase, followed by one or more Data phases.
PCI Express Transfer	During a transfer, data is moved from the source to the destination on the PCI Express interface or Local Bus.
PECS	PCI Express Configuration Space.
PEX	PCI Express.
Port	Interface between a PCI Express component and the *Link*. Consists of transmitters and receivers, as follows: • An *ingress* port receives a packet. • An *egress* port transmits a packet. • A *Link* is a physical connection between two devices that consists of x*N lanes*. • A x1 Link consists of one Transmit and one Receive signal, wherein each signal is a differential pair. This is one lane. There are four lines or signals in a x1 Link.
Posted Transaction	Memory Write that does not return a completion to the master.
Preempt	Ongoing transaction is interrupted to perform another transaction.
Primary Interface	Interface closest to the PCI Express Root Complex (Endpoint mode) or the Local host CPU (Root Complex mode).
PU	Signal is internally pulled up.

Terms and Abbreviations	Definition
QoS	Quality of Service.
RC	Root Complex.
RCB	Read Boundary Completion.
Request packet	A *Non-Posted Request packet* transmitted by a Requester contains a completion packet returned by the associated completer. A *Posted Request packet* transmitted by a Requester does not contain a completion packet returned by the completer.
Requester	Device that originates a transaction or places a transaction sequence into the PCI Express fabric.
RO	Relaxed Ordering.
RoHS	Restrictions on the use of certain Hazardous Substances (RoHS) Directive.
Root Complex	Denotes the device that connects the CPU and memory subsystem to the PCI Express fabric. It can support one or more PCI Express ports.
Root Complex Mode	The primary interface is the Local Bus interface. The secondary interface is the PCI Express interface.
Rx	Receiver.
SC	Successful Completion.
Secondary Interface	The interface farthest from the PCI Express Root Complex (Endpoint mode) or the Local host CPU (Root Complex mode).
SPI	Serial Peripheral Interface
STRAP	Strapping pads (*such as*, BAR0ENB#, IDDQN#, MODE[1:0], and USERi) must be connected to H or L on the board.
STS	Sustained Tri-State Output, Driven High for One CLK before Float.
Switch	Device that appears to software as two or more logical bridges.
TAP	Test Access Port.
TC	Traffic Class.
TLP	Translation Layer Packet.
TP	Totem Pole.
TS	Tri-State Bi-Directional.
Tx	Transmitter.
Upstream	Transactions that are forwarded from the secondary interface to the primary interface of a bridge are said to be *flowing upstream*.
UR	Unsupported request.
VC	Virtual Channel.

Data Book Notations and Conventions

Notation / Convention	Description
Blue text	Indicates that the text is hyperlinked to its description elsewhere in the data book. Left-click the blue text to learn more about the hyperlinked information. This format is often used for register names, register bit and field names, register offsets, chapter and section titles, figures, and tables.
XXXp0	The lowercase "p = positive" or "n = negative" suffix indicates the differential pair of signal, which are always used together.
# = Active-Low signals	Unless specified otherwise, Active-Low signals are identified by a "#" appended to the term (*for example*, PERST#).
Program/code samples	Monospace font (*program or code samples*) is used to identify code samples or programming references. These code samples are case-sensitive, unless specified otherwise.
command_done	Interrupt format.
Command/Status	Register names.
Parity Error Detected	Register parameter [field] or control function.
Upper Base Address[31:16]	Specific Function in 32-bit register bounded by bits [31:16].

Number multipliers	k = 1,000 (10^3) is generally used with frequency response.
	K = 1,024 (2^{10}) is used for memory size references.
	KB = 1,024 bytes.
	M = meg.
	    = 1,000,000 when referring to frequency (decimal notation)
	    = 1,048,576 when referring to memory sizes (binary notation)

1Fh	h = suffix which identifies hex values. Each prefix term is equivalent to a 4-bit binary value (nibble). Legal prefix terms are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
1010b	b = suffix which identifies binary notation (*for example*, 01b, 010b, 1010b, and so forth). Not used with single-digit values of 0 or 1.
0 through 9	Decimal numbers, or single binary numbers.
byte	Eight bits – abbreviated to "B" (*for example*, 4B = 4 bytes)
LSB	Least-Significant Byte.
lsb	Least-significant bit.
MSB	Most-Significant Byte.
msb	Most-significant bit.
DWord	DWord (32 bits) is the primary register size in the PEX 8311.
Reserved	Do not modify *reserved* bits and words. Unless specified otherwise, these bits read as 0 and must be written as 0.

Contents

Registers

PCI Express Configuration Registers

Local Configuration Space Registers

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Chapter 1   Introduction

1.1   Features

- Forward and Reverse bridging between the PCI Express interface and Local Bus
- Root Complex and Endpoint PCI Express mode support
- PCI Express single-lane (x1) port (one Virtual Channel)
- PCI Express 2.5 Gbps per direction
- PCI Express full Split Completion protocol
- Serial Peripheral Interface (SPI) Serial EEPROM port
- Internal 8-KB shared RAM available to the PCI Express interface and Local Bus
- General-purpose I/Os – Four GPIO balls, one GPI ball, and one GPO ball
- Low-power CMOS in 337-ball PBGA Package
- 1.5 and 2.5V core operating voltage, 3.3V I/O
- PCI Express Power Management
    - Link Power Management states
        - **Endpoint mode** – L0, L0s, L1, L2/L3 Ready, and L3
        - **Root Complex mode** – L0, L0s, L1, L2, L2/L3 Ready, and L3
    - Device Power Management states
        - **Endpoint mode** – D0 (D0_uninitialized, D0_active), D1, and D3 (D3hot, D3cold)
        - **Root Complex mode** – D0 (D0_uninitialized, D0_active), D1, D2, and D3 (D3hot, D3cold)
- Bus Mastering interface between a PCI Express port and 32-bit, 66-MHz processor Local Bus
    - *Hot-Plug r1.1*-compatible in Endpoint mode
    - Direct connection to three types of Local Bus processor interface
        - **C mode (non-multiplexed address/data)** – Intel i960, DSPs, custom ASICs and FPGAs, and others
        - **J mode (multiplexed address/data)** – Intel i960, IBM PowerPC 401, DSPs, FPGAs, and others
        - **M mode** – Motorola MPC850 and MPC860, and IBM PowerPC 801
    - Asynchronous clock input for Local Bus
    - Commercial Temperature Range operation with Industrial Temperature Range supported under specific conditions
    - IEEE 1149.1 JTAG boundary scan

- Three Data Transfer modes – *Direct Master*, *Direct Slave*, and *DMA*
    - **Direct Master** – A type of transfer that originates from a Master on the Local Bus and is addressed to a PCI Express device
        - Two Local Bus Address spaces to the PCI Express Space – one to PCI Express memory and one to PCI Express I/O
        - Generates PCI Express Memory and I/O transaction types, including Memory Write/Read, I/O Write/Read, and Type 0 and Type 1 configuration in Root Complex Mode
        - Read Ahead, Programmable Read Prefetch Counter(s) (C, J, and M modes)
        - MPC850 and MPC860 Delayed Read and IDMA support (M mode)
    - **Direct Slave** – A type of transfer that originates from a PCI Express device and is addressed to a 32-, 16-, or 8-bit Local Bus device
        - Two general-purpose Address spaces to the Local Bus and one Expansion ROM Address space
        - Delayed Write, Read Ahead, Posted Write, Programmable Read Prefetch Counter
        - Programmable Local Bus Ready timeout and recovery
    - **DMA** – PEX 8311 services data transfer descriptors, mastering on the PCI Express interface and Local Bus during transfer
        - Two independent channels
        - **DMA Block mode** – Single descriptor execution
        - **DMA Scatter/Gather mode** – Descriptors in PCI Express or Local Bus memory; Linear descriptor list execution; Dynamic descriptor DMA Ring Management mode with Valid bit semaphore control; Burst descriptor loading
        - Hardware EOT/Demand controls to stop/pause DMA in any mode
        - Programmable Local Bus burst lengths, including infinite burst
    - Six independent, programmable FIFOs – Direct Master Read and Write, Direct Slave Read and Write, DMA Channel 0 and Channel 1
    - Advanced features common to Direct Master, Direct Slave, and DMA
        - Zero wait state burst operation
        - 264-Megabytes-per-second bursts on the Local Bus
        - Deep FIFOs, which prolong maximum PCI Express package generation
        - Unaligned transfers on the PCI Express interface and Local Bus
        - On-the-fly Local Bus Endian conversion
        - Programmable Local Bus wait states
        - Parity checking on the PCI Express interface and Local Bus
- I_2O *r1.5*-Ready Messaging Unit
- Twelve 32-bit **Mailbox** (eight on the Local and four on the PCI Express end of the logic) and two 32-bit **Doorbell** registers enable general-purpose messaging
- Reset and interrupt signal directions configurable for Endpoint and Root Complex applications
- Programmable Interrupt Generator
- Microwire serial EEPROM interface – Stores user-specified power-on/reset Configuration register values
- Local Configuration Space **(LCS)** register-compatible with the PCI 9056, and PCI 9656

- Compliant with the following standards
    - PCI Local Bus Specification, Revision 3.0 (*PCI r3.0)*
    - PCI Local Bus Specification, Revision 2. 2 (*PCI r2.2*)
    - PCI to PCI Bridge Architecture Specification, Revision 1.1 (*PCI-to-PCI Bridge r1.1*)
    - PCI Bus Power Management Interface Specification, Revision 1.1 (*PCI Power Mgmt. r1.1*)
    - PCI Hot Plug Specification, Revision 1.1 (*PCI Hot Plug r1.1*)
    - PCI Standard Hot Plug Controller and Subsystem Specification, Revision 1.0
      (*PCI Standard Hot Plug r1.0*)
    - PCI Express Base Specification, Revision 1.0a (*PCI Express r1.0a*)
    - PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0 (*PCI Express-to-PCI/
      PCI-X Bridge r1.0*)
    - *PCI Express Card Electromechanical Specification, Revision 1.1 (PCI Express CEM 1.1)*
    - Intelligent I/O (I$_2$O) Architecture Specification, Revision 1.5 (*I$_2$O r1.5*)

Figure 1-1.   PEX 8311 Block Diagram
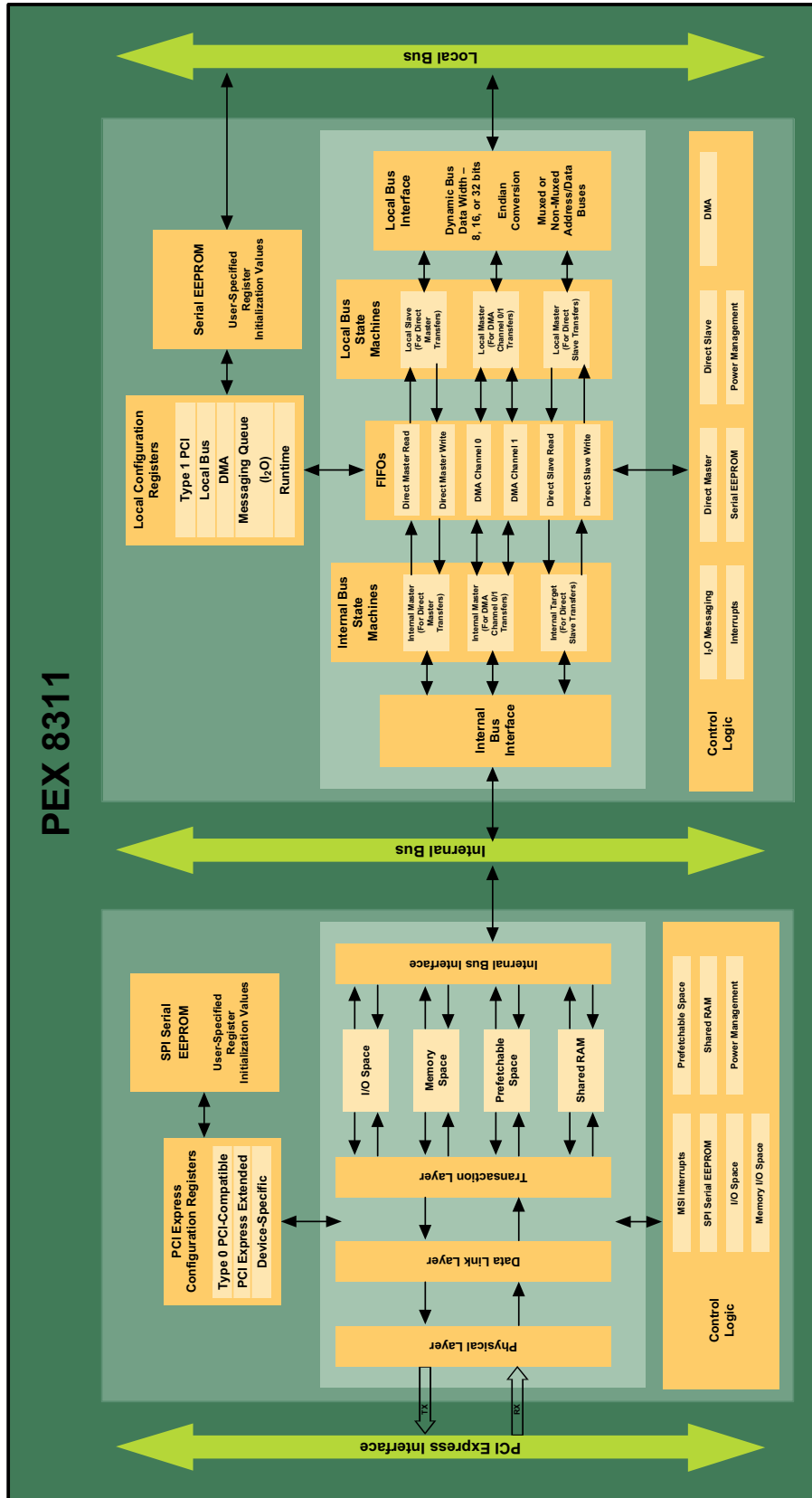
1.2   Overview

The PLX Technology ExpressLane™ PEX 8311 is a PCI Express-to-Generic Local Bus bridge. This device features PLX proprietary Data Pipe Architecture® technology. This technology consists of powerful, flexible engines for high-speed Data transfers, as well as intelligent Messaging Units for managing distributed I/O functions.

1.2.1   PCI Express Endpoint Interface

The PEX 8311 includes the following PCI Express Endpoint Interface features:

- Full 2.5 Gbps per direction
- Single lane and Single virtual channel operation
- Compatible with multi-lane and multi-virtual channel PCI Express devices
- Packetized serial traffic with PCI Express Split Completion protocol
- Data Link Layer CRC generator and checker
- Automatic Retry of bad packets
- Integrated low-voltage differential drivers
- 8b/10b signal encoding
- In-band interrupts and messages
- Message Signaled Interrupt (MSI) support

1.2.2   High-Speed Data Transfers

Data Pipe Architecture technology provides independent Direct Transfer and DMA methods for moving data. Data Pipe Architecture technology Data transfer supports the following:

- PCI Express-to-Local Bus Burst transfers at the maximum bus rates (Direct Slave)
- PCI Express Memory-Mapped Single access to internal Configuration registers
- PCI Express Type 0 Single access to **LCS** registers
- PCI Express Memory-Mapped Single/Burst access to internal shared RAM
- PCI Express Configuration access to **PECS** registers (Endpoint mode only)
- Local Bus access to PCI Express (Direct Master)
- Local Bus Single access to LCS Configuration registers
- Local Bus Configuration access to **PECS** Configuration registers (Root Complex mode only)
- Local Bus Memory-Mapped Single/Burst access to internal shared RAM
- Unaligned transfers on Local Bus
- On-the-fly Local Bus Endian conversion
- Programmable Local Bus wait states
- Parity checking on PCI Express interface and Local Bus

Figure 1-2.   High-Speed Data Transfers
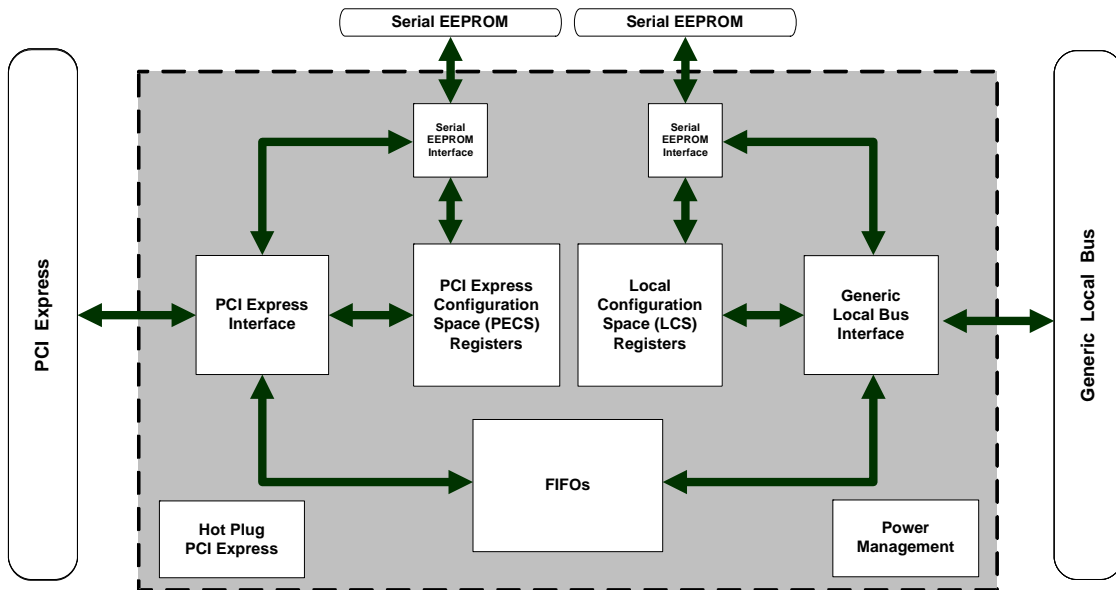
1.2.2.1   Direct Transfers

Data Pipe Architecture technology Direct Transfers are used by a Transfer Initiator on the PCI Express or Local Bus interface to move data through the PEX 8311 to a device on the other bus. The Transfer Initiator takes responsibility for moving the data into the PEX 8311 on a Write, or out of the PEX 8311 on a Read. The PEX 8311 is responsible for moving the data out to the target device on a write, or in from the target device on a read.

1.2.2.1.1   Direct Master

When a Device on the PEX 8311 Local Bus initiates a Read or Write to an address mapped as PCI Express Memory or I/O space, the PEX 8311 initiates a Read or Write transaction in PCI Express space. In other words "Local Bus addresses PCI Express." This type of transfer is termed a *Direct Master transfer.* The PEX 8311 becomes a traffic generator on the PCI Express interface. Data Pipe Architecture technology provides independent FIFOs for Direct Master Read and Write transfers. It also supports mapping of one or more independent Direct Master Local Bus Address spaces to PCI Express addresses, as illustrated in Figure 1-3.

Direct Master transfers support generation of PCI Express Memory and I/O transaction types, including Type 0 and Type 1 cycles for system configuration in Root Complex mode only.

Figure 1-3.   Direct Master Address Mapping
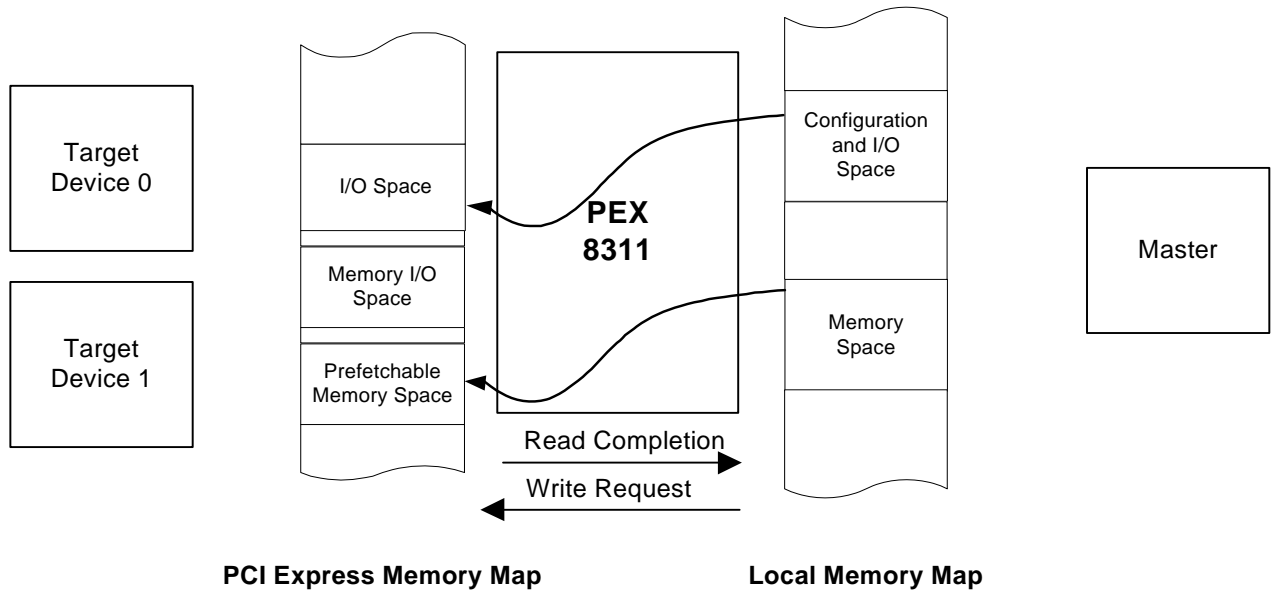
1.2.2.1.2   Direct Slave

When a device in PCI Express Space initiates a Read or Write to a Memory or I/O address mapped as PEX 8311 Local Space, that Read or Write request is executed on the PEX 8311 Local Bus. In other words, "PCI Express addresses Local Bus." This type of transfer is termed a *Direct Slave transfer.* The PEX 8311 is a slave (technically, a target) on the PCI Express Link. Data Pipe Architecture technology provides independent FIFOs for Direct Slave Read and Write transfers. It also supports mapping of one or more independent Direct Slave PCI Express Address spaces to Local Bus addresses, as illustrated in Figure 1-4.

With software, Direct Slave transfers support Local Bus Data transfers of various widths (*for example*, on a 32-bit Local Bus, data widths of 8, 16, and 32 bits are supported).

Figure 1-4.   Direct Slave Address Mapping

PCI Express Memory Map   **Local Memory Map**
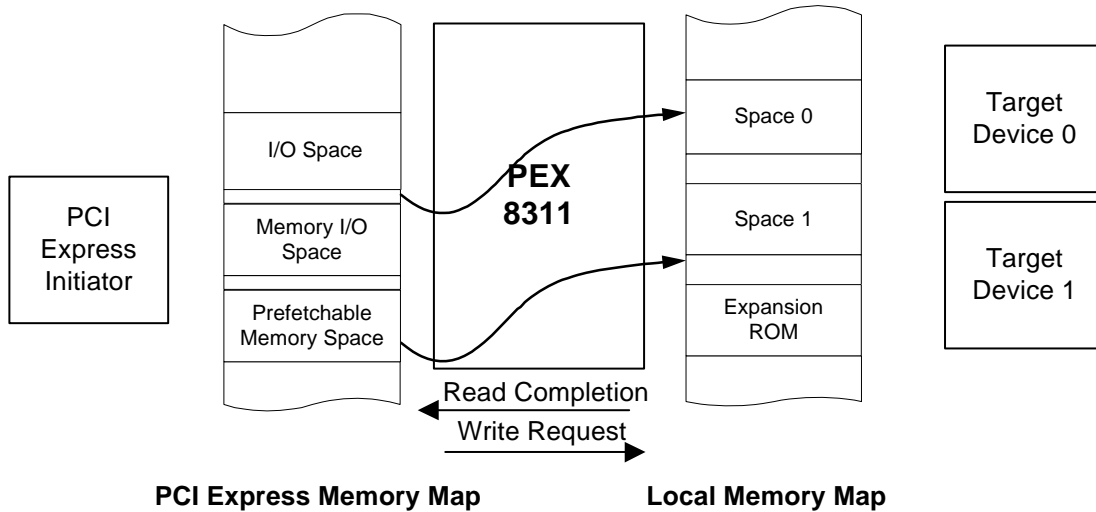
1.2.2.2 DMA

When a device initiates data traffic on either bus utilizing Data Pipe Architecture technology DMA transfers, instead of the Master moving data, it places a description of the entire transfer in the PEX 8311 registers and allows the PEX 8311 to perform the entire Data transfer with its DMA engine. This offers two main benefits:

- Data movement responsibilities are off-loaded from the Master. A transfer descriptor is short and takes little effort on the part of the Master to load. After the descriptor is loaded into the PEX 8311, the Master is free to spend its time and resources elsewhere.

- Because the PEX 8311 supports multiple DMA channels, each with its own FIFO, it can simultaneously service multiple PCI Express and processor Local Bus Masters. During DMA transfers, the PEX 8311 masters each bus. Consequently, during DMA transfers, there are no external masters to Retry. During DMA transfers, when the PEX 8311 is Retried or Data Transfer is preempted on either bus, it can simply change context to another transfer and continue. Furthermore, DMA transfers can simultaneously run with Direct Master and Direct Slave transfers, providing support for several simultaneous Data transfers. Direct Master and Direct Slave transfers retain higher priority than DMA.

Data Pipe Architecture technology supports two DMA transfer modes – *Block* and *Scatter/Gather*.

1.2.2.2.1 DMA Block Mode

DMA Block mode is the simplest DMA mode. A Local Bus Master or PCI Express device programs the description of a single transfer in the PEX 8311 and sets the *DMA Channel Start* bit for the affected DMA channel (**LCS_DMACSR0/1**[1]=1). The PEX 8311 indicates DMA completion to the Master, by setting the *DMA Channel Done* bit for the affected DMA channel in one of the registers polled by the Master (**LCS_DMACSR0/1**[4]) or by generating an interrupt.

1.2.2.2.2 DMA Scatter/Gather Mode

In most cases, however, one descriptor is not sufficient. A Local Bus Master or PCI Express device typically generates a list of several descriptors in its memory before submitting them to the PEX 8311. In these cases, DMA Scatter/Gather mode is used to enable the PEX 8311 list processing with minimal Master intervention.

With DMA Scatter/Gather mode, the Local Bus Master or PCI Express device tells the PEX 8311 the location of the first descriptor in its list, sets the *DMA Channel Start* bit for the affected DMA channel (**LCS_DMACSR0/1**[1]=1), then waits for the PEX 8311 to service the entire list. This offloads both data and DMA descriptor transfer responsibilities from the Master.

Data Pipe Architecture technology supports DMA Scatter/Gather mode descriptor lists in PCI Express, 8-KB shared, or Local Bus memory. It also supports linear and circular descriptor lists, the latter being termed *DMA Ring Management mode*.

DMA Ring Management mode uses a *Valid* bit in each descriptor to enable dynamic list management. In this case, the Local Bus Master or PCI Express device and the PEX 8311 continuously "walk" the descriptor list, the Master in the lead filling invalid descriptors, setting the *Ring Management Valid* bit for the affected DMA channel when done (**LCS_DMASIZ0/1**[31]=1), and the PEX 8311 following behind servicing valid descriptors, resetting the Valid bit when done. The PEX 8311 supports write back to serviced descriptors, allowing status and actual Terminal Count to post prior to resetting the *Valid* bit for the affected DMA channel.

1.2.2.2.3   Hardware DMA Controls – EOT and Demand Mode

To optimize DMA transfers in datacom/telecom and other applications, Data Pipe Architecture technology supports hardware controls of the Data transfer.

With End of Transfer (EOT), an EOT# signal is asserted to the PEX 8311 to end the transfer. When EOT# is asserted, the PEX 8311 immediately terminates the current DMA transfer and writes back to the current DMA descriptor the actual number of bytes transferred. Data Pipe Architecture technology also supports unlimited bursting. EOT and unlimited bursting are especially useful in applications *such as* Ethernet adapter boards, wherein the lengths of read packets are not known until the packets are read.

In DMA Demand mode, a hardware DREQ*x*#/DACK*x*# signal pair is used to pause and resume the DMA transfer. Data Pipe Architecture technology provides one DREQ*x*#/DACK*x*# signal pair for each DMA channel. Demand mode provides a means for a peripheral device with its own FIFO to control DMA transfers. The peripheral device uses Demand mode both to pause the transfer when the FIFO is full on a write or empty on a read and to resume the transfer when the FIFO condition changes to allow the Data transfer to continue. Demand mode can also be used for many non-FIFO-based applications.

1.2.3   Intelligent Messaging Unit

Data Pipe Architecture technology provides two methods for managing system I/O through messaging.

The first method is provided through general-purpose **Mailbox** and **Doorbell** registers. When all PCI Express-based components are under direct control of the system designer (*for example*, an embedded system, *such as* a set-top box), it is often desirable to implement an application-specific Messaging Unit through the general-purpose **Mailbox** and **Doorbell** registers.

The second method is provided through Intelligent I/O (I$_2$O) support. As the device-independent, industry-standard method for I/O control, I$_2$O is the easiest way to obtain interoperability of all PCI-based components in the system.

1.2.4   Register Compatibility with PCI 9x56 I/O Accelerators

The PEX 8311 *PCI Express r1.0a*-compliant device extends the PLX family of PCI 9xxx series devices, to provide an easy migration path for existing Generic Local Bus-to-PCI designs to the new PCI Express interface.

The PCI Express Configuration Space (**PECS**) register set is backward-compatible with the PEX 8111 PCI Express-to-PCI Bus Bridge. The Local Configuration Space (**LCS**) register set is backward-compatible with the previous generation PCI 9056 and PCI 9656 I/O Accelerators.

The PEX 8311 incorporates the industry-leading PLX Data Pipe Architecture technology, including programmable Direct Master and Direct Slave transfer modes, intelligent DMA engines, and PCI messaging functions.

1.2.5   Applications

The PEX 8311 continues the PLX tradition of extending its product capabilities to meet the leading edge requirements of I/O intensive embedded-processor applications. The PEX 8311 builds upon the industry-leading PCI 9056, and PCI 9656 products, providing an easy upgrade path to PCI Express interface and Local Bus operation. The PEX 8311 supports all Conventional PCI processors and designs, using the C, J, or M Local Bus interfaces. Additionally, the PEX 8311 offers several important new features that expand its applicability and performance.

1.2.5.1   High-Performance PCI Express Endpoint Boards

The PEX 8311 is designed for traditional PCI Express Endpoint board applications to provide an easy migration of existing Conventional PCI designs, based on the PCI 9056 and PCI 9656 Local Bus-to-PCI I/O Accelerators, to PCI Express. Specific applications include high-performance communications, networking, disk control, and data encryption adapters.

Today, Power Management and Green PCs are major initiatives in Conventional PCI applications. The PEX 8311 supports Active and Device State Power Management.

Figure 1-5 illustrates the PEX 8311 in a PCI Express Endpoint board application with a CPU, with C, J, or M Local Bus modes.

The C and J Local Bus modes, in addition to supporting Intel i960 processors, are being adopted by designers of a wide variety of devices, ranging from DSPs to custom ASICs, because of their high speed, low overhead, and relative simplicity.

For applications using I/O types not supported directly by the processor, *such as* SCSI for storage applications, the PEX 8311 provides a high-speed interface between the processor and PCI Express-based I/O devices. Furthermore, the Local Bus interface supports processors that do not include integrated I/O.

Figure 1-5.   PEX 8311 PCI Express Adapter Board with C, J, or M Mode Processor
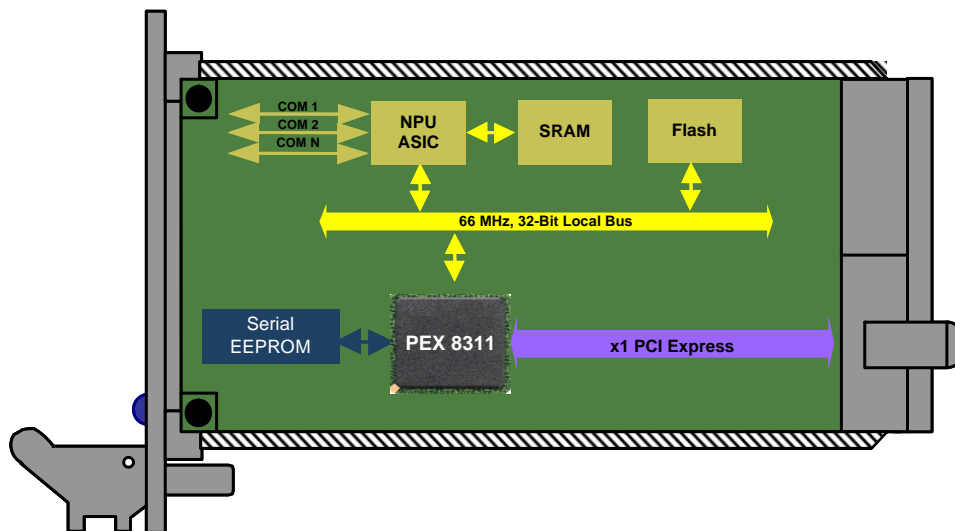
1.2.5.2   High-Performance Embedded Root Complex Designs

I/O intensive embedded Root Complex designs are another major PEX 8311 application, which include network switches and routers, printer engines, and set-top boxes, CompactPCI system boards, and industrial equipment.

While the support requirements of these embedded Root Complex designs share many similarities with Endpoint board designs, *such as* their requirement for intelligent management of Local Bus I/O, PCI Express Board Electromechanical guidelines, there are three significant differences.

First, the Root Complex is responsible for configuring the PCI Express System hierarchy. The PEX 8311 supports PCI Express Type 0 and Type 1 Configuration cycles to accomplish this.

Second, the Root Complex is responsible for accepting Message Signaled Interrupt (MSI) messages from PCI Express downstream devices, as well as providing Root Complex-specific Configuration Registers to control the overall system. The PEX 8311 provides MSI acceptance that is routed to the Local Bus as a Local Bus Interrupt or Local System Error signal.

Third, for Root Complex, the directions of the reset signal reverse. The PEX 8311 includes a strapping option for reversing the directions of the PCI Express and Local Bus reset signals. In one setting, the direction is appropriate for an Endpoint; in the other setting, it is appropriate for a Root Complex.

Figure 1-6 illustrates the PEX 8311 in an embedded Root Complex system.

Figure 1-6.   PEX 8311 in Embedded Root Complex System
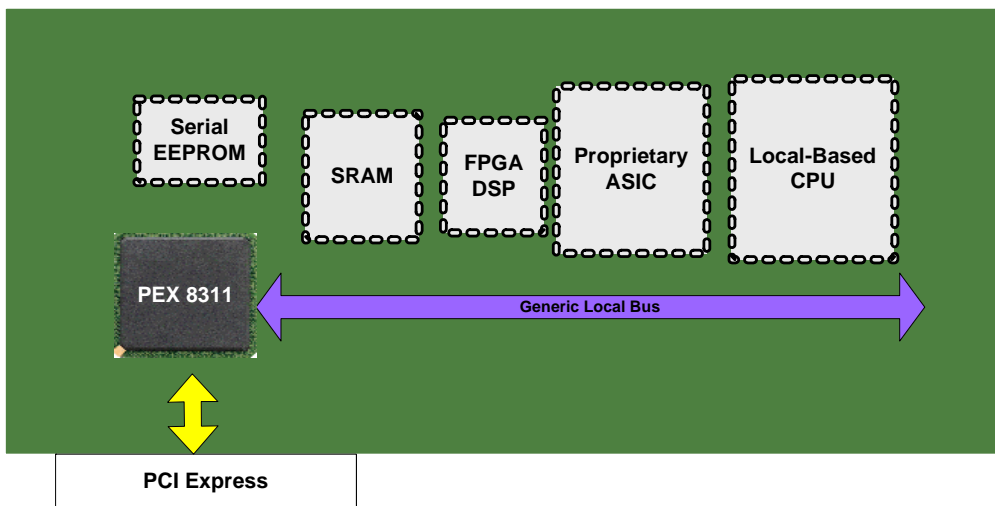
1.2.5.3　High-Performance Motorola MPC850 and MPC860 PowerQUICC Designs – M Mode Only

A key application for the PEX 8311 is Motorola MPC850- or MPC860-based adapters for telecom and networking applications. These applications include high-performance communications, such as WAN/LAN controller cards, high-speed modem cards, Frame Relay cards, routers, and switches.

The PEX 8311 simplifies these designs by providing an industry-leading enhanced direct-connect interface to the MPC850 or MPC860 processor. The flexible PEX 8311 3.3V, 5V tolerant I/O buffers, combined with Local Bus operation up to 66 MHz, are ideally suited for current and future PowerQUICC processors.

The PEX 8311 supports the MPC850 and MPC860 IDMA channels for movement of data between the integrated MPC850 or MPC860 communication channels and the PCI Bus.

In addition, the PEX 8311 makes use of the advanced Data Pipe Architecture technology, allowing unlimited burst capability, as shown in Figure 1-7.

Regarding items 1 and 2 in Figure 1-7:

1. For PowerQUICC IDMA operation, the PEX 8311 transfers data to the PCI Express Bus under the control of the IDMA handshake protocol using Direct Master transfers (1).

2. Simultaneously, the PEX 8311 DMA can be operated bi-directionally, with the PEX 8311 as the Master for both buses, to manage transfers of data between the PCI Express and Local Buses (2).

This is a prime example of how the PEX 8311 provides superior general-purpose bus master performance and provides designers using the PowerQUICC processor with greater flexibility in implementing multiple simultaneous I/O transfers. The PEX 8311 has unlimited bursting capability, which enhances most MPC850 or MPC860 PowerQUICC designs.

Figure 1-7.　High-Performance MPC850 or MPC860 PowerQUICC Adapter Design
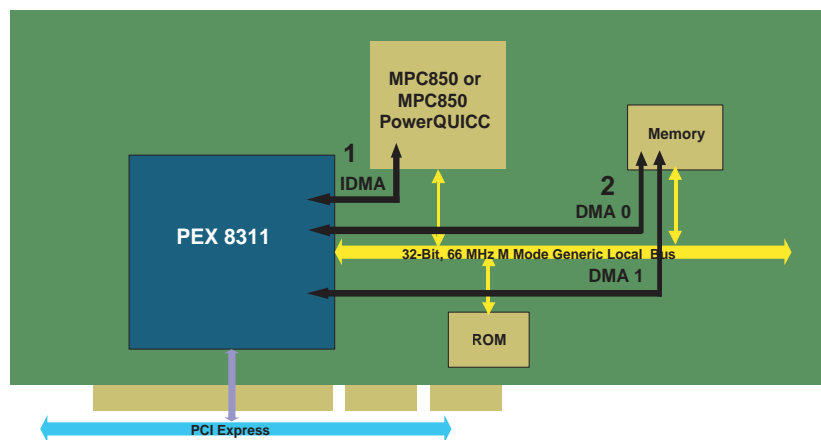
1.2.6   Data Transfer

The PEX 8311 allows for Local Burst Transfers up to 264 Mbps and six Programmable FIFOs for Zero Wait State Burst operation. Table 1-1 defines FIFO depth.

Table 1-1.   FIFO Depth

FIFO	Depth
Direct Master Write	64 Dwords
Direct Master Read	32 Dwords
Direct Slave Write	64 Dwords
Direct Slave Read	32 Dwords
DMA Channel 0	64 Dwords
DMA Channel 1	64 Dwords

The PEX 8311 includes the following additional data transfer features:

- **Unaligned Transfer Support** – Allows transferring data on any byte-boundary combination of the Local Address spaces. Only the last and first data of the PCI Express packet can be unaligned.

- **Big/Little Endian Conversion** – Supports dynamic switching between Big Endian (Address Invariance) and Little Endian (Data Invariance) operations for Direct Master, Direct Slave, DMA, and internal Register accesses on the Local Bus.

- **On-the-Fly Endian Conversion of Local Bus Data Transfers** – Supports on-the-fly Endian conversion of Local Bus Data transfers. The Local Bus can be applied as Big/Little Endian by using the BIGEND# input ball or programmable internal register configuration. When BIGEND# is asserted, it overrides the internal register configuration during Direct Master transfers, and internal Register accesses on the Local Bus.

- **C and J Mode Data Transfers** – Provided to communicate with i960, PPC401, DSPs, ASICs, and FPGA processors, using three possible Data Transfer modes:
  - Direct Master Operation
  - Direct Slave Operation
  - DMA Operation

- **M Mode Data Transfers.** Communicates with the MPC850 or MPC860, using three possible Data Transfer modes:
  - Direct Master Operation, including support for MPC850 and MPC860 IDMA/SDMA Operation
  - Direct Slave Operation
  - DMA Operation

- **Three PCI Express-to-Local Address Spaces** – The PEX 8311 supports three PCI Express-to-Local Address spaces in Direct Slave mode – *Space 0*, *Space 1*, and *Expansion ROM*. These spaces allow any PCI Express upstream device to access the Local Bus Memory spaces with programmable wait states, bus data width, burst capabilities, and so forth.

- **Direct Master and Direct Slave Read Ahead Mode** – Allows prefetched data to be read from the internal Read FIFO instead of the external bus. The address must be subsequent to the previous address and Dword-aligned. This feature allows for increased bandwidth utilization through reduced data latency.
    - **PCI Express Read Ahead for Direct Master Reads** – The DM Read FIFO works in conjunction with Read Ahead capability in the PCI Express interface, to greatly reduce completion time for follow-on sequential Reads from the host. For example, when the Local CPU reads one DWord mapped as PCI Express Space, up to 4 KB of sequential data can be requested in anticipation of a sequential Read from the Local Master.
    - **Local Bus Read Ahead for Direct Slave Reads** – The PEX 8311 includes programmable control to prefetch data during Direct Slave and Direct Master prefetches (known or unknown size). To perform Burst reads, prefetching must be enabled. The prefetch size can be programmed to match the Master burst length, or can be used as Direct Master or Direct Slave Read Ahead mode data. Reads single data (8, 16, or 32 bit) when the Master initiates a single cycle; otherwise, the PEX 8311 prefetches the programmed size.
- **Posted Memory Writes** – Supports Posted Memory Writes for maximum performance and to avoid potential deadlock situations.
- **64-bit PCI Express Addresses** – Supports generation of 64-bit PCI Express Address TLPs beyond the low 4-GB Address Boundary space. The 64-bit PCI Express Address TLPs can be used during PEX 8311 upstream traffic generation (Direct Master and DMA).

1.2.7   Messaging Unit

The PEX 8311 includes the following Messaging Unit features:

- **I$_2$O-Ready Messaging Unit** – Incorporates the I$_2$O-Ready Messaging Unit, which enables the adapter or embedded system to communicate with other I$_2$O-supported devices. The I$_2$O Messaging Unit is fully compatible with the *I$_2$O r1.5* PCI Extension.
- **Mailbox Registers** – Includes twelve 32-bit **Mailbox** registers that can be accessed from the PCI Express interface or Local Bus. Only the eight Mailboxes on the Local Bus can be used for the I$_2$O Messaging Unit.
- **Doorbell Registers** – Includes two 32-bit **Doorbell** registers. One register asserts interrupts from the PCI Express interface to the Local Bus. The other generates Message interrupts from the Local Bus to the PCI Express interface.

1.2.8   Root Complex Features

The PEX 8311 includes the following Root Complex features:

- **Type 0 and Type 1 Configuration** – In Direct Master mode, supports Type 0 and Type 1 PCI Express Configuration TLP generation.
- **Reset Signal Direction** – Includes a strapping option (ROOT_COMPLEX#) to reverse the direction of the PCI Express interface and Local Bus Reset signals. When the ROOT_COMPLEX# ball is strapped Low, the LRESET# signal becomes an input, and the PERST# signal becomes an output.

1.2.9   Electrical/Mechanical

The PEX 8311 includes the following electrical/mechanical features:

- **Packaging** – Available in a 337-ball, 21 x 21 mm^2 PBGA package.

- **1.5V and 2.5V Core, 3.3V I/O** – Low-power CMOS 1.5V and 2.5V core with 3.3V I/O. Typically consumes less than 500 mW total, when operating full-speed at room temperature.

- **5V Tolerant Operation** – Provides 3.3V signaling with 5V I/O tolerance on Local Bus.

- **Commercial Temperature Range Operation** – The PEX 8311 works in a 0 to +70°C temperature range.

    – However the PEX 8311 supports the Industrial Temperature Range of -40 ºC to +85 ºC. With the maximum power supply provided and in a worst case I/O switching scenario, the PEX 8311's maximum power dissipation is at 1.31W. It is highly recommended that the maximum power dissipation does not exceed 1.31W to ensure proper operation, which is guaranteed to work in the Industrial Temperature range with 0 m/s airflow.

Note: Junction-to-Ambient Package Thermal Resistance – Thetaj-a = 23.28 °C/W, at 0 m/s Linear Air Flow.

- **JTAG** – Supports *IEEE 1149.1* JTAG boundary-scan.

1.2.10   Miscellaneous

Other features provided in the PEX 8311 are as follows:

Serial EEPROM Interface – Includes two optional serial EEPROM interfaces, Microwire and SPI, used to load configuration information for Local Bus and PCI Express Configuration Registers, respectively. This is useful for loading information unique to a particular adapter, *such as* the Device or Vendor ID, especially in designs that do not include a Local processor.

Interrupt Generator – Can assert Local and generate PCI Express interrupts from external and internal sources.

1.3   Compatibility with Other PLX Devices

1.3.1   Ball Compatibility

The PEX 8311 is *not* ball compatible with other PLX Bus Master Accelerators, Target I/O Accelerators, PCI Express Bridges, nor Switches.

1.3.2   Register Compatibility

All registers implemented in the PCI 9056 and PCI 9656 are implemented in the PEX 8311.

The PEX 8311 is *not* register-compatible with the following PLX Target I/O Accelerators – PCI 9030, PCI 9050, nor PCI 9052.

The PEX 8311 includes many new bit definitions and several new registers. (Refer to Chapter 19, "PCI Express Configuration Registers.")

- All internal registers are accessible from the PCI Express interface or Local Bus
- Most internal registers can be set up through an external serial EEPROM
    – **PECS** register set includes all PEX 8111 registers
    – **LCS** register set includes all PCI 9056-device registers
- Internal registers allow Writes to and Reads from an external serial EEPROM
- Internal registers allow control of the GPIO, GPI, and GPO balls

Chapter 2   Ball Descriptions

2.1   Introduction

This chapter provides descriptions of the PEX 8311 signal balls. The signals are divided into the following groups:

- PCI Express Signals
  - PCI Express Interface Signals
  - PCI Express Configuration Space Serial EEPROM Support Signals
- Local Bus Signals
  - Local Bus Interface C Mode Signals (Non-Multiplexed)
  - Local Bus Interface J Mode Signals (Multiplexed)
  - Local Bus Interface M Mode Signals (Non-Multiplexed)
  - Local Configuration Space Serial EEPROM Interface Signals
- Miscellaneous Signals
- JTAG Interface Signals
- Test Signals
- No Connect Signals
- Power and Ground Signals

2.2   Ball Description Abbreviations

Table 2-1.   Ball Description Abbreviations

Abbreviation	Description
#	Active Low
DIFF	PCI Express Differential buffer
DTS	Driven Tri-State, driven High for one-half CLK before float
I	Input
I/O	Bi-Directional
O	Output
OD	Open Drain Output
PD	100KΩ Pull-Down resistor
PU	100KΩ Pull-Up resistor (unless noted as another value)
S	Schmitt Trigger
STS	Sustained Tri-State, driven inactive one Clock cycle before float
TP	Totem Pole
TS	Tri-State

2.3   PCI Express Signals

This section provides descriptions of the PEX 8311 PCI Express signal balls. The signals are divided into the following two groups:

- PCI Express Interface Signals
- PCI Express Configuration Space Serial EEPROM Support Signals

2.3.1   PCI Express Interface Signals

Table 2-2.   PCI Express Interface Signals (9 Balls)

Signal	Type	Balls	Description
PCI Express Differential Signal Pairs (6 Balls)			
PERn0	I DIFF	F2	**Receive Minus** PCI Express Differential Receive signal
PERp0	I DIFF	G1	**Receive Plus** PCI Express Differential Receive signal
PETn0	O DIFF	K2	**Transmit Minus** PCI Express Differential Transmit signal. Series 100nF AC coupling capacitor required on each transmit line.
PETp0	O DIFF	J1	**Transmit Plus** PCI Express Differential Transmit signal. Series 100nF AC coupling capacitor required on each transmit line
REFCLK-	I DIFF	H2	**PCI Express Clock Input Minus** PCI Express differential, 100-MHz Spread Spectrum Reference Clock. In Endpoint mode, connected to the PCI Express REFCLK- signal. In Root Complex mode, connected to an external differential clock source.
REFCLK+	I DIFF	H1	**PCI Express Clock Input Plus** PCI Express differential, 100-MHz Spread Spectrum Reference Clock. In Endpoint mode, connected to the PCI Express REFCLK+ signal. In Root Complex mode, connected to an external differential clock source.
Single-Ended Signals (3.3V) (3 Balls)			
PERST#	I/O 6 mA 3.3V	C3	**PCI Express Reset** In Endpoint mode, PERST# is an input. It resets the entire bridge when asserted. In Root Complex mode, PERST# is an output. It is asserted when a PCI reset is detected.
WAKEIN#	I 3.3V	B2	**Wake In Signal** In Root Complex mode, WAKEIN# is an input, and indicates that the PCI Express device requested a wakeup while the Link is in the L2 state.
WAKEOUT#	OD 6 mA 3.3V	D1	**Wake Out Signal** In Endpoint mode, WAKEOUT# is an output, and asserted when the Link is in the L2 state.

2.3.1.1   PCI Express Layout and Design Rules

All PCI Express transmitters are AC-coupled. Use 0.075 to 0.2 μF, 0603 to 0402 size (preferred) footprints. For add-in boards, place AC capacitors within 250 mil from the board edge gold fingers. For system boards, place AC capacitors within 400 mil from connector pins.

PCB traces (with PCB dielectric material FR4) typically introduce as much as 0.25 to 0.35 dB of loss, and 1 ps (or more) of jitter per 2.54 cm (1 inch) per pair. Vias can introduce as much as 0.25 dB of loss [approximately equivalent to 2.54-cm (1-inch) trace]. Pad size for vias is 25 mil or less, with a finished hole size of 14 mil or less.

Remove signal via pads that have unused internal layers. The *PCI Express CEM 1.1* requires that the add-in board length match the Transmitted, Received, and Reference Clock pairs within 5 mil. *For example*, if PETp0 = 10.16 cm (4.000 inches) from connector to ball, PETn0 should be a length of between 10.148 to 10.173 cm (3.995 to 4.005 inches).

2.3.2   PCI Express Configuration Space Serial EEPROM Support Signals

Table 2-3.   PCI Express Configuration Space Serial EEPROM Support Signals (4 Balls)

Signal	Type	Balls	Description
EECLK	O TP 3 mA 3.3V	L4	**Serial EEPROM Clock** Provides the serial bit clock to the serial EEPROM. Connects directly to the serial EEPROM's Serial Clock input (SCK) pin. EECLK frequency is programmable by the **PECS_EECLKFREQ** register, and varies from 2 to 25 MHz.
EECS#	O TP 3 mA 3.3V	K3	**Serial EEPROM Chip Select** Active-Low serial EEPROM Chip Select. Connects directly to the serial EEPROM's CS# input pin.
EERDDATA	I 3.3V	M3	**Serial EEPROM Read Data** Inputs Serial Read data from the serial EEPROM. Connect to the serial EEPROM's Serial Data Out (SO) pin, and pull to 3.3V through a 10KΩ or lower resistor.
EEWRDATA	O TP 3 mA 3.3V	L3	**Serial EEPROM Write Data** Outputs Serial data to be written to the serial EEPROM. Connects directly to the serial EEPROM Serial Data Input (SI) pin.

2.4   Local Bus Signals

This section provides descriptions of the PEX 8311 Local Bus-specific signal balls, which includes their pull-up and pull-down resistor requirements. The signals are divided into the following groups:

- Local Bus Interface
    - Local Bus Interface C Mode Signals (Non-Multiplexed)
    - Local Bus Interface J Mode Signals (Multiplexed)
    - Local Bus Interface M Mode Signals (Non-Multiplexed)
- Local Configuration Space Serial EEPROM Interface Signals

Note: *Certain balls change type when in Reset/BDSEL mode. This is indicated in the **Type** column for the associated balls. Balls with a type that makes no mention of Reset/BDSEL mode maintain only the one type, which is indicated in the **Type** column entry for that ball, regardless of the silicon mode. For balls that include a Reset/BDSEL mode type, the other specified type is used in all other silicon modes.*

Reset/BDSEL mode is defined as:

- *ROOT_COMPLEX# is de-asserted and PERST# is asserted (PCI Express Reset input in Endpoint mode), or*
- *ROOT_COMPLEX# is asserted and LRESET# is asserted (Local Bus Reset input in Root Complex mode), or*
- *BD_SEL# is de-asserted (Bridge is in Test mode, all Local I/Os are tri-stated)*

2.4.1 Local Bus Signal Pull-Up and Pull-Down Resistor Requirements

The balls defined in Table 2-4 have an internal 100KΩ pull-up resistor to VDD3.3. Due to the weak value of these internal pull-up resistors, it is strongly recommended that external pull-up resistors to 3.3V or pull-down resistors (3KΩ to 10KΩ) be used on those signal balls when implementing them in a design. However, depending upon the application, certain signal balls defined in Table 2-4 can remain unconnected, driven or tied High or Low. External pull-up or pull-down resistors on the Address and/or Data Buses are recommended, but not required.

Table 2-4. Balls with Internal Resistors (to VDD3.3)

Local Bus Mode			Ball	Comment
C	J	M		
Balls with Internal 100KΩ Pull-Up Resistors				
✓	✓		ADS#	
✓	✓	✓	BAR0ENB#	
		✓	BDIP#	
		✓	BI#	
✓	✓		BIGEND#	
		✓	BIGEND#/WAIT#	
✓	✓		BLAST#	
✓	✓		BTERM#	
		✓	BURST#	
✓	✓	✓	CCS#	
✓	✓	✓	DACK[1:0]#	
	✓		DEN#	
✓	✓		DMPAF/EOT#	
		✓	DP[0:3]	
✓	✓		DP[3:0]	
✓	✓	✓	DREQ[1:0]#	
	✓		DT/R#	
✓	✓	✓	EEDI/EEDO	Although the EEDI/EEDO ball has an internal pull-up resistor, it can become necessary to add an external pull-up or pull-down resistor. (Refer to Section 4.3.1, "PEX 8311 Initialization from Serial EEPROM," for further details.)

Table 2-4.   Balls with Internal Resistors (to VDD3.3) (Cont.)

Local Bus Mode			Ball	Comment
C	J	M		
Balls with Internal 100KΩ Pull-Up Resistors				
		✓	LA[0:1, 3:31]	
✓	✓		LA[28:2]	
✓			LA[31:30]	
	✓		LAD[31:0]	
✓	✓		LBE[3:0]#	
		✓	LD[0:31]	
✓			LD[31:0]	
✓	✓	✓	LINTi#	
✓	✓	✓	LINTo#	
✓	✓	✓	LRESET#	
✓	✓		LSERR#	
✓	✓		LW/R#	
		✓	MDREQ#/DMPAF/EOT#	
		✓	RD/WR#	
✓	✓		READY#	
✓	✓	✓	ROOT_COMPLEX#	
		✓	TA#	
		✓	TEA#	
		✓	TS#	
		✓	TSIZ[0:1]	
✓	✓		WAIT#	
Balls with Internal 10KΩ Pull-Up Resistors				
✓	✓	✓	PMEIN#	If PMEIN# is not used, this ball can remain unconnected.
Balls with Internal 100KΩ Pull-Down Resistors				
✓	✓	✓	IDDQEN#	Pull IDDQEN# to 3.3V through a resistor of 1KΩ or less.

The balls defined in Table 2-5 do not have internal resistors. Because the Open Drain (OD) balls (*for example*, BREQo) are created using I/O buffers, they must be pulled-up to ensure their input buffer is at a known state, which are tri-stated when not driven (STS). Recommended resistor pull-up value is 4.7Ω to 10KΩ.

Table 2-5.   Pull-Up/Pull-Down Resistor Recommendations for Balls with No Internal Resistors

Local Bus Mode			Ball	Recommendation
C	J	M		
	✓		ALE	Requires an external pull-down resistor.
✓	✓	✓	BAR0ENB#	Requires an external pull-up or pull-down for standard operation. Functionality dependent.
		✓	BB#	Requires an external pull-up resistor (recommend 4.7KΩ or less).
✓	✓	✓	BD_SEL#	Must be tied to ground during standard operation.
		✓	BG#	Input that should be pulled High, or driven High or Low.
		✓	BR#	Output that is always driven by the PEX 8311. Therefore, an external pull-up or pull-down resistor is *not* required.
✓	✓		BREQi	Pulled, tied, or driven Low.
✓	✓		BREQo	Requires an external pull-down resistor.
✓	✓	✓	CLKIN	Does *not* require an external pull-up nor pull-down resistor.
✓	✓	✓	EECS	Outputs that are always driven by the PEX 8311 and can be connected or remain unconnected (floating).
✓	✓	✓	EESK	Outputs that are always driven by the PEX 8311 and can be connected or remain unconnected (floating).
✓	✓	✓	ITDO	Requires an external pull-up resistor.
		✓	LA2	Requires an external pull-up resistor.
✓			LA29	Requires an external pull-up resistor to 3.3V (recommend 10KΩ),
✓	✓	✓	LCLK	Does *not* require an external pull-up nor pull-down resistor.
✓	✓		LHOLD	Output ball, floats during Reset or BD_SEL# assertion; therefore, an external pull-up or pull-down resistor is *not* required.
✓	✓		LHOLDA	Input ball, pull Low or drive High or Low.
		✓	MODE[0:1]	Tie High or Low.
✓	✓		MODE[1:0]	Tie High or Low.
✓	✓	✓	PLXT1	Requires an external pull-up resistor.
✓	✓	✓	PLXT2	Requires an external pull-down resistor.
✓	✓	✓	PMEOUT#	Power Management Event in Root Complex mode. Requires an external pull-up resistor.
		✓	RETRY#	Requires an external pull-up resistor.
✓	✓	✓	ROOT_COMPLEX#	**Endpoint mode** – Due to a weak pull-up value, requires an external pull-up resistor. **Root Complex mode** – Requires an external pull-down resistor.

Table 2-5.   Pull-Up/Pull-Down Resistor Recommendations for Balls with No Internal Resistors (Cont.)

Local Bus Mode			Ball	Recommendation
C	J	M		
✓	✓	✓	TCK, TDI, TDO. TMS, TRST#	For designs that do not implement JTAG: • Ground the TRST# ball • Drive, pull, or tie the TCK, TDI, and TMS inputs to a known value *IEEE Standard 1149.1-1990* requires pull-up resistors on the TDI, TMS, and TRST# balls. To remain *PCI r2.2*-compliant, no internal pull-up resistors are provided on JTAG balls; therefore, the pull-up resistors must be externally added to the PEX 8311 when implementing JTAG.
✓	✓	✓	USERi/LLOCKi#	Use a pull-up resistor. (Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior.")
✓	✓	✓	USERo/LLOCKo#	External pull-up or pull-down resistor is *not* required.

2.4.2　　　Local Bus Interface C Mode Signals (Non-Multiplexed)

Table 2-6.　Local Bus Interface C Mode Signals (96 Balls)

Signal	Type	Balls	Description
ADS#	I/O TS 24 mA PU	F19	**Address Strobe** Indicates the valid address and start of a new Bus access. ADS# is asserted for the first clock of the Bus access.
BIGEND#	I PU	D18	**Big Endian Select** Can be asserted during the Local Bus Address phase of a Direct Master transfer or Configuration register access to specify use of Big Endian Byte ordering. Uses an AL_BTT24_U buffer (which includes a pull-up resistor). *Note:　Big Endian Byte ordering can also be programmed through the **LCS_BIGEND** register.*
BLAST#	I/O TS 24 mA PU	F20	**Burst Last** As an input, the Local Bus Master asserts BLAST# to indicate the last Data transfer of a Bus access. As an output, the PEX 8311 asserts BLAST# to indicate the last Data transfer of the Bus access.
BREQi	I	G18	**Bus Request In** Asserted to indicate a Local Bus Master requires the bus. When enabled through the Configuration registers, the PEX 8311 releases the bus during a Direct Slave or DMA transfer when BREQi is asserted.
BREQo	O DTS 24 mA	G17	**Bus Request Out** When the Backoff Timer expires, the PEX 8311 asserts BREQo until it is granted the Local Bus.
BTERM#	I/O DTS 24 mA PU	J19	**Burst Terminate** As an input, BTERM# assertion causes the PEX 8311 (as the Local Master) to break the transfer (typically a burst). When the transfer is not completed, the PEX 8311 generates a new Address cycle and continues the transfer. As an output, the PEX 8311 (as a Local Target) only asserts BTERM# to request the Master to break the transfer when a PCI Express Abort condition is detected.
CCS#	I PU	D17	**Configuration Register Select** PEX 8311 **LCS** registers are selected when CCS# is asserted Low during Local Bus accesses to the PEX 8311.

Table 2-6.   Local Bus Interface C Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
DACK[1:0]#	O TP 24 mA PU When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], balls go Hi-Z.	B18, C20	**DMA Channel *x* Demand Mode Acknowledge (2 Balls)** When DMA Channel *x* is programmed through the **LCS DMA** registers to operate in Demand mode, this output indicates a DMA transfer is in progress. DACK0# is associated with Channel 0. DACK1# is associated with Channel 1.
DMPAF EOT#	When **LCS_DMAMODE0/1**[14]=1 I PU otherwise O TP 24 mA PU When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.	C18	Multiplexed I/O ball. Default functionality is DMPAF output (**LCS_DMAMODE0/1**[14]=0). **Direct Master Programmable Almost Full** DMPAF (Output): Direct Master Write FIFO Almost Full status output. Programmable through **LCS_DMPBAM**[10, 8:5]. **End of Transfer for Current DMA Channel** EOT# (Input): Terminates the current DMA transfer. EOT# serves as a general-purpose EOT. Therefore, be aware of DMA channel activity before asserting EOT#.
DP[3:0]	I/O TS 24 mA PU	M15, M16, L15, L16	**Data Parity** Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for writes to or reads by the PEX 8311. Parity is asserted for reads from or writes by the PEX 8311.
DREQ[1:0]#	I PU	B17, C19	**DMA Channel *x* Demand Mode Request (2 Balls)** When DMA Channel 0 is programmed through the Configuration registers to operate in Demand mode, this input serves as a DMA request. DREQ0# is associated with Channel 0. DREQ1# is associated with Channel 1.

Table 2-6.   Local Bus Interface C Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
LA[31:2]	I/O TS 24 mA PU (LA[31:30, 28:2] only)	Y7, W8, Y8, W9, Y9, W10, Y10, V11, W11, Y11, W12, Y12, W13, Y13, W14, Y14, V15, W15, Y15, U16, V16, W16, Y16, U17, V17, W17, Y17, V18, W18, Y18	**Local Address Bus (30 Balls)** Carries the upper 30 bits of the physical Address Bus. Incremented during bursts to indicate successive Data cycles.
LBE[3:0]#	I/O TS 24 mA PU	Y19, Y20, W20, W19	**Local Byte Enables (4 Balls)** Encoded, based on the bus data-width configuration, as follows: **32-Bit Bus** The four Byte Enables indicate which of the four bytes are valid during a Data cycle: LBE3# Byte Enable 3 – LD[31:24] LBE2# Byte Enable 2 – LD[23:16] LBE1# Byte Enable 1 – LD[15:8] LBE0# Byte Enable 0 – LD[7:0] **16-Bit Bus** LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: LBE3# Byte High Enable (BHE#) – LD[15:8] LBE2# *not used* LBE1# Address bit 1 (LA1) LBE0# Byte Low Enable (BLE#) – LD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA[1:0], respectively: LBE3# *not used* LBE2# *not used* LBE1# Address bit 1 (LA1) LBE0# Address bit 0 (LA0)
LCLK	I	J20	**Local Processor Clock** Local Bus clock input. *Note: LCLK must be driven at all times during standard operation.*
LD[31:0]	I/O TS 24 mA PU	V19, V20, U19, U20, T17, T18, T19, T20, R17, R18, R19, R20, P17, P18, P19, P20, N17, N18, N19, N20, M17, M18, M19, M20, L17, L18, L19, L20, K17, K18, K19, K20	**Local Data Bus (32 Balls)** When the PEX 8311 is the Local Bus Master, it carries 8-, 16-, or 32-bit data quantities, depending upon bus data-width configuration. Direct Master accesses to the PEX 8311 are 32 bits only.

Table 2-6.   Local Bus Interface C Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
LHOLD	O TP 24 mA When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.	G20	**Local Hold Request** Asserted to request use of the Local Bus.
LHOLDA	I	G19	**Local Hold Acknowledge** The external Local Bus Arbiter asserts LHOLDA when bus ownership is granted in response to LHOLD. Do not grant the Local Bus to the PEX 8311, unless requested by LHOLD.
LINTi#	I PU	E20	**Local Interrupt Input** When enabled by the **LCS Interrupt Control/Status** register (**LCS_INTCSR**[11, 8] = 11b), PCI Express Assert_INTA and Deassert_INTA messages are transmitted to PCI Express Space following LINTi# signal assertions (High-Low) and de-assertions (Low-High), respectively.
LINTo#	O OD 24 mA PU	E19	**Local Interrupt Output** Synchronous output that remains asserted when the interrupt is enabled [by way of the **LCS Interrupt Control/Status** register (**LCS_INTCSR**)] and the interrupt condition exists.
LRESET#	When ROOT_COMPLEX# is asserted I PU otherwise O TP 24 mA PU	E18	**Local Bus Reset** As an input, in Root Complex mode, PERST# is generated as long as LRESET# is asserted. Resets the PEX 8311. As an output, in Endpoint mode, LRESET# is asserted when the PEX 8311 is in reset (PERST#=0). Can be used to reset the backend logic on the board. When ROOT_COMPLEX# is Low (asserted), LRESET# is an input. When asserted, all internal logic and registers are forced to their initial states, and PERST# is asserted to PCI Express Space. When ROOT_COMPLEX# is High (de-asserted), LRESET# is an output that is asserted in response all PCI Express resets, Soft resets, and Local Bus device resets. (Refer to Chapter 3, "Reset Operation and Initialization Summary," for further details.)
LSERR#	O OD 24 mA PU	J18	**Local System Error Interrupt Output** Synchronous output that remains asserted when the interrupt is enabled (by way of the **LCS_INTCSR** register) and the interrupt condition exists.

Table 2-6. Local Bus Interface C Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
LW/R#	I/O TS 24 mA PU	U18	**Local Write/Read** Asserted Low for Reads and High for Writes.
PMEIN#	I PU (10K)	C16	**Power Management Event Input** **(Endpoint Mode Only)** When the PEX 8311 is operating in Endpoint mode (ROOT_COMPLEX# is de-asserted), asserting PMEIN# Low generates a PM_PME message to PCI Express Space. (Refer to Section 14.3, "Endpoint Mode Local Bus Power Management," for details.) PMEIN# has an internal 10KΩ pull-up resistor to VDD3.3.
PMEOUT#	OD 24 mA	B10	**Power Management Event Out** Valid only in Root Complex mode (ROOT_COMPLEX# is asserted). Open Drain output used to signal to a Local Host that a PM_PME message was received from a device in PCI Express Space. PMEOUT# is *not* 5V tolerant. (Refer to Section 14.4.3, "Root Complex PMEOUT# Signal," for details.)
READY#	I/O DTS 24 mA PU	F18	**Ready I/O** Direct Slave or DMA accesses: A Local Slave asserts READY# to indicate that Read data on the bus is valid or when Write data is to be sampled on the next rising edge of LCLK. READY# input is not sampled until the internal Wait State Counter(s) expires (WAIT# output is de-asserted). Direct Master accesses from external Local Master: READY# is an output, driven Low when Read data on the bus is valid or when write data is to be sampled on the next rising edge of LCLK.
USERi LLOCKi#	I	D20	Multiplexed input ball. Default functionality is USERi (**LCS_CNTRL**[18]=1). **User Input** USERi: General-purpose input that can be read in the PEX 8311 Configuration registers. Also used to select the PEX 8311 behavior in response to PCI Express accesses during initialization. (Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior.") **Local Lock Input** LLOCKi#: Used only when multiple processors have access to the same PCI resource. Indicates an atomic operation that can require multiple transactions to complete. Used by the PEX 8311 for direct Local access to the PCI Express bridge. Must be tied High.

Table 2-6.   Local Bus Interface C Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
USERo LLOCKo#	O TP 24 mA When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.	D19	Multiplexed output ball. Default functionality is USERo (**LCS_CNTRL**[19]=1). **User Output** USERo: General-purpose output controlled from the PEX 8311 Configuration registers. Driven Low during software reset. [Refer to Section 3.1.2.2, "Local Bus Bridge Local Bus Reset," (Endpoint mode) or Section 3.2.1, "Local Bus Reset," (Root Complex mode) for details.] **Local Lock Output** LLOCKo#: Indicates an atomic operation for a Direct Slave PCI Express-to-Local Bus access can require multiple transactions to complete.
WAIT#	I/O TS 24 mA PU	H17	**Wait I/O** As an input, the Local Bus Master can assert WAIT# to pause the PEX 8311 (insert wait states) during a Direct Master access Data phase. As an output, the PEX 8311 can be programmed to insert wait states (to pause the Local Slave) by asserting WAIT# for a pre-defined number of Local Bus Clock cycles during Direct Slave transfers.

2.4.3   Local Bus Interface J Mode Signals (Multiplexed)

Table 2-7.   Local Bus Interface J Mode Signals (96 Balls)

Signal	Type	Balls	Description
ADS#	I/O TS 24 mA PU	F19	**Address Strobe** Indicates a valid address and start of a new Bus access. ADS# is asserted for the first clock of the Bus access.
ALE	I/O TS 24 mA	Y8	**Address Latch Enable** Indicates the valid address and start of a new Bus access. ALE is asserted for the first clock of the Bus access. As an input, the PEX 8311 latches the incoming address on the positive edge of LCLK, following ALE assertion. Verify that the ALE pulse is similar to the example provided in Figure 23-3, "PEX 8311 ALE Output Delay to Local Clock." As an output, refer to Figure 23-3.
BIGEND#	I PU	D18	**Big Endian Select** Can be asserted during the Local Bus Address phase of a Direct Master transfer or Configuration register access to specify use of Big Endian Byte ordering. Uses an AL_BTT24_U buffer (which includes a pull-up resistor). *Note: Big Endian Byte ordering can also be programmed through the **LCS_BIGEND** register.*
BLAST#	I/O TS 24 mA PU	F20	**Burst Last** As an input, the Local Bus Master asserts BLAST# to indicate the last Data transfer of a Bus access. As an output, the PEX 8311 asserts BLAST# to indicate the last Data transfer of the Bus access.
BREQi	I	G18	**Bus Request In** Asserted to indicate a Local Bus Master requires the bus. When enabled through the Configuration registers, the PEX 8311 releases the bus during a Direct Slave or DMA transfer when BREQi is asserted.
BREQo	O DTS 24 mA	G17	**Bus Request Out** When the Backoff Timer expires, the PEX 8311 asserts BREQo until it is granted the Local Bus.
BTERM#	I/O DTS 24 mA PU	J19	**Burst Terminate** As an input, BTERM# assertion causes the PEX 8311 (as the Local Master) to break the transfer (typically a burst). When the transfer is not completed, the PEX 8311 generates a new Address cycle and continues the transfer. As an output, the PEX 8311 (as a Local Target) only asserts BTERM# to request the Master to break the transfer when a PCI Abort condition is detected.

Table 2-7.   Local Bus Interface J Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
CCS#	I PU	D17	**Configuration Register Select** When asserted Low, CCS# Reads or Writes by external Local Masters are directed to the PEX 8311 **LCS** registers.
DACK[1:0]#	O TP 24 mA PU When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], balls go Hi-Z.	B18, C20	**DMA Channel *x* Demand Mode Acknowledge (2 Balls)** When DMA Channel *x* is programmed through the Configuration registers to operate in Demand mode, this output indicates a DMA transfer is in progress. DACK0# is associated with Channel 0. DACK1# is associated with Channel 1.
DEN#	O TS 24 mA PU	W8	**Data Enable** When asserted Low, the Local Bus device can drive the Local Data Bus. Used in conjunction with DT/R# to provide control for data transceivers attached to the Local Bus.
DMPAF EOT#	When **LCS_DMAMODE0/1** [14]=1 I PU otherwise O TP 24 mA PU When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.	C18	Multiplexed I/O ball. Default functionality is DMPAF output (**LCS_DMAMODE0/1**[14]=0). **Direct Master Programmable Almost Full** DMPAF (Output): Direct Master Write FIFO Almost Full status output. Programmable through **LCS_DMPBAM**[10, 8:5]. **End of Transfer for Current DMA Channel** EOT# (Input): Terminates the current DMA transfer. EOT# serves as a general-purpose EOT. Therefore, be aware of DMA channel activity before asserting EOT#.
DP[3:0]	I/O TS 24 mA PU	M15, M16, L15, L16	**Data Parity (4 Balls)** Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for Writes to or on Reads by the PEX 8311. Parity is asserted for Reads from or Writes by the PEX 8311.

Table 2-7.   Local Bus Interface J Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
DREQ[1:0]#	I PU	B17, C19	**DMA Channel *x* Demand Mode Request (2 Balls)** When DMA Channel 0 is programmed through the Configuration registers to operate in Demand mode, this input serves as a DMA request. DREQ0# is associated with Channel 0. DREQ1# is associated with Channel 1.
DT/R#	O TS 24 mA PU	Y7	**Data Transmit/Receive** When asserted High, indicates the PEX 8311 is driving data onto the Local Data Bus. Used in conjunction with DEN#, to provide control for data transceivers attached to the Local Bus. When asserted Low, indicates that the PEX 8311 receives data. Refer also to Timing Diagram 6-53 and Timing Diagram 6-54.
LA[28:2]	I/O TS 24 mA PU	W9, Y9, W10, Y10, V11, W11, Y11, W12, Y12, W13, Y13, W14, Y14, V15, W15, Y15, U16, V16, W16, Y16, U17, V17, W17, Y17, V18, W18, Y18	**Local Address Bus (27 Balls)** Provides the current Dword address (except the upper three bits [31:29]) during any phase of an access. Incremented on successive Data cycles during Burst cycles. LBE[1:0]# can be encoded to provide LA[1:0].
LAD[31:0]	I/O TS 24 mA PU	V19, V20, U19, U20, T17, T18, T19, T20, R17, R18, R19, R20, P17, P18, P19, P20, N17, N18, N19, N20, M17, M18, M19, M20, L17, L18, L19, L20, K17, K18, K19, K20	**Local Address/Data Bus (32 Balls)** During an Address phase: As a Local Bus Master, the PEX 8311 provides a 32-bit address for 8-bit data quantities, and LAD[31:0] provide byte addressing. For 16-bit data quantities, LAD[31:1] provide word addressing and LAD[0] is driven to 0. For 32-bit data quantities, LAD[31:2] provide Dword addressing and LAD[1:0] are driven to 00b. As a Local Bus Slave, Master accesses to the PEX 8311 can only be 32-bit quantities (LAD[1:0] are ignored). The input address is latched into the PEX 8311, on the positive edge of LCLK during ADS# assertion or following ALE assertion. During a Data phase: As a Local Bus Master, the PEX 8311 provides an 8-bit data quantity on LAD byte lanes, 16-bit data quantities on LAD word lanes, and 32-bit data quantities on LAD[31:0], depending on the bus data-width access. As a Local Bus Slave, 32-bit Data Bus for reading from or writing to the PEX 8311.

Table 2-7.   Local Bus Interface J Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
LBE[3:0]#	I/O TS 24 mA PU	Y19, Y20, W20, W19	**Local Byte Enable (4 Balls)** Encoded, based on the bus data-width configuration, as follows: **32-Bit Bus** The four Byte Enables indicate which of the four bytes are valid during a Data cycle: LBE3# Byte Enable 3 – LAD[31:24] LBE2# Byte Enable 2 – LAD[23:16] LBE1# Byte Enable 1 – LAD[15:8] LBE0# Byte Enable 0 – LAD[7:0] **16-Bit Bus** LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: LBE3# Byte High Enable (BHE#) – LAD[15:8] LBE2# *not used* LBE1# Address bit 1 (LA1) LBE0# Byte Low Enable (BLE#) – LAD[7:0] **8-Bit Bus** LBE[1:0]# are encoded to provide LA[1:0], respectively: LBE3# *not used* LBE2# *not used* LBE1# Address bit 1 (LA1) LBE0# Address bit 0 (LA0)
LCLK	I	J20	**Local Processor Clock** Local Bus clock input. *Note: LCLK must be driven at all times during standard operation.*
LHOLD	O TP 24 mA When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.	G20	**Local Hold Request** Asserted to request use of the Local Bus.
LHOLDA	I	G19	**Local Hold Acknowledge** The external Local Bus Arbiter asserts LHOLDA when bus ownership is granted in response to LHOLD. Do not grant the Local Bus to the PEX 8311, unless requested by LHOLD.

Table 2-7.   Local Bus Interface J Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
LINTi#	I PU	E20	**Local Interrupt Input (Endpoint Mode Only)** In Endpoint Mode only (ROOT_COMPLEX# is de-asserted), when enabled by way of the **LCS Interrupt Control/Status** register (**LCS_INTCSR**[11,8] = 11b), High-Low and Low-High transitions on LINTi# cause Assert_INTA and Deassert_INTA messages to be sent to PCI Express Space.
LINTo#	O OD 24 mA PU	E19	**Local Interrupt Output** Synchronous output that remains asserted when the interrupt is enabled [by way of the **LCS Interrupt Control/Status** register (**LCS_INTCSR**)] and the interrupt condition exists.
LRESET#	When ROOT_COMPLEX# is asserted I PU otherwise O TP 24 mA PU	E18	**Local Bus Reset** As an input, in Root Complex mode, PERST# is generated when LRESET# is asserted. Resets the PEX 8311. As an output, in Endpoint mode, LRESET# is asserted when the PEX 8311 is in reset (PERST#=0). Can be used to reset the backend logic on the board.
LSERR#	O OD 24 mA PU	J18	**Local System Error Interrupt Output** Synchronous output that remains asserted when the interrupt is enabled (by way of the **LCS_INTCSR** register) and the interrupt condition exists.
LW/R#	I/O TS 24 mA PU	U18	**Local Write/Read** Asserted Low for Reads and High for Writes.
PMEIN#	I PU (10K)	C16	**Power Management Event Input (Endpoint Mode Only)** When the PEX 8311 is operating in Endpoint mode (ROOT_COMPLEX# is de-asserted), asserting PMEIN# Low generates a PM_PME message to PCI Express Space. (Refer to Section 14.3, "Endpoint Mode Local Bus Power Management," for details.) PMEIN# has an internal 10KΩ pull-up resistor to VDD3.3.
PMEOUT#	OD 24 mA	B10	**Power Management Event Out** Valid only in Root Complex mode (ROOT_COMPLEX# is asserted). Open Drain output used to request a change in the power state. PMEOUT# is *not* 5V tolerant.

Table 2-7.   Local Bus Interface J Mode Signals (96 Balls) (Cont.)

Signal	Type	Balls	Description
READY#	I/O DTS 24 mA PU	F18	**Ready I/O** Direct Slave or DMA accesses: A Local Slave asserts READY# to indicate that Read data on the bus is valid or that Write data will be sampled on the next rising edge of LCLK. READY# input is not sampled until the internal Wait State Counter(s) expires (WAIT# output is de-asserted). Direct Master accesses from external Local Master: READY# is an output, driven Low when Read data is valid or when Write data is to be sampled on the next LCLK rising edge.
USERi LLOCKi#	I	D20	Multiplexed input ball. Default functionality is USERi (**LCS_CNTRL**[18]=1). **User Input** USERi: General-purpose input that can be read in the PEX 8311 Configuration registers. Also used to select the PEX 8311 behavior in response to PCI Express accesses during initialization. (Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior.") **Local Lock Input** LLOCKi#: Indicates an atomic operation that can require multiple transactions to complete. Used by the PEX 8311 for direct Local access to the internal PCI Bus.
USERo LLOCKo#	O TP 24 mA When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.	D19	Multiplexed output ball. Default functionality is USERo (**LCS_CNTRL**[19]=1). **User Output** USERo: General-purpose output controlled from the PEX 8311 Configuration registers. Driven Low during software reset. [Refer to Section 3.1.2.2, "Local Bus Bridge Local Bus Reset," (Endpoint mode) or Section 3.2.1, "Local Bus Reset," (Root Complex mode) for details.] **Local Lock Output** LLOCKo#: Indicates an atomic operation for a Direct Slave PCI Express-to-Local Bus access that can require multiple transactions to complete.
WAIT#	I/O TS 24 mA PU	H17	**Wait I/O** As an input, the Local Bus Master can assert WAIT# to pause the PEX 8311 (insert wait states) during a Direct Master access Data phase. As an output, the PEX 8311 can be programmed to insert wait states (to pause the Local Slave) by asserting WAIT# for a pre-defined number of Local Bus Clock cycles during Direct Slave transfers.

2.4.4   Local Bus Interface M Mode Signals (Non-Multiplexed)

Table 2-8.   Local Bus Interface M Mode Signals (96 Balls)

Signal	Type	Balls	Description
BB#	I/O DTS 24 mA	G18	**Bus Busy** As an input, the PEX 8311 monitors BB# to determine whether an external Master has ended a Bus cycle. As an output, the PEX 8311 asserts BB# after an external Local Bus Arbiter has granted ownership of the Local Bus and BB# is detected de-asserted. It is recommended that an external pull-up resistor value of 4.7KΩ be applied to guarantee a fast transition to the inactive state when the PEX 8311 relinquishes Local Bus ownership.
BDIP#	I/O TS 24 mA PU	H17	**Burst Data in Progress** As an input, driven by the Bus Master during a Burst transaction. The Master de-asserts before the last Data phase on the bus. As an output, driven by the PEX 8311 during the Data phase of a Burst transaction. The PEX 8311 de-asserts before the last Burst Data phase on the bus.
BG#	I	G19	**Bus Grant** The external Local Bus Arbiter asserts BG# in response to BR#. Indicates that the requesting Master is next.
BI#	I PU	J19	**Burst Inhibit** When asserted, indicates that the Target device does not support Burst transactions.
BIGEND# WAIT#	When (**LCS_MARBR**[31]=0) I else I/O TS 24 mA PU	D18	Multiplexed I/O ball. Default functionality is BIGEND#, Big Endian input (**LCS_MARBR**[31])=0). **Big Endian** BIGEND# (Input): Can be asserted during the Local Bus Address phase of a Direct Master transfer or Configuration register access to specify use of Big Endian Byte ordering. *Note: Big Endian Byte ordering can also be programmed through the **LCS_BIGEND** register.* **WAIT I/O** WAIT# (I/O): As an input, the Local Bus Master may assert WAIT# to pause the PEX 8311 (insert wait states) during a Direct Master access Data phase. As an output, the PEX 8311 may be programmed to insert wait states (to pause the Local Slave) by asserting WAIT# for a pre-defined number of Local Bus clock cycles during Direct Slave transfers.

Table 2-8.   Local Bus Interface M Mode Signals (96 Balls)(Cont.)

Signal	Type	Balls	Description
BR#	O TP 24 mA When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], balls go Hi-Z.	G20	**Bus Request** The PEX 8311 asserts BR# to request use of the Local Bus. The external Local Bus Arbiter asserts BG# when the Master is next in line for bus ownership.
BURST#	I/O TS 24 mA PU	F20	**Burst** As an input, driven by the Master along with address and data, indicating that a Burst transfer is in progress. As an output, driven by the PEX 8311 along with address and data, indicating that a Burst transfer is in progress.
CCS#	I PU	D17	**Configuration Register Select** PEX 8311 **LCS** registers are selected when CCS# is asserted Low during Local Bus accesses to the PEX 8311.
DACK[1:0]#	O TP 24 mA PU When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], balls go Hi-Z.	B18, C20	**DMA Channel *x* Demand Mode Acknowledge (2 Balls)** When DMA Channel *x* is programmed through the **LCS DMA** registers to operate in Demand mode, this output indicates a DMA transfer is in progress. DACK0# is associated with Channel 0. DACK1# is associated with Channel 1.
DP[0:3]	I/O TS 24 mA PU	M15, M16, L15, L16	**Data Parity (4 Balls)** Parity is even for each of up to four byte lanes on the Local Bus. Parity is checked for Writes to or on Reads by the PEX 8311. Parity is asserted for Reads from or Writes by the PEX 8311.
DREQ[1:0]#	I PU	B17, C19	**DMA Channel *x* Demand Mode Request (2 Balls)** When DMA Channel 0 is programmed through the Configuration registers to operate in Demand mode, this input serves as a DMA request. DREQ0# is associated with Channel 0. DREQ1# is associated with Channel 1.

Table 2-8. Local Bus Interface M Mode Signals (96 Balls)(Cont.)

Signal	Type	Balls	Description
LA[0:31]	I/O TS 24 mA PU (LA[0:1, 3:31] only)	Y7, W8, Y8, W9, Y9, W10, Y10, V11, W11, Y11, W12, Y12, W13, Y13, W14, Y14, V15, W15, Y15, U16, V16, W16, Y16, U17, V17, W17, Y17, V18, W18, Y18, W20, W19	**Local Address Bus (32 Balls)** Carries the 32 bits of the physical Address Bus.
LCLK	I	J20	**Local Processor Clock** Local clock input. *Note: LCLK must be driven at all times during standard operation.*
LD[0:31]	I/O TS 24 mA PU	V19, V20, U19, U20, T17, T18, T19, T20, R17, R18, R19, R20, P17, P18, P19, P20, N17, N18, N19, N20, M17, M18, M19, M20, L17, L18, L19, L20, K17, K18, K19, K20	**Local Data Bus (32 Balls)** When the PEX 8311 is the Local Bus Master, it carries 8-, 16-, or 32-bit data quantities, depending upon bus data-width configuration. All Master accesses to the PEX 8311 are 32 bits only.
LINTi#	I PU	E20	**Local Interrupt Input** When enabled by the **LCS Interrupt Control/Status** register (**LCS_INTCSR**[11, 8] = 11b), PCI Express Assert_INTA and Deassert_INTA messages are transmitted to PCI Express Space following LINTi# signal assertions (High-Low) and de-assertions (Low-High), respectively.
LINTo#	O OD 24 mA PU	E19	**Local Interrupt Output** Synchronous output that remains asserted when the interrupt is enabled [by way of the **LCS Interrupt Control/Status** register (**LCS_INTCSR**)] and the interrupt condition exists.
LRESET#	When (ROOT_COMPLEX# is asserted) I PU else O TP 24 mA PU	E18	**Local Bus Reset** As an input, in Root Complex mode, PERST# is generated as long as LRESET# is asserted. Resets the PEX 8311. As an output, in Endpoint mode, LRESET# is asserted when the PEX 8311 is in reset (PERST#=0). Can be used to reset the backend logic on the board. When ROOT_COMPLEX# is Low (asserted), LRESET# is an input. When asserted, all internal logic and registers are forced to their initial states, and PERST# is asserted to PCI Express Space. When ROOT_COMPLEX# is High (de-asserted), LRESET# is an output that is asserted in response all PCI Express resets, Soft resets, and Local Bus device resets. (Refer to Chapter 3, "Reset Operation and Initialization Summary," for further details.)

Table 2-8.   Local Bus Interface M Mode Signals (96 Balls)(Cont.)

Signal	Type	Balls	Description
MDREQ# DMPAF EOT#	When (**LCS_DMAMODE0/1**[14]=1) I PU else O TP 24 mA PU When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.	C18	Multiplexed I/O ball. Default functionality is MDREQ#/ DMPAF output (**LCS_DMAMODE0/1**[14]=0). **IDMA Data Transfer Request** MDREQ# (Output): IDMA M mode Data transfer request start. When asserted, indicates that Data transfer should start. De-asserted only when the number of Direct Master FIFO entries exceed the value programmed in **LCS_DMPBAM**[10, 8:5]. **Direct Master Programmable Almost Full** DMPAF (Output): Direct Master Write FIFO Almost Full status output. Programmable through **LCS_DMPBAM**[10, 8:5]. **End of Transfer for Current DMA Channel** EOT# (Input): Terminates the current DMA transfer. EOT# serves as a general-purpose EOT. Therefore, be aware of DMA channel activity before asserting EOT#.
PMEIN#	I PU (10K)	C16	**Power Management Event Input (Endpoint Mode Only)** When the PEX 8311 is operating in Endpoint mode (ROOT_COMPLEX# is de-asserted), asserting PMEIN# Low generates a PM_PME message to PCI Express Space. (Refer to Section 14.3, "Endpoint Mode Local Bus Power Management," for details.) PMEIN# has an internal 10KΩ pull-up resistor to VDD3.3.
PMEOUT#	OD 24 mA	B10	**Power Management Event Out** Valid only in Root Complex mode (ROOT_COMPLEX# is asserted). Open Drain output used to signal to a Local Host that a PM_PME message was received from a device in PCI Express Space. PMEOUT# is *not* 5V tolerant. (Refer to Section 14.4.3, "Root Complex PMEOUT# Signal," for details.)
RD/WR#	I/O TS 24 mA PU	U18	**Read/Write** Asserted High for Reads and Low for Writes.
RETRY#	O DTS 24 mA	G17	**Retry** Driven by the PEX 8311 when it is a Slave, to indicate that the Local Master must release the bus.

Table 2-8. Local Bus Interface M Mode Signals (96 Balls)(Cont.)

Signal	Type	Balls	Description
TA#	I/O DTS 24 mA PU	F18	**Transfer Acknowledge** As an input, when the PEX 8311 is a Bus Master, indicates that a Write Data transfer is complete or that Read data on the bus is valid. As an output, when a Local Bus access is made to the PEX 8311, indicates that a Write Data transfer is complete or that Read data on the bus is valid.
TEA#	I/O OD 24 mA PU	J18	**Transfer Error Acknowledge** Driven by the Target device, indicating that an error condition occurred during a Bus cycle.
TS#	I/O TS 24 mA PU	F19	**Address Strobe** Local Master asserts TS# to start a Bus access.
TSIZ[0:1]	I/O TS 24 mA PU	Y19, Y20	**Transfer Size** Driven by the current Master along with the address, indicating the Data Transfer size. (Refer to Section 9.3.10.5, "Direct Slave Transfer Size – M Mode Only," for further details.)
USERi LLOCKi#	I	D20	Multiplexed input ball. Default functionality is USERi (**LCS_CNTRL**[18]=1). **User Input** USERi: General-purpose input that can be read in the PEX 8311 Configuration registers. Also used to select the PEX 8311 behavior in response to PCI Express accesses during initialization. (Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior.") **Local Lock Input** LLOCKi#: Indicates an atomic operation that can require multiple transactions to complete. Used by the PEX 8311 for direct Local access to the internal PCI Bus.
USERo LLOCKo#	O TP 24 mA When [(ROOT_COMPLEX# is not asserted and PERST# is asserted) or (ROOT_COMPLEX# and LRESET# are asserted) or BD_SEL# is not asserted)], ball goes Hi-Z.	D19	Multiplexed output ball. Default functionality is USERo (**LCS_CNTRL**[19]=1). **User Output** USERo: General-purpose output controlled from the PEX 8311 Configuration registers. Driven Low during software reset. [Refer to Section 3.1.2.2, "Local Bus Bridge Local Bus Reset," (Endpoint mode) or Section 3.2.1, "Local Bus Reset," (Root Complex mode) for details.] **Local Lock Output** LLOCKo#: Indicates an atomic operation for a Direct Slave PCI Express-to-Local Bus access that can require multiple transactions to complete.

2.4.5   Local Configuration Space Serial EEPROM Interface Signals

Table 2-9.   Local Configuration Space Serial EEPROM Interface Signals (3 Balls)

Signal	Type	Balls	Description
EECS	O TP 12 mA When BD_SEL# is not asserted, ball goes Hi-Z.	A20	**Serial EEPROM Chip Select**
EEDI/EEDO	I/O TS 12 mA PU When **LCS_CNTRL**[31]=1, ball goes Hi-Z.	B20	**Serial EEPROM Data In/Serial EEPROM Data Out** Multiplexed Write and Read data to the serial EEPROM.
EESK	O TP 12 mA When BD_SEL# is not asserted, ball goes Hi-Z.	A19	**Serial EEPROM Clock** Serial bit clock for the serial EEPROM.

2.5   Miscellaneous Signals

Table 2-10.   Miscellaneous Signals (11 Balls)

Signal	Type	Balls	Description
BAR0ENB#	I 3.3V PU	E1	**PCI Express Base Address 0 Register Enable** When Low, the **PECS_PCIBASE0** register is enabled. When High, the **PECS_PCIBASE0** register is disabled, unless enabled by the **PECS_DEVSPECCTL** register *PCI Express Base Address 0 Enable* bit.
GPIO[3:0]	I/O 12 mA 3.3V PU	A1, D3, B1, C1	**General-Purpose I/O (4 Balls)** Program as an Input or Output general-purpose ball. Internal device status is also an output on GPIO[3:0]. Interrupts are generated on balls that are programmed as inputs. The **PECS_GPIOCTL** register is used to configure these I/O. GPIO0 defaults to a Link Status output. GPIO1 defaults to an input. When GPIO2 is Low at the trailing edge of RESET#, the **PECS_TLPCFG0** register *Limit Completion Flow Control Credit* bit is set. When GPIO3 is Low at the trailing edge of RESET#, the **PECS_TLPCFG0** register *Delay Link Training* bit is set.

MODE[1:0]	I	H20, H19	**Local Bus Mode (2 Balls)**
			MODE0 selects the PEX 8311 Local Bus operation mode:
			MODE0 MODE1 Local Bus Mode
			  0 0 C
			  0 1 *Reserved*
			  1 0 J
			  1 1 *Reserved*
			The MODE input level must be stable at power-on.
			Connect MODE1 to ground for standard operation

CLKIN	I 3.3V	A15	**Internal Clock Input** A 66-MHz clock input to the internal PEX 8311 interface. CLKIN can be directly connected as a source to CLKOUT through an external damping resistor (0Ω recommended value) when the ROOT_COMPLEX# signal is de-asserted (Endpoint mode). Avoid connecting CLKOUT directly to CLKIN, use a 0 ohms resistor to create a test point. An external 66-MHz clock source (oscillator) is required when the ROOT_COMPLEX# signal is asserted (Root Complex mode). Use internal clock requirement guidelines. When an external source is used, follow the *PCI r2.2* guidelines.
CLKOUT	O TP 26 mA 33Ω Series-Terminated	A8	**Internal Clock Output** A buffered clock output derived from REFCLK. Frequency is programmable, depending on the **PECS_DEVINIT** register CLKOUT Frequency field value. DEfault signal frequency is 66 MHz at 1:2 duty cycle (1/3 High, 2/3 Low). CLKOUT has an internal 33 Ohm series terminator.
PWR_OK	O 6 mA 3.3V	D2	**Power OK** Valid only in Endpoint mode. When the available power indicated in the PCI Express Set Slot Power Limit message is greater than or equal to the power requirement indicated in the **PECS_POWER** register, PWR_OK is asserted.
ROOT_COMPLEX#	I 3.3V PU	A18	**ROOT_COMPLEX# Mode Select** When Low (asserted), the PEX 8311 acts as a PCI Express Root Complex device (North bridge). When High (de-asserted), the PEX 8311 acts as a PCI Express Endpoint device (peripheral board).

2.6   JTAG Interface Signals

Table 2-11.   JTAG Interface Signals (5 Balls)

Signal	Type	Balls	Description
TCK	I	A13	**Test Clock** JTAG test clock. Sequences the Test Access Port (TAP) Controller as well as all JTAG registers. Ground when JTAG is not used.
TDI	I PU	A14	**Test Data Input** Serial data input to **JTAG Instruction** and **Data** registers. TAP Controller state and particular instruction held in the instruction register determines which register is fed by TDI for a specific operation. TDI is sampled into the JTAG registers on the rising edge of TCK. Hold open when JTAG is not used.
TDO	O TS 12 mA 3.3V	C14	**Test Data Output** Serial data output for **JTAG Instruction** and **Data** registers. The TAP Controller state and particular instruction held in the instruction register determines which register feeds TDO for a specific operation. Only one register (instruction or data) is allowed as the active connection between TDI and TDO for any given operation. TDO changes state on the falling edge of TCK and is only active during the shifting of data through the device. TDO is placed into a high-impedance state at all other times. Hold open when JTAG is not used.
TMS	I PU	A11	**Test Mode Select** Mode input signal to the TAP Controller. The TAP Controller is a 16-state FSM that provides the control logic for JTAG. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP Controller. Hold open when JTAG is not used.
TRST#	I PU	B14	**Test Reset** Active-Low input used to reset the Test Access Port. When JTAG functionality is not used, the TRST# input should be pulled or driven Low, to place the JTAG TAP Controller into the Test-Logic-Reset state, which disables the test logic and enables standard logic operation. Alternatively, if TRST# input is High, the JTAG TAP Controller can be placed into the Test-Logic-Reset state by initializing the JTAG TAP Controller's Instruction register to contain the IDCODE instruction, or by holding the TMS input High for at least five rising edges of the TCK input.

2.7 Test Signals

Table 2-12.   Test Signals (12 Balls)

Signal	Type	Balls	Description
BD_SEL#	I PCI	B19	**Board Select** Selects a device to operate in standard mode. When asserted Low, standard operation is selected. When asserted High, Factory Test operation is selected.
BTON	I	D10	**Test Enable** Connect to ground for standard operation.
BUNRI	I	F3	**Test Mode Select** Connect to ground for standard operation.
IDDQEN#	I PD	V10	**IDDQ Enable** Places the PEX 8311 Local Bus Output buffers into a quiescent state. Asserting IDDQEN# to logic Low (0) along with BD_SEL# to logic High (1) forces the PEX 8311 Local Bus I/Os to be tri-stated and all analog power is disabled. For standard operation, pull IDDQEN# High, using a resistor of 10KΩ or less.
ITDO	I/O	C15	**Internal Test Data** External pull-up resistor required for standard operation.
PLXT1	I	A3	**PLX-Defined Test 1** Connect to power through a pull-up resistor for standard operation.
PLXT2	I	A10	**PLX-Defined Test 2** Must be connected to ground for standard operation.
SMC	I	V4	**Scan Path Mode Control** Connect to ground for standard operation.
TEST	I	N1	**Test Mode Select** Connect to ground for standard operation.
TMC	I	E2	**Test Mode Control** Connect to ground for standard operation.
TMC1	I	V3	**IDDQ Test Control Input** Connect to ground for standard operation.
TMC2	I	E3	**I/O Buffer Control** Connect to ground for standard operation.

2.8 No Connect Signals

Table 2-13.   No Connect Signals (59 Balls)

Signal	Type	Balls	Description
N/C	I/O Manufacturer Test Balls	A4, A5, A6, A7, A9, A12, B3, B4, B5, B6, B7, B8, B9, B11, B12, B13, C4, C5, C6, C7, C8, C10, C11, C12, D4, D5, D11, D16, E4, E6, M2, N2, N3, N4, P1, P2, P3, P4, R1, R2, R3, R4, T1, T2, T3, T4, U1, U2, U3, U4, U7, V2, V5, V6, V7, V8, W6, W7, Y6	**No Connect (59 Balls)** Signals designated *N/C* are true no connects and cannot be used to route other functional signals across the board. Must remain floating for standard operation. ***Note:*** *We recommend connecting T4 to PERST# through a schottky diode, BAT54 or equivalent, see PEX8311 erratum titled 'External Reset for PCLKO clock generator insures reliable PCLKO output'*

2.9 Power and Ground Signals

Table 2-14. Power and Ground Signals (138 Balls)

Signal	Type	Balls	Description
Main Power (Core Logic, I/O Buffers – 128 Balls)			
AVDD	Power	G3	**Analog Supply Voltage** Connect to the +1.5V power supply.
VDD1.5	Power	C2, C9, C13, D6, L1, L2, M1, W5	**Core Supply Voltage (8 Balls)** Connect to the +1.5V power supply.
VDD2.5	Power	C17, H18, J17, T16, U15, V9, Y5	**Local Core Supply Voltage (7 Balls)** Connect to the +2.5V power supply.
VDD3.3	Power	D7, D8, D9, E5, E9, E15, E16, E17, F5, F15, F16, F17, G15, G16, H16, J16, K16, N16, P16, R16, T12, T15, U10, U11, U14, V14	**I/O Supply Voltage (26 Balls)** Connect to the +3.3V power supply.
GND	Ground	A2, A16, A17, B15, B16, D12, D13, D14, D15, E7, E8, E10, E11, E12, E13, E14, F6, F7, F8, F9, F10, F11, F12, F13, F14, G5, G6, G7, H5, H6, H15, J5, J6, J15, K4, K5, K6, K15, L5, L6, M4, M5, M6, N5, N6, N15, P5, P6, P15, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, T5, T6, T7, T8, T9, T10, T11, T13, T14, U5, U6, U8, U9, U12, U13, V1, V12, V13, W1, W2, W3, W4, Y1, Y2, Y3, Y4	**Ground (86 Balls)** Connect to ground.

Table 2-14.   Power and Ground Signals (138 Balls) (Cont.)

Signal	Type	Balls	Description
PCI Express Interface Power (10 Balls)			
AVSS	Ground	J3	**Analog Ground** Connect to ground.
VDD_P	Power	J2	**PLL Supply Voltage** Connect to the +1.5V filtered PLL power supply.
VDD_R	Power	H3	**Receiver Supply Voltage** Connect to the +1.5V power supply.
VDD_T	Power	J4	**Transmitter Supply Voltage** Connect to the +1.5V power supply.
VSS_C	Ground	F4	**Common Ground** Connect to ground.
VSS_P0	Ground	H4	**PLL Ground** Connect to ground.
VSS_P1	Ground	G4	**PLL Ground** Connect to ground.
VSS_R	Ground	F1	**Receiver Ground** Connect to ground.
VSS_RE	Ground	G2	**Receiver Ground** Connect to ground.
VSS_T	Ground	K1	**Transmitter Ground** Connect to ground.

2.10   Ball Assignments

2.10.1   Ball Assignments by Location

Table 2-15.   Ball Assignments by Location

Location	Local Bus Mode		
	C	**J**	**M**
A1	GPIO3	GPIO3	GPIO3
A2	GND	GND	GND
A3	PLXT1	PLXT1	PLXT1
A4	N/C	N/C	N/C
A5	N/C	N/C	N/C
A6	N/C	N/C	N/C
A7	N/C	N/C	N/C
A8	CLKOUT	CLKOUT	CLKOUT
A9	N/C	N/C	N/C
A10	PLXT2	PLXT2	PLXT2
A11	TMS	TMS	TMS
A12	N/C	N/C	N/C
A13	TCK	TCK	TCK
A14	TDI	TDI	TDI
A15	CLKIN	CLKIN	CLKIN
A16	GND	GND	GND
A17	GND	GND	GND
A18	ROOT_COMPLEX#	ROOT_COMPLEX#	ROOT_COMPLEX#
A19	EESK	EESK	EESK
A20	EECS	EECS	EECS
B1	GPIO1	GPIO1	GPIO1
B2	WAKEIN#	WAKEIN#	WAKEIN#
B3	N/C	N/C	N/C
B4	N/C	N/C	N/C
B5	N/C	N/C	N/C
B6	N/C	N/C	N/C
B7	N/C	N/C	N/C
B8	N/C	N/C	N/C
B9	N/C	N/C	N/C
B10	PMEOUT#	PMEOUT#	PMEOUT#
B11	N/C	N/C	N/C
B12	N/C	N/C	N/C
B13	N/C	N/C	N/C

Table 2-15.   Ball Assignments by Location (Cont.)

Location	Local Bus Mode		
	C	J	M
B14	TRST#	TRST#	TRST#
B15	GND	GND	GND
B16	GND	GND	GND
B17	DREQ1#	DREQ1#	DREQ1#
B18	DACK1#	DACK1#	DACK1#
B19	BD_SEL#	BD_SEL#	BD_SEL#
B20	EEDI/EEDO	EEDI/EEDO	EEDI/EEDO
C1	GPIO0	GPIO0	GPIO0
C2	VDD1.5	VDD1.5	VDD1.5
C3	PERST#	PERST#	PERST#
C4	N/C	N/C	N/C
C5	N/C	N/C	N/C
C6	N/C	N/C	N/C
C7	N/C	N/C	N/C
C8	N/C	N/C	N/C
C9	VDD1.5	VDD1.5	VDD1.5
C10	N/C	N/C	N/C
C11	N/C	N/C	N/C
C12	N/C	N/C	N/C
C13	VDD1.5	VDD1.5	VDD1.5
C14	TDO	TDO	TDO
C15	ITDO	ITDO	ITDO
C16	PMEIN#	PMEIN#	PMEIN#
C17	VDD2.5	VDD2.5	VDD2.5
C18	DMPAF or EOT#	DMPAF or EOT#	MDREQ# or DMPAF or EOT#
C19	DREQ0#	DREQ0#	DREQ0#
C20	DACK0#	DACK0#	DACK0#
D1	WAKEOUT#	WAKEOUT#	WAKEOUT#
D2	PWR_OK	PWR_OK	PWR_OK
D3	GPIO2	GPIO2	GPIO2
D4	N/C	N/C	N/C
D5	N/C	N/C	N/C
D6	VDD1.5	VDD1.5	VDD1.5
D7	VDD3.3	VDD3.3	VDD3.3
D8	VDD3.3	VDD3.3	VDD3.3
D9	VDD3.3	VDD3.3	VDD3.3
D10	BTON	BTON	BTON

Table 2-15.   Ball Assignments by Location (Cont.)

Location	Local Bus Mode		
	C	**J**	**M**
D11	N/C	N/C	N/C
D12	GND	GND	GND
D13	GND	GND	GND
D14	GND	GND	GND
D15	GND	GND	GND
D16	N/C	N/C	N/C
D17	CCS#	CCS#	CCS#
D18	BIGEND#	BIGEND#	BIGEND# or WAIT#
D19	USERo or LLOCKo#	USERo or LLOCKo#	USERo or LLOCKo#
D20	USERi or LLOCKi#	USERi or LLOCKi#	USERi or LLOCKi#
E1	BAR0ENB#	BAR0ENB#	BAR0ENB#
E2	TMC	TMC	TMC
E3	TMC2	TMC2	TMC2
E4	N/C	N/C	N/C
E5	VDD3.3	VDD3.3	VDD3.3
E6	N/C	N/C	N/C
E7	GND	GND	GND
E8	GND	GND	GND
E9	VDD3.3	VDD3.3	VDD3.3
E10	GND	GND	GND
E11	GND	GND	GND
E12	GND	GND	GND
E13	GND	GND	GND
E14	GND	GND	GND
E15	VDD3.3	VDD3.3	VDD3.3
E16	VDD3.3	VDD3.3	VDD3.3
E17	VDD3.3	VDD3.3	VDD3.3
E18	LRESET#	LRESET#	LRESET#
E19	LINTo#	LINTo#	LINTo#
E20	LINTi#	LINTi#	LINTi#
F1	VSS_R	VSS_R	VSS_R
F2	PERn0	PERn0	PERn0
F3	BUNRI	BUNRI	BUNRI
F4	VSS_C	VSS_C	VSS_C
F5	VDD3.3	VDD3.3	VDD3.3
F6	GND	GND	GND
F7	GND	GND	GND

Table 2-15.   Ball Assignments by Location (Cont.)

Location	Local Bus Mode		
	C	J	M
F8	GND	GND	GND
F9	GND	GND	GND
F10	GND	GND	GND
F11	GND	GND	GND
F12	GND	GND	GND
F13	GND	GND	GND
F14	GND	GND	GND
F15	VDD3.3	VDD3.3	VDD3.3
F16	VDD3.3	VDD3.3	VDD3.3
F17	VDD3.3	VDD3.3	VDD3.3
F18	READY#	READY#	TA#
F19	ADS#	ADS#	TS#
F20	BLAST#	BLAST#	BURST#
G1	PERp0	PERp0	PERp0
G2	VSS_RE	VSS_RE	VSS_RE
G3	AVDD	AVDD	AVDD
G4	VSS_P1	VSS_P1	VSS_P1
G5	GND	GND	GND
G6	GND	GND	GND
G7	GND	GND	GND
G15	VDD3.3	VDD3.3	VDD3.3
G16	VDD3.3	VDD3.3	VDD3.3
G17	BREQo	BREQo	RETRY#
G18	BREQi	BREQi	BB#
G19	LHOLDA	LHOLDA	BG#
G20	LHOLD	LHOLD	BR#
H1	REFCLK+	REFCLK+	REFCLK+
H2	REFCLK-	REFCLK-	REFCLK-
H3	VDD_R	VDD_R	VDD_R
H4	VSS_P0	VSS_P0	VSS_P0
H5	GND	GND	GND
H6	GND	GND	GND
H15	GND	GND	GND
H16	VDD3.3	VDD3.3	VDD3.3
H17	WAIT#	WAIT#	BDIP#
H18	VDD2.5	VDD2.5	VDD2.5

Table 2-15.   Ball Assignments by Location (Cont.)

Location	Local Bus Mode		
	C	**J**	**M**
H19	MODE0	MODE0	MODE0
H20	MODE1	MODE1	MODE1
J1	PETp0	PETp0	PETp0
J2	VDD_P	VDD_P	VDD_P
J3	AVSS	AVSS	AVSS
J4	VDD_T	VDD_T	VDD_T
J5	GND	GND	GND
J6	GND	GND	GND
J15	GND	GND	GND
J16	VDD3.3	VDD3.3	VDD3.3
J17	VDD2.5	VDD2.5	VDD2.5
J18	LSERR#	LSERR#	TEA#
J19	BTERM#	BTERM#	BI#
J20	LCLK	LCLK	LCLK
K1	VSS_T	VSS_T	VSS_T
K2	PETn0	PETn0	PETn0
K3	EECS#	EECS#	EECS#
K4	GND	GND	GND
K5	GND	GND	GND
K6	GND	GND	GND
K15	GND	GND	GND
K16	VDD3.3	VDD3.3	VDD3.3
K17	LD3	LAD3	LD28
K18	LD2	LAD2	LD29
K19	LD1	LAD1	LD30
K20	LD0	LAD0	LD31
L1	VDD1.5	VDD1.5	VDD1.5
L2	VDD1.5	VDD1.5	VDD1.5
L3	EEWRDATA	EEWRDATA	EEWRDATA
L4	EECLK	EECLK	EECLK
L5	GND	GND	GND
L6	GND	GND	GND
L15	DP1	DP1	DP2
L16	DP0	DP0	DP3
L17	LD7	LAD7	LD24
L18	LD6	LAD6	LD25

Table 2-15. Ball Assignments by Location (Cont.)

Location	Local Bus Mode		
	C	J	M
L19	LD5	LAD5	LD26
L20	LD4	LAD4	LD27
M1	VDD1.5	VDD1.5	VDD1.5
M2	N/C	N/C	N/C
M3	EERDDATA	EERDDATA	EERDDATA
M4	GND	GND	GND
M5	GND	GND	GND
M6	GND	GND	GND
M15	DP3	DP3	DP0
M16	DP2	DP2	DP1
M17	LD11	LAD11	LD20
M18	LD10	LAD10	LD21
M19	LD9	LAD9	LD22
M20	LD8	LAD8	LD23
N1	TEST	TEST	TEST
N2	N/C	N/C	N/C
N3	N/C	N/C	N/C
N4	N/C	N/C	N/C
N5	GND	GND	GND
N6	GND	GND	GND
N15	GND	GND	GND
N16	VDD3.3	VDD3.3	VDD3.3
N17	LD15	LAD15	LD16
N18	LD14	LAD14	LD17
N19	LD13	LAD13	LD18
N20	LD12	LAD12	LD19
P1	N/C	N/C	N/C
P2	N/C	N/C	N/C
P3	N/C	N/C	N/C
P4	N/C	N/C	N/C
P5	GND	GND	GND
P6	GND	GND	GND
P15	GND	GND	GND
P16	VDD3.3	VDD3.3	VDD3.3
P17	LD19	LAD19	LD12
P18	LD18	LAD18	LD13

Table 2-15.   Ball Assignments by Location (Cont.)

Location	Local Bus Mode		
	C	**J**	**M**
P19	LD17	LAD17	LD14
P20	LD16	LAD16	LD15
R1	N/C	N/C	N/C
R2	N/C	N/C	N/C
R3	N/C	N/C	N/C
R4	N/C	N/C	N/C
R5	GND	GND	GND
R6	GND	GND	GND
R7	GND	GND	GND
R8	GND	GND	GND
R9	GND	GND	GND
R10	GND	GND	GND
R11	GND	GND	GND
R12	GND	GND	GND
R13	GND	GND	GND
R14	GND	GND	GND
R15	GND	GND	GND
R16	VDD3.3	VDD3.3	VDD3.3
R17	LD23	LAD23	LD8
R18	LD22	LAD22	LD9
R19	LD21	LAD21	LD10
R20	LD20	LAD20	LD11
T1	N/C	N/C	N/C
T2	N/C	N/C	N/C
T3	N/C	N/C	N/C
T4	N/C	N/C	N/C
T5	GND	GND	GND
T6	GND	GND	GND
T7	GND	GND	GND
T8	GND	GND	GND
T9	GND	GND	GND
T10	GND	GND	GND
T11	GND	GND	GND
T12	VDD3.3	VDD3.3	VDD3.3
T13	GND	GND	GND
T14	GND	GND	GND
T15	VDD3.3	VDD3.3	VDD3.3

Table 2-15. Ball Assignments by Location (Cont.)

Location	Local Bus Mode		
	C	J	M
T16	VDD2.5	VDD2.5	VDD2.5
T17	LD27	LAD27	LD4
T18	LD26	LAD26	LD5
T19	LD25	LAD25	LD6
T20	LD24	LAD24	LD7
U1	N/C	N/C	N/C
U2	N/C	N/C	N/C
U3	N/C	N/C	N/C
U4	N/C	N/C	N/C
U5	GND	GND	GND
U6	GND	GND	GND
U7	N/C	N/C	N/C
U8	GND	GND	GND
U9	GND	GND	GND
U10	VDD3.3	VDD3.3	VDD3.3
U11	VDD3.3	VDD3.3	VDD3.3
U12	GND	GND	GND
U13	GND	GND	GND
U14	VDD3.3	VDD3.3	VDD3.3
U15	VDD2.5	VDD2.5	VDD2.5
U16	LA12	LA12	LA19
U17	LA8	LA8	LA23
U18	LW/R#	LW/R#	RD/WR#
U19	LD29	LAD29	LD2
U20	LD28	LAD28	LD3
V1	GND	GND	GND
V2	N/C	N/C	N/C
V3	TMC1	TMC1	TMC1
V4	SMC	SMC	SMC
V5	N/C	N/C	N/C
V6	N/C	N/C	N/C
V7	N/C	N/C	N/C
V8	N/C	N/C	N/C
V9	VDD2.5	VDD2.5	VDD2.5
V10	IDDQEN#	IDDQEN#	IDDQEN#
V11	LA24	LA24	LA7
V12	GND	GND	GND

Table 2-15. Ball Assignments by Location (Cont.)

Location	Local Bus Mode		
	C	J	M
V13	GND	GND	GND
V14	VDD3.3	VDD3.3	VDD3.3
V15	LA15	LA15	LA16
V16	LA11	LA11	LA20
V17	LA7	LA7	LA24
V18	LA4	LA4	LA27
V19	LD31	LAD31	LD0
V20	LD30	LAD30	LD1
W1	GND	GND	GND
W2	GND	GND	GND
W3	GND	GND	GND
W4	GND	GND	GND
W5	VDD1.5	VDD1.5	VDD1.5
W6	N/C	N/C	N/C
W7	N/C	N/C	N/C
W8	LA30	DEN#	LA1
W9	LA28	LA28	LA3
W10	LA26	LA26	LA5
W11	LA23	LA23	LA8
W12	LA21	LA21	LA10
W13	LA19	LA19	LA12
W14	LA17	LA17	LA14
W15	LA14	LA14	LA17
W16	LA10	LA10	LA21
W17	LA6	LA6	LA25
W18	LA3	LA3	LA28
W19	LBE0#	LBE0#	LA31
W20	LBE1#	LBE1#	LA30
Y1	GND	GND	GND
Y2	GND	GND	GND
Y3	GND	GND	GND
Y4	GND	GND	GND
Y5	VDD2.5	VDD2.5	VDD2.5
Y6	N/C	N/C	N/C
Y7	LA31	DT/R#	LA0
Y8	LA29	ALE	LA2
Y9	LA27	LA27	LA4

Table 2-15.   Ball Assignments by Location (Cont.)

Location	Local Bus Mode		
	C	**J**	**M**
Y10	LA25	LA25	LA6
Y11	LA22	LA22	LA9
Y12	LA20	LA20	LA11
Y13	LA18	LA18	LA13
Y14	LA16	LA16	LA15
Y15	LA13	LA13	LA18
Y16	LA9	LA9	LA22
Y17	LA5	LA5	LA26
Y18	LA2	LA2	LA29
Y19	LBE3#	LBE3#	TSIZ0
Y20	LBE2#	LBE2#	TSIZ1

2.11   PEX 8311 Physical Layout

Figure 2-1.   PEX 8311 Physical Ball Assignment – C, J, and M Modes (See-Through Top View)

Chapter 3   Reset Operation and Initialization Summary

3.1   Endpoint Mode Reset Operation

The PEX 8311 operates in Endpoint mode when the ROOT_COMPLEX# ball is strapped High.

The actions that the PEX 8311 takes upon receipt of various reset events and interface initialization requirements are described in the following sections.f

3.1.1   Full Device Resets

The PEX 8311 receives four types of reset over the PCI Express interface:

- Physical layer resets that are platform-specific and referred to as *Fundamental Resets* (Cold/Warm Reset; PCI Express PERST# signal is asserted (refer to *PCI Express Base 1.0a*, Section 6.6)
- PCI Express Physical Layer mechanism (Hot Reset)
- PCI Express Data Link transitioning to the PCI Express interface DL_Down state
- PCI Express Power Management Reset (D3 to D0 state)

These four PCI Express interface reset sources are described in the sections that follow. PCI Express Reset events initiate a Local Bus Reset, which resets PEX 8311 registers and Local Bus backend logic.

Table 3-1 defines which device resources are reset when each of the PCI Express reset sources are asserted.

Table 3-1.   Full Device Reset Behavior

Reset Sources	Device Resources			
	PCI Express Interface Logic	Local Interface Logic	LRESET# Is Asserted	Configuration Registers
PCI Express PERST# signal is asserted	✓	✓	✓	✓
PCI Express Hot Reset	✓	✓	✓	✓[a]
PCI Express Link Down	✓	✓	✓	✓[a]
D3 to D0 Power Management Reset	✓	✓	✓	✓

a. The **PECS_GPIOCTL** register is not reset for Link Down nor Hot Reset.

3.1.1.1   PCI Express Reset PERST# Input (Hard Reset)

The PCI Express Reset PERST# input ball is a PCI Express System reset. It is asserted by the Root Complex and causes all PCI Express downstream devices to reset. The PEX 8311 is reset upon receiving PERST# asserted and causes Local LRESET# to assert. Most Local Bus output signals are set to float while LRESET# remains asserted, with the exceptions defined in Table 3-2.

The PEX 8311 uses the PCI Express PERST# signal as a Fundamental Reset input. When PERST# assertion follows the power-on event, it is referred to as a *Cold Reset*. The PCI Express system also generates this signal without removing power; which is referred to as a *Warm Reset*. The PEX 8311 treats Cold and Warm Resets without distinction. When PERST# input is asserted Low, all PEX 8311 internal logic is asynchronously reset, and all Configuration registers are initialized to their default values when PERST# is asserted. The PEX 8311 also places its Local Bus outputs into a high-impedance state, unless stated otherwise in Table 3-2 and Section 2.4, "Local Bus Signals."

The PEX 8311 propagates the Cold/Warm Reset from the PCI Express interface to the Local reset interface. The LRESET# signal is asserted while PERST# is asserted. During a Cold Reset, LRESET# is asserted for at least 100 ms after the power levels are valid. During other types of resets, LRESET# is asserted for at least 1 ms. Local Bus Masters must allow sufficient time for the **LCS** serial EEPROM load to complete before attempting accesses to PEX 8311 registers or PCI Express Space (this time depends upon the serial EEPROM load length).

Table 3-2.   Local Bus Output Signals that Do Not Float when PERST# Is Asserted

Signal	Value when PERST# Is Asserted
EECS	0
EESK	0
LRESET#	0
USERo	0

3.1.1.2   Link Training and Status State Machine (LTSSM) Hot Reset

PCI Express supports the Link Training Control Reset (a training sequence with the *Hot Reset* bit asserted), or Hot Reset (as described in *PCI Express Base 1.0a*, Section 4.2.5.11), for propagating Reset requests downstream. When the PEX 8311 receives a Hot Reset on the PCI Express interface, it propagates that reset to the Local LRESET# signal. In addition, the PEX 8311 discards all transactions being processed and returns registers, state machines, and externally observable state internal logic to the state-specified default or initial conditions. Software is responsible for ensuring that the Link Reset assertion and de-assertion messages are timed such that the bridge adheres to proper reset assertion and de-assertion durations on the Local LRESET# signal.

3.1.1.3   Primary Reset Due to Data Link Down

When the PEX 8311 PCI Express interface is in standard operation and the Link is down, the Transaction and Data Link Layers enter the DL_Down state. The PEX 8311 discards all transactions being processed and returns registers, state machines, and externally observable state internal logic to the state-specified default or initial conditions. In addition, the entry of the PEX 8311 PCI Express interface into DL_Down status initiates a Local Bus reset, using the Local LRESET# signal.

3.1.1.4   PCI Express Configuration Space Power Management Reset

When the **PECS Power Management Control/Status** register *Power State* field (**PECS_PWRMNGCSR**[1:0]) transitions from 11b (D3) to 00b (D0), a Full Device Reset is initiated. The effects of this reset are identical to a PERST# Hard Reset, as described in Section 3.1.1.1. This sequence includes:

1. All logic is reset.
2. All **PECS** and **LCS** registers are reset.
3. Local LRESET# is asserted.
4. **PECS** and **LCS** serial EEPROMs load.

3.1.2   Local Bus Bridge Resets

In addition to PCI Express interface reset sources, the PEX 8311 supports the following Partial Device Resets:

- Local Bus Bridge Full Reset, by way of the **PECS Bridge Control** register (**PECS_BRIDGECTL**[6])

- Local Bus Bridge Local Bus Reset, by way of the **LCS Control** register (**LCS_CNTRL**[30])

When attempting a Configuration access to the PEX 8311 on the Local Bus, the Local Bus Master device must allow sufficient time for the **LCS** serial EEPROM load to complete before attempting accesses to the PEX 8311 (this time depends upon the serial EEPROM load length).

3.1.2.1   Local Bus Bridge Full Reset by way of PECS Bridge Control Register

A Local Bus interface reset is initiated by software, by setting the **PECS Bridge Control** register *Local Bridge Full Reset* bit (**PECS_BRIDGECTL**[6]). This targeted reset is used for various reasons, including recovery from error conditions on the Local Bus, or to initiate re-enumeration. Writing 1 to the *Local Bridge Full Reset* bit resets all **Local Space Configuration** registers and Local Bus logic, and forces the Local Bus Reset (LRESET#) signal to assert.

The Local Bus bridge and backend logic remain held in reset while the *Local Bridge Full Reset* bit remains set. Software is responsible for ensuring that the PEX 8311 does not receive transactions that require forwarding to the **LCS** registers or Local Bus while the *Local Bridge Full Reset* bit is set. When the *Local Bridge Full Reset* bit is cleared, the **LCS** registers are initialized from the **LCS** serial EEPROM, or set to hardwired defaults if no serial EEPROM is present. Designers must allow sufficient time for this operation to complete before attempting accesses to **LCS** registers or devices on the opposite bus. In addition, the **LCS PCI Configuration** registers (*such as*, **LCS_PCICR** and **LCS_PCIBAR0**, **LCS_PCIBAR1**, **LCS_PCIBAR2**, and **LCS_PCIBAR3**) must be re-initialized by system software before attempting accesses from PCI Express Space to the **LCS** Memory-Mapped registers or Local Bus.

3.1.2.2   Local Bus Bridge Local Bus Reset

A Local Bus bridge Local Bus reset is initiated by the **LCS Control** register *Local Bus Reset* bit. When the *Local Bus Reset* bit is set (**LCS_CNTRL**[30]=1), the following functional blocks are reset:

- Local Bus logic
- DMA logic
- Local Space FIFOs
- **LCS Local Configuration** and **Messaging Queue** registers

The internal PCI Bus logic, **LCS PCI Configuration**, **DMA**, and **Runtime** registers, and *Local Init Status* bit (**LCS_LMISC1**[2]) are not reset.

When the *Local Bus Reset* bit is set (**LCS_CNTRL**[30]=1), the PEX 8311 responds to Type 0/Type 1, Memory-Mapped Configuration access to **LCS PCI Configuration**, **Local**, **Runtime**, and **DMA** registers, initiated from the PCI Express interface. Because the Local Bus is in reset, **LCS Local Configuration** and **Messaging Queue** registers are not accessible from PCI Express Space, and accesses are ***not*** allowed on the Local Bus. The PEX 8311 remains in this condition until the PCI Express Root Complex clears the bit (**LCS_CNTRL**[30]=0). The Local Bus serial EEPROM is reloaded when the *Reload Configuration Registers* bit is set (**LCS_CNTRL**[29]=1).

During a software reset, USERo is driven Low. USERo (and PERST#) behavior is as follows:

- During a Hard reset (PERST#=0), USERo is tri-stated. On the second rising edge of LCLK after PERST# is de-asserted, LRESET# is de-asserted. On the next falling edge of LCLK, USERo is driven to 0 (from tri-state). On the next rising edge of LCLK, USERo is driven to the value specified in **LCS_CNTRL**[16] (default value = 1).

- When the *Local Bus Reset* bit is set (**LCS_CNTRL**[30]=1), the LRESET# and USERo signals are asserted Low (0). When the *Local Bus Reset* bit is cleared (**LCS_CNTRL**[30]=0), USERo reverts to the value specified in **LCS_CNTRL**[16], one LCLK after the LRESET# signal is de-asserted (driven to 1).

Note: *The Local Bus cannot clear* **LCS_CNTRL***[30] because the Local Bus is in a reset state, although the Local processor does not use LRESET# to reset.*

3.1.2.3   Local Configuration Space Power Management Reset

An **LCS** Power Management Reset occurs when the **LCS Power Management Control/Status** register *Power State* field (**LCS_PMCSR**[1:0]) transitions from D3hot-to-D0. This action results in a Local Bus bridge Full Reset, as described in Section 3.1.2, "Local Bus Bridge Resets."

3.2   Root Complex Mode Reset Operation

The PEX 8311 operates in Root Complex mode when its ROOT_COMPLEX# signal is strapped Low. Table 3-3 defines the four Root Complex mode Reset mechanisms.

Table 3-4 defines which device resources are reset when each of the Local Bus reset sources are asserted or set.

Table 3-3.   Root Complex Mode Reset Mechanisms

Reset Mechanism	Reset Type	Description
Local LRESET# signal	Hard Reset	Upon LRESET# assertion, all internal logic and registers are reset, and a Fundamental Reset is output to PCI Express Space through PERST# assertion. When LRESET# is de-asserted, the **PECS** and **LCS** serial EEPROMs are loaded.
LCS Control register *Local Bus Reset* bit (**LCS_CNTRL**[30])	PCI Express Bridge Reset	Causes a Partial Reset of the Local Bus bridge and Full Reset of the PCI Express bridge. When cleared, the **PECS** and **LCS** serial EEPROMs are loaded.
PECS Bridge Control register *PCI Express Hot Reset* bit (**PECS_BRIDGECTL**[6])	PCI Express Interface Reset	Generates an LTSSM Hot Reset to PCI Express Space.
PECS Power Management Control/Status register *Power State* bit transition from D3 to D0 state (**PECS_PWRMNGCSR**[1:0])	PCI Express Power Management Reset	Resets the **PECS PCI Configuration** registers, and generates an LTSSM Hot Reset to PCI Express Space.

Table 3-4.   Root Complex Mode Reset Behavior

Reset Source	Device Resources				
	LCS Registers		PECS Registers	PCI Express Reset Out	
	Local, Runtime, Messaging Queue	PCI, DMA, EEPROM_RD	ALL_REGS, EEPROM_RD	Hot Reset (LTSSM)	Fundamental Reset (PERST#)
LRESET# signal	✓	✓	✓	✓	✓
LCS_CNTRL[30]=1		✓	✓	✓	✓
PECS_BRIDGECTL[6]=1				✓	
PECS_PWRMNGCSR[1:0] D3hot to D0			✓	✓	

3.2.1   Local Bus Reset

In Root Complex mode (ROOT_COMPLEX# strapped Low), the Local LRESET# signal is the primary hardware Reset input. LRESET# assertion results in a complete reset of all PEX 8311 internal logic and **PECS** and **LCS** registers. LRESET# assertion also causes PERST# assertion, which resets downstream devices as well. The **PECS** and **LCS** register serial EEPROM load begins after LRESET# is de-asserted.

Table 3-5 defines the Local Bus Output signals that do not float when LRESET# is asserted.

Table 3-5.   Local Bus Output Signals that Do Not Float when LRESET# Is Asserted

Signal	Value when LRESET# Is Asserted
EECS	0
EESK	0
USERo	0

3.2.2   PCI Express Bridge Reset

A reset to the PCI Express interface, PCI Express logic, and localized Local Bus logic within the PEX 8311 is initiated by the **LCS Control** register *PCI Express Bridge Reset* bit. When the *PCI Express Bridge Reset* bit is set (**LCS_CNTRL**[30]=1), the following functional blocks are reset:

* Master logic on the Internal PCI Bus
* Slave logic on the Internal PCI Bus
* DMA logic
* **LCS Type 1 Configuration**, **Mailbox**, and **DMA** *registers*, and all **PECS** registers
* PCI Express logic
* Local Space FIFOs
* Internal interrupts/lock
* Power Management interrupts
* PERST# is asserted to PCI Express interface

The Local Bus logic, **LCS Configuration**, **Runtime**, and **Messaging Queue** registers are *not* reset. A PCI Express Bridge Reset is cleared only by a Local Bus Master on the Local Bus. The PEX 8311 remains in this reset condition for the duration that the *PCI Express Bridge Reset* bit is set (**LCS_CNTRL**[30]=1). During this time, the PEX 8311 responds only to Local Bus-initiated **LCS Configuration**, **Runtime**, and **DMA** registers' accesses.

Note: *The PCI Express Bridge Reset bit cannot be cleared from the PCI Express interface because the PCI Express is in a reset state and Configuration accesses to Root Complex by the downstream devices are illegal.*

3.2.3   PCI Express Hot Reset by way of PECS Bridge Control Register

A PCI Express interface reset is initiated by software, by setting the **PECS Bridge Control** register *PCI Express Hot Reset* bit (**PECS_BRIDGECTL**[6]). This targeted reset is used for various reasons, including recovery from error conditions on the PCI Express interface, or to initiate re-enumeration.

A Write to the *PCI Express Hot Reset* bit causes a PCI Express Link Training and Status State Machine (LTSSM) Hot Reset sequence to transmit, without affecting the **LCS** registers. In addition, the logic associated with the PCI Express interface is re-initialized and transaction buffers associated with the PCI Express interface are cleared.

3.2.4   PCI Express Configuration Space Power Management Reset

When the **PECS Power Management Control/Status** register *Power State* field (**PECS_PWRMNGCSR**[1:0]) changes from 11b (D3) to 00b (D0), a Fundamental Reset of the PCI Express bridge is initiated. This sequence includes:

1. All **PECS** registers are reset.
2. All PCI Express logic is reset.
3. LTSSM Hot Reset is transmitted to PCI Express Space.
4. PECS serial EEPROM loads.

LCS registers are *not* affected. Register values loaded by the Local Host processor, after the **PECS** serial EEPROM loads, must be restored before resuming operation.

3.3   Initialization Summary

3.3.1   PCI Express Interface

The PEX 8311 supports the following initialization sequences on the PCI Express interface:

- No serial EEPROM, blank serial EEPROM, or invalid serial EEPROM
    - If the first byte read from the serial EEPROM is not a valid signature byte (5Ah), then an invalid serial EEPROM is detected. In this case, the default PCI Express Device ID (8111h) is selected. Use a 10KΩ pull-up resistor to ensure that EERDDATA is High when no serial EEPROM is installed.
    - Enable the PCI Express and internal PCI Buss, using default register values.
- Valid serial EEPROM with Configuration register data
    - Enable the PCI Express and internal PCI Buss using register values loaded from the serial EEPROM. The **PECS_DEVINIT** register interface enable bits are the last bits set by the serial EEPROM.

3.3.2   Local Bus Interface

The PEX 8311 supports the following initialization sequences on the Local Bus interface:

- No serial EEPROM, blank serial EEPROM, or Local Bus Processor
    - If the EEDI/EEDO ball is always High (1KΩ pull-up resistor is recommended), then no physical serial EEPROM is detected. In this case, the Local Processor must be present to configure the PEX 8311 Local Bus and set Local Init Status bit **LCS_LMISC1**[2]=1.
    - If the EEDI/EEDO ball is always Low (1KΩ pull-down resistor is recommended), then no physical serial EEPROM is detected. In this case, the PEX 8311 Local Bus is reverted to its default values and sets the Local Init Status bit **LCS_LMISC1**[2]=1 by itself, regardless of whether the Local Processor is present. Local Bus Device ID (9056h) is selected.
- Valid serial EEPROM with configuration register data
    - The PEX 8311 Local Bus is configured by the serial EEPROM, and the designer must determine whether to set the Local Init Status bit by serial EEPROM or Local Processor, when present.

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Chapter 4   Serial EEPROM Controllers

4.1   Overview

For initializing its internal registers following power-on or exit from reset, the PEX 8311 provides two serial EEPROM interfaces:

- **SPI-compatible interface** – Used to load registers in PCI Express Configuration Space (**PECS**)
- **Micro-Wire-compatible interface** – Used to load registers in Local Configuration Space (**LCS**)

These serial EEPROMs are required only when default values are not suitable for the application in use.

4.2   PCI Express Configuration Space Serial EEPROM Interface (SPI-Compatible Interface)

The PEX 8311 provides an interface to SPI-compatible serial EEPROMs. This interface consists of a Chip Select, Clock, Write Data, and Read Data balls, and operates at up to 25 MHz. Compatible 128-byte serial EEPROMs include the Atmel AT25010A, Catalyst CAT25C01, and ST Microelectronics M95010W. The PEX 8311 supports up to a 16-MB serial EEPROM, utilizing 1-, 2-, or 3-byte addressing. ThePEX 8311 automatically determines the appropriate addressing mode.

4.2.1 Serial EEPROM Data Format

The serial EEPROM data is stored in the following format, as defined in Table 4-1.

Table 4-1. Serial EEPROM Data

Location	Value	Description
0h	5Ah	Validation Signature
1h	Refer to Table 4-2	Serial EEPROM Format Byte
2h	REG BYTE COUNT (LSB)	Configuration register Byte Count (LSB)
3h	REG BYTE COUNT (MSB)	Configuration register Byte Count (MSB)
4h	REGADDR (LSB)	1st Configuration Register Address (LSB)
5h	REGADDR (MSB)	1st Configuration Register Address (MSB)
6h	REGDATA (Byte 0)	1st Configuration Register Data (Byte 0)
7h	REGDATA (Byte 1)	1st Configuration Register Data (Byte 1)
8h	REGDATA (Byte 2)	1st Configuration Register Data (Byte 2)
9h	REGDATA (Byte 3)	1st Configuration Register Data (Byte 3)
Ah	REGADDR (LSB)	2nd Configuration Register Address (LSB)
Bh	REGADDR (MSB)	2nd Configuration Register Address (MSB)
Ch	REGDATA (Byte 0)	2nd Configuration Register Data (Byte 0)
Dh	REGDATA (Byte 1)	2nd Configuration Register Data (Byte 1)
Eh	REGDATA (Byte 2)	2nd Configuration Register Data (Byte 2)
Fh	REGDATA (Byte 3)	2nd Configuration Register Data (Byte 3)
……		
REG BYTE COUNT + 4	MEM BYTE COUNT (LSB)	Shared memory Byte Count (LSB)
REG BYTE COUNT + 5	MEM BYTE COUNT (MSB)	Shared memory Byte Count (MSB)
REG BYTE COUNT + 6	SHARED MEM (Byte 0)	1st byte Shared memory
REG BYTE COUNT + 7	SHARED MEM (Byte 1)	2nd byte of Shared Memory
……		
FFFFh	SHARED MEM (Byte *n*)	Last byte of Shared Memory

Table 4-2 defines the serial EEPROM Format Byte organization.

Table 4-2.   Serial EEPROM Format Byte

Bits	Description
0	**Configuration Register Load** When set, Configuration registers are loaded from the serial EEPROM. The address of the first Configuration register is located at bytes 3 and 4 in the serial EEPROM. When cleared, and REG BYTE COUNT is non-zero, the Configuration data is read from the serial EEPROM and discarded.
1	**Shared Memory Load** When set, shared memory is loaded from the serial EEPROM starting at location REG BYTE COUNT + 6. The Byte Number to load is determined by the value in serial EEPROM locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5.
7:2	*Reserved*

4.2.2   Initialization

After the device reset is de-asserted, the **Status** register within the serial EEPROM is read to determine whether a serial EEPROM is installed. A pull-up resistor on the EERDDATA ball produces a value of FFh when there is no serial EEPROM installed. If a serial EEPROM is detected, the first byte (validation signature) is read. If a value of 5Ah is read, it is assumed that the serial EEPROM is programmed for the PEX 8311. The serial EEPROM address width is determined while this first byte is read. If the first byte is not 5Ah, the serial EEPROM is blank, or programmed with invalid data. In this case, the PCI Express interface and Generic Local Bus are enabled for a default enumeration. Also, the **PECS_EECTL** register *Serial EEPROM Address Width* field reports a value of 0 (undetermined width).

When the serial EEPROM contains valid data, the second byte (Serial EEPROM Format Byte) is read to determine which sections of the serial EEPROM are loaded into the PEX 8311 Configuration registers and memory.

Bytes 2 and 3 determine the amount of serial EEPROM locations containing configuration register addresses and data. Each configuration register entry consists of two bytes of register address (bit 12 Low selects the PCI Configuration registers, and bit 12 High selects the Memory-Mapped Configuration registers) and four bytes of register Write data. If bit 1 of the serial EEPROM Format Byte is set, locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5 are read to determine the number of bytes to transfer from the serial EEPROM into shared memory.

REG BYTE COUNT must be a multiple of 6 and MEM BYTE COUNT must be a multiple of 4.

The EECLK ball frequency is determined by the **PECS_EECLKFREQ** register *EE Clock Frequency* field. The default clock frequency is 2 MHz. At this clock rate, it takes about 24 μs per DWORD during Configuration register or shared memory initialization. For faster loading of large serial EEPROMs that support a faster clock, the first configuration register load from the serial EEPROM is to the **PECS_EECLKFREQ** register.

Note: When operating in Root Complex mode, ensure that the serial EEPROM sets the
***PECS_DEVINIT** register PCI Enable bit. When operating in Endpoint mode, ensure*
*the serial EEPROM sets the **PECS_DEVINIT** register PCI Express Enable bit.*

4.2.3   Serial EEPROM Random Read/Write Access

A PCI Express or internal PCI Bus Master can use the **PECS_EECTL** register to access the serial EEPROM. This register contains 8-bit Read and Write data fields, Read and Write Start signals, and related status bits.

The following "C" routines demonstrate the firmware protocol required to access the serial EEPROM through the **PECS_EECTL** register. An interrupt is generated when the **PECS_EECTL** register *Serial EEPROM Busy* bit moves from true to false.

4.2.3.1   Serial EEPROM Opcodes

```
READ_STATUS_EE_OPCODE = 5
WREN_EE_OPCODE = 6
WRITE_EE_OPCODE = 2
READ_EE_OPCODE = 3
```

4.2.3.2   Serial EEPROM Low-Level Access Routines

```
int EE_WaitIdle()
{
    int eeCtl, ii;
    for (ii = 0; ii < 100; ii++)
     {
        PEX 8311Read(EECTL, eeCtl);        /* read current value in EECTL */
        if ((eeCtl & (1 << EEPROM_BUSY)) == 0) /* loop until idle */
            return(eeCtl);
    }
    PANIC("EEPROM Busy timeout!\n");
}
void EE_Off()
{
    EE_WaitIdle();                         /* make sure EEPROM is idle */
    PEX 8311Write(EECTL, 0);               /* turn off everything (especially
EEPROM_CS_ENABLE)*/
}
int EE_ReadByte()
{
    int eeCtl = EE_WaitIdle();             /* make sure EEPROM is idle */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
            (1 << EEPROM_BYTE_READ_START);
    PEX 8311Write(EECTL, eeCtl);           /* start reading */
    eeCtl = EE_WaitIdle();                 /* wait until read is done */
    return((eeCtl >> EEPROM_READ_DATA) & FFh); /* extract read data from
EECTL */
}
void EE_WriteByte(int val)
{
    int eeCtl = EE_WaitIdle();             /* make sure EEPROM is idle */
    eeCtl &= ~(FFh << EEPROM_WRITE_DATA);/* clear current WRITE value */
    eeCtl |= (1 << EEPROM_CS_ENABLE) |
            (1 << EEPROM_BYTE_WRITE_START) |
            ((val & FFh) << EEPROM_WRITE_DATA);
    PEX 8311Write(EECTL, eeCtl);
}
```

4.2.3.3   Serial EEPROM Read Status Routine

```
...
EE_WriteByte(READ_STATUS_EE_OPCODE);    /* read status opcode */
status = EE_ReadByte();                 /* get EEPROM status */
EE_Off();                               /* turn off EEPROM */
...
```

4.2.3.4   Serial EEPROM Write Data Routine

```
...
EE_WriteByte(WREN_EE_OPCODE);           /* must first write-enable */
EE_Off();                               /* turn off EEPROM */
EE_WriteByte(WRITE_EE_OPCODE);          /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM        /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);           /* send high byte of address */
#endif
EE_WriteByte(addr >> 8);                /* send next byte of address */
EE_WriteByte(addr);                     /* send low byte of address */
for (ii = 0; ii < n; ii++)
{
    EE_WriteByte(buffer[ii]);           /* send data to be written */
}
EE_Off();                               /* turn off EEPROM */
...
```

4.2.3.5   Serial EEPROM Read Data Routine

```
...
EE_WriteByte(READ_EE_OPCODE);           /* opcode to write bytes */
#ifdef THREE_BYTE_ADDRESS_EEPROM        /* three-byte addressing EEPROM? */
    EE_WriteByte(addr >> 16);           /* send high byte of address */
#endif
EE_WriteByte(addr >> 8);                /* send next byte of address */
EE_WriteByte(addr);                     /* send low byte of address */
for (ii = 0; ii < n; ii++)
{
    buffer[ii] = EE_ReadByte(buffer[ii]);   /* store read data in buffer */
}
EE_Off();                               /* turn off EEPROM */
```

4.3   Local Configuration Space Serial EEPROM Interface (Micro-Wire-Compatible Interface)

This section describes **LCS** serial EEPROM use within the PEX 8311. The PEX 8311 Local Bus supports 2K- or 4K-bit serial EEPROMs. The PEX 8311 requires serial EEPROMs that support sequential reads.

The PEX 8311 supports two serial EEPROM load lengths – long serial EEPROM and extra long serial EEPROM (refer to Figure 4-1):

- **Long Load mode** – Default. The PEX 8311 Local Bus loads 34, 16-bit words from the serial EEPROM when the *Extra Long Load from Serial EEPROM* bit is cleared (**LCS_LBRD0**[25]=0)

- **Extra Long Load mode** – The PEX 8311 Local Bus loads 50, 16-bit words from the serial EEPROM when the *Extra Long Load from Serial EEPROM* bit is set (**LCS_LBRD0**[25]=1)

The serial EEPROM is read or written from the PCI Express interface or Local Bus, through the **LCS Serial EEPROM Control** register bits (**LCS_CNTRL**[31, 27:24]) or VPD capability on the Local Configuration Space.

The 3.3V serial EEPROM clock (EESK) is internally derived. The PEX 8311 generates the serial EEPROM clock by internally dividing CLKIN by 268. When CLKIN is 66 MHz (default frequency of CLKOUT), EESK is 248.7 kHz.

During Local Bus serial EEPROM loading, the PEX 8311 accepts Direct Slave accesses; however, until the *Local Init Status* bit is set, Completion responses can take longer than usual (in the case of a Read access). Local Processor accesses are delayed by holding READY# (C or J mode) or TA# (M mode) de-asserted.

Figure 4-1.   Serial EEPROM Memory Map
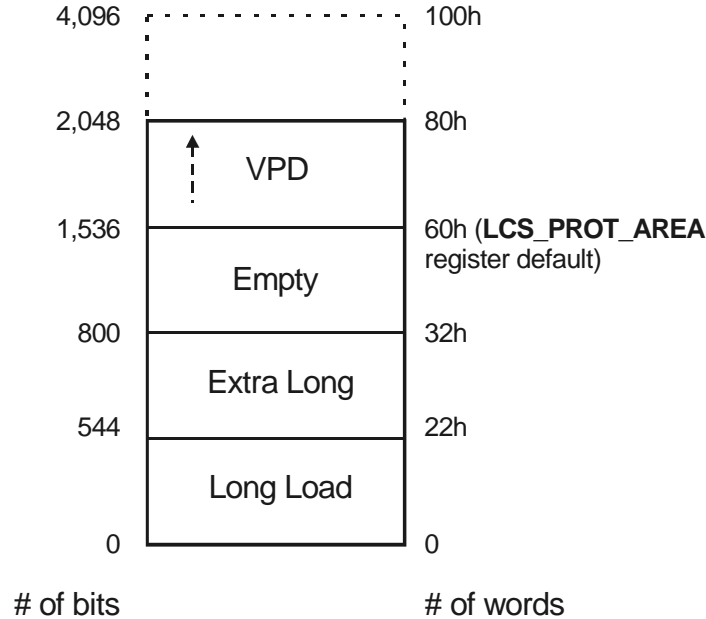
4.3.1   PEX 8311 Initialization from Serial EEPROM

After reset, the PEX 8311 attempts to read the serial EEPROM to determine its presence. A first-returned bit cleared to 0 indicates a serial EEPROM is present. The first word is then checked to verify that the serial EEPROM is programmed. If the first word (16 bits) is all ones (1), a blank serial EEPROM is present. If the first word (16 bits) is all zeros (0), no serial EEPROM is present. For both conditions, the PEX 8311 reverts to the default values. (Refer to Table 4-3.) The *Serial EEPROM Present* bit is set (**LCS_CNTRL**[28]=1) when the serial EEPROM is detected as present and is programmed or blank.

If a valid, non-blank serial EEPROM is present, the **LCS** registers are programmed with the contents of the serial EEPROM, as defined in Table 4-3. Following serial EEPROM load, a Local processor can perform additional register initialization by way of CCS# register accesses. The serial EEPROM is reloaded by setting the *Reload Configuration Registers* bit (**LCS_CNTRL**[29]=1).

The PEX 8311 internally Retries all PCI Express-initiated accesses, or allows Master Aborts until the *Local Init Status* bit is set to "done" (**LCS_LMISC1**[2]=1). To enable access from the PCI Express interface after **LCS** registers are loaded from the serial EEPROM, **LCS_LMISC1**[2] must be set to 1 by the serial EEPROM or a CCS# Write by a Local Master.

Note: All PCI Express accesses are granted after the Local Init Status bit is set.

Table 4-3. Serial EEPROM Guidelines

Local Processor	Local Bus Serial EEPROM	System Boot Condition	Device which Sets LCS_LMISC1[2]
None	None	The PEX 8311 Local Bus uses default values. The EEDI/EEDO ball must be pulled Low – a 1KΩ resistor is required (rather than pulled High, which is typically executed for this ball). If the PEX 8311 Local Bus detects all zeros (0), it reverts to default values and sets the *Local Init Status* bit (**LCS_LMISC1**[2]=1) by itself.	PEX 8311
None	Programmed	Boot with serial EEPROM values. The *Local Init Status* bit must be set (**LCS_LMISC1**[2]=1) by the serial EEPROM.	Serial EEPROM
None	Blank	The PEX 8311 Local Bus detects a blank device, reverts to default values, and sets the *Local Init Status* bit (**LCS_LMISC1**[2]=1) by itself.	PEX 8311
Present	None	The Local processor programs the PEX 8311 registers, then sets the *Local Init Status* bit (**LCS_LMISC1**[2]=1). A 1KΩ or greater value pull-up resistor or EEDI/EEDO is recommended, but not required. The EEDI/EEDO ball has an internal pull-up resistor. [Refer to Table 2-4, "Balls with Internal Resistors (to VDD3.3)."] *Note: Certain systems can avoid configuring devices that do not respond with successful completion or completion with CRS set. In this case, the Root Complex times out after completion. In addition, certain systems can hang when Direct Slave reads and writes take overly long (during initialization, the Root Complex also performs Direct Slave accesses). The value of the Direct Slave Retry Delay Clocks in the Local Configuration space (LCS_LBRD0[31:28]) can resolve this.*	Local CPU
Present	Programmed	Load serial EEPROM; however, the Local processor cannot reprogram the PEX 8311. Either the Local processor or the serial EEPROM must set the *Local Init Status* bit (**LCS_LMISC1**[2]=1).	Serial EEPROM or Local CPU
Present	Blank	The PEX 8311 detects a blank serial EEPROM and reverts to default values. *Notes: In certain systems, the Local processor can be overly late to re-configure the PEX 8311 registers before the BIOS configures them. The serial EEPROM is programmed through the PEX 8311 after the system boots in this condition.*	PEX 8311

Note: When the serial EEPROM is missing and a Local processor is present with blank Flash, the condition None/None (as defined in Table 4-3) applies, until the processor's Flash is programmed.

A pull-up resistor is recommended for all above conditions except None/None.

4.3.2   Local Initialization and PCI Express Interface Behavior

The PEX 8311 issues an internal Retry or allows an internal Master Abort to generate to the internal PCI Express interface block, depending on the USERi strapping option during the PEX 8311 RESET condition until the *Local Init Status* bit is set (**LCS_LMISC1**[2]=1). This bit is programmed in three ways:

1. By the Local processor, through the Local Configuration register.

2. By the serial EEPROM, during a serial EEPROM load, when the Local processor does not set this bit.

3. If the Local processor and the serial EEPROM are missing, or the serial EEPROM is blank (with or without a Local processor), the PEX 8311 uses defaults and sets this bit. (Refer to Table 4-3.)

To avoid the PEX 8311 generating Unsupported Request (UR) to the Root Complex Configuration Register accesses to the Local Configuration space during serial EEPROM loading, the USERi ball must be pulled High. The PEX 8311 determines the behavior, as follows:

• The USERi ball is sampled at the rising edge of PERST# to determine the selected response mode during Local Bus initialization.

• If USERi is Low (through an external 1KΩ pull-down resistor), the PEX 8311 responds with UR Completions to the PCI Express Type 1 accesses to the PEX 8311 Local Configuration space until Local Bus initialization is complete.

• If USERi is High (through an external 1KΩ to 4.7KΩ pull-up resistor), the PEX 8311 responds to PCI Express Type 1 accesses to the Local Configuration space, with either Completion with CRS set or Successful Completion with data after Local Bus initialization is complete. This depends on the **PECS PCI Express Device Control** register *Bridge Configuration Retry Enable* bit being set (**PECS_DEVCTL**[15]=1). Local Bus initialization is complete when the *Local Init Status* bit is set (**LCS_LMISC1**[2]=1).

During run time, USERi is used as a general-purpose input. (Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior.")

4.3.2.1   Long Serial EEPROM Load

If the Extra Long Load from Serial EEPROM bit is *not* set (**LCS_LBRD0**[25]=0), the registers defined in Table 4-4 are loaded from the serial EEPROM after a reset is de-asserted. The serial EEPROM is organized in words (16 bits). The PEX 8311 first loads the Most Significant Word bits (MSW[31:16]), starting from the Most Significant Bit (MSB[31]). The PEX 8311 then loads the Least Significant Word bits (LSW[15:0]), starting again from the Most Significant Bit (MSB[15]). Therefore, the PEX 8311 loads the Device ID, Vendor ID, Class Code, and so forth.

The serial EEPROM values are programmed using a serial EEPROM programmer. The values can also be programmed using the PEX 8311 VPD function [refer to Chapter 17, "Vital Product Data (VPD)"] or through the **LCS Serial EEPROM Control** register (**LCS_CNTRL**).

Using the **LCS_CNTRL** register or VPD, the designer can perform reads and writes from/to the serial EEPROM, 32 bits at a time. Program serial EEPROM values in the order defined in Table 4-4. The 34, 16-bit words defined in the table are stored sequentially in the serial EEPROM.

4.3.2.2   Extra Long Serial EEPROM Load

If the *Extra Long Load from Serial EEPROM* bit is set (**LCS_LBRD0**[25]=1), the registers defined in Table 4-4 and Table 4-5 are loaded from the serial EEPROM, with the Table 4-4 values loaded first.

Program serial EEPROM values in the order defined in Table 4-5. Store the 50, 16-bit words defined in Table 4-4 and Table 4-5 sequentially in the serial EEPROM, with the Table 4-4 values loaded first.

Table 4-4.   Long Serial EEPROM Load Registers

Serial EEPROM Byte Offset	Description	Register Bits Affected
0h	PCI Device ID	**LCS_PCIIDR**[31:16]
2h	PCI Vendor ID	**LCS_PCIIDR**[15:0]
4h	PCI Class Code	**LCS_PCICCR**[23:8]
6h	PCI Class Code / Revision ID	**LCS_PCICCR**[7:0] / **LCS_PCIREV**[7:0]
8h	PCI Maximum Latency / PCI Minimum Grant	**LCS_PCIMLR**[7:0] / **LCS_PCIMGR**[7:0]
Ah	Internal PCI Wire Interrupt / Internal PCI Interrupt Line	**LCS_PCIIPR**[7:0] / **LCS_PCIILR**[7:0]
Ch	MSW of Mailbox 0 (User-Defined)	**LCS_MBOX0**[31:16]
Eh	LSW of Mailbox 0 (User-Defined)	**LCS_MBOX0**[15:0]
10h	MSW of Mailbox 1 (User-Defined)	**LCS_MBOX1**[31:16]
12h	LSW of Mailbox 1 (User-Defined)	**LCS_MBOX1**[15:0]
14h	MSW of Direct Slave Local Address Space 0 Range	**LCS_LAS0RR**[31:16]
16h	LSW of Direct Slave Local Address Space 0 Range	**LCS_LAS0RR**[15:0]
18h	MSW of Direct Slave Local Address Space 0 Local Base Address (Remap)	**LCS_LAS0BA**[31:16]
1Ah	LSW of Direct Slave Local Address Space 0 Local Base Address (Remap)	**LCS_LAS0BA**[15:2, 0], *Reserved* [1]
1Ch	MSW of Mode/DMA Arbitration	**LCS_MARBR**[31,29:16] or **LCS_DMAARB**[31, 29:16], *Reserved* [30]
1Eh	LSW of Mode/DMA Arbitration	**LCS_MARBR**[15:0] or **LCS_DMAARB**[15:0]
20h	Local Miscellaneous Control 2 / Serial EEPROM Write-Protected Address Boundary	**LCS_LMISC2**[5:0], *Reserved* [7:6] / **LCS_PROT_AREA**[6:0], *Reserved* [7]
22h	Local Miscellaneous Control 1 / Local Bus Big/Little Endian Descriptor	**LCS_LMISC1**[7:0] / **LCS_BIGEND**[7:0]
24h	MSW of Direct Slave Expansion ROM Range	**LCS_EROMRR**[31:16]
26h	LSW of Direct Slave Expansion ROM Range	**LCS_EROMRR**[15:11, 0], *Reserved* [10:1]
28h	MSW of Direct Slave Expansion ROM Local Base Address (Remap) (all modes) and BREQo Control (C and J modes only)	**LCS_EROMBA**[31:16]
2Ah	LSW of Direct Slave Expansion ROM Local Base Address (Remap) (all modes) and BREQo Control (C and J modes only)	**LCS_EROMBA**[15:11, 5:0], *Reserved* [10:6]

Table 4-4.   Long Serial EEPROM Load Registers (Cont.)

Serial EEPROM Byte Offset	Description	Register Bits Affected
2Ch	MSW of Local Address Space 0/Expansion ROM Bus Region Descriptor	**LCS_LBRD0**[31:16]
2Eh	LSW of Local Address Space 0/Expansion ROM Bus Region Descriptor	**LCS_LBRD0**[15:0]
30h	MSW of Local Range for Direct Master-to-PCI Express	**LCS_DMRR**[31:16]
32h	LSW of Local Range for Direct Master-to-PCI Express (*Reserved*)	**LCS_DMRR**[15:0]
34h	MSW of Local Base Address for Direct Master-to-PCI Express Memory	**LCS_DMLBAM**[31:16]
36h	LSW of Local Base Address for Direct Master-to-PCI Express Memory (*Reserved*)	**LCS_DMLBAM**[15:0]
38h	MSW of Local Bus Address for Direct Master-to-PCI Express I/O Configuration	**LCS_DMLBAI**[31:16]
3Ah	LSW of Local Bus Address for Direct Master-to-PCI Express I/O Configuration (*Reserved*)	**LCS_DMLBAI**[15:0]
3Ch	MSW of PCI Express Base Address (Remap) for Direct Master-to-PCI Express Memory	**LCS_DMPBAM**[31:16]
3Eh	LSW of PCI Express Base Address (Remap) for Direct Master-to-PCI Express Memory	**LCS_DMPBAM**[15:0]
40h	MSW of PCI Configuration Address for Direct Master-to-PCI Express I/O Configuration	**LCS_DMCFGA**[31, 23:16], *Reserved* [30:24]
42h	LSW of PCI Configuration Address for Direct Master-to-PCI Express I/O Configuration	**LCS_DMCFGA**[15:0]

Table 4-5.   Extra Long Serial EEPROM Load Registers

Serial EEPROM Byte Offset	Description	Register Bits Affected
44h	PCI Subsystem ID	**LCS_PCISID**[15:0]
46h	PCI Subsystem Vendor ID	**LCS_PCISVID**[15:0]
48h	MSW of Direct Slave Local Address Space 1 Range (1 MB)	**LCS_LAS1RR**[31:16]
4Ah	LSW of Direct Slave Local Address Space 1 Range (1 MB)	**LCS_LAS1RR**[15:0]
4Ch	MSW of Direct Slave Local Address Space 1 Local Base Address (Remap)	**LCS_LAS1BA**[31:16]
4Eh	LSW of Direct Slave Local Address Space 1 Local Base Address (Remap)	**LCS_LAS1BA**[15:2, 0], ***Reserved*** [1]
50h	MSW of Local Address Space 1 Bus Region Descriptor	**LCS_LBRD1**[31:16]
52h	LSW of Local Address Space 1 Bus Region Descriptor (***Reserved***)	**LCS_LBRD1**[15:0]
54h	Hot Swap Control/Status (***Reserved***)	***Reserved***
56h	Hot Swap Next Capability Pointer / Hot Swap Control (***Reserved***)	**LCS_HS_NEXT**[7:0] / **LCS_HS_CNTL**[7:0]
58h	***Reserved***	***Reserved***
5Ah	Internal Arbiter Control	**LCS_PCIARB**[3:0], ***Reserved*** [15:4]
5Ch	Power Management Capabilities	**LCS_PMC**[15:9, 2:0]
5Eh	Power Management Next Capability Pointer (***Reserved***) / Power Management Capability ID (***Reserved***)	***Reserved***
60h	Power Management Data / PMCSR Bridge Support Extension (***Reserved***)	**LCS_PMDATA**[7:0] / ***Reserved***
62h	Power Management Control/Status	**LCS_PMCSR**[14:8]

4.3.3   Serial EEPROM Access

The **LCS_CNTRL**[31, 27:24] register bits are programmed to control the EESK, EECS, and EEDI/EEDO settings. Bit 24 is used to generate EESK (clock), bit 25 controls the Chip Select, bit 26 controls the EEDI output logic level, and bit 31 enables the EEDO Input buffer. Bit 27, when read, returns the value of EEDI.

Setting **LCS_CNTRL**[31, 25:24] to 1 causes the output to go High. A pull-up resistor is required on the EEDI/EEDO ball for the ball to go High when bit 31 is set. When reading the EEPROM, **LCS_CNTRL**[31] must be set to 1.

To perform the read, the basic approach is to set the EECS and EEDO bits (**LCS_CNTRL**[25, 31]=11b, respectively) to the desired level and then toggle EESK High and Low until completed. *For example*, reading the serial EEPROM at Location 0 involves the following steps:

1. Clear the *EECS*, *EEDI*, *EEDO*, and *EESK Input Enable* bits.

2. Set EECS High.

3. Toggle EESK High, then Low.

4. Set the EEDI bit High (Start bit).

5. Toggle EESK High, then Low.

6. Repeat step 5.

7. Clear EEDI.

8. Toggle EESK High, then Low.

9. Toggle EESK High, then Low 8 times (clock in Serial EEPROM Address 0).

10. Set EEDO Input Enable to 1 (**LCS_CNTRL**[31]=1) to float the EEDO input for reading.

11. Toggle EESK High, then Low 16 times (clock in 1 word from serial EEPROM).

12. After each clock pulse, read bit 27 and save.

13. Clear the *EECS* bit.

14. Toggle EESK High, then Low. The read is complete.

The serial EEPROM uses word addressing with 8-bit sequential address values. Due to PEX 8311 Local Bus EEPROM interface EEDI/EEDO signal multiplexing and to avoid contention between the least-significant Address bit and the serial EEPROM's Start bit, Read access to an odd-numbered Word address (bit 0 is set) must be performed by using the even-numbered Word address (bit 0 is cleared), along with the serial EEPROM's sequential read functionality, clocking in 32 (or more) Data bits while keeping EECS continually asserted during the Read access.

During a serial EEPROM Write operation, the serial EEPROM's programming cycle is triggered by EECS de-assertion. When EECS is re-asserted, the serial EEPROM drives its Ready status on its DO pin connected to the PEX 8311 EEDI/EEDO ball. (Refer to the manufacturer's data sheet for Ready functionality.) Ready status (DO=1) indicates internal Write Completion. If the PEX 8311 is driving the EEDI (EEDI/EEDO ball) signal to a logic Low when EECS is re-asserted after a Write operation, contention exists on the multiplexed EEDI/EEDO bus. The contention is released when Ready functionality is cleared by clocking in a *Start* bit (causing the serial EEPROM to float its DO output). To remove contention following a Write cycle, re-assert EECS after waiting the Minimum Chip Select Low Time, and, after Ready status is High or the Write Cycle Time expires (typically 10 to 15 μs), set the EEDI output to logic High, then clock the *Start* bit into the serial EEPROM by toggling EESK High, then Low. This Start bit is used as part of the next serial EEPROM instruction, or, the cycle is terminated by de-asserting EECS. Contention can also be avoided by setting the EEDI output High after clocking out the LSB of the data after each Write sequence.

The serial EEPROM can also be read or written, using the VPD function. [Refer to Chapter 17, "Vital Product Data (VPD)."]

4.3.4   Serial EEPROM Initialization Timing Diagram

Figure 4-2.   Serial EEPROM Initialization Timing Diagram
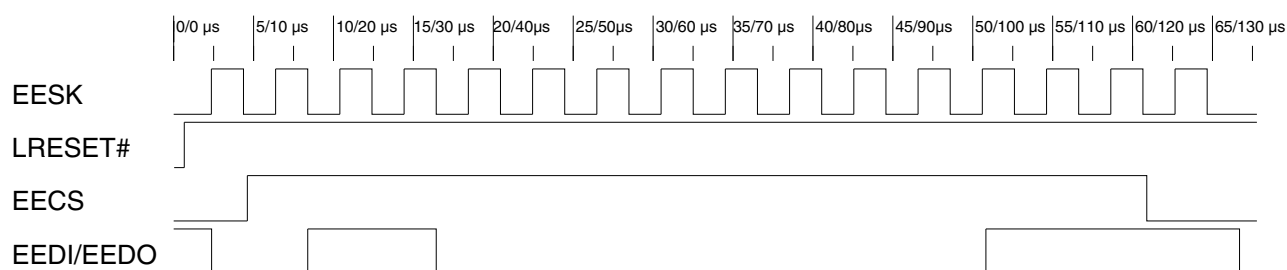
> *Notes:*   *Time scales provided are based on a 66-MHz internal clock.*
>
> *The EEDI/EEDO signal is not sampled by the serial EEPROM until after EECS is asserted.*
>
> *Upon LRESET# de-assertion, the PEX 8311 issues a Read command of Serial EEPROM Address 0.*
>
> *For this timing diagram, no serial EEPROM is present; however, the Local processor is present to perform initialization. Therefore, the PEX 8311 does not detect a serial EEPROM Start bit because the EEDI/EEDO signal is sampled High (due to the internal pull-up resistor). Thereafter, the EESK, EECS and EEDI/EEDO signal balls are driven to 0.*
>
> *When the PEX 8311 detects a serial EEPROM Start bit and the first 16 bits (which correspond to **LCS_PCIIDR**[31:16]) are not all zeros (0) or all ones (1), the PEX 8311 continues to assert EECS and generate the serial EEPROM clock (EESK) to load its registers with the programmed serial EEPROM values.*
>
> *The first bit downloaded after the Start bit is **LCS_PCIIDR**[31].*

Figure 4-3 illustrates the approximate length of time required to detect the Start bit, and length of time required for Long or Extra Long Serial EEPROM Load. While the PEX 8311 is downloading serial EEPROM data, PCI accesses to the PEX 8311 are Retried and Local Master accesses are accepted; however, the accesses do not complete (C or J mode – READY# is de-asserted; M mode – TA# is de-asserted) until the serial EEPROM download completes.

Figure 4-3.   Serial EEPROM Timeline
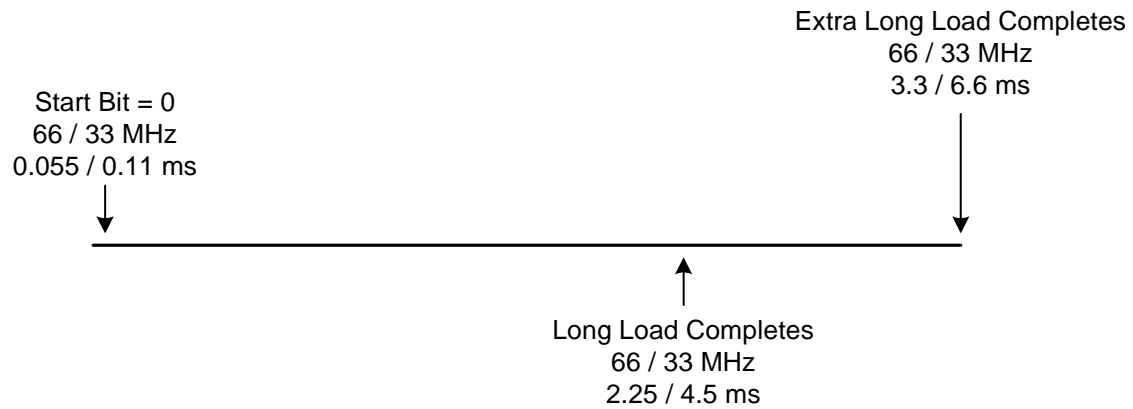
Chapter 5   Local Bus Operation

5.1   Local Bus Cycles

The PEX 8311 interfaces the PCI Express interface to three Local Bus types, as defined in Table 5-1. It operates in one of three modes – M, C, or J, selected through the MODE[1:0] balls – corresponding to the three bus types.

In M mode, the PEX 8311 provides a direct connection to the MPC850 or MPC860 address and data lines, regardless of the PEX 8311 Big or Little Endian modes.

Table 5-1.   MODE Ball-to-Bus Mode Cross-Reference

MODE1	MODE0	Bus Mode	Bus Type
0	0	C	Intel/Generic, 32-bit non-multiplexed
0	1	J	Intel/Generic, 32-bit multiplexed
1	0	*Reserved*	–
1	1	M	Motorola, 32-bit non-multiplexed

5.1.1   Local Bus Arbitration and BREQi – C and J Modes

The PEX 8311 asserts LHOLD to request the Local Bus for a Direct Slave or DMA transfer. The PEX 8311 owns and becomes the Local Bus Master when both LHOLD and LHOLDA are asserted. As the Local Bus Master, the PEX 8311 responds to BREQi assertion to relinquish Local Bus ownership during Direct Slave or DMA transfers when either of the following conditions are true:

- BREQi is asserted and enabled (**LCS_MARBR**[18]=1)
- Gating is enabled and the Local Bus Latency Timer is enabled and expires (**LCS_MARBR**[27, 16, 7:0])

Before releasing the Local Bus, the PEX 8311 attempts to transfer up to a total of three additional Dwords of data. This includes the last transfer with BLAST# asserted. The actual number of additional transfers depends upon the Local Bus data width and address when BREQi is asserted. The minimum assertion duration of the BREQi signal is one Local Bus Clock cycle. Typically, Local Bus logic asserts BREQi and holds it asserted until either BLAST# is asserted (BLAST#=0) or LHOLD is de-asserted (LHOLD=0).

When the PEX 8311 releases the Local Bus, the external Local Bus Arbiter can grant the Local Bus to another Master. If the PEX 8311 must complete the disconnected transfer, it requests the Local Bus by re-asserting LHOLD upon detection of LHOLDA de-assertion and the Local Bus Pause Timer being zero (0), when enabled.

LHOLDA must be asserted only in response to an LHOLD request from the PEX 8311. If LHOLDA is asserted before LHOLD is asserted, the Local Bus locks. For applications where the PEX 8311 is the only Local Bus Master, tie LHOLD to LHOLDA (pull down with a 4KΩ to 10KΩ resistor) to form a simple arbiter.

Note: *The Local Bus Pause Timer applies only to DMA operation. It does not apply to Direct Slave operations.*

5.1.1.1   Local Bus Arbitration Timing Diagram – C and J Modes

Figure 5-1.   Local Bus Arbitration (LHOLD and LHOLDA) Timing Diagram – C and J Modes
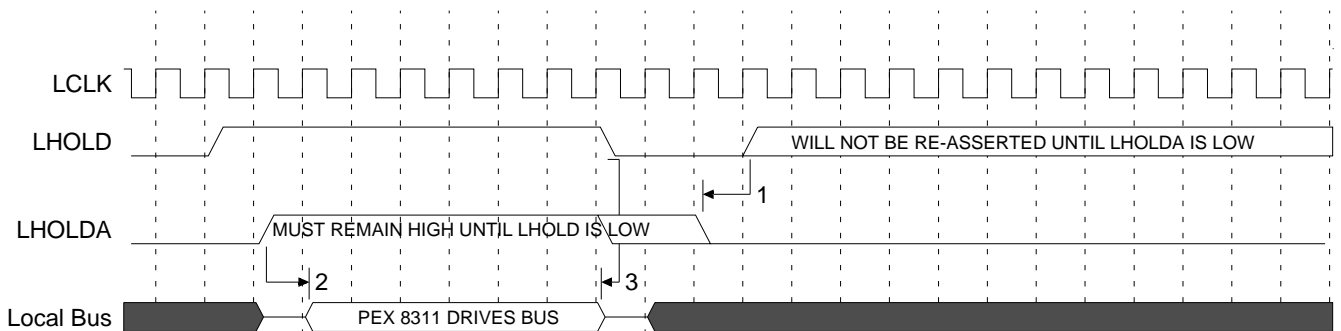
Notes: *In response to the PEX 8311 assertion of LHOLD, the external Local Bus Arbiter asserts LHOLDA to grant the Local Bus to the PEX 8311. In Figure 5-1, the Local Bus Arbiter asserts LHOLDA immediately upon detection of LHOLD assertion; however, the Local Bus Arbiter has the option, when necessary, to assert LHOLDA significantly later.*

Figure 5-1 was created using the Timing Designer tool. It is accurate and adheres to its specified protocol(s). This diagram illustrates transfers and signal transitions; however, it should not be relied upon to exactly indicate, on a clock-for-clock basis, wherein PEX 8311-driven signal transitions will occur.

5.1.2   Local Bus Arbitration – M Mode

The PEX 8311 asserts BR# to request the Local Bus for a Direct Slave or DMA transfer, then waits for the external Local Bus Arbiter to assert BG#. Upon receiving BG#, the PEX 8311 waits for BB# to de-assert (to ensure that no other Master is driving the bus) before it asserts BB# (on the next rising edge of the Local clock) to become the Local Bus Master and drive the bus. As the Local Bus Master, the PEX 8311 continues to assert BB# until the transaction is complete or the Local Bus Latency Timer (**LCS_MARBR**[7:0]), if enabled (**LCS_MARBR**[16]=1), expires (whichever occurs first).

Note: *The Local Bus Pause Timer applies only to DMA operation. It does **not** apply*
          to Direct Slave operation.

5.1.2.1   Local Bus Arbitration Timing Diagram – M Mode

Figure 5-2.   Local Bus Arbitration (BR#, BG#, and BB#) – M Mode
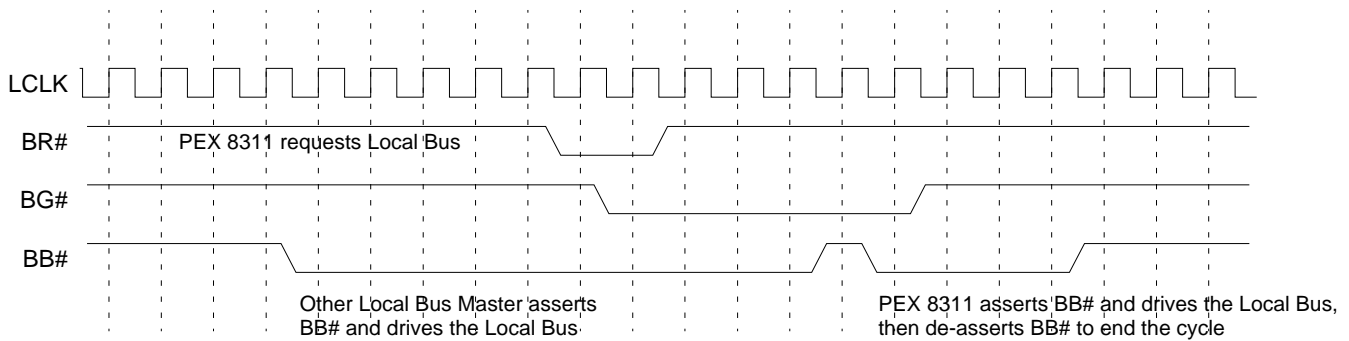
Note: *Timing Diagram 5-2 was created using the Timing Designer tool. It is accurate and adheres to its specified*
          *protocol(s). This diagram illustrates transfers and signal transitions; however, it is **not** to be relied upon to exactly*
          show, on a clock-for-clock basis, where PEX 8311-driven signal transitions occur.

5.2 Big Endian/Little Endian

5.2.1 PCI Express Data Bits Mapping onto Local Bus

PCI Express is a serial interface; therefore, for clarity, the description is provided from the perspective of data being de-packetized and assembled into a Dword of payload data. Table 5-7 through Table 5-6 clarify PEX 8311 signal mapping between the data from the PCI Express interface and Local Bus during Big/Little Endian conversion.

Notes:

1. *In each Local Bus ball entry, **n-m** denotes that that row's PCI AD[n] maps to Local Bus ball **m** during Local Bus cycle **n** that results from the PCI Express cycle (PCI Express-to-Local Bus transfers) or in the PCI Express cycle (Local-to-PCI Express transfers). Examples follow. (Refer to Table 5-2 for Ball A, B, C, and D for C, J, and M modes.)*

   Low Byte Lane Tables
   In the Low Byte Lane tables, the shaded entry Local Bus ball "A" for PCI Express Dword format data ball AD21 during 16-bit Little Endian Local Bus transfers denotes that during a PCI Express-to-Local Bus transfer, the value of PCI Express Dword format data ball AD21 during each PCI Express transfer occurs on Local Bus ball "B" of the second resulting 16-bit Local Bus transfer. During a Local-to-PCI Express transfer, it denotes that the value of PCI Express Dword format data ball AD21 results from the value of Local Bus ball "B" during the second 16-bit Local Bus transfer.

   High Byte Lane Tables
   In the Low Byte Lane tables, the shaded entry Local Bus ball "C" for PCI Express Dword format data ball AD21 during 16-bit Little Endian Local Bus transfers denotes that during a PCI Express-to-Local Bus transfer, the value of PCI Express Dword format data ball AD21 during each PCI Express transfer occurs on Local Bus ball "D" of the second resulting 16-bit Local Bus transfer. During a Local-to-PCI Express transfer, it denotes that the value of PCI Express Dword format data ball AD21 results from the value of Local Bus ball "D" during the second 16-bit Local Bus transfer.

2. *Mappings occur only during Data phases. Addresses always map directly, as indicated in the 32-bit Little Endian column after the address translation specified in the Configuration registers is performed.*

3. *Big/Little Endian modes are selected by register bits and ball signals, depending on the Data phase type (Direct Master Read/Write, Direct Slave Read/Write, DMA PCI Express-to-Local Bus/Local Bus-to-PCI Express, and Configuration register read/write). (For further details, refer to the LCS_BIGEND register, and the BIGEND# ball description).*

Table 5-2.   Low/High Byte Lane Local Bus Ball Mapping for Note 1

Local Bus Mode	Low Byte Lane			High Byte Lane		
	Table	A	B	Table	C	D
C	Table 5-3	2-LD10	LD10	Table 5-4	2-LD21	LD21
J	Table 5-5	2-LAD5	LAD5	Table 5-6	2-LAD21	LAD21
M	Table 5-7	2-LD26	LD26	Table 5-8	2-LD10	LD10

Table 5-3.   PCI Express Dword Format Bus Data Bits Mapping onto Local Bus C Mode – Low Byte Lane

PCI Express Dword Format Bus (Internal AD)	C Mode Local Bus Ball Byte Lane Mode = 0 (LCS_BIGEND[4]=0)					
	Little Endian			Big Endian		
	32-Bit	**16-Bit**	**8-Bit**	**32-Bit**	**16-Bit**	**8-Bit**
AD0	1-LD0	1-LD0	1-LD0	1-LD24	1-LD8	1-LD0
AD1	1-LD1	1-LD1	1-LD1	1-LD25	1-LD9	1-LD1
AD2	1-LD2	1-LD2	1-LD2	1-LD26	1-LD10	1-LD2
AD3	1-LD3	1-LD3	1-LD3	1-LD27	1-LD11	1-LD3
AD4	1-LD4	1-LD4	1-LD4	1-LD28	1-LD12	1-LD4
AD5	1-LD5	1-LD5	1-LD5	1-LD29	1-LD13	1-LD5
AD6	1-LD6	1-LD6	1-LD6	1-LD30	1-LD14	1-LD6
AD7	1-LD7	1-LD7	1-LD7	1-LD31	1-LD15	1-LD7
AD8	1-LD8	1-LD8	2-LD0	1-LD16	1-LD0	2-LD0
AD9	1-LD9	1-LD9	2-LD1	1-LD17	1-LD1	2-LD1
AD10	1-LD10	1-LD10	2-LD2	1-LD18	1-LD2	2-LD2
AD11	1-LD11	1-LD11	2-LD3	1-LD19	1-LD3	2-LD3
AD12	1-LD12	1-LD12	2-LD4	1-LD20	1-LD4	2-LD4
AD13	1-LD13	1-LD13	2-LD5	1-LD21	1-LD5	2-LD5
AD14	1-LD14	1-LD14	2-LD6	1-LD22	1-LD6	2-LD6
AD15	1-LD15	1-LD15	2-LD7	1-LD23	1-LD7	2-LD7
AD16	1-LD16	2-LD0	3-LD0	1-LD8	2-LD8	3-LD0
AD17	1-LD17	2-LD1	3-LD1	1-LD9	2-LD9	3-LD1
AD18	1-LD18	2-LD2	3-LD2	1-LD10	2-LD10	3-LD2
AD19	1-LD19	2-LD3	3-LD3	1-LD11	2-LD11	3-LD3
AD20	1-LD20	2-LD4	3-LD4	1-LD12	2-LD12	3-LD4
AD21	1-LD21	2-LD5	3-LD5	1-LD13	2-LD13	3-LD5
AD22	1-LD22	2-LD6	3-LD6	1-LD14	2-LD14	3-LD6
AD23	1-LD23	2-LD7	3-LD7	1-LD15	2-LD15	3-LD7
AD24	1-LD24	2-LD8	4-LD0	1-LD0	2-LD0	4-LD0
AD25	1-LD25	2-LD9	4-LD1	1-LD1	2-LD1	4-LD1
AD26	1-LD26	2-LD10	4-LD2	1-LD2	2-LD2	4-LD2
AD27	1-LD27	2-LD11	4-LD3	1-LD3	2-LD3	4-LD3
AD28	1-LD28	2-LD12	4-LD4	1-LD4	2-LD4	4-LD4
AD29	1-LD29	2-LD13	4-LD5	1-LD5	2-LD5	4-LD5
AD30	1-LD30	2-LD14	4-LD6	1-LD6	2-LD6	4-LD6
AD31	1-LD31	2-LD15	4-LD7	1-LD7	2-LD7	4-LD7

**Table 5-4. PCI Express Dword Format Bus Data Bits Mapping onto Local Bus C Mode –
High Byte Lane**

PCI Express Dword Format Bus (Internal AD)	C Mode Local Bus Ball Byte Lane Mode = 1 (LCS_BIGEND[4]=1)					
	Little Endian			Big Endian		
	32-Bit	**16-Bit**	**8-Bit**	**32-Bit**	**16-Bit**	**8-Bit**
AD0	1-LD0	1-LD16	1-LD24	1-LD24	1-LD24	1-LD24
AD1	1-LD1	1-LD17	1-LD25	1-LD25	1-LD25	1-LD25
AD2	1-LD2	1-LD18	1-LD26	1-LD26	1-LD26	1-LD26
AD3	1-LD3	1-LD19	1-LD27	1-LD27	1-LD27	1-LD27
AD4	1-LD4	1-LD20	1-LD28	1-LD28	1-LD28	1-LD28
AD5	1-LD5	1-LD21	1-LD29	1-LD29	1-LD29	1-LD29
AD6	1-LD6	1-LD22	1-LD30	1-LD30	1-LD30	1-LD30
AD7	1-LD7	1-LD23	1-LD31	1-LD31	1-LD31	1-LD31
AD8	1-LD8	1-LD24	2-LD24	1-LD16	1-LD16	2-LD24
AD9	1-LD9	1-LD25	2-LD25	1-LD17	1-LD17	2-LD25
AD10	1-LD10	1-LD26	2-LD26	1-LD18	1-LD18	2-LD26
AD11	1-LD11	1-LD27	2-LD27	1-LD19	1-LD19	2-LD27
AD12	1-LD12	1-LD28	2-LD28	1-LD20	1-LD20	2-LD28
AD13	1-LD13	1-LD29	2-LD29	1-LD21	1-LD21	2-LD29
AD14	1-LD14	1-LD30	2-LD30	1-LD22	1-LD22	2-LD30
AD15	1-LD15	1-LD31	2-LD31	1-LD23	1-LD23	2-LD31
AD16	1-LD16	2-LD16	3-LD24	1-LD8	2-LD24	3-LD24
AD17	1-LD17	2-LD17	3-LD25	1-LD9	2-LD25	3-LD25
AD18	1-LD18	2-LD18	3-LD26	1-LD10	2-LD26	3-LD26
AD19	1-LD19	2-LD19	3-LD27	1-LD11	2-LD27	3-LD27
AD20	1-LD20	2-LD20	3-LD28	1-LD12	2-LD28	3-LD28
AD21	1-LD21	2-LD21	3-LD29	1-LD13	2-LD29	3-LD29
AD22	1-LD22	2-LD22	3-LD30	1-LD14	2-LD30	3-LD30
AD23	1-LD23	2-LD23	3-LD31	1-LD15	2-LD31	3-LD31
AD24	1-LD24	2-LD24	4-LD24	1-LD0	2-LD16	4-LD24
AD25	1-LD25	2-LD25	4-LD25	1-LD1	2-LD17	4-LD25
AD26	1-LD26	2-LD26	4-LD26	1-LD2	2-LD18	4-LD26
AD27	1-LD27	2-LD27	4-LD27	1-LD3	2-LD19	4-LD27
AD28	1-LD28	2-LD28	4-LD28	1-LD4	2-LD20	4-LD28
AD29	1-LD29	2-LD29	4-LD29	1-LD5	2-LD21	4-LD29
AD30	1-LD30	2-LD30	4-LD30	1-LD6	2-LD22	4-LD30
AD31	1-LD31	2-LD31	4-LD31	1-LD7	2-LD23	4-LD31

Table 5-5.   PCI Express Dword Format Bus Data Bits Mapping onto Local Bus J Mode – Low Byte Lane

PCI Express Dword Format Bus (Internal AD)	J Mode Local Bus Ball Byte Lane Mode = 0 (LCS_BIGEND[4]=0)					
	Little Endian			Big Endian		
	32-Bit	16-Bit	8-Bit	32-Bit	16-Bit	8-Bit
AD0	1-LAD0	1-LAD0	1-LAD0	1-LAD24	1-LAD8	1-LAD0
AD1	1-LAD1	1-LAD1	1-LAD1	1-LAD25	1-LAD9	1-LAD1
AD2	1-LAD2	1-LAD2	1-LAD2	1-LAD26	1-LAD10	1-LAD2
AD3	1-LAD3	1-LAD3	1-LAD3	1-LAD27	1-LAD11	1-LAD3
AD4	1-LAD4	1-LAD4	1-LAD4	1-LAD28	1-LAD12	1-LAD4
AD5	1-LAD5	1-LAD5	1-LAD5	1-LAD29	1-LAD13	1-LAD5
AD6	1-LAD6	1-LAD6	1-LAD6	1-LAD30	1-LAD14	1-LAD6
AD7	1-LAD7	1-LAD7	1-LAD7	1-LAD31	1-LAD15	1-LAD7
AD8	1-LAD8	1-LAD8	2-LAD0	1-LAD16	1-LAD0	2-LAD0
AD9	1-LAD9	1-LAD9	2-LAD1	1-LAD17	1-LAD1	2-LAD1
AD10	1-LAD10	1-LAD10	2-LAD2	1-LAD18	1-LAD2	2-LAD2
AD11	1-LAD11	1-LAD11	2-LAD3	1-LAD19	1-LAD3	2-LAD3
AD12	1-LAD12	1-LAD12	2-LAD4	1-LAD20	1-LAD4	2-LAD4
AD13	1-LAD13	1-LAD13	2-LAD5	1-LAD21	1-LAD5	2-LAD5
AD14	1-LAD14	1-LAD14	2-LAD6	1-LAD22	1-LAD6	2-LAD6
AD15	1-LAD15	1-LAD15	2-LAD7	1-LAD23	1-LAD7	2-LAD7
AD16	1-LAD16	2-LAD0	3-LAD0	1-LAD8	2-LAD8	3-LAD0
AD17	1-LAD17	2-LAD1	3-LAD1	1-LAD9	2-LAD9	3-LAD1
AD18	1-LAD18	2-LAD2	3-LAD2	1-LAD10	2-LAD10	3-LAD2
AD19	1-LAD19	2-LAD3	3-LAD3	1-LAD11	2-LAD11	3-LAD3
AD20	1-LAD20	2-LAD4	3-LAD4	1-LAD12	2-LAD12	3-LAD4
AD21	1-LAD21	2-LAD5	3-LAD5	1-LAD13	2-LAD13	3-LAD5
AD22	1-LAD22	2-LAD6	3-LAD6	1-LAD14	2-LAD14	3-LAD6
AD23	1-LAD23	2-LAD7	3-LAD7	1-LAD15	2-LAD15	3-LAD7
AD24	1-LAD24	2-LAD8	4-LAD0	1-LAD0	2-LAD0	4-LAD0
AD25	1-LAD25	2-LAD9	4-LAD1	1-LAD1	2-LAD1	4-LAD1
AD26	1-LAD26	2-LAD10	4-LAD2	1-LAD2	2-LAD2	4-LAD2
AD27	1-LAD27	2-LAD11	4-LAD3	1-LAD3	2-LAD3	4-LAD3
AD28	1-LAD28	2-LAD12	4-LAD4	1-LAD4	2-LAD4	4-LAD4
AD29	1-LAD29	2-LAD13	4-LAD5	1-LAD5	2-LAD5	4-LAD5
AD30	1-LAD30	2-LAD14	4-LAD6	1-LAD6	2-LAD6	4-LAD6
AD31	1-LAD31	2-LAD15	4-LAD7	1-LAD7	2-LAD7	4-LAD7

Table 5-6.　PCI Express Dword Format Bus Data Bits Mapping onto Local Bus J Mode – High Byte Lane

PCI Express Dword Format Bus (Internal AD)	J Mode Local Bus Ball Byte Lane Mode = 1 (LCS_BIGEND[4]=1)					
	Little Endian			Big Endian		
	32-Bit	16-Bit	8-Bit	32-Bit	16-Bit	8-Bit
AD0	1-LAD0	1-LAD16	1-LAD24	1-LAD24	1-LAD24	1-LAD24
AD1	1-LAD1	1-LAD17	1-LAD25	1-LAD25	1-LAD25	1-LAD25
AD2	1-LAD2	1-LAD18	1-LAD26	1-LAD26	1-LAD26	1-LAD26
AD3	1-LAD3	1-LAD19	1-LAD27	1-LAD27	1-LAD27	1-LAD27
AD4	1-LAD4	1-LAD20	1-LAD28	1-LAD28	1-LAD28	1-LAD28
AD5	1-LAD5	1-LAD21	1-LAD29	1-LAD29	1-LAD29	1-LAD29
AD6	1-LAD6	1-LAD22	1-LAD30	1-LAD30	1-LAD30	1-LAD30
AD7	1-LAD7	1-LAD23	1-LAD31	1-LAD31	1-LAD31	1-LAD31
AD8	1-LAD8	1-LAD24	2-LAD24	1-LAD16	1-LAD16	2-LAD24
AD9	1-LAD9	1-LAD25	2-LAD25	1-LAD17	1-LAD17	2-LAD25
AD10	1-LAD10	1-LAD26	2-LAD26	1-LAD18	1-LAD18	2-LAD26
AD11	1-LAD11	1-LAD27	2-LAD27	1-LAD19	1-LAD19	2-LAD27
AD12	1-LAD12	1-LAD28	2-LAD28	1-LAD20	1-LAD20	2-LAD28
AD13	1-LAD13	1-LAD29	2-LAD29	1-LAD21	1-LAD21	2-LAD29
AD14	1-LAD14	1-LAD30	2-LAD30	1-LAD22	1-LAD22	2-LAD30
AD15	1-LAD15	1-LAD31	2-LAD31	1-LAD23	1-LAD23	2-LAD31
AD16	1-LAD16	2-LAD16	3-LAD24	1-LAD8	2-LAD24	3-LAD24
AD17	1-LAD17	2-LAD17	3-LAD25	1-LAD9	2-LAD25	3-LAD25
AD18	1-LAD18	2-LAD18	3-LAD26	1-LAD10	2-LAD26	3-LAD26
AD19	1-LAD19	2-LAD19	3-LAD27	1-LAD11	2-LAD27	3-LAD27
AD20	1-LAD20	2-LAD20	3-LAD28	1-LAD12	2-LAD28	3-LAD28
AD21	1-LAD21	2-LAD21	3-LAD29	1-LAD13	2-LAD29	3-LAD29
AD22	1-LAD22	2-LAD22	3-LAD30	1-LAD14	2-LAD30	3-LAD30
AD23	1-LAD23	2-LAD23	3-LAD31	1-LAD15	2-LAD31	3-LAD31
AD24	1-LAD24	2-LAD24	4-LAD24	1-LAD0	2-LAD16	4-LAD24
AD25	1-LAD25	2-LAD25	4-LAD25	1-LAD1	2-LAD17	4-LAD25
AD26	1-LAD26	2-LAD26	4-LAD26	1-LAD2	2-LAD18	4-LAD26
AD27	1-LAD27	2-LAD27	4-LAD27	1-LAD3	2-LAD19	4-LAD27
AD28	1-LAD28	2-LAD28	4-LAD28	1-LAD4	2-LAD20	4-LAD28
AD29	1-LAD29	2-LAD29	4-LAD29	1-LAD5	2-LAD21	4-LAD29
AD30	1-LAD30	2-LAD30	4-LAD30	1-LAD6	2-LAD22	4-LAD30
AD31	1-LAD31	2-LAD31	4-LAD31	1-LAD7	2-LAD23	4-LAD31

**Table 5-7. PCI Express Dword Format Bus Data Bits Mapping onto Local Bus M Mode –
Low Byte Lane**

PCI Express Dword Format Bus (Internal AD)	M Mode Local Bus Ball Byte Lane Mode = 0 (LCS_BIGEND[4]=0)					
	Little Endian			Big Endian		
	32-Bit	16-Bit	8-Bit	32-Bit	16-Bit	8-Bit
AD0	1-LD31	1-LD31	1-LD31	1-LD7	1-LD23	1-LD31
AD1	1-LD30	1-LD30	1-LD30	1-LD6	1-LD22	1-LD30
AD2	1-LD29	1-LD29	1-LD29	1-LD5	1-LD21	1-LD29
AD3	1-LD28	1-LD28	1-LD28	1-LD4	1-LD20	1-LD28
AD4	1-LD27	1-LD27	1-LD27	1-LD3	1-LD19	1-LD27
AD5	1-LD26	1-LD26	1-LD26	1-LD2	1-LD18	1-LD26
AD6	1-LD25	1-LD25	1-LD25	1-LD1	1-LD17	1-LD25
AD7	1-LD24	1-LD24	1-LD24	1-LD0	1-LD16	1-LD24
AD8	1-LD23	1-LD23	2-LD31	1-LD15	1-LD31	2-LD31
AD9	1-LD22	1-LD22	2-LD30	1-LD14	1-LD30	2-LD30
AD10	1-LD21	1-LD21	2-LD29	1-LD13	1-LD29	2-LD29
AD11	1-LD20	1-LD20	2-LD28	1-LD12	1-LD28	2-LD28
AD12	1-LD19	1-LD19	2-LD27	1-LD11	1-LD27	2-LD27
AD13	1-LD18	1-LD18	2-LD26	1-LD10	1-LD26	2-LD26
AD14	1-LD17	1-LD17	2-LD25	1-LD9	1-LD25	2-LD25
AD15	1-LD16	1-LD16	2-LD24	1-LD8	1-LD24	2-LD24
AD16	1-LD15	2-LD31	3-LD31	1-LD23	2-LD23	3-LD31
AD17	1-LD14	2-LD30	3-LD30	1-LD22	2-LD22	3-LD30
AD18	1-LD13	2-LD29	3-LD29	1-LD21	2-LD21	3-LD29
AD19	1-LD12	2-LD28	3-LD28	1-LD20	2-LD20	3-LD28
AD20	1-LD11	2-LD27	3-LD27	1-LD19	2-LD19	3-LD27
AD21	1-LD10	2-LD26	3-LD26	1-LD18	2-LD18	3-LD26
AD22	1-LD9	2-LD25	3-LD25	1-LD17	2-LD17	3-LD25
AD23	1-LD8	2-LD24	3-LD24	1-LD16	2-LD16	3-LD24
AD24	1-LD7	2-LD23	4-LD31	1-LD31	2-LD31	4-LD31
AD25	1-LD6	2-LD22	4-LD30	1-LD30	2-LD30	4-LD30
AD26	1-LD5	2-LD21	4-LD29	1-LD29	2-LD29	4-LD29
AD27	1-LD4	2-LD20	4-LD28	1-LD28	2-LD28	4-LD28
AD28	1-LD3	2-LD19	4-LD27	1-LD27	2-LD27	4-LD27
AD29	1-LD2	2-LD18	4-LD26	1-LD26	2-LD26	4-LD26
AD30	1-LD1	2-LD17	4-LD25	1-LD25	2-LD25	4-LD25
AD31	1-LD0	2-LD16	4-LD24	1-LD24	2-LD24	4-LD24

**Table 5-8.   PCI Express Dword Format Bus Data Bits Mapping onto Local Bus M Mode –
High Byte Lane**

PCI Express Dword Format Bus (Internal AD)	M Mode Local Bus Ball Byte Lane Mode = 1 (LCS_BIGEND[4]=1)					
	Little Endian			Big Endian		
	32-Bit	16-Bit	8-Bit	32-Bit	16-Bit	8-Bit
AD0	1-LD31	1-LD15	1-LD7	1-LD7	1-LD7	1-LD7
AD1	1-LD30	1-LD14	1-LD6	1-LD6	1-LD6	1-LD6
AD2	1-LD29	1-LD13	1-LD5	1-LD5	1-LD5	1-LD5
AD3	1-LD28	1-LD12	1-LD4	1-LD4	1-LD4	1-LD4
AD4	1-LD27	1-LD11	1-LD3	1-LD3	1-LD3	1-LD3
AD5	1-LD26	1-LD10	1-LD2	1-LD2	1-LD2	1-LD2
AD6	1-LD25	1-LD9	1-LD1	1-LD1	1-LD1	1-LD1
AD7	1-LD24	1-LD8	1-LD0	1-LD0	1-LD0	1-LD0
AD8	1-LD23	1-LD7	2-LD7	1-LD15	1-LD15	2-LD7
AD9	1-LD22	1-LD6	2-LD6	1-LD14	1-LD14	2-LD6
AD10	1-LD21	1-LD5	2-LD5	1-LD13	1-LD13	2-LD5
AD11	1-LD20	1-LD4	2-LD4	1-LD12	1-LD12	2-LD4
AD12	1-LD19	1-LD3	2-LD3	1-LD11	1-LD11	2-LD3
AD13	1-LD18	1-LD2	2-LD2	1-LD10	1-LD10	2-LD2
AD14	1-LD17	1-LD1	2-LD1	1-LD9	1-LD9	2-LD1
AD15	1-LD16	1-LD0	2-LD0	1-LD8	1-LD8	2-LD0
AD16	1-LD15	2-LD15	3-LD7	1-LD23	2-LD7	3-LD7
AD17	1-LD14	2-LD14	3-LD6	1-LD22	2-LD6	3-LD6
AD18	1-LD13	2-LD13	3-LD5	1-LD21	2-LD5	3-LD5
AD19	1-LD12	2-LD12	3-LD4	1-LD20	2-LD4	3-LD4
AD20	1-LD11	2-LD11	3-LD3	1-LD19	2-LD3	3-LD3
AD21	1-LD10	2-LD10	3-LD2	1-LD18	2-LD2	3-LD2
AD22	1-LD9	2-LD9	3-LD1	1-LD17	2-LD1	3-LD1
AD23	1-LD8	2-LD8	3-LD0	1-LD16	2-LD0	3-LD0
AD24	1-LD7	2-LD7	4-LD7	1-LD31	2-LD15	4-LD7
AD25	1-LD6	2-LD6	4-LD6	1-LD30	2-LD14	4-LD6
AD26	1-LD5	2-LD5	4-LD5	1-LD29	2-LD13	4-LD5
AD27	1-LD4	2-LD4	4-LD4	1-LD28	2-LD12	4-LD4
AD28	1-LD3	2-LD3	4-LD3	1-LD27	2-LD11	4-LD3
AD29	1-LD2	2-LD2	4-LD2	1-LD26	2-LD10	4-LD2
AD30	1-LD1	2-LD1	4-LD1	1-LD25	2-LD9	4-LD1
AD31	1-LD0	2-LD0	4-LD0	1-LD24	2-LD8	4-LD0

5.2.2   Local Bus Big/Little Endian Mode Accesses

For each of the following transfer types, the PEX 8311 Local Bus is independently programmed, by way of the **LCS_BIGEND** register, to operate in Little or Big Endian mode:

- Local Bus accesses to the PEX 8311 **LCS** Configuration registers
- Direct Slave PCI accesses to Local Address Space 0, Space 1, and Expansion ROM
- DMA Channel *x* accesses to the Local Bus
- Direct Master accesses to the internal PCI Bus

For Local Bus accesses to the LCS Configuration registers and Direct Master accesses, use BIGEND# to dynamically change the Endian mode.

Note: *The PCI Express interface is serial and always Little Endian. For Little Endian-to-Big Endian conversion, only byte lanes are swapped, not individual bits.*

Chapter 6   C and J Modes Functional Description

6.1   Introduction

The functional operation described in this section is modified or programmed through the PEX 8311 LCS registers.

6.2   Recovery States (J Mode Only)

In J mode, the PEX 8311 inserts one recovery state on the Local Bus between the last Data transfer and the next Address cycle.

Note: *The PEX 8311 does **not** support the i960J function that uses READY# input to add recovery states. No additional recovery states are added when READY# input remains asserted during the last Data cycle.*

6.3   Wait State Control

6.3.1   Wait State Control

If the PEX 8311 Local Bus READY# mode is disabled (**LCS_LBRD0/1**[6]=0 for Space 0/1, **LCS_LBRD0**[22]=0 for Expansion ROM, and/or LCS_DMAMODE0/**1**[6]=0 for DMA Channel 0/1), the external READY# input signal does not affect wait states for a Local access. Wait states between Data cycles are internally asserted by Wait State Counter(s) for the affected Local Address space and/or DMA channel (**LCS_LBRD0/1**[5:2] for Space 0/1, **LCS_LBRD0**[21:18] for Expansion ROM, and/or **LCS_DMAMODE0/1**[5:2] for DMA Channel 0/1). The Wait State Counter(s) is initialized with its Configuration register value at the start of each Data access.

If READY# mode is enabled (**LCS_LBRD0/1**[6]=1 for Space 0/1, **LCS_LBRD0**[22]=1 for Expansion ROM, and/or **LCS_DMAMODE0/1**[6]=1 for DMA Channel 0/1), it has no effect until the Wait State Counter(s) reaches 0. READY# then controls the number of additional wait states.

BTERM# input is not sampled until the Wait State Counter(s) reaches 0. BTERM# assertion overrides READY# when BTERM# is enabled (**LCS_LBRD0/1**[7]=1 for Space 0/1, **LCS_LBRD0**[23]=1 for Expansion ROM, and/or **LCS_DMAMODE0/1**[7]=1 for DMA Channel 0/1) and asserted.

Figure 6-1 illustrates the PEX 8311 wait states for C and J modes.

Figure 6-1.   Wait States – C and J Modes
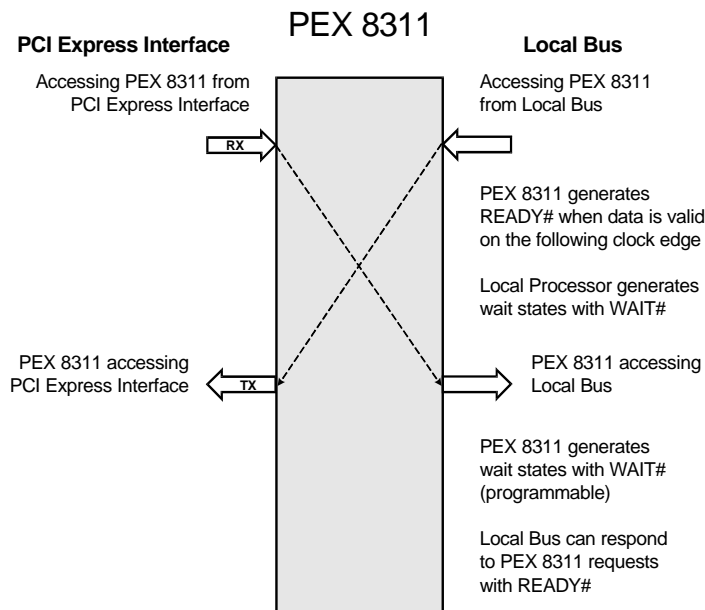
Note: Figure 6-1 represents a sequence of Bus cycles.

6.3.2   Local Bus Wait States

In Direct Master mode when accessing the PEX 8311 registers, the PEX 8311 acts as a Local Bus Slave. The PEX 8311 inserts wait states by delaying the READY# signal. The Local Bus Master inserts wait states with the WAIT# signal. For Writes to PEX 8311 registers, assert WAIT# until data is valid.

In Direct Slave and DMA modes, the PEX 8311 acts as a Local Bus Master. The PEX 8311 inserts Local Bus Slave wait states with the WAIT# signal. The Local Bus Target asserts external wait states by delaying the READY# signal. The Internal Wait State Counter(s) is programmed to insert wait states between the address and first data states, with the same number of wait states between subsequent data within bursts. (Refer to Table 6-1.)

For Direct Master writes, to insert wait states between the Address phase and the first data, the WAIT# signal must be asserted during the Address phase [ADS# (C mode) or ALE (J mode) assertion]. Thereafter, WAIT# is toggled, as necessary, to insert wait states.

During Direct Master accesses, when WAIT# is asserted during the Address phase (ADS# assertion) or after the ADS# assertion for a Direct Master Read, the PEX 8311 latches the address but does not begin an internal request on the PCI Express interface, no TLP Read request is generated until WAIT# is de-asserted. This results in the PEX 8311 not having the data available on the Local Bus. In this case, WAIT# de-assertion by the Local Bus Master enables the PEX 8311 to become the Direct Master Read access on the Local Bus. WAIT# assertion by the Local Bus Master on the second Local Bus Clock cycle after the Address phase (ADS# is de-asserted) allows the Direct Master Read access to generate a TLP Read request on the PCI Express interface.

Note: *Do not use READY# as a gating signal for WAIT# de-assertion. Otherwise, the PEX 8311 does not complete the transfer.*

Table 6-1.   Internal Wait State Counters

Bits	Description
LCS_LBRD0[5:2]	Local Address Space 0 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
LCS_LBRD1[5:2]	Local Address Space 1 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
LCS_LBRD0[21:18]	Expansion ROM Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
LCS_DMAMODE0[5:2]	DMA Channel 0 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
LCS_DMAMODE1[5:2]	DMA Channel 1 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)

6.4   C and J Modes Functional Timing Diagrams

General notes about timing designer (graphical) waveforms:
The graphical Timing Diagrams were created using the Timing Designer
tool. They are accurate and adhere to their specified protocol(s). These
diagrams show transfers and signal transitions; however, they should
not be relied upon to show exactly, on a clock-for-clock basis, wherein
PEX 8311-driven signal transitions will occur.

General notes about captured waveforms:
The captured Timing Diagrams were captured from a simulation signal
display tool that displays the results of stimulus run on the netlist. Using the
netlist illustrates realistic delay on signals driven by the PEX 8311. Signals
driven by the test environment to the PEX 8311 are quite fast. Leading zeros
(0) for buses such as LD[31:0] (C mode) or LAD[31:0] (J mode), may or
may not be shown. When no value for a bus is shown while the PEX 8311
is executing a transfer, it is because the entire value cannot be displayed in
the available space or is irrelevant. When the PEX 8311 is not executing a
transfer on that bus, the value is not shown because it is either irrelevant or
unknown (any or all signals are 1, 0, or Z).

For the J mode waveforms, the Local Address Bus balls (LA[28:2])
are optional and may not be shown.

Timing Diagram 6-1. BREQo and Deadlock
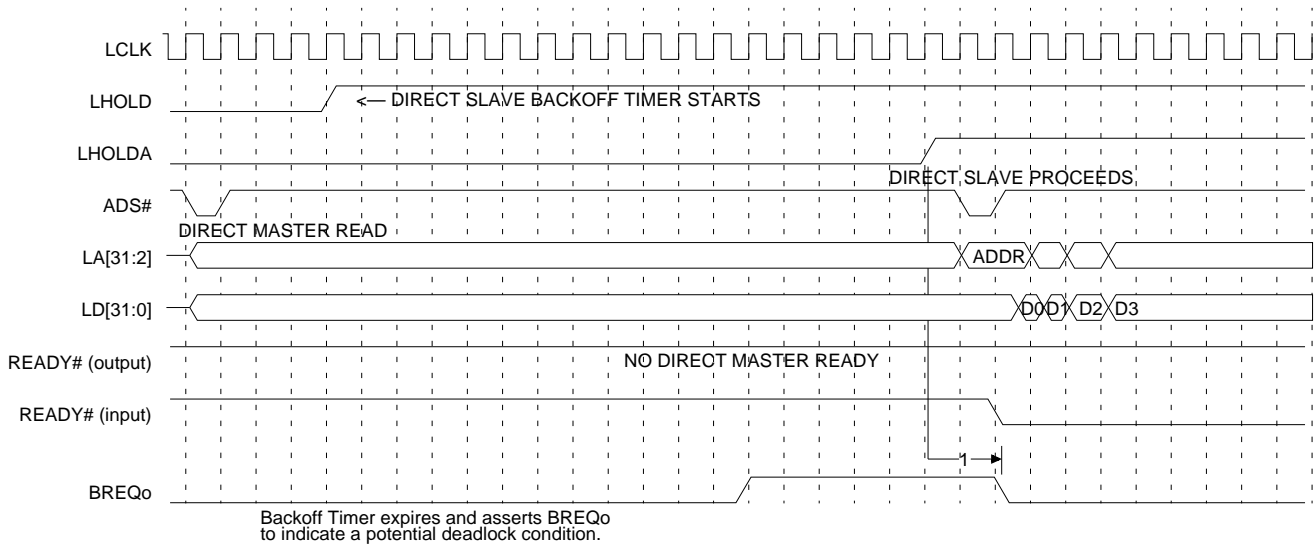
Notes: *For partial deadlock, Direct Slave Retry Delay Clocks field (LCS_LBRD0[31:28]) is used to issue Retrys*
to the Direct Master attempting the Direct Slave access.

Timing Diagram 6-1 contains C mode signals/names. The overall behavior in J mode is the same. Arrow 1
indicates that LHOLDA assertion causes the PEX 8311 to de-assert BREQo. The READY# (output and input)
signals are the same ball. The PEX 8311 READY# ball is an input while processing Direct Slave Reads and
an output when processing Direct Master Reads.

6.4.1   Configuration Timing Diagrams

Timing Diagram 6-2. Local Write to Configuration Register (C Mode)
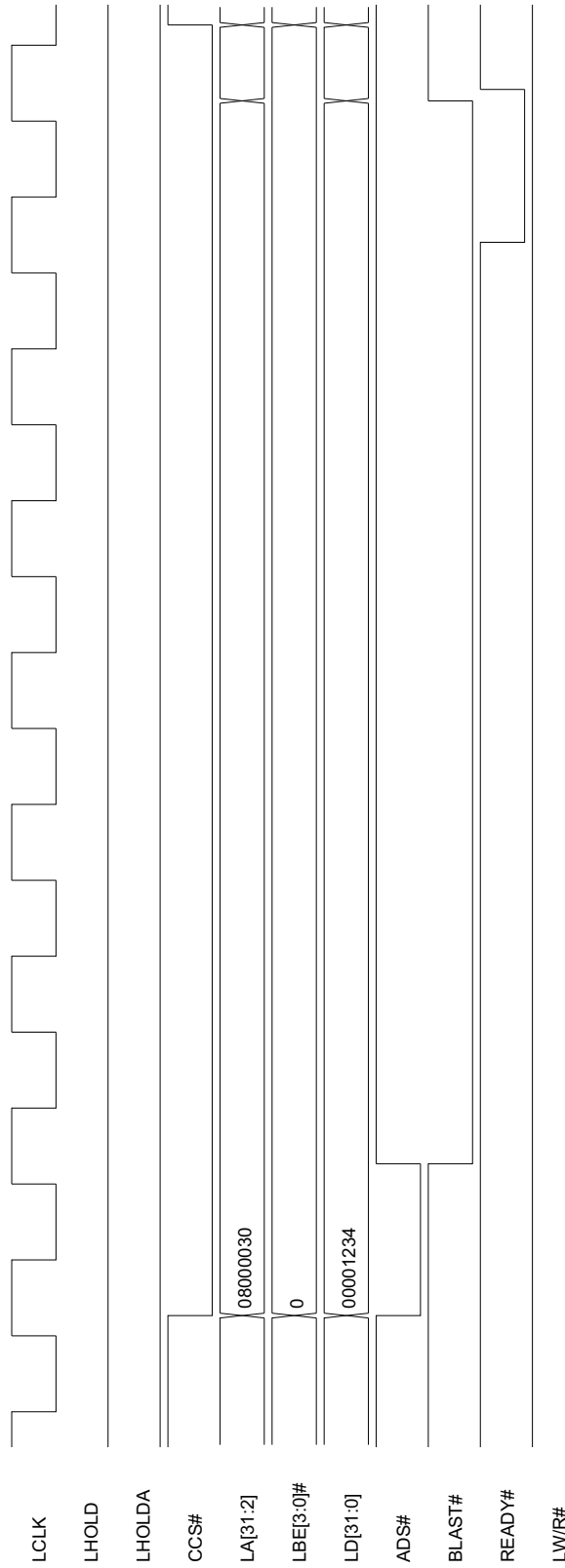
LCLK

LHOLD

LHOLDA

CCS#

LA[31:2]   08000030

LBE[3:0]#   0

LD[31:0]   00001234

ADS#

BLAST#

READY#

LW/R#

Notes: *Local Configuration Write to* **LCS_MBOX0** *(LOC:C0h) register.*

CCS# is asserted for multiple Clock cycles, but it is required to be asserted only during the **ADS#** *Clock cycle.*

Only the LA[8:2] signals are used to decode the register.

LA[31:2] is a Dword address (Master accesses to the PEX 8311 are always 32-bit data quantities).

Timing Diagram 6-3. Local Read of Configuration Register (C Mode)

LCLK

LHOLD

LHOLDA

CCS#

LA[31:2]   08000030

LBE[3:0]#   0

LD[31:0]   F0430043   00001234

ADS#

BLAST#

READY#

LW/R#
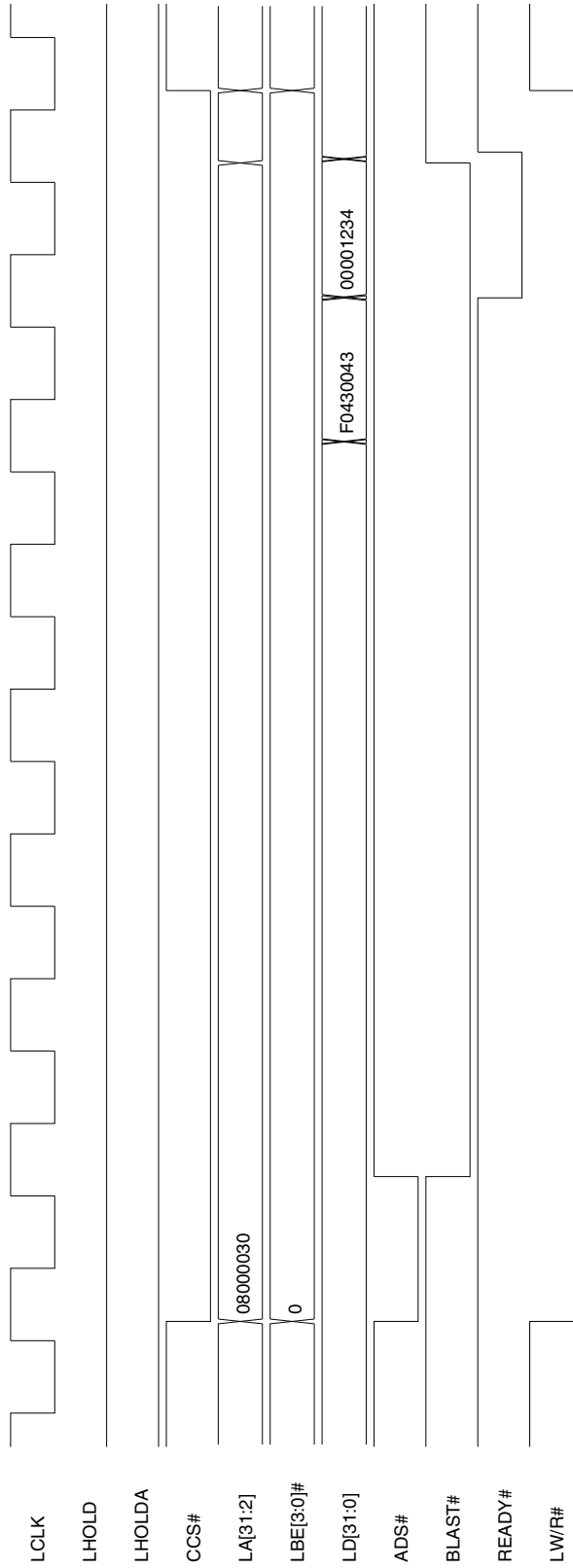
Notes: *Local Configuration Read of **LCS_MBOX0** (LOC:C0h) register.*

CCS# is asserted for multiple Clock cycles, but it is required to be asserted only during the ADS# Clock cycle.

Only the LA[8:2] signals are used to decode the register.

LA[31:2] is the Dword address (Master accesses to the PEX 8311 are always 32-bit data quantities).

The PEX 8311 starts driving the LD[31:0] bus with meaningless data (F043_0043h), one cycle before

it asserts READY# with the data read from the register.

Timing Diagram 6-4. Local Write to Configuration Register (J Mode)
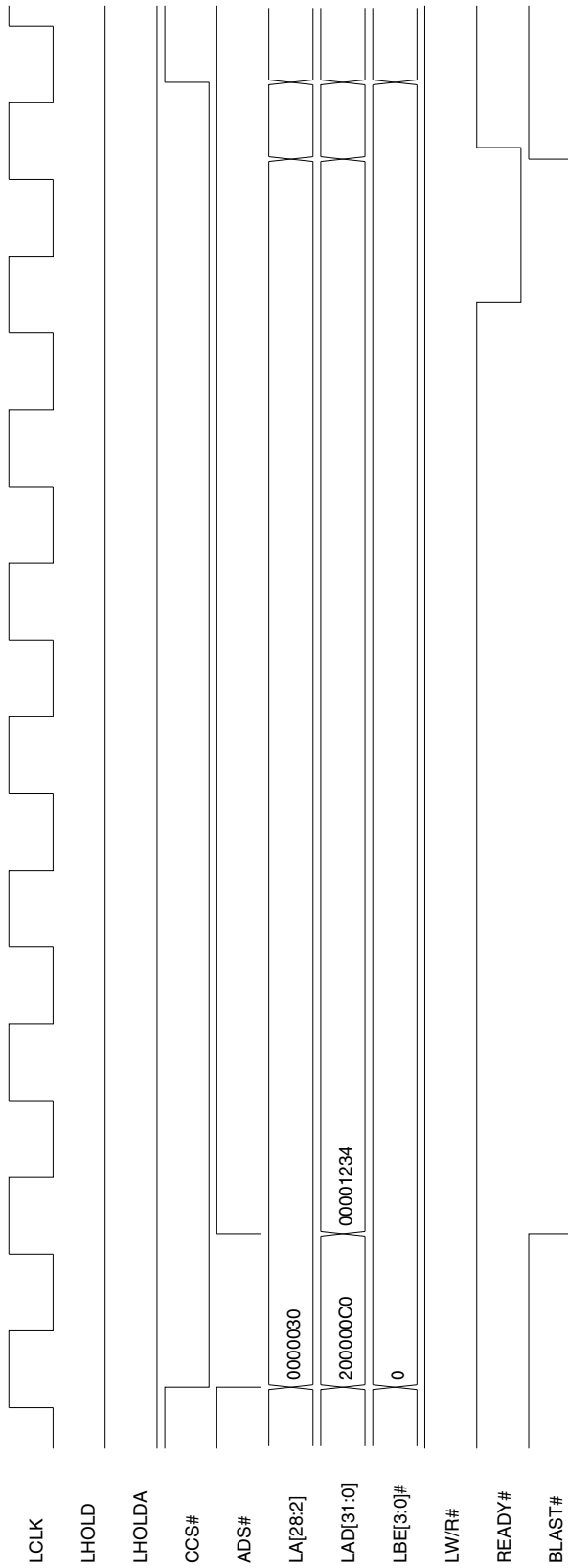
LCLK

LHOLD

LHOLDA

CCS#

ADS#

LA[28:2]   0000030

LAD[31:0]   200000C0   00001234

LBE[3:0]#   0

LW/R#

READY#

BLAST#

Notes: *Local Configuration Write to* **LCS_MBOX0** *(LOC:C0h) register.*

CCS# is asserted for multiple Clock cycles; however, it is only required to be asserted during the ADS# *Clock cycle (or while* ALE *is asserted, which is not shown).*

Only the LAD[8:2] signals are used to decode the **LCS_MBOX0** *register.*

LA[28:2] is shown; however, it is not used by the PEX 8311 during Local Master accesses to the PEX 8311.

Local Master accesses to the PEX 8311 are always 32-bit data quantities.

Timing Diagram 6-5. Local Read of Configuration Register (J Mode)

LCLK

LHOLD

LHOLDA

CCS#

ADS#

LA[28:2]   0000030 | |

LAD[31:0]   200000C0 | 00001234 |

LBE[3:0]#   0

LW/R#

READY#

BLAST#
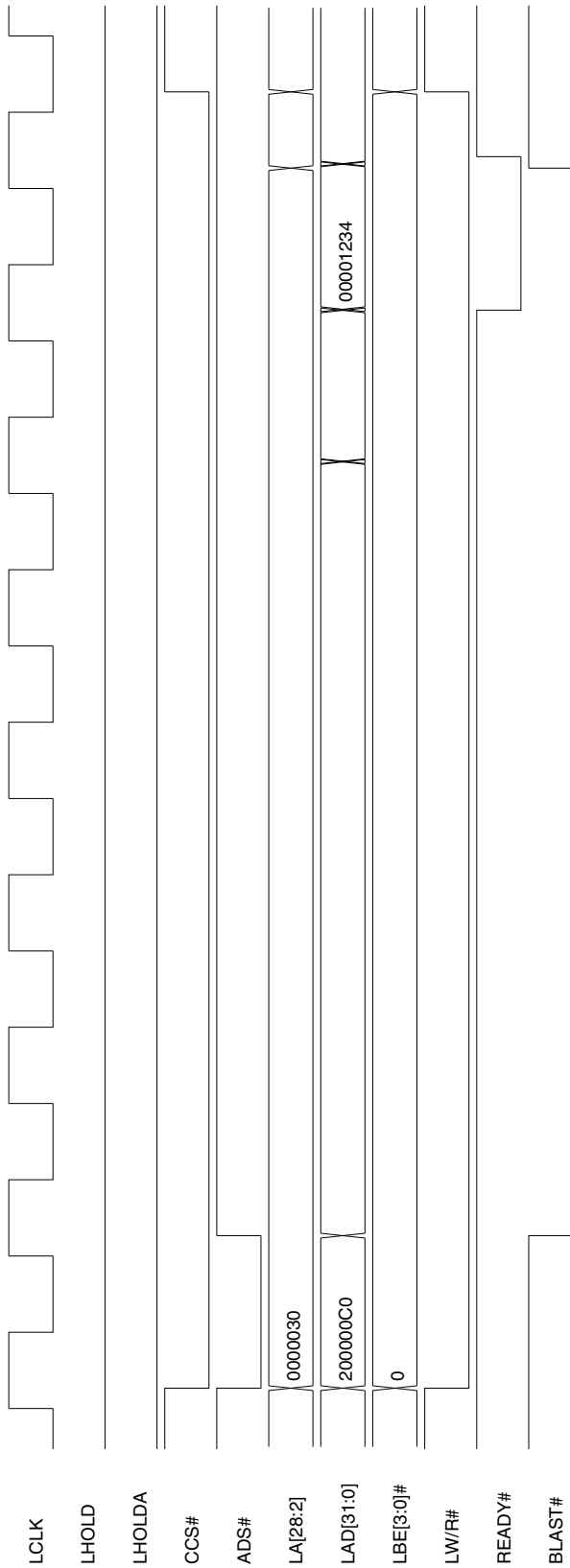
Notes: Local Configuration Read to **LCS_MBOX0** (LOC:C0h) register.

CCS# is asserted for multiple Clock cycles; however, it is only required to be asserted during the ADS# Clock cycle (or while ALE is asserted, which is not shown).

Only the LAD[8:2] signals are used to decode the **LCS_MBOX0** *register.*

LA[28:2] is shown; however, it is not used by the PEX 8311 when a Local Master accesses the PEX 8311.

Local Master accesses to the PEX 8311 are always 32-bit data quantities.

6.5 C Mode Functional Timing Diagrams

6.5.1 C Mode Direct Master Timing Diagrams

Timing Diagram 6-6. Direct Master Configuration Write – Type 0 or Type 1
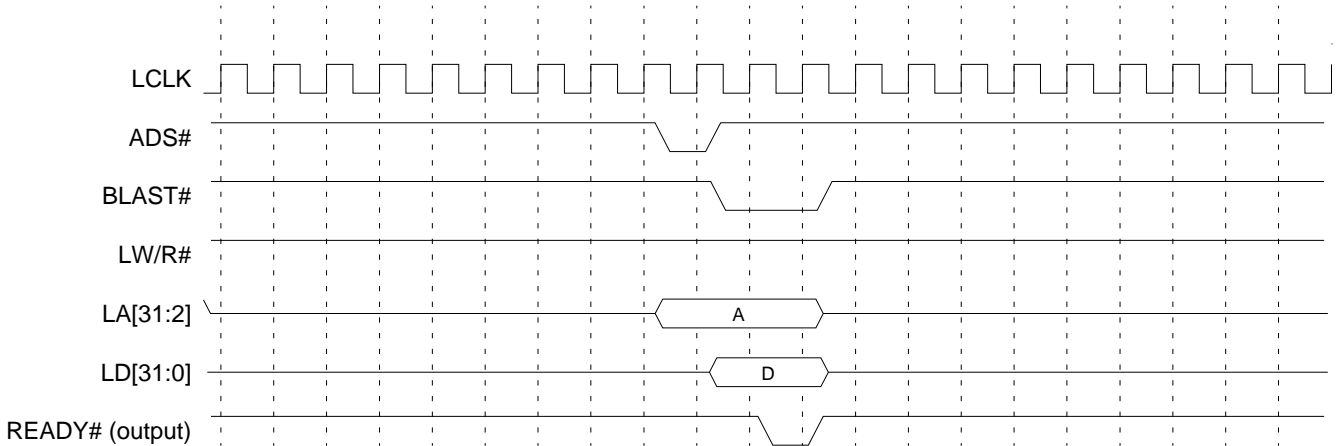
Note: Timing Diagram 6-6 illustrates a Direct Master Configuration Write that causes the PEX 8311 to generate a 32-bit PCI Type 0 or Type 1 Configuration Write cycle. Refer to Section 10.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," for details.

Timing Diagram 6-7. Direct Master Configuration Read – Type 0 or Type 1
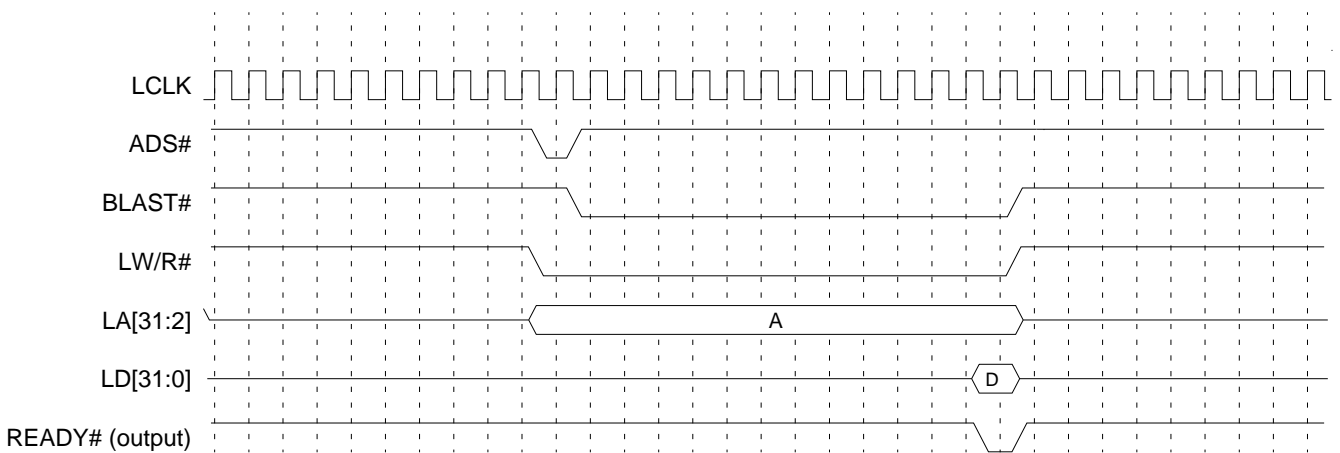
Note: Timing Diagram 6-7 illustrates a Direct Master Configuration Read that causes the PEX 8311 to generate a 32-bit PCI Type 0 or Type 1 Configuration Read cycle. Refer to Section 10.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," for details.

Timing Diagram 6-8. Direct Master Single Cycle Write

LCLK

LHOLD

LHOLDA

LA[31:2]   25950000

LBE[3:0]#   0

LD[31:0]   04030201

ADS#

BLAST#

READY#

LW/R#
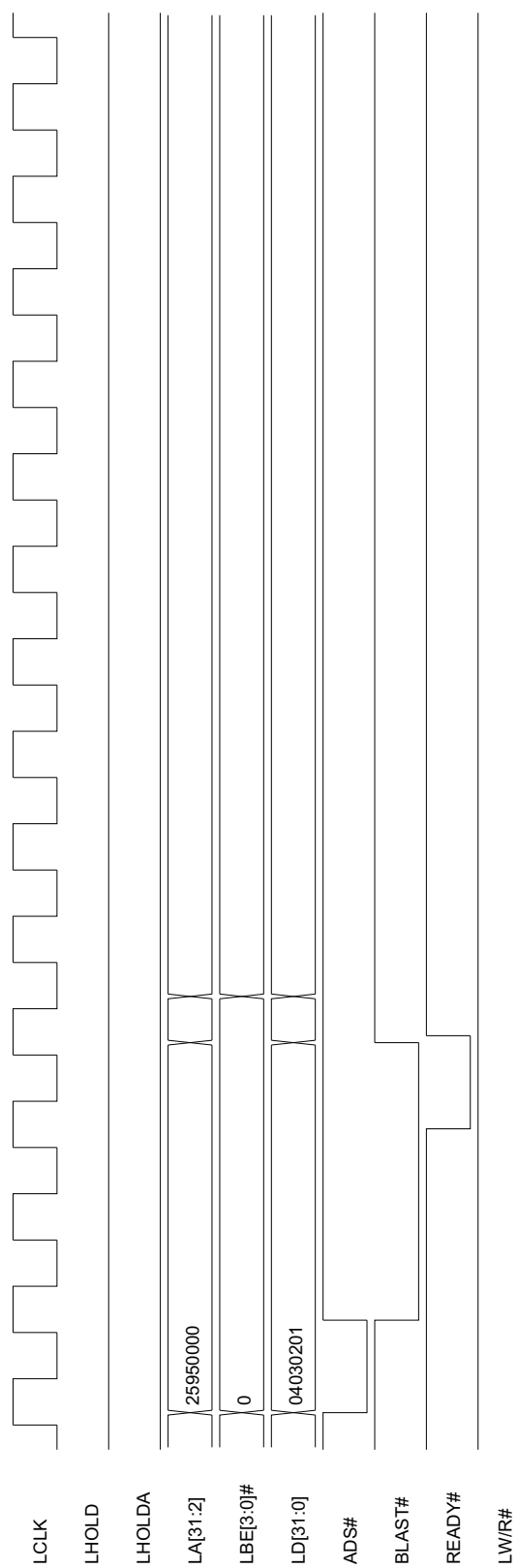
Note: Key register value is LCS_DMPBAM[15:0]=00E3h.

Timing Diagram 6-9. Direct Master Single Cycle Read

Signal	
LCLK	
LHOLD	
LHOLDA	
LA[31:2]	25950000
LBE[3:0]#	0
LD[31:0]	DATA
ADS#	
BLAST#	
READY#	
LW/R#	
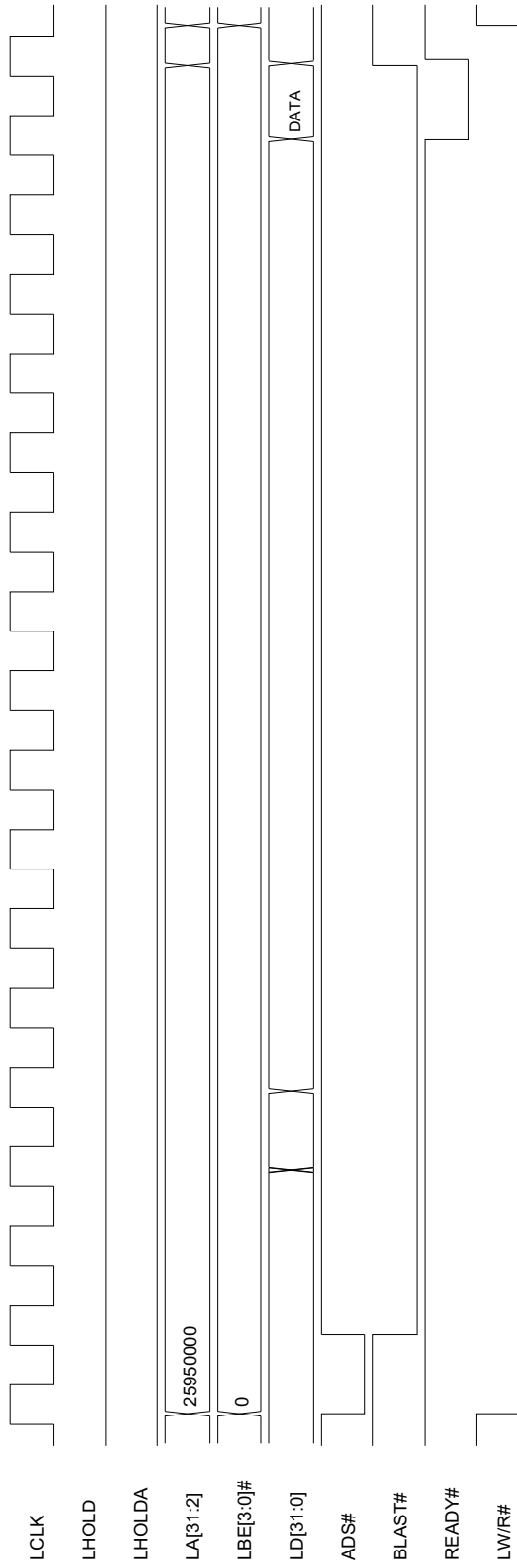
Note: Key register value is LCS_DMPBAM[15:0]=00E3h.

Timing Diagram 6-10. Direct Master Burst Write of 8 Dwords

LCLK	
LHOLD	
LHOLDA	
LA[31:2]	25950000
LBE[3:0]#	0
LD[31:0]	03020100
ADS#	
BLAST#	
READY#	
LW/R#	
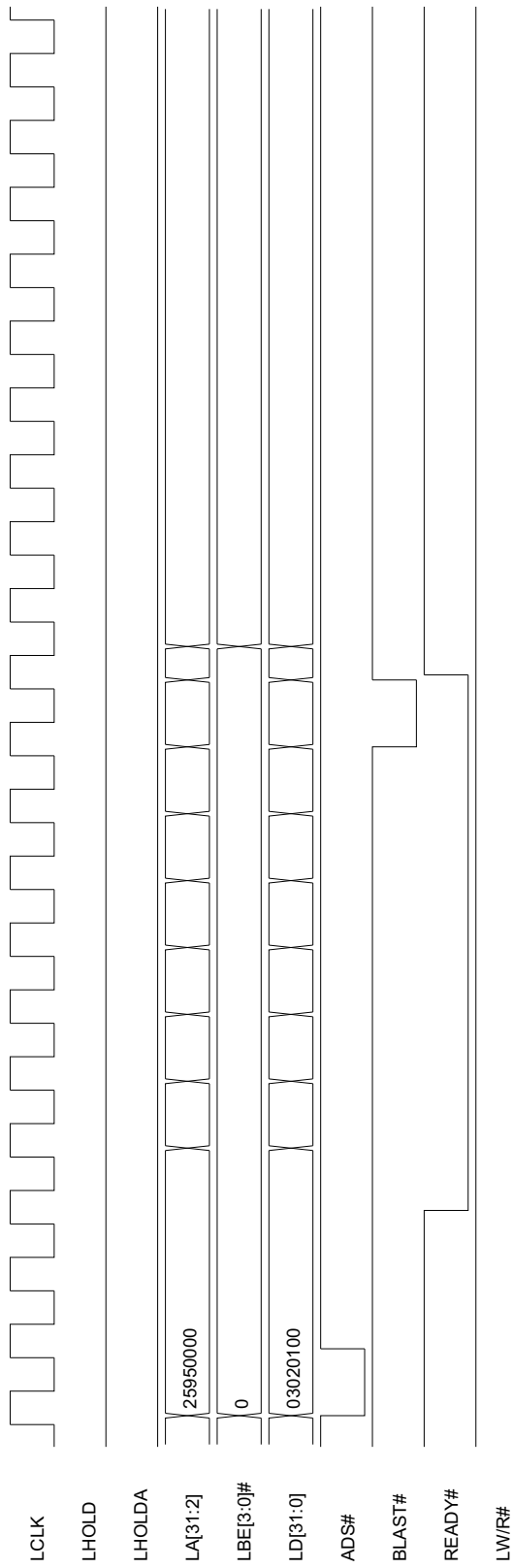
Note: Key register value is LCS_DMPBAM[15:0]=0007h.

Timing Diagram 6-11. Direct Master Burst Read of 8 Dwords

LCLK

LHOLD

LHOLDA

LA[31:2]   25950000

LBE[3:0]#   0

LD[31:0]

ADS#

BLAST#

READY#

LW/R#
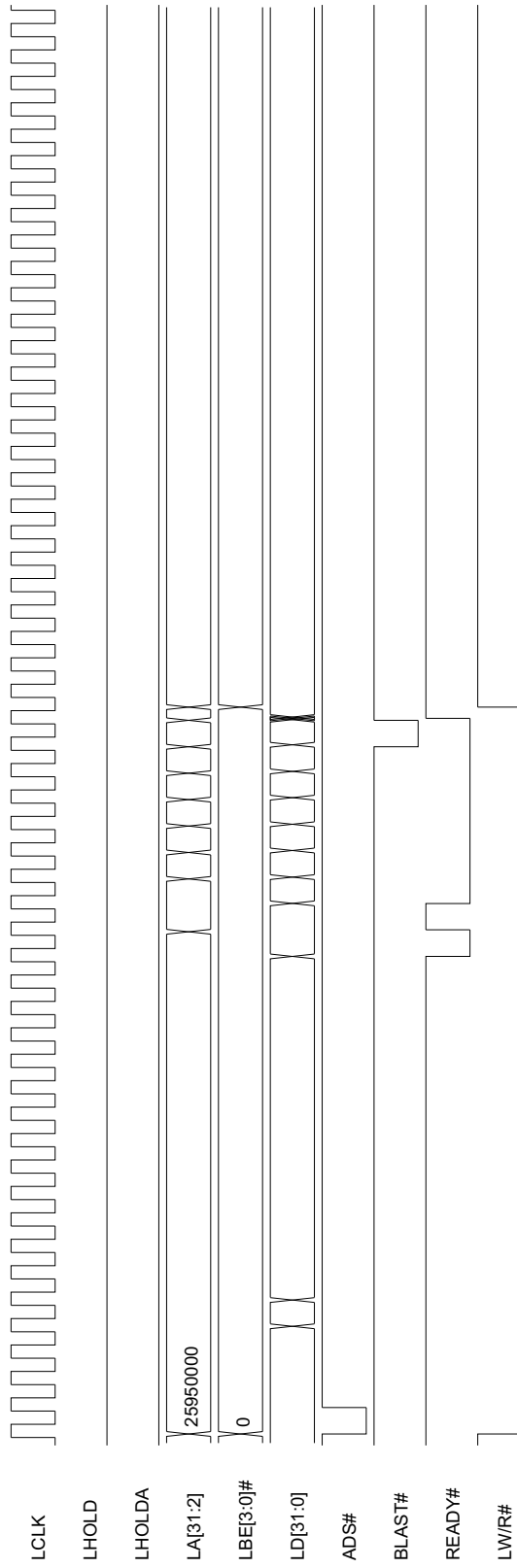
Note: Key register value is LCS_DMPBAM[15:0]=0007h.

6.5.2   C Mode Direct Slave Timing Diagrams

Timing Diagram 6-12. Direct Slave Burst Write Suspended by Single Cycle BREQi
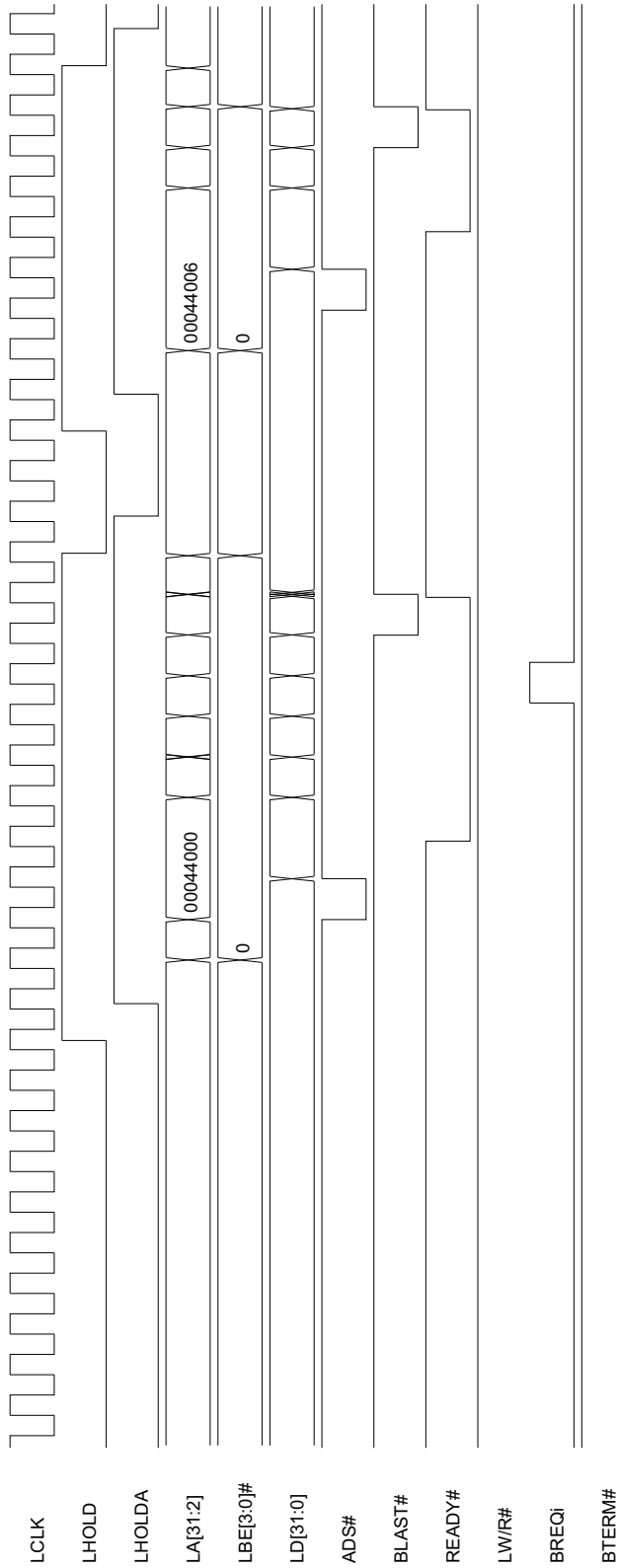
LCLK

LHOLD

LHOLDA

LA[31:2]   00044000   00044006

LBE[3:0]#   0   0

LD[31:0]

ADS#

BLAST#

READY#

LW/R#

BREQi

BTERM#

*Notes: This 9-Dword Direct Slave Burst Write transfer is suspended by a single-Clock cycle BREQi assertion.
The remaining 3 Dwords are transferred after the PEX 8311 is granted the Local Bus again.*

Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=45C2h.

Timing Diagram 6-13. Direct Slave Burst Write Suspended by Multi-Cycle BREQi
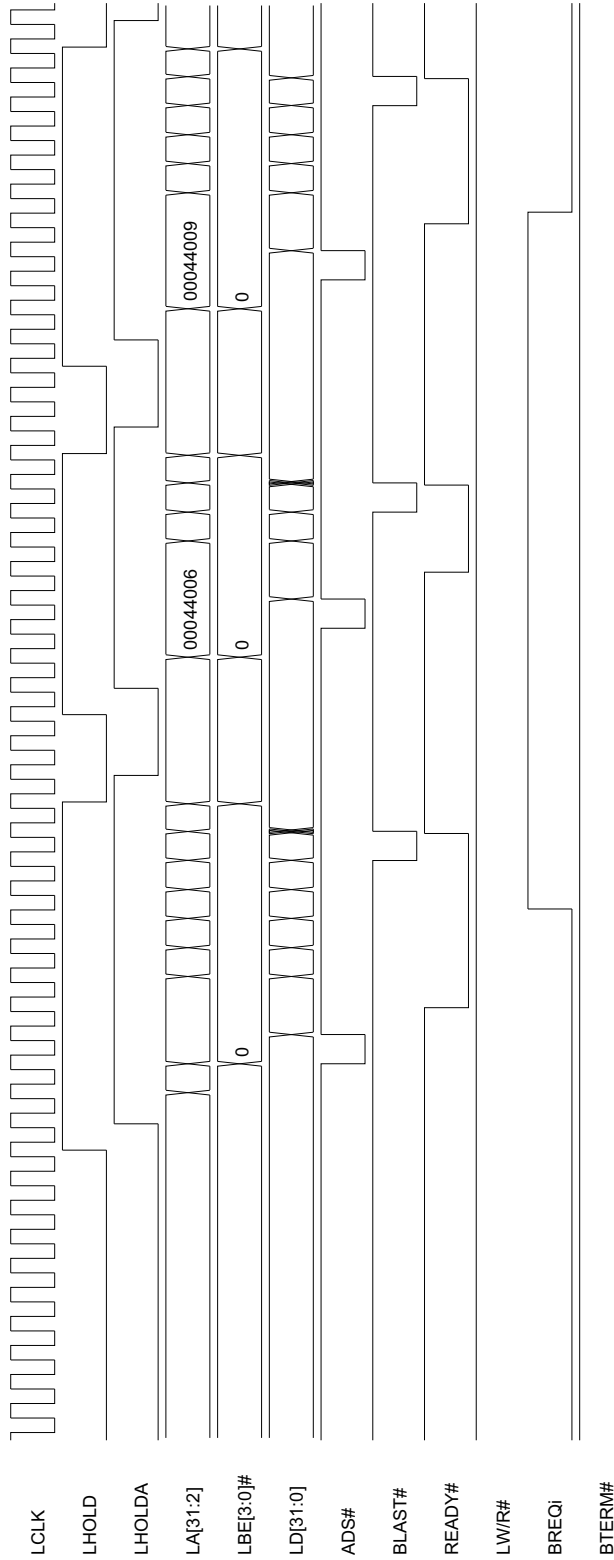
LCLK

LHOLD

LHOLDA

LA[31:2]   00044006   00044009

LBE[3:0]#   0   0   0

LD[31:0]

ADS#

BLAST#

READY#

LW/R#

BREQi

BTERM#

Notes: *This 14-Dword Direct Slave Burst Write transfer is suspended twice by a multi-Clock cycle BREQi assertion.*

Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=45C2h.

Timing Diagram 6-14. Direct Slave Burst Write Interrupted by Single Cycle BTERM#
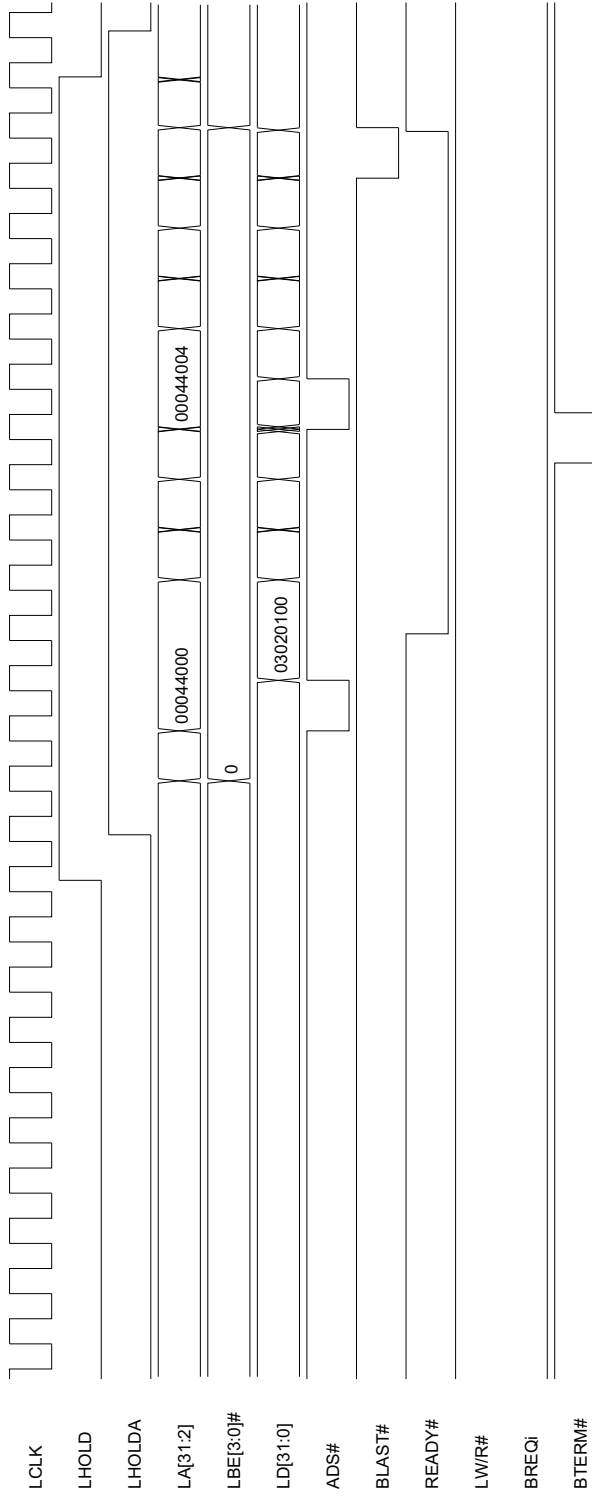
Notes: *This 9-Dword Direct Slave Burst Write transfer is interrupted by a single-Clock cycle BTERM# assertion.*
The remaining 5 Dwords are transferred after the PEX 8311 generates a new Address phase on the Local Bus.

Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=45C2h.

Timing Diagram 6-15. Direct Slave Burst Write Interrupted by Multi-Cycle BBTERM#
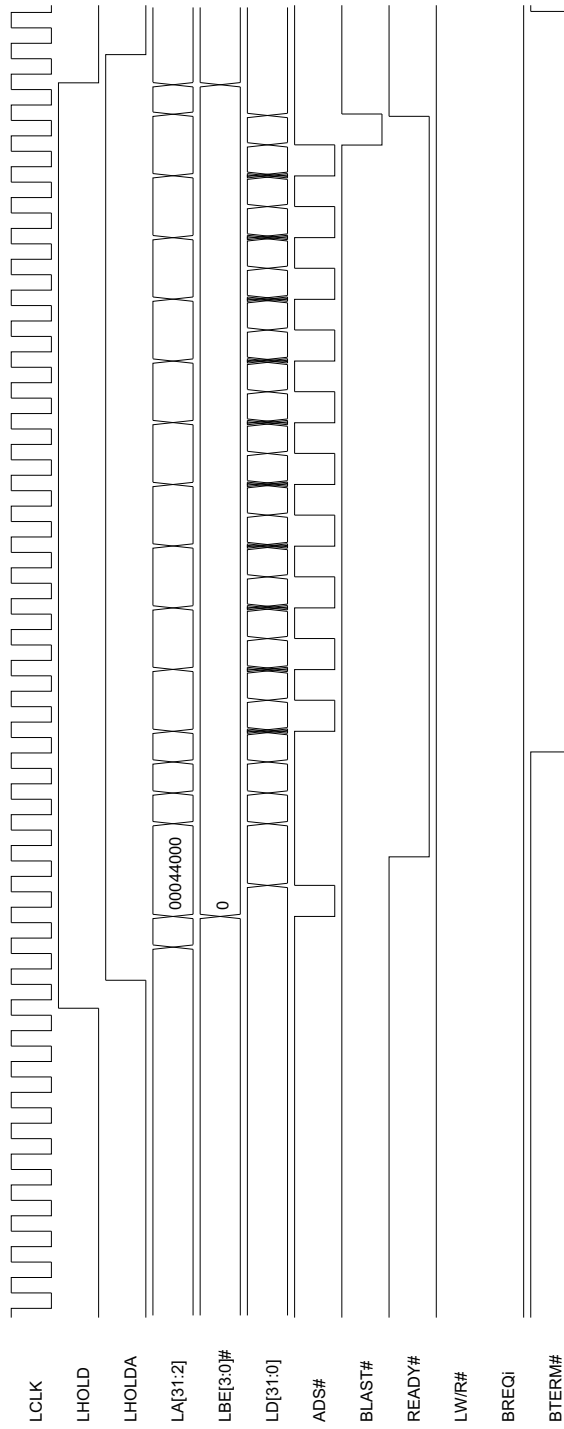
Notes: *This 14-Dword Direct Slave Burst Write transfer is interrupted multiple times by a multi-Clock cycle BTERM# assertion.*

The PEX 8311 generates a new Address phase for each Dword of data transferred, provided that BTERM# remains asserted.

Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=45C2h.

Timing Diagram 6-16. Direct Slave Single Cycle Write (8-Bit Local Bus)

LCLK

LHOLD

LHOLDA

LA[31:2]

LBE[3:0]#

LD[7:0]

ADS#

BLAST#

READY#

LW/R#
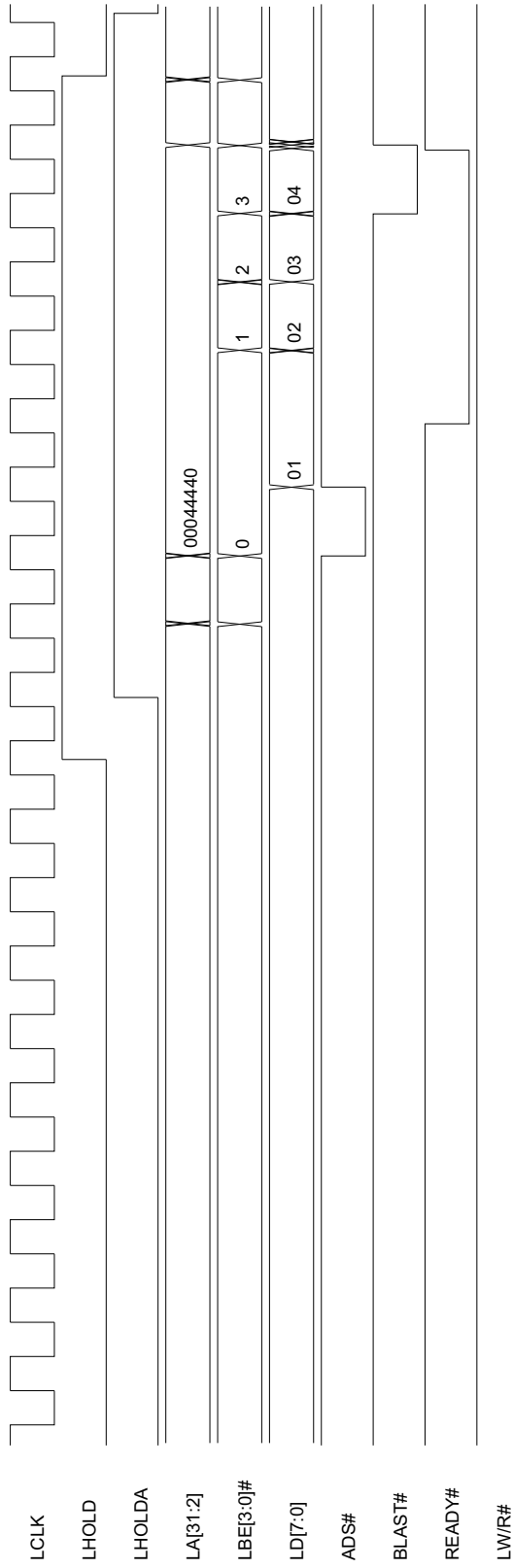
Note: Key bit/register values are LCS_MARBR[24]=1 and LCS_LBRD1[15:0]=0D40h.

Timing Diagram 6-17. Direct Slave Single Cycle Write (16-Bit Local Bus)

LCLK

LHOLD

LHOLDA

LA[31:2]   00044840

LBE[3:0]#   0   2

LD[15:0]   0201   0403

ADS#

BLAST#

READY#

LW/R#
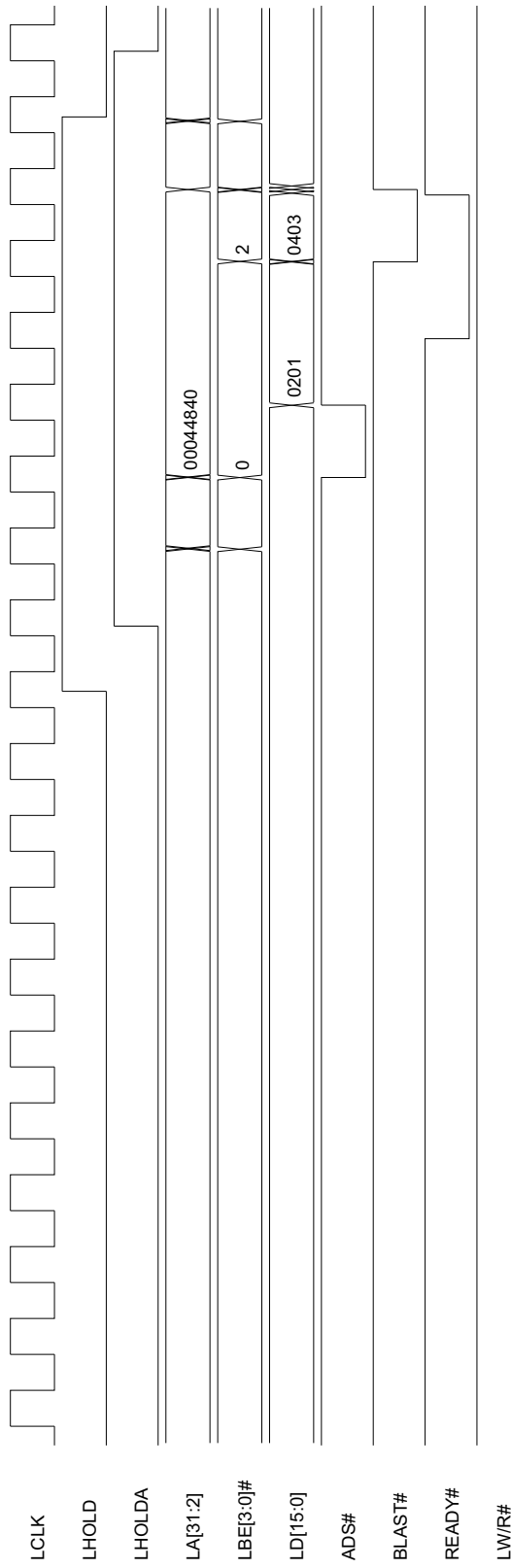
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=1541h.

Timing Diagram 6-18. Direct Slave Single Cycle Write (32-Bit Local Bus)

LCLK

LHOLD

LHOLDA

LA[31:2]   00044000

LBE[3:0]#   0

LD[31:0]   04030201

ADS#

BLAST#

READY#

LW/R#
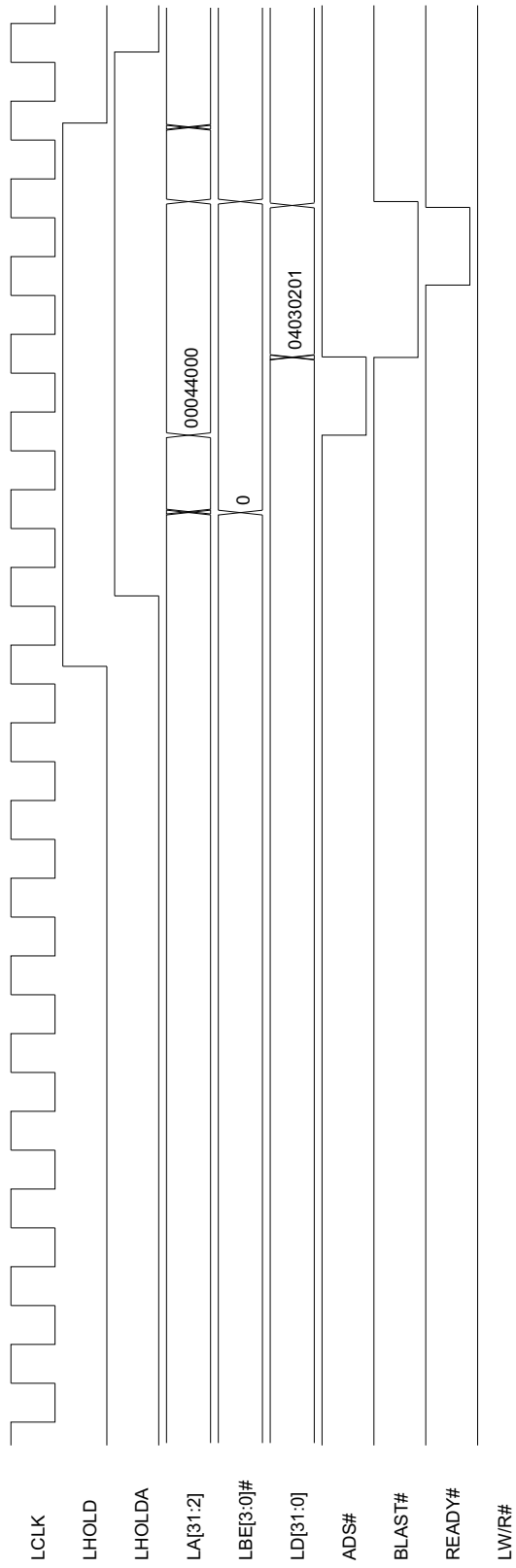
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=0D42h.

Timing Diagram 6-19. Direct Slave Single Cycle Read (8-Bit Local Bus)
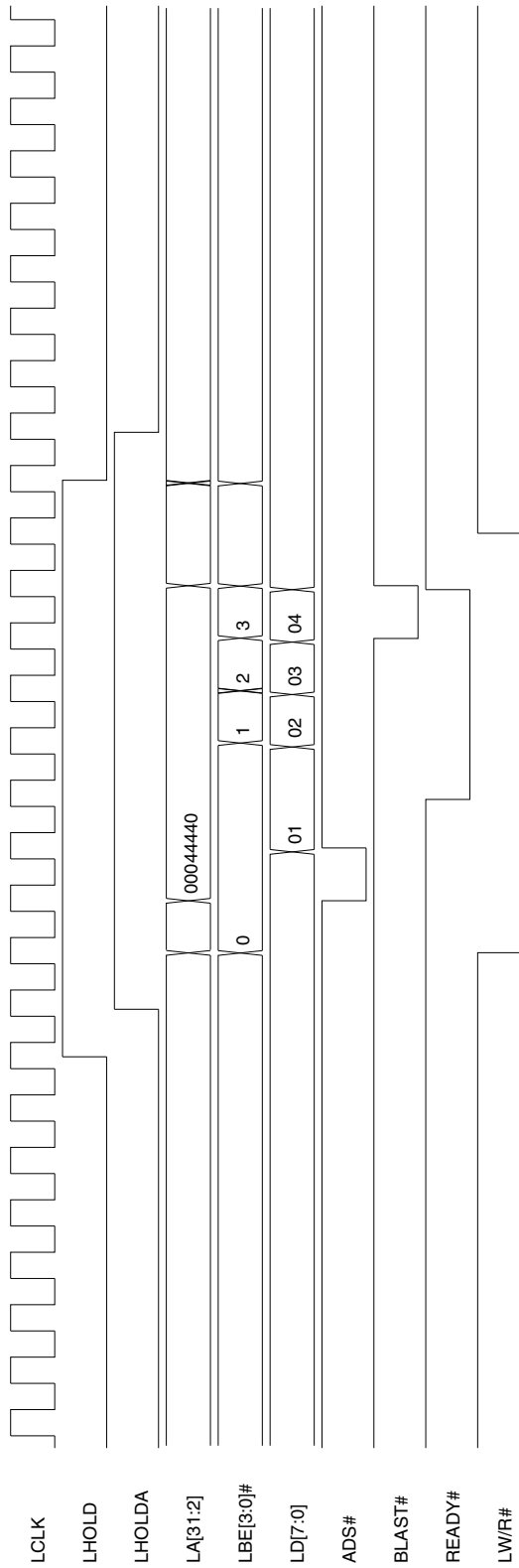
Note: *Key bit/register values are LCS_MARBR[24]=1 and LCS_LBRD1[15:0]=0D40h.*

Timing Diagram 6-20. Direct Slave Single Cycle Read (16-Bit Local Bus)

LCLK
LHOLD
LHOLDA
LA[31:2]
LBE[3:0]#
LD[15:0]
ADS#
BLAST#
READY#
LW/R#

LA[31:2]: 00044840

LBE[3:0]#: 0 / 2

LD[15:0]: 0201 / 0403
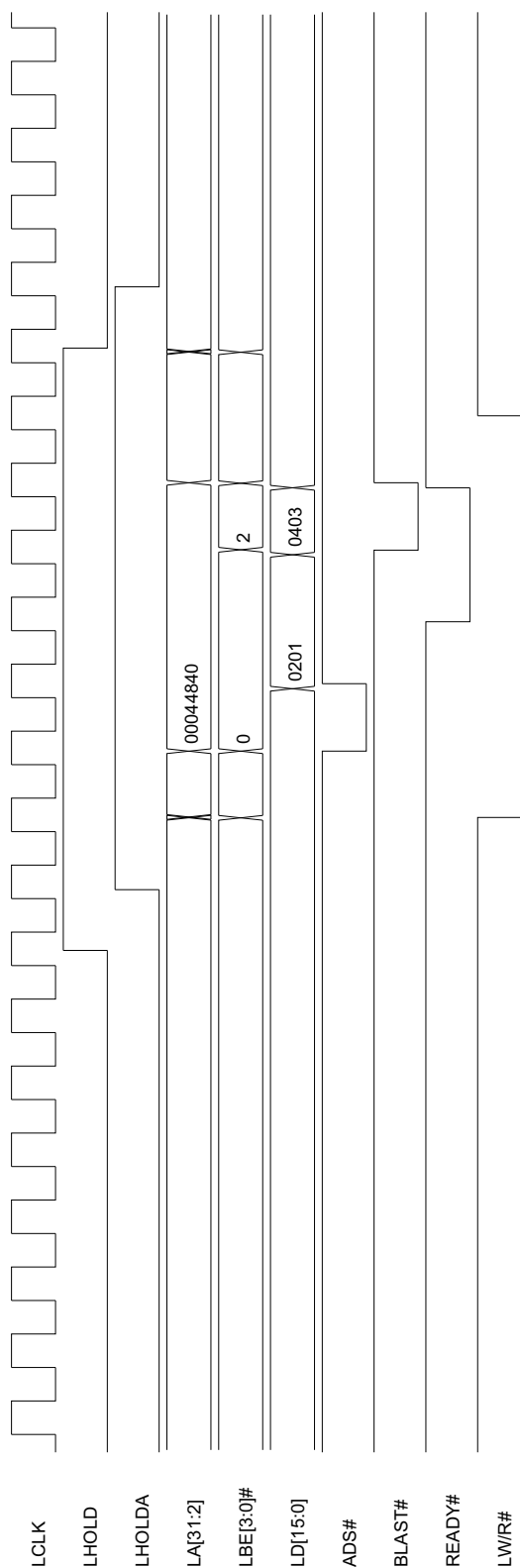
Note: *Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=1541h.*

Timing Diagram 6-21. Direct Slave Single Cycle Read (32-Bit Local Bus)

LCLK

LHOLD

LHOLDA

LA[31:2]   00044000

LBE[3:0]#   0

LD[31:0]   04030201

ADS#

BLAST#

READY#

LW/R#
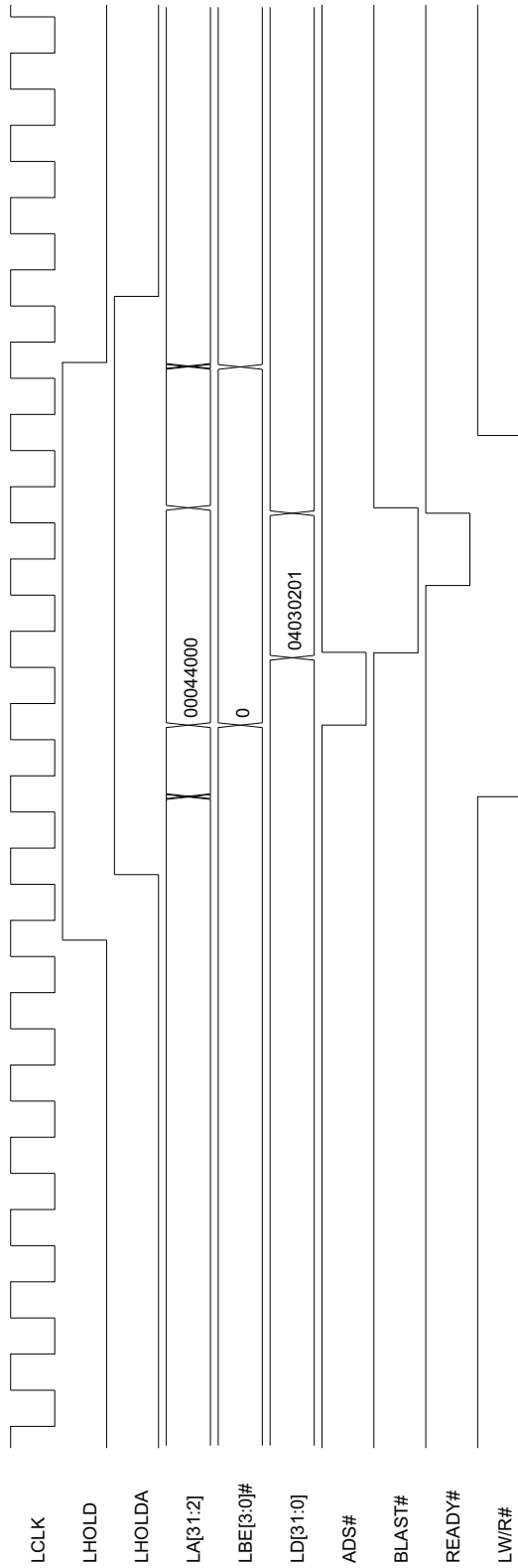
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=0D42h.

Timing Diagram 6-22. Direct Slave Burst Write of 4 Dwords (8-Bit Local Bus)
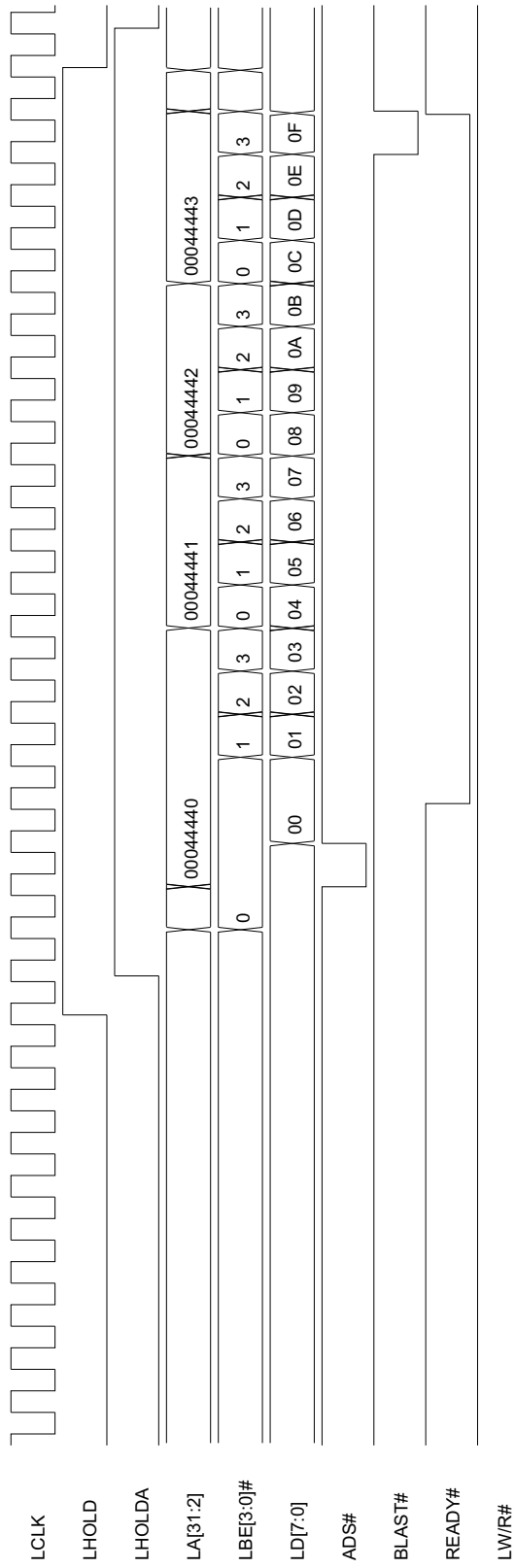
Note: *Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=25C0h.*

Timing Diagram 6-23. Direct Slave Burst Write of 4 Dwords (16-Bit Local Bus)

LCLK				
LHOLD				
LHOLDA				
LA[31:2]	00044840	00044841	00044842	00044843
LBE[3:0]#	0	2	2 0	2 0	2
LD[15:0]	0100	0302 0504	0706 0908	0B0A 0D0C	0F0E
ADS#				
BLAST#				
READY#				
LW/R#				
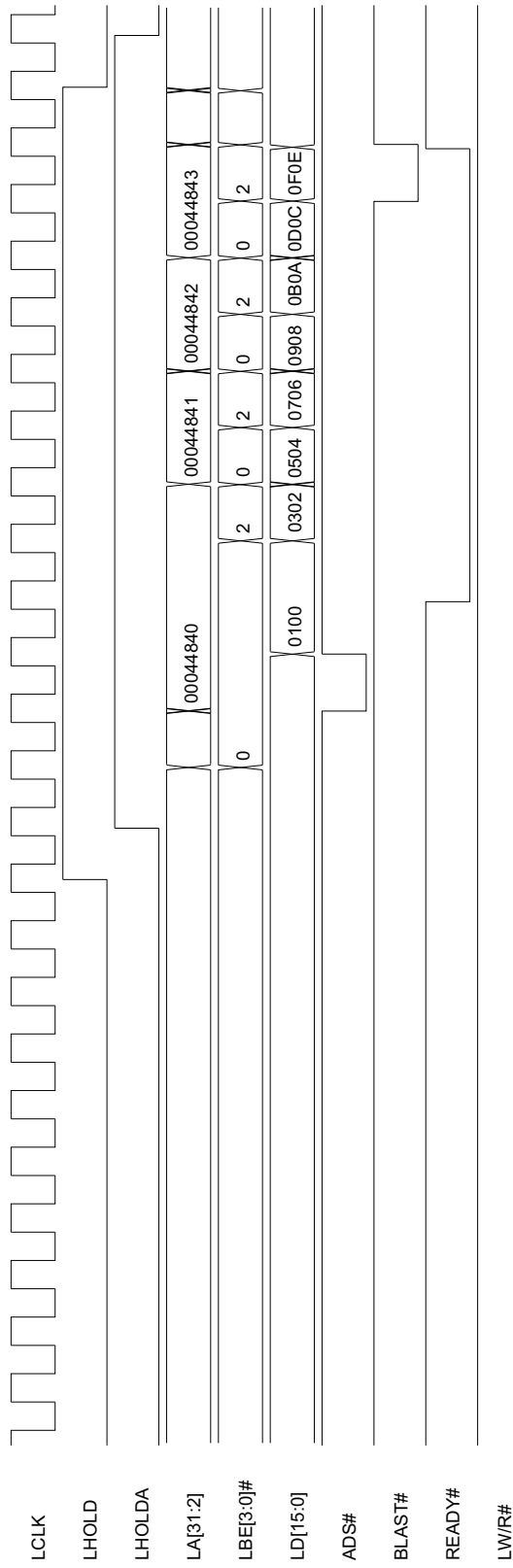
Note: Key bit/register values are LCS_MARBR[24]=1 and LCS_LBRD1[15:0]=25C1h.

Timing Diagram 6-24. Direct Slave Burst Write of 4 Dwords (32-Bit Local Bus)

LCLK

LHOLD

LHOLDA

LA[31:2]   00044000

LBE[3:0]#   0

LD[31:0]   03020100

ADS#

BLAST#

READY#

LW/R#
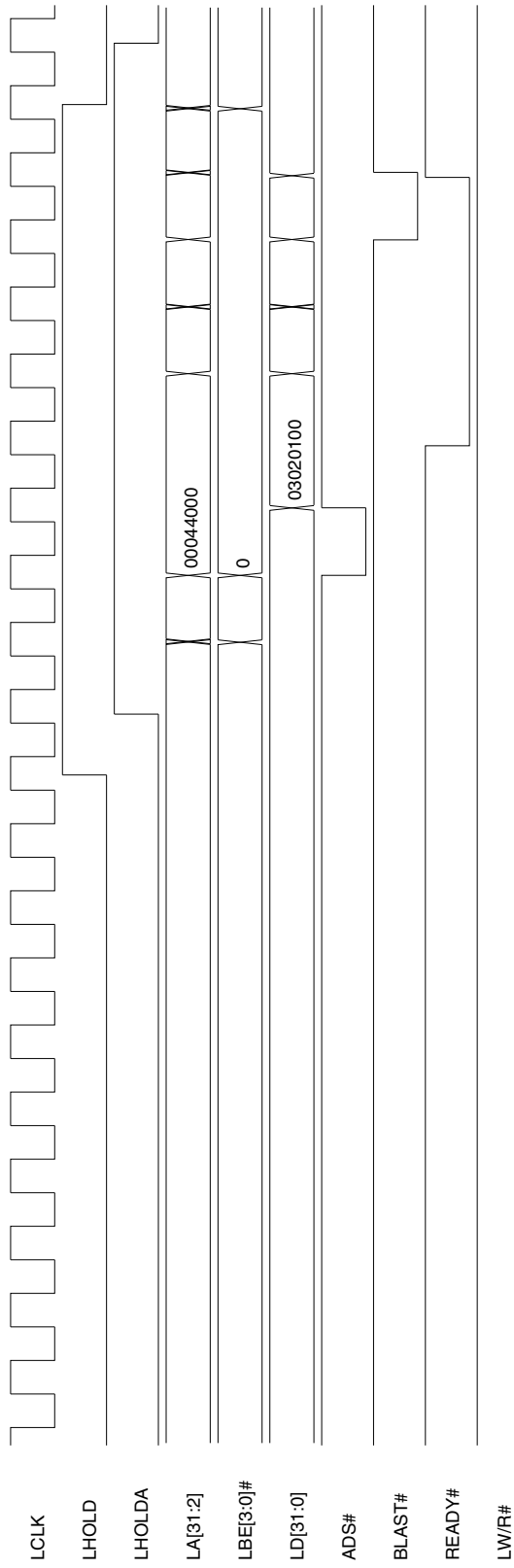
*Note: Key bit/register values are **LCS_MARBR**[24]=0 and **LCS_LBRD1**[15:0]=25C2h.*

Timing Diagram 6-25. Direct Slave Burst Read of 4 Dwords (8-Bit Local Bus)

LCLK
LHOLD
LHOLDA
LA[31:2]
LBE[3:0]#
LD[7:0]
ADS#
BLAST#
READY#
LW/R#
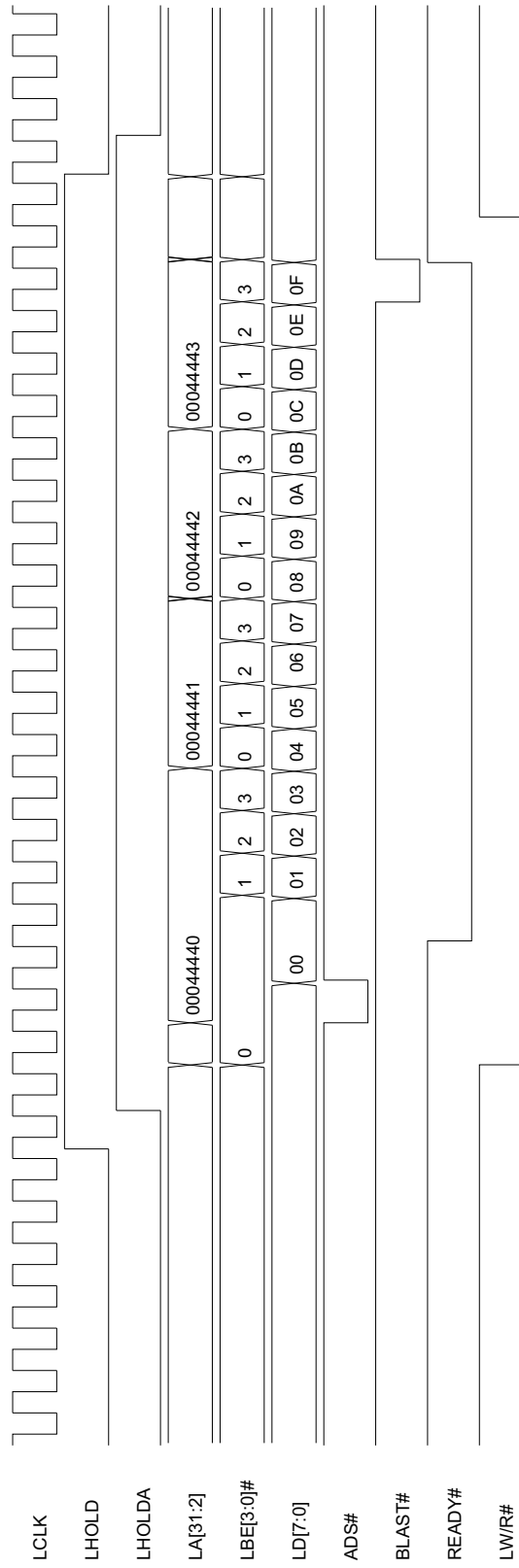
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=25C0h.

Timing Diagram 6-26. Direct Slave Burst Read of 4 Dwords (16-Bit Local Bus)
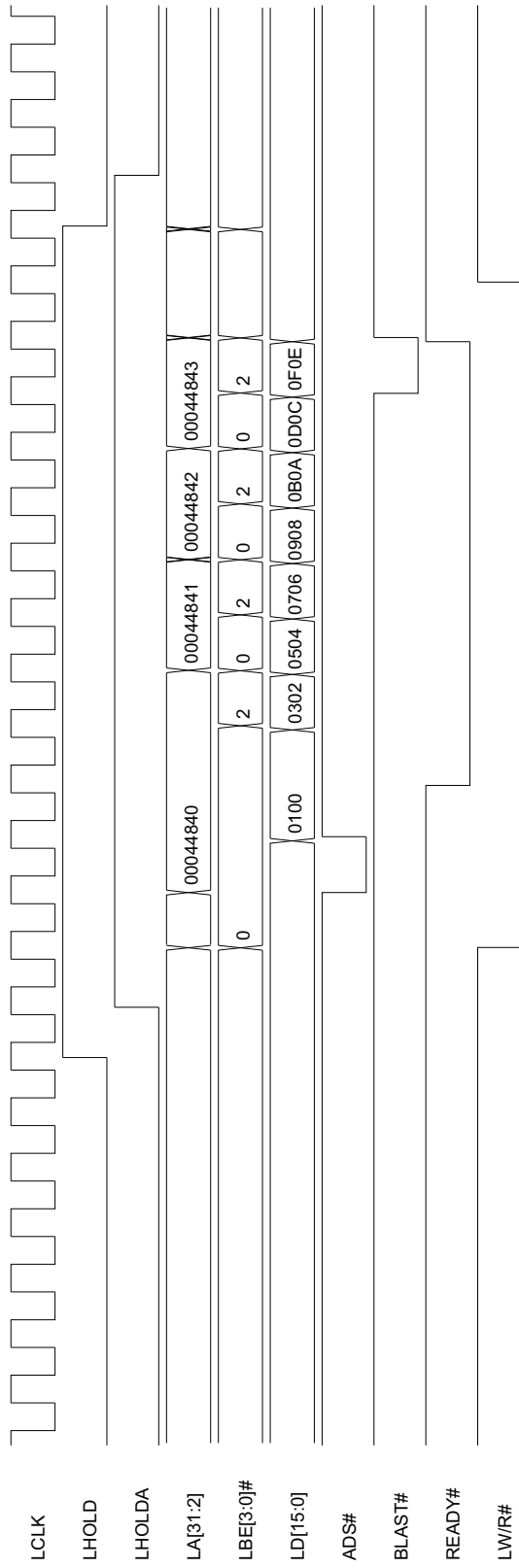
Note: Key bit/register values are LCS_MARBR[24]=1 and LCS_LBRD1[15:0]=25C1h.

Timing Diagram 6-27. Direct Slave Burst Read of 4 Dwords (32-Bit Local Bus)

LCLK	
LHOLD	
LHOLDA	
LA[31:2]	00044000
LBE[3:0]#	0
LD[31:0]	03020100
ADS#	
BLAST#	
READY#	
LW/R#	
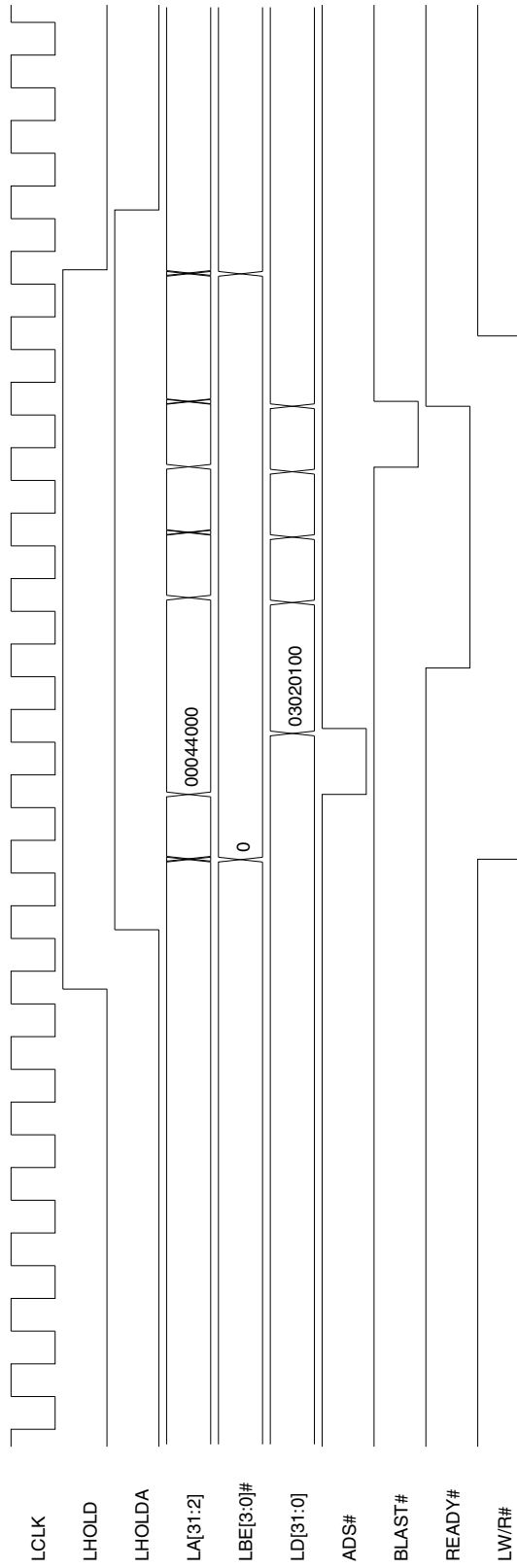
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=25C2h.

6.5.3   C Mode DMA Timing Diagrams

Timing Diagram 6-28. DMA PCI Express-to-Local (32-Bit Local Bus)
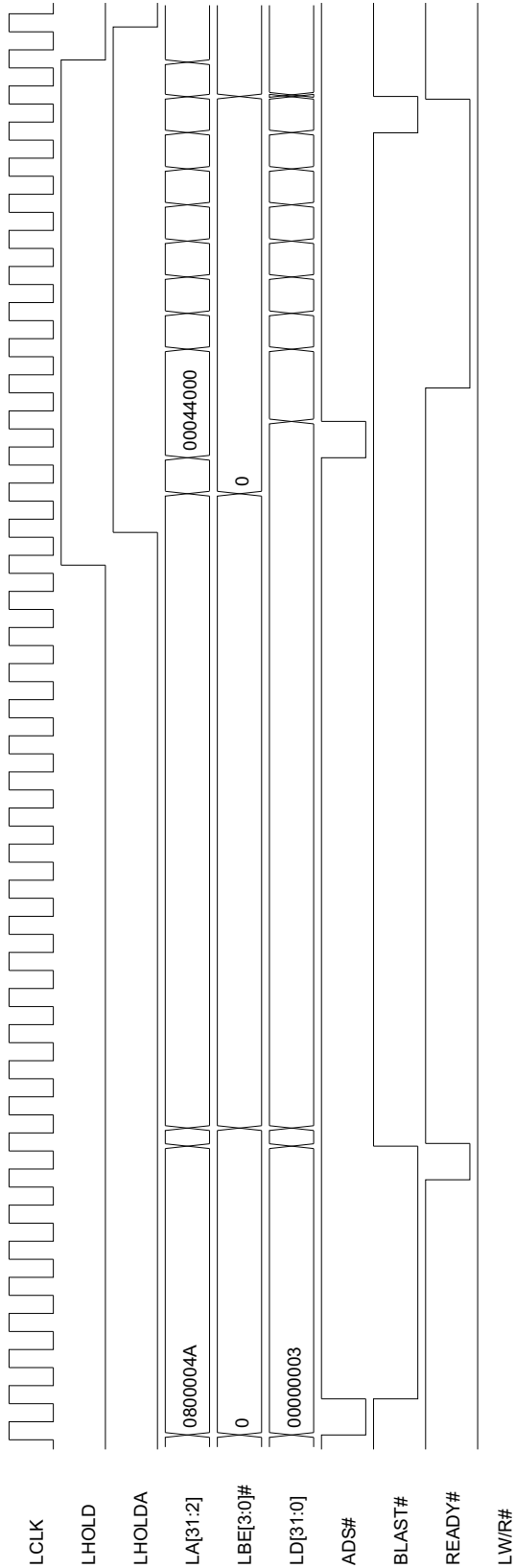
Notes: *The writing of the registers, to set up this 32-byte DMA Block mode transfer using DMA Channel 0/1, is not shown.*

Writing the LCS_DMACSR0/1 register (LOC:128h/LOC:129h) with 03h enables and starts this DMA transfer.

Timing Diagram 6-29. DMA Local-to-PCI Express (32-Bit Local Bus)
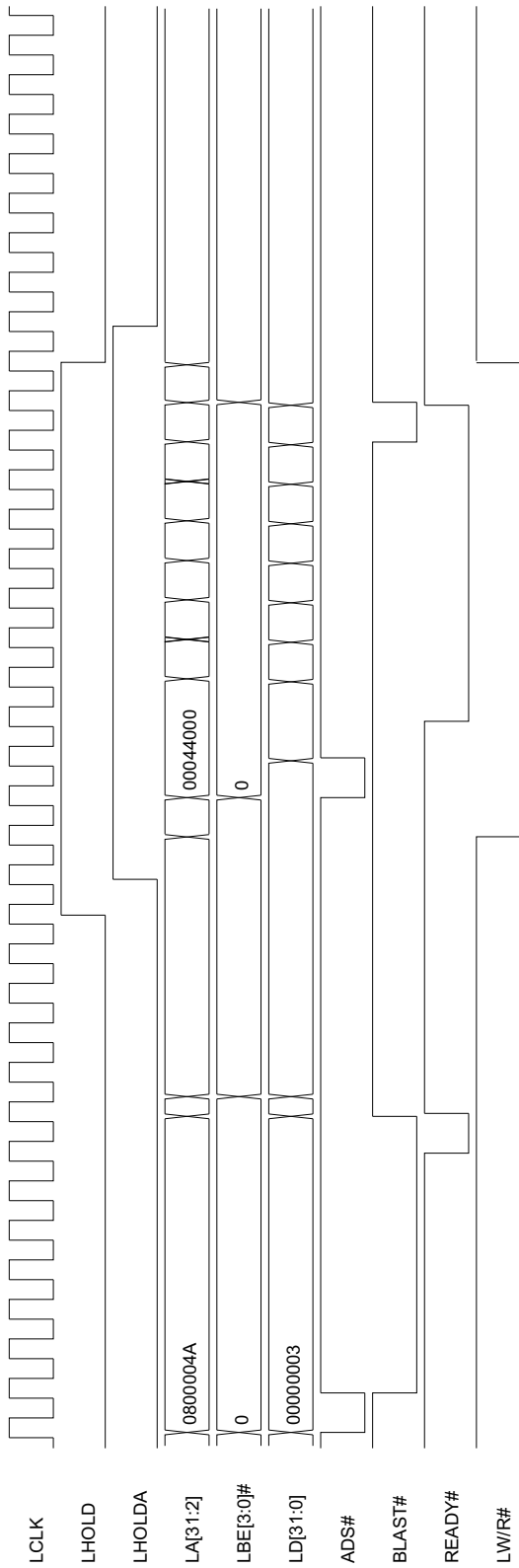
Notes: *The writing of the registers to set up this 32-byte DMA Block mode transfer using DMA Channel 0/1 is not shown.*

Writing the LCS_DMACSR0/1 register (LOC:128h/LOC:129h) with 03h enables and starts this DMA transfer.

Timing Diagram 6-30. DMA PCI Express-to-Local Demand Mode (32-Bit Local Bus)
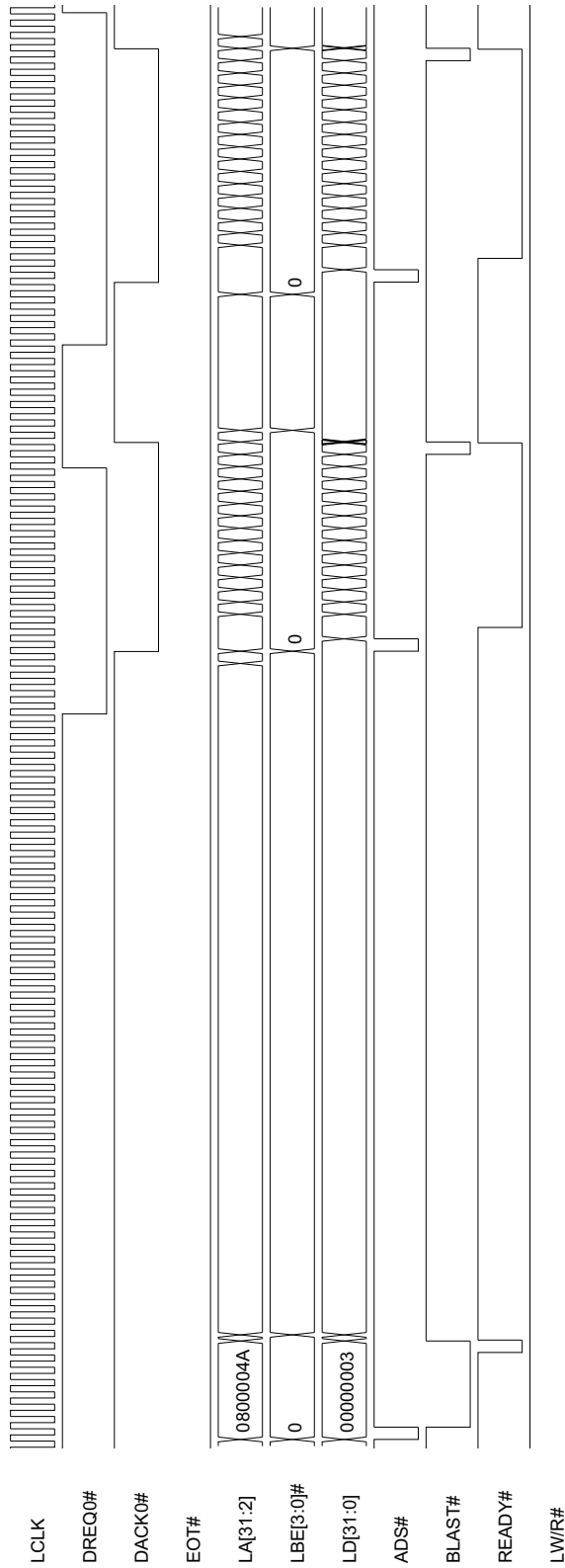
Notes: *The Channel 0/1 Demand mode DMA transfer starts when the* **LCS_DMACSR0/1[1:0]** *bits are written to 11b.*

The PEX 8311 does not attempt to arbitrate for and Write data to the Local Bus until it detects that DREQx# is asserted.

The transfer is temporarily suspended when DREQx# is de-asserted, then resumed upon its re-assertion.

Timing Diagram 6-31. DMA Local-to-PCI Express Demand Mode (32-Bit Local Bus)
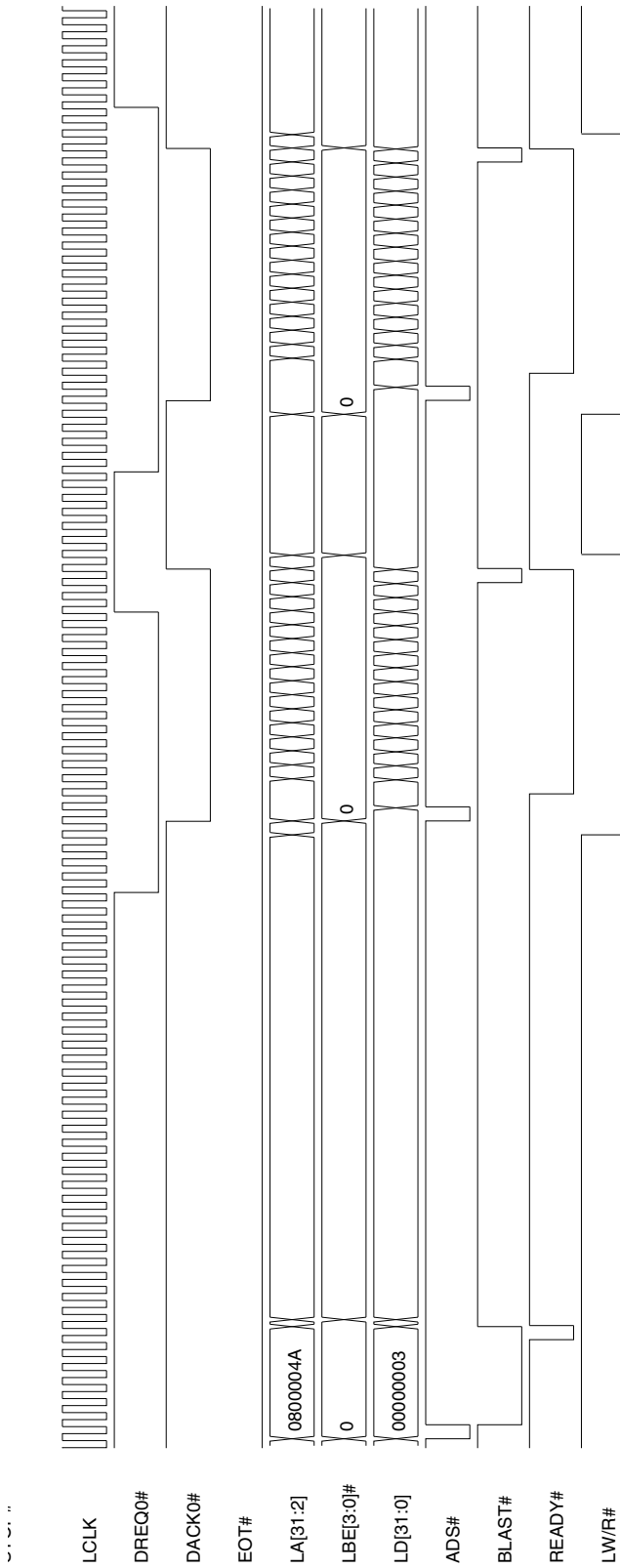
Note: *The Channel 0/1 Demand mode DMA transfer starts when the* **LCS_DMACSR0/1**[1:0] *bits are written to 11b and the PEX 8311 detects that DREQx# is asserted. Once started, the PEX 8311 arbitrates for and Reads data from the Local Bus, then Writes the data to the internal PCI Bus until the transfer is temporarily suspended when DREQx# is de-asserted. The transfer resumes upon DREQx# re-assertion.*

Timing Diagram 6-32. DMA Local-to-PCI Express Demand Mode with EOT# Assertion (32-Bit Local Bus)
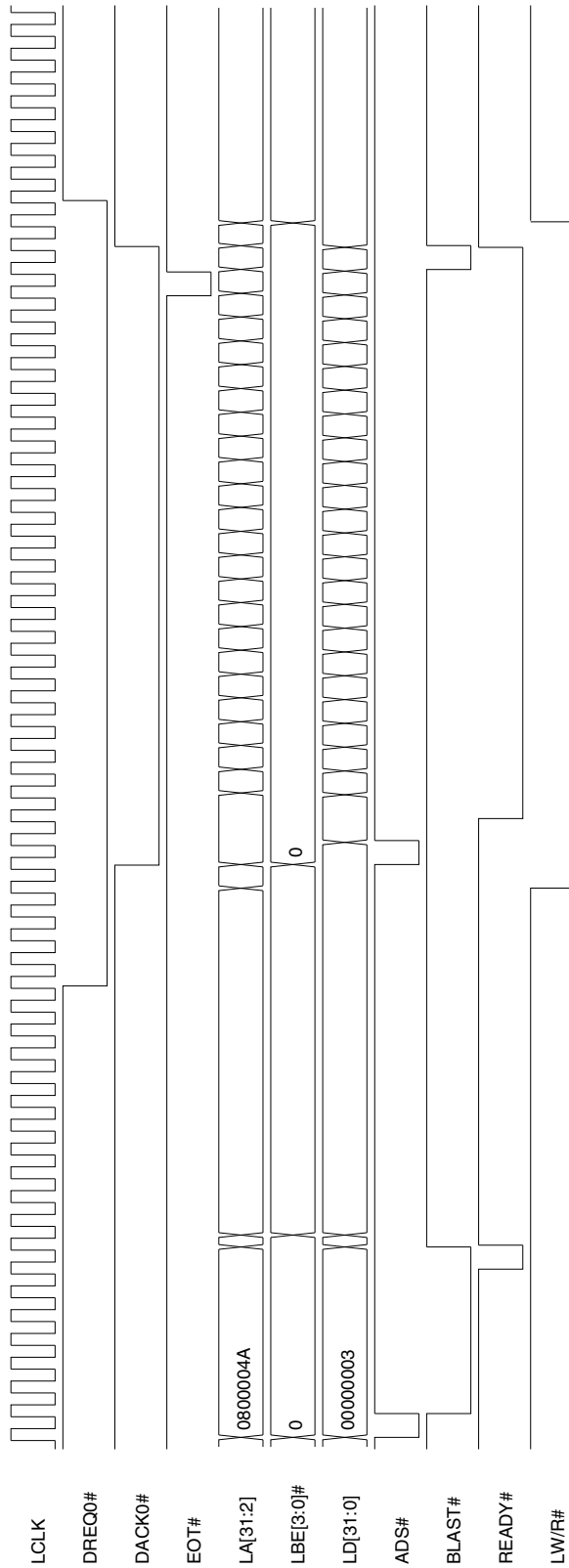
Signal	Value
LCLK	
DREQ0#	
DACK0#	
EOT#	
LA[31:2]	0800004A
LBE[3:0]#	0
LD[31:0]	00000003
ADS#	
BLAST#	
READY#	
LW/R#	

Notes: *The Channel 0/1 Demand mode DMA transfer starts when the* **LCS_DMACSR0/1**[1:0] *bits are written to 11b and the PEX 8311 detects that DREQx# is asserted. Once started, the PEX 8311 arbitrates for and Reads data from the Local Bus, then Writes the data to the internal PCI Bus until the transfer is terminated with an EOT# assertion. Data read into the DMA FIFO is written to the internal PCI Bus.*

6.6   J Mode Functional Timing Diagrams

6.6.1   J Mode Direct Master Timing Diagrams

Timing Diagram 6-33. Direct Master Single Cycle Write
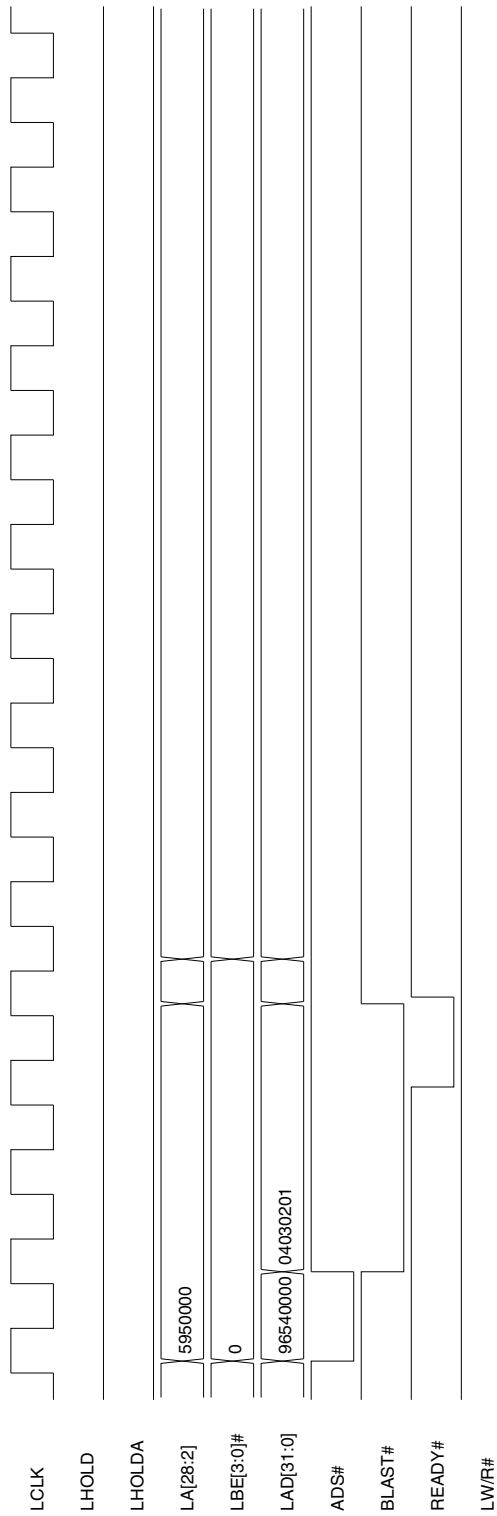
Note: Key register value is LCS_DMPBAM[15:0]=00E3h.

Timing Diagram 6-34. Direct Master Single Cycle Read

LCLK

LHOLD

LHOLDA

LA[28:2]   5950000

LBE[3:0]#   0

LAD[31:0]   DATA

ADS#

BLAST#

READY#

LW/R#
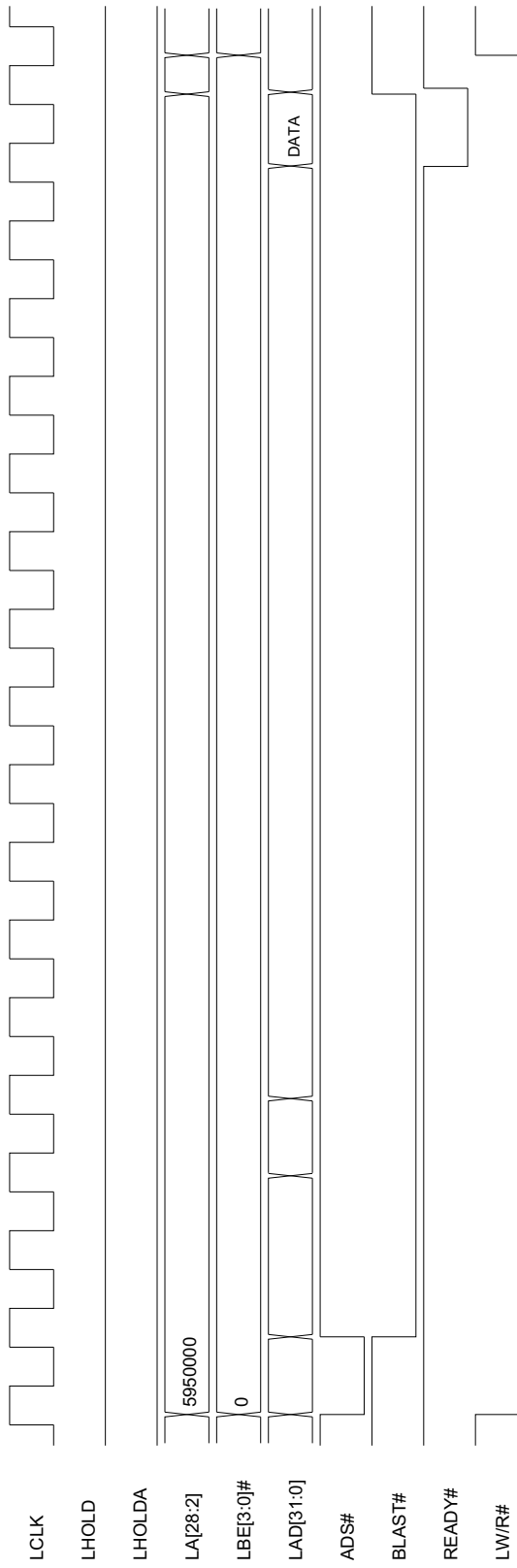
Note: Key register value is LCS_DMPBAM[15:0]=00E3h.

Timing Diagram 6-35. Direct Master Burst Write of 8 Dwords

LCLK

LHOLD

LHOLDA

LA[28:2]   5950000

LBE[3:0]#   0

LAD[31:0]   03020100

ADS#

BLAST#

READY#

LW/R#
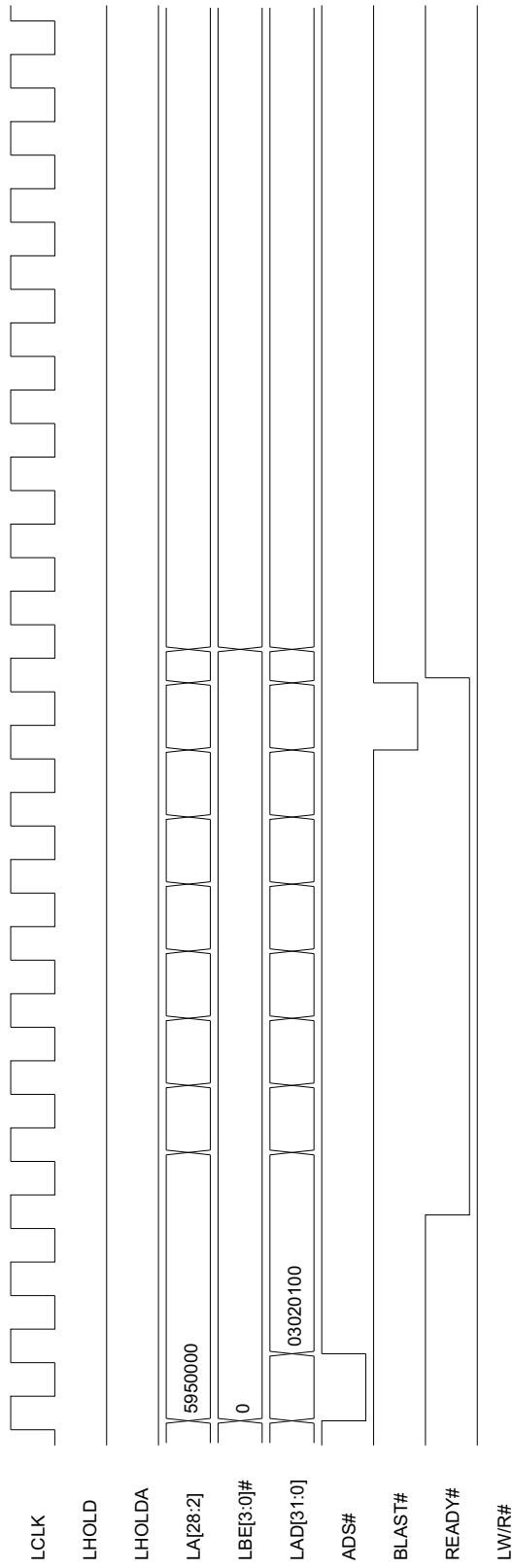
Note: Key register value is LCS_DMPBAM[15:0]=0007h.

Timing Diagram 6-36. Direct Master Burst Read of 8 Dwords

LCLK

LHOLD

LHOLDA

LA[28:2]   5950000

LBE[3:0]#   0

LAD[31:0]

ADS#

BLAST#

READY#

LW/R#
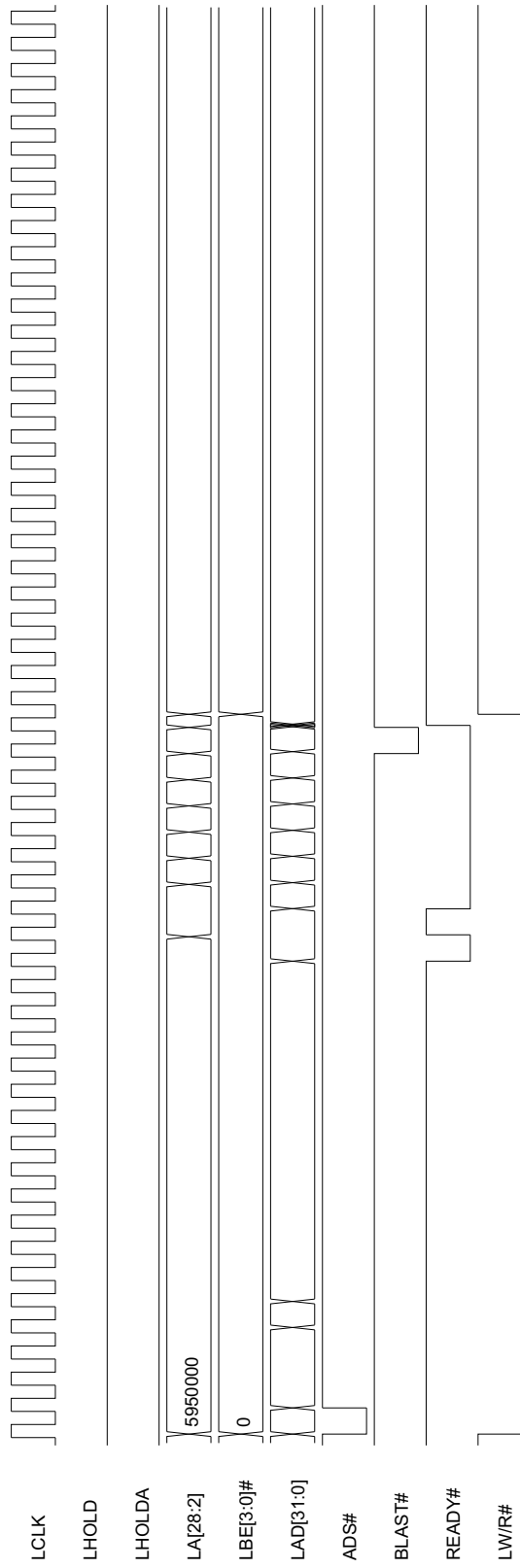
Note: Key register value is LCS_DMPBAM[15:0]=0007h.

6.6.2   J Mode Direct Slave Timing Diagrams

Timing Diagram 6-37. Direct Slave Burst Write Suspended by Single Cycle BREQi

LCLK
LHOLD
LHOLDA
LA[28:2]   0044000   0044006
LBE[3:0]#   0   0
LAD[31:0]
ADS#
ALE
BLAST#
READY#
LW/R#
BREQi
BTERM#

Notes: *This 9-Dword Direct Slave Burst Write transfer is suspended by a single-Clock cycle BREQi assertion.*
        The remaining 3 Dwords are transferred after the PEX 8311 is granted the Local Bus again.

        Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=45C2h.

Timing Diagram 6-38. Direct Slave Burst Write Suspended by Multi-Cycle BREQi

LCLK

LHOLD

LHOLDA

LA[28:2]   0044000   0044006   0044009

LBE[3:0]#   0   0   0

LAD[31:0]

ADS#

ALE

BLAST#

READY#

LW/R#

BREQi

BTERM#

Notes: *This 14-Dword Direct Slave Burst Write transfer is suspended twice by a multi-Clock cycle BREQi assertion.*

   Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=45C2h.

Timing Diagram 6-39. Direct Slave Burst Write Interrupted by Single Cycle BTERM#
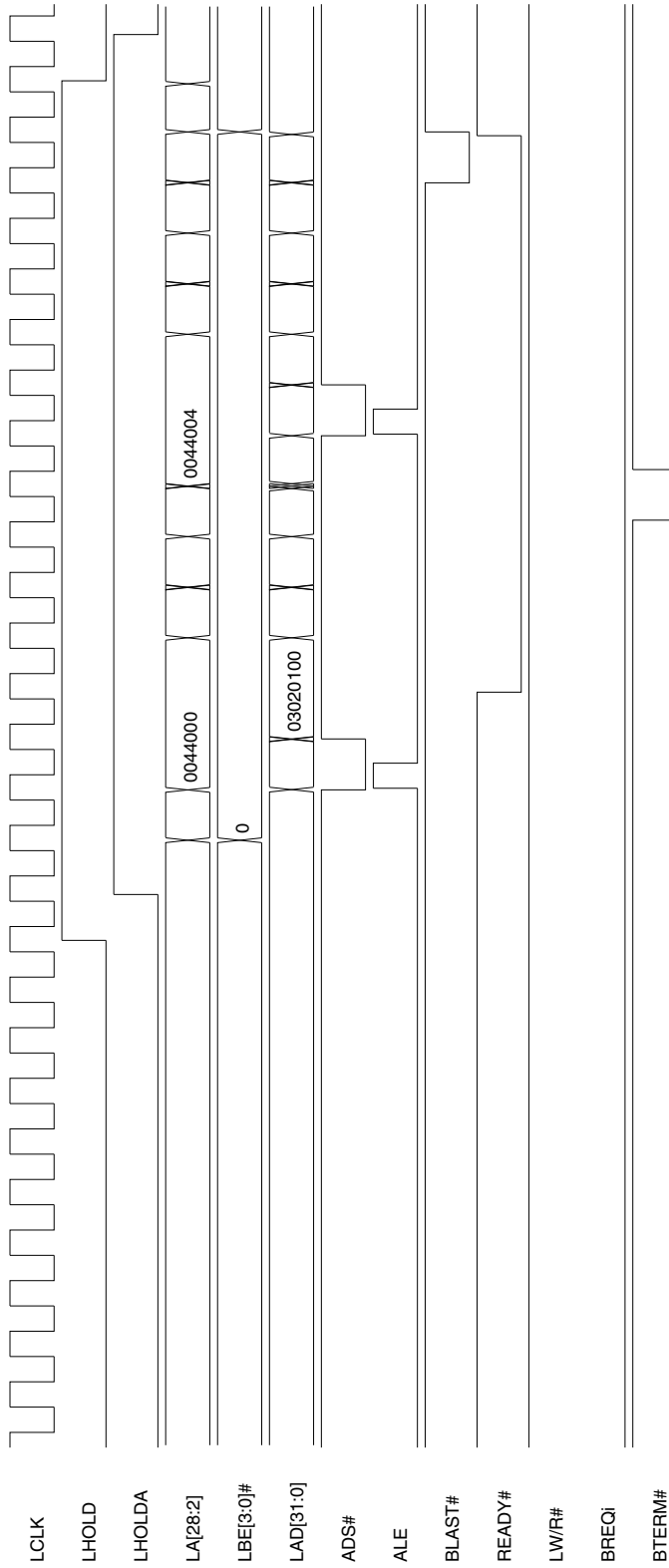
LCLK

LHOLD

LHOLDA

LA[28:2]   0044000   0044004

LBE[3:0]#   0

LAD[31:0]   03020100

ADS#

ALE

BLAST#

READY#

LW/R#

BREQi

BTERM#

Notes: *This 9-Dword Direct Slave Burst Write transfer is interrupted by a single-Clock cycle BTERM# assertion.*
After the Address cycle is generated as a result of BTERM# assertion, the fifth Dword of the transfer
is re-written, and the four remaining Dwords are written to complete the transfer.

Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRDI[15:0]=45C2h.

Timing Diagram 6-40. Direct Slave Burst Write Interrupted by Multi-Cycle BTERM#
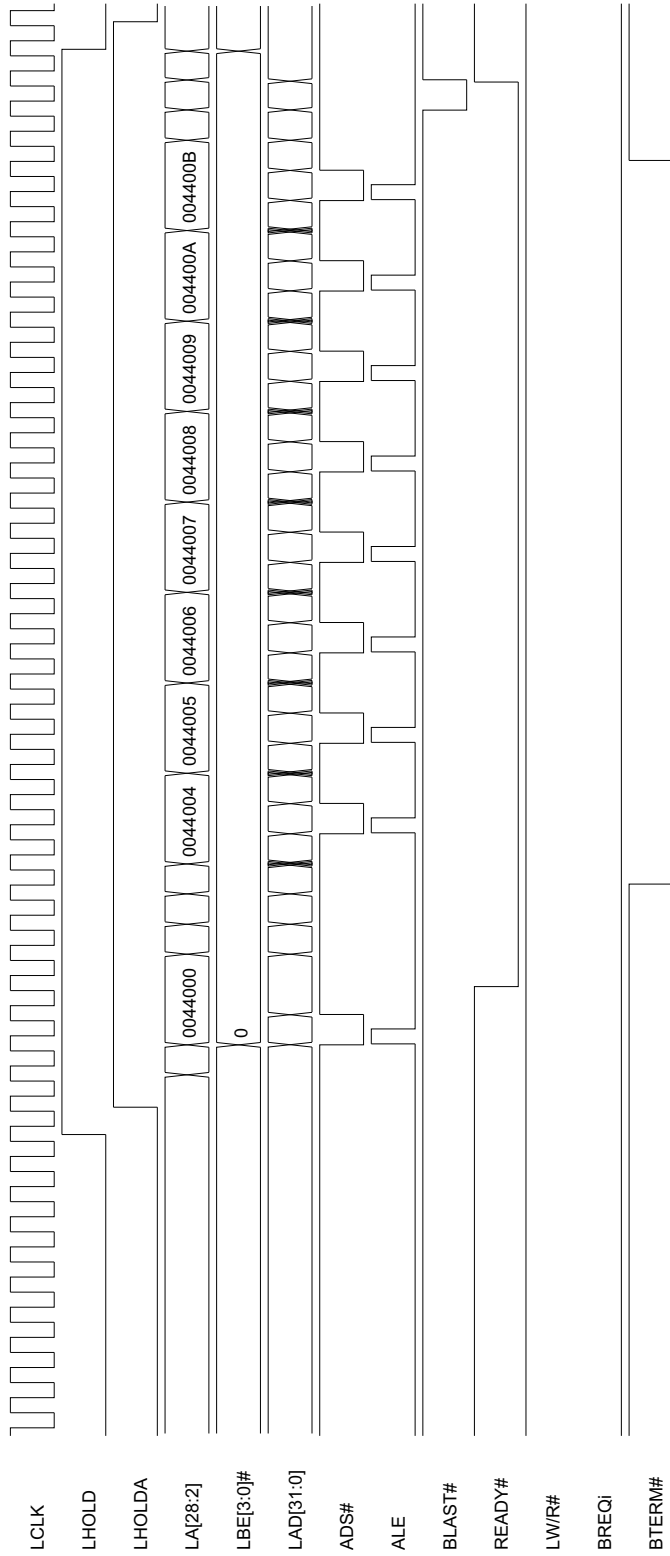
| LCLK |
| LHOLD |
| LHOLDA |
| LA[28:2] |
| LBE[3:0]# |
| LAD[31:0] |
| ADS# |
| ALE |
| BLAST# |
| READY# |
| LW/R# |
| BREQi |
| BTERM# |

Notes: *This 14-Dword Direct Slave Burst Write transfer is interrupted multiple times by a multi-Clock cycle BTERM# assertion. Six Dwords are written once and 8 Dwords are written a second time for each new Address phase generated.*

Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=45C2h.

Timing Diagram 6-41. Direct Slave Single Cycle Write (8-Bit Local Bus)
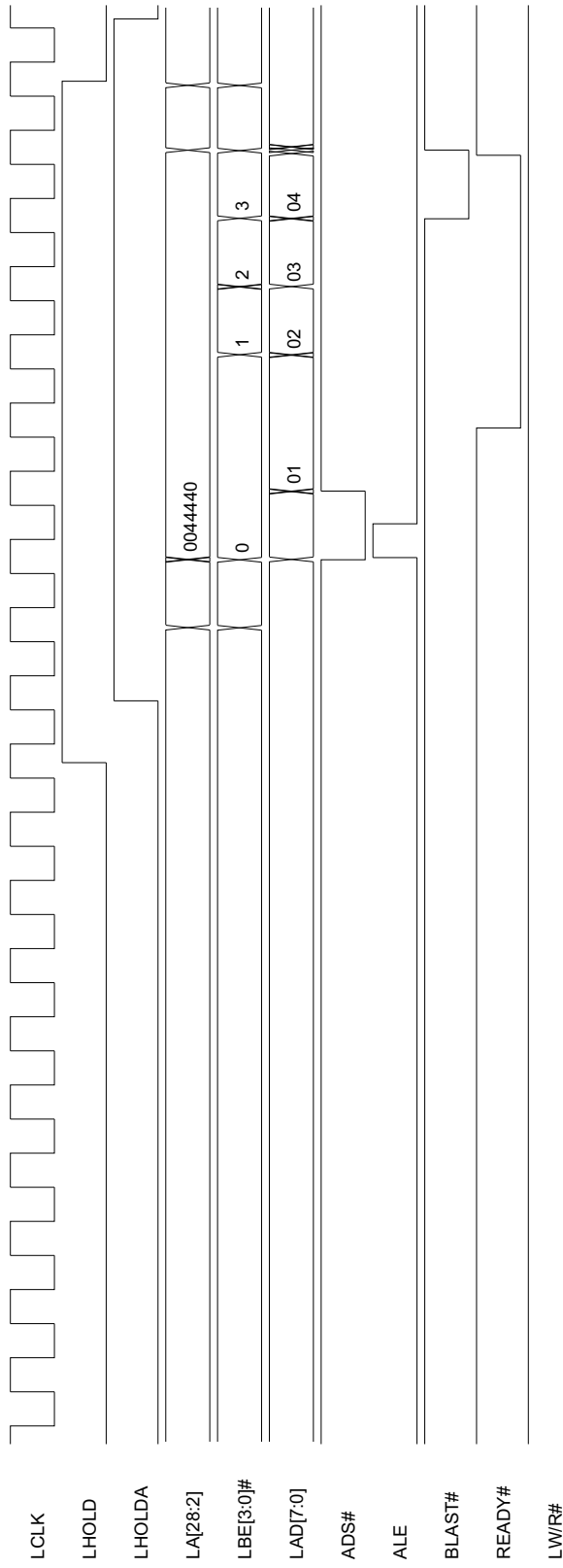
Note: Key bit/register values are LCS_MARBR[24]=1 and LCS_LBRD1[15:0]=0D40h.

Timing Diagram 6-42. Direct Slave Single Cycle Write (16-Bit Local Bus)

LCLK

LHOLD

LHOLDA

LA[28:2]   0044840

LBE[3:0]#   0   2

LAD[15:0]   0201   0403

ADS#

ALE

BLAST#

READY#

LW/R#
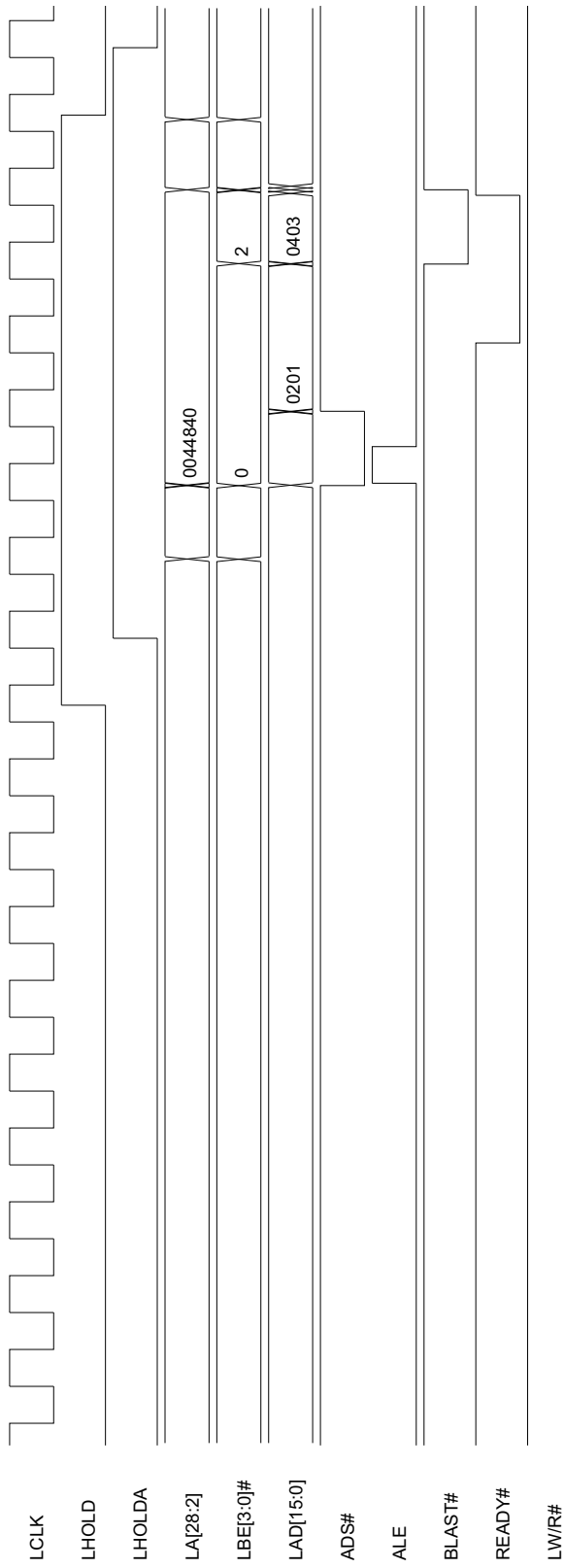
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=1541h.

Timing Diagram 6-43. Direct Slave Single Cycle Write (32-Bit Local Bus)
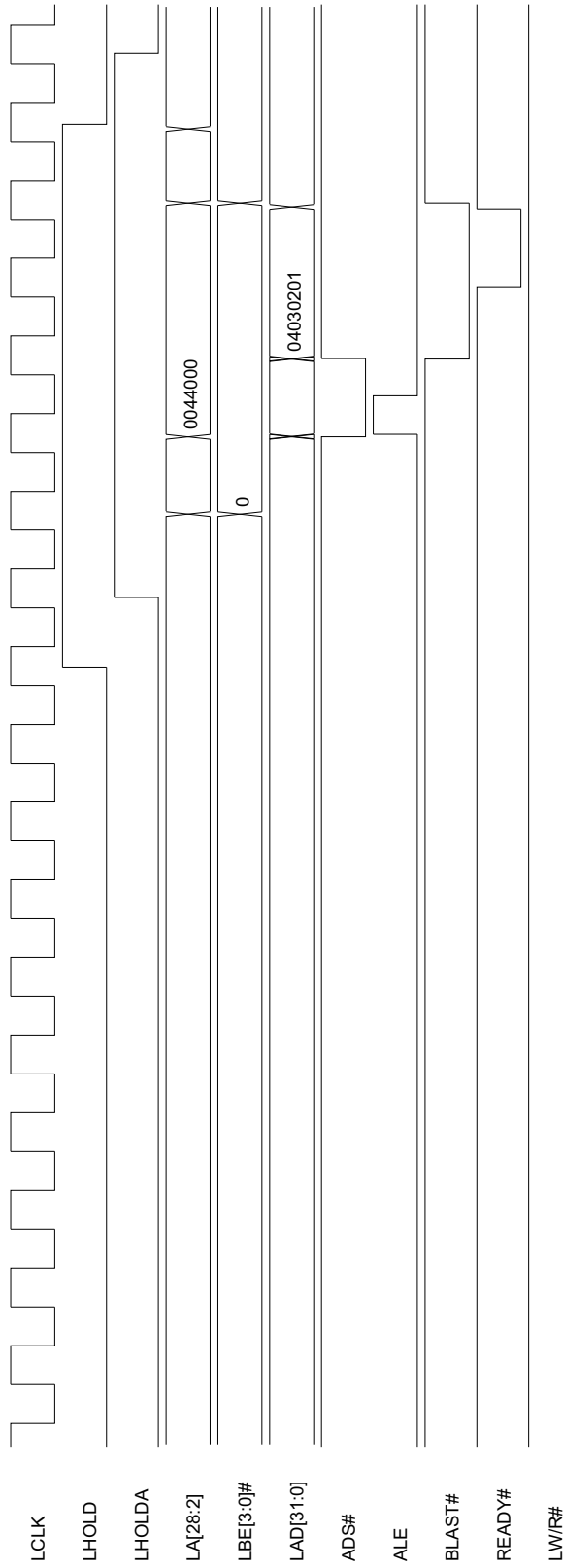
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=0D42h.

Timing Diagram 6-44. Direct Slave Single Cycle Read (8-Bit Local Bus)
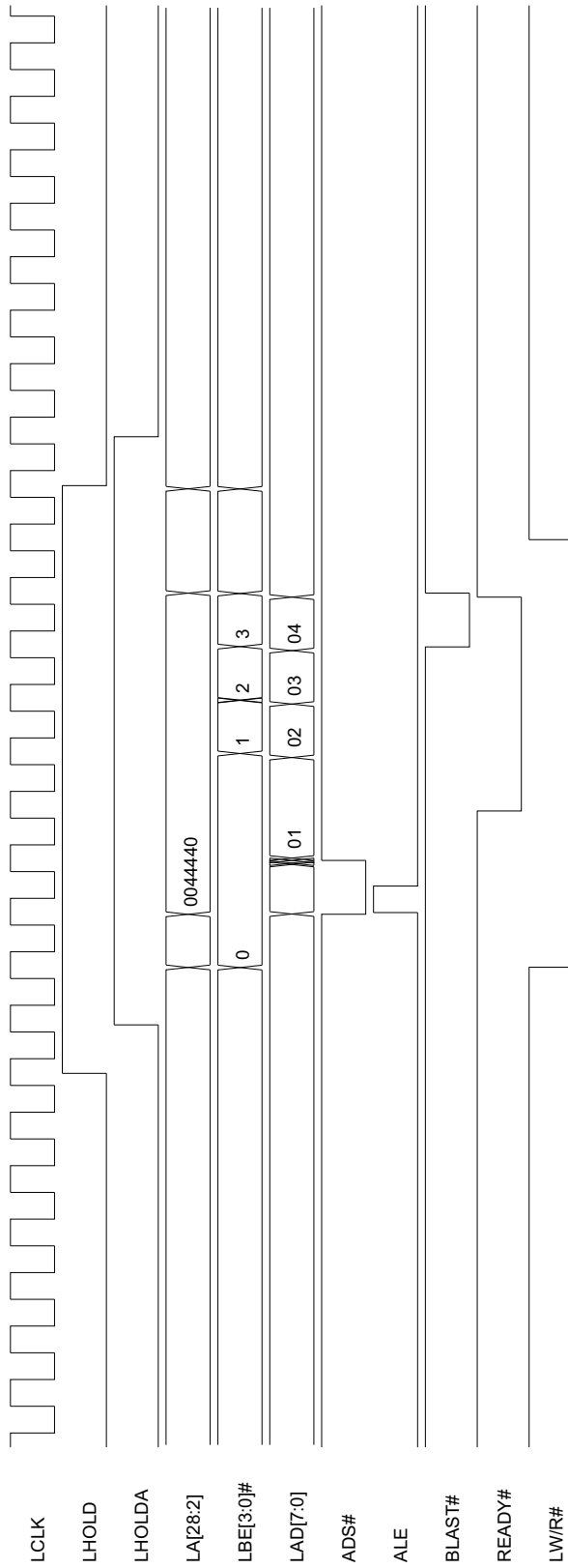
Note: *Key bit/register values are* *LCS_MARBR[24]=1 and* *LCS_LBRD1[15:0]=0D40h.*

Timing Diagram 6-45. Direct Slave Single Cycle Read (16-Bit Local Bus)

LCLK
LHOLD
LHOLDA
LA[28:2]
LBE[3:0]#
LAD[15:0]
ADS#
ALE
BLAST#
READY#
LW/R#
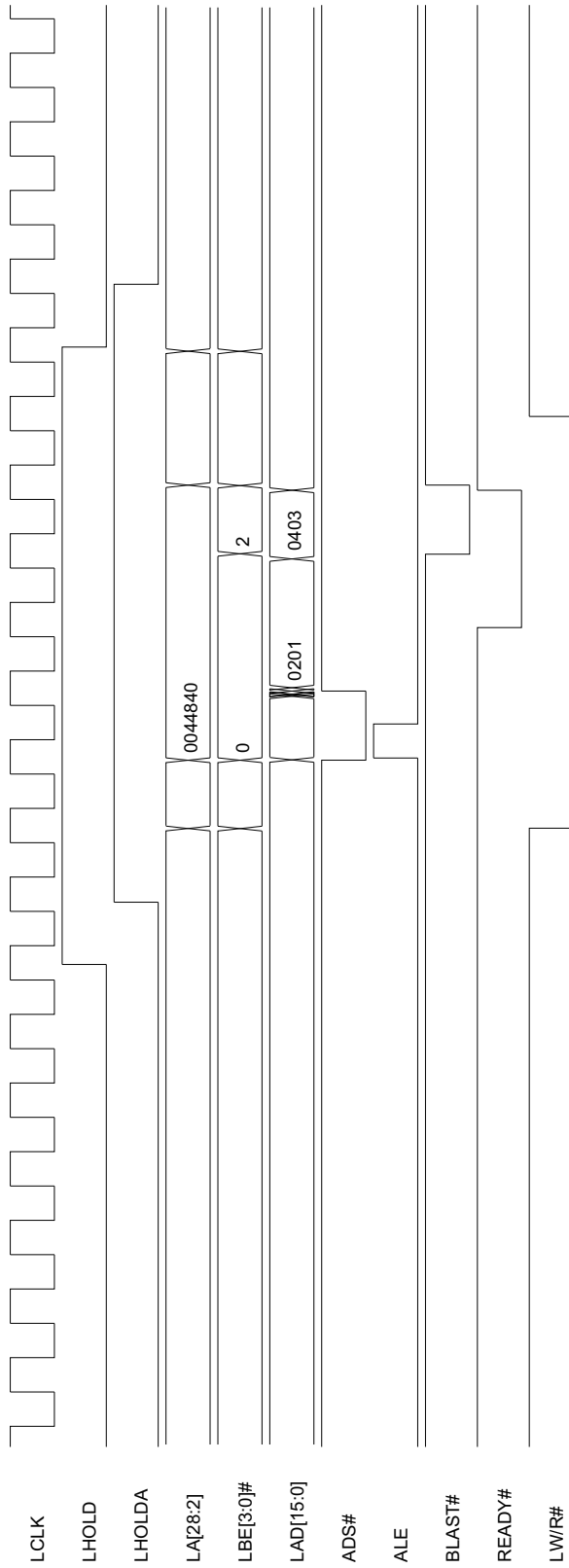
Note: *Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=1541h.*

Timing Diagram 6-46. Direct Slave Single Cycle Read (32-Bit Local Bus)

LCLK

LHOLD

LHOLDA

LA[28:2]   0044000

LBE[3:0]#   0

LAD[31:0]   04030201

ADS#

ALE

BLAST#

READY#

LW/R#
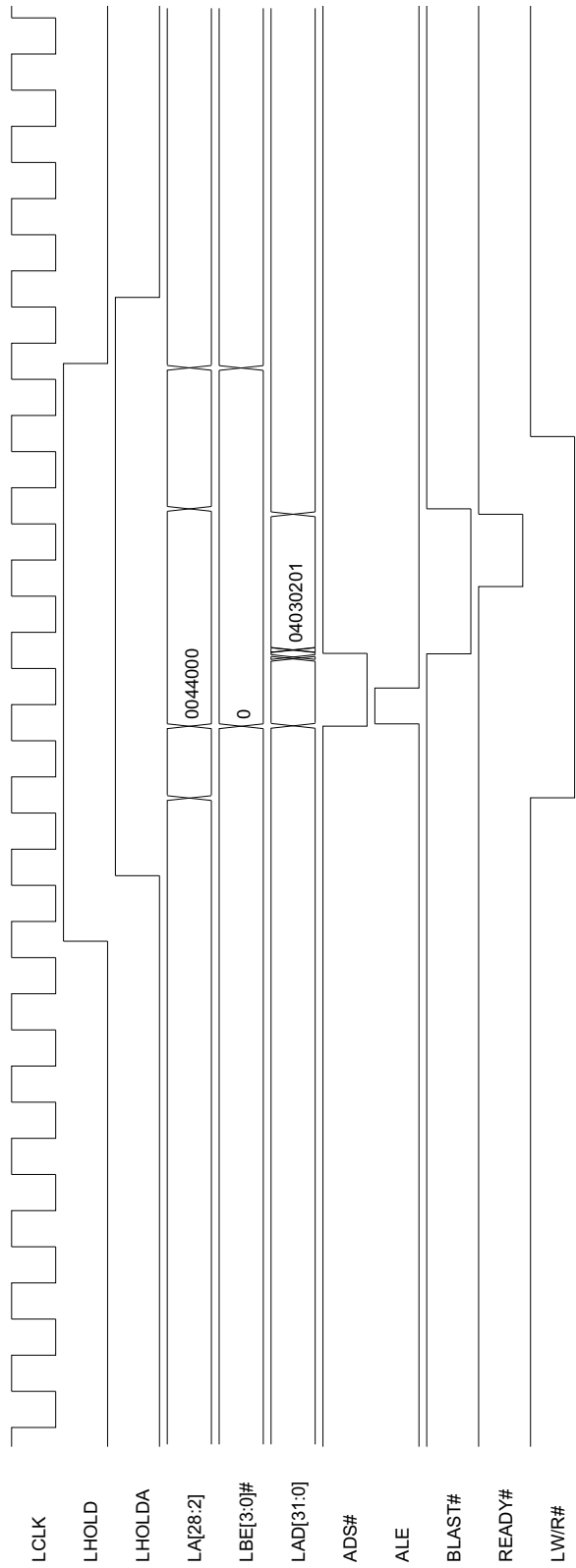
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=0D42h.

Timing Diagram 6-47. Direct Slave Burst Write of 4 Dwords (8-Bit Local Bus)
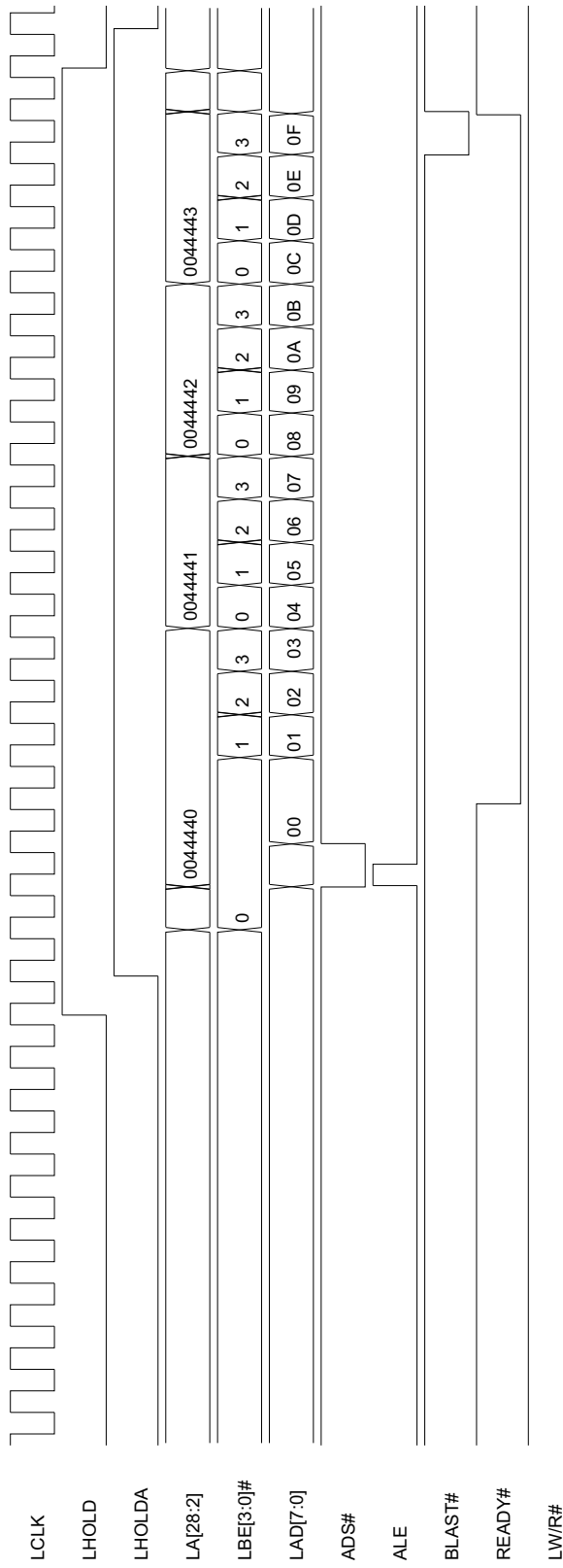
*Note: Key bit/register values are **LCS_MARBR**[24]=0 and **LCS_LBRD1**[15:0]=25C0h.*

Timing Diagram 6-48. Direct Slave Burst Write of 4 Dwords (16-Bit Local Bus)
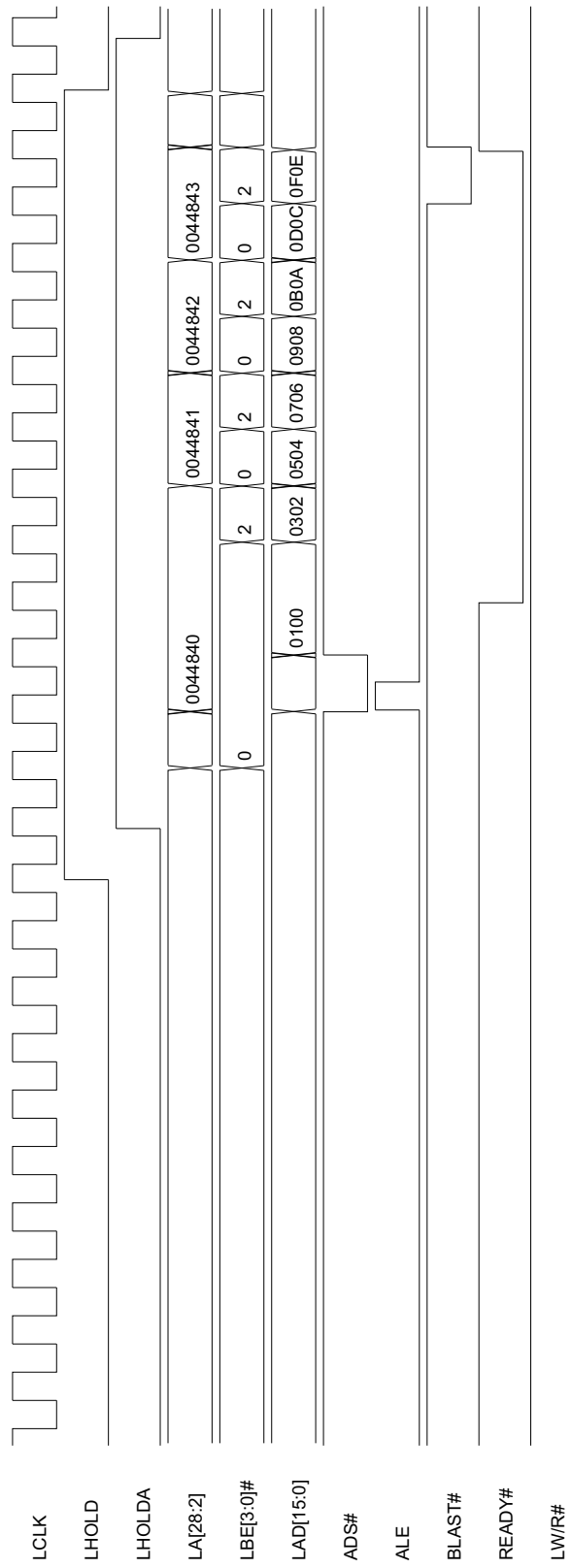
Note: *Key bit/register values are LCS_MARBR[24]=1 and LCS_LBRD1[15:0]=25C1h.*

Timing Diagram 6-49. Direct Slave Burst Write of 4 Dwords (32-Bit Local Bus)

LCLK	
LHOLD	
LHOLDA	
LA[28:2]	0044000
LBE[3:0]#	0
LAD[31:0]	03020100
ADS#	
ALE	
BLAST#	
READY#	
LW/R#	

Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=25C2h.

Timing Diagram 6-50. Direct Slave Burst Read of 4 Dwords (8-Bit Local Bus)

LCLK

LHOLD

LHOLDA

LA[28:2]   0044440   0044441   0044442   0044443

LBE[3:0]#   0   1 2 3   0 1 2 3   0 1 2 3   0 1 2 3

LAD[7:0]   01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F

ADS#

ALE

BLAST#

READY#

LW/R#
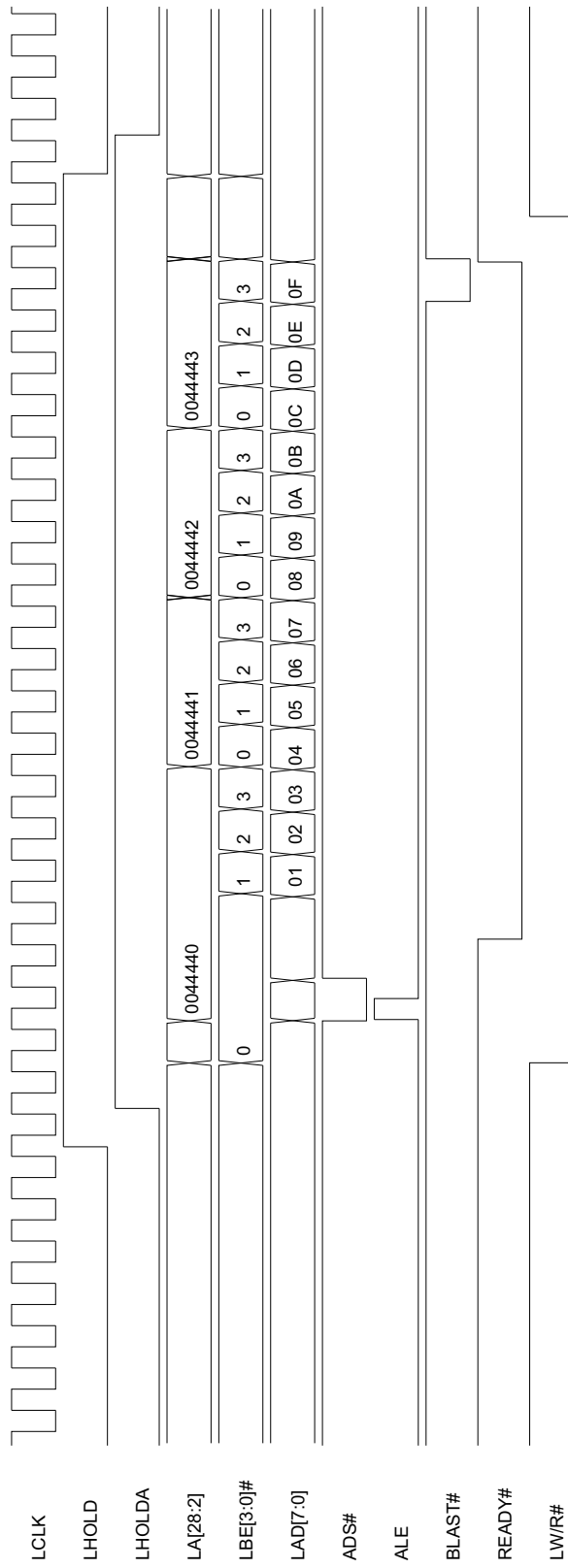
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=25C0h.

Timing Diagram 6-51. Direct Slave Burst Read of 4 Dwords (16-Bit Local Bus)
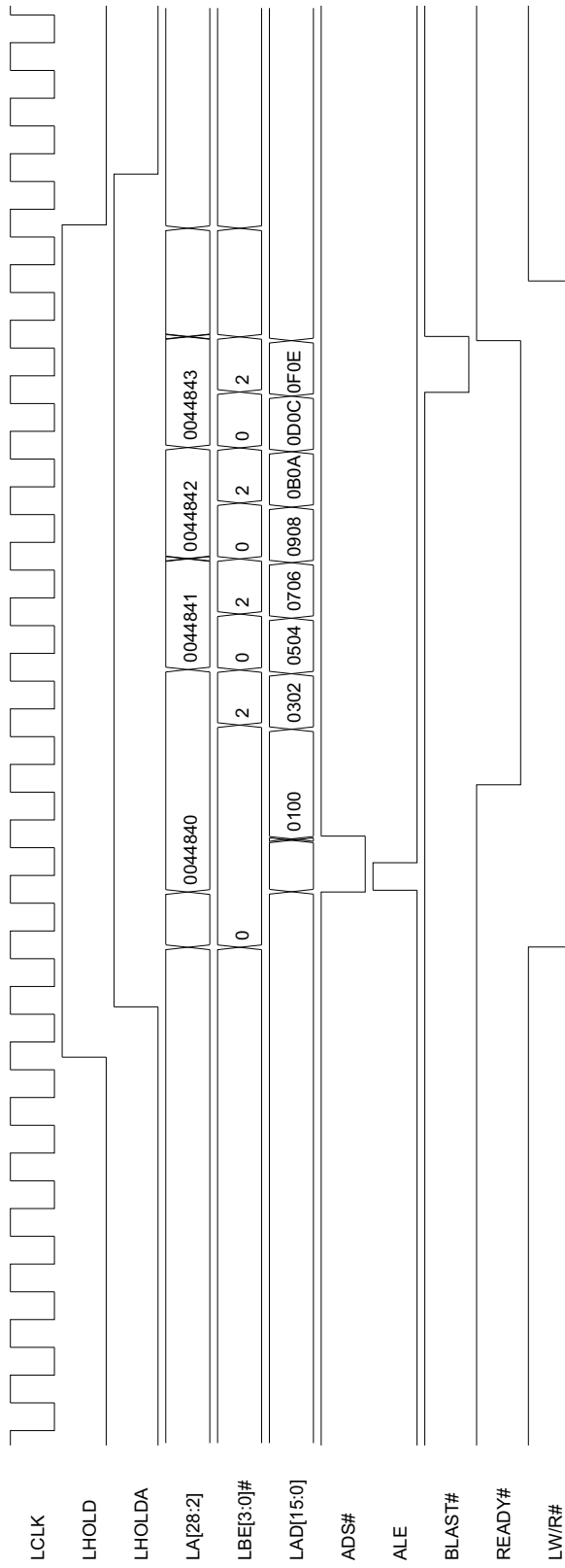
Note: Key bit/register values are LCS_MARBR[24]=1 and LCS_LBRD1[15:0]=25C1h.

Timing Diagram 6-52.   Direct Slave Burst Read of 4 Dwords (32-Bit Local Bus)

LCLK

LHOLD

LHOLDA

LA[28:2]   0044000

LBE[3:0]#   0

LAD[31:0]   03020100

ADS#

ALE

BLAST#

READY#

LW/R#
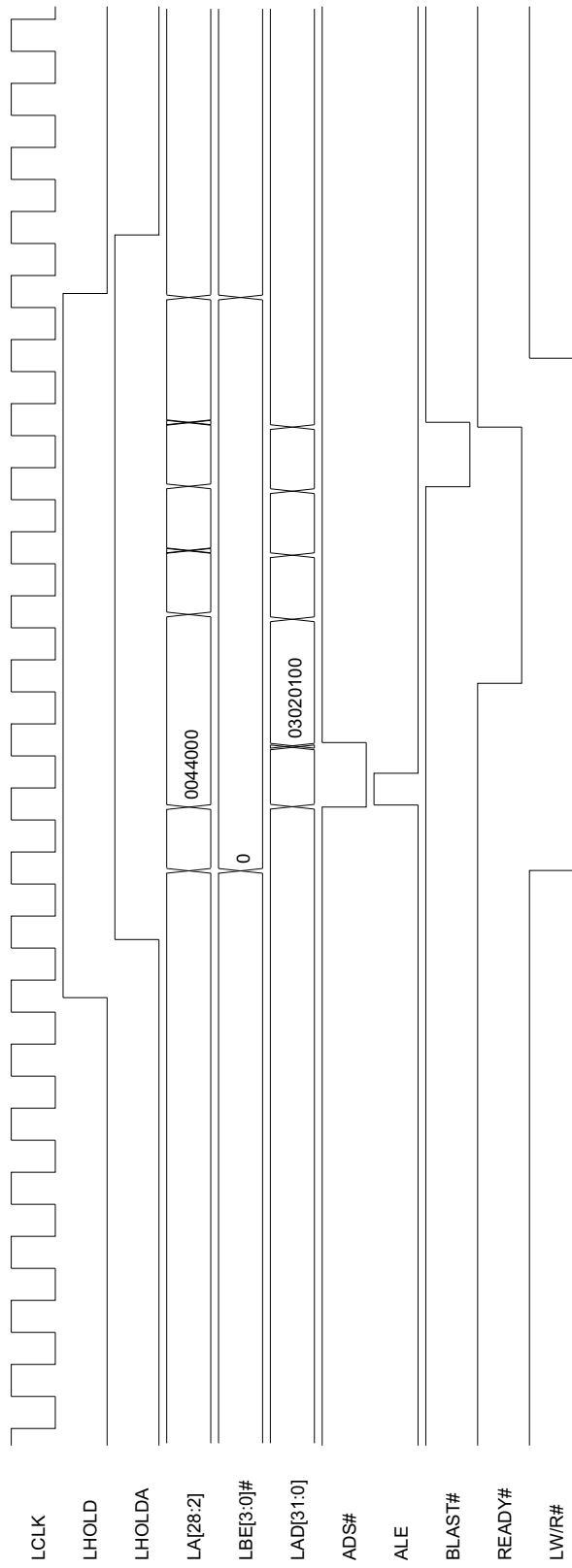
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRDI[15:0]=25C2h.

Timing Diagram 6-53. Direct Slave Write with DT/R# and DEN#
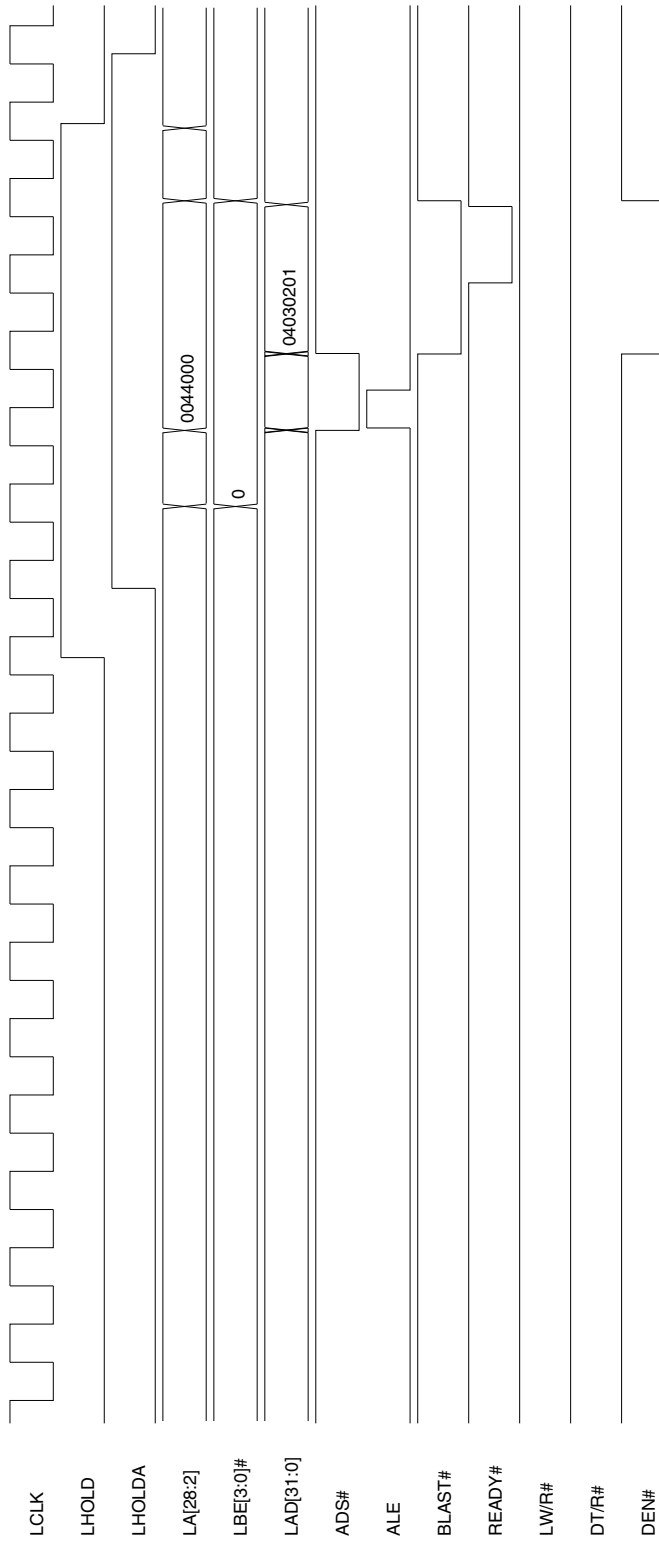
Note: *This single-cycle Direct Slave Write to a 32-bit Local Bus device/transceivers timing diagram includes the DT/R# and DEN# signals. The PEX 8311 always tri-states the DT/R# and DEN# signals, except during the time it owns the Local Bus (LHOLD and LHOLDA are asserted) to process a Direct Slave or DMA transfer. Because the DT/R# and DEN# signal balls are pulled up, they are seen as a 1 (High) in this diagram when the PEX 8311 is not driving them. DT/R# and DEN# can be ORed to create the DIR signal for the transceiver(s).*

Timing Diagram 6-54. Direct Slave Read with DT/R# and DEN#

LCLK

LHOLD

LHOLDA

LA[28:2]   0044000

LBE[3:0]#   0

LAD[31:0]   04030201

ADS#

ALE

BLAST#

READY#

LW/R#

DT/R#

DEN#
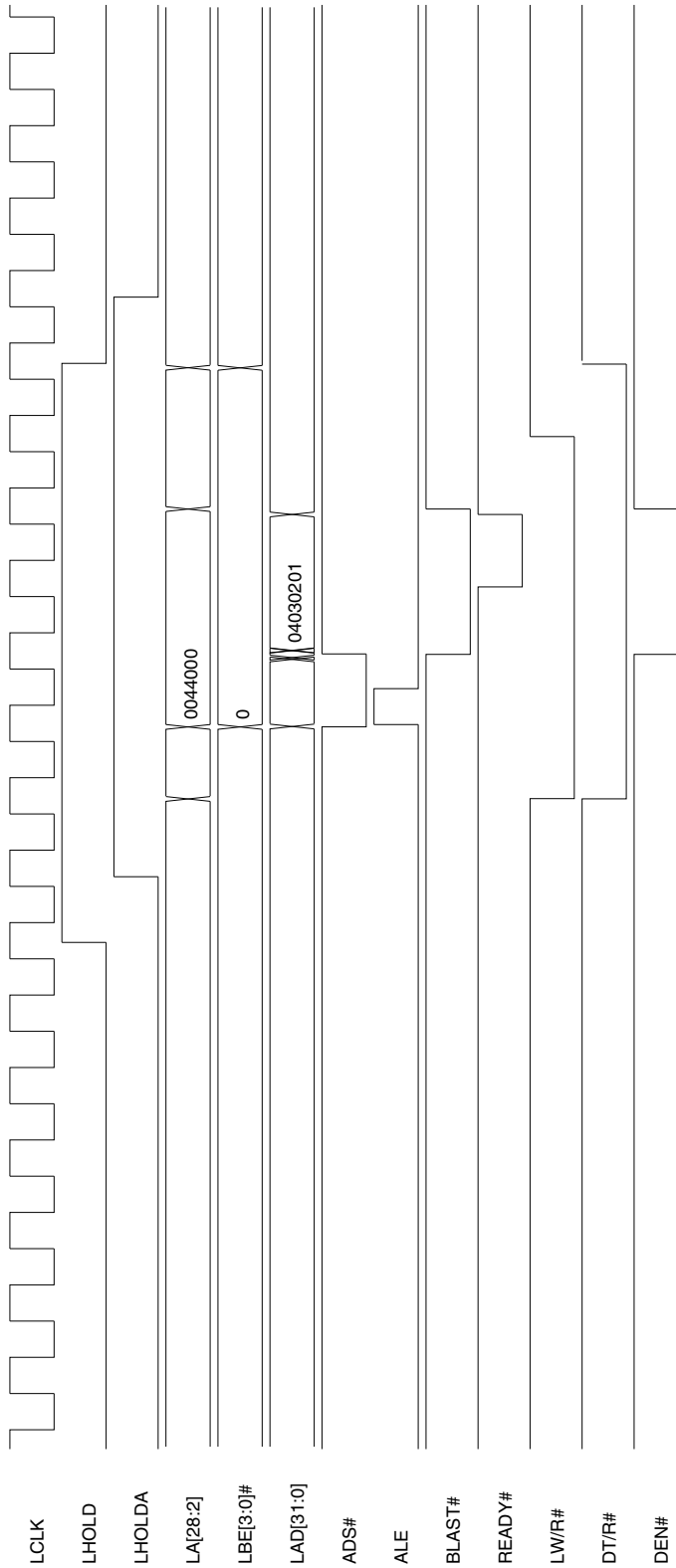
Note: *This single-cycle Direct Slave Read from a 32-bit Local Bus device/transceivers timing diagram includes the DT/R# and DEN# signals. The PEX 8311 always tri-states the DT/R# and DEN# signals, except during the time it owns the Local Bus (LHOLD and LHOLDA are asserted) to process a Direct Slave or DMA transfer. Because the DT/R# and DEN# signal balls are pulled up, they are seen as a 1 (High) in this diagram when the PEX 8311 is not driving them. DT/R# and DEN# can be ORed to create the DIR signal for the transceiver(s).*

6.6.3 J Mode DMA Timing Diagrams

Timing Diagram 6-55. DMA PCI Express-to-Local (32-Bit Local Bus)
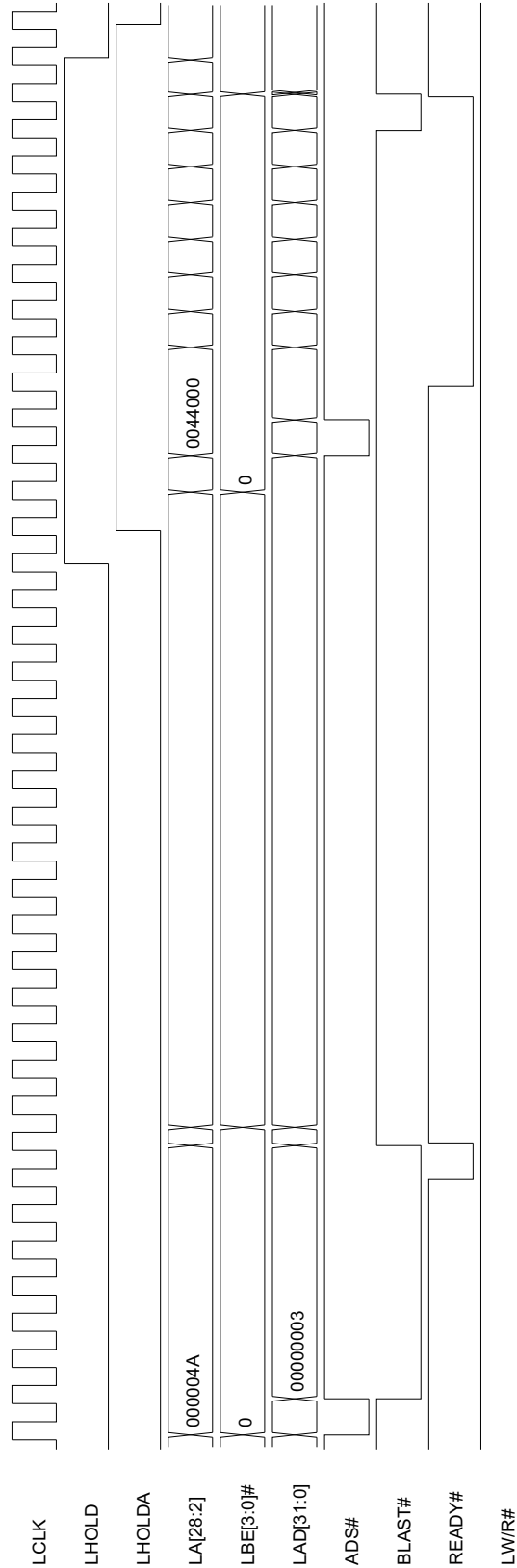
Notes: *The writing of the registers to set up this 32-byte DMA Block mode transfer using DMA Channel 0/1 is not shown.*

Writing the LCS_DMACSR0/1 register (LOC:128h/LOC:129h) with 03h enables and starts this DMA transfer.

Timing Diagram 6-56. DMA Local-to-PCI Express (32-Bit Local Bus)
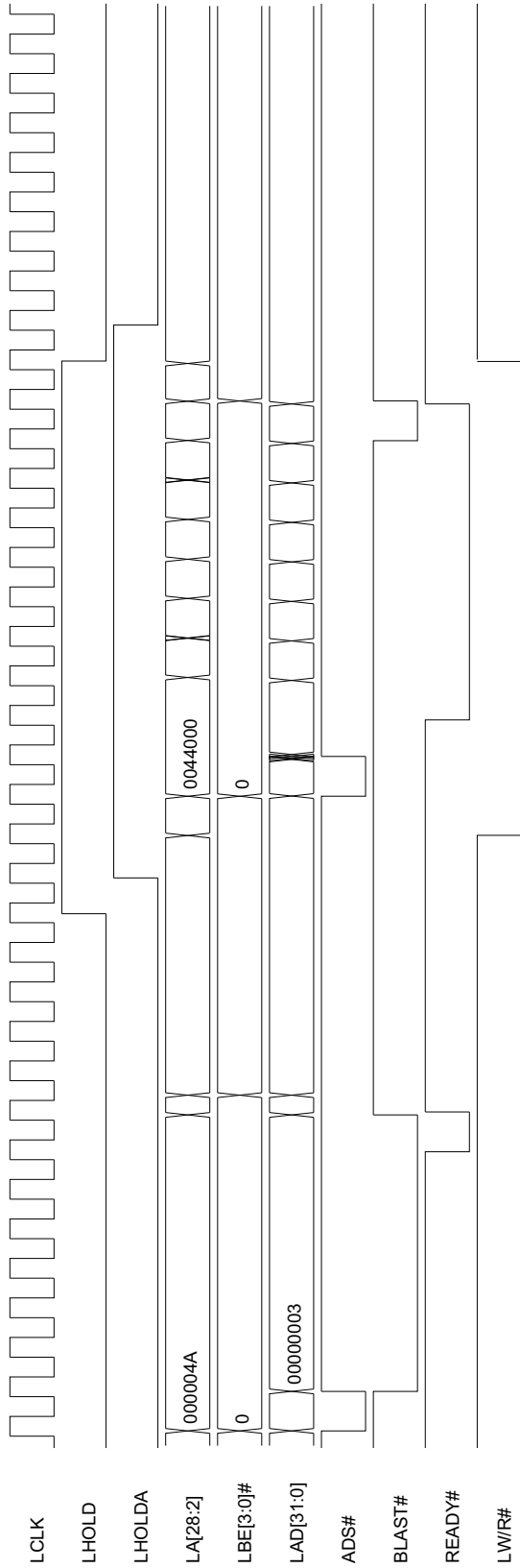
LCLK

LHOLD

LHOLDA

LA[28:2]   000004A   0044000

LBE[3:0]#   0   0

LAD[31:0]   00000003

ADS#

BLAST#

READY#

LW/R#

Notes: *The writing of the registers to set up this 32-byte DMA Block mode transfer using DMA Channel 0/1 is not shown.*

Writing the LCS_DMACSR0/1 register (LOC:128h/LOC:129h) with 03h enables and starts this DMA transfer.

Timing Diagram 6-57. DMA PCI Express-to-Local Demand Mode (32-Bit Local Bus)
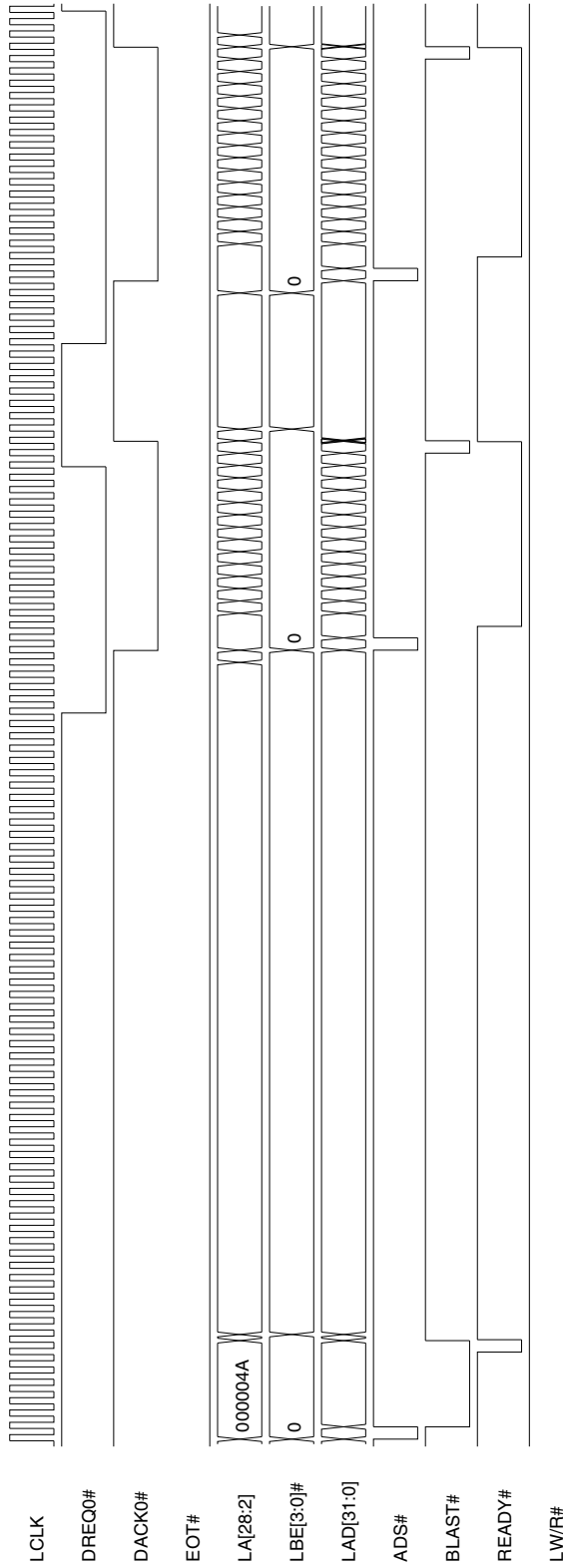
Notes: *The Channel 0/1 Demand mode DMA transfer starts when the* LCS_DMACSR0/1[1:0] *bits are written to 11b.*

The PEX 8311 does not attempt to arbitrate for and Write data to the Local Bus until it detects that the DREQx# is asserted.
The transfer is temporarily suspended when DREQx# is de-asserted, then resumed upon its re-assertion.

Timing Diagram 6-58. DMA Local-to-PCI Express Demand Mode (32-Bit Local Bus)
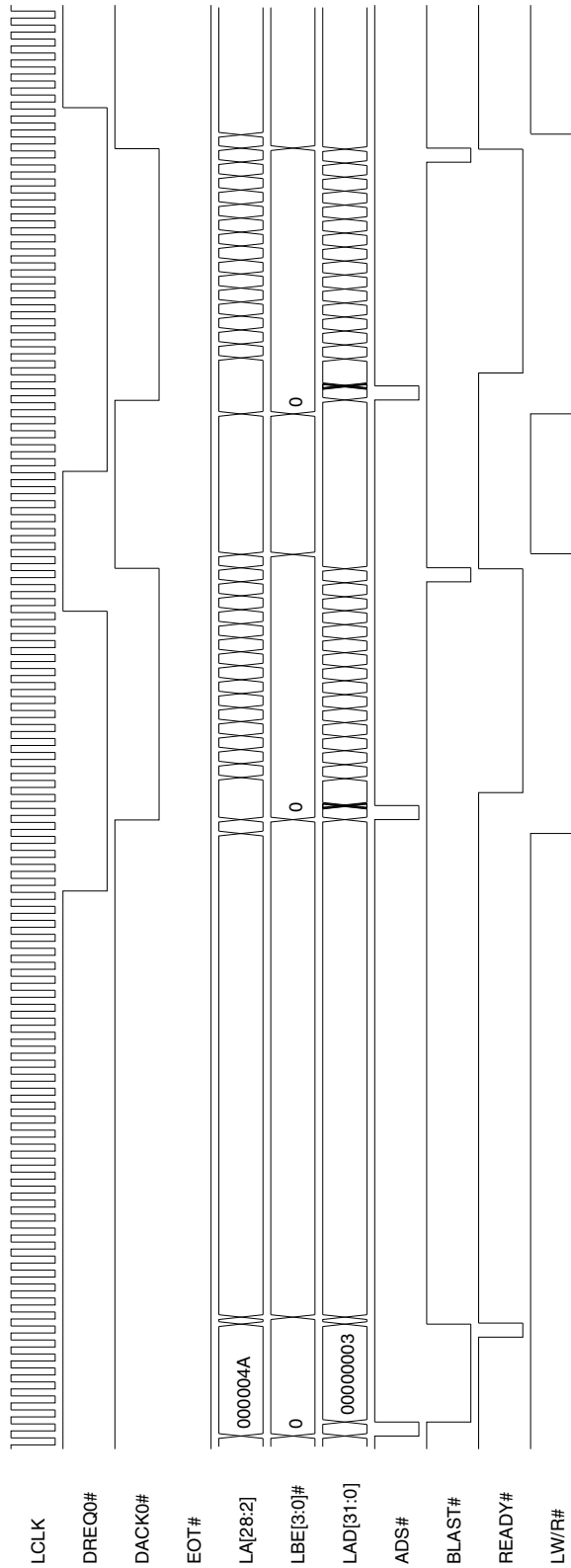
Note: *The Channel 0/1 Demand mode DMA transfer starts when the* ***LCS_DMACSR0/1****[1:0] bits are written to 11b and the PEX 8311 detects that the DREQx# signal is asserted. Once started, the PEX 8311 arbitrates for and Reads data from the Local Bus, then writes the data to the internal PCI Bus until the transfer is temporarily suspended when DREQx# is de-asserted. The transfer resumes upon DREQx# re-assertion.*

Timing Diagram 6-59. DMA Local-to-PCI Express Demand Mode with EOT# Assertion (32-Bit Local Bus)
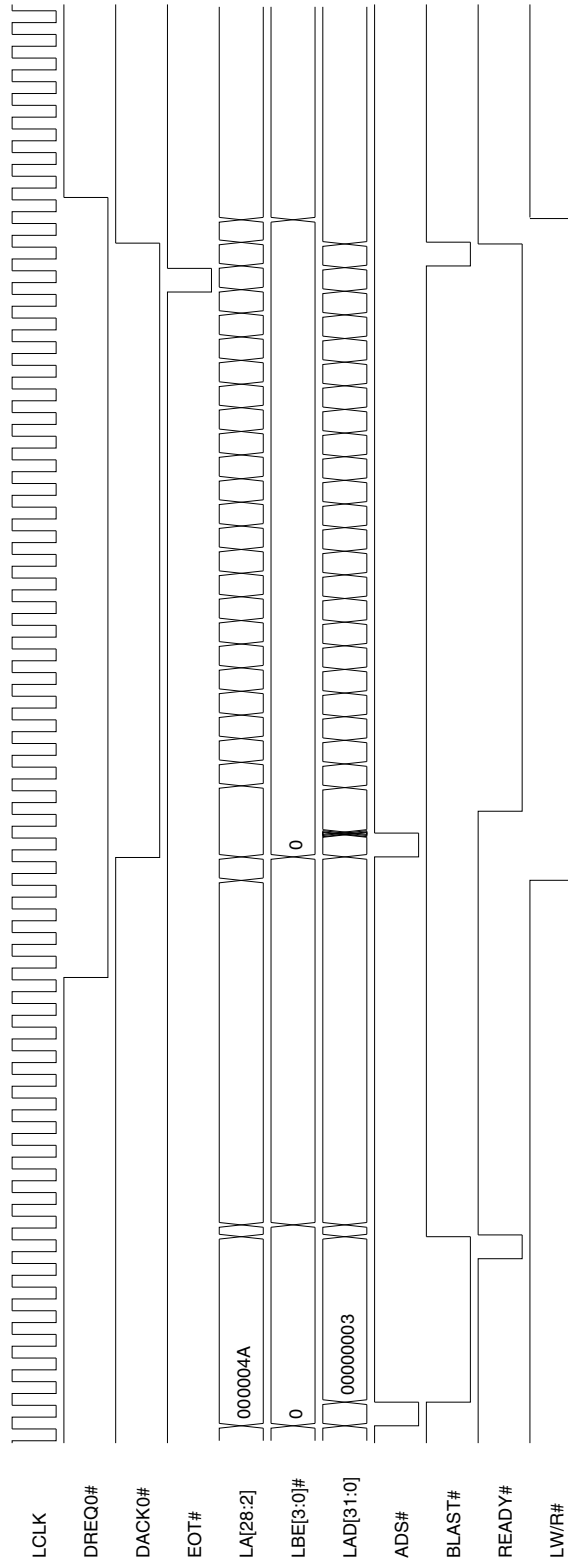
Note: *The Channel 0/1 Demand mode DMA transfer starts when the* ***LCS_DMACSR0/1***[1:0] *bits are written to 11b and the PEX 8311 detects that the DREQx# signal is asserted. Once started, the PEX 8311 arbitrates for and Reads data from the Local Bus, then Writes the data to the internal PCI Bus until the transfer is terminated with an EOT# assertion. All data that is read into the DMA FIFO is written to the internal PCI Bus.*

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Chapter 7   M Mode Functional Description

7.1　　Introduction

The functional operation described in this section can be modified through the PEX 8311 LCS registers.

7.2　　Wait State Control

The TA# signal overrides the programmable Wait State Counter(s) (**LCS_LBRD0**[5:2] for Space 0, **LCS_LBRD1**[5:2] for Space 1, **LCS_LBRD0**[21:18] for Expansion ROM, and/or **LCS_DMAMODE0/1**[5:2] for Channel *x*), and can be used to introduce additional wait states. Figure 7-1 illustrates the PEX 8311 wait states for M mode.

Figure 7-1.　Wait States – M Mode
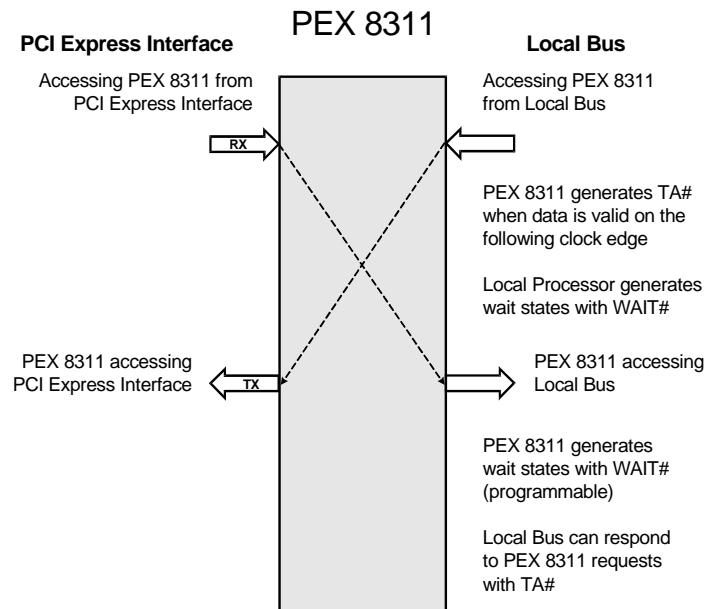
Note:　Figure 7-1 represents a sequence of Bus cycles.

7.2.1   Local Bus Wait States

In Direct Master mode, when accessing the PEX 8311 registers or transferring data, the PEX 8311 is a Local Bus Slave. As a Local Bus Slave, the PEX 8311 inserts external wait states with the TA# signal.

In Direct Slave and DMA modes, the PEX 8311 acts as a Local Bus Master. When TA# input is disabled, the Internal Wait State Counter(s) can be used to program the number of internal wait states between the first address-to-data state, and subsequent data-to-data in Burst mode. (Refer to Table 7-1.)

In Direct Slave and DMA modes, if TA# is enabled (**LCS_LBRD0**[6]=1 for Space 0, **LCS_LBRD1**[6]=1 for Space 1, **LCS_LBRD0**[22]=1 for Expansion ROM, and/or **LCS_DMAMODE0/1**[6]=1 for Channel *x*), do not use the Wait State Counter(s) nor WAIT# ball. The external memory control can use the TA# input to insert wait states.

Table 7-1.   Internal Wait State Counters

Bits	Description
LCS_LBRD0[5:2]	Local Address Space 0 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
LCS_LBRD1[5:2]	Local Address Space 1 Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
LCS_LBRD0[21:18]	Expansion ROM Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)
LCS_DMAMODE0/1[5:2]	DMA Channel *x* Internal Wait State Counter (address-to-data; data-to-data; 0 to 15 wait states)

7.3 M Mode Functional Timing Diagrams

General notes about timing designer (graphical) waveforms:
The graphical Timing Diagrams were created using the Timing Designer tool. They are accurate and adhere to their specified protocol(s). These diagrams show transfers and signal transitions; however, they should not be relied upon to show exactly, on a clock-for-clock basis, wherein PEX 8311-driven signal transitions will occur.

General notes about captured waveforms:
The captured Timing Diagrams were captured from a simulation signal display tool that displays the results of stimulus run on the netlist. Using the netlist illustrates realistic delay on signals driven by the PEX 8311. Signals driven by the test environment to the PEX 8311 are quite fast. Leading zeros (0) for buses such as AD[31:0] or LD[0:31], may or may not be shown. When no value for a bus is shown while the PEX 8311 is executing a transfer, it is because the entire value cannot be displayed in the available space or is irrelevant. When the PEX 8311 is not executing a transfer on that bus, the value is not shown because it is either irrelevant or unknown (any or all signals are 1, 0, or Z).

For these waveforms, the external Local Bus Arbiter "parks" the PEX 8311 on the Local Bus (BG# asserted throughout) or grants and "parks" the Local Bus to the PEX 8311 upon detecting that the PEX 8311 has requested the Local Bus by asserting BR#.

7.3.1 Configuration Timing Diagrams

Timing Diagram 7-1. PCI Configuration Write to PCI Configuration Register

PCLK	
FRAME#	
AD[31:0]	00001030	0000EFFF
C/BE[3:0]#	B	0
IDSEL	
IRDY#	
DEVSEL#	
TRDY#	
STOP#	
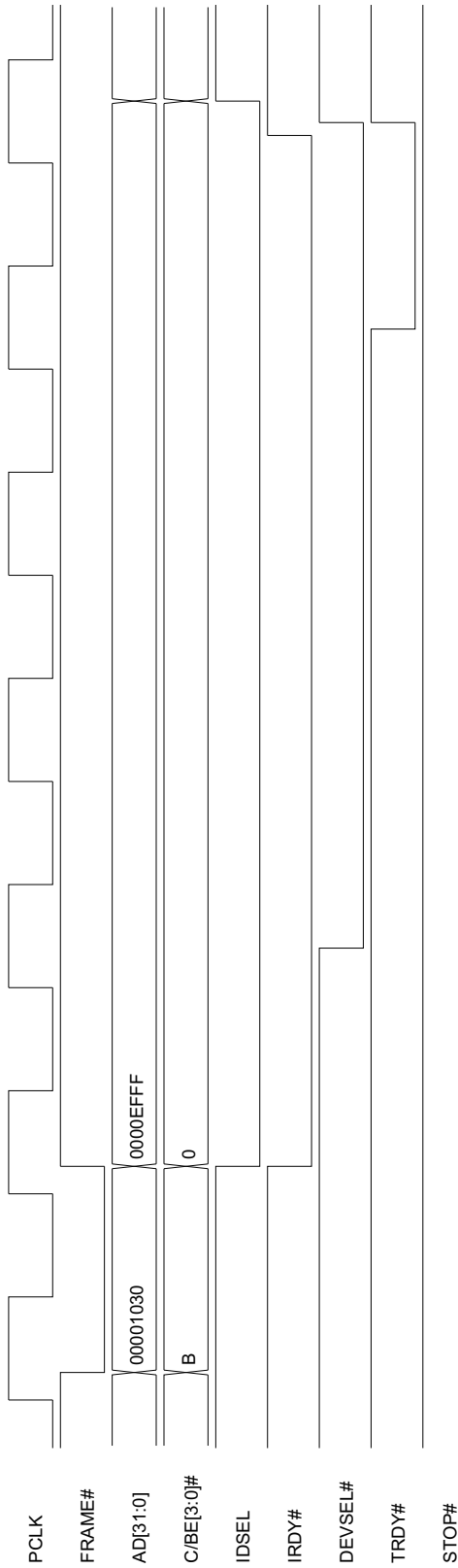
Notes: *PCI Configuration Write to the LCS_PCIERBAR (PCI:30h) register.*

IDSEL = AD[12].

Timing Diagram 7-2. PCI Configuration Read of PCI Configuration Register

PCLK

FRAME#

AD[31:0]   00001000   905610B5

C/BE[3:0]#   A   0

IDSEL

IRDY#

DEVSEL#

TRDY#

STOP#
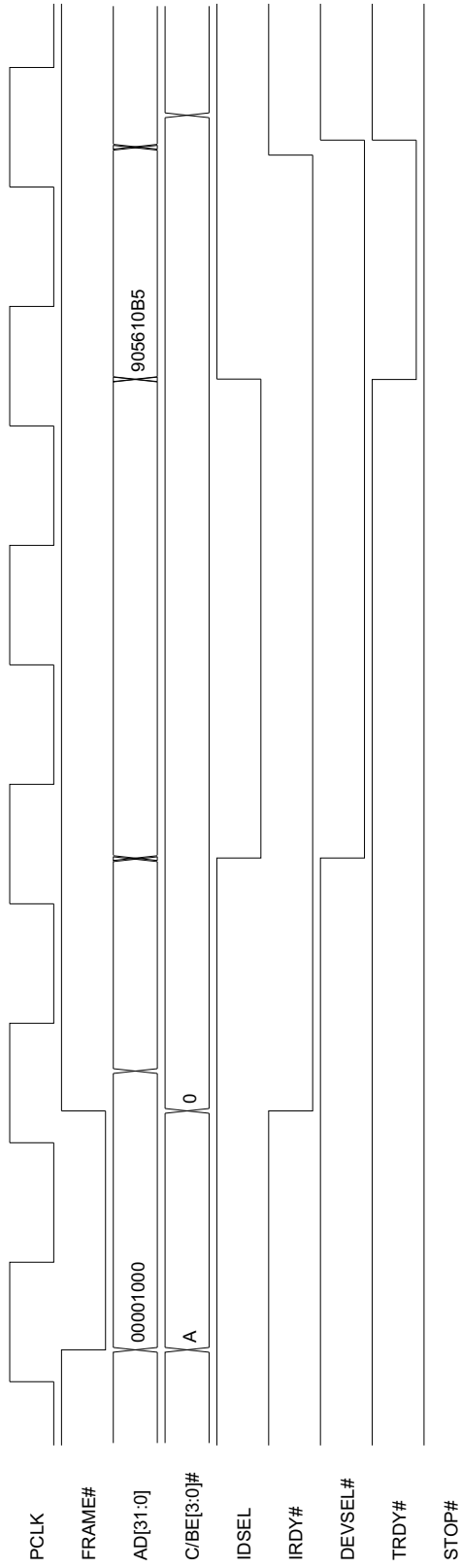
Notes: *PCI Configuration Read of the LCS_PCIIDR (PCI:00h) register.*

IDSEL = AD[12].

Timing Diagram 7-3. Local Write to Configuration Register

LCLK

BR#

BG#

BB#

CCS#

LA[0:31]   200000C0

TSIZ[0:1]   0

LD[0:31]   00001234

TS#

BURST#

BDIP#

TA#

RD/WR#
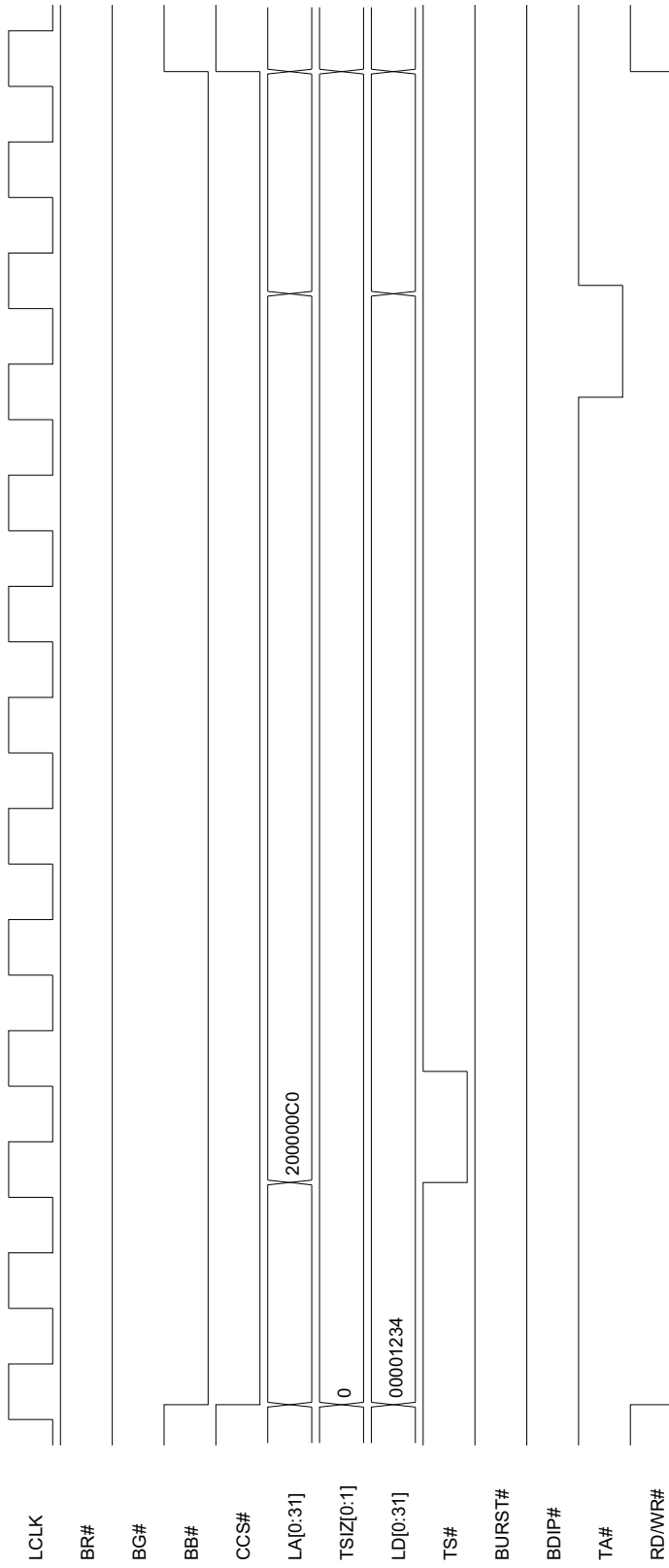
Notes: *Local Configuration Write to the LCS_MBOX0 (LOC:C0h) register.*

CCS# is asserted for multiple Clock cycles, but it is required to be asserted only during the TS# Clock cycle.

Only the LA[23:29] signals are used to decode the LCS_MBOX0 register.

Timing Diagram 7-4. Local Read of Configuration Register

LCLK

BR#

BG#

BB#

CCS#

LA[0:31] 200000C0

TSIZ[0:1] 0

LD[0:31] 00001234

TS#

BURST#

BDIP#

TA#

RD/WR#
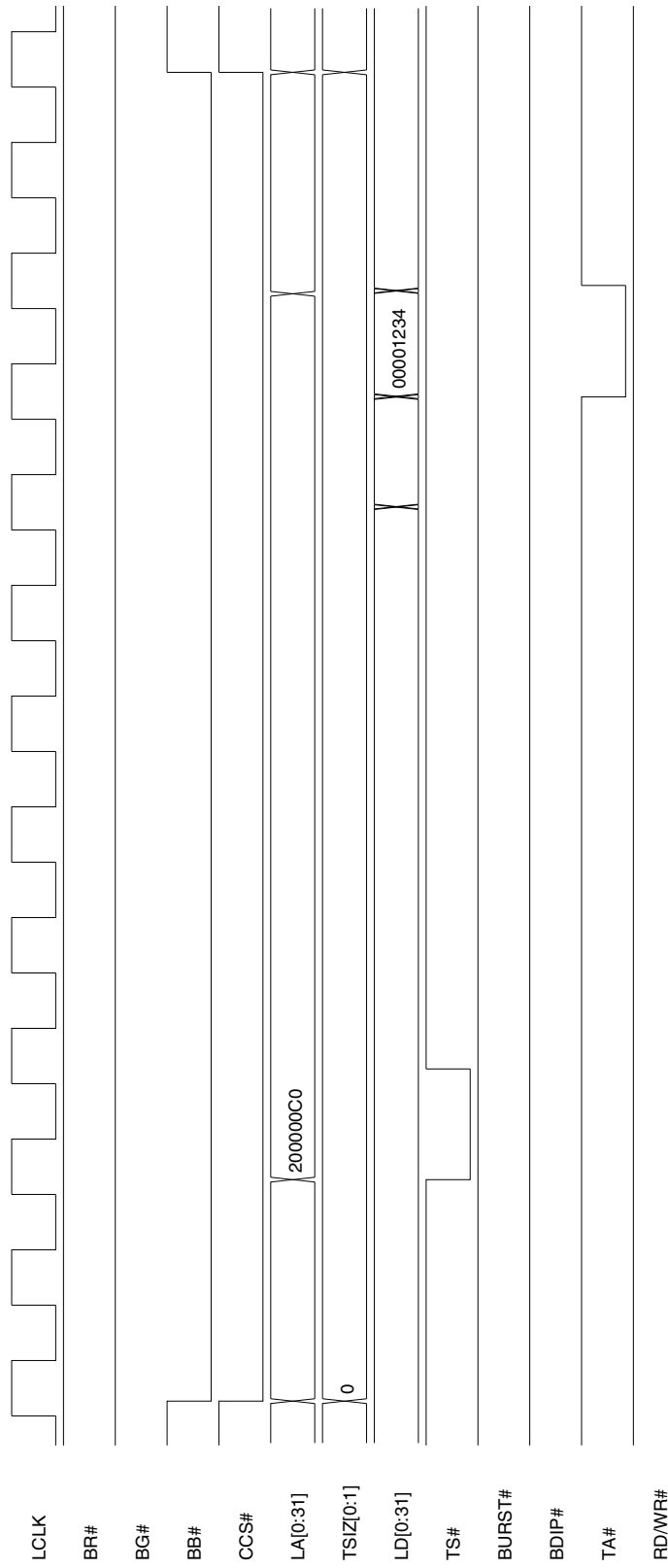
Notes: *Local Configuration Read of the LCS_MBOX0 (LOC:C0h) register.*

CCS# is asserted for multiple Clock cycles, but it is required to be asserted only during the TS# Clock cycle.

Only the LA[23:29] signals are used to decode the LCS_MBOX0 register.

The PEX 8311 starts driving the LD[0:31] bus with meaningless data one cycle before it asserts the TA# signal with the data read from the LCS_MBOX0 register.

7.3.2   M Mode Direct Master Timing Diagrams

Timing Diagram 7-5. Direct Master Burst Write of 6 Dwords, Continuous Burst Mode
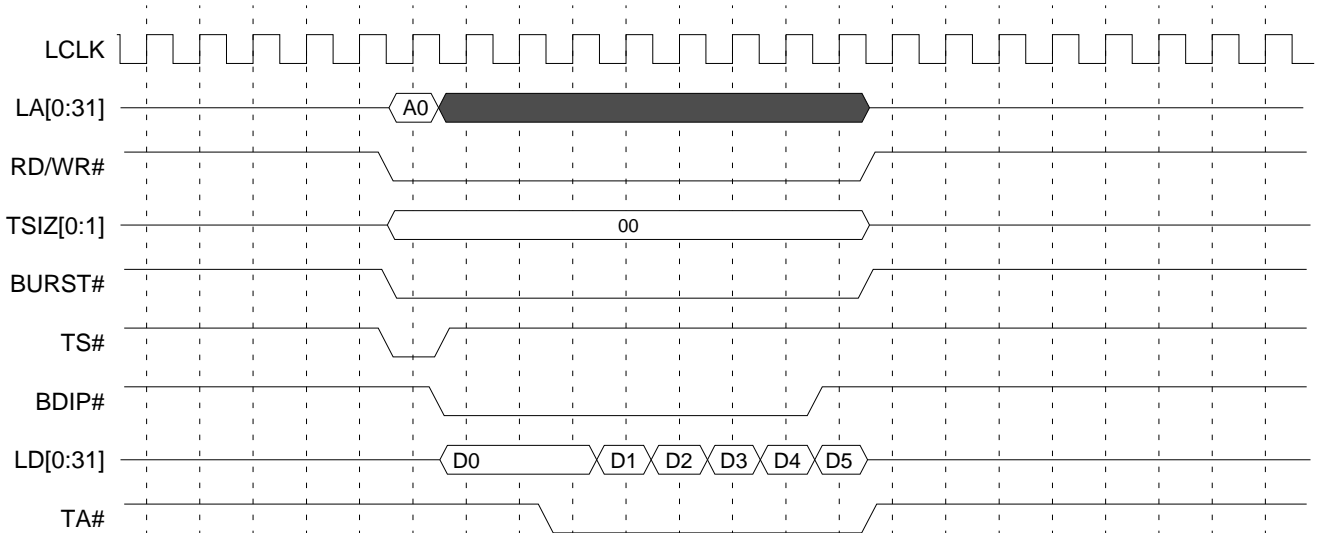
Timing Diagram 7-6. Direct Master Burst Read of 6 Dwords, Continuous Burst Mode
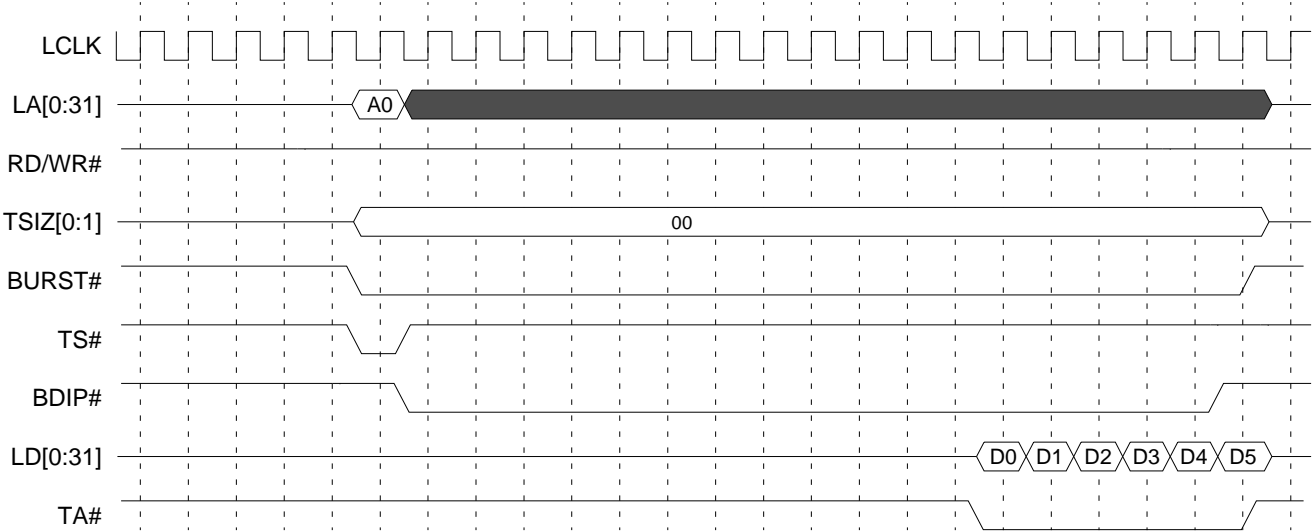
Timing Diagram 7-7. Direct Master Burst Write of 8 Dwords

PCLK
REQ#
GNT#
FRAME#
AD[31:0]
C/BE[3:0]#
IRDY#
DEVSEL#
TRDY#
STOP#

LCLK
BR#
BG#
BB#
LA[0:31]
TSIZ[0:1]
LD[0:31]
TS#
BURST#
BDIP#
TA#
RD/WR#
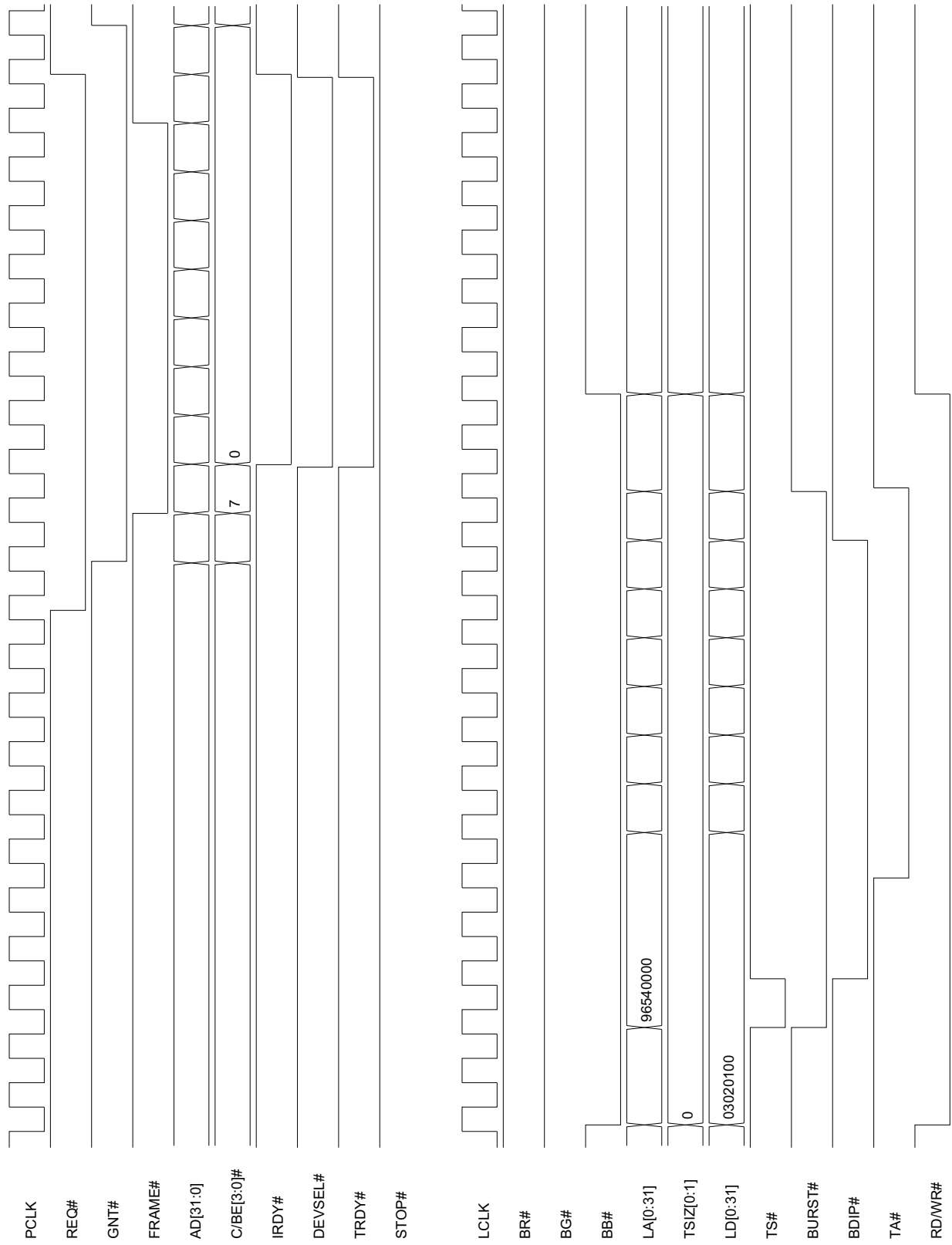
Note: *Key register value is LCS_DMPBAM[15:0]=0007h.*

Timing Diagram 7-8. Direct Master Burst Read of 8 Dwords

PCLK

REQ#

GNT#

FRAME#

AD[31:0]

C/BE[3:0]#   6   0

IRDY#

DEVSEL#

TRDY#

STOP#

LCLK

BR#

BG#

BB#

LA[0:31]   96540000

TSIZ[0:1]   0

LD[0:31]

TS#

BURST#

BDIP#

TA#

RD/WR#
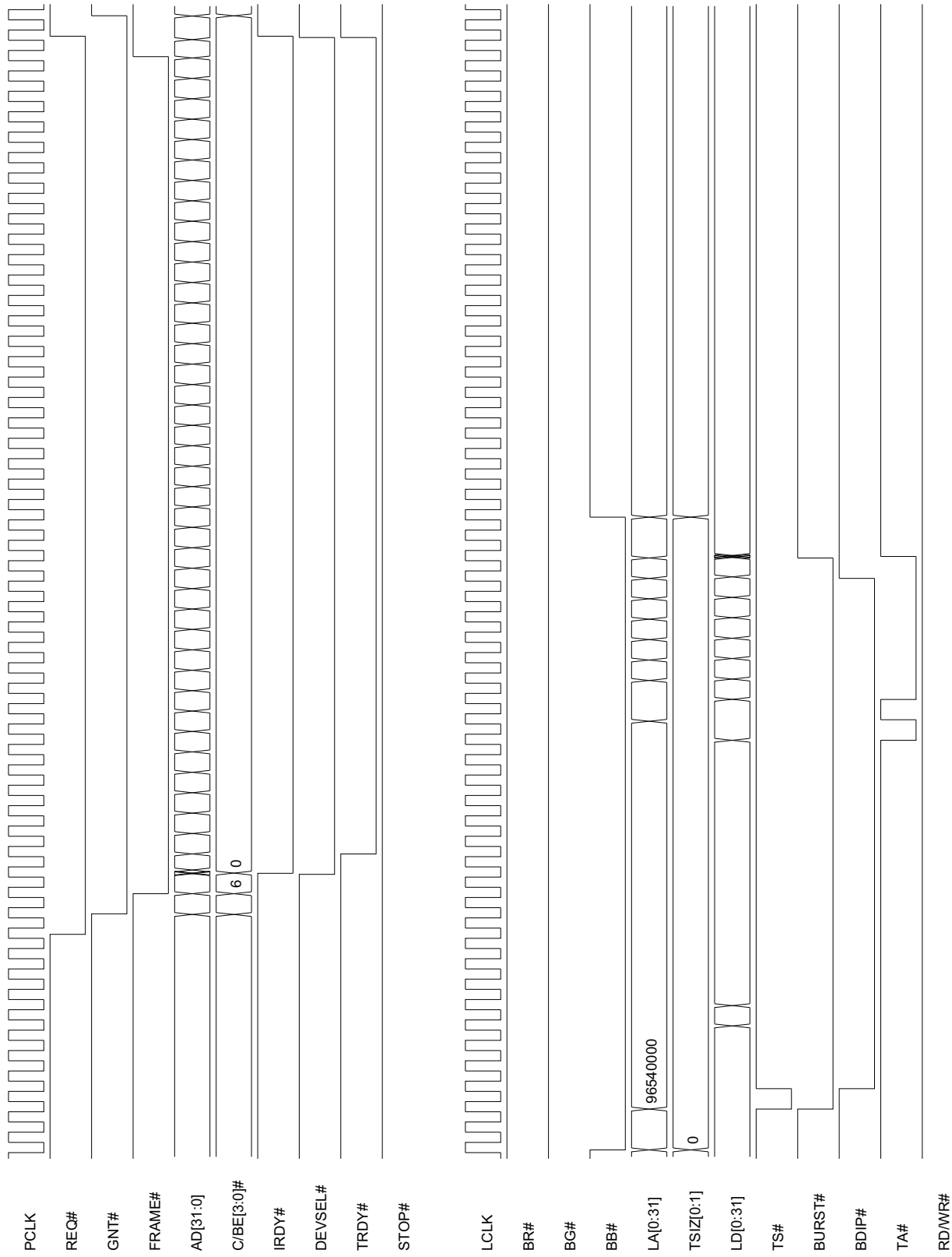
Note: Key register value is LCS_DMPBAM[15:0]=0007h.

Timing Diagram 7-9. TEA# Assertion Caused by Direct Master Abort during Direct Master Single Cycle Read
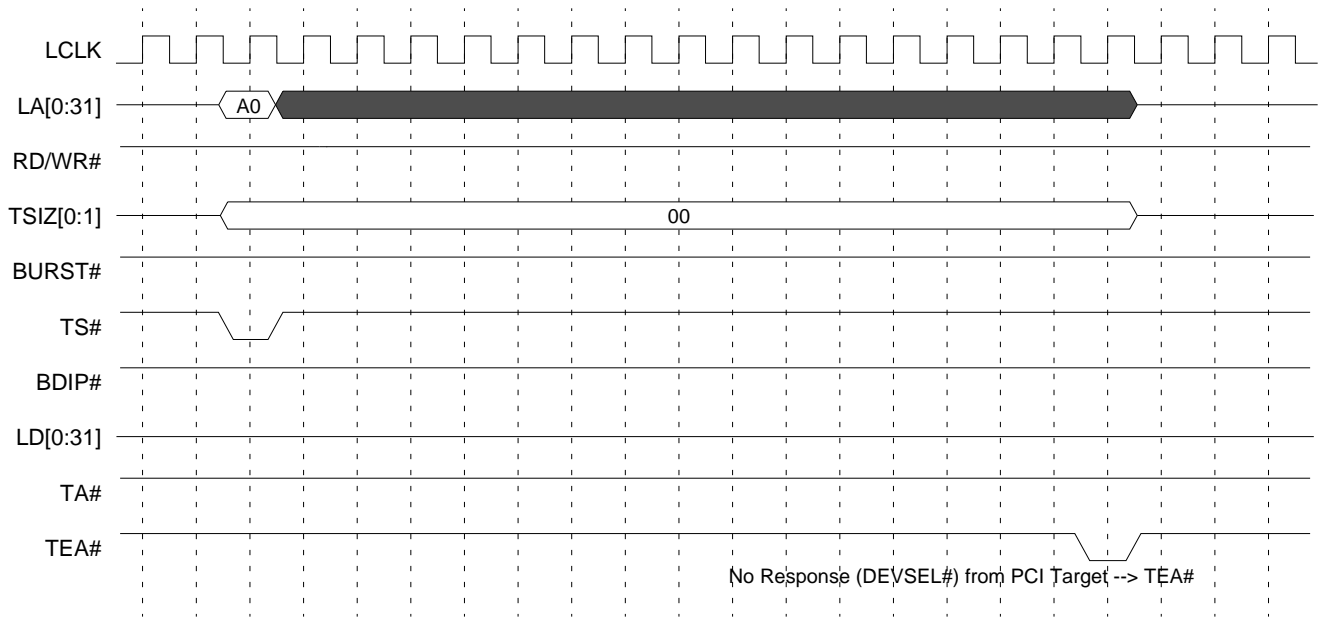
7.3.3   M Mode Direct Slave Timing Diagrams

Timing Diagram 7-10. Direct Slave Burst Write of 10 Dwords, Zero Wait States, Continuous Burst Mode
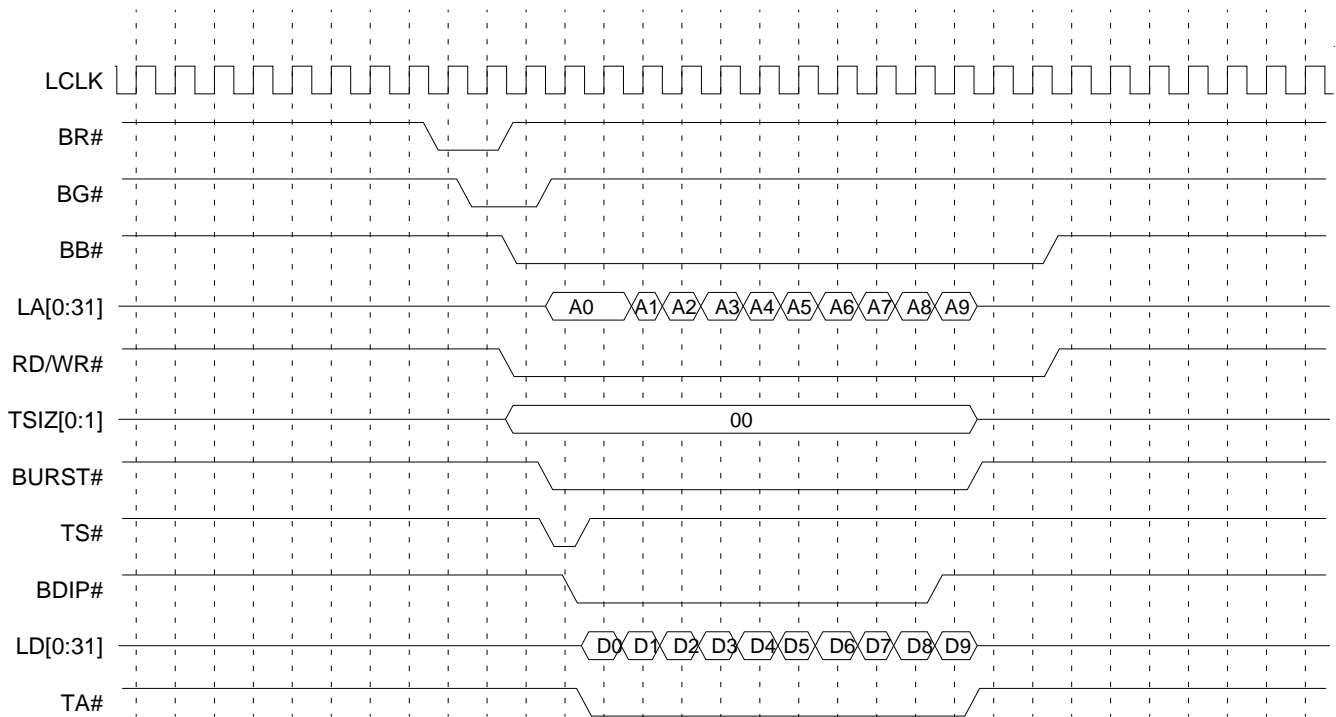
Timing Diagram 7-11. Direct Slave Burst Read of 10 Dwords, Zero Wait States, Continuous Burst Mode
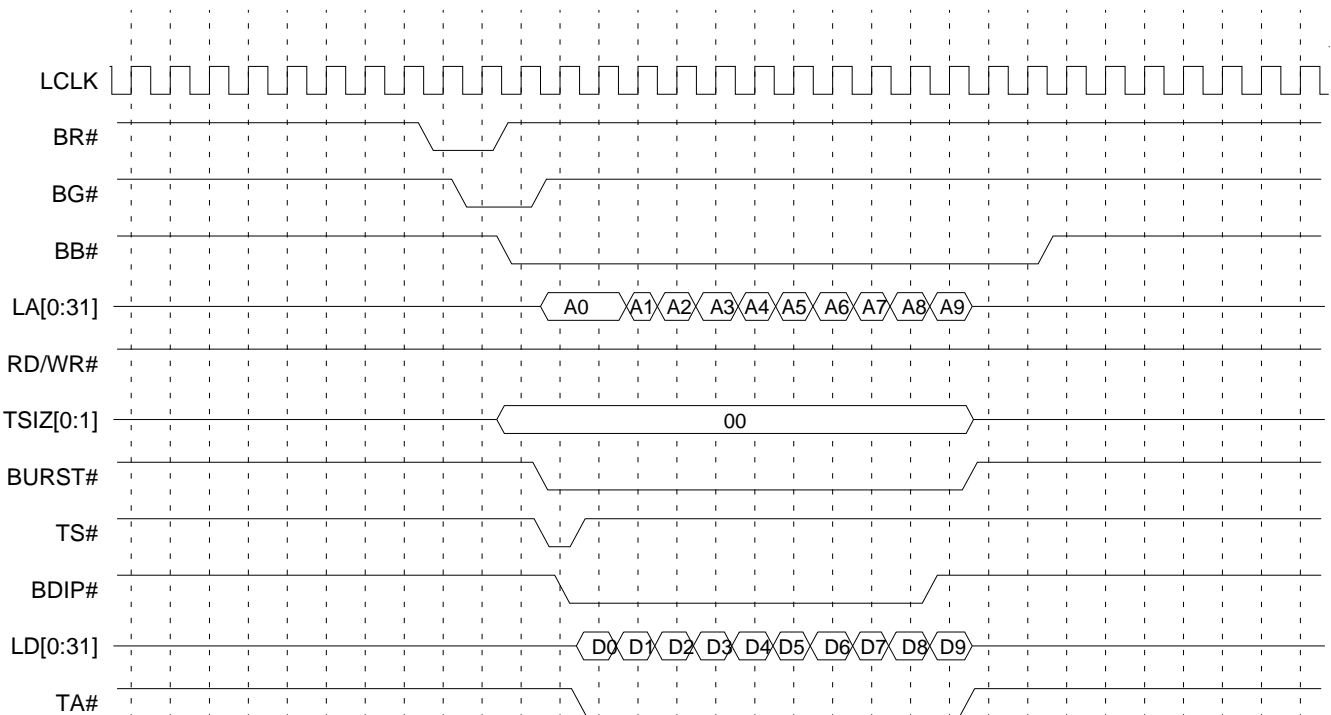
Timing Diagram 7-12. Direct Slave Single Cycle Write (8-Bit Local Bus)
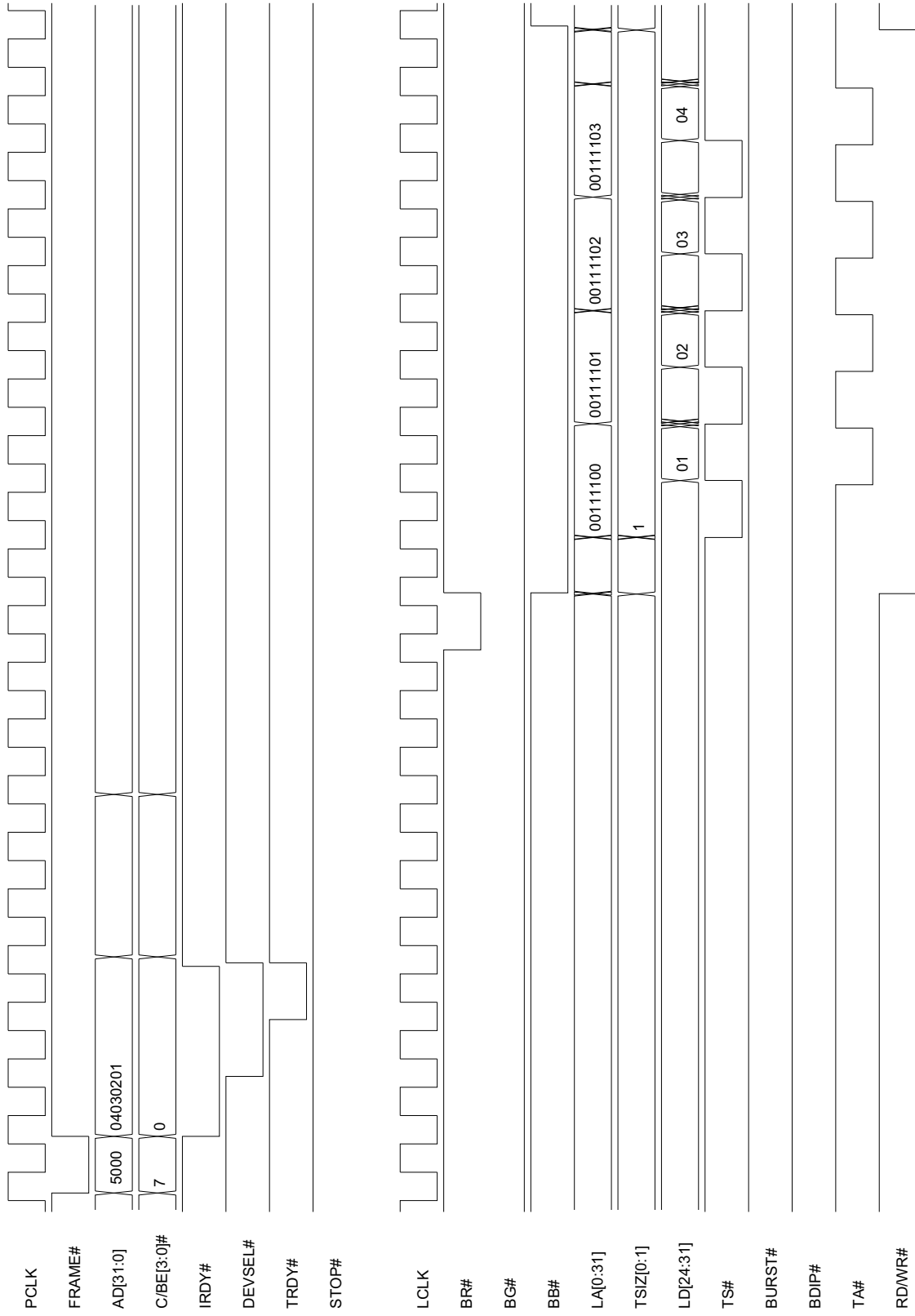
Note: *Key bit/register values are LCS_MARBR[24]=1, LCS_BIGEND[4]=0, and LCS_LBRD1[15:0]=0D40h.*

Timing Diagram 7-13. Direct Slave Single Cycle Write (16-Bit Local Bus)
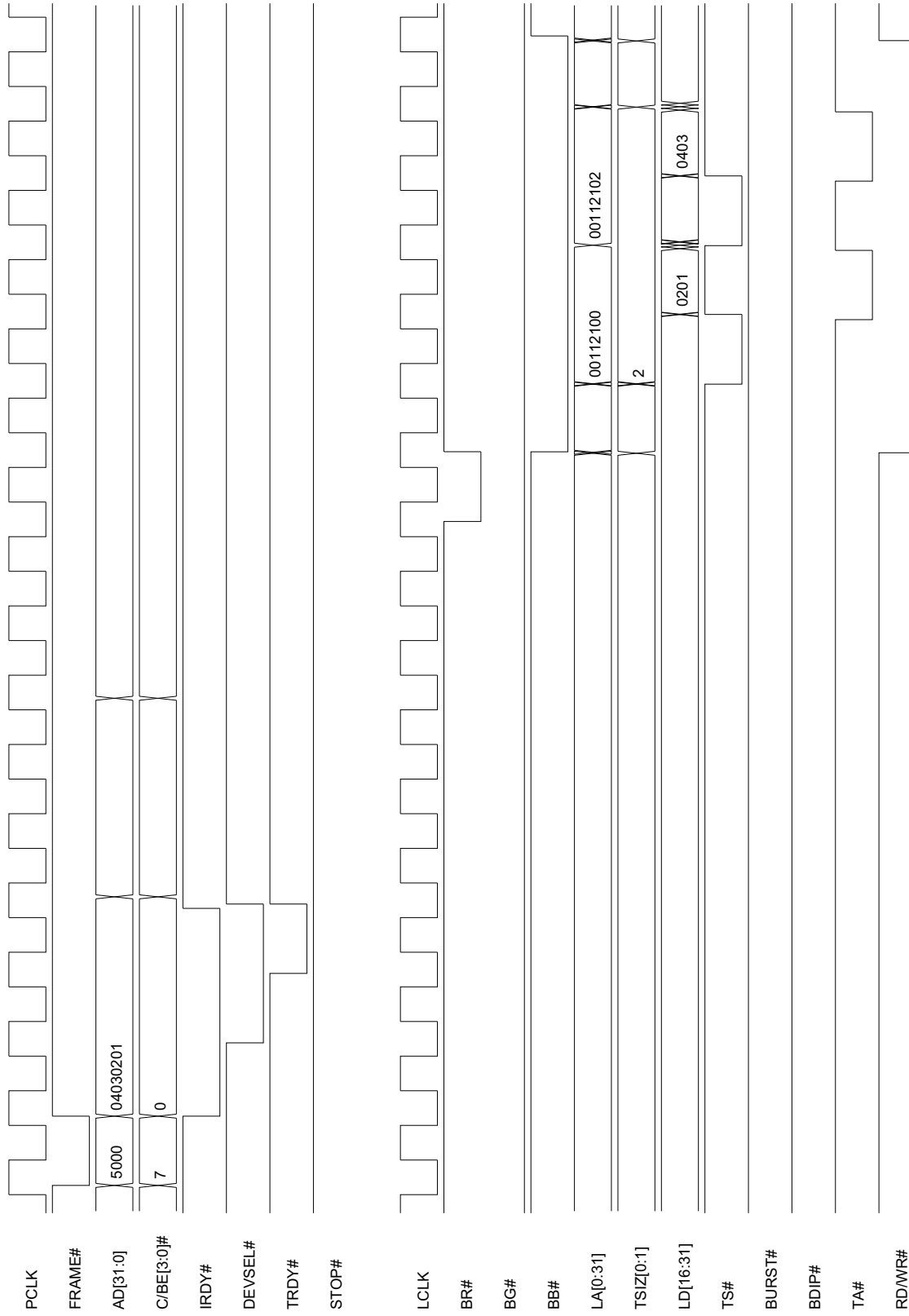
PCLK

FRAME#

AD[31:0] 5000 04030201

C/BE[3:0]# 7 0

IRDY#

DEVSEL#

TRDY#

STOP#

LCLK

BR#

BG#

BB#

LA[0:31] 00112100 00112102

TSIZ[0:1] 2

LD[16:31] 0201 0403

TS#

BURST#

BDIP#

TA#

RD/WR#

Note: Key bit/register values are LCS_MARBR[24]=0, LCS_BIGEND[4]=0, and LCS_LBRD1[15:0]=1541h.

Timing Diagram 7-14. Direct Slave Single Cycle Write (32-Bit Local Bus)

PCLK

FRAME#

AD[31:0]   5000   04030201

C/BE[3:0]#   7   0

IRDY#

DEVSEL#

TRDY#

STOP#

LCLK

BR#

BG#

BB#

LA[0:31]   00110000

TSIZ[0:1]   0

LD[0:31]

TS#

BURST#

BDIP#

TA#

RD/WR#
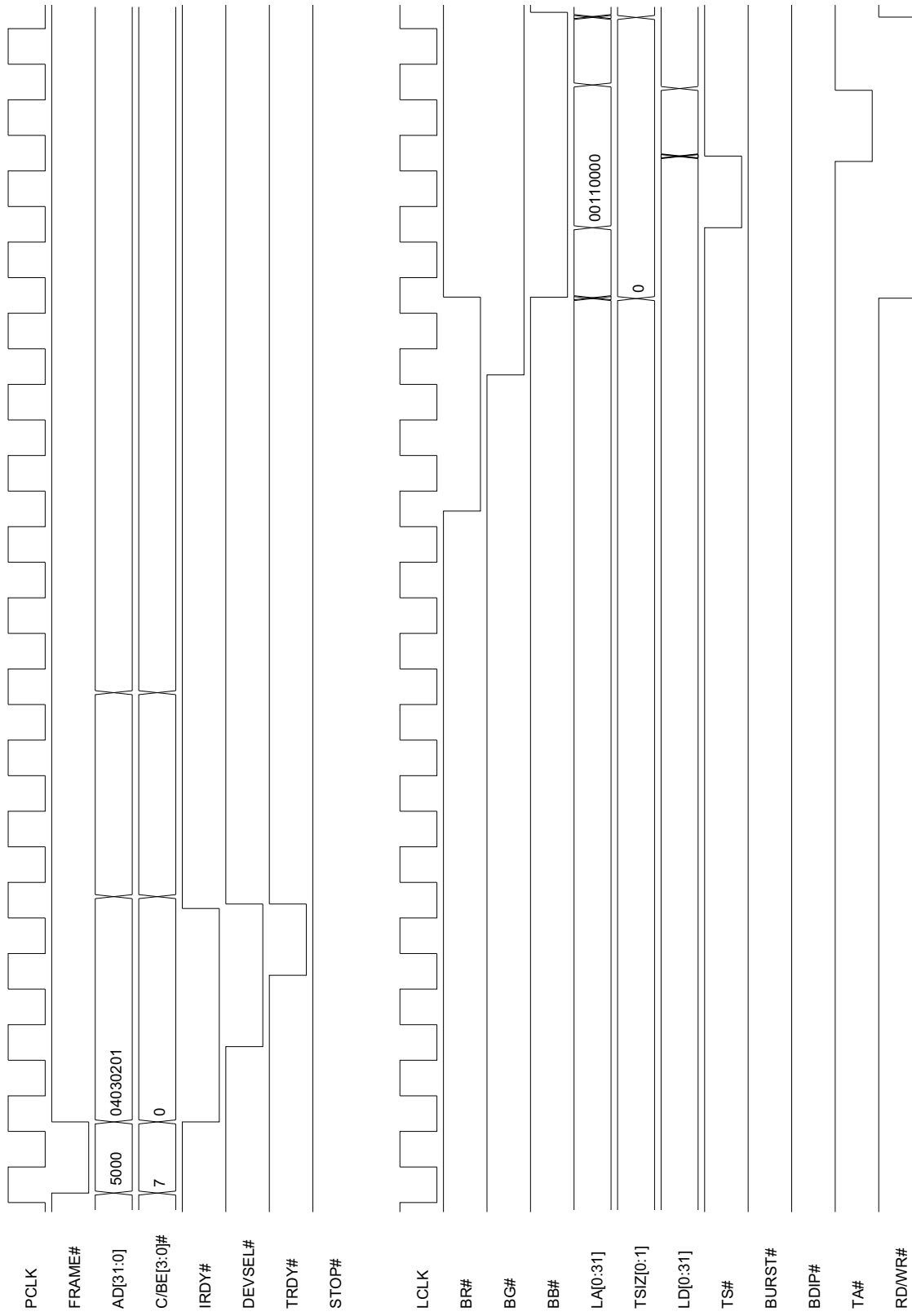
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=0D42h.

Timing Diagram 7-15. Direct Slave Single Cycle Read (8-Bit Local Bus)

PCLK
FRAME#
AD[31:0]
C/BE[3:0]#
IRDY#
DEVSEL#
TRDY#
STOP#

LCLK
BR#
BG#
BB#
LA[0:31]
TSIZ[0:1]
LD[24:31]
TS#
BURST#
BDIP#
TA#
RD/WR#
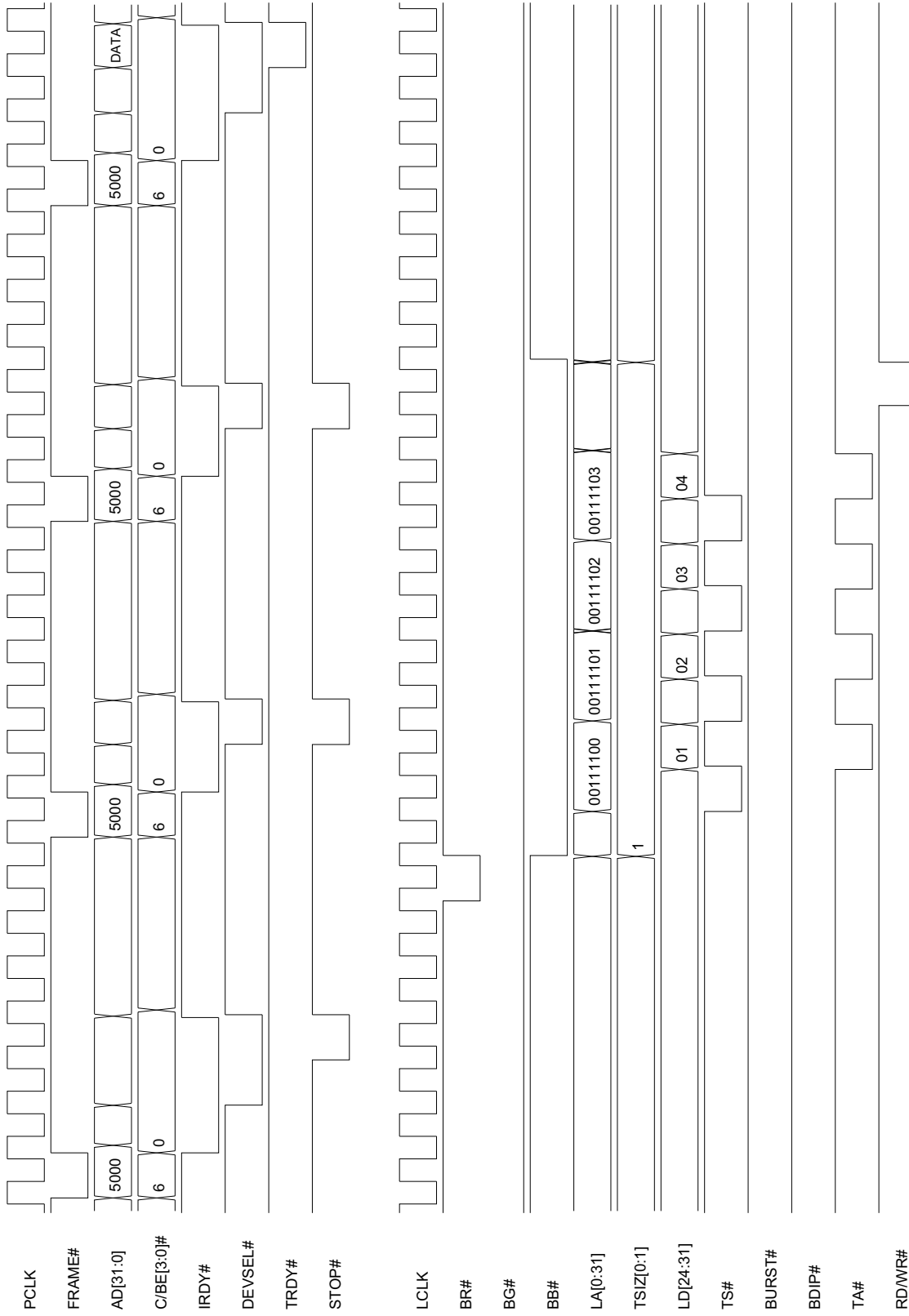
Notes: *Hex value for AD[31:0] DATA = 0403_0201h.*

Timing Diagram 7-16. Direct Slave Single Cycle Read (16-Bit Local Bus)

PCLK

FRAME#

AD[31:0] 5000 DATA

C/BE[3:0]# 6 0

IRDY#

DEVSEL#

TRDY#

STOP#

LCLK

BR#

BG#

BB#

LA[0:31] 00112100 00112102

TSIZ[0:1] 2

LD[16:31] 0201 0403

TS#

BURST#

BDIP#

TA#

RD/WR#
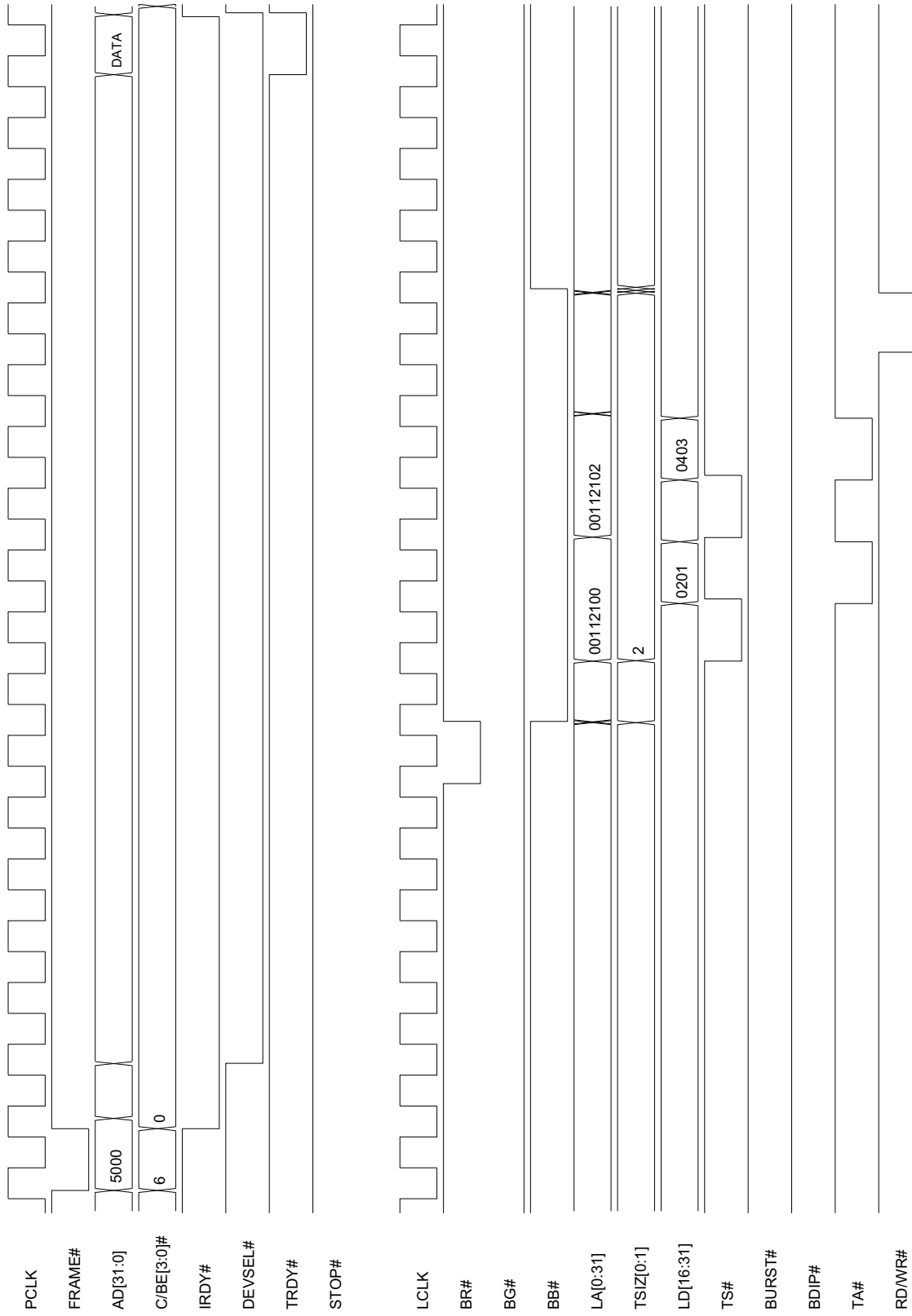
Notes: *Hex value for AD[31:0] DATA = 0403_0201h.*

Key bit/register values are LCS_MARBR[24]=0, LCS_BIGEND[4]=0, and LCS_LBRD1[15:0]=1541h.

Timing Diagram 7-17. Direct Slave Single Cycle Read (32-Bit Local Bus)

PCLK

FRAME#

AD[31:0]   96550000   DATA

C/BE[3:0]#   6   0

IRDY#

DEVSEL#

TRDY#

STOP#

LCLK

BR#

BG#

BB#

LA[0:31]   00110000

TSIZ[0:1]   0

LD[0:31]

TS#

BURST#

BDIP#

TA#

RD/WR#
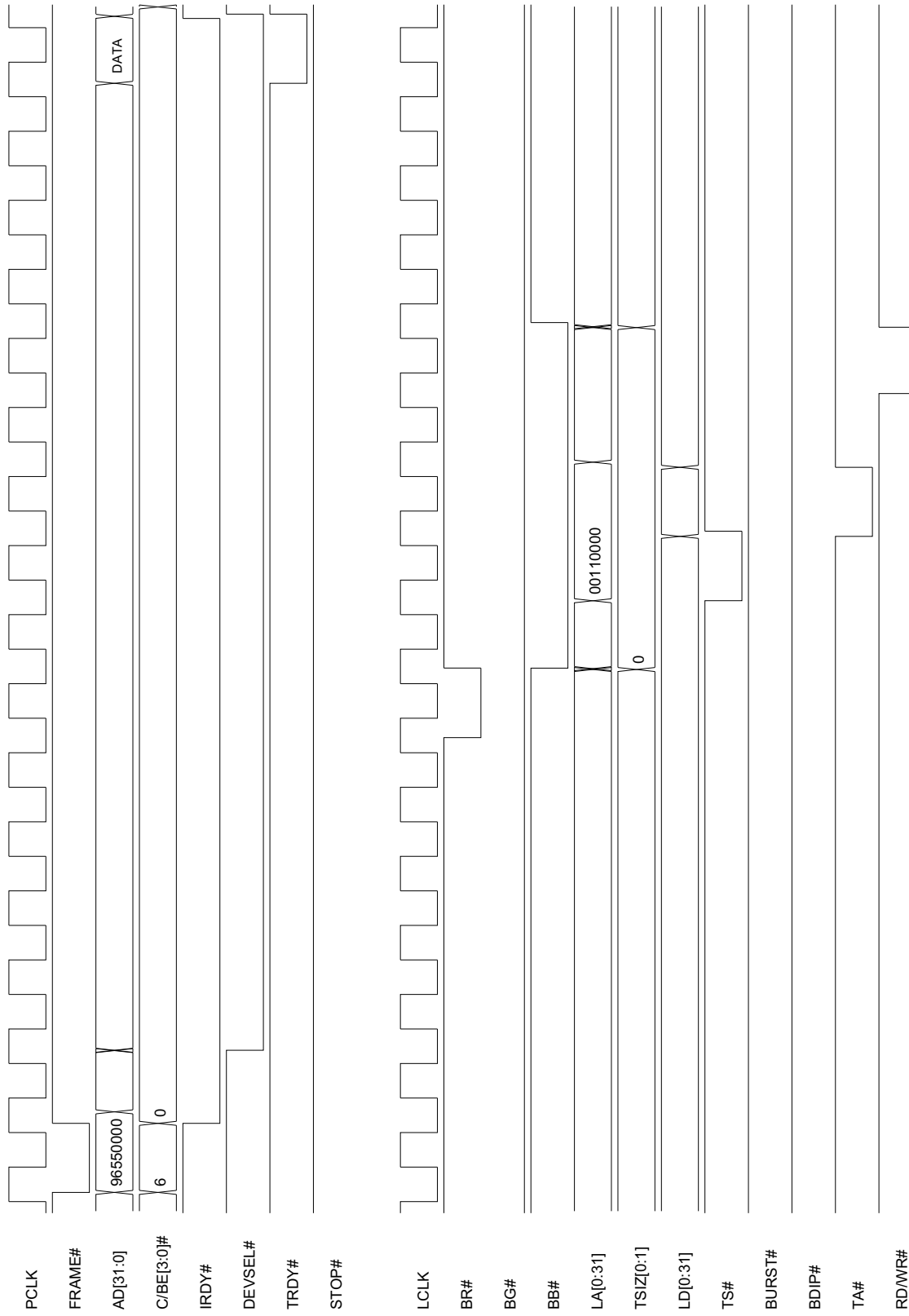
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=0D42h.

Timing Diagram 7-18. Direct Slave Burst Write of 4 Dwords (8-Bit Local Bus)
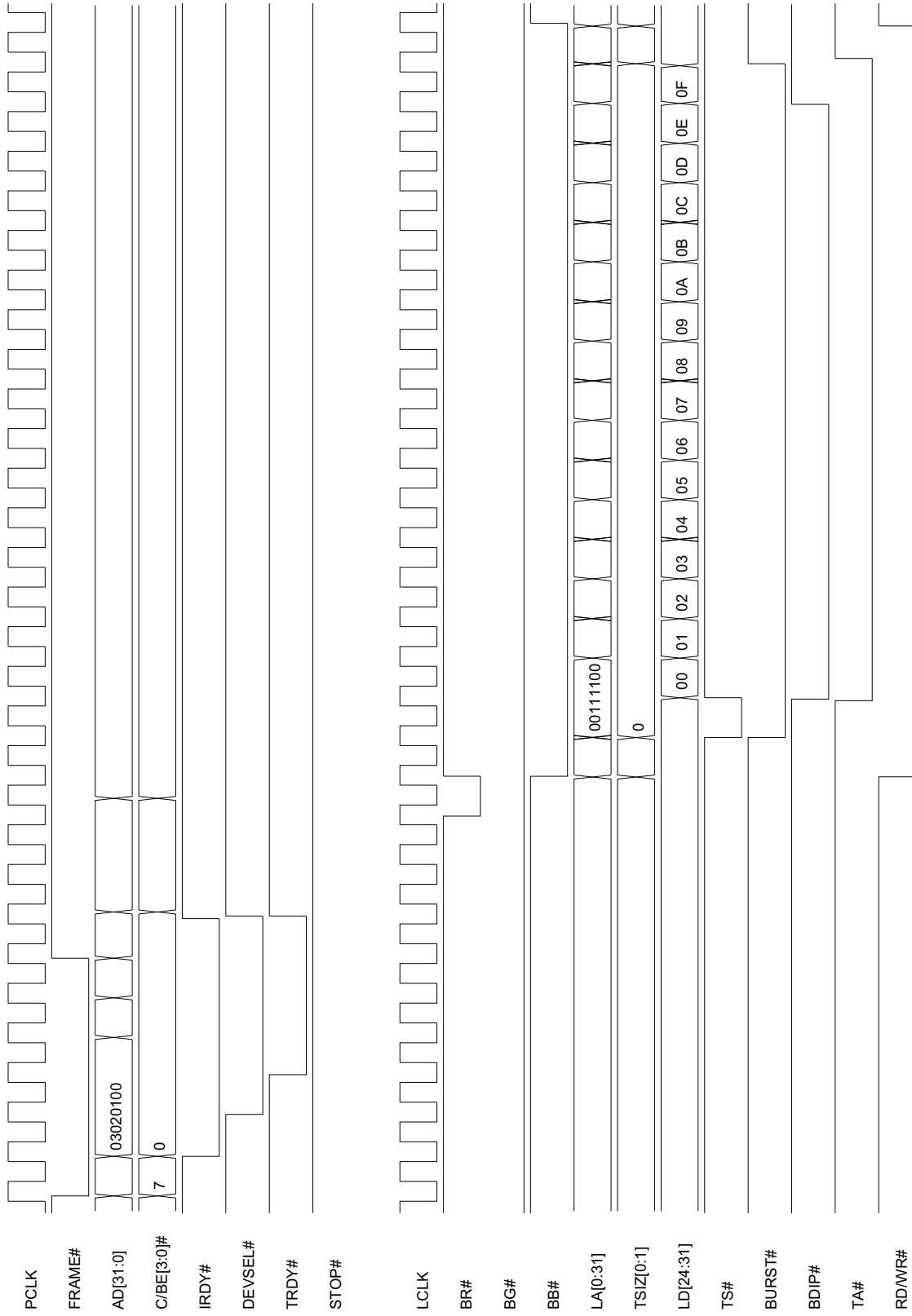
Note: *Key bit/register values are LCS_MARBR[24]=0, LCS_BIGEND[4]=0, and LCS_LBRD1[15:0]=25C0h.*

Timing Diagram 7-19. Direct Slave Burst Write of 4 Dwords (16-Bit Local Bus)
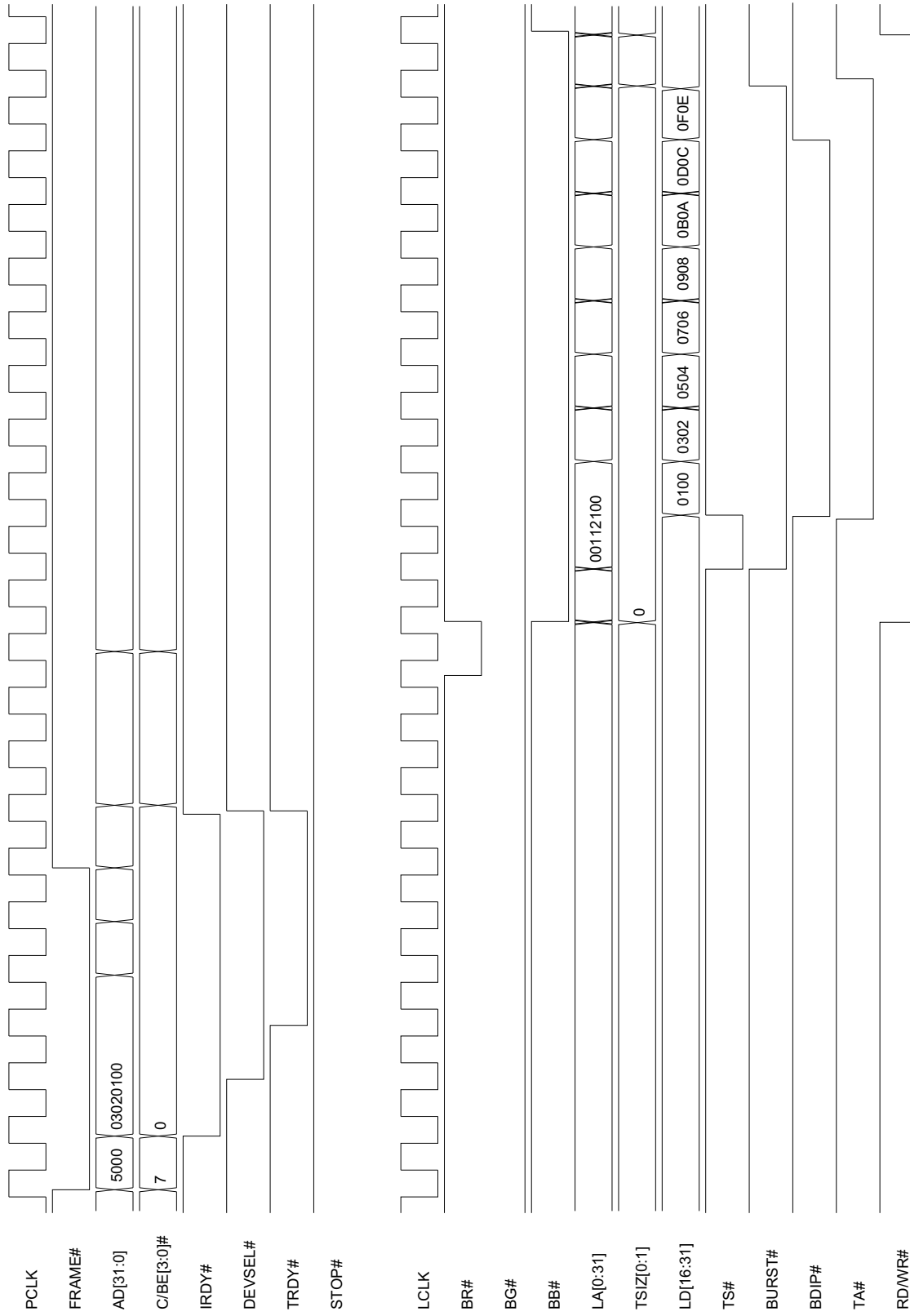
PCLK
FRAME#
AD[31:0]
C/BE[3:0]#
IRDY#
DEVSEL#
TRDY#
STOP#

LCLK
BR#
BG#
BB#
LA[0:31]
TSIZ[0:1]
LD[16:31]
TS#
BURST#
BDIP#
TA#
RD/WR#

Note: Key bit/register values are LCS_MARBR[24]=1, LCS_BIGEND[4]=0, and LCS_LBRD1[15:0]=25C1h.

Timing Diagram 7-20. Direct Slave Burst Write of 4 Dwords (32-Bit Local Bus)

PCLK

FRAME#

AD[31:0]   5000   03020100

C/BE[3:0]#   7   0

IRDY#

DEVSEL#

TRDY#

STOP#

LCLK

BR#

BG#

BB#

LA[0:31]   00110000

TSIZ[0:1]   0

LD[0:31]

TS#

BURST#

BDIP#

TA#

RD/WR#
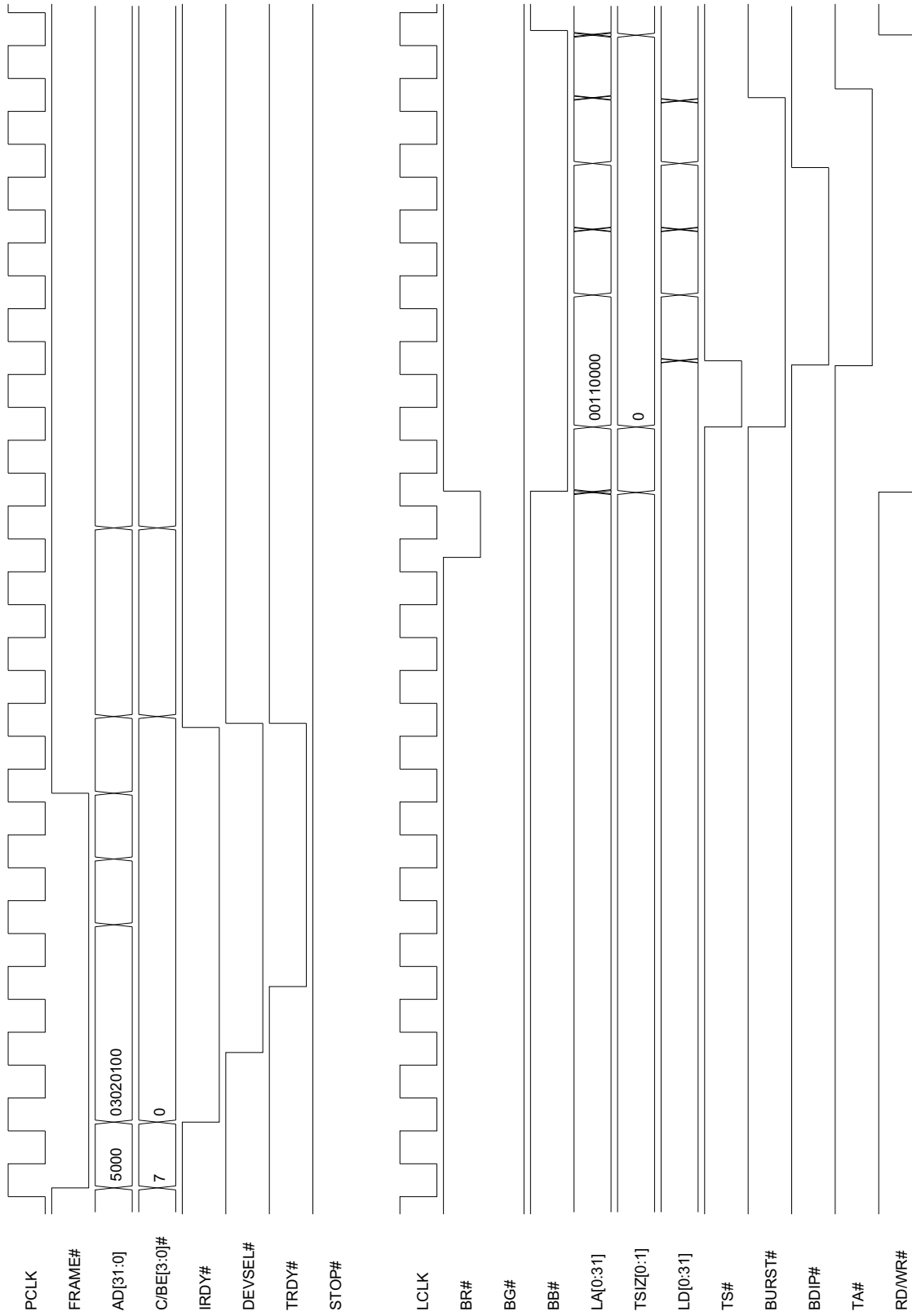
Note: Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=25C2h.

Timing Diagram 7-21. Direct Slave Burst Read of 4 Dwords (8-Bit Local Bus)
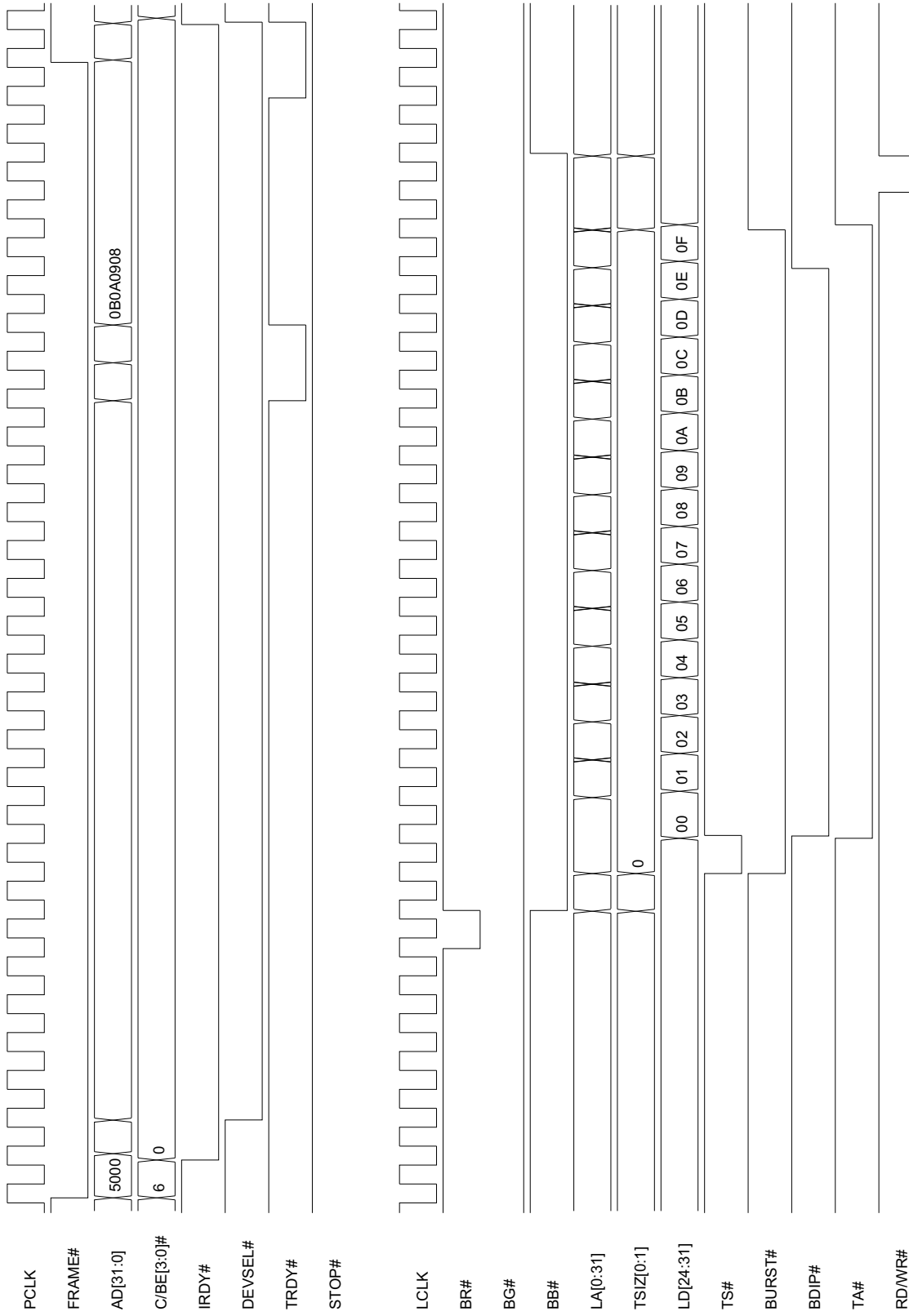
PCLK
FRAME#
AD[31:0]
C/BE[3:0]#
IRDY#
DEVSEL#
TRDY#
STOP#

LCLK
BR#
BG#
BB#
LA[0:31]
TSIZ[0:1]
LD[24:31]
TS#
BURST#
BDIP#
TA#
RD/WR#

Note: *Key bit/register values are LCS_MARBR[24]=0, LCS_BIGEND[4]=0, and LCS_LBRD1[15:0]=25C0h.*

Timing Diagram 7-22. Direct Slave Burst Read of 4 Dwords (16-Bit Local Bus)
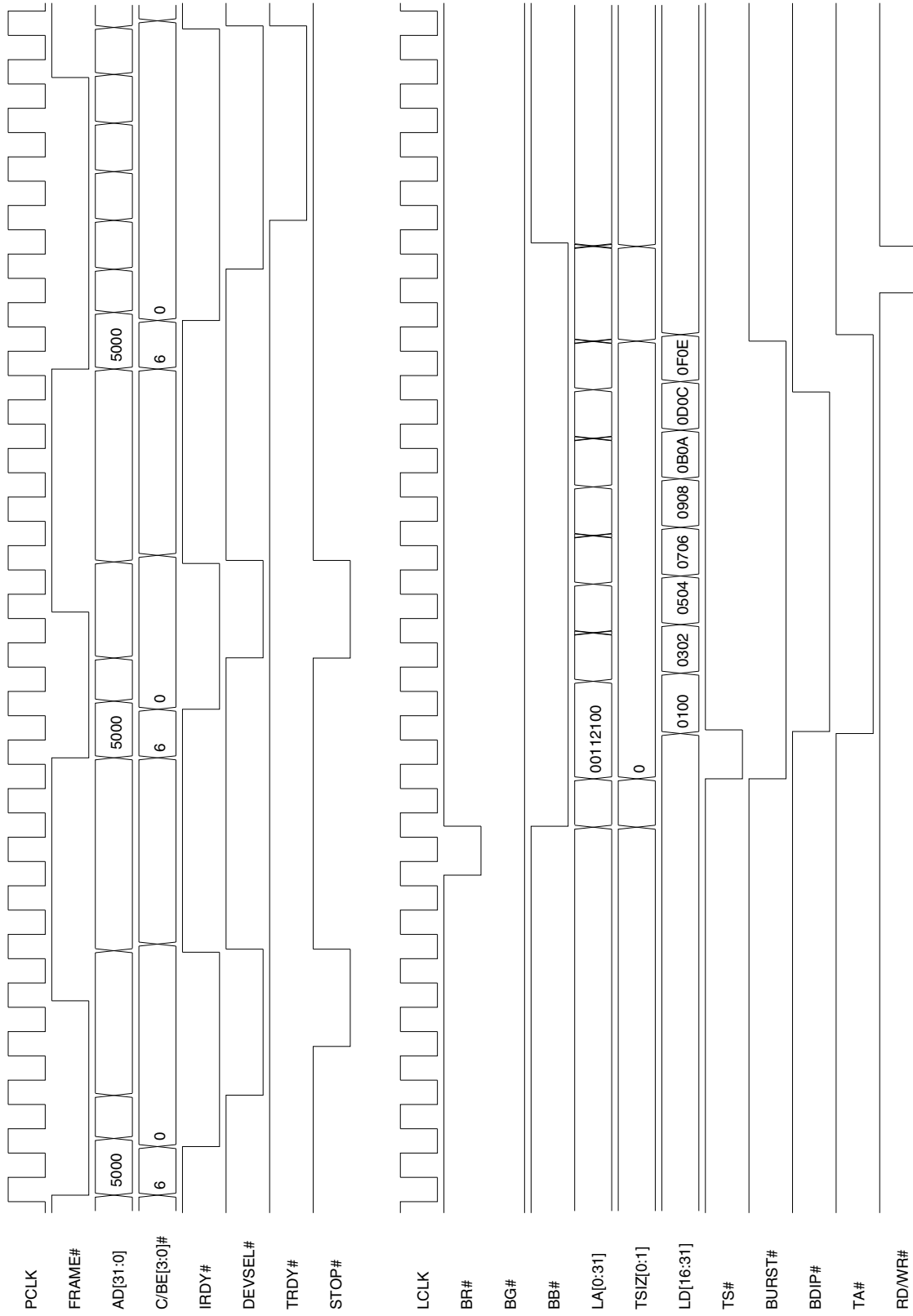
Note: *Key bit/register values are LCS_MARBR[24]=0, LCS_BIGEND[4]=0, and LCS_LBRD1[15:0]=25C1h.*

Timing Diagram 7-23. Direct Slave Burst Read of 4 Dwords (32-Bit Local Bus)

PCLK

FRAME#

AD[31:0]   5000

C/BE[3:0]#   6   0

IRDY#

DEVSEL#

TRDY#

STOP#

LCLK

BR#

BG#

BB#

LA[0:31]   00110000

TSIZ[0:1]   0

LD[0:31]

TS#

BURST#

BDIP#

TA#

RD/WR#
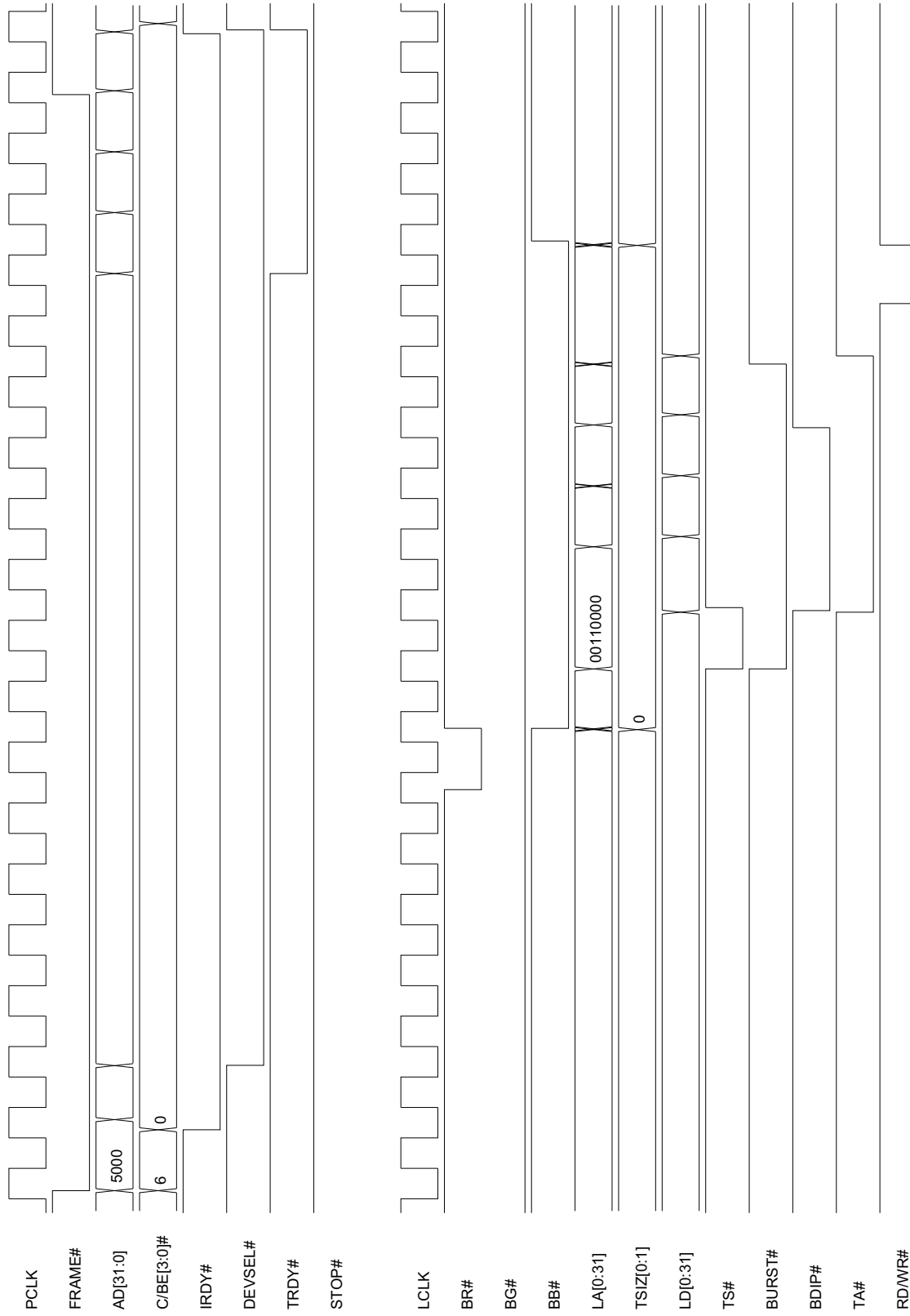
Note: *Key bit/register values are LCS_MARBR[24]=0 and LCS_LBRD1[15:0]=25C2h.*

7.3.4   M Mode DMA Timing Diagrams

Timing Diagram 7-24. DMA PCI-to-Local, Continuous Burst Mode, with EOT# Assertion
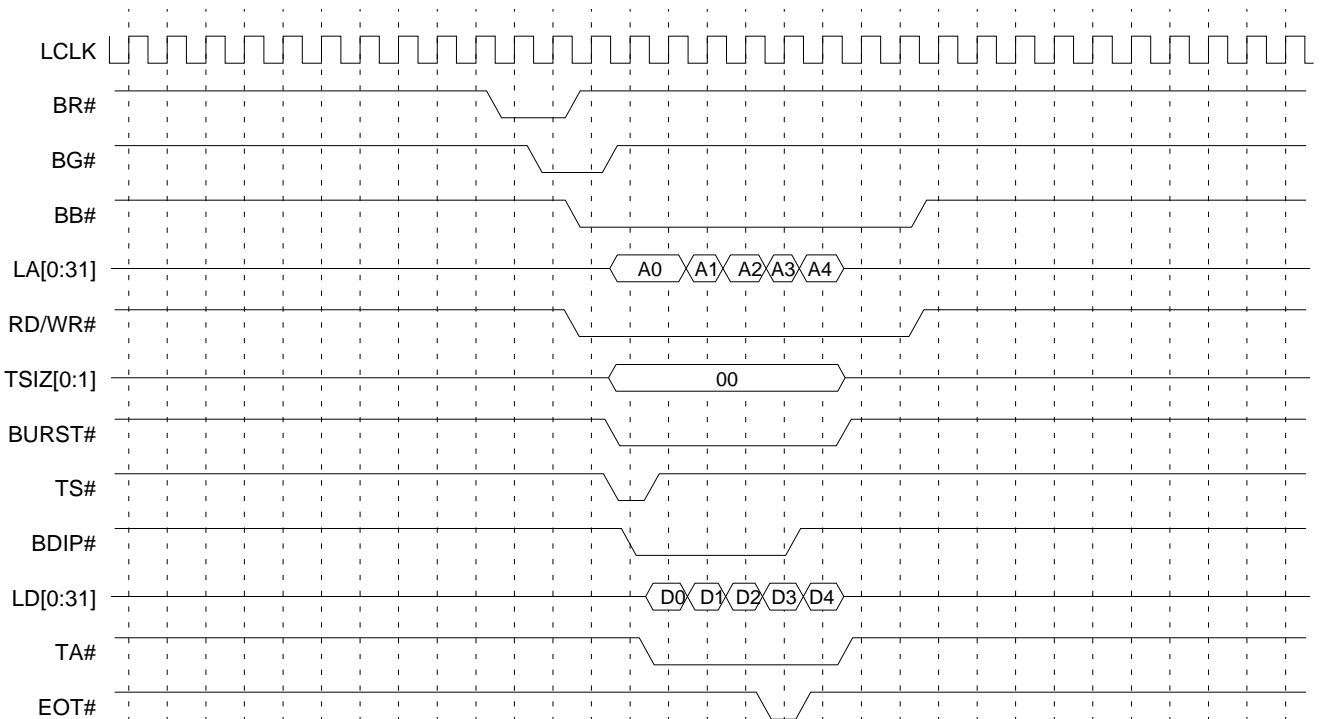
Note: *For a PCI-to-Local DMA with EOT# assertion, all data read by the PEX 8311 from the PCI Bus is not necessarily written to the Local Bus – any data that is not written to the Local Bus due to EOT# assertion is flushed. For this example, the DMA Transfer Size Count is assumed to be greater than or equal to the size of the transfer shown.*

Timing Diagram 7-25. DMA Local-to-PCI, Continuous Burst Mode, with EOT# Assertion
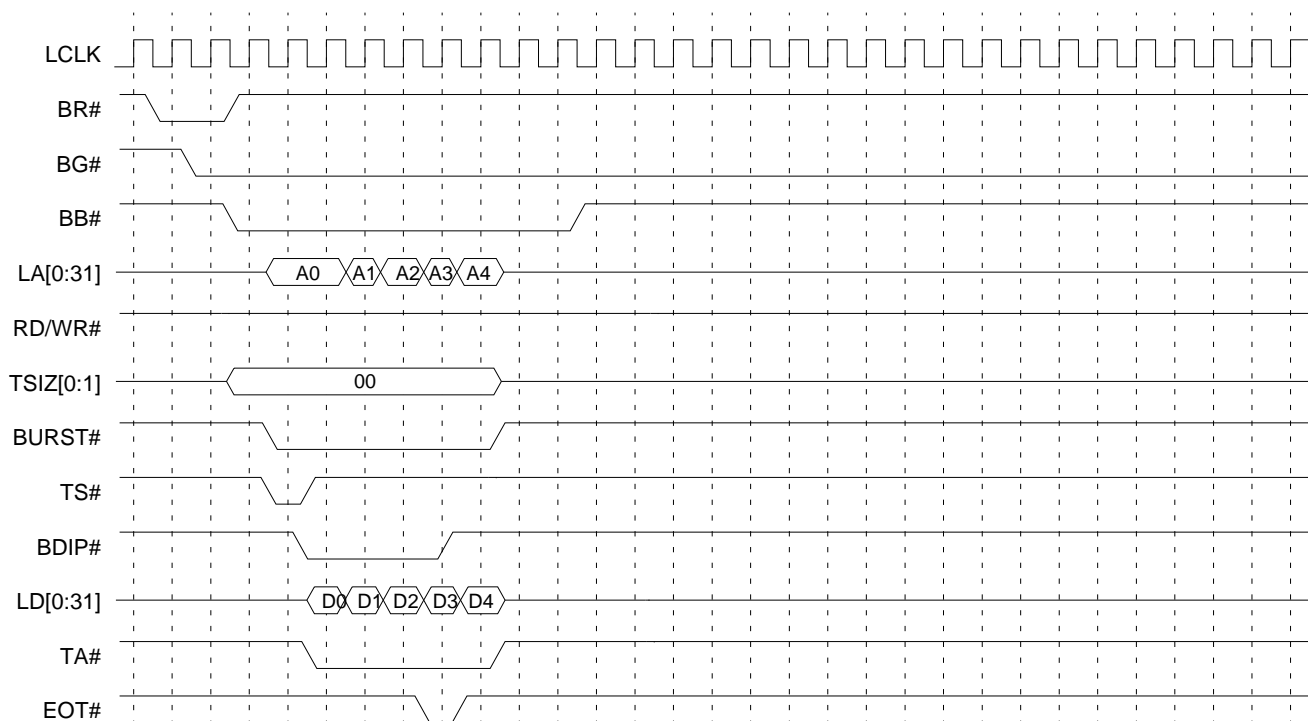
Note: *For a Local-to-PCI DMA with EOT# assertion, all data read by the PEX 8311 from the Local Bus is written to the PCI Bus. For this example, the DMA Transfer Size Count is assumed to be greater than or equal to the size of the transfer shown.*

**Timing Diagram 7-26. Local Bus Latency Timer (Eight Clocks) and Pause Timer (Four Clocks)
in DMA Operation**

LCLK

BR#

Local Bus Pause Timer expires, resume DMA operation

BG#

Kick off Local Bus Latency Timer

BB#

Kick off Local Bus Pause Timer

TS#

Local Bus Latency Timer expires --> PEX 8311 releases Local Bus after last data
(transferred or up to Quad-Dword boundary during burst)

TA#

RD/WR#
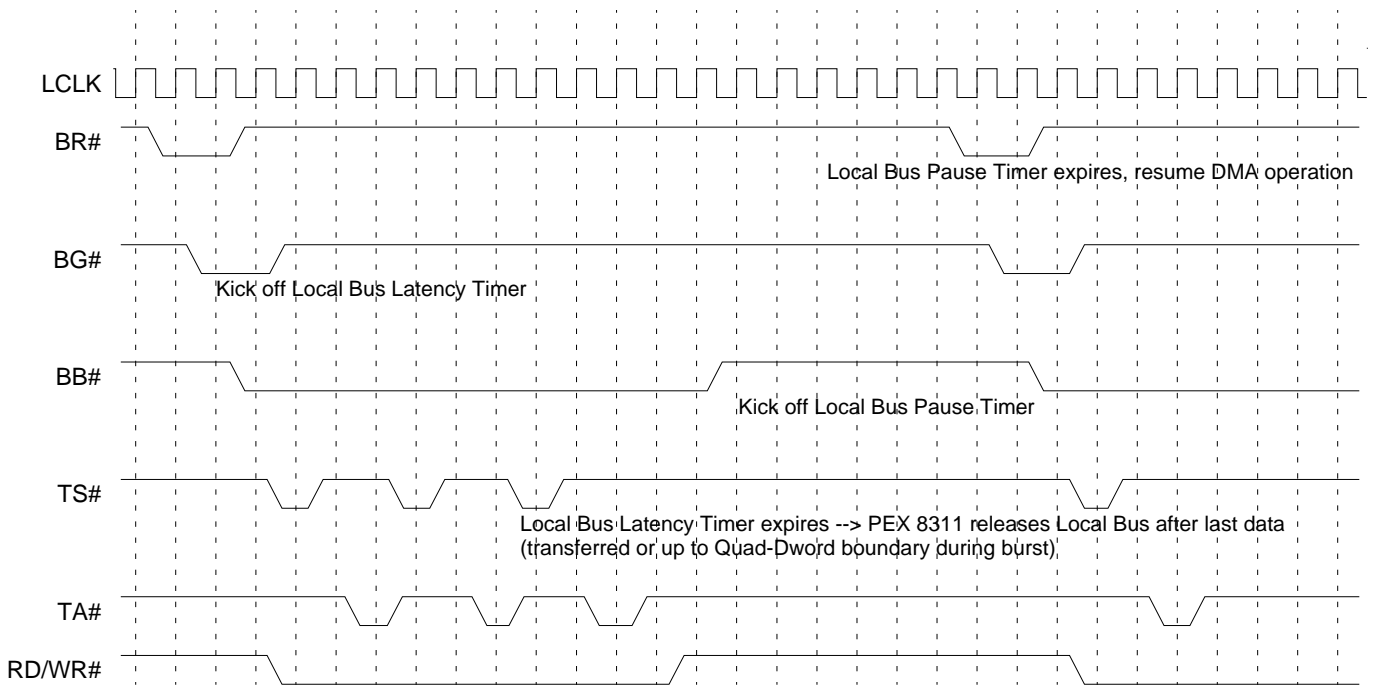
**Timing Diagram 7-27. Local Bus Latency Timer (Eight Clocks) and Pause Timer (Four Clocks)
in DMA Operation, Continuous Burst Mode**

LCLK

BR#

Local Bus Pause Timer expires, resume DMA operation

BG#

(BG#) Kick off Local Bus Latency Timer

BB#

(BB# de-asserts) Kick off Local Bus Pause Timer

TS#

Local Bus Latency Timer expires --> PEX 8311 finishes current data and one more
data is transferred before releasing the Local Bus (de-asserts BB#)

TA#

RD/WR#
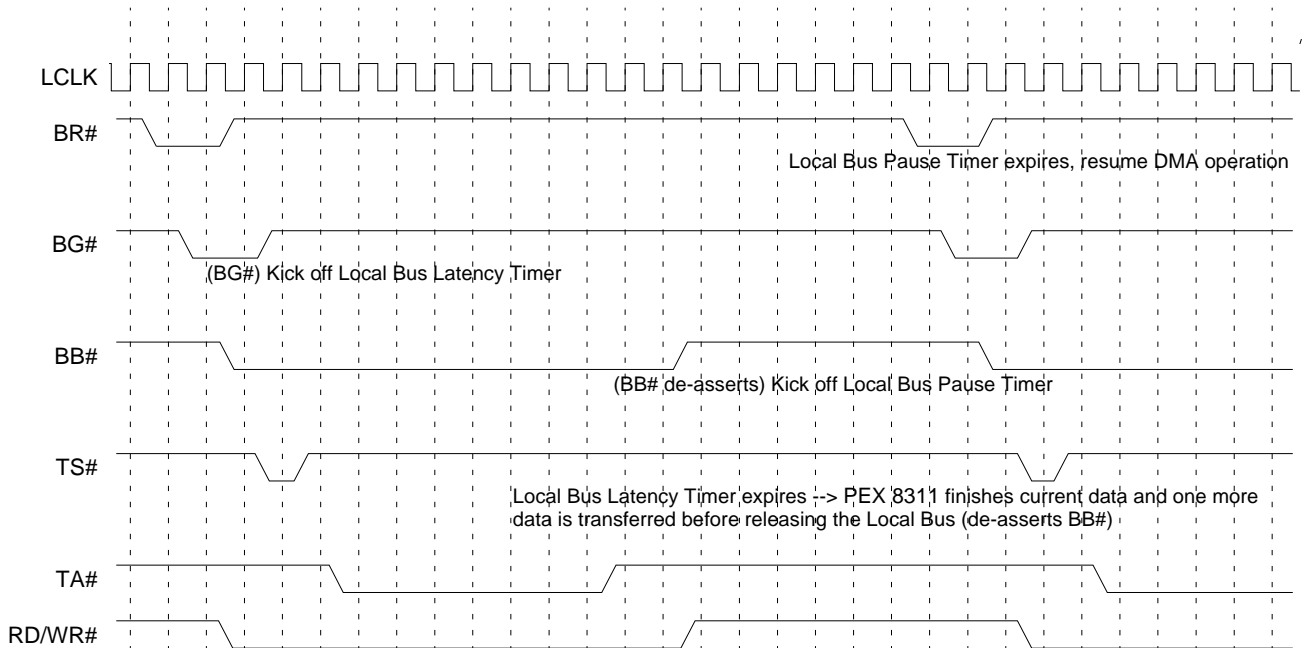
Timing Diagram 7-28. DMA PCI-to-Local, Continuous Burst Mode, Transfer Size = 10 Dwords
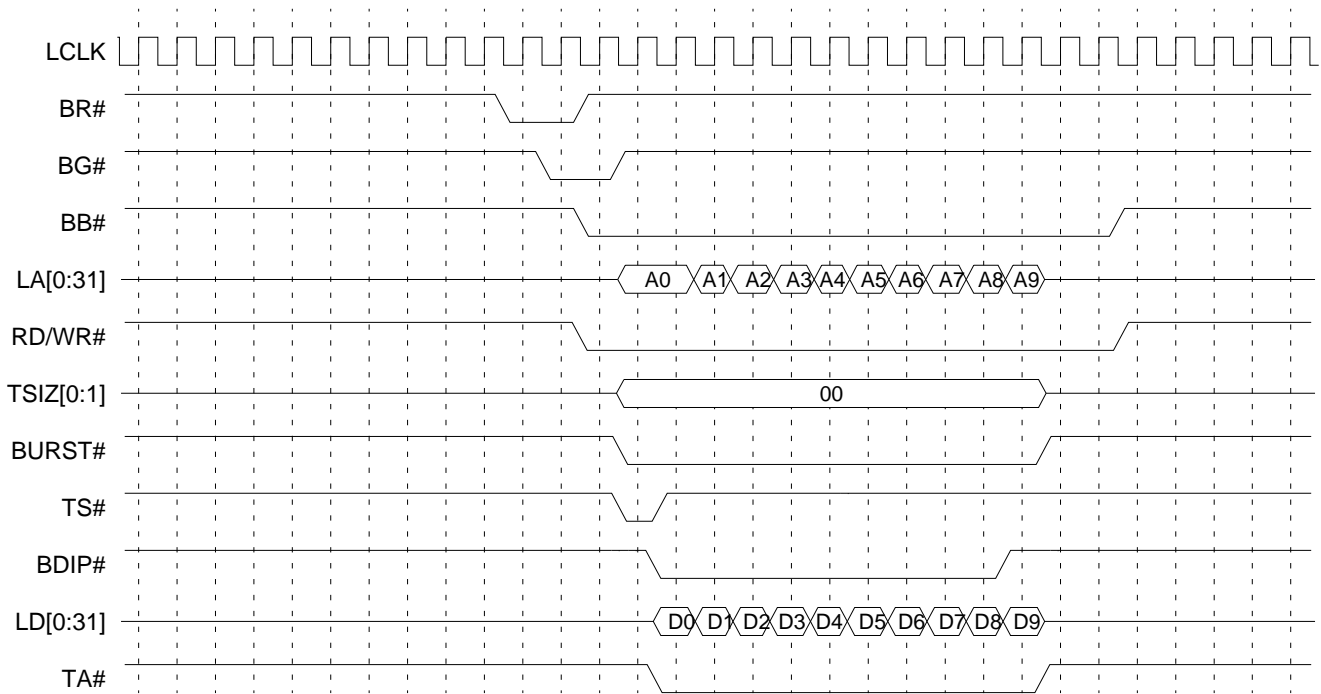
Timing Diagram 7-29. DMA Local-to-PCI, Continuous Burst Mode, Transfer Size = 10 Dwords
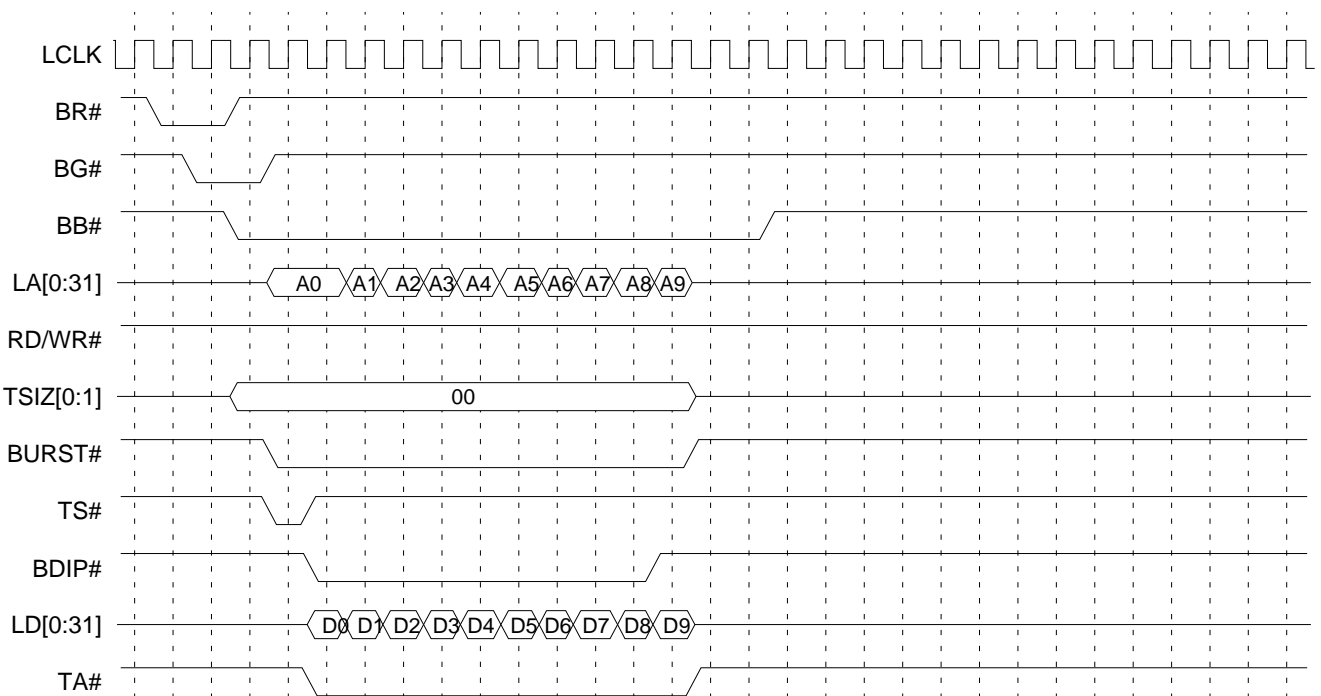
Timing Diagram 7-30. IDMA Single Write Cycle
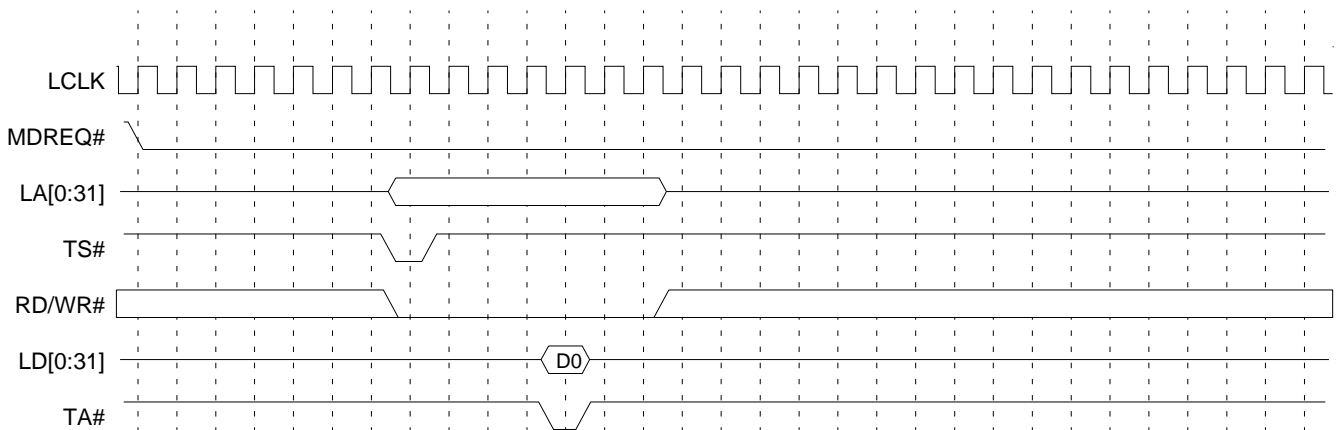
Note: *The PEX 8311 treats the IDMA function from the MPC850 or MPC860 the same as a Direct Master cycle.*

The MPC850 or MPC860 starts the IDMA cycle when the IDMA Enable bit is set in the respective MPC850 or MPC860 register.

User must clear the IDMA Enable bit when the MPC850 or MPC860 is done (monitor interrupt) with the IDMA cycle.

Timing Diagram 7-31. DMA PCI-to-Local (32-Bit Local Bus)
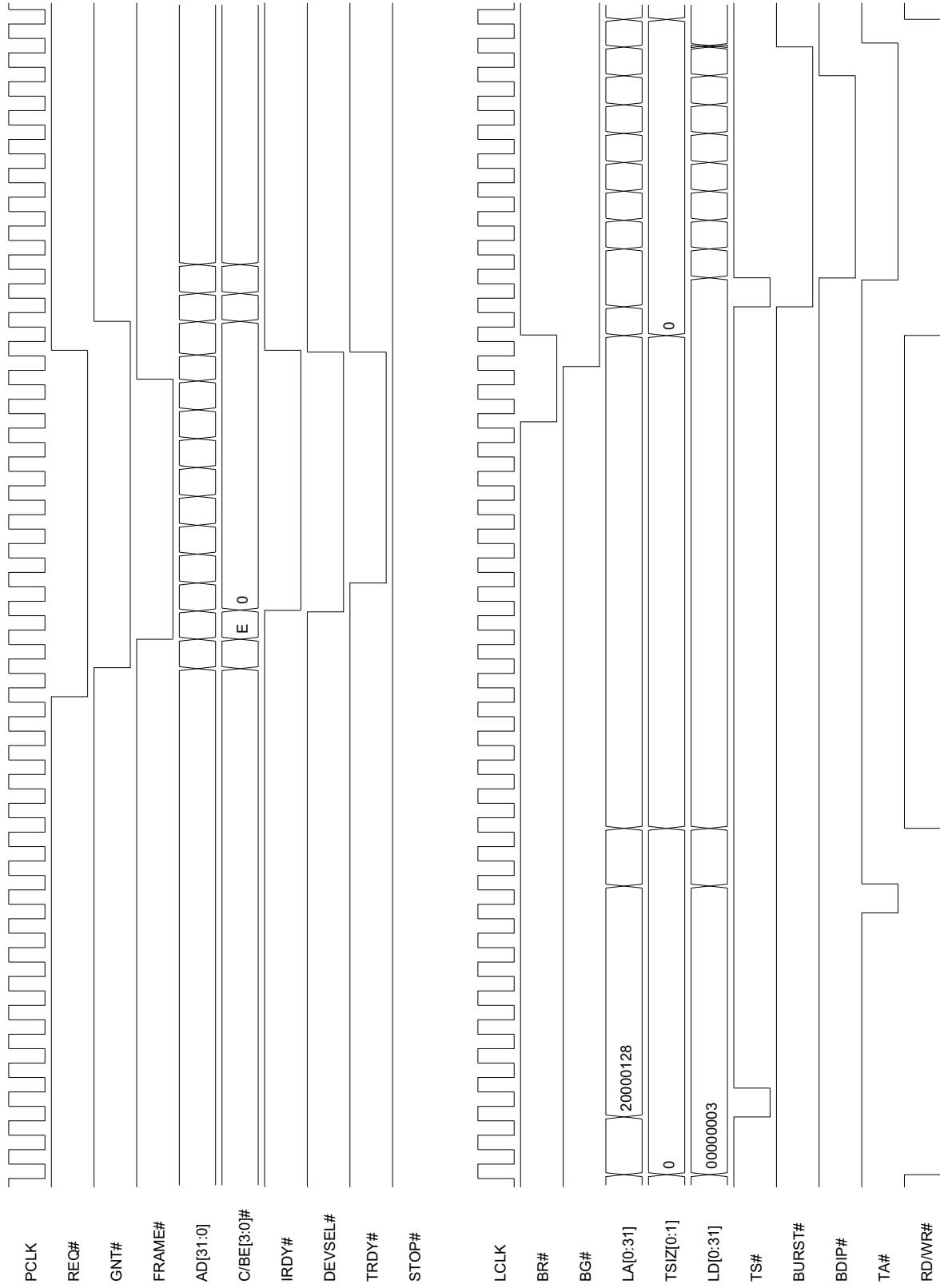
PCLK
REQ#
GNT#
FRAME#
AD[31:0]
C/BE[3:0]#
IRDY#
DEVSEL#
TRDY#
STOP#

LCLK
BR#
BG#
LA[0:31] 20000128
TSIZ[0:1] 0
LD[0:31] 00000003
TS#
BURST#
BDIP#
TA#
RD/WR#

Notes: *The writing of the registers to set up this 32-byte DMA Block mode transfer using DMA Channel x is not shown.*

Writing the LCS_DMACSR0/1 register (LOC:128h, 129h) with 03h enables and starts this DMA transfer.

Timing Diagram 7-32. DMA Local-to-PCI (32-Bit Local Bus)
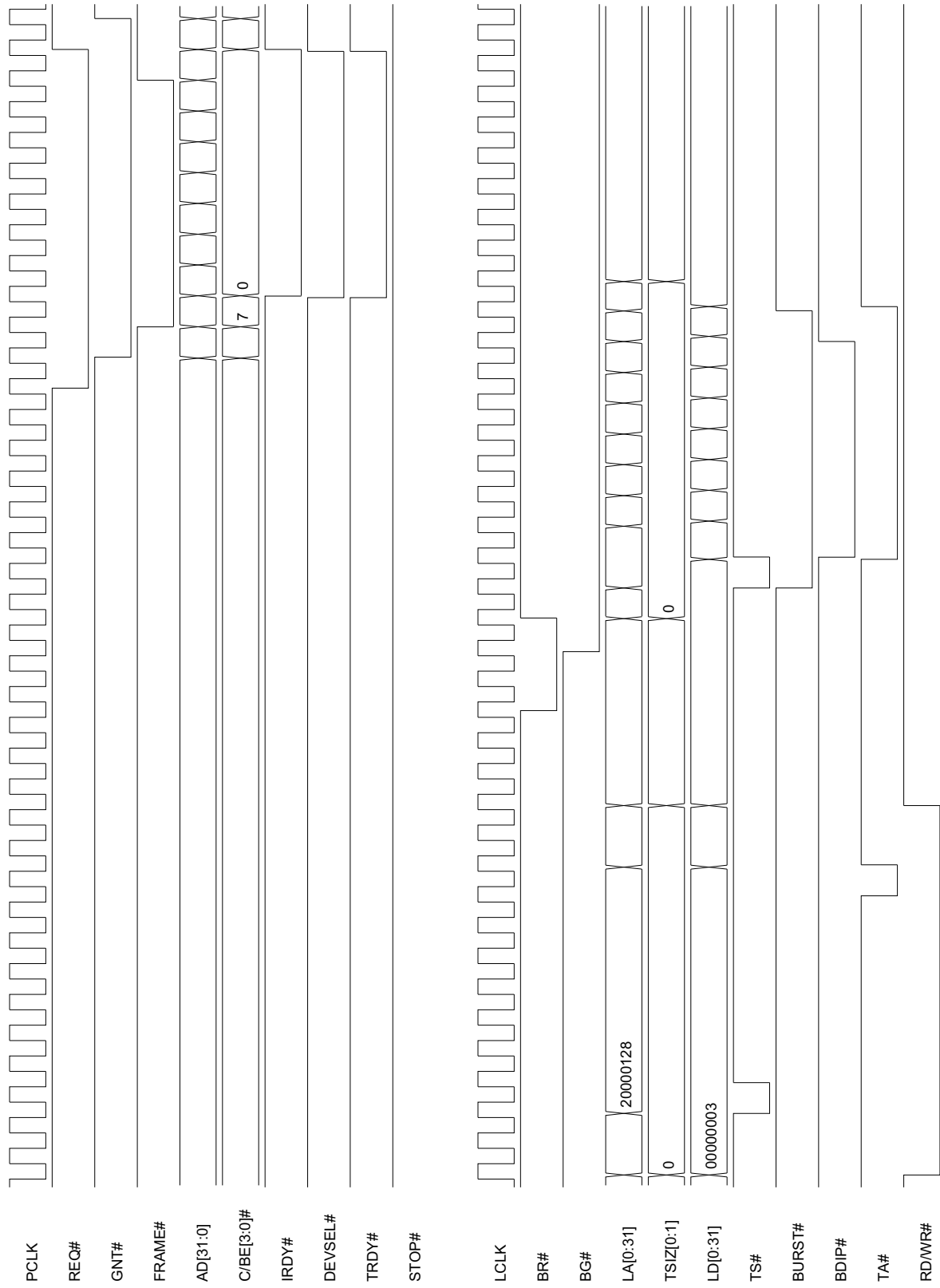
PCLK
REQ#
GNT#
FRAME#
AD[31:0]
C/BE[3:0]#
IRDY#
DEVSEL#
TRDY#
STOP#

LCLK
BR#
BG#
LA[0:31]
TSIZ[0:1]
LD[0:31]
TS#
BURST#
BDIP#
TA#
RD/WR#

Notes: *The writing of the registers to set up this 32-byte DMA Block mode transfer using DMA Channel x is not shown.*

Writing the LCS_DMACSR0/1 register (LOC:128h, 129h) with 03h enables and starts this DMA transfer.

Timing Diagram 7-33. DMA PCI-to-Local Demand Mode (32-Bit Local Bus)
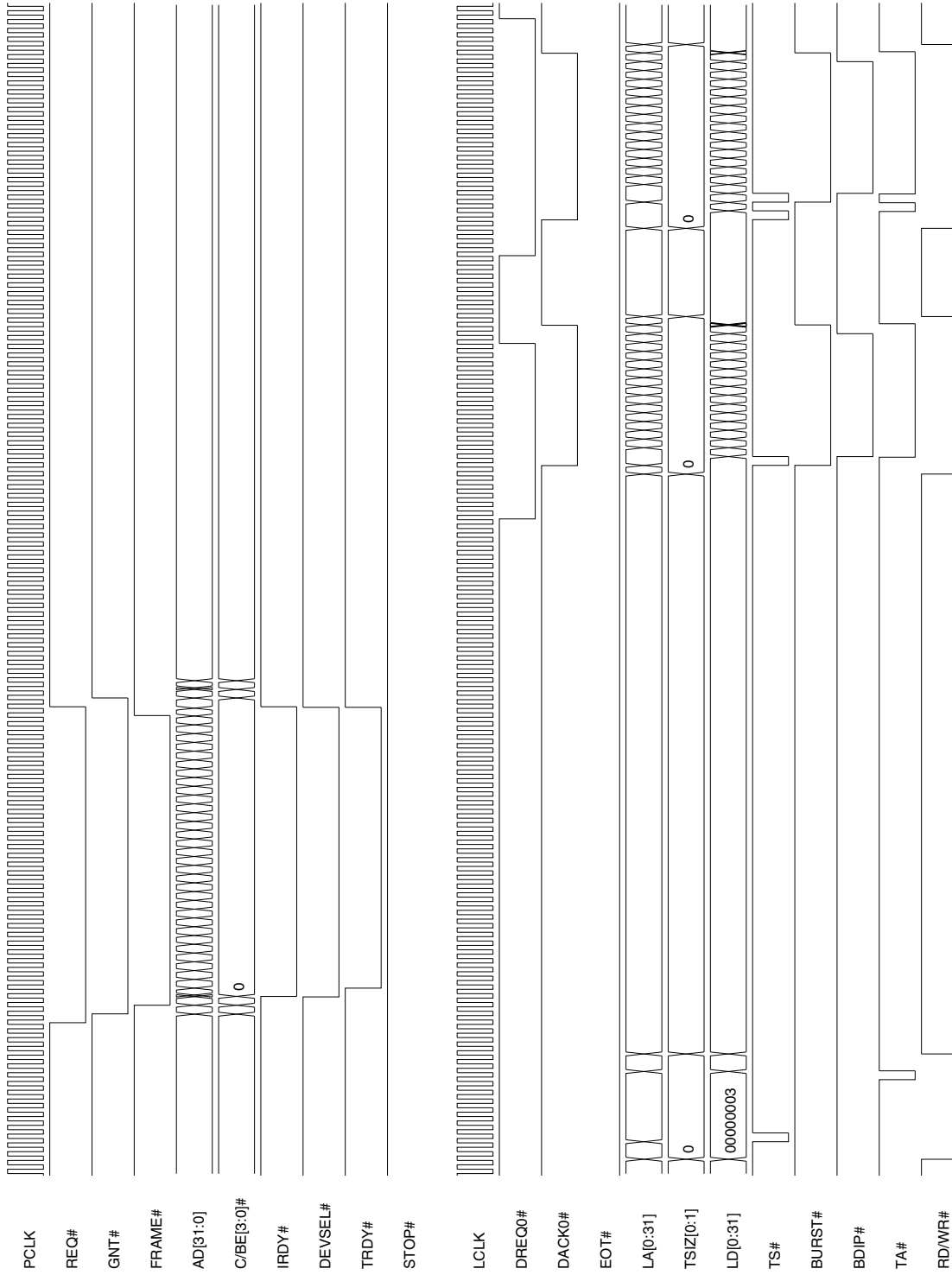
Notes: *The Channel x Demand mode DMA transfer starts when the LCS_DMACSR0/1[1:0] bits are written to 11b.*

The PEX 8311 does not attempt to arbitrate for and write data to the Local Bus until it detects that the DREQx# signal asserted.

The transfer is temporarily suspended when DREQx# is de-asserted, then resumed upon its re-assertion.

Timing Diagram 7-34. DMA Local-to-PCI Demand Mode (32-Bit Local Bus)

PCLK

REQ#

GNT#

FRAME#

AD[31:0]

C/BE[3:0]#

IRDY#

DEVSEL#

TRDY#

STOP#

LCLK

DREQ0#

DACK0#

EOT#

LA[0:31]

TSIZ[0:1]

LD[0:31]

TS#

BURST#

BDIP#

TA#

RD/WR#
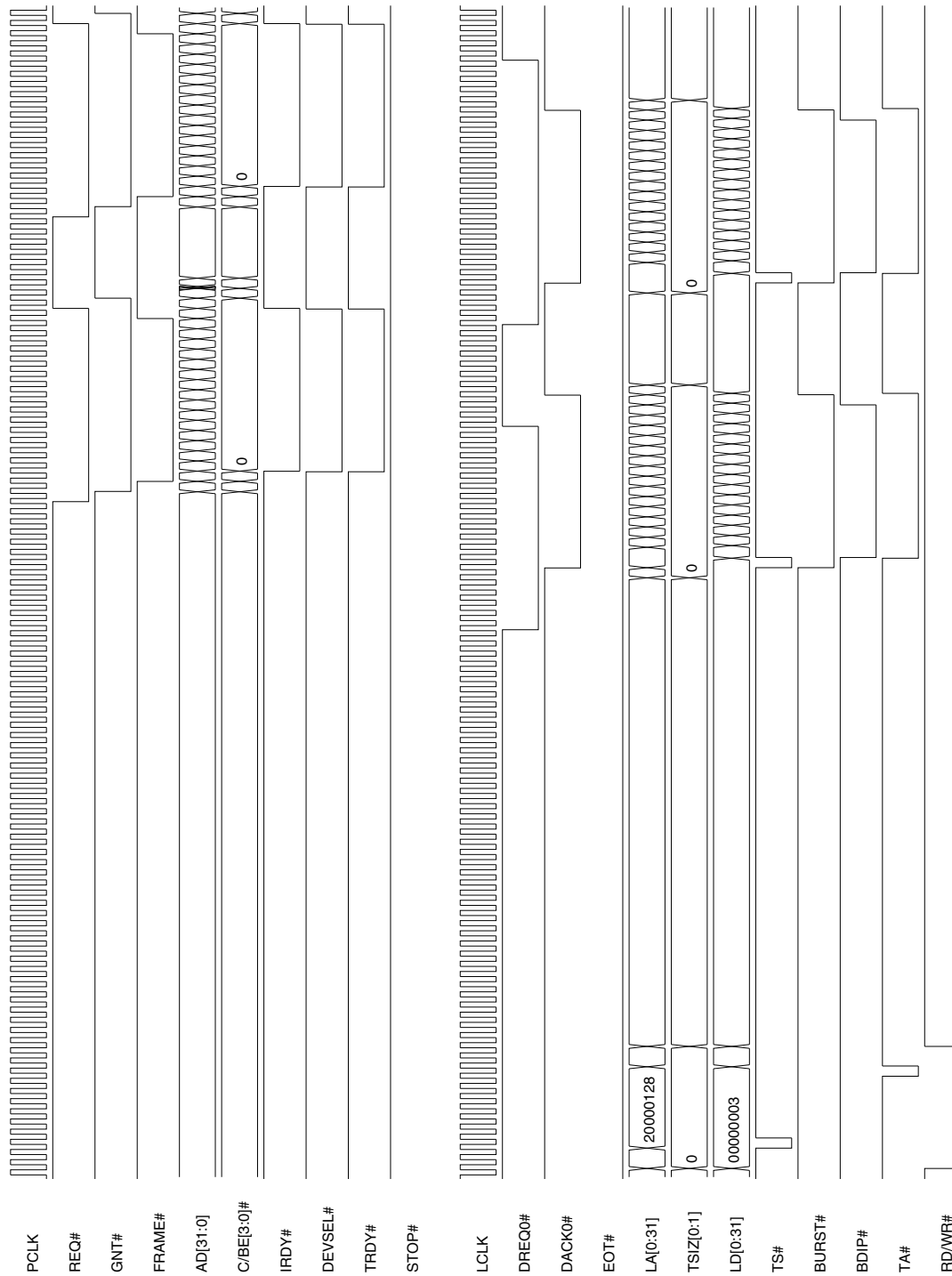
Notes: *The Channel 0 Demand mode DMA transfer starts when the LCS_DMACSR0/1[1:0] bits are written to 11b and*

the PEX 8311 detects the DREQ0# signal asserted. Once started, the PEX 8311 arbitrates for and reads data from the Local Bus,

then writes the data to the PCI Bus until the transfer is temporarily suspended when DREQ0# is de-asserted. The transfer resumes upon DREQ0# re-assertion.

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Chapter 8   PCI Express Bridge
Transaction Forwarding

8.1   Introduction

The PEX 8311 is a multi-function device, consisting of a PCI Express-to-PCI bridge function that is internally hardwired to a PCI-to-Local Bus bridge function. *That is*, there are two sets of Configuration registers to program (**PECS** and **LCS**), as well as two levels of Transaction Forwarding rules that are applied to all transactions forwarded from one bridge to the other, to registers or shared memory. This chapter describes the Address Mapping options and Transaction Forwarding rules specific to the PEX 8311 PCI Express bridge function.

When the PEX 8311 is configured as an endpoint (Endpoint mode – ROOT_COMPLEX# is strapped High), its primary (or upstream-facing) interface is PCI Express, and its secondary (or downstream-facing) interface is Local Bus. When ROOT_COMPLEX# is strapped Low (Root Complex mode), the direction of each interface is reversed. Table 8-1 defines which interface is primary (upstream) or secondary (downstream) for the two PEX 8311 bridge modes.

For transactions originating in PCI Express Space, the PEX 8311 uses the five Address spaces defined in the *PCI Express-to-PCI/PCI-X Bridge r1.0*, Chapter 3, which are as follows:

- PCI-Compatible Configuration Space (Type 1)
- PCI Express Enhanced Configuration Space
- Memory-Mapped I/O (32-bit Address window, Non-Prefetchable)
- Prefetchable Memory Space (32- or 64-bit Address window)
- I/O Space (32-bit Address window)

The first two spaces are available only to the primary, or upstream-facing port, and provide the upstream processor with exclusive programming access to the PEX 8311 PCI-Compatible and PCI Express Enhanced Configuration registers. (Refer to Table 8-1.)

Table 8-1.   Primary and Secondary Interface Definitions for Endpoint and Root Complex Modes

ROOT_COMPLEX#	Bridge Mode	Primary Interface (Upstream)	Secondary Interface (Downstream)
High	Endpoint	PCI Express	Local
Low	Root Complex	Local	PCI Express

8.2   Endpoint Configuration Space Mapping

In Endpoint mode (ROOT_COMPLEX# strapped High), **PECS** PCI-Compatible Configuration and **PECS** PCI Express Enhanced Configuration spaces are available only to the PCI Express Interface, and cannot be programmed by way of the Local Bus bridge.

The other three Address spaces – Memory-Mapped I/O, Prefetchable Memory, or Conventional PCI I/O – determine which transactions to forward downstream or upstream. The Memory Base, Remap, and I/O ranges are defined by a set of **Base**, **Remapped**, and **Limit** registers in the Configuration header.

Shared Memory, Direct Slave, and Expansion ROM are mapped as either Memory-Mapped I/O, Prefetchable Memory, or Conventional PCI I/O to these three Address spaces on the PCI Express bridge. Mapping options are selected by way of **LCS** Configuration registers. **LCS** Configuration registers are loaded by **LCS** serial EEPROM or by a Local Master using CCS# accesses on a Local Bus. Transactions forwarded through the PCI Express bridge that do not decode must be 32-bit address only, and must decode into one of the Local Bus bridge's mapped Address ranges, or they may be returned as a Master Abort on the internal PCI Bus.

From the Local Bus viewpoint, all PCI Express bridge **PECS** registers, Memory-Mapped I/O, Prefetchable (32- or 64-bit) Memory, or I/O spaces are accessible by way of the Direct Master channel on the Local Bus bridge. DMA transfers are limited to Memory spaces only. Transactions originating on the Local Bus bridge that do not satisfy Forwarding rules on the PCI Express bridge can be returned as a Master Abort on the internal PCI Bus.

The remainder of this chapter describes Transaction Forwarding rules that are applied to transactions initiated on the PCI Express interface or Local Bus, for both Endpoint and Root Complex modes.

8.3   I/O Space

The I/O Address space determines whether to forward I/O Read or I/O Write transactions across the PEX 8311. PCI Express uses the 32-bit Short Address Format (DWORD-aligned) for I/O transactions.

8.3.1   Enable Bits

Two **PECS** Configuration register bits control I/O transaction forwarding through the PCI Express bridge:

- **PECS_PCICMD** register *I/O Access Enable*
- **PECS_PCICMD** register *Bus Master Enable*

The **PECS_PCICMD** *I/O Access Enable* bit must be set for I/O transactions to be forwarded downstream. When cleared, the following occurs:

- **Endpoint mode** (ROOT_COMPLEX# strapped High) – All I/O requests originating in PCI Express space are completed with Unsupported Request status. All Direct Master I/O accesses from the Local Bus are forwarded to PCI Express Space.
- **Root Complex mode** (ROOT_COMPLEX# strapped Low) – All Direct Master I/O accesses from the Local Bus terminate with Master Abort/LSERR# (if enabled). All I/O transactions originating on PCI Express are forwarded to the Local Bus bridge for decode.

The *Bus Master Enable* bit must be set for I/O transactions to be forwarded upstream. When cleared, the following occurs:

- **Endpoint mode** (ROOT_COMPLEX# strapped High) – All Direct Master I/O transactions forwarded from the Local Bus bridge are ignored, and result in a Master Abort on the internal PCI Bus. LSERR# can be asserted, if enabled.
- **Root Complex mode** (ROOT_COMPLEX# strapped Low) – All I/O requests originating in PCI Express space are completed with an Unsupported Request status.

The following **LCS** register bits control forwarding of I/O accesses originating in PCI Express Space through the Local Bus bridge:

- **LCS_PCICR** register *I/O Access Enable*
- **LCS_LAS0BA** *Local Address Space 0 Enable*
- **LCS_LAS0RR** *Memory Space 0 Indicator*
- **LCS_LAS1BA** *Local Address Space 1 Enable*
- **LCS_LAS1RR** *Memory Space 1 Indicator*

The following **LCS** register bits control forwarding of Direct Master I/O transactions (originating in Local space) to the PCI Express bridge:

- **LCS_PCICR** register *Bus Master Enable*
- **LCS_CNTRL** PCI Command Codes Control for Direct Master accesses

To enable I/O transaction forwarding from the PCI Express bridge I/O space to the Local Bus, by way of Direct Slave Space 0/1, the following registers must be set:

- I/O access must be enabled (**LCS_PCICR**[0]=1),
- One or more of the Local Address spaces must be enabled (**LCS_LAS0BA** and/or **LCS_LAS1BA**[0]=1), and
- The appropriate *Memory Space Indicator* bit must be set to map the Local Address space into I/O space (**LCS_LAS0RR** and/or **LCS_LAS1RR**[0]=1)

If any of these bits are not set, PCI Express I/O-initiated transactions that are mapped to disabled space are completed with Unsupported Request status.

The **PECS_PCICMD** and **LCS_PCICR** *Bus Master Enable* bits must be set for I/O transactions to be forwarded upstream.

- **Endpoint mode** (ROOT_COMPLEX# strapped High) – If these bits are not set, the Local Bus-initiated transactions to PCI Express (upstream) as an I/O transaction are stalled and a Local Bus error condition might occur.
- **Root Complex mode** (ROOT_COMPLEX# strapped Low) – If these bits are not set, the Local Bus-initiated transactions to PCI Express (downstream) as an I/O transaction are stalled and a Local Bus error condition might occur.

8.3.2   I/O Base, Space Base, Range, and Limit Registers

8.3.2.1   PECS I/O Base, Space Base, Range, and Limit Registers

The following **PECS** registers define the range of I/O addresses to forward across the PCI Express bridge:

- **PECS_IOBASE**[7:4] (corresponds to Address bits [15:12])
- **PECS_IOBASEUPPER**[15:0] (corresponds to Address bits [31:16])
- **PECS_IOLIMIT**[7:4] (corresponds to Address bits [15:12])
- **PECS_IOLIMITUPPER**[15:0] (corresponds to Address bits [31:16])

The PEX 8311 **PECS** I/O Base consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit register define bits [15:12] of the I/O Base address. The lower four bits of the 8-bit register determine the PEX 8311's I/O address capability. The 16 bits of the **PECS_IOBASEUPPER** register define bits [31:16] of the I/O Base address.

The **PECS** I/O Limit consists of one 8-bit register and one 16-bit register. The upper four bits of the 8-bit register define bits [15:12] of the I/O Limit. The lower four bits of the 8-bit register determine the PEX 8311's I/O address capability, and reflect the value of the same field in the **PECS_IOBASE** register. The 16 bits of the **PECS_IOLIMITUPPER** register define bits [31:16] of the I/O Limit address.

Because Address bits [11:0] are not included in the Address space decoding, the I/O Address range retains a granularity of 4 KB, and is always aligned to a 4-KB Address Boundary space. The maximum I/O range is 4 GB.

For 16-bit I/O addressing, when the **PECS_IOBASE** register has a value greater than the **PECS_IOLIMIT** register, the I/O range is disabled. For 32-bit I/O addressing, when the I/O Base specified by the **PECS_IOBASE** and **PECS_IOBASEUPPER** registers has a value greater than the I/O Limit specified by the **PECS_IOLIMIT** and **PECS_IOLIMITUPPER** registers, the I/O range is disabled. In these cases, I/O transactions are forwarded upstream, and no I/O transactions are forwarded downstream.

8.3.2.2   LCS I/O Base, Space Base, Range, and Limit Registers

The **LCS** registers described in this section are used to map resources on the Local Bus bridge, relative to I/O forwarding on the PCI Express bridge.

- **LCS_PCIBAR0** maps Memory Base Address for LCS Runtime, Messaging, and DMA registers
- **LCS_PCIBAR1** maps I/O Base Address for **LCS Runtime**, **Messaging**, and **DMA** registers

The following **LCS** registers are used to map access to the Local Bus by way of Direct Slave Space 0, for I/O accesses forwarded from PCI Express Space:

- **LCS_PCIBAR2** PCI Express Base Address for Accesses to Local Bus by way of Direct Slave Space 0
- **LCS_LAS0RR** Space 0 Range
- **LCS_LAS0BA** Space 0 Remap Address

The following **LCS** registers are used to map access to the Local Bus by way of Direct Slave Space 1, for I/O accesses forwarded from PCI Express Space:

- **LCS_PCIBAR3** PCI Express Base Address for Accesses to Local Address Space 1
- **LCS_LAS1RR** Space 1 Range
- **LCS_LAS1BA** Space 1 Remap Address

The following **LCS** registers are used to map access to the Local Bus by way of Expansion ROM space, for I/O accesses forwarded from PCI Express Space:

- **LCS_PCIERBAR** PCI Express Base Address for Local Expansion ROM)
- **LCS_EROMRR** Expansion ROM Range
- **LCS_EROMBA**[31:11] Expansion ROM Remap Address

The Local Bus bridge Direct Slave spaces (Space 0 and Space 1 only), when configured for I/O transactions, consist of a 32-bit PCI Express Base Address register for each Space in which bit 1 is always cleared to 0 and upper bits [31:2] are used as a PCI Express Base Address for access to Local Address.

Each Local Bus bridge Direct Slave space provides a dedicated 32-bit Direct Slave Local Address Range register. For I/O accesses, bit 1 is always cleared to 0 and upper bits [31:2] are used to define the range of each Direct Slave space.

Each Local Bus bridge Direct Slave space also provides a dedicated 32-bit Direct Slave Local Base Address Remap register that maps all incoming traffic from PCI Express (I/O space) to Local Bus. The upper bits [31:2] are used to map downstream traffic to the Local Bus. (Refer to Section 9.3, "Direct Slave Operation," for further details.)

The following **LCS** registers define Direct Master channel for Local-to-PCI Express I/O accesses:

- **LCS_DMRR** Direct Master I/O Range
- **LCS_DMLBAI** Direct Master I/O Remap Address
- **LCS_DMCFGA** Local Base Address for Accesses to PCI Express I/O Address
- **LCS_DMDAC** Direct Master PCI Express DAC Upper Address (must be cleared to 0)

By default, the Local Bus is a Memory-Mapped bus. Direct Master access to PCI Express I/O is supported when the *Direct Master I/O Access Enable* and *Master Enable* bits are set (**LCS_DMPBAM**[1]=1 and **LCS_PCICR**[2]=1, respectively).

The Direct Master space (Local-to-PCI Express Memory space), when configured for I/O transactions (**LCS_CNTRL**[15:8]), consists of a 32-bit Local Base Address register in which the upper 15 bits [31:16] are used for decoding Local Bus accesses. The Direct Master Base Address value must be multiple of the 64-KB Range value.

The Direct Master space provides a 32-bit Direct Master Range register, in which the upper 15 bits [31:16] are used to define a range of the Direct Master space.

The Direct Master space provides a dedicated 32-bit PCI Express Base Address Remap register. The upper 15 bits [31:16] are used to remap decoded Local Bus accesses to PCI Express I/O space and then to the PCI Express interface. (Refer to Section 9.2, "Direct Master Operation," for further details.)

DMA transactions are not supported in PCI Express I/O space.

PCI Express-initiated I/O transactions that fall within the range defined by the Base and Limit are forwarded to the Local Bus. Local Bus-initiated I/O transactions that are within the range are ignored. I/O transactions on the PEX 8311 upstream bus that do not fall within the range defined by the Base and Limit are ignored. I/O transactions on the PEX 8311 downstream bus that do not fall within the range are forwarded upstream. (Refer to Figure 8-1 and Figure 8-2.)

8.3.2.3   I/O Forwarding Illustrations

Figure 8-1 illustrates I/O forwarding in Endpoint mode. Figure 8-2 illustrates I/O forwarding in Root Complex mode.

Figure 8-1.   I/O Forwarding in Endpoint Mode
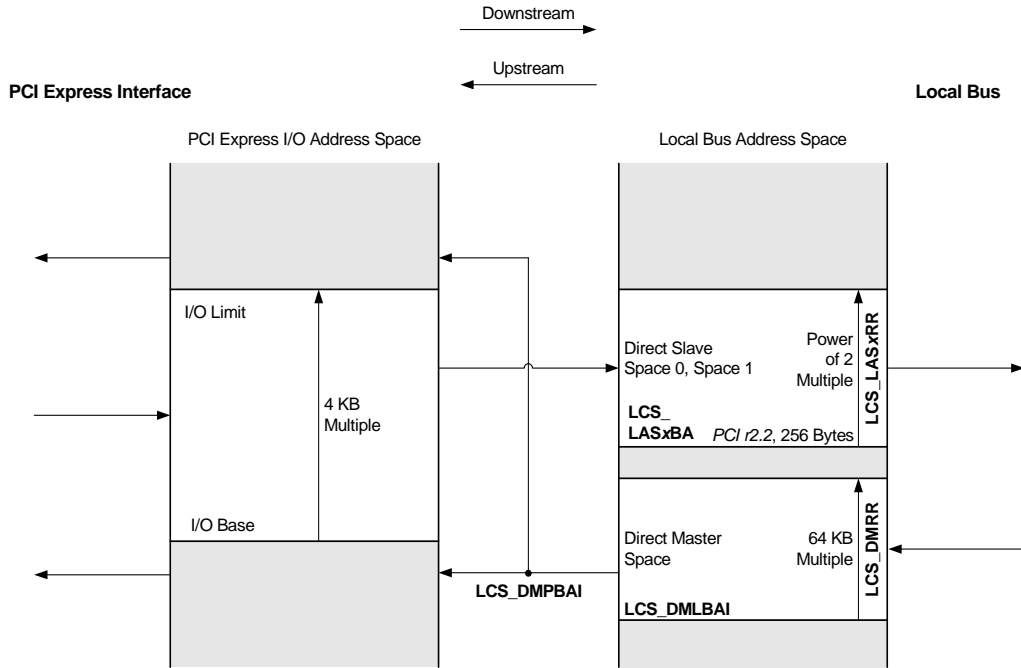
Figure 8-2.   I/O Forwarding in Root Complex Mode
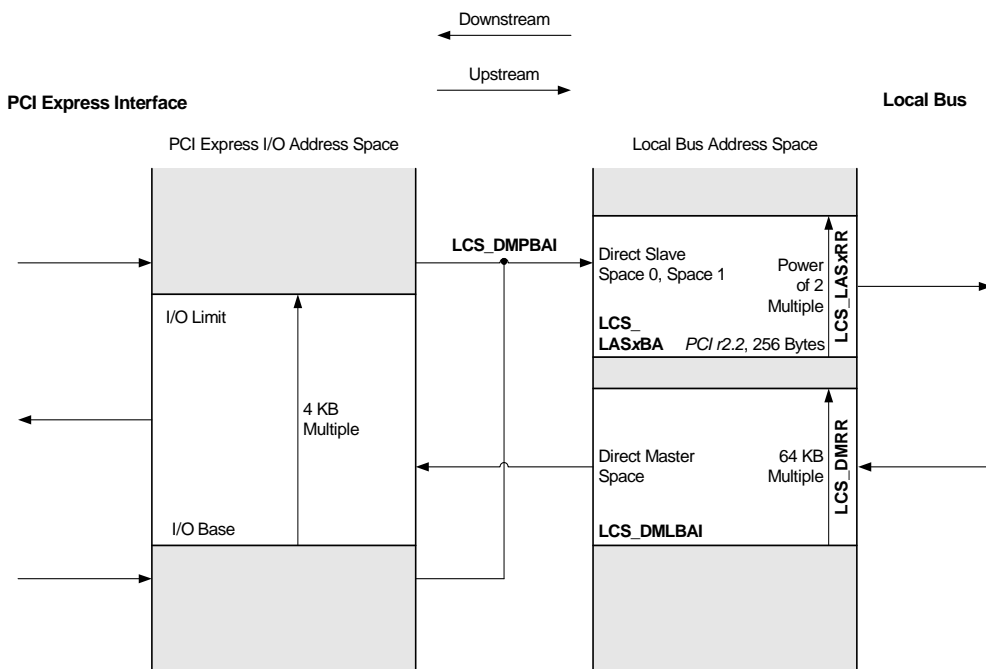
8.4   Memory-Mapped I/O Space

The Memory-Mapped I/O Address space determines whether to forward Non-Prefetchable Memory Read or Write transactions across the PEX 8311. For Local Bus-to-PCI Express Reads, prefetching occurs in this space only when the Memory Read Line or Memory Read Multiple commands are issued by the Direct Master Space and/or DMA Controller on the internal PCI Bus, because the transfer is mapped to Memory-Mapped I/O space on the PEX 8311 PCI Express interface. For PCI Express-to-Local Bus Reads, the Memory-Mapped I/O space is mapped to one of the Direct Slave spaces and the number of bytes to read is determined by the Memory Read Request TLP. Transactions that are forwarded using this Address space are limited to a 32-bit range.

8.4.1   Enable Bits

The following **PECS** register bits control Memory-Mapped I/O transaction forwarding between the Local Bus bridge and PCI Express Space:

- **PECS_PCICMD** register *Memory Space Enable*
- **PECS_PCICMD** register *Bus Master Enable*

The *Memory Space Enable* bit must be set for Memory transactions to be forwarded downstream. When cleared, the following occurs:

- **Endpoint mode** (ROOT_COMPLEX# strapped High) – All Non-Posted Memory requests originating in PCI Express space are completed with an Unsupported Request status, and Posted Write data is discarded. All Memory accesses forwarded from the Local Bus bridge are forwarded to PCI Express space.
- **Root Complex mode** (ROOT_COMPLEX# strapped Low) – All Memory accesses forwarded by the Local Bus bridge receive no response from the PCI Express bridge, and result in a Master Abort on the internal PCI Bus. All Non-Posted Memory requests originating in PCI Express Space are forwarded to the Local Bus bridge for decode.

The *Bus Master Enable* bit must be set for Memory transactions to be forwarded upstream. When cleared, the following occurs:

- **Endpoint mode** (ROOT_COMPLEX# strapped High) – All Memory accesses forwarded by the Local Bus bridge receive no response from the PCI Express bridge and result in a Master Abort on the internal PCI Bus.
- **Root Complex mode** (ROOT_COMPLEX# strapped Low) – All Non-Posted Memory requests originating in PCI Express Space are completed with an Unsupported Request status, and Posted Write data is discarded.

The following **LCS** register bits control the PEX 8311 response to re-map Memory-Mapped I/O transactions forwarded from PCI Express-to-Local Bus Spaces and onto the Local Bus:

- **LCS_PCICR** register *Memory Space Enable*
- **LCS_LAS0RR** *Memory Space 0 Indicator*
- **LCS_LAS0BA** *Local Address Space 0 Enable*
- **LCS_LAS1RR** *Memory Space 1 Indicator*
- **LCS_LAS1BA** *Local Address Space 1 Enable*
- **LCS_EROMRR** *Local Address Expansion ROM Enable*

The following **LCS** register bits control Direct Master or DMA Memory transaction forwarding to PCI Express Bridge Memory-Mapped I/O space:

- **LCS_PCICR** register *Bus Master Enable*
- **LCS_CNTRL** PCI Command Codes Control for Direct Master and DMA Accesses
    - **Endpoint mode** (ROOT_COMPLEX# strapped High) – If these bits are not set, Direct Master or DMA accesses to PCI Express result in a Master Abort on the internal PCI Bus. Posted Write data is discarded.
    - **Root Complex mode** (ROOT_COMPLEX# strapped Low) – If these bits are not set, Local Bus-initiated transactions to PCI Express Memory-Mapped I/O space (upstream) is stalled and Local Bus error conditions might occur.

8.4.2   Memory-Mapped I/O Transaction Forwarding Control Registers

8.4.2.1   PECS Memory-Mapped I/O Transaction Forwarding Control Registers

The following **PECS** registers are used to qualify Memory-Mapped I/O transactions. for forwarding across the PCI Express bridge:

- **PECS_MEMBASE**[15:4] (corresponds to Address bits [31:20])
- **PECS_MEMLIMIT**[15:4] (corresponds to Address bits [31:20])

PECS_MEMBASE[15:4] define bits [31:20] of the Memory-Mapped I/O Base address. **PECS_MEMLIMIT**[15:4] define bits [31:20] of the Memory-Mapped I/O Limit. Bits [3:0] of each register are hardwired to 0h.

Because Address bits [19:0] are not included in the Address space decoding, the Memory-Mapped I/O Address range retains a granularity of 1 MB, and is always aligned to a 1-MB Address Boundary space. The maximum Memory-Mapped I/O range is 4 GB.

If **PECS_MEMBASE** is programmed to a value greater than **PECS_MEMLIMIT**, the Memory-Mapped I/O range is disabled. In this case, Memory transaction forwarding is determined by the **PECS_PREBASE** and **PECS_PRELIMIT** registers.

8.4.2.2   LCS Memory-Mapped I/O Transaction Forwarding Control Registers

The **LCS** registers described in this section are used to map resources on the Local Bus bridge relative to Memory-Mapped I/O forwarding on the PCI Express bridge.

- **LCS_PCIBAR0** PCI Express Base Address for Memory accesses to **LCS Runtime**, **Messaging**, and **DMA** registers

The following **LCS** registers are used to map access to the Local Bus by way of Direct Slave Space 0, for Memory-Mapped I/O accesses forwarded from PCI Express Space:

- **LCS_PCIBAR2** PCI Express Base Address for Accesses to Local Address Space 0
- **LCS_LAS0RR** Space 0 Range
- **LCS_LAS0BA** Space 0 Remap Address

The following **LCS** registers are used to map access to the Local Bus by way of Direct Slave Space 1, for Memory-Mapped I/O accesses forwarded from PCI Express Space:

- **LCS_PCIBAR3** PCI Express Base Address for Accesses to Local Address Space 1
- **LCS_LAS1RR** Space 1 Range
- **LCS_LAS1BA** Space 1 Remap Address

The following **LCS** registers are used to map access to the Local Bus by way of Expansion ROM space, for Memory-Mapped I/O accesses forwarded from PCI Express Space:

- **LCS_PCIERBAR** PCI Express Base Address for Local Expansion ROM
- **LCS_EROMRR** Expansion ROM Range
- **LCS_EROMBA**[31:11] Expansion ROM Remap Address

The Local Bus bridge Direct Slave spaces (Space 0, Space 1, and Expansion ROM), when configured for Memory Transactions, consist of a 32-bit LCS PCI Base Address register for each space (**LCS_PCIBAR2** and **LCS_PCIBAR3**), in which bits [2:1] are always cleared to 00b, bit 3 defines whether space is prefetchable, and upper bits [31:4] are used as a PCI Express Base Address for access to Local Address.

Each Local Bus bridge Direct Slave space provides a dedicated 32-bit Direct Slave Local Address Range register. For Memory-Mapped accesses, bits [2:1] are always cleared to 00b, bit 3 defines whether space is prefetchable, and upper bits [31:4] are used to define the range of each Direct Slave space.

Each Local Bus bridge Direct Slave space also provides a dedicated 32-bit Direct Slave Local Base Address Remap register that maps all incoming traffic from PCI Express (Memory-Mapped I/O space)-to-Local Bus. Upper bits [31:4] are used to map downstream traffic to the Local Bus. (Refer to Section 9.3, "Direct Slave Operation," for further details.)

Memory transactions that fall within the range defined by the Base and Limit are forwarded downstream (PCI Express-to-Local Bus in Endpoint mode, Local Bus-to-PCI Express in Root Complex mode), and Memory transactions forwarded upstream that are within the range are ignored. Downstream Memory transactions that do not fall within the range defined by the Base and Limit are ignored on the upstream bus, and are forwarded upstream from the downstream interface.

Memory transactions that fall within the range defined by the Base and Limit are forwarded downstream from the primary interface to the secondary interface, and Memory transactions on the secondary interface that are within the range are ignored. Memory transactions that do not fall within the range defined by the Base and Limit are ignored on the primary interface and are forwarded upstream from the secondary interface (provided they are not in the Address range defined by the set of **Prefetchable Memory Address** registers or are not forwarded downstream by the VGA mechanism).

The following **LCS** registers define Direct Master space for Local-to-PCI Express Memory-Mapped I/O accesses:

- **LCS_DMLBAM** Local Base Address for Accesses to PCI Express Dual Address
- **LCS_DMRR** Direct Master Memory Range
- **LCS_DMPBAM** Direct Master Memory Remap Address
- **LCS_DMDAC** Direct Master PCI Express DAC Upper Address (must be cleared to 0, as Memory-Mapped I/O space is 32-bit address only)

The following **LCS** registers define the DMA Channels for Local-to-PCI Express Memory-Mapped I/O accesses:

- **LCS_DMAPADR0/1** Physical 32-bit PCI Express Memory Base address to be used as source or destination for DMA transfers
- **LCS_DMADAC0/1** (must be cleared to 0, because Memory-Mapped I/O space is 32-bit address only)

By default, the Local Bus is a Memory-Mapped bus. For the PEX 8311 to generate Memory-Mapped transactions by way of Direct Master or DMA, the **LCS_CNTRL**[15:0] must be programmed to PCI Express Memory Command Codes before transactions begin.

The Direct Master space (Local-to-PCI Express Memory space), when configured to Memory transactions (**LCS_CNTRL**[15:8]), consists of a 32-bit Local Base Address register, in which the upper 15 bits [31:16] are used for decoding Local Bus accesses. The Direct Master Base Address value must be multiple of the 64-KB Range value.

The Direct Master space provides a 32-bit Direct Master Range register, in which the upper 15 bits [31:16] are used to define a range of the Direct Master space.

The Direct Master space provides a dedicated 32-bit PCI Express Base Address Remap register. The upper 15 bits [31:16] are used to remap decoded Local Bus accesses to PCI Express Memory-Mapped I/O space and then to the PCI Express interface. (Refer to Section 9.2, "Direct Master Operation," for further details.)

The PEX 8311 does not perform Address Translation for DMA transactions, as the transactions directly address physical memory on both the Local and PCI Express interfaces. **LCS_CNTRL**[7:0] are used to configure PEX 8311 DMA transactions, to drive PCI Memory Command codes during DMA transactions. (Refer to Section 9.5, "DMA Operation," for further details.)

8.4.2.3   Memory-Mapped I/O Forwarding Illustrations

Figure 8-3 illustrates Memory-Mapped I/O forwarding in Endpoint mode. Figure 8-4 illustrates Memory-Mapped I/O forwarding in Root Complex mode.

Figure 8-3.   Memory-Mapped I/O Forwarding in Endpoint Mode
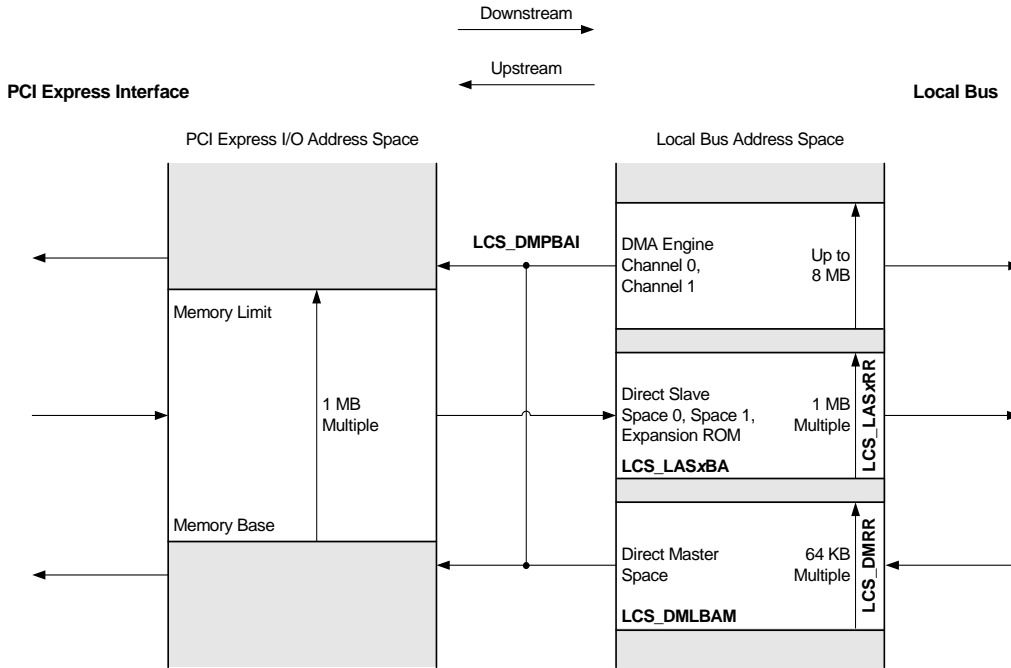
Figure 8-4.   Memory-Mapped I/O Forwarding in Root Complex Mode
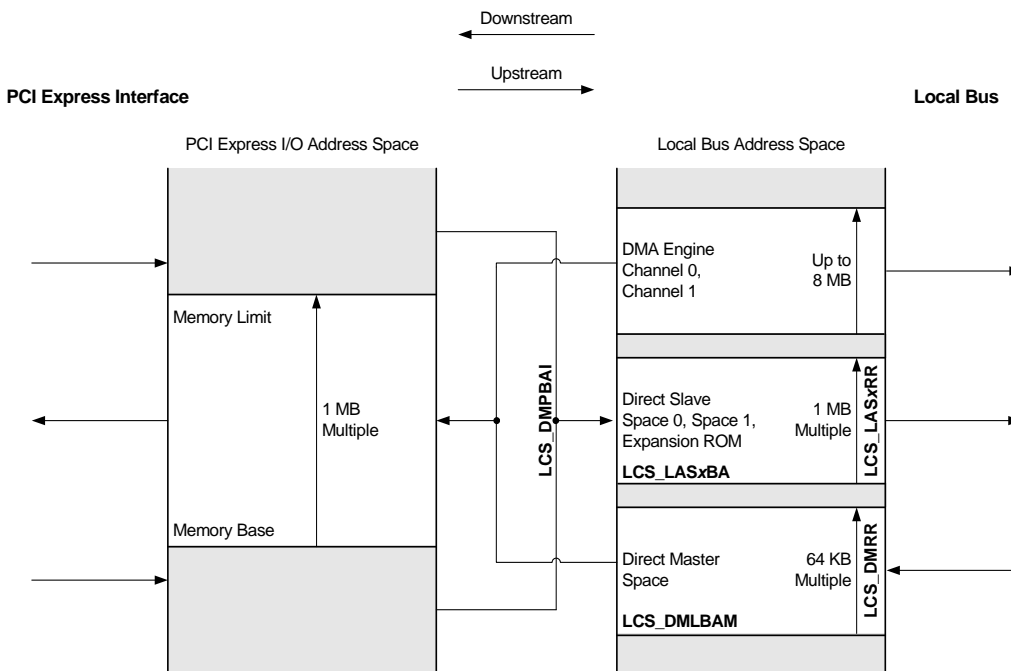
8.5   Prefetchable Space

The Prefetchable Address space determines whether to forward Prefetchable Memory Read or Write transactions from PCI Express to the Local Bus bridge, and vice-versa. Prefetchable Memory transactions can maintain short (32-bit) or long (64-bit) Address formats. Although the PEX 8311 PCI Express bridge is capable of forwarding Long Address Format transactions to the Local Bus bridge, it supports only 32-bit Address transactions. Therefore the PEX 8311 must be mapped into the lower 4-GB Address range and avoid sending Long Address Format transactions. In the opposite direction, however, the PEX 8311 Direct Master channel is capable of generating Long Address Format transactions directed toward the PCI Express bridge.

8.5.1   Enable Bits

The Prefetchable space responds to the Enable bits, as described in Section 8.4.1.

8.5.2   Prefetchable Memory Base and Limit Registers

8.5.2.1   PECS Prefetchable Memory Base and Limit Registers

The following **PECS** registers define the rules for forwarding Prefetchable Memory accesses across the PCI Express bridge:

- **PECS_PREBASE**[15:4] (corresponds to Address bits [31:20])
- **PECS_PREBASEUPPER**[31:0] (corresponds to Address bits [63:32])
- **PECS_PRELIMIT**[15:4] (corresponds to Address bits [31:20])
- **PECS_PRELIMITUPPER**[31:0] (corresponds to Address bits [63:32])

PECS_PREBASE[15:4] register define bits [31:20] of the Prefetchable Memory Base address. **PECS_PRELIMIT**[15:4] register define bits [31:20] of the Prefetchable Memory Limit. Bits [3:0] of each register are hardwired to 0h. For 64-bit addressing, the **PECS_PREBASEUPPER** and **PECS_PRELIMITUPPER** registers are also used to define the space.

Because Address bits [19:0] are not included in the Address space decoding, the Prefetchable Memory Address range retains a granularity of 1 MB, and is always aligned to a 1-MB Address Boundary space. The maximum Prefetchable Memory range is 4 GB with 32-bit addressing, and 2^{61} with 64-bit addressing.

If **PECS_PREBASE** is programmed to a value greater than **PECS_PRELIMIT**, the Prefetchable Memory range is disabled. In this case, Memory transaction forwarding is determined by the **PECS_MEMBASE** and **PECS_MEMLIMIT** registers.

The   **PECS_PREBASE**,   **PECS_PREBASEUPPER**,   **PECS_PRELIMIT**,   and **PECS_PRELIMITUPPER** registers must be considered when disabling the Prefetchable range.

Note: The PREBASE and PRELIMIT values above are 64-bit values formed by concatenating the **PECS_PREBASEUPPER** *and* **PECS_PREBASE**, *and* **PECS_PRELIMITUPPER** *and* **PECS_PRELIMIT**, *registers.*

8.5.2.2   LCS Prefetchable Memory Base and Limit Registers

The **LCS** registers described in this section are used to map resources on the Local Bus bridge relative to Prefetchable Memory-Mapped I/O forwarding on the PCI Express bridge.

The following **LCS** registers are used to map access to the Local Bus by way of Direct Slave Space 0, for Prefetchable Memory-Mapped I/O accesses forwarded from PCI Express Space:

- **LCS_PCIBAR2** PCI Express Base Address for Accesses to Local Address Space 0

- **LCS_LAS0RR** Space 0 Range

- **LCS_LAS0BA** Space 0 Remap Address

The following **LCS** registers are used to map access to the Local Bus by way of Direct Slave Space 1, for Prefetchable Memory-Mapped I/O accesses forwarded from PCI Express Space:

- **LCS_PCIBAR3** PCI Express Base Address for Accesses to Local Address Space 1

- **LCS_LAS1RR** Space 1 Range

- **LCS_LAS1BA** Space 1 Remap Address

The following **LCS** registers are used to map access to the Local Bus by way of Expansion ROM space, for Prefetchable Memory-Mapped I/O accesses forwarded from PCI Express Space:

- **LCS_PCIERBAR** PCI Express Base Address for Local Expansion ROM

- **LCS_EROMRR** Expansion ROM Range

- **LCS_EROMBA**[31:11] Expansion ROM Remap Address

The Local Bus bridge Direct Slave spaces (Space 0, Space 1, and Expansion ROM), when configured for Memory transactions, consist of a 32-bit PCI Express Base Address register for each space (**LCS_PCIBAR2** and **LCS_PCIBAR3**), in which bits [2:1] are always cleared to 00b, bit 3 defines whether space is prefetchable, and upper bits [31:4] are used as a PCI Express Base Address for access to Local Addresses.

Each Local Bus bridge Direct Slave space provides a dedicated 32-bit Direct Slave Local Address Range register. For Memory-Mapped accesses, bits [2:1] are always cleared to 00b, bit 3 defines whether space is prefetchable, and upper bits [31:4] are used to define the range of each Direct Slave space.

Each Local Bus bridge Direct Slave space also provides a dedicated 32-bit Direct Slave Local Base Address Remap register that maps all incoming traffic from PCI Express (Prefetchable Memory-Mapped space)-to-Local Bus. The upper bits [31:4] are used to map downstream traffic to the Local Bus. (Refer to Section 9.3, "Direct Slave Operation," for further details.)

Memory transactions that fall within the range defined by the Base, Range, and Limit are forwarded downstream from the upstream to downstream bus. Memory transactions on the downstream bus that are within the range are ignored.

Memory transactions that do not fall within the range defined by the Base, Range, and Limit are ignored on the upstream bus, and are forwarded upstream from the downstream-to-upstream bus (provided they are not within the address range defined by the Memory-Mapped I/O Address register set or are not forwarded downstream by another mechanism).

The following **LCS** registers define Direct Master space for Local-to-PCI Express Prefetchable Memory-Mapped I/O accesses:

- **LCS_DMLBAM** Local Base Address for Accesses to PCI Express Memory Address
- **LCS_DMRR** Direct Master Memory Range
- **LCS_DMPBAM** Direct Master Memory Remap Address
- **LCS_DMDAC** PCI Express DAC Base Address for Direct Master Accesses (cleared to 0 for SAC and non-zero for DAC accesses)

The following **LCS** registers define the DMA Channels for Local-to-PCI Express Prefetchable Memory-Mapped I/O accesses:

- **LCS_DMAPADR0/1** Physical 32-bit PCI Express Memory Base address to be used as source or destination for DMA transfers
- **LCS_DMADAC0/1** (must be cleared to 0, because Memory-Mapped I/O space is 32-bit address only)

By default, the Local Bus is a Memory-Mapped bus. For the PEX 8311 to generate Memory-Mapped transactions by way of Direct Master or DMA, the **LCS_CNTRL**[15:0] must be programmed to PCI Express Memory Command codes before transactions begin.

The Direct Master space (Local-to-PCI Express Memory space), when configured to Memory transactions (**LCS_CNTRL**[15:8]), consists of a 32-bit Local Base Address register, in which the upper 15 bits [31:16] are used for decoding Local Bus accesses. The Direct Master Base Address value must be multiple of the 64-KB Range value.

The Direct Master space provides a 32-bit Direct Master Range register, in which the upper 15 bits [31:16] are used to define a range of the Direct Master space.

The Direct Master space provides a dedicated 32-bit PCI Express Base Address Remap register. The upper 15 bits [31:16] are used to remap decoded Local Bus accesses to PCI Express Prefetchable Memory-Mapped space and then to the PCI Express interface. (Refer to Section 9.2, "Direct Master Operation," for further details.)

The PEX 8311 does not perform Address Translation for DMA transactions. Source and destination addresses are used to map DMA transactions from the PEX 8311 Configuration registers. **LCS_CNTRL**[7:0] are used to configure PEX 8311 DMA transactions, to drive PCI Express Memory Command codes during DMA transactions. (Refer to Section 9.5, "DMA Operation," for further details.)

8.5.2.3   Memory-Mapped I/O and Prefetchable Memory Forwarding Illustrations

Figure 8-5 illustrates Memory-Mapped I/O and Prefetchable Memory forwarding in Endpoint mode. Figure 8-6 illustrates Memory-Mapped I/O and Prefetchable Memory forwarding in Root Complex mode.

Figure 8-5.   Memory-Mapped I/O and Prefetchable Memory Forwarding in Endpoint Mode

Short Address Format = 32-Bit Address Cycle
Long Address Format = 64-Bit Address Cycle
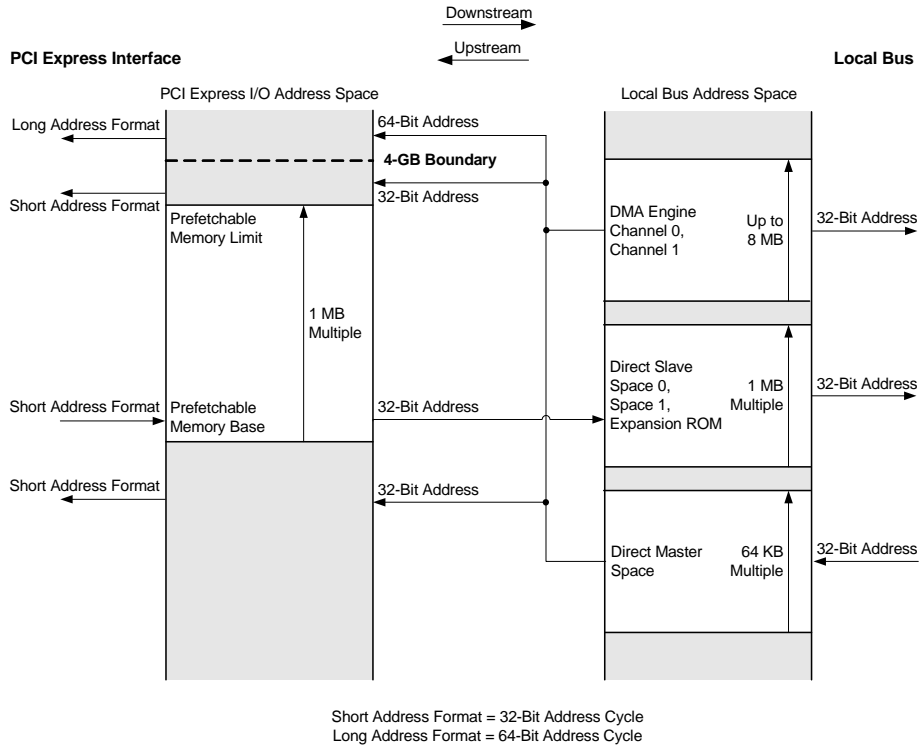
Figure 8-6. Memory-Mapped I/O and Prefetchable Memory Forwarding in Root Complex Mode

Short Address Format = 32-Bit Address Cycle
Long Address Format = 64-Bit Address Cycle
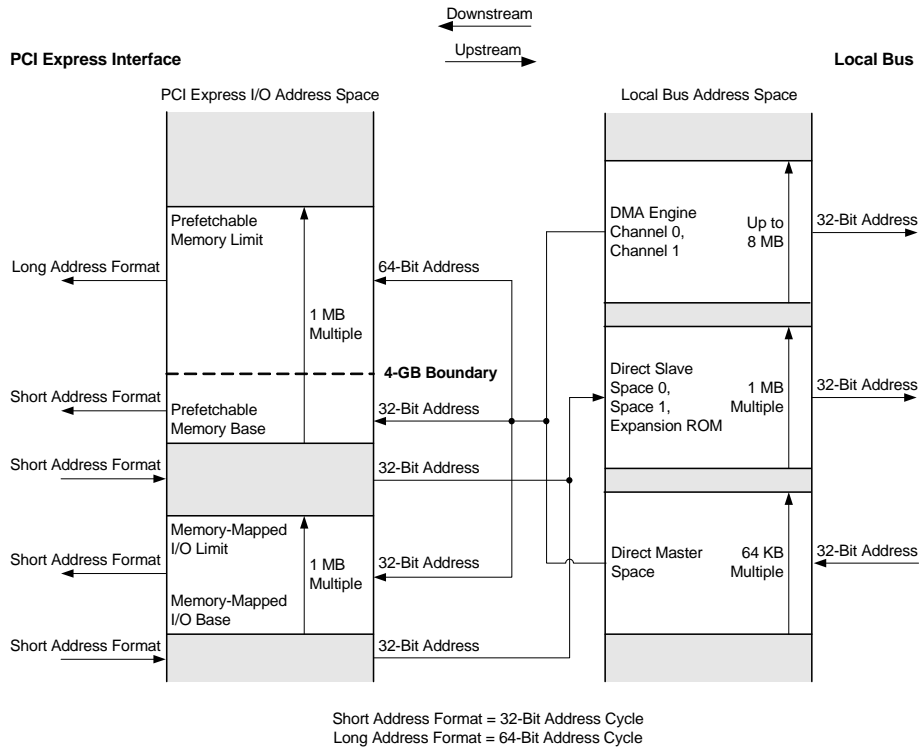
8.5.3   64-Bit Addressing

The PEX 8311 supports generation of 64-bit Long Address format for Direct Master and DMA transactions, as illustrated in Figure 8-5 and Figure 8-6. This allows the PEX 8311 and Local Processors to access devices in PCI Express Space that reside above the 4-GB Address Boundary space.

64-bit addressing is ***not supported*** for Direct Slave accesses to Local Bus Space. For this reason, the PEX 8311 must always be mapped to Memory or I/O addresses below the 4-GB Address Boundary space. Additional limitations for Endpoint and Root Complex modes are described in Section 8.5.3.1 and Section 8.5.3.2.

8.5.3.1   Endpoint Mode 64-Bit Addressing

The PEX 8311 supports generation of PCI Express TLP with Long Address format to upstream devices. The **PECS_PREBASEUPPER** and **PECS_PRELIMITUPPER** registers must be cleared to 0h, and the **LCS_DMDAC** and **LCS_DMADAC0/1** registers must be set to a non-zero value. A value of 0h in the **LCS_DMDAC** and **LCS_DMADAC0/1** registers prevents the PEX 8311 from responding to Local Bus transactions, by internally generating a Dual Address Cycle to Prefetchable Memory. Internal accesses are Single Address Cycle. The internal Dual Address Cycle accesses (TLP with Long Address format) is used to address devices located above the 4-GB Address Boundary space.

When the PEX 8311 detects a downstream access, PCI Express Memory transaction with an address above the 4-GB Address Boundary space, the transaction is completed with Unsupported Request status. The PEX 8311 generates upstream traffic – TLP with Long Address format – in response to Local Bus accesses to address devices located above the 4-GB Address Boundary space only when Direct Master and/or DMA accesses internally fall within the range of Prefetchable memory.

Upstream traffic from the Local Bus, Direct Master, and/or DMA that internally falls outside both the Prefetchable Memory space and Memory-Mapped I/O space must be Single Address Cycle, **LCS_DMDAC** and **LCS_DMADAC0/1** cleared to 0h for the PEX 8311 to address devices located below the 4-GB Address Boundary space, TLP with Short Address format.

8.5.3.2   Root Complex Mode 64-Bit Addressing

If the **PECS_PREBASEUPPER** and **PECS_PRELIMITUPPER** registers are both cleared to 0h, the PEX 8311 generation of addresses above the 4-GB Address Boundary space, TLP with Long Address format, are ***not supported***.

Local Bus-initiated transactions by way of Direct Master and DMA Dual Address Cycle accesses are internally ignored by the Prefetchable Memory space. Local Bus System errors (LSERR#) are generated, when enabled.

If the PEX 8311 PCI Express Prefetchable Memory space is located entirely above the 4-GB Address Boundary space, the **PECS_PREBASEUPPER** and **PECS_PRELIMITUPPER** registers are both set to non-zero values. The PEX 8311 ignores Single Address Cycle Memory transactions internally generated by Direct Master or DMA, and forwards PCI Express Memory transactions with addresses below the 4-GB Address Boundary space upstream to the Local Bus Spaces (Direct Slave) (unless they fall within the Memory-Mapped I/O range).

Local Bus accesses by way of Direct Master and/or DMA Dual Address Cycle transaction that internally fall within the range defined by the **PECS_PREBASE**, **PECS_PREBASEUPPER**, **PECS_PRELIMIT**, and **PECS_PRELIMITUPPER** registers are forwarded downstream to the PCI Express interface.

Dual Address Cycle transactions that internally do not fall within the range defined by these registers are ignored.

If the PEX 8311 detects an upstream access, PCI Express memory transaction above the 4-GB Address Boundary space that falls within the range defined by these registers, it is completed with Unsupported Request status.

If the PEX 8311 PCI Express Prefetchable Memory space spans the 4-GB Address Boundary space, the **PECS_PREBASEUPPER** register is cleared to 0h, and the **PECS_PRELIMITUPPER** register is set to a non-zero value.

If the Local Bus accesses, Direct Master and/or DMA Single Address Cycle that are greater than or equal to the Prefetchable Memory Base address, the transaction is forwarded downstream to the PCI Express interface.

If an upstream, PCI Express Memory transaction is detected with an address below the 4-GB Address Boundary space, and is less than the Prefetchable Memory Base address, the transaction is forwarded upstream to the Local Bus Spaces (Direct Slave). If the Local Bus accesses, Direct Master and/or DMA Dual Address Cycle are mapped to be less than or equal to the **PECS_PRELIMIT** register, the transaction is forwarded downstream to the PCI Express interface.

When the PEX 8311 detects an upstream access, the PCI Express memory transaction above the 4-GB Address Boundary space is less than or equal to the **PECS_PRELIMIT** register, it is completed with Unsupported Request status.

Local Bus-initiated transactions by way of Direct Master and DMA Dual Address Cycle accesses that are greater than the **PECS_PRELIMIT** register are ignored by the Prefetchable Memory space. Local Bus System errors (LSERR#) are generated, when enabled.

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Chapter 9   Direct Data Transfer Modes

9.1   Introduction

The PEX 8311 Local Bus supports three Direct Data Transfer modes:

- **Direct Master**
    - **C and J modes** – Local CPU accesses PCI Express memory or I/O
    - **M mode** – Local CPU accesses PCI memory or I/O, including support for MPC850 and MPC860 Independent (IDMA) and Serial (SDMA) Operation
- **Direct Slave** – PCI Express Initiator accesses Local memory or I/O
- **DMA** – PEX 8311 DMA Controller generates Read/Write requests to PCI Express memory to/from Local memory

9.1.1   Dummy Cycles

9.1.1.1   Dummy Cycles – C and J Modes

Direct Slave Write Data Transfer mode does not generate dummy cycles. However, in special cases, it passes dummy cycles from the PCI Express interface to the Local Bus. The Local Bus LBE[3:0]# can be encoded to provide LA[1:0] balls must be monitored for dummy cycles to be recognized on the Local Bus because no other Data Transfer modes generate dummy cycles. The PEX 8311 suppresses dummy cycles, to avoid generating them on the PCI Express interface and Local Bus.

9.1.1.2   Dummy Cycles – M Mode

None of the Data Transfer modes generate dummy cycles. The PEX 8311 suppresses all dummy cycles on the PCI Express interface and Local Bus.

9.2   Direct Master Operation

The PEX 8311 supports a direct access to the PCI Express interface, the Local processor, or an intelligent controller by mapping Direct Master Memory and/or I/O space to any PCI Express Space described in Chapter 8, "PCI Express Bridge Transaction Forwarding." Master mode must be enabled in the **LCS PCI Command** register (**LCS_PCICR**[2]=1) for the Local Bus and PCI Express interface. The following registers define Local-to-PCI Express accesses (refer to Figure 9-1):

- Direct Master Memory and I/O Range (**LCS_DMRR**)
- Local Base Address for Direct Master to PCI Express Memory (**LCS_DMLBAM**)
- Local Base Address for Direct Master to PCI Express I/O and Configuration (**LCS_DMLBAI**)
- PCI Express Base Address (**LCS_DMPBAM**)
- Direct Master Configuration (**LCS_DMCFGA**)
- Direct Master PCI Express Dual Address Cycles (**LCS_DMDAC**)
- Master Enable (**LCS_PCICR**)
- PCI Command Code (**LCS_CNTRL**)

Figure 9-1.   Direct Master Access of PCI Express Interface
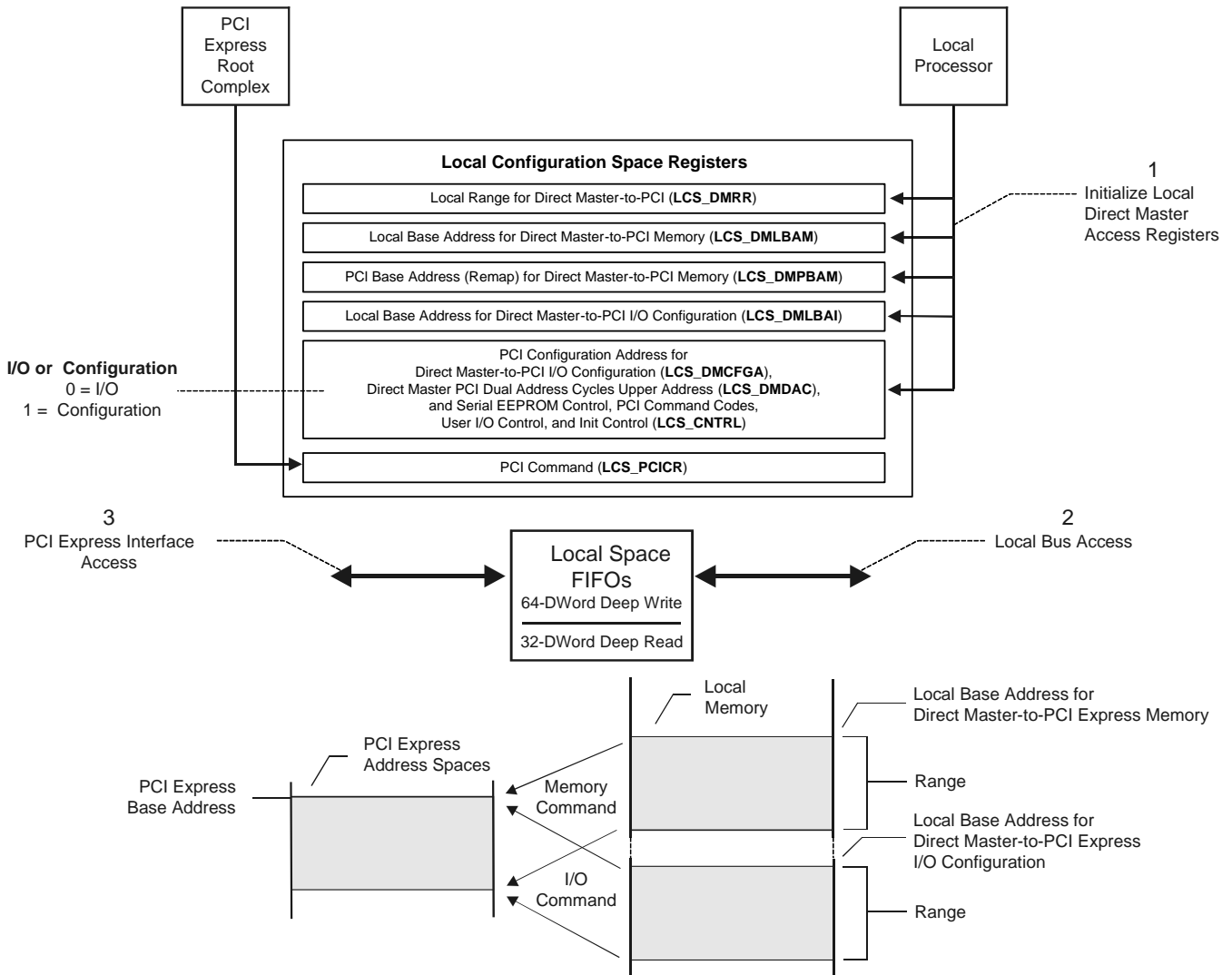
9.2.1 Direct Master Memory and I/O Decode

The Range register, LCS_DMRR, and the Local Base Address, LCS_DMLBAM/LCS_DMLBAI, specify the Local Address bits to use for decoding a Local-to-PCI Express Space access (Direct Master). The Memory or I/O Space range must be a power of 2 and the LCS_DMRR register value must be two's complement of the range value. In addition, the Local Base Address must be a multiple of the range value.

Any Local Master Address starting from the Direct Master Local Base Address (Memory or I/O) to the range value is recognized as a Direct Master access by the PEX 8311. Direct Master cycles are then decoded as Memory, I/O, or Type 0 or Type 1 Configuration to one of the three PCI Express Spaces in the PEX 8311. Moreover, a Direct Master Memory or I/O cycle is remapped according to the Remap register value, which must be a multiple of the Direct Master range value (not the LCS_DMRR register value).

The PEX 8311 can accept Memory cycles only from the Local processor. The Local Base address and range determine whether Memory or I/O transactions occur to one of the PCI Express Space within the PEX 8311.

9.2.2 Direct Master FIFOs

For Direct Master Memory access to one of the three PCI Express Spaces and then to the PCI Express interface, the PEX 8311 has a 64-Dword (256-byte) Write FIFO and a 32-Dword (128-byte) Read FIFO. Each FIFO is designed such that one FIFO location can store 2 Dwords of data. The FIFOs enable the Local Bus to operate independently with the PEX 8311 PCI Express Spaces and allows high-performance bursting between Direct Master space and PCI Express Space (internally within the PEX 8311), as well as the Local Bus. In a Direct Master Write, the Local processor (Master) Writes data to the PCI Express interface. In a Direct Master Read, the Local processor (Master) Reads data from the PCI Express interface by issuing a TLP Read request and accepting a Completion. Figure 9-2 through Figure 9-5 illustrate the FIFOs that function during a Direct Master Write and Read, respectively.

Figure 9-2.   Direct Master Write – M Mode
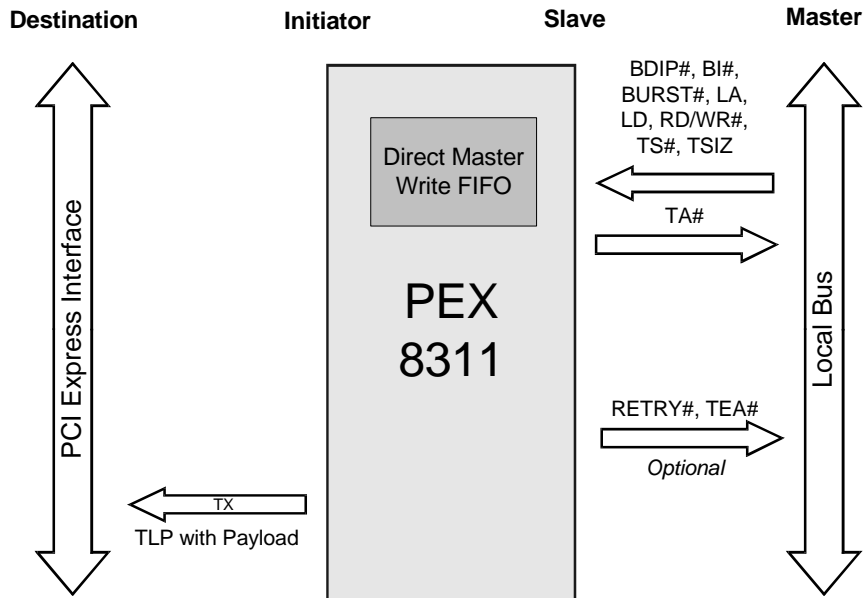
Figure 9-3.   Direct Master Read – M Mode
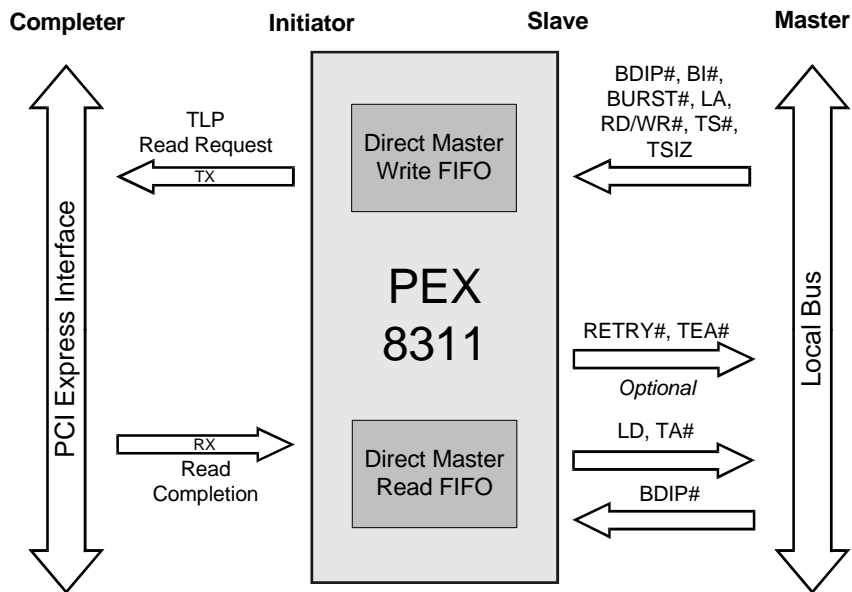
Note: Figure 9-2 and Figure 9-3 represent a sequence of Bus cycles.

Figure 9-4. Direct Master Write – C and J Modes
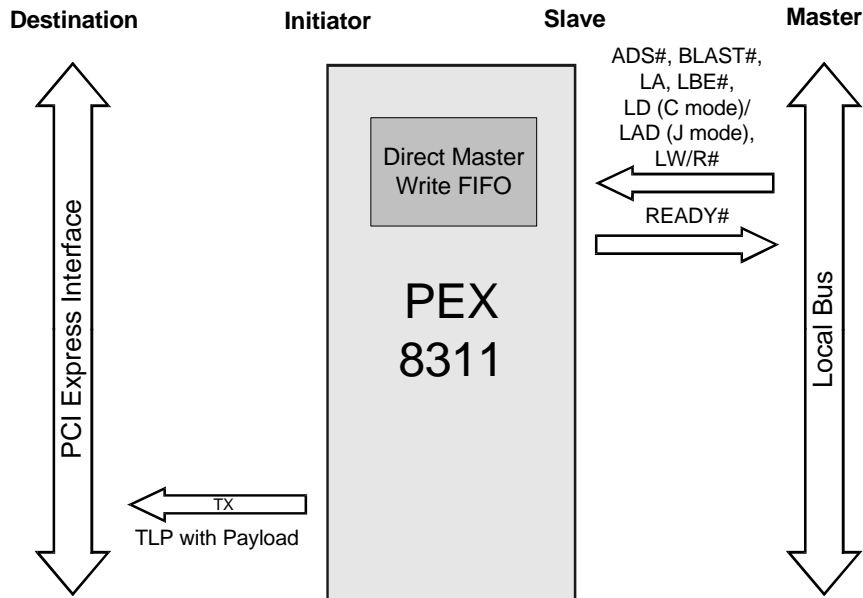
Figure 9-5. Direct Master Read – C and J Modes
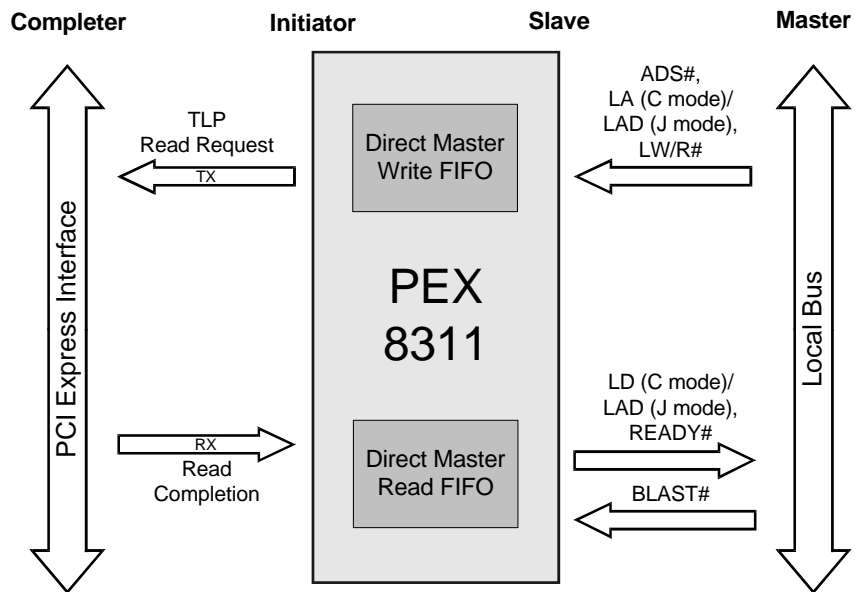
Note: Figure 9-4 and Figure 9-5 represent a sequence of Bus cycles.

9.2.3   Direct Master Memory Access

9.2.3.1   Direct Master Memory Access – C and J Modes

The Local processor transfers data through a single or Burst Read/Write Memory transaction to one of the PCI Express Spaces within the PEX 8311 and then to the PCI Express interface.

The PEX 8311 converts the parallel Local Read/Write access to serial TLP Read/Write request on to PCI Express interface accesses. The Local Address space starts from the Direct Master Local Base Address up to the range. Remap (PCI Express Base Address) defines the PCI starting address and PCI Express address.

A Local Bus Processor single cycle causes an internal single cycle transaction to one of the mapped PCI Express Spaces. The PCI Express performs a PCI Express TLP request with single data payload. A Local processor Burst cycle causes an internal Burst transaction between Direct Master space and PCI Express Space within the PEX 8311. The PEX 8311 performs a Maximum Payload Read/Write request transaction on the PCI Express interface. The PEX 8311 supports Continuous Burst transfers.

The Local Bus Processor (a Local Bus Master) initiates transactions when the Memory address on the Local Bus matches the Memory space decoded for Direct Master operations.

9.2.3.1.1   Direct Master Command Codes to PCI Express Address Spaces –
C and J Modes

The PEX 8311 becomes an internal PCI Bus Master, to perform Direct Master transfers. The internal PCI Command Code used by the PEX 8311 during a Direct Master transfer is specified by the value(s) contained in the **LCS_CNTRL**[15:0] bits, except when Memory Write and Invalidate (MWI) mode is selected in the **LCS** registers (**LCS_PCICR**[4]=1; **LCS_DMPBAM**[9]=1; **LCS_PCICLSR**[7:0] = Cache Line Size of 8 or 16 Dwords). In MWI mode for Direct Master transfers, when the starting address alignment is aligned with the Cache Line Size and upon determining it can transfer at least one Cache Line of data, the PEX 8311 uses an internal PCI Command Code of Fh, regardless of the **LCS_CNTRL**[15:0] register bit values.

For direct Local-to-PCI Express accesses, the PEX 8311 uses the internal PCI Commands Codes defined in Table 9-1 through Table 9-3.

Table 9-1.   Internal PCI Command Codes for Direct Master or DMA Accesses to PCI Express Memory Spaces Memory-Mapped I/O or Prefetchable Address Spaces Access

Command Type	Code (C/BE[3:0]#)
Memory Read	0110b (6h)
Memory Write	0111b (7h)
Memory Read Multiple	1100b (Ch)
Dual Address Cycle	1101b (Dh)
Memory Read Line	1110b (Eh)
Memory Write and Invalidate	1111b (Fh)

Table 9-2.   Internal PCI Command Codes for Local-to-PCI Express I/O Address Space Access

Command Type	Code (C/BE[3:0]#)
I/O Read	0010b (2h)
I/O Write	0011b (3h)

Table 9-3.   Internal PCI Command Codes for Local-to-PCI Express I/O-Mapped Configuration Access

Command Type	Code (C/BE[3:0]#)
Configuration Memory Read	1010b (Ah)
Configuration Memory Write	1011b (Bh)

9.2.3.1.2   Direct Master Writes – C and J Modes

For a Local Bus Write, the Local Bus Master writes data to the Direct Master Write FIFO. When the first data is in the FIFO, the Local Bus bridge begins issuing Writes to the PCI Express bridge. If the transactions satisfy the Forwarding rules, the PCI Express bridge accepts the data and forms them into PCI Express Write request Transaction Layer Packets (TLPs). The PEX 8311 then generates a PCI Express TLP Write request and transfers the data on the PCI Express Link to its destination. The PEX 8311 continues to accept Writes and returns READY# until the Direct Master Write FIFO is full. The PEX 8311 then holds READY# de-asserted until space becomes available in the Direct Master Write FIFO. A programmable Direct Master "almost full" status output is provided (DMPAF signal). (Refer to **LCS_DMPBAM**[10, 8:5].)

Local Bus processor single cycle Write transactions result in PEX 8311 transfers of 1 Dword of payload to the PCI Express interface.

A Local processor, with no burst limitations and a Burst cycle Write transaction of 2 Dwords, causes the PEX 8311 to perform two single Writes into the PCI Express Space when the Local Bus starting address is X0h or X8h. The same type of transfer with a Local Bus starting address of X4h or XCh results in a 2-Dword burst to the PCI Express Space within the PEX 8311. Three (or more) Dwords at any Dword address, with Burst cycles of any type, result in the PEX 8311 bursting data onto the PCI Express Space within the PEX 8311. The PEX 8311 generates a PCI Express TLP Write request for each Direct Master Write entered the PCI Express Space to the PCI Express interface.

9.2.3.1.3 Direct Master Reads – C and J Modes

For a Local Bus Read, the PEX 8311 arbitrates for the PCI Express Space, and writes a read address directly into it. The PEX 8311 generates a PCI Express TLP Read request and as Read Completion returns the PEX 8311 accepts it and directly writes the data into the Direct Master Read FIFO, through one of the PCI Express Spaces. The PEX 8311 asserts Local Bus READY# to indicate that the requested data is on the Local Bus.

The PEX 8311 holds READY# de-asserted while Read data is not available from its source, PCI Express device or PEX 8311's PCI Express Space. Programmable prefetch modes available for Direct Master have an efficient Data transfer from the PCI Express Space into the Direct Master Read FIFO, when prefetch is enabled – Prefetch, 4, 8, 16, or Continuous Data – until the Direct Master cycle ends. The Read cycle is terminated when Local BLAST# input is asserted. Unused Read data is flushed from the FIFO.

The PEX 8311 prefetch mechanism has no effect for single cycle (Local BLAST# input is asserted during the clock following ADS#) Direct Master reads unless Read Ahead mode is enabled and the prefetch length is set to Continuous (**LCS_DMPBAM**[2, 11]=10b, respectively). (Refer to Section 9.2.7 for details regarding Read Ahead mode.) For single cycle Direct Master Reads (Read Ahead mode is disabled, **LCS_DMPBAM**[2]=0), the PEX 8311 requests 1 Dword Read request on the PCI Express interface.

For single cycle Direct Master Reads, the PEX 8311 passes the Local Byte Enables (LBE[3:0]#) to the PCI Express Space within the PEX 8311 to read only the bytes requested by the Local Master device. The PEX 8311 generates a PCI Express TLP Read request, with the byte field indicating the bytes required by the Local Master device.

For Burst Cycle Reads, the PEX 8311 reads entire Dwords (all Byte Enables are asserted) within the PEX 8311, regardless of whether the Local Byte Enables are contiguous. The PEX 8311 generates a PCI Express TLP Read request with byte field of 1, indicating the Read request is contiguous, except for the first and the last data when Local Bus read is unaligned.

When the Direct Master Prefetch Limit bit is enabled (**LCS_DMPBAM**[11]=1), the PEX 8311 terminates a Read prefetch at 4-KB boundaries internally between Direct Master and PCI Express Space, and restarts it as a new Read Prefetch cycle at the start of a new boundary. If the bit is disabled (**LCS_DMPBAM**[11]=0), the Direct Master Read prefetch crosses the PCI Express Space 4-KB boundaries. PCI Express does not allow the cross of 4-KB Address Boundary space; therefore, the PEX 8311 generates at least two individual PCI Express TLP Read requests for data before a 4-KB and after a 4-KB Address Boundary space.

When the 4-KB Prefetch Limit bit is enabled, and the PEX 8311 started a Direct Master read to the PCI Express interface Address FF8h (2 Dwords before the 4-KB Address Boundary space), the PEX 8311 does *not* internally perform a Burst prefetch of 2 Dwords. The PEX 8311 instead performs an internal prefetch of two single cycle Dwords between Direct Master and PCI Express Space, to prevent crossing the PCI Express Space 4-KB Address Boundary space limit. The cycle then continues by starting at the new boundary.

9.2.3.2   Direct Master Memory Access – M Mode

The MPC850 or MPC860 transfers data through a single or Burst Read/Write Memory transaction, or through SDMA channels to the PEX 8311 and PCI Bus. The MPC850 or MPC860 IDMA/SDMA accesses to the PEX 8311 appear as Direct Master operations. (Refer to Section 9.2.13 for further details about IDMA/SDMA accesses.)

The PEX 8311 converts the Local Read/Write access to PCI Bus accesses. The Local Address space starts from the Direct Master Local Base Address up to the range. Remap (PCI Base Address) defines the PCI starting address.

An MPC850 or MPC860 single cycle causes a single cycle PCI transaction. An MPC850 or MPC860 Burst cycle causes a PCI burst transaction. Local bursts are limited to 16 bytes (4 Dwords) in the MPC850 or MPC860 Bus protocol.

The PEX 8311 supports bursts beyond the 16-byte boundary (PLX Continuous Burst mode) when BDIP# input remains asserted beyond a 16-byte boundary by an external Local Bus Master. To finish the Continuous Burst, the external Master should de-assert BDIP# in the last Data phase.

Transactions are initiated by the MPC850 or MPC860 (a Local Bus Master) when the Memory address on the Local Bus matches the Memory space decoded for Direct Master operations.

9.2.3.2.1   Direct Master Writes – M Mode

For a Local Bus Write, the Local Bus Master writes data to the Direct Master Write FIFO. When the first data is in the FIFO, the PEX 8311 becomes the PCI Bus Master, arbitrates for the PCI Bus, and writes data to the PCI Slave device. The PEX 8311 continues to accept Writes and returns TA# until the Direct Master Write FIFO is full. The PEX 8311 then holds TA# de-asserted until space becomes available in the Direct Master Write FIFO. A programmable Direct Master "almost full" status output is provided (DMPAF signal). (Refer to **LCS_DMPBAM**[10, 8:5].) The PEX 8311 asserts RETRY# when the Direct Master Write FIFO is full, implying that the Local Master can relinquish Local Bus ownership and finish the Write operation at a later time (**LCS_LMISC1**[6]).

MPC850 or MPC860 single cycle Write transactions result in PEX 8311 transfers of 1 Dword of data to the PCI Bus.

MPC850 or MPC860 Burst cycle Write transactions of 4 Dwords result in PEX 8311 Burst transfers of 4 Dwords to the PCI Bus.

A Local processor (MPC850 or MPC860), with no burst limitations and a Burst cycle Write transaction of 2 Dwords, causes the PEX 8311 to perform two single Writes to the PCI Bus if the Local Bus starting address is X0h or X8h. The same type of transfer with a Local Bus starting address of X4h or XCh results in a 2-Dword burst to the PCI Bus without dummy cycles. Three (or more) Dwords at any Dword address, with Burst cycles of any type, result in the PEX 8311 bursting data onto the PCI Bus without dummy cycles.

9.2.3.2.2   Direct Master Reads – M Mode

For a Local Bus read, the PEX 8311 becomes a PCI Bus Master, arbitrates for the PCI Bus, and reads data from the PCI Slave device directly into the Direct Master Read FIFO. The PEX 8311 asserts Local Bus TA# to indicate that the requested data is on the Local Bus.

The PEX 8311 holds TA# de-asserted while receiving data from the PCI Bus. Programmable Prefetch modes are available if prefetch is enabled – prefetch, 4, 8, 16, or continuous data – until the Direct Master cycle ends. The Read cycle is terminated when the Local BDIP# input is de-asserted. Unused Read data is flushed from the FIFO.

The PEX 8311 does not prefetch PCI data for single cycle (Local BURST# input is not asserted during the first Data phase) Direct Master reads unless Read Ahead mode is enabled and prefetch length is set to continuous (**LCS_DMPBAM**[2, 11]=10b, respectively). (Refer to Section 9.2.7 for details regarding Read Ahead mode.) For single cycle Direct Master reads of the PCI Bus (Read Ahead mode disabled, **LCS_DMPBAM**[2]=0), the PEX 8311 reads 1 Dword from the PCI Bus.

For single cycle Direct Master reads, the PEX 8311 derives the PCI Byte Enables from the Local Bus address and TSIZ[0:1] signals.

For Burst Cycle reads, the PEX 8311 reads entire Dwords (all PCI Byte Enables are asserted) of the PCI Bus.

If the Direct Master Prefetch Limit bit is enabled (**LCS_DMPBAM**[11]=1), the PEX 8311 terminates a Read prefetch at 4-KB boundaries and restarts it as a new PCI Read Prefetch cycle at the start of a new boundary. If the bit is disabled (**LCS_DMPBAM**[11]=0), the prefetch crosses the 4-KB boundaries.

If the 4-KB Prefetch Limit bit is enabled and the PEX 8311 has started a Direct Master read to the PCI Bus, PCI Address FF8h (2 Dwords before the 4-KB boundary), the PEX 8311 does *not* perform a Burst prefetch of 2 Dwords. The PEX 8311 instead performs a prefetch of two single cycle Dwords to prevent crossing the PCI 4-KB boundary limit. The cycle then continues by starting at the new boundary.

9.2.4   Direct Master I/O

Direct Master I/O space provides the capability for the Local Bus Master (Intelligent device) to generate Type 0 Configuration accesses to access the **PECS** registers and to generate Type 1 Configuration accesses to the PCI Express downstream devices. Type 0 and Type 1 Configuration accesses can only be generated by upstream devices (*that is*, this feature is used only when the PEX 8311 is in Root Complex mode).

Direct Master I/O space can also be used to generate I/O-Mapped transactions to the PEX 8311's Address space, which then is used to generate I/O transactions on the PCI Express interface. Refer to Section 10.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," for detailed descriptions of Type 0 and Type 1 Configuration access generation.

When the *Configuration Enable* bit is cleared (**LCS_DMCFGA**[31]=0), a single I/O access is made to the internal PCI Express Space within the PEX 8311. The *Local Address, Remapped Decode Address* bits, and Local Byte Enables are encoded to provide the address and are output with an I/O Read or Write command during a PCI Express Address cycle. When the *Configuration Enable* bit is set (**LCS_DMCFGA**[31]=1), the cycle becomes a Type 0 or Type 1 PCI Configuration cycle. (Refer to Section 10.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," and the **LCS_DMCFGA** register for details.)

When the *I/O Remap Select* bit is set (**LCS_DMPBAM**[13]=1), Address bits [31:16] (when internally accessing PCI Express Space from within the PEX 8311) are forced to 0 for the 64-KB I/O Address limit. When the *I/O Remap Select* bit is cleared (**LCS_DMPBAM**[13]=0), **LCS_DMPBAM**[31:16] are used as the remap addresses for the PCI Express Space accesses.

9.2.4.1   Direct Master I/O – C and J Modes

For Writes, data is loaded into the Direct Master Write FIFO and READY# is returned to the Local Bus. For Reads, the PEX 8311 holds READY# de-asserted while receiving a Dword from the PCI Express interface.

Local Burst accesses are internally broken into single I/O (Address/Data) cycles when accessing PCI Express Space. The PEX 8311 does not prefetch Read data for I/O nor Configuration Reads.

For Direct Master I/O and Configuration cycles, the PEX 8311 internally passes Local Byte Enables to the PCI Express Space, which are then used to generate PCI Express TLP requests with the exact byte fields required by the Local Bus Master

9.2.4.2   Direct Master I/O – M Mode

For Writes, data is loaded into the Direct Master Write FIFO and TA# is returned to the Local Bus. For Reads, the PEX 8311 holds TA# de-asserted while receiving a Dword from the PCI Express interface.

Local Burst accesses are internally broken into single I/O (Address/Data) cycles when accessing PCI Express Space. The PEX 8311 does not prefetch Read data for I/O nor Configuration Reads.

For Direct Master I/O and Configuration cycles, the PEX 8311 derives the PCI Byte Enables from the Local Bus address and TSIZ[0:1] signals.

9.2.5   Direct Master Delayed Write Mode

The PEX 8311 supports Direct Master Delayed Write mode transactions, in which Posted Write data accumulates in the Direct Master Write FIFO before the PEX 8311 internally requests arbitration to the PCI Express Space. Direct Master Delayed Write mode is programmable to delay internal arbitration for the number of internal clocks selected in **LCS_DMPBAM**[15:14]. This feature is useful for gaining higher throughput during Direct Master Write Burst transactions for conditions in which the Local clock frequency is slower than the internal clock frequency, as well as for the PEX 8311 PCI Express interface to collect sufficient data to generate a PCI Express TLP Write request with Maximum Payload Size.

The PEX 8311 only uses the Delay Counter and accumulates data in the Direct Master Write FIFO for Burst transactions on the Local Bus. A single cycle Write on the Local Bus immediately starts internal arbitration to the PCI Express Space (ignores delay setting).

9.2.6   Direct Master Delayed Read Mode – M Mode Only

The PEX 8311 supports Direct Master Delayed Read transactions. When the *Direct Master Delayed Read Enable* bit is set (**LCS_LMISC1**[4]=1), the PEX 8311 asserts RETRY# and prefetches Read data each time the Local Master requests a read. During a PCI data prefetch, the Local Master is capable of performing other transactions and free to return for requested data at a later time. In this mode, it is required that a Local processor repeat the Retried transaction exactly as the original request, including TSIZ[0:1] assertion, and read at least one data. Otherwise, the PEX 8311 indefinitely Retries the Local Bus Master. When Direct Master Delayed Read mode is disabled (**LCS_LMISC1**[4]=0), the Local Master must retain the Local Bus and wait for the requested data (TA# remains de-asserted until data is available to the Local Bus).

9.2.7   Direct Master Read Ahead Mode

The PEX 8311 only supports Direct Master Read Ahead mode (**LCS_DMPBAM**[2]=1) when the
Direct Master   Read   Prefetch   Size   Control   bits   are   set   to   continuous   prefetch
(**LCS_DMPBAM**[12, 3]=00b). Other *Direct Master Read Prefetch Size Control* bit settings turn off
Direct Master Read Ahead mode. Direct Master Read Ahead mode allows prefetched data to be
buffered in the internal PEX 8311 internal FIFO in anticipation of local master requesting the data. The
address must be contiguous to the previous address and Dword-aligned (next address = current address
+ 4). Direct Master Read Ahead mode functions are used with or without Direct Master Delayed Read
mode.

A Local Bus single cycle Direct Master transaction, with Direct Master Read Ahead mode enabled,
results in the PEX 8311 processing continuous PCI Express TLP Read request generation to remain
ahead of what the Local Bus Master is reading, when the *Direct Master Read Prefetch Size Control* bits
are set to continuous prefetch. (Refer to Figure 9-6.)

The Direct Master Read Ahead stops on the internal PCI Bus after one of the following occurs:

•   Local Bus completes reading data

•   Prefetch count has been reached

Caution: ***To prevent constant locking of the internal PCI Bus between Direct Master and
PCI Express Spaces, do not simultaneously enable Direct Master Read Ahead
and Direct Master PCI Read modes (LCS_DMPBAM[2, 4]≠11b, respectively).***

Figure 9-6.   Direct Master Read Ahead Mode
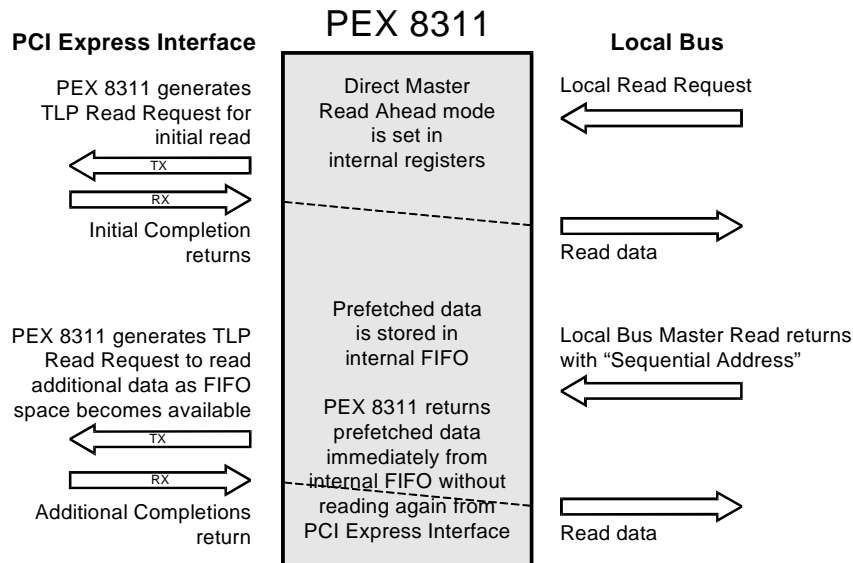
Note: Figure 9-6 represents a sequence of Bus cycles.

Table 9-4.   Example of PCI Express Behavior with Direct Master Read Ahead Mode Enabled

Direct Master Local Bus Cycle to PEX 8311	Direct Master PCI Express Interface Behavior with Direct Master Read Prefetch Size Control Bits Not Set to Continuous Prefetch (LCS_DMPBAM[12, 3]≠00b)	Direct Master PCI Express Interface Behavior with Direct Master Read Prefetch Size Control Bits Set to Continuous Prefetch (LCS_DMPBAM[12, 3]=00b)
Single cycle read followed by single cycle read	Two individual PCI Express TLP Dword Read request generation	Single PCI Express TLP Read request generation with Maximum Read payload
Single cycle read followed by consecutive address Burst Read cycle	Single PCI Express TLP Dword Read request generation followed by another PCI Express TLP Read request generation with Maximum Read payload	Single PCI Express TLP Read request generation with Maximum Read payload followed by another Single PCI Express TLP Read request generation for additional data with Read Ahead
Burst cycle read of four Data cycles, followed by consecutive address Burst cycle read of four Data cycles	Two individual PCI Express TLP Read requests are generated for each Local Bus Read cycle	Single PCI Express TLP Read request generation with Maximum Read payload followed by another PCI Express Read request with Maximum Read payload when additional data is required
Burst cycle read of four Data cycles, followed by consecutive address single cycle read	Single PCI Express TLP Read request generation with Maximum payload followed by another PCI Express TLP Dword Read request generation	Single PCI Express TLP Read request generation with Maximum Read payload followed by another PCI Express Read request with Maximum Read payload when additional data is required

9.2.8   Direct Master PCI Express Long Address Format

The PEX 8311 supports Long Address Format generation, for 64-bit addressing to access devices located above the 4-GB Address Boundary space by utilizing Direct Master Dual Address Cycle (DAC) register (**LCS_DMDAC**) for Direct Master transactions. The Direct Master space must be mapped to PCI Express Prefetchable space and the **LCS_DMDAC** register must be programmed to a non-zero value for 64-bit addressing to occur on the PCI Express interface. (Refer to Section 8.5.3, "64-Bit Addressing," for further details.) When the **LCS_DMDAC** register has a value of 0h, the PEX 8311 performs a Short Address Format on the PCI Express interface.

9.2.9   Internal PCI Bus Master/Target Abort

This section describes how the PEX 8311 handles Direct Master accesses that result in Master/Target Abort conditions on the internal PCI Bus that connects the PCI Express and Local Bus bridges.

For Direct Master accesses forwarded on the internal PCI Bus to the PCI Express bridge, the *Received Master/Target Abort* flag is set (**LCS_PCISR**[13 and/or 12]=1) if the PCI Express bridge:

- Does not claim the access (assert internal DEVSEL#) within six CLKOUT cycles (Master Abort)
- Returns a Target Abort
- Returns Retry more than 256 consecutive times (Retry Timeout)

Accesses originating on the Local Bus and forwarded to the PCI Express bridge for decoding are returned as a Master/Target Abort (**LCS_PCISR**[13 and/or 12]=1) in the following cases:

- PCI Express bridge does not claim the access (assert DEVSEL#) within six clocks on the internal PCI Bus (Master Abort)
- PCI Express bridge responds with Target Abort on the internal PCI Bus
- PCI Express bridge responds with Retry for more than 256 consecutive times (Retry timeout)

As a result, the PEX 8311 Local Bus logic sets the **LCS_PCISR** register *Received Master Abort* bit. The Local Bus Master must clear the *Received Master Abort* bit (**LCS_PCISR**[13]=0) and continue by processing the next task.

When an internal PEX 8311 Master/Target Abort or Retry Timeout is encountered during a Direct Master transfer with multiple Direct Master operations posted in the Direct Master Write FIFO (*for example*, an address, followed by data, followed by another address, followed by data), the PEX 8311 flushes the entire Direct Master Write FIFO when *Direct Master (PCI Initiator) Write FIFO Flush during PCI Master Abort* is disabled (**LCS_LMISC1**[3]=0). When the bit is enabled (**LCS_LMISC1**[3]=1), the PEX 8311 flushes only the aborted Direct Master operation in the Direct Master Write FIFO and skips to the next available address in the FIFO entry. The PEX 8311 does **not** perform any further DM accesss to the PEX 8311 PCI Express Address spaces until the *Received Master/Target Abort* bits are cleared (**LCS_PCISR**[13:12]=00b, respectively).

When an internal PEX 8311 Master/Target Abort is encountered during a Direct Master transfer to the PEX 8311 PCI Express Address space, the PEX 8311 stores the Abort address into **LCS_PABTADR**[31:0] and sets the *Received Master/Target Abort* bits (**LCS_PCISR**[13:12]=11b, respectively). The PEX 8311 disables accesses to the PCI Express Address spaces within the PEX 8311 when **LCS_PCISR**[13:12]=11b. Therefore, in this condition, the PEX 8311 does not perform internal arbitration to the PCI Express Address spaces, to execute new or pending Direct Master or DMA transfers. Should this occur, Read, then clear the *Received Master/Target Abort* bits before starting new Direct Master or DMA transfers. The *Abort Address* field (**LCS_PABTADR**[31:0]) contents are updated for each Master/Target Abort. (For details regarding DMA Master/Target Abort, refer to Section 9.5.18.)

The PEX 8311 Master/Target Abort logic is used by a Local Bus Master to perform a Direct Master Bus poll of devices, to determine whether devices exist (typically when the Local Bus performs Configuration cycles to the PCI Express interface, in Root Complex mode only).

9.2.9.1   Internal PCI Bus Master/Target Abort – C and J Modes

The *Received Master Abort* bit status can also be returned to the Local Bus by way of LSERR#, when enabled [**LCS_INTCSR**[0]=1, which is used as a Non-Maskable Interrupt (NMI)]. (Refer to Chapter 11, "Error Handling," for the LSERR# usage model.)

When Direct Master Writes are posted and internal to the PEX 8311 and a Master/Target Abort occurs, LSERR# is asserted, when enabled (**LCS_INTCSR**[0]=1). When a Local Bus Master is waiting for READY#, LSERR# is asserted along with BTERM#, for Direct Master Read operations only. The Local Bus Master's interrupt handler can take the appropriate application-specific action. It can then clear the *Received Master* or *Target Abort* bit (**LCS_PCISR**[13 or 12]=1, respectively; writing 1 clears the bit to 0) to de-assert the LSERR# interrupt and re-enable Direct Master transfers.

When a Local Bus Master is attempting a Burst Read to the PEX 8311 PCI Express Address space that is not responding (internal Master/Target Abort), it receives READY# and BTERM# until the Local Bus completes a transfer. In addition, the PEX 8311 asserts LSERR# when **LCS_INTCSR**[1:0]=11b (which is used as an NMI). When the Local processor cannot terminate its Burst cycle, it can cause the Local processor to hang. The Local Bus must then be reset from the PCI Express interface. If a Local Bus Master cannot terminate its cycle with BTERM# output, ensure that it does ***not*** perform Burst cycles when attempting to determine whether other devices exist on the PCI Express interface.

9.2.9.2   Internal PCI Bus Master/Target Abort – M Mode

The *Received Master Abort* bit status can also be returned to the Local Bus by way of TEA#, when enabled [**LCS_INTCSR**[0]=1, which is used as a Non-Maskable Interrupt (NMI)]. (Refer to Chapter 11, "Error Handling," for the TEA# usage model.)

When Direct Master Writes are posted and internal to the PEX 8311 and a Master/Target Abort occurs, TEA# is asserted, when enabled (**LCS_INTCSR**[0]=1). When a Local Bus Master is waiting for TA#, TEA# is asserted along with BI#, for Direct Master Read operations only. The Local Bus Master's interrupt handler can take the appropriate application-specific action. It can then clear the *Received Master* or *Target Abort* bit (**LCS_PCISR**[13 or 12]=1, respectively; writing 1 clears the bit to 0) to de-assert the TEA# interrupt and re-enable Direct Master transfers.

When a Local Bus Master is attempting a Burst Read to the PEX 8311 PCI Express Address space that is not responding (internal Master/Target Abort), it receives TA# and BI# until the Local Bus completes a transfer. In addition, the PEX 8311 asserts TEA# when **LCS_INTCSR**[1:0]=11b (which is used as an NMI). When the Local processor cannot terminate its Burst cycle, it can cause the Local processor to hang. The Local Bus must then be reset from the PCI Express interface. If a Local Bus Master cannot terminate its cycle with BI# output, ensure that it does ***not*** perform Burst cycles when attempting to determine whether other devices exist on the PCI Express interface.

9.2.10   Direct Master Memory Write and Invalidate

The PEX 8311 can be programmed to perform Memory Write and Invalidate (MWI) cycles internally between Direct Master and PCI Express Address spaces. The PEX 8311 supports generating internal MWI transfers for Cache Line Sizes of 8 or 16 Dwords. Size is specified in the *System Cache Line Size* field (**LCS_PCICLSR**[7:0]). When a size other than 8 or 16 is specified, the PEX 8311 performs internal Write transfers (using the Command Code programmed in **LCS_CNTRL**[7:4]) rather than MWI transfers. Internal MWI accesses to the PCI Express Spaces do not affect PEX 8311 TLP Write request generation and performance on the PCI Express interface.

Direct Master MWI transfers are enabled when the *MWI Mode* and *MWI Enable* bits are set (**LCS_DMPBAM**[9]=1 and **LCS_PCICR**[4]=1, respectively).

In MWI mode, when the start address of the Direct Master transfer is on a cache line boundary, the PEX 8311 waits until the number of Dwords required for the specified Cache Line Size are written from the Local Bus before starting an internal MWI access to PCI Express Address space. This ensures a complete Cache Line Write can complete in one internal Write cycle.

When the start address is not on a Cache Line boundary, the PEX 8311 defaults to an internal Write access using the Command Codes from the **LCS_CNTRL**[15:12] bits, and the PEX 8311 does not terminate a non-MWI Write at an MWI Cache boundary. The non-MWI Write transfer continues until the Data transfer is complete. When PCI Express Address space disconnects before a Cache Line is completed, the PEX 8311 completes the remainder of that Cache Line, using non-MWI Writes.

When the Direct Master Write is less than the Cache Line Size, the PEX 8311 waits until the next Direct Master Write begins before starting an internal arbitration to the PCI Express Address space. The internal Write retains the MWI command, regardless of the number of Dwords in the Direct Master Write FIFO, which can result in an internal Write completing an MWI cycle with less than one Cache Line of data. For this reason, ensure that Burst Writes are equal to, or multiples of, the Cache Line Size.

M mode only – Because the MPC850 or MPC860 is limited to bursts of 4 Dwords, MWI should be used only with DMA (DMA does not have this issue) or with Direct Master cycles in Continuous Burst mode.

9.2.11   Direct Master Write FIFO Programmable Almost Full, DMPAF Flag

The PEX 8311 supports the Direct Master Write FIFO Programmable Full Flag (**LCS_DMPBAM** [10, 8:5]. The DMPAF signal is used as a hardware indicator Direct Master Write FIFO Full Flag. Note that in M mode, DMPAF is multiplexed with the signals MDREQ# and EOT#. The DMPAF function is selected by programming DMAMODE0[14] and DMAMODE1[14] = 00b. An alternative method (software polling a register bit) is also provided to check the *Direct Master Write FIFO Full Status Flag* (**LCS_MARBR**[30]). To enable DMPAF signal functionality and disable EOT#, clear the *DMA Channel EOT# Enable* bit for the affected DMA channel (**LCS_DMAMODE0/1**[14]=0; default configuration).

DMPAF output assertion relies on the programmable value in **LCS_DMPBAM**[10, 8:5] to determine when to signal that the Direct Master Write FIFO is almost full. After DMPAF assertion, the PEX 8311 de-asserts DMPAF upon the last word of the transfer entering into the internal Data Out Holding latch before entering the PEX 8311 PCI Express Address space. The DMPAF signal indicates the Direct Master Write FIFO status, *not* transfer status completion.

9.2.12   RETRY# Capability – M Mode Only

The PEX 8311 supports a Direct Master Write FIFO full condition in one of two ways:

- When FIFO Almost Full Retry is enabled (**LCS_LMISC1**[6]=1), the PEX 8311 asserts Local RETRY# to force the Local Master to stop its Write cycle. The Local Master can later return and complete the Write.

- If FIFO Almost Full Retry is disabled (**LCS_LMISC1**[6]=0), the PEX 8311 de-asserts TA# (and does not assert RETRY#) until there is space in the FIFO for additional Write data.

9.2.13   IDMA Operation – M Mode Only

The PEX 8311 supports the MPC850 or MPC860 Independent DMA (IDMA) mode, using the MDREQ# signal and operating in Direct Master mode. MDREQ# is connected to the MPC850 or MPC860 DREQx# input balls. After programming the MPC850 or MPC860 IDMA channel, the PEX 8311 uses Direct Master mode to transfer data between the PCI Express Bus and the MPC850 or MPC860 internal dual-port RAM (or external memory). The data count is controlled by the IDMA Byte counter and throttled by the PEX 8311 MDREQ# signal. When the PEX 8311 Direct Master Write FIFO is nearly full, MDREQ# is de-asserted to the MPC850 or MPC860, indicating that it should inhibit transferring further data (the FIFO threshold count in the PEX 8311 must be set to a value of at least 6 Dwords below the full capacity of the FIFO – 58 Dwords to prevent FIFO overflow (**LCS_DMPBAM**[10, 8:5]). The Retry function can be used to communicate to the Local Bus Master that it should relinquish Local Bus ownership.

*Note: The Direct Master Write FIFO Almost Full RETRY# Output Enable bit can be disabled (**LCS_LMISC1**[6]=0) to prevent RETRY# assertion.*

In IDMA reads (PEX 8311 to the Local Bus), MDREQ# is asserted (indicating data is available), although the Read FIFO is empty. Any Local Bus read of the PCI Express Bus causes the PEX 8311 to send a PCIe read request, the completion of which will place data in the Direct Master Read FIFO buffer. When sufficient data is in the FIFO, the PEX 8311 completes the Local Bus cycle by asserting Transfer Acknowledge (TA#).

In IDMA writes (Local-to-PCI Bus), MDREQ# is asserted (indicating that the Direct Master FIFO is capable of accepting additional data). After the IDMA has transferred all required bytes [MPC850 or MPC860 Byte counter decrements to zero (0)], the MPC850 or MPC860 generates an internal interrupt, which in turn should execute the code to disable the IDMA channel (the PEX 8311 may still assert MDREQ# output). The PEX 8311 does *not* use the MPC850 nor MPC860 SDACK[1:0]# signals (no connection).

Refer to Section 9.2 for further details about Direct Master Data transfers.

9.2.14   SDMA Operation – M Mode Only

The PEX 8311 supports the MPC850 or MPC860 Serial DMA (SDMA) mode, using Direct Master mode. No handshake signals are required to perform the SDMA operation.

The Retry function can be used to communicate to the Local Bus Master that it should relinquish Local Bus ownership. The *Direct Master Write FIFO Almost Full RETRY# Output Enable* bit can be disabled (**LCS_LMISC1**[6]=0) to prevent RETRY# assertion.

*Note: The Direct Master Write FIFO can be programmed to identify the full status condition (**LCS_DMPBAM**[10, 8:5]). The Direct Master Write FIFO Full Status Flag is in **LCS_MARBR**[30].*

9.3   Direct Slave Operation

For Direct Slave writes, the PCI Express interface writes data to the Local Bus. Direct Slave is Write/ Read requests that are initiated from the PCI Express interface, with the highest priority.

For Direct Slave reads, the PCI Express device initiates Read requests to the PEX 8311. The PEX 8311 arbitrates on the Local Bus and becomes the Local Bus Master. The PEX 8311 reads data from the Local Bus Slave into the Direct Slave Read FIFO and returns the data to the PCI Express Read Requester by way of initiating PCI Express Read Completion. Direct Slave or Direct Master preempts DMA; however, Direct Slave does *not* preempt Direct Master on the Local Bus. (Refer to Section 9.3.11.)

The PEX 8311 supports Burst Memory-Mapped Transfer accesses and I/O-Mapped, Single-Transfer PCI Express-to-Local Bus accesses through a 32-Dword (128-byte) Direct Slave Read FIFO and a 64-Dword (256-byte) Direct Slave Write FIFO on the Local Bus. The PCI Express Base Address registers on the PEX 8311 Local Bus (**LCS_PCIBAR0**, **LCS_PCIBAR1**, **LCS_PCIBAR2**, and **LCS_PCIBAR3**) are provided to set the adapter location in respect to the PCI Express Address spaces as either Memory- or I/O-Mapped space. In addition, Local mapping registers allow Address Translation from the PCI Express Address space to the Local Address space.

Three Local Address spaces are available:

- Space 0
- Space 1
- Expansion ROM[1] (Expansion ROM is intended to support a bootable Host ROM device)

Direct Slave supports on-the-fly Local Bus Endian conversion for Space 0, Space 1, and Expansion ROM space.

Each Local space is programmed to operate with an 8-, 16-, or 32-bit Local Bus data width. The PEX 8311 includes an internal wait state generator and READY# input signal that is used to externally assert wait states. READY# is selectively enabled or disabled for each Local Address space (**LCS_LBRD0/1**[6] for Space 0/1, and/or **LCS_LBRD0**[22] for Expansion ROM).

Independent of the PCI Express interface, the Local Bus can perform:

- Bursts as long as data is available (Continuous Burst mode)
- Bursts of 4 Dwords, words, or bytes at a time (Burst-4 mode, recommended)
- Continuous single cycles (default)

The *Direct Slave Retry Delay Clock* field (**LCS_LBRD0**[31:28]) can be used to program the period of time in which the PEX 8311 holds the internal PCI Bus in a wait state. The PEX 8311 internally issues a Retry to the PCI Express Address Space transaction when the programmed time period expires. This occurs when the PEX 8311 cannot gain control of the Local Bus and continue providing data to the PCI Express Address space within the programmed time period.

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1.   Expansion ROM is not restricted to ROM devices. It can be used as another Memory-Mapped space to the Local Bus devices in embedded systems.

9.3.1   Direct Slave Writes

For a PCI Express interface Write, the PCI Express device initiates a Write request and writes data to the PEX 8311 PCI Express Address space. The PCI Express Address space internally arbitrates to complete the Direct Slave Write transfer by transferring payload data to the Direct Slave Write FIFO. When the first data is in the FIFO, the PEX 8311 arbitrates for the Local Bus, becomes the Local Bus Master, and writes data to a Local slave device. The PEX 8311 continues to accept Writes until the Direct Slave Write FIFO is full. The PEX 8311 then issues internal wait states between the PCI Express and Local Bus Address spaces until space becomes available in the Direct Slave Write FIFO, or issues a Retry to the PCI Express Address space, dependent upon the **LCS_LBRD0**[27] register bit setting.

9.3.1.1   Direct Slave Writes – C and J Modes

A PCI Express single data (1-Dword) cycle Write transaction results in a PEX 8311 transfer of 1 Dword of data onto the Local Bus. A PCI Express multiple Data (2 or more Dwords) cycle results in a Burst transfer of multiple data (2 or more Dwords) onto the Local Bus, when the *Burst* bit for the affected Local Address space is enabled (**LCS_LBRD0**[24]=1 for Space 0, **LCS_LBRD1**[8]=1 for Space 1, and/or **LCS_LBRD0**[26]=1 for Expansion ROM).

The PEX 8311 can be programmed to generate wait states on the internal PCI Bus if the Direct Slave Write FIFO becomes full (LCS_MARBR[24] = 0). The PEX 8311 can also be programmed to retain the Local Bus and continue asserting LHOLD, when the Direct Slave Write FIFO becomes empty. If the Local Bus Latency Timer is enabled (**LCS_MARBR**[16]=1) and expires (**LCS_MARBR**[7:0]), the Local Bus is dropped.

A continuous Write cycle (multiple Dwords in one payload) from the PCI Express interface through the PEX 8311 performs a Local Bus Burst transaction, when the following conditions are true:

- The address is Dword-aligned,
- The Direct Slave Write FIFO contains at least 2 Dwords, and
- The PCI Express single payload contains contiguous data. Default by the *PCI Express Base 1.0a*.

Figure 9-7 illustrates the FIFOs that function during a Direct Slave Write in C and J modes.

Figure 9-7. Direct Slave Write – C and J Modes
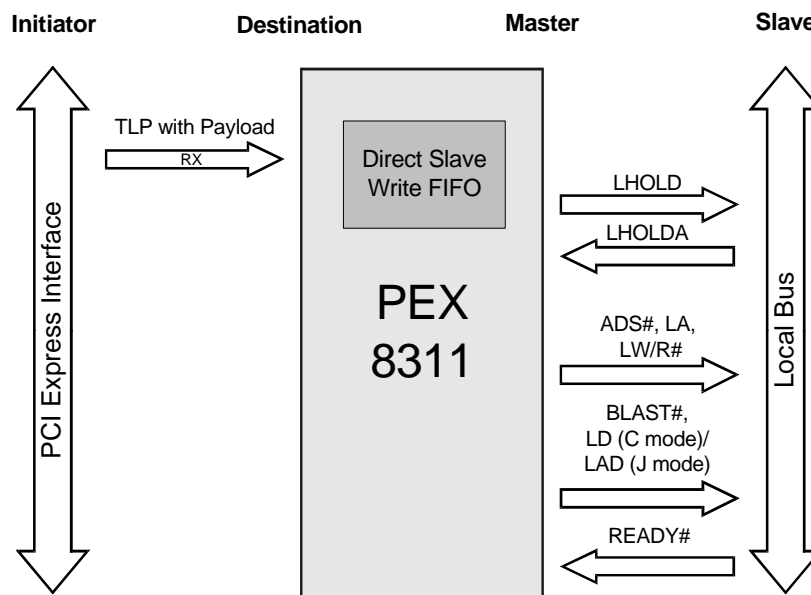
Note: Figure 9-7 represents a sequence of Bus cycles.

9.3.1.2   Direct Slave Writes – M Mode

A PCI Express single Dword Write transaction results in a PEX 8311 transfer of 1 Dword of data onto the Local Bus. A PCI Express transaction with 2 Dwords of data results in PEX 8311 Burst transfers of 2 Dwords [when the *BI Mode* bit is enabled] onto the Local Bus, if the *Burst* bit is enabled (**LCS_LBRD0**[24]=1 for Space 0, **LCS_LBRD1**[8]=1 for Space 1, and/or **LCS_LBRD0**[26]=1 for Expansion ROM).

By means of the local bus latency timer the PEX 8311 can be programmed to retain the Local Bus when the Direct Slave Write FIFO becomes empty. If the Local Bus Latency Timer is enabled (**LCS_MARBR**[16]=1) and expires (**LCS_MARBR**[7:0]), the Local Bus is dropped

A continuous Write cycle (multiple Dwords in one payload) from the PCI Express interface through the PEX 8311 performs an MPC850 or MPC860 Burst transaction, when the following conditions are true:

• The address is Dword-aligned,

• The Direct Slave Write FIFO contains at least 4 Dwords, and

• The PCI Express single payload contains contiguous data. Default by the *PCI Express Base 1.0a*.

Figure 9-8 illustrates the FIFOs that function during a Direct Slave Write in M mode.

Figure 9-8.   Direct Slave Write – M Mode
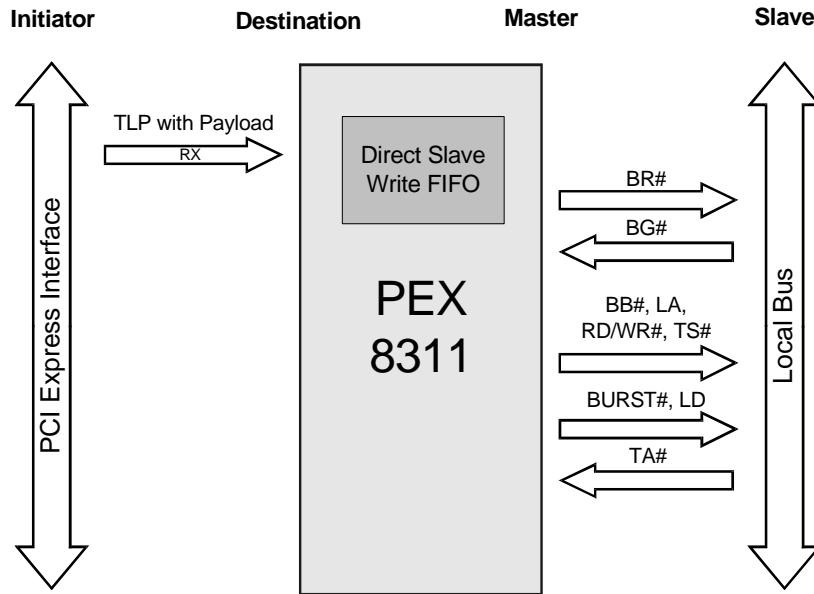
Note: Figure 9-8 represents a sequence of Bus cycles.

9.3.1.3   Dummy Cycles

9.3.1.3.1   Dummy Cycles – C and J Modes

The PEX 8311 transfers dummy data by way of a dummy cycle, with LBE[3:0]#=Fh when the last data of the PCI Express payload is dummy data (Byte Field = 0h and the Local Bus data width is 32 bits). The PEX 8311 suppresses all other dummy cycles, other than the last data of the burst, and/or if the Local Bus data width is 8 or 16 bits.

9.3.1.3.2   Dummy Cycles – M Mode

The PEX 8311 suppresses all dummy cycles on the Local Bus.

9.3.2   Direct Slave Reads

The PEX 8311 issues internal wait states to the PCI Express Address space as a Read request is processed until the PEX 8311 Local Bus receives data from the Local Bus Slave. (Refer to Section 9.3.4.) Programmable Prefetch modes are available, when prefetch is enabled – prefetch, 1 to 16, or continuous data – until the Direct Slave Read ends. The Local prefetch continues until sufficient data is fetched for the PCI Express transfer, or until the prefetch conditions set in the bus region descriptors are met. Extra prefetched data is flushed from the FIFO unless Direct Slave Read Ahead mode is enabled (**LCS_MARBR**[28]=1).

For the highest data transfer rate, the PEX 8311 can be programmed to prefetch data for any PCI Express Read request on the Local Bus. When Prefetch is enabled (**LCS_LBRD0**[8]=0 for Space 0, **LCS_LBRD1**[9]=0 for Space 1, and/or **LCS_LBRD0**[9]=0 for Expansion ROM), prefetch is from 1 to 16 Dwords or until all PCI Express Read requests are completed. When the PEX 8311 prefetches, it drops the Local Bus after reaching the Prefetch Counter limit. In Continuous Prefetch mode, the PEX 8311 prefetches when FIFO space is available and stops prefetching when the PCI Express Address space stops requesting Read data. When Read prefetching is disabled, the PEX 8311 disconnects from the Local Bus after each Read transfer is performed.

In addition to Prefetch mode, the PEX 8311 supports Direct Slave Read Ahead mode (**LCS_MARBR**[28]=1). (Refer to Section 9.3.6.)

9.3.2.1   Direct Slave Reads – C and J Modes

For PCI Express interface Direct Slave Prefetch Read transfers starting at a Dword-aligned boundary, the PEX 8311 prefetches the amount specified in the Prefetch Counter(s). When a Direct Slave Prefetch Burst Read transfer is performed to a Local Bus device that cannot burst, and READY# is asserted for only one clock period, the PEX 8311 retains the Read data in the Direct Slave Read FIFO without ever transferring to the PCI Express Address space to generate a Read Completion TLP. This occurs because the PEX 8311 Local Bus interface is built with 2-Dword FIFO architecture per each Direct Slave FIFO location, and a prefetch mechanism is required to prefetch further data for transferring to occur. Under such conditions, it is necessary to disable a Prefetch or Burst feature.

Only PCI Express single Dword Read requests result in the PEX 8311 passing requested Byte Enables (TLP Byte field) to a Local Bus Target device by way of LBE[3:0]# assertion back to a PCI Express Read Requester. This transaction results in the PEX 8311 reading 1 Dword or partial Dword data. For all other types of Read transactions (PCI Express Multiple Data Read request Dword-Aligned and Unaligned), the PEX 8311 reads Local Bus data with all bytes asserted (LBE[3:0]#=0h)

The PEX 8311 performs only single cycle transfers for Direct Slave I/O accesses by the PCI Express Address space to the Local Bus Address space, when Direct Slave space(s) is I/O-mapped.

The PEX 8311 can be programmed to retain the Local Bus and continue asserting LHOLD when the Direct Slave Read FIFO becomes full. When the Local Bus Latency Timer is enabled (**LCS_MARBR**[16]=1) and expires (**LCS_MARBR**[7:0]), the Local Bus is dropped.

Figure 9-9 illustrates the FIFOs that function during a Direct Slave Read in C and J modes.

Figure 9-9.   Direct Slave Read – C and J Modes
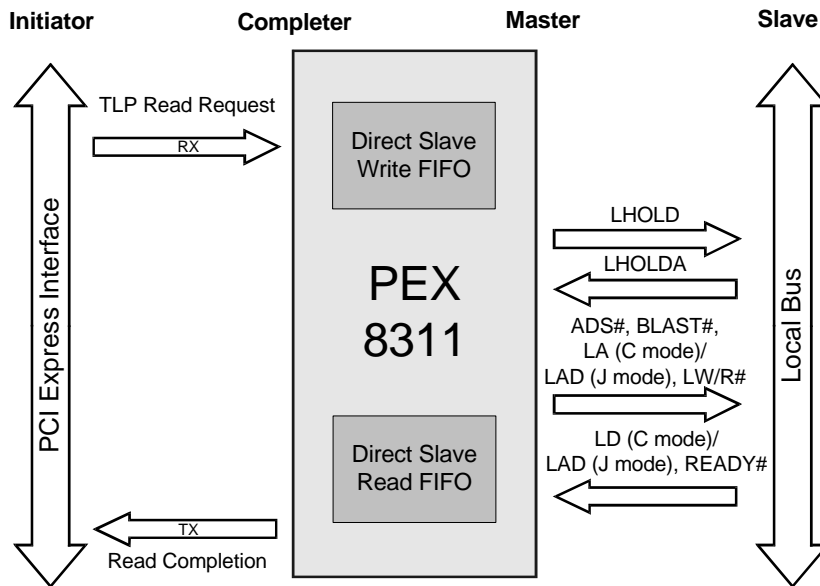
Note: Figure 9-9 represents a sequence of Bus cycles.

9.3.2.2   Direct Slave Reads – M Mode

For PCI Express interface Direct Slave Prefetch Read transfers starting at a Dword-aligned boundary, the PEX 8311 prefetches the amount specified in the Prefetch Counter(s). When a Direct Slave Prefetch Burst Read transfer is performed to a Local Bus device that cannot burst, and TA# is asserted for only one clock period, the PEX 8311 retains the Read data in the Direct Slave Read FIFO without ever transferring to the PCI Express Address space to generate a Read Completion TLP. This occurs because the PEX 8311 Local Bus interface is built with 2-Dword FIFO architecture per each Direct Slave FIFO location, and a prefetch mechanism is required to prefetch further data for transferring to occur. Under such conditions, it is necessary to disable a Prefetch or Burst feature.

Only PCI Express single Dword Read requests result in the PEX 8311 passing requested Byte Enables (TLP Byte field) to a Local Bus Target device by way of TSIZ[0:1] assertion. This transaction results in the PEX 8311 reading 1 Dword or partial Dword data. For all other types of Read transactions (PCI Express Multiple Data Read request Dword-Aligned and Unaligned), the PEX 8311 reads one or more complete Dwords (4 bytes).

For Read accesses mapped to PCI I/O space, the PEX 8311 does not prefetch Read data. Rather, it breaks each read of a Burst cycle into a single Address/Data cycle on the Local Bus.

If the Local Bus Latency Timer is enabled (**LCS_MARBR**[16]=1) and expires (**LCS_MARBR**[7:0]), and M mode protocol requirements are met, the Local Bus is dropped.

Figure 9-10 illustrates the FIFOs that function during a Direct Slave Read in M mode.

Figure 9-10.   Direct Slave Read – M Mode
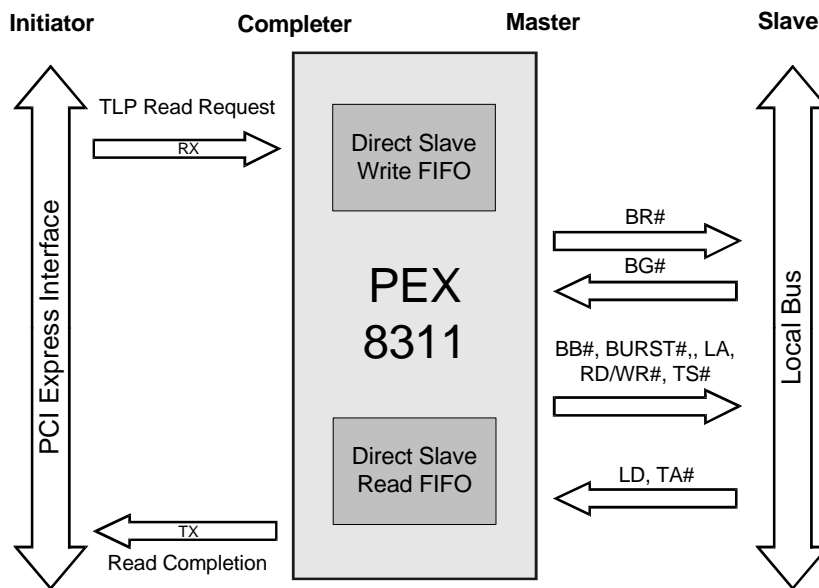
Note: Figure 9-10 represents a sequence of Bus cycles.

9.3.3   Direct Slave Lock

The PEX 8311 supports direct PCI Express-to-Local Bus exclusive accesses (locked atomic operations). A PCI Express-locked operation to the Local Bus results in the entire address Space 0, Space 1, and Expansion ROM space being locked until they are released by the PCI Express interface. Locked operations are enabled or disabled with the Memory Read Locked request on the *Direct Slave Internal LOCK# Input Enable* bit (**LCS_MARBR**[22]) for the internal LOCK# signal.

9.3.4   PCI Compliance Enable

The PEX 8311 can be programmed through the *PCI Compliance Enable* bit to perform Read/Write transactions between PCI Express and Local Bus Spaces in compliance with the *PCI r2.2* (**LCS_MARBR**[24]=1). The following sections describe the behavior of the PEX 8311 when **LCS_MARBR**[24]=1.

9.3.4.1   Direct Slave Delayed Read Mode – C and J Modes

PCI Express single Dword or partial Dword Direct Slave Read request always result in a 1-Dword single cycle transfer on the Local Bus, with the corresponding Local Byte Enables (LBE[3:0]#) asserted to reflect the PCI Express Byte field of the Requester unless the *PCI Read No Flush Mode* bit is enabled (**LCS_MARBR**[28]=1). (Refer to Section 9.3.6.) This causes the PEX 8311 to Retry internal PCI Express Address Space accesses to the Local Bus Spaces that follow, until the original Read address and Byte field of the Read request match.

PCI Express multiple Data Dword-aligned and unaligned Direct Slave Read requests result in a Prefetch Burst Read Cycle transfer on the Local Bus, with all Local Byte Enables (LBE[3:0]#=0h) asserted, when the Burst bit for the affected Local Address space is enabled (**LCS_LBRD0**[24]=1 for Space 0, **LCS_LBRD1**[8]=1 for Space 1, and/or **LCS_LBRD0**[26]=1 for Expansion ROM). (Refer to Figure 9-11.)

Figure 9-11.   Direct Slave Delayed Read Mode – C, J, and M Modes
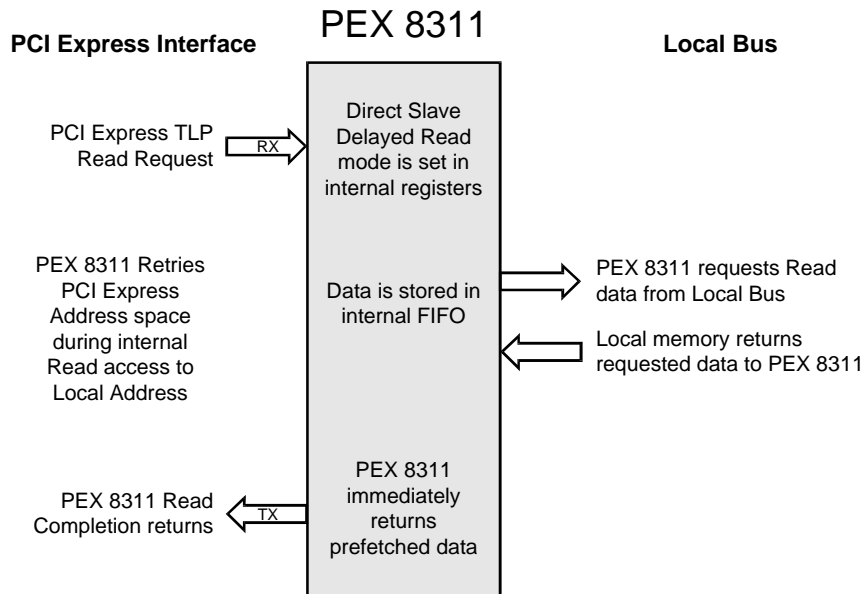
Note: Figure 9-11 represents a sequence of Bus cycles.

9.3.4.2 Direct Slave Delayed Read Mode – M Mode

PCI Express Dword cycle aligned or unaligned Direct Slave Read transactions always result in a 1-Dword single cycle transfer on the Local Bus, with corresponding Local Address and TSIZ[0:1] to reflect the PCI Byte Enables (C/BE[3:0]#) unless the *PCI Read No Flush Mode* bit is enabled (**LCS_MARBR**[28]=1). (Refer to Section 9.3.6.) This causes the PEX 8311 to internally retry all Read requests that follow, until the original PCI Byte Enables are matched.

16-byte-aligned address Direct Slave Read transactions always result in a Prefetch Burst Read Cycle transfer on the Local Bus, with all Transfer Size signals (TSIZ[0:1]) asserted, if the Burst bit(s) is enabled (**LCS_LBRD0**[24]=1 for Space 0, **LCS_LBRD1**[8]=1 for Space 1, and/or **LCS_LBRD0**[26]=1 for Expansion ROM). The unaligned Direct Slave Read transactions always result in Prefetch Single Cycle transfers on the Local Bus until the next 16-byte-aligned address. The Local Bus Prefetch burst starts on a 16-byte aligned address boundary if more data is required to be prefetched. (Refer to Figure 9-11.)

9.3.4.3 2^{15} Internal Clock Timeout

When the PEX 8311 PCI Express Address space does not complete the originally requested Direct Slave Delayed Read transfer, the PEX 8311 flushes the Direct Slave Read FIFO after 2^{15} internal clocks and accepts a new Direct Slave Read access. All other Direct Slave Read accesses before the 2^{15} internal clock timeout are Retried internally between PCI Express Address space and Local Bus Spaces within the PEX 8311.

9.3.4.4 *PCI r2.2* 16- and 8-Clock Rule

The PEX 8311 internally guarantees that if the first Direct Slave Write data coming from the PCI Express Address spaces cannot be accepted by the PEX 8311 Local Spaces and/or the first Direct Slave Read data cannot be returned by the PEX 8311 Local spaces to the PCI Express Address spaces within 16 internal clocks from the beginning of the internal start of the transfer, the PEX 8311 issues an internal Retry to the PCI Express Address space(s).

During successful Direct Slave Read and/or Write accesses, the subsequent data after the first access must be accepted for Writes or returned for Reads within 8 internal clocks. Otherwise, the PEX 8311 issues an internal disconnect to the PCI Express Address space(s). In addition, the PEX 8311 internally supports the following *PCI r2.2* functions between PCI Express Address spaces and Local spaces:

- No Write while a Delayed Read is pending (Local Retries for Writes) (**LCS_MARBR**[25])
- Write and flush pending Delayed Read (**LCS_MARBR**[26])

9.3.5 Direct Slave Delayed Write Mode

9.3.5.1 Direct Slave Delayed Write Mode – C and J Modes

The PEX 8311 supports Direct Slave Delayed Write mode transactions, in which Posted Write data coming from PCI Express Address spaces accumulates in the Direct Slave Write FIFO before the PEX 8311 requests ownership of the Local Bus (LHOLD assertion). Direct Slave Delayed Write mode can be programmed to delay LHOLD assertion for the number of Local clocks specified in **LCS_LMISC2**[4:2].

9.3.5.2 Direct Slave Delayed Write Mode – M Mode

The PEX 8311 supports Direct Slave Delayed Write mode transactions, in which Posted Write data coming from PCI Express Address spaces accumulates in the Direct Slave Write FIFO before the PEX 8311 requests ownership of the Local Bus (BR# assertion). Direct Slave Delayed Write mode can be programmed to delay BR# assertion for the number of Local clocks specified in **LCS_LMISC2**[4:2].

9.3.6 Direct Slave Read Ahead Mode

The PEX 8311 also supports Direct Slave Read Ahead mode (**LCS_MARBR**[28]=1) in Local Spaces, wherein prefetched data is read from the internal Direct Slave FIFO by the PCI Express Address spaces instead of directly from the Local Bus. For these features to be in effect, all PCI Express Read requests must be subsequent to the previous address and Dword-aligned (next address = current address + 4) for Direct Slave Read request transfers. Direct Slave Read Ahead mode functions are used with or without Direct Slave Delayed Read mode. (Refer to Figure 9-12.)

Figure 9-12.   Direct Slave Read Ahead Mode
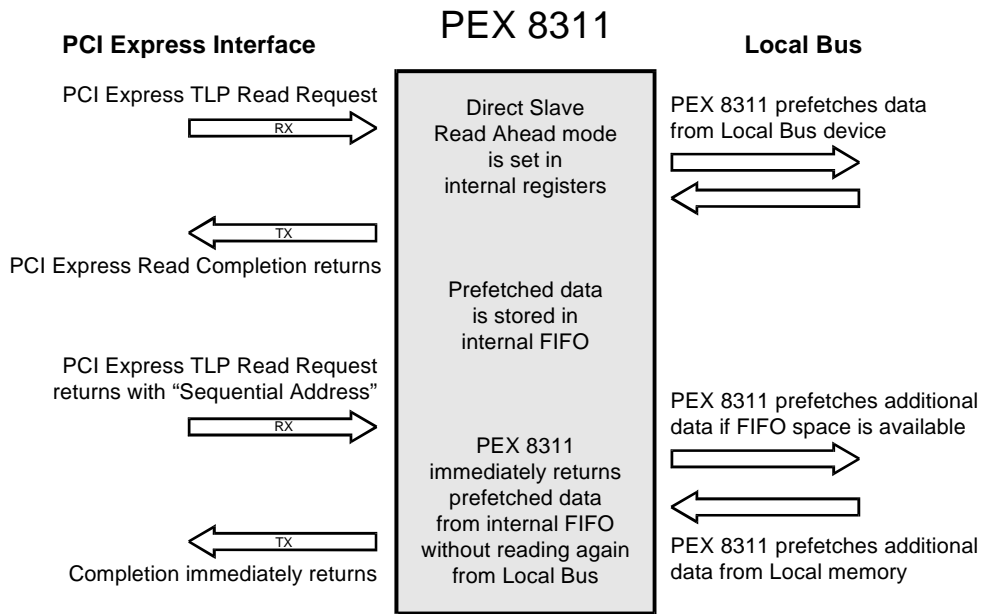
Note: Figure 9-12 represents a sequence of Bus cycles.

9.3.7   Direct Slave Local Bus READY# Timeout Mode – C and J Modes Only

Direct Slave Local Bus READY# Timeout mode is enabled/disabled by **LCS_LMISC2**[0].

When Direct Slave Local Bus READY# Timeout mode is disabled (**LCS_LMISC2**[0]=0), *and* the PEX 8311 is mastering the Local Bus during a Direct Slave Read or Write Data transfer, *and* no Local Bus device asserts READY# in response to the Local Bus address generated by the PEX 8311, the PEX 8311 hangs on the Local Bus waiting for READY# assertion. To recover, reset the PEX 8311.

When Direct Slave Local Bus READY# Timeout mode is enabled (**LCS_LMISC2**[0]=1), *and* the PEX 8311 is mastering the Local Bus during a Direct Slave Read or Write Data transfer, the PEX 8311 uses the *READY# Timeout Select* bit (**LCS_LMISC2**[1]) to determine when to timeout while waiting for a Local Bus device to assert READY# in response to the Local Bus address generated by the PEX 8311:

- When **LCS_LMISC2**[1]=0, the PEX 8311 waits 32 Local Bus clocks for READY# assertion before timing out
- When **LCS_LMISC2**[1]=1, the PEX 8311 waits 1,024 Local Bus clocks for READY# assertion before timing out

When a Direct Slave Local Bus READY# Timeout occurs during a Direct Slave Read (PCI Express Read request), the PEX 8311 issues a Target Abort to the PCI Express Address space(s) which is then converted into the PCI Express Completion Abort to the PCI Express Read Requester. When the PCI Express Address space is in the process of accessing Local space(s) (*that is*, the PEX 8311 Local Address space(s) is not awaiting a PCI Express Address space Retry of the Direct Slave Read), the Target Abort is immediately issued to the PCI Express Address space(s), which is converted to the PCI Express Completion Abort to the PCI Express Read Requester. When the PCI Express Address space is not currently accessing Local Address space(s) the PEX 8311 (*that is*, the PEX 8311 Local Address space(s) is awaiting a PCI Express Address space Retry of the Direct Slave Read), the PEX 8311 issues a Target Abort the next time the PCI Express Address space(s) repeats the Direct Slave read, which then is converted to the PCI Express Completion Abort to the PCI Express Read Requester.

When a Direct Slave Local Bus READY# Timeout occurs during a Direct Slave Write (PCI Express Write request) *and* the PCI Express Address space(s) is currently accessing Local Address spaces the PEX 8311 (*that is*, the PCI Express Address space(s) has not posted the Direct Slave Write into the Local Address space(s) within the PEX 8311), the PEX 8311 immediately issues a Target Abort to the PCI Express Address space(s), which is then converted to ERR_NONFATAL message. (Refer to Chapter 11, "Error Handling," for details.) When the PCI Express Address space(s) is not currently accessing Local Address space(s) the PEX 8311 (*that is*, the PCI Express Address space(s) has posted the Direct Slave write into the Local Address space), the PEX 8311 does **not** issue to the PCI Express Address space(s) any indication that the timeout occurred.

Caution: ***Use the PEX 8311 Direct Slave Local Bus READY# Timeout feature only during design debug. This feature allows illegal Local Bus addresses to be easily detected and debugged. After the design is debugged and legal addresses are guaranteed, disable Direct Slave Local Bus READY# Timeout mode to avoid unreported timeouts during Direct Slave Writes.***

9.3.8   Direct Slave Local Bus TA# Timeout Mode – M Mode Only

Direct Slave Local Bus TA# Timeout mode is enabled/disabled by **LCS_LMISC2**[0].

If Direct Slave Local Bus TA# Timeout mode is disabled (**LCS_LMISC2**[0]=0), *and* the PEX 8311 is mastering the Local Bus during a Direct Slave Read or Write Data transfer, *and* no Local Bus device asserts TA# in response to the Local Bus address generated by the PEX 8311, the PEX 8311 hangs on the Local Bus waiting for TA# assertion. To recover, reset the PEX 8311.

If Direct Slave Local Bus TA# Timeout mode is enabled (**LCS_LMISC2**[0]=1), *and* the PEX 8311 is mastering the Local Bus during a Direct Slave Read or Write Data transfer, the PEX 8311 uses the *TA# Timeout Select* bit (**LCS_LMISC2**[1]) to determine when to timeout while waiting for a Local Bus device to assert TA# in response to the Local Bus address generated by the PEX 8311:

- When **LCS_LMISC2**[1]=0, the PEX 8311 waits 32 Local Bus clocks for TA# assertion before timing out
- When **LCS_LMISC2**[1]=1, the PEX 8311 waits 1,024 Local Bus clocks for TA# assertion before timing out

If a Direct Slave Local Bus TA# Timeout occurs during a Direct Slave read, the PEX 8311 issues a Target Abort to the PCI Bus Master. If the PCI Bus Master is currently mastering the PEX 8311 (*that is*, the PEX 8311 is not awaiting a PCI Bus Master Retry of the Direct Slave Read), the Target Abort is immediately issued. If the PCI Bus Master is not currently mastering the PEX 8311 (*that is*, the PEX 8311 is awaiting a PCI Bus Master Retry of the Direct Slave Read), the PEX 8311 issues a Target Abort the next time the PCI Bus Master repeats the Direct Slave Read.

If a Direct Slave Local Bus TA# Timeout occurs during a Direct Slave Write *and* the PCI Bus Master is currently mastering the PEX 8311 (*that is*, the PCI Bus Master has not posted the Direct Slave Write to the PEX 8311), the PEX 8311 immediately issues a Target Abort to the PCI Bus Master. If the PCI Bus Master is not currently mastering the PEX 8311 (*that is*, the PCI Bus Master has posted the Direct Slave Write to the PEX 8311), the PEX 8311 does *not* issue to the PCI Bus Master any indication that the timeout occurred.

Caution: ***Use the PEX 8311 Direct Slave Local Bus TA# Timeout feature only during design debug. This feature allows illegal Local Bus addresses to be easily detected and debugged. Once the design is debugged and legal addresses are guaranteed, disable Direct Slave Local Bus TA# Timeout mode to avoid unreported timeouts during Direct Slave Writes.***

9.3.9   Direct Slave Transfer Error

The PEX 8311 supports Local Bus error conditions that use TEA# as an input. A Local Bus device may assert TEA#, either before or simultaneously with TA#. In either case, the PEX 8311 tries to complete the current transaction by transferring data and then asserting TS# for every address that follows, waiting for another TA# or TEA# to be issued (used to flush the Direct Slave FIFOs). To prevent bursting, hold TEA# asserted until the Direct Slave transfer completes. After sensing that TEA# is asserted, the PEX 8311 asserts PCI SERR# and sets an error flag, using the *Signaled System Error (SERR# Status)* bit (**LCS_PCISR**[14]=1). When set, this indicates a catastrophic error occurred on the Local Bus. SERR# can be masked off by resetting the *TEA# Input Interrupt Mask* bit (**LCS_LMISC1**[5]=0).

9.3.10   Direct Slave PCI Express-to-Local Address Mapping

Note: Not applicable in I₂O mode.

Three Local Address spaces – Space 0, Space 1, and Expansion ROM – are accessible from the PCI Express interface through the PEX 8311 PCI Express Address spaces. Each is defined by a set of three registers:

- **LCS Direct Slave Local Address Space Range** (**LCS_LAS0RR**, **LCS_LAS1RR**, and/or **LCS_EROMRR**)

- **LCS Direct Slave Local Address Space Local Base Address** (Remap) (**LCS_LAS0BA**, **LCS_LAS1BA**, and/or **LCS_EROMBA**)

- **LCS PCI Express Base Address** (**LCS_PCIBAR2**, **LCS_PCIBAR3**, and/or **LCS_PCIERBAR**)

A fourth register, the **LCS Bus Region Descriptor** register for PCI Express-to-Local Accesses for the affected Local Address space (**LCS_LBRD0/1**), defines the Local Bus characteristics for the Direct Slave regions. (Refer to Figure 9-13.)

Each PCI Express-to-Local Address space is defined as part of reset initialization, as described in Section 9.3.10.1. These Local Bus characteristics are modified at any time before actual data transactions.

9.3.10.1   Direct Slave Local Bus Initialization

Range – Specifies which PCI Express Address bits of PCI Express Address space(s) to use for decoding a PCI Express access to Local Bus Space. Each bit corresponds to a PCI Express Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others.

Remap PCI Express-to-Local Addresses into a Local Address Space – Bits in this register remap (replace) the PCI Express Address bits used in decode as the Local Address bits.

Local Bus Region Descriptor – Specifies the Local Bus characteristics.

9.3.10.2   Direct Slave PCI Express Initialization

After a PCI Express Reset (PERST#), the software determines which PCI Express Address spaces are present and the amount of resource allocation required by each. It then configures the subordinate bus (the internal PCI Bus between the PCI Express Address spaces and Local Bus Spaces) and determines the amount of Address space required by writing all ones (1) to a **PCI Express Base Address** register and then reading back the value. The PEX 8311 Local Bus Space (**PCI Express Base Address** registers) returns zeros (0) in the "don't care" *Address* bits, effectively specifying the Address space required. The PCI Express software then maps the Local Address space into the PCI Express Address space, by programming the *PCI Express Base Address* register. (Refer to Figure 9-13.)

Figure 9-13.   Local Bus Direct Slave Access
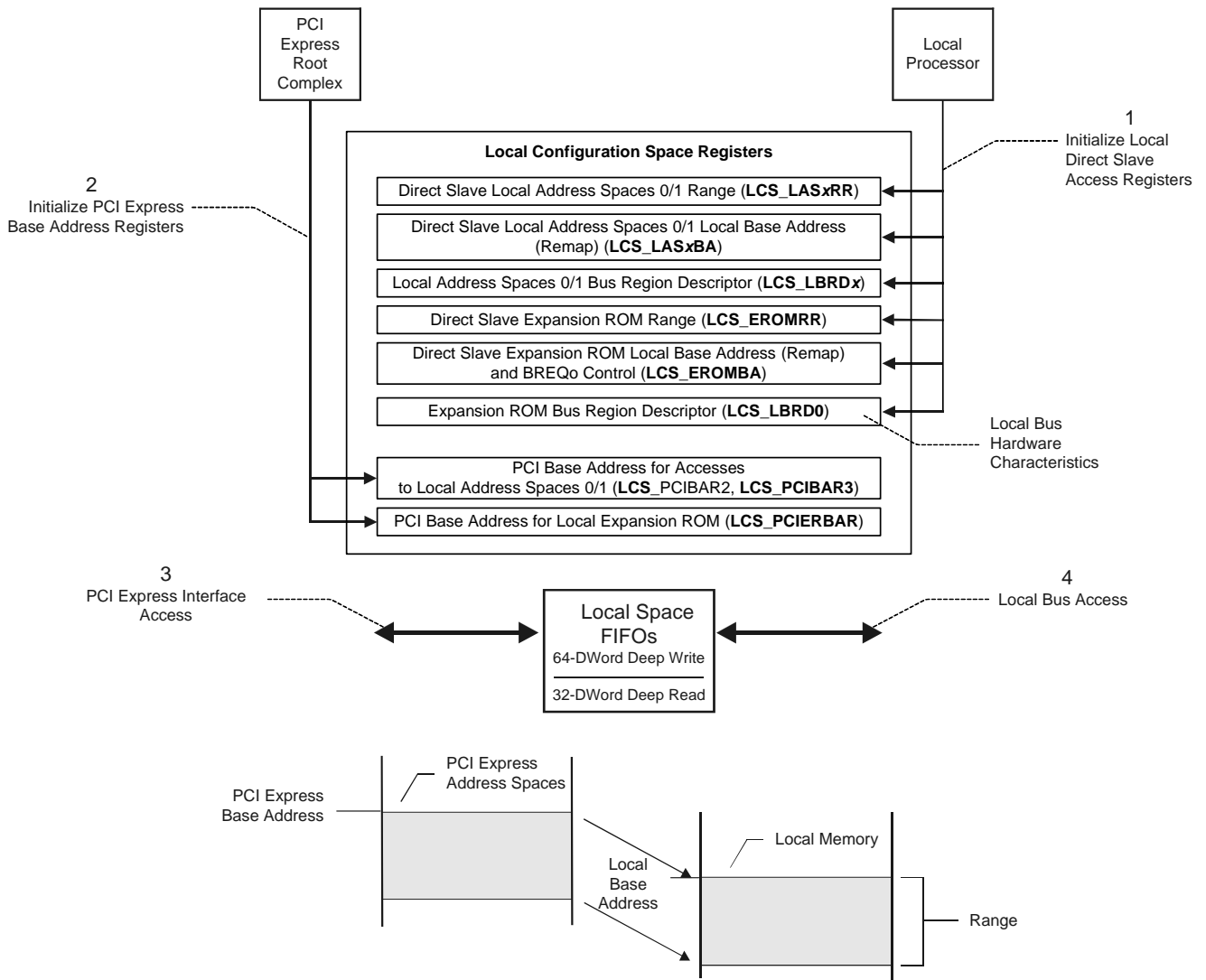
9.3.10.3   Direct Slave PCI Express Initialization Example

A 1-MB Local Address space, 1230_0000h through 123F_FFFFh, is accessible by the PCI Express Address space, using the internal PCI Bus at PCI Express addresses 7890_0000h through 789F_FFFFh.

1. Local initialization software or the serial EEPROM contents set the **Range** and **Local Base Address** registers, as follows:

- **Range** – FFF0_0000h (1 MB, decode the upper 12 *PCI Express Address* bits).
- **Local Base Address (Remap)** – 1230_0000h (Local Base Address for PCI Express-to-Local accesses [*Space Enable* bit for the affected Local Address space must be set, to be recognized by the PCI Host (**LCS_LAS0BA** and/or **LCS_LAS1BA**[0]=1)].

2. PCI Express Initialization software writes all ones (1) to the PEX 8311 Local Bus, PCI Express Base Address, then reads it back again.

- The PEX 8311 returns a value of FFF0_0000h. The PCI Express software then writes to the PCI Express Base Address register(s).
- **PCI Express Base Address** – 7890_0000h (the PEX 8311 Local Bus, **PCI Express Base Address for Access to the Local Address Space** registers, **LCS_PCIBAR2** and **LCS_PCIBAR3**).

9.3.10.4   Direct Slave Byte Enables – C and J Modes Only

During a Local Bus bridge Direct Slave transfer, each of three spaces (Space 0, Space 1, and Expansion ROM) are programmed to operate in an 8-, 16-, or 32-bit Local Bus data width, by encoding the Local Byte Enables (LBE[3:0]#), as defined in Table 9-5.

Table 9-5.   Direct Slave Byte Enables – C and J Modes Only

Bus Width	Local Bus Mode	
	C	J
32 bit	The four Byte Enables indicate which of the four bytes are valid during a Data cycle: • LBE3# Byte Enable 3 – LD[31:24] • LBE2# Byte Enable 2 – LD[23:16] • LBE1# Byte Enable 1 – LD[15:8] • LBE0# Byte Enable 0 – LD[7:0]	The four Byte Enables indicate which of the four bytes are valid during a Data cycle: • LBE3# Byte Enable 3 – LAD[31:24] • LBE2# Byte Enable 2 – LAD[23:16] • LBE1# Byte Enable 1 – LAD[15:8] • LBE0# Byte Enable 0 – LAD[7:0]
16 bit	LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: • LBE3# Byte High Enable (BHE#) – LD[15:8] • LBE2# *not used* • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) – LD[7:0]	LBE[3, 1:0]# are encoded to provide BHE#, LA1, and BLE#, respectively: • LBE3# Byte High Enable (BHE#) – LAD[15:8] • LBE2# *not used* • LBE1# Address bit 1 (LA1) • LBE0# Byte Low Enable (BLE#) – LAD[7:0]
8 bit	LBE[1:0]# are encoded to provide LA[1:0], respectively: • LBE3# *not used* • LBE2# *not used* • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0)	LBE[1:0]# are encoded to provide LA[1:0], respectively: • LBE3# *not used* • LBE2# *not used* • LBE1# Address bit 1 (LA1) • LBE0# Address bit 0 (LA0)

9.3.10.5   Direct Slave Transfer Size – M Mode Only

The TSIZ[0:1] balls correspond to the Data Transfer size on the Local Bus, as defined in Table 9-6 and Table 9-7.

Table 9-6.   Data Bus TSIZ[0:1] Contents for Single Write Cycles – M Mode Only

Transfer Size	TSIZ[0:1]		Address		32-Bit Port Size				16-Bit Port Size		8-Bit Port Size
			LA30	LA31	LD[0:7]	LD[8:15]	LD[16:23]	LD[24:31]	LD[0:7]	LD[8:15]	LD[0:7]
Byte	0	1	0	0	OP0	–	–	–	OP0	–	OP0
	0	1	0	1	–	OP1	–	–	–	OP1	OP1
	0	1	1	0	–	–	OP2	–	OP2	–	OP2
	0	1	1	1	–	–	–	OP3	–	OP3	OP3
Word	1	0	0	0	OP0	OP1	–	–	OP0	OP1	–
	1	0	1	0	–	–	OP2	OP3	OP2	OP3	–
Dword	0	0	0	0	OP0	OP1	OP2	OP3	–	–	–

*Note: The "–" symbol indicates that a byte is **not** required to be delivered during that Write cycle.
However, the PEX 8311 drives these byte lanes, although the data is not used.*

Table 9-7.   Data Bus TSIZ[0:1] Requirements for Single Read Cycles – M Mode Only

Transfer Size	TSIZ[0:1]		Address		32-Bit Port Size				16-Bit Port Size		8-Bit Port Size
			LA30	LA31	LD[0:7]	LD[8:15]	LD[16:23]	LD[24:31]	LD[0:7]	LD[8:15]	LD[0:7]
Byte	0	1	0	0	OP0	–	–	–	OP0	–	OP0
	0	1	0	1	–	OP1	–	–	–	OP1	OP1
	0	1	1	0	–	–	OP2	–	OP2	–	OP2
	0	1	1	1	–	–	–	OP3	–	OP3	OP3
Word	1	0	0	0	OP0	OP1	–	–	OP0	OP1	–
	1	0	1	0	–	–	OP2	OP3	OP2	OP3	–
Dword	0	0	0	0	OP0	OP1	OP2	OP3	–	–	–

*Note: The "–" symbol indicates that a valid byte is **not** required during that Read cycle.
However, the PEX 8311 drives these byte lanes, although the data is not used.*

9.3.11   Direct Slave Priority

9.3.11.1   Direct Slave Priority – C and J Modes

Direct Slave accesses on the Local Bus have a higher priority than DMA accesses, thereby preempting DMA transfers. During a DMA transfer, when the PEX 8311 detects a pending Direct Slave access (PCI Express Posted Write request), it releases the Local Bus. The PEX 8311 resumes the DMA operation after the Direct Slave access completes on the Local Bus.

When the PEX 8311 DMA Controller owns the Local Bus, its LHOLD output and LHOLDA input are asserted. When a Direct Slave access occurs, the PEX 8311 releases the Local Bus by de-asserting LHOLD and floating the Local Bus outputs. After the PEX 8311 senses that LHOLDA is de-asserted, it requests the Local Bus for a Direct Slave transfer by asserting LHOLD. When the PEX 8311 receives LHOLDA, it performs the Direct Slave transfer. After completing a Direct Slave transfer, the PEX 8311 releases the Local Bus by de-asserting LHOLD and floating the Local Bus outputs. After the PEX 8311 senses that LHOLDA is de-asserted and the Local Bus Pause Timer Counter is zero (**LCS_MARBR**[15:8]=0h) or disabled (**LCS_MARBR**[17]=0), it requests the Local Bus to complete the DMA transfer by re-asserting LHOLD. When the PEX 8311 receives LHOLDA and LHOLD=1, it drives the bus and continues the DMA transfer.

9.3.11.2   Direct Slave Priority – M Mode

Direct Slave accesses have a higher priority than DMA accesses, thereby preempting DMA transfers. During a DMA transfer, if the PEX 8311 detects a pending Direct Slave access, it releases the Local Bus. The PEX 8311 resumes DMA operation after the Direct Slave access completes.

When the PEX 8311 DMA Controller(s) owns the Local Bus, its BR# output and BG# input are asserted. When a Direct Slave access occurs, the PEX 8311 releases the Local Bus by de-asserting BB# and floating the Local Bus outputs. After the PEX 8311 senses that BG# is de-asserted, it requests the Local Bus for a Direct Slave transfer by asserting BR#. When the PEX 8311 receives BG#, and BB# is de-asserted, it drives the bus and performs the Direct Slave transfer. To complete the Direct Slave transfer, the PEX 8311 releases the Local Bus by de-asserting BB# and floating the Local Bus outputs. After the PEX 8311 senses that BG# is de-asserted and the Local Bus Pause Timer Counter is zero (**LCS_MARBR**[15:8]=00h) or disabled (**LCS_MARBR**[17]=0), it requests a DMA transfer from the Local Bus by re-asserting BR#. When the PEX 8311 senses that BG# is asserted and BB# is de-asserted, it drives the bus and continues the DMA transfer.

9.3.12 Local Bus Direct Slave Data Transfer Modes

9.3.12.1 Local Bus Direct Slave Data Transfer Modes – C and J Modes

The PEX 8311 supports C and J modes with three Local Bus Data Transfer modes:

- Single Cycle – Default data transfer mode
- Burst-4 – Compatible with C and J modes
- Continuous Burst – Provides the highest throughput

Table 9-8 summarizes the register settings used to select Local Bus Data Transfer modes. It also indicates the data quantity transferred per Address Cycle (ADS#).

Notes: *The BTERM#/BI# ball is referred to as the BTERM# ball in C and J modes, and as the BI# ball in M mode.*

*The BTERM# Input Enable bits (**LCS_LBRD0**[7] for Space 0, **LCS_LBRD1**[7] for Space 1, and/or **LCS_LBRD0**[23] for Expansion ROM) function as BI Mode bits in M mode.*

The term Burst Forever *was formerly used to describe* Continuous Burst.

Table 9-8. Local Bus Data Transfer Modes – C and J Modes

Local Bus Data Transfer Modes	Burst Enable Bit	BTERM# Input Enable Bit	Result
Single Cycle (default)	0	X	One ADS# per data.
Burst-4	1	0	One ADS# per four Data cycles (recommended for i960 and PPC401).
Continuous Burst	1	1	One ADS# per data burst or until BTERM# is asserted.

Note: "X" is "Don't Care."

9.3.12.2   Local Bus Direct Slave Data Transfer Modes – M Mode

The PEX 8311 supports M mode with three Local Bus Data Transfer modes:

- Single Cycle – Default data transfer mode
- Burst-4 – Compatible with M mode (MPC850- and MPC860)
- Continuous Burst – Provides the highest throughput

Table 9-8 summarizes the register settings used to select Local Bus Data Transfer modes. It also indicates the data quantity transferred per Address Cycle (TS#).

Notes: *The BTERM#/BI# ball is referred to as the BTERM# ball in C and J modes, and as the BI# ball in M mode.*

The BTERM# Input Enable bits (LCS_LBRD0[7] for Space 0, LCS_LBRD1[7] for Space 1, and/or LCS_LBRD0[23] for Expansion ROM) function as BI Mode bits in M mode.

The term Burst Forever *was formerly used to describe* Continuous Burst.

Table 9-9.   Local Bus Data Transfer Modes – M Mode

Local Bus Data Transfer Modes	Burst Enable Bit	BI Mode Bit	Result
Single Cycle (default)	0	X	One TS# per data.
Burst-4	1	0	One TS# per 16 bytes (recommended for MPC850 or MPC860).
Continuous Burst	1	1	One TS# per data burst or until BI# is asserted.

Note: "X" is "Don't Care."

9.3.12.3   Single Cycle Mode

9.3.12.3.1   Single Cycle Mode – C and J Modes

Single Cycle mode is the default Data Transfer mode. In Single Cycle mode, the PEX 8311 issues one ADS# per Data cycle. The starting address for a single cycle Data transfer resides on any address.

For single cycle Data transfers, Burst mode is disabled (**LCS_LBRD0**[24]=0 for Space 0, **LCS_LBRD1**[8]=0 for Space 1, and/or **LCS_LBRD0**[26]=0 for Expansion ROM). For a 32-bit Local Bus, when a starting address in a Direct Slave transfer is *not* aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary.

9.3.12.3.2   Single Cycle Mode – M Mode

Single Cycle mode is the default Data Transfer mode. In Single Cycle mode, the PEX 8311 issues one TS# per Data cycle. The starting address for a single cycle Data transfer resides on any address. If a starting address in a Direct Slave PCI Express-to-Local transfer is *not* aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next 4-Dword boundary.

For single cycle Data transfers, Burst mode is disabled (**LCS_LBRD0**[24]=0 for Space 0, **LCS_LBRD1**[8]=0 for Space 1, and/or **LCS_LBRD0**[26]=0 for Expansion ROM). For a 32-bit Local Bus, when a starting address in a Direct Slave transfer is *not* aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary.

9.3.12.3.3   Partial Data Accesses

Partial Data accesses (not all Byte Enables are asserted) are broken into single cycles. When there is remaining data that is *not* Dword-aligned during the transfer, it results in a single cycle Data transfer.

9.3.12.4   Burst-4 Mode

Burst-4 mode forces the PEX 8311 to perform Data transfers as bursts of four Data cycles (4 Dwords, four 16-bit words, or 4 bytes to a 32-, 16-, or 8-bit bus, respectively).

9.3.12.4.1   Burst-4 Mode – C and J Modes

Burst-4 mode Data transfers are set up by enabling bursting and clearing the *BTERM# Input Enable* bit for the affected Local Address space (**LCS_LBRD0** [24, 7]=10b for Space 0, **LCS_LBRD1**[8:7]=10b for Space 1, and/or **LCS_LBRD0**[26, 23]=10b for Expansion ROM, respectively).

Burst-4 mode bursting starts on any data boundary and bursts to the next four-data boundary. The first burst starts on any address and moves to the data boundary. The next bursts are four Data cycles. The first or last burst can be less than four Data cycles. The PEX 8311 can continue to burst by asserting ADS# and performing another burst. For a 32-bit Local Bus, when a starting address in a Direct Slave transfer is *not* aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary. (Refer to Table 9-10.)

Table 9-10.   Burst-4 Mode – C, J, and M Modes

Local Bus Data Width	Burst-4
32 bit	4 Dwords start/stop at a 4-Dword boundary
16 bit	4 words start/stop at a 4-word boundary
8 bit	4 bytes start/stop at a 4-byte boundary

Note: The first or last burst can be less than four Data cycles.

9.3.12.4.2   Burst-4 Mode – M Mode

Burst-4 mode Data transfers are set up by enabling bursting and clearing the *BI Mode* bit for the affected Local Address space (**LCS_LBRD0**[24, 7]=10b for Space 0, **LCS_LBRD1**[8:7]=10b for Space 1, and/or **LCS_LBRD0**[26, 23]=10b for Expansion ROM, respectively).

Burst-4 mode bursting starts on any data boundary and bursts to the next four-data boundary. The first burst starts on any address and moves to the data boundary. The next bursts are four Data cycles. The first or last burst can be less than four Data cycles. The PEX 8311 can continue to burst by asserting TS# and performing another burst. For a 32-bit Local Bus, when a starting address in a Direct Slave transfer is *not* aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary. (Refer to Table 9-10.)

9.3.12.4.3   Partial Data (<4 Bytes) Accesses

Partial Data accesses occur when either the first, last, or both PCI Express data are unaligned, Byte Enable Field are *not* all asserted. For a 32-bit Local Bus, they are broken in single cycles until the next Dword boundary.

9.3.12.5   Continuous Burst Mode

Continuous Burst mode enables the PEX 8311 to perform data bursts of longer than four Data cycles. However, special external interface devices are required that can accept bursts longer than four Data cycles.

9.3.12.5.1   Continuous Burst Mode – C and J Modes

Continuous Burst mode Data transfers are set up by enabling, bursting, and setting the *BTERM# Input Enable* bit for the affected Local Address space (**LCS_LBRD0**[24, 7]=11b for Space 0, **LCS_LBRD1**[8:7]=11b for Space 1, and/or **LCS_LBRD0**[26, 23]=11b for Expansion ROM, respectively).

The PEX 8311 asserts one ADS# cycle and continues to burst data. If a Slave device requires a new Address cycle (ADS#), it can assert the BTERM# input. The PEX 8311 completes the current Data transfer and stops the burst. The PEX 8311 continues the transfer by asserting ADS# and starting a new burst at the next address.

9.3.12.5.2   Continuous Burst Mode – M Mode

Continuous Burst mode Data transfers are set up by enabling, bursting, and setting the *BI Mode* bit for the affected Local Address space (**LCS_LBRD0**[24, 7]=11b for Space 0, **LCS_LBRD1**[8:7]=11b for Space 1, and/or **LCS_LBRD0** [26, 23]=11b for Expansion ROM, respectively).

The PEX 8311 asserts one TS# cycle and continues to burst data. If a Slave device requires a new Address cycle (TS#), it can assert the BI# input. The PEX 8311 completes the current Data transfer and stops the burst. The PEX 8311 continues the transfer by asserting TS# and starting a new burst at the next address.

9.3.13   Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Express Transaction Initiator or PEX 8311 DMA Controller are written.

9.3.14   Local Bus Read Accesses

For Single Cycle Local Bus Read accesses, when the PEX 8311 is the Local Bus Master, the PEX 8311 reads only bytes corresponding to Byte Enables requested by the PCI Express Read Request Initiator. For Burst Read cycles, the PEX 8311 passes all bytes and is programmed to:

- Prefetch

- Perform Direct Slave Read Ahead mode

- Generate internal wait states

- Enable external wait control (READY# input)

- Enable type of Burst mode to perform

9.3.15   Direct Slave Accesses to 8- or 16-Bit Local Bus

9.3.15.1   Direct Slave Accesses to 8- or 16-Bit Local Bus – C Mode

PCI Express access to an 8- or 16-bit Local Bus results in the Local Data being broken into multiple Local Bus width transfers. For each transfer, Byte Enables LBE[1:0]# are encoded to provide Local Address bits LA[1:0].

9.3.15.2   Direct Slave Accesses to 8- or 16-Bit Local Bus – J Mode

PCI Express access to an 8- or 16-bit Local Bus results in the Local Data being broken into multiple Local Bus width transfers. For each transfer, Byte Enables LBE[1:0]# are encoded to provide Local Address bits LA[1:0]. LAD[1:0] also provide these Address bits during the Address phase.

9.3.15.3   Direct Slave Accesses to 8- or 16-Bit Local Bus – M Mode

PCI Express access to an 8- or 16-bit Local Bus results in the PCI Bus Dword being broken into multiple Local Bus transfers. For each transfer, Byte Enables are encoded to provide Transfer Size bits TSIZ[0:1].

9.3.16   Local Bus Data Parity

Generation or use of Local Bus Data parity is optional. The Local Bus Parity Check is passive and provides only parity information to the Local processor during Direct Master and Direct Slave transfers.

9.3.16.1   Local Bus Data Parity – C and J Modes

There is one Data parity ball for each byte lane of the PEX 8311 data bus (DP[3:0]). "Even data parity" is asserted for each lane during Local Bus Reads from the PEX 8311 and during PEX 8311 Master Writes to the Local Bus.

Even Data parity is checked for Direct Master Writes and Direct Slave Reads. If an error is detected, the PEX 8311 sets the *Direct Master Write/Direct Slave Read Local Data Parity Check Error Status* bit (**LCS_INTCSR**[7]=1) and generates an interrupt (LSERR#), when enabled (**LCS_INTCSR**[0, 6]=11b, respectively). This occurs in the Clock cycle following the data being checked.

For applications in which READY# is disabled in the PEX 8311 registers, READY# requires an external pull-down resistor, to allow **LCS_INTCSR**[7] to be set and the LSERR# interrupt to be asserted.

9.3.16.2   Local Bus Data Parity – M Mode

There is one Data parity ball for each byte lane of the PEX 8311 data bus (DP[0:3]). "Even data parity" is asserted for each lane during Local Bus Reads from the PEX 8311 and during PEX 8311 Master Writes to the Local Bus.

Even Data parity is checked for Direct Master Writes and Direct Slave Reads. If an error is detected, the PEX 8311 sets the *Direct Master Write/Direct Slave Read Local Data Parity Check Error Status* bit (**LCS_INTCSR**[7]=1) and generates an interrupt (LINTo#), when enabled (**LCS_INTCSR**[0, 6]=11b, respectively). This occurs in the Clock cycle following the data being checked.

For applications in which TA# is disabled in the PEX 8311 registers, TA# requires an external pull-down resistor, to allow **LCS_INTCSR**[7] to be set and the LINTo# interrupt to be asserted.

9.4   Deadlock Conditions

A deadlock can occur within the PEX 8311 when a PCI Express Address space must access the PEX 8311 Local Bus at the same time a Master on the PEX 8311 Local Bus must access the PCI Express Address space to transfer data to the PCI Express interface. This type of deadlock is a *Partial Deadlock*.

Note: *Full deadlock is impossible to encounter in the PEX 8311 bridge with PCI Express Ingress/*
           Egress direction, as well as the internal PCI Bus between PCI Express Address and
           Local space architecture.

Partial deadlock occurs when the PCI Express device tries to access the PEX 8311 Local Bus concurrently with the PEX 8311 Local Master trying to access the PCI Express device Local Bus. This applies only to Direct Master and Direct Slave accesses through the PEX 8311. Deadlock does ***not*** occur in transfers through the PEX 8311 DMA Channels or registers (*such as*, **Mailboxes**).

For partial deadlock, accesses by the PCI Express Address spaces to the Local Spaces times out (*Direct Slave Retry Delay Clocks*, **LCS_LBRD0**[31:28]) and the PEX 8311 responds with an internal Retry. This allows the Direct Master to complete and free up the Local Bus. Possible solutions are described in the following sections for cases in which internal timeout is undesirable, and back off the Local Bus Master is used to resolve deadlock conditions.

9.4.1   Backoff

9.4.1.1   Backoff – C and J Modes

The backoff sequence is used to break a deadlocked condition. The PEX 8311 BREQo signal indicates that a deadlock condition has occurred.

The PEX 8311 starts the Backoff Timer (refer to the **LCS_EROMBA** register for further details) when it detects the following conditions:

- PCI Express Address space is attempting to access memory or an I/O device on the Local Bus through the Local Address space and is not gaining access (*for example*, LHOLDA is not received).

- Local Bus Master is performing a Direct Bus Master Read access to the PCI Express Address space to generate a TLP Read request on the PCI Express interface. Or, a Local Bus Master is performing a Direct Bus Master Write access to the PCI Express Address space to generate a TLP Write request on the PCI Express interface and the PEX 8311 Direct Master Write FIFO cannot accept another Write cycle.

When Local Bus Backoff is enabled (**LCS_EROMBA**[4]=1), the Backoff Timer expires, and the PEX 8311 has not received LHOLDA, the PEX 8311 asserts BREQo. External bus logic can use BREQo to perform Backoff.

The Backoff cycle is device/bus architecture dependent. External logic (an Arbiter) can assert the necessary signals to cause a Local Bus Master to release a Local Bus (backoff). After the Local Bus Master backs off, it can grant the bus to the PEX 8311 by asserting LHOLDA.

After BREQo is asserted, READY# for the current Data cycle is never asserted (the Local Bus Master must perform backoff). When the PEX 8311 detects LHOLDA asserted, it proceeds with the PCI Express-to-Local Bus access. When this access completes and the PEX 8311 releases the Local Bus, external logic can release the backoff and the Local Bus Master can resume the cycle interrupted by the Backoff cycle. The PEX 8311 Direct Master Write FIFO retains accepted data (*that is*, the last data for which READY# was asserted).

After the backoff condition ends, the Local Bus Master restarts the last cycle with ADS#. Ensure that for Writes, data following ADS# is data the PEX 8311 did not acknowledge prior to the Backoff cycle (*for example*, the last data for which READY# is not asserted).

For Direct Master Read cycles (the PEX 8311 generated PCI Express TLP Read request), when the PEX 8311 is able to receive a Read Completion as the Local Bus Master that initiated the Direct Master Read cycle is backed off, the Local Bus Master receives that data when the Local Master restarts the same last cycle (data is *not* read twice). The PEX 8311 is *not* allowed to perform a new Read.

9.4.1.2   Backoff – M Mode

The backoff sequence is used to break a deadlocked condition. The PEX 8311 RETRY# signal indicates that a deadlock condition has occurred.

The PEX 8311 starts the Backoff Timer (refer to the **LCS_EROMBA** register for further details) when it detects the following conditions:

- PCI Express Address space is attempting to access memory or an I/O device on the Local Bus through the Local Address space and is not gaining access (*for example*, BG# is not received).
- Local Bus Master is performing a Direct Bus Master Read access to the PCI Express Address space to generate a TLP Read request on the PCI Express interface. Or, a Local Bus Master is performing a Direct Bus Master Write access to the PCI Express Address space to generate a TLP Write request on the PCI Express interface and the PEX 8311 Direct Master Write FIFO cannot accept another Write cycle.

When Local Bus Backoff is enabled (**LCS_EROMBA**[4]=1), the Backoff Timer expires, and the PEX 8311 has not received BG#, the PEX 8311 asserts RETRY#. External bus logic can use RETRY# to perform Backoff.

The Backoff cycle is device/bus architecture dependent. External logic (an Arbiter) can assert the necessary signals to cause a Local Bus Master to release a Local Bus (backoff). After the Local Bus Master backs off, it can grant the bus to the PEX 8311 by asserting BG#.

After RETRY# is asserted, TA# for the current Data cycle is never asserted (the Local Bus Master must perform backoff). When the PEX 8311 detects BG# asserted, it proceeds with the PCI Express-to-Local Bus access. When this access completes and the PEX 8311 releases the Local Bus, external logic can release the backoff and the Local Bus Master can resume the cycle interrupted by the Backoff cycle. The PEX 8311 Direct Master Write FIFO retains accepted data (*that is*, the last data for which TA# was asserted).

After the backoff condition ends, the Local Bus Master restarts the last cycle with TS#. Ensure that for Writes, data following TS# is data the PEX 8311 did not acknowledge prior to the Backoff cycle (*for example*, the last data for which READY# is not asserted).

For Direct Master Read cycles (the PEX 8311 generated PCI Express TLP Read request), when the PEX 8311 is able to receive a Read Completion as the Local Bus Master that initiated the Direct Master Read cycle is backed off, the Local Bus Master receives that data when the Local Master restarts the same last cycle (data is *not* read twice). The PEX 8311 is *not* allowed to perform a new Read.

9.4.1.3   Software/Hardware Solution for Systems without Backoff Capability

For adapters that do not support Backoff, a possible deadlock solution is as follows.

PCI Express Root Complex software/driver, external Local Bus hardware, general-purpose output USERo and input USERi are used to prevent deadlock. USERo (or a GPIO configured as an output) is asserted to request that the external Local Bus Arbiter not grant the bus to any Local Bus Master except the PEX 8311. Status output from the Local Bus Arbiter is connected to USERi (or a GPIO configured as an input) to indicate that no Local Bus Master owns the Local Bus, allowing the PCI Express transaction-initiating device to determine that no Local Bus Master that currently owns the Local Bus can read input. The PCI Express transaction initiating device can then perform Direct Slave access (PCI Express-to-Local Bus Write/Read request). When the PCI Express device finishes, it de-asserts USERo.

9.4.1.4   Preempt Solution

For devices that support preempt, USERo can be used to preempt the current Local Bus Master device. When USERo is asserted, the current Local Bus Master device completes its current cycle and releases the Local Bus, de-asserting LHOLD (C or J mode) or BB# (M mode).

9.4.1.5   Software Solutions to Deadlock

Both PCI Express and Local Bus software can use a combination of **Mailbox** registers, **Doorbell** registers, interrupts, Direct Local-to-PCI Express accesses, and Direct PCI Express-to-Local accesses to avoid deadlock.

9.5   DMA Operation

The PEX 8311 supports two independent DMA channels – Channel 0 and Channel 1 – capable of transferring data from PCI Express-to-Local and Local-to-PCI Express.

Each channel consists of a DMA Controller and a dedicated bi-directional FIFO. Both channels support Block DMA, Scatter/Gather, and Demand Mode transfers, with or without End of Transfer (EOT#). Master mode must be enabled for both the Local Address spaces and PCI Express Address spaces (**LCS_PCICR**[2]=1) before the PEX 8311 starts generating TLPs on the PCI Express interface. In addition, DMA Channel 0 and Channel 1 are programmed to:

- Operate with 8-, 16-, or 32-bit Local Bus data widths
- Use 0 to 15 internal wait states (Local Bus)
- Enable/disable external wait states (Local Bus)
- Enable/disable Local Bus burst capability
- Set Local Burst mode (refer to Table 9-11, Table 9-12, and Section 9.5.19)
- Hold Local address constant (Local Slave is FIFO) or incremented
- Internally perform Memory Write and Invalidate (Command Code = Fh) or normal Memory Write (Command Code = 7h) to PCI Express Address spaces
- Stop/pause Local transfer with or without BLAST# (C or J mode) or BDIP# (M mode) (DMA Fast/Slow Terminate mode)
- Operate in DMA Clear Count mode

The Local Bus Latency Timer (**LCS_MARBR**[7:0]) determines the number of Local clocks the PEX 8311 can burst data before relinquishing Local Bus ownership. The Local Pause Timer (**LCS_MARBR**[15:8]) sets how soon (after the Latency Timer times out) the DMA channel can re-request the Local Bus.

Table 9-11.   DMA Local Burst Modes – C and J Modes

Mode	Burst Enable Bit	*BTERM#* Input Enable Bit	Result
Single Cycle (default)	Disabled (0)	X	Single cycle (default Local Burst mode)
Burst-4	Enabled (1)	Disabled (0)	Burst up to four Data cycles
Continuous Burst	Enabled (1)	Enabled (1)	Continuous Burst (terminate when BTERM# is asserted or transfer is complete)

Table 9-12.   DMA Local Burst Modes – M Mode

Mode	Burst Enable Bit	BI Mode Bit	Result
Single Cycle (default)	Disabled (0)	X	One TS# per data
Burst-4	Enabled (1)	Disabled (0)	One TS# per 16 bytes (recommended for MPC850 or MPC860)
Continuous Burst	Enabled (1)	Enabled (1)	One TS# per data burst or until BI# is asserted

Note: "X" is "Don't Care.

9.5.1   Dual Address Cycles

9.5.1.1   Dual Address Cycles – C and J Modes

The PEX 8311 supports generating internal PCI Express Dual Address Cycles (DAC) to the PCI Express Prefetchable Address space with the upper 32-bit register for the affected DMA channel (**LCS_DMADAC0/1**), which is then translated to TLP Long Address format generation on the PCI Express interface, to access devices located above the 4-GB Address Boundary space.

9.5.1.2   Dual Address Cycles – M Mode

The PEX 8311 supports PCI Express Dual Address Cycles (DAC) with the upper 32-bit register(s) for the affected DMA channel (**LCS_DMADAC0/1**). The PEX 8311 suppresses all dummy cycles on the PCI Express interface and Local Bus.

The PEX 8311 supports PCI Express Dual Address Cycles (DAC) when it is a PCI Bus Master using the **LCS_DMADAC0/1** register(s) for Block DMA transactions. Scatter/Gather DMA can use the DAC function by way of the **LCS_DMADAC0/1** register(s) or **LCS_DMAMODE0/1**[18]. The DAC command is used to transfer a 64-bit address to devices that support 64-bit addressing when the address is above the 4-GB Address Boundary space. The PEX 8311 performs a DAC within two PCI clock periods, when the first PCI address is a Lo-Addr, with the command (C/BE[3:0]#) "Dh", and the second PCI address is a Hi-Addr, with the command (C/BE[3:0]#) "6h" or "7h", depending upon whether it is a PCI Read or PCI Write cycle. (Refer to Figure 9-14.)

Figure 9-14.   Internal PCI Bus Dual Address Cycle Timing
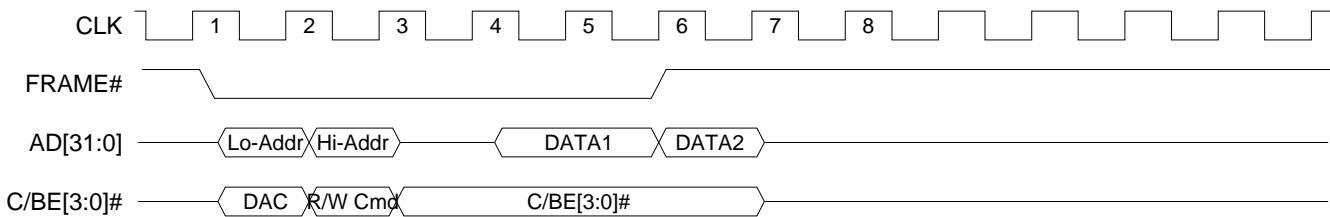
9.5.2   Master Command Codes

The PEX 8311 becomes an internal PCI Bus Master to perform DMA transfers. The internal PCI Command Code used by the PEX 8311 during DMA transfers is specified by the value(s) contained in the **LCS_CNTRL**[15:0] register bits. To operate in Memory Write and Invalidate (MWI) mode, set the following **LCS** registers – **LCS_PCICR**[4]=1; **LCS_DMAMODE0/1**[13]=1; **LCS_PCICLSR**[7:0] = Cache Line Size of 8 or 16 Dwords. In MWI mode for DMA Local-to-PCI Express transfers, when the starting address alignment is aligned with the Cache Line Size and upon determining it can transfer at least one Cache Line of data, the PEX 8311 uses an internal PCI Command Code of Fh, regardless of the **LCS_CNTRL**[15:0] bit values.

For DMA Local-to-PCI Express accesses, the PEX 8311 uses the internal commands defined in Table 9-13.

Table 9-13.   Internal PCI Command Codes for DMA-to-PCI Express Memory I/O-Mapped and/or Prefetchable Memory Address Spaces Accesses

Command Type	Code (C/BE[3:0]#)
Memory Read	0110b (6h)
Memory Write	0111b (7h)
Memory Read Multiple	1100b (Ch)
Dual Address Cycle	1101b (Dh)
Memory Read Line	1110b (Eh)
Memory Write and Invalidate	1111b (Fh)

*Note: DMA can only perform Memory accesses. DMA **cannot** perform I/O nor Configuration accesses.*

9.5.3   DMA PCI Express Long Address Format

The PEX 8311 supports Long Address Format generation, for 64-bit addressing to access devices located above the 4-GB Address Boundary space by utilizing DMA Dual Address Cycle (DAC) register (**LCS_DMADAC0/1**) for DMA Block Mode transactions. DMA Scatter/Gather mode can use the DAC function by way of the **LCS_DMADAC0/1** register or **LCS_DMAMODE0/1**[18] register for the affected DMA channel. The DMA space must be mapped to PCI Express Prefetchable space and **LCS_DMADAC0/1**, and/or **LCS_DMAMODE0/1**[18], register for the affected DMA channel must be programmed to a non-zero value and enabled, respectively, for 64-bit addressing to occur on the PCI Express interface. (Refer to Section 8.5.3, "64-Bit Addressing," for further details.) When the **LCS_DMADAC0/1** register for the affected DMA channel has a value of 0h (feature enabled when **LCS_DMADAC0/1** register value is ***not*** 0h), the PEX 8311 performs a Short Address Format on the PCI Express interface.

9.5.4   DMA Block Mode

The PCI Express device or Local processor sets the DMA PCI and Local starting addresses, Transfer Byte Count, and transfer direction. The PCI Express device or Local processor then sets the *DMA Channel Start* and *Enable* bits (**LCS_DMACSR0/1**[1:0]=11b) to initiate a transfer. The PEX 8311 internally accesses PCI Express Address spaces to generate a TLP on the PCI Express interface and Local Bus, and transfers data. After the transfer completes, the PEX 8311 sets the *Channel Done* bit for the affected DMA channel (**LCS_DMACSR0/1**[4]=1), and can assert an interrupt(s) (**LCS_INTCSR**[16 and/or 8] and/or **LCS_DMAMODE0/1**[17 and/or 10]) to the Local processor or the PCI Express interface (programmable). The *Channel Done* bit for the affected DMA channel can be polled, instead of interrupt generation, to indicate DMA transfer status.

DMA registers are accessible from the PCI Express interface and Local Bus. (Refer to Figure 9-15.)

Figure 9-15.   DMA Block Mode Initialization (Single Address or Dual Address PCI)
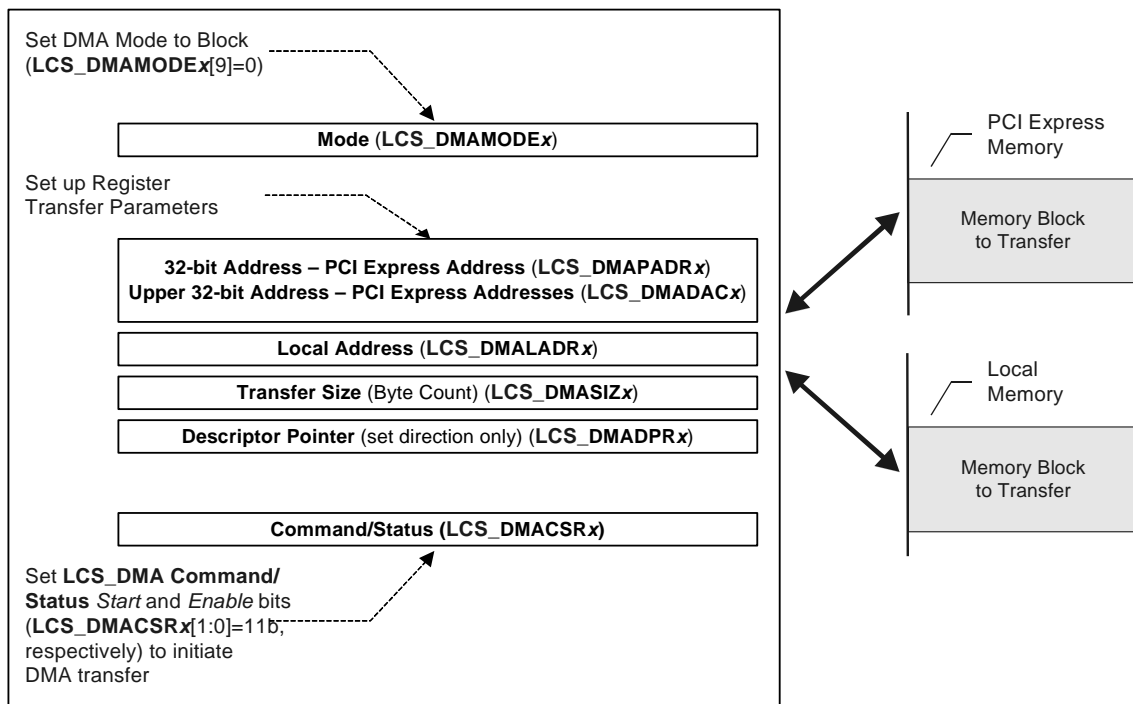
During DMA transfers, the PEX 8311 is the transaction Initiator (generates TLP) on the PCI Express interface and Master on the Local Bus. For simultaneous access, Direct Slave or Direct Master has a higher priority than DMA.

The DMA Controller releases the internal PCI Bus when one of the following conditions occur (refer to Figure 9-16 through Figure 9-19):

- Local DMA FIFO is full (PCI Express-to-Local)
- Local DMA FIFO is empty (Local-to-PCI Express)
- Terminal Count is reached
- PCI Bus Latency Timer expires (**LCS_PCILTR**[7:0]) – normally programmed by the System BIOS according to the **PCI Maximum Latency** (**LCS_PCIMLR**) register value
- PCI Express bridge issues a Disconnect to the DMA Controller

The PEX 8311 releases the Local Bus, when one of the following conditions occur:

- Local DMA FIFO is empty (PCI Express-to-Local)
- Local DMA FIFO is full (Local-to-PCI Express)
- Terminal Count is reached
- Local Bus Latency Timer is enabled (**LCS_MARBR**[16]=1) and expires (**LCS_MARBR**[7:0])
- Direct Slave (PCI Express-to-Local Read/Write) request is pending
- BREQi is asserted (C or J mode only)

Figure 9-16. DMA, PCI Express-to-Local Bus – M Mode
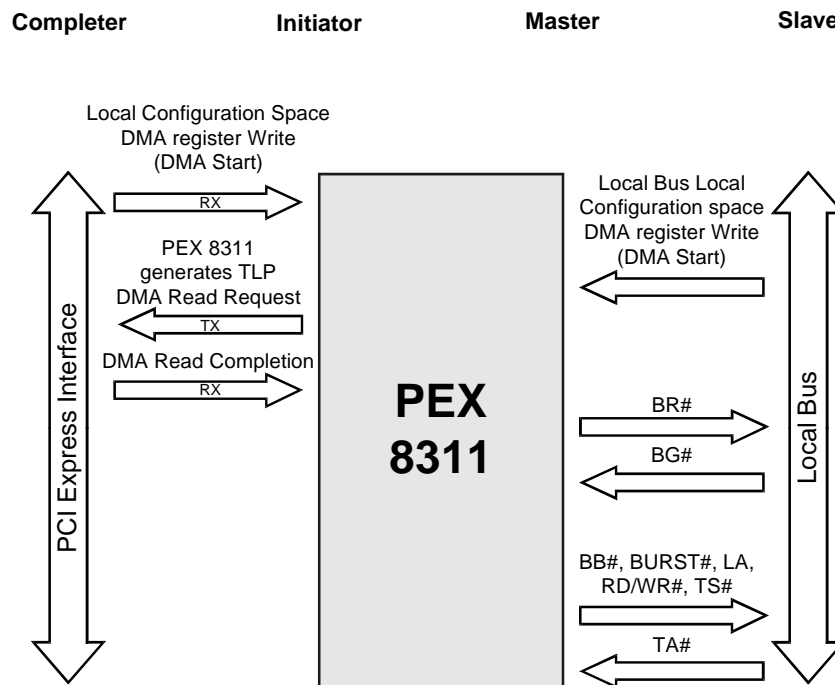
Figure 9-17.   DMA, Local-to-PCI Express – M Mode
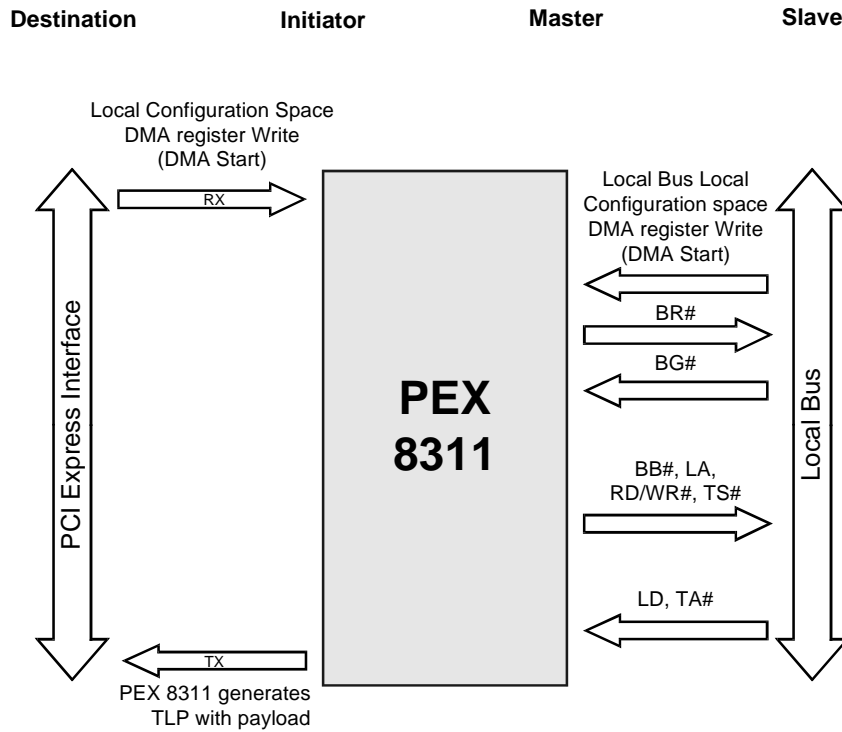
Note: Figure 9-16 and Figure 9-17 represent a sequence of Bus cycles.

Figure 9-18.   DMA, PCI Express-to-Local Bus – C and J Modes
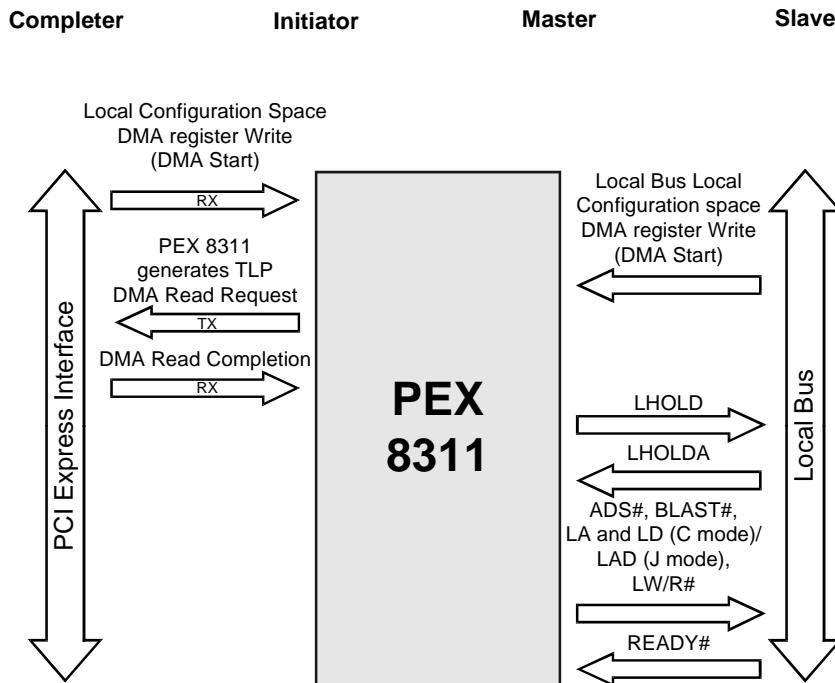
Figure 9-19.   DMA, Local-to-PCI Express – C and J Modes
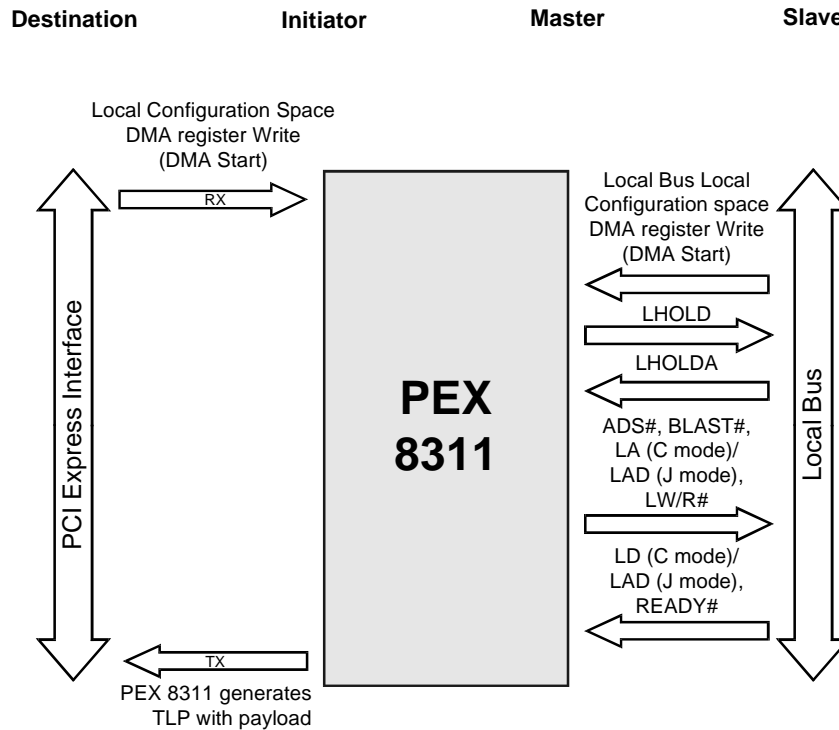
Note: Figure 9-18 and Figure 9-19 represent a sequence of Bus cycles.

9.5.4.1   DMA Block Mode PCI Express Dual Address Cycles

The PEX 8311 supports generation of PCI Express TLP Long Address format (64-bit address) to access devices located above the 4-GB Address Boundary space. The DMA Local Space must be internally mapped to PCI Express Prefetch Address space for 64-bit addresses to generate in DMA Block mode. When the **LCS_DMADAC0/1** register for the affected DMA channel has a value of 0h, the PEX 8311 generates PCI Express TLP Short Address format (32-bit address). Other values cause a Dual Address Cycle to internally generate between DMA Local Space and PCI Express Prefetchable Address space, causing the PCI Express TLP Long Address format to generate on the PCI Express interface.

The PEX 8311 supports the DAC feature in DMA Block mode. When the **LCS_DMADAC0/1** register(s) contains a value of 0h, the PEX 8311 performs a Single Address Cycle (SAC) on the PCI Bus. Any other value causes a Dual Address to appear on the PCI Bus. (Refer to Figure 9-14.)

9.5.5   DMA Scatter/Gather Mode

In DMA Scatter/Gather mode, the PCI Express device or Local processor sets up descriptor blocks in PCI Express or Local memory composed of PCI and Local addresses, Terminal Count, transfer direction, and address of the next descriptor block. (Refer to Figure 9-20 and Figure 9-21.) The PCI Express device or Local processor then:

- Enables DMA Scatter/Gather mode for the affected DMA channel
  (**LCS_DMAMODE0/1**[9]=1)

- Sets up the Initial Descriptor Block address in the **Descriptor Pointer** register for the affected DMA channel (**LCS_DMADPR0/1**)

- Initiates the transfer by setting a control bit for the affected DMA channel
  (**LCS_DMACSR0/1**[1:0]=11b)

The PEX 8311 supports zero wait state Descriptor Block bursts from the Local Bus when the *Local Burst Enable* bit for the affected DMA channel is enabled (**LCS_DMAMODE0/1**[8]=1).

The PEX 8311 loads the first descriptor block and initiates the Data transfer. The PEX 8311 continues to load descriptor blocks and transfer data until it detects that the *End of Chain* bit for the affected DMA channel is set (**LCS_DMADPR0/1**[1]=1). After it detects that the bit is set, the PEX 8311 completes the current descriptor block, sets the *DMA Done* bit for the affected DMA channel (**LCS_DMACSR0/1**[4]=1), and asserts a PCI Express or Local interrupt (Assert_INTA or LINTo#, respectively), when the interrupt is enabled (**LCS_DMAMODE0/1**[10]=1).

The PEX 8311 can also be programmed to assert PCI Express or Local interrupts after each descriptor is loaded, and the corresponding Data transfer is finished.

The DMA Controller can be programmed to clear the Transfer Size at completion of each DMA transfer, using the *DMA Clear Count Mode* bit for the affected DMA channel (**LCS_DMAMODE0/1**[16]=1).

Notes: *In DMA Scatter/Gather mode, the descriptor includes the PCI and Local Address space, Transfer Size, and Next Descriptor Pointer. It also includes a PCI Express 64-bit address value, when the DAC Chain Load bit for the affected DMA channel is enabled (**LCS_DMAMODE0/1[18]=1**). Otherwise, the **LCS_DMADAC0/1** register values are used.*

*The Descriptor Pointer register for the affected DMA channel (**LCS_DMADPR0/1**) contains Descriptor Location (bit 0), End of Chain (bit 1), Interrupt after Terminal Count (bit 2), Direction of Transfer (bit 3), and Next Descriptor Address (bits [31:4]) bits.*

DMA descriptors stored on the Local Bus are accessed using the same bus data width as programmed for the Data transfer.

A DMA descriptor can be located on PCI Express or Local memory, or both (for example, one descriptor on Local memory, another descriptor on PCI Express memory and vice-versa). The descriptors can also be located in the PCI Express Shared Memory, within the PEX 8311 bridge.

**Figure 9-20.   DMA Scatter/Gather Mode from PCI Express-to-Local Bus
(Control Access from Local Bus)**

Read and Write cycles continue...
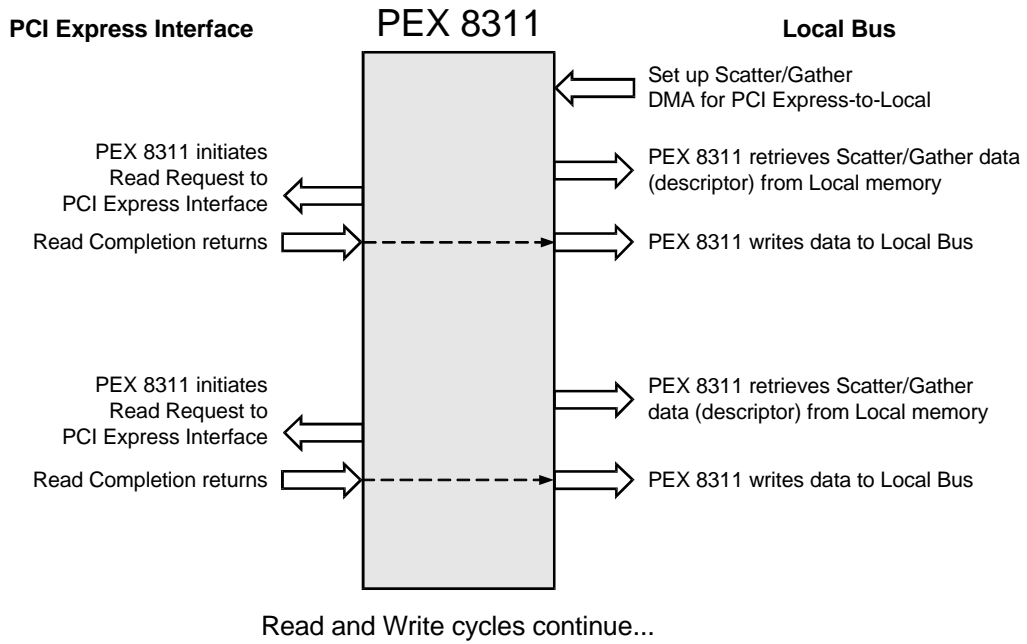
**Figure 9-21.   DMA Scatter/Gather Mode from Local-to-PCI Express
(Control Access from PCI Express Interface)**

Read and Write cycles continue...
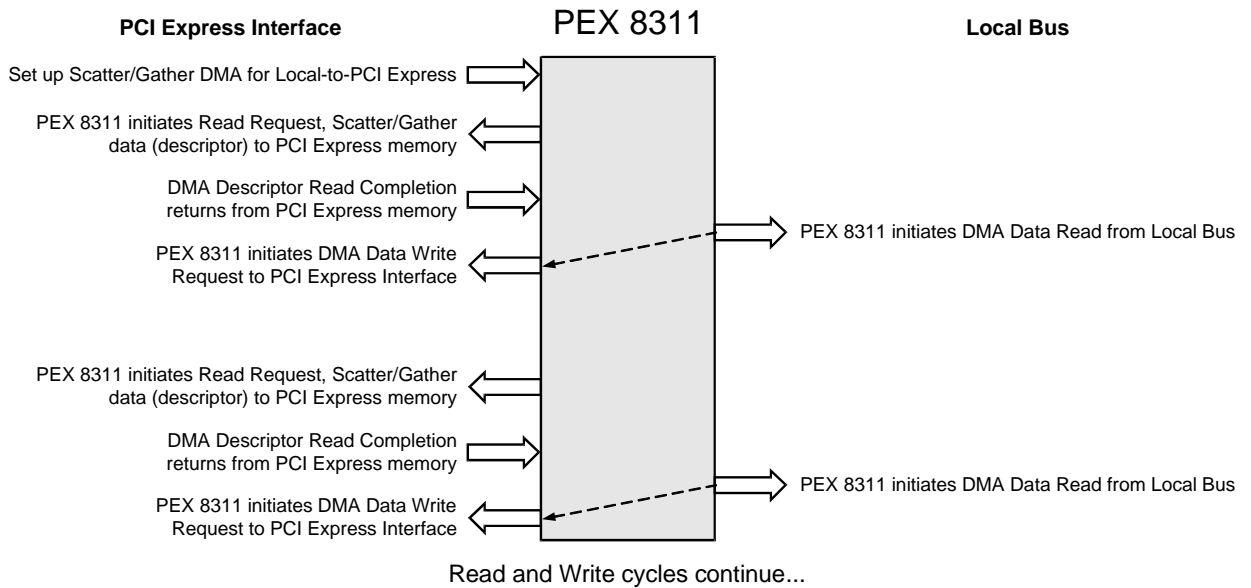
Note: Figure 9-20 and Figure 9-21 represent a sequence of Bus cycles.

9.5.5.1   Scatter/Gather DMA PCI Express Long Address Format

The PEX 8311 supports generation of the PCI Express Long Address format to access devices located above the 4-GB Address Boundary space in DMA Scatter/Gather mode for Data transfers only. Ensure that descriptor blocks reside below the 4-GB Address Boundary space. For PCI Express Long Address generation support the Local DMA space must be mapped to the PCI Express Prefetchable Address space. The PEX 8311 provides three different options of how PCI Express Long Address format Scatter/Gather DMA is used. Assuming the descriptor blocks are located on the PCI Express interface:

- **LCS_DMADAC0/1** has a non-zero value. **LCS_DMAMODE0/1**[18] is cleared to 0. The PEX 8311 performs a PCI Express Short Address format (32-bit address) 4-Dword descriptor block load from PCI Express memory and DMA transfer with PCI Express Long Address format on the PCI Express interface. (Refer to Figure 9-22.) Ensure that the DMA descriptor block starting addresses are 16-byte-aligned.

- **LCS_DMADAC0/1** has a value of 0h. **LCS_DMAMODE0/1**[18] is set to 1. The PEX 8311 performs a PCI Express Short Address format 5-Dword descriptor block load from PCI Express Memory and DMA transfer with PCI Express Long Address format on the PCI Express interface. (Refer to Figure 9-23.) Ensure that the DMA descriptor block starting addresses are 32-byte-aligned.

- **LCS_DMADAC0/1** has a non-zero value. **LCS_DMAMODE0/1**[18] is set to 1. The PEX 8311 performs a PCI Express Short Address format 5-Dword descriptor block load from PCI Express memory and DMA transfer with PCI Express Long Address format on the PCI Express interface. The fifth descriptor overwrites the value of the **LCS_DMADAC0/1** register for the affected DMA channel. (Refer to Figure 9-23.) Ensure that the DMA descriptor block starting addresses are 32-byte-aligned.

**Figure 9-22.   DMA Scatter/Gather Mode Descriptor Initialization
[PCI Express Short/Long Address Format PCI Express Address
(LCS_DMADAC0/1)
Register-Dependent]**
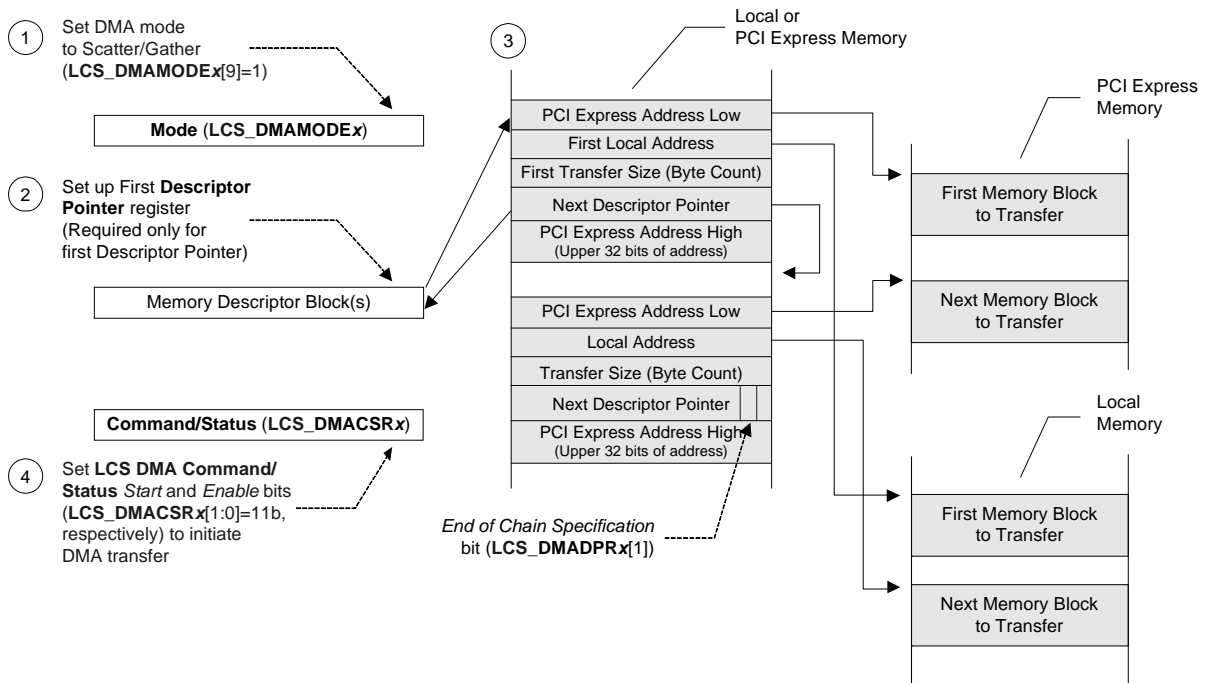
**Figure 9-23.   DMA Scatter/Gather Mode Descriptor Initialization
[PCI Express Long Address Format (LCS_DMAMODE0/1[18])
Descriptor-Dependent (PCI Express Address High Added)]**
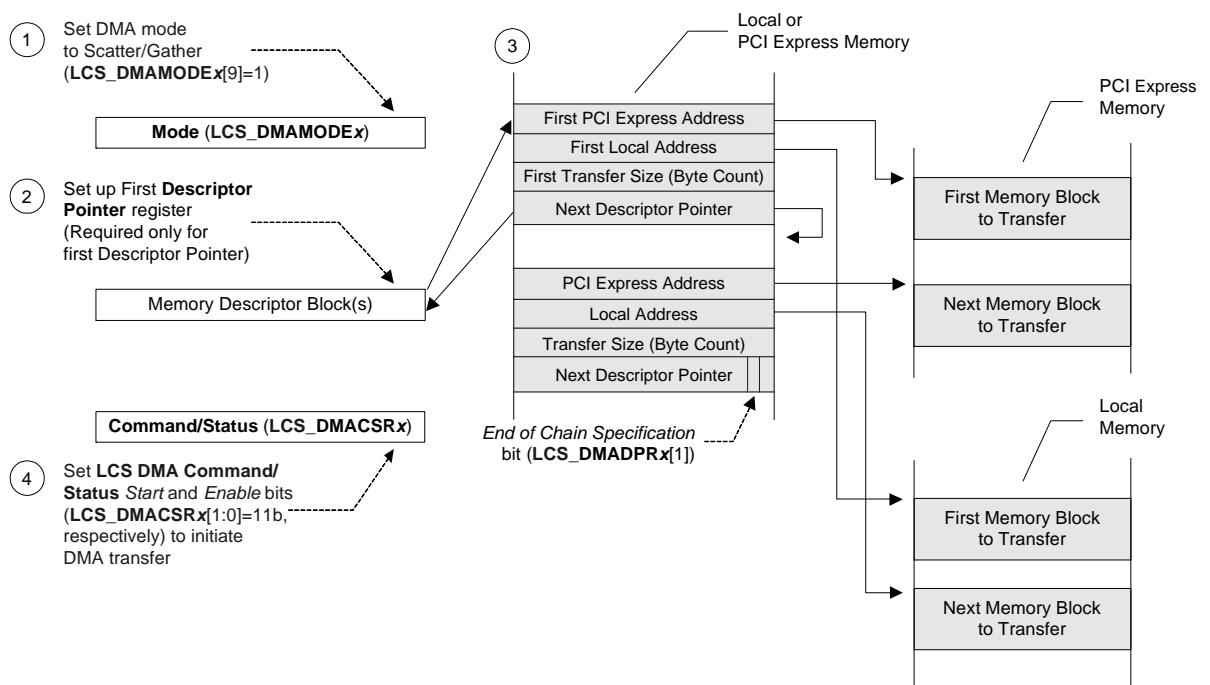
9.5.5.2   DMA Clear Count Mode

The PEX 8311 supports DMA Clear Count mode (Write-Back feature, **LCS_DMAMODE0/1** [16]). The PEX 8311 clears each Transfer Size descriptor to zero (0) by writing to its location on the PCI Express and/or Local Bus memory at the end of each transfer chain. This feature is available for DMA descriptors located on the PCI Express interface and Local Bus.

DMA Clear Count mode can also be used in conjunction with the EOT feature (**LCS_DMAMODE0/ 1**[14]). EOT# assertion during DMA Data transfers causes the PEX 8311 to write back the amount of data bytes not transferred to the destination bus.

When encountering a PCI Master/Target Abort internally between Local DMA Spaces and PCI Express Address spaces or Unsupported Request/Completer Abort on the PCI Express interface on a DMA Data transfer, the PEX 8311 writes random values when the descriptor is on the Local Bus. No write occurs when the descriptor is on the PCI Express interface.

Note: *DMA Clear Count mode works only if there is more than one descriptor in the descriptor chain, because the first descriptor is written directly into the PEX 8311 DMA Configuration registers and the remainder are loaded from PCI Express or Local memory.*

9.5.5.3   Ring Management DMA (Valid Mode)

In DMA Scatter/Gather mode, when the *Ring Management Valid Mode Enable* bit for the affected DMA channel is cleared (**LCS_DMAMODE0/1**[20]=0), the Valid bit for the affected DMA channel [bit 31 of the Terminal Count] is ignored. When the *Ring Management Valid Mode Enable* bit for the affected DMA channel is set to 1, the DMA descriptor proceeds only when the *Ring Management Valid* bit for the affected DMA channel is set (**LCS_DMASIZ0/1**[31]=1). When the *Valid* bit is set, the Terminal Count is 0, the descriptor is not the last descriptor, and the DMA Controller proceeds to the next descriptor in the chain.

When the *Ring Management Valid Stop Control* bit for the affected DMA channel is cleared (**LCS_DMAMODE0/1**[21]=0), the Scatter/Gather DMA Controller continuously polls the descriptor with the *Valid* bit for the affected DMA channel cleared to 0 (invalid descriptor) until the *Valid* bit is read as 1, which initiates the DMA transfer. When the *Valid* bit is read as 1, the DMA transfer for the affected DMA channel begins.

When the *Ring Management Valid Stop Control* bit for the affected DMA channel is set to 1, the Scatter/ Gather DMA Controller pauses when a *Valid* bit with a value of 0 is detected. In this case, the processor must restart the DMA Controller by setting the *DMA Channel Start* bit for the affected DMA channel (**LCS_DMACSR0/1**[1]=1). The *DMA Clear Count Mode* bit for the affected DMA channel must be enabled (**LCS_DMAMODE0/1**[16]=1) for the *Ring Management Valid* bit for the affected DMA channel (**LCS_DMASIZ0/1**[31]) to clear at the completion of each descriptor. (Refer to Figure 9-24 and/or Figure 9-25 for the Ring Management DMA descriptor load sequence for PCI Express Short and Long Address formats.)

Notes: *In Ring Management DMA Scatter/Gather mode, the descriptor includes the Transfer Size with a valid Descriptor bit, PCI Express and Local Address space, and Next Descriptor Pointer. It also includes a PCI Express 64-bit Address value when the DAC Chain Load bit for the affected DMA channel is enabled (**LCS_DMAMODE0/1**[18]=1). Otherwise, the **LCS_DMADAC0/1** register value for the affected DMA channel is used.*

In Ring Management mode, the Transfer Size is loaded before the PCI Express address.

**Figure 9-24. Ring Management DMA Scatter/Gather Mode Descriptor Initialization
[PCI Express Short/Long Address Format
PCI Express Address (LCS_DMADAC0/1) Register-Dependent]**
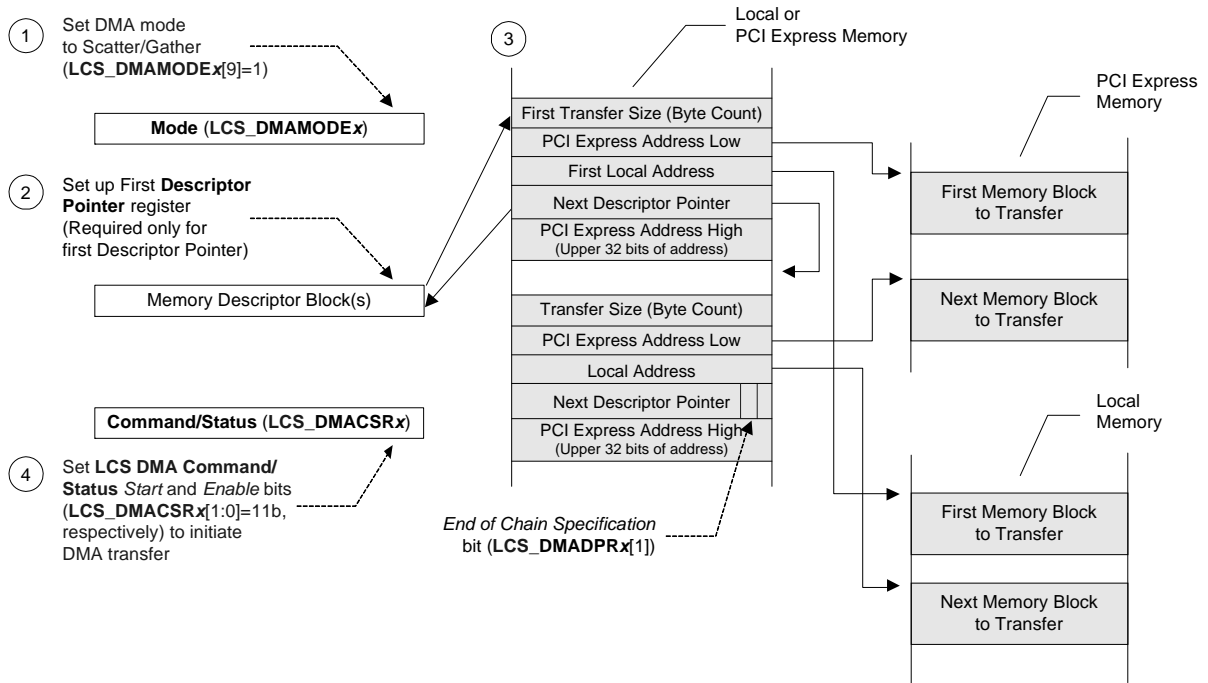
**Figure 9-25. Ring Management DMA Scatter/Gather Mode Descriptor Initialization
[PCI Express Long Address Format (LCS_DMAMODE0/1[18])
Descriptor-Dependent (PCI Express Address High Added)]**
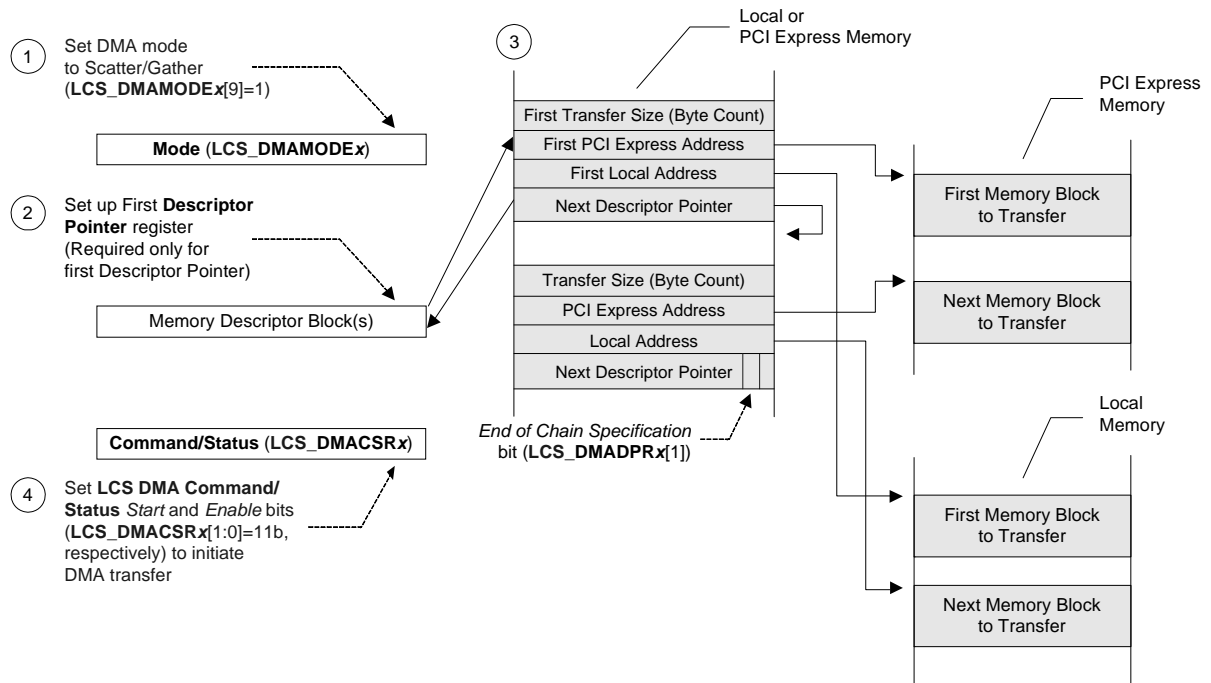
9.5.6   DMA Memory Write and Invalidate

The PEX 8311 can be programmed to perform Memory Write and Invalidate (MWI) cycles between Local DMA Spaces and PCI Express Address spaces for DMA transfers, as well as Direct Master (Local-to-PCI Express) transfers. (Refer to Section 9.2.10.) The PEX 8311 supports MWI transfers for Cache Line Sizes of 8 or 16 Dwords. Size is specified in the Local Bus register *System Cache Line Size* bits (**LCS_PCICLSR**[7:0]). When a size other than 8 or 16 is specified, the PEX 8311 performs Write transfers (using the Command Code programmed in **LCS_CNTRL**[7:4]), rather than MWI transfers. Internal MWI accesses to the PCI Express Spaces do not affect PEX 8311 TLP Write request generation and performance on the PCI Express interface.

DMA MWI transfers are enabled when the *Memory Write and Invalidate Mode for DMA Transfers* and *Memory Write and Invalidate Enable* bits are set (**LCS_DMAMODE0/1**[13]=1 and **LCS_PCICR**[4]=1, respectively).

In MWI mode, the PEX 8311 waits until the number of Dwords required for specified Cache Line Size are read from the Local Bus before starting the internal access from Local DMA Space to PCI Express Address space. This ensures a complete Cache Line Write can complete within one internal transaction. When a PCI Express Space disconnects before the internal Cache Line completes, the Local DMA Space completes the remainder of that Cache Line, using normal Writes before resuming MWI transfers. When an MWI cycle is internally in progress, the PEX 8311 continues to burst when another Cache Line is read from the Local Bus before the cycle completes. Otherwise, the PEX 8311 terminates the burst and waits for the next Cache Line to be read from the Local Bus. When the final transfer is not a complete Cache Line, the PEX 8311 completes the DMA transfer, using normal Writes.

An EOT# assertion, or DREQ*x*# de-assertion in DMA Demand mode occurring before the Cache Line is read from the Local Bus, results in a normal internal Write transaction from Local DMA Space to PCI Express Address space Write of the data read into a DMA FIFO. When the DMA Data transfer starts from a Non-Cache Line boundary, it first performs normal Writes until it reaches the Cache Line boundary internally within PEX 8311. When the DMA Data transfer has more than one line of data in the DMA FIFO, it starts the MWI transfer.

9.5.7   DMA Abort

DMA transfers can be aborted by software commands, or by issuing the EOT# signal. (Refer to Section 9.5.14 for further details regarding EOT#.)

To abort a DMA transfer:

1. Clear the *DMA Channel Enable* bit for the affected DMA channel (**LCS_DMACSR0/1**[0]=0).

2. Abort the DMA transfer by setting the *DMA Channel Abort* bit for the affected DMA channel, along with the *DMA Channel Start* bit for the affected DMA channel (**LCS_DMACSR0/1**[2:1]=11b, respectively).

3. Wait until the *DMA Channel Done* bit for the affected DMA channel is set (**LCS_DMACSR0/1**[4]=1).

Note: *One to two Data transfers occur after the Abort bit is set. Software can simultaneously set LCS_DMACSR0/1[2:0]. Setting software commands to abort a DMA transfer when no DMA cycles are in progress causes the next DMA transfer to abort.*

9.5.8   DMA Channel Priority

The *DMA Channel Priority* field (**LCS_MARBR**[20:19]) is used to specify the priorities defined in Table 9-14.

Table 9-14.   DMA Channel Priority Bit Specifications

LCS_MARBR[20:19]	Channel Priority
00b	Rotating
01b	DMA Channel 0
10b	DMA Channel 1
11b	*Reserved*

9.5.9   DMA Channel *x* Interrupts

A DMA channel can generate PCI Express Wire Interrupt (INTA#), as well as generate Local interrupts when done (transfer complete) or after a transfer is complete for the current descriptor in DMA Scatter/Gather mode. The *DMA Channel Interrupt Select* bit for the affected DMA channel determines whether to generate a PCI Express or Local interrupt (**LCS_DMAMODE0/1**[17]=1 or 0, respectively). The PCI Express device or Local processor can read the *DMA Channel Interrupt Active* bit for the affected DMA channel, to determine whether a DMA Channel interrupt is pending (**LCS_INTCSR**[22 and/or 21]=1).

The *DMA Channel Done* bit for the affected DMA channel (**LCS_DMACSR0/1**[4]) can be used to determine whether an interrupt is one of the following:

- DMA Done interrupt
- Transfer complete for current descriptor interrupt

Setting **LCS_DMAMODE0/1**[10]=1 enables a DMA Channel Done interrupt. In DMA Scatter/Gather mode, the **Descriptor Pointer** register *Interrupt after Terminal Count* bit for the affected DMA channel (**LCS_DMADPR0/1**[2], loaded from Local memory) specifies whether to generate an interrupt when the transfer ends on the current descriptor.

Setting **LCS_DMACSR0/1**[3]=1 clears an interrupt for the affected DMA channel.

9.5.10   DMA Data Transfers

The PEX 8311 DMA Controller can be programmed to transfer data from PCI Express-to-Local or Local-to-PCI Express, as illustrated Figure 9-26 through Figure 9-29.

Figure 9-26.   PCI Express-to-Local DMA Data Transfer Operation – M Mode
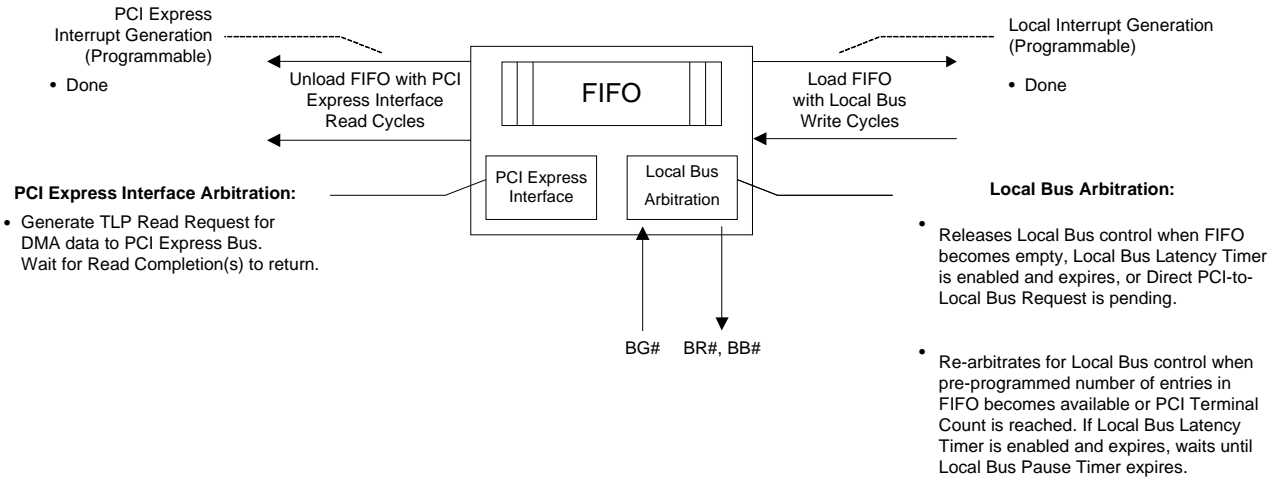
Figure 9-27.   Local-to-PCI Express DMA Data Transfer Operation – M Mode
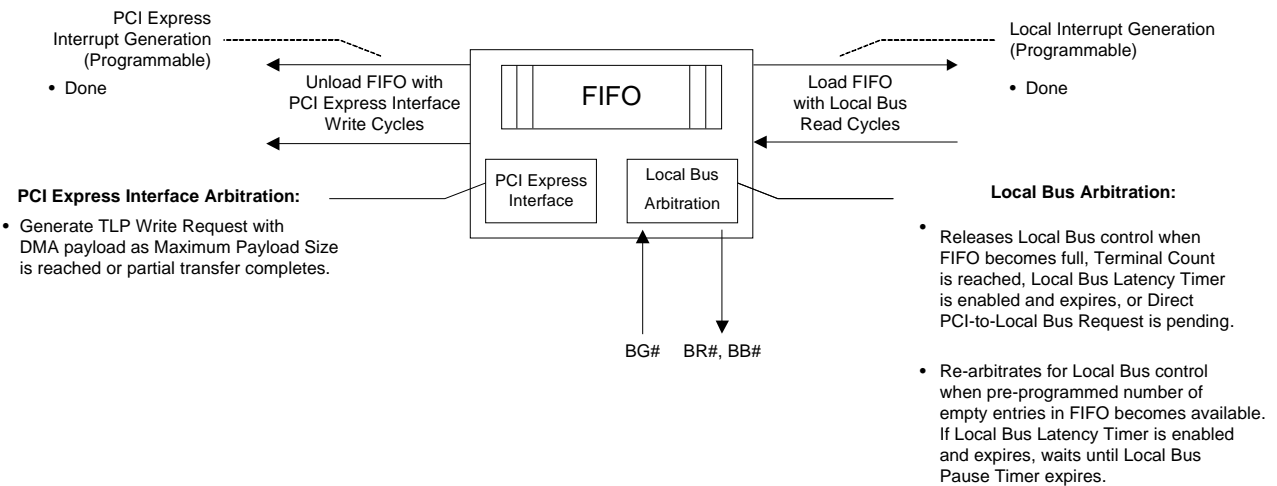
Figure 9-28. PCI Express-to-Local DMA Data Transfer Operation – C and J Modes

PCI Express
Interrupt Generation
(Programmable)
• Done

Unload FIFO with PCI
Express Interface
Read Cycles

FIFO

Load FIFO
with Local Bus
Write Cycles

Local Interrupt Generation
(Programmable)
• Done

PCI Express
Interface

Local Bus
Arbitration

PCI Express Interface Arbitration:
• Generate TLP Read Request for
DMA data to PCI Express Bus.
Wait for Read Completion(s) to return.

Local Bus Arbitration:
• Releases Local Bus control when FIFO
becomes empty, Local Bus Latency Timer
is enabled and expires, BREQi is asserted,
or Direct PCI-to-Local Bus Request
is pending.

• Re-arbitrates for Local Bus control when
pre-programmed number of entries in
FIFO becomes available or PCI Terminal
Count is reached. If Local Bus Latency
Timer is enabled and expires, waits until
Local Bus Pause Timer expires.

LHOLDA   LHOLD

Figure 9-29. Local-to-PCI Express DMA Data Transfer Operation – C and J Modes

PCI Express
Interrupt Generation
(Programmable)
• Done

Unload FIFO with
PCI Express Interface
Write Cycles

FIFO

Load FIFO
with Local Bus
Read Cycles

Local Interrupt Generation
(Programmable)
• Done

PCI Express
Interface

Local Bus
Arbitration

PCI Express Interface Arbitration:
• Generate TLP Write Request with
DMA payload as Maximum Payload Size
is reached or partial transfer completes.

Local Bus Arbitration:
• Releases Local Bus control when
FIFO becomes full, Terminal Count
is reached, Local Bus Latency Timer
is enabled and expires, BREQi is
asserted, or Direct PCI-to-Local Bus
Request is pending.

• Re-arbitrates for Local Bus control
when pre-programmed number of
empty entries in FIFO becomes available.
If Local Bus Latency Timer is enabled
and expires, waits until Local Bus
Pause Timer expires.

LHOLDA   LHOLD

9.5.11   DMA Local Bus Error Condition – M Mode Only

The PEX 8311 supports Local Bus error conditions with the TEA# signal. A device on the Local Bus can assert TEA#, either before or simultaneously with TA#. In either case, the PEX 8311 attempts to finish the current transaction by transferring data and then asserting TS# for every address that follows, waiting for another TA# or TEA# to be issued to flush the FIFOs. After sensing that TEA# is asserted, the PEX 8311 asserts PCI SERR# and sets the Signaled System Error (SERR# Status) bit (**LCS_PCISR**[14]=1), if enabled (**LCS_PCICR**[8]=1), indicating a catastrophic error occurred on the Local Bus. SERR# can be masked by resetting the *TEA# Input Interrupt Mask* bit (**LCS_LMISC1**[5]=0).

The PEX 8311 Local Bus Pause and Latency Timers (**LCS_MARBR**[15:0]) can be used to better use the Local Bus.

9.5.12   DMA Unaligned Transfers

For unaligned Local-to-PCI Express transfers, the PEX 8311 reads a partial Dword from the Local Bus. It continues to read Dwords from the Local Bus. Dwords are assembled, aligned to the PCI Express interface address, and loaded into the FIFO, then the data is passed to the PCI Express Address space for TLP Write request to generate.

For PCI Express-to-Local transfers, a TLP Read request is generated (PCI Express allows the first and the last data to unalign). As PCI Express Read Completion is received the data is passed from the PCI Express Space to Local DMA Space (FIFO), Dwords are assembled from the FIFO, aligned to the Local Bus address and written to the Local Bus.

The Byte Enables for writes determine least significant Address bits for the start of a transfer on the Local Bus, as well as on the internal PCI Bus between Local DMA and PCI Express Address spaces. For the last transfer, Byte Enables specify the bytes to write.

9.5.13 DMA Demand Mode, Channel *x*

9.5.13.1 DMA Demand Mode, Channel *x* – C and J Modes

DMA Demand mode allows the transfer of DMA data to be controlled by the DREQx# input pin(s). When DREQx# is asserted, the PEX 8311 starts a DMA transfer, based upon the values programmed into the DMA registers or by using internally stored values when resuming the transfer after it was paused in response to a DREQx# de-assertion. The PEX 8311 asserts DACKx#, to indicate that the DMA transfer is in-progress on the Local Bus. DACKx# asserts with ADS#, and remains asserted until one clock before the PEX 8311 de-asserts LHOLD to release the Local Bus. Data is only written to, or read from, the Local Bus while DACKx# is asserted. DACKx# de-assertion indicates that the DMA transfer has completed or is being paused in response to a DREQx# de-assertion, or because the PEX 8311 needs to release the Local Bus as described in Section 5.4.4.2. While processing in DMA Demand mode, the amount of data transferred during a Local Bus access depends upon the length and timing of the DREQx# assertion. If DREQx# is not asserted a sufficient length of time that allows all data to be transferred to complete the DMA transfer, the PEX 8311 transfers data in Lword-sized chunks until it releases the Local Bus. For an 8-bit Local Bus device, the PEX 8311 releases the Local Bus after transferring the last byte of an Lword. For a 16-bit Local Bus device, the PEX 8311 releases the bus after transferring the last word of an Lword, unless it is the last byte or word of the transfer.

Each DMA channel is capable of two types of transfers, PCIe-to-Local or Local-to-PCIe, as selected by the DMA Channel x Direction of Transfer bit (LCS_DMADPRx[3]). In either case, the PEX 8311 becomes an Initiator on the PCI Express and Local Buses, to execute the DMA transfer. If the DMA Local-to-PCIe FIFO becomes full, DACKx# is de-asserted and the DREQx# assertion is ignored. Subsequent transfers do not occur until DACKx# is re-asserted, indicating that additional room is now available in the FIFO. The following can be used to modify the functionality of the DMA Demand mode transfer:

- DMA Channel x Fast/Slow Terminate Mode Select bit (LCS_DMAMODEx[15]) setting
- PCI Express Bus starting or resuming address
- Local Bus starting or resuming address
- Local Bus widths

The functional changes that these items cause are explained, in detail, in the sections that follow. DREQx# can be asserted from one clock to more clocks than is necessary, to transfer all the DMA data. This, combined with the other factors that modify the PEX 8311 functionality, create a wide variety of responses to the assertion of DREQx#. The simplest way to use DMA Demand mode is to use Slow Terminate Mode (LCS_DMAMODEx[15]=0) to assert the DREQx# pin, wait for DACKx# to assert, allow some data to transfer before de-asserting DREQx#, then continue to accept or provide data until the last Lword is transferred with BLAST# asserted. If the DREQx# assertion for a DMA transfer will never resume for ongoing transfers, a DMA Abort procedure or the EOT# Input signal/pin assertion can be applied, to terminate the DMA transfer and/or flush the DMA FIFO.

Note: If bursting is enabled (LCS_DMAMODEx[8]=1) when DMA Constant Address mode is also enabled (LCS_DMAMODEx [11]=1), the PEX 8311 enables Continuous Burst mode, regardless of the Continuous Burst bit setting (LCS_DMADMODEx[7]=x).

9.5.13.1.1 Fast/Slow Terminate Mode

In Slow Terminate mode (LCS_DMAMODEx[15]=0), the PEX 8311 adheres to the C and J mode protocol and asserts BLAST# output, to indicate that the current Data transfer is the last Lword to be transferred before releasing the Local Bus while processing in DMA Demand mode.

In Fast Terminate Mode (LCS_DMAMODEx[15]=1) the PEX 8311 is not required to adhere to the C and J mode protocol regarding BLAST# output assertion (to indicate that the current data transfer is the last Lword to be transferred before releasing the Local Bus). However, the PEX 8311 still asserts BLAST# in Fast Terminate mode if DREQx# input is de-asserted and the external READY#=0 (asserted), on the transfer before the Local Address is to be LA[2:0]=000b (C mode) or LAD[2:0]=000b (J mode), or if the internal Wait State Counter(s) decrements to 0 for the current Lword.

Slow Terminate mode is the default setting. Running in Slow Terminate mode is recommended, unless the user needs the PEX 8311 to immediately release the Local Bus, and is willing to account for a disconnection with or without BLAST# assertion on the last Data transfer. Running in Fast Terminate mode is usually combined with EOT# assertion, to terminate/ complete the DMA transfer and/or flush the DMA FIFO.

9.5.13.1.2   PCIe-to-Local DMA Demand Mode

For a PCIe-to-Local Bus DMA Demand Mode transfer, independent of the DREQx# assertion the PEX 8311 starts reading data from the PCIe Bus into the DMA FIFO, upon the setting of the DMA Channel x Start bit (LCS_DMACSRx[1]=1). The PEX 8311 continued to read data from the PCIe Bus, and attempts to keep the FIFO full, until the entire DMA transfer is complete. The PEX 8311 waits for at least 2 Lwords of data to be read into the DMA FIFO and DREQx# to be asserted before attempting to arbitrate for, and write data to, the Local Bus. The PEX 8311's behavior in response to DREQx# assertion depends upon the following:

- When, and for how long, DREQx# is asserted
- Where DREQx# is de-asserted with relation o DACKx#
- Data availability
- PCIe and Local Bus starting or resumption addresses
- DMA Channel x Fast/Slow Terminate Mode Select bit (LCS_DMAMODEx[15]) setting
- Transfer/protocol dependencies

At least 2 Lwords of data must be available in the FIFO, for the PEX 8311 to respond to DREQx# assertion for one or more Local clock periods. The detailed response descriptions that follow assume that 2 Lwords have already been read into the FIFO, or that DREQx# is being asserted for a sufficient length of time to read 2 Lwords into the FIFO.

EOT# assertion causes the PEX 8311 to terminate the ongoing DMA transfer and flush the FIFO. However, before the PEX 8311 releases the Local Bus, it may or may not need to write additional data. Details of the terminating Local Bus behavior, when EOT# is asserted, are also provided below.

Slow Terminate mode (LCS_DMAMODEx[15]=0)

- DREQx# assertion for one Local clock period when at least 2 Lwords of data are available in the FIFO, or assertion up to, but not including, the first Clock cycle with DACKx# asserted, results in a one Lword transfer on the Local Bus with a BLAST# assertion.
- DREQx# de-assertion on the clock period of DACKx# assertion, or any clock period after DACKx# assertion, results in one to two additional Lword transfers on the Local Bus. BLAST# is asserted with the last Lword.
- DREQx# assertion (when 2 or more Lwords are available in the FIFO), then de-assertion followed by a re-assertion, up to and including the first cycle of DACKx# assertion, causes the PEX 8311 to hold LHOLD asserted and continue to transfer additional Lwords as long as DREQ# remains asserted and data is available. Otherwise, the PEX 8311 asserts BLAST#, transfers one Lword release, and re-arbitrates for the Local Bus when it detects that DREQx# is asserted again. For each transfer, BLAST# is asserted with the last Lword.
- If EOT# is asserted and DREQx# is de-asserted on the same clock, the PEX 8311 transfers one additional Lword with BLAST# asserted, before terminating the ongoing DMA Data transfer and flushing the DMA FIFO.

Fast Terminate mode (LCS_DMAMODEx[15]=1)

- DREQx# assertion for one Local clock period when at least 2 Lwords of data are available in the FIFO, or assertion up to, but not including, the first Clock cycle with DACKx# asserted, results in a one Lword transfer on the Local Bus with a BLAST# assertion.

- DREQx# de-assertion on the same clock as DACKx# assertion, or any other Clock cycle thereafter in which DACKx# is asserted, results in one additional Lword transferred to the Local Bus without BLAST# assertion.

- DREQx# assertion (when 2 or more Lwords are available in the FIFO), then de-assertion followed by a re-assertion, up to and including the first cycle of DACKx# assertion, causes the PEX 8311 to hold LHOLD asserted and continue to transfer additional Lwords, as long as DREQx# remains asserted and data is available. Otherwise, the PEX 8311 asserts BLAST#, transfers one Lword release, and rearbitrates for the Local Bus when it detects that DREQx# is asserted again. Upon the following DREQx# de-assertion, one additional Lword is transferred on the Local Bus without a BLAST# assertion.

- If DREQx# is de-asserted during the transfer, the PEX 8311 can assert BLAST# if either of the following conditions are met:
    - Data is the last Lword for the entire DMA transfer
    - Local Bus Latency Timer expires

- If EOT# is asserted and DREQx# is de-asserted on the same clock that the PEX 8311 transfers valid data, the PEX 8311 does not assert BLAST# nor provide valid data on subsequent Clock cycles.

The PEX 8311 releases the Local Bus 2 clocks after EOT# is asserted, terminates the ongoing DMA Data transfer, and flushes the DMA FIFO.

9.5.13.1.3   Local-to-PCIe DMA Demand Mode

For a Local-to-PCIe Bus DMA Demand Mode transfer, the PEX 8311 does not arbitrate on the Local Bus to read data into the DMA FIFO until the DMA Channel x start bit (LCS_DMACSRx[1]=1) and the DREQx# signal/pin is asserted. As long as DREQx# is asserted, the PEX 8311 continues to read data from the Local Bus and attempts to keep the FIFO full, until the entire DMA transfer is complete. The PEX 8311 waits for at least 1 Lword of data to be read into the DMA FIFO before attempting to arbitrate for, and write data to, the PCIe Bus. The PEX 8311 behavior in response to DREQx# assertion depends upon the following:

- When, and for how long, DREQx# is asserted

- Where DREQx# is de-asserted with relation to DACKx#

- Data availability

- PCIe and Local Bus starting or resumption addresses

- DMA Channel x Fast/Slow Terminate Mode Select bit (LCS_DMAMODEx[15]) setting

- Transfer/protocol dependencies

For transfers that are reading data from a 32-bit Local Bus device, the PEX 8311 requires 1 or 2 Lwords to be read (explanation follows) and placed into the DMA FIFO before it arbitrates for, and writes data to, the PCIe Bus. As a result, if 2 Lwords must be read, one Lword of data will remain in the DMA FIFO until the second Lword is read. Upon reading the required amount of data, the PEX 8311 then arbitrates for, and writes the data to, the PCIe Bus.

For non-Lword aligned transfers that read data from 8- or 16-bit Local Bus devices, the PEX 8311 requires a minimum amount of bytes or words to be read from the Local Bus device before it arbitrates for, and writes data to, the PCIe Bus. The number of bytes or words that it must read before transferring the data to the PCIe Bus is determined by the PCIe starting address. As a result, there could be seven or fewer bytes remaining in the DMA FIFO at any given time. Therefore, once a DMA Demand Mode transfer is started (DREQx# asserted), it may be necessary for the PEX 8311 to read more bytes, words or Lwords from the Local Bus than are required to complete the DMA transfer. If bytes, words, or an Lword remain in the DMA FIFO due to a DREQx# de-assertion, when DREQx# is re-asserted (and additional data is read), that data is transferred to the PCIe Bus. If the DREQx# assertion never resumes for ongoing transfers, a DMA Abort procedure or EOT# assertion can be applied to terminate/complete the ongoing DMA transfer.

It is recommended that DREQx# be asserted until DACKx# is asserted and at least 4 Lwords of data are read into the DMA FIFO. However, the following information is provided, for allowing smaller transfers inside an ongoing DMA transfer.

Because there are 2 Lwords per DMA FIFO location, the PEX 8311 places data into the DMA FIFO in 2-Lword quantities. Therefore, when DREQx# is de-asserted the PEX 8311 continues to read data up to the next Qword-aligned boundary [X0h or X8h address boundary (Local Address LA[2:0]=000b (C mode) or LAD[2:0]=000b (J mode))].

Detailed descriptions of the PEX 8311's response to DREQx# assertion when the DMA transfer first starts or resumes reading data from Local Bus are provided below.

EOT# assertion causes the PEX 8311 to terminate the ongoing DMA transfer. However, before the PEX 8311 releases the Local Bus, it may or may not need to read additional data. Details of the terminating Local Bus behavior when EOT# is asserted are also provided below. All data that is read into the DMA FIFO is written to the PCIe Bus.

Slow Terminate mode (LCS_DMAMODEx[15]=0)

- If the PCIe destination address is X0h/X8h, and DREQx# is asserted for one Local Bus Clock cycle, or asserted then de-asserted on any cycle before READY# is asserted, the PEX 8311 requires 2 Lwords to be read into the DMA FIFO.

- If the PCIe destination address is X0h/X8h, and DREQx# is asserted and remains asserted until it is de-asserted on the first or second cycle that data is transferred (READY# asserted), the PEX 8311 requires one additional Lword to be read into the DMA FIFO.

- If the PCIe destination address is X0h/X8h, and DREQx# is asserted and held asserted until it is de-asserted on a cycle that is transferring the 3, 5, 7… (Odd) Lword with READY# asserted, the PEX 8311 requires one additional Lword to be read into the DMA FIFO.

- If the PCIe destination address is X0h/X8h, and DREQx# is asserted and held asserted until it is de-asserted on a cycle that is transferring the 4, 6, 8… (Even) Lword with READY# asserted, the PEX 8311 requires two additional Lwords to be read into the DMA FIFO.

- If the PCIe destination address is X4h/XCh, and DREQx# is asserted for one Local Bus Clock cycle, or is asserted and then de-asserted before or on the same cycle that the PEX 8311 asserts ADS#, the PEX 8311 requires 1 Lword to be read into the DMA FIFO.

- If the PCIe destination address is X4h/XCh, and DREQx# is asserted and remains asserted on the cycle that the PEX 8311 asserts ADS# and then de-asserts before any data is transferred (READY# not asserted), the PEX 8311 requires 2 Lwords to be read into the DMA FIFO.

- If the PCIe destination address is X4h/XCh, and DREQx# is asserted and held asserted until it is de-asserted on a cycle that is transferring the first or an even 2, 4, 6, 8… Lword with READY# asserted, the PEX 8311 requires one additional Lword to be read into the DMA FIFO.

- If the PCIe destination address is X4h/XCh, and DREQx# is asserted and held asserted until it is de-asserted on a cycle that is transferring the 3, 5, 7… (Odd) Lword with READY# asserted, the PEX 8311 requires two additional Lwords to be read into the DMA FIFO.

- If EOT# is asserted along with DREQx# de-assertion while the PEX 8311 is reading data (READY# asserted), the PEX 8311 asserts BLAST# and must read one additional Lword of data before releasing the Local Bus. Otherwise, upon the re-assertion of READY#, the PEX 8311 must read one L word before asserting BLAST#and reading a second Lword.

Fast Terminate mode (LCS_DMAMODEx[15]=1)

- If DREQx# is asserted for one Local clock period or is asserted and remains asserted until it is de-asserted before or during a Data transfer, the PEX 8311 does not assert BLAST#; however, it requires one to two additional Lwords to be read into the DMA FIFO.

- If DREQx# is de-asserted during the Data transfer, the PEX 8311 can assert BLAST# if any of the following conditions are met:
    - Starting PCIe address is X4h/XCh
    - Data is the last data for the entire DMA transfer
    - Local Bus Latency Timer expires

- If EOT# is asserted along with DREQx# de-assertion while the PEX 8311 is reading data (READY# asserted), the PEX 8311 reads one additional Lword of data (during the cycle that EOT# is asserted), then immediately releases the Local Bus. Otherwise, the PEX 8311 waits for the re-assertion of READY# to read 1 Lword of data before releasing the Local Bus.

9.5.13.1.4   End of Transfer (EOT#) Input

EOT# is a one-clock wide pulse that ends a DMA transfer. It should be asserted only when the PEX 8311 owns the Local Bus. Depending on whether Fast or Slow Terminate mode is selected, the DMA transfer ends without a BLAST# assertion (Fast Terminate mode) or with BLAST# asserted (Slow Terminate mode). The LCS_DMAMODEx[15:14] bits enable and control how the PEX 8311 responds to an EOT# input assertion.

In Fast Terminate mode, if EOT# is asserted while the PEX 8311 receives an external READY# signal assertion, the DMA Controller(s) ends the DMA transfer and releases the Local Bus. In Slow Terminate mode, if EOT# is asserted while the PEX 8311 receives an external READY# signal assertion, the DMA Controller(s) completes the current Lword and one additional Lword. If the DMA FIFO is full or empty after the Data phase in which EOT# is asserted, the second Lword is not transferred.

If the PEX 8311 does not require that BLAST# output be driven for the last data transferred when a DMA transfer is terminated using EOT#, the Fast Terminate mode setting (LCS_DMAMODEx[15]=1) may be used. If EOT# is asserted in Fast Terminate mode, the DMA Controller(s) terminates the DMA transfer and releases the Local Bus upon receiving an external READY# signal assertion. Or, the internal Wait State Counter(s) decrements to 0 for the current Lword when EOT# is asserted. If the data is the last data in the transfer, BLAST# is asserted on the last transfer.

If the PEX 8311 requires that BLAST# output be asserted on the last data transfer when a DMA transfer is terminated using EOT#, then the Slow Terminate mode setting (LCS_DMAMODEx[15]=0) must be used. If EOT# is asserted in Slow Terminate mode, the DMA Controller(s) transfers one or two additional Lwords, depending upon the Local Bus data width and the address when EOT# is asserted.

The DMA Controller(s) terminates a transfer on an Lword boundary after EOT# is asserted. For an 8-bit bus, the PEX 8311 terminates after transferring the last byte for the Lword. For a 16-bit bus, the PEX 8311 terminates after transferring the last word for the Lword.

During the descriptor loading on the Local Bus, EOT# assertion causes a complete descriptor load and no subsequent Data transfer; however, this is not recommended. EOT# has no effect when loading the descriptor from the PCIe Bus.

9.5.13.2   DMA Demand Mode, Channel *x* – M Mode

DMA Demand mode allows the transfer of DMA data to be controlled by the DREQx# input pin(s). WhenDREQx# is asserted, the PEX 8311 starts a DMA transfer, based upon the values programmed into the DMA registers or by using internally stored values when resuming the transfer after it was paused in response to a DREQx# de-assertion. The PEX 8311 asserts DACKx#, to indicate that the DMA transfer is in-progress on the Local Bus. DACKx# asserts with TS#, and remains asserted until one clock before the PEX 8311 de-asserts BB# to release the Local Bus.

Data is only written to, or read from, the Local Bus while DACKx# is asserted. DACKx# de-assertion indicates that the DMA transfer has completed or is being paused in response to a DREQx# de-assertion, or because the PEX 8311 needs to release the Local Bus as described in Section 9.5.4.

While processing in DMA Demand mode, the amount of data transferred during a Local Bus access depends upon the length and timing of the DREQx# assertion. If DREQx# is not asserted a sufficient length of time that allows all data to be transferred to complete the DMA transfer, the PEX 8311 transfers data in Lword-sized chunks until it releases the Local Bus. For an 8-bit Local Bus device, the PEX 8311 releases the Local Bus after transferring the last byte of an Lword.

For a 16-bit Local Bus device, the PEX 8311 releases the bus after transferring the last word of an Lword, unless it is the last byte or word of the transfer.

Each DMA channel is capable of two types of transfers, PCIe-to-Local or Local-to-PCIe, as selected by the DMA Channel x Direction of Transfer bit (LCS_DMADPRx[3]). In either case, the PEX 8311 becomes An Initiator on the PCIe and Local Buses, to execute the DMA transfer. If the DMA Local-to-PCIe FIFO becomes full, DACKx# is de-asserted and the DREQx# assertion is ignored. Subsequent transfers do not occur until DACKx# is re-asserted, indicating that additional room is now available in the FIFO.

The following can be used to modify the functionality of the DMA Demand mode transfer:

- DMA Channel x Continuous Burst Enable bit (LCS_DMAMODEx[7]) setting
- DMA Channel x Fast/Slow Terminate Mode Select bit (LCS_DMAMODEx[15]) setting
- PCIe Bus starting or resuming address
- Local Bus starting or resuming address
- Local Bus widths

The functional changes that these items cause are explained, in detail, in the sections that follow.

DREQx# can be asserted from one clock to more clocks than is necessary, to transfer all the DMA data. This, combined with the other factors that modify the PEX 8311 functionality, create a wide variety of responses to the assertion of DREQx#. The simplest way to use DMA Demand mode is to use Slow Terminate Mode (LCS_DMAMODEx[15]=0) to assert the DREQx# pin, wait for DACKx# to assert, allow some data to transfer before de-asserting DREQx#, then continue to accept or provide data until the PEX 8311 releases the Local Bus. If the DREQx# assertion for a DMA transfer will never resume for ongoing transfers, a DMA Abort procedure or the EOT# Input signal/pin assertion can be applied, to terminate/complete the DMA transfer and/or flush the DMA FIFO.

Note: If bursting is enabled (LCS_DMAMODEx[8]=1) when DMA Constant Address mode is also enabled (LCS_DMAMODEx [11]=1), the PEX 8311 enables Continuous Burst mode, regardless of the Continuous Burst bit setting (LCS_DMADMODEx[7]=x).

9.5.13.2.1   Fast/Slow Terminate Mode

In Slow Terminate mode (LCS_DMAMODEx[15]=0), the PEX 8311 adheres to the M mode protocol and de-asserts the BDIP# output, to indicate that the current Data transfer is the last Lword to be transferred of a burst before releasing the Local Bus while processing in DMA Demand mode.

In Fast Terminate Mode (LCS_DMAMODEx[15]=1) the PEX 8311 is not required to adhere to the M mode protocol regarding BDIP# output de-assertion (to indicate that the current data transfer is the last Lword to be transferred of a burst before releasing the Local Bus). Additionally, it forces the PEX 8311 into Continuous Burst mode, regardless of the LCS_DMAMODEx[7] register bit setting.

Slow Terminate mode is the default setting. Running in Slow Terminate mode is recommended, unless the user needs the PEX 8311 to immediately release the Local Bus, and is willing to account for a disconnection without BDIP# assertion on the last Data transfer.

Running in Fast Terminate mode is usually combined with EOT# assertion, to terminate/complete the DMA transfer and/or flush the DMA FIFO.

9.5.13.2.2   PCIe-to-Local DMA Demand Mode

For a PCIe-to-Local Bus DMA Demand Mode transfer, independent of the DREQx# assertion the PEX 8311 starts reading data from the PCIe Bus into the DMA FIFO, upon the setting of the DMA Channel x Start bit (LCS_DMACSRx[1]=1). The PEX 8311 continued to read data from the PCIe Bus, and attempts to keep the FIFO full, until the entire DMA transfer is complete. The PEX 8311 waits for at least 2 Lwords of data to be read into the DMA FIFO and DREQx# to be asserted before attempting to arbitrate for, and write data to, the Local Bus. The PEX 8311's behavior in response to DREQx# assertion depends upon the following:

- When, and for how long, DREQx# is asserted
- Where DREQx# is de-asserted with relation to DACKx#
- Data availability
- PCIe and Local Bus starting orresumption addresses
- DMA Channel x Fast/Slow Terminate Mode Select bit (LCS_DMAMODEx[15]) setting
- DMA Channel x Continuous Burst Enable bit (LCS_DMAMODEx[7]) setting
- Transfer/protocol dependencies

At least 2 Lwords of data must be available in the FIFO, for the PEX 8311 to respond to DREQx# assertion for one or more Local clock periods. The detailed response descriptions that follow assume that 2 Lwords have already been read into the FIFO, or that DREQx# is being asserted for a sufficient length of time to read 2 Lwords into the FIFO.

EOT# assertion causes the PEX 8311 to terminate the ongoing DMA transfer and flush the FIFO. However,before the PEX 8311 releases the Local Bus, it may or may not need to write additional data. Details of the terminating Local Bus behavior, when EOT# is asserted, are also provided below.

**Slow Terminate mode (LCS_DMAMODEx[15]=0) in Burst-4 mode
(LCS_DMAMODEx[8, 7]=10b)**

- If the Local Bus starting or resuming address is double Qword-aligned (LA[28:31]=0h), and DREQx# is asserted for one Local Bus clock cycle, or is asserted then de-asserted before the fourth Data transfer of a 4-Lword burst, the PEX 8311 executes/completes a 4-Lword Burst write and releases the Local Bus.
- If DREQx# remains asserted, the PEX 8311 completes the current 4-Lword burst and continues to execute and complete additional 4-Lword Burst writes.
- If DREQx# is de-asserted on the fourth Data transfer of any 4-Lword burst, the PEX 8311 completes the current burst and must complete one additional 4-Lword burst.
- If the Local Bus starting or resuming address is not double Qword-aligned (LA[28:31]≠0h), the PEX 8311 single cycles up to next double Qword-aligned boundary, then starts bursting 4 Lwords at a time.
- If DREQx# is de-asserted during a burst, the PEX 8311 completes the current burst and must complete one additional 4-Lword burst if DREQx# is de-asserted on the fourth Data transfer.

- If DREQx# is de-asserted during or before the start of a single cycle write, the PEX 8311 completes that write, then releases the Local Bus.

- If DREQx# is de-asserted during TS# assertion, the PEX 8311 must complete the current single cycle write and one additional single cycle write or 4-Lword Burst write.

- If EOT# is asserted along with DREQx# de-assertion while the PEX 8311 is writing the fourth Data transfer of the 4-Lword burst, the PEX 8311 must complete the current 4-Lword burst and one additional 4-Lword burst before releasing the Local Bus. Otherwise, the PEX 8311 will complete the current 4-Lword burst, and then release the Local Bus.

- If EOT# is asserted along with DREQx# de-assertion while the PEX 8311 is executing a single cycle write, the PEX 8311 completes that write and must complete another single cycle writeor a 4-Lword Burst write before terminating the ongoing DMA Data transfer, flushing the DMA FIFO, and releasing the Local Bus.

Slow Terminate mode (LCS_DMAMODEx[15]=0) in Continuous Burst mode (LCS_DMAMODEx[8, 7]=11b)

Regardless of the Local Bus starting or resuming address, if DREQx# is asserted for one Local Bus Clock cycle, or asserted then de-asserted before or with TS# assertion, the PEX 8311 executes a 1-Lword single cycle write before it releases the Local Bus.

- If the Local Bus starting or resuming address is double Qword-aligned (LA[28:31]=0h), and DREQx# remains asserted past the assertion of TS#, the PEX 8311 starts a Burst write. The PEX 8311 continues bursting until DREQx# is de-asserted. Upon DREQx# de-assertion, the PEX 8311 completes the current Data cycle and one additional Data cycle, with BDIP# de-asserted, before releasing the Local Bus.

- If the Local Bus starting or resuming address is not double Qword-aligned (LA[28:31]≠0h), and DREQx# remains asserted past TS# assertion, the PEX 8311 single cycles up to the next double Qword-aligned boundary, then starts a burst. After the PEX 8311 starts a burst, it continues to burst Write data until DREQx# is de-asserted. Upon DREQx# de-assertion, the PEX 8311 complete the current Data cycle and one additional Data cycle with BDIP# de-asserted, before releasing the Local Bus.

- If DREQx# is de-asserted while the PEX 8311 is executing a single cycle transfer, the PEX 8311 must complete the current single cycle, and may or may not need to complete one additional single cycle or 1-Lword burst.

- If EOT# is asserted along with DREQx# de-assertion while the PEX 8311 is bursting (writing) data, the PEX 8311 must complete the current Data cycle and one additional Data cycle with BDIP# de-asserted, before releasing the Local Bus.

- If the PEX 8311 is executing a single cycle transfer when EOT# is asserted along with DREQx# de-assertion, it must complete the current single cycle, and may or may not need to complete one additional single cycle or 1-Lword burst.

- If the PEX 8311 is asserting TS# for a Burst transfer when EOT# is asserted along with DREQx# de-assertion, the PEX 8311 must complete a 2-Lword burst before terminating the ongoing DMA Data transfer, flushing the DMA FIFO, and releasing the Local Bus.

Fast Terminate mode (LCS_DMAMODEx[15]=1), Continuous Burst mode (LCS_DMAMODEx[8, 7]=1xb)

In Fast Terminate mode (LCS_DMAMODEx[15]=1), the PEX 8311 defaults into Continuous Burst mode, regardless of the DMA Channel x Continuous Burst Mode bit (LCS_DMAMODEx[7]) setting. With these settings, the PEX 8311 operates the same as Slow Terminate/ Continuous Burst mode, with the following differences:

- BDIP# is never asserted.

- If DREQx# is de-asserted during a single cycle transfer, the PEX 8311 releases the Local Bus after the current write transfer completes. For a burst, the PEX 8311 writes one additional Lword with DREQx# de-asserted and TA# asserted [or the internal Wait State Counter(s) has decremented to 0] or wait for TA# assertion to complete the Write cycle before releasing the Local Bus.
- If EOT# is asserted along with DREQx# de-assertion while the PEX 8311 is starting a transfer to write data or is waiting (TA# de-asserted) to write data during a burst, the PEX 8311 must write one additional Lword of data before it releases the Local Bus. The PEX 8311 completes the final data transfer if TA# is asserted with EOT#, or when TA# becomes asserted after EOT# assertion.

If EOT# is asserted while waiting to complete a single cycle transfer, the PEX 8311 completes that transfer before releasing the Local Bus.

9.5.13.2.3   Local-to-PCIe DMA Demand Mode

For a Local-to-PCIe Bus DMA Demand Mode transfer, the PEX 8311 does not arbitrate on the Local Bus to read data into the DMA FIFO until the DMA Channel x Start bit (LCS_DMACSRx[1]=1) and the DREQx# signal/pin is asserted. As long as DREQx# is asserted, the PEX 8311 continues to read data from the Local Bus and attempts to keep the FIFO full, until the entire DMA transfer is complete. The PEX 8311 waits for at least 1 Lword of data to be read into the DMA FIFO before attempting to arbitrate for, and write data to, the PCIe Bus. The PEX 8311 behavior in response to DREQx# assertion depends upon the following:

- When, and for how long, DREQx# is asserted
- Where DREQx# is de-asserted with relation to DACKx#
- Data availability
- PCIe and Local Bus starting or resumption addresses
- DMA Channel x Fast/Slow Terminate Mode Select bit (LCS_DMAMODEx[15]) setting
- DMA Channel x Continuous Burst Enable bit (LCS_DMAMODEx[7]) setting
- Transfer/protocol dependencies

For transfers that are reading data from a 32-bit Local Bus device, the PEX 8311 require 1 or 2 Lwords to be read (explanation follows) and put into the DMA FIFO before it arbitrates for, and writes data to, the PCIe Bus.

As a result, if 2 Lwords must be read, one Lword of data will remain in the DMA FIFO until the second Lword is read. Upon reading the required amount of data, the PEX 8311 will then arbitrate for, and write the data to, the PCIe Bus.

For non-Lword aligned transfers that read data from 8- or 16-bit Local Bus devices, the PEX 8311 requires a minimum amount of bytes or words to be read from the Local Bus device before it arbitrates for, and writes data to, the PCIe Bus. The number of bytes or words that it must read before transferring the data to the PCIe Bus is determined by the PCIe starting address. As a result, there could be seven or fewer bytes remaining in the DMA FIFO at any given time.

Therefore, once a DMA Demand Mode transfer is started (DREQx# asserted), it may be necessary for the PEX 8311 to read more bytes, words or Lwords from the Local Bus than are required to complete the DMA transfer. If bytes, words, or an Lword remain in the DMA FIFO due to a DREQx# de-assertion, when DREQx# is re-asserted (and additional data is read), that data is transferred to the PCIe Bus. If the DREQx# assertion never resumes for ongoing transfers, a DMA Abort procedure or EOT# assertion can be applied to terminate/complete the ongoing DMA transfer.

Because there are 2 Lwords per DMA FIFO location, upon a DREQx# de-assertion, the PEX 8311 may or may not need to continue to read or write additional data. It is recommended that DREQx# be asserted until DACKx# is asserted and at least 4 Lwords of data are read into the DMA FIFO.

The PEX 8311's responses for allowing smaller transfers inside an ongoing DMA transfer are provided below.

EOT# assertion causes the PEX 8311 to terminate the ongoing DMA transfer. However, before the PEX 8311 releases the Local Bus, it may or may not need to read additional data. Details of the terminating Local Bus behavior when EOT# is asserted are also provided below. All data that is read into the DMA FIFO is written to the PCIe Bus.

Slow Terminate mode (LCS_DMAMODEx[15]=0) in Burst-4 mode (LCS_DMAMODEx[8, 7]=10b)

- If the Local Bus starting or resuming address is double Qword-aligned (LA[28:31]=0h), and DREQx# is asserted for one Local Bus clock cycle, or asserted then de-asserted before the fourth Data transfer of a 4-Lword burst, the PEX 8311 executes/ completes a 4-Lword Burst read, and then releases the Local Bus.

- If DREQx# remains asserted, the PEX 8311 completes the current 4-Lword burst and continues to execute and complete additional 4-Lword Burst reads.

- If DREQx# is de-asserted on or after the third Data transfer of any 4-Lword burst, the PEX 8311 completes the current burst and must complete one additional 4-Lword burst.

- If the Local Bus starting address is not double Qword-aligned (LA[28:31]≠0h), the PEX 8311 single cycles up to next double Qword-aligned boundary, then starts bursting 4 Lwords at a time.

- If DREQx# is de-asserted during a burst, the PEX 8311 completes the current burst and may need to complete an additional 4-Lword burst.

- If DREQx# is de-asserted during or before the start of a single cycle read, the PEX 8311 completes that read and any additional single cycle reads, then completes a 4-Lword burst.

- If EOT# is asserted along with DREQx# de-assertion while the PEX 8311 is reading the fourth Data transfer of the 4-Lword burst, the PEX 8311 must complete the current 4-Lword burst and one additional 4-Lword burst, before releasing the Local Bus. Otherwise, it will complete the current 4-Lword burst, and then release the Local Bus.

Slow Terminate mode (LCS_DMAMODEx[15]=0) in Continuous Burst mode (LCS_DMAMODEx[8, 7]=11b)

- Depending upon the PCIe and Local Bus starting or resuming addresses, where and how long DREQx# is asserted and where it is de-asserted, the PEX 8311 must execute zero to three single cycle transfers, followed by bursts of any size. The size of the burst is determined by the length of time DREQx# remains asserted. Any DREQx# assertion causes the PEX 8311 to read at least one Lword of data. The only time the PEX 8311 starts or resumes the transfer with a burst is if the address is double Qword-aligned (LA[28:31]=0h).

- After DREQx# is de-asserted, the DMA controller(s) release the Local Bus after the completion of one to two additional Lword Data transfers.

- The transfer are paused on an Lword boundary (LA[30:31]=00b). For a burst, the PEX 8311 reads one additional Lword with BDIP# asserted, then releases the Local Bus after another Lword is read with BDIP# de-asserted and TA# asserted [or the internal Wait State Counter(s) has decrementedto 0].

- If DREQx# is de-asserted while the PEX 8311 is single cycling, the PEX 8311 must complete the current single cycle read and one additional Lword read, before releasing the Local Bus.

- If EOT# is asserted along with DREQx# de-assertion while the PEX 8311 is reading data or waiting (TA# de-asserted) to read data during a burst, the PEX 8311 must read two more Lwords of data before it releases the Local Bus. One during the cycle that EOT# is asserted or when TA# becomes asserted, and one additional Lword with BDIP# de-asserted.

- If EOT# is asserted while waiting to complete a single cycle transfer, the PEX 8311 will complete that transfer and one additional Lword Data transfer before releasing the Local Bus.

Fast Terminate mode (LCS_DMAMODEx[15]=1), Continuous Burst mode (LCS_DMAMODEx[8, 7]=1xb)

In Fast Terminate mode (LCS_DMAMODEx[15]=1), the PEX 8311 defaults into Continuous Burst mode, regardless of the DMA Channel x Continuous Burst Mode bit (LCS_DMAMODEx[7]) setting. With these settings, the PEX 8311 operates the same as Slow Terminate/ Continuous Burst mode, with the following differences:

- BDIP# is never asserted.

- If DREQx# is de-asserted during a single cycle, the PEX 8311 releases the Local Bus after the current read completes, and may or may not need to execute one additional single cycle read. For a burst, the PEX 8311 will read one additional Lword with DREQx# de-asserted and TA# asserted [or the internal Wait State Counter(s) has decremented to 0] or wait for TA# assertion and read the last data before releasing the Local Bus.

- If EOT# is asserted along with DREQx# de-assertion while the PEX 8311 is starting a transfer to read data or is waiting (TA# de-asserted) to read data during a burst, the PEX 8311 must read one additional Lword of data before it releases the Local Bus. The PEX 8311 will complete the final data transfer if TA# is asserted with EOT# or when TA# becomes asserted after EOT# assertion.

    If EOT# is asserted while waiting to complete a single cycle transfer, the PEX 8311 completes that transfer before releasing the Local Bus.

9.5.13.2.4 End of Transfer (EOT#) Input

EOT# is a one-clock wide pulse that ends a DMA transfer. It should be asserted only when the PEX 8311 owns the Local Bus. Depending on whether Fast or Slow Terminate mode is selected, the DMA transfer ends without a BDIP# assertion (Fast Terminate mode) or with BDIP# asserted (Slow Terminate mode). The LCS DMAMODEx[15:14] bits enable and control how the PEX 8311 responds to an EOT# input assertion.

In Fast Terminate mode, if EOT# is asserted while the PEX 8311 receives an external TA# signal assertion, the DMA Controller(s) ends the DMA transfer and releases the Local Bus. In Slow Terminate mode, if EOT# is asserted while the PEX 8311 receives an xternal TA# signal assertion, the DMA Controller(s) ontinues to transfer data to the nearest 16-byte boundary before terminating the DMA transfer.

If Slow Terminate and Burst-4 modes are enabled (LCS_DMAMODEx[15, 7]=00b, respectively), and EOT# is asserted during the Data-Transfer phase of the last four bytes of a 16-byte transfer, the PEX 8311 completes the transfer and performs an additional 16-byte transfer to satisfy the BDIP# de-assertion protocol. Otherwise, it completes the current 16-byte transfer.

Regardless of the BI Mode bit(s) setting with the Fast/ Slow Terminate Mode Select disabled (LCS_DMAMODEx [15, 7]=1xb), the DMA Controller(s) terminates a transfer on an Lword boundary after EOT# is asserted.

For an 8-bit bus, the PEX 8311 terminates after transferring the last byte for the Lword. For a 16-bit bus, the PEX 8311 terminates after transferring the last word for the Lword. In single cycle mode (burst disabled), the transfer is terminated at the next Lword boundary after EOT# occurs. The exception to this is when EOT# occurs on the last four bytes of the Transfer Count setting.

During the descriptor loading on the Local Bus, EOT# assertion causes a complete descriptor load and no subsequent Data transfer; however, this is not recommended. EOT# has no effect when loading the descriptor from the PCIe Bus.

9.5.14 DMA Arbitration

9.5.14.1 DMA Arbitration – C and J Modes

When a DMA transfer is in progress, the PEX 8311 DMA Controller releases control of the Local Bus (de-asserts LHOLD) when any of the following conditions occur:

* DMA FIFO is full (PCI Express-to-Local) or empty (Local-to-PCI Express)
* Direct Slave access is pending (pre-empt from Direct Slave)
* BREQi is enabled and asserted (pre-empt from Direct Master)
* Terminal Count is reached (normal termination)
* EOT# input is enabled and asserted
* Local Bus Latency Timer is enabled (**LCS_MARBR**[16]=1) and expires (**LCS_MARBR**[7:0]=00h)

After LHOLD is de-asserted, it remains de-asserted for a minimum of 2 LCLK periods (idle cycles), after which it can re-assert (in the case of a Preempting Direct Slave Access pending). If the Generic Local Bus is released as a result of the Local Bus Latency Timer expiring, LHOLD remains de-asserted until the Local Bus Pause Timer (**LCS_MARBR**[15:8]) expires.

The PEX 8311 DMA Controller releases its internal PCI Bus to the PCI Express interface when one of the following conditions occur:

* DMA FIFO is empty (PCI Express-to-Local) or full (Local-to-PCI Express)
* Terminal Count is reached (normal termination)
* Grant from PCI Express interface is removed
* Internal PCI Bus Latency Timer expires (**LCS_PCILTR**[7:0]=00h)
* Target Disconnect is received

After the DMA Controller releases the internal PCI Bus, if data remains to be transferred, the controller requests the bus after the pre-programmed number of entries are available in the FIFO, or after 2 clocks (in the case of a Target Retry).

9.5.14.2 DMA Arbitration – M Mode

The PEX 8311 asserts BR# when it is necessary for the device to be the Local Bus Master. Upon receiving BG#, the PEX 8311 waits for BB# to be de-asserted. The PEX 8311 then asserts BB# at the next rising edge of the Local clock after sensing that BB# is de-asserted (no other device is acting as Local Bus Master). The PEX 8311 continues to assert BB# while acting as the Local Bus Master until one of the following conditions occur:

* Local Bus Latency Timer is enabled (**LCS_MARBR**[16]=1) and expires (**LCS_MARBR**[7:0])
* Direct Slave access is pending
* EOT# input is received (if enabled)

The DMA Controller(s) releases control of the PCI Bus when one of the following occurs:

* FIFOs are full or empty
* PCI Bus Latency Timer expires (**LCS_PCILTR**[7:0]) – and loses the PCI GNT# signal
* Target disconnect response is received

The DMA Controller(s) de-asserts PCI REQ# for a minimum of two PCI clocks.

9.5.15   Local Bus DMA Priority

9.5.15.1   Local Bus DMA Priority – C and J Modes

The PEX 8311 supports programmable Local Bus arbitration priority for DMA Channel 0 and Channel 1, when both channels are active (priority set with **LCS_MARBR**[20:19]). Block and DMA Scatter/Gather modes have priority over DMA Demand mode. DMA transfer direction does ***not*** influence DMA channel priority.

There are three types of priorities:

- **Rotational Priority (LCS_MARBR[20:19]=00b)** – Depends on the transfer direction, however, when the starting bus is the same for both DMA channels, in the freshly started DMA, Channel 0 always starts first. Rotational priority does not start unless the ongoing DMA channel Data transfer is interrupted by the Local Bus Latency Timer expiration, preempted by a Direct Slave Data transfer, or another termination occurs – EOT# assertion, DREQ*x*# de-assertion, or BREQi assertion.

  The other DMA channel then owns the Local Bus until the previously described interrupts or terminations occur. Rotational priority occurs each time a DMA channel loses Local Bus ownership, unless one of the DMA channels previously completed its transfer.

- **Channel 0 Priority (LCS_MARBR[20:19]=01b)** – DMA Channel 0 completes the transfer on the Local Bus before Channel 1. If Channel 1 is performing a Data transfer, with Channel 0 set as highest priority and started, Channel 1 continues its transfer until the Local Bus Latency Timer (**LCS_MARBR**[7:0]) expires, preempted by a Direct Slave Data transfer, or another termination occurs – EOT# assertion, DREQ*x*# de-assertion, or BREQi assertion.

  Channel 0 then owns the Local Bus until transfer completion, before Channel 1 can continue the interrupted transfer, unless Channel 1 previously completed its transfer.

- **Channel 1 Priority (LCS_MARBR[20:19]=10b)** – DMA Channel 1 completes its transfer on the Local Bus before Channel 0. If Channel 0 is performing a Data transfer, with Channel 1 set as highest priority and started, Channel 0 continues its transfer until the Local Bus Latency Timer expires, preempted by a Direct Slave Data transfer, or another termination occurs – EOT# assertion, DREQ*x*# de-assertion, or BREQi assertion.

  Channel 1 then owns the Local Bus until transfer completion, before Channel 0 can continue the interrupted transfer, unless Channel 0 previously completed its transfer.

9.5.15.2   Local Bus DMA Priority – M Mode

The PEX 8311 supports programmable Local Bus arbitration priority for DMA Channel 0 and Channel 1, when both channels are active (priority set with **LCS_MARBR**[20:19]). Block and DMA Scatter/Gather modes have priority over DMA Demand mode. DMA transfer direction does ***not*** influence DMA channel priority.

There are three types of priorities:

- **Rotational Priority (LCS_MARBR[20:19]=00b)** – Depends on the transfer direction, however, when the starting bus is the same for both DMA channels, in the freshly started DMA, Channel 0 always starts first. Rotational priority does not start unless the ongoing DMA channel Data transfer is interrupted by the Local Bus Latency Timer expiration, preempted by a Direct Slave Data transfer, or another termination occurs – EOT# assertion or DREQ*x*# de-assertion.

  The other DMA channel then owns the Local Bus until the previously described interrupts or terminations occur. Rotational priority occurs each time a DMA channel loses Local Bus ownership, unless one of the DMA channels previously completed its transfer.

- **Channel 0 Priority (LCS_MARBR[20:19]=01b)** – DMA Channel 0 completes the transfer on the Local Bus before Channel 1. If Channel 1 is performing a Data transfer, with Channel 0 set as highest priority and started, Channel 1 continues its transfer until the Local Bus Latency Timer (**LCS_MARBR**[7:0]) expires, preempted by a Direct Slave Data transfer, or another termination occurs – EOT# assertion or DREQ*x*# de-assertion.

  Channel 0 then owns the Local Bus until transfer completion, before Channel 1 can continue the interrupted transfer, unless Channel 1 previously completed its transfer.

- **Channel 1 Priority (LCS_MARBR[20:19]=10b)** – DMA Channel 1 completes its transfer on the Local Bus before Channel 0. If Channel 0 is performing a Data transfer, with Channel 1 set as highest priority and started, Channel 0 continues its transfer until the Local Bus Latency Timer expires, preempted by a Direct Slave Data transfer, or another termination occurs – EOT# assertion or DREQ*x*# de-assertion.

  Channel 1 then owns the Local Bus until transfer completion, before Channel 0 can continue the interrupted transfer, unless Channel 0 previously completed its transfer.

9.5.16   Local Bus Latency and Pause Timers

9.5.16.1   Local Bus Latency and Pause Timers – C and J Modes

The **LCS** Local Bus Latency and Pause Timers are programmable with the Mode/DMA Arbitration register (**LCS_MARBR**[7:0, 15:8], respectively). When the Local Bus Latency Timer is enabled (**LCS_MARBR**[16]=1) and expires (**LCS_MARBR**[7:0]), the PEX 8311 completes the current Dword transfer and releases LHOLD. After its programmable Pause Timer expires, the PEX 8311 re-asserts LHOLD. The PEX 8311 continues to transfer when it receives LHOLDA.

The DMA transfer is paused by writing 0 to the *Channel Enable* bit for the affected DMA channel (**LCS_DMACSR0/1**[0]=0). To acknowledge the disable, the PEX 8311 receives at least one data from the bus before it stops transferring data. However, this is ***not*** recommended during a burst.

The **LCS** Local Bus Latency Timer starts after the Local Bus is granted to the PEX 8311, and the Local Bus Pause Timer starts after the external Local Bus Arbiter de-asserts LHOLDA.

9.5.16.2   Local Bus Latency and Pause Timers – M Mode

The Local Bus Latency and Pause Timers are programmable with the Mode/DMA Arbitration register (**LCS_MARBR**[7:0, 15:8], respectively). If the Local Bus Latency Timer is enabled (**LCS_MARBR**[16]=1) and expires (**LCS_MARBR**[7:0]), the PEX 8311 completes a Dword transfer up to the nearest 16-byte boundary and releases the Local Bus, de-asserting BB#. After the programmable Pause Timer expires, it arbitrates for the bus by asserting BR#. When the PEX 8311 receives BG#, it asserts BB# and continues to transfer until the FIFO is empty for a PCI-to-Local transfer or full for a Local-to-PCI transfer.

The DMA transfer can be paused by writing 0 to the *Channel Enable* bit for the affected DMA channel (**LCS_DMACSR0/1**[0]=0). To acknowledge the disable, the PEX 8311 receives at least one data from the bus before it stops. However, this is ***not*** recommended during a burst.

The DMA Local Bus Latency Timer starts after the Local Bus is granted to the PEX 8311, and the Local Bus Pause Timer starts after the PEX 8311 de-asserts BB#.

9.5.17   DMA FIFO Programmable Threshold

The PEX 8311 supports programmable DMA FIFO threshold (**LCS_DMATHR**). The **LCS_DMATHR** register can be programmed with any of four different FIFO Full/Empty conditions, for DMA Channel *x* (0 or 1), as defined in Table 9-15. (Refer to the **LCS_DMATHR** register and Table 20-6, "LCS_DMATHR Nibble Values," for further details.)

Table 9-15.   LCS_DMATHR FIFO Threshold

DMA Transfer	Condition	Description
PCI Express-to-Local	DMA Channel *x* FIFO Almost Full	Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for writes.
	DMA Channel *x* FIFO Almost Empty	Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the PCI Express Address to initiate TLP Read requests on the PCI Express interface.
Local-to-PCI Express	DMA Channel *x* FIFO Almost Full	Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the PCI Express Address to initiate TLP Write requests on the PCI Express interface.
	DMA Channel *x* FIFO Almost Empty	Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for reads.

9.5.18   DMA Internal PCI Bus Master/Target Abort

The following describes how the PEX 8311 logic handles internal Master/Target Abort between Local and PCI Express Spaces, as well as Unsupported Requests and Completion Aborts received on the PCI Express interface.

During a DMA transaction on the PCI Express interface and upon encountering either internal Master/Target Abort between Local DMA and PCI Express Address space, or receiving PCI Express UR/CA, the PEX 8311 Master/Target Abort logic enables the PEX 8311 to successfully recover during transfers. The Local Bus Master must clear the *Received Master* or *Target Abort* bit (LCS_PCISR[13 or 12]=0, respectively) and continue by processing the next task, as the bits is set when an abort is encountered. Not clearing the bit prevents the PEX 8311 from initiating PCI Express transactions.

If an internal Master/Target Abort or 256 consecutive Master Retry timeout to the PCI Express Address spaces is encountered during a transfer, the PEX 8311 asserts:

- **C or J mode** – LSERR#, when enabled [LCS_INTCSR[0]=1, which can be used as a Non-Maskable Interrupt (NMI)]

- **M mode** – LINTo#, if enabled (**LCS_INTCSR**[16, 12]=11b, respectively), which can be used as an interrupt

Refer to Chapter 11, "Error Handling," for error handling behavior. The PEX 8311 also flushes the internal Master FIFOs (DMA and Direct Master).

The PEX 8311 DMA channels function independently when a Master/Target Abort occurs. When one DMA channel encounters a Master/Target Abort, the FIFO on the aborted channel is flushed. PCI Express transactions initiation capabilities for both DMA channels are disabled until the *Received Master/Target Abort* bits are cleared (Local Bus register **LCS_PCISR**[13:12]=00b, respectively). However, when the second DMA channel begins a new operation while the first DMA channel is receiving an internal Master/Target Abort, the FIFO contents of the second DMA channel are not affected, and its new or pending Direct Master operations successfully complete. (For Direct Master Master/Target Abort details, refer to Section 9.2.9.)

Note: *In applications in which both DMA channels are used and one of the DMA channels*
           encounters an internal Master/Target Abort, clear the Received Master/Target Abort bits
           *(**LCS_PCISR**[13:12]=00b, respectively), and allow the non-aborted DMA channel to*
           complete its Data transfer before the aborted DMA channel's registers are re-initialized
           and the transfer restarted.

If an internal Master/Target Abort is encountered during a DMA transfer, the PEX 8311 stores the Abort Address into **LCS_PABTADR**[31:0]. The **LCS_PABTADR** register contents are updated for each internal Master/Target Abort. Read and clear the *Received Master/Target Abort* bits before starting a new DMA or Direct Master, Type 0 or Type 1 Configuration transfer (Root Complex mode only).

Table 9-16 defines the PEX 8311's response to Master/Target Abort conditions encountered on the internal PCI Bus between the Local and PCI Express bridges while a DMA transfer is in progress.

Table 9-16.   DMA Mode-Specific Responses to Master/Target/Retry Abort Conditions on Internal PCI Bus

DMA Operating Mode	PEX 8311 Response
Local-to-PCI Express, in Slow Terminate Mode (LCS_DMAMODE0/**1**[15]=0	PEX 8311 immediately releases the internal PCI Bus and sets the *Received Master/Target Abort* bits (LCS_PCISR[13 or 12]=1, respectively). The address of the aborted transaction is saved in the LCS_PABTADR register. The affected DMA channel (and the unaffected DMA channel, if active) continues to read data from the Local Bus until its FIFO is full or the Terminal Count is reached, then sets its *DMA Channel Done* bit (LCS_DMACSR0/**1**[4]=1). Both DMA Channels remain unable to initiate transfers on the internal PCI Bus until software reads and clears the *Received Master/Target Abort* bits (**LCS_PCISR**[13:12]=00b). Once cleared, any transfers pending on the unaffected channel proceed to completion normally.
Local-to-PCI Express, in Fast Terminate Mode (**LCS_DMAMODE0/1**[15]=1)	1. The affected DMA channel immediately halts, and the external Local Bus and internal PCI Bus are released. 2. PEX 8311 writes the Abort address to the **LCS_PABTADR** register. 3. PEX 8311 sets *Received Master* or *Target Abort* bit (**LCS_PCISR**[13 or 12]=1, respectively), as is **LCS_INTCSR**[26 or 25]. 4. PEX 8311 flushes the affected DMA channel's FIFO contents. 5. *DMA Channel Done* bit for the affected DMA channel is set (**LCS_DMACSR0/1**[4]=1). Both DMA channels remain unable to initiate transfers to PCI Express Space until software reads and clears the *Received Master/Target Abort* bits (**LCS_PCISR**[13:12]=00b). Once cleared, any transfer pending on the unaffected channel proceeds to completion normally.
PCI Express-to-Local, Independent of Fast/Slow Terminate Mode (**LCS_DMAMODE0/1**[15]=0 or 1)	1. PEX 8311 releases the internal PCI Bus. 2. PEX 8311 terminates the Burst transfer on the Generic Local Bus. 3. PEX 8311 single cycles the remaining FIFO contents to the Generic Local Bus. 4. PEX 8311 sets the *Received Master/Target Abort* bits (**LCS_PCISR**[13:12]=11b). 5. PEX 8311 sets the *DMA Channel Done* bit for the affected DMA channel (**LCS_DMACSR0/1**[4]=1). Both DMA channels remain unable to initiate transfers on the internal PCI Bus until software reads and clears the *Received Master/Target Abort* bits (**LCS_PCISR**[13:12]=00b). Once cleared, any transfers pending on the unaffected channel proceed to completion normally.
Local-to-PCI Express, with EOT# assertion on Generic Local Bus	Upon encountering an internal Master/Target Abort between the Local DMA and PCI Express Address spaces concurrent with EOT# assertion on the Local Bus, the PEX 8311 terminates the Data transfer on the internal PCI Bus and Local Bus and sets the *DMA Channel Done* bit for the affected DMA channel (**LCS_DMACSR0/1**[4]=1).
PCI Express-to-Local, with EOT# assertion on Generic Local Bus	Upon encountering an internal Master/Target Abort between the Local DMA and PCI Express Address spaces concurrent with EOT# assertion on the Local Bus, the PEX 8311 flushes the DMA PCI Express-to-Local FIFO before encountering the Master/Target Abort.
PCI Express-to-Local Scatter/ Gather, Ring Management with EOT# assertion on the Local Bus	With the EOT# function enabled for the affected DMA channel (**LCS_DMAMODE0/1** [14]=1), EOT# End Link enabled for the affected DMA channel (**LCS_DMAMODE0/1** [19]=1), and the DMA Descriptor Links located on the Local Bus, the PEX 8311 starts the DMA Descriptor load and then transfers data after the *DMA Channel Enable* and *Start* bits are set for the affected DMA channel (**LCS_DMACSR0/1**[0:1]=11b, respectively). Upon receiving the internal Target Abort between Local DMA and PCI Express Address spaces and concurrent with EOT# assertion on the Local Bus during a Scatter/Gather DMA PCI Express-to-Local Data transfer, the PEX 8311 pauses the transfer in response to the Target Abort. The PEX 8311 then flushes the DMA FIFO and sets the *DMA Channel Done* bit for the affected DMA channel (**LCS_DMACSR0/1**[4]=1) after sampling that EOT# is asserted. No further DMA Descriptor load is performed after the *Received Target Abort* bit is cleared (**LCS_PCISR**[12]=0), and the Scatter/Gather DMA transfer is terminated.

9.5.19   Local Bus DMA Data Transfer Modes

9.5.19.1   Local Bus DMA Data Transfer Modes – C and J Modes

The PEX 8311 supports C and J modes with three Local Bus Data Transfer modes:

- Single Cycle – Default data transfer mode
- Burst-4 – Compatible with C and J modes
- Continuous Burst – Provides the highest throughput

Table 9-17 defines the register settings used to select Local Bus Data Transfer modes. It also indicates the data quantity transferred per Address Cycle (ADS#).

Notes: *The BTERM#/BI# ball is referred to as the BTERM# ball in C and J modes, and as the BI# ball in M mode.*

         The BTERM# Input Enable bits (LCS_DMAMODE0/1[7] for Channel x) function as BI Mode bits in M mode.

         The term Burst Forever *was formerly used to describe* Continuous Burst.

Table 9-17.   Local Bus Data Transfer Modes – C and J Modes

Mode	Burst Enable Bit	BTERM# Input Enable Bit	Result
Single Cycle (default)	Disabled (0)	X	One ADS# per data.
Burst-4	Enabled (1)	Disabled (0)	One ADS# per four Data cycles (recommended for i960 and PPC401).
Continuous Burst	Enabled (1)	Enabled (1)	One ADS# per data burst or until BTERM# is asserted.

Note: *"X" is "Don't Care."*

9.5.19.2   Local Bus DMA Data Transfer Modes – M Mode

The PEX 8311 supports M mode with three Local Bus Data Transfer modes:

- Single Cycle – Default data transfer mode
- Burst-4 – Compatible with M mode (MPC850- and MPC860)
- Continuous Burst – Provides the highest throughput

Table 9-18 summarizes the register settings used to select Local Bus Data Transfer modes. It also indicates the data quantity transferred per Address Cycle (TS#).

Notes: *The BTERM#/BI# ball is referred to as the BTERM# ball in C and J modes,
and as the BI# ball in M mode.*

*The BTERM# Input Enable bits (LCS_DMAMODE0/1[7] for Channel x) function
as BI Mode bits in M mode.*

The term Burst Forever was formerly used to describe Continuous Burst.

Table 9-18.   Local Bus Data Transfer Modes – M Mode

Local Bus Data Transfer Modes	Burst Enable Bit	BI Mode Bit	Result
Single Cycle (default)	Disabled (0)	X	One TS# per data.
Burst-4	Enabled (1)	Disabled (0)	One TS# per 16 bytes (recommended for MPC850 or MPC860).
Continuous Burst	Enabled (1)	Enabled (1)	One TS# per data burst or until BI# is asserted.

Note: "X" is "Don't Care."

9.5.19.3   Single Cycle Mode

9.5.19.3.1   Single Cycle Mode – C and J Modes

Single Cycle mode is the default Data Transfer mode. In Single Cycle mode, the PEX 8311 issues one ADS# per data cycle. The starting address for a single cycle Data transfer is on any address.

For single cycle Data transfers, Burst mode is disabled (**LCS_DMAMODE0/1**[8]=0). For a 32-bit Local Bus, when a starting address in a DMA PCI Express-to-Local transfer is *not* aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary.

9.5.19.3.2   Single Cycle Mode – M Mode

Single Cycle mode is the default Data Transfer mode. In Single Cycle mode, the PEX 8311 issues one TS# per data cycle. The starting address for a single cycle Data transfer is on any address. If a starting address in a DMA PCI Express-to-Local transfer is not aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next 4-Dword boundary.

For single cycle Data transfers, Burst mode is disabled (**LCS_DMAMODE0/1**[8]=0). For a 32-bit Local Bus, when a starting address in a DMA PCI Express-to-Local transfer is *not* aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary.

9.5.19.3.3   Partial Data Accesses

Partial Data accesses (not all Byte Enables are asserted) are broken into single cycles. When there is remaining data that is *not* Dword-aligned during DMA PCI Express-to-Local transfers, it results in a single cycle Data transfer.

9.5.19.4   Burst-4 Mode

Burst-4 mode forces the PEX 8311 to perform Data transfers as bursts of four Data cycles (4 Dwords, four 16-bit words, or 4 bytes to a 32-, 16-, or 8-bit bus, respectively).

9.5.19.4.1   Burst-4 Mode – C and J Modes

Burst-4 mode Data transfers are set up by enabling bursting and clearing the *BTERM# Input Enable* bit for the affected DMA channel (**LCS_DMAMODE0/1**[8:7]=10b, respectively).

Burst-4 mode bursting starts on any data boundary and bursts to the next four-data boundary. The first burst starts on any address and moves to the data boundary. The next bursts are four Data cycles. The first or last burst can be less than four Data cycles. The PEX 8311 can continue to burst by asserting ADS# and performing another burst. For a 32-bit Local Bus, when a starting address in a DMA PCI Express-to-Local transfer is *not* aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary. (Refer to Table 9-19.)

Table 9-19.   Burst-4 Mode – C, J, and M Modes

Local Bus Data Width	Burst-4
32 bit	4 Dwords start/stop at a 4-Dword boundary
16 bit	4 words start/stop at a 4-word boundary
8 bit	4 bytes start/stop at a 4-byte boundary

Note: The first or last burst can be less than four Data cycles.

9.5.19.4.2   Burst-4 Mode – M Mode

Burst-4 mode Data transfers are set up by enabling bursting and clearing the *BI Mode* bit for the affected DMA channel (**LCS_DMAMODE0/1**[8:7]=10b, respectively).

Burst-4 mode bursting starts on any data boundary and bursts to the next four-data boundary. The first burst starts on any address and moves to the data boundary. The next bursts are four Data cycles. The first or last burst can be less than four Data cycles. The PEX 8311 can continue to burst by asserting TS# and performing another burst. For a 32-bit Local Bus, when a starting address in a DMA PCI Express-to-Local transfer is *not* aligned to a Dword boundary, the PEX 8311 performs a single cycle until the next Dword boundary. (Refer to Table 9-19.)

9.5.19.4.3   Partial Data (<4 Bytes) Accesses

Partial Data accesses occur when either the first, last, or both (first and last) PCI Express data are unaligned, and the Byte Enables bits are *not* all asserted. For a 32-bit Local Bus, they are broken in single cycles until the next Dword boundary.

9.5.19.5   Continuous Burst Mode

Continuous Burst mode enables the PEX 8311 to perform data bursts of longer than four Data cycles. However, special external interface devices are required that can accept bursts longer than four Data cycles.

For DMA, when Burst-4 mode is implemented with Address Increment disabled (**LCS_DMAMODE0/1**[11]=1), the PEX 8311 defaults to Continuous Burst mode.

9.5.19.5.1   Continuous Burst Mode – C and J Modes

Continuous Burst mode Data transfers are set up by enabling, bursting, and setting the *BTERM# Input Enable* bit for the affected DMA channel (**LCS_DMAMODE0/1**[8:7]=11b, respectively).

The PEX 8311 asserts one ADS# cycle and continues to burst data. If a Slave device requires a new Address cycle (ADS#), it can assert the BTERM# input. The PEX 8311 completes the current Data transfer and stops the burst. The PEX 8311 continues the transfer by asserting ADS# and starting a new burst at the next address.

9.5.19.5.2   Continuous Burst Mode – M Mode

Continuous Burst mode Data transfers are set up by enabling, bursting, and setting the *BI Mode* bit for the affected DMA channel (**LCS_DMAMODE0/1**[8:7]=11b, respectively).

The PEX 8311 asserts one TS# cycle and continues to burst data. If a Slave device requires a new Address cycle (TS#), it can assert the BI# input. The PEX 8311 completes the current Data transfer and stops the burst. The PEX 8311 continues the transfer by asserting TS# and starting a new burst at the next address.

9.5.19.6   Local Bus Read Accesses

For Single Cycle Local Bus Read accesses, when the PEX 8311 is the Local Bus Master, the PEX 8311 reads only bytes corresponding to Byte Enables requested by the PCI Express Read request initiator. For Burst Read cycles, the PEX 8311 passes all bytes and is programmed to:

- Prefetch
- Perform Direct Slave Read Ahead mode
- Generate internal wait states
- Enable external wait control (READY# input)
- Enable type of Burst mode to perform

9.5.20   Local Bus Write Accesses

For Local Bus writes, only bytes specified by a PCI Express transaction initiator or PEX 8311 DMA Controller are written.

9.5.21   Local Bus DMA Data Parity

9.5.21.1   Local Bus DMA Data Parity – C and J Modes

Generation or use of Local Bus Data parity is optional. The Local Bus Parity Check is passive and provides only parity information to the Local processor during DMA transfers.

There is one data parity ball for each byte lane of the PEX 8311 Data bus (DP[3:0]). "Even data parity" is asserted for each lane during Local Bus Reads from the PEX 8311 and during PEX 8311 Master Writes to the Local Bus.

Even data parity is checked for DMA Local Bus Reads. When an error is detected during DMA Local-to-PCI Express transfer, the PEX 8311 sets the *Local Data Parity Check Error Status* bit (**LCS_INTCSR**[7]=1) and asserts an interrupt (LSERR#), when enabled (**LCS_INTCSR**[0, 6]=11b, respectively). This occurs in the Clock cycle following the data being checked.

For applications in which READY# is disabled in the PEX 8311 registers, an external pull-down resistor is required for READY# to allow **LCS_INTCSR**[7] and the LSERR# interrupt to be set and asserted, respectively.

9.5.21.2   Local Bus DMA Data Parity – M Mode

Generation or use of Local Bus data parity is optional. The Local Bus Parity Check is passive and provides only parity information to the Local processor during DMA transfers.

There is one data parity ball for each byte lane of the PEX 8311 Data bus (DP[0:3]). "Even data parity" is asserted for each lane during Local Bus Reads from the PEX 8311 and during PEX 8311 Master Writes to the Local Bus.

Even data parity is checked for DMA Local Bus Reads. When an error is detected during DMA Local-to-PCI Express transfer, the PEX 8311 sets the *Local Data Parity Check Error Status* bit (**LCS_INTCSR**[7]=1) and asserts an interrupt (LINTo#), when enabled (**LCS_INTCSR**[0, 6]=11b, respectively). This occurs in the Clock cycle following the data being checked.

For applications in which TA# is disabled in the PEX 8311 registers, an external pull-down resistor is required for TA# to allow **LCS_INTCSR**[7] and the LINTo# interrupt to be set and asserted, respectively.

9.6   Response to Local Bus FIFO Full or Empty

9.6.1   Response to Local Bus FIFO Full or Empty – C and J Modes

Table 9-20 defines the PEX 8311 response to full and empty Local Bus FIFOs in C and J modes.

Table 9-20.   Response to Local Bus FIFO Full or Empty – C and J Modes

Mode	Data Direction	FIFO	PCI Express Interface	Local Bus
Direct Master Write	Local-to-PCI Express	Full	Normal	De-asserts READY#
		Empty	Normal	Normal
Direct Master Read	PCI Express-to-Local	Full	Normal	Normal
		Empty	Normal	De-asserts READY#
Direct Slave Write	PCI Express-to-Local	Full	Normal	Normal
		Empty	Normal	De-asserts LHOLD or retains the Local Bus, asserts BLAST#[a]
Direct Slave Read	Local-to-PCI Express	Full	Normal	De-asserts LHOLD or retains the Local Bus, asserts BLAST#[a]
		Empty	Normal	Normal
DMA	Local-to-PCI Express	Full	Normal	Asserts BLAST#, de-asserts LHOLD[b]
		Empty	Normal	Normal
	PCI Express-to-Local	Full	Normal	Normal
		Empty	Normal	Asserts BLAST#, de-asserts LHOLD[b]

a.   LHOLD de-assertion depends upon the Local Bus Direct Slave Release Bus Mode bit being set
(**LCS_MARBR**[21]=1).
b.   BLAST# de-assertion depends upon the DMA Channel Fast/Slow Terminate Mode Select bit setting for the
affected DMA channel (**LCS_DMAMODE0/1**[15]).

9.6.2   Response to Local Bus FIFO Full or Empty – M Mode

Table 9-21 defines the PEX 8311 response to full and empty Local Bus FIFOs in M mode.

Table 9-21.   Response to FIFO Full or Empty – M Mode

Mode	Direction	FIFO	PCI Bus	Local Bus
Direct Master Write	Local-to-PCI	Full	Normal	De-asserts TA#, RETRY#[a]
		Empty	De-asserts REQ# (releases the PCI Bus)	Normal[5]
Direct Master Read	PCI-to-Local	Full	De-asserts REQ# or throttles IRDY#[b]	Normal[5]
		Empty	Normal	De-asserts TA#
Direct Slave Write	PCI-to-Local	Full	Disconnects or throttles TRDY#[c]	Normal[5]
		Empty	Normal	Retains the Local Bus
Direct Slave Read	Local-to-PCI	Full	Normal	Retains the Local Bus
		Empty	Throttles TRDY#[d]	Normal[e]
DMA	Local-to-PCI	Full	Normal	Normal[5]
		Empty	De-asserts REQ#	Normal[5]
	PCI-to-Local	Full	De-asserts REQ#	Normal[5]
		Empty	Normal	Normal[5]

a.   RETRY# assertion depends upon the Direct Master Write FIFO Almost Full RETRY# Output Enable bit being set (**LCS_LMISC1**[6]=1).
b.   Throttle IRDY# depends upon the Direct Master PCI Read Mode bit being set (**LCS_DMPBAM**[4]=1).
c.   Throttle TRDY# depends upon the Direct Slave PCI Write Mode bit being set (**LCS_LBRD0**[27]=1).
d.   If PCI Compliance is enabled (**LCS_MARBR**[24]=1), PCI Retry is issued instead of throttling TRDY#.
e.   Release Local Bus ownership per MPC850/MPC860 protocol.

Chapter 10   Configuration Transactions

10.1   Introduction

Configuration requests are initiated only by the Root Complex in a PCI Express-based system. PCI Express devices maintain a Configuration space that is accessed by way of Type 0 and Type 1 Configuration transactions:

* Type 0 Configuration transactions are used to access the **PECS** registers (Type 0 registers). PCI Express Memory-Mapped transactions are used to access the Device-Specific registers, through the **PECS_PCIBASE0** register.

* Type 1 Configuration transactions are used to access the PEX 8311 **LCS PCI** registers in Endpoint mode. In addition, Type 1 Configuration transactions are used to access PEX 8311 downstream devices in Root Complex mode. To access **LCS Control** registers (**Local**, **Runtime**, **DMA**, and **Messaging Queue**), Memory- or I/O-Mapped transactions are used in the **LCS_PCIBAR0** or **LCS_PCIBAR1** registers, respectively, in Endpoint mode. The Local Bus Master can access all **LCS** registers in Endpoint or Root Complex mode, with the CCS# signal asserted during the Local Address phase.

Table 10-1 through Table 10-4 define Configuration address formatting.

Table 10-1.   PCI Express

3124	2319	1816	1512	118	72	10
Bus Number	Device Number	Function Number	*Rsvd*	Extended Register Address	Register Address	*Rsvd*

Table 10-2.   Internal Type 0 Configuration Transactions (at Initiator)

3116		1511	108	72	10	
Device Number single-bit decoding		*Rsvd*	Function Number	Register Number	0	0

Table 10-3.   Internal Type 0 Configuration Transactions (at Target)

3111	108	72	10	
Rsvd	Function Number	Register Number	0	0

Table 10-4.   Internal Type 1 Configuration Transactions

3124	2316	1511	108	72	10	
Rsvd	Bus Number	Device Number	Function Number	Register Number	0	1

10.2   Type 0 Configuration Transactions

The PEX 8311 only responds to Type 0 Configuration transactions on the PCI Express interface (Endpoint mode). A Type 0 Configuration transaction is used to configure the PCI Express Configuration space, and is not forwarded to the PEX 8311 Local Configuration space. The PEX 8311 ignores Type 0 Configuration transactions from downstream devices. Type 0 Configuration transactions always result in the transfer of one DWORD.

A Type 1 Configuration transaction is used to configure the Local Configuration space when operating in Endpoint mode.

When Configuration Write data is poisoned, the data is discarded and a Non-Fatal Error message is generated, when enabled.

10.3   Type 1 Configuration Transactions

Type 1 Configuration transactions are used for device configuration in a hierarchical bus system. Bridges and switches are the only types of devices that respond to Type 1 Configuration transactions.

Type 1 Configuration transactions are used when the transaction is intended for a device residing on a bus other than the one from which the Type 1 request is issued. The PEX 8311 only responds to Type 1 Configuration transactions on the PCI Express interface (Endpoint mode) when the transactions are to the PEX 8311 **LCS PCI** registers. Type 1 PCI Express Configuration transactions are internally converted to Type 0 Configuration transaction.

The *Bus Number* field in a Configuration Transaction request specifies a unique bus in the hierarchy on which the transaction Target resides. The bridge compares the specified bus number with the **PECS_SECBUSNUM** and **PECS_SUBBUSNUM** registers to determine whether to forward a Type 1 Configuration transaction across the bridge.

When a Type 1 Configuration transaction is received on the upstream interface, the following tests are applied, in sequence, to the *Bus Number* field to determine how the transaction is handled:

- If the *Bus Number field* is equal to the **PECS_SECBUSNUM** register value, and the conditions for converting the transaction into a special cycle transaction are met, the PEX 8311 forwards the Configuration request to the downstream device (secondary interface) as a special cycle transaction. If the conditions are not met, the PEX 8311 forwards the Configuration request to the downstream device as a Type 0 Configuration transaction.

- If the *Bus Number* field is not equal to the **PECS_SECBUSNUM** register value but is within the range of the **PECS_SECBUSNUM** and **PECS_SUBBUSNUM** (inclusive) registers, the Type 1 Configuration request is specifying a bus located behind the bridge. In this case, the PEX 8311 forwards the Configuration request to the downstream device as a Type 1 Configuration transaction.

- If the *Bus Number* field does not satisfy the above criteria, the Type 1 Configuration request is specifying a bus that is not located behind the bridge. In this case, the Configuration request is invalid.

  – If the upstream interface is PCI Express, a completion with Unsupported Request status is returned.

  – If the upstream interface is the Generic Local Bus, the Configuration request is internally ignored, resulting in a Master Abort. LSERR# (C or J mode) or LINTo# (M mode) is asserted on the Local Bus, when enabled (**LCS_INTCSR**[0]=1).

Note: *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.*

The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.

10.4   Type 1-to-Type 0 Conversion

The PEX 8311 performs a Type 1-to-Type 0 conversion when the Type 1 transaction is generated on the primary interface and is intended for a device attached directly to the downstream bus (*for example*, PCI Express Type 1 Configuration accesses to the **LCS PCI** registers are internally converted to Type 0 accesses). The PEX 8311 must first convert the Type 1 Configuration transaction to Type 0, for the device to be able to respond to it.

Type 1-to-Type 0 conversions are performed only in the downstream direction. The PEX 8311 only generates Type 0 Configuration transactions on the secondary interface, never on the primary interface.

Note: *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus in Root Complex mode.*

The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.

10.4.1   Type 1-to-Type 0 Conversion – Endpoint Mode

The PEX 8311 internally converts a Type 1 transaction on the PCI Express interface to a Type 0 transaction, to provide accessibility to the **LCS PCI** registers when the following are true:

- Type 1 *Bus Number* field of the Configuration request is equal to the **PECS_SECBUSNUM** register value
- Conditions for conversion to a special cycle transaction are not met

The PEX 8311 then performs the following on the Local Bus interface:

1. Clears Address bits AD[1:0] to 00b.
2. Derives Address bits AD[7:2] directly from the Configuration request *Register Address* field.
3. Derives Address bits AD[10:8] directly from the Configuration request *Function Number* field.
4. Clears Address bits AD[15:11] to 0h.
5. Decodes the *Device Number* field and set a single Address bit, AD[20], during the Address phase.
6. Verifies that the *Extended Register Address* field in the configuration request is zero (0h). When the value is non-zero, the PEX 8311 does not forward the transaction, and treats it as an Unsupported request on the PCI Express interface, and a received Master Abort on the internal PCI Bus.

Type 1-to-Type 0 transactions are performed as Non-Posted transactions.

Perform Memory- or I/O-Mapped accesses to access the remainder of the **LCS** registers (**Local**, **Runtime**, **DMA**, and **Messaging Queue**) on the PCI Express interface, through the **LCS_PCIBAR0** or **LCS_PCIBAR1** register.

10.4.2   Type 1-to-Type 0 Conversion – Root Complex Mode

The Local Bus Master configures the **LCS** registers (**Type 1 PCI**, **Local**, **Runtime**, and **DMA**) by Direct Master access, using the CCS# Local Bus ball. Type 0 Configuration accesses must be generated internally by the Local Bus Master, to configure the PCI Express Configuration space. Type 1 Configuration accesses must be generated internally by the Local Bus Master, to configure downstream devices on the PCI Express interface. If required, the internal Type 1 Configuration access is converted to Type 0 on the PCI Express interface of the PEX 8311 bridge.

10.4.2.1   Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)

When the *Configuration Enable* bit is set (**LCS_DMCFGA**[31]=1), a Configuration access is made internally to the PCI Express interface. In addition to enabling this bit, all register information must be provided. (Refer to the **LCS_DMCFGA** register.) The Register Number and Device Number bits (**LCS_DMCFGA**[7:2, 15:11], respectively) must be modified and a new Direct Master Read/Write cycle must be performed at the Direct Master I/O Base address for each Configuration register. Type 0 Configuration transactions are used to perform accesses to the **PECS** registers. Type 1 Configuration transactions are used to access other **PECS** registers of devices downstream from the PEX 8311. Before performing Non-Configuration cycles (plain I/O accesses), the Configuration Enable bit must be cleared (**LCS_DMCFGA**[31]=0).

When the PCI Configuration Address register selects a Type 0 command, **LCS_DMCFGA**[10:0] are copied to Address bits [10:0]. **LCS_DMCFGA**[15:11] (Device Number) are translated into a single bit being set in PCI Express Address bits [31:11]. The PEX 8311 PCI Express Bridge Configuration Access Select (IDSEL) is internally hardwired to **LCS_DMCFGA**[24]. In addition, PCI Express Address bit [24], device Dh, must be programmed into the **LCS_DMCFGA**[15:11] register before Type 0 Configuration accesses can begin.

For a Type 1 command, **LCS_DMCFGA**[23:0] are copied to PCI Express Address bits [23:0]. The PCI Express Address bits [31:24] are cleared to 0. A Configuration Read or Write Command Code is output with the address during the PCI Express Address cycle. (Refer to the **LCS_DMCFGA** register.)

For Writes, Local data is loaded into the Write FIFO and READY# (C or J mode) or TA# (M mode) is returned. For Reads, the PEX 8311 holds READY# (C or J mode) or TA# (M mode) de-asserted while receiving a Dword from the PCI Express interface.

Note: *Per the PCI Express Base 1.0a, the Type 0 and Type 1 Configuration cycles can only be preformed by upstream devices. Therefore, the PEX 8311 supports Type 0 and Type 1 Configuration access generation only in Root Complex mode (ROOT_COMPLEX#=0).*

10.4.2.1.1   Direct Master Type 0 Configuration Cycle Example

To perform a Type 0 Configuration cycle to the PEX 8311 PCI Express **LCS** registers, device on internal AD[24]:

1. PEX 8311 must be configured to allow Direct Master access to the PEX 8311 internal PCI Bus interface. The PEX 8311 must also be enabled to master the internal PCI Bus interface (**LCS_PCICR**[2]=1).

   In addition, Direct Master Memory and I/O access must be enabled (**LCS_DMPBAM**[1:0]=11b).

2. Local memory map selects the Direct Master range. For this example, use a range of 1 MB:

   1 MB = 2^{20} = 0010_0000h

3. Value to program into the Range register is two's complement of 0010_0000h:

   LCS_DMRR = FFF0_0000h

4. Local memory map determines the Local Base Address for the Direct Master-to-PCI Express I/O Configuration register. For this example, use 4000_0000h:

   LCS_DMLBAI = 4000_0000h

5. The PCI device and PCI Configuration register that the PCI Configuration cycle is accessing must be known. In this example, the internal AD[24] (logical device #13=0Dh) is used, as it is internally hardwired and connected to the PCI Express interface. Also, access **LCS_PCIBAR0** (the fourth register, counting from 0; use Table 19-5, "PCI-Compatible Type 1 Configuration Register Map," for reference). Set **LCS_DMCFGA**[31, 23:0], as defined in Table 10-5.

After these registers are configured, a single Local Master Memory cycle to the I/O Base address is necessary to generate an internal Configuration Read or Write cycle within the PEX 8311. The PEX 8311 takes the Local Bus Master Memory cycle and checks for the *Configuration Enable* bit (**LCS_DMCFGA**[31]). When set to 1, the PEX 8311 internally converts the current cycle to a PCI Configuration cycle, using the **LCS_DMCFGA** register and Write/Read signal (C or J mode – LW/R#; M mode – RD/WR#).

Table 10-5.   Direct Master Configuration Cycle Example LCS_DMCFGA[31, 23:0] Settings

Bits	Description	Value
1:0	Type 0 Configuration.	00b
7:2	Register Number. Fourth register. Must program a "4" into this value, beginning with bit 2.	0001_00b
10:8	Function Number.	000b
15:11	Device Number *n* - 11, where *n* is the value in AD[*n*] = 24 - 11 = 13.	0110_1b
23:16	Bus Number.	00h
31	Configuration Enable.	1

10.4.2.1.2   Direct Master Type 1 Configuration Cycle Example

The PEX 8311 forwards an internally generated Type 1 transaction to a Type 0 transaction on the PCI Express interface when the following is true during the access:

- Address bits AD[1:0] are set to 01b.
- Type 1 Configuration Request Bus Number field (AD[23:16]) is equal to the **PECS_SECBUSNUM** register value.
- Bus command on the internal PCI Bus is a Configuration Read or Write.
- Type 1 Configuration Request *Device Number* field (AD[15:11]) is zero (00h). When the field is non-zero, the transaction is ignored, resulting in a Master Abort. Local Bus LSERR# (C or J mode) or LINTo# (M mode) is asserted to indicate a Master Abort condition, when enabled (**LCS_INTCSR**[0]=1).

The PEX 8311 then creates a PCI Express Configuration request according to the following steps:

1. Sets the request Type field to Configuration Type 0.
2. Derives the *Register Address* field [7:2] directly from the Configuration Request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Derive the *Function Number* field [18:16] directly from the Configuration Request *Function Number* field.
5. Derives the *Device Number* field [23:19] directly from the Configuration Request *Device Number* field (forced to zero).
6. Derives the *Bus Number* field [31:24] directly from the Configuration Request *Bus Number* field.

Type 1 to Type 0 transactions are performed as non-posted (delayed) transactions.

10.5   Type 1-to-Type 1 Forwarding

Type 1-to-Type 1 transaction forwarding provides a hierarchical Configuration mechanism when two or more levels of bridges/switches are used. When the PEX 8311 detects a Type 1 Configuration transaction intended for a PCI Bus downstream from the downstream bus, it forwards the transaction unchanged to the downstream bus.

In this case, the transaction target does not reside on the secondary interface, but is located on a bus segment further downstream. Ultimately, this transaction is converted to a Type 0 or special cycle transaction by a downstream bridge/switch device.

Note: *The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.*

10.5.1   Type 1-to-Type 1 Forwarding – Root Complex Mode

The PEX 8311 forwards a Type 1 transaction to a Type 1 transaction on the PCI Express interface, when the following are true during the access:

- Address bits AD[1:0] are set to 01b.
- Value specified by the Bus Number field is within the range of bus numbers between the **PECS_SECBUSNUM** (exclusive) and the **PECS_SUBBUSNUM** (inclusive).
- Bus command on the internal PCI Bus is a Configuration Read or Write.

The PEX 8311 then creates a PCI Express Configuration request according to the following steps:

1. Sets the request Type field to Configuration Type 1.
2. Derives the *Register Address* field [7:2] directly from the Configuration Request *Register Address* field.
3. Clears the *Extended Register Address* field [11:8] to 0h.
4. Derives the *Function Number* field [18:16] directly from the Configuration Request *Function Number* field.
5. Derives the *Device Number* field [23:19] directly from the Configuration Request *Device Number* field.
6. Derives the *Bus Number* field [31:24] directly from the Configuration Request *Bus Number* field.

Type 1-to-Type 1 Forwarding transactions are performed as Non-Posted (Delayed) transactions.

10.6   Type 1-to-Special Cycle Forwarding

The Type 1 Configuration mechanism is used to generate special cycle transactions in hierarchical systems. When acting as a target, the PEX 8311 ignores special cycle transactions, and does not forward the transactions to the PCI Express interface.

- In Endpoint mode, special cycle transactions can only be generated in the downstream direction (PCI Express to the Local PCI Configuration space)

- In Root Complex mode, special cycle transactions are also generated in the downstream direction (Direct Master Type 1 transactions to PCI Express)

Note: The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus in Root Complex mode.

The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.

A Type 1 Configuration Write request on the PCI Express interface is converted to a special cycle on the internal interface to the PEX 8311 **LCS PCI** registers, when all the following conditions are met:

- Type 1 Configuration request *Bus Number* field is equal to the **PECS_SECBUSNUM** register value.

- *Device Number* field is all ones (1h)

- *Function Number* field is all ones (1h)

- *Register Address* field is all zeros (0h)

- *Extended Register Address* field is all zeros (0h)

When the PEX 8311 initiates the transaction on the internal PCI Bus, the bus command is converted from a Configuration Write to a special cycle. The Address and Data fields are forwarded, unchanged, from PCI Express to the internal PCI Bus. Because the PEX 8311 does ***not support*** internal special cycles, a Master Abort is generated. After the Master Abort is detected, a Successful Completion TLP is returned to the PCI Express.

10.7   PCI Express Enhanced Configuration Mechanisms

The PCI Express Enhanced Configuration mechanism adds four extra bits to the Register Address field to expand the space to 4,096 bytes. The PEX 8311 forwards configuration transactions only when the Extended Register Address bits are all zeros (0h). This prevents address aliasing for Direct Master Type 0/Type 1 Configuration accesses, which do not support Extended Register Addressing.

When a Configuration transaction targets the PEX 8311 **LCS PCI** register and retains a non-zero value in the Extended Register Address, the PEX 8311 treats the transaction as if it received a Master Abort on the internal PCI Bus.

The PEX 8311 then performs the following:

1. Sets the appropriate status bits for the destination bus, as if the transaction executed and received a Master Abort

2. Generates a PCI Express completion with Unsupported Request status

10.7.1   Memory-Mapped Indirect – Root Complex Mode Only

In Root Complex mode, the PEX 8311 provides the capability for a Local Bus Master (LCPU or similar) to access downstream PCI Express Configuration registers using Direct Master Memory-Mapped transactions. The 4-KB region of the Memory range defined by the **PECS_PCIBASE0** register is used for this mechanism. Memory Reads and Writes to **PECS_PCIBASE0**, offsets 2000h to 2FFFh, result in a PCI Express Configuration transaction. The transaction address is determined by the **PECS_ECFGADDR** register. This Address register format is defined in Table 10-6.

After the **PECS_ECFGADDR** register is programmed to point to a particular device, the entire 4-KB Configuration space of a PCI Express endpoint is directly accessed, using Memory Read and Write transactions. Only single DWORDs are transferred during Enhanced Configuration transactions.

Table 10-6.   PECS_ECFGADDR Address Register Format

31	3028	2720	1915	1412	110
Enhanced Enable	*Rsvd*	Bus Number	Device Number	Function Number	*Rsvd*

10.8   Configuration Retry Mechanism

10.8.1   Configuration Retry Mechanism – Endpoint Mode

The PEX 8311 supports returning completions for Configuration requests that target the **LCS PCI** registers prior to the Completion Timeout Timer expiration in the Root Complex. This requires the PEX 8311to take ownership of Configuration requests forwarded across the internal PCI Bus:

- When the Configuration request to the **LCS PCI** registers successfully completes prior to the Completion Timeout Timer expiration, the PEX 8311 returns a completion with Successful Status to the PCI Express interface.

- When the Configuration request to the **LCS PCI** registers encounters an error condition prior to the Completion Timeout Timer expiration, the PEX 8311 returns an appropriate error completion to the PCI Express interface.

- When the Configuration request to the **LCS PCI** registers does not complete, either successfully or with an error, prior to Completion Timeout Timer expiration, the PEX 8311 returns a completion with Configuration Retry Status (CRS) to the PCI Express interface.

After the PEX 8311 returns a completion with CRS to PCI Express, the PEX 8311 continues to internally keep the configuration transaction alive, until at least one DWORD is transferred. The PEX 8311 Retries the transaction until it completes internally, or until the maximum number of retries is reached.

When another **PECS-to-LCS PCI** registers transaction is detected while the previous transaction is being Retried, a completion with CRS is immediately returned.

When the configuration transaction internally completes after the return of a completion with CRS on PCI Express, the PEX 8311 discards the completion information. PCI Express devices that implement this option are also required to implement bit 15 of the **PECS_DEVCTL** register as the *Bridge Configuration Retry Enable* bit.

When this bit is cleared, the PEX 8311 does not return a completion with CRS on behalf of Configuration requests that targeted the **LCS PCI** registers. The lack of a completion is to result in eventual Completion Timeout at the Root Complex.

By default, the PEX 8311 does not return CRS for Configuration requests for access performed to the **LCS PCI** registers. This can result in lengthy completion delays that must be comprehended by the Completion Timeout value in the Root Complex.

10.8.2 Configuration Retry Mechanism – Root Complex Mode

In Root Complex mode, the PEX 8311 can detect a completion with CRS status from a downstream PCI Express device. The **PECS_DEVSPECCTL** register *CRS Retry Control* field determines the PEX 8311 response in Root Complex mode when a Direct Master Type 1-to-PCI Express Configuration transaction is terminated with a Configuration Request Retry status, as defined in Table 10-7 (C or J mode) and Table 10-8 (M mode).

Table 10-7. CRS Retry Control – C or J Mode

CRS Retry Control Field	Response
00b	Retry once after 1s. When another CRS is received, Target Abort is internally generated. Local Bus LSERR# is asserted, when enabled (**LCS_INTCSR**[0]=1).
01b	Retry eight times, once per second. When another CRS is received, Target Abort is internally generated. Local Bus LSERR# is asserted, when enabled (**LCS_INTCSR**[0]=1).
10b	Retry once per second until successful completion.
11b	*Reserved*

Table 10-8. CRS Retry Control – M Mode

CRS Retry Control Field	Response
00b	Retry once after 1s. When another CRS is received, Target Abort is internally generated. Local Bus LINTo# is asserted, when enabled (**LCS_INTCSR**[0]=1).
01b	Retry eight times, once per second. When another CRS is received, Target Abort is internally generated. Local Bus LINTo# is asserted, when enabled (**LCS_INTCSR**[0]=1).
10b	Retry once per second until successful completion.
11b	*Reserved*

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Chapter 11   Error Handling

11.1   Endpoint Mode Error Handling

When the PEX 8311 detects errors, it sets the appropriate error status bits [Conventional PCI Error bit(s) and PCI Express Error Status bit(s)], and optionally generates an error message on the PCI Express interface. Each error condition has a default error severity level, and a corresponding error message generated on the PCI Express interface.

Error message generation on the PCI Express interface is controlled by four **PECS** Control bits:

* **PECS_PCICMD** register *Internal SERR# Enable* bit
* **PECS_DEVCTL** register *Fatal Error Reporting Enable* bit
* **PECS_DEVCTL** register *Non-Fatal Error Reporting Enable* bit
* **PECS_DEVCTL** register *Correctable Error Reporting Enable* bit

Error message generation on the PCI Express interface is also controlled by two **LCS** register Control bits:

* **LCS_PCICR** register *Internal SERR# Enable* bit
* **LCS_PCICR** register *Parity Error Response Enable* bit

PCI Express ERR_FATAL messages are enabled for transmission when the *Internal SERR# Enable* or *Fatal Error Reporting Enable* bit is set. ERR_NONFATAL messages are enabled for transmission when the *Internal SERR# Enable* or *Non-Fatal Error Reporting Enable* bit is set. ERR_COR messages are enabled for transmission when the *Correctable Error Reporting Enable* bit is set.

The **PECS_DEVSTAT** register *Fatal Error Detected*, *Non-Fatal Error Detected*, and *Correctable Error Detected* status bits are set for the corresponding errors on the PCI Express, regardless of the error Reporting Enable bits.

11.1.1 PCI Express Originating Interface (PCI Express-to-Local Bus)

This section describes error support for transactions that originate on the PCI Express interface, and that targeted to the PEX 8311 Local Configuration space, as well as the Local Bus. When a Write request or Read Completion is received with a poisoned TLP, the entire data payload of the PCI Express transaction must be considered as corrupt. Invert the parity for data when completing the transaction.

Table 11-1 defines the translation a bridge must perform when it forwards a Non-Posted PCI Express request (Read or Write) to the PEX 8311 Local Configuration space or Local Bus, and the request is immediately completed, either normally or with an error condition. The PEX 8311 internal PCI Bus error condition status bits are checked in the **LCS_PCISR** register. Internal error status bits are set, regardless of respective error interrupt enable bit values.

Table 11-1.   Translation Performed when Bridge Forwards Non-Posted PCI Express Request

Immediate Local or Internal PCI Bus Termination	PCI Express Completion Status
Data Transfer with Parity error (Reads)	Successful (poisoned TLP)
Completion with Parity error (Non-Posted Writes)	Unsupported Request
Internal Master Abort (Abort to Local Address space)	Unsupported Request
Internal Target Abort (Abort to Local Address space)	Completer Abort

11.1.1.1 Received Poisoned TLP

When the PEX 8311 PCI Express interface receives a Write request or Read Completion with poisoned data, the following occur:

- **PECS_PCISTAT** and **LCS_PCISR** register *Detected Parity Error* bits are set.
- **PECS_PCISTAT** register *Master Data Parity Error* bit is set when the poisoned TLP is a Read Completion and the **PECS_PCICMD** register *Parity Error Response Enable* bit is set.
- ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:
  - **PECS_PCICMD** and **LCS_PCICR** register Internal SERR# Enable bits are set –or–
  - **PECS_DEVCTL** register Non-Fatal Error Reporting Enable bit is set
- **PECS_PCISTAT** and **LCS_PCISR** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bits are set.
- Parity bit associated with each DWORD of data is inverted.
- For a poisoned Write request, the **PECS_SECSTAT** register *Secondary Master Data Parity Error* bit is set when the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set,
- Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.1.1.2　Internal PCI Bus Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PEX 8311 Local Bus and an Uncorrectable Internal error is detected.

11.1.1.2.1　Immediate Reads

When the PEX 8311 forwards a Read request (I/O, Memory, or Configuration) from the PCI Express to the Local Bus and detects an Uncorrectable Data error on the internal PCI Bus while receiving an immediate response from the completer (Local Address spaces, Local Configuration space, or Local Bus Target), the following occur.

1. **PECS_SECSTAT** register *Secondary Master Data Parity Error* bit is set when the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set.

2. **PECS_SECSTAT** register *Secondary Detected Parity Error* bit is set.

3. Parity Error signal is asserted on the internal PCI Bus interface when the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set.

4. **LCS Interrupt Control/Status** register *Local Data Parity Check Error* bit is set (**LCS_INTCSR**[7]=1), when enabled (**LCS_INTCSR**[6]=1).

5. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

After detecting an Uncorrectable Data error on the destination bus for an Immediate Read transaction, the PEX 8311 continues to fetch data until the Byte Count is satisfied or the target ends the transaction. When the PEX 8311 creates the PCI Express completion, it forwards it with Successful Completion and poisons the TLP.

11.1.1.2.2　Posted Writes

The PEX 8311 ignores Local Bus Parity errors asserted by Local Bus Targets. When the PEX 8311 detects a Parity error asserted by the Local Address space on the internal PCI Bus while forwarding a non-poisoned Posted Write transaction from PCI Express-to-Local Bus, the following occur:

1. **PECS_SECSTAT** register *Secondary Master Data Parity Error* bit is set when the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set.

2. ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:

   - **PECS_PCICMD** and **LCS_PCICR** register *Internal SERR# Enable* bits are set –or–
   - **PECS_DEVCTL** register *Non-Fatal Error Reporting Enable* bit is set

3. **PECS_PCISTAT** and **LCS_PCISR** register *Signaled System Error* bits are set when the *Internal SERR# Enable* bits are set.

4. After the error is detected, remainder of the data is forwarded.

5. **LCS_PCISR** register *Detected Parity Error* bit is set.

6. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.1.1.2.3   Non-Posted Writes

The PEX 8311 ignores Local Bus Parity errors asserted by Local Bus Targets. When the PEX 8311 detects a Parity error asserted by the Local Address space on the internal PCI Bus while forwarding a non-poisoned Non-Posted Write transaction from PCI Express-to-Local Bus, the following occur:

1. **PECS_SECSTAT** register *Secondary Master Data Parity Error* bit is set when the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set.

2. ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:

   • **PECS_PCICMD** and **LCS_PCICR** register *Internal SERR# Enable* bits are set –or–

   • **PECS_DEVCTL** register *Non-Fatal Error Reporting Enable* bit is set

3. **PECS_PCISTAT** and **LCS_PCISR** register *Signaled System Error* bits are set when the *Internal SERR# Enable* bits are set.

4. After the error is detected, remainder of the data is forwarded.

5. **LCS_PCISR** register *Detected Parity Error* bit is set.

6. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.1.1.3   Internal PCI Bus Address Errors

When the PEX 8311 forwards transactions from PCI Express-to-Local Bus, PCI Express Address errors are internally reported by Parity and System Error signal assertion. When the PEX 8311 detects an internal System Error signal asserted, the following occur:

1. **PECS_SECSTAT** register *Secondary Received System Error* bit is set.

2. ERR_FATAL message is generated on the PCI Express interface, when the following conditions are met:

    • **PECS_BRIDGECTL** register *Secondary Internal SERR# Enable* bit is set

    • **PECS_PCICMD** and **LCS_PCICR** register *Internal SERR# Enable* bits are set or **PECS_DEVCTL** register *Fatal Error Reporting Enable* bit is set

3. **PECS_PCISTAT** and **LCS_PCISR** register *Signaled System Error* bits are set when the *Secondary Internal SERR# Enable* and *Internal SERR# Enable* bits are set.

4. **LCS_PCISR** register *Detected Parity Error* and *Signaled System Error* bits are set when forwarded Address Parity was internally detected, when enabled.

5. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.1.1.4   Internal PCI Bus Master Abort on Posted Transaction

When a Posted Write transaction forwarded from PCI Express-to-Local Bus results in a Master Abort on the internal PCI Bus (**LCS_PCISR**[11]), the following occur:

1. Entire transaction is discarded.

2. **PECS_SECSTAT** register *Secondary Received Master Abort* bit is set.

3. ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:

    • **PECS_BRIDGECTL** register Master Abort Mode bit is set

    • **PECS_PCICMD** register *Internal SERR# Enable* bit or **PECS_DEVCTL** register *Non-Fatal Error Reporting Enable* bit is set

4. **PECS_PCISTAT** register *Signaled System Error* bit is set when the *Master Abort Mode* and *Internal SERR# Enable* bits are set.

11.1.1.5   Internal PCI Bus Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-Local Bus results in a Master Abort on the internal PCI Bus, the following occur:

1. Completion with Unsupported Request status is returned on the PCI Express.

2. **PECS_SECSTAT** register *Secondary Received Master Abort* bit is set.

11.1.1.6   Internal PCI Bus Target Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in a Target Abort on the internal PCI Bus (**LCS_PCISR**[11]), the following occur:

1. Entire transaction is discarded.

2. **PECS_SECSTAT** register *Secondary Received Target Abort* bit is set.

3. ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:
   - **PECS_PCICMD** register *Internal SERR# Enable* bit is set –or–
   - **PECS_DEVCTL** register *Non-Fatal Error Reporting Enable* bit is set

4. **PECS_PCISTAT** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bit is set.

5. **LCS_PCISR** register *Signaled Target Abort* bit is set (**LCS_PCISR**[11]=1).

11.1.1.7   Internal PCI Bus Target Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in a Target Abort on the internal PCI Bus (**LCS_PCISR**[11]), the following occur:

1. Completion with Completer Abort status is returned on the PCI Express.

2. **PECS_SECSTAT** register *Secondary Received Target Abort* bit is set.

3. **PECS_PCISTAT** and **LCS_PCISR** register *Signaled Target Abort* bits are set.

4. ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:
   - **PECS_PCICMD** register *Internal SERR# Enable* bit is set –or–
   - **PECS_DEVCTL** register *Non-Fatal Error Reporting Enable* bit is set

5. **PECS_PCISTAT** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bits are set.

6. **LCS_PCISR** register *Signaled Target Abort* bit is set (**LCS_PCISR**[11]=1).

11.1.1.8   Internal PCI Bus Retry Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in the maximum number of internal PCI Bus Retries (Local Retries) (selectable in the **PECS_PCICTL** register), the following occur:

1. Remaining data is discarded.

2. **PECS_IRQSTAT** register *PCI Express-to-Local Retry Interrupt* bit is set.

11.1.1.9   Internal PCI Bus Retry Abort on Non-Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in the maximum number of internal PCI Bus Retries (Local Retries) (selectable in the **PECS_PCICTL** register), the following occur:

1. Completion with Completer Abort status is returned on the PCI Express.
2. **PECS_IRQSTAT** register *PCI Express-to-Local Retry Interrupt* bit is set.
3. **PECS_PCISTAT** and **LCS_PCISR** register *Signaled Target Abort* bits are set.

11.1.2   Local Bus Originating Interface (Internal to PCI Express)

This section describes error support for transactions that cross the PEX 8311 when the originating side is the Local Bus, and the destination side is PCI Express. The PEX 8311 supports TLP poisoning as a transmitter to permit proper forwarding of Parity errors that occur on the Local Bus or PEX 8311 internal PCI Bus. Posted Write data received from the Local Bus with bad parity is forwarded to PCI Express as a Poisoned TLPs.

Table 11-2 provides the error forwarding requirements for Uncorrectable Data errors detected by the PEX 8311 when a transaction targets the PCI Express interface.

Table 11-3 describes the bridge behavior on an internal PCI Bus Delayed transaction that is forwarded by the PEX 8311 to PCI Express as a Memory Read or I/O Read/Write request, and the PCI Express interface returns a completion with UR or CA status for the request.

Table 11-2.   Error Forwarding Requirements

Received Local or Internal PCI Bus Error	Forwarded PCI Express Error
Write with Parity error	Write request with poisoned TLP
Read Completion with Parity error in Data phase	Read completion with poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write completion with Completer Abort status

Table 11-3.   Bridge Behavior on Internal PCI Bus Delayed Transaction

PCI Express Completion Status	Internal PCI Bus Immediate Response to Local Bus	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory Read or I/O Read)	Internal Target Abort	Normal completion, return FFFF_FFFFh
Unsupported Request (on I/O Write)	Internal Target Abort	Normal completion
Completer Abort	Internal Target Abort	

11.1.2.1   Received Internal Errors

11.1.2.1.1   Uncorrectable Data Error on Non-Posted Write

When a Non-Posted Write is addressed such that it crosses the PEX 8311 bridge, and the PEX 8311 detects an Uncorrectable Data error on the internal PCI Bus, the following occur:

1. **PECS_SECSTAT** register *Secondary Detected Parity Error* status bit is set.
2. If the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set, the transaction is discarded and not forwarded to PCI Express. The Parity Error signal is asserted on the internal PCI Bus.
3. If the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is not set, the data is forwarded to PCI Express as a poisoned TLP. Also, the **PECS_PCISTAT** register *Master Data Parity Error* bit is set when the **PECS_PCICMD** register *Parity Error Response Enable* bit is set. The Parity Error signal is not asserted on the internal PCI Bus.
4. **LCS_PCISR** register *Master Data Parity Error* bit is set.
5. **LCS_PCISR** register *Detected Parity Error* bit is set.
6. **LCS Interrupt Control/Status** register *Local Data Parity Error Check* bit is set, when enabled (**LCS_INTCSR**[6]=1), and Local Data Parity is detected.
7. Local Bus System Error signal (C or J mode – **LSERR#**; M mode – **LINTo#**) is asserted, when enabled (**LCS_INTCSR**[0]=1), and Local Data Parity and internal Parity Error are detected.

11.1.2.1.2   Uncorrectable Data Error on Posted Write

When the PEX 8311 detects an Uncorrectable Data error on the internal PCI Bus for a Posted Write transaction from the Local Bus, the following occur:

1. Internal Parity Error signal is asserted, when the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set.
2. **PECS_SECSTAT** register *Secondary Detected Parity Error* status bit is set.
3. Posted Write transaction is forwarded to PCI Express as a poisoned TLP.
4. **PECS_PCISTAT** register *Master Data Parity Error* bit is set when the **PECS_PCICMD** register *Parity Error Response Enable* bit is set.
5. **LCS_PCISR** register *Master Data Parity Error* bit is set.
6. **LCS_PCISR** register *Detected Parity Error* bit is set.
7. **LCS Interrupt Control/Status** register *Local Data Parity Error Check* bit is set, when enabled (**LCS_INTCSR**[6]=1) and Local Data Parity is detected.
8. Local Bus System Error signal (C or J mode – **LSERR#**; M mode – **LINTo#**) is asserted, when enabled (**LCS_INTCSR**[0]=1), and Local Data Parity and internal Parity error are detected.

11.1.2.1.3   Uncorrectable Data Error on Internal Delayed Read Completions

When the PEX 8311 forwards a non-poisoned Read Completion from PCI Express-to-Local Bus, and it detects the internal Parity Error signal asserted, the remainder of the completion is forwarded.

When the PEX 8311 forwards a poisoned Read Completion from PCI Express-to-Local Bus, the PEX 8311 proceeds with the previously mentioned actions when it detects the internal Parity Error signal asserted internally by the PCI Master, but no error message is generated on the PCI Express interface. Error conditions are passed to the Local Bus when the following occur:

1. **LCS_PCISR** register *Master Data Parity Error* bit is set.
2. **LCS_PCISR** register *Detected Parity Error* bit is set.
3. **LCS Interrupt Control/Status** register *Local Data Parity Error Check* bit is set, when enabled (**LCS_INTCSR**[6]=1), and Local Data Parity is detected.

4. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1), and Local Data Parity and internal Parity error are detected.

5. **LCS_PCISR** register *Signaled System Error* bit is set when internal Data Parity error is detected.

11.1.2.1.4   Uncorrectable Address Error

When the PEX 8311 detects an Uncorrectable Address error, and Parity error detection is enabled by way of the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit, the following occur:

1. Transaction is terminated with internal Target Abort.

2. **PECS_SECSTAT** register *Secondary Detected Parity Error* status bit is set, independent of the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit value.

3. **PECS_PCISTAT** register *Secondary Signaled Target Abort* bit is set.

4. ERR_FATAL message is generated on the PCI Express interface when the following conditions are met:

- **PECS_PCICMD** register *Internal SERR# Enable* bit is set –or–
- **PECS_DEVCTL** register *Fatal Error Reporting Enable* bit is set

5. **PECS_PCISTAT** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bit is set.

6. **LCS_PCISR** register *Received Target Abort* bit is set (**LCS_PCISR**[12]=1).

7. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

8. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit set, when enabled (**LCS_INTCSR**[10]=1). This causes a PCI Express Interrupt message to generate to the PCI Express interface.

11.1.2.2   Unsupported Request (UR) Completion Status

The PEX 8311 provides two methods for handling a PCI Express completion received with Unsupported Request (UR) status in response to a request originated by the Local Bus (Direct Master or DMA). The response is controlled by the **PECS_BRIDGECTL** register *Master Abort Mode* bit. In either case, the **PECS_PCISTAT** register *Received Master Abort* bit is set.

11.1.2.2.1   Master Abort Mode Bit Cleared

This is the default (PCI compatibility) mode, and an Unsupported Request is not considered as an error.

When a Non-Posted Write transaction results in a completion with Unsupported Request status, the PEX 8311 completes the Write transaction on the originating bus normally and discards the Write data.

When a Local Bus-initiated Read transaction results in the return of a completion with Unsupported Request status, the PEX 8311 returns FFFF_FFFFh to the Local Bus Master and normally terminates the Read transaction on the Local Bus.

11.1.2.2.2   Master Abort Mode Bit Set

When the **PECS_BRIDGECTL** register *Master Abort Mode* bit is set, the PEX 8311 signals an internal Target Abort to the Local Bus-originated cycle of an upstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface results in a completion with UR Status. The following occur:

1. **PECS_PCISTAT** register *Secondary Signaled Target Abort* bit is set.

2. **LCS_PCISR** register *Received Target Abort* bit is set.

3. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

4. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit is set, when enabled (**LCS_INTCSR**[10]=1). Causes a PCI Express Interrupt message to generate to the PCI Express interface.

11.1.2.3   Completer Abort (CA) Completion Status

When the PEX 8311 receives a completion with Completer Abort status on the PCI Express interface, in response to a forwarded Non-Posted transaction from Local Bus, the **PECS_PCISTAT** and **LCS_PCISR** register *Received Target Abort* bits are set. A CA response results in a Delayed Transaction Target Abort on the internal PCI Bus. The PEX 8311 provides data to the Local Bus Read Requester, up to the point where data was successfully returned from the PCI Express interface, then signals the internal Target Abort. The **PECS_PCISTAT** register *Secondary Signaled Target Abort* bit is set when signaling an internal Target Abort. The following occur:

1. **LCS_PCISR** register *Received Target Abort* bit is set.

2. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

3. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit is set, when enabled (**LCS_INTCSR**[10]=1). Causes a PCI Express Interrupt message to generate to the PCI Express interface.

11.1.3   Timeout Errors

11.1.3.1   PCI Express Completion Timeout Errors

The PCI Express Completion Timeout mechanism allows requesters to abort a Non-Posted request when a completion does not arrive within a reasonable length of time. The PEX 8311, when acting as initiator on PCI Express on behalf of internally generated requests or when forwarding requests from a Local Bus, takes ownership of the transaction.

When a Completion Timeout is detected and the Link is up, the PEX 8311 responds as if it received a completion with Unsupported Request status. The following occur:

1. ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:
   - **PECS_PCICMD** register *Internal SERR# Enable* bit is set –or–
   - **PECS_DEVCTL** register *Non-Fatal Error Reporting Enable* bit is set
2. **PECS_PCISTAT** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bit is set.
3. **LCS_PCISR** register *Received Master Abort* bit is set.
4. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).
5. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit is set, when enabled (**LCS_INTCSR**[10]=1). Causes a PCI Express Interrupt message to generate to the PCI Express interface.

When the Link is down, the **PECS_PCICTL** register *Direct Master Configuration Access Retry Count* field determines the quantity of internal PCI Bus Retries that occur before a Master Abort is internally returned. When a Master Abort is internally encountered, the LSERR# signal (C or J mode) or LINTo# (M mode) is asserted on the Local Bus, when enabled (**LCS_INTCSR**[0]=1).

11.1.3.2   Internal PCI Bus Delayed Transaction Timeout Errors

The PEX 8311 contains Delayed Transaction Timers for each Queued Delayed transaction. When a Delayed Transaction Timeout is detected, the following occur:

1. ERR_NONFATAL message is generated on the PCI Express interface, when the following conditions are met:
    - **PECS_BRIDGECTL** register *Discard Timer Internal SERR# Enable* bit is set
    - **PECS_PCICMD** register *Internal SERR# Enable* bit or **PECS_DEVCTL** register *Non-Fatal Error Reporting Enable* bit is set

2. **PECS_PCISTAT** register *Signaled System Error* bit is set when the *Internal SERR# Enable* bit is set.

3. **PECS_BRIDGECTL** register *Discard Timer Status* bit is set.

The PEX 8311 supports converting internal Retries to PCI Express Address spaces into a Target Abort, when enabled (**LCS_INTCSR**[12]=1). When enabled and the Retry Counter expires, the following occur:

1. **LCS_PCISR** register *Received Target Abort* bit set.

2. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

3. **LCS Interrupt Control/Status** register *PCI Abort Interrupt Active* bit is set, when enabled (**LCS_INTCSR**[10]=1). Causes a PCI Express Interrupt message to generate to the PCI Express interface.

11.1.4   Other Errors

The PEX 8311 Local Bus logic can generate an Internal PCI Bus System Error, when enabled (**LCS_PCICR**[8]=1), that compromises system integrity. When the PEX 8311 detects Internal PCI Bus System Error asserted, the following occur:

1. **PECS_SECSTAT** register *Secondary Received System Error* bit is set.

2. ERR_FATAL message is generated on the PCI Express interface, when the following conditions are met:
    - **PECS_BRIDGECTL** register *Secondary Internal SERR# Enable* bit is set
    - **PECS_PCICMD** and **LCS_PCICR** register *Internal SERR# Enable* bits are set or **PECS_DEVCTL** register *Fatal Error Reporting Enable* bit is set

3. **PECS_PCISTAT** and **LCS_PCISR** register *Signaled System Error* bits are set when the *Secondary Internal SERR# Enable* and *Internal SERR# Enable* bits are set.

11.2   Root Complex Mode Error Handling

When the PEX 8311 detects errors, it sets the appropriate error status bits [Conventional PCI Error bit(s) and PCI Express Error Status bit(s)]. PCI Express Error messages are ***not*** generated in Root Complex mode.

11.2.1   PCI Express Originating Interface (PCI Express-to-Local Bus)

This section describes error support for transactions that cross the PEX 8311 when the originating side is the PCI Express (downstream) interface, and the destination side is Local Bus (upstream) interface.

When a Write Request or Read Completion is received with a poisoned TLP, the entire data payload of the PCI Express transaction is considered corrupt. The PEX 8311 inverts the parity for data when completing the transaction on the Local Bus. The internal Parity Error is generated (**LCS_PCISR**[15] is set) and the Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

Table 11-4 defines the translation the PEX 8311 performs when it forwards a non-posted PCI Express request (Read or Write) to the internal PCI Bus and then to the Local Bus, and the request is immediately completed on the internal PCI Bus, either normally or with an error condition. The PEX 8311 internal PCI Bus error condition status bits are checked in the **LCS_PCISR** register. Internal error status bits are set, regardless of whether their respective error interrupt is enabled. The PEX 8311 ignores Parity error reporting on the destination Local Bus.

Table 11-4.   PEX 8311 Translation – Non-Posted PCI Express Request

Immediate internal PCI Bus and Local Bus Termination	PCI Express Completion Status
Data Transfer with Parity error (reads)	Successful (poisoned TLP)
Completion with Parity error (Non-Posted Writes)	Unsupported Request
Internal Master Abort (Abort to Local Address space)	Unsupported Request
Internal Target Abort (Abort to Local Address space)	Completer Abort

11.2.1.1   Received Poisoned TLP

When the PEX 8311 PCI Express interface receives a Write Request or Read Completion with poisoned data, the following occur:

1. **PECS_SECSTAT** register *Secondary Detected Parity Error* bit is set.

2. **PECS_SECSTAT** register *Secondary Master Data Parity Error* bit is set when the poisoned TLP is a Read Completion and the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set.

3. *Parity* bit associated with each DWORD of data is inverted.

4. For a poisoned Write request, the **PECS_PCISTAT** register *Master Data Parity Error* bit is set when the **PECS_PCICMD** register *Parity Error Response Enable* bit is set, and the bridge detects the internal Parity Error signal asserted when the PEX 8311 Local Bus Address space detects inverted parity.

5. **LCS_PCISR** register *Detected Parity Error* bit is set.

6. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.2.1.2   Internal Uncorrectable Data Errors

The following sections describe how errors are handled when forwarding non-poisoned PCI Express transactions to the PEX 8311 Local Bus, and an Uncorrectable Error is internally detected.

11.2.1.2.1   Immediate Reads

When the PEX 8311 forwards a Read request (I/O or Memory) from the PCI Express interface to the Local Bus interface, and detects an Uncorrectable Data error on the internal PCI Bus while receiving an immediate response from the PEX 8311 Local Bus logic, the following occur:

1. **PECS_PCISTAT** register *Master Data Parity Error* bit is set when the **PECS_PCICMD** register *Parity Error Response Enable* bit is set.

2. **PECS_PCISTAT** register *Detected Parity Error* bit is set.

3. Parity Error signal (**LCS_PCICR**[6] and **LCS_PCISR**[15]) is asserted on the internal PCI Bus when the **PECS_PCICMD** register *Parity Error Response Enable* bit is set.

4. **LCS Interrupt Control/Status** register *Local Data Parity Check Error* bit is set when a Local Data Parity error is detected.

5. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[6, 0]=11b).

After detecting an Uncorrectable Data error on the destination bus for an Immediate Read transaction, the PEX 8311 continues to fetch data until the Byte Count is satisfied or the target ends the transaction.

When the PEX 8311 creates the PCI Express completion, it forwards it with Successful Completion status and poisons the TLP.

11.2.1.2.2   Non-Posted Writes

When the PEX 8311 detects the internal Parity Error signal asserted while forwarding a non-poisoned, Non-Posted Write transaction from PCI Express to the Local Bus, the following occur:

1. **PECS_PCISTAT** register *Master Data Parity Error* bit is set when the **PECS_PCICMD** register *Parity Error Response Enable* bit is set.

2. PCI Express completion with Unsupported Request status is returned.

3. **LCS_PCISR** register *Detected Parity Error* bit is set.

4. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.2.1.2.3   Posted Writes

When the PEX 8311 detects the internal Parity Error signal asserted while forwarding a non-poisoned, Posted Write transaction from PCI Express to the Local Bus, the following occur:

1. **PECS_PCISTAT** register *Master Data Parity Error* bit is set when the **PECS_PCICMD** register *Parity Error Response Enable* bit is set

2. After the error is detected, remainder of the data is forwarded.

3. **LCS_PCISR** register *Detected Parity Error* bit is set.

4. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.2.1.3   Internal Address Errors

When the PEX 8311 forwards transactions from PCI Express-to-Local Bus, Address errors are reported by the PEX 8311 internal Parity Error signal assertion, when enabled (**LCS_PCICR**[6]=1). In addition, the PEX 8311 can generate a Local System Error (C or J mode – LSERR#; M mode – LINTo#), when enabled (**LCS_INTCSR**[0]=1), and allows the Local Bus Master (Root Complex device) to service the error. The internal Error status bits must be monitored (**LCS_PCISR** register). When an Address error is encountered, the following occur:

1. **LCS_PCISR** register *Detected Parity Error* bit is set.
2. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.2.1.4   Internal Master Abort on Posted Transaction

When a transaction forwarded from PCI Express-to-Local Bus results in internal Master Abort, the following occur:

1. Entire transaction is discarded.
2. **PECS_PCISTAT** register *Received Master Abort* bit is set.

11.2.1.5   Internal Master Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-Local Bus results in an internal Master Abort, the following occur:

1. PCI Express completion with Unsupported Request status is returned.
2. Set the **PECS_PCISTAT** register *Received Master Abort* bit.

11.2.1.6   Internal Target Abort on Posted Transaction

When a Posted transaction forwarded from PCI Express-to-Local Bus results in an internal Target Abort, the following occur:

1. Entire transaction is discarded.
2. **PECS_PCISTAT** register *Received Target Abort* bit is set.
3. **LCS_PCISR** register *Signaled Target Abort* bit is set.
4. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.2.1.7   Internal Target Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-Local Bus results in an internal Target Abort, the following occur:

1. PCI Express completion with Completer Abort status is returned.

2. **PECS_PCISTAT** register *Received Target Abort* bit is set.

3. **LCS_PCISR** register *Signaled Target Abort* bit is set.

4. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.2.1.8   Internal Retry Abort on Posted Transaction

When a Posted transaction forwarded from PCI Express-to-Local Bus results in a Retry Abort on the internal PCI Bus, the following occur:

1. Entire transaction is discarded.

2. **PECS_IRQSTAT** register *PCI Express-to-Local Retry Interrupt* bit is set.

11.2.1.9   Internal Retry Abort on Non-Posted Transaction

When a Non-Posted transaction forwarded from PCI Express-to-Local Bus results in a Retry Abort on the internal PCI Bus, the following occur:

1. PCI Express completion with Completer Abort status is returned.

2. **PECS_IRQSTAT** register *PCI Express-to-Local Retry Interrupt* bit is set.

3. **PECS_SECSTAT** register *Secondary Signaled Target Abort* bit is set.

11.2.2   Local Originating Interface (Local-to-PCI Express)

This section describes error support for transactions that cross the bridge when the originating side is the Local Bus (downstream) interface, and the destination side is PCI Express (upstream) interface. The PEX 8311 supports TLP poisoning as a transmitter to permit proper forwarding of Parity errors that occur on either the PEX 8311 Local Bus or internal PCI Bus. Posted Write data received on the Local Bus with bad parity are forwarded to the PCI Express interface as poisoned TLPs.

Table 11-5 defines the error forwarding requirements for Uncorrectable Data errors detected by the PEX 8311 when a transaction targets the PCI Express interface.

Table 11-5.   Error Forwarding Requirements

Received Local or Internal PCI Bus Error	Forwarded PCI Express Error
Write with Parity error	Write request with poisoned TLP
Read Completion with Parity error in Data phase	Read completion with poisoned TLP
Configuration or I/O Completion with Parity error in Data phase	Read/Write completion with Completer Abort status

Table 11-6 and Table 11-7 describe the bridge behavior on an internal Delayed transaction between Local Bus and PCI Express Address spaces that is forwarded to the PCI Express interface as a Memory Read or I/O Read/Write request, and the PCI Express interface returns a completion with UR or CA status for the request.

Table 11-6. Bridge Behavior on Internal Delayed Transaction – C and J Modes

PCI Express Completion Status	Internal PCI Bus Immediate Response to Local Bus	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory Read or I/O Read)	Target Abort. The PEX 8311 *Received Target Abort* bit is set (**LCS_PCISR**[12]=1). LSERR# is asserted, when enabled (**LCS_INTCSR**[0]=1).	Normal completion, return FFFF_FFFFh.
Unsupported Request (on I/O Write)	Target Abort. The PEX 8311 *Received Target Abort* bit is set (**LCS_PCISR**[12]=1). LSERR# is asserted, when enabled (**LCS_INTCSR**[0]=1).	Normal completion.
Completer Abort	Target Abort. The PEX 8311 *Received Target Abort* bit is set (**LCS_PCISR**[12]=1). LSERR# is asserted, when enabled (**LCS_INTCSR**[0]=1).	

Table 11-7. Bridge Behavior on Internal Delayed Transaction – M Mode

PCI Express Completion Status	Internal PCI Bus Immediate Response to Local Bus	
	Master Abort Mode = 1	Master Abort Mode = 0
Unsupported Request (on Memory Read or I/O Read)	Target Abort. The PEX 8311 *Received Target Abort* bit is set (**LCS_PCISR**[12]=1). LINTo# is asserted, when enabled (**LCS_INTCSR**[0]=1).	Normal completion, return FFFF_FFFFh.
Unsupported Request (on I/O Write)	Target Abort. The PEX 8311 *Received Target Abort* bit is set (**LCS_PCISR**[12]=1). LINTo# is asserted, when enabled (**LCS_INTCSR**[0]=1).	Normal completion.
Completer Abort	Target Abort. The PEX 8311 *Received Target Abort* bit is set (**LCS_PCISR**[12]=1). LINTo# is asserted, when enabled (**LCS_INTCSR**[0]=1).	

11.2.2.1   Received Internal Errors

11.2.2.1.1   Uncorrectable Data Error on Non-Posted Write

When a Non-Posted Write is addressed such that its destination is the PCI Express interface, and the PEX 8311 detects an Uncorrectable Data error on the internal PCI Bus, the following occur:

1. **PECS_PCISTAT** register *Detected Parity Error* status bit is set.

2. If the **PECS_PCICMD** register *Parity Error Response Enable* bit is set, the transaction is discarded and not forwarded to PCI Express. The internal Parity Error signal is asserted to the Local Bus Address space.

3. If the **PECS_PCICMD** register *Parity Error Response Enable* bit is not set, the data is forwarded to PCI Express as a poisoned TLP. The **PECS_SECSTAT** register *Secondary Master Data Parity Error* bit is set when the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set. The internal Parity Error signal is not asserted to the PEX 8311 Local Bus Address space.

4. **LCS_PCISR** register *Master Data Parity Error* bit is set.

5. **LCS_PCISR** register *Detected Parity Error* bit is set.

6. **LCS_INTCSR** register *Local Data Parity Check Error* bit is set.

7. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[6, 0]=11b), when a Local Data Parity error is encountered.

11.2.2.1.2   Uncorrectable Data Error on Posted Write

When the PEX 8311 detects an Uncorrectable Data error on the internal PCI Bus for a Posted Write transaction that is targeted to the PCI Express interface, the following occur:

1. Internal Parity Error signal is asserted to the Local Bus Address space, when the **PECS_PCICMD** register *Parity Error Response Enable* bit is set.

2. **PECS_PCISTAT** register *Detected Parity Error* status bit is set.

3. Posted Write transaction is forwarded to PCI Express as a poisoned TLP.

4. **PECS_SECSTAT** register *Secondary Master Data Parity Error* bit is set when the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set.

5. **LCS_PCISR** register *Master Data Parity Error* bit is set.

6. **LCS_PCISR** register *Detected Parity Error* bit is set.

7. **LCS_INTCSR** register *Local Data Parity Check Error* bit is set.

8. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[6, 0]=11b), when a Local Data Parity error is encountered.

11.2.2.1.3   Uncorrectable Data Error on Internal Delayed Read Completions

When the PEX 8311 forwards a non-poisoned or poisoned Read Completion from PCI Express-to-Local Bus, and internal Parity Error signal is asserted by the PEX 8311 Local Bus logic (Requester of the Read), the following occur:

1. Remainder of completion is forwarded.

2. Local Bus Master (Root Complex) services the internal Parity Error assertion. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[1:0]=11b).

3. **LCS_PCISR** register *Master Data Parity Error* bit is set.

4. **LCS_PCISR** register *Detected Parity Error* bit is set.

5. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1), due to the internal Parity error detection.

11.2.2.1.4   Uncorrectable Address Error

When the PEX 8311 detects an Uncorrectable Address error and Parity error detection is enabled by the **PECS_PCICMD** register *Parity Error Response Enable* bit, the following occur:

1. Transaction is terminated with an internal Target Abort. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

2. **PECS_PCISTAT** register *Signaled Target Abort* bit is set.

3. **PECS_PCISTAT** register *Detected Parity Error* status bit is set, independent of the setting of the **PECS_PCICMD** register *Parity Error Response Enable* bit.

4. Internal System Error is asserted, when enabled, by way of the **PECS_PCICMD** register.

5. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[1:0]=11b).

6. **PECS_PCICMD** register *Internal SERR# Enable* bit is set.

7. **PECS_PCISTAT** register *Signaled System Error* bit is set when the internal System Error signal is asserted.

8. **LCS_PCISR** register *Received Target Abort* bit is set.

9. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[1:0]=11b), due to the internal Target Abort and System Error signal assertion.

11.2.2.1.5   Internal Master Abort

When a Local Bus access (Local Address space) encounters an internally generated Master Abort, the entire transaction is discarded and not forwarded to the PCI Express interface. The BTERM# (C or J mode) or TEA# (M-mode) signal is asserted to the Local Bus Master when it is a Read cycle only and the following occur:

1. **LCS_PCISR** register *Received Master Abort* bit is set.

2. Local Bus System error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).

11.2.2.2   Unsupported Request (UR) Completion Status

The PEX 8311 provides two methods for handling a PCI Express completion received with Unsupported Request (UR) status in response to a request originated by the Local Bus. The response is controlled by the **PECS_BRIDGECTL** register *Master Abort Mode* bit. In either case, the **PECS_SECSTAT** register *Secondary Received Master Abort* bit is set.

11.2.2.2.1   Master Abort Mode Bit Cleared

This is the default compatibility mode, and an Unsupported Request is not considered as an error. When a Local Bus-initiated Read transaction results in the return of a completion with UR status, the PEX 8311 returns FFFF_FFFFh to the Local Bus (originating Local Bus Master) and successfully terminates the Read transaction. When a Non-Posted Write transaction results in a completion with UR status, the PEX 8311 completes the Write transaction on the Local Bus normally and discards the Write data.

11.2.2.2.2   Master Abort Mode Bit Set

When the *Master Abort Mode* bit is set, the PEX 8311 signals an internal Target Abort to the Local Bus. As a result, the initiator of a downstream Read or Non-Posted Write transaction when the corresponding request on the PCI Express interface completes with UR status. The following occur:

1. **PECS_PCISTAT** register *Signaled Target Abort* bit is set.
2. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[1:0]=11b).
3. **LCS_PCISR** register *Received Target Abort* bit is set.

11.2.2.3   Completer Abort (CA) Completion Status

When the PEX 8311 receives a completion with Completer Abort status on the PCI Express interface in response to a forwarded Non-Posted Local Bus transaction, the **PECS_SECSTAT** register *Secondary Received Target Abort* bit is set. A completion with CA status results in a Delayed Transaction Target Abort on the internal PCI Bus. The PEX 8311 provides data to the requesting Local Bus Master, up to the point where data was successfully returned from the PCI Express interface prior to encountering CA. The following occur:

1. **PECS_PCISTAT** register *Signaled Target Abort* status bit is set when signaling Target Abort.
2. Local Bus System error (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[0]=1).
3. **LCS_PCISR** register *Received Target Abort* bit is set.

11.2.3 Timeout Errors

11.2.3.1 PCI Delayed Transaction Timeout Errors

The PCI Express Completion Timeout mechanism allows requesters to abort a Non-Posted request when a completion does not arrive within a reasonable time. The PEX 8311, when acting as initiators on PCI Express on behalf of internally generated requests and requests forwarded from the PCI Express interface, behave as endpoints for requests of which they take ownership. When a Completion Timeout is detected and the Link is up, the PEX 8311 responds as if an Unsupported Request Completion was received.

When the Link is down, the **PECS_PCICTL** register *Direct Master Configuration Access Retry Count* field determines the number of internally generated Retries to occur before an internal Master Abort is returned to the PEX 8311 Local Bus logic.

11.2.3.2 Internal Delayed Transaction Timeout Errors

The PEX 83111 contains Delayed Transaction Timers for each Queued Delayed transaction. When a Delayed Transaction Timeout is detected, the following occur:

1. **PECS_BRIDGECTL** register *Discard Timer Status* bit is set.

2. Delayed request is removed from the Non-Posted Transaction queue.

3. Internal System Error signal is asserted, when the **PECS_PCICMD** register *Internal SERR# Enable* bit is set.

4. Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted, when enabled (**LCS_INTCSR**[1:0]=11b).

11.2.4 Other Errors

11.2.4.1 Other Errors – C and J Modes

When detecting errors, internal System Error signal assertion can compromise system integrity. The PEX 8311 ignores Internal System Error signal assertion in Root Complex mode, and allows the Local Bus Master (Root Complex) to service the LSERR# interrupt, when enabled and generated. The LSERR# bits – **LCS_INTCSR**[12, 6, 1:0] – are used to enable or disable LSERR# sources. LSERR# is a level output that remains asserted when the *Interrupt Status* or *Enable* bits are set.

11.2.4.2 Other Errors – M Mode

When detecting errors, internal System Error signal assertion can compromise system integrity. The PEX 8311 ignores Internal System Error signal assertion in Root Complex mode, and allows the Local Bus Master (Root Complex) to service the LINTo# interrupt, when enabled and generated. The LINTo# bits – **LCS_INTCSR**[12, 6, 1:0] – are used to enable or disable LINTo# sources. LINTo# is a level output that remains asserted when the *Interrupt Status* or *Enable* bits are set.

11.2.5   PCI Express Error Messages

When the PEX 8311 detects an ERR_FATAL, ERR_NONFATAL, or ERR_COR error, or receives an ERR_FATAL, ERR_NONFATAL, or ERR_COR message, the internal System Error signal is asserted when the corresponding Reporting Enable bit in the **PECS_ROOTCTL** register is set (Root Complex mode only), and the Local Bus System Error signal (C or J mode – LSERR#; M mode – LINTo#) is asserted in response to the internal System error, when enabled (**LCS_INTCSR**[1:0]=11b). When an ERR_FATAL or ERR_NONFATAL message is received, the **PECS_SECSTAT** register *Secondary Received System Error* bit is set, independent of the **PECS_ROOTCTL** register Reporting Enable bits.

When an Unsupported Request is received by the PEX 8311, a **PECS_IRQSTAT** register interrupt status bit is set. This status bit is enabled to generate an internal PCI wire interrupt (INTA#) or MSI.

Chapter 12   Interrupts

12.1   Introduction

This chapter provides information about PEX 8311 interrupts, interrupt sources, and user I/O ball functionality. Figure 12-1 illustrates the interrupts sources and output types possible for PCI Express Spaces. Figure 12-2 (C and J modes) and Figure 12-3 (M mode) illustrate the interrupts sources and output types possible for Local Bus Spaces.

In PCI Express Space, interrupts are passed using in-band messaging, in one direction only. In Local Bus Space, Local interrupts can be generated in Endpoint and Root Complex modes.

In Endpoint mode, the PEX 8311 transmits Interrupt messages to PCI Express Space. In Root Complex mode, the PEX 8311 receives Interrupt messages.

The following sections describe the various interrupt sources and interrupt outputs supported in Endpoint and Root Complex modes.

Figure 12-1.   PCI Express Interrupt Messaging (Endpoint Mode)
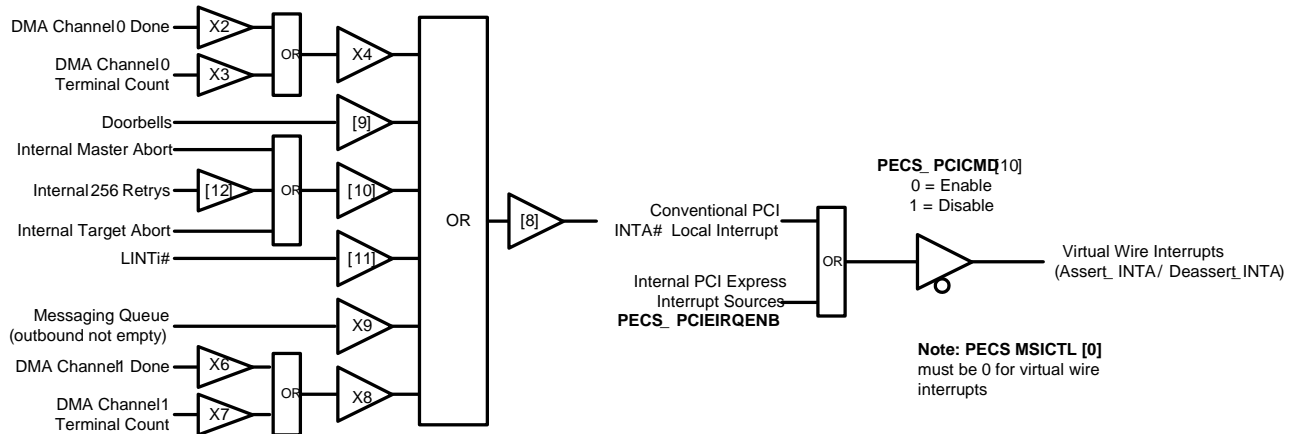
The numbers in [brackets] represent **LCS_INTCSR** register bits

X2 = *DMA Channel 0 Done Interrupt Enable* bit (**LCS_ DMAMODE0**[10])
X3 = *DMA Channel 0 Interrupt after Terminal Count* bit (**LCS_ DMADPR 0**[2])
X4 = *Local DMA Channel 0 Interrupt Enable* and *Select* bits
        (**LCS_INTCSR**[18] and **LCS_ DMAMODE0** [17], respectively)
X6 = *DMA Channel 1 Done Interrupt Enable* bit (**LCS_DMAMODE1** [10])
X7 = *DMA Channel 1 Interrupt after Terminal Count* bit (**LCS_ DMADPR1**[2])
X8 = *Local DMA Channel1 Interrupt Enable* and *Select* bits
        (**LCS_INTCSR** [19] and **LCS_ DMAMODE1** [17], respectively)

For X4 and X8 : If **LCS_ DMAMODEx**[17]=0 , LINTo# is asserted
                      If **LCS_ DMAMODEx**[17]=1 , INTA# is asserted

Notes: *Only one Assert_INTA message is generated regardless of how many interrupts are active.*

When all pending interrupts are cleared or disabled one Deassert_INTA message is generated.

When MSI is enabled, local interrupts are disabled.

Figure 12-2.   Local Interrupt and Error Sources – C and J Modes
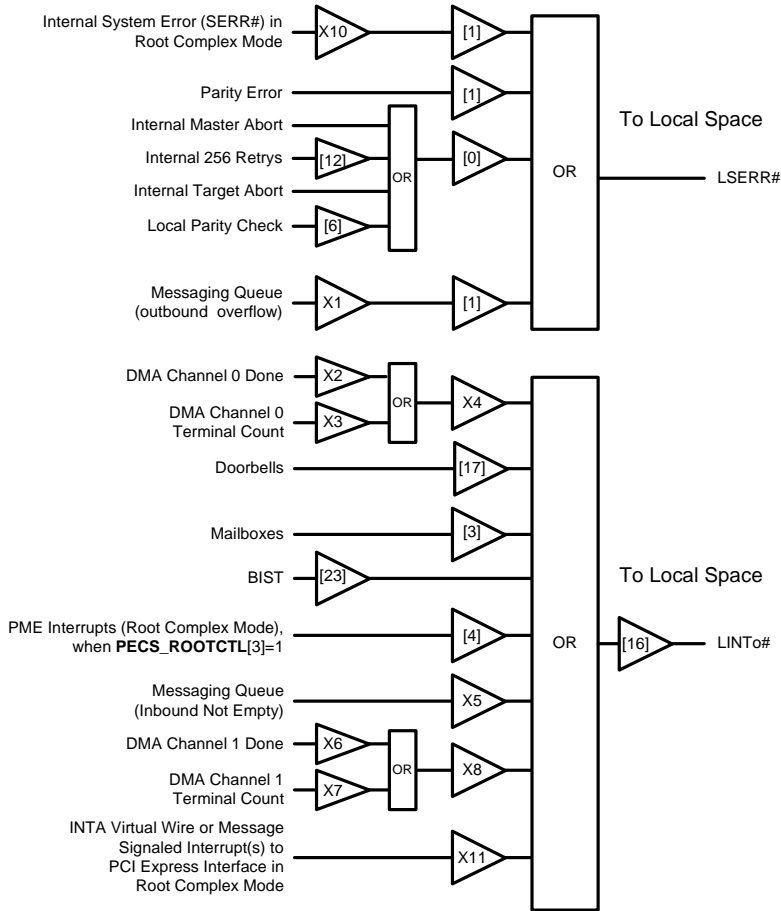
The numbers in [brackets] represent **LCS_INTCSR** register bits.

X1 =   *Outbound Free Queue Overflow Interrupt Full* and *Mask* bits
          (**LCS_QSR**[7:6], respectively)
X2 =   *DMA Channel 0 Done Interrupt Enable* bit (**LCS_DMAMODE0**[10])
X3 =   *DMA Channel 0 Interrupt after Terminal Count* bit (**LCS_DMADPR0**[2])
X4 =   *Local DMA Channel 0 Interrupt Enable* and *Select* bits
          (**LCS_INTCSR**[18] and **LCS_DMAMODE0**[17], respectively)
X5 =   *Inbound Post Queue Interrupt Not Empty* and *Mask* bits
          (**LCS_QSR**[5:4], respectively)
X6 =   *DMA Channel 1 Done Interrupt Enable* bit (**LCS_DMAMODE1**[10])
X7 =   *DMA Channel 1 Interrupt after Terminal Count* bit (**LCS_DMADPR1**[2])
X8 =   *Local DMA Channel 1 Interrupt Enable* and *Select* bits
          (**LCS_INTCSR**[19] and **LCS_DMAMODE1**[17], respectively)
X10 = *LSERR# Interrupt Status* bit (**LCS_CNTRL**[21])
X11 = *LINTo# Interrupt Status* bit (**LCS_CNTRL**[20])

For X4 and X8: If **LCS_DMAMODE*x***[17]=0, LINTo# is asserted
                          If **LCS_DMAMODE*x***[17]=1, INTA# is asserted

Figure 12-3.   Local Interrupt and Error Sources – M Mode
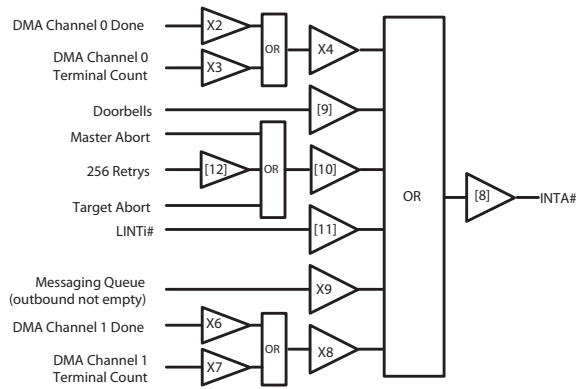
The numbers in [brackets] represent INTCSR register bits
X1 = Outbound Free Queue Overflow Interrupt Full and Mask bits
        (QSR[7:6], respectively)
X2 = DMA Channel 0 Done Interrupt Enable bit (DMAMODE0[10])
X3 = DMA Channel 0 Interrupt after Terminal Count bit (DMADPR0[2])
X4 = Local DMA Channel 0 Interrupt Enable and Select bits
        (INTCSR[18] and DMAMODE0[17], respectively)
X5 = Inbound Post Queue Interrupt Not Empty and Mask bits
        (QSR[5:4], respectively)
X6 = DMA Channel 1 Done Interrupt Enable bit (DMAMODE1[10])
X7 = DMA Channel 1 Interrupt after Terminal Count bit (DMADPR1[2])
X8 = Local DMA Channel 1 Interrupt Enable and Select bits
        (INTCSR[19] and DMAMODE1[17], respectively)
X9 = Outbound Post Queue Interrupt and Mask bits
        (OPQIS[3] and OPQIM[3], respectively)
X10 = LSERR# Interrupt Status bit (CNTRL[21])
X11 = LINTo# Interrupt Status bit (CNTRL[20])

For X4 and X8, if DMAMODE   x[17]=0, then LINTo# is asserted and
                    if DMAMODE   x[17]=1, then INTA# is asserted
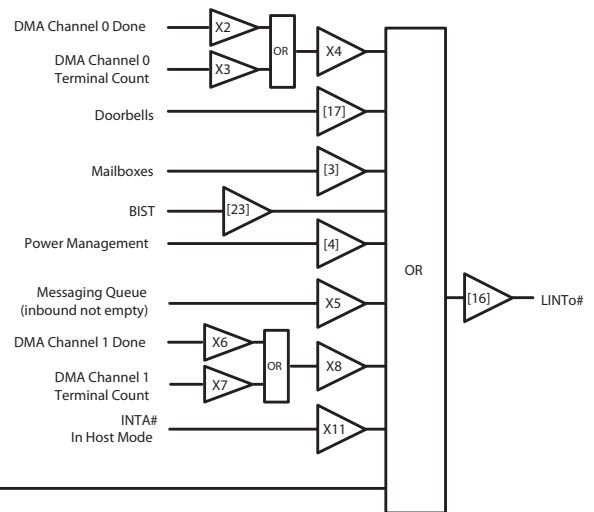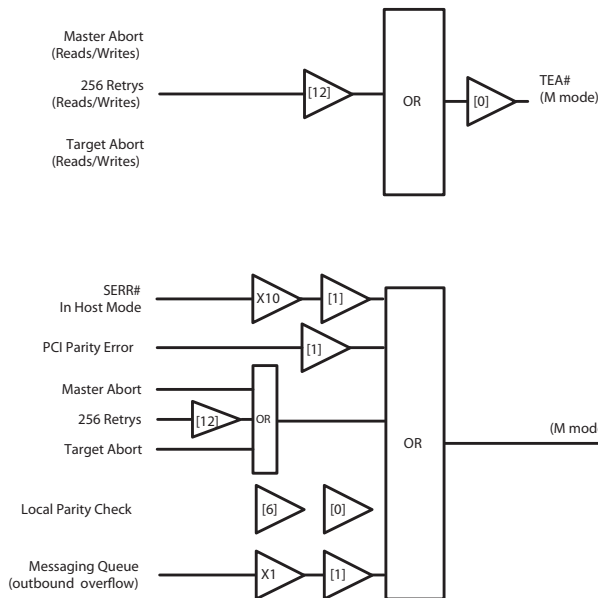
12.2   Endpoint Mode PCI Express Interrupts

In Endpoint mode, PCI Express Interrupt sources can be grouped into two main branches – Local interrupts and PCI Express Bridge interrupts:

- Local interrupts are gated by the **LCS_INTCSR** register, and are passed to the PCI Express bridge by way of the Conventional PCI INTA# signal
- PCI Express Bridge interrupts are gated by the **PECS_PCIIRQENB** register, and support several internal bridge functions

Sources of internal and external interrupts can cause the PEX 8311 to issue interrupts on the PCI Express interface.

12.3   Endpoint Mode Local Interrupts

For Conventional PCI compatibility, the PCI INT*x* emulation mechanism is used to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software, provides the same level of service as the corresponding PCI interrupt signaling mechanism, and is independent of System Interrupt Controller specifications. This Conventional PCI-compatibility mechanism virtualizes PCI physical interrupt signals by using an in-band signaling mechanism.

Note: Local interrupts are disabled when MSI interrupts are enabled. MSI interrupts are supported only for PCI Express Bridge Internally Generated Interrupts (See section Section 12.3.2).

12.3.1   Local Interrupt Sources

Local interrupts from internal sources are gated by the **LCS_INTCSR** register. (Refer to Figure 12-2.) Local interrupts are passed to the PCI Express bridge by way of the Conventional PCI INTA# signal. Sources of Local interrupts are as follows:

- **Mailbox** registers written
- **Doorbell** registers written
- DMA Done or Abort
- DMA Terminal Count
- internal PCI Bus Master/Target Aborts
- 256 Consecutive Retries between Local Address and PCI Express Address spaces
- Messaging Outbound Post queue not empty
- Local Bus Interrupt input (LINTi#) assertion

12.3.1.1   Local Configuration Space Mailbox Register Interrupts

The PEX 8311 Local Bus logic has eight, 32-bit **Mailbox** registers that are written to and read from the PCI Express interface and Local Bus. These registers are used to pass command and status information directly between the PCI Express and Local Bus devices. (Refer to Figure 12-4.) For the PCI Express interface to be able to access Mailbox registers, a Type 1 Configuration access (Type 1 access is internally converted to Type 0) must be performed to the Local Configuration space.

A Local interrupt (LINTo#) is asserted, when enabled (**LCS_INTCSR**[3, 16]=11b, respectively), when the PCI Express Root Complex Writes to one of the first four **Mailbox** registers (**LCS_MBOX0**, **LCS_MBOX1**, **LCS_MBOX2**, or **LCS_MBOX3**).

Regardless of whether LINTo# is enabled, a PCI Express Write to one of the first four **Mailbox** registers sets a corresponding status bit in **LCS_INTCSR**[31:28], provided the Mailbox interrupts are enabled (**LCS_INTCSR**[3]=1).

To clear the LINTo# assertion caused by the PCI Express Root Complex Write(s) of any of the first four **Mailbox** registers, a Local Bus device must read each **Mailbox** register that was written.

Figure 12-4.   Local Mailbox and Doorbell Message Passing

12.3.1.2   Doorbell Registers

The PEX 8311 has two 32-bit **Doorbell** registers. One is assigned to the PCI Express interface; the other to the Local Bus interface.

A PCI Express Root Complex can assert a Local interrupt output (LINTo#) by writing any number other than all zeros (0) to the *PCI Express-to-Local Doorbell* bits (**LCS_P2LDBELL**[31:0]). The Local Interrupt remains asserted until all **LCS_P2LDBELL** bits are cleared to 0. A Local processor can cause a PCI Express assert message interrupt generation by writing any number other than all zeros (0) to the *Local-to-PCI Express Doorbell* bits (**LCS_L2PDBELL**[31:0]). The PEX 8311 generates a PCI Express De-assert PCI Express Message interrupt after all **LCS_L2PDBELL** bits are cleared to 0. (Refer to Figure 12-4.)

12.3.1.2.1   Local-to-PCI Express Interrupt

A Local Bus Master can cause the PEX 8311 to generate PCI Express message interrupt by writing to the *Local-to-PCI Express Doorbell* bits (**LCS_L2PDBELL**[31:0]). The PCI Express Root Complex can read the *PCI Express Doorbell Interrupt Active* bit (**LCS_INTCSR**[13]) to determine whether a PCI Express Doorbell interrupt is pending; therefore, if **LCS_INTCSR**[13]=1, read the PEX 8311 **LCS_L2PDBELL** register.

Each *Local-to-PCI Express Doorbell* bit is individually controlled. The *Local-to-PCI Express Doorbell* bits are set only by the Local Bus. From the Local Bus, writing 1 to any bit position sets that bit and writing 0 has no effect. Local-to-PCI Express Doorbell register bits are cleared only from the PCI Express interface. From the PCI Express interface, writing 1 to any bit position clears that bit and writing 0 has no effect.

The PEX 8311 does not generate PCI Express de-assert interrupt messages until all Local-to-PCI Express Doorbell register bits are cleared, the *PCI Express Doorbell Interrupt Enable* bit is cleared, or the PCI Interrupt is disabled (**LCS_INTCSR**[9:8]=00b, respectively).

To prevent race conditions from occurring when the PCI Express interface is accessing the **LCS_L2PDBELL** register (or **LCS** registers), the PEX 8311 automatically de-asserts READY# output to prevent Local Bus Configuration accesses.

12.3.1.2.2   PCI Express-to-Local Interrupt

The PCI Root Complex can assert a Local interrupt output (LINTo#) by writing 1 to any of the *PCI Express-to-Local Doorbell* bits (**LCS_P2LDBELL**[31:0]). The Local processor can read the *Local Doorbell Interrupt Active* bit (**LCS_INTCSR**[20]) to determine whether a Local doorbell interrupt is pending; therefore, if **LCS_INTCSR**[20]=1, read the **LCS_P2LDBELL** register.

Each PCI Express-to-Local Doorbell register bit is individually controlled. The *PCI Express-to-Local Doorbell* bits are set only by the PCI Express interface. From the PCI Express interface, writing 1 to any bit position sets that bit and writing 0 has no effect. PCI Express-to-Local Doorbell register bits are cleared only from the Local Bus. From the Local Bus, writing 1 to any bit position clears that bit and writing 0 has no effect.

*Note: When the Local Bus cannot clear a Doorbell interrupt, do **not** use the LCS_P2LDBELL register.*

The Local interrupt remains set when any *PCI Express-to-Local Doorbell* bits are set and the *Local Doorbell Interrupt Enable* bit is set (**LCS_INTCSR**[17]=1).

To prevent race conditions when the Local Bus is accessing the **LCS_P2LDBELL** register (or Local Configuration registers), the PEX 8311 automatically issues an internal Retry to the PCI Express Address spaces.

12.3.1.3   Internal Master/Target Abort Interrupt

The PEX 8311 sets the internal PCI Bus *Received Master* or *Target Abort* bit (**LCS_PCISR**[13 or 12]=1, respectively) when accessing PEX 8311 PCI Express Address space, and it detects an internal Master or Target Abort. These status bits cause the PCI Express message interrupt to generate when interrupts are enabled (**LCS_INTCSR**[10, 8]=11b).

The interrupt remains set when the *Received Master* or *Target Abort* bit remains set and the PCI Master/ Target Abort interrupt is enabled. Use PCI Type 1 (Type 1 is internally converted to Type 0) PCI Express Configuration or Local accesses to the **LCS_PCISR** register to clear the internal PCI Bus *Received Master* and *Target Abort* bits (**LCS_PCISR**[13:12]=00b, respectively).

The *Interrupt Control/Status* bits (**LCS_INTCSR**[26:24]) are latched at the time of internal PCI Master or Target Abort interrupt. When an abort occurs, these bits provide information, *such as* which device was the Master when the abort occurred. In addition, when internal Master or Target Abort occurs, the current Address (Abort Address) is stored in the *PCI Abort Address* bits (**LCS_PABTADR**[31:0]).

12.3.2   PCI Express Bridge Internally Generated Interrupts

PCI Express Bridge interrupts from internal sources are gated by the **PECS_PCIIRQENB** register, and support several internal bridge functions. PCI Express Bridge interrupt sources are as follows:

- Serial EEPROM done
- GPIO Interrupt active
- PCI Express-to-Local Retry interrupt
- Mailbox interrupt
- PCI Express Internal interrupt

12.3.2.1   PCI Express Configuration Space Mailbox Register Interrupts

The PEX 8311 PCI Express interface logic has four, 32-bit **Mailbox** registers that are written to and read from the PCI Express interface and Local Bus. These registers are used to pass command and status information directly between the PCI Express and Local Bus devices. (Refer to Figure 12-5.) For PCI Express and Local Bus Master to access **Mailbox** registers a Memory- or I/O-Mapped access through the **PECS_PCIBASE0** register must be performed.

In Endpoint mode, the PEX 8311 is programmed to generate PCI Express interrupts (either virtual wire or message interrupt) only as a result of the Mailbox Write accesses, when enabled (**PECS_PCIEIRQENB** register). The Mailbox interrupt statuses are located in the **PECS_IRQSTAT** register. Writing 1 to a Mailbox interrupt status register clears the respective Mailbox interrupt.

Figure 12-5.   PCI Express Mailboxes

PCI Express Interface   Local Bus

Mailbox registers can be read and/or written from
PCI Express Interface and/or Local Bus

| Mailbox 0 |
| Mailbox 1 |
| Mailbox 2 |
| Mailbox 3 |
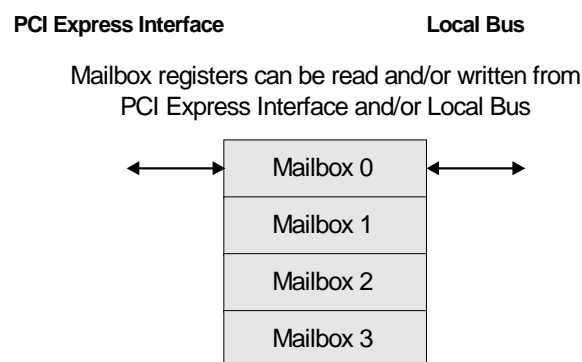
12.4   PCI Express Interrupt Messaging

Two types of messaging are supported for PCI Express interrupts:

- Virtual Wire (INTA#) messaging, as defined in the *PCI Express Base 1.0a*
- Message Signaled Interrupts (MSI), as defined in the *PCI r3.0*

These two messaging types are mutually exclusive, and only one or the other can be used in a system design.

12.4.1   Virtual Wire Interrupts

When MSI is disabled, Virtual Wire interrupts are used to support internal interrupt events. Internal interrupt sources are masked by the **PECS_PCICMD** register *Interrupt Disable* bit and are routed to one of the virtual interrupts using the **PECS_PCIINTPIN** register. PCI Express Assert_INTA and Deassert_INTA messages are not masked by the **PECS_PCICMD** register *Bus Master Enable* bit. The internal interrupt is processed the same as the external Local LINTi# signal.

Local interrupts are "virtualized" in PCI Express, using Assert_INTA and Deassert_INTA messages for the internal PCI Wire interrupt. This message pairing provides a mechanism to preserve the level-sensitive semantics of the PCI interrupts. The Assert_INTA and Deassert_INTA messages transmitted on the PCI Express Link capture the asserting/de-asserting edge of the respective source of the interrupt.

For example, if all interrupt sources are enabled and not active, activation of one interrupt source causes an Assert_INTA message to be sent to PCI Express Space. Subsequent assertions of other interrupt sources, provided at least one interrupt source remains asserted, do not cause subsequent Assert_INTA messages. When all pending interrupts are cleared or disabled, a Deassert_INTA message is sent to PCI Express Space.

The Requester ID used in the PCI Express Assert_INTA and Deassert_INTA messages transmitted by the PEX 8311 (irrespective of whether the source is internal or external to the bridge) equals the bridge PCI Express interface Bus and Device Numbers. The Function Number subfield is cleared to 0.

12.4.1.1   Virtual INT*x* Wire Interrupts

The PCI Express interface supports the INTA# Virtual Wire Interrupt feature for Conventional PCI systems that support internal INTA# interrupt signals. Internal INTA# interrupts are "virtualized" in the PCI Express Link, using Assert_INTA and Deassert_INTA messages for internal PCI Wire interrupts:

- Assert_INTA messages, that indicate a High-to-Low transition of the virtual INTA# signal
- Deassert_INTA messages, that indicate a Low-to-High transition of the virtual INTA# signal

This message pairing provides a mechanism to preserve the level-sensitive semantics of the PCI interrupts. The Assert_INTA and Deassert_INTA messages transmitted on the PCI Express Link capture the asserting/de-asserting edge of the respective interrupt sources.

When MSI is disabled, Virtual Wire interrupts are used to support internal interrupt events.

When the PEX 8311 signals an interrupt, it also sets a bit within a device-specific register (**PECS_PCISTAT**) to indicate that an interrupt is pending.

Internal interrupt sources are masked by the **PECS_PCICMD** register *Interrupt Disable* bit and routed to one of the virtual interrupts, using the **PECS_PCIINTPIN** register. PCI Express Assert_INT*x* and Deassert_INTA messages are not masked by the **PECS_PCICMD** register *Bus Master Enable* bit. The internal interrupt is processed the same as the external Local Bus LINTi# signal.

12.4.2   Message Signaled Interrupts

The PEX 8311 supports interrupts using Message Signaled Interrupts (MSI), as defined in the *PCI r3.0*.

With this mechanism, the PEX 8311 signals an interrupt by writing to a specific memory location. The PEX 8311 uses the 64-bit Message Address version of the MSI capability structure and clears the *No Snoop* and *Relaxed Ordering* bits in the Requester Attributes. **PECS_MSIADDR**, **PECS_MSIUPPERADDR**, and **PECS_MSIDATA** registers are associated with the MSI feature. (Refer to Chapter 19, "PCI Express Configuration Registers," for details.) When an internal interrupt event occurs, the value in the **PECS_MSIDATA** register is written to the PCI Express address specified by the **PECS_MSIADDR** and **PECS_MSIUPPERADDR** registers.

The MSI feature is enabled by the **PECS_MSICTL** register *MSI Enable* bit. When MSI is enabled, the Virtual Wire Interrupt feature is disabled. MSI interrupts are generated independently of the **PECS_PCICMD** register *Interrupt Disable* bit. MSI interrupts are gated by the **PECS_PCICMD** register *Bus Master Enable* bit.

Note: *The No Snoop and Relaxed Ordering bits are cleared because the PEX 8311 does not support these features.*

12.4.2.1   PCI Express MSI Mechanism

The PCI Express MSI mechanism is compatible with the MSI Capability defined in the *PCI r3.0*.

The MSI method uses Memory Write transactions to deliver interrupts. MSI is an edge-triggered interrupt.

12.4.2.1.1   MSI Operation

At configuration time, system software traverses the function capability list. If a Capability ID of 05h is found, the function implements MSI [**PECS_MSIID**, Message Signaled Interrupts Capability ID]. System software reads the **MSI Capability Structure** registers to determine function capabilities.

The PEX 8311 supports only one MSI message; therefore, the *Multiple Message Enable* and *Multiple Message Capable* fields are always 0.

The **PECS_MSICTL** register *MSI 64-Bit Address Capable* bits are enabled, by default.

System software initializes the **MSI Capability Structure** registers with a system-specified message. If the MSI function is enabled, after an interrupt event occurs, the interrupt module generates a DWord Memory write to the address specified by the **PECS_MSIADDR** register contents. The data written is the contents of the Message Data register lower two bytes and zeros (0) in the upper two bytes. Because the *Multiple Message Enable* field is always 000b, the Interrupt Generation module is not permitted to change the low-order bits of Message data.

12.4.3   Local Interrupt Output (LINTo#)

LINTo#, or individual sources of an interrupt, are enabled, disabled, or cleared, using the PEX 8311 register bits described in this section. In addition, interrupt status bits for each interrupt source are provided.

LINTo# is a level output that remains asserted when the *Interrupt Status* or *Enable* bits are set. Interrupts can be cleared by disabling the *Interrupt Enable* bit of a source, or by clearing the cause of the interrupt. The *Local Interrupt Output Enable* bit (**LCS_INTCSR**[16]) can be used to enable or disable the LINTo# interrupt ball.

LINTo# is asserted, when enabled (**LCS_INTCSR**[16]=1), in the following cases (refer to Figure 12-2):

- DMA *Channel x Done* is set, and interrupt is enabled (**LCS_DMACSR0/1**[4]=1 and **LCS_DMAMODE0/1**[17, 10]=01b)

- DMA *Channel x Terminal Count* is reached, and interrupt is enabled (**LCS_DMADPR0/1**[2]=1 and **LCS_DMAMODE0/1**[17]=0)

- Write to **Doorbell** registers, when **LCS_INTCSR**[17]=1

- Write to **Mailbox** registers, when **LCS_INTCSR**[2]=1

- Built-In Self Test (BIST) interrupt, when **LCS_PCIBISTR**[6]=1 (bit status is reflected in **LCS_INTCSR**[23])

- PCI Power Management Power State value, **LCS_PMCSR**[1:0], changes when **LCS_INTCSR**[4]=1

- *Messaging Queue Interrupt Not Empty* and *Interrupt Not Empty Mask* bits are set (**LCS_QSR**[5:4]=11b)

12.4.3.1   Additional LINTo# Interrupts – M Mode Only

In M mode, a LINTo# interrupt is also asserted if any of the following conditions occur:

- *PCI Bus Received Master* or *Target Abort* bit is set (**LCS_PCISR**[13 or 12]=1, respectively)

- *Detected Parity Error* bit is set (**LCS_PCISR**[15]=1)

- *Direct Master Write/Direct Slave Read Local Data Parity Check Error Status* bit is set (**LCS_INTCSR**[7]=1)

- Messaging Outbound Free queue overflows

- PCI SERR# assertion if the ROOT_COMPLEX# ball is asserted Low

Each of these additional sources of LINTo# assertion in M mode can be masked by **LCS_INTCSR**[12, 6, 1:0], except for PCI Master or Target Aborts. (Refer to Figure 12-1 and Figure 12-1.) The *Local Interrupt Output Enable* bit (**LCS_INTCSR**[16]) can be used to enable or disable the LINTo# interrupt ball. TEA# is always enabled and only 256 Retries can be masked from causing TEA# assertion. Local Parity errors can be masked separately from asserting LINTo#, using **LCS_INTCSR**[6]. The LINTo# signal is a level output that remains asserted as long as the *Interrupt Status* or *Enable* bits are set.

12.4.4 Local Bus System Error, LSERR# (Local NMI) – C and J Modes Only

An LSERR# interrupt is asserted when any of the following conditions occur:

- Internal PCI Bus *Received Master Abort* (UR) or *Target Abort* (CA) bit is set (LCS_PCISR[13 or 12]=1, respectively)
- *Detected Parity Error* bit is set (**LCS_PCISR**[15]=1)
- *Direct Master Write/Direct Slave Read Local Data Parity Check Error Status* bit is set (LCS_INTCSR[7]=1)
- Messaging Outbound Free queue overflows
- Fatal and Non-Fatal error (internal SERR#) assertion when ROOT_COMPLEX# is asserted Low

LSERR# is always enabled. **LCS_INTCSR**[12, 6, 1:0] is used to enable or disable LSERR# sources. (Refer to Figure 12-2.) Local Parity errors are masked from asserting LSERR#, using **LCS_INTCSR**[6]. LSERR# is a level output that remains asserted when the *Interrupt Status* or *Enable* bits are set.

12.4.5 Built-In Self-Test Interrupt (BIST)

A PCI Express Root Complex can assert a Local interrupt by performing a PCI Express Type 1 Configuration Write to Local Configuration space (Type 1 is internally converted to Type 0) that sets the *PCI Built-In Self-Test Interrupt Enable* bit (LCS_PCIBISTR[6]=1). A Local processor can read the *BIST Interrupt Active* bit (**LCS_INTCSR**[23]) to determine whether a BIST interrupt is pending.

The Local interrupt and **LCS_INTCSR**[23] remain set when **LCS_PCIBISTR**[6]=1. The Local Bus then resets **LCS_INTCSR**[23] by way of **LCS_PCIBISTR**[6] when the BIST interrupt completes.

Note: *The PEX 8311 does **not** have an internal BIST.*

12.4.6 DMA Channel *x* Interrupt

A DMA channel can assert a PCI Express message or Local interrupt when done (transfer is complete), or, in DMA Scatter/Gather mode, after a transfer is complete for the current descriptor. The *DMA Channel Interrupt Select* bit for the affected DMA channel (LCS_DMAMODE0/**1**[17]) selects the routing of the interrupt – PCI Express or Local Bus (Assert_INTA or LINTo#, respectively). The PCI Express Root Complex or Local Bus Master can read the *DMA Channel Interrupt Active* bit for the affected DMA channel (**LCS_INTCSR**[22 and/or 21]=1) to determine whether a DMA Channel interrupt is pending.

The *DMA Channel Done* bit for the affected DMA channel (LCS_DMACSR0/**1**[4]) is used to determine whether an interrupt is one of the following:

- DMA Done interrupt
- Transfer complete for current descriptor interrupt
- DMA Transfer was aborted

The *DMA Channel Done Interrupt Enable* bit for the affected DMA channel (**LCS_DMAMODE0/1** [10]=1) enables a Done interrupt. In DMA Scatter/Gather mode, the **DMA Channel Descriptor Pointer** register *Channel Interrupt after Terminal Count* bit for the affected DMA channel (LCS_DMADPR0/**1**[2]) specifies whether to assert an interrupt at the end of the transfer for the current descriptor.

A DMA Channel interrupt is cleared by writing 1 to the *Channel Clear Interrupt* bit for the affected DMA channel (**LCS_DMACSR0/1**[3]=1).

12.5   Root Complex Mode PCI Express Interrupts

In Root Complex mode, the PEX 8311 passes PCI Express Assert_INTA or Deassert_INTA message interrupts as they are received to the Local Bus (LINTo#). The PEX 8311 recognizes only INTA types of PCI Express interrupts received on the PCI Express interface in Root Complex mode. The internal PCI Wire interrupt (INTA#) is asserted and passed to the Local Bus, independently of the **PECS_PCICMD** register *Interrupt Disable* bit. The internal PCI Wire Interrupt signal is asserted only when the PEX 8311 is in power state D0.

12.5.1   Local Interrupt Output (LINTo#)

LINTo#, or individual sources of an interrupt, are enabled, disabled, or cleared, using the PEX 8311 register bits described in this section. In addition, interrupt status bits for each interrupt source are provided.

LINTo# is a level output that remains asserted when the *Interrupt Status* or *Enable* bits are set. Interrupts can be cleared by disabling the *Interrupt Enable* bit of a source, or by clearing the cause of the interrupt. The *Local Interrupt Output Enable* bit (LCS_INTCSR[16]) can be used to enable or disable the LINTo# interrupt ball.

LINTo# is asserted, when enabled (**LCS_INTCSR**[16]=1), in the following cases (refer to Figure 12-2):

- DMA *Channel 0 Done* is set, and interrupt is enabled (LCS_DMACSR0[4]=1 and LCS_DMAMODE0[17, 10]=01b)
- DMA *Channel 0 Terminal Count* is reached, and interrupt is enabled (LCS_DMADPR0[2]=1 and **LCS_DMAMODE0**[17]=0)
- DMA *Channel 1 Done* is set, and interrupt is enabled (LCS_DMACSR1[4]=1 and LCS_DMAMODE1[17, 10]=01b)
- DMA *Channel 1 Terminal Count* is reached, and interrupt is enabled (LCS_DMADPR1[2]=1 and **LCS_DMAMODE1**[17]=0)
- Write to **Doorbell** registers, when **LCS_INTCSR**[17]=1
- Write to **Mailbox** registers, when **LCS_INTCSR**[2]=1
- Built-In Self Test (BIST) interrupt, when LCS_PCIBISTR[6]=1 (bit status is reflected in **LCS_INTCSR**[23])
- PCI Power Management Power State value, LCS_PMCSR[1:0], changes when **LCS_INTCSR**[4]=1
- *Messaging Queue Interrupt Not Empty* and *Interrupt Not Empty Mask* bits are set (LCS_QSR[5:4]=11b)
- **PECS** serial EEPROM transaction performed
- Any GPIO bit that is programmed as an input
- **Mailbox** registers written
- PCI Express Assert_INTA interrupt message (reflected in **LCS_INTCSR**[20]=1)
- Local Data Parity Error for Direct Master Write, Direct Slave Read, and DMA Local-to-PCI Express transactions

Local Parity errors are masked separately from asserting LINTo# using **LCS_INTCSR**[6].

12.5.1.1   Internal INTA# Wire Signals

When an internal interrupt event occurs, it can cause the internal INTA# wire to assert and pass to the Local Bus. Internal PCI Express interrupt sources are masked by the **PECS_PCICMD** register *Interrupt Disable* bit and are routed to the INTA# wire signals, using the **PECS_PCIINTPIN** register. The INTA# signal is asserted only when Message Signaled Interrupts (MSI) are disabled.

12.5.1.2   Message Signaled Interrupts

The PEX 8311 does not support Message Signaled Interrupts (MSI) generated by downstream devices on the PCI Express interface. With this mechanism, devices signal an interrupt by writing to a specific memory location. The PEX 8311 uses the 64-bit Message Address version of the MSI capability structure. The **PECS_MSIADDR**, **PECS_MSIUPPERADDR**, and **PECS_MSIDATA** Configuration registers are associated with the MSI feature. When an internal interrupt event occurs, the value in the **PECS_MSIDATA** register is written to one of the Local Address space address-mapped locations (Direct Slave Space 0, Direct Slave Space 1, and/or Expansion ROM) specified by the **PECS_MSIADDR** and **PECS_MSIUPPERADDR** Configuration registers.

The MSI feature is enabled by the **PECS_MSICTL** register *MSI Enable* bit. When MSI is enabled, the internal INTA# Wire Interrupt signals for internally generated interrupts are disabled. Local Bus interrupt (LINTo#) signal is not asserted. MSI interrupts are generated independently of the **PECS_PCICMD** register *Interrupt Disable* bit. MSI interrupts are gated by the **PECS_PCICMD** register *Bus Master Enable* bit.

12.5.2   PCI Express Configuration Space Mailbox Register Interrupts

The PEX 8311 PCI Express interface logic has four, 32-bit **Mailbox** registers that are written to and read from the PCI Express interface and Local Bus. These registers are used to pass command and status information directly between the PCI Express and Local Bus devices. (Refer to Figure 12-6.) For PCI Express and Local Bus Masters to access **Mailbox** registers, a Memory- or I/O-Mapped access through the **PECS_PCIBASE0** register must be performed.

In Root Complex mode, the PEX 8311 is programmed to generate Local interrupts only as a result of the Mailbox Write accesses, when enabled (**PECS_PCIIRQENB** register). To pass the interrupt to the Local Bus, LCS_INTCSR[8, 16] must be enabled. The Mailbox interrupt statuses are located in the **PECS_IRQSTAT** register. Writing 1 to a Mailbox interrupt status register clears the respective Mailbox interrupt.

Figure 12-6.   PCI Express Mailboxes

PCI Express Interface   **Local Bus**

Mailbox registers can be read and/or written from
PCI Express Interface and/or Local Bus
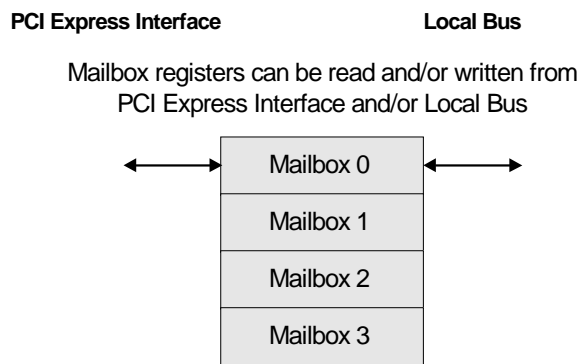
12.5.3   Local Configuration Space Mailbox Register Interrupts

The PEX 8311 Local Bus logic has eight, 32-bit **Mailbox** registers that are written to and read from the PCI Express interface and Local Bus. These registers are used to pass command and status information directly between the PCI Express and Local Bus devices. (Refer to Figure 12-4.) For PCI Express to access **Mailbox** registers, a Type 1 Configuration access (Type 1 access is internally converted to Type 0) must be performed to Local Configuration space.

A Local interrupt (LINTo#) is asserted, when enabled (**LCS_INTCSR**[3, 16]=11b), when the PCI Express Root Complex writes to one of the first four **Mailbox** registers (LCS_MBOX0, LCS_MBOX1, LCS_MBOX2, or LCS_MBOX3).

Regardless of whether LINTo# is enabled, a PCI Express write to one of these four **Mailbox** registers sets a corresponding status bit in **LCS_INTCSR**[31:28], provided the Mailbox interrupts are enabled (**LCS_INTCSR**[3]=1).

To clear the LINTo# assertion caused by the PCI Express Root Complex write(s) of any of the four **Mailbox** registers, a Local Bus device must read each **Mailbox** register that was written.

12.5.4   Doorbell Registers

The PEX 8311 has two 32-bit **Doorbell** registers. One is assigned to the PCI Express interface; the other to the Local Bus interface.

A PCI Express Root Complex can assert a Local interrupt output (LINTo#) by writing any number other than all zeros (0) to the *PCI Express-to-Local Doorbell* bits (**LCS_P2LDBELL**[31:0]). The Local Interrupt remains asserted until all **LCS_P2LDBELL** bits are cleared to 0. A Local processor can cause a PCI Express assert message interrupt generation by writing any number other than all zeros (0) to the *Local-to-PCI Express Doorbell* bits (**LCS_L2PDBELL**[31:0]). The PEX 8311 generates a PCI Express De-assert PCI Express Message interrupt after all **LCS_L2PDBELL** bits are cleared to 0h. (Refer to Figure 12-4.)

12.5.4.1   Local-to-PCI Express Interrupt

A Local Bus Master cannot cause the PEX 8311 to generate a PCI Express message interrupt by writing to the *Local-to-PCI Express Doorbell* bits (**LCS_L2PDBELL**[31:0]). In the PCI Express system interrupts are routed to the Root Complex and can only be generated upstream. When a Local Bus Master (Root Complex device) must pass information to downstream devices by way of the Local-to-PCI Express Doorbell register, it can still perform a write to the Doorbell register. Downstream devices can poll the *PCI Express Doorbell Interrupt Active* bit (**LCS_INTCSR**[13]), by way of a Memory-Mapped transaction, to determine whether a PCI Express Doorbell interrupt is pending; therefore, if **LCS_INTCSR**[13]=1, read the **LCS_L2PDBELL** register by way of a Memory-Mapped transaction.

Each **LCS_L2PDBELL** register bit is individually controlled. **LCS_L2PDBELL** register bits are set only by the Local Bus. From the Local Bus, writing 1 to any bit position sets that bit and writing 0 has no effect. **LCS_L2PDBELL** register bits are cleared only from the PCI Express interface. From the PCI Express interface, writing 1 to any bit position clears that bit and writing 0 has no effect.

12.5.4.1.1   Local-to-PCI Express Interrupt – C and J Modes

To prevent race conditions from occurring when the PCI Express interface is accessing the **LCS_L2PDBELL** register (or **LCS** Configuration registers), the PEX 8311 automatically de-asserts READY# output to prevent Local Bus Configuration accesses.

12.5.4.1.2   Local-to-PCI Express Interrupt – M Mode

To prevent race conditions from occurring when the PCI Bus is accessing the Local-to-PCI Doorbell register (**LCS_L2PDBELL**) (or any Configuration register), the PEX 8311 automatically de-asserts TA# output to prevent Local Bus Configuration accesses.

12.5.4.2   PCI Express-to-Local Interrupt

Downstream devices can assert a Local interrupt output (LINTo#) by writing 1 to any *PCI Express-to-Local Doorbell* bits (**LCS_P2LDBELL**[31:0]). The Local processor can read the *Local Doorbell Interrupt Active* bit (**LCS_INTCSR**[20]) to determine whether a Local Doorbell interrupt is pending; therefore, if **LCS_INTCSR**[20]=1, read the **LCS_P2LDBELL** register.

Each **LCS_P2LDBELL** register bit is individually controlled. **LCS_P2LDBELL** register bits are set only by the PCI Express interface. From the PCI Express interface, writing 1 to any bit position sets that bit and writing 0 has no effect. **LCS_P2LDBELL** register bits are cleared only from the Local Bus. From the Local Bus, writing 1 to any bit position clears that bit and writing 0 has no effect.

Note: *When the Local Bus cannot clear a Doorbell interrupt, do **not** use the **LCS_P2LDBELL** register.*

The Local interrupt remains set when any **LCS_P2LDBELL** register bits are set and the *Local Doorbell Interrupt Enable* bit is set (**LCS_INTCSR**[17]=1).

To prevent race conditions when the Local Bus is accessing the **LCS_P2LDBELL** register (or **LCS** Configuration registers), the PEX 8311 automatically issues an internal Retry to the PCI Express Address Spaces.

12.5.5   DMA Channel *x* Interrupt

A DMA channel can assert a Local interrupt when done (transfer is complete), or, in DMA Scatter/ Gather mode, after a transfer is complete for the current descriptor. The *DMA Channel Interrupt Select* bit for the affected DMA channel (**LCS_DMAMODE0/1**[17]) must be set to route the interrupt to Local Bus (LINTo#). In the PCI Express interface, system interrupts are routed upstream to the Root Complex. The Local Bus Master can read the *DMA Channel Interrupt Active* bit for the affected DMA channel (**LCS_INTCSR**[22 and/or 21]=1), to determine whether a DMA Channel interrupt is pending.

The *DMA Channel Done* bit for the affected DMA channel (**LCS_DMACSR0/1**[4]) is used to determine whether an interrupt is one of the following:

- DMA Done interrupt
- Transfer complete for current descriptor interrupt
- DMA Transfer was aborted

The *DMA Channel Done Interrupt Enable* bit for the affected DMA channel (**LCS_DMAMODE0/1** [10]=1) enables a Done interrupt. In DMA Scatter/Gather mode, the **DMA Channel Descriptor Pointer** register *Channel Interrupt after Terminal Count* bit for the affected DMA channel (**LCS_DMADPR0/1**[2]) specifies whether to assert an interrupt at the end of the transfer for the current descriptor.

A DMA Channel interrupt is cleared by writing 1 to the *Channel Clear Interrupt* bit for the affected DMA channel (**LCS_DMACSR0/1**[3]=1).

12.5.6   Local Interrupt Input (LINTi#)

The PEX 8311 ignores the Local Interrupt Input (LINTi#) signal assertion in Root Complex mode.

12.6   Miscellaneous

12.6.1   M Mode Local Bus TEA# Signal

The Transfer Error Acknowledge (TEA#) signal is a wired-*OR* M mode bus signal that is asserted by a Slave device on the Local Bus for one Local Bus Clock cycle.

The PEX 8311 supports TEA# assertion by the MPC850 or MPC860 processor (Local Bus Monitor Timeout logic) to the PEX 8311 when the PEX 8311 is a Local Bus Master during a Direct Slave or DMA transfer Data phase. TEA# assertion to the PEX 8311 during a Direct Slave or DMA Data transfer causes the PEX 8311 to assert a new TS# for every TEA# until the Direct Slave Write or DMA FIFO is empty or the required Read is complete through the Direct Slave Read or DMA FIFO. Additionally, SERR# is asserted, if enabled, to indicate a System error to the PCI Bus, if the *M Mode TEA# Input Interrupt Mask* bit is disabled (**LCS_LMISC1**[5]=1). The PEX 8311 never asserts TEA# when it is a Local Bus Master.

The PEX 8311 supports TEA# assertion to the MPC850 or MPC860 Processor Memory Controller when the PEX 8311 is a Slave on the Local Bus during the Data phase of Direct Master IDMA/SDMA transfers.

TEA# is enabled if **LCS_INTCSR**[0]=1. The PEX 8311 asserts TEA# when any of the following conditions occur:

- PEX 8311 Received Target Abort bit is set (**LCS_PCISR**[12]=1)
- 256 consecutive Master Retrys to a PCI Target converted to a Received Target Abort (**LCS_INTCSR**[27, 12]=11b and **LCS_PCISR**[12]=1)
- *Received Master Abort* bit is set (**LCS_PCISR**[13]=1)

If the PEX 8311 asserts TEA#, the PEX 8311stops driving the Local Bus on the next Local Bus Clock cycle.

If any of the three previously described Abort conditions occur, the following examples describe when the PEX 8311 asserts TEA# during the following types of transfers:

- For a pending Direct Master Posted Write transfer, TEA# is asserted during a Data phase on the ensuing Direct Master Read and Write accesses
- For an ongoing Direct Master Read/Write transfer, TEA# is asserted during a Data phase of the ongoing Direct Master Read/Write transfer
- For a pending (RETRY# asserted) Direct Master Delayed Read transfer, TEA# is asserted during a Data phase on the ensuing Direct Master Read and Write accesses
- For a DMA access on the PCI Bus while the MPC850 or MPC860 is arbitrating to perform a Direct Master Read or Write transfer, TEA# is asserted during a Data phase of the started Direct Master Read and Write transfer
- For a posted Direct Master write followed by a Direct Master Read transfer, TEA# is asserted during a Data phase of the ensuing Direct Master Read access

Note: *If enabled, LINTo# is immediately asserted upon detection of the Abort conditions that cause the PEX 8311 to assert TEA#.*

The PEX 8311 ignores TEA# assertion by the MPC850 or MPC860 Local Bus Monitor Timeout logic during Direct Master Read and Write IDMA/SDMA transfers.

12.6.2   M Mode PCI SERR#

The PEX 8311 also asserts SERR# and sets the Signaled System Error bit (**LCS_PCISR**[14]=1) if the
Local Bus responds with TEA# to the PEX 8311 during Direct Slave and/or DMA transfers. The
SERR# interrupt assertion can be masked by writing 0 to the *TEA# Input Interrupt Mask* bit
(**LCS_LMISC1**[5]=0).

Chapter 13 Exclusive (Locked) Access

13.1 Endpoint Mode Exclusive Accesses

The exclusive access mechanism allows non-exclusive accesses to proceed concurrently with exclusive accesses. This allows a master to hold a hardware lock across several accesses, without interfering with non-exclusive Data transfers. Masters and targets not involved in the exclusive accesses are allowed to proceed with non-exclusive accesses while another master retains a bus lock.

Exclusive access support in the PEX 8311 is enabled by the **PECS_PCICTL** register *Lock Enable* bit and **LCS_MARBR** register *Direct Slave Internal LOCK# Input Enable* bit. When the **PECS_PCICTL** register *Lock Enable* bit is cleared to 0, PCI Express Memory Read Locked requests are terminated with a completion with UR status. The PEX 8311 also supports the Local Bus LOCK (LLOCKo#) signal to assert, to monitor lock accesses. PCI Express exclusive accesses to the PEX 8311 cause Local Bus LOCK (LLOCKo#) to assert, when enabled (**LCS_CNTRL**[19]=1).

13.1.1 Lock Sequence across PEX 8311

Locked transaction sequences are generated by the Host CPU as one or more Reads followed by a number of Writes to the same locations. In Endpoint mode, the PEX 8311 supports only locked transactions in the downstream direction (PCI Express-to-Local, Direct Slave transactions). Upstream locked transactions are not allowed. The initiation of a Locked transaction sequence through the PEX 8311 is as follows:

1. Locked transaction starts with a Memory Read Locked request.

2. Successive Reads for the Locked transaction also use Memory Read Locked requests.

3. Successful Memory Read Locked requests use the CplDLk Completion type, CplD. Unsuccessful Memory Read Locked requests use the CplLk Completion type. (For further details, refer to the *PCI Express Base 1.0a*, Table 2-3.)

4. When the Locked Completion for the first Locked Read request is returned, the PEX 8311 does not accept new Local Bus-initiated requests from the internal PCI Bus to PCI Express Address space. DMA and Direct Master transactions are stacked in the PEX 8311 Local FIFOs. The Local Bus LLOCKo# signal is used to monitor PCI Express exclusive lock transactions before initiating upstream transactions.

5. Writes for the locked sequence use Memory Write requests.

6. PEX 8311 remains locked until it is unlocked by the PCI Express interface. Unlock is then propagated to the Local Bus by terminating the locked sequence.

7. PCI Express Unlock message is used to indicate the end of a locked sequence. Upon receiving an Unlock message, the PEX 8311 unlocks itself. When the PEX 8311 is not locked, it ignores the Unlock message.

When the Locked Read request is queued in the PCI Express Address space PCI Express-to-Local Non-Posted Transaction queue, subsequent Non-Posted, Non-Locked requests from the PCI Express interface are completed with Unsupported Request status. Requests queued before the Locked Read request are allowed to complete.

13.1.2   General Master Rules for Supporting Internal LOCK# Transactions

The PEX 8311 must obey the following rules when internally performing locked sequences:

- Master can access only a single resource during a Lock operation
- First transaction of a lock operation must be a Memory Read transaction
- Internal LOCK# signal must be asserted during the Clock cycle following the Address phase and held asserted to maintain control
- Internal LOCK# signal must be released when the initial transaction of the lock request is terminated with Retry (Lock was not established)
- Internal LOCK# signal must be released when an access is internally terminated by the PEX 8311 Local Bus logic Target Abort or Master Abort
- Internal LOCK# signal must be de-asserted between consecutive Lock operations for a minimum of one Clock cycle while the bus is in the Idle state

13.1.3   Acquiring Exclusive Access across PEX 8311

When a PCI Express Memory Read Locked request appears at the output of the Non-Posted Request queue, the locked request is performed to the Local Bus. The PEX 8311 monitors the internal LOCK# signal state when attempting to establish lock. When it is asserted, the PEX 8311 does not request to start the transaction to the Local Bus.

When the PEX 8311 Local Bus logic terminates the first exclusive access transaction with an internal Retry, the PEX 8311 terminates the transaction and releases the internal LOCK# signal. After the first Data phase completes, the PEX 8311 holds the internal LOCK# signal asserted, until either the lock operation completes or an internal Master Abort or Target Abort causes early termination.

When the PCI Express Exclusive Access transaction successfully locks the PEX 8311 Local Bus logic the entire address Space 0, Space 1, and Expansion ROM space on the Local Bus are locked until they are released by the PCI Express Master. Internal locked operations are enabled or disabled with the internal *LOCK# Input Enable* bit (**LCS_MARBR**[22]).

13.1.4   Non-Posted Transactions and Lock

The PEX 8311 must consider itself locked when a Memory Read Locked request is detected on the output of the Non-Posted Request queue, although no data has transferred. This condition is referred to as a target-lock. While in target-lock, the PEX 8311 does not process any new requests on the PCI Express.

The PEX 8311 locks the Local Bus when the lock sequence on the Local Bus completes (LLOCKo# is asserted). A target-lock becomes a full-lock when the locked request completes on the PCI Express. At this point, the PCI Express master has established the lock.

13.1.5   Continuing Exclusive Access

When the PEX 8311 performs another transaction to a locked Local Bus. LLOCKo# is de-asserted during the Address phase. The locked Local Bus accepts and responds to the request. LLOCKo# is asserted one Clock cycle after the Address phase to keep the target in the locked state and allow the PEX 8311 to retain ownership of LLOCKo# signal beyond the end of the current transaction.

13.1.6   Completing Exclusive Access

When the PEX 8311 receives an Unlock Message from the PCI Express, it de-asserts the internal LOCK# and Local Bus LLOCKo# signals.

13.1.7 Invalid PCI Express Requests while Locked

When the PEX 8311 is locked, it accepts only PCI Express Memory Read Locked or Memory Write transactions that are being forwarded to the Local Bus. Other types of transactions are terminated with a completion with Unsupported Request status, including Non-Posted accesses to internal Configuration registers and shared memory.

13.1.8 Locked Transaction Originating on Local Bus

Locked transactions originating on the Local Bus are not allowed to propagate to the PCI Express interface in Endpoint mode. When a locked transaction performed on the Local Bus is intended for the PEX 8311, the PEX 8311 ignores the transaction. The PEX 8311 Local Bus logic can accept the locked transaction; however, PCI Express Address space ignores it. An internal Master Abort is generated.

13.1.9 Internal PCI Bus Errors while Locked

13.1.9.1 Internal Master Abort during Posted Transaction

When an internal Master Abort occurs during a PCI Express-to-Local Bus Locked Write transaction between PCI Express Address and Local Bus Spaces, the PEX 8311 de-asserts the internal LOCK# signal. The PCI Express interface is released from the locked state, although no Unlock message is received. Write data is discarded. The LLOCKo# signal is not asserted on the Local Bus.

Refer to Section 11.1.1.4, "Internal PCI Bus Master Abort on Posted Transaction," for further details describing the action taken when a Master Abort is detected during a Posted transaction.

13.1.9.2 Internal Master Abort during Non-Posted Transaction

When an internal Master Abort occurs during a PCI Express-to-Local Bus Locked Read transaction, the PEX 8311 de-asserts internal LOCK# signal. The PCI Express interface is released from the locked state, although no Unlock message is received. A CplLk with Unsupported Request status is returned to the PCI Express interface.

Refer to Section 11.1.1.5, "Internal PCI Bus Master Abort on Non-Posted Transaction," for further details describing the action taken when a Master Abort is detected during a Non-Posted transaction.

13.1.9.3 Internal Target Abort during Posted Transaction

When an internal Target Abort occurs between PCI Express Address and Local Bus Spaces during a PCI Express-to-Local Bus Locked Write transaction, the PEX 8311 de-asserts the internal LOCK# signal. The PCI Express interface is released from the locked state, although no Unlock message is received. Write data is discarded. The LLOCKo# signal is not asserted on the Local Bus.

Refer to Section 11.1.1.6, "Internal PCI Bus Target Abort on Posted Transaction," for further details describing the action taken when a Target Abort is detected during a Posted transaction.

13.1.9.4 Internal Target Abort during Non-Posted Transaction

When an internal Target Abort occurs between PCI Express Address and Local Bus Spaces during a PCI Express-to-Local Bus Locked Read transaction, the PEX 8311 de-asserts the internal LOCK# signal. The PCI Express interface is released from the locked state, although no Unlock message is received. A CplLk with Completer Abort status is returned to the PCI Express interface. The LLOCKo# signal is not asserted on the Local Bus.

Refer to Section 11.1.1.7, "Internal PCI Bus Target Abort on Non-Posted Transaction," for further details describing the action taken when a Target Abort is detected during a Non-Posted transaction.

13.2   Root Complex Mode Exclusive Accesses

The PEX 8311 is allowed to pass Locked transactions from the Local Bus to the PCI Express (downstream direction, Direct Master transactions). When a locked request (LLOCKi# is asserted) is initiated on the Local Bus, a Memory Read Locked request is issued to the PCI Express interface. Subsequent Locked Read transactions targeting the PEX 8311 use the Memory Read Locked request on the PCI Express interface. Subsequent Locked Write transactions use the Memory Write request on the PCI Express interface. The PEX 8311 must transmit the Unlock message when Local Lock sequence is complete.

Exclusive access support in the PEX 8311 is enabled by the **PECS_PCICTL** register *Lock Enable* and **LCS_MARBR** register *Local Bus LLOCKi# Enable* bits. When these bits are cleared, the LLOCKi# signal is ignored, and Locked transactions are treated as Unlocked transactions.

13.2.1   Internal Target Rules for Supporting LLOCKi#

The following are the internal target rules for supporting LLOCKi#:

- The PEX 8311, acting as the target of an access, locks itself when the LLOCKi# signal is de-asserted during the Address phase and asserted during the following Clock cycle

- Lock is established when LLOCKi# signal is de-asserted during the Address phase, asserted during the following Clock cycle, and data is transferred during the current transaction

- After lock is established, the PEX 8311 remains locked until LLOCKi# is sampled de-asserted at the Address Phase, regardless of how the transaction is terminated

- The PEX 8311 is not allowed to accept new requests (from Local Bus or PCI Express) while it remains in a locked condition, except from the owner of LLOCKi#

13.2.2   Acquiring Exclusive Access across PEX 8311

A Local Bus Master attempts to forward a Memory Read Locked transaction to the PCI Express interface. The PEX 8311 terminates the transaction with an internal Retry, and the locked request is written to the PCI Express Address Space PCI Express-to-Local Non-Posted Transaction queue. When this locked request reaches the top of the queue, the locked request is performed on the PCI Express interface as a Memory Read Locked request. When the PCI Express responds with a Locked Completion, the Locked request is updated with completion status. When the Local Bus Master Retries or the PEX 8311 internally Retries the Memory Read Locked request, the PEX 8311 responds with the lock sequence, thereby completing the transaction.

When the PEX 8311 is locked, it only accepts Local Bus Locked transactions that are being forwarded to the PCI Express interface. Other bus transactions are terminated with an internal Retry, including accesses to the **PECS** registers and shared memory. The **LCS** registers can be successfully accessed. PCI Express requests are terminated with a completion with Unsupported Request status.

13.2.3   Completing Exclusive Access

When the PEX 8311 detects that LLOCKi# and BLAST# (for C or J mode) or LLOCKi# and BDIP# (for M mode) are de-asserted, it transmits an Unlock message to the PCI Express interface.

13.2.4   PCI Express Locked Read Request

When a Locked Read request is performed on the PCI Express interface, the PEX 8311 responds with a completion with Unsupported Request status.

Chapter 14   Power Management

14.1   Introduction

The PEX 8311 Power Management (PM) programming involves two sets of PM registers. These register sets provide programmability for the PCI Express and Local Bus bridge functions, respectively. The functions of one set of Power Management registers are largely independent of the another. The only exception is in cases where a Power Management State transition results in a reset of the bridge, because this reset is propagated to all downstream devices as well. Chapter 3, "Reset Operation and Initialization Summary," describes Power Management Reset functions.

The PEX 8311 PCI Express bridge function provides PCI-Compatible (Type 1) Extended Capability registers and PCI Function Power Management (D-State) functions, as defined in the *PCI Power Mgmt. r1.1*. In addition, it provides PCI Express Active State Link Power Management functions as per the *PCI Express Base 1.0a*, Section 5.4.1. The PEX 8311 Local Bus bridge function provides **LCS** PCI-Compatible Configuration Space registers and Power Management functions, as defined in the *PCI Power Mgmt. r1.1*.

Power Management signaling with devices on the Local Bus is performed using the PMEIN# and PMEOUT# signals, respectively. In Endpoint mode (ROOT_COMPLEX# strapped High), devices on the Local Bus assert PMEIN#, which the PEX 8311 forwards to PCI Express space as a PM_PME message. PMEOUT# has no function in Endpoint mode. In Root Complex mode, PM_PME messages received from downstream devices are passed to local devices by way of the PMEOUT# signal. PMEIN# has no function in Root Complex mode.

Because PMEIN# and PMEOUT# are directly routed to the PCI Express bridge, all Power Management signaling between devices on the Local Bus and PCI Express interface effectively bypasses the Local Bus bridge. The Local Bus bridge has no Power Management signaling capability. The **LCS Power Management** registers are limited to Local Bus bridge Power State management only.

It is the responsibility of system software to ensure that power state transitions of all devices in the system are sequenced in the proper order:

- **Endpoint mode (ROOT_COMPLEX# strapped High)** – System software should power down Local Bus devices first, then the PEX 8311 Local Bus bridge, and the PCI Express bridge last.

- **Root Complex mode (ROOT_COMPLEX# strapped Low)** – System software running on the Local processor must power down the downstream devices in PCI Express Space first, then the PCI Express bridge, and the Local Bus bridge last.

Transitions to higher-power states from low-power or power-off states, by definition, can only be performed in the order of upstream devices first, and proceeding downstream.

The remainder of this chapter is organized into the following subsections:

- Section 14.2, "Endpoint Mode PCI Express Power Management," describes PCI Express Power Management in Endpoint mode (ROOT_COMPLEX# strapped High)

- Section 14.3, "Endpoint Mode Local Bus Power Management," describes Local Bus Power Management functions supported in Endpoint mode only (ROOT_COMPLEX# strapped High)

- Section 14.4, "Root Complex Mode PCI Express Power Management," describes PCI Express Power Management in Root Complex mode (ROOT_COMPLEX# strapped Low)

14.2   Endpoint Mode PCI Express Power Management

The PEX 8311 PCI Express bridge implements PCI Express-PM capabilities and protocols, as defined in the *PCI Express Base 1.0a*, Chapter 5. PCI Express Power Management is compatible with the *PCI Power Mgmt. r1.1* (PCI-PM), and the *Advanced Configuration and Power Interface (ACPI) Specification, Revision 2.0*. In addition, PCI Express-PM also defines PCI Express-native Power Management extensions that provide capabilities beyond the scope of PCI-PM.

14.2.1   Endpoint Mode PCI Express Power Management Configuration Registers

The **PECS PCI Capabilities Pointer** (PECS_PCICAPPTR) register points to the Base address of PEX 8311 **PECS Power Management Configuration** registers (Offset 40h in the **PECS** Type 1 PCI-Compatible Configuration Space). Section 19.7, "PCI-Compatible Capability Registers," describes the PCI Express Power Management Configuration registers.

14.2.2   Endpoint Mode PCI Express-PM Link Power States (L-States)

The PEX 8311 implements the PCI Express-PM Active State Link Power Management extensions, as defined in *PCI Express Base 1.0a*, Section 5.4.1. PCI Express-PM defines a set of Link Power Management states (L-States) that a PCI Express physical Link is permitted to enter, in response to changes in the device's PCI-PM D-State or by action of PCI Express-PM Active State Power Management (ASPM) system software. Link States are native to PCI Express, and are not visible to Conventional PCI-PM software.

Table 14-1 defines the PCI Express-PM Link Power states (L-States) supported by the PEX 8311 PCI Express bridge in Endpoint mode.

Table 14-1.   PCI Express Link Power States (Endpoint Mode)

Link States	Description
L0	**Link Active** All PCI Express operations are enabled.
L0s	**Low Resume Latency, Energy-Saving "Standby" State**
L1	**Higher Latency, Lower Power "Standby" State** L1 support is required for PCI-PM compatible Power Management. L1 is optional for Active State Link Power Management. All platform-provided main power supplies and component Reference Clocks must remain active at all times in L1. The PEX 8311 internal PLLs are shut off in L1, enabling greater energy savings at a cost of increased exit latency. The L1 state is entered only when all downstream elements, including the Local Bus bridge and programmed to a D-state other than D0, or when the downstream component requests L1 entry (Active State Link PM) and receives positive acknowledgement for the request. Exit from L1 is initiated by a transaction originating in PCI Express Space targeting **LCS** registers or a device on the Local Bus, or by the need of the Local Bus bridge to initiate a transaction heading upstream. Transition from L1-to-L0 is typically a few microseconds. TLP and DLLP communication over a Link that remains in the L1 state is prohibited. The PEX 8311 only requests L1 entry for *PCI Power Mgmt. r1.1*-compatible Power Management. When PMEIN# is asserted, the PEX 8311 requests a transition from L1-to-L0.
L2/L3 Ready	**Staging Point for Removal of Main Power** State that a given Link enters into when the platform is preparing to enter its system sleep state. Following the completion of the L2/L3 Ready state transition protocol for that Link, the Link is then ready for L3 upon removal of power. The PEX 8311 responds to the PCI Express PME_Turn_Off message by returning a PME_To_Ack acknowledgement the upstream device, then transitioning to L2/L3 Ready state. The PCI Express PME_Turn_Off message terminates at the PEX 8311 PCI Express bridge and is not communicated to the Local Bus bridge nor devices on the Local Bus. While in L2/L3 Ready state, TLP and DLLP communication over the Link is disabled. As a result, the PEX 8311 does not generate PM_PME messages in response to PMEIN# assertions. The device exits from L2/L3 Ready to L0 when a request originating in PCI Express Space targeting the PEX 8311 Local Bus bridge is received before main power is removed and the platform power manager decides not to enter the system sleep state. A Link's transition into the L2/L3 Ready state is one of the final stages involving PCI Express protocol, leading up to the platform entering a system sleep state wherein main power is shut off (*such as*, ACPI S3 or S4 sleep state).
L2	*Not supported* The PEX 8311 does not provide auxiliary power support and therefore does not support the L2 state. L2/L3-to-L2 transitions settle directly into the L3 state.
L3	**Link-Off State** Power-off state.

14.2.3   Endpoint Mode Link State Transitions

Figure 14-1 illustrates the L-state transitions that occur during the course of Link operations in Endpoint mode (ROOT_COMPLEX# strapped High). Indicated in the figure is a case wherein the platform does not provide Vaux. Transitions from one L-state to another always pass through the L0 state during the transition process, with the exceptions of the L2/L3 Ready-to-L2 or L2/L3 Ready-to-L3 transitions. When in the L2/L3 Ready state, the device is ready for removal of power, and no TLP nor DLLP communication is possible on the Link. From this state, therefore, the L-State directly transitions to L3 when main power is removed as a result of a D-state transition to D3. Because L2 is *not supported* on the PEX 8311, L2/L3 Ready-to-L2 directly settle into the L3 state.

The following sequence, leading up to entering a system sleep state, illustrates the multi-step Link state transition process:

1. System software directs all PEX 8311 functions to the D3hot state.

2. The PEX 8311 initiates the Link's transition to the L1 state, as required.

3. System software causes the Root Complex to broadcast the PME_Turn_Off message to the PEX 8311, in preparation for removing the main power source.

4. The PME_Turn_Off message causes the PEX 8311 Link to transition (return) to L0 to transmit a PME_To_Ack message in response.

5. After the PME_To_Ack message is transmitted, the PEX 8311 Link transitions to the L2/L3 Ready state.

In summary:

- L0 –> L1 –> L0 –> L2/L3 Ready

- L2/L3 Ready entry sequence is initiated at the completion of the PME_Turn_Off/PME_To_Ack protocol handshake

Figure 14-1.   L-State Transitions during Link Operations
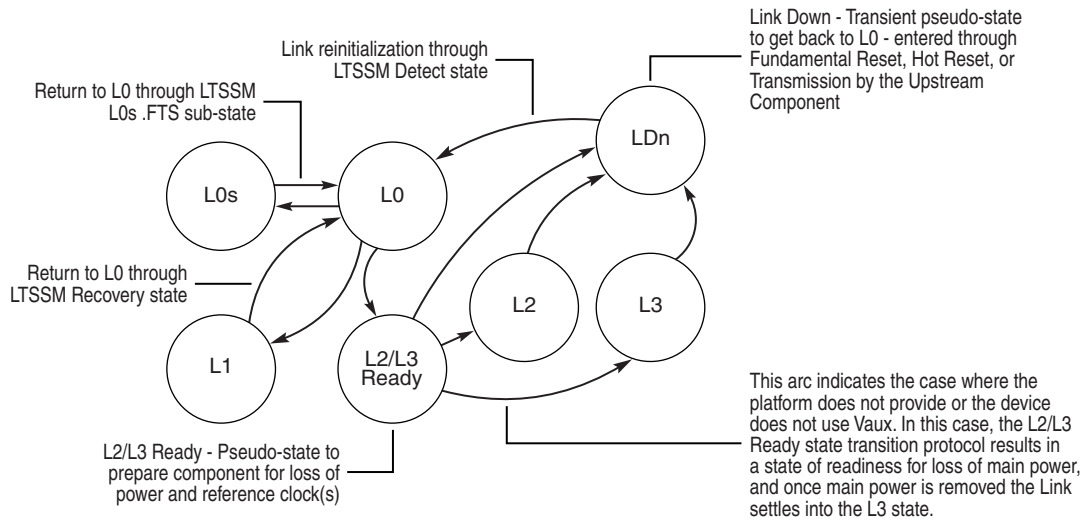
Note: In this case, the L2/L3 Ready state transition protocol results in a state of readiness for loss of main power, and after removal, the Link settles into the L3 state.

It is also possible to remove power without first placing all devices into the D3hot state:

1. System software causes the Root Complex to broadcast the PME_Turn_Off message, in preparation for removing the main power source.

2. The PEX 8311 responds with a PME_To_Ack message.

3. After the PME_To_Ack message is transmitted, the PEX 8311 component initiates the L2/L3 Ready transition protocol.

In summary:

- L0 –> L2/L3 Ready

14.2.4 Endpoint Mode PCI Express-PM Device Power States (D-States)

Table 14-2 defines the PCI-PM power states (D-States) supported by the PEX 8311 in Endpoint mode (ROOT_COMPLEX# strapped High). The PCI-PM power state is programmable by way of the **PECS Power Management Control/Status** register *Power State* field (**PECS_PWRMNGCSR**[1:0]). A D3hot-to-D0 state change results in a Fundamental Reset of the PEX 8311, which is propagated to all devices on the Local Bus. Following a D3hot-to-D0 transition, system software must allow a minimum reset recovery time of at least 10 ms (Note: actual recovery time is 70 ms; see erratum titled 'D3hot to D0 Reset') before attempting accesses to the PEX 8311. Any attempt to access the PEX 8311 during the reset recovery time (including Configuration Request packets) results in undefined behavior.

Table 14-2.   PCI Express Bridge PCI-PM Power States (Endpoint Mode)

D-State	Description
D0_uninitialized	**Power-On Default State** Entered when power is initially applied. The **PECS_PCICMD** register *I/O Access Enable*, *Memory Space Enable*, and *Bus Master Enable* bits are all cleared to 0.
D0_active	**Fully Operational** Follows action by system software to initialize the **PECS PCI-Compatible Configuration** registers, or to restore them from a previously saved context. At least one of the following **PECS_PCICMD** register bits must be set: • *I/O Access Enable* • *Memory Space Enable* • *Bus Master Enable*
D1	**Light Sleep** Only PCI Express Type-1 Configuration accesses are supported. All other requests received are completed with an Unsupported Request (UR) status. With the exception of PME messages, all PCI Express message generation is disabled.
D2	**Heavy Sleep** *Not supported* Same restrictions as D1.
D3hot	**Ready for Power-Off** The PEX 8311 register contents are not maintained. Only PCI Express Type 1 Configuration request types are accepted. All other requests received are completed with an Unsupported Request (UR) status. With the exception of PME messages, all PCI Express message generation is disabled. From this state, the next power state is D3cold or D0_uninitialized. When transitioning from D3hot-to-D0, a full-device, Fundamental Reset of the PEX 8311 and all Local Bus hardware is automatically generated.
D3cold	**Power-Off** A power-on sequence transitions a function from the D3cold state to the D0_uninitialized state. At this point, software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its D0_active state.

14.2.5   Endpoint Mode Power Management Event Signaling

Local Bus devices assert PMEIN# to signal a Power Management Event (PME) upstream to the system, usually to wake the system from a low-power sleep state. The PEX 8311 responds to PMEIN# assertions by transmitting a PM_PME message upstream to PCI Express space. There are no internal sources for PM_PME message generation by the PEX 8311.

Power Management messages are used to signal system software that one or more devices on the PEX 8311 Local Bus is signaling a Power Management event (PME). Because multiple devices can be wire-ORed to a single PMEIN# signal, system software must identify the source of a PCI PME that is reported by a PM_PME message. When the PME originates from an agent on the PEX 8311 Local Bus, the PM_PME Message Requester ID reports that the Bus Number of the Local Bus bridge (PECS_SECBUSNUM register), with Device Number and Function Number are zero (0).

When the PME message is transmitted to the host, the **PECS Power Management Control/Status** register *PME Status* bit is set (**PECS_PWRMNGCSR**[15]=1) and a 100 ms timer is started. If the *PME Status* bit is not cleared by system software within 100 ms, another PME message is transmitted.

When the system is ready to power-down the PEX 8311, it places the PEX 8311's PCI Express bridge into the D3hot power state (**PECS_PWRMNGCSR**[1:0]=11b). It then programs the Root Complex to broadcast a PCI Express PME_Turn_Off message to all downstream devices. Upon receiving the PME_Turn_Off message, the PEX 8311 transmits a PME_To_Ack message upstream and transitions its Link to the L2/L3 Ready state, ready to be powered down. All PCI Express message generation, including PME messages, are disabled at this time.

When the upstream device returns the PEX 8311 power state to D0, PME messages are re-enabled. The PCI Express PME_Turn_Off message terminates at the PEX 8311, and is not communicated to downstream devices.

The PEX 8311 polls PMEIN# every 256 ms. A PCI Express PM_PME message is generated when PMEIN# is asserted High-to-Low.

14.2.6   Set Slot Power

When a PCI Express Link first comes up, or the Root Complex **Slot Capabilities** register *Slot Power Limit Value* or *Slot Power Limit Scale* fields (**PECS_SLOTCAP**[14:7 or 16:15], respectively) are changed, the Root Complex transmits a Set Slot Power message. When the PEX 8311 receives this message, it updates the **PECS Device Capabilities** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields (**PECS_DEVCAP**[25:18 or 27:26], respectively).

When the available power indicated by the **PECS Device Capabilities** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields is greater than or equal to the power requirement indicated in the **PECS_POWER** (101Ch) register, the PWR_OK signal is asserted.

14.3   Endpoint Mode Local Bus Power Management

Local Bus bridge Power Management functions are supported in Endpoint mode only (Root Complex# strapped High). For Root Complex mode (ROOT_COMPLEX# strapped Low), the PCI Express bridge provides the Power Management functions for all downstream devices, as described in Section 14.4.

The PEX 8311 Local Bus bridge provides PCI-compatible configuration space registers and PCI-PM functions, as defined in the *PCI Express Base 1.0a.* These functions provide the means for Power Management system software to:

- Get Power Management Capabilities
- Set Power State
- Get Power Status

PME signaling between the PCI Express interface and Local Bus is provided by the PEX 8311 PCI Express bridge. (Refer to Section 14.2 and Section 14.4). The PEX 8311 Local Bus bridge has no PME signals associated with it. The **LCS Power Management Control/Status** register *PME_En* and *PME_Status* bits (LCS_PMCSR[8, 15], respectively) have no function, and therefore should not be enabled.

There is no inherent power-saving capability provided by the PEX 8311 Local Bus bridge. If the Local Bus bridge is idle, changing the **LCS Power Management Control/Status** register *Power State* field (**LCS_PMCSR**[1:0]) from D0_active-to-D3hot does not reduce the power consumed. It simply places the Local Bus bridge in a lower "function" state, thereby preventing any actions that could increase power consumption.

14.3.1   Local Bus Bridge Power Management Configuration Registers

The **LCS PCI Status** register (LCS_PCISR) and **LCS New Capability Pointer** register (LCS_CAP_PTR) indicate whether a new capability (*such as*, a Power Management function) is available. System software detects that New Capability function support is provided when the **LCS PCI Status** register *New Capability Functions Support* bit is set (**LCS_PCISR**[4]=1). This bit is readable from the PCI Express interface and Local Bus, and writable only from the Local Bus. **LCS_CAP_PTR** provides an offset into **LCS** PCI Configuration Space, which is the location of the first item in a New Capabilities Linked List.

The **LCS Power Management Capability ID** register (LCS_PMCAPID) specifies the PCI-SIG-assigned Power Management Capability ID, 01h. The **LCS Power Management Next Capability Pointer** register (LCS_PMNEXT) points to the first location of the next item in the Capabilities Linked list. If Power Management is the last item in the list, clear this register to 00h.

Note: *The default value for **LCS_PMNEXT** is 48h, which points to the Conventional PCI, PCI 9x56-compatible Hot Swap Extended Capabilities registers. The PEX 8311, however, does **not support** Hot Swap functions; therefore, **LCS_PMNEXT** should be loaded from the LCS Serial EEPROM with 00h (end of Linked list) or with 4Ch (offset location of the **PCI Vital Product Identification** register, **LCS_PVPDID**) to access VPD.*

14.3.2   Local Bus Bridge Device Power States (D-States)

The PEX 8311 Local Bus bridge implements PCI-PM power states (D-States), as defined in the *PCI Express Base 1.0a*. Power states are programmed by way of the **LCS Power Management Control/Status** register *Power State* field (LCS_PMCSR[1:0]). Table 14-3 defines the supported power states.

The transition from the D3hot-to-D0 state causes an automatic Full Reset of the Local Bus bridge. Following the reset, the PEX 8311 reloads the LCS registers from the serial EEPROM, overwriting values that were modified by system software at enumeration time, *such as* the **LCS PCIBAR*x*** registers and **LCS Internal PCI Interrupt Line** register (LCS_PCIILR) value (IRQ assignment) contents. It is the responsibility of system software to save affected LCS PCI-Compatible Configuration registers prior to this time and to restore them following the D3hot-to-D0 state transition.

Table 14-3.   Local Bus Bridge PCI-PM Power States

D-State	Description
D0_uninitialized	**Power-On Default State** Entered following power-on, reset, or from D3hot. Supports CCS# Configuration accesses from the Local Bus. Supports Type 1 (internally converted to Type 0) Configuration accesses from PCI Express Space after the *Local Init Status* bit is set (LCS_LMISC1[2]=1) by a Local Master or from the **LCS** serial EEPROM.
D0_active	**Fully Operational** Entry implies that system software has initialized the **LCS PCI-Compatible Configuration** registers or restored them from values saved prior to entering D3hot. At least one of the following **LCS PCI Command** register (LCS_PCICR) bits must be set: • *I/O Access Enable* (bit 0) • *Memory Space Enable* (bit 1) • *Bus Master Enable* (bit 2)
D1	**Light Sleep** Only PCI Express Type 1 Configuration accesses are supported. All other PCI Express requests received are completed with an Unsupported Request (UR) status.
D2	**Heavy Sleep** *Not supported* Same restrictions as D1.
D3hot	**Ready for Power-Off** LCS register contents are *not* maintained. Only PCI Express Type 1 Configuration request types are accepted. All Local interrupt sources are disabled. From this state, the next power state is D3cold or D0_uninitialized. When transitioning from D3hot-to-D0, a full-device, Fundamental Reset of the PEX 8311 and all Local Bus hardware is automatically generated.
D3cold	**Power-Off**

14.3.3   Local Interrupt (LINTo#) Options

LINTo#, when enabled, can be asserted to signal Local Bus processors any time the **LCS Power Management Control/Status** register *Power State* field (LCS_PMCSR[1:0]) is modified by system software. *For example*, LINTo# can be used to pass an interrupt to Local processors when system software updates the **LCS** *Power State* field in preparation for power down. To enable LINTo# assertion, set the **LCS Interrupt Control/Status** register *Local Interrupt Output Enable* and *Power Management Interrupt Enable* bits (LCS_INTCSR[16, 4]=11b, respectively) and clear the interrupt by setting the *Power Management Interrupt* bit (**LCS_INTCSR**[5]=1).

The *Data_Scale* field (**LCS_PMCSR**[14:13]) indicates the scaling factor to use when interpreting the value of the *Power Management Data* field (LCS_PMDATA[7:0]). The value and meaning of this field depends upon the data value specified in the *Data_Select* field (**LCS_PMCSR**[12:9]). The *Data_Scale* field value is unique for each *Data_Select* bit combination. For *Data_Select* values from 8 to 15, the *Data_Scale* field always returns zero (**LCS_PMCSR**[14:13]=00b).

LCS_PMDATA provides static operating data, *such as* power consumed or heat dissipation.

14.3.4   D0-to-D3hot Power-Down Example

This following sequence transitions the Local Bus bridge to the D3hot state in preparation for power-off:

1. System software writes to the **LCS Power Management Control/Status** register to change the power state to D3hot (LCS_PMCSR[1:0]=11b).

2. If enabled (LCS_INTCSR[16]=1), the PEX 8311 asserts LINTo# following the **LCS** D-State change.

3. The Local CPU has 200 μs to read the Power Management information from the PEX 8311 LCS_PMCSR register, save all volatile register data, and implement the power-saving function.

4. After the Local CPU implements the power-saving function, all Local Bus devices are in their lowest power configuration, and ready for power-down.

5. System software clears **LCS PCI Control** register (**LCS_PCICR[2:1]** = 00b), disabling Direct Master and Direct Slave spaces, and the DMA Channels on the Local Bus bridge. In addition, PCI Express interrupt generation is disabled (LCS_INTCSR[8]=0).

Note: *In the D3hot state, only Type 1 Configuration Access requests from the PCI Express interface or CCS# Register accesses from Local Bus cycles are granted. The PEX 8311 automatically performs a Soft Reset to the Local Bus on D3-to-D0 power state transitions, then reloads the Configuration register values stored in the serial EEPROM.*

14.4   **Root Complex Mode PCI Express Power Management**

When the PEX 8311 PCI Express interface is configured as a downstream-facing port (ROOT_COMPLEX# strapped Low), the PEX 8311 PCI Express interface implements PCI Express Active State Power Management (ASPM) functions and protocols, as defined in the *PCI Express Base 1.0a*, Section 5.4.1.

14.4.1   **Root Complex Active State Power Management (ASPM)**

14.4.1.1   **ASPM Link Power States (L-States)**

Table 14-4 defines the Link power states supported by the PEX 8311 in Root Complex mode.

Table 14-4.   Supported Link Power States (Root Complex Mode)

Link Power State	Description
L0	**Active State** All PCI Express operations are enabled.
L0s	**Low-Resume Latency, Energy-Saving "Standby" State** When enabled by the serial EEPROM or external driver, the PEX 8311 transmitter transitions to L0s after a low resume latency, energy-saving "standby" state. L0s support is required for Active State Link Power Management (ASPM). It is not applicable to *PCI Power Mgmt. r1.1*-compatible Power Management. All main power supplies, component Reference Clocks, and components' internal PLLs must always remain active during L0s. TLP and DLLP communication is disabled in this state. L0s is used exclusively for PCI Express-native ASPM functions. The PCI Express physical layer provides mechanisms for quick transitions from L0s-to-L0. When common (distributed) Reference Clocks are used on both sides of a given Link, the transition time from L0s-to-L0 is typically fewer than 100 symbol times.
L1	**Higher-Latency, Lower-Power "Standby" State** L1 support is required for PCI-PM-compatible Power Management. L1 is optional for ASPM. All platform-provided main power supplies and component Reference Clocks must always remain active in L1. A component's internal PLLs are shut off in L1, enabling greater energy savings at a cost of increased exit latency. The L1 state is entered when all functions of a downstream component on a given PCI Express Link are programmed to a D-state other than D0, or when the downstream component requests L1 entry (Active State Link PM) and receives positive acknowledgement for the request. Exit from L1 is initiated by an upstream-initiated transaction targeting the downstream component, or by the downstream component's need to initiate a transaction heading upstream. Transition from L1-to-L0 is typically a few microseconds. TLP and DLLP communication over a Link that remains in the L1 state is prohibited.
L2/L3 Ready	**Staging Point for Removal of Main Power** L2/L3 Ready transition protocol support is required. The L2/L3 Ready state is related to *PCI Power Mgmt. r1.1* D-state transitions. L2/L3 Ready is the state that a given Link enters into when the platform is preparing to enter its system sleep state. Following the completion of the L2/L3 Ready state transition protocol for that Link, the Link is then ready for L2 or L3; the Link is not actually in either of those states until main power is removed. If the platform implements a Vaux Supply voltage, after main power is removed, the Link settles into the L2 state; otherwise, it settles into the L3 state. The PEX 8311 does not have Vaux capability; however, it supports L2 when the system Vaux supply is used as the main power to the PEX 8311. The L2/L3 Ready state entry transition process must start as soon as possible, following PME_To_Ack TLP acknowledgment of a PME_Turn_Off message. The downstream component initiates L2/L3 Ready entry by injecting a PM_Enter_L23 DLLP onto its Transmit port. TLP and DLLP communication over a Link that remains in L2/L3 Ready is prohibited. The device exits from L2/L3 Ready to L0 when an upstream-initiated transaction targeting the downstream device occurs before main power is removed and the platform power manager decides not to enter the system sleep state. A Link's transition into the L2/L3 Ready state is one of the final stages involving PCI Express protocol, leading up to the platform entering into a system sleep state wherein main power is shut off (*for example*, ACPI S3 or S4 sleep state).
L2	**Auxiliary-Powered Link Deep Energy-Saving State**
L3	**Link-Off State** Power-off state.

14.4.2   Root Complex PCI Express-PM Device Power Management

The PEX 8311 provides the PCI Express-PM Configuration registers and functions, as defined in *PCI Express Base 1.0a* and *PCI Power Mgmt. r1.1*. The **PECS PCI Capabilities Pointer** (PECS_PCICAPPTR) register points to the Base address of PEX 8311 **PECS Power Management Configuration** registers (Offset 40h in the **PECS** Type 1 PCI-Compatible Configuration Space). Section 19.7, "PCI-Compatible Capability Registers," describes the PCI Express Power Management Configuration registers.

14.4.2.1   Power States

Table 14-5 defines the power states supported by the PEX 8311, selectable by way of the PECS Power Management Control/Status register Power State field, PECS_PWRMNGCSR[1:0].

Table 14-5.   PCI Express Bridge Power States (Root Complex Mode)

D-State	Description
D0_uninitialized	**Power-On Default State** Entered when power is initially applied. The **PECS_PCICMD** register *I/O Access Enable*, *Memory Space Enable*, and *Bus Master Enable* bits are all cleared to 0.
D0_active	**Fully Operational** Follows action by system software to initialize the PECS PCI-Compatible Configuration registers, or to restore them from a previously saved context. At least one of the following **PECS_PCICMD** register bits must be set: • *I/O Access Enable* (bit 0 • *Memory Space Enable* (bit 1) • *Bus Master Enable* (bit 2)
D1	**Light Sleep** Only Direct Master Type 1 Configuration accesses or LCS register accesses (by way of CCS#) are accepted by the PEX 8311's Local Bus. All other Direct Master accesses result in a Master Abort on the internal PCI Bus. PCI Express interrupts, by way of LINTo#, are disabled (other LINTo# sources on the PEX 8311 Local Bus bridge are not affected). The PMEOUT# signal is asserted and the PCI clock continues to run.
D2	**Heavy Sleep** Same as D1, except that the PCI Host stops the PCI clock.
D3hot	**Ready for Power-Off** Configuration register values are not maintained. Only Direct Master Type 1 Configuration accesses or **LCS** register accesses (by way of CCS#) are accepted by the PEX 8311's Local Bus. All other Direct Master accesses result in a Master Abort on the internal PCI Bus. From this state, the next power state is D3cold or D0_uninitialized. When transitioning from D3hot-to-D0, the PEX 8311's PCI Express bridge is reset, and an LTTSM Hot Reset training sequence is transmitted to the downstream device(s) in PCI Express Space.
D3cold	**Device is Powered Off** A power-on sequence transitions a function from the D3cold-to-D0_uninitialized. At this point, software must perform a full initialization of the function to re-establish all functional context, completing the restoration of the function to its D0_active state.

14.4.3   Root Complex PMEOUT# Signal

PME messages from the PCI Express interface are translated to the PCI backplane PMEOUT# signal on the PEX 8311. The **PECS Power Management Control/Status** register *PME Status* bit is set (**PECS_PWRMNGCSR**[15]=1) on the occurrence of one or more of the following events:

- PEX 8311 receives a PCI Express PM_PME message from the downstream PCI Express device
- PEX 8311 WAKEIN# signal is asserted by the downstream device
- A PCI Express beacon is detected
- The PCI Express Link transitions to the L2/L3 Ready state

PMEOUT# is asserted when the *PME Status* bit is set and PME is enabled (**PECS_PWRMNGCSR** [15, 8]=11b).

14.4.4   Root Complex Power Down Sequence

This section lists the sequence required to place the PEX 8311 PCI Express bridge in a powered-down state. (The PEX 8311's Local Bus bridge must be in the D0 state and ready to forward Direct Master Type 1 Configuration transactions to the PCI Express bridge.)

During a Link power-down, the following sequence occurs:

1. System software on the Local processor, by way of Direct Master Type 1 Configuration accesses, places all PCI Express devices downstream of the PEX 8311 in the D3hot power state.
2. PEX 8311 initiates a transition to the L1 Link state.
3. Local Processor places PEX 8311 PCI Express bridge in the D3hot power state.
4. PEX 8311 initiates a transition to L0 Link state.
5. PEX 8311 generates a PCI Express PME_Turn_Off message to the downstream PCI Express device.
6. Downstream device responds with a PME_To_Ack message.
7. Downstream device transmits a DLLP to request transition to the L2/L3 Ready state (L2.Idle Link state).
8. PEX 8311 acknowledges the request, completing the transition to the L2.Idle Link state.
9. PMEOUT# signal is asserted to the PEX 8311 Local Bus.
10. PEX 8311 is ready for power-down.

14.4.5   Root Complex Set Slot Power

When a PCI Express Link first comes up, or the **Slot Capabilities** register *Slot Power Limit Value* or *Slot Power Limit Scale* fields (**PECS_SLOTCAP**[14:7 or 16:15], respectively) are changed, the PEX 8311 transmits a Set Slot Power message to the downstream PCI Express device. When the downstream device receives this message, it updates the **PECS Device Capabilities** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields (**PECS_DEVCAP**[25:18 or 27:26], respectively).

LINTo# is asserted each time the power state in **LCS_PMCSR**[1:0] changes. The transition from the D3hot power state to the D0 power state causes a soft reset. A soft reset should be initiated only from the PCI Bus because the Local Bus interface is reset during a Soft Reset. In Adapter mode (ROOT_COMPLEX#=1), the PEX 8311 issues LRESET# and resets Local Configuration and Messaging Queue registers, Local Bus logic, PCI and Local DMA logic, and all FIFOs. After power-on reset is complete, the PEX 8311 reloads its original values, overwriting the **PCI Interrupt Line** register (**LCS_PCIILR**) value (IRQ assignment) contents. The driver must save the **LCS_PCIILR** value before entering the Power Management state for restoration. To allow LINTo# to assert, set the *LINTo# Enable* and *Power Management Interrupt Enable* bits (**LCS_INTCSR**[16, 4]=11b, respectively) and clear the interrupt by setting the *Power Management Interrupt* bit (**LCS_INTCSR**[5]=1).

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Chapter 15   PCI Express Messages

15.1   Endpoint Mode PCI Express Messages

PCI Express defines a set of messages that are for in-band communication of events (*such as* interrupts), generally replacing the need for sideband signals. These messages can also be used for general-purpose messaging. This section describes the PCI Express-to-Local Bus support requirements for these messages.

PCI Express messages are routed explicitly or implicitly, depending on specific field encodings in the message request header. An explicitly routed message is routed based on a specific address, or an ID field contained within the message header. The destination of an implicitly routed message is inferred from the message *Type* field.

15.1.1   PCI INTA# Virtual Wire Interrupt Signaling

INTA# Interrupt Signaling messages are used for in-band communication to the Local Bus. (Refer to Section 12.2, "Endpoint Mode PCI Express Interrupts," for details.)

15.1.2   Power Management Messages

Power Management messages support Power Management Events, signaled by sources integrated into the PEX 8311 and for Local Bus devices. (Refer to Section 14.2, "Endpoint Mode PCI Express Power Management," for details.)

15.1.3   Error Signaling Messages

The PEX 8311 bridge transmits Error Signaling messages on the PCI Express interface, to signal errors for any of the following:

- A particular transaction
- The Link Interface
- Errors internal to the bridge
- Local-related errors detected on the Local Bus interface

The message types include ERR_COR, ERR_FATAL, and ERR_NONFATAL. The relevant Mask bits are located in the PCI Express Capability structure. (Refer to Section 11.1, "Endpoint Mode Error Handling," for details.)

15.1.4   Locked Transactions Support

PCI Express Unlock messages support Locked Transaction sequences in the downstream direction. (Refer to Section 13.1, "Endpoint Mode Exclusive Accesses," for details.)

15.1.5   Slot Power Limit Support

The Root Complex or a switch transmit the Set_Slot_Power_Limit message to endpoints, including bridges. The PEX 8311 supports and complies with these messages. These messages are particularly relevant to devices implemented on add-in boards. (Refer to Section 14.4, "Root Complex Mode PCI Express Power Management," for details.)

15.1.6   Hot Plug Signaling Messages

The PEX 8311 does *not support* Hot Plug signaling, and ignores the associated messages.

15.2   Root Complex Mode PCI Express Messages

In Root Complex mode (ROOT_COMPLEX# strapped Low), the PEX 8311 provides support for the following message types:

- PCI Express Virtual Wire interrupts
- Power Management interrupts
- Error messages

15.2.1   PCI INTA# Virtual Wire Interrupt Message Support

The PEX 8311 controls the state of the corresponding Local Bus interrupt balls, based on the Assert_INTA and Deassert_INTA messages received. (Refer to Section 12.5, "Root Complex Mode PCI Express Interrupts," for details.)

15.2.2   Power Management Message Support

The PEX 8311 generates a PME_Turn_Off message when placed into power state D3. The PEX 8311 then waits for the PME_To_Ack message from the downstream device on the PCI Express interface before proceeding with the power-down sequence.

15.2.2.1   PME Handling Requirements

The PEX 8311 asserts PMEOUT# on the Local Bus for the following PCI Express events:

- PCI Express WAKEIN# signal is asserted while the Link is in the L2 state
- PCI Express beacon is received while the Link is in the L2 state
- PCI Express PM_PME message is received

For compatibility with existing software, the PEX 8311 does not signal PMEOUT# unless PMEOUT# signaling is enabled by the **PECS Power Management Control/Status** register *PME Enable* bit (**PECS_PWRMNGCSR**[8]=1). The PEX 8311 sets the *PME Status* bit when PMEOUT# is signaled and clears PMEOUT# when the **PECS Power Management Control/Status** register *PME Status* or *PME Enable* bit is cleared (**PECS_PWRMNGCSR**[15 or 8]=0). PME messages received while the *PME Enable* bit is cleared are ignored and the *PME Status* bit is not set during this time.

15.2.3   Error Signaling Message Support

The PEX 8311 converts ERR_COR, ERR_FATAL, and ERR_NONFATAL messages to LSERR# (C or J mode) or LINTo# (M mode) on the Local Bus. (Refer to Section 11.2, "Root Complex Mode Error Handling," for details.)

15.2.4   Locked Transaction Support

The PEX 8311 is allowed to pass Locked transactions from the Local Bus to the PCI Express interface. The PEX 8311 uses the Memory Read Locked request to initiate a locked sequence when a locked request is transmitted on the Local Bus. Subsequent Locked Read transactions targeting the bridge use the Memory Read Locked request on PCI Express. Subsequent Locked Write transactions use the Memory Write request on the PCI Express interface. The PEX 8311 transmits the Unlock message when the Local Lock sequence is complete. (Refer to Section 13.2, "Root Complex Mode Exclusive Accesses," for details.)

15.2.5   Slot Power Limit Support

The Root Complex transmits the Set Slot Power Limit message to endpoints. The PEX 8311 supports and complies with these messages. These messages are particularly relevant to devices implemented on add-in boards. (Refer to Section 14.4, "Root Complex Mode PCI Express Power Management," for details.)

Chapter 16   Intelligent I/O (I$_2$O)

16.1   Introduction

This chapter discusses the I$_2$O-compatible Messaging Unit.

16.2   I$_2$O-Compatible Messaging Unit

The I$_2$O-compatible Messaging Unit supplies two message paths (refer to the *I$_2$O r1.5* for details):

- Two inbound FIFOs to receive messages from the PCI Express interface
- Two outbound FIFOs to pass messages to the PCI Express interface

The **I$_2$O-compatible Messaging Unit Configuration** registers are located in Local Configuration Space (**LCS**). Accesses to these registers from the PCI Express interface are accomplished by way of Memory-Mapped transactions.

Figure 16-1 and Figure 16-2 illustrate I$_2$O architecture.

Figure 16-1.   Typical I$_2$O Server/Endpoint Board Design
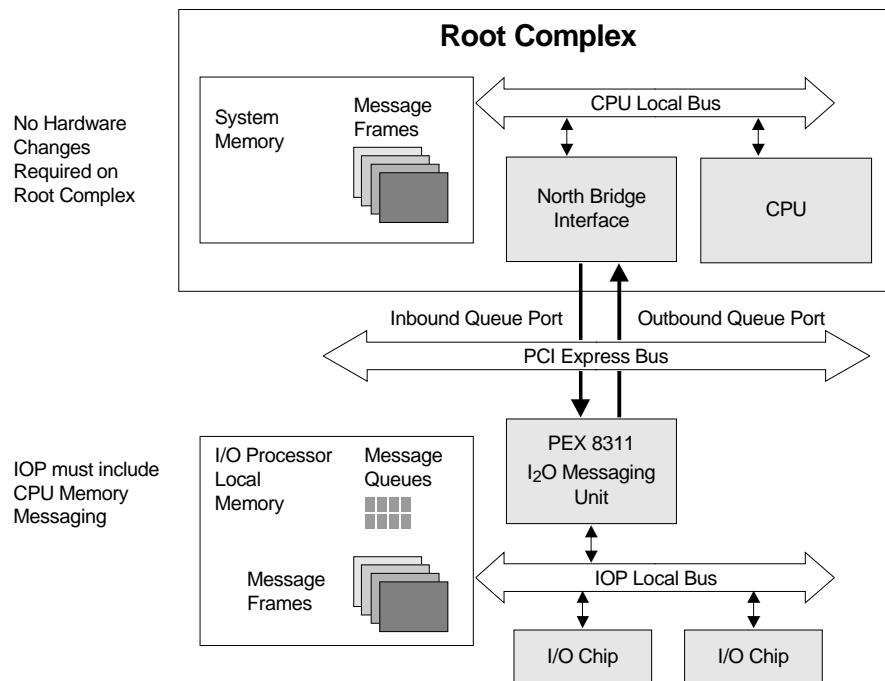
Figure 16-2.   Driver Architecture Compared
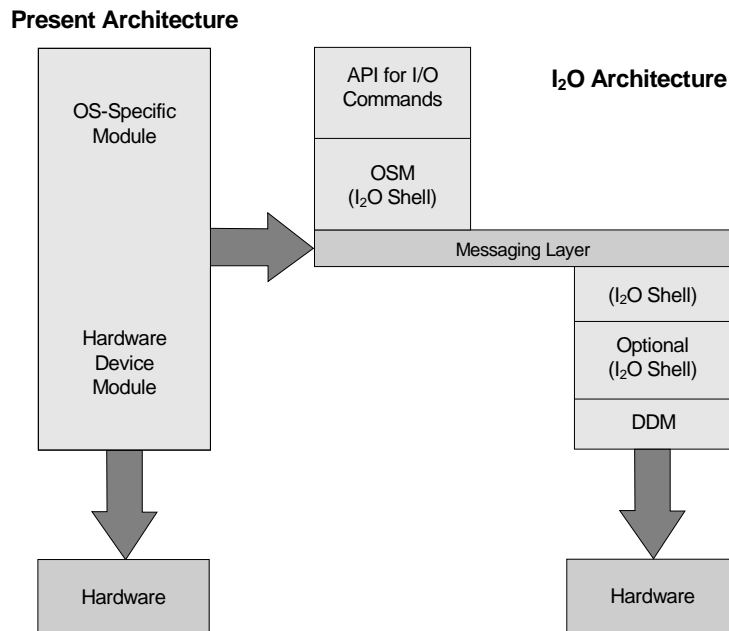
Note: *The acronyms used in Figure 16-2 are defined as follows:*

- *OS – Operating System*
- *OSM – Operating System Manager*
- *API – Application Programming Interface*
- *DDM – Driver Developing Manager*

16.2.1 Inbound Messages

Inbound messages reside in a pool of message frames (minimum 64-byte frames) allocated in the shared Local Bus I/O Processor (IOP) memory. The Inbound Message queue is comprised of a pair of rotating FIFOs implemented in Local memory. The Inbound Free List FIFO holds the Message Frame Addresses (MFAs) of available message frames in Local memory. The Inbound Post Queue FIFO holds the MFAs of all currently posted messages in Local Bus IOP memory.

External PCI Express agents, through the Inbound Queue Port location in PCI Express Address space, access the inbound circular FIFOs. (Refer to Table 16-2.) The Inbound Queue Port, when read by an external PCI Express agent, returns an Inbound Free List FIFO MFA. The external PCI Express agent places the MFA into the Inbound Post Queue FIFO by writing its MFA to the Inbound Queue Port location.

16.2.2 Outbound Messages

Outbound messages reside in a pool of message frames (minimum 64-byte frames) allocated in the shared PCI Express interface (System) memory. The Outbound Message queue is comprised of a pair of rotating FIFOs implemented in Local memory. The Outbound Free List FIFO holds the MFAs of available message frames in the System memory. The Outbound Post Queue FIFO holds the MFAs of all currently posted messages in the Local Bus (IOP) memory.

External PCI Express agents, through the Outbound Queue Port location in PCI Express Address space, access the outbound circular FIFOs. (Refer to Table 16-2.) The Outbound Queue Port, when read by an external PCI Express agent, returns the Outbound Post Queue FIFO MFA. The External PCI Express agent places free message frames into the Outbound Free List FIFO by writing the free MFA into the Outbound Queue Port location.

Memory for the circular FIFOs must be allocated in Local (IOP) memory. The queue Base address is stored in the *Queue Base Address* field (LCS_QBAR[31:20]). Each FIFO entry is a 32-bit data value. Each Read and Write of the queue must be a single 32-bit access.

Circular FIFOs range in size from 4-KB to 64-KB entries. The four FIFOs must be the same size and contiguous. Therefore, the total amount of Local memory needed for circular FIFOs ranges from 64 KB to 1 MB. The FIFO size is specified in the *Circular Queue Size* field (LCS_MQCR[5:1]).

The starting address of each FIFO is based on the queue Base address and FIFO size, as defined in Table 16-1.

Table 16-1.   Queue Starting Address

FIFO	Starting Address
Inbound Free List	**LCS_QBAR**
Inbound Post List	**LCS_QBAR** + (1 * FIFO Size)
Outbound Post List	**LCS_QBAR** + (2 * FIFO Size)
Outbound Free List	**LCS_QBAR** + (3 * FIFO Size)

16.2.3   I₂O Pointer Management

The FIFOs always reside in shared Local (IOP) memory and are allocated and initialized by the IOP. Before setting the *Queue Enable* bit (LCS_MQCR[15]), the Local processor must initialize the following registers, with the initial offset according to the configured FIFO size:

- **Inbound Post** and **Free Head Pointer** (LCS_IPHPR and LCS_IFHPR, respectively)
- **Inbound Post** and **Free Tail Pointer** (LCS_IPTPR and LCS_IFTPR, respectively)
- **Outbound Post** and **Free Head Pointer** (LCS_OPHPR and LCS_OFHPR, respectively)
- **Outbound Post** and **Free Tail Pointer** (LCS_OPTPR and LCS_OFTPR, respectively)

The PEX 8311 automatically adds the queue Base address to the offset in each **Head** and **Tail Pointer** register. The software can then enable I₂O. After initialization, ensure that the Local software does *not* write to the pointers managed by the PEX 8311 hardware.

Empty flags are set when the queues are disabled (**LCS_MQCR**[0]=0), or the Head and Tail Pointers are equal. This occurs independently of how the Head and Tail Pointers are set.

An empty flag is cleared, signifying not empty, only when the queues are enabled (**LCS_MQCR**[0]=1) and the pointers become not equal.

When an empty flag is cleared and the queues are enabled, the empty flag is set only when the Tail Pointer is incremented and the Head and Tail Pointers become equal.

Full flags are always cleared when the queues are disabled or the Head and Tail Pointers are not equal.

A full flag is set when the queues are enabled, the Head Pointer is incremented, and the Head and Tail Pointers become equal.

Each circular FIFO has a Head Pointer and a Tail Pointer, which are offsets from the queue Base address. (Refer to Table 16-2.) Writes to a FIFO occur at the head of the FIFO and reads occur from the tail. Head and Tail Pointers are incremented by the Local processor or PEX 8311 hardware. The unit that writes to the FIFO also maintains the pointer. Pointers are incremented after a FIFO access. Both pointers wrap around to the first address of the circular FIFO when they reach the FIFO size, allowing the Head and Tail Pointers to continuously "chase" one another in the circular FIFO. The PEX 8311 automatically wraps the pointers that it maintains. The IOP software must wrap the pointers that it maintains. When they are equal, the FIFO is empty. To prevent overflow conditions, I₂O specifies that the number of message frames allocated are to be less than or equal to the number of entries in a FIFO. (Refer to Figure 16-3.)

Each inbound MFA is specified by I₂O as the offset from the start of shared Local (IOP) memory to the start of the message frame. Each outbound MFA is specified as the offset from System memory location 0000_0000h to the start of the message frame in shared System memory. Because the MFA is an actual address, the message frames need not be contiguous. The IOP allocates and initializes inbound message frames in shared IOP memory, using any suitable memory-allocation technique. The System allocates and initializes outbound message frames in shared System memory using any suitable memory allocation technique. Message frames are a minimum of 64 bytes in length.

I₂O uses a "push" (write-preferred) memory model. That means the IOP writes messages and data to the shared System memory, and the System writes messages and data to shared IOP memory. Ensure that software makes use of Burst and DMA transfers wherever possible to guarantee efficient use of the PCI Express interface for message passing. (Refer to the *I₂O r1.5* for further details about message passing implementation.)

Figure 16-3. Circular FIFO Operation
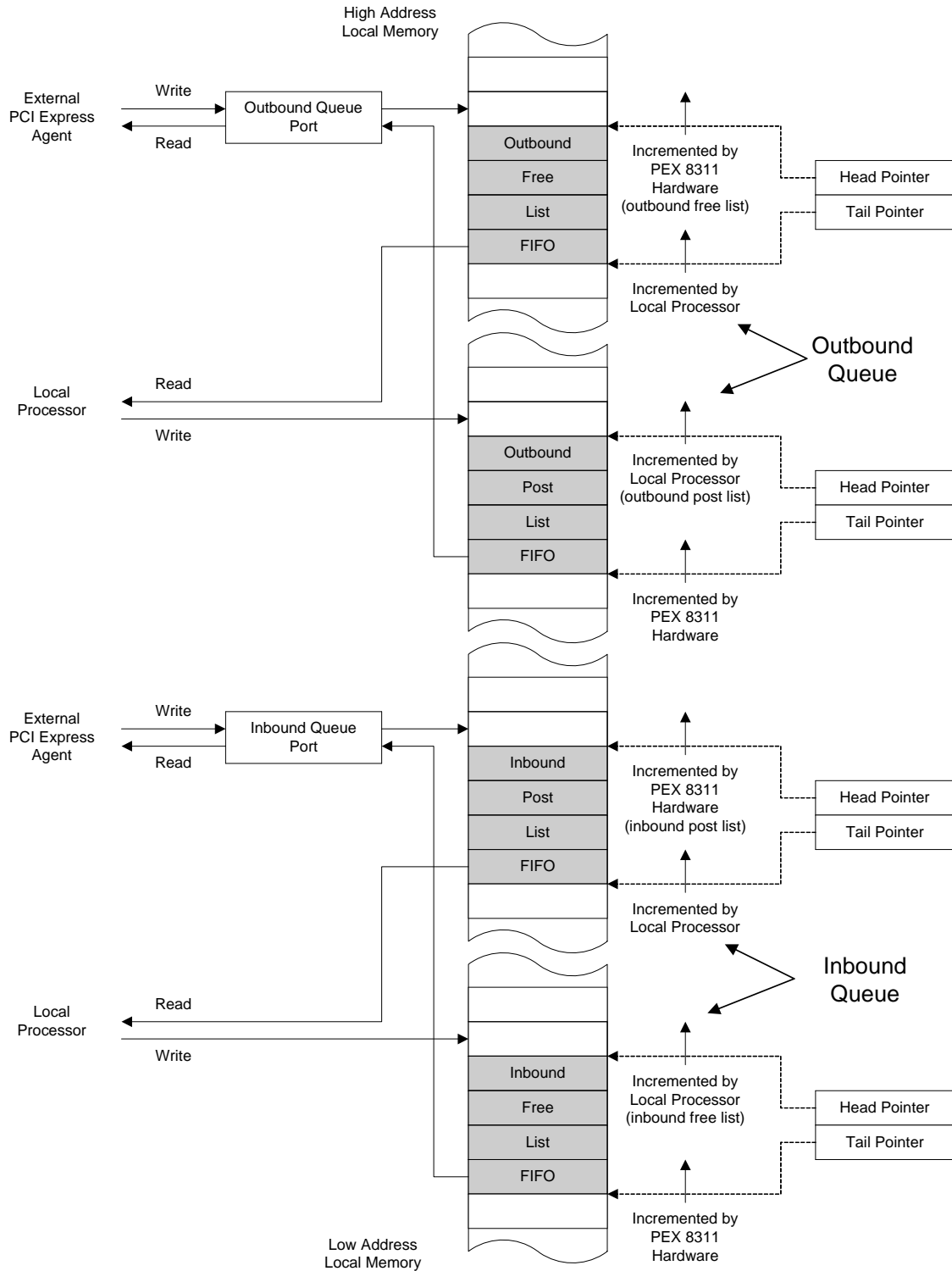
16.2.4   Inbound Free List FIFO

The Local processor allocates inbound message frames in its shared memory and can place the address of a free (available) message frame into the Inbound Free List FIFO by writing its MFA into the FIFO location pointed to by the **Queue Base Address** register (LCS_QBAR) + **Inbound Free Head Pointer** register (LCS_IFHPR). The Local processor must then increment the **LCS_IFHPR** register.

A PCI Express Root Complex or other PCI Express IOP can obtain the MFA of a free message frame by reading the Inbound Queue Port Address (40h). When the FIFO is empty (no free inbound message frames are currently available, Head and Tail Pointers are equal), the PEX 8311 returns 1 (FFFF_FFFFh). When the FIFO is not empty (Head and Tail Pointers are not equal), the PEX 8311 reads the MFA pointed to by the **Queue Base Address** register (**LCS_QBAR**) + **Inbound Free Tail Pointer** register (LCS_IFTPR), returns its value, and increments the **LCS_IFTPR** register. When the Inbound Free queue is not empty, and the *Inbound Free Queue Prefetch Enable* bit is set (LCS_QSR[3]=1), the next entry in the FIFO is read from the Local Bus into a prefetch register. The prefetch register then provides the data for the next PCI Express Read request from this queue, thereby reducing the number of potential wait states gathering the data from the Local Bus. (Refer to Figure 16-3.)

16.2.5   Inbound Post Queue FIFO

A PCI Express Root Complex or other PCI Express IOP can write a message into an available message frame in the shared Local (IOP) memory. It can then post that message by writing the MFA to the Inbound queue Port address (40h). When the port is written, the PEX 8311 writes the MFA to the Inbound Post Queue FIFO location pointed to by the **Queue Base Address** register (LCS_QBAR) + FIFO Size + **Inbound Post Head Pointer** register (LCS_IPHPR). After the PEX 8311 writes the MFA to the Inbound Post Queue FIFO, it increments the **LCS_IPHPR** register.

The **Inbound Post Tail Pointer** register (LCS_IPTPR) points to the Inbound Post Queue FIFO location that holds the MFA of the oldest posted message. The Local processor maintains the Tail Pointer. After a Local processor reads the oldest MFA, it can remove the MFA from the Inbound Post Queue FIFO by incrementing the **LCS_IPTPR** register.

The PEX 8311 asserts a Local interrupt when the Inbound Post Queue FIFO is not empty. The *Inbound Post Queue Interrupt Not Empty* bit (LCS_QSR[5]) indicates the interrupt status. The interrupt clears when the Inbound Post Queue FIFO is empty. The *Inbound Post Queue Interrupt Not Empty Mask* bit can mask the interrupt (**LCS_QSR**[4]=1).

From the time a PCI Express Write transaction is received, Direct Slave accesses to the PEX 8311 are retried internally, until the data is written in Local memory and the **Inbound Post Head Pointer** register (**LCS_IPHPR**) is incremented.

16.2.6 Outbound Post Queue FIFO

A Local Master (IOP) can write a message into an available message frame in shared Host memory. It can then post that message by writing the MFA to the Outbound Post Queue FIFO location pointed to by the **Queue Base Address** register (LCS_QBAR) + **Outbound Post Head Pointer** register (LCS_OPHPR) + (2 * FIFO Size). The Local processor then increments the **LCS_OPHPR** register.

A PCI master can obtain the MFA of the oldest posted message by reading the Outbound queue Port address (44h). When the FIFO is empty (no more outbound messages are posted, Head and Tail Pointers are equal), the PEX 8311 returns -1 (FFFF_FFFFh). When the Outbound Post Queue FIFO is not empty (Head and Tail Pointers are not equal), the PEX 8311 reads the MFA pointed to by the **Queue Base Address** register (**LCS_QBAR**) + (2 * FIFO Size) + **Outbound Post Tail Pointer** register (LCS_OPTPR), returns its value, and increments the **LCS_OPTPR** register.

The PEX 8311 generates a PCI Express message interrupt, when enabled when the **LCS_OPHPR** register is not equal to the **LCS_OPTPR** register. The *Outbound Post Queue Interrupt* bit (LCS_OPQIS[3]) indicates the interrupt status. When the pointers become equal, both the interrupt and **LCS_OPQIS**[3] are automatically cleared. Pointers become equal when a PCI Express Root Complex or other PCI Express IOP reads sufficient FIFO entries to empty the FIFO. The **Outbound Post Queue Interrupt Mask** register can mask the interrupt (LCS_OPQIM[3]=1).

16.2.7 Outbound Post Queue

To reduce read latency, prefetching from the tail of the queue occurs when the queue is not empty and the Tail Pointer is incremented (queue has been read from), or when the queue is empty and the Head Pointer is incremented (queue has been written to). When the PCI Express Root Complex reads the Outbound Post queue, the data is immediately available.

16.2.8 Inbound Free Queue

To reduce read latency, prefetching from the tail of the queue occurs when the queue is not empty and the Tail Pointer is incremented (queue has been read from), or when the queue is empty and the Head Pointer is incremented (queue has been written to). When the PCI Express Root Complex reads the Inbound Free queue, the data is immediately available.

16.2.9   Outbound Free List FIFO

The PCI Express Root Complex or other PCI Express IOP allocates outbound message frames in its shared memory. The PCI Express Root Complex can place the address of a free (available) message frame into the Outbound Free List FIFO by writing an MFA to the Outbound queue Port address (44h). When the port is written, the PEX 8311 writes the MFA to the Outbound Free List FIFO location pointed to by the **Queue Base Address** register (LCS_QBAR) + (3 * FIFO Size) + **Outbound Free Head Pointer** register (LCS_OFHPR). After the PEX 8311 writes the MFA to the Outbound Free List FIFO, it increments the **LCS_OFHPR** register.

When the IOP needs a free outbound message frame, it must first check whether any free frames are available. When the Outbound Free List FIFO is empty (Outbound Free Head and Tail Pointers are equal), the IOP must wait for the PCI Express Root Complex to place at least one additional outbound free MFA in the Outbound Free List FIFO. When the Outbound Free List FIFO is not empty (Head and Tail Pointers are not equal), the IOP can obtain the MFA of the oldest free outbound message frame by reading the location pointed to by the **Queue Base Address** register (**LCS_QBAR**) + (3 * FIFO Size) + **Outbound Free Tail Pointer** register (LCS_OFTPR). After the IOP reads the MFA, it must increment the **LCS_OFTPR** register. To prevent overflow conditions, I$_2$O specifies the number of message frames allocated are to be less than or equal to the number of entries in a FIFO. The PEX 8311 also checks for Outbound Free List FIFO overflows. When the Head Pointer is incremented and becomes equal to the Tail Pointer, the Outbound Free List FIFO is full, and the PEX 8311 asserts a Local Bus System Error LSERR# (C or J mode) or LINTo# (M mode) interrupt. The interrupt is recorded in the *Outbound Free Queue Overflow Interrupt Full* bit (LCS_QSR[7]).

From the time the PCI Express Write transaction is received until the data is written into Local memory and the **LCS_OFHPR** register is incremented, any Direct Slave access to the PEX 8311 is retried internally. The Direct Slave Write data is accumulated in the PCI Express queue.

16.2.10   I$_2$O Enable Sequence

To enable I$_2$O, the Local processor performs the following:

- Maps one of the PCI Express Address spaces to Direct Slave Space 1
- Initializes Direct Slave Space 1 address and range (minimum 1,024 bytes)
- Initializes all FIFOs and Message Frame memory
- Sets the **LCS** *PCI Base Class Code* bits (LCS_PCICCR[23:16]) as an I$_2$O device with programming interface 01h
- Sets the *I$_2$O Decode Enable* bit (**LCS_QSR**[0]=1)
- Sets the *Local Init Status* bit to "done" (LCS_LMISC1[2]=1)
- Disables all Direct Slave prefetch mechanisms (LCS_LBRD0[8] for Space 0, LCS_LBRD1[9] for Space 1, and/or **LCS_LBRD0**[9] for Expansion ROM)

Note: *The Local Bus serial EEPROM must **not** set the Local Init Status bit for the PEX 8311 to issue internal Retrys to all PCI Express Configuration Space accesses on the Local Bus until the Local Init Status bit is set to "done" by the Local processor.*

Enabling I₂O Decode causes resources to remap, for use in I₂O mode (LCS_QSR[0]=1). When set, all **Memory-Mapped Configuration** registers and Local Address Space 1 share the **LCS_PCIBAR0** register. The PCI Express Type 1 (Type 1 is internally converted to Type 0) Configuration accesses to **LCS_PCIBAR0** offset 00h to FFh result in accesses to the **LCS Local**, **Runtime**, **DMA**, and **Messaging Queue** registers.

Accesses above **LCS_PCIBAR0** offset FFh result in Local Space accesses, beginning at offset 100h from the internal *Remap PCI Express Address to Local Address Space 1* into the *Remap LCS_PCIBAR3 Base Address to Local Address Space 1 Base Address* bits (LCS_LAS1BA[31:4]). Therefore, space located at offset 00h to FFh from **LCS_LAS1BA** is not addressable from the PCI Express interface using **LCS_PCIBAR0**.

Note: *Because PCI Express accesses to **LCS_PCIBAR0** offset 00h to FFh result in internal Configuration accesses, the Inbound Free MFA must be greater than FFh.*

Table 16-2.   Circular FIFO Summary

FIFO Name	PCI Port	Generate PCI Express Message Interrupt	Generate Local Interrupt	Head Pointer Maintained By	Tail Pointer Maintained By
Inbound Free List FIFO	Inbound Queue Port (PCI Express Root Complex Read Request)	No	No	Local processor	PEX 8311 hardware
Inbound Post List FIFO	Inbound Queue Port (PCI Express Root Complex Write Request)	No	Yes, when Port is written	PEX 8311 hardware	Local processor
Outbound Post List FIFO	Outbound Queue Port (PCI Express Root Complex Read Request)	Yes, when FIFO is not empty	No	Local processor	PEX 8311 hardware
Outbound Free List FIFO	Outbound Queue Port (PCI Express Root Complex Write Request)	No	**C and J Modes –** Yes (LSERR#), when FIFO is full **M Mode –** Yes (LINTo#), when FIFO is full	PEX 8311 hardware	Local processor

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![PLX Technology logo] **Chapter 17   Vital Product Data (VPD)**

17.1   Overview

VPD provides optional bits that are used to identify and track a device. These bits are set to make each device unique. In the original *PCI Local Bus Specification*, Device ID, Vendor ID, Revision ID, Class Code ID, and Subsystem Vendor ID were required in the Configuration Space Header and for basic device identification and configuration. Although this information allows a device to be configured, it is not sufficient to allow each device unique identification. The VPD optional information capability enables new support tools and reduces the cost of computer ownership.

In the *PCI r2.2*, the VPD function defines a storage device and access method for VPD, as well as defining the Read-Only and Read/Write bits. The PEX 8311 stores VPD in a **LCS** serial EEPROM. Access to VPD is through the New Capabilities function of the **LCS PCI** Configuration registers.

17.2   Local Configuration Space VPD Capabilities Registers

The following sections describe the **LCS VPD Capabilities** registers. As defined in Table 17-1, they include the **VPD Control** and **Data** registers. PCI Express accesses to the **VPD** registers must be Type 1 accesses (which are internally converted to Type 0) to **LCS PCI Extended Capability** registers. Local Bus accesses to the **VPD** registers are accomplished directly by way of Direct Master Memory cycles, with CCS# asserted.

17.2.1   VPD Control Register

The **VPD Control** register is 32 bits wide and is documented as three smaller registers – **VPD ID**, **Next_Cap Pointer**, and **VPD Address** (refer to Table 17-1 and Register 20-34 through Register 20-36):

- **VPD ID** (**LCS_PVPDID**[7:0]; PCI:4Ch, LOC:18Ch). PCI-SIG-assigned value of 03h. The VPD ID is hardwired.

- **Next_Cap Pointer** (**LCS_PVPD_NEXT**[7:0]; PCI:4Dh, LOC:18Dh).Point to the next New Capability structure. The PEX 8311 defaults to 0h. Because VPD is the last feature of the New Capability structure, this field is cleared to 0h. Bits [1:0] are *reserved* by *PCI r2.2*, and are cleared to 00b.

- **VPD Address** (**LCS_PVPDAD**[14:0]; PCI:4Eh, LOC:18Eh). Specify the VPD byte address to access. All accesses are 32 bits wide. For VPD writes, the byte address must be Dword-aligned (**LCS_PVPDAD**[1:0]=00b). For VPD reads, the byte address must be word-aligned (**LCS_PVPDAD**[0]=0). Bits [14:9] are ignored.

  (**LCS_PVPDAD**[15]; PCI:4Eh, LOC:18Eh). The *F* bit controls the direction of the next VPD cycle and indicates when the VPD cycle is complete. For Write cycles, the 4 bytes of data are first written into the *VPD Data* bits, after which the VPD Address is written at the same time the *F* bit is set to 1. The *F* bit is cleared when the serial EEPROM Data transfer completes. For Read cycles, the VPD Address is written at the same time the *F* bit is cleared to 0. The *F* bit is set when 4 bytes of data are read from the serial EEPROM.

17.2.2   VPD Data Register

The **VPD Data** register is 32 bits wide and is documented as a single 32-bit register. (Refer to Table 17-1.)

VPD Data (**LCS_PVPDATA**[31:0]; PCI:50h, LOC:190h). The **LCS_PVPDATA** register is used to read/write data to/from the VPD serial EEPROM. It is not, however, a pure read/write register. The data read from this register is the data read during the last VPD Read operation. The data written to this register is the data written to the serial EEPROM during a VPD Write operation. The register's words are stored in the serial EEPROM, in Big Endian order, beginning at the serial EEPROM word address specified by the *VPD Address* bits (**LCS_PVPDAD**[8:1]). Four bytes are always transferred between the register and serial EEPROM.

Table 17-1.   VPD Data Register Documentation

Register Bit Range	31	30 16	15 8	7 0
VPD Control Register	F (**LCS_PVP DAD**[15])	VPD Address (**LCS_PVPDAD**[14:0])	Next_Cap Pointer (0h) (**LCS_PVPD_NEXT**[7:0])	VPD ID (03h) (**LCS_PVPDID**[7:0])
VPD Data Register	VPD Data (**LCS_PVPDATA**[31:0])			

17.3   VPD Serial EEPROM Partitioning

To support VPD, the serial EEPROM is partitioned into Read-Only and Read/Write portions. The boundary between Read-Only and Read/Write is set with the *Serial EEPROM Location Starting at Dword Boundary for VPD Accesses* field (**LCS_PROT_AREA**[6:0]).

17.4   Sequential Read-Only

The first 1,536 bits, 192 bytes of the serial EEPROM contain Read-Only information. After power-on, the Read-Only portion of the serial EEPROM is loaded into the PEX 8311, using the serial EEPROM's Sequential Read protocol. Sequential words are read by holding EECS asserted, following the issuance of a serial EEPROM Read command.

17.5   **Random Read and Write**

The PEX 8311 can read and write the Read/Write portion of serial EEPROM, using the VPD function. It can also read the Read-Only portion of the serial EEPROM. The writable portion of the serial EEPROM starts at the Dword specified by **LCS_PROT_AREA**[6:0] and continues to the top of the serial EEPROM. The *Serial EEPROM Location Starting at Dword Boundary for VPD Accesses* field (**LCS_PROT_AREA**[6:0]) designate this portion. This register is loaded at power-on and can be written with the necessary value, starting at Location 0. This provides the capability of writing the entire serial EEPROM. Writes to serial EEPROM are comprised of the following three commands:

- Write Enable
- Write Data, followed by Write Data (two 16-bit writes)
- Write Disable

This is performed to ensure against accidental writes to the serial EEPROM. Random cycles allow VPD information to be written and read at any time.

To perform a VPD write to the serial EEPROM, the following steps are necessary:

1. Disable EEDO input (**LCS_CNTRL**[31]=0, default).
2. Change the write-protected serial EEPROM address in **LCS_PROT_AREA**[6:0] to the necessary Dword location. Value of 0h makes the entire serial EEPROM writable.
3. Write necessary data into the **LCS_PVPDATA** register.
4. Write the serial EEPROM destination address in the **LCS_PVPDAD** register, and the *F* bit to 1 (**LCS_PVPDAD**[15]=1). **LCS_PVPDAD**[1:0] must be 00b (address is Dword-aligned).
5. Poll the *F* bit until it changes to 0 (**LCS_PVPDAD**[15]=0), to ensure that the write completes.

To perform a VPD read from serial EEPROM, the following steps are necessary:

1. Disable EEDO input (**LCS_CNTRL**[31]=0, default).
2. Write the serial EEPROM destination address in the **LCS_PVPDAD** register, and 0 to the *F* bit (**LCS_PVPDAD**[15]=0). **LCS_PVPDAD**[0] must be 0 (address is word-aligned).
3. Poll the *F* bit until it changes to 1 (**LCS_PVPDAD**[15]=1), to ensure that the Read data is available.
4. Read back the **LCS_PVPDATA** register, to obtain the requested data.

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Chapter 18   General-Purpose I/Os

18.1   Overview

The PEX 8311 supports one GPI, one GPO, and four GPIO signals.

18.2   USERi and USERo Signals

The PEX 8311 supports user input and output balls, USERi and USERo. Both are multiplexed with other signals. By default, the PEX 8311 configures these balls as USERi and USERo:

- USERi is selected when **LCS_CNTRL**[18]=1. User Input data is read from the *General-Purpose Input* bit (**LCS_CNTRL**[17]). (Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior," for USERi strapping options during reset.)

- USERo is selected when **LCS_CNTRL**[19]=1. User Output data is logged by writing to the *General-Purpose Output* bit (**LCS_CNTRL**[16]).

During a software reset, USERo is driven Low. USERo behavior is as follows:

- During a hard reset (PERST#=0), USERo is tri-stated. On the second rising edge of LCLK after PERST# is de-asserted, LRESET# is de-asserted. On the next falling edge of LCLK, USERo is driven to 0 (from tri-state). On the next rising edge of LCLK, USERo is driven to the value specified in **LCS_CNTRL**[16] (default value = 1).

- When the *Local Bus Reset* bit is set (**LCS_CNTRL**[30]=1), the LRESET# and USERo signals are asserted Low (0). When the *Local Bus Reset* bit is cleared (**LCS_CNTRL**[30]=0), USERo reverts to the value specified in **LCS_CNTRL**[16], one LCLK after the LRESET# signal is de-asserted (driven to 1).

18.3   GPIO Signals

The PEX 8311 provides four GPIO balls (GPIO[3:0]) that can be independently programmed as Inputs or Outputs at any given time. Control of these GPIO balls is located in the **PECS_GPIOCTL** and **PECS_GPIOSTAT** registers.

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Chapter 19 PCI Express Configuration Registers

19.1 Introduction

This chapter describes the PCI Express Configuration Space (**PECS**) register set. Local Configuration Space (**LCS**) registers are described in Chapter 20, "Local Configuration Space Registers."

19.2 Register Description

The **PCI-Compatible** Configuration registers are accessed by the PCI Express Root Complex (Endpoint mode) or Local host (Root Complex mode), using the PCI Configuration Address space. All **PECS** registers can be accessed from the PCI Express interface or Local Bus, using memory Reads or Writes to the 64-KB Memory space defined by the **PECS_PCIBASE0** register. Additionally, the **PECS** register default values can be overwritten by the PCI Express interface serial EEPROM.

In Root Complex mode, a Local Bus Master cannot access the **PCI Express Extended Capability** registers by way of PCI Configuration transactions. To access the **PCI Express Extended Capability** registers, use the method detailed in Section 10.7.1, "Memory-Mapped Indirect – Root Complex Mode Only."

When the Configuration registers are accessed using Memory transactions to the **PECS_PCIBASE0** register, the address mapping defined in Table 19-1 is used.

Many **PECS** registers can be loaded from the PCI Express Configuration Space serial EEPROM, as indicated in Table 19-5 to Table 19-8. Details of the serial EEPROM interface and contents are provided in Section 4.2, "PCI Express Configuration Space Serial EEPROM Interface (SPI-Compatible Interface)."

Each register is 32 bits wide, and accessed one byte, word, or DWORD at a time. These registers use Little Endian Byte Ordering, which is consistent with the *PCI r3.0*. The least significant byte in a DWORD is accessed at Address 0. The least significant bit in a DWORD is 0, and the most significant bit is 31.

After the PEX 8311 is powered up or reset, the registers are set to their default values. Writes to unused registers are ignored, and reads from unused registers return a value of 0.

Table 19-1. PECS_PCIBASE0 Address Mapping

Address Offset	Register Space
0000h – 0FFFh	PCI-Compatible Configuration registers
1000h – 1FFFh	Main Configuration registers
2000h – 2FFFh	Memory-Mapped indirect access to downstream PCI Express Endpoint registers (Root Complex mode only)
8000h – 9FFFh	8-KB internal shared memory

19.2.1 Indexed Addressing

In addition to Memory-Mapped accesses, the PEX 8311 **Main Configuration** registers are accessed using the **PECS_MAININDEX** and **PECS_MAINDATA** registers. This method allows **Main Configuration** registers to be accessed using Configuration transactions, rather than Memory transactions. First, the **Main Configuration** register offset is written to the **PECS_MAININDEX** register (Offset 84h). Then, the **Main Configuration** register is written or read by accessing the **PECS_MAINDATA** register (Offset 88h).

19.3 PCI Express Configuration Space Configuration Access Types

Table 19-2 defines the Configuration access types referenced by the registers in this chapter.

Table 19-2.   Configuration Access Types

Access Type	Description
CFG	Initiated by PCI Configuration transactions (Type 0 accesses) on the primary interface.
MM	Initiated by PCI Express Memory transactions on either the primary or secondary interface, using the Address range defined by the **PECS_PCIBASE0** register.
EE	Initiated by the Serial EEPROM Controller during initialization.

Note: *The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.*

The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.

19.4   PCI Express Configuration Space Register Attributes

Table 19-3 defines the register attributes used to indicate access types provided by each register bit.

Table 19-3.   Access Provided by Register Bits

Register Attribute	Description
HwInit	**Hardware Initialized** Hardware initialized register or register bit. The register bits are initialized by a PEX 8311 hardware initialization mechanism or PEX 8311 Serial EEPROM register initialization feature. Register bits are Read-Only after initialization and can only be reset with "Fundamental Reset."
RO	**Read-Only Register** Register bits are Read-Only and cannot be altered by software. Register bits are initialized by a PEX 8311 hardware initialization mechanism or PEX 8311 Serial EEPROM register initialization feature.
RsvdP	***Reserved* and Preserved** *Reserved* for future RW implementations. Registers are Read-Only and must return 0 when read. Software must preserve value read for writes to bits.
RsvdZ	***Reserved* and Zero** *Reserved* for future RW1C implementations. Registers are Read-Only and must return 0 when read. Software must use 0 for writes to bits.
RW	**Read-Write Register** Register bits are Read-Write and are set or cleared by software to the needed state.
RW1C	**Read-Only Status, Write 1 to Clear Status Register** Register bits indicate status when read; a set bit indicating a status event is cleared by writing 1. Writing 0 to RW1C bits has no effect.
WO	**Write-Only** Used to indicate that a register is written by the Serial EEPROM Controller.

19.5   PCI Express Configuration Space Register Summary

Table 19-4.   Register Summary

Register Group	PCI Space	Address Range
PCI-Compatible Type 1 Configuration Registers	PCI Express Configuration (Endpoint mode); PCI Configuration (Root Complex mode)	000h – 0FFh
	Memory-Mapped, BAR 0	000h – 0FFh
PCI Express Extended Capability Registers	PCI Express Configuration (Endpoint mode)	100h – 1FFh
	Memory-Mapped, BAR 0	100h – 1FFh
Main Control Registers	Memory-Mapped, BAR 0; Indexed, by way of the **PECS_MAININDEX/PECS_MAINDATA** registers (Offset 84h and Offset 88h, respectively)	1000h – 10FFh
PCI Express Configuration Registers using Enhanced Configuration Access	Memory-Mapped, BAR 0	2000h – 2FFFh
8-KB General-Purpose Memory	Memory-Mapped, BAR 0	8000h – 9FFFh

19.6   PCI-Compatible Type 1 Configuration Registers

This section details the **PECS** PCI-Compatible Type 1 Configuration registers. Table 19-5 defines the register map.

Table 19-5.   PCI-Compatible Type 1 Configuration Register Map

PCI Configuration Register Address	31 24	23 16	15 8	7 0
00h	PCI Device ID		PCI Vendor ID	
04h	PCI Status (Endpoint Mode) PCI Status (Root Complex Mode)		PCI Command (Endpoint Mode) PCI Command (Root Complex Mode)	
08h	PCI Class Code			PCI Device Revision ID
0Ch	PCI Built-In Self-Test (*Not Supported*)	PCI Header Type	Internal PCI Bus Latency Timer	PCI Cache Line Size
10h	PCI Express Base Address 0			
14h	PCI Express Base Address 1			
18h	Secondary Latency Timer (Endpoint Mode Only)	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number
1Ch	Secondary Status (Endpoint Mode) Secondary Status (Root Complex Mode)		I/O Limit	I/O Base
20h	Memory Limit		Memory Base	
24h	Prefetchable Memory Limit		Prefetchable Memory Base	
28h	Prefetchable Memory Base Upper 32 Bits			
2Ch	Prefetchable Memory Limit Upper 32 Bits			
30h	I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits	
34h	*Reserved*			PCI Capabilities Pointer
38h	PCI Express Base Address for Expansion ROM (*Not Supported*)			
3Ch	Bridge Control (Endpoint Mode) Bridge Control (Root Complex Mode)		Internal PCI Wire Interrupt	Internal PCI Interrupt Line

Register 19-1. Offset 00h PECS_PCIVENDID PCI Vendor ID

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Vendor ID** Identifies the device manufacturer. Hardwired to the PLX PCI-SIG-assigned Vendor ID, 10B5h.	RO	RW	WO	10B5h

Register 19-2. Offset 02h PECS_PCIDEVID PCI Device ID

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Device ID** Identifies the particular device. Defaults to 8111h when the serial EEPROM is blank, or no serial EEPROM is present.	RO	RW	WO	8111h

Register 19-3. Offset 04h PECS_PCICMD PCI Command (Endpoint Mode)

Bit(s)	Description	CFG	MM	EE	Default
0	**I/O Access Enable** 1 = Enables PEX 8311 to respond to I/O Space accesses on the PCI Express interface These accesses must be directed to a target on the Local Bus, because the PEX 8311 does not have internal I/O-Mapped resources.	RW	RW	WO	0
1	**Memory Space Enable** 0 = PEX 8311 responds to Memory requests on the PCI Express interface with an Unsupported Request completion. 1 = Enables PEX 8311 to respond to Memory Space accesses on the PCI Express interface. These accesses are directed to a target on the Local Bus, or to internal Memory-Mapped registers.	RW	RW	WO	0
2	**Bus Master Enable** 0 = PEX 8311 must disable response as a target to Memory or I/O transactions on the Local Bus interface (they cannot be forwarded to the PCI Express interface). 1 = Enables PEX 8311 to issue Memory and I/O Read/Write requests on the PCI Express interface. Requests other than Memory or I/O requests are not controlled by this bit.	RW	RW	WO	0
3	**Special Cycle Enable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0

Register 19-3. Offset 04h PECS_PCICMD PCI Command (Endpoint Mode) (Cont.)

Bit(s)	Description	CFG	MM	EE	Default
4	**Memory Write and Invalidate** 0 = Memory Write command is used instead of the Memory Write and Invalidate command 1 = Enables the PEX 8311 internal PCI Bus master logic to use the Memory Write and Invalidate command	RW	RW	WO	0
5	**VGA Palette Snoop** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
6	**Parity Error Response Enable** Controls the response to Data Parity errors forwarded from the PCI Express interface (*such as*, a poisoned TLP). 0 = PEX 8311 must ignore (but records status, *such as* setting the **PECS_PCISTAT** register *Detected Parity Error* bit) detected Data Parity errors, and continue standard operation 1 = PEX 8311 must take its normal action when a Data Parity error is detected	RW	RW	WO	0
7	**Address Stepping Enable** The PEX 8311 performs Address Stepping for PCI Configuration cycles; therefore, this bit is read/write with an initial value of 1.	RW	RW	WO	1
8	**Internal SERR# Enable** 1 = Enables reporting of Fatal and Non-Fatal errors to the Root Complex *Note:* *Errors are reported when enabled through this bit or through the* **PECS_DEVCTL** *register PCI-Express-specific bits.*	RW	RW	WO	0
9	**Fast Back-to-Back Enable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
10	**Interrupt Disable** When set to 1: • PEX 8311 is prevented from generating INTA# interrupt messages on behalf of functions integrated into the bridge • INTA# emulation interrupts previously asserted must be de-asserted There is no effect on INTA# messages generated on behalf of INTA# inputs associated with the Local Bus interface.	RW	RW	WO	0
15:11	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-4. Offset 04h PECS_PCICMD PCI Command (Root Complex Mode)

Bit(s)	Description	CFG	MM	EE	Default
0	**I/O Access Enable** 0 = PCI Express I/O accesses to the PEX 8311 result in a Master Abort. 1 = Enables the PEX 8311 to respond to I/O Space accesses on the Local Bus interface. These accesses are directed to a target on the PCI Express interface, because the PEX 8311 does not have internal I/O-Mapped devices.	RW	RW	WO	0
1	**Memory Space Enable** 0 = PCI Express Memory accesses to the PEX 8311 result in a Master Abort. 1 = Enables the PEX 8311 to respond to Memory Space accesses on the Local Bus interface. These accesses are directed to a target on the PCI Express interface, or to internal Memory-Mapped registers.	RW	RW	WO	0
2	**Bus Master Enable** 0 = PEX 8311 must disable response as a target to Memory or I/O transactions on the PCI Express interface (they cannot be forwarded to the Local Bus interface). In this case, Memory and I/O requests are terminated with an Unsupported Request completion. 1 = Enables the PEX 8311 to perform Memory or I/O transactions on the internal PCI Bus. Configuration transactions are forwarded from the PCI Express interface and performed on the internal PCI Bus independent of this bit.	RW	RW	WO	0
3	**Special Cycle Enable** A bridge does not respond to special cycle transactions; therefore, forced to 0.	RO	RO	–	0
4	**Memory Write and Invalidate** 0 = Memory Write command is used instead of the Memory Write and Invalidate command 1 = Enables the PEX 8311 internal PCI Bus master logic to use the Memory Write and Invalidate command	RW	RW	WO	0
5	**VGA Palette Snoop** 1 = I/O Writes in the first 64 KB of the I/O Address space with Address bits [9:0] equal to 3C6h, 3C8h, and 3C9h (inclusive of ISA aliases – AD[15:10] are not decoded and can be any value) must be positively decoded on the PCI interface and forwarded to the PCI Express interface	RW	RW	WO	0
6	**Parity Error Response Enable** 1 = Enables PCI parity checking	RW	RW	WO	0
7	*Reserved*	RsvdP	RsvdP	–	0
8	**Internal SERR# Enable** 1 = Enables the internal SERR# signal to assert	RW	RW	WO	0
9	**Fast Back-to-Back Enable** *Not supported* The PEX 8311 PCI master interface does not perform Fast Back-to-Back transactions; therefore, forced to 0.	RO	RO	–	0
10	**Interrupt Disable** 1 = PEX 8311 is prevented from asserting INTA# signals on behalf of functions integrated into the bridge There is no effect on INTA# signals asserted on behalf of INTA# messages associated with the PCI Express interface.	RW	RW	WO	0
15:11	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-5. Offset 06h PECS_PCISTAT PCI Status (Endpoint Mode)

Bit(s)	Description	CFG	MM	EE	Default
2:0	*Reserved*	RsvdZ	RsvdZ	–	000b
3	**Interrupt Status** 1 = Indicates that an INTA# interrupt message is pending on behalf of functions integrated into the bridge. Does not reflect the status of INTA# inputs associated with the Local Bus interface.	RO	RO	–	0
4	**Capabilities List** 1 = Indicates whether the **New Capabilities Pointer** at offset 34h is valid. Because PCI Express devices are required to implement the PCI Express Capability structure, this bit is hardwired to 1.	RO	RO	–	1
5	**66 MHz Capable (Internal Clock Frequency)** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
6	*Reserved*	RsvdZ	RsvdZ	–	0
7	**Fast Back-to-Back Transactions Capable** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	0
8	**Master Data Parity Error** Used to report Data Parity error detection by the bridge. Set to 1 when the **PECS_PCICMD** register *Parity Error Response Enable* bit is set and either of the following two conditions occur: • Bridge receives a completion marked *poisoned* on PCI Express interface • Bridge poisons a Write request or Read Completion on PCI Express interface Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**DEVSEL Timing** Does not apply to PCI Express; therefore, forced to 0.	RO	RO	–	00b
11	**Signaled Target Abort** Set when the bridge completes a request as a transaction target on the PCI Express interface using Completer Abort completion status. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Received Target Abort** Set when the bridge receives a completion with Completer Abort completion status on the PCI Express interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Received Master Abort** Set when the bridge receives a completion with Unsupported Request completion status on the PCI Express interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Signaled System Error** Set when the bridge transmits an ERR_FATAL or ERR_NONFATAL message to the Root Complex, and the **PECS_PCICMD** register *Internal SERR# Enable* bit is set. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Detected Parity Error** Set by the bridge when it receives a poisoned TLP on the PCI Express interface, regardless of the **PECS_PCICMD** register *Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 19-6. Offset 06h PECS_PCISTAT PCI Status (Root Complex Mode)

Bit(s)	Description	CFG	MM	EE	Default
2:0	*Reserved*	RsvdZ	RsvdZ	–	000b
3	**Interrupt Status** Reflects the state of the PEX 8311 internal PCI interrupt status. INTA# is asserted when this bit is High, the **PECS_PCICMD** register *Interrupt Disable* bit is Low, and the Power State is D0.	RO	RO	–	0
4	**Capabilities List** Indicates whether the **New Capabilities Pointer** at offset 34h is valid.	RO	RO	–	1
5	**66 MHz Capable (Internal Clock Frequency)** Optional bit that indicates whether the PEX 8311 is capable of running at 66 MHz. 0 = Indicates 33 MHz 1 = Indicates that the PEX 8311 is 66-MHz capable	RO	RW	WO	1
6	*Reserved*	RsvdZ	RsvdZ	–	0
7	**Fast Back-to-Back Transactions Capable** *Not supported* The PEX 8311 does not accept Fast Back-to-Back transactions; therefore, forced to 0.	RO	RO	–	0
8	**Master Data Parity Error** Indicates that a Data Parity error occurred when the PEX 8311 was the internal PCI Bus Master. The **PECS_PCICMD** register *Parity Error Response Enable* bit must be set for this bit to set. Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**DEVSEL Timing** Determines how quickly the PEX 8311 PCI Express bridge responds to a Direct Master transaction on its internal PCI Bus. A value of 01b indicates a medium response.	RO	RO	–	01b
11	**Signaled Target Abort** Set when the PEX 8311 is acting as an internal PCI Bus Target, and terminates its transaction with a Target Abort. A Target Abort occurs when a target detects a Fatal error and is unable to complete the transaction. This never occurs in the PEX 8311; therefore, 0 is always returned.	RsvdZ	RsvdZ	–	0
12	**Received Target Abort** Set when the PEX 8311 is acting as an internal PCI Bus Master, with its transaction terminated with a Target Abort. A Target Abort occurs when a target detects a Fatal error and is unable to complete the transaction. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Received Master Abort** Set when the PEX 8311 is acting as an internal PCI Bus Master, with its transaction terminated with a Master Abort. A Master Abort occurs when there is an invalid address on the internal PCI Bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Signaled System Error** Set when the PEX 8311 asserts the internal SERR# signal. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Detected Parity Error** Set when the PEX 8311 detects a Parity error on incoming addresses or data from the internal PCI Bus, regardless of the **PECS_PCICMD** register *Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 19-7. Offset 08h PECS_PCIDEVREV PCI Device Revision ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Express Block Device Revision ID** Identifies the PCI Express block of PEX 8311 silicon revision. Bits [3:0] represent the minor revision number and bits [7:4] represent the major revision number.	RO	RO	–	21h

Register 19-8. Offset 09h PECS_PCICLASS PCI Class Code

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Programming Interface**	RO	RW	WO	00h
15:8	**Subclass Code**	RO	RW	WO	04h
23:16	**Base Class Code**	RO	RW	WO	06h

Register 19-9. Offset 0Ch PECS_PCICACHESIZE PCI Cache Line Size

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Cache Line Size** Specifies the System Cache Line Size (in units of DWords). The value in this register is used by PCI master devices to determine whether to use Read, Memory Read Line, Memory Read Multiple or Memory Write Invalidate commands to access memory. The PEX 8311 supports Cache Line Sizes of only 2, 4, 8, 16, or 32 DWORDs. Writes of values other than these result in a Cache Line Size of 0; however, the value written is nonetheless returned when this register is read.	RW	RW	WO	0h

Register 19-10. Offset 0Dh PECS_PCILATENCY Internal PCI Bus Latency Timer

Bit(s)	Description	CFG	MM	EE	Default
Note:	*In the **CFG**, **MM**, and **EE** columns, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*				
7:0	**Internal PCI Bus Latency Timer** Also referred to as the Primary Latency Timer for Type 1 Configuration Space Header devices. The Primary/Master Latency Timer does not apply to PCI Express (Endpoint mode). In Root Complex mode, specifies (in units of internal clocks) the value of the Latency Timer during Bus Master bursts. When the Latency Timer expires, the PEX 8311 must terminate its tenure on the bus.	RO (E) RW (RC)	RO (E) RW (RC)	– (E) WO (RC)	0h

Register 19-11. Offset 0Eh PECS_PCIHEADER PCI Header Type

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Header Type** Specifies the format of the second part of the pre-defined configuration header starting at offset 10h. For PCI bridges, this field is forced to 1.	RO	RO	–	1h

Register 19-12. Offset 0Fh PECS_PCIBIST PCI Built-In Self-Test

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Built-In Self-Test** *Not supported* Always returns a value of 0h.	RO	RO	–	0h

Register 19-13. Offset 10h PECS_PCIBASE0 PCI Express Base Address 0

Bit(s)	Description	CFG	MM	EE	Default
0	**Space Type** When Low, this space is accessed as memory. When High, this space is accessed as I/O. *Note: Hardwired to 0.*	RO	RO	–	0
2:1	**Address Type** Indicates the type of addressing for this space. 00b = Locate anywhere in 32-bit Address space (default) 01b = Locate below 1 MB 10b = Locate anywhere in 64-bit Address space 11b = *Reserved*	RO	RW	WO	10b
3	**Prefetch Enable** 1 = Indicates that prefetching has no side effects on reads	RO	RW	WO	1
15:4	**Base Address** This section of the Base address is ignored for a 64-KB space. *Note: Hardwired to 0.*	RO	RO	–	0h
31:16	**Base Address** Specifies the upper 16 bits of the 32-bit starting Base address of the 64-KB Address space for the PEX 8311 Configuration registers and shared memory.	RW	RW	WO	0h

Register 19-14. Offset 14h PECS_PCIBASE1 PCI Express Base Address 1

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Base Address 1** Determines the upper 32 bits of the address when **PECS_PCIBASE0** is configured for 64-bit addressing.	RW	RW	WO	0h

Register 19-15. Offset 18h PECS_PRIMBUSNUM Primary Bus Number

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Primary Bus Number** Used to record the Bus Number of the internal PCI Bus segment to which the bridge primary interface is connected. *Note: The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.*	RW	RW	WO	0h

Register 19-16. Offset 19h PECS_SECBUSNUM Secondary Bus Number

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Secondary Bus Number** Used to record the Bus Number of the internal PCI Bus segment to which the bridge secondary interface is connected. *Note: The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.*	RW	RW	WO	0h

Register 19-17. Offset 1Ah PECS_SUBBUSNUM Subordinate Bus Number

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Subordinate Bus Number** Used to record the Bus Number of the highest-numbered internal PCI Bus segment behind (or subordinate to) the bridge. *Note: In Endpoint mode, the Subordinate Bus Number is always equal to the Secondary Bus Number.*	RW	RW	WO	0h

Register 19-18. Offset 1Bh PECS_SECLATTIMER Secondary Latency Timer (Endpoint Mode Only)

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Secondary Latency Timer** Valid only in Endpoint mode. Specifies (in units of internal clocks) the Latency Timer value during secondary internal PCI Bus Master bursts. When the Latency Timer expires, the PEX 8311 must terminate its tenure on the bus.	RW	RW	WO	0h

Register 19-19. Offset 1Ch PECS_IOBASE I/O Base

Bit(s)	Description	CFG	MM	EE	Default
3:0	**I/O Base Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other values are *reserved*.	RO	RW	WO	0000b
7:4	**I/O Base** Determines the starting address at which I/O transactions on the primary interface are forwarded to the secondary interface. Bits [3:0] correspond to Address bits AD[15:12]. For address decoding purposes, the bridge assumes that the lower 12 Address bits, AD[11:0], of the I/O Base address are zero (0h). Therefore, the bottom of the defined I/O Address range is aligned to a 4-KB Address Boundary space, and the top is one less than a 4-KB Address Boundary space. *Note: The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	0h

Register 19-20. Offset 1Dh PECS_IOLIMIT I/O Limit

Bit(s)	Description	CFG	MM	EE	Default
3:0	**I/O Limit Address Capability** Indicates the type of addressing for this space. 0000b = 16-bit I/O address 0001b = 32-bit I/O address All other values are *reserved*. The value returned in this field is derived from the **PECS_IOBASE** register *I/O Base Address Capability* field.	RO	RO	–	0000b
7:4	**I/O Limit** Determines the I/O Space range forwarded from the primary interface to the secondary interface. Bits [3:0] correspond to Address bits AD[15:12]. For address decoding purposes, the bridge assumes that the lower 12 Address bits, AD[11:0], of the I/O Limit address are FFFh. When there are no I/O addresses on the secondary interface, this field is programmed to a value smaller than the **PECS_IOBASE** register *I/O Base* field. In this case, the bridge does not forward I/O transactions from the primary interface to the secondary interface; however, it does forward all I/O transactions from the secondary interface to the primary interface. *Note: The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	0h

Register 19-21. Offset 1Eh PECS_SECSTAT Secondary Status (Endpoint Mode)

Bit(s)	Description	CFG	MM	EE	Default
4:0	*Reserved*	RsvdZ	RsvdZ	–	0h
5	**Secondary 66 MHz Capable (Internal Clock Frequency)** Indicates whether the Local Bus interface is capable of operating at 66 MHz.	RO	RO	–	0
6	*Reserved*	RsvdZ	RsvdZ	–	0
7	**Secondary Fast Back-to-Back Transactions Capable** *Not supported* Indicates whether the internal PCI Bus is capable of decoding Fast Back-to-Back transactions. The PEX 8311 does **not support** Fast Back-to-Back decoding.	RO	RO	–	0
8	**Secondary Master Data Parity Error** Reports Data Parity error detection by the bridge when it is the master of the transaction on the Local Bus interface. Set when the following three conditions are true: • Bridge is the bus master of the transaction on Local Bus interface • Bridge asserted internal PERR# (Read transaction) or detected internal PERR# asserted (Write transaction) • **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**Secondary DEVSEL Timing** Hardwired to 01b.	RO	RO	–	01b
11	**Secondary Signaled Target Abort** Reports Target Abort termination signaling by the bridge when it responds as the transaction target on the internal PCI Bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Secondary Received Target Abort** Reports Target Abort termination detection by the bridge when it is the transaction master on the internal PCI Bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Secondary Received Master Abort** Reports Master Abort termination detection by the bridge when it is the transaction master on the internal PCI Bus. Also set for a PCI Express-to-PCI Configuration transaction with an extended address not equal to 0. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Secondary Received System Error** Reports internal SERR# assertion detection on the internal PCI Bus. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Secondary Detected Parity Error** Reports Address or Data Parity error detection by the bridge on the internal PCI Bus. Set when any of the following three conditions are true: • Bridge detects an Address Parity error as a potential target • Bridge detects a Data Parity error when Write transaction target • Bridge detects a Data Parity error when Read transaction master Set irrespective of the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 19-22. Offset 1Eh PECS_SECSTAT Secondary Status (Root Complex Mode)

Bit(s)	Description	CFG	MM	EE	Default
4:0	*Reserved*	RsvdZ	RsvdZ	–	0h
5	**Secondary 66 MHz Capable (Internal Clock Frequency)** Not valid for PCI Express. Indicates whether the PCI Express interface is capable of operating at 66 MHz. Forced to 0.	RO	RO	–	0
6	*Reserved*	RsvdZ	RsvdZ	–	0
7	**Secondary Fast Back-to-Back Transactions Capable** Not valid for PCI Express. Indicates whether the PCI Express interface is capable of decoding Fast Back-to-Back transactions when the transactions are from the same master, but to different targets. Forced to 0.	RO	RO	–	0
8	**Secondary Master Data Parity Error** Used to report Data Parity error detection by the bridge. Set when the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit is set and either of the following two conditions occur: • Bridge receives a completion marked *poisoned* on the PCI Express interface • Bridge poisons a Write request or Read Completion on the PCI Express interface Writing 1 clears this bit.	RW1C	RW1C	–	0
10:9	**Secondary DEVSEL Timing** Does not apply to PCI Express; therefore, forced to 00b.	RO	RO	–	00b
11	**Secondary Signaled Target Abort** Set when the bridge completes a request as a transaction target on the PCI Express interface using Completer Abort completion status. Writing 1 clears this bit.	RW1C	RW1C	–	0
12	**Secondary Received Target Abort** Set when the bridge receives a completion with Completer Abort completion status on the PCI Express interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
13	**Secondary Received Master Abort** Set when the bridge receives a completion with Unsupported Request completion status on the PCI Express interface. Writing 1 clears this bit.	RW1C	RW1C	–	0
14	**Secondary Received System Error** Set when the PEX 8311 receives an ERR_FATAL or ERR_NONFATAL message from the downstream PCI Express device. Writing 1 clears this bit.	RW1C	RW1C	–	0
15	**Secondary Detected Parity Error** Set by the bridge when it receives a poisoned TLP on the PCI Express interface, regardless of the **PECS_BRIDGECTL** register *Secondary Parity Error Response Enable* bit state. Writing 1 clears this bit.	RW1C	RW1C	–	0

Register 19-23. Offset 20h PECS_MEMBASE Memory Base

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Reserved** *Note: Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Base** Determines the starting address at which Memory transactions on the primary interface are forwarded to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Memory Base address are zero (0h). The bottom of the defined Memory Address range is aligned to a 1-MB Address Boundary space, and the top is one less than a 1-MB Address Boundary space. *Note: The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.* *The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.*	RW	RW	WO	–

Register 19-24. Offset 22h PECS_MEMLIMIT Memory Limit

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Reserved** *Note: Hardwired to 0h.*	RsvdP	RsvdP	–	0h
15:4	**Memory Limit** Determines the Memory Space range forwarded from the primary interface to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Memory Limit address are FFFFFh. When there are no Memory-Mapped I/O addresses on the secondary interface, this field must be programmed to a value smaller than the **PECS_MEMBASE** register *Memory Base* field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary interface, the bridge does not forward Memory transactions from the primary interface to the secondary interface; however, it does forward all Memory transactions from the secondary interface to the primary interface. *Note: The primary interface is the PCI Express interface in Endpoint mode, and the Local Bus interface in Root Complex mode.* *The secondary interface is the Local Bus interface in Endpoint mode, and the PCI Express interface in Root Complex mode.*	RW	RW	WO	–

Register 19-25. Offset 24h PECS_PREBASE Prefetchable Memory Base

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Prefetchable Base Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other values are ***reserved***. *Note: This field must be set to 0001b in order to perform 64 bit either Direct Master transfers or DMA transfer to addresses over 4GB.*	RO	RW	WO	0000b
15:4	**Prefetchable Memory Base** Determines the starting address at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Base address are zero (0h). The bottom of the defined Prefetchable Memory Address range is aligned to a 1-MB Address Boundary space, and the top is one less than a 1-MB Address Boundary space. *Note: The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	–

Register 19-26. Offset 26h PECS_PRELIMIT Prefetchable Memory Limit

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Prefetchable Limit Address Capability** Indicates the type of addressing for this space. 0000b = 32-bit I/O address 0001b = 64-bit I/O address All other values are ***reserved***. The value returned in this field is derived from the **PECS_PREBASE** register *Prefetchable Base Address Capability* field.	RO	RO	–	0000b
15:4	**Prefetchable Memory Limit** Determines the Prefetchable Memory Space range forwarded from the primary interface to the secondary interface. The upper 12 bits of this register correspond to Address bits AD[31:20]. For address decoding purposes, the bridge assumes that the lower 20 Address bits, AD[19:0], of the Prefetchable Memory Limit address are FFFFFh. When there is no Prefetchable memory on the secondary interface, this field must be programmed to a value smaller than the **PECS_PREBASE** register *Prefetchable Memory Base* field. When there is no Prefetchable memory, and no Memory-Mapped I/O on the secondary interface, the bridge does not forward Memory transactions from the primary interface to the secondary interface; however, it does forward all Memory transactions from the secondary interface to the primary interface. *Note: The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	–

Register 19-27. Offset 28h PECS_PREBASEUPPER Prefetchable Memory Base Upper 32 Bits

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Base Upper 32 Bits** When the **PECS_PREBASE** register *Prefetchable Base Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Base Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the starting address at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface. *Note: The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	0h

Register 19-28. Offset 2Ch PECS_PRELIMITUPPER Prefetchable Memory Limit Upper 32 Bits

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Prefetchable Memory Limit Upper 32 Bits** When the **PECS_PRELIMIT** register *Prefetchable Limit Address Capability* field indicates 32-bit addressing, this register is Read-Only and returns 0h. When the *Prefetchable Limit Address Capability* field indicates 64-bit addressing, this register determines the upper 32 bits of the range at which Prefetchable Memory transactions on the primary interface are forwarded to the secondary interface. *Notes: Refer to Section 8.5.2, "Prefetchable Memory Base and Limit Registers," for further details.* *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	0h

Register 19-29. Offset 30h PECS_IOBASEUPPER I/O Base Upper 16 Bits

Bit(s)	Description	CFG	MM	EE	Default
15:0	**I/O Base Upper 16 Bits** When the **PECS_IOBASE** register *I/O Base Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0. When the *I/O Base Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the starting address at which I/O transactions on the primary interface are forwarded to the secondary interface. *Note:* *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	–

Register 19-30. Offset 32h PECS_IOLIMITUPPER I/O Limit Upper 16 Bits

Bit(s)	Description	CFG	MM	EE	Default
15:0	**I/O Limit Upper 16 Bits** When the **PECS_IOLIMIT** register *I/O Limit Address Capability* field indicates 16-bit addressing, this register is Read-Only and returns 0. When the *I/O Limit Address Capability* field indicates 32-bit addressing, this register determines the upper 16 bits of the range at which I/O transactions on the primary interface are forwarded to the secondary interface. *Notes:* *Refer to Section 8.3, "I/O Space," for further details.* *The primary interface is PCI Express in Endpoint mode, and Local Bus in Root Complex mode.* *The secondary interface is Local Bus in Endpoint mode, and PCI Express in Root Complex mode.*	RW	RW	WO	–

Register 19-31. Offset 34h PECS_PCICAPPTR PCI Capabilities Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Capabilities Pointer** Provides the offset location of the first New Capabilities register.	RO	RW	WO	40h
31:8	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-32. Offset 3Ch PECS_PCIINTLINE Internal PCI Interrupt Line

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Internal PCI Interrupt Line** Indicates to which system interrupt controller input the device Interrupt pin is connected. Device drivers and operating systems use this field.	RW	RW	WO	0h

Register 19-33. Offset 3Dh PECS_PCIINTPIN Internal PCI Wire Interrupt

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Internal PCI Wire Interrupt** For Endpoint mode, this register identifies the Conventional PCI interrupt message(s) that the PEX 8311 uses. The only valid value is 1h, which maps to Conventional PCI Interrupt messages for INTA#. Value of 0 indicates that the PEX 8311 does not use Conventional PCI Interrupt messages. For Root Complex mode, this register selects the internal PCI INTA# Wire interrupt.	RO	RW	WO	1h

Register 19-34. Offset 3Eh PECS_BRIDGECTL Bridge Control (Endpoint Mode)

Bit(s)	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable** Controls the bridge response to Address and Data Parity errors on the Local Bus interface. 0 = PEX 8311 must ignore Parity errors detected and continue standard operation. A bridge must generate parity, regardless of whether Parity error reporting is disabled. Also, the bridge must always forward Posted Write data with poisoning, from Local-to-PCI Express on a PCI Data Parity error, regardless of this bit's setting. 1 = PEX 8311 must take its normal action when a Parity error is detected.	RW	RW	WO	0
1	**Secondary Internal SERR# Enable** Controls forwarding of Local Bus interface internal SERR# assertions to the PCI Express interface. The bridge transmits an ERR_FATAL message on the PCI Express interface when all the following conditions are true: • Internal SERR# is asserted on the Local Bus interface • This bit is set • **PECS_PCICMD** register *Internal SERR# Enable* bit is set or **PECS_DEVCTL** register *Fatal Error Reporting Enable* or *Non-Fatal Error Reporting Enable* bit is set	RW	RW	WO	0

Register 19-34. Offset 3Eh PECS_BRIDGECTL Bridge Control (Endpoint Mode) (Cont.)

Bit(s)	Description	CFG	MM	EE	Default
2	**ISA Enable** Modifies the bridge response to ISA I/O addresses that are enabled by the **PECS_IOBASE** and **PECS_IOLIMIT** registers and located in the first 64 KB of the PCI I/O Address space. 1 = PEX 8311 blocks forwarding of I/O transactions, from the PCI Express interface to the Local Bus interface, that address the last 768 bytes in each 1-KB block In the opposite direction (Local Bus interface to the PCI Express interface), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.	RW	RW	WO	0
3	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When set to 1, the bridge positively decodes and forwards the following accesses on the PCI Express interface to the Local Bus interface (and, conversely, blocks the forwarding of these addresses from the Local Bus interface to PCI Express interface): • Memory accesses in the range 000A_0000h to 000B_FFFFh • I/O address in the first 64 KB of the I/O Address space [Address[31:16] for PCI Express are zero (0000h)] and where Address[9:0] is in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] can be any value and is not used in decoding) Additionally, when this bit is set, VGA address forwarding is independent of the bit 2 (*ISA Enable*) value, and the I/O and Memory Address ranges defined by the **PECS_IOBASE**, **PECS_IOLIMIT**, **PECS_MEMBASE**, **PECS_MEMLIMIT**, **PECS_PREBASE**, and **PECS_PRELIMIT** registers. VGA address forwarding is qualified by the **PECS_PCICMD** register *I/O Access Enable* and *Memory Space Enable* bits. 0 = Do not forward VGA-compatible Memory and I/O addresses from the PCI Express interface to Local Bus interface (addresses defined above), unless they are enabled for forwarding by the defined I/O and Memory Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the PCI Express interface to the Local Bus interface (when the *I/O Access Enable* and *Memory Space Enable* bits are set), independent of the I/O and Memory Address ranges and *ISA Enable* bit	RW	RW	WO	0

Register 19-34. Offset 3Eh PECS_BRIDGECTL Bridge Control (Endpoint Mode) (Cont.)

Bit(s)	Description	CFG	MM	EE	Default
4	**VGA 16-Bit Decode** Enables the bridge to provide 16-bit decoding of the VGA I/O address, precluding the decoding of alias addresses every 1 KB. Useful only when bit 3 (*VGA Enable*) is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. Enables system configuration software to select between 10- and 16-bit I/O address decoding for VGA I/O register accesses that are forwarded from the PCI Express interface to the Local Bus interface, when the *VGA Enable* bit is set to 1. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	RW	WO	0
5	**Master Abort Mode** Controls bridge behavior when it receives a Master Abort termination on the internal PCI Bus or an Unsupported Request on PCI Express. 0 = Do not report Master Aborts • When PCI Express UR is received: – Return FFFF_FFFFh to internal PCI Bus for reads – Complete Non-Posted Write normally on internal PCI Bus and discard the Write data – Discard posted internal PCI Bus-to-PCI Express Write data • When PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-internal PCI Bus 1 = Report Master Aborts • When PCI Express UR is received: – Complete Reads and Non-Posted Writes with PCI Target Abort – Discard posted internal PCI Bus-to-PCI Express Write data • When PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-internal PCI Bus – Transmit ERR_NONFATAL message for Posted Writes	RW	RW	WO	0
6	**Local Bridge Full Reset** 1 = Forces LRESET# assertion on the Local Bus. Additionally, the bridge Local Bus interface, and buffers between the PCI Express and Local Bus interfaces, must be initialized to their default state. The PCI Express interface and Configuration Space registers must not be affected by setting this bit. Because LRESET# is asserted while this bit is set, software must observe proper PCI Reset timing requirements.	RW	RW	WO	0
7	**Fast Back-to-Back Enable** *Not supported* Controls bridge ability to generate Fast Back-to-Back transactions to different devices on the Local Bus interface.	RO	RO	–	0

Register 19-34. Offset 3Eh PECS_BRIDGECTL Bridge Control (Endpoint Mode) (Cont.)

Bit(s)	Description	CFG	MM	EE	Default
8	**Primary Discard Timer** In Endpoint mode, this bit does not apply and is forced to 0.	RO	RO	–	0
9	**Secondary Discard Timer** Selects the number of internal clocks that the bridge waits for a master on the Local Bus interface to repeat a Delayed Transaction request. The counter starts after the completion (PCI Express Completion associated with the Delayed Transaction request) reaches the head of the bridge downstream queue (*that is*, all ordering requirements are satisfied and the bridge is ready to complete the Delayed Transaction with the originating master on the Local Bus). When the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed Transaction from its queue and sets bit 10 (*Discard Timer Status*). 0 = Secondary Discard Timer counts 2^{15} internal clock periods 1 = Secondary Discard Timer counts 2^{10} internal clock periods	RW	RW	WO	0
10	**Discard Timer Status** 1 = Secondary Discard Timer has expired and a Delayed Completion is discarded from a queue within the bridge Writing 1 clears this bit.	RW1C	RW1C	WO	0
11	**Discard Timer Internal SERR# Enable** When set to 1, enables the bridge to generate an ERR_NONFATAL message on the PCI Express interface when the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue within the bridge. 0 = Do not generate ERR_NONFATAL message on the PCI Express interface as a result of the Secondary Discard Timer expiration 1 = Generate ERR_NONFATAL message on the PCI Express interface when the Secondary Discard Timer expires and a Delayed Transaction is discarded from a queue within the bridge	RW	RW	WO	0
15:12	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-35. Offset 3Eh PECS_BRIDGECTL Bridge Control (Root Complex Mode)

Bit(s)	Description	CFG	MM	EE	Default
0	**Secondary Parity Error Response Enable** Controls the PEX 8311 response to Data Parity errors forwarded from the Local Bus interface (*such as*, a poisoned TLP). 0 = PEX 8311 must ignore detected Data Parity errors, and continue standard operation 1 = PEX 8311 must take its normal action when a Data Parity error is detected	RW	RW	WO	0
1	**Secondary Internal SERR# Enable** No effect in Root Complex mode. PCI Express interface error reporting using internal SERR# is controlled by the **PECS_ROOTCTL** register.	RW	RW	WO	0
2	**ISA Enable** Modifies the PEX 8311 response to ISA I/O addresses that are enabled by the **PECS_IOBASE** and **PECS_IOLIMIT** registers and located in the first 64 KB of the PCI Express I/O Address space. 1 = PEX 8311 blocks forwarding of I/O transactions, from the Local Bus interface to the PCI Express interface, that address the last 768 bytes in each 1-KB block In the opposite direction (PCI Express interface to the Local Bus interface), I/O transactions are forwarded when they address the last 768 bytes in each 1-KB block.	RW	RW	WO	0
3	**VGA Enable** Modifies the PEX 8311 response to VGA-compatible addresses. When set to 1, the bridge positively decodes and forwards the following accesses on the Local Bus interface to the PCI Express interface (and, conversely, blocks the forwarding of these addresses from the PCI Express interface to the Local Bus interface): • Memory accesses in the range 000A_0000h to 000B_FFFFh • I/O address in the first 64 KB of the I/O Address space [Address[31:16] for PCI Express are zero (0000h)] and where Address[9:0] is in the range of 3B0h to 3BBh or 3C0h to 3DFh (inclusive of ISA address aliases – Address[15:10] can be any value and is not used in decoding) Additionally, when this bit is set, VGA address forwarding is independent of the bit 2 (*ISA Enable*) value, and the I/O and Memory Address ranges defined by the **PECS_IOBASE**, **PECS_IOLIMIT**, **PECS_MEMBASE**, **PECS_MEMLIMIT**, **PECS_PREBASE**, **PECS_PRELIMIT** registers. VGA address forwarding is qualified by the **PECS_PCICMD** register *I/O Access Enable* and *Memory Space Enable* bits. 0 = Do not forward VGA-compatible Memory and I/O addresses from the Local Bus interface to the PCI Express interface (addresses defined above), unless they are enabled for forwarding by the defined I/O and Memory Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the Local Bus interface to the PCI Express interface (when the *I/O Access Enable* and *Memory Space Enable* bits are set), independent of the I/O and Memory Address ranges and *ISA Enable* bit	RW	RW	WO	0

Register 19-35. Offset 3Eh PECS_BRIDGECTL Bridge Control (Root Complex Mode) (Cont.)(Cont.)

Bit(s)	Description	CFG	MM	EE	Default
4	**VGA 16-Bit Decode** Enables the bridge to provide 16-bit decoding of the VGA I/O address, precluding the decoding of alias addresses every 1 KB. Useful only when bit 3 (*VGA Enable)* is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. Enables system configuration software to select between 10- and 16-bit I/O address decoding for all VGA I/O register accesses that are forwarded from the Local Bus interface to the PCI Express interface, when the *VGA Enable* bit is set to 1. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses	RW	RW	WO	0
5	**Master Abort Mode** Controls bridge behavior when it receives a Master Abort termination on the internal PCI Bus or an Unsupported Request on PCI Express. 0 = Do not report Master Aborts • When PCI Express UR is received: – Return FFFF_FFFFh to internal PCI Bus for reads – Complete Non-Posted Write normally on internal PCI Bus and discard the Write data – Discard posted internal PCI Bus-to-PCI Express Write data • When PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-internal PCI Bus 1 = Report Master Aborts • When PCI Express UR is received: – Complete Reads and Non-Posted Writes with PCI Target Abort – Discard posted internal PCI Bus-to-PCI Express Write data • When PCI transaction terminates with Master Abort: – Complete Non-Posted transaction with Unsupported Request – Discard Posted Write data from PCI Express-to-internal PCI Bus – Transmit ERR_NONFATAL message for Posted Writes	RW	RW	WO	0
6	**PCI Express Hot Reset** When set, causes an LTSSM Hot Reset training sequence to be generated on the PCI Express interface. (Refer to Chapter 3, "Reset Operation and Initialization Summary," for further details.) When set, causes a Hot Reset to communicate on the PCI Express interface. The PCI Express interface, and buffers between the Local Bus and PCI Express interfaces, must be returned to their default state. The Local Bus interface and Configuration Space registers are not affected by setting this bit.	RW	RW	WO	0
7	**Fast Back-to-Back Enable** *Not supported* Controls bridge ability to generate Fast Back-to-Back transactions to different devices on the PCI Express interface.	RO	RO	–	0

Register 19-35. Offset 3Eh PECS_BRIDGECTL Bridge Control (Root Complex Mode) (Cont.)(Cont.)

Bit(s)	Description	CFG	MM	EE	Default
8	**Primary Discard Timer** Selects the number of internal clocks that the bridge waits for a master on the Local Bus interface to repeat a Delayed Transaction request. The counter starts after the completion (PCI Express Completion associated with the Delayed Transaction request) reaches the head of the bridge downstream queue (*that is*, all ordering requirements are satisfied and the bridge is ready to complete the Delayed Transaction with the originating master on the PCI Express interface). When the originating master does not repeat the transaction before the counter expires, the bridge deletes the Delayed Transaction from its queue and sets bit 10 (*Discard Timer Status*). 0 = Secondary Discard Timer counts 2^{15} internal clock periods 1 = Secondary Discard Timer counts 2^{10} internal clock periods	RW	RW	WO	0
9	**Secondary Discard Timer** In Root Complex mode, this bit does not apply and is forced to 0.	RO	RO	–	0
10	**Discard Timer Status** 1 = Primary Discard Timer has expired and a Delayed Completion is discarded from a queue within the bridge	RW1C	RW1C	–	0
11	**Discard Timer Internal SERR# Enable** When set to 1, enables the bridge to assert internal SERR# on the Local Bus interface when the Primary Discard Timer expires and a Delayed Transaction is discarded from a queue within the bridge. 0 = Do not assert internal SERR# on the Local Bus interface as a result of the Primary Discard Timer expiration 1 = Generate internal SERR# on the Local Bus interface when the Primary Discard Timer expires and a Delayed Transaction is discarded from a queue within the bridge	RW	RW	WO	0
15:12	*Reserved*	RsvdP	RsvdP	–	0h

19.7   PCI-Compatible Capability Registers

This section details the **PECS** PCI-Compatible Capability registers. Table 19-6 defines the register map.

Table 19-6.   PCI-Compatible Capability Register Map

PCI Configuration Register Address	31 24	23 16	15 8	7 0
40h	Power Management Capabilities (Endpoint Mode) Power Management Capabilities (Root Complex Mode)		Power Management Next Capability Pointer	Power Management Capability ID
44h	Power Management Data	Power Management Bridge Support (Endpoint Mode) Power Management Bridge Support (Root Complex Mode)	Power Management Control/Status (Endpoint Mode) Power Management Control/Status (Root Complex Mode)	
48h	Device-Specific Control			
4Ch	*Reserved*			
50h	Message Signaled Interrupts Control		Message Signaled Interrupts Next Capability Pointer	Message Signaled Interrupts Capability ID
54h	Message Signaled Interrupts Address			
58h	Message Signaled Interrupts Upper Address			
5Ch	*Reserved*		Message Signaled Interrupts Data	
60h	PCI Express Capabilities		PCI Express Next Capability Pointer	PCI Express Capability ID
64h	Device Capabilities			
68h	PCI Express Device Status		PCI Express Device Control	
6Ch	Link Capabilities			
70h	Link Status		*Reserved*	Link Control
74h	Slot Capabilities			
78h	Slot Status		Slot Control	
7Ch	*Reserved*		Root Control (Root Complex Mode Only)	
80h	Root Status (Root Complex Mode Only)			
84h	Main Control Register Index			
88h	Main Control Register Data			

Register 19-36. Offset 40h PECS_PWRMNGID Power Management Capability ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Power Management Capability ID** Specifies the Power Management Capability ID.	RO	RO	–	01h

Register 19-37. Offset 41h PECS_PWRMNGNEXT Power Management Next Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Power Management Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List, Message Signaled Interrupts.	RO	RW	WO	50h

Register 19-38. Offset 42h PECS_PWRMNGCAP Power Management Capabilities (Endpoint Mode)

Bit(s)	Description	CFG	MM	EE	Default
2:0	**PME Version** Default 010b indicates compliance with the *PCI Power Mgmt. r1.1.*	RO	RW	WO	010b
3	**PME Clock** For Endpoint mode, does not apply to PCI Express; therefore, must always retain a value of 0.	RO	RO	–	0
4	*Reserved*	RsvdP	RsvdP	–	0
5	**Device-Specific Initialization** Indicates that the PEX 8311 requires special initialization following a transition to the D0_uninitialized state before the generic class device driver uses it.	RO	RW	WO	0
8:6	**AUX Current** Reports the 3.3Vaux auxiliary current requirements for the PCI function. When PCI backplane PME# generation from D3cold is not supported by the function, must return a value of 000b.	RO	RW	WO	000b
9	**D1 Support** Specifies that the PEX 8311 supports the D1 state.	RO	RW	WO	1
10	**D2 Support** Specifies that the PEX 8311 does **not support** the D2 state.	RO	RW	WO	0
15:11	**PME Support** Default 11001b indicates that the corresponding PEX 8311 port forwards PME messages in the D0, D3hot, and D3cold power states. XXXX1b = Assertable from D0 XXX1Xb = Assertable from D1 XX1XXb = *Reserved* X1XXXb = Assertable from D3hot 1XXXXb = Assertable from D3cold	RO	RW	WO	11001b

Register 19-39. Offset 42h PECS_PWRMNGCAP Power Management Capabilities
(Root Complex Mode)

Bit(s)	Description	CFG	MM	EE	Default
2:0	**PME Version** Default 010b indicates compliance with the *PCI Power Mgmt. r1.1.*	RO	RW	WO	010b
3	**PME Clock** When Low, indicates that no internal clock is required to generate PME#. When High, indicates that an internal clock is required to generate PME#.	RO	RW	WO	0
4	*Reserved*	RsvdP	RsvdP	–	0
5	**Device-Specific Initialization** Indicates that the PEX 8311 requires special initialization following a transition to the D0_uninitialized state before the generic class device driver uses it.	RO	RW	WO	0
8:6	**AUX Current** Reports the 3.3Vaux auxiliary current requirements for the PCI function. When PMEOUT# generation from D3cold is not supported by the function, must return a value of 000b.	RO	RW	WO	000b
9	**D1 Support** Specifies that the PEX 8311 supports the D1 state.	RO	RW	WO	1
10	**D2 Support** Specifies that the PEX 8311 does *not support* the D2 state.	RO	RW	WO	0
15:11	**PME Support** Default 11001b indicates that the corresponding PEX 8311 port forwards PME messages in the D0, D3hot, and D3cold power states. XXXX1b = Assertable from D0 XXX1Xb = Assertable from D1 XX1XXb = *Reserved* X1XXXb = Assertable from D3hot 1XXXXb = Assertable from D3cold	RO	RW	WO	11001b

Register 19-40. Offset 44h PECS_PWRMNGCSR Power Management Control/Status (Endpoint Mode)

Bit(s)	Description	CFG	MM	EE	Default
1:0	**Power State** Used to determine or change the current power state. 00b = D0 01b = D1 10b = *Reserved* 11b = D3hot A transition from state D3 to state D0 causes a Soft Reset to occur. In state D1, when the *D1 Support* bit is set, PCI Express Memory and I/O accesses are disabled, as well as the PCI interrupt, and only Configuration cycles are allowed. In state D3hot, these functions are also disabled.	RW	RW	WO	00b
7:2	*Reserved*	RsvdP	RsvdP	–	0h
8	**PME Enable** Enables a PME message to transmit upstream.	RW	RW	WO	0
12:9	**Data Select** *Not supported* Always returns a value of 0h.	RO	RO	–	0h
14:13	**Data Scale** *Not supported* Always returns a value of 00b.	RO	RO	–	00b
15	**PME Status** Indicates that a PME message was transmitted upstream. Writing 1 clears this bit.	RW1C	RW1C	–	0

**Register 19-41. Offset 44h PECS_PWRMNGCSR Power Management Control/Status
(Root Complex Mode)**

Bit(s)	Description	CFG	MM	EE	Default
1:0	**Power State** Used to determine or change the current power state. 00b = D0 01b = D1 10b = *Reserved* 11b = D3hot A transition from state D3 to state D0 causes a Soft Reset. In state D1, when the *D1 Support* bit is set, PCI Express Memory and I/O accesses are disabled, as well as the PCI interrupt, and only Configuration cycles are allowed. In state D3hot, these functions are also disabled.	RW	RW	WO	00b
7:2	*Reserved*	RsvdP	RsvdP	–	0h
8	**PME Enable** Enables the PMEOUT# signal to assert.	RW	RW	WO	0
12:9	**Data Select** *Not supported* Always returns a value of 0h.	RO	RO	–	0h
14:13	**Data Scale** *Not supported* Always returns a value of 00b.	RO	RO	–	00b
15	**PME Status** When bit 8 (*PME Enable*) is set High, indicates that PMEOUT# is being driven. Writing 1 from the internal PCI Bus clears this bit.	RW1C	RW1C	–	0

Register 19-42. Offset 46h PECS_PWRMNGBRIDGE Power Management Bridge Support (Endpoint Mode)

Bit(s)	Description	CFG	MM	EE	Default
5:0	*Reserved*	RsvdP	RsvdP	–	0h
6	**B2/B3 Support** *Not supported* in Endpoint mode; therefore, forced to 0.	RO	RO	–	0
7	**Bus Power/Clock Control Enable** *Not supported* in Endpoint mode; therefore, forced to 0.	RO	RO	–	0

Register 19-43. Offset 46h PECS_PWRMNGBRIDGE Power Management Bridge Support (Root Complex Mode)

Bit(s)	Description	CFG	MM	EE	Default
5:0	*Reserved*	RsvdP	RsvdP	–	0h
6	**B2/B3 Support** 0 = Indicates that, when the bridge function is programmed to D3hot, power is removed (B3) from the PCI Express interface. Useful only when bit 7 (*Bus Power/Clock Control Enable*) is set 1 = Indicates that, when the bridge function is programmed to D3hot, the PCI Express interface internal clock is stopped (B2)	RO	RW	WO	0
7	**Bus Power/Clock Control Enable** 1 = Indicates that the bus power/clock control mechanism (as defined in the *PCI-to-PCI Bridge r1.1*, Section 4.7.1) is enabled	RO	RW	WO	0

Register 19-44. Offset 47h PECS_PWRMNGDATA Power Management Data

Bit(s)	Description	CFG	MM	EE	Default
7:0	**Power Management Data** *Not supported* Always returns a value of 0h.	RO	RO	–	0h

Register 19-45. Offset 48h PECS_DEVSPECCTL Device-Specific Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Blind Prefetch Enable** 0 = Memory Read command on the internal PCI Bus that targets the PCI Express Memory space causes only 1 word to be read from the PCI Express interface 1 = Memory Read command on the internal PCI Bus that targets the PCI Express Memory space causes a cache line to be read from the PCI Express interface	RW	RW	WO	0
1	**PCI Express Base Address 0 Enable** 1 = Enables the PCI Express Base Address 0 space for Memory-Mapped access to the Configuration registers and shared memory. PCI Express Base Address 0 is also enabled when the BAR0ENB# ball is Low.	RW	RW	WO	0
2	**L2 Enable** Valid only in Root Complex mode. 0 = Power state change to D3 does not cause the PEX 8311 to change the Link state to L2 1 = Power state change to D3 causes the PEX 8311 to change the Link state to L2	RW	RW	WO	0
3	**PMU Power Off** 1 = Link has transitioned to the L2/L3 Ready state, and is ready to power down	RO	RO	–	0
7:4	**PMU Link State** Indicates the Link state. 0001b = L0 0010b = L0s 0100b = L1 1000b = L2	RO	RO	–	–
9:8	**CRS Retry Control** Determines the PEX 8311 PCI Express bridge's response on the internal PCI Bus when a Direct Master Configuration transaction originating on the Local Bus and forwarded to a device in PCI Express Space is terminated with a Configuration Request Retry status. 00b = Retry once after 1s. When another CRS is received, Target Abort on the internal PCI Bus. 01b = Retry eight times, once per second. When another CRS is received, Target Abort on the internal PCI Bus. 10b = Retry once per second until successful completion. 11b = *Reserved*.	RW	RW	WO	00b
10	**WAKE Out Enable** Valid only in Endpoint mode. 1 = WAKEOUT# signal is asserted when the Link is in the L2 state	RW	RW	WO	0
11	**Beacon Generate Enable** Valid only in Endpoint mode. 1 = Beacon is generated when the Link is in the L2 state	RW	RW	WO	0

Register 19-45. Offset 48h PECS_DEVSPECCTL Device-Specific Control (Cont.)

Bit(s)	Description	CFG	MM	EE	Default
12	**Beacon Detect Enable** Valid only in Root Complex mode. 1 = Beacon detected while the Link is in the L2 state causes the PEX 8311 to set the **PECS Power Management Control/Status** register *PME Status* bit (PECS_PWRMNGCSR[15])	RW	RW	WO	0
13	**PLL Locked** High when the internal PLL is locked.	RO	RO	–	–
15:14	*Reserved*	RsvdP	RsvdP	–	00b
20:16	**Link Training and Status State Machine** *For internal use only*	RO	RO	–	–
31:21	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-46. Offset 50h PECS_MSIID Message Signaled Interrupts Capability ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**MSI Capability ID** Specifies the Message Signaled Interrupts Capability ID.	RO	RO	–	5h

Register 19-47. Offset 51h PECS_MSINEXT Message Signaled Interrupts Next Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**MSI Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List, PCI Express Capability.	RO	RW	WO	60h

Register 19-48. Offset 52h PECS_MSICTL Message Signaled Interrupts Control

Bit(s)	Description	CFG	MM	EE	Default
Note:	*In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*				
0	**MSI Enable** When set to 1: • Enables the PEX 8311 to use MSI to request service • Virtual interrupt support for internal interrupt sources is disabled for Endpoint mode • INTA# output is disabled in Root Complex mode *Note: When MSI interrupts are enabled, virtual wire interrupt sources, including local bus interrupts, are disabled*	RW	RW	WO	0
3:1	**Multiple Message Capable** System software reads this field to determine the number of requested messages. The number of requested messages must be aligned to a power of two (when a function requires three messages, it requests four). 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b, 111b = **Reserved**	RO	RO	–	000b
6:4	**Multiple Message Enable** System software writes to this field to indicate the number of allocated messages (equal to or less than the number of requested messages). The number of allocated messages is aligned to a power of two. 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b, 111b = **Reserved**	RW	RW	WO	000b
7	**MSI 64-Bit Address Capable** 1 = PEX 8311 is capable of generating a 64-bit Message address	RO	RW	WO	1 (E) 0 (RC)
8	**Per Vector Masking Capable** *Not supported* Forced to 0.	RO	RO	–	0
15:9	**Reserved**	RsvdP	RsvdP	–	0h

Register 19-49. Offset 54h PECS_MSIADDR Message Signaled Interrupts Address

Bit(s)	Description	CFG	MM	EE	Default
1:0	*Reserved*	RsvdP	RsvdP	–	00b
31:2	**MSI Address** When the **PECS_MSICTL** register *MSI Enable* bit (bit 0) is set, the register contents specify the DWORD-aligned address for the MSI Memory Write transaction. Address bits [1:0] are driven to zero (00b) during the Address phase.	RW	RW	WO	0h

Register 19-50. Offset 58h PECS_MSIUPPERADDR Message Signaled Interrupts Upper Address

Bit(s)	Description	CFG	MM	EE	Default
31:0	**MSI Upper Address** Optionally implemented only when the device supports 64-bit Message addressing [**PECS_MSICTL** register *MSI 64-Bit Address Capable* bit (bit 7) is set]. When the **PECS_MSICTL** register *MSI Enable* bit (bit 0) is set, the register contents specify the upper 32 bits of a 64-bit Message address. When the register contents are zero (0h), the PEX 8311 uses the 32-bit address specified by the **PECS_MSIADDR** register.	RW	RW	WO	0h

Register 19-51. Offset 5Ch PECS_MSIDATA Message Signaled Interrupts Data

Bit(s)	Description	CFG	MM	EE	Default
15:0	**MSI Data** When the **PECS_MSICTL** register *MSI Enable* bit (bit 0) is set, the message data is driven onto the lower word (AD[15:0]) of the Memory Write transaction Data phase.	RW	RW	WO	0h
31:16	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-52. Offset 60h PECS_PCIEXID PCI Express Capability ID

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Express Capability ID** Specifies the PCI Express Capability ID.	RO	RW	–	10h

Register 19-53. Offset 61h PECS_PCIEXNEXT PCI Express Next Capability Pointer

Bit(s)	Description	CFG	MM	EE	Default
7:0	**PCI Express Next Capability Pointer** Points to the first location of the next item in the New Capabilities Linked List.	RO	RW	WO	0h

Register 19-54. Offset 62h PECS_PCIEXCAP PCI Express Capabilities

Bit(s)	Description	CFG	MM	EE	Default
Note:	*In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*				
3:0	**Capability Version** Indicates the PCI Express Capability structure version number.	RO	RW	WO	1h
7:4	**Device/Port Type** Indicates the type of PCI Express logical device. 0000b = PCI Express Endpoint Device 0001b = Conventional PCI Express Endpoint Device 0100b = Root Port of PCI Express Root Complex 0101b = Upstream Port of PCI Express Switch 0110b = Downstream Port of PCI Express Switch 0111b = PCI Express-to-PCI/PCI-X Bridge 1000b = PCI/PCI-X-to-PCI Express Bridge All other values are ***reserved***.	RO	RW	WO	0111b (E) 1000b (RC)
8	**Slot Implemented** 1 = Indicates that the PCI Express Link associated with this port is connected to a slot	RO	RW	WO	0
13:9	**Interrupt Message Number** When this function is allocated more than one MSI interrupt number, this field must contain the offset between the Base Message data and the MSI message generated when status bits in the **PECS_SLOTSTAT** or **PECS_ROOTSTAT** register of this capability structure are set. For the field to be correct, hardware must update it when the number of MSI messages assigned to the device changes.	RO	RO	–	0h
15:14	***Reserved***	RsvdP	RsvdP	–	00b

Register 19-55. Offset 64h PECS_DEVCAP Device Capabilities

Bit(s)	Description	CFG	MM	EE	Default
2:0	**Maximum Payload Size Supported** Indicates the supported Maximum Payload Size for TLPs. 000b = 128 bytes *Note: Because the PEX 8311 only supports a Maximum Payload Size of 128 bytes, this field is hardwired to 000b.*	RO	RO	–	000b
4:3	**Phantom Functions Supported** *Not supported* Hardwired to 00b. Indicates support for the use of unclaimed Function Numbers to extend the number of outstanding transactions allowed, by logically combining unclaimed Function Numbers (called Phantom Functions) with the *Tag* identifier.	RO	RO	–	00b
5	**Extended Tag Field Supported** Indicates the maximum supported size of the *Tag* field. 0 = 5-bit *Tag* field is supported 1 = 8-bit *Tag* field is supported *Note: 8-bit Tag field support must be enabled by the corresponding Control field in the* **PECS_DEVCTL** *register.*	RO	RW	WO	0
8:6	**Endpoint L0s Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L0s state to the L0 state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the reported L0s Acceptable Latency number to compare against the L0s exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port, to determine whether Active State Link PM L0s entry is used with no performance loss. 000b = Less than 64 ns 001b = 64 ns to less than 128 ns 010b = 128 ns to less than 256 ns 011b = 256 ns to less than 512 ns 100b = 512 ns to 1 μs 101b = 1 μs to less than 2 μs 110b = 2 to 4 μs 111b = More than 4 μs	RO	RW	WO	000b

Register 19-55. Offset 64h PECS_DEVCAP Device Capabilities (Cont.)

Bit(s)	Description	CFG	MM	EE	Default
11:9	**Endpoint L1 Acceptable Latency** Indicates the acceptable total latency that an Endpoint withstands due to the transition from the L1 state to the L0 state. It is essentially an indirect measure of the Endpoint internal buffering. Power management software uses the report L1 Acceptable Latency number to compare against the L1 exit latencies reported by all components comprising the data path from this Endpoint to the Root Complex Root Port to determine whether Active State Link PM L1 entry is used with no performance loss. 000b = Less than 1 μs 001b = 1 μs to less than 2 μs 010b = 2 μs to less than 4 μs 011b = 4 μs to less than 8 μs 100b = 8 μs to less than 16 μs 101b = 16 μs to less than 32 μs 110b = 32 to 64 μs 111b = More than 64 μs	RO	RW	WO	000b
12	**Attention Button Present** *Not supported* Forced to 0.	RO	RO	–	0
13	**Attention Indicator Present** *Not supported* Forced to 0.	RO	RO	–	0
14	**Power Indicator Present** *Not supported* Forced to 0.	RO	RO	–	0
17:15	*Reserved*	RsvdP	RsvdP	–	000b
25:18	**Captured Slot Power Limit Value** Specifies the upper limit on power supplied by slot in combination with the *Slot Power Limit Scale* value. The Power limit (in Watts) is calculated by multiplying the value in this field by the *Slot Power Limit Scale* field value. Value is set by the Set Slot Power Limit message.	RO	RW	WO	0h
27:26	**Captured Slot Power Limit Scale** Specifies the scale used for the *Slot Power Limit Value*. Value is set by the Set Slot Power Limit message. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	RW	WO	00b
31:28	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-56. Offset 68h PECS_DEVCTL PCI Express Device Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Correctable Error Reporting Enable** Valid only in Endpoint mode. Controls Correctable error reporting. When a Correctable error is detected in Endpoint mode and this bit is set, an ERR_COR message is transmitted to the Root Complex.	RW	RW	WO	0
1	**Non-Fatal Error Reporting Enable** Valid only in Endpoint mode. Controls Non-Fatal error reporting. When a Non-Fatal error is detected in Endpoint mode and this bit is set, an ERR_NONFATAL message is transmitted to the Root Complex.	RW	RW	WO	0
2	**Fatal Error Reporting Enable** Valid only in Endpoint mode. Controls Fatal error reporting. When a Fatal error is detected in Endpoint mode and this bit is set, an ERR_FATAL message is transmitted to the Root Complex.	RW	RW	WO	0
3	**Unsupported Request Reporting Enable** Valid only in Endpoint mode. Controls Unsupported Request reporting. When an Unsupported Request response is received from the PCI Express in Endpoint mode and this bit is set, a ERR_NONFATAL message is transmitted to the Root Complex.	RW	RW	WO	0
4	**Enable Relaxed Ordering** *Not supported* 1 = Device is permitted to set the *Relaxed Ordering* bit in the Attributes field of transactions it initiates that do not require Strong Write ordering Forced to 0.	RO	RO	–	0
7:5	**Maximum Payload Size** Sets the maximum TLP payload size for the device. As a receiver, the device must handle TLPs as large as the set value. As a transmitter, the device must not generate TLPs exceeding the set value. Permissible values for transmitted TLPs are indicated in the **PECS_DEVCAP** register *Maximum Payload Size Supported* field. 000b = 128 bytes 001b = 256 bytes 010b = 512 bytes 011b = 1,024 bytes 100b = 2,048 bytes 101b = 4,096 bytes 110b, 111b = *Reserved*	RW	RW	WO	000b

Register 19-56. Offset 68h PECS_DEVCTL PCI Express Device Control (Cont.)

Bit(s)	Description	CFG	MM	EE	Default
8	**Extended Tag Field Enable** 0 = Device is restricted to a 5-bit *Tag* field. Forced to 0 when the **PECS_DEVCAP** register *Extended Tag Field Supported* bit is cleared. 1 = Enables the device to use an 8-bit *Tag* field as a Requester.	RW	RW	WO	0
9	**Phantom Function Enable** *Not supported* Hardwired to 0.	RO	RO	–	0
10	**Auxiliary (AUX) Power PM Enable** *Not supported* Hardwired to 0.	RO	RO	–	0
11	**Enable No Snoop** *Not supported* Hardwired to 0. 1 = PEX 8311 is permitted to set the *No Snoop* bit in the Requester Attributes of transactions it initiates that do not require hardware-enforced cache coherency. Setting this bit to 1 does not cause a device to blindly set the *No Snoop* attribute on transactions that it initiates. Although this bit is set to 1, a device only sets the *No Snoop* attribute on a transaction when it can guarantee that the transaction address is not stored in a system cache. The PEX 8311 never sets the *No Snoop* attribute; therefore, forced to 0.	RO	RO	–	0
14:12	**Maximum Read Request Size** The value specified in this register is the upper boundary of this field if the **PECS_DEVSPECCTL** register *Blind Prefetch Enable* bit is set. Sets the maximum Read Request size for the device as a Requester. The device must not generate Read Requests with size exceeding the set value. 000b = 128 bytes 001b = 256 bytes 010b = 512 bytes 011b = 1,024 bytes 100b = 2,048 bytes 101b = 4,096 bytes 110b, 111b = *Reserved*	RW	RW	WO	010b
15	**Bridge Configuration Retry Enable** 0 = PEX 8311 does not generate completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions. 1 = PEX 8311 generates completions with Completion Retry Status on behalf of PCI Express-to-PCI Configuration transactions. This occurs after a delay determined by the **PECS CRS Timer** register.	RW	RW	WO	0

Register 19-57. Offset 6Ah PECS_DEVSTAT PCI Express Device Status

Bit(s)	Description	CFG	MM	EE	Default
0	**Correctable Error Detected** Indicates detected Correctable errors status. Errors are logged in this register, regardless of whether error reporting is enabled in the **PECS_DEVCTL** register.	RW1C	RW1C	–	0
1	**Non-Fatal Error Detected** Indicates detected Non-Fatal errors status. Errors are logged in this register, regardless of whether error reporting is enabled in the **PECS_DEVCTL** register.	RW1C	RW1C	–	0
2	**Fatal Error Detected** Indicates detected Fatal errors status. Errors are logged in this register, regardless of whether error reporting is enabled in the **PECS_DEVCTL** register.	RW1C	RW1C	–	0
3	**Unsupported Request Detected** Indicates that the PEX 8311 received an Unsupported Request. Errors are logged in this register, regardless of whether error reporting is enabled in the **PECS_DEVCTL** register.	RW1C	RW1C	–	0
4	**AUX Power Detected** Devices that require AUX power report this bit as set when the device detects AUX power.	RO	RO	–	0
5	**Transactions Pending** Because the PEX 8311 does not internally generate Non-Posted transactions, this bit is forced to 0.	RO	RO	–	0
15:6	*Reserved*	RsvdZ	RsvdZ	–	0h

Register 19-58. Offset 6Ch PECS_LINKCAP Link Capabilities

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Maximum Link Speed** Indicates the maximum Link speed of the given PCI Express Link. Set to 0001b for 2.5 Gbps. All other values are ***reserved***.	RO	RO	–	0001b
9:4	**Maximum Link Width** Indicates the maximum width of the given PCI Express Link. By default, the PEX 8311 has a x1 Link; therefore, this field is hardwired to 000001b. All other values are ***not supported***.	RO	RO	–	000001b
11:10	**Active State Link PM Support** Indicates the level of active state power management supported on the given PCI Express Link. 01b = L0s Entry supported 11b = L0s and L1 supported 00b, 10b = ***Reserved***	RO	RW	WO	11b
14:12	**L0s Exit Latency** Indicates the L0s exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete the transition from L0s to L0. 000b = Less than 64 ns 001b = 64 ns to less than 128 ns 010b = 128 ns to less than 256 ns 011b = 256 ns to less than 512 ns 100b = 512 ns to 1 μs 101b = 1 μs to less than 2 μs 110b = 2 to 4 μs 111b = More than 4 μs	RO	RW	WO	100b
17:15	**L1 Exit Latency** Indicates the L1 exit latency for the given PCI Express Link. The value reported indicates the length of time this port requires to complete the transition from L1 to L0. 000b = Less than 1 μs 001b = 1 μs to less than 2 μs 010b = 2 μs to less than 4 μs 011b = 4 μs to less than 8 μs 100b = 8 μs to less than 16 μs 101b = 16 μs to less than 32 μs 110b = 32 to 64 μs 111b = More than 64 μs	RO	RW	WO	100b
23:18	***Reserved***	RsvdP	RsvdP	–	0h
31:24	**Port Number** Indicates the PCI Express port number for the given PCI Express Link.	RO	RW	WO	0h

Register 19-59. Offset 70h PECS_LINKCTL Link Control

Bit(s)	Description	CFG	MM	EE	Default
Note:	In the **CFG**, **MM**, and **EE** columns, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.				
1:0	**Active State Link PM Control** Controls the level of active state PM supported on the given PCI Express Link. 00b = Disabled 01b = L0s Entry Supported 10b = *Reserved* 11b = L0s and L1 Entry Supported *Note:* *"L0s Entry Enabled" indicates the Transmitter entering L0s.*	RW	RW	WO	00b
2	*Reserved*	RsvdP	RsvdP	–	0
3	**Read Completion Boundary (RCB) Control** 0 = Read Completion boundary is 64 bytes 1 = Read Completion boundary is 128 bytes	RW (E) RO (RC)	RW	WO	0
4	**Link Disable** Valid only in Root Complex mode. 1 = Disables the Link. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.	RO (E) RW (RC)	RO (E) RW (RC)	– (E) WO (RC)	0
5	**Retrain Link** Valid only in Root Complex mode. 1 = Initiates Link retraining. Always returns 0 when read.	RO (E) RW (RC)	RO (E) RW (RC)	– (E) WO (RC)	0
6	**Common Clock Configuration** 0 = Indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. Components use this common clock configuration information to report the correct L0s and L1 Exit Latencies. 1 = Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock.	RW	RW	WO	0
7	**Extended Sync** 1 = Forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from the L1 state prior to entering the L0 state. This mode provides external devices monitoring the Link sufficient time to achieve bit and symbol lock before the Link enters the L0 state and resumes communication.	RW	RW	WO	0
15:8	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-60. Offset 72h PECS_LINKSTAT Link Status

Bit(s)	Description	CFG	MM	EE	Default
3:0	**Link Speed** Indicates the negotiated Link speed of the given PCI Express Link. Set to 0001b for 2.5 Gbps. All other values are *reserved*.	RO	RO	–	0001b
9:4	**Negotiated Link Width** Indicates the negotiated width of the given PCI Express Link. By default, the PEX 8311 has a x1 Link; therefore, this field is hardwired to 000001b. All other values are *not supported*.	RO	RO	–	000001b
10	**Link Training Error** Valid only in Root Complex mode. Indicates that a Link Training error occurred. Cleared by hardware upon successful training of the Link to the L0 state.	RO	RO	–	0
11	**Link Training** Valid only in Root Complex mode. Indicates that Link training is in progress; hardware clears this bit after Link training is complete.	RO	RO	–	0
12	**Slot Clock Configuration** Indicates that the component uses the same physical reference clock that the platform provides on the connector. When the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be cleared.	HwInit	RW	WO	0
15:13	*Reserved*	RsvdZ	RsvdZ	–	000b

Register 19-61. Offset 74h PECS_SLOTCAP Slot Capabilities

Bit(s)	Description	CFG	MM	EE	Default
0	**Attention Button Present** *Not supported* Forced to 0.	RO	RO	–	0
1	**Power Controller Present** *Not supported* Forced to 0.	RO	RO	–	0
2	**MRL Sensor Present** *Not supported* Forced to 0.	RO	RO	–	0
3	**Attention Indicator Present** *Not supported* Forced to 0.	RO	RO	–	0
4	**Power Indicator Present** *Not supported* Forced to 0.	RO	RO	–	0
5	**Hot Plug Surprise** *Not supported* Forced to 0.	RO	RO	–	0
6	**Hot Plug Capable** *Not supported* Forced to 0.	RO	RO	–	0
14:7	**Slot Power Limit Value** Valid only in Root Complex mode. In combination with the *Slot Power Limit Scale* value, specifies the upper limit on power supplied by the slot. The Power limit (in Watts) is calculated by multiplying the value in this field by the *Slot Power Limit Scale* field value. Writes to this register cause the PEX 8311 to transmit the Set Slot Power Limit message downstream.	RO	RW	WO	25d
16:15	**Slot Power Limit Scale** Valid only in Root Complex mode. Specifies the scale used for the *Slot Power Limit Value*. Writes to this register cause the PEX 8311 to transmit the Set Slot Power Limit message downstream. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	RW	WO	00b
18:17	***Reserved***	RsvdP	RsvdP	–	00b
31:19	**Physical Slot Number** *Not supported* Forced to 0h.	RO	RO	–	0h

Register 19-62. Offset 78h PECS_SLOTCTL Slot Control

Bit(s)	Description	CFG	MM	EE	Default
0	**Attention Button Pressed Enable** *Not supported* Forced to 0.	RW	RW	WO	0
1	**Power Fault Detected Enable** *Not supported* Forced to 0.	RW	RW	WO	0
2	**MRL Sensor Changed Enable** *Not supported* Forced to 0.	RW	RW	WO	0
3	**Presence Detect Changed Enable** *Not supported* Forced to 0.	RW	RW	WO	0
4	**Command Completed Interrupt Enable** *Not supported* Forced to 0.	RW	RW	WO	0
5	**Hot Plug Interrupt Enable** *Not supported* Forced to 0.	RW	RW	WO	0
7:6	**Attention Indicator Control** *Not supported* Forced to 00b.	RW	RW	WO	00b
9:8	**Power Indicator Control** *Not supported* Forced to 00b.	RW	RW	WO	00b
10	**Power Controller Control** *Not supported* Forced to 0.	RW	RW	WO	0
15:11	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-63. Offset 7Ah PECS_SLOTSTAT Slot Status

Bit(s)	Description	CFG	MM	EE	Default
0	**Attention Button Pressed** *Not supported* Forced to 0.	RO	RO	–	0
1	**Power Fault Detected** *Not supported* Forced to 0.	RO	RO	–	0
2	**MRL Sensor Changed** *Not supported* Forced to 0.	RO	RO	–	0
3	**Presence Detect Changed** *Not supported* Forced to 0.	RO	RO	–	0
4	**Command Completed** *Not supported* Forced to 0.	RO	RO	–	0
5	**MRL Sensor State** *Not supported* Forced to 0.	RO	RO	–	0
6	**Presence Detect State** *Not supported* Forced to 1.	RO	RO	–	1
15:7	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-64. Offset 7Ch PECS_ROOTCTL Root Control (Root Complex Mode Only)

Bit(s)	Description	CFG	MM	EE	Default
0	**System Error on Correctable Error Enable** 1 = System error (internal SERR#) is generated when an ERR_COR error is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself	RW	RW	WO	0
1	**System Error on Non-Fatal Error Enable** 1 = System error (internal SERR#) is generated when an ERR_NONFATAL error is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself	RW	RW	WO	0
2	**System Error on Fatal Error Enable** 1 = System error (internal SERR#) is generated when an ERR_FATAL error is reported by devices in the hierarchy associated with this Root Port, or by the Root Port itself	RW	RW	WO	0
3	**PME Interrupt Enable** 1 = Enables PME interrupt generation upon PME message receipt as reflected in the **PECS Root Status** register *PME Status* bit is set (PECS_ROOTSTAT[16]). A PME interrupt is also generated when the *PME Status* bit is set when this bit is set from a cleared state.	RW	RW	WO	0
31:4	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-65. Offset 80h PECS_ROOTSTAT Root Status (Root Complex Mode Only)

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PME Requester ID** Indicates the PCI Requester ID of the last PME Requester.	RO	RO	–	–
16	**PME Status** Indicates that PME was asserted by the Requester ID indicated in field [15:0] (*PME Requester ID*). Subsequent PMEs remain pending until this bit is cleared by software, by writing 1.	RW1C	RW1C	–	0
17	**PME Pending** Indicates that another PME is pending when bit 16 (*PME Status*) is set. When the *PME Status* bit is cleared by software, the PME is delivered by hardware by setting the *PME Status* bit again and updating the Requester ID appropriately. Cleared by hardware when no other PMEs are pending.	RO	RO	–	–
31:18	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-66. Offset 84h PECS_MAININDEX Main Control Register Index

Bit(s)	Description	CFG	MM	EE	Default
11:0	**Main Control Register Index** Selects a **Main Control** register that is accessed by way of the **PECS_MAINDATA** register.	RW	RW	WO	0h
31:12	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-67. Offset 88h PECS_MAINDATA Main Control Register Data

Bit(s)	Description	CFG	MM	EE	Default
31:0	**Main Control Register Data** Writes to and reads from this register are mapped to a **Main Control** register selected by the **PECS_MAININDEX** register.	RW	RW	WO	0h

19.8   PCI Express Extended Capability Registers

This section details the **PECS** PCI Express Extended Capability registers. Table 19-7 defines the register map.

Table 19-7.   PCI Express Extended Capability Register Map

PCI Express Configuration Register Offset	31 20	19 16	15 8	7 0
100h	Power Budgeting Next Capability Offset	Power Budgeting Capability Version	Power Budgeting PCI Express Extended Capability ID	
104h	Reserved			Power Budgeting Data Select
108h	Power Budgeting Data			
10Ch	Reserved			Power Budget Capability
110h	Serial Number Next Capability Offset	Serial Number Capability Version	Serial Number PCI Express Extended Capability ID	
114h	Serial Number Low (Lower DWORD)			
118h	Serial Number Hi (Upper DWord)			

19.8.1   PCI Express Power Budgeting Registers

Register 19-68. Offset 100h PECS_PWRCAPHDR Power Budgeting Capability Header

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI-SIG-defined ID Number that indicates the nature and format of the extended capability.	RO	RW	WO	4h
19:16	**Capability Version** PCI-SIG-defined Version Number that indicates the version of the capability structure present.	RO	RW	WO	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express Capability structure, or 000h when no other items exist in the New Capabilities Linked List. Set to 110h when Serial Number Capability must be enabled.	RO	RW	WO	000h

Register 19-69. Offset 104h PECS_PWRDATASEL Power Budgeting Data Select

Bit(s)	Description	CFG	MM	EE	Default
	Note: *The PECS_PWRDATA register returns the DWORD of Power Budgeting Data selected by the this register. When PECS_PWRDATASEL has a value greater than or equal to the number of operating conditions for which the PEX 8311 provides power information, this register returns all zeros (0h). The PEX 8311 supports 32 operating conditions.*				
7:0	**Data Select Register** Indexes the Power Budgeting Data reported through the **PECS_PWRDATA** register. Selects the DWORD of Power Budgeting Data that is to appear in the **PECS_PWRDATA** register. The PEX 8311 supports values from 0 to 31 for this field. For values greater than 31, a value of 0h is returned when the **PECS_PWRDATA** register is read.	RW	RW	WO	0h
31:8	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-70. Offset 108h PECS_PWRDATA Power Budgeting Data

Bit(s)	Description	CFG	MM	EE	Default
Note:	*This register returns the DWORD of Power Budgeting Data selected by the **PECS_PWRDATASEL** register. When the PECS_PWRDATASEL register has a value greater than or equal to the number of operating conditions for which the PEX 8311 provides power information, this register returns all zeros (0h). The PEX 8311 supports 32 operating conditions.*				
7:0	**Base Power** Specifies (in Watts) the base power value in the given operating condition. This value must be multiplied by the *Data Scale* to produce the actual power consumption value.	RO	RW	WO	0h
9:8	**Data Scale** Specifies the scale to apply to the *Base Power* value. The PEX 8311 power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	RO	RW	WO	00b
12:10	**PM Sub-State** Specifies the power management sub-state of the operating condition being described. 000b = Default Sub-State All other values = Device-Specific Sub-State	RO	RW	WO	000b
14:13	**PM State** Specifies the power management state of the operating condition being described. A device returns 11b in this field and Aux or PME Aux in field [17:15] (*PM Type*), to specify the D3cold PM state. An encoding of 11b along with any other *PM Type* field value specifies the D3hot state. 00b = D0 01b = D1 10b = *Reserved* 11b = D3	RO	RW	WO	00b
17:15	**PM Type** Specifies the type of the operating condition being described. 000b = PME Aux 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other values are *reserved*.	RO	RW	WO	000b
20:18	**Power Rail** Specifies the power rail of the operating condition being described. 000b = Power (12V) 001b = Power (3.3V) 111b = Thermal 010b = Power (1.8V) All other values are *reserved*.	RO	RW	WO	000b
31:21	*Reserved*	RsvdP	RsvdP	–	0h

Register 19-71. Offset 10Ch PECS_PWRBUDCAP Power Budget Capability

Bit(s)	Description	CFG	MM	EE	Default
0	**System Allocated** 1 = Indicates that the device power budget is included within the system power budget. Software must ignore Reported Power Budgeting Data for power budgeting decisions.	RO	RW	WO	0
31:1	*Reserved*	RsvdP	RsvdP	–	0h

19.8.2   PCI Express Serial Number Registers

Register 19-72. Offset 110h PECS_SERCAPHDR Serial Number Capability Header

Bit(s)	Description	CFG	MM	EE	Default
15:0	**PCI Express Extended Capability ID** PCI-SIG-defined ID Number that indicates the nature and format of the extended capability. Forced to 0 when Serial Number Capability is disabled.	RO	RO	–	3h
19:16	**Capability Version** PCI-SIG-defined Version Number that indicates the version of the capability structure present. Forced to 0 when Serial Number Capability is disabled.	RO	RO	–	1h
31:20	**Next Capability Offset** Contains the offset to the next PCI Express Capability structure, or 000h when no other items exist in the New Capabilities Linked List.	RO	RO	–	000h

Register 19-73. Offset 114h PECS_SERNUMLOW Serial Number Low (Lower DWORD)

Bit(s)	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the lower DWORD of the IEEE-defined 64-bit extended unique identifier. Includes a 24-bit Company ID value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0 when Serial Number Capability is disabled.	RO	RW	WO	0h

Register 19-74. Offset 118h PECS_SERNUMHI Serial Number Hi (Upper DWord)

Bit(s)	Description	CFG	MM	EE	Default
31:0	**PCI Express Device Serial Number** Contains the upper DWORD of the IEEE-defined 64-bit extended unique identifier. This identifier includes a 24-bit Company ID value assigned by the IEEE registration authority and a 40-bit extension identifier assigned by the manufacturer. Forced to 0 when Serial Number Capability is disabled.	RO	RW	WO	0h

19.9   Main Control Registers

This section details the **PECS** Main Control registers. Table 19-8 defines the register map.

Table 19-8.   Main Control Register Map

PCI Express Configuration Register Address	31 24	23 16	15 8	7 0
1000h	Device Initialization			
1004h	Serial EEPROM Control			
1008h	Serial EEPROM Clock Frequency			
100Ch	PCI Control			
1010h	PCI Express Interrupt Request Enable			
1014h	PCI Interrupt Request Enable			
1018h	Interrupt Request Status			
101Ch	Power (Endpoint Mode Only)			
1020h	General-Purpose I/O Control			
1024h	General-Purpose I/O Status			
1030h	Mailbox 0			
1034h	Mailbox 1			
1038h	Mailbox 2			
103Ch	Mailbox 3			
1040h	*Reserved*		Chip Silicon Revision	
1044h	Diagnostic Control (Factory Test Only)			
1048h	*Reserved*	TLP Controller Configuration 0		
104Ch	TLP Controller Configuration 1			
1050h	TLP Controller Configuration 2			
1054h	*Reserved*	TLP Controller Tag		
1058h	TLP Controller Time Limit 0			
105Ch	TLP Controller Time Limit 1			
1060h	*Reserved*		CRS Timer	
1064h	Enhanced Configuration Address			

Register 19-75. Offset 1000h PECS_DEVINIT Device Initialization

Bit(s)	Description	Access	Default
3:0	**CLKOUT Clock Frequency** Controls the CLKOUT ball frequency. 0000b = 0; the clock is stopped and remains at a logic Low. Non-zero values represent divisors of the 100-MHz REFCLK. 0001b = 100 0010b = 50 0011b = 66 (default; CLKOUT frequency is 66 MHz) 0100b = 25 0101b = 20 0110b = 16.7 0111b = 14.3 1000b = 12.5 1001b = 11.1 1010b = 10 1011b = 9.1 1100b = 8.3 1101b = 7.7 1110b = 7.1 1111b = 6.7	RW	0011b
4	**PCI Express Enable** 0 = Configuration accesses to the PEX 8311 result in a completion status of Configuration Request Retry Status. 1 = PEX 8311 responds normally to PCI Express Configuration accesses. Automatically set when a valid serial EEPROM is not detected.	RW	0
5	**PCI Enable** 0 = PCI accesses to the PEX 8311 result in a Target Retry response. 1 = PEX 8311 responds normally to PCI accesses. Automatically set when a valid serial EEPROM is not detected.	RW	0
31:6	*Reserved*	RsvdP	0h

Register 19-76. Offset 1004h PECS_EECTL Serial EEPROM Control

Bit(s)	Description	Access	Default
7:0	**Serial EEPROM Write Data** Determines the byte written to the serial EEPROM when bit 16 (*Serial EEPROM Byte Write Start*) is set. Represents an opcode, address, or data being written to the serial EEPROM.	RW	0h
15:8	**Serial EEPROM Read Data** Determines the byte read from the serial EEPROM when bit 17 (*Serial EEPROM Byte Read Start*) is set.	RO	–
16	**Serial EEPROM Byte Write Start** 1 = Value in field [7:0] (*Serial EEPROM Write Data*) is written to the serial EEPROM. Automatically cleared when the Write operation is complete.	RW	0
17	**Serial EEPROM Byte Read Start** 1 = Byte is read from the serial EEPROM, and is accessed using field [15:8] (*Serial EEPROM Read Data*). Automatically cleared when the Read operation is complete.	RW	0
18	**Serial EEPROM Chip Select Enable** 1 = Serial EEPROM Chip Select is enabled.	RW	0
19	**Serial EEPROM Busy** 1 = Serial EEPROM Controller is busy performing a Byte Read or Write operation. An interrupt can be generated when this bit goes false.	RO	0
20	**Serial EEPROM Valid** A serial EEPROM with 5Ah in the first byte is detected.	RO	–
21	**Serial EEPROM Present** Set when the Serial EEPROM Controller determines that a serial EEPROM is connected to the PEX 8311.	RO	–
22	**Serial EEPROM Chip Select Active** Set when the EECS# ball to the serial EEPROM is active. The Chip Select can be active across multiple byte operations.	RO	–
24:23	**Serial EEPROM Address Width** Reports the addressing width of the installed serial EEPROM. A non-zero value is reported only when the validation signature (5Ah) is successfully read from the first serial EEPROM location. If there is no serial EEPROM present, or if the first byte read is not a valid signature byte (5Ah), 0 is returned. 00b = Undetermined 01b = 1 byte 10b = 2 bytes 11b = 3 bytes *Note: Programs that reference this value to determine the address width used for Serial EEPROM Writes do not function when a 0 value is read. To program a blank or corrupted serial EEPROM, programs must use either a user-entered or hardwired value.*	RO	–
30:25	*Reserved*	RsvdP	0h
31	**Serial EEPROM Reload** Writing 1 to this bit causes the Serial EEPROM Controller to perform an initialization sequence. Configuration registers and shared memory are loaded from the serial EEPROM. Reading this bit returns 0 while the initialization is in progress, and 1 when initialization is complete.	RW	0

Register 19-77. Offset 1008h PECS_EECLKFREQ Serial EEPROM Clock Frequency

Bit(s)	Description	Access	Default
2:0	**Serial EEPROM Clock Frequency** Controls the EECLK ball frequency. 000b = 2 MHz 001b = 5 MHz 010b = 8.3 MHz 011b = 10 MHz 100b = 12.5 MHz 101b = 16.7 MHz 110b = 25 MHz 111b = *Reserved*	RW	000b
31:3	*Reserved*	RsvdP	0h

Register 19-78. Offset 100Ch PECS_PCICTL PCI Control

Bit(s)	Description	Access	Default
0	**PCI Multi-Level Arbiter** 0 = PCI requesters are placed into a single-level Round-Robin arbiter, each with equal access to the internal PCI Bus 1 = Two-level arbiter is selected	RW	0
3:1	**Internal Arbiter Park Select** Determines which PCI master controller is granted the internal PCI Bus when there are no pending requests. 000b = Last Grantee 001b = PCI Express Interface 010b, 011b = *Reserved* 100b = External Requester 0 101b = External Requester 1 110b = External Requester 2 111b = External Requester 3	RW	000b
4	**Bridge Mode** Reflects the ROOT_COMPLEX# ball status. When Low, the PEX 8311 operates in Root Complex mode (Local-to-PCI Express). When High, the device operates in Endpoint mode (PCI Express-to-Local).	RO	–
5	*Reserved*	RO	0
6	**Locked Transaction Enable** 0 = PCI Express Memory Read Locked requests are completed with UR status, and the internal LOCK# signal is not driven in Endpoint mode In Root Complex mode, the internal LOCK# signal is ignored. When set, Locked transactions are propagated through the PEX 8311, from the Local Bus interface to the PCI Express interface.	RW	0
7	*Reserved*	RO	0
15:8	**Direct Master Configuration Access Retry Count** Specifies PCI Express bridge Retry behavior in response to Direct Master Type 1 Configuration transfers forwarded from the Local Bus bridge. Valid only in Root Complex mode when the PCI Express Link is down. Determines the number of times to Retry a PCI Type 1 Configuration transaction to the PCI Express interface before aborting the transfer (in units of 2^{14} Retries). A value of 0h indicates that the transaction is Retried forever. A value of 255 selects a Retry Count of 2^{24}. When the timer times out, a Target Abort is returned to the Local Bus bridge (**LCS_INTCSR**[24]=1).	RW	80h

Register 19-78. Offset 100Ch PECS_PCICTL PCI Control (Cont.)

Bit(s)	Description	Access	Default
23:16	**PCI Express-to-Local Retry Count** Determines the number of times to Retry a PCI Express-to-Local transaction before aborting the transfer (in units of 2^4 Retries). A value of 0h indicates that the transaction is Retried forever. A value of 255 selects a Retry Count of 2^{24}.	RW	0h
24	**Memory Read Line Enable** 0 = PEX 8311 issues a Memory Read command for transactions that do not start on a Cache boundary. 1 = Memory Read Line command is issued when a transaction is not aligned to a Cache boundary, and the Burst Transfer Size is at least one Cache Line of data. The PCI burst is stopped at the Cache Line boundary when the Burst Transfer Size is less than one Cache Line of data or when a Memory Read Multiple command is started.	RW	1
25	**Memory Read Multiple Enable** 0 = PEX 8311 issues a Memory Read command for transactions that start on a cache boundary. 1 = Memory Read Multiple command is issued when a transaction is aligned to a Cache boundary, and the Burst Transfer Size is at least one Cache Line of data. The PCI burst continues when the Burst Transfer Size remains greater than or equal to one Cache Line of data.	RW	1
26	**Don't Care/No Function** 0 = PEX 8311 accepts the internal PCI Byte Enables that are not valid until the internal IRDY# signal is asserted. 1 = PEX 8311 expects the internal PCI Byte Enables to be valid in the clock tick following the Address phase. For maximum compatibility with non-compliant PCI devices, clear this bit to 0. For maximum performance, set this bit to 1.	RW	0
29:27	**Programmed Prefetch Size** Valid only for Memory Read Line and Memory Read Multiple transactions, or Memory Read transactions with the **PECS_DEVSPECCTL** register *Blind Prefetch Enable* bit set. Determines the number of bytes requested from the PCI Express interface as a result of a PCI-to-PCI Express read. Enable feature only when the PCI initiator reads all requested data without disconnecting. Otherwise, performance is impacted. The Prefetch Size is limited by the **PECS_DEVCTL** register *Maximum Read Request Size* field. 000b = Disabled 001b = 64 bytes 010b = 128 bytes 011b = 256 bytes 100b = 512 bytes 101b = 1,024 bytes 110b = 2,048 bytes 111b = 4,096 bytes (refer to Note) *Note: If the Programmed Prefetch Size is 4 KB, the **PECS_TLPCFG0** register Limit Completion Flow Control Credit bit must be set.*	RW	000b
31:30	***Reserved***	RsvdP	00b

Register 19-79. Offset 1010h PECS_PCIEIRQENB PCI Express Interrupt Request Enable

Bit(s)	Description	Access	Default
Notes:	In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.		
	Assert is issued on the first interrupt only when there is more than one interrupt pending. De-assert is issued only as the last pending interrupt is cleared.		
0	**Serial EEPROM Done Interrupt Enable** 0 = Generates a Deassert_IntA message to PCI Express Space when a serial EEPROM Read or Write transaction completes, if no other interrupts are pending 1 = Generates an Assert_IntA message to PCI Express Space when a serial EEPROM Read or Write transaction completes, if no other interrupts are pending	RW	0
1	**GPIO Interrupt Enable** 0 = Generates a Deassert_IntA message to PCI Express Space when a GPIO ball interrupt is active, if no other interrupts are pending 1 = Generates an Assert_IntA message to PCI Express Space when a GPIO ball interrupt is active, if no other interrupts are pending	RW	0
2	*Reserved*	RsvdP	0
3	**PCI Express-to-Local Retry Interrupt Enable** 0 = Generates a Deassert_IntA message to PCI Express Space when the PCI Express-to-Local Retry Count Interrupt is reached, if no other interrupts are pending 1 = Generates an Assert_IntA message to PCI Express Space when the PCI Express-to-Local Retry Count Interrupt is reached, if no other interrupts are pending	RW	0
4	**Mailbox 0 Interrupt Enable** 0 = Generates a Deassert_IntA message to PCI Express Space when Mailbox 0 is written, if no other interrupts are pending 1 = Generates an Assert_IntA message to PCI Express Space when Mailbox 0 is written, if no other interrupts are pending	RW	0
5	**Mailbox 1 Interrupt Enable** 0 = Generates a Deassert_IntA message to PCI Express Space when Mailbox 1 is written, if no other interrupts are pending 1 = Generates an Assert_IntA message to PCI Express Space when Mailbox 1 is written, if no other interrupts are pending	RW	0
6	**Mailbox 2 Interrupt Enable** 0 = Generates a Deassert_IntA message to PCI Express Space when Mailbox 2 is written, if no other interrupts are pending 1 = Generates an Assert_IntA message to PCI Express Space when Mailbox 2 is written, if no other interrupts are pending	RW	0
7	**Mailbox 3 Interrupt Enable** 0 = Generates a Deassert_IntA message to PCI Express Space when Mailbox 3 is written, if no other interrupts are pending 1 = Generates an Assert_IntA message to PCI Express Space when Mailbox 3 is written, if no other interrupts are pending	RW	0
30:8	*Reserved*	RsvdP	0h
31	**PCI Express Internal Interrupt Enable** 0 = Generates a Deassert_IntA message to PCI Express Space as a result of an internal PEX 8311 interrupt source, if no other interrupts are pending. The internal interrupt is serviced as either a Message Signaled Interrupt (MSI) or Virtual Wire interrupt. 1 = Generates an Assert_IntA message to PCI Express Space as a result of an internal PEX 8311 interrupt source, if no other interrupts are pending. The internal interrupt is serviced as either a Message Signaled Interrupt (MSI) or Virtual Wire interrupt.	RW	1 (E) 0 (RC)

Register 19-80. Offset 1014h PECS_PCIIRQENB PCI Interrupt Request Enable

Bit(s)	Description	Access	Default
Note:	*In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*		
0	**Serial EEPROM Done Interrupt Enable** 1 = Enables a PCI interrupt to generate when a serial EEPROM Read or Write transaction completes	RW	0
1	**GPIO Interrupt Enable** 1 = Enables a PCI interrupt to generate when an interrupt is active from one of the GPIO balls	RW	0
2	*Reserved*	RsvdP	0
3	**PCI Express-to-Local Retry Interrupt Enable** 1 = Enables a PCI interrupt to generate when the PCI Express-to-Local Retry Count is reached	RW	0
4	**Mailbox 0 Interrupt Enable** 1 = Enables a PCI interrupt to generate when Mailbox 0 is written	RW	0
5	**Mailbox 1 Interrupt Enable** 1 = Enables a PCI interrupt to generate when Mailbox 1 is written	RW	0
6	**Mailbox 2 Interrupt Enable** 1 = Enables a PCI interrupt to generate when Mailbox 2 is written	RW	0
7	**Mailbox 3 Interrupt Enable** 1 = Enables a PCI interrupt to generate when Mailbox 3 is written	RW	0
8	**Unsupported Request Interrupt Enable** 1 = Enables a PCI interrupt to generate when an Unsupported Request Completion response is received from the PCI Express interface	RW	0
30:9	*Reserved*	RsvdP	0h
31	**PCI Internal Interrupt Enable** 1 = Enables a PCI interrupt to generate as a result of an internal PEX 8311 interrupt source	RW	0 (E) 1 (RC)

Register 19-81. Offset 1018h PECS_IRQSTAT Interrupt Request Status

Bit(s)	Description	Access	Default
0	**Serial EEPROM Done Interrupt** 1 = Serial EEPROM Read or Write transaction completed. Writing 1 clears this bit.	RW1C	0
1	**GPIO Interrupt** Conveys the interrupt status for the GPIO[3:0] balls. 1 = **PECS_GPIOSTAT** register is read, to determine the cause of the interrupt. Set independently of the *Interrupt Enable* bit (PECS_PCIEIRQENB[1]).	RO	0
2	*Reserved*	RsvdP	0
3	**PCI Express-to-Local Retry Interrupt** Set when the PCI Express-to-PCI Retry count is reached. Writing 1 clears this status bit.	RW1C	0
4	**Mailbox 0 Interrupt** Set when Mailbox 0 is written. Writing 1 clears this bit.	RW1C	0
5	**Mailbox 1 Interrupt** Set when Mailbox 1 is written. Writing 1 clears this bit.	RW1C	0
6	**Mailbox 2 Interrupt** Set when Mailbox 2 is written. Writing 1 clears this bit.	RW1C	0
7	**Mailbox 3 Interrupt** Set when Mailbox 3 is written. Writing 1 clears this bit.	RW1C	0
8	**Unsupported Request Interrupt** Set when an Unsupported Request Completion is received from the PCI Express interface.	RW1C	0
31:9	*Reserved*	RsvdZ	0h

Register 19-82. Offset 101Ch PECS_POWER Power (Endpoint Mode Only)

Bit(s)	Description	Access	Default
7:0	**Power Compare 0** Specifies the power required for the PEX 8311 and downstream PCI devices in Endpoint mode. It is compared with the **PECS_DEVCAP** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the *Captured Slot Power Limit Scale* field is 00b (scale = 1.0x).	RW	0h
15:8	**Power Compare 1** Specifies the power required for the PEX 8311 and downstream PCI devices in Endpoint mode. It is compared with the **PECS_DEVCAP** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the *Captured Slot Power Limit Scale* field is 01b (scale = 0.1x).	RW	0h
23:16	**Power Compare 2** Specifies the power required for the PEX 8311 and downstream PCI devices in Endpoint mode. It is compared with the **PECS_DEVCAP** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the *Captured Slot Power Limit Scale* field is 10b (scale = 0.01x).	RW	0h
31:24	**Power Compare 3** Specifies the power required for the PEX 8311 and downstream PCI devices in Endpoint mode. It is compared with the **PECS_DEVCAP** register *Captured Slot Power Limit Value* field. When the *Captured Slot Power Limit Value* is greater than or equal to this field, the PWR_OK signal is asserted. Used when the *Captured Slot Power Limit Scale* field is 11b (scale = 0.001x).	RW	0h

Register 19-83. Offset 1020h PECS_GPIOCTL General-Purpose I/O Control

Bit(s)	Description	Access	Default
0	**GPIO0 Data** When programmed as an output, values written to this bit appear on the GPIO0 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO0 ball.	RW	0
1	**GPIO1 Data** When programmed as an output, values written to this bit appear on the GPIO1 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO1 ball.	RW	0
2	**GPIO2 Data** When programmed as an output, values written to this bit appear on the GPIO2 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO2 ball.	RW	0
3	**GPIO3 Data** When programmed as an output, values written to this bit appear on the GPIO3 ball. Reading this bit returns the value that was previously written. When programmed as an input, reading this bit returns the value present on the GPIO3 ball.	RW	0
4	**GPIO0 Output Enable** 0 = GPIO0 ball is an input 1 = GPIO0 ball is an output Field [13:12] (*GPIO Diagnostic Select*) overrides this bit when a diagnostic output is selected.	RW	1
5	**GPIO1 Output Enable** 0 = GPIO1 ball is an input 1 = GPIO1 ball is an output Field [13:12] (*GPIO Diagnostic Select*) overrides this bit when a diagnostic output is selected.	RW	0
6	**GPIO2 Output Enable** 0 = GPIO2 ball is an input 1 = GPIO2 ball is an output Field [13:12] (*GPIO Diagnostic Select*) overrides this bit when a diagnostic output is selected.	RW	0
7	**GPIO3 Output Enable** 0 = GPIO3 ball is an input 1 = GPIO3 ball is an output Field [13:12] (*GPIO Diagnostic Select*) overrides this bit when a diagnostic output is selected.	RW	0
8	**GPIO0 Interrupt Enable** 1 = Changes on the GPIO0 ball (when programmed as an input) are enabled to generate an interrupt	RW	0
9	**GPIO1 Interrupt Enable** 1 = Changes on the GPIO1 ball (when programmed as an input) are enabled to generate an interrupt	RW	0
10	**GPIO2 Interrupt Enable** 1 = Changes on the GPIO2 ball (when programmed as an input) are enabled to generate an interrupt	RW	0
11	**GPIO3 Interrupt Enable** 1 = Changes on the GPIO3 ball (when programmed as an input) are enabled to generate an interrupt	RW	0

Register 19-83. Offset 1020h PECS_GPIOCTL General-Purpose I/O Control (Cont.)

Bit(s)	Description	Access	Default
13:12	**GPIO Diagnostic Select** Selects diagnostic signals that are output on the GPIO balls. 00b = Normal GPIO operation 01b = GPIO0 driven High when Link is up. GPIO[3:1] operate normally 10b = GPIO[3:0] are driven with the lower four bits of the LTSSM state machine for 2s, alternating with GPIO[1:0] driven with the upper two bits of the LTSSM state machine for 1s 11b = GPIO[3:0] driven with PMU Linkstate (L2, L1, L0s, and L0) **LTSSM Codes** 00h – L3_L2 (Fundamental Reset) 01h – Detect 02h – Polling.Active 03h – Polling.Configuration 04h – Polling.Compliance 05h – Configuration.Linkwidth.Start & Accept (Root Complex mode) 06h – Configuration.Lanenum.Wait & Accept (Root Complex mode) 07h – Configuration.Complete (Root Complex mode) 08h – Configuration.Idle (Root Complex mode) 09h – Configuration.Linkwidth.Start (Endpoint mode) 0Ah – Configuration.Linkwidth.Accept (Endpoint mode) 0Bh – Configuration.Lanenum.Wait & Accept (Endpoint mode) 0Ch – Configuration.Complete (Endpoint mode) 0Dh – Configuration.Idle (Endpoint mode) 0Eh – L0 0Fh – L0 (Transmit E.I.Ordered-set) 10h – L0 (Wait E.I.Ordered-set) 12h – L1.Idle 14h – L2.Idle 15h – Recovery.Rcvrlock (Extended Sync enabled) 16h – Recovery.Rcvrlock 17h – Recovery.RcvrCfg 18h – Recovery.Idle 19h – Disabled (Transmit TS1) 1Ah – Disabled (Transmit E.I.Ordered-set) 1Dh – Disabled (Wait Electrical Idle) 1Eh – Disabled (Disable) 1Fh – Loopback.Entry 20h – Loopback.Active 21h – Loopback.Exit 22h – Hot Reset (Wait TS1 with Hot Reset, Root Complex mode) 23h – Hot Reset (Reset Active) 24h – Loopback.Actice (Transmit E.I.Ordered-set) 25h – Loopback.Active (Wait Electrical Idle)	RW	01b
31:14	*Reserved*	RsvdP	0h

Register 19-84. Offset 1024h PECS_GPIOSTAT General-Purpose I/O Status

Bit(s)	Description	Access	Default
0	**GPIO0 Interrupt** Set when the state of the GPIO0 ball changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
1	**GPIO1 Interrupt** Set when the state of the GPIO1 ball changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
2	**GPIO2 Interrupt** Set when the state of the GPIO2 ball changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
3	**GPIO3 Interrupt** Set when the state of the GPIO3 ball changes and the ball is programmed as an input. Writing 1 clears this bit.	RW1C	0
31:4	*Reserved*	RsvdZ	0h

Register 19-85. Offset 1030h PECS_MAILBOX0 Mailbox 0

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or Local Bus. Interrupts are generated to either interface when this register is written.	RW	FEED_FACEh

Register 19-86. Offset 1034h PECS_MAILBOX1 Mailbox 1

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or Local Bus. Interrupts are generated to either interface when this register is written.	RW	0h

Register 19-87. Offset 1038h PECS_MAILBOX2 Mailbox 2

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or Local Bus. Interrupts are generated to either interface when this register is written.	RW	0h

Register 19-88. Offset 103Ch PECS_MAILBOX3 Mailbox 3

Bit(s)	Description	Access	Default
31:0	**Mailbox Data** Written or read from the PCI Express interface or Local Bus. Interrupts are generated to either interface when this register is written.	RW	0h

Register 19-89. Offset 1040h PECS_CHIPREV Chip Silicon Revision

Bit(s)	Description	Access	Default
Note:	*This register is the silicon revision, encoded as a 4-digit BCD value. For the first release of the bridge (Rev. AA), the register's value is 0201h. The least-significant digit is incremented for mask changes, and the most-significant digit is incremented for major revisions.*		
15:0	**Chip Revision** Returns the current PEX 8311 silicon revision number.	RO	0201h
31:16	*Reserved*	RsvdP	0h

Register 19-90. Offset 1044h PECS_DIAG Diagnostic Control *(Factory Test Only)*

Bit(s)	Description	Access	Default
0	**Fast Times** 1 = Internal timers and counters operate at a fast speed for factory testing	RW	0
1	**Force PCI Interrupt** 1 = Forces the PCI INTA# interrupt signal to assert. Effective only when the **PECS_PCICMD** register *Interrupt Disable* bit is Low.	RW	0
2	**Force Internal SERR#** 1 = Forces the internal SERR# interrupt signal to assert when the **PECS_PCICMD** register *Internal SERR# Enable* bit is set (Root Complex mode). In Endpoint mode, the **PECS_BRIDGECTL** register *Secondary Internal SERR# Enable* bit must be set.	RW	0
3	**Force PCI Express Interrupt** 1 = Forces an interrupt to the PCI Express Root Complex using Message Signaled Interrupts (MSI) or virtual wire INTA# interrupts	RW	0
31:4	*Reserved*	RsvdP	0h

Register 19-91. Offset 1048h PECS_TLPCFG0 TLP Controller Configuration 0

Bit(s)	Description	Access	Default
Note:	*In the **Default** column, "E" indicates Endpoint mode, and "RC" indicates Root Complex mode.*		
7:0	**CFG_NUM_FTS** Forced NUM_FTS signal. [*NUM_FTS* is the number of Fast Training sequence (0 to 255).] For detailed information, refer to the *PCI Express Base 1.0a*, Section 4.2.4.3.	RW	20h
8	**CFG_ACK_FMODE** PCI Express core ACK_DLLP transmitting interval mode. 0 = Core hardware uses own interval value 1 = Core hardware uses *CFG_ACK_COUNT* as interval value	RW	0
9	**CFG_TO_FMODE** PCI Express core Timeout detection mode for the Replay Timer. 0 = Core hardware uses own timer value 1 = Core hardware uses *CFG_TO_COUNT* as timer value	RW	0
10	**CFG_PORT_DISABLE** 1 = PCI Express interface is disabled. This allows the endpoint to disable the PCI Express connection when powered up or before the configuration is complete.	RW	0
11	**CFG_RCV_DETECT** Asserted when the PCI Express core establishes the PCI Express connection.	RO	0
12	**CFG_LPB_MODE** Link Loop-Back mode.	RW	0
13	**CFG_PORT_MODE** 0 = Link core is configured as an upstream port (Endpoint mode) 1 = Link core is configured as a downstream port (Root Complex mode)	RW	0 (E) 1 (RC)
14	*Reserved*	RsvdP	0
15	**CFG_ECRC_GEN_ENABLE** *Not supported* 1 = Link is allowed generate End-to-end Cyclic Redundancy Check (ECRC). The PEX 8311 does ***not support*** ECRC; therefore, clear this bit to 0.	RW	0

Register 19-91. Offset 1048h PECS_TLPCFG0 TLP Controller Configuration 0 (Cont.)

Bit(s)	Description	Access	Default
16	**TLB_CPLD_NOSUCCESS_MALFORM_ENABLE** 0 = Received completion is retained 1 = Completion received when completion timeout expired is treated as a malformed TLB and is discarded	RW	1
17	**Scrambler Disable** 0 = Data scrambling is enabled. 1 = Data scrambling is disabled. Only set for testing and debugging.	RW	0
18	**Delay Link Training** 0 = Link training is allowed to commence immediately after reset is de-asserted. 1 = Link training is delayed for 12 ms after reset is de-asserted. Automatically set when GPIO3 is Low during reset.	RW	0
19	**Decode Primary Bus Number** 0 = PEX 8311 ignores the Primary Bus Number in a PCI Express Type 0 Configuration Request. 1 = PEX 8311 compares the Primary Bus Number in a PCI Express Type 0 Configuration request with the **PECS_PRIMBUSNUM** register. When they match, the request is accepted. Otherwise, an Unsupported Request is returned. This comparison occurs only after the first Type 0 Configuration Write occurs.	RW	0
20	**Ignore Function Number** 0 = PEX 8311 only responds to Function Number 0 during a Type 0 Configuration transaction. Accesses to other function numbers result in an Unsupported Request (PCI Express) or Master Abort (PCI). 1 = PEX 8311 ignores the Function Number in a PCI or PCI Express Type 0 Configuration Request, and responds to all eight functions.	RW	0
21	**Check RCB Boundary** 0 = PEX 8311 ignores Read Completion Boundary (RCB) violations. 1 = PEX 8311 checks for RCB violations. When detected, the PEX 8311 treats it as a malformed TLP (packet is dropped and a Non-Fatal Error message is transmitted).	RW	0
22	**Limit Completion Flow Control Credit** 0 = PEX 8311 advertises infinite flow control credits for completions. 1 = PEX 8311 advertises completion flow control credits, based on available FIFO storage. This bit must be set when the **PECS_PCICTL** register *Programmed Prefetch Size* field is set to 4 KB. When GPIO2 is Low during reset, this bit is automatically set. Because this bit is used during Link training, it must be set by driving GPIO2 Low during reset.	RW	0
23	**L2 Secondary Bus Reset** When ROOT_COMPLEX# is strapped Low, the PEX 8311 is in the L2/L3 Ready state, and a Direct Master Configuration access to PCI Express Space is Retried until the L2PE_RETRY_COUNT expires, this bit selects one of two possible responses: • When cleared, the PEX 8311 responds by generating an LTSSM Hot Reset training sequence on the PCI Express interface • When set, the PEX 8311 responds with a Master Abort, which if enabled, is returned to the Local host by way of LSERR# (C or J mode) or LINTo# (M mode)	RW	1
31:24	*Reserved*	RsvdP	0h

Register 19-92. Offset 104Ch PECS_TLPCFG1 TLP Controller Configuration 1

Bit(s)	Description	Access	Default
20:0	**CFG_TO_COUNT** PCI Express core replay timer timeout value when *CFG_TO_FMODE* is set to 1.	RW	D4h
30:21	**CFG_ACK_COUNT** PCI Express core ACK DLLP transmitting interval value when *CFG_ACK_FMODE* is set to 1.	RW	0h
31	*Reserved*	RsvdP	0

Register 19-93. Offset 1050h PECS_TLPCFG2 TLP Controller Configuration 2

Bit(s)	Description	Access	Default
15:0	**CFG_COMPLETER_ID0** Bits [15:8] – Bus number Bits [7:3] – Device number Bits [2:0] – Function number When TLB0_TRANS is asserted with a Type 0 Configuration Cycle, this signal latches CFG_TLB0_BUS_NUMBER[7:0] and CFG_TLB0_DEV_NUMBER[4:0] into the corresponding bits.	RW	0h
26:16	**Update Credit FC** Controls a counter that determines the gap between UpdateFC DLLPs (in units of 62.5 MHz clocks = 16 ns = 4 symbol times). When data or headers are read from the TLP Controller, the Credit Allocation Manager transmits a set of UpdateFC DLLPs; posted, non-posted, and completion when the **PECS_TLPCFG0** register *Limit Completion Flow Control Credit* bit is set. While transmitting the set of DLLPs, the Credit Allocation Manager uses the counter value to insert gaps between the DLLPs.	RW	1h
31:27	*Reserved*	RsvdP	0h

Register 19-94. Offset 1054h PECS_TLPTAG TLP Controller Tag

Bit(s)	Description	Access	Default
7:0	**TAG BME1** Message Request *Tag* field.	RW	0h
15:8	**TAG ERM** Error Manager *Tag* field.	RW	0h
23:16	**TAG PME** Power Manager *Tag* field.	RW	0h
31:24	*Reserved*	RsvdP	0h

Register 19-95. Offset 1058h PECS_TLPTIMELIMIT0 TLP Controller Time Limit 0

Bit(s)	Description	Access	Default
23:0	**BME_COMPLETION_TIMEOUT_LIMIT** Bus master engine completion timeout (in units of internal clocks). The default value produces a 10-ms timeout.	RW	A2C2Ah
27:24	**L2L3_PWR_REMOVAL_TIME_LIMIT** This value determines the amount of time before power is removed after entering the L2 state (in units of internal clocks). Enter this value as at least 100 ns.	RW	8h
31:28	*Reserved*	RsvdP	0h

Register 19-96. Offset 105Ch PECS_TLPTIMELIMIT1 TLP Controller Time Limit 1

Bit(s)	Description	Access	Default
10:0	**ASPM_LI_DLLP_INTERVAL_TIME_LIMIT** Determines the time interval between two consecutive PM_ACTIVE_STATE_REQUEST_L1 DLLP transmissions (in units of internal clocks). Allow at least 10 μs spent in LTSSM L0 and L0s state before the next PM_ACTIVE_STATE_REQUEST_L1 DLLP is transmitted. Detailed information is in the *PCI Express Base 1.0a Errata*, page 19.	RW	29Ah
31:11	*Reserved*	RsvdP	0h

Register 19-97. Offset 1060h PECS_CRSTIMER CRS Timer

Bit(s)	Description	Access	Default
15:0	**CRS Timer** Valid only in Endpoint mode when the **PECS_DEVCTL** register *Bridge Configuration Retry Enable* bit is set. Determines the amount of microseconds to wait before returning a completion with CRS status in response to a PCI Express-to-PCI Configuration transaction. When the timer times out and the completion with CRS status is returned, the transaction is discarded from the Non-Posted Transaction queue.	RW	25d
31:16	*Reserved*	RsvdP	0h

Register 19-98. Offset 1064h PECS_ECFGADDR Enhanced Configuration Address

Bit(s)	Description	Access	Default
11:0	*Reserved*	RsvdP	0h
14:12	**Configuration Function Number** Provides the Function Number for an enhanced Configuration transaction.	RW	000b
19:15	**Configuration Device Number** Provides the Device Number for an enhanced Configuration transaction.	RW	0h
27:20	**Configuration Bus Number** Provides the Bus Number for an enhanced Configuration transaction.	RW	0h
30:28	*Reserved*	RsvdP	0h
31	**Enhanced Configuration Enable** Used only in Root Complex mode. 0 = Accesses to the **Base Address 0** register, offset 2000h, are not responded to by the PEX 8311 1 = Accesses to the **Base Address 0** register, offset 2000h, are forwarded to the PCI Express interface as a Configuration request	RW	0

Chapter 20 Local Configuration Space Registers

20.1 Introduction

This chapter describes the Local Configuration Space (**LCS**) register set. PCI Express Configuration Space (**PECS**) registers are described in Chapter 19, "PCI Express Configuration Registers."

20.2 Register Description

The **LCS PCI** registers are accessed from the PCI Express interface, using Type 1 Configuration accesses (PCI Express Type 1 accesses are internally converted to Type 0). The remainder of the **LCS Local**, **Runtime**, **DMA**, and **Messaging Queue** registers are accessed from the PCI Express interface, using Memory- or I/O-Mapped accesses through the **LCS_PCIBAR0** or **LCS_PCIBAR1** registers, respectively. **LCS** registers are accessed directly by the Local Bus Master in Endpoint or Root Complex mode, by way of CCS# register Read/Write transactions.

In Root Complex mode, a Local Bus Master cannot access the **PCI Express Extended Capability** registers by way of PCI Configuration transactions. To access the **PCI Express Extended Capability** registers, use the method detailed in Section 10.7.1, "Memory-Mapped Indirect – Root Complex Mode Only."

20.3   PEX 8311 Local Configuration Space

20.3.1   Local Configuration Space Access

The PEX 8311 **LCS** internal registers provide maximum flexibility in bus-interface control and performance. These registers are accessible from the PCI Express interface and Local Bus (refer to Figure 20-1) and include the following:

- PCI Configuration
- Local Configuration
- DMA
- Mailbox
- PCI Express-to-Local and Local-to-PCI Express Doorbell
- Messaging Queue (I_2O)
- Power Management
- Hot Swap (***Reserved***)
- VPD

Figure 20-1.   PEX 8311 Internal Local Configuration Space Register Accesses
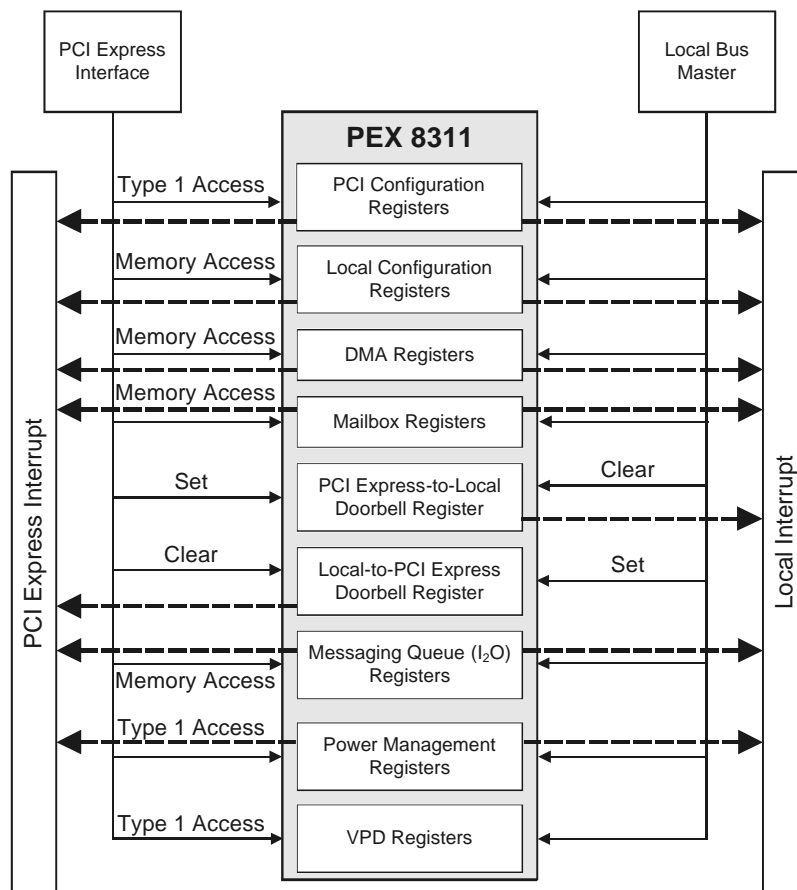
20.3.2   New Capabilities Function Support

The New Capabilities Function Support includes PCI Power Management, Hot Swap, and VPD features, as defined in Table 20-1.

*Note: Although the PEX 8311 provides **Hot Swap** Configuration registers, the Hot Swap feature is **not supported**.*

When a New Capabilities Function is not used and passed over in the Capability Pointer's Linked List, the unused New Capabilities Function registers are set to default values.

Table 20-1.   New Capabilities Function Support Features in Local Configuration Space PCI Registers

New Capability Function	PCI Register Offset Location
First (Power Management)	40h, when the New Capabilities Function Support bit is enabled (**LCS_PCISR**[4]=1; default). (Refer to Chapter 14, "Power Management," for details.)
Second (Hot Swap)	48h, which is pointed to from **LCS_PMNEXT**[7:0].
Third (VPD)	4Ch, which is pointed to from **LCS_HS_NEXT**[7:0]. Because **LCS_PVPD_NEXT**[7:0] defaults to 0h, this indicates that VPD is the last New Capability Function Support feature of the PEX 8311. [Refer to Chapter 17, "Vital Product Data (VPD)," for details.]

20.3.3   Local Bus Access to Local Configuration Space Registers

The Local Bus Master can access PEX 8311 **LCS** registers through an external Chip Select. The PEX 8311 responds to a Local Bus access when the PEX 8311 Configuration Chip Select input (CCS#) is asserted Low during the Address phase.

Local Read or Write accesses to the PEX 8311 internal registers must be DWord accesses. Local accesses to the PEX 8311 internal registers are Burst or Non-Burst accesses.

The READY# signal indicates that the Data transfer is complete.

Using a Local CPU to perform accesses to the PEX 8311 Configuration registers, these accesses must be 32-bit, with LBE[3:0]# asserted.

20.4 PCI Configuration Registers

This section details the **LCS** PCI Configuration registers. Table 20-2 defines the register map.

Notes: *All registers can be written to or read from in Byte, Word, or Dword accesses.*

"Yes" in the register Read and Write columns indicates the register is writable by the PCI Express interface and Local Bus.

Table 20-2. PCI Configuration Register Map

PCI Configuration Register Address	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits.					PCI/Local Writable	Serial EEPROM Writable
		31 30 24	23 16	15 8	7 0			
00h	00h	Device ID		Vendor ID			Local	Yes
04h	04h	PCI Status		PCI Command			Yes	No
08h	08h	PCI Class Code			PCI Revision ID		Local	Yes
0Ch	0Ch	PCI Built-In Self-Test (BIST)	PCI Header Type	Internal PCI Bus Latency Timer	PCI Cache Line Size		Yes	No
10h	10h	PCI Express Base Address for Memory Accesses to Local, Runtime, DMA, and Messaging Queue Registers (**LCS_PCIBAR0**)					Yes	No
14h	14h	PCI Express Base Address for I/O Accesses to Local, Runtime, DMA, and Messaging Queue Registers (**LCS_PCIBAR1**)					Yes	No
18h	18h	PCI Express Base Address for Accesses to Local Address Space 0 (**LCS_PCIBAR2**)					Yes	No
1Ch	1Ch	PCI Express Base Address for Accesses to Local Address Space 1 (**LCS_PCIBAR3**)					Yes	No
20h	20h	PCI Express Base Address 4 (*Reserved*)					No	No
24h	24h	PCI Express Base Address 5 (*Reserved*)					No	No
28h	28h	PCI Cardbus Information Structure Pointer (*Not Supported*)					No	No
2Ch	2Ch	PCI Subsystem ID		PCI Subsystem Vendor ID			Local	Yes
30h	30h	PCI Express Base Address for Local Expansion ROM					Yes	No
34h	34h	Reserved			New Capability Pointer		Local	No
38h	38h	*Reserved*					No	No
3Ch	3Ch	PCI Maximum Latency	PCI Minimum Grant	Internal PCI Wire Interrupt	Internal PCI Interrupt Line		Yes	Yes
40h	180h	Power Management Capabilities		Power Management Next Capability Pointer	Power Management Capability ID		Local [31:21, 19:8]	Yes [31:25, 18:16]
44h	184h	Power Management Data	PMCSR Bridge Support Extensions (*Reserved*)	Power Management Control/ Status			PCI [15, 12:8, 1:0], Local [31:24, 15:8, 1:0]	Yes [31:24, 14:8]

Table 20-2.   PCI Configuration Register Map (Cont.)

PCI Configuration Register Address	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits.					PCI/Local Writable	Serial EEPROM Writable
		31 30 24	**23 16**	**15 8**	**7 0**			
48h	188h	*Reserved*	Hot Swap Control/Status (Not Supported)	Hot Swap Next Capability Pointer	Hot Swap Control (Not Supported) (Capability ID)		PCI [23:22, 19, 17], Local [23:22, 17, 15:0]	Yes [15:0]
4Ch	18Ch	F PCI Vital Product Data Address		PCI Vital Product Data Next Capability Pointer	PCI Vital Product Identification (Capability ID)		PCI [31:16], Local [31:8]	No
50h	190h	PCI VPD Data					Yes	No

Notes: *Refer to the PCI r2.2 for definitions of the registers defined in this table.*

   Where Writable bit numbers are not listed, refer to the individual register descriptions to determine which bits are writable.

Register 20-1. PCI:00h, LOC:00h LCS_PCIIDR PCI Configuration ID

Bit(s)	Description	Read	Write	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PLX PCI-SIG-assigned Vendor ID, 10B5h, when the serial EEPROM is blank, or no serial EEPROM is present.	Yes	Local/ Serial EEPROM	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to 9056h when the serial EEPROM is blank, or no serial EEPROM is present.	Yes	Local/ Serial EEPROM	9056h

Register 20-2. PCI:04h, LOC:04h LCS_PCICR PCI Command

Bit(s)	Description	Read	Write	Default
0	**I/O Space** Writing 0 disables the PEX 8311 from responding to I/O Space accesses. Writing 1 allows the PEX 8311 to respond to I/O Space accesses.	Yes	Yes	0
1	**Memory Space** Writing 0 disables the PEX 8311 from responding to Memory Space accesses. Writing 1 allows the PEX 8311 to respond to Memory Space accesses.	Yes	Yes	0
2	**Master Enable** Writing 0 disables the PEX 8311 from generating Bus Master accesses. Writing 1 allows the PEX 8311 to behave as a Bus Master.	Yes	Yes	0
3	**Special Cycle** *Not supported*	Yes	No	0
4	**Memory Write and Invalidate Enable** Writing 1 enables Memory Write and Invalidate mode for Direct Master and DMA. *Note: Refer to* **LCS_DMPBAM***[9] for Direct Master,* *and* **LCS_DMAMODE0/1***[13] for DMA.*	Yes	Yes	0
5	**VGA Palette Snoop** *Not supported*	Yes	No	0
6	**Parity Error Response** Writing 0 disables internal PERR# from being asserted when a Parity error is detected. Writing 1 enables internal PERR# to assert when a Parity error is detected. Parity error status is reported in **LCS_PCISR**[15], regardless of this bit's value.	Yes	Yes	0
7	**Stepping Control** Controls whether the PEX 8311 does address/data stepping. Writing 0 indicates the PEX 8311 never does stepping. Writing 1 indicates the PEX 8311 always does stepping. *Note: Hardwired to 0.*	Yes	No	0
8	**Internal SERR# Enable** Writing 0 disables the internal SERR# driver. Writing 1 enables the internal SERR# driver.	Yes	Yes	0
9	**Fast Back-to-Back Enable** Indicates what type of fast back-to-back transfers a Master can perform on the bus. Writing 0 indicates Fast Back-to-Back transfers can occur only to the same agent as in the previous cycle. Writing 1 indicates Fast Back-to-Back transfers can occur to any agent on the bus. *Note: Hardwired to 0.*	Yes	No	0
15:10	*Reserved*	Yes	No	0h

Register 20-3. PCI:06h, LOC:06h LCS_PCISR PCI Status

Bit(s)	Description	Read	Write	Default
3:0	*Reserved*	Yes	No	0h
4	**New Capability Functions Support** Writing 1 supports New Capabilities Functions. When enabled, the first New Capability Function ID is located at the PCI Configuration Space offset determined by the New Capabilities Linked List pointer value at offset 34h. Can be written only from the Local Bus. Read-Only from the internal PCI Bus.	Yes	Local	1
5	**66 MHz Capable** 1 = PEX 8311 supports a 66-MHz internal clock environment	Yes	Local	1
6	*Reserved*	Yes	No	0
7	**Fast Back-to-Back Capable** Writing 1 indicates an adapter can accept Fast Back-to-Back transactions. *Note:* *Hardwired to 1.*	Yes	No	1
8	**Master Data Parity Error** Set to 1 when the following three conditions are met: • Internal PERR# is asserted; • PEX 8311 was the internal PCI Bus Master for an operation in which the error occurred; and • **PCI Command** register *Parity Error Response* bit is set (**LCS_PCICR**[6]=1). Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
10:9	**DEVSEL Timing** *Note:* *Hardwired to 01b.*	Yes	No	01b
11	**Signaled Target Abort** 1 = Indicates PEX 8311 signaled an internal Target Abort. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
12	**Received Target Abort** 1 = Indicates the PEX 8311 received an internal Target Abort signal. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
13	**Received Master Abort** 1 = Indicates the PEX 8311 received an internal Master Abort signal. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
14	**Signaled System Error (Internal SERR# Status)** 1 = Indicates the PEX 8311 reported an internal System error on internal SERR#. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
15	**Detected Parity Error** 1 = Indicates the PEX 8311 has detected an internal PCI Bus Parity error internally, regardless of whether Parity error handling is disabled [**PCI Command** register *Parity Error Response* bit is cleared (**LCS_PCICR**[6]=0)]. One of three conditions can cause this bit to be set when the PEX 8311 detects a Parity error during: • PCI Express Address phase • PCI Data phase when the PEX 8311 is the Target of a Write • Direct Master or DMA Read operation Writing 1 clears this bit to 0.	Yes	Yes/Clr	0

Register 20-4. PCI:08h, LOC:08h LCS_PCIREV PCI Revision ID

Bit(s)	Description	Read	Write	Default
7:0	**Revision ID** Silicon Revision of the PEX 8311 Local Bus logic.	Yes	Local/ Serial EEPROM	BAh

Register 20-5. PCI:09h - 0Bh, LOC:09h - 0Bh LCS_PCICCR PCI Class Code

Bit(s)	Description	Read	Write	Default
7:0	**Register Level Programming Interface** None defined.	Yes	Local/ Serial EEPROM	00h
15:8	**Sub-class Code (Other Bridge Device)**	Yes	Local/ Serial EEPROM	80h
23:16	**Base Class Code (Bridge Device)**	Yes	Local/ Serial EEPROM	06h

Register 20-6. PCI:0Ch, LOC:0Ch LCS_PCICLSR PCI Cache Line Size

Bit(s)	Description	Read	Write	Default
7:0	**System Cache Line Size** Specifies (in units of 32-bit words – 8 or 16 Dwords) the System Cache Line Size. When a size other than 8 or 16 is specified, the PEX 8311 performs Write transfers rather than Memory Write and Invalidate transfers.	Yes	Yes	0h

Register 20-7. PCI:0Dh, LOC:0Dh LCS_PCILTR Internal PCI Bus Latency Timer

Bit(s)	Description	Read	Write	Default
7:0	**Internal PCI Bus Latency Timer** Specifies length of time (in units of internal PCI Bus clocks) the PEX 8311, as a Bus Master, can burst data on the internal PCI Bus.	Yes	Yes	0h

Register 20-8. PCI:0Eh, LOC:0Eh LCS_PCIHTR PCI Header Type

Bit(s)	Description	Read	Write	Default
6:0	**Configuration Layout Type** Specifies layout of registers 10h through 3Fh in **LCS PCI-compatible** Configuration register space. Header Type 0 is defined for all PCI devices other than PCI-to-PCI bridges (Header Type 1) and Cardbus bridges (Header Type 2). Leave cleared for most applications.	Yes	Local	0h
7	**Multi-Function Device** *Not supported. Local processors should never write 1 to this bit.* 1 = Indicates multiple (up to eight) functions (logical devices) each containing its own, individually addressable Configuration space, 64 Dwords in size	Yes	Local	0

Register 20-9. PCI:0Fh, LOC:0Fh LCS_PCIBISTR PCI Built-In Self-Test (BIST)

Bit(s)	Description	Read	Write	Default
3:0	**Built-In Self-Test Pass/Fail** Writing 0h indicates the PEX 8311 passed its test. Non-0h values indicate the PEX 8311 failed its test. Device-specific failure codes are encoded in a non-0h value.	Yes	Local	0h
5:4	*Reserved*	Yes	No	00b
6	**PCI Built-In Self-Test Interrupt Enable** The internal PCI Bus writes 1 to enable BIST interrupts. Generates a BIST interrupt to the Local Bus. Reset by the Local Bus when BIST is complete. Software fails the PEX 8311 when BIST is not complete after 2s. *Note: Refer to LCS_INTCSR[23] for BIST Interrupt status.*	Yes	Yes	0
7	**Built-In Self-Test Support** Returns 0 when the PEX 8311 is not BIST-compatible. Returns 1 when the PEX 8311 supports BIST.	Yes	Local	0

Register 20-10. PCI:10h, LOC:10h LCS_PCIBAR0 PCI Express Base Address for Memory Accesses to Local, Runtime, DMA, and Messaging Queue Registers

Bit(s)	Description	Read	Write	Default
	Note: For I$_2$O, the Inbound message frame pool must reside in the Address space pointed to by LCS_PCIBAR0. *Message Frame Address (MFA) is defined by I$_2$O as an offset from this Base address to the start of the message frame.*			
0	**Memory Space Indicator** 0 = Indicates this register maps into Memory space *Note: Hardwired to 0.*	Yes	No	0
2:1	**Register Location** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space *Note: Hardwired to 00b.*	Yes	No	00b
3	**Prefetchable** Writing 1 indicates there are no side effects on reads. Does not affect PEX 8311 operation. *Note: Hardwired to 0.*	Yes	No	0
8:4	**Memory Base Address** Memory Base address for access to **Local**, **Runtime**, **DMA**, and **Messaging Queue** registers (requires 512 bytes). *Note: Hardwired to 0h.*	Yes	No	0h
31:9	**Memory Base Address** Memory Base address for access to **Local**, **Runtime**, **DMA**, and **Messaging Queue** registers.	Yes	Yes	0h

Register 20-11. PCI:14h, LOC:14h LCS_PCIBAR1 PCI Express Base Address for I/O Accesses to Local, Runtime, DMA, and Messaging Queue Registers

Bit(s)	Description	Read	Write	Default
Note:	*This register is enabled or disabled by setting or clearing the I/O Base Address Register Enable bit (LCS_LMISC1[0]).*			
0	**I/O Space Indicator** 1 = Indicates this register maps into I/O space *Note: Hardwired to 1.*	Yes	No	1
1	*Reserved*	Yes	No	0
7:2	**I/O Base Address** Base Address for I/O access to **Local**, **Runtime**, **DMA**, and **Messaging Queue** registers (requires 256 bytes). *Note: Hardwired to 0h.*	Yes	No	0h
31:8	**I/O Base Address** Base Address for I/O access to **Local**, **Runtime**, **DMA**, and **Messaging Queue** registers.	Yes	Yes	0h

Register 20-12. PCI:18h, LOC:18h LCS_PCIBAR2 PCI Express Base Address for Accesses to Local Address Space 0

Bit(s)	Description	Read	Write	Default
Note:	*Configure LCS_LAS0RR before configuring this register.*			
	When allocated, Local Address Space 0 is enabled or disabled by setting or clearing LCS_LAS0BA[0].			
0	**Memory Space Indicator** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. (Bit is writable by way of the LCS_LAS0RR register.)	Yes	No	0
2:1	**Register Location (If Memory Space)** Specified in the **LCS_LAS0RR** register. When mapped into I/O space (**LCS_PCIBAR2**[0]=1), bit 1 is always 0 and bit 2 is included in the Base Address (**LCS_PCIBAR2**[31:4]). 00b = Locate anywhere in 32-bit Memory Address space 01b = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, *Reserved* 10b or 11b = *Reserved*	Yes	When Bit 0 = 0: No When Bit 0 = 1: Bit 1 No, Bit 2 Yes	00b
3	**Prefetchable (If Memory Space)** Writing 1 indicates there are no side effects on Reads. Reflects the value of **LCS_LAS0RR**[3] and provides only status to the system. Does not affect PEX 8311 operation. The associated **Bus Region Descriptor** register (LCS_LBRD0) controls prefetching functions of this Address space. When mapped into I/O space (**LCS_PCIBAR2**[0]=1), bit 3 is included in the Base Address (**LCS_PCIBAR2**[31:4]).	Yes	Memory: No I/O: Yes	0
31:4	**Base Address** Base Address for access to Local Address Space 0.	Yes	Yes	0h

Register 20-13. PCI:1Ch, LOC:1Ch LCS_PCIBAR3 PCI Express Base Address for Accesses to Local Address Space 1

Bit(s)	Description	Read	Write	Default
	Note: Configure **LCS_LAS1RR** *before configuring* **LCS_PCIBAR3**.			
	When allocated, Local Address Space 1 is enabled or disabled by setting or clearing **LCS_LAS1BA***[0].*			
0	**Memory Space Indicator** Writing 0 indicates the register maps into Memory space. Writing 1 indicates the register maps into I/O space. (Bit is writable by way of the LCS_LAS1RR register.)	Yes	No	0
2:1	**Register Location** Specified in the **LCS_LAS1RR** register. When mapped into I/O space (**LCS_PCIBAR3**[0]=1), bit 1 is always 0 and bit 2 is included in the Base Address (**LCS_PCIBAR3**[31:4]). 00b = Locate anywhere in 32-bit Memory Address space 01b = *PCI r2.1*, Locate below 1-MB Memory Address space *PCI r2.2*, *Reserved* 10b or 11b = *Reserved*	Yes	When Bit 0 = 0: No When Bit 0 = 1: Bit 1 No, Bit 2 Yes	00b
3	**Prefetchable (If Memory Space)** Writing 1 indicates there are no side effects on Reads. Reflects the value of **LCS_LAS1RR**[3] and provides only status to the system. Does not affect PEX 8311 operation. The associated Bus Region Descriptor register (LCS_LBRD1) controls prefetching functions of this Address space. When mapped into I/O space (**LCS_PCIBAR3**[0]=1), bit 3 is included in the Base Address (**LCS_PCIBAR3**[31:4]).	Yes	Memory: No I/O: Yes	0
31:4	**Base Address** Base address for access to Local Address Space 1. When I_2O Decode is enabled (**LCS_QSR**[0]=1), **LCS_PCIBAR3**[31:4] return 0h.	Yes	Yes	0h

Register 20-14. PCI:20h, LOC:20h LCS_PCIBAR4 PCI Express Base Address 4

Bit(s)	Description	Read	Write	Default
31:0	*Reserved*	Yes	No	0h

Register 20-15. PCI:24h, LOC:24h LCS_PCIBAR5 PCI Express Base Address 5

Bit(s)	Description	Read	Write	Default
31:0	*Reserved*	Yes	No	0h

Register 20-16. PCI:28h, LOC:28h LCS_PCICIS PCI Cardbus Information Structure Pointer

Bit(s)	Description	Read	Write	Default
31:0	**Cardbus Information Structure (CIS) Pointer for PC Cards** *Not supported*	Yes	No	0h

Register 20-17. PCI:2Ch, LOC:2Ch LCS_PCISVID PCI Subsystem Vendor ID

Bit(s)	Description	Read	Write	Default
15:0	**Subsystem Vendor ID (Unique Add-In Board Vendor ID)** The PLX PCI-SIG-assigned Vendor ID is 10B5h.	Yes	Local/ Serial EEPROM	10B5h

Register 20-18. PCI:2Eh, LOC:2Eh LCS_PCISID PCI Subsystem ID

Bit(s)	Description	Read	Write	Default
15:0	**Subsystem ID (Unique Add-In Board Device ID)**	Yes	Local/ Serial EEPROM	9056h

Register 20-19. PCI:30h, LOC:30h LCS_PCIERBAR PCI Express Base Address for Local Expansion ROM

Bit(s)	Description	Read	Write	Default
0	**Address Decode Enable** Works in conjunction with LCS_EROMRR[0]. Writing 0 indicates that the PEX 8311 does not accept accesses to Expansion ROM address. Cleared to 0 when there is no Expansion ROM. Writing 1 indicates that the PEX 8311 accepts Memory accesses to the Expansion ROM address.	Yes	Yes	0
10:1	*Reserved*	Yes	No	0h
31:11	**Expansion ROM Base Address (Upper 21 Bits).**	Yes	Yes	0h

Register 20-20. PCI:34h, LOC:34h LCS_CAP_PTR New Capability Pointer

Bit(s)	Description	Read	Write	Default
7:0	**New Capability Pointer** Provides an offset into PCI Configuration Space for location of the Power Management capability in the New Capabilities Linked List. *Note:* *For the New Capability Pointer features, this field must always contain the default value of 40h.*	Yes	Local	40h
31:8	*Reserved*	Yes	No	0h

Register 20-21. PCI:3Ch, LOC:3Ch LCS_PCIILR Internal PCI Interrupt Line

Bit(s)	Description	Read	Write	Default
7:0	**Internal PCI Interrupt Line Routing Value** Value indicates which input of the System Interrupt Controller(s) is connected to the PEX 8311 INTA# output.	Yes	Yes/Serial EEPROM	0h

Register 20-22. PCI:3Dh, LOC:3Dh LCS_PCIIPR Internal PCI Wire Interrupt

Bit(s)	Description	Read	Write	Default
7:0	**Internal PCI Wire Interrupt** Indicates which Wire interrupt the PEX 8311 uses. The following values are valid: 0h = No Wire interrupt 1h = INTA#	Yes	Local/ Serial EEPROM	1h

Register 20-23. PCI:3Eh, LOC:3Eh LCS_PCIMGR PCI Minimum Grant

Bit(s)	Description	Read	Write	Default
7:0	**Minimum Grant** Specifies how long a burst period the PEX 8311 needs, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 μs increments.	Yes	Local/ Serial EEPROM	0h

Register 20-24. PCI:3Fh, LOC:3Fh LCS_PCIMLR PCI Maximum Latency

Bit(s)	Description	Read	Write	Default
7:0	**Maximum Latency** Specifies how often the PEX 8311 must gain access to the internal PCI Bus. Value is a multiple of 1/4 μs increments.	Yes	Local/ Serial EEPROM	0h

Register 20-25. PCI:40h, LOC:180h LCS_PMCAPID Power Management Capability ID

Bit(s)	Description	Read	Write	Default
7:0	**Power Management Capability ID** The PCI-SIG-assigned Capability ID for Power Management is 01h.	Yes	No	01h

Register 20-26. PCI:41h, LOC:181h LCS_PMNEXT Power Management Next Capability Pointer

Bit(s)	Description	Read	Write	Default
7:0	**Next_Cap Pointer** Provides an offset into PCI Configuration space for location of the Hot Swap capability in the New Capabilities Linked List. When Power Management is the last capability in the list, clear to 00h. Otherwise, these bits must contain the default value of 48h.	Yes	Local	48h

Register 20-27. PCI:42h, LOC:182h LCS_PMC Power Management Capabilities

Bit(s)	Description	Read	Write	Default
2:0	**Version** Reading value of 010b indicates this function complies with *PCI Power Mgmt. r1.1*.	Yes	Local/ Serial EEPROM	010b
3	**Internal Clock Required for PME# Signal** 1 = Indicates that a function relies on the presence of the internal clock for PME# operation. Because the PEX 8311 does not require the internal clock for PME#, cleared to 0 in the serial EEPROM.	Yes	Local	0
4	*Reserved*	Yes	No	0
5	**Device-Specific Implementation (DSI)** 1 = PEX 8311 requires special initialization following a transition to a D0_uninitialized state before a generic class device driver is able to use the PEX 8311	Yes	Local	0
8:6	**AUX Current** Refer to the *PCI Power Mgmt. r1.1*.	Yes	Local	000b
9	**D1 Support** 1 = PEX 8311 supports the D1 power state	Yes	Local/ Serial EEPROM	0
10	**D2 Support** Specifies that the PEX 8311 does ***not support*** the D2 state.	Yes	Local/ Serial EEPROM	0
15:11	**PME Support** Reserved. Default = 0	Yes	Local/ Serial EEPROM	0000_0b

Register 20-28. PCI:44h, LOC:184h LCS_PMCSR Power Management Control/Status

Bit(s)	Description	Read	Write	Default
1:0	**Power State** Determines or changes the current power state. 00b = D0 01b = D1 10b = *Reserved* 11b = D3hot In a D3hot power state, PCI Express Memory and I/O accesses are disabled, as well as internal interrupts, and only configuration accesses are allowed. The same is true for the D1 power state, when the *D1 Support* bit is set (LCS_PMC[9]=1). Transition from D3hot-to-D0 power state causes a Soft Reset.	Yes	Yes	00b
7:2	*Reserved*	Yes	No	0h
8	**PME_En** Writing 1 enables generation of PM PME messages to PCI Express Space. *Notes: Value after reset is indeterminate (either 1 or 0) at time of initial operating system boot when the internal PRESENT_DET signal is connected to power (D3cold power state support).* *Value after reset is 0 when the internal PRESENT_DET signal is connected to ground (no D3cold power state support).*	Yes	Yes/Serial EEPROM	Sticky bit, refer to Note
12:9	**Data_Select** Selects which data to report through the LCS_PMDATA register and field [14:13] (*Data_Scale*).	Yes	Yes/Serial EEPROM	0h
14:13	**Data_Scale** Indicates the scaling factor to use when interpreting the value of the **Data** register. Bit values and definitions depend on the data value selected by field [12:9] (*Data_Select*). When the Local CPU initializes the Data_Scale values, the *Data_Select* field must be used to determine which Data_Scale value the Local CPU is writing. For Power Consumed and Power Dissipated data, the following scale factors (in Watts) are used. 00b = Unknown 01b = 0.1x 10b = 0.01x 11b = 0.001x	Yes	Local/Serial EEPROM	00b
15	**PME_Status** Reserved. Default = 0	Yes	Local/Set, PCI/Clr	Sticky bit, refer to Note

Register 20-29. PCI:46h, LOC:186h LCS_PMCSR_BSE PMCSR Bridge Support Extensions

Bit(s)	Description	Read	Write	Default
7:0	*Reserved*	Yes	No	0h

Register 20-30. PCI:47h, LOC:187h LCS_PMDATA Power Management Data

Bit(s)	Description	Read	Write	Default
7:0	**Power Management Data** Provides operating data, *such as* power consumed or heat dissipation. Data returned is selected by the *Data_Select* field (LCS_PMCSR[12:9]) and scaled by the *Data_Scale* field (**LCS_PMCSR**[14:13]). Data Select Description 0 D0 Power Consumed 1 D1 Power Consumed 2 *Reserved* 3 D3 Power Consumed 4 D0 Power Dissipated 5 D1 Power Dissipated 6 *Reserved* 7 D3 Power Dissipated	Yes	Local/Serial EEPROM	0h

Register 20-31. PCI:48h, LOC:188h LCS_HS_CNTL Hot Swap Control *(Not Supported)*

Bit(s)	Description	Read	Write	Default
7:0	**Hot Swap ID** *Not supported* The Hot Swap Capability ID is 06h. To disable Hot Swap capabilities, clear this register to 00h.	Yes	Local/ Serial EEPROM	06h

Register 20-32. PCI:49h, LOC:189h LCS_HS_NEXT Hot Swap Next Capability Pointer

Bit(s)	Description	Read	Write	Default
7:0	**Next_Cap Pointer** Provides an offset into PCI Configuration space for location of the VPD capability in the New Capabilities Linked List. This field must contain the default value of 4Ch.	Yes	Local/ Serial EEPROM	4Ch

Register 20-33. PCI:4Ah, LOC:18Ah LCS_HS_CSR Hot Swap Control/Status *(Not Supported)*

Bit(s)	Description	Read	Write	Default
0	*Reserved*	Yes	No	0
1	**ENUM# Interrupt Mask (EIM)** *Not supported* Writing 0 enables interrupt assertion. Writing 1 masks interrupt assertion.	Yes	Yes/Clr	0
2	*Reserved*	Yes	No	0
3	**LED Software On/Off Switch** *Not supported* Writing 0 de-asserts the LEDon# signal. Writing 1 asserts the LEDon# signal.	Yes	PCI	0
5:4	**Programming Interface 0 (PI = 0)** *Not supported*	Yes	No	00b
6	**ENUM# Status – Extraction** *Not supported* Writing 1 reports the ENUM# assertion for removal process.	Yes	Yes/Clr	0
7	**ENUM# Status – Insertion** *Not supported* Writing 1 reports the ENUM# assertion for insertion process.	Yes	Yes/Clr	0
15:8	*Reserved*	Yes	No	0h

Register 20-34. PCI:4Ch, LOC:18Ch LCS_PVPDID PCI Vital Product Identification

Bit(s)	Description	Read	Write	Default
7:0	**VPD ID** The PCI-SIG-assigned Capability ID for VPD is 03h.	Yes	No	03h

Register 20-35. PCI:4Dh, LOC:18Dh LCS_PVPD_NEXT PCI Vital Product Data Next Capability Pointer

Bit(s)	Description	Read	Write	Default
7:0	**Next_Cap Pointer** Because VPD is the last capability in the list, cleared to 0h.	Yes	Local	0h

Register 20-36. PCI:4Eh, LOC:18Eh LCS_PVPDAD PCI Vital Product Data Address

Bit(s)	Description	Read	Write	Default
14:0	**VPD Address** VPD byte address to be accessed. All accesses are 32 bits wide. For VPD writes, the byte address must be Dword-aligned (bits [1:0]=00b). For VPD reads, the byte address must be word-aligned (bit 0 = 0). **LCS_PVPDAD**[14:9] are ignored.	Yes	Yes	0h
15	**F** Controls the direction of the next VPD cycle and indicates when the VPD cycle is complete. Writing 0 along with the VPD address causes a read of VPD information into **LCS_PVPDATA**. The hardware sets this bit to 1 when the VPD Data transfer is complete. Writing 1 along with the VPD address causes a write of VPD information from **LCS_PVPDATA** into a storage component. The hardware clears this bit to 0 after the Write operation is complete.	Yes	Yes	0

Register 20-37. PCI:50h, LOC:190h LCS_PVPDATA PCI VPD Data

Bit(s)	Description	Read	Write	Default
31:0	**VPD Data** Refer to Section 17.2.2, "VPD Data Register," for details.	Yes	Yes	0h

20.5 Local Configuration Registers

This section details the **LCS** Local Configuration registers. Table 20-3 defines the register map.

Note: *"Yes" in the register Read and Write columns indicates the register is writable by the PCI Express interface and Local Bus.*

Table 20-3. Local Configuration Register Map

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits.				PCI/Local Writable	Serial EEPROM Writable
		31 24 23 16 15 8 7 0					
00h	80h	Direct Slave Local Address Space 0 Range				Yes	Yes
04h	84h	Direct Slave Local Address Space 0 Local Base Address (Remap)				Yes	Yes
08h	88h	Mode/DMA Arbitration				Yes	Yes
0Ch	8Ch	Local Miscellaneous Control 2	Serial EEPROM Write-Protected Address Boundary	Local Miscellaneous Control 1	Big/Little Endian Descriptor	Yes	Yes
10h	90h	Direct Slave Expansion ROM Range				Yes	Yes
14h	94h	Direct Slave Expansion ROM Local Base Address (Remap) and BREQo Control				Yes	Yes
18h	98h	Local Address Space 0/Expansion ROM Bus Region Descriptor				Yes	Yes
1Ch	9Ch	Local Range for Direct Master-to-PCI Express				Yes	Yes
20h	A0h	Local Base Address for Direct Master-to-PCI Express Memory	Reserved			Yes	Yes
24h	A4h	Local Base Address for Direct Master-to-PCI Express I/O Configuration	Reserved			Yes	Yes
28h	A8h	PCI Express Base Address (Remap) for Direct Master-to-PCI Express Memory				Yes	Yes
2Ch	ACh	PCI Configuration Address for Direct Master-to-PCI Express I/O Configuration				Yes	Yes
F0h	170h	Direct Slave Local Address Space 1 Range				Yes	Yes
F4h	174h	Direct Slave Local Address Space 1 Local Base Address (Remap)				Yes	Yes
F8h	178h	Local Address Space 1 Bus Region Descriptor				Yes	Yes
FCh	17Ch	Direct Master PCI Express Dual Address Cycles Upper Address				Yes	No
100h	1A0h	Internal Arbiter Control				Yes	Yes
104h	1A4h	PCI Abort Address				No	No

Notes: *PCI offset registers 100h and 104h are accessible only by way of the **LCS_PCIBAR0** register.*

Refer to the individual register descriptions to determine which bits are writable.

Register 20-38. PCI:00h, LOC:80h LCS_LAS0RR Direct Slave Local Address Space 0 Range

Bit(s)	Description	Read	Write	Default
0	**Memory Space Indicator** Writing 0 indicates Local Address Space 0 maps into PCI Express Memory space. Writing 1 indicates Local Address Space 0 maps into PCI Express I/O space.	Yes	Yes/Serial EEPROM	0
2:1	When mapped into Memory space (**LCS_LAS0RR**[0]=0), the only valid value is 00b. Locate anywhere in PCI Express Address space. When mapped into I/O space (**LCS_LAS0RR**[0]=1), bit 1 must be cleared to 0. Bit 2 is included with **LCS_LAS0RR**[31:3] to indicate the decoding range.	Yes	Yes/Serial EEPROM	00b
3	When mapped into Memory space (**LCS_LAS0RR**[0]=0), writing 1 indicates reads are prefetchable (does not affect PEX 8311 operation, but is used for system status). When mapped into I/O space (**LCS_LAS0RR**[0]=1), this bit is included with **LCS_LAS0RR**[31:4, 2] to indicate the decoding range.	Yes	Yes/Serial EEPROM	0
31:4	Specifies which PCI Express Address bits to use for decoding a PCI access to Local Address Space 0. Each bit corresponds to a PCI Express Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others (used in conjunction with **LCS_PCIBAR2**). Default is 1 MB. *Notes: LCS_LAS0RR range (**not** the Range register) must be power of 2. "Range register value" is two's complement of the range.* *Per PCI r2.2, limit I/O-Mapped spaces to 256 bytes per space.*	Yes	Yes/Serial EEPROM	FFF0_000h

Register 20-39. PCI:04h, LOC:84h LCS_LAS0BA Direct Slave Local Address Space 0 Local Base Address (Remap)

Bit(s)	Description	Read	Write	Default
0	**Local Address Space 0 Enable** Writing 1 enables decoding of PCI Express Addresses for Direct Slave access to Local Address Space 0. Writing 0 disables decoding.	Yes	Yes/Serial EEPROM	0
1	*Reserved*	Yes	No	0
3:2	When Local Address Space 0 is mapped into Memory space (**LCS_LAS0RR**[0]=0), **LCS_LAS0BA**[3:2] must be 00b. When mapped into I/O space (**LCS_LAS0RR**[0]=1), included with **LCS_LAS0BA**[31:4] for remapping.	Yes	Yes/Serial EEPROM	00b
31:4	**Remap LCS_PCIBAR2 Base Address to Local Address Space 0 Base Address** The **LCS_PCIBAR2** Base address translates to the Local Address Space 0 Base Address programmed in this register. A Direct Slave access to an offset from **LCS_PCIBAR2** maps to the same offset from this Local Base address. *Note: Remap Address value must be a multiple of the **LCS_LAS0RR** range (**not** the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 20-40. PCI:08h or ACh, LOC:88h or 12Ch LCS_MARBR Mode/DMA Arbitration

Bit(s)	Description	Read	Write	Default
7:0	**Local Bus Latency Timer** **C and J Modes:** Number of Local Bus Clock cycles to occur before de-asserting LHOLD and releasing the Local Bus. The Local Bus Latency Timer starts counting upon LHOLDA assertion. When **LCS_MARBR**[16]=1, specifies the minimum delay (in LCLK cycles) before interrupting a continuing Direct Slave or DMA transfer and releasing the Local Bus by de-asserting LHOLD. The Local Bus Latency Timer starts counting upon ADS# assertion. Refer to Section 9.5.14.1, "DMA Arbitration – C and J Modes," and Section 9.5.16.1, "Local Bus Latency and Pause Timers – C and J Modes," for further details. **M Mode:** Number of Local Bus Clock cycles to occur before de-asserting BB# and releasing the Local Bus. The Local Bus Latency Timer starts counting upon BB# assertion. When **LCS_MARBR**[16]=1, specifies the minimum delay (in LCLK cycles) before interrupting a continuing Direct Slave or DMA transfer and releasing the Local Bus by de-asserting BB#. The Local Bus Latency Timer starts counting upon TS# assertion. Refer to Section 9.5.14.2, "DMA Arbitration – M Mode," and Section 9.5.16.2, "Local Bus Latency and Pause Timers – M Mode," for further details.	Yes	Yes/Serial EEPROM	0h
15:8	**Local Bus Pause Timer** Valid only during DMA transfers. **C and J Modes:** Number of Local Bus Clock cycles to occur before re-asserting LHOLD after releasing the Local Bus. When **LCS_MARBR**[17]=1, specifies the minimum delay (in LCLK cycles) before re-asserting LHOLD to resume a previously interrupted DMA transfer. **M Mode:** Number of Local Bus Clock cycles to occur before re-asserting BR# after releasing the Local Bus. When **LCS_MARBR**[17]=1, specifies the minimum delay (in LCLK cycles) before re-asserting BR# to resume a previously interrupted DMA transfer.	Yes	Yes/Serial EEPROM	0h

Register 20-40. PCI:08h or ACh, LOC:88h or 12Ch LCS_MARBR Mode/DMA Arbitration (Cont.)

Bit(s)	Description	Read	Write	Default
16	**Local Bus Latency Timer Enable** Writing 0 disables the Local Bus Latency Timer. Writing 1 enables the Local Bus Latency Timer.	Yes	Yes/Serial EEPROM	0
17	**Local Bus Pause Timer Enable** Writing 0 disables the Pause Timer. Writing 1 enables the Pause Timer.	Yes	Yes/Serial EEPROM	0
18	**C and J Mode Local Bus BREQi Enable** **C and J Modes:** Writing 1 enables the Local Bus BREQi. When BREQi is asserted, the PEX 8311 de-asserts LHOLD and releases the Local Bus. Regardless of the type of transfer, if BREQi is asserted while the PEX 8311 is transferring data on the Local Bus, the PEX 8311 will attempt to transfer up to a total of three additional Dwords of data, which includes the last transfer with BLAST# asserted. The actual number of additional transfers depends upon the Local Bus width and address when BREQi is asserted. The minimum assertion duration of BREQi is one Local Bus Clock cycle. Assert BREQi and allow it to remain asserted until either BLAST# is asserted (BLAST#=0) or LHOLD is de-asserted (LHOLD=0). **M Mode:** This bit is *not used* in M mode. *Reserved, not serial EEPROM writable, and cleared to 0.*	Yes	Yes/Serial EEPROM	0
20:19	**DMA Channel Priority** Writing 00b indicates a Rotational Priority scheme. Writing 01b indicates Channel 0 has priority. Writing 10b indicates Channel 1 has priority. Value of 11b is *reserved*.	Yes	Yes/Serial EEPROM	00b
21	**Local Bus Direct Slave Release Bus Mode** **C and J Modes:** 1 = PEX 8311 de-asserts LHOLD and releases the Local Bus when either of the following conditions occur: • Direct Slave Write FIFO becomes empty during a Direct Slave Write • Direct Slave Read FIFO becomes full during a Direct Slave Read **M Mode:** This bit must be cleared to 0.	Yes	Yes/Serial EEPROM	1
22	**Direct Slave Internal LOCK# Input Enable** Writing 0 disables Direct Slave locked sequences. Writing 1 enables Direct Slave locked sequences.	Yes	Yes/Serial EEPROM	0
23	*Reserved*	Yes	Yes/Serial EEPROM	0

Register 20-40. PCI:08h or ACh, LOC:88h or 12Ch LCS_MARBR Mode/DMA Arbitration (Cont.)

Bit(s)	Description	Read	Write	Default
24	**PCI Compliance Enable** 0 = New *PCI r2.2* features are not enabled (reverts to *PCI r2.1 behavior*). 1 = PEX 8311 internally performs PCI Read and Write transactions in compliance with the *PCI r2.2*. Setting this bit enables Direct Slave Delayed Reads, 2^{15} internal clock timeout on Retrys, 8- and 16-clock PCI latency rules, and enables the option to select PCI Read No Write mode (Retries for Writes) (**LCS_MARBR**[25]). *Note: Refer to Section 9.3.4, "PCI Compliance Enable," for further details.*	Yes	Yes/Serial EEPROM	0
25	**PCI Read No Write Mode (Local Retries for Writes)** When PCI Compliance is enabled (**LCS_MARBR**[24]=1): 0 (or **LCS_MARBR**[24]=0) = Allows Writes to occur while a Delayed Read is pending 1 = Forces a Local Retry on Writes when a Delayed Read is pending	Yes	Yes/Serial EEPROM	0
26	**PCI Read with Write Flush Mode** 0 = Does not affect a pending Delayed Read when a Write cycle occurs 1 = Flushes a pending Delayed Read cycle when a Write cycle is detected	Yes	Yes/Serial EEPROM	0
27	**C and J Mode Gate Local Bus Latency Timer with BREQi** 0, or when the Local Bus Latency Timer is disabled (**LCS_MARBR**[16]=0) = BREQi assertion causes the PEX 8311 to release the Local Bus. 1 = Local Bus Latency Timer counts only while BREQi is asserted (BREQi=1). Therefore, the Local Bus Latency Timer cannot expire unless BREQi is asserted for the number of Local clocks programmed into **LCS_MARBR**[7:0]. BREQi can be toggled, as needed, to enable or disable the Local Bus Latency Timer Counter. *Note: Refer to Section 5.1.1, "Local Bus Arbitration and BREQi – C and J Modes," for further details.* **M Mode:** This bit is *not used* in M mode. ***Reserved, not serial EEPROM writable, and cleared to 0.***	Yes	Yes/Serial EEPROM	0

Register 20-40. PCI:08h or ACh, LOC:88h or 12Ch LCS_MARBR Mode/DMA Arbitration (Cont.)

Bit(s)	Description	Read	Write	Default
28	**PCI Read No Flush Mode** Writing 0 submits a request to flush the Direct Slave Read FIFO when a PCI Read cycle completes. Writing 1 submits a request to not flush the Direct Slave Read FIFO when a PCI Read cycle completes (Direct Slave Read Ahead mode).	Yes	Yes/Serial EEPROM	0
29	**Device and Vendor ID Select** 0 = Reads from the PCI Configuration register address 00h return the Device and Vendor IDs 1 = Reads from the PCI Configuration register address 00h return the Subsystem and Subsystem Vendor IDs	Yes	Yes/Serial EEPROM	0
30	**Direct Master Write FIFO Full Status Flag** 1 = Direct Master Write FIFO is almost full. Reflects the DMPAF ball value, as determined by the Programmable Almost Full Flag value in **LCS_DMPBAM**[10, 8:5].	Yes	No	0
31	**M Mode BIGEND#/WAIT# I/O Select** Writing 0 selects Big Endian input functionality. Writing 1 selects the Wait I/O functionality of the signal. **C and J Modes:** This bit is *not used* in C and J modes. *Reserved, not serial EEPROM writable, and cleared to 0.*	Yes	Yes/Serial EEPROM	0

Register 20-41. PCI:0Ch, LOC:8Ch LCS_BIGEND Big/Little Endian Descriptor

Bit(s)	Description	Read	Write	Default
0	**Configuration Register Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Local accesses to the Configuration registers. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
1	**Direct Master Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Direct Master accesses. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
2	**Direct Slave Local Address Space 0 Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Direct Slave accesses to Local Address Space 0. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
3	**Direct Slave Expansion ROM Space Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Direct Slave accesses to Expansion ROM. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
4	**Big Endian Byte Lane Mode** **C and J Modes:** Writing 0 specifies that in any Endian mode, use the following byte lanes: • [15:0] for a 16-bit Local Bus • [7:0] for an 8-bit Local Bus Writing 1 specifies that in any Endian mode, use the following byte lanes: • [31:16] for a 16-bit Local Bus • [31:24] for an 8-bit Local Bus **M Mode:** Writing 0 specifies that in any Endian mode, use the following byte lanes: • [0:15] for a 16-bit Local Bus • [0:7] for an 8-bit Local Bus Writing 1 specifies that in any Endian mode, use the following byte lanes: • [16:31] for a 16-bit Local Bus • [24:31] for an 8-bit Local Bus	Yes	Yes/Serial EEPROM	0
5	**Direct Slave Local Address Space 1 Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for Direct Slave accesses to Local Address Space 1. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
6	**DMA Channel 1 Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for DMA Channel 1 accesses to the Local Bus. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0
7	**DMA Channel 0 Big Endian Mode (Address Invariance)** Writing 0 specifies use of Little Endian data ordering for DMA Channel 0 accesses to the Local Bus. Writing 1 specifies Big Endian ordering.	Yes	Yes/Serial EEPROM	0

Register 20-42. PCI:0Dh, LOC:8Dh LCS_LMISC1 Local Miscellaneous Control 1

Bit(s)	Description	Read	Write	Default
0	**I/O Base Address Register Enable** 0 = **LCS_PCIBAR1** is disabled. This option is intended for embedded systems only. 1 = **LCS PCI Express Base Address for I/O accesses to Local, Runtime, DMA, and Messaging Queue Registers** register (**LCS_PCIBAR1**) is enabled. Set this bit to 1 for PC platforms.	Yes	Yes/Serial EEPROM	1
1	**I/O Base Address Register Shift** When the **I/O Base Address** register is disabled and this bit is cleared to 0 (**LCS_LMISC1**[1:0]=00b), then **LCS_PCIBAR2** and **LCS_PCIBAR3** remain at PCI Configuration addresses 18h and 1Ch. When the **I/O Base Address** register is disabled and this bit is set to 1 (**LCS_LMISC1**[1:0]=10b), **LCS_PCIBAR2** (Local Address Space 0) and **LCS_PCIBAR3** (Local Address Space 1) are shifted to become **LCS_PCIBAR1** and **LCS_PCIBAR2** at PCI Configuration addresses 14h and 18h. Set when a blank region in **I/O Base Address** register space cannot be accepted by the system BIOS.	Yes	Yes/Serial EEPROM	0
2	**Local Init Status** Reading 1 indicates Local Init is done. Responses to PCI accesses prior to this bit being set are determined by the USERi state when the PEX 8311 receives an external reset at PERST# de-assertion in Endpoint mode (ROOT_COMPLEX#=1), or LRESET# input de-assertion in Root Complex mode (ROOT_COMPLEX#=0). *Note: Refer to Section 4.3.2, "Local Initialization and PCI Express Interface Behavior," for further details.*	Yes	Local/ Serial EEPROM	0
3	**Direct Master (PCI Initiator) Write FIFO Flush during PCI Master Abort** 0 = PEX 8311 flushes the Direct Master Write FIFO each time a PCI Master/ Target Abort or Retry timeout occurs 1 = PEX 8311 retains data in the Direct Master Write FIFO	Yes	Yes/Serial EEPROM	0

Register 20-42. PCI:0Dh, LOC:8Dh LCS_LMISC1 Local Miscellaneous Control 1 (Cont.)

Bit(s)	Description	Read	Write	Default
4	**M Mode Direct Master Delayed Read Enable** Writing 1 enables the PEX 8311 to operate in Delayed Transaction mode for Direct Master reads. The PEX 8311 issues a RETRY# to the M mode Master and prefetches Read data from the PCI Bus. **C and J Modes:** This bit is *not used* in C and J modes. ***Reserved, not serial EEPROM writable, and cleared to 0.***	Yes	Yes/Serial EEPROM	0
5	**M Mode TEA# Input Interrupt Mask** When set to 1, TEA# input causes SERR# output to assert on the PCI Bus, if enabled (**LCS_PCICR**[8]=1), and the Signaled System Error [*Signaled System Error (Internal SERR# Status)*] bit is set (**LCS_PCISR**[14]=1). Writing 0 masks the TEA# input to assert SERR#. **LCS_PCISR**[14] is set to 1 in both cases. **C and J Modes:** This bit is *not used* in C and J modes. ***Reserved, not serial EEPROM writable, and cleared to 0.***	Yes	Yes/Serial EEPROM	0
6	**M Mode Direct Master Write FIFO Almost Full RETRY#** **Output Enable** 1 = PEX 8311 issues a RETRY# when the Direct Master Write FIFO is almost full **C and J Modes:** This bit is *not used* in C and J modes. ***Reserved, not serial EEPROM writable, and cleared to 0.***	Yes	Yes/Serial EEPROM	0
7	**Disconnect with Flush Read FIFO** Value of 0, or clearing of the *PCI Compliance Enable* bit (**LCS_MARBR**[24]=0) = Causes a new Direct Slave Read request to Retry when a Delayed Read is pending in the Read FIFO. When PCI Compliance is enabled (**LCS_MARBR**[24]=1), value of 1 causes acceptance of a new Read request with flushing of the Read FIFO when a Direct Slave Read request does not match an existing, pending Delayed Read in the Read FIFO.	Yes	Yes/Serial EEPROM	0

Register 20-43. PCI:0Eh, LOC:8Eh LCS_PROT_AREA Serial EEPROM Write-Protected Address Boundary

Bit(s)	Description	Read	Write	Default
6:0	**Serial EEPROM Location Starting at Dword Boundary (48 Dwords = 192 Bytes) for VPD Accesses** Value is the number of Dwords that are VPD write-protected (starting from serial EEPROM byte address 00h). The corresponding serial EEPROM byte (VPD) address is this value multiplied by 4. Default value of 30h sets the boundary at serial EEPROM byte (VPD) address C0h. Value of 40h write protects a 2K-bit serial EEPROM. A maximum value of 7Fh write-protects all but 2 words in a 4K-bit serial EEPROM. Serial EEPROM addresses below this boundary are Read-Only. *Note: PEX 8311 Configuration data is stored below Dword address 19h.*	Yes	Yes/Serial EEPROM	30h
7	*Reserved*	Yes	No	0

Register 20-44. PCI:0Fh, LOC:8Fh LCS_LMISC2 Local Miscellaneous Control 2

Bit(s)	Description	Read	Write	Default
0	**READY#/TA# Timeout Enable** **C and J Modes:** 1 = Enables READY# timeout. **M Mode:** 1 = Enables TA# timeout.	Yes	Yes/Serial EEPROM	0
1	**READY#/TA# Timeout Select** **C and J Modes:** 0 = READY# times out in 32 clocks 1 = READY# times out in 1,024 clocks **M Mode:** 0 = TA# times out in 32 clocks 1 = TA# times out in 1,024 clocks	Yes	Yes/Serial EEPROM	0
4:2	**Direct Slave Delayed Write Mode** Delay in LCLK of LHOLD assertion for PCI Burst Writes. 000b = 0 LCLK 001b = 4 LCLK 010b = 8 LCLK 011b = 16 LCLK 100b = 20 LCLK 101b = 24 LCLK 110b = 28 LCLK 111b = 32 LCLK	Yes	Yes/Serial EEPROM	000b
5	**Direct Slave Write FIFO Full Condition** 0 = Retries Direct Slave Read accesses when the Direct Slave Write FIFO is full with Direct Slave Write data 1 = Guarantees that when the Direct Slave Write FIFO is full with Direct Slave Write data, there is always one location remaining empty for the Direct Slave Read address to be accepted by the PEX 8311	Yes	Yes/Serial EEPROM	0
7:6	*Reserved*	Yes	No	00b

Register 20-45. PCI:10h, LOC:90h LCS_EROMRR Direct Slave Expansion ROM Range

Bit(s)	Description	Read	Write	Default
0	**Address Decode Enable** Bit 0 is enabled only from the serial EEPROM. To disable, clear the PCI Express Expansion ROM *Address Decode Enable* bit to 0 (**LCS_PCIERBAR**[0]=0).	Yes	Serial EEPROM Only	0
10:1	*Reserved*	Yes	No	0h
31:11	Specifies which PCI Express Address bits to use for decoding a PCI Express-to-Local Bus Expansion ROM. Each bit corresponds to a PCI Express Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others (used in conjunction with **LCS_PCIERBAR**). The minimum range, when enabled, is 2 KB, and maximum range allowed by *PCI r2.2* is 16 MB. *Notes: LCS_EROMRR range (**not** the Range register) must be power of 2. "Range register value" is two's complement of the range.* *Program **LCS_EROMRR** by way of the serial EEPROM to a value of 0h, unless Expansion ROM is present on the Local Bus. When the value is not 0h, system BIOS can attempt to allocate Expansion ROM Address space and then access it at the Local Address space specified in **LCS_EROMBA**[31:11] (default value is 0h) to determine whether the Expansion ROM image is valid. When the image is not valid, as defined in the PCI r2.2, Section 6.3.1.1 (PCI Express Expansion ROM Header Format), the system BIOS unmaps the Expansion ROM Address space that it initially allocated, by writing 0h to **LCS_PCIERBAR**.*	Yes	Yes/Serial EEPROM	0h

**Register 20-46. PCI:14h, LOC:94h LCS_EROMBA Direct Slave Expansion ROM
Local Base Address (Remap) and BREQo Control**

Bit(s)	Description	Read	Write	Default
3:0	**C and J Mode Backoff Request Delay Clocks** Number of Local Bus clocks in which a Direct Slave LHOLD request is pending and a Local Direct Master access is in progress and not being granted the bus (LHOLDA) before asserting BREQo. BREQo remains asserted until the PEX 8311 receives LHOLDA (LSB is 8 or 64 clocks). **M Mode RETRY# Signal Assertion Delay Clocks** Number of Local Bus clocks in which a Direct Slave BR# request is pending and a Local Direct Master access is in progress and not being granted the bus (BG#) before asserting RETRY#. Once asserted, RETRY# remains asserted until the PEX 8311 samples BB# de-assertion by the external Local Bus Arbiter (LSB is 8 or 64 clocks).	Yes	Yes/Serial EEPROM	0h
4	**Local Bus Backoff Enable** **C and J Modes:** Writing 1 enables the PEX 8311 to assert BREQo. **M Mode:** Writing 1 enables the PEX 8311 to assert RETRY#.	Yes	Yes/Serial EEPROM	0
5	**Backoff Timer Resolution** Writing 1 changes the LSB of the Backoff Timer from 8 to 64 clocks.	Yes	Yes/Serial EEPROM	0
10:6	*Reserved*	Yes	No	0h
31:11	**Remap PCI Express Expansion ROM into Local Address Space** Bits in this register remap (replace) the PCI Express Address bits used in decode as Local Address bits. *Note: Remap Address value must be a multiple of the **LCS_EROMRR** range (**not** the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 20-47. PCI:18h, LOC:98h LCS_LBRD0 Local Address Space 0/Expansion ROM Bus Region Descriptor

Bit(s)	Description	Read	Write	Default
1:0	**Local Address Space 0 Local Bus Data Width** Writing of the field value indicates the associated bus data width. 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes/Serial EEPROM	11b
5:2	**Local Address Space 0 Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes/Serial EEPROM	0h
6	**Local Address Space 0 READY#/TA# Input Enable** **C and J Modes:** Writing 0 disables READY# input. Writing 1 enables READY# input. **M Mode:** Writing 0 disables TA# input. Writing 1 enables TA# input.	Yes	Yes/Serial EEPROM	1
7	**Local Address Space 0 Continuous Burst Enable** **C and J Modes:** Also referred to as the *BTERM# Input Enable* bit. When bursting is enabled (**LCS_LBRD0**[24]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, **LCS_LBRD0**[6]=1). *Note: Refer to Section 9.3.12, "Local Bus Direct Slave Data Transfer Modes," for further details.* **M Mode:** Also referred to as the *BI Mode* bit. When bursting is enabled (**LCS_LBRD0**[24]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. *Note: Refer to Section 9.3.12, "Local Bus Direct Slave Data Transfer Modes," for further details.*	Yes	Yes/Serial EEPROM	0

**Register 20-47. PCI:18h, LOC:98h LCS_LBRD0 Local Address Space 0/Expansion ROM
Bus Region Descriptor (Cont.)**

Bit(s)	Description	Read	Write	Default
8	**Local Address Space 0 Prefetch Disable** When mapped into Memory space (**LCS_LAS0RR**[0]=0), writing 0 enables Read prefetching. Writing 1 disables prefetching. When prefetching is disabled, the PEX 8311 disconnects after each Memory read.	Yes	Yes/Serial EEPROM	0
9	**Expansion ROM Space Prefetch Disable** Writing 0 enables Read prefetching. Writing 1 disables prefetching. When prefetching is disabled, the PEX 8311 disconnects after each Memory read.	Yes	Yes/Serial EEPROM	0
10	**Local Address Space 0/Expansion ROM Space Prefetch Counter Enable** 0 = PEX 8311 ignores the count and continues prefetching as follows: • **If PCI Read No Flush mode is enabled (LCS_MARBR[28]=1)** – Continues prefetching until the Direct Slave Read FIFO is full, or • **If PCI Read No Flush mode is disabled (LCS_MARBR[28]=0)** – Continues prefetching until PCI Read Completion, at which time the Direct Slave Read FIFO is flushed. 1, and Memory prefetching is enabled = PEX 8311 prefetches up to the number of Dwords specified in the Prefetch Counter (**LCS_LBRD0**[14:11])	Yes	Yes/Serial EEPROM	0
14:11	**Local Address Space 0/Expansion ROM Space Prefetch Counter** Number of Dwords to prefetch during Memory Read cycles (0 to 15). A count of zero selects a prefetch of 16 Dwords.	Yes	Yes/Serial EEPROM	0h
15	*Reserved*	Yes	No	0

Register 20-47. PCI:18h, LOC:98h LCS_LBRD0 Local Address Space 0/Expansion ROM Bus Region Descriptor (Cont.)

Bit(s)	Description	Read	Write	Default
17:16	**Expansion ROM Space Local Bus Data Width** Writing of the field value indicates the associated bus data width. 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes/Serial EEPROM	11b
21:18	**Expansion ROM Space Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes/Serial EEPROM	0h
22	**Expansion ROM Space READY#/TA# Input Enable** **C and J Modes:** Writing 0 disables READY# input. Writing 1 enables READY# input. **M Mode:** Writing 0 disables TA# input. Writing 1 enables TA# input.	Yes	Yes/Serial EEPROM	1
23	**Expansion ROM Space Continuous Burst Enable** **C and J Modes:** Also referred to as the *BTERM# Input Enable* bit. When bursting is enabled (**LCS_LBRD0**[26]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, **LCS_LBRD0**[22]=1). *Note: Refer to Section 9.3.12, "Local Bus Direct Slave Data Transfer Modes," for further details.* **M Mode:** Also referred to as the *BI Mode* bit. When bursting is enabled (**LCS_LBRD0**[26]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. *Note: Refer to Section 9.3.12, "Local Bus Direct Slave Data Transfer Modes," for further details.*	Yes	Yes/Serial EEPROM	0

Register 20-47. PCI:18h, LOC:98h LCS_LBRD0 Local Address Space 0/Expansion ROM Bus Region Descriptor (Cont.)

Bit(s)	Description	Read	Write	Default
24	**Local Address Space 0 Burst Enable** Writing 1 enables bursting. Writing 0 disables bursting.	Yes	Yes/Serial EEPROM	0
25	**Extra Long Load from Serial EEPROM** Writing 0 indicates not to load the **Subsystem ID**, **Local Address Space 1** registers, and **Internal Arbiter** register values. Writing 1 loads the **Subsystem ID**, **Local Address Space 1** registers, and **Internal Arbiter** register values.	Yes	Serial EEPROM Only	0
26	**Expansion ROM Space Burst Enable** Writing 1 enables bursting. Writing 0 disables bursting.	Yes	Yes/Serial EEPROM	0
27	**Direct Slave PCI Write Mode** Determines the response of the Local Bus bridge to a Direct Slave Write when the Direct Slave Write FIFO is full. 0 = Retry 1 = Wait until sufficient space is available *Note: Used for all three Local Address spaces – Space 0, Space 1, and Expansion ROM.*	Yes	Yes/Serial EEPROM	0
31:28	**Direct Slave Retry Delay Clocks** Number of internal clocks (multiplied by 8) from the beginning of a Direct Slave access until a Local Retry is issued, when the transfer was not completed. Valid for Read cycles only when **LCS_MARBR**[24]=0. Valid for Write cycles only when **LCS_LBRD0**[27]=1. *Note: Used for all three Local Address spaces – Space 0, Space 1, and Expansion ROM.*	Yes	Yes/Serial EEPROM	4h (32 clocks)

Register 20-48. PCI:1Ch, LOC:9Ch LCS_DMRR Local Range for Direct Master-to-PCI Express

Bit(s)	Description	Read	Write	Default
15:0	*Reserved* (64-KB increments).	Yes	No	0h
31:16	Specifies the size (in bytes) of the range of PCI Express addresses to be mapped into Local Bus addresses for Direct Master access. Each bit corresponds to a PCI Express Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0h to all others. *Note: LCS_DMRR range (**not** the Range register) must be power of 2. "Range register value" is two's complement of the range.*	Yes	Yes/Serial EEPROM	0h

Register 20-49. PCI:20h, LOC:A0h LCS_DMLBAM Local Base Address for Direct Master-to-PCI Express Memory

Bit(s)	Description	Read	Write	Default
15:0	*Reserved*	Yes	No	0h
31:16	Assigns a value to bits to use for decoding Local-to-PCI Express Memory accesses. *Note: Local Base Address value must be a multiple of the **LCS_DMRR** range (**not** the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 20-50. PCI:24h, LOC:A4h LCS_DMLBAI Local Base Address for Direct Master-to-PCI Express I/O Configuration

Bit(s)	Description	Read	Write	Default
15:0	*Reserved*	Yes	No	0h
31:16	Assigns a value to bits to use for decoding Direct Master I/O or Direct Master Configuration accesses. *Notes: Local Base Address value must be a multiple of the **LCS_DMRR** range (**not** the Range register). I/O Address space is 64 KB.* *Refer to **LCS_DMPBAM**[13] for the I/O Remap Address option.*	Yes	Yes/Serial EEPROM	0h

Register 20-51. PCI:28h, LOC:A8h LCS_DMPBAM PCI Express Base Address (Remap)
for Direct Master-to-PCI Express Memory

Bit(s)	Description	Read	Write	Default
0	**Direct Master Memory Access Enable** Writing 0 disables decode of Direct Master Memory accesses. Writing 1 enables decode of Direct Master Memory accesses within the Address space defined by the **LCS_DMLBAM** and **LCS_DMRR** registers.	Yes	Yes/Serial EEPROM	0
1	**Direct Master I/O Access Enable** Writing 0 disables decode of Direct Master I/O accesses. Writing 1 enables decode of Direct Master I/O accesses within the 64-KB Address space beginning at the **LCS_DMLBAI** Base address.	Yes	Yes/Serial EEPROM	0
2	**Direct Master Read Ahead Mode** Valid only when **LCS_DMPBAM**[12, 3]=00b. Writing 0 submits a request to flush the Read FIFO when a Local Read cycle completes. Writing 1 submits a request to not flush the Read FIFO when the Local Read cycle completes (Direct Master Read Ahead mode). *Caution: To prevent constant locking of the internal PCI Bus, do not simultaneously enable this bit and Direct Master PCI Read mode (LCS_DMPBAM[2, 4]≠11b).*	Yes	Yes/Serial EEPROM	0
12, 3	**Direct Master Read Prefetch Size Control** 00b = PEX 8311 continues to prefetch Read data from the internal PCI Bus until the Direct Master Read access is finished. This can result in an additional four unneeded Dwords being prefetched from the internal PCI Bus. 01b = Prefetch up to 4 Dwords from the internal PCI Bus. 10b = Prefetch up to 8 Dwords from the internal PCI Bus. 11b = Prefetch up to 16 Dwords from the internal PCI Bus. *Caution: Direct Master Burst reads must not exceed the programmed limit.*	Yes	Yes/Serial EEPROM	00b
4	**Direct Master PCI Read Mode** Writing 0 indicates that the PEX 8311 Local Bus bridge disconnects from the PCI Express bridge when the FIFO becomes full. (Because no other devices are contending for access, there is no need to release it.) Writing 1 indicates the PEX 8311 holds the PCI Express Bridge in a wait state when the Read FIFO becomes full. *Caution: To prevent constant locking of the internal PCI Bus, do not simultaneously enable this bit and Direct Master Read Ahead mode (LCS_DMPBAM[2, 4]≠11b).*	Yes	Yes/Serial EEPROM	0
10, 8:5	**Programmable Almost Full Flag** **C and J Modes:** When the number of entries in the 64-Dword Direct Master Write FIFO exceeds a (programmed value +1, times 2), DMPAF is asserted High. **M Mode:** When the number of entries in the 64-Dword Direct Master Write FIFO exceeds a (programmed value +1, times 2), MDREQ#/DMPAF is asserted High.	Yes	Yes/Serial EEPROM	00000b

**Register 20-51. PCI:28h, LOC:A8h LCS_DMPBAM PCI Express Base Address (Remap)
for Direct Master-to-PCI Express Memory (Cont.)**

Bit(s)	Description	Read	Write	Default
9	**Memory Write and Invalidate Mode** 1 = PEX 8311 waits for 8 or 16 Dwords to be written from the Local Bus before starting a PCI access. Memory Write and Invalidate cycles to the internal PCI Bus must be 8- or 16-Dword bursts.	Yes	Yes/Serial EEPROM	0
11	**Direct Master Prefetch Limit** Writing 0 results in continuous prefetch over the boundary space. Writing 1 causes the PEX 8311 to terminate a prefetch at 4-KB boundaries and restart when the boundary is crossed.	Yes	Yes/Serial EEPROM	0
13	**I/O Remap Select** Writing 0 uses **LCS_DMPBAM**[31:16] as PCI Express Address bits [31:16] for PCI Express I/O Direct Master transactions. Writing 1 forces PCI Express Address bits [31:16] to all zeros (0) for PCI Express I/O Direct Master transactions.	Yes	Yes/Serial EEPROM	0
15:14	**Direct Master Delayed Write Mode** Delays internal PCI Bus request after Direct Master Burst Write cycle has started. 00b = No delay; immediately start cycle 01b = Delay 4 internal clocks 10b = Delay 8 internal clocks 11b = Delay 16 internal clocks	Yes	Yes/Serial EEPROM	00b
31:16	**Remap Local-to-PCI Express Space into PCI Express Address Space** Bits in this register remap (replace) Local Address bits used in decode as the PCI Express Address bits. *Note:* *Remap Address value must be a multiple of the* **LCS_DMRR** *range* (***not** the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 20-52. PCI:2Ch, LOC:ACh LCS_DMCFGA PCI Configuration Address
for Direct Master-to-PCI Express I/O Configuration

Bit(s)	Description	Read	Write	Default
1:0	**Configuration Cycle Type** 00b = Type 0 01b = Type 1	Yes	Yes/Serial EEPROM	00b
7:2	**Register Number**	Yes	Yes/Serial EEPROM	0h
10:8	**Function Number**	Yes	Yes/Serial EEPROM	000b
15:11	**Device Number**	Yes	Yes/Serial EEPROM	0h
23:16	**Bus Number**	Yes	Yes/Serial EEPROM	0h
30:24	*Reserved*	Yes	No	0h
31	**Conversion Enable** 1 = I/O accesses are converted to a Type 0 or Type 1 **LCS** PCI Configuration Space access In Root Complex mode, use Type 0 accesses to configure the PEX 8311 **PECS** registers, and Type 1 accesses to configure downstream PCI Express devices. *Note: Refer to the Direct Master Type 0 Configuration Cycle Example in Section 10.4.2.1, "Direct Master Configuration (PCI Type 0 or Type 1 Configuration Cycles)," for further details.*	Yes	Yes/Serial EEPROM	0

Register 20-53. PCI:F0h, LOC:170h LCS_LAS1RR Direct Slave Local Address Space 1 Range

Bit(s)	Description	Read	Write	Default
0	**Memory Space Indicator** Writing 0 indicates Local Address Space 1 maps into PCI Express Memory space. Writing 1 indicates Local Address Space 1 maps into PCI Express I/O space.	Yes	Yes/Serial EEPROM	0
2:1	When mapped into Memory space (**LCS_LAS1RR**[0]=0), the only valid value is 00b. Locate anywhere in PCI Express Address space. When mapped into I/O space (**LCS_LAS1RR**[0]=1), bit 1 must be cleared to 0. Bit 2 is included with **LCS_LAS1RR**[31:3] to indicate the decoding range.	Yes	Yes/Serial EEPROM	00b
3	When mapped into Memory space (**LCS_LAS1RR**[0]=0), writing 1 indicates reads are prefetchable (does not affect PEX 8311 operation, but is used for system status). When mapped into I/O space (**LCS_LAS1RR**[0]=1), included with **LCS_LAS1RR**[31:4, 2] to indicate the decoding range.	Yes	Yes/Serial EEPROM	0
31:4	Specifies which PCI Express Address bits to use for decoding a PCI access to Local Address Space 1. Each bit corresponds to a PCI Express Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others. (Used in conjunction with **LCS_PCIBAR3**.) Default is 1 MB. When I$_2$O Decode is enabled (**LCS_QSR**[0]=1), defines **LCS_PCIBAR0** (minimum range is 1,024 bytes). *Notes: LCS_LAS1RR range (**not** the Range register) must be power of 2. "Range register value" is two's complement of the range.* *Per PCI r2.2, limit I/O-Mapped spaces to 256 bytes per space.*	Yes	Yes/Serial EEPROM	FFF0_000h

Register 20-54. PCI:F4h, LOC:174h LCS_LAS1BA Direct Slave Local Address Space 1 Local Base Address (Remap)

Bit(s)	Description	Read	Write	Default
0	**Local Address Space 1 Enable** Writing 1 enables decoding of PCI Express Addresses for Direct Slave access to Local Address Space 1. Writing 0 disables decoding.	Yes	Yes/Serial EEPROM	0
1	*Reserved*	Yes	No	0
3:2	When Local Address Space 1 is mapped into Memory space (**LCS_LAS1RR**[0]=0), **LCS_LAS1BA**[3:2] must be 00b. When mapped into I/O space (**LCS_LAS1RR**[0]=1), included with **LCS_LAS1BA**[31:4] for remapping.	Yes	Yes/Serial EEPROM	00b
31:4	**Remap LCS_PCIBAR3 Base Address to Local Address Space 1 Base Address** The **LCS_PCIBAR3** Base address translates to the Local Address Space 1 Base Address programmed in this register. A Direct Slave access to an offset from **LCS_PCIBAR3** maps to the same offset from this Local Base address. *Note: Remap Address value must be a multiple of the **LCS_LAS1RR** range (**not** the Range register).*	Yes	Yes/Serial EEPROM	0h

Register 20-55. PCI:F8h, LOC:178h LCS_LBRD1 Local Address Space 1 Bus Region Descriptor

Bit(s)	Description	Read	Write	Default
1:0	**Local Address Space 1 Local Bus Data Width** Writing of the field value indicates the associated bus data width. 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes/Serial EEPROM	11b
5:2	**Local Address Space 1 Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes/Serial EEPROM	0h
6	**Local Address Space 1 READY#/TA# Input Enable** **C and J Modes:** Writing 0 disables READY# input. Writing 1 enables READY# input. **M Mode:** Writing 0 disables TA# input. Writing 1 enables TA# input.	Yes	Yes/Serial EEPROM	1
7	**Local Address Space 1 Continuous Burst Enable** **C and J Modes:** Also referred to as the *BTERM# Input Enable* bit. When bursting is enabled (**LCS_LBRD1**[8]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, **LCS_LBRD1**[6]=1). *Note: Refer to Section 9.3.12, "Local Bus Direct Slave Data Transfer Modes," for further details.* **M Mode:** Also referred to as the *BI Mode* bit. When bursting is enabled (**LCS_LBRD1**[8]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. *Note: Refer to Section 9.3.12, "Local Bus Direct Slave Data Transfer Modes," for further details.*	Yes	Yes/Serial EEPROM	0
8	**Local Address Space 1 Burst Enable** Writing 1 enables bursting. Writing 0 disables bursting.	Yes	Yes/Serial EEPROM	0
9	**Local Address Space 1 Prefetch Disable** When mapped into Memory space (**LCS_LAS1RR**[0]=0), writing 0 enables Read prefetching. Writing 1 disables prefetching. When prefetching is disabled, the PEX 8311 disconnects after each Memory read.	Yes	Yes/Serial EEPROM	0
10	**Local Address Space 1 Prefetch Counter Enable** 0 = PEX 8311 ignores the count and continues prefetching as follows: • **If PCI Read No Flush mode is enabled (LCS_MARBR[28]=1)** – Continues prefetching until the Direct Slave Read FIFO is full, or • **If PCI Read No Flush mode is disabled (LCS_MARBR[28]=0)** – Continues prefetching until PCI Read Completion, at which time the Direct Slave Read FIFO is flushed. 1, and Memory prefetching is enabled = PEX 8311 prefetches up to the number of Dwords specified in the Prefetch Counter (**LCS_LBRD1**[14:11])	Yes	Yes/Serial EEPROM	0
14:11	**Local Address Space 1 Prefetch Counter** Number of Dwords to prefetch during Memory Read cycles (0 to 15). A count of zero selects a prefetch of 16 Dwords.	Yes	Yes/Serial EEPROM	0h
31:15	*Reserved*	Yes	No	0h

Register 20-56. PCI:FCh, LOC:17Ch LCS_DMDAC Direct Master PCI Express Dual Address Cycles Upper Address

Bit(s)	Description	Read	Write	Default
31:0	**Upper 32 Bits of PCI Express Dual Address Cycle PCI Express Address during Direct Master Cycles** 0h = PEX 8311 performs a 32-bit address Direct Master access	Yes	Yes	0h

Register 20-57. PCI:100h, LOC:1A0h LCS_PCIARB Internal Arbiter Control

Bit(s)	Description	Read	Write	Default
	Notes: *The fields in this register must remain at their default values during standard operation.* *This register **cannot** be accessed from the internal PCI Bus by an I/O access, because of the PCI r2.2 PCI I/O space 256-byte limitation.* *Serial EEPROMs should load only zeros (0) to this register.*			
3:0	***Reserved***	Yes	Local/ Serial EEPROM	0h
31:4	***Reserved***	Yes	No	0h

Register 20-58. PCI:104h, LOC:1A4h LCS_PABTADR PCI Abort Address

Bit(s)	Description	Read	Write	Default
	Note: *This register **cannot** be accessed from the internal PCI Bus by an I/O access, because of the PCI r2.2 PCI I/O space 256-byte limitation.*			
31:0	**Master/Target Abort Address** When a Master/Target Abort occurs, the PCI Express address wherein the abort occurred is written to this register.	Yes	No	0h

20.6   Runtime Registers

This section details the **LCS** Runtime registers. Table 20-4 defines the register map.

Note: *"Yes" in the register Read and Write columns indicates the register is writable by the PCI Express interface and Local Bus.*

Table 20-4.   Runtime Register Map

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits. 31 16 15 8 7 0			PCI/Local Writable	Serial EEPROM Writable
40h	C0h	Mailbox 0 (refer to Notes)			Yes	Yes
44h	C4h	Mailbox 1 (refer to Notes)			Yes	Yes
48h	C8h	Mailbox 2			Yes	No
4Ch	CCh	Mailbox 3			Yes	No
50h	D0h	Mailbox 4			Yes	No
54h	D4h	Mailbox 5			Yes	No
58h	D8h	Mailbox 6			Yes	No
5Ch	DCh	Mailbox 7			Yes	No
60h	E0h	PCI Express-to-Local Doorbell			Yes	No
64h	E4h	Local-to-PCI Express Doorbell			Yes	No
68h	E8h	Interrupt Control/Status			Yes	No
6Ch	ECh	Serial EEPROM Control, PCI Command Codes, User I/O Control, and Init Control			Yes	No
70h	F0h	Device ID	Vendor ID		No	No
74h	F4h	*Reserved*		PCI Hardwired Revision ID	No	No
78h	C0h	Mailbox 0 (refer to Notes)			Yes	Yes
7Ch	C4h	Mailbox 1 (refer to Notes)			Yes	Yes

Notes: *The **LCS_MBOX0** register is always accessible at PCI Express address 78h, Local address C0h.*
*The **LCS_MBOX1** register is always accessible at PCI Express address 7Ch, Local address C4h.*

*When I$_2$O Decode is disabled (**LCS_QSR**[0]=0), **LCS_MBOX0** and **LCS_MBOX1** are also accessible at PCI Express addresses 40h and 44h for PCI 9054 compatibility. When I$_2$O Decode is enabled (**LCS_QSR**[0]=1), the Inbound and Outbound Queue pointers are accessed at PCI Express addresses 40h and 44h, replacing **LCS_MBOX0** and **LCS_MBOX1** in PCI Express Address space.*

Refer to the individual register descriptions to determine which bits are writable.

Register 20-59. PCI:40h or 78h, LOC:C0h LCS_MBOX0 Mailbox 0

Bit(s)	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register** *Note:* The **Inbound Queue Port** *register (**LCS_IQP**) replaces this register at PCI:40h when I₂O Decode is enabled (**LCS_QSR**[0]=1). **LCS_MBOX0** is always accessible at PCI Express address 78h and Local address C0h. Refer to Section 16.2.10, "I₂O Enable Sequence," for further details.*	Yes	Yes/Serial EEPROM	0h

Register 20-60. PCI:44h or 7Ch, LOC:C4h LCS_MBOX1 Mailbox 1

Bit(s)	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register** *Note:* The **Outbound Queue Port** *register (**LCS_OQP**) replaces this register at PCI:44h when I₂O Decode is enabled (**LCS_QSR**[0]=1). **LCS_MBOX1** is always accessible at PCI Express address 7Ch and Local address C4h. Refer to Section 16.2.10, "I₂O Enable Sequence," for further details.*	Yes	Yes/Serial EEPROM	0h

Register 20-61. PCI:48h, LOC:C8h LCS_MBOX2 Mailbox 2

Bit(s)	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 20-62. PCI:4Ch, LOC:CCh LCS_MBOX3 Mailbox 3

Bit(s)	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 20-63. PCI:50h, LOC:D0h LCS_MBOX4 Mailbox 4

Bit(s)	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 20-64. PCI:54h, LOC:D4h LCS_MBOX5 Mailbox 5

Bit(s)	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 20-65. PCI:58h, LOC:D8h LCS_MBOX6 Mailbox 6

Bit(s)	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 20-66. PCI:5Ch, LOC:DCh LCS_MBOX7 Mailbox 7

Bit(s)	Description	Read	Write	Default
31:0	**32-Bit Mailbox Register**	Yes	Yes	0h

Register 20-67. PCI:60h, LOC:E0h LCS_P2LDBELL PCI Express-to-Local Doorbell

Bit(s)	Description	Read	Write	Default
31:0	**Doorbell Register** The internal PCI Bus Master can write to this register and assert a Local interrupt output (LINTo#) to the Local processor. The Local processor can then read this register to determine which *Doorbell* bit was set. The internal PCI Bus Master sets the doorbell by writing 1 to a particular bit. The Local processor can clear a *Doorbell* bit by writing 1 to that bit position.	Yes	Yes/Clr	0h

Register 20-68. PCI:64h, LOC:E4h LCS_L2PDBELL Local-to-PCI Express Doorbell

Bit	Description	Read	Write	Default
31:0	**Doorbell Register** The Local processor can write to this register and assert the internal PCI Wire interrupt (INTA#). The internal PCI Bus Master can then read this register to determine which *Doorbell* bit was set. The Local processor sets the doorbell by writing 1 to a particular bit. The internal PCI Bus Master can clear a *Doorbell* bit by writing 1 to that bit position.	Yes	Yes/Clr	0h

Register 20-69. PCI:68h, LOC:E8h LCS_INTCSR Interrupt Control/Status

Bit(s)	Description	Read	Write	Default
0	**Enable Interrupt Sources (Bit 0)** **C and J Modes:** Writing 1 enables LSERR# to assert upon detection of a Local Parity error or PCI Abort. *Note: Refer to Figure 12-2, "Local Interrupt and Error Sources – C and J Modes," for further details.* **M Mode:** Writing 1 enables the TEA# ball and enables LINTo# to be asserted upon detection of a Local Parity error. *Note: Refer to Figure 12-3, "Local Interrupt and Error Sources – M Mode," for further details.*	Yes	Yes	0
1	**Enable Interrupt Sources (Bit 1)** **C and J Modes:** Writing 1 enables LSERR# to assert upon detection of an internal SERR# assertion in Root Complex mode, or detection of a PCI Parity error or a messaging queue outbound overflow. *Note: Refer to Figure 12-2, "Local Interrupt and Error Sources – C and J Modes," for further details.* **M Mode:** Writing 1 enables LINTo# to be asserted upon detection of an internal SERR# assertion in Root Complex mode, or detection of a PCI Parity error or a messaging queue outbound overflow. *Note: Refer to Figure 12-3, "Local Interrupt and Error Sources – M Mode," for further details.*	Yes	Yes	0
2	**Generate Internal PCI Bus Internal SERR# Interrupt** 0 = Writing 1 asserts the internal SERR# interrupt	Yes	Yes	0
3	**Mailbox Interrupt Enable** Writing 1 enables a Local interrupt output (LINTo#) to assert when the internal PCI Bus writes to LCS_MBOX0 through LCS_MBOX3. To clear a LINTo# interrupt, the Local Bus Master must read the Mailbox. Used in conjunction with the *Local Interrupt Output Enable* bit (**LCS_INTCSR**[16]).	Yes	Yes	0

Register 20-69. PCI:68h, LOC:E8h LCS_INTCSR Interrupt Control/Status (Cont.)

Bit(s)	Description	Read	Write	Default
4	**Power Management Interrupt Enable** Writing 1 enables a Local interrupt output (LINTo#) to assert when the Power Management Power State changes.	Yes	Yes	0
5	**Power Management Interrupt** 1 = Indicates a Power Management interrupt is pending. A Power Management interrupt is caused by a change in the **LCS Power Management Control/Status** register *Power State* field (LCS_PMCSR[1:0]). Writing 1 clears the interrupt. Writable from the internal PCI Bus only in the D0 power state.	Yes	Yes/Clr	0
6	**Direct Master Write/Direct Slave Read Local Data Parity Check Error Enable** **C and J Modes:** Writing 1 enables a Local Bus Data Parity Error signal to assert through the LSERR# ball. **LCS_INTCSR**[0] must be enabled for this to have an effect. **M Mode:** Writing 1 enables a Local Bus Data Parity Error signal to be asserted through the LINTo# ball. **LCS_INTCSR**[0] must be enabled for this to have an effect.	Yes	Yes	0
7	**Direct Master Write/Direct Slave Read Local Data Parity Check Error Status** 1 = Indicates the PEX 8311 detected a Local Data Parity Check error, regardless of whether bit 6 (*Parity Check Error*) is disabled (cleared to 0). Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
8	**Internal PCI Wire Interrupt Enable** Writing 1 enables internal PCI Wire interrupts (INTA#).	Yes	Yes	1
9	**PCI Express Doorbell Interrupt Enable** Writing 1 enables Local-to-PCI Express Doorbell interrupts. Used in conjunction with bit 8 (*Internal PCI Wire Interrupt Enable*). Clearing the **LCS_L2PDBELL** register bits that caused the interrupt also clears the interrupt.	Yes	Yes	0
10	**PCI Abort Interrupt Enable** Used in conjunction with bit 8 (*Internal PCI Wire Interrupt Enable*). Clearing the *Received Master Abort* and *Received Target Abort* bits (LCS_PCISR[13:12], respectively) also clears the PCI interrupt. 1 = Enables a Master Abort or Master detection of a Target Abort to assert the internal PCI Wire interrupt (INTA#).	Yes	Yes	0
11	**Local Interrupt Input Enable** Writing 1 enables a Local interrupt input (LINTi#) assertion to assert the internal PCI Wire interrupt (INTA#). Used in conjunction with bit 8 (*Internal PCI Wire Interrupt Enable*). De-asserting LINTi# also clears the interrupt.	Yes	Yes	0

Register 20-69. PCI:68h, LOC:E8h LCS_INTCSR Interrupt Control/Status (Cont.)

Bit(s)	Description	Read	Write	Default
12	**Retry Abort Enable** Writing 0 enables the PEX 8311 to indefinitely attempt Master Retrys. Writing 1 enables the PEX 8311 to treat 256 consecutive internal Master Retrys to a Target (PCI Express Address space) as a Target Abort.	Yes	Yes	0
13	**PCI Express Doorbell Interrupt Active** 1 = Indicates the PCI Express Doorbell interrupt is active	Yes	No	0
14	**PCI Abort Interrupt Active** 1 = Indicates the PCI Master or Target Abort interrupt is active	Yes	No	0
15	**Local Interrupt Input Active** 1 = Indicates the Local interrupt input (LINTi#) is active	Yes	No	0
16	**Local Interrupt Output Enable** Writing 1 enables Local interrupt output (LINTo#).	Yes	Yes	1
17	**Local Doorbell Interrupt Enable** Writing 1 enables PCI Express-to-Local Doorbell interrupts. Used in conjunction with bit 16 (*Local Interrupt Output Enable*). Clearing the LCS_P2LDBELL register bits that caused the interrupt also clears the interrupt.	Yes	Yes	0
18	**DMA Channel 0 Interrupt Enable** Writing 1 enables DMA Channel 0 interrupts. Used in conjunction with the *DMA Channel 0 Interrupt Select* bit (LCS_DMAMODE0[17]). Setting the *DMA Channel 0 Clear Interrupt* bit (LCS_DMACSR0[3]=1) also clears the interrupt.	Yes	Yes	0
19	**DMA Channel 1 Interrupt Enable** Writing 1 enables DMA Channel 1 interrupts. Used in conjunction with the *DMA Channel 1 Interrupt Select* bit (LCS_DMAMODE1[17]). Setting the *DMA Channel 1 Clear Interrupt* bit (LCS_DMACSR1[3]=1) also clears the interrupt.	Yes	Yes	0
20	**Local Doorbell Interrupt Active** Reading 1 indicates that the Local Doorbell interrupt is active.	Yes	No	0
21	**DMA Channel 0 Interrupt Active** Reading 1 indicates that the DMA Channel 0 interrupt is active.	Yes	No	0
22	**DMA Channel 1 Interrupt Active** Reading 1 indicates that the DMA Channel 1 interrupt is active.	Yes	No	0
23	**Built-In Self-Test (BIST) Interrupt Active** Reading 1 indicates the BIST interrupt is active. The BIST interrupt is enabled by writing 1 to the *PCI Built-In Self-Test Interrupt Enable* bit (LCS_PCIBISTR[6]=1). Clearing the *Enable* bit (**LCS_PCIBISTR**[6]=0) also clears the interrupt. *Note: Refer to the LCS_PCIBISTR register for a description of the self-test.*	Yes	No	0

Register 20-69. PCI:68h, LOC:E8h LCS_INTCSR Interrupt Control/Status (Cont.)

Bit(s)	Description	Read	Write	Default
24	Reading 0 indicates the Direct Master was the Bus Master during a Master or Target Abort.	Yes	No	1
25	Reading 0 indicates that DMA Channel 0 was the Bus Master during a Master or Target Abort.	Yes	No	1
26	Reading 0 indicates that DMA Channel 1 was the Bus Master during a Master or Target Abort.	Yes	No	1
27	Reading 0 indicates that the PEX 8311 asserted a Target Abort after internal 256 consecutive Master Retrys to a Target (PCI Express Address spaces).	Yes	No	1
28	Reading 1 indicates that the internal PCI Bus wrote data to LCS_MBOX0. Enabled only when the *Mailbox Interrupt Enable* bit is set (**LCS_INTCSR**[3]=1).	Yes	No	0
29	Reading 1 indicates that the internal PCI Bus wrote data to LCS_MBOX1. Enabled only when the *Mailbox Interrupt Enable* bit is set (**LCS_INTCSR**[3]=1).	Yes	No	0
30	Reading 1 indicates that the internal PCI Bus wrote data to LCS_MBOX2. Enabled only when the *Mailbox Interrupt Enable* bit is set (**LCS_INTCSR**[3]=1).	Yes	No	0
31	Reading 1 indicates that the internal PCI Bus wrote data to LCS_MBOX3. Enabled only when the *Mailbox Interrupt Enable* bit is set (**LCS_INTCSR**[3]=1).	Yes	No	0

Register 20-70. PCI:6Ch, LOC:ECh LCS_CNTRL Serial EEPROM Control, PCI Command Codes, User I/O Control, and Init Control

Bit(s)	Description	Read	Write	Default
3:0	**PCI Read Command Code for DMA**	Yes	Yes	1110b
7:4	**PCI Write Command Code for DMA**	Yes	Yes	0111b
11:8	**PCI Express Memory Read Command Code for Direct Master**	Yes	Yes	0110b
15:12	**PCI Express Memory Write Command Code for Direct Master**	Yes	Yes	0111b
16	**General-Purpose Output** Writing 0 causes USERo to go Low. Writing 1 causes USERo to go High.	Yes	Yes	1
17	**General-Purpose Input** Reading 0 indicates the USERi ball is Low. Reading 1 indicates the USERi ball is High.	Yes	No	–
18	**USERi or LLOCKi# Ball Select** Writing 0 selects LLOCKi# as an input to the PEX 8311. Writing 1 selects USERi as an input to the PEX 8311.	Yes	Yes	1
19	**USERo or LLOCKo# Ball Select** Writing 0 selects LLOCKo# as an output from the PEX 8311. Writing 1 selects USERo as an output from the PEX 8311.	Yes	Yes	1
20	**LINTo# Interrupt Status** When ROOT_COMPLEX# is enabled, reading 1 indicates the LINTo# interrupt is active by way of the internal PCI Wire interrupt (INTA#). Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
21	**LSERR#/TEA# Interrupt Status** **C and J Modes:** When ROOT_COMPLEX# is enabled, reading 1 indicates the LSERR# interrupt is active by way of the internal SERR# System error. Writing 1 clears this bit to 0. **M Mode:** When ROOT_COMPLEX# is enabled, reading 1 indicates the TEA# interrupt is active by way of the internal SERR# System error. Writing 1 clears this bit to 0.	Yes	Yes/Clr	0
23:22	*Reserved*	Yes	No	00b

Register 20-70. PCI:6Ch, LOC:ECh LCS_CNTRL Serial EEPROM Control, PCI Command Codes, User I/O Control, and Init Control (Cont.)

Bit(s)	Description	Read	Write	Default
24	**Serial EEPROM Clock for PCI or Local Bus Reads or Writes to Serial EEPROM (EESK)** Toggling this bit toggles the serial EEPROM Clock output.	Yes	Yes	0
25	**Serial EEPROM Chip Select (EECS)** For PCI or Local Bus Reads or Writes to the serial EEPROM, setting this bit to 1 provides the serial EEPROM Chip Select output.	Yes	Yes	0
26	**Write Bit to Serial EEPROM (EEDI)** For Writes, the EEDI output signal is input to the serial EEPROM. Clocked into the serial EEPROM by the serial EEPROM clock. *Note: Refer to Section 4.3.3, "Serial EEPROM Access," for further details.*	Yes	Yes	0
27	**Read Bit from Serial EEPROM (EEDO)** *Note: Refer to Section 4.3.3, "Serial EEPROM Access," for details.*	Yes	No	–
28	**Serial EEPROM Present** 1 = Indicates that a blank or programmed serial EEPROM is present (serial EEPROM *Start* bit is detected)	Yes	No	0
29	**Reload Configuration Registers** 0 = Writing 1 causes the PEX 8311 to reload the **LCS Configuration** registers from the serial EEPROM *Note: This bit is not self-clearing.*	Yes	Yes	0
30	**Local Bus Reset (Endpoint Mode)** Writing 1 holds the PEX 8311 Local Bus logic in a Reset state, and asserts LRESET# output. Contents of the **PCI Configuration** and **Runtime** registers are not reset. A Local Bus Reset is cleared only from the internal PCI Bus. **PCI Express Bridge Reset (Root Complex Mode)** Writing 1 holds the PEX 8311 internal PCI Bus logic and DMA Configuration registers in a Reset state, and asserts PERST# output. Contents of the **LCS Configuration**, **Runtime**, and **Messaging Queue** registers are not reset. A PCI Express Bridge Reset is cleared only from the Local Bus.	Yes	Yes	0
31	**EEDO Input Enable** 0 = Allows VPD cycles to occur. 1 = EEDI/EEDO I/O buffer is placed in a bus high-impedance state, enabling the serial EEPROM data to be read. The serial EEPROM data resides in **LCS_CNTRL**[27].	Yes	Yes	0

Register 20-71. PCI:70h, LOC:F0h LCS_PCIHIDR PCI Hardwired Configuration ID

Bit(s)	Description	Read	Write	Default
15:0	**Vendor ID** Identifies the device manufacturer. Hardwired to the PLX PCI-SIG-assigned Vendor ID, 10B5h.	Yes	No	10B5h
31:16	**Device ID** Identifies the particular device. Hardwired to 9056h.	Yes	No	9056h

Register 20-72. PCI:74h, LOC:F4h LCS_PCIHREV PCI Hardwired Revision ID

Bit(s)	Description	Read	Write	Default
7:0	**Revision ID** Hardwired Silicon Revision of the PEX 8311 Local Bus logic.	Yes	No	BAh

20.7   DMA Registers

This section details the **LCS** DMA registers. Table 20-5 defines the register map.

Note: "Yes" in the register Read and Write columns indicates the register is writable by the PCI Express interface and Local Bus.

Table 20-5.   DMA Register Map

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits.			PCI/Local Writable	Serial EEPROM Writable
		31	**16 15**	**8 7 0**		
80h	100h	DMA Channel 0 Mode			Yes	No
84h/88h‡	104h/108h‡	DMA Channel 0 PCI Express Address			Yes	No
88h/8Ch‡	108h/10Ch‡	DMA Channel 0 Local Address			Yes	No
8Ch/84h‡	10Ch/104h‡	DMA Channel 0 Transfer Size (Bytes)			Yes	No
90h	110h	DMA Channel 0 Descriptor Pointer			Yes	No
94h	114h	DMA Channel 1 Mode			Yes	No
98h/9Ch‡	118h/11Ch‡	DMA Channel 1 PCI Express Address			Yes	No
9Ch/A0h‡	11Ch/120h‡	DMA Channel 1 Local Address			Yes	No
A0h/98h‡	120h/118h‡	DMA Channel 1 Transfer Size (Bytes)			Yes	No
A4h	124h	DMA Channel 1 Descriptor Pointer			Yes	No
A8h	128h	*Reserved*	DMA Channel 1 Command/ Status	DMA Channel 0 Command/ Status	Yes	No
ACh	12Ch	DMA Arbitration			Yes	Yes
B0h	130h	DMA Threshold			Yes	No
B4h	134h	DMA Channel 0 PCI Express Dual Address Cycle Upper Address			Yes	No
B8h	138h	DMA Channel 1 PCI Express Dual Address Cycle Upper Address			Yes	No

*Notes: ‡ PCI and Local Configuration offset depends upon the **LCS_DMAMODE0/1**[20] setting(s).*

Refer to the individual register descriptions to determine which bits are writable.

Register 20-73. PCI:80h, LOC:100h LCS_DMAMODE0 DMA Channel 0 Mode

Bit(s)	Description	Read	Write	Value after Reset
1:0	**DMA Channel 0 Local Bus Data Width** Writing of the field value indicates the associated bus data width. 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes	11b
5:2	**DMA Channel 0 Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes	0h
6	**DMA Channel 0 READY#/TA# Input Enable** **C and J Modes:** Writing 0 disables READY# input. Writing 1 enables READY# input. **M Mode:** Writing 0 disables TA# input. Writing 1 enables TA# input.	Yes	Yes	1
7	**DMA Channel 0 Continuous Burst Enable** **C and J Modes:** Also referred to as the *BTERM# Input Enable* bit. When bursting is enabled (**LCS_DMAMODE0**[8]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, **LCS_DMAMODE0**[6]=1). *Note: Refer to Section 9.5.19, "Local Bus DMA Data Transfer Modes," for further details.* **M Mode:** Also referred to as the *BI Mode* bit. When bursting is enabled (**LCS_DMAMODE0**[8]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. *Note: Refer to Section 9.5.19, "Local Bus DMA Data Transfer Modes," for further details.*	Yes	Yes	0
8	**DMA Channel 0 Local Burst Enable** Writing 0 disables Local bursting. Writing 1 enables Local bursting.	Yes	Yes	0
9	**DMA Channel 0 Scatter/Gather Mode** Writing 0 indicates that DMA Block mode is enabled. Writing 1 indicates that DMA Scatter/Gather mode is enabled. For Scatter/Gather mode, the DMA source and destination addresses and Byte Count are loaded from memory in PCI or Local Address spaces.	Yes	Yes	0
10	**DMA Channel 0 Done Interrupt Enable** Writing 0 disables an interrupt when done. Writing 1 enables an interrupt when done. When DMA Clear Count mode is enabled (**LCS_DMAMODE0**[16]=1), the interrupt does not occur until the Byte Count is cleared.	Yes	Yes	0
11	**DMA Channel 0 Local Addressing Mode** Writing 0 indicates the Local Address is incremented. Writing 1 holds the Local Address Bus constant.	Yes	Yes	0

Register 20-73. PCI:80h, LOC:100h LCS_DMAMODE0 DMA Channel 0 Mode (Cont.)

Bit(s)	Description	Read	Write	Value after Reset
12	**DMA Channel 0 Demand Mode** Writing 1 causes the DMA Channel 0 DMA Controller to operate in Demand mode. In Demand mode, the DMA Controller transfers data when its DREQ0# input is asserted. Asserts DACK0# to indicate that the current Local Bus transfer is in response to DREQ0# input. The DMA Controller transfers Dwords (32 bits) of data. This could result in multiple transfers for an 8- or 16-bit bus.	Yes	Yes	0
13	**DMA Channel 0 Memory Write and Invalidate Mode for DMA Transfers** The PEX 8311 supports Memory Write and Invalidate sizes of 8 or 16 Dwords. The size is specified in the *System Cache Line Size* field (LCS_PCICLSR[7:0]). When a size other than 8 or 16 is specified, the PEX 8311 performs Write transfers, rather than Memory Write and Invalidate transfers. Transfers must start and end at Cache Line boundaries. LCS_PCICR[4] must be set to 1. 1 = PEX 8311 performs Memory Write and Invalidate cycles to the internal PCI Bus	Yes	Yes	0
14	**DMA Channel 0 EOT# Enable** Writing 0 disables the EOT# input ball. Writing 1 enables the EOT# input ball. When **LCS_DMAMODE0**[14] and LCS_DMAMODE1[14]=00b, the EOT# ball becomes the DMPAF ball.	Yes	Yes	0
15	**DMA Channel 0 Fast/Slow Terminate Mode Select** **C and J Modes:** Writing 0 sets the PEX 8311 into Slow Terminate mode. As a result, BLAST# is asserted on the last Data transfer to terminate the DMA transfer. Writing 1 sets the PEX 8311 into Fast Terminate mode, and indicates that the PEX 8311 DMA transfer immediately terminates when EOT# (if enabled) is asserted, or during DMA Demand mode when DREQ0# is de-asserted. **M Mode:** Writing 0 sets the PEX 8311 into Slow Terminate mode. As a result, BDIP# is de-asserted at the nearest 16-byte boundary and the DMA transfer stops. Writing 1 sets the PEX 8311 into Fast Terminate mode, and indicates that BDIP# output is disabled. As a result, the PEX 8311 DMA transfer immediately terminates when EOT# (if enabled) is asserted, or during DMA Demand mode when DREQ0# is de-asserted.	Yes	Yes	0

Register 20-73. PCI:80h, LOC:100h LCS_DMAMODE0 DMA Channel 0 Mode (Cont.)

Bit(s)	Description	Read	Write	Value after Reset
16	**DMA Channel 0 Clear Count Mode** Writing 1 clears the Byte Count in each Scatter/Gather descriptor when the corresponding DMA transfer is complete.	Yes	Yes	0
17	**DMA Channel 0 Interrupt Select** Writing 0 routes the DMA Channel 0 interrupt to the Local interrupt output (LINTo#)). Writing 1 routes the DMA Channel 0 interrupt to the internal PCI Wire interrupt (INTA#).	Yes	Yes	0
18	**DMA Channel 0 DAC Chain Load** 1 = Enables the descriptor to load the PCI Express Dual Address Cycles value. Otherwise, the descriptor loads the **LCS_DMADAC0** register contents.	Yes	Yes	0
19	**DMA Channel 0 EOT# End Link** Used only for Scatter/Gather DMA transfers. 0 = Indicates that when EOT# is asserted, the DMA transfer ends the current Scatter/Gather transfer and does not continue with the remaining Scatter/Gather transfers 1 = Indicates that when EOT# is asserted, the DMA transfer ends the current Scatter/Gather Link and continues with the remaining Scatter/Gather transfers	Yes	Yes	0
20	**DMA Channel 0 Ring Management Valid Mode Enable** 0 = Indicates that the *DMA Channel 0 Ring Management Valid* bit (LCS_DMASIZ0[31]) is ignored. 1 = Indicates that the DMA descriptors are processed only when the *DMA Channel 0 Ring Management Valid* bit is set (**LCS_DMASIZ0**[31]=1). When the *Valid* bit is set, the Terminal Count is 0, and the descriptor is not the last descriptor in the chain. The DMA Channel 0 DMA Controller then moves to the next descriptor in the chain. *Note: Descriptor Memory fields are re-ordered when this bit is set.*	Yes	Yes	0
21	**DMA Channel 0 Ring Management Valid Stop Control** 0 = Indicates that the Scatter/Gather DMA Controller continuously polls a descriptor with the *Valid* bit cleared to 0 (invalid descriptor) when Ring Management Valid mode is enabled (bit 20 is set to 1). 1 = Indicates the Scatter/Gather Controller stops polling when the *DMA Channel 0 Ring Management Valid* bit with a value of 0 is detected (**LCS_DMASIZ0**[31]=0). In this case, the CPU must restart the DMA Channel 0 DMA Controller by setting the *DMA Channel 0 Start* bit (LCS_DMACSR0[1]=1). A pause clearing the *DMA Channel 0 Start* bit (**LCS_DMACSR0**[1]=0) sets the *DMA Channel 0 Done* bit (**LCS_DMACSR0**[4]=1).	Yes	Yes	0
31:22	*Reserved*	Yes	No	0h

Register 20-74. PCI:84h, LOC:104h when LCS_DMAMODE0[20]=0 or PCI:88h, LOC:108h when LCS_DMAMODE0[20]=1 LCS_DMAPADR0 DMA Channel 0 PCI Express Address

Bit(s)	Description	Read	Write	Default
31:0	**DMA Channel 0 PCI Express Address** Indicates from where in PCI Express Memory space DMA transfers (Reads or Writes) start. Value is a physical address.	Yes	Yes	0h

Register 20-75. PCI:88h, LOC:108h when LCS_DMAMODE0[20]=0 or PCI:8Ch, LOC:10Ch when LCS_DMAMODE0[20]=1 LCS_DMALADR0 DMA Channel 0 Local Address

Bit(s)	Description	Read	Write	Default
31:0	**DMA Channel 0 Local Address** Indicates from where in Local Memory space DMA transfers (Reads or Writes) start.	Yes	Yes	0h

Register 20-76. PCI:8Ch, LOC:10Ch when LCS_DMAMODE0[20]=0 or PCI:84h, LOC:104h when LCS_DMAMODE0[20]=1 LCS_DMASIZ0 DMA Channel 0 Transfer Size (Bytes)

Bit(s)	Description	Read	Write	Default
22:0	**DMA Channel 0 Transfer Size (Bytes)** Indicates the number of bytes to transfer during a DMA operation.	Yes	Yes	0h
30:23	*Reserved*	Yes	No	0h
31	**DMA Channel 0 Ring Management Valid** When Ring Management Valid mode is enabled (**LCS_DMAMODE0**[20]=1), indicates the validity of this DMA descriptor.	Yes	Yes	0

Register 20-77. PCI:90h, LOC:110h LCS_DMADPR0 DMA Channel 0 Descriptor Pointer

Bit(s)	Description	Read	Write	Default
0	**DMA Channel 0 Descriptor Location** Writing 0 indicates Local Address space. Writing 1 indicates PCI Express Address space.	Yes	Yes	0
1	**DMA Channel 0 End of Chain** Writing 0 indicates not end of chain descriptor. (Same as DMA Block mode.) Writing 1 indicates end of chain.	Yes	Yes	0
2	**DMA Channel 0 Interrupt after Terminal Count** Writing 0 disables interrupts from being asserted. Writing 1 causes an interrupt to assert after the Terminal Count for this descriptor is reached.	Yes	Yes	0
3	**DMA Channel 0 Direction of Transfer** Writing 0 indicates transfers from the internal PCI Bus to the Local Bus. Writing 1 indicates transfers from the Local Bus to the internal PCI Bus.	Yes	Yes	0
31:4	**DMA Channel 0 Next Descriptor Address** X0h-aligned (**LCS_DMADPR0**[3:0]=0h).	Yes	Yes	0h

Register 20-78. PCI:94h, LOC:114h LCS_DMAMODE1 DMA Channel 1 Mode

Bit(s)	Description	Read	Write	Default
1:0	**DMA Channel 1 Local Bus Data Width** Writing of the field value indicates the associated bus data width. 00b = 8 bit 01b = 16 bit 10b or 11b = 32 bit	Yes	Yes	11b
5:2	**DMA Channel 1 Internal Wait State Counter** Address-to-Data; Data-to-Data; 0 to 15 Wait States.	Yes	Yes	0h
6	**DMA Channel 1 READY#/TA# Input Enable** **C and J Modes:** Writing 0 disables READY# input. Writing 1 enables READY# input. **M Mode:** Writing 0 disables TA# input. Writing 1 enables TA# input.	Yes	Yes	1
7	**DMA Channel 1 Continuous Burst Enable** **C and J Modes:** Also referred to as the *BTERM# Input Enable* bit. When bursting is enabled (**LCS_DMAMODE1**[8]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. Writing 1 additionally enables BTERM# input, which when asserted overrides the READY# input state (when READY# is enabled, **LCS_DMAMODE1**[6]=1). *Note: Refer to Section 9.5.19, "Local Bus DMA Data Transfer Modes," for further details.* **M Mode:** Also referred to as the *BI Mode* bit. When bursting is enabled (**LCS_DMAMODE1**[8]=1), writing 0 enables Burst-4 mode and writing 1 enables Continuous Burst mode. *Note: Refer to Section 9.5.19, "Local Bus DMA Data Transfer Modes," for further details.*	Yes	Yes	0
8	**DMA Channel 1 Local Burst Enable** Writing 0 disables Local bursting. Writing 1 enables Local bursting.	Yes	Yes	0
9	**DMA Channel 1 Scatter/Gather Mode** Writing 0 indicates that DMA Block mode is enabled. Writing 1 indicates that DMA Scatter/Gather mode is enabled. For Scatter/Gather mode, the DMA source and destination addresses and Byte Count are loaded from memory in PCI or Local Address spaces.	Yes	Yes	0
10	**DMA Channel 1 Done Interrupt Enable** Writing 0 disables an interrupt when done. Writing 1 enables an interrupt when done. When DMA Clear Count mode is enabled (**LCS_DMAMODE1**[16]=1), the interrupt does not occur until the Byte Count is cleared.	Yes	Yes	0
11	**DMA Channel 1 Local Addressing Mode** Writing 0 indicates the Local Address is incremented. Writing 1 holds the Local Address Bus constant.	Yes	Yes	0

Register 20-78. PCI:94h, LOC:114h LCS_DMAMODE1 DMA Channel 1 Mode (Cont.)

Bit(s)	Description	Read	Write	Default
12	**DMA Channel 1 Demand Mode** Writing 1 causes the DMA Channel 1 DMA Controller to operate in Demand mode. In Demand mode, the DMA Controller transfers data when its DREQ1# input is asserted. Asserts DACK1# to indicate that the current Local Bus transfer is in response to DREQ1# input. The DMA Controller transfers Dwords (32 bits) of data. This could result in multiple transfers for an 8- or 16-bit bus.	Yes	Yes	0
13	**DMA Channel 1 Memory Write and Invalidate Mode for DMA Transfers** The PEX 8311 supports Memory Write and Invalidate sizes of 8 or 16 Dwords. The size is specified in the *System Cache Line Size* field (LCS_PCICLSR[7:0]). When a size other than 8 or 16 is specified, the PEX 8311 performs Write transfers, rather than Memory Write and Invalidate transfers. Transfers must start and end at Cache Line boundaries. LCS_PCICR[4] must be set to 1. 1 = PEX 8311 performs Memory Write and Invalidate cycles to the internal PCI Bus	Yes	Yes	0
14	**DMA Channel 1 EOT# Enable** Writing 0 disables the EOT# input ball. Writing 1 enables the EOT# input ball. When **LCS_DMAMODE0**[14] and **LCS_DMAMODE1**[14]=00b, the EOT# ball becomes the DMPAF ball.	Yes	Yes	0
15	**DMA Channel 1 Fast/Slow Terminate Mode Select** **C and J Modes:** Writing 0 sets the PEX 8311 into Slow Terminate mode. As a result, BLAST# is asserted on the last Data transfer to terminate the DMA transfer. Writing 1 sets the PEX 8311 into Fast Terminate mode, and indicates that the PEX 8311 DMA transfer immediately terminates when EOT# (if enabled) is asserted, or during DMA Demand mode when DREQ1# is de-asserted. **M Mode:** Writing 0 sets the PEX 8311 into Slow Terminate mode. As a result, BDIP# is de-asserted at the nearest 16-byte boundary and the DMA transfer stops. Writing 1 sets the PEX 8311 into Fast Terminate mode, and indicates that BDIP# output is disabled. As a result, the PEX 8311 DMA transfer immediately terminates when EOT# (if enabled) is asserted, or during DMA Demand mode when DREQ1# is de-asserted.	Yes	Yes	0

Register 20-78. PCI:94h, LOC:114h LCS_DMAMODE1 DMA Channel 1 Mode (Cont.)

Bit(s)	Description	Read	Write	Default
16	**DMA Channel 1 Clear Count Mode** Writing 1 clears the Byte Count in each Scatter/Gather descriptor when the corresponding DMA transfer is complete.	Yes	Yes	0
17	**DMA Channel 1 Interrupt Select** Writing 0 routes the DMA Channel 1 interrupt to the Local interrupt output (LINTo#). Writing 1 routes the DMA Channel 1 interrupt to the internal PCI Wire interrupt (INTA#).	Yes	Yes	0
18	**DMA Channel 1 DAC Chain Load** 1 = Enables the descriptor to load the PCI Express Dual Address Cycles value. Otherwise, the descriptor loads the **LCS_DMADAC1** register contents.	Yes	Yes	0
19	**DMA Channel 1 EOT# End Link** Used only for Scatter/Gather DMA transfers. 0 = Indicates indicates that when EOT# is asserted, the DMA transfer ends the current Scatter/Gather transfer and does not continue with the remaining Scatter/Gather transfers. 1 = Indicates that when EOT# is asserted, the DMA transfer ends the current Scatter/Gather Link and continues with the remaining Scatter/Gather transfers.	Yes	Yes	0
20	**DMA Channel 1 Ring Management Valid Mode Enable** 0 = Indicates that the *DMA Channel 1 Ring Management Valid* bit (LCS_DMASIZ1[31]) is ignored. 1 = Indicates that the DMA descriptors are processed only when the *DMA Channel 1 Ring Management Valid* bit is set (**LCS_DMASIZ1**[31]=1). When the *Valid* bit is set, the Terminal Count is 0, and the descriptor is not the last descriptor in the chain. The DMA Channel 1 DMA Controller then moves to the next descriptor in the chain. *Note: Descriptor Memory fields are re-ordered when this bit is set.*	Yes	Yes	0
21	**DMA Channel 1 Ring Management Valid Stop Control** 0 = Indicates that the Scatter/Gather DMA Controller continuously polls a descriptor with the *Valid* bit cleared to 0 (invalid descriptor) when Ring Management Valid mode is enabled (**LCS_DMAMODE1**[20]=1). 1 = Indicates the Scatter/Gather Controller stops polling when the *DMA Channel 1 Ring Management Valid* bit with a value of 0 is detected (**LCS_DMASIZ1**[31]=0). In this case, the CPU must restart the DMA Channel 1 DMA Controller by setting the *DMA Channel 1 Start* bit (LCS_DMACSR1[1]=1). A pause clearing the *DMA Channel 1 Start* bit (**LCS_DMACSR1**[1]=0) sets the *DMA Channel 1 Done* bit (**LCS_DMACSR1**[4]=1).	Yes	Yes	0
31:22	*Reserved*	Yes	No	0h

**Register 20-79. PCI:98h, LOC:118h when LCS_DMAMODE1[20]=0 or
PCI:9Ch, LOC:11Ch when LCS_DMAMODE1[20]=1 LCS_DMAPADR1
DMA Channel 1 PCI Express Address**

Bit(s)	Description	Read	Write	Default
31:0	**DMA Channel 1 PCI Express Address** Indicates from where in PCI Express Memory space DMA transfers (Reads or Writes) start. Value is a physical address.	Yes	Yes	0h

**Register 20-80. PCI:9Ch, LOC:11Ch when LCS_DMAMODE1[20]=0 or
PCI:A0h, LOC:120h when LCS_DMAMODE1[20]=1 LCS_DMALADR1
DMA Channel 1 Local Address**

Bit(s)	Description	Read	Write	Default
31:0	**DMA Channel 1 Local Address** Indicates from where in Local Memory space DMA transfers (Reads or Writes) start.	Yes	Yes	0h

**Register 20-81. PCI:A0h, LOC:120h when LCS_DMAMODE1[20]=0 or
PCI:98h, LOC:118h when LCS_DMAMODE1[20]=1 LCS_DMASIZ1
DMA Channel 1 Transfer Size (Bytes)**

Bit(s)	Description	Read	Write	Default
22:0	**DMA Channel 1 Transfer Size (Bytes)** Indicates the number of bytes to transfer during a DMA operation.	Yes	Yes	0h
30:23	*Reserved*	Yes	No	0h
31	**DMA Channel 1 Ring Management Valid** When Ring Management Valid mode is enabled (**LCS_DMAMODE1**[20]=1), indicates the validity of this DMA descriptor.	Yes	Yes	0

Register 20-82. PCI:A4h, LOC:124h LCS_DMADPR1 DMA Channel 1 Descriptor Pointer

Bit(s)	Description	Read	Write	Default
0	**DMA Channel 1 Descriptor Location** Writing 0 indicates Local Address space. Writing 1 indicates PCI Express Address space.	Yes	Yes	0
1	**DMA Channel 1 End of Chain** Writing 0 indicates not end of chain descriptor. (Same as DMA Block mode.) Writing 1 indicates end of chain.	Yes	Yes	0
2	**DMA Channel 1 Interrupt after Terminal Count** Writing 0 disables interrupts from being asserted. Writing 1 causes an interrupt to assert after the Terminal Count for this descriptor is reached.	Yes	Yes	0
3	**DMA Channel 1 Direction of Transfer** Writing 0 indicates transfers from the internal PCI Bus to the Local Bus. Writing 1 indicates transfers from the Local Bus to the internal PCI Bus.	Yes	Yes	0
31:4	**DMA Channel 1 Next Descriptor Address** X0h-aligned (**LCS_DMADPR1**[3:0]=0h).	Yes	Yes	0h

Register 20-83. PCI:A8h, LOC:128h LCS_DMACSR0 DMA Channel 0 Command/Status

Bit(s)	Description	Read	Write	Default
0	**DMA Channel 0 Enable** Writing 0 disables DMA Channel 0 from starting a DMA transfer, and when in the process of transferring data, suspends the transfer (pause). Writing 1 enables DMA Channel 0 to transfer data.	Yes	Yes	0
1	**DMA Channel 0 Start** Writing 1 causes DMA Channel 0 to start transferring data when the channel is enabled.	No	Yes/Set	0
2	**DMA Channel 0 Abort** Writing 1 causes DMA Channel 0 to abort the current transfer. Bit 0 (*DMA Channel 0 Enable*) must be cleared to 0. Sets bit 4 (*DMA Channel 0 Done*) to 1 when the abort is complete.	No	Yes/Set	0
3	**DMA Channel 0 Clear Interrupt** Writing 1 clears DMA Channel 0 interrupts.	No	Yes/Clr	0
4	**DMA Channel 0 Done** Reading 0 indicates the Channel transfer is not complete. Reading 1 indicates the transfer is complete. The transfer is complete because the DMA transfer finished successfully, or the DMA transfer was aborted when software set bit 2 (*DMA Channel 0 Abort*) to 1.	Yes	No	1
7:5	*Reserved*	Yes	No	000b

Register 20-84. PCI:A9h, LOC:129h LCS_DMACSR1 DMA Channel 1 Command/Status

Bit(s)	Description	Read	Write	Default
0	**DMA Channel 1 Enable** Writing 0 disables DMA Channel 1 from starting a DMA transfer, and when in the process of transferring data, suspends the transfer (pause). Writing 1 enables DMA Channel 1 to transfer data.	Yes	Yes	0
1	**DMA Channel 1 Start** Writing 1 causes DMA Channel 1 to start transferring data when the channel is enabled.	No	Yes/Set	0
2	**DMA Channel 1 Abort** Writing 1 causes DMA Channel 1 to abort the current transfer. Bit 0 (*DMA Channel 1 Enable*) must be cleared to 0. Sets bit 4 (*DMA Channel 1 Done*) to 1 when the abort is complete.	No	Yes/Set	0
3	**DMA Channel 1 Clear Interrupt** Writing 1 clears DMA Channel 1 interrupts.	No	Yes/Clr	0
4	**DMA Channel 1 Done** Reading 0 indicates the Channel transfer is not complete. Reading 1 indicates the transfer is complete. The transfer is complete because the DMA transfer finished successfully, or the DMA transfer was aborted when software set bit 2 (*DMA Channel 1 Abort*) to 1.	Yes	No	1
7:5	*Reserved*	Yes	No	000b

Register 20-85. PCI:ACh, LOC:12Ch LCS_DMAARB DMA Arbitration

Same as Register 20-40, **LCS_MARBR**.

Register 20-86. PCI:B0h, LOC:130h LCS_DMATHR DMA Threshold

Bit(s)	Description	Read	Write	Default
3:0	**DMA Channel 0 PCI Express-to-Local Almost Full (C0PLAF)** Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for writes. Nibble values 0h through Eh are used. (Refer to Table 20-6.) Value of Fh is *reserved*. (15 - C0PLAF) > C0LPAE.	Yes	Yes	0h
7:4	**DMA Channel 0 Local-to-PCI Express Almost Empty (C0LPAE)** Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for reads. Nibble values 0h through Eh are used. (Refer to Table 20-6.) Value of Fh is *reserved*. (15 - C0PLAF) > C0LPAE.	Yes	Yes	0h
11:8	**DMA Channel 0 Local-to-PCI Express Almost Full (C0LPAF)** Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the internal PCI Bus for writes. Nibble values 0h through Eh are used. (Refer to Table 20-6.) Value of Fh is *reserved*.	Yes	Yes	0h
15:12	**DMA Channel 0 PCI Express-to-Local Almost Empty (C0PLAE)** Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the internal PCI Bus for reads. Nibble values 0h through Eh are used. (Refer to Table 20-6.) Value of Fh is *reserved*.	Yes	Yes	0h
19:16	**DMA Channel 1 PCI Express-to-Local Almost Full (C1PLAF)** Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for writes. Nibble values 0h through Eh are used. (Refer to Table 20-6.) Value of Fh is *reserved*. (15 - C1PLAF) > C1LPAE.	Yes	Yes	0h
23:20	**DMA Channel 1 Local-to-PCI Express Almost Empty (C1LPAE)** Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the Local Bus for reads. Nibble values 0h through Eh are used. (Refer to Table 20-6.) Value of Fh is *reserved*. (15 - C1PLAF) > C1LPAE.	Yes	Yes	0h
27:24	**DMA Channel 1 Local-to-PCI Express Almost Full (C1LPAF)** Number of full (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the internal PCI Bus for writes. Nibble values 0h through Eh are used. (Refer to Table 20-6.) Value of Fh is *reserved*.	Yes	Yes	0h
31:28	**DMA Channel 1 PCI Express-to-Local Almost Empty (C1PLAE)** Number of empty (Dword x 2) entries (plus 1, times 2) in the FIFO before requesting the internal PCI Bus for reads. Nibble values 0h through Eh are used. (Refer to Table 20-6.) Value of Fh is *reserved*.	Yes	Yes	0h

Nibble values 0h through Eh are used to set the number of full or empty Dword entries for each 4-bit field of the **LCS_DMATHR** register, as defined in Table 20-6.

Table 20-6. LCS_DMATHR Nibble Values

Nibble Value	Setting	Nibble Value	Setting	Nibble Value	Setting
0h	4 Dwords	5h	24 Dwords	Ah	44 Dwords
1h	8 Dwords	6h	28 Dwords	Bh	48 Dwords
2h	12 Dwords	7h	32 Dwords	Ch	52 Dwords
3h	16 Dwords	8h	38 Dwords	Dh	58 Dwords
4h	20 Dwords	9h	40 Dwords	Eh	60 Dwords

Register 20-87. PCI:B4h, LOC:134h LCS_DMADAC0 DMA Channel 0 PCI Express Dual Address Cycle Upper Address

Bit(s)	Description	Read	Write	Default
31:0	**Upper 32 Bits of the PCI Express Dual Address Cycle PCI Express Address during DMA Channel 0 Cycles** 0h = PEX 8311 performs a 32-bit address DMA Channel 0 access	Yes	Yes	0h

Register 20-88. PCI:B8h, LOC:138h LCS_DMADAC1 DMA Channel 1 PCI Express Dual Address Cycle Upper Address

Bit(s)	Description	Read	Write	Default
31:0	**Upper 32 Bits of the PCI Express Dual Address Cycle PCI Express Address during DMA Channel 1 Cycles** 0h = PEX 8311 performs a 32-bit address DMA Channel 1 access	Yes	Yes	0h

20.8   Messaging Queue (I$_2$O) Registers

This section details the **LCS** Messaging Queue (I$_2$O) registers. Table 20-7 defines the register map.

Note: *"Yes" in the register Read and Write columns indicates the register is writable by the
PCI Express interface and Local Bus.*

Table 20-7.   Messaging Queue (I$_2$O) Register Map

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PEX 8311 family and to ensure compatibility with future enhancements, write 0 to all unused bits.		PCI/Local Writable	Serial EEPROM Writable
		31 24 23 16 15 8 7 0			
30h	B0h	Outbound Post Queue Interrupt Status		No	No
34h	B4h	Outbound Post Queue Interrupt Mask		Yes	No
40h	–	Inbound Queue Port		PCI	No
44h	–	Outbound Queue Port		PCI	No
C0h	140h	Messaging Queue Configuration		Yes	No
C4h	144h	Queue Base Address		Yes	No
C8h	148h	Inbound Free Head Pointer		Yes	No
CCh	14Ch	Inbound Free Tail Pointer		Yes	No
D0h	150h	Inbound Post Head Pointer		Yes	No
D4h	154h	Inbound Post Tail Pointer		Yes	No
D8h	158h	Outbound Free Head Pointer		Yes	No
DCh	15Ch	Outbound Free Tail Pointer		Yes	No
E0h	160h	Outbound Post Head Pointer		Yes	No
E4h	164h	Outbound Post Tail Pointer		Yes	No
E8h	168h	*Reserved*	Queue Status/ Control	Yes	No

Notes: *When I$_2$O Decode is enabled (**LCS_QSR**[0]=1), the PCI Express Root Complex or other IOP uses the
Inbound Queue Port to read Message Frame Addresses (MFAs) from the Inbound Free List FIFO and to
write MFAs to the Inbound Post Queue FIFO. The Outbound Queue Port reads MFAs from the Outbound
Post Queue FIFO and writes MFAs to the Outbound Free List FIFO.*

*Each Inbound MFA is specified by I$_2$O as an offset from the PCI Express Memory Base address (programmed
in **LCS_PCIBAR0**) to the start of the message frame. That is, all inbound message frames reside in
LCS_PCIBAR0 Memory space.*

*Each Outbound MFA is specified by I$_2$O as an offset from system address 0000_0000h. Outbound MFA
is a physical 32-bit address of the frame in shared PCI Express system memory.*

*The Inbound and Outbound queues can reside in Local Address Space 0 or Space 1 by programming **LCS_QSR**.
The queues need not be in shared memory.*

Refer to the individual register descriptions to determine which bits are writable.

Register 20-89. PCI:30h, LOC:B0h LCS_OPQIS Outbound Post Queue Interrupt Status

Bit(s)	Description	Read	Write	Default
2:0	*Reserved*	Yes	No	000b
3	**Outbound Post Queue Interrupt** Set when the Outbound Post queue is not empty. Not affected by the *Outbound Post Queue Interrupt Mask* bit (LCS_OPQIM[3]) state.	Yes	No	0
31:4	*Reserved*	Yes	No	0h

Register 20-90. PCI:34h, LOC:B4h LCS_OPQIM Outbound Post Queue Interrupt Mask

Bit(s)	Description	Read	Write	Default
2:0	*Reserved*	Yes	No	000b
3	**Outbound Post Queue Interrupt Mask** Writing 1 masks the Outbound Post queue interrupt.	Yes	Yes	1
31:4	*Reserved*	Yes	No	0h

Register 20-91. PCI:40h LCS_IQP Inbound Queue Port

Bit(s)	Description	Read	Write	Default
31:0	Value written by the PCI Master is stored into the Inbound Post queue, which is located in Local memory at the address pointed to by the **Queue Base Address** register (LCS_QBAR) + Queue Size + **Inbound Post Head Pointer** register (LCS_IPHPR). From the time of the PCI write until the Local Memory write and update of the Inbound Post Queue Head Pointer, further accesses to this register result in a Retry. A Local interrupt output (LINTo#) is asserted when the Inbound Post queue is not empty. When the port is read by the PCI Master, the value is read from the Inbound Free queue, which is located in Local memory at the address pointed to by the **Queue Base Address** register (**LCS_QBAR**) + **Inbound Free Tail Pointer** register (LCS_IFTPR). When the queue is empty, FFFF_FFFFh is returned.	PCI	PCI	0h

Register 20-92. PCI:44h LCS_OQP Outbound Queue Port

Bit(s)	Description	Read	Write	Default
31:0	Value written by the PCI Master is stored into the Outbound Free queue, which is located in Local memory at the address pointed to by the **Queue Base Address** register (LCS_QBAR) + 3*Queue Size + **Outbound Free Head Pointer** register (LCS_OPHPR). From the time of the PCI write until the Local Memory write and update of the Outbound Free Queue Head Pointer, further accesses to this register result in a Retry. When the queue fills, Local interrupt LSERR# (C or J mode) or LINTo#) (M mode) is asserted. When the port is read by the PCI Master, the value is read from the Outbound Post queue, which is located in Local memory at the address pointed to by the **Queue Base Address** register (**LCS_QBAR**) + 2*Queue Size + **Outbound Post Tail Pointer** register (LCS_OPTPR). When the queue is empty, FFFF_FFFFh is returned. The internal PCI Wire interrupt (INTA#) is asserted when the Outbound Post queue is not empty.	PCI	PCI	0h

Register 20-93. PCI:C0h, LOC:140h LCS_MQCR Messaging Queue Configuration

Bit(s)	Description	Read	Write	Default
0	**Queue Enable** When cleared to 0, writes are accepted but ignored and reads return FFFF_FFFFh. Writing 1 allows accesses to the Inbound and Outbound Queue ports.	Yes	Yes	0
5:1	**Circular Queue Size** Contains the size of one of the four circular FIFO queues. Each of the queues are the same size. **Bits [5:1]** **Number of Entries** **Total Size** 00_001b 4-KB entries 64 KB 00_010b 8-KB entries 128 KB 00_100b 16-KB entries 256 KB 01_000b 32-KB entries 512 KB 10_000b 64-KB entries 1 MB	Yes	Yes	00_001b
31:6	*Reserved*	Yes	No	0h

Register 20-94. PCI:C4h, LOC:144h LCS_QBAR Queue Base Address

Bit(s)	Description	Read	Write	Default
19:0	*Reserved*	Yes	No	0h
31:20	**Queue Base Address** Local Memory Base address of circular queues. Queues must be aligned on a 1-MB Address Boundary space.	Yes	Yes	0h

Register 20-95. PCI:C8h, LOC:148h LCS_IFHPR Inbound Free Head Pointer

Bit(s)	Description	Read	Write	Default
1:0	*Reserved*	Yes	No	00b
19:2	**Inbound Free Head Pointer** Local Memory Offset for the Inbound Free queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 20-96. PCI:CCh, LOC:14Ch LCS_IFTPR Inbound Free Tail Pointer

Bit(s)	Description	Read	Write	Default
1:0	*Reserved*	Yes	No	00b
19:2	**Inbound Free Tail Pointer** Local Memory offset for the Inbound Free queue. Maintained by the hardware and incremented by the modulo of the Queue Size.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 20-97. PCI:D0h, LOC:150h LCS_IPHPR Inbound Post Head Pointer

Bit(s)	Description	Read	Write	Default
1:0	*Reserved*	Yes	No	00b
19:2	**Inbound Post Head Pointer** Local Memory offset for the Inbound Post queue. Maintained by the hardware and incremented by the modulo of the Queue Size.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 20-98. PCI:D4h, LOC:154h LCS_IPTPR Inbound Post Tail Pointer

Bit(s)	Description	Read	Write	Default
1:0	*Reserved*	Yes	No	00b
19:2	**Inbound Post Tail Pointer** Local Memory offset for the Inbound Post queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 20-99. PCI:D8h, LOC:158h LCS_OFHPR Outbound Free Head Pointer

Bit(s)	Description	Read	Write	Default
1:0	*Reserved*	Yes	No	00b
19:2	**Outbound Free Head Pointer** Local Memory offset for the Outbound Free queue. Maintained by the hardware and incremented by the modulo of the Queue Size.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 20-100. PCI:DCh, LOC:15Ch LCS_OFTPR Outbound Free Tail Pointer

Bit(s)	Description	Read	Write	Default
1:0	*Reserved*	Yes	No	00b
19:2	**Outbound Free Tail Pointer** Local Memory offset for the Outbound Free queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 20-101. PCI:E0h, LOC:160h LCS_OPHPR Outbound Post Head Pointer

Bit(s)	Description	Read	Write	Default
1:0	*Reserved*	Yes	No	00b
19:2	**Outbound Post Head Pointer** Local Memory offset for the Outbound Post queue. Maintained by the Local CPU software.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 20-102. PCI:E4h, LOC:164h LCS_OPTPR Outbound Post Tail Pointer

Bit(s)	Description	Read	Write	Default
1:0	*Reserved*	Yes	No	00b
19:2	**Outbound Post Tail Pointer** Local Memory offset for the Outbound Post queue. Maintained by the hardware and incremented by the modulo of the Queue Size.	Yes	Yes	0h
31:20	**Queue Base Address**	Yes	No	0h

Register 20-103. PCI:E8h, LOC:168h LCS_QSR Queue Status/Control

Bit(s)	Description	Read	Write	Default
0	**I₂O Decode Enable** 1 = Replaces the LCS_MBOX0 and LCS_MBOX1 registers with the **Inbound Queue Port** and **Outbound Queue Port** registers and redefines Local Address Space 1 as the PCI Express Memory Base address to be accessed by LCS_PCIBAR0. Program former Local Address Space 1 registers – LCS_LAS1RR, LCS_LAS1BA, and LCS_LBRD1 – to configure their shared I₂O Memory space, defined as the PCI Express Memory Base address.	Yes	Yes	0
1	**Queue Local Space Select** 0 = Local Address Space 0 Bus Region Descriptor is used for Queue accesses 1 = Local Address Space 1 Bus Region Descriptor is used for Queue accesses	Yes	Yes	0
2	**Outbound Post Queue Prefetch Enable** Writing 1 causes prefetching to occur from the Outbound Post queue when the queue is not empty.	Yes	Yes	0
3	**Inbound Free Queue Prefetch Enable** Writing 1 causes prefetching to occur from the Inbound Free queue when the queue is not empty.	Yes	Yes	0
4	**Inbound Post Queue Interrupt Not Empty Mask** Writing 1 masks the Inbound Post Queue Not Empty interrupt from generating a Local interrupt. Value of 0 clears the mask.	Yes	Yes	1
5	**Inbound Post Queue Interrupt Not Empty** Set when the Inbound Post queue is not empty. Not affected by the bit 4 (*Inbound Post Queue Interrupt Not Empty Mask*) state.	Yes	No	0
6	**Outbound Free Queue Overflow Interrupt Full Mask** **C and J Modes:** 0 = Clears the mask 1 = Masks the Local LSERR# (NMI) interrupt **M Mode:** 0 = Clears the mask 1 = Masks the Local LINTo# (NMI) interrupt	Yes	Yes	1
7	**Outbound Free Queue Overflow Interrupt Full** **C and J Modes:** Set when the Outbound Free queue becomes full. A Local LSERR# interrupt is asserted. Writing 1 clears the interrupt. **M Mode:** Set when the Outbound Free queue becomes full. A Local LINTo# interrupt is asserted. Writing 1 clears the interrupt.	Yes	Yes/Clr	0
31:8	*Reserved*	Yes	No	0h

Chapter 21   Testability and Debug

21.1   JTAG Interface

The PEX 8311 provides a Joint Test Action Group (JTAG) Boundary Scan interface, which is used to debug board connectivity for each ball. Due to the two-die designs, the PEX 8311 JTAG Boundary Scan is serially interconnected. The PEX 8311 provides two individual BSDL files for each die.

21.1.1   *IEEE Standard 1149.1* Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly referred to as the *JTAG Debug port*, is an architectural standard described in the *IEEE Standard 1149.1-1990 IEEE Standard Test Access Port and Boundary-Scan Architecture*. This standard describes a method for accessing internal bridge facilities, using a four- or five-signal interface.

The JTAG Debug port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1b-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- JTAG Signals – JTAG Debug port implements the four required JTAG signals (TCK, TDI, TDO, TMS) and the optional TRST# signal
- JTAG Clock Requirements – TCK signal frequency can range from DC to 10 MHz
- JTAG Reset Requirements – Refer to Section 21.1.4, "JTAG Reset Input TRST#"

21.1.2   JTAG Instructions

The JTAG Debug port provides the *IEEE standard 1149.1* EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE instructions, as defined in Table 21-1. ***PRIVATE instructions are for PLX use only.*** Invalid instructions behave as the BYPASS instruction.

Table 21-1 defines the PCI Express JTAG instructions, along with their input codes. The PEX 8311 returns the PCI Express IDCODE values defined in Table 21-2.

Table 21-1.   PEX 8311 PCI Express Die EXTEST, IDCODE, SAMPLE/PRELOAD, BYPASS, and PRIVATE Instructions

Instruction	Input Code	Comments
EXTEST	00000b	
IDCODE	00001b	
SAMPLE/PRELOAD	00011b	
BYPASS	11111b	
PRIVATE[a]	00011b	*IEEE Standard 1149.1-1990*
	00100b	
	00101b	
	00110b	
	00111b	
	01000b	
	01001b	
	01010b	

a.   *Warning: Non-PLX use of PRIVATE instructions can cause a component to operate in a hazardous manner.*

Table 21-2.   PEX 8311 PCI Express Die JTAG IDCODE Values

PEX 8311	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
Bits	0010b	1000_0001_1101_0010b	000_0001_0000b	1
Hex	2h	81D2h	10h	1h
Decimal	2	33234	16	1

The PEX 8311 returns the Local Bus IDCODE values defined in Table 21-3. Table 21-4 defines the JTAG instructions, with their input codes.

Table 21-3. PEX 8311 Local Bus Die JTAG IDCODE Value

M S B																															L S B
3 1	3 0	2 9	2 8	2 7	2 6	2 5	2 4	2 3	2 2	2 1	2 0	1 9	1 8	1 7	1 6	1 5	1 4	1 3	1 2	1 1	1 0	9	8	7	6	5	4	3	2	1	0

Version				Part Number (PCI 9056 when converted to decimal)														PLX Manufacturer Identity													
0	0	0	1	0	0	1	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	1	1	1	0	0	1	1	0	1	1

Table 21-4. PEX 8311 Local Bus Die JTAG Instructions

Instruction	Input Code	Comments
EXTEST	00b	*IEEE Standard 1149.1-1990*
IDCODE	01b	
SAMPLE/PRELOAD	10b	
BYPASS	11b	

21.1.3   JTAG Boundary Scan

Scan Description Language (BSDL), IEEE 1149.1b-1994, is a supplement to *IEEE Standard 1149.1-1990* and *IEEE 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture. BSDL*, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, which allows a rigorous description of testability features in components which comply with the standard. It is used by automated test pattern generation tools for package interconnect tests and Electronic Design Automation (EDA) tools for synthesized test logic and verification. *BSDL* supports robust extensions that are used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of *BSDL* include the logical port description, physical ball map, instruction set, and boundary register description.

The logical port description assigns symbolic names to the PEX 8311 balls. Each ball has a logical type of In, Out, In Out, Buffer, or Linkage that defines the logical direction of signal flow.

The physical ball map correlates the bridge logical ports to the physical balls of a specific package. A *BSDL* description maintains several physical ball maps; each map is assigned a unique name.

Instruction set statements describe the bit patterns that must be shifted into the Instruction register to place the bridge in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the bridge.

The Boundary register description lists each cell or shift stage of the Boundary register. Each cell has a unique number; the cell numbered 0 is the closest to the Test Data Out (TDO) ball and the cell with the highest number is closest to the Test Data In (TDI) ball. Each cell contains additional information, including:

- Cell type
- Logical port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

21.1.4   JTAG Reset Input TRST#

The TRST# input ball is the asynchronous JTAG logic reset. TRST# assertion causes the PEX 8311 TAP Controller to initialize. In addition, when the TAP Controller is initialized, it selects the PEX 8311 normal logic path (PCI Express interface-to-I/O). It is recommended that the following be taken into consideration when implementing the asynchronous JTAG logic reset on a board:

- When JTAG functionality is required, consider one of the following:
  - TRST# input signal uses a Low-to-High transition one time during the PEX 8311 boot-up, along with the PERST# signal (ROOT_COMPLEX# is strapped High) or LRESET# signal (ROOT_COMPLEX# is strapped Low).
  - Hold the PEX 8311 TMS ball High while transitioning the PEX 8311 TCK ball five times.
- When JTAG functionality is not required, the TRST# signal must be directly connected to ground.

Chapter 22   Shared Memory

22.1   Overview

The PEX 8311 includes a 2K x 32-bit (8-KB) memory block that is accessed from the PCI Express interface serial EEPROM, PCI Express interface, or Local Bus.

22.2   PCI Express Serial EEPROM Accesses

When the *Shared Memory Load* bit in the Serial EEPROM Format byte is set, the shared memory is loaded from the serial EEPROM starting at location REG BYTE COUNT + 6. The number of bytes to load is determined by the value in EEPROM locations REG BYTE COUNT + 4 and REG BYTE COUNT + 5. The serial EEPROM data is always loaded into the shared memory, starting at Address 0. Data is transferred from the serial EEPROM to the shared memory (in units of DWORDs). (Refer to Chapter 4, "Serial EEPROM Controllers," for details.)

22.3   PCI Express Accesses

The shared memory is accessed from PCI Express Space, using the 64-KB Address space defined by the **PECS_PCIBASE0** register. The shared memory is located at address offset 8000h in this space. PCI Express Posted Writes are used to write data to the shared memory. Single or Burst Writes are accepted, and PCI Express first and last Byte Enables are supported. When shared Memory Write data is poisoned, the data is discarded and an ERR_NONFATAL message is generated, when enabled. PCI Express Non-Posted Reads are used to read data from the shared memory. Either Single or Burst Reads are accepted. When the 8-KB Address Boundary space of the shared memory is reached during a Burst Write or Read, the address wraps around to the beginning of the memory.

22.4   Local Bus Accesses

Local Bus Masters access the PEX 8311's shared memory by way of Memory-Mapped Direct Master transaction, using the 64-KB Address space defined by the **PECS_PCIBASE0** register. The shared memory is located at offset 8000h in this space. Local Bus Single or Burst Writes are used to write data to the shared memory. Local Bus Byte Enables are supported for each DWORD transferred. Local Bus Single or Burst Reads are used to read data from the shared memory. When the 8-KB boundary of the shared memory is reached during a Burst Write or Read, an internal Disconnect is generated to the Local Address space during the transaction.

22.5   Scatter/Gather DMA Descriptors

The DMA descriptors can be stored in the shared memory for ease of access and to overcome bus latency on the PCI Express interface. The PEX 8311 accesses the PCI Express shared memory as a Memory-Mapped transaction during the descriptor load access. For further details, refer to Section 9.5.5, "DMA Scatter/Gather Mode."

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Chapter 23 Electrical Specifications

23.1 Power-Up Sequence

As in all multiple power supply devices, ensure proper power-on procedures for the PEX 8311.

The PEX 8311 includes four power supplies, requiring voltages of 3.3V, 2.5V, 1.5V, and 1.5V (filtered), respectively. The only sequencing requirement is that the 2.5V and 1.5V supplies must reach nominal operating voltage no later than 10 ms after power is applied to the 3.3V I/O supply balls. This delay allows the 2.5V and 1.5V supplies to be regulated from 3.3V, without need for load switching or power sequencing circuitry.

Caution: ***Never apply power only to the 3.3V supply balls, as the un-powered core logic presents a low-resistance path to ground, and high current flow results. Maintaining this condition for more than 10 ms damages or shortens the life of the PEX 8311.***

Table 23-1. Supply Voltages

Supply Voltage	Supply Balls	Description	Maximum Delay from 3.3V
3.3V	VDD3.3	3.3V I/O Buffers	–
2.5V	VDD2.5	Local Bus core logic	+10 ms
1.5V	VDD1.5, AVDD, VDD_T, VDD_R	PCI Express core logic, analog, and differential signals	
1.5V (filtered)	VDD_P	PLL Supply	

23.2 Power-Down Sequence

The 3.3V, 2.5V, and 1.5V power supply is powered down in any order.

23.3 3.3V and 5V Mixed-Voltage Devices

The PEX 8311 I/O buffers are 3.3V-based, but 5V tolerant. They are capable of receiving 5V signals and their output levels meet 5V TTL specifications.

23.4   Absolute Maximum Ratings

Caution: Conditions that exceed the Absolute Maximum limits can destroy the PEX 8311.

Table 23-2.   Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Supply Voltages	With Respect to Ground	-0.5	+1.8	V
VDD3.3	3.3V Supply Voltages	With Respect to Ground	-0.5	+4.6	V
VDD2.5	2.5V Supply Voltage	With Respect to Ground	-0.5	+3.6	V
V_{IN}	DC Input Voltage	3.3V buffer	-0.5	VDD3.3 +0.5	V
		5V Tolerant buffer (Local)	-0.5	VDD3.3 +0.5	V
I_{OUT}	DC Output Current, Per Ball	3 mA Buffer	-10	+10	mA
		6 mA Buffer	-20	+20	mA
		12 mA Buffer	-40	+40	mA
		24 mA Buffer	-70	+70	mA
T_{STG}	Storage Temperature	No bias	-65	+150	°C
T_{AMB}	Ambient Temperature (Commercial)	Under bias	0	+70	°C
V_{ESD}	ESD Rating	R = 1.5KΩ, C = 100 pF		2	KV
V_{OUT}	DC Output Voltage	3.3V, 5V Tolerant buffer (Local)	-0.5	VDD3.3 +0.5	V
Maximum Power Consumption	Power (refer to Table 23-6)			1.2	W

23.5   Recommended Operating Conditions

Caution: Conditions that exceed the Operating limits can cause the PEX 8311 to malfunction.

Table 23-3.   Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
VDD1.5, VDD_P, VDD_R, VDD_T, AVDD	1.5V Supply Voltages		1.4	1.6	V
VDD3.3	3.3V Supply Voltages		3.0	3.6	V
VDD2.5	2.5V Supply Voltage		2.3	2.7	V
V_N	Negative Trigger Voltage	3.3V buffer	0.8	1.7	V
		5V tolerant buffer	0.8	1.7	V
V_P	Positive Trigger Voltage	3.3V buffer	1.3	2.4	V
		5V tolerant buffer	1.3	2.4	V
V_{IL}	Low Level Input Voltage	3.3V buffer	0	0.7	V
		5V tolerant buffer	0	0.8	V
V_{IH}	High Level Input Voltage	3.3V buffer	1.7	VDD3.3 +0.5	V
		5V tolerant buffer	2.0	VDD3.3 +0.5	V
I_{OL}	Low Level Output Current	3 mA buffer (V_{OL} = 0.4)	3		mA
		6 mA buffer (V_{OL} = 0.4)	6		mA
		12 mA buffer (V_{OL} = 0.4)	12		mA
		24 mA buffer (V_{OL} = 0.4)	24		mA
I_{OH}	High Level Output Current	3 mA buffer (V_{OH} = 2.4)		-3	mA
		6 mA buffer (V_{OH} = 2.4)		-6	mA
		12 mA buffer (V_{OH} = 2.4)		-12	mA
		24 mA buffer (V_{OH} = 2.4)		-24	mA
T_A	Operating Temperature (Commercial) [1]		0	70	°C
t_R	Input Rise Times	Normal input		200	ns
t_F	Input Fall Time			200	ns
t_R	Input Rise Times	Schmitt input		10	ms
t_F	Input Fall Time			10	ms

[1] *Industrial Temperature Range of -40 ºC to +85 ºC is supported. With the maximum power supply provided and in a worst case I/O switching scenario, the PEX 8311's maximum power dissipation will be at 1.31W. It is highly recommended that the maximum power dissipation does not exceed 1.31W to ensure proper operation, which is guaranteed to work in the Industrial Temperature range with 0 m/s airflow.*

Junction-to-Ambient Package Thermal Resistance – Thetaj-a = 23.28 °C/W, at 0 m/s Linear Air Flow.

Table 23-4.   Capacitance (Sample Tested Only)

Parameter	Test Conditions	Ball Type	Value		Units
			Typical	**Maximum**	
C_{IN}	$V_{IN} = 0V$	Input	4	6	pF
C_{OUT}	$V_{OUT} = 0V$	Output	6	10	pF

Table 23-5.   Electrical Characteristics over Operating Range

Parameter	Description	Test Conditions		Minimum	Maximum	Units	Buffer Type
$V_{OH}{}^1$	Output High Voltage	V_{DD} = Minimum $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -12.0 mA	2.4	–	V	Local
$V_{OL}{}^1$	Output Low Voltage		I_{OL} = +12 mA	–	0.4	V	
$V_{OH}{}^2$	Output High Voltage		I_{OH} = -24.0 mA	2.4	–	V	
$V_{OL}{}^2$	Output Low Voltage		I_{OL} = +24 mA	–	0.4	V	
V_{IH}	Input High Level	–	–	2.0	VDD3.3 +0.5	V	
V_{IL}	Input Low Level	–	–	-0.5	+0.8	V	

[1.] *For 12 mA I/O or output cells (Local Bus).*

[2.] *For 24 mA I/O or output cells (Local Bus). For 24 mA I/O or output cells (Local Bus). The PEX 8311 Local Bus is proprietary to PLX; therefore, the values reported are best-case estimates. The I/O buffer drive strength is 24mA by design. The V_{OL}/V_{OH} lists a 90% worst-case scenario; however, this is still an approximation. Therefore, 10% margin still remains for the worst case. In addition, the 24 mA drive strength is estimated to have 10% uncertainty.*

23.6   Operating Current

Table 23-6.   Maximum Operating Power Consumption

Symbol	Parameter	Test Conditions	Max	Unit
I$_{VDD1.5}$	VDD1.5 Supply Current	VDD1.5 = 1.6V	375	mW
I$_{VDD2.5}$	VDD2.5 Supply Current	VDD2.5 = 2.7V	365	mW
I$_{VDD3.3}$	VDD3.3 Supply Current	VDD3.3 = 3.6V	475	mW
Total			1.2	W

23.7   Local Bus Inputs

Table 23-7 defines the CLKIN specifications. Figure 23-1 illustrates the PEX 8311 Local input setup and hold timing. Table 23-8 through Table 23-10 define the Local Bus Worst Case T$_{SETUP}$ and T$_{HOLD}$ values for each Local Bus mode. T$_{SETUP}$ is the setup time, the time that an input signal is stable before the rising edge of LCLK. T$_{HOLD}$ is the time that an input signal is stable after the rising edge of LCLK.

Table 23-7.   LCLK and CLKIN Specifications

Clock Input Frequency	Minimum	Maximum
Local (LCLK)	> 0 MHz	66 MHz
Internal PCI (CLKIN)		

> *Note: LCLK must toggle at a stable frequency at all times during normal device operation. Similarly, for Root Complex applications, the externally supplied CLKIN must be toggled at all times during standard operation. (CLKIN is internally sourced, by way of CLKOUT, for Endpoint mode).*

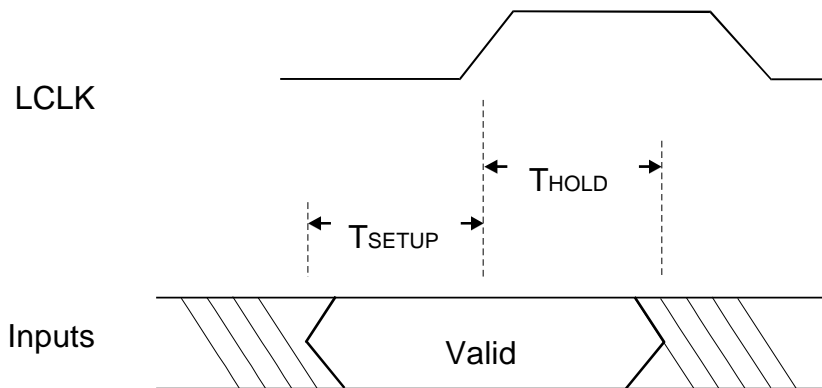**Figure 23-1.   PEX 8311 Local Input Setup and Hold Timing**

Table 23-8.   C Mode Local Bus Worst Case Input AC Timing Specifications

Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}	Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}
	V_{CC} = 3.0V, T_A = 70°C			V_{CC} = 3.0V, T_A = 70°C	
ADS#	2.1 ns	1 ns	LA[31:2]	3.4 ns	1 ns
BIGEND#	4.0 ns	1 ns	LBE[3:0]#	3.6 ns	1 ns
BLAST#	3.4 ns	1 ns	LD[31:0]	3.1 ns	1 ns
BREQi	3.0 ns	1 ns	LHOLDA	2.5 ns	1 ns
BTERM#	4.0 ns	1 ns	LW/R#	3.5 ns	1 ns
CCS#	2.9 ns	1 ns	READY#	4.0 ns	1 ns
DMPAF/EOT#	4.2 ns	1 ns	USERi/LLOCKi#	2.9 ns	1 ns
DP[3:0]	2.9 ns	1 ns	WAIT#	4.0 ns	1 ns
DREQ[1:0]#	3.3 ns	1 ns			

Table 23-9.   J Mode Local Bus Worst Case Input AC Timing Specifications

Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}	Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}
	V_{CC} = 3.0V, T_A = 70°C			V_{CC} = 3.0V, T_A = 70°C	
ADS#	2.1 ns	1 ns	DREQ[1:0]#	3.3 ns	1 ns
ALE	1.7 ns	1 ns	LA[28:2]	3.4 ns	1 ns
BIGEND#	4.0 ns	1 ns	LAD[31:0]	3.1 ns	1 ns
BLAST#	3.4 ns	1 ns	LBE[3:0]#	3.6 ns	1 ns
BREQi	3.0 ns	1 ns	LHOLDA	2.5 ns	1 ns
BTERM#	4.2 ns	1 ns	LW/R#	3.5 ns	1 ns
CCS#	2.9 ns	1 ns	READY#	4.2 ns	1 ns
DMPAF/EOT#	4.2 ns	1 ns	USERi/LLOCKi#	2.9 ns	1 ns
DP[3:0]	2.9 ns	1 ns	WAIT#	4.0 ns	1 ns

Table 23-10.   M Mode Local Bus Worst Case Input AC Timing Specifications

Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}	Signals (Synchronous Inputs)	T_{SETUP}	T_{HOLD}
	V_{CC} = 3.0V, T_A = 70°C			V_{CC} = 3.0V, T_A = 70°C	
BB#	2.7 ns	1 ns	LA[0:31]	3.6 ns	1 ns
BDIP#	3.8 ns	1 ns	LD[0:31]	3.1 ns	1 ns
BG#	2.9 ns	1 ns	MDREQ#/DMPAF/EOT#	4.2 ns	1 ns
BI#	4.0 ns	1 ns	RD/WR#	3.5 ns	1 ns
BIGEND#/WAIT#	3.8 ns	1 ns	TA#	4.1 ns	1 ns
BURST#	4.1 ns	1 ns	TEA#	4.4 ns	1 ns
CCS#	2.9 ns	1 ns	TS#	2.1 ns	1 ns
DP[0:3]	2.9 ns	1 ns	TSIZ[0:1]	3.6 ns	1 ns
DREQ[1:0]#	3.3 ns	1 ns	USERi/LLOCKi#	3.2 ns	1 ns

23.8　Local Bus Outputs

illustrates the PEX 8311 Local output delay timing. through define the T_{VALID} (MAX) values for the C, J, and M Local Bus modes. T_{VALID} is output valid (clock-to-out), the time after the rising edge of LCLK until the output is stable. T_{VALID} (MIN) is no less than 2.2 ns for each signal for the C, J, and M Local Bus modes.

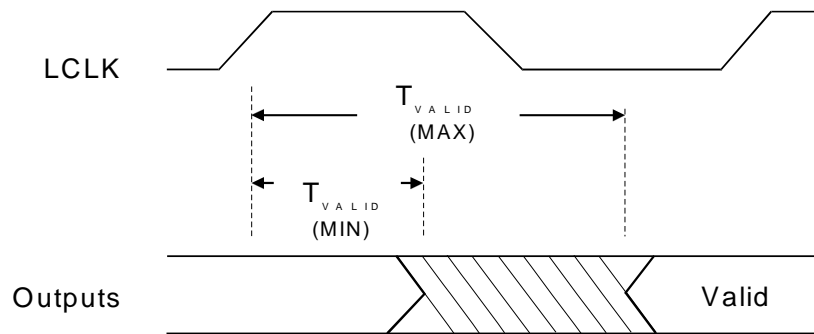**Figure 23-2.　PEX 8311 Local Output Delay**

Table 23-11.   C Mode Local Bus T$_{VALID}$ (MAX) Output AC Timing Specifications

Signals (Synchronous Outputs)	Output T$_{VALID}$ C$_L$ = 50 pF, V$_{CC}$ = 3.0V, T$_A$ = 70°C	Signals (Synchronous Outputs)	Output T$_{VALID}$ C$_L$ = 50 pF, V$_{CC}$ = 3.0V, T$_A$ = 70°C
ADS#	6.3 ns	LBE[3:0]#	6.3 ns
BLAST#	6.3 ns	LD[31:0]	6.4 ns
BREQo	6.8 ns	LHOLD	6.8 ns
BTERM#	6.8 ns	LSERR#	7.5 ns
DACK[1:0]#	6.3 ns	LW/R#	6.3 ns
DMPAF/EOT#	6.6 ns	READY#	7.2 ns
DP[3:0]	6.8 ns	USERo/LLOCKo#	6.3 ns
LA[31:2]	6.8 ns	WAIT#	6.4 ns

Notes: On High-to-Low transitions, output T$_{VALID}$ values increase/decrease by 16 ps for each increase/decrease of 1 pF.

On Low-to-High transitions, output T$_{VALID}$ values increase/decrease by 20 ps for each increase/decrease of 1 pF.

On High-to-Low transitions, the slew rate at 50 pF loading is 1.93V/ns typical; 0.94V/ns worst case.

On Low-to-High transitions, the slew rate at 50 pF loading is 1.15V/ns typical; 0.70V/ns worst case.

Table 23-12.   J Mode Local Bus T$_{VALID}$ (MAX) Output AC Timing Specifications

Signals (Synchronous Outputs)	Output T$_{VALID}$ C$_L$ = 50 pF, V$_{CC}$ = 3.0V, T$_A$ = 70°C	Signals (Synchronous Outputs)	Output T$_{VALID}$ C$_L$ = 50 pF, V$_{CC}$ = 3.0V, T$_A$ = 70°C
ADS#	6.3 ns	LA[28:2]	6.4 ns
ALE	Refer to Figure 23-3	LAD[31:0]	6.4 ns
BLAST#	6.3 ns	LBE[3:0]#	6.3 ns
BREQo	6.8 ns	LHOLD	6.8 ns
BTERM#	6.8 ns	LSERR#	7.5 ns
DACK[1:0]#	6.3 ns	LW/R#	6.3 ns
DEN#	6.4 ns	READY#	7.2 ns
DMPAF/EOT#	6.6 ns	USERo/LLOCKo#	6.3 ns
DP[3:0]	6.8 ns	WAIT#	6.4 ns
DT/R#	6.3 ns		

Notes: On High-to-Low transitions, output T$_{VALID}$ values increase/decrease by 16 ps for each increase/decrease of 1 pF.

On Low-to-High transitions, output T$_{VALID}$ values increase/decrease by 20 ps for each increase/decrease of 1 pF.

On High-to-Low transitions, the slew rate at 50 pF loading is 1.93V/ns typical; 0.94V/ns worst case.

On Low-to-High transitions, the slew rate at 50 pF loading is 1.15V/ns typical; 0.70V/ns worst case.

**Table 23-13.   M Mode Local Bus T$_{VALID}$ (MAX) Output AC Timing Specifications**

Signals (Synchronous Outputs)	Output T$_{VALID}$ C$_L$ = 50 pF, V$_{CC}$ = 3.0V, T$_A$ = 70°C	Signals (Synchronous Outputs)	Output T$_{VALID}$ C$_L$ = 50 pF, V$_{CC}$ = 3.0V, T$_A$ = 70°C
BB#	6.8 ns	MDREQ#/DMPAF/ EOT#	6.6 ns
BDIP#	6.4 ns	RD/WR#	6.3 ns
BIGEND#/WAIT#	6.3 ns	RETRY#	6.8 ns
BR#	6.8 ns	TA#	7.2 ns
BURST#	6.3 ns	TEA#	7.5 ns
DACK[1:0]#	6.3 ns	TS#	6.3 ns
DP[0:3]	6.8 ns	TSIZ[0:1]	6.3 ns
LA[0:31]	6.8 ns	USERo/LLOCKo#	6.3 ns
LD[0:31]	6.3 ns		

Notes: *On High-to-Low transitions, output T$_{VALID}$ values increase/decrease by 16 ps for each increase/decrease of 1 pF.*

   On Low-to-High transitions, output T$_{VALID}$ values increase/decrease by 20 ps for each increase/decrease of 1 pF.

   On High-to-Low transitions, the slew rate at 50 pF loading is 1.93V/ns typical; 0.94V/ns worst case.

   On Low-to-High transitions, the slew rate at 50 pF loading is 1.15V/ns typical; 0.70V/ns worst case.

23.9   ALE Output Delay Timing for Local Bus Clock Rates

Figure 23-3 illustrates the PEX 8311 ALE output delay timing for any processor/Local Bus clock rate.

Figure 23-3.   PEX 8311 ALE Output Delay to Local Clock
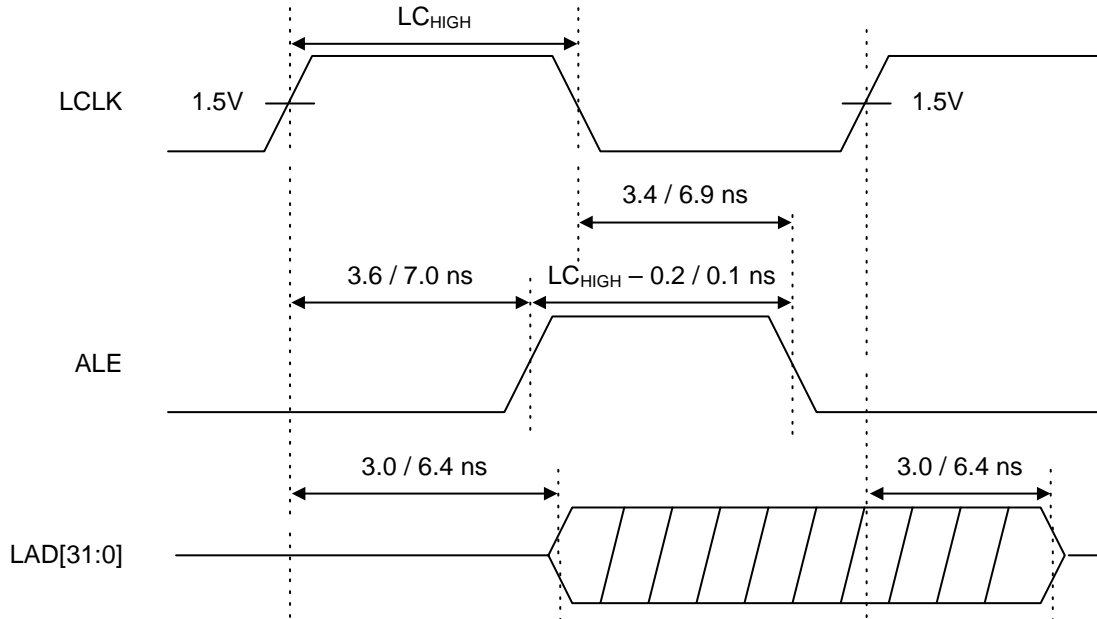
Notes: LC_{HIGH} *is the time, in ns, that the processor/Local Bus clock is High.*

Times indicated in Figure 23-3 are "minimum/maximum" values.

Chapter 24   Thermal and Mechanical Specifications

24.1   Thermal Specifications

Table 24-1 defines the PEX 8311 lead-free package thermal resistance.

Table 24-1.   Package Thermal Resistance

Thermal Resistance, junction to case ($\Theta_{j\text{-}c}$)	4.22 °C/W				
Maximum Junction Temperature	**125°C**				
Junction to Ambient ($\Theta_{j\text{-}a}$)	0 m/s	0.5 m/s	1 m/s	2 m/s	3 m/s
($\Theta_{j\text{-}a}$)	23.28 °C/W	19.60 °C/W	18.14 °C/W	16.48 °C/W	15.42 °C/W

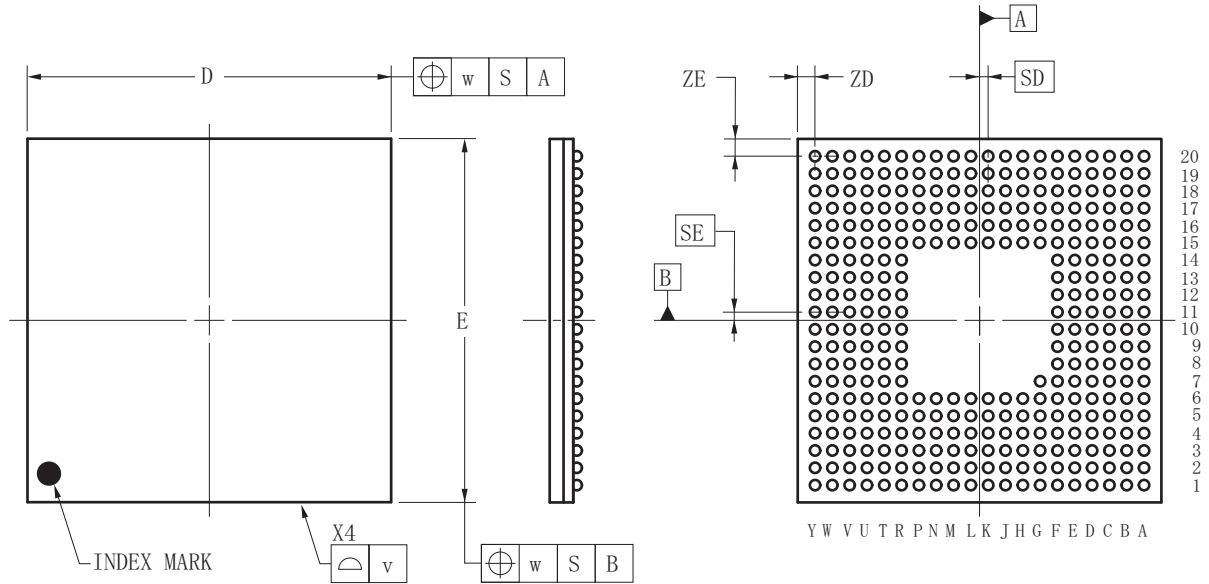## 24.2   General Package Specifications

Table 24-2 lists general package specifications. For a more complete list, refer to Figure 24-1.

Table 24-2.   General Package Specifications

Parameter	Specification
Package Type	Plastic Ball Grid Array (PBGA)
Number of Balls	337
Package Dimensions	21 x 21 mm^2 (approximately 1.86 ±0.14-mm high)
Ball Matrix Pattern	20 x 20
Ball Pitch	1.00 mm
Ball Diameter	0.60 ±0.10 mm
Ball Spacing	0.40 mm

24.3   Mechanical Dimensions

Figure 24-1.   Package Mechanical Dimensions

D   ⊕ w S A

ZE   ZD   SD   A

SE

B

20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1

Y W V U T R P N M L K J H G F E D C B A

E

INDEX MARK

X4
⌒ v   ⊕ w S B

A

// y1 S   A2   S

⌒ y S   e   A1

φ b ⊕ φ x Ⓜ S A B

(UNIT:mm)

ITEM	DIMENSIONS
D	21.00±0.10
E	21.00±0.10
v	0.20
w	0.30
e	1.00
SD	0.50
SE	0.50
A	1.86±0.14
A1	0.50±0.10
A2	1.36
b	0.60±0.10
x	0.10
y	0.15
y1	0.35
ZD	1.00
ZE	1.00
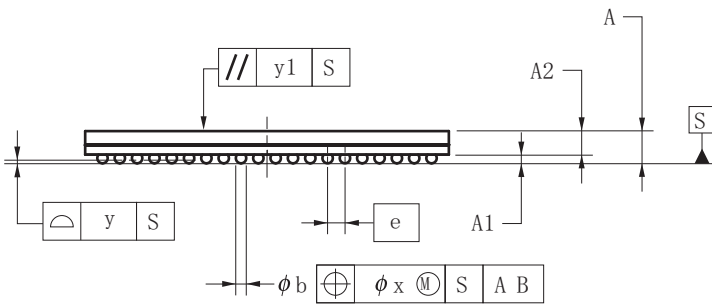
Appendix A   General Information

A.1   Product Ordering Information

Contact your local PLX Sales Representative for ordering information.

Table A-1.   Product Ordering Information

Part Number	Description
PEX8311-AA66BC F	PEX 8311 PCI Express-to-Generic Local Bus Bridge, Standard Plastic BGA (21 x 21 mm^2, 337-Ball) Lead-Free Package

PEX8311-AA66BC F

F – Lead-Free, RoHS-Compliant

C – Commercial Temperature

B – Plastic Ball Grid Array Package

AA – Silicon Revision
66 – Speed Grade (66 MHz Local Bus)

8311 – Part Number
PEX – PCI Express Product Family

PEX 8311RDK	PEX 8311 Rapid Development Kit
SDK	Windows Host-side and Local-side Software Development Kit

A.2   United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at <u>www.plxtech.com</u>.

A.3   Technical Support

PLX Technology, Inc., technical support information is listed at <u>www.plxtech.com/support</u>, or call 800 759-3735 (domestic only) or 408 774-9060.