PCI 9054 RDK-LITE CPLD Code Release Note

Introduction
This code has been created to enhance the functionality of the PCI 9054RDK-LITE. The local bus arbitration code has been modified from the version supplied on the Rapid Development Kit board. It will allow the user to perform direct master operations when more than one local bus master has been added to the board's prototyping area.

The starting address for the SRAM space was also changed from 2000_0000h to 0000_0000h.

Included Files
```
sramctrtrin02.v – Verilog source
sramctrtrin02.pof – Altera compiled programming file
```

Required Programming Equipment
The Altera CPLD on the RDK board is in-system programmable using Altera's download cable and programming software. For those users that don't have the capability of programming Altera CPLDs in-system, the following equipment can be used:

The programming software is included in Altera's free E+MAX software, which is available on Altera's website www.altera.com

The ByteBlasterMV download cable (Part Number PL-BYTEBLASTERMV) is available from Altera's on-line store https://buy.altera.com/ecommerce/index.asp

Instructions for using the cable to program Altera's CPLDs are contained in the ByteBlasterMV datasheet http://www.altera.com/literature/ds/dsbytemv.pdf

Programming Instructions

1. Plug the download cable into header JP1, making sure that the cable is oriented to connect the signals as shown below.

ByteBlasterMV Header Signals	JP1 Header Pins
TCK (Pin 1)	1
TMS (Pin 5)	5
TDI (Pin 9)	9
TDO (Pin 3)	3
VCC (Pin 4)	4
GND (Pin 10)	10

2. Plug the RDK into the host PC and turn the power on. Power for the download cable is supplied through the JP1 header.
3. Follow the Altera instructions for downloading the programming file to the CPLD.