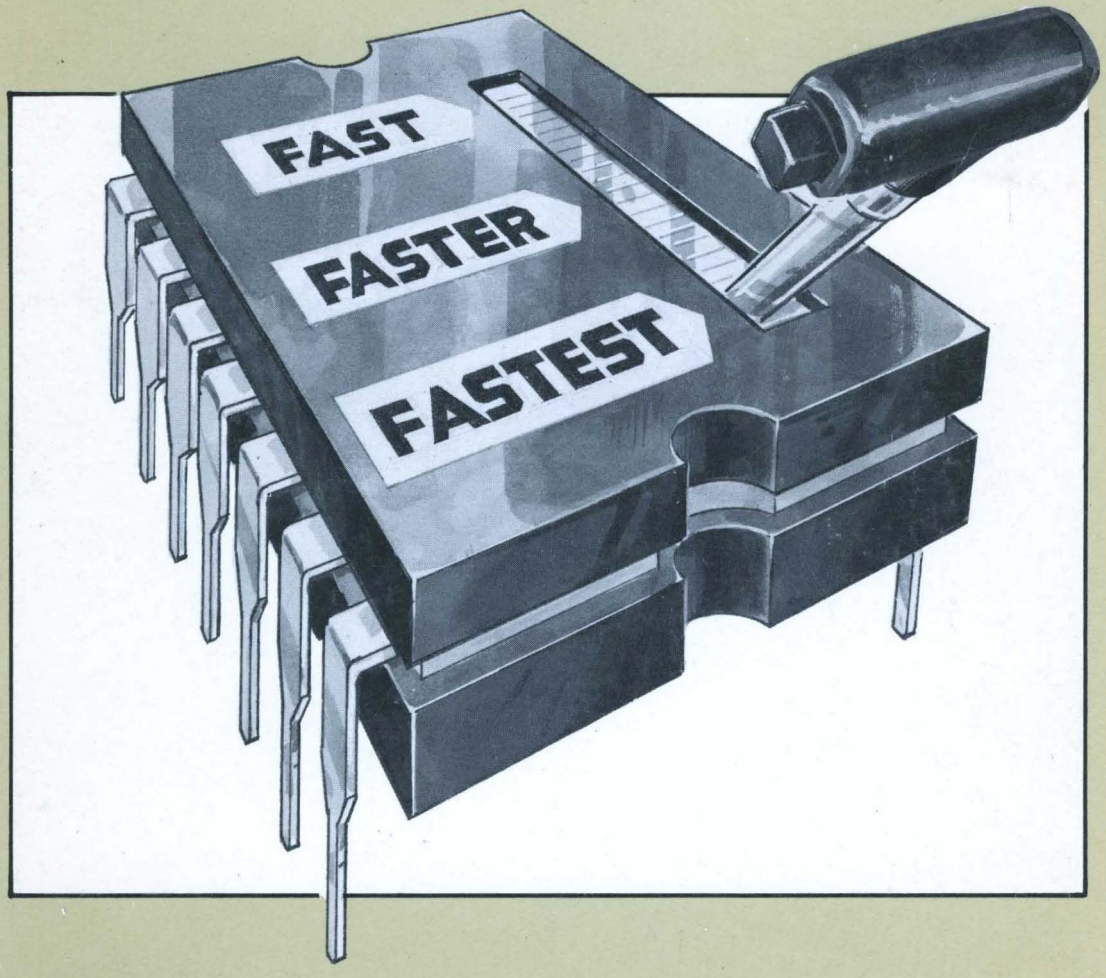
ECL Logic & Data Conversion IC Handbook



Plessey Semiconductors

ECL Logic & Data Conversion IC Handbook

OCTOBER 1980

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

Contents

8. ECL III DATA

Low Z devices available on request

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1. Product Information

Building Block IC's

Plessey integrated circuits are on the leading edge of technology without pushing the ragged edge of capability.

We developed the first 2 GHz counter. And a family of prescalers and controllers for your TV, radio and instrumentation frequency synthesizers.

We have a monolithic 1 GHz amplifier. And a complete array of complex integrated function blocks for radar signal processing and radio communications.

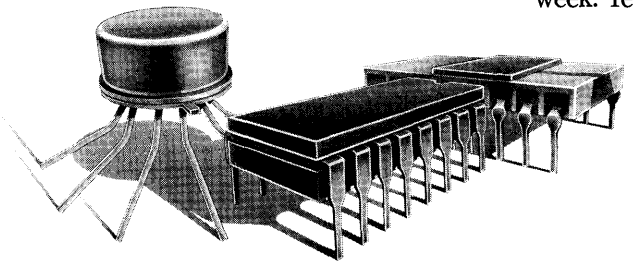
We can supply data conversion devices with propagation delays of just 2½ nanoseconds.

And a range of MNOS logic that stores data for a year when you remove the power, yet uses only standard supplies and is fully TTL/CMOS-compatible.

To develop this edge, we developed our own processes, both bipolar and MOS. The processes were designed for quality and repeatability, then applied to our high volume lines. Most of our IC's are available screened to MIL-STD-883B, and our quality levels exceed the most stringent military, TV and automotive requirements.

Millions of Plessey complex function building block IC's are being used in TV sets and car radios; CATV, navigation and radar systems; frequency synthesizers and telecommunications equipment.

Our global scope of operations, our high volume manufacturing facilities, our proprietary processes ensure that we will continue to deliver state-of-the-art technology and reliability in IC devices at the appropriate prices and in the required volumes. Day after day. Week after week. Year after year.



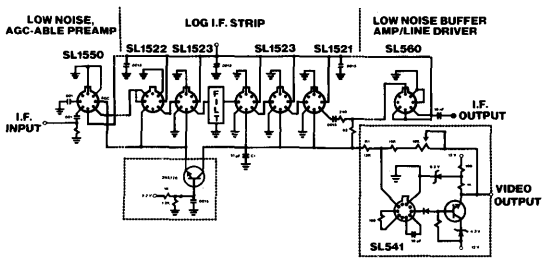
Plessey Semiconductors

1641 Kaiser Avenue, Irvine, CA 92714. (714) 540-9979

Radar Signal Processing

Since the performance of a radar receiver is critically dependent on the performance of its I.F. strip, we offer a range of "building block" IC's that can be used in systems with different performance requirements and configurations.

The logarithmic I.F. strip shown is an example of a low cost, high performance strip fabricated with Plessey IC's. It uses only five devices and a single interstage filter to achieve a logging range of 90 dB, ±1 dB accuracy, −90 dBm tangential sensitivity and a video rise time of 20 ns or less.



Three other Plessey IC's complete the system simply and economically. The AGC-able SL1550 on the front end improves noise figure, dynamic range and sensitivity. The SL541 lets you vary video output levels, with on-chip compensation making it easy to use. And the SL560 is a "gain block" that replaces your hybrid and discrete amplifiers, usually with no external components.

Another advanced system function block is the Plessey SL531 True Log Amplifier. A 6-stage log strip requires a minimum of external components (one capacitor, one resistor per stage), yet has a band-width of 500 MHz, a dynamic range of 70 dB and has a phase shift of only ±3° over its entire range. As with most of our other devices, it operates over the full MIL-temp range and is available screened to MIL-STD-883.

The chart summarizes our Radar Signal Processing IC's. Whether you're working with radar and ECM, weapons control or navigation and guidance systems, our IC's are a simpler, less expensive, more flexible alternative to whatever you're using now for any I.F. strip up to 160 MHz.

For more details, please use the postage-paid reply card at the back of this book to order our RADAR AND RADIO COMMUNICATIONS IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

PLESSEY IC'S FOR RADAR I.F.'S

Wideband Amplifiers for Successive Detection Log Strips

SL521 30 to 60 MHz center frequency, 12 dB gain.
SL523 Dual SL521 (series).
SL1521 60 to 120 MHz center frequency, 12 dB gain.
SL1522 Dual SL1521 (parallel).
SL1523 Dual SL1521 (series).

Low Phase Shift Amplifiers

SL531 True log I.F. amplifier, 10-200 MHz, ±0.5°/10 dB max phase shift.
SL532 400 MHz bandwidth limiting amplifier, 1° phase shift max. when overdriven 12 dB.

Linear Amplifiers

SL550 125 MHz bandwidth, 40 dB gain, 25 dB swept gain control range, 1.8 dB noise figure, interfaces to microwave mixers.
SL1550 320 MHz bandwidth version of SL550.
SL560 300 MHz bandwidth, 10 to 40 dB gain, 1.8 dB noise figure drives 50 ohm loads, low power consumption.

Video Amplifiers and Detectors

SL510 Detector (DC to 100 MHz) and video amplifier (DC to 24 MHz) may be used separately, 11 dB incremental gain 28 dB dynamic range.
SL511 Similar to SL510 with DC to 14 MHz video amplifier, 16 dB incremental gain.
SL541 High speed op amp configuration, 175 V/μs slew rate 50 ns settling time, stable 70 dB gain, 50 ns recovery from overload.

MNOS Non-Volatile Logic

As semiconductors become more pervasive in military and commercial applications, the need for non-volatile data retention becomes more and more critical.

Plessey NOVOL MNOS devices answer that need, and will retain their data for at least a year (−40°C to +70°C) in the event of "power down" or a system crash.

Our devices all operate from standard MOS supplies and are fully compatible with your TTL/CMOS designs. The high voltages normally associated with electrically-alterable memories are generated on-chip to make system interface simpler and less expensive.

Plessey NOVOL devices provide a reliable, sensible alternative to CMOS with battery back-up or mechanical, electro-mechanical and magnetic devices. Applications include metering, security code storage, microprocessor back-up, elapsed time indicators, counters, latching relays and a variety of commercial, industrial and military systems.

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PLESSEY NOVOL MNOS

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* COMING SOON

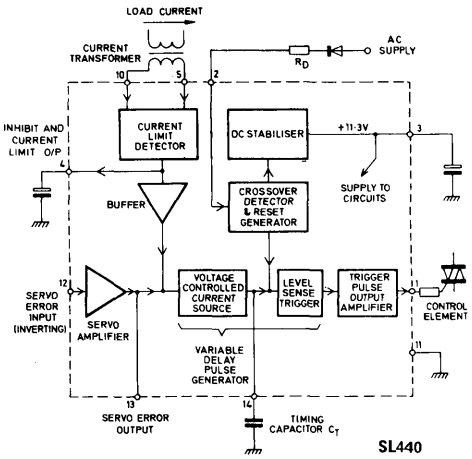
Power Control

Plessey power control devices are highly integrated not just to solve the problems, but to solve them at a lower cost than any other available method.

For timing, our devices use a pulse integration technique that eliminates the need for expensive electrolytic capacitors, thus increasing accuracy and repeatability while reducing costs. An integral supply voltage sensing circuit inhibits triac gate drive circuitry if the supply is dangerously low to prevent half-wave firing and firing without achieving complete bulk conduction. A zero-voltage spike filter prevents misfiring on noise inputs. Symmetrical control prevents the introduction of dc components onto the power lines.

Devices have been tailored for specific applications as indicated in the chart. For more information, please use the postage-paid reply card at the back of this book to order our POWER CONTROL IC HANDBOOK, or contact your nearest Plessey Semiconductors representative.

SL440	**Proportional phase control for motors, lamps and lower power, fast response heating.**
SL441	**Similar to SL440, with proportional temperature control and thermister malfunction sensing, for hairdryers, soldering irons and food warmers.**
SL442	**Switch mode power supply control, up to 40 kHz, integral oscillator, variable ratio space/mark pulses, soft-start, dynamic current limiting, OVP.**
SL443	**Similar to SL441 with manual power control, long timing periods for hot plates, electric blankets and traffic lights.**
SL444	**Similar to SL441 for 240V permanent magnet motor with thermal trip, current limit detector.**
SL445	**Proportional or On/Off control, temperature trip/inhibit circuitry, LED and alarm drive facilities, for ovens, heaters, industrial temperature controllers.**
SL446	**On/Off servo loop temperature controller, low external component count, for water and panel heaters, refrigerators, irons.**
TBA1085	**Motor speed control**



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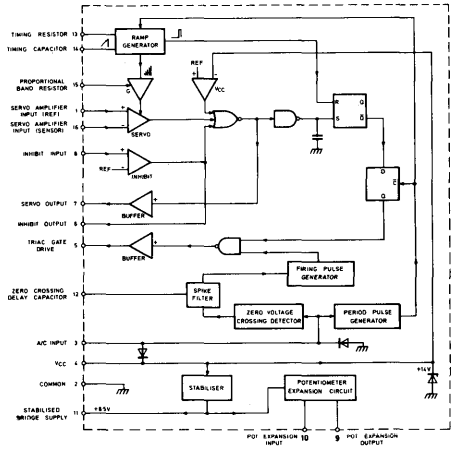


SL445

Processes, Testing and Quality Control

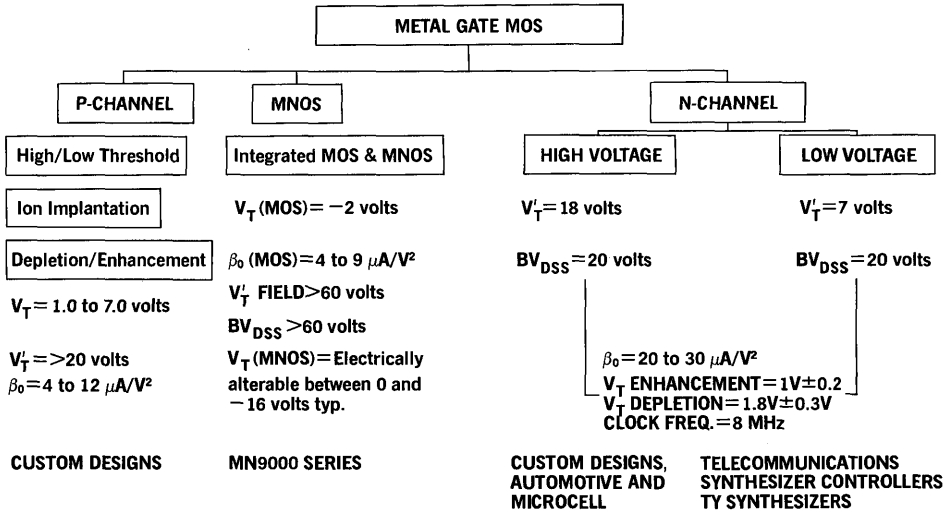
Just as we applied our systems knowledge to the partitioning of functions to make our IC's extremely flexible and cost effective, development ensures that any new products we introduce will be on the leading edge of technology, yet with the same

Plessey MOS Processes

P-channel metal gate MOS has been in production for years and is used for both standard Plessey products and custom LSI. Using ion implantation to modify transistor and field threshold voltages, we can reproduce virtually any p-channel metal gate process, with or without depletion loads.

MNOS (non-volatile) is essentially a p-MOS process with variable threshold memory transistors fabricated alongside conventional MOS transistors. A modified oxide-nitride gate dielectric permits the injection and retention of charge to change the threshold voltage. Current Plessey products will retain an injected charge for at least a year, and include an on-chip high voltage generator so that they may be used with standard supply voltages.

N-channel metal gate MOS uses an auto-registration co-planar process with layout similar to our p-MOS. Ion implantation is used to define the threshold voltage of the depletion and enhancement transistors. The constant-current-like characteristics of depletion load devices give the most effective driving capability, and enhancement-depletion technology simplifies design and increases packing density. The field threshold voltage is also controlled by an ion implant, allowing the use of a lightly doped substrate. This reduces both the body constant and the junction capacitance and results in faster switching speeds.



Plessey Bipolar Processes

Bipolar Process I is a conventional buried +N layer diffusion process with f_t=600 MHz and other characteristics similar to industry-standard processes. Applications range from high reliability military devices to high volume consumer products.

Process Variant	A	B	G	D
Application	General Purpose	Non Saturating Logic	Saturating Logic	Linear Consumer
BV_{CBO} @ 10μA	20V min.	10V min.	10V min.	45V min.
BV_{EBO} @ 10μA	5.3V to 5.85V	5.15V min.	5.15V min.	6.8V to 7.4V
LV_{CEO}	12V min.	8V min.	8V min.	20V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.43V max.	0.32V max.	0.43V max.	0.6V max.
h_{FE} @ I_C=5mA, V_{CE}=5V	40 to 200	50 min.	50 min.	50 to 200
f_T @ I_C=5mA, V_{CE}=5V	500 MHz	500 MHz min.	500 MHz min.	350 MHz min.

Bipolar High Voltage (HV) Process is a variant of Process I that yields an LV_{ceo} greater than 45 volts. Doping levels can be controlled and an extra diffusion used to fabricate a buried avalanche diode with a 40 V breakdown for absorbing powerful noise transients without being destroyed.

Process Variant	CA
BV_{CBO} @ 10μA	80V min.
BV_{EBO} @ 10μA	7.2V to 8.0V
LV_{CEO}	45V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.4V max.
h_{FE} @ I_C=5mA V_{CE}=5V,	80 to 300
f_T @ I_C=5mA, V_{CE}=5V	250 MHz min.

Bipolar Process III uses very shallow diffusion and extremely narrow spacing for high frequency integrated circuits with unusually low power consumption and high packing densities. An f_t of 2.5 GHz allows us to routinely produce analog amplifiers with bandwidths as high as 300 MHz and low power dividers and prescalers that operate at frequencies up to 1.2 GHz. Process variants allow us to produce devices with an extended β, higher breakdown voltages and very small geometries.

Process Variant	WE
Application	Digital
BV_{CBO} @ 10μA	10V min.
BV_{EBO} @ 10μA	5.1V to 5.8V
LV_{CEO}	7V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.5V max.
h_{FE} @ I_C=5mA, V_{CE}=2V	40 to 200
f_T @ I_C=5mA, V_{CE}=2V	1.8 GHz

Bipolar Process 3V is an extension of our Process III. Ion implantation and washed emitters have given the process an f_t=6.5 GHz, allowing us to produce dividers working at 2 GHz, logic gates with delays of less than 500 picoseconds and linear amplifiers at 1 GHz.

Process Variant	WV
Application	Digital
BV_{CBO} @ 10μA	8V min.
BV_{EBO} @ 10μA	3.0V to 5.0V
LV_{CEO}@ 5mA	6V min.
$V_{CE\ (SAT)}$ @ I_B=1mA, I_C=10mA	0.5V max.
h_{FE} @ I_C=10mA, V_{CE}=5V	40 to 120
f_T @ I_C=5mA, V_{CE}=2V	6.5 GHz

Testing and Quality Control

A major thrust of our development work is to ensure that our processes will routinely produce reliable devices. Our Process III has a projected MTBF of 400,000 hours while our Process I is even better.

Our facilities include the latest test equipment (such as the Macrodata MD501, Teradyne J324 and Fairchild Sentry VII and Sentinel) to allow us to perform all the necessary functional and parametric testing in-house. We have an internal capability to provide specific applications-oriented screening, and most Plessey IC's are available screened to MIL-STD-883 and other international specifications. Our quality levels exceed the most stringent military, TV and automotive requirements as a matter of course.

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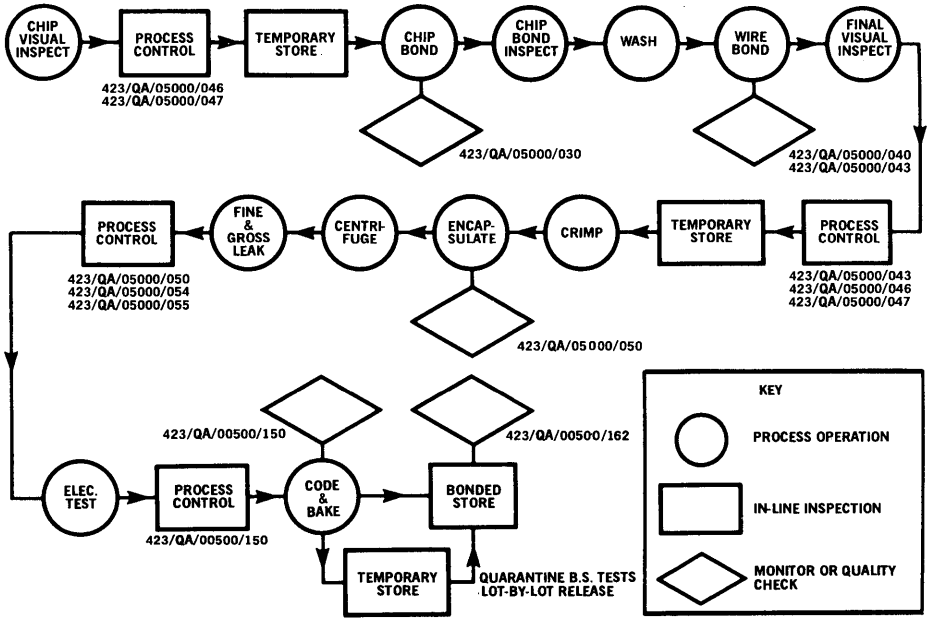
ASSEMBLY OF INTEGRATED CIRCUITS
QUALITY ASSURANCE



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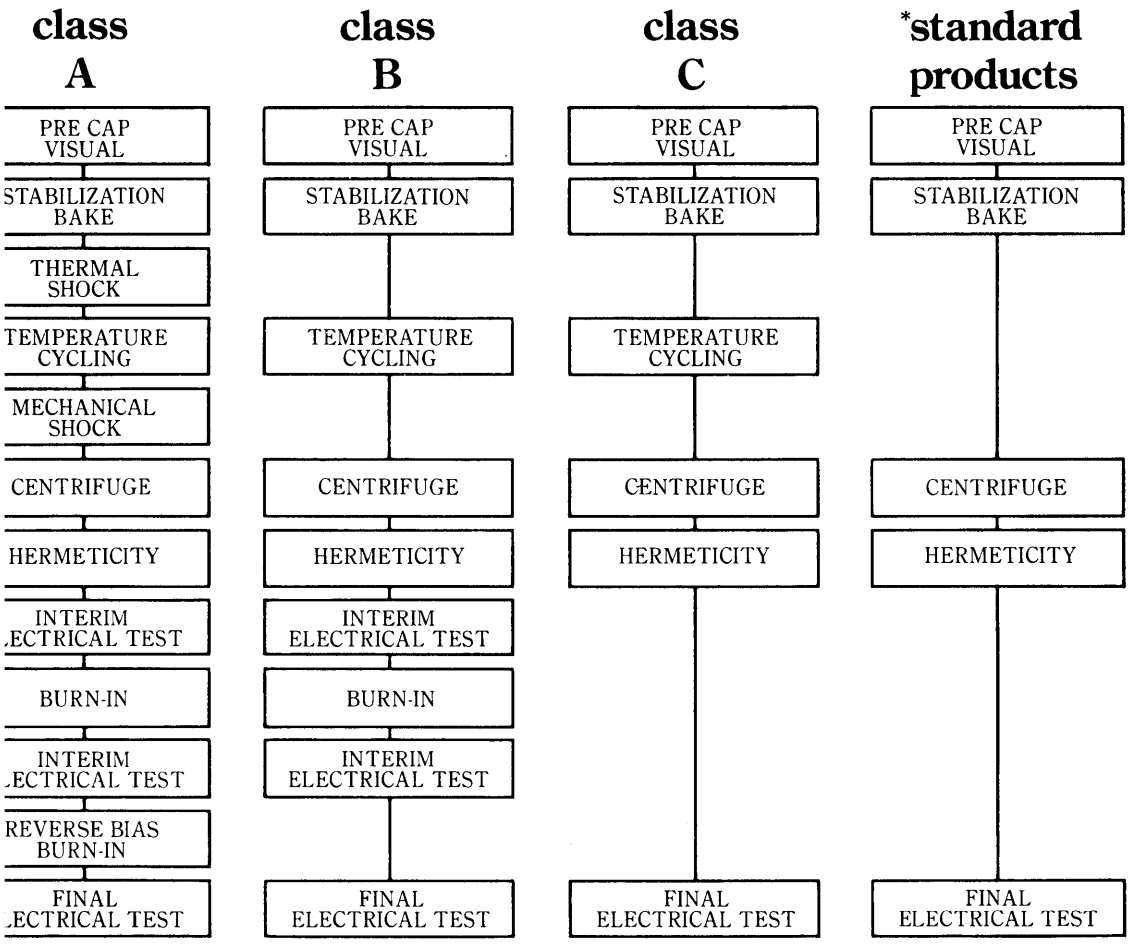

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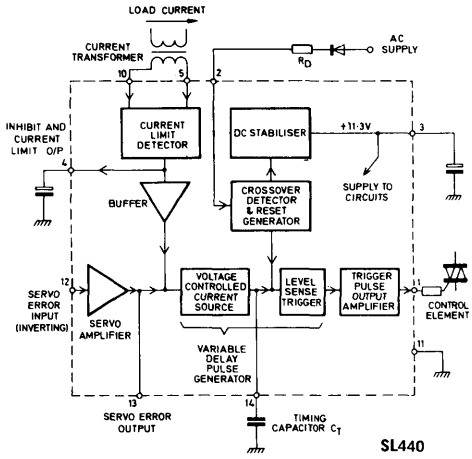

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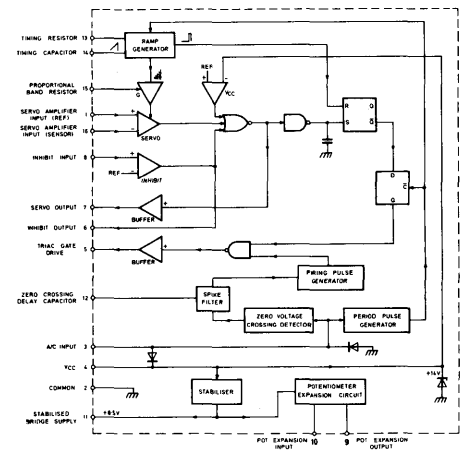

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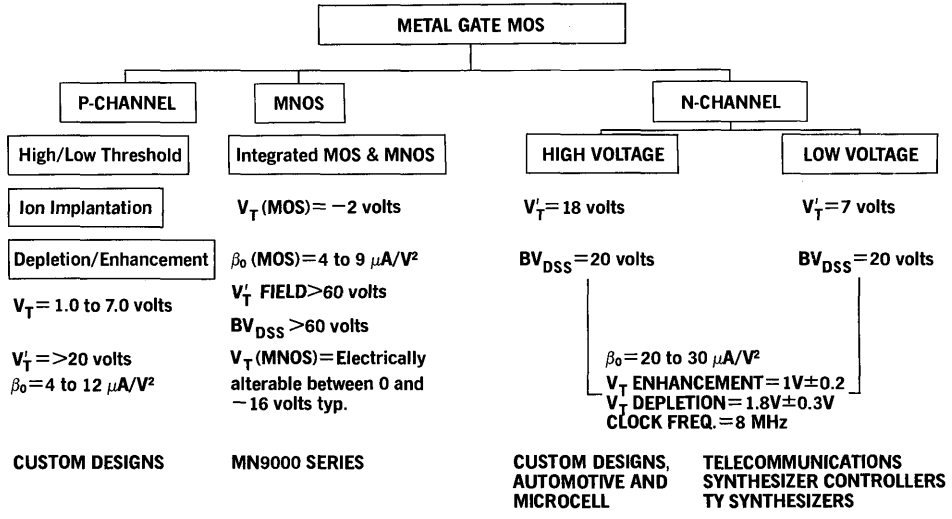

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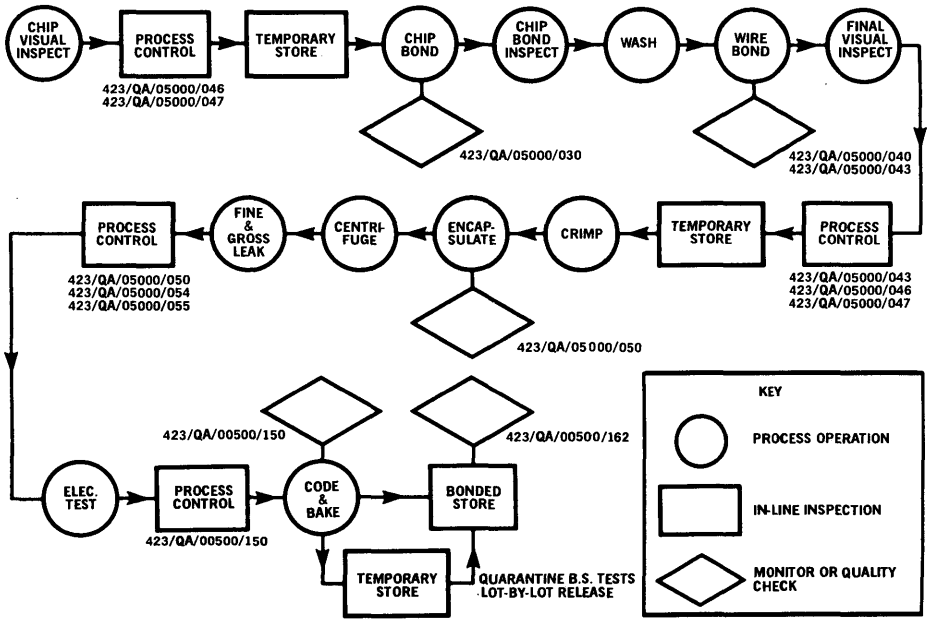

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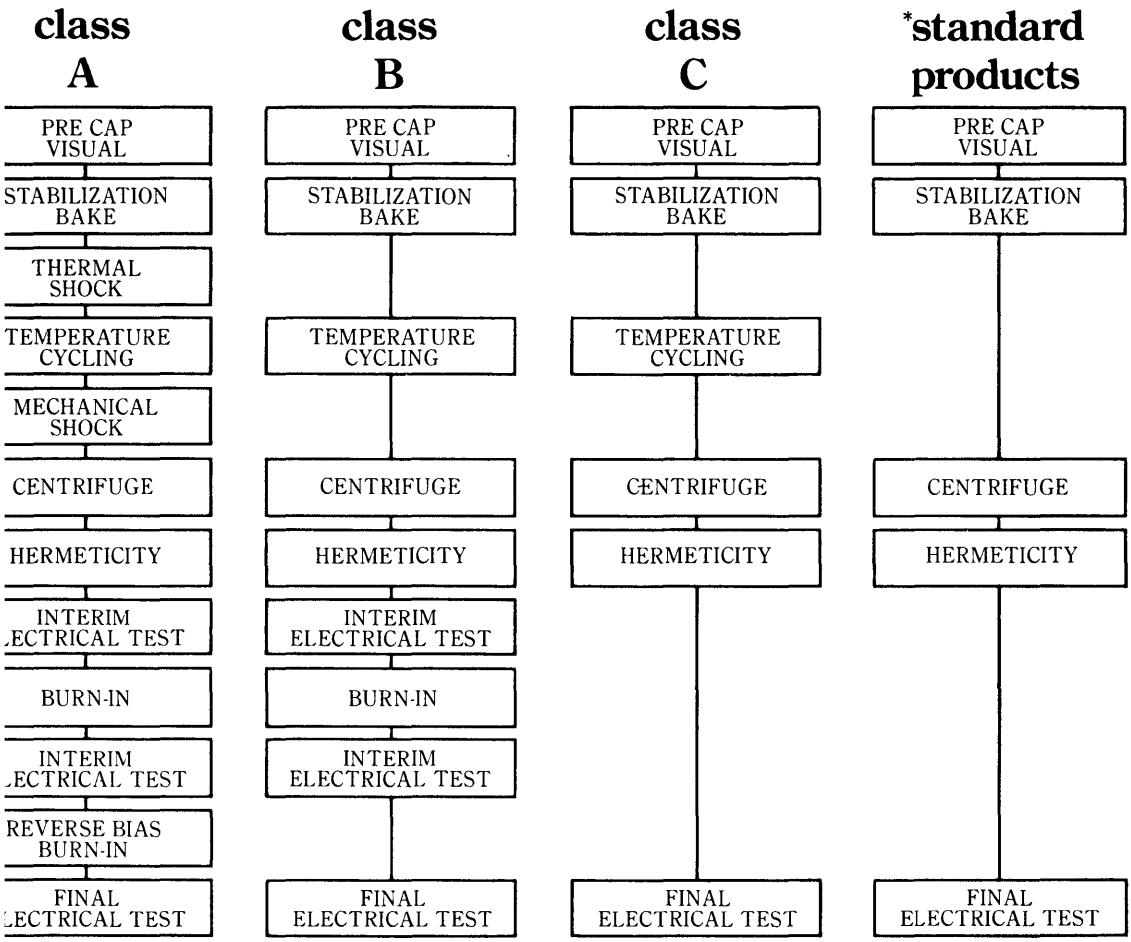

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2. A to D Conversion

Introduction

Most variables encountered in electronic systems change in a continuous or analogue fashion, and indeed most transducers provide analogue outputs. Nevertheless, there is a growing trend to apply more and more digital control and computation hardware to commercial, industrial and military equipment. One reason for this is the increasing availability of digital logic and memory integrated circuits at very attractive prices. Recently, the high speed capability of the ECL logic family has extended the range of frequencies for which digital processing is possible. The advantages of digital processing techniques are well known, and include such benefits as high accuracy and high noise immunity in environments which could seriously impair the performance of an equivalent analogue system. Analogue to digital converters (ADCs) are an essential part of all such systems.

Digital signal processing is now practical at video and IF frequencies and is consequently being applied to television and radar systems. Other areas in which high speed analogue to digital conversion is being used are fast transient analysis, fast data transmission and secure speech transmission.

1 A to D conversion

CONVERSION METHODS

There is a great variety of conversion techniques which are at present being pursued. It is fair to say that the majority of these are more suitable for lower speeds where they have achieved low cost, low power consumption, or extremely high accuracy up to at least 14 bits. When the highest possible conversion speed is essential the choice of techniques is narrowed down considerably.

The majority of ADCs accept an AC input signal, which can occupy an equal positive and negative range, and the input/output function is usually linear. The output code is normally a binary N-bit code in which the all '0's state corresponds with the most negative input voltage and the all '1's state corresponds with the most positive input voltage. In some cases the outputs may be presented as an N-bit output code plus a sign bit, giving the converter effectively N+1 bit accuracy. ADCs do exist which differ from these formats to fit special needs, such as a Gray coded output or logarithmic transfer characteristic.

All parallel

The fastest known conversion method is the all parallel converter shown in Fig. 1. It is so called because 2^n-1 comparators compare the analogue input with an equal number of reference voltages. The reference voltages are uniformly spaced, and span an equal positive and negative range. The centre reference voltage is therefore zero. The outputs of the comparators are encoded by logic circuitry to give an N-bit logic code. A latch signal is fed to the comparators which forces them to make an unambiguous decision, i.e.

give a true logic '0' or '1' at the output, so preventing spurious output codes. In this way, a synchronous output is obtained. This is a very basic converter schematic and a practical ADC may include refinements such as output latches to re-time the output bits, an input sample and hold circuit, or the provision of a "conversion complete" timing signal. The speed of this type of converter is in principle only limited by the time the comparators take to make an unambiguous decision. There is also the advantage that if the "acquisition times" of the comparators are well matched, the system can be operated without an input sample and hold circuit.

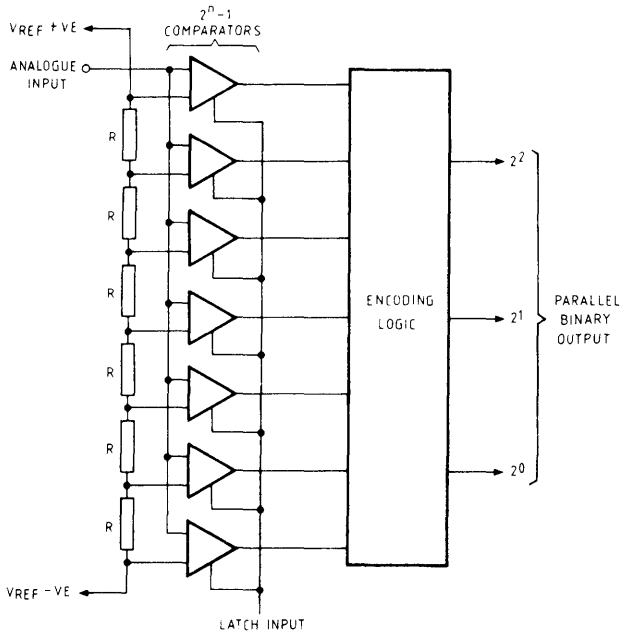

Fig. 1 The all parallel conversion method

All parallel, or "flash" converters as they are sometimes called, can be conveniently constructed using discrete comparators up to four or five bits. Beyond this it is highly desirable to have more than one comparator integrated into a single monolithic chip, to offset the problem of increasing size and cost. It is difficult to distribute the analogue input signal to a large array of discrete comparators with sufficient amplitude and phase accuracy, and to provide adequate latch timing accuracy. In addition, the output encoding gives rise to timing problems for higher bit accuracies. An integrated circuit which offers four or more comparators in a single package will considerably ease the above problems.

All-parallel converters have been built which are capable of clocking at up to 100 million samples per second, and with accuracies of up to 6 bits.

Parallel/series

The parallel/series conversion method is a hybrid form which is a compromise between the characteristics of all-parallel and all-series converters. A variety of designs are possible using 2, 3 or even more stages of conversion. Fig. 2 shows a converter in which two four-bit stages are connected in series to give eight-bit conversion accuracy. The analogue input is fed into a four-bit all-parallel converter of the type previously described, after first being sampled by a sample and hold circuit. Here, a coarse quantisation is performed which provides the four most significant bits (MSBs) of the output code. The output is fed into a four-bit digital to analogue converter (DAC), having eight-bit accuracy. The result is an analogue level which is an approximation of the input to the nearest four-bit code below the original signal. This is then fed into a subtractor circuit element together with the sampled analogue input.

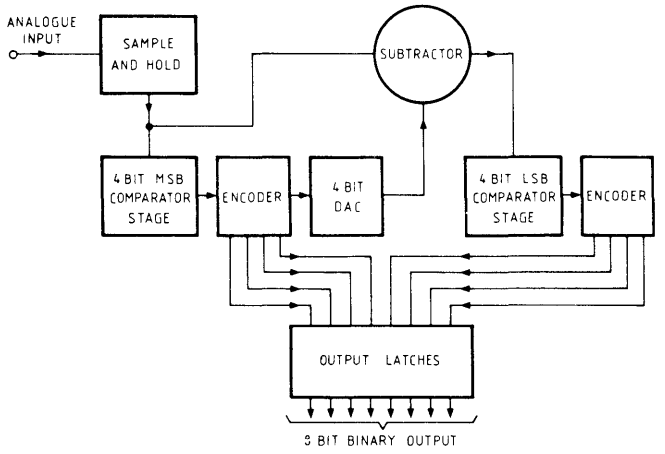

Fig. 2 The parallel series conversion method

The difference voltage will come within the range of the second four-bit ADC stage, which is again an all-parallel converter. The quantised output provides the four least significant bits (LSBs). Since the analogue signal has to propagate through an ADC and a DAC, and be compared with the input, the sample and hold is required to store the analogue signal for approximately one clock period to the full eight-bit accuracy. The outputs from the two stages are re-timed in a group of latches to give synchronous outputs.

The parallel-series converter has the advantage over the all-parallel of using less hardware, and hence less power is consumed. For example, an eight-bit all-parallel ADC uses 255 comparators, whereas a 4 $\times$ 4 bit parallel/series converter uses only 30 comparators. However, because the analogue signal has to propagate through several stages, conversion rate is lower than is possible with the all-parallel converter. The parallel/series ADC therefore provides a compromise between cost, power consumption, size and conversion speed. Other versions of the parallel/series converter may have more stages, for instance, 3 $\times$ 3 $\times$ 3 bit stages could be used to give nine-bit accuracy using 21 comparators, at correspondingly lower speed.

Successive approximation

The third converter to be described is the successive approximation type. It has been hitherto regarded as a slow conversion method, but with today's technology – ultra fast comparators, fast current switching, etc.– a very useful performance is obtainable. An attractive feature of the successive approximation technique is that it requires very little hardware. It is consequently possible to integrate an ADC of this type onto a single chip with eight-bit or higher accuracies. The successive approximation converter, shown in block form in Fig. 3 uses a DAC in a feedback loop. In operation, the shift register sets a 1 in the MSB latch, all other latches being in the logic 0 state. The DAC output is compared with the analogue input and the MSB latch remains set or is reset to 0 depending on whether the analogue input is greater or less than the DAC output. During successive clock periods this process is repeated with bits of diminishing significance. The DAC output therefore becomes a progressively more accurate approximation to the analogue input, taking N clock periods to achieve N-bit resolution. As with the parallel/series ADC a sample and hold is essential, although it may not be included in a monolithic converter. Using present-day technology, a monolithic successive approximation converter of eight-bit accuracy and a sample rate of 15MHz is feasible.

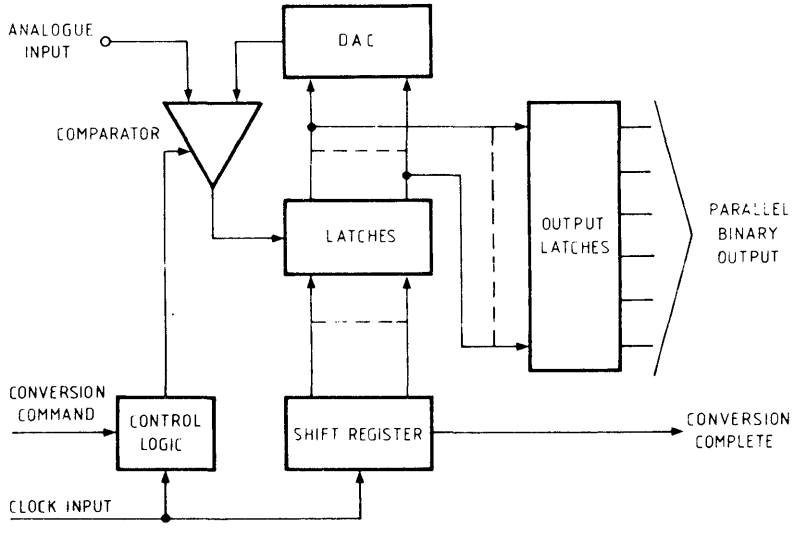

Fig. 3 The successive approximation conversion method

SPEED, RESOLUTION AND ACCURACY

The most important parameters when designing an A-D converter system are speed, resolution and accuracy. Speed is usually expressed as maximum sample rate and the maximum input frequency is limited by the Nyquist theorem to half of the maximum sample rate. In most converters, it is essential that this input limit does physically exist in the form of a low pass filter. Furthermore, the Nyquist limit point is actually 3db down, so for a flat response, the input should be rather less than half the sample rate.

Resolution of a converter is defined by the number of bits available, e.g. an eight-bit converter has a resolution of 1 part in $(2^8 - 1)$ or 1 in 255 (zero is also a step, so 256 levels are defined).

Accuracy may be equal to, or better than, the resolution, i.e. the converter may be specified as $\frac{1}{2}$LSB or even $\frac{1}{4}$LSB, or, exceptionally, $\frac{1}{10}$LSB. While $\frac{1}{2}$LSB is the minimum accuracy that will guarantee monotonicity, $\frac{1}{4}$LSB may be useful when, for instance, the temperature coefficient is $\frac{1}{4}$LSB over the range. In this case, the sum of a $\frac{1}{4}$LSB basic accuracy, plus a $\frac{1}{4}$LSB temperature shift will give a $\frac{1}{2}$LSB accuracy over the temperature range. Many converters are not specified to the most desirable degree of accuracy. A common specification on eight-bit conversion is 1% i.e. 0.5% when the resolution is 1 in 255, i.e. the resolution is greater than the accuracy.

Usually, this type of converter will be monotonic over the full range, but departs from the ideal linearity in the mid-range; the error occurs at the mid-range, because the start and end points are defined by scale and offset factors. At lower speeds, specific systems may demand a higher resolution (i.e. number of bits) than can be achieved with a matching accuracy and linearity. A typical example is high quality audio in which quantisation noise and hence dynamic range is of extreme importance, but absolute accuracy is of less importance.

At video speeds, resolution and accuracy are usually equal except under transient conditions, when small inaccuracies are tolerable – an example is in video processing when the interval between fields may be used for programme source change.

THE COMPARATOR – AN IMPORTANT CIRCUIT ELEMENT

The ADCs described above use at least one comparator. Indeed all conversion techniques use a comparator of some kind. The speed performance in most, if not all, conversion systems is dependent on the response time of the comparator(s). Even low speed converters can require fast comparators, especially when very high resolution is required.

To achieve the highest possible conversion rates, a comparator with an extremely fast response is needed. To make an impact on the attainable performance of high speed converters it is essential to start with the comparator design.

Until recently, commercial comparators have used high gain (greater than 1000) to obtain the mV resolution necessary in A-D conversion.

When the converter operates in a synchronous mode (which is invariably the case in present-day converters) there will be a clock pulse available to enable the comparators to operate in the latching or sample and hold mode. In essence a latch is a positive feedback circuit: during the latch cycle, the gain tends towards infinity. This feature ensures that a comparator of even

very low gain in the sample mode will resolve a 1mV signal. By accepting a low gain, the comparator design can be optimised for a very wide bandwidth and extremely fast response time.

Later sections of this handbook describe the Plessey high speed comparators which use this principle to achieve set up times of 2ns and input to output delays of less than 3ns.

3. Practical System Design

Practical system design

MICROSTRIP TECHNIQUES

Microstrip techniques have been used in the microwave field for many years and are now well characterised. Relatively recently, the advantages of accurate matching and minimisation of reflections associated with microstrip have been adopted for high speed digital circuitry. When the edge speed in a circuit is comparable with the propagation delay down the lines in use, microstrip is needed.

A cross-section diagram is shown in Fig. 4. Points to note are that the devices are usually mounted on the ground-plane side of the double-sided board; the presence of the ground plane accurately defines the line impedances, provides low impedance current path for the ground supply and convenient decoupling for the other rails.

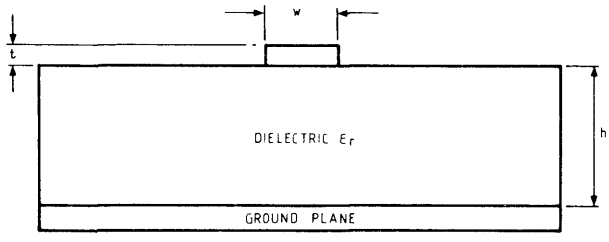

Fig. 4

The characteristic impedance, Zo, of a microstrip line is

$$Zo = \frac{87}{\sqrt{\xi r + 1.41}} \ell n \left(\frac{5.98\ h}{0.8\ w + t} \right)$$

r = relative dielectric constant of the board, typically r = 5 for glass-epoxy.
w, h and t are defined on Fig. 4.

Standard tables and graphs are available in the literature on microstrip to calculate the line width needed for a given Zo (Fig. 5).

In practice, line impedances greater than about 150 ohms are not realisable in the copper-glass-epoxy system.

The technology of microstrip board is relatively straightforward and follows good printed circuit board practice. The use of double-sided board is strongly recommended.

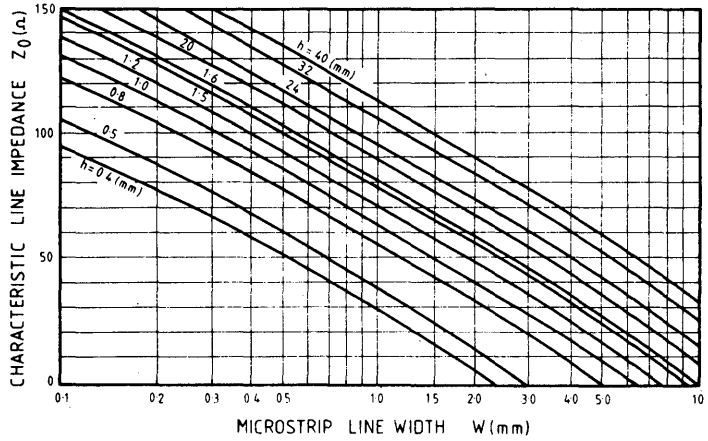

Fig. 5 Characteristic line impedance as a function of the line width for microstrip lines (Parameter is board thickness h(mm) ξr = 5, t = 35μ)

The choice of board thickness and specification depends primarily on the application; best results are obtained with good quality board of reproducible characteristics. The capacitance per unit length of conductor is predictable from modified parallel-plate capacitor formulae; in practice, the graph of Fig. 6 is a good guide. Variations in dielectric constant of the board change Zo in the ratio of about ±2% in Zo for ±5% in ξr.

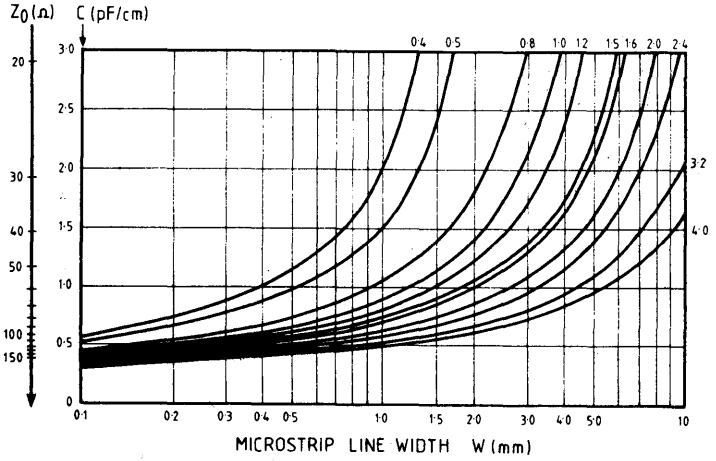

Fig. 6 Intrinsic line capacitance as a function of line width for microstrip lines. (parameter is board thickness ξr = 5, t = 35μ)

The inductance per unit length of the line may be calculated from the formula:

$$Lo = Zo^2 . Co$$

where Zo = characteristic impedance
Co = capacitance per unit length

The propagation delay of the line is approximately

$$t_{pd} = 3.3 \times 10^{-2} . \sqrt{0.475 \xi r + 0.67} \text{ ns/cm}$$

Most glass-epoxy board has $\xi r \simeq 5$, so $t_{pd} = 0.058$ ns/cm. The relationship between t_{pd} and ξr is illustrated in Fig. 7.

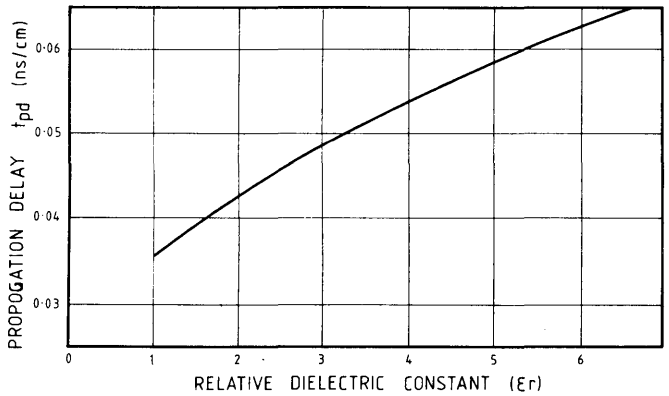

Fig. 7 Propagation delay as a function of the relative dielectric constant of the board material for microstrip lines

Line loading

Most devices connected to the microstrip load the lines capacitively. In some cases, such as logic inputs, there is only a single load capacitance on a relatively long line, and the effect can be ignored. On parallel outputs, especially where settling times are important, the effect of loading on the line must be compensated for. Basically, this means that the total load capacitance per unit length of line must be calculated and then the line designed in such a way that the loaded impedance matches the actual working impedance desired. Load capacitance per device is taken from the manufacturer's data or by measurement from the devices.

A fairly accurate assessment of the inter-device spacing is needed, and the types of device must be considered. Eventually, some figure of C_D, the

load capacitance per unit line length, can be derived. The standard equation for loaded lines is

$$Zo = \frac{Zo'}{\sqrt{1 + \frac{C_D}{C_O}}}$$

where Zo′ is the characteristic unloaded impedance
Zo is the loaded impedance
C_D is the load capacitance in pF/cm
Co is the line capacitance in pF/cm

Tables and graphs for this function are shown in Fig. 8.

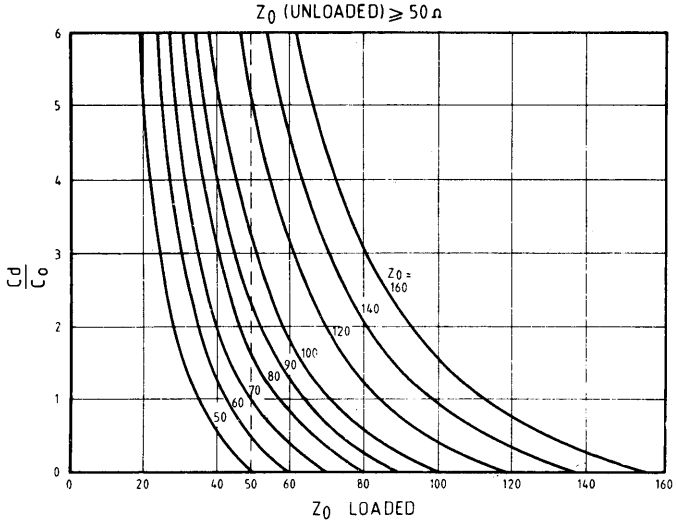

Fig. 8

Tables and graphs for this function are shown in Fig. 8.

Loading in most systems is distributed, in the way described, along the lines but, in reality, does represent discrete 'lumps' of capacitance at finite points, and so any compensation scheme cannot be perfect, but practical systems if well-designed show minimal line impedance disturbance. Of course, the propagation delay is increased by capacitive loading, in the ratio

$$t_{pd} = t'_{pd}\sqrt{1 + \frac{C_D}{C_O}}$$

where t_{pd} = final delay
t'_{pd} = delay of unloaded transmission line

This function is illustrated in Fig. 9.

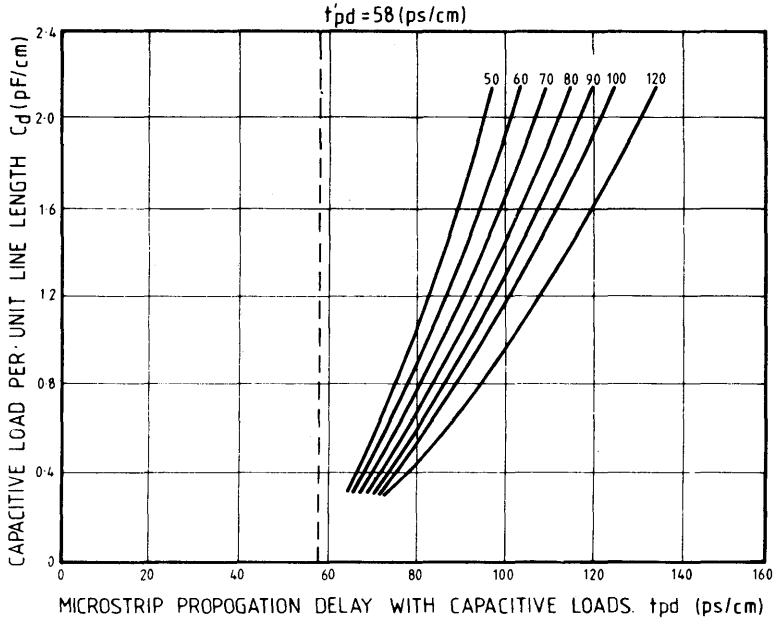

Fig. 9 Variation of the propagation delay line of a microstrip line as a function of the capacitive load per unit length. ξr = 5, Parameter is Z_o

ECL IN ANALOGUE TO DIGITAL CONVERTER SYSTEMS

Plessey A-D products are ECL compatible in terms of input and output logic levels. If full use is to be made of the advantages of ECL, proper transmission line design rules must be observed. Fig. 10 shows a simple line with driver and load. Initially, we assume that the line delay is appreciably longer than the rise and fall times, so that reflections occur at full amplitude. The output voltage swing at point A is a function of the internal device voltage swing, the output impedance, and the line impedance

$$V_A = V_{INT} \times \frac{Zo}{Ro + Zo}$$

Normally, Ro is small, so $V_A \simeq V_{INT}$.

This signal arrives at point B after time t. The voltage reflection coefficient at the distant end of the line is ρL, which is given by the formula

$$\rho L = \frac{R_L - Zo}{R_L + Zo}$$

If $R_L = Zo$ there is no reflection; even if R_L is an approximation to Zo, the reflections will not be large, as a 1% change in R_L changes ρL by only 0.5%.

When a reflection occurs, however, it will return to A, arriving at a time 2t, and be reflected with a reflection coefficient

$$\rho s = \frac{Ro - Zo}{Ro + Zo}$$

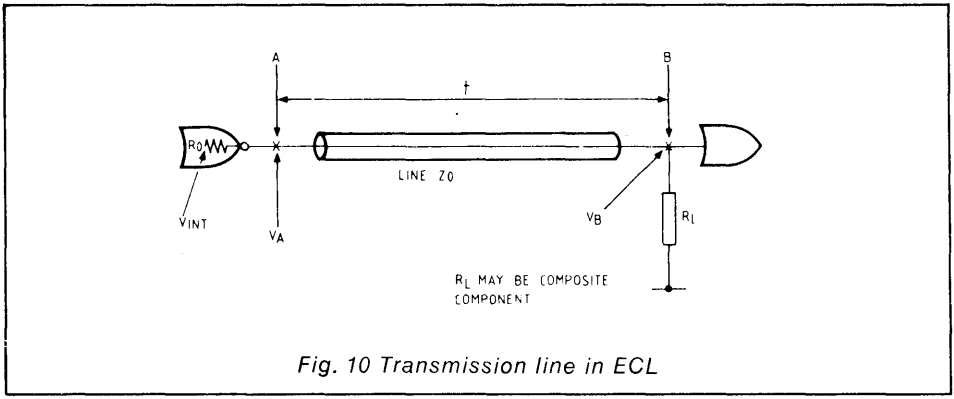

Fig. 10 Transmission line in ECL

In the worst case conditions, the signal will suffer many reflections of significant amplitude: clearly this is not permissible, as it represents 'ringing' on the line. In ECL practice, ringing should be maintained below 15% under-maintained for short runs; Table 1 illustrates the maximum lengths allowed, assuming 20%–80% rise/fall times of 3ns.

Line impedance	Fanout			
	1	2	4	8
50	21.1	19.1	17.0	14.5
68	17.8	15.7	12.7	10.2
75	17.5	15.0	11.7	9.1
82	16.8	14.5	10.7	8.4
90	16.5	13.7	9.9	7.6
100	16.0	13.0	9.1	6.6

Permissible unterminated line lengths (cm)

Table 1

The simplest termination scheme is shown in Fig. 11a. Since the input impedance of ECL parts is relatively high, R_L is made equal to Zo. Then $\rho L = 0$ and the voltage on the line is the full ECL swing. In large systems, this technique is used extensively but has the disadvantage of requiring a —2 volt rail in addition to the normal supply. Fig. 11b shows a convenient realisation of the same circuit using 0 and —5.2 volt rails only. With parallel terminated lines, the load provides the pulldown for the driving device. This termination is the fastest form for ECL. The full amplitude signal is progapated down the line, undistorted and, as $\rho L \simeq 0$, overshoot and ringing are practically eliminated. The Thevenin form (Fig. 11b) is fully equivalent to the system of Fig. 11a but operates on more convenient power rails. Clearly, the parallel combination

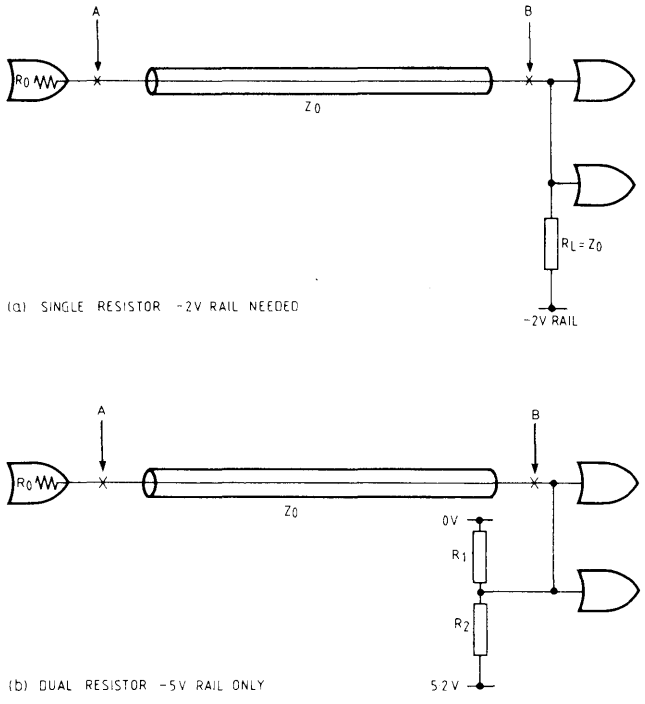

Fig. 11 Terminated line parallel termination
(a) Single resistor —2V rail needed
(b) Dual resistor —5V rail only

of R_1 and R_2 must be equal to Zo, while the defined voltage at the input must be the —2v used in Fig. 11a (when the driver output is 'low'). These conditions lead to:

$$\text{for } Z_0 = 50\Omega$$
$$R_1 = 81\Omega$$
$$\text{and } R_2 = 130\Omega$$

General results are given in Fig. 12.

When driving a large fanout, loads may be distributed along the full length of a parallel terminated line, although only a single line is permissible at 50Ω.

The other major form of line termination is the series system (Fig. 13). Reflections are eliminated at the driving end of the line by making

$$R_S + R_O = Z_O$$

The reflection coefficient of the load is —1.

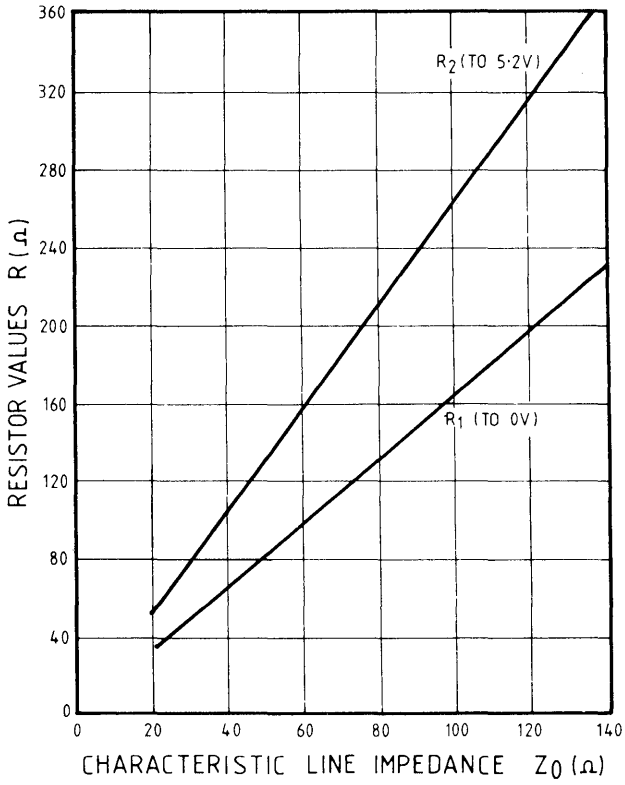

Fig. 12 Thevenin equivalent resistors for parallel line-termination

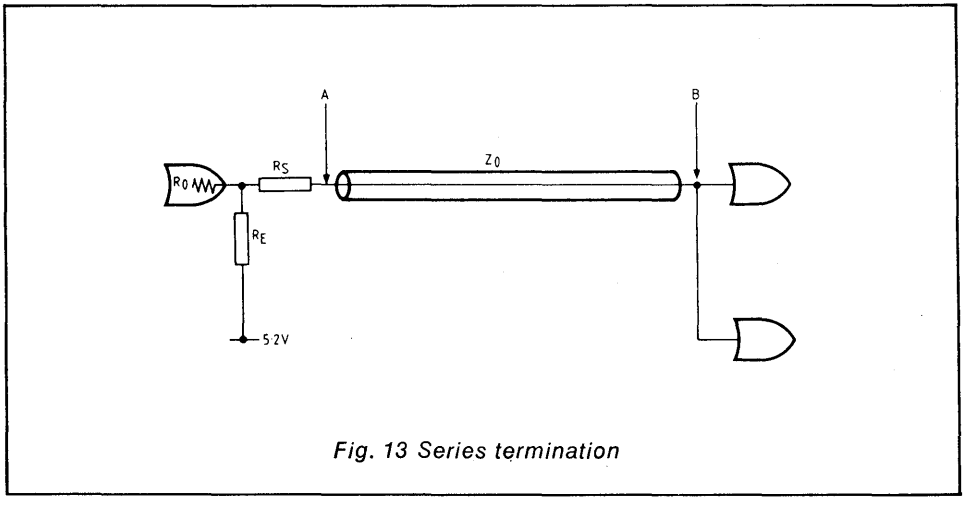

Fig. 13 Series termination

This represents a 100% reflection at the load end of the line. As the propagated signal is of only half amplitude, the 180° phase change at the load interface is essential to provide the full logic swing at this point.

Typically, R_O for ECL10k devices is 7Ω, so in 50Ω systems, $R_S = 43\Omega$. R_E is fanout dependent, and is given by

$$R_{EMAX} = \frac{10Zo - Rs}{n} \text{ where } n = \text{fanout.}$$

The advantage of series termination is in simplicity, both in configuration and power supplies. Disdavantages are that distributed loading is not permissible, although lumped loading at the line end is satisfactory.

Voltage drops across Rs limit loading to less than 10. However, multiple Zo lines, with separate Rs resistors may be used. Overall slower propagation delay in series terminated mode may be a disadvantage, partly overcome by multiple transmission lines. This leads to the final line termination form, Fig. 14.

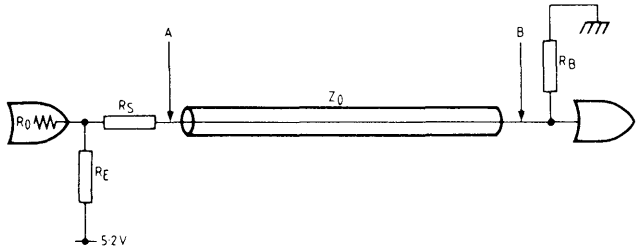

Fig. 14 50Ω line driver

It can be seen from Fig. 14 that the driver is doubly terminated, and resembles both series and parallel systems. At the distant (B) end of the line,

$$R_B = Zo$$

so there is no reflection.

At the driving end, Rs acts as a series damping resistor, and, although it is not generally possible to accurately match Zo at this point, any residual reflections on the line are further attenuated. The chief advantage of this scheme is the ability to drive a 50 ohm line terminated directly to ground, while using the conventional 0V and —5.2V supplies. Another advantage is the ability to drive long lines with low reflections; the disadvantage is that the effect of Rs and R_B is to reduce the signal amplitude on the line; the device at B should be some form of line receiver or comparator.

At the driving device output, the 'low' level must be pulled down to —2 volts. Therefore

$$\frac{Rs + R_B}{Rs + R_E + R_B} = \frac{2}{5.2}$$

and $R_B = Zo$ (usually 50Ω for output line driving)
and R_E may be set within limits, arbitrarily, to provide an adequate 'pull-down' current.

Convenient practical values are

$$\left.\begin{aligned} R_B &= 50\Omega \\ R_S &= 27\Omega \\ R_E &= 130\Omega \end{aligned}\right\} \text{ Nearest preferred values.}$$

Further information can be obtained from ECL data and applications handbooks.

A TYPICAL SYSTEM

Modern equipment practice is heavily weighted in favour of 50Ω systems, and in key items such as coaxial cable and connectors it may not be easy to procure a wide range of alternatives. In this environment, where board-to-board, or board-to-external facility connections are used, coaxial 50Ω design is strongly advised. On an individual board, interconnection at 50Ω is commonly used for analogue lines, although digital signals may be conveniently operated at higher impedances. For the ultimate in performance, however, 50Ω (loaded) systems are preferred.

System design demands a range of component blocks with, desirably, a high state of integration. However, two circuit blocks currently not economically available in integrated form are the buffer amplifier and the sample-and-hold. Typical applications of the buffer amplifier are high speed driving of 50Ω analogue lines, DAC output buffering, and sample-and-hold buffering. A commercially available hybrid buffer amplifier (LH0063) has been used with success. Discrete buffer amplifiers can be constructed, the main parameters being slew rate and phase distortion. The ability to drive 50Ω lines is essential.

A sample-and-hold is needed in those video systems where the aperture time must be short compared with the time taken for the A-D to perform the conversion. Typical examples are systems where series-parallel type converters are used; an input analogue sample-and-hold is essential, as the LSB's are encoded some time after the MSB's. Fully parallel analogue to digital converters can operate without sample-and-hold; this is sometimes known as 'sampling-on-the-fly'. In this case, the parallel converter, by virtue of its latch action, performs an effective sample-and-hold function on the digital output word.

One measure of a sample-and-hold 'quality' is the aperture time, which is the uncertainty in the time at which the sample is taken. The best analogue sample-and-holds have $t_{aperture} = 20$ ps rms. Digital sample and holds are more difficult to measure, but should be approaching this figure. The aperture time requirement of a sample-and-hold is calculated from the maximum input slew rate and the accuracy required. If the maximum input frequency is f, and the number of bits is n, then:–

$$t_{aperture} < \frac{1}{2^{n+1}.\pi.f.}$$

In an 8-bit system, if the input bandwidth is 10 MHz, and therefore the sample rate > 20 MHz, the required aperture time is calculated to be 62 ps or better.

Current analogue high speed sample-and-hold circuit design is discrete, using a ring of Schottky diodes for fast switching, usually transformer driven, The basic circuit is shown in Fig.15, A long tailed pair of very fast transistors is driven by a narrow ECL-derived pulse.

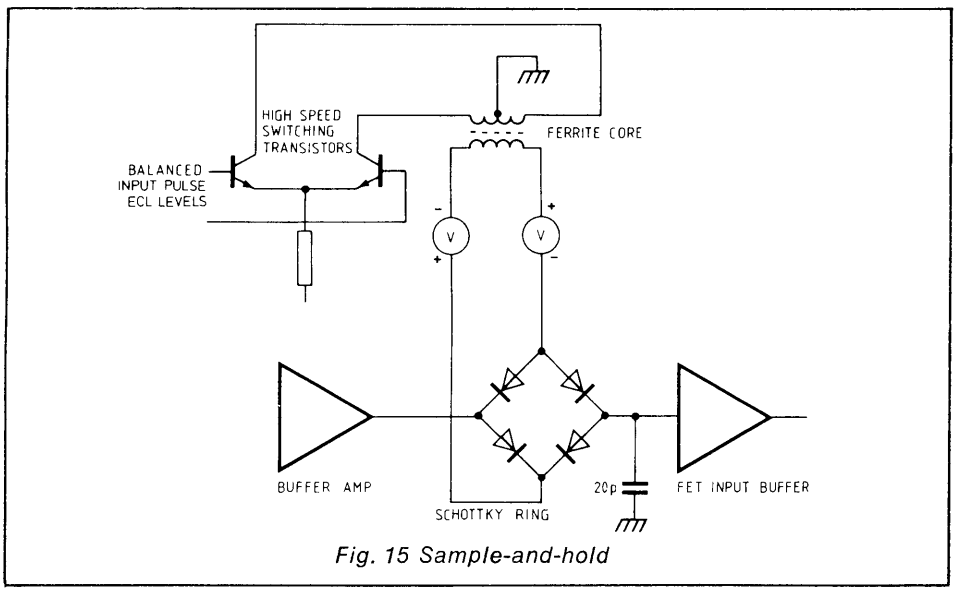

Fig. 15 Sample-and-hold

Normally, the diode ring is biased 'off' but, during the pulse, a relatively large forward current, of the order of 20–30 mA, is driven through the ring. The 'hold' capacitor charges to the voltage present at the output of the driver stage. After the pulse, the only discharge paths for the capacitor are the internal leakage, the diode ring reverse leakage, and the input current of the buffer amplifier. Low discharge rates imply low 'droop' of the signal output from the buffer amplifier; an FET input for the buffer is usually necessary. An advantage of this type of circuit is the full balance, which tends to cancel out feedthrough of the sampling pulse. The limiting factors are the time taken for the input pulse to switch the diodes, the parasitic capacitances of the diodes, and the finite input current and bandwidth of the buffer amplifier.

Digital sample-and-hold facilities are sometimes provided in all-parallel converters, by supplying a latch signal to all comparator stages in precise synchronism with the input analogue voltage. This means that the propagation delays of the lines must be accurately designed. When properly designed, digital sample-and-hold will compare favourably in aperture time with the best analogue circuits, and have the additional advantage of an indefinitely long 'hold' time, making them ideal for fast sample, long hold applications.

Testing the assembled system

The usual test instrument for high speed A-D systems is the oscilloscope, either real-time or sampling. Certainly, the oscilloscope display will illustrate whether the device is operating, and give some idea of the accuracy, limited to about six bits or so in dynamic range by the on-screen resolution. A fast D to A converter can help in A-D projects by reconverting the digital output so the difference between signals can be examined, either in the analogue mode by D-A converting the A-D output, or digitally, by D-A converting a digital input and reconverting in the A-D. In either case, the permissible error function is relatively easily described and is amenable to calculation.

The A-D and D-A test method was applied to a 5-bit A-D converter with the results shown in Figs. 16 and 17. The first of these shows the digitising of a 300 kHz ramp to 5 bits resolution; there are no missing codes and no significant glitches. Sampling near the Nyquist rate is shown in Fig. 17. The technique here is to set up for a small difference frequency between the input signal and half the clock frequency. The oscilloscope timebase is set to a relatively low sweep rate, and the output waveform observed is the 'beat' frequency between the input and half the clock rate. If the clock were to be set at precisely twice the input frequency, the display would consist of only two sample points per cycle of the input, positioned according to the phase separation between the input and the clock. With a small difference in frequency, successive conversions produce an output waveform in a manner similar to a sampling oscilloscope.

No sample-and-hold was used on the A-D; the on-chip latches proved satisfactory to a clock rate of 125 MHz.

One of the major problems in practical systems is ripples caused by reflections. A useful tool in checking line impedances is the time domain reflectometer; accuracies of 1% in line impedance measurement can be made, and line discontinuities are detected as distances in physical dimensions, so positive location is possible. Redesign of the defective components may significantly help the overall system performance.

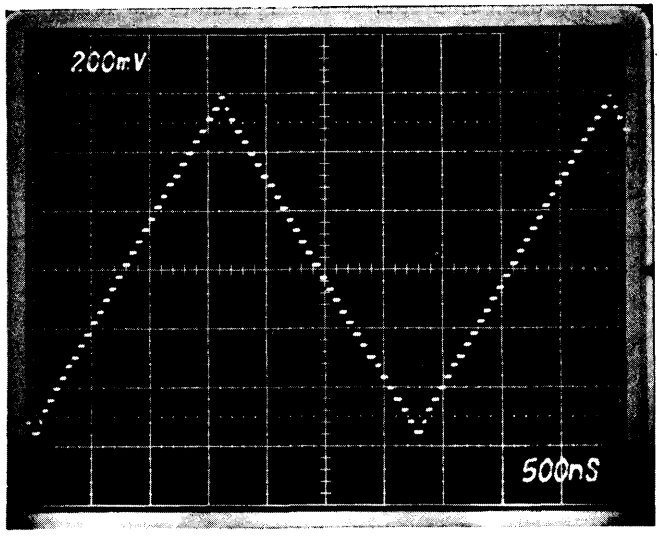

Fig. 16

4. The SP9750 Comparator

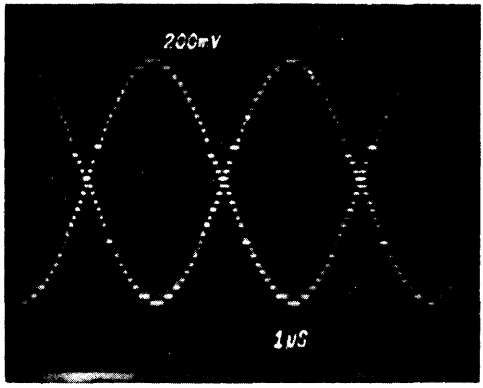

Fig. 17

The SP9750 comparator

GENERAL DESCRIPTION

The SP9750 is a high speed comparator tailored to the needs of the parallel/series type of converter described in Section 1.

Its most important features are:

1. The response is faster than other commercially available comparators

2. Integrated onto the comparator chip are additional features relevant to the construction of fast A-D converters.

The addition of the extra features on to the comparator not only reduces the system cost and complexity but also allows higher performance systems to be built.

Using the low gain principle already discussed, the comparator design could follow the latest high frequency amplifier practice. Fig. 18 shows the schematic diagram of the comparator section of the SP9750. It consists of a

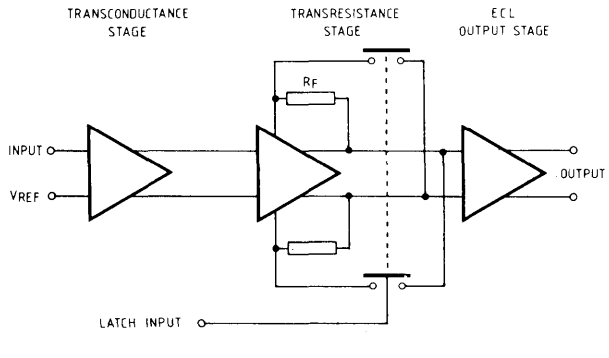

Fig. 18 Schematic diagram of the comparator section of SP9750

mutual conductance or "gm" stage, a trans-resistance second stage, finally feeding an ECL logic output stage. The trans-resistance stage is a shunt feedback amplifier in which the transfer resistance is approximately equal to the feedback resistor value. The input impedance of this stage is low and so the effect of shunt capacitance on this point is minimised. Output impedance is also low giving similar advantages. The resulting circuit has a 300MHz bandwidth in the sample mode and can acquire an input signal change in 2ns. The input offset voltage is ±5mV and the resolution is 1mV, i.e. ±0.5mV.

In the design of very high speed converters, the propagation delays between IC packages have a strong influence on the maximum conversion speed attainable. By including additional system functions on the comparator chip these are minimised, and the bonus of a lower package count and lower power dissipation also ensues. The following four functions are available:

1. A two-input gate
2. Four emitter follower outputs from (1) for wired "OR" decoding
3. A precision current source set by an external resistor
4. A high speed precision switch for (3)

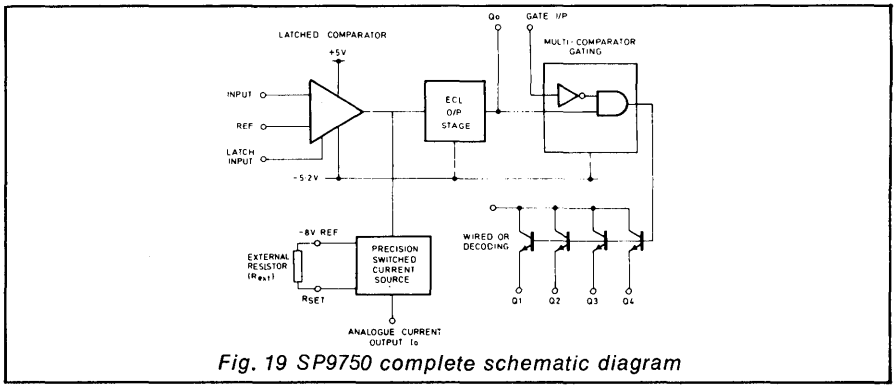

Fig. 19 SP9750 complete schematic diagram

These are shown in block form in Fig. 19. Fig. 20 shows how fifteen SP9750s can be interconnected in a four-bit converter stage. The comparators are connected to form a four-bit all-parallel ADC similar to Fig. 1. The two input gates decode the comparator outputs by detecting the highest level comparator with a logic '1' at the output. The gate at this level puts out a unique '1' to the four emitter followers which can be wired "OR" connected to give a four-bit binary code. Also shown in the diagram is the function of the precision current output. These currents, which are equally weighted for all comparators, turn on when the comparator input is above the reference voltage. Therefore by summing all of these currents, an analogue reconstruction of the input signal to the nearest four bits below the input is obtained. Only fifteen comparators are required to construct a 4-bit ADC and a 4-bit DAC. Such a stage can be used as the MSB stage of a parallel/series type converter. The temperature compensation of the current output is sufficient to allow its use in converters of at least eight-bit accuracy. Similar stages can form the LSB stage of a parallel/series system, only in this case the current output would not be used.

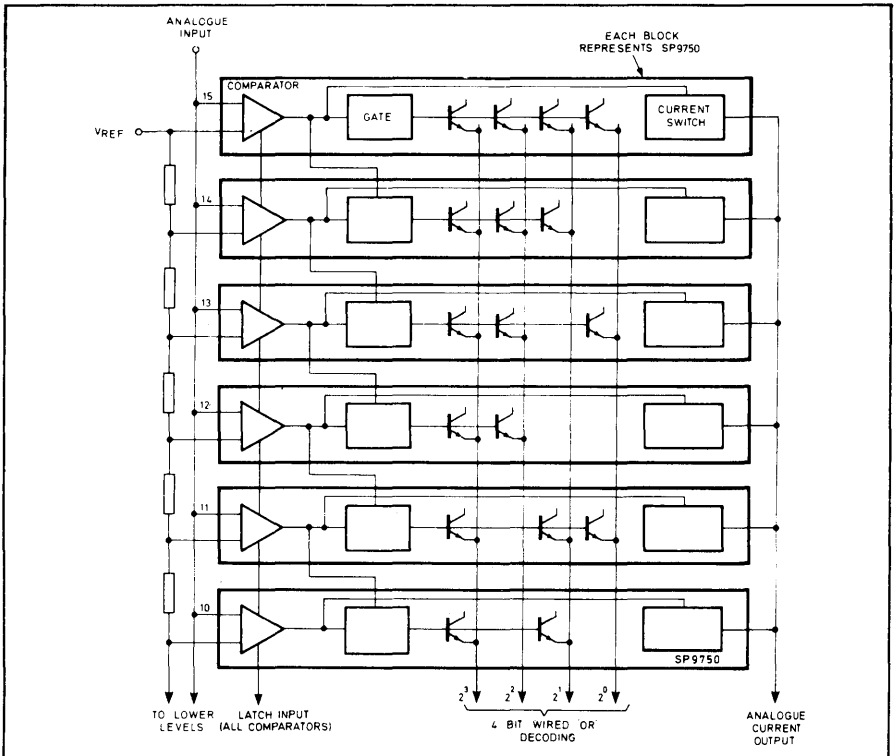

Fig. 20 A 4-bit converter using SP9750 showing the top 6 levels only

The SP9750 has been optimised for use in a four by four bit parallel/series converter system, but it is by no means limited in its application. It is not only being designed into a variety of other systems, but also its extremely fast response has found it a place in such areas as fast pulse detection and instrumentation.

Circuit description

Fig. 21 shows the complete circuit diagram of the SP9750. The inputs are buffered with emitter followers to avoid the switching effect of input currents which would exist with a direct connection to the long-tailed pair first stage. The diodes in the collectors of the first stage are for DC level shifting. The DC conditions are arranged so that for a perfectly matched circuit with the inputs shorted together, there is zero voltage across the feedback resistors (R_f).

The output from the second stage which is a swing of about 400mV is fed into the current switch via an attenuator. This direct route to the current switch gives the fastest possible D to A function. The attenuator avoids using excessive drive to the switch which would increase the settling time of the analogue current output. The analogue current source transistor uses a novel connection of transistors which minimises the effect of temperature and Hfe etc, on the output current stability.

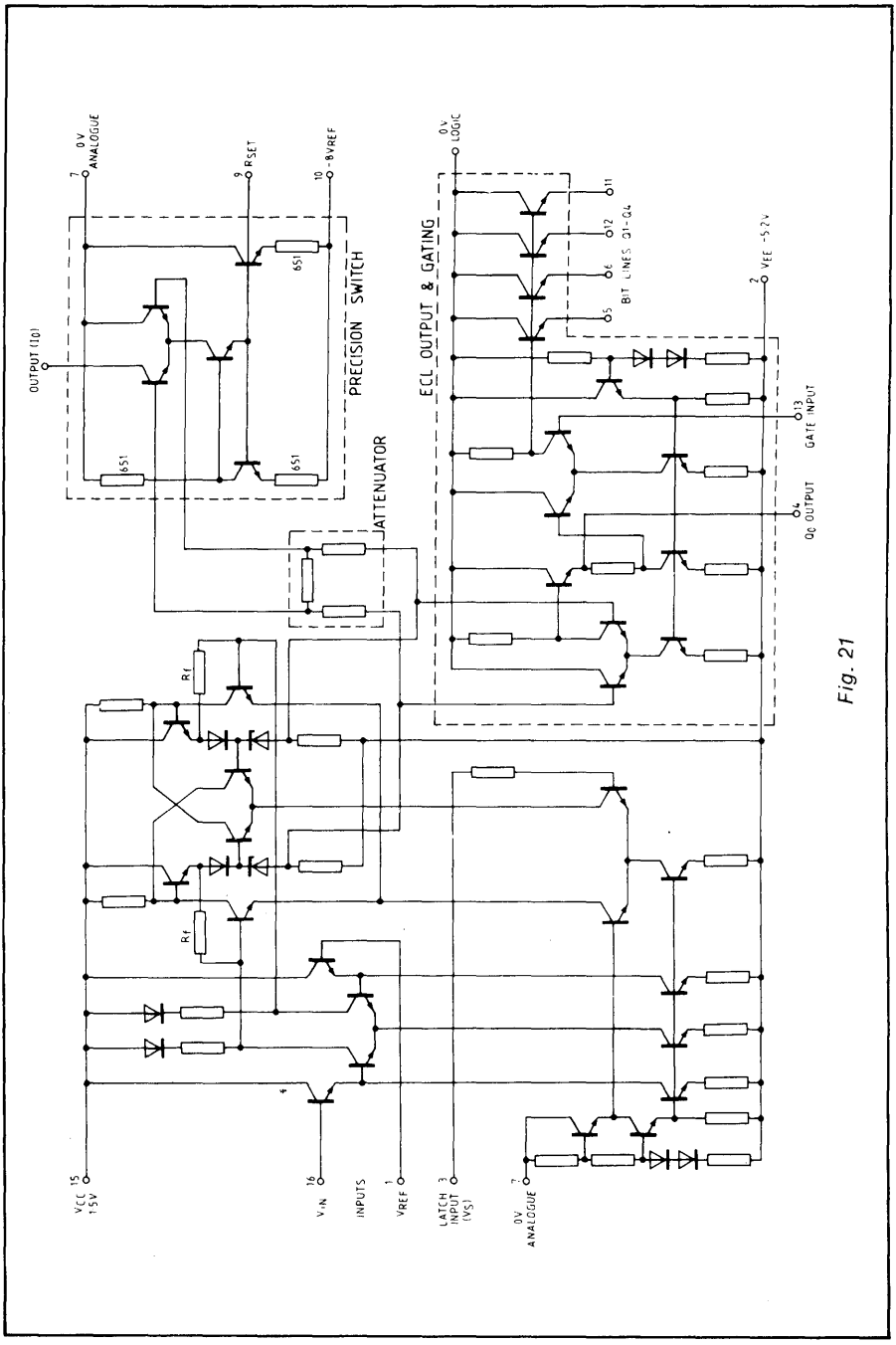
0V ANALOGUE
RSET
-8VREF
0V LOGIC
OUTPUT (10)
651
651
651
PRECISION SWITCH
ATTENUATOR
ECL OUTPUT & GATING
BIT LINES Q1-Q4
VEE -5.2V
GATE INPUT
Q6 OUTPUT
Rf
Rf
VCC 15 +5V
V-IN 16
INPUTS
VREF 1
LATCH INPUT (VS) 3
0V ANALOGUE 7

Fig. 21

The ECL output stage is conventional but an unusual circuit is used to provide the comparator output gating. The Boolean function required is: gate output = $A\bar{B}$, which might be described as a partial exclusive 'OR' function. It is achieved by level shifting the B input by one half of an ECL output voltage swing, and feeding this into a single ECL gate structure. This circuit uses minimal chip area. Four emitter follower outputs from the gate are provided which can be wire OR-ed as previously described.

Conversion rate/Hardware tradeoffs

An 'n' bit converter can be arranged in a number of ways using parallel and series parallel techniques. For example, three stages could be used, each resolving some of the bits.

i.e. $a + b + c = n$

In an 'a' bits conversion, the number of comparators needed is $(2^a - 1)$. Thus the total number of comparators is:–

$$(2^a - 1) + (2^b - 1) + (2^c - 1)$$

In some circumstances, under and over-ranging may be needed, which will require two extra comparators.

Typical examples are the 4 × 4, two stage converter for eight bits, where:–

$$a + b = n$$
$$4 + 4 = 8$$

Number of comparators $= 2^4 + 2^4 - 2 = 30$

When stages are cascaded in this way, the interstage delay must be taken into account. Of primary interest is the D/A current output settling to the desired accuracy.

Each SP9750 contributes one fifteenth of the full scale current, and only one or two comparators are likely to be in a critical settling condition when the latch closes. Therefore if settling to $\frac{1}{2}$ LSB is required (0.2%) two comparators need to settle to 3% or 1.5% for individual comparators. This takes place in less than 10ns. Allowing 10ns for the interstage difference amplifier to settle and a further 10ns for the sample and hold function and logic timing errors, the total conversion period is 30ns or a sampling rate of 33MHz. The corresponding figure for 3 stage is 20–25MHz.

Improved circuit design techniques would increase these figures. For instance, analogue delay could be used between stages to equalise the settling delay of the D/A current output. Perfect cancellation would reduce the conversion period by 10ns bringing the sampling rate to 50MHz. Another technique which has been used is additional comparators in the second or subsequent stage to correct errors from the first stage brought about by latching the first stage before the sample and hold has fully settled. The improved performance offered by such circuit innovations is traded against increased circuit complexity and hence cost.

D TO A CONVERTER USING THE SP9750

When used as originally intended, in a 4 × 4 parallel-series ADC, the output currents from the first four bits of conversion are summed to produce the interstage digital-to-analog function. It is this D-A facility which is used here, but with a binary weighting for the output currents instead of the equal weighting of the A-D system.

A total of 'n' devices only are needed for the 'n' bit conversion, unless the MSB current needed is more than 10mA. If, say, 20mA MSB current is needed, two devices will run in parallel, as in the scheme to be described, giving a total of 'n + 1' devices. The D-A system block diagram is Fig. 22.

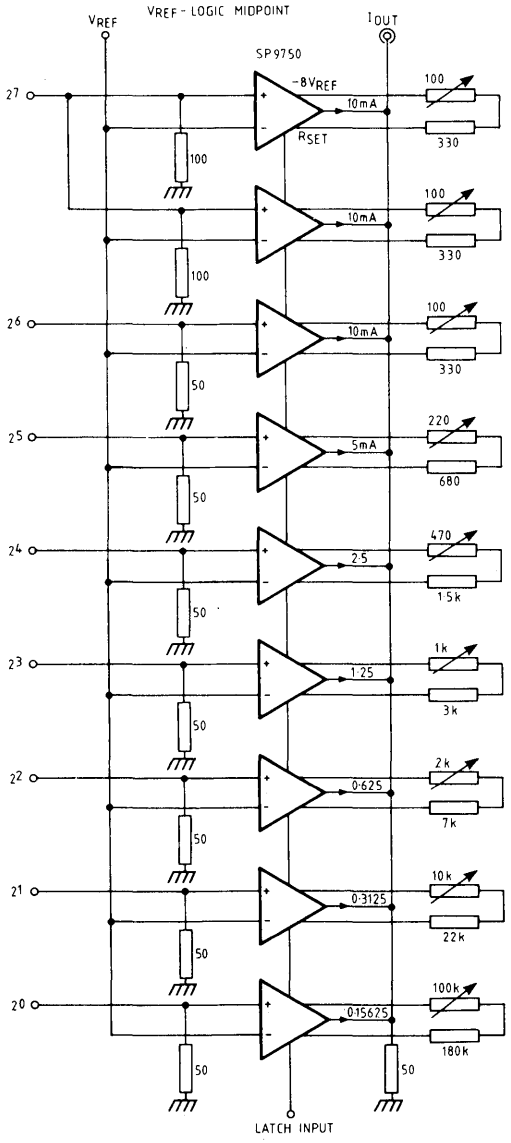

Fig. 22 8-bit DAC using SP9750s

In the D-A application, the 'analog' inputs are switched by logic signals from the 'n' bits of incoming data, giving a marginal improvement in the operating speed compared with normal analog operation. The ancillary facilities ($Q_0 - Q_4$ outputs) which are used in the ADC encoding matrix are not used in the DAC. The SP9750 incorporates a latch, as is becoming standard in high speed comparators, and this feature is exploited here to provide a fast digital sample-and-hold. The current output settling time (10ns to 0.2% for the SP9750) is the main limiting factor in this type of DAC; eight-bit accuracy should be available in about 10–15ns from the input command.

The comparator has a maximum input current of 25μA, which allows it to be set up to receive logic input swings (ECL or TTL) by connecting the reference input to the appropriate voltage. The ECL input to the latch stage is made low for follow or high for hold.

The output current is set by an external resistor and the −8 volt rail, which should be stable enough for the accuracy needed. The maximum output current from a single device should not be much more than 10mA; the relationship of output current to negative reference rail is nominally

$$I_{out} = \frac{V_{rail}}{2 \times R_{ext}}$$

In practice, deviations from this rule are found at low output currents, due to on-chip bias conditions, and a table has been drawn up (Table 2) which illustrates the values of R_{ext} for given output currents.

Output current (mA)	Tail resistor (R_{ext})	
	Fixed	Variable
(mA)	(Ω)	(Ω)
10	330	100
5	680	220
2.5	1.5k	470
1.25	3k	1k
0.625	7.5k	2.2k
0.312	22k	10k
0.156	180k	100k

Table 2

System Aspects

The most used type of high-speed DAC is probably the eight-bit system, so the description here is for eight bits, with an MSB of 20mA, which requires two SP9750s in parallel. No problems are encountered in parallel device operation. The total of nine comparators are laid out in a U-shaped configuration on $\frac{1}{16}''$ PCB with a top surface ground plane. The design value for the transmission line signal paths is 50Ω, enabling the DAC to directly drive 50Ω systems, or the 50Ω input of a fast real time or sampling scope. The option of terminating the board end of the transmission line or leaving it open is available. The latter case provides a full-scale swing of 2 volts (40mA into 50Ω) while termination of the line on the PCB halves the output voltage swing by giving an effective 25Ω load, but gives better settling time by reducing reflections on the summing line.

The device input capacitance is small, and 50Ω nominal lines are used with 50Ω terminations. The two MSB devices are fed through 100Ω lines with 100Ω terminations in parallel. Drive from ECL matched to 50Ω by terminating networks optimises the switching speed, although TTL-level (LS or S) is also possible by resetting the V_{ref} inputs rail to a mid-level point.

On the output current summing line, the typical output capacitance per device is 2pF. The line is fed from both sides, so an unloaded line impedance of 110Ω is predicted for the 50Ω loaded condition. All input lines are made of equal lengths, although some advantage may be gained by equalising the input to output delays; in either case, the MSB should be located furthest from the output connector and as close as possible to the end termination of the line.

Testing the DAC

Each comparator is configured as in Fig. 23 and the potentiometers have to be 'set up' to provide eight-bit accuracy. There are two ways to do this: either DC, using a DVM and setting each current independently of the others or dynamically, driving the inputs with a digital code. The dynamic method provides 'hands-on' practical feel for the DAC operation at high speed, and is recommended if a fast real time scope is available. A simple drive circuit uses two ECL10k Hexadecimal counters (MC10136s) in synchronous count mode, overflowing at the 256 count. For the eight-bit converter, this gives a

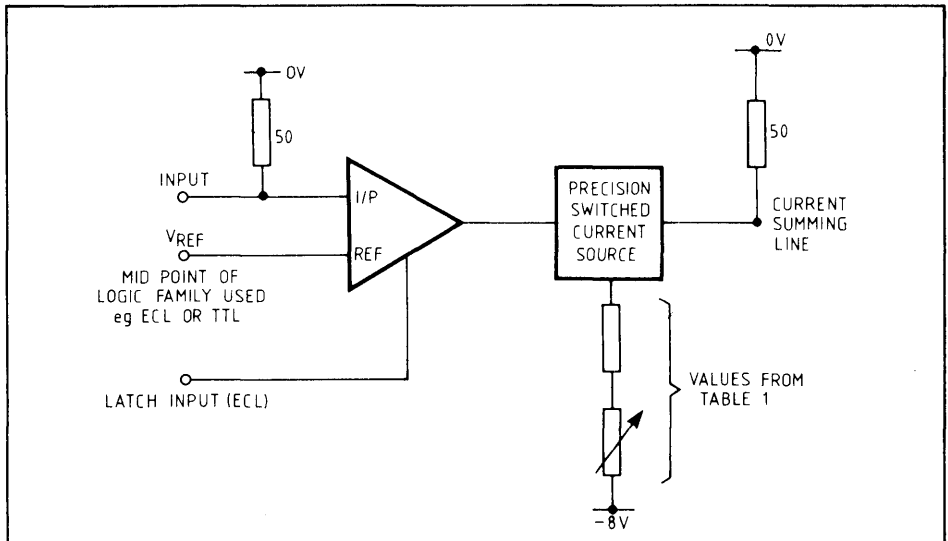

Fig. 23 Comparator configuration

full-scale ramp output, which is easily trimmed for linearity. The system diagram is shown in Fig. 24. Nominal MSB is 20mA, bit 7 is 10mA and so on down. A small overall scaling error can be trimmed out using the —8 volt rail. Independent setting of the current sources instead of the conventional R-2R ladder improves speed performance and prevents interaction between sources.

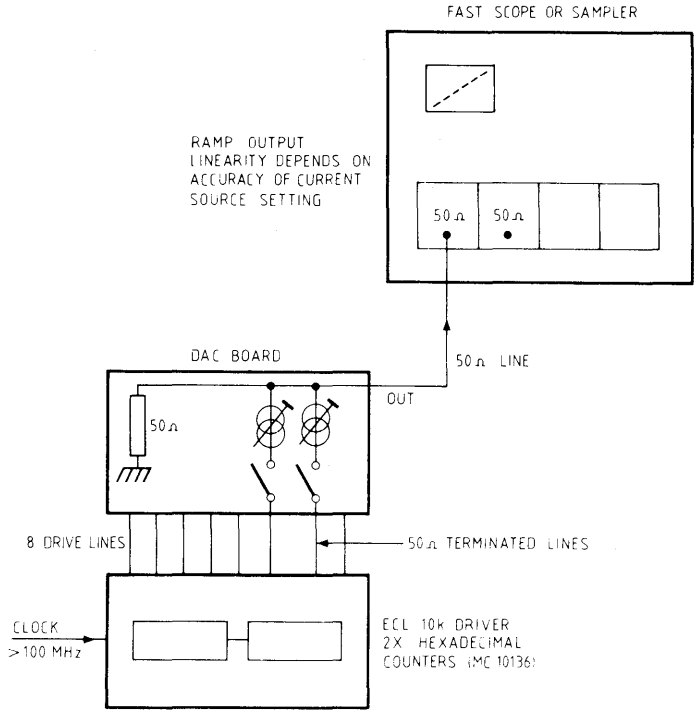

Fig. 24 Setting up the DAC

Fig. 25 shows the full-scale ramp maintaining linearity at more than 50MHz input to the LSB. The full-scale transition (Fig. 26) at the end of the ramp, takes less than 15ns, dominated of course by the MSB transition, shown clocked at about 14MHz in Fig. 27.

The limiting factor in the DAC testing is the ECL10k drivers; output glitches are seen at the MSB transition (0111 1111 to 1000 0000) and at the lower counter full transition (0000 1111 to 0001 0000); these are attributed to timing errors caused by internal 'counter full' to '$\overline{\text{carry out}}$' delay. The manufacturer's figures put this at 5ns, although the glitches seen are shorter, about 3ns overall. The minimum clock period accepted by the counters is 9ns so the DAC LSB state changes occur at this interval, comparable to the I_{out} settling time of the SP9750 (typically 10ns to 0.2%) indicating a maximum data rate of more than 50MHz.

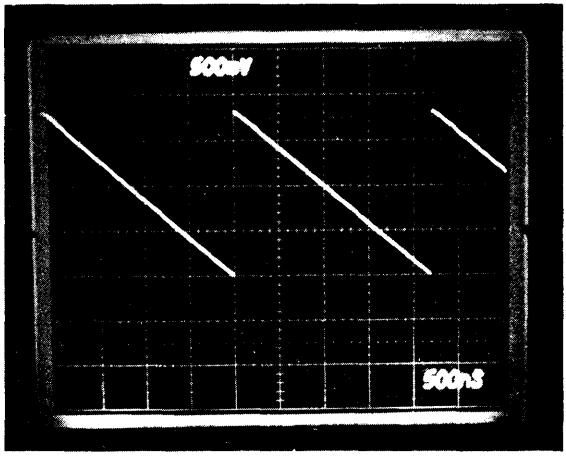

Fig. 25

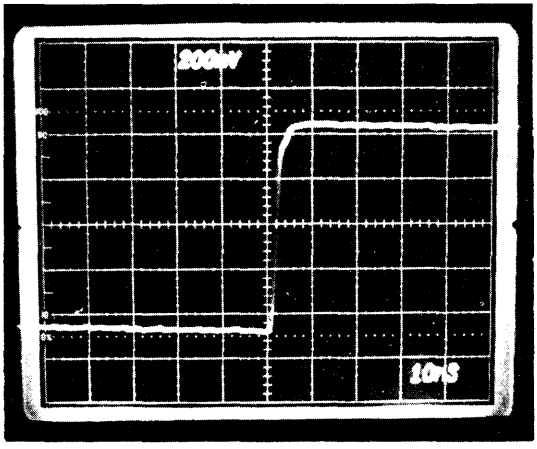

Fig. 26

5. The SP9685 Comparator

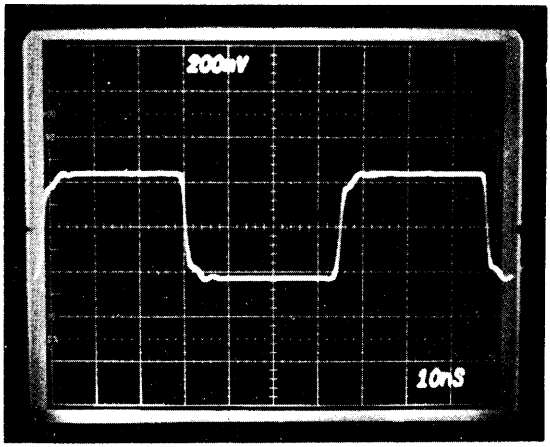

Fig. 27

The SP9685 comparator

GENERAL DESCRIPTION

The SP9685 is a high speed latched comparator, the circuit diagram for which is shown in Fig. 28. The unlatched gain is approximately 50dB at frequencies up to over 200MHz. The main differences between the SP9685 and the SP9750 are as follows:–

1. The SP9685 is a simple comparator and does not include the gates and precision current sources of the SP9750.
2. The unlatched gain of the SP9685 is greater than that of the SP9750.
3. The latch enable control of the SP9685 has the opposite phase of operation to that of the SP9750 latch control.
4. Two gain stages follow the latch of the SP9685 whereas only one is used on the SP9750.
5. Q and $\bar{Q}$ outputs are provided on the SP9685.

Short pulse detector

This simple circuit for the SP9685 has applications in nucleonics and high energy physics. In its simplest form, the circuit is shown in Fig. 29.

A positive going pulse of any width, down to the minimum defined by the propagation delay plus the setup time, and of any height between the maximum common mode signal and the minimum overdrive that will reliably switch the comparator can be quickly detected and will cause the circuit to

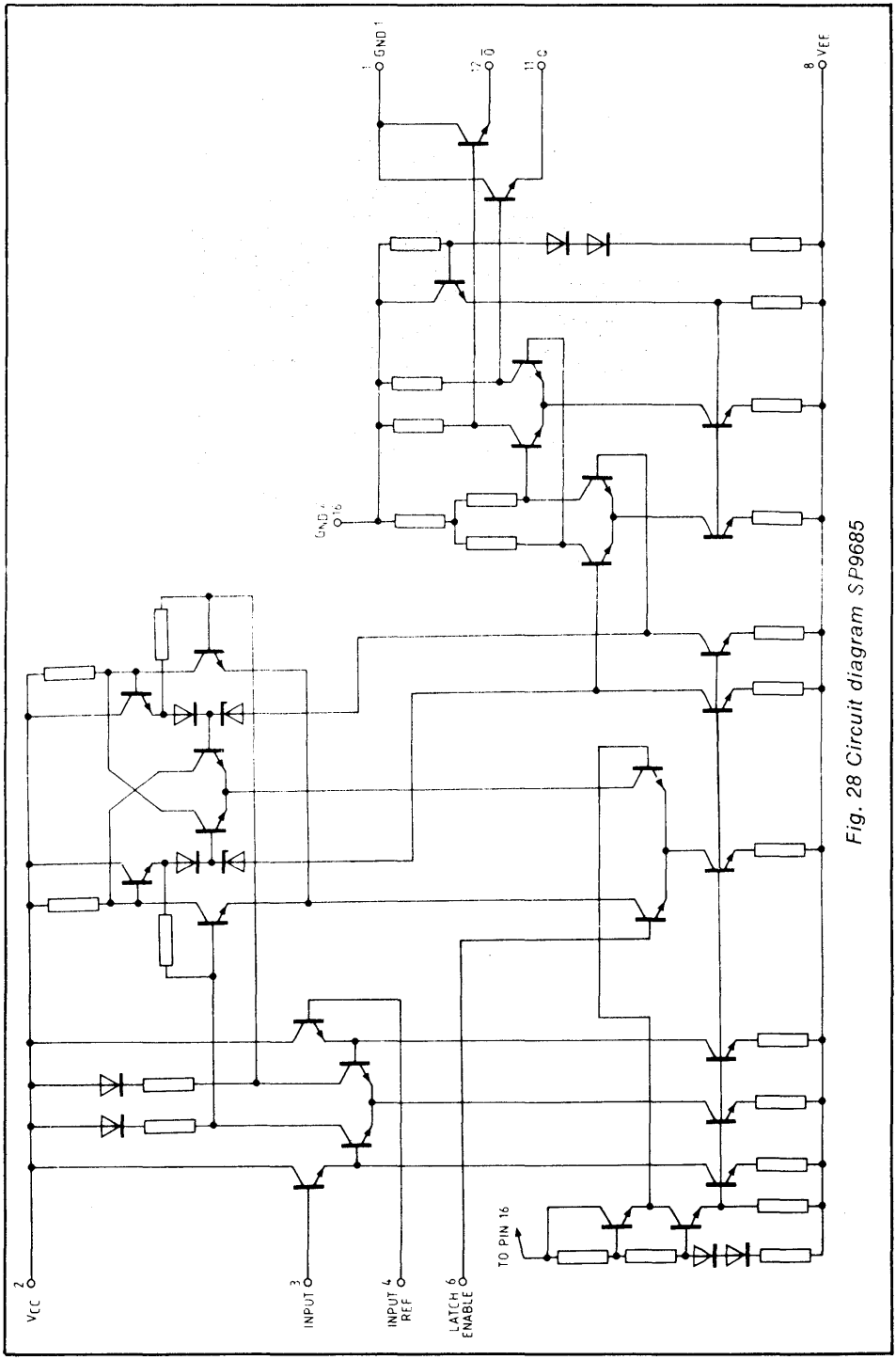

Fig. 28 Circuit diagram SP9685

latch, ignoring further inputs. Practical minimum values are a 3ns pulse width and a 10mV amplitude for reliable latching. The input biasing should be set for a mid input range threshold. Alternative forms of the same basic circuit could be used to detect negative going pulses, by feeding Q back to the latch, or detect pulses greater than a preset height, by shifting the threshold bias point.

Resetting the simple circuit can only be achieved by removing the power supplies. It is possible to produce an external resettable latch using ECLIII which will not degrade the performance if powering down is not an acceptable method.

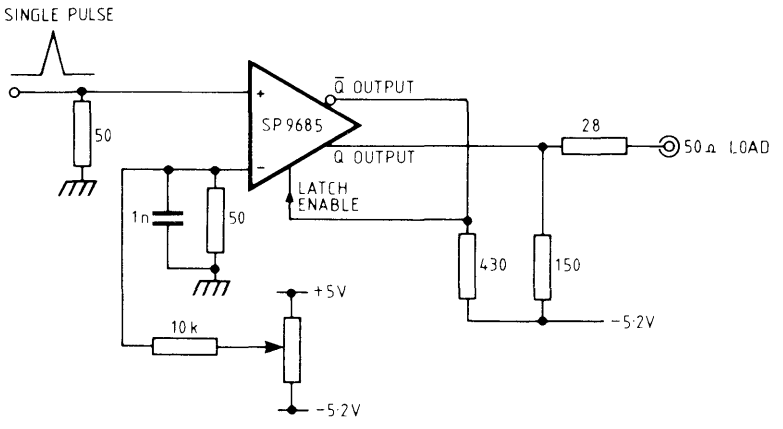

Fig. 29 Short pulse detector

An ECL two-phase clock oscillator

This simple oscillator circuit is capable of relatively high stability and wide frequency range (up to 200MHz). The maximum frequency limit is determined by the device propagation delay (typically 2ns) and the external strays. At low frequencies (below 5MHz) operation is possible, but high frequency instability on the clock edges may be seen. In practice, this is unlikely to be a restriction on the use of the device. An empirical relationship between R and C values and frequency is shown in Table 3. In the circuit shown (Fig. 30) output matching networks are included so that the device can drive 50ohm lines terminated to ground. Where higher impedance lines or short runs are used the output networks may be omitted. However, because the device edge speeds are comparable with ECLIII, good ECL practice in line matching and termination, preferably with a ground plane structure, should be employed as described in Section 3. The input bias conditions are determined by the output potentiometer R_1:R_2. It can be shown that a ratio of 3.6:1 will give a minimum of HF instability when operating at low frequency.

C_1 pf	$F_{osc}(R_3 = 1K\Omega)$MHz	$F_{osc}(R_3 = 330\Omega)$MHz
0	161	190
2.2	64	160
2.7	59	156
3.3	54	152
3.9	46	140
4.7	42	132
5.6	38	120
6.8	33	103
8.2	30	88
10	28	77

Table 3

One side of the capacitor C_1 is grounded, and all or part of the effective capacitance can be made voltage variable, producing a high frequency voltage controlled oscillator with direct ECL drive. Spectral analysis indicates that the noise sidebands from this type of oscillator are 40dB down at 50kHz away from the carrier.

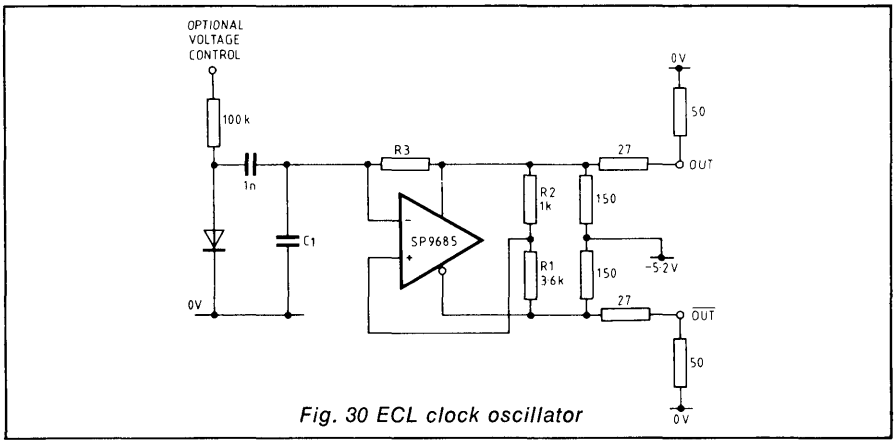

Fig. 30 ECL clock oscillator

A HIGH SPEED WINDOW DETECTOR

The SP9685 can be used to detect whether an input is within a specified voltage range. The basic circuit is well known and is shown in Fig. 31 in a form to give ECL levels. The output drives a 50Ω load to ground or, without the 27Ω series resistor, further ECL stages.

Fig. 32 illustrates the operation of the circuit which has been set up to detect a window of ±20mV about 0 volts. As the input voltage crosses zero the output changes from high to low and back again in a time mainly determined by the ECL rise and fall times. This circuit is thus detecting the crossing of the 40mV window by a signal slewing at 50V/μ sec.

Applications of the high speed window detector are in fast tracking A-D converters and high speed zero crossing detectors. The operational limit is the device propagation delay (typically 2ns) which defines the minimum width of the threshold crossing pulse.

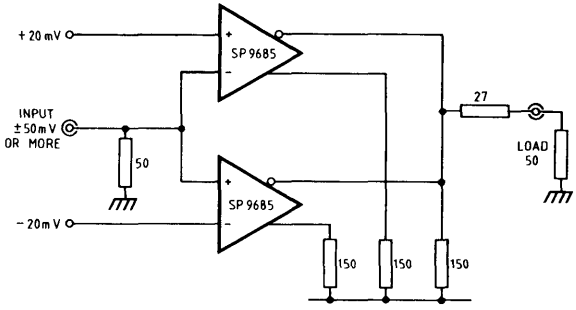

Fig. 31 High speed window detector

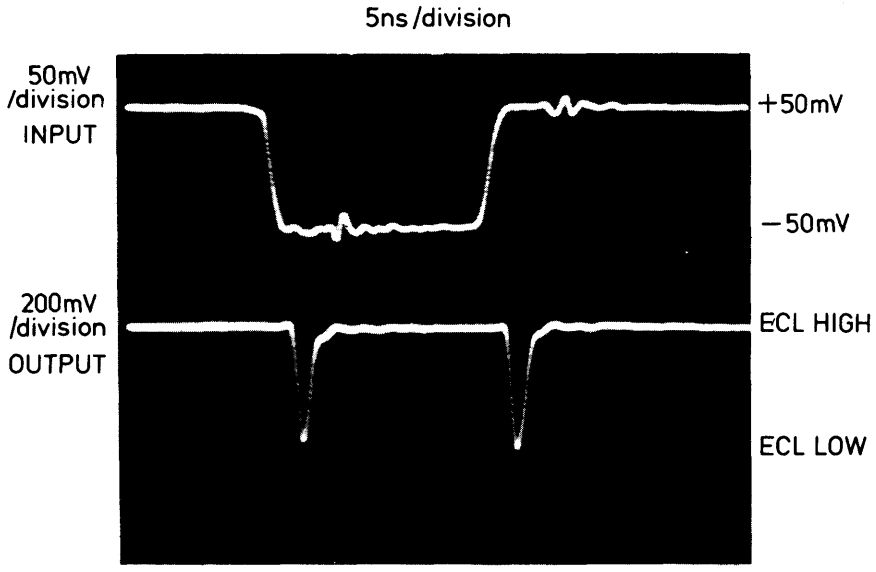

Fig. 32 Performance of high speed window detector

6. U.L.A. For Subnanosecond System Design

Uncommitted Logic Arrays for Subnanosecond System Design

In high speed computer systems the overall gate delay within a complete system is made up of two constituent parts, the intrinsic gate delay and the interconnection delay. It has been usual to try to equalise these constituents and in consequence in systems using industry standard ECL 10K integrated circuits and multi-layer printed circuit board technology, the total 'system' gate delay is typically four nsecs; made up of two nsecs due to the gate itself and two nsecs due to the interconnections (Ref. 1). When the higher performance ECL 100K range was introduced, offering 700 psec logic at the same level of integration, the gain in overall system performance without a radical change in interconnection technology was small. This trend is likely to continue and the application areas for ultra high speed logic will be severely limited unless improvements in gate performance are accompanied by a significant increase in the available level of integration. Improvements to the system architecture will also be necessary to maximise the number of serial logic operations contained on a single integrated circuit chip.

As a result of increasing levels of integration standard product families are becoming less easy to identify. This problem has been overcome in the computer industry by the development of the uncommitted logic array (ULA) (Refs.2,3,4). These are fixed arrays of standard components and gates contained on a silicon chip and customisation is achieved by changing only the metal interconnection patterns. In those areas where the system architecture can be partitioned appropriately this approach has many attractions. Inevitably, partitioning problems due to logic and pin limitations arise, and this generates a requirement for 'infill' logic. There are occasions where this 'infill' could result either in the very low utilisation of the ULA, or a return to the slower ECL parts. Both of these approaches can result in a significant loss in performance.

To overcome this problem a family of ultra high speed devices has been designed which enables all parts of a high performance digital system to be integrated in state-of-the-art technology without compromise. The family, which is based on two small scale (SSI) and two medium scale (MSI) parts developed on the high performance variant of Plessey Process III (Ref.5), offers gate propagation delays of less than 500 picoseconds together with flip-flop clock rates in excess of 500 MHz. It is possible by using these components to construct large digital systems in which the total system gate delay is less than one nanosecond.

SSI Devices

The high speed variant of Process III uses a two micron epitaxial layer and ion implantation for the base and emiter stages. The resulting process offers a peak transistor F_T of 5.5 GHz compared with 2.5 GHz for devices on the standard process at the same current level.

This capability offers two possibilities: higher performance at the same power levels as existing devices, or the same performance for reduced power dissipation. The two SSI devices described below reflect these options, being high performance and low power versions of existing standard ECL products.

1. Dual High Speed Gate

This dual four-input OR/NOR gate offers a packaged delay (typical) of 550 picoseconds. This delay includes some 180 picoseconds contributed by the standard 16-lead ceramic dual-in-line package; the on-chip delay is therefore of the order of 350-400 picoseconds.

2. Dual High Speed Flip-Flop

There are two variants of this circuit, both of which are dual master slave type D flip-flops, with different power requirements. The lower power variant of the new circuit operates at a clock frequency of 400 MHz and the higher power variant at 550 MHz. (All of these values are typical). A contributory factor to the high performance in this case is the use of two layers of metallisation; this also has the added advantage of reducing the overall chip size.

MSI Devices

In an attempt to identify the optimum circuit configuration required for advanced ULA systems, two MSI parts have been designed. The circuits are similar in complexity but, whereas the first uses a simple single level ECL gate structure, the second uses a multi-level structure. Extensive evaluation of both designs has been carried out.

(a) An ECL MSI Subnanosecond ULA

This circuit is based on a single level ECL logic gate and is designed to simplify the customisation procedure. Up to 100 gate functions may be realised

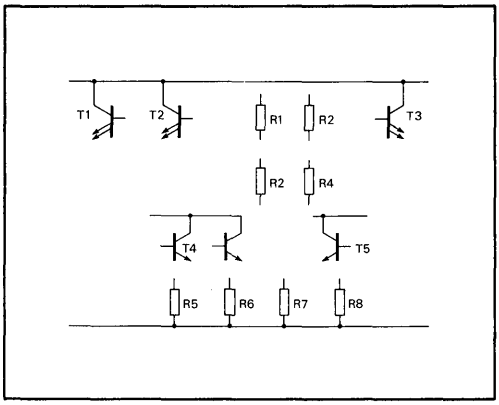

Figure 1 MSI ULA Cell Components

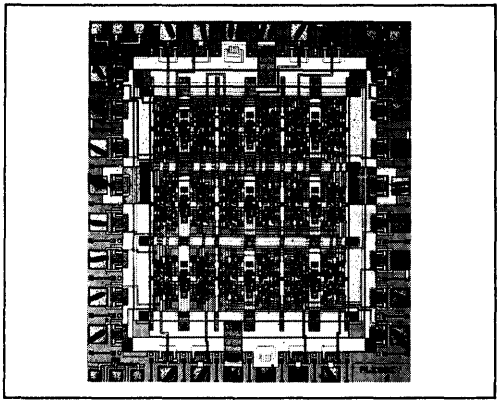

Figure 2 MSI ULA Chip Photograph (2.3 × 2.6mm)

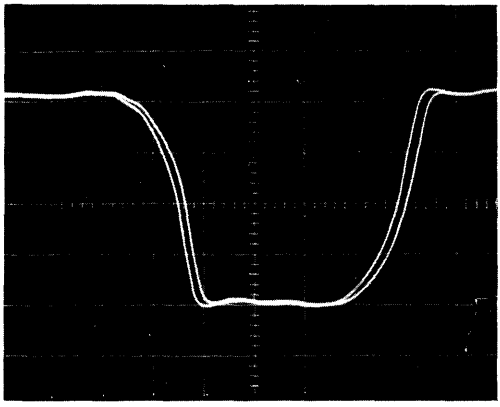

Figure 3 Performance of MSI ULA (2 nsec per division)

using this circuit. The 36 cells (*Figure 1*) are arranged in blocks of four around a central reference supply; the cell layout and component values have been optimised so that emitter and collector dot functions (giving wired OR/AND) are realised with the minimum performance degration. Inputs and outputs to the array are through 28 bonding pads, each of which has associated with it a buffer transistor capable of driving a 50 ohm line at ECL 10K logic levels. Customisation of the array is on two layers of metallisation, and software has been developed to assist in the layout of the circuit (*Figure 2*). Gate delays have been measured at 500 picoseconds (*Figure 3*) for an internal gate, to which 80 picoseconds are added for a typical emitter dot function and 200 picoseconds for a typical collector dot function. Flip-flop clock rates in excess of 400 MHz have been measured.

Six variants of this circuit have been designed and particular attention has been paid to worst case configurations. For instance one of these six was a Dual Parity Generator/Checker requiring the use of an array of non-equivalence gates which is not easily realised in a single-level, ECL logic gate structure. Extensive emitter and collector dotting is required, as illustrated by *Figure 4*. Despite the inefficient realisation of this function (there are in fact ten serial gates in the path from data to output) the propagation delay is only 3.5 nsecs when packaged in a standard 24-lead dual-in-line package.

(b) An ECL MSI Master Chip

This is a high speed component array for implementing multi-level stacked ECL functions. The chip (*Figure 2*) is subdivided into eight major cells, each of which can be customised to realise a master-slave D-type flip-flop and has 32 external

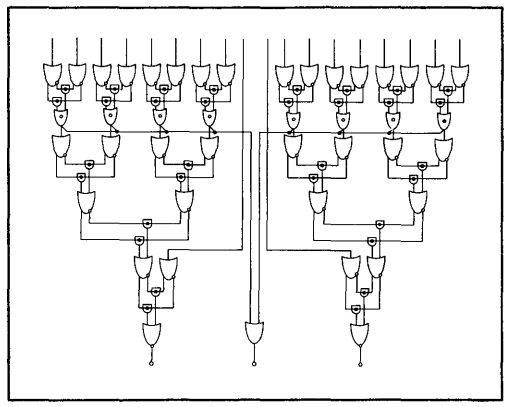

Figure 4 Realisation of Dual Parity Circuit

connections. A major cell is divided into two minor cells (*Figure 6*), each of which has the capability of (typically) a two-input exclusive OR gate or a triple three-input OR gate. Emitter dotting and collector dotting may also be used to increase the logic capability of the circuit. Gate delays on this circuit are of the order of 550 picoseconds and maximum flip-flop clock rates in excess of 500 MHz. Five variants of this circuit have been completed; its application is primarily in those areas where the packing density and power dissipation of circuits can be optimised by use of the multi-level logic capability. One such example is illustrated by *Figure 7*. This variant is a dual quad master slave flip-flop with asynchronous set and reset which is to be used to provide the output latches for a fast A-D converter chip set. Whilst power dissipation has been reduced as far as possible (in order that a standard 24-lead dual-in-line package may be used), typical operating speeds are still expected to be in the region of 400 MHz.

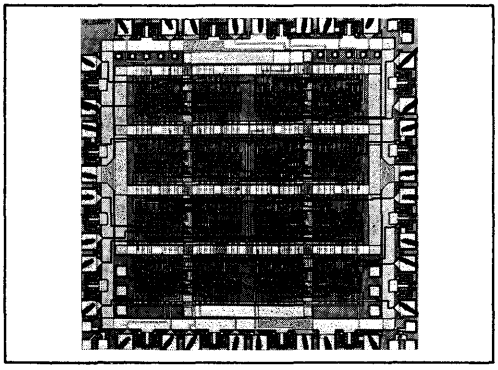

Figure 5 MSI Master Chip Photograph

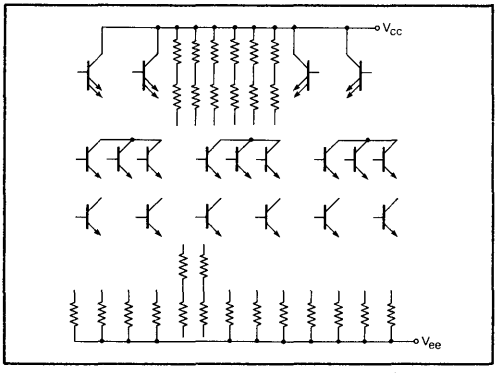

Figure 6 MSI Master Chip Minor Cell Components

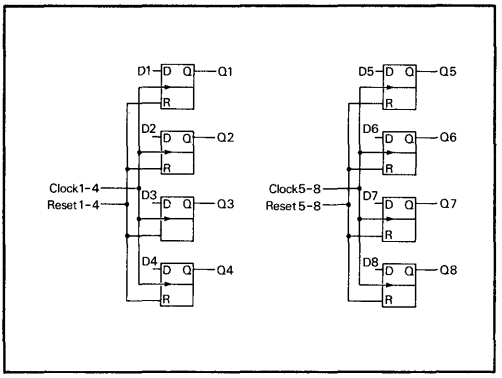

Figure 7 Octal D-Type Variant of MSI Master Chip

	16 bit operand		64 bit operand	
	IC Count	Time nS	IC Count	Time nS
ULA multiplier & ECL 10K	41	110		
ULA multiplier & ECL 100K	32	88	71	284
ULA multiplier & high speed ULA	26	80	56	250

Figure 8 Fast Multiplier Performance Comparison

L.S.I. Devices

The majority of second generation ULAs now being introduced use multi-level ECL logic structures as described for the ECL MSI Master Chip above. Comprehensive computer aided designs have been developed to enable the layout of these circuits to be designed quickly and efficiently. This approach has consequences concerning the achievable performance and packing density. The use of CAD techniques has generally resulted in the introduction of standard metallisation cells which are used to design an area of the circuit to perform a particular logic function. These cells (necessary to reduce a complex I.C. design to a simple topological problem) are superimposed on the array and interconnected automatically. As with all CAD and standard cell-based systems, this results in an increase in the redundancy of the on-chip logic (customisation efficiencies of 70% are typical) and substantial

increase in the typical interconnection length (unless this can be interactively avoided). For logic operating at less than 500 psecs, the performance penalty caused by the compromised cell layout and the increased interconnection capacitance (both caused by the automatic layout methodology) may eventually prove prohibitive. The development of highly optimised single-level structures, working off reduced voltage supplies to minimise power dissipation, may become the preferred approach due to the inherent layosut simplicity.

As a result of the development work above, a larger version of the MSI subnanosecond ULA has been designed. This circuit, which contains 144 of the single-level cells contained in the smaller circuit, offers a logic capability of up to 400 gates. Two power options are offered. The first, consistent with the smaller circuit, dissipates three wats and offers a gate propagation delay of 500 picoseconds. The second, which is metal compatible with the first, will offer a gate delay of 1.3 nsecs for a power dissipation of 500 mW. Both chips measure 3.5 × 4.1mm and have 64 pin connections.

System Implications

Work carried out on fast multipliers has shown that significant advantages are to be gained both in terms of package count and performance using the family as described. A 16 × 16 bit multiplier using the 36-cell array uses a chip count of 26 and achieves a multiplication time of 80 nsecs. By use of the larger array it should be possible to construct a 64 × 64-bit multiplier which will achieve a 128-bit product in 150 nsecs using 56 devices.

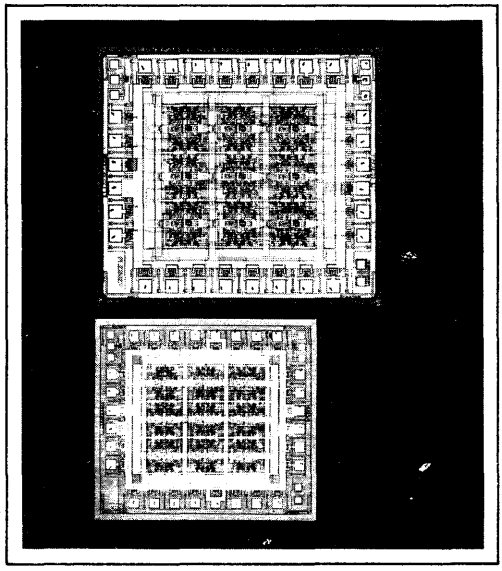

Figure 9 Scaled and Full-size ULA Chips

Future Developments

As a step towards very high speed integration (V.H.S.I.), a 25% linear dimension shrink has been applied to the 36-cell ULA. The scaled circuit uses three micron minimum geometries and has been processed using conventional photolithographic techniques. In the shrunk ULA (*Figure 9*), not only is the local gate delay reduced, but the parasitic delays have also been halved when compared with the full-size version (*Figure 10*). (The parasitic delays are those caused by the capacitance introduced by the on-chip interconnections and by use of the 'wire and' and 'wire or' functions). This reduction improves the system performance significantly as is illustrated by

Complexity	100 gates
Internal gate delay	375 psecs
Wire 'OR' delay	40 psecs
Wire 'AND' delay	100 psecs
Max. flip-flop clock rate	950 MHz
Power dissipation	800 mW
Pin connections	28
Chip dimension	1.8 x 2.0 mm

Figure 10 Performance of Scaled ULA

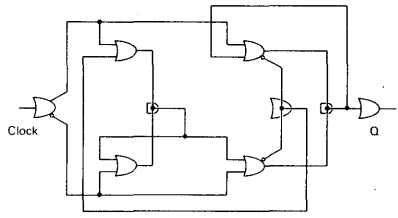

Figure 11 2 Counter Circuit

the counter circuit of *Figure 11*. Because of the simple cell structure this circuit has been realised using a combination of basic gates, 'wire or' and 'wire and' functions. The perfornace of the counter has increased from less than 500 MHz to over 950 MHz (*Figure 12*) and the on-chip gate delays are now less than 400 picoseconds.

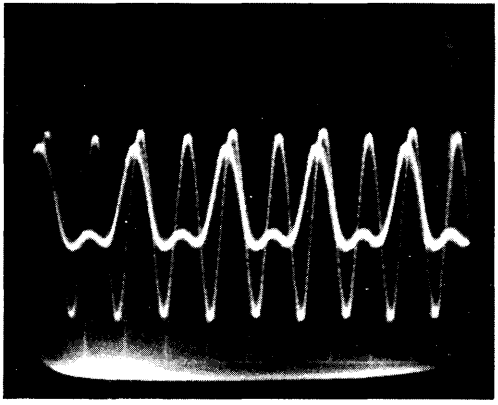

Figure 12 Counter Performance (1 nsec per division)

Conclusions

A range of devices has been developed which enables subnanosecond performance to be maintained across the whole of a digital system. Developments are now under way which should allow three micron geometries and less to be used in future designs. The impact of this, together with fundamental improvements in the basic transistor structure, should allow local gate delays of 200 picoseconds and system gate delays of 500 picoseconds to be achieved within the next few years.

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7. SP9000 Data

PLESSEY
Semiconductors

SP9000 SERIES
DATA CONVERSION PRODUCTS

SP 9685
ULTRA FAST COMPARATOR

The SP 9685 is an ultra-fast comparator, and the SP 9687 is an ultra-fast dual comparator, both manufactured with a high performance bipolar process which makes possible very short propagation delays 2.2 nS typ ./ 2.7 nS typ. respectively. The circuits have differential inputs and complementary outputs fully compatible with ECL logic levels. The output currents capability are adequate for driving 50 ohm terminated transmission lines. The high resolution available makes the devices ideally suited to analogue-to-digital signal processing applications.

With the SP 9685 a latch function is provided to allow the comparator to be used in a sample-hold mode. When the latch enable input is ECL high, the comparator functions normally. When the latch enable is driven low, the outputs are forced to an unambiguous ECL logic state dependent on the input conditions at the time of the latch input transition. If the latch function is not used the latch enable may be connected to ground.

With the SP 9687 a latch function is provided to allow the comparator to operate in the follow-hold or sample-hold mode. The latch function inputs are intended to be driven from the complementary outputs of a standard ECL gate. If $\overline{LE}$ is high, and $\overline{LE}$ is low, the comparator function is in operation. When $\overline{LE}$ is driven low and $\overline{LE}$ high, the outputs are locked into the logical states at the time of arrival of the latch signal. If the latch function is not used, $\overline{LE}$ Must be connected to ground.

Both devices are compatible with the AM 685/AM 687 respectively but operate from conventional +5V and–5.2V rails.

FEATURES

- Propagation Delay 2.2 ns typ/2.7 ns typ respectively.
- Latch Set-up Time 1 ns max./0.5 ns typ
- Complementary ECL Outputs
- 50 Ω Line Driving Capability
- Excellent Common Mode Rejection
- Pin Compatible with AM 685/687 but faster

QUICK REFERENCE DATA

- Supply voltages +5V, –5.2V
- Operating tempurature range $-30^{o}C$ to $+85^{o}C$

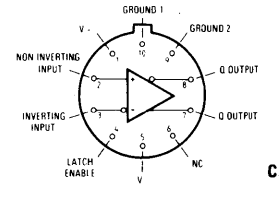
ABSOLUTE MAXIMUM RATINGS

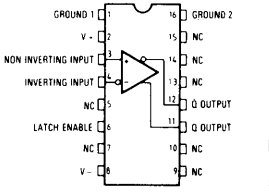
Positive supply voltage	6V
Negative supply voltage	—6V
Output current	30mA
Input voltage	± 5V
Differential input voltage	± 5V
Power dissipation	500mW
Storage	—55° to 150°C
Lead temperature (soldering 60 sec)	300°

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{AMB} = 25°C
V_{CC} = +5.0V ± .25V
V_{EE} = –5.2V ± .25V
R_L = 50 Ω

SP 9687
ULTRA FAST DUAL COMPARATOR





On metal package, pin 5 is connected to case. On DIP pin 8 is connected to case

Fig. 1 Pin connections

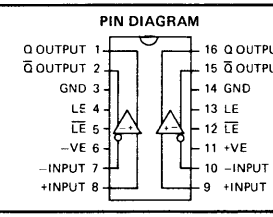
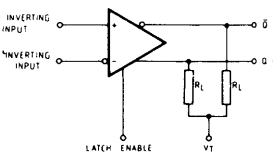


Fig. 1A



The outputs are open emitters, therefore external pulldown resistors are required. These resistors may be in the range of 50–200Ω connected to –2.0V or 200–2000Ω connected to –5.2V

Fig. 2 Functional diagram

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Input offset voltage	Both	−5		+5	mV	Rs 100 ohms
Input bias current	Both		10	20	uA	
Input offset current	Both			5	uA	
Supply Currents Icc	SP 9685		19	23	mA	
IEE			23	34	mA	
	SP 9687		30		mA	
			54		mA	
Total Power Dissipation	SP 9685		210	300	mW	
	SP 9687		430		mW	Nominal Conditions
Min. Latch Set-up Time	SP 9685		0.5	1	ns	
	SP 9687		0.5		ns	
Input to Q Output Delay	SP 9685		2.2	3	ns	
	SP 9687		2.7	4	ns	
Input to $\overline{Q}$ Output Delay	SP 9685		2.2	3	ns	
	SP 9687		2.7	4	ns	100 mV pulse
Latch to Q delay	SP 9685		2.5	3	ns	10 mV Overdrive
	SP 9687		2.7	4	ns	
Latch to $\overline{Q}$ delay	SP 9685		2.5	3	ns	
	SP 9687		2.7	4	ns	
Min. latch pulse width	Both		2	3	ns	
Min. hold time	Both			1	ns	
Common Mode Range	Both	−2.5		+2.5	V	
Input Capacitance	Both		3		pF	
Input Resistance	Both	60			K ohms	
Output Logic Levels						
Output High	Both	−.96		−.81	V	At Nominal Supply
Output Low	Both	−1.85		−1.65	V	Voltages.
Common Mode Rejection Ratio	Both	80			dB	See Fig. 4
Supply Voltage Rejection Ratio	Both	60			dB	

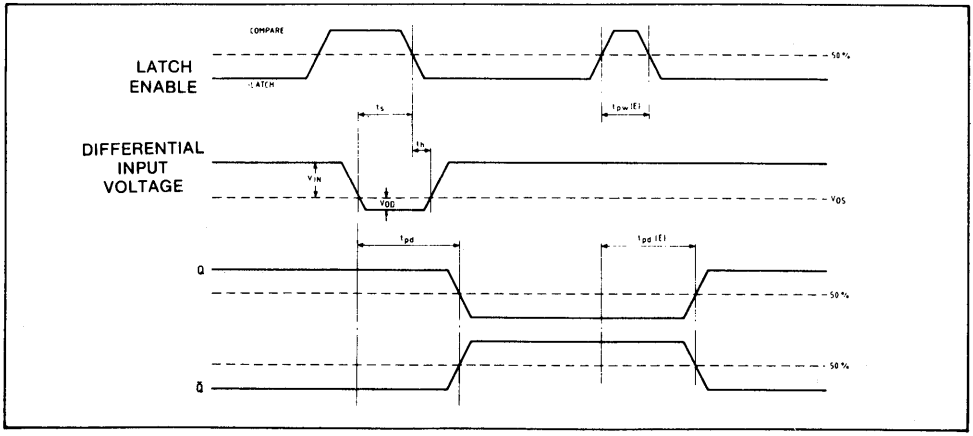


Fig. 3 Timing diagram

OPERATING NOTES

Timing diagram

The timing diagram, Figure 3, shows in graphic form a sequence of events in the SP9685. It should not be interpreted as 'typical' in that several parameters are multi-valued and the worst case conditions are illustrated. The top line shows two latch enable pulses, high for 'compare', and low for latch. The first pulse is used to highlight the 'compare' function, where part of the input action takes place in the compare mode. The leading edge of the input signal, here illustrated as a large amplitude, small overdrive pulse, switches the comparator over after a time tpd. Output Q and $\overline{Q}$ transitions are essentially similar in timing. The input signal must occur at a time t_s before the latch falling edge, and must be maintained for a time t_h after the latch falling edge, in order to be acquired. After t_h, the output ignores the input status until the latch is again strobed. A minimum latch pulse with $t_{pw(E)}$ is required for the strobe operation, and the output transitions occur after a time $t_{pd(E)}$.

Definition of terms

Vos Input offset voltage – The potential difference required between the input terminals to obtain zero output potential difference.

Ios Input offset current – The difference between

the currents into the inputs when there is zero potential difference between the outputs.

I_B Input bias currents - The average of the two input currents. I_B is a chip design trade-off parameter; externally, it is desirable to have I_B as low as possible, while internally, circuit performance requirements demand higher I_B.

R_{IN} Input resistance - The resistance looking into either input with the other grounded.

C_{IN} Input capacitance - The capacitance looking into either input pin with the other grounded.

Switching terms (refer to Fig. 3)

t_{pd+} Input to output high delay – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output LOW to HIGH transition.

t_{pd-} Input to output low delay – The propagation delay measured from the time the input signal crosses the input offset voltage to the 50% point of an output HIGH to LOW transition.

$t_{pd+(E)}$ Latch enable to output high delay – The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition.

$t_{pd-(E)}$ Latch enable to output low delay – The propagation delay measured from the 50% point of the latch enable signal LOW to HIGH transistion to the 50% point of an output HIGH to LOW transition.

t_s Minimum set-up time – The minimum time before the negative transition of the latch enable signal that an input signal change must be present in order to be acquired and held at the outputs.

t_h The minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

$t_{pw(E)}$ Minimum latch enable pulse width – The minimum time that the latch enable signal must be HIGH in order to acquire and hold an input signal change.

V_{CM} Input voltage range – The range of input voltages for which the offset and propagation delay specifications are valid.

CMRR Common mode rejection ratio – The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Latched and unlatched gain

The gain of a high speed, high gain comparator is difficult to measure, because of input noise and the possibility of oscillations when in the linear region. For a full ECL output level swing, the unlatched input shift required is approximately 1mV. In the latched mode, the feedback action in effect enhances the gain and the limitation in the noise/oscillation level; under these conditions the usable resolution is 100µV, although this is only achieved by careful circuit design and layout.

Interconnection techniques

High speed components in general need special precautions in circuit board design to achieve optimum system performance. The SP 9685/SP9687, with around 50 dB gain at 200MHz, should be provided with a ground plane having a low inductance ground return. All lead lengths should be as short as possible, and RF decoupling capacitors should be mounted close to the supply pins. In most applications, it will be found to be necessary to solder the device directly into the circuit board. The output lines should be designed as microstrip transmission lines backed by the ground plane with a characteristic impedance between 50Ω and 150Ω. Terminations to −2V, or Thevenin equivalents, should be used.

Measurement of propagation and latch delays

A simple test circuit is shown in Figure 4. The operating sequence is:

1. Power up and apply input and latch signals. Input 100mV square wave, latch ECL levels. Connect monitoring scope(s).
2. Select 'offset null'.
3. Adjust offset null potentiometer for an output which switches evenly between states on clock pulses.
4. Measure input/output and latch/output delays at 5mV offset, 10mV offset and 25mV offset.

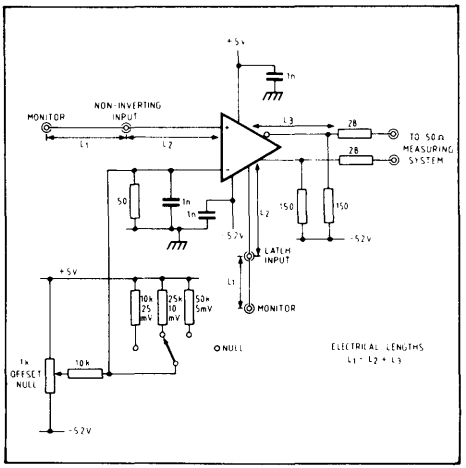


Fig. 4 SP9685/9687 test circuit

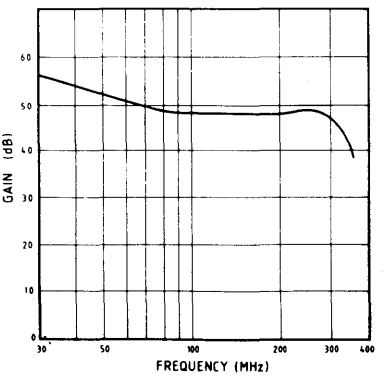


Fig. 5 Open loop gain as a function of frequency

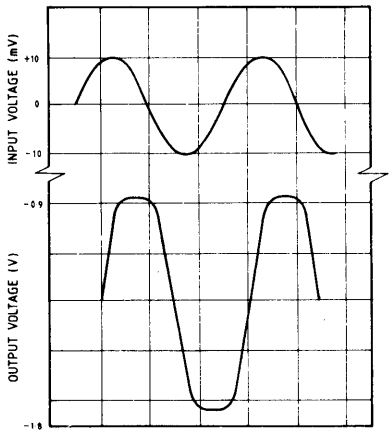


Fig. 6 Response to a 100MHz sine wave

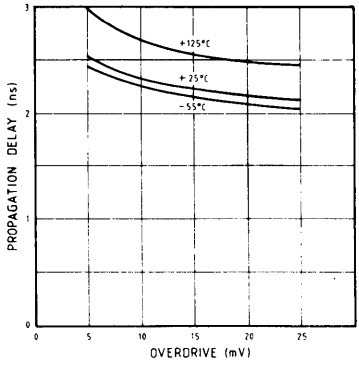


Fig. 7 Propagation delay, latch to output as a function of overdrive

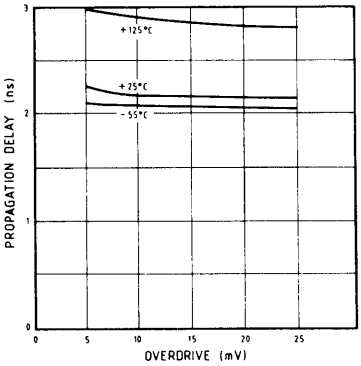


Fig. 8 Propagation delay, input to output as a function overdrive

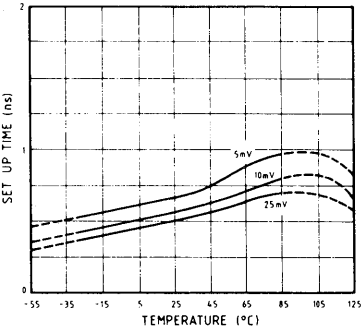


Fig. 9 Set-up time as a function of temperature

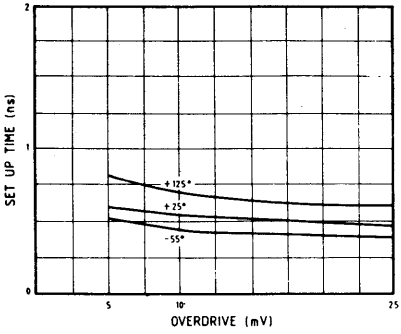


Fig. 10 Set-up time as a function of input overdrive

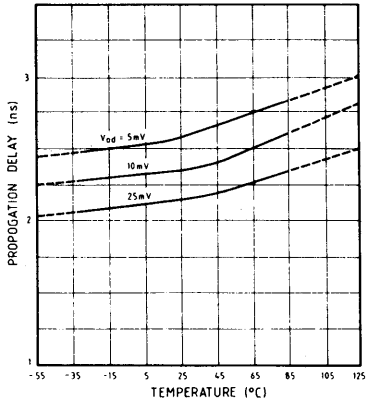


Fig. 11 Propagation delay, input to output as a function of temperature

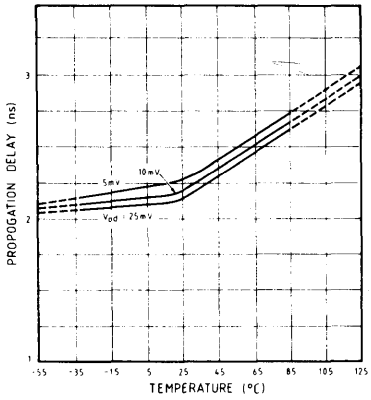


Fig. 12 Propagation delay, latch to output as a function of temperature

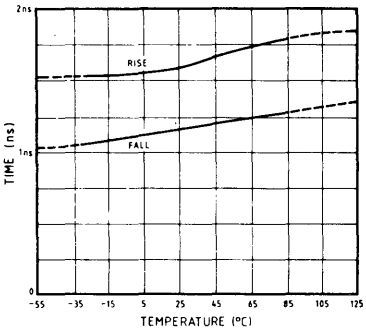


Fig. 13 Output rise and fall times as a function of temperature

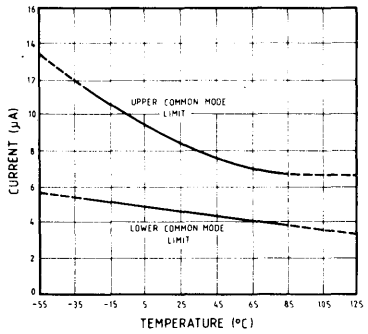


Fig. 14 Input bias currents as a function of temperature

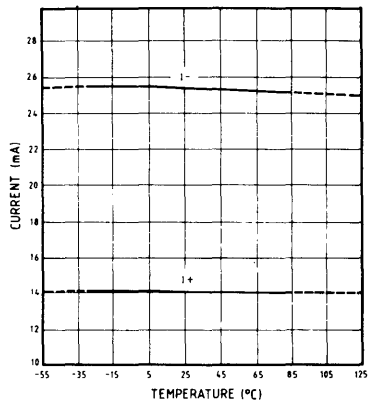


Fig. 15 Supply current as a function of temperature

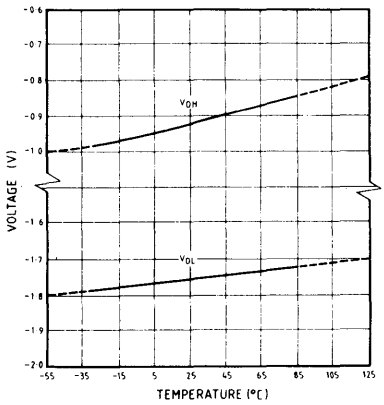


Fig. 16 Output levels as a function of temperature

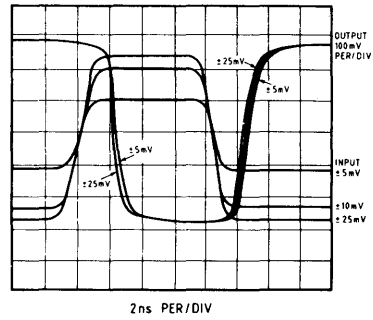


Fig. 17 Response to various input signal levels

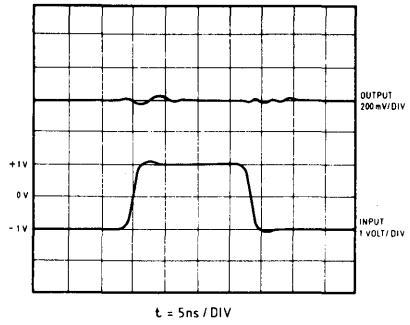


Fig. 18 Common mode pulse response

SP9750

HIGH SPEED COMPARATOR

The SP9750 is a high speed comparator with a latch circuit and other facilities intended for use in the construction of fast A–D converter systems. The speed capability of the device is compatible with conversion rates of up to 100 Mega-samples per second. Input and output logic levels are ECL compatible.

FEATURES

- Latch Set-up Time 2ns Max.
- Max. Input Offset Voltage 5mV
- Propagation Delay 3ns (Typ.)
- ECL Compatible
- Comparator Output Gating
- Wired OR Decoding for 4 Bits
- Current Output Settling to 0.2% in 8ns

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	–5.5V
Reference supply voltage	–8.5V
Reference current output	15 mA
Input voltage	±4V
Differential input voltage	±6V
Power dissipation	500 mW
Operating temperature range	–30°C to +85°C
Storage temperature range	–65°C to +150°C
Lead temperature (soldering 30 sec)	300°C

Logic input voltages to gate and latch V_{EE} to 0

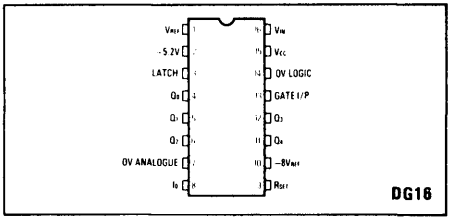


Fig. 1 Pin connections

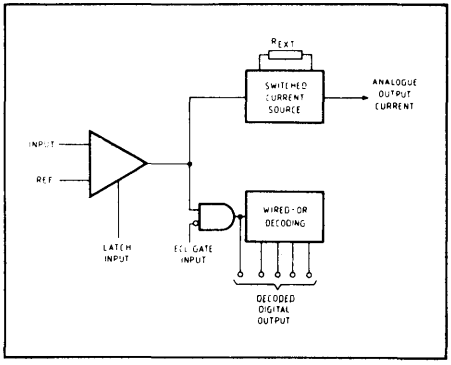


Fig. 2 Block diagram of SP9750

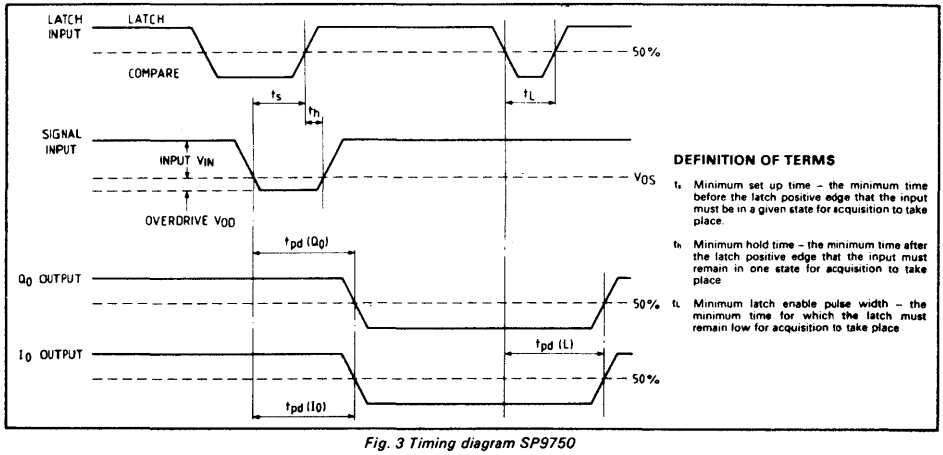


Fig. 3 Timing diagram SP9750

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{AMB} = +25°C
V_{CC} = +5V ±0.25V
V_{EE} = −5.2V ±0.25V
V_{REF} = −8V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input offset voltage	−5		+5	mV	
Input bias current			25	µA	
Input offset current			5	µA	
Supply currents V_{CC}		16	20	mA	
V_{EE}		35	42	mA	
V_{REF}		14	18	mA	
Total power dissipation		390	470	mW	
Analogue O/P current 'on'		5		mA	See operating note 1
Analogue O/P current 'off'			5	µA	+5V on pin 8
Precision current stability		20		ppm/°C	Also depends on R_{EXT}
Min. latch set-up time (t_s)			2	ns	See operating note 2
Input to Q_o O/P delay (tpd (Q_o))		3	4.5	ns	V_{IN} = 100 mV, 25 mV over drive, 50Ω load
Input to I_o delay (tpd (I_o))		3	4.5	ns	on I_o to 0 volts (Note 3)
Delay gate input to Q_{1-4} high		1.5	2.5	ns	See operating note 4
Delay gate input to Q_{1-4} low		1.5	2.5	ns	
Latch to I_o (tpd (LI_o))					
between 50% points		3	4.5	ns	
to 1% settling		4	8	ns	See operating note 5
to 0.2% settling		8	12	ns	
Min. hold time t_h		1		ns	
Min. latch pulse width (t_L)		2		ns	
Common mode range	−2.5V		+2.5V	V	
Diff. mode range			5	V	
Node capacitance I_o		3.5		pf	
Node capacitance analogue input			3	pf	
Input resistance	60			KΩ	
Output logic levels					
Logic '1'	−.98		−0.78	V	V_{CC} = +5V, V_{EE} = −5.2V
Logic '0'	−1.85		−1.6	V	R_L = 220Ω to −2V

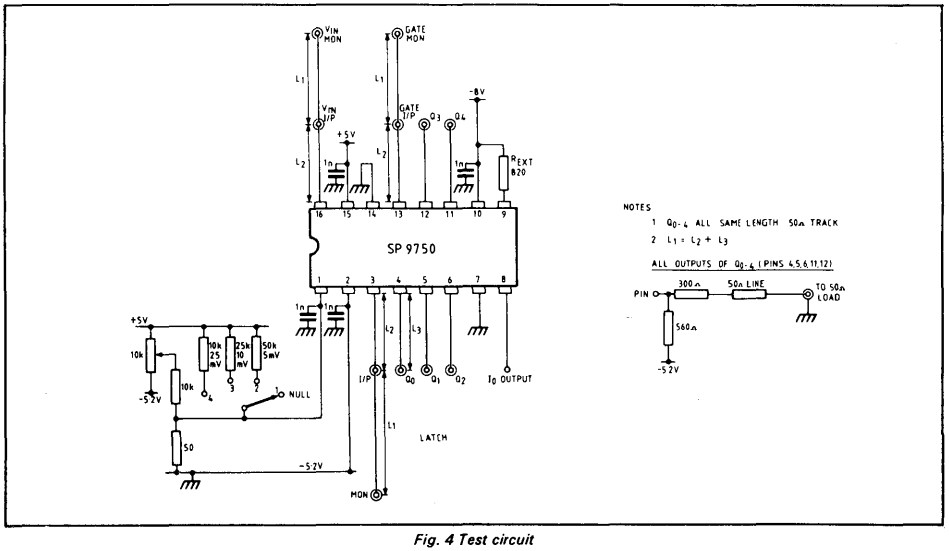


Fig. 4 Test circuit

GENERAL DESCRIPTION

The SP9750 is a fast comparator combined with a latch facility which allows the device to be operated in the sample and hold mode.

When the latch is 'low' the comparator is in the 'follow' mode, and when the latch is driven 'high' the output is locked in the existing state. The latch circuitry will therefore always produce a decision on the input state.

The comparator has a relatively low gain in the follow mode, which assists in achieving an extremely fast response. However, due to the positive feedback action of the latch function, the gain approaches infinity during the latch cycle, thereby ensuring high resolution.

In addition to the basic comparator, the following functions are provided on the chip to optimise the performance of high speed parallel-series-parallel A to D converter systems.

1. An ECL compatible gating function for simplified multi-comparator output logic.
2. Four emitter follower outputs from the gate to provide wired OR decoding for four bits.
3. A precision current source, set by an external resistor.
4. A high speed switch for the precision current to provide a fast and convenient reconstruction of the analogue input. Summing the currents in a multi-level comparator chain provides the D to A conversion directly for the construction of converters of the parallel-series-parallel type.

The philosophy adopted in the SP9750 makes possible the construction of ultra-fast, high accuracy parallel-series-parallel converters by integrating a significant portion of the system function on the same chip as the comparator. The result is not only to reduce considerably the total hardware count but to reduce the propagation delays where they are most critical, and eliminate redundant operations.

OPERATING NOTES

1. The analogue output current (Io) is set by means of an external setting resistor (R_{EXT}) and is equal to the reference voltage on Pin 9 (−8V nominal), divided by 2 x R_{EXT}. The accuracy of this reference voltage must be consistent with the conversion accuracy required. The output (Pin 8) compliance is −0.8V to +5.0 volts for correct operation.
2. This parameter is defined with +100 mV input and −10 mV overdrive, corrected to take account of the comparator offset, i.e. the switching threshold effectively is at OV on the input waveform. The relationship between setup time and overdrive is shown in Fig. 7c. The test circuit diagram, Fig. 4 indicates a method of performing this test.
3. Due to the relatively low gain of the comparator in the unlatched state, propagation measurements are defined with a 25 mV overdrive. The relationship between overdrive and delay is shown in Figs. 7a and 7b.
4. The gate input accepts an ECL drive. The outputs Q_1 to Q_4 are active when the gate input is at an ECL 'low' level, (−1.75V) and are switched by the internal circuitry. A 'high' gate input (− 0.9 V) switches the outputs to 'low', allowing the bussing of multiple devices onto the Q_1 – Q_4 rails.
5. Output settling times are measured at 10 mV overdrive conditions; larger overdrives produce shorter delays.
6. The test arrangement shown in Fig. 4 provides for a simple dynamic test of the SP9750 functions. When the switch is in position 1, the input offset voltage is nulled with the potentiometer, a condition detected by observing the output to be at the mid-point of its range (I_o or Q_o). The latch must be 'low' for this measurement. The offset voltage can be measured with a high impedance instrument. Positions 2, 3 and 4 provide increasing amounts of bias to the reference input corresponding to overdrives of 5mV, 10 mV, and 25 mV. For convenience of operation, the input analogue signal is referred to ground, and the reference input is set above ground, so that an input waveform which is positive going and referred to ground is all that is necessary. It should have an amplitude of (100 mV + overdrive voltage) and should have less than 5% overshoot. The risetime should be about 2 nS. Simple circuit modifications and a negative going signal would provide for inputs of opposite polarity. For accurate timing, the path length L_1 should be equal to $L_2 + L_3$ properly terminated.

Static (DC) measurements can also be performed on the same test arrangement.

APPLICATIONS

Although the SP9750 was aimed at a particular system configuration it is sufficiently flexible to find application in a variety of conversion methods. In an all-parallel A–D converter, the SP9750 is capable of achieving sampling rates of up to 100 Megasamples per second. This technique is usable up to 5-bit accuracy. For higher bit accuracies, techniques such as the parallel-series method are required. Fig. 5 shows the schematic diagram of an A–D converter system capable of giving 8-bit accuracy at sampling rates of up to 30 Mega-samples per second. The SP9750 is used in two 4-bit stages operating in the parallel-series-parallel mode. The analogue current output settling time from the first stage (an effective DAC facility) is dominated by the settling time of the one comparator which has the smallest overdrive. All other comparators have longer to settle, since the preceding sample and hold must be allowed to settle. For an 8-bit system, each comparator in the first 4-bit conversion has a weighting of 1/15 of full scale input. Therefore the settling band of interest for ± ½ L.S.B. is 2.9%. Typically the SP9750 settles to less than this, 1%, in four nanoseconds, illustrating the possibility of converter construction at higher speeds, or higher accuracies.

In order to achieve the optimum performance of this device, care must be taken to ensure that good layout practice is used, consistent with high frequency practice. A ground plane construction should be used and all leads should be designed to be microstrip transmission lines. The device should be soldered directly into the circuit board and the supplies decoupled with RF capacitors as close to each device as possible. In addition, to achieve the shortest possible settling time for the analogue current output, it is essential to keep the stray capacitance on Pin 9 (R_{SET}) to a minimum.

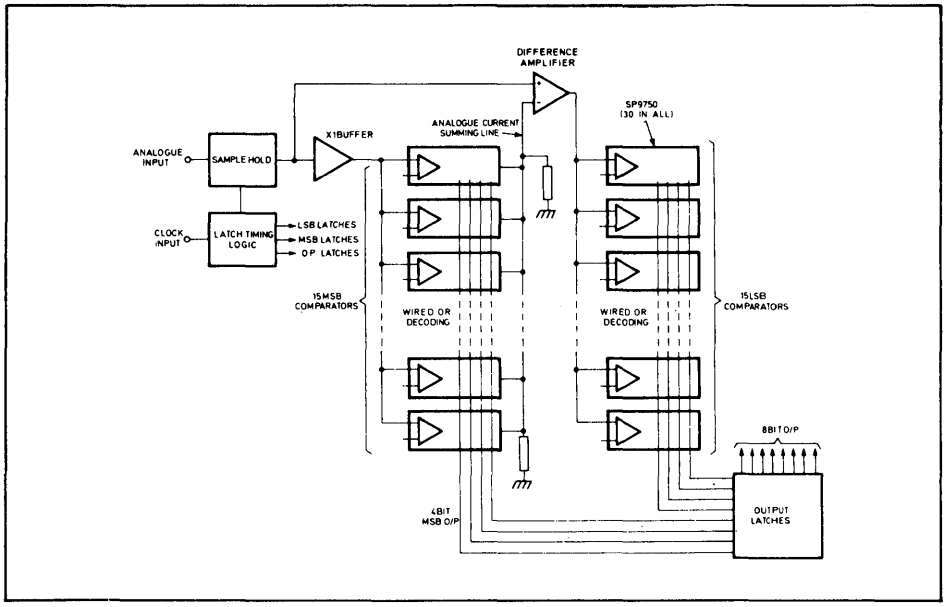


Fig. 5 Block diagram of a 4 x 4 bit parallel-series A/D converter

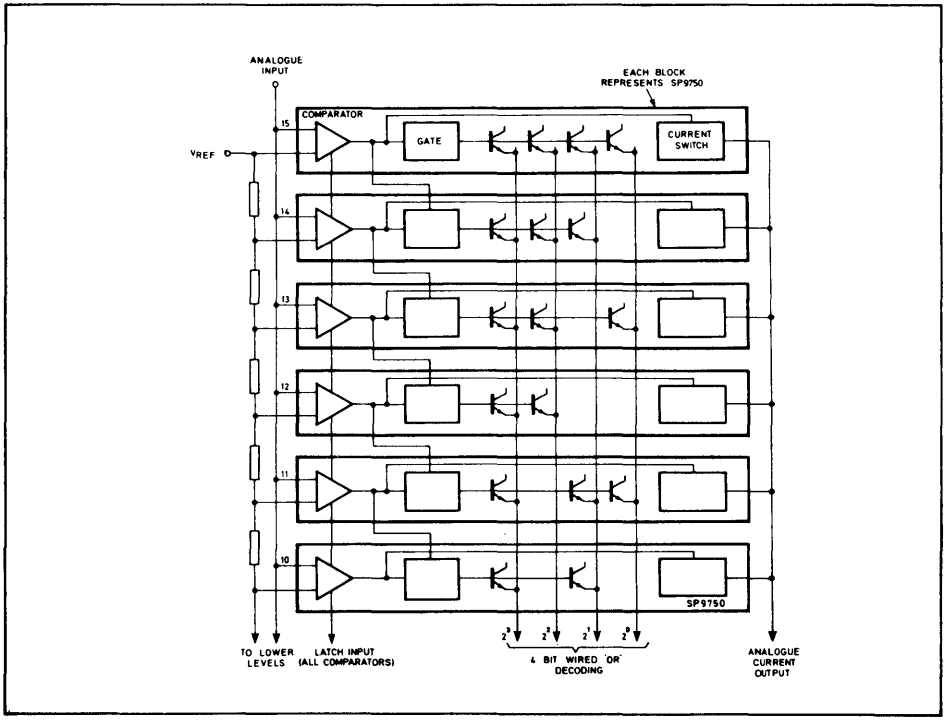


Fig. 6 Block diagram of 4-bit LSB stage showing top six levels

Fig. 7 Performance curves. Unless otherwise specified, standard conditions for all curves are $T_{AMB} = 25°C$, $V_{CC} = 5.0V$, $V_{EE} = -5.2V$, $V_{REF} = -8.0V$, I_O load $= 50\Omega$

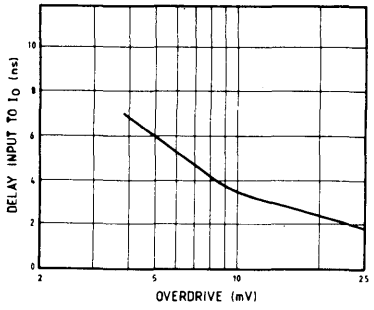


Fig. 7a input to 1_O output delay v. overdrive

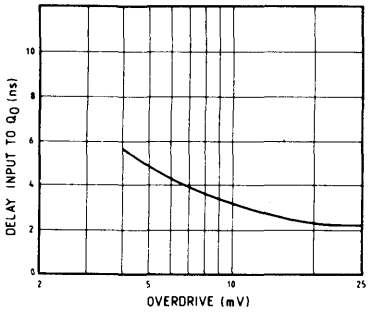


Fig. 7b Input to Q_O output delay v. overdrive

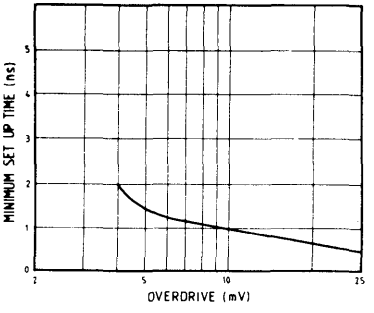


Fig. 7c T_S v. overdrive set-up time

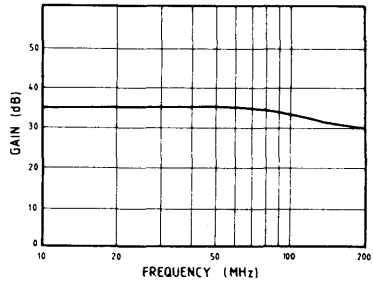


Fig. 7d Small signal gain v. frequency (to Q_O output). Latch input low.

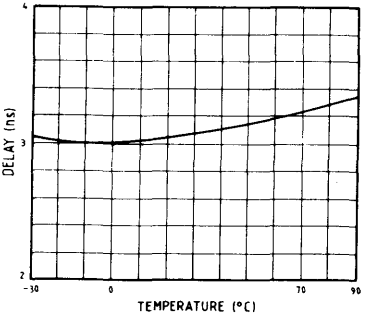


Fig. 7e Input to 1_O output delay as a function ot temperature

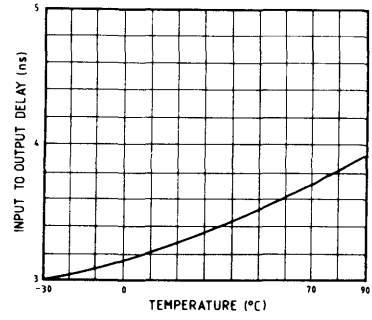


Fig. 7f Input to Q_O output delay as a function of temperature

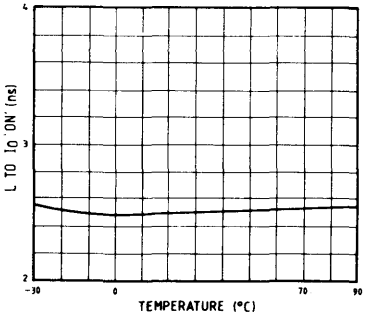


Fig. 7g Latch to I_O 'on' delay as a function of temperature

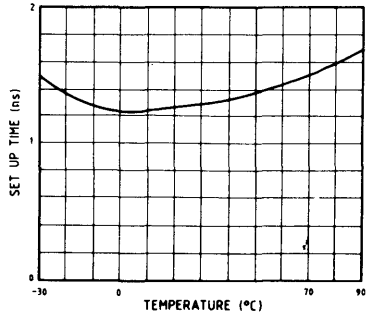


Fig. 7h Minimum set-up time as a function of temperature

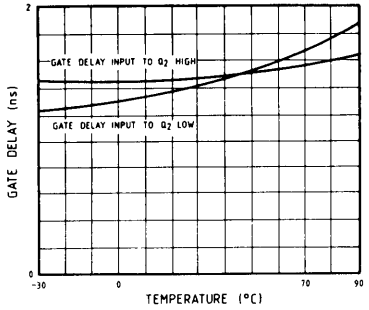


Fig. 7i Gate input to Q_1 – Q_4 delay variation with temperature

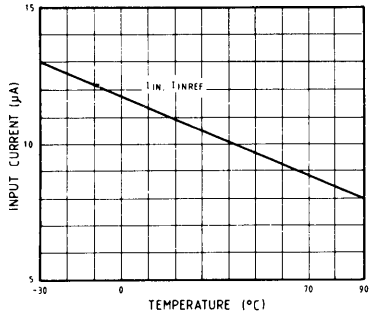


Fig. 7k Input current variation with temperature

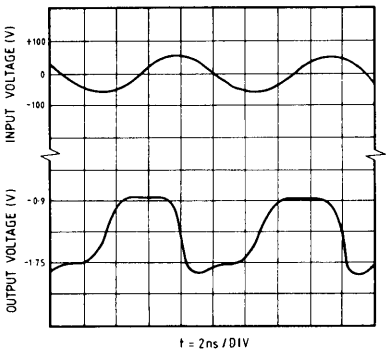


Fig. 7j Response to 100MHz sine wave

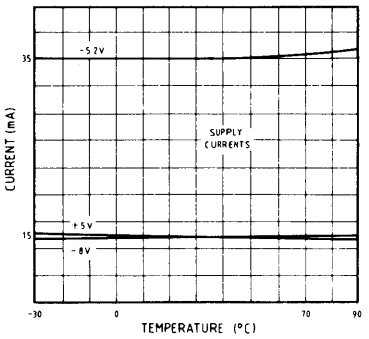


Fig. 7l Supply current variation with temperature

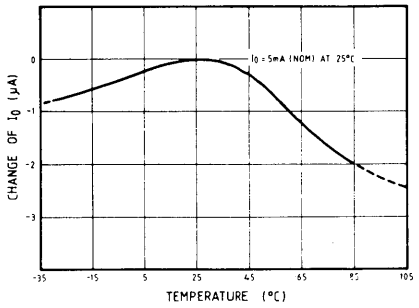


Fig. 7M Analogue output current variation with temperature

SP9752

TWO BIT EXPANDABLE A TO D CONVERTER

The SP9752 is a circuit block containing four comparators with associated decoding logic intended for use in the construction of A/D converter systems where the ultimate in speed performance is required.. Input and output logic levels are ECL compatible.

FEATURES

- Minimum set–up time 2 nS
- Maximum input offset 5 mV
- Latch to output delay 4 nS
- Maximum clock frequency 125 MHz
- Four comparators in 16–lead pack
- On–chip decoding with carry and $\overline{carry}$

GENERAL DESCRIPTION

Following the concept of the SP9750 and SP9685 high speed latched comparators, the SP9752 contains four comparator elements with master–slave latches in a configuration optimised for use in fast parallel, or combinatiob series–parallel A–D converters. Each comparator has a relatively low gain in the track mode, followed by a latch stage conferring essentially infinite gain in the hold mode to produce an unambiguous decision. On–chip decoding logic converts the master latch outputs into binary coded format, then slave latches hold the information through the clock period for maximum system flexibility. The provision of a complementary carry out (Co) eases the decode logic requirement. It is anticipated that most ystem designs using the SP9752 will be realised in ECL 10K logic for high speed operation with a minimum package count. Logic inputs to, and futputs from, the device are fully ECL compatible.

The basic comparator circuit is shown in Figure 3. Transistors Q1A, Q1B, Q2A, Q2B provide high input impedance, low offset modest gain in the track mode, but are switched off in hold when the cross–coupled pair Q5A, Q5B provide the latch function.

The slave latches are essentially simplified versions of the master latches. Master–slave action is determined be on–chip timing operations, and produces essentially glitch–free output conditions which are a pre–requisite of a successful multi–chip converter.

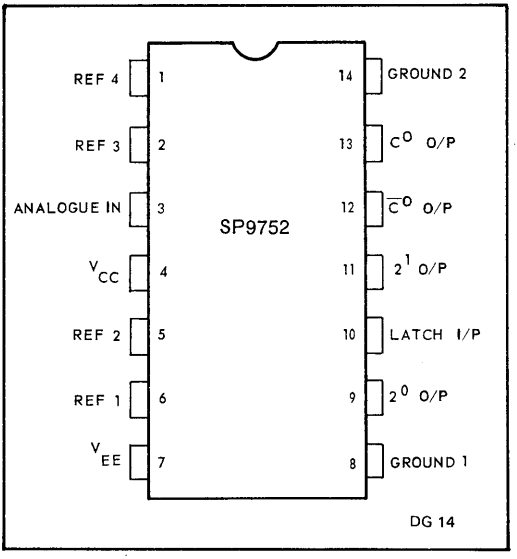


Fig. 1 Pin Connections.

DEFINTIONS

t_{pw} Minimum latch pulse width – the minimum time that the latch signal must be in the high (ECL definition) state for input acquisition to take place.

t_h Minimum hold time – the minimum time for which the input signal must maintain a particular level after the negative latch transistion for acquisition to take place.

t_s Minimum latch set–up time – the minimum time before the negative latch transistion that an input signal must be present for acquisition to take place.

t_{pd} Latch–to–output delay – the propagation delay measured from the 50% point of a latch transition to the 50%point of the corresponding output transition.

F_{CM} Maximum clock frequency – the maximum repetition rate of the latch command.

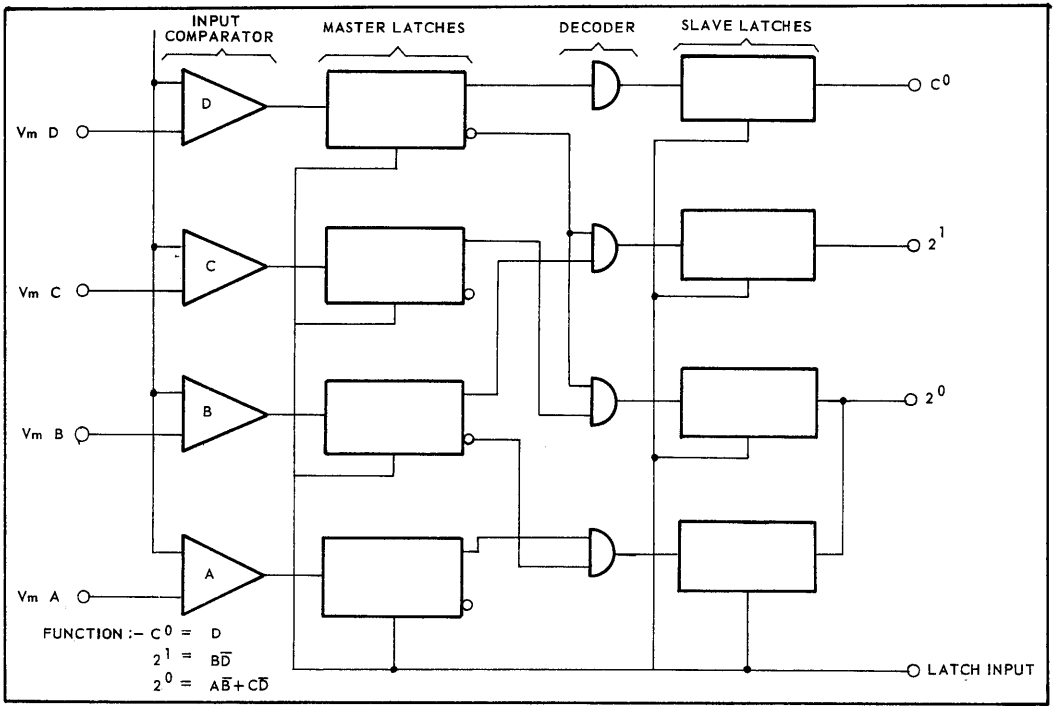

INPUT COMPARATOR
MASTER LATCHES
DECODER
SLAVE LATCHES
Vm D
Vm C
Vm B
Vm A
D
C
B
A
C0
21
20
LATCH INPUT
FUNCTION :- C0 = D
21 = BD̄
20 = AB̄+CD̄

Fig. 2.

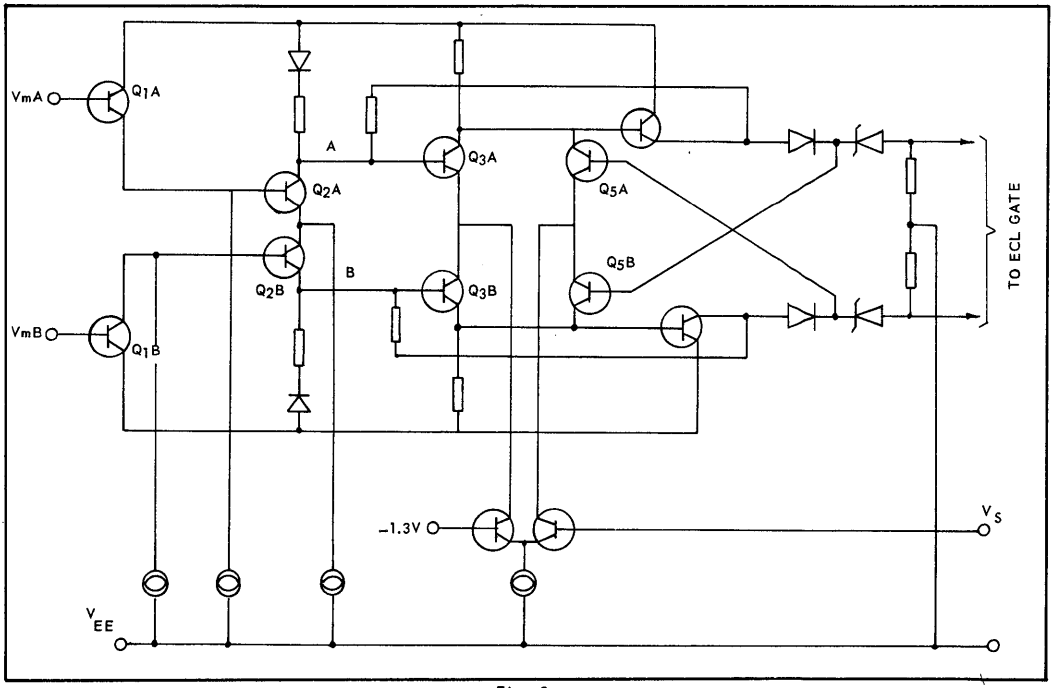

VmA
VmB
Q1A
Q1B
Q2A
Q2B
Q3A
Q3B
Q5A
Q5B
A
B
-1.3V
VS
VEE
TO ECL GATE

Fig. 3

ELECTRICAL CHARACTERISTICS

Test Conditions:–

T_{AMB} = 20°C

V_{CC} = 5.00V ±.25V

V_{EE} = –7.00 ±.25V

R_L = 50 ohm (equivalent)

Characteristic	Min	Typ	Max	Units	Comments
Input Offset Voltage	–5		+5	mV	R_{SOURCE} <100 Ω
Input Bias Current		14	40	µA	
Reference Input Current		4	10	µA	
Supply Current I_{CC}		41	60	mA	
Supply Current I_{ee}		76	90	mA	
Total Power Dissipation		750		mW	
Min. Latch Set–up Time			2	nS	
Latch to Output Delay		4		nS	Input o/d> 10mV
Min. Hold Time		4		nS	
Min. Latch Pulse Width		4		nS	
Max. Clock Frequency		125		MHz	
Input Capacitance		6.2		pF	
Latch Input Capacitance		2.6		pF	
Common Mode Range	–2.0		+2.0	V	
Output Logic Levels					
Output High	–.96		–.81	V	) Standard ECL
Output Low	–1.85		–1.65	V	)
Operating Temp. Range	–30°		+85°	°C	500 L.F.P.M. air flow

DYNAMIC TESTING

High speed testing of devices of this kind is necessarily a difficult undertaking and the suggested circuit shown in Figure 4 should be carefully constructed if accurate results are to be obtained. The test arrangement is designed to select a single comparator and to measure the response times from the latch to the outputs. Input to output delay are difficult to deal with due to the master/slave action; more relevant are the set–up and hold times. Operation is as follows:

1. Select the comparator to be tested by S3
2. Select position 1 on S2
3. Adjust for a middle state of the outputs using S1. The output should be randomly triggered by noise into alernate states.
4. Set up offset (2mV, 5mV or 10mV on S2 and measure the appropriate delays.
5. Repeat 1–4 on next comparator.

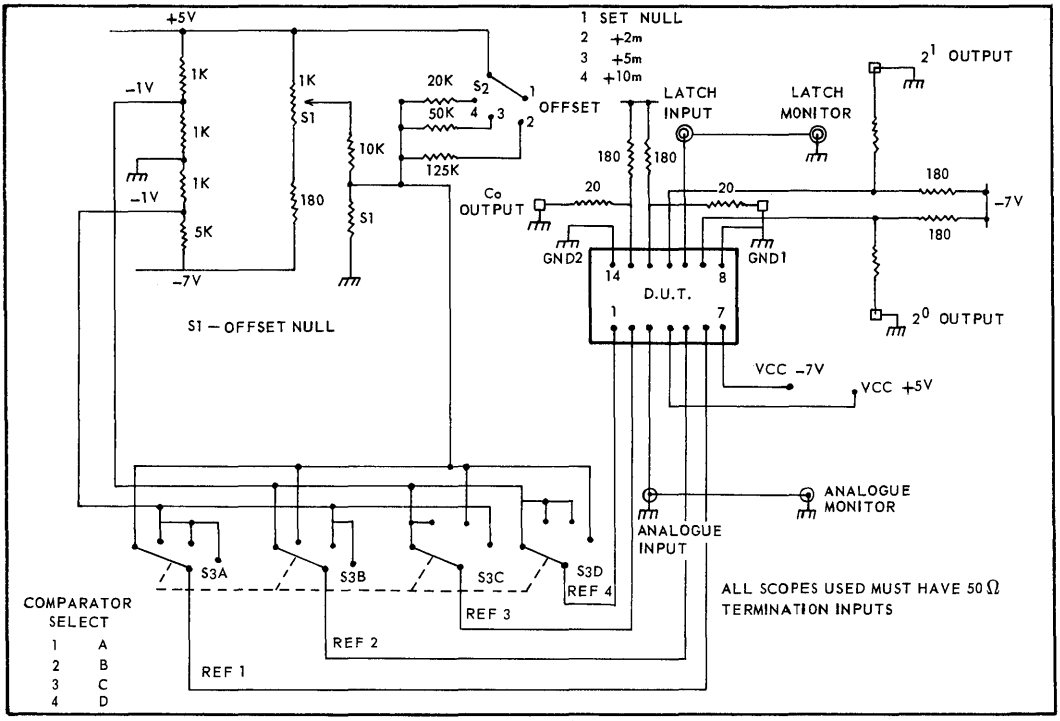


Fig. 4 Dynamic Test Box Wiring Diagram.

APPLICATIONS

5–bit ADC 125 MHz

A five–bit all–parallel ADC is shown in Figure 5. Operation at 125MHz is possible with no missing codes. Analogue and latch inputs are distributed along transmission lines designed to have matched propagation delays, to minimise latch aperture error. in many applications this avoids the need for a separate sample and hold function. The system input voltage range is ±1.5 volts at 50 ohms. En–coding is by ECL 10K logic, which is the prime speed limitation

The use of master/slave latching retimes the outputs which are available for the whole clock period.

This converter concept can be extended in principle to nine bits, but practical considerations limit the usefulness in all–parallel systems to six or seven bits, as, for example, seven bits require 32 SP9752's eight bits require 64, ect. In addition, latch and input signal distribution of sufficient accuracy becomes difficult, particularly in relation to aperture error.

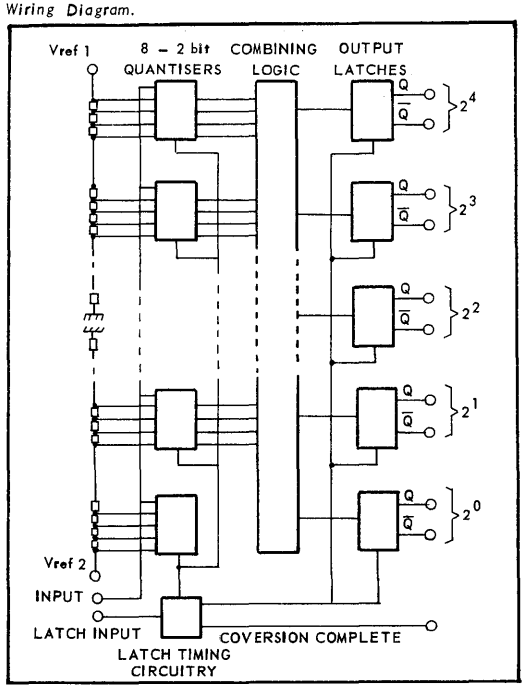


Fig. 5 Block Diagram of 5 bit A/D Converter.

SP9754

FOUR BIT EXPANDABLE A TO D CONVERTER

The SP9754 is a fast 4 bit A/D converter, expandable up to 8 bits without additional encoding circuitry.

It can convert at sample rates from DC to 110MHz, with analogue inputs up to Nyquist frequencies. All output levels are E.C.L. compatible.

The latch function to the device provides on–chip sampling which allows the converter to operate with out an external sample and hold. Data is clocked through the device in masterslave fashion, ensuring that all outputs are synchronous and valid for the complete clock period.

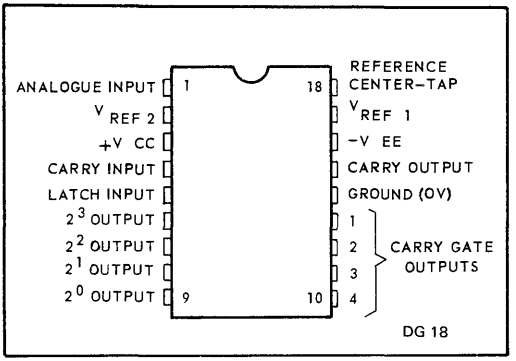


Fig. 1 Pin Connections

FEATURES

- No external components for 4–bit conversion.
- 110MHz conversion rate.
- On–chip encoding for expansion to 8 bits.
- No external sample and hold needed.
- On–chip resistor reference divider.
- Bit size 10–100mV.
- ECL compatible.

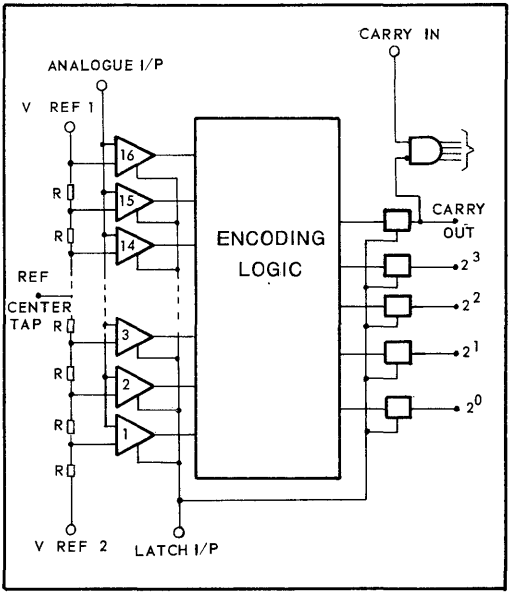


Fig. 2 Functional Diagram

ABSOLUTE MAXIMUM RATINGS

Positive supply voltage	+5.5V
Negative supply voltage	–7.5V
Operating temperature range	$-30^{o}C$ to $85^{o}C$
Storage temperature	$-55^{o}C$ to $+125^{o}C$
Lead temperature (soldering 60sec)	$300^{o}C$

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):–

T_{AMB} = 25°C

V_{CC} = +5V

V_{EE} = –7V

R_L = 100 ohm to –2V

CHARACTERISTIC	SYMBOL	VALUE				CONDITIONS
		Min	Typ	Max	Units	
Analogue input current	I_B		30	100	µA	V_{IN} = OV
Analogue input capacitance	C_{IN}		10		pF	
Common mode range	V_{CM}	–2		+2	V	
Maximum input slewrate			1000		V/µsec	
Latch input capacitance	C_{IN}		2		pF	
Positive supply current	I+		55	65	mA	) See Fig. 11.
Negative supply current	I–		85	95	mA	)
Reference resistor chain			25		Ω	
Reference bit size		10		100	mV	
Comparator offset voltage	V_{os}	–5		+5	mV	
Total power dissipation	P_{DISS}		950	1100	mW	All outputs loaded
Output logic levels						
Logic high	V_{OH}	–0.930		–0.720	V	) for 100 ohm load
Logic Low	V_{OL}	–1.850		–1.620	V	) to –2V
Min. latch set–up time	t_S		1.5	2	nsec	10mV overdrive
Latch to output propagation delay						
Latch enable to output high	$t_{pd}+(E)$		6	8	nsec	
Latch enable to output low	$t_{pd}-(E)$		5	8	nsec	
Carry input to M.S.B. delay	t_{pd} (C)		3	5	nsec	
Max. sample rate	$F_{c\ max.}$	100	110		MHz	

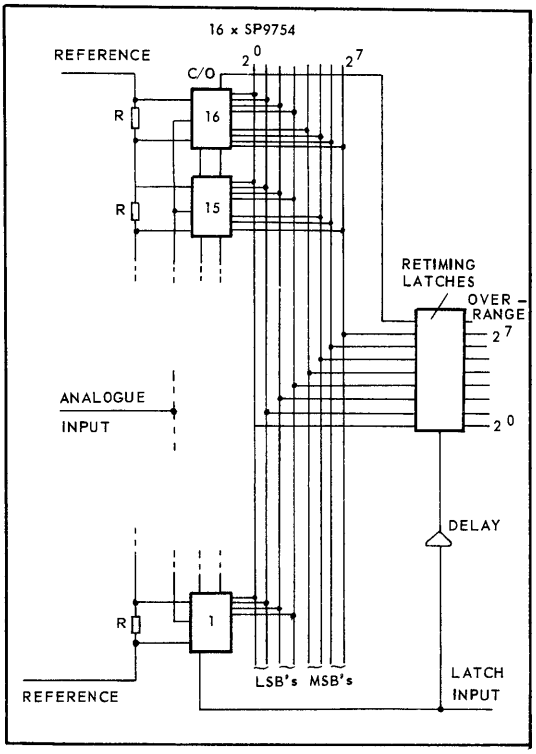


Fig. 3 8–bit All Parallel System

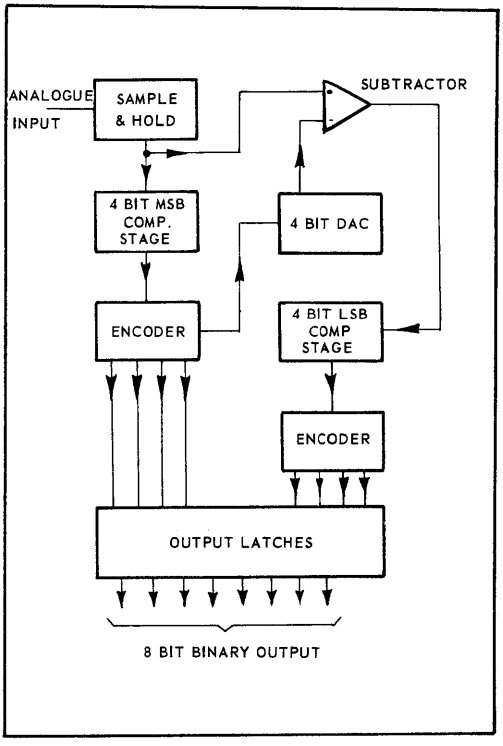


Fig. 4 Parallel Series Parallel System

PERFORMANCE CURVES

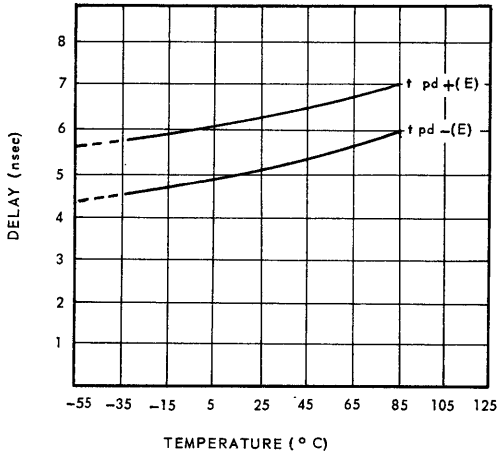


Fig. 5 Latch to Output Propagation Delay as a Function of Temperature

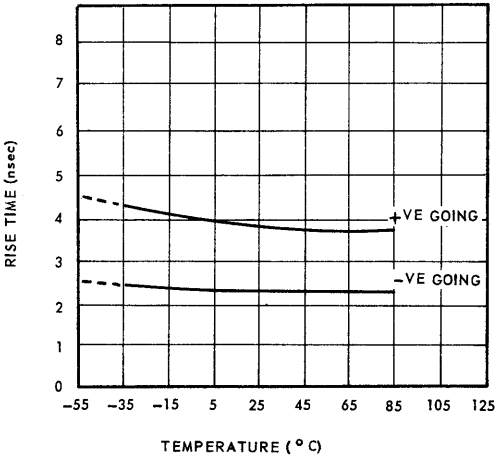


Fig. 6 Output Rise/Fall Times as a Function of Temperature

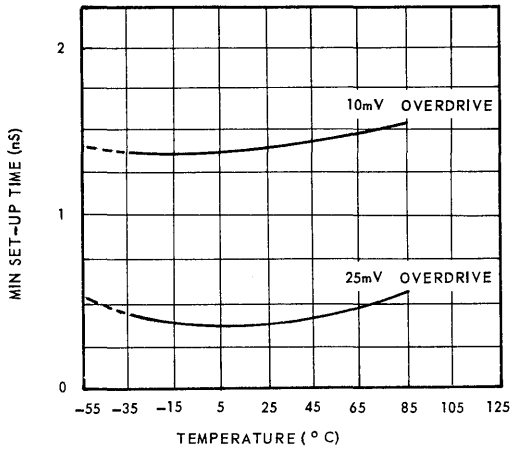


Fig. 7 Set-up Time as a Function of Temperature

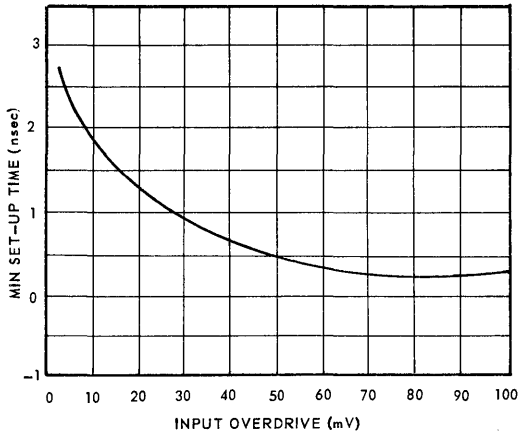


Fig. 8 Set-up Time as a Function of Overdrive

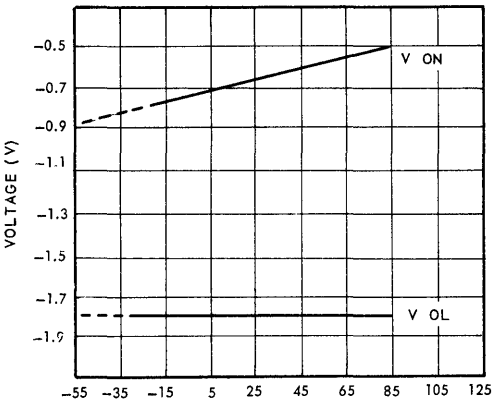


Fig. 9 Output Logic Levels as a Function of Temperature

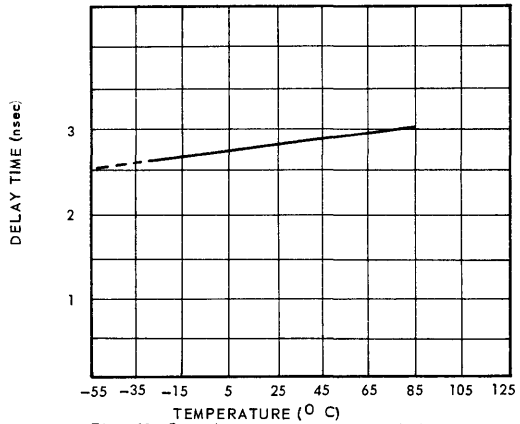


Fig. 10 Carry Input to M.S.B. Output Delay as a Function to Temperature

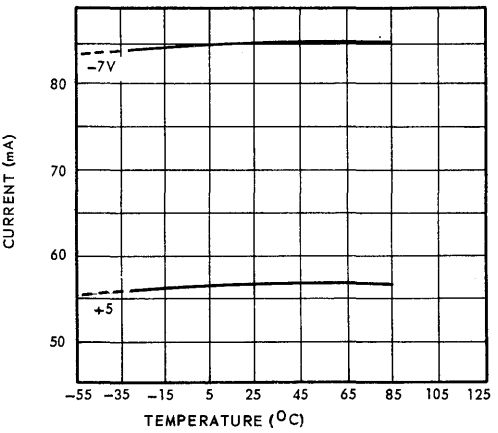


Fig. 11 Supply Current as a Function of Temperature

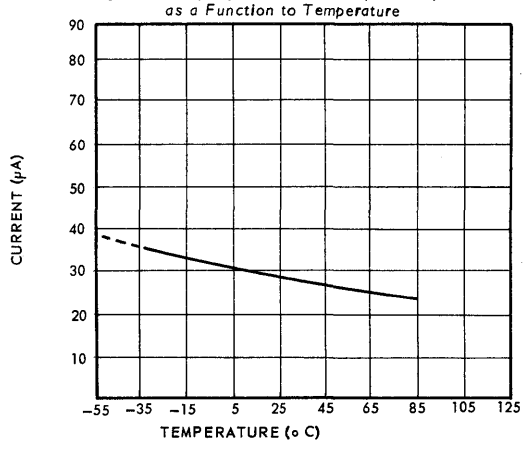


Fig. 12 Analogue Input Current as a Function of Temperature

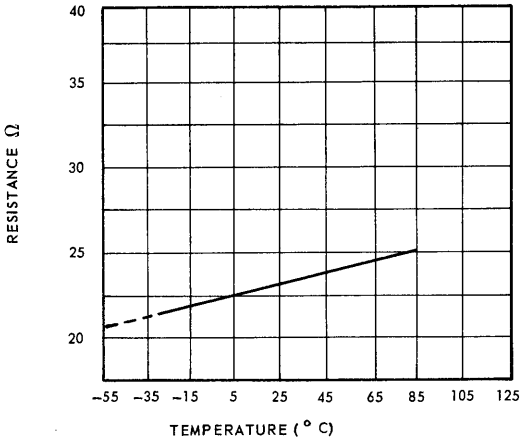


Fig. 13 Network Resistance as a Function of Temperature

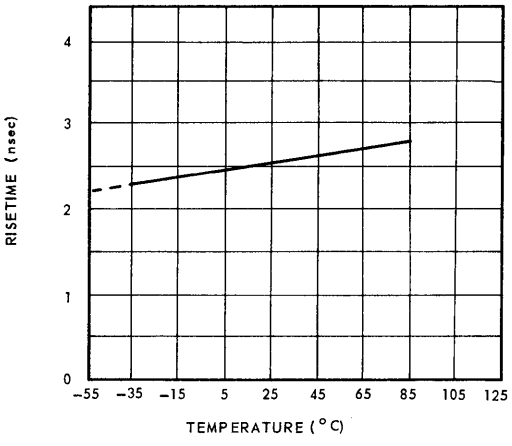


Fig. 14 M.S.B. Output Edge Speeds as a Function of Temperature

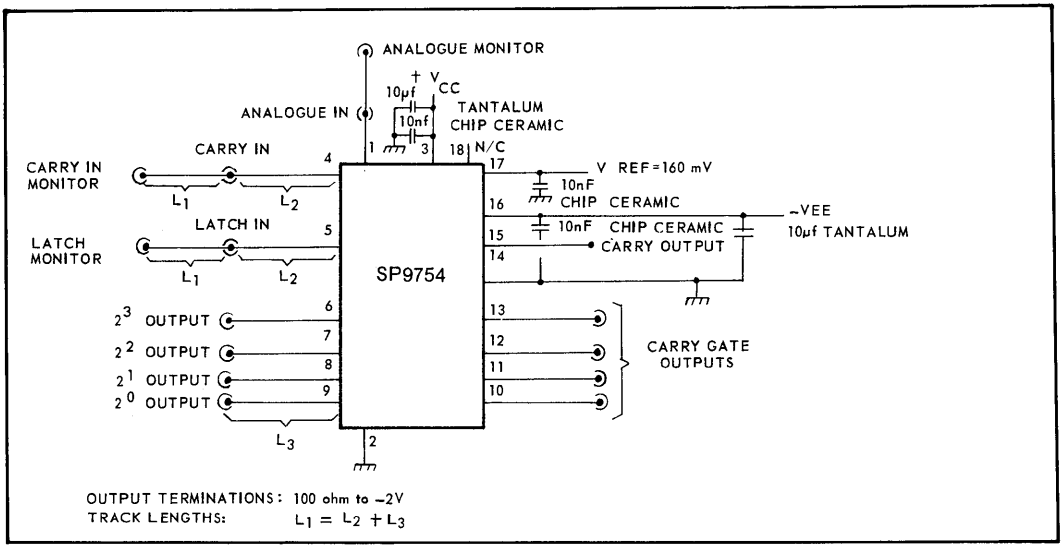
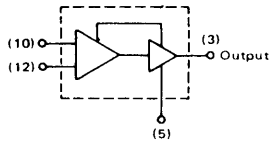


Fig. 15 Test and Applications Circuit for SP9754

8. ECL III Technical Data

VOLTAGE-CONTROLLED OSCILLATOR

SP1648



Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

DG 14

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silcon chip. Output levels are compatible with PECL III logic levels. The oscillator requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The SP1648 is used in the Phase-Locked Loop shown in Figure 9. This device may be used in many applications requiring a fixed or variable frequency clock source of high spectral purity (See figure 2).

The SP1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

SUPPLY VOLTAGE	GND PINS	SUPPLY PINS
+5.0 Vdc	7, 8	1, 14
-5.2 Vdc	1, 14	7, 8

FIGURE 1 – CIRCUIT SCHEMATIC

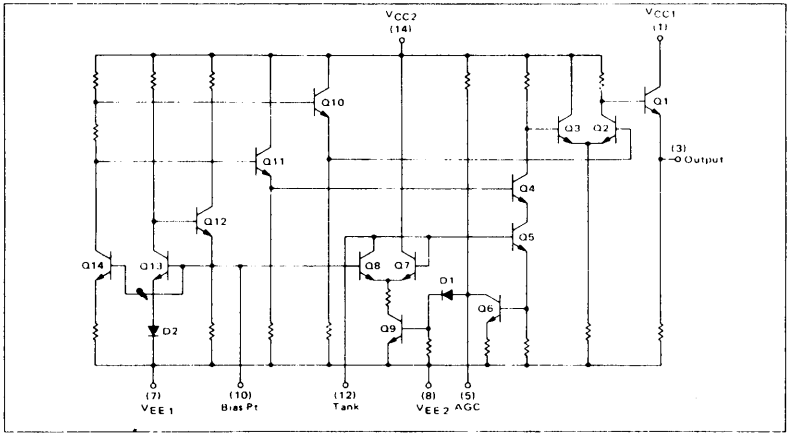
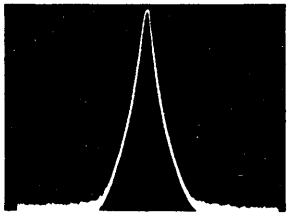
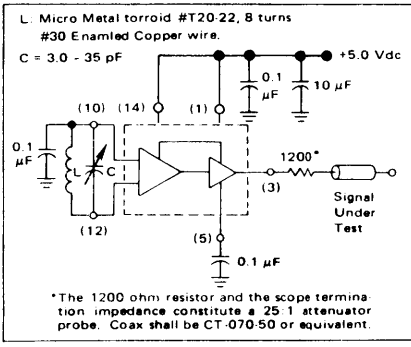


FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT



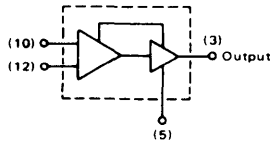
B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



*The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 volts



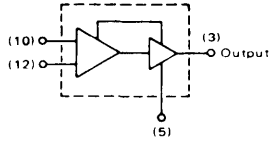
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	mAdc I_L
-30°C	+1.960	+1.410	5.0	-5.0
+25°C	+1.800	+1.300	5.0	-5.0
+85°C	+1.680	+1.180	5.0	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{CC}	I_L	V_{EE} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	40	—	—	mAdc	—	—	1.14	—	7,8
Logic "1" Output Voltage	V_{OH}	3	3.94	4.18	4.04	4.25	4.11	4.36	Vdc	—	12	1.14	3	7,8
Logic "0" Output Voltage	V_{OL}	3	3.16	3.40	3.20	3.43	3.23	3.46	Vdc	12	—	1.14	3	7,8
Bias Voltage*	V_{Bias}	10	1.51	1.86	1.40	1.70	1.28	1.58	Vdc	—	—	1.14	—	7,8
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max						
Peak to Peak Tank Voltage	V_{p-p}	12	—	—	—	—	500	—	—	—	—	mV	See Figure 3	—	1.14	3	7,8
Output Duty Cycle	V_{DC}	3	—	—	—	—	50	—	—	—	—	%	See Figure 3	—	1.14	3	7,8
Oscillation Frequency	f_{max}	—	—	—	—	200	225	—	—	—	—	MHz	See Figure 3	—	1.14	3	7,8

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 volts

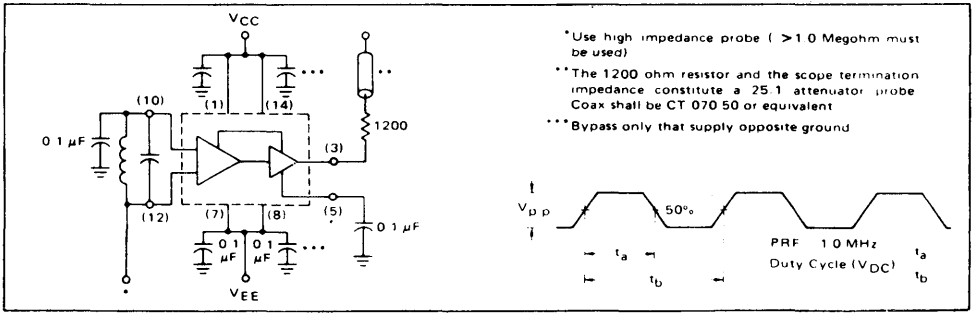


@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	mAdc I_L
-30°C	-3.300	-3.800	-5.2	-5.0
+25°C	-3.400	-3.900	-5.2	-5.0
+85°C	-3.500	-4.000	-5.2	-5.0

Characteristic	Symbol	Pin Under Test	SP1648 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	V_{EE}	I_L	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	—	—	—	41	—	—	mAdc	—	—	7.8	—	1.14
Logic "1" Output Voltage	V_{OH}	3	-1.045	-0.815	-0.960	-0.750	-0.890	-0.650	Vdc	—	12	7.8	3	1.14
Logic "0" Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	12	—	7.8	3	1.14
Bias Voltage*	V_{Bias}	10	-3.690	-3.340	-3.800	-3.500	-3.920	-3.620	Vdc	—	—	7.8	—	1.14
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max						
Peak to Peak Tank Voltage	V_{p-p}	12	—	—	—	—	500	—	—	—	—	mV	See Figure 3	—	7.8	3	1.14
Output Duty Cycle	V_{DC}	3	—	—	—	—	50	—	—	—	—	%	See Figure 3	—	7.8	3	1.14
Oscillation Frequency	f_{max}	—	—	—	—	200	225	—	—	—	—	MHz	See Figure 3	—	7.8	3	1.14

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS



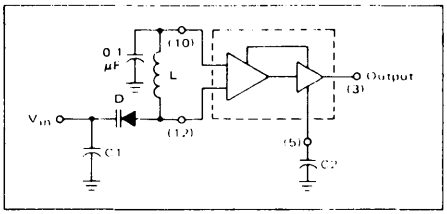
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (Q4) is used to translate from the emitter follower (Q5) to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provide a highly buffered output which produces a square wave. Transistors Q10 thru Q14 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

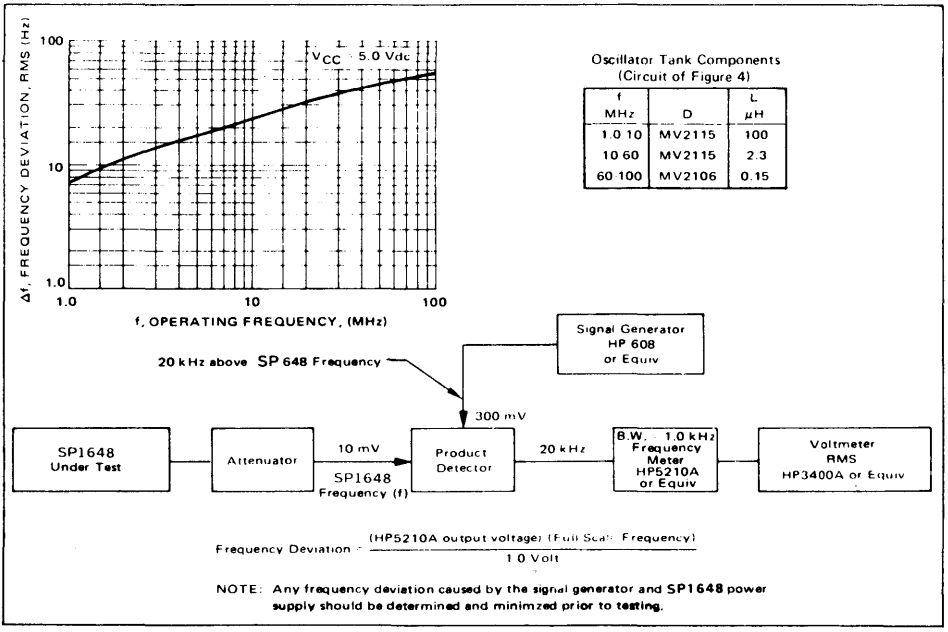
When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$ 1.4 V for positive supply operation).

FIGURE 4 – THE SP1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



NOTE: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimized prior to testing.

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE
USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^oC$

FIGURE 6

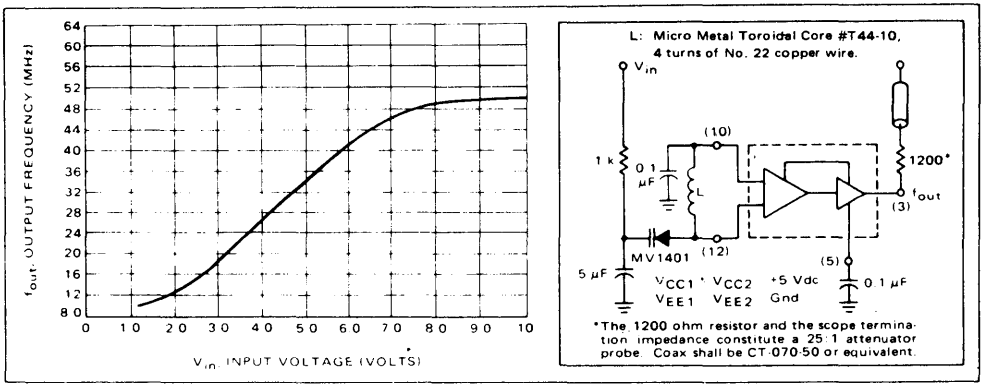


FIGURE 7

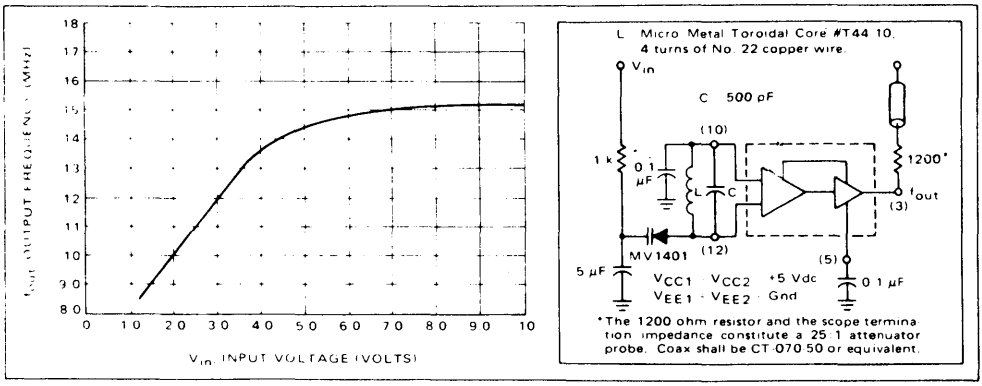
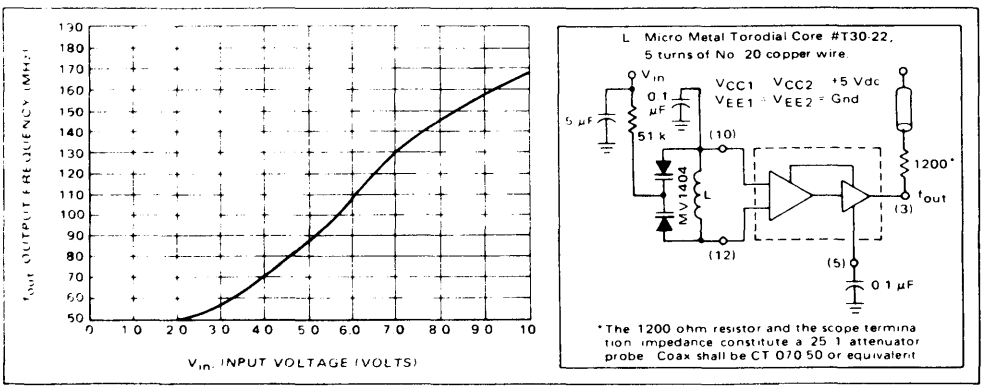


FIGURE 8



Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7 and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (pluse the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\ (max) + C_S}}{\sqrt{C_D\ (min) + C_S}}$$

$$\text{where } f_{min} = \frac{1}{2\pi\sqrt{L\ (C_D\ (max) + C_S)}}$$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins (see Figure 2).

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the SP1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and land-mobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translation, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lock-up. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION

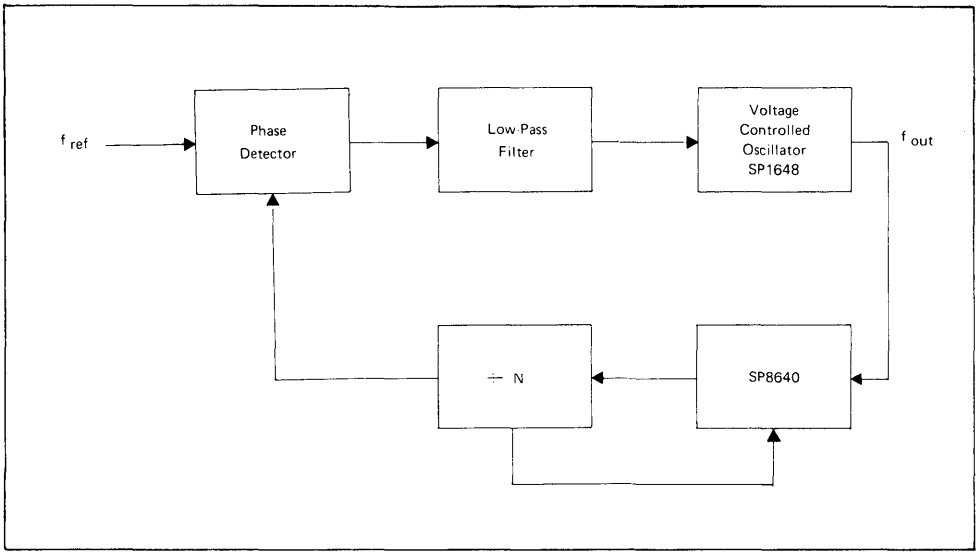


Figure 10 shows the SP1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the SP1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the SP1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the PECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT

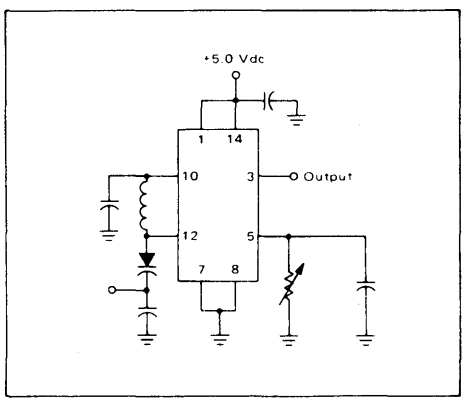


FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE SP1648 (SQUARE WAVE OUTPUT)

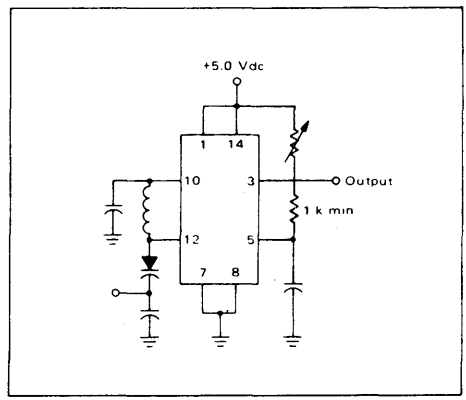


FIGURE 12 – CIRCUIT SCHEMATIC USED FOR COLLECTOR OUTPUT OPERATION

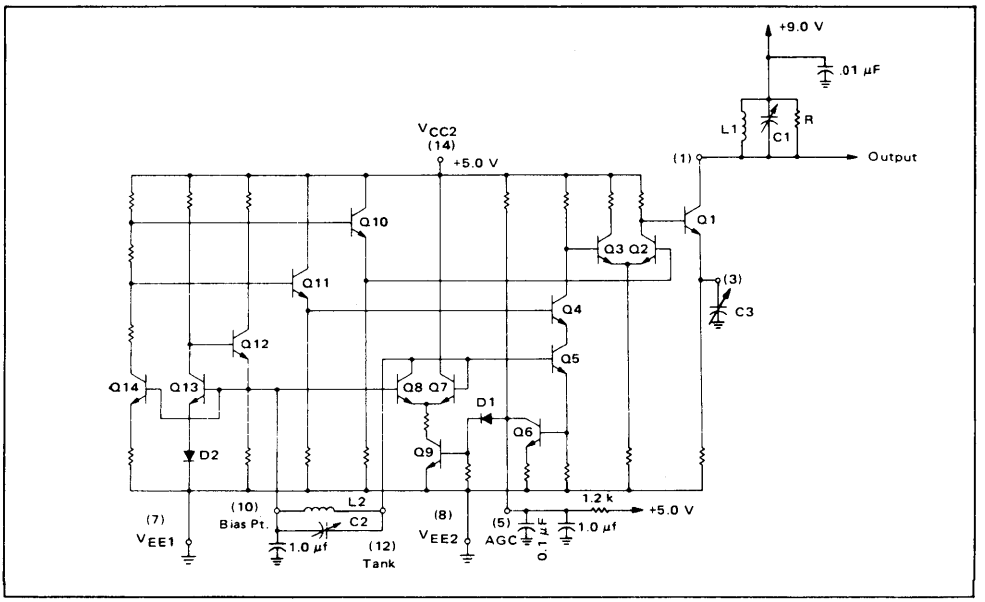


FIGURE 13 – POWER OUTPUT versus COLLECTOR LOAD

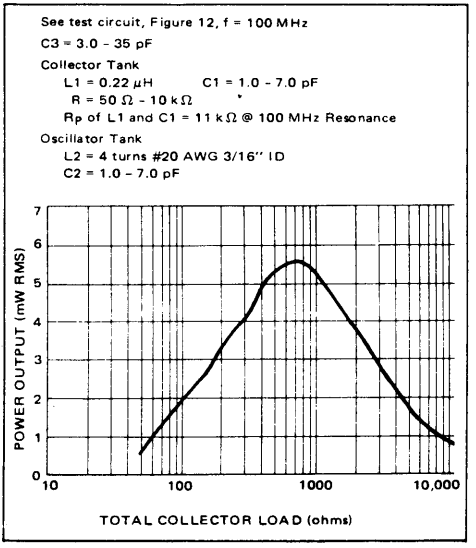
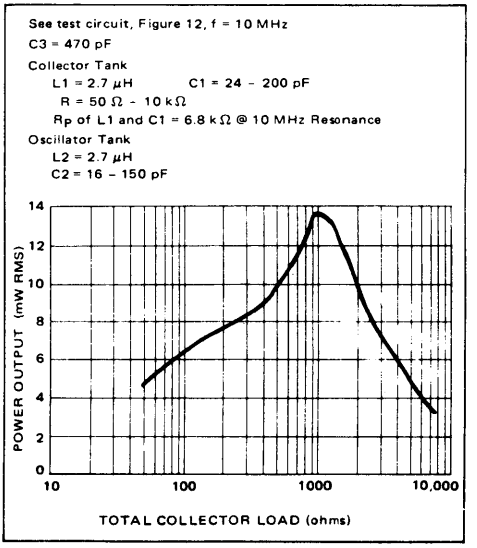
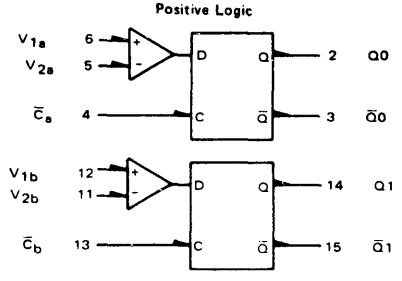


FIGURE 14 – POWER OUTPUT versus COLLECTOR LOAD



SP1650 • SP1651



V_{CC} = +5.0 V = Pin 7,10
V_{EE} = -5.2 V = Pin 8
Gnd = Pin 1,16

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (**SP1650**)
  = 3.0 ns typ (**SP1651**)
- Input Slew Rate = 350 V/μs (**SP1650**)
  = 500 V/μs (**SP1651**)
- Differential Input Voltage:
  -5.0 V to +5.0 V (-30°C to +85°C)
- Common Mode Range:
  -3.0 V to +2.5 V (-30°C to +85°C) (**SP1650**)
  -2.5 V to +3.0 V (-30°C to +85°C) (**SP1651**)
- Resolution: ≤20 mV (-30°C to +85°C)
- Drives 50 Ω lines

DG 16

The **SP1650** and the **SP1651** are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The **SP1650** provides high impedance Darlington inputs, while the **SP-1651** is a lower impedance option, with higher input slew rate and higher speed capability.

Complementary outputs permit maximum utility for applications in high speed test equipment, frequency measurement, sample and hold, peak voltage detection, transmitters, receivers, memory translation, sense amplifiers and more.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$) operate from PECL III or PECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}0$ is the logic complement of Q0. When the clock input goes to a low logic level, the outputs are latched in their present state.

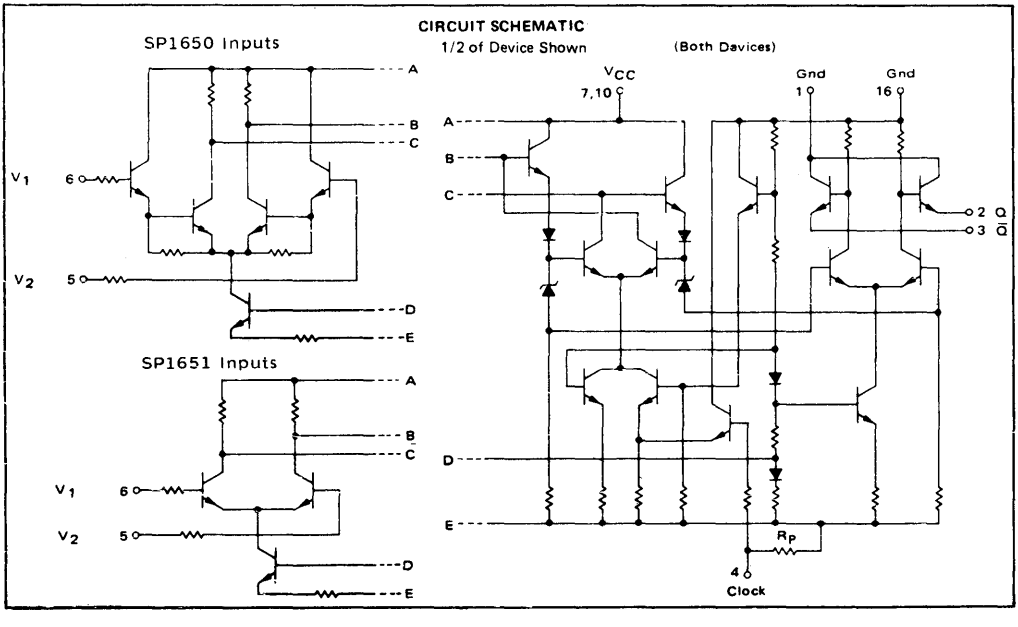
Assessment of the performance differences between the **SP1650** and the **SP1651** may be based upon the relative behaviors shown in Figures 3 and 6.

TRUTH TABLE

$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

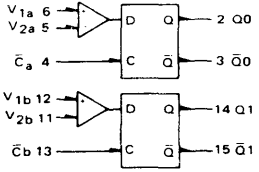
CIRCUIT SCHEMATIC
1/2 of Device Shown (Both Devices)



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data

POSITIVE LOGIC



@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

TEST VOLTAGE VALUES (Volts)

Characteristic	Symbol	Pin Under Test	SP1650/SP1651 Test Limits ① -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③	Gnd
			TEST VOLTAGE APPLIED TO PINS LISTED BELOW																			
Power Supply Drain Current																						
Positive	I_{CC}	7,10	-	-	-	25*	-	-	mAdc		4.13			6,12	-	-	-	-	-	7,10	8	1,5,11,16
Negative	I_E	8	-	-	-	55*	-	-	mAdc	4.13	-	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
Input Current	I_{in}																					
SP1650		6	-	-	-	10	-	-	µAdc	4	13	-	-	12	-	6	-	-	-	7,10	8	1,5,11,16
SP1651		6	-	-	-	40	-	-	µAdc	4	13	-	-	12	-	6	-	-	-	7,10	8	1,5,11,16
Input Leakage Current	I_R																					
SP1650		6	-	-	-	7	-	-	µAdc	4	13	-	-	12	-	-	-	6	-	7,10	8	1,5,11,16
SP1651		6	-	-	-	10	-	-	µAdc	4	13	-	-	12	-	-	-	6	-	7,10	8	1,5,11,16
Input Clock Current	I_{inH}	4	-	-	-	350	-	-	µAdc	4	13	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
	I_{inL}	4	-	-	0.5	-	-	-	µAdc		13	-	-	6,12	-	-	-	-	-	7,10	4,8	1,5,11,16
Logic "1" Output Voltage	V_{OH}	2	-1045	-0875	-0960	-0810	-0890	-0700	Vdc	4.13	-	-	-	6,12	-	-	-	-	-	7,10	8	1,5,11,16
		2													5,11	-	-	-	-			1,6,12,16
		2												-	-	6,12	5,11	-	-			1,16
		2												-	-	-	-	5,11	6,12			1,16
		3												-	6,12	-	-	-	-			1,5,11,16
		3												5,11	-	-	-	-	-			1,6,12,16
		3												-	-	5,11	6,12	-	-			1,16
		3												-	-	-	-	6,12	5,11			1,16
Logic "0" Output Voltage	V_{OL}	2	-1890	-1650	-1850	-1620	-1830	-1575	Vdc	4.13	-	-	-	-	6,12	-	-	-	-	7,10	8	1,5,11,16
		2												5,11	-	-	-	-	-			1,6,12,16
		2												-	-	5,11	6,12	-	-			1,16
		2												-	-	-	-	6,12	5,11			1,16
		3												6,12	-	-	-	-	-			1,5,11,16
		3												-	5,11	-	-	-	-			1,6,12,16
		3												-	-	6,12	5,11	-	-			1,16
		3												-	-	-	-	5,11	6,12			1,16
Logic "1" Threshold Voltage ①	V_{OHA}	2	-1065	-	-0980	-	-0910	-	Vdc	-	13	4	-	6	-	-	-	-	-	7,10	8	1,5,16
②		2		-		-		-		-		-	4	-	6	-	-	-	-			
		3	-	-	-	-	-	-	*	-	-	4	-	-	6	-	-	-	-	-	-	-
		3	-	-	-	-	-	-		-	-	-	4	6	-	-	-	-	-	-	-	-
Logic "0" Threshold Voltage ①	V_{OLA}	3	-	-1630	-	-1600	-	-1555	Vdc	-	13	4	-	6	-	-	-	-	-	7,10	8	1,5,16
②		3	-		-		-			-		-	4	-	6	-	-	-	-			
		2	-	-	-	-	-	-		-	-	4	-	-	6	-	-	-	-	-	-	-
		2	-	-	-	-	-	-		-	-	-	4	6	-	-	-	-	-	-	-	-

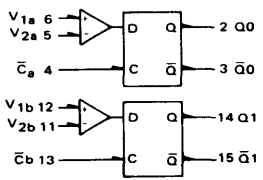
NOTES ① All data is for a SP1650 or SP1651, except data marked (*) which refers to the entire package
② These tests done in order indicated. See Figure 4.
③ Maximum Power Supply Voltages (beyond which device life may be impaired)
V_{EE} +0.5 to -7.12 Vdc

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
SP1650	+3.000	+2.980	-2.500	-2.480
SP1651	+2.500	+2.480	-3.000	-2.980

SWITCHING TIMES

POSITIVE LOGIC



@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①
-30°C	+2.000	See Note ④		+1.040	+2.00	+7.00	-3.20
+25°C	+2.000			+1.110	+2.00	+7.00	-3.20
+85°C	+2.000			+1.190	+2.00	+7.00	-3.20

Characteristic	Symbol	Pin Under Test	SP1650/1651 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{R1}	V_{R2}	V_{R3}	V_X	V_{XX}	V_{CC} ①	V_{EE} ①	See Figure 2 P1	P2	P3	P4
Switching Times Propagation Delay (50% to 50%) V-Input to Output	t_{6+2+}	2	2.0	5.0	2.0	5.0	2.0	5.7	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{6+2+}	2								–	5	–					–	6	–	–
	t_{6+2+}	2								–	–	5					–	–	6	–
	t_{6+3-}	3								5	–	–					6	–	–	–
	t_{6+3-}	3								–	5	–					–	6	–	–
	t_{6+3-}	3								–	–	5					–	–	6	–
	t_{6-2-}	2								5	–	–					6	–	–	–
	t_{6-2-}	2								–	5	–					–	6	–	–
	t_{6-2-}	2								–	–	5					–	–	6	–
	t_{6-3+}	3								5	–	–					6	–	–	–
	t_{6-3+}	3								–	5	–					–	6	–	–
	t_{6-3+}	3								–	–	5					–	–	6	–
Clock to Output ②	t_{4+2+}	2	2.0	4.7	2.0	4.7	2.0	5.2	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
	t_{4+2-}	2								6	–	–	–				5	–	–	
	t_{4+3+}	3								6	–	–	–				5	–	–	
	t_{4+3-}	3								5	–	–	–				6	–	–	
Clock Enable Time ③	t_{setup}	6	–	–	2.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Clock Aperture Time ③	t_{ap}	6	–	–	1.5	–	–	–	ns	5	–	–	–	1,11,16	7,10	8	6	–	–	4
Rise Time (10% to 90%)	t_{2+}	2	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3+}	3	1.0	3.5	1.0	3.5	1.0	3.8	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
Fall Time (10% to 90%)	t_{2-}	2	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–
	t_{3-}	3	1.0	3.0	1.0	3.0	1.0	3.3	ns	5	–	–	4	1,11,16	7,10	8	6	–	–	–

NOTES: ① Maximum Power Supply Voltages (beyond which device life may be impaired: $|V_{CC}| + |V_{EE}| \leq 12$ Vdc.

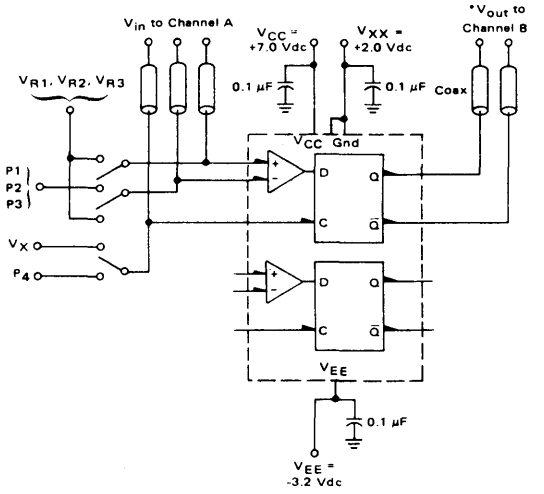
② Unused clock inputs may be tied to ground.

③ See Figure 8.

④

All Temperatures	V_{R2}	V_{R3}
SP1650	+4.900	-0.400
SP1651	+4.400	-0.900

FIGURE 1 – SWITCHING TIME TEST CIRCUIT @ 25°C



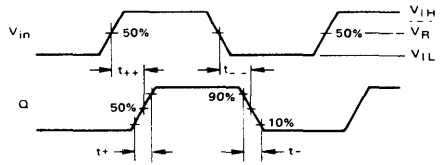
50-ohm termination to ground located in each scope channel input
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

*Complement of output under test should always be loaded with 50-ohms to ground.

FIGURE 2 – SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

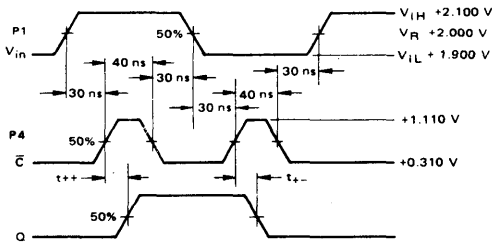


Test pulses: t_+, t_- = 1.5 ±0.2 ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle
V_{IH} is applied to $\overline{C}$ during tests.

TEST PULSE LEVELS

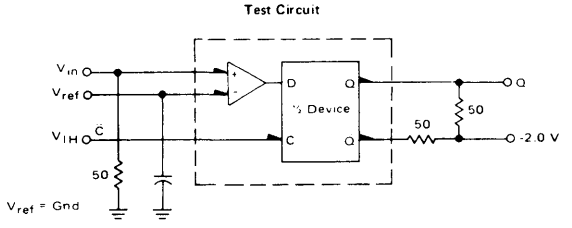
	Pulse 1		Pulse 2		Pulse 3	
	SP1650	SP1651	SP1650	SP1651	SP1650	SP1651
V_{IH}	+2.100 V	+2.100 V	+5.000 V	+4.500 V	-0.300 V	-0.800 V
V_R	+2.000 V	+2.000 V	+4.900 V	+4.400 V	-0.400 V	-0.900 V
V_{IL}	+1.900 V	+1.900 V	+4.800 V	+4.300 V	-0.500 V	-1.000 V

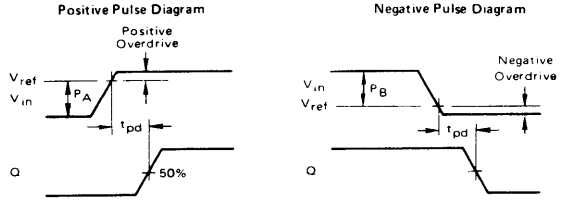
Clock to Output



P4: t_+, t_- = 1.5 ± 0.2 ns.

FIGURE 3 – PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE





Input switching time is constant at 1.5 ns (10% to 90%).

Propagation Delay versus Pulse Amplitude

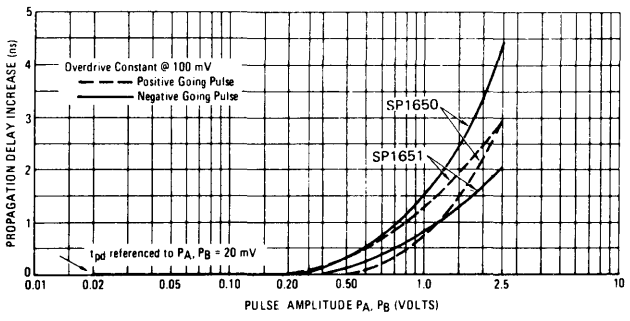


FIGURE 3 (continued)

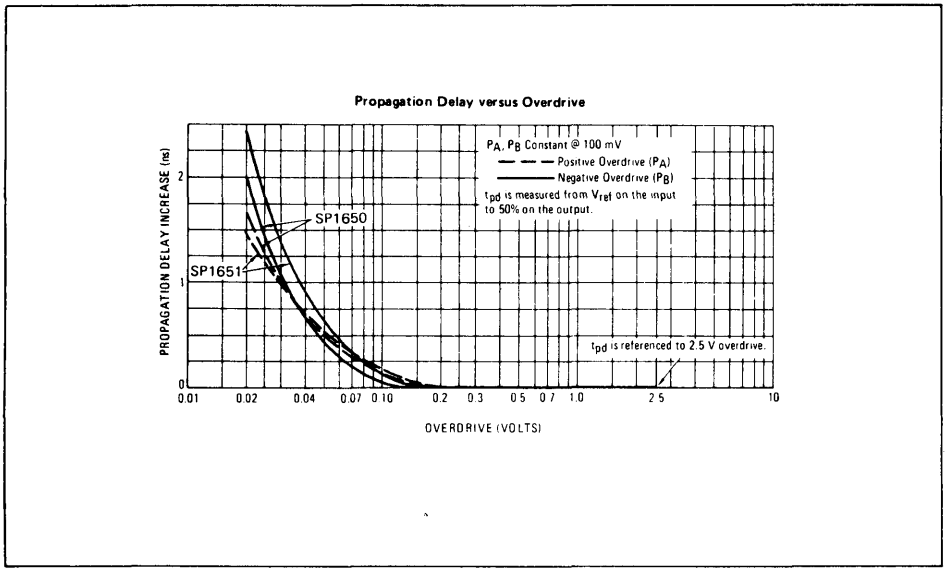


FIGURE 4 – LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

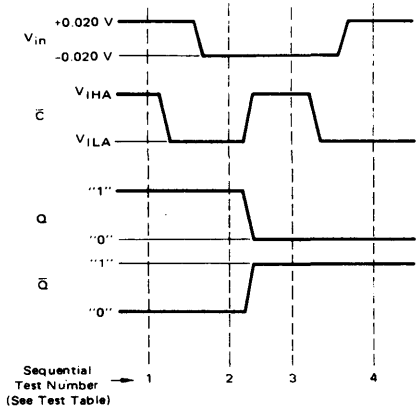
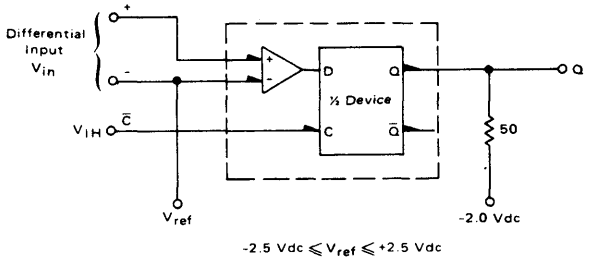


FIGURE 5 – TRANSFER CHARACTERISTICS (Q versus V_{in})

Test Configuration



-2.5 Vdc ≤ V_{ref} ≤ +2.5 Vdc

Typical Transfer Curves

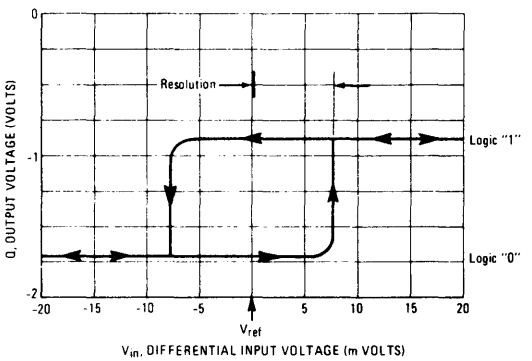
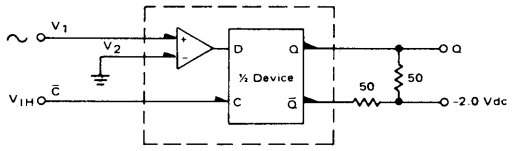
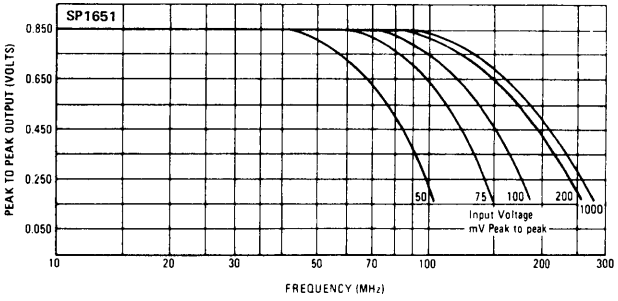


FIGURE 6 – OUTPUT VOLTAGE SWING versus FREQUENCY

(A) Test Circuit



(B) Typical Output Logic Swing versus Frequency



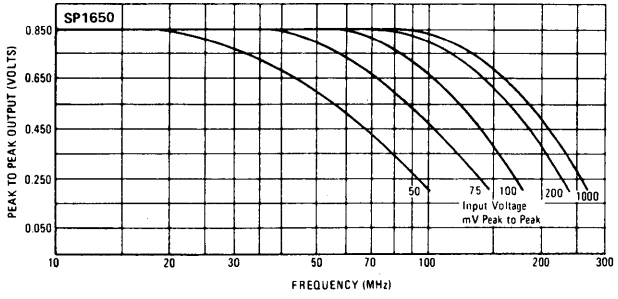
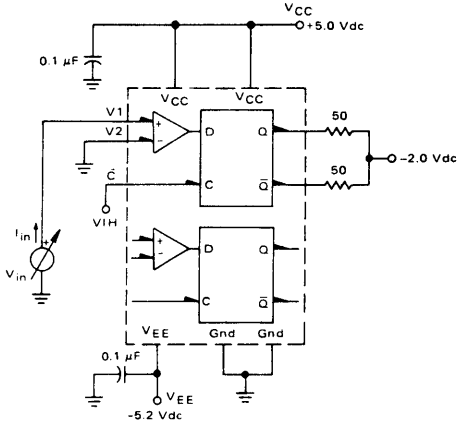
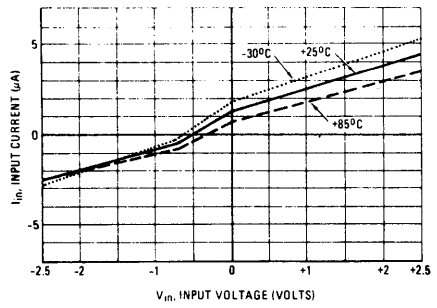


FIGURE 7 – INPUT CURRENT versus INPUT VOLTAGE

TEST CIRCUIT



Typical SP1650 (Complementary Input Grounded)



Typical SP1651 (Complementary Input Grounded)

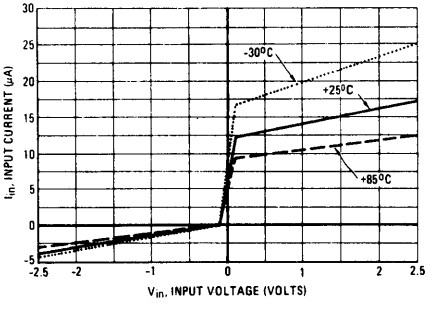
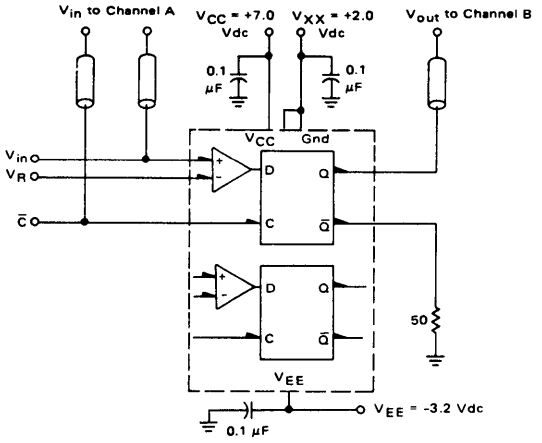


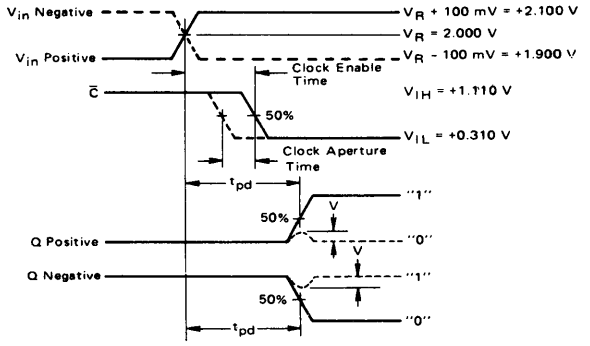
FIGURE 8 – CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

Analog Signal Positive and Negative Slew Case

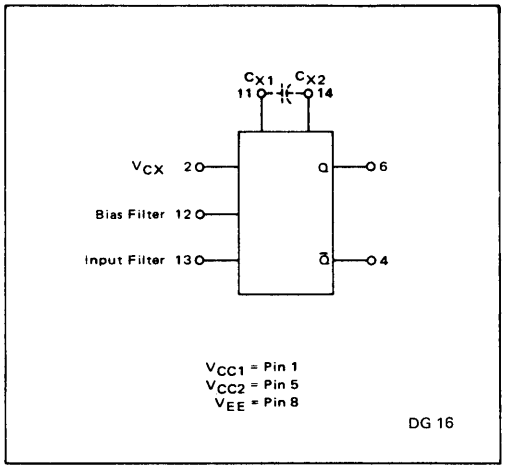


——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

– – – – – – Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

VOLTAGE-CONTROLLED MULTIVIBRATOR

SP1658

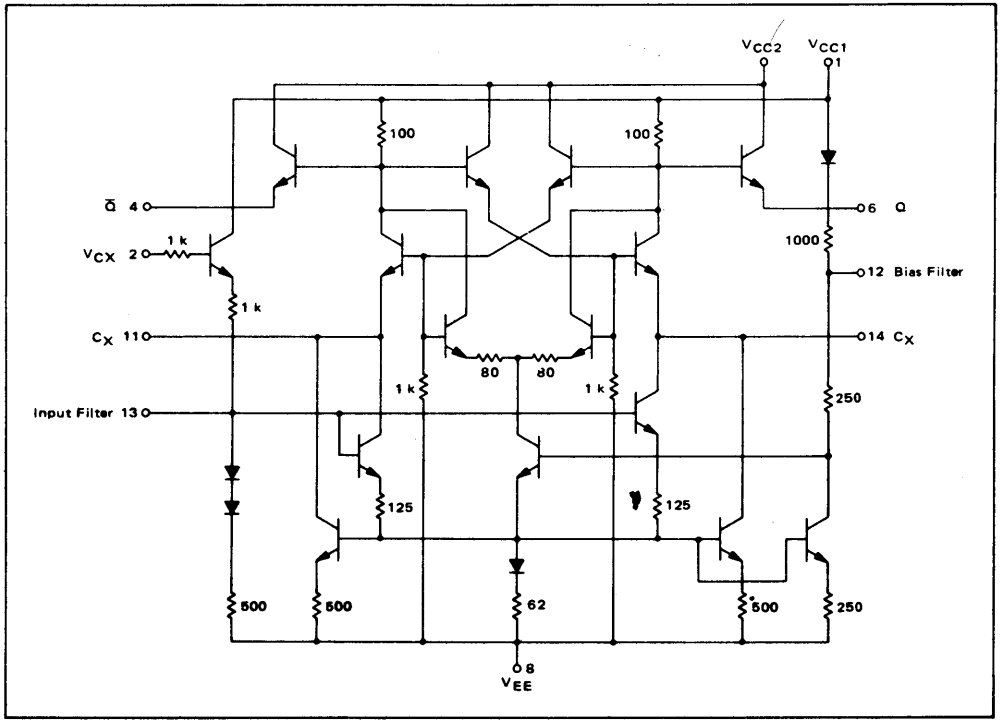


The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with PECL, III and PECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

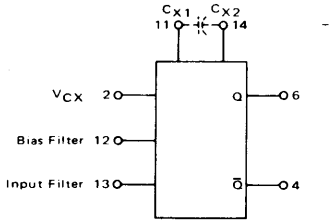
The 'SP1658' is useful in phase-locked loops, frequency synthesizer and clock signal generation applications for instrumentation, communication, and computer systems.

FIGURE 1 – CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.



@ Test Temperature	TEST VOLTAGE VALUES Vdc ±1% V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}
-30°C	0.0	-2.0	-1.0	+2.0	-5.2
+25°C	0.0	-2.0	-1.0	+2.0	-5.2
+85°C	0.0	-2.0	-1.0	+2.0	-5.2

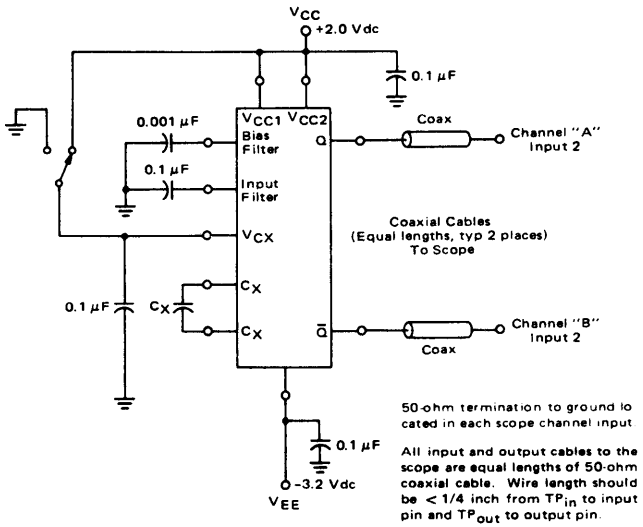
Characteristic	Symbol	Pin Under Test	SP1658 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8*	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
		8**	–	–	–	–	32	–	–	mAdc	2	–	–	–	8	1,5
Input Current	I_{inH}	2*	–	–	–	–	350	–	–	µAdc	2	–	–	–	8	1,5
Input Leakage Current	I_{inL}	2*	–	–	0.5	–	·	–	–	µAdc	–	2	–	–	8	1,5
"Q" High Output Voltage	V_{OH}	4*	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	–	8	1,5
		6**	-1.045	-0.875	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	–	2	–	8	1,5
"Q̄" Low Output Voltage	V_{OL}	4*	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	–	8	1,5
		6**	-1.890	-1.650	-1.850	–	-1.620	-1.830	-1.575	Vdc	–	–	2	–	8	1,5
AC Characteristics (Figure 2) (Tests shown for one output, but checked on both)											C_{X1}	C_{X2}	Gnd		V_{EE} -3.2 V	V_{CC} +2.0 V
Rise Time (10% to 90%)	t+	6	–	2.7	–	1.6	2.7	–	3.0	ns	–	11,14	–	2	8	1,5
Fall Time (10% to 90%)	t-	6	–	2.7	–	1.4	2.7	–	3.0	ns	–	11,14	–	2	2	1,5
Oscillator Frequency	f_{osc1}	–	130	–	130	155	175	110	–	MHz	–	11,14	–		8	1,5
	f_{osc2}	–	–	–	78	90	100	–	–	MHz	11,14	–	–		8	1,5
Tuning Ratio Test 1	TR	–	–	–	3.1	4.5	··	–	–	–	11,14	–	–		8	1,5

*Germanium diode (0.4 drop) forward biased from 11 to 14 (11 → 14).
**Germanium diode (0.4 drop) forward biased from 14 to 11 (11 → 14).

$$1TR = \frac{\text{Output frequency at } V_{CX} = \text{Gnd}}{\text{Output frequency at } V_{CX} = -2.0\ V}$$

C1 = 0.01 µF connected from pin 12 to Gnd.
C2 = 0.001 µF connected from pin 13 to Gnd.
C_{X1} = 10 pF connected from pin 11 to pin 14.
C_{X2} = 5 pF connected from pin 11 to pin 14.

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



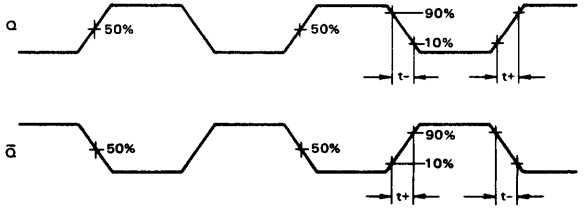


FIGURE 3 – OUTPUT FREQUENCY versus CAPACITANCE FOR VARIOUS VALUES OF INPUT VOLTAGE

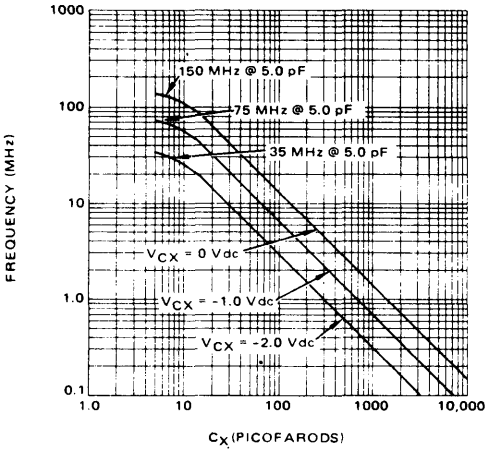


FIGURE 4 – RMS NOISE DEVIATION versus OPERATING FREQUENCY

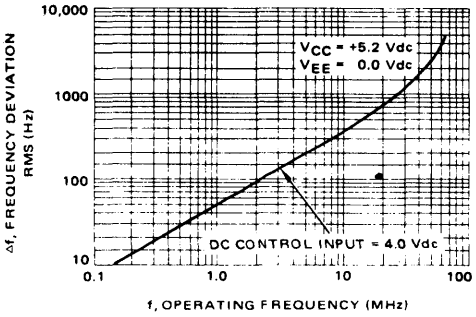
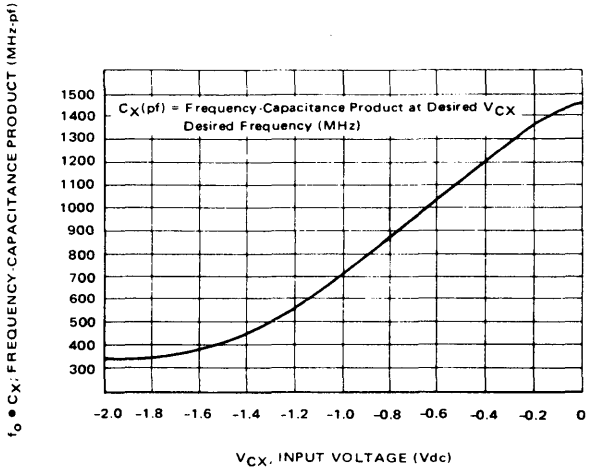


FIGURE 5 – FREQUENCY-CAPACITANCE PRODUCT versus CONTROL VOLTAGE (V_{CX})

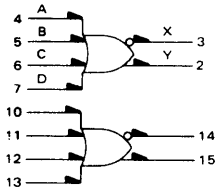


DUAL 4-INPUT GATE

SP1660

SP1660 provides simultaneous OR-NOR or AND-NAND output functions with the capability of driving 50-ohm lines. These devices contain an internal bias reference voltage insuring that the threshold point is always in the center of the transition region over the temperature range (-30° to +85°C). The input pulldown resistors eliminate the need to tie unused inputs to V_{EE}

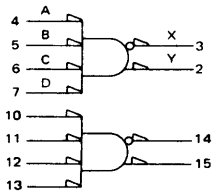
POSITIVE LOGIC



$X = \overline{A + B + C + D}$

$Y = A + B + C + D$

NEGATIVE LOGIC



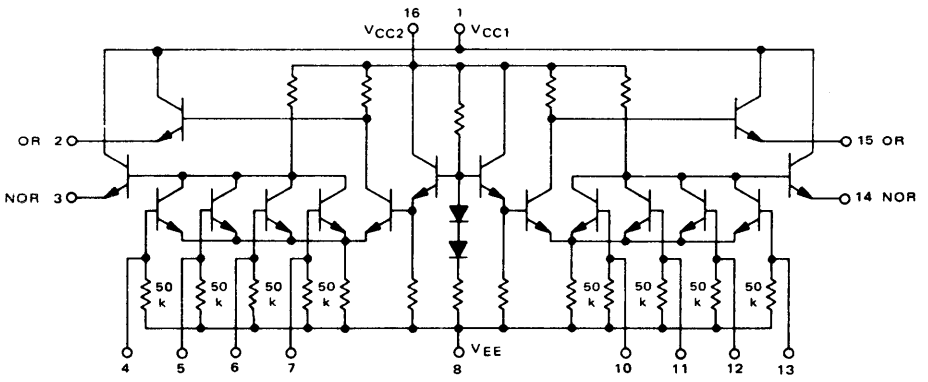
$X = \overline{A \bullet B \bullet C \bullet D}$

$Y = A \bullet B \bullet C \bullet D$

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 120 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

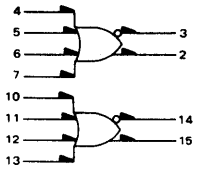
DG 16

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (LIC21 4A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



ϕ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1660 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mAdc	–	–	–	–	8	1,16
Input Current	I_{inH}	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
NOR Logic "1" Output Voltage	V_{OH} ϕ	3	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	– – – –	4 5 6 7	– – – –	– – – –	8	1,16
NOR Logic "0" Output Voltage	V_{OL} ϕ	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4 5 6 7	– – – –	– – – –	– – – –	8	1,16
OR Logic "1" Output Voltage	V_{OH} ϕ	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4 5 6 7	– – – –	– – – –	– – – –	8	1,16
OR Logic "0" Output Voltage	V_{OL} ϕ	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	– – – –	4 5 6 7	– – – –	– – – –	8	1,16
NOR Logic "1" Threshold Voltage	V_{OHA} ϕ	3	-1.065	–	-0.980	–	-0.910	–	Vdc	– – – –	– – – –	– – – –	4 5 6 7	8	1,16
NOR Logic "0" Threshold Voltage	V_{OLA} ϕ	3	–	-1.630	–	-1.600	–	-1.555	Vdc	– – – –	– – – –	4 5 6 7	–	8	1,16
OR Logic "1" Threshold Voltage	V_{OHA} ϕ	2	-1.065	–	-0.980	–	-0.910	–	Vdc	– – – –	– – – –	4 5 6 7	–	8	1,16
OR Logic "0" Threshold Voltage	V_{OLA} ϕ	2	–	-1.630	–	-1.600	–	-1.555	Vdc	– – – –	– – – –	– – – –	4 5 6 7	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+3-}	3	–	1.8	–	1.7	–	1.9	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9			2	–	–		
	t_{4+2+}	2	–	1.6	–	1.5	–	1.7			2	–	–		
	t_{4-3+}	3	–	1.6	–	1.5	–	1.7			3	–	–		
Rise Time	t_{3+}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{3-}	3	–	2.2	–	2.1	–	2.3	ns	4	3	–	–	8	1,16
	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to the input under test.

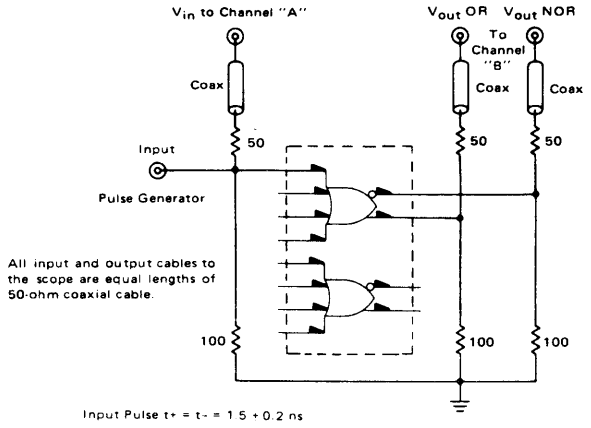
ϕ NOTES

The electrical specifications shown above apply to the SP1660 under the following conditions:

1. The package is housed in a suitable heat sink.†
   or
2. Air is blown transversely over the package. See general information section for more details.

†A suitable heat sink is an IERC LIC21A4A2WCB or equivalent

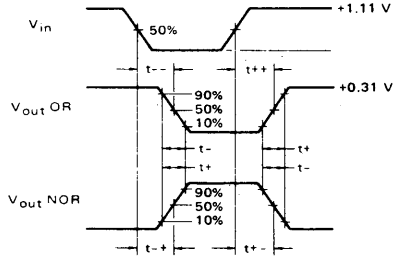
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Input Pulse t+ = t- = 1.5 +0.2 ns

Unused outputs connected to a 50-ohm resistor to ground

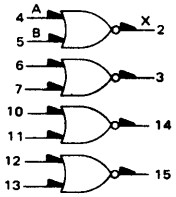
PROPAGATION DELAY



QUAD 2-INPUT "NOR" GATE

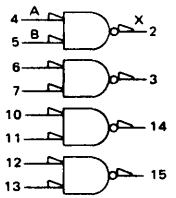
SP1662

POSITIVE LOGIC



$X = \overline{A + B}$

NEGATIVE LOGIC



$X = \overline{A \bullet B}$

Four 2-input NOR or NAND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range (-30 to +85°C).

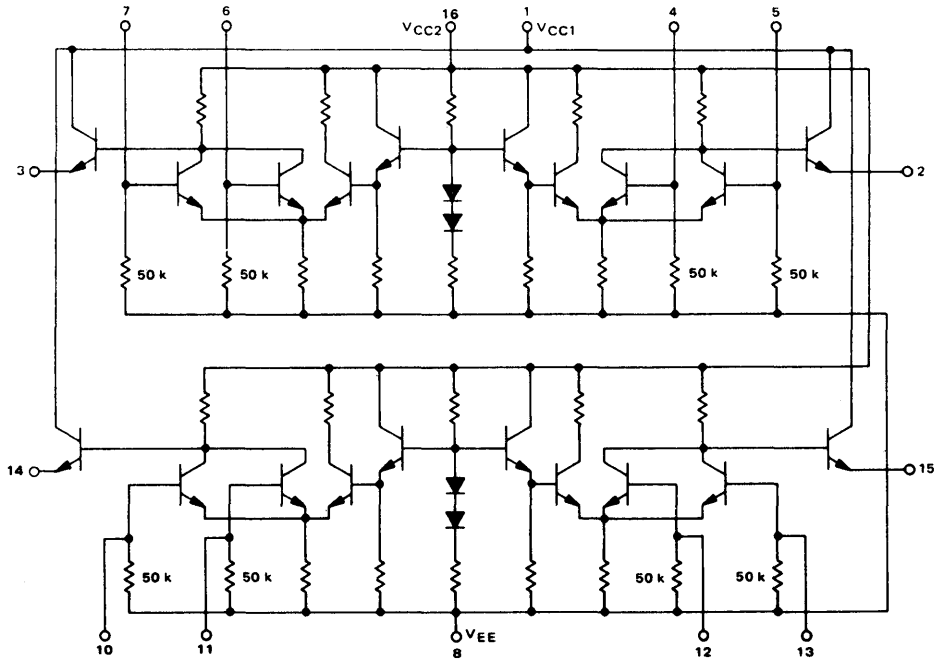
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

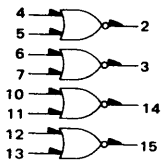
DG 16

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink(IERC-21 4A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

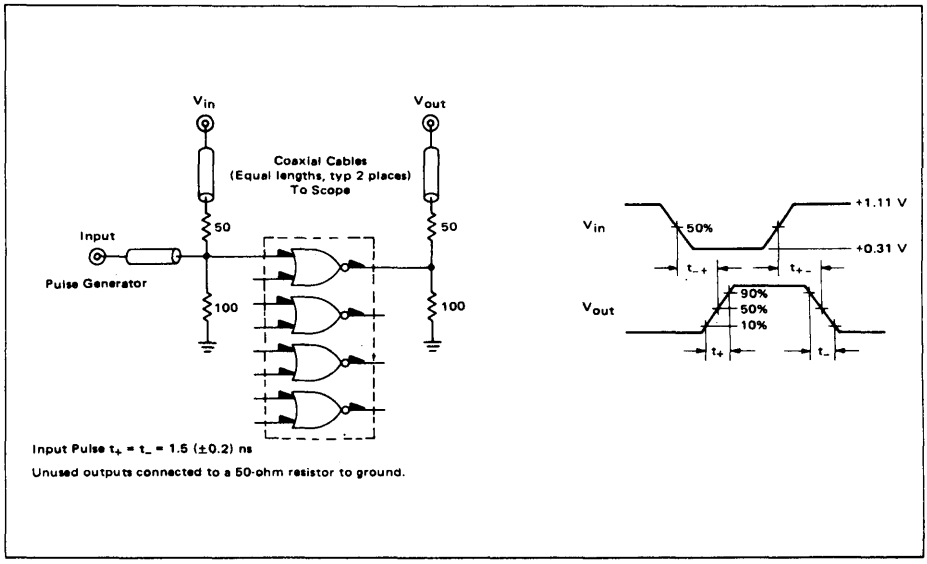


@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1662 Test Limits -30°C Min	-30°C Max *	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	4	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	5	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	–	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	5	–	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	4	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	5	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	4	–	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	–	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	1.6	1.0	1.5	–	1.7	ns	4	2	–	–	8	1,16
	t_{4-2-}	2	–	1.8	1.1	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	1.4	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	1.2	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



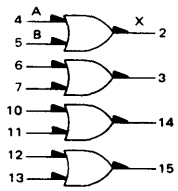
QUAD 2-INPUT "OR" GATE

SP1664

Four 2-input OR or AND gating functions in a single package. An internal bias reference voltage insures that the threshold point remains in the center of the transition region over the temperature range -30 to +85°C.

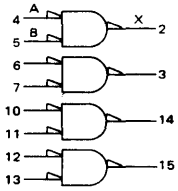
Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



X = A + B

NEGATIVE LOGIC



X = A • B

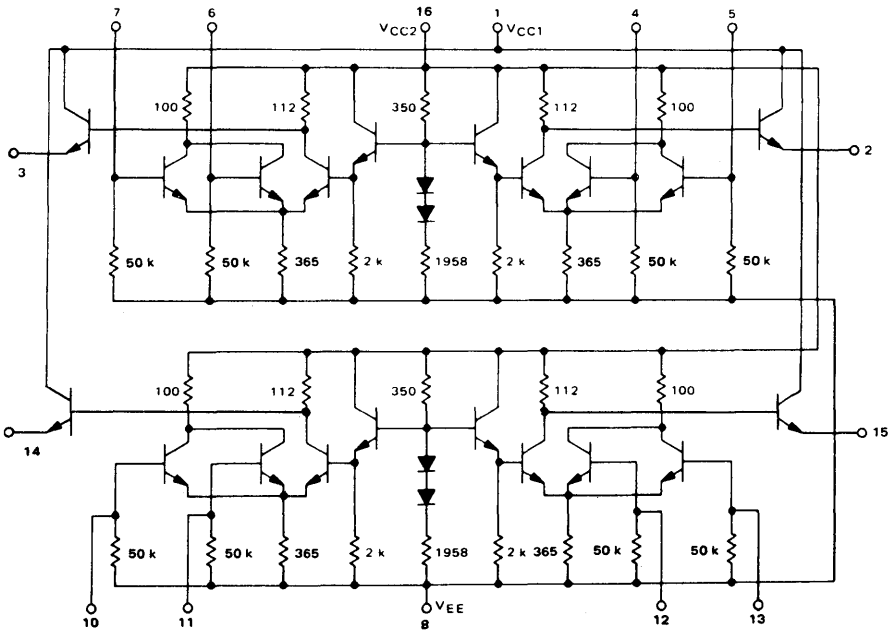
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

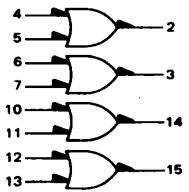
DG 16

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink(IERC-21 4 A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

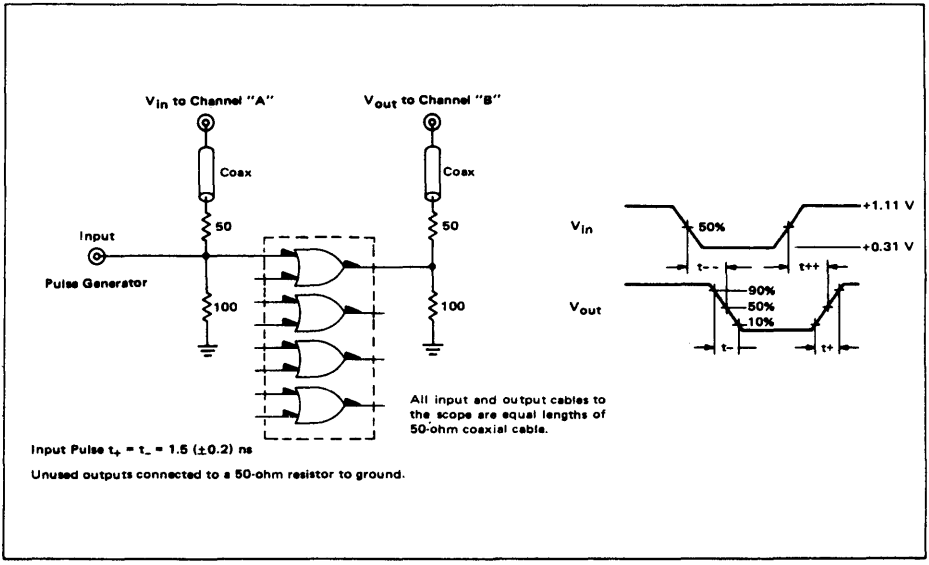


@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.096	-1.485	-5.2
+85°C	-0.700	-1.830	-1.026	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1664 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	56	–	–	mAdc	–	–	–	–	8	1,16
Input Current	$I_{in\,H}$	*	–	–	–	350	–	–	µAdc	*	–	–	–	8	1,16
	$I_{in\,L}$	*	–	–	0.5	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	4	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	–	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	4	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	4	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	5	–	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	4	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	5	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Propagation Delay	t_{4+2+}	2	–	1.6	–	1.5	–	1.7	ns	4	2	–	–	8	1,16
	t_{4-2-}	2	–	1.8	–	1.7	–	1.9	ns	4	2	–	–	8	1,16
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3	ns	4	2	–	–	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



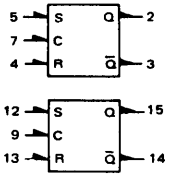
Input Pulse $t_+ = t_- = 1.5$ (±0.2) ns

Unused outputs connected to a 50-ohm resistor to ground.

SP1666

This device consists of two Set-Reset flip-flops in a single package which require a clock input to enable the set-reset inputs. Internal input pull-down resistors eliminate the need to return unused inputs to a negative voltage. The device is useful as a high-speed dual storage element.

POSITIVE LOGIC



t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No Load)

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

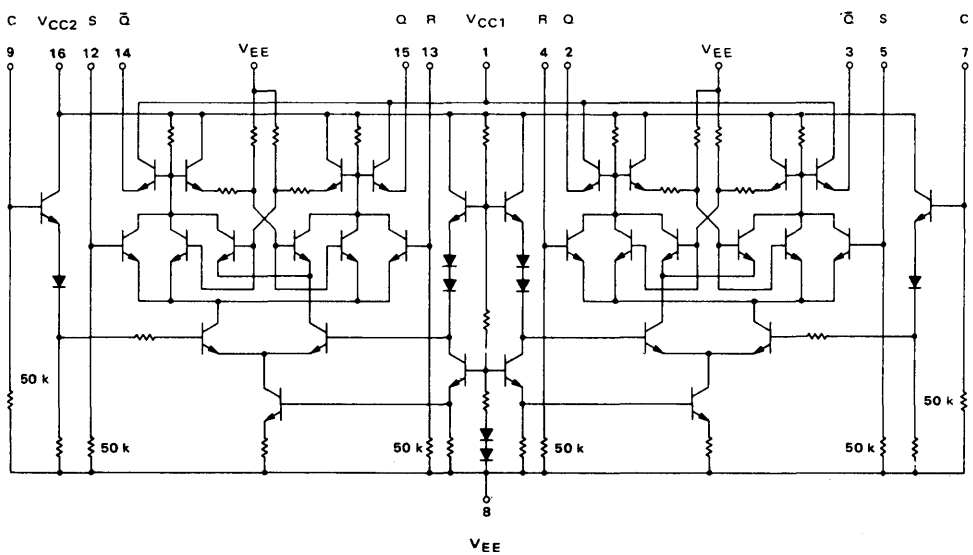
TRUTH TABLE

S	R	C	Q_{n+1}
ϕ	ϕ	0	Q_n
0	0	1	Q_n
1	0	1	1
0	1	1	0
1	1	1	N.D.

ϕ = Don't Care
N.D. = Not Defined

DG 16

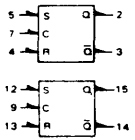
CIRCUIT SCHEMATIC



Numbers at ends of terminals denote pin numbers for L package (Case 620).
Numbers in parenthesis denote pin numbers for F package (Case 650).

ELECTRICAL CHARACTERISTICS

This MECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC 21 4A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

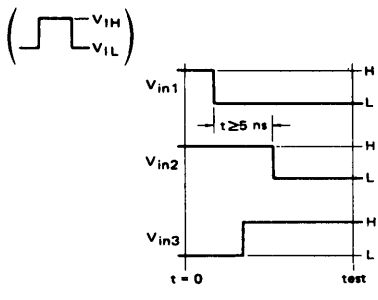


@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1666 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85 Min	+85 Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E ①	8	–	–	–	55	–	–	mAdc	7.9	–	–	–	8	1,16
Input Current	I_{inH}	12	–	–	–	0.370	–	–	mAdc	9,12	–	–	–	8	1,16
		13	–	–	–	0.370	–	–	mAdc	9,13	–	–	–	8	1,16
		9	–	–	–	0.225	–	–	mAdc	9	–	–	–	8	1,16
	I_{inL}	12	–	–	0.500	–	–	–	μAdc	–	12	–	–	8	1,16
		9,13	–	–	0.500	–	–	–	μAdc	–	9,13	–	–	8	1,16
Q Logic "1" Output Voltage	V_{OH}	15 ②	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	13	–	–	8	1,16
		15 ③	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
Q Logic "0" Output Voltage	V_{OL}	15 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	12	–	–	8	1,16
		15 ⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
$\bar{Q}$ Logic "1" Output Voltage	V_{OH}	14 ④	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	12	–	–	8	1,16
		14 ⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
$\bar{Q}$ Logic "0" Output Voltage	V_{OL}	14 ②	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	13	–	–	8	1,16
		14 ③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
Q Logic "1" Output Threshold Voltage	V_{OHA}	15 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	12	13	8	1,16
		15 ⑦	-1.065	–	-0.980	–	-0.910	–	Vdc	–	13	9	–	8	1,16
Q Logic "0" Output Threshold Voltage	V_{OLA}	15 ⑥	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	13	12	8	1,16
$\bar{Q}$ Logic "1" Output Threshold Voltage	V_{OHA}	14 ⑥	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	13	12	8	1,16
$\bar{Q}$ Logic "0" Output Threshold Voltage	V_{OLA}	14 ⑥	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	12	13	8	1,16
		14 ⑦	–	-1.630	–	-1.600	–	-1.555	Vdc	–	13	9	–	8	1,16
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{9+15-}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15	–	–	8	1,16
	t_{9-15-}	15									15	–	–		
	t_{9-14-}	14									14	–	–		
	t_{9+14-}	14									14	–	–		
Set Input	t_{12+15-}	15	1.0	2.5	1.0	2.3	1.1	2.7	ns	12	15	–	–	8	1,16
	t_{12+14-}	14							ns	12	14	–	–	8	1,16
Reset Input	t_{13-14-}	14							ns	13	14	–	–	8	1,16
	t_{13-15+}	15							ns	13	15	–	–	8	1,16
Rise Time	t_+	14,15	0.8	2.8	0.8	2.5	0.9	2.9	ns	9	14,15	–	–	8	1,16
Fall Time	t_-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15	–	–	8	1,16

○ Notes appear on page following Electrical Characteristics tables

NOTES



① I_E is measured with no output pull-down resistors.

② Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to S (V_{IH} to V_{IL})

③ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to S (V_{IH} to V_{IL})

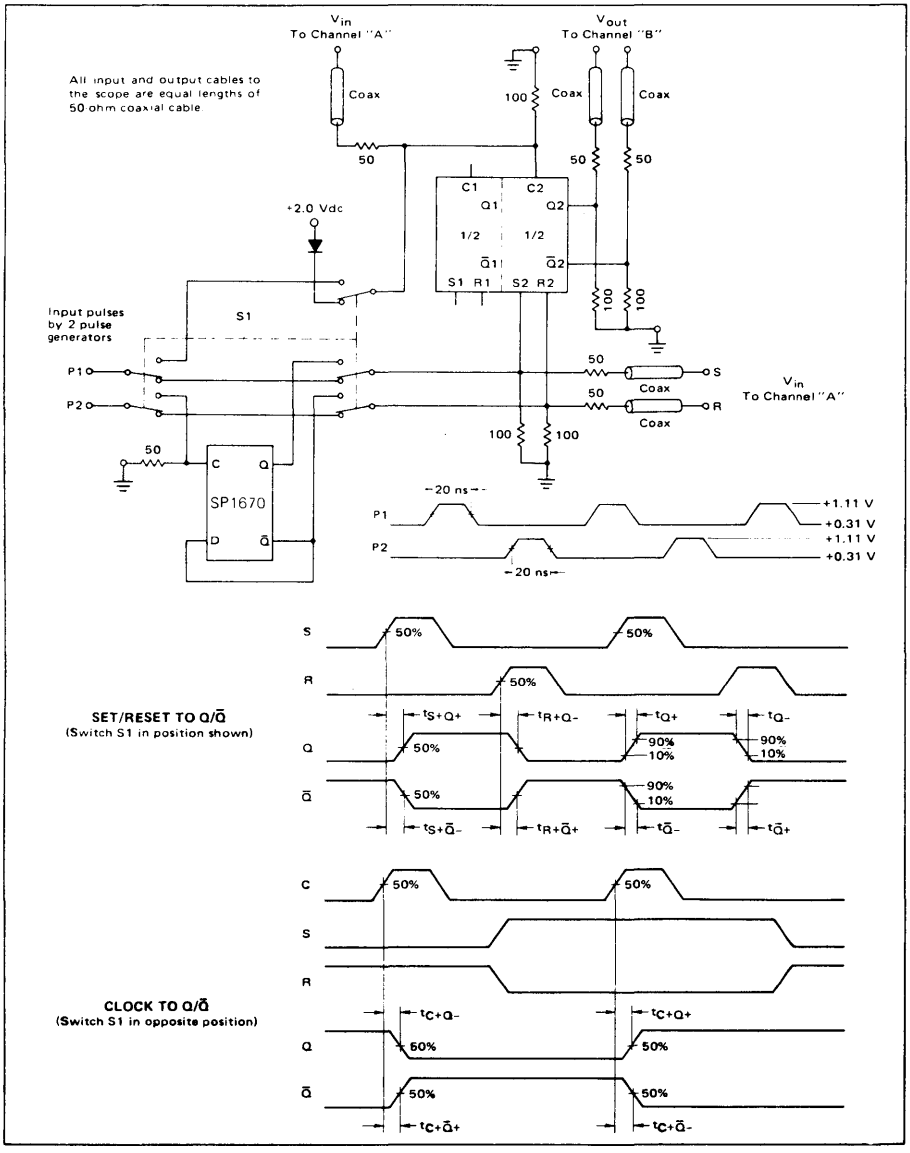
④ Apply Sequentially: V_{in1} to C (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

⑤ Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to R (V_{IH} to V_{IL})

⑥ Apply V_{in3} to C (V_{IH} to V_{IL})

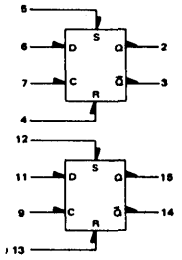
⑦ Apply V_{in3} to S (V_{IH} to V_{IL})

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



SP1668

POSITIVE LOGIC



This device is a Dual Clocked Latch/R-S Flip-Flop. Whenever the Clock is low, the R-S inputs control the output state. Whenever the Clock is high, the output follows the data (D) input.

TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	ϕ	0	Q_n
1	0	ϕ	0	1
0	1	ϕ	0	0
1	1	ϕ	0	**
ϕ	ϕ	0	1	0
ϕ	ϕ	1	1	1

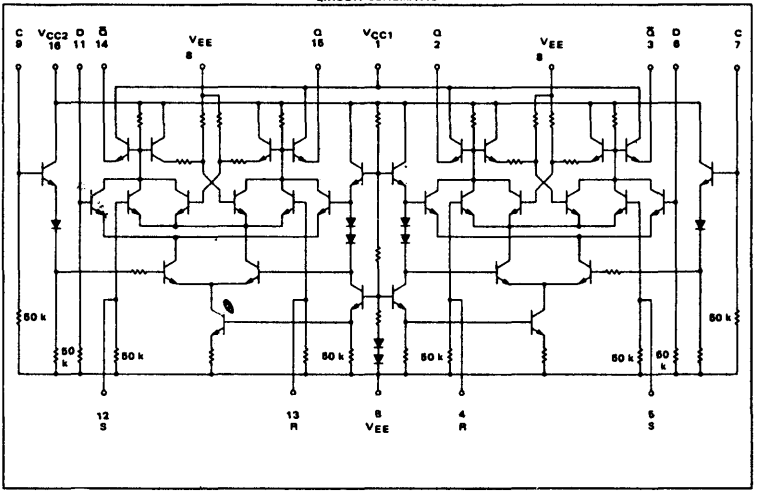
**Output state not defined ϕ = Don't Care

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No load)

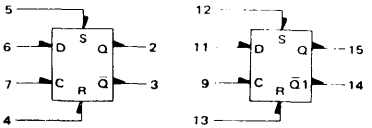
DG 16

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



@Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

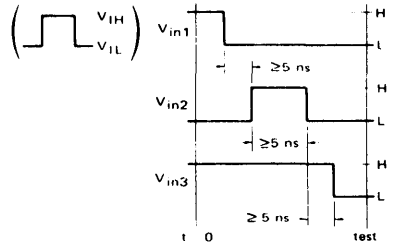
Characteristic	Symbol	Pin Under Test	SP1668 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E (Hi-Z) 1	8			–	55	–	–	mAdc	7,9	–	–	–	8	1,16
Input Current	I_{in} H	11,12,13②			–	0.370	–	–	mAdc	11,12,13	–	–	–	8	1,16
		9		–	–	0.225	–	–	mAdc	9		–	–	8	1,16
	I_{in} L	11,12,13②	–	–	0.500	–		–	μAdc	–	11,12,13	–	–	8	1,16
		9			0.500	–		–	μAdc	–	9	–	–	8	1,16
"Q" Logic "1" Output Voltage	V_{OH}	15 ③	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc		13			8	1,16
		15 ④	-1.045	-0.875	-0.960	-1.810	-0.890	-0.700	Vdc	9	–	–		8	1,16
"Q" Logic "0" Output Logic	V_{OL}	15 ⑤	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	12	–	–	8	1,16
		15 ⑥	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–		8	1,16
"Q̄" Logic "1" Output Voltage	V_{OH}	14 ⑤	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	12	–	–	8	1,16
		14 ⑥	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	9	–	–	–	8	1,16
"Q̄" Logic "0" Output Voltage	V_{OL}	14 ③	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	13	–	–	8	1,16
		14 ④	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	9	–	–	–	8	1,16
"Q" Logic "1" Output Threshold Voltage	V_{OHA}	15	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	12	13	8	1,16
		15 ⑦	↓	–	↓	–	↓	–	↓	–		11	–	↓	↓
		15 ⑤								11		9	–		
"Q" Logic "0" Output Threshold Voltage	V_{OLA}	15	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	13	12	8	1,16
		15 ⑥	–	↓	–	↓	–	↓	↓		–	–	11	↓	↓
		15 ③	–		–		–				11	9	–		
"Q̄" Logic "1" Output Threshold Voltage	V_{OLA}	14	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	13	12	8	1,16
		14 ⑥	↓	–		–	↓	–	↓	–	–	–	11	↓	↓
		14 ③		–		–		–		–	11	9	–		
"Q̄" Logic "0" Output Threshold Voltage	V_{OLA}	14	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	12	13	8	1,16
		14 ⑦	–	↓	–	↓	–	↓	↓	–	–	11	–	↓	↓
		14 ⑤	–		–		–			–	–	9	–		
Switching Times (50 Ω Load)										Pulse In	Pulse Out			-3.2 V	+2.0 V
Clock Input	t_{9+15+}	15	1.0	2.7	1.0	2.5	1.1	2.8	ns	9	15	–	–	8	1,16
	t_{9+15-}	15	↓	↓	↓	↓	↓	↓	↓	↓	15	–	–	↓	↓
	t_{9+14-}	14									14	–	–		
	t_{9+14+}	14									14	–	–		
Rise Time	t_+	14,15	0.8	2.8	0.9	2.5	0.9	2.9	ns	9	14,15	–	–	8	1,16
Fall Time	t_-	14,15	0.5	2.4	0.5	2.2	0.5	2.6	ns	9	14,15	–		8	1,16
Set Input	t_{12+15+}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	15	–	–	8	1,16
	t_{12+14-}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	12	14	–	–	8	1,16
Reset Input	t_{13+14+}	14	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	14	–	–	8	1,16
	t_{13+15-}	15	1.0	2.5	1.1	2.3	1.1	2.7	ns	13	15	–	–	8	1,16

○Notes appear on page following Electrical Characteristics tables.

NOTES

① I_E is measured with no output pulldown resistors.

② Test voltage applied to pin under test.



③ Apply V_{in1} to S (V_{IH} to V_{IL}).

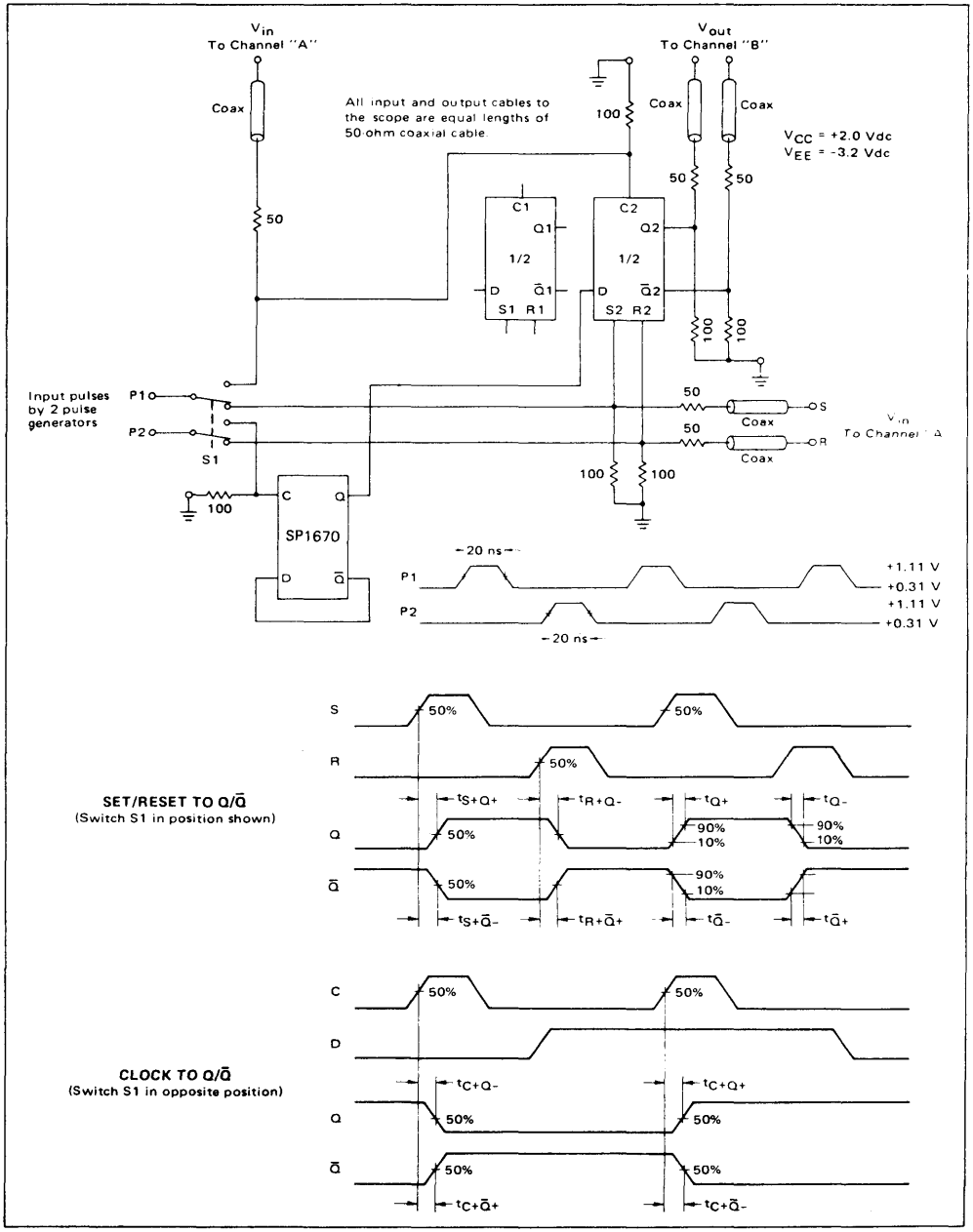
④ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})
V_{in3} to D (V_{IH} to V_{IL})

⑤ Apply V_{in1} to R (V_{IH} to V_{IL})

⑥ Apply Sequentially: V_{in1} to S (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})

⑦ Apply Sequentially: V_{in1} to R (V_{IH} to V_{IL})
V_{in2} to C (V_{IH}, V_{IL})

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS @ 25°C



MASTER-SLAVE
TYPE D FLIP-FLOP

SP1670

The SP1670 is a Type D Master-Slave Flip-Flop designed for use in high speed digital applications. Master slave construction renders the SP1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

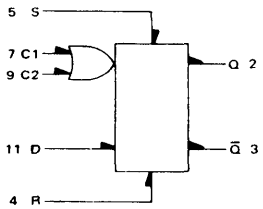
When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

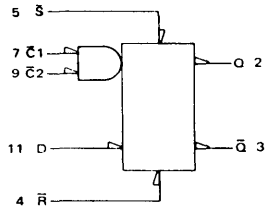
Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



NEGATIVE LOGIC



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

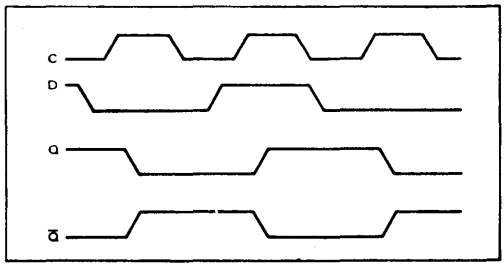
Power Dissipation = 220 mW typical (No Load)
f_{tog} = 350 MHz typ

TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↗	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↗	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
C = C1 + C2

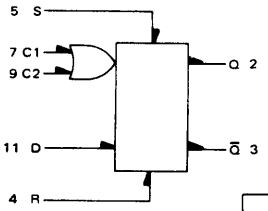
TIMING DIAGRAM



DG 16

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-'2214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

SP 1670 Test Limits

Characteristic	Symbol	Pin Under Test	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	P_1	P_2	P_3	(V_{CC}) Gnd
Power Supply Drain	I_E	8	–	–	–	48		–	mAdc	7,9	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\,H}$	4	–	–	–	550	–	–	μAdc	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–	–		7	–	–	–		–	–	–	
		11				270				11	–	–	–		–	–	–	
	$I_{in\,L}$	4	–	–	0.5	–	–	–	μAdc	9	4	–	–	8	–	–	–	1,16
		5	–	–						9	5				–			
		9	–	–	–	–	–	–		7	9				–			
		7	–	–						9	7				–			
		11	–	–	–	–	–	–		9	11	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc		4,7,11	–	–	8	9	5	–	1,16
		3								11	5,9	–	–		7	4		
		2								11	5,7	–	–		4	9		
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	11	5,7	–	–	8	9	4	–	1,16
		3									4,9,11				7	5		
		2									4,7,11				5	9		
		3								11	5,9				4	7		
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc		4,7,11	–	–	8	9		5	1,16
		3		–		–		–		11	5,9	–			7		4	
		2		–		–		–		11	5,7	–			4	–	9	
		3		–		–		–		–	4,9,11	–			5		7	
		2		–		–		–		–	5,7	11			4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	11	5,7	–	–	8	9		4	1,16
		3									4,9,11				7		5	
		2								–	4,7,11				5		9	
		3								11	5,9				4		7	
		2								–	4,7		11		5	9	–	
		3								–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						-3.2 Vdc				+2.0 Vdc
Clock to Output Delay	t_{7+2+}	9,2	1.0	2.7	1.1	2.5	1.1	2.9	ns	–	–	–	–	8	–	–	–	1,16
(See Figure 1)	t_{7-2-}	9,2								–	–	–	–		–	–	–	
	t_{7+3-}	9,3								–	–	–	–		–	–	–	
	t_{7-3+}	9,3								–	–	–	–		–	–	–	
Set to Output Delay	t_{5+2+}	5,2								–	–	–	–		–	–	–	
(See Figure 2)	t_{5+3-}	5,3								–	–	–	–		–	–	–	
Reset to Output Delay	t_{4+2-}	4,2								–	–	–	–		–	–	–	
(See Figure 2)	t_{4+3+}	4,3								–	–	–	–		–	–	–	
Output Rise Time	$t_{2+,3+}$	2,3	0.9	2.7	1.0	2.5	1.0	2.9		–	–	–	–		–	–	–	
Fall Time	$t_{2-,3-}$	2,3	0.5	2.1	0.6	1.9	0.6	2.3		–	–	–	–		–	–	–	
(See Figure 2)																		
Set Up Time	t_{S}"1"	2		–	–	0.4	–	–		–	6	–	–		–	–	–	
(See Figure 3)	t_{S}"0"	2		–	–	0.5	–	–		–	6	–	–		–	–	–	
Hold Time	t_{H}"1"	2	–		–	0.3	–	–		–	6	–	–		–	–	–	
(See Figure 3)	t_{H}"0"	2	–		–	0.5	–	–		–	6		–		–	–	–	
Toggle Frequency (See Figure 4)	f_{Tog}	2	270		300	–	270	–	MHz	–	–		–		–	–	–	–

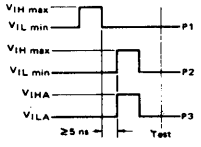


FIGURE 1 – PROPAGATION DELAY TEST CIRCUIT

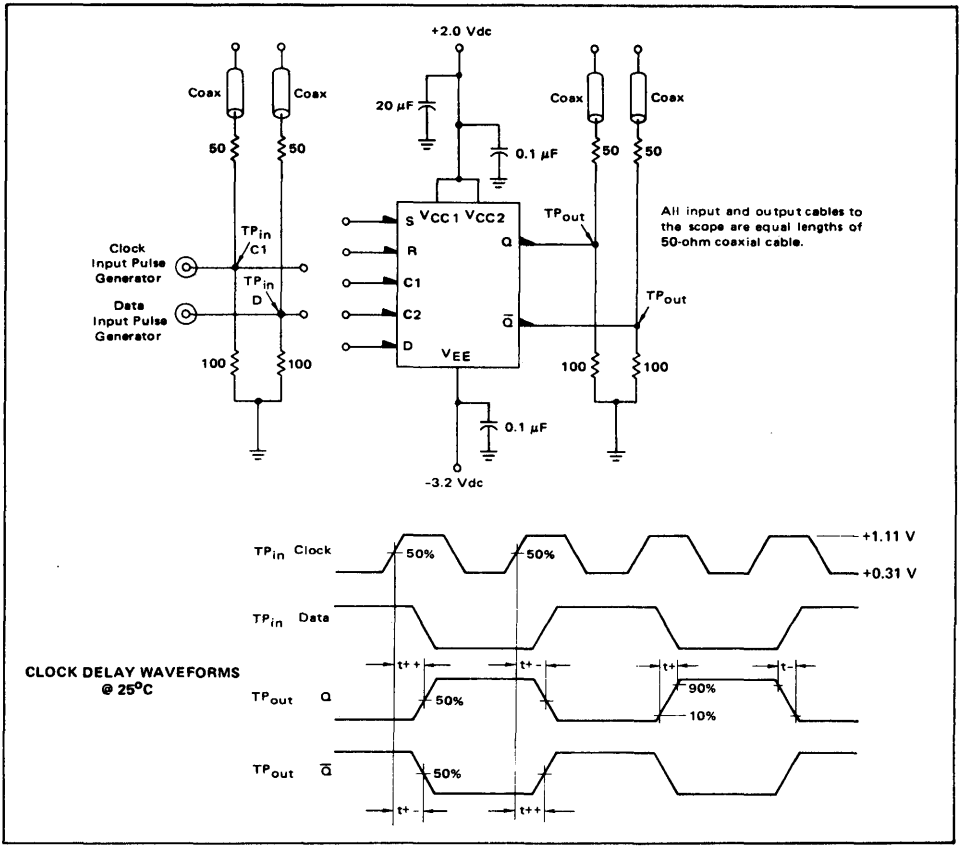


FIGURE 2 – SET-RESET DELAY WAVEFORMS @ 25°C

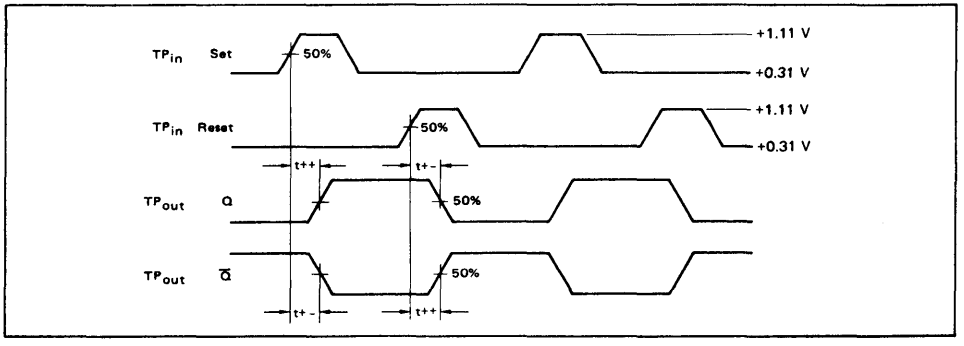
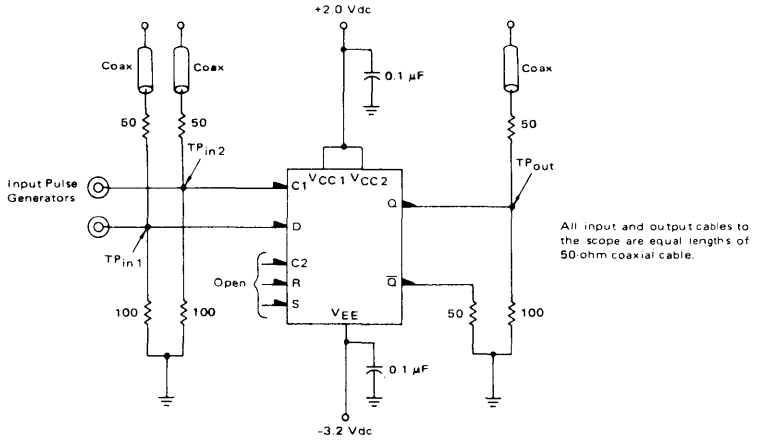
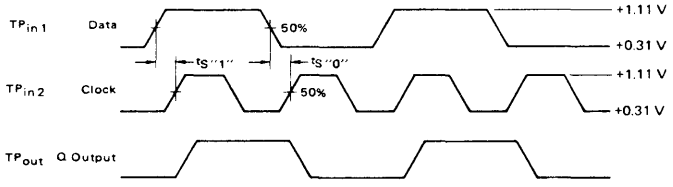


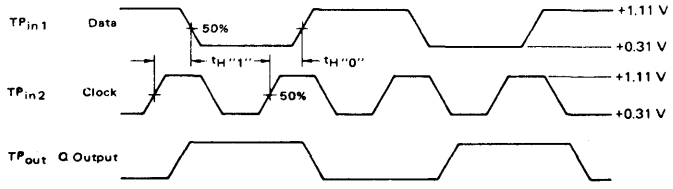
FIGURE 3 – SET UP AND HOLD TIME TEST CIRCUIT



SET UP TIME WAVEFORMS @ 25°C



HOLD TIME WAVEFORMS @ 25°C



Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data (D) input.

FIGURE 4 – TOGGLE FREQUENCY TEST CIRCUIT

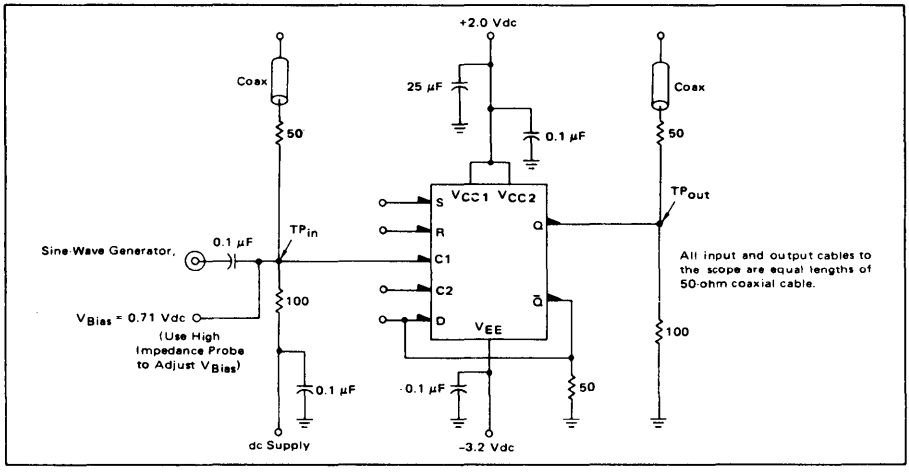


FIGURE 5 – TOGGLE FREQUENCY WAVEFORMS

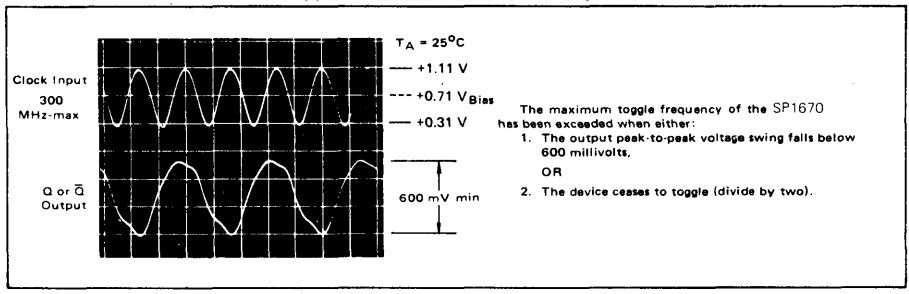


FIGURE 6 – MAXIMUM TOGGLE FREQUENCY (TYPICAL)

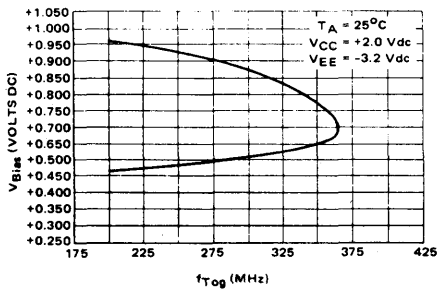
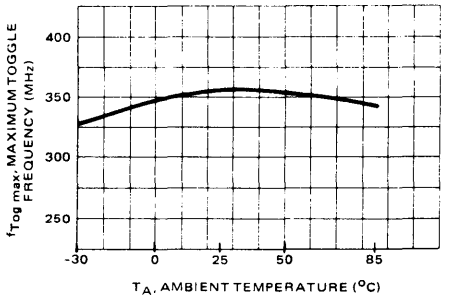


Figure 6 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal. V_{Bias} is defined by the test circuit in Figure 4, and waveform Figure 5.

Figures 8 and 9 illustrate minimum clock pulse width recommended for reliable operation of the SP1670.

FIGURE 7 – TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



Temperature	-30°C	+25°C	+85°C
V_{Bias}	+0.660 Vdc	+0.710 Vdc	+0.765 Vdc

FIGURE 8 – MINIMUM "DOWN TIME" TO CLOCK
OUTPUT LOAD = 50 Ω

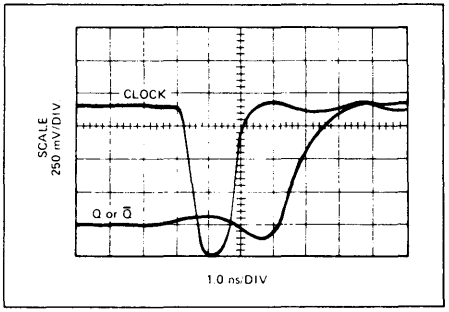
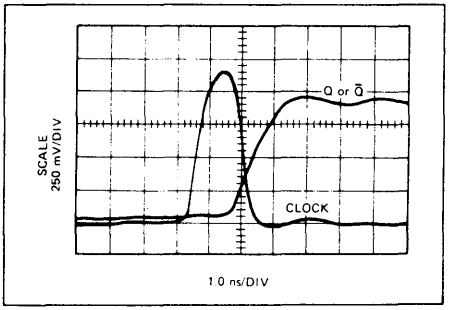


FIGURE 9 – MINIMUM "UP TIME" TO CLOCK
OUTPUT LOAD = 50 Ω



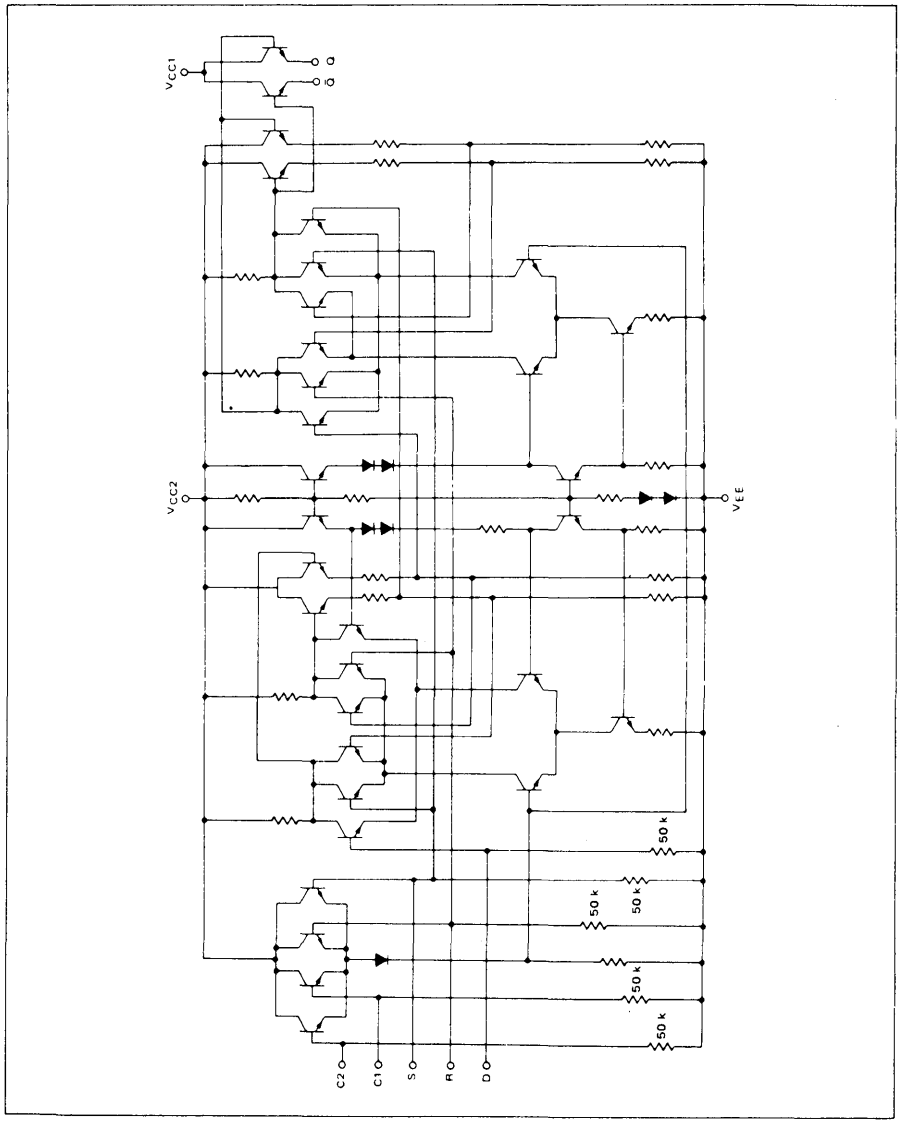


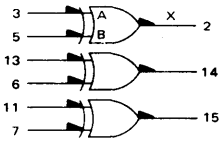
FIGURE 10 – SP1670 CIRCUIT SCHEMATIC

TRIPLE 2-INPUT
EXCLUSIVE-OR GATE

SP1672

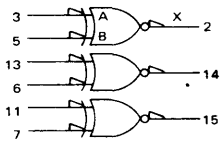
This three gate array is designed to provide the positive logic Exclusive-OR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (-30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

POSITIVE LOGIC



$X = A \bullet \overline{B} + \overline{A} \bullet B$

NEGATIVE LOGIC



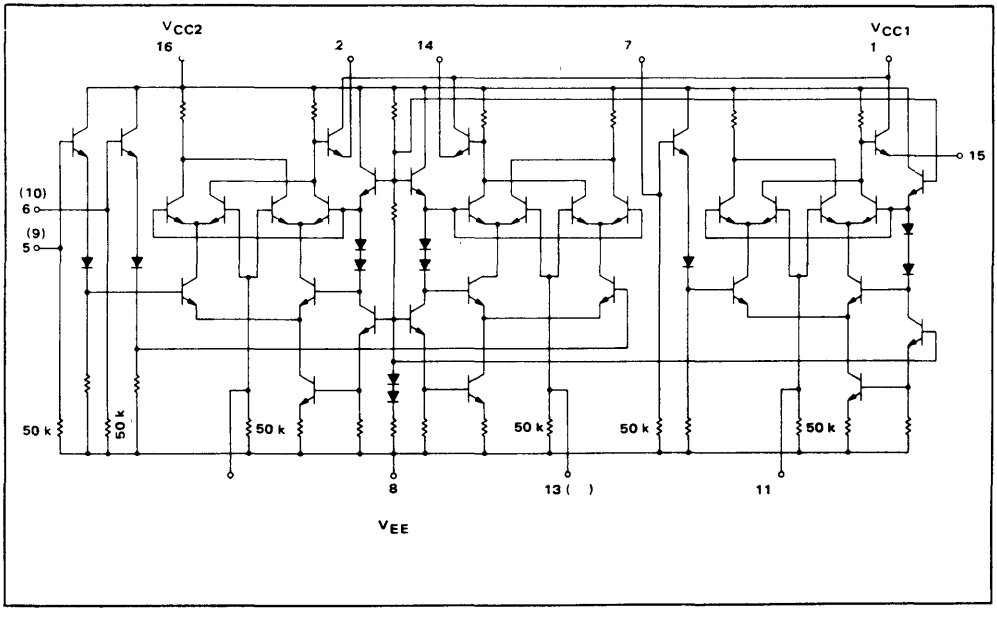
$X = A \bullet B + \overline{A} \bullet \overline{B}$

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = -25 mAdc max

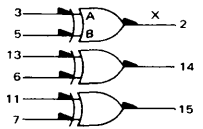
DG 16

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

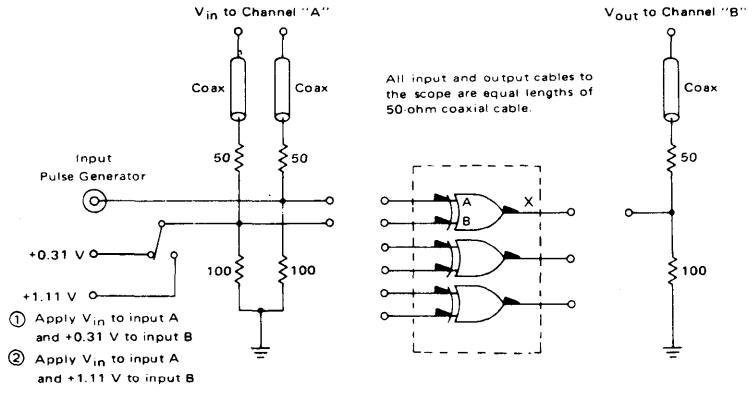


@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

Characteristic	Symbol	Pin Under Test	SP1672 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8				55	–		mAdc	All Inputs		–	–	8	1,16
Input Current	$I_{in\ H}$	3,11,13	–		–	350		–	μAdc	*	–	–	–	8	1,16
	0.75 $I_{in\ H}$	5,6,7	–		–	270	–		μAdc	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–		0.5		–		μAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3	5	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	5	3	–	–	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3,5	–	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	–	3,5	–	–	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	3	5	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	5	3	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	3,5	–	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	–	3,5	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max				Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay	t_{3+2+}	2	–	2.0	–	1.8	–	2.3	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	–	2.0	–	1.8	–	2.3		–	–				
	t_{3+2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{3-2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{5+2+}	2	–	2.5	–	2.3	–	2.8		–	–	5			
	t_{5-2+}	2	–		–		–			–	–				
	t_{5+2-}	2	–		–		–			–	–				
	t_{5-2-}	2	–		–		–			–	–				
Rise Time	t_{2+}	2	–	2.7	–	2.5	–	2.9	ns	–	–	3	2	8	1,16
Fall Time	t_{2-}	2	–	2.4	–	2.2	–	2.6	ns	–	–	3	2	8	1,16

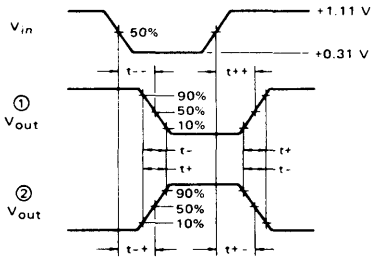
*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



Unused outputs connected to a 50-ohm resistor to ground.

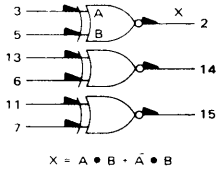
PROPAGATION DELAY



TRIPLE 2-INPUT
EXCLUSIVE-NOR GATE

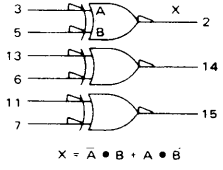
SP1674

POSITIVE LOGIC



$X = A \bullet B + \bar{A} \bullet \bar{B}$

NEGATIVE LOGIC



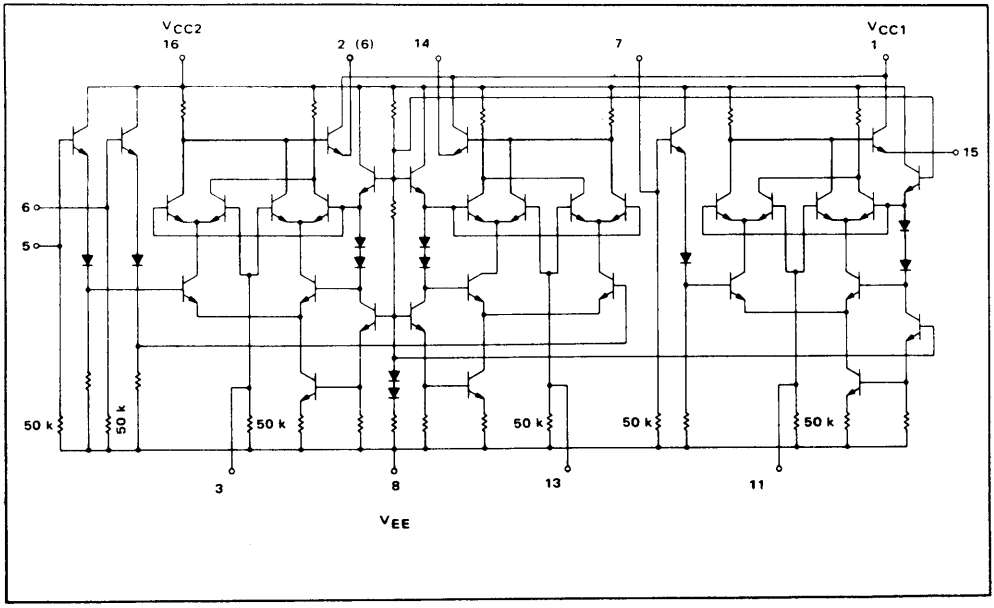
$X = \bar{A} \bullet B + A \bullet \bar{B}$

This three gate array is designed to provide the positive logic Exclusive-NOR function in high speed applications. These devices contain a temperature compensated internal bias which insures that the threshold point remains in the center of the transition region over the temperature range (-30° to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8
t_{pd} = 1.1 ns typ (510-ohm load)
= 1.3 ns typ (50-ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = -25 mAdc max

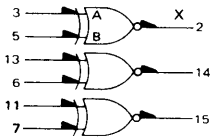
DG 16

CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.

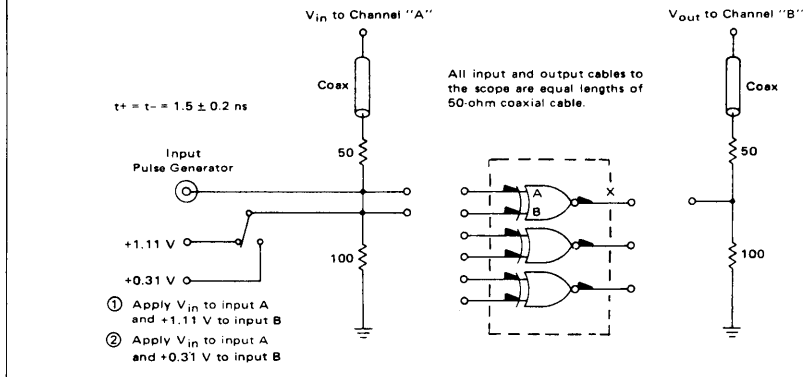


@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	-5.2

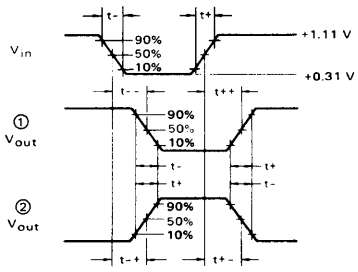
Characteristic	Symbol	Pin Under Test	SP1674. Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	8	–	–	–	55	–	–	mAdc	All Inputs	–	–	–	8	1,16
Input Current	I_{inH}	3,11,13	–	–	–	350	–	–	µAdc	*	–	–	–	8	1,16
	0.75 I_{inH}	5,6,7	–	–	–	270	–	–	µAdc	*	–	–	–	8	1,16
	I_{inL}	*	–	–	0.5	–	–	–	µAdc	–	*	–	–	8	1,16
Logic "1" Output Voltage	$V_{OH\phi}$	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	3,5	–	–	–	8	1,16
		2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	–	3,5	–	–	8	1,16
Logic "0" Output Voltage	$V_{OL\phi}$	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	3	5	–	–	8	1,16
		2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	5	3	–	–	8	1,16
Logic "1" Threshold Voltage	$V_{OHA\phi}$	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	3,5	–	8	1,16
		2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	–	–	3,5	8	1,16
Logic "0" Threshold Voltage	$V_{OLA\phi}$	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	3	5	8	1,16
		2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	–	5	3	8	1,16
Switching Times (50 Ω Load)												Pulse In	Pulse Out		
Propagation Delay	t_{3+2+}	2	–	2.0	–	1.8	–	2.3	ns	–	–	3	2	8	1,16
	t_{3-2+}	2	–	2.0	–	1.8	–	2.3		–	–				
	t_{3t2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{3-2-}	2	–	2.1	–	1.9	–	2.4		–	–				
	t_{5+2+}	2	–	2.5	–	2.3	–	2.8		–	–	5			
	t_{5-2+}	2	–		–		–			–	–				
	t_{5+2-}	2	–		–		–			–	–				
	t_{5-2-}	2	–		–		–			–	–				
Rise Time	t_{6+}	2	–	2.7	–	2.5	–	2.9	ns	–	–	3	2	8	1,16
Fall Time	t_{6-}	2	–	2.4	–	2.2	–	2.6	ns	–	–	3	2	8	1,16

*Individually test each input applying V_{IH} or V_{IL} to input under test.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



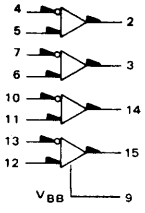
PROPAGATION DELAY



QUAD LINE RECEIVER

SP1692

Four differential amplifiers with emitter followers intended for use in sensing differential signals over long lines.



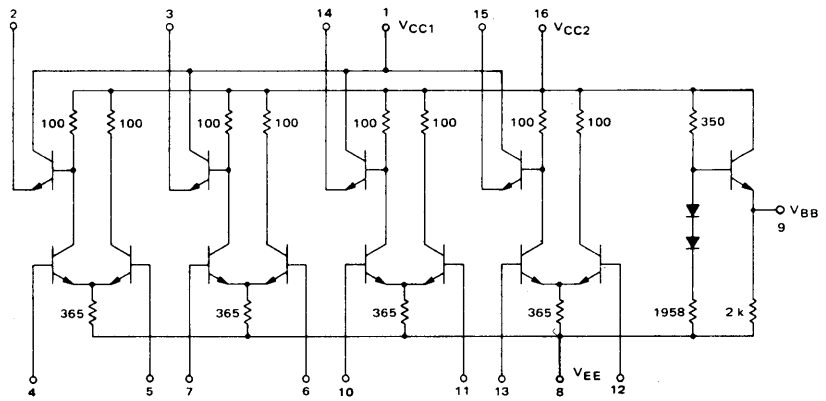
V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 220 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max

DG 16

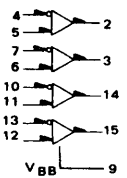
CIRCUIT SCHEMATIC



See General Information section for packaging information.

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink (IERC-LIC-214A2WCB or equivalent) or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or is mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to -2.0 Vdc. See general information section for complete thermal data.



● Test Temperature	TEST VOLTAGE VALUES					
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}
-30°C	-0.875	-1.890	-1.180	-1.515	From Pin 9	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485		-5.2
+85°C	-0.700	-1.830	-1.025	-1.440		-5.2

Characteristic	Symbol	Pin Under Test	SP1692 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{EE}	Gnd
Power Supply Drain Current	I_E	8	–	–	–	50	–	–	mAdc	–	4,7,10,13	–	–	5,6,11,12	8	1,16
Input Current	I_{in}	4	–	–	–	250	–	–	µAdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Input Leakage Current	I_R	4	–	–	–	100	–	–	µAdc	–	7,10,13	–	–	5,6,11,12	8,4	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	7,10,13	4	–	–	5,6,11,12	8	1,16
Logic "0" Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4	7,10,13	–	–	5,6,11,12	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	Vdc	–	7,10,13	–	4	5,6,11,12	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	Vdc	–	7,10,13	4	–	5,6,11,12	8	1,16
Reference Voltage	V_{BB}	9	1.375	1.275	-1.35	-1.25	1.30	1.20	Vdc	–	–	–	–	5,6,11,12	8	1,16
Switching Times (50 Ω Load)			Min	Max	Min	Max	Min	Max		Pulse In		Pulse Out				
Propagation Delay	t_{4-2+}	2	–	1.6	–	1.5	–	1.7	ns	4		2		5,6,11,12	8	1,16
	t_{4+2-}	2	–	1.8	–	1.7	–	1.9								
Rise Time	t_{2+}	2	–	2.2	–	2.1	–	2.3								
Fall Time	t_{2-}	2	–	2.2	–	2.1	–	2.3								

APPLICATIONS INFORMATION

The SP1692 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. The line is driven with a SP1660 OR/NOR gate. The SP1660 is terminated with 50 ohm resistors to -2.0 volts. At the end of the twisted pair a 100 ohm termination resistor is placed across the differential line receiver inputs of the SP1692. Illustrated in Figure 2 is the sending and receiving waveforms at a data rate of 400 megabits per second over an 18 foot twisted pair cable. The waveform picture of Figure 3 shows a 5 nanosecond pulse being propagated down the 18 foot line. The delay time for the line is 1.68 ns/foot.

The SP1692 may also be applied as a high frequency schmitt trigger as illustrated in Figure 4. This circuit has been used in excess of 200 MHz. The SP1692 when loaded into 50 ohms will produce an output rising edge of about 1.5 nanoseconds.

FIGURE 1 – LINE DRIVER/RECEIVER

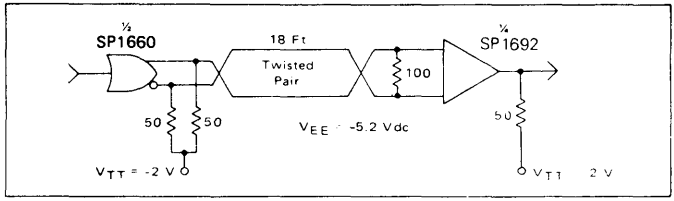


FIGURE 2 – 400 MBS WAVEFORMS

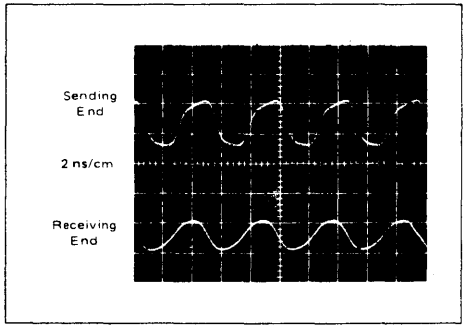
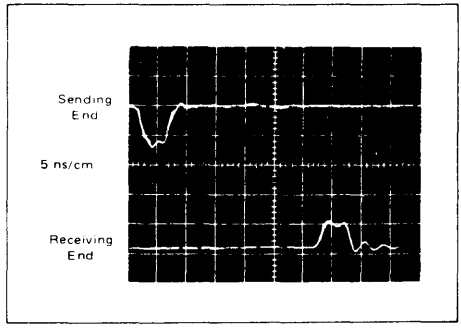


FIGURE 3 – PULSE PROPAGATION WAVEFORMS



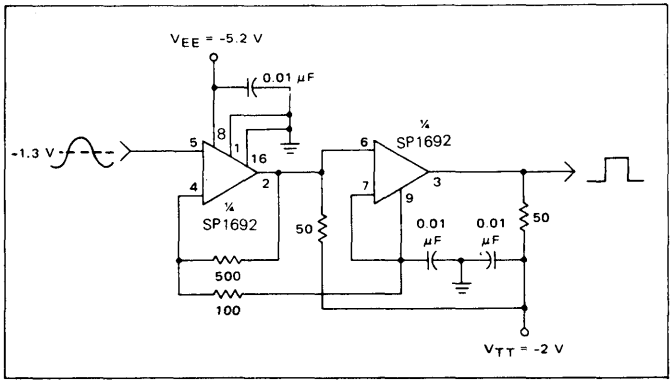


FIGURE 4 – 200 MHz SCHMITT TRIGGER

9. Subnanosecond Logic Data

Plessey Semiconductors
1641 Kaiser Avenue,
Irvine, CA. 92714

SUB-NANOSECOND LOGIC

ADVANCE INFORMATION

SP16F60

DUAL 4-INPUT OR/NOR GATE

SP16F60 provides simultaneous OR-NOR output functions with the capability of driving 50 Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (—30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

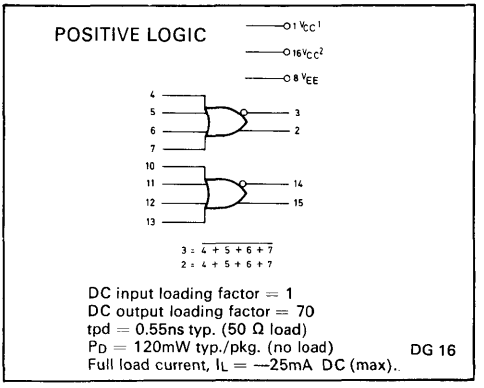


Fig. 1 Logic diagram

FEATURES

- Gate Switching Speed 550ps Typ.
- ECL III and ECL 10K Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation
- Pin and Power Compatible with SP1660

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems
- Nucleonics

ABSOLUTE MAXIMUM RATINGS

Power supply voltage | Vcc - VEE |	8V
Base input voltage	OV to VEE
O/P source current	<40mA
Storage temperature	—55°C to +150°C
Junction operating temperature	< +125C

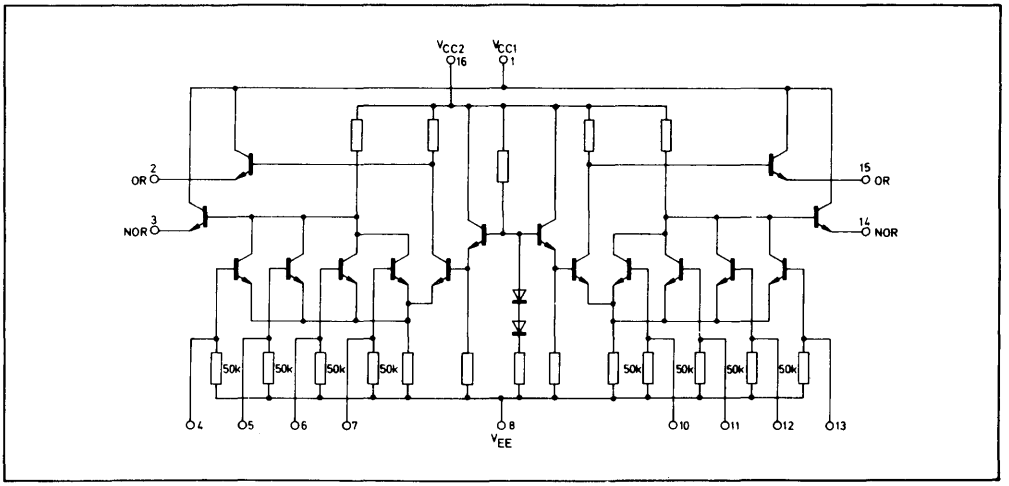


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equiblirium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50-ohm resistor to −2.0 Vdc.

@ Test Temperature	TEST VOLTAGE VALUES (V)				
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
-30°C	−0.875	−1.890	−1.180	−1.515	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+85°C	-0.700	−1.830	−1.025	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	SP16F60 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Units	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	V_{CC} (Gnd)
Power Supply Drain Current	I_E	8	–	–	–	28	–	–	mA	–	–	–	–	8	1,16
Input Current	$I_{in\ H}$	*	–	–	–	350	–	–	μA	*	–	–	–	8	1,16
	$I_{in\ L}$	*	–	–	0.5	–	–	–	μA	–	*	–	–	8	1,16
NOR Logic 1 Output Voltage	V_{OH}	3	-1.045	-0.875	-0.960	-0.810	-1.890	-0.700	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 0 Output Voltage	V_{OL}	3	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 1 Output Voltage	V_{OH}	2	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	V	4	–	–	–	8	1,16
										5	–	–	–		
										6	–	–	–		
										7	–	–	–		
OR Logic 0 Output Voltage	V_{OL}	2	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	V	–	4	–	–	8	1,16
										–	5	–	–		
										–	6	–	–		
										–	7	–	–		
NOR Logic 1 Threshold Voltage	V_{OHA}	3	-1.065	–	-0.980	–	-0.910	–	V	–	–	–	4	8	1,16
				–		–		–		–	–	–	5		
				–		–		–		–	–	–	6		
				–		–		–		–	–	–	7		
NOR Logic 0 Threshold Voltage	V_{OLA}	3	–	-1.630	–	-1.600	–	-1.555	V	–	–	4	–	8	1,16
			–		–		–			–	–	5	–		
			–		–		–			–	–	6	–		
			–		–		–			–	–	7	–		
OR Logic 1 Threshold Voltage	V_{OHA}	2	-1.065	–	-0.980	–	-0.910	–	V	–	–	4	–	8	1,16
				–		–		–		–	–	5	–		
				–		–		–		–	–	6	–		
				–		–		–		–	–	7	–		
OR Logic 0 Threshold Voltage	V_{OLA}	2	–	-1.630	–	-1.600	–	-1.555	V	–	–	–	4	8	1,16
			–		–		–			–	–	–	5		
			–		–		–			–	–	–	6		
			–		–		–			–	–	–	7		
Switching Times (50Ω Load)			Typ	Max	Typ	Max	Typ	Max		Pulse In	Pulse Out			-3.2V	+2.0V
Propagation Delay	t_{4+3-}	3	–	–	0.55	0.8	–	–	ns	4	3	–	–	8	1,16
	t_{4-2-}	2	–	–			–	–			2	–	–		
	t_{4+2+}	2	–	–			–	–			2	–	–		
	t_{4-3+}	3	–	–			–	–			3	–	–		
Rise Time 20% to 80%	t_{3+}	3	1.5	2.1	0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2+}	2	1.5	2.1	0.35	0.6	–	–	ns	4	2	–	–	8	1,16
Fall Time 20% to 80%	t_{3-}	3	1.4	2.1	0.4	0.6	–	–	ns	4	3	–	–	8	1,16
	t_{2-}	2	1.4	2.1	0.35	0.6	–	–	ns	4	2	–	–	8	1,16

* Individually test each input applying V_{IH} or V_{IL} to the input under test.

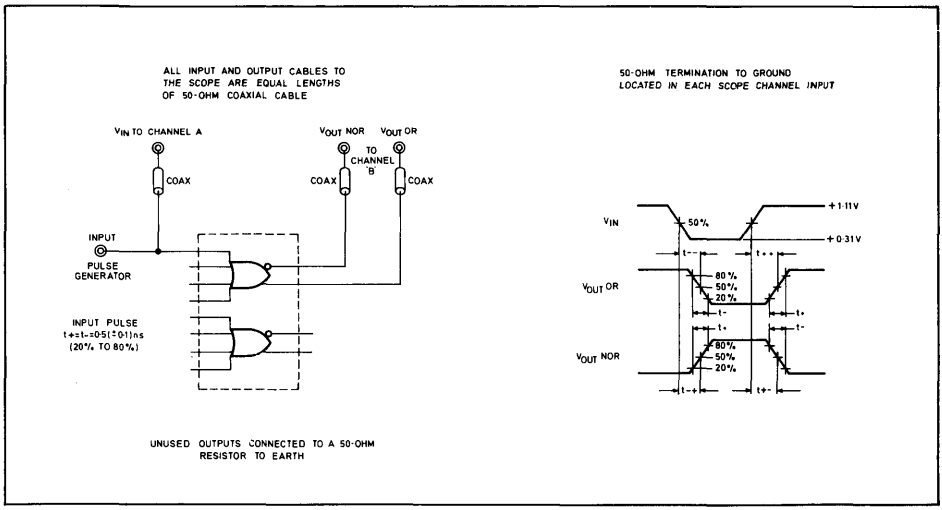


Fig. 3 Switching time test circuit and waveforms at +25°C

SP9131

550 MHz DUAL TYPE D MASTER SLAVE FLIP-FLOP

The **SP9131** is a dual master slave type D flip-flop which is pin-for-pin compatible with the **SP9131**, but with improved dynamic performance and increased power dissipation.

R-S TRUTH TABLE

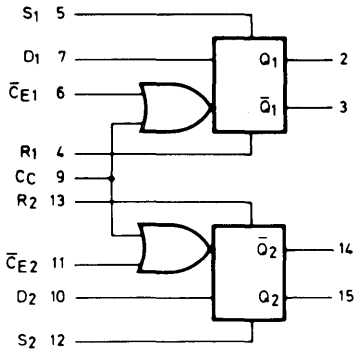
R	S	$Q_n - 1$
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

CLOCKED TRUTH TABLE

C	D	$Q_n - 1$
L	ø	Q_n
H	L	L
H	H	H

ø = Don't Care
$C = \overline{C_E} + C_C$.
A clock H is a clock transition from a low to a high state.

P_D = 364mW
f_{TOG} = 550 MHz (typ)



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

DG 16

Fig. 1 Logic diagram

ELECTRICAL CHARACTERISTICS

This series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

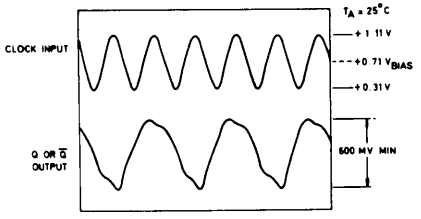
" Test Temperature	TEST VOLTAGE VALUES (Volts)				
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°C	−0.89	−1.89	−1.205	−1.500	−5.2
25°C	−0.81	−1.85	−1.105	−1.475	−5.2
85°C	−0.70	−1.825	−1.035	−1.44	−5.2

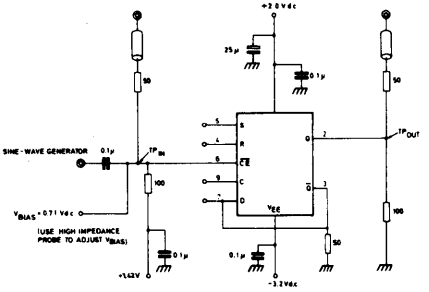
Characteristic	Symbol	Pin Under Test	SP10S131 Test Limits −30 C Min	−30 C Max	25°C Min	25°C Typ	25°C Max	+85 C Min	+85 C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(Vcc) Gnd
Power Supply Drain Current	I_E	8	—	—	—	45	56	—	—	mAdc	—	—	—	—	8	1.16
Input Current	I_{inH}	4	—	—	—		330	—	—	µAdc	4	—	—	—	8	1.16
		5	—	—	—	—	330	—	—		5	—	—	—		
		6	—	—	—		220	—	—		6	—	—	—		
		7	—	—	—	—	245	—	—		7	—	—	—		
		9	—	—	—	—	265	—	—		9	—	—	—		
Input Leakage Current	I_{inL}	4,5,*	—	—	0.5	—	—	—	—	µAdc	—	—	—	—	8	1.16
		6,7,9*	—	—	0.5	—	—	—	—	µAdc	—	—	—	—	8	1.16
Logic "1" Output Voltage	V_{OH}	2	-1.06	-0.89	-0.96	—	-0.81	-0.89	-0.70	Vdc	5	—	—	—	8	1.16
		2	-1.06	-0.89	-0.96	—	-0.81	-0.89	-0.70	Vdc	7	—	—	—	8	1.16
Logic "0" Output Voltage	V_{OL}	3	-1.89	-1.675	-1.85	—	-1.65	-1.825	-1.615	Vdc	5	—	—	—	8	1.16
		3	-1.89	-1.675	-1.85	—	-1.65	-1.825	-1.615	Vdc	7	—	—	—	8	1.16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.08	—	-0.98	—	—	-0.91	—	Vdc	—	—	5	—	8	1.16
		2	-1.08	—	-0.98	—	—	-0.91	—	Vdc	—	—	7	9	8	1.16
Logic "0" Threshold Voltage	V_{OLA}	3	—	-1.655	—	—	-1.63	—	-1.595	Vdc	—	—	5	—	8	1.16
		3	—	-1.655	—	—	-1.63	—	-1.595	Vdc	—	—	7	9	8	1.16
Switching Times Clock Input											-1.11 Vdc		Pulse In	Pulse Out	-3.2Vdc	-2.0Vdc
Propagation Delay	t_{9-2-}	2	—	—		1.3		—	—	ns	—	—	9	2	8	1.16
	t_{9-2+}	2	—	—				—	—		7	—	9	2		
	t_{6-2+}	2	—	—				—	—		7	—	6	2		
	t_{6-2-}	2	—	—				—	—		—	—	6	2		
Rise Time (20 to 80%)	t_{2+}	2	—	—		2.0		—	—		7	—	9	2		
Fall Time (20 to 80%)	t_{2-}	2	—	—		1.3		—	—		—	—	9	2		
Set Input Propagation Delay	t_{5-2-}	2	—	—		1.5		—	—	ns	—	—	5	2	8	1.16
	t_{12-15-}	15	—	—				—	—		6	—	12	15		
	t_{5-3-}	3	—	—				—	—		—	—	5	3		
	t_{12-14-}	14	—	—				—	—		9	—	12	14		
Reset Input Propagation Delay	t_{4-2-}	2	—	—		1.5		—	—	ns	—	—	4	2	8	1.16
	t_{13-15-}	15	—	—				—	—		6	—	13	15		
	t_{4-3-}	3	—	—				—	—		—	—	4	3		
	t_{13-14-}	14	—	—				—	—		9	—	13	14		
Setup Time	t_{setup}	7	—	—		—	1.3	—	—	ns	—	—	6.7	2	8	1.16
Hold Time	t_{hold}	7	—	—		—	0.4	—	—	ns	—	—	6.7	2	8	1.16
Toggle Frequency (Max)	f_{Tog}	2	—	—		400	—	—	—	MHz	—	—	6	2	8	1.16

*Individually test each input; apply V_{IL} min to pin under test.

Output level to be measured after a clock pulse has been applied to the C_E input (pin 6) $\sqcap_{V_{IL\ min}}^{-V_{IH\ max}}$

This is advance information and specifications are subject to change without notice.

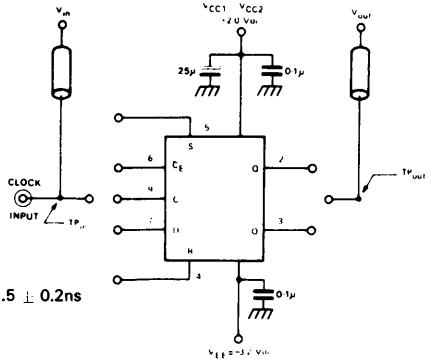




50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.

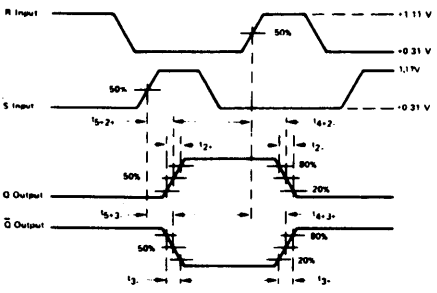
Fig. 2 Toggle frequency test circuit

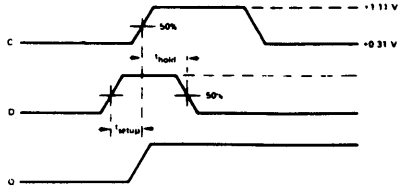


Input Pulse
$t_+ = t_- = 1.5 \pm 0.2$ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.





NOTE:
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).
t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

Fig. 3 Switching time test circuit and waveforms at +25°C

ECL Gate Arrays

LA1000 Uncommitted Logic Array – 36-Cell

* 75–gate approx. equivalent
* 0.55 nsec (0.4) OR/NOR gate delay
* 0.75 nsec (0.5) OR–AND–INV gate delay
* 500 MHz (900) D–type toggle frequency
* 1 Watt max. power dissipation
* 24 input/output pins

LA 2000 Uncommitted Logic Array – 144-Cell

* 300–gate approx. equivalent
* 0.55 nsec (0.4) OR/NOR gate delay
* 0.75 nsec (9.5) OR–AND–INV gate delay
* 500 MHz (900) D–type toggle frequency
* 4 Watts max. power dissipation
* 36 input pins, 20 input/output pins

LA 3000 Uncommitted Logic Array – 144-Cell

* 300–gate approx. equivalent
* 3.0 nsec OR/NOR gate delay
* 5.0 nsec OR–AND–INV gate delay
* 100 MHz D–type toggle frequency
* 1 Watt max. power dissipation
* 36 input pins, 20 input/output pins

SUBNANOSECOND ECL GATE ARRAY

A Gate array, sometimes also referred to as an uncommitted logic array (U.L.A.) or a masterslice, is an integrated circuit that consists of a regular pattern of identical groups of components or cells. The interconnection of these components and cells is determined by the customer, and a special mask (or masks) is designed to perform his function. The cells are not necessarily committed to logic functions, but may in some cases be connected to form simple linear functions.

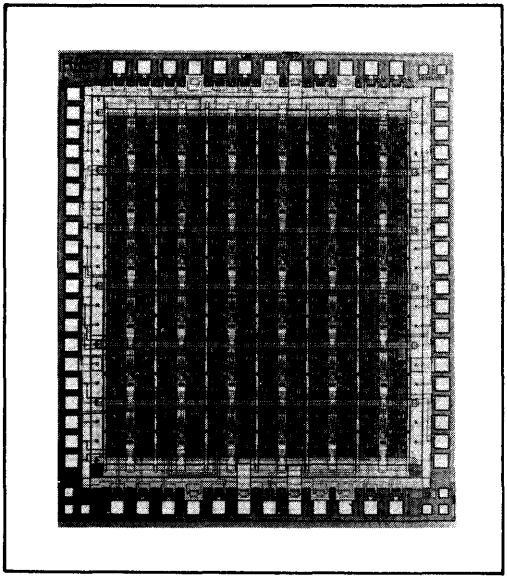
Gate Arrays have been developed in a variety of technologies, both MOS and bipolar. A number of different circuit techniques have also been used (e.g. Integrated Injection Logic (I2L), Resistor Transistor Logic (RTL), Emitter Coupled Logic (ECL) etc.). Whilst these products are clearly aimed at different market areas, the basic principles are the same, i.e. it is a technique which offers:–

1. Low cost
2. Low risk
3. Quick turnround time

The resulting L.S.I. devices exhibit only a marginal reduction in performance and some increase in silicon area over a full custom circuit.

The Plessey ECL Gate Array Family

These arrays are based on the use of uncommitted ECL 2 input OR–NOR gates..



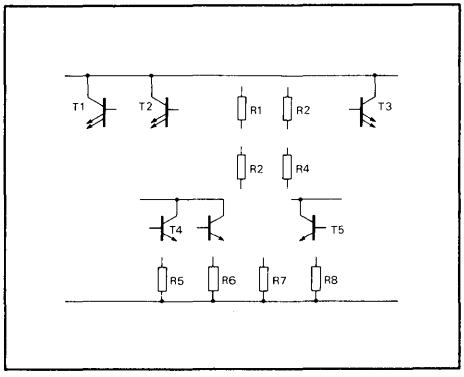


Figure 1 MSI ULA Cell Components

These circuits make up the current family. Th one shown (ULA 2000) contains 144 of the cells above. Gate delays are typically 500 picosecon and D–type flip flop clock frequencies in excess of 400 MHz.

ULA1000, 2000 and 3000

To satisfy the demand for ever higher performance and increased cost effectiveness in a variety of system fields such as computation, instrumentation and communications, a range of ULA devices offering the ultimate in performance has been developed. Each of these contains a number of the cells shown on the previous page. The six size and performance of the numbers of this family are as follows:–

	Cell Count	Gate Delay	Maximum Power Dissipation
ULA 1000	36	500 psecs	900mW
ULA 2000	144	500 psecs	3.5 Watts
ULA 3000	144	2.0 nsecs	750mW

Slices containing all the relevant diffusions and contact windows are held in stock and only the three metallisation layers (2 metal and 1 via) are required to produce a new variant.

CIRCUIT ORGANISATION

The basic gate can be operated with either a full ECL logic swing (850 mVolts) or a reduced swing (500 mVolts). The cell output transistor can be connected as required to either the OR or NOR load resistor. Two current source resistors are provided within the cell which are used as the pull–down resistors connected to the bases of input transistors.

A major cell is built up of four such minor cells together with an associated reference voltage supply Two layers of metallisation are used for power supply distribution and cell inter–connections. Although the function of the minor cell is nominally that of a two–input OR–NOR gate, the fact that all components are uncommitted within the cell means that standard custom design ECL logic techniques may be employed to increase the logic capability of the circuits. Emitter dotting may be performed on any of the six emitter follower outputs and collector dotting may also be performed; in this case one of the available emitter follower transistors is used as a diode clamp. In this way the wire–or and wire–and functions are realised and the overall logical power of the array is increased considerably; gate equivalents of up to 75 gates can be realised on ULA 1000 and 300 gates on ULA 2000 and 3000.

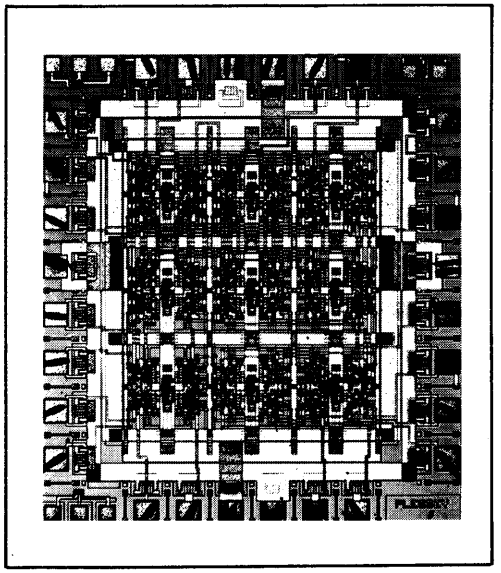


Figure 2 MSI ULA Chip Photograph (2.3 × 2.6mm)

Circuits are packaged in a manner acceptable to the user, but normally this implies conventional dual–in–line packages with pin counts determined by the particular application.

PROGRAMMING THE GATE ARRAYS

All components within a major cell are connected on first layer metal. Routing between major cells is on first layer along the rows (horizontally) and on second layer along the columns (vertically). There are eight horizontal and sixteen vertical tracks associated with each major cell.

After receipt of a custom design requirement, the following design procedure is adopted:–

1. Partition the system into suitable subsections applicable to the gate array .
2. Optimise the individual circuit designs for the gate array design constraints.
3. Place the individual cells within the array.
4. Program the cell interconnections – this involves generating first layer metallisation second layer metallisation and vias (Figure 6).
5. Program the internal cell component connections. A library of possible connections exists, and these are placed oh on the cell as required by the cell function and the interconnections specified above.
6 Program the input/output buffers.

The comprehensive computer aids that have been developed for these gate arrays allow simulation layouts and test sequence generation to be completed in 2–4 weeks. A number of possible customer interfaces are possible, from logic specification at the one extreme to magnetic tape (containing all the layout information necessary to drive the maskmaking pattern generator) at the other.

	ULA 1000	ULA 2000	ULA 3000
Complexity	75 gates	300 gates	300 gates
Internal gate delay	550 psecs	550 psecs	2.0 nsecs
Wire OR delay	80 psecs	80 psecs	200 psecs
Wire AND delay	200 psecs	200 psecs	1.0 nsecs
Max. flip–flop clock rate	400MHz	400 MHz	200 MHz
Power dissipation	900 mW	3.5 W	750 mW
Pin connections	28	64	64
Chip dimensions	91 x 102 mils	170 x 137 mils	170 x 137 mils

Performance summary of the ULA family members.

Plessey world-wide

PLESSEY SALES REPRESENTATIVES:

ALABAMA:	Huntsville	(205) 883-9260	REMCO
ARIZONA:	Scottsdale	(602) 948-4404	Faser Technical Sales
CANADA:	Bolton	(416) 857-4302	MacKay Associates
CALIFORNIA:	Goleta	(805) 964-8751	The Thorson Company of So. California
	Woodland Hills	(213) 340-9143	RELCOM
FLORIDA:	Plantation	(305) 473-2101	Gallagher Associates
GEORGIA:	Duluth	(404) 476-1730	REMCO
ILLINOIS:	Elk Grove Village	(312) 956-1000	Micro Sales Inc.
MARYLAND:	Beltsville	(301) 937-8321	Applied Engineering Consultants
MASSACHUSETTS:	Natick	(617) 655-6080	Wayland Engineering Sales
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MINNESOTA:	Bloomington	(612) 884-8291	Electronics Sales Agency Inc.
MISSOURI:	Independence	(816) 254-3600	Engineering Services Company
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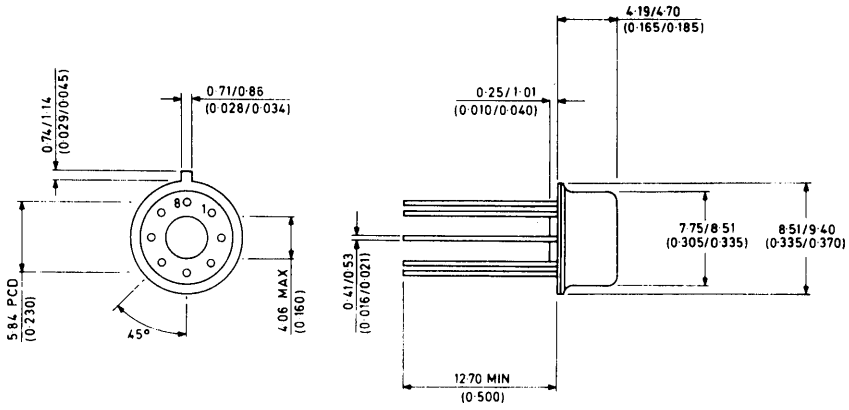

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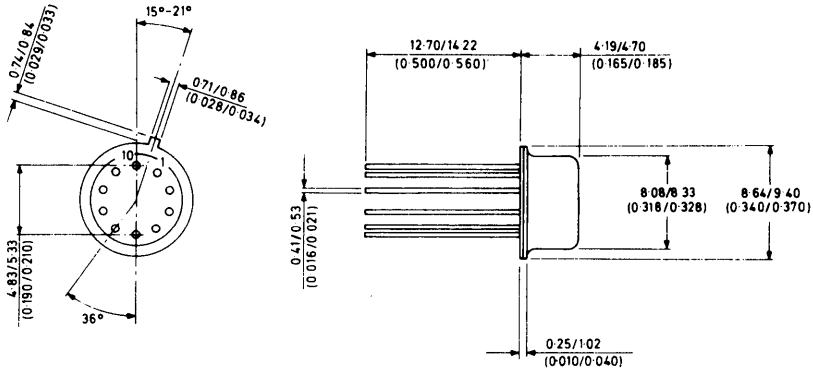

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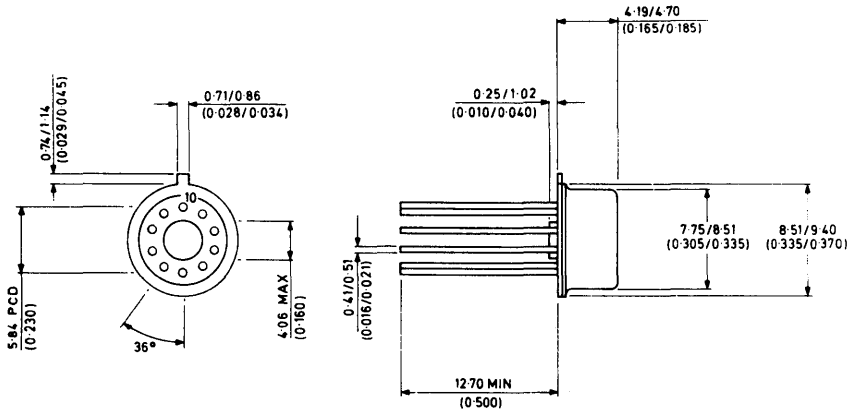

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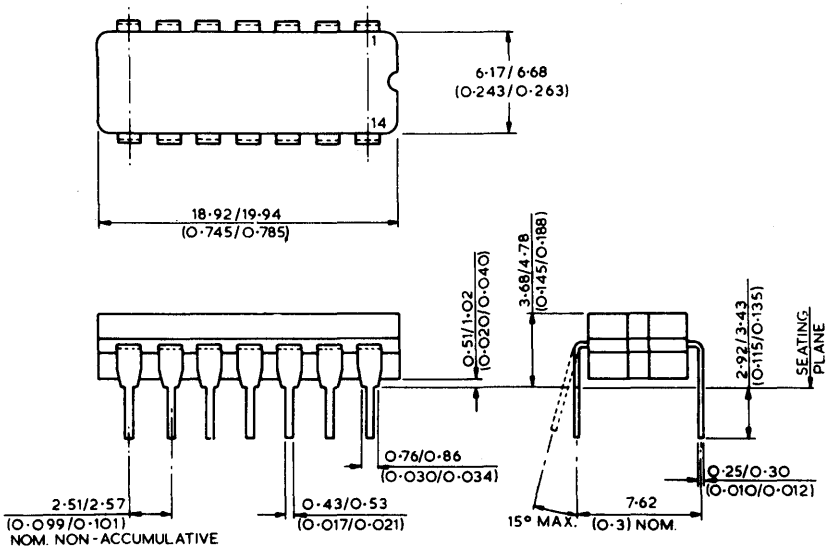

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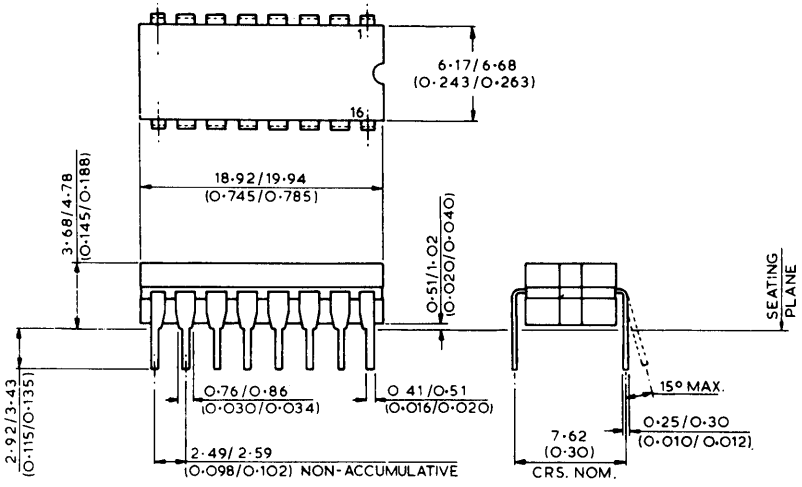

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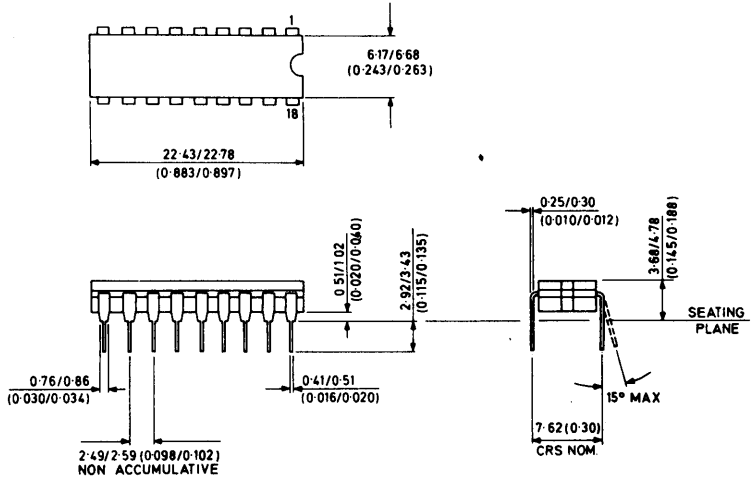

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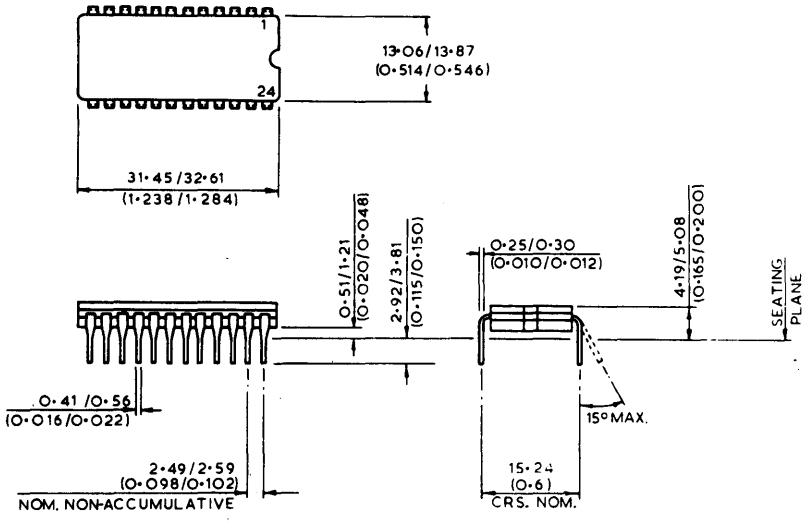

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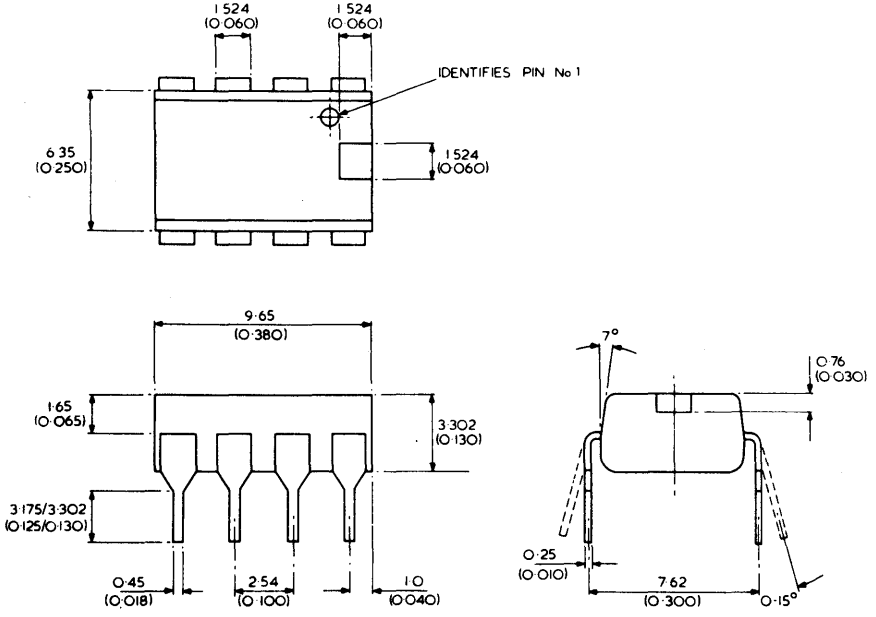

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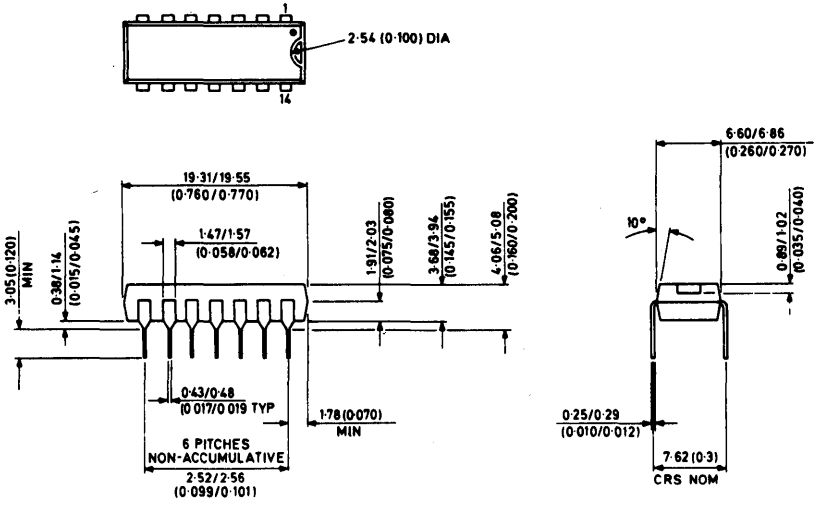

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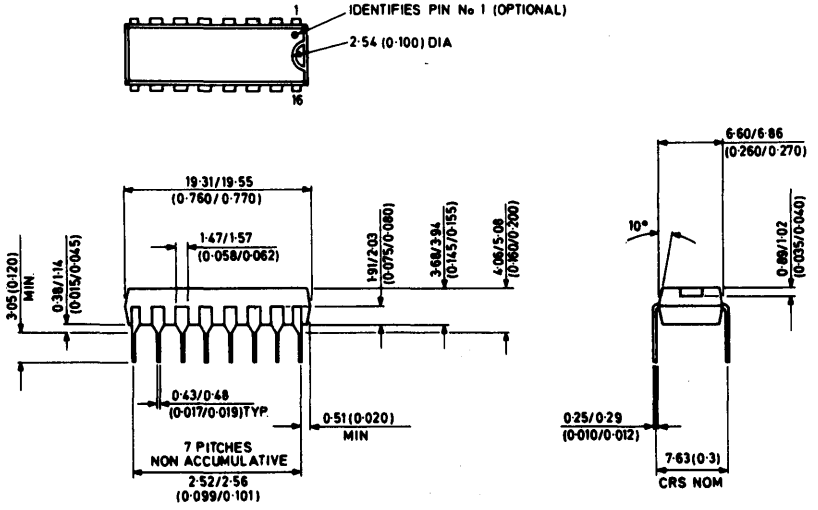

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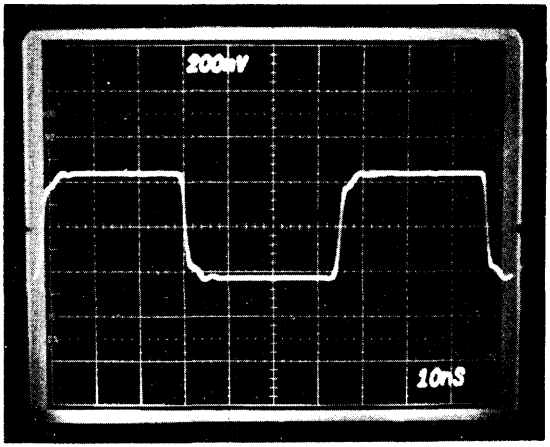

Fig. 27

The SP9685 comparator

GENERAL DESCRIPTION

The SP9685 is a high speed latched comparator, the circuit diagram for which is shown in Fig. 28. The unlatched gain is approximately 50dB at frequencies up to over 200MHz. The main differences between the SP9685 and the SP9750 are as follows:–

1. The SP9685 is a simple comparator and does not include the gates and precision current sources of the SP9750.
2. The unlatched gain of the SP9685 is greater than that of the SP9750.
3. The latch enable control of the SP9685 has the opposite phase of operation to that of the SP9750 latch control.
4. Two gain stages follow the latch of the SP9685 whereas only one is used on the SP9750.
5. Q and $\bar{Q}$ outputs are provided on the SP9685.

Short pulse detector

This simple circuit for the SP9685 has applications in nucleonics and high energy physics. In its simplest form, the circuit is shown in Fig. 29.

A positive going pulse of any width, down to the minimum defined by the propagation delay plus the setup time, and of any height between the maximum common mode signal and the minimum overdrive that will reliably switch the comparator can be quickly detected and will cause the circuit to