

PHILIPS

Signetics TTL

IC09N New series 1984

PHILIPS

Data handbook



Electronic
components
and materials

Integrated circuits

Book IC09N
New series

1984

TTL Logic series

NEW HANDBOOK SERIES

signetics

TTL LOGIC SERIES

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DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.

Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

- T1 Tubes for r.f. heating**
- T2a Transmitting tubes for communications, glass types**
- T2b Transmitting tubes for communications, ceramic types**
- T3 Klystrons, travelling-wave tubes, microwave diodes**
- ET3 Special Quality tubes, miscellaneous devices (will not be reprinted)**
- T4 Magnetrons**
- T5 Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications
- T6 Geiger-Müller tubes**
- T7 Gas-filled tubes**
Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories
- T8 Picture tubes and components**
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display
- T9 Photo and electron multipliers**
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates
- T10 Camera tubes and accessories**
- T11 Microwave semiconductors and components**
- T12 Vidicons and Newvicons**
- T13 Image intensifiers**
- T14 Infrared detectors**

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

- S1 Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes(< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
- S2 Power diodes, thyristors, triacs**
Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs
- S3 Small-signal transistors**
- S4a Low-frequency power transistors and hybrid modules**
- S4b High-voltage and switching power transistors**
- S5 Field-effect transistors**
- S6 R.F. power transistors and modules**
- S7 Microminiature semiconductors for hybrid circuits**
- S8 Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.
- S9 Power MOS transistors**
- S10 Wideband transistors and wideband hybrid IC modules**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES

- IC1** Bipolar ICs for radio and audio equipment
- IC2** Bipolar ICs for video equipment
- IC3** ICs for digital systems in radio, audio and video equipment
- IC4** Digital integrated circuits
CMOS HE4000B family
- IC5** Digital integrated circuits – ECL
ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs
- IC6** Professional analogue integrated circuits
- IC7** Signetics bipolar memories
- IC8** Signetics analogue circuits
- IC9** Signetics TTL logic
- IC10** Signetics Integrated Fuse Logic (IFL)
- IC11** Microprocessors, microcomputers and peripheral circuitry

NEW SERIES

- | | | |
|--------------|--|------------------|
| IC01N | Radio, audio and associated systems
Bipolar, MOS | |
| IC02N | Video and associated systems
Bipolar, MOS | |
| IC03N | Telephony equipment
Bipolar, MOS | |
| IC04N | HE4000B logic family
CMOS | |
| IC05N | HE4000B logic family uncased integrated circuits
CMOS | (published 1984) |
| IC06N | PC54/74HC/HCU/HCT logic families
HCMOS | |
| IC07N | PC54/74HC/HCU/HCT uncased integrated circuits
HCMOS | |
| IC08N | 10K and 100K logic family
ECL | |
| IC09N | Logic series
TTL | (published 1984) |
| IC10N | Memories
MOS, TTL, ECL | |
| IC11N | Analogue - industrial | |
| IC12N | Semi-custom gate arrays & cell libraries
ISL, ECL, CMOS | |
| IC13N | Semi-custom integrated fuse logic
IFL series 20/24/28 | |
| IC14N | Microprocessors, microcontrollers & peripherals
Bipolar, MOS | |
| IC15N | Logic series
FAST TTL | (published 1984) |

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

- C1 Assemblies for industrial use**
PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs
- C2 Television tuners, video modulators, surface acoustic wave filters**
- C3 Loudspeakers**
- C4 Ferroxcube potcores, square cores and cross cores**
- C5 Ferroxcube for power, audio/video and accelerators**
- C6 Synchronous motors and gearboxes**
- C7 Variable capacitors**
- C8 Variable mains transformers**
- C9 Piezoelectric quartz devices**
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements
- C10 Connectors**
- C11 Non-linear resistors**
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
- C12 Variable resistors and test switches**
- C13 Fixed resistors**
- C14 Electrolytic and solid capacitors**
- C15 Film capacitors, ceramic capacitors**
- C16 Permanent magnet materials**
- C17 Stepping motors and associated electronics**
- C18 D.C. motors**
- C19 Piezoelectric ceramics**
- C20 Wire-wound components for TVs and monitors**

PREFACE

Signetics would like to thank you for your interest in our products. We hope you find the product information you need on the TTL data sheets contained in this data manual. The information is presented in a concise and consistent format for easy device and parameter location. This manual contains product information on most Signetics TTL devices. The majority of this book is dedicated to the 54/74, 54S/74S, 54LS/74LS, and 8T families. Each data sheet stands alone and contains the full DC and AC specifications for that particular part type.

Changes from the 1982 edition include:

- expanded Technology and Function Cross Reference guides
- addition of the S.O. package as an option for many commercial part types
- deletion of the hermetic CERDIP package as a commercial option
- addition of a chapter Surface Mounted Devices (SMD)
- addition of 21 products not listed in the 1982 Data Manual
- FAST and HC/HCT technologies are referred to in the Technology and Function Cross Reference guides. These products are highlighted by a shaded area to indicate that data sheets are contained in separate publications available from your nearest Signetics Sales Office.

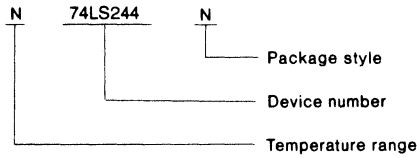
Signetics is continually developing new products. As you see new product announcements, you should contact your local Signetics sales office, representative or authorized distributor or write Signetics, c/o Information Services at 811 East Arques Avenue, P.O. Box 3409, Sunnyvale, California 94088-3409, for the latest technical information.



ORDERING INFORMATION

The Signetics TTL logic products are available in a variety of packages and two temperature ranges. The correct ordering code of part number for the devices is an alpha-numeric sequence as explained below. The commercial range (7400, N8T, etc.) devices are available in standard plastic DIP and surface mounted SO plastic packages. and the military range (5400, S8T, etc.) devices are available in ceramic DIP, flatpack, and leadless chip carrier packages. All devices are not available in both temperature ranges or all packages. The ordering codes on the individual data sheets indicate the normal or planned availability of the product. However, the availability of specific part numbers can be obtained from your local Signetics sales office or franchised distributor.

Ordering Code



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
N = Commercial range 0°C to 70°C	74LS244	N = Plastic DIP D = SO Plastic
S = Military range -55°C to 125°C	54LS244	F = Ceramic DIP W = Ceramic Flatpack G = Ceramic Leadless Chip Carrier

TTL PRODUCT STATUS AND DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Section 1 Selection Guide

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HC/HCT TECHNOLOGY SELECTION GUIDE

TECHNOLOGY SELECTION GUIDE

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
74/54							
00	Quad 2-Input NAND Gate	A	A	A	A	A	A
01	Quad 2-Input NAND Gate, OC	A	A	A	A	A	A
02	Quad 2-Input NOR Gate	A	A	A	A	Q1 84	Q1 84
03	Quad 2-Input NAND Gate	A	A	A	A	A	A
04	Hex Inverter	A	A	A	A	Q2 84	Q2 84
05	Hex Inverter, OC	A	A	A	A	A	A
06	Hex Inverter Buffer/Driver, OC	A	A	A	A	A	A
07	Hex Buffer/Driver, OC	A	A	A	A	A	A
08	Quad 2-Input	A	A	A	A	Q2 84	Q2 84
09	Quad 2-Input AND Gate, OC	A	A	A	A	A	A
10	Triple 3-Input NAND Gate	A	A	A	A	Q2 84	Q2 84
11	Triple 3-Input AND Gate	A	A	A	A	Q2 84	Q2 84
13	Dual 4-Input NAND Schmitt Trigger	A	A	A	A	A	A
14	Hex Schmitt Trigger	A	A	A	A	Q2 84	Q2 84
16	Hex Inverter Buffer/Driver, OC	A	A	A	A	A	A
17	Hex Buffer/Driver, OC	A	A	A	A	A	A
20	Dual 4-Input NAND Gate	A	A	A	A	Q2 84	Q2 84
21	Dual 4-Input AND Gate	A	A	A	A	A	A
25	Dual 4-Input NOR with Strobe	A	A	A	A	A	A
26	Quad 2-Input NAND Gate, OC	A	A	A	A	A	A
27	Triple 3-Input NOR Gate	A	A	A	A	Q1 84	Q1 84
28	Quad 2-Input NOR Buffer	A	A	A	A	A	A
30	8-Input NAND Gate	A	A	A	A	A	A
32	Quad 2-Input OR Gate	A	A	A	A	Q2 84	Q2 84
33	Quad 2-Input NOR Buffer	A	A	A	A	A	A
37	Quad 2-Input NAND Buffer	A	A	A	1H 84	A	A
38	Quad 2-Input NAND Buffer, OC	A	A	A	1H 84	A	A
39	Quad 2-Input NAND Buffer, OC	A	A	A	A	A	A
40	Dual 4-Input NAND Buffer	A	A	A	1H 84	A	A
42	BCD-to-Decimal Decoder	A	A	A	A	Q2 84	Q2 84
45	BCD-to-Decimal Decoder/Driver, OC	A	A	A	A	A	A
50	Expandable Dual 2-Wide 2-Input AOI Gate	A	A	A	A	A	A
51	Dual 2-Wide 2-Input AOI Gate	A	A	A	A	A	A
54	4-Wide 2-Input AOI Gate	A	A	A	A	A	A
64	4-2-3-2 Input AOI Gate	A	A	A	A	A	A
73	Dual J-K Master-Slave Flip-Flop	A	A	A	A	Q1 84	Q1 84
74	Dual D-Type Positive Edge-Triggered Flip-Flop	A	A	A*	A	A	A
75	Quad Bistable Latch	A	A	A	A	Q1 84	Q1 84
76	Dual J-K Master-Slave Flip-Flop	A	A	A	A	A	A
83	4-Bit Binary Full Adder, Ripple Carry	A	A	A*	A	A	A
85	4-Bit Magnitude Comparator	A	A	A	1H 84	Q2 84	Q2 84
86	Quad 2-Input Exclusive-OR Gate	A	A	A	A	A	A
90	Decade Ripple Counter	A	A	A	A	A	A
91	8-Bit Shift Register	A	A	A	A	A	A
92	Divide-by-12 Counter	A	A	A	A	A	A
93	4-Bit Binary Ripple Counter	A	A	A	A	A	A
94	4-Bit PISO Shift Register	A	A	A	A	A	A
95	4-Bit Shift Register	A	A	A**	A	A	A
96	5-Bit Shift Register	A	A	A	A	A	A
107	Dual J-K Master-Slave Flip-Flop	A	A	A	A	Q1 84	Q1 84
109	Dual J-K Positive Edge-Triggered Flip-Flop	A	A	A*	A	Q1 84	Q1 84
112	Dual J-K Negative Edge-Triggered Flip-Flop	A	A	A	2H 84	Q2 84	Q2 84
113	Dual J-K Negative Edge-Triggered Flip-Flop	A	A	A	2H 84	A	A
114	Dual J-K Negative Edge-Triggered Flip-Flop	A	A	A	2H 84	A	A
116	Dual 4-Bit Latch with Clear	A	A	A	A	A	A

*A Version; **B Version;

FAST and HC/HCT data sheets are contained in separate publications. Please contact nearest Sales Office for more information.

HC/HCT TECHNOLOGY SELECTION GUIDE

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DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
121	Monostable Multivibrator	A					
123	Retriggerable Monostable Multivibrator	A				A	A
125	Quad 3-State Buffer	A		A			
126	Quad 3-State Buffer	A		A			
128	Quad 2-Input NOR Buffer	A					
132	Quad Schmitt Trigger	A		A	A	A	A
133	13-Input NAND Gate		A				
134	12-Input NAND Gate, 3-State		A				
135	Quad Exclusive-OR/NOR Gate		A				
136	Quad Exclusive-OR, OC			A			
138	3-to-8 Decoder/Demultiplexer		A	A	A	Q1 84	Q1 84
139	Dual 2-to-4 Decoder/Demultiplexer		A	A	A	A	A
140	Dual 4-Input NAND Line Driver		A				
145	BCD-to-Decimal Decoder/Driver, OC	A					
147	10-to-4 Priority Encoder	A				Q1 84	Q1 84
148	8-to-3 Priority Encoder	A			2H 84		
150	16-to-6 Multiplexer	A					
151	8-to-1 Multiplexer	A	A	A	1H 84	Q1 84	Q1 84
153	Dual 4-to-1 Multiplexer	A	A	A	2H 84	A	A
154	4-to-16 Decoder/Demultiplexer	A		A		A	A
155	Dual 2-to-4 Decoder/Demultiplexer	A		A			
156	Dual 2-to-4 Decoder/Demultiplexer, OC	A		A			
157	Quad 2-to-1 Multiplexer	A	A	A	A	A	A
158	Quad 2-to-1 Multiplexer	A	A	A	A	A	A
160	Synchronous 4-Bit Decade Counter	A		A*	2H 84	Q2 84	Q2 84
161	Synchronous 4-Bit Binary Counter	A		A*	2H 84	Q2 84	Q2 84
162	Synchronous 4-Bit Decade Counter			A*	2H 84	Q2 84	Q2 84
163	Synchronous 4-Bit Binary Counter	A		A*	2H 84	Q2 84	Q2 84
164	8-Bit PISO Shift Register	A		A	2H 84	A	A
165	8-Bit PISO Shift Register	A				A	A
166	8-Bit PISO Shift Register	A				Q1 84	Q1 84
168	Decade Up/Down Counter		A	A*	2H 84		
169	Binary Up/Down Counter		A	A*	2H 84		
170	4 x 4 Register File, OC	A					
172	16-Bit Multiple Port Register File		A				
173	Quad D-Type Flip-Flop, 3-State	A	A	A		Q2 84	Q2 84
174	Hex D-Type Flip-Flop with Clear	A	A	A	2H 84	Q2 84	Q2 84
175	Quad D-Type Flip-Flop	A	A	A	2H 84	Q1 84	Q1 84
180	8-Bit Odd/Even Parity Checker	A					
181	4-Bit Arithmetic Logic Unit	A	A	A	2H 84		
182	Look-Ahead Generator		A		2H 84		
190	Decade Up/Down Counter	A			2H 84	Q2 84	Q2 84
191	Binary Up/Down Counter	A		A	2H 84	Q2 84	Q2 84
192	Decade Up/Down Counter	A		A	2H 84	Q1 84	Q1 84
193	4-Bit Binary Up/Down Counter	A		A	2H 84	Q2 84	Q2 84
194	4-Bit Bidirectional Shift Register	A	A	A	A	A	A
195	4-Bit Parallel-Access Shift Register	A	A	A	1H 84	A	A
197	Presetable Binary Counter			A			
198	8-Bit Bidirectional Universal Shift Register				1985		
199	8-Bit Universal Shift Register	A					
221	Dual Monostable Multivibrator	A				P	P
225	FIFO		A				
238	1-of-8 Decoder/Demultiplexer, True/Inverting					Q1 84	Q1 84
240	Octal 3-State Buffer		A	A	A	A	A
241	Octal 3-State Buffer		A	A	A	A	A

*A Version; **B Version;

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HC/HCT TECHNOLOGY SELECTION GUIDE

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
242	Quad Bus Transceiver		A	A	A	Q1 84	Q1 84
243	Quad Bus Transceiver		A	A	A	Q1 84	Q1 84
244	Octal 3-State Buffer		A	A	A	A	A
245	Octal Bus Transceiver		A	A	1H 84	A	A
251	8-to-1 Multiplexer, 3-State		A	A	1H 84	A	A
253	Dual 4-to-1 Multiplexer, 3-State		A	A	2H 84	A	A
256	Dual 4-Bit Addressable Latch		A	A	A		
257	Quad 2-to-1 Multiplexer, 3-State		A	A*	A	A	A
258	Quad 2-to-1 Multiplexer, 3-State			A*	A		
259	8-Bit Addressable Latch			A	A	Q2 84	Q2 84
260	Dual 5-Input NOR Gate		A	A			
266	Quad Exclusive-OR, OC			A			
269	8-Bit Up/Down Counter				1H 84		
273	Octal D Flip-Flop		A	A	1H 84	Q1 84	Q1 84
279	Quad S-R Latch	A					
280	9-Bit Odd/Even Parity Generator/Checker		A		A*	A	A
283	4-Bit Adder			A	1985		
290	Decade Counter			A			
293	4-Bit Binary Counter			A			
295	4-Bit Shift Register, 3-State			A**			
297	Digital Phase-Locked Loop Filter					Q1 84	Q1 84
298	Quad 2-Port Register	A		A	1H 84		
299	Octal Shift/Storage Register, 3-State				2H 84	Q1 84	Q1 84
322	Octal Shift/Storage Register				2H 84		
323	Octal Shift/Storage Register				2H 84		
350	4-Bit Four-Way Shifter		A		A		
352	Dual 4-to-1 Multiplexer, Inverting			A	2H 84		
353	Dual 4-to-1 Multiplexer, Inverting, 3-State			A	2H 84		
354	8-Input Multiplexer/Register, 3-State					Q2 84	Q2 84
356	8-Input Multiplexer/Register, 3-State					Q2 84	Q2 84
363	Octal Latch, 3-State, MOS Compatible Outputs			A			
364	Octal D Flip-Flop, 3-State, MOS Compatible Outputs			A			
365	Hex Buffer with Common Enable, 3-State	A		A*	1H 84	Q3 84	Q3 84
366	Hex Inverter with Common Enable, 3-State	A		A*	1H 84	Q1 84	Q1 84
367	Hex Buffer, 4-Bit and 2-Bit, 3-State	A		A*	1H 84	Q1 84	Q1 84
368	Hex Inverter, 4-Bit and 2-Bit, 3-State	A		A*	1H 84	Q1 84	Q1 84
373	Octal Latch, 3-State		A	A	A	Q1 84	Q1 84
374	Octal D Flip-Flop, 3-State		A	A	A	Q1 84	Q1 84
375	Quad Latch			A			
377	Octal D-Type Flip-Flop with Enable			A	A	A	A
378	Hex D Flip-Flop with Enable			A	2H 84		
379	Quad D Flip-Flop with Enable				2H 84		
384	8-Bit Serial/Parallel Two's Complement Multiplexer					P	P
390	Dual Decade Ripple Counter			A		Q1 84	Q1 84
393	Dual Binary Ripple Counter			A			
395	4-Bit Cascadable Shift Register, 3-State			A	1H 84		
398	4-Bit Flip-Flop, True/Complement				2H 84		
399	4-Bit Flip-Flop, True/Complement				2H 84		
423	Dual Retriggerable Monostable Multivibrator					P	P
445	BCD-to-Decimal Decoder with 7V Output			A			

*A Version; **B Version;

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HC/HCT TECHNOLOGY SELECTION GUIDE

DEVICE NUMBER	DESCRIPTION	STD	S	LS	FAST	HC	HCT
490	Dual Decade Ripple Counter			A			
521	8-Bit Comparator				A		
524	8-Bit Register Comparator				1H 84		
533	Inverting Octal D Latch, 3-State				A	Q1 84	Q1 84
534	Octal D Flip-Flop, 3-State				A	A	A
540	Octal Driver			A		Q1 84	Q1 84
541	Octal Driver			A		Q1 84	Q1 84
545	Octal Bus Transceiver				1H 84		
563	Octal Transparent Inverting Latch, 3-State					A	A
564	Octal D Type Inverting Flip-Flop, 3-State					Q1 84	Q1 84
568	BCD Decade Up/Down Synchronous Counter			A*	2H 84		
569	4-Bit Binary Up/Down Synchronous Counter			A*	2H 84		
573	Octal Transparent Latch, 3-State					A	A
574	Octal D Type Flip-Flop, Positive Edge-Triggered, 3-State					Q2 84	Q2 84
579	8-Bit Up/Down Counter, Common I/O				1H 84		
588	GPIO Compatible Octal Transceiver				1H 84		
595	8-Bit Shift Register with Output Latch				84		
596	8-Bit Shift Register with Output Latch				84		
597	8-Bit Shift Register with Input Latch				84		
598	8-Bit Shift Register with Input Latch				84		
604	Dual 8-Bit Latch				1H 84		
605	Dual 8-Bit Latch				1H 84		
620	Octal Transceiver, 3-State			A	1H 84		
621	Octal Transceiver, OC			84	1H 84		
622	Octal Transceiver, 3-State			84	1H 84		
623	Octal Transceiver, OC			A	1H 84		
630	Memory Error Detector/Corrector, 3-State				1H 84		
631	Memory Error Detector/Corrector				1H 84		
640	Octal Bus Transceiver, 3-State			A	1H 84	A	A
640-1	Octal Bus Transceiver, 3-State, 48mA Sink Capability			A			
641	Octal Bus Transceiver, OC			A			
641-1	Octal Bus Transceiver, OC, 48mA Sink Capability			A			
642	Octal Bus Transceiver, OC			A			
642-1	Octal Bus Transceiver, OC, 48mA Sink Capability			A			
643	Octal True/Inverting Transceiver, 3-State					A	A
645	Octal Bus Transceiver, 3-State			A			
645-1	Octal Bus Transceiver, 3-State, 48mA Sink Capability			A			
646	Octal Bus Transceiver with Registers				1H 84	P	P
647	Octal Bus Transceiver with Registers				1H 84		
648	Octal Bus Transceiver with Registers				1H 84	P	P
649	Octal Bus Transceiver with Registers				1H 84		
655	Octal Buffer with Parity Generator-Checker				A		
656	Octal Buffer with Parity Generator-Checker				A		
657	Octal Bus Transceiver with Parity Generator-Checker				1H 84		
670	4 x 4 Register File, 3-State			A		Q2 84	Q2 84
673	16-Bit SIPO Shift Register				2H 84		
674	16-Bit PISO Shift Register				2H 84		
675	16-Bit PISO Shift Register with Serial Output Capability				2H 84		
676	16-Bit PISO Shift Register with Parallel Output Capability				2H 84		
686	8-Bit Magnitude Comparator					A	A
751	8-Bit Binary Counter, 3-State				2H 84		
752	8-Bit BCD Counter, 3-State				2H 84		
764	Dual Port RAM Controller with DRAM Refresh			84			
779	8-Bit Counter				1H 84		

*A Version. **B Version

FAST and HC/HCT data sheets are contained in separate publications. Please contact nearest Sales Office for more information.

FUNCTION CROSS REFERENCE GUIDE

The Function Cross Reference Guide is provided for customer reference only. It does not represent all the devices available from Signetics' Logic Division. The device number given is a base number. Check the Number Cross Reference Guide for the complete part number and availability.

GATES

FUNCTION	DEVICE NO.
Inverters	
Hex Inverter	04
Hex Inverter, OC	05
Hex Inverter buffer/Driver, OC (30V)	06
Hex Inverter Schmitt Trigger	14
Hex Inverter Buffer/Driver, OC (15V)	16
Hex inverter (15V to TTL Levels)	4049
Hex Inverter Unbuffered Outputs	4069UB
Hex inverter Schmitt Trigger	40106
Dual Complementary Pair and Inverter, Unbuffered	4007UB
NAND	
Quad 2-Input	00
Quad 2-Input, OC	01
Quad 2-Input, OC	03
Quad 2-Input, OC	26
Triple 3-Input	10
Dual 4-Input, Schmitt Trigger	13
Dual 4-Input	20
8-Input	30
Quad 2-Input, Schmitt Trigger	132
Quad 2-Input	4011
Quad 2-Input, Unbuffered Outputs	4011UB
Dual 4-Input	4012
Triple 3-Input	4013
8-Input	4068
12-Input	134
13-Input	133
AND	
Quad 2-Input	08
Quad 2-Input	4081
Quad 2-Input, OC	09
Triple 3-Input	11
Dual 4-Input	21
Dual 4-Input	4082
NOR	
Quad 2-Input	02
Quad 2-Input	28

FUNCTION	DEVICE NO.
NOR (Continued)	
Quad 2-Input	128
Quad 2-Input	4001
Quad 2-Input, Unbuffered Output	4001UB
Quad 2-Input, OC	33
Triple 3-Input	27
Triple 3-Input	4025
Dual 3-Input, with Inverter	4000
Dual 4-Input	4002
Dual 4-Input, with Strobe	25
Dual 5-Input	260
8-Input	4078
OR	
Quad 2-Input	32
Quad 2-Input	4071
Triple 3-Input	4075
Dual 4-Input	4072
Exclusive-OR	
Quad	86
Quad	4030
Quad, OC	136
Quad	4070
Quad Exclusive OR-NOR	135
Exclusive-NOR	
Quad	4077
Quad, OC	266
Quad Exclusive OR-NOR	135
Combination Gates	
Expandable Dual 2-Wide 2-Input AND-OR-Invert	50
Dual 2-Wide 2-Input AND-OR-Invert	51
4-Wide 2-Input AND-OR-Invert	54
4-2-3-2 Input AND-OR-Invert	64
Dual 3-Input NOR Gate with Inverter	4000
Dual Complementary Pair and Inverter, Unbuffered	4007UB
Dual 2-Wide 2-Input AND-OR-Invert	4085
4-Wide 2-Input AND-OR-Invert	4086

DUAL FLIP-FLOPS

FUNCTION	DEVICE NUMBER	CLOCK EDGE	SET	CLEAR
D	74		LOW	LOW
D	4013		HIGH	HIGH
JK	73			LOW
JK	76		LOW	LOW
JK	107			LOW
JK	109		LOW	LOW
JK	112		LOW	LOW
JK	113		LOW	
JK	4027		HIGH	HIGH

Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

FUNCTION CROSS REFERENCE GUIDE

MULTIPLE FLIP-FLOPS

FUNCTION	DEVICE NUMBER	RESET (LEVEL)	CLOCK EDGE	OUTPUT
Quad D	175	LOW		True, Comp
Quad D	40175	LOW		True
Quad D with Enable	379			True, Comp
Quad D, 3-State	4079	HIGH		True
Quad D, 3-State	8T10	HIGH		True
Hex D	174	LOW		True
Hex D with Enable	378			True
Octal D	273	LOW		True
Octal D, 3-State	374			True
Octal D, 3-State	534			Comp
Octal D, 3-State	564			Comp
Octal D, 3-State	574			True
Octal D, 3-State	40374			True
Octal D, 3-State	8TS806			True
Octal D, 3-State	8TS808			Comp
Octal D, 3-State, MOS Compatible Outputs	364			True

OTHER REGISTERS, REGISTER FILES

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY*	CLOCK
Quad 2 Port	298	4 x 2		2D (mux)	
Quad 2 Port	398	4 x 2		2D (mux)	
Quad 2 Port	399	4 x 2		2D (mux)	
Register File, OC	170	4 x 4		4A	
Multiple Port Register File, 3-State	172	16		3D (mux)	
4 x 4 Register File, 3-State	670	4 x 4		4A	
16 x 5 FIFO, 3-State	225	5		5S	
4 x 16 FIFO	40105	4	D	4S	

*D = D type input, A = Asynchronous data input, S = Synchronous data input

Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

FUNCTION CROSS REFERENCE GUIDE

SHIFT REGISTERS

FUNCTION	DEVICE NUMBER	BITS	SERIAL ENTRY	PARALLEL ENTRY	CLOCK
Serial In/Serial Out Shift Register	91	8	D _A and D _B		┐
Serial In/Serial Out Shift Right	4006	(2 × 4) (2 × 5)	D		┐
Serial In/Serial Out Shift Right	4031	64	D _A + D _B		┐
Dual Serial In/Serial Out Shift Right, 3-State	4517	(4 × 16)	D		┐
Quad Serial In/Serial Out Shift Right	4731	64	D		┐
Serial In/Serial Out Variable Length Shift Right	4557	1 to 64	D _A + D _B		┐ and ┐
Serial In/Serial Out Shift Right, 3-State	4094	8	D		┐
Parallel/Serial In/Serial Out Shift Right	94	4	D	2 × 4A (mux)	┐
Parallel/Serial In/Serial Out Shift Right	165	8	D	8A	┐
Parallel/Serial In/Serial Out Shift Right	166	8	D	8S	┐
Parallel/Serial In/Serial Out Shift Right	195	4	J, \bar{K}	4S	┐
Parallel/Serial In/Serial Out Shift Right	199	8	J, K	8S	┐
Parallel/Serial In/Serial Out Shift Right	597	8	D	8S	┐
Parallel/Serial In/Serial Out Shift Right	4014	8	D	8S	┐
Parallel/Serial In/Serial Out Shift Right	4021	8	D	8A	┐
Parallel/Serial In/Serial Out Shift Right	8274	10	D	10S	┐
Parallel/Serial In/Serial Out Shift Right, 3-State	598	8	S ₀ , S ₁	8S	┐
Serial In/Parallel Out Shift Right	164	8	D ₀ and D ₁		┐
Serial In/Parallel Out Shift Right, with Reset	8273	10	D		┐ or ┐
Dual Serial In/Parallel Out Shift Right	4015	4	D		┐
Serial In/Parallel Out, 3-State	595	8	D		┐
Serial In/Parallel Out, OC	596	8	D		┐
Parallel In/Serial In/Parallel Out Shift Right	95	4	D	5A	┐
Parallel In/Serial In/Parallel Out Shift Right	96	5	D	5A	┐
Parallel In/Serial In/Parallel Out Shift Right	40195	4	J, \bar{K}	4S	┐
Parallel In/Serial In/Parallel Out Shift Right	8271	4	D	4S	┐
Parallel In/Serial In/Parallel Out Shift Right	82S71	4	D	4S	┐
Parallel In/Serial In/Parallel Out Shift Right	4035	4	J, \bar{K}	4S	┐
Parallel In/Serial In/Parallel Out Shift Right, 3-State	295	4	D	4S	┐
Parallel In/Serial In/Parallel Out Shift Right, 3-State	395	4	D	4S	┐
Parallel In/Serial In/Parallel Out Shift Right, 3-State	322	8	D ₀ + D ₁	8S (I/O)	┐
Parallel In/Serial In/Parallel Out Bidirectional	194	4	Dr, D _L	4S	┐
Parallel In/Serial In/Parallel Out Bidirectional	198	8	Dr, D _L	8S	┐
Parallel In/Serial In/Parallel Out Bidirectional	40194	4	Dr, D _L	4S	┐
Parallel In/Serial In/Parallel Out Bidirectional, 3-State	299	8	Dr, D _L	8S	┐
Parallel In/Serial In/Parallel Out Bidirectional, 3-State	323	8	Dr, D _L	8S (I/O)	┐
Parallel In/Serial In/Parallel Out Bidirectional, 3-State	40194	4	Dr, D _L	4S	┐

S = Synchronous, A = Asynchronous

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

FUNCTION CROSS REFERENCE GUIDE

LATCHES

FUNCTION	DEVICE NUMBER	COMMON CLEAR (LEVEL)	ENABLE INPUT (LEVEL)	OUTPUT
Quad D	75		2 (H)	True, Comp
Quad D	375		2 (H)	True, Comp
Quad D	4042		2 (H)	True
Quad SR	279			True
Quad SR, 3-State	4043			True
Quad SR, 3-State	4044			True
Dual 4-Bit Transparent	116	LOW	2 (L)	True
Dual 4-Bit Addressable	256	LOW	1 (L)	True
Dual 4-Bit, Strobed	4508	HIGH	1 (L)	True
6-Bit (2-Bit and 4-Bit)	8T3404		1 (L)	Comp
8-Bit Addressable	259	LOW	1 (H)	True
8-Bit Addressable	4724	HIGH	1 (L)	True
8-Bit Addressable	9334	LOW	1 (L)	True
Octal, 3-State	373		1 (H)	True
Octal Inverting, 3-State	533		1 (H)	Comp
Octal Transparent, 3-State	40373		1 (H)	True
Octal Transparent, 3-State	8TS805		1 (H)	True
Octal Inverting, 3-State	8TS807		1 (H)	Comp
Octal, 3-State with MOS Compatible Outputs	363		1 (H)	True

MULTIPLEXERS

FUNCTION	DEVICE NUMBER	ENABLE INPUT (LEVEL)	SELECT INPUTS	OUTPUT
Quad 2-Input	157	1 (L)	1	True
Quad 2-Input	158	1 (L)	1	True
Quad 2-Input	298	Clocked $\bar{\text{L}}$	1	True, Latched
Quad 2-Input	398	1 (H)	1	True, Comp Registered
Quad 2-Input	399	1 (H)	1	True, Registered
Quad 2-Input	4019		2	True
Quad 2-Input	4519		2	True
Quad 2-Input	8266		2	True
Quad 2-Input	9322	1 (L)	1	True
Quad 2-Input, 3-State	257		1	True
Quad 2-Input, 3-State	258		1	Comp
Quad 2-Input, OC	8234		2	Comp
Dual 4-Input	153	2 (L)	2	True, Comp
Dual 4-Input	352	2	2	Comp
Dual 4-Input	9309		2	True, Comp
Dual 4-Input	4539	2 (L)	2	True
Dual 4-Input, 3-State	253		2	True
Dual 4-Input, 3-State	353	2	2	Comp
8-Input	9312	1 (L)	3	True, Comp
8-Input	151	1 (L)	3	True, Comp
8-Input, 3-State	251		1	True, Comp
8-Input, 3-State	356	1 (L)	3	True, Latched
8-Input, 3-State	354	2 (L)	3	True, Latched
8-Input, 3-State	4512	1 (L)	3	True
16-Input	150	1 (L)	4	Comp

ANALOG MULTIPLEXERS/DEMULPLEXERS AND SWITCHES

FUNCTION	DEVICE NUMBER	FUNCTION	DEVICE NUMBER
Triple 2-Channel Mux/Demux	4053	16-Channel Mux/Demux	4066
Dual 4-Channel Mux/Demux	4052	Quad Bilateral Switches	4016
8-Channel Mux/Demux	4051	Quad Bilateral Switches	4067

Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

FUNCTION CROSS REFERENCE GUIDE

COUNTERS

FUNCTION	DEVICE NUMBER	MODULUS	PARALLEL ENTRY	PRESETTABLE	CLOCK EDGE
Asynchronous	90	2 × 5			
Asynchronous	290	2 × 5			
Asynchronous	92	2 × 6			
Asynchronous	93	2 × 8			
Asynchronous	293	2 × 8			
Asynchronous	176	2 × 5	A	X	
Asynchronous	177	2 × 8	A	X	
Asynchronous	197	2 × 8	A	X	
Asynchronous	290	2 × 5			
Asynchronous	293	2 × 8			
Asynchronous	390	2 × 5			
Asynchronous	393	2 × 8			
Asynchronous	490	2 × 5			
Asynchronous	4020	12			
Asynchronous	4024	7			
Asynchronous	4040	14			
Asynchronous with Oscillator	4060	14			
Synchronous	160	10	S	X	
Synchronous	161	16	S	X	
Synchronous	162	10	S	X	
Synchronous	163	16	S	X	
Synchronous, 3-State	751	256	S	X	
Synchronous, 3-State	752	100	S	X	
Synchronous	4256	16	A		
Synchronous	40161	16	S	X	
Synchronous	40163	16	S	X	
Synchronous (Dual)	4518	10			
Synchronous (Dual)	4520	16			
Up/Down	168	10	S	X	
Up/Down	169	16	S	X	
Up/Down	190	10	A	X	
Up/Down	191	16	A	X	
Up/Down	192	10	A	X	
Up/Down	193	16	A	X	
Up/Down	269	8	S	X	
Up/Down	4029	10, 16	A	X	
Up/Down	4510	10	A	X	
Up/Down	4516	16	A	X	
Up/Down	40193	16	A	X	
Up/Down, 3-State	568	10	S	X	
Up/Down, 3-State	569	16	S	X	
Up/Down, 3-State	579	8	S (I/O)	X	
Up/Down, 3-State	779	8	S (I/O)	X	
Frequency Divider	4059	Programmable 3 to 15,999			
Johnson	4017	10			
Johnson	4018	5	A		
Johnson	4022	8			

S = Synchronous A = Asynchronous

Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

FUNCTION CROSS REFERENCE GUIDE

TRI-STATE BUFFERS, DRIVERS AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Buffer	125	True
Quad Buffer	126	True
Quad Bus Driver	8T09	
Quad Bus Transceiver	242	Comp
Quad Bus Transceiver	243	True
Quad Bus Transceiver	8T34	Comp
Quad Bus Transceiver	8T126	Comp
Quad Bus Transceiver	8T127	Comp
Quad Bus Transceiver	8T128	True
Quad Bus Transceiver	8T129	True
Hex Buffer	365	True
Hex Inverter	366	Comp
Hex Buffer, 4-Bit and 2-Bit	367	True
Hex Inverter, 4-Bit and 2-Bit	368	Comp
Hex Buffer	8T95	True
Hex Inverter	8T96	Comp
Hex Buffer	8T97	True
Hex Inverter	8T98	Comp
Hex Buffer	40097	True
Hex Buffer	40098	Comp
Octal Buffer	240	Comp
Octal Buffer	241	True
Octal Buffer	244	True
Octal Buffer	40240	Comp
Octal Buffer	40244	True
Octal Buffer	540	Comp
Octal Buffer	541	True
Octal Buffer with Parity Generator-Checker	655	Comp
Octal Buffer with Parity Generator-Checker	656	True
Octal Transceiver	245	True
Octal Transceiver	545	True
Octal Transceiver with IEEE-488 Termination Resistors	588	True
Octal Transceiver	620	Comp
Octal Transceiver	623	True
Octal Transceiver	640, 640-1	Comp
Octal Transceiver	643	True, Comp
Octal Transceiver	645, 645-1	True
Octal Bus Transceiver with Parity Generator-Checker	657	True
Octal Transceiver	40245	True
Octal Transceiver	8T125	Comp
Octal Transceiver/Register	646	True
Octal Transceiver/Register	648	Comp

LEVEL TRANSLATORS

FUNCTION	DEVICE NUMBER
Hex Inverting Buffer, Up to 15V Input, TTL Level Output	4049
Hex Non-Inverting Buffer, Up to 15V Input, TTL Level Output	4050
Quad Voltage Translator, 3-State, TTL Input, 15V Output	4104
Quad Transceiver, MOS/CMOS to TTL	8T26
Quad Transceiver, MOS/CMOS to TTL	8T28

PRIORITY ENCODERS

FUNCTION	DEVICE NUMBER	INPUT ENABLE (LEVEL)	INPUT/OUTPUT (LEVEL)
8-to-3	148	LOW	Active-LOW
8-to-3	4532	HIGH	Active-HIGH
10-to-4 (BCD)	147		Active-LOW

Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

FUNCTION CROSS REFERENCE GUIDE

DECODERS/DEMULTIPLEXERS

FUNCTION	DEVICE NUMBER	ADDRESS INPUTS	ENABLE (LEVEL)	OUTPUT (LEVEL)
Dual 1 of 4	139	2 + 2	1 (L) + 1 (L)	4 (L) + 4 (L)
Dual 1 of 4	155	2	2 (L) + 1 (L), 1 (H)	4 (L) + 4 (L)
Dual 1 of 4	156	2	2 (L) + 1 (L), 1 (H)	4 (L) + 4 (L)
Dual 1 of 4	4555	2 + 2	1 (L) + 1 (L)	4 (H)
Dual 1 of 4	4556	2 + 2	1 (L) + 1 (L)	4 (L)
1 of 8	138	3	2 (L) 1 (H)	8 (L)
1 of 8	82S50	4 (BCD)		8 (L)
1 of 10	42	4 (BCD)		10 (L)
1 of 10, OC	45	4 (BCD)		10 (L)
1 of 10, OC	145	4 (BCD)		10 (L)
1 of 10, OC	445	4 (BCD)		10 (L)
1 of 10	4028	4 (BCD)		10 (H)
1 of 10	9301	4 (BCD)		10 (L)
1 of 10	82S52	4 (BCD)		10 (L)
1 of 16	154	4	2 (L)	16 (L)
1 of 16	4514	4 (Latched)	1 (L)	16 (H)
1 of 16	4515	4 (Latched)	1 (L)	16 (L)
BCD to 7 Segment Decoder/Driver	4511	4 (Latched)	1 (L)	7 (H)
BCD to 7 Segment Decoder/Driver	4543	4 (Latched)		7 (H)

BUFFERS, DRIVERS AND RECEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad 2-Input NOR Buffer	128	
Quad Buffer	4041	True, Comp
Hex Buffer	4049	Comp
Hex Buffer	4050	True
Strobed Hex Inverter/Buffer	4502	Comp
Dual 4-Input NAND Line Driver	140	
Dual Line Driver (AND/OR)	8T13	
Dual EIA-232B/MIL Line Driver	8T15	Comp
Dual EIA-232B/MIL Receiver	8T16	
Dual Line Driver for IBM 360/370 Interface	8T23	
Dual Line Receiver for IBM 360/370 Interface	8T24	
Hex Bus Receiver (DM8837)	8T37	

OPEN COLLECTOR, BUFFERS, DRIVERS, AND TRANSCEIVERS

FUNCTION	DEVICE NUMBER	OUTPUT
Quad Bus Transceiver	8T38	
Quad Bus Transceiver	8T26	Comp
Quad Bus Transceiver	8T28	True
Hex Inverter	05	Comp
Hex Inverter/Driver	06	Comp
Hex Buffer/Driver	07	True
Hex Buffer/Driver	16	Comp
Hex buffer/Driver	17	True
Octal Transceiver	621	True
Octal Transceiver	622	Comp
Octal Transceiver	641, 641-1	True
Octal Transceiver	642, 642-2	Comp
Octal Transceiver and Registers	647	True
Octal Transceiver and Registers	649	Comp
BCD to Decimal Decoder/Driver	45	Active-LOW
BCD to Decimal Decoder/Driver	145	Active-LOW

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

FUNCTION CROSS REFERENCE GUIDE

MULTIVIBRATORS AND PHASE LOCKED LOOPS

FUNCTION	DEVICE NUMBER
Monostable Multivibrator	121
Dual Retriggerable Monostable Multivibrator	123
Dual Monostable Multivibrator	221
Dual Retriggerable Monostable Multivibrator	423
Dual Monostable Multivibrator	425
Dual Retriggerable Monostable Multivibrator	433
Monostable/Bistable Multivibrator	4047
Digital Phase Locked Loop Filter	297
Phase Locked Loop	4046

ARITHMETIC FUNCTIONS

FUNCTION	DEVICE NUMBER
4-Bit Binary Full Adder, Ripple Carry	83
4-Bit Binary Full Adder, Fast Carry	283
4-Bit Binary Full Adder	4005
4-Bit BCD Full Adder	82S83
4-Bit ALU	181
4-Bit ALU	82S83
Look Ahead Carry Generator	182

COMPARATORS

FUNCTION	DEVICE NUMBER
4-Bit Comparator	85
4-Bit Comparator	4585
5-Bit Comparator	9324
8-Bit Comparator	521
8-Bit Comparator	585

PARITY

FUNCTION	DEVICE NUMBER
8-Bit Odd/Even Parity Checker	180
8-Bit Parity Generator/Checker	8262
8-Bit Parity Generator/Checker	82S62
9-Bit Odd/Even Parity Generator/Checker	280
13-Bit Parity Generator/Checker	4531

SPECIAL FUNCTIONS

FUNCTION	DEVICE NUMBER
Dual-Port RAM Controller with Dynamic Memory Refresh	764
IEC/IEEE Bus Interface	4738
Frequency Synthesizer	4750
A.C. Motor Control Circuit	4752
18-Element Bar Graph LCD Driver	4754

☐ Function not continued in this manual. Please check Technology Selection Guide for appropriate technology—FAST or CMOS.

NOTES

Section 2 Quality and Reliability

QUALITY AND RELIABILITY

SIGNETICS LOGIC QUALITY

Signetics' Logic Division has put together a winning process for manufacturing ICs with built-in quality and reliability. We're striving to ship zero defects, and current quality levels demonstrate our commitment to this goal. Quality guarantees are continually being reviewed to reflect the tangible improvements we have made.

The digital ICs produced in the Logic Division must meet rigid criteria as defined by our design rules and evaluated in a thorough product characterization process. The capabilities of our manufacturing process are measured and the results evaluated and reported through our corporate-wide data base system, QA05. The SURE (Systematic Uniform Reliability Evaluation) program monitors the performance of our product in a variety of accelerated environmental stress conditions. All of these programs and systems are intended to prevent product-related problems and to inform our customers and employees of our progress in achieving zero defects.

RELIABILITY BEGINS WITH THE DESIGN

Reliability and quality must begin with design. No amount of extra testing or inspection will produce reliable ICs from a design that is inherently unreliable. Signetics follows very strict design and layout practices with its digital circuits. To eliminate the possibility of metal migration, current density in any path cannot exceed 2×10^5 amps/cm². Layout rules are followed to minimize the possibility of shorts, circuit anomalies, and SCR type latch-up effects. Numerous ground-to-substrate connections are required to ensure that the entire chip is at the same ground potential, thereby precluding internal noise problems.

PRODUCT CHARACTERIZATION

Before a new design is released, the characterization phase must be completed so that the distribution of parameters resulting from lot-to-lot variations is well within specified limits. Such extensive characterization data also provides a basis for identifying unique application-related problems which are not part of normal data sheet guarantees. Characterization takes place from -55°C to $+125^\circ\text{C}$ and a $+10\%$ supply voltage.

QA05

The QA05 system collects the results of product assurance testing on all finished goods lots and feeds this data back to concerned organizations where appropriate action can be taken. The QA05 reports EPA (Estimated Process Average) and AOQ (Average Outgoing Quality) results for electrical, visual/mechanical, hermeticity, and documentation audits. Data from this system is available on request.

THE SURE PROGRAM

The SURE (Systematic Uniform Reliability Evaluation) program audits/monitors products from all Signetics' divisions under a variety of accelerated environmental stress conditions. This program, first introduced in 1964, has evolved to suit changing product complexities and performance requirements.

The SURE III program has two major functions: long-term accelerated stress performance audit and a short-term accelerated stress monitor. In the case of logic products, samples are selected which represent all generic product groups in all wafer fabrication and assembly locations. A series of detailed specifications (3230-009X) defines the criteria by which sample selection and evaluation testing is conducted.

THE LONG-TERM AUDIT

One-hundred devices from each generic family are subjected to each of the following stresses every eight weeks:

- High Temperature Operating Life: $T_j = 150^\circ\text{C}$, 1000 hours, static biased or dynamic operation, as appropriate (worst-case bias configuration is chosen);
- High Temperature Storage: $T_j = 150^\circ\text{C}$, 1000 hours;
- Temperature-Humidity Biased Life: 85°C , 85% relative humidity, 1000 hours, static biased;
- Temperature Cycling (Air-to-Air): -65°C to $+150^\circ\text{C}$, 1000 cycles.

THE SHORT-TERM MONITOR

Every other week a 50-piece sample from each generic family is run to 168 hours of pressure pot (15 psig, 121°C , 100% saturated steam) and 300 cycles of thermal shock (-65°C to $+150^\circ\text{C}$).

In addition, each Signetics assembly plant performs SURE product monitor stresses weekly on each generic family and molded package, by pin count and frame type. Fifty pieces are run on each stress, in pressure pot to 96 hours, thermal shock to 300 cycles.

SURE REPORTS

The data from these test matrices provides a basic understanding of product capability, an estimated failure rate resulting from each stress, and an indication of major failure mechanisms. This data is compiled periodically and is available to customers upon request.

RELIABILITY ENGINEERING

In addition to the product performance monitors encompassed in the Logic SURE Program, Signetics' Corporate and Division Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering program are:

- evaluation and qualification of new or changed materials, assembly/wafer-fab processes and equipment, product designs, facilities and subcontractors;
- device or generic group failure rate studies;
- advanced environmental stress development;
- failure mechanism characterization.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE monitor; however, more highly accelerated conditions and extended durations typify the engineering projects. Additional stress systems such as biased pressure pot, power-temperature cycling, and cycle-biased temperature-humidity are also included in the evaluation programs.

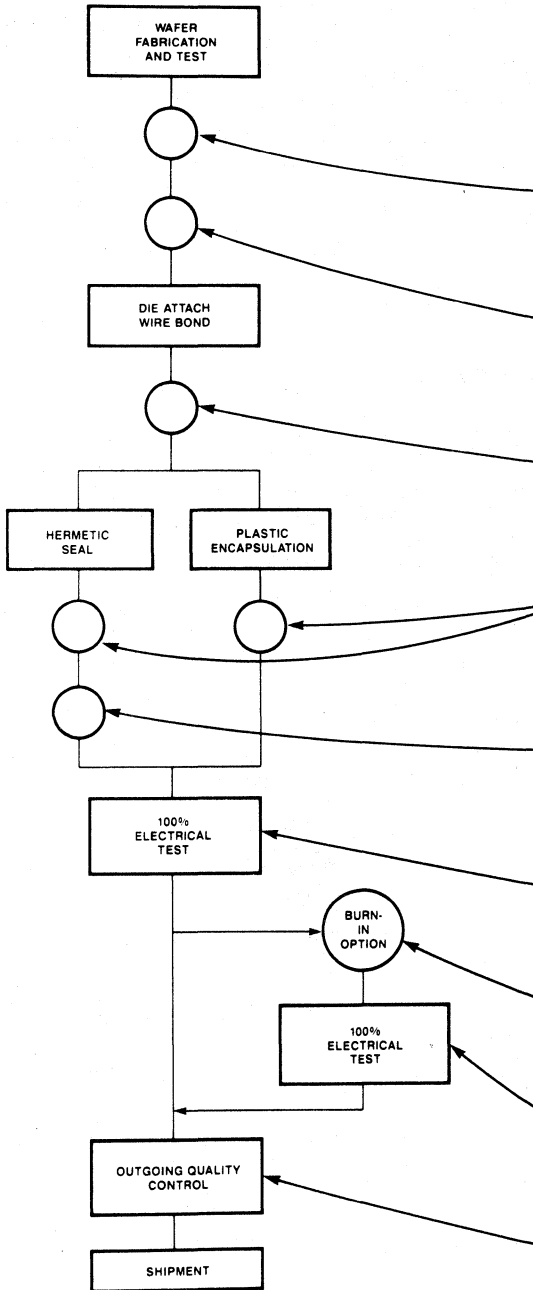
FAILURE ANALYSIS

The SURE Program and the Reliability Engineering Program both include failure analysis activities and are complemented by Corporate, Divisional, and Plant Failure Analysis departments. These engineering units provide a service to our customers who desire detailed failure analysis support, and they in turn provide Signetics with the technical understanding of the failure

QUALITY AND RELIABILITY

Process Flows

This diagram shows the process flow for all Signetics Logic integrated circuits. This includes TTL, Schottky, Low Power Schottky, Interface and FAST.



Scanning Electron Microscope Control (SEM)

Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

Die Sort Visual Acceptance

Product is inspected for defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Defects such as scratches, smears and glassivated bonding pads are included in the lot acceptance criteria.

Pre-Seal Visual Acceptance

Product is inspected to detect any damage incurred at the die attach and wire bonding stations. Defects such as scratches, contamination and smeared ball bonds are included in the lot acceptance criteria.

Symbolization

Devices are marked with the device number and date code using laser marking equipment. This prevents part number mixing during later processing steps.

Seal Tests

Package seal integrity is ensured by 100% fine and gross leak testing.

100% Production Electrical Testing

Every device is tested for functional and DC parameters at 25°C guard banded to assure performance over temperature. Selected product lines receive 100% AC testing. Product assurance sampling is performed at room, hot and cold temperatures and includes AC/DC and functionality.

Burn-In (Level B Option)

Devices are burned in for 21 hours. $T_j = 175^\circ\text{C}$ maximum.

100% Production Electrical Testing

Every device is tested for functional and DC parameters at 70°C. Selected product lines receive 100% AC testing. Product assurance sampling is performed at room, hot and cold temperatures and includes AC/DC functionality.

QA Guarantees

A final QA inspection step guarantees the mechanical and electrical quality. Every shipment is sealed and identified by QA personnel.

QUALITY AND RELIABILITY

modes and mechanisms actually experienced in service. This information is essential feedback, necessary for the continued assessment of the applicability of the stress conditions utilized to measure product performance.

ZERO DEFECTS PROGRAM

Industry Requires Improved Product Quality

In recent years United States industry, and particularly those of you who buy integrated circuits, has increasingly demanded improved product quality. We at Signetics believe you have every right to expect quality products. If you buy components from a quality conscious manufacturer, the reward can be summed up in the words, *lower cost of ownership*.

Those of you who invest in costly test equipment and engineering to assure that

incoming products meet your specifications have a special understanding of the cost of ownership. And your cost does not end there; you are also burdened with inflated inventories, lengthened lead times, and more rework.

Signetics Understands Customers' Needs

Signetics has long had an organization of quality professionals inside the operating units, coordinated by a corporate quality department. This organization provides leadership, feedback, and direction for

achieving our high level of quality. Special programs are targeted on specific quality issues. For example, a program to reduce electrically defective units improved outgoing quality levels by an order of magnitude.

In 1980 we recognized that in order to achieve outgoing levels on the order of 100 PPM (parts per million), down from an industry practice of 10,000 PPM, we needed to supplement our traditional quality programs with one that encompassed all activities and all levels of the company. Such unprecedented low defect levels could only be achieved by contributions from all employees, from the R&D laboratory to the shipping dock. In short, a program that would effect a total cultural change within Signetics in our attitude toward quality.

This new concept is based on the 14-step quality improvement program developed by Phil Crosby and outlined in his book *Quality is Free*. The program focuses on defect prevention as the means of attaining improved quality.

Quality Pays Off for Our Customers

Signetics' dedicated programs in product quality improvement, supplemented by close working relationships with many of our customers, have improved outgoing product quality more than twenty-fold. Today, many major customers no longer test Signetics circuits. Incoming product moves directly from the receiving dock to the production line, greatly accelerating throughput and reducing inventories. Additional customers have pared significantly the amount of sampling done on our products. Others are beginning to adopt these cost-saving practices.

We closely monitor the electrical, visual, and mechanical quality of all our products and review each return to find and correct the cause. Since 1981, over 90% of our customers report a significant improvement in overall quality.

At Signetics, quality means more than working circuits. It means on-time delivery of the *right* quantity of the *right* product at

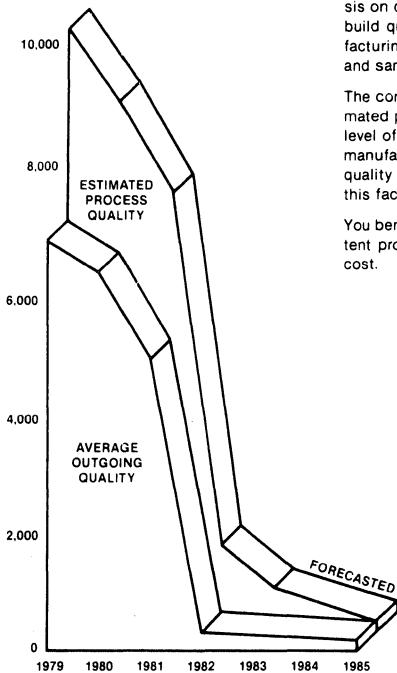
LOGIC PRODUCT QUALITY GOALS (1984-1986)

	ELECTRICAL	VISUAL/MECHANICAL	CUMULATIVE
1984 EPQ/AOQ Targets, PPM	150/100	500/250	650/350
1985 EPQ/AOQ Targets, PPM	100/50	300/100	400/150
1986 EPQ/AOQ Targets, PPM	50/10	100/50	150/60



This graph shows how dramatically electrical, mechanical, and visual defects have been reduced across all product lines.

Defective Parts Per Million



These improvements result from our emphasis on defect prevention which allows us to build quality into the product during manufacturing, instead of relying on screening and sampling to remove defective parts.

The corresponding improvement in the estimated process quality (which measures the level of defective units produced during the manufacturing process prior to outgoing quality assurance) conclusively supports this fact.

You benefit from improved and more consistent product conformance at lower product cost.

QUALITY AND RELIABILITY

the *agreed upon* price. Our quality improvement programs extend out from the traditional areas of product conformance into the administrative areas which affect order entry, scheduling, delivery, shipping, and invoicing.

Ongoing Quality Programs at Signetics

The "14-Step" Quality Improvement Program or "Do it Right the First Time"

The intent of this innovative program is to change the perception of Signetics' employees that somehow quality is solely a manufacturing issue where some level of defects is inevitable. This attitude has been replaced by one of acceptance of the fact that all errors and defects are preventable, a point of view shared by technical and administrative functions equally, and, we are sure, welcomed by our customers.

This program is company-wide and top down. It is personally led by President Charles Harwood who, with his staff, forms the corporate quality improvement team which implements corporate quality policy. Supporting the corporate quality improvement team are more than 40 quality improvement teams representing every unit in the company, each led by the unit manager.

Key components of the program are the Quality College, the "Make Certain" Program, Corrective Action Teams, and the Error Cause Removal System.

The core concepts of doing it right the first time are embodied in the four absolutes of quality:

1. The definition of quality is conformance to requirements.
2. The system to achieve quality improvement is prevention.
3. The performance standard is zero defects.
4. The measurement system is the cost of quality.

Quality College

Almost continuously in session, the Quality College is a prerequisite for all management and technical employees. The intensive two-day curriculum is built around the four "absolutes" of quality; colleges are conducted at company facilities throughout the world. More than 3000 employees have attended.

"Making Certain" — Administrative Quality Improvement

Signetics' experience has shown that the largest source of errors affecting product and service quality is found in paperwork and in other administrative functions. The "Make Certain" program focuses the attention of management and administrative personnel on error prevention, beginning with each employee's own actions.

This program promotes defect prevention in three ways: by educating employees as

to the impact and cost of administrative errors, by changing attitudes from accepting occasional errors to one of accepting a personal work standard of zero defects, and by providing a formal mechanism for preventing errors.

Corrective Action Teams

Employees with the perspective, knowledge, and necessary skills are formed into ad hoc groups called Correction Action Teams. These teams, the major force within the company for quality improvement, resolve administrative, technical and manufacturing problems.

Error Cause Removal (ECR) System

The ECR System permits our employees to report to management any impediment to doing their job right the first time. Once reported, management is obliged to respond promptly with a corrective program. Doing it right the first time in all company activities produces lower cost of ownership through product defect prevention and in all other ways meets our customers' expectations.

Product Quality Program

To reduce defects in outgoing products to nearly immeasurable levels, we created the Product Quality Program. This is managed by the Product Engineering Council, a task force composed of the top product engineering and test professionals in the company. This group:

1. Sets aggressive product quality improvement goals.
2. Provides corporate-level visibility and focuses on problem areas.
3. Serves as a corporate resource for any group requiring assistance in quality improvement.
4. Drives quality improvement projects.

As a result of this aggressive program, every major customer who reports back to us on product performance is reporting significant progress.

Standard Quality Programs

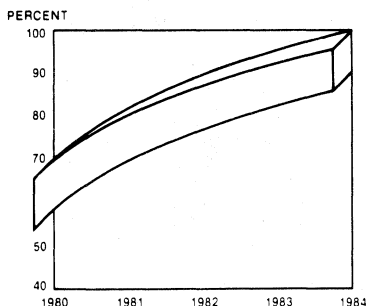
"SURE" — The acronym stands for **S**ystematic **U**niform **Q**uality **E**valuation and is an ongoing product evaluation first introduced in 1964. This activity provides our customers and us with an ongoing view of reliability performance of all generic families of Signetics' products.

Product Monitor — Each manufacturing facility monitors its generic product groups with short-term stress tests, pressure pot and thermal shock. These tests are performed weekly, and performance trends are

Performance to Schedule

Signetics' attention to administrative quality has resulted in improved performance to schedule. Doing it right the first time means on-time delivery.

On-Time Delivery



Signetics is Organized for Quality

Managing Cultural Change — The "14-Step" Program

- Quality College
- Quality Improvement Teams
- "Make Certain" Program
- Corrective Action Teams
- Error Cause Removal System

Engineering Quality into the Product

- SURE Program
- Manufacturing Plant Product Monitoring
- Qualification Programs
- Vendor Certification Programs
- Product Quality Program

Supporting Quality Maintenance

- Product Line
- Quality and Reliability Assurance
- Corporate Quality and Reliability
- Failure Analysis Laboratories
- Reliability Data Base
- Statistical Quality Control

QUALITY AND RELIABILITY

monitored to ensure that unwanted process deviations are spotted quickly and corrected before appearing in products received by our customers.

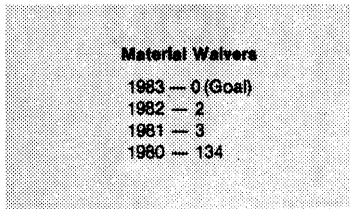
Qualification — Formal qualification procedures are required for all new or changed products, processes and facilities. These procedures ensure the high level of product reliability our customers expect. New facilities are qualified by the corporation and by the quality organizations of the product line that will operate the facility. After qualification, products manufactured by the new facility are subjected to highly accelerated environmental stresses to ensure that the products can meet rigorous failure rate requirements. New or changed processes are qualified similarly.

Failure Analysis — This vital function is conducted by product line and plant failure analysis units coordinated through the corporate failure analysis group, a part of corporate reliability engineering. Our ten failure analysis groups will be expanded to 16 by the end of 1984 in our ongoing effort to accelerate and improve our understanding of product failure mechanisms.

Reliability Data Base — This computerized data base contains product reliability information collected from around the world. It is updated and published quarterly in "Signetics Product Reliability Summary."

Many customers use this information in lieu of running their own qualification tests, thereby eliminating time-consuming and costly procedures.

Vendor Certification Program — Our vendors are taking ownership of their own product quality by establishing improved process control and inspection systems. They subscribe to the zero defects philosophy. Progress has been excellent. Through intensive work with vendors, we have improved our lot acceptance rate on incoming materials as shown in the graph. Simultaneously, waivers of incoming material have been eliminated.



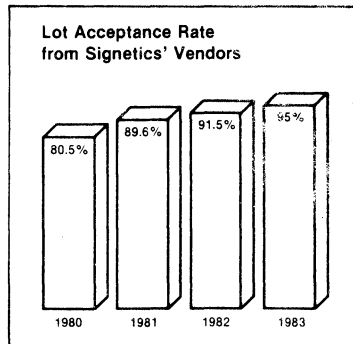
Higher incoming quality material to us ensures higher outgoing quality products for you.

Quality and Reliability Organization

Quality and reliability specialists at the product-line level are involved in all aspects of the product, from design through every step in the manufacturing process, and provide product assurance testing of outgoing product. A separate corporate-level group provides direction and common facilities.

Quality and Reliability Functions

- Manufacturing quality control
- Product assurance testing
- Laboratory facilities — failure analysis, chemical, metallurgy, thin film, oxides
- Environmental stress testing
- Quality and reliability engineering
- Customer liaison



Communicating with Each Other

For information on Signetics' quality programs or for any question concerning product quality, the field representative in your area will provide you with the quickest access to answers. Or, write on your letterhead directly to the Corporate Director of Quality at the corporate address shown at the back of this data manual.

We are dedicated to preventing defects. When product problems do occur, we want to know about them so we can eliminate their causes. We are committed to zero defects. Here are some ways we can help each other:

- Provide us with one informed contact within your organization. This will establish continuity and build confidence levels.
- Periodic face-to-face exchanges of data and quality improvement ideas between your engineers and ours can help prevent problems before they occur.
- Test correlation data is very useful. Line-pull information and field failure reports also help us improve product performance.
- Provide us with as much specific data on the problem as soon as possible to speed analysis and enable us to take corrective action.
- An advance sample of the devices in question can start us on the problem resolution before physical return of shipment.

This teamwork with you will allow us to achieve our mutual goal of improved product quality.

NOTES

Section 3

TTL User's Guide

TTL USER'S GUIDE

INTRODUCTION

The TTL Logic devices described in this data manual differ widely in function, complexity and performance, but their electrical input and output characteristics are very similar and are defined and tested to guarantee compatibility. The data sheets that make up this book cover four major categories of TTL circuits and a series of TTL compatible interface products.

The oldest TTL product category is the gold-doped double-diffused type which is made up of the 54/7400 family of devices. This family reflects the same performance ranges and differ only in functions and pin configuration.

The remaining two categories of products are fabricated with a non-saturating Schottky clamped transistor technique. The 54S/74S00 family of TTL products are very high performance, high power devices. The most popular TTL category is the 54LS/74LS Low Power Schottky family. These products feature the performance of the 54/74 family at about 1/4 the power.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages and currents as shown below.

OPERATING TEMPERATURE AND VOLTAGE RANGES

The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0 volts. Commercial grade parts are guaranteed to perform with a $\pm 5\%$ supply tolerance ($\pm 250\text{mV}$) over an ambient temperature range of 0°C to 70°C .

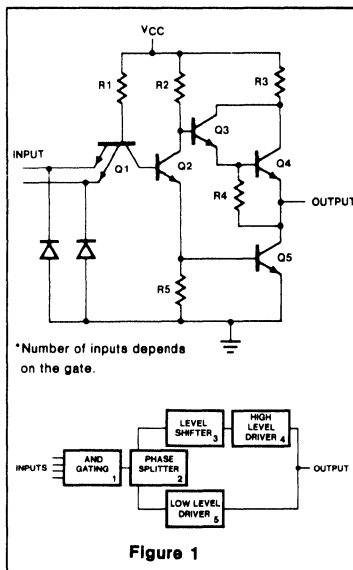
The Military grade parts are guaranteed to perform with a $\pm 10\%$ supply tolerance ($\pm 500\text{mV}$) over an ambient temperature range of -55°C to $+125^\circ\text{C}$.

The actual junction temperature can be calculated by multiplying the power dissipation of the device with the thermal resistance of the package and adding it to the measured ambient temperature T_A or package (case) temperature T_C . The thermal resistance for the various packages in which the TTL products are offered is specified with the Package Information in Section 7 of this manual.

GENERAL TTL CIRCUIT CHARACTERISTICS

All TTL products are derived from a common NAND logic structure. The NAND circuit is actually five subcircuits as shown in Figure 1 and each performs a separate function. The input circuit (1) is an AND gate usually fabricated with a multi-emitter transistor which characterizes TTL technology. Many Schottky processed circuits have been designed with PNP or diode inputs in order to optimize the speed/power performance of the circuits.

NAND Gate Example



The phase splitter (2) provides the inversion and amplification in the circuit. It determines whether the outputs are active level HIGH or active level LOW. The level shifter (3) provides noise immunity between the HIGH and LOW output levels, and minimizes the possibility of having both HIGH level driver (4) and LOW level driver (5) on simultaneously.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	54/74	54S/74S	54LS/74LS
V_{CC} supply voltage, continuous (Note a)	7.0V	7.0V	7.0V
Input voltage, continuous (Notes a and b)	-0.5V to +5.5V	-0.5V to +5.5V	-0.5V to +7.0V ^(b)
Input current, continuous	-30mA to +5mA	-30mA to +5mA	-30mA to +1mA
Voltage applied to HIGH outputs (Note a)	-0.5V to V_{CC}	-0.5V to 7.0V	-0.5V to V_{CC}
Voltage applied to "off" Open Collector outputs (Notes a and c)	-0.5V to 7.0V	-0.5V to 7.0V	-0.5V to 7.0V
Current into LOW standard output, continuous	30mA	40mA	15mA
Current into LOW buffer output, continuous	80mA	100mA	50mA
Operating free air temperature range (Mil)		-55°C to +125°C	
Operating free air temperature range (Com'l)		0°C to +70°C	
Storage temperature range		-65°C to +150°C	

NOTES

- a. Voltages are referenced to device ground terminal.
- b. LS devices are generally limited to 7.0V minimum input voltage. Exceptions are called out on individual product data sheets.
- c. Some open collector devices are specially processed to handle higher output voltages of from 15V to 30V. The Absolute Maximum voltage for these devices is 10% over the specified V_{OUT} test condition.

TTL USER'S GUIDE

TTL INPUT CONFIGURATIONS

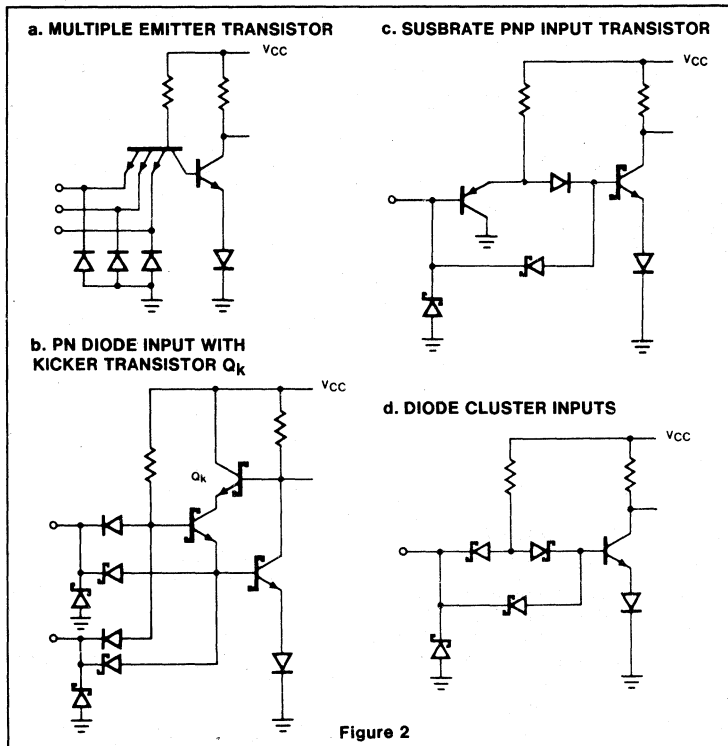


Figure 2

The level shifter (3) and HIGH level driver (4) combine to form an emitter follower circuit that tracks the voltage at the collector of the phase splitter. This circuit is usually designed to drive very heavy capacitive loads so that the initial rise time of the output is determined primarily by the rise time at the phase splitter collector. The LOW level driver (5) is usually a saturating transistor for the gold doped process devices, or a Schottky diode clamped transistor for the Schottky processed devices. These output transistors are designed to sink the rated fan-out current which characterizes the various TTL families.

Input Circuits

The input circuits as described above are basically AND gate configurations designed with multiple-emitter NPN transistors (MET), substrate PNP transistors, or various junction and Schottky diodes as shown in Figure 2. All of the circuit configurations have very high impedance in the HIGH state. When the input voltage is above the circuit threshold voltage, all of the inputs act like reversed biased diodes.

The MET transistors are actually operated in the inverse mode, but the gain is so low there is very little current flowing into the devices.

The LOW level input impedance of the MET and diode inputs is determined by the internal pull-up resistor. This resistor is nominally $2K\Omega$ for 54S/74S inputs, and it is $16K\Omega$ to $20K\Omega$ for the 54LS/74LS inputs. Some 54LS/74LS buffer devices have substrate PNP inputs which exhibit very high impedance at both HIGH and LOW input logic levels. This is used to minimize the input load factor and produce better output drive and performance.

The inputs to all Signetics TTL devices have clamp diodes to ground to minimize negative ringing effects. These diodes are designed to operate in the ac mode and cannot handle heavy dc currents for long periods.

Output Circuits

The output circuit configurations used for the TTL products in this manual are shown in Figure 3. The basic advantages and dis-

advantages of each configuration are given for reference. The different circuits are used to optimize the functional and performance requirements of the various devices, and are not necessarily restricted to individual TTL families. The pull-down circuit (not shown) on the base of the LOW level driver is usually a resistor which provides a means of turning off the output transistor. The majority of the 54S/74S and 54LS/74LS devices use a resistor-transistor network which acts to square-up the $V_{IN}-V_{OUT}$ transfer characteristics of the device.

A resistive pull-up can be added to any TTL output circuit increasing V_{OH} to almost V_{CC} , but only circuits "c," "d," and "e" can be pulled higher than V_{CC} , e.g., to +7.0V for driving MOS circuits. Configurations "a" and "b" have a diode associated with the resistor at the output which clamps the output one diode drop above V_{CC} . This is an important consideration in large systems where sections might be powered down ($V_{CC}=0$). In this state, the outputs of circuits "a" and "b" represent a very low impedance at a fairly low voltage ($<1.0V$), while the outputs of circuits "c," "d," and "e" represent a high impedance and thus a logic HIGH, more appropriate for isolation from the rest of the system.

The output impedance of a typical TTL device in both the LOW and HIGH state is shown in Figure 4. In the LOW state, the output impedance is determined by a saturated transistor (about 8Ω to 10Ω). However, at very high sinking current, especially at low temperature, the output device is not able to stay in saturation and the output impedance rises as shown.

When switching from the LOW to the HIGH state, the totem-pole output structure provides a low output impedance capable of rapidly charging capacitive loads. However, charge and discharge currents must also flow through the V_{CC} and the ground distribution networks. The V_{CC} and ground lines should therefore be short and adequately decoupled.

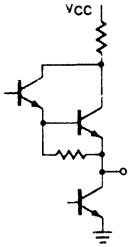
3-State Outputs

Some of the buffers and registers have 3-state outputs designed for "busing." This type of output electrically performs as a totem-pole output with the additional feature that the output may be disabled, neither sinking nor sourcing current. The 3-state outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from

TTL USER'S GUIDE

TTL OUTPUT CONFIGURATIONS

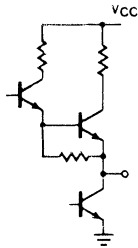
a. DARLINGTON



ADVANTAGE:
 High ac drive capability
 $V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$
 Small size (transistors share one common isolation)

DISADVANTAGE:
 Output cannot be pulled higher than one diode drop above V_{CC}

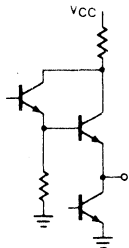
b. 2-STAGE EMITTER FOLLOWER ("DARLINGTON SPLIT")



ADVANTAGE:
 High ac drive capability
 $V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$

DISADVANTAGE:
 Larger than circuit A
 Output cannot be pulled higher than one diode drop above V_{CC}

c. DARLINGTON WITH RESISTOR TO GROUND



ADVANTAGE:
 High ac drive capability
 Lower $V_{OH} = (V_{CC} - 2 V_{BE})$ increases speed
 Outputs can be pulled higher than V_{CC}

DISADVANTAGE:
 Higher dissipation
 Lower noise immunity in the HIGH state

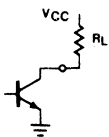
d. TRANSISTOR-DIODE



ADVANTAGE:
 Lowest power consumption
 Small size
 Outputs can be pulled higher than V_{CC}

DISADVANTAGE:
 Less ac drive capability

e. OPEN COLLECTOR



ADVANTAGE:
 Bussable, allows collector ANDING (Wired-OR)

DISADVANTAGE:
 High output impedance in the HIGH state
 Slow, especially with capacitive loading
 Requires additional resistor

Figure 3

TYPICAL INPUT / OUTPUT CHARACTERISTICS

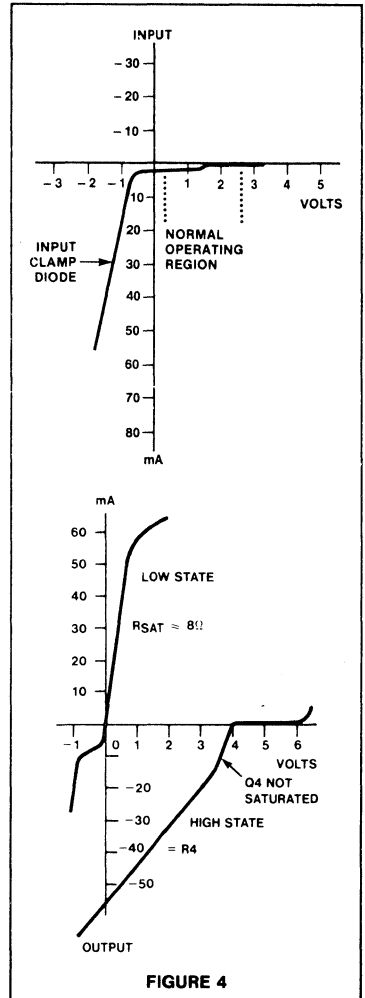


FIGURE 4

excessive power dissipation, only one 3-state output should be active at any time.

DESIGN CONSIDERATIONS

The properties of high speed TTL logic circuits dictate that some care be used in the design and layout of a system. Some general "design considerations" are included in this section. This is not intended to be a thorough guideline for designing TTL systems, but a reference for some of the constraints and techniques to be considered when designing the system.

TTL USER'S GUIDE

Mixing 54/74 and 54LS/74LS is less restrictive, and the overall system design need not be so elaborate. Standard two sided PC boards can be used with good, well decoupled power and ground grid systems. The signal transitions are slower and therefore generate less noise. However, good high speed design techniques are still required, especially when working with counters, registers, or other devices with memory.

Clock Pulse Requirements

Most TTL flip-flop circuits are master-slave devices which makes their clock inputs level sensitive. This is an improvement over ac coupled clock inputs, but it does not make the devices fully insensitive to clock edge rates. The dc level at which the data in the master (input section) is transferred to the slave (output section) is the normal threshold voltage for the devices. For most Signetics TTL devices this level is 1.4V at 25°C, and it changes at a rate of about -4mV/°C.

When the clock input reaches the threshold voltage, the internal gates and the changing outputs start to dump current into the ground lead of the device. If there are enough internal gates or loaded outputs changing at the same time, the chip ground reference level (and therefore the clock input reference level) can rise by as much as 500mV. This ground noise is the algebraic sum of the internal and external ground plane noise. If the clock input of a positive edge triggered device is at or near the threshold of the device during the ground noise transient period, it is quite possible for the internal device to receive multiple clock pulses.

For this reason the rise time on positive edge-triggered devices should be less than the nominal clock to output delay time measured between the 0.8V and 2.0V levels of the clock driver. This edge rate is obtainable from almost any Signetics TTL device of the same family, as long as it is driving no more than rated fan out and no more than 12 to 16 inches of line. When clock pulses are distributed on lines over 16 inches long, all of the clock inputs should be clustered at the receiving end of the line to avoid reflection problems at the driving end.

Special Note

Some of the Signetics Counters and registers have been designed with a special clock buffer that includes a small amount of hysteresis to minimize clock edge rate and noise problems. The LS160A, LS161A,

LS162A, LS163A, LS364, and LS374 all have the special clock buffers to increase their tolerance of slow positive clock edges and heavy ground noise.

TTL OUTPUTS TIED TOGETHER

The only TTL outputs that are designed to be tied together are open collector and 3-state outputs. Standard TTL outputs should not be tied together unless their logic levels will always be the same; either all HIGH or all LOW. When connecting open collector or 3-state outputs together some general guidelines must be observed:

Open Collector

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have a pull-up resistor (or resistors) added between the OR-tie connector and V_{CC} to establish an active HIGH level. Only special high voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of

the pull-up resistor is determined as follows:

$$R(\text{Min}) = \frac{V_{CC}(\text{Max}) - V_{OL}}{I_{OL} - N_2(I_{IL})}$$

$$R(\text{Max}) = \frac{V_{CC}(\text{Min}) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

where: I_{OL} = Minimum I_{OL} guarantee or OR-tied elements.

N₂(I_{IL}) = Cumulative maximum input LOW current for all inputs tied to OR-tie connection.

N₁(I_{OH}) = Cumulative maximum output HIGH leakage current for all outputs tied to OR-tie connection.

N₂(I_{IH}) = Cumulative maximum input HIGH leakage current for all inputs tied to OR-tie connection.

If a resistor divider network is used to provide the HIGH level, the R(Max) must be decreased enough to provide the required (V_{OH}/R(pull-down)) current.

Minimum propagation delay results when the minimum value of external pull-up resistor is used in Load Circuit 1, Figure 5.

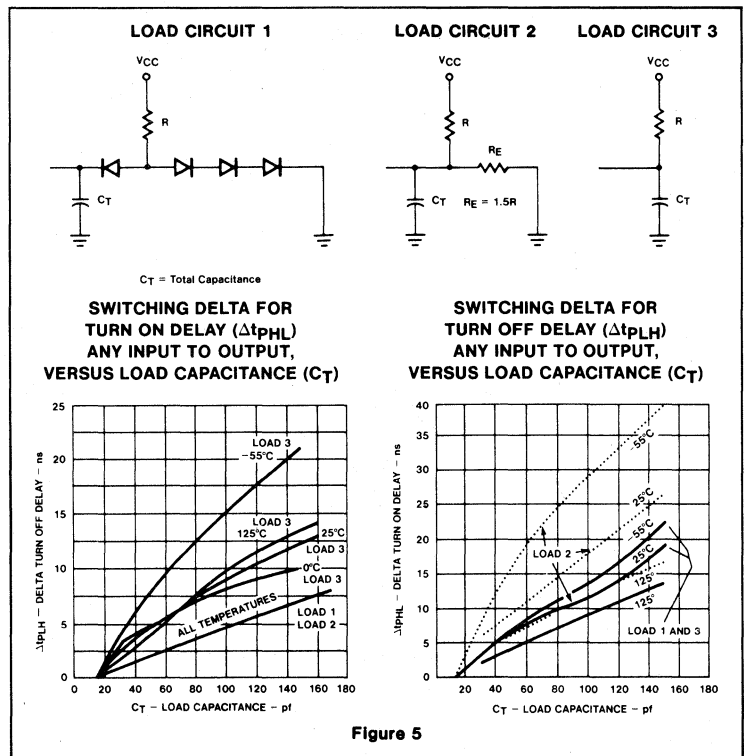


Figure 5

TTL USER'S GUIDE

Diodes should be fast recovery 1N4376 or equivalent. External pull-up resistor Load Circuits 2 and 3 give progressively slower propagation delays.

3-STATE OUTPUTS

3-State Outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-state output should be active at any time. This generally requires that the Output Enable signals be non-overlapping. When TTL decoders are used to enable 3-state outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally be guaranteed when the address is changing.

Since most 3-state Output Enable signals are active LOW, shift registers or edge-triggered storage registers provide good Output Enable buffers. Shift registers with one circulating LOW bit, like the "164" or "194" are ideal for sequential enable signals. The "174" or "273" can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from LOW-to-HIGH faster than from HIGH-to-LOW, the selection of one device at a time is assured.

POWER SUPPLY DECOUPLING

Power supply capacitance decoupling is required for any TTL system. Generally $0.01\mu\text{F}$ per synchronously driven gate and at least $0.1\mu\text{F}$ for each 20 gates is required regardless of synchronization. Counters and shift registers are especially susceptible to power and ground line noise. They should be decoupled with a $0.1\mu\text{F}$ capacitor for each eight internal flip-flops, or one capacitor for each two devices put as close as possible to the devices. Buffers and line drivers should be heavily decoupled at the driver power pins, due to

the large current transients needed to charge and discharge the lines.

On-Board Regulation

In most digital systems, there is a large current requirement, and the current supplied usually comes from a main supply. TTL logic tends to generate current spikes during switching due to the overlap in conduction of both upper and lower transistors, thus creating V_{CC} noise. An on-board regulator would not only regulate the power supplied to the circuits on-board, but also would isolate the noise otherwise propagated to the reset of the system. Systems designed using this technique would not need tight regulation on the main power supply.

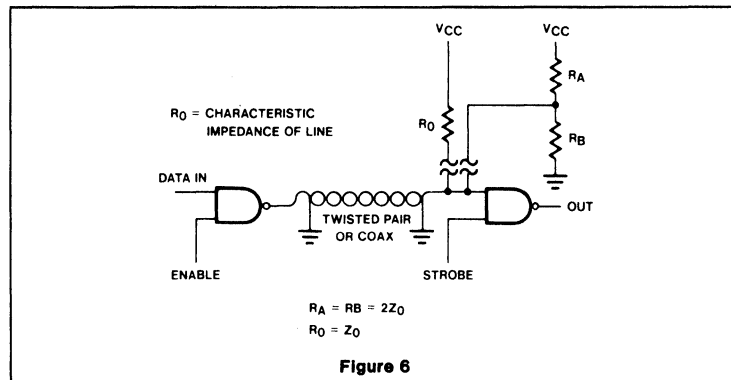
LINE DRIVING AND RECEIVING

Open wire connections between TTL circuits should not be bundled, tied, or routed together. Instead, point-to-point wiring should be used, preferably above a ground plane which reduces coupling between conductors.

Single line wire interconnections should not exceed two feet; for wires longer than

15 inches, a ground plane is essential to provide adequate system performance. Over 2-foot twisted pairs or coaxial cable should be used. The characteristic impedance of an open wire over a ground plane is about 150Ω , while for twisted pairs of #26 wire the impedance is about 120Ω . For added protection against crosstalk, coaxial cables can be used but coaxial cables having very low characteristic impedances are difficult to drive. For best performance, coaxial cables with a characteristic impedance R_0 of 100Ω should be used. Resistive pull-ups at the receiving end can be used to increase noise margins. If reflection effects are unacceptable, the line must be terminated in its characteristic impedance. One method is shown in Figure 6 where the output of the line is tied to V_{CC} through a resistor equivalent to the characteristic impedance of the line. Therefore, R_0 is fairly small, and the driving gate must sink the current through it in addition to the current from the inputs being driven. Terminating the line in a voltage divider with two resistors, each twice the line impedance, reduces the extra sink current by 50%. It is preferable to dedicate gates solely for line driving if the line length is in excess of five feet.

TTL DRIVING TWISTED PAIR



TTL USER'S GUIDE

Clamp Diode Effect on Negative Input Voltages

All Signetics TTL circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative dc voltages or long duration negative pulses especially for 54LS/74LS product. If the input voltage of an LS device is taken more than 0.5 volts negative (referenced to the device ground terminal) for more than 0.5 micro-seconds, it is possible to activate a parasitic circuit component which can cause the HIGH level output of that gate to degrade sufficiently to cause a logic error.

Disposition of Unused Inputs

Electrically open inputs degrade ac noise immunity as well as the switching speed of a circuit. To optimize performance, each input must be connected to a low impedance source. Unused active HIGH NOR or OR inputs must be returned to ground or a LOW level output. Unused active HIGH NAND or AND inputs should be maintained at a voltage greater than 2.7V, but not exceeding the Absolute Maximum Rating. This eliminates the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect the unused active LOW inputs of the TTL devices to ground. The active HIGH inputs should be tied through a resistor of from 1K to 10KΩ to V_{CC}. The unused active HIGH LS inputs can be tied directly to V_{CC}, as long as the leads are very short and the supply is adequately decoupled.
2. Connect the unused HIGH input to the output of an unused gate that is forced HIGH.
3. Tie unused NAND or AND inputs (multi-emitter inputs) of non-LS devices to a used input of the same gate, provided the HIGH level fan out of the driving circuit is not exceeded. Note that the LOW level fan out is not increased by this connection because the inputs share a common base pull-up resistor.

NOTE
For 54LS/74LS devices do *not* connect multiple inputs of a common gate together. This would increase the input coupling capacitance and reduce the ac noise immunity.

Unused Gates

It is recommended that the outputs of unused gates be forced HIGH by tying a NAND gate input or all NOR gate inputs to ground. This lowers the power dissipation and supplies a logic HIGH at the gate output which can be used at unused inputs to other gates.

Increasing Fan Out

To increase fan out, inputs and outputs of gates on the same package may be paralleled. It is advisable to limit the gates being paralleled to those in a single package to avoid large transient supply currents due to different switching times of the gates. This is not detrimental to the devices, but could cause logic problems if the gates are being used as clock drivers.

Isolation Diodes

NEVER REVERSE THE V_{CC} AND GROUND POTENTIALS. Catastrophic failure can occur if more than 100mA is conducted through a forward biased substrate (isolation) diode.

Input Loading and Output Drive Characteristics

The logic levels of all the TTL products are fully compatible with each other. However, the inputs loading and output drive characteristics of each of these families is different and must be taken into consideration when mixing the TTL families in a system. Table I shows the relative drive capabilities of each family for the Commercial temperature and voltage ranges. For Military ranges the 74LS drive capabilities must be cut in half. You will note that the 74LS Buffers have three times the drive capability of the standard 74LS devices; in fact, they can drive more loads than any other non-buffer TTL device.

Mixing TTL Families

Most TTL families are intended to be used together, but this cannot be done indiscriminately. Each family of TTL devices has unique input and output characteristics optimized to get the desired speed or power features. Fast devices like 54S/74S and 54/74F are designed with relatively low input and output impedances. The speed of these devices is determined primarily by fast rise and fall times internally as well as at the input and output nodes. These fast transitions cause noise of various types in the system. Power and ground line noise is generated by the large currents needed to charge and discharge the circuit and load capacitances during the switching transitions. Signal line noise is generated by the fast output transitions and the relatively low output impedances, which tend to increase reflections.

The noise generated by these 54S/74S and 54/74F devices can only be tolerated in systems designed with very short signal leads, elaborate ground planes, and good, well decoupled power distribution networks. Mixing the slower TTL families like 54/74 and 54LS/74LS with the higher speed families is also possible but must be done with caution. The slower speed families are more susceptible to induced noise than the higher speed families due to their higher input and output impedances. The low power Schottky 54LS/74LS family is especially sensitive to induced noise and must be isolated as much as possible from the 54S/74S and 54/74F devices. Separate or isolated power and ground systems are recommended, and the LS input signal lines should not run adjacent to lines driven by 54S/74S and 54/74F devices.

DRIVING DEVICE	NUMBER OF LOADS DRIVEN					
	74F	74LS	74	74S	8200 AND 9300	82500
74F	33	50	12.5	10	12	50
74F Buffer	106	160	40	32	40	160
74LS	13	20	5	4	5	20
*74LS Buffer	40	60	15	12	15	60
74	26	40	10	8	10	40
74 Buffer	78	120	30	24	30	120
74S	33	50	12.5	10	12	50
74S Buffer	100	150	37.5	30	37	150
8200 & 9300	26	40	10	8	10	40
82500	33	50	12	10	12	50

*The 74LS Buffers include 3-state outputs except LS253 & LS670

TTL USER'S GUIDE

DC SYMBOLS AND DEFINITIONS

Voltages - All voltages are referenced to ground. Negative voltage limits are specified as absolute values (i.e., $-10V$ is greater than $-1.0V$).

V_{CC}	Supply voltage: The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
V_{IK}	Input clamp voltage: The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.
V_{IH}	Input HIGH voltage: The range of input voltages recognized by the device as a logic HIGH.
$V_{IH}(\text{Min})$	Minimum Input HIGH voltage: This value is the guaranteed input HIGH threshold for the device. The minimum allowed input HIGH in a logic system.
V_{IL}	Input LOW voltage: The range of input voltages recognized by the device as a logic LOW.
$V_{IL}(\text{Max})$	Maximum Input LOW voltage: This value is the guaranteed input LOW threshold for the device. The maximum allowed input LOW in a logic system.
V_M	Measurement voltage: The reference voltage level on ac waveforms for determining ac performance. Usually specified as 1.5V for most TTL families, but 1.3V for the Low Power Schottky 54LS/74LS family.
$V_{OH}(\text{Min})$	Output HIGH voltage: The minimum guaranteed HIGH voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.
$V_{OL}(\text{Max})$	Output LOW voltage: The maximum guaranteed LOW voltage at an output terminal sinking the specified load current I_{OL} .
V_{T+}	Positive-going threshold voltage: The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below $V_{T-}(\text{Min})$.
V_{T-}	Negative-going threshold voltage: The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above $V_{T+}(\text{Max})$.

Currents—Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC}	Supply current: The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.
I_I	Input leakage current: The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.
I_{IH}	Input HIGH current: The current flowing into an input when a specified HIGH level voltage is applied to that input.
I_{IL}	Input LOW current: The current flowing out of an input when a specified LOW level voltage is applied to that input.
I_{OH}	Output HIGH current: The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.
I_{OL}	Output LOW current: The current flowing into an output which is in the LOW state.
I_{OS}	Output short-circuit current: The current flowing out of an output which is in the HIGH state when that output is short circuit to ground.
I_{OZH}	Output off current HIGH: The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.
I_{OZL}	Output off current LOW: The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

TTL USER'S GUIDE

AC SWITCHING PARAMETERS AND DEFINITIONS

f_{MAX}	The maximum clock frequency: The maximum input frequency at a clock input for predictable performance. Above this frequency the device may cease to function.	t_{PZL}	Output enable time to a LOW level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "off" state to the LOW level.
t_{PLH}	Propagation delay time: The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.	t_h	Hold time: The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.
t_{PHL}	Propagation delay time: The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.	t_s	Setup time: The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_{PHZ}	Output disable time from HIGH level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the HIGH level to a high impedance "off" state.	t_w	Pulse width: The time between the specified reference points on the leading and trailing edges of a pulse.
t_{PLZ}	Output disable time from LOW level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the LOW level to a high impedance "off" state.	t_{rec}	Recovery time: The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.
t_{PZH}	Output enable time to a HIGH level of a 3-state output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "off" state to the HIGH level.	t_{TLH}	Transition time: LOW to HIGH, the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW to HIGH.
		t_{THL}	Transition time: LOW to HIGH, the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from LOW to HIGH.
		t_r, t_f	Clock input rise and fall times: 10% to 90% value.

Section 4
54/74 Series

Quad Two-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7400	9ns	8mA
74LS00	9.5ns	1.6mA
74S00	3ns	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7400N • N74LS00N N74S00N	
Plastic SO	N74LS00D N74S00D	
Ceramic DIP		S5400F • S54LS00F S54S00F
Flatpack		S5400W • S54LS00W S54S00W
LLCC		S54LS00G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

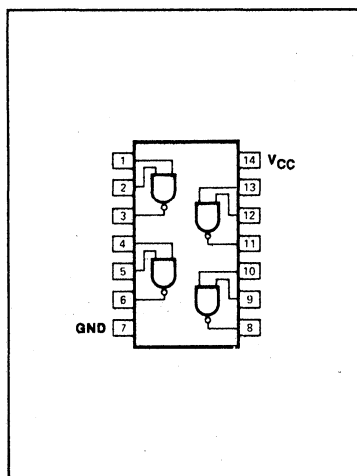
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

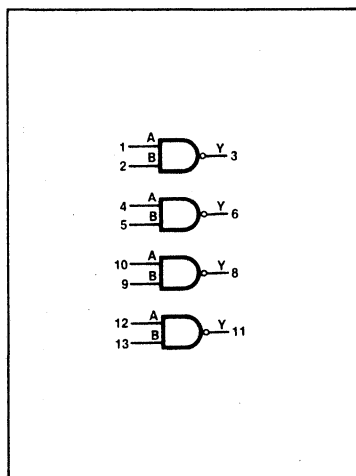
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1uI	1SuI	1LSuI
Y	Output	10uI	10SuI	10LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74S unit load (SuI) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

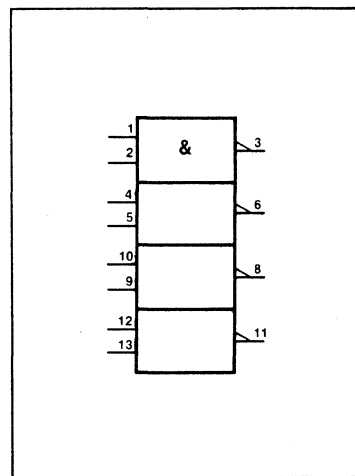
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



4

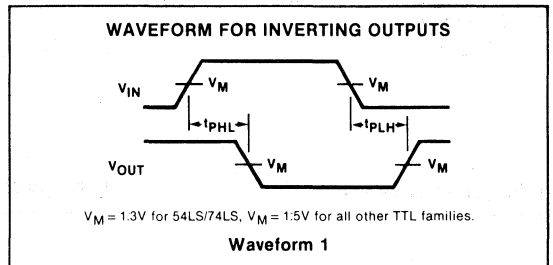
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7400			54/74LS00			54/74S00			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁴	V	
		Com'l		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA	74LS				0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5		-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA	
		V _I = 7.0V						0.1			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA	
		V _I = 2.7V						20		50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA	
		V _I = 0.5V								-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40		-100	mA
		Com'l	-18		-55	-20		-100	-40		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		4	8		0.8	1.6		10	16	mA
		I _{CCL} Outputs LOW		12	22		2.4	4.4		20	36	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay	Waveform 1		22		15		4.5	ns
t _{PHL}			15		15		5.0	

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-400			-400			-1000	μA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{PLH}, t_{PHL} Values should be less than or equal to the table entries.

V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{PLH}	t _{PHL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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Quad Two-Input NAND Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS01	16ns	1.6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS01N	
Plastic SO	N74LS01D	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

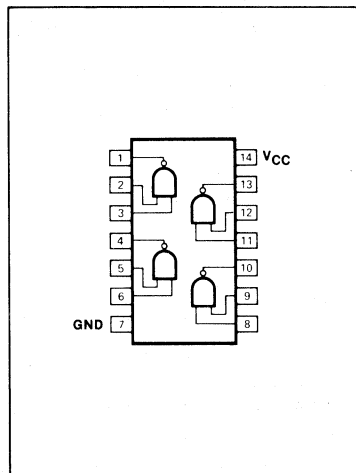
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

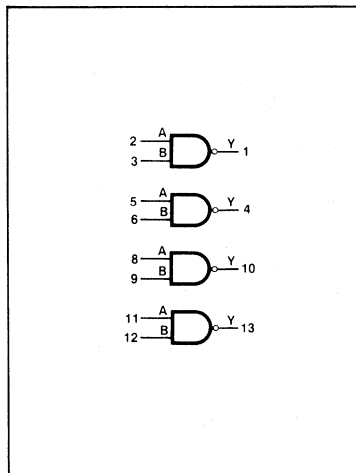
PINS	DESCRIPTION	54/74LS
A, B	Inputs	1LSul
Y	Output	10LSul

NOTE
Where a 54/74LS unit load (LSul) is $20\mu A$ I_{IH} and -0.4 mA I_{IL} .

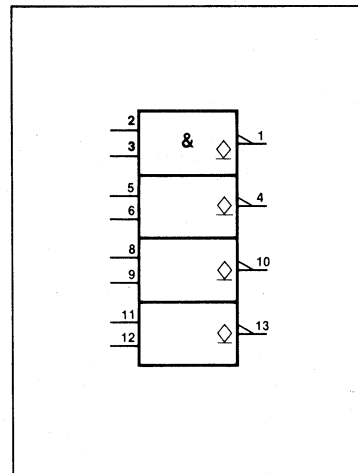
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I _{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

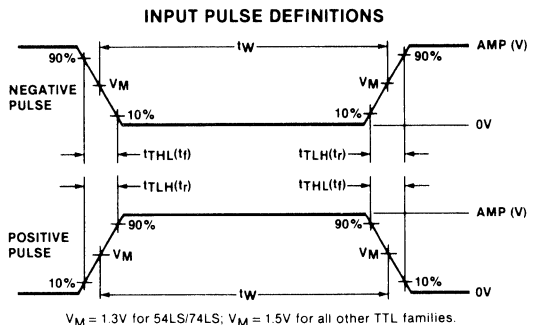
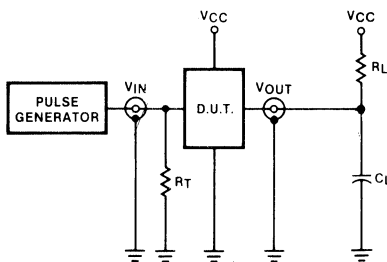
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l				+ 0.8
I _{IK}	Input clamp current				- 18	mA
V _{OH}	HIGH-level output voltage				5.5	V
I _{OL}	LOW-level output current	Mil			4	mA
		Com'l				8
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0			70

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

GATE

54/74LS01

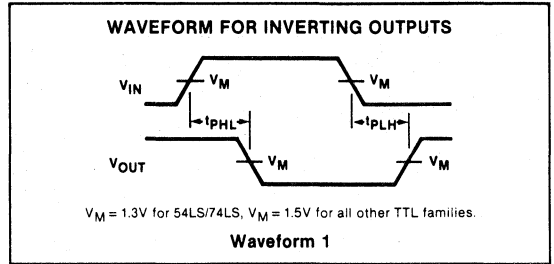
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS01			UNIT	
		Min	Typ ²	Max		
I_{OH}	HIGH-level output current $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5\text{V}$			100	μA	
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
		$I_{OL} = 4\text{mA}$	74LS	0.25	0.4	V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_1 = I_{IK}$			-1.5	V	
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			0.1	mA	
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA	
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-0.4	mA	
I_{CC}	Supply current (total) $V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		0.8	1.6	mA
		I_{CCL} Outputs LOW		2.4	4.4	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORM



AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Waveform 1		32 28	ns

Quad Two-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7402	10ns	11mA
74LS02	10ns	2.2mA
74S02	3.5ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7402N • N74LS02N N74S02N	
Plastic SO	N74LS02D • N74S02D	
Ceramic DIP		S54S02F • S54LS02F
Flatpack		S54S02W • S54LS02W
LLCC		S54LS02G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

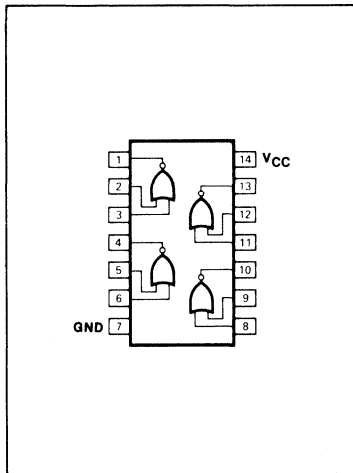
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

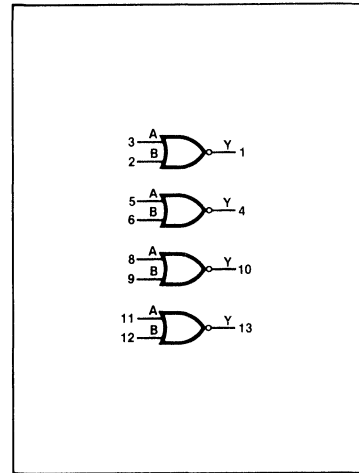
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50µA I_{IH} and -2.0mA I_{IL} , and 54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL} .

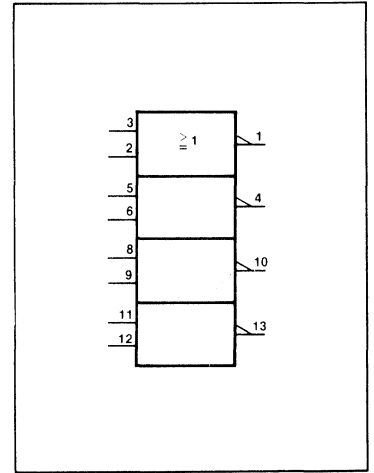
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

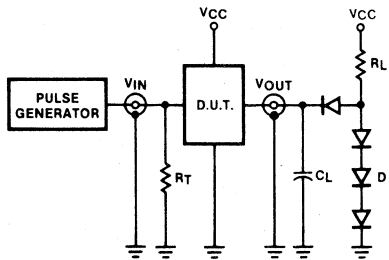
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			÷ 0.8			+ 0.7			+ 0.8	V
	Com'l			+ 0.8			+ 0.8			+ 0.8	V
I _{IK} Input clamp current				- 12			- 18			- 18	mA
I _{OH} HIGH-level output current				- 400			- 400			- 1000	µA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	- 55		+ 125	- 55		+ 125	- 55		+ 125	°C
	Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

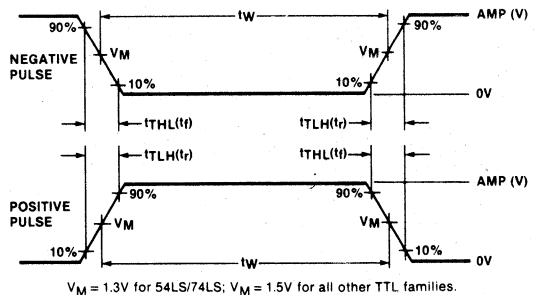
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{TTL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

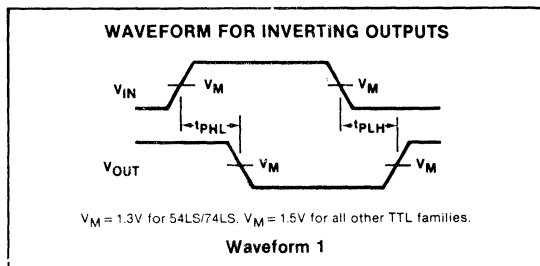
PARAMETER	TEST CONDITIONS ¹	54/7402			54/74LS02			54/74S02			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	Mil		0.2	0.4		0.25	0.4		0.5 ⁴	V	
		Com'l		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA	74LS				0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA	
		V _I = 7.0V					0.1				mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V		40							μA	
		V _I = 2.7V					20			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V		-1.6			-0.4				mA	
		V _I = 0.5V								-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40		-100	mA
		Com'l	-18		-55	-20		-100	-40		-100	mA
I _{CC} Supply Current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		8	16		1.6	3.2		17	29	mA
		I _{CCL} Outputs LOW		14	27		2.8	5.4		26	45	mA

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NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 15		15 15		5.5 5.5	ns

Quad Two-Input NAND Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7403	35ns (t_{PLH}) 8ns (t_{PHL})	8mA
74S03	5ns (t_{PLH}) 4.5ns (t_{PHL})	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7403N • N74S03N	
Plastic SO	N74S03D	
Ceramic DIP		S5403F
Flatpack		S5403W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

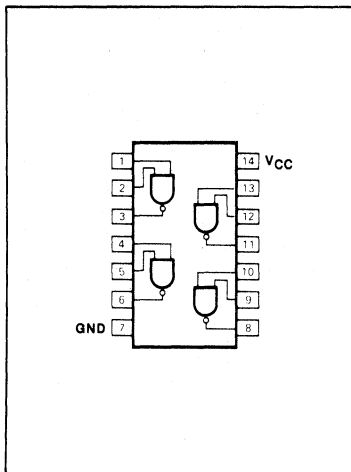
PINS	DESCRIPTION	54/74	54/74S
A, B	Inputs	1uI	1SuI
Y	Output	10uI	10SuI

H = HIGH voltage level
L = LOW voltage level

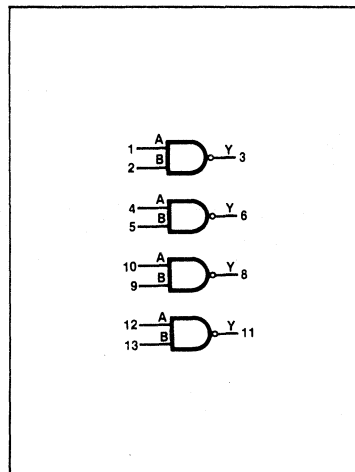
NOTE

Where a 54/74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 54/74S unit load (SuI) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

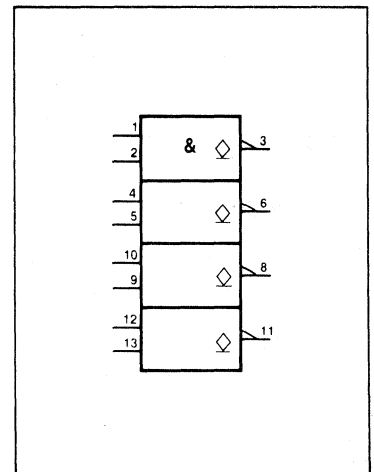
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54S	74	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +5	-30 to +5	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125		0 to 70		°C

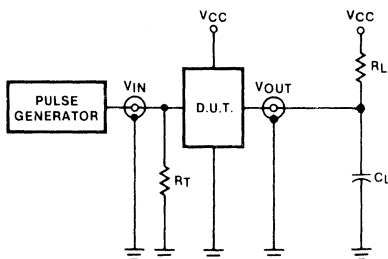
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0		2.0				V
V _{IL}	LOW-level input voltage	Mil			+0.8			+0.8	V
		Com'l			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA	
V _{OH}	HIGH-level output voltage			5.5			5.5	V	
I _{OL}	LOW-level output current	Mil			16			20	mA
		Com'l			16			20	mA
T _A	Operating free-air temperature	Mil	-55		+125	-55		+125	°C
		Com'l	0		70	0		70	°C

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TEST CIRCUITS AND WAVEFORMS

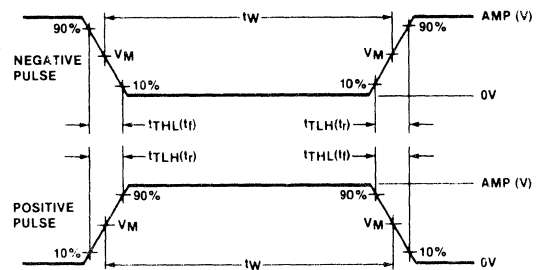
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{PLH}, t_{PHL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{PLH}	t _{PHL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

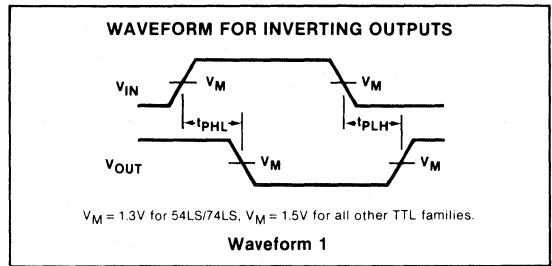
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7403			54/74S03			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
I_{OH}	HIGH-level output current $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5\text{V}$			250			250	μA
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	Mil	0.2	0.4			0.5	V
		Com'l	0.2	0.4			0.5	V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5			-1.2	V
I_I	Input current at maximum input voltage $V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0			1.0	mA
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$		40				μA
		$V_I = 2.7\text{V}$					50	μA
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$		-1.6				mA
		$V_I = 0.5\text{V}$					-2.0	mA
I_{CC}	Supply current (total) $V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	4	8	6	13.2	mA	
		I_{CCL} Outputs LOW	12	22	20	36	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORM



AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74S		UNIT
		$C_L = 15\text{pF}, R_L = 400\Omega$		$C_L = 15\text{pF}, R_L = 280\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	For 54/7403 only, $R_L = 4\text{k}\Omega$ for t_{PLH} . Waveform 1		45 15		7.5 7.0	ns

INVERTERS

54/7404, LS04, S04

Hex Inverter

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7404	10ns	12mA
74LS04	9.5ns	2.4mA
74S04	3ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7404N • N74LS04N N74S04N	
Plastic SO	N74LS04D • N74S04D	
Ceramic DIP		S5404F • S54LS04F S54S04F
Flatpack		S5404W • S54LS04W S54S04W
LLCC		S54LS04G

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FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

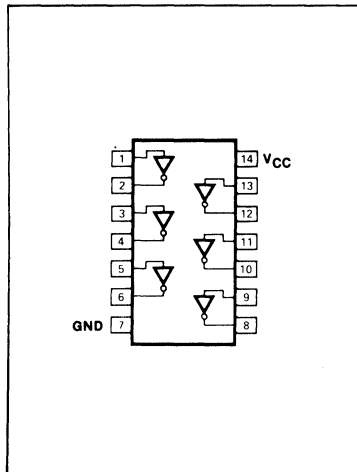
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

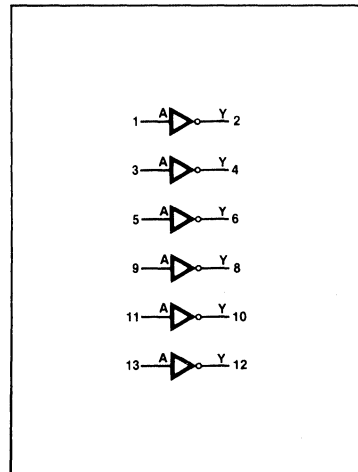
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A	Input	1uI	1Sul	1LSul
Y	Output	10uI	10Sul	10LSul

NOTE
Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50µA I_{IH} and -2.0mA I_{IL} , and 54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL} .

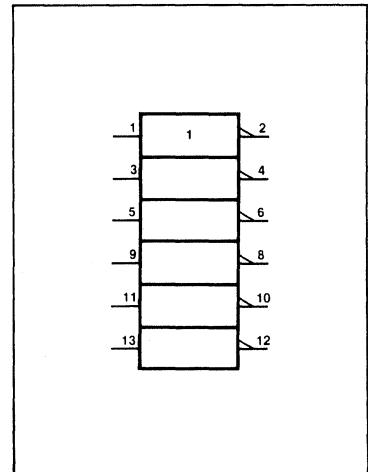
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



INVERTERS

54/7404, LS04, S04

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

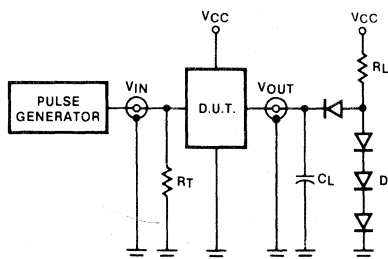
RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74			54/74LS			54/74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-400			-400			-1000	µA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

NOTE
 V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

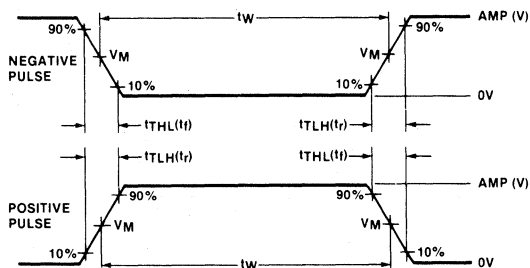
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 †T_{TLH}, †T_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS. V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	†T _{TLH}	†T _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

INVERTERS

54/7404, LS04, S04

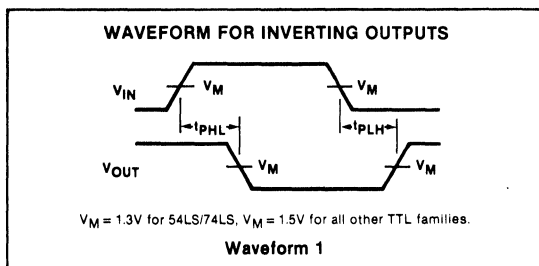
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7404			54/74LS04			54/74S04			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁴	V
			Com'l			0.2	0.4		0.35	0.5		0.5
		I _{OL} = 4mA	74LS						0.25	0.4		
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA
		V _I = 7.0V						0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40							μA
		V _I = 2.7V						20			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4				mA
		V _I = 0.5V									-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40		-100	mA
		Com'l	-18		-55	-20		-100	-40		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		6	12		1.2	2.4		15	24	mA
		I _{CCL} Outputs LOW		18	33		3.6	6.6		30	54	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 15		15 15		4.5 5.0	ns

INVERTERS

54/7405, LS05, S05

Hex Inverter (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7405	40ns (t _{PLH}) 8ns (t _{PHL})	12mA
74LS05	17ns (t _{PLH}) 15ns (t _{PHL})	2.4mA
74S05	5ns (t _{PLH}) 4.5ns (t _{PHL})	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = - 55°C to + 125°C
Plastic DIP	N7405N • N74LS05N N74S05N	
Plastic SO	N74LS05D • N74S05D	
Ceramic DIP		

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

H = HIGH voltage level
L = LOW voltage level

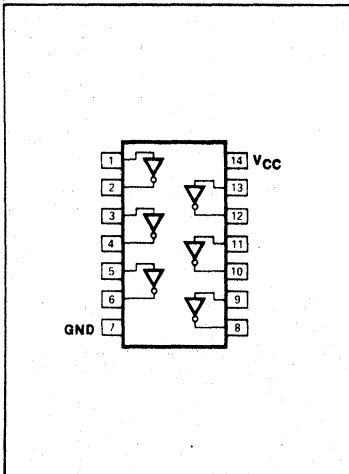
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A	Input	1uI	1SuI	1LSuI
Y	Output	10uI	10SuI	10LSuI

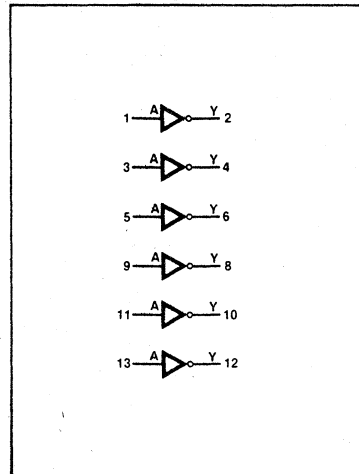
NOTE

Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and - 1.6mA I_{IL}, a 54/74S unit load (SuI) is 50µA I_{IH} and - 2.0mA I_{IL}, and 54/74LS unit load (LSuI) is 20µA I_{IH} and - 0.4mA I_{IL}.

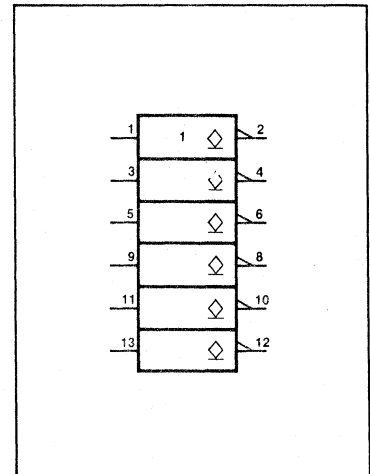
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



INVERTERS

54/7405, LS05, S05

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

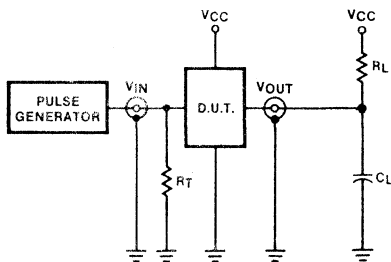
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
V _{OH} HIGH-level output voltage				5.5			5.5			5.5	V
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

4

TEST CIRCUITS AND WAVEFORMS

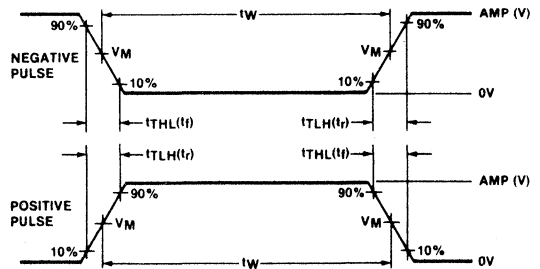
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

INVERTERS

54/7405, LS05, S05

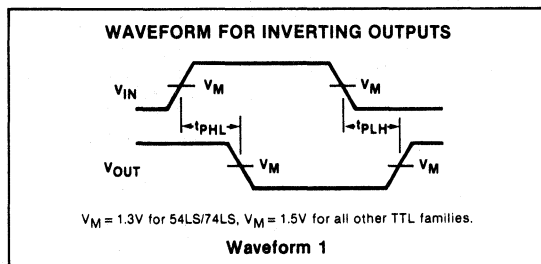
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹			54/7405			54/74LS05			54/74S05			UNIT
				Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5\text{V}$					250			100			250	μA
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$	Mil	0.2	0.4		0.25	0.4				0.5	V
			Com'l	0.2	0.4		0.35	0.5				0.5	V
			$I_{OL} = 4\text{mA}$				0.25	0.4					
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.5			-1.5			-1.2	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$			1.0						1.0	mA	
		$V_I = 7.0\text{V}$						0.1					mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$			40							μA	
		$V_I = 2.7\text{V}$						20			50	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$			-1.6			-0.4				mA	
		$V_I = 0.5\text{V}$									-2.0	mA	
I_{CC} Supply Current (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		6	12		1.2	2.4		9	19.8	mA	
		I_{CCL} Outputs LOW		18	33		3.6	6.6		30	54	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORM



AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		$C_L = 15\text{pF}, R_L = 400\Omega$		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}, R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	For 54/7405 only, $R_L = 4\text{k}\Omega$ for t_{PLH} . Waveform 1		55 15		32 28		7.5 7.0	ns

INVERTER/BUFFER/DRIVERS

54/7406, 07

'06 Hex Inverter Buffer/Driver (Open Collector)
'07 Hex Buffer/Driver (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7406	10ns (t_{PLH}) 15ns (t_{PHL})	31mA
7407	6ns (t_{PLH}) 20ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7406N • N7407N	
Plastic SO	N7406D • N7407D	

FUNCTION TABLE

'06		'07	
INPUT	OUTPUT	INPUT	OUTPUT
A	Y	A	Y
H	L	H	H
L	H	L	L

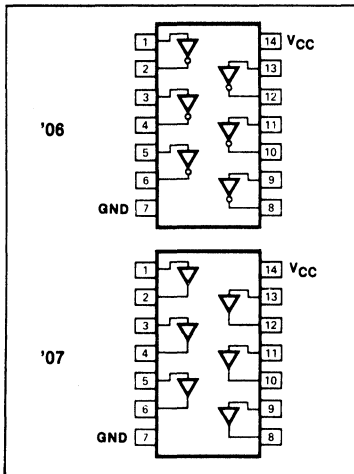
H = HIGH voltage level
 L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

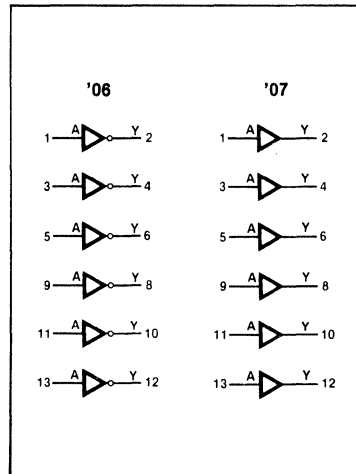
PINS	DESCRIPTION	54/74
A	Input	1uI
Y	Output	10uI

NOTE
 Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.8mA I_{IL}$.

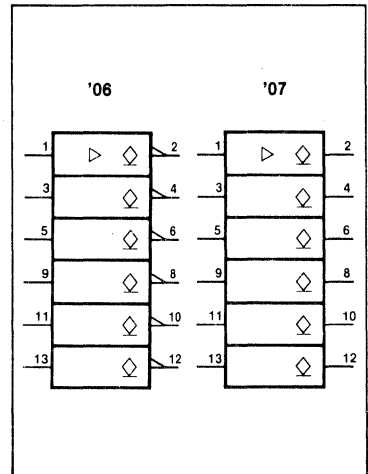
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



INVERTER/BUFFER/DRIVERS

54/7406, 07

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

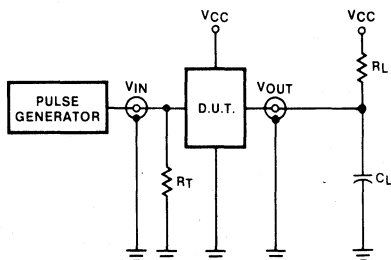
PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I_{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + 30	- 0.5 to + 30	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				- 12	mA
V_{OH}	HIGH-level output voltage				30	V
I_{OL}	LOW-level output current	Mil			30	mA
		Com'l			40	mA
T_A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

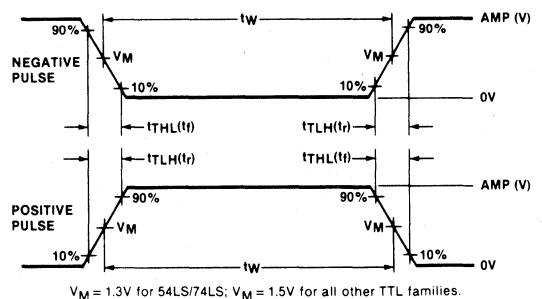
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

INVERTER/BUFFER/DRIVERS

54/7406, 07

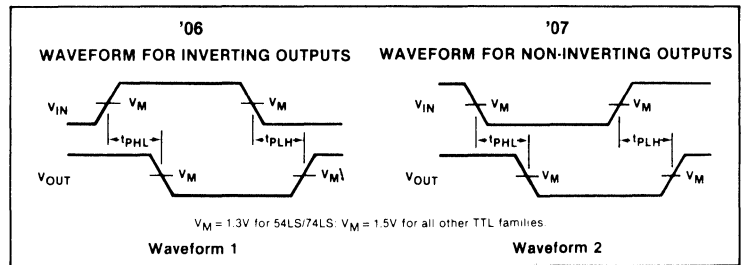
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7406, 54/7407			UNIT	
		Min	Typ ²	Max		
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 30\text{V}$			250	μA	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = 16\text{mA}$		0.4	V	
		$I_{OL} = 30\text{mA}$	Mil	0.7	V	
		$I_{OL} = 40\text{mA}$	Com'l	0.7	V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6	mA	
I_{CC} Supply current (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	'06	30	48	mA
				I_{CCL} Outputs LOW	32	51
		I_{CCH} Outputs HIGH	'07	29	41	mA
				I_{CCL} Outputs LOW	21	30

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORMS



AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/7406		54/7407		UNIT
		$C_L = 15\text{pF}, R_L = 110\Omega$		$C_L = 15\text{pF}, R_L = 110\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1, '06 Waveform 2, '07		15		10	ns
			23		30	

4

GATES

54/7408, LS08, S08

Quad Two-Input AND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7408	15ns	16mA
74LS08	9ns	3.4mA
74S08	5ns	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7408N • N74LS08N N74S08N	
Plastic SO	N74LS08N • N74S08N	
Ceramic DIP		S54S08F • S54LS08F
Flatpack		S54S08W • S54LS08W
LLCC		S54LS08G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

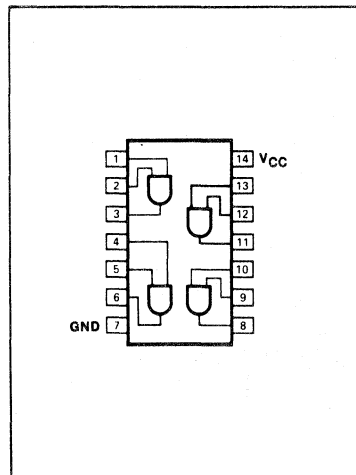
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

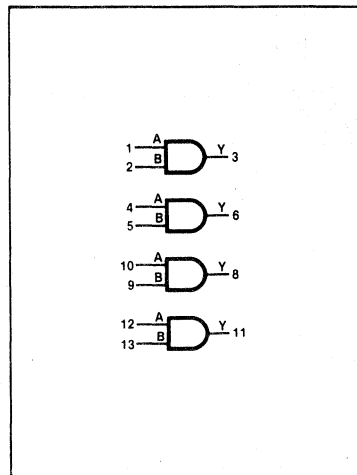
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1uI	1Sul	1LSul
Y	Output	10uI	10Sul	10LSul

NOTE
Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

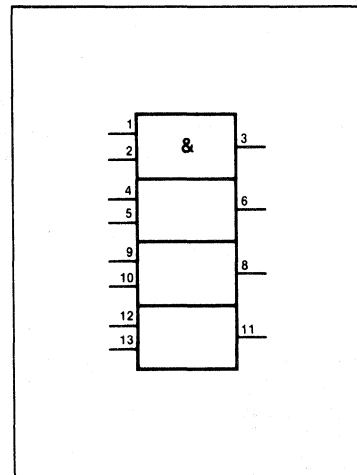
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

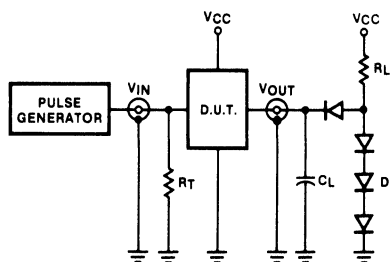
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-800			-400			-1000	μA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

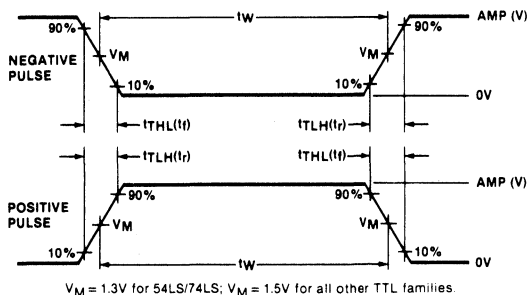
NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

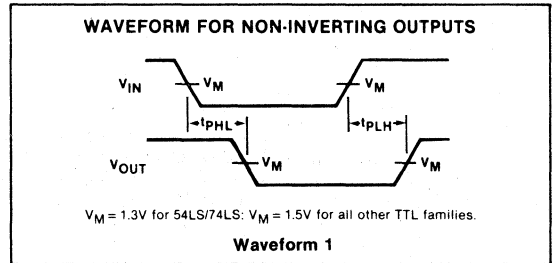
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7408			54/74LS08			54/74S08			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.25	0.4		0.5 ⁴	V	
		I _{OL} = 4mA	Com'l		0.2	0.4		0.35	0.5		0.5	V
			74LS					0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5		-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA	
		V _I = 7.0V						0.1			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA	
		V _I = 2.7V						20		50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA	
		V _I = 0.5V								-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40	-100	mA	
		Com'l	-18		-55	-20		-100	-40	-100	mA	
I _{CC} Supply Current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		11	21		2.4	4.8		18	32	mA
		I _{CCL} Outputs LOW		20	33		4.4	8.8		32	57	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		27 19		15 20		7.0 7.5	ns

**Quad Two-Input AND Gate
(Open Collector)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS09	23ns	4.3

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74LS09N

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH voltage level
L = LOW voltage level

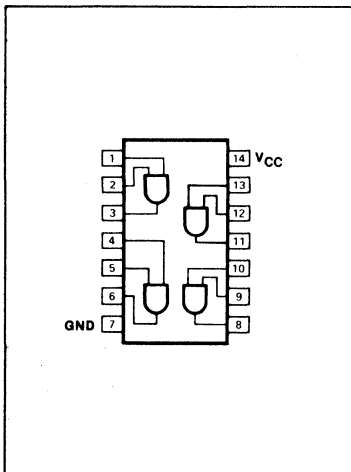
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
A, B	Inputs	1LSul
Y	Output	10LSul

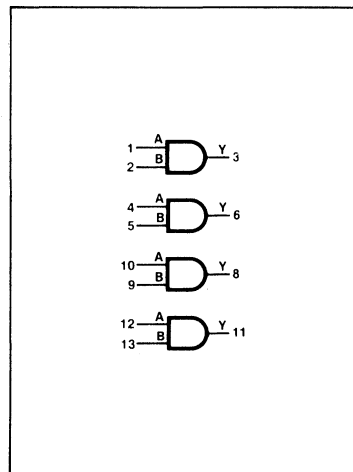
NOTE
Where 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

4

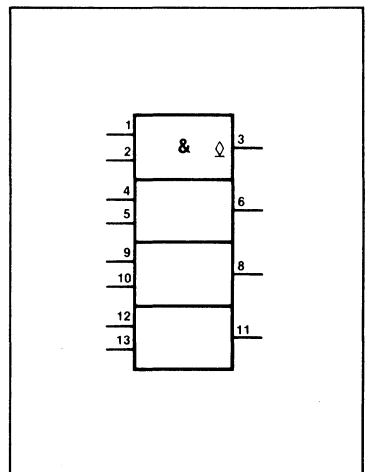
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

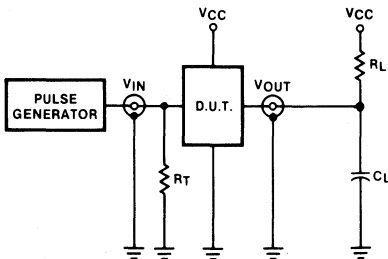
PARAMETER		74LS	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V _{CC}	Supply voltage	Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Com'l			+ 0.8	V
I _{IK}	Input clamp current				-18	mA
I _{OH}	HIGH-level output voltage				-400	μA
I _{OL}	LOW-level output current	Com'l			8	mA
T _A	Operating free-air temperature	Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

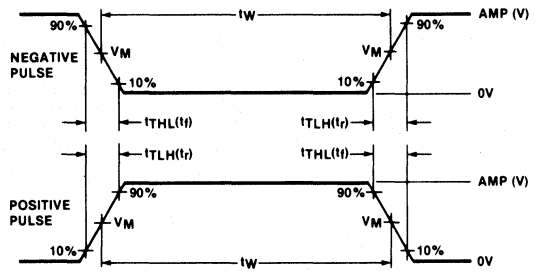
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

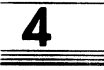
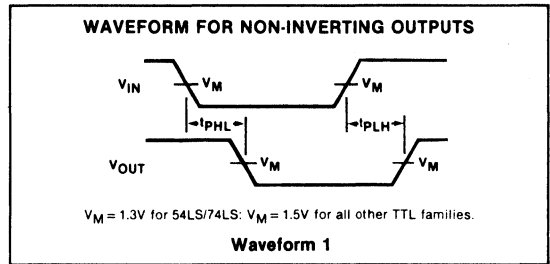
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74LS09			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OH} = MAX Com ¹	2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OL} = 4mA		0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = 18mA			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX			-100	mA
I _{CC} Supply Current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH	2.4	4.8	mA
		I _{CCL} Outputs LOW	4.4	8.8	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL}	Propagation delay	Waveform 1	35 35	ns

GATES

54/7410, 54/7411, LS10, LS11, S10, S11

Triple Three-Input NAND ('10), AND ('11) Gates

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7410	9ns	6mA
74LS10	10ns	1.2mA
74S10	3ns	12mA
7411	10ns	11mA
74LS11	9ns	2.6mA
74S11	5ns	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP '10	N7410N • N74LS10N • N74S10N	
'11	N74111N • N74LS111N • N74S111N	
Plastic SO '10	N74LS10D • N74S10D	
Plastic SO '11	N74LS11D • N74S11D	
Ceramic DIP '10		S54S10F • S54LS10F
'11		S5411F • S54S11F
Flatpack '10		S54S10W • S54LS10W
'11		S5411W • S54S11W
LLCC '10		S54LS10G

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y('10)	Y('11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

H = HIGH voltage level
L = LOW voltage level

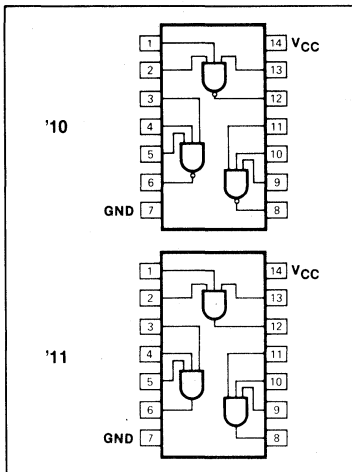
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A-C	Inputs	1uI	1SuI	1LSuI
Y	Output	10uI	10SuI	10LSuI

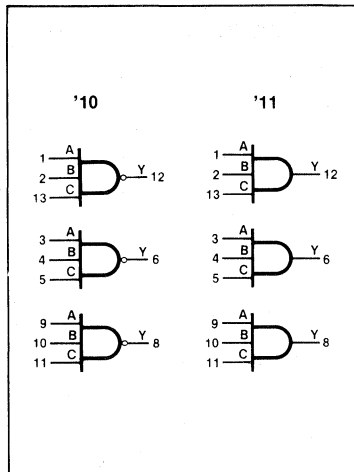
NOTE

Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL}, a 54/74S unit load (SuI) is 50µA I_{IH} and -2.0mA I_{IL}, and 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL}.

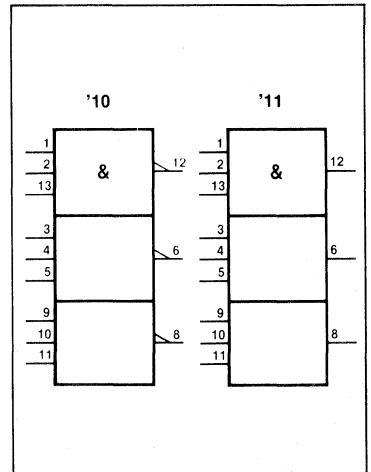
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



GATES

54/7410, 54/7411, LS10, LS11, S10, S11

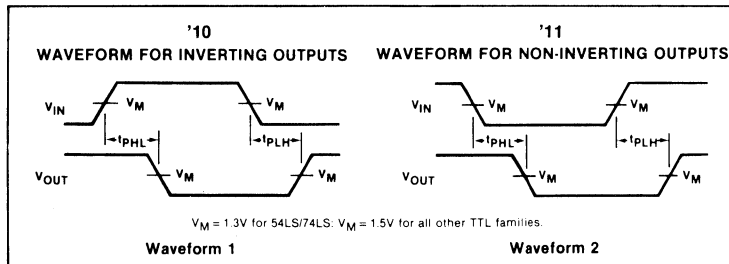
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7410, 11			54/74LS10, 11			54/74S10, 11			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁴	V	
			Com'l			0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5		-1.2	V		
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA		
		V _I = 7.0V						0.1			mA		
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA		
		V _I = 2.7V						20		50	μA		
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA		
		V _I = 0.5V								-2.0	mA		
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40	-100	mA		
		Com'l	-18		-55	-20		-100	-40	-100	mA		
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH	'10		3	6		0.6	1.2		7.5	12	mA
				I _{CCL} Outputs LOW		9	16.5		1.8	3.3		15	27
		I _{CCH} Outputs HIGH	'11		6	12		1.8	3.6		13.5	24	mA
				I _{CCL} Outputs LOW		15	20		3.3	6.6		24	42

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1, '10		22 15		15 15		4.5 5.0	ns
t _{PLH} t _{PHL} Propagation delay	Waveform 2, '11		27 19		15 20		7.0 7.5	ns

Dual 4-Input NAND Schmitt Trigger

DESCRIPTION

The '13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX} , the gate will respond in the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7413	17ns	17mA
74LS13	17ns	3.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7413N • N74LS13N	
Ceramic DIP		S54LS13F
Flatpack		S54LS13W

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

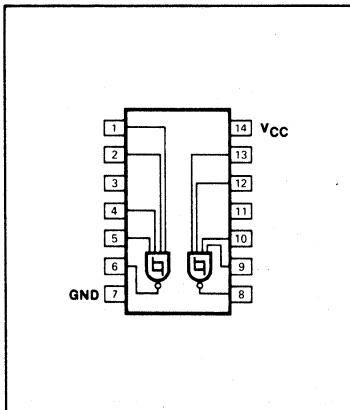
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

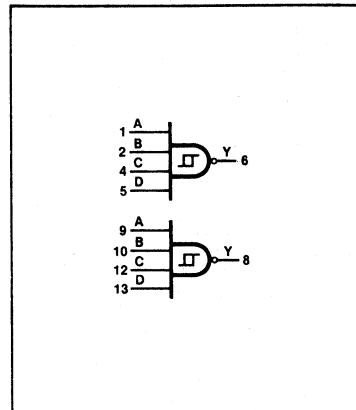
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

NOTE
 Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and -0.4mA I_{IL} .

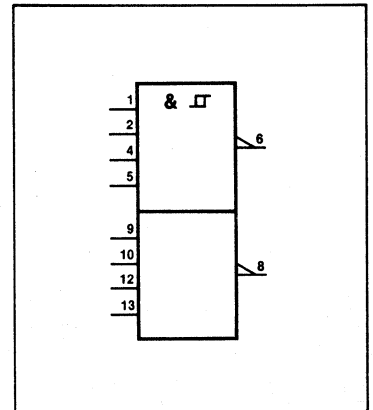
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
I _{IK}	Input clamp current			-12			-18	mA	
I _{OH}	HIGH-level output current			-800			-400	μA	
I _{OL}	LOW-level output current	Mil		16			4	mA	
		Com'l		16			8	mA	
T _A	Operating free-air temperature	Mil	-55	+125	-55		+125	°C	
		Com'l	0	70	0		70	°C	

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

GATES

54/7413, LS13

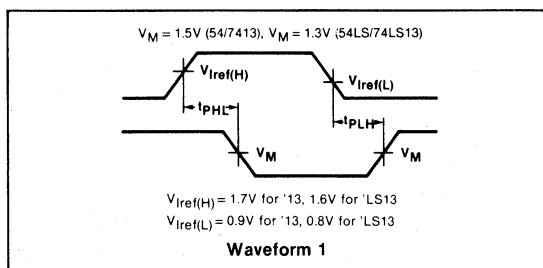
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7413			54/74LS13			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{T+} Positive-going threshold	V _{CC} = 5.0V	1.5	1.7	2.0	1.4	1.6	1.9	V		
V _{T-} Negative-going threshold	V _{CC} = 5.0V	0.6	0.9	1.1	0.5	0.8	1.0	V		
ΔV _T Hysteresis (V _{T+} - V _{T-})	V _{CC} = 5.0V	0.4	0.8		0.4	0.8		V		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _I = V _{T-} - MIN, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		V	
		Com'l	2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _I = V _{T+} + MAX	Mil		0.2	0.4		0.25	0.4	V	
		Com'l			0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}						-1.5	V		
I _{T+} Input current at positive-going threshold	V _{CC} = 5.0V, V _I = V _{T+}			-0.65			-0.14	mA		
I _{T-} Input current at negative-going threshold	V _{CC} = 5.0V, V _I = V _{T-}			-0.85			-0.18	mA		
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA		
		V _I = 7.0V					0.1	mA		
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40			μA		
		V _I = 2.7V					20	μA		
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V						-1.6	mA		
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	mA	
		Com'l	-18		-55	-20		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		14	23		2.9	6	mA	
		I _{CCL} Outputs LOW		20	32		4.1	7	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM

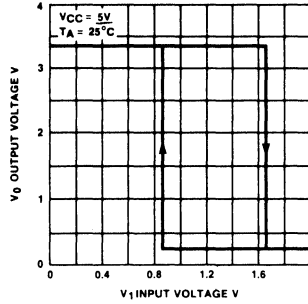


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

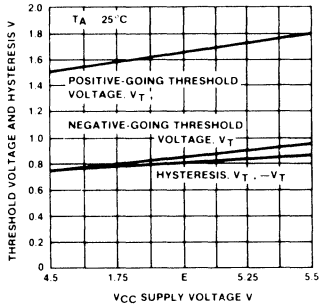
PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		27 22		22 27	ns

TYPICAL CHARACTERISTICS

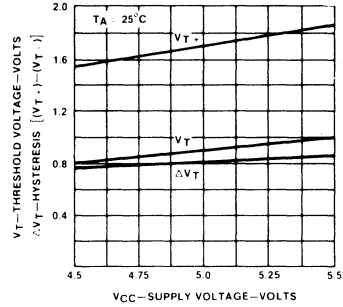
(54/74, 54LS/74LS)
VIN vs VOUT
TRANSFER FUNCTION



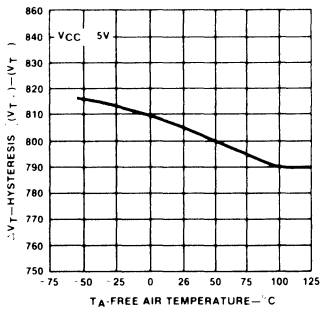
(54/74)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



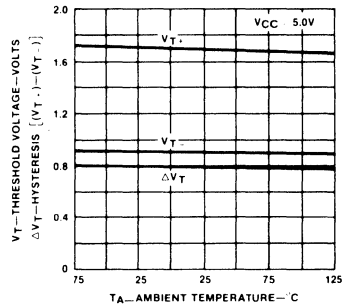
(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



(54/74)
HYSTERESIS vs TEMPERATURE



(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
AMBIENT TEMPERATURE



4

SCHMITT TRIGGERS

54/7414, LS14

Hex Inverter Schmitt Trigger

DESCRIPTION

The '14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7414	15ns	31mA
74LS14	15ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7414N • N74LS14N	
Plastic SO	N74LS14D	
Ceramic DIP		S5414F • S54LS14F
Flatpack		S5414W • S54LS14W

FUNCTION TABLE

INPUT	OUTPUT
A	Y
0	1
1	0

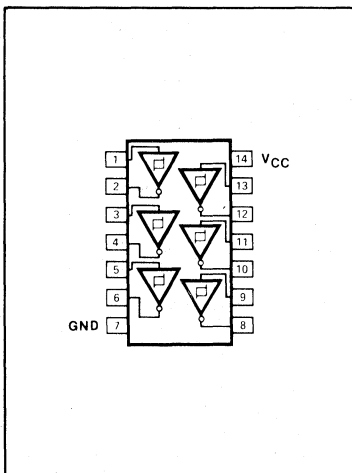
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
A	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

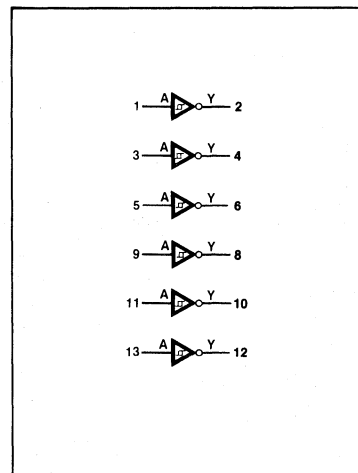
NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and -0.4mA I_{IL} .

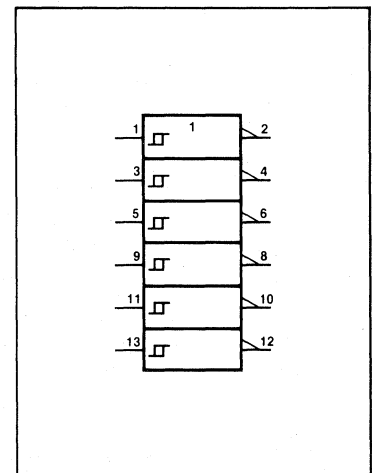
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

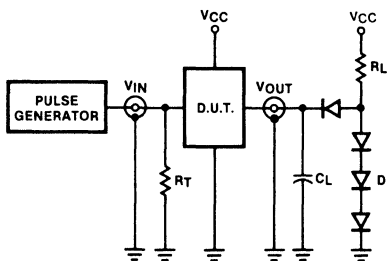
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current				-800			-400	μA
I _{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

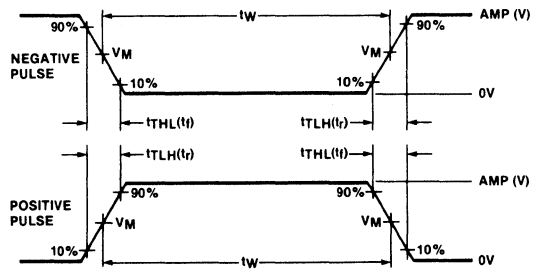
4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

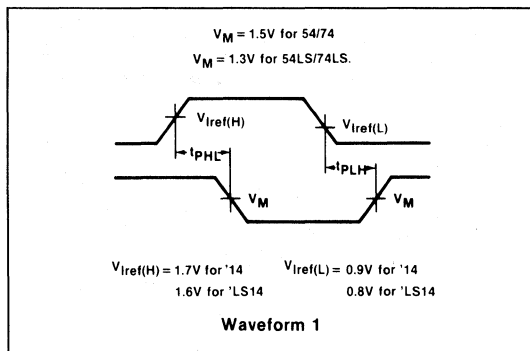
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7414			54/74LS14			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{T+} Positive-going threshold	V _{CC} = 5.0V	1.5	1.7	2.0	1.4	1.6	1.9	V		
V _{T-} Negative-going threshold	V _{CC} = 5.0V	0.6	0.9	1.1	0.5	0.8	1.0	V		
ΔV _T Hysteresis (V _{T+} - V _{T-})	V _{CC} = 5.0V	0.4	0.8		0.4	0.8		V		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _I = V _{T-} MIN, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _I = V _{T+} MAX	I _{OL} = MAX	Mil	0.2	0.4		0.25	0.4	V	
			Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V		
I _{T+} Input current at positive-going threshold	V _{CC} = 5.0V, V _I = V _{T+}		-0.43			-0.14		mA		
I _{T-} Input current at negative-going threshold	V _{CC} = 5.0V, V _I = V _{T-}		-0.56			-0.18		mA		
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA		
		V _I = 7.0V					0.1	mA		
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40			μA		
		V _I = 2.7V					20	μA		
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.2			-0.4	mA		
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	mA	
		Com'l	-18		-55	-20		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		22	36		8.6	16	mA	
		I _{CCL} Outputs LOW		39	60		12	21	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS

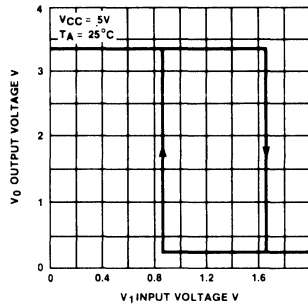


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

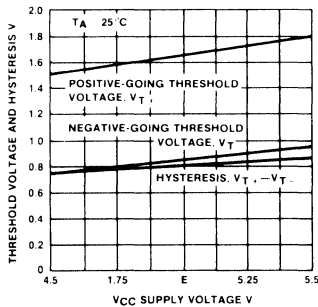
PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 22		22 22	ns

TYPICAL CHARACTERISTICS

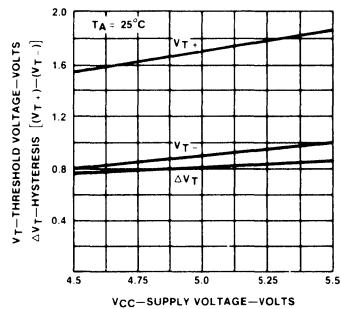
(54/74, 54LS/74LS)
VIN vs VOUT
TRANSFER FUNCTION



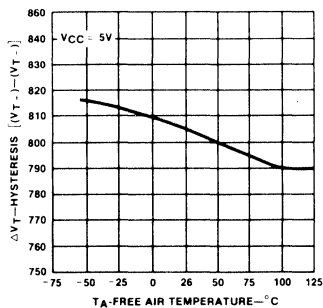
(54/74)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



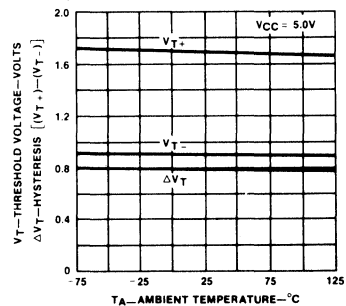
(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



(54/74)
HYSTERESIS vs TEMPERATURE



(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
AMBIENT TEMPERATURE



INVERTER/BUFFER/DRIVERS

54/7416, 17

'16 Hex Inverter Buffer/Driver (Open Collector)
'17 Hex Buffer/Driver (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7416	10ns (t _{PLH}) 15ns (t _{PHL})	31mA
7417	6ns (t _{PLH}) 20ns (t _{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = - 55°C to + 125°C
Plastic DIP	N7416N • N7417N	
Plastic SO	N7417D	

FUNCTION TABLE

'16		'17	
INPUT	OUTPUT	INPUT	OUTPUT
A	Y	A	Y
L	H	L	L
H	L	H	H

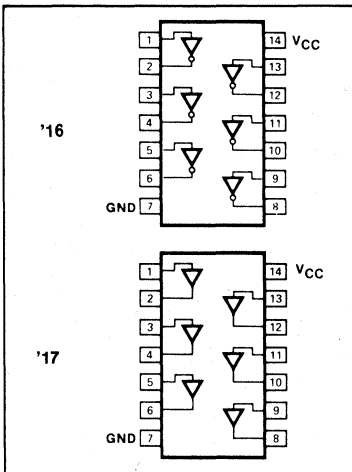
H = HIGH voltage level
 L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

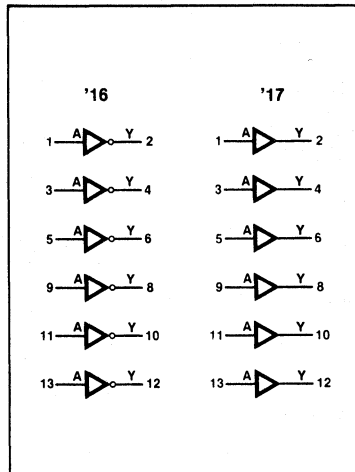
PINS	DESCRIPTION	54/74
A	Input	1uI
Y	Output	10uI

NOTE
 A 54/74 unit load (uI) is understood to be 40µA I_{IH} and - 1.6mA I_{IL}.

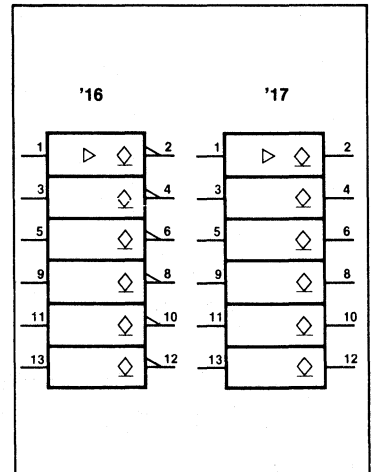
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to +15	-0.5 to +15	V
T_A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current			-12	mA	
V_{OH}	HIGH-level output voltage			15	V	
I_{OL}	LOW-level output current	Mil			30	mA
		Com'l			40	mA
T_A	Operating free-air temperature	Mil	-55		+125	°C
		Com'l	0		70	°C

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS

INPUT PULSE DEFINITIONS

$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

INVERTER/BUFFER/DRIVERS

54/7416, 17

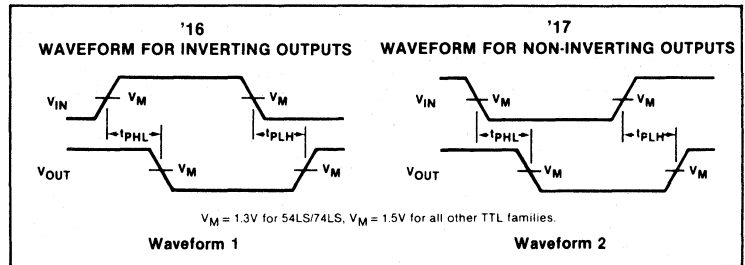
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7416, 54/7417			UNIT	
		Min	Typ ²	Max		
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 15\text{V}$			250	μA	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = 16\text{mA}$		0.4	V	
		$I_{OL} = 30\text{mA}$	Mil	0.7	V	
		$I_{OL} = 40\text{mA}$	Com'l	0.7	V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_1 = I_{IK}$			-1.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6	mA	
I_{CC} Supply current (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	'16	30	48	mA
				I_{CCL} Outputs LOW	32	51
		I_{CCH} Outputs HIGH	'17	29	41	mA
				I_{CCL} Outputs LOW	21	30

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORMS



AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/7416		54/7417		UNIT
		$C_L = 15\text{pF}, R_L = 110\Omega$				
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1, '16 Waveform 2, '17		15 23	10 30		ns

GATES

54/7420, 54/7421, LS20, LS21, S20

Dual Four-Input NAND ('20), AND ('21) Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7420	10ns	8mA
74LS20	10ns	0.8mA
74S20	3ns	8mA
7421	12ns	8mA
74LS21	9ns	1.7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP '20	N7420N • N74LS20N N74S20N	
	'21	N7421N • N74LS21N
Plastic SO	N74LS20D • N74S20D N74LS21D	
Ceramic DIP '20		S5420F • S54LS20F S54S20F
Flatpack '20		S5420W • S54LS20W S54S20W
LLCC		S54LS20G

FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y('20)	Y('21)
L	X	X	X	H	L
X	L	X	X	H	L
X	X	L	X	H	L
X	X	X	L	H	L
H	H	H	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

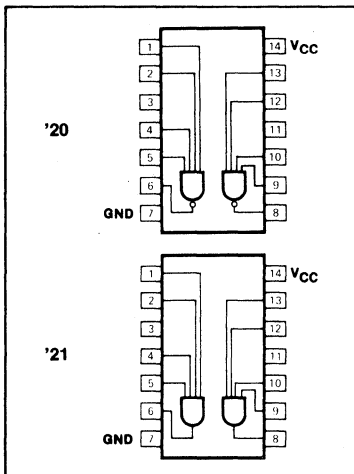
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A-D	Inputs	1uI	1SuI	1LSuI
Y	Output	10uI	10SuI	10LSuI

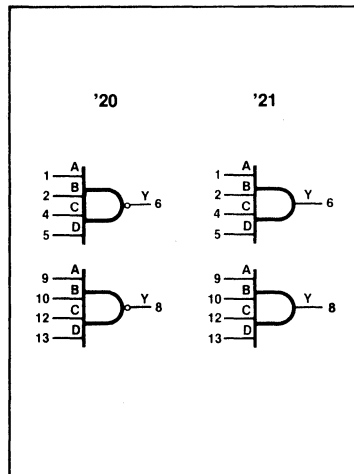
NOTE

Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (SuI) is 50µA I_{IH} and -2.0mA I_{IL} , and 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL} .

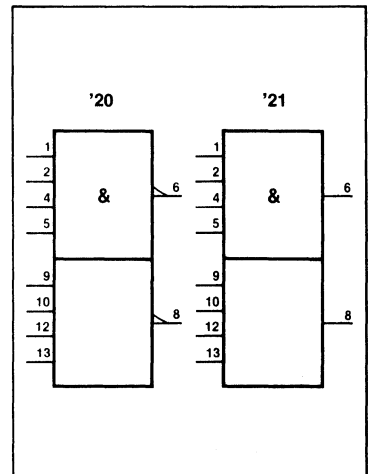
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



GATES

54/7420, 54/7421, LS20, LS21, S20

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

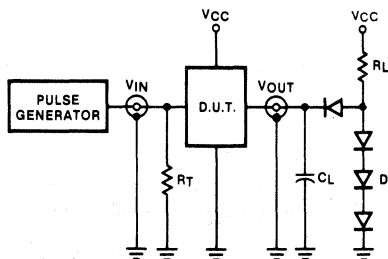
PARAMETER	54/74			54/74LS			54/74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	Mil	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current	'20			-400			-400			-1000	μA
	'21			-800			-400			-1000	μA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

NOTE

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

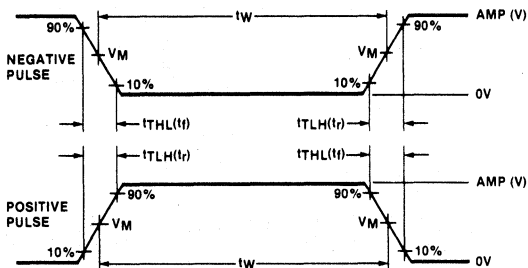
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

GATES

54/7420, 54/7421, LS20, LS21, S20

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

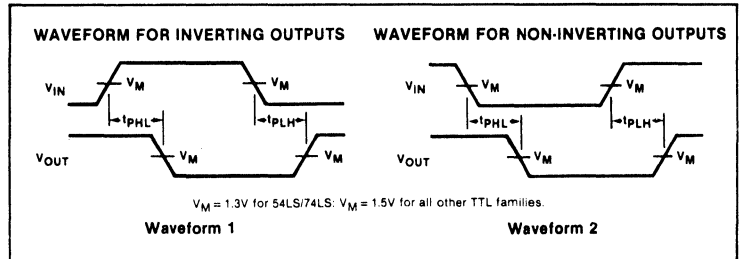
PARAMETER	TEST CONDITIONS ¹	54/7420, 21			54/74LS20, 21			54/74S20			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁴	V	
			Com'l		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA	74LS					0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA	
		V _I = 7.0V						0.1				mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40							μA	
		V _I = 2.7V						20			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4				mA	
		V _I = 0.5V									-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40		-100	mA	
		Com'l	-18		-55	-20		-100	-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH	'20		2	4		0.4	0.8		5	8	mA
				I _{CCL} Outputs LOW		6	11		1.2	2.2		10	18
		I _{CCH} Outputs HIGH	'21		6	8		1.2	2.4				mA
				I _{CCL} Outputs LOW		11	13		2.2	4.4			

4

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



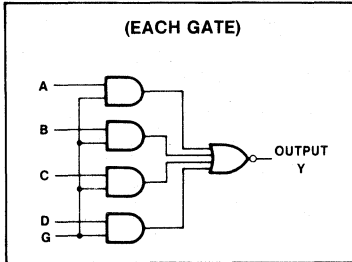
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1, '20		22 15		15 15		4.5 5.0	ns
t _{PLH} t _{PHL} Propagation delay	Waveform 2, '21		27 19		15 20			ns

Dual Four-Input NOR Gate With Strobe

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7425	9ns	9mA

LOGIC DIAGRAM



ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7425N	
Ceramic DIP		S5425F
Flatpack		S5425W

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
X	X	X	X	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	H	H

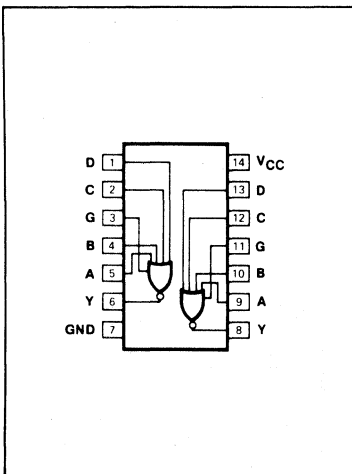
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

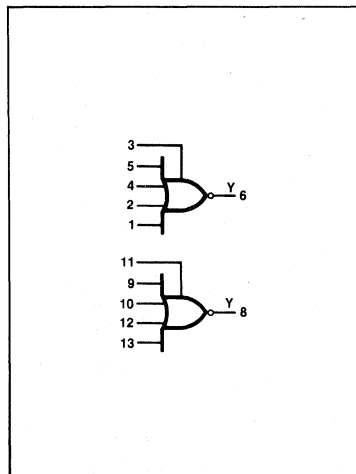
PINS	DESCRIPTION	54/74
A-D	Inputs	1uI
G	Input	4uI
Y	Output	10uI

NOTE
Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

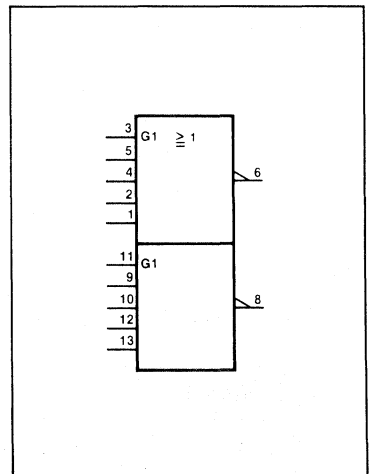
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current			-12	mA	
I_{OH}	HIGH-level output current			-800	μA	
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	-55		+125	°C
		Com'l	0		70	°C

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

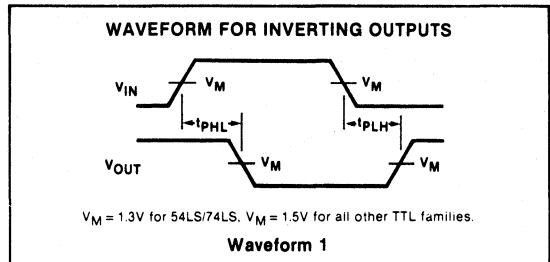
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7425			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4	V	
		Com'l	2.4	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	G input			160	μA
		Other Inputs			40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	G input			-6.4	mA
		Other inputs			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	mA
		Com'l	-18		-55	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH		8	16	mA
		I _{CC} L Outputs LOW		10	19	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT	
		C _L = 15pF, R _L = 400Ω			
		Min	Max		
t _{PLH} t _{PHL}	Propagation delay	Waveform 1		22 15	ns

Quad Two-Input NAND Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7426	14ns	8mA
74LS26	16ns	1.6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7426N • N74LS26N	
Plastic SO	N74LS26D	
Ceramic DIP		S5426F

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

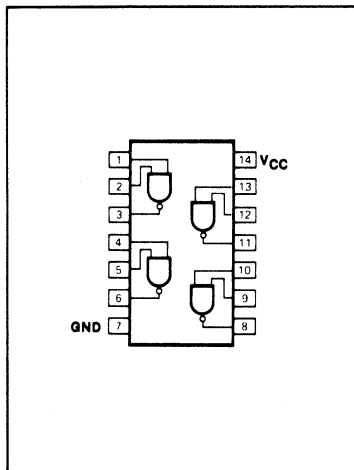
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

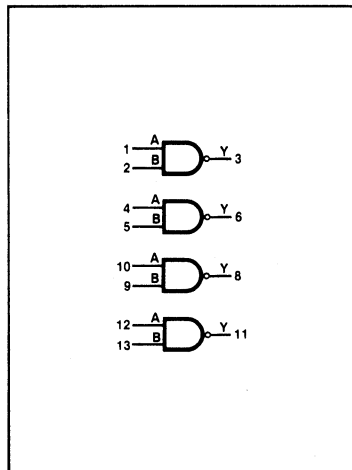
PINS	DESCRIPTION	54/74	54/74LS
A, B	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$ and a 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

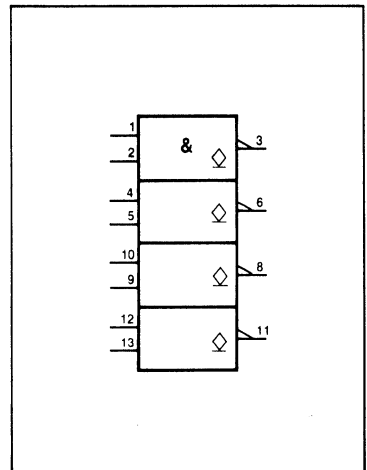
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



GATES

54/7426, LS26

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

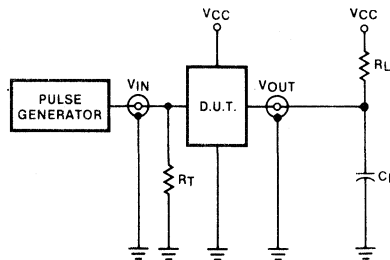
PARAMETER		54	54LS	74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +15	-0.5 to +15	-0.5 to +15	-0.5 to +15	V
T _A	Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

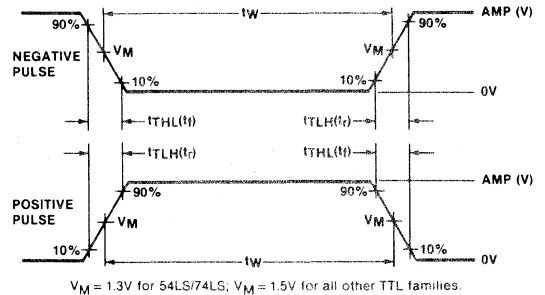
PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V	
V _{IL}	LOW-level input voltage	Mil				+0.7			V
		Com'l				+0.8			V
I _{IK}	Input clamp current				-12			mA	
V _{OH}	HIGH-level output voltage				15			V	
I _{OL}	LOW-level output current	Mil				4			mA
		Com'l				8			mA
T _A	Operating free-air temperature	Mil	-55	+125		-55	+125		°C
		Com'l	0	70		0	70		°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



INPUT PULSE DEFINITIONS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS			
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}
54/74	3.0V	1MHz	500ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns
54S/74S	3.0V	1MHz	500ns	2.5ns

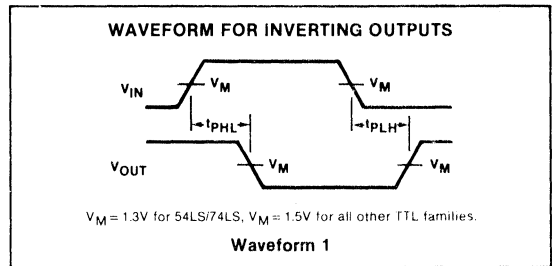
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7426			54/74LS26			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
I _{OH} HIGH-level output current	V _{CC} = MIN, V _{IL} = MAX	V _{OH} = 15V		~1000		1000	μA	
		V _{OH} = 12V		50		50	μA	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil	0.2	0.4	0.25	0.4	V
			Com'l	0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA	74LS			0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5		-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V		1.0			mA	
		V _I = 7.0V				0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V		40			μA	
		V _I = 2.7V				20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6		-0.4	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		4	8	0.8	1.6	mA
		I _{CCL} Outputs LOW		12	22	2.4	4.4	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C _L = 15pF, R _L = 1kΩ		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		24 17		32 28	ns

4

Triple Three-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7427	9ns	13mA
74LS27	10ns	2.7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7427N • N74LS27N	
Plastic SO	N74LS27D	

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

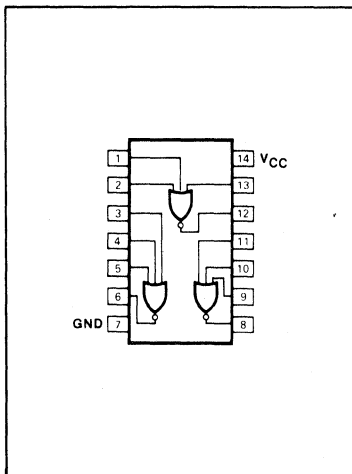
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

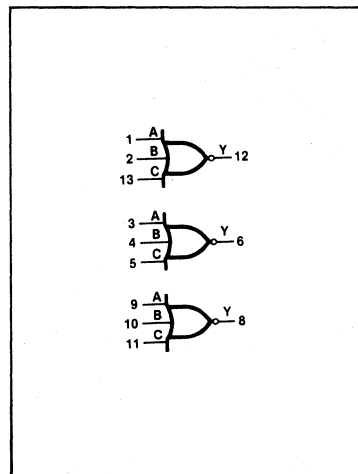
PINS	DESCRIPTION	54/74	54/74LS
A-C	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

NOTE
 Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL} .

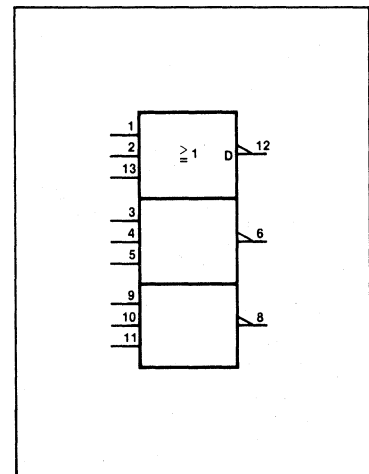
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to -5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

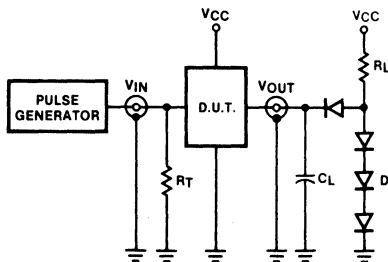
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current				-800			-400	μA
I _{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

4

TEST CIRCUITS AND WAVEFORMS

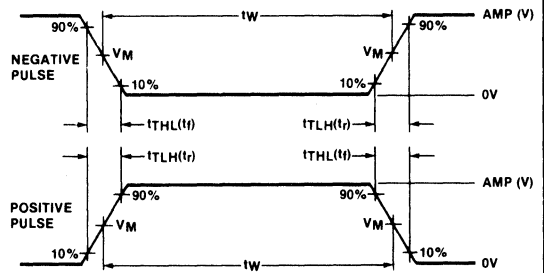
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

GATES

54/7427, LS27

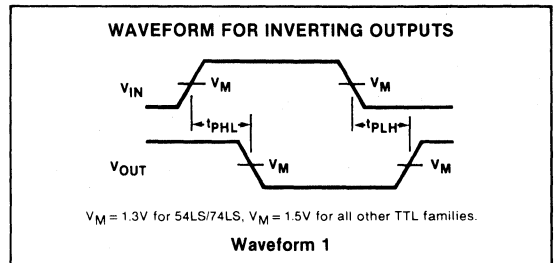
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7427			54/74LS27			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA	
		V _I = 7.0V						0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40				μA	
		V _I = 2.7V						20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6			-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	mA	
		Com'l	-18		-55	-20		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		10	16		2.0	4	mA	
		I _{CCL} Outputs LOW		16	26		3.4	6.8	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay	Waveform 1	15 11	15 15	ns	

Quad Two-Input NOR Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7428	7ns	23mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7428N	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

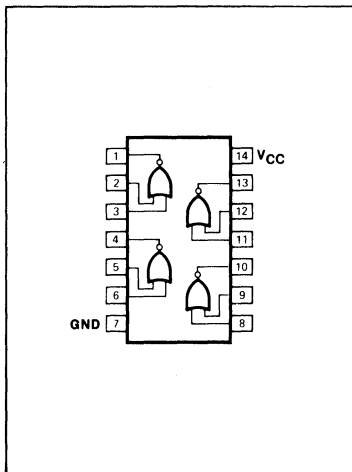
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
A, B	Inputs	1uI
Y	Output	30uI

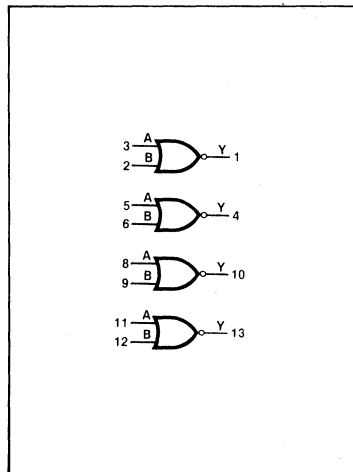
NOTE

Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

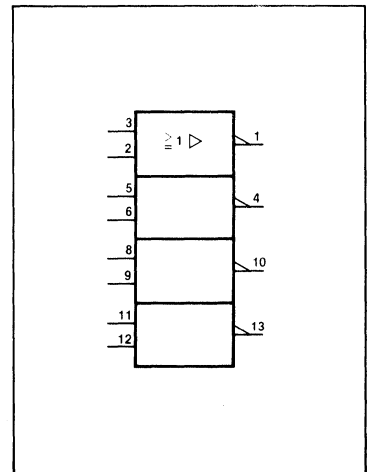
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

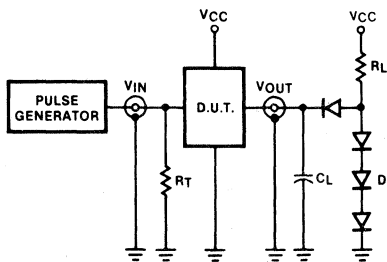
PARAMETER		54	74	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I _{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V	
V _{IL}	LOW-level input voltage	Mil		+ 0.8	V	
		Com'l		+ 0.8	V	
I _{IK}	Input clamp current			- 12	mA	
I _{OH}	HIGH-level output current			- 2400	μA	
I _{OL}	LOW-level output current	Mil		48	mA	
		Com'l		48	mA	
T _A	Operating free-air temperature	Mil	- 55	+ 125	°C	
		Com'l	0	70	°C	

TEST CIRCUITS AND WAVEFORMS

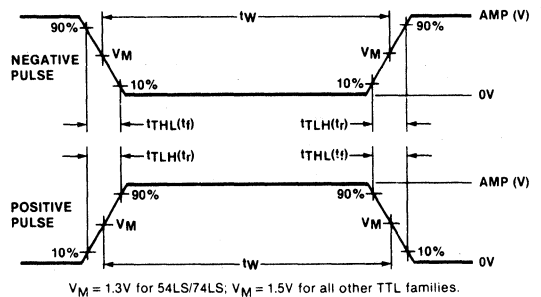
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

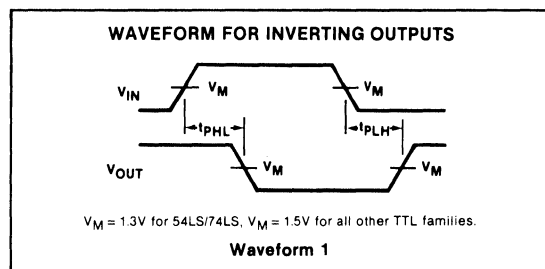
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7428			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4	V	
		Com'l	2.4	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-70	-180	mA	
		Com'l	-70	-180	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		12	21	mA
		I _{CCL} Outputs LOW		33	57	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT
		R _L = 133Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1 C _L = 50pF		9.0	ns
			12	
t _{PLH} t _{PHL} Propagation delay	Waveform 1 C _L = 150pF		15	ns
			18	

4

GATES

54/7430, LS30

Eight-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7430	11ns	2mA
74LS30	11ns	0.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N7430N • N74LS30N	
Plastic SO	N74LS30D	
Ceramic DIP		S54LS30F
Flatpack		S54LS30W

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
X	X	X	X	X	X	X	X	L
H	H	H	H	H	H	H	H	L

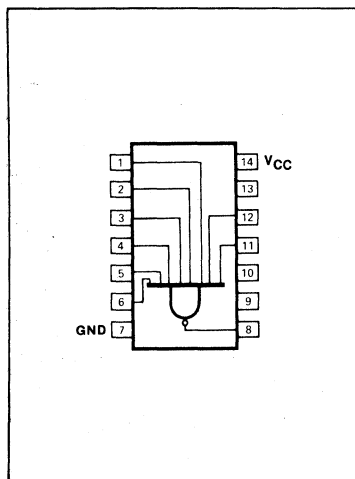
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

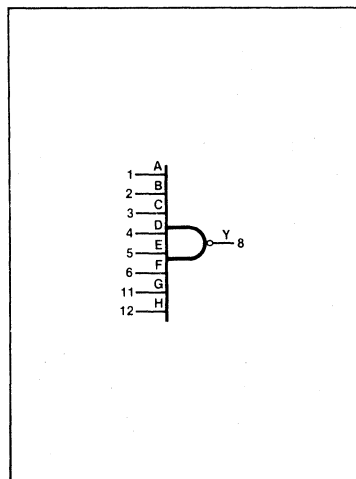
PINS	DESCRIPTION	54/74	54/74LS
A-H	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

NOTE
 Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL}, and 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL}.

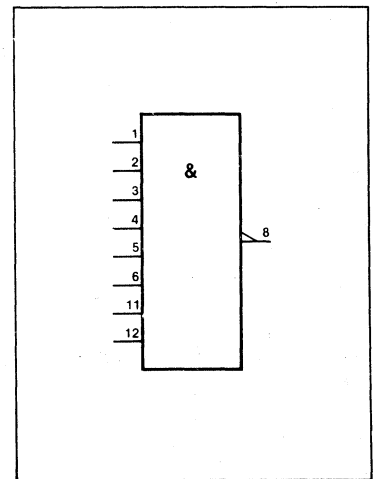
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125		0 to 70		°C

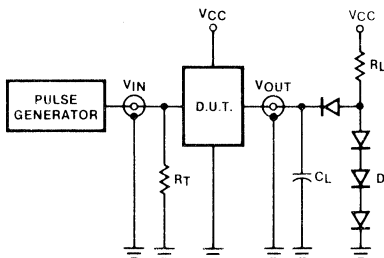
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V	
V_{IL}	LOW-level input voltage	Mil				+0.7			V
		Com'l				+0.8			V
I_{IK}	Input clamp current				-12			mA	
I_{OH}	HIGH-level output current				-400			μ A	
I_{OL}	LOW-level output current	Mil				16			mA
		Com'l				16			mA
T_A	Operating free-air temperature	Mil	-55	+125		-55	+125		°C
		Com'l	0	70		0	70		°C

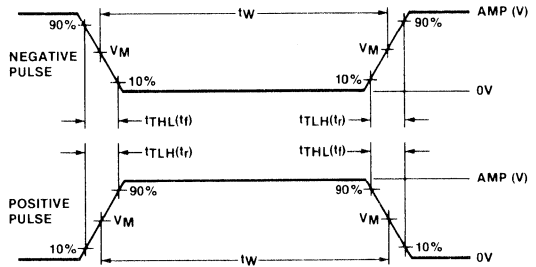
4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

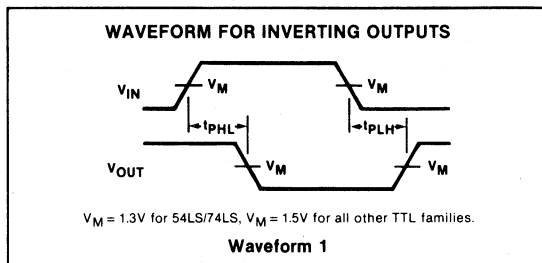
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7430			54/74LS30			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l			0.2	0.4		0.35	0.5
		I _{OL} = 4mA	74LS						0.25	0.4
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA	
		V _I = 7.0V						0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40				μA	
		V _I = 2.7V						20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6			-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	mA	
		Com'l	-18		-55	-20		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		1	2		0.35	0.5	mA	
		I _{CCL} Outputs LOW		3	6		0.6	1.1	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Waveform 1		22 15		15 20	ns

Quad Two-Input OR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7432	12ns	19mA
74LS32	14ns	4.0mA
74S32	4ns	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7432N • N74LS32N N74S32N	
Plastic SO	N74LS32D • N74S32D	
Ceramic DIP		S5432F • S54LS32F
Flatpack		S5432W • S54LS32W
LLCC		S54LS32G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

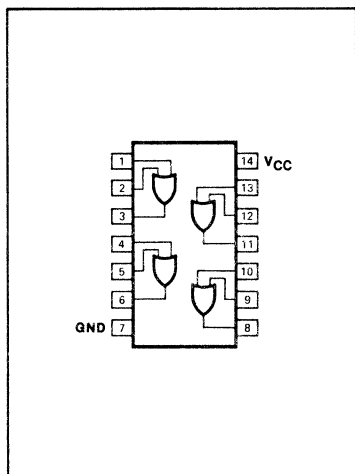
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1uI	1SuI	1LSuI
Y	Output	10uI	10SuI	10LSuI

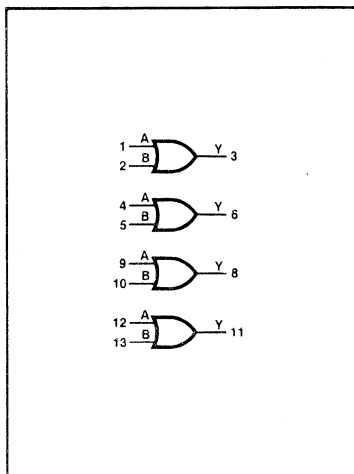
NOTE

Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (SuI) is 50µA I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL} .

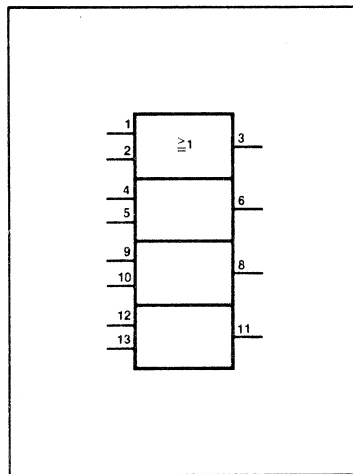
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



4

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

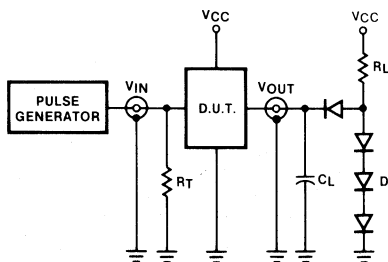
PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

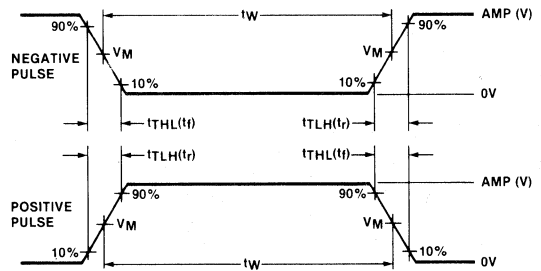
PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-800			-400			-1000	μA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS			
	Amplitude	Rep. Rate	Pulse Width	t _{THL}
54/74	3.0V	1MHz	500ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns
54S/74S	3.0V	1MHz	500ns	2.5ns

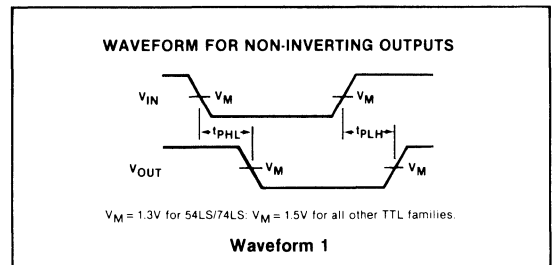
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/7432			54/74LS32			54/74S32			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
		Com ¹	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5	V
			Com ¹		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA
		V _I = 7.0V						0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40							μA
		V _I = 2.7V						20			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4				mA
		V _I = 0.5V									-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40		-100	mA
		Com ¹	-18		-55	-20		-100	-40		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		15	22		3.1	6.2		18	32	mA
		I _{CCL} Outputs LOW		23	38		4.9	9.8		38	68	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25 °C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25 °C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		15 22		22 22		7.0 7.0	ns

BUFFERS

54/7433, LS33

Quad Two-input NOR Buffer (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7433	11ns	23mA
74LS33	19ns	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7433N • N74LS33N	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

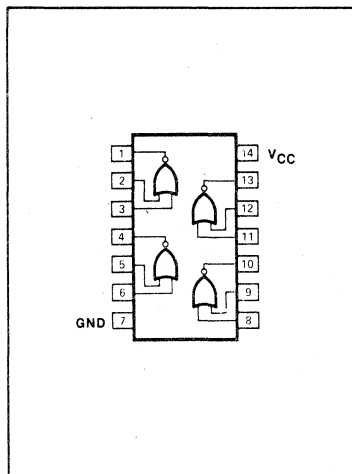
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
A, B	Inputs	1uI	1LSuI
Y	Output	30uI	30LSuI

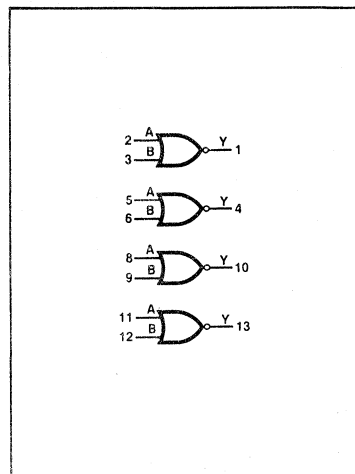
NOTE

Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

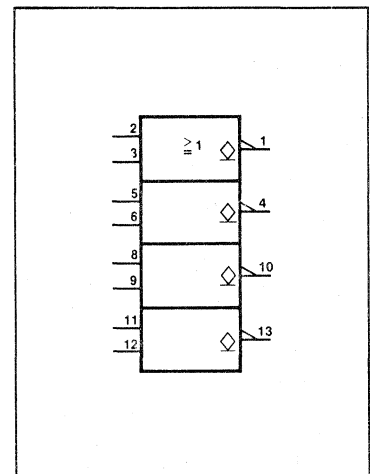
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUFFERS

54/7433, LS33

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to -5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

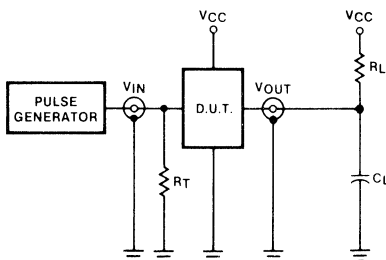
RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74			54/74LS			UNIT		
	Min	Nom	Max	Min	Nom	Max			
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V	
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V	
V _{IH} HIGH-level input voltage	2.0			2.0			V		
V _{IL} LOW-level input voltage	Mil				+0.7			V	
	Com'l				+0.8			V	
I _{IK} Input clamp current				-12			-18	mA	
V _{OH} HIGH-level output voltage				5.5			5.5	V	
I _{OL} LOW-level output current	Mil				48			12	mA
	Com'l				48			24	mA
T _A Operating free-air temperature	Mil	-55	+125		-55	+125		°C	
	Com'l	0	70		0	70		°C	

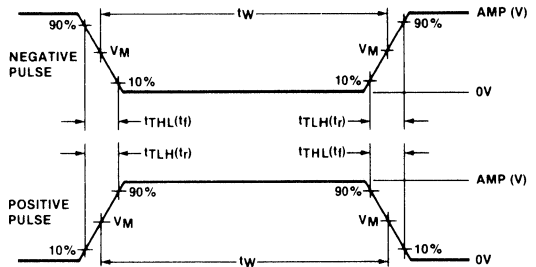
4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS

54/7433, LS33

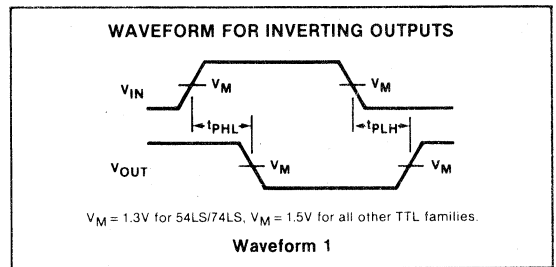
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7433			54/74LS33			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
I _{OH} HIGH-level output current	V _{CC} = MIN, V _{IL} = MAX, V _{OH} = 5.5V			250			250	μA
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil	0.2	0.4	0.25	0.4	V
			Com'l	0.2	0.4	0.35	0.5	V
		I _{OL} = 12mA	74LS			0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V		1.0				mA
		V _I = 7.0V				0.1		mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V		40				μA
		V _I = 2.7V				20		μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		12	21	1.8	3.6	mA
		I _{CCL} Outputs LOW		33	57	6.9	13.8	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		R _L = 133Ω		C _L = 45pF, R _L = 667Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	C _L = 50pF for 54/7433 Waveform 1		15 18		32 28	ns
t _{PLH} t _{PHL}	C _L = 150pF for 54/7433 Waveform 1		22 24			ns

BUFFERS

54/7437, LS37, S37

Quad Two-Input NAND Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7437	11ns	22mA
74LS37	12ns	3.5mA
74S37	4ns	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7437N • N74LS37N N74S37N	
Plastic SO	N74S37D	
Ceramic DIP		S54S37F • S54LS37F
Flatpack		S54S37W • S54LS37W
LLCC		S54LS37G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

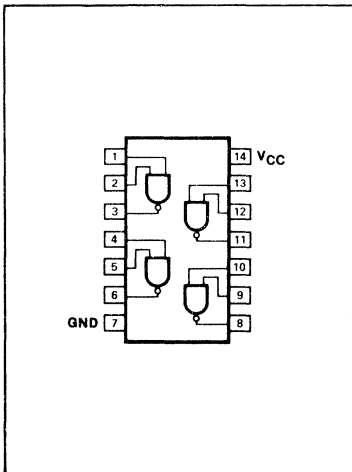
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1uI	2SuI	1LSuI
Y	Output	30uI	30SuI	30LSuI

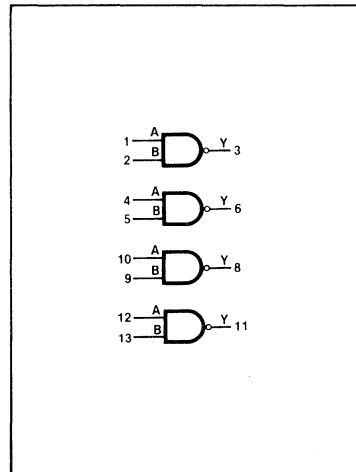
NOTE

Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (SuI) is 50µA I_{IH} and -2.0mA I_{IL} , and 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL} .

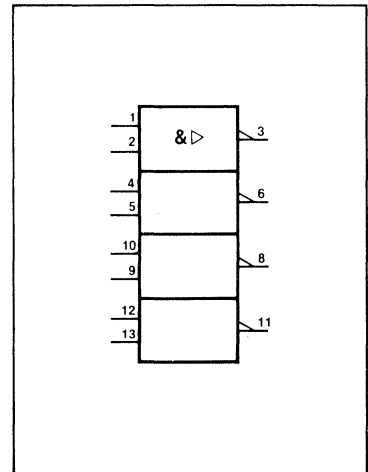
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



4

BUFFERS

54/7437, LS37, S37

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

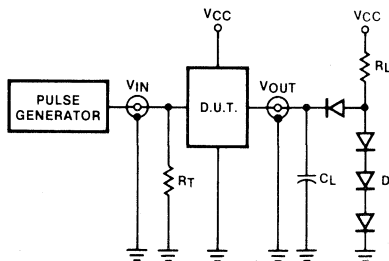
PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-1200			-1200			-3000	μA
I _{OL} LOW-level output current	Mil			48			12			60	mA
	Com'l			48			24			60	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

NOTE

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

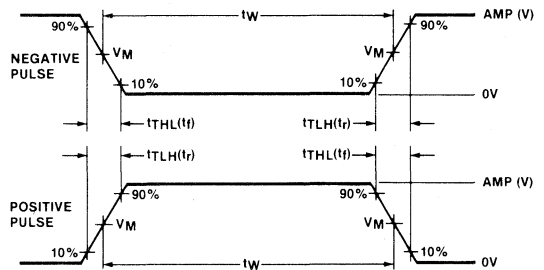
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS

54/7437, LS37, S37

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

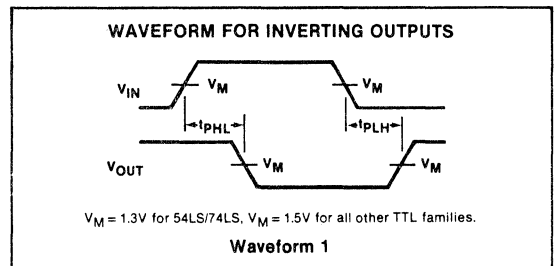
PARAMETER	TEST CONDITIONS ¹	54/7437			54/74LS37			54/74S37			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁴	V
			Com'l		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 12mA	74LS					0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA
		V _I = 7.0V						0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40							μA
		V _I = 2.7V						20			100	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4				mA
		V _I = 0.5V									-4.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-70	-30		-100	-50		-225	mA
		Com'l	-18		-70	-30		-100	-50		-225	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		9	15.5		0.9	2		20	36	mA
		I _{CCL} Outputs LOW		34	54		6	12		46	80	mA

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NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second for the 54/7437 and 54/74LS37, and 100 milliseconds for the 54/74S37.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT		
		C _L = 45pF, R _L = 133Ω		C _L = 45pF, R _L = 667Ω		C _L = 50pF, R _L = 93Ω				
		Min	Max	Min	Max	Min	Max			
t _{PLH} t _{PHL}	Propagation delay	Waveform 1			22 15		24 24		6.5 6.5	ns

BUFFERS

54/7438, LS38, S38

Quad Two-Input NAND Buffers (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7438	13ns	28mA
74LS38	19ns	3.5mA
74S38	6.5ns	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7438N • N74LS38N N74S38N	
Plastic SO	N74S38D • N74LS38D	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

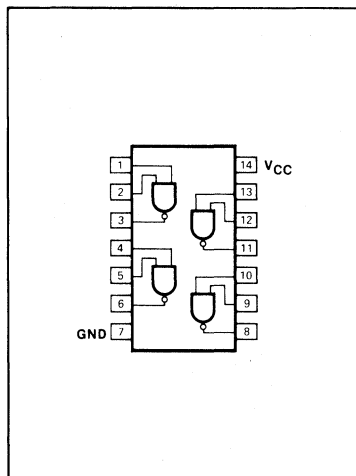
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	2Sul	1LSul
Y	Output	30ul	30Sul	30LSul

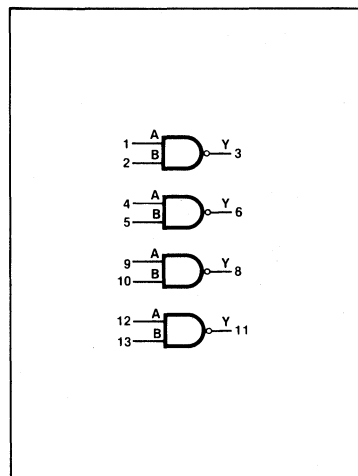
NOTE

Where a 54/74 unit load (ul) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

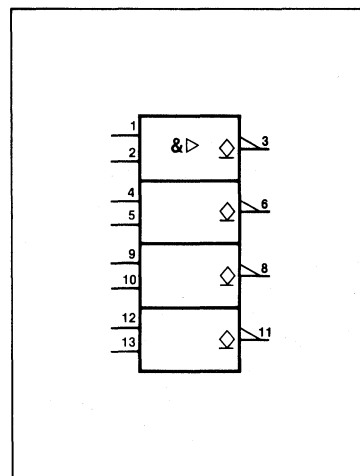
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUFFERS

54/7438, LS38, S38

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74			54/74LS			54/74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
V _{OH} HIGH-level output voltage				5.5			5.5			5.5	V
I _{OL} LOW-level output current	Mil			48			12			60	mA
	Com'l			48			24			60	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS

INPUT PULSE DEFINITIONS

V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS

54/7438, LS38, S38

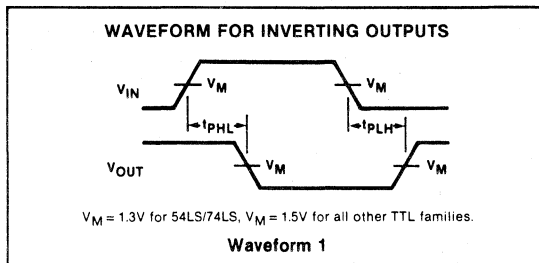
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/7438			54/74LS38			54/74S38			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5\text{V}$				250			250			250	μA
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}$	$I_{OL} = \text{MAX}$	Mil	0.2	0.4		0.25	0.4			0.5	V
			Com'l	0.2	0.4		0.35	0.5			0.5	V
		$I_{OL} = 12\text{mA}$	74LS				0.25	0.4				V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.5			-1.5			-1.2	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$			1.0						1.0	mA
		$V_I = 7.0\text{V}$						0.1				mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$			40							μA
		$V_I = 2.7\text{V}$						20			100	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$			-1.6			-0.4				mA
		$V_I = 0.5\text{V}$									-4.0	mA
I_{CC} Supply current (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		5	8.5		0.9	2		20	36	mA
		I_{CCL} Outputs LOW		34	54		6	12		46	80	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORM



AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		$C_L = 45\text{pF}, R_L = 133\Omega$		$C_L = 45\text{pF}, R_L = 667\Omega$		$C_L = 50\text{pF}, R_L = 93\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1		22 18		32 28		10 10	ns

Quad Two-Input NAND Buffer (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7439	11ns	4.5mA (I_{CCH}) 30mA (I_{CCL})

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7439N	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = HIGH voltage level
L = LOW voltage level

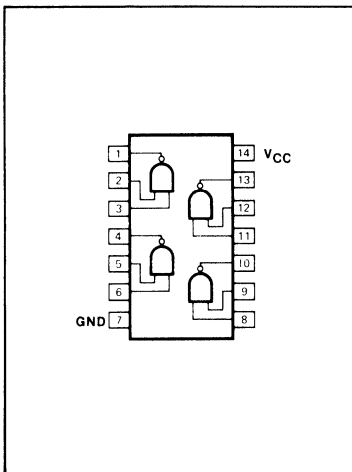
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
A, B	Inputs	1uI
Y	Output	30uI

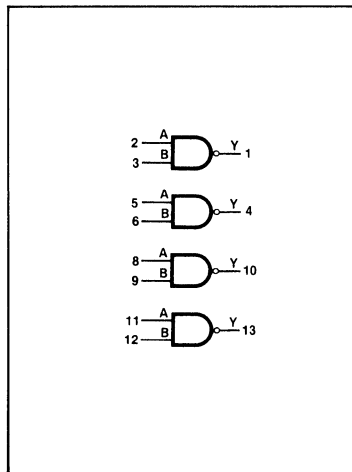
NOTE
A 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

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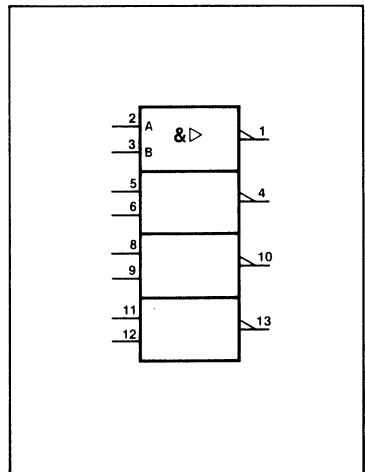
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

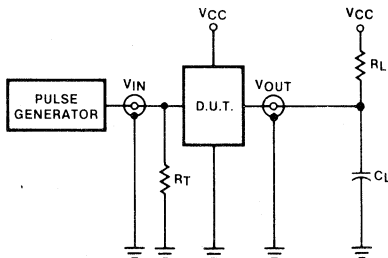
PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

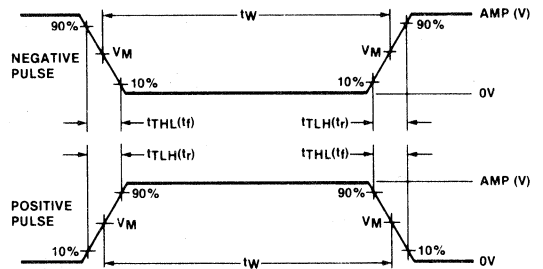
PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current			-12	mA	
V_{OH}	HIGH-level output voltage			5.5	V	
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			48	mA
T_A	Operating free-air temperature	Mil	-55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns*

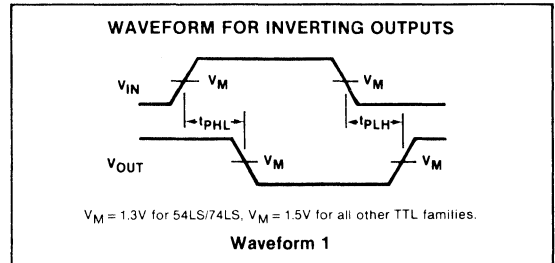
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7439			UNIT
		Min	Typ ²	Max	
I_{OH}	HIGH-level output current $V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5\text{V}$			250	μA
V_{OL}	LOW-level output voltage $V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	Mil	0.2	0.4	V
		Com'l	0.2	0.4	V
V_{IK}	Input clamp voltage $V_{CC} = \text{MIN}, I_1 = I_{IK}$			-1.5	V
I_i	Input current at maximum input voltage $V_{CC} = \text{MAX}, V_i = 5.5\text{V}$			1.0	mA
I_{IH}	HIGH-level input current $V_{CC} = \text{MAX}, V_i = 2.4\text{V}$			40	μA
I_{IL}	LOW-level input current $V_{CC} = \text{MAX}, V_i = 0.4\text{V}$			-1.6	mA
I_{CC}	Supply current (total) $V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	4.5	8.5	mA
		I_{CCL} Outputs LOW	30	54	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.

AC WAVEFORM



4

AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		$C_L = 45\text{pF}, R_L = 133\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Waveform 1		22 18	ns

BUFFERS

54/7440, LS40, S40

Dual Four-Input NAND Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7440	11ns	11mA
74LS40	12ns	1.8mA
74S40	6ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7440N • N74LS40N N74S40N	
Ceramic DIP		S54S40F
Flatpack		S54S40W

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

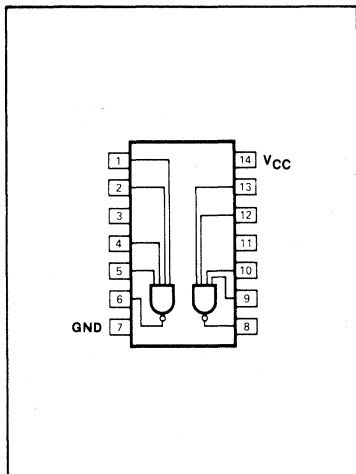
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A-D	Inputs	1uI	2Sul	1LSul
Y	Output	30uI	30Sul	30LSul

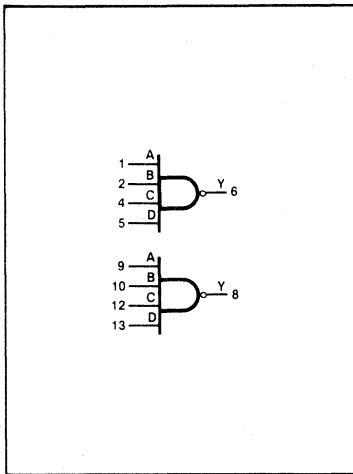
NOTE

Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50µA I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL} .

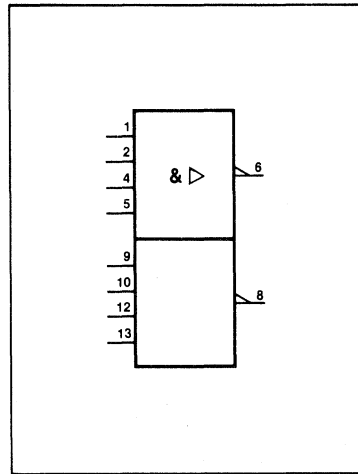
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUFFERS

54/7440, LS40, S40

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

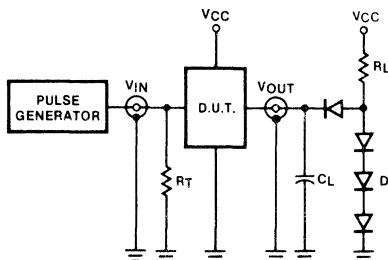
RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74			54/74LS			54/74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	Mil	2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-1200			-1200			-3000	μA
I _{OL} LOW-level output current	Mil			48			12			60	mA
	Com'l			48			24			60	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

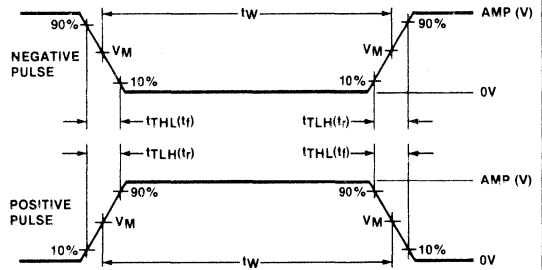
NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

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BUFFERS

54/7440, LS40, S40

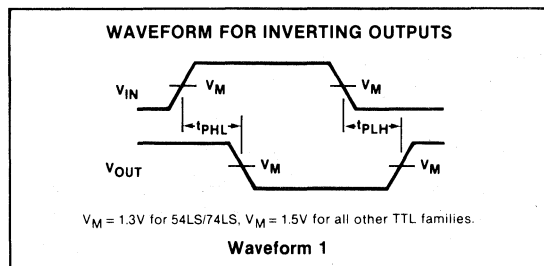
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7440			54/74LS40			54/74S40			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁴	V
			Com'l		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 12mA	74LS					0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA
		V _I = 7.0V						0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40							μA
		V _I = 2.7V						20			100	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4				mA
		V _I = 0.5V									-4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-70	-15		-100	-50		-225	mA
		Com'l	-18		-70	-15		-100	-50		-225	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		4	8		0.45	1		10	18	mA
		I _{CCL} Outputs LOW		17	27		3	6		25	44	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. The 54/74S40 test time for I_{OS} should not exceed 100ms.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 133Ω		C _L = 45pF, R _L = 667Ω		C _L = 50pF, R _L = 93Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 15		24 24		6.5 6.5	ns

BCD-To-Decimal Decoder (1-of-10)

- **Mutually exclusive outputs**
- **1-of-8 demultiplexing capability**
- **Outputs disabled for input codes above nine**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7442	15ns	28mA
74LS42	18ns	7mA

DESCRIPTION

The '42 decoder accepts four active HIGH BCD inputs and provides 10 mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the '42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input, A_3 , produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N7442N • N74LS42N	
Plastic SO	N74LS54D	
Ceramic DIP		S5442F • S54LS42F
Flatpack		S5442W • S54LS42W
LLCC		S54LS42G

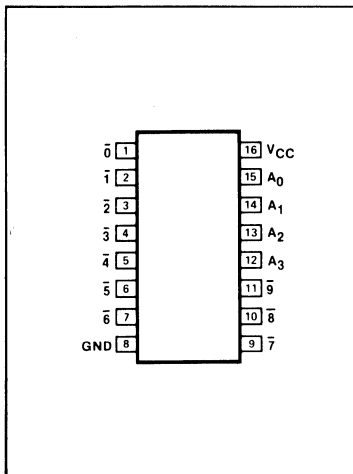
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INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

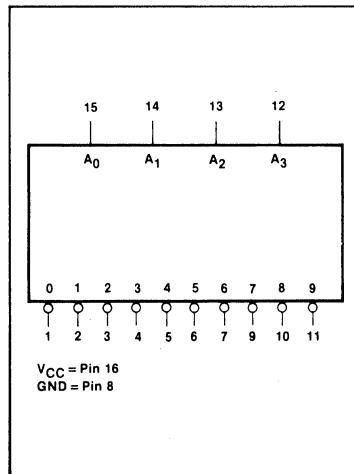
PINS	DESCRIPTION	54/74	54/74LS
A_0-A_3	Inputs	1uI	1LSuI
$\bar{0}-\bar{9}$	Outputs	10uI	10LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and - 1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and - 0.4mA I_{IL} .

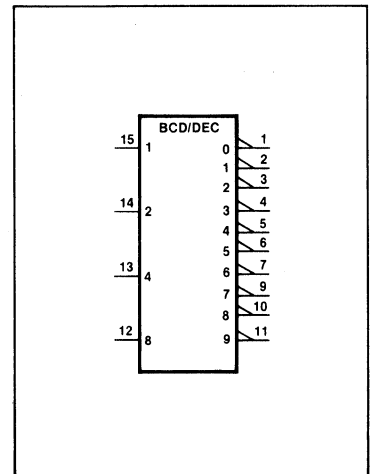
PIN CONFIGURATION



LOGIC SYMBOL



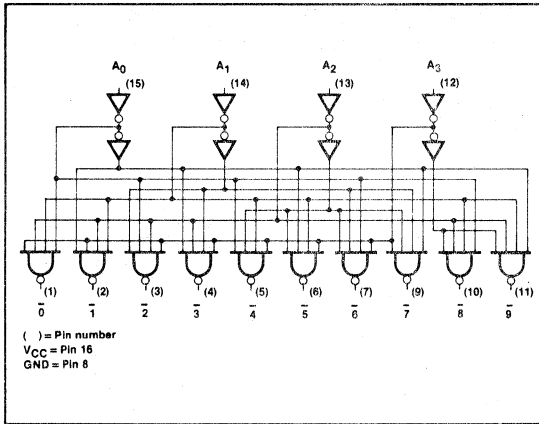
LOGIC SYMBOL (IEEE/IEC)



DECODERS

54/7442, LS42

LOGIC DIAGRAM



FUNCTION TABLE

A ₃	A ₂	A ₁	A ₀	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	H	H	H	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	H	H	H	H	L
H	L	H	H	H	H	H	H	H	H	H	H	H	L
H	L	L	L	H	H	H	H	H	H	H	H	H	H
H	L	L	H	H	H	H	H	H	H	H	H	H	H
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to -5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current				-800			-400	μA
I _{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

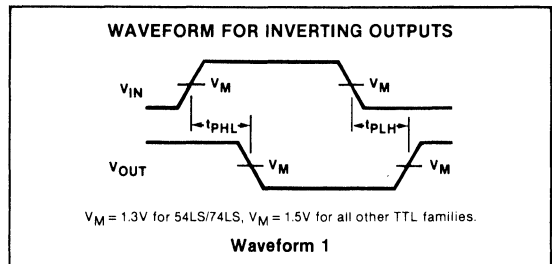
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/7442			54/74LS42			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		Mil	2.4	3.4		2.5	3.4	V	
			Com'l	2.4	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX		I _{OL} = MAX	Mil	0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5
			I _{OL} = 4mA	74LS					0.25	0.4
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.5		-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX		V _I = 5.5V			1.0			mA	
			V _I = 7.0V					0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX		V _I = 2.4V			40			μA	
			V _I = 2.7V					20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V					-1.6		-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		Mil	-20		-55	-20		-100	mA
			Com'l	-18		-55	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		Mil		28	41		7	13	mA
			Com'l		28	56		7	13	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all outputs open and all inputs grounded.

AC WAVEFORM

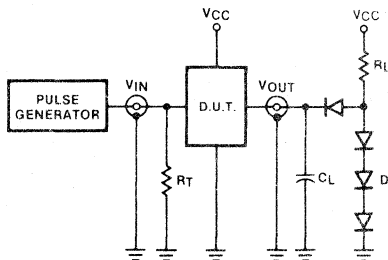


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH}	Propagation delay	Waveform 1				ns
t _{PHL}	Address to output	3 logic levels		30	30	
t _{PLH}	Propagation delay	Waveform 1				ns
t _{PHL}	Address to output	2 logic levels		25	25	

TEST CIRCUITS AND WAVEFORMS

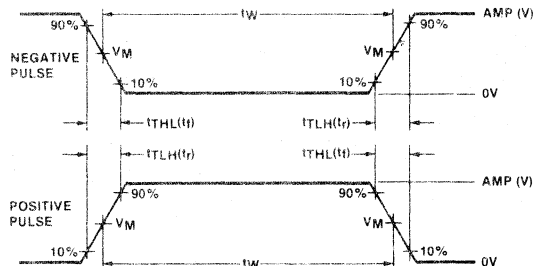
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODER/DRIVER

54/7445

BCD-To-Decimal Decoder/Driver (Open Collector)

- 80mA output sink capability
- 30V output breakdown voltage
- Ideally suited as lamp or solenoid driver
- See '42 for standard TTL output version
- See '145 for "LS" version

TYPE	MAX I_{OL}	TYPICAL SUPPLY CURRENT (Total)
7445	80mA	43mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7445N	

DESCRIPTION

The '45 decoder accepts BCD inputs on the A_0 to A_3 address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are off. This device can therefore be used as a 1-of-8 decoder with A_3 used as an active LOW enable.

The '45 can sink 20mA while maintaining the standardized guaranteed output LOW voltage (V_{OL}) of 0.4V, but it can sink up to 80mA with a guaranteed V_{OL} of less than 0.9V.

The '45 features an output breakdown voltage of 30V and is ideally suited as a lamp or solenoid driver.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

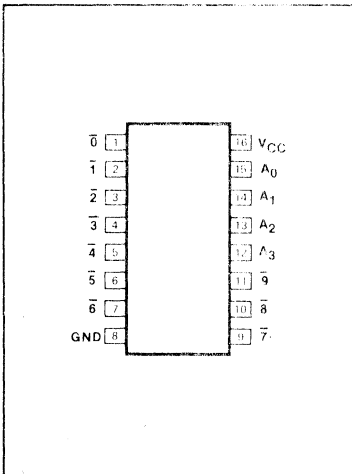
PINS	DESCRIPTION	54/74
A_0 - A_3	Inputs	1ui
$\bar{0}$ - $\bar{9}$	Outputs	12.5ui†

NOTE

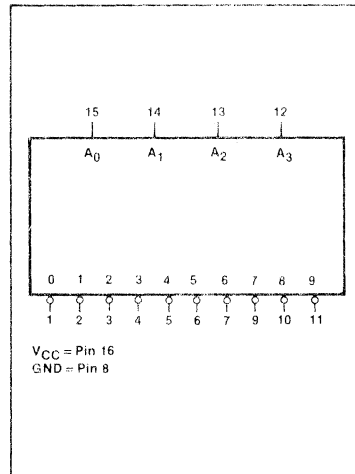
† A 54/74 unit load (ui) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} .



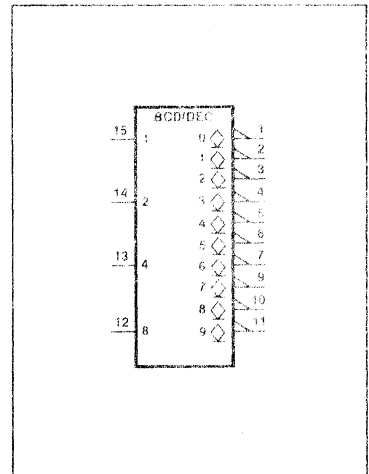
PIN CONFIGURATION



LOGIC SYMBOL



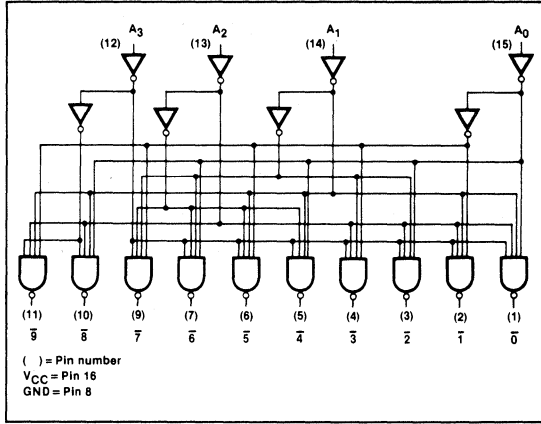
LOGIC SYMBOL (IEEE/IEC)



DECODER/DRIVER

54/7445

LOGIC DIAGRAM



FUNCTION TABLE

A ₃	A ₂	A ₁	A ₀	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +30	-0.5 to +30	V
T _A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT		
		Min	Nom	Max			
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	V	
V _{IH}	HIGH-level input voltage	2.0			V		
V _{IL}	LOW-level input voltage	Mil			+0.8	V	
		Com'l			+0.8	V	
I _{IK}	Input clamp current				-12	mA	
V _{OH}	HIGH-level output voltage				30	V	
I _{OL}	LOW-level output current	Mil			80	mA	
		Com'l			80	mA	
T _A	Operating free-air temperature	Mil	-55			+125	°C
		Com'l	0			70	°C

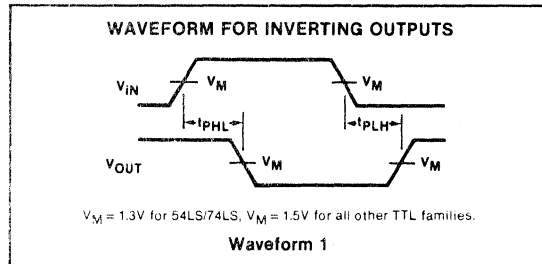
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7445			UNIT
		Min	Typ ²	Max	
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 30V$			250	μA
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$			0.4	V
				0.5	0.9
V_{IK} input clamp voltage	$V_{CC} = \text{MIN}, I_1 = I_{IK}$			-1.5	V
I_1 Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_1 = 5.5V$			1.0	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_1 = 2.4V$			40	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_1 = 0.4V$			-1.6	mA
I_{CC} Supply current ³ (total)	$V_{CC} = \text{MAX}$	Mil	43	62	mA
		Com'l	43	70	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.
- Measure I_{CC} with all inputs grounded and outputs open.

AC WAVEFORM



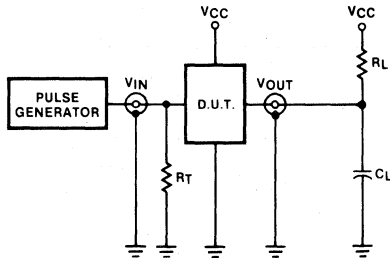
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AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		$C_L = 15\text{pF}, R_L = 100\Omega$		
		Min	Max	
t_{PLH} Propagation delay	Waveform 1		50	ns
t_{PHL} Address to output			50	

TEST CIRCUITS AND WAVEFORMS

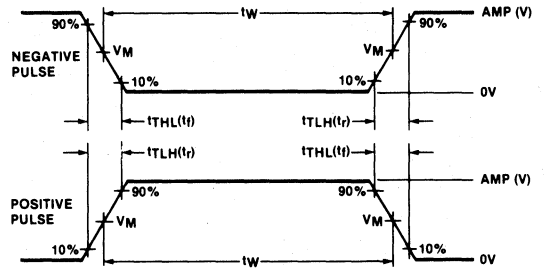
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

GATES

54/7451, LS51, S51

**'51, 'S51 Dual 2-Wide 2-Input AND-OR-Invert Gate
'LS51 Dual 2-Wide 3-Input, 2-Wide 2-Input AND-OR-Invert Gate**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7451	11ns	5.7mA
74LS51	12ns	1.1mA
74S51	3.5ns	11mA

FUNCTION TABLE
'51, 'S51, 1/2 'LS51

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
All other combinations				H

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7451N • N74LS51N N74S51N	
Plastic SO	N74LS51D • N74S51D	
Ceramic DIP		S54S51F • S54LS51F
Flatpack		S54S51W • S54LS51W

'LS51

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

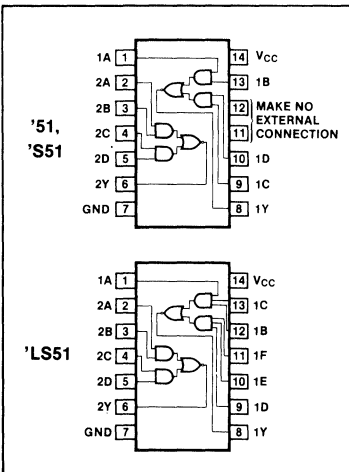
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1uI	1SuI	1LSuI
Y	Output	10uI	10SuI	10LSuI

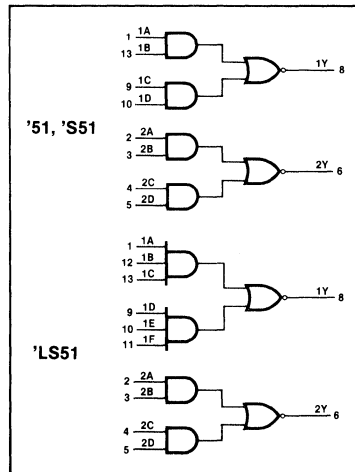
NOTE

Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (SuI) is 50µA I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL} .

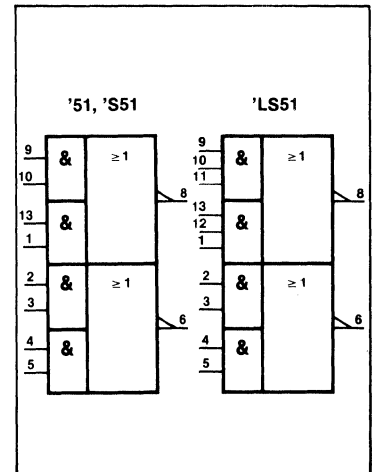
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-400			-400			-1000	μA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

NOTE

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

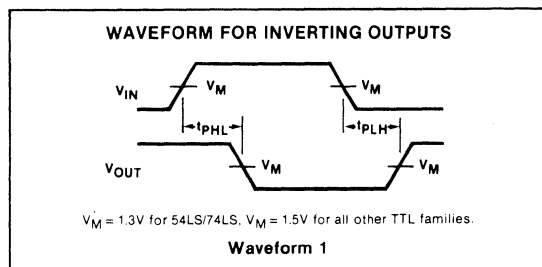
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/7451			54/74LS51			54/74S51			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4		V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5 ⁴	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5				-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0							1.0	mA
		V _I = 7.0V						0.1					mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40								μA
		V _I = 2.7V						20				50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6				-0.4				mA
		V _I = 0.5V										-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40		-100	mA	
		Com'l	-18		-55	-20		-100	-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		4	8		0.8	1.6		8.2	17.8	mA	
		I _{CCL} Outputs LOW		7.4	14		1.4	2.8		13.6	22	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 15		20 20		5.5 5.5	ns

4

GATE

54/74LS54

Four-Wide Two- & Three-Input AND-OR-Invert Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS54	12ns	0.9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS54N	
Plastic SO	N74LS54D	

FUNCTION TABLE

INPUTS										OUTPUT
A	B	C	D	E	F	G	H	J	K	Y
H	H	X	X	X	X	X	X	X	X	L
X	X	H	H	H	X	X	X	X	X	L
X	X	X	X	X	H	H	X	X	X	L
X	X	X	X	X	X	X	H	H	H	L
All other combinations										H

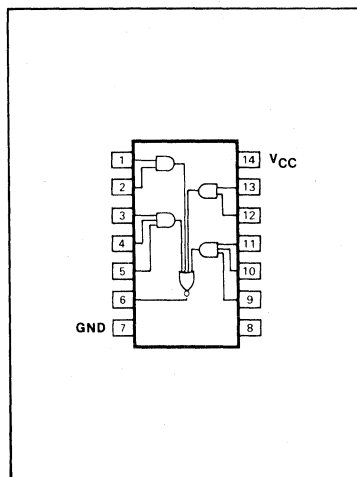
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

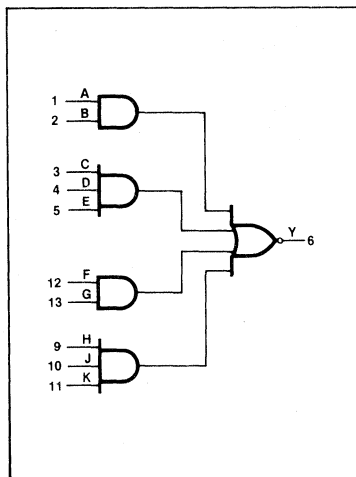
PINS	DESCRIPTION	54/74LS
A-K	Inputs	1LSul
Y	Output	10LSul

NOTE
 Where a 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

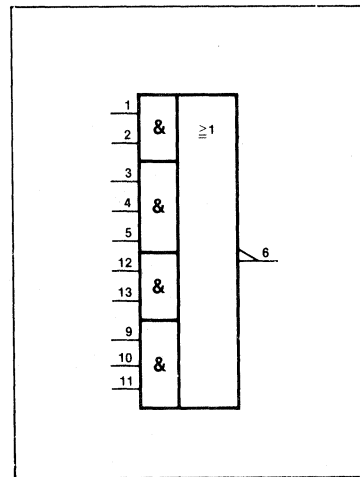
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I _{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current				- 400	μA
I _{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

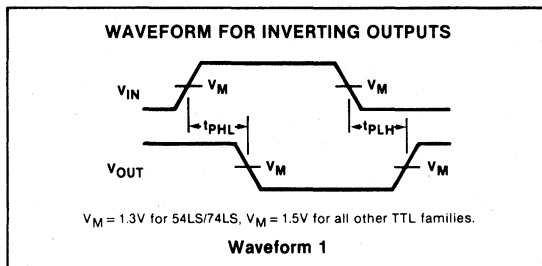
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS54			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V	
		Com'l	2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
		I _{OL} = 4mA	74LS	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			- 1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			- 0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		- 20	- 100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		0.8	1.6	mA
		I _{CCL} Outputs LOW		1.0	2.0	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		20 20	ns

Four-Two-Three-Two-Input AND-OR-Invert Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S64	3.5ns	8mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S64N	
Plastic SO	N74S64D	

FUNCTION TABLE

INPUTS											OUTPUT
A	B	C	D	E	F	G	H	J	K	L	Y
H	H	X	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

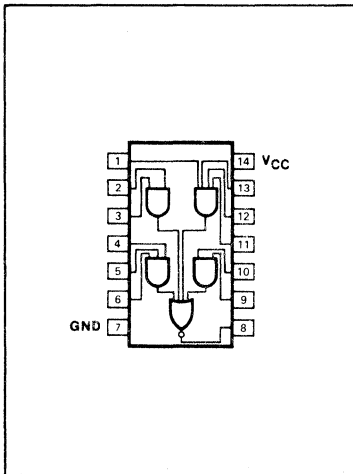
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

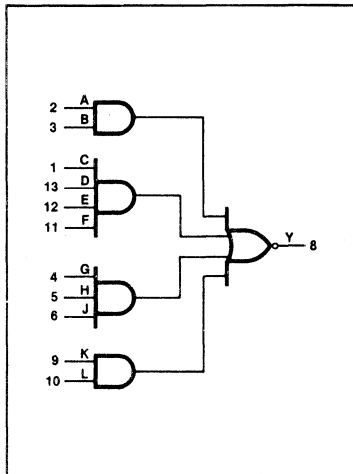
PINS	DESCRIPTION	54/74S
A-L	Inputs	1Sul
Y	Output	10Sul

NOTE
 A 54/74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

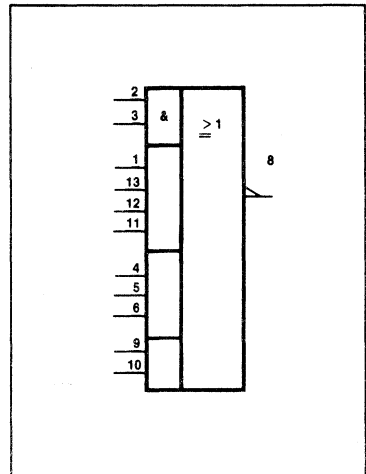
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

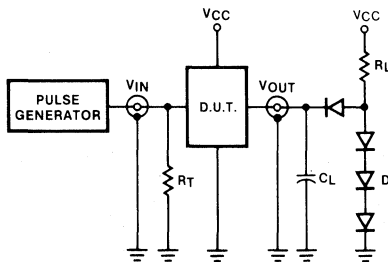
PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I_{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

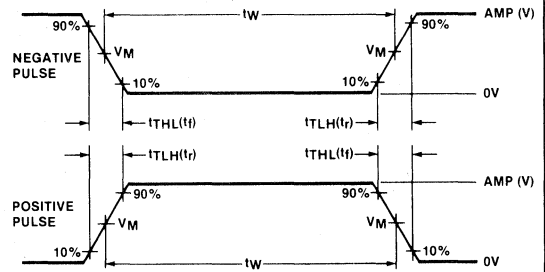
PARAMETER		54/74S			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				- 18	mA
I_{OH}	HIGH-level output current				- 1000	μA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{PLH} , t_{PHL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{PLH}	t_{PHL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

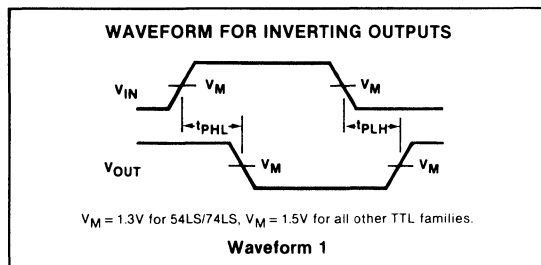
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74S64			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V
		Com'l	2.7	3.4	V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX	Mil		0.5	V
		Com'l		0.5	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			- 1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			- 2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	- 40		- 100	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH	7	12.5	mA
		I _{CCL} Outputs LOW	8.5	16	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74S		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		5.5 5.5	ns

FLIP-FLOPS

54/7473, LS73

Dual J-K Flip-Flop

DESCRIPTION

The '73 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 7473 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW transition. For the 7473, the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS73 is a negative edge-triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset (\bar{R}_D) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the \bar{Q} output HIGH.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7473	20MHz	10mA
74LS73	45MHz	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7473N • N74LS73N	
Ceramic DIP		S5473F • S54LS73F
Flatpack		S5473W • S54LS73W

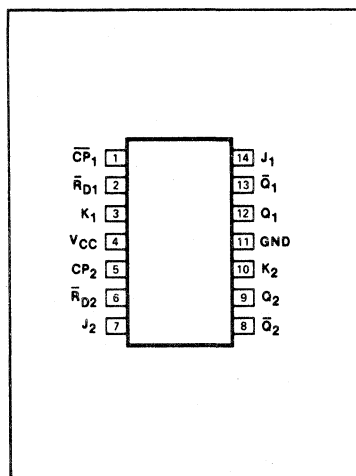
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
$\bar{C}P$	Clock input	2uI	4LSuI
\bar{R}_D	Reset input	2uI	3LSuI
J, K	Data inputs	1uI	1LSuI
Q, \bar{Q}	Outputs	10uI	10LSuI

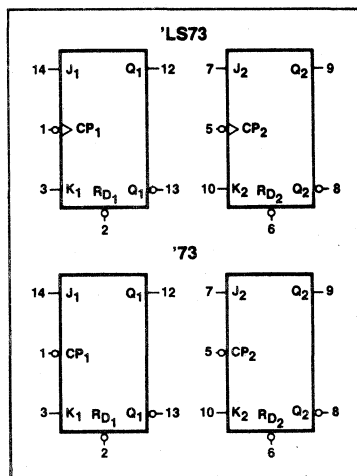
NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and -0.4mA I_{IL} .

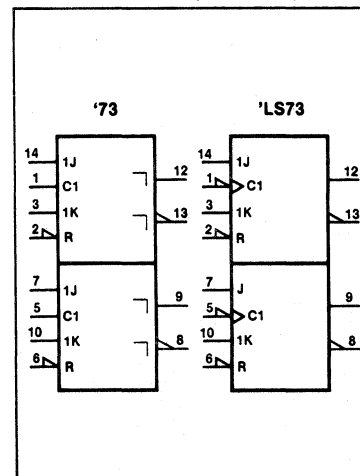
PIN CONFIGURATION



LOGIC SYMBOL



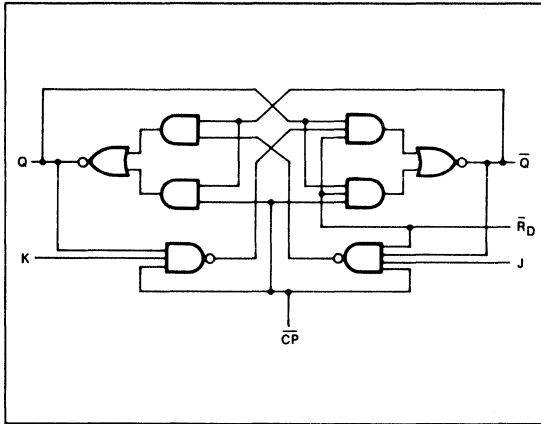
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/7473, LS73

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{R}_D	$\overline{CP}^{(b)}$	J	K	Q	\bar{Q}
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H		h	h	q	\bar{q}
Load "0" (Reset)	H		l	h	L	q
Load "1" (Set)	H		h	l	H	L
Hold "no change"	H		l	l	q	\bar{q}

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(a)
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(a)
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 = Positive Clock pulse.

NOTES

- a. The J and K inputs of the 7473 must be stable while the Clock is HIGH for conventional operation.
- b. The 74LS73 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-12			-18	mA
I_{OH} HIGH-level output current				-400			-400	μ A
I_{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

FLIP-FLOPS

54/7473, LS73

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7473			54/74LS73			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.2	0.4		0.25	0.4	V	
			Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.5		-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V	All Inputs				1.0		mA	
			J, K Inputs						0.1	mA
		V _I = 7.0V	\bar{R}_D Inputs						0.3	mA
			$\bar{C}\bar{P}$ Inputs						0.4	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	J, K Inputs				40		μ A	
			\bar{R}_D Inputs				80		μ A	
			$\bar{C}\bar{P}$ Inputs				80		μ A	
		V _I = 2.7V	J, K Inputs						20	μ A
			\bar{R}_D Inputs						60	μ A
			$\bar{C}\bar{P}$ Inputs						80	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	J, K Inputs				-1.6		-0.4	mA	
		\bar{R}_D Inputs				-3.2		-0.8	mA	
		$\bar{C}\bar{P}$ Inputs				-3.2		-0.8	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-57		-20		-100	mA
		Com'l	-18		-57		-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX				10	40		4	8	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum Clock frequency	Waveform 3	15		30		MHz
t _{PLH} Propagation delay	Waveform 1, 'LS73 Waveform 3, '73		25		20	ns
t _{PHL} Clock to output			40		30	
t _{PLH} Propagation delay	Waveform 2		25		20	ns
t _{PHL} \bar{R}_D to output			40		30	

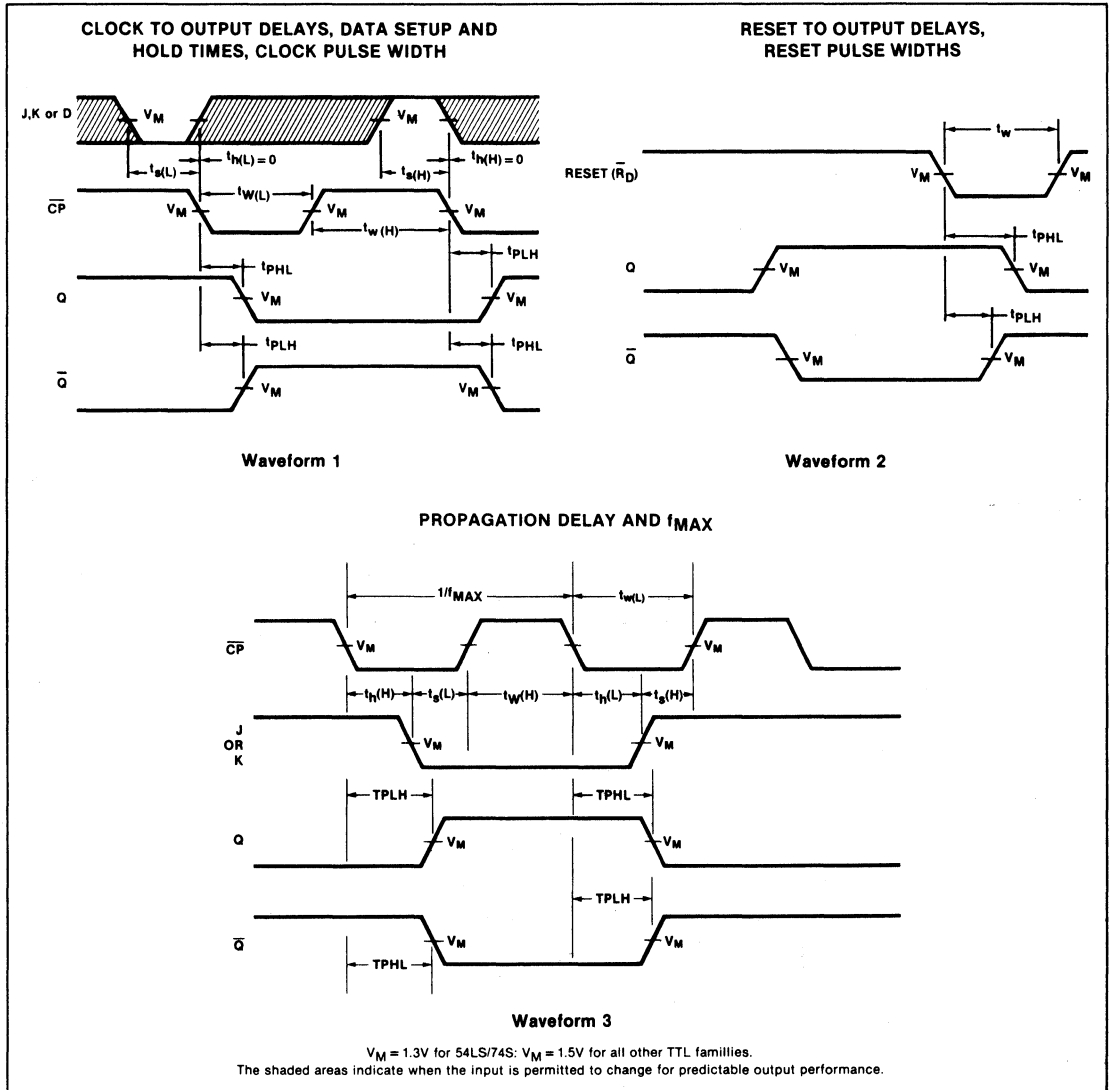
NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		Min	Max	Min	Max	
$t_{w(H)}$ Clock pulse width (HIGH)	Waveform 1	20		20		ns
$t_{w(L)}$ Clock pulse width (LOW)	Waveform 1	47				ns
$t_{w(L)}$ Reset pulse width (LOW)	Waveform 2	25		25		ns
t_s Setup time J or K to Clock ^(a)	Waveform 1	0		20		ns
t_h Hold time J or K to Clock	Waveform 1	0		0		ns

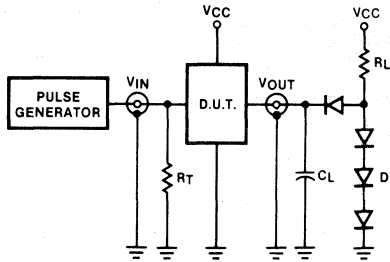
AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS

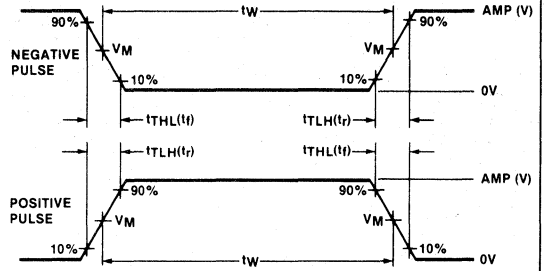
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOPS

54/7474, LS74A, S74

Dual D-Type Flip-Flop

DESCRIPTION

The '74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and Q outputs.

Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7474	25MHz	17mA
74LS74A	33MHz	4mA
74S74	100MHz	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7474N • N74LS74AN N74S74N	
Plastic SO	N741S74AD • N74S74D	
Ceramic DIP		S5474F • S54LS74AF S54S74F
Flatpack		S5474W • S54LS74AW S54S74W
LLCC		S54LS74AG

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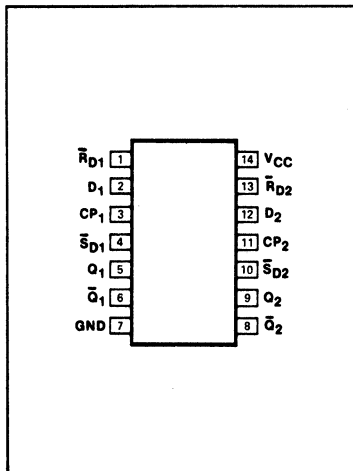
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
D	Input	1uI	1Sul	1LSul
\bar{R}_D	Input	2uI	3Sul	2LSul
\bar{S}_D	Input	1uI	2Sul	2LSul
CP	Input	2uI	2Sul	1LSul
Q, \bar{Q}	Outputs	10uI	10Sul	10LSul

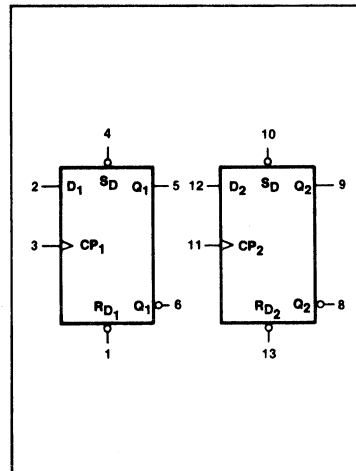
NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

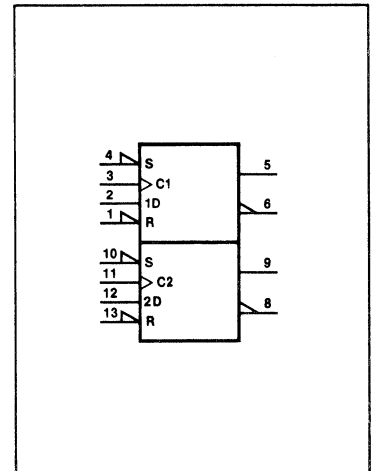
PIN CONFIGURATION



LOGIC SYMBOL



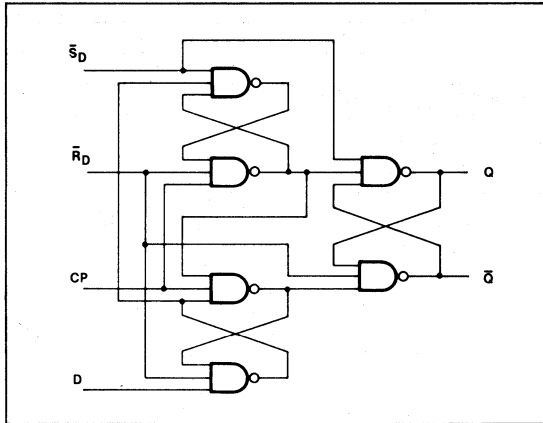
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/7474, LS74A, S74

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	\bar{R}_D	CP	D	Q	\bar{Q}
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined ^(a)	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

NOTE

(a) Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I_{IK} Input clamp current				-12			-18			-18	mA
I_{OH} HIGH-level output current				-400			-400			-1000	μA
I_{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

NOTE
 $V_{IL} = +0.7V$ MAX for 54S at $T_A = +125^\circ C$ only.

FLIP-FLOPS

54/7474, LS74A, S74

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/7474			54/74LS74A			54/74S74			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4		V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁶	V	
			Com'l		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA	74LS					0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V				1.0					1.0	mA	
		V _I = 7.0V	D input					0.1					mA
			\bar{R}_D input						0.2				mA
			\bar{S}_D input						0.2				mA
			CP input						0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	D input			40						μ A	
			\bar{R}_D input			120						μ A	
			\bar{S}_D input			80						μ A	
		CP input			80						μ A		
		V _I = 2.7V	D input						20			50	μ A
			\bar{R}_D input						40			150	μ A
	\bar{S}_D input							40			100	μ A	
	CP input							20			100	μ A	
	I _{IL} LOW-level input current ⁵	V _{CC} = MAX	V _I = 0.4V	D input			-1.6			-0.4			mA
				\bar{R}_D input			-3.2			-0.8			mA
\bar{S}_D input						-1.6			-0.8			mA	
CP input					-3.2			-0.4			mA		
V _I = 0.5V			D input									-2	mA
			\bar{R}_D input									-6	mA
		\bar{S}_D input									-4	mA	
		CP input									-4	mA	
I _{OS} Short-circuit output current ³		V _{CC} = MAX	Mil	-20		-57	-20		-100	-40		-100	mA
			Com'l	-18		-57	-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			17	30		4	8		30	50	mA	

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the shorted circuit should not exceed one second.
- Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and \bar{Q} outputs HIGH in turn.
- Set is tested with reset HIGH and reset is tested with set HIGH.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		C _L = 15pF, R _L = 280 Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	15		25		75		MHz
t _{PLH} Propagation delay	Waveform 1		25		25		9	ns
t _{PHL} Clock to output			40		40		9	
t _{PLH} Propagation delay	Waveform 2		25		25		6	ns
t _{PHL} Set or Reset to output		CP = HIGH		40		40		
t _{PHL} Set or Reset to output	Waveform 2		40		40		8	ns
	CP = LOW							

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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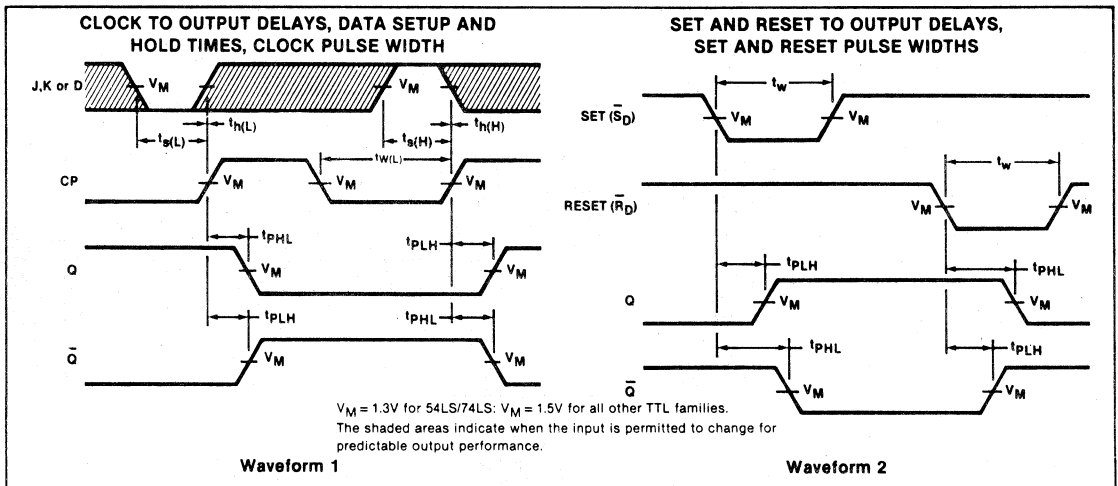
FLIP-FLOPS

54/7474, LS74A, S74

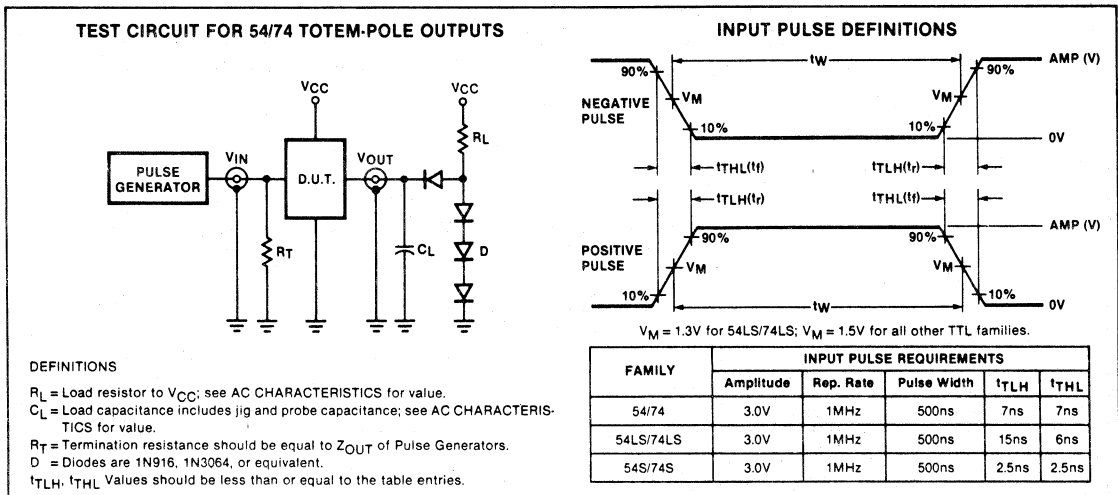
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{W(H)}$ Clock pulse width (HIGH)	Waveform 1	30		25		6		ns
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	37				7.3		ns
$t_{W(L)}$ Set or reset pulse width (LOW)	Waveform 2	30		25		7		ns
$t_s(H)$ Setup time (HIGH) data to clock	Waveform 1	20		20		3		ns
$t_s(L)$ Setup time (LOW) data to clock	Waveform 1	20		20		3		ns
t_h Hold time data to clock	Waveform 1	5		5		2		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



LATCHES

54/7475, LS75

Quad Bistable Latch

- 4-bit bistable latch
- Refer to 54LS/74LS375 for V_{CC} and GND on corner pins

DESCRIPTION

The '75 has four bistable latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the Data inputs as long as E is HIGH. The data on the D inputs one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7475	18ns (t_{PLH}) 9ns (t_{PHL})	32mA
74LS75	15ns (t_{PLH}) 9ns (t_{PHL})	6.3mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7475N • N74LS75N	
Plastic SO	N74LS25D	
Ceramic DIP		S5475F • S54LS75F
Flatpack		S5475W • S54LS75W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

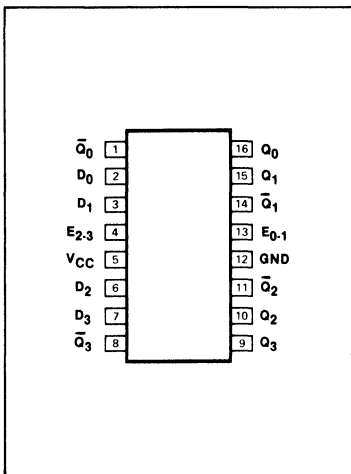
PINS	DESCRIPTION	54/74	54/74LS
D	Input	2uI	1LSUI
E	Input	4uI	4LSUI
All	Outputs	10uI	10LSuI

NOTE

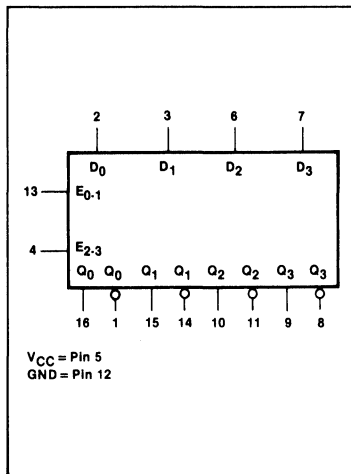
Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA$.



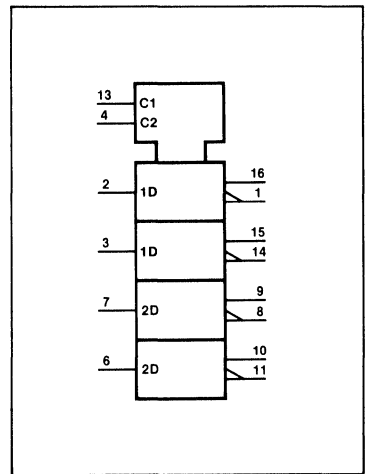
PIN CONFIGURATION



LOGIC SYMBOL



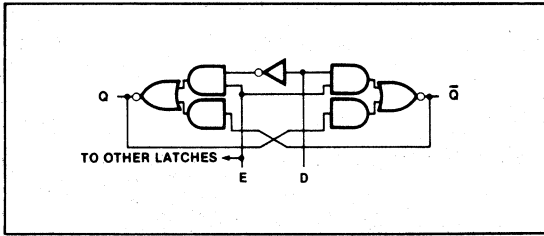
LOGIC SYMBOL (IEEE/IEC)



LATCHES

54/7475, LS75

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS	
	E	D	Q	\bar{Q}
Data Enabled	H	L	L	H
	H	H	H	L
Data Latched	L	X	q	\bar{q}

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-12			-18	mA
I_{OH} HIGH-level output current				-400			-400	μ A
I_{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

LATCHES

54/7475, LS75

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7475			54/74LS75			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l			0.2	0.4		0.35	0.5
		I _{OL} = 4mA	74LS						0.25	0.4
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}							-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						1.0	mA	
		V _I = 7.0V	D inputs						0.1	mA
			E inputs						0.4	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	D inputs			80			μA	
			E inputs			160			μA	
		V _I = 2.7V	D inputs						20	μA
			E inputs						80	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	D inputs			-3.2			-0.4	mA
			E inputs			-6.4			-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-57	-20			-100	mA
		Com'l	-18		-57	-20			-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		32	46		6.3	12	mA	
		Com'l		32	53		6.3	12	mA	

- NOTES**
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with all inputs grounded and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay Data to Q output	Waveform 1		30 25		27 17	ns
t _{PLH} t _{PHL} Propagation delay Data to Q̄ output	Waveform 2		40 15		20 15	ns
t _{PLH} t _{PHL} Propagation delay Enable to Q output	Waveform 3		30 15		27 25	ns
t _{PLH} t _{PHL} Propagation delay Enable to Q̄ output	Waveform 3		30 15		30 15	ns

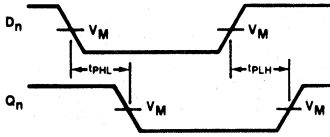
AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		Min	Max	Min	Max	
t _W Enable pulse width	Waveform 3	20		20		ns
t _s Setup time, Data to Enable	Waveform 4	20		20		ns
t _h Hold time, Data to Enable	Waveform 4	5.0		5.0		ns

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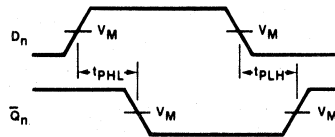
AC WAVEFORMS

PROPAGATION DELAY DATA TO Q OUTPUTS



Waveform 1

PROPAGATION DELAY DATA TO Q̄ OUTPUTS

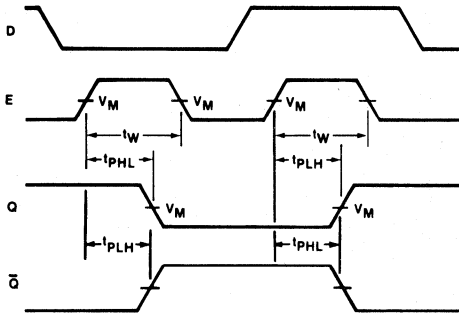


Waveform 2

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

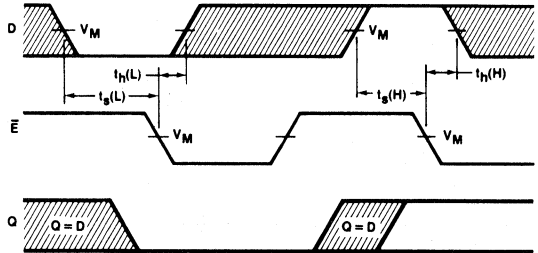
The shaded areas indicate when the input is permitted to change for predictable output performance.

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



Waveform 3

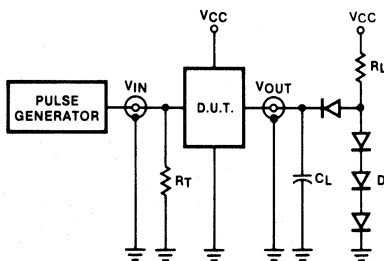
DATA SETUP AND HOLD TIMES



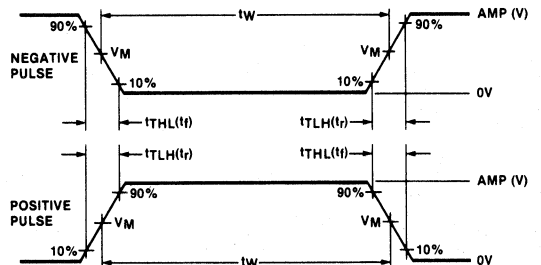
Waveform 4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOPS

54/7476, LS76

Dual J-K Flip-Flop

DESCRIPTION

The '76 is a dual J-K flip-flop with individual J, K, Clock, Set and Reset inputs. The 7476 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge-triggered flip-flop. The J and K inputs must be stable only one setup time prior to the HIGH-to-LOW Clock transition.

The Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs. When LOW, they override the Clock and Data inputs, forcing the outputs to the steady state levels as shown in the Function Table.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7476	20MHz	10mA
74LS76	45MHz	4mA

ORDERING CODE

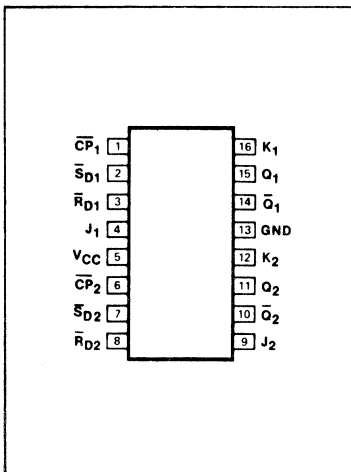
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7476N • N74LS76N	
Ceramic DIP		S5476F • S54LS76F
Flatpack		S5476W • S54LS76W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

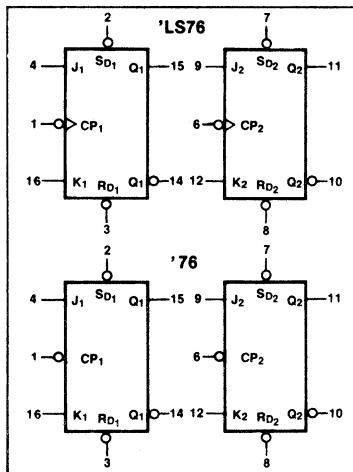
PINS	DESCRIPTION	54/74	54/74LS
$\bar{C}\bar{P}$	Clock input	2uI	2LSuI
\bar{R}_D, \bar{S}_D	Reset and Set inputs	2uI	2LSuI
J, K	Data inputs	1uI	1LSuI
Q, \bar{Q}	Outputs	10uI	10LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and -0.4mA I_{IL} .

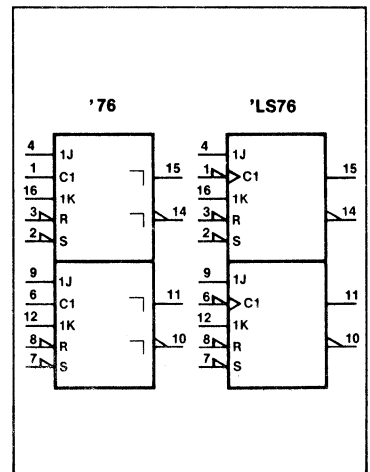
PIN CONFIGURATION



LOGIC SYMBOL



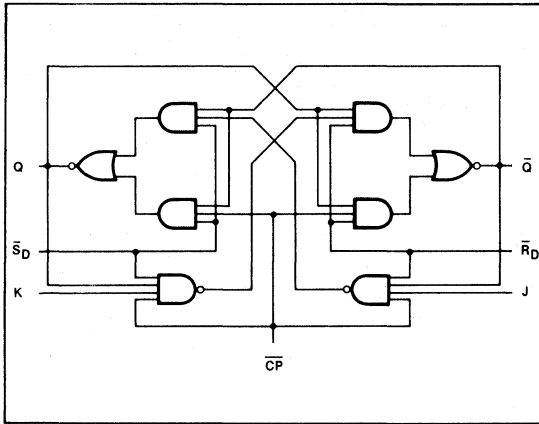
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/7476, LS76

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	$\overline{CP}^{(b)}$	J	K	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined ^(a)	L	L	X	X	X	H	H
Toggle	H	H	\downarrow	h	h	\bar{q}	q
Load "0" (Reset)	H	H	\downarrow	l	h	L	L
Load "1" (Set)	H	H	\downarrow	h	l	H	L
Hold "no change"	H	H	\downarrow	l	l	q	\bar{q}

- H = HIGH voltage level steady state.
- h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(c)
- L = LOW voltage level steady state.
- l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.^(c)
- q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
- X = Don't care.
- \downarrow = Positive Clock pulse.

NOTES

- a. Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.
- b. The 74LS76 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.
- c. The J and K inputs of the 7476 must be stable while the Clock is HIGH for conventional operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-12			-18	mA
I_{OH} HIGH-level output current				-400			-400	μ A
I_{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7476			54/74LS76			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V				1.0			mA	
		V _I = 7.0V	J, K Inputs					0.1	mA	
			$\overline{S}_D, \overline{R}_D$ Inputs					0.3	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	J, K Inputs			40			μA	
			$\overline{S}_D, \overline{R}_D$ Inputs			80			μA	
			\overline{CP} Inputs			80			μA	
		V _I = 2.7V	J, K Inputs					20	μA	
			$\overline{S}_D, \overline{R}_D$ Inputs					60	μA	
			\overline{CP} Inputs					80	μA	
I _{IL} LOW-level input current ⁵	V _{CC} = MAX, V _I = 0.4V	J, K Inputs			-1.6			-0.4	mA	
		$\overline{S}_D, \overline{R}_D$ Inputs			-3.2			-0.8	mA	
		\overline{CP} Inputs			-3.2			-0.8	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-57	-20		-100	mA	
		Com'l	-18		-57	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			10	40		4	8	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs HIGH in turn.
- \overline{S}_D is tested with \overline{R}_D HIGH, and \overline{R}_D is tested with \overline{S}_D HIGH.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
f _{MAX} Maximum Clock frequency	Waveform 3	15		30		MHz
t _{PLH} Propagation delay	Waveform 1, 'LS76		25		20	ns
t _{PHL} Clock to output	Waveform 3, '76		40		30	
t _{PLH} Propagation delay	Waveform 2		25		20	ns
t _{PHL} \overline{S}_D or \overline{R}_D to output			40		30	

NOTE

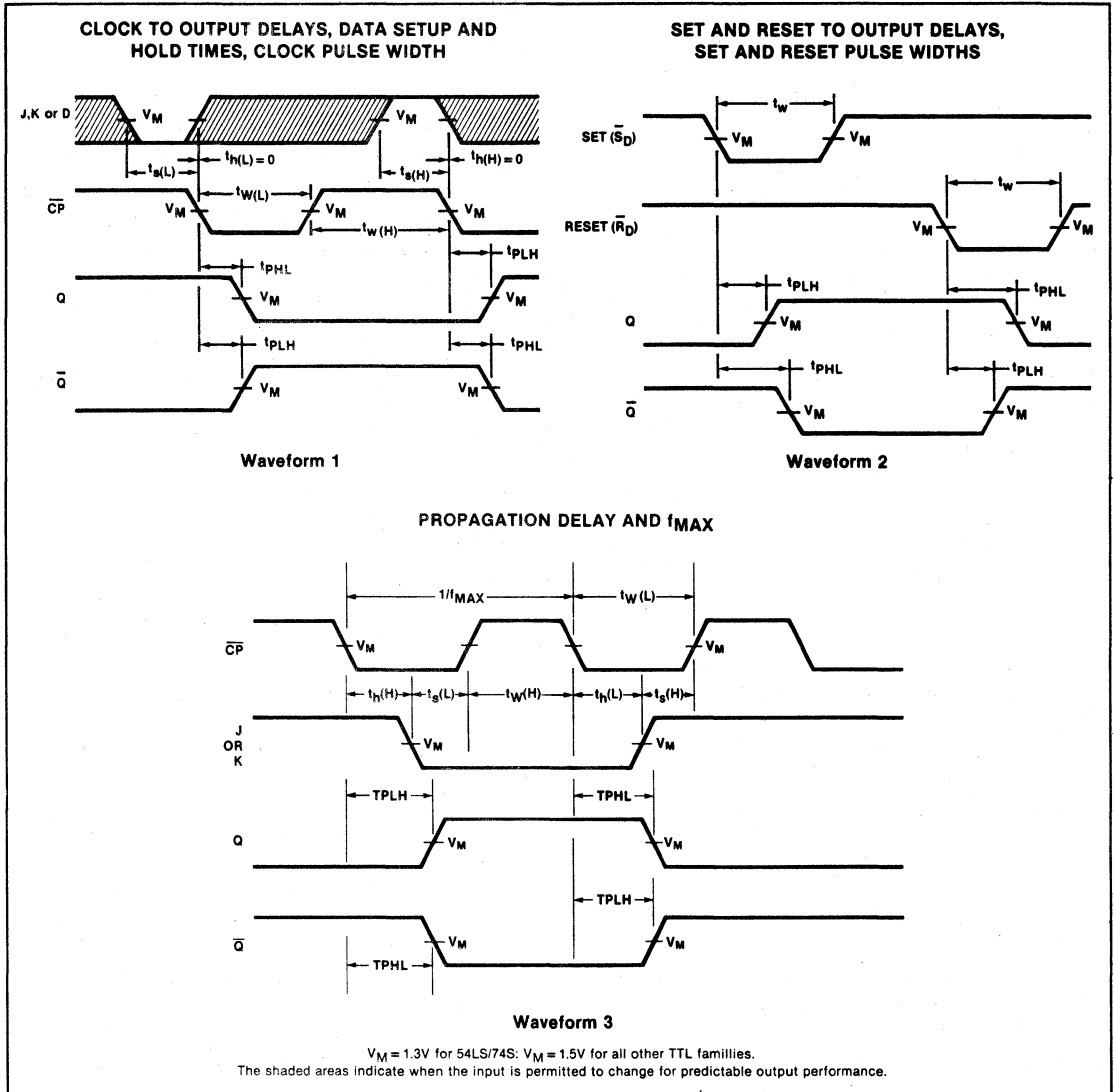
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

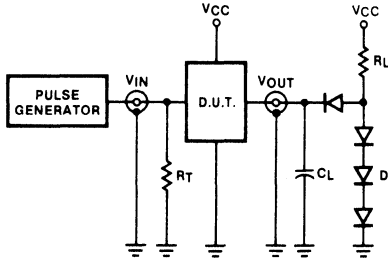
PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		Min	Max	Min	Max	
$t_{w(H)}$	Clock pulse width (HIGH)	20		20		ns
$t_{w(L)}$	Clock pulse width (LOW)	47				ns
$t_{w(L)}$	Reset pulse width (LOW)	25		25		ns
t_s	Setup time J or K to Clock ^(c)	0		20		ns
t_h	Hold time J or K to Clock	0		0		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

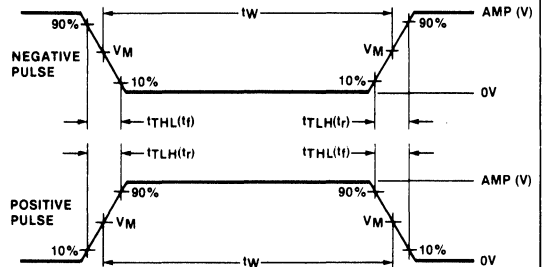
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

ADDERS

54/7483, LS83A

4-Bit Full Adder

- High speed 4-bit binary addition
- Cascadeable in 4-bit increments
- LS83A has fast internal carry lookahead
- See '283 for corner power pin version

TYPE	TYPICAL ADD TIMES (Two 8-bit Words)	TYPICAL SUPPLY CURRENT (Total)
7483	23ns	66mA
74LS83A	25ns	19mA

DESCRIPTION

The '83 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs (Σ_1 - Σ_4) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the '83 can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). See Function Table. With active-HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN} , A_1 , B_1 , can arbitrarily be assigned to pins 10, 11, 13, etc.

ORDERING CODE

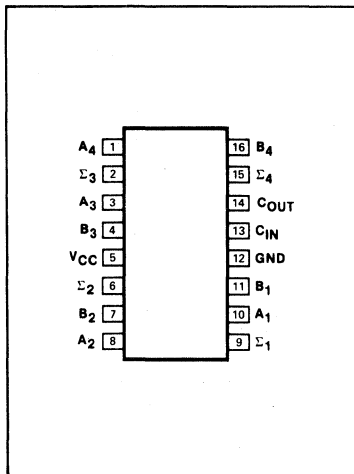
PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7483N • N74LS83AN	
Plastic SO	N74LS83AD	
Ceramic DIP		S5483F • S54LS83AF
Flatpack		S5483W • S54LS83AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

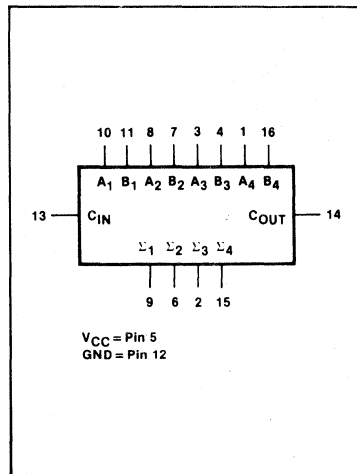
PINS	DESCRIPTION	54/74	54/74LS
$A_1, B_1, A_3, B_3, C_{IN}$	Inputs	2ul	
A_2, B_2, A_4, B_4	Inputs	1ul	
A, B	Inputs		2LSul
C_{IN}	Input		1LSul
Sum	Outputs	10ul	10LSul
Carry	Output	5ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$ and a 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

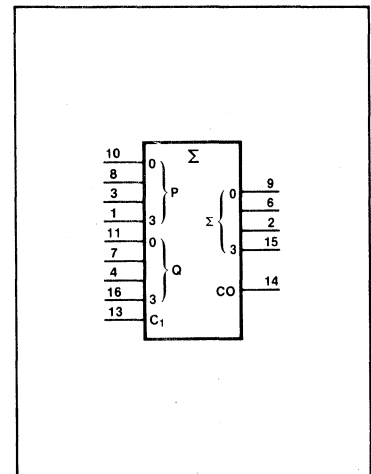
PIN CONFIGURATION



LOGIC SYMBOL



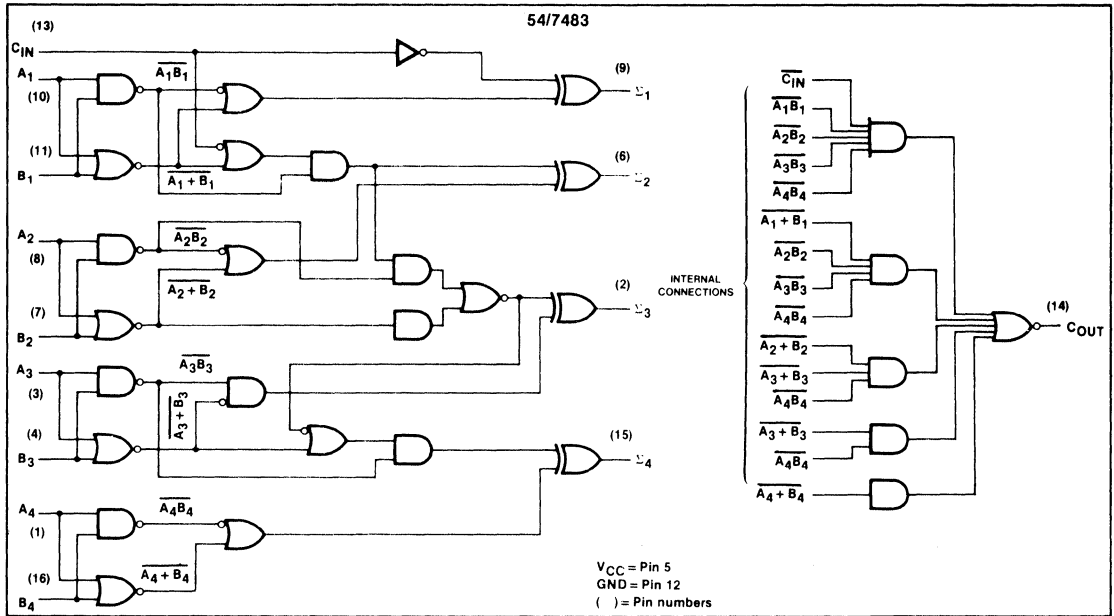
LOGIC SYMBOL (IEEE/IEC)



ADDERS

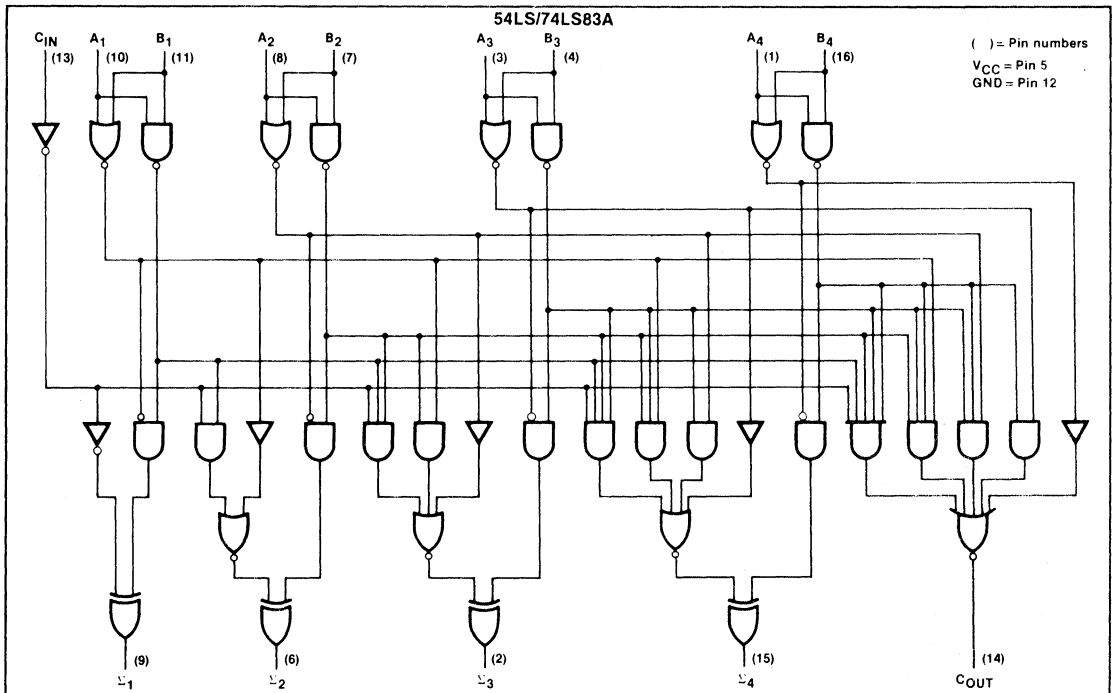
54/7483, LS83A

LOGIC DIAGRAM



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LOGIC DIAGRAM



ADDERS

54/7483, LS83A

FUNCTION TABLE

PINS	C _{IN}	A ₁	A ₂	A ₃	A ₄	B ₁	B ₂	B ₃	B ₄	Σ ₁	Σ ₂	Σ ₃	Σ ₄	C _{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10 + 9 = 19)
(carry + 5 + 6 = 12)

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current	Sum			-800			-400	μA
	Carry			-400			-400	μA
I _{OL} LOW-level output current	Sum	Mil		16			4	mA
		Com'l		16			8	mA
	Carry	Mil		8			4	mA
		Com'l		8			8	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

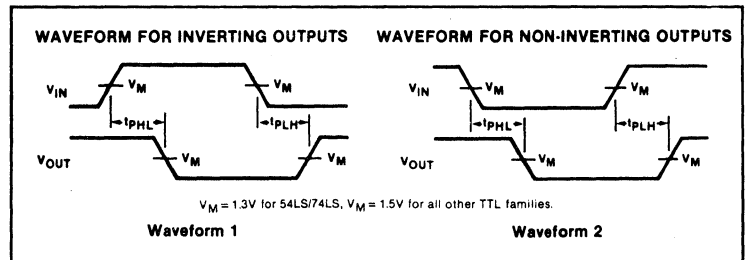
PARAMETER	TEST CONDITIONS ¹		54/7483			54/74LS83A			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		V	
		Com'l	2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.25	0.4	V	
		I _{OL} = 4mA					0.35	0.5	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA	
		V _I = 7.0V	A, B Inputs					0.2	mA	
C _{IN} input							0.1	mA		
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	A ₁ , B ₁ , A ₃ , B ₃ , C _{IN}		80				μA	
			A ₂ , B ₂ , A ₄ , B ₄		40				μA	
		V _I = 2.7V	A, B inputs					40	μA	
			C _{IN} input					20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	A ₁ , B ₁ , A ₃ , B ₃ , C _{IN}			-3.2				mA	
		A ₂ , B ₂ , A ₄ , B ₄			-1.6				mA	
		A, B inputs						-0.8	mA	
		C _{IN} input						-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Sum outputs	Mil	-20	-55	-20		-100	mA	
			Com'l	-18	-55	-20		-100	mA	
		C _{OUT} output	Mil	-20	-70	-20		-100	mA	
			Com'l	-18	-70	-20		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX, outputs open	All inputs at 4.5V	Mil		66	99		19	34	mA
			Com'l		66	110		19	34	mA
		All inputs grounded						22	39	mA
		All B inputs low, other inputs at 4.5V						19	34	mA

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NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		$C_L = 50\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_1	Waveforms 1 & 2		34 34	24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_2	Waveforms 1 & 2		35 35	24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_3	Waveforms 1 & 2		50 40	24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_4	Waveforms 1 & 2		50 50	24 24	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveforms 1 & 2		40 35	24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2 $R_L = 780\Omega$ for 54/7483		20 20	17 22	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveforms 1 & 2 $R_L = 780\Omega$ for 54/7483		22 22	17 17	ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

COMPARATORS

54/7485, LS85, S85

4-Bit Magnitude Comparator

- Magnitude comparison of any binary words
- Serial or parallel expansion without extra gating
- Use 54S/74S85 for very high speed comparisons

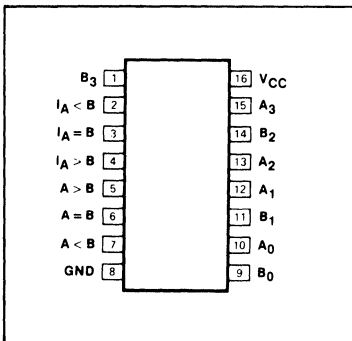
DESCRIPTION

The '85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted (A_0-A_3) and (B_0-B_3), where A_3 and B_3 are the most significant bits.

The operation of the '85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the $A>B$, $A=B$ and $A<B$ outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B} = \text{LOW}$, $I_{A=B} = \text{HIGH}$, and $I_{A<B} = \text{LOW}$.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7485	23ns	55mA
74LS85	23ns	10mA
74S85	12ns	73mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7485N • N74LS85N N74S85N	
Plastic SO	N74LS85D • N74S85D	
Ceramic DIP		S5485F • S54LS85F S54S85F
Flatpack		S5485W • S54LS85W S54S85W
LLCC		S54LS85G



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
$A_0-A_3, B_0-B_3, I_{A=B}$	Inputs	3ul	3Sul	3LSul
$I_{A<B}, I_{A>B}$	Inputs	1ul	1Sul	1LSul
$A=B, A<B, A>B$	Outputs	10ul	10Sul	10LSul

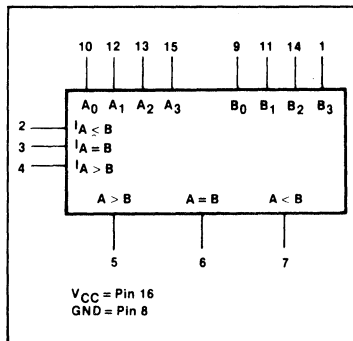
NOTE

A 54/74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 54/74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and a 54/74LS-unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$

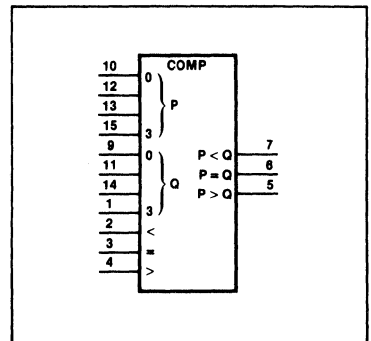
The parallel expansion scheme shown in Figure A demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by

labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ LOW. The '85 can be used as a 5-bit comparator only when the outputs are used to drive the (A_0-A_3) and (B_0-B_3) inputs of another '85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

LOGIC SYMBOL



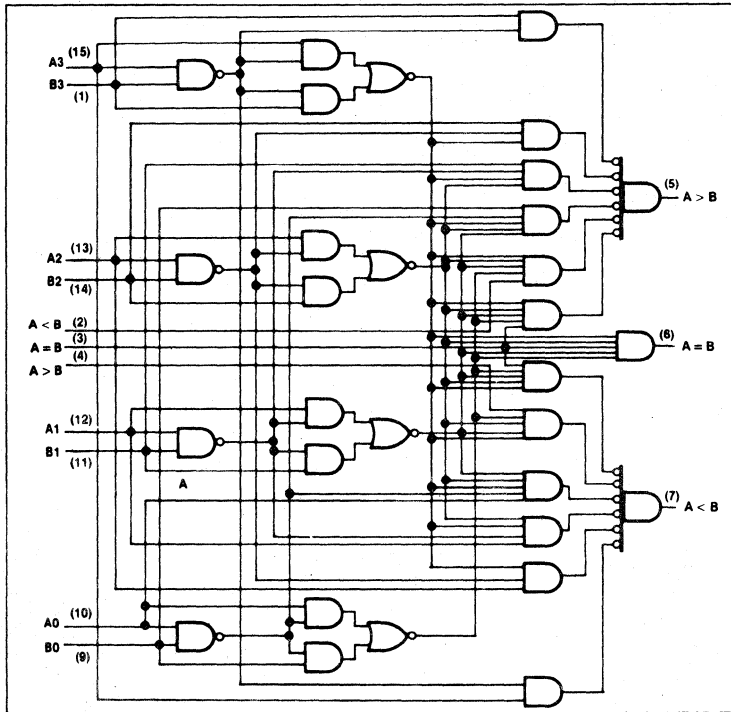
LOGIC SYMBOL (IEEE/IEC)



COMPARATORS

54/7485, LS85, S85

LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	I _{A>B}	I _{A<B}	I _{A=B}	A > B	A < B	A = B
A ₃ > B ₃	X	X	X	X	X	X	H	L	L
A ₃ < B ₃	X	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ > B ₂	X	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ < B ₂	X	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	X	X	X	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	L	L	H	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	H	L	L	H	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	X	X	H	L	L	H
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	H	H	L	L	L	L
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	L	L	L	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

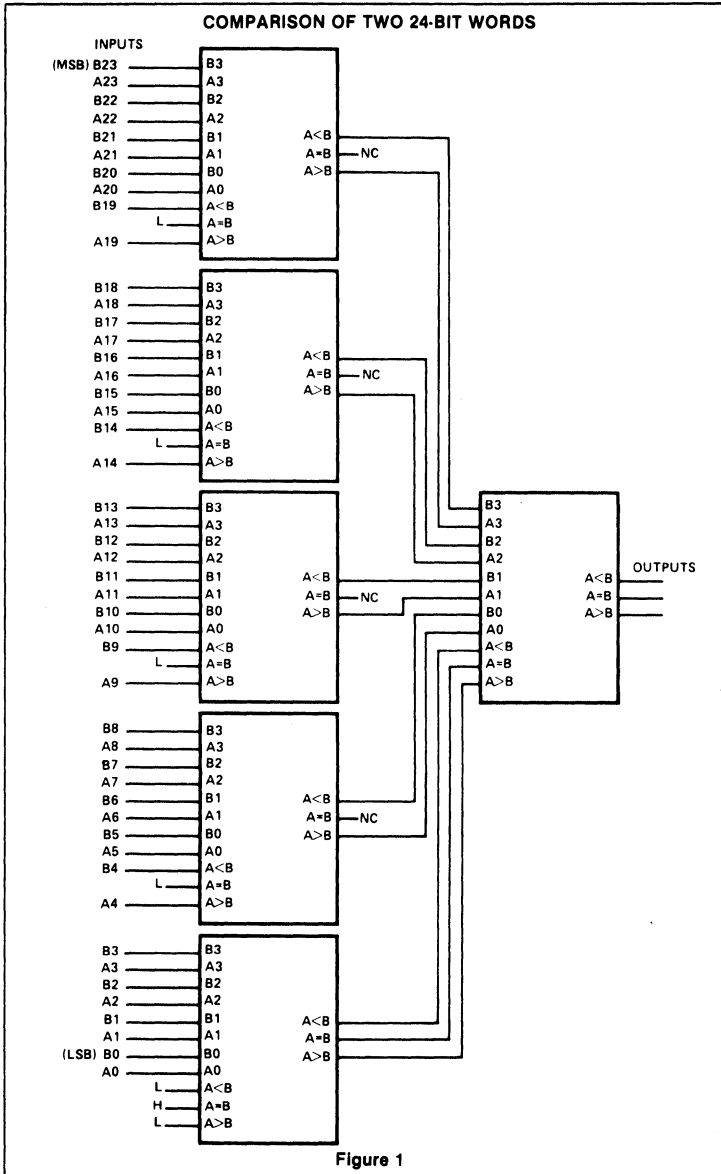


TABLE 1.

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS		
		54/74	54S/74S	54LS/74LS
1-4 Bits	1	23ns	12ns	23ns
5-25 Bits	2-6	40ns	22ns	46ns
25-120 Bits	8-31	63ns	34ns	69ns

COMPARATORS

54/7485, LS85, S85

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			2.0			V	
V _{IL}	LOW-level input voltage	Mil		+0.8			+0.7			+0.8	V	
		Com'l		+0.8			+0.8			+0.8	V	
I _{IK}	Input clamp current			-12			-18			-18	mA	
I _{OH}	HIGH-level output current			-400			-400			-1000	μA	
I _{OL}	LOW-level output current	Mil		16			4			20	mA	
		Com'l		16			8			20	mA	
T _A	Operating free-air temperature	Mil	-55	+125	-55		+125	-55		+125	°C	
		Com'l	0	70	0		70	0		70	°C	

NOTE

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

COMPARATORS

54/7485, LS85, S85

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/7485			54/74LS85			54/74S85			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4		V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁵	V	
			Com'l		0.2	0.4		0.35	0.5		0.5	V	
		I _{OL} = 4mA	74LS					0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5				-1.5			V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V				1.0					1.0	mA	
		V _I = 7.0V	I _{A<B} , I _{A>B}						0.1				mA
			Other inputs						0.3				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	I _{A<B} , I _{A>B}			40						μA	
			Other Inputs			120						μA	
		V _I = 2.7V	I _{A<B} , I _{A>B}						20		50	μA	
			Other inputs						60		150	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	I _{A<B} , I _{A>B}			-1.6			-0.4			mA	
			Other inputs			-4.8			-1.2			mA	
		V _I = 0.5V	I _{A<B} , I _{A>B}								-2.0	mA	
			Other inputs								-6.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40		-100	mA	
		Com'l	-18		-55	-20		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			55	88		10.4	20		73	115	mA	
	S54S85W only, T _A = 125°C										110	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the shorted circuit should not exceed one second.
- I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5V.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

4

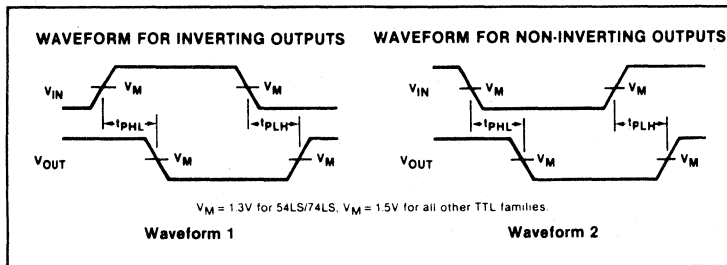
COMPARATORS

54/7485, LS85, S85

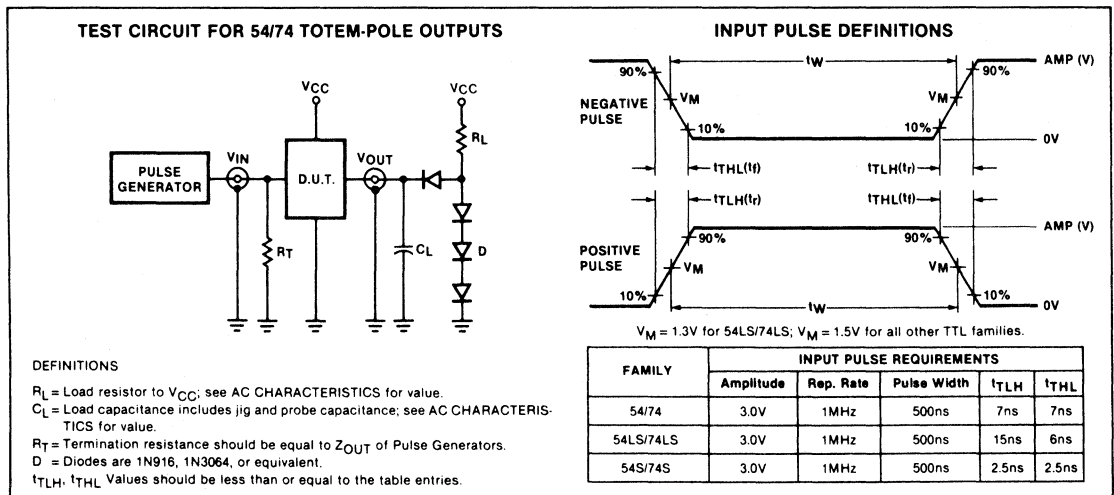
AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A < B, A > B output Waveform 1 3 logic levels		26 30		36 30		16 16.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output Waveform 2 4 logic levels		35 30		45 45		18 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A < B}$ and $I_{A = B}$ input to A > B output Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A = B}$ input to A = B output Waveform 2 2 logic levels		20 17		20 26		10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A > B}$ and $I_{A = B}$ input to A < B output Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



Quad Two-Input Exclusive-OR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7486	14ns	30mA
74LS86	10ns	6.1mA
74S86	7ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7486N • N74LS86N N74S86N	
Plastic SO	N74LS86D • N74S86D	
Ceramic DIP		S5486F • S54LS86F S54S86F
Flatpack		S5486W • S54LS86W S54S86W
LLCC		S54LS86G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

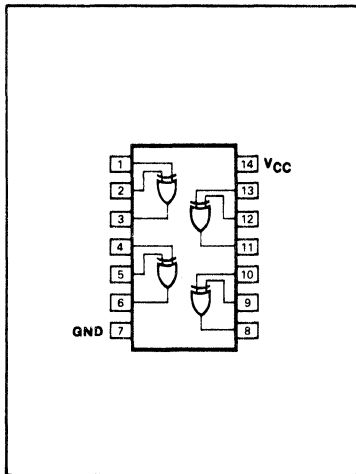
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

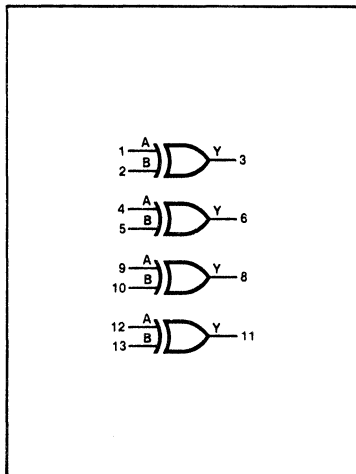
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ui	1Sui	1LSui
Y	Output	10ui	10Sui	10LSui

NOTE
Where a 54/74 unit load (ui) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sui) is 50µA I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSui) is 20µA I_{IH} and -0.4mA I_{IL} .

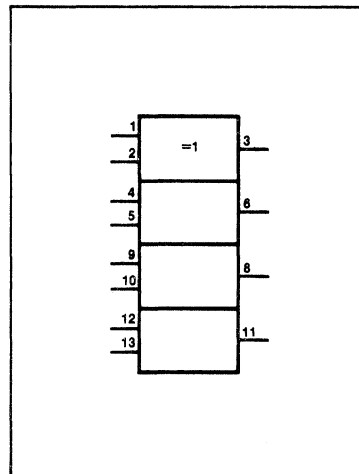
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

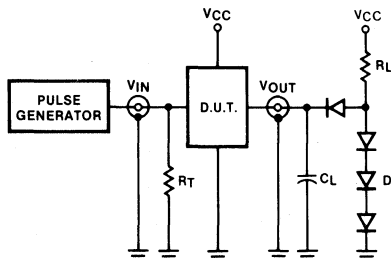
PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-800			-400			-1000	μA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

NOTE

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

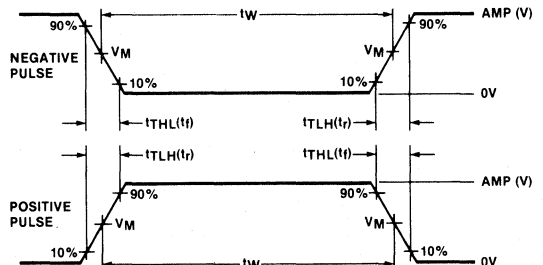
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

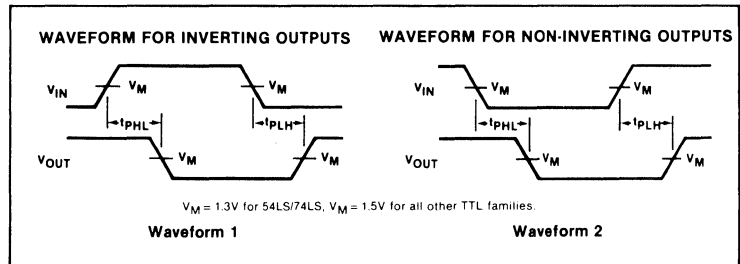
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/7486			54/74LS86			54/74S86			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁵	V
			Com'l		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA
		V _I = 7.0V						0.2				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40							μA
		V _I = 2.7V						40			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.8				mA
		V _I = 0.5V									-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-15		-100	-40		-100	mA
		Com'l	-18		-55	-15		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		30	43		6.1	10		50	75	mA
		Com'l		30	50		6.1	10		50	75	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with inputs grounded and outputs open.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay A or B to output	Other input LOW Waveform 2		23		23		10.5	ns
t _{PHL} Propagation delay A or B to output			17		17		10	
t _{PLH} Propagation delay A or B to output	Other input HIGH Waveform 1		30		30		10.5	ns
t _{PHL} Propagation delay A or B to output			22		22		10	

COUNTERS

54/7490, LS90

Decade Counter

DESCRIPTION

The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($\overline{MR}_1, \overline{MR}_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($\overline{MS}_1, \overline{MS}_2$) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the \overline{CP}_1 input must be externally connected to the Q_0 output. The \overline{CP}_0 input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-two counter the Q_3 output must be connected externally to the \overline{CP}_0 input. The input count is then applied to the CP₁ input and a divide-by-ten square wave is obtained at

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7490	30MHz	30mA
74LS90	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$ N7490N • N74LS90N	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP		
Ceramic DIP	S54LS90F	
Flatpack	S54LS90W	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
\overline{CP}_0	Input	2uI	6LSuI
\overline{CP}_1	Input	4uI	8LSuI
MR, MS	Inputs	1uI	1LSuI
Q_0-Q_3	Outputs	10uI	10LSuI

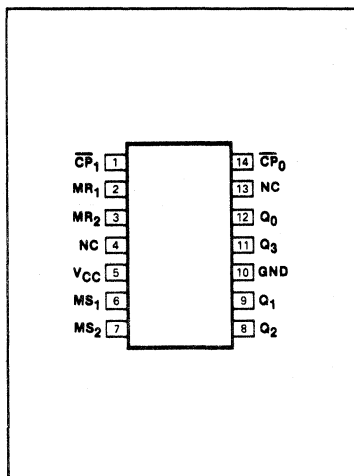
NOTE

Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL} .

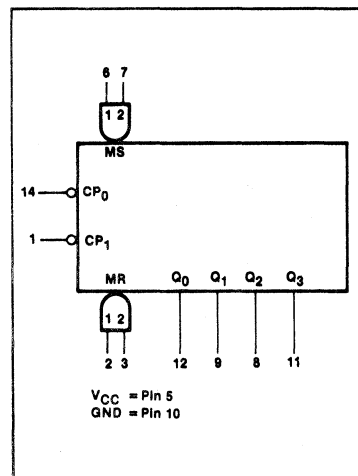
output Q_0 . To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the

divide-by-two function (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain a divide-by-five operation at the Q_3 output.

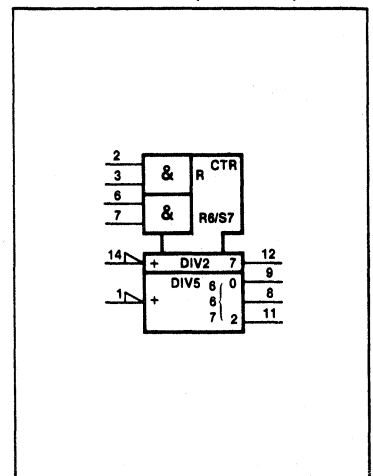
PIN CONFIGURATION



LOGIC SYMBOL



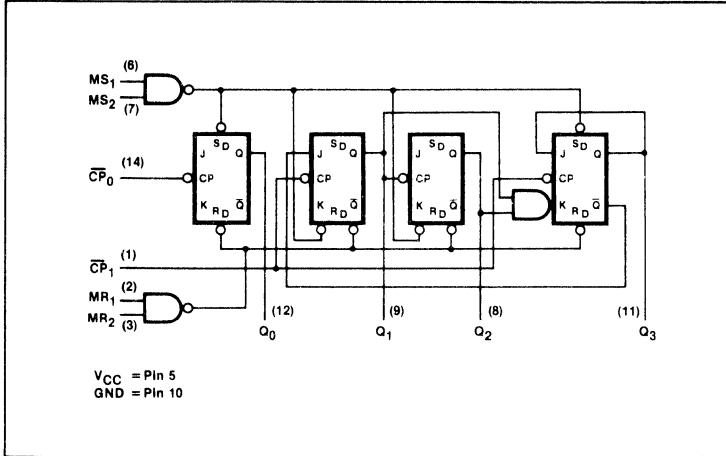
LOGIC SYMBOL (IEEE/IEC)



COUNTERS

54/7490, LS90

LOGIC DIAGRAM



MODE SELECTION— FUNCTION TABLE

RESET/SET INPUTS				OUTPUTS			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X				Count
X	L	X	L				Count
L	X	X	L				Count
H	L	L	X				Count

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

BCD COUNT SEQUENCE— FUNCTION TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	L	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE
 Output Q₀ connected to input \overline{CP}_1 .

4

ABSOLUTE MAXIMUM RATINGS

(Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

NOTE
 V_{IN} is limited to +5.5V on \overline{CP}_0 and \overline{CP}_1 inputs on the 54/74LS90 only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current				-800			-400	μA
I _{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

COUNTERS

54/7490, LS90

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	54/7490			54/74LS90			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V	All inputs '90			1.0			mA	
		V _I = 7.0V	MR, MS inputs					0.1	mA	
		V _I = 5.5V	\overline{CP}_0 input						0.2	mA
			\overline{CP}_1 input						0.4	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	MR, MS inputs			40			μ A	
			\overline{CP}_0 input			80			μ A	
			\overline{CP}_1 input			160			μ A	
		V _I = 2.7V	MR, MS inputs						20	μ A
			\overline{CP}_0 input ⁵						40	μ A
			\overline{CP}_1 input ⁵						80	μ A
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	MR, MS inputs			-1.6			-0.4	mA
			\overline{CP}_0 input			-3.2			-2.4	mA
			\overline{CP}_1 input			-6.4			-3.2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil		-20		-55	-20		-100	mA
		Com'l		-18		-55	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		30	46		9	15	mA	
		Com'l		30	53		9	15	mA	

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
- The maximum limit for the 54LS90 only is 80 μ A for \overline{CP}_0 and 160 μ A for \overline{CP}_1 inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} Input count frequency, \overline{CP}_0 to Q ₀	Waveform 1	10		32		MHz
f _{MAX} Input count frequency, \overline{CP}_1 to Q ₁		10		16		
t _{PLH} Propagation delay	Waveform 1			16		ns
t _{PHL} \overline{CP}_0 input to Q ₀ output				18		
t _{PLH} Propagation delay	Waveform 1			16		ns
t _{PHL} \overline{CP}_1 input to Q ₁ output				21		
t _{PLH} Propagation delay	Waveform 1			32		ns
t _{PHL} \overline{CP}_1 input to Q ₂ output				35		
t _{PLH} Propagation delay	Waveform 1			32		ns
t _{PHL} \overline{CP}_1 input to Q ₃ output				35		
t _{PLH} Propagation delay	Waveform 1		100	48		ns
t _{PHL} \overline{CP}_0 input to Q ₃ output			100	50		
t _{PHL} MR input to any output	Waveform 2			40		ns
t _{PLH} MS input to Q ₀ and Q ₃ outputs	Waveform 3			30		ns
t _{PHL} MS input to Q ₁ and Q ₂ outputs	Waveform 2			40		ns

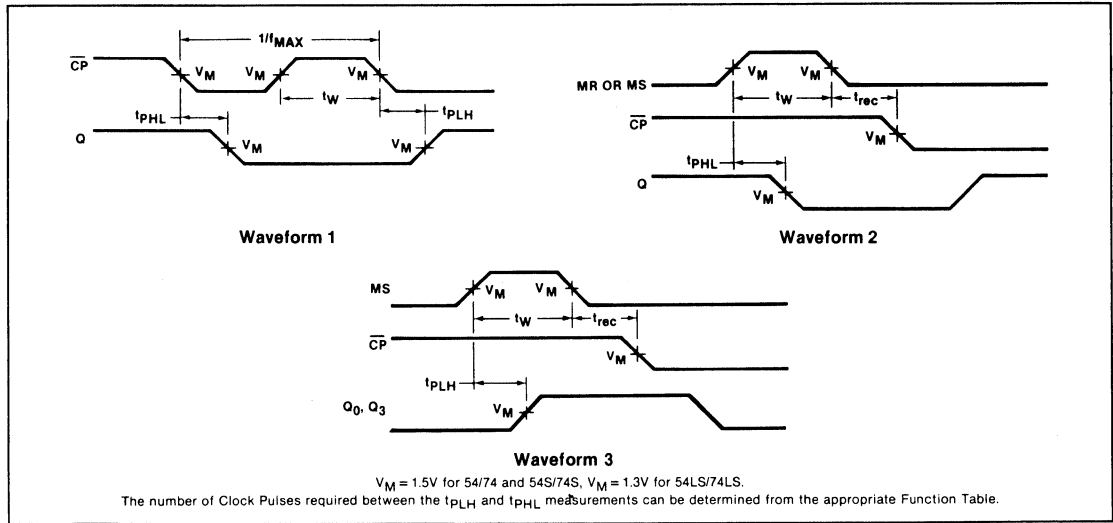
NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

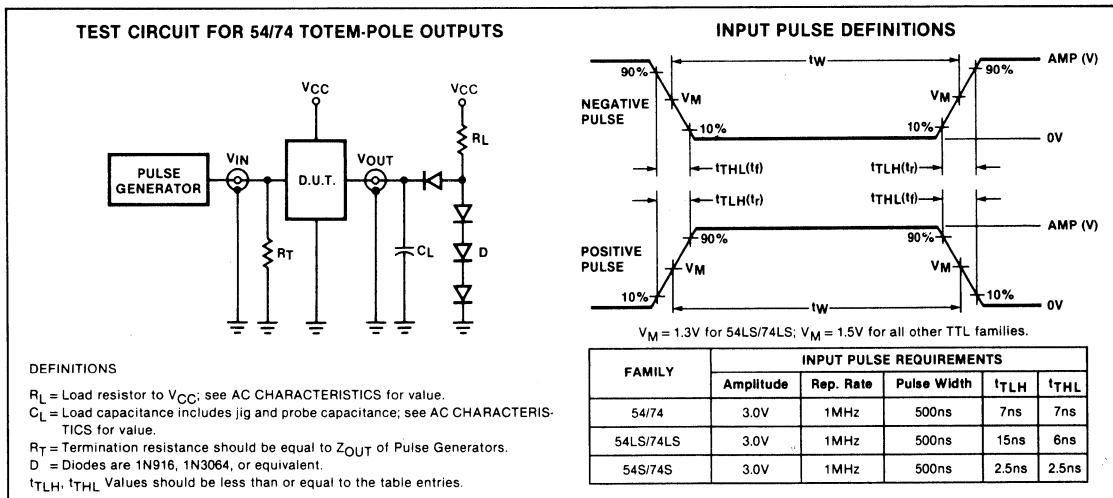
PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		Min	Max	Min	Max	
t_W \overline{CP}_0 pulse width	Waveform 1	50		15		ns
t_W \overline{CP}_1 pulse width	Waveform 1	50		30		ns
t_W MS, MR pulse width	Waveform 2	50		15		ns
t_{rec} Recovery time, MR to \overline{CP}	Waveform 2			25		ns
t_{rec} Recover time, MS to \overline{CP}	Waveforms 2 & 3			25		ns

AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS



REGISTER

54/7491A

8-Bit Shift Register

- 8-bit serial-in-serial-out shift register
- Common buffered clock
- 2-input gate for serial data entry
- True and Complement outputs

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7491A	18MHz	35mA

DESCRIPTION

The '91A is an 8-bit serial-in-serial-out shift register. The serial data is entered through a 2-input AND gate (D_{Sa} and D_{Sb}). HIGH data is entered when both D_{Sa} and D_{Sb} are HIGH. LOW data is entered when either Serial Data input is LOW. The Data inputs are edge-triggered and must be stable just one setup time prior to the LOW-to-HIGH transition of the Clock input (CP) for predictable operation. The data is shifted one bit to the right ($Q_0 - Q_2 \dots - Q_7$) synchronous with each LOW-to-HIGH clock transition. The '91A has no reset capacity, so initialization requires the shifting in of at least 8 bits of known data. Once the register is fully loaded, the Q output follows the Serial inputs delayed by eight clock pulses. The Complement (\bar{Q}) output from the last stage is also available for simpler decoding applications.

ORDERING CODE

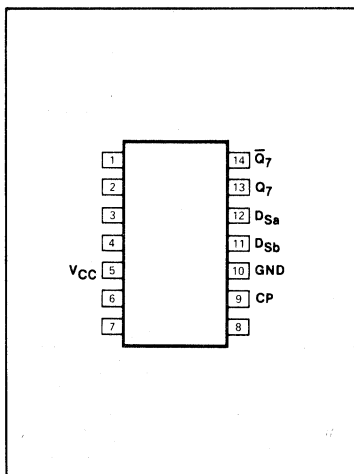
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7491AN	
Ceramic DIP		S5491AF
Flatpack		S5491AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

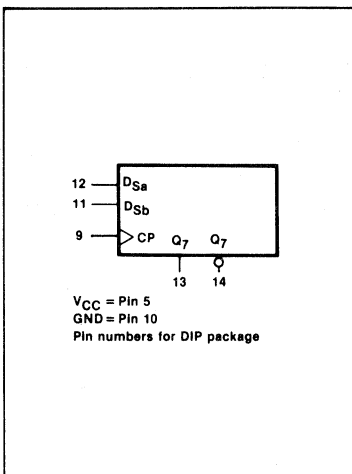
PINS	DESCRIPTION	54/74
All	Inputs	1ul
All	Outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

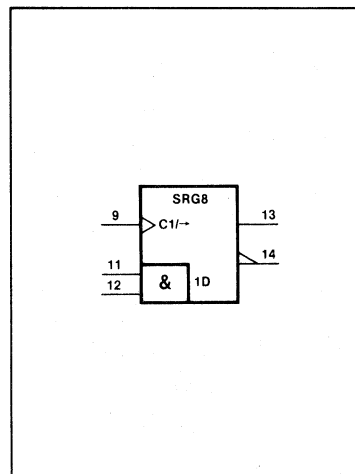
PIN CONFIGURATION



LOGIC SYMBOL



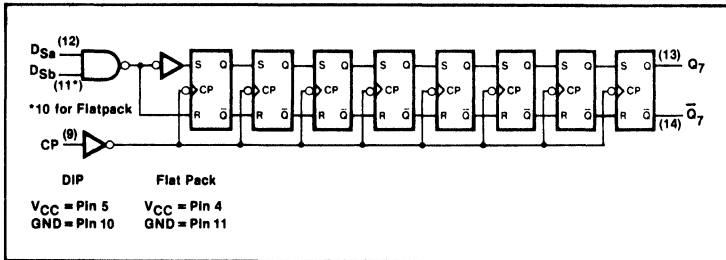
LOGIC SYMBOL (IEEE/IEC)



REGISTER

54/7491A

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			FIRST STAGE		OUTPUTS	
	CP	D _{sa}	D _{sb}	Q ₀	Q ₀ ⁻	Q ₇	Q ₇ ⁻
Shift, reset first stage	↑	l	X	L	H	Q ₆	Q ₆ ⁻
	↑	X	l	L	H	Q ₆	Q ₆ ⁻
Shift, set first stage	↑	h	h	H	L	Q ₆	Q ₆ ⁻

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 q_n = Lower case letters indicate the state of the referenced register output one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH Clock transition.

4

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I _{IN} Input current	- 30 to + 5	- 30 to + 5	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT
		Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+ 0.8	V
	Com'l			+ 0.8	V
I _{IK} Input clamp current				- 12	mA
I _{OH} HIGH-level output current				- 400	μA
I _{OL} LOW-level output current	Mil			16	mA
	Com'l			16	mA
T _A Operating free-air temperature	Mil	- 55		+ 125	°C
	Com'l	0		70	°C

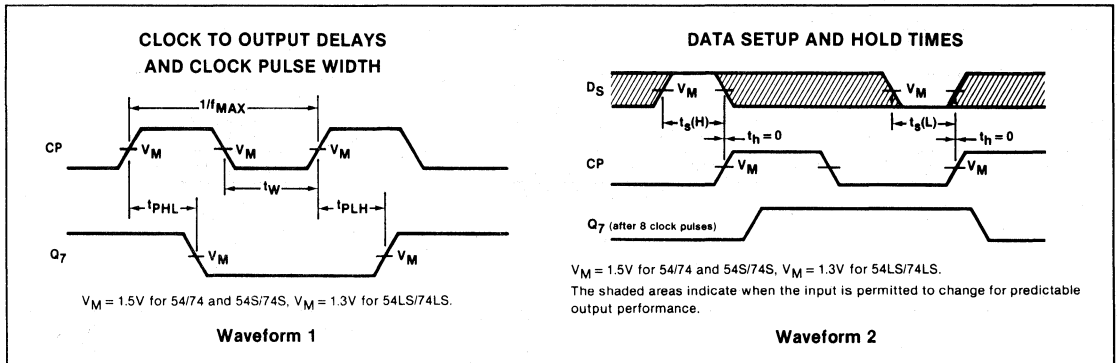
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7491A			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4	V	
		Com'l	2.4	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20	-57	mA	
		Com'l	-18	-57	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		35	50	mA
		Com'l		35	58	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- All typical values are at V_{CC} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured after the eighth clock pulse with the output open and D_{Sa} and D_{Sb} inputs grounded.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	10		MHz
t _{PLH} Propagation delay	Waveform 1		40	ns
t _{PHL} Clock to output			40	

NOTE

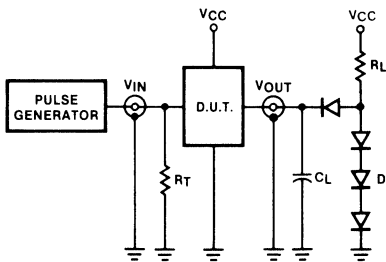
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		Min	Max	
t_w Clock pulse width	Waveform 1	25		ns
t_s Setup time, Data to clock	Waveform 2	25		ns
t_h Hold time, Data to clock	Waveform 2	0		ns

TEST CIRCUITS AND WAVEFORMS

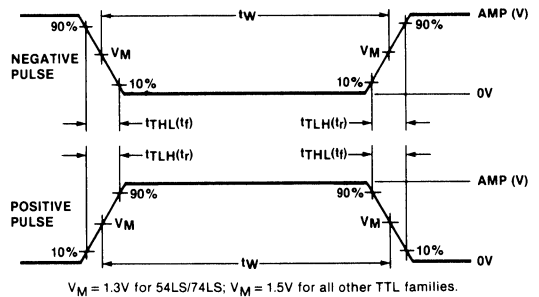
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

4

COUNTERS

54/7492, LS92

Divide-By-Twelve Counter

DESCRIPTION

The '92 is a 4-bit, ripple-type Divide-by-12 Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-six section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR₁+MR₂) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a Modulo-12, Divide-by-12 Counter the \overline{CP}_1 input must be externally connected to the Q₀ output. The \overline{CP}_0 input receives the incoming count and Q₃ produces a symmetrical divide-by-12 square wave output. In a divide-by-six counter no external connections are required. The first flip-flop is used as a binary element for the divide-by-two function. The \overline{CP}_1 input is used to obtain divide-by-three operation at the Q₁ and Q₂ outputs and divide-by-six operation at the Q₃ output.

TYPE	TYPICAL f _{MAX}	TYPICAL SUPPLY CURRENT
7492	28MHz	28mA
74LS92	42MHz	9mA

ORDERING CODE

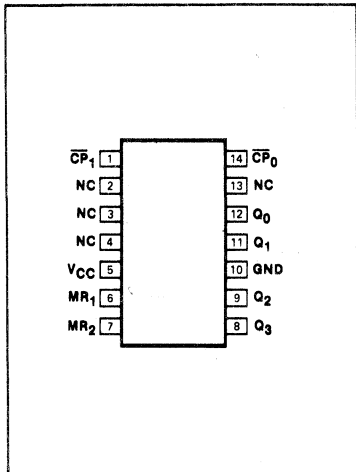
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = - 55°C to + 125°C
Plastic DIP	N7492N • N74LS92N	
Ceramic DIP		S54LS92F
Flatpack		S54LS92W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

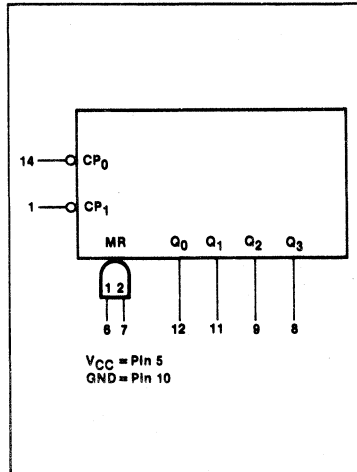
PINS	DESCRIPTION	54/74	54/74LS
MR	Master Reset inputs	1uI	1LSuI
CP ₀	Input	2uI	6LSuI
CP ₁	Input	4uI	8LSuI
Q ₀ -Q ₃	Outputs	10uI	10LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and - 1.6mA I_{IL}, and a 54/74LS unit load (LSuI) is 20µA I_{IH} and - 0.4mA I_{IL}.

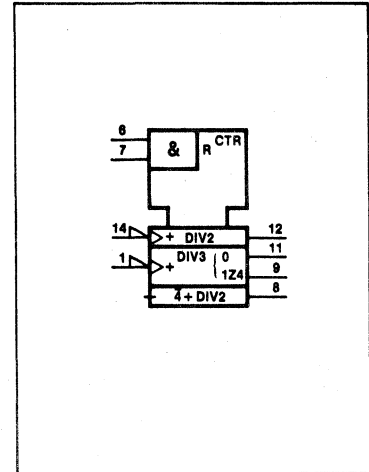
PIN CONFIGURATION



LOGIC SYMBOL



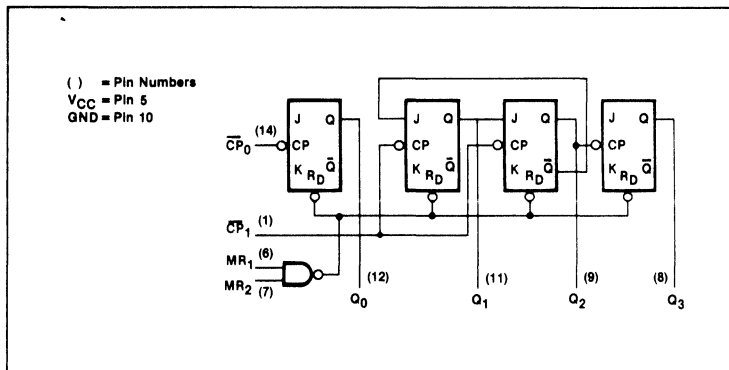
LOGIC SYMBOL (IEEE/IEC)



COUNTERS

54/7492, LS92

LOGIC DIAGRAM



FUNCTION TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE
 Output Q₀ connected to input \overline{CP}_1 .

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

NOTE
 V_{IN} is limited to +5.5V on \overline{CP}_0 and \overline{CP}_1 inputs on the 54/74LS92 only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current				-800			-400	μA
I _{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

4

COUNTERS

54/7492, LS92

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	54/7492			54/74LS92			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V	All inputs '92					1.0	mA	
		V _I = 7.0V	MR inputs					0.1	mA	
		V _I = 5.5V	\overline{CP}_0 input						0.2	mA
\overline{CP}_1 input							0.4	mA		
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	MR inputs			40			μ A	
			\overline{CP}_0 input			80			μ A	
			\overline{CP}_1 input			160			μ A	
		V _I = 2.7V	MR inputs					20	μ A	
			\overline{CP}_0 input ⁵					40	μ A	
\overline{CP}_1 input ⁵						80	μ A			
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	MR inputs			-1.6			-0.4	mA
			\overline{CP}_0 input			-3.2			-2.4	mA
			\overline{CP}_1 input			-6.4			-3.2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20	-55	-20			-100	mA	
		Com'l	-18	-55	-20			-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		44		9	15	mA		
		Com'l		51		9	15	mA		

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
- The maximum limit for the 54LS92 only is 80 μ A for \overline{CP}_0 and 160 μ A for \overline{CP}_1 inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

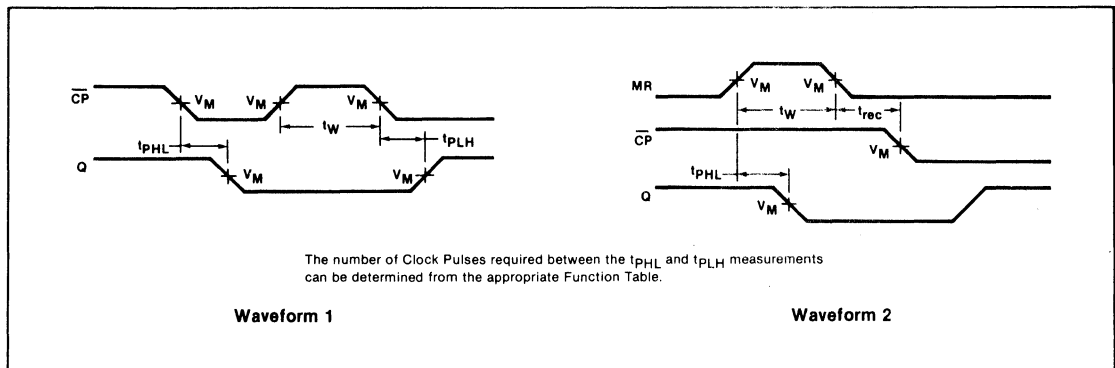
PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} \overline{CP}_0 input count frequency	Waveform 1	10		32		MHz
f _{MAX} \overline{CP}_1 input count frequency	Waveform 1	10		16		
t _{PLH} Propagation delay	Waveform 1				16	ns
t _{PHL} \overline{CP}_0 input to Q ₀ output					18	
t _{PLH} Propagation delay	Waveform 1				16	ns
t _{PHL} \overline{CP}_1 input to Q ₁ output					21	
t _{PLH} Propagation delay	Waveform 1				16	ns
t _{PHL} \overline{CP}_1 input to Q ₂ output					21	
t _{PLH} Propagation delay	Waveform 1				32	ns
t _{PHL} \overline{CP}_1 input to Q ₃ output					35	
t _{PLH} Propagation delay	Waveform 1		100		48	ns
t _{PHL} \overline{CP}_0 input to Q ₃ output			100		50	
t _{PHL} MR input to any output	Waveform 2				40	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_p, t_r, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

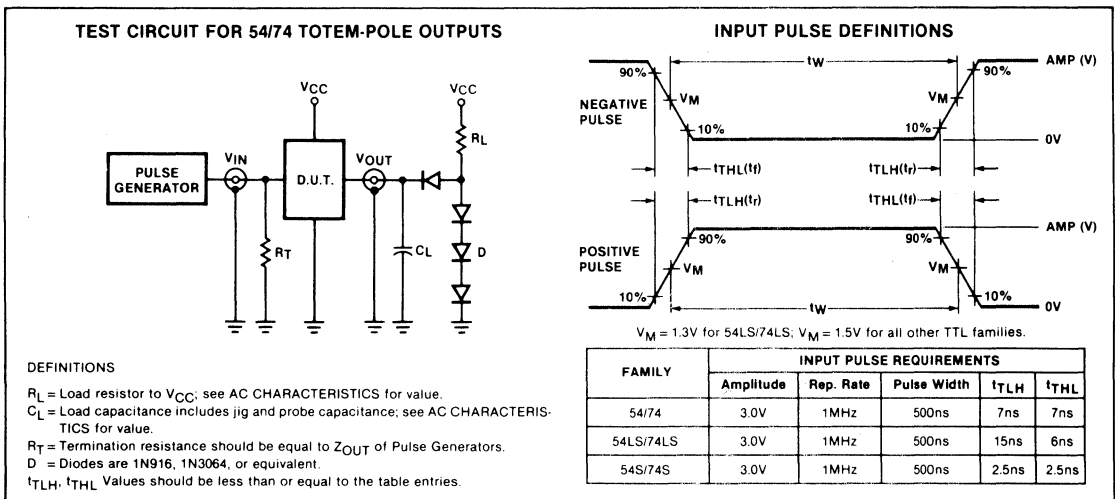
PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		Min	Max	Min	Max	
t_W \overline{CP}_0 pulse width	Waveform 1	50		15		ns
t_W \overline{CP}_1 pulse width	Waveform 1	50		30		ns
t_W MR pulse width	Waveform 2	50		15		ns
t_{rec} Recovery time, MR to \overline{CP}	Waveform 2			25		ns

AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS



4-Bit Binary Ripple Counter

DESCRIPTION

The '93 is a 4-bit, ripple-type Binary Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q_0 must be connected externally to input \overline{CP}_1 . The input count pulses are applied to input \overline{CP}_0 . Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the Function Table. As a 3-bit ripple counter the input count pulses are applied to input \overline{CP}_1 . Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7493	40MHz	28mA
74LS93	42MHz	9mA

ORDERING CODE

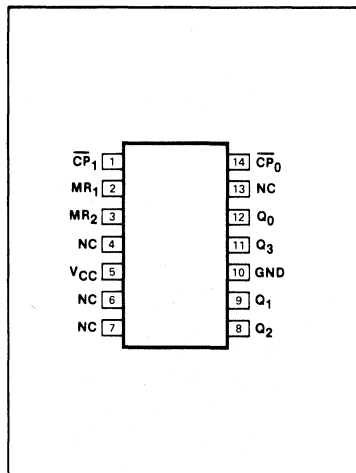
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N7493N • N74LS93N	
Plastic SO	N74LS93D	
Ceramic DIP		S5493F • S54LS93F
Flatpack		S5493W • S54LS93W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

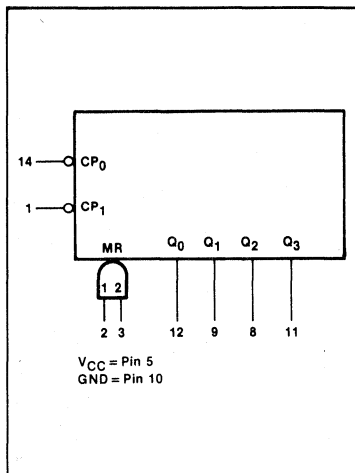
PINS	DESCRIPTION	54/74	54/74LS
MR	Master Reset inputs	1uI	1LSuI
\overline{CP}_0	Input	2uI	6LSuI
\overline{CP}_1	Input	2uI	4LSuI
Q_0-Q_3	Outputs	10uI	10LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

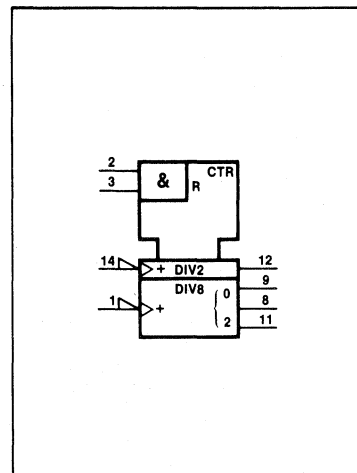
PIN CONFIGURATION



LOGIC SYMBOL



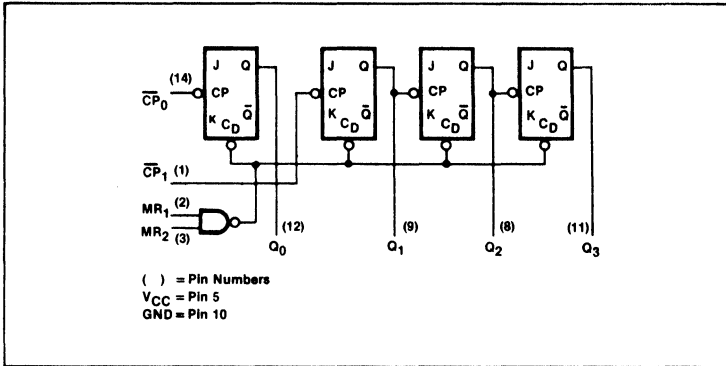
LOGIC SYMBOL (IEEE/IEC)



COUNTERS

54/7493, LS93

LOGIC DIAGRAM



FUNCTION TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE
Output Q₀ connected to input \overline{CP}_1 .

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H				Count
H	L				Count
L	L				Count

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

NOTE
V_{IN} is limited to 5.5V on \overline{CP}_0 and \overline{CP}_1 inputs only on the 54/74LS93.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current				-800			-400	μA
I _{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

COUNTERS

54/7493, LS93

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7493			54/74LS93			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4	0.25	0.4	V
			Com'l		0.2	0.4	0.35	0.5	V
		I _{OL} = 4mA	74LS				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V	All inputs '93			1.0		mA	
		V _I = 7.0V	MR inputs				0.1	mA	
		V _I = 5.5V	CP ₀ , CP ₁ inputs				0.2	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	MR inputs			40		μA	
			CP ₀ , CP ₁ inputs			80		μA	
		V _I = 2.7V	MR inputs				20	μA	
			CP ₀ , CP ₁ inputs ⁵				40	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	MR inputs			-1.6		-0.4	mA
			CP ₀ input			-3.2		-2.4	mA
			CP ₁ input			-3.2		-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	mA
		Com'l	-18		-55	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		28	46		9	15	mA
		Com'l		28	53		9	15	mA

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
- The maximum limit for the 54LS93 only is 80μA for CP₀ and CP₁ inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

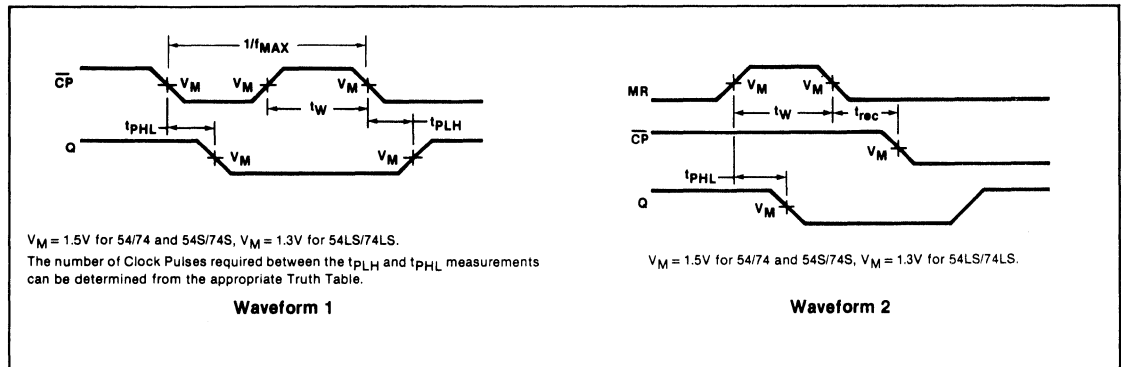
PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
f _{MAX} CP ₀ input count frequency	Waveform 1	10		32		MHz
f _{MAX} CP ₁ input count frequency		10		16		
t _{PLH} Propagation delay	Waveform 1				16	ns
t _{PHL} CP ₀ input to Q ₀ output					18	
t _{PLH} Propagation delay	Waveform 1				16	ns
t _{PHL} CP ₁ input to Q ₁ output					21	
t _{PLH} Propagation delay	Waveform 1				32	ns
t _{PHL} CP ₁ input to Q ₂ output					35	
t _{PLH} Propagation delay	Waveform 1				51	ns
t _{PHL} CP ₁ input to Q ₃ output					51	
t _{PLH} Propagation delay	Waveform 1		135		70	ns
t _{PHL} CP ₀ input to Q ₃ output			135		70	
t _{PHL} MR input to any output	Waveform 2				40	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

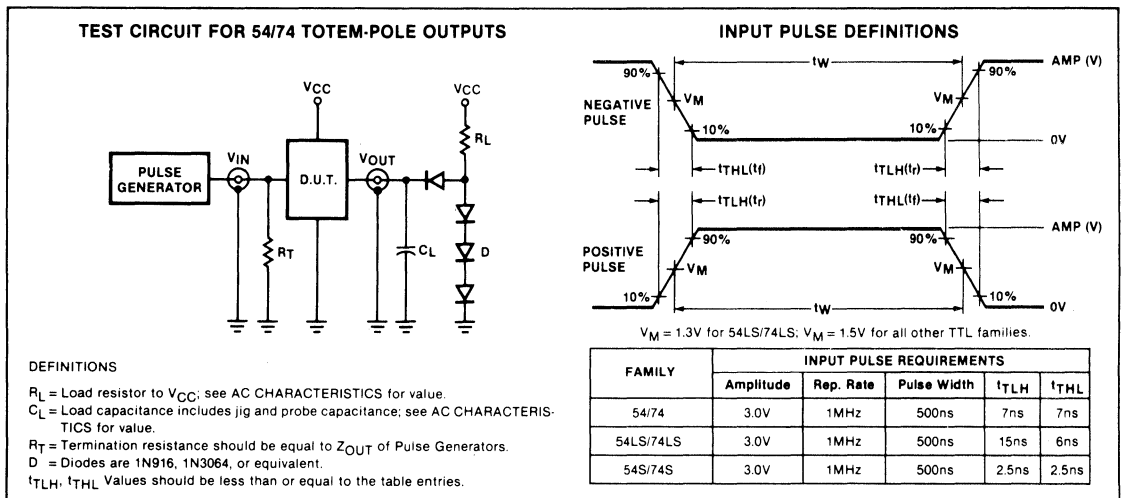
PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		Min	Max	Min	Max	
t_W \overline{CP}_0 pulse width	Waveform 1	50		15		ns
t_W \overline{CP}_1 pulse width	Waveform 1	50		30		ns
t_W MR pulse width	Waveform 2	50		15		ns
t_{rec} Recovery time, MR to \overline{CP}	Waveform 2			25		ns

AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS



SHIFT REGISTER

54/7494

4-Bit Shift Register

- 4-bit parallel-to-serial converter
- Two asynchronous ones transfer parallel data ports
- Buffered active HIGH Master Reset
- Buffered positive edge-triggered clock

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
7494	25ns	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7494N	

DESCRIPTION

The '94 is a 4-bit shift register with serial and parallel (ones transfer) data entry. To facilitate parallel ones transfer from two sources, two Parallel Load inputs (PL_0 and PL_1) with associated Parallel Data inputs (D_{0a} - D_{0d} and D_{1a} - D_{1d}) are provided. To accommodate these extra inputs only the output of the last stage is available. The asynchronous Master Reset (MR) is active HIGH. When MR is HIGH, it overrides the clock and clears the register, forcing Q_d LOW.

Four flip-flops are connected so that shifting is synchronous; they change state when the clock goes from LOW-to-HIGH. Data is accepted at the serial D_S input prior to this clock transition. Two Parallel Load inputs and Parallel Data inputs allow an asynchronous ones transfer from two

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

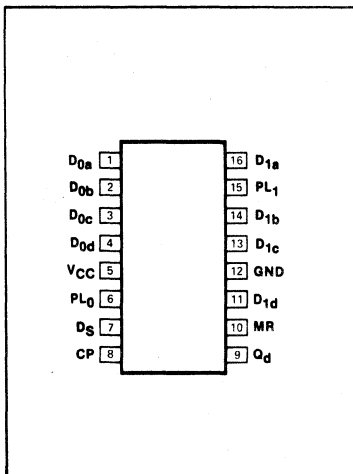
PINS	DESCRIPTION	54/74
PL_0, PL_1	Parallel Load inputs	4uI
D_S, D_n, CP, MR	All other inputs	1uI
Q_d	Serial Data output	10uI

NOTE
Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

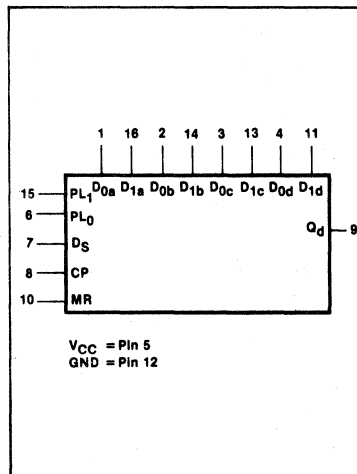
sources. The flip-flops can be set independently to the HIGH state when the appropriate Parallel input is activated. Parallel inputs D_{0a} through D_{0d} are activated during the time the PL_0 is HIGH and Parallel inputs D_{1a} through D_{1d} are activated when PL_1 is HIGH. If both sets of inputs are activated, a HIGH on either input will

set the flip-flops to a HIGH. The register should not be clocked while the Parallel Load inputs are activated. The Parallel Load and Parallel Data inputs will override the MR if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

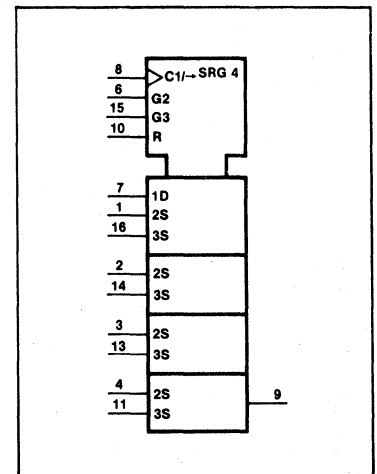
PIN CONFIGURATION



LOGIC SYMBOL



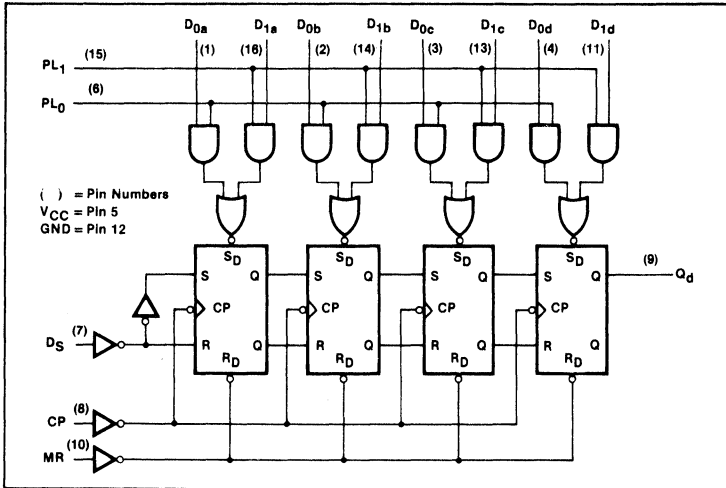
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER

54/7494

LOGIC DIAGRAM



4

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	PL ₀	PL ₁	D _{0n}	D _{1n}	MR	CP	D _s	Q _a	Q _b	Q _c	Q _d
Parallel load	H	L	L	X	X	X	X	Q _a	Q _b	Q _c	Q _d
	H	L	H	X	X	X	X	H	H	H	H
	L	H	X	L	X	X	X	Q _a	Q _b	Q _c	Q _d
	L	H	X	H	X	X	X	H	H	H	H
Reset (clear)	L	L	X	X	H	X	X	L	L	L	L
Shift right	L	L	X	X	L	↑	↓	L	Q _a	Q _b	Q _c
	L	L	X	X	L	↓	↑	H	Q _a	Q _b	Q _c

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 q_n = Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH Clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

SHIFT REGISTER

54/7494

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				- 12	mA
I_{OH}	HIGH-level output current				- 400	μ A
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	- 55		+ 125	$^{\circ}$ C
		Com'l	0		70	$^{\circ}$ C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/7494			UNIT	
		Min	Typ ²	Max		
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	Mil	2.4	3.4		V
		Com'l	2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = \text{MAX}$	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V_{IK}	$V_{CC} = \text{MIN}, I_I = I_{IK}$				- 1.5	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$				1.0	mA
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$	PL ₀ , PL ₁ inputs			160	μ A
		Other inputs			40	μ A
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	PL ₀ , PL ₁ inputs			- 6.4	mA
		Other inputs			- 1.6	mA
I_{OS}	$V_{CC} = \text{MAX}$	Mil	- 20		- 57	mA
		Com'l	- 18		- 57	mA
I_{CC}	$V_{CC} = \text{MAX}$	Mil		35	50	mA
		Com'l		35	58	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^{\circ}\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Parallel Load inputs grounded. Master Reset grounded following momentary application of 4.5V, all other inputs at 4.5V and outputs open.

AC CHARACTERISTICS $T_A = 25^{\circ}\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT		
		$C_L = 15\text{pF}, R_L = 400\Omega$				
		Min	Max			
f_{MAX}	Maximum clock frequency	Waveform 1		10	MHz	
t_{PLH}	Propagation delay	Waveform 1			40	ns
	Clock to output				40	ns
t_{PLH}	Propagation delay Parallel Load or Parallel Data to output	Waveform 2			35	ns
t_{PHL}	Propagation delay MR to output	Waveform 2			40	ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f pulse width or duty cycle.

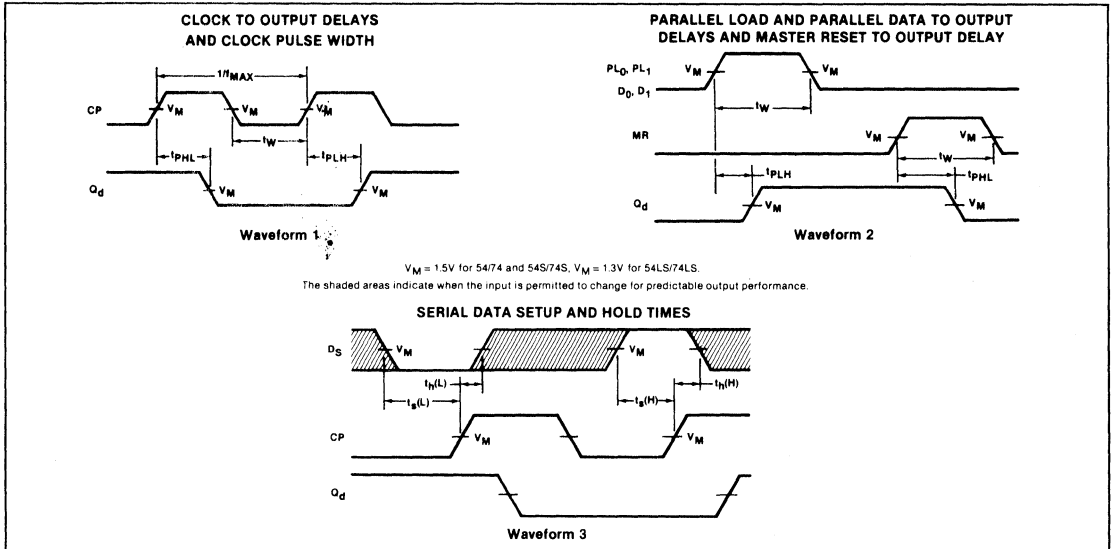
SHIFT REGISTER

54/7494

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

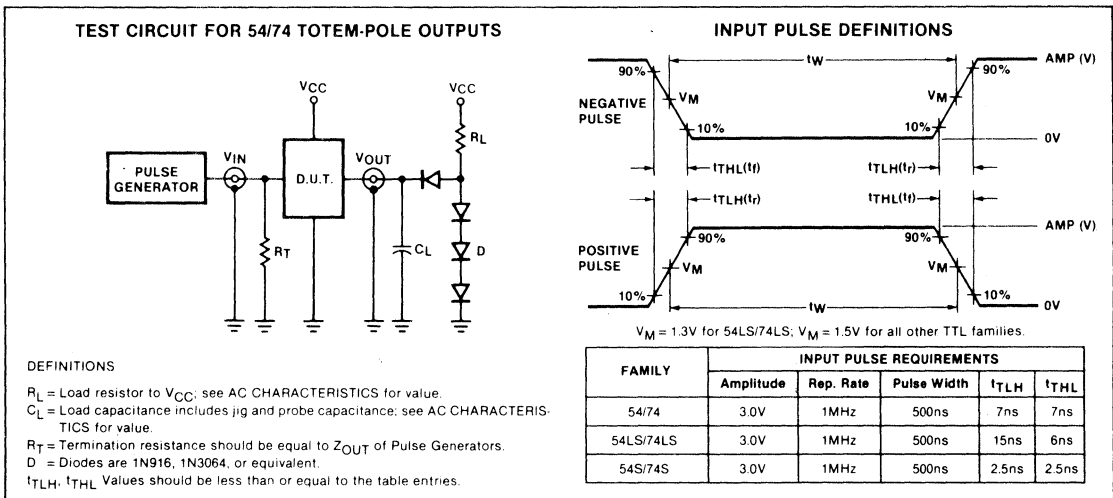
PARAMETER	TEST CONDITIONS	54/74		UNIT
		Min	Max	
$t_{W(L)}$ Clock pulse width, LOW	Waveform 1	35		ns
$t_{W(H)}$ MR pulse width, HIGH	Waveform 2	30		ns
$t_{W(H)}$ Parallel Load or Data pulse width, HIGH	Waveform 2	30		ns
$t_s(H)$ Setup time HIGH, D_S to CP	Waveform 3	35		ns
$t_s(L)$ Setup time LOW, D_S to CP	Waveform 3	25		ns
t_h Hold time HIGH or LOW, D_S to CP	Waveform 3	0		ns

AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS



SHIFT REGISTERS

54/7495, LS95B

4-Bit Shift Register

- Separate negative-edge-triggered shift and parallel load clocks
- Common mode control input
- Shift right serial input
- Synchronous shift or load capabilities

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7495	36MHz	39mA
74LS95B	36MHz	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7495N • N74LS95BN	
Ceramic DIP		S5495F • S54LS95BF
Flatpack		S5495W • S54LS95BW

DESCRIPTION

The '95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has serial Data (D_S) and four parallel Data (D_0 - D_3) inputs and four Parallel outputs (Q_0 - Q_3). The serial or parallel mode of operation is controlled by a Mode Select input (S) and two Clock inputs (\overline{CP}_1 and \overline{CP}_2). The serial (shift right) or parallel data transfers occur synchronously with the HIGH-to-LOW transition of the selected Clock input.

When the Mode Select input (S) is HIGH, \overline{CP}_2 is enabled. A HIGH-to-LOW transition on enabled \overline{CP}_2 loads parallel data from the D_0 - D_3 inputs into the register. When S is LOW, \overline{CP}_1 is enabled. A HIGH-to-LOW transition on enabled \overline{CP}_1 shifts the data from Serial input D_S to Q_0 and transfers the data in Q_0 to Q_1 , Q_1 to Q_2 , and Q_2 to Q_3 respectively (shift right). Shift left is accomplished by externally connecting Q_3 to

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
S	Input	2uI	1LSuI
Other	Inputs	1uI	1LSuI
Q	Output	10uI	10LSuI

NOTE

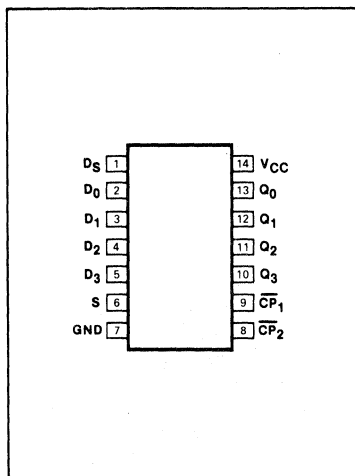
Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and - 1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and - 0.4mA I_{IL} .

D_2 , Q_2 to D_1 , Q_1 to D_0 , and operating the '95 in the parallel mode (S = HIGH).

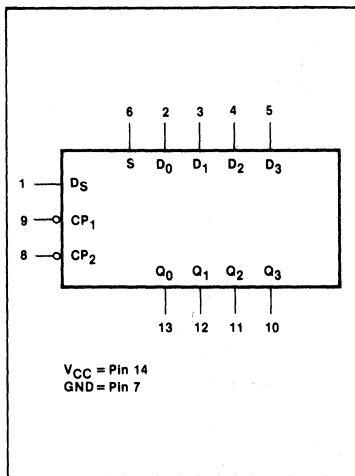
In normal operations the Mode Select (S) should change states only when both

Clock inputs are LOW. However, changing S from HIGH-to-LOW while \overline{CP}_2 is LOW, or changing S from LOW-to-HIGH while \overline{CP}_1 is LOW will not cause any changes on the register outputs.

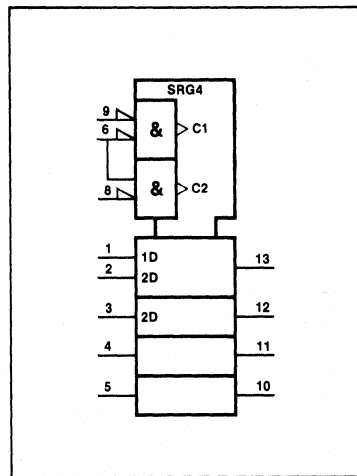
PIN CONFIGURATION



LOGIC SYMBOL



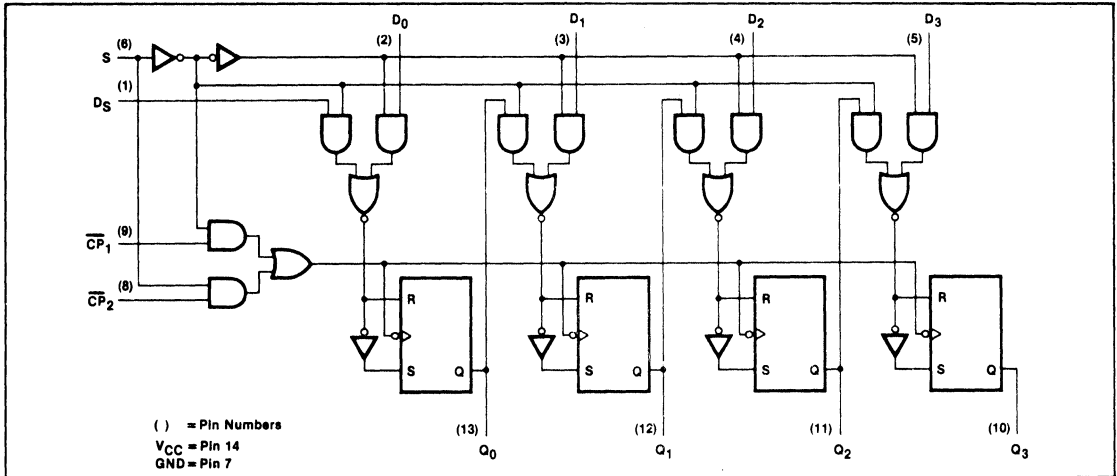
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTERS

54/7495, LS95B

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	+0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	CP ₁	CP ₂	D _S	D _N	Q ₀	Q ₁	Q ₂	Q ₃
Parallel load	H	X	↓	X	↓	L	L	L	L
	H	X	↓	X	h	H	H	H	H
Shift right	L	↓	X	↓	X	L	q ₀	q ₁	q ₂
	L	↓	X	h	X	H	q ₀	q ₁	q ₂
Mode change	↓	L	X	X	X	no change			
	↓	H	X	X	X	undetermined			
	↓	X	L	X	X	no change			
	↓	X	H	X	X	undetermined			

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition.
 L = LOW voltage level steady state.
 ↓ = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.
 q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition.
 X = Don't care.
 ↓ = HIGH-to-LOW transition of Clock or Mode Select.
 ↓ = LOW-to-HIGH transition of Mode Select.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74			54/74LS			UNIT	
	Min	Nom	Max	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			V	
V _{IL} LOW-level input voltage	Mil				+0.7			V
	Com'l				+0.8			V
I _{IK} Input clamp current				-12			mA	
I _{OH} HIGH-level output current				-800			μA	
I _{OL} LOW-level output current	Mil				4			mA
	Com'l				8			mA
T _A Operating free-air temperature	Mil	-55	+125		-55	+125		°C
	Com'l	0	70		0	70		°C

4

SHIFT REGISTERS

54/7495, LS95B

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	54/7495			54/74LS95B			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.25	0.4	V
		Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V					0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	S input		80			μA	
			Other inputs		40			μA	
		V _I = 2.7V	S input				20	μA	
			Other inputs				20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	S input		-3.2		-0.4	mA	
			Other inputs		-1.6		-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18		-57	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			39	63		13	21	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Serial Data input and all outputs open; Parallel Data inputs grounded; Mode Select input at 4.5V and a momentary 3V, then ground, applied to the Clock inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
f _{MAX} Maximum Clock frequency	Waveform 1	25		25		MHz
t _{PLH} Propagation delay	Waveform 1		27		27	ns
t _{PHL} Clock to output			32		32	

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SHIFT REGISTERS

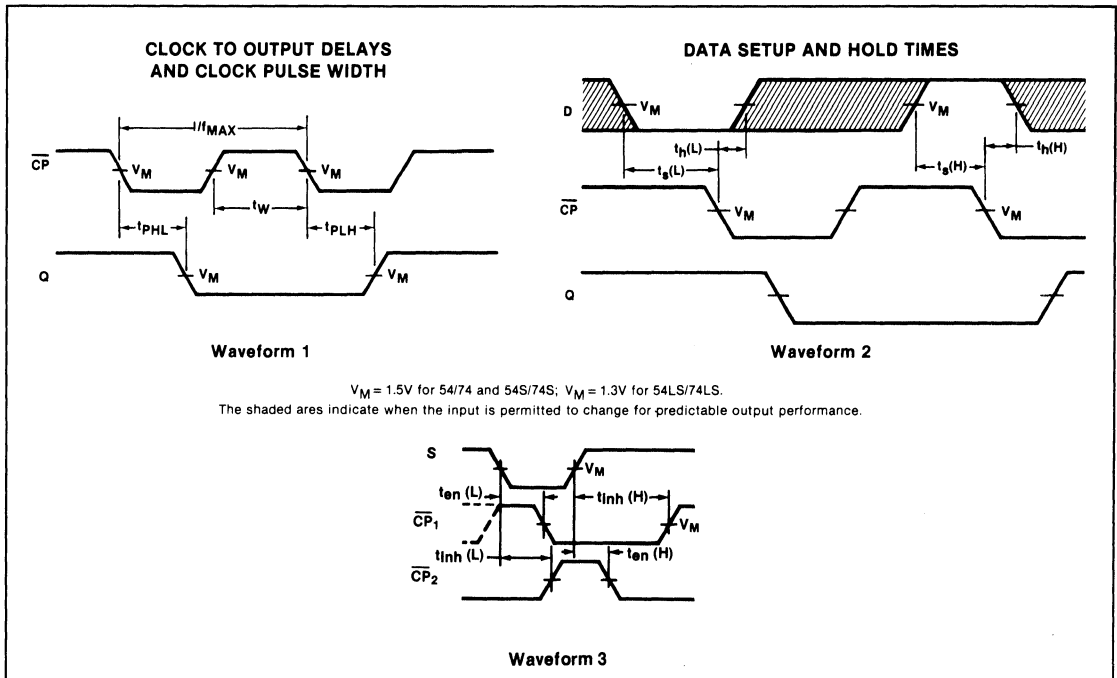
54/7495, LS95B

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$	Clock pulse width, HIGH	20		25		ns
t_s	Setup time, Data to Clock	15		20		ns
t_h	Hold time, Data to Clock	0		10		ns
$t_{en(L)}$	Enable time, LOW mode Select to \overline{CP}_1	30		20		ns
$t_{en(H)}$	Enable time, HIGH mode Select to \overline{CP}_2	30		20		ns
$t_{inh(H)}$	Inhibit time, HIGH mode Select to \overline{CP}_1 (L-H)	5		20		ns
$t_{inh(L)}$	Inhibit time, LOW mode Select to \overline{CP}_2 (L-H)	5		20		ns

AC WAVEFORMS

4

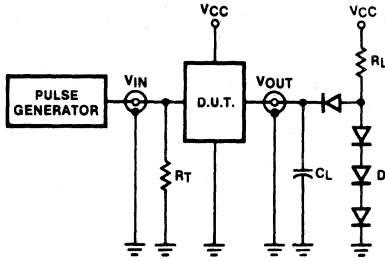


SHIFT REGISTERS

54/7495, LS95B

TEST CIRCUITS AND WAVEFORMS

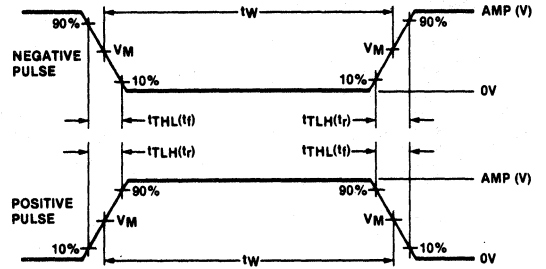
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTERS

54/7496, LS96

5-Bit Shift Register

- 5-bit parallel-to-serial or serial-to-parallel converter
- Asynchronous ones transfer preset entry
- Buffered positive-triggered clock
- Buffered active LOW Clear (Master Reset)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7496	25ns	48mA
74LS96	25ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N7496N • N74LS96N	
Ceramic DIP		S5496F • S54LS96F
Flatpack		S5496W • S54LS96W

DESCRIPTION

The '96 is a 5-bit shift register with both serial and parallel (ones transfer) data entry. Since the '96 has the output of each stage available as well as a D-type serial input and ones transfer inputs on each stage, it can be used in 5-bit serial-to-parallel, serial-to-serial and some parallel-to-serial data operations.

The '96 is five master/slave flip-flops connected to perform right shift. The flip-flops change state on the LOW-to-HIGH transition of the clock. The Serial (S) input is edge-triggered and must be stable only one setup time before the LOW-to-HIGH clock transition.

Each flip-flop has asynchronous set inputs, allowing them to be independently set HIGH. The set inputs are controlled by a common active HIGH Preset Enable (PE) input. The PE input is not buffered, and care must be taken not to overload the driving element. When the PE is HIGH, a

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
Preset Enable	Inputs	5uI	5LSuI
All other	Inputs	1uI	1LSuI
Q	Outputs	10uI	10LSuI

NOTE

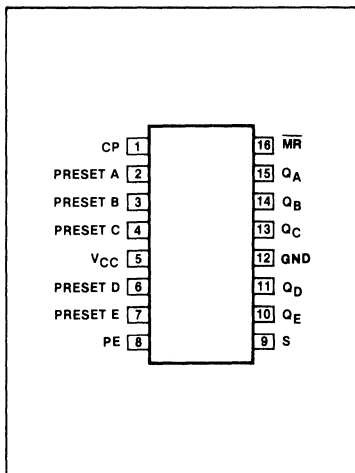
A 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL} .

HIGH on the Preset (A-E) inputs will set the associated flip-flops HIGH. A LOW on the A-E inputs will cause "no change" in the appropriate flip-flops.

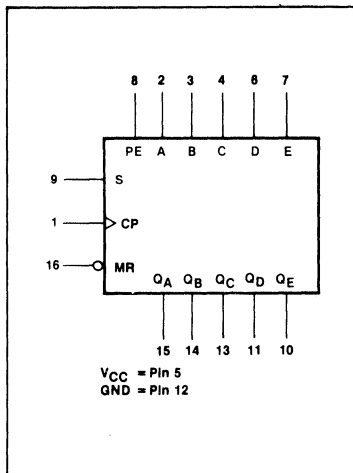
The asynchronous active LOW Clear (\overline{MR}) is buffered. When LOW, the MR overrides the

clock and clears the register if the PE is not active. The Preset inputs override the \overline{MR} , forcing the flip-flops HIGH if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

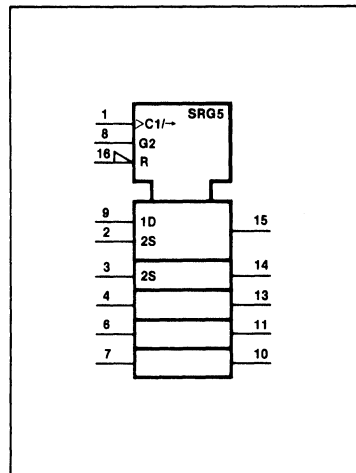
PIN CONFIGURATION



LOGIC SYMBOL



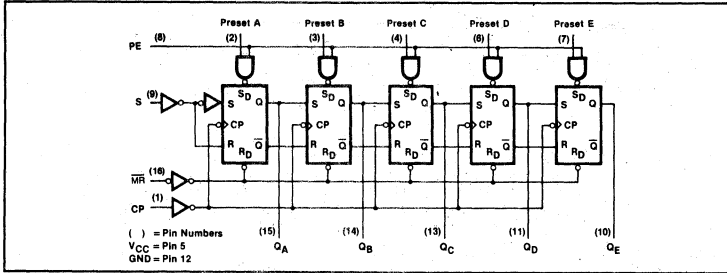
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTERS

54/7496, LS96

LOGIC DIAGRAM



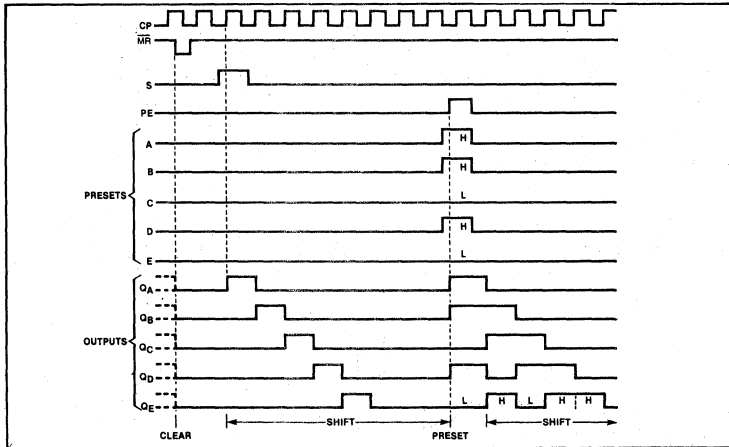
FUNCTION TABLE

MASTER RESET	PRESET ENABLE	PRESET					CLOCK	SERIAL	OUTPUTS				
		A	B	C	D	E			Q _A	Q _B	Q _C	Q _D	Q _E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}
H	H	H	L	H	L	H	L	X	H	Q _{B0}	H	Q _{D0}	H
H	L	X	X	X	X	X	L	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}
H	L	X	X	X	X	X	↑	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}
H	L	X	X	X	X	X	↓	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}

H = HIGH voltage level, (steady state)
 L = LOW voltage level (steady state)
 X = Irrelevant (any input, including transitions)
 ↑ = Transition from LOW-to-HIGH level

Q_{A0}, Q_{B0}, etc = The level of Q_A, Q_B, ect, respectively before the indicated steady-state input conditions were established.
 Q_{An}, Q_{Bn}, etc = The level of Q_A, Q_B, etc, respectively before the most recent ↑ transition of the clock.

TYPICAL MASTER RESET, SHIFT, PRESET, AND SHIFT SEQUENCES



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

SHIFT REGISTERS

54/7496, LS96

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.8			+ 0.7	V
		Com'l			+ 0.8			+ 0.8	V
I _{IK}	Input clamp current				- 12			- 18	mA
I _{OH}	HIGH-level output current				- 400			- 400	μA
I _{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	- 55		+ 125	°C
		Com'l	0		70	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹	54/7496			54/74LS96			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4	V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.25	0.4	V
		I _{OL} = 4mA		0.2	0.4		0.35	0.5	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}				- 1.5			- 1.5	V
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V	PE inputs					0.5	mA
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V	PE inputs		200			μA	
			Other inputs		40			μA	
		V _I = 2.7V	PE inputs					100	μA
			Other inputs					20	μA
I _{IL}	LOW-level input current V _{CC} = MAX V _I = 0.4V	PE inputs			- 8			- 2	mA
		Other inputs			- 1.6			- 0.4	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	Mil	- 20		- 57	- 20		- 100	mA
		Com'l	- 18		- 57	- 20		- 100	mA
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX	Mil		48	68		12	20	mA
		Com'l		48	79		12	20	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at V_{CC} = 5V, T_A = 25°C.

3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

4. Measure I_{CC} with Clear grounded and all other inputs and outputs open.

SHIFT REGISTERS

54/7496, LS96

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	10		25		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		40		40	ns
t_{PLH} Propagation delay Preset or Preset Enable to output	Waveform 2		35		35	ns
t_{PHL} Propagation delay $\overline{\text{MR}}$ to output	Waveform 2		55		55	ns

NOTE

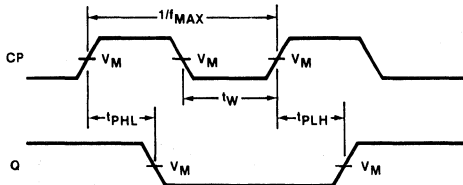
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		Min	Max	Min	Max	
$t_{\text{W(L)}}$ Clock pulse width, LOW	Waveform 1	35		20		ns
$t_{\text{W(L)}}$ $\overline{\text{MR}}$ pulse width, LOW	Waveform 2	30		30		ns
$t_{\text{W(H)}}$ Preset or Preset Enable pulse width, HIGH	Waveform 2	30		30		ns
t_s Setup time, S to CP	Waveform 3	30		30		ns
t_h Hold time, S to CP	Waveform 3	0		0		ns

AC WAVEFORMS

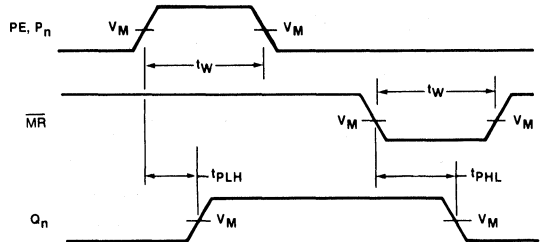
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



$V_M = 1.5\text{V}$ for 54/74 and 54S/74S, $V_M = 1.3\text{V}$ for 54LS/74LS.

Waveform 1

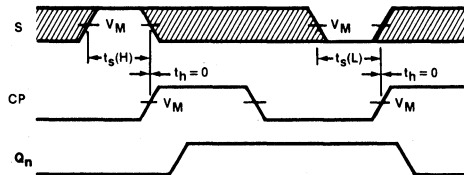
PARALLEL LOAD AND PARALLEL DATA TO OUTPUT DELAYS AND MASTER RESET TO OUTPUT DELAY



$V_M = 1.5\text{V}$ for 54/74 and 54S/74S, $V_M = 1.3\text{V}$ for 54LS/74LS.

Waveform 2

DATA SETUP AND HOLD TIME



$V_M = 1.5\text{V}$ for 54/74 and 54S/74S, $V_M = 1.3\text{V}$ for 54LS/74LS.
The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

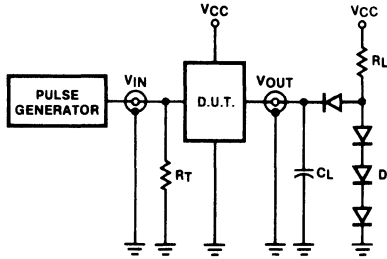
Waveform 3

SHIFT REGISTERS

54/7496, LS96

TEST CIRCUITS AND WAVEFORMS

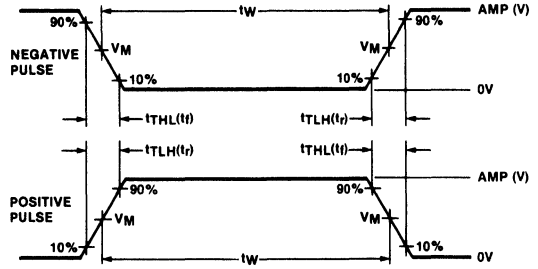
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOPS

54/74107, LS107

Dual J-K Flip-Flop

DESCRIPTION

The '107 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 74107 is a positive pulse-triggered flip-flop. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. For these devices the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS107 is a negative edge-triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset (\bar{R}_D) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the \bar{Q} output HIGH.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74107	20MHz	20mA
74LS107	45MHz	4mA

ORDERING CODE

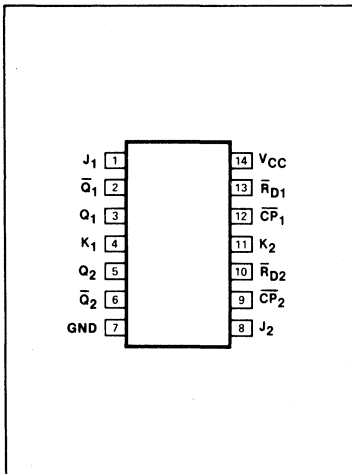
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74107N • N74LS107N	
Plastic SO	N74LS107D	
Ceramic DIP		S54LS107F
Flatpack		S54LS107W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

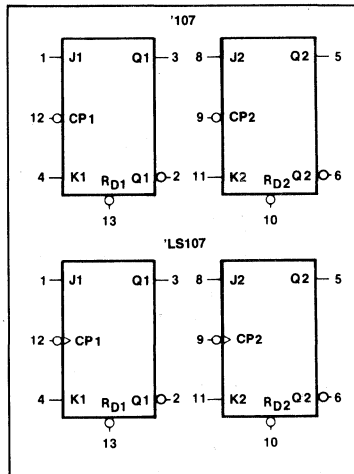
PINS	DESCRIPTION	54/74	54/74LS
$\bar{C}P$	Clock input	2uI	4LSuI
\bar{R}_D	Reset input	2uI	3LSuI
J, K	Data inputs	1uI	1LSuI
Q, \bar{Q}	Outputs	10uI	10LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and -0.4mA I_{IL} .

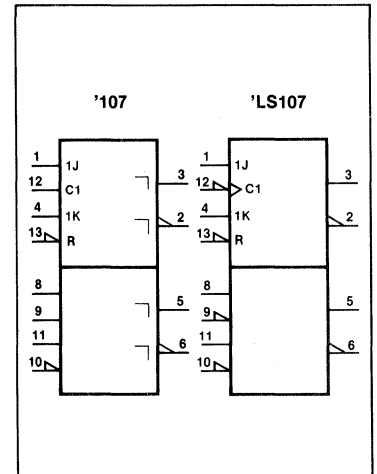
PIN CONFIGURATION



LOGIC SYMBOL



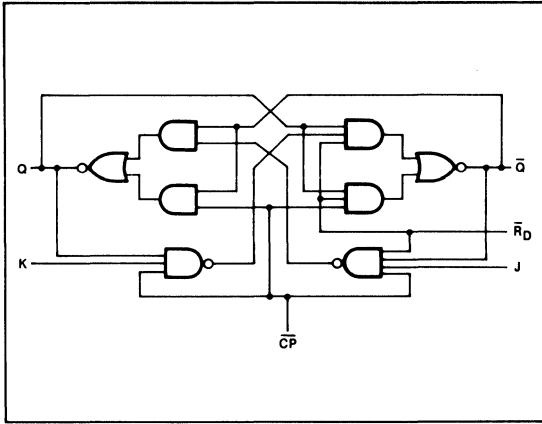
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/74107, LS107

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{R}_D	$\bar{C}\bar{P}^{(b)}$	J	K	Q	\bar{Q}
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	\lrcorner	h	h	\bar{q}	q
Load "0" (Reset)	H	\lrcorner	l	h	L	H
Load "1" (Set)	H	\lrcorner	h	l	H	L
Hold "no change"	H	\lrcorner	l	l	q	\bar{q}

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 \lrcorner = Positive Clock pulse.

NOTES

- a. The J and K inputs of the 54/74107 must be stable while the Clock is HIGH for conventional operation.
- b. The 54/74LS107 is edge-triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-12			-18	mA
I_{OH} HIGH-level output current				-400			-400	μ A
I_{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

FLIP-FLOPS

54/74107, LS107

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74107			54/74LS107			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}						-1.5	-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V				1.0			mA	
		V _I = 7.0V	J, K Inputs						0.1	mA
			\bar{R}_D Inputs						0.3	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	J, K Inputs				40			μ A
			\bar{R}_D Inputs				80			μ A
			$\bar{C}P$ Inputs				80			μ A
		V _I = 2.7V	J, K Inputs						20	μ A
			\bar{R}_D Inputs						60	μ A
			$\bar{C}P$ Inputs						80	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	J, K Inputs				-1.6		-0.4	mA	
		\bar{R}_D Inputs				-3.2		-0.8	mA	
		$\bar{C}P$ Inputs				-3.2		-0.8	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-57	-20		-100	mA	
		Com'l	-18		-57	-20		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX				40			8	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock Input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum Clock frequency	Waveform 3	15		30		MHz
t _{PLH} Propagation delay t _{PHL} Clock to Output	Waveform 1, 'LS107		25		20	ns
	Waveform 3, '107		40		30	
t _{PLH} Propagation delay t _{PHL} Reset to Output	Waveform 2		25		20	ns
			40		30	

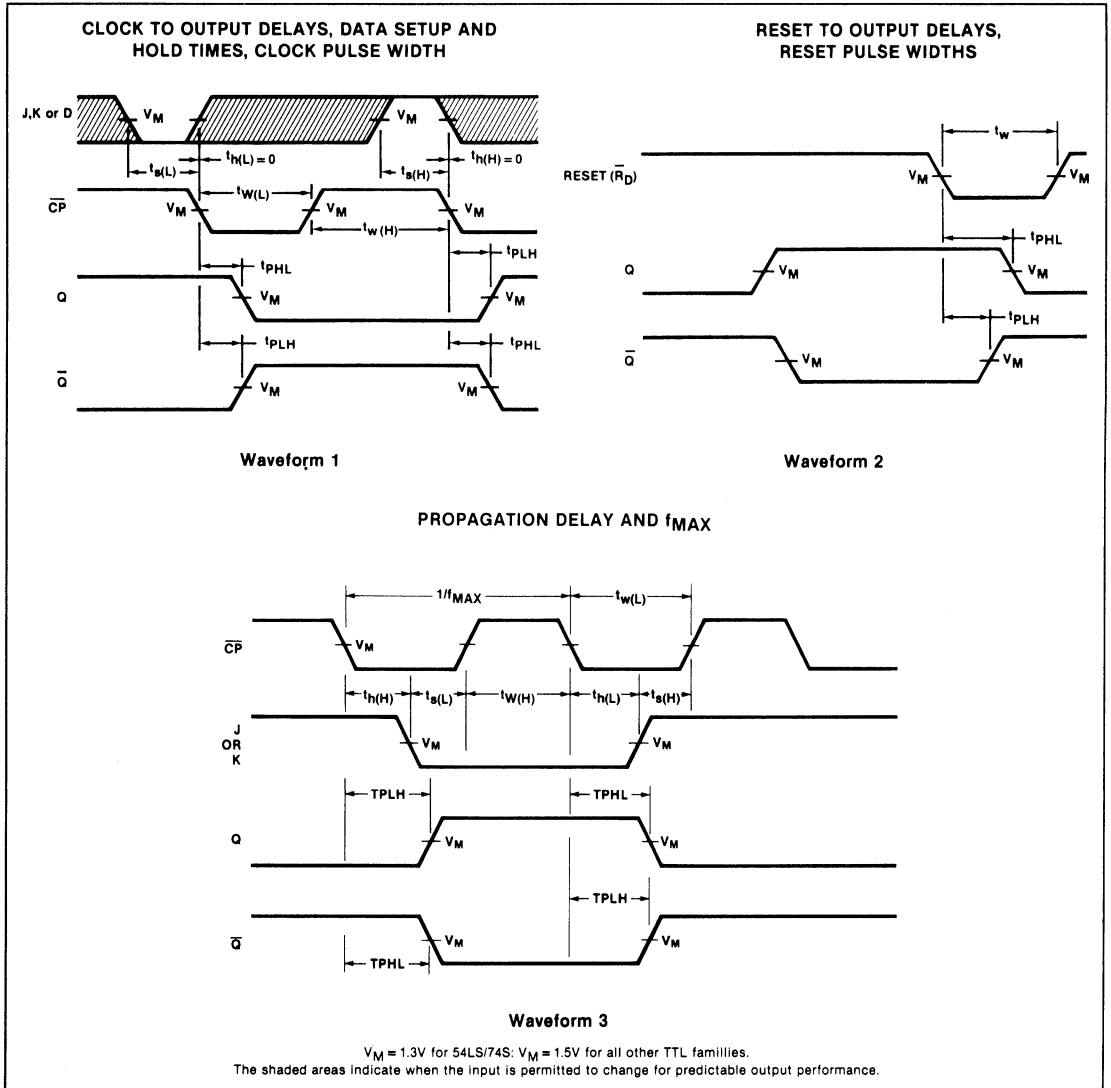
NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

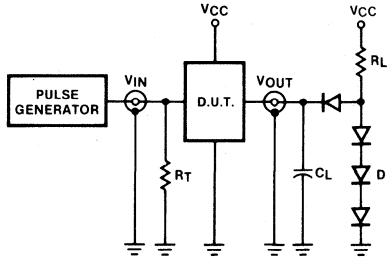
PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		Min	Max	Min	Max	
$t_{w(H)}$ Clock pulse width (HIGH)	Waveform 1	20		20		ns
$t_{w(L)}$ Clock pulse width (LOW)	Waveform 1	47		13		ns
$t_{w(L)}$ Reset pulse width (LOW)	Waveform 2	25		25		ns
t_s Setup time J or K to Clock ^(b)	Waveform 1	0		20		ns
t_h Hold time J or K to Clock	Waveform 1	0		0		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

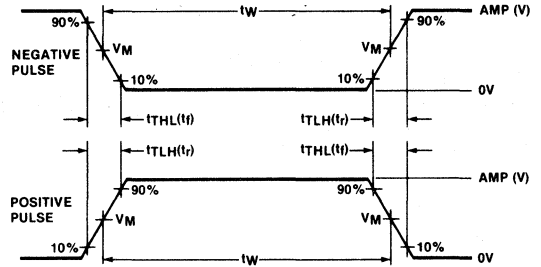
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOPS

54/74109, LS109A

Dual J-K̄ Positive Edge-Triggered Flip-Flop

DESCRIPTION

The '109 is a dual positive edge-triggered J-K̄-type flip-flop featuring individual J, K̄, Clock, Set and Reset inputs; also complementary Q and Q̄ outputs.

Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active LOW inputs and operate independently of the Clock input.

The J and K̄ are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select-Truth Table.

The J and K̄ inputs must be stable just one setup time prior to the LOW-to-HIGH transition of the Clock for predictable operation. The J-K̄ design allows operation as a D flip-flop by tying the J and K̄ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74109	33MHz	9mA
74LS109A	33MHz	4mA

ORDERING CODE

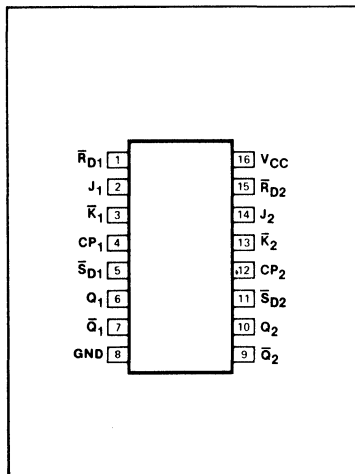
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74109N • N74LS109AN	
Plastic SO	N74LS109D	
Ceramic DIP		S54109F • S54LS109AF
Flatpack		S54109W • S54LS109AW
LLCC		S54LS109G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

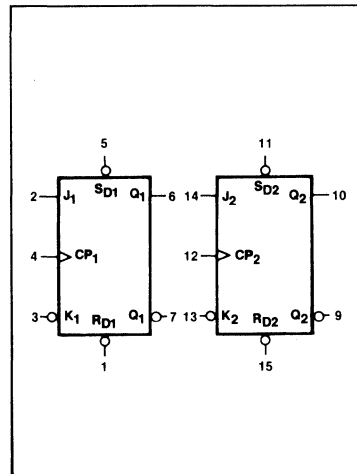
PINS	DESCRIPTION	54/74	54/74LS
CP	Clock input	2ul	1LSul
\bar{R}_D	Reset input	4ul	2LSul
\bar{S}_D	Set input	2ul	2LSul
J, K̄	Data inputs	1ul	1LSul
Q, Q̄	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

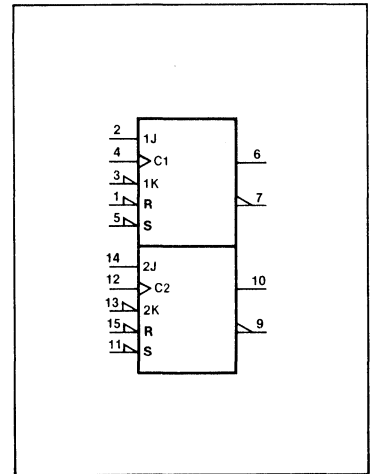
PIN CONFIGURATION



LOGIC SYMBOL



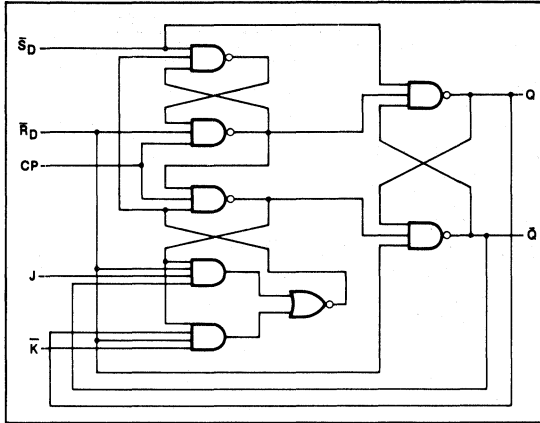
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/74109, LS109A

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	\bar{S}_D	\bar{R}_D	CP	J	\bar{K}	Q	\bar{Q}
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note)	L	L	X	X	X	H	H
Toggle	H	H	1	h	l	\bar{q}	q
Load "0" (Reset)	H	H	1	l	l	L	H
Load "1" (Set)	H	H	1	h	h	H	L
Hold "no change"	H	H	1	l	h	q	\bar{q}

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH Clock transition.
 1 = LOW-to-HIGH Clock transition.

NOTE
 Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-12			-18	mA
I_{OH} HIGH-level output current				-800			-400	μ A
I_{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74109			54/74LS109			UNIT			
			Min	Typ ²	Max	Min	Typ ²	Max				
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		Mil	2.4	3.4		2.5	3.4	V			
			Com'l	2.4	3.4		2.7	3.4	V			
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX		I _{OL} = MAX		0.2	0.4		0.25	0.4	V		
			I _{OL} = 4mA	Mil				0.35	0.5	V		
				Com'l				0.35	0.5	V		
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}							-1.5	V			
I _I Input current at maximum input voltage	V _{CC} = MAX		V _I = 5.5V						1.0	mA		
			V _I = 7.0V		J, \bar{K} Inputs						0.1	mA
					\bar{R}_D, \bar{S}_D Inputs						0.2	mA
					CP Inputs						0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX		V _I = 2.4V		J, \bar{K} Inputs				40	μ A		
					\bar{R}_D Inputs				160	μ A		
					\bar{S}_D, CP Inputs				80	μ A		
			V _I = 2.7V		J, \bar{K} Inputs					20	μ A	
					\bar{R}_D, \bar{S}_D Inputs					40	μ A	
					CP Inputs					20	μ A	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V		J, \bar{K} Inputs				-1.6		-0.4	mA		
			\bar{R}_D Inputs				-4.8		-0.8	mA		
			\bar{S}_D Inputs				-3.2		-0.8	mA		
			CP Inputs				-3.2		-0.4	mA		
I _{OS} Short-circuit output current ³	V _{CC} = MAX			-30		-85	-20		-100	mA		
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX				9	30		4	8	mA		

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400 Ω		C _L = 15pF, R _L = 2k Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		25		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 1		16 28		25 40	ns
t _{PLH} Propagation delay t _{PHL} Reset to output	Waveform 2		15 25		25 40	ns
t _{PLH} Propagation delay t _{PHL} Set to output	Waveform 2		15 35		25 40	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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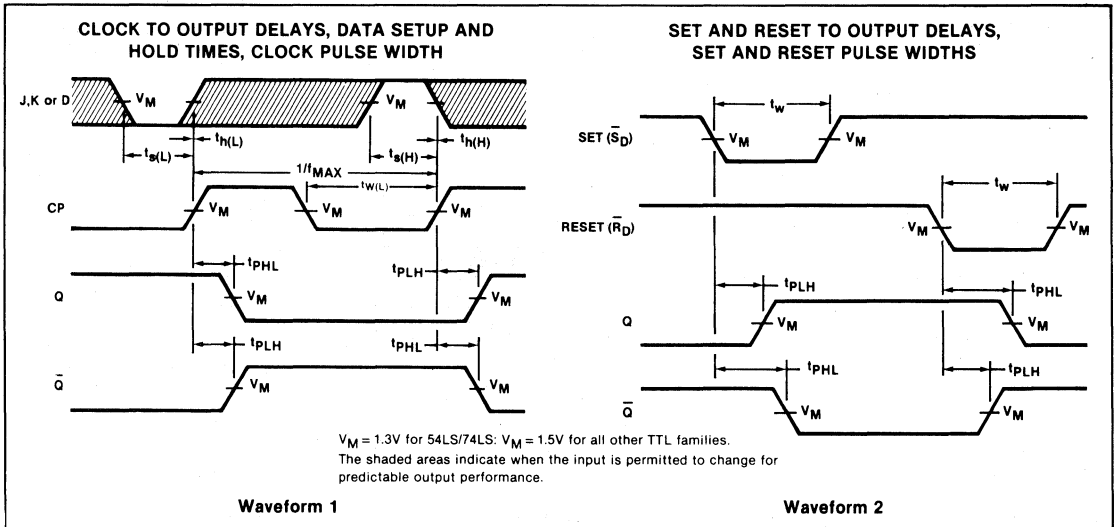
FLIP-FLOPS

54/74109, LS109A

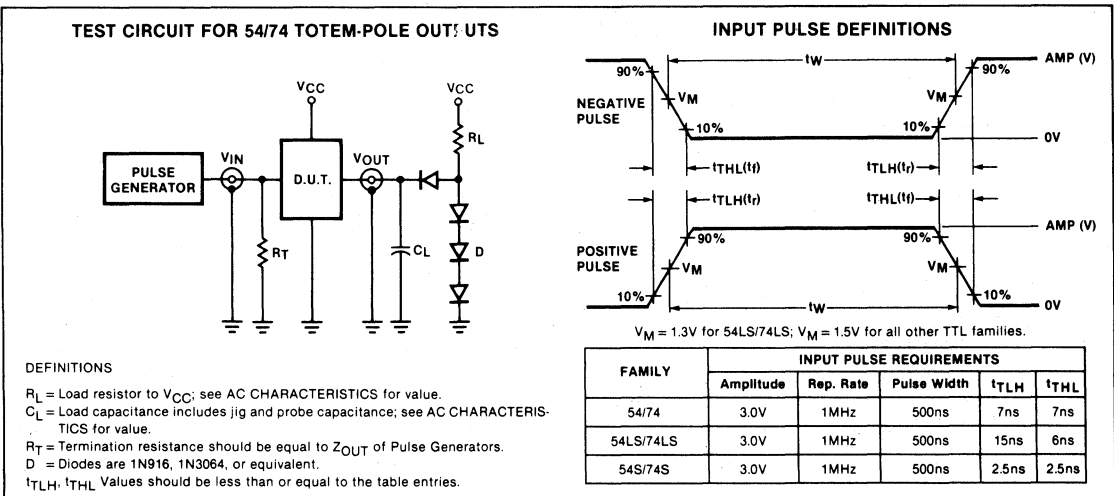
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$ Clock pulse width (HIGH)	Waveform 1	20		25		ns
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	20		15		ns
$t_{W(L)}$ Set or Reset pulse width (LOW)	Waveform 2	20		25		ns
t_s Setup time J or K to Clock	Waveform 1	10		20		ns
t_h Hold time J or K to Clock	Waveform 1	6.0		5.0		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



FLIP-FLOPS

54/74LS112, S112

Dual J-K Edge-Triggered Flip-Flop

DESCRIPTION

The '112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set (\bar{S}_D) and Reset (\bar{R}_D) inputs, when LOW, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\bar{C}\bar{P}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\bar{C}\bar{P}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\bar{C}\bar{P}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS112	45MHz	4mA
74S112	125MHz	15mA

ORDERING CODE

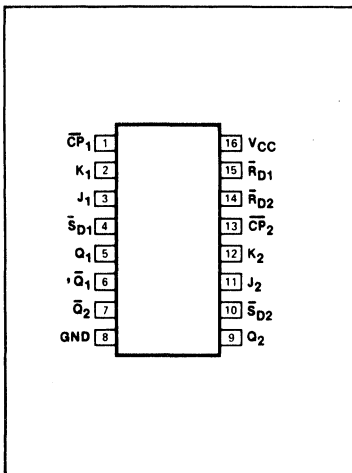
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S112N • N74LS112N	
Plastic SO	N74LS112D • N74S112D	
Ceramic DIP		S54S112F • S54LS112F
Flatpack		S54S112W • S54LS112W
LLCC		S54LS112G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

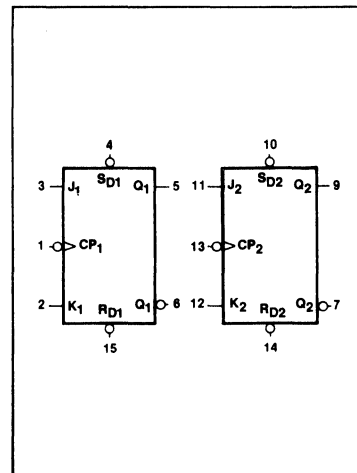
PINS	DESCRIPTION	54/74S	54/74LS
$\bar{C}\bar{P}$	Clock input	2Sul	4LSul
\bar{R}_D, \bar{S}_D	Reset and Set inputs	3.5Sul	3LSul
J, K	Data inputs	1Sul	1LSul
Q, \bar{Q}	Outputs	10Sul	10LSul

NOTE
A 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

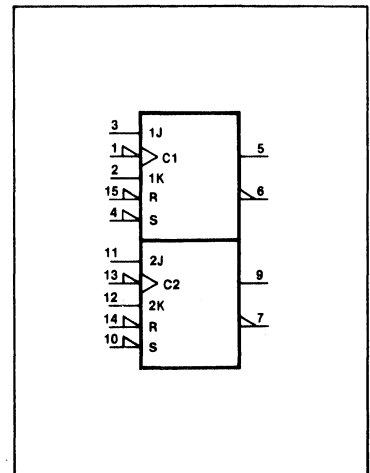
PIN CONFIGURATION



LOGIC SYMBOL



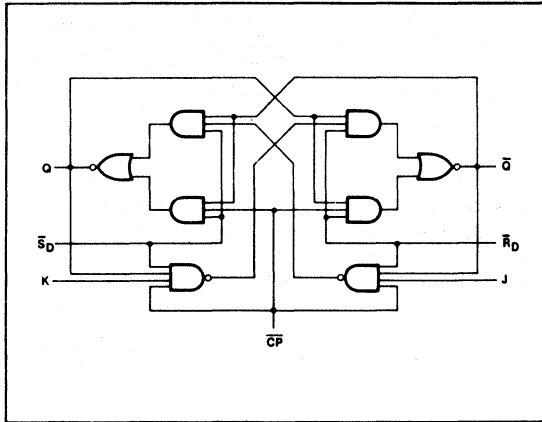
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/74LS112, S112

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	S _D	R _D	CP	J	K	Q	Q̄
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	q̄	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	q̄

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
 q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
 X = Don't care.
 ↓ = HIGH-to-LOW Clock transition.

NOTE
 Both outputs will be HIGH while both S_D and R_D are LOW, but the output states are unpredictable if S_D and R_D go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to -7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-18			-18	mA
I _{OH} HIGH-level output current				-400			-1000	μA
I _{OL} LOW-level output current	Mil			4			20	mA
	Com'l			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

NOTE
 V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS112			54/74S112			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		2.5	3.4	V	
		Com'l	2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.25	0.4		0.5 ⁵	V
		I _{OL} = 4mA	Com'l		0.35	0.5		0.5	V
			74LS		0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA	
		V _I = 7.0V	J, K Inputs		0.1			mA	
			\bar{R}_D, \bar{S}_D Inputs		0.3			mA	
			$\bar{C}\bar{P}$ Inputs		0.4			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	J, K Inputs		20		50	μA	
			\bar{R}_D, \bar{S}_D Inputs		60		100	μA	
			$\bar{C}\bar{P}$ Inputs		80		100	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	J, K Inputs		-0.4			mA	
			\bar{R}_D, \bar{S}_D Inputs		-0.8			mA	
			$\bar{C}\bar{P}$ Inputs		-0.8			mA	
		V _I = 0.5V	J, K Inputs					-1.6	mA
			\bar{R}_D, \bar{S}_D Inputs					-7	mA
			$\bar{C}\bar{P}$ Inputs					-4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			4	8		15	50	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.
 - V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum Clock frequency	Waveform 1	30		80		MHz
t _{PLH} Propagation delay	Waveform 1		20		7.0	ns
t _{PHL} Clock to output			30		7.0	
t _{PLH} Propagation delay	Waveform 2		20		7.0	ns
t _{PHL} \bar{S}_D or \bar{R}_D to output			30		7.0	

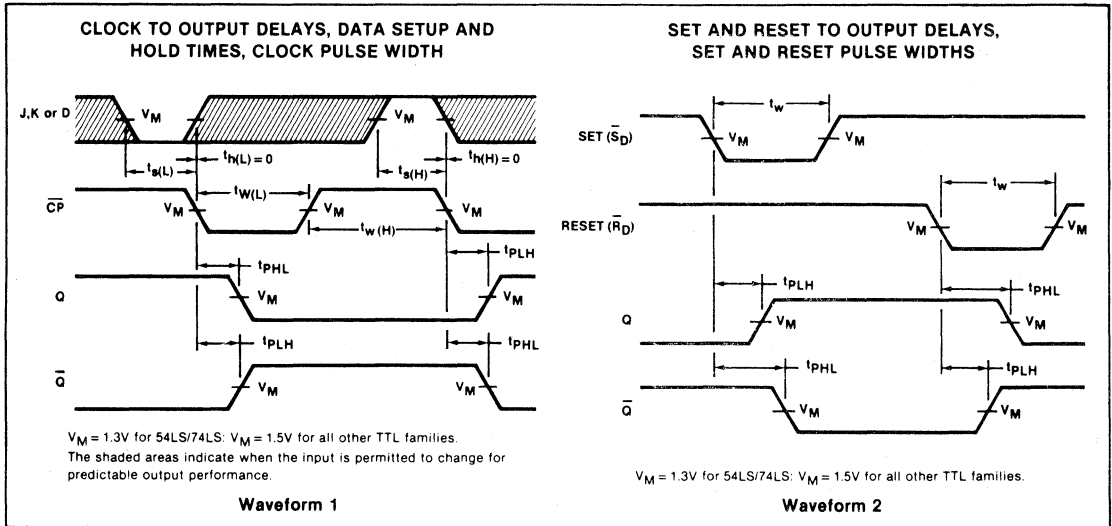
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.



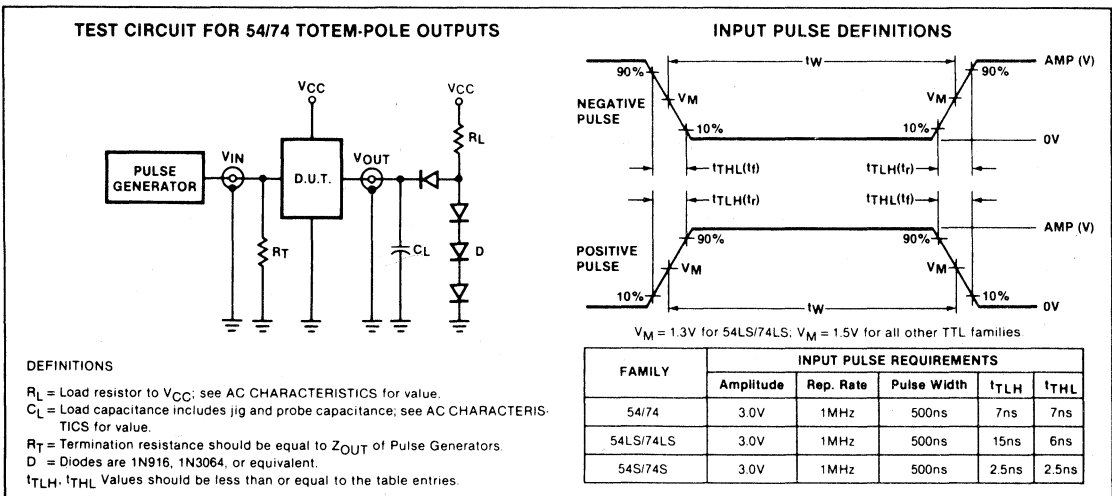
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74LS		54/74S		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$ Clock pulse width (HIGH)	Waveform 1	20		6.0		ns
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	13		6.5		ns
$t_{W(L)}$ Set or Reset pulse width (LOW)	Waveform 2	25		8.0		ns
t_s Setup time J or K to Clock	Waveform 1	20		3.0		ns
t_h Hold time J or K to Clock	Waveform 1	0		0		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



FLIP-FLOPS

54/74LS113, S113

Dual J-K Edge-Triggered Flip-Flop

DESCRIPTION

The '113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set (\bar{S}_D) input, when LOW, forces the outputs to the steady state levels as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock (\bar{CP}) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the \bar{CP} is HIGH and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of \bar{CP} .

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS113	45MHz	4mA
74S113	125MHz	15mA

ORDERING CODE

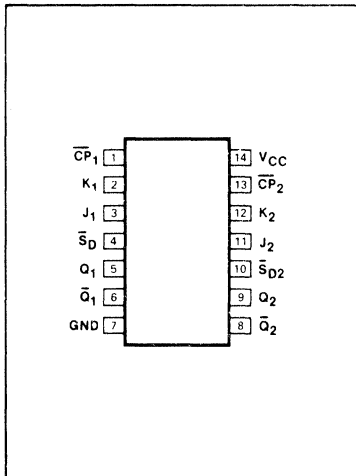
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S113N • N74LS113N	
Ceramic DIP		S54S113F • S54LS113F
Flatpack		S54S113W • S54LS113W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

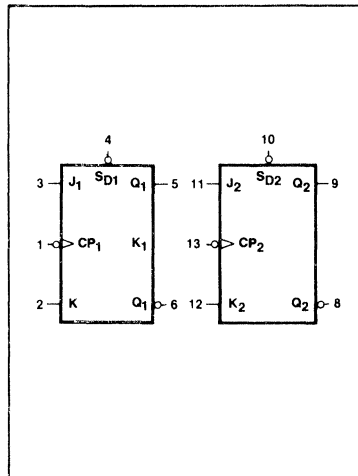
PINS	DESCRIPTION	54/74S	54/74LS
\bar{CP}	Clock input	2Sul	4LSul
\bar{S}_D	Set inputs	3.5Sul	3LSul
J, K	Data inputs	1Sul	1LSul
Q, \bar{Q}	Outputs	10Sul	10LSul

NOTE
A 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

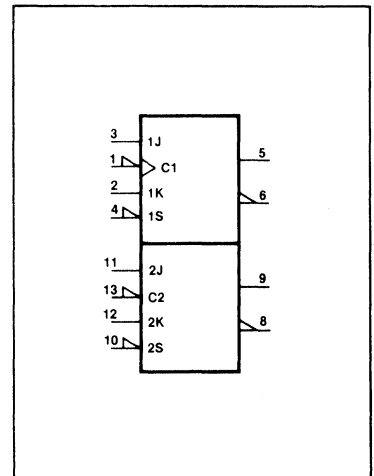
PIN CONFIGURATION



LOGIC SYMBOL



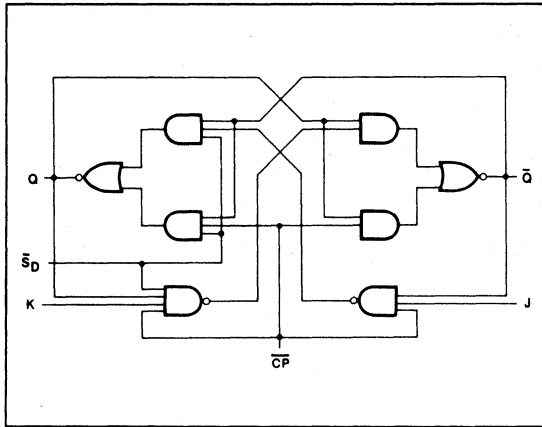
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/74LS113, S113

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	\bar{S}_D	$\bar{C}P$	J	K	Q	\bar{Q}
Asynchronous Set	L	X	X	X	H	L
Toggle	H	i	h	h	\bar{q}	q
Load "0" (Reset)	H	i	i	h	L	H
Load "1" (Set)	H	i	h	i	H	L
Hold "no change"	H	i	i	i	q	\bar{q}

- H = HIGH voltage level steady state.
- h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
- L = LOW voltage level steady state.
- l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
- q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
- X = Don't care.
- i = HIGH-to-LOW Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to -7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-18			-18	mA
I_{OH} HIGH-level output current				-400			-1000	μ A
I_{OL} LOW-level output current	Mil			4			20	mA
	Com'l			8			20	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

NOTE
 $V_{IL} = +0.7V$ MAX for 54S at $T_A = +125^\circ C$ only.

FLIP-FLOPS

54/74LS113, S113

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS113			54/74S113			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		2.5	3.4	V	
		Com'l	2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4		0.5 ⁵	V	
			Com'l	0.35	0.5		0.5	V	
		I _{OL} = 4mA	74LS	0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA	
		V _I = 7.0V	J, K Inputs		0.1			mA	
			\bar{S}_D Inputs		0.3			mA	
			$\bar{C}\bar{P}$ Inputs		0.4			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	J, K Inputs		20		50	μ A	
			\bar{S}_D Inputs		60		100	μ A	
			$\bar{C}\bar{P}$ Inputs		80		100	μ A	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	J, K Inputs		-0.4			mA	
			\bar{S}_D Inputs		-0.8			mA	
			$\bar{C}\bar{P}$ Inputs		-0.8			mA	
		V _I = 0.5V	J, K Inputs					-1.6	mA
			\bar{S}_D Inputs					-7	mA
			$\bar{C}\bar{P}$ Inputs					-4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			4	8		15	50	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs HIGH in turn.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 2k Ω		C _L = 15pF, R _L = 280 Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum Clock frequency	Waveform 1	30		80		MHz
t _{PLH} Propagation delay	Waveform 1		20		7.0	ns
t _{PHL} Clock to output			30		7.0	
t _{PLH} Propagation delay	Waveform 2		20		7.0	ns
t _{PHL} Set to output			30		7.0	

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

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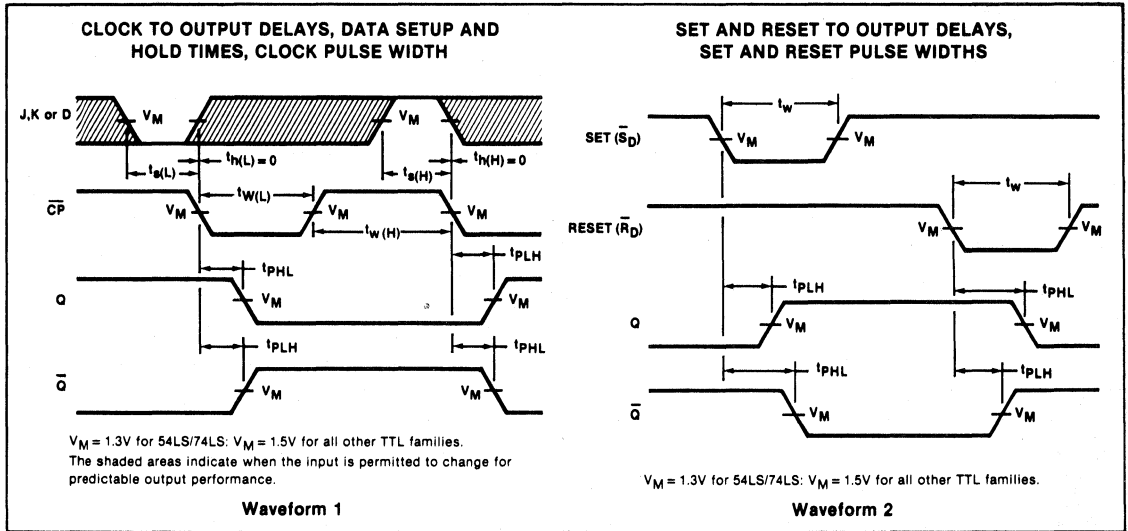
FLIP-FLOPS

54/74LS113, S113

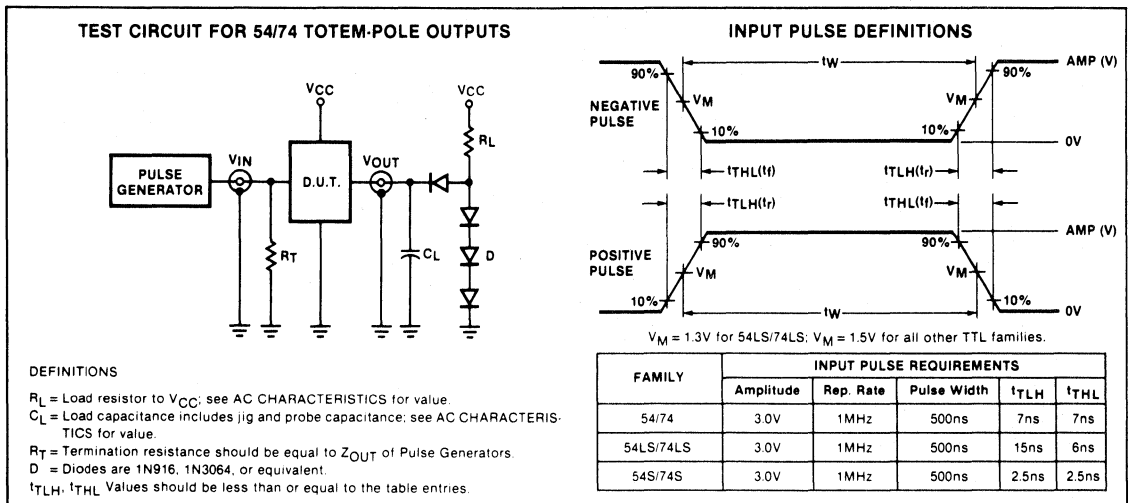
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74LS		54/74S		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$ Clock pulse width (HIGH)	Waveform 1	20		6.0		ns
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	13		6.5		ns
$t_{W(L)}$ Set pulse width (LOW)	Waveform 2	25		8.0		ns
t_s Setup time J or K to Clock	Waveform 1	20		3.0		ns
t_h Hold time J or K to Clock	Waveform 1	0		0		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



LATCH

54/74116

Dual 4-Bit Transparent Latch

DESCRIPTION

The '116 has two independent 4-bit transparent latches. Each 4-bit latch is controlled by a two-input active LOW Enable gate (\bar{E}_0 and \bar{E}_1). When both \bar{E}_0 and \bar{E}_1 are LOW, the data enters the latch and appears at the output. The outputs follow the Data inputs as long as \bar{E}_0 and \bar{E}_1 are LOW. The data on the D inputs one setup time before the LOW-to-HIGH transition of \bar{E}_0 or \bar{E}_1 will be stored in the latch. The Latched outputs remain stable as long as either \bar{E}_0 or \bar{E}_1 is HIGH.

Each 4-bit latch has an active LOW asynchronous Master Reset (\bar{MR}) input. When LOW, the \bar{MR} input overrides the Data and Enable inputs and sets the four Latch outputs LOW.

TYPE	TYPICAL PROPAGATION DELAY—DATA TO OUTPUT	TYPICAL SUPPLY CURRENT (Total)
74116	11ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74116N	
Ceramic DIP		S54116F
Flatpack		S54116W

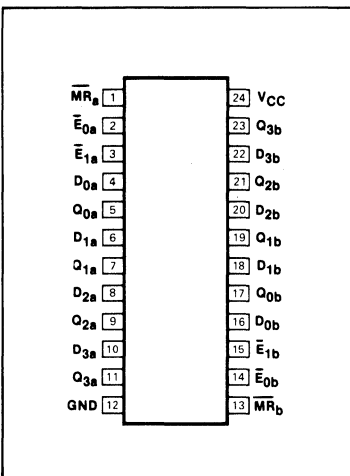
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
\bar{E}_0, \bar{E}_1	Enable inputs	1uI
D_0-D_3	Data inputs	1.5uI
\bar{MR}	Master Reset input	1uI
Q_0-Q_3	Latch outputs	10uI

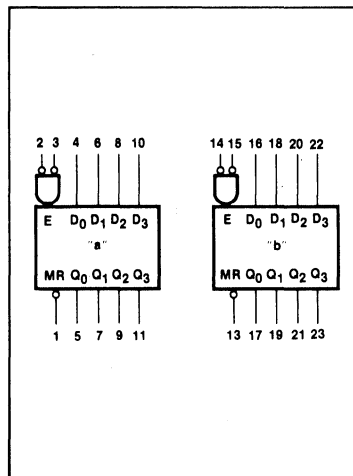
NOTE
Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} .

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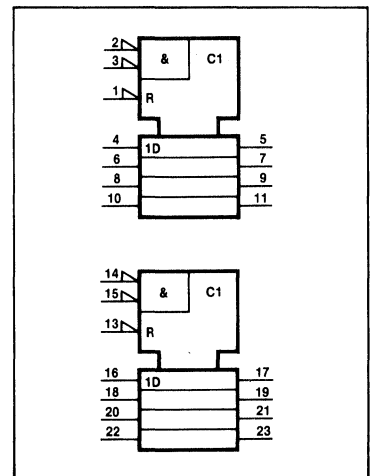
PIN CONFIGURATION



LOGIC SYMBOL



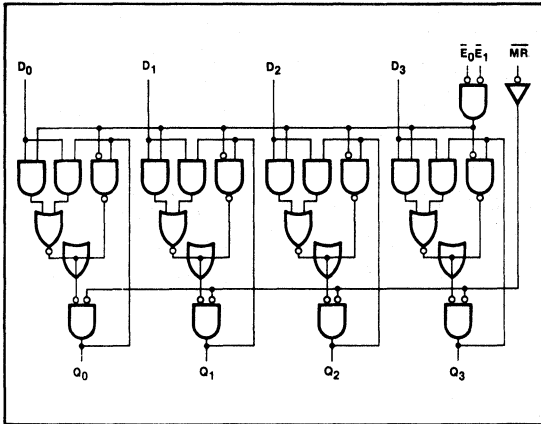
LOGIC SYMBOL (IEEE/IEC)



LATCH

54/74116

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUT
	\overline{MR}	\overline{E}_0	\overline{E}_1	D_n	Q_n
Reset (clear)	L	X	X	X	L
Enable latch	H	L	L	L	L
	H	L	L	H	H
Latch data	H	l	L	l	L
	H	L	l	h	H

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH Enable transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Enable transition.
 X = Don't care.
 † = LOW-to-HIGH Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to +15	-0.5 to +15	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT
		Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8	V
	Com'l			+0.8	V
I_{IK} Input clamp current				-12	mA
I_{OH} HIGH-level output current				-800	μA
I_{OL} LOW-level output current	Mil			16	mA
	Com'l			16	mA
T_A Operating free-air temperature	Mil	-55		+125	°C
	Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74116			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4	V
		Com'l	2.4	3.4	V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.2	V
		Com'l		0.2	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			- 1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	\bar{E} , \bar{MR} Inputs		40	μ A
		D Inputs		60	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	\bar{E} , \bar{MR} Inputs		- 1.6	mA
		D Inputs, initial peak		- 2.4	mA
		D Inputs, steady-state		- 1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	- 20	- 57	mA
		Com'l	- 18	- 57	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		60	mA
		Condition 2		40	70

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Condition 1. Measure I_{CC} with all inputs grounded and all outputs open. Condition 2. Measure I_{CC} with \bar{E} inputs grounded, all other inputs at 4.5V and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay Enable to output	Waveform 1		30 22	ns
t _{PLH} t _{PHL} Propagation delay Data to output	Waveform 2		15 18	ns
t _{PHL} Propagation delay \bar{MR} to output	Waveform 3		22	ns



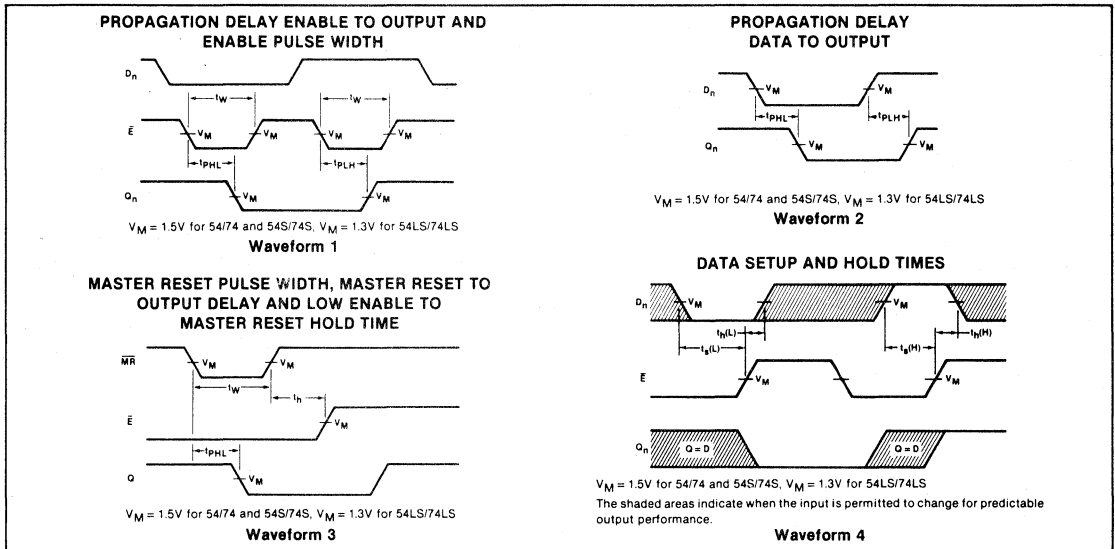
LATCH

54/74116

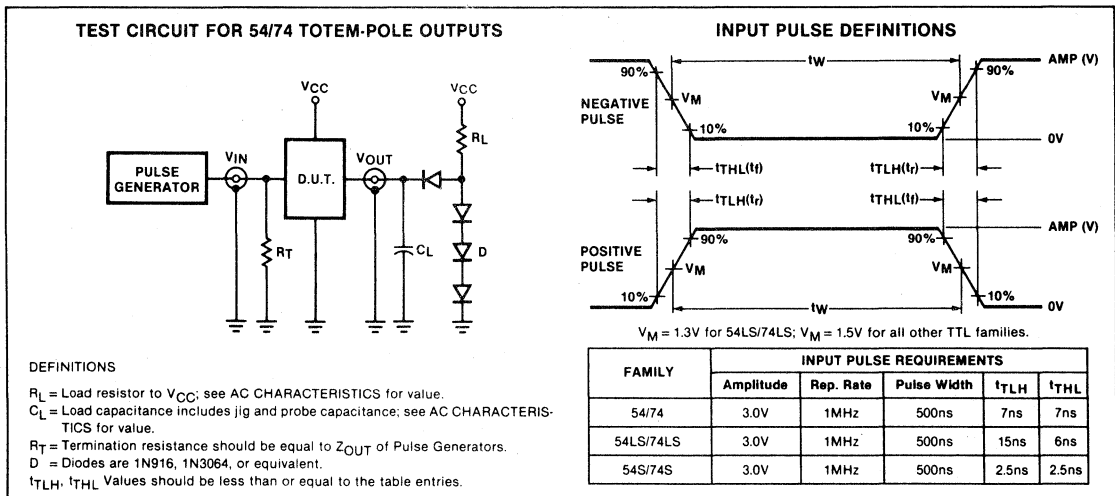
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		Min	Max	
t_W Enable pulse width	Waveform 1	18		ns
t_W Master Reset pulse width	Waveform 3	18		ns
$t_s(H)$ Setup time HIGH Data to Enable	Waveform 4	8.0		ns
$t_h(H)$ Hold time HIGH Data to Enable	Waveform 4		-2.0	ns
$t_s(L)$ Setup time LOW Data to Enable	Waveform 4	14.0		ns
$t_h(L)$ Hold time LOW Data to Enable	Waveform 4	8.0		ns
$t_h(L)$ Hold time LOW Enable to Master Reset to load HIGH	Waveform 3	8.0		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



MULTIVIBRATOR

54/74121

Monostable Multivibrator

- Very good pulse width stability
- Virtually immune to temperature and voltage variations
- Schmitt trigger input for slow input transitions
- Internal timing resistor provided

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74121	43ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74121N	
Plastic SO	N74121D	
Ceramic DIP		S54121F
Flatpack		S54121W

DESCRIPTION

These multivibrators feature dual active LOW going edge inputs and a single active HIGH going edge input which can be used as an active HIGH enable input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry. Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 20 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC} , C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

FUNCTION TABLE

INPUTS			OUTPUTS	
\bar{A}_1	\bar{A}_2	B	Q	\bar{Q}
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↑	H	↓	↑
↓	H	H	↓	↑
↓	↓	H	↓	↑
L	X	↑	↓	↑
X	L	↑	↓	↑

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH transition
 ↓ = HIGH-to-LOW transition

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
\bar{A}_1, \bar{A}_2	Inputs	1uI
B	Input	2uI
Q, \bar{Q}	Outputs	10uI

NOTE
 A 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 30kΩ

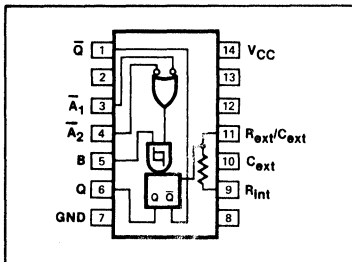
for the 54121 and 2KΩ to 40kΩ for the 74121). Throughout these ranges, pulse width is defined by the relationship: (see Figure 1)

$$t_W(\text{out}) = C_{ext} R_{ext} \ln 2$$

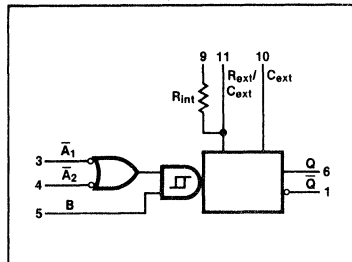
$$t_W(\text{out}) \approx 0.7 C_{ext} R_{ext}$$

In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4kΩ may be used.

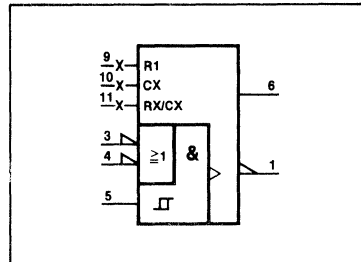
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MULTIVIBRATOR

54/74121

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I _{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
I _{IK}	Input clamp current				- 12	mA
I _{OH}	HIGH-level output current				- 400	μA
I _{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
dv/dt	Rate of rise or fall of input pulse	B input	1			V/s
		\bar{A}_1, \bar{A}_2 inputs	1			V/μs
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74121			UNIT	
		Min	Typ ²	Max		
V _{T+}	Positive-going threshold at \bar{A} and B V _{CC} = MIN			2.0	V	
V _{T-}	Negative-going threshold at \bar{A} and B V _{CC} = MIN	0.8			V	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4	V	
		Com'l	2.4	3.4	V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			- 1.5	V	
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.4V	\bar{A}_1, \bar{A}_2 inputs			40	μA
		B input			80	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V	\bar{A}_1, \bar{A}_2 inputs			- 1.6	mA
		B input			- 3.2	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	Mil	- 20		- 55	mA
		Com'l	- 18		- 55	mA
I _{CC}	Supply current (total) V _{CC} = MAX	Quiescent		13	25	mA
		Triggered		23	40	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

MULTIVIBRATOR

54/74121

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

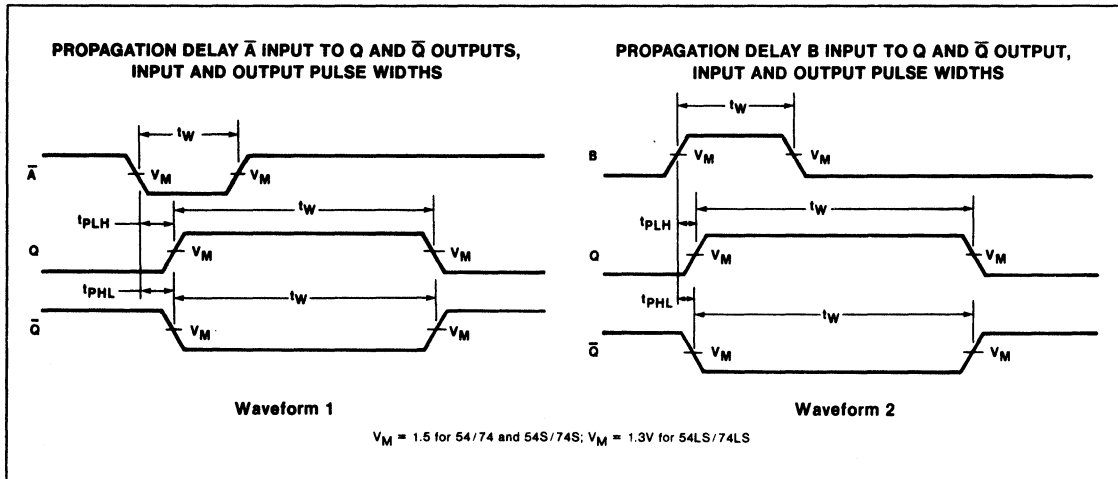
PARAMETER	TEST CONDITIONS	54/74		UNIT	
		$C_L = 15\text{pF}$, $R_L = 400\Omega$			
		Min	Max		
t_{PLH} t_{PHL}	Propagation delay \bar{A} input to Q & \bar{Q} output	Waveform 1		ns	
	$C_{ext} = 80\text{pF}$, R_{int} to V_{CC}	70	80		
t_{PLH} t_{PHL}	Propagation delay B input to Q & \bar{Q} output	Waveform 2		ns	
	$C_{ext} = 80\text{pF}$, R_{int} to V_{CC}	55	65		
t_W	Minimum output pulse width	$C_{ext} = 0\text{pF}$, R_{int} to V_{CC}	20	50	ns
t_W	Output pulse width	$C_{ext} = 80\text{pF}$, R_{int} to V_{CC}	70	150	ns
		$C_{ext} = 100\text{pF}$, $R_{ext} = 10\text{k}\Omega$	600	800	ns
		$C_{ext} = 1\mu\text{F}$, $R_{ext} = 10\text{k}\Omega$	6.0	8.0	ms

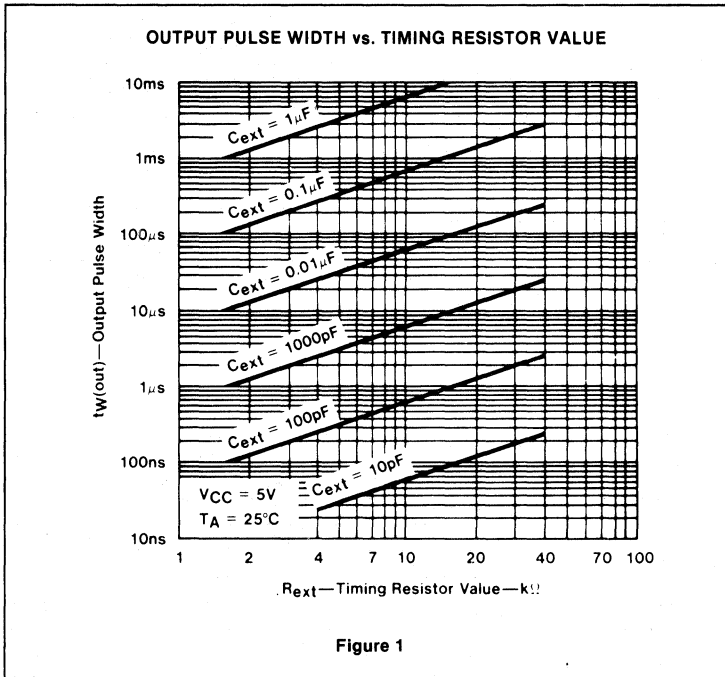
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT	
		Min	Max		
t_W	Minimum input pulse width to trigger	Waveforms 1 & 2		ns	
R_{ext}	External timing resistor range	Mil	1.4	30	k Ω
		Com'l	1.4	40	k Ω
C_{ext}	External timing capacitance range	0	1000	μF	
Output duty cycle	$R_{ext} = 2\text{k}\Omega$		67	%	
	$R_{ext} = R_{ext}(\text{Max})$		90	%	

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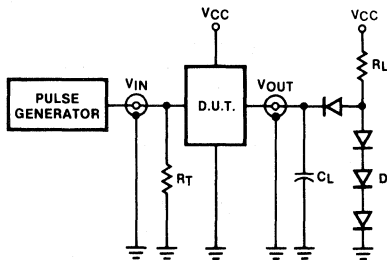
AC WAVEFORMS





TEST CIRCUITS AND WAVEFORMS

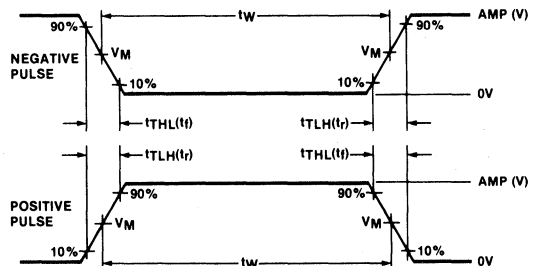
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIVIBRATOR

54/74123

Dual Retriggerable Monostable Multivibrator

- DC triggered from active HIGH or active LOW inputs
- Retriggerable for very long pulses—up to 100% duty cycle
- Direct reset terminates output pulse
- Compensated for V_{CC} and temperature variations

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74123	24ns	46mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74123N	
Plastic SO	N74123D	
Ceramic DIP		S54123F
Flatpack		S54123W

DESCRIPTION

The '123 is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance (R_{ext}) and capacitance (C_{ext}) values. Once triggered, the basic pulse width may be extended by retriggering the gated active LOW going edge input (\bar{A}) or the active HIGH going edge input (B), or be reduced by use of the overriding active LOW reset.

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000pF$, see Figure A.

When $C_{ext} > 1000pF$, the output pulse width is defined as:

$$t_W \cong 0.28 R_{ext} \cdot C_{ext} \left(1 + \frac{0.7}{R_{ext}} \right)$$

The external resistance and capacitance are normally connected as shown in Fig-

FUNCTION TABLE

INPUTS			OUTPUTS	
R_D	\bar{A}	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		
↑	L	H		

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH transition
 ↓ = HIGH-to-LOW transition
 = One HIGH-level pulse
 = One LOW-level pulse

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
\bar{A} , B	Inputs	1uI
R_D	Input	2uI
Q, \bar{Q}	Outputs	10uI

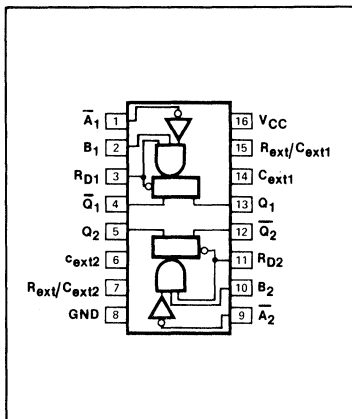
NOTE
 A 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} .

ure B. If an electrolytic capacitor is to be used with an inverse voltage rating of less than 1V then Figure C should be used. (Inverse voltage rating of an electrolytic is normally specified at 5% of the forward voltage rating.) If the inverse voltage

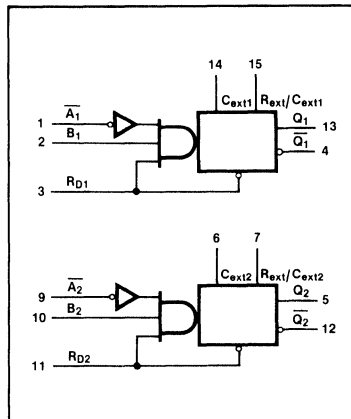
rating is 1V or more (this includes a 100% safety margin) then Figure B can be used. Note that if Figure C is used the timing equations change as follows:

$$t_W \cong 0.25 R_{ext} \cdot C_{ext} \left(1 + \frac{0.7}{R_{ext}} \right)$$

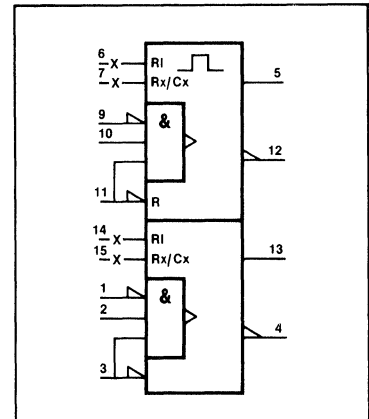
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MULTIVIBRATOR

54/74123

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I_{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
I_{IK}	Input clamp current			- 12	mA	
I_{OH}	HIGH-level output current			- 800	μ A	
I_{OL}	LOW-level output current	Mil		16	mA	
		Com'l		16	mA	
T_A	Operating free-air temperature	Mil	- 55	+ 125	°C	
		Com'l	0	70	°C	
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage			+ 0.8	V	

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74123			UNIT		
		Min	Typ ²	Max			
V_{OH}	HIGH-level output voltage ⁵	$V_{CC} = \text{MIN}, I_{OH} = \text{MAX}$	Mil	2.4	3.4	V	
			Com'l	2.4	3.4	V	
V_{OL}	LOW-level output voltage ⁵	$V_{CC} = \text{MIN}, I_{OL} = \text{MAX}$	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			- 1.5	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$	\bar{A}, B inputs		40	μ A	
			R_D input		80	μ A	
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$	\bar{A}, B inputs		- 1.6	mA	
			R_D input		- 3.2	mA	
I_{OS}	Short-circuit output current ^{3,5}	$V_{CC} = \text{MAX}$	- 10		- 40	mA	
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	Quiescent	46	66	mA	
			Triggered	46	66	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Quiescent I_{CC} is measured (after being reset) with 2.4V applied to both R_D and \bar{A} inputs, B inputs grounded and all outputs open. Triggered I_{CC} is measured with 2.4V applied to all R_D and B inputs, \bar{A} inputs grounded and all outputs open. For both measurements, $C_{EXT} = 0.02\mu\text{F}$ and $R_{EXT} = 25\text{k}\Omega$.
- Ground C_{EXT} to measure V_{OH} at Q, V_{OL} at \bar{Q} , or I_{OS} at Q. C_{EXT} is open to measure V_{OH} at \bar{Q} , V_{OL} at Q, or I_{OS} at \bar{Q} .

MULTIVIBRATOR

54/74123

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

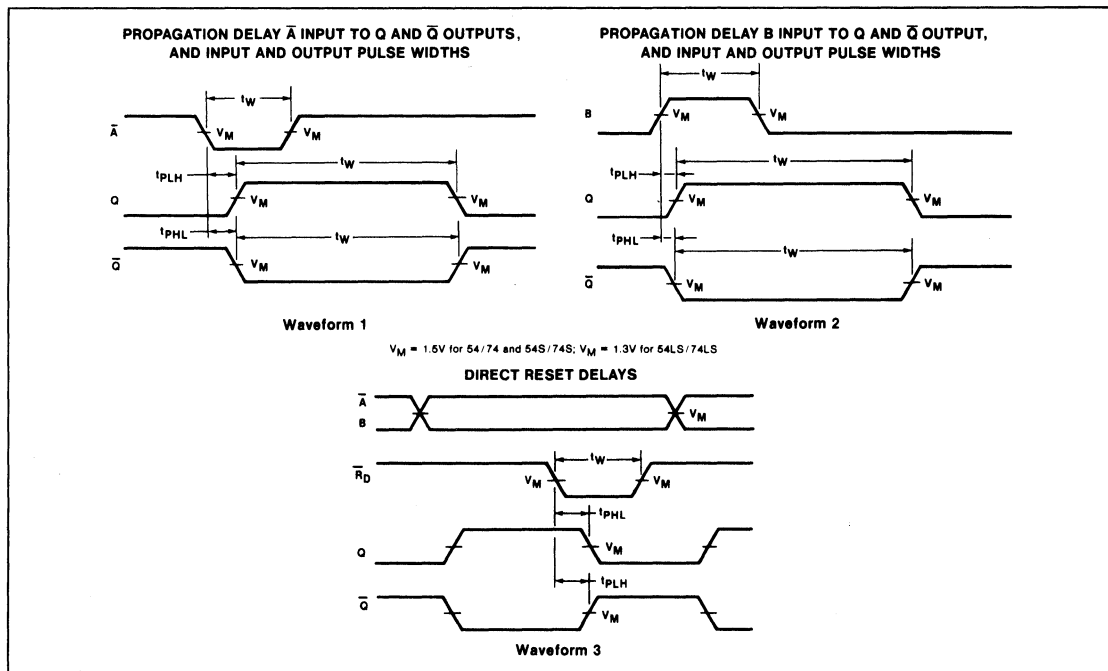
PARAMETER	TEST CONDITIONS	54/74		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		
		Min	Max	
t_{PLH} t_{PHL} Propagation delay \bar{A} input to Q & \bar{Q} output	Waveform 1 $C_{ext} = 0\text{pF}$, $R_{ext} = 5\text{k}\Omega$		33 40	ns
t_{PLH} t_{PHL} Propagation delay B input to Q & \bar{Q} output	Waveform 2 $C_{ext} = 0\text{pF}$, $R_{ext} = 5\text{k}\Omega$		28 36	ns
t_{PLH} t_{PHL} Propagation delay \bar{R}_D input to Q & \bar{Q} output	Waveform 3 $C_{ext} = 0\text{pF}$, $R_{ext} = 5\text{k}\Omega$		40 27	ns
t_W Q Minimum Q pulse width	Waveforms 1 & 2 $C_{ext} = 0\text{pF}$, $R_{ext} = 5\text{k}\Omega$		65	ns
t_W Q Output pulse width	Waveforms 1 & 2 $C_{ext} = 1000\text{pF}$, $R_{ext} = 10\text{k}\Omega$	2.76	3.37	μs

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		Min	Max	
t_W Minimum input pulse width	Waveforms 1, 2 & 3	40		ns
R_{ext} External timing resistor range	Mil	5.0	25	k Ω
	Com'l	5.0	50	
C_{ext} External timing capacitance range		No restriction		pF
C_{RxCx} Stray capacitance to GND at R_{ext}/C_{ext} terminal			50	pF

4

AC WAVEFORMS

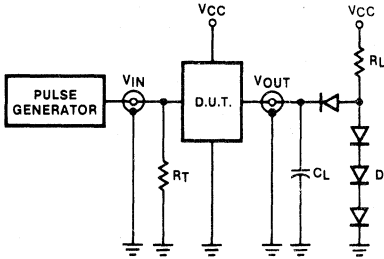


MULTIVIBRATOR

54/74123

TEST CIRCUITS AND WAVEFORMS

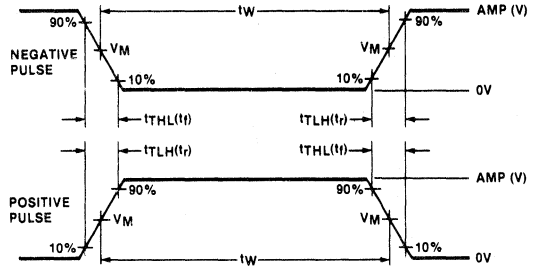
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

TYPICAL PERFORMANCE CHARACTERISTICS

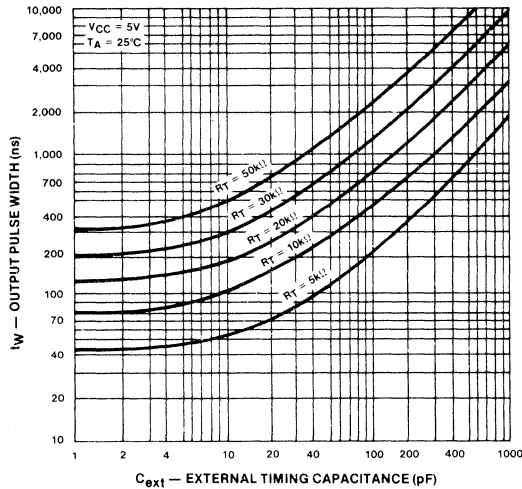


Figure A

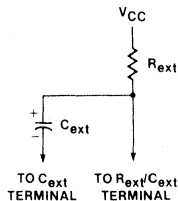


Figure B

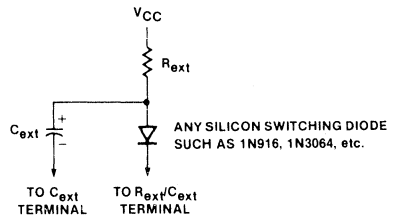


Figure C

BUFFERS

54/74125, 54/74126, LS125A, LS126A

Quad 3-State Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74125	10ns	32mA
74LS125A	8ns	11mA
74126	10ns	36mA
74LS126A	9ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74125N • N74LS125N N74126N • N74LS126N	
Plastic SO	N74LS125AD	
Ceramic DIP		S54LS125AF S54126F • S54LS126AF
Flatpack		S54LS125AW S54126W • S54LS126AW
LLCC		S54LS125G

FUNCTION TABLE '125, 'LS125A

INPUTS		OUTPUT
C	A	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE '126, 'LS126A

INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	(Z)

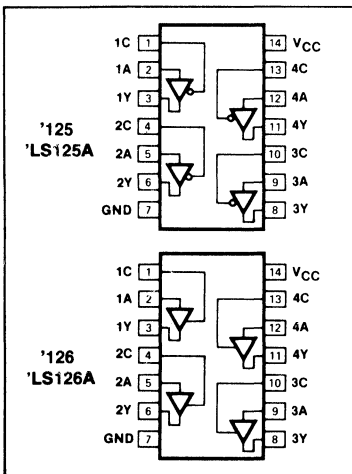
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off)

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

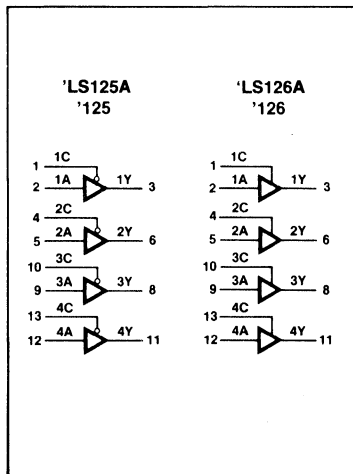
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1uI	1LSuI
All	Outputs	10uI	30LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} and, and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and -0.4mA I_{IL} .

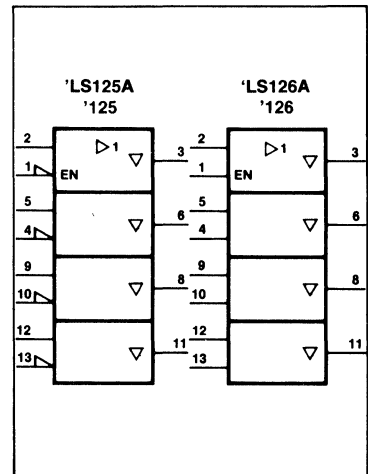
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUFFERS

54/74125, 54/74126, LS125A, LS126A

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

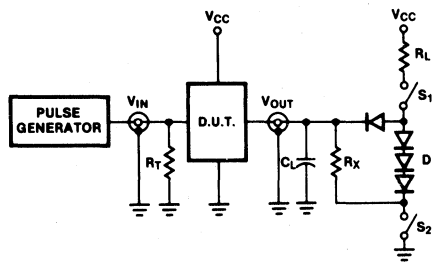
PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current	Mil			-2.0			-1.0	mA
	Com'l			-5.2			-2.6	mA
I _{OL} LOW-level output current	Mil			16			12	mA
	Com'l			16			24	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



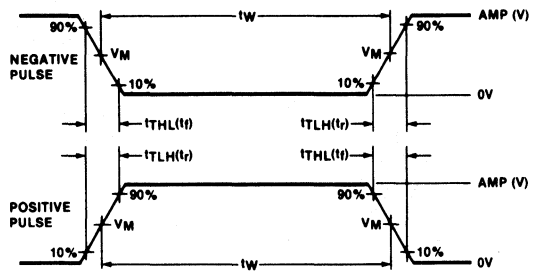
SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS

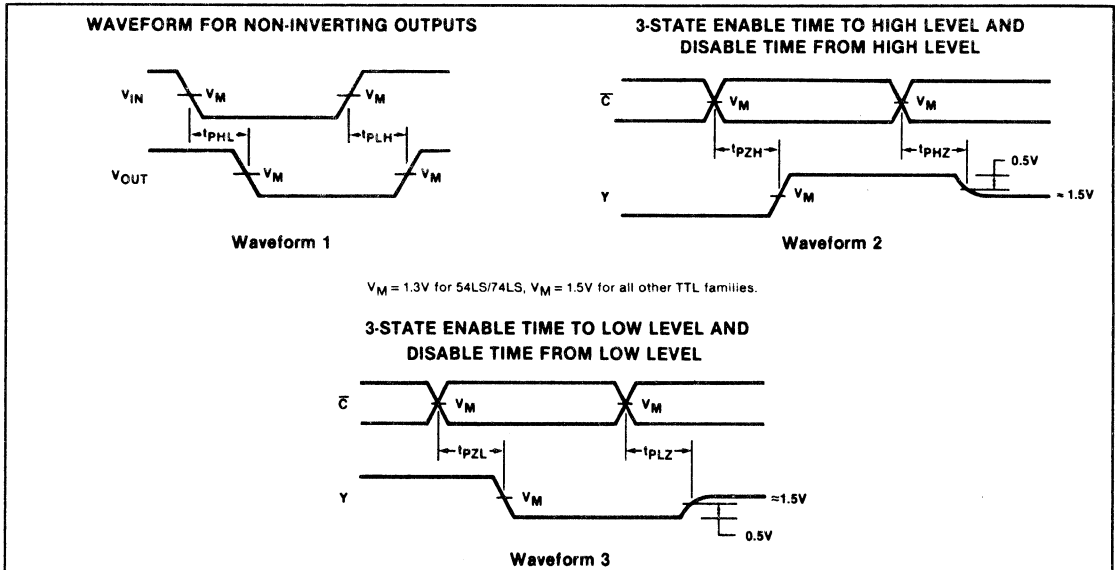
54/74125, 54/74126, LS125A, LS126A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74125 54/74126			54/74LS125A 54/74LS126A			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.3		2.4			V
		Com'l	2.4	3.1		2.4			V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.4		0.25	0.4	V
			Com'l			0.4		0.35	0.5
		I _{OL} = 12mA	74LS					0.25	0.4
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.4V				40			20	μA
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.4V				-40			-20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA
		V _I = 7.0V						0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40				μA
		V _I = 2.7V						20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-30		-70	-40		-130	mA
		Com'l	-28		-70	-40		-130	mA
I _{CC} Supply current (total)	V _{CC} = MAX	'125		32	54		11	20	mA
		'126		36	62		12	22	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



4

BUFFERS**54/74125, 54/74126, LS1254A, LS126A****AC CHARACTERISTICS** $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74125		54/74LS125A		54/74126		54/74LS126A		UNIT
		$C_L = 50\text{pF}$ $R_L = 400\Omega$		$C_L = 45\text{pF}$ $R_L = 667\Omega$		$C_L = 50\text{pF}$ $R_L = 400\Omega$		$C_L = 45\text{pF}$ $R_L = 667\Omega$		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay		13		15		13		15	ns
t_{PHL}	Data to output		18		18		18		18	
t_{PZH}	Enable to HIGH		17		20		18		25	ns
t_{PZL}	Enable to LOW		25		25		25		35	ns
t_{PHZ}	Disable from HIGH		8.0		20		16		25	ns
t_{PLZ}	Disable from LOW		12		20		18		25	ns

BUFFER

54/74128

Quad Two-Input NOR Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74128	7ns	23mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74128N	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

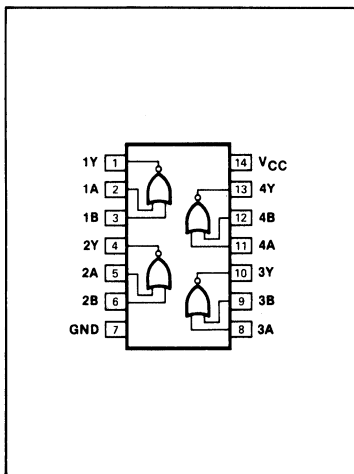
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
A, B	Inputs	1ul
Y	Output	30ul

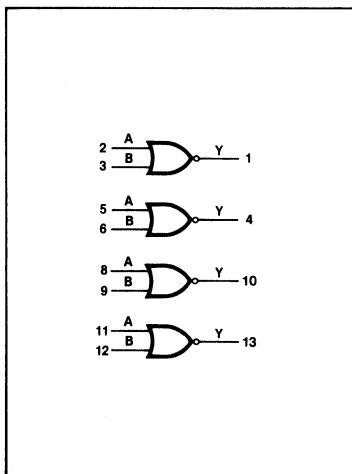
NOTE
Where a 54/74 unit load is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

4

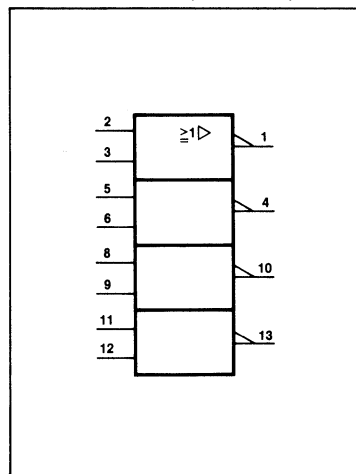
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUFFER

54/74128

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

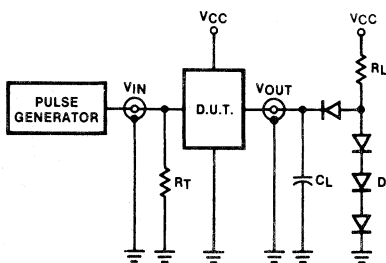
PARAMETER		54	74	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT		
		Min	Nom	Max			
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	V	
V _{IH}	HIGH-level input voltage	2.0			V		
V _{IL}	LOW-level input voltage	Mil			+0.8	V	
		Com'l			+0.8	V	
I _{IK}	Input clamp current				-12	mA	
I _{OH}	HIGH-level output current	Mil			-29	mA	
		Com'l			-42.4	mA	
I _{OL}	LOW-level output current	Mil			48	mA	
		Com'l			48	mA	
T _A	Operating free-air temperature	Mil	-55			+125	°C
		Com	0			70	°C

TEST CIRCUITS AND WAVEFORMS

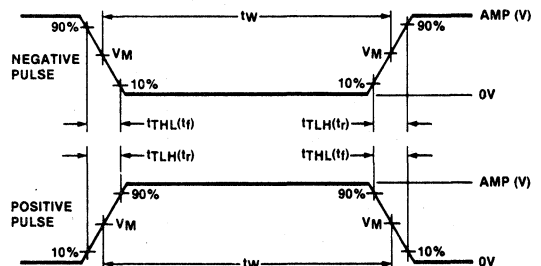
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

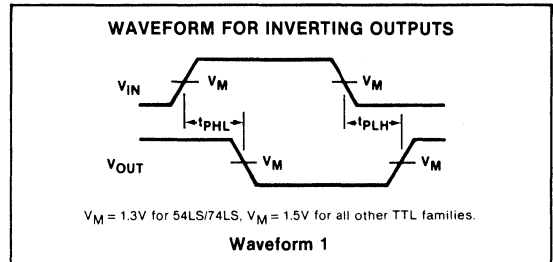
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74128			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = 0.8V, I _{OH} = -2.4mA	2.4	3.4		V	
	V _{CC} = MIN, V _{IL} = 0.4V, I _{OH} = -13.2mA	2.4			V	
	V _{CC} = MIN, V _{IL} = 0.4V, I _{OH} = MAX	Mill	2.0			V
		Com'l	2.0			V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX	Mill		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _i = I _{IK}				-1.5	V
I _i Input current at maximum input voltage	V _{CC} = MAX, V _i = 5.5V				1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _i = 2.4V				40	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _i = 0.4V				-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-70			-180	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		12	21	mA
		I _{CCL} Outputs LOW		33	57	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT
		R _L = 133Ω		
		Min	Max	
t _{PLH} t _{PHL}	Waveform 1, C _L = 50pF		9 12	ns
t _{PLH} t _{PHL}	Waveform 1, C _L = 150pF		15 18	ns

SCHMITT TRIGGERS

54/74132, LS132

Quad 2-Input NAND Schmitt Trigger

DESCRIPTION

The 132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mW) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+MAX} , the gate will respond to the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74132	15ns	21mA
74LS132	15ns	7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74132N • N74LS132N	
Ceramic DIP		S54132F • S54LS132F
Flatpack		S54132W • S54LS132W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

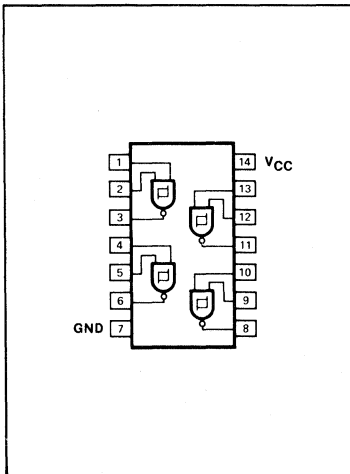
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

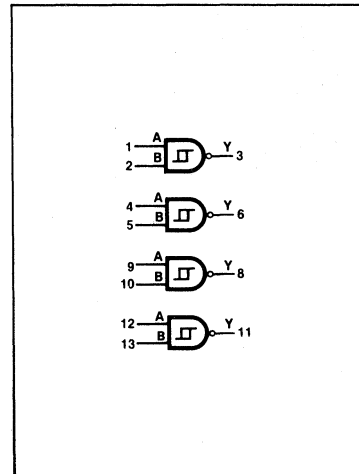
PINS	DESCRIPTION	54/74	54/74LS
A, B	Inputs	1uI	1LSuI
Y	Output	10uI	10LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

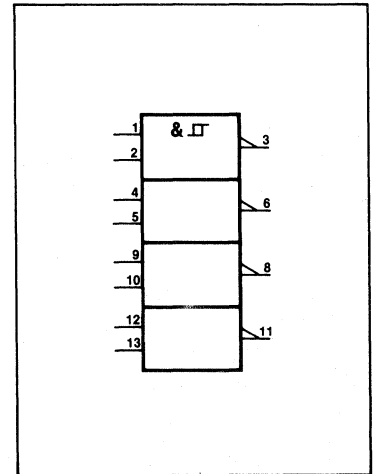
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
I _{IK}	Input clamp current			-12			-18	mA	
I _{OH}	HIGH-level output current			-800			-400	μA	
I _{OL}	LOW-level output current	Mil		16			4	mA	
		Com'l		16			8	mA	
T _A	Operating free-air temperature	Mil	-55	+125	-55		+125	°C	
		Com'l	0	70	0		70	°C	



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

SCHMITT TRIGGERS

54/74132, LS132

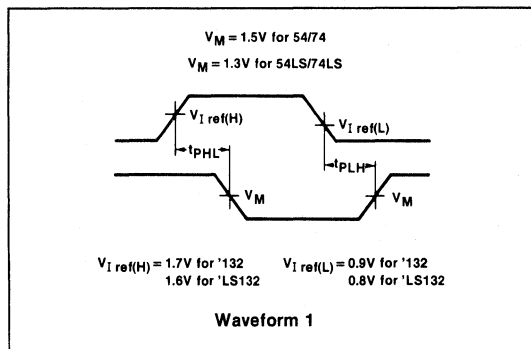
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74132			54/74LS132			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{T+} Positive-going threshold	V _{CC} = 5.0V	1.5	1.7	2.0	1.4	1.6	1.9	V
V _{T-} Negative-going threshold	V _{CC} = 5.0V	0.6	0.9	1.1	0.5	0.8	1.0	V
ΔV _T Hysteresis (V _{T+} - V _{T-})	V _{CC} = 5.0V	0.4	0.8		0.4	0.8		V
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _I = V _{T-} MIN, I _{OH} = MAX	Mil	2.4	3.4	2.5	3.4		V
		Com'l	2.4	3.4	2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _I = V _{T+} MAX	I _{OL} = MAX	Mil	0.2	0.4	0.25	0.4	V
		I _{OL} = 4mA	Com'l	0.2	0.4	0.35	0.5	V
			74LS				0.25	0.4
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5		-1.5	V	
I _{T+} Input current at positive-going threshold	V _{CC} = 5.0V, V _I = V _{T+}		-0.43		-0.14		mA	
I _{T-} Input current at negative-going threshold	V _{CC} = 5.0V, V _I = V _{T-}		-0.56		-0.18		mA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V		1.0			mA	
		V _I = 7.0V				0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V		40			μA	
		V _I = 2.7V				20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.2		-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-18	-55	-20	-100	mA	
		Com'l	-18	-55	-20	-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		15	24	5.9	11	mA
		I _{CCL} Outputs LOW		26	40	8.2	14	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS

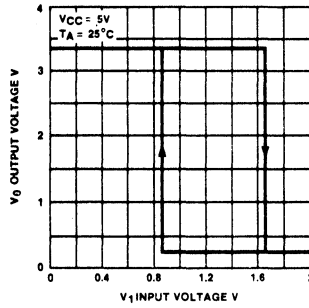


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

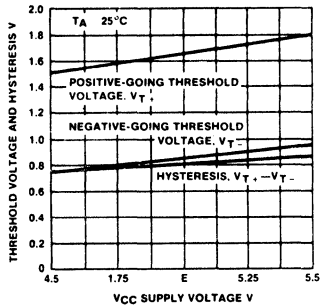
PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		22 22		22 22	ns

TYPICAL CHARACTERISTICS

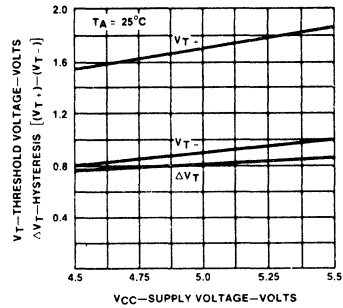
(54/74, 54LS/74LS)
VIN vs VOUT
TRANSFER FUNCTION



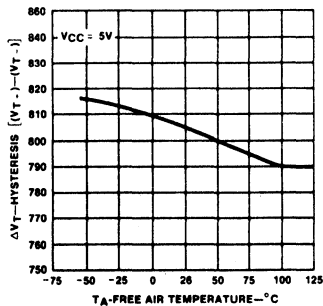
(54/74)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



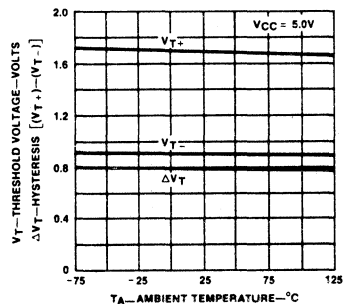
(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
POWER SUPPLY VOLTAGE



(54/74)
HYSTERESIS vs TEMPERATURE



(54LS/74LS)
THRESHOLD VOLTAGE AND
HYSTERESIS vs
AMBIENT TEMPERATURE



GATE

54/74S133

13-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S133	4ns	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S133N	
Plastic SO	N74S133D	
Ceramic DIP		S54S133F
Flatpack		S54S133W

FUNCTION TABLE

INPUTS	OUTPUT
A ... M	\bar{Y}
H ... H one input = L	L H

H = HIGH voltage level
L = LOW voltage level

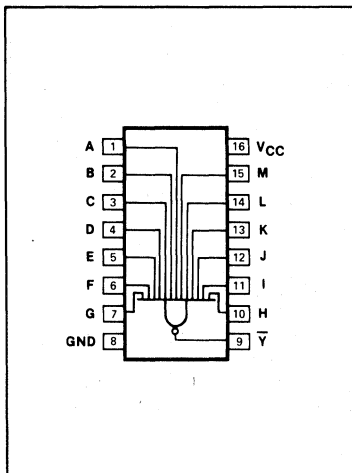
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
\bar{Y}	Output	10Sul

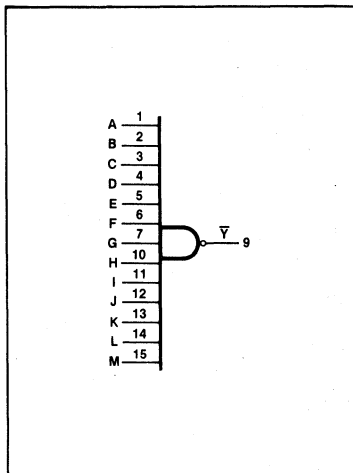
NOTE

A 54/74S unit load (Sul) is understood to be $50\mu A I_{IH}$ and $-2.0mA I_{IL}$.

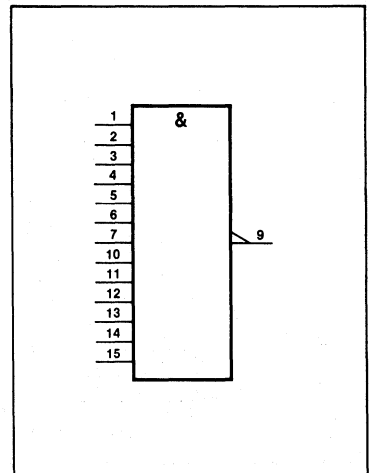
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54S	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

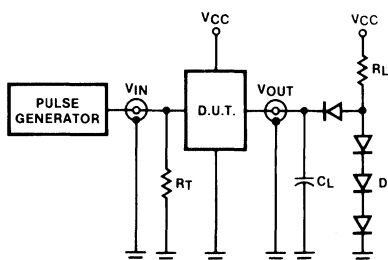
PARAMETER		54/74S			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I _{IK}	Input clamp current				-18	mA
I _{OH}	HIGH-level output current				-1000	μA
I _{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T _A	Operating free-air temperature	Mil	-55		+125	°C
		Com'l	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

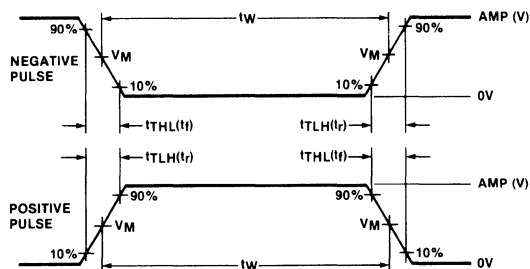
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TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

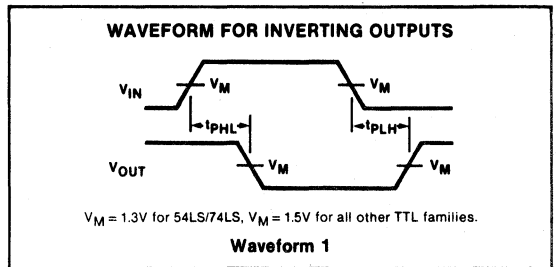
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74S133			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V	
		Com'l	2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX	Mil		0.5 ⁴	V	
		Com'l		0.5	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			- 1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			- 2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	- 40		- 100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		3	5	mA
		I _{CCL} Outputs LOW		5.5	10	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54S/74LS		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		6.0 7.0	ns

GATE

54/74S134

12-Input NAND Gate (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
74S134	5ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S134N	
Plastic SO	N74S134D	

FUNCTION TABLE

INPUTS		OUTPUT
$D_0 \dots D_{11}$	\overline{OE}	\overline{Y}
H ... H	L	L
one input = L	L	H
X ... X	H	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance "off" state

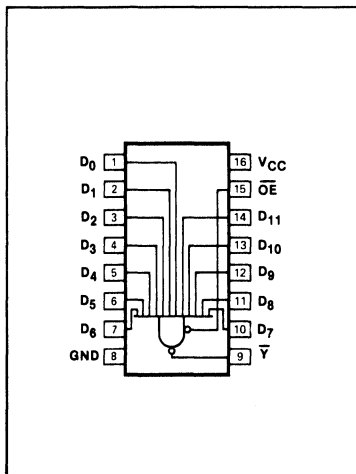
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
\overline{Y}	Output	10Sul

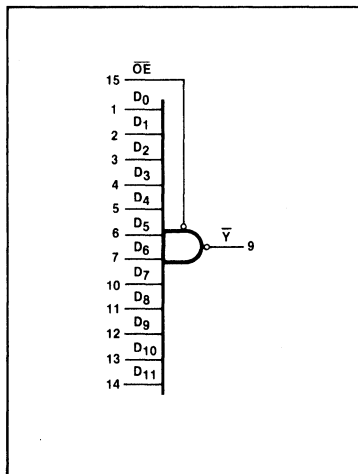
NOTE
 Where a 54/74S unit load (Sul) is understood to be $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .



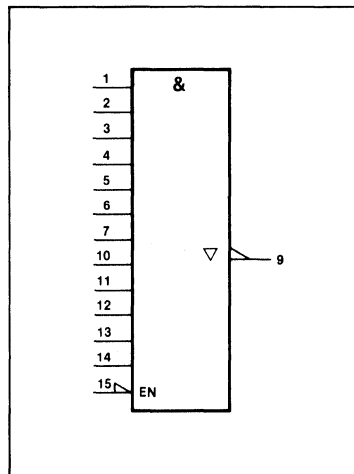
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74S			UNIT		
		Min	Nom	Max			
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	V	
V_{IH}	HIGH-level input voltage	2.0			V		
V_{IL}	LOW-level input voltage	Mil			+0.8	V	
		Com'l			+0.8	V	
I_{IK}	Input clamp current				-18	mA	
I_{OH}	HIGH-level output current	Mil			-2	mA	
		Com'l			-6.5	mA	
I_{OL}	LOW-level output current	Mil			20	mA	
		Com'l			20	mA	
T_A	Operating free-air temperature	Mil	-55			+125	°C
		Com'l	0			70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
 R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1k Ω for 54/74, 54S/74S, R_X = 5k Ω for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

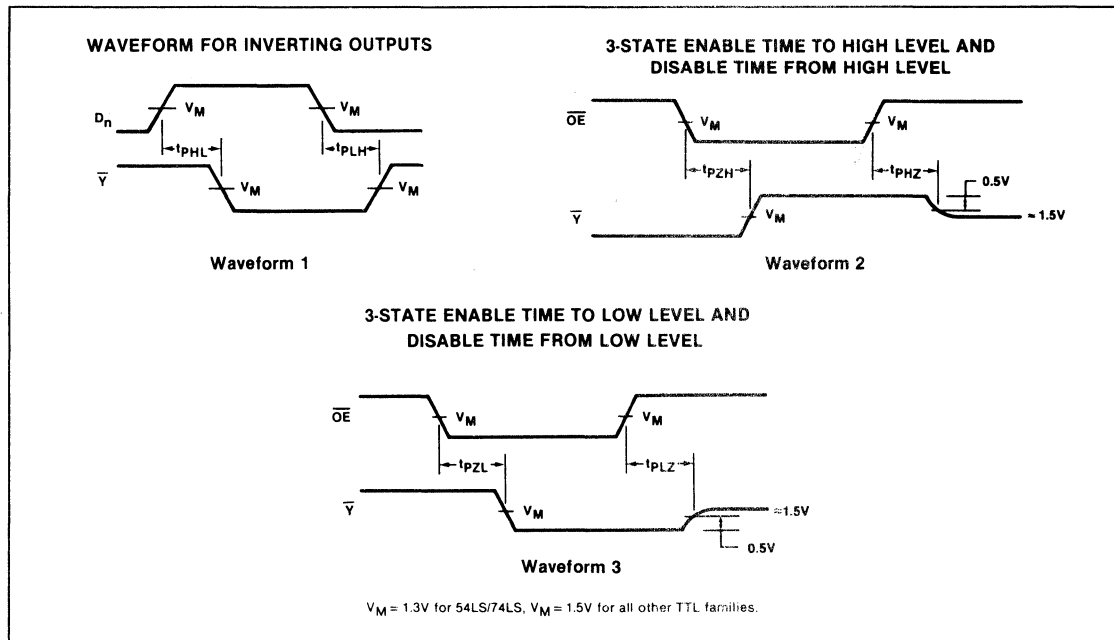
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74S134			UNIT		
		Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OH} = -2mA	Mil	2.4	3.4		V
		I _{OH} = -6.5mA	Com'l	2.4	3.2		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX		Mil			0.5	V
			Com'l				0.5
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.2	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.4V					50	μA
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.5V					-50	μA
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V					1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V					50	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V					-2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX			-40		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CC} H Outputs HIGH			7	13	mA
		I _{CC} L Outputs LOW			9	16	mA
		I _{CC} Z Outputs OFF			14	25	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_O = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



4

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54S/74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	
t_{PLH} Propagation delay	Waveform 1		6.0	ns
t_{PHL} Propagation delay	Waveform 1		7.5	ns
t_{PZH} Enable to HIGH	Waveform 2, $C_L = 50\text{pF}$		19.5	ns
t_{PZL} Enable to LOW	Waveform 3, $C_L = 50\text{pF}$		21	ns
t_{PHZ} Disable from HIGH	Waveform 2, $C_L = 5\text{pF}$		8.5	ns
t_{PLZ} Disable from LOW	Waveform 3, $C_L = 5\text{pF}$		14	ns

Quad Exclusive OR/NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S135	9ns	65mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S135N	
Ceramic DIP		S54S135F
Flatpack		S54S135W

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = HIGH voltage level
 L = LOW voltage level

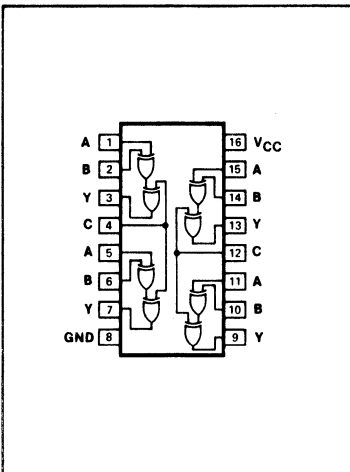
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S
All	Inputs	1Sui
All	Outputs	10Sui

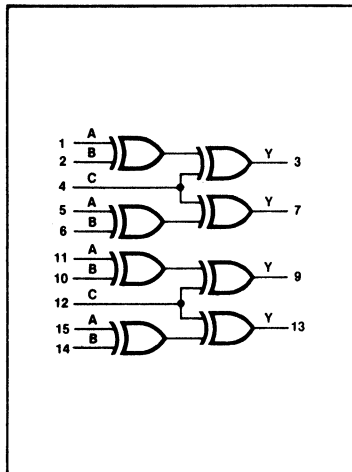
NOTE
 A 54/74S unit load (Sui) is understood to be 50µA I_{IH} and -2.0mA I_{IL} .

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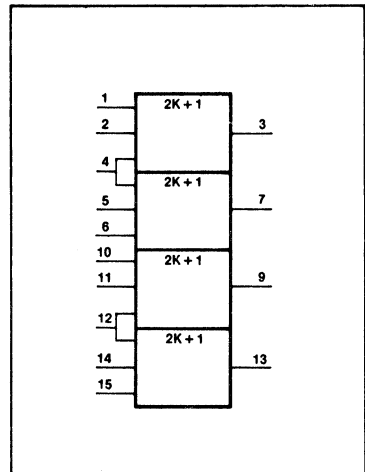
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



GATE

54/74S135

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54S	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I _{IN} Input current	- 30 to + 5	- 30 to + 5	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A Operating free-air temperature range	- 55 to + 125	0 to 70	°C

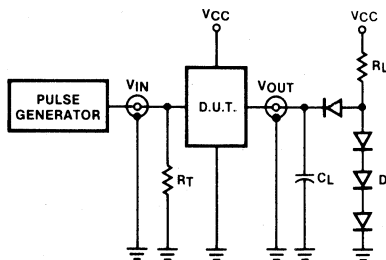
RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74S			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.5	V
	Com'l	4.75	5.25	V
V _{IH} HIGH-level input voltage		2.0		V
V _{IL} LOW-level input voltage	Mil		+ 0.8	V
	Com'l		+ 0.8	V
I _{IK} Input clamp current			- 18	mA
I _{OH} HIGH-level output current			- 1000	μA
I _{OL} LOW-level output current	Mil		20	mA
	Com'l		20	mA
T _A Operating free-air temperature	Mil	- 55	+ 125	°C
	Com'l	0	70	°C

NOTE
V_{IL} = + 0.45V MAX for 54S at T_A = + 125°C only.

TEST CIRCUITS AND WAVEFORMS

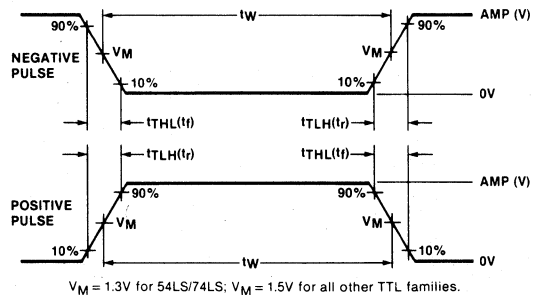
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

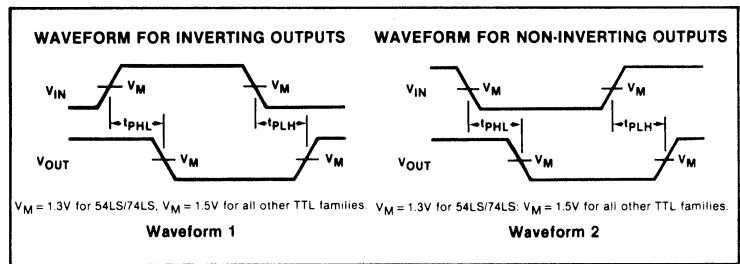
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74S135			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V
		Com'l	2.7	3.4	V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.5 ⁵	V
		Com'l		0.5	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			- 1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			- 2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	- 40		- 100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		65	99	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the inputs grounded and the outputs open.
- V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54S/74S		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
t _{PLH} Propagation delay A or B to output	Waveform 2, C = LOW, B or A = LOW		13	ns
			15	
t _{PLH} Propagation delay A or B to output	Waveform 1, C = LOW, B or A = HIGH		12	ns
			13.5	
t _{PLH} Propagation delay A or B to output	Waveform 1, C = HIGH, B or A = LOW		15	ns
			10	
t _{PLH} Propagation delay A or B to output	Waveform 2, C = HIGH, B or A = HIGH		12	ns
			11	
t _{PLH} Propagation delay C to output	Waveform 2, A = B		12	ns
			14.5	
t _{PLH} Propagation delay C to output	Waveform 1, A ≠ B		11.5	ns
			12	

4

Quad Two-Input Exclusive-OR Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS136	18ns	6.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS136N	
Ceramic DIP		S54LS136F
Flatpack		S54LS136W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

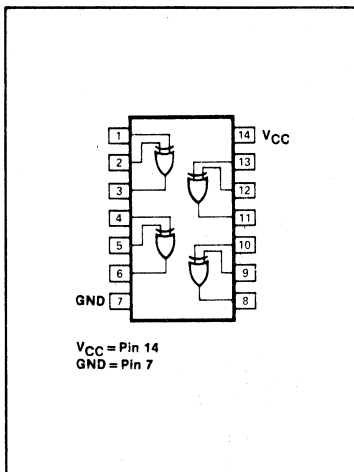
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

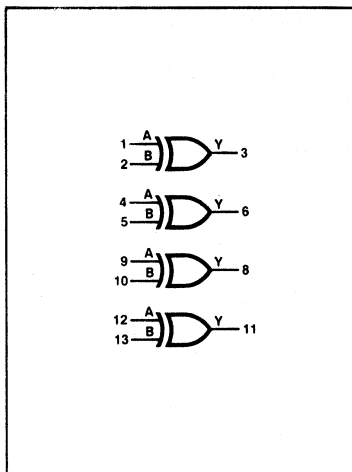
PINS	DESCRIPTION	54/74LS
A, B	Inputs	2LSul
Y	Output	10LSul

NOTE
Where a 54/74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

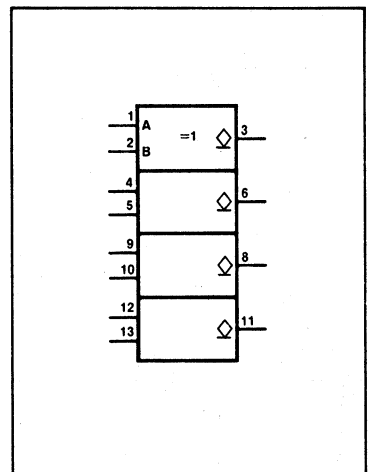
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I_{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

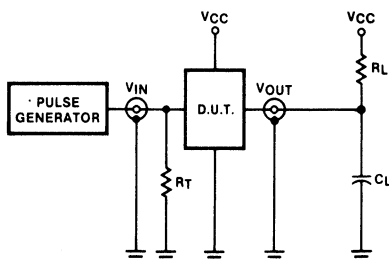
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT		
		Min	Nom	Max			
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	V	
V_{IH}	HIGH-level input voltage	2.0			V		
V_{IL}	LOW-level input voltage	Mil			+ 0.7	V	
		Com'l			+ 0.8	V	
I_{IK}	Input clamp current				- 18	mA	
V_{OH}	HIGH-level output voltage				5.5	V	
I_{OL}	LOW-level output current	Mil			4	mA	
		Com'l			8	mA	
T_A	Operating free-air temperature	Mil	- 55			+ 125	°C
		Com'l	0			70	°C

4

TEST CIRCUITS AND WAVEFORMS

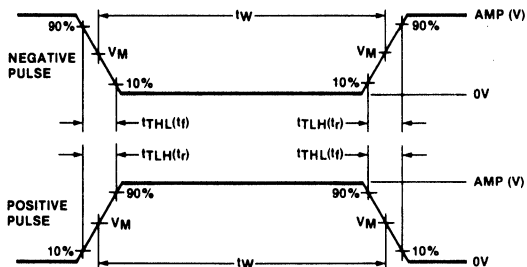
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

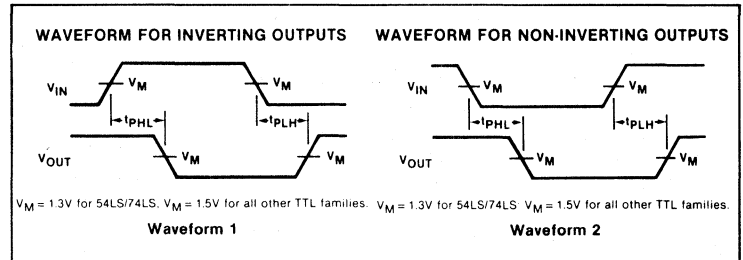
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS136			UNIT	
		Min	Typ ²	Max		
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = \text{MAX}$			100	μA	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			0.2	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			40	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-0.8	mA	
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$		6.1	10	mA	

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
3. I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with one input of each gate at 4.5V, the other inputs grounded, and all outputs open.

AC WAVEFORMS



AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74LS		UNIT
		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		
		Min	Max	
t_{PLH} Propagation delay	Other input LOW Waveform 2		30	ns
t_{PHL} A or B to output			30	
t_{PLH} Propagation delay	Other input HIGH Waveform 1		30	ns
t_{PHL} A or B to output			30	

DECODERS/DEMULTIPLEXERS

54/74LS138, S138

1-Of-8 Decoder/Demultiplexer

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Direct replacement for Intel 3205

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS138	20ns	6.3mA
74S138	7ns	49mA

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\bar{0}$ - $\bar{7}$). The device features three Enable inputs: two active LOW (\bar{E}_1, \bar{E}_2) and one active HIGH (E_3). Every output will be HIGH unless E_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

ORDERING CODE

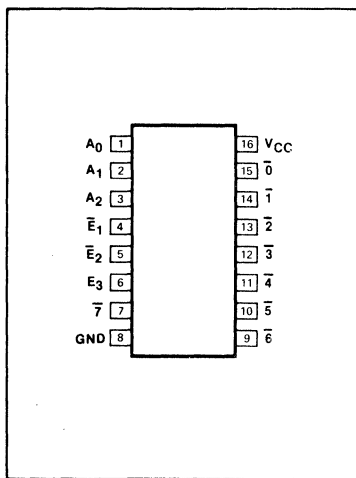
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74S138N • N74LS138N	
Plastic SO	N74LS138D • N74S138D	
Ceramic DIP		S54S138F • S54LS138F
Flatpack		S54S138W • S54LS138W
LLCC		S54LS138G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

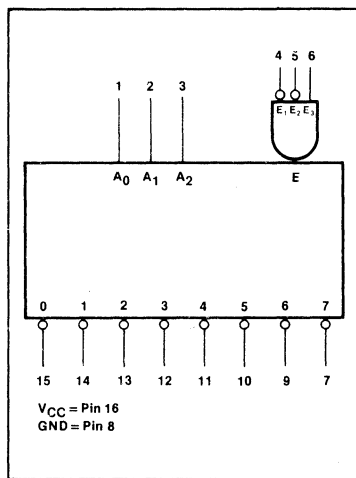
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE
Where a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

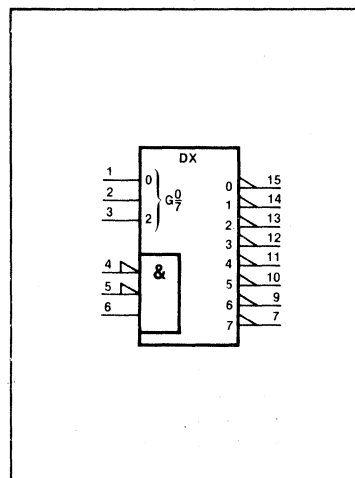
PIN CONFIGURATION



LOGIC SYMBOL



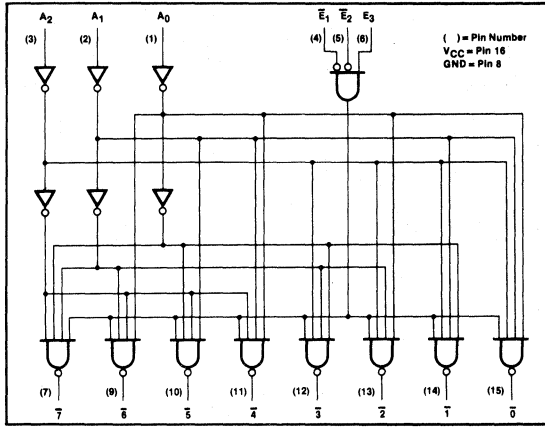
LOGIC SYMBOL (IEEE/IEC)



DECODERS/DEMULTIPLEXERS

54/74LS138, S138

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	0	1	2	3	4	5	6	7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	L	H	H	H	L	H	H	H
L	L	H	H	H	L	L	H	H	H	L	L	H	H
L	L	H	H	L	H	L	H	H	H	L	L	L	H
L	L	H	H	H	H	L	H	H	H	L	L	L	L

NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125			0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-18			-18	mA
I_{OH} HIGH-level output current				-400			-1000	μ A
I_{OL} LOW-level output current	Mil			4			20	mA
	Com'l			8			20	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

NOTE
 $V_{IL} = +0.7V$ MAX for 54S at $T_A = +125^\circ C$ only.

DECODERS/DEMULTIPLEXERS

54/74LS138, S138

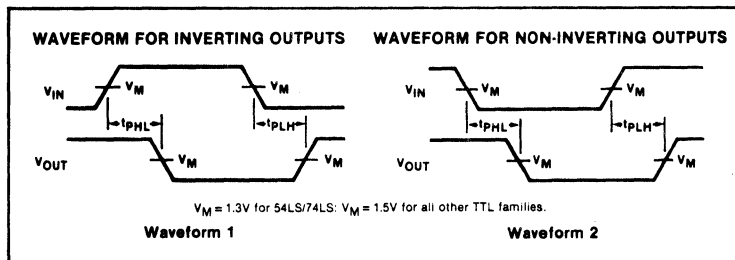
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS138			54/74S138			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		2.5	3.4	V	
		Com'l	2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.25	0.4		0.5 ⁵	V
			Com'l		0.35	0.5		0.5	V
		I _{OL} = 4mA	74LS		0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA	
		V _I = 7.0V			0.1			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-0.4			mA	
		V _I = 0.5V					-2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-20		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		6.3	10		49	74	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- To measure I_{CC}, outputs must be enabled and open.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS

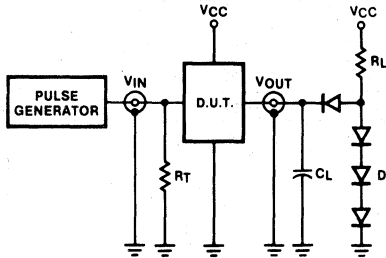


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} Propagation delay	Waveform 2 2 logic levels		20		7	ns
t _{PHL} Address to output			41		10.5	
t _{PLH} Propagation delay	Waveform 1 3 logic levels		27		12	ns
t _{PHL} Address to output			39		12	
t _{PLH} Propagation delay	Waveform 2 2 logic levels		18		8	ns
t _{PHL} Enable to output			32		11	
t _{PLH} Propagation delay	Waveform 1 3 logic levels		26		11	ns
t _{PHL} Enable to output			38		11	

TEST CIRCUITS AND WAVEFORMS

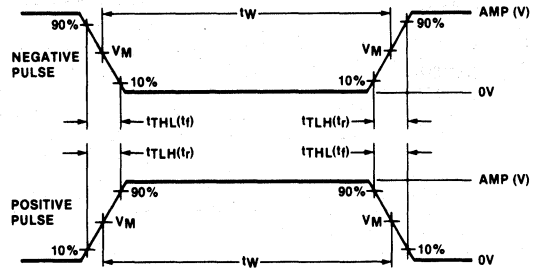
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODERS/DEMULPLEXERS

54/74LS139, S139

Dual 1-of-4 Decoder/Demultiplexer

- Demultiplexing capability
- Two independent 1-of-4 decoders
- Multifunction capability
- Replaces 9321 and 93L21 for higher performance

TYPE	TYPICAL PROPAGATION DELAY (Enable at 2 logic levels)	TYPICAL SUPPLY CURRENT (Total)
74LS139	19ns	6.8mA
74S139	6ns	60mA

DESCRIPTION

The '139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0, A_1) and providing four mutually exclusive active LOW outputs ($\bar{0}$ - $\bar{3}$). Each decoder has an active LOW Enable (\bar{E}). When \bar{E} is HIGH, every output is forced HIGH. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

ORDERING CODE

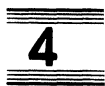
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74S139N • N74LS139N	
Plastic SO	N74LS139D • N74S139D	
Ceramic DIP		S54S139F • S54LS139F
Flatpack		S54S139W • S54LS139W
LLCC		S54LS139G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

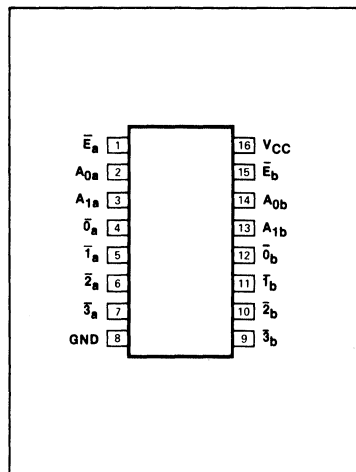
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE

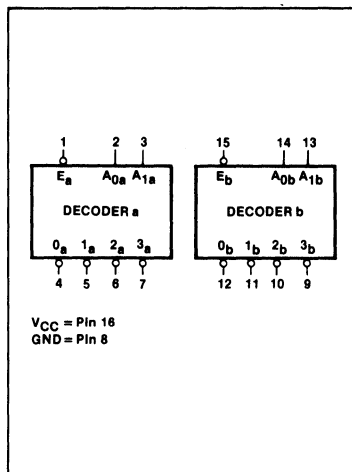
A 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .



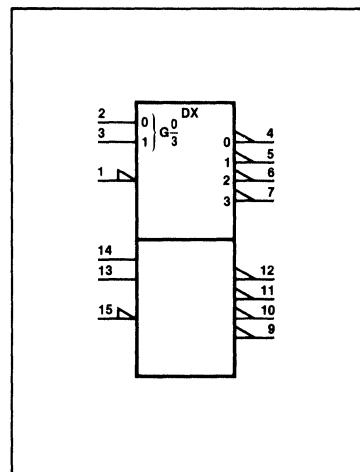
PIN CONFIGURATION



LOGIC SYMBOL



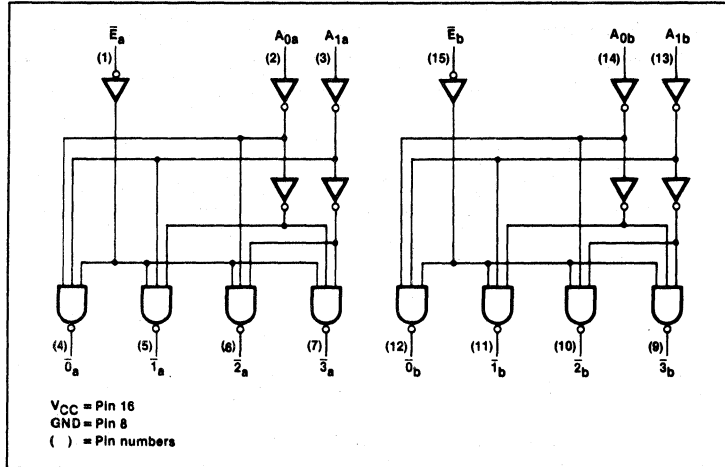
LOGIC SYMBOL (IEEE/IEC)



DECODERS/DEMULTIPLEXERS

54/74LS139, S139

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS			
\bar{E}	A_0	A_1	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	L	H	L	H	H
L	L	H	H	H	L	H
L	L	H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-18			-18	mA
I_{OH} HIGH-level output current				-400			-1000	μ A
I_{OL} LOW-level output current	Mil			4			20	mA
	Com'l			8			20	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

NOTE
 V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DECODERS/DEMULTIPLEXERS

54/74LS139, S139

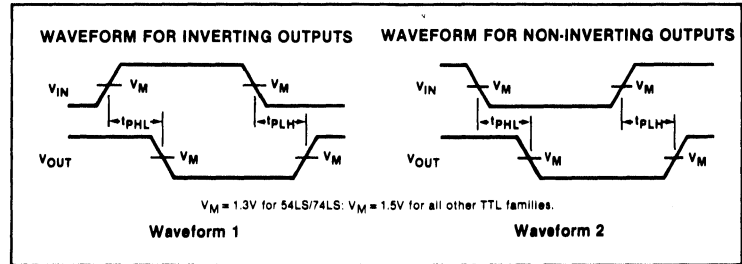
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS139			54/74S139			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		2.5	3.4	V	
		Com'l	2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.25	0.4		0.5 ⁵	V	
			Com'l		0.35	0.5		0.5	V
		I _{OL} = 4mA	74LS		0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA	
		V _I = 7.0V			0.1			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-0.4			mA	
		V _I = 0.5V					-2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-15		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		6.8	11		60	90	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- To measure I_{CC}, outputs must be enabled and open.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74LS		54/74S		UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Waveform 2 Address to output		20 33		7.5 10	ns
t _{PLH} t _{PHL}	Waveform 1 Address to output		29 38		12 12	ns
t _{PLH} t _{PHL}	Waveform 2 Enable to output		24 32		8 10	ns

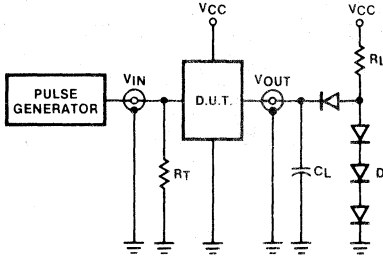


DECODERS/DEMULTIPLEXERS

54/74LS139, S139

TEST CIRCUITS AND WAVEFORMS

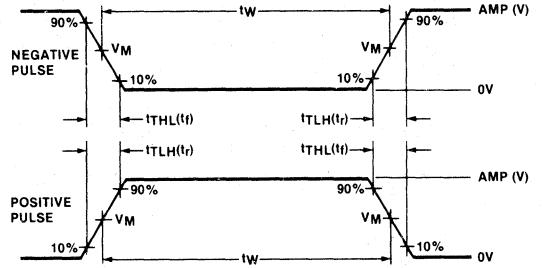
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Dual Four-Input NAND 50-Ohm Line Driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S140	4ns	10mA (I_{CCH}) 25mA (I_{CCL})

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S140N	
Ceramic DIP		S54S140F
Flatpack		S54S140W

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	\bar{Y}
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

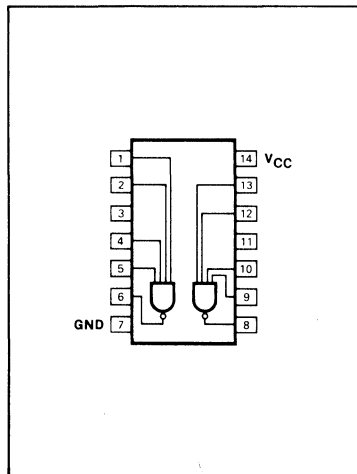
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S
A-D	Inputs	2Sul
\bar{Y}	Output	30Sul

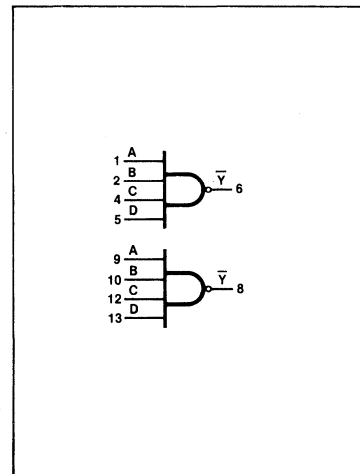
NOTE
Where a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} .



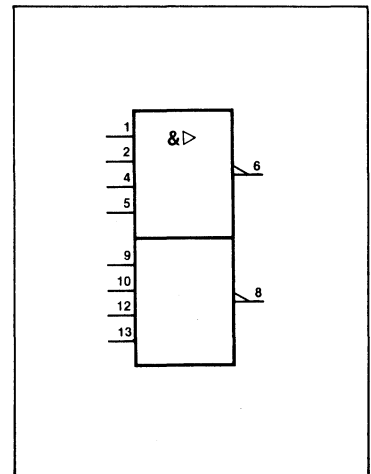
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LINE DRIVER

54/74S140

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I_{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

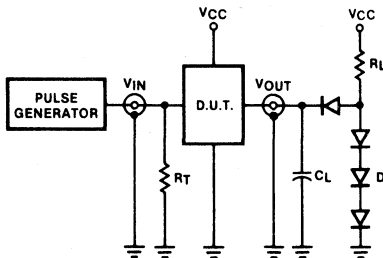
PARAMETER		54/74S			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.5	V
		Com'l	4.75	5.25	V
V_{IH}	HIGH-level input voltage	2.0		V	
V_{IL}	LOW-level input voltage	Mil		+ 0.8	V
		Com'l		+ 0.8	V
I_{IK}	Input clamp current			- 18	mA
I_{OH}	HIGH-level output current			- 40	mA
I_{OL}	LOW-level output current	Mil		60	mA
		Com'l		60	mA
T_A	Operating free-air temperature	Mil	- 55	+ 125	°C
		Com'l	0	70	°C

NOTE

$V_{IL} = + 0.7V$ MAX for 54S at $T_A = + 125^\circ C$ only.

TEST CIRCUITS AND WAVEFORMS

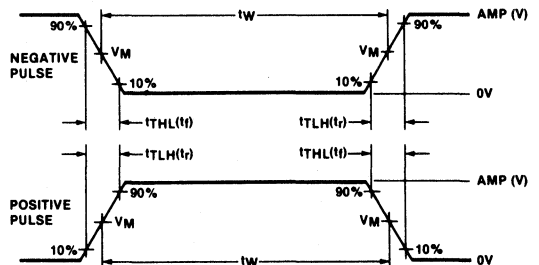
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LINE DRIVER

54/74S140

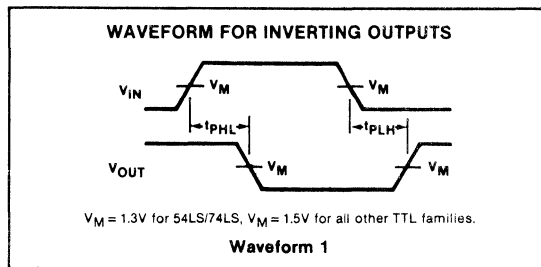
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74S140			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = -3mA	Mil	2.5	3.4	V	
		Com'l	2.7	3.4	V	
	V _{CC} = MIN, V _{IL} = 0.5V, R _O = 50Ω to ground		2.0		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX	Mil		0.5 ⁴	V	
		Com'l		0.5	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			100	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			-4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-50		-225	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		10	18	mA
		I _{CCL} Outputs LOW		25	44	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed 100 milliseconds.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74S		UNIT
		C _L = 50pF, R _L = 93Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1		6.5	ns
			6.5	

4

DECODER/DRIVER

54/74145

BCD-To-Decimal Decoder/Driver (Open Collector)

- 80mA output drive capability
- 15V output breakdown voltage
- See '45 for 30V output voltage
- See '42 for standard TTL outputs

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74145	24ns	43mA

DESCRIPTION

The '145 is a 1-of-10 decoder with Open Collector outputs. This decoder accepts BCD inputs on the A₀ to A₃ address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A₃ used as an active LOW enable.

The '145 features an output breakdown voltage of 15V. This device is ideal as a lamp or solenoid driver.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	MILITARY RANGES V _{CC} = 5V ± 10%; T _A = - 55°C to + 125°C
Plastic DIP	N74145N	
Plastic SO	N74145D	

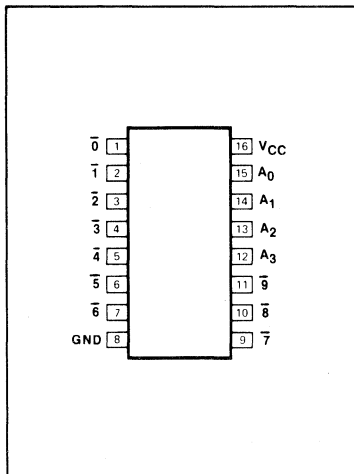
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
All	Inputs	1uI
All	Outputs	12.5uI

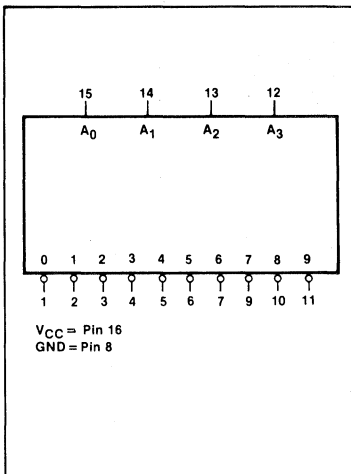
NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and - 1.6mA I_{IL}.

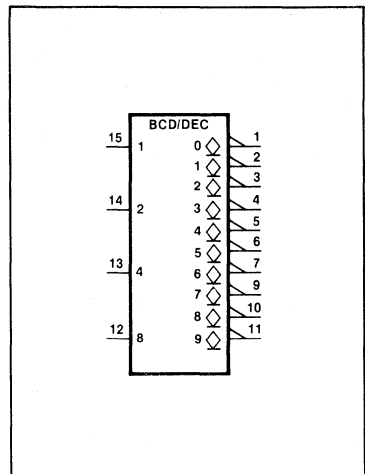
PIN CONFIGURATION



LOGIC SYMBOL



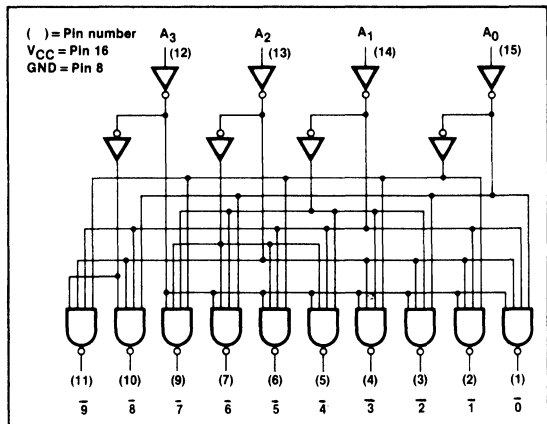
LOGIC SYMBOL (IEEE/IEC)



DECODER/DRIVER

54/74145

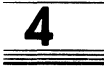
LOGIC DIAGRAM



FUNCTION TABLE

A ₃	A ₂	A ₁	A ₀	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I _{IN} Input current	- 30 to + 5	- 30 to + 5	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to + 15	- 0.5 to + 15	V
T _A Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT
		Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+ 0.8	V
	Com'l			+ 0.8	V
I _{IK} Input clamp current				- 12	mA
V _{OH} HIGH-level output voltage				15	V
I _{OL} LOW-level output current	Mil			80	mA
	Com'l			80	mA
T _A Operating free-air temperature	Mil	- 55		+ 125	°C
	Com'l	0		70	°C

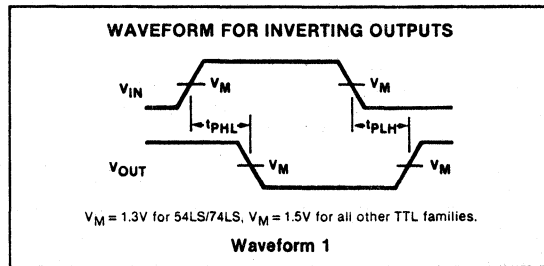
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74145			UNIT
		Min	Typ ²	Max	
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = \text{MAX}$			250	μA
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = 80\text{mA}$	0.5	0.9	V
		$I_{OL} = 20\text{mA}$		0.4	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6	mA
I_{CC} Supply current ³ (total)	$V_{CC} = \text{MAX}$	Mil	43	62	mA
		Com'l	43	70	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- Measure I_{CC} with all inputs grounded and outputs open.

AC WAVEFORMS

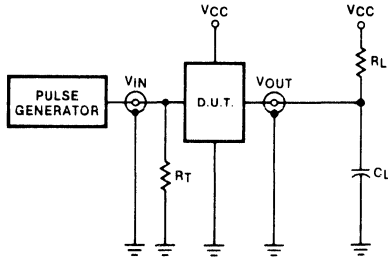


AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		$C_L = 15\text{pF}, R_L = 100\Omega$		
		Min	Max	
t_{PLH} Propagation delay	Waveform 1		50	ns
t_{PHL} Address to output			50	

TEST CIRCUITS AND WAVEFORMS

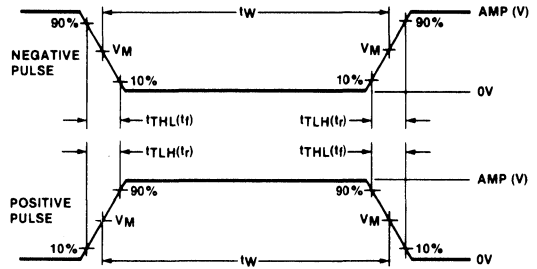
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

ENCODER

54/74147

10-Line-To-4-Line Priority Encoder

- Encodes 10-line decimal to 4-line BCD
- Useful for 10-position switch encoding
- Used in code converters and generators

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74147	10ns	46mA

DESCRIPTION

The '147 9-input priority encoder accepts data from nine active-LOW inputs (\bar{I}_1 - \bar{I}_9) and provides a binary representation on the four active-LOW outputs (\bar{A}_0 - \bar{A}_3). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line \bar{I}_9 having the highest priority.

The device provides the 10-line-to-4-line priority encoding function by use of the implied decimal "zero." The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74147N	
Ceramic DIP		S54147F
Flatpack		S54147W

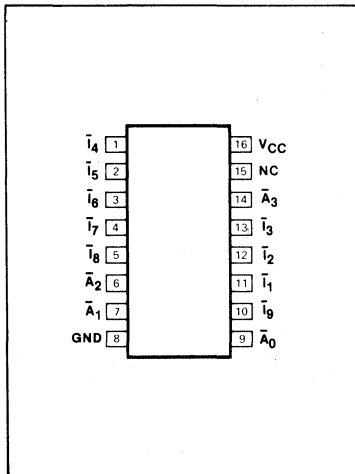
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
All	Inputs	1ul
All	Outputs	10ul

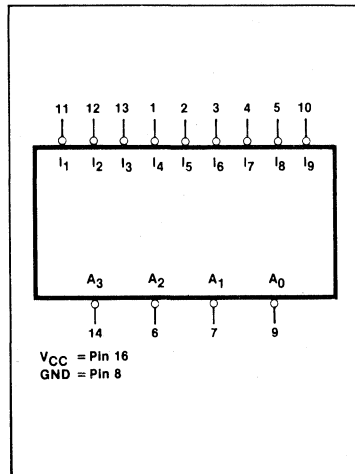
NOTE

A 54/74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

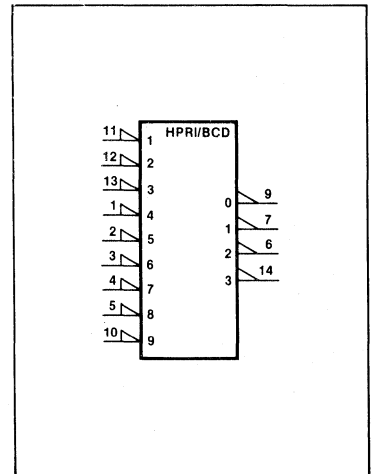
PIN CONFIGURATION



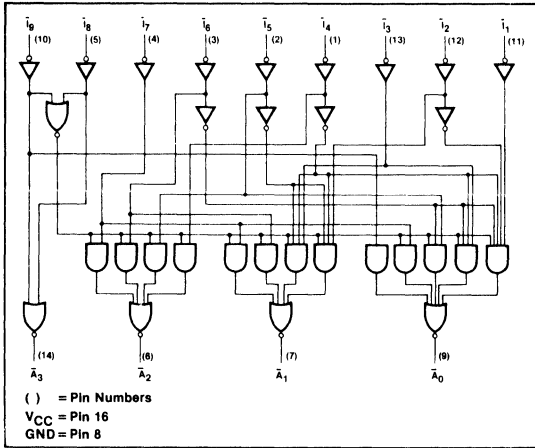
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS										OUTPUTS			
\bar{i}_1	\bar{i}_2	\bar{i}_3	\bar{i}_4	\bar{i}_5	\bar{i}_6	\bar{i}_7	\bar{i}_8	\bar{i}_9	\bar{i}_{10}	\bar{A}_3	\bar{A}_2	\bar{A}_1	\bar{A}_0
H	H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	L	L	L	L
X	X	X	X	X	X	X	L	H	H	H	H	H	H
X	X	X	X	X	L	H	H	H	H	H	L	L	L
X	X	X	X	L	H	H	H	H	H	H	L	L	L
X	X	L	H	H	H	H	H	H	H	H	L	L	L
X	L	H	H	H	H	H	H	H	H	H	L	L	L
L	H	H	H	H	H	H	H	H	H	H	H	L	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to +5.5	- 0.5 to +5.5	V
I _{IN} Input current	- 30 to +5	- 30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to +V _{CC}	- 0.5 to +V _{CC}	V
T _A Operating free-air temperature range	- 55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT
		Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+ 0.8	V
	Com'l			+ 0.8	V
I _{IK} Input clamp current				- 12	mA
I _{OH} HIGH-level output current				- 800	μA
I _{OL} LOW-level output current	Mil			16	mA
	Com'l			16	mA
T _A Operating free-air temperature	Mil	- 55		+ 125	°C
	Com'l	0		70	°C

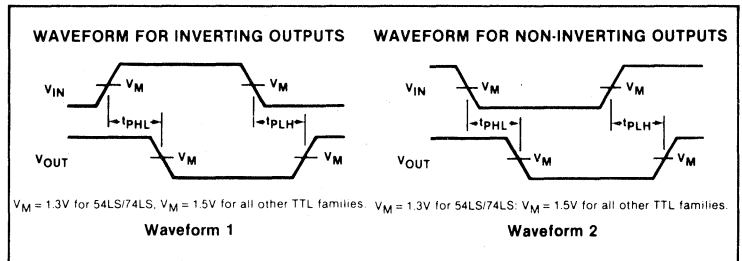
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74147			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.3	V	
		Com'l	2.4	3.3	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			40	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-35	-85	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		50	70	mA
		Condition 2		42	62	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Condition 1: Measure I_{CC} with T₇ grounded, other inputs and outputs open. Condition 2: Measure I_{CC} with all inputs and outputs open.

AC WAVEFORMS

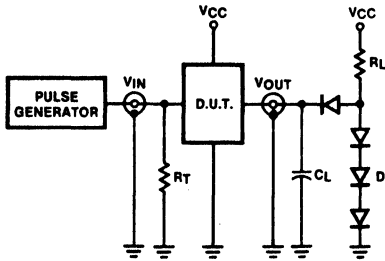


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1 Out-of-phase output		19	ns
			19	
t _{PLH} t _{PHL} Propagation delay	Waveform 2 In-phase output		14	ns
			11	

TEST CIRCUITS AND WAVEFORMS

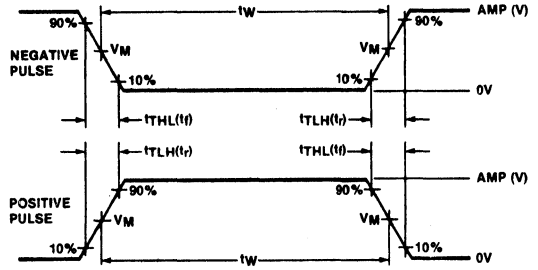
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

ENCODER

54/74148

8-Input Priority Encoder

- Code conversions
- Multi-channel D/A converter
- Decimal-to-BCD converter
- Cascading for priority encoding of "N" bits
- Input Enable capability
- Priority encoding—automatic selection of highest priority input line
- Output Enable—active LOW when all inputs HIGH
- Group Signal output—active when any input is LOW

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74148	10ns	38mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74148N	
Plastic SO		
Ceramic DIP		S54148F
Flatpack		S54148W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
\bar{I}_0	Input	1ul
$\bar{I}_1 - \bar{I}_7$	Inputs	2ul
\bar{EI}	Input	2ul
All	Outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

DESCRIPTION

The '148 8-input priority encoder accepts data from eight active-LOW inputs and provides a binary representation on the three active-LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line \bar{I}_7 having the highest priority.

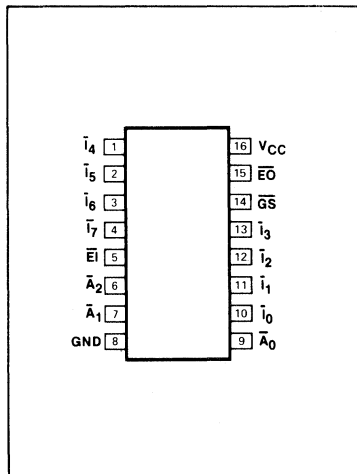
A HIGH on the Enable Input (\bar{EI}) will force all outputs to the inactive (HIGH) state and

allow new data to settle without producing erroneous information at the outputs.

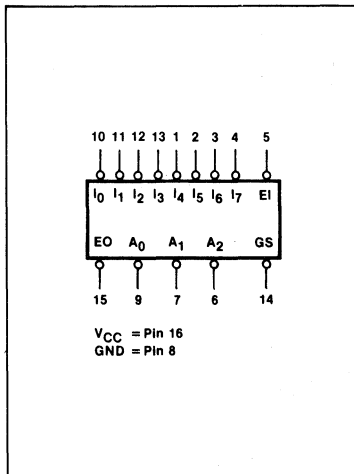
A Group Signal (\bar{GS}) output and an Enable Output (\bar{EO}) are provided with the three data outputs. The \bar{GS} is active-LOW when

any input is LOW; this indicates when any input is active. The \bar{EO} is active-LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both \bar{EO} and \bar{GS} are active-HIGH when the Enable Input is HIGH.

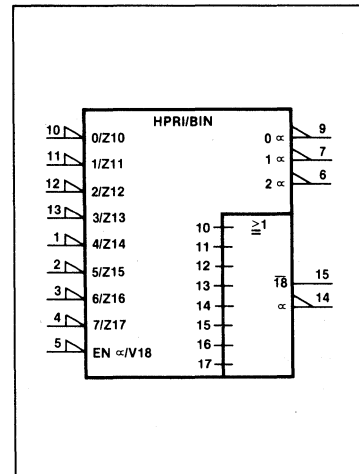
PIN CONFIGURATION



LOGIC SYMBOL



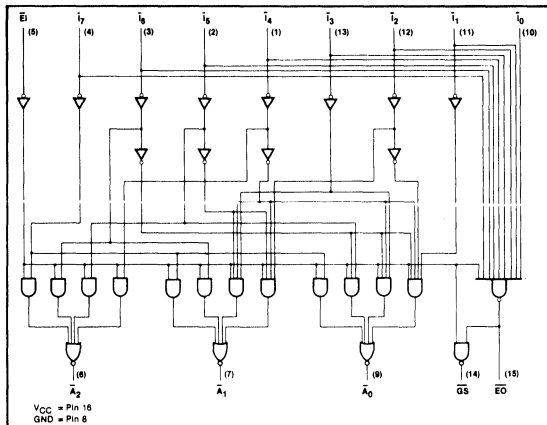
LOGIC SYMBOL (IEEE/IEC)



ENCODER

54/74148

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS								OUTPUTS					
$\bar{E}1$	\bar{I}_0	\bar{I}_1	\bar{I}_2	\bar{I}_3	\bar{I}_4	\bar{I}_5	\bar{I}_6	\bar{I}_7	GS	\bar{A}_0	\bar{A}_1	\bar{A}_2	$\bar{E}0$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	L	L	L	L	L
L	X	X	X	X	X	X	X	L	L	L	L	L	L
L	X	X	X	X	X	X	L	H	L	L	L	L	H
L	X	X	X	X	X	L	H	H	L	L	L	L	H
L	X	X	X	X	L	H	H	H	L	L	L	L	H
L	X	X	L	H	H	H	H	H	L	L	L	L	H
L	X	L	H	H	H	H	H	H	L	L	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

4

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT
		Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8	V
	Com'l			+0.8	V
I _{IK} Input clamp current				-12	mA
I _{OH} HIGH-level output current				-800	μA
I _{OL} LOW-level output current	Mil			16	mA
	Com'l			16	mA
T _A Operating free-air temperature	Mil	-55		+125	°C
	Com'l	0		70	°C

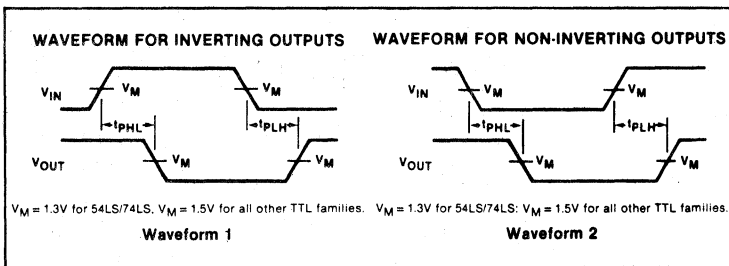
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74148			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.3	V	
		Com'l	2.4	3.3	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	T ₀ input		40	μA	
		Other inputs		80	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	T ₀ input		-1.6	mA	
		Other inputs		-3.2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-35		-85	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		40	60	mA
		Condition 2		35	55	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Condition 1: Measure I_{CC} with T₀ and E_I grounded, other inputs and outputs open. Condition 2: Measure I_{CC} with all inputs and outputs open.

AC WAVEFORMS

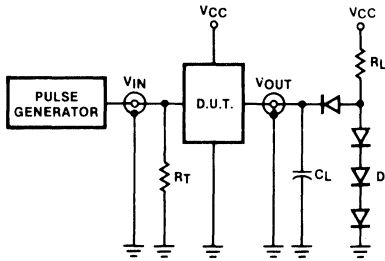


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} Propagation delay t _{PHL} T _n input to A _n outputs	Waveform 2, In-phase output		15 14	ns
t _{PLH} Propagation delay t _{PHL} T _n input to A _n outputs	Waveform 1, Out-of-phase output		19 19	ns
t _{PLH} Propagation delay t _{PHL} T _N input to E _O output	Waveform 1, Out-of-phase output		10 25	ns
t _{PLH} Propagation delay t _{PHL} T _n input to G _S output	Waveform 2, In-phase output		30 25	ns
t _{PLH} Propagation delay t _{PHL} E _I input to A _n outputs	Waveform 2, In-phase output		15 15	ns
t _{PLH} Propagation delay t _{PHL} E _I input to E _O output	Waveform 2, In-phase output		15 30	ns
t _{PLH} Propagation delay t _{PHL} E _I input to G _S output	Waveform 2, In-phase output		12 15	ns

TEST CIRCUITS AND WAVEFORMS

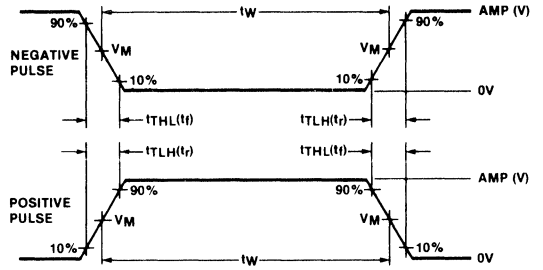
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIPLEXER

54/74150

16-Input Multiplexer

- Select data from 16 sources
- Demultiplexing capability
- Active-LOW enable or strobe
- Inverting data output

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74150	17ns	40mA

DESCRIPTION

The '150 is a logical implementation of a single-pole, 16-position switch with the switch position controlled by the state of four Select inputs, S_0, S_1, S_2, S_3 . The Multiplexer output (\bar{Y}) inverts the selected data. The Enable input (\bar{E}) is active-LOW. When \bar{E} is HIGH the \bar{Y} output is HIGH regardless of all other inputs. In one package the '150 provides the ability to select from 16 sources of data or control information.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74150N	

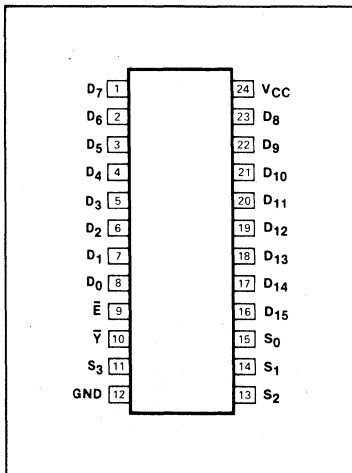
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
All	Inputs	1ul
\bar{Y}	Output	10ul

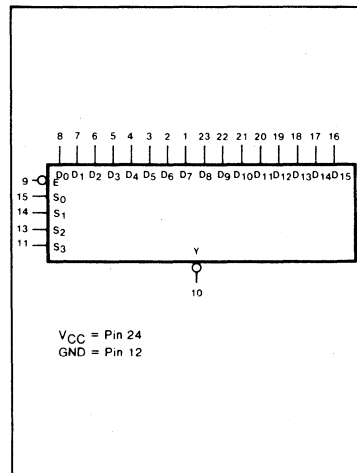
NOTE

A 54/74 unit load (ul) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} .

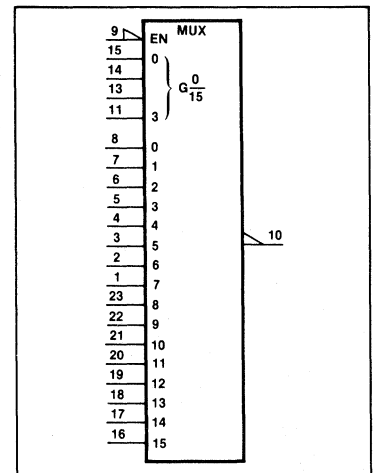
PIN CONFIGURATION



LOGIC SYMBOL



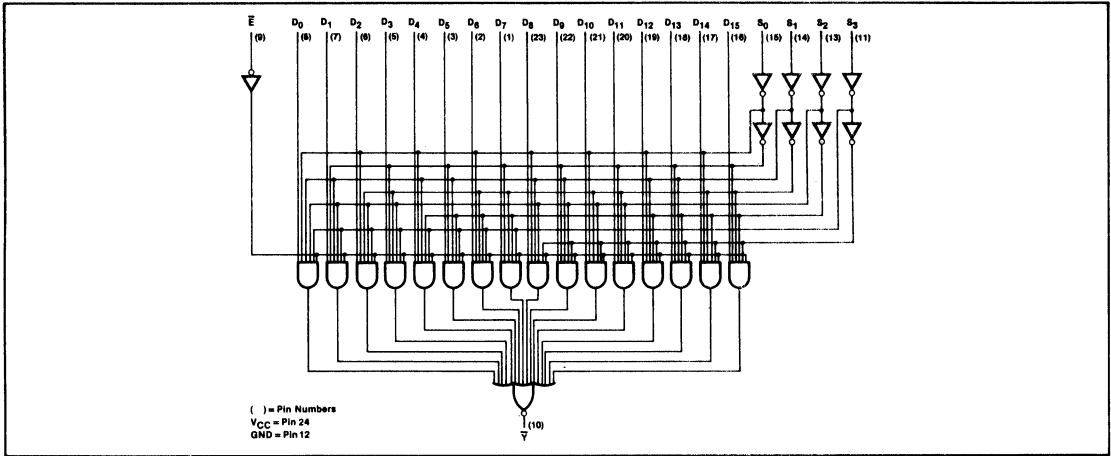
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER

54/74150

LOGIC DIAGRAM



4

FUNCTION TABLE

				INPUTS																OUTPUT	
S ₃	S ₂	S ₁	S ₀	\bar{E}	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇	D ₈	D ₉	D ₁₀	D ₁₁	D ₁₂	D ₁₃	D ₁₄	D ₁₅	\bar{Y}
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

MULTIPLEXER

54/74150

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I_{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage	Mil		+ 0.8	V	
		Com'l		+ 0.8	V	
I_{IK}	Input clamp current			- 12	mA	
I_{OH}	HIGH-level output current			- 800	μ A	
I_{OL}	LOW-level output current	Mil		16	mA	
		Com'l		16	mA	
T_A	Operating free-air temperature	Mil	- 55	+ 125	°C	
		Com'l	0	70	°C	

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74150			UNIT	
		Min	Typ ²	Max		
V_{OH}	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	Mil	2.4	3.4	V	
		Com'l	2.4	3.4	V	
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = \text{MAX}$	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V_{IK}	$V_{CC} = \text{MIN}, I_I = I_{IK}$			- 1.5	V	
I_I	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH}	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40 ³	μ A	
I_{IL}	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			- 1.6	mA	
I_{OS}	Short-circuit output current ³	Mil	- 20	- 55	mA	
		Com'l	- 18	- 55	mA	
I_{CC}	Supply current ⁴ (total)			40	68	mA

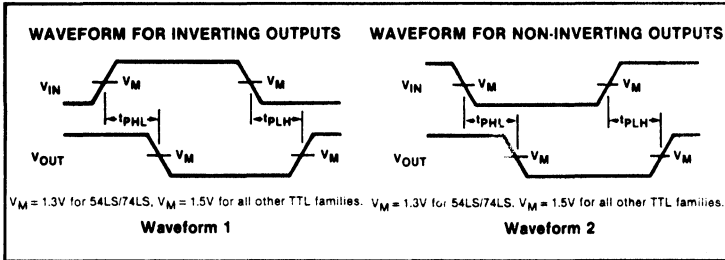
NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC\text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with E, S₀-S₃ inputs at 4.5V, all other inputs and outputs open.

MULTIPLEXER

54/74150

AC WAVEFORMS

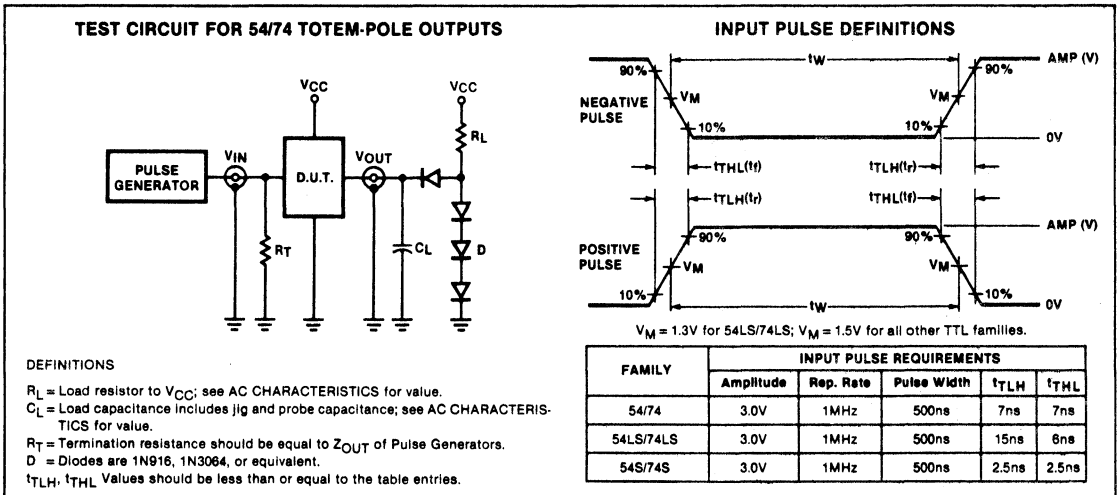


AC CHARACTERISTICS $T_A = 25^\circ C, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		$C_L = 15pF, R_L = 400\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to \bar{Y} output	Waveform 1	35 33	ns
t_{PLH} t_{PHL}	Propagation delay Enable to \bar{Y} output	Waveform 2	24 30	ns
t_{PLH} t_{PHL}	Propagation delay Data to \bar{Y} output	Waveform 1	14 20	ns

4

TEST CIRCUITS AND WAVEFORMS



MULTIPLEXERS

54/74151, LS151, S151

8-Input Multiplexer

- **Multifunction capability**
- **Complementary outputs**
- **See '251 for 3-state version**

TYPE	TYPICAL PROPAGATION DELAY (Enable to \bar{Y})	TYPICAL SUPPLY CURRENT (Total)
74151	18ns	29mA
74LS151	12ns	6mA
74S151	9ns	45mA

DESCRIPTION

The '151 is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2 . True (Y) and Complement (\bar{Y}) outputs are both provided. The Enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, the \bar{Y} output is HIGH and the Y output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Y = \bar{E} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

In one package the '151 provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74151N • N74LS151N N74S151N	
Plastic SO	N74LS151D • N74S151D	
Ceramic DIP		S54151F • S54LS151F S54S151F
Flatpack		S54151W • S54LS151W S54S151W

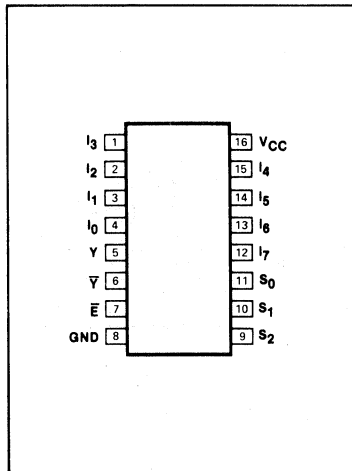
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1uI	1SuI	1LSuI
All	Outputs	10uI	10SuI	10LSuI

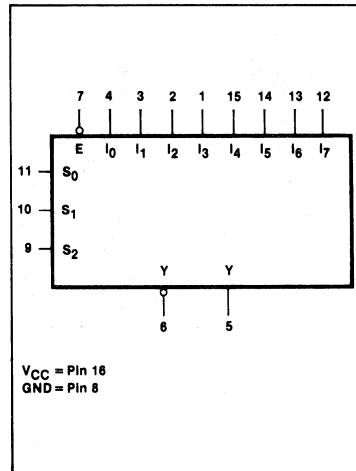
NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , and a 54/74S unit load (SuI) is 50 μ A I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and -0.4mA I_{IL} .

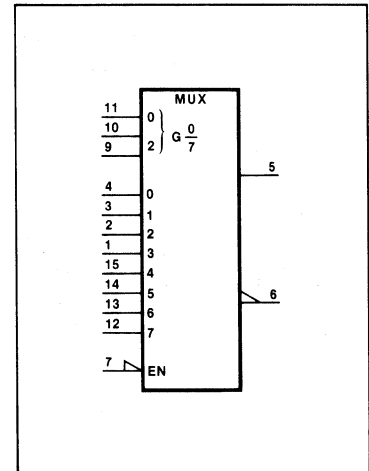
PIN CONFIGURATION



LOGIC SYMBOL



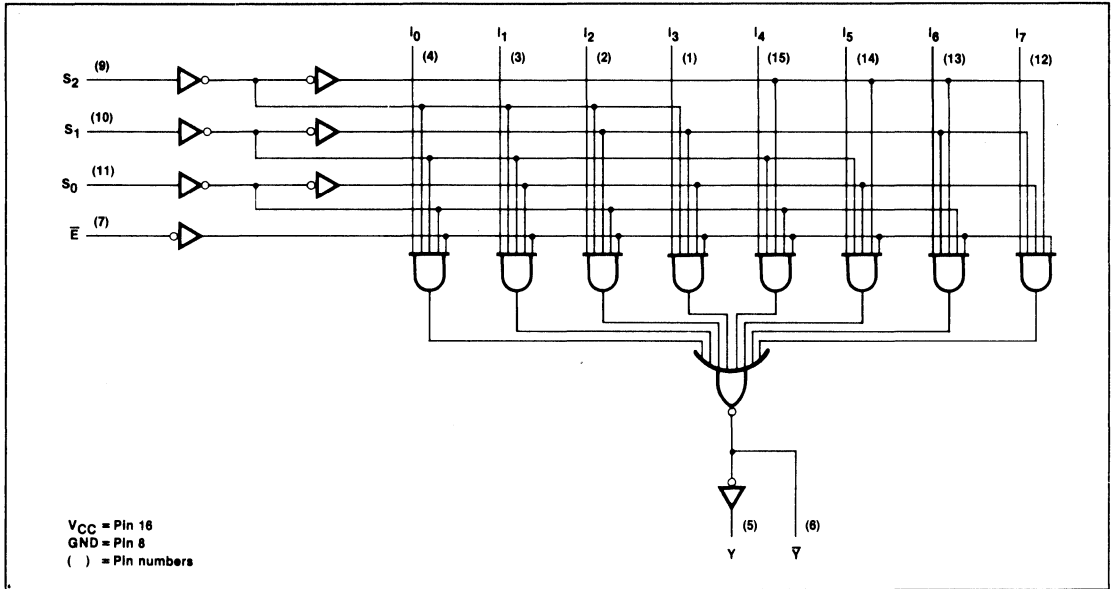
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXERS

54/74151, LS151, S151

LOGIC DIAGRAM



4

FUNCTION TABLES

INPUTS													OUTPUTS	
\bar{E}	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	\bar{Y}	Y	
H	X	X	X	X	X	X	X	X	X	X	X	H	L	
L	L	L	L	L	X	X	X	X	X	X	X	H	L	
L	L	L	L	H	X	X	X	X	X	X	X	L	H	
L	L	L	H	X	L	X	X	X	X	X	X	H	L	
L	L	L	H	X	H	X	X	X	X	X	X	L	H	
L	L	H	L	X	X	L	X	X	X	X	X	H	L	
L	L	H	L	X	X	H	X	X	X	X	X	L	H	
L	L	H	H	X	X	X	L	X	X	X	X	H	L	
L	L	H	H	X	X	X	H	X	X	X	X	L	H	
L	H	L	L	X	X	X	X	L	X	X	X	H	L	
L	H	L	L	X	X	X	X	H	X	X	X	L	H	
L	H	L	H	X	X	X	X	L	X	X	X	H	L	
L	H	L	H	X	X	X	X	H	X	X	X	L	H	
L	H	H	L	X	X	X	X	X	X	L	X	H	L	
L	H	H	L	X	X	X	X	X	X	H	X	L	H	
L	H	H	H	X	X	X	X	X	X	X	L	H	L	
L	H	H	H	X	X	X	X	X	X	X	H	L	H	

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

MULTIPLEXERS

54/74151, LS151, S151

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

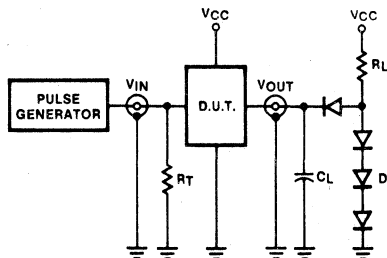
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-800			-400			-1000	µA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX FOR 54S at T_A = +125°C only.

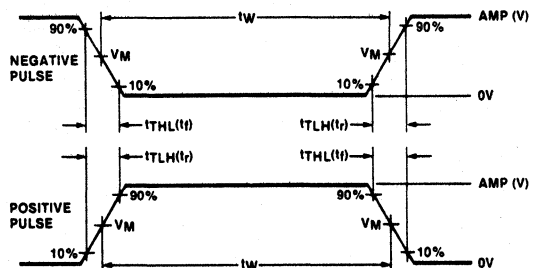
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS
 R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIPLEXERS

54/74151, LS151, S151

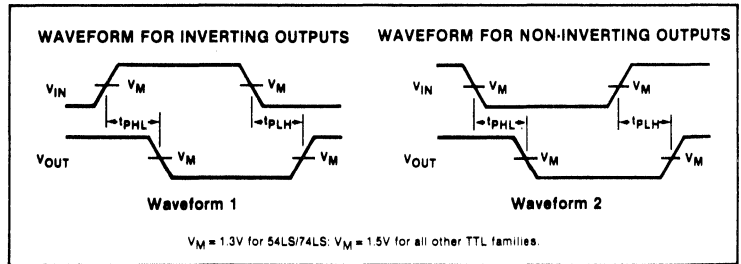
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74151			54/74LS151			54/74S151			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁵	V
			Com'l			0.2	0.4		0.35	0.5		0.5
		I _{OL} = 4mA	74LS					0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA
		V _I = 7.0V						0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40							μA
		V _I = 2.7V						20			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4				mA
		V _I = 0.5V									-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40		-100	mA
		Com'l	-18		-55	-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		29	48		6	10		45	70	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} on the 54/74151 with E and S₀-S₂ at 4.5V, all other inputs and outputs open. Measure I_{CC} on the 54/74LS151 and 54/74S151 with all inputs at 4.5V and outputs open.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay Select to Y output	Waveform 2		52		43		18	ns
t _{PHL}		30		30		18		
t _{PLH} Propagation delay Select to \bar{Y} output	Waveform 1		35		23		15	ns
t _{PHL}		33		32		13.5		
t _{PLH} Propagation delay Enable to Y output	Waveform 1		52		42		16.5	ns
t _{PHL}		30		32		18		
t _{PLH} Propagation delay Enable to \bar{Y} output	Waveform 2		24		24		13	ns
t _{PHL}		30		30		12		
t _{PLH} Propagation delay Data to Y output	Waveform 2		29		32		12	ns
t _{PHL}		24		26		12		
t _{PLH} Propagation delay Data to \bar{Y} output	Waveform 1		20		21		7.0	ns
t _{PHL}		14		20		7.0		

MULTIPLEXERS

54/74153, LS153, S153

Dual 4-Line To 1-Line Multiplexer

- **Non-inverting outputs**
- **Separate Enable for each section**
- **Common Select inputs**
- **See '253 for 3-State version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74153	18ns	36mA
74LS153	18ns	6.2mA
74S153	9ns	45mA

DESCRIPTION

The '153 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables (\bar{E}_a, \bar{E}_b) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced LOW when the corresponding Enables (\bar{E}_a, \bar{E}_b) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Y_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The '153 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74153N • N74LS153N N74S153N	
Plastic SO	N74LS153D • N74S153D	
Ceramic DIP		S54153F • S54LS153F S54S153F
Flatpack		S54153W • S54LS153W S54S153W
LLCC		S54S153G • S54LS153G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

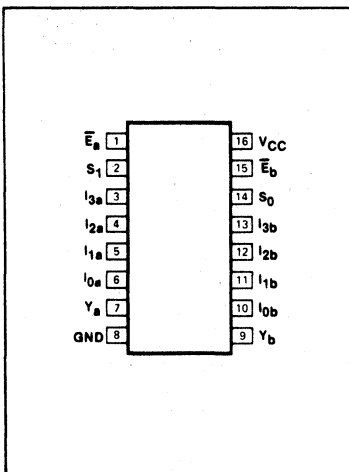
PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1uI	1Sul	1LSul
All	Outputs	10uI	10Sul	10LSul

NOTE
Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50µA I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL} .

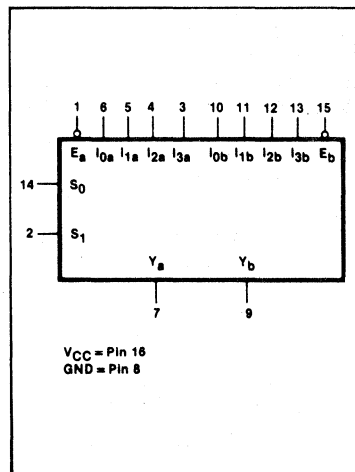
determine the particular register from which the data came. An alternative application is as a function generator. The de-

vice can generate two functions or three variables. This is useful for implementing highly irregular random logic.

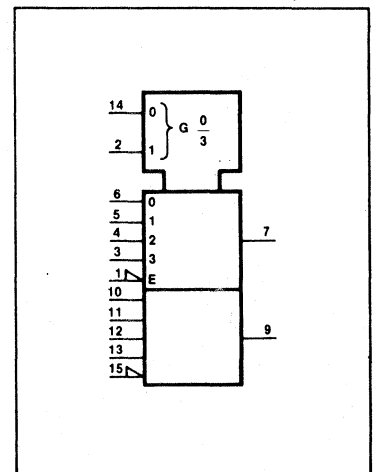
PIN CONFIGURATION



LOGIC SYMBOL



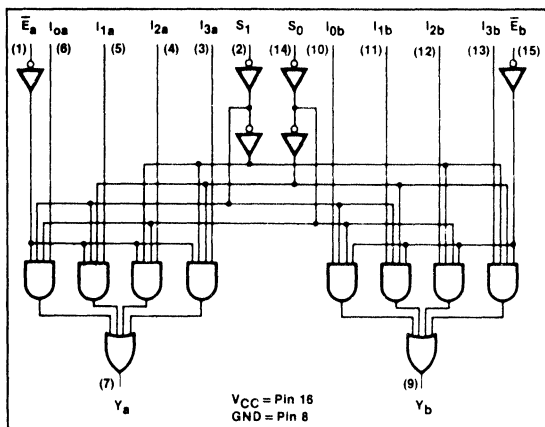
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXERS

54/74153, LS153, S153

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S ₀	S ₁	\bar{E}	I ₀	I ₁	I ₂	I ₃	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74			54/74LS			54/74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage	2.0			2.0			2.0			V	
V _{IL} LOW-level input voltage	Mil	+0.8			+0.7			+0.8			V
	Com'l	+0.8			+0.8			+0.8			V
I _{IK} Input clamp current	-12			-18			-18			mA	
I _{OH} HIGH-level output current	-800			-400			-1000			μA	
I _{OL} LOW-level output current	Mil	16			4			20			mA
	Com'l	16			8			20			mA
T _A Operating free-air temperature	Mil	-55	+125	-55	+125	-55	+125	-55	+125	°C	
	Com'l	0	70	0	70	0	70	0	70	°C	

NOTE
 V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

MULTIPLEXERS

54/74153, LS153, S153

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74153			54/74LS153			54/74S153			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4		0.5 ⁵	V	
		Com'l		0.2	0.4		0.35	0.5		0.5	V	
							0.25	0.4			V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA	
		V _I = 7.0V					0.1				mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA	
		V _I = 2.7V					20			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA	
		V _I = 0.5V								-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-20		-100	-40		-100	mA
		Com'l	-18		-57	-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		36	52		6.2	10		45	70	mA
		Com'l		36	60		6.2	10		45	70	mA

NOTES

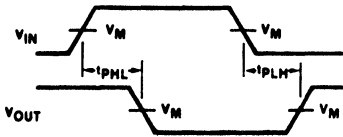
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all inputs grounded and all outputs open.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C _L = 30pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t _{PLH} Propagation delay Select to output	Waveform 2		34		29		18	ns
t _{PHL} Enable to output			34		38		18	
t _{PLH} Propagation delay Enable to output	Waveform 1		30		24		15	ns
t _{PHL} Data to output			23		32		13.5	
t _{PLH} Propagation delay Data to output	Waveform 2		18		15		9.0	ns
t _{PHL} Select to output			23		26		9.0	

AC WAVEFORMS

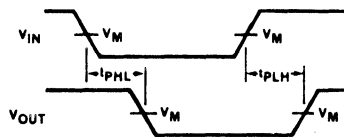
WAVEFORM FOR INVERTING OUTPUTS



$V_M = 1.3V$ for 54LS/74LS, $V_M = 1.5V$ for all other TTL families.

Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS

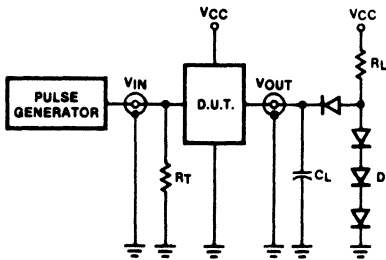


$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

Waveform 2

TEST CIRCUITS AND WAVEFORMS

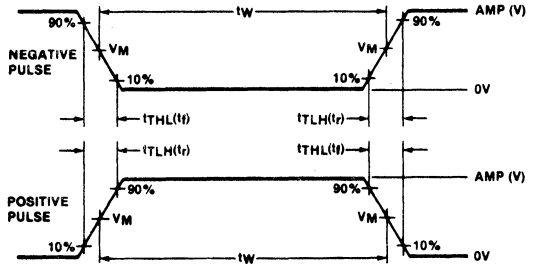
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODER/DEMULTIPLEXERS

54/74154, LS154

1-of-16 Decoder/Demultiplexer

- 16-line demultiplexing capability
- Mutually exclusive outputs
- 2-input enable gate for strobing or expansion

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74154	21ns	34mA
74LS154	15ns	9mA

DESCRIPTION

The '154 decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The '154 can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74154N • N74LS154N	
Ceramic DIP		S54154F • S54LS154F
Flatpack		S54154W • S54LS154W

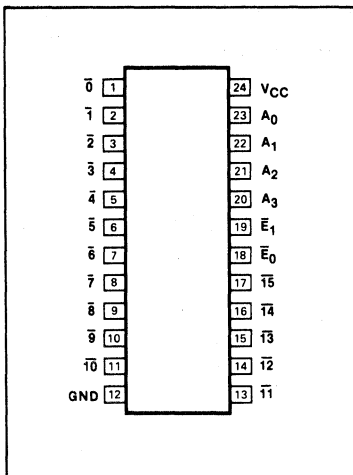
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1uI	1LSuI
All	Outputs	10uI	10LSuI

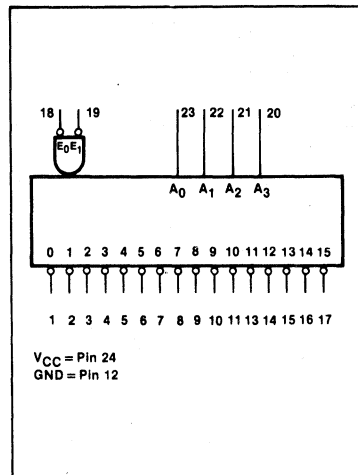
NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and -0.4mA I_{IL} .

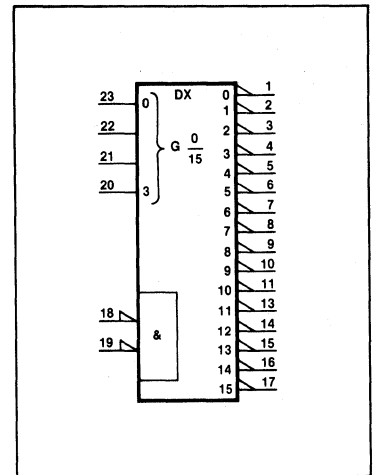
PIN CONFIGURATION



LOGIC SYMBOL



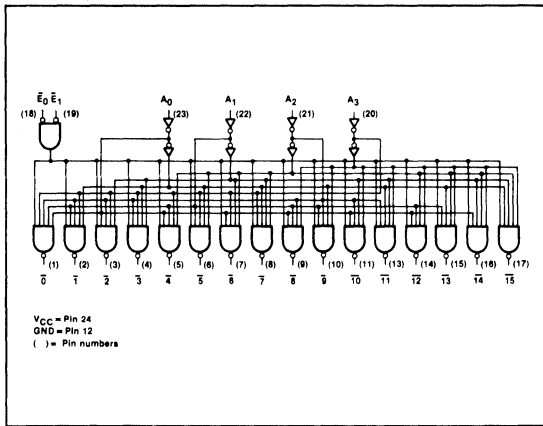
LOGIC SYMBOL (IEEE/IEC)



DECODER/DEMULTIPLEXERS

54/74154, LS154

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS																
E_0	E_1	A_3	A_2	A_1	A_0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

4

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-12			-18	mA
I_{OH} HIGH-level output current				-800			-400	μA
I_{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

DECODER/DEMULTIPLEXERS

54/74154, LS154

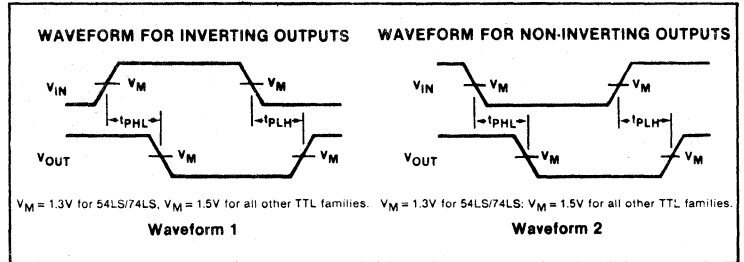
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74154			54/74LS154			UNIT			
		Min	Typ ²	Max	Min	Typ ²	Max				
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V			
		Com'l	2.4	3.4		2.7	3.4	V			
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V	
			Com'l			0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS						0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V		
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V							1.0	mA	
		V _I = 7.0V								0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V								40	μA
		V _I = 2.7V									20
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V								-1.6	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-15		-100		mA	
		Com'l	-18		-57	-15		-100		mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		34	49		9	14		mA	
		Com'l		34	56		9	14		mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all inputs grounded and all outputs open.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

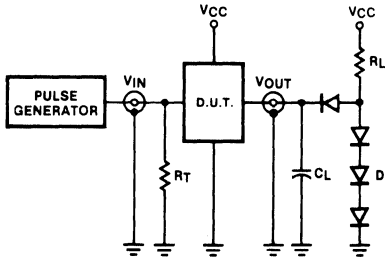
PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Address to output	Waveform 1		36 33		ns
				36 33		
t _{PLH} t _{PHL}	Propagation delay Enable to output	Waveform 2		30 27		ns
				30 27		

DECODER/DEMULTIPLEXERS

54/74154, LS154

TEST CIRCUITS AND WAVEFORMS

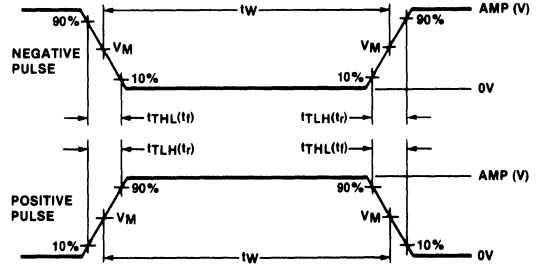
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODERS/DEMULTIPLEXERS

54/74155, LS155

Dual 2-Line To 4-Line Decoder/Demultiplexer

- Common Address inputs
- True or complement data demultiplexing
- Dual 1-of-4 or 1-of-8 decoding
- Function generator applications

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74155	18ns	25mA
74LS155	17ns	6.1mA

DESCRIPTION

The '155 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address input (A_0, A_1) and provide four mutually exclusive active-LOW outputs ($\bar{0}$ - $\bar{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input ($E_a \cdot \bar{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the \bar{E}_a or E_a inputs respectively. The decoder "b" enable gate requires two active-LOW inputs ($\bar{E}_b \cdot \bar{E}_b$). The device can be used as a 1-of-8 decoder/demultiplexer by tying E_a to \bar{E}_b and relabeling the common connection address as (A_2); forming the common enable by connecting the remaining \bar{E}_b and \bar{E}_a .

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74155N • N74LS155N	
Plastic SO	N74LS155D	

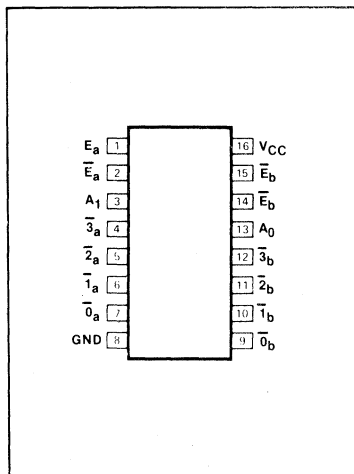
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

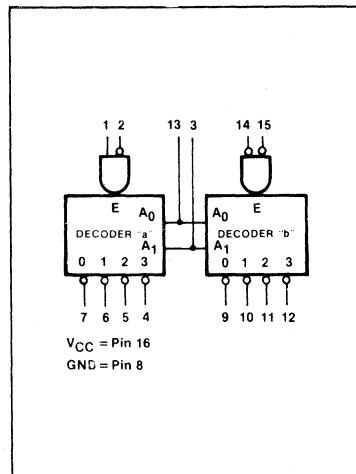
NOTE

Where a 54/74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

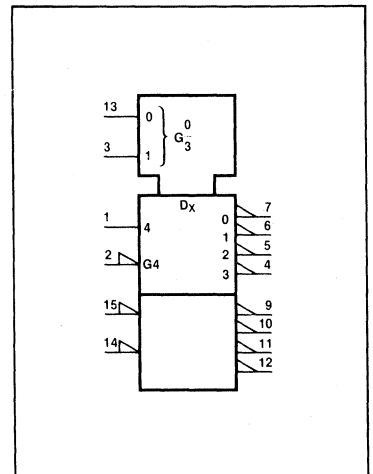
PIN CONFIGURATION



LOGIC SYMBOL



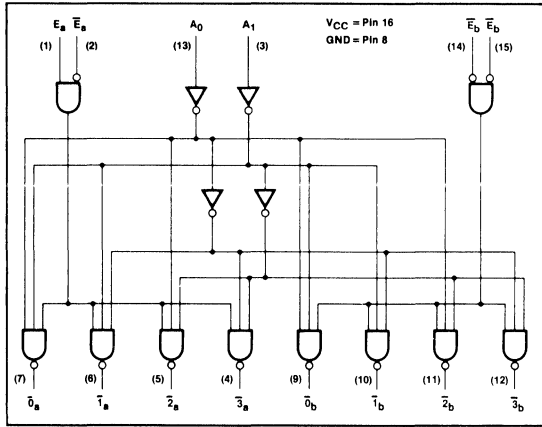
LOGIC SYMBOL (IEEE/IEC)



DECODERS/DEMULTIPLEXERS

54/74155, LS155

LOGIC DIAGRAM



FUNCTION TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A ₀	A ₁	E _a	E _a [̄]	0	1	2	3	E _b [̄]	E _b	0	1	2	3
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	L	L	L	L	L	H	H	H
L	L	H	L	L	L	H	H	L	L	L	L	H	H
L	H	H	L	H	H	L	L	L	L	H	H	L	L
H	H	H	L	H	H	H	L	L	L	H	H	L	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

4

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current				-800			-400	μA
I _{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

DECODERS/DEMULTIPLEXERS

54/74155, LS155

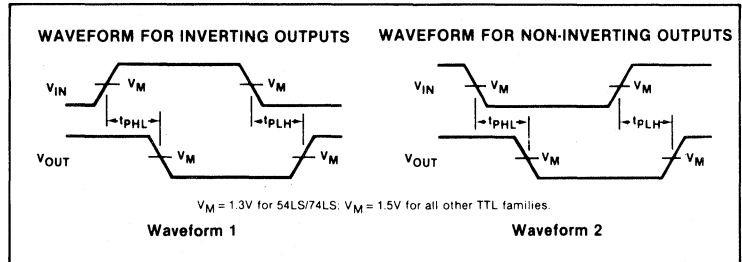
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74155			54/74LS155			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.25	0.4	V	
		I _{OL} = 4mA	Com'l		0.2	0.4		0.35	0.5	V
			74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V		
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA		
		V _I = 7.0V					0.1	mA		
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40			μA		
		V _I = 2.7V					20	μA		
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-1.6			-0.4	mA		
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	-15		-100	mA	
		Com'l	-18		-57	-15		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		25	35		6.1	10	mA	
		Com'l		25	40		6.1	10	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with A₁, A₀ and E_a inputs at 4.5V, and E_b, E_a inputs grounded, and outputs open.

AC WAVEFORMS

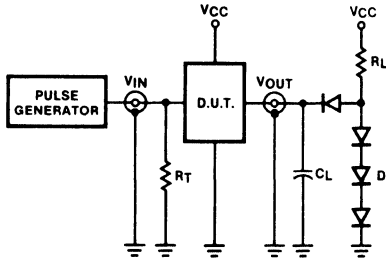


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay Address to output	Waveform 1	32 32	26 30		ns
t _{PLH} t _{PHL}	Propagation delay E _a or E _b to output	Waveform 2	20 27	15 30		ns
t _{PLH} t _{PHL}	Propagation delay E _a to output	Waveform 1	24 30	27 27		ns

TEST CIRCUITS AND WAVEFORMS

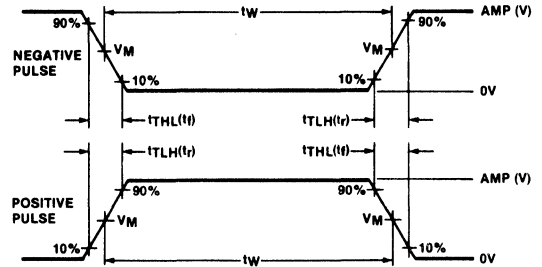
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODERS/DEMULTIPLXERS

54/74156, LS156

**Dual 2-Line To 4-Line Decoder/Demultiplexer
(Open Collector)**

- Common Address inputs
- True or complement data demultiplexing
- Dual 1-of-4 or 1-of-8 decoding
- Function generator applications
- Outputs can be tied together

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74156	20ns	25mA
74LS156	31ns	6.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74156N • N74LS156N	
Plastic SO	N74LS156D	
Ceramic DIP		S54LS156F
Flatpack		S54LS156W

DESCRIPTION

The '156 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address inputs (A_0, A_1) and provide four mutually exclusive active-LOW outputs ($\bar{0}$ - $\bar{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input (E_a, \bar{E}_a). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the \bar{E}_a or E_a inputs respectively. The decoder "b" enable gate requires two active-LOW inputs (\bar{E}_b, \bar{E}_b). The device can be used as a 1-of-8 decoder/demultiplexer by tying E_a to \bar{E}_b and relabeling the common connection address as (A_2); forming the common enable by connecting the remaining \bar{E}_b and \bar{E}_a .

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1uI	1LSuI
All	Outputs	10uI	10LSuI

NOTE

Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

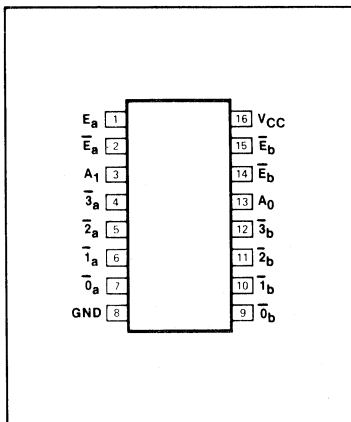
The '156 can be used to generate all four minterms of two variables. The four minterms are useful to replace multiple gate functions in some applications. A further advantage of the '156 is being able to AND the minterm functions by tying outputs

together. Any number of terms can be wired-AND as shown in the formula below:

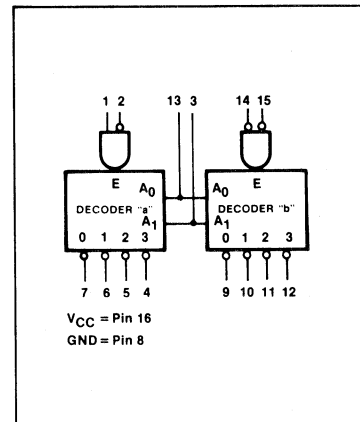
$$f = (E + A_0 + A_1) \cdot (E + \bar{A}_0 + A_1) \cdot (E + A_0 + \bar{A}_1) \cdot (E + A_0 + A_1)$$

where $E = E_a + E_a$; $E = E_b + E_b$.

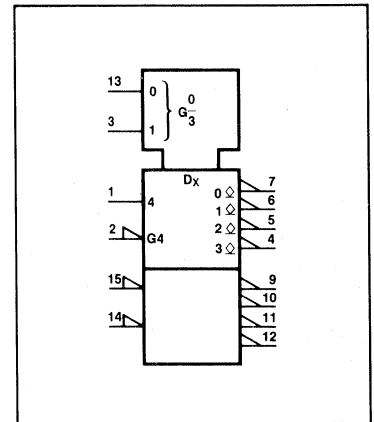
PIN CONFIGURATION



LOGIC SYMBOL



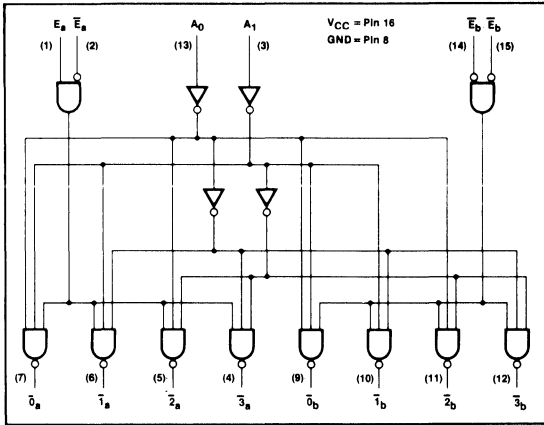
LOGIC SYMBOL (IEEE/IEC)



DECODERS/DEMULTIPLEXERS

54/74156, LS156

LOGIC DIAGRAM



FUNCTION TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A ₀	A ₁	E _a	\bar{E}_a	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	\bar{E}_b	\bar{E}_b	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	L	H	H	L	L	L	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	L	H
L	H	H	L	L	H	L	H	L	L	H	H	L	H
L	H	H	L	L	H	H	L	L	L	H	H	L	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
V _{OH} HIGH-level output voltage				5.5			5.5	V
I _{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

DECODERS/DEMULTIPLEXERS

54/74156, LS156

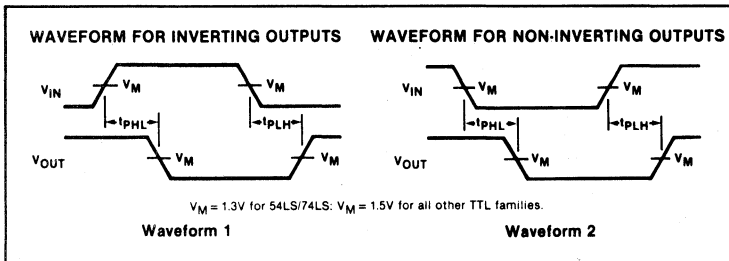
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74156			54/74LS156			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 5.5\text{V}$			250			100	μA	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	Mil	0.2	0.4		0.25	0.4	V
			Com'l	0.2	0.4		0.35	0.5	V
		$I_{OL} = 4\text{mA}$	74LS				0.25	0.4	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5			-1.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$			1.0			mA	
		$V_I = 7.0\text{V}$					0.1	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$			40			μA	
		$V_I = 2.7\text{V}$					20	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-1.6			-0.4	mA	
I_{CC} Supply current ³ (total)	$V_{CC} = \text{MAX}$	Mil	25	35		6.1	10	mA	
		Com'l	25	40		6.1	10	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- Measure I_{CC} with A_1, A_0 and E_a inputs at 4.5V, and E_b, E_a inputs grounded, and outputs open.

AC WAVEFORMS

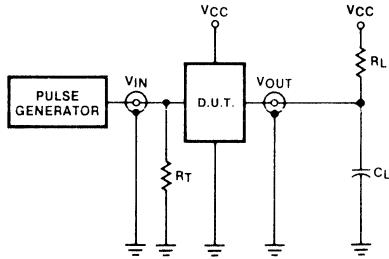


AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		$C_L = 15\text{pF}, R_L = 400\Omega$		$C_L = 15\text{pF}, R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Address to output	Waveform 1		34 34		46 51	ns
t_{PLH} t_{PHL} E_a or E_b to output	Waveform 2		23 30		40 51	ns
t_{PLH} t_{PHL} E_a to output	Waveform 1		27 33		48 48	ns

TEST CIRCUITS AND WAVEFORMS

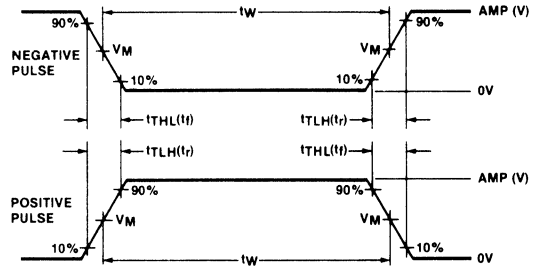
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

'157 Quad 2-Input Data Selector/Multiplexer (Non-Inverted) '158 Quad 2-Input Data Selector/Multiplexer (Inverted)

DESCRIPTION

The '157 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common Select input (S). The Enable input (\bar{E}) is active LOW. When \bar{E} is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the '157. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$\begin{aligned} Y_a &= \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ Y_b &= \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ Y_c &= \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ Y_d &= \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

The '158 is similar but has inverting outputs:

$$\begin{aligned} \bar{Y}_a &= \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S}) \\ \bar{Y}_b &= \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S}) \\ \bar{Y}_c &= \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S}) \\ \bar{Y}_d &= \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S}) \end{aligned}$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74157	13ns	30mA
74LS157	13ns	9.7mA
74S157	7.4ns	50mA
74158	13ns	30mA
74LS158	13ns	4.8mA
74S158	6ns	40mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74157N • N74158N N74S157N • N74LS157N N74S158N • N74LS158N	
Plastic SO	N74LS157D N74LS158D	
Ceramic DIP		S54157F S54S157F • S54LS157F S54S158F • S54LS158F
Flatpack		S54157W S54S157W • S54LS157W S54S158W • S54LS158W
LLCC		

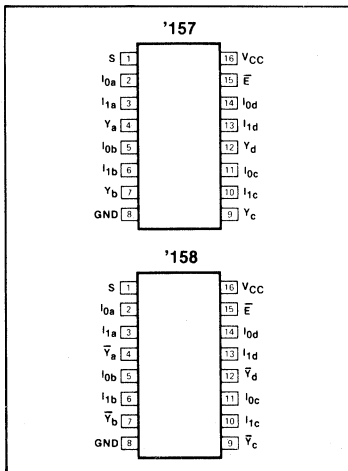
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
S, \bar{E}	Inputs	1uI	2Sul	2LSul
Data	Inputs	1uI	1Sul	1LSul
All	Outputs	10uI	10Sul	10LSul

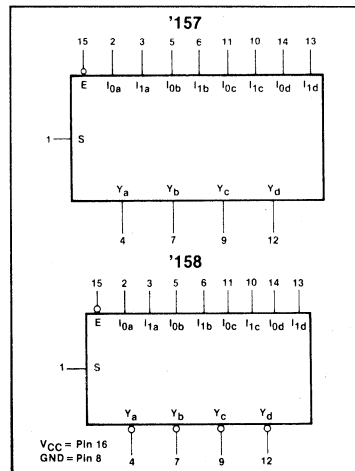
NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

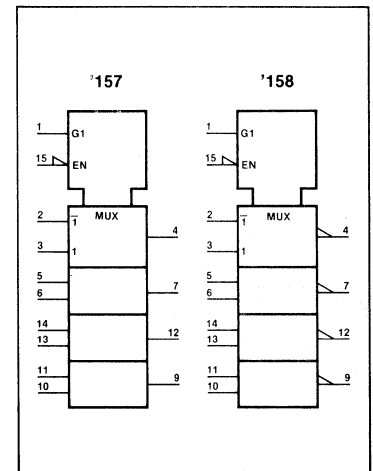
PIN CONFIGURATION



LOGIC SYMBOL

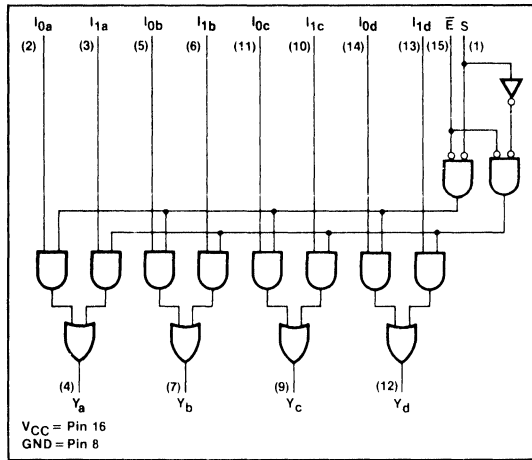


LOGIC SYMBOL (IEEE/IEC)

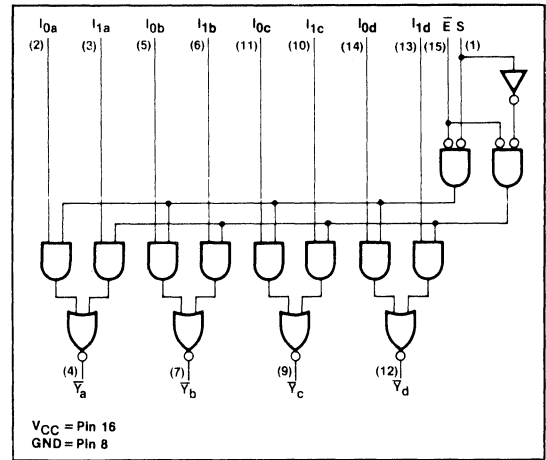


DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

LOGIC DIAGRAM, '157



LOGIC DIAGRAM, '158



FUNCTION TABLE, '157

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
\bar{E}	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	L	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

FUNCTION TABLE, '158

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
\bar{E}	S	I_0	I_1	\bar{Y}
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125			0 to 70			°C

DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

RECOMMENDED OPERATING CONDITIONS

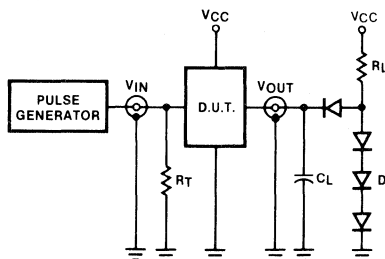
PARAMETER		54/74			54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			2.0				V
V _{IL}	LOW-level input voltage	Mil			+ 0.8			+ 0.7			+ 0.8	V
		Com'l			+ 0.8			+ 0.8			+ 0.8	V
I _{IK}	Input clamp current			- 12			- 18			- 18	mA	
I _{OH}	HIGH-level output current			- 800			- 400			- 1000	μA	
I _{OL}	LOW-level output current	Mil		16			4			20	mA	
		Com'l		16			8			20	mA	
T _A	Operating free-air temperature	Mil	- 55		+ 125	- 55		+ 125	- 55		+ 125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE

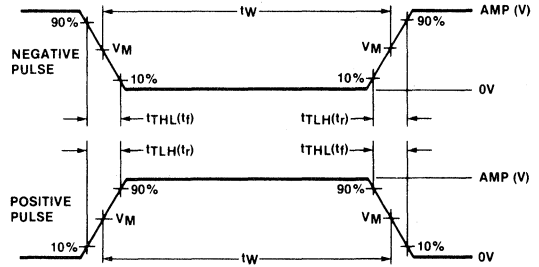
V_{IL} = + 0.7V MAX for 54S at + 125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74157, 158			54/74LS157, 158			54/74S157, 158			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4		V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5 ⁶	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V				1.0					1.0	mA	
		V _I = 7.0V	S, \bar{E} Inputs						0.2				mA
			Data inputs						0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	S, \bar{E} inputs			40						μ A	
			Data inputs			40						μ A	
		V _I = 2.7V	S, \bar{E} inputs						40			100	μ A
			Data inputs						20			50	μ A
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	S, \bar{E} inputs			-1.6			-0.8			mA	
			Data inputs			-1.6			-0.4			mA	
		V _I = 0.5V	S, \bar{E} inputs									-4	mA
			Data inputs									-2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		Mil	-20		-55	-20		-100	-40		-100	mA
			Com'l	-18		-55	-20		-100	-40		-100	mA
I _{CC} Supply current ^{4,5} (total)	V _{CC} = MAX	Note 4	'157, '158		30	48							mA
		Note 4	'LS157					9.7	16				mA
		Note 4	'LS158					4.8	8				mA
		Note 5	'S157 All inputs = 4.5V								50	78	mA
		Note 5	'S158 All inputs = 4.5V								39	61	mA
		Note 5	'S158 I _{0A} , I _{0B} , I _{0C} , I _{0D} at 4.5V, other inputs at 0V								41	81	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - I_{CC} is measured with 4.5V applied to all inputs and all outputs open.
 - I_{CC} is measured with all outputs open.
 - V_{OL} = +0.45V MAX for 54S at +125°C only.

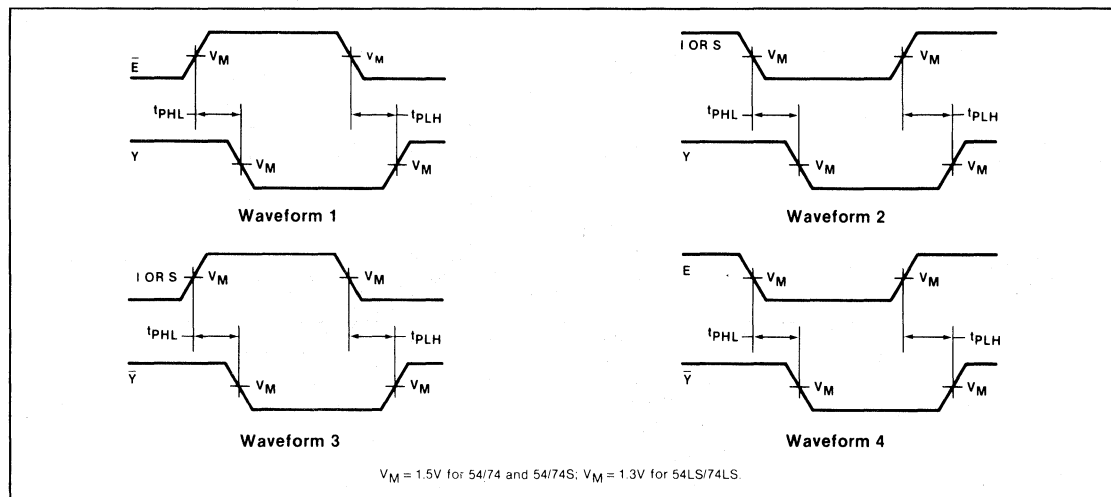
4

DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay Data to output	Waveform 2, '157		14 14		14 14		7.5 6.5	ns
t_{PLH} t_{PHL} Propagation delay Enable to output	Waveform 1, '157		20 21		20 21		12.5 12	ns
t_{PLH} t_{PHL} Propagation delay Select to output	Waveform 2, '157		23 27		23 27		15 15	ns
t_{PLH} t_{PHL} Propagation delay Data to output	Waveform 3, '158		14 14		12 15		6.0 6.0	ns
t_{PLH} t_{PHL} Propagation delay Enable to output	Waveform 4, '158		20 21		17 24		11.5 12	ns
t_{PLH} t_{PHL} Propagation delay Select to output	Waveform 3, '158		23 27		20 24		12 12	ns

AC WAVEFORMS



COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

'160, '162 BCD Decade Counter
'161, '163 4-Bit Binary Counter

- Synchronous counting and loading
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous reset ('160, '161)
Synchronous reset ('162, '163)
- Hysteresis on Clock input (LS only)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74160-74163	32MHz	61mA
74LS160A-74LS163A	32MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74160N • N74LS160AN N74161N • N74LS161AN N74LS162AN N74163N • N74LS163AN	
Plastic SO	N74LS161AD • N74LS163AD	
Ceramic DIP		S54160F • S54LS160AF S54161F • S54LS161AF S54LS162AF S54163F • S54LS163AF
Flatpack		S54160W • S54LS160AW S54161W • S54LS161AW S54LS162AW S54163W • S54LS163AW
LLCC		S54LS161AG • S54LS163AG

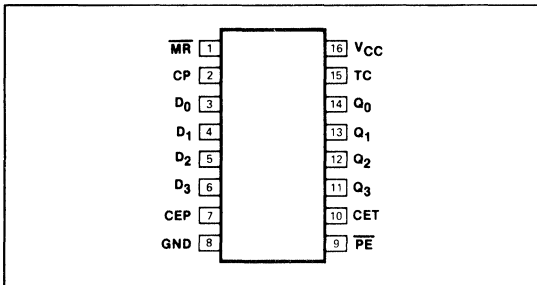
DESCRIPTION

Synchronous presettable decade (54/74160, 54/74LS160A, 54/74LS162A) and 4-bit (54/74161, 54/74LS161A, 54/74163, 54/74LS163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

The outputs of the counters may be preset to HIGH or LOW level. A LOW level at the Parallel Enable (\overline{PE}) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the positive-going edge of the clock (providing that the setup and hold requirements for \overline{PE} are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A LOW level at the Master Reset (\overline{MR}) input sets all four outputs of the flip-flops (Q_0 - Q_3) in '160, 'LS160A, '161, and 'LS161A to LOW levels regardless of the levels at CP, \overline{PE} , CET and CEP inputs (thus providing an asynchronous clear function).

PIN CONFIGURATION



INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

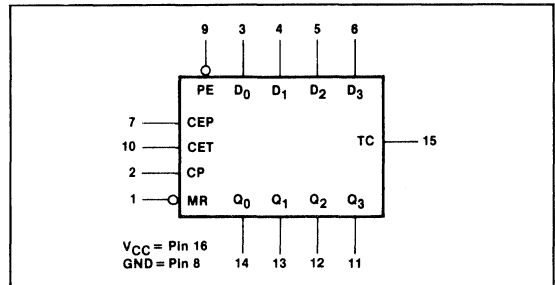
PINS	DESCRIPTION	54/74	54/74LS
CP, CET	Inputs	2ul	2LSul
D, CEP	Inputs	1ul	1LSul
\overline{PE}	Input	1ul	2LSul
All	Outputs	10ul	10LSul
\overline{MR}	Input ('160, '161)	1ul	1LSul
\overline{MR}	Input ('162, '163)	1ul	2LSul

NOTE
Where a 54/74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

For the 'LS162A, '163, and LS163A, the clear function is synchronous. A LOW level at the Master Reset (\overline{MR}) input sets all four outputs of the flip-flops (Q_0 - Q_3) to LOW levels after the next positive-going transition on the Clock (CP) input (providing that the setup and hold requirements

for \overline{MR} are met). This action occurs regardless of the levels at \overline{PE} , CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

LOGIC SYMBOL



COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to the HIGH level output of Q_0 . This pulse can be used to enable the next cascaded stage (see Figure B).

For conventional operation of 54/74160, 54/74161 and 54/74163, the following transitions should be avoided.

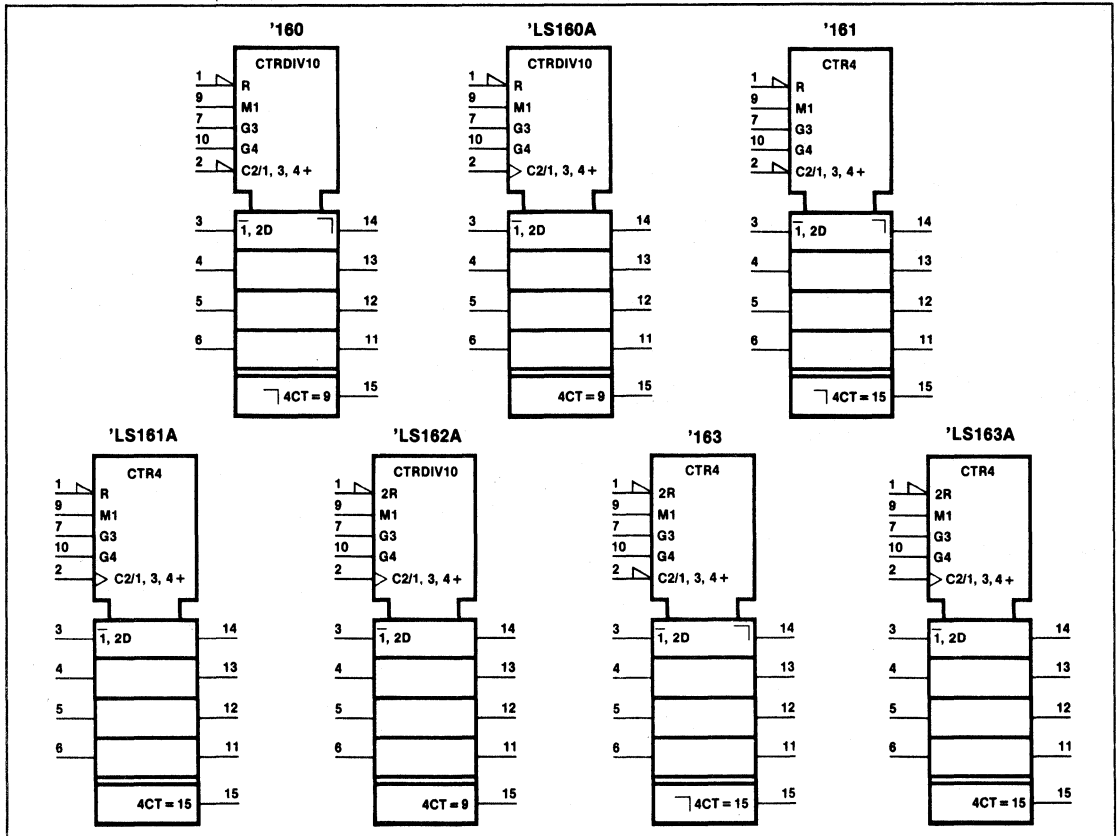
1. HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transitions on the Parallel Enable input when CP is LOW, if the count enables and \overline{MR} are HIGH at or before the transition.

For 54/74163 there is an additional transition to be avoided.

3. LOW-to-HIGH transition on the \overline{MR} input when clock is LOW, if the Enable and \overline{PE} inputs are HIGH at or before the transition.

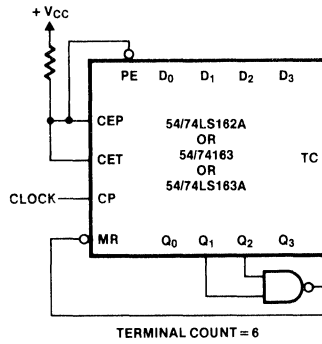
These restrictions are not applicable to 54/74LS160A, 54/74LS161A, 54/74LS162A and 54/74LS163A.

LOGIC SYMBOL (IEEE/IEC)



COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

4



TERMINAL COUNT = 6

Figure A

SYNCHRONOUS MULTISTAGE COUNTING SCHEME

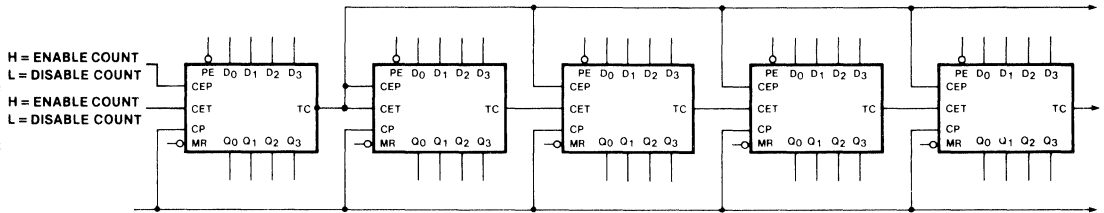
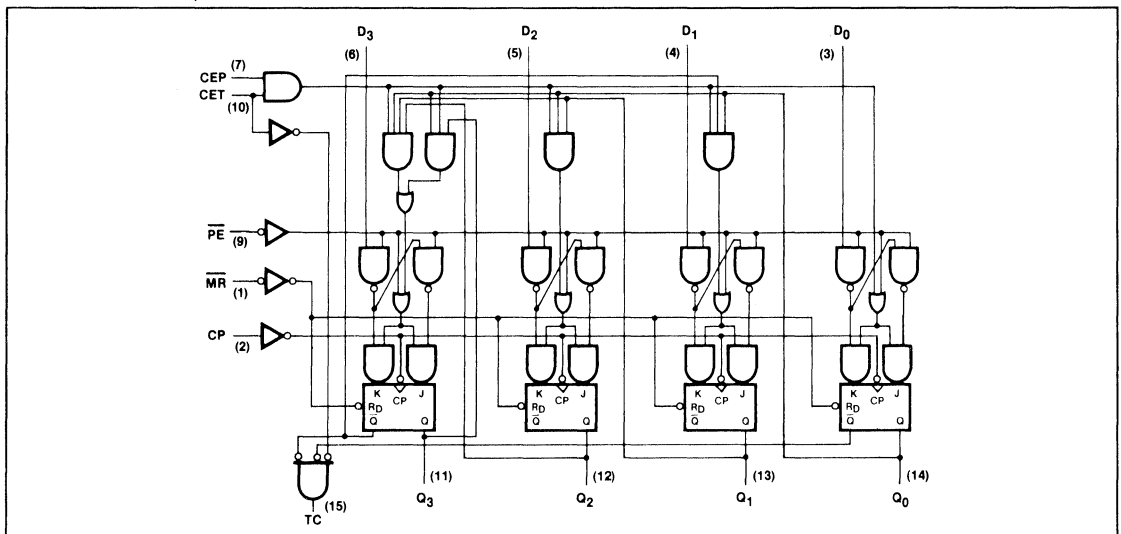


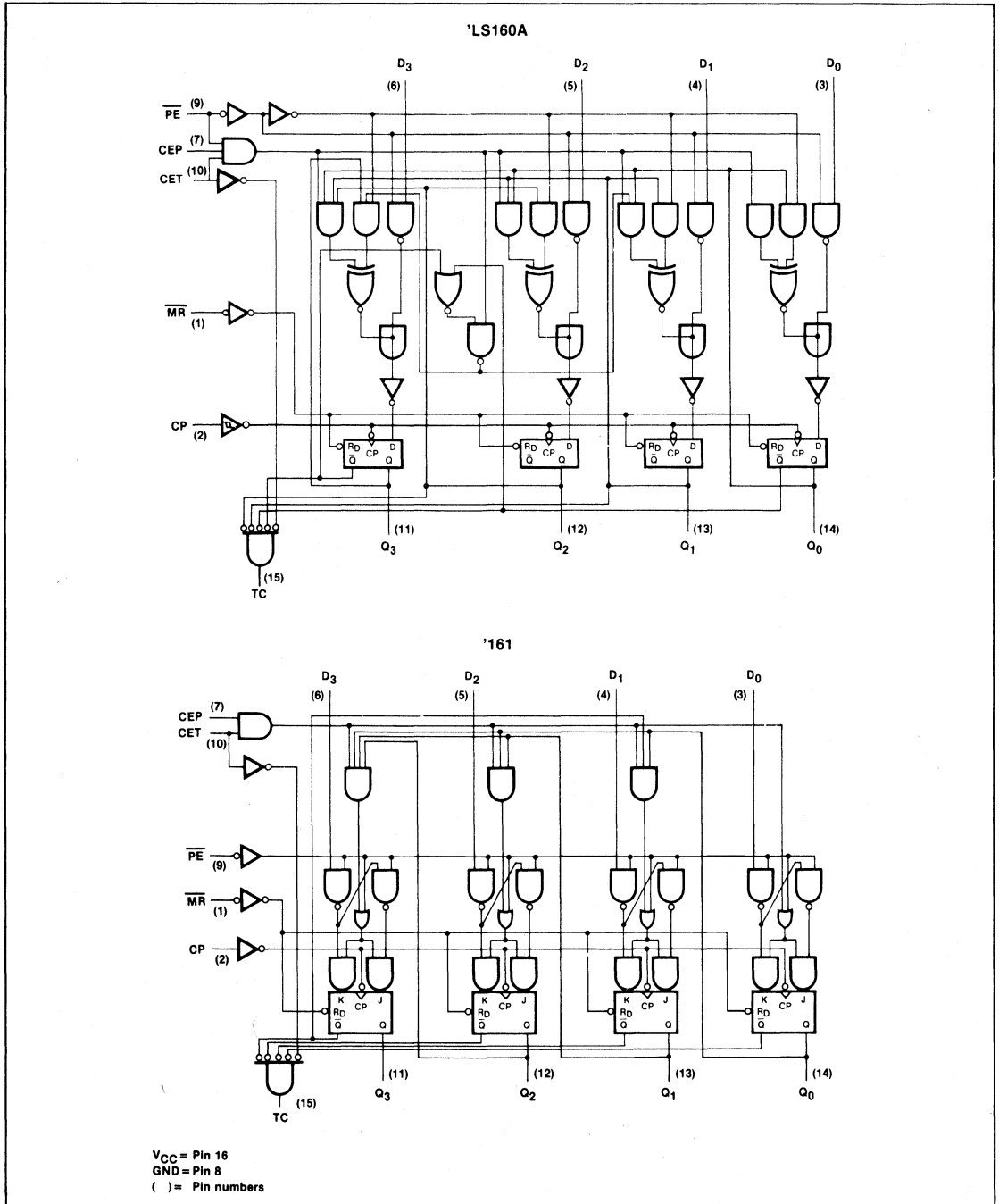
Figure B

LOGIC DIAGRAM, 54/74160



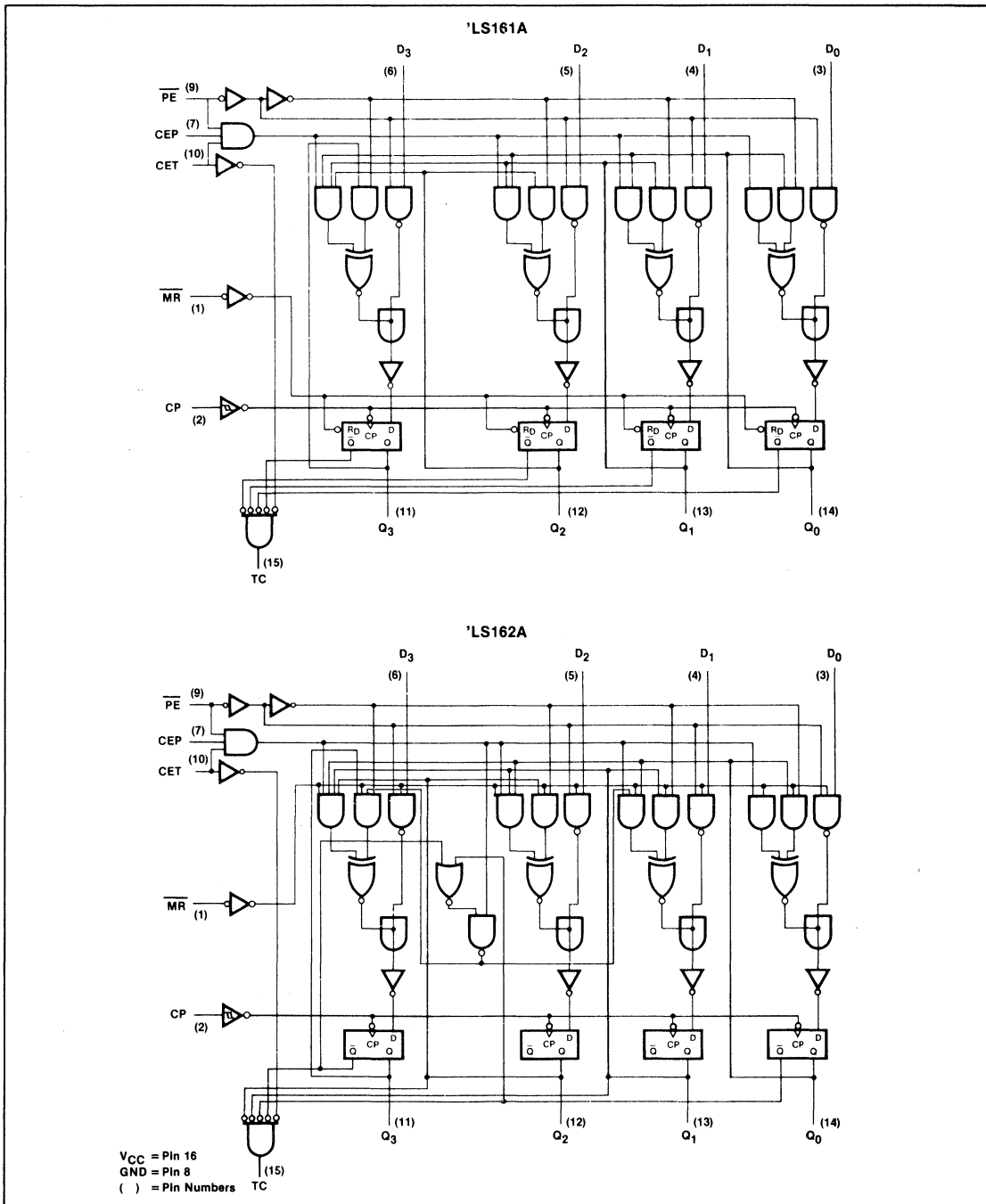
COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

LOGIC DIAGRAMS



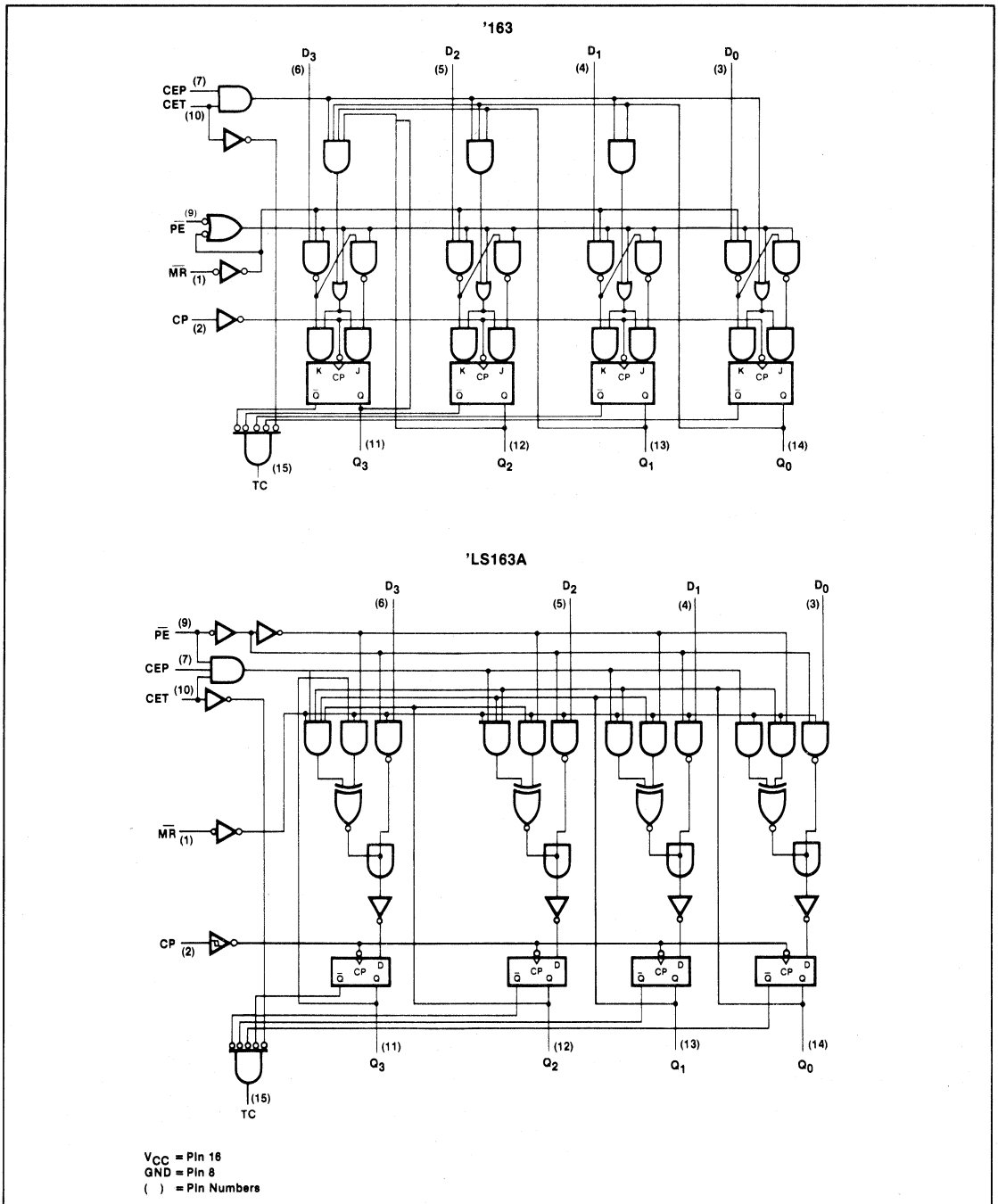
COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

LOGIC DIAGRAMS



COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

LOGIC DIAGRAMS



COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

MODE SELECT—FUNCTION TABLE, '160, '161

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{MR}	CP	CEP	CET	\overline{PE}	D_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(a)
Count	H	↑	h	h	h ^(c)	X	count	(a)
Hold (do nothing)	H	X	l ^(b)	X	h ^(c)	X	q _n	(a)
	H	X	X	l ^(b)	h ^(c)	X	q _n	L

MODE SELECT—FUNCTION TABLE, '162, '163

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{MR}	CP	CEP	CET	\overline{PE}	D_n	Q_n	TC
Reset (Clear)	l	l	X	X	X	X	L	L
Parallel Load	h ^(f)	l	X	X	l	l	L	L
	h ^(f)	↑	X	X	l	h	H	(d)
Count	h ^(f)	↑	h	h	h ^(f)	X	count	(d)
Hold (do nothing)	h ^(f)	X	l ^(e)	X	h ^(f)	X	q _n	(d)
	h ^(f)	X	X	l ^(e)	h ^(f)	X	q _n	L

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

X = Don't care.

q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.

↑ = LOW-to-HIGH clock transition.

NOTES

(a) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for '161 and HLLH for '160).

(b) The HIGH-to-LOW transition of CEP or CET on the 54/74161 and 54/74160 should only occur while CP is HIGH for conventional operation.

(c) The LOW-to-HIGH transition of \overline{PE} on the 54/74161 and 54/74160 should only occur while CP is HIGH for conventional operation.

(d) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for '162 and HHHH for '163).

(e) The HIGH-to-LOW transition of CEP or CET on the 54/74163 should only occur while CP is HIGH for conventional operation.

(f) The LOW-to-HIGH transition of \overline{PE} or \overline{MR} on the 54/74163 should only occur while CP is HIGH for conventional operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125		0 to 70		°C

4

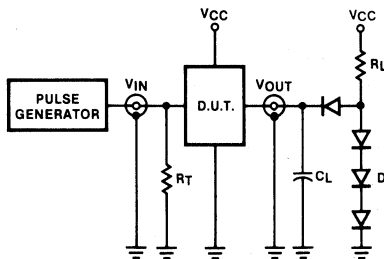
COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.8			+ 0.7	V
		Com'l			+ 0.8			+ 0.8	V
I _{IK}	Input clamp current				- 12			- 18	mA
I _{OH}	HIGH-level output current				- 800			- 400	μA
I _{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	- 55		+ 125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

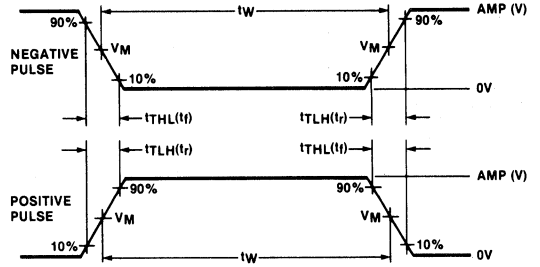
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74160, '161 '163			54/74LS160A, '161A '162A, '163A			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		V	
		Com'l	2.4	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.5		-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V				1.0			mA	
		V _I = 7.0V	D, CEP						0.1	mA
			PE, CP, CET						0.2	mA
			MR ('LS160A, 'LS161A)						0.1	mA
			MR ('LS162A, 'LS163A)						0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	CP, CET			80			μA	
			Other inputs			40			μA	
		V _I = 2.7V	D, CEP						20	μA
			PE, CP, CET						40	μA
			MR ('LS160A, 'LS161A)						20	μA
			MR ('LS162A, 'LS163A)						40	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	CP, CET			-3.2			mA	
			Other inputs			-1.6			mA	
		V _I = 0.4V	D, CEP						-0.4	mA
			PE, CP, CET						-0.8	mA
			MR ('LS160A, 'LS161A)						-0.4	mA
			MR ('LS162A, 'LS163A)						-0.8	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		Mil	-20		-57	-20		-100	mA
			Com'l	-18		-57	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	I _{CCH} All outputs HIGH	Mil		59	85		18	31	mA
			Com'l		59	94		18	31	mA
		I _{CCL} All outputs LOW	Mil		63	91		19	32	mA
			Com'l		63	101		19	32	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CCH} is measured with PE input HIGH, again with PE input LOW, all other inputs HIGH and outputs open. I_{CCL} is measured with Clock input HIGH, again with Clock input LOW, all other inputs low and outputs open.

4

COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	25		25		MHz
t_{PLH} Propagation delay t_{PHL} Clock to Terminal Count	Waveform 1		35 35		35 35	ns
t_{PLH} Propagation delay t_{PHL} Clock to Q outputs	Waveform 1, PE = HIGH		20 23		24 27	ns
t_{PLH} Propagation delay t_{PHL} Clock to Q outputs	Waveform 1, PE = LOW		25 29		24 27	ns
t_{PLH} Propagation delay t_{PHL} CET input to TC output	Waveform 2		16 16		14 14	ns
t_{PHL} Propagation delay, $\overline{\text{MR}}$ to Q outputs ('160, '161)	Waveform 3		38		28	ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_f , t_r , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		Min	Max	Min	Max	
$t_{\text{W(L)}}$ Clock pulse width (LOW)	Waveform 1	25		25		ns
t_{W} Master Reset pulse width ('160, '161)	Waveform 3	20		20		ns
t_{W} Master Reset pulse width ('162, '163)	Waveform 6	20		20		ns
t_{s} Setup time, Data to Clock	Waveform 5	20		20		ns
t_{h} Hold time, Data to Clock ¹	Waveform 5	3		3		ns
t_{s} Setup time, CEP or CET to Clock	Waveform 4	20		20		ns
t_{h} Hold time, CEP or CET to Clock	Waveform 4	0		0		ns
t_{s} Setup time, $\overline{\text{PE}}$ to Clock	Waveform 5	25		20		ns
t_{h} Hold time, $\overline{\text{PE}}$ to Clock	Waveform 5	0		0		ns
t_{s} Setup time, $\overline{\text{MR}}$ to Clock ('162, '163)	Waveform 6	20		20		ns
t_{h} Hold time, $\overline{\text{MR}}$ to Clock ('162, '163)	Waveform 6	0		0		ns
t_{rec} Recovery time, $\overline{\text{MR}}$ to CP	Waveform 3	25		15		ns

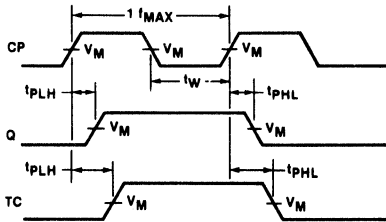
NOTE 1

For 15 ns rise time only, Hold time must be increased by 0.3 ns for each nanosecond decrease in rise time.

COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

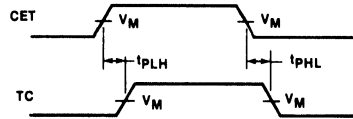
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, MAXIMUM FREQUENCY, AND CLOCK PULSE WIDTH



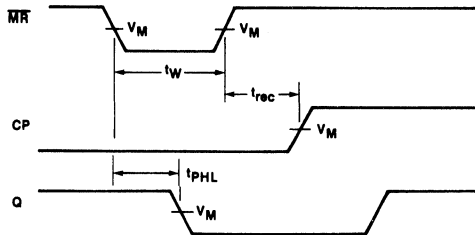
Waveform 1

PROPAGATION DELAYS CET INPUT TO TC OUTPUT



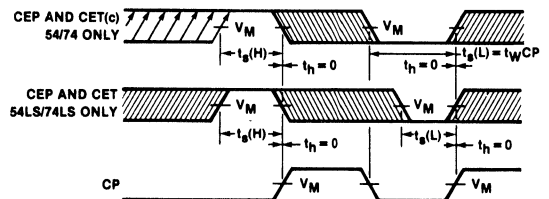
Waveform 2

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME ('160, '161)



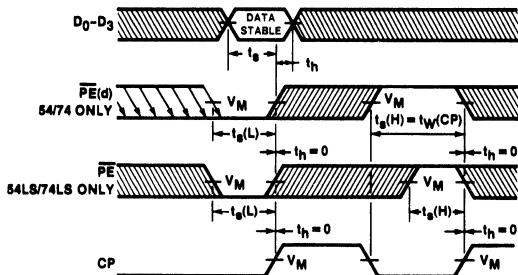
Waveform 3

CET AND CET SETUP AND HOLD TIMES



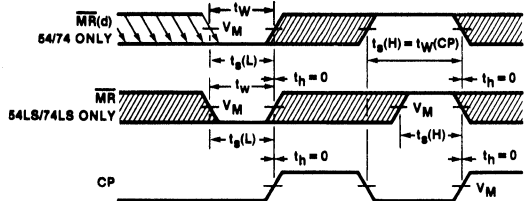
Waveform 4

PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES



Waveform 5

SYNCHRONOUS RESET SETUP, PULSE WIDTH AND HOLD TIMES ('162, '163)



Waveform 6

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

SHIFT REGISTERS

54/74164, LS164

8-Bit Serial-In Parallel-Out Shift Register

- Gated serial Data inputs
- Typical shift frequency of 36MHz
- Asynchronous Master Reset
- Fully buffered Clock and Data inputs

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74164	36MHz	37mA
74LS164	36MHz	16mA

DESCRIPTION

The '164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one setup time before the rising clock edge. A LOW level on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74164N • N74LS164N	
Plastic SO	N74LS164D	
Ceramic DIP		S54164F • S54LS164F
Flatpack		S54LS164W
LLCC		S54LS164G

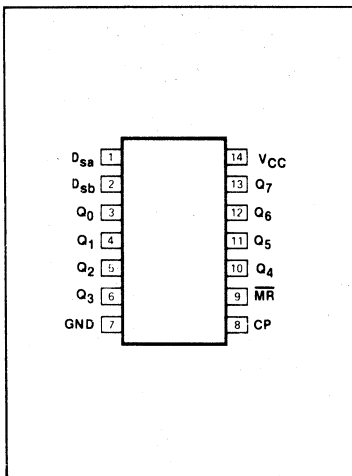
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1uI	1LSuI
All	Ouputs	5uI	10LSuI

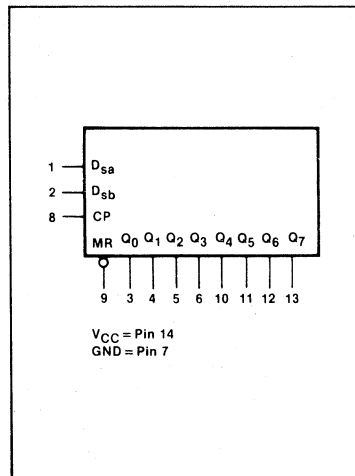
NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and - 1.6mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and - 0.4mA I_{IL} .

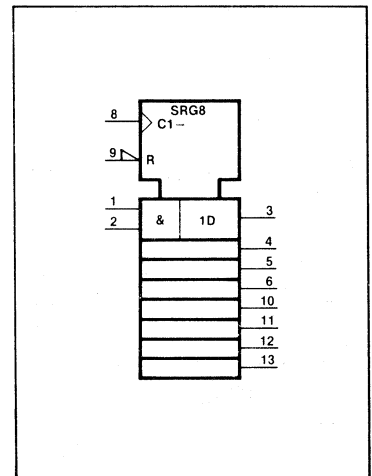
PIN CONFIGURATION



LOGIC SYMBOL



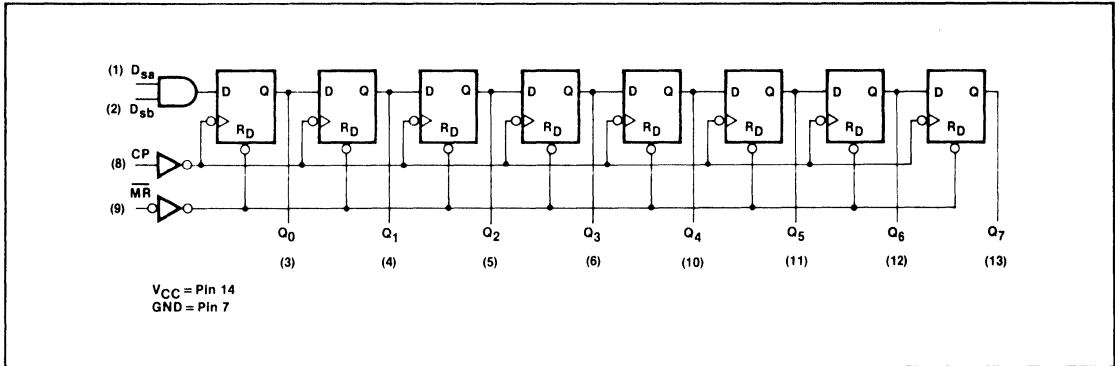
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTERS

54/74164, LS164

LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	MR	CP	D _{sa}	D _{sb}	Q ₀	Q ₁	—	Q ₇
Reset (Clear)	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q ₀	—	q ₆
	H	↑	l	h	L	q ₀	—	q ₆
	H	↑	h	l	L	q ₀	—	q ₆
	H	↑	h	h	H	q ₀	—	q ₆

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH Clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V	
V _{IL}	LOW-level input voltage	Mil		+0.8			+0.7	V	
		Com'l		+0.8			+0.8	V	
I _{IK}	Input clamp current			-12			-18	mA	
I _{OH}	HIGH-level output current			-400			-400	μA	
I _{OL}	LOW-level output current	Mil			8			4	mA
		Com'l			8			8	mA
T _A	Operating free-air temperature	Mil	-55		+125	-55		+125	°C
		Com'l	0		70	0		70	°C

SHIFT REGISTERS

54/74164, LS164

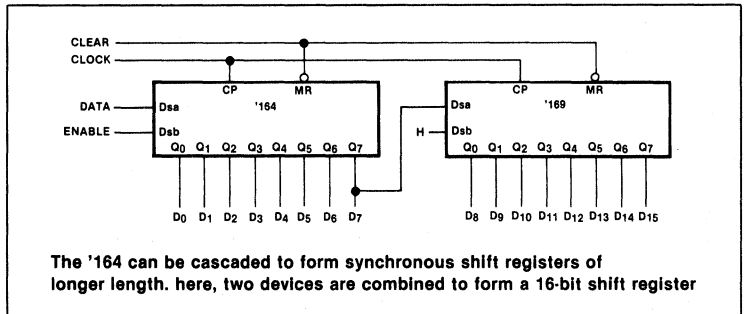
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74164			54/74LS164			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.2	0.4		0.25	0.4	V
			Com'l		0.2	0.4		0.35	0.5
		I _{OL} = 4mA	74LS					0.25	0.4
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V					0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40			μA	
		V _I = 2.7V					20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6		-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-10		-27.5	-20		-100	mA
		Com'l	-9		-27.5	-20		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		37	54		16	27	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the Serial inputs grounded, the Clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

APPLICATION



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		C _L = 15pF, R _L = 800Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
f _{MAX} Maximum shift frequency	Waveform 1	25		25		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 1		27 32		27 32	ns
t _{PHL} Propagation delay MR to output	Waveform 2		36		36	ns
t _{PLH} Propagation delay t _{PHL} Clock to output	C _L = 50pF for these parameters	Waveform 1	30 37			ns
t _{PHL} Propagation delay MR to output		Waveform 2	42			ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

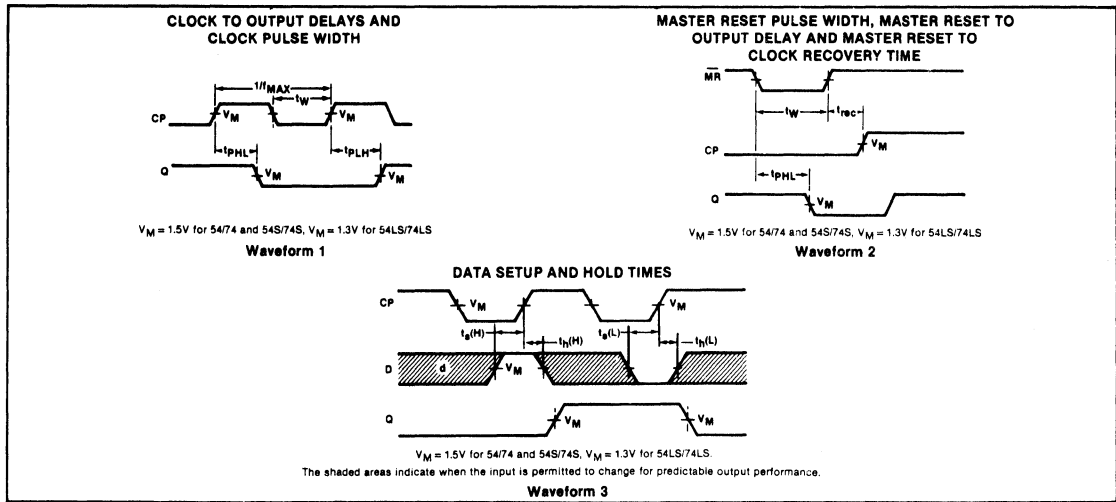
SHIFT REGISTERS

54/74164, LS164

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

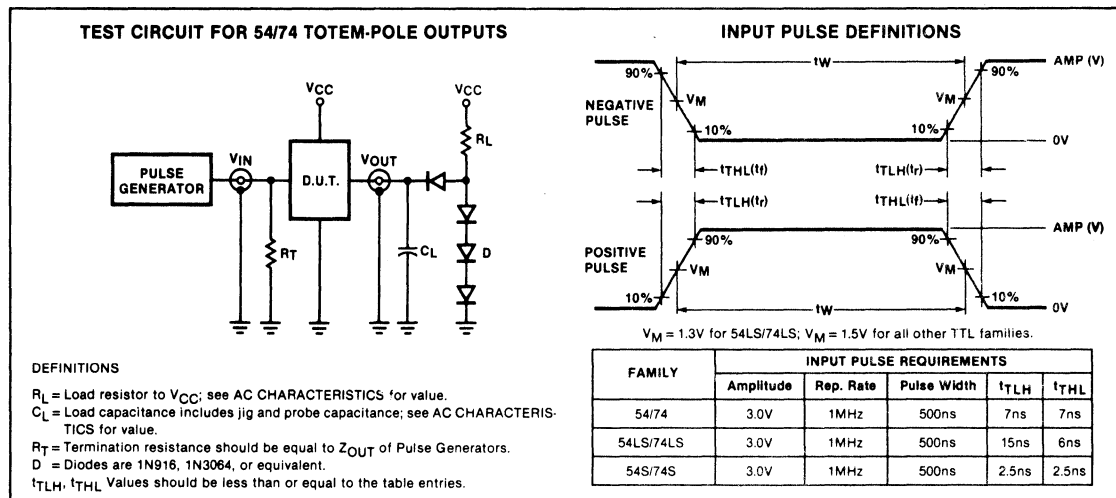
PARAMETER	TEST CONDITIONS	54/74		54/74LS		UNIT
		Min	Max	Min	Max	
t_W Clock pulse width	Waveform 1	20		20		ns
t_W MR pulse width	Waveform 2	20		20		ns
t_s Setup time Data to Clock	Waveform 3	15		15		ns
t_h Hold time Data to Clock	Waveform 3	5.0		5.0		ns
t_{rec} MR to Clock recovery time	Waveform 2	30		30		ns

AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS



SHIFT REGISTER

54/74165

8-Bit Serial/Parallel-In, Serial-Out Shift Register

- Asynchronous 8-bit parallel load
- Synchronous Serial input
- Clock Enable for "do nothing" mode
- See '166 for fully synchronous operation

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74165	26MHz	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74165N	
Ceramic DIP		S54165F
Flatpack		S54165W

DESCRIPTION

The '165 is an 8-bit parallel load or serial-in shift register with complementary Serial outputs (Q_7 and \bar{Q}_7) available from the last stage. When the Parallel Load (\overline{PL}) input is LOW, parallel data from the D_0 - D_7 inputs are loaded into the register asynchronously. When the \overline{PL} input is HIGH, data enters the register serially at the D_S input and shifts one place to the right (Q_0 - Q_1 - Q_2 , etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The Clock input is a gated-OR structure which allows one input to be used as an active LOW Clock Enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

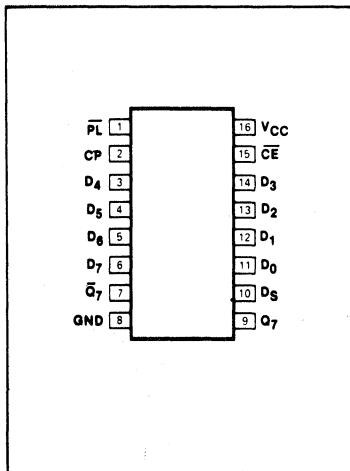
PINS	DESCRIPTION	54/74
\overline{PL}	Input	2uI
Other	Inputs	1uI
All	Outputs	10uI

NOTE
A 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} .

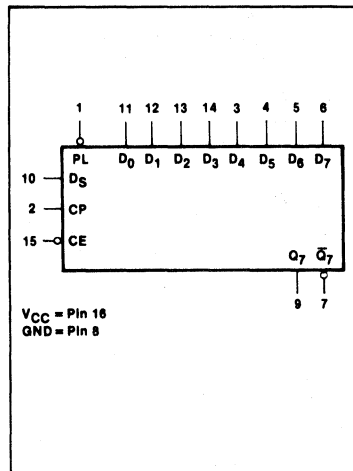
of \overline{CE} input should only take place while the CP is HIGH for predictable operation. Also, the CP and \overline{CE} inputs should be

LOW before the LOW-to-HIGH transition of \overline{PL} to prevent shifting the data when \overline{PL} is released.

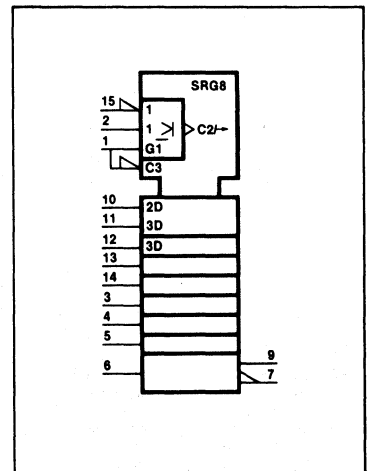
PIN CONFIGURATION



LOGIC SYMBOL



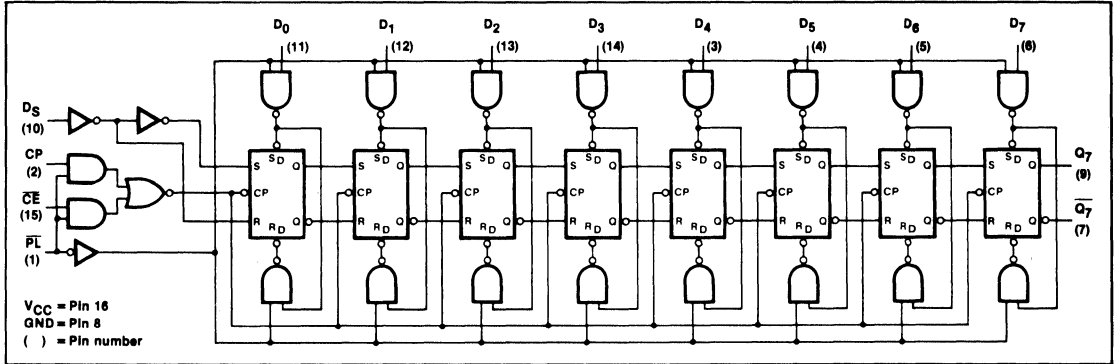
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER

54/74165

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUTS	
	\overline{PL}	\overline{CE}	CP	D_S	D_0-D_7	Q_0	Q_1-Q_6	Q_7	$\overline{Q_7}$
Parallel load	L	X	X	X	L	L	L-L	L	H
	L	X	X	X	H	H	H-H	H	L
Serial shift	H	L	!	l	X	L	q_0-q_6	q_6	$\overline{q_6}$
	H	L	!	h	X	H	q_0-q_6	q_6	$\overline{q_6}$
Hold "do nothing"	H	H	X	X	X	q_0	q_1-q_6	q_7	$\overline{q_7}$

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 q_n = Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ! = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

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SHIFT REGISTER

54/74165

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 12	mA
I _{OH}	HIGH-level output current				- 800	μA
I _{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74165			UNIT	
		Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		V
		Com'l	2.4	3.4		V
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}				-1.5	V
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 5.5V				1.0	mA
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.4V	PL input			80	μA
		Other inputs			40	μA
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V	PL input			-3.2	mA
		Other inputs			-1.6	mA
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	Mil	-20		-55	mA
		Com'l	-18		-55	mA
I _{CC}	Supply Current ⁴ (total) V _{CC} = MAX			42	63	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With the outputs open, CE and CP at 4.5V, and a clock pulse applied to the PL input, I_{CC} is measured first with the Parallel Data inputs at 4.5V, then with the Parallel Data inputs grounded.

SHIFT REGISTER

54/74165

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		
		Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	20	MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1	24 31	ns
t_{PLH} t_{PHL}	Propagation delay PL to output	Waveform 2	31 40	ns
t_{PLH} t_{PHL}	Propagation delay D_7 to Q_7	Waveform 3	17 36	ns
t_{PLH} t_{PHL}	Propagation delay D_7 to \bar{Q}_7	Waveform 3	27 27	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		Min	Max	
t_W	Clock pulse width	Waveform 1	25	ns
t_W	PL pulse width	Waveform 2	15	ns
t_s	Setup time, D_S to clock	Waveform 4	20	ns
t_h	Hold time, D_S to clock	Waveform 4	0	ns
$t_s(L)$	Setup time, LOW $\bar{C}E$ to clock	Waveform 4	30	ns
t_h	Hold time, $\bar{C}E$ to clock	Waveform 4	0	ns
t_s	PL setup time to clock	Waveform 2	45	ns
t_s	Setup time, D_5 and $D_7^{(a)}$ to $\bar{P}L$	Waveform 5	10	ns

NOTE
(a) The remaining six Data inputs and D_S are LOW. Prior to test, HIGH level data is loaded into D_7 input.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

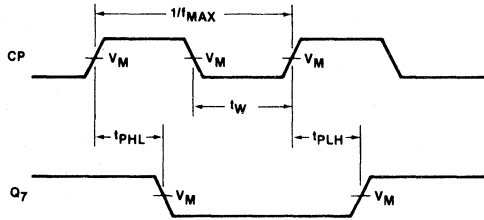
4

SHIFT REGISTER

54/74165

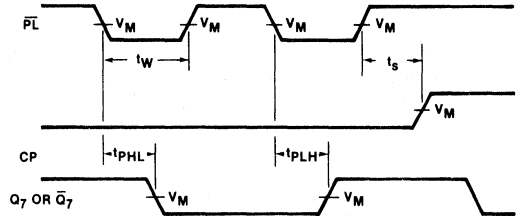
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

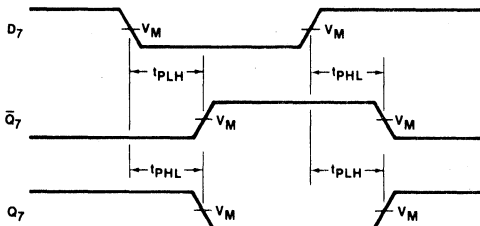
PARALLEL LOAD PULSE WIDTH, PL TO OUTPUT DELAYS, AND PL TO CLOCK SETUP TIME



Waveform 2

The changing output assumes internal Q₆ opposite state from Q₇.

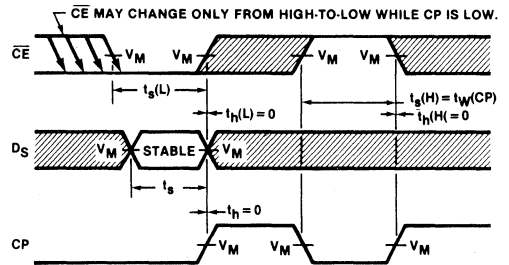
PARALLEL DATA TO OUTPUT DELAYS



CONDITIONS: \overline{PL} = LOW

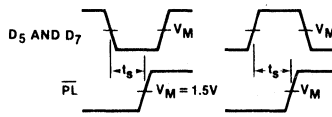
Waveform 3

CLOCK ENABLE AND SERIAL DATA SETUP AND HOLD TIMES



Waveform 4

SETUP TIMES TO ACTIVE LOW PARALLEL LOAD



Waveform 5

$V_M = 1.5V$ for 54/74 and 54/74S; $V_M = 1.3V$ for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

SHIFT REGISTER

54/74166

8-Bit Serial/Parallel-In, Serial-Out Shift Register

- Synchronous parallel to serial applications
- Synchronous serial data input for easy expansion
- Clock enable for "do nothing" mode
- Asynchronous Master Reset
- See '165 for asynchronous parallel data load

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74166	35MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74166N	
Plastic SO	N74166D	
Ceramic DIP		S54166F
Flatpack		S54166W

DESCRIPTION

The '166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable (\overline{PE}) input. When the \overline{PE} is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When \overline{PE} is HIGH, data is entered into internal bit position Q_0 from Serial Data input (D_S), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_6 input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
All	Inputs	1uI
Q_7	Output	10uI

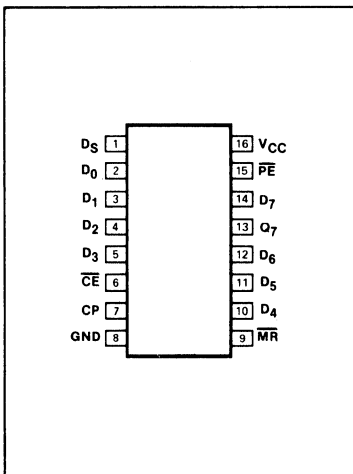
NOTE

Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

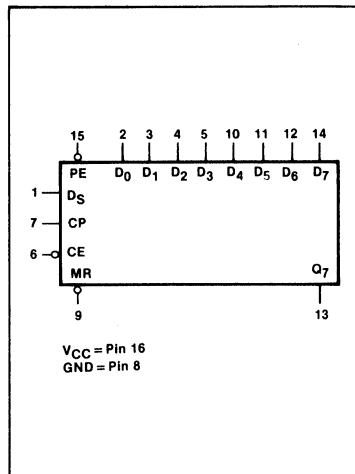
is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of \overline{CE} input should only take place while the CP is HIGH for predictable operation.

A LOW on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

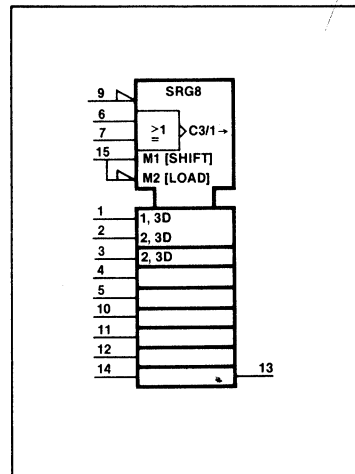
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

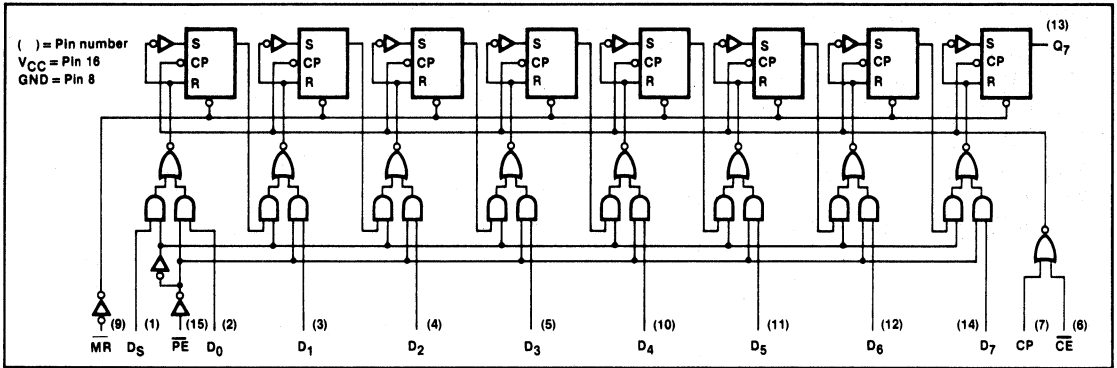


4

SHIFT REGISTER

54/74166

LOGIC DIAGRAM

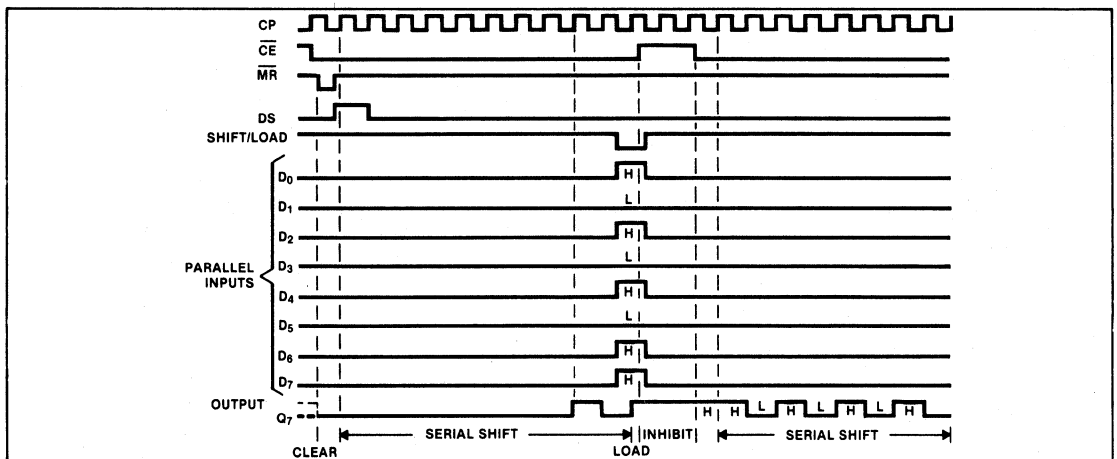


MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS				Q _n REGISTER			OUTPUT
	PE	CE	CP	D _S	D ₀ -D ₇	Q ₀	Q ₁ -Q ₆	Q ₇
Parallel Load	l	l	l	X	l-l	L	L-L	L
Serial Shift	h	l	l	l	X-X	L	q ₀ -q ₅	q ₆
Hold (do nothing)	X	h	X	X	X-X	q ₀	q ₁ -q ₆	q ₇

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
 q_n = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH Clock transition.
 X = Don't care.
 l = LOW-to-HIGH Clock transition.

TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

SHIFT REGISTER

54/74166

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 12	mA
I _{OH}	HIGH-level output current				- 800	μA
I _{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74166			UNIT	
		Min	Typ ²	Max		
V _{OH}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		V
		Com'l	2.4	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK}	V _{CC} = MIN, I _I = I _{IK}				- 1.5	V
I _I	V _{CC} = MAX, V _I = 5.5V				1.0	mA
I _{IH}	V _{CC} = MAX, V _I = 2.4V				40	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4V				- 1.6	mA
I _{OS}	V _{CC} = MAX	Mil	- 20		- 57	mA
		Com'l	- 18		- 57	mA
I _{CC}	V _{CC} = MAX		90	127		mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with 4.5V applied to the Serial Input, a momentary ground, then 4.5V applied to Clock, all other inputs grounded and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT	
		C _L = 15pF, R _L = 400Ω			
		Min	Max		
f _{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t _{PLH}	Propagation delay	Waveform 1		26	ns
t _{PHL}	Clock to output			30	ns
t _{PHL}	Propagation delay MR to output	Waveform 2		35	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

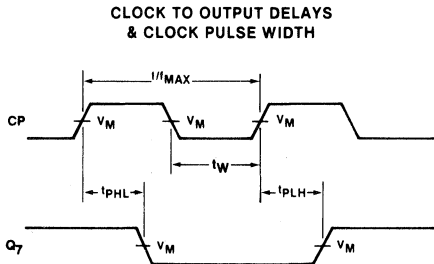
SHIFT REGISTER

54/74166

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		Min	Max	
t_W	Clock pulse width	20		ns
t_W	$\overline{\text{MR}}$ pulse width	20		ns
t_s	Setup time data to clock	20		ns
t_h	Hold time data to clock	0		ns
t_s	Setup time $\overline{\text{CE}}$ to clock	30		ns
t_h	Hold time $\overline{\text{CE}}$ to clock	0		ns
t_s	Setup time $\overline{\text{PE}}$ to clock	30		ns
t_h	Hold time $\overline{\text{PE}}$ to clock	0		ns
t_{rec}	Recovery time $\overline{\text{MR}}$ to clock	30		ns

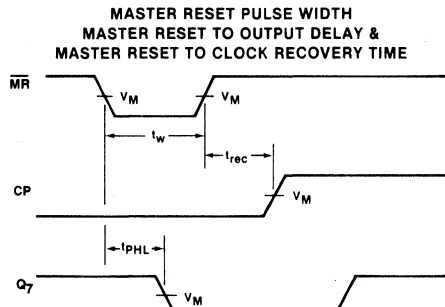
AC WAVEFORMS



$V_M = 1.5\text{V}$ for 54/74 and 54S/74S, $V_M = 1.3\text{V}$ for 54LS/74LS

The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

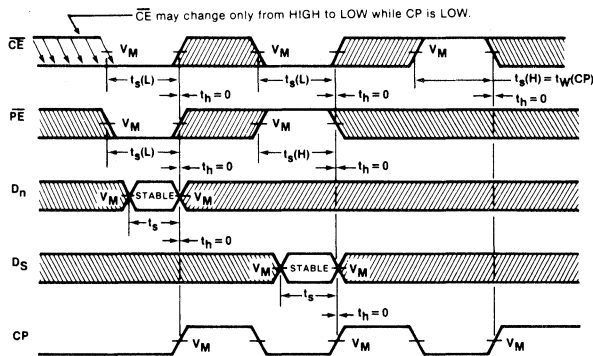
The changing output assumes internal Q_6 opposite state from Q_7 .



$V_M = 1.5\text{V}$ for 54/74 and 54S/74S, $V_M = 1.3\text{V}$ for 54LS/74LS

The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

Waveform 1



CONDITIONS; $\overline{\text{MR}} = \text{HIGH}$

$V_M = 1.5\text{V}$ for 54/74 and 54S/74S, $V_M = 1.3\text{V}$ for 54LS/74LS.

The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

The shaded areas indicate when the input is permitted to change for predictable performance.

The changing output assumes internal Q_6 opposite state from Q_7 .

Waveform 2

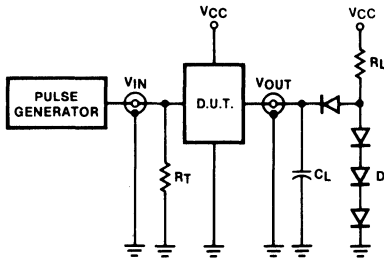
Waveform 3

SHIFT REGISTER

54/74166

TEST CIRCUITS AND WAVEFORMS

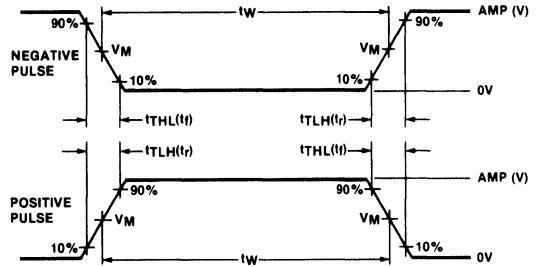
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

4-BIT BIDIRECTIONAL COUNTERS

54/74LS168A, 54/74LS169A, S168A, S169A

4-Bit Up/Down Synchronous Counter

- Synchronous counting and loading
- Up/down counting
- Modulo 16 binary counter — '169A
- BCD decade counter — '168A
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock

DESCRIPTION

The '168A is a synchronous, presettable BCD decade up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS168A	32MHz	20mA
74S168A	70MHz	100mA
74LS169A	32MHz	20mA
74S169A	70MHz	100mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS168AN • N74S168AN N74LS169AN • N74S169AN	
Plastic SO	N74LS169AD N74S168AD • N74S169AD	
Ceramic DIP		S54LS168AF • S54S168AF S54LS169AF • S54S169AF
Flatpack		S54LS168AW • S54LS169AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
\overline{PE}	Input	1Sul	2LSul
\overline{CET}	Input	2Sul	1LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE

Where a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

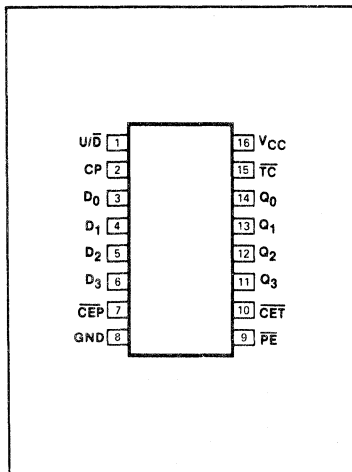
counter and causes the data at the D_n input to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

The direction of counting is controlled by the Up/Down (U/\overline{D}) input; a HIGH will

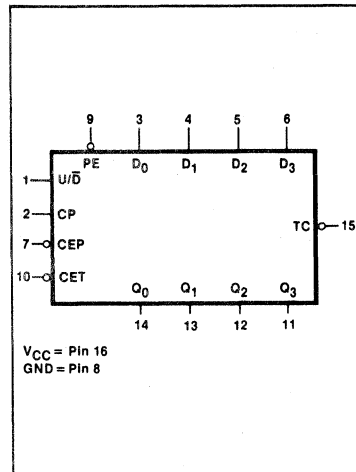
cause the count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. In-

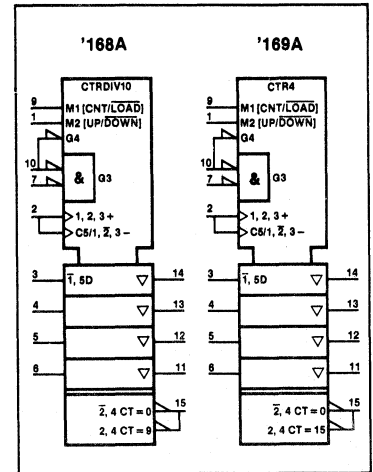
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



4-BIT BIDIRECTIONAL COUNTERS 54/74LS168A, 54/74LS169A, S168A, S169A

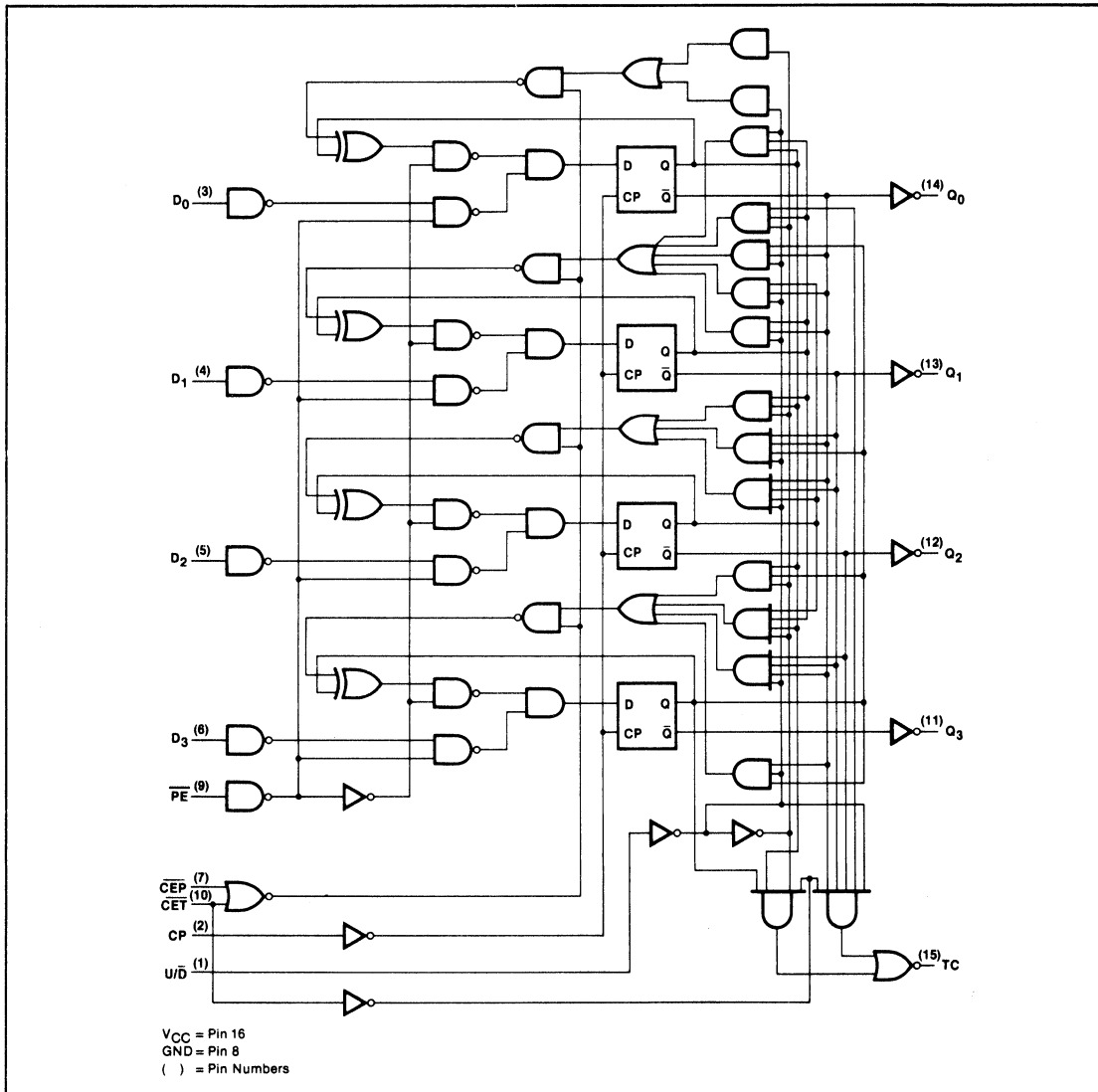
strumental in accomplishing this function are two Count Enable inputs (\overline{CET} and \overline{CEP}) and a Terminal Count (\overline{TC}) output. Both Count Enable inputs must be LOW to count. The \overline{CET} input is fed forward to en-

able the \overline{TC} output. The \overline{TC} output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level \overline{TC} pulse is used to enable suc-

cessive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

The '169A is identical except that it is a Modulo 16 counter.

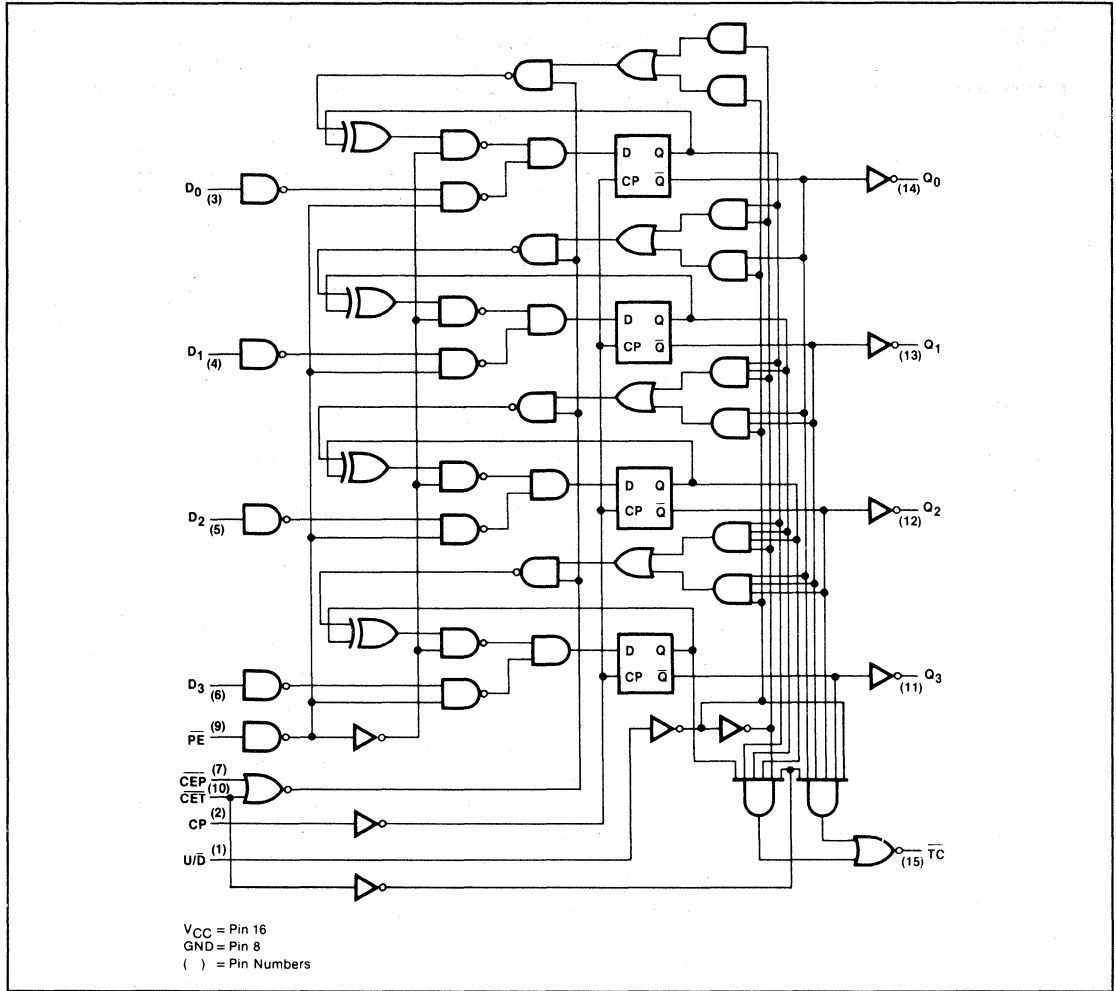
LOGIC DIAGRAM, '168A



4-BIT BIDIRECTIONAL COUNTERS

54/74LS168A, 54/74LS169A, S168A, S169A

LOGIC DIAGRAM, '169A



SYNCHRONOUS MULTISTAGE COUNTING SCHEME

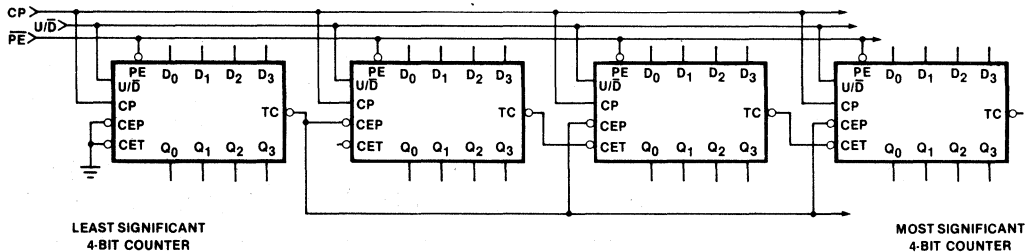


Figure A

4-BIT BIDIRECTIONAL COUNTERS

54/74LS168A, 54/74LS169A, S168A, S169A

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/D	\overline{CEP}	\overline{CET}	\overline{PE}	D _n	Q _n	\overline{TC}
Parallel Load	l	X	X	X	l	l	L	(a)
	l	X	X	X	l	h	H	(a)
Count Up	l	h	l	l	h	X	Count Up	(a)
Count Down	l	l	l	l	h	X	Count Down	(a)
Hold (do nothing)	l	X	h	X	h	X	q _n	(a)
	l	X	X	h	h	X	q _n	H

H = HIGH voltage level steady state

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L = LOW voltage level steady state

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X = Don't care

q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition

l = LOW-to-HIGH clock transition

NOTE

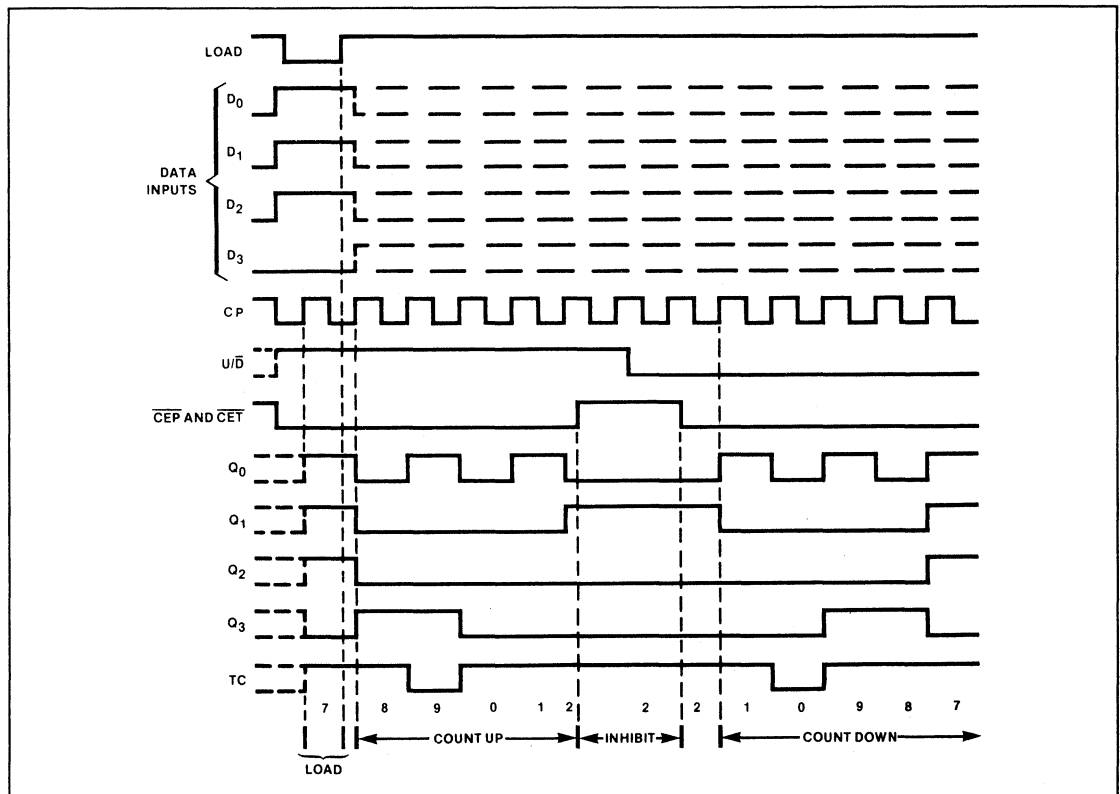
a. The \overline{TC} is LOW when \overline{CET} is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169A.

The \overline{TC} is LOW when \overline{CET} is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168A.

WAVEFORM (Typical Load, Count, and inhibit Sequences)

Illustrated below is the following sequence for the '168A. The operation of the '169A is similar.

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



4-BIT BIDIRECTIONAL COUNTERS

54/74LS168A, 54/74LS169A, S168A, S169A

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

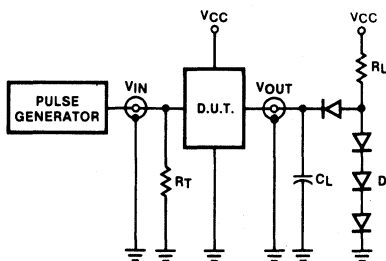
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-18			-18	mA
I _{OH} HIGH-level output current				-400			-1000	μA
I _{OL} LOW-level output current	Mil			4			20	mA
	Com'l			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

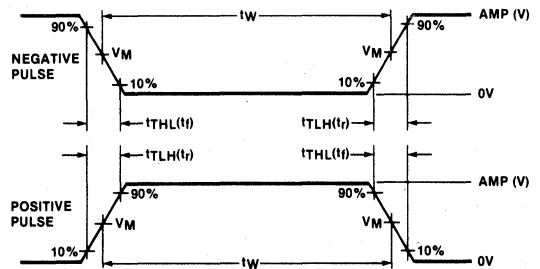
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

4-BIT BIDIRECTIONAL COUNTERS

54/74LS168A, 54/74LS169A, S168A, S169A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS168A, 169A			54/74S168A, 169A			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		2.5	3.4	V	
		Com'l	2.7	3.4		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4			0.5 ⁵	V
			Com'l		0.35	0.5			0.5
		I _{OL} = 4mA	74LS		0.25	0.4			
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}						-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						1.0	mA
		V _I = 7.0V	\overline{PE} input					0.2	mA
			Other inputs					0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	\overline{PE} input				40	-200	μ A
			\overline{CET} input				20	100	μ A
			Other inputs				20	50	μ A
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	\overline{PE} input				-0.8		mA
			Other inputs				-0.4		mA
		V _I = 0.5V	\overline{CET} input					-4.0	mA
			Other inputs					-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-20		-100	-40		mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			20	34		55	80	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - I_{CC} is measured after applying a momentary 4.5V, then ground to the Clock input with all other inputs grounded and outputs open.
 - V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S				UNIT
		C _L = 15pF R _L = 2k Ω		C _L = 15pF, R _L = 280 Ω U/D = HIGH		C _L = 15pF, R _L = 280 Ω U/D = LOW		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		40		40		MHz
t _{PLH} Propagation delay t _{PHL} Clock to Q output	Waveform 1	20	23	12	15	12	15	ns
t _{PLH} Propagation delay t _{PHL} Clock to TC	Waveform 1	35	35	17	25	15	25	ns
t _{PLH} Propagation delay t _{PHL} \overline{CET} to TC	Waveform 2	14	14	11	15	11	15	ns
t _{PLH} Propagation delay t _{PHL} U/D control to TC ^(b)	Waveform 3	25	29	15	15	10	20	ns

- NOTE
- Propagation delay time from up/down to terminal count must be measured with the counter at either a minimum or a maximum count. As the logic level of the Up/Down Input is changed, the Terminal Count output will follow. If the count is minimum (0), the Terminal Count output transition will be in phase. If the count is maximum (9 for 168A or 15 for 169A), the Terminal Count output will be out of phase.
- Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

4

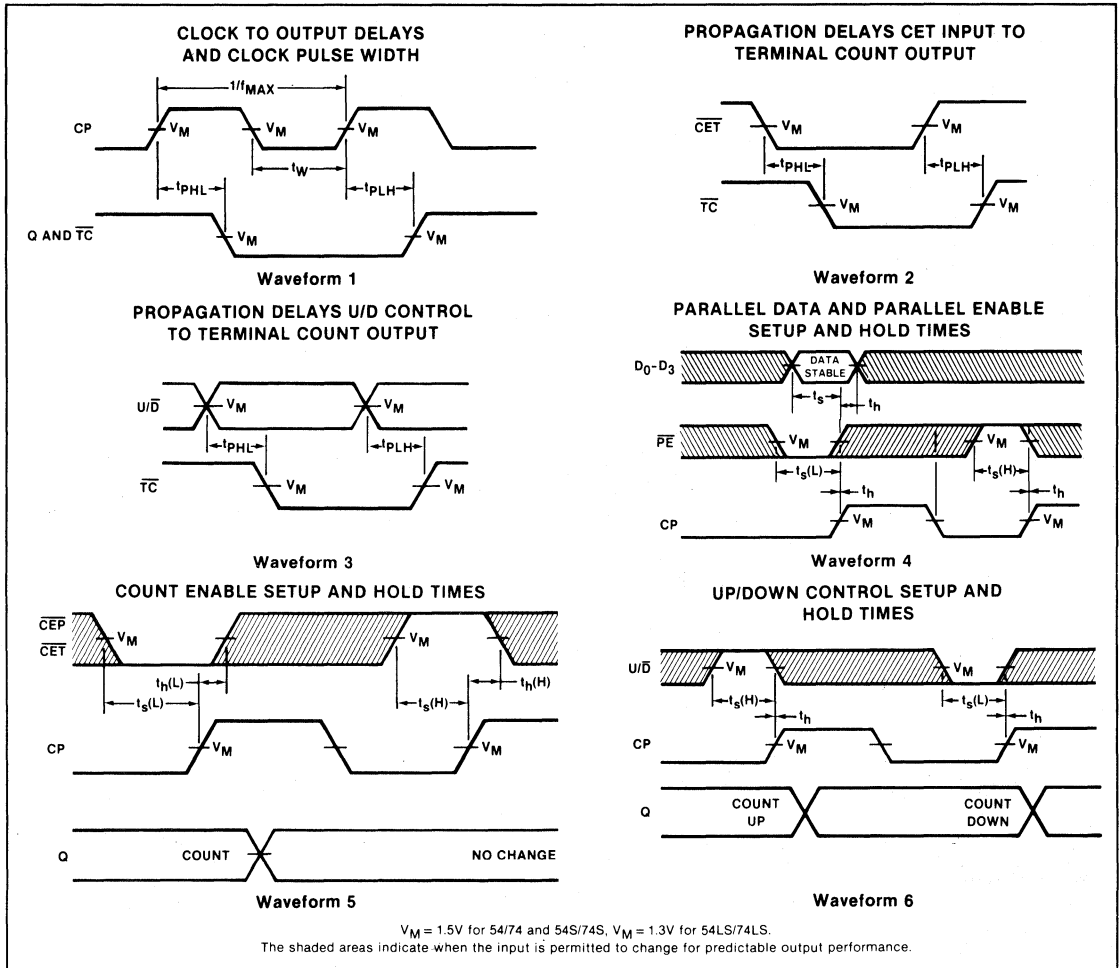
4-BIT BIDIRECTIONAL COUNTERS

54/74LS168A, 54/74LS169A, S168A, S169A

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		Min	Max	Min	Max	
t_W Clock pulse width	Waveform 1	25		10		ns
t_s Setup time, data to clock	Waveform 4	20		6		ns
t_h Hold time, data to clock	Waveform 4	0		1		ns
t_s Setup time, \overline{PE} to clock	Waveform 4	25		9		ns
t_h Hold time, \overline{PE} to clock	Waveform 4	0		0		ns
t_s Setup time, \overline{CEP} & \overline{CET} to clock	Waveform 5	20		16		ns
t_h Hold time, \overline{CEP} & \overline{CET} to clock	Waveform 5	0		0		ns
t_s Setup time, U/\overline{D} to clock	Waveform 6	30		20		ns
t_h Hold time, U/\overline{D} to clock	Waveform 6	0		0		ns

AC WAVEFORMS



4 x 4 Register File (Open Collector)

- Simultaneous and independent Read and Write operations
- Expandable to 1024 words by n-bits
- Open Collector outputs for wired-AND expansion
- See '670 for 3-State output version

TYPE	TYPICAL PROPAGATION DELAY (RE to Q)	TYPICAL SUPPLY CURRENT (Total)
74170	10ns (t _{PLH}) 20ns (t _{PHL})	127mA
74LS170	20ns (t _{PLH}) 20ns (t _{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	MILITARY RANGES V _{CC} = 5V ± 10%; T _A = - 55°C to + 125°C
Plastic DIP	N74170N • N74LS170N	

DESCRIPTION

The '170 is a 16-bit register file organized as 4 words of 4 bits each, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable (WE) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the WE is LOW. Data supplied at the inputs will be read out in true (non-inverting) form. Data and Write Address inputs are inhibited when WE is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable (RE) is

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
D, W _A , W _B , R _A , R _B	Inputs	1uI	1LSuI
WE, RE	Inputs	1uI	2LSuI
All	Outputs	10uI	10LSuI

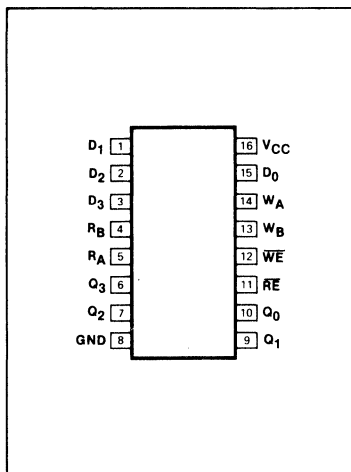
NOTE

Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and - 1.6mA I_{IL} and a 54/74LS unit load (LSuI) is 20µA I_{IH} and - 0.4mA I_{IL}.

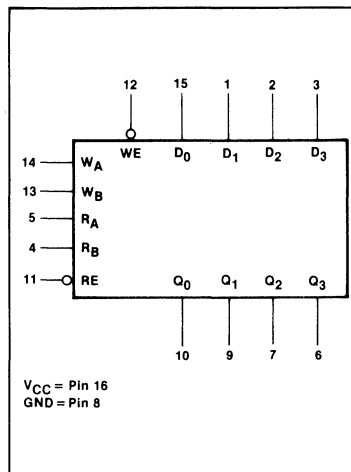
LOW. Data outputs are inhibited and remain HIGH when the Read Enable input is HIGH. This permits simultaneous reading and writing, eliminates recovery times, and is limited in speed only by the read time and the write time.

Up to 256 devices can be stacked to increase the word size to 1024 locations by tying the Open Collector outputs together. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

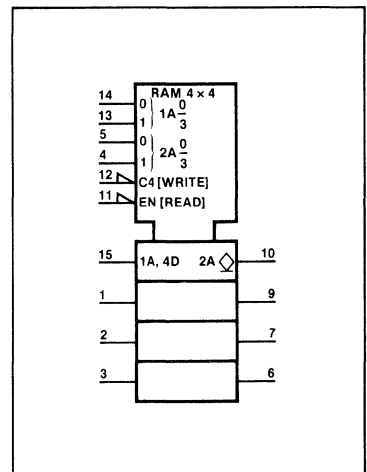
PIN CONFIGURATION



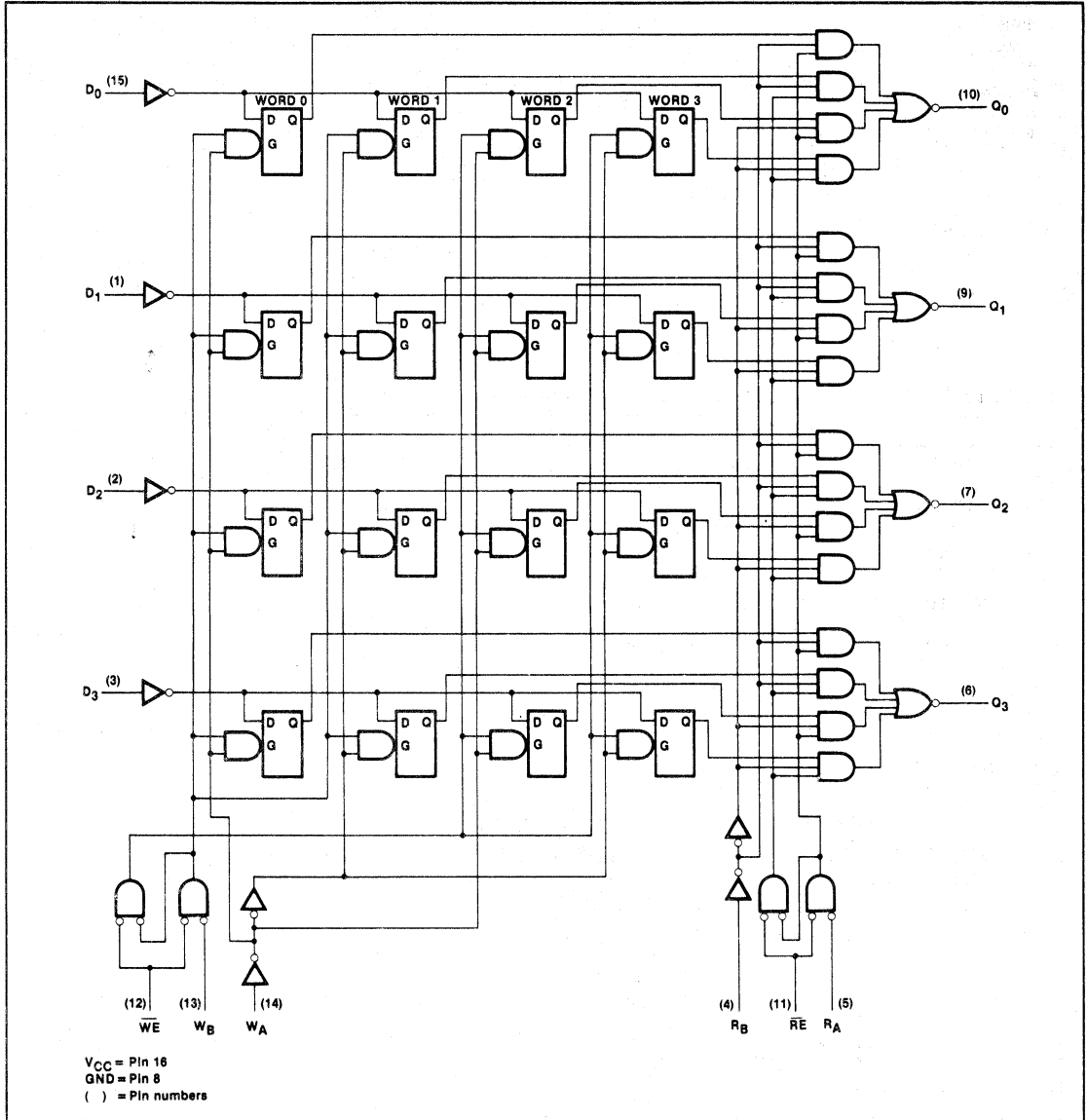
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES ^(a)
	\overline{WE}	D_n	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS Q_n
	\overline{RE}	INTERNAL LATCHES ^(b)	
Read	L	L	L
	L	H	H
Disabled	H	X	H

H = HIGH voltage level

L = LOW voltage level

X = Don't care

NOTES

a. The Write Address (W_A and W_B) to the "Internal latches" must be stable while \overline{WE} is LOW for conventional operation.

b. The selection of the "Internal latches" by Read Address (R_A and R_B) are not constrained by \overline{WE} or \overline{RE} operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

4

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-12			-18	mA
V_{OH} HIGH-level output voltage				5.5			5.5	V
I_{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

REGISTER FILES

54/74170, LS170

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74170			54/74LS170			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
I _{OH} HIGH-level output current	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 5.5V			30			100	μA	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.2	0.4		0.25	0.4	V
			Com'l	0.2	0.4		0.35	0.5	V
			I _{OL} = 4mA				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V	D, W _A , W _B , R _A , R _B inputs				0.1	mA	
			\overline{WE} , \overline{RE} inputs				0.2	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40			μA	
		V _I = 2.7V	D, W _A , W _B , R _A , R _B inputs				20	μA	
			\overline{WE} , \overline{RE} inputs				40	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	D, W _A , W _B , R _A , R _B inputs			-1.6		-0.4	mA	
		\overline{WE} , \overline{RE} inputs			-1.6		-0.8	mA	
I _{CC} Supply current ³ (total)	V _{CC} = MAX	Mil		127	140		25	40	mA
		Com'l		127	150		25	40	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Measure I_{CC} with 4.5V applied to all Data and both Enable inputs, the Address inputs grounded and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

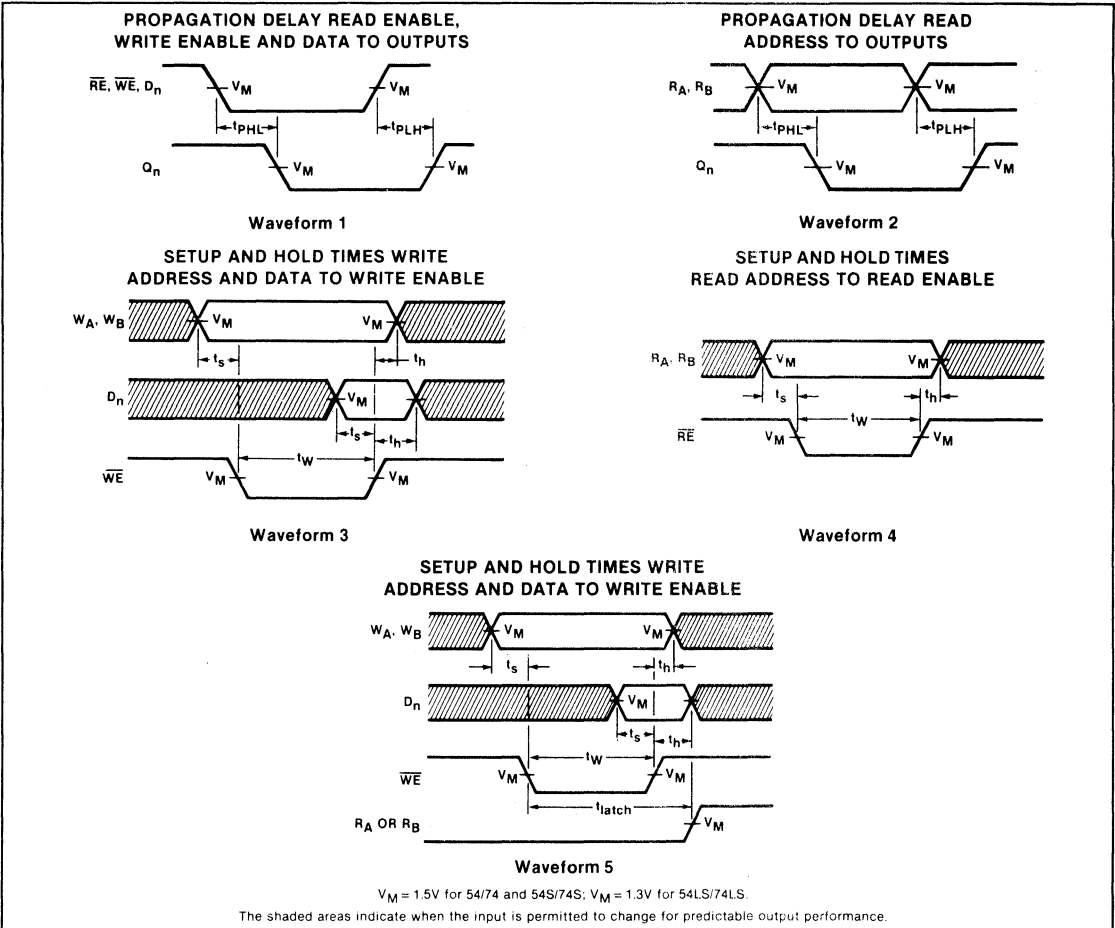
PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT	
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ			
		Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation delay Read Enable to output	Waveform 1			15 30	30 30	ns
t _{PLH} t _{PHL}	Propagation delay Read Address to output	Waveform 2			35 40	40 40	ns
t _{PLH} t _{PHL}	Propagation delay Write Enable to output	Waveform 1			40 45	45 40	ns
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 1			30 45	45 35	ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		Min	Max	Min	Max	
t_W Write Enable pulse width	Waveform 3	25		25		ns
t_s Setup time, Data to positive-going $\overline{WE}^{(c)}$	Waveform 3	10		10		ns
t_h Hold time, Data to positive-going $\overline{WE}^{(c)}$	Waveform 3	15		15		ns
t_s Setup time, Read Address to negative-going $\overline{WE}^{(c)}$	Waveform 3	15		15		ns
t_h Hold time, Read Address to positive-going $\overline{WE}^{(c)}$	Waveform 3	5.0		5.0		ns
t_W Read Enable pulse width	Waveform 4	25		25		ns
t_{latch} Latch time for new data ^(d)	Waveform 5	25		25		ns

- NOTES
- c. Write Address setup time will protect the data written into the previous address. If protection of data in the previous address is not required, t_s (Write Address to \overline{WE}) can be ignored, as any address selection sustained for the final 30ns of the \overline{WE} pulse and during t_h (Write Address to \overline{WE}) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
 - d. Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of \overline{WE} to the rising edge of R_A or R_B . \overline{RE} must be LOW.

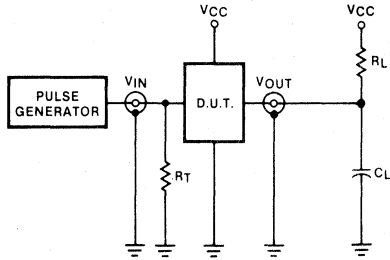
AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS

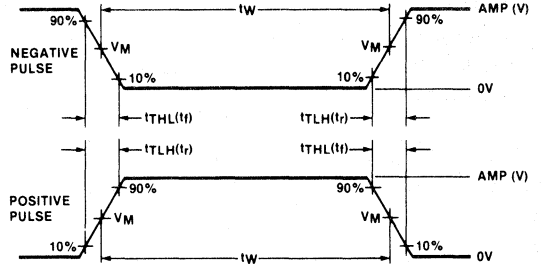
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

16-Bit Multiple Port Register File (3-State)

- Simultaneous and Independent Read and Write operations
- Expandable to 1024 words on n-bits
- 3-State outputs

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74S172	40MHz	160mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S172N	

DESCRIPTION

The '172 is a high-performance, 16-bit multiport register file with 3-State outputs organized as eight words of two bits each. Multiple address decoding circuitry is used so that the read and write operation can be performed independently on up to three word locations. Data can be written into two word locations through Input Port "A" or Input Port "C" while data is simultaneously read from both output Port "B" and output Port "C".

Port "A" is an input port which can be used to write two bits of data (D_{A0} , D_{A1}) into one of eight register locations selected by the Address inputs (A_{A0} , A_{A1} , A_{A2}). When the Write Enable (WE_A) input is LOW one setup time prior to the LOW-to-HIGH transition of the Clock (CP) input, the data is written into the selected location.

Port "B" is an output port which can be used to read two bits of data from one of eight register locations selected by the Address inputs (A_{B0} , A_{B1} , A_{B2}). When the Read Enable (RE_B) is LOW, the selected 2-bit word appears on outputs Q_{B0} and Q_{B1} . When RE_B is HIGH, the Q_{B0} and Q_{B1}

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
All	Inputs	1Sul
All	Outputs	8Sul

NOTE
A 54/74S unit load (Sul) is 50 μ A and I_{IH} and $-2.0mA$ I_{IL} .

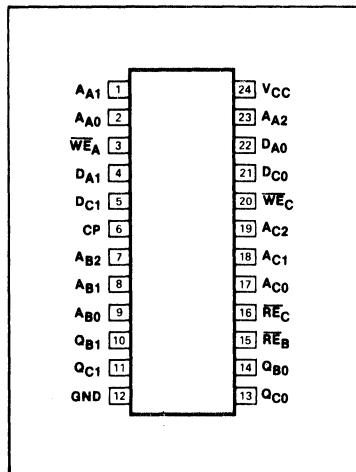
outputs are in the HIGH impedance "off" state. The read operation is independent of the clock.

Port "C" is a read/write port that has separate Data input and Data output sections, but common Address inputs (A_{C0} , A_{C1} , A_{C2}). Data can be simultaneously written into and read from the same register location. Port "C" can be used to write data into one location while Port "A" is writing into a different location, but data cannot be written reliably into the same location simultaneously.

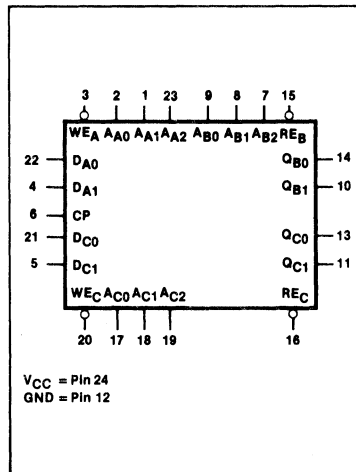
If both Ports "A" and "C" are enabled for writing into the same location during the same clock cycle, the LOW data will predominate if there is a conflict.

The register operation is essentially a master-slave flip-flop. Each master acts as a transparent D latch when selected by the "A" or "C" address and the clock and applicable write enable are LOW. The data in the master is transferred to the slave (or output section) following the LOW-to-HIGH transition of the Clock (CP). The Address inputs must be stable while the

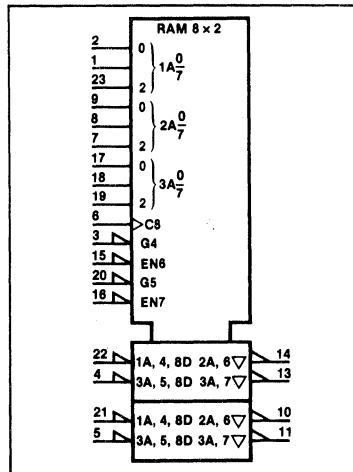
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



4

REGISTER FILE

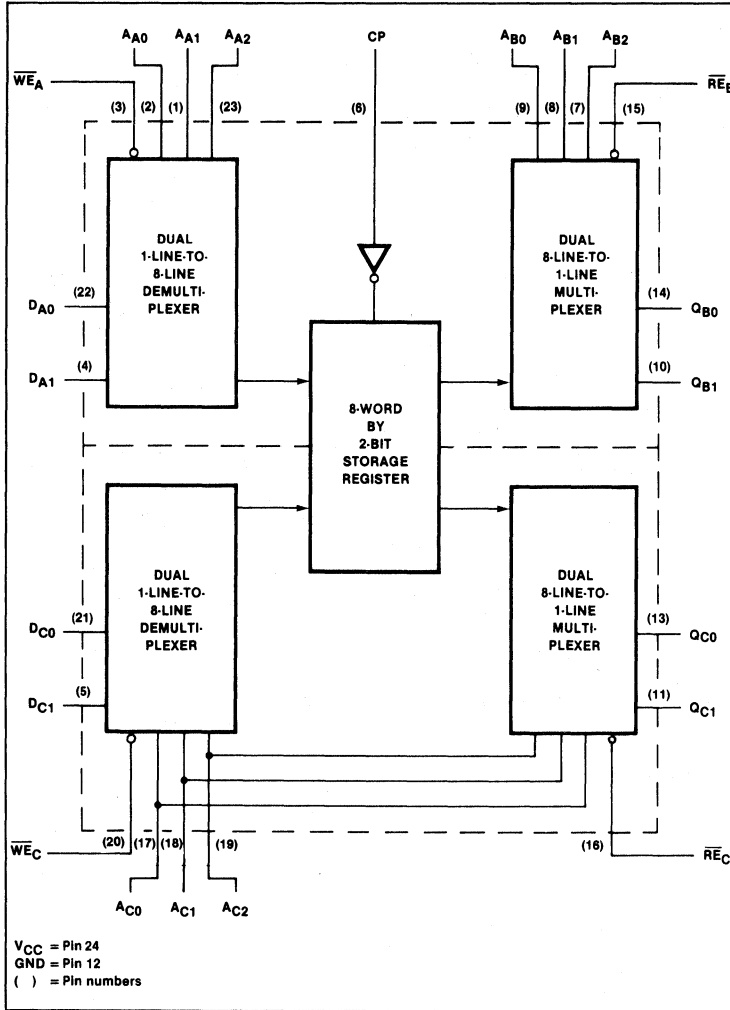
74S172

Clock and Write Enable inputs are LOW to ensure retention of data previously written into the other locations. Any number of

masters can be altered while the clock and write enable are LOW, but the new data will not be loaded into the slaves, or be

available at the outputs, until the clock goes HIGH.

BLOCK DIAGRAM



WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS			ADDRESSED REGISTER
	CP	\overline{WE}	D_n	
Write Data ^(a)	l	l	l	L
	t	l	h	H
Hold ^(b)	l	h	X	no change

READ MODE SELECT TABLE

OPERATING MODE	\overline{RE}	ADDRESSED REGISTER	OUTPUTS
			Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH or HIGH-to-LOW clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 (Z) = HIGH impedance (off) state.
 t = LOW-to-HIGH clock transition.
 † = HIGH-to-LOW clock transition.

NOTES

- The Write Address (A_n and A_c) to the "internal register" must be stable while \overline{WE} and CP are LOW for conventional operation.
- The Write Enable must be HIGH before the HIGH-to-LOW clock transition to ensure that the data in the register is not changed.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74S	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74S			UNIT
			Min	Nom	Max	
V _{CC}	Supply voltage	Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 12	mA
I _{OH}	HIGH-level output current				- 5.2	mA
I _{OL}	LOW-level output current	Com'l			20	mA
T _A	Operating free-air temperature	Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74S172			UNIT
		Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX			V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX			V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			V
I _{OZH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.4V			μA
I _{OZL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.4V			μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.4V			μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V	CP, WE _A , WE _C , A _{CO} -A _{C2}	-1.6	mA
			Other inputs	-0.8	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX			mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX			mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_O = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with all inputs at 4.5V and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74S		UNIT
		C _L = 50pF, R _L = 400Ω		
		Min	Max	
f _{MAX}	Maximum clock frequency	Waveform 1		MHz
t _{PLH}	Propagation delay	Waveform 2		ns
t _{PHL}	Address (B or C) to output	Waveform 2		ns
t _{PLH}	Propagation delay	Waveform 1		ns
t _{PHL}	Clock to output	Waveform 1		ns
t _{PZH}	Read enable time to HIGH	Waveform 3		ns
t _{PZL}	Read enable time to LOW	Waveform 4		ns
t _{PHZ}	Disable time from HIGH	Waveform 3, C _L = 5pF		ns
t _{PLZ}	Disable time from LOW	Waveform 4, C _L = 5pF		ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.



AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74S		UNIT
		Min	Max	
t_w Clock pulse width	Waveform 1	25		ns
t_s Setup time, Write Address (A or C) to negative-going Clock and \overline{WE}	Waveform 5	15		ns
t_h Hold time, Write Address (A or C) to positive-going Clock and \overline{WE}	Waveform 5	0		ns
$t_s(H)$ Setup time, HIGH Data to Clock	Waveform 5	30		ns
$t_h(H)$ Hold time, HIGH Data to Clock	Waveform 5	0		ns
$t_s(L)$ Setup time, LOW Data to Clock	Waveform 5	20		ns
$t_h(L)$ Hold time, LOW Data to Clock	Waveform 5	0		ns
t_s Setup time, LOW \overline{WE} to positive-going Clock	Waveform 6	35		ns
t_h Hold time, LOW \overline{WE} to positive-going Clock	Waveform 6	0		ns
t_s Setup time, HIGH \overline{WE} to negative-going Clock	Waveform 6	10		ns
t_h Hold time, HIGH \overline{WE} to positive-going Clock	Waveform 6	0		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = $1k\Omega$ for 54/74, 54S/74S, $5k\Omega$ for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

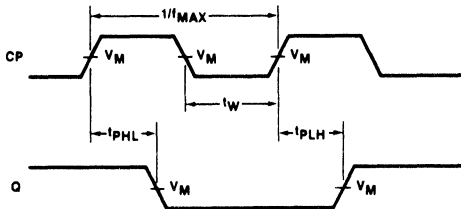
INPUT PULSE DEFINITIONS

$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

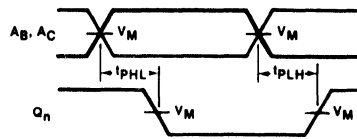
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



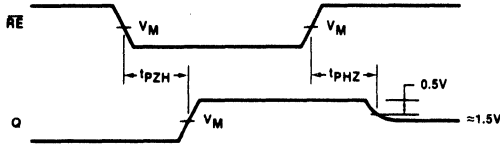
Waveform 1

PROPAGATION DELAY READ ADDRESS TO OUTPUTS



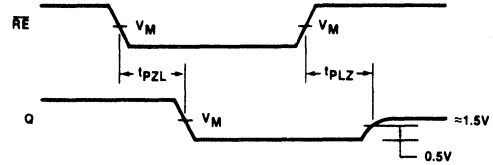
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



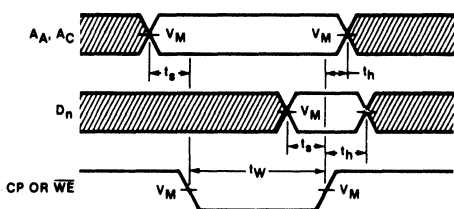
Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



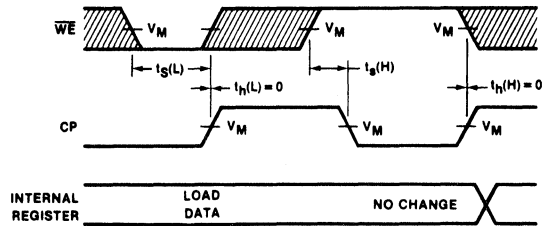
Waveform 4

SETUP AND HOLD TIMES WRITE ADDRESS AND DATA TO WRITE ENABLE



Waveform 5

WRITE ENABLE SETUP AND HOLD TIMES



Waveform 6

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

4

FLIP-FLOPS

54/74173, LS173

Quad D-Type Flip-Flop With 3-State Outputs

- Edge-triggered D-type register
- Gated input enable for hold "do nothing" mode
- 3-State output buffers
- Gated output enable control
- Pin compatible with the 8T10 and DM8551

DESCRIPTION

The '173 is a 4-bit parallel load register with clock enable control, 3-State buffered outputs and master reset. When the two Clock Enable (\bar{E}_1 and \bar{E}_2) inputs are LOW, the data on the D inputs is loaded into the register synchronously with the LOW-to-HIGH Clock (CP) transition. When one or both \bar{E} inputs are HIGH one setup time before the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and Clock Enable inputs are fully edge triggered and must be stable only one setup time before the LOW-to-HIGH clock transition.

The Master Reset (MR) is an active HIGH asynchronous input. When the MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74173	35MHz	50mA
74LS173	50MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74173N • N74LS173N	
Plastic SO	N74LS173D	
Ceramic DIP		S54LS173F
Flatpack		S54LS173W
LLCC		S54LS173G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

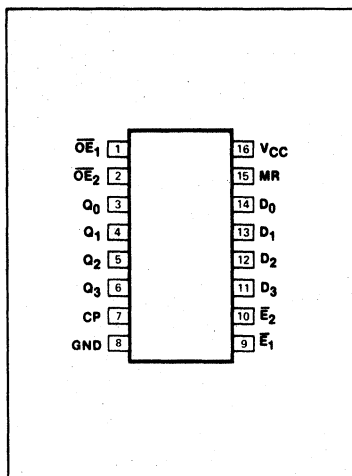
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1uI	1LSuI
All	Outputs	10uI	30LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$ and a 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

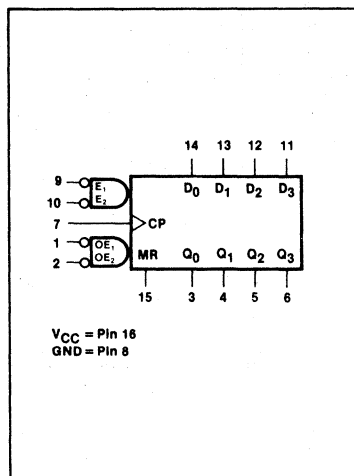
The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable (\bar{OE}_1 and \bar{OE}_2) inputs are LOW, the data in the register is presented at the Q outputs. When one or both \bar{OE} inputs is

HIGH, the outputs are forced to a HIGH impedance "off" state. The 3-State output buffers are completely independent of the register operation; the \bar{OE} transition does not affect the clock and reset operations.

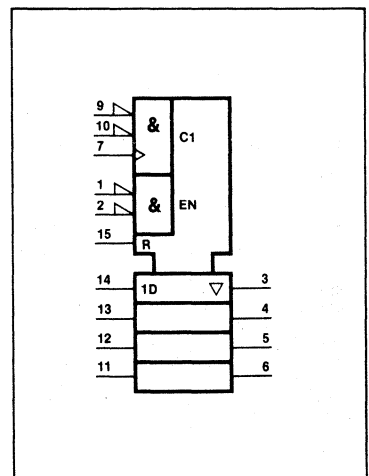
PIN CONFIGURATION



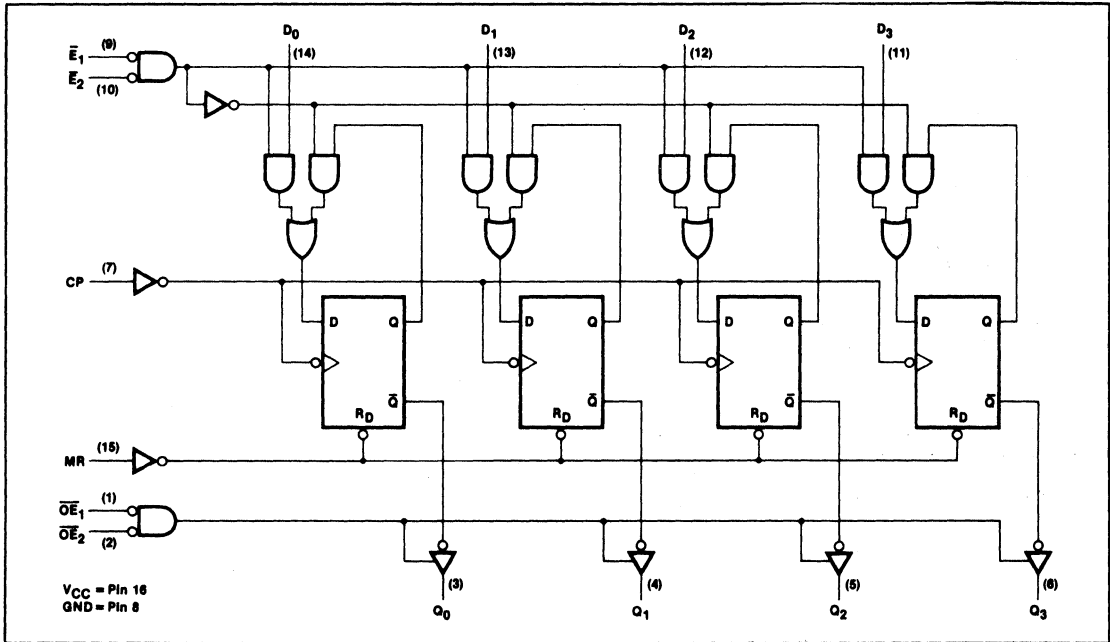
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



4

MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	\bar{E}_1	\bar{E}_2	D_n	Q_n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (no change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS	
	Q_n (Register)		\bar{OE}_1	\bar{OE}_2	Q_0, Q_1, Q_2, Q_3
Read	L	L	L	L	L
	H	L	L	L	H
Disabled	X	X	H	X	(Z)
	X	X	X	H	(Z)

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 q_n = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 (Z) = HIGH impedance "off" state.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

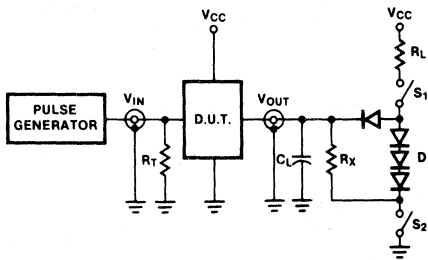
PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18	mA
I _{OH} HIGH-level output current	Mil			-2.0			-1.0	mA
	Com'l			-5.2			-2.6	mA
I _{OL} LOW-level output current	Mil			16			12	mA
	Com'l			16			24	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



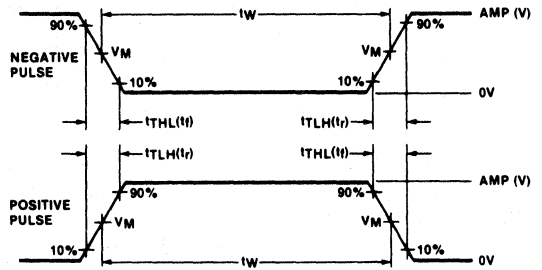
SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOPS

54/74173, LS173

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74173			54/74LS173			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4			2.4	3.4		V
		Com'l	2.4			2.4	3.1		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.4		0.25	0.4	V
			Com'l		0.4		0.35	0.5	V
		I _{OL} = 12mA	74LS				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.4V			40				μA
		V _O = 2.7V					20		μA
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 0.4V				-40			-20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA
		V _I = 7.0V					0.1		mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40				μA
		V _I = 2.7V					20		μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-30		-70	-30		-130	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			50	72		20	30	mA

- NOTES
 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 2. All typical values are at V_{CC} = 5V, T_A = 25°C.
 3. I_{OS} is tested with V_{OUT} = +0.5V, and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 4. Measure I_{CC} with MR grounded following momentary connection to 4.5V, \overline{OE}_2 , \overline{E}_1 , \overline{E}_2 and all Data inputs grounded, CP and \overline{OE}_1 at 4.5V, and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C _L = 50pF, R _L = 400Ω		C _L = 45pF, R _L = 667Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		30		MHz
t _{PLH} Propagation delay	Waveform 1		43		25	ns
t _{PHL} Clock to output			31		30	
t _{PHL} Propagation delay, MR to output	Waveform 4		27		35	ns
t _{PZH} Output enable to HIGH level	Waveform 2		30		23	ns
t _{PZL} Output enable to LOW level	Waveform 3		30		27	ns
t _{PHZ} Output disable from HIGH level	Waveform 2, C _L = 5pF		14		17	ns
t _{PLZ} Output disable from LOW level	Waveform 3, C _L = 5pF		20		17	ns

NOTE
 Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

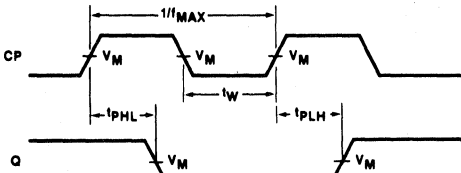
AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		Min	Max	Min	Max	
t _w (CP) Clock pulse width	Waveform 1	20		20		ns
t _w (MR) MR pulse width	Waveform 4	20		20		ns
t _s (D) Setup time, Data to Clock	Waveform 5	10		17		ns
t _h (D) Hold time, Data to Clock	Waveform 5	10		0		ns
t _s (\overline{E}) Setup time, Enable to Clock	Waveform 5	17		35		ns
t _h (\overline{E}) Hold time, Enable to Clock	Waveform 5	2		0		ns
t _{rec} (MR) Recovery time, Master Reset to Clock	Waveform 4	10		17		ns

4

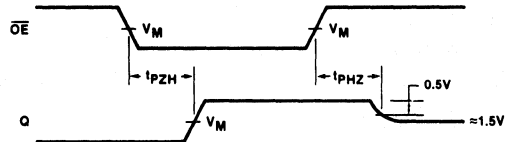
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



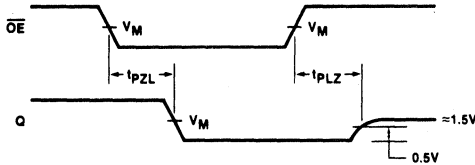
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



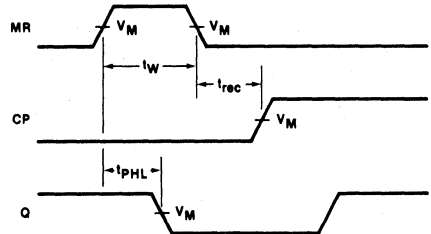
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



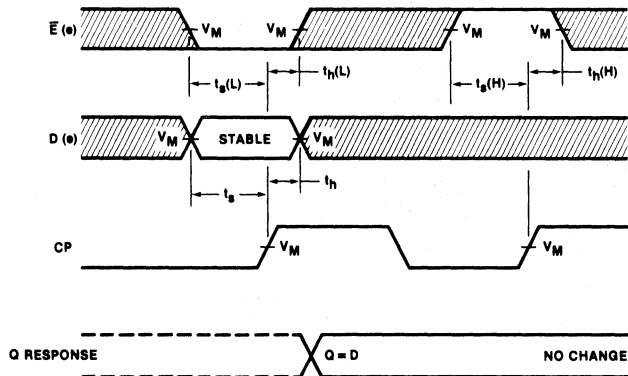
Waveform 3

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 4

SETUP (t_s) AND HOLD (t_h) TIMES FOR DATA (D) AND ENABLE (E) INPUTS



Waveform 5

$V_M = 1.5V$ for 54/74 and 54/74S; $V_M = 1.3V$ for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

FLIP-FLOPS

54/74174, LS174, S174

Hex D Flip-Flops

- Six edge-triggered D-type flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74174	35MHz	45mA
74LS174	40MHz	16mA
74S174	110MHz	90mA

DESCRIPTION

The '174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74174N • N74LS174N N74S174N	
Plastic SO	N74LS174D N74S174D	
Ceramic DIP		S54174F • S54LS174F S54S174F
Flatpack		S54174W • S54LS174W S54S174W
LLCC		S54S174G • S54LS174G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

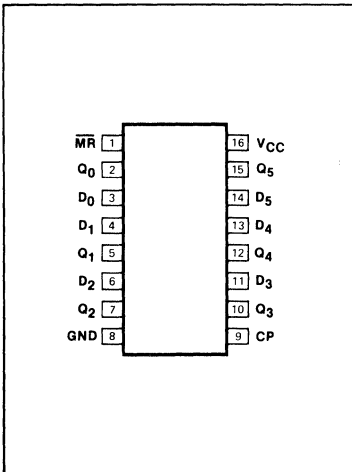
PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1uI	1Sul	1LSul
Q_0 - Q_5	Outputs	10uI	10Sul	10LSul

NOTE

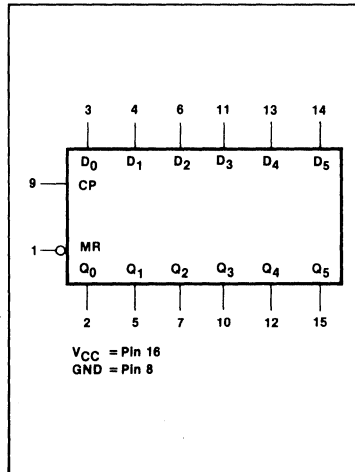
Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .



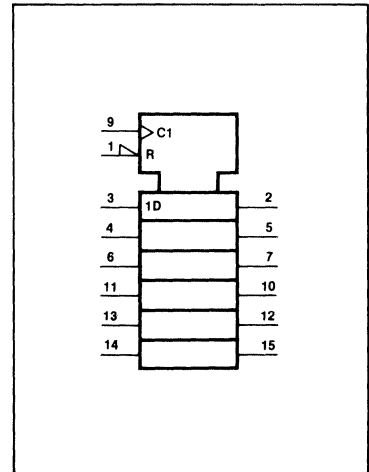
PIN CONFIGURATION



LOGIC SYMBOL



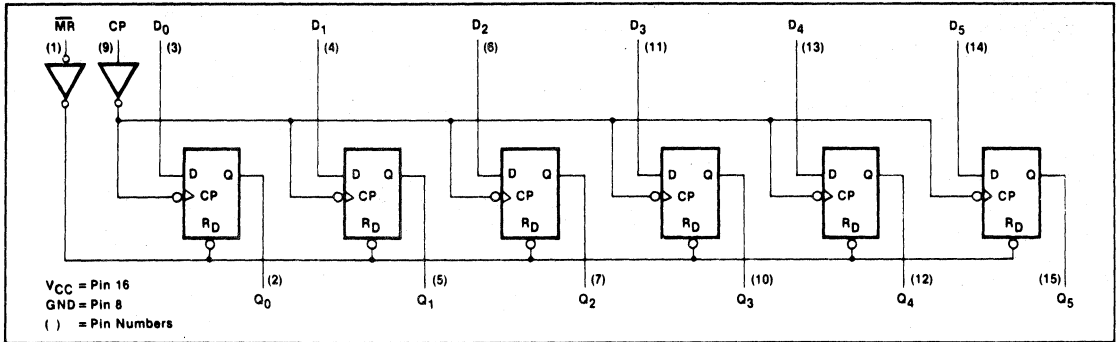
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/74174, LS174, S174

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	\overline{MR}	CP	D _n	Q _n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↓	l	L

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-
to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-
to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			2.0			V	
V _{IL}	LOW-level input voltage	Mil	+0.8			+0.7			+0.8			V
		Com'l	+0.8			+0.8			+0.8			V
I _{IK}	Input clamp current	-12			-18			-18			mA	
I _{OH}	HIGH-level output current	-800			-400			-1000			μA	
I _{OL}	LOW-level output current	Mil	16			4			20			mA
		Com'l	16			8			20			mA
T _A	Operating free-air temperature	Mil	-55	+125	-55	+125	-55	+125	-55	+125	°C	
		Com'l	0	70	0	70	0	70	0	70	°C	

NOTE
V_{IL} = +0.7V MAX for 54S at +125°C only.

FLIP-FLOPS

54/74174, LS174, S174

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74174			54/74LS174			54/74S174			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Min	2.4	3.4		2.5	3.4		2.5	3.4	V
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.25	0.4		0.5 ⁵	V
		Com'l		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA	74LS				0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5				-1.5		-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA
		V _I = 7.0V						0.1			mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA
		V _I = 2.7V						20		50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA
		V _I = 0.5V								-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Min	-20		-57	-20		-100	-40	-100	mA
		Com'l	-18		-57	-20		-100	-40	-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		45	65		16	26		90	144	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured after a momentary ground, then 4.5V is applied to Clock, with 4.5V applied to all Data and \overline{MR} inputs and all outputs open.
- V_{OL} = +0.45V MAX for 54S at +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

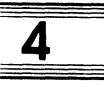
PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		30		75		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 1		30		30		13	ns
			35		30		17	
t _{PHL} Propagation delay \overline{MR} to output	Waveform 3		35		35		22	ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		Min	Max	Min	Max	Min	Max	
t _{W(L)} Clock pulse width (LOW)	Waveform 1	20		20		7.0		ns
t _W Master Reset pulse width	Waveform 3	20		20		10		ns
t _s Setup time, data to CP	Waveform 2	20		20		5.0		ns
t _h Hold time, data to CP	Waveform 2	5		5		3.0		ns
t _{rec} Recovery time, \overline{MR} to CP	Waveform 3	25		25		5.0		ns

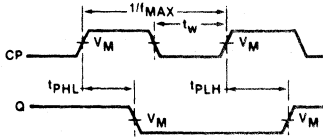


FLIP-FLOPS

54/74174, LS174, S174

AC WAVEFORMS

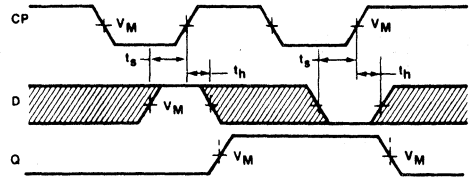
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS

Waveform 1

DATA SET-UP AND HOLD TIMES

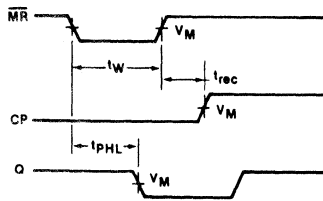


$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance

Waveform 2

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

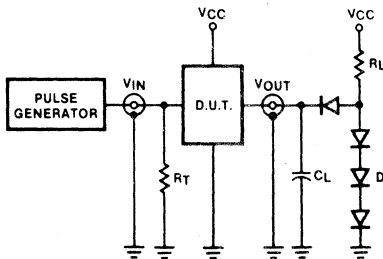


$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.

Waveform 3

TEST CIRCUITS AND WAVEFORMS

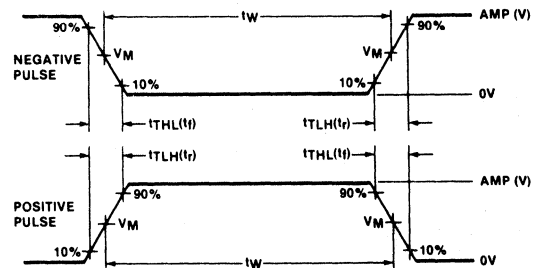
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS, $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOPS

54/74175, LS175, S175

Quad D Flip-Flop

- Four edge-triggered D flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74175	35MHz	30mA
74LS175	40MHz	11mA
74S175	110MHz	60mA

DESCRIPTION

The '175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and \bar{Q} outputs. The common buffered Clock (CP) and Master Reset (\bar{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \bar{MR} input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74175N • N74LS175N N74S175N	
Plastic S0	N74LS175D • N74S175D	
Ceramic DIP		S54175F • S54LS175F
Flatpack		S54175W • S54LS175W
LLCC		S54LS195G

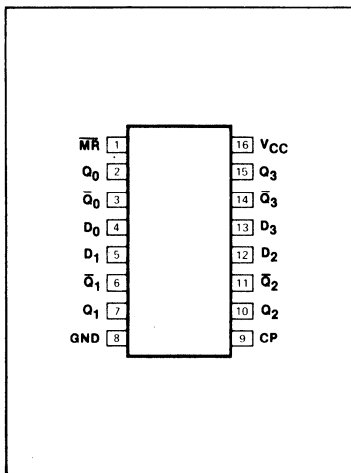


INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

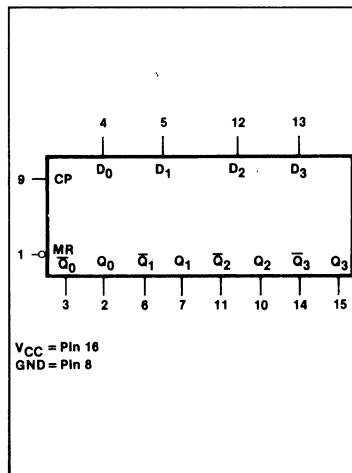
PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

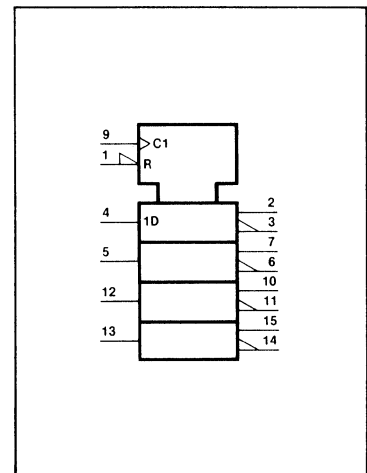
PIN CONFIGURATION



LOGIC SYMBOL



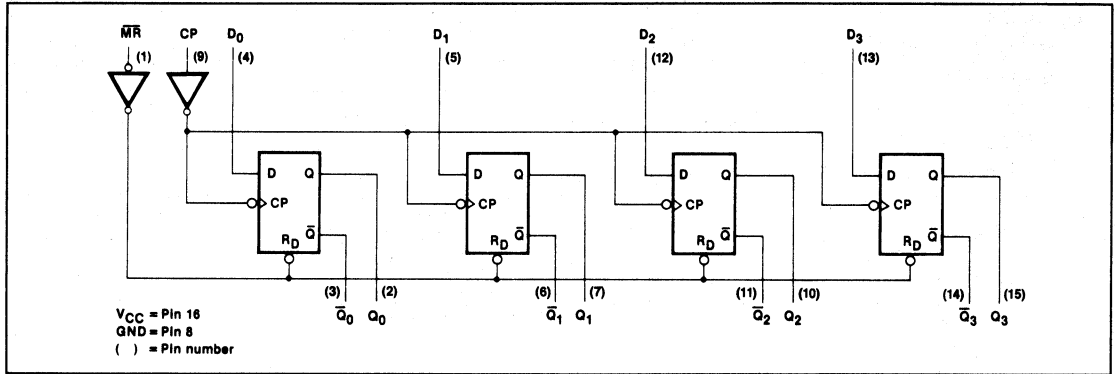
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/74175, LS175, S175

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	\overline{MR}	CP	D _n	Q _n	\overline{Q}_n
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74			54/74LS			54/74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
	Com'l			+0.8			+0.8			+0.8	V
I _{IK} Input clamp current				-12			-18			-18	mA
I _{OH} HIGH-level output current				-800			-400			-1000	μA
I _{OL} LOW-level output current	Mil			16			4			20	mA
	Com'l			16			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	0		70	°C

FLIP-FLOPS

54/74175, LS175, S175

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74175			54/74LS175			54/74S175			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4		V	
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5	V
			Com'l			0.2	0.4		0.35	0.5			0.5
		I _{OL} = 4mA	74LS						0.25	0.4			
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5				-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0							1.0	mA
		V _I = 7.0V						0.1					mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40								μA
		V _I = 2.7V						20				50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4					mA
		V _I = 0.5V										-2.0	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-57	-20		-100	-40		-100	mA	
		Com'l	-18		-57	-20		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			30	45		11	18		60	96	mA	

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - With all outputs open and 4.5V applied to all Data and Master Reset inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		30		75		MHz
t _{PLH} Propagation delay t _{PFL} Clock to outputs	Waveform 1		30 35		25 25		12 17	ns
t _{PLH} Propagation delay t _{PFL} MR to outputs	Waveform 3		25 35		30 30		15 22	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_I, t_I, pulse width or duty cycle.

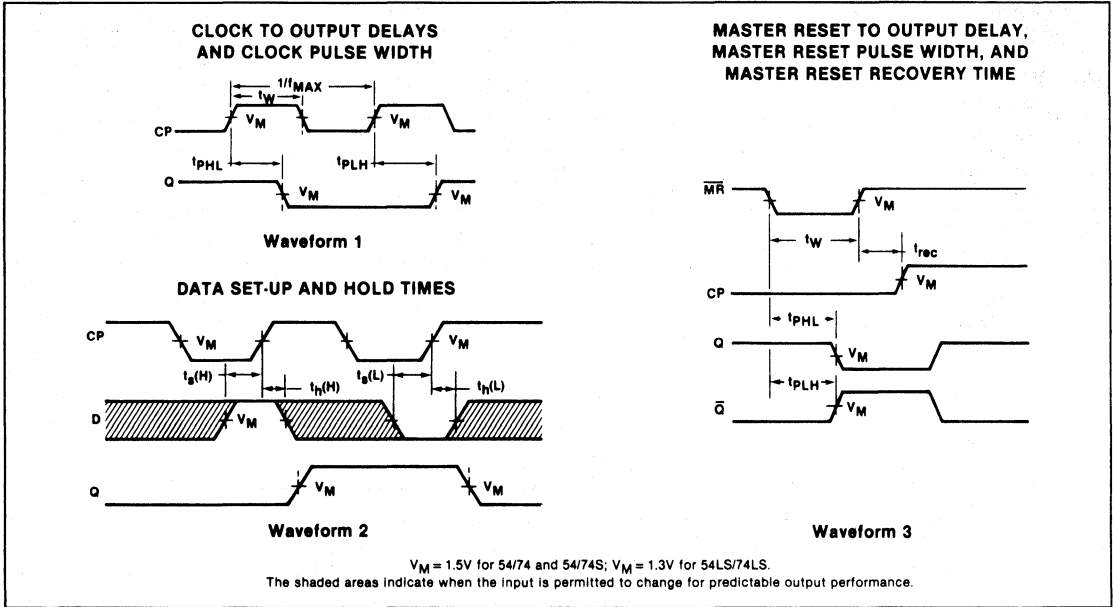
AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		Min	Max	Min	Max	Min	Max	
t _W Clock pulse width	Waveform 1	20		20		7		ns
t _W Master Reset pulse width	Waveform 3	20		20		10		ns
t _s (H) Setup time, HIGH data to CP	Waveform 2	20		20		5		ns
t _h (H) Hold time, HIGH data to CP	Waveform 2	5		5		3		ns
t _s (L) Setup time, LOW data to CP	Waveform 2	20		20		5		ns
t _h (L) Hold time, LOW data to CP	Waveform 2	5		5		3		ns
t _{rec} Recovery time, MR to CP	Waveform 3	25		25		5		ns

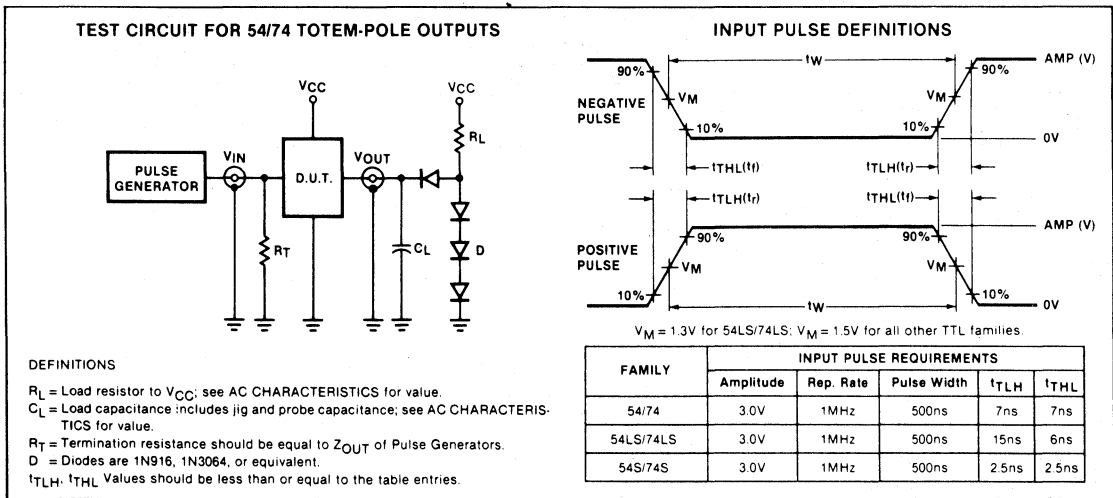
FLIP-FLOPS

54/74175, LS175, S175

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



PARITY GENERATOR/CHECKER

54/74180

9-Bit Odd/Even Parity Generator/Checker

- Word length easily expanded by cascading
- Generate even or odd parity
- Checks for parity errors
- See '280 for faster parity checker

TYPE	TYPICAL PROPAGATION DELAY, P _O = 0V	TYPICAL SUPPLY CURRENT
74180	36ns	34mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{CC} = 5V ± 5%; T _A = 0°C to +70°C	MILITARY RANGES V _{CC} = 5V ± 10%; T _A = -55°C to +125°C
Plastic DIP	N74180N	
Ceramic DIP		S54180F
Flatpack		S54180W

DESCRIPTION

The '180 is a 9-bit parity generator or checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even and Odd parity enable inputs and parity outputs are available for generating or checking parity on 8-bits.

True active-HIGH or true active-LOW parity can be generated at both the Even and Odd outputs. True active-HIGH parity is established with Even Parity enable input (P_E) set HIGH and the Odd Parity enable input (P_O) set LOW. True active-LOW parity is established when P_E is LOW and P_O is HIGH. When both enable inputs are at the same logic level, both outputs will be forced to the opposite logic level.

Parity checking of a 9-bit word (8 bits plus parity) is possible by using the two enable inputs plus an inverter as the ninth data input. To check for true active-HIGH parity,

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
I ₀ -I ₇	Data inputs	1ul
P _E , P _O	Parity inputs	2ul
Σ _E , Σ _O	Parity outputs	10ul

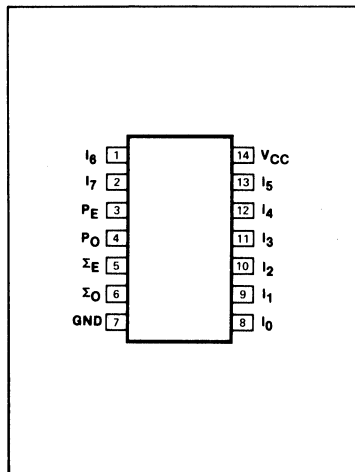
NOTE

A 54/74 unit load (ul) is understood to be 40μA I_{IH} and -1.6mA I_{IL}.

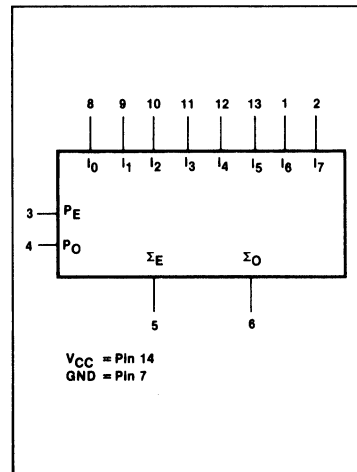
the ninth data input is tied to the P_O input and an inverter is connected between the P_O and P_E inputs. To check for true active-LOW parity, the ninth data input is tied to the P_E input and an inverter is connected between the P_E and P_O inputs.

Expansion to larger word sizes is accomplished by serially cascading the '180 in 8-bit increments. The Even and Odd parity outputs of the first stage are connected to the corresponding P_E and P_O inputs, respectively, of the succeeding stage.

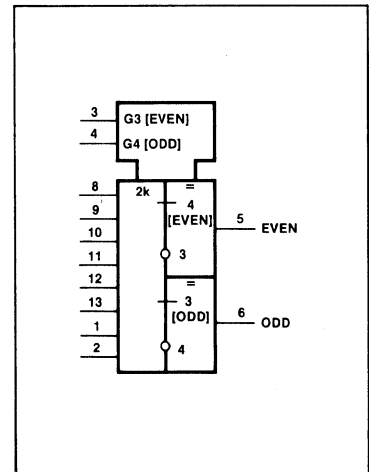
PIN CONFIGURATION



LOGIC SYMBOL



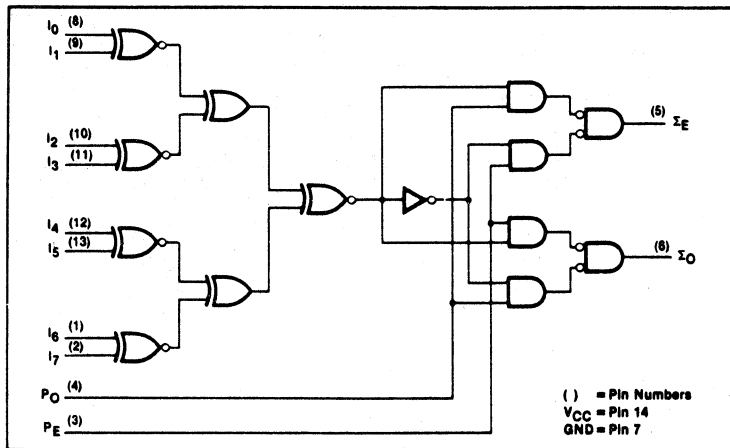
LOGIC SYMBOL (IEEE/IEC)



PARITY GENERATOR/CHECKER

54/74180

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS		OUTPUTS		
Number of HIGH Data Inputs (I ₀ -I ₇)	P _E	P _O	Σ _E	Σ _O
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5V to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT
		Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+0.8	V
	Com'l			+0.8	V
I _{IK} Input clamp current				-12	mA
I _{OH} HIGH-level output current				-800	μA
I _{OL} LOW-level output current	Mil			16	mA
	Com'l			16	mA
T _A Operating free-air temperature	Mil	-55		+125	°C
	Com'l	0		70	°C

PARITY GENERATOR/CHECKER

54/74180

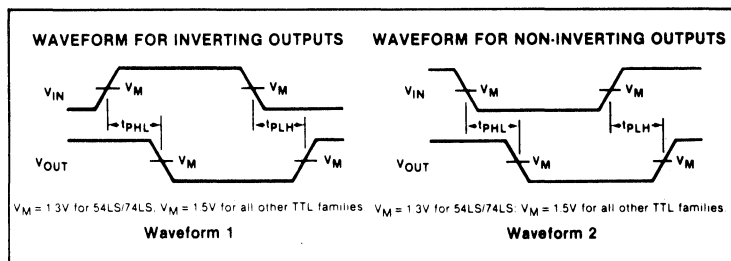
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74180			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.3	V	
		Com'l	2.4	3.3	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V	I ₀ -I ₇ inputs			40	μA
		P _E , P _O inputs			80	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	I ₀ -I ₇ inputs			-1.6	mA
		P _{0E} , P ₀ inputs			-3.2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-55	mA
		Com'l	-18		-55	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		34	49	mA
		Com'l		34	56	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with P_E and P_O inputs at 4.5V, all other inputs and outputs open.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

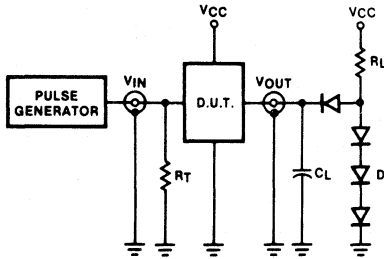
PARAMETER	TEST CONDITIONS	54/74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay Data to Even output	Waveforms 1 & 2, P _O = 0V		60 68	ns
t _{PLH} t _{PHL} Propagation delay Data to Odd output	Waveforms 1 & 2, P _O = 0V		48 38	ns
t _{PLH} t _{PHL} Propagation delay Data to Even output	Waveforms 1 & 2, P _E = 0V		48 38	ns
t _{PLH} t _{PHL} Propagation delay Data to Odd output	Waveforms 1 & 2, P _E = 0V		60 68	ns
t _{PLH} t _{PHL} Propagation delay P _E or P _O to output	Waveform 1		20 10	ns

PARITY GENERATOR/CHECKER

54/74180

TEST CIRCUITS AND WAVEFORMS

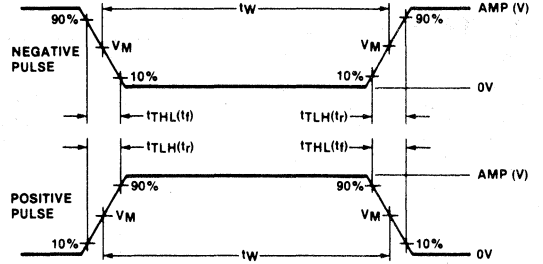
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

ARITHMETIC LOGIC UNITS

54/74181, LS181, S181

4-Bit Arithmetic Logic Unit

- Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations
- Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations
- Full lookahead carry for high-speed arithmetic operation on long words

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74181	22ns	91mA
74LS181	22ns	21mA
74S181	11ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74181N • N74LS181N N74S181N	
Ceramic DIP		S54181F • S54LS181F S54S181F
Flatpack		S54LS181W

DESCRIPTION

The '181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0 - S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look-

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
Mode	Input	1uI	1SuI	1LSuI
\bar{A} or \bar{B}	Inputs	3uI	3SuI	3LSuI
S	Inputs	4uI	4SuI	4LSuI
Carry	Input	5uI	5SuI	5LSuI
F_0 - F_3 , A = B, C_{n+4}	Outputs	10uI	10SuI	10LSuI
\bar{G}	Output	10uI	10SuI	40LSuI
\bar{P}	Output	10uI	10SuI	20LSuI

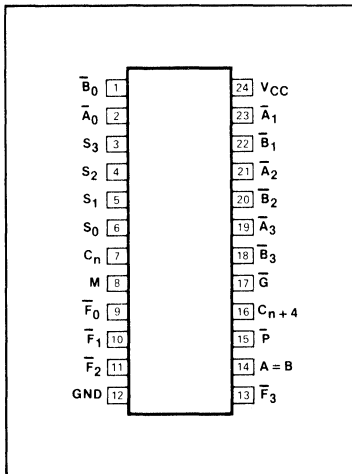
NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (SuI) is 50 μ A I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSuI) is 20 μ A I_{IH} and -0.4mA I_{IL} .

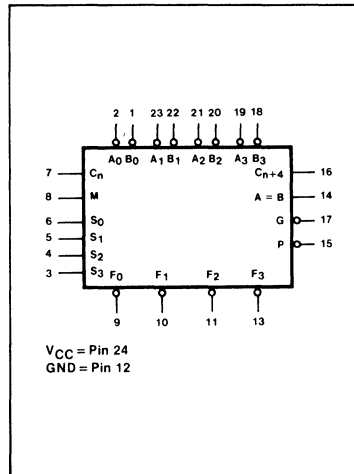
ahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages

using the signals \bar{P} (Carry Propagate) and \bar{G} (Carry Generate). \bar{P} and \bar{G} are not affected by carry in. When speed require-

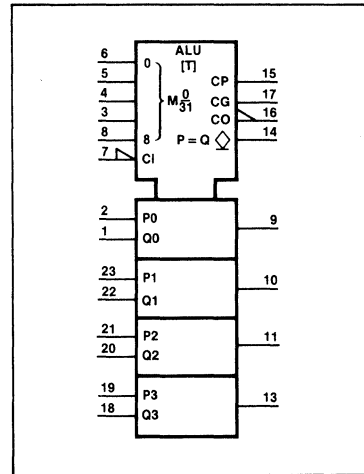
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ARITHMETIC LOGIC UNITS

54/74181, LS181, S181

ments are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the '182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The $A = B$ output from the device goes HIGH when all four \bar{F} outputs are HIGH and can be used to indicate logic equiva-

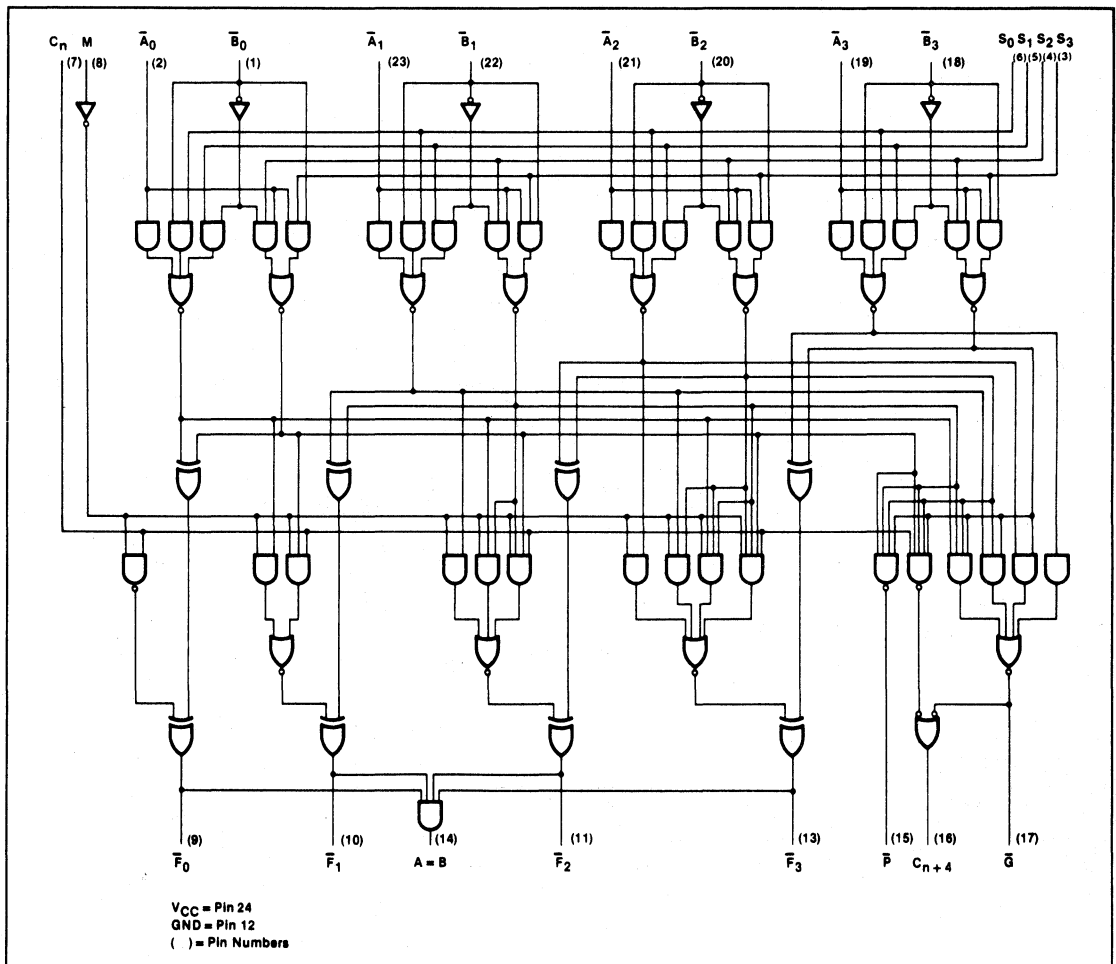
lence over 4 bits when the unit is in the subtract mode. The $A = B$ output is open collector and can be wired-AND with other $A = B$ outputs to give a comparison for more than 4 bits. The $A = B$ signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHLH generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

LOGIC DIAGRAM

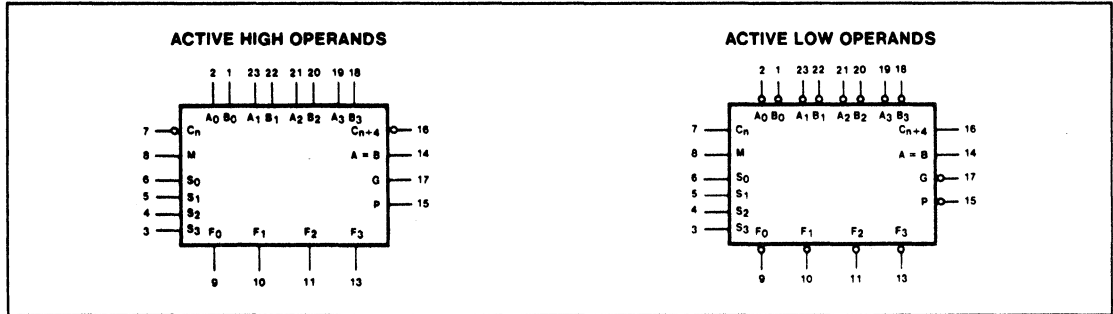


MODE SELECT—FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S ₃	S ₂	S ₁	S ₀	LOGIC (M = H)	ARITHMETIC** (M = L) (C _n = H)
L	L	L	L	\bar{A}	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	\overline{AB}	A + \bar{B}
L	L	H	H	Logical 0	minus 1
L	H	L	L	\overline{AB}	A plus \overline{AB}
L	H	L	H	\bar{B}	(A + B) plus \overline{AB}
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	\overline{AB}	AB minus 1
H	L	L	L	$\overline{A+B}$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + \bar{B}) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	$A + \bar{B}$	(A + B) plus A
H	H	H	L	A + B	(A + \bar{B}) plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S ₃	S ₂	S ₁	S ₀	LOGIC (M = H)	ARITHMETIC** (M = L) (C _n = L)
L	L	L	L	\bar{A}	A minus 1
L	L	L	H	\overline{AB}	AB minus 1
L	L	H	L	$\overline{A+B}$	\overline{AB} minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + \bar{B})
L	H	L	H	\bar{B}	AB plus (A + \bar{B})
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	A + \bar{B}	A + \bar{B}
H	L	L	L	\overline{AB}	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	\overline{AB} plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	\overline{AB}	AB plus A
H	H	H	L	AB	\overline{AB} plus A
H	H	H	H	A	A

L = LOW voltage
 H = HIGH voltage level
 *Each bit is shifted to the next more significant position.
 **Arithmetic operations expressed in 2s complement notation.



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

ARITHMETIC LOGIC UNITS

54/74181, LS181, S181

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.8			+ 0.7			+ 0.8	V
		Com'l			+ 0.8			+ 0.8			+ 0.8	V
I _{IK}	Input clamp current			- 12			- 18			- 18	mA	
I _{OH}	HIGH-level output current			- 800			- 400			- 1000	μA	
I _{OL}	LOW-level output current	Mil		16			4			20	mA	
		Com'l		16			8			20	mA	
T _A	Operating free-air temperature	Mil	- 55		+ 125	- 55		+ 125	- 55		+ 125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = + 0.7V MAX for 54S at T_A = + 125°C only.

SUM MODE TEST TABLE I

FUNCTION INPUTS: S₀ = S₃ = 4.5V, S₁ = S₂ = M = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t _{PLH} t _{PHL}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C _n	\bar{F}_i
t _{PLH} t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C _n	\bar{F}_i
t _{PLH} t _{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{P}
t _{PLH} t _{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{P}
t _{PLH} t _{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	\bar{G}
t _{PLH} t _{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	\bar{G}
t _{PLH} t _{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	C _{n+4}
t _{PLH} t _{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	C _{n+4}
t _{PLH} t _{PHL}	C _n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or C _{n+4}

ARITHMETIC LOGIC UNITS

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DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = 4.5V, S_0 = S_3 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B}, C_n	$A = B$
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B}, C_n	$A = B$
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	C_{n+4}
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B}, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All \bar{A} and \bar{B}	None	Any \bar{F} or C_{n+4}

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LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{F}_i	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B}, C_n	\bar{F}_i	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

ARITHMETIC LOGIC UNITS

54/74181, LS181, S181

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹			54/74181			54/74LS181			54/74S181			UNIT		
				Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Any output except A = B	Mil	2.4	3.4		2.5	3.4		2.5	3.4		V		
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX All outputs	Mil		0.2	0.4		0.25	0.4			0.5 ⁵	V		
			Com'l		0.2	0.4		0.35	0.5			0.5	V		
		I _{OL} = 4mA G output	74LS					0.25	0.4					V	
			Mil					0.47	0.7					V	
			Com'l					0.47	0.7					V	
			Mil					0.35	0.6					V	
Com'l					0.35	0.5					V				
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.5			-1.5			-1.2	V		
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V	Mode input					1.0			0.1			1.0	mA	
		A or B inputs					1.0			0.3			1.0	mA	
		S inputs					1.0			0.4			1.0	mA	
		Carry input					1.0			0.5			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	Mode input					40						μA	
			A or B inputs					120							μA
			S inputs					160							μA
			Carry input					200							μA
		V _I = 2.7V	Mode input								20			50	μA
			A or B inputs								60			150	μA
			S inputs								80			200	μA
			Carry input								100			250	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	Mode input					-1.6						mA	
			A or B inputs					-4.8			-1.2				mA
			S inputs					-6.4			-1.6				mA
			Carry input					-8			-2				mA
		V _I = 0.5V	Mode input											-2	mA
			A or B inputs											-6	mA
			S inputs											-8	mA
			Carry input											-10	mA
I _{OH} HIGH-level output current	V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 5.5V A = B only					250			100			250	μA		
I _{OS} Short-circuit output current ³	V _{CC} = MAX Any output except A = B	Mil	-20		-55	-15		-100	-40			-100	mA		
		Com'l	-18		-57	-15		-100	-40			-100	mA		
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Note 4a	Mil	88	127		20	32		120	220		mA		
			Com'l	88	140		20	34		120	220		mA		
		Note 4b	Mil	94	135		21	35		120	220		mA		
			Com'l	94	150		21	37		120	220		mA		

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with the following conditions: a. S₀ through S₃, M, and A inputs are at 4.5V, other inputs grounded, all outputs open. b. S₀ through S₃ and M inputs are at 4.5V, other inputs grounded, all outputs open.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

ARITHMETIC LOGIC UNITS

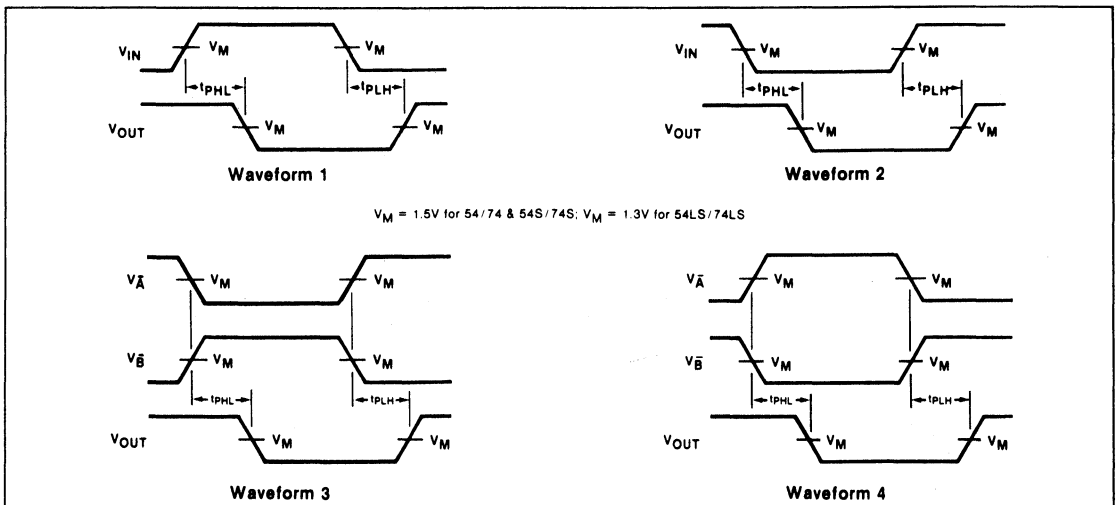
54/74181, LS181, S181

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		$C_L = 15\text{pF}$ $R_L = 400\Omega$		$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} C_n to C_{n+4}	$M = 0\text{V}$, Sum or Diff Mode see Waveform 2 and Tables I & II		18 19		27 20		10.5 10.5	ns
t_{PLH} Propagation delay t_{PHL} C_n to \bar{F} outputs	$M = 0\text{V}$, Sum or Diff Mode see Waveform 2 and Tables I & II		19 18		26 20		12 12	ns
t_{PLH} Propagation delay t_{PHL} \bar{A} or \bar{B} inputs to \bar{G} output	$M = S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		19 19		29 23		12 12	ns
t_{PLH} Propagation delay t_{PHL} \bar{A} or \bar{B} inputs to \bar{G} output	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		25 25		32 32		15 15	ns
t_{PLH} Propagation delay t_{PHL} \bar{A} or \bar{B} inputs to \bar{F} output	$M = S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		19 25		30 30		12 12	ns
t_{PLH} Propagation delay t_{PHL} \bar{A} or \bar{B} inputs to \bar{F} output	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		25 25		30 33		15 15	ns
t_{PLH} Propagation delay t_{PHL} \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	$M = S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		42 32		32 20		16.5 16.5	ns
t_{PLH} Propagation delay t_{PHL} \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		48 34		32 32		20 22	ns
t_{PLH} Propagation delay t_{PHL} \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	$M = 4.5\text{V}$, Logic Mode see Waveform 2 and Table III		48 34		33 38		20 22	ns
t_{PLH} Propagation delay t_{PHL} \bar{A} or \bar{B} inputs to C_{n+4} output	$M = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$, $S_1 = S_2 = 0\text{V}$ Sum Mode, see Waveform 1 and Table I		43 41		38 38		18.5 18.5	ns
t_{PLH} Propagation delay t_{PHL} \bar{A} or \bar{B} inputs to C_{n+4} output	$M = 0\text{V}$, $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 4 and Table II		50 50		41 41		23 23	ns
t_{PLH} Propagation delay t_{PHL} \bar{A} or \bar{B} inputs to $A = B$ output	$M = S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		50 48		50 62		23 30	ns

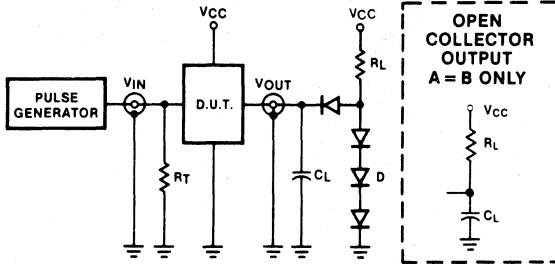
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AC WAVEFORMS

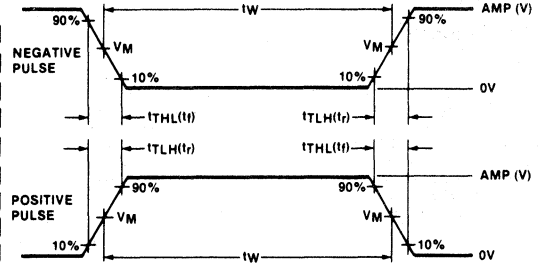


TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

CARRY GENERATOR

54/74S182

Lookahead Carry Generator

- Provides carry lookahead across a group of four ALU's
- Multi-level lookahead for high-speed arithmetic operation over long word lengths

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S182	5.8ns	69mA

DESCRIPTION

The '182 carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\bar{P}_0, \bar{P}_1, \bar{P}_2, \bar{P}_3$) and Carry Generate ($\bar{G}_0, \bar{G}_1, \bar{G}_2, \bar{G}_3$) signals and an active HIGH Carry input (C_n) and provides anticipated active HIGH carries ($C_{n+x}, C_{n+y}, C_{n+z}$) across four groups of binary adders. The '182 also has active LOW Carry Propagate (\bar{P}) and Carry Generate (\bar{G}) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 = P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0$$

$$\bar{G} = \bar{G}_3 + \bar{P}_3 \bar{G}_2 + \bar{P}_3 \bar{P}_2 \bar{G}_1 + \bar{P}_3 \bar{P}_2 \bar{P}_1 \bar{G}_0$$

$$\bar{P} = \bar{P}_3 \bar{P}_2 \bar{P}_1 \bar{P}_0$$

The '182 can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74S182N	
Plastic SO	N74S182D	
Ceramic DIP		S54S182F
Flatpack		S54S182W

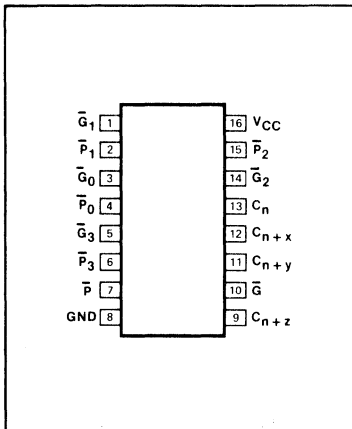
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S
C_n	Input	1Sul
\bar{P}_3	Input	2Sul
\bar{P}_2	Input	3Sul
$\bar{P}_0, \bar{P}_1, \bar{G}_3$	Inputs	4Sul
\bar{G}_0, \bar{G}_2	Inputs	7Sul
\bar{G}_1	Input	8Sul
All	Outputs	10Sul

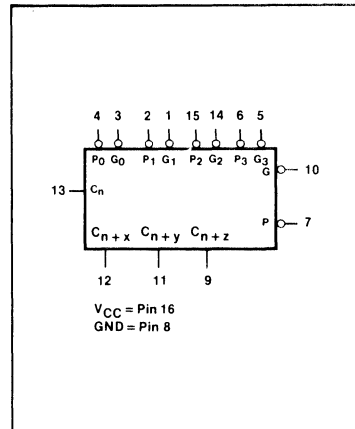
NOTE

A 54/74S unit load (Sul) is 50µA I_{IH} and -2.0mA I_{IL} .

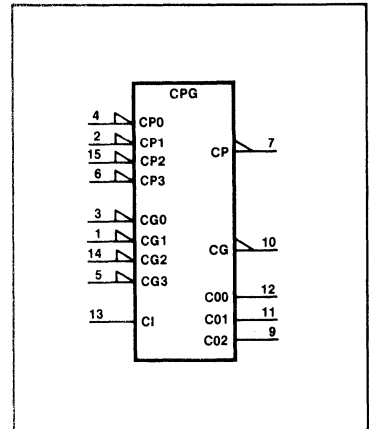
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

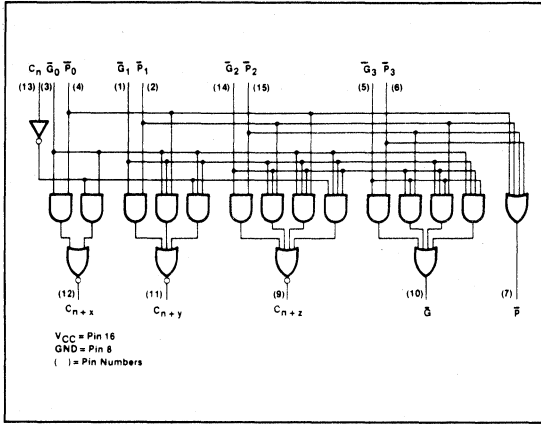


4

CARRY GENERATOR

54/74S182

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	\bar{G}_0	\bar{P}_0	\bar{G}_1	\bar{P}_1	\bar{G}_2	\bar{P}_2	\bar{G}_3	\bar{P}_3	C_{n+x}	C_{n+y}	C_{n+z}	\bar{G}	\bar{P}
X	H	H							L				
L	H	X							L				
X	L	X							L				
H	X	L							H				
X	X	X	H	H						L			
X	H	X	H	X						L			
L	X	X	H	X						L			
X	X	X	X	L						L			
X	X	X	L	X						L			
X	L	X	X	X						L			
H	X	L	X	L						H			
X	X		X	X	X	H	H					H	
X	X		H	H	H	X	X	X				H	
X	H		H	X	H	X	H	X				H	
X	X		X	X	X	L	X	L				L	
X	X		X	X	X	X	X	L				L	
X	L		L	X	X	X	X	L				L	
L	X		X	L	X	X	L	L				L	
	H		X		X		X						H
	X		H		X		X						H
	X		X		H		X						H
	L		L		X		L						L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54S	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

CARRY GENERATOR

54/74S182

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74S			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current				- 1000	μA
I _{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH}, t_{TLL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{TLL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

CARRY GENERATOR

54/74S182

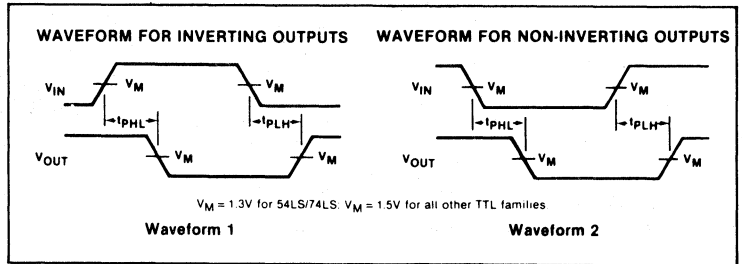
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74S182			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V	
		Com'l	2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.5 ⁵	V	
		Com'l		0.5	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	C _n input		50	μA	
		\overline{P}_3 input		100	μA	
		\overline{P}_2 input		150	μA	
		$\overline{P}_0, \overline{P}_1, \overline{G}_3$ inputs		200	μA	
		$\overline{G}_0, \overline{G}_2$ inputs		350	μA	
		\overline{G}_1 input		400	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V	C _n input		-2	mA	
		\overline{P}_3 input		-4	mA	
		\overline{P}_2 input		-6	mA	
		$\overline{P}_0, \overline{P}_1, \overline{G}_3$ inputs		-8	mA	
		$\overline{G}_0, \overline{G}_2$ inputs		-14	mA	
		\overline{G}_1 input		-16	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-40	-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		69	99	mA
		Com'l		69	109	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with $\overline{G}_0, \overline{G}_1$ and \overline{G}_2 inputs at 4.5V, all other inputs grounded and all outputs open.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74S		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
t _{PLH} Propagation delay t _{PHL} \overline{G}_n or \overline{P}_n to any C output	Waveform 1		7.0 7.0	ns
t _{PLH} Propagation delay t _{PHL} \overline{G}_n or \overline{P}_n to \overline{G} output	Waveform 2		7.5 10.5	ns
t _{PLH} Propagation delay t _{PHL} \overline{P}_n to \overline{P} output	Waveform 2		6.5 10	ns
t _{PLH} Propagation delay t _{PHL} C _n to any C output	Waveform 2		10 10.5	ns

COUNTERS

54/74190, 191, LS191

'190 Presettable BCD/Decade Up/Down Counter
'191 Presettable 4-Bit Binary Up/Down Counter

- Synchronous, reversible counting
- BCD/decade — '190
4-bit binary — '191
- Synchronous, reversible counting
- Asynchronous parallel load capability
- Count enable control for synchronous expansion
- Single Up/Down control input

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74190	25MHz	65mA
74191	25MHz	65mA
74LS191	25MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74190N N74191N • N74LS191N	
Plastic SO	N74LS191D	
Ceramic DIP		S54190F S54191F • S54LS191F
		S54190W S54191W • S54LS191W
Flatpack		

DESCRIPTION

The '190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The '191 is similar, but is a 4-bit binary counter.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the counter and appears on the outputs when the Parallel Load (\overline{PL}) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable (\overline{CE}) input. When \overline{CE} is LOW, internal state changes are initiated

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
\overline{CE}	Input	3uI	3LSuI
Other	Inputs	1uI	1LSuI
All	Outputs	10uI	10LSuI

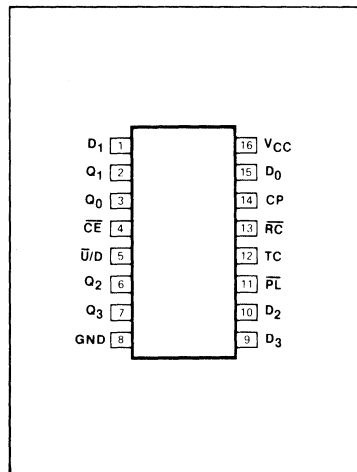
NOTE

Where a 54/74 unit load is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

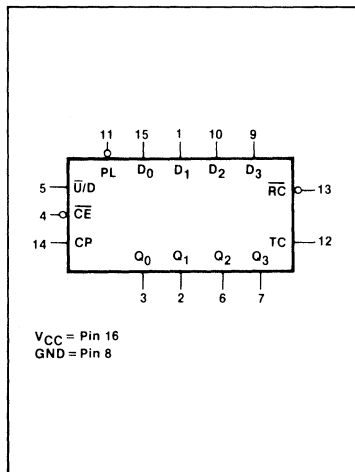
synchronously by the LOW-to-HIGH transition of the Clock input. The Up/Down ($\overline{U/D}$) input signal determines the direction of counting as indicated in the Mode Select Table. The \overline{CE} input may go LOW

when the clock is in either state, however, the LOW-to-HIGH \overline{CE} transition must occur only when the clock is HIGH. Also, the $\overline{U/D}$ input should be changed only when either \overline{CE} or CP is HIGH.

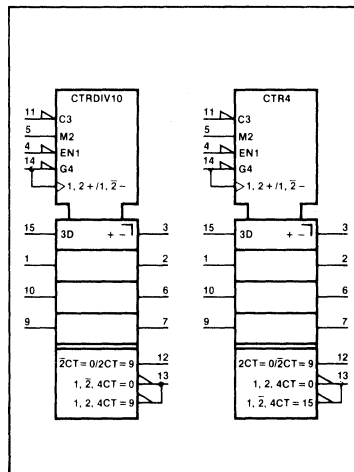
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock (\overline{RC}). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U/D}$ is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the \overline{RC} output. When TC is HIGH and \overline{CE} is LOW, the RC follows the Clock Pulse (CP) delayed by two gate delays. The \overline{RC} output essentially duplicates the LOW clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A,

each \overline{RC} output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH signal on \overline{CE} inhibits the \overline{RC} output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure B shows a method of causing state changes to occur simultaneously in all stages. The \overline{RC} outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The LOW state duration of the clock in this

configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the \overline{RC} output of any package goes HIGH shortly after its CP input goes HIGH, there is no such restriction on the HIGH state duration of the clock.

In Figure C, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the \overline{CE} input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own \overline{CE} , therefore, the simple inhibit scheme of Figure A and B does not apply.

N-STAGE COUNTER USING RIPPLE CLOCK

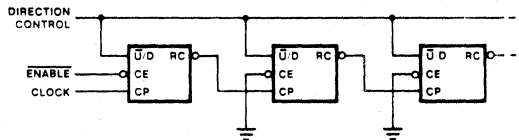


Figure A

SYNCHRONOUS N-STAGE COUNTER USING RIPPLE CARRY/BORROW

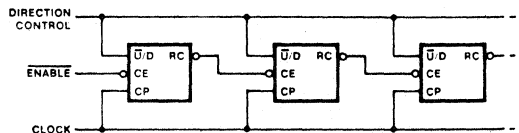


Figure B

SYNCHRONOUS N-STAGE COUNTER WITH PARALLEL GATED CARRY/BORROW

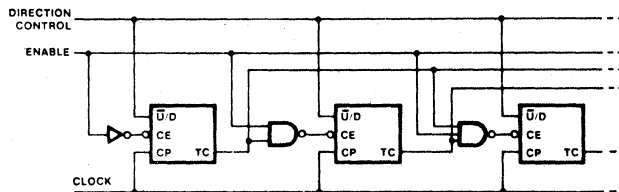
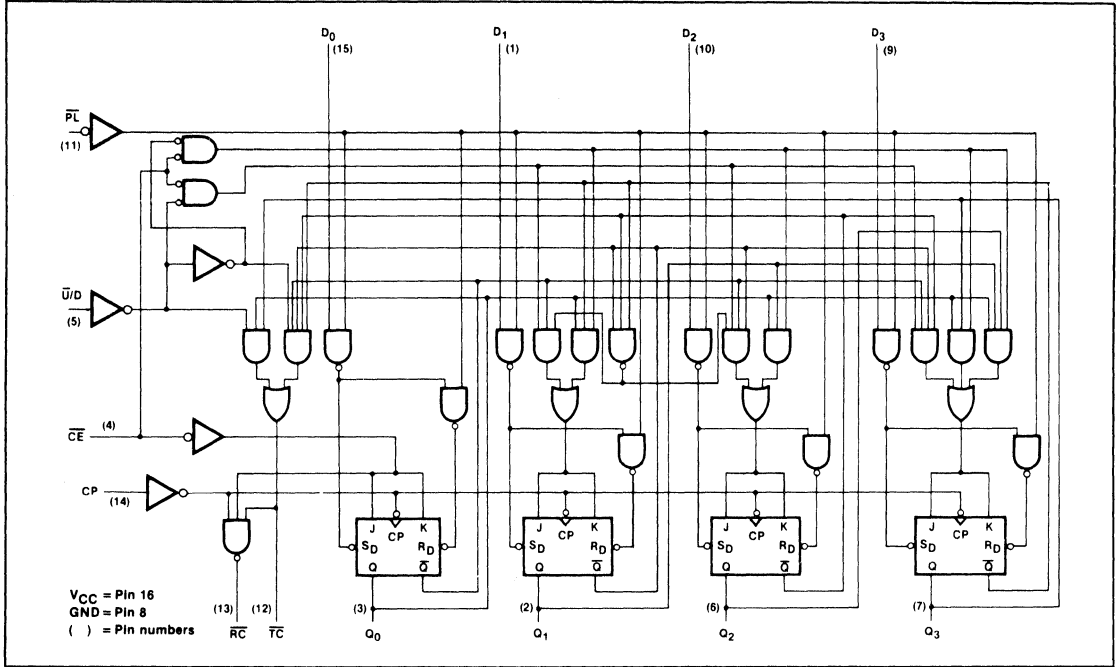


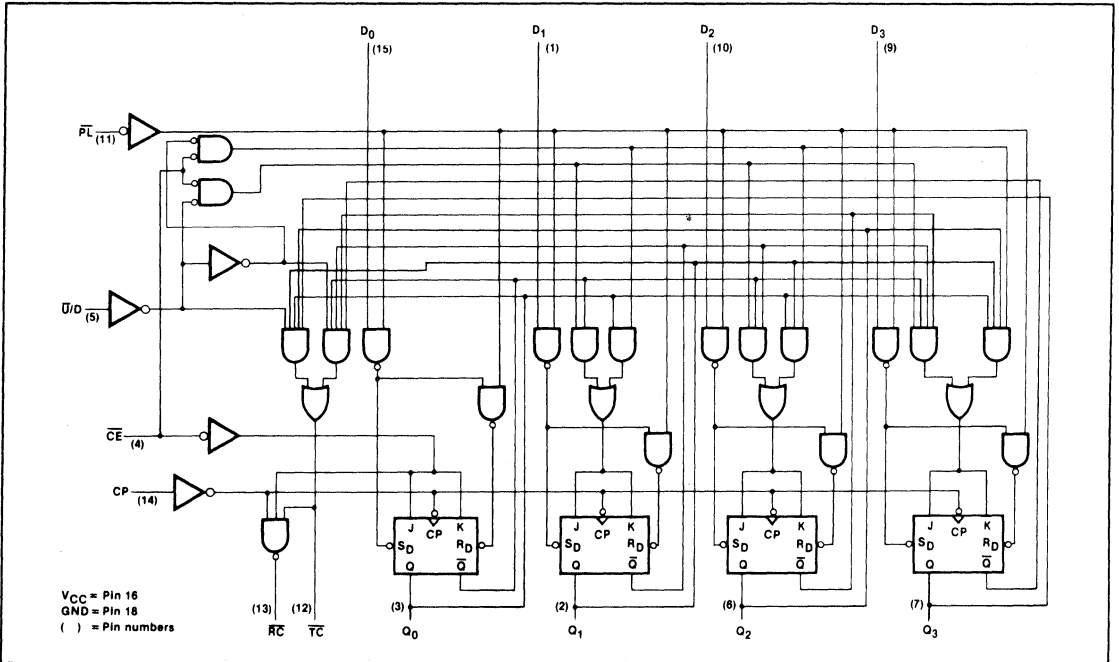
Figure C

LOGIC DIAGRAM '190



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LOGIC DIAGRAM '191



COUNTERS

54/74190, 191, LS191

MODE SELECT—FUNCTION TABLE, '190, '191

OPERATING MODE	INPUTS					OUTPUTS
	\overline{PL}	$\overline{U/D}$	\overline{CE}	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	1	1	X	count up
Count down	H	H	1	1	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND \overline{RC} FUNCTION TABLE, '190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U/D}$	\overline{CE}	CP	Q_0	Q_1	Q_2	Q_3	TC	\overline{RC}
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	$\overline{\text{L}}$	H	X	X	H	$\overline{\text{L}}$	$\overline{\text{L}}$
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	$\overline{\text{L}}$	L	L	L	L	$\overline{\text{L}}$	$\overline{\text{L}}$

TC AND \overline{RC} FUNCTION TABLE, '191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U/D}$	\overline{CE}	CP	Q_0	Q_1	Q_2	Q_3	TC	\overline{RC}
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	$\overline{\text{L}}$	H	H	H	H	$\overline{\text{L}}$	$\overline{\text{L}}$
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	$\overline{\text{L}}$	L	L	L	L	$\overline{\text{L}}$	$\overline{\text{L}}$

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 1 = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 1 = LOW-to-HIGH clock transition.
 $\overline{\text{L}}$ = LOW pulse.
 $\overline{\text{L}}$ = TC goes LOW on a LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

COUNTERS

54/74190, 191, LS191

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V	
V _{IL}	LOW-level input voltage	Mil		+ 0.8			+ 0.7	V	
		Com'l		+ 0.8			+ 0.8	V	
I _{IK}	Input clamp current			- 12			- 18	mA	
I _{OH}	HIGH-level output current			- 800			- 400	μA	
I _{OL}	LOW-level output current	Mil		16			4	mA	
		Com'l		16			8	mA	
T _A	Operating free-air temperature	Mil	- 55	+ 125	- 55		+ 125	°C	
		Com'l	0	70	0		70	°C	

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

4

PARAMETER	TEST CONDITIONS ¹	54/74190, 191			54/74LS191			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MIN, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4	V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	Mil		0.2	0.4		0.25	0.4	V
		Com'l		0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS				0.25	0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.5	V	
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0			mA	
		V _I = 7.0V	\overline{CE} input				0.3	mA	
V _I = 2.4V	Other inputs					0.1	mA		
	I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V	\overline{CE} input		120			μA
Other inputs					40			μA	
V _I = 2.7V			\overline{CE} input				60	μA	
			Other inputs				20	μA	
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V	\overline{CE} input		-4.8		-1.2	mA	
			Other inputs		-1.6		-0.4	mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	Mil	-20		-65	-20	-100	mA	
		Com'l	-18		-65	-20	-100	mA	
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX	Mil		65	99		20	35	mA
		Com'l		65	105		20	35	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with all inputs grounded and all outputs open.

COUNTERS

54/74190, 191, LS191

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum input count frequency	Waveform 1	20		20		MHz
t_{PLH} Propagation delay t_{PHL} Clock to Q output	Waveform 1		24 36		24 36	ns
t_{PLH} Propagation delay t_{PHL} Clock to \overline{RC} output	Waveform 2		20 24		20 24	ns
t_{PLH} Propagation delay t_{PHL} Clock to TC output	Waveform 1		42 52		42 52	ns
t_{PLH} Propagation delay t_{PHL} $\overline{U/D}$ to \overline{RC} output	Waveform 7		45 45		45 45	ns
t_{PLH} Propagation delay t_{PHL} $\overline{U/D}$ to TC output	Waveform 7		33 33		33 33	ns
t_{PLH} Propagation delay t_{PHL} Data to Q outputs	Waveform 3		22 50		32 40	ns
t_{PLH} Propagation delay t_{PHL} \overline{PL} to any output	Waveform 4		33 50		33 50	ns
t_{PLH} Propagation delay t_{PHL} \overline{CE} to \overline{RC} output	Waveform 2		33 33		33 33	ns

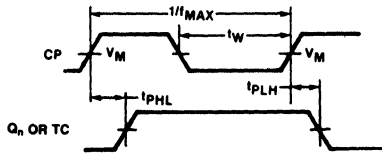
NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

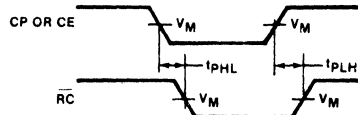
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		Min	Max	Min	Max	
t_W CP pulse width	Waveform 1	25		25		ns
t_W \overline{PL} pulse width	Waveform 5	35		35		ns
t_s Setup time, Data to \overline{PL}	Waveform 6	20		20		ns
t_h Hold time, Data to \overline{PL}	Waveform 6	0		5		ns
t_{rec} Recovery time, \overline{PL} to CP	Waveform 5	40		40		ns
$t_s(L)$ Setup time, LOW \overline{CE} to Clock	Waveform 8	40		40		ns
$t_h(L)$ Hold time, LOW \overline{CE} to Clock	Waveform 8	0		0		ns

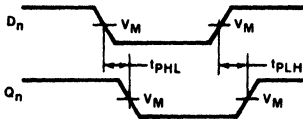
AC WAVEFORMS



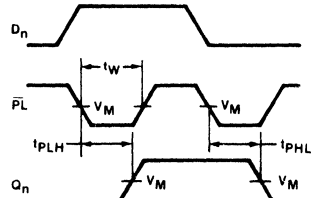
Waveform 1



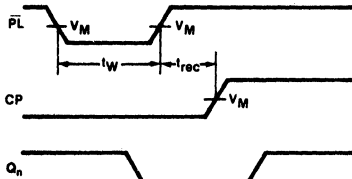
Waveform 2



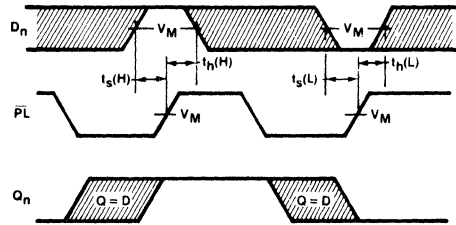
Waveform 3



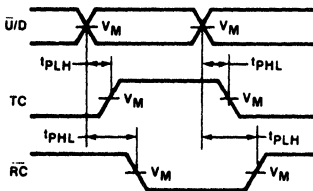
Waveform 4



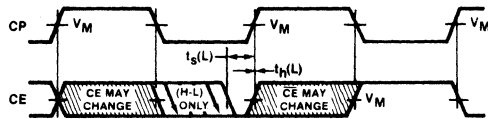
Waveform 5



Waveform 6



Waveform 7



Waveform 8

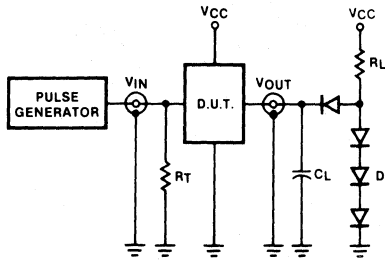
$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

COUNTERS

54/74190, 191, LS191

TEST CIRCUITS AND WAVEFORMS

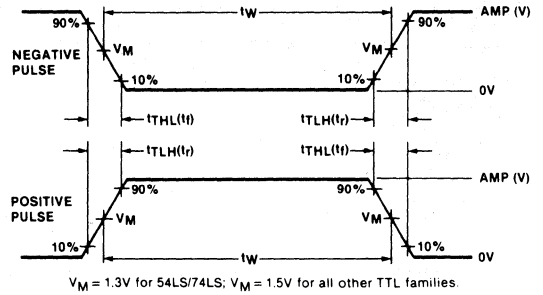
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS

54/74192, 54/74193, LS192, LS193

'192 Presettable BCD Decade Up/Down Counter
'193 Presettable 4-Bit Binary Up/Down Counter

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset (clear)
- Expandable without external logic

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74192	32MHz	65mA
74LS192	32MHz	19mA
74193	32MHz	65mA
74LS193	32MHz	19mA

DESCRIPTION

The '192 and '193 are 4-bit synchronous up/down counters — the '192 counts in BCD mode and the '193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either Clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up . . . if CP_D is pulsed while the CP_U is held HIGH, the device will count down. Only one Clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74192N • N74LS192N N74193N • N74LS193N	
Plastic SO	N74LS193D	
Ceramic DIP		S54LS192F S54193F • S54LS193F
Flatpack		S54LS192W S54193W • S54LS193W
LLCC		S54LS193G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1uI	1LSuI
All	Outputs	10uI	10LSuI

NOTE

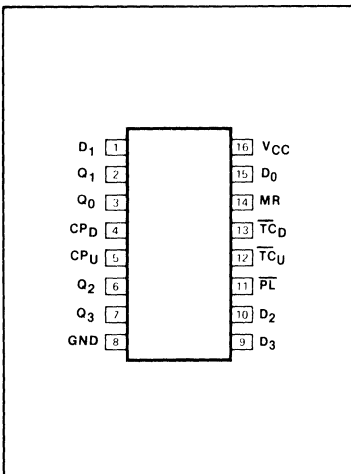
Where a 54/74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , and a 54/74LS unit load (LSuI) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

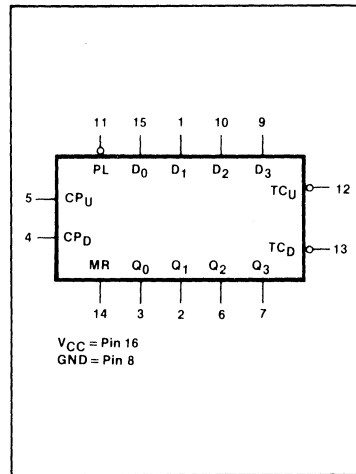
One clock should be held HIGH while counting with the other, because the cir-

cuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

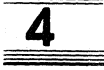
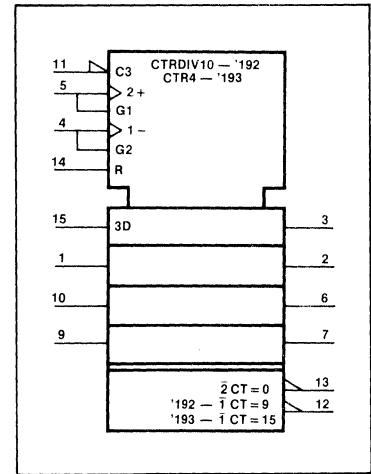
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



COUNTERS

54/74192, 54/74193, LS192, LS193

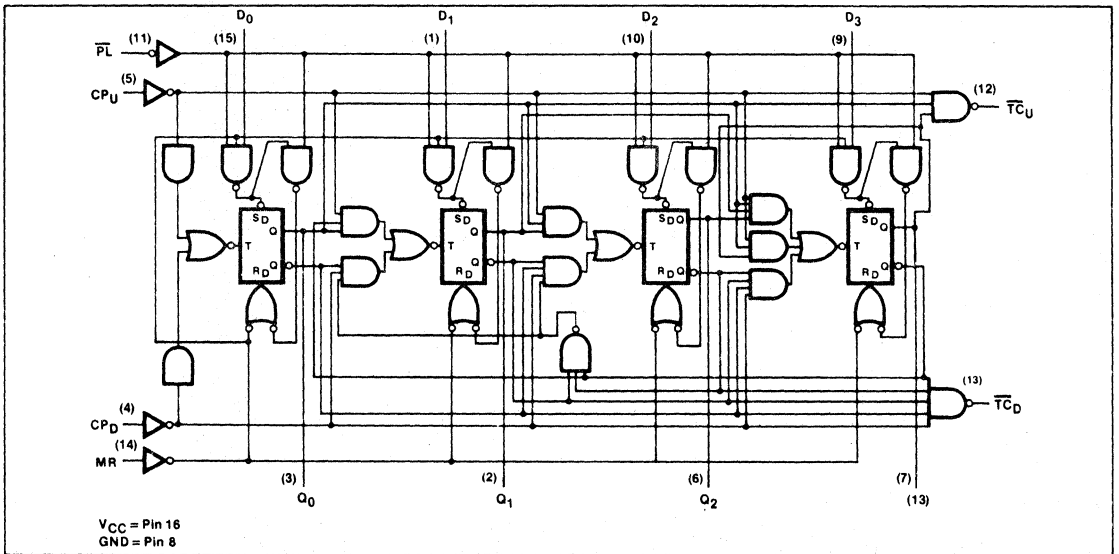
The Terminal Count Up (\overline{TC}_U) and Terminal Count down (\overline{TC}_D) outputs are normally HIGH. When the circuit has reached the maximum count state of 9 (for the '192 and 15 for the '193), the next HIGH-to-LOW transition of CP_U will cause \overline{TC}_U to go LOW. \overline{TC}_U will stay LOW until CP_U goes HIGH again, duplicating the count up clock, although delayed by two gate delays. Likewise, the \overline{TC}_D output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The \overline{TC} outputs can be

used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

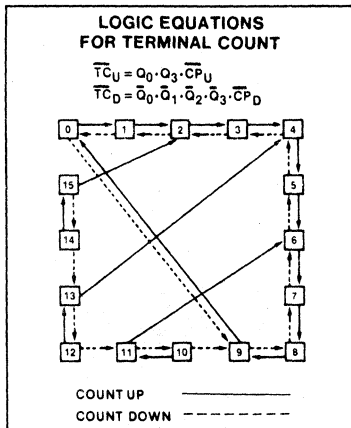
The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D_0 - D_3) is loaded into the

counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load (PL) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs LOW. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM, '192



STATE DIAGRAM, '192



LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \cdot Q_3 \cdot \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$$

MODE SELECT—FUNCTION TABLE, '192

OPERATING MODE	INPUTS								OUTPUTS					
	MR	PL	CP _U	CP _D	D ₀	D ₁	D ₂	D ₃	Q ₀	Q ₁	Q ₂	Q ₃	\overline{TC}_U	\overline{TC}_D
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	H	X	H	X	X	H	Q _n = D _n			L	H	
Count up	L	H	↑	H	X	X	X	X	Count up				H ^(a)	H
Count down	L	H	H	↓	X	X	X	X	Count down				H	H ^(b)

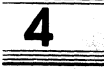
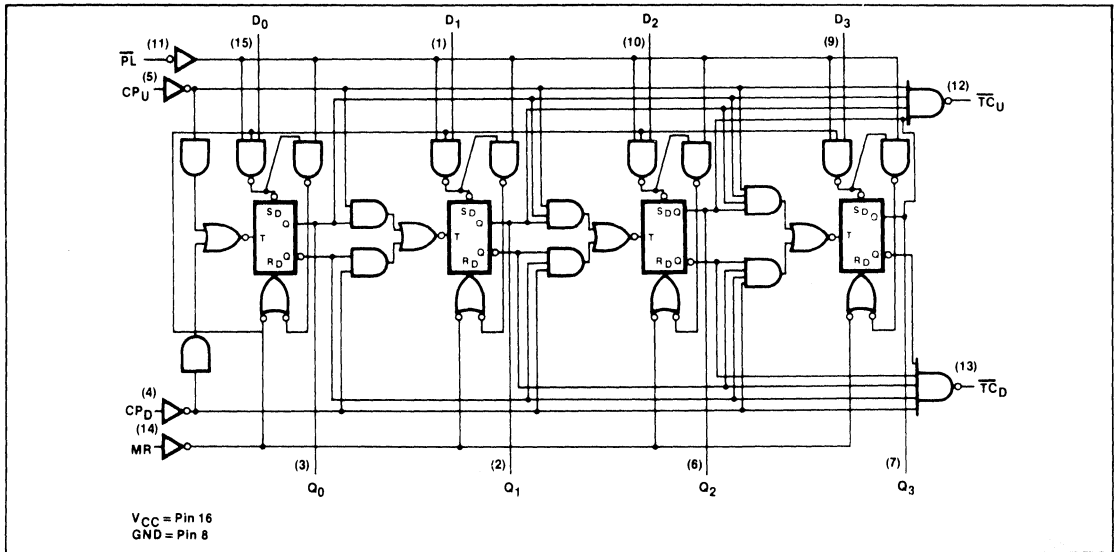
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH clock transition

NOTES
 a. \overline{TC}_U = CP_U at terminal count up (HLLH).
 b. \overline{TC}_D = CP_D at terminal count down (LLLL).

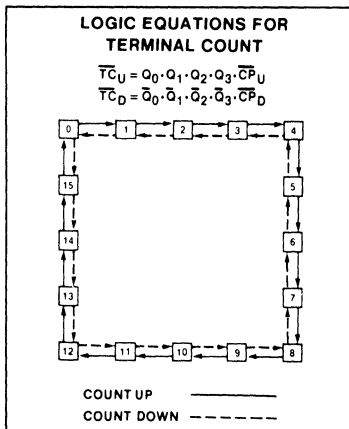
COUNTERS

54/74192, 54/74193, LS192, LS193

LOGIC DIAGRAM, '193



STATE DIAGRAM, '193



MODE SELECT—FUNCTION TABLE, '193

OPERATING MODE	INPUTS								OUTPUTS					
	MR	P \overline{L}	CP $_U$	CP $_D$	D $_0$	D $_1$	D $_2$	D $_3$	Q $_0$	Q $_1$	Q $_2$	Q $_3$	\overline{TC}_U	\overline{TC}_D
Reset clear	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
Count up	L	H	↑	H	X	X	X	X	Count up				H ^(c)	H
Count down	L	H	H	↓	X	X	X	X	Count down				H	H ^(d)

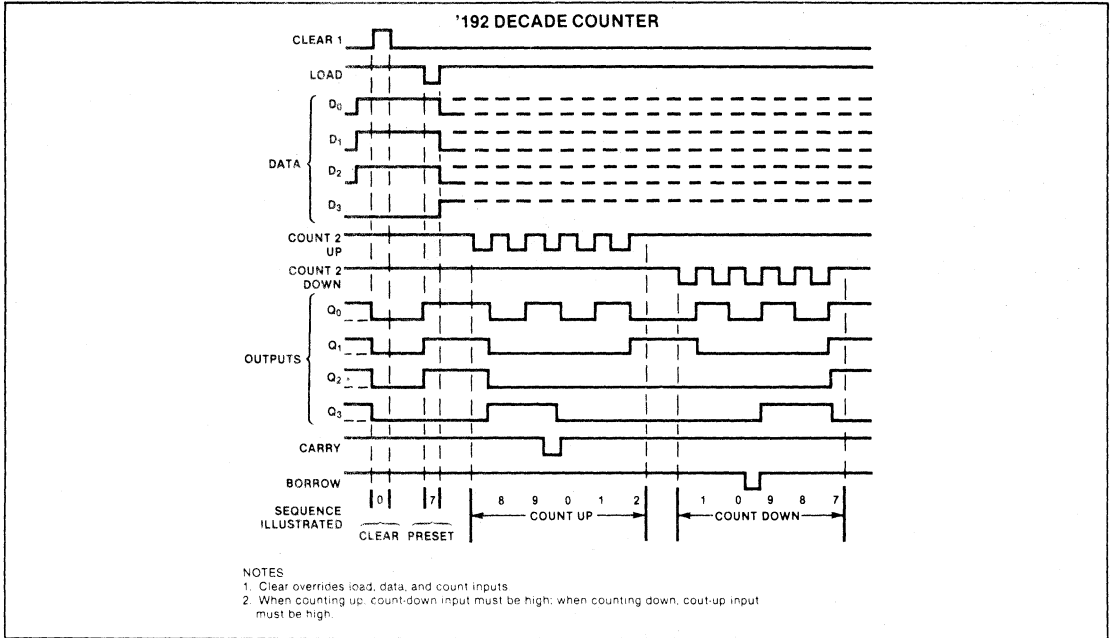
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH clock transition

NOTES
 c. $\overline{TC}_U = CP_U$ at terminal count up (HHHH).
 d. $\overline{TC}_D = CP_D$ at terminal count down (LLLL).

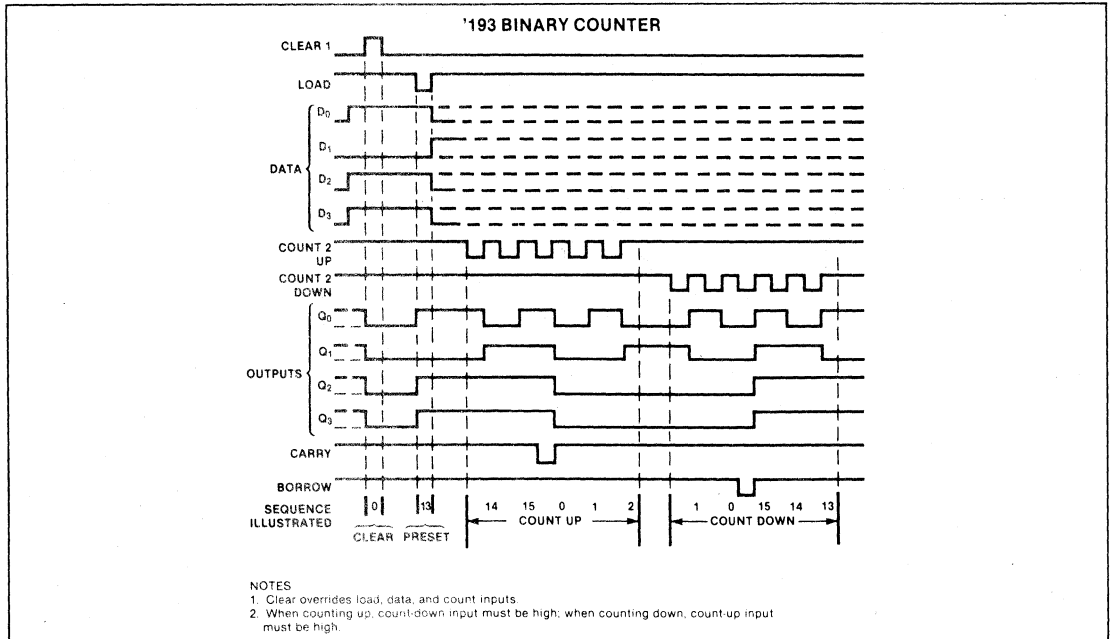
COUNTERS

54/74192, 54/74193, LS192, LS193

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



COUNTERS

54/74192, 54/74193, LS192, LS193

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V	
V _{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18	mA	
I _{OH}	HIGH-level output current			-800			-400	mA	
I _{OL}	LOW-level output current	Mil		16			4	mA	
		Com'l		16			8	mA	
T _A	Operating free-air temperature	Mil	-55	+125	-55		+125	°C	
		Com'l	0	70	0		70	°C	

4

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74192, '193			54/74LS192, '193			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.4	V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.2	0.4		0.25	0.4	V
			Com'l	0.2	0.4		0.35	0.5	V
		I _{OL} = 4mA	74LS				0.25	0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX		V _I = 5.5V		1.0		mA	
				V _I = 7.0V				0.1	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX		V _I = 2.4V		40		μA	
				V _I = 2.7V				20	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6		-0.4	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		Mil	-20	-65	-20	-100	mA
				Com'l	-18	-65	-20	-100	mA
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX		Mil	65	89	19	34	mA
				Com'l	65	102	19	34	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with Parallel Load and Master Reset inputs grounded, all other outputs at 4.5V and all outputs open.

COUNTERS

54/74192, 54/74193, LS192, LS193

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	Min	Max	
f_{MAX} Maximum input count frequency	Waveform 1	25		25		MHz
t_{PLH} Propagation delay t_{PHL} CP_U input to \overline{TC}_U output	Waveform 2		26 24		26 24	ns
t_{PLH} Propagation delay t_{PHL} CP_D input to \overline{TC}_D output	Waveform 2		24 24		24 24	ns
t_{PLH} Propagation delay t_{PHL} CP_U or CP_D to Q_n outputs	Waveform 1		38 47		38 47	ns
t_{PLH} Propagation delay t_{PHL} PL input to Q_n output	Waveform 3		40 40		40 40	ns
t_{PHL} Propagation delay, MR to output	Waveform 4		35		35	ns

NOTE

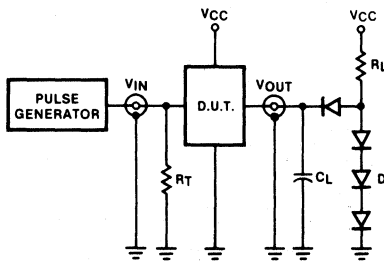
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

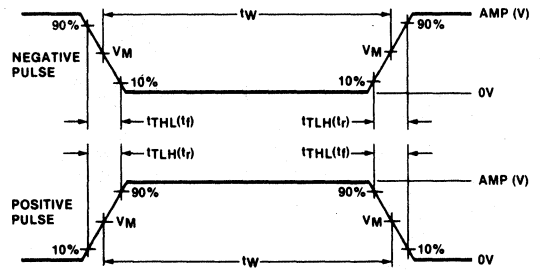
PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		Min	Max	Min	Max	
t_W CP_U pulse width	Waveform 1	20		20		ns
t_W CP_D pulse width	Waveform 1	20		20		ns
t_W PL pulse width	Waveform 3	20		20		ns
t_W MR pulse width	Waveform 4	20		20		ns
t_s Setup time, Data to \overline{PL}	Waveform 5	20		20		ns
t_h Hold time, Data to \overline{PL}	Waveform 5	0		5		ns
t_{rec} Recovery time, \overline{PL} to CP	Waveform 3	40		40		ns
t_{rec} Recovery time, MR to CP	Waveform 4	40		40		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

DEFINITIONS

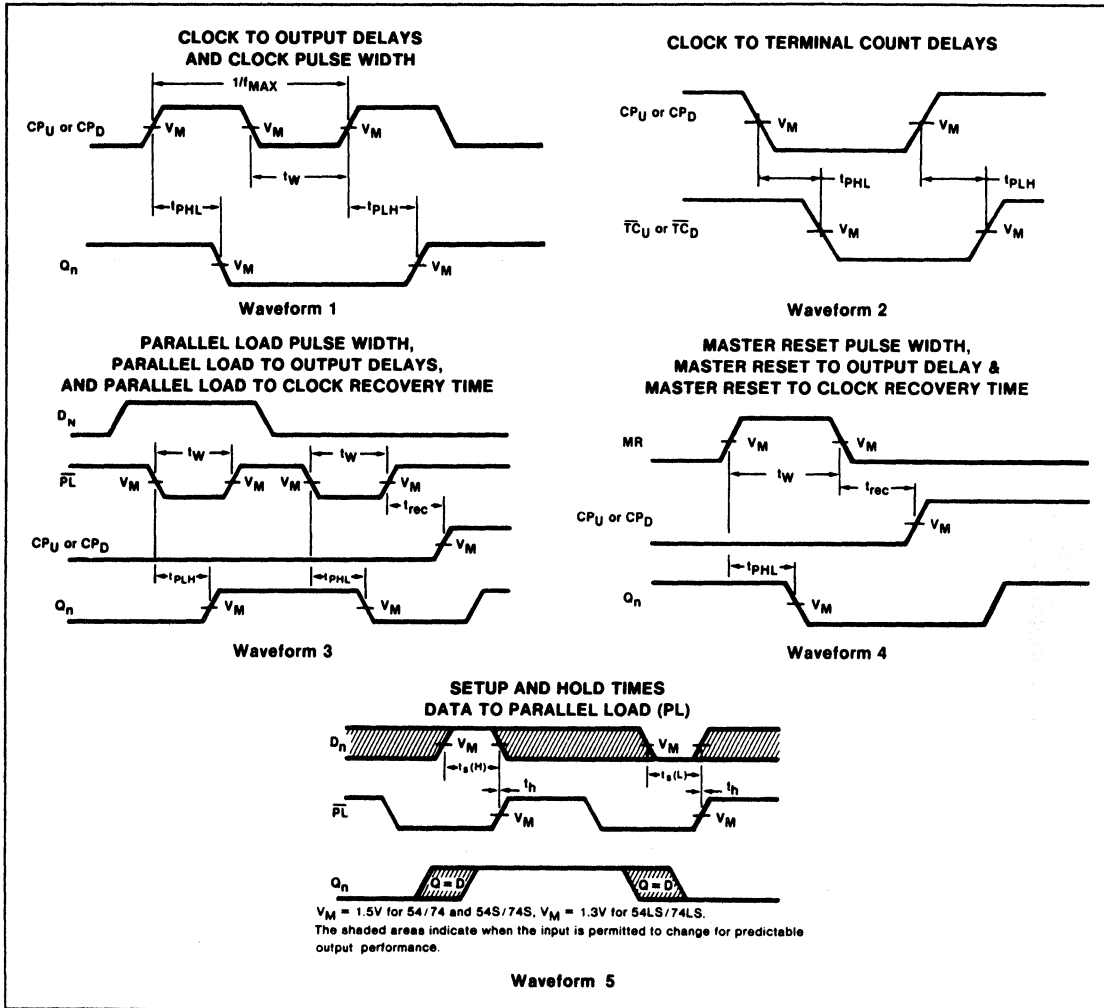
- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS

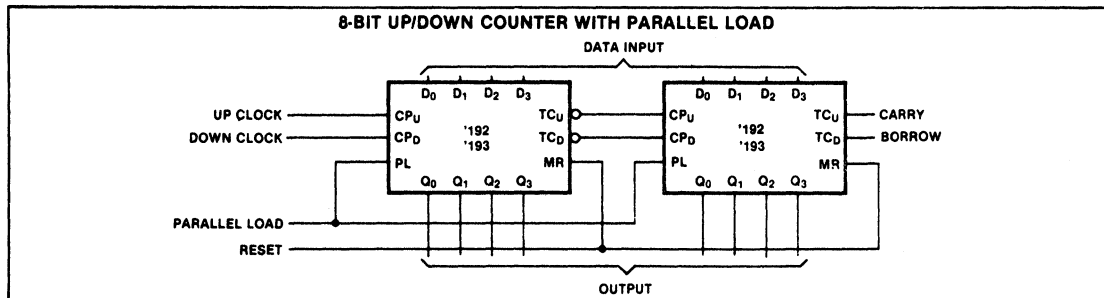
54/74192, 54/74193, LS192, LS193

AC WAVEFORMS



4

APPLICATION



SHIFT REGISTERS

54/74194, LS194A, S194

4-Bit Bidirectional Universal Shift Register

- Buffered clock and control inputs
- Shift left and shift right capability
- Synchronous parallel and serial data transfers
- Easily expanded for both serial and parallel operation
- Asynchronous Master Reset
- Hold (do nothing) mode

DESCRIPTION

The functional characteristics of the '194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 20ns (typical) for the 54/74 and 54LS/74LS, and 12ns (typical) for 54S/74S, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The '194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1 . As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, Q_0-Q_1 , etc.) or, right to left (shift left, Q_3-Q_2 , etc.) or, parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR} , D_{SL}) to allow multistage

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74194	36MHz	39mA
74LS194A	36MHz	15mA
74S194	105MHz	85mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74194N • N74LS194AN N74S194N	
Plastic SO	N74LS194AD • N74S194D	
Ceramic DIP		S54194F • S54LS194AF S54S194F
Flatpack		S54194W • S54LS194AW S54S194W
LLCC		S54194G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1uI	1Sul	1LSul
Q_0-Q_3	Outputs	10uI	10Sul	10LSul

NOTE

Where a 54/74 unit load (uI) is understood to be 40 μ A I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

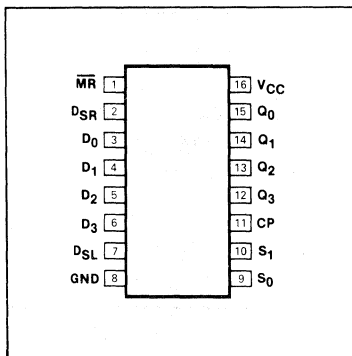
shift right or shift left data transfers without interfering with parallel load operation.

Mode Select and Data inputs on the 54S/74S194 and 54LS/74LS194A are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. The Mode Select inputs of the 54/74194 are

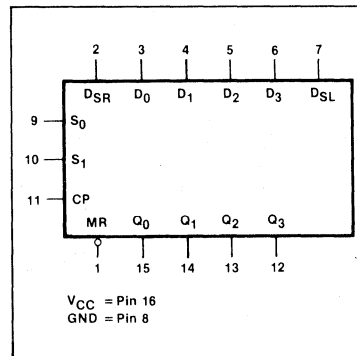
gated with the clock and should be changed from HIGH-to-LOW only while the Clock input is HIGH.

The four parallel data inputs (D_0-D_3) are D-type inputs. Data appearing on D_0-D_3 inputs when S_0 and S_1 are HIGH is transferred to the Q_0-Q_3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset (\overline{MR}) overrides all other input conditions and forces the Q outputs LOW.

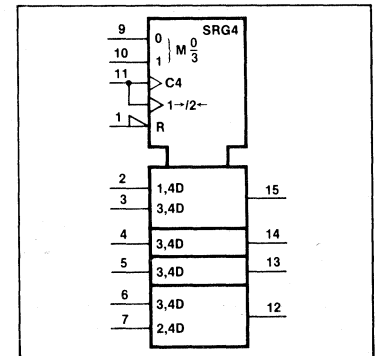
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	\overline{MR}	S ₁	S	D _{SR}	D _{SL}	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l ^(a)	l ^(a)	X	X	X	q ₀	q ₁	q ₂	q ₃
Shift Left	l	H	h	l ^(a)	X	l	X	q ₁	q ₂	q ₃	L
	l	H	h	l ^(a)	X	h	X	q ₁	q ₂	q ₃	H
Shift Right	l	H	l ^(a)	h	l	X	X	L	q ₀	q ₁	q ₂
	l	H	l ^(a)	h	h	X	X	H	q ₀	q ₁	q ₂
Parallel Load	l	H	h	h	X	X	d _n	d ₀	d ₁	d ₂	d ₃

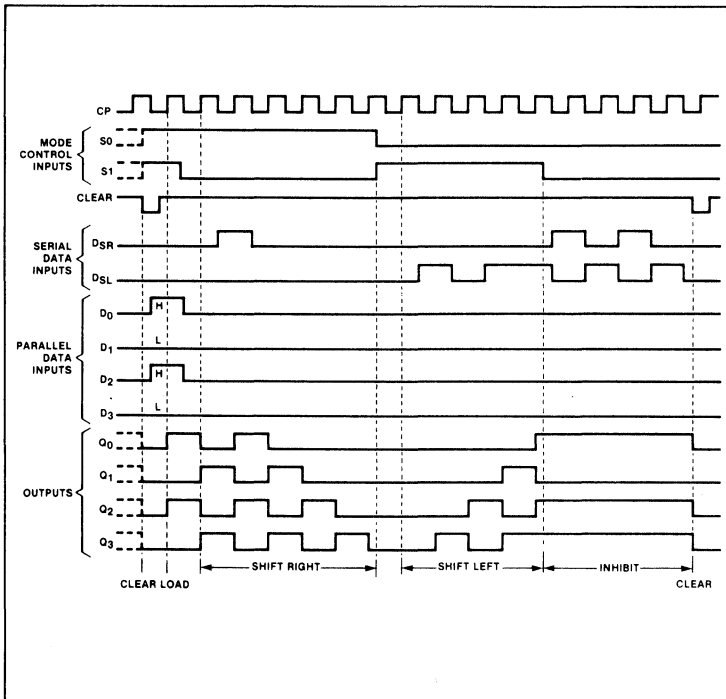
H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 d_n(q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 l = LOW-to-HIGH clock transition.

NOTES

a. The HIGH-to-LOW transition of the S₀ and S₁ inputs on the 54/74194 should only take place while CP is HIGH for conventional operation.



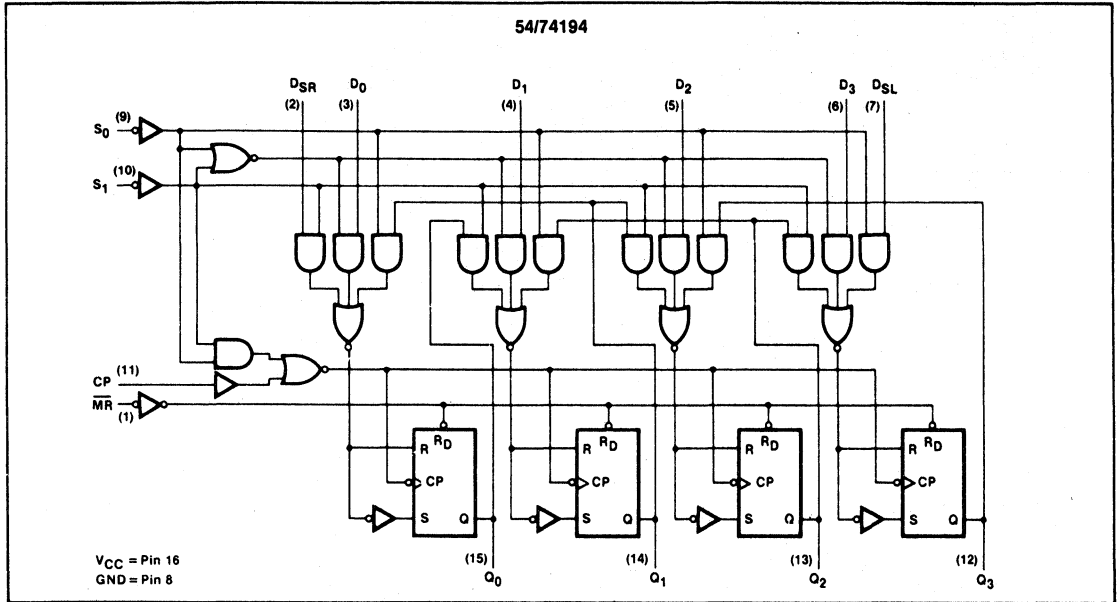
TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



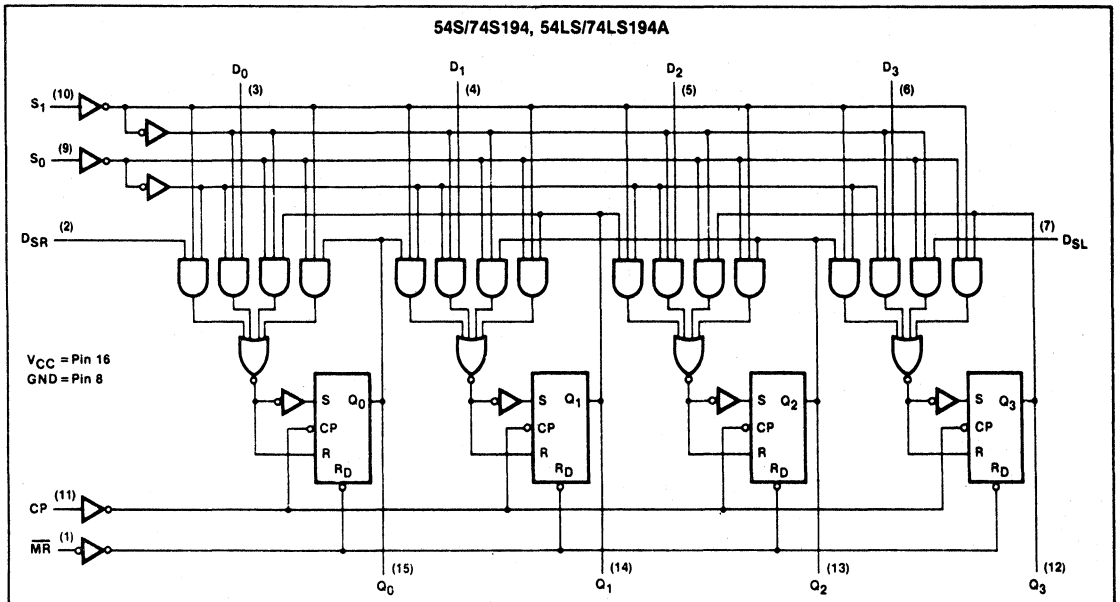
SHIFT REGISTERS

54/74194, LS194A, S194

LOGIC DIAGRAM



LOGIC DIAGRAM



SHIFT REGISTERS

54/74194, LS194A, S194

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			2.0			V	
V_{IL}	LOW-level input voltage	Mil		+0.8			+0.7			+0.8	V	
		Com'l		+0.8			+0.8			+0.8	V	
I_{IK}	Input clamp current			-12			-18			-18	mA	
I_{OH}	HIGH-level output current			-800			-400			-1000	μA	
I_{OL}	LOW-level output current	Mil		16			4			20	mA	
		Com'l		16			8			20	mA	
T_A	Operating free-air temperature	Mil	-55	+125	-55		+125	-55		+125	°C	
		Com'l	0	70	0		70	0		70	°C	

NOTE

 $V_{IL} = +0.7V$ MAX for 54S at $T_A = +125^\circ\text{C}$ only.

4

SHIFT REGISTERS

54/74194, LS194A, S194

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74194			54/74LS194A			54/74S194			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.5		2.5	3.4	V	
		Com'l	2.4	3.4		2.7	3.5		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.25	0.4		0.5 ⁵	V	
			Com'l		0.2	0.4		0.35	0.5		0.5	V
		I _{OL} = 4mA	74LS					0.25	0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0					1.0	mA	
		V _I = 7.0V						0.1			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40						μA	
		V _I = 2.7V						20		50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-1.6			-0.4			mA	
		V _I = 0.5V								-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20		-57	-20		-100	-40	-100	mA	
		Com'l	-18		-57	-20		-100	-40	-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		39	63		15	23		85	135	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With all outputs open, D_i inputs grounded and 4.5V applied to S₀, S₁, \overline{MR} and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		25		70		MHz
t _{PLH} Propagation delay	Waveform 1		22		22	4.0	12	ns
t _{PHL} Clock to output			26		26	4.0	16.5	
t _{PHL} Propagation delay MR to output	Waveform 2		37		30		18.5	ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

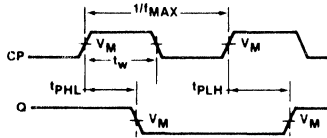
PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		Min	Max	Min	Max	Min	Max	
t _{W(H)} Clock pulse width, HIGH	Waveform 1	20		20		7		ns
t _{W(L)} \overline{MR} pulse width, LOW	Waveform 2	20		20		12		ns
t _s Setup time, Data to Clock	Waveform 3	20		20		5.0		ns
t _h Hold time, Data to Clock	Waveform 3	0		0		3.0		ns
t _{s(L)} Setup time LOW, S _n to CP ^(a)	Waveform 4	30		30		11		ns
t _{s(H)} Setup time HIGH, S _n to CP	Waveform 4	30		30		11		ns
t _h Hold time, S _n to CP	Waveform 4	0		0		3.0		ns
t _{rec} Recovery time, \overline{MR} to CP	Waveform 2	25		25		9.0		ns

SHIFT REGISTERS

54/74194, LS194A, S194

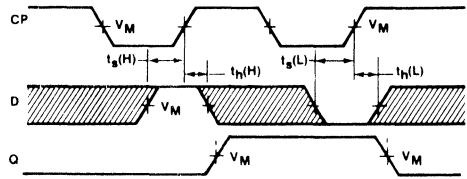
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SET-UP AND HOLD TIMES

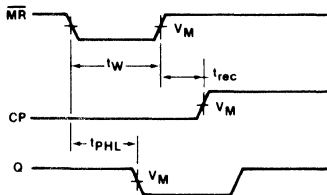


Waveform 3

$V_M = 1.5V$ for 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

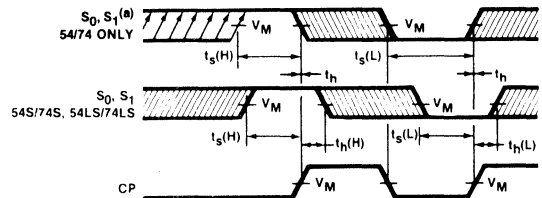
The shaded areas indicate when the input is permitted to change predictable output performance

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

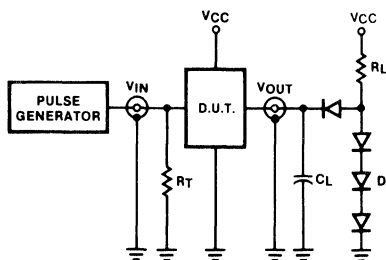
SETUP AND HOLD TIMES FOR S₀ AND S₁ INPUTS



Waveform 4

TEST CIRCUITS AND WAVEFORMS

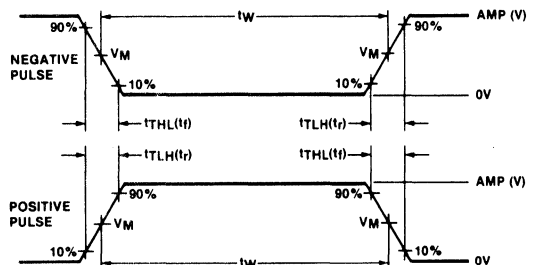
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

4

SHIFT REGISTERS

54/74195, LS195A, S195

4-Bit Parallel Access Shift Register

- Buffered Clock and Control inputs
- Shift right and parallel load capability
- J-K (D) inputs to first stage
- Complement output from last stage
- Asynchronous Master Reset

DESCRIPTION

The functional characteristics of the '195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The '195 operates on two primary modes: shift right (Q_0-Q_1) and parallel load, which are controlled by the state of the Parallel Enable (\overline{PE}) input. Serial data enters the first flip-flop (Q_0) via the J and \overline{K} inputs when the \overline{PE} input is HIGH, and is shifted 1 bit in the direction $Q_0-Q_1-Q_2-Q_3$ following each LOW-to-HIGH clock transition. The J and \overline{K} inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the \overline{PE} input is LOW. After the LOW-to-HIGH clock transition, data on the parallel

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74195	39MHz	39mA
74LS195A	39MHz	14mA
74S195	105MHz	70mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74195N • N74LS195AN N74S195N	
Plastic SO	N74LS195AD	
Ceramic DIP		S54LS195AF
Flatpack		S54LS195AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1uI	1Sul	1LSul
All	Outputs	10uI	10Sul	10LSul

NOTE

Where a 54/74 unit load (uI) is understood to be 40uA I_{IH} and -1.6mA I_{IL} , a 54/74S unit load (Sul) is 50uA I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSul) is 20uA I_{IH} and -0.4mA I_{IL} .

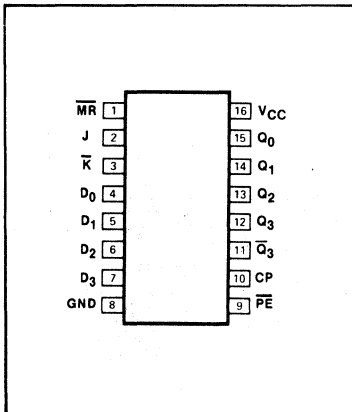
inputs (D_0-D_3) is transferred to the respective Q_0-Q_3 outputs. Shift left operation (Q_3-Q_2) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the \overline{PE} input low.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The '195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, \overline{K} , D_n ,

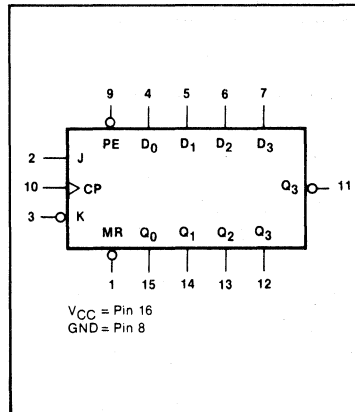
and \overline{PE} inputs for logic operation, other than the setup and release time requirements.

A LOW on the asynchronous Master Reset (\overline{MR}) input sets all Q outputs LOW, independent of any other input condition. The \overline{MR} on the 54/74195 is gated with the clock. Therefore, the LOW-to-HIGH \overline{MR} transition should only occur while the clock is LOW to avoid false clocking on the 54/74195.

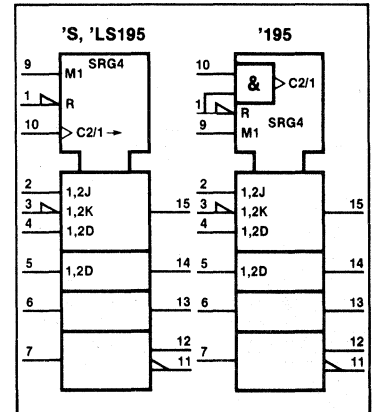
PIN CONFIGURATION



LOGIC SYMBOL



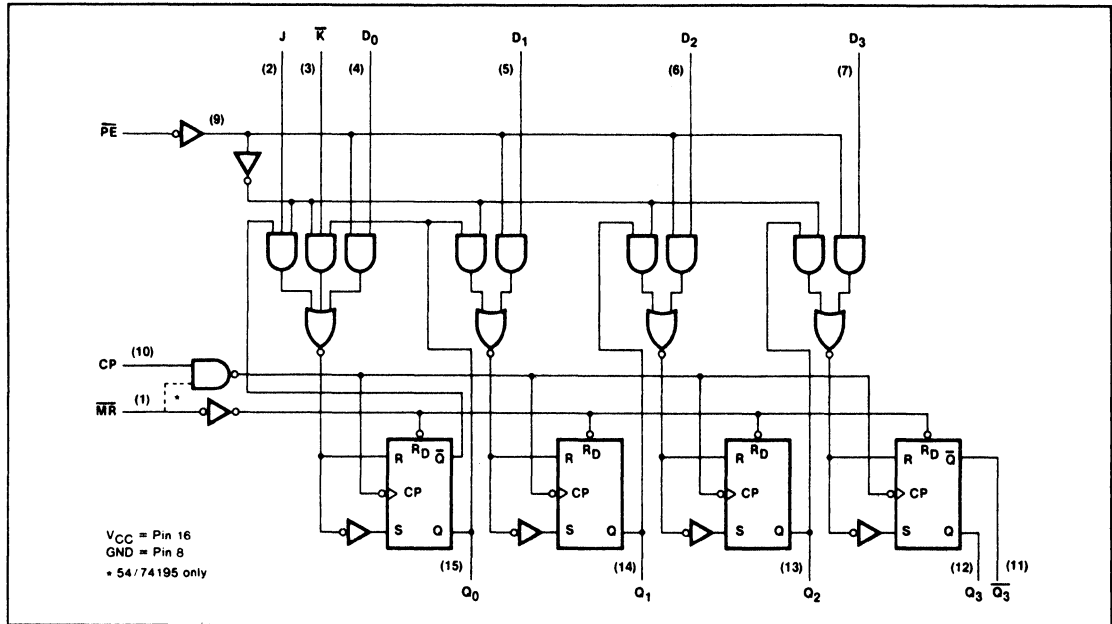
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTERS

54/74195, LS195A, S195

LOGIC DIAGRAM



4

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	MR	CP	PE	J	K	D _n	Q ₀	Q ₁	Q ₂	Q ₃	Q ₃ [̄]
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q ₀	q ₁	q ₂	q ₂ [̄]
Shift, Reset First Stage	H	↑	h	l	l	X	L	q ₀	q ₁	q ₂	q ₂ [̄]
Shift, Toggle First Stage	H	↑	h	h	l	X	q ₀ [̄]	q ₀	q ₁	q ₂	q ₂ [̄]
Shift, Retain First Stage	H	↑	h	l	h	X	q ₀	q ₀	q ₁	q ₂	q ₂ [̄]
Parallel Load	H	↑	l	X	X	d _n	d ₀	d ₁	d ₂	d ₃	d ₃ [̄]

H = HIGH voltage level.
 L = LOW voltage level.
 X = Don't care.
 ↑ = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125			0 to 70			°C

SHIFT REGISTERS

54/74195, LS195A, S195

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.8			+ 0.7			+ 0.8	V
		Com'l			+ 0.8			+ 0.8			+ 0.8	V
I _{IK}	Input clamp current			- 12			- 18			- 18	mA	
I _{OH}	HIGH-level output current			- 800			- 400			- 1000	μA	
I _{OL}	LOW-level output current	Mil		16			4			20	mA	
		Com'l		16			8			20	mA	
T _A	Operating free-air temperature	Mil	- 55		+ 125	- 55		+ 125	- 55		+ 125	°C
		Com'l	0		70	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74195			54/74LS195A			54/74S195			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, I _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4		2.7	3.4	V		
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.25	0.4			0.5	V	
		I _{OL} = 4mA	Com'l		0.2	0.4		0.35	0.5			0.5	V
			74LS					0.25	0.4				V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			- 1.5			- 1.5			- 1.2	V		
I _I	Input current at maximum input voltage V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA	
		V _I = 7.0V						0.1				mA	
I _{IH}	HIGH-level input current V _{CC} = MAX	V _I = 2.4V			40							μA	
		V _I = 2.7V						20			50	μA	
I _{IL}	LOW-level input current V _{CC} = MAX	V _I = 0.4V			- 1.6			- 0.4				mA	
		V _I = 0.5V									- 2	mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	Mil	- 20		- 57	- 20		- 100	- 40		- 100	mA	
		Com'l	- 18		- 57	- 20		- 100	- 40		- 100	mA	
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX	Mil		39	63		14	21		70	99	mA	
		Com'l		39	63		14	21		70	109	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With all outputs open, \overline{PE} grounded, and 4.5V applied to the J, \overline{K} , and Data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V to \overline{MR} , and then a momentary ground, followed by 4.5V to clock.

SHIFT REGISTERS

54/74195, LS195A, S195

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT	
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$			
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Maximum clock frequency	Waveform 1		30		30		70	MHz
t_{PLH}	Propagation delay	Waveform 1			22		22	12	ns
t_{PHL}	Clock to output	Waveform 1			26		26	16.5	
t_{PHL}	Propagation delay MR to output	Waveform 2			30		30	18.5	ns

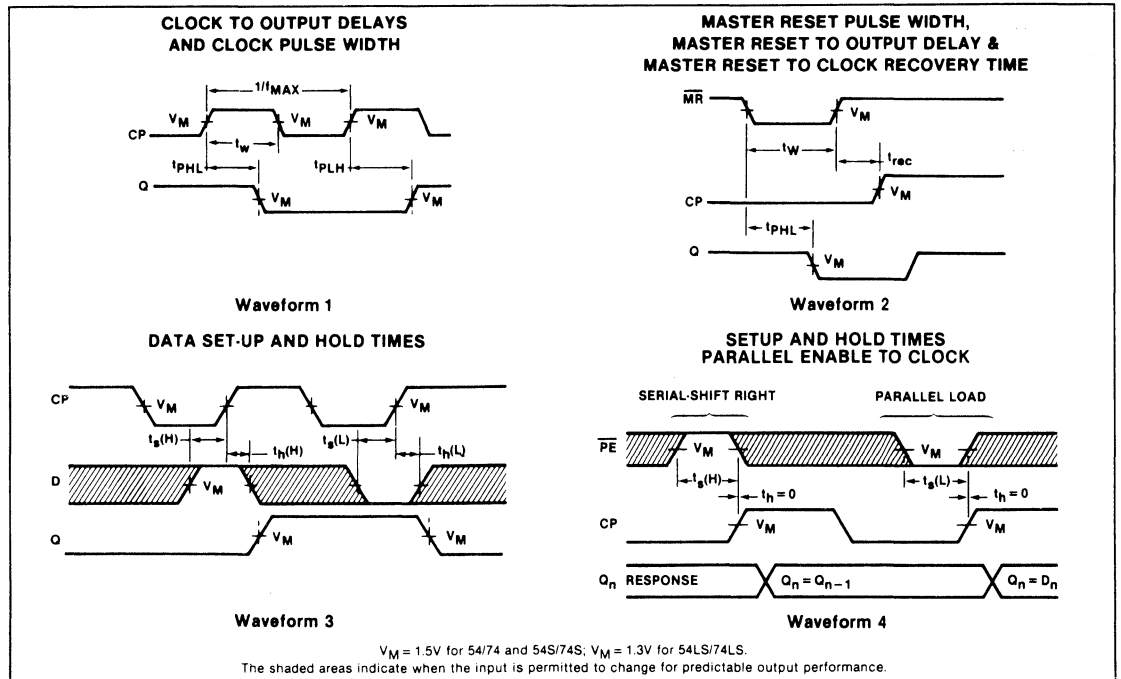
NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT	
		Min	Max	Min	Max	Min	Max		
t_W	Clock pulse width	Waveform 1		16		16		7	ns
t_W	Master Reset pulse width	Waveform 2		12		12		12	ns
t_s	Setup time, J, \bar{K} and Data to Clock	Waveform 3		20		15		5.0	ns
t_h	Hold time, J, \bar{K} and Data to Clock	Waveform 3		0		0		3.0	ns
t_s	Setup time, \bar{PE} to Clock	Waveform 4		25		25		11	ns
t_h	Hold time, \bar{PE} to Clock	Waveform 4		0		0		0	ns
t_{rec}	Recovery time, \bar{MR} to Clock	Waveform 2		25		25		9.0	ns

AC WAVEFORMS



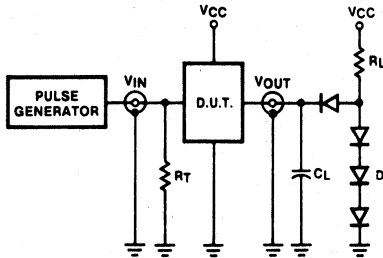
4

SHIFT REGISTERS

54/74195, LS195A, S195

TEST CIRCUITS AND WAVEFORMS

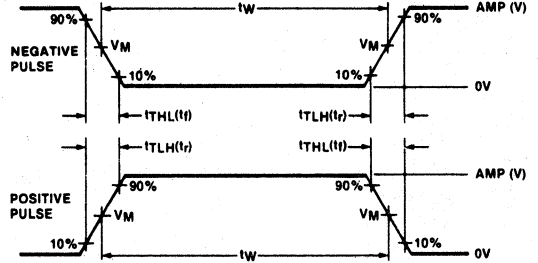
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTER

54/74LS197

Presetable 4-Bit Binary Ripple Counter

- High speed 4-bit binary counting
- Asynchronous parallel load for presetting counter
- Overriding Master Reset
- Buffered Q₀ output drives CP₁ input plus standard fan-out

TYPE	TYPICAL f _{MAX}	TYPICAL SUPPLY CURRENT
74LS197	40MHz	16mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = - 55°C to + 125°C
Plastic DIP	N74LS197N	
Plastic SO	N74LS197D	
Ceramic DIP		S54LS197F
Flatpack		S54LS197W

DESCRIPTION

The '197 is an asynchronously presetable binary ripple counter partitioned into divide-by-2 and divide-by-8 sections with each section having a separate Clock input. State changes are initiated in the counting modes by the HIGH-to-LOW transition of the Clock inputs, however, state changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs, that the unequal delays can lead to decoding spikes, and thus a decoded signal should not be used as a strobe or clock. The Q₀ flip-flop is triggered by the CP₀ input while the CP₁ input triggers the divide-by-8 section.

The device has an asynchronous active-LOW Master Reset (MR) input which overrides all other inputs and forces all out-

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

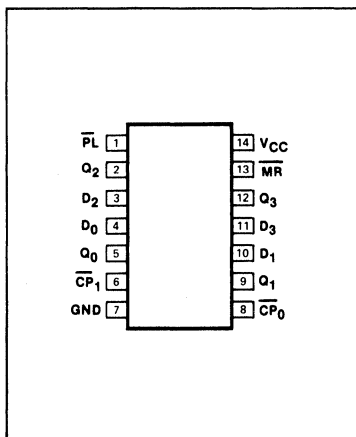
PINS	DESCRIPTION	54/74LS
CP ₀	Clock input	6LSul
CP ₁	Clock input	3.5LSul
All	Other inputs	1LSul
Q ₀ -Q ₃	Outputs	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20µA I_{IH} and - 0.4mA I_{IL}.

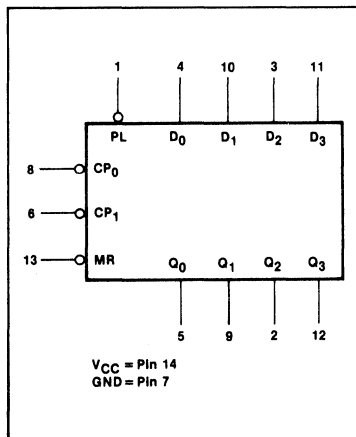
puts LOW. The counter is also asynchronously presetable. A LOW on the Parallel Load (PL) input overrides the Clock inputs and loads the data from parallel Data (D₀-

D₃) inputs into the flip-flops. The counter acts as a transparent latch while the PL is LOW and any change in the D_n inputs will be reflected in the outputs.

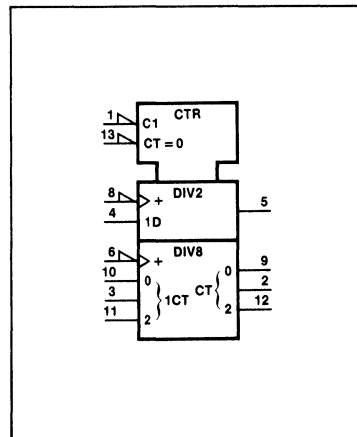
PIN CONFIGURATION



LOGIC SYMBOL



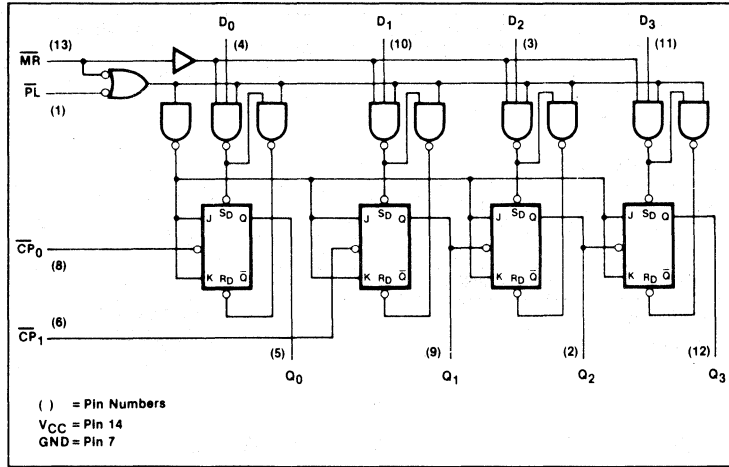
LOGIC SYMBOL (IEEE/IEC)



COUNTER

54/74LS197

LOGIC DIAGRAM



COUNT SEQUENCE

COUNT	4-BIT BINARY ¹			
	Q ₃	Q ₂	Q ₁	Q ₀
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE
 1. Q₀ connected to input \overline{CP}_1 ; input applied to \overline{CP}_0 .

MODE SELECT— FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUT
	MR	PL	CP	D _n	Q _n
Reset (Clear)	L	X	X	X	L
Parallel Load	H	L	X	L	L
	H	L	X	H	H
Count	H	H	↓	X	count

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↓ = HIGH-to-LOW Clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +1	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74LS			UNIT	
	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+0.7	V
	Com'l			+0.8	V
I _{IK} Input clamp current				-18	mA
I _{OH} HIGH-level output current				-400	μA
I _{OL} LOW-level output current	Mil			4	mA
	Com'l			8	mA
T _A Operating free-air temperature	Mil	-55		+125	°C
	Com'l	0		70	°C

COUNTER

54/74LS197

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS197			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V	
		Com'l	2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	Mil		0.25	0.4	V
		Com'l		0.35	0.5	V
	I _{OL} = MAX					
	I _{OL} = 4mA	74LS		0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				- 1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V	D ₀ -D ₃ , \overline{PL}			0.1	mA
		\overline{MR} , $\overline{CP_0}$, $\overline{CP_1}$			0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	D ₀ -D ₃ , \overline{PL}			20	μ A
		\overline{MR} , $\overline{CP_0}$, $\overline{CP_1}$			40	μ A
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	D ₀ -D ₃ , \overline{PL}			- 0.4	mA
		\overline{MR} input			- 0.8	mA
		$\overline{CP_0}$ input			- 2.4	mA
		$\overline{CP_1}$ input			- 1.3	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		- 20		- 100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			16	27	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with all inputs grounded and all outputs open.



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 15pF, R _L = 2k Ω		
		Min	Max	
f _{MAX} Maximum count frequency	Waveform 1	$\overline{CP_0}$	30	MHz
		$\overline{CP_1}$	15	MHz
t _{PLH} t _{PHL} Propagation delay CP ₀ to Q ₀	Waveform 1		15 21	ns
t _{PLH} t _{PHL} Propagation delay CP ₁ to Q ₁	Waveform 1		19 35	ns
t _{PLH} t _{PHL} Propagation delay CP ₁ to Q ₂	Waveform 1		51 63	ns
t _{PLH} t _{PHL} Propagation delay CP ₁ to Q ₃	Waveform 1		78 95	ns
t _{PLH} t _{PHL} Propagation delay Data to output	Waveform 2		27 44	ns
t _{PLH} t _{PHL} Propagation delay PL to output	Waveform 3		39 45	ns
t _{PHL} Propagation delay MR to output	Waveform 4		51	ns

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

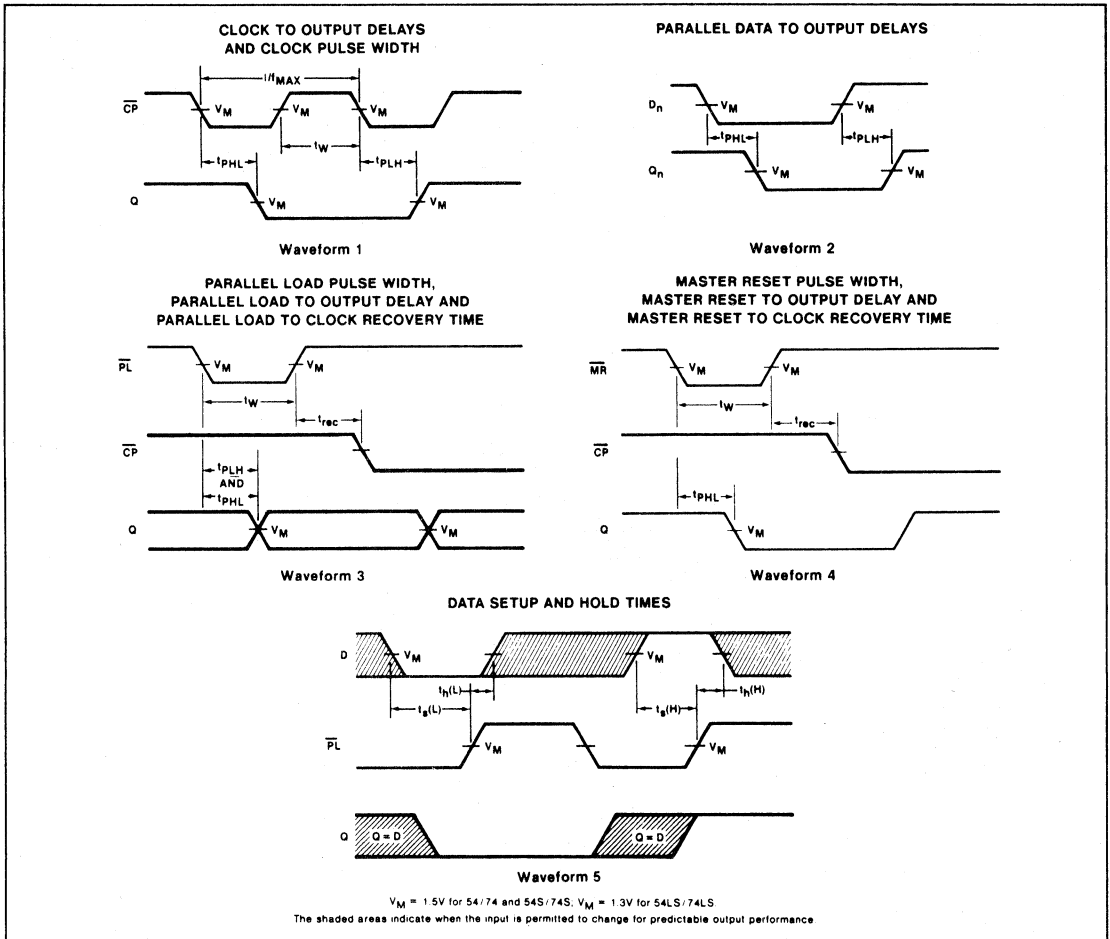
COUNTER

54/74LS197

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

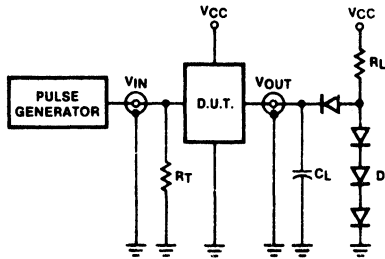
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_w Clock pulse width	Waveform 1	\overline{CP}_0	20	ns
		\overline{CP}_1	30	ns
t_w \overline{MR} pulse width	Waveform 4	15		ns
t_w \overline{PL} pulse width	Waveform 3	20		ns
$t_s(H)$ Setup time HIGH Data to \overline{PL}	Waveform 5	10		ns
$t_h(H)$ Hold time HIGH Data to \overline{PL}	Waveform 5	20		ns
$t_s(L)$ Setup time LOW Data to \overline{PL}	Waveform 5	15		ns
$t_h(L)$ Hold time LOW Data to \overline{PL}	Waveform 5	20		ns
t_{rec} Recovery time \overline{MR} to \overline{CP}	Waveform 4	30		ns
t_{rec} Recovery time \overline{PL} to \overline{CP}	Waveform 3	30		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

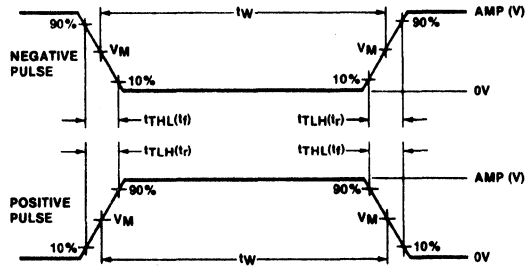
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTER

54/74199

8-Bit Parallel-Access Shift Register

- Buffered clock and control inputs
- Shift right and parallel load capability
- Fully synchronous data transfers
- J-K (D) inputs to first stage
- Clock enable for hold (do nothing) mode
- Asynchronous Master Reset

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74199	35MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74199N	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
All	Inputs	1ul
Q_0-Q_7	Parallel outputs	10ul

NOTE

A 54/74 unit load (ul) is understood to be $40\mu A$ I_{IH} AND $-1.6mA$ I_{IL} .

DESCRIPTION

The functional characteristics of the '199 8-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

The '199 operates in two primary modes: shift right (Q_0-Q_1) and parallel load, which are controlled by the state of the Parallel Enable (\overline{PE}) input. Serial data enters the first flip-flop (Q_0) via the J and \overline{K} inputs when the \overline{PE} input is HIGH, and is shifted one bit in the direction $Q_0-Q_1-Q_3$ following each LOW-to-HIGH clock transition. The J and \overline{K} inputs provide the flexibility of the J-K type input for special ap-

plications and, by tying the two pins together, the simple D-type input for general applications. The device appears as eight common clocked D flip-flops when the \overline{PE} input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0-D_7) is transferred to the respective Q_0-Q_7 outputs.

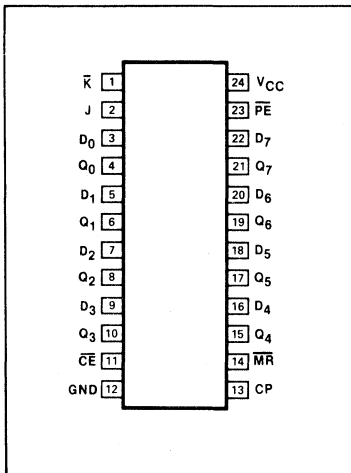
All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The '199 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, \overline{K} , D_n , and \overline{PE} inputs for logic operation, other

than the setup and release time requirements.

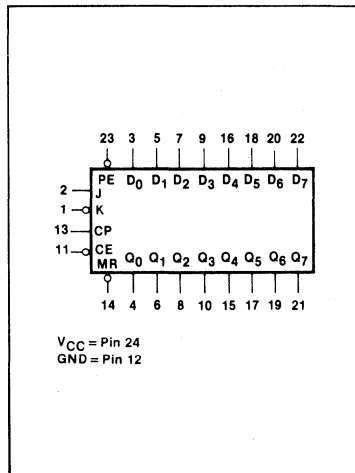
The clock input is a gated OR structure which allows one input to be used as an active-LOW Clock Enable (\overline{CE}) input. The pin assignment for the CP and \overline{CE} inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of \overline{CE} input should only take place while the CP is HIGH for conventional operation.

A LOW on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

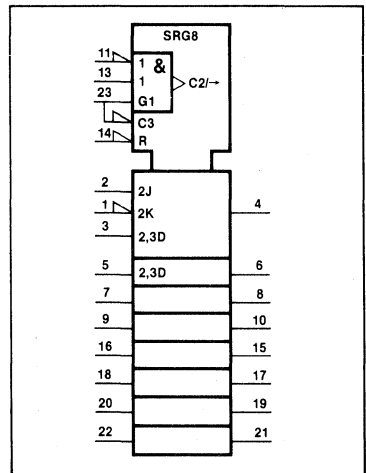
PIN CONFIGURATION



LOGIC SYMBOL



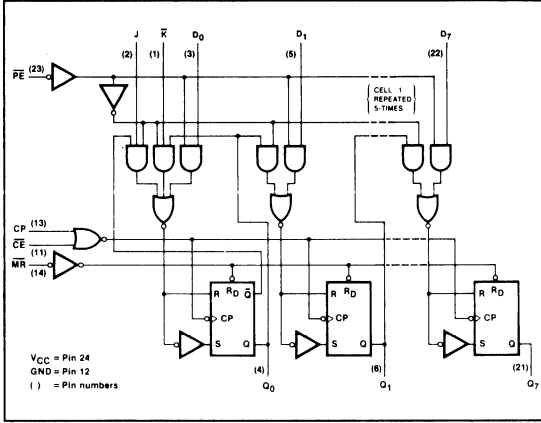
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER

54/74199

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

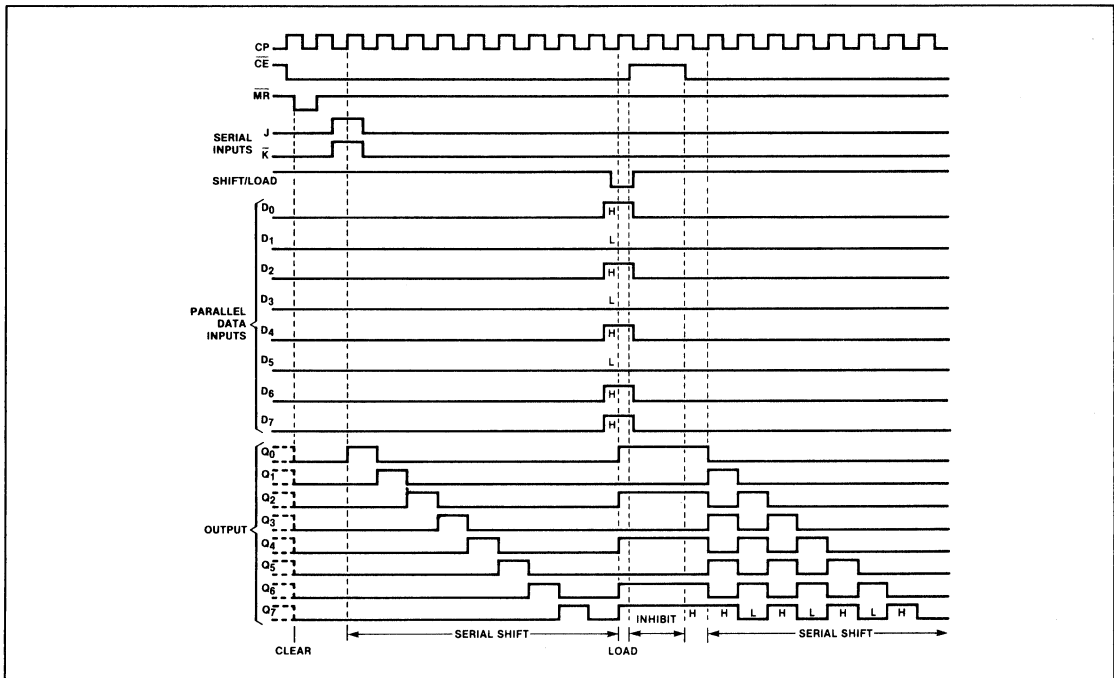
OPERATING MODES	INPUTS						OUTPUTS	
	\overline{MR}	CP	\overline{CE}	\overline{PE}	J	\overline{K}	D_n	Q_0 Q_1 ... Q_6 Q_7
Reset (clear)	L	X	X	X	X	X	X	L L ... L L
Shift, Set First Stage	H	↑	l	h	h	h	X	H Q_0 ... Q_5 Q_6
Shift, Reset First Stage	H	↑	l	h	l	l	X	L Q_0 ... Q_5 Q_6
Shift, Toggle First Stage	H	↑	l	h	h	l	X	$\overline{Q_0}$ Q_0 ... Q_5 Q_6
Shift, Retain First Stage	H	↑	l	h	l	h	X	Q_0 Q_0 ... Q_5 Q_6
Parallel Load	H	↑	l	l	X	X	d_n	d_0 d_1 ... d_6 d_7
Hold (do nothing)	H	↑	h ^(a)	X	X	X	X	Q_0 Q_1 ... Q_6 Q_7

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 l = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 $d_n(Q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
 ↑ = LOW-to-HIGH clock transition.

NOTE
 a. The LOW-to-HIGH transition of \overline{CE} should only occur while CP is HIGH for conventional operation.



TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I_{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage	Mil		+ 0.8	V	
		Com'l		+ 0.8	V	
I_{IK}	Input clamp current			- 12	mA	
I_{OH}	HIGH-level output current			- 800	μA	
I_{OL}	LOW-level output current	Mil		16	mA	
		Com'l		16	mA	
T_A	Operating free-air temperature	Mil	- 55	+ 125	°C	
		Com'l	0	70	°C	

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		54/74199			UNIT
				Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}$	Mil	2.4	3.4		V
			Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = \text{MAX}$	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			- 1.5	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA	
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$			40	μA	
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			- 1.6	mA	
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	Mil	- 20		- 57	mA
			Com'l	- 18		- 57	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$		90	127	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with \bar{K}, J and D inputs at 4.5V, momentary ground clock, then apply 4.5V, ground \bar{CE}, \bar{MR} and \bar{PE} .

SHIFT REGISTER

54/74199

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		
		Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} Propagation delay Clock to output	Waveform 1		26	ns
t_{PHL} Propagation delay MR to output			30	
t_{PHL} Propagation delay MR to output	Waveform 2		35	ns

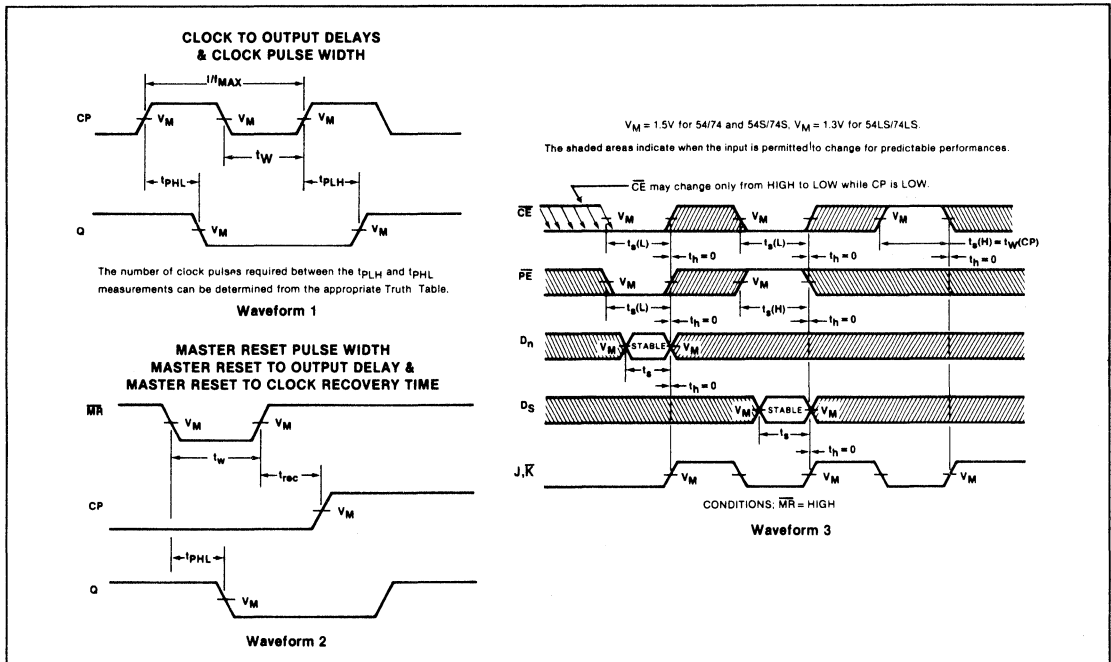
Per industry convention, f_{MAX} is the worst case of the maximum device operating frequency with no constraints on t_f , t_r , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74		UNIT
		Min	Max	
t_W Clock pulse width	Waveform 1	20		ns
t_W MR pulse width	Waveform 2	20		ns
t_s Setup time, J, \bar{K} and Data to clock	Waveform 3	20		ns
t_h Hold time, J, \bar{K} and Data to clock	Waveform 3	0		ns
t_s Setup time, \bar{CE} to clock	Waveform 3	30		ns
t_h Hold time, \bar{CE} to clock	Waveform 3	0		ns
t_s Setup time, \bar{PE} to clock	Waveform 3	30		ns
t_h Hold time, \bar{PE} to clock	Waveform 3	0		ns
t_{rec} Recovery time, MR to clock	Waveform 2	30		ns

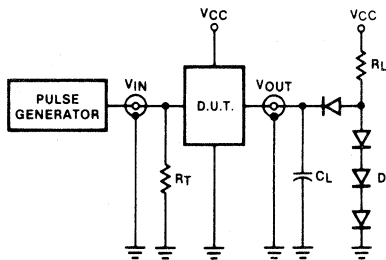
4

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

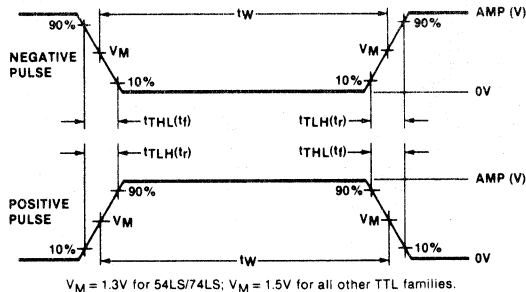
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIVIBRATOR

54/74221

Dual Monostable Multivibrator

- Pulse width variance is typically less than $\pm 0.5\%$ for 98% of the units
- The '221 demonstrates electrical and switching characteristics that are virtually identical to the '121 one-shots
- Pin-out is identical to the '123
- Overriding Reset terminates output pulse
- B input has hysteresis for improved noise immunity
- Maximum pulse width:
54221: 21 seconds
74221: 28 seconds

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74221	42ns	36mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74221N	
Plastic SO	N74221D	
Ceramic DIP		S54221F
Flatpack		S54221W

FUNCTION TABLE

(Each monostable)

INPUTS			OUTPUTS	
\bar{R}_D	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	L		
H	L	H		
L	L	H		

In addition, see description and switching characteristics.

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 ↑ = LOW-to-HIGH transition
 ↓ = HIGH-to-LOW transition
 = One HIGH-level pulse
 = One LOW-level pulse

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
\bar{A}	Input	1uI
B, \bar{R}_D	Inputs	2uI
All	Outputs	10uI

NOTE
 A 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$.

DESCRIPTION

The '221 is a dual monostable multivibrator with performance characteristics virtually identical to those of the '121. Each multivibrator features an active LOW going edge input (\bar{A}) and an active HIGH going edge input (B), either of which can be used as an Enable input.

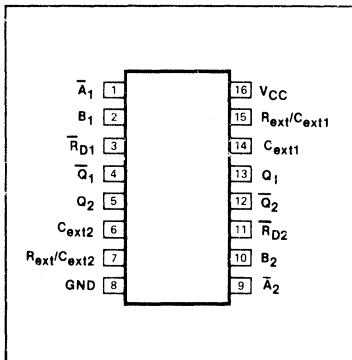
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the \bar{A} and B inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW Reset (\bar{R}_D). Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the FEA-

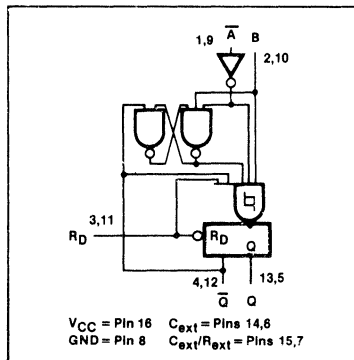
TURES by choosing appropriate timing components. With $R_{ext} = 2k\Omega$ and $C_{ext} = 0$, an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In
 (Continued)

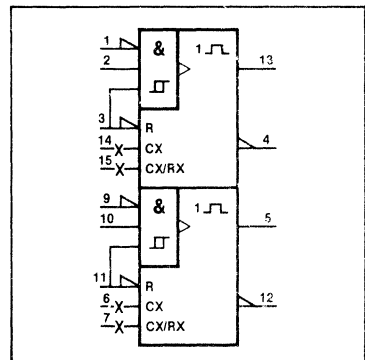
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MULTIVIBRATOR

54/74221

DESCRIPTION (Continued)

most applications, pulse stability will only be limited by the accuracy of external timing components.

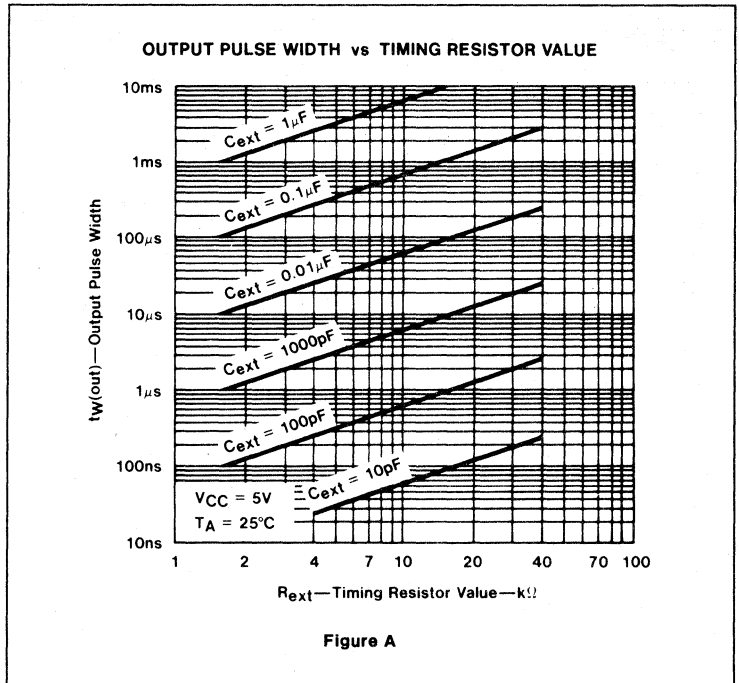
Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10 μ F) and more than one decade of timing resistance (2k Ω to 30k Ω for the 54221 and 2k Ω to 40k Ω for the 74221). Throughout these ranges, pulse width is defined by the following relationship: (see Figure A)

$$t_w(\text{out}) = C_{\text{ext}} R_{\text{ext}} \ln 2$$

$$t_w(\text{out}) \cong 0.7 C_{\text{ext}} R_{\text{ext}}$$

In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μ F and timing resistance as low as 1.4k Ω may be used.

Pin assignments for these devices are identical to those of the '123 so that the '221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext} .



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	74	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	$^{\circ}$ C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			UNIT
		Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
I_{IK} Input clamp current				-12	mA
I_{OH} HIGH-level output current				-800	μ A
I_{OL} LOW-level output current	Mil			16	mA
	Com'l			16	mA
T_A Operating free-air temperature	Mil	-55		+125	$^{\circ}$ C
	Com'l	0		70	$^{\circ}$ C

MULTIVIBRATOR

54/74221

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74221			UNIT	
		Min	Typ ²	Max		
V _{T+}	Positive-going threshold at A and B V _{CC} = MIN			2.0	V	
V _{T-}	Negative-going threshold at A and B V _{CC} = MIN	0.8			V	
V _{OH}	HIGH-level output voltage V _{CC} = MIN, I _{OH} = MAX	Mil	2.4	3.4	V	
		Com'l	2.4	3.4	V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, I _{OL} = MAX	Mil		0.2	0.4	V
		Com'l		0.2	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.4V	A input		40	μA	
		B, R _D inputs		80	μA	
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V	A input		-1.6	mA	
		B, R _D inputs		-3.2	mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX	Mil	-20	-55	mA	
		Com'l	-18	-55	mA	
I _{CC}	Supply current (total) V _{CC} = MAX	Quiescent		26	50	mA
		Triggered		46	80	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH}	Propagation delay A input to Q & Q output Waveform 1 C _{ext} = 80pF, R _{ext} = 2kΩ		70	ns
t _{PHL}			80	ns
t _{PLH}	Propagation delay B input to Q & Q output Waveform 2 C _{ext} = 80pF, R _{ext} = 2kΩ		55	ns
t _{PHL}			65	ns
t _{PLH}	Propagation delay R _D input to Q & Q output Waveform 3 C _{ext} = 80pF, R _{ext} = 2kΩ		40	ns
t _{PHL}			27	ns
t _W	Minimum output pulse width C _{ext} = 0pF, R _{ext} = 2kΩ	20	50	ns
t _W	C _{ext} = 80pF, R _{ext} = 2kΩ	70	150	ns
	C _{ext} = 100pF, R _{ext} = 10kΩ	650	750	ns
	C _{ext} = 1μF, R _{ext} = 10kΩ	6.5	7.5	ms

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT	
		Min	Max		
t _W	Minimum input pulse width to trigger Waveforms 1 & 2	50		ns	
t _W	Minimum Reset pulse width Waveform 3	20		ns	
t _{rec}	Recovery time from Reset to trigger input Waveform 3	15		ns	
R _{ext}	External timing resistor range	Mil	1.4	30	kΩ
		Com'l	1.4	40	kΩ
C _{ext}	External timing capacitance range	0	1000	μF	
Output duty cycle	R _{ext} = 2kΩ		67	%	
	R _{ext} = R _{ext} (MAX)		90	%	

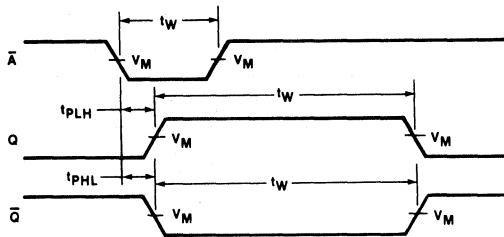
4

MULTIVIBRATOR

54/74221

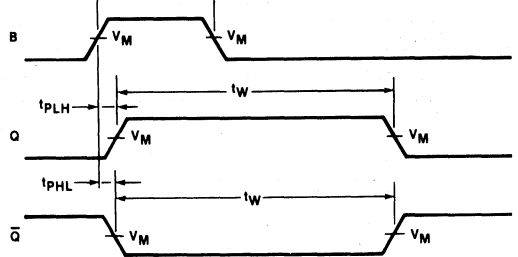
AC WAVEFORMS

PROPAGATION DELAY \bar{A} INPUT TO Q AND \bar{Q} OUTPUTS, AND INPUT AND OUTPUT PULSE WIDTHS



Waveform 1

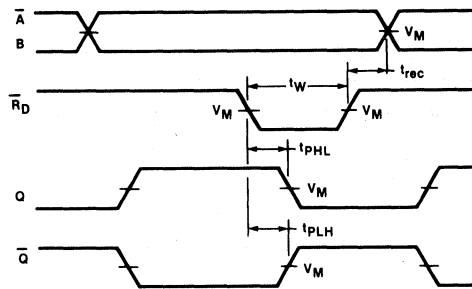
PROPAGATION DELAY B INPUT TO Q AND \bar{Q} OUTPUT, AND INPUT AND OUTPUT PULSE WIDTHS



Waveform 2

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

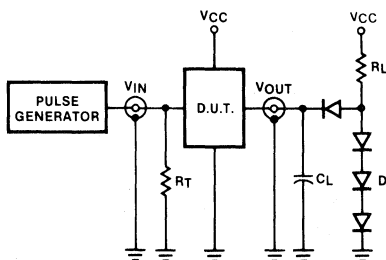
DIRECT RESET DELAYS AND RECOVERY TIME



Waveform 3

TEST CIRCUITS AND WAVEFORMS

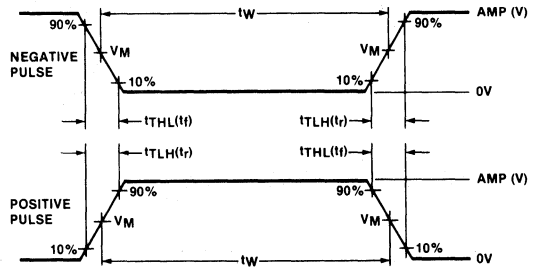
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS

54/74LS240, 54/74LS241, S240, S241

'240 Octal Inverter Buffer (3-State)
'241 Octal Buffer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS240	11ns	24mA
74S240	4.5ns	93mA
74LS241	12ns	25mA
74S241	6ns	112mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = -55°C to + 125°C
Plastic DIP	N74LS240N • N74S240N N74LS241N • N74S241N	
Plastic SO	N74LS240D • N74S240D N74LS241D • N74S241D	
Ceramic DIP		S54LS240F • S54S240F S54LS241F • S54S241F
LLCC		S54LS240G • S54LS241G

FUNCTION TABLE, '240

INPUTS				OUTPUTS	
OE _a	I _a	OE _b	I _b	Y _a	Y _b
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

FUNCTION TABLE, '241

INPUTS				OUTPUTS	
OE _a	I _a	OE _b	I _b	Y _a	Y _b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

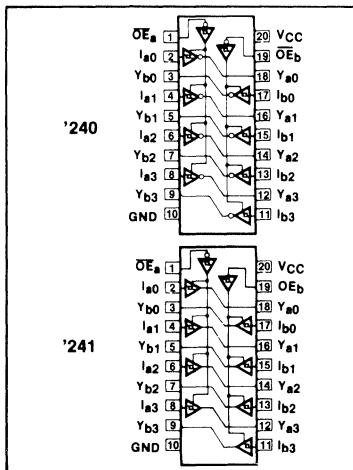
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

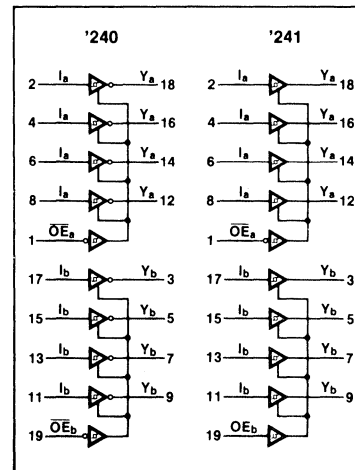
PINS	DESCRIPTION	54/74S	54/74LS
I _{a0} -I _{a3} , I _{b0} -I _{b3}	Inputs	1Sul	1LSul
OE _a , OE _b , OE _b	Inputs	1Sul	1LSul
All	Outputs	24Sul	32LSul

NOTE
A 54/74S unit load (Sul) is 50µA I_{IH} and - 2.0mA I_{IL} and a 54/74LS unit load (LSul) is 20µA I_{IH} and - 0.4mA I_{IL}.

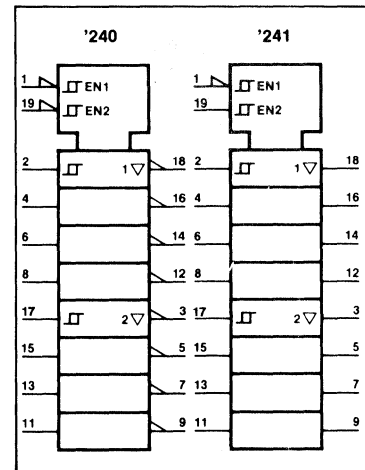
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUFFERS

54/74LS240, 54/74LS241, S240, S241

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

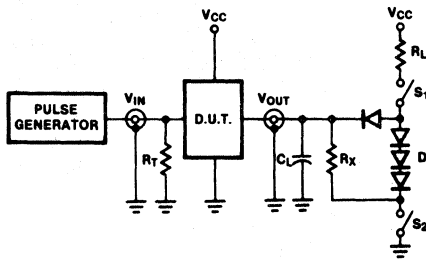
PARAMETER		54LS	54S	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V	
V _{IL}	LOW-level input voltage	Mil				+0.8			V
		Com'l				+0.8			V
I _{IK}	Input clamp current				-18			mA	
I _{OH}	HIGH-level output current	Mil				-12			mA
		Com'l				-15			mA
I _{OL}	LOW-level output current	Mil				12			mA
		Com'l				24			mA
T _A	Operating free-air temperature	Mil	-55	+125		-55	+125		°C
		Com'l	0	70		0	70		°C
External resistance between any input or V _{CC} and ground					40			kΩ	

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



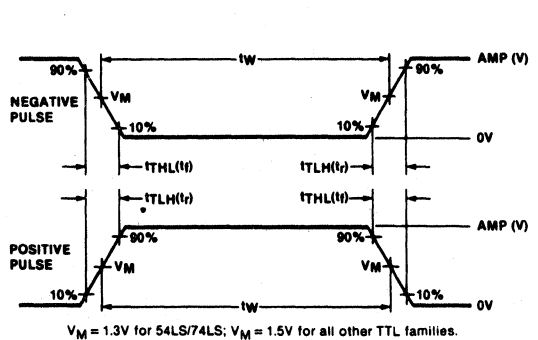
SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generator.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS

54/74LS240, 54/74LS241, S240, S241

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74LS240, 241			54/74S240, 241			UNIT		
			Min	Typ ²	Max	Min	Typ ²	Max			
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$		0.2	0.4		0.2	0.4		V		
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = 0.5V, I_{OH} = \text{MAX}$		2.0			2.0			V		
	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OH} = -3\text{mA}$	2.4	3.4		2.4	3.4		V		
		$I_{OH} = -1\text{mA}$ 74S				2.7			V		
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	Mil					0.55	V		
			Com'l					0.55	V		
		$I_{OL} = 12\text{mA}$ 74LS				0.4			V		
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$							-1.5	V		
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$V_O = 2.4V$						50	μA		
		$V_O = 2.7V$			20				μA		
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$V_O = 0.4V$			-20				μA		
		$V_O = 0.5V$						-50	μA		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5V$						1.0	mA		
		$V_I = 7.0V$			0.1				mA		
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$				20			50	μA		
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4V$			-0.2				mA		
		$V_I = 0.5V$	$I_{a0} - I_{a3}, I_{b0} - I_{b3}$ inputs						-400	μA	
			$\overline{OE}_a, \overline{OE}_b, OE_b$ inputs						-2	mA	
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$		-40		-130	-80		-180	mA		
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH}	'LS240	Mil & Com'l		17	27			mA	
					I_{CCL}		26	44			mA
					I_{CCZ}		29	50			mA
		I_{CCH}	'LS241	Mil & Com'l		17	27			mA	
					I_{CCL}		27	46			mA
					I_{CCZ}		32	54			mA
		I_{CCH}	'S240	Mil				80	123	mA	
					Com'l				80	135	mA
				Mil				100	145	mA	
					Com'l				100	150	mA
				I_{CCL}	Mil				100	145	mA
						Com'l				100	150
		I_{CCH}	'S241	Mil				95	147	mA	
					Com'l				95	160	mA
				Mil				120	170	mA	
					Com'l				120	180	mA
I_{CCL}	Mil						120	170	mA		
				Com'l				120	180	mA	

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.
 - I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - I_{CC} is measured with outputs open.

4

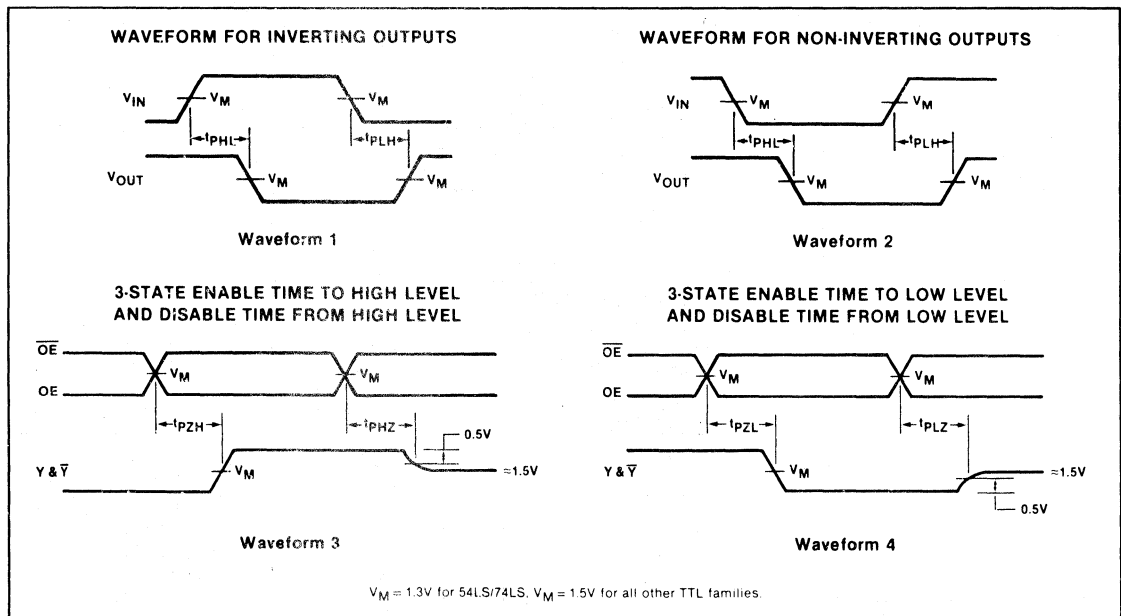
BUFFERS

54/74LS240, 54/74LS241, S240, S241

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		$C_L = 50\text{pF}$, $R_L = 90\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1, '240		14 18		7 7	ns
t_{PLH} t_{PHL} Propagation delay	Waveform 2, '241		18 18		9 9	ns
t_{pZH} Enable to HIGH	Waveform 3	LS	23			ns
		'S240			10	ns
		'S241			12	ns
t_{pZL} Enable to LOW	Waveform 4		30		15	ns
t_{PHZ} Disable from HIGH	Waveform 3, $C_L = 5\text{pF}$		18		9	ns
t_{PLZ} Disable from LOW	Waveform 4, $C_L = 5\text{pF}$		25		15	ns

AC WAVEFORMS



TRANSCEIVERS

54/74LS242, LS243

**'242 Quad Inverting Transceiver (3-State)
'243 Quad Transceiver (3-State)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS242	10ns	27mA
74LS243	12ns	28mA

FUNCTION TABLE, '242

INPUTS		INPUT/OUTPUT	
\overline{OE}_A	OE_B	A_n	B_n
L	L	INPUT	$B = \overline{A}$
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	$A = \overline{B}$	INPUT

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS242N • N74LS243N	
Ceramic DIP	N74LS242F • N74LS243F	S54LS242F • S54LS243F
Flatpack		S54LS242W • S54LS243W

FUNCTION TABLE, '243

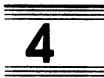
INPUTS		INPUT/OUTPUT	
\overline{OE}_A	OE_B	A_n	B_n
L	L	INPUT	$B = A$
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	$A = B$	INPUT

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

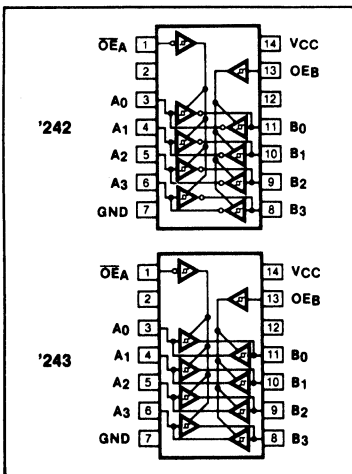
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
A, B	Outputs	30LSul

H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state
(a) = This condition is not allowed due to excessive currents.

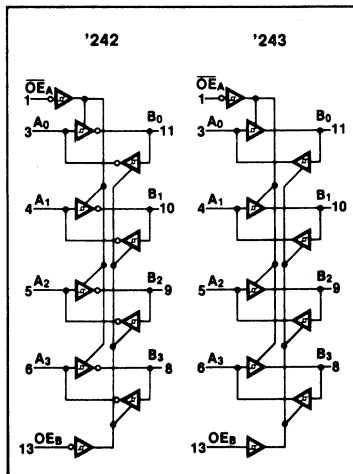
NOTE
Where a 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.



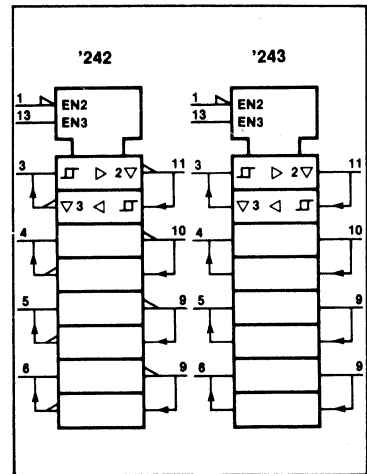
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVERS

54/74LS242, LS243

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to +7.0	- 0.5 to +7.0	V
I _{IN} Input current	- 30 to +1	- 30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to +V _{CC}	- 0.5 to +V _{CC}	V
T _A Operating free-air temperature range	- 55 to +125	0 to 70	°C

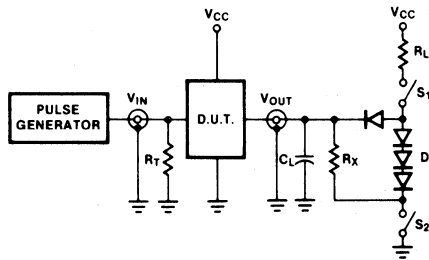
NOTE
V_{IN} limited to + 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74LS			UNIT	
	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+ 0.7	V
	Com'l			+ 0.8	V
I _{IH} Input clamp current				- 18	mA
I _{OH} HIGH-level output current	Mil			- 12	mA
	Com'l			- 15	mA
I _{OL} LOW-level output current	Mil			12	mA
	Com'l			24	mA
T _A Operating free-air temperature	Mil	- 55		+ 125	°C
	Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



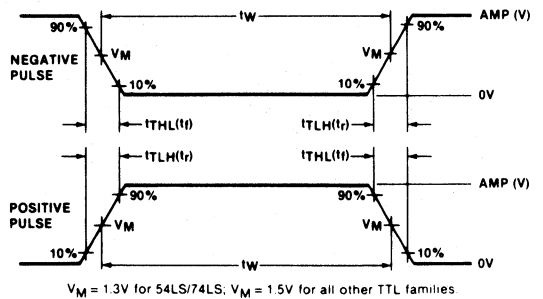
SWITCH POSITION

Test	Switch 1	Switch 2
I _{PZH}	Open	Closed
I _{PZL}	Closed	Open
I _{PHZ}	Closed	Closed
I _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVERS

54/74LS242, LS243

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74LS242 54/74LS243			UNIT	
			Min	Typ ²	Max		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$		0.2	0.4		V	
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = 0.5V, I_{OH} = \text{MAX}$		2.0			V	
	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -3\text{mA}$		2.4	3.1		V	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	Mil	0.25	0.4	V	
			Com'l	0.35	0.5	V	
		$I_{OL} = 12\text{mA}$	74LS	0.25	0.4	V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$				-1.5	V	
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_O = 2.7V$				40	μA	
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_O = 0.4V$				-200	μA	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5V$ A, B inputs			0.1	mA	
		$V_I = 7.0V$ OE_A, OE_B inputs			0.1	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$				20	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4V$	A inputs $\overline{OE}_A, OE_B = V_{IL} = \text{MAX}$			-0.2	mA	
		B inputs $\overline{OE}_A, OE_B = V_{IH} = \text{MIN}$			-0.2	mA	
		\overline{OE}_A, OE_B inputs			-0.2	mA	
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$		-40		-130	mA	
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	'242		22	38	mA
		I_{CCL} Outputs LOW			29	50	mA
		I_{CCZ} Outputs OFF			29	50	mA
		I_{CCH} Outputs HIGH	'243		22	38	mA
		I_{CCL} Outputs LOW			29	50	mA
		I_{CCZ} Outputs OFF			32	54	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with outputs open and transceivers enabled in one direction only, or with all transceivers disabled.

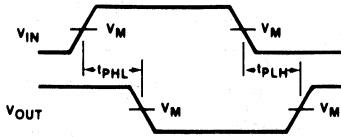
AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74LS242		54/74LS243		UNIT
		$C_L = 45\text{pF}, R_L = 667\Omega$		$C_L = 45\text{pF}, R_L = 667\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1		14 18			ns
t_{PLH} t_{PHL} Propagation delay	Waveform 2			18 18		ns
t_{PZH} Enable to HIGH	Waveform 3		23		23	ns
t_{PZL} Enable to LOW	Waveform 4		30		30	ns
t_{PHZ} Disable from HIGH	Waveform 3, $C_L = 5\text{pF}$		18		18	ns
t_{PLZ} Disable from LOW	Waveform 4, $C_L = 5\text{pF}$		25		25	ns

4

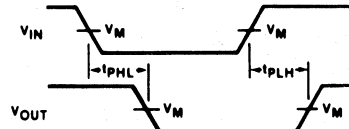
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

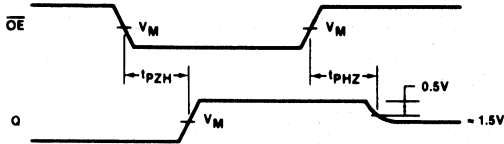
WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 2

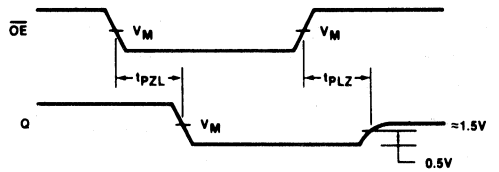
$V_M = 1.3V$ for 54LS/74LS, $V_M = 1.5V$ for all other TTL families.

3-STATE ENABLE TIME TO HIGH LEVEL AND
DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND
DISABLE TIME FROM LOW LEVEL



Waveform 4

BUFFERS

54/74LS244, S244

Octal Buffers (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS244	12ns	25mA
74S244	6ns	112mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS244N • N74S244N	
Plastic SO	74LS244D	
Ceramic DIP		S54LS244F • S54S244F
LLCC		S54LS244G

FUNCTION TABLE

INPUTS				OUTPUTS	
\overline{OE}_a	I_a	\overline{OE}_b	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

H = HIGH voltage level

L = LOW voltage level

X = Don't care

(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

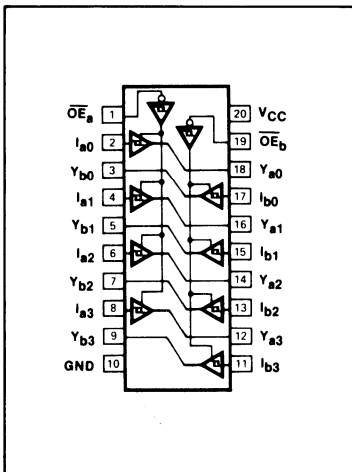
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	24Sul	30LSul

NOTE

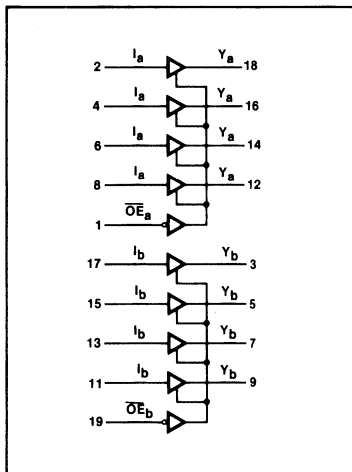
A 54/74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and a 54/74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .



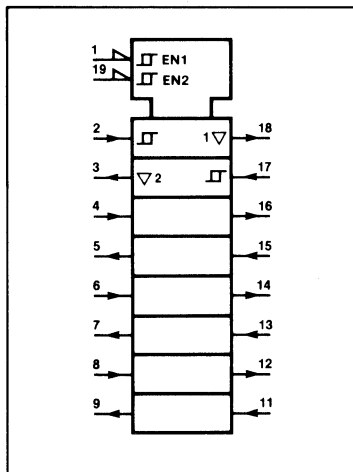
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUFFERS

54/74LS244, S244

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

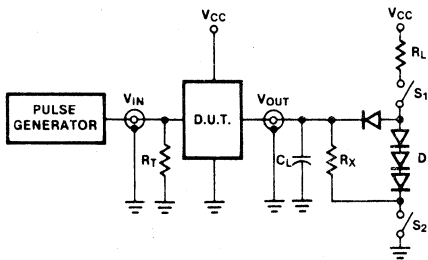
PARAMETER		54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V	
V _{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I _{IK}	Input clamp current			-18			-18	mA	
I _{OH}	HIGH-level output current	Mil			-12			-12	mA
		Com'l			-15			-15	mA
I _{OL}	LOW-level output current	Mil			12			48	mA
		Com'l			24			64	mA
T _A	Operating free-air temperature	Mil	-55		+125	-55		+125	°C
		Com'l	0		70	0		70	°C

NOTE

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



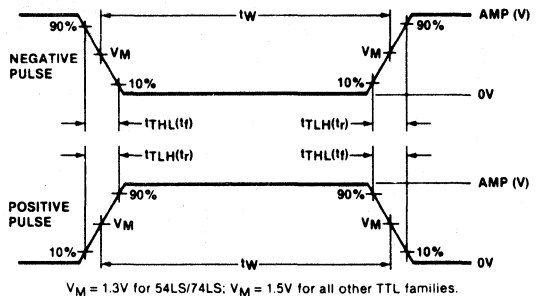
SWITCH POSITION

Test	Switch 1	Switch 2
¹ PZH	Open	Closed
¹ PZL	Closed	Open
¹ PHZ	Closed	Closed
¹ PLZ	Closed	Closed

DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7.5ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS

54/74LS244, S244

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS244			54/74S244			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$	0.2	0.4		0.2	0.4		V		
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = 0.5V, I_{OH} = \text{MAX}$	2.0			2.0			V		
	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -3\text{mA}$	2.4	3.4		2.4			V		
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	Mil			0.4		0.55	V	
			Com'l			0.5		0.55	V	
		$I_{OL} = 12\text{mA}$	74LS			0.4			V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$					-1.5		-1.2	V	
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$V_O = 2.7V$					20		μA	
		$V_O = 2.4V$						50	μA	
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$V_O = 0.4V$					-20		μA	
		$V_O = 0.5V$						-50	μA	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5V$						1.0	mA	
		$V_I = 7.0V$					0.1		mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$						20		μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4V$					-0.2		mA	
		$V_I = 0.5V$	$\overline{\text{OE}}$ inputs						-2.0	mA
			Other inputs						-0.4	mA
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$	-40		-130	-80			-180	mA	
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH	Mil	17	27	95	147	mA		
			Com'l	17	27	95	160	mA		
		I_{CCL} Outputs LOW	Mil	27	46	120	170	mA		
			Com'l	27	46	120	180	mA		
		I_{CCZ} Outputs OFF	Mil	32	54	120	170	mA		
			Com'l	32	54	120	180	mA		

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.
 - I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC\text{ MAX}} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - I_{CC} is measured with outputs open.

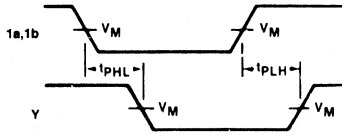
AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		$C_L = 45\text{pF}, R_L = 667\Omega$		$C_L = 50\text{pF}, R_L = 90\Omega$		
		Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		18		9	ns
t_{PHL} Propagation delay	Waveform 1		18		9	ns
t_{PZH} Enable to HIGH	Waveform 2		23		12	ns
t_{PZL} Enable to LOW	Waveform 3		30		15	ns
t_{PHZ} Disable from HIGH	Waveform 2, $C_L = 5\text{pF}$		18		9	ns
t_{PLZ} Disable from LOW	Waveform 3, $C_L = 5\text{pF}$		25		15	ns



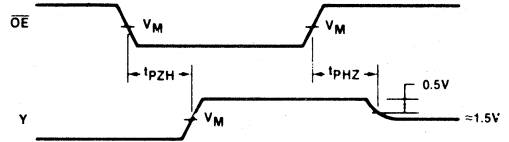
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



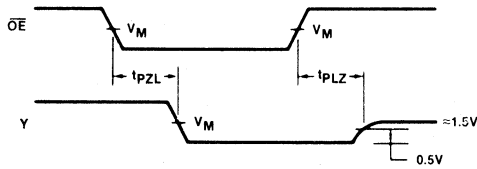
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

$V_M = 1.3V$ for 54LS/74LS. $V_M = 1.5V$ for all other TTL families.

TRANSCIEVER

54/74LS245

Octal Transceiver (3-State)

- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS245	8ns	58mA

DESCRIPTION

The 'LS245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS245N	
Plastic SO	N74LS245D	
Ceramic DIP		S54LS245F
LLCC		S54LS245G

4

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/R	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

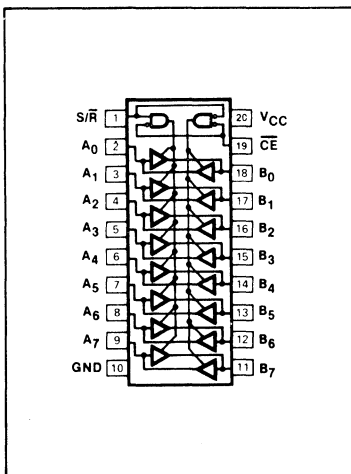
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance "off" state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

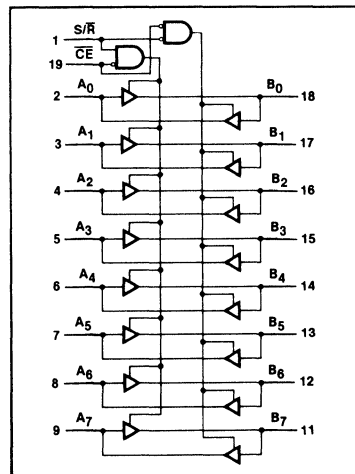
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSuI
All	Outputs	30LSuI

NOTE
 A 54/74LS unit load (LSuI) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

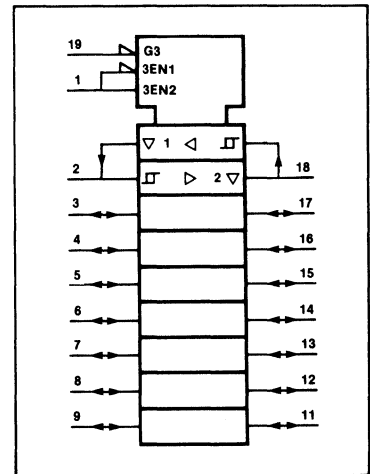
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVER

54/74LS245

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

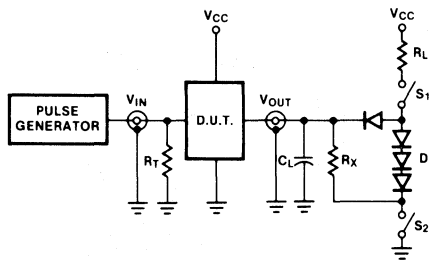
NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74LS			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.5	V
	Com'l	4.75	5.0	5.25
V _{IH} HIGH-level input voltage		2.0		V
V _{IL} LOW-level input voltage	Mil		+0.7	V
	Com'l		+0.8	V
I _{IK} Input clamp current			-18	mA
I _{OH} HIGH-level output current	Mil		-12	mA
	Com'l		-15	mA
I _{OL} LOW-level output current	Mil		12	mA
	Com'l		24	mA
T _A Operating free-air temperature	Mil	-55	+125	°C
	Com'l	0	70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



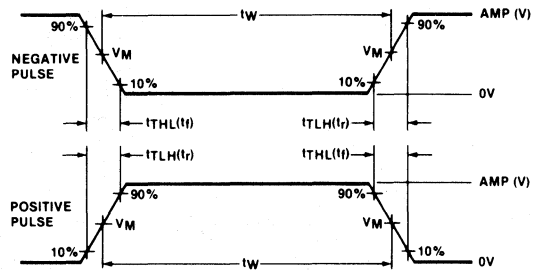
SWITCH POSITION

Test	Switch 1	Switch 2
I _{PZH}	Open	Closed
I _{PZL}	Closed	Open
I _{PHZ}	Closed	Closed
I _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S. R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

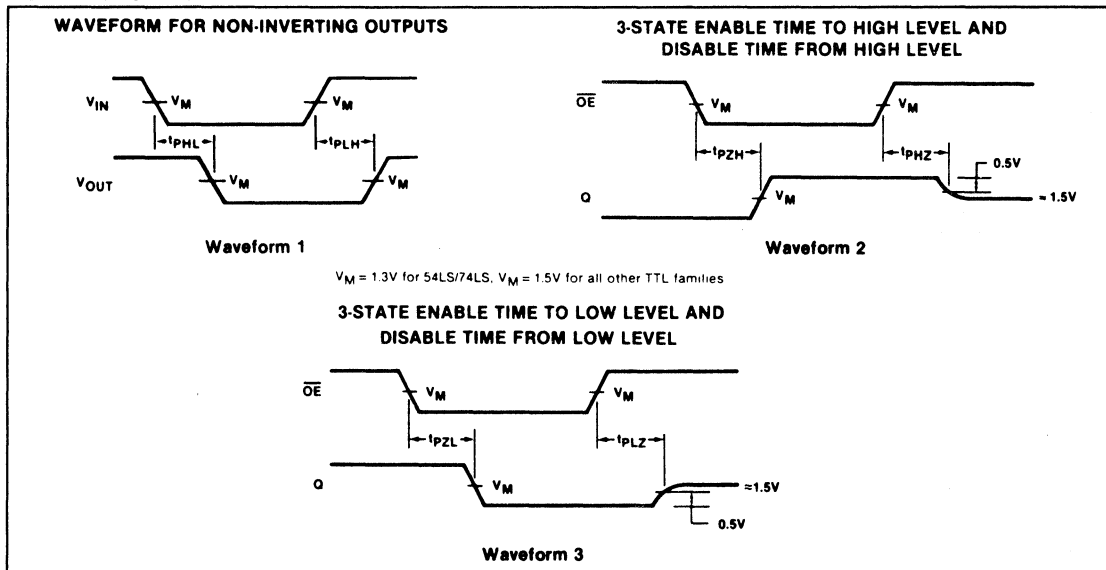
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS245			UNIT	
		Min	Typ ²	Max		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$	0.2	0.4		V	
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OH} = \text{MAX}$	2.0		V	
		$I_{OH} = -3\text{mA}$	2.4	3.4	V	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	Mil		0.4	V
			Com'l		0.5	V
		$I_{OL} = 12\text{mA}$	74LS		0.4	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V	
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.7\text{V}, \overline{CE} = 2.0\text{V}$			20	μA	
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_O = 0.4\text{V}, \overline{CE} = 2.0\text{V}$			-200	μA	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$	A, B inputs		0.1	mA
		$V_I = 7.0\text{V}$	S/ \overline{R} , \overline{CE} inputs		0.1	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-0.2	mA	
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$			-40	-130	mA
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		48	70	mA
		I_{CCL} Outputs LOW		62	90	mA
		I_{CCZ} Outputs OFF		64	95	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
 - I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with outputs open.

AC WAVEFORMS



TRANSCEIVER

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	
t_{PLH} Propagation delay	Waveform 1		12	ns
t_{PHL} Propagation delay	Waveform 1		12	ns
t_{PZH} Enable to HIGH	Waveform 2		40	ns
t_{PZL} Enable to LOW	Waveform 3		40	ns
t_{PHZ} Disable from HIGH	Waveform 2, $C_L = 5\text{pF}$		25	ns
t_{PLZ} Disable from LOW	Waveform 3, $C_L = 5\text{pF}$		25	ns

MULTIPLEXERS

54/74LS251A, S251

8-Input Multiplexer (3-State)

- High speed 8-to-1 multiplexing
- True and complement outputs
- Both outputs are 3-State for further multiplexer expansion
- 3-State outputs are buffer type with 12mA/24mA outputs for Military/ Commercial applications

TYPE	TYPICAL PROPAGATION DELAY (Data to Y)	TYPICAL SUPPLY CURRENT (Total)
74LS251A	18ns	9mA
74S251	8ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S251N • N74LS251AN	
Ceramic DIP		S54S251F • S54LS251AF
Flatpack		S54S251W • S54LS251AW
LLCC		S54LS251G

DESCRIPTION

The '251 is a logical implementation of a single-pole, 8-position switch with the state of three Select inputs (S_0, S_1, S_2) controlling the switch position. Assertion (Y) and Negation (\bar{Y}) outputs are both provided. The Output Enable input (OE) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \overline{OE} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

Both outputs are in the HIGH impedance (HIGH Z) state when the output enable is HIGH, allowing multiplexer expansion by tying the outputs of up to 128 devices

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

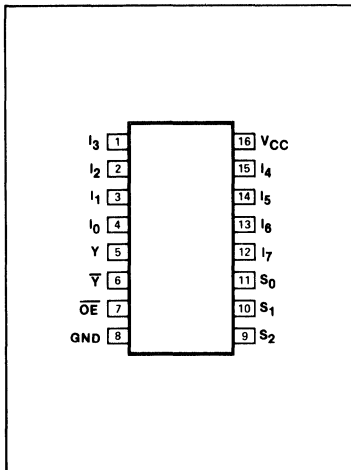
NOTE

A 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0 mA I_{IL} and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4 mA I_{IL} .

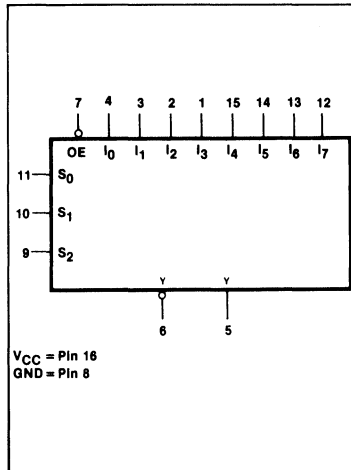
together. All but one device must be in the HIGH impedance state to avoid high currents that would exceed the maximum ratings, when the outputs of the 3-State

devices are tied together. Design of the output enable signals must ensure there is no overlap in the active LOW portion of the enable voltages.

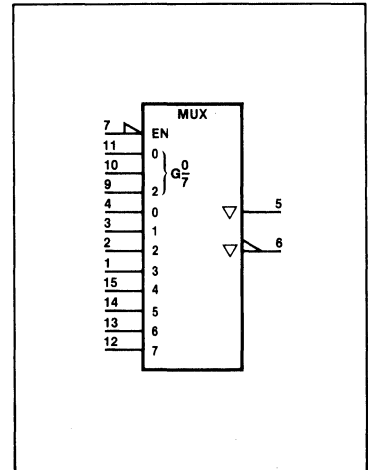
PIN CONFIGURATION



LOGIC SYMBOL



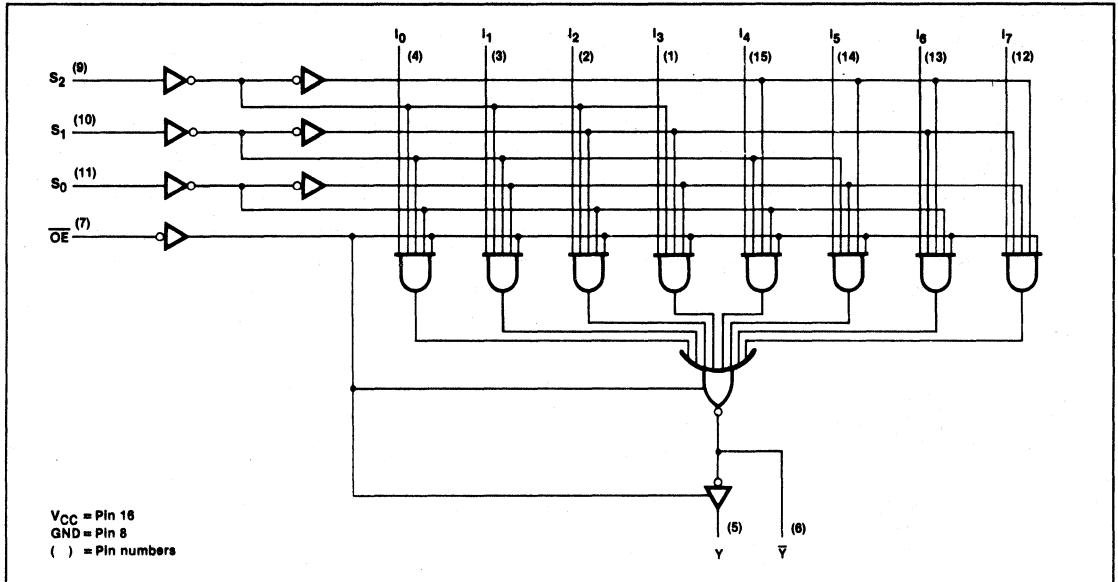
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXERS

54/74LS251A, S251

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS													OUTPUTS	
OE	S ₂	S ₁	S ₀	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	Y-bar	Y	
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)	
L	L	L	L	L	X	X	X	X	X	X	X	H	L	
L	L	L	L	H	X	X	X	X	X	X	X	L	H	
L	L	L	H	H	X	X	X	X	X	X	X	L	H	
L	L	H	L	X	X	L	X	X	X	X	X	H	L	
L	L	H	H	X	X	H	X	X	X	X	X	L	H	
L	L	H	H	X	X	X	L	X	X	X	X	H	L	
L	L	H	H	X	X	X	H	X	X	X	X	L	H	
L	H	L	L	X	X	X	X	L	X	X	X	H	L	
L	H	L	H	X	X	X	X	X	L	X	X	L	H	
L	H	H	L	X	X	X	X	X	H	X	X	H	L	
L	H	H	H	X	X	X	X	X	X	X	X	L	H	
L	H	H	L	X	X	X	X	X	X	H	X	L	H	
L	H	H	H	X	X	X	X	X	X	X	L	H	L	
L	H	H	H	X	X	X	X	X	X	X	H	L	H	

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance (off) state

MULTIPLEXERS

54/74LS251A, S251

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output for HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

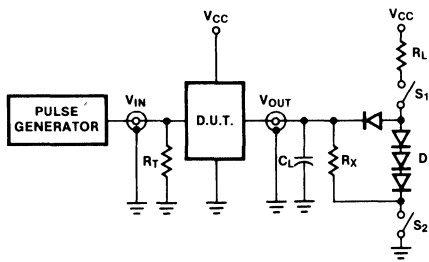
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-18			-18	mA
I _{OH} HIGH-level output current	Mil			-1.0			-2.0	mA
	Com'l			-2.6			-6.5	mA
I _{OL} LOW-level output current	Mil			12			20	mA
	Com'l			24			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



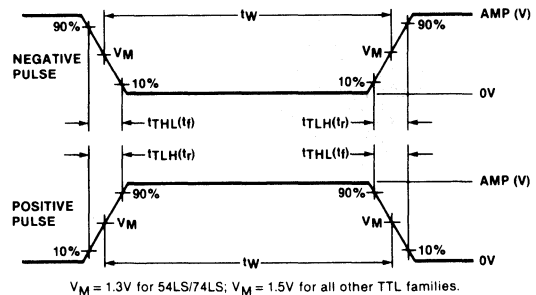
SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

4

MULTIPLEXERS

54/74LS251A, S251

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS251A			54/74S251			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5			2.4	3.4	V	
		Com'l	2.7			2.4	3.2	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4			0.5 ⁵	V
			Com'l	0.35	0.5			0.5	V
		I _{OL} = 12mA	74LS	0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.2	V
I _{ozH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.4V						50	μA
		V _O = 2.7V				20			μA
I _{ozL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V				-20			μA
		V _O = 0.5V						-50	μA
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						1.0	mA
		V _I = 7.0V				0.1			mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V				20		50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V				-0.4			mA
		V _I = 0.5V						-2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX			-30		-130	-40		mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Outputs "on"				12			mA
		Outputs "off"				15		85	mA

NOTES

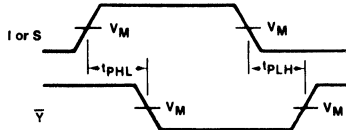
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} on the 54/74S251 with all inputs at 4.5V and all outputs open. Measure I_{CC} on the 54/74LS251A in the following manner: 1. Outputs "on": Data and select inputs at 4.5V, output enable grounded and all outputs open. 2. Outputs "off": Data and select inputs at 4.5V, output enable at 4.5V and all outputs open.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		C _L = 45pF, R _L = 667Ω		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay Select to Y output	Waveform 2		35 40		18 19.5	ns
t _{PLH} t _{PHL} Propagation delay Select to \bar{Y} output	Waveform 1		28 33		15 13.5	ns
t _{PLH} t _{PHL} Propagation delay Data to Y output	Waveform 2		28 28		12 12	ns
t _{PLH} t _{PHL} Propagation delay Data to \bar{Y} output	Waveform 1		15 15		7.0 7.0	ns
t _{PZH} Output enable to HIGH level	Waveform 3 C _L = 50pF for 'S251		25		19.5	ns
t _{PZL} Output enable to LOW level	Waveform 4 C _L = 50pF for 'S251		25		21	ns
t _{PHZ} Output disable from HIGH level	Waveform 3, C _L = 5pF		30		8.5	ns
t _{PLZ} Output disable from LOW level	Waveform 4, C _L = 5pF		20		14	ns

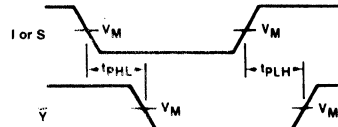
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



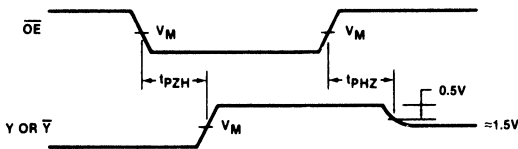
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



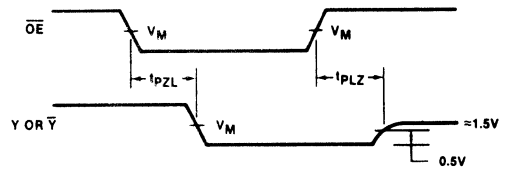
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

MULTIPLEXERS

54/74LS253, S253

Dual 4-Input Multiplexer (3-State)

- 3-State outputs for bus interface and multiplex expansion
- Common Select inputs
- Separate Output Enable inputs

TYPE	TYPICAL PROPAGATION DELAY (From Data)	TYPICAL SUPPLY CURRENT (Total)
74LS253	15ns	8mA
74S253	8ns	48mA

DESCRIPTION

The '253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{OE}_a, \overline{OE}_b$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

The '253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$Y_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S253N • N74LS253N	
Plastic SO	N74LS253D • N74S253D	
Ceramic DIP		S54S253F • S54LS253F
Flatpack		S54S253W • S54LS253W

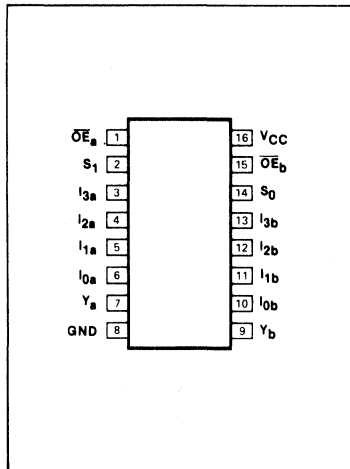
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

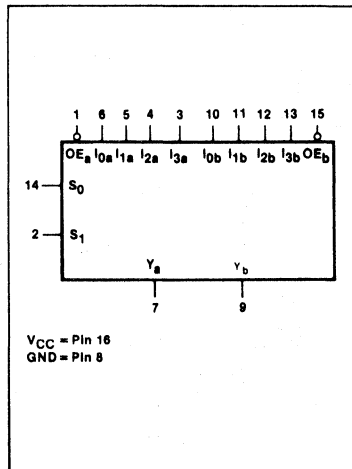
NOTE

A 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} , and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

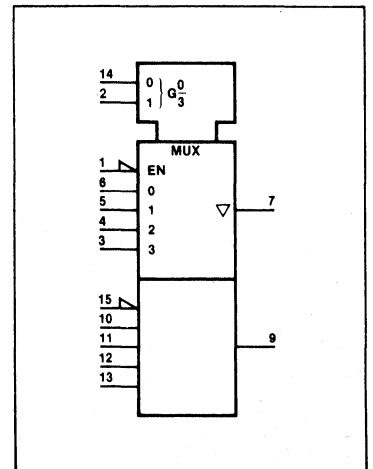
PIN CONFIGURATION



LOGIC SYMBOL



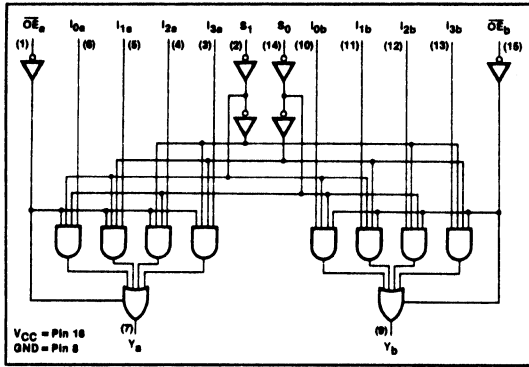
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXERS

54/74LS253, S253

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S ₀	S ₁	I ₀	I ₁	I ₂	I ₃	OE	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	L	X	L	X	X	L	L
L	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-18			-18	mA
I _{OH} HIGH-level output current	Mil			-1.0			-2.0	mA
	Com'l			-2.6			-6.5	mA
I _{OL} LOW-level output current	Mil			4			20	mA
	Com'l			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

MULTIPLEXERS

54/74LS253, S253

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS253			54/74S253			UNIT	
		Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V	
		Com'l	2.4	3.1		2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4			0.5 ⁵	V
			Com'l	0.35	0.5			0.5	V
		I _{OL} = 4mA	74LS	0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5		-1.2	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.7V			20			μA	
		V _O = 2.4V					50	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V			-20			μA	
		V _O = 0.5V					-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA	
		V _I = 7.0V			0.1			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V			20		50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-0.4			mA	
		V _I = 0.5V					-2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-15		-100	-40	-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		7	12		70	mA	
		Condition 2		8.5	14			mA	

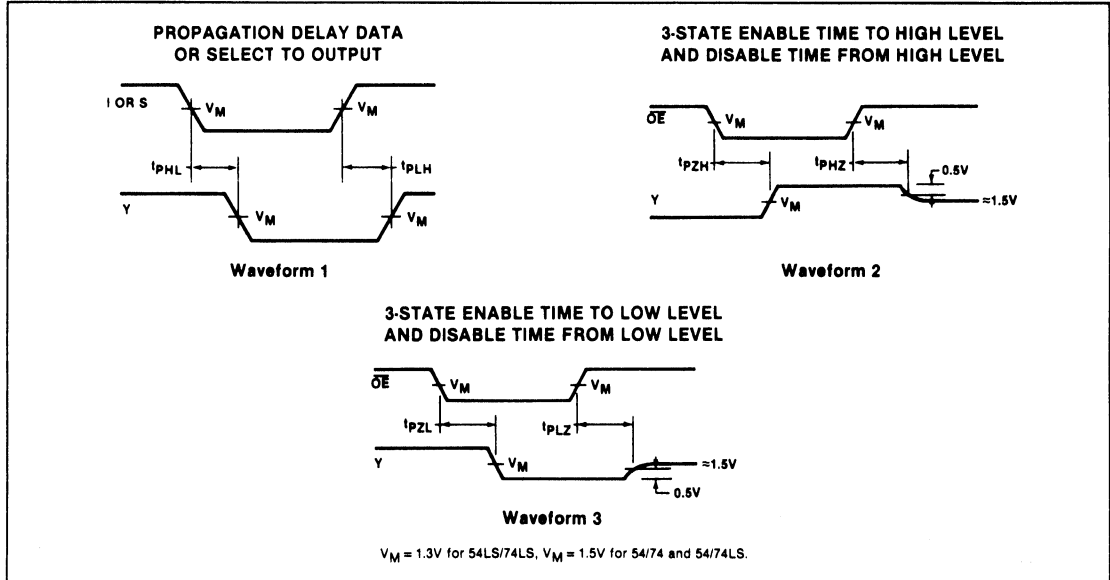
NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_OUT = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured under the following conditions with the outputs open: *Condition 1*: All inputs grounded. *Condition 2*: \overline{OE} at 4.5V, all inputs grounded.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

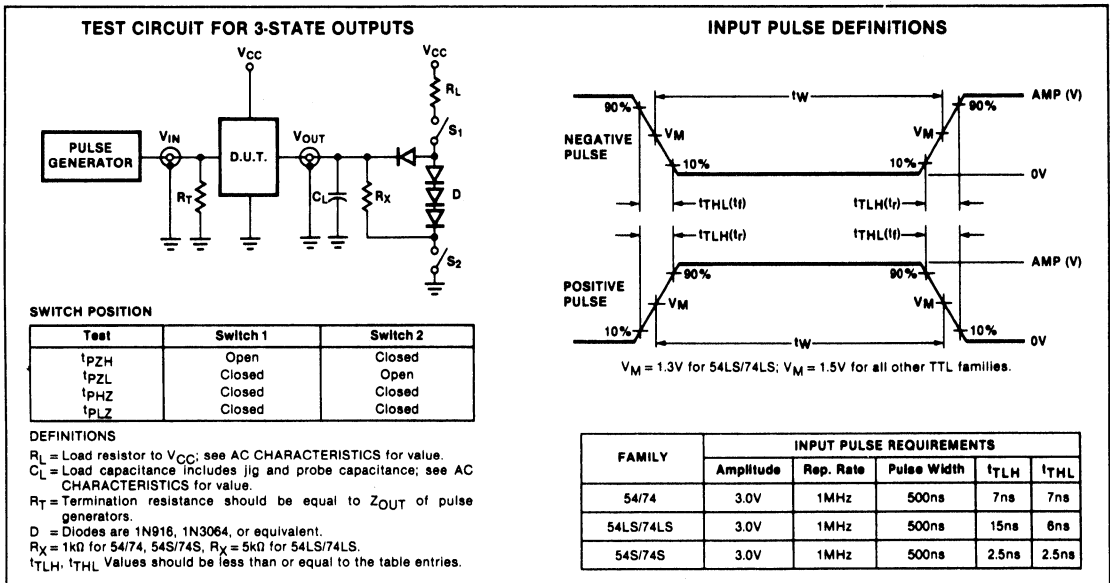
PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Data to output	Waveform 1		25 20		9.0 9.0	ns
t _{PLH} Propagation delay t _{PHL} Select to output	Waveform 1		45 32		18 18	ns
t _{PZH} Output enable to HIGH level	Waveform 2		28		13	ns
t _{PZL} Output enable to LOW level	Waveform 3		23		14	ns
t _{PHZ} Output disable from HIGH level	Waveform 2, C _L = 5pF		41		8.5	ns
t _{PLZ} Output disable from LOW level	Waveform 3, C _L = 5pF		27		14	ns

AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS



LATCH

54/74LS256

Dual 4-Bit Addressable Latch

- Combines dual demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as dual 1-of-4 active HIGH decoder

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS256	19ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS256N	
Plastic SO	N74LS256D	
Ceramic DIP		S54LS256F
Flatpack		S54LS256W

DESCRIPTION

The '256 dual addressable latch has four distinct modes of operation and are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

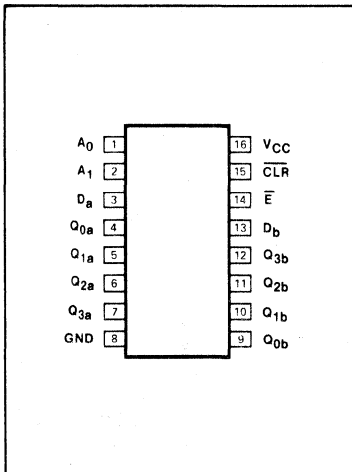
PINS	DESCRIPTION	54/74LS
\bar{E}	Input	2LSul
Other	Inputs	1LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

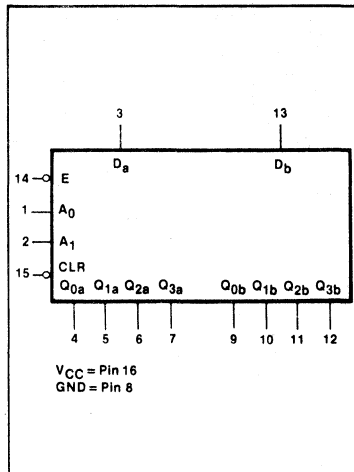
held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode (CLR = \bar{E} = LOW), addressed outputs will follow

the level of the D inputs, with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

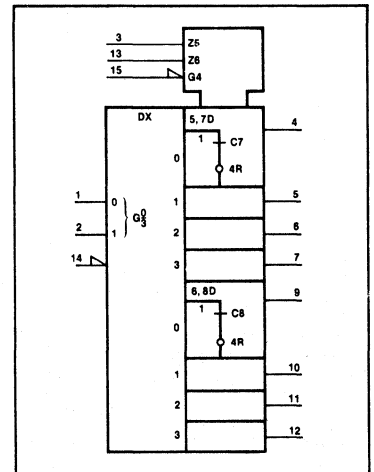
PIN CONFIGURATION



LOGIC SYMBOL



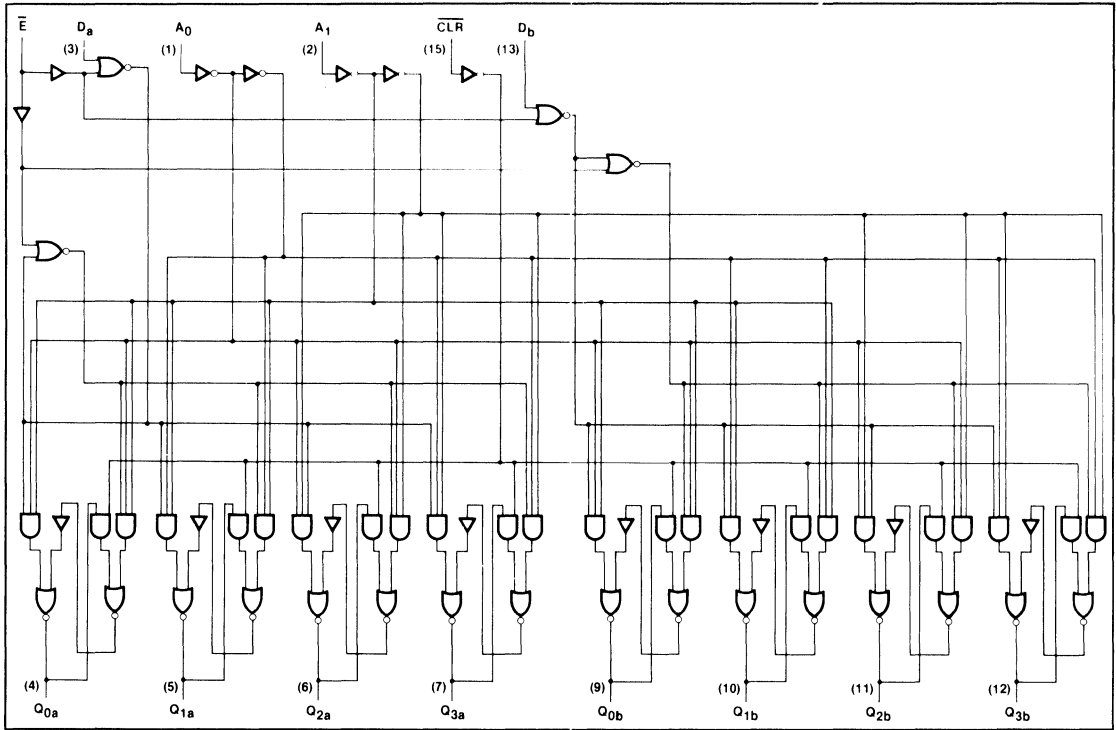
LOGIC SYMBOL (IEEE/IEC)



LATCH

54/74LS256

LOGIC DIAGRAM



4

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	CLR	E	D	A ₀	A ₁	Q ₀	Q ₁	Q ₂	Q ₃
Clear	L	H	X	X	X	L	L	L	L
Demultiplex (active HIGH decoder when D = H)	L	L	d	L	L	Q = d	L	L	L
	L	L	d	L	H	L	Q = d	L	L
	L	L	d	H	H	L	L	Q = d	L
Store (do nothing)	H	H	X	X	X	q ₀	q ₁	q ₂	q ₃
Addressable latch	H	L	d	L	L	Q = d	q ₁	q ₂	q ₃
	H	L	d	H	L	q ₀	Q = d	q ₂	q ₃
	H	L	d	L	H	q ₀	q ₁	Q = d	q ₃
	H	L	d	H	H	q ₀	q ₁	q ₂	Q = d

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 X = Don't care.
 d = HIGH or LOW data one setup time prior to the LOW-to-HIGH Enable transition.
 q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	-30 to +1	mA
V _{OUT} Voltage applied to output for HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current				- 400	μA
I _{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹		54/74LS256			UNIT
				Min	Typ ²	Max	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5			V
			Com'l	2.7			V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.4	V
				Com'l		0.5	V
			I _{OL} = 4mA	74LS		0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				- 1.5	V
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				0.1	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	\bar{E} input			40	μA
			Other inputs			20	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V	\bar{E} input			- 0.8	mA
			Other inputs			- 0.4	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		- 15		- 100	mA
I _{CC}	Supply current (total)	V _{CC} = MAX			22	36	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. All typical values are at V_{CC} = 5V, T_A = 25°C.

3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS		54LS/74LS		UNIT
				C _L = 15pF, R _L = 2kΩ		
				Min	Max	
t _{PLH}	Propagation delay	Waveform 1		35	ns	
t _{PHL}	Enable to output			24		
t _{PLH}	Propagation delay	Waveform 2		32	ns	
t _{PHL}	Data to output			21		
t _{PLH}	Propagation delay	Waveform 3		38	ns	
t _{PHL}	Address to output			29		
t _{PHL}	Propagation delay, Clear to output	Waveform 4		27	ns	

LATCH

54/74LS256

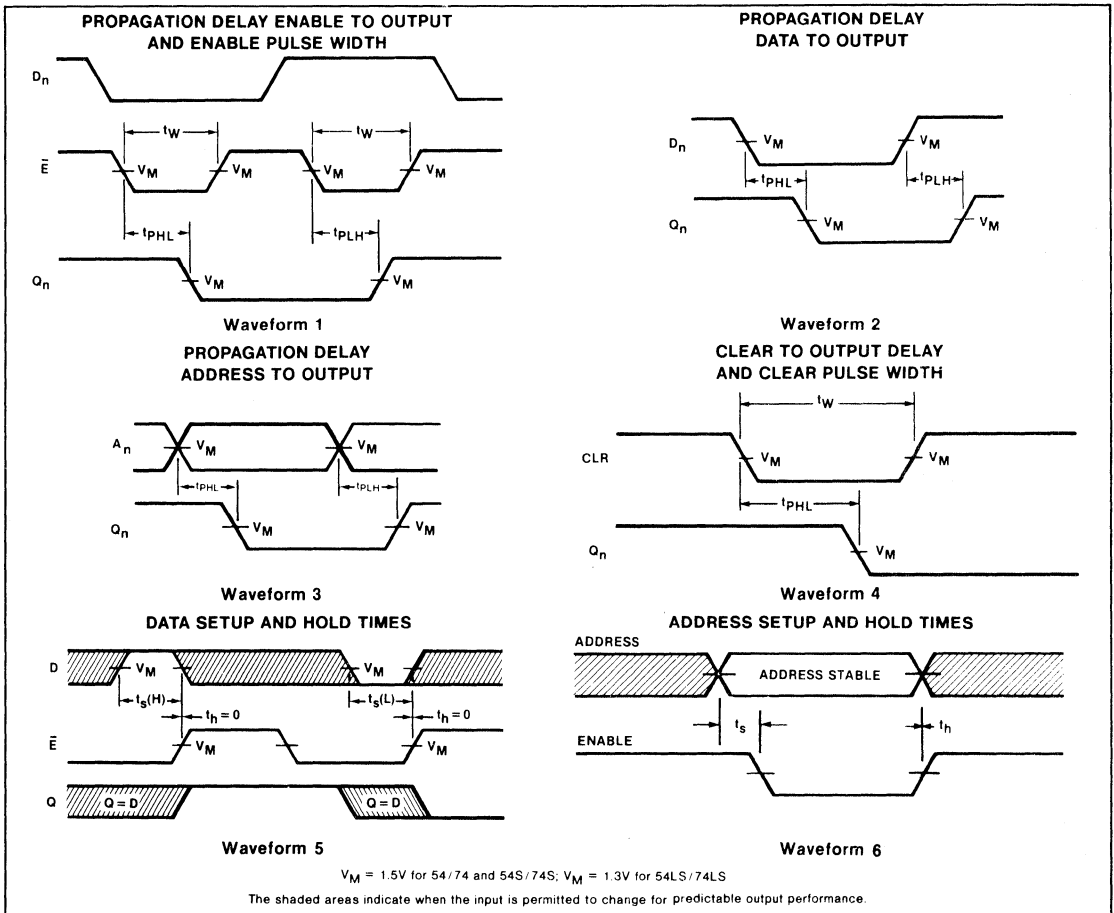
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_W Enable pulse width	Waveform 1	15		ns
t_W Clear pulse width	Waveform 4	15		ns
$t_s(H)$ Setup time HIGH, Data to Enable	Waveform 5	15		ns
$t_h(H)$ Hold time HIGH, Data to Enable	Waveform 5	0		ns
$t_s(L)$ Setup time LOW, Data to Enable	Waveform 5	15		ns
$t_h(L)$ Hold time LOW, Data to Enable	Waveform 5	0		ns
t_s Setup time, Address to Enable ^(a)	Waveform 6	15		ns
t_h Hold time, Address to Enable ^(b)	Waveform 6	0		ns

NOTES

- a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC WAVEFORMS



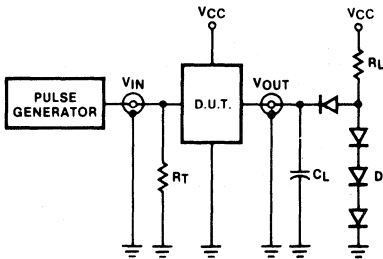
4

LATCH

54/74LS256

TEST CIRCUITS AND WAVEFORMS

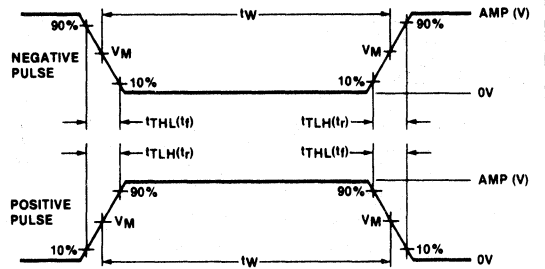
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DATA SELECTORS/MULTIPLEXERS

54/74LS257A, S257

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)

- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS257A	13ns	9mA
74S257	6.6ns	56mA

DESCRIPTION

The '257 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The '257 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input (\overline{OE}) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S257N • N74LS257AN	
Plastic SO	N74LS257AD • N74S257D	
Ceramic DIP		S54S257F • S54LS257AF
Flatpack		S54S257W • S54LS257AW
LLCC		S54LS257AG

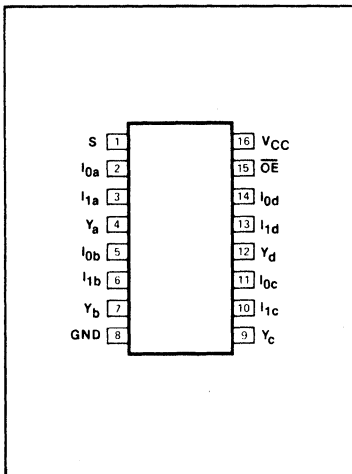
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
S	Input	2Sul	2LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

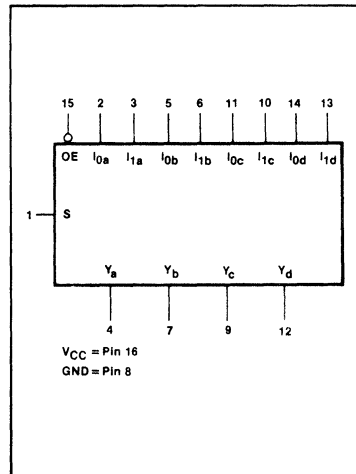
NOTE
Where a 54/74S unit load (Sul) is 50 μ A I_{IH} and $-2.0mA$ I_{IL} , and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and $-0.4mA$ I_{IL} .

4

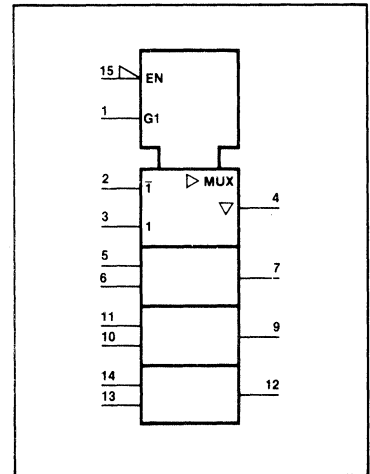
PIN CONFIGURATION



LOGIC SYMBOL



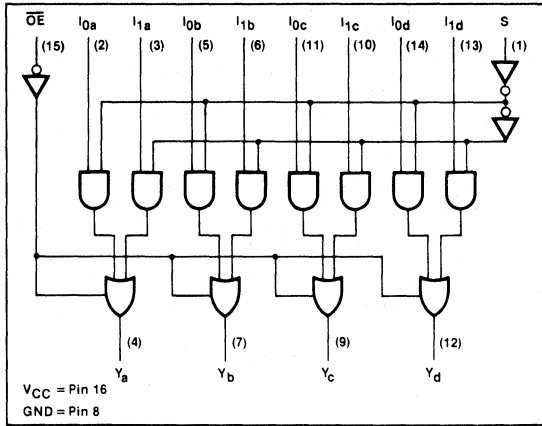
LOGIC SYMBOL (IEEE/IEC)



DATA SELECTORS/MULTIPLEXERS

54/74LS257A, S257

LOGIC DIAGRAM



FUNCTION TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
OE	S	I ₀	I ₁	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	L	L	L
L	L	H	X	H
L	L	H	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-18			-18	mA
I _{OH} HIGH-level output current	Mil			-1.0			-2.0	mA
	Com'l			-2.6			-6.5	mA
I _{OL} LOW-level output current	Mil			12			20	mA
	Com'l			24			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DATA SELECTORS/MULTIPLEXERS

54/74LS257A, S257

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹			54/74LS257A			54/74S257			UNIT	
				Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OH} = MAX	Mil	2.4	3.4		2.4	3.4		V	
			Com'l	2.4	3.1		2.4	3.2		V	
		I _{OH} = -1mA	74S				2.7			V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.25	0.4			0.5 ⁵	V	
			Com'l		0.35	0.5			0.5	V	
		I _{OL} = 12mA	74LS		0.25	0.4				V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.5			-1.2	V	
I _{ozH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.7V				20				μA	
		V _O = 2.4V							50	μA	
I _{ozL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V				-20				μA	
		V _O = 0.5V							-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V								1.0	mA
		V _I = 7.0V	S input				0.2				mA
			Other inputs				0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	S input				40			100	μA
			Other inputs				20			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	S input				-0.8				mA
			Other inputs				-0.4				mA
		V _I = 0.5V	S input							-4	mA
			Other inputs							-2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX			-30		-130	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH			6.2	10		44	68	mA	
		I _{CCL} Outputs LOW			10	16		60	93	mA	
		I _{CCZ} Outputs OFF			12	19		64	99	mA	

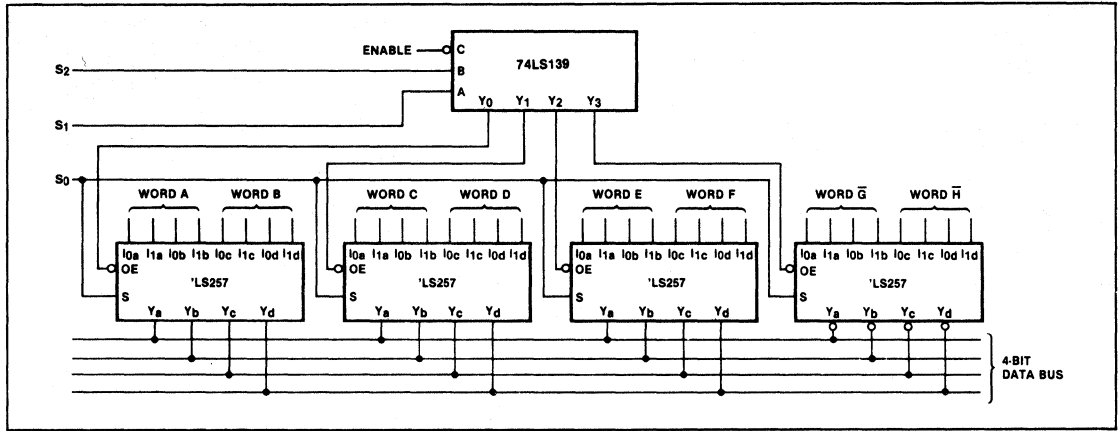
- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_O = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.
 - V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25 °C, V_{CC} = 5.0V

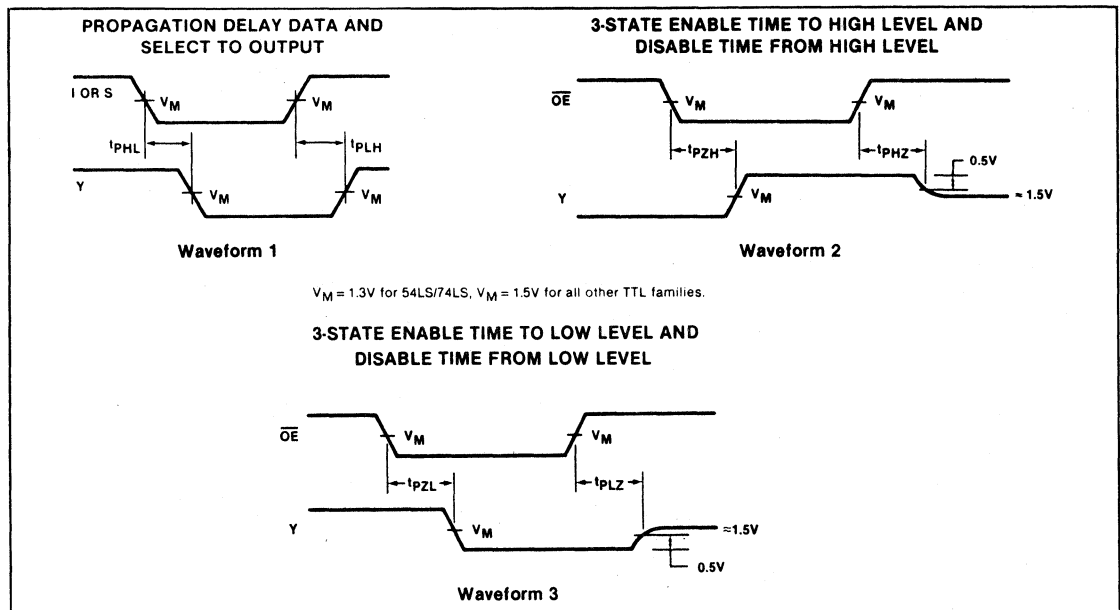
PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		C _L = 45pF, R _L = 667Ω		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Data to output	Waveform 1		18		7.5	ns
			18		7.5	
t _{PLH} Propagation delay t _{PHL} Select to output	Waveform 1		21		15	ns
			21		15	
t _{PZH} Output enable to HIGH level	Waveform 2		30		19.5	ns
t _{PZL} Output enable to LOW level	Waveform 3		30		21	ns
t _{PHZ} Output disable from HIGH level	Waveform 2, C _L = 5pF		30		8.5	ns
t _{PLZ} Output disable from LOW level	Waveform 3, C _L = 5pF		25		14	ns

4

APPLICATION

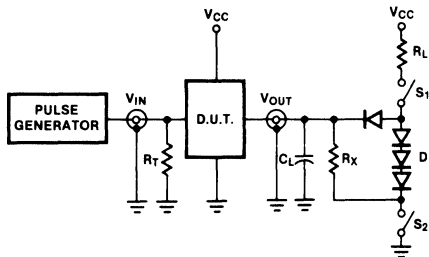


AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



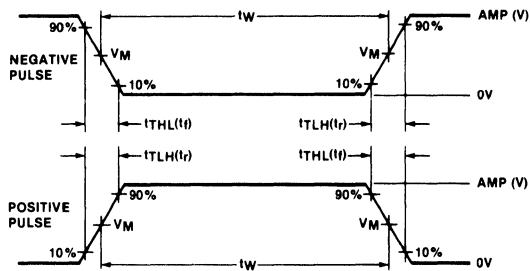
SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns



DATA SELECTORS/MULTIPLEXERS

54/74LS258A, S258

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)

- Multifunction capability
- Inverting data path
- 3-State outputs
- See '257 for non-inverting version

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS258A	13ns	9mA
74S258	6ns	48mA

DESCRIPTION

The '258 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in inverted (complementary) form.

The '258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input (\overline{OE}) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs of the 3-state devices are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S258N • N74LS258AN	
Plastic SO	N74LS258AD	
Ceramic DIP		S54S258F • S54LS258AF
Flatpack		S54S258W • S54LS258AW

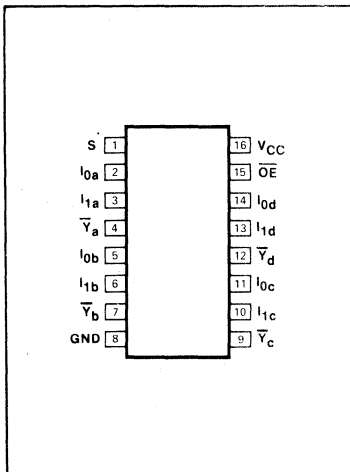
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
S	Input	2Sul	2LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

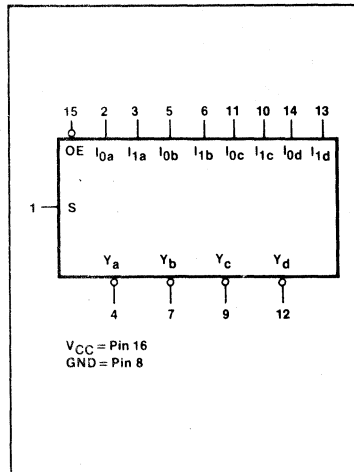
NOTE

Where a 54/74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and a 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

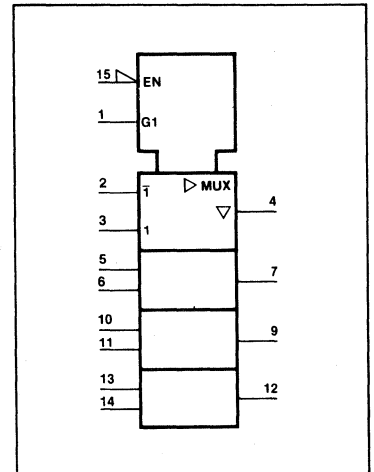
PIN CONFIGURATION



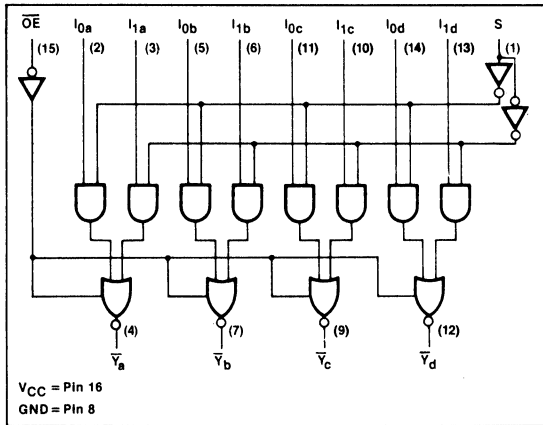
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
		I_0	I_1	
\overline{OE}	S	I_0	I_1	\overline{Y}
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	L	L	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-18			-18	mA
I_{OH} HIGH-level output current	Mil			-1.0			-2.0	mA
	Com'l			-2.6			-6.5	mA
I_{OL} LOW-level output current	Mil			12			20	mA
	Com'l			24			20	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DATA SELECTORS/MULTIPLEXERS

54/74LS258A, S258

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74LS258A			54/74S258			UNIT		
			Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OH} = MAX	Mil	2.4	3.4		2.4	3.4	V		
			Com'l	2.4	3.1		2.4	3.2	V		
		I _{OH} = -1mA	74S				2.7		V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.25	0.4			0.5 ⁵ V		
			Com'l		0.35	0.5			0.5 V		
		I _{OL} = 12mA	74LS		0.25	0.4			V		
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}							-1.5	-1.2	V	
I _{ozH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.7V							20	μA	
		V _O = 2.4V								50	μA
I _{ozL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V							-20	μA	
		V _O = 0.5V								-50	μA
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V								1.0	mA
		V _I = 7.0V	S input							0.2	mA
			Other inputs							0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V	S input						40	100	μA
			Other inputs						20	50	μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V	S input						-0.8	mA	
			Other inputs						-0.4	mA	
		V _I = 0.5V	S input							-4	mA
			Other inputs							-2	mA
I _{os} Short-circuit output current ³	V _{CC} = MAX			-30		-130	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH			4	7		36	56	mA	
		I _{CCL} Outputs LOW			8.8	14		52	81	mA	
		I _{CCZ} Outputs OFF			12	19		56	87	mA	

NOTES

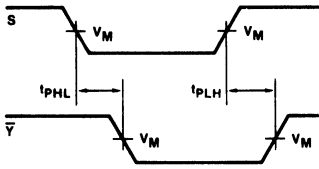
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OJT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		C _L = 45pF, R _L = 667Ω		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} Propagation delay	Waveform 4	18		6.0		ns
t _{PHL} Data to output		18		6.0		
t _{PLH} Propagation delay	Waveforms 1 & 4	21		12		ns
t _{PHL} Select to output		21		12		
t _{pZH} Output enable to HIGH level	Waveform 2	30		19.5		ns
t _{pZL} Output enable to LOW level	Waveform 3	30		21		ns
t _{PHZ} Output disable from HIGH level	Waveform 2, C _L = 5pF	30		8.5		ns
t _{PLZ} Output disable from LOW level	Waveform 3, C _L = 5pF	25		14		ns

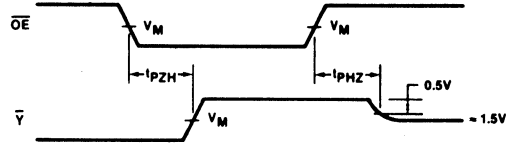
AC WAVEFORMS

PROPAGATION DELAY SELECT OUTPUT



Waveform 1

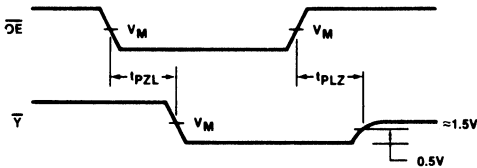
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

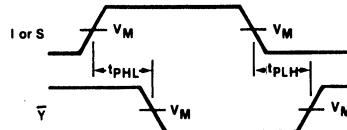
$V_M = 1.3V$ for 54LS/74LS. $V_M = 1.5V$ for all other TTL families

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

PROPAGATION DELAY DATA AND SELECT OUTPUT

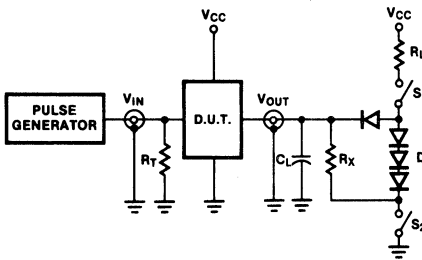


Waveform 4

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



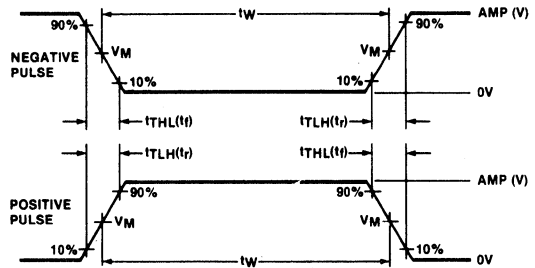
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 $R_X = 1k\Omega$ for 54/74, 54S/74S, $R_X = 5k\Omega$ for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH

54/74LS259

8-Bit Addressable Latch

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as a 1-of-8 active HIGH decoder

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS259	19ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{cc} = 5V ± 5%; T _A = 0°C to + 70°C	MILITARY RANGES V _{cc} = 5V ± 10%; T _A = -55°C to + 125°C
Plastic DIP	N74LS259N	
Plastic SO	N74LS259D	
Ceramic DIP		S54LS259F
Flatpack		S54LS259W

DESCRIPTION

The '259 addressable latch has four distinct modes of operation that are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	10LSul

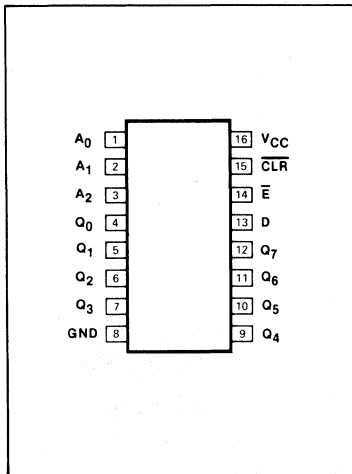
NOTE

A 54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL}.

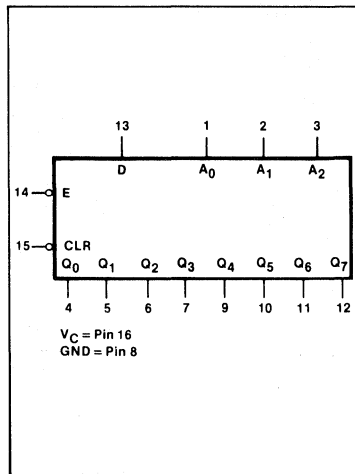
or demultiplexing mode ($\overline{CLR} = \overline{E} = \text{LOW}$), addressed outputs will follow the level of the D inputs, with all other outputs LOW.

In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

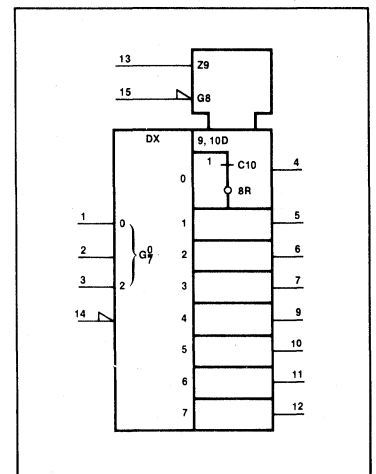
PIN CONFIGURATION



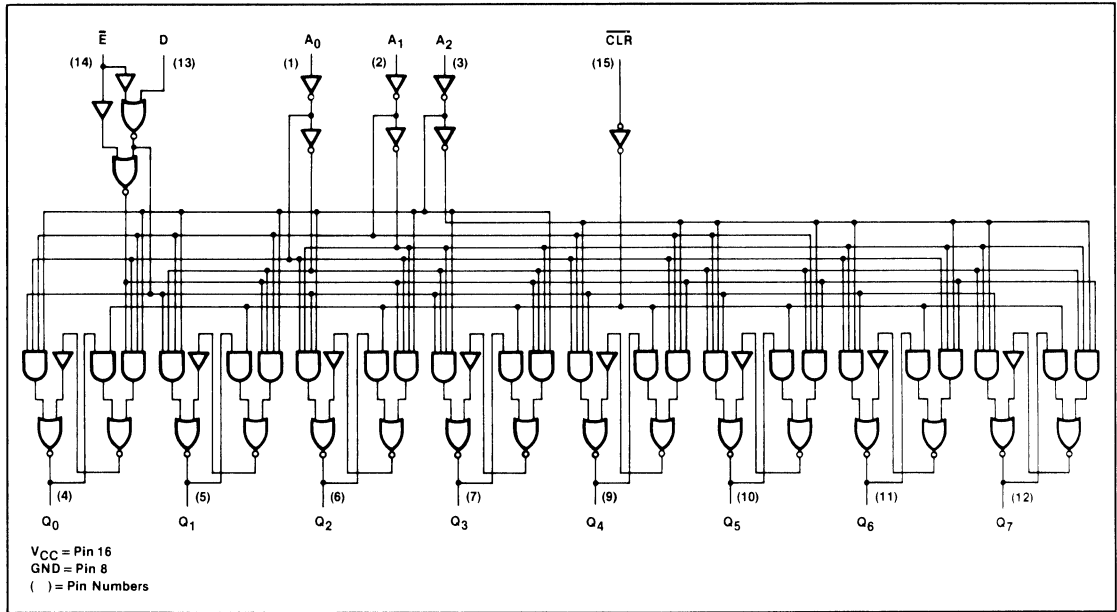
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



4

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	CLR̄	Ē	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	L	L	L	L	L	L
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q = d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q = d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q = d	q ₃	q ₄	q ₅	q ₆	q ₇
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q = d

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 X = Don't care.
 d = HIGH or LOW data one setup time prior to the LOW-to-HIGH Enable transition.
 q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

LATCH

54/74LS259

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I _{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I _{IH}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current				- 400	μA
I _{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

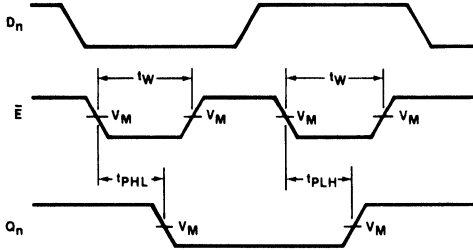
PARAMETER	TEST CONDITIONS ¹	54/74LS259			UNIT	
		Min	Typ ²	Max		
V _{OH}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V	
		Com'l	2.7	3.4	V	
V _{OL}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.25	0.4	V
				0.35	0.5	V
		I _{OL} = 4mA	74LS	0.25	0.4	V
V _{IK}	V _{CC} = MIN, I _I = I _{IK}				- 1.5	V
I _I	V _{CC} = MAX, V _I = 7.0V				0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7V				20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4V				- 0.4	mA
I _{OS}	V _{CC} = MAX	- 20			- 100	mA
I _{CC}	V _{CC} = MAX		22	36	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the inputs grounded and the outputs open.

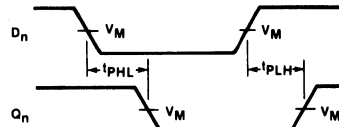
AC WAVEFORMS

PROPAGATION DELAY ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



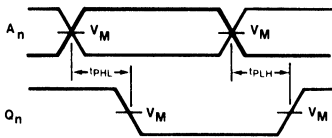
Waveform 1

PROPAGATION DELAY DATA TO OUTPUT



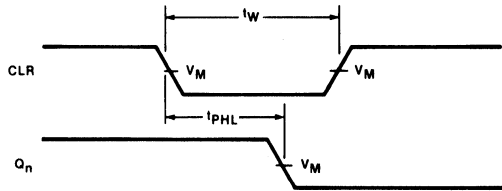
Waveform 2

PROPAGATION DELAY ADDRESS TO OUTPUT



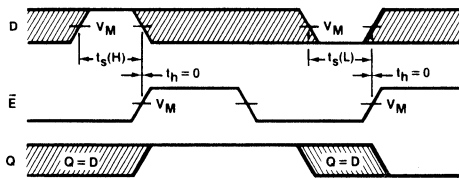
Waveform 3

CLEAR TO OUTPUT DELAY AND CLEAR PULSE WIDTH



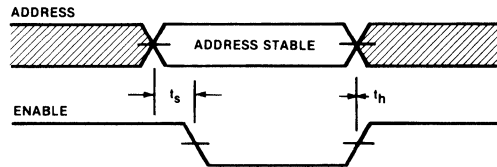
Waveform 4

DATA SETUP AND HOLD TIMES



Waveform 5

ADDRESS SETUP AND HOLD TIMES



Waveform 6

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

LATCH

54/74LS259

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1	35 24	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2	32 21	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 3	38 29	ns
t_{PHL}	Propagation delay, Clear to output	Waveform 4	27	ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

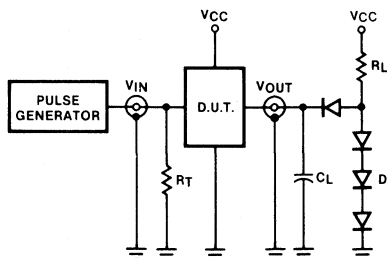
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_W	Enable pulse width	Waveform 1	15	ns
t_W	Clear pulse width	Waveform 4	15	ns
$t_s(H)$	Setup time HIGH, Data to Enable	Waveform 5	15	ns
$t_h(H)$	Hold time HIGH, Data to Enable	Waveform 5	5	ns
$t_s(L)$	Setup time LOW, Data to Enable	Waveform 5	15	ns
$t_h(L)$	Hold time LOW, Data to Enable	Waveform 5	5	ns
t_s	Setup time, Address to Enable ^(a)	Waveform 6	15	ns
t_h	Hold time, Address to Enable ^(b)	Waveform 6	15	ns

NOTES

- a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
- b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

TEST CIRCUITS AND WAVEFORMS

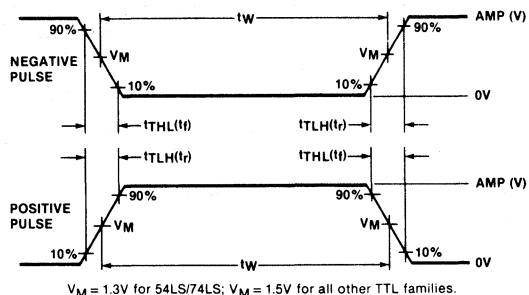
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

GATES

54/74LS260, S260

Dual 5-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS260	9ns	4mA
74S260	4ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{cc} = 5V ± 5%; T _A = 0°C to + 70°C	V _{cc} = 5V ± 10%; T _A = -55°C to + 125°C
Plastic DIP	N74S260N • N74LS260N	
Plastic SO	N74LS260D • N74S260D	
Ceramic DIP		S54S260F • S54LS260F
Flatpack		S54S260W • S54LS260W
LLCC		S54S260G

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

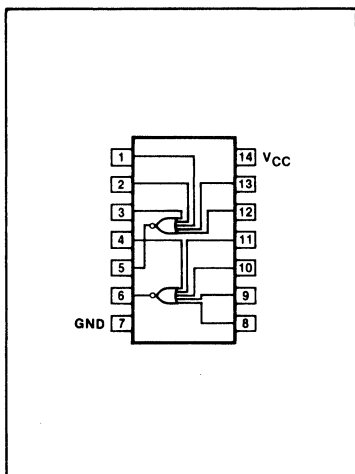
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
A-E	Inputs	1Sul	1LSul
Y	Outputs	10Sul	10LSul

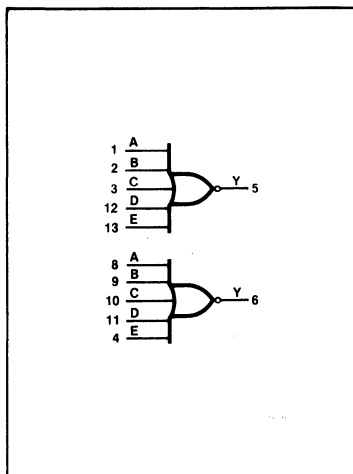
NOTE
 Where a 54/74S unit load (Sul) is 50µA I_{IH} and - 2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20µA I_{IH} and - 0.4mA I_{IL}.



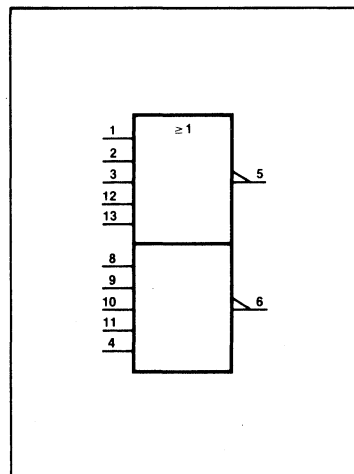
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	54S	74LS	74S	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I _{IN} Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

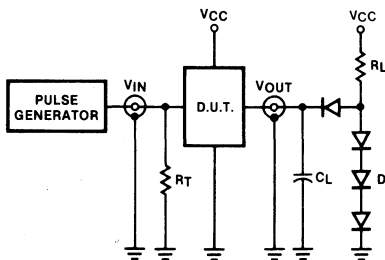
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			2.0			V
V _{IL} LOW-level input voltage	Mil			+0.7			+0.8	V
	Com'l			+0.8			+0.8	V
I _{IK} Input clamp current				-18			-18	mA
I _{OH} HIGH-level output current				-400			-1000	μA
I _{OL} LOW-level output current	Mil			4			20	mA
	Com'l			8			20	mA
T _A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

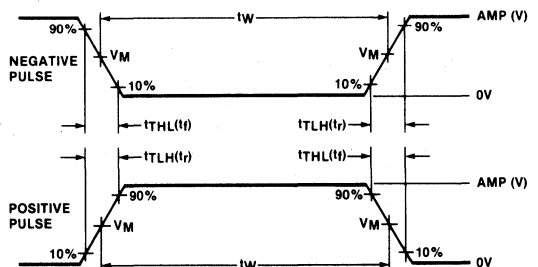
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

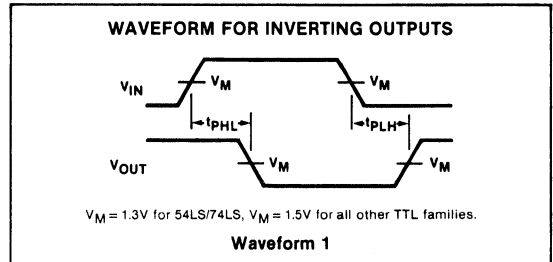
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS260			54/74S260			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5		2.5			V
		Com'l	2.7		2.7			V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN	I _{OL} = MAX	Mil		0.4		0.5 ⁴	V
			Com'l		0.5		0.5	V
		I _{OL} = 4mA	74LS		0.4			V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5		-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V					1.0	mA
		V _I = 7.0V		0.1			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V		20		50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V		-0.4			mA	
		V _I = 0.5V				-2	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-15	-100	-40	-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCH} Outputs HIGH		4		17	29	mA
		I _{CCL} Outputs LOW		5.5		26	45	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORM



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL}	Propagation delay	Waveform 1	12 12	5.5 6.0	ns	

GATE

54/74LS266

Quad 2-Input Exclusive-NOR Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS266	18ns	8mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{cc} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{cc} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS266N	
Ceramic DIP		S54LS266F
Flatpack		S54LS266W
LLCC		S54LS266G

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

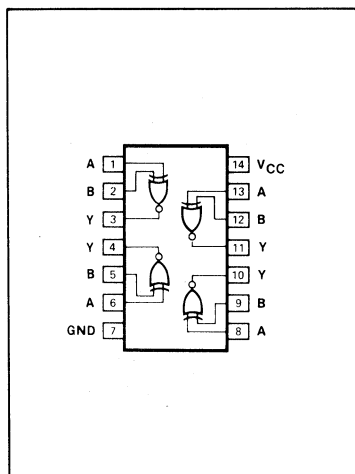
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

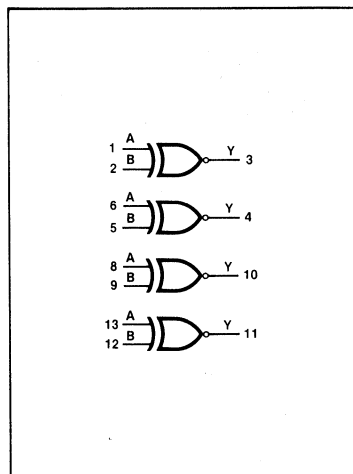
PINS	DESCRIPTION	54/74LS
A, B	Inputs	2LSul
Y	Output	10LSul

NOTE
A 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

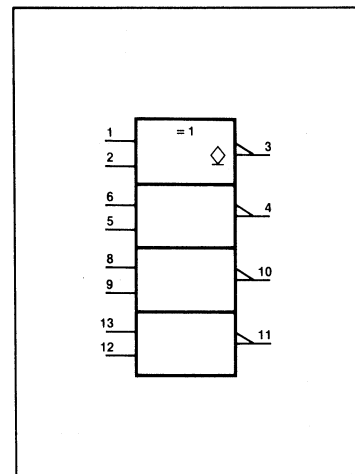
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I _{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

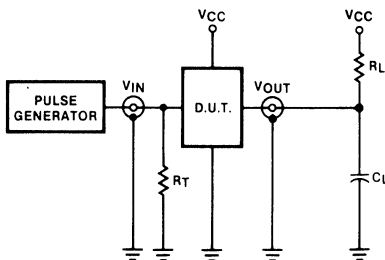
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT		
		Min	Nom	Max			
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	V	
V _{IH}	HIGH-level input voltage	2.0			V		
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V	
		Com'l			+ 0.8	V	
I _{IK}	Input clamp current				- 18	mA	
V _{OH}	HIGH-level output voltage				5.5	V	
I _{OL}	LOW-level output current	Mil			4	mA	
		Com'l			8	mA	
T _A	Operating free-air temperature	Mil	- 55			+ 125	°C
		Com'l	0			70	°C

4

TEST CIRCUITS AND WAVEFORMS

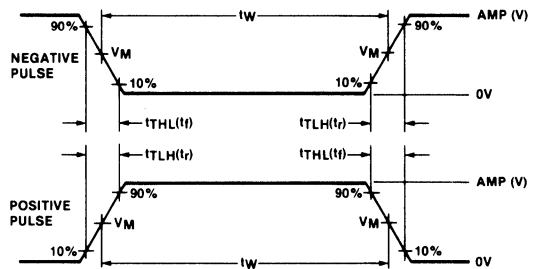
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

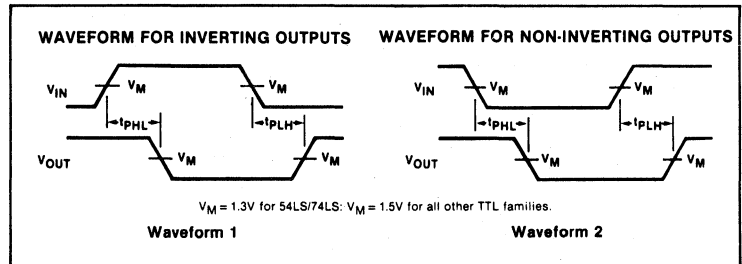
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS266			UNIT	
		Min	Typ ²	Max		
I _{OH} HIGH-level output current	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, V _{OH} = 5.5V			100	μA	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.2	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			40	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.8	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		8	13	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with one input of each gate at 4.5V, the other inputs grounded and the outputs open.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} Propagation delay A or B to output	Waveform 1, other input LOW		30	ns
t _{PHL} Propagation delay A or B to output			30	
t _{PLH} Propagation delay A or B to output	Waveform 2, other input HIGH		30	ns
t _{PHL} Propagation delay A or B to output			30	

FLIP-FLOPS

54/74LS273, S273

Octal D Flip-Flops

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- High speed Schottky version available
- Buffered common clock
- Buffered, asynchronous Master Reset
- Slim 20-pin plastic and ceramic DIP packages
- See '377 for Clock Enable version
- See '373 for transparent latch version
- See '374 for 3-state version

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS273	40MHz	17mA
74S273	95MHz	109mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S273N • N74LS273N	
Plastic SO	N74LS273D • N74S273D	
Ceramic DIP		S54LS273F
LLCC		S54LS273G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

DESCRIPTION

The '273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition,

NOTE

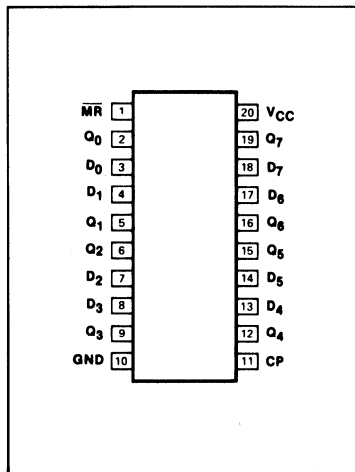
A 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

is transferred to the corresponding flip-flop's Q output.

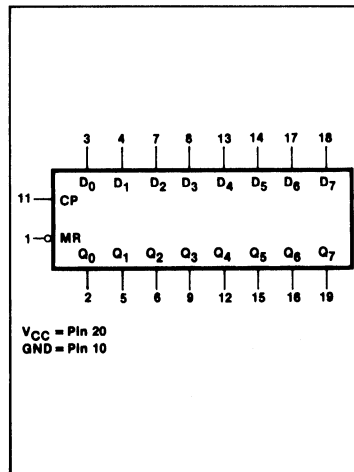
All outputs will be forced LOW independently of Clock or Data inputs by a LOW

voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

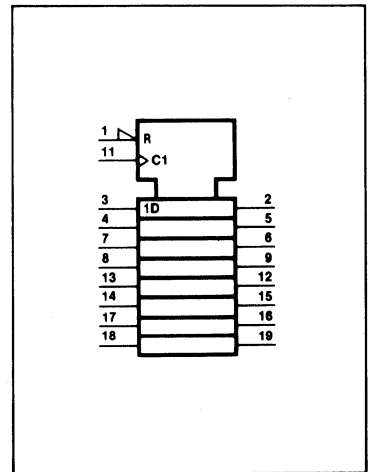
PIN CONFIGURATION



LOGIC SYMBOL



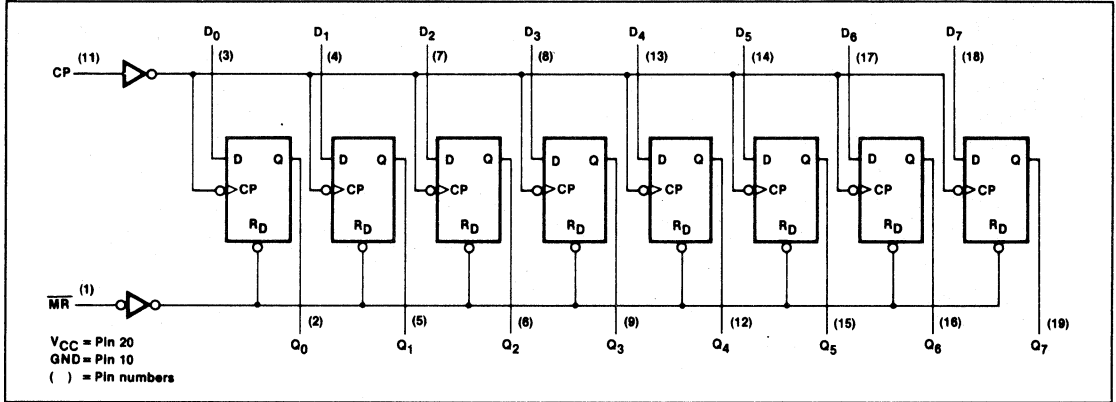
LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS

54/74LS273, S273

LOGIC DIAGRAM



MODE SELECT--FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	\overline{MR}	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V	
V_{IL}	LOW-level input voltage	Mil				+0.8			V
		Com'l				+0.8			V
I_{IK}	Input clamp current				-18			mA	
I_{OH}	HIGH-level output current				-400			μA	
I_{OL}	LOW-level output current	Mil				4			mA
		Com'l				8			mA
T_A	Operating free-air temperature	Mil	-55	+125		-55	+125		°C
		Com'l	0	70		0	70		°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS273			54/74S273			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		2.5		V		
		Com'l	2.7	3.4		2.7		V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4			0.5	V	
			Com'l		0.35	0.5			0.5	V
		I _{OL} = 4mA	74LS		0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}						-1.5	-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V						1.0	mA	
		V _I = 7.0V				0.1			mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V					20		50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V							mA	
		V _I = 0.5V						-2.0	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-20			-100	-40		mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			17	27		109	150	mA	

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} after a momentary ground, then 4.5V is applied to clock with all outputs open and 4.5V applied to all Data inputs and the Master Reset input.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	30		75		MHz
t _{PLH} Propagation delay	Waveform 1		27		15	ns
t _{PHL} Clock to output			27		15	
t _{PHL} Propagation delay, MR to output	Waveform 2		27		15	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

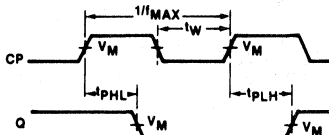
AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
		Min	Max	Min	Max	
t _{w(L)} Clock pulse width (LOW)	Waveform 1	20		7.0		ns
t _w Master Reset pulse width	Waveform 2	20		10		ns
t _{s(H)} Setup time, HIGH data to CP	Waveform 3	20		5.0		ns
t _{h(H)} Hold time, HIGH data to CP	Waveform 3	5.0		3.0		ns
t _{s(L)} Setup time, LOW data to CP	Waveform 3	20		5.0		ns
t _{h(L)} Hold time, LOW data to CP	Waveform 3	5.0		3.0		ns
t _{rec} Recovery time, MR to CP	Waveform 2	25		5.0		ns



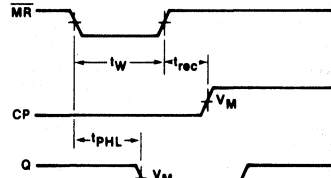
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



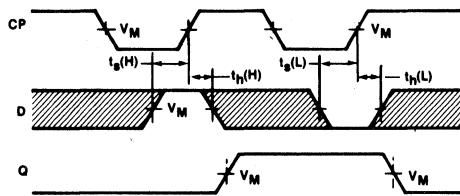
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

DATA SET-UP AND HOLD TIMES

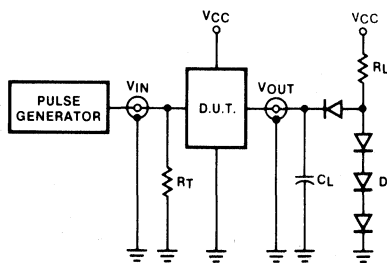


Waveform 3

$V_M = 1.5V$ for 54/74 and 54/74S; $V_M = 1.3V$ for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

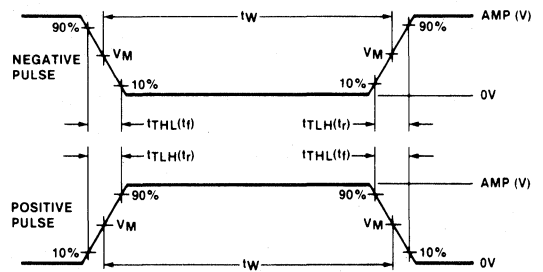
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH

54/74279

Quad Set-Reset Latch

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74279	13ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = -55°C to + 125°C
Plastic DIP	N74279N	
Plastic SO	N74279D	
Ceramic DIP		S54279F
Flatpack		S54279W

FUNCTION TABLE

INPUTS			OUTPUT
\bar{S}_1	\bar{S}_2	\bar{R}	Q
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No change

L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.

h = The output is HIGH as long as \bar{S}_1 or \bar{S}_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the truth table.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

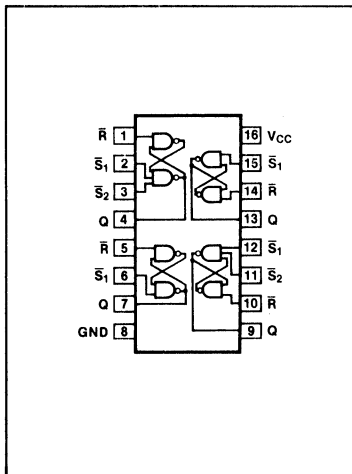
PINS	DESCRIPTION	54/74
All	Inputs	1uI
Q	Output	10uI

NOTE

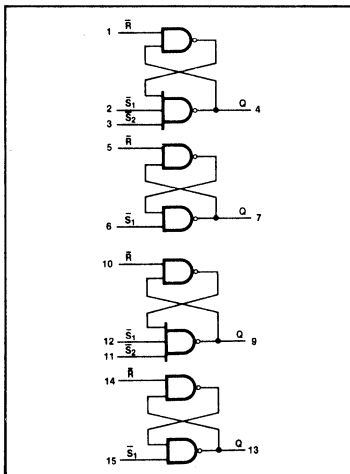
A 54/74 unit load (uI) is 40µA I_{IH} and - 1.6mA I_{IL}.

4

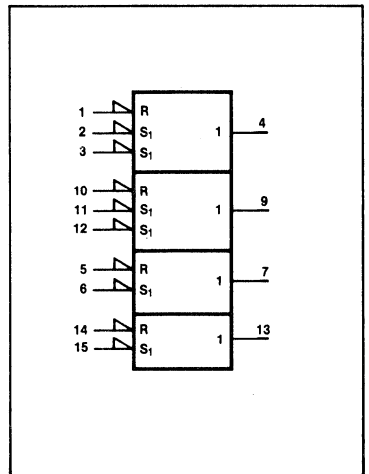
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LATCH

54/74279

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

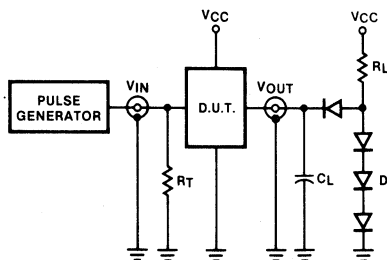
PARAMETER	54	74	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I _{IN} Input current	- 30 to + 5	- 30 to + 5	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

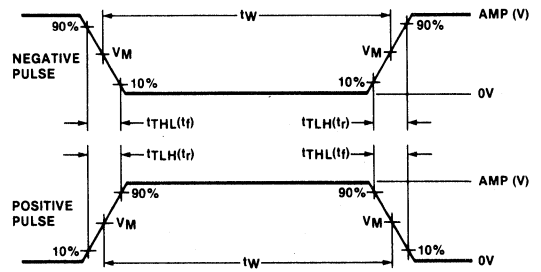
PARAMETER	54/74			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.5	V
	Com'l	4.75	5.25	V
V _{IH} HIGH-level input voltage		2.0		V
V _{IL} LOW-level input voltage	Mil		+ 0.8	V
	Com'l		+ 0.8	V
I _{IK} Input clamp current			- 12	mA
I _{OH} HIGH-level output current			- 800	μA
I _{OL} LOW-level output current	Mil		16	mA
	Com'l		16	mA
T _A Operating free-air temperature	Mil	- 55	+ 125	°C
	Com'l	0	70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

DEFINITIONS

- R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

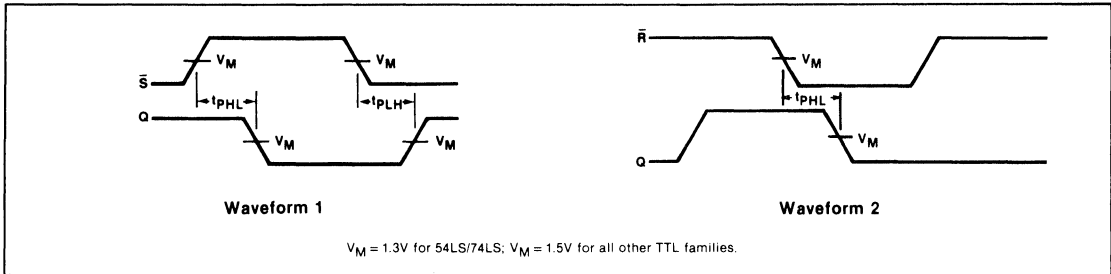
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74279		UNIT	
		Min	Typ ²		Max
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4	V
		Com'l	2.4	3.4	V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.2	0.4
		Com'l		0.2	0.4
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V				1.0
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.4V				40
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-1.6
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-18		-55
		Com'l	-18		-57
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			18	30

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all \bar{R} inputs grounded, all \bar{S} inputs at 4.5V, and all outputs open.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		UNIT
		C _L = 15pF, R _L = 400Ω		
		Min	Max	
t _{PLH} Propagation delay Set to output	Waveform 1		22	ns
t _{PHL} Propagation delay Reset to output			15	
t _{PHL} Propagation delay Reset to output	Waveform 2		27	ns

PARITY GENERATOR/CHECKER

54/74S280

9-Bit Odd/Even Parity Generator/Checker

- **Buffered inputs — one normalized load**
- **Word-length easily expanded by cascading**
- **Similar pin configuration to '180 for easy system up-grading**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
74S280	16ns	67mA

DESCRIPTION

The '280 is a 9-bit parity generator or checker commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is HIGH when an even number of Data inputs (I_0-I_8) are HIGH. The Odd parity output (Σ_O) is HIGH when an odd number of data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E) of up to nine parallel devices to the Data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 40ns with the 'S280.

ORDERING CODE

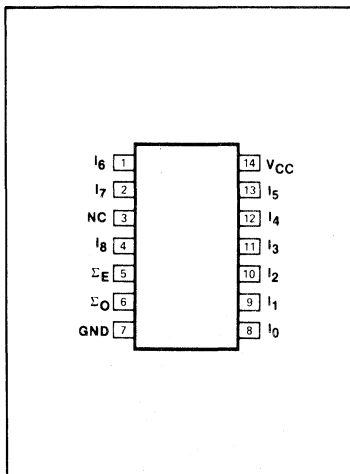
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S280N	
Ceramic DIP		S54S280F
Flatpack		S54S280W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

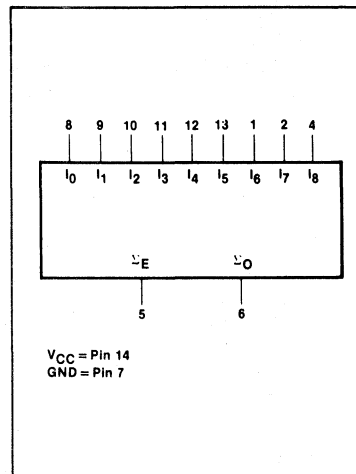
PINS	DESCRIPTION	54/74S
I_0-I_8	Data inputs	1Sul
Σ_E, Σ_O	Parity outputs	10Sul

NOTE
A 54/74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

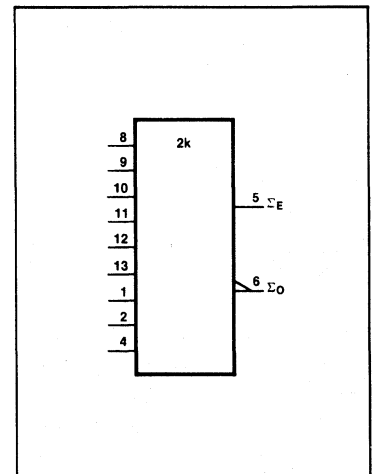
PIN CONFIGURATION



LOGIC SYMBOL



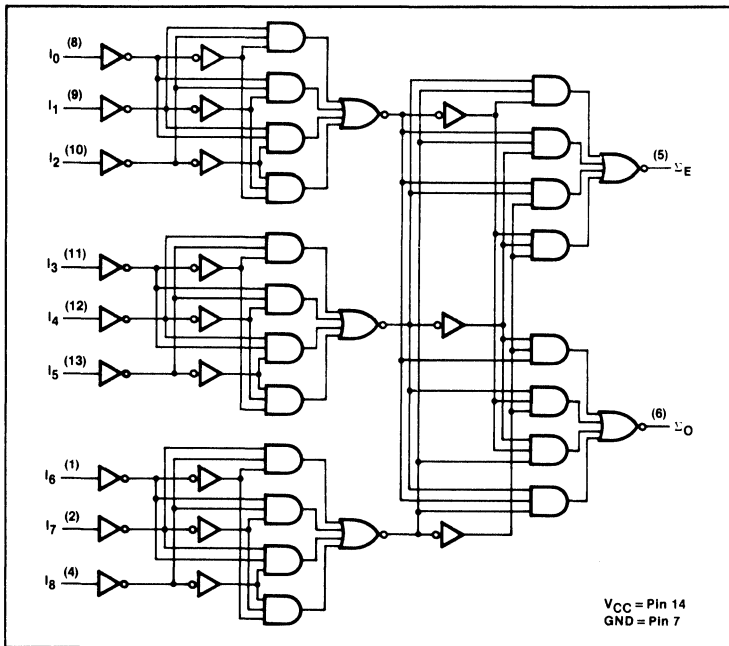
LOGIC SYMBOL (IEEE/IEC)



PARITY GENERATOR/CHECKER

54/74S280

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS Number of HIGH Data inputs (I_0-I_8)	OUTPUTS	
	Σ_E	Σ_O
Even	H	L
Odd	L	H

H = HIGH voltage level
L = LOW voltage level

4

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54S	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I_{IN} Input current	- 30 to + 5	- 30 to + 5	mA
V_{OUT} Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74S			UNIT
		Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			V
V_{IL} LOW-level input voltage	Mil			+ 0.8	V
	Com'l			+ 0.8	V
I_{IK} Input clamp current				- 18	mA
I_{OH} HIGH-level output current				- 1000	μ A
I_{OL} LOW-level output current	Mil			20	mA
	Com'l			20	mA
T_A Operating free-air temperature	Mil	- 55		+ 125	°C
	Com'l	0		70	°C

$V_{IL} = + 0.7V$ MAX for 54S at $T_A = + 125^\circ C$ only.

PARITY GENERATOR/CHECKER

54/74S280

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74S280			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IL} = MAX, I _{OH} = MAX, V _{IH} = MIN	Mil	2.5	3.4	V
		Com'l	2.7	3.4	V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, I _{OL} = MAX, V _{IL} = MAX	Mil		0.5 ⁵	V
		Com'l		0.5	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			- 1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			50	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V			- 2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	- 40		- 100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Mil		99	mA
		Com'l		105	mA

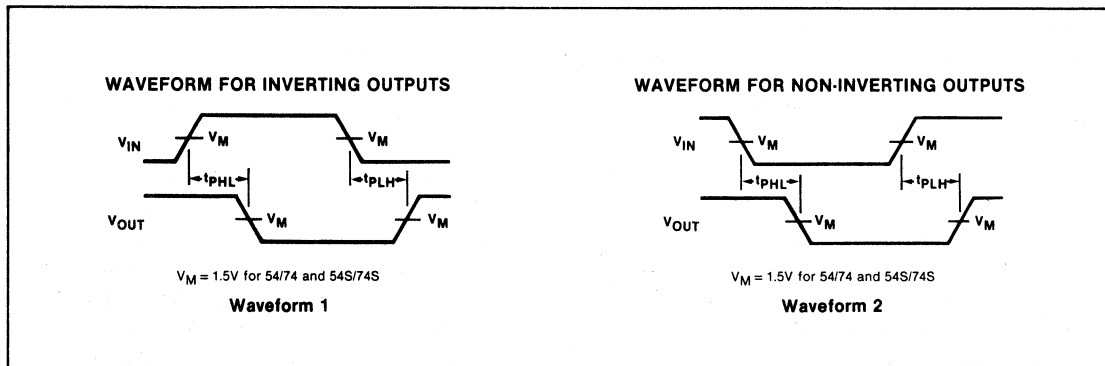
NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all inputs grounded and all outputs open.
- V_{OL} = +0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

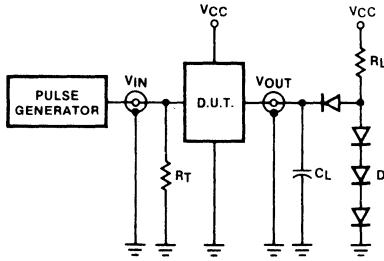
PARAMETER	TEST CONDITIONS	54/74S280		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
t _{PLH} Propagation delay t _{PHL} Data to Even output	Waveforms 1 & 2		21 18	ns
t _{PLH} Propagation delay t _{PHL} Data to Odd output	Waveforms 1 & 2		21 18	ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

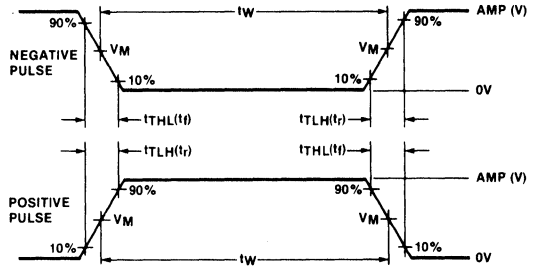
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

ADDER

54/74LS283

4-Bit Full Adder With Fast Carry

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal carry lookahead

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS283	13ns	20mA

DESCRIPTION

The '283 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the '283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic)—see Function Table. In case of all active LOW operands the results $\Sigma_1 - \Sigma_4$ and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN} , A_1 , B_1 can arbitrarily be assigned to pins 5, 6, 7, etc.

ORDERING CODE

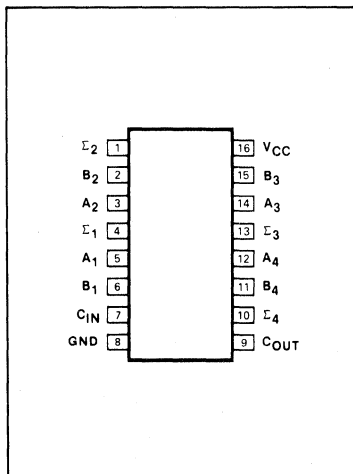
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS283N	
Plastic SO	N74LS283D	
Ceramic DIP		S54LS283F
Flatpack		S54LS283W
LLCC		S54LS283G

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

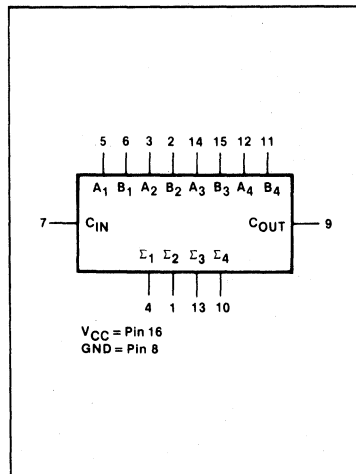
PINS	DESCRIPTION	54/74LS
A, B	Inputs	2LSul
C_{IN}	Input	1LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL} .

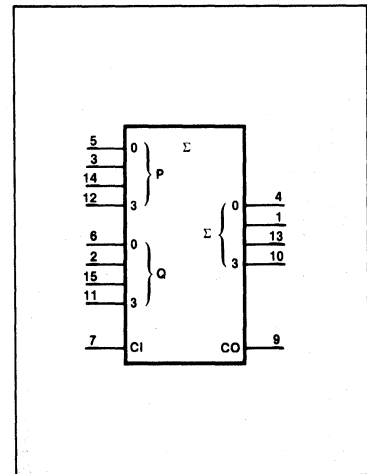
PIN CONFIGURATION



LOGIC SYMBOL



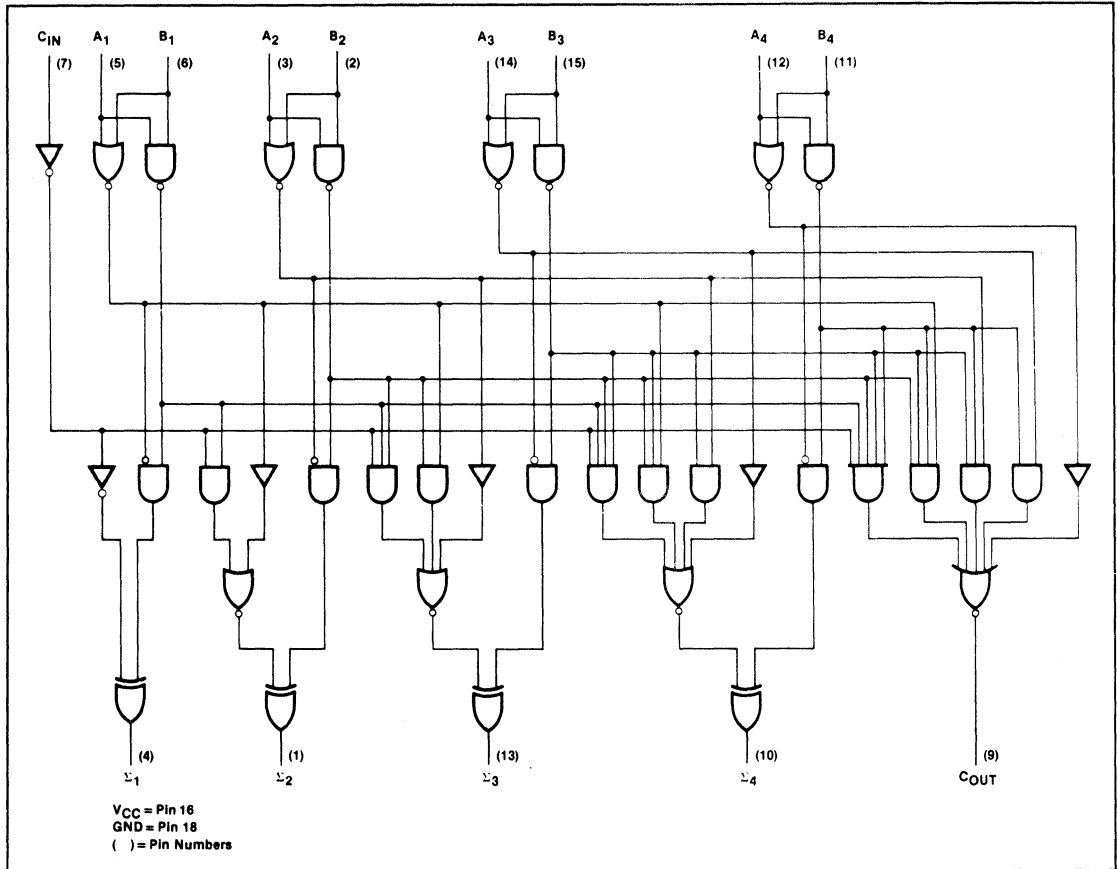
LOGIC SYMBOL (IEEE/IEC)



ADDER

54/74LS283

LOGIC DIAGRAM



4

FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Example:
 1001
 1010
 10011
 (10 + 9 = 19)
 (carry + 5 + 6 = 12)

H = LOW voltage level
 L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I_{IN} Input current	-30 to +1	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current				- 400	μA
I _{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

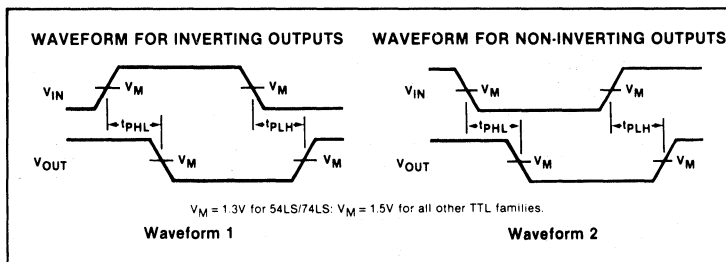
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS283			UNIT	
		Min	Typ ²	Max		
V _{OH}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		V
		Com'l	2.7	3.4		V
V _{OL}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
		I _{OL} = 4mA	74LS	0.25	0.4	V
V _{IK}	V _{CC} = MIN, I _I = I _{IK}				- 1.5	V
I _I	V _{CC} = MAX, V _I = 7.0V	A, B inputs			0.2	mA
		C _{IN} input			0.1	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7V	A, B inputs			40	μA
		C _{IN} input			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4V	A, B inputs			- 0.8	mA
		C _{IN} input			- 0.4	mA
I _{OS}	V _{CC} = MAX		- 20		- 100	mA
I _{CC}	V _{CC} = MAX	Condition 1		22	39	mA
		Condition 2		19	34	mA
		Condition 3		19	34	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} should be measured with all outputs open and the following conditions:
 Condition 1: All inputs grounded.
 Condition 2: All B inputs LOW, other inputs at 4.5V.
 Condition 3: All inputs at 4.5V.

AC WAVEFORMS



ADDER

54/74LS283

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	
t_{PLH} t_{PHL} Propagation delay C_{IN} to Σ_1	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL} Propagation delay C_{IN} to Σ_2	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL} Propagation delay C_{IN} to Σ_3	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL} Propagation delay C_{IN} to Σ_4	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL} Propagation delay A_i or B_i to Σ_i	Waveforms 1 & 2		24 24	ns
t_{PLH} t_{PHL} Propagation delay C_{IN} to C_{OUT}	Waveform 2		17 22	ns
t_{PLH} t_{PHL} Propagation delay A_i or B_i to C_{OUT}	Waveforms 1 & 2		17 17	ns



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS

INPUT PULSE DEFINITIONS

$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

COUNTER

54/74LS290

Decade Counter

DESCRIPTION

The '290 is a 4-bit, ripple type decade counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) which overrides the Clock and MR Inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the \overline{CP}_1 input must be externally connected to the Q_0 output. The \overline{CP}_0 input receives the incoming count, producing a BCD count sequence. In a symmetrical bi-quinary divide-by-ten counter the Q_3 output must be connected externally to the \overline{CP}_0 input. The input count is then applied to the \overline{CP}_1 input and a divide-by-ten square wave is obtained at

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS290	42MHz	9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS290N	
Plastic SO	N74LS290D	
Ceramic DIP		S54LS290F
Flatpack		S54LS290W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

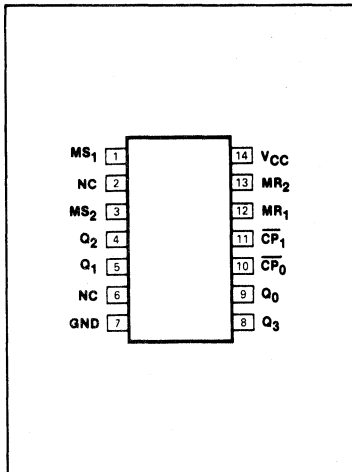
PINS	DESCRIPTION	54/74LS
MR, MS	Inputs	1LSul
\overline{CP}_0	Input	4LSul
\overline{CP}_1	Input	8LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

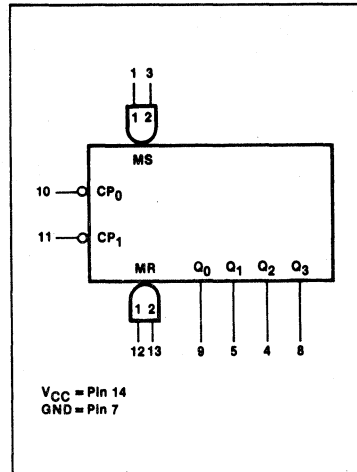
output Q_0 . To operate as a divide-by-two and a divide-by-five counter, no external interconnections are required. The first flip-flop is used as a binary element for the

divide-by-two function (\overline{CP}_0 as the input and Q_0 as the output). The \overline{CP}_1 input is used to obtain divide-by-five operation at the Q_3 output.

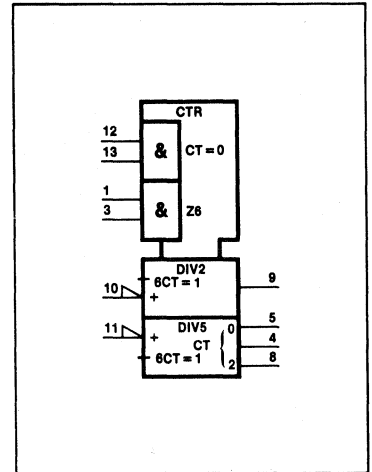
PIN CONFIGURATION



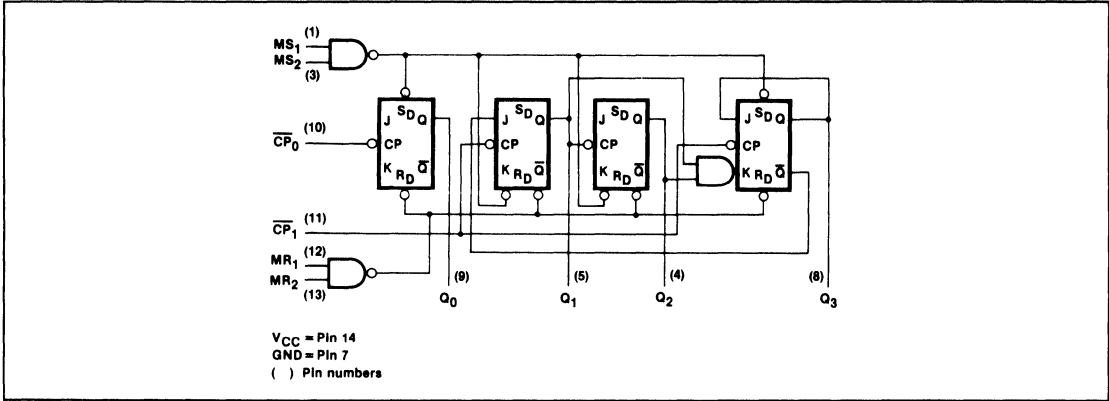
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECTION—FUNCTION TABLE

RESET/SET INPUTS				OUTPUTS			
MR ₁	MR ₂	MS ₁	MS ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X		Count		
X	L	X	L		Count		
L	X	X	L		Count		
X	L	L	X		Count		

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

BCD COUNT SEQUENCE—FUNCTION TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE
 Output Q₀ connected to input CP₁.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

NOTE
 V_{IN} limited to +5.5V on CP₀ and CP₁ inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current				- 400	μA
I _{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74LS290			UNIT		
			Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		V	
			Com'l	2.7	3.4		V	
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4	V	
				Com'l	0.35	0.5	V	
			I _{OL} = 4mA	74LS	0.25	0.4	V	
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				- 1.5	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V	MR, MS inputs			0.1	mA
				CP ₀ input			0.2	mA
			V _I = 5.5V	CP ₁ input			0.4	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	MR, MS inputs			20	μA	
			CP ₀ input ⁵			40	μA	
			CP ₁ input ⁵			80	μA	
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V	MR, MS inputs			- 0.4	mA	
			CP ₀ input			- 2.4	mA	
			CP ₁ input			- 3.2	mA	
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		- 20		- 100	mA	
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX			9	15	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
- The maximum limit for the 54LS290 only is 80μA for CP₀ and 160μA for CP₁ inputs.

COUNTER

54/74LS290

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	
f_{MAX} $\overline{\text{CP}}_0$ input count frequency	Waveform 1	32		MHz
f_{MAX} $\overline{\text{CP}}_1$ input count frequency	Waveform 1	16		MHz
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CP}}_0$ input to Q_0 output	Waveform 1		16 18	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CP}}_1$ input to Q_1 output	Waveform 1		16 21	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CP}}_1$ input to Q_2 output	Waveform 1		32 35	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CP}}_1$ input to Q_3 output	Waveform 1		32 35	ns
t_{PLH} Propagation delay t_{PHL} $\overline{\text{CP}}_0$ input to Q_3 output	Waveform 1		48 50	ns
t_{PHL} MR input to any output	Waveform 2		40	ns
t_{PLH} MS input to Q_0 and Q_3 outputs	Waveform 3		30	ns
t_{PHL} MS input to Q_1 and Q_2 outputs	Waveform 2		40	ns

NOTE

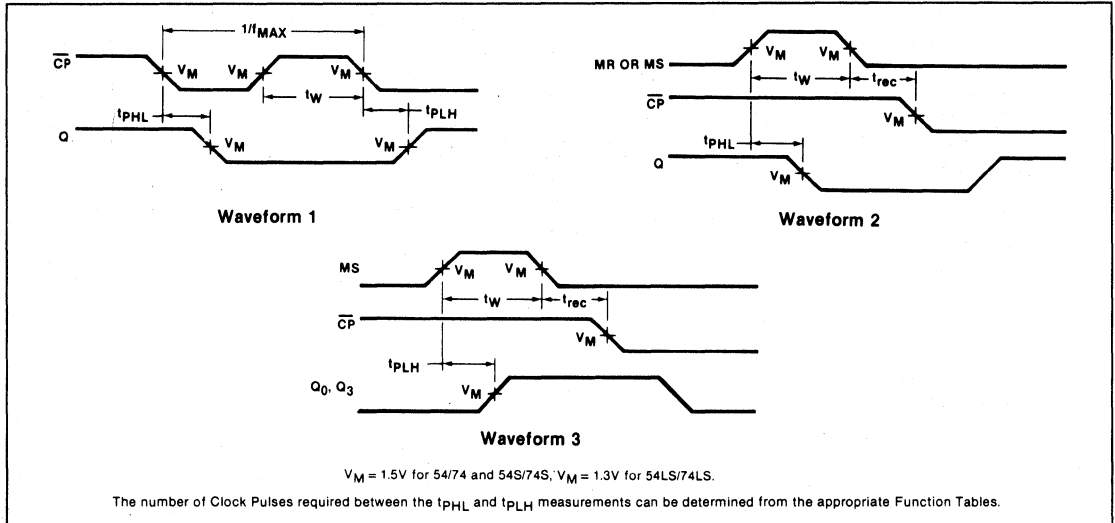
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

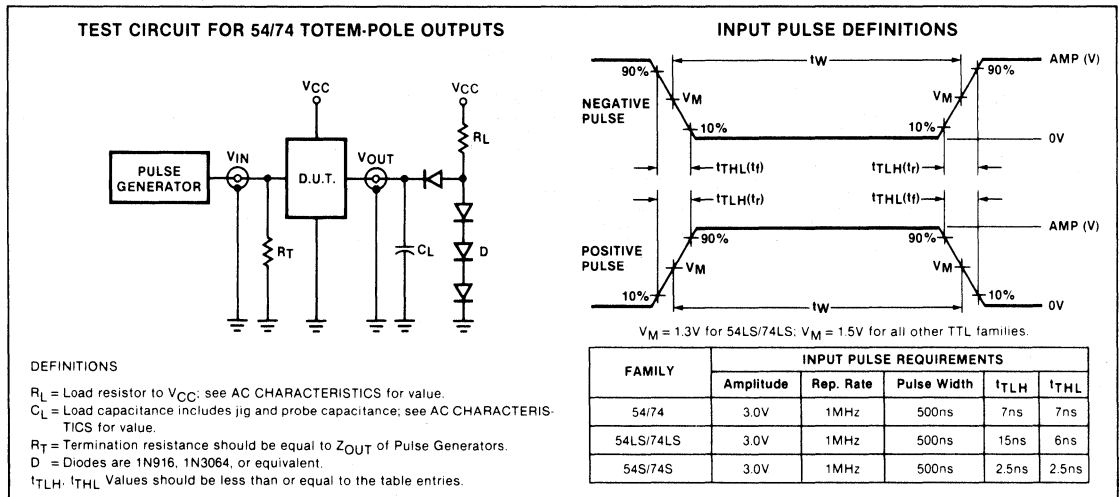
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_w $\overline{\text{CP}}_0$ pulse width	Waveform 1	15		ns
t_w $\overline{\text{CP}}_1$ pulse width	Waveform 1	30		ns
t_w MR pulse width	Waveform 2	15		ns
t_{rec} Recovery time, MR to $\overline{\text{CP}}$	Waveform 2	25		ns
t_{rec} Recovery time, MS to $\overline{\text{CP}}$	Waveforms 2 and 3	25		ns

4

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



4-Bit Binary Ripple Counter

DESCRIPTION

The '293 is a 4-bit ripple type binary counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR₁ MR₂) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q₀ must be connected externally to input CP₁. The input count pulses are applied to input CP₀. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q₀, Q₁, Q₂ and Q₃ outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input CP₁. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q₁, Q₂ and Q₃ outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

TYPE	TYPICAL f _{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS293	42MHz	9mA

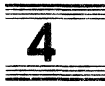
ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = -55°C to + 125°C
Plastic DIP	N74LS293N	
Plastic SO	N74LS293D	
Ceramic DIP		S54LS293F
Flatpack		S54LS293W

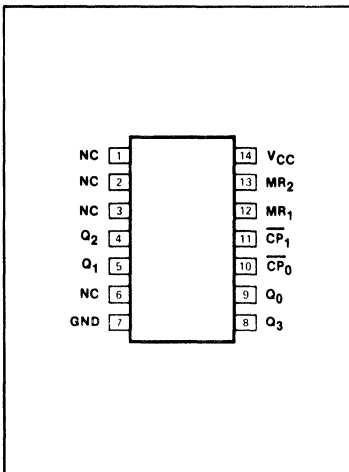
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
MR	Inputs	1LSul
CP ₀	Input	6LSul
CP ₁	Input	4LSul
All	Outputs	10LSul

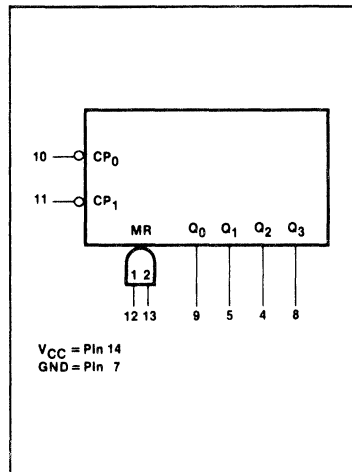
NOTE
A 54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL}.



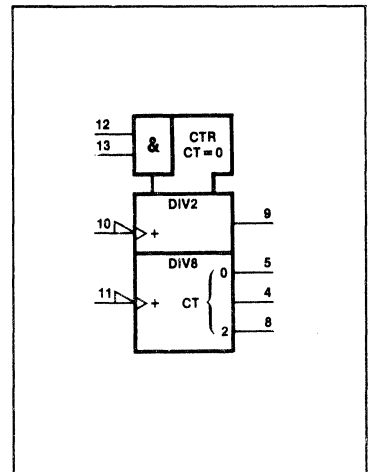
PIN CONFIGURATION



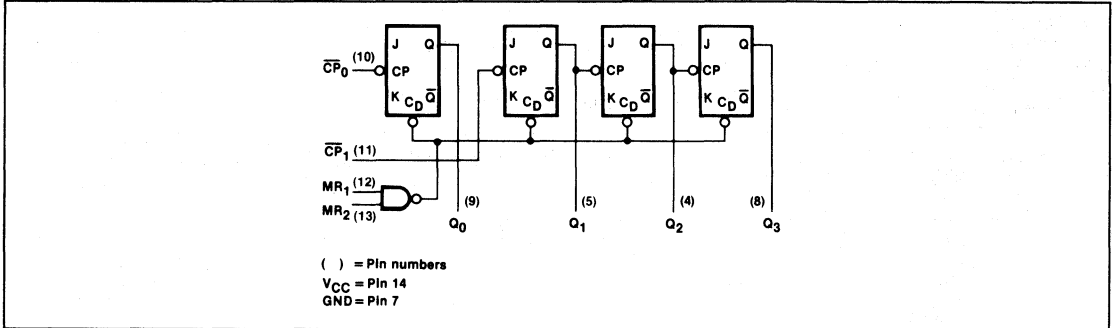
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECTION

RESET INPUTS		OUTPUTS			
MR ₁	MR ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	H	L	L	L	L
L	H		Count		
H	L		Count		
L	L		Count		

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

FUNCTION TABLE

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE
 Output Q₀ connected to input \overline{CP}_1 .

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I_{IN} Input current	-30 to +1	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

NOTE
 V_{IN} limited to 5.5V on \overline{CP}_0 and \overline{CP}_1 inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current				- 400	μA
I _{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS293			UNIT		
		Min	Typ ²	Max			
V _{OH}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		V	
		Com'l	2.7	3.4		V	
V _{OL}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.25	0.4	V
			Com'l		0.35	0.5	V
		I _{OL} = 4mA	74LS		0.25	0.4	V
V _{IK}	V _{CC} = MIN, I _I = I _{IK}				- 1.5	V	
I _I	V _{CC} = MAX	V _I = 7.0V	MR inputs		0.1	mA	
		V _I = 5.5V	CP inputs		0.2	mA	
I _{IH}	V _{CC} = MAX, V _I = 2.7V		MR inputs		20	μA	
			CP inputs ⁵		40	μA	
I _{IL}	V _{CC} = MAX, V _I = 0.4V		MR inputs		- 0.4	mA	
			CP ₀ input		- 2.4	mA	
			CP ₁ input		- 1.6	mA	
I _{OS}	V _{CC} = MAX		- 20		- 100	mA	
I _{CC}	V _{CC} = MAX			9	15	mA	

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with Clock inputs grounded, all outputs open, both MR inputs grounded following momentary connection to 4.5V.
 - The maximum limit for the 54LS293 is 80μA for CP₀ and CP₁ inputs.

COUNTER

54/74LS293

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	
f_{MAX} \overline{CP}_0 input count frequency	Waveform 1	32		MHz
f_{MAX} \overline{CP}_1 input count frequency	Waveform 1	16		MHz
t_{PLH} t_{PHL} Propagation delay \overline{CP}_0 input to Q_0 output	Waveform 1		16 18	ns
t_{PLH} t_{PHL} Propagation delay \overline{CP}_1 input to Q_1 output	Waveform 1		16 21	ns
t_{PLH} t_{PHL} Propagation delay \overline{CP}_1 input to Q_2 output	Waveform 1		32 35	ns
t_{PLH} t_{PHL} Propagation delay \overline{CP}_1 input to Q_3 output	Waveform 1		51 51	ns
t_{PLH} t_{PHL} Propagation delay \overline{CP}_0 input to Q_3 output	Waveform 1		70 70	ns
t_{PHL} MR input to any output	Waveform 2		40	ns

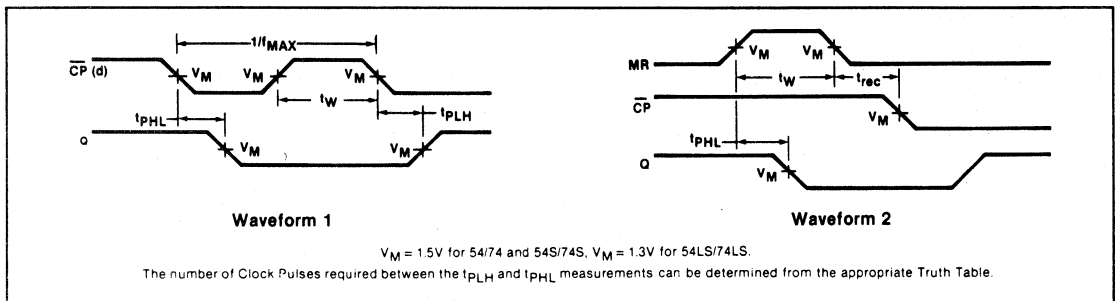
NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

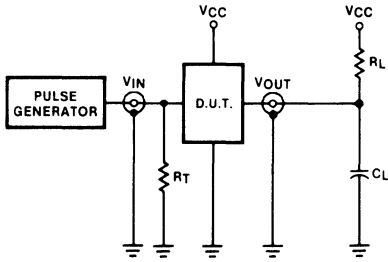
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_W \overline{CP}_0 pulse width	Waveform 1	15		ns
t_W \overline{CP}_1 pulse width	Waveform 1	30		ns
t_W MR pulse width	Waveform 2	15		ns
t_{rec} Recovery time, MR to \overline{CP}	Waveform 2	25		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

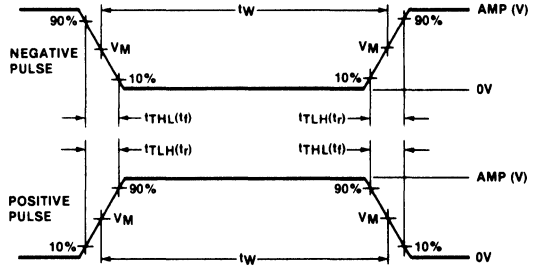
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTER

54/74LS295B

4-Bit Shift Register With 3-State Outputs

- 4-bit parallel load shift register
- Independent 3-State buffer outputs
- See '395 for serial expansion and Master Reset version

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS295B	45MHz	17mA

DESCRIPTION

The '295B is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data outputs (D_0 – D_3) into the register synchronous with the HIGH-to-LOW transition of the Clock input (\overline{CP}). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction (Q_0 – Q_1 – Q_2 – Q_3) synchronous with the negative transition of the Clock. The PE and Data inputs are fully edge triggered and must be stable only one setup time prior to the HIGH-to-LOW transition of the Clock.

The 3-State output buffers are designed to drive heavily loaded 3-state buses or large capacitive loads. The active HIGH Output Enable (OE) controls all four 3-state buffers independent of the register operation.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS295BN	
Ceramic DIP		S54LS295BF
Flatpack		S54LS295BW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

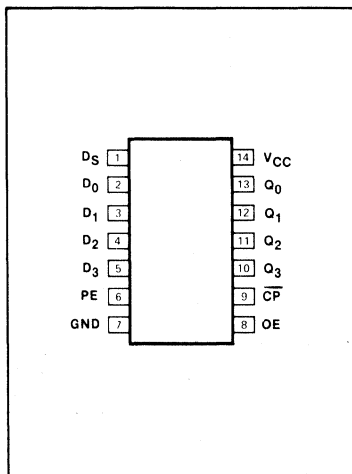
NOTE

A 54/74LS unit load (LSul) is $20\mu A$ and I_{IH} and $-0.4mA$ I_{IL} .

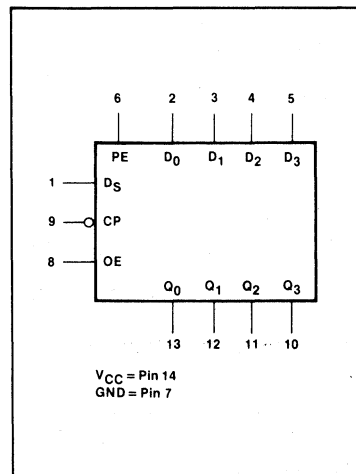
When OE is HIGH the data in the register appears at the outputs. When OE is LOW

the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

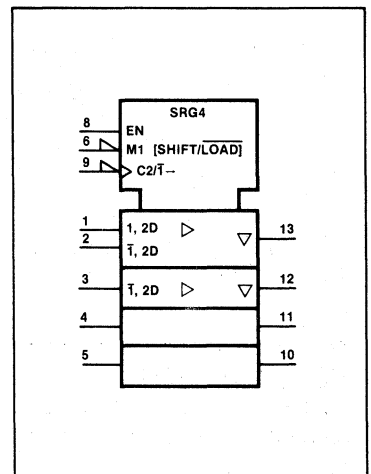
PIN CONFIGURATION



LOGIC SYMBOL



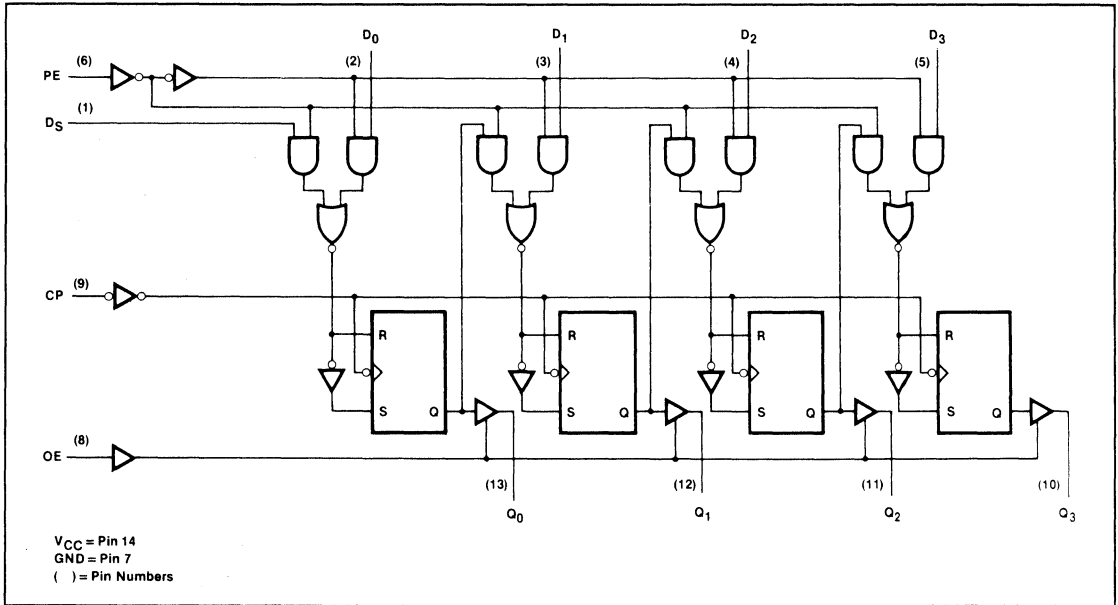
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER

54/74LS295B

LOGIC DIAGRAM



4

MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS				REGISTER OUTPUTS			
	\overline{CP}	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Shift right	l	l	l	X	L	Q_0	Q_1	Q_2
	l	l	h	X	H	Q_0	Q_1	Q_2
Parallel load	l	h	X	l	L	L	L	L
	l	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	OE	Q_n (Register)	Q_0, Q_1, Q_2, Q_3
Read	H	L	L
	H	H	H
Disabled	L	X	(Z)

H = HIGH voltage level.
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition.
 L = LOW voltage level.
 l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.
 q_n = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition.
 X = Don't care.
 (Z) = HIGH impedance "off" state.
 † = HIGH-to-LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I_{IN} Input current	- 30 to + 1	- 30 to + 1	mA
V_{OUT} Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current	Mil			- 1.0	mA
		Com'l			- 2.6	mA
I _{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS295B			UNIT		
		Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		V	
		Com'l	2.4	3.1		V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.25	0.4	V
			Com'l		0.35	0.5	V
		I _{OL} = 12mA	74LS		0.25	0.4	V
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}				-1.5	V	
I _{ozH}	Off-state output current, HIGH-level voltage applied V _{CC} = MAX, V _{IL} = MAX, V _O = 2.7V				20	μA	
I _{ozL}	Off-state output current, LOW-level voltage applied V _{CC} = MAX, V _{IH} = MIN, V _O = 0.4V				- 20	μA	
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 7.0V				0.1	mA	
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.7V				20	μA	
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.4V				- 0.4	mA	
I _{os}	Short-circuit output current ³ V _{CC} = MAX		- 30		- 130	mA	
I _{CC}	Supply current ⁴ (total) V _{CC} = MAX	Condition 1		16	29	mA	
		Condition 2		17	33	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the outputs open, D_S and PE at 4.5V, and the Data inputs grounded under the following conditions:
Condition 1: OE at 4.5V and a momentary 3V, then ground, applied to the Clock input.
Condition 2: OE and Clock input grounded.

SHIFT REGISTER

54/74LS295B

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	
f_{MAX} Maximum Clock frequency	Waveform 1	30		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		23 30	ns
t_{PZH} Enable time to HIGH level	Waveform 2		26	ns
t_{PZL} Enable time to LOW level	Waveform 3		30	ns
t_{PHZ} Disable time from HIGH level	Waveform 2, $C_L = 5\text{pF}$		20	ns
t_{PLZ} Disable time from LOW level	Waveform 3, $C_L = 5\text{pF}$		20	ns

NOTE

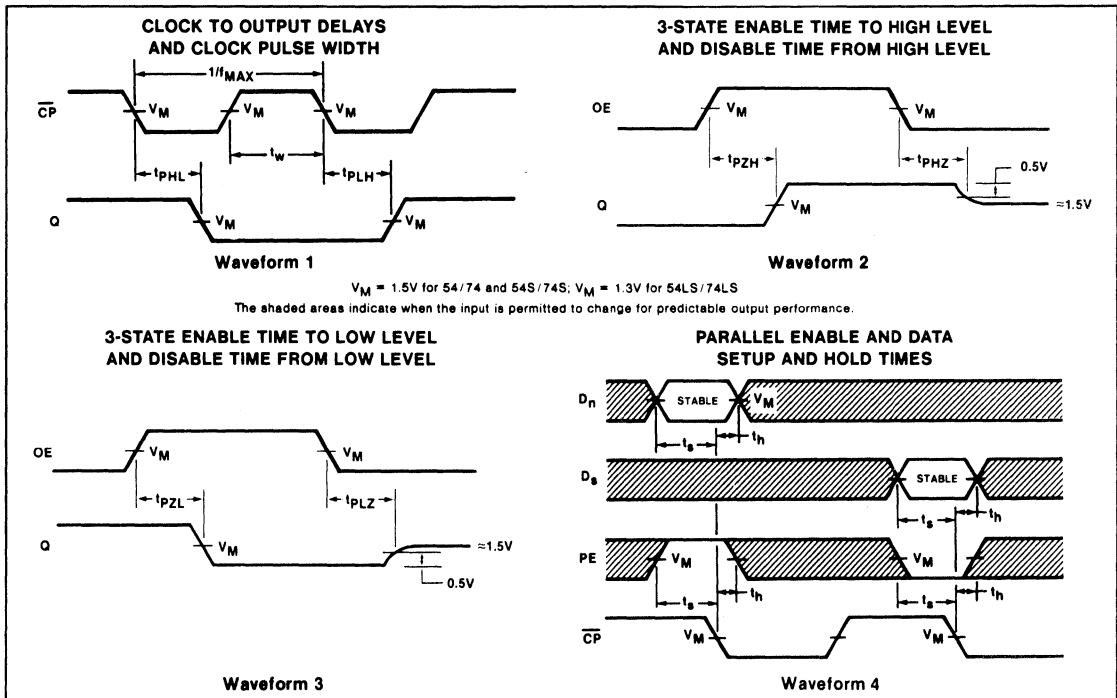
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_W Clock pulse width	Waveform 1	16		ns
t_s Setup time, Data to clock	Waveform 4	20		ns
t_h Hold time, Data to clock	Waveform 4	20		ns
t_s Setup time, PE to clock	Waveform 4	20		ns
t_h Hold time, PE to clock	Waveform 4	10		ns

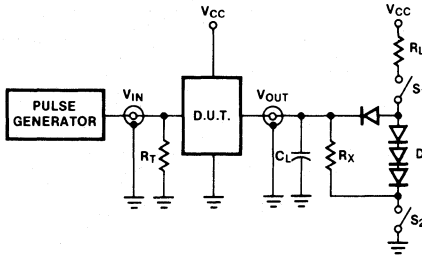
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AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



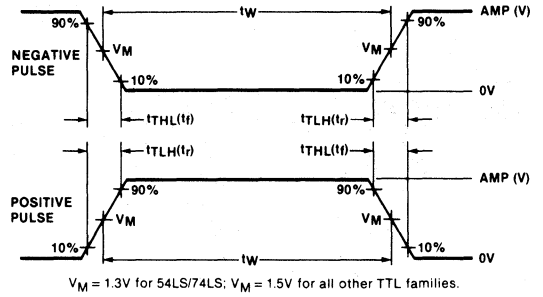
SWITCH POSITION

Test	Switch 1	Switch 2
tPZH	Open	Closed
tPZL	Closed	Open
tPHZ	Closed	Closed
tPLZ	Closed	Closed

DEFINITIONS

RL = Load resistor to VCC; see AC CHARACTERISTICS for value.
 CL = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 RT = Termination resistance should be equal to ZOUT of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 RX = 1kΩ for 54/74, 54S/74S, RX = 5kΩ for 54LS/74LS.
 tTLH, tTHL Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	tTLH	tTHL
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

PORT REGISTERS

54/74298, LS298

Quad 2-Port Register

- Fully synchronous operation
- Select from two data sources
- Buffered, negative edge triggered clock

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74298	19ns	39mA
74LS298	19ns	13mA

DESCRIPTION

This device is a high-speed Quad 2-Port Register. It selects 4 bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input (\overline{CP}). The 4-bit register is fully edge triggered. The Data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74298N • N74LS298N	
Ceramic DIP		S54LS298F
Flatpack		S54LS298W

**MODE SELECT—
FUNCTION TABLE**

OPERATING MODE	INPUTS				OUTPUTS
	\overline{CP}	S	I_0	I_1	Q_n
Load Source "0"	l	l	l	X	L
	l	l	h	X	H
Load Source "1"	l	h	X	l	L
	l	h	X	h	H

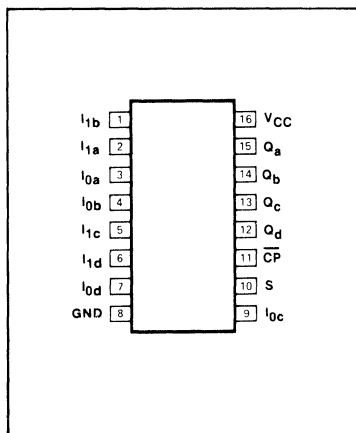
H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.
 X = Don't care
 ↓ = HIGH-to-LOW clock transition.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

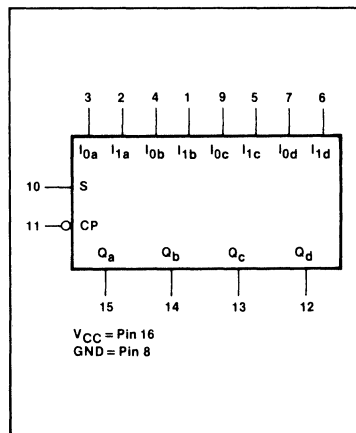
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1uI	1LSuI
All	Outputs	10uI	10LSuI

NOTE
 Where a 54/74 unit load (uI) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, and a 54/74LS unit load (LSuI) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

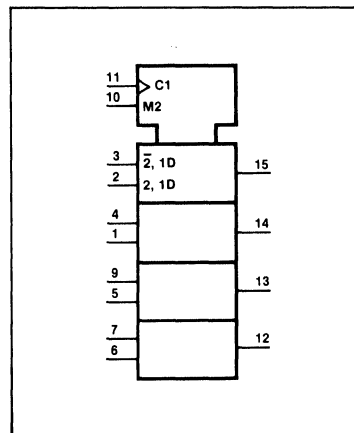
PIN CONFIGURATION



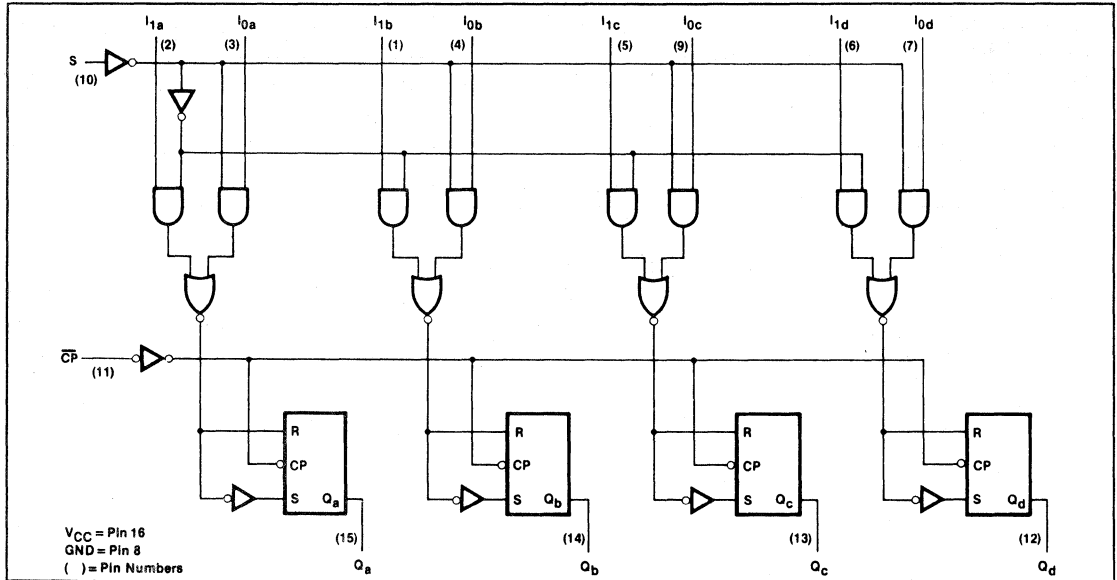
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54	54LS	74	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8			+0.7	V
	Com'l			+0.8			+0.8	V
I_{IK} Input clamp current				-12			-18	mA
I_{OH} HIGH-level output current				-800			-400	μ A
I_{OL} LOW-level output current	Mil			16			4	mA
	Com'l			16			8	mA
T_A Operating free-air temperature	Mil	-55		+125	-55		+125	°C
	Com'l	0		70	0		70	°C

PORT REGISTERS

54/74298, LS298

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74298			54/74LS298			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX I _{OH} = MAX	Mil	2.4	3.4		2.5	3.4	V		
		Com'l	2.4	3.4		2.7	3.4	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX			0.4		0.25	0.4	V	
		I _{OL} = 4mA	Mil			0.4		0.35	0.5	V
			74LS					0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				- 1.5		- 1.5	V		
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0			mA		
		V _I = 7.0V					0.1	mA		
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40			μA		
		V _I = 2.7V					20	μA		
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				- 1.6		- 0.4	mA		
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	- 20		- 57	- 20		- 100	mA	
		Com'l	- 18		- 57	- 20		- 100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			39	65		13	21	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25 °C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured after applying a momentary 4.5V, followed by ground to the Clock input, with all other inputs low and all outputs open.

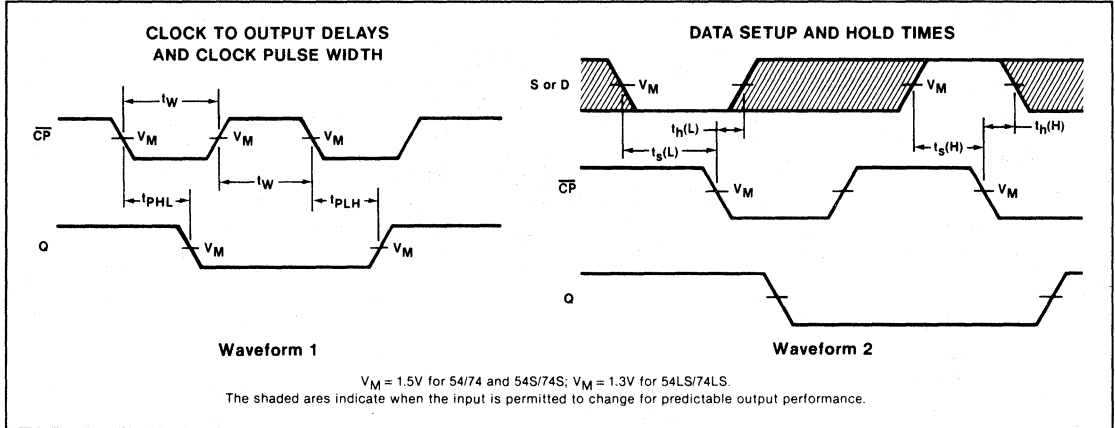
AC CHARACTERISTICS T_A = 25 °C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		
		Min	Max	Min	Max	
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 1		27		27	ns
			32		32	

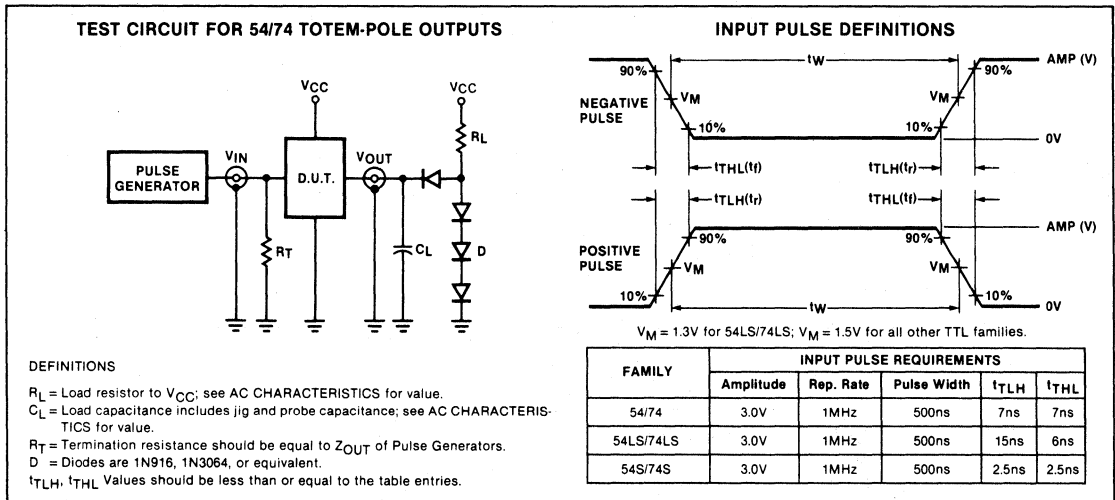
AC SETUP REQUIREMENTS T_A = 25 °C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		Min	Max	Min	Max	
t _w Clock pulse width	Waveform 1	20		20		ns
t _s Setup time, Data to Clock	Waveform 2	15		15		ns
t _h Hold time, Data to Clock	Waveform 2	5		5		ns
t _s Setup time, Select to Clock	Waveform 2	25		25		ns
t _h Hold time, Select to Clock	Waveform 2	0		0		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



SHIFTER

54/74S350

4-Bit Shifter With 3-State Outputs

- Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines
- 3-State outputs for bus organized systems
- Alternate source AM25S10

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S350	7ns	71mA

DESCRIPTION

The '350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.

The '350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical — with logic zeros filled in at either end of the shifting field.
2. Arithmetic — where the sign bit is extended during a shift down.
3. End around — where the data word forms a continuous loop.

The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active LOW Output Enable (\overline{OE}) input controls the state of the outputs. The outputs are in the HIGH impedance "off" state when \overline{OE} is HIGH, and they are active when \overline{OE} is LOW.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S350N	
Ceramic DIP		S54S350F
Flatpack		S54S350W

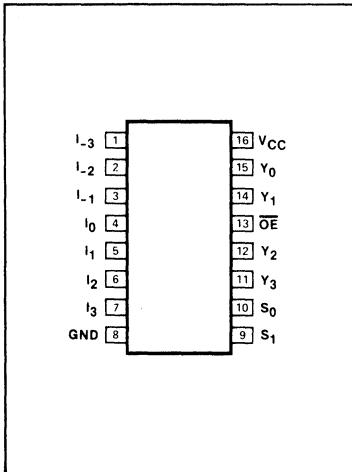
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
All	Outputs	10Sul

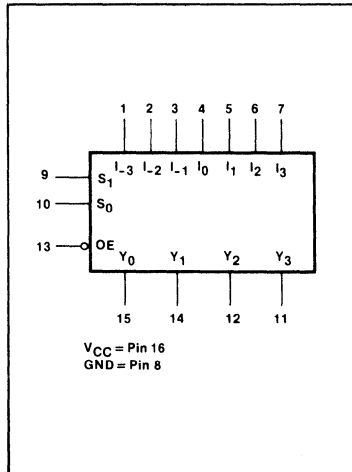
NOTE
A 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} .



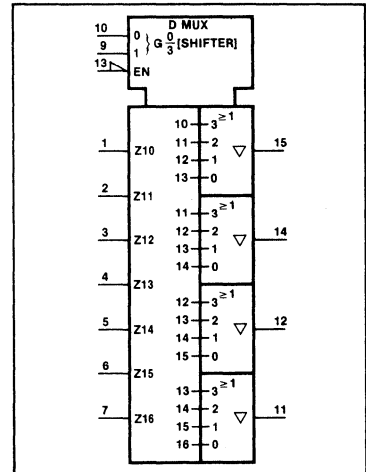
PIN CONFIGURATION



LOGIC SYMBOL



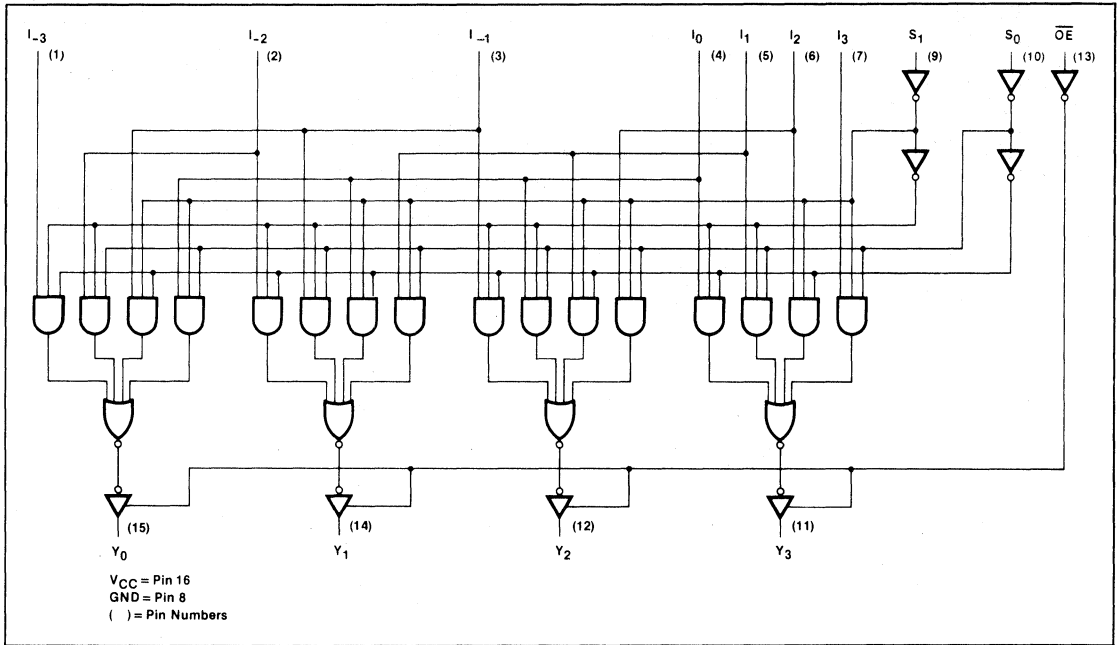
LOGIC SYMBOL (IEEE/IEC)



SHIFTER

54/74S350

LOGIC DIAGRAM



FUNCTION TABLE

OE	S ₁	S ₀	I ₃	I ₂	I ₁	I ₀	I ₋₁	I ₋₂	I ₋₃	Y ₃	Y ₂	Y ₁	Y ₀
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D ₃	D ₂	D ₁	D ₀	X	X	X	D ₃	D ₂	D ₁	D ₀
L	L	H	X	D ₂	D ₁	D ₀	D ₋₁	X	X	D ₂	D ₁	D ₀	D ₋₁
L	H	L	X	X	D ₁	D ₀	D ₋₁	D ₋₂	X	D ₁	D ₀	D ₋₁	D ₋₂
L	H	H	X	X	X	D ₀	D ₋₁	D ₋₂	D ₋₃	D ₀	D ₋₁	D ₋₂	D ₋₃

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state
D_n = HIGH or LOW state of referenced I_n input

LOGIC EQUATIONS

$$\begin{aligned}
 Y_0 &= \bar{S}_0 \cdot \bar{S}_1 \cdot I_0 + S_0 \cdot \bar{S}_1 \cdot I_{-1} + \bar{S}_0 \cdot S_1 \cdot I_{-2} + S_0 \cdot S_1 \cdot I_{-3} \\
 Y_1 &= \bar{S}_0 \cdot \bar{S}_1 \cdot I_1 + S_0 \cdot \bar{S}_1 \cdot I_0 + \bar{S}_0 \cdot S_1 \cdot I_{-1} + S_0 \cdot S_1 \cdot I_{-2} \\
 Y_2 &= \bar{S}_0 \cdot \bar{S}_1 \cdot I_2 + S_0 \cdot \bar{S}_1 \cdot I_1 + \bar{S}_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot I_{-1} \\
 Y_3 &= \bar{S}_0 \cdot \bar{S}_1 \cdot I_3 + S_0 \cdot \bar{S}_1 \cdot I_2 + \bar{S}_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0
 \end{aligned}$$

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I _{IH}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current	Mil			- 2.0	mA
		Com'l			- 6.5	mA
I _{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = + 125°C only.

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74S350			UNIT	
		Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4		V
			Com'l	2.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.5 ⁴	V
			Com'l		0.5	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.2	V
I _{OZH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.4V			50	μA
I _{OZL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _O = 0.5V			-50	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V			1.0	mA
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			50	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.5V			-2.0	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	-40		-100	mA
I _{CC}	Supply current (total)	V _{CC} = MAX, V _{IN} = 0V		71	85	mA

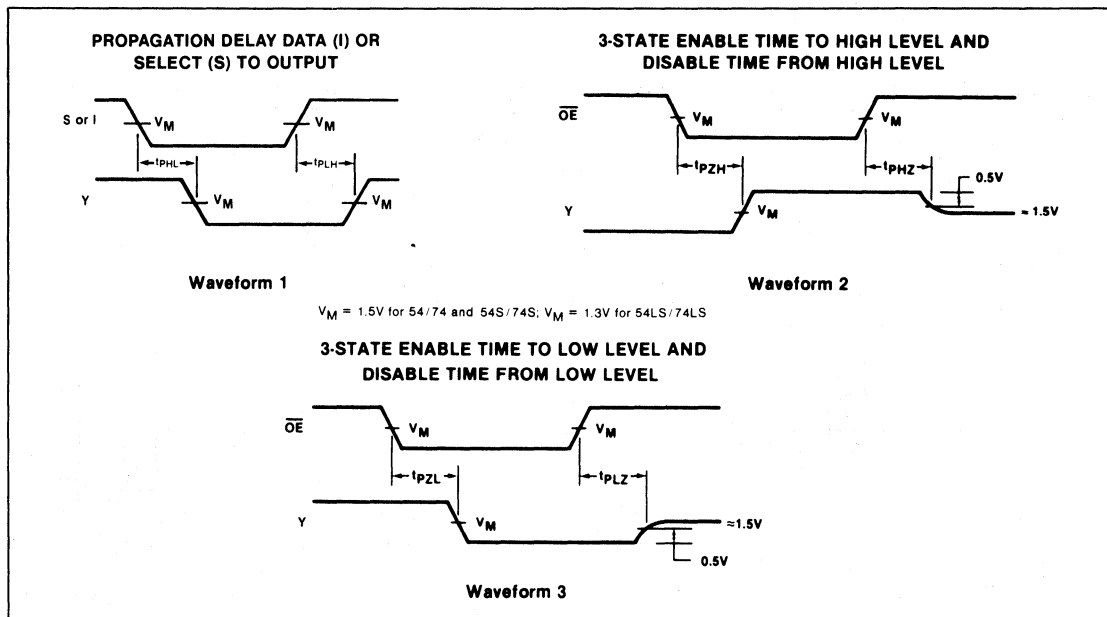
NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

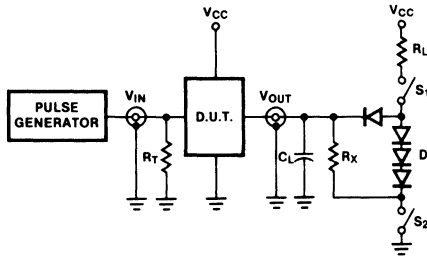
PARAMETER	TEST CONDITIONS	54S/74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		
t_{PZH}	Enable time to HIGH level	Waveform 2		ns
t_{PZL}	Enable time to LOW level	Waveform 3		ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, $C_L = 5\text{pF}$		ns
t_{PLZ}	Disable time from LOW level	Waveform 3, $C_L = 5\text{pF}$		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



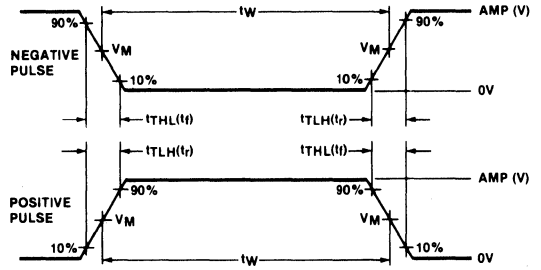
SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

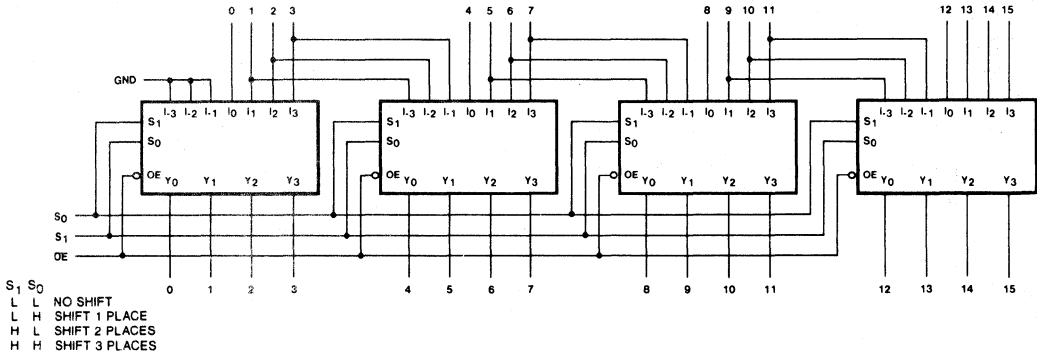


V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

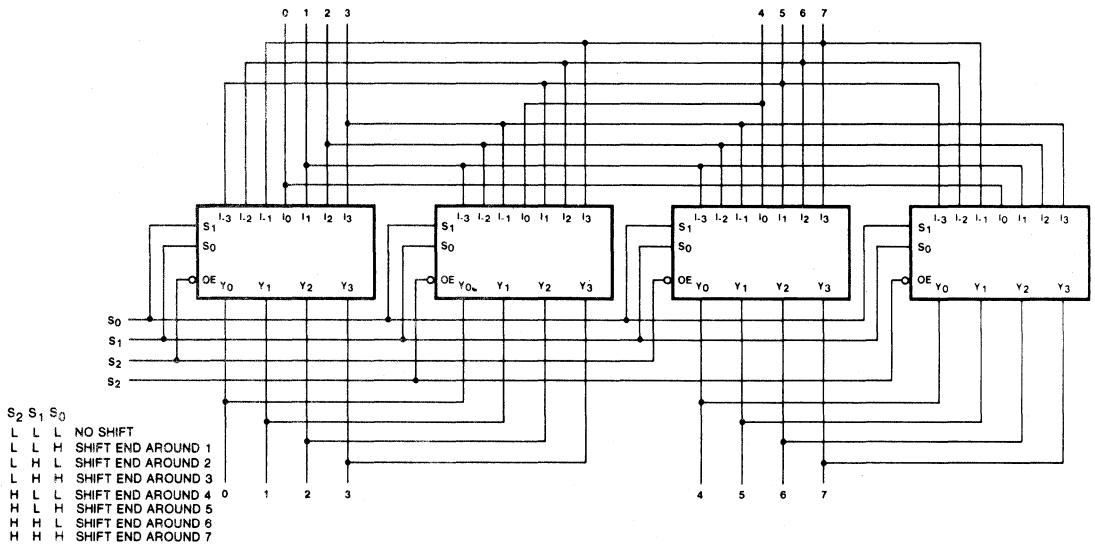
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

APPLICATIONS

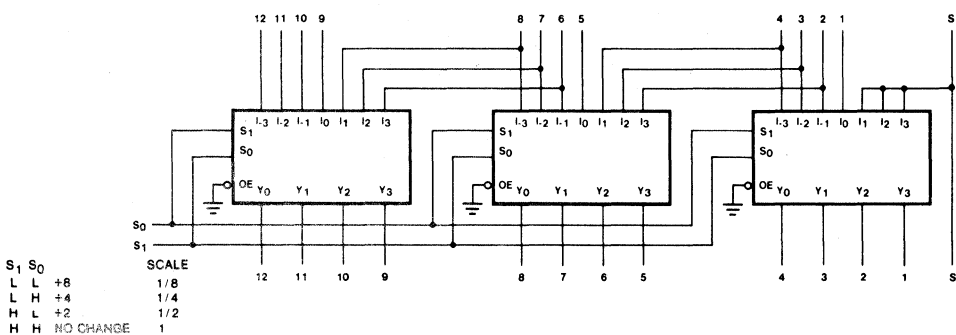
16-BIT SHIFT-UP 0, 1, 2, OR 3 PLACES



8-BIT END AROUND SHIFT 0, 1, 2, 3, 4, 5, 6, 7 PLACES



13-BIT 2's COMPLEMENT SCALER



MULTIPLEXER

54/74LS352

Dual 4-Line To 1-Line Multiplexer

- Inverting version of 'LS153
- Separate Enable for each section
- Common Select inputs
- See 'LS353 for 3-State version

DESCRIPTION

The 'LS352 is a dual 4-input multiplexer that can select 2 bits of data from up to eight sources under control of the common Select inputs (S₀, S₁). The two 4-input multiplexer circuits have individual active LOW Enables (\bar{E}_a , \bar{E}_b) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced HIGH when the corresponding Enables (\bar{E}_a , \bar{E}_b) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Y_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS352	15ns	6.2mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{CC} = 5V ± 5%; T _A = 0°C to +70°C	MILITARY RANGES V _{CC} = 5V ± 10%; T _A = -55°C to +125°C
Plastic DIP	N74LS352N	
Ceramic DIP		S54LS352F
Flatpack		S54LS352W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

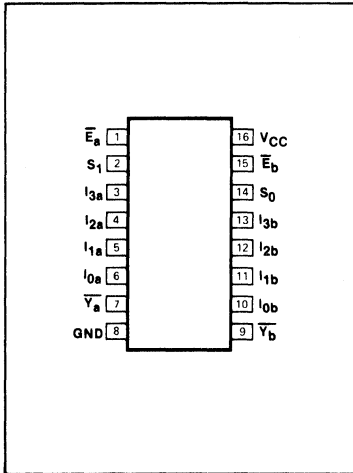
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	10LSul

Note:
Where a 54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL}.

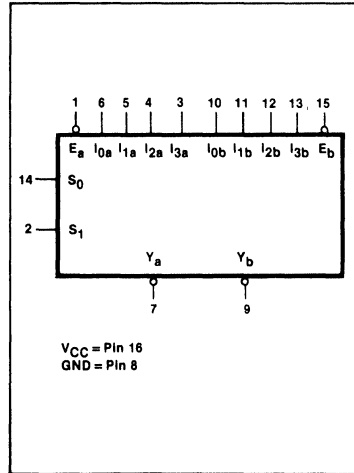
The 'LS352 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The de-

vice can generate two functions or three variables. This is useful for implementing highly irregular random logic.

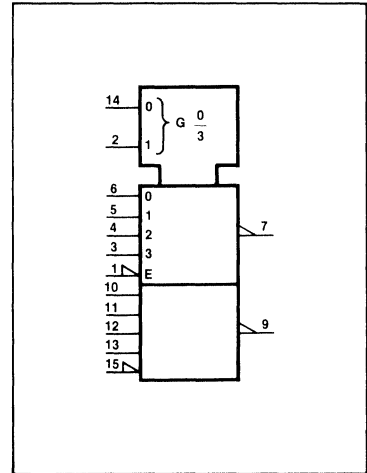
PIN CONFIGURATION



LOGIC SYMBOL



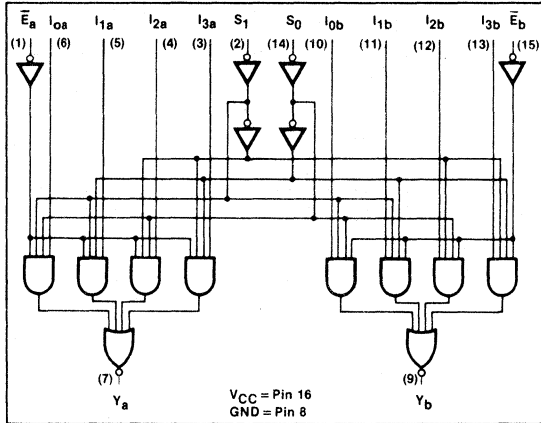
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER

54/74LS352

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		INPUTS (a or b)				OUTPUT	
S ₀	S ₁	\bar{E}	I ₀	I ₁	I ₂	I ₃	Y
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to +7.0	- 0.5 to +7.0	V
I _{IN} Input current	- 30 to +1	- 30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to +V _{CC}	- 0.5 to +V _{CC}	V
T _A Operating free-air temperature range	- 55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT
		Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+ 0.7	V
	Com'l			+ 0.8	V
I _{IK} Input clamp current				- 18	mA
I _{OH} HIGH-level output current				- 400	μA
I _{OL} LOW-level output current	Mil			4	mA
	Com'l			8	mA
T _A Operating free-air temperature	Mil	- 55		+ 125	°C
	Com'l	0		70	°C

MULTIPLEXER

54/74LS352

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS352			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V	
		Com'l	2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
		I _{OL} = 4mA	74LS	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V		0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.7V		20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V		-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Mil	-20	-100	mA	
		Com'l	-20	-100	mA	
I _{CC} L Supply current (total)	V _{CC} = MAX	Mil		6.2	10	mA
		Com'l		6.2	10	mA

4

- NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 2. All typical values are at V_{CC} = 5V, T_A = 25°C.
 3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

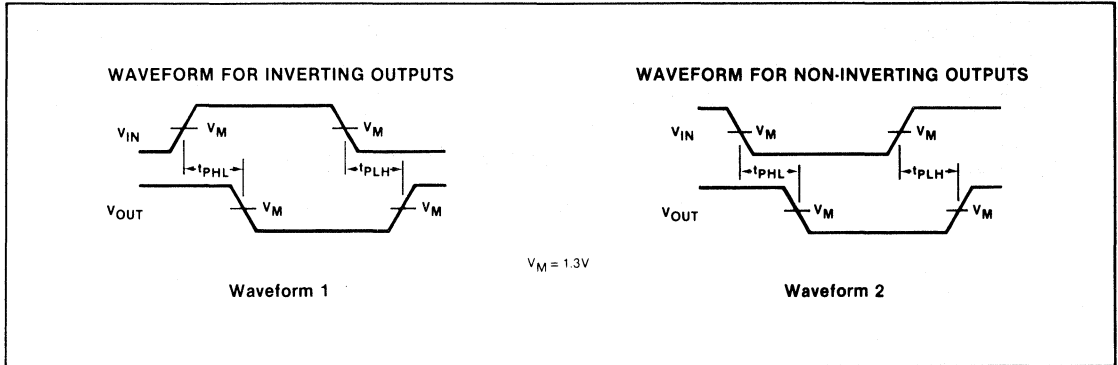
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay Select to output	Waveform 1 or 2		29 38	ns
t _{PLH} t _{PHL} Propagation delay Enable to output			24 32	
t _{PLH} t _{PHL} Propagation delay Data to output	Waveform 1		20 26	ns

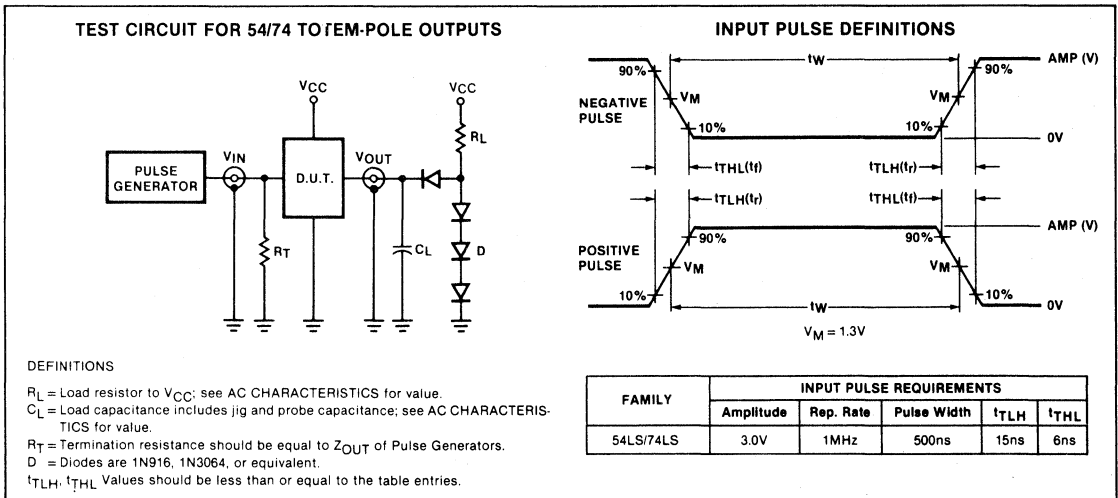
MULTIPLEXER

54/74LS352

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



MULTIPLEXER

54/74LS353

Dual 4-Input Multiplexer (3-State)

- Inverting version of 'LS253
- 3-State outputs for bus interface and multiplex expansion
- Common Select inputs
- Separate Output Enable inputs

TYPE	TYPICAL PROPAGATION DELAY (From Data)	TYPICAL SUPPLY CURRENT (Total)
74LS353	12ns	8mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74LS353N	
Ceramic DIP		S54LS353F
Flatpack		S54LS353W

DESCRIPTION

The 'LS353 has two identical 4-input multiplexers with 3-State outputs which select two bits from eight sources selected by common Select inputs (S_0, S_1). When the individual Output Enable (E_{0a}, E_{0b}) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

The 'LS353 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$Y_a = \overline{OE_a} \cdot (I_{0a} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1a} \cdot \overline{S_1} \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S_0} + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{OE_b} \cdot (I_{0b} \cdot \overline{S_1} \cdot \overline{S_0} + I_{1b} \cdot \overline{S_1} \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S_0} + I_{3b} \cdot S_1 \cdot S_0)$$

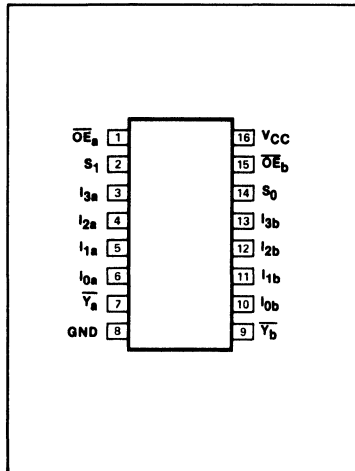
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	10LSul

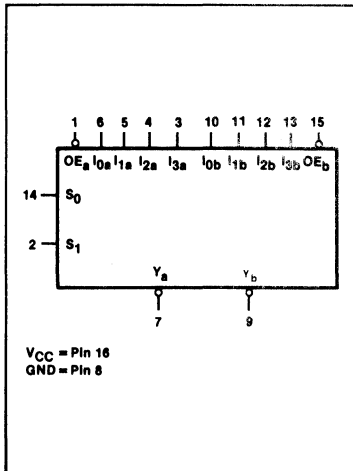
Note:
54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL} .

All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

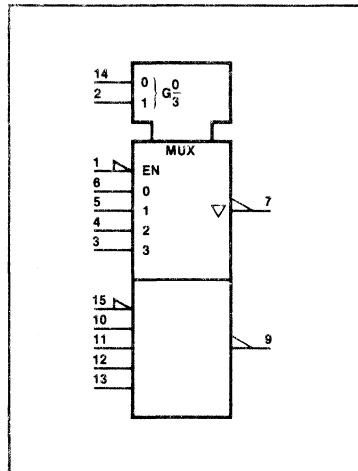
PIN CONFIGURATION



LOGIC SYMBOL



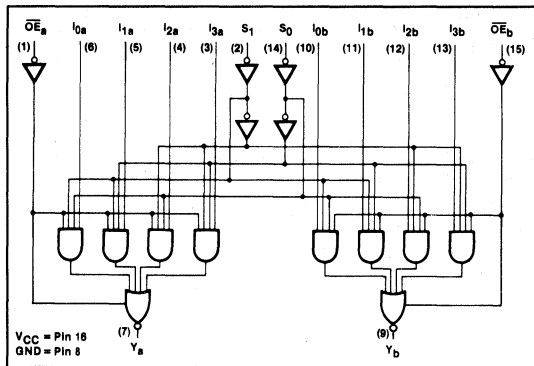
LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER

54/74LS353

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	\overline{OE}	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0		V	
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current			-18	mA	
I_{OH}	HIGH-level output current	Mil			-1.0	mA
		Com'l			-2.6	mA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	-55		+125	°C
		Com'l	0		70	°C

MULTIPLEXER

54/74LS353

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS353			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4	V	
		Com'l	2.4	3.1	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
		I _{OL} = 4mA	74LS	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _{ozH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.7V		20	μA	
I _{ozL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V		-20	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V		0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V		-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX			-15	-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		7	12	mA
		Condition 2		8.5	14	mA

NOTES

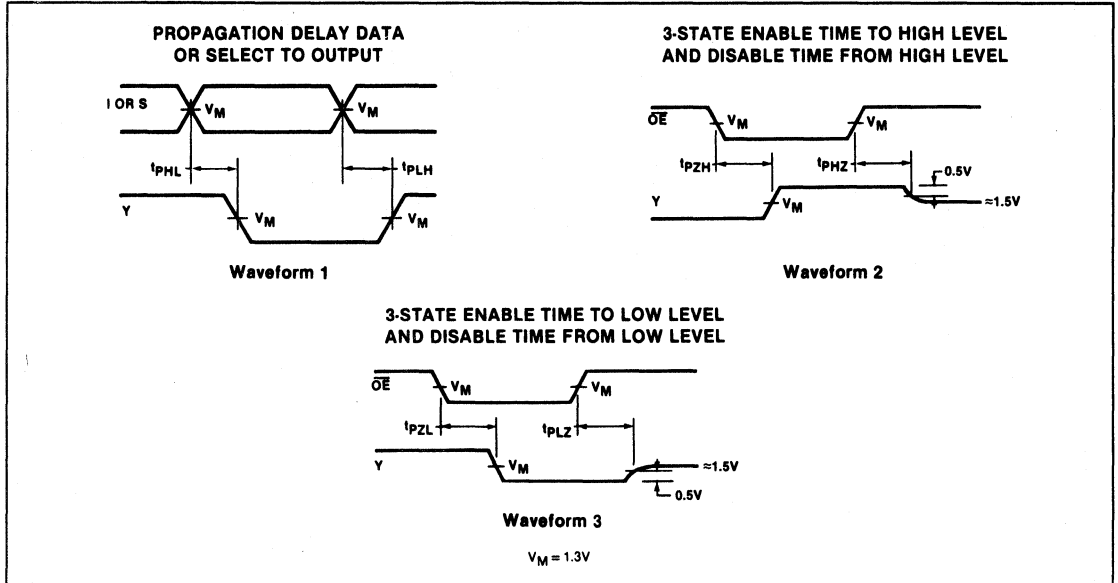
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured under the following conditions with the outputs open: *Condition 1*: All inputs grounded. *Condition 2*: \overline{OE} at 4.5V, all inputs grounded.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

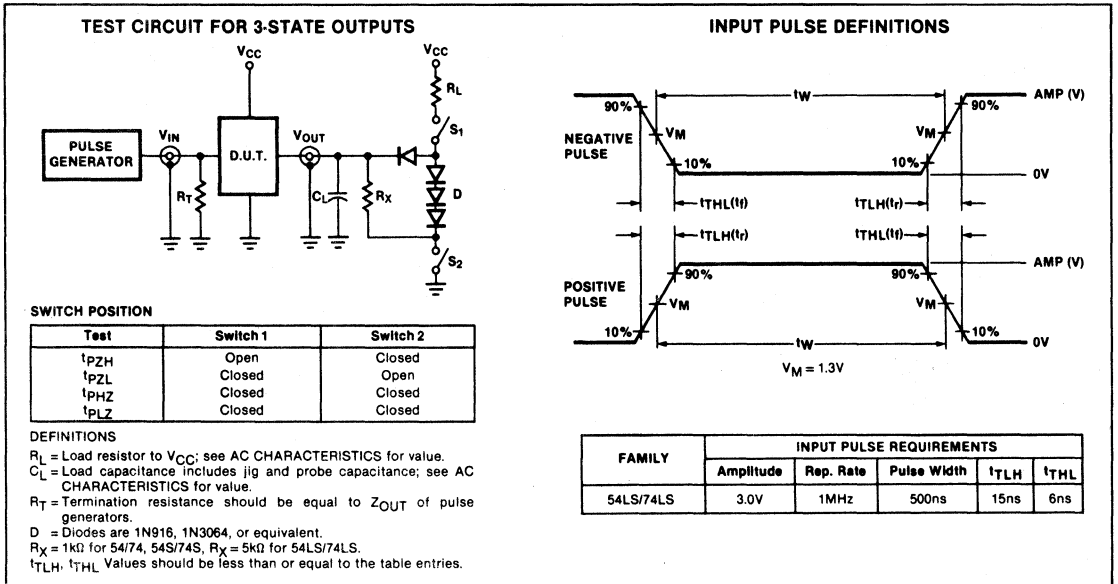
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} t _{PHL} Propagation delay Data to output	Waveform 1	25	20	ns
t _{PLH} t _{PHL} Propagation delay Select to output	Waveform 1	45	32	ns
t _{PZH} Output enable to HIGH level	Waveform 2	23		ns
t _{PZL} Output enable to LOW level	Waveform 3	23		ns
t _{PHZ} Output disable from HIGH level	Waveform 2, C _L = 5pF	41		ns
t _{PLZ} Output disable from LOW level	Waveform 3, C _L = 5pF	27		ns

4

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



LATCH

54/74LS363

Octal Transparent Latch With 3-State Outputs

- 8-bit transparent latch
- 3-State MOS compatible output buffers
- Common Latch Enable input with hysteresis
- Common 3-state Output Enable control
- Independent latch and 3-state buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS363	19ns	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS363N	
Ceramic DIP	S54LS363F	
LLCC	S54LS363G	

DESCRIPTION

The '363 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs is transferred to the Latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the Data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about 1V closer to V_{CC} , or to over 3.5V at minimum V_{CC} . This feature makes these

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

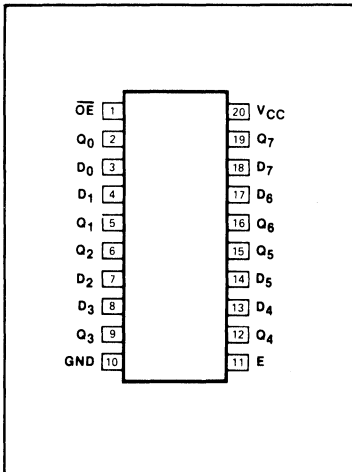
NOTE
A 54/74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V.

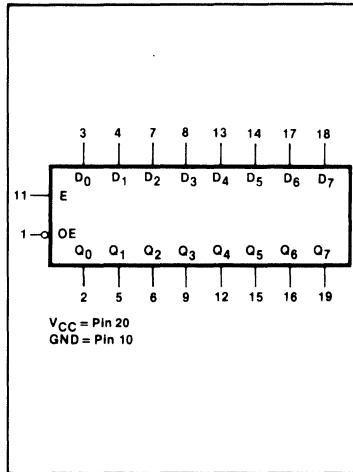
The active LOW Output Enable (\overline{OE}) controls all eight 3-state buffers independent

of the latch operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

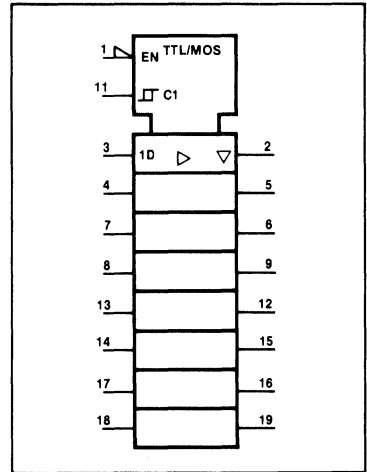
PIN CONFIGURATION



LOGIC SYMBOL



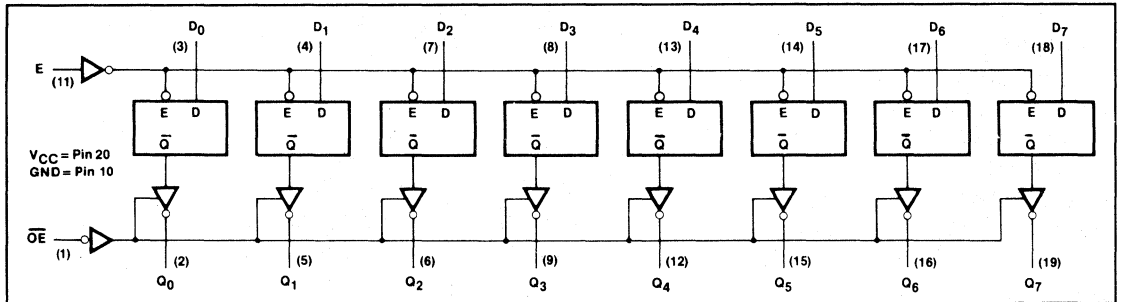
LOGIC SYMBOL (IEEE/IEC)



LATCH

54/74LS363

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS Q ₀ -Q ₇
	\overline{OE}	E	D _n		
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW enable transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
 (Z) = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT		
		Min	Nom	Max			
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	V	
V _{IH}	HIGH-level input voltage	2.0			V		
V _{IL}	LOW-level input voltage	Mil			+0.7	V	
		Com'l			+0.8	V	
I _{IH}	Input clamp current				-18	mA	
I _{OH}	HIGH-level output current	Mil			-1.0	mA	
		Com'l			-2.6	mA	
I _{OL}	LOW-level output current	Mil			12	mA	
		Com'l			24	mA	
T _A	Operating free-air temperature	Mil	-55			+125	°C
		Com'l	0			70	°C

LATCH

54/74LS363

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74LS363			UNIT	
			Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		Mil	3.45		V	
			Com'l	3.65		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX		I _{OL} = MAX		0.25	0.4	V
				Com'l	0.35	0.5	V
			I _{OL} = 12mA	74LS	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IL} = MAX, V _O = 3.65V				20	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 0.4V				-20	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-30		-130	mA	
I _{CC} Supply current (total)	V _{CC} = MAX, \overline{OE} = 4.5V			42	70	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_O = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

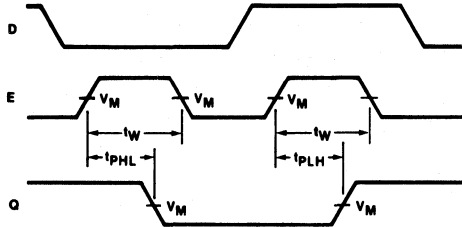
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT	
		C _L = 45pF, R _L = 667Ω			
		Min	Max		
t _{PLH} t _{PHL}	Propagation delay Latch Enable to output	Waveform 1		30 36	ns
t _{PLH} t _{PHL}	Propagation delay Data to output	Waveform 4		23 27	ns
t _{PZH}	Enable time to HIGH level	Waveform 2		28	ns
t _{PZL}	Enable time to LOW level	Waveform 3		36	ns
t _{PHZ}	Disable time from HIGH level	Waveform 2, C _L = 5pF		20	ns
t _{PLZ}	Disable time from LOW level	Waveform 3, C _L = 5pF		25	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t _W	Latch Enable pulse width	Waveform 1	15	ns
t _S	Setup time, Data to Latch Enable	Waveform 5	0	ns
t _H	Hold time, Data to Latch Enable	Waveform 5	10	ns

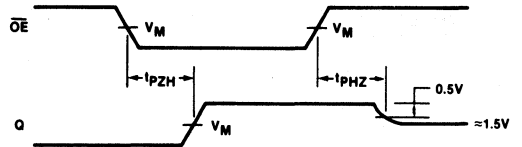
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



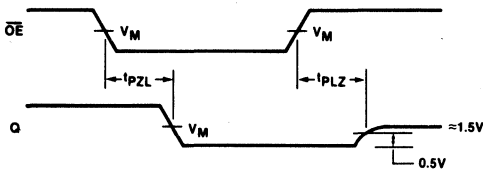
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



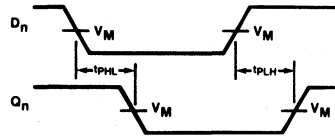
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



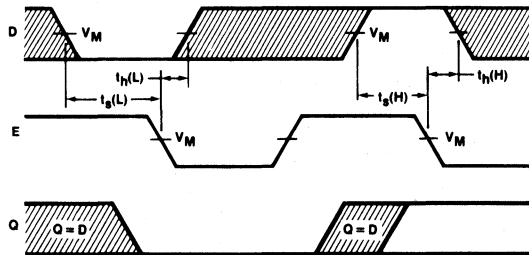
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



Waveform 4

DATA SETUP AND HOLD TIMES



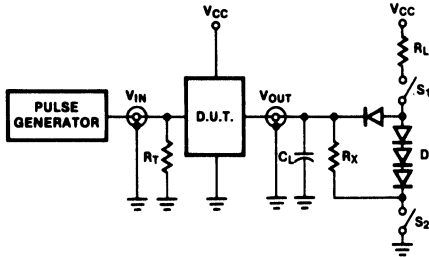
Waveform 5

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



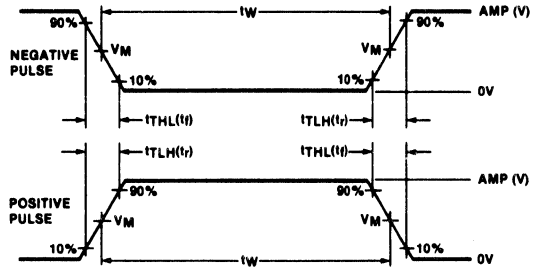
SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOP

54/74LS364

Octal D Flip-Flop With 3-State Outputs

- 8-bit positive edge-triggered register
- 3-State MOS compatible output buffers
- Common Clock input with hysteresis
- Common 3-state Output Enable control
- Independent register and 3-state buffer operation

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS364	50MHz	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS364N	
Ceramic DIP		S54LS364F
LLCC		S54LS364G

DESCRIPTION

The '364 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

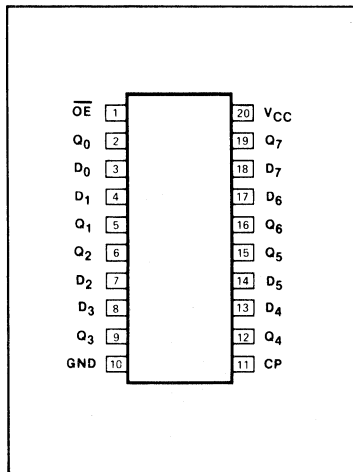
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

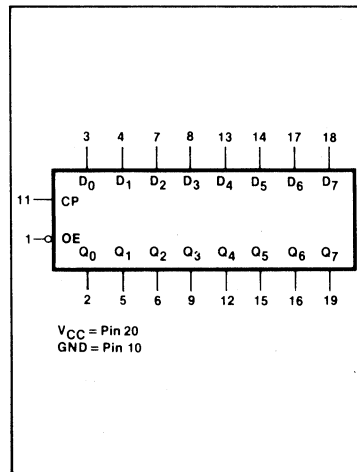
1V closer to V_{CC} , or to over 3.5V at minimum V_{CC} . This feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V. The active LOW Output Enable (\overline{OE}) controls all eight 3-state buffers inde-

pendent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

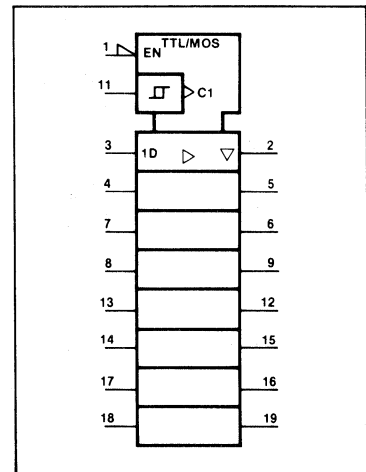
PIN CONFIGURATION



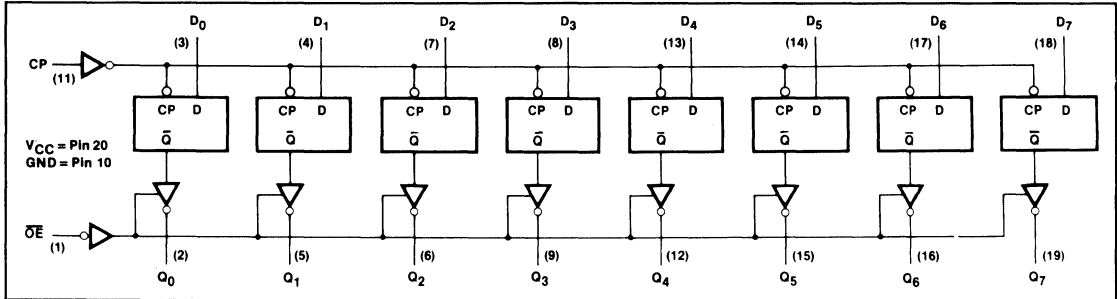
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		Q_0-Q_7
Load and read register	L	l	l	L	L
	L	l	h	H	H
Latch register and disable outputs	H	l	l	L	(Z)
	H	l	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 (Z) = HIGH impedance "off" state
 l = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I_{IN} Input current	-30 to +1	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT
		Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			V
V_{IL} LOW-level input voltage	Mil			+0.7	V
	Com'l			+0.8	V
I_{IH} Input clamp current				-18	mA
I_{OH} HIGH-level output current	Mil			-1.0	mA
	Com'l			-2.6	mA
I_{OL} LOW-level output current	Mil			12	mA
	Com'l			24	mA
T_A Operating free-air temperature	Mil	-55		+125	°C
	Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS364			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Min	3.45		V	
		Com ¹	3.65		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Min	0.25	0.4	V
			Com ¹	0.35	0.5	V
		I _{OL} = 12mA	74LS	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IL} = MAX, V _O = 3.65V			20	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 0.4V			-20	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-30		-130	mA	
I _{CC} Supply current (total)	V _{CC} = MAX, \overline{OE} = 4.5V		42	70	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 45pF, R _L = 667Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	35		MHz
t _{PLH} Propagation delay	Waveform 1		33	ns
t _{PHL} Clock to output			34	
t _{PZH} Enable time to HIGH level	Waveform 2		28	ns
t _{PZL} Enable time to LOW level	Waveform 3		36	ns
t _{PHZ} Disable time from HIGH level	Waveform 2, C _L = 5pF		18	ns
t _{PLZ} Disable time from LOW level	Waveform 3, C _L = 5pF		24	ns

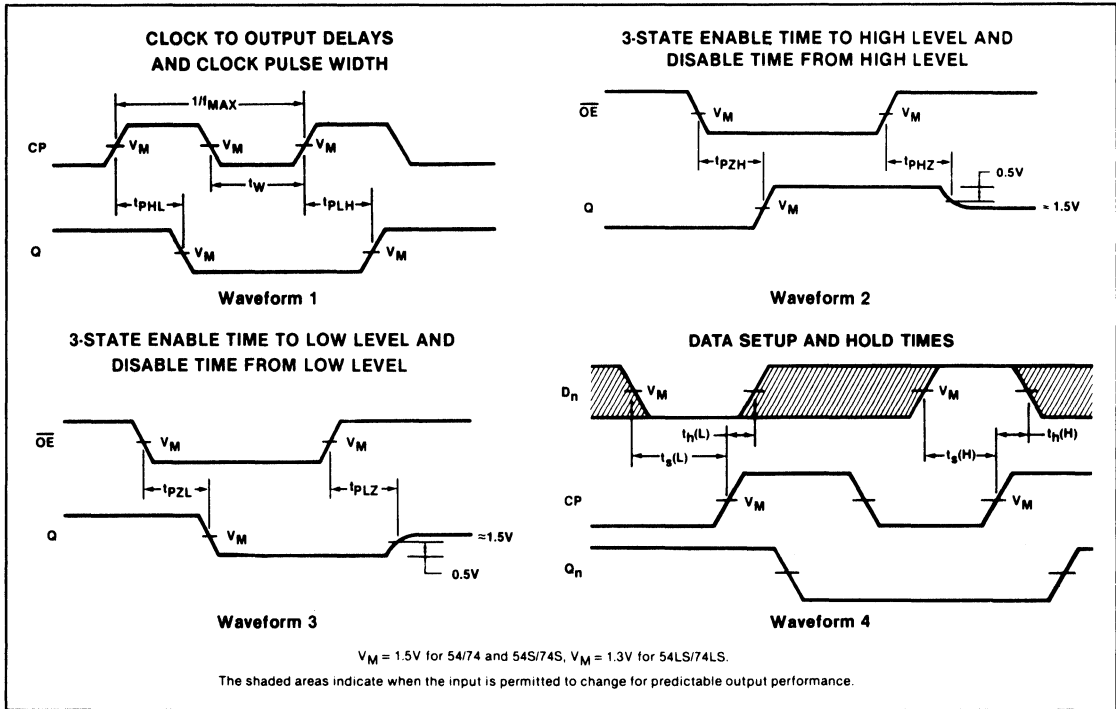
NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

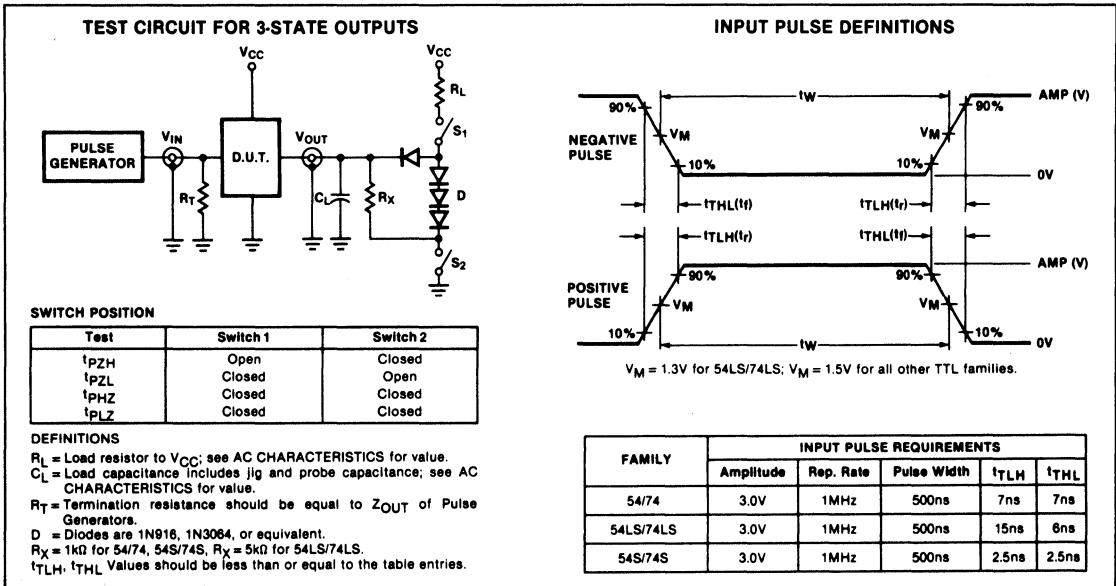
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t _w Clock pulse width	Waveform 1	15		ns
t _s Setup time, Data to clock	Waveform 4	20		ns
t _h Hold time, Data to clock	Waveform 4	0		ns

AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS



**'365A, '367A Hex Buffer/Driver (3-State)
'366A, '368A Hex Inverter Buffer (3-State)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74365A, 367A	10ns	65mA
74LS365A, 367A	10ns	14mA
74366A, 368A	9ns	59mA
74LS366A, 368A	10ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to +70°C	V _{CC} = 5V ± 10%; T _A = -55°C to +125°C
Plastic DIP	N74365AN • N74LS365AN N74366AN • N74LS366AN N74367AN • N74LS367AN N74368AN • N74LS368AN	
Plastic SO	N74LS365AD • N74LS367AD N74LS368AD	
Ceramic DIP		S54365AF • S54LS365AF S54366AF • S54LS366AF S54367AF • S54LS367AF S54368AF • S54LS368AF
Flatpack		S54365AW • S54LS365AW S54366AW • S54LS366AW S54367AW • S54LS367AW S54368AW • S54LS368AW
LLCC		S54LS365AG S54LS367AG

FUNCTION TABLE, '365A, '366A

INPUTS			OUTPUTS	
\overline{OE}_1	\overline{OE}_2	I	Y	\overline{Y}
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

FUNCTION TABLE, '367A, '368A

INPUTS		OUTPUTS	
\overline{OE}	I	Y	\overline{Y}
L	L	L	H
L	H	H	L
H	X	(Z)	(Z)

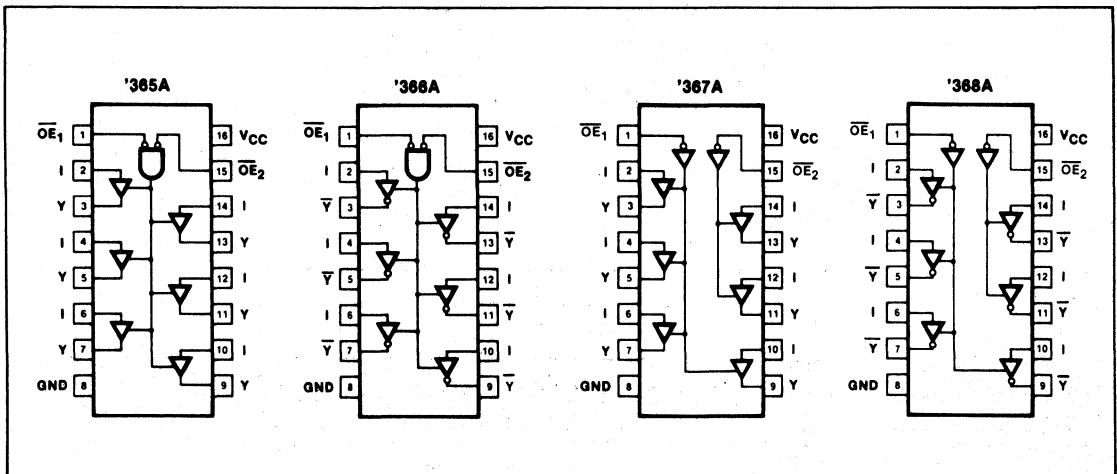
L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1uI	1LSuI
All	Outputs	20uI	30LSuI

NOTE
Where a 54/74 unit load (uI) is understood to be 40µA I_{IH} and -1.6mA I_{IL} and a 54/74LS unit load (LSuI) is 20µA I_{IH} and -0.4mA I_{IL}.

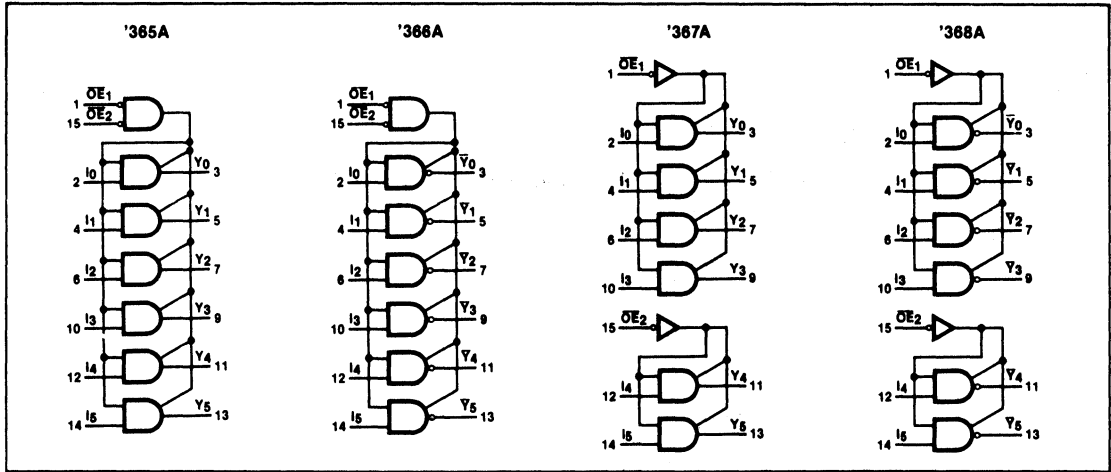
PIN CONFIGURATION



BUFFERS/DRIVERS

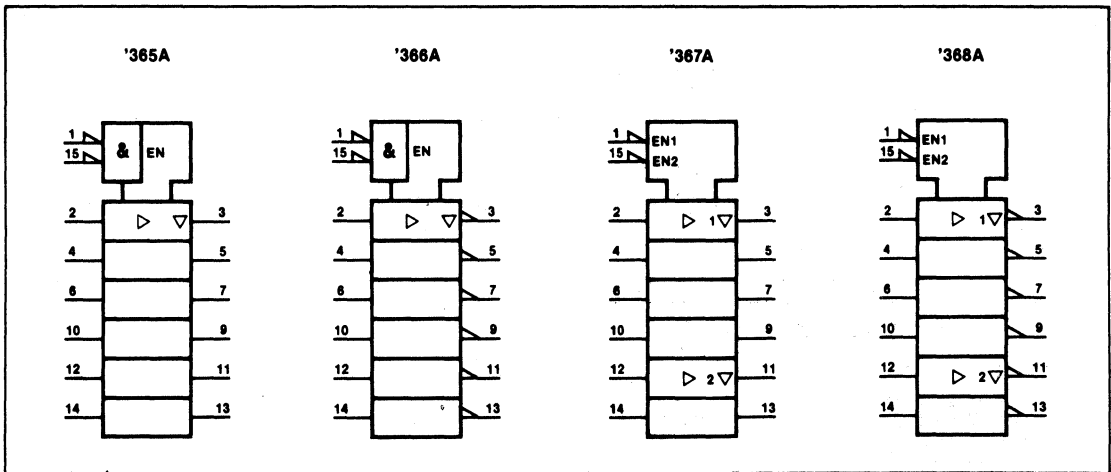
54/74365A, 366A, 367A, 368A, LS365A, LS366A, LS367A, LS368A

LOGIC SYMBOL



4

LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

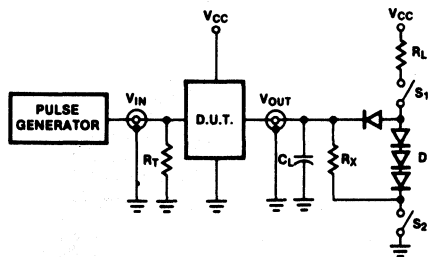
PARAMETER	54	54LS	74	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	V
I _{IN} Input current	-30 to +5	-30 to +1	-30 to +5	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74			54/74LS			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Min	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			V	
V _{IL}	LOW-level input voltage	Min		+ 0.8			+ 0.7	V	
		Com'l		+ 0.8			+ 0.8	V	
I _{IK}	Input clamp current			- 12			- 18	mA	
I _{OH}	HIGH-level output current	Min		- 2.0			- 1.0	mA	
		Com'l		- 5.2			- 2.6	mA	
I _{OL}	LOW-level output current	Min		32			12	mA	
		Com'l		32			24	mA	
T _A	Operating free-air temperature	Min	- 55	+ 125	- 55		+ 125	°C	
		Com'l	0	70	0		70	°C	

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



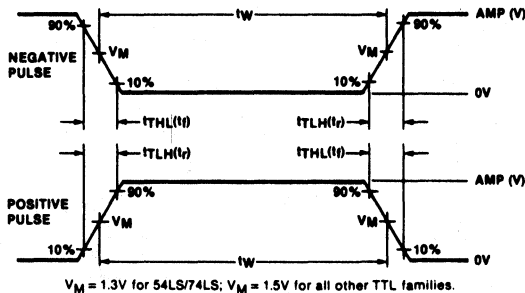
SWITCH POSITION

Test	Switch 1	Switch 2
I _{PZH}	Open	Closed
I _{PZL}	Closed	Open
I _{PHZ}	Closed	Closed
I _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS/DRIVERS

54/74365A, 366A, 367A, 368A, LS365A, LS366A, LS367A, LS368A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74365A, '366A, '367A, '368A			54/74LS365A, '366A, '367A, '368A			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		MII	2.4	3.3		2.4	3.3	V
			Com'I	2.4	3.1		2.4	3.1	V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	MII		0.4		0.25	0.4	V
			Com'I			0.4	0.35	0.5	V
		I _{OL} = 12mA	74LS				0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 2.4V				40			20	μA
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _{IL} = MAX, V _O = 0.4V				-40			-20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0				mA
		V _I = 7.0V						0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V			40				μA
		V _I = 2.7V						20	μA
I _{IL} LOW-level input current	V _{CC} = MAX	I inputs, V _I = 0.5V Either \overline{OE} input at 2.0V Does not apply to 'LS365A or 'LS367A			-40			-20	μA
		I inputs V _I = 0.4V Both \overline{OE} inputs at 0.4V			-1.6			-0.4	mA
		\overline{OE} inputs V _I = 0.4V			-1.6			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-40		-130	-30		-130	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	'365A, '367A		65	85		14	24	mA
		'366A, '368A		59	77		12	21	mA

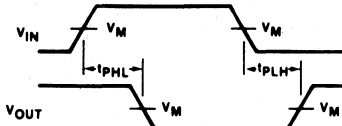
- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with Data inputs grounded and Output Enable inputs at 4.5V.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C _L = 50pF, R _L = 400Ω		C _L = 45pF, R _L = 667Ω		
		Min	Max	Min	Max	
t _{PLH} t _{PHL} Propagation delay	Waveform 1, '366A, '368A		17 16		15 18	ns
t _{PLH} t _{PHL} Propagation delay	Waveform 2, '365A, '367A		16 22		16 22	ns
t _{PZH} Enable to HIGH	Waveform 3		35		35	ns
t _{PZL} Enable to LOW	Waveform 4	'365A, '367A	37		40	ns
		'366A, '368A	37		45	ns
t _{PHZ} Disable from HIGH	Waveform 3, C _L = 5pF	'365A, '367A	11		30	ns
		'366A, '368A	11		32	ns
t _{PLZ} Disable from LOW	Waveform 4, C _L = 5pF		27		35	ns

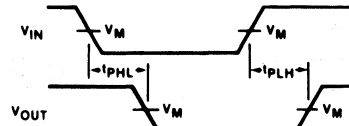
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



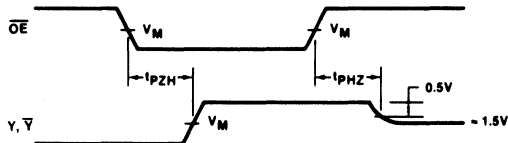
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



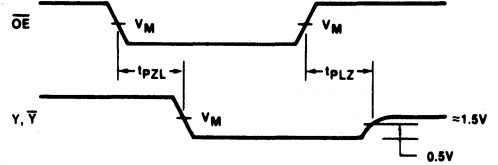
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

$V_M = 1.3V$ for 54LS/74LS, $V_M = 1.5V$ for all other TTL families.

LATCHES/FLIP-FLOPS

54/74LS373, 54/74LS374, S373, S374

**'373 Octal Transparent Latch With 3-State Outputs
'374 Octal D Flip-Flop With 3-State Outputs**

- 8-bit transparent latch — '373
- 8-bit positive, edge-triggered register — '374
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS373	19ns	24mA
74S373	10ns	105mA
74LS374	19ns	27mA
74S374	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = -55°C to + 125°C
Plastic DIP	N74LS373N • N74S373N N74LS374N • N74S374N	
Plastic SO	N74LS373D • N74S373D N74LS374D • N74S374D	
Ceramic DIP		S54LS373F • S54S373F S54LS374F • S54S374F
LLCC		S54S374G S54LS373G • S54LS374G

DESCRIPTION

The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

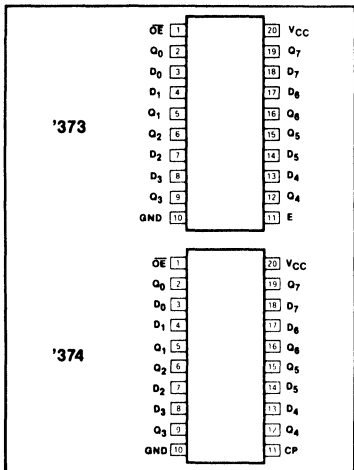
NOTE
Where a 54/74S unit load (Sul) is 50 μ A I_{IH} and - 2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20 μ A I_{IH} and - 0.4mA I_{IL}.

are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

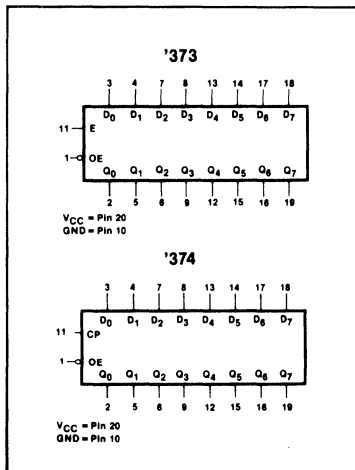
The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

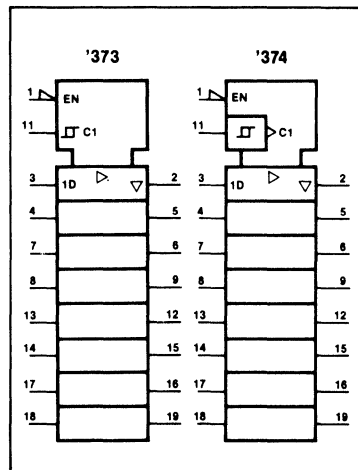
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LATCHES/FLIP-FLOPS

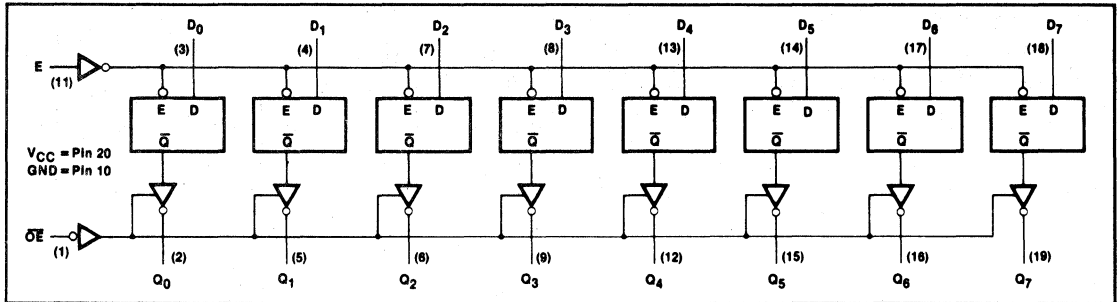
54/74LS373, 54/74LS374, S373, S374

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls

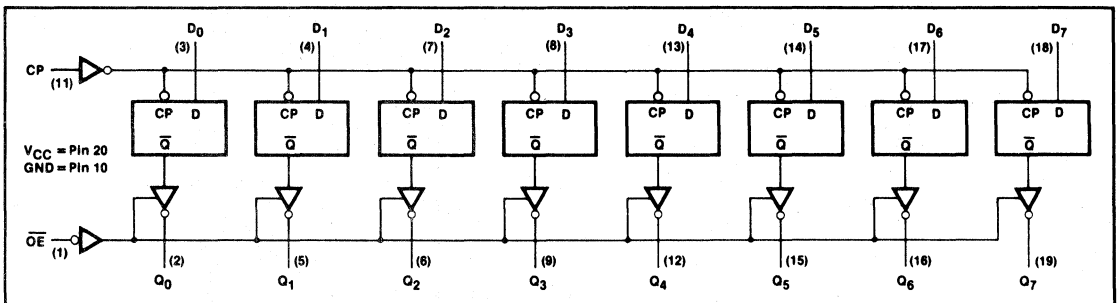
all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in

the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



MODE SELECT—FUNCTION TABLE, '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	E	D_n		Q_0-Q_7
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

MODE SELECT—FUNCTION TABLE, '374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		Q_0-Q_7
Load and read register	L	l	l	L	L
	L	l	h	H	H
Load register and disable outputs	H	l	l	L	(Z)
	H	l	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW \overline{OE} transition
 L = LOW voltage level

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW \overline{OE} transition
 (Z) = HIGH impedance "off" state
 1 = LOW-to-HIGH clock transition

LATCHES/FLIP-FLOPS

54/74LS373, 54/74LS374, S373, S374

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT	
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V	
V_{IN}	Input voltage	-0.5 to +7.0	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V	
I_{IN}	Input current	-30 to +1	-30 to +5	-30 to +1	-30 to +5	mA	
V_{OUT}	Voltage applied to output in HIGH output state.	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V	
T_A	Operating free-air temperature range	-55 to +125			0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			54/74S			UNIT	
		Min	Nom	Max	Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			V	
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA	
I_{OH}	HIGH-level output current	Mil			-1.0			-2.0	mA
		Com'l			-2.6			-6.5	mA
I_{OL}	LOW-level output current	Mil			12			20	mA
		Com'l			24			20	mA
T_A	Operating free-air temperature	Mil	-55		+125	-55		+125	°C
		Com'l	0		70	0		70	°C

NOTE

$V_{IL} = +0.7V$ MAX for 54S at $T_A = +125^\circ C$ only.

LATCHES/FLIP-FLOPS

54/74LS373, 54/74LS374, S373, S374

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS373, 374			54/74S373, 374			UNIT		
		Min	Typ ²	Max	Min	Typ ²	Max			
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4		2.4	3.0	V		
		Com'l	2.4	3.1		2.4	3.1	V		
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.25	0.4			0.5 ⁴	V	
		I _{OL} = 12mA	Mil		0.35	0.5			0.5	V
			74LS		0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.2	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.7V			20				μA	
		V _O = 2.4V						50	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.4V			-20				μA	
		V _O = 0.5V						-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V			0.1				mA	
		V _I = 5.5V						1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				20			50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V			-0.4				mA	
		V _I = 0.5V						-0.25	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-30		-130	-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCZ} \overline{OE} = 4.5V 'LS373		24	40				mA	
		I _{CCL} \overline{OE} = 0V 'S373					105	160	mA	
		I _{CCZ} \overline{OE} = 4.5V 'LS374		27	40				mA	
		I _{CCL} All inputs grounded 'S374					102	140	mA	
		I _{CCZ} CP, \overline{OE} = 4.5V 'S374 D inputs = GND					131	180	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

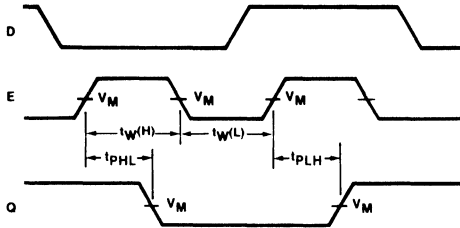
PARAMETER	TEST CONDITIONS	54/74LS		54/74S		UNIT
		C _L = 45pF, R _L = 667Ω		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 6, '374	35		75		MHz
t _{PLH} Propagation delay	Waveform 1, '373		30		14	ns
t _{PHL} Latch Enable to output			30		18	
t _{PLH} Propagation delay	Waveform 4, '373		18		12	ns
		t _{PHL} Data to output		18		
t _{PLH} Propagation delay	Waveform 6, '374		28		15	ns
		t _{PHL} Clock to output		28		
t _{PZH} Enable time to HIGH level	Waveform 2		28		15	ns
t _{PZL} Enable time to LOW level	Waveform 3, '373 '374		36		18	ns
			28		18	
t _{PHZ} Disable time from HIGH level	Waveform 2, C _L = 5pF		20		9	ns
t _{PLZ} Disable time from LOW level	Waveform 3, C _L = 5pF		25		12	ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

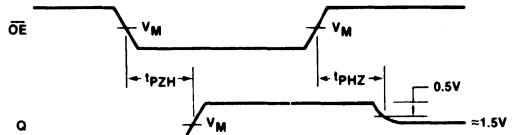
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



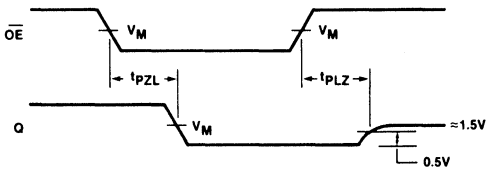
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



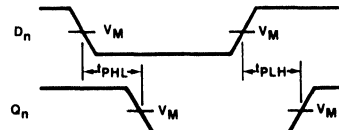
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



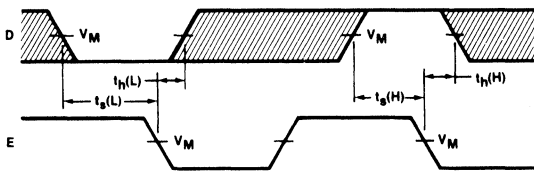
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



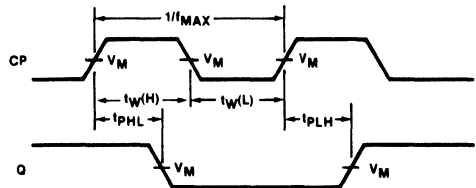
Waveform 4

DATA SETUP AND HOLD TIMES



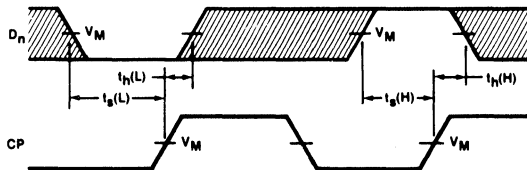
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

4

LATCHES/FLIP-FLOPS

54/74LS373, 54/74LS374, S373, S374

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74LS		54/74S		UNIT
		Min	Max	Min	Max	
$t_{W(H)}$ $t_{W(L)}$ Latch Enable pulse width	Waveform 1, '373	15 15		6 7.3		ns
t_s Setup time, Data to Latch Enable	Waveform 5, '373	5		0		ns
t_h Hold time, Data to Latch Enable	Waveform 5, '373	20		10		ns
$t_{W(H)}$ $t_{W(L)}$ Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns
t_s Setup time, Data to Clock	Waveform 7, '374	20		5		ns
t_h Hold time, Data to Clock	Waveform 7, '374	0		2		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Open

DEFINITIONS
 R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 $R_X = 1\text{k}\Omega$ for 54/74, 54S/74S, $R_X = 5\text{k}\Omega$ for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH

54/74LS375

Quad Bistable Latch

- Quad transparent latch
- Complementary outputs

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS375	12ns	6.3mA

DESCRIPTION

The '375 has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH Enable Input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the Data Inputs as long as E is HIGH. The data on the D inputs one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched output remains stable as long as the enable is LOW.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS375N	
Plastic SO	N74LS375D	
Ceramic DIP		S54LS375F
Flatpack		S54LS375W
LLCC		S54LS375G

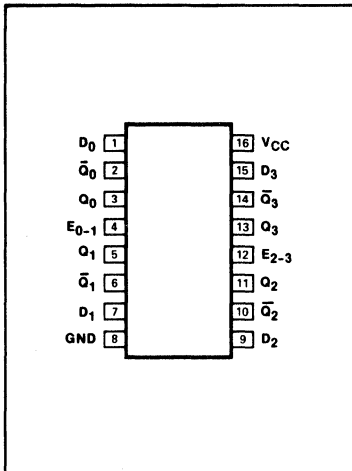
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
D ₀ -D ₃	Inputs	1LSul
E ₀₋₁ , E ₂₋₃	Inputs	4LSul
All	Outputs	10LSul

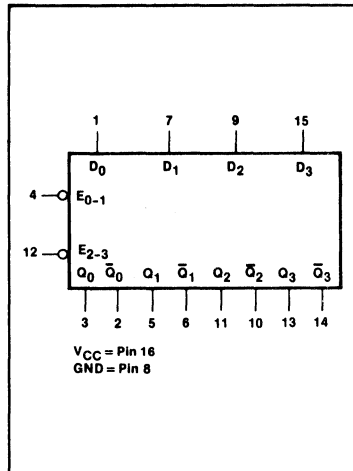
NOTE
A 54/74LS unit load (LSul) is 20µA I_{IH} and -0.4mA I_{IL}.

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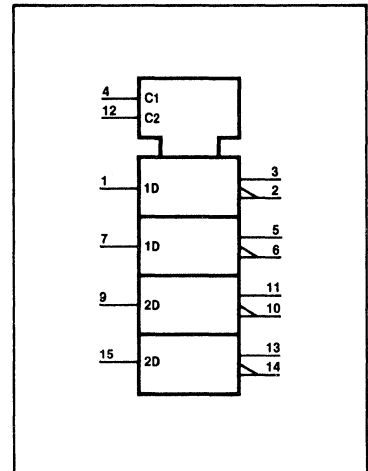
PIN CONFIGURATION



LOGIC SYMBOL



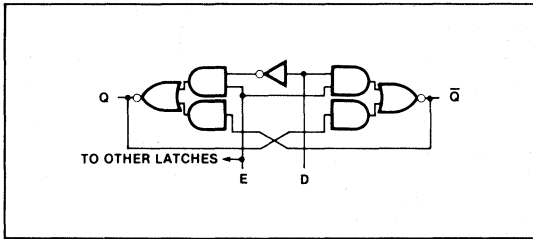
LOGIC SYMBOL (IEEE/IEC)



LATCH

54/74LS375

LOGIC DIAGRAM (Each Latch)



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS	
	E	D	Q	\bar{Q}
Data Enabled	H	L	L	H
	H	H	H	L
Data Latched	L	X	q	\bar{q}

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT
		Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+0.7	V
	Com'l			+0.8	V
I _{IK} Input clamp current				-18	mA
I _{OH} HIGH-level output current				-400	μA
I _{OL} LOW-level output current	Mil			4	mA
	Com'l			8	mA
T _A Operating free-air temperature	Mil	-55		+125	°C
	Com'l	0		70	°C

LATCH

54/74LS375

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS375			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.5	V	
		Com'l	2.7	3.5	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
		I _{OL} = 4mA	74LS	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			- 1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V	D ₀ -D ₃ inputs		0.1	mA	
		E ₀₋₁ , E ₂₋₃ inputs		0.4	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	D ₀ -D ₃ inputs		20	μA	
		E ₀₋₁ , E ₂₋₃ inputs		80	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	D ₀ -D ₃ inputs		- 0.4	mA	
		E ₀₋₁ , E ₂₋₃ inputs		- 1.6	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	- 20		- 100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		6.3	12	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Test I_{CC} with all inputs grounded and all outputs open.



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} Propagation delay Data to Q output	Waveform 1		27	ns
t _{PHL} Propagation delay Data to Q̄ output			17	
t _{PLH} Propagation delay Data to Q̄ output	Waveform 2		20	ns
t _{PHL} Propagation delay Enable to Q output			15	
t _{PLH} Propagation delay Enable to Q output	Waveform 3		27	ns
t _{PHL} Propagation delay Enable to Q̄ output			25	
t _{PLH} Propagation delay Enable to Q̄ output	Waveform 3		30	ns
t _{PHL} Propagation delay Enable to Q output			15	

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

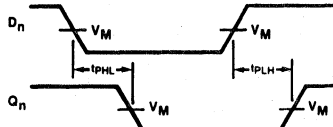
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t _W Enable pulse width	Waveform 3	20		ns
t _s Setup time, Data to Enable	Waveform 4	20		ns
t _h Hold time, Data to Enable	Waveform 4	0		ns

LATCH

54/74LS375

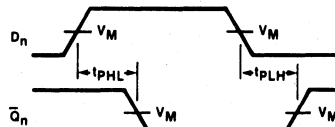
AC WAVEFORMS

PROPAGATION DELAY DATA TO Q OUTPUTS



Waveform 1

PROPAGATION DELAY DATA TO Q̄ OUTPUTS

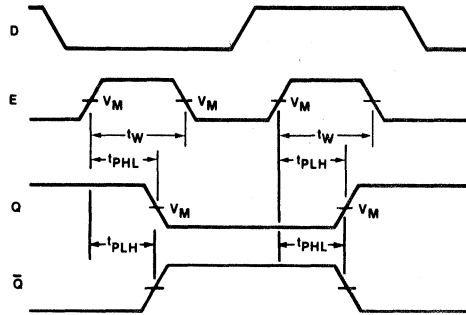


Waveform 2

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

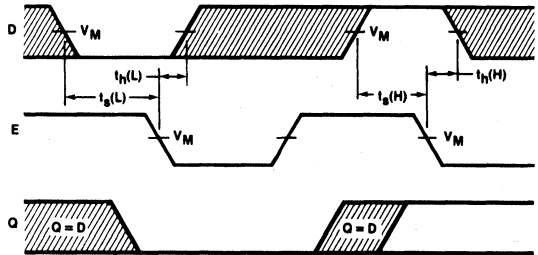
The shaded areas indicate when the input is permitted to change for predictable output performance.

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



Waveform 3

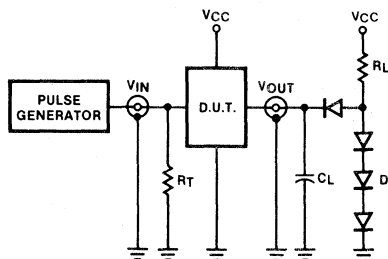
DATA SETUP AND HOLD TIMES



Waveform 4

TEST CIRCUITS AND WAVEFORMS

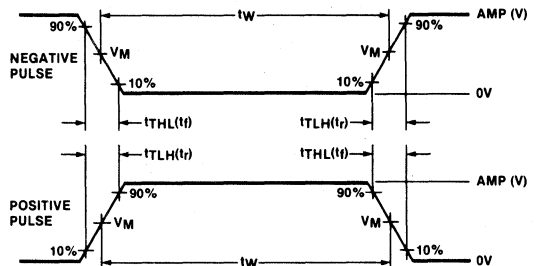
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal D Flip-Flop With Clock Enable

- Ideal for addressable register applications
- Clock Enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Slim 20-pin plastic and ceramic DIP packages
- See '273 for Master Reset version
- See '373 for transparent latch version
- See '374 for 3-state version

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS377	40MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS377N	
Plastic SO	N74LS377D	
Ceramic DIP		S54LS377F

DESCRIPTION

The '377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-

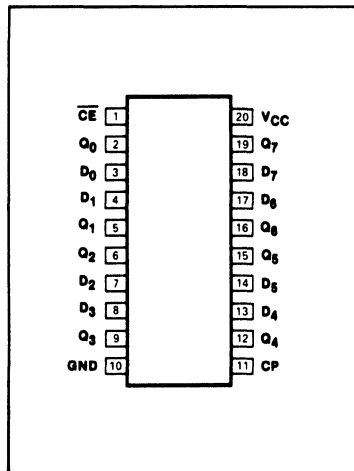
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	10LSul

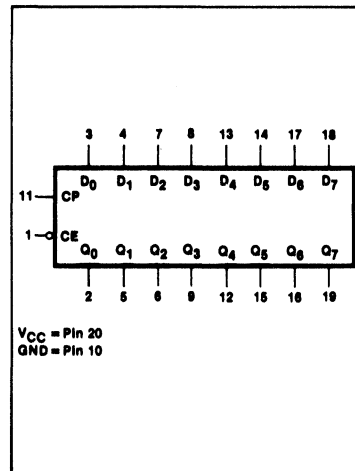
NOTE
A 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

flip's Q output. The \overline{CE} input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

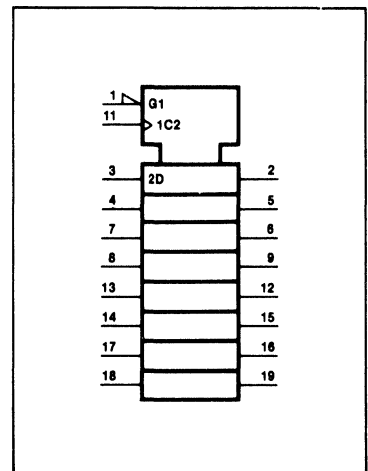
PIN CONFIGURATION



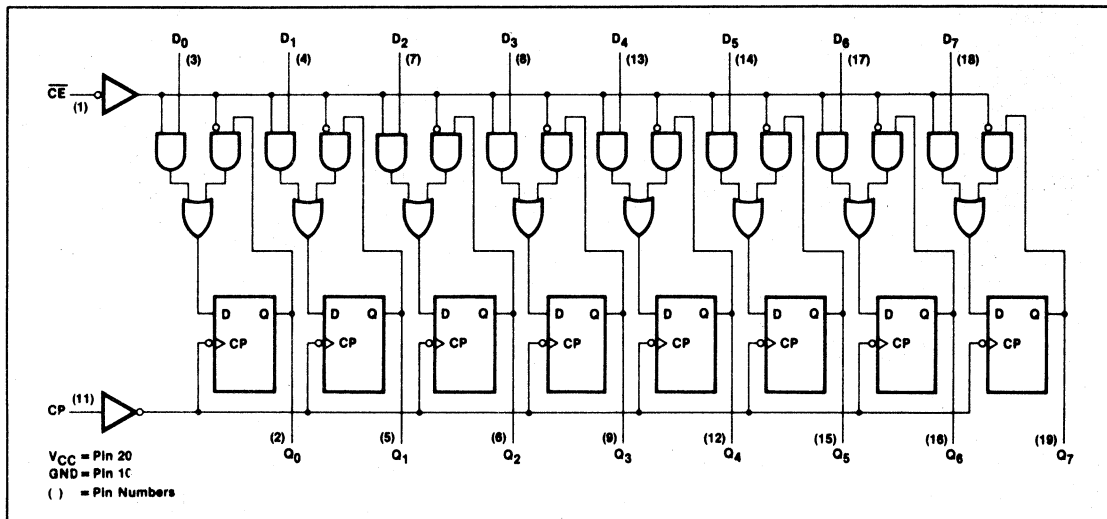
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	\overline{CE}	D_n	Q_n
Load "1"	l	l	h	H
Load "0"	l	l	l	L
Hold (do nothing)	l	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 l = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I_{IN} Input current	-30 to +1	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current				- 400	μA
I _{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

4

PARAMETER	TEST CONDITIONS ¹	54/74LS377			UNIT		
		Min	Typ ²	Max			
V _{OH}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.5	V		
		Com'l	2.7	3.5	V		
V _{OL}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.25	0.4	V	
		I _{OL} = 4mA	74LS		0.35	0.5	V
					0.25	0.4	V
V _{IK}	V _{CC} = MIN, I _I = I _{IK}				- 1.5	V	
I _I	V _{CC} = MAX, V _I = 7.0V				0.1	mA	
I _{IH}	V _{CC} = MAX, V _I = 2.7V				20	μA	
I _{IL}	V _{CC} = MAX, V _I = 0.4V				- 0.4	mA	
I _{OS}	V _{CC} = MAX		- 20		- 100	mA	
I _{CC}	V _{CC} = MAX	I _{CCH} Outputs HIGH		18	28	mA	
		I _{CCL} Outputs LOW		22	35	mA	

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - With all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

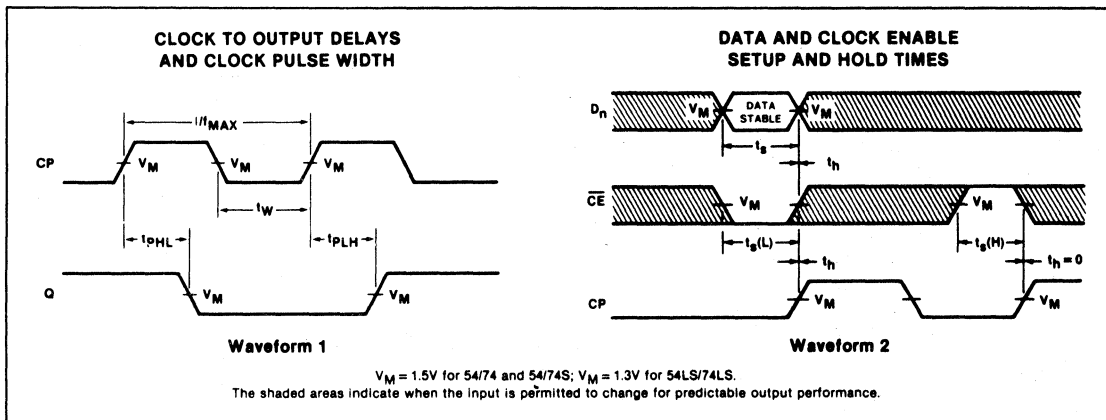
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
f _{MAX}	Waveform 1	30		MHz
t _{PLH} t _{PHL}	Waveform 1		27	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

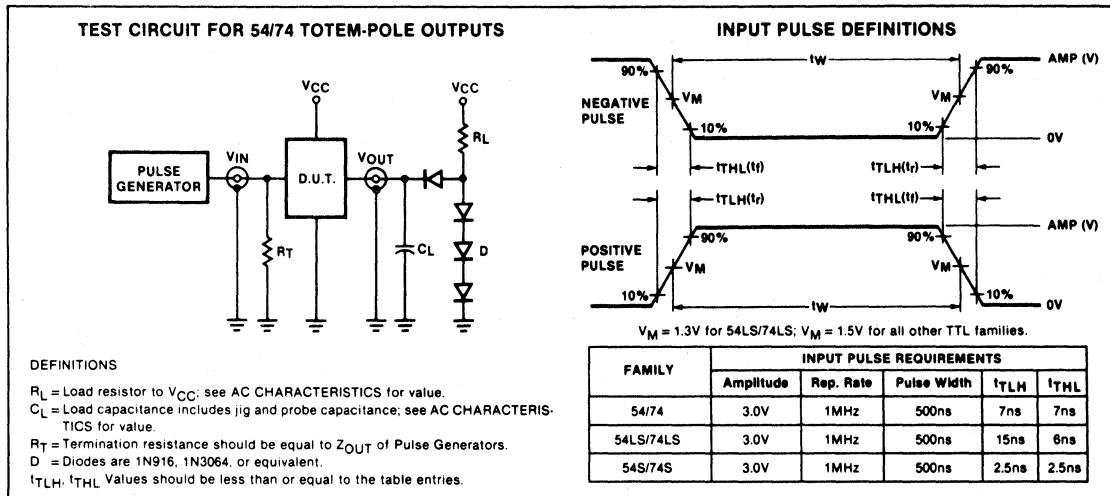
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
$t_W(L)$ Clock pulse width (LOW)	Waveform 1	20		ns
t_s Setup time, Data to CP	Waveform 2	20		ns
t_h Hold time, Data to CP	Waveform 2	5		ns
t_s Setup time, \overline{CE} to CP	Waveform 2	20		ns
t_h Hold time, \overline{CE} to CP	Waveform 2	5		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



FLIP-FLOP

54/74LS378

Hex D Flip-Flop With Clock Enable

- Ideal for addressable register applications
- Six edge-triggered D flip-flops
- Buffered common clock
- Clock Enable for address and data synchronization applications
- See '174 for Master Reset version

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS378	40MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS378N	
Ceramic DIP	S54LS378F	
Flatpack	S54LS378W	

DESCRIPTION

The '378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable (\overline{CE}) is low.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input is also edge-triggered and must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

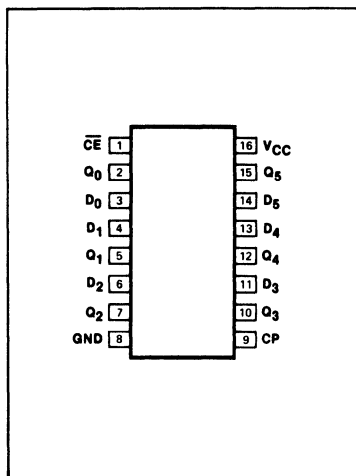
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	10LSul

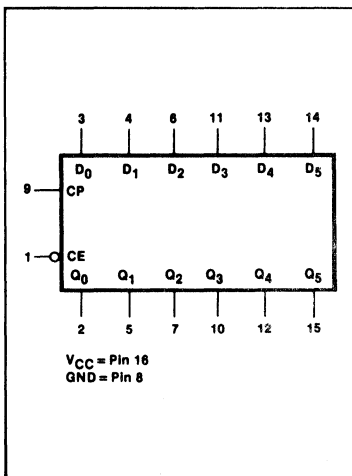
NOTE

Where a 54/74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

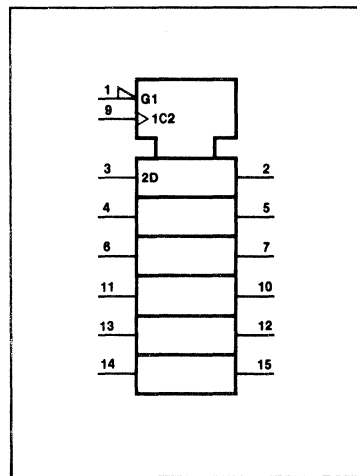
PIN CONFIGURATION



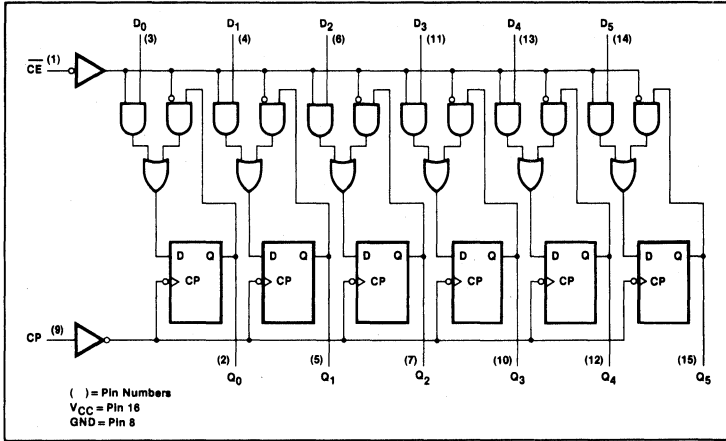
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—
FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	CE	D _n	Q _n
Load "1"	↑	↓	h	H
Load "0"	↑	↓	l	L
Hold (do nothing)	↑	X	X	no change

H = HIGH voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT
		Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+0.7	V
	Com'l			+0.8	V
I _{IK} Input clamp current				-18	mA
I _{OH} HIGH-level output current				-400	mA
I _{OL} LOW-level output current	Mil			4	mA
	Com'l			8	mA
T _A Operating free-air temperature	Mil	-55		+125	°C
	Com'l	0		70	°C

FLIP-FLOP

54/74LS378

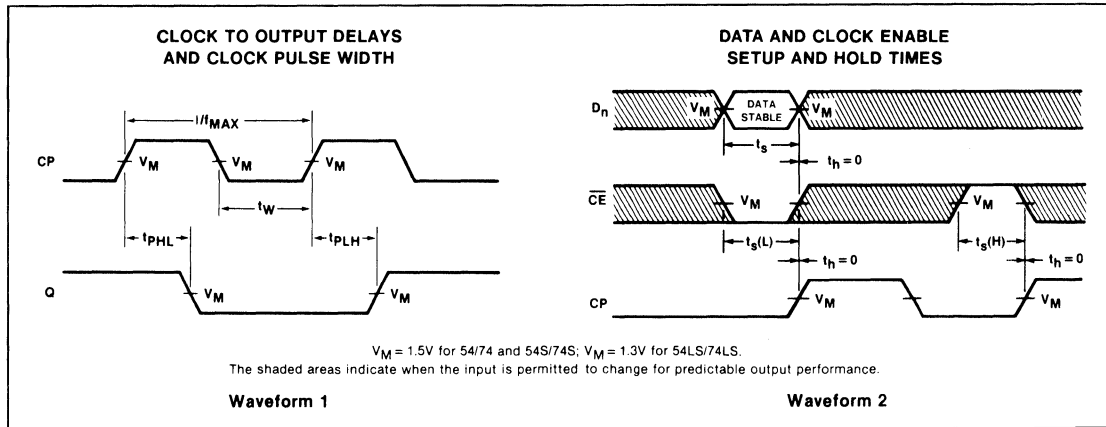
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS378			UNIT
		Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.5	V
		Com'l	2.7	3.5	V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	Mil		0.25	V
		Com'l		0.35	V
		I _{OL} = MAX			
	I _{OL} = 4mA	74LS		0.25	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V			0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V			-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-20	-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			15	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at V_{CC} = 5V, T_A = 25°C.
 - I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - With ground applied to all data inputs and the Clock Enable input and all outputs open, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.



AC WAVEFORMS



AC CHARACTERISTICS T_A = 25 °C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	30		MHz
t _{PLH} Propagation delay	Waveform 1		27	ns
t _{PHL} Clock to output			27	

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

FLIP-FLOP

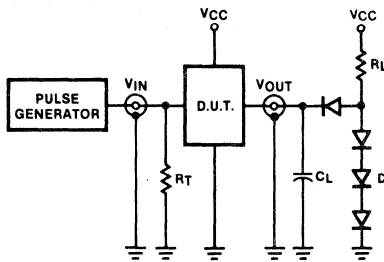
54/74LS378

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	20		ns
t_s Setup time, Data to CP	Waveform 2	20		ns
t_h Hold time, Data to CP	Waveform 2	5		ns
t_s Setup time, \overline{CE} to CP	Active state	25		ns
	Inactive state	10		ns
t_h Hold time, \overline{CE} to CP	Waveform 2	5		ns

TEST CIRCUITS AND WAVEFORMS

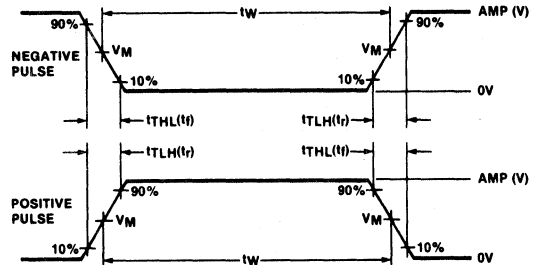
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTER

54/74LS390

Dual Decade Ripple Counter

- Two BCD decade or bi-quinary counters
- One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100
- Two Master Resets to clear each decade counter individually

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS390	55MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS390N	
Plastic SO	N74LS390D	

DESCRIPTION

The '390 is a dual 4-bit decade ripple counter divided into four separately clocked sections. The counter has two divide-by-two sections and two divide-by-five sections. These sections are normally used in a BCD decade or a bi-quinary configuration, since they share a common Master Reset input. If the two Master Resets can be used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

Each section is triggered by the HIGH-to-LOW transition of the Clock (\overline{CP}) inputs. For BCD decade operation, the Q_0 output is connected to the \overline{CP}_1 input of the divide-by-five section. For bi-quinary decade operation (50% duty cycle output), the

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
MR	Inputs	1LSul
CP_0	Inputs	4LSul
CP_1	Inputs	6LSul
All	Outputs	10LSul

NOTE

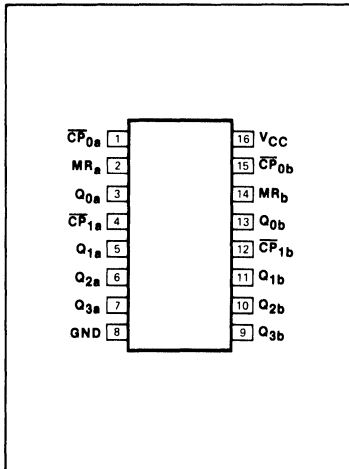
A 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

Q_3 output is connected to the CP_0 input, and Q_0 becomes the decade output.

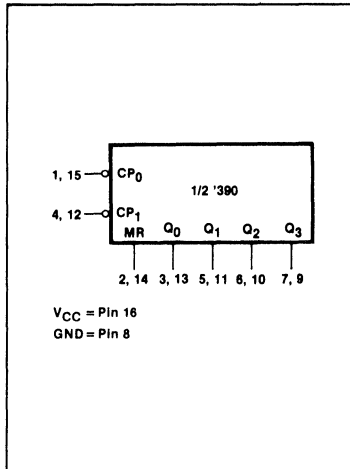
The Master Resets (MR_a and MR_b) are active HIGH asynchronous inputs to each

decade counter which operate on the portion of the counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clocks and sets the four outputs LOW.

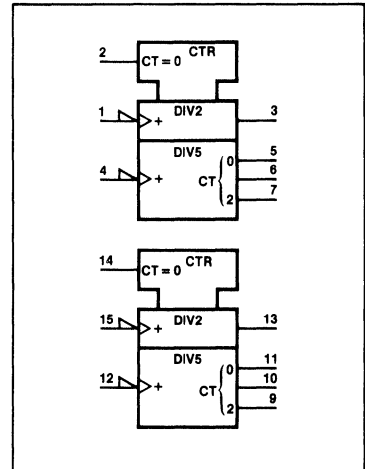
PIN CONFIGURATION



LOGIC SYMBOL



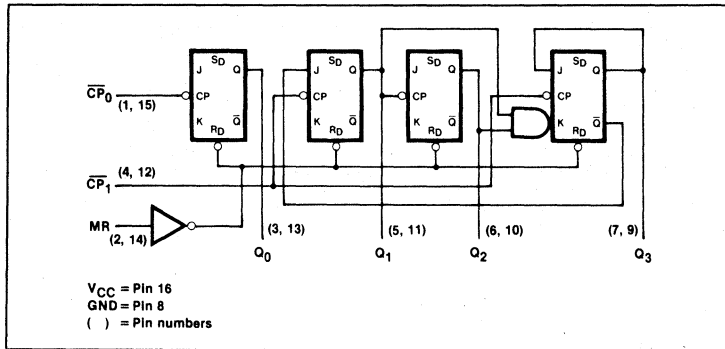
LOGIC SYMBOL (IEEE/IEC)



COUNTER

54/74LS390

LOGIC DIAGRAM



BCD COUNT SEQUENCE FOR 1/2 THE '390

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

H = HIGH voltage level
L = LOW voltage level

NOTE

Output Q₀ is connected to input \overline{CP}_1 with Counter input on \overline{CP}_0 .

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE '390

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

NOTE

Output Q₃ is connected to input \overline{CP}_0 with Counter input on \overline{CP}_1 .

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I _{IN} Input current	-30 to +1	-30 to +1	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

NOTE

V_{IN} limited to 5.5V on \overline{CP}_0 and \overline{CP}_1 inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current				- 400	μA
I _{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74LS390			UNIT		
			Min	Typ ²	Max			
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4		V	
			Com'l	2.7	3.4		V	
V _{OL}	LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.25	0.4	V	
			I _{OL} = 4mA	Mil		0.35	0.5	V
				74LS		0.25	0.4	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				- 1.5	V	
I _I	Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V	MR inputs		0.1	mA	
			V _I = 5.5V	\overline{CP}_0 inputs		0.2	mA	
				\overline{CP}_1 inputs		0.4	mA	
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	MR inputs			20	μA	
			\overline{CP}_0 inputs			100	μA	
			\overline{CP}_1 inputs			200	μA	
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V	MR inputs			- 0.4	mA	
			\overline{CP}_0 inputs			- 1.6	mA	
			\overline{CP}_1 inputs			- 2.4	mA	
I _{OS}	Short-circuit output current ³	V _{CC} = MAX		- 20		- 100	mA	
I _{CC}	Supply current ⁴ (total)	V _{CC} = MAX			15	26	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with MR inputs grounded following momentary connection to 4.5V, all other inputs grounded and outputs open.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT	
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$			
		Min	Max		
f_{MAX}	$\overline{\text{CP}}_0$ input count frequency	Waveform 1	25		MHz
f_{MAX}	$\overline{\text{CP}}_1$ input count frequency	Waveform 1	12.5		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_0$ to Q_0	Waveform 1		20 20	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_0$ to Q_2	Waveform 1		60 60	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ to Q_1 or Q_3	Waveform 1		21 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{\text{CP}}_1$ to Q_2	Waveform 1		39 39	ns
t_{PHL}	Propagation delay, MR to Q	Waveform 2		39	ns

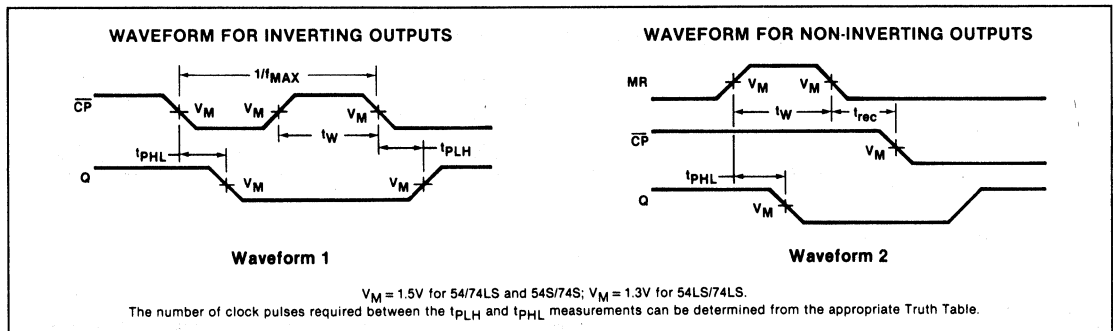
NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

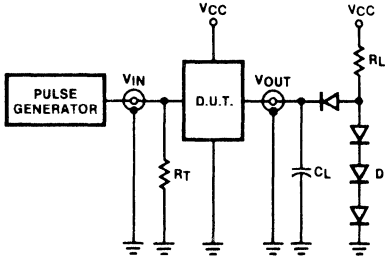
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT	
		Min	Max		
t_w	$\overline{\text{CP}}_0$ pulse width	Waveform 1	20		ns
t_w	$\overline{\text{CP}}_1$ pulse width	Waveform 1	40		ns
t_w	MR pulse width	Waveform 2	20		ns
t_{rec}	Recovery time, MR to $\overline{\text{CP}}$	Waveform 2	25		ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

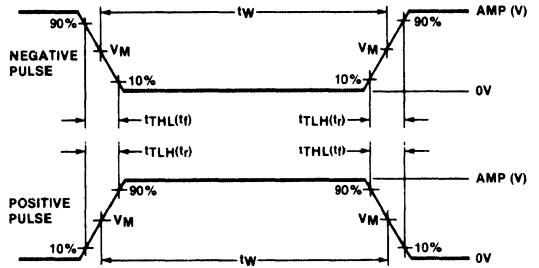
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTER

54/74LS393

Dual 4-Bit Binary Ripple Counter

- Two 4-bit binary counters
- Divide-by any binary module up to 28 in one package
- Two Master Resets to clear each 4-bit counter individually

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS393	35MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS393N	
Plastic SO	N74LS393D	
Ceramic DIP		S54LS393F
Flatpack		S54LS393W

DESCRIPTION

The '393 is a Dual 4-Bit Binary Ripple Counter with separate Clock and Master Reset inputs to each counter. The operation of each half of the '393 is the same as the '93 except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the Clock (\overline{CP}_a and \overline{CP}_b) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding.

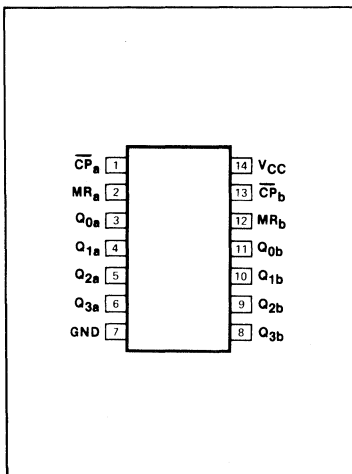
The Master Resets (MR_a and MR_b) are active-HIGH asynchronous inputs to each 4-bit counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clock and sets the outputs LOW.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

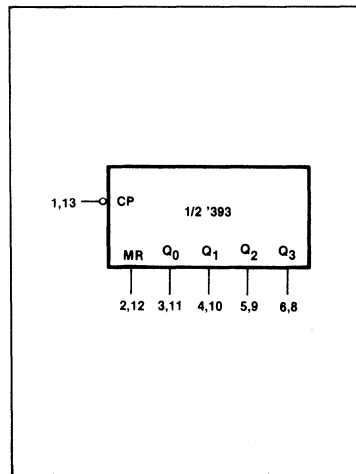
PINS	DESCRIPTION	54/74LS
MR	Master Reset input	1LSul
\overline{CP}	Clock input	4LSul
Q	Output	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

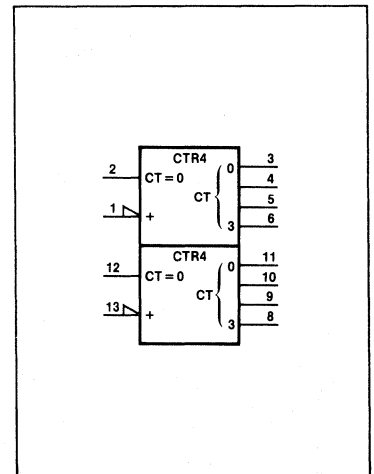
PIN CONFIGURATION



LOGIC SYMBOL



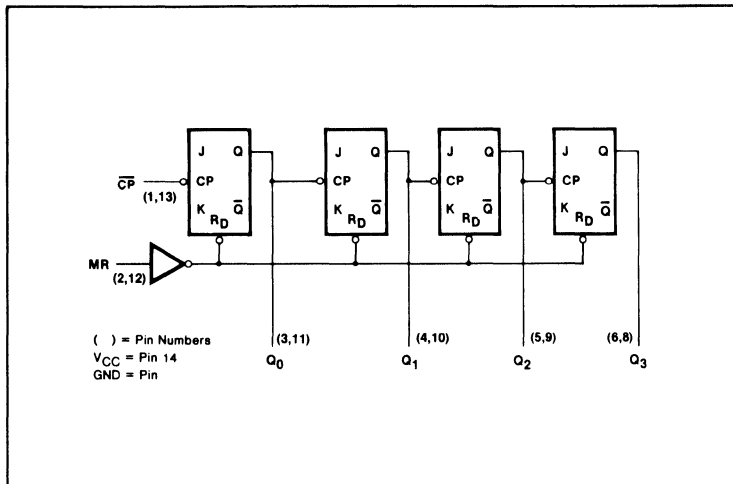
LOGIC SYMBOL (IEEE/IEC)



COUNTER

54/74LS393

LOGIC DIAGRAM



COUNT SEQUENCE FOR 1/2 THE '393

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = HIGH voltage level
L = LOW voltage level



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I _{IN} Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A Operating free-air temperature range	- 55 to + 125	0 to 70	°C

NOTE
V_{IN} limited to + 5.5V on CP input only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT
		Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+ 0.7	V
	Com'l			+ 0.8	V
I _{IK} Input clamp current				- 18	mA
I _{OH} HIGH-level output current				- 400	μA
I _{OL} LOW-level output current	Mil			4	mA
	Com'l			8	mA
T _A Operating free-air temperature	Mil	- 55		+ 125	°C
	Com'l	0		70	°C

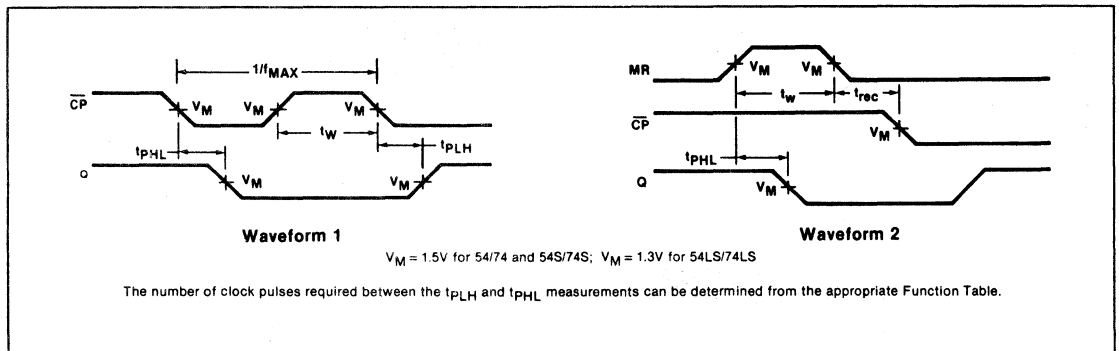
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS393			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V	
		Com'l	2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4	V
			Com'l		0.35	0.5
		I _{OL} = 4mA	74LS		0.25	0.4
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V	MR input		0.1	mA
		V _I = 5.5V	CP input		0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	MR input		20	μA	
		CP input		100	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	MR input		-0.4	mA	
		CP input		-1.6	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-20	-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		15	26	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with both MR inputs grounded following momentary connection to 4.5V, all other inputs grounded and all outputs open.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
f _{MAX} CP input count frequency	Waveform 1	25		MHz
t _{PLH} Propagation delay CP to Q ₀	Waveform 1		20	ns
t _{PHL} Propagation delay CP to Q ₃	Waveform 1		60	ns
t _{PHL} Propagation delay, MR to Q	Waveform 2		39	ns

NOTE

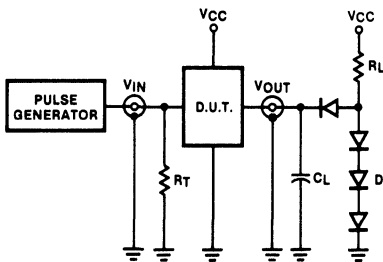
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_w \overline{CP} pulse width	Waveform 1	20		ns
t_w MR pulse width	Waveform 2	20		ns
t_{rec} Recovery time, MR to \overline{CP}	Waveform 2	25		ns

TEST CIRCUITS AND WAVEFORMS

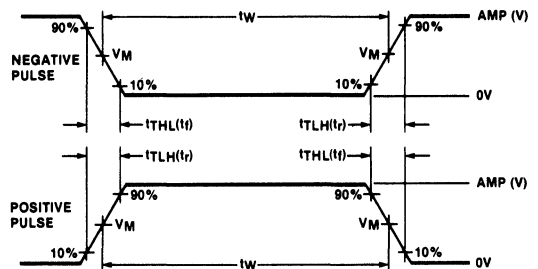
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTER

54/74LS395A

4-Bit Cascadable Shift Register With 3-State Outputs

- 4-bit parallel load shift register
- Independent 3-state buffer outputs
- Separate Q₃ output for serial expansion
- Asynchronous Master Reset

TYPE	TYPICAL f _{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS395A	45MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{CC} = 5V ± 5%; T _A = 0°C to +70°C	MILITARY RANGES V _{CC} = 5V ± 10%; T _A = -55°C to +125°C
Plastic DIP	N74LS395AN	
Ceramic DIP		S54LS395AF
Flatpack		S54LS395AW

DESCRIPTION

The '395 is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs (D₀-D₃) into the register synchronous with the HIGH-to-LOW transition of the Clock input (CP). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q₀ flip-flop, and the data in the register is shifted one bit to the right in the direction (Q₀-Q₁-Q₂-Q₃) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the HIGH-to-LOW transition of the clock.

The Master Reset (MR) is an asynchronous active-LOW input. When LOW, the MR overrides the clock and all other inputs and clears the register.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

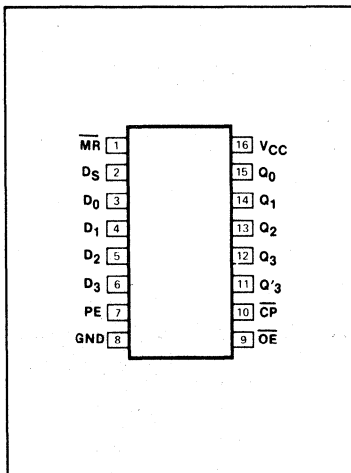
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
Q ₀ -Q ₃	Outputs	30LSul
Q ₃	Output	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL}.

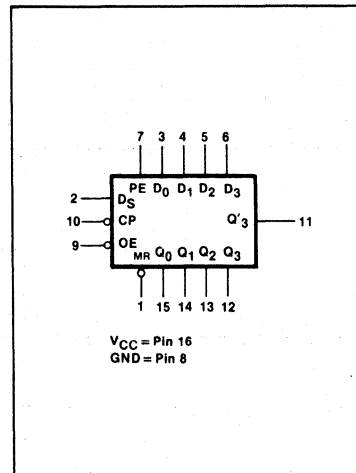
The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads. The active-LOW Output Enable (OE) controls all four 3-state buffers independent of the register operation. The data in the register appears at the outputs when OE is LOW. The outputs are in the HIGH impedance "off" state, which

means they will neither drive nor load the bus when OE is HIGH. The output from the last stage is brought out separately. This output (Q₃) is tied to the Serial Data input (D_S) of the next register for serial expansion applications. The Q₃ output is not affected by the 3-state buffer operation.

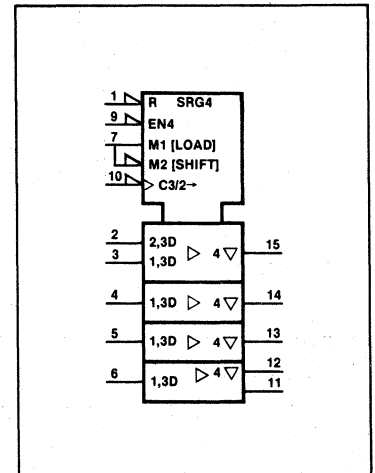
PIN CONFIGURATION



LOGIC SYMBOL



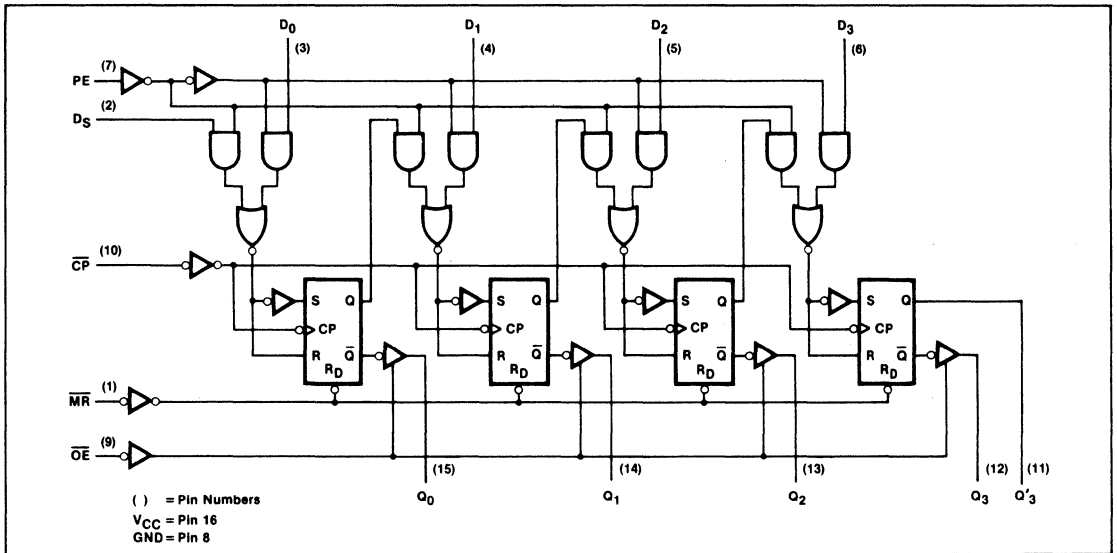
LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER

54/74LS395A

LOGIC DIAGRAM



4

MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS			
	\overline{MR}	\overline{CP}	PE	D _S	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H	l	l	l	X	L	q ₀	q ₁	q ₂
Parallel load	H	l	h	X	l	L	L	L	L
	H	l	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	\overline{OE}	Q _n (Register)	Q ₀ , Q ₁ , Q ₂ , Q ₃	Q ₃
Read	L	L	L	L
	L	H	H	H
Disable buffers	H	L	(Z)	L
	H	H	(Z)	H

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition
 q_n = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition
 X = Don't care
 (Z) = HIGH impedance "off" state
 l = HIGH-to-low transition

SHIFT REGISTER**54/74LS395A****ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +1	-30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT		
		Min	Nom	Max			
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	V	
V_{IH}	HIGH-level input voltage	2.0			V		
V_{IL}	LOW-level input voltage	Mil			+0.7	V	
		Com'l			+0.8	V	
I_{IK}	Input clamp current				-18	mA	
I_{OH}	HIGH-level output current	Q_3'				-400	μ A
		Q_0-Q_3	Mil			-1.0	mA
			Com'l			-2.6	mA
I_{OL}	LOW-level output current	Q_3'	Mil			4	mA
			Com'l			8	mA
		Q_0-Q_3	Mil			12	mA
			Com'l			24	mA
		T_A	Operating free-air temperature	Mil	-55		+125
Com'l	0				70	°C	

SHIFT REGISTER

54/74LS395A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74LS395A			UNIT	
			Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Q ₃	Mil	2.5	3.4	V	
			Com'l	2.7	3.4	V	
		Q ₀ , Q ₁ , Q ₂ , Q ₃			2.4	3.1	V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	Q ₃	I _{OL} = MAX	Mil	0.25	0.4	V
			I _{OL} = 4mA	Com'l	0.35	0.5	V
		Q ₀ , Q ₁ , Q ₂ , Q ₃	I _{OL} = MAX	Mil	0.25	0.4	V
				Com'l	0.35	0.5	V
			I _{OL} = 12mA	74LS	0.25	0.4	V
				74LS	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MIN, V _{IH} = MIN, V _O = 2.7V	Q ₀ , Q ₁ , Q ₂ , Q ₃			20	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MIN, V _{IH} = MIN, V _O = 0.4V	Q ₀ , Q ₁ , Q ₂ , Q ₃			-20	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V				0.1	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				20	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V				-0.4	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Q ₃	-20		-100	mA	
		Q ₀ , Q ₁ , Q ₂ , Q ₃	-30		-130	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX	Condition 1		19	34	mA	
		Condition 2		19	31	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_OUT = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with D_S and Master Reset at 4.5V. The Data inputs grounded and outputs open under the following conditions: *Condition 1*: OE at 4.5V. A momentary 3V, then ground, applied to CP. *Condition 2*: Ground OE and CP inputs.

AC CHARACTERISTICS T_A = 25 °C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 45pF, R _L = 667Ω		
		Min	Max	
f _{MAX} Maximum Clock frequency	Waveform 1	30		MHz
t _{PLH} Propagation delay t _{PHL} Clock to Buffer outputs	Waveform 1		30 30	ns
t _{PLH} Propagation delay t _{PHL} Clock to Q ₃ output	Waveform 1, R _L = 2kΩ, C _L = 15pF		30 30	ns
t _{PHL} Propagation delay, MR to output	Waveform 2		35	ns
t _{PZH} Enable time to HIGH level	Waveform 3		25	ns
t _{PZL} Enable time to LOW level	Waveform 4		25	ns
t _{PHZ} Disable time from HIGH level	Waveform 3, C _L = 5pF		17	ns
t _{PLZ} Disable time from LOW level	Waveform 4, C _L = 5pF		20	ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

4

SHIFT REGISTER

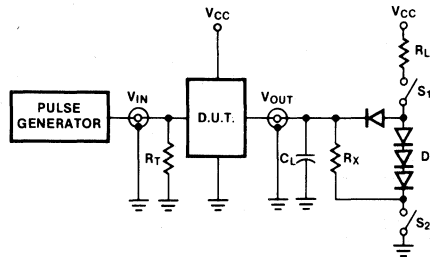
54/74LS395A

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_W Clock pulse width	Waveform 1	16		ns
t_W Master Reset pulse width	Waveform 2	25		ns
t_s Setup time, Data to clock	Waveform 5	20		ns
t_h Hold time, Data to clock	Waveform 5	10		ns
t_s Setup time, PE to clock	Waveform 5	40		ns
t_h Hold time, PE to clock	Waveform 5	10		ns
t_{rec} Recovery time, \overline{MR} to clock	Waveform 2	30		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



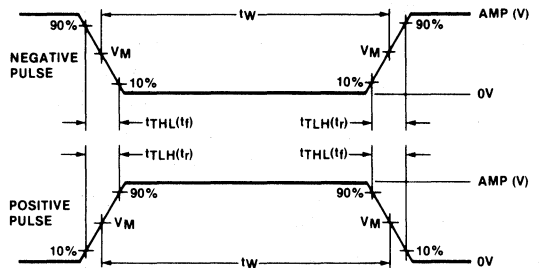
SWITCH POSITION

Test	Switch 1	Switch 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = $1k\Omega$ for 54/74, 54S/74S, $R_X = 5k\Omega$ for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.
 Q_3 is a standard totem-pole output.

INPUT PULSE DEFINITIONS

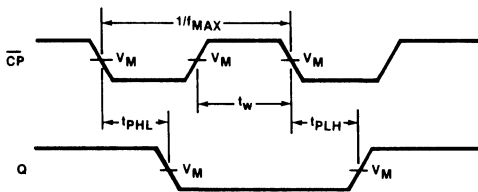


$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

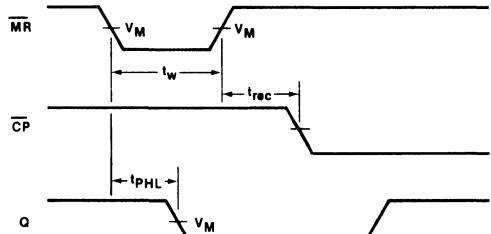
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



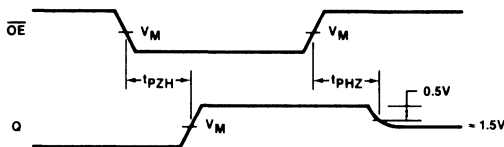
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



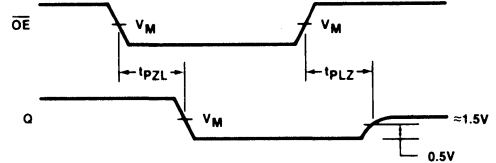
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



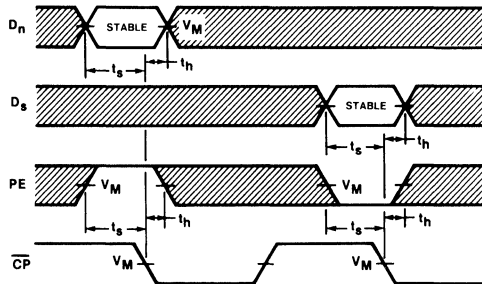
Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

PARALLEL ENABLE AND DATA SETUP AND HOLD TIMES



Waveform 5

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

4

DECODER/DRIVER

54/74LS445

BCD-To-Decimal Decoder/Driver (Open Collector)

- 80mA output drive capability
- 7V output breakdown voltage
- See '45 for 30V output voltage
- See '42 for standard TTL outputs

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS445	39ns	7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N74LS445N	
Ceramic DIP		S54LS445F
Flatpack		S54LS445W

DESCRIPTION

The '445 is a 1-of-10 decoder with open collector outputs. This decoder accepts BCD inputs on the A₀ to A₃ address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A₃ used as an active LOW enable.

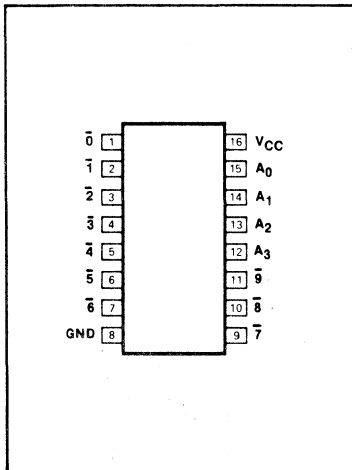
The '445 features an output breakdown voltage of 7V. This device is ideal as a lamp or solenoid driver.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

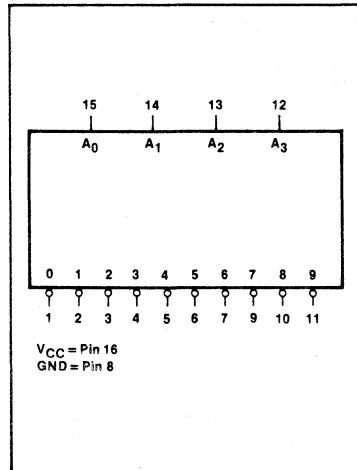
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL}.

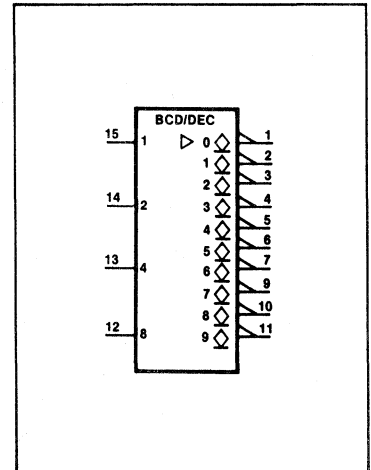
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



DECODER/DRIVER

54/74LS445

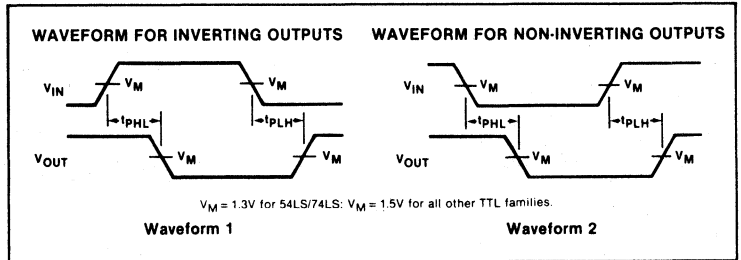
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS445			UNIT	
		Min	Typ ²	Max		
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, V_{OH} = 7.0\text{V}$			250	μA	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
		$I_{OL} = 12\text{mA}$	74LS	0.25	0.4	V
			74LS	1.6	3.0	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			0.1	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-0.4	mA	
I_{CC} Supply current ³ (total)	$V_{CC} = \text{MAX}$		7	13	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^\circ\text{C}$.
- Measure I_{CC} with all inputs grounded and all outputs open.

AC WAVEFORMS

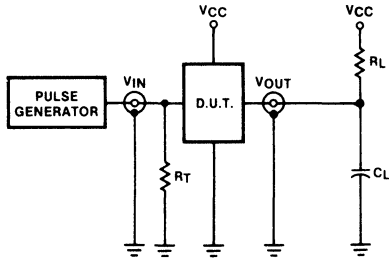


AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 45\text{pF}, R_L = 665\Omega$		
		Min	Max	
t_{PLH} Propagation delay	Waveforms 1 & 2		50	ns
t_{PHL} Address to output			50	

TEST CIRCUITS AND WAVEFORMS

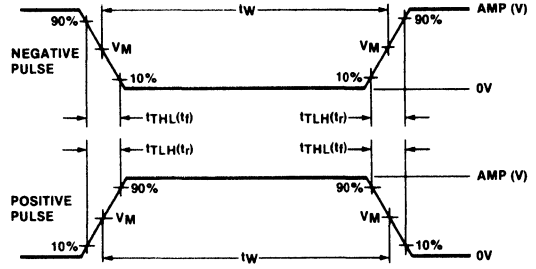
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns



COUNTER

54/74LS490

Dual BCD Decade Ripple Counter

- Two BCD decade counters
- Asynchronous Master Set (set-to-9)
- Asynchronous Master Reset (clear)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS490	55MHz	15mA

DESCRIPTION

The '490 is a Dual BCD Decade Ripple Counter with separate Clock, Master Set, and Master Reset inputs to each counter. The operation of each half of the '490 is the same as the '90 used in the BCD decade mode.

The counters are triggered by the HIGH-TO-LOW transition of the Clock (\overline{CP}) inputs. No external connections are required to get the full BCD (8421) decade counting scheme from the counters. The counter outputs are internally connected as clocks or decoded inputs to succeeding stages. Since this is a ripple type counter, the outputs do not change synchronously and should not be used for high speed address decoding.

The Master Set (MS) and Master Reset (MR) are asynchronous active-HIGH inputs. The HIGH MR input overrides the clock and clears the associated 4 bits of the counter. The HIGH MS input overrides the clock and MR inputs and sets the associated 4 bits to nine (HLLH).

ORDERING CODE

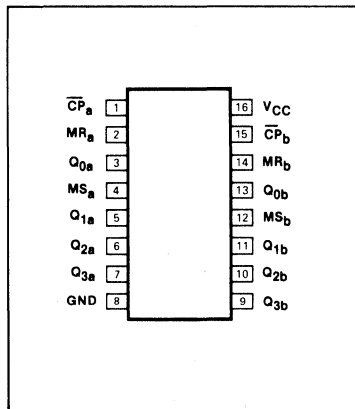
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS490N	
Ceramic DIP		S54LS490F
Flatpack		S54LS490W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

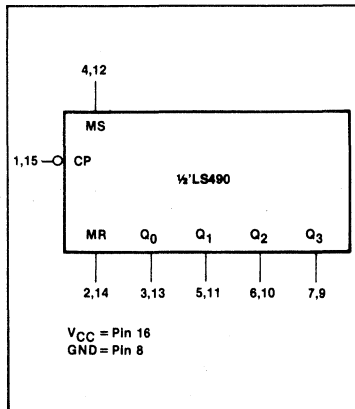
PINS	DESCRIPTION	54/74LS
\overline{CP}	Input	4LSul
MR, MS	Inputs	1LSul
Q_0-Q_3	Outputs	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

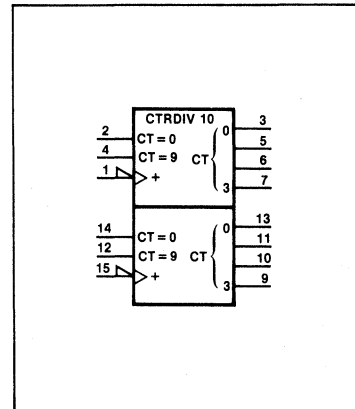
PIN CONFIGURATION



LOGIC SYMBOL



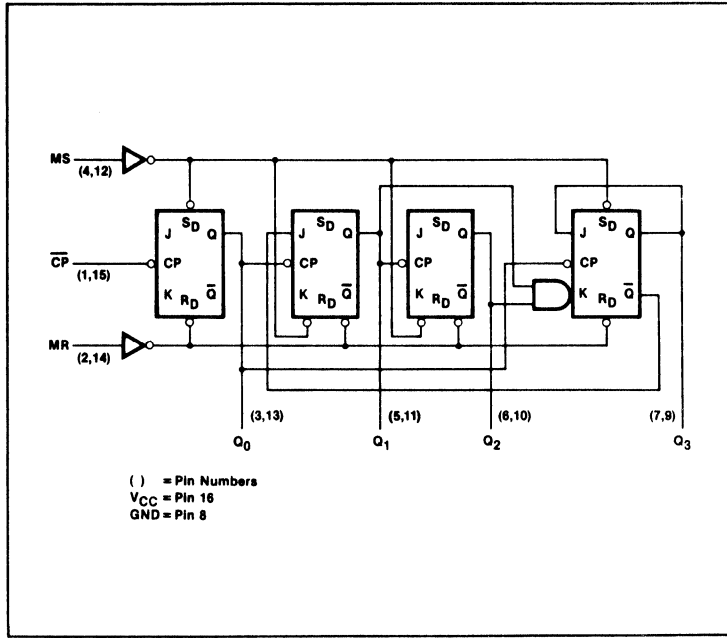
LOGIC SYMBOL (IEEE/IEC)



COUNTER

54/74LS490

LOGIC DIAGRAM



MODE SELECTION—FUNCTION TABLE FOR 1/2 THE '490

RESET/SET INPUTS		OUTPUTS			
MR	MS	Q ₀	Q ₁	Q ₂	Q ₃
H	L	L	L	L	L
L	H	H	L	L	L
L	L	Count			

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

BCD COUNT SEQUENCE FOR 1/2 THE '490

COUNT	OUTPUTS			
	Q ₀	Q ₁	Q ₂	Q ₃
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE
 Output Q₀ connected to input \overline{CP}_1 .

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I_{IN} Input current	-30 to +1	-30 to +1	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

NOTE
 V_{IN} limited to +5.5V on \overline{CP} input only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT
		Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			V
V_{IL} LOW-level input voltage	Mil			+0.7	V
	Com'l			+0.8	V
I_{IK} Input clamp current				-18	mA
I_{OH} HIGH-level output current				-400	μA
I_{OL} LOW-level output current	Mil			4	mA
	Com'l			8	mA
T_A Operating free-air temperature	Mil	-55		+125	°C
	Com'l	0		70	°C

4

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS490			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5	3.4	V	
		Com'l	2.7	3.4	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
		I _{OL} = 4mA	74LS	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 7.0V	MR, MS inputs		0.1	mA
		V _I = 5.5V	CP input		0.2	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V		MR, MS inputs		20	μA
			CP input		100	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V		MR, MS inputs		-0.4	mA
			CP input		-1.6	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX			-20	-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			15	26	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with all outputs open, MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
f _{MAX} CP input count frequency	Waveform 1	35		MHz
t _{PLH} t _{PHL} Propagation delay CP to Q ₀	Waveform 1		20 20	ns
t _{PLH} t _{PHL} Propagation delay CP to Q ₁ or Q ₃	Waveform 1		39 39	ns
t _{PLH} t _{PHL} Propagation delay CP to Q ₂	Waveform 1		54 54	ns
t _{PHL} Propagation delay, MR to Q	Waveform 2		39	ns
t _{PLH} t _{PHL} Propagation delay MS to Q	Waveforms 2 & 3		39 36	ns

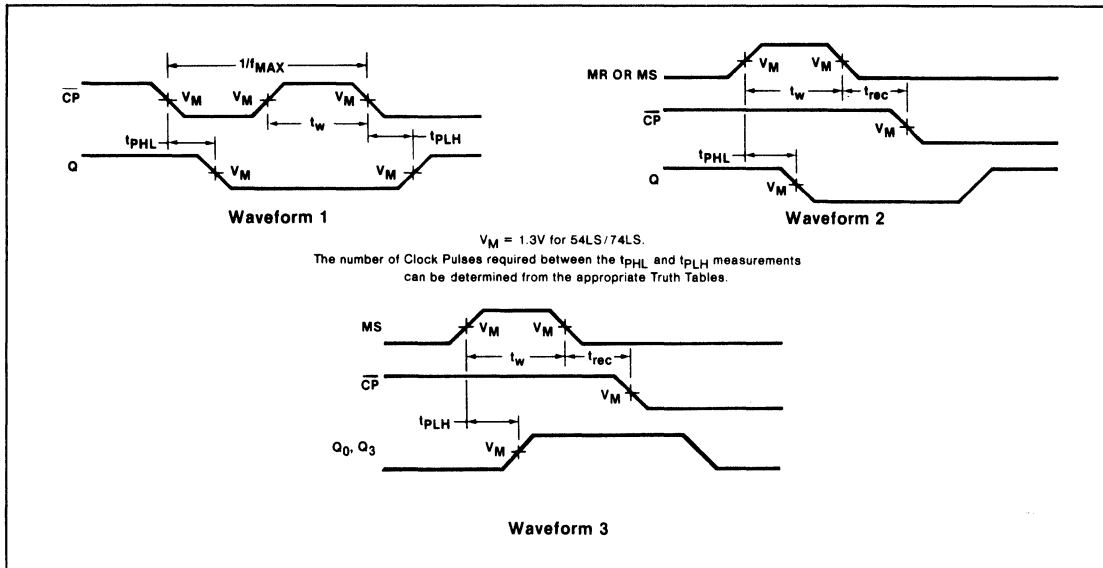
NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

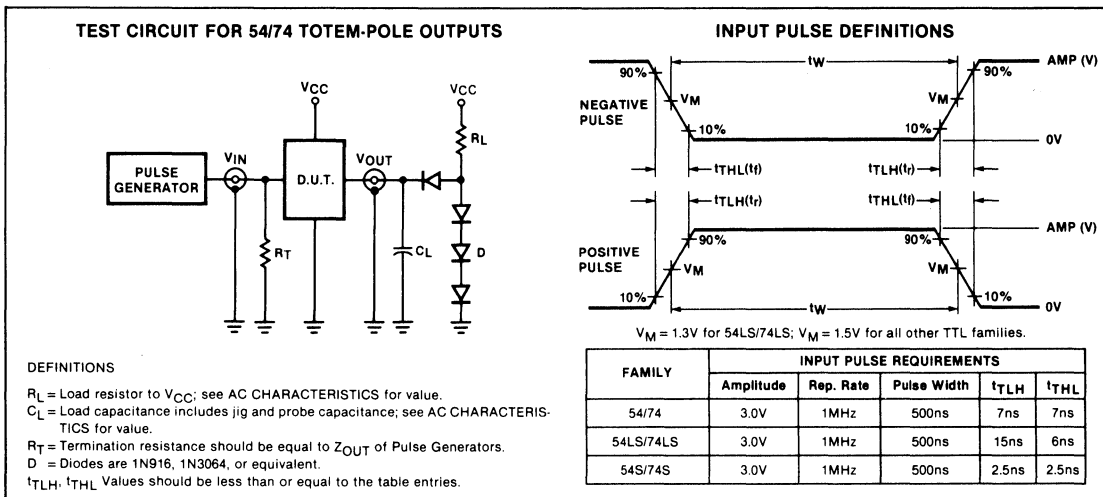
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t _W CP pulse width	Waveform 1	20		ns
t _W MR pulse width	Waveform 2	20		ns
t _W MS pulse width	Waveforms 2 & 3	20		ns
t _{rec} Recovery time, MR to CP	Waveform 2	25		ns
t _{rec} Recovery time, MS to CP	Waveforms 2 & 3	25		ns

AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS



FLIP-FLOP

54/74S534

Octal D Flip-Flop With 3-State Outputs

- 8-bit positive, edge-triggered register
- Inverting outputs
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S534	8ns	116mA

DESCRIPTION

The '534 is an 8-bit, edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's \overline{Q} output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers inde-

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74S534N	
Ceramic DIP		S54S534F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

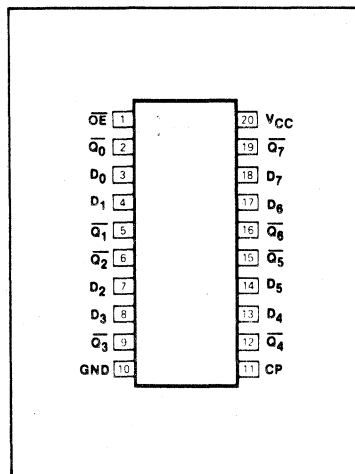
PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
Where a 54/74S unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} .

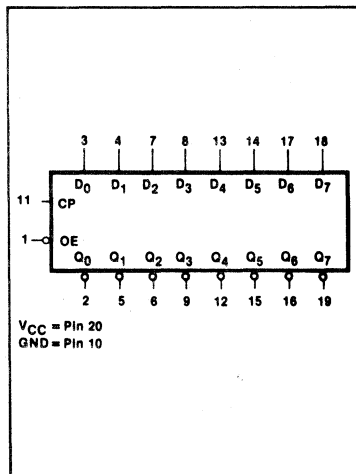
pendent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH,

the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

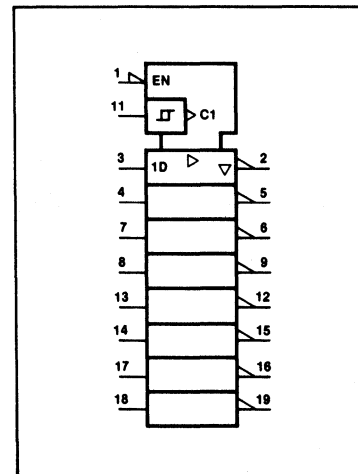
PIN CONFIGURATION



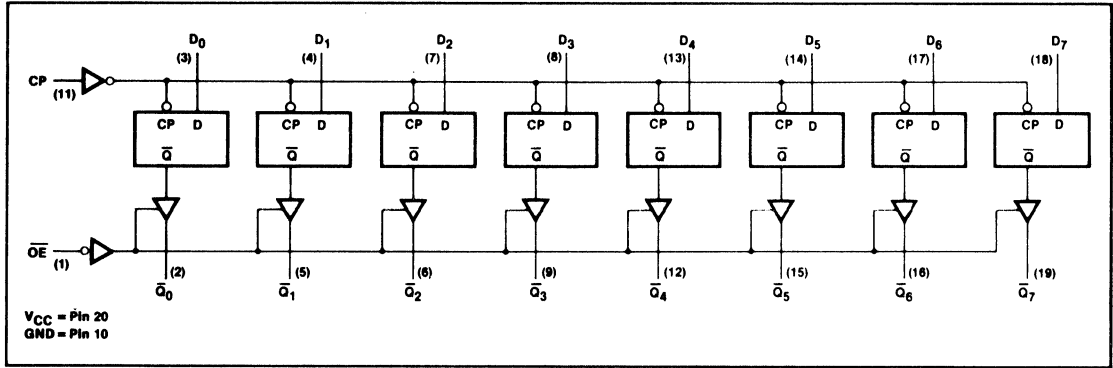
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		Q_0-Q_7
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Load register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 (Z) = HIGH impedance "off" state
 ↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54S	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state.	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_A Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74S			UNIT
		Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			V
V_{IL} LOW-level input voltage	Mil			+0.8	V
	Com'l			+0.8	V
I_{IK} Input clamp current				-18	mA
I_{OH} HIGH-level output current	Mil			-2.0	mA
	Com'l			-6.5	mA
I_{OL} LOW-level output current	Mil			20	mA
	Com'l			20	mA
T_A Operating free-air temperature	Mil	-55		+125	°C
	Com'l	0		70	°C

NOTE
 V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		54/74S534			UNIT	
			Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		Mil	2.4	3.0	V	
			Com'l	2.4	3.1	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil		0.5 ⁴	V	
			Com'l		0.5	V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.2	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 2.4V			50	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN	V _O = 0.5V			-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.5V			-0.25	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-40		-100	mA	
I _{CC} Supply Current (total)	V _{CC} = MAX	I _{CCL}	All inputs grounded		102	140	mA
		I _{CCZ}	CP, \overline{OE} = 4.5V D inputs = GND		131	180	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54S/74S		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 3	75		MHz
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 3		15 17	ns
t _{PZH} Enable time to HIGH level	Waveform 1		15	ns
t _{PZL} Enable time to LOW level	Waveform 2		18	ns
t _{PHZ} Disable time from HIGH level	Waveform 1, C _L = 5pF		9	ns
t _{PLZ} Disable time from LOW level	Waveform 2, C _L = 5pF		12	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

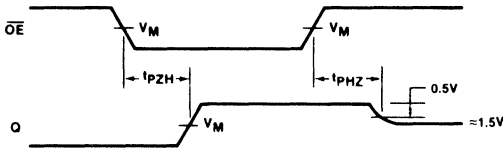
PARAMETER	TEST CONDITIONS	54S/74S		UNIT
		Min	Max	
t _{w(H)} t _{w(L)} Clock pulse width	Waveform 3	6 7.3		ns
t _s Setup time, Data to Clock	Waveform 4	5		ns
t _h Hold time, Data to Clock	Waveform 4	2		ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

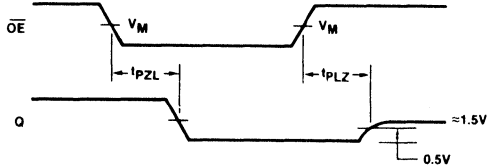
AC WAVEFORMS

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



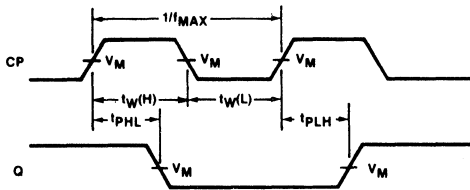
Waveform 1

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



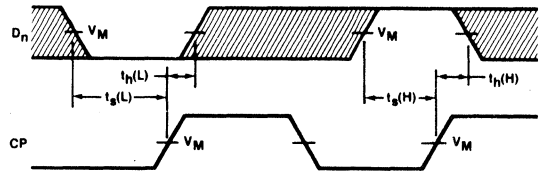
Waveform 2

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 3

DATA SETUP AND HOLD TIMES



Waveform 4

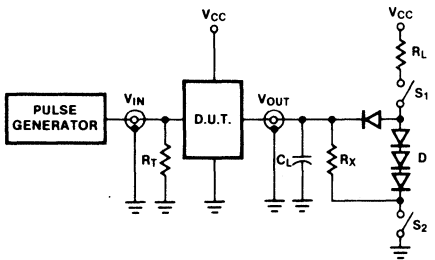
$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



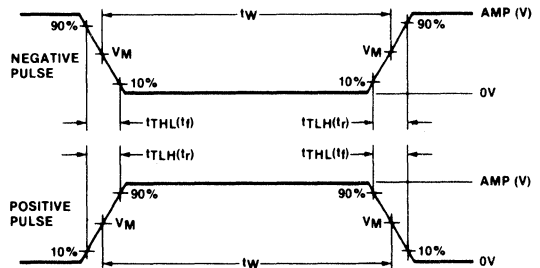
SWITCH POSITION

Test	Switch 1	Switch 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pHL}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 $R_X = 1k\Omega$ for 54/74, 54S/74S, $R_X = 5k\Omega$ for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS, $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS/DRIVERS

54/74LS540, 54/74LS541

Octal Buffer/Line Driver (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS540	9ns	22mA
74LS541	10ns	23mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS540N • N74LS541N	
Plastic SO	N74LS540D • N74LS541D	
Ceramic DIP		S54LS540F • S54LS541F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

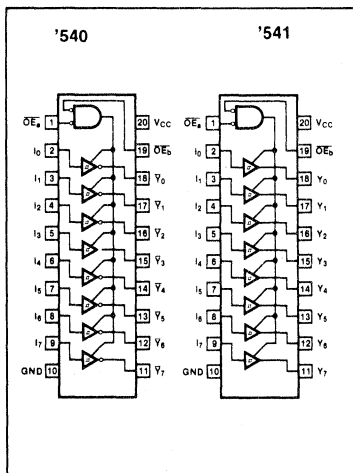
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20 μ A I_{IH} and $-0.4mA$ I_{IL} .

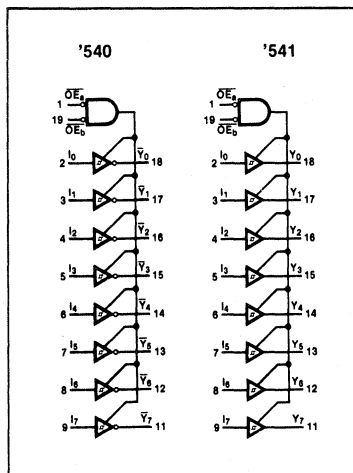
FUNCTION TABLE

INPUTS			OUTPUTS	
\overline{OE}_1	\overline{OE}_2	I	Y	\overline{Y}
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

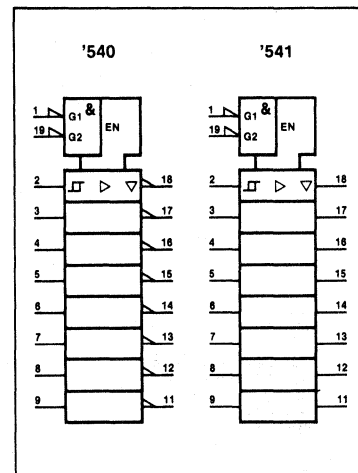
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUFFERS/DRIVERS

54/74LS540, 54/74LS541

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +7.0	-0.5 to +7.0	V
I _{IN}	Input current	-30 to +1	-30 to +1	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	-55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I _{IK}	Input clamp current				-18	mA
I _{OH}	HIGH-level output current	Mil			-12	mA
		Com'l			-15	mA
I _{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T _A	Operating free-air temperature	Mil	-55		+125	°C
		Com'l	0		70	°C

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
I _{PZH}	Open	Closed
I _{PZL}	Closed	Open
I _{PHZ}	Closed	Closed
I _{PLZ}	Closed	Closed

DEFINITIONS
 R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

BUFFERS/DRIVERS

54/74LS540, 54/74LS541

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹			54/74LS540, 541			UNIT
				Min	Typ ²	Max	
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$			0.2	0.4		V
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = 0.5V, I_{OH} = \text{MAX}$			2.0			V
	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = -3\text{mA}$			2.4	3.4		V
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$	Mil		0.25	0.4	V
			Com'l		0.35	0.5	V
		$I_{OL} = 12\text{mA}$	74LS		0.25	0.4	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_1 = I_{IK}$					-1.5	V
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_H = \text{MIN}, V_{IL} = \text{MAX}, V_O = 2.7V$					20	μA
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_H = \text{MIN}, V_{IL} = \text{MAX}, V_O = 0.4V$					-20	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$					0.1	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$					20	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4V$					-0.2	mA
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$			-40		-130	mA
I_{CC} Supply current (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH			16	25	mA
		I_{CCL} Outputs LOW			27	45	mA
		I_{CCZ} Outputs OFF			31	52	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V, T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5V$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}, V_{CC} = 5.0V$

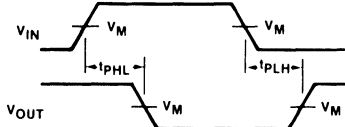
PARAMETER	TEST CONDITIONS	54/74LS540		54/74LS541		UNIT
		$C_L = 45\text{pF}, R_L = 667\Omega$		$C_L = 45\text{pF}, R_L = 667\Omega$		
		Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveforms 1 & 2		15		15	ns
			15		18	
t_{PZH} Output enable time to HIGH level	Waveform 3		25		32	ns
t_{PZL} Output enable time to LOW level	Waveform 4		38		38	ns
t_{PHZ} Output disable time from HIGH level	Waveform 3, $C_L = 5\text{pF}$		18		18	ns
t_{PLZ} Output disable time from LOW level	Waveform 4, $C_L = 5\text{pF}$		25		29	ns

BUFFERS/DRIVERS

54/74LS540, 54/74LS541

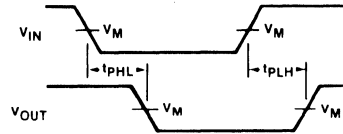
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



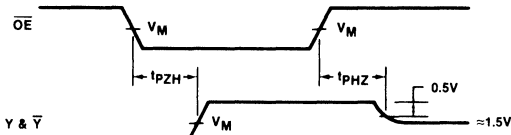
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



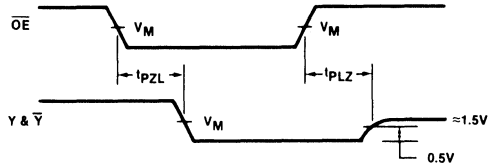
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

3-STATE BIDIRECTIONAL COUNTERS

54/74LS568A, 569A

- Speed improved over LS568/LS569
- Synchronous counting and loading
- UP/DOWN counting
- BCD decade counter — '568A
- Modulo 16 binary counter — '569A
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous Master Reset
- 3-State Counter outputs
- Gated Carry output

'568A BCD Decade Up/Down Synchronous Counter (3-State)
'569A 4-Bit Binary Up/Down Synchronous Counter (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS568A	35MHz	28mA
74LS569A	35MHz	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS568AN • N74LS569AN	
Ceramic DIP		S54LS568AF • S54LS569AF

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
$Q_0 - Q_3$	Outputs	30LSul
\overline{TC} , GC	Outputs	10LSul

NOTE

A 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

DESCRIPTION

The '568A and '569A are synchronous pre-settable UP/DOWN counters featuring an internal carry look-ahead for applications in high speed counting designs.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count-Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the Clock.

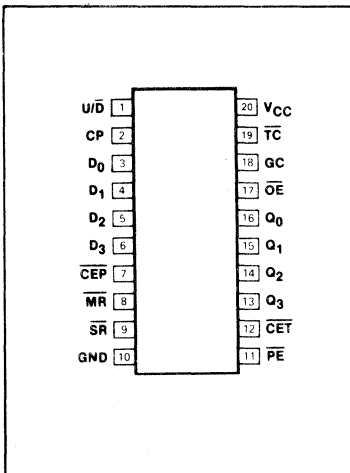
The counter is fully programmable; that is,

the outputs may be preset to either level. Presetting is synchronous with the Clock, and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the Clock. The Synchronous Reset (\overline{SR}), when LOW one setup time before the LOW-to-HIGH transition of the Clock, overrides the \overline{CEP} , \overline{CET} and \overline{PE} inputs, and causes the flip-flops to go LOW coincident with the positive Clock transition.

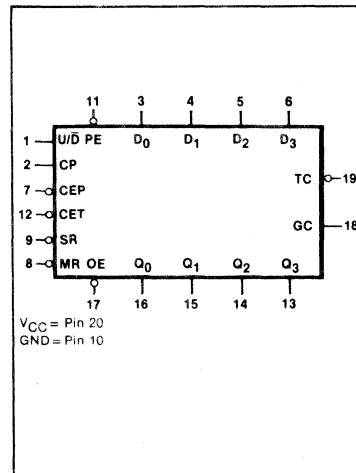
The Master Reset (\overline{MR}) is an asynchronous overriding clear function which forces all stages to a LOW state while the \overline{MR} input is LOW without regard to the Clock.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (\overline{CET} and \overline{CEP}) and a Terminal Count (\overline{TC}) output. Both Count Enable inputs must be LOW to count. The \overline{CET} input is fed forward to enable the \overline{TC} output. The \overline{TC} output thus

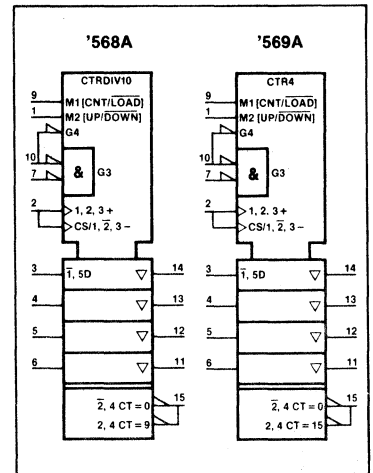
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



3-STATE BIDIRECTIONAL COUNTERS

54/74LS568A, 569A

enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q₀ output. This LOW level \overline{TC} pulse is used to enable successive cascaded stages. See Figure A in '168/169 data sheet for the fast synchronous multistage counting connections.

The Gated Clock output (GC) is a Terminal Count output which provides a HIGH-

LOW-HIGH pulse for a duration equal to the LOW time of the Clock pulse when \overline{TC} is LOW. The GC output can be used as a Clock input for the next stage in a simple ripple expansion scheme.

The direction of counting is controlled by the UP/DOWN (U/D) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The active LOW Output Enable (\overline{OE}) input controls the 3-State buffer outputs independent of the counter operation. When \overline{OE} is LOW, the count appears at the buffer outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

MODE SELECT—FUNCTION TABLE

COUNTER OPERATING MODES	INPUTS								COUNTER STATES			
	\overline{MR}	CP	\overline{SR}	U/D	\overline{PE}	\overline{CEP}	\overline{CET}	D _n	Q ₀	Q ₁	Q ₂	Q ₃
Asynchronous Reset	L	X	X	X	X	X	X	X	L	L	L	L
Synchronous Reset	H	↑	↓	X	X	X	X	X	L	L	L	L
Parallel load	H	↑	h	X	↓	X	X	↓	L	L	L	L
	H	↑	h	X	↓	X	X	h	H	H	H	H
Count up	H	↑	h	h	h	↓	↓	X	count up			
Count down	H	↑	h	↓	h	↓	↓	X	count down			
Hold (do nothing)	H	↑	h	X	h	h	X	X	no change			
	H	↑	h	X	h	X	h	X	no change			

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	\overline{OE}	Q _n -Counter	Q ₀ , Q ₁ , Q ₂ , Q ₃
Read counter	L	L	L
	L	H	H
Disable outputs	H	L	(Z)
	H	H	(Z)

TERMINAL COUNT FUNCTION TABLE, '568A

INPUTS				COUNTER STATES				OUTPUTS	
CP	U/D	\overline{CEP}	\overline{CET}	Q ₀	Q ₁	Q ₂	Q ₃	\overline{TC}	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	X	X	H	L	H
L	H	L	L	H	X	X	H	L	L
X	H	H	L	H	X	X	H	L	H
X	H	X	H	H	X	X	H	H	H

TERMINAL COUNT FUNCTION TABLE, '569A

INPUTS				COUNTER STATES				OUTPUTS	
CP	U/D	\overline{CEP}	\overline{CET}	Q ₀	Q ₁	Q ₂	Q ₃	\overline{TC}	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	H	H	H	L	H
L	H	L	L	H	H	H	H	L	L
X	H	H	L	H	H	H	H	L	H
X	H	X	H	H	H	H	H	H	H

H = HIGH voltage level

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

↓ = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition

X = Don't care

(Z) = HIGH impedance "off" state

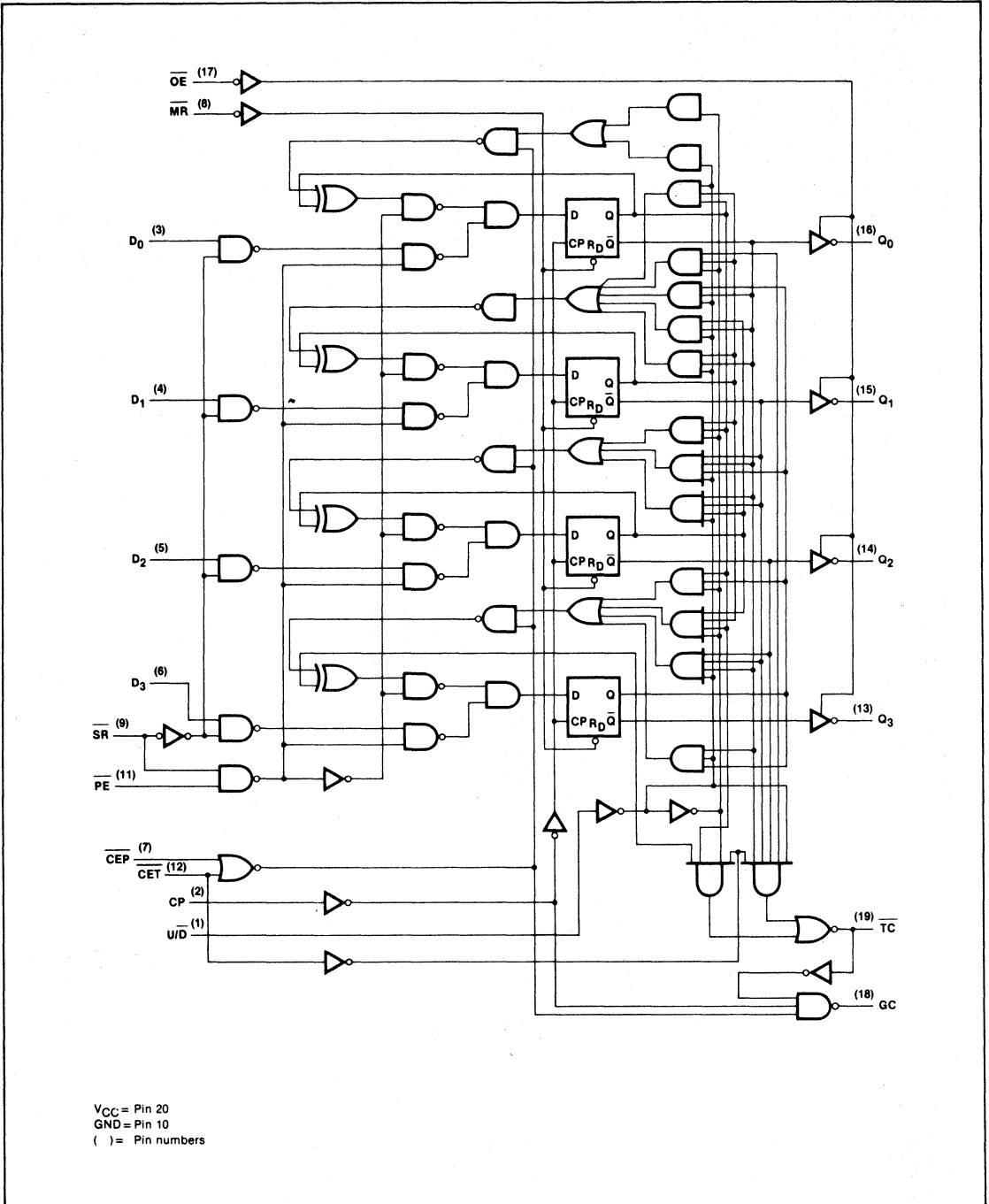
↑ = LOW-to-HIGH clock transition

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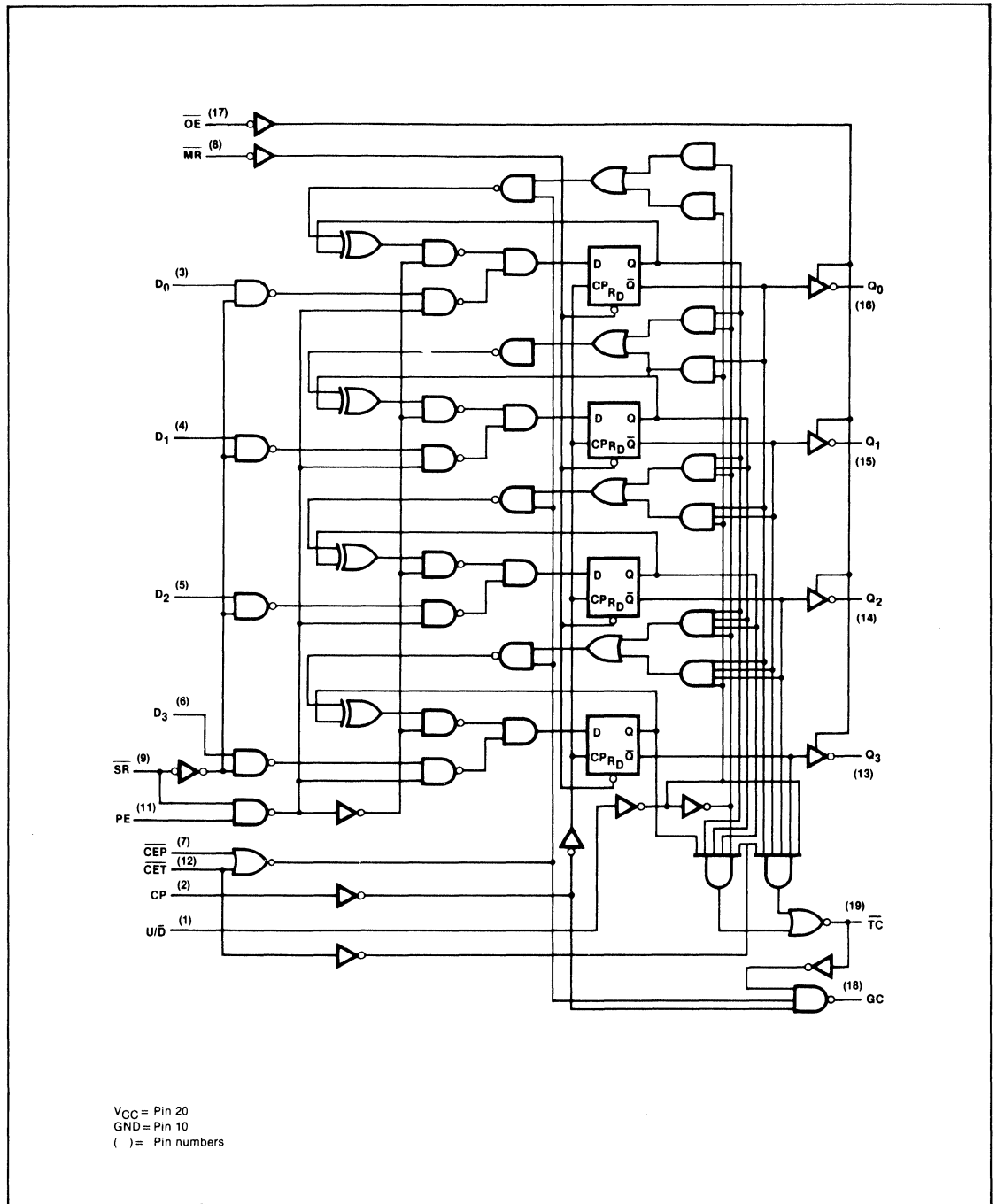
3-STATE BIDIRECTIONAL COUNTERS

54/74LS568A, 569A

LOGIC DIAGRAM, '568A



LOGIC DIAGRAM, '569A



V_{CC} = Pin 20
 GND = Pin 10
 () = Pin numbers

3-STATE BIDIRECTIONAL COUNTERS

54/74LS568A, 569A

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I_{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage	Mil		+ 0.7	V	
		Com'l		+ 0.8	V	
I_{IK}	Input clamp current			- 18	mA	
I_{OH}	HIGH-level output current	Q_0-Q_3	Mil		- 1.0	mA
			Com'l		- 2.6	mA
		\overline{TC} , GC			- 400	μ A
I_{OL}	LOW-level output current	Q_0-Q_3	Mil		12	mA
			Com'l		24	mA
		\overline{TC} , GC	Mil		4	mA
			Com'l		8	mA
T_A	Operating free-air temperature	Mil	- 55	+ 125	°C	
		Com'l	0	70	°C	

3-STATE BIDIRECTIONAL COUNTERS

54/74LS568A, 569A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER	TEST CONDITIONS ¹			54/74LS568, 569			UNIT
				Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	Q ₀ -Q ₃	I _{OH} = MAX	Mill	2.4		V
				Com'l	2.4		V
		\overline{TC} , GC	I _{OH} = MAX	Mill	2.4		V
				Com'l	2.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	Q ₀ -Q ₃	I _{OL} = MAX	Mill		0.4	V
				Com'l		0.5	V
		\overline{TC} , GC	I _{OL} = 12mA	74LS		0.4	V
			I _{OL} = MAX	Mill		0.4	V
				Com'l		0.5	V
			I _{OL} = 4mA	74LS		0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}					-1.5	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.7V					20	μA
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _O = 0.4V					-20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V					0.1	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V					-0.4	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	Q ₀ -Q ₃		-30		-100	mA
		\overline{TC} , GC		-15		-100	mA
I _{CC} Supply current (total)	V _{CC} = MAX				28	43	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_OUT = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

4

3-STATE BIDIRECTIONAL COUNTERS

54/74LS568A, 569A

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	35		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		15 20	ns
t_{PLH} Propagation delay t_{PHL} Clock to $\overline{\text{TC}}$	Waveform 2		20 25	ns
t_{PLH} Propagation delay t_{PHL} CET to $\overline{\text{TC}}$	Waveform 3		14 15	ns
t_{PLH} Propagation delay t_{PHL} U/ $\overline{\text{D}}$ control to $\overline{\text{TC}}$	Waveform 4		20 25	ns
t_{PLH} Propagation delay t_{PHL} Clock to GC	Waveform 2		15 17	ns
t_{PLH} Propagation delay t_{PHL} CET or CEP to GC	Waveform 2		16 26	ns
t_{PHL} Propagation delay $\overline{\text{MR}}$ to output	Waveform 5		20	ns
t_{PZH} Output enable to HIGH level	Waveform 6		15	ns
t_{PZL} Output enable to LOW level	Waveform 7		15	ns
t_{PHZ} Output disable from HIGH level	Waveform 6, $C_L = 5\text{pF}$		20	ns
t_{PLZ} Output disable from LOW level	Waveform 7, $C_L = 5\text{pF}$		22	ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

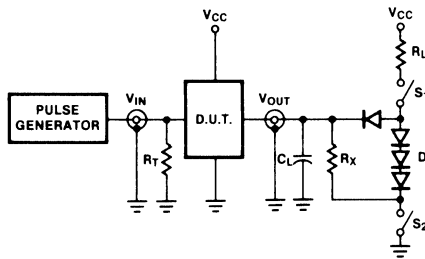
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_W Clock pulse width	Waveform 1	20		ns
t_s Setup time data to clock	Waveform 8	20		ns
t_h Hold time data to clock	Waveform 8	0		ns
t_s Setup time $\overline{\text{PE}}$ to clock	Waveform 8	25		ns
t_h Hold time $\overline{\text{PE}}$ to clock	Waveform 8	0		ns
t_s Setup time $\overline{\text{CEP}}$ & $\overline{\text{CET}}$ to clock	Waveform 9	20		ns
t_h Hold time $\overline{\text{CEP}}$ & $\overline{\text{CET}}$ to clock	Waveform 9	0		ns
t_s Setup time U/ $\overline{\text{D}}$ to clock	Waveform 10	30		ns
t_h Hold time U/ $\overline{\text{D}}$ to clock	Waveform 10	0		ns
t_s Setup time $\overline{\text{SR}}$ to clock	Waveform 11	30		ns
t_h Hold time $\overline{\text{SR}}$ to clock	Waveform 11	0		ns
t_{rec} Recovery time $\overline{\text{MR}}$ to clock	Waveform 5	20		ns

3-STATE BIDIRECTIONAL COUNTERS

54/74LS568A, 569A

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



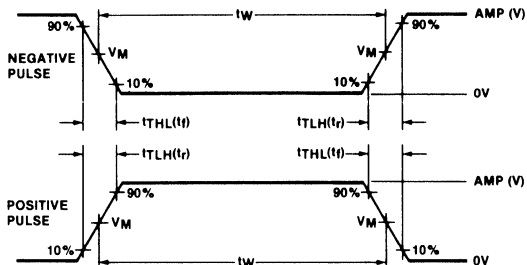
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1k Ω for 54/74, 54S/74S, R_X = 5k Ω for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



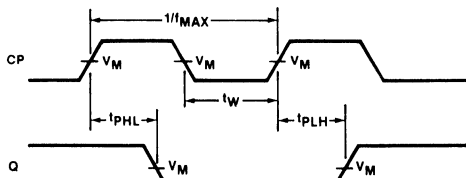
$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns



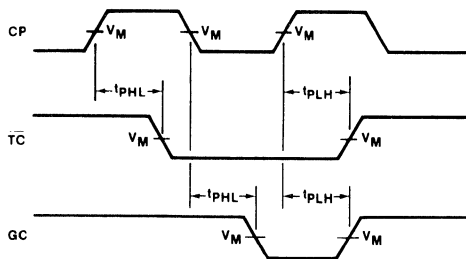
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

CLOCK TO TERMINAL COUNT DELAYS



Waveform 2

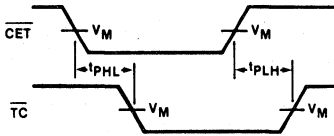
$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS

3-STATE BIDIRECTIONAL COUNTERS

54/74LS568A, 569A

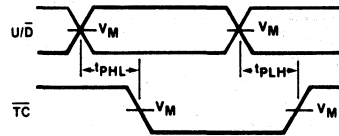
AC WAVEFORMS (Continued)

PROPAGATION DELAYS \overline{CET} INPUT TO TERMINAL COUNT OUTPUT



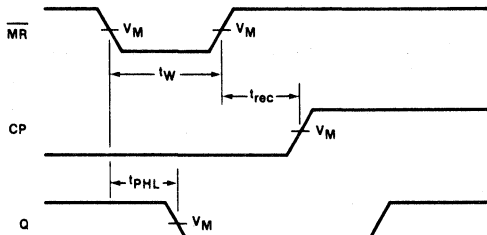
Waveform 3

PROPAGATION DELAYS U/D CONTROL TO TERMINAL COUNT OUTPUT



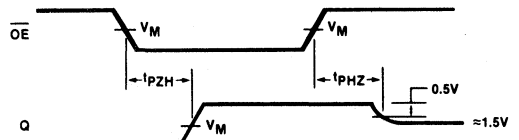
Waveform 4

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



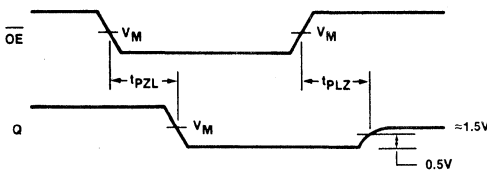
Waveform 5

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



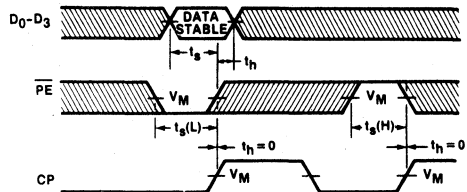
Waveform 6

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 7

PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES



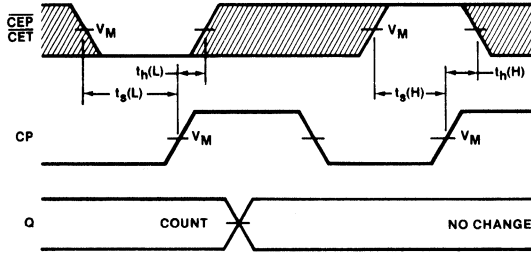
Waveform 8

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

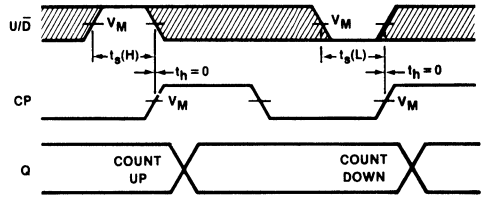
AC WAVEFORMS (Continued)

COUNT ENABLE SETUP AND HOLD TIMES



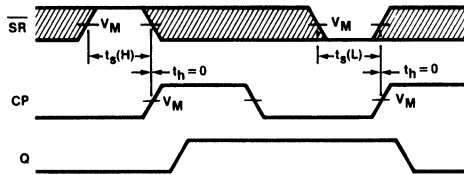
Waveform 9

UP/DOWN CONTROL SETUP AND HOLD TIMES



Waveform 10

SYNCHRONOUS RESET SETUP AND HOLD TIMES



Waveform 11

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS
 The shaded areas indicate when the input is permitted to change for predictable output performance.

TRANSCEIVERS

54/74LS620, LS623

Preliminary LS620

- Octal bidirectional bus interface
- 3-State buffer outputs
 - LS620, inverting
 - LS623, non-inverting
- Hysteresis on all Data inputs
- PNP inputs for reduced loading

DESCRIPTION

The 'LS623 is an octal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The outputs are capable of sinking 24mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The LS620 is an inverting version of the 'LS623. Both have built-in hysteresis to minimize ac noise effects.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission

'LS620 Inverting Octal Bus Transceiver (3-State)
'LS623 Non-Inverting Octal Bus Transceiver (3-State)

Type	Typical Propagation Delay	Typical Supply Current (Total)
74LS620		50mA
74LS623	9ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS620N • N74LS623N	
Ceramic DIP		S54LS620F • S54LS623F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

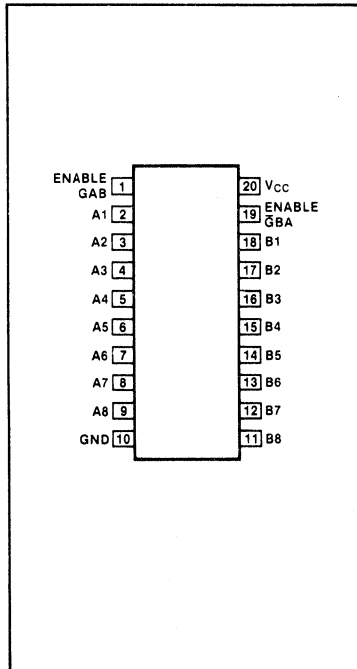
NOTE
 A 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\bar{G}BA$ and GAB). The enable inputs can be used to disable the device so that the buses are effectively isolated.

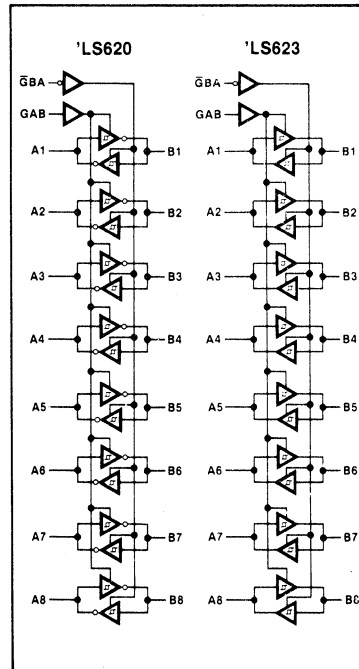
The dual-enable configuration gives the 'LS620 and 'LS623 the capability to store

data by simultaneous enabling of $\bar{G}BA$ and GAB . Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

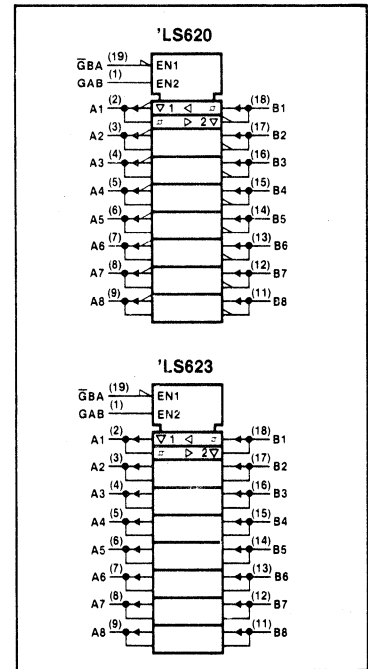
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE)



TRANSCEIVERS

54/74LS620, LS623

Preliminary LS620

FUNCTION TABLE

ENABLE	INPUTS		OPERATION	
	$\bar{G}BA$	GAB	'LS620	'LS623
L	L	L	\bar{B} data to A bus	B data to A bus
H	H	H	\bar{A} data to B bus	A data to B bus
H	L	L	(Z)	(Z)
L	H	H	\bar{B} data to A bus, \bar{A} data to B bus	B data to A bus, A data to B bus

H = HIGH voltage level

L = LOW voltage level

(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I_{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

NOTE

 V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT
		Min	Nom	Max	
V_{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage		2.0			V
V_{IL} LOW-level input voltage	Mil			+ 0.5	V
	Com'l			+ 0.6	V
I_{IK} Input clamp current				- 18	mA
I_{OH} HIGH-level output current	Mil			- 12	mA
	Com'l			- 15	mA
I_{OL} LOW-level output current	Mil			12	mA
	Com'l			24	mA
T_A Operating free-air temperature	Mil	- 55		+ 125	°C
	Com'l	0		70	°C

TRANSCEIVERS

54/74LS620, LS623

Preliminary LS620

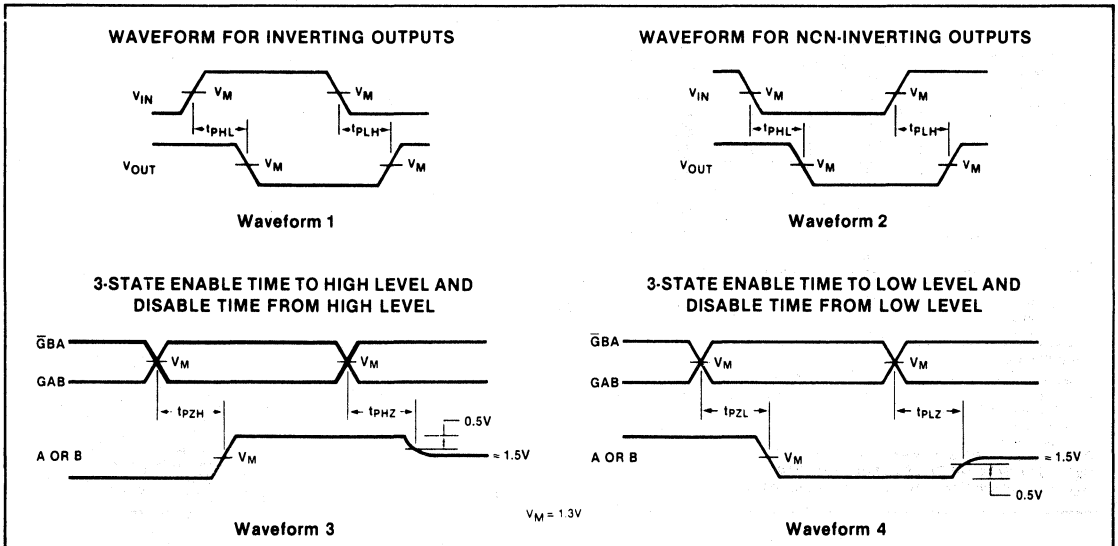
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS620, 54/74LS623			UNIT	
		Min	Typ ²	Max		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input	Mil	0.1		V	
		Com'l	0.2		V	
V_{OL} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OH} = \text{MAX}$	2.0		V	
		$I_{OH} = -3\text{mA}$	2.4	3.4	V	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = 12\text{mA}$	Mil	0.25	0.4	V
			Com'l	0.25	0.4	V
		$I_{OL} = 24\text{mA}$	74LS	0.35	0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$				-1.5	V
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$, \bar{G} input = 2.0V, $V_O = 2.7\text{V}$				20	μA
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$, \bar{G} input = 2.0V, $V_O = 0.4\text{V}$				-400	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$ A or B input			0.1	mA
		$V_I = 7.0\text{V}$, \bar{G} BA or GAB input			0.1	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$				20	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$				-0.4	mA
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$		-40		-130	mA
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		59	70	mA
		I_{CCL} Outputs LOW		42	90	mA
		I_{CCZ} Outputs OFF		64	95	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC}\text{MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with outputs open.

AC WAVEFORMS



TRANSCEIVERS

54/74LS620, LS623

Preliminary LS620

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74LS620		54/74LS623		UNIT
		$C_L = 45\text{pF}$, $R_L = 867\Omega$		$C_L = 45\text{pF}$, $R_L = 867\Omega$		
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A input to B output	Waveform 1, '620	10	15	15	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output	Waveform 1, '620 Waveform 2, '623	10	15	15	ns
t_{PZH}	Enable to HIGH $\bar{G}BA$ input to A output	Waveform 3	40	40	40	ns
t_{PZH}	Enable to HIGH GAB input to B output	Waveform 3	40	40	40	ns
t_{PZL}	Enable to LOW $\bar{G}BA$ input to A output	Waveform 4	40	40	40	ns
t_{PZL}	Enable to LOW GAB input to B output	Waveform 4	40	40	40	ns
t_{PHZ}	Disable from HIGH $\bar{G}BA$ input to A output	Waveform 3, $C_L = 5\text{pF}$	25	25	25	ns
t_{PHZ}	Disable from HIGH GAB input to B output	Waveform 3, $C_L = 5\text{pF}$	25	25	25	ns
t_{PLZ}	Disable from LOW $\bar{G}BA$ input to A output	Waveform 4, $C_L = 5\text{pF}$	25	25	25	ns
t_{PLZ}	Disable from LOW GAB input to B output	Waveform 4, $C_L = 5\text{pF}$	25	25	25	ns

☐ Test limits in screened columns are preliminary.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
 R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 $R_X = 1\text{k}\Omega$ for 54/74, 54S/74S, $R_X = 5\text{k}\Omega$ for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVERS

54/74LS621, LS622

Preliminary

'LS621 Non-Inverting Octal Bus Transceiver (Open Collector)
'LS622 Inverting Octal Bus Transceiver (Open Collector)

FEATURES

- Octal bidirectional bus interface
- Open-collector output
 - LS621, non-inverting
 - LS622, inverting
- Hysteresis on all Data inputs
- PNP inputs for reduced loading

DESCRIPTION

The 'LS621 is an octal transceiver featuring non-inverting open-collector bus compatible outputs in both send and receive directions. The outputs are capable of sinking 24mA and sourcing up to 15mA, providing very good capacitive drive characteristics. The 'LS622 is an inverting version of the 'LS621. Both have built-in hysteresis to minimize ac noise effects.

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\bar{G}BA$ and GAB).

Type	Typical Propagation Delay	Typical Supply Current (Total)
74LS621		
74LS622		

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS621N • N74LS622N	
Ceramic DIP		S54LS621F • S54LS622F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSuI
All	Outputs	30LSuI

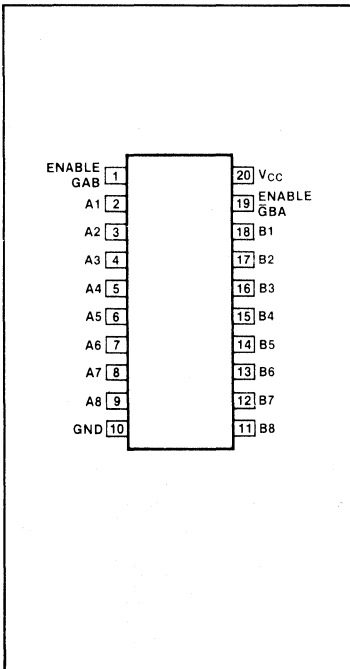
NOTE
A 54/74LS unit load (LSuI) is 20 μ A I_{IH} and $-0.4mA$ I_{IL} .

The enable inputs can be used to disable the device so that the buses are effectively isolated.

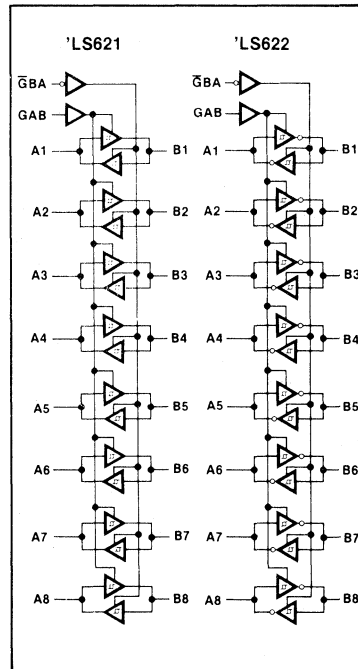
The dual-enable configuration gives the 'LS621 and 'LS622 the capability to store data by simultaneous enabling of $\bar{G}BA$ and GAB . Each output reinforces its input

in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

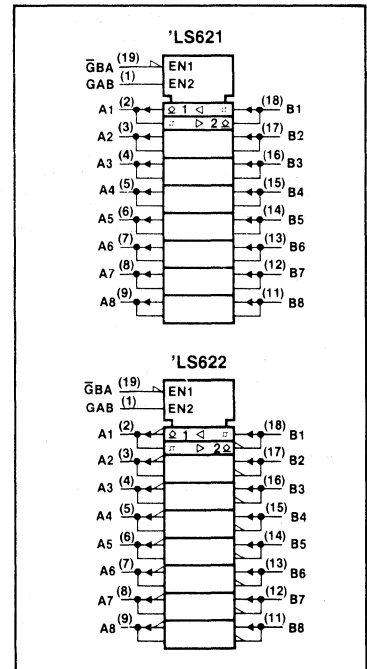
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE)



TRANSCEIVERS

54/74LS621, LS622

Preliminary

FUNCTION TABLE

ENABLE	INPUTS	OPERATION	
		'LS621	'LS622
$\bar{G}BA$	GAB		
L	L	B data to A bus	\bar{B} data to A bus
H	H	A data to B bus	\bar{A} data to B bus
H	L	(Z)	(Z)
L	H	B data to A bus, A data to B bus	\bar{B} data to A bus, \bar{A} data to B bus

H = HIGH voltage level

L = LOW voltage level

(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I_{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

4

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage	Mil			+ 0.5	V
		Com'l			+ 0.6	V
I_{IK}	Input clamp current			- 18	mA	
V_{OH}	HIGH-level output voltage			5.5	V	
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

TRANSCEIVERS

54/74LS621, LS622

Preliminary

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS621, 54/74LS622			UNIT	
		Min	Typ ²	Max		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input	Mil	0.1	0.4	V	
		Com'l	0.2	0.4	V	
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{OH} = 5.5V$			100	μA	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = 12mA$	Mil	0.25	0.4	V
		$I_{OL} = 24mA$	Com'l	0.25	0.4	V
			74LS	0.35	0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$			-1.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 7.0V$			0.1	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7V$			20	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4V$			-0.4	mA	
I_{CC} Supply current ³ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH			70	mA
		I_{CCL} Outputs LOW			90	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$.
- Measure I_{CC} with outputs open.

AC CHARACTERISTICS $T_A = 25^\circ C$, $V_{CC} = 5.0V$

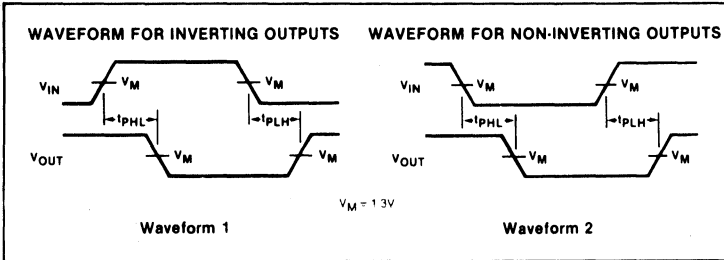
PARAMETER	TEST CONDITIONS	54/74LS621		54/74LS622		UNIT
		$C_L = 45pF$, $R_L = 667\Omega$		$C_L = 45pF$, $R_L = 667\Omega$		
		Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 2, '621	25		25	ns
t_{PHL}	A input to B output					
t_{PLH}	Propagation delay	Waveform 2, '621	25		25	ns
t_{PHL}	B input to A output					
t_{PLH}	Propagation delay G _B A input to A output G _A B input to B output	Waveform 1	40		40	ns
		Waveform 2	40		40	
t_{PHL}	Propagation delay G _B A input to A output G _A B input to B output	Waveform 2	50		60	ns
		Waveform 1	50		60	

TRANSCEIVERS

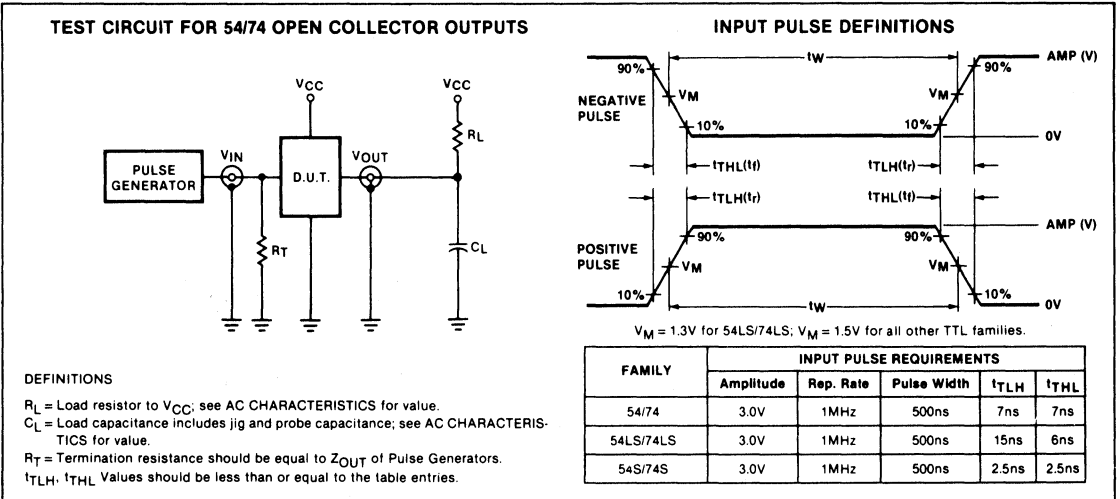
54/74LS621, LS622

Preliminary

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS



4

TRANSCEIVER

54/74LS640, 74LS640-1

Inverting Octal Bus Transceiver (3-State)

- Octal bidirectional bus interface
- Inverting 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability ('LS640-1)

DESCRIPTION

The 'LS640 is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. In addition, the 74LS640-1 features a 48mA sink current capability. The device features a Chip Enable (\overline{CE}) input for easy cascading and a Send/Receive (S/R) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS640 & -1	7ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS640N N74LS640-1N	
Ceramic DIP		S54LS640F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

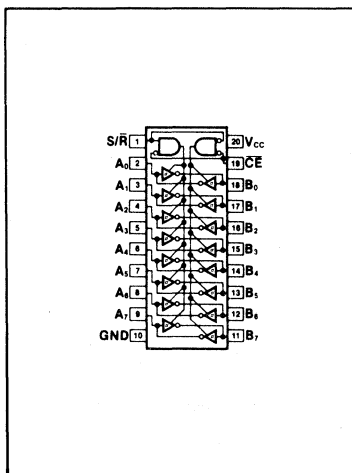
NOTE
A 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL} .

FUNCTION TABLE

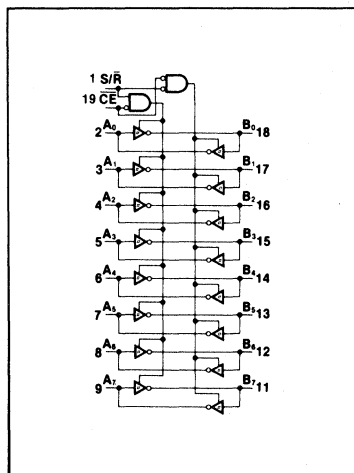
INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/R	A_n	B_n
L	L	$A = \overline{B}$	INPUTS
L	H	INPUTS	$B = \overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

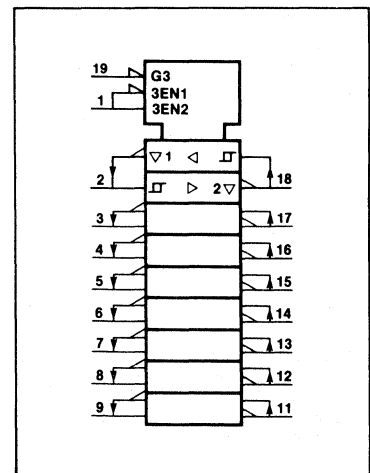
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS & -1	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I _{IN} Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A Operating free-air temperature range	- 55 to + 125	0 to 70	°C

NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74LS & -1			UNIT	
	Min	Nom	Max		
V _{CC} Supply voltage	Mil	4.5	5.0	5.5	V
	Com'l	4.75	5.0	5.25	V
V _{IH} HIGH-level input voltage		2.0			V
V _{IL} LOW-level input voltage	Mil			+ 0.5	V
	Com'l			+ 0.6	V
I _{IK} Input clamp current				- 18	mA
I _{OH} HIGH-level output current	Mil			- 12	mA
	Com'l			- 15	mA
I _{OL} LOW-level output current	Mil			12	mA
	Com'l			24	mA
	74LS-1 only			48	mA
T _A Operating free-air temperature	Mil	- 55		+ 125	°C
	Com'l	0		70	°C

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS
 R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVER

54/74LS640, 74LS640-1

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER	TEST CONDITIONS ¹		54/74LS640			74LS640-1			UNIT		
			Min	Typ ²	Max	Min	Typ ²	Max			
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input		Mil	0.1	0.4				V		
			Com'l	0.2	0.4		0.2	0.4		V	
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$		$I_{OH} = \text{MAX}$	2.0			2.0		V		
			$I_{OH} = -3\text{mA}$	2.4	3.4		2.4	3.4		V	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$		$I_{OL} = 12\text{mA}$	Mil		0.25	0.4			V	
				Com'l		0.25	0.4		0.25	0.4	V
			$I_{OL} = 24\text{mA}$	74LS		0.35	0.5		0.35	0.5	V
									0.4	0.5	V
$I_{OL} = 48\text{mA}$								V			
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$					-1.5		-1.5	V		
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$, \overline{CE} input = 2.0V, $V_O = 2.7\text{V}$					20		20	μA		
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$, \overline{CE} input = 2.0V, $V_O = 0.4\text{V}$					-400		-400	μA		
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$ A or B input				0.1		0.1	mA		
		$V_I = 7.0\text{V}$ $\overline{S/\overline{R}}$ or \overline{CE} input				0.1		0.1	mA		
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$					20		20	μA		
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$					-0.4		-0.4	mA		
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$			-40		-130	-40	-130	mA		
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$		I_{CCH} Outputs HIGH		48	70		48	70	mA	
			I_{CCL} Outputs LOW		62	90		62	90	mA	
			I_{CCZ} Outputs OFF		64	95		64	95	mA	

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
3. I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC\text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

TRANSCEIVER

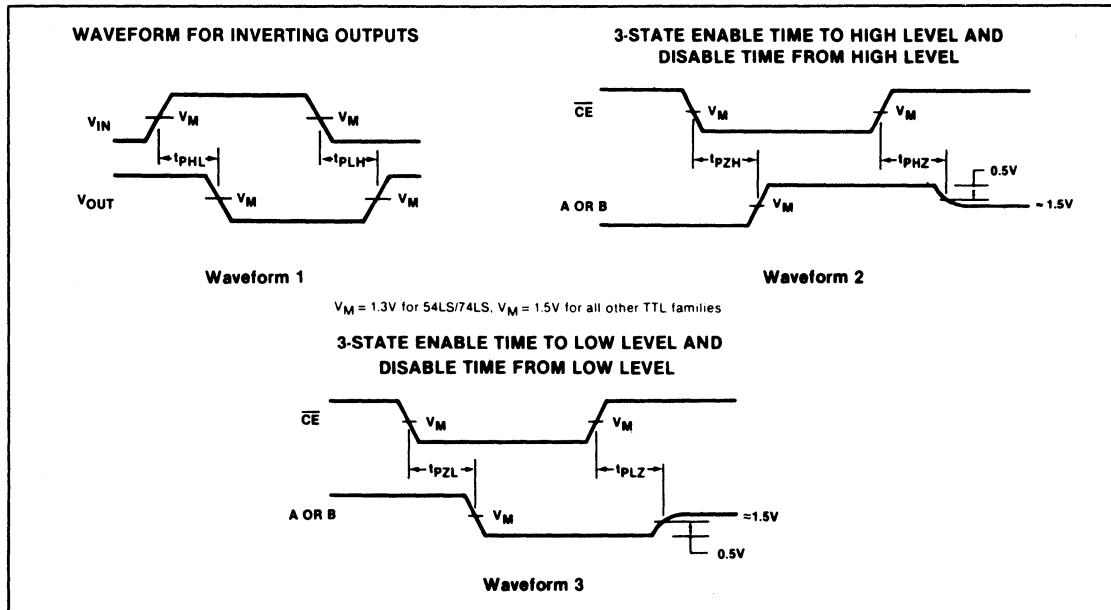
54/74LS640, 74LS640-1

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74LS & -1		UNIT
		$C_L = 45\text{pF}$, $R_L = 667\Omega$		
		Min	Max	
t_{PLH} t_{PHL} Propagation delay A input to B output	Waveform 1		10 15	ns
t_{PLH} t_{PHL} Propagation delay B input to A output	Waveform 1		10 15	ns
t_{PZH} Enable to HIGH \overline{CE} , S/\overline{R} inputs to A output	Waveform 2		40	ns
t_{PZH} Enable to HIGH \overline{CE} , S/\overline{R} inputs to B output	Waveform 2		40	ns
t_{PZL} Enable to LOW \overline{CE} , S/\overline{R} inputs to A output	Waveform 3		40	ns
t_{PZL} Enable to LOW \overline{CE} , S/\overline{R} inputs to B output	Waveform 3		40	ns
t_{PHZ} Disable from HIGH \overline{CE} , S/\overline{R} inputs to A output	Waveform 2, $C_L = 5\text{pF}$		25	ns
t_{PHZ} Disable from HIGH \overline{CE} , S/\overline{R} inputs to B output	Waveform 2, $C_L = 5\text{pF}$		25	ns
t_{PLZ} Disable from LOW \overline{CE} , S/\overline{R} inputs to A output	Waveform 3, $C_L = 5\text{pF}$		25	ns
t_{PLZ} Disable from LOW \overline{CE} , S/\overline{R} inputs to B output	Waveform 3, $C_L = 5\text{pF}$		25	ns

4

AC WAVEFORMS



TRANSCEIVERS

54/74LS641, LS642, 74LS641-1, LS642-1

Octal Bus Transceiver (Open Collector)

- Octal bidirectional bus interface
- Open Collector Outputs
 - 'LS641, non-inverting
 - 'LS642, inverting
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability ('LS641-1, LS642-1)

FUNCTION TABLE, 'LS641

INPUTS		INPUTS/OUTPUTS	
CE	S/R	A _n	B _n
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	(Z)	(Z)

FUNCTION TABLE, 'LS642

INPUTS		INPUTS/OUTPUTS	
CE	S/R	A _n	B _n
L	L	A = \bar{B}	INPUTS
L	H	INPUTS	B = \bar{A}
H	X	(Z)	(Z)

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance "off" state

TYPE	TYPICAL PROPAGATION DELAY (A to B)	TYPICAL SUPPLY CURRENT (Total)
74LS641 & -1	17ns	58mA
74LS642 & -1	17ns	58mA

ORDERING CODE

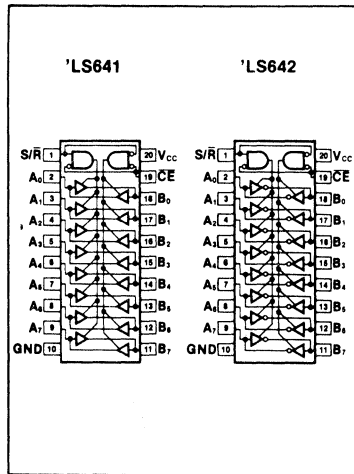
PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to +70°C	V _{CC} = 5V ± 10%; T _A = -55°C to +125°C
Plastic DIP	N74LS641N N74LS641-1N N74LS642N N74LS642-1N	
Ceramic DIP		S54LS641F S54LS642F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

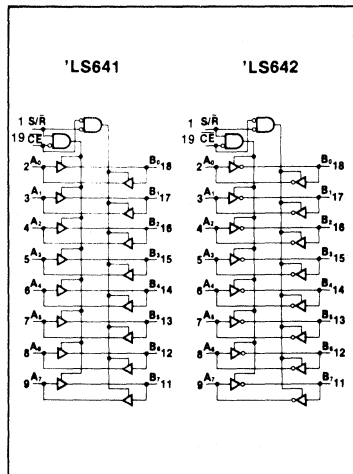
PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
 A 54/74LS unit load (LSul) is 20 μ A I_{IH} and -0.4mA I_{IL}.

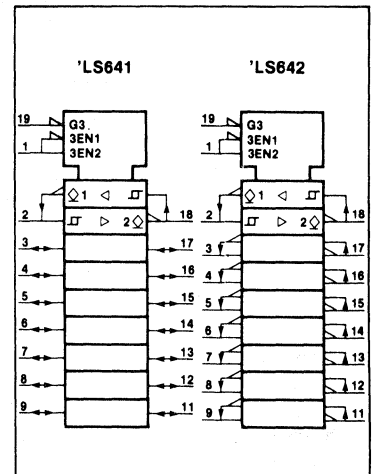
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVERS

54/74LS641, LS642, 74LS641-1, LS642-1

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS & -1	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I _{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

NOTE
V_{IN} limited to 5.5V on A and B inputs only.

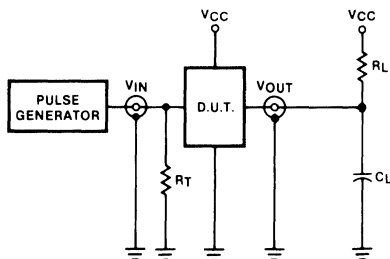
RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS & -1			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V	
V _{IL}	LOW-level input voltage	Mil			+ 0.5	V
		Com'l			+ 0.6	V
I _{IK}	Input clamp current			- 18	mA	
V _{OH}	HIGH-level output voltage			5.5	V	
I _{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
		74LS-1 only			48	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

4

TEST CIRCUITS AND WAVEFORMS

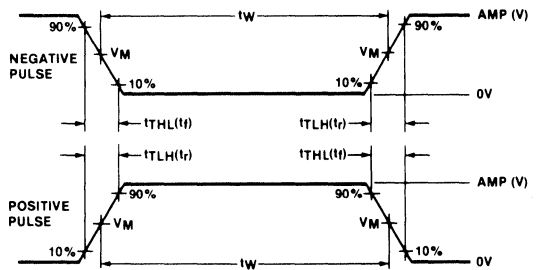
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVERS

54/74LS641, LS642, 74LS641-1, LS642-1

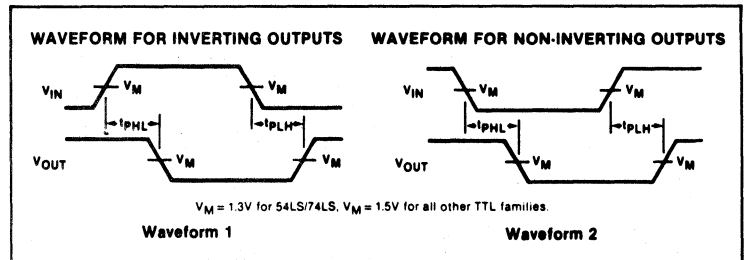
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER	TEST CONDITIONS ¹		54/74LS641			74LS641-1			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input	Mil	0.1	0.4					V	
		Com'l	0.2	0.4		0.2	0.4		V	
I_{OH} HIGH-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{OH} = 5.5V$				100			100	μA	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = 12mA$	Mil		0.25	0.4				V
			Com'l		0.25	0.4		0.25	0.4	V
		$I_{OL} = 24mA$	74LS		0.35	0.5		0.35	0.5	V
								0.4	0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$				-1.5			-1.5	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5V$ A or B input			0.1			0.1	mA	
		$V_I = 7.0V$ S/ \bar{R} or \bar{CE} input			0.1			0.1	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7V$				20			20	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4V$				-0.4			-0.4	mA	
I_{CC} Supply current ³ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH		48	70		48	70	mA	
		I_{CCL} Outputs LOW		62	90		62	90	mA	
		I_{CCZ} Outputs OFF		64	95		64	95	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$
- Measure I_{CC} with outputs open.

AC WAVEFORMS



AC CHARACTERISTICS $T_A = 25^\circ C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	$C_L = 45pF$, $R_L = 667\Omega$		UNIT
		Min	Max	
t_{PLH} Propagation delay t_{PHL} A input to B output	Waveform 1		25	ns
t_{PLH} Propagation delay t_{PHL} B input to A output	Waveform 1		25	ns
t_{PLH} Propagation delay \bar{CE} , S/ \bar{R} inputs to A output \bar{CE} input to B output S/ \bar{R} input to B output	Waveform 1		40	ns
	Waveform 1		40	
	Waveform 2		40	
t_{PHL} Propagation delay \bar{CE} , S/ \bar{R} inputs to A output \bar{CE} input to B output S/ \bar{R} input to B output	Waveform 2		50	ns
	Waveform 2		50	
	Waveform 1		50	

TRANSCEIVER

54/74LS645, 74LS645-1

Octal Bus Transceiver (3-State)

- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability ('LS645-1)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS645 & -1	10ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N74LS645N N74LS645-1N	
Ceramic DIP		S54LS645F

DESCRIPTION

The 'LS645 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. In addition, the 74LS645-1 features a 48mA sink current capability. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

NOTE

A 54/74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
CE	S/R	A _n	B _n
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	(Z)	(Z)

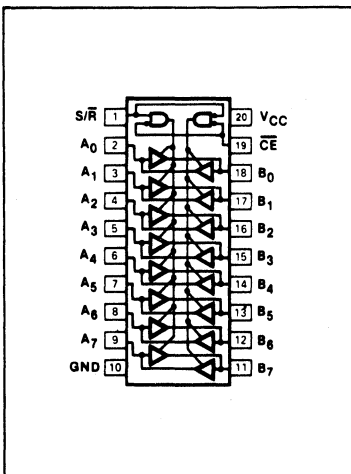
H = HIGH voltage level

L = LOW voltage level

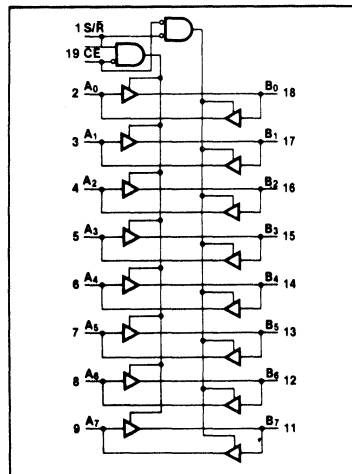
X = Don't care

(Z) = HIGH impedance "off" state

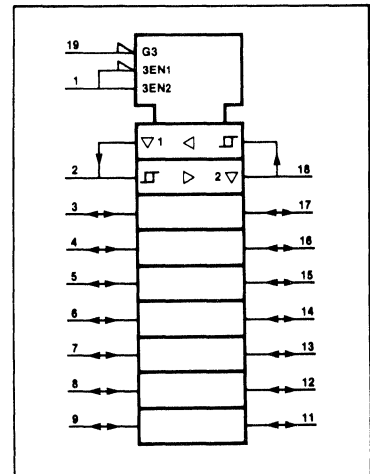
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVER

54/74LS645, 74LS645-1

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	54LS	74LS & -1	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I _{IN} Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A Operating free-air temperature range	- 55 to + 125	0 to 70	°C

NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	54/74LS & -1			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	Mil	4.5	5.5	V
	Com'l	4.75	5.25	V
V _{IH} HIGH-level input voltage	2.0			V
V _{IL} LOW-level input voltage	Mil	+ 0.5		V
	Com'l	+ 0.6		V
I _{IK} Input clamp current				- 18 mA
I _{OH} HIGH-level output current	Mil	- 12		mA
	Com'l	- 15		mA
I _{OL} LOW-level output current	Mil	12		mA
	Com'l	24		mA
	74LS-1 only	48		mA
T _A Operating free-air temperature	Mil	- 55	+ 125	°C
	Com'l	0	70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS
 R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

TRANSCEIVER

54/74LS645, 74LS645-1

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER	TEST CONDITIONS ¹		54/74LS645			74LS645-1			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$, A or B input		Mil	0.1	0.4				V	
			Com'l	0.2	0.4		0.2	0.4	V	
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OH} = \text{MAX}$		2.0			2.0		V	
		$I_{OH} = -3\text{mA}$		2.4	3.4		2.4	3.4	V	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = 12\text{mA}$	Mil		0.25	0.4			V	
			Com'l		0.25	0.4	0.25	0.4	V	
		$I_{OL} = 24\text{mA}$		74LS		0.35	0.5	0.35	0.5	V
		$I_{OL} = 48\text{mA}$						0.4	0.5	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$					-1.5		-1.5	V	
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}$, \overline{CE} input = 2.0V, $V_O = 2.7\text{V}$					20		20	μA	
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}$, \overline{CE} input = 2.0V, $V_O = 0.4\text{V}$					-400		-400	μA	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$	A or B input			0.1		0.1	mA	
		$V_I = 7.0\text{V}$	S/R or \overline{CE} input			0.1		0.1	mA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7\text{V}$					20		20	μA	
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4\text{V}$					-0.4		-0.4	mA	
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$			-40		-130	-40	-130	mA	
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	I_{CCH} Outputs HIGH			48	70		48	70	mA
		I_{CCL} Outputs LOW			62	90		62	90	mA
		I_{CCZ} Outputs OFF			64	95		64	95	mA

- NOTES
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 - All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
 - I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 - Measure I_{CC} with outputs open.

4

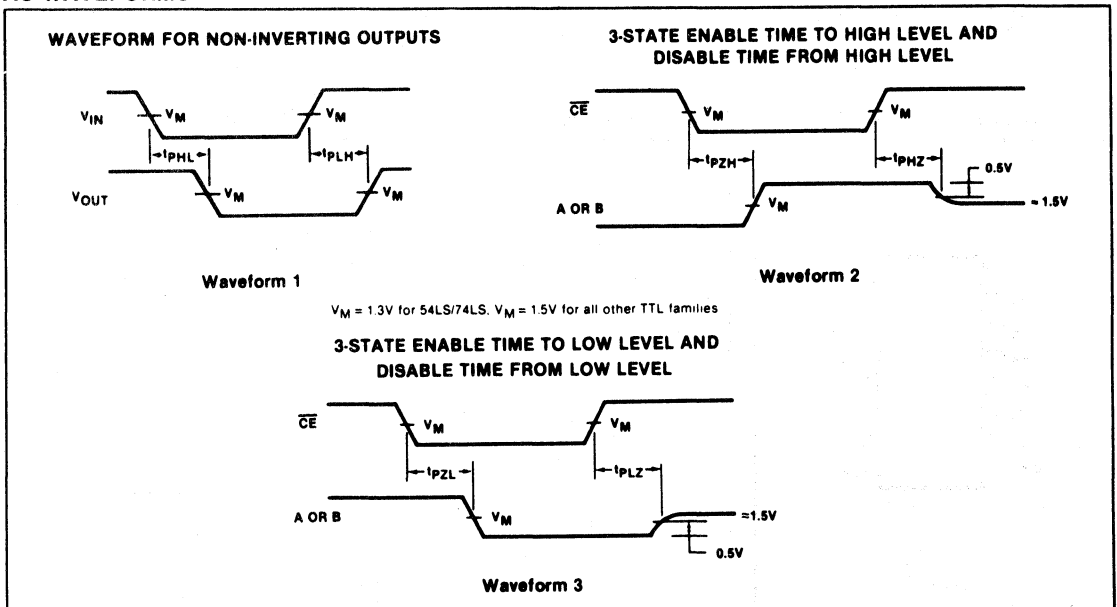
TRANSCEIVER

54/74LS645, 74LS645-1

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54/74LS & -1		UNIT
		$C_L = 45\text{pF}$, $R_L = 687\Omega$		
		Min	Max	
t_{PLH} t_{PHL} Propagation delay A input to B output	Waveform 1		15 15	ns
t_{PLH} t_{PHL} Propagation delay B input to A output	Waveform 1		15 15	ns
t_{PZH} Enable to HIGH CE, S/R inputs to A output	Waveform 2		40	ns
t_{PZH} Enable to HIGH CE, S/R inputs to B output	Waveform 2		40	ns
t_{PLZ} Enable to LOW CE, S/R inputs to A output	Waveform 3		40	ns
t_{PLZ} Enable to LOW CE, S/R inputs to B output	Waveform 3		40	ns
t_{PHZ} Disable from HIGH CE, S/R inputs to A output	Waveform 2, $C_L = 5\text{pF}$		25	ns
t_{PHZ} Disable from HIGH CE, S/R inputs to B output	Waveform 2, $C_L = 5\text{pF}$		25	ns
t_{PLZ} Disable from LOW CE, S/R inputs to A output	Waveform 3, $C_L = 5\text{pF}$		25	ns
t_{PLZ} Disable from LOW CE, S/R inputs to B output	Waveform 3, $C_L = 5\text{pF}$		25	ns

AC WAVEFORMS



REGISTER FILE

54/74LS670

4 x 4 Register File (3-State)

- Simultaneous and Independent Read and Write operations
- Expandable to almost any word size and bit length
- 3-State outputs
- See '170 for open collector version

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS670	25ns	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = -55°C to + 125°C
Plastic DIP	N74LS670N	
Ceramic DIP	S54LS670F	
Flatpack	S54LS670W	
LLCC	S54LS670G	

DESCRIPTION

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable (\overline{WE}) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the \overline{WE} is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when \overline{WE} is HIGH.

Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable (\overline{RE}) is

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
D ₀ -D ₃ , W _A , W _B , R _A , R _B	Inputs	1LSuI
\overline{WE}	Input	2LSuI
\overline{RE}	Input	3LSuI
Q ₀ -Q ₃	Outputs	10LSuI

NOTE

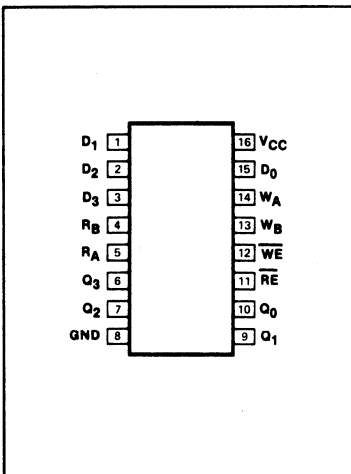
A 54/74LS unit load (LSuI) is 20μA I_{IH} and -0.4mA I_{IL}.

LOW. Data outputs are in the HIGH impedance "off" state when the Read Enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

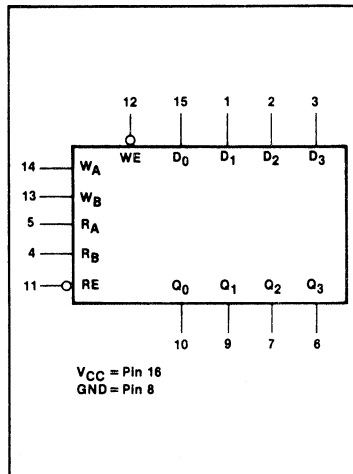
Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible

by tying pull-up resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

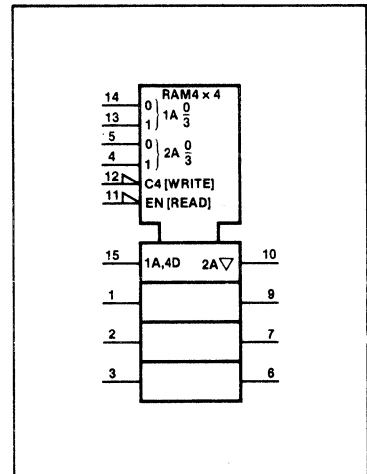
PIN CONFIGURATION



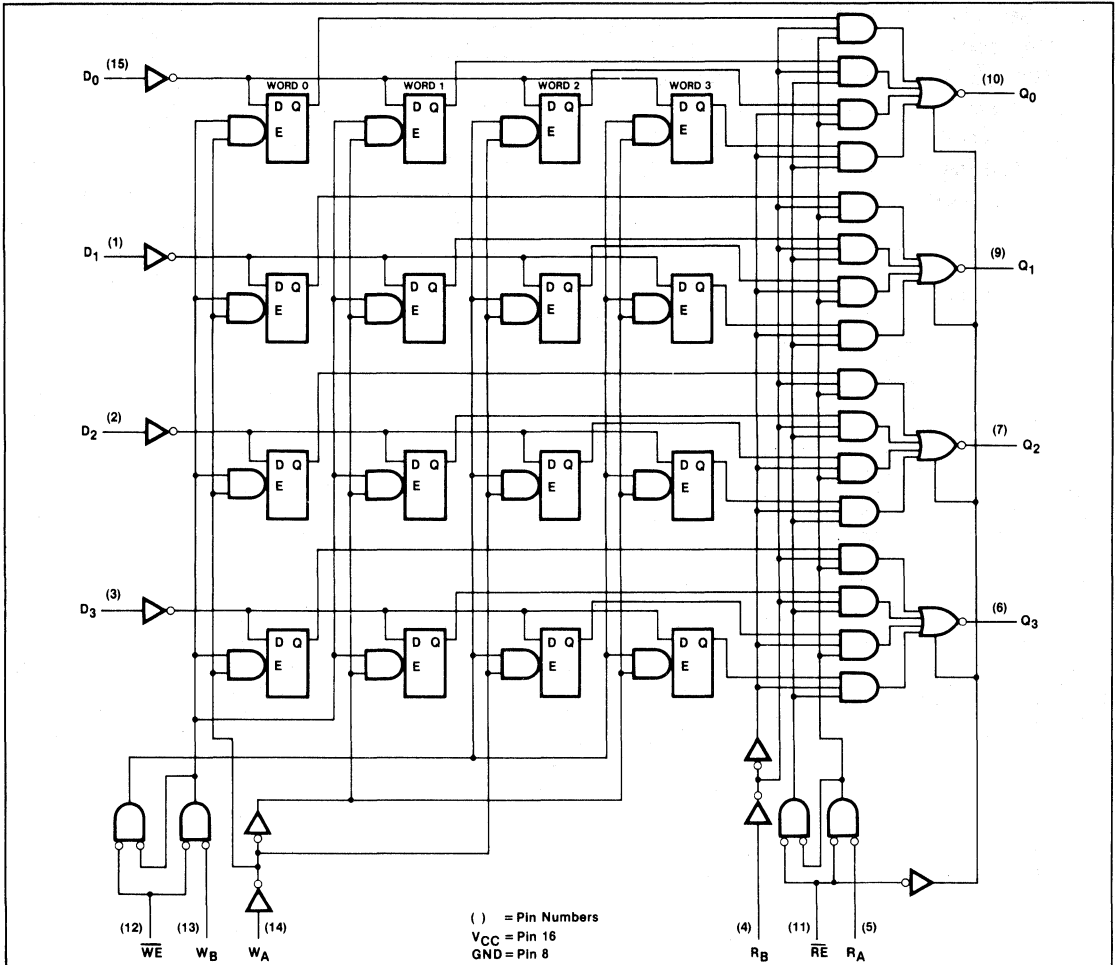
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES ^(a)
	\overline{WE}	D _n	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE

a. The Write Address (W_A and W_B) to the "internal latches" must be stable while \overline{WE} is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT Q _n
	\overline{RE}	INTERNAL LATCHES ^(b)	
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

NOTE

b. The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by \overline{WE} or \overline{RE} operation.

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance "off" state.

REGISTER FILE

54/74LS670

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I_{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				- 18	mA
I_{OH}	HIGH-level output current	Mil			- 1.0	mA
		Com'l			- 2.6	mA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

4

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS670			UNIT	
		Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.4	V	
		Com'l	2.4	3.1	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	Mil	0.25	0.4	V
			Com'l	0.35	0.5	V
		I _{OL} = 4mA	74LS	0.25	0.4	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			- 1.5	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 2.7V			20	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 0.4V			- 20	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 7.0V	D ₀ -D ₃ , W _A , W _B , R _A , R _B inputs			0.1	mA
		WE input			0.2	mA
		RE input			0.3	mA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V	D ₀ -D ₃ , W _A , W _B , R _A , R _B inputs			20	μA
		WE input			40	μA
		RE input			60	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V	D ₀ -D ₃ , W _A , W _B , R _A , R _B inputs			- 0.4	mA
		WE input			- 0.8	mA
		RE input			- 1.2	mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	- 20		- 100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		30	50	mA	

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with 4.5V applied to all Data inputs and Read Enable and Write Enable inputs, ground Read Address and Write Address inputs and leave all outputs open. This is a worst-case condition.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		C _L = 15pF, R _L = 2kΩ		
		Min	Max	
t _{PLH} Propagation delay	Waveform 2		40	ns
t _{PHL} Read Address to output			45	
t _{PLH} Propagation delay	Waveform 1		45	ns
t _{PHL} Write Enable to output			50	
t _{PLH} Propagation delay	Waveform 1		45	ns
t _{PHL} Data to output			40	
t _{PZH} Enable time to HIGH level	Waveform 4		35	ns
t _{PZL} Enable time to LOW level	Waveform 5		40	ns
t _{PHZ} Disable time from HIGH level	Waveform 4, C _L = 5pF		50	ns
t _{PLZ} Disable time from LOW level	Waveform 5, C _L = 5pF		35	ns

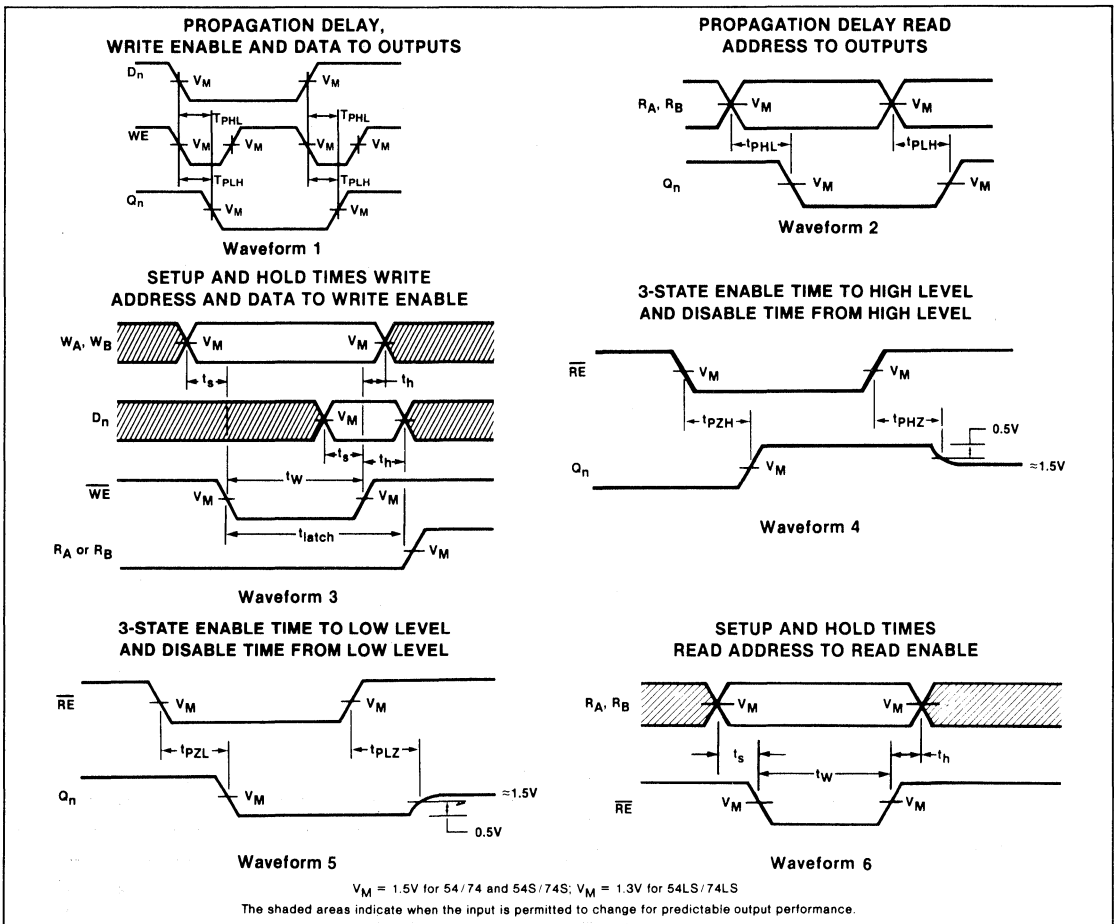
AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
t_W Read Enable pulse width	Waveform 6	25		ns
t_W Write Enable pulse width	Waveform 3, $\overline{RE} = \leq 0.8\text{V}$	25		ns
t_s Setup time, Data to positive-going $\overline{WE}^{(c)}$	Waveform 3	10		ns
t_h Hold time, Data to positive-going $\overline{WE}^{(c)}$	Waveform 3	15		ns
t_s Setup time, Write Address to negative-going $\overline{WE}^{(c)}$	Waveform 3	15		ns
t_h Hold time, Write Address to negative-going $\overline{WE}^{(d)}$	Waveform 3	5.0		ns
t_{latch} Latch time for new data ^(d)	Waveform 3	25		ns

NOTES

- c. Write address setup time will protect the data written into the previous address. If protection of data in the previous address is not required, t_s (write address to \overline{WE}) can be ignored, as any address selection sustained for the final 30ns of the \overline{WE} pulse and during t_h (write address to \overline{WE}) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
- d. Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of \overline{WE} to the rising edge of R_A or R_B . \overline{RE} must be LOW.

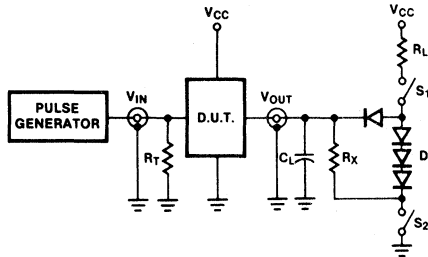
AC WAVEFORMS



4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



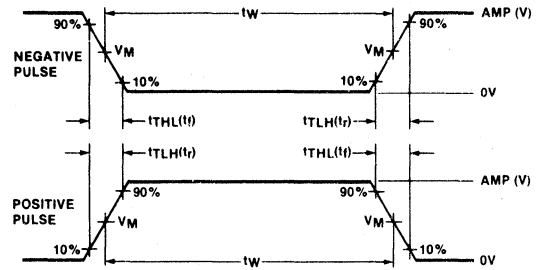
SWITCH POSITION

Test	Switch 1	Switch 2
t _{PZH}	Open	Closed
t _{PZL}	Closed	Open
t _{PHZ}	Closed	Closed
t _{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

RAM CONTROLLER

54/74LS764

Preliminary

Dual-Port Dynamic RAM Controller

FEATURES

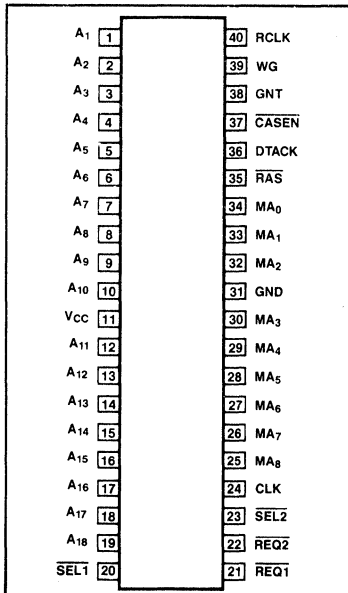
- Arbitration for 2 microprocessors, refresh, RAS/CAS generation, access ready timing and address multiplexing with a single 40-pin chip
- Nine address pins allow control of DRAMs up to 256K
- Convenient pinout and other support chips on the right
- Separate refresh clock allows adjustable refresh timing

DESCRIPTION

The 74LS764 Dual-Port Dynamic RAM controller is a 40-pin, bipolar, memory controller designed to perform the functions of arbitrator, access signal controller, and refresher for interfacing industry standard Dynamic RAMs to at most two processors, known as 'users'. The number of address lines inter-faceable to the controlled DRAMs (18) indicates that the LS764 will control DRAMs of up to 256K in size, with the number of 256K banks of controlled DRAM limited by the output capability of the RAS, CASEN, and the MA0-8 address lines.

The CP input determines the speed at which the controller will function, with a suggested limit of 50 MHz. The RCP input determines the period of refresh for each row after it is divided by 50 internally.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS764		175 mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C	V _{CC} = 5V ± 10%; T _A = -55°C to + 125°C
Plastic DIP	N74LS764N	
Plastic SO	N74LS764D	
Ceramic DIP		
Ceramic LLC		

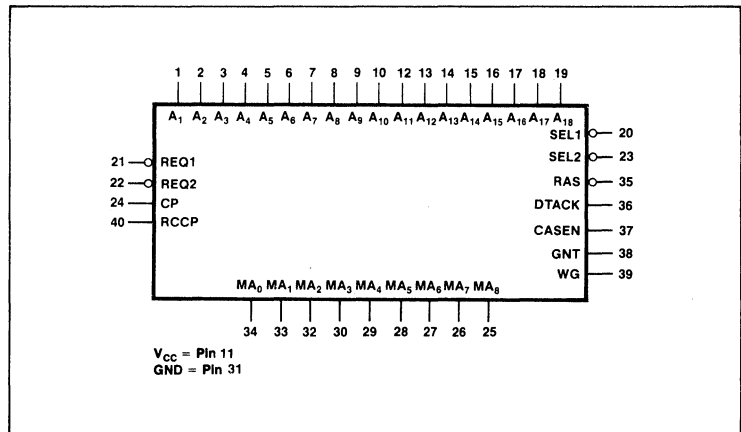
NOTE:

SO Package is surface mounted micro-miniature DIP available 1984.
LLCC is 20 pin surface mounted leadless chip carrier.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F/74 (U.L.) High/Low
REQ1, REQ2	Request Inputs (Active Low)	
CP	Clock Input	
RCP	Refresh Clock Input	
A1-A18	Address Inputs	
GNT	Grant Output (Active High)	
SEL1, SEL2	Select Outputs (Active Low)	
DTACK	Data Transfer Acknowledge Output	
RAS	Row Address Select Output	
WG	Write Gate Output	
CASEN	Column Access Select Enable Output	
MA0-MA8	Address Outputs	

LOGIC SYMBOL



4

RAM CONTROLLER

54/74LS764

Preliminary

Access to the controlled DRAM is accomplished by bringing one of the two REQ inputs low. Initial arbitration indicates on the SEL outputs which user will be granted access next, after the current cycle (access or refresh) is completed. When the current cycle is completed, the GNT output is brought high to indicate that a memory access cycle is now commencing for the selected user. This GNT signal, when decoded with the proper SEL output, can be used as a wait signal for some popular microprocessors. Once the GNT signal has become true, the address inputs A1-A18 are latched internally, and A1-A9 are propagated to the MA0-8 outputs. One-half CP cycle later, the RAS output becomes active, and at the next half-cycle of CP, the address lines A10-A18 are selected and propagated to the MA0-8 outputs, and the WG output (WRITE GATE) becomes active, indicating the proper time for WE going to the DRAMs to become active for an 'EARLY WRITE' cycle. This WG signal, when used with the SEL signal, can be used to gate in the WR signal coming from the user to produce a proper WE signal for the DRAMs. After 1/2 CP cycle allows the address to propagate and stabilize, the

CASEN output becomes active, which can be used as a CAS output or decoded with higher order address lines to produce multiple CAS signals.

After the CASEN signal has become active, 3 CP cycles occur before RAS is turned off, giving a total pulse width for RAS of 4 CP cycles. At the same time, the DTACK output becomes active, indicating that data is valid on the DRAM data lines, or that proper access time has been reached, indicating to the user that it can now commence to withdraw its request. All signal lines are held in this state until the user finally brings its REQ input high, at which time, after synchronization, the GNT, SEL and other signals become inactive and a new access or refresh cycle is serviced.

The refresh cycle commences from internal requests generated from the CP divided by 50 to produce a refresh request every 12.5 μ sec when using a 4 MHz RCP. In this cycle the internal refresh counter addresses are allowed to propagate and settle on the MA0-8 address outputs, at which time the RAS signal becomes active for 4 CP cycles, then inactive for 3 CP cycles, to meet the

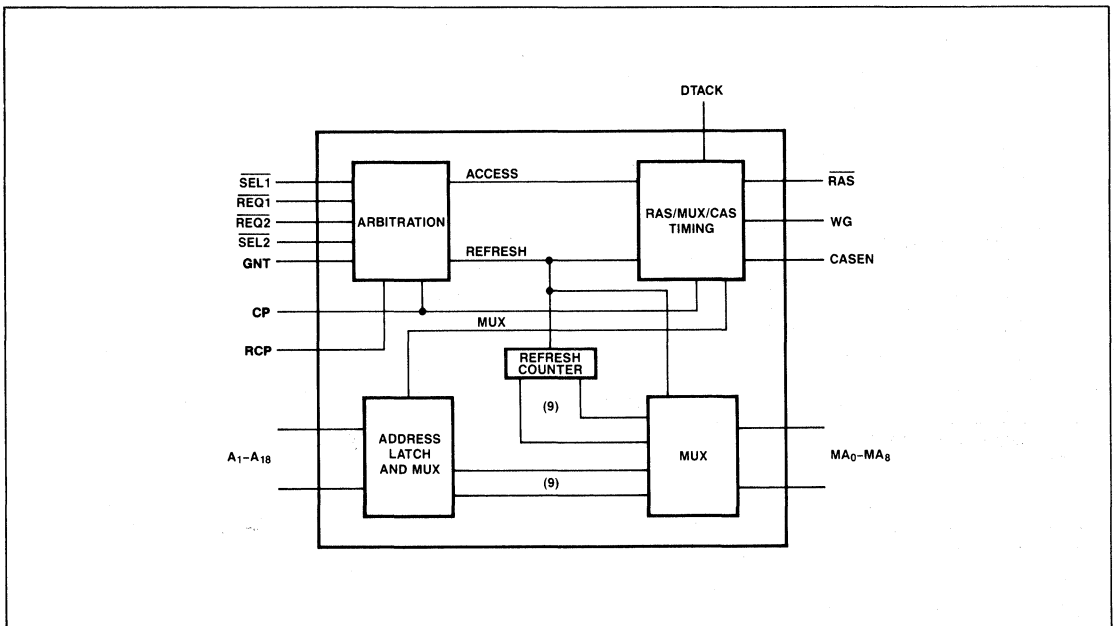
precharge requirement of DRAMs. This refresh request takes priority over the two REQ inputs, except when one of them is in the process of being serviced when the refresh request comes active. In that case the refresh cycle would start immediately after the current user is serviced.

REQ contention is resolved by sampling the REQ inputs on different edges of the CP, which resolves the problem of Requests coming simultaneously, but also introduces a delay of up to 1 CP cycle for resolution.

The RAS, CASEN, and MA0-8 address line outputs have 48 mA outputs and a 'slow ramp' feature to promote proper interfacing to standard DRAM inputs. The outputs are specified to handle up to 256 pF without degradation of control and minimal degradation of access time. Indicating at the present time a limit of 32 devices connected to any one pin (8 pF load per input).

The LS764 will be housed in a 40-pin DIP, with specifications made in the commercial range.

BLOCK DIAGRAM



RAM CONTROLLER

54/74LS764

Preliminary

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54LS	74LS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I _{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74LS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V	
V _{IL}	LOW-level input voltage	Mil		+ 0.7	V	
		Com'l		+ 0.8	V	
I _{IK}	Input clamp current			- 18	mA	
I _{OH}	HIGH-level output current			- 400	μA	
I _{OL}	LOW-level output current	Mil		4	mA	
		Com'l		8	mA	
T _A	Operating free-air temperature	Mil	- 55	+ 125	°C	
		Com'l	0	70	°C	

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	54/74LS			UNIT
		Min	Typ ²	Max	
V _{OH}	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.5		V
		Com'l	2.7		V
V _{OL}	V _{CC} = MIN, V _{IN} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.4	V
			Com'l	0.5	V
		I _{OL} = 4mA	74LS		0.4
V _{IK}	V _{CC} = MIN, I _I = I _{IK}			- 1.5	V
I _I	V _{CC} = MAX, V _I = 7.0V			0.5	mA
I _{IH}	V _{CC} = MAX, V _I = 2.7V			20	μA
I _{IL}	V _{CC} = MAX, V _I = 0.4V			- 0.2	mA
I _{OS}	V _{CC} = MAX	- 15		- 100	mA
I _{CC}	V _{CC} = MAX		175	200	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

RAM CONTROLLER

54/74LS764

Preliminary

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		
		Min	Max	
t_{SEL1} SELECT 1 TIME (REQ1 to SEL1)	Waveform 1	$t_s + 25$	user 2 time + $1 T_{CP} + 25$	ns
t_{SEL2} SELECT 2 TIME (REQ2 to SEL2)		$t_s + 25$	user 1 time + $1 T_{CP} + 25$	ns
t_{GNT1} GRANT 1 TIME (SEL1 to GNT1)		$t_{WCP(H)}$	$7.5 T_{CP}$	ns
t_{GNT2} GRANT 2 TIME (SEL2 to GNT1)		$1 T_{CP}$	$8 T_{CP}$	ns
t_{GRA} GNT to ROW ADDRESS			24	ns
t_{GRAS} GNT to $\overline{\text{RAS}}$			$t_{WCP(L)} + 24$	ns
t_{GWG} GNT to WG			$1 T_{CP}$	ns
t_{GCA} GNT to COLUMN ADDRESS			$1 T_{CP} + 24$	ns
t_{GCAS} GNT to $\overline{\text{CASEN}}$			$1.5 T_{CP} + 21$	ns
t_{GDT} GNT to DTACK			$4.5 T_{CP}$	ns
t_{REFREQ} REFRESH REQUEST CLOCK PERIOD			$50 T_{RCP}$	ns
t_{WRAS} $\overline{\text{RAS}}$ PULSE WIDTH			$4.0 T_{CP}$	ns

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

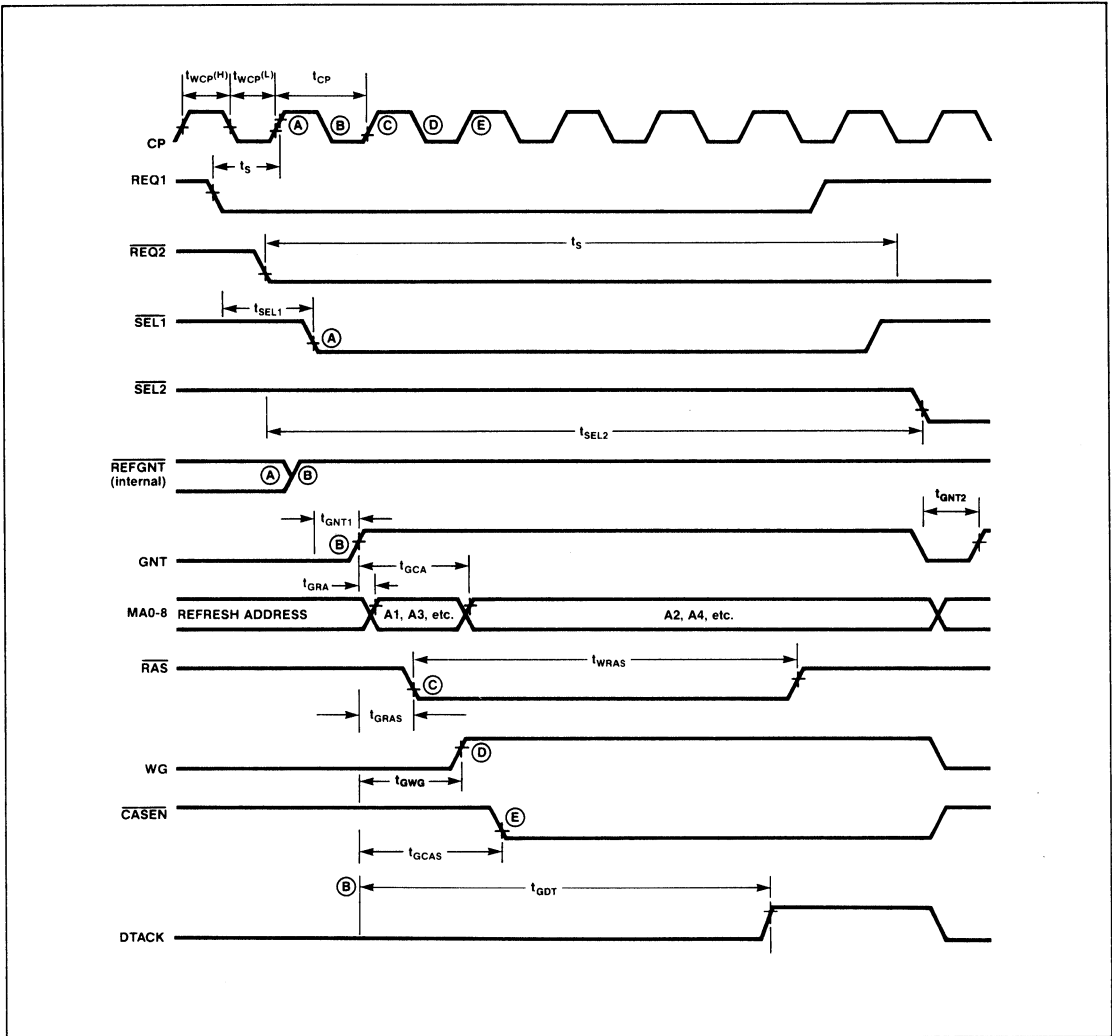
PARAMETER	TEST CONDITIONS	54LS/74LS		UNIT
		Min	Max	
$t_{WCP(H)}$ CP Pulse width (H)	Waveform 1	12.5		ns
$t_{WCP(L)}$ CP Pulse width (L)		12.5		ns
$t_{WRCP(H)}$ RCP Pulse width (H)		12.5		ns
$t_{WRCP(L)}$ RCP Pulse width (L)		12.5		ns
t_s SET-UP TIME (REQ to CLOCK)		8		ns
t_h HOLD TIME (REQ from CLOCK)		0		ns
t_{CP} One Clock Period of CP		25		ns
t_{RCP} One Clock Period of RCP		25		ns

NOTES

1. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

Preliminary

AC WAVEFORMS



4

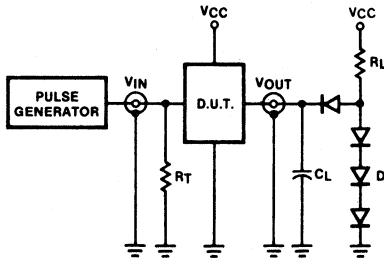
RAM CONTROLLER

54/74LS764

Preliminary

TEST CIRCUITS AND WAVEFORMS

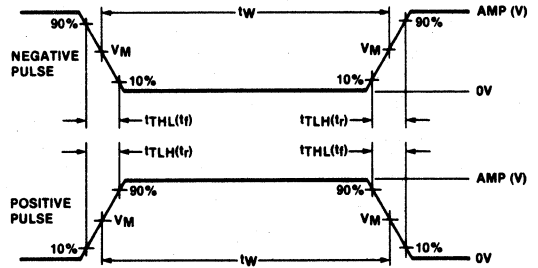
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

- R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
- D = Diodes are 1N916, 1N3064, or equivalent.
- t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Section 5

8T Series

QUAD BUS DRIVER

8T09

3-State Quad Bus Driver

- High speed
- Quad bus driver
- 40 mA Low-state drive
- 300 pF load driving capability

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T09	7 ns	

DESCRIPTION

The 8T09 is a high speed quad bus driver device for applications requiring up to 25 loads interconnected on a single bus.

The tri-state outputs present a high impedance to the bus when disabled (control input "1"), and active drive when enabled (control input "0"). This eliminates the resistor pull-up requirement while providing performance superior to open collector schemes. Each output can sink 40 mA and drive 300 pF loading with guaranteed propagation delay less than 20 nanoseconds.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T09N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
DATA	Input	1 ul
DISABLE	Input	1 ul
3, 6, 8, 11	Output	10 ul

NOTE

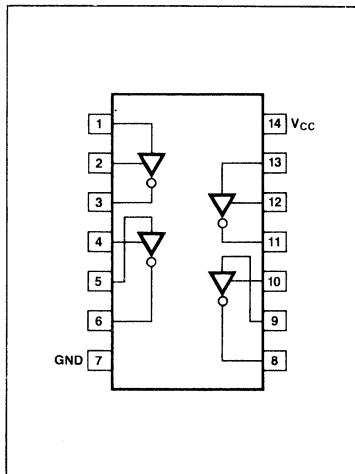
A unit load (ul) is 40 μA I_{IH} and -1.6 mA I_{IL} .

FUNCTION TABLE

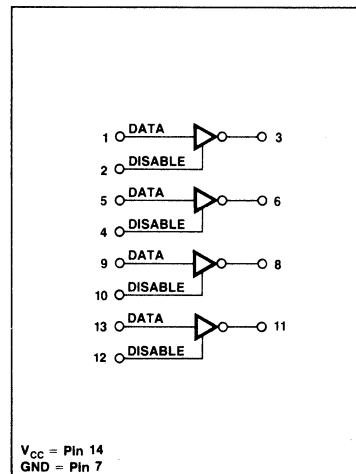
DATA	DISABLE	OUTPUT
0	0	1
1	0	0
0	1	Hi-Z
1	1	Hi-Z

5

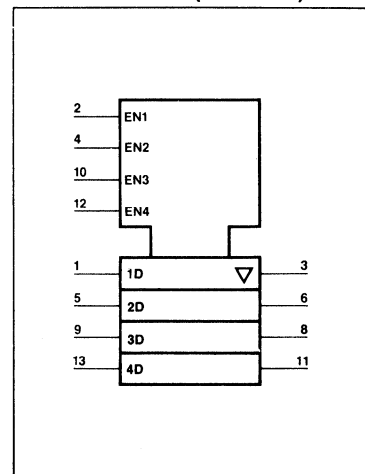
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



QUAD BUS DRIVER**8T09****ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			0.8	V
I _{IK}	Input clamp current			- 12	mA
I _{OH}	HIGH-level output current			- 5.2	mA
I _{OL}	LOW-level output current			40	mA
T _A	Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹	8T09		UNIT
		Min	Max	
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12 mA		V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = - 5.2 mA		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 40 mA		V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5 V		μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V		mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX		mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V		mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

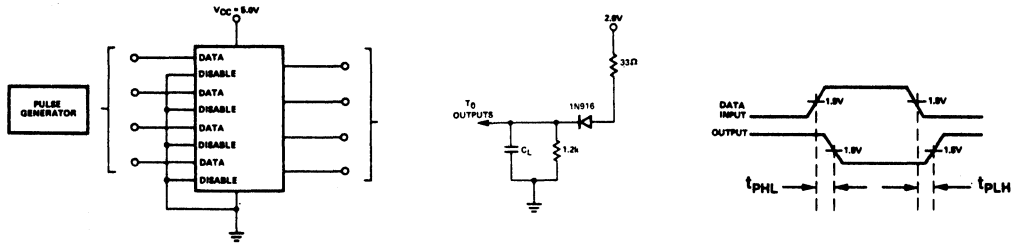
2. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	Min	Max	UNIT
t _{PLH}	Propagation delay	Figure 1	CL = 30 pF	ns
t _{PHL}	Data to output			
t _{PZH}	Enable to HIGH	Figure 3	CL = 30 pF CL = 300 pF	ns
t _{PZL}	Enable to LOW	Figure 2	CL = 30 pF CL = 300 pF	ns
t _{PHZ}	Disable from HIGH	Figure 3	CL = 30 pF CL = 300 pF	ns
t _{PLZ}	Disable from LOW	Figure 2	CL = 30 pF CL = 300 pF	ns

AC TEST FIGURES AND WAVEFORMS

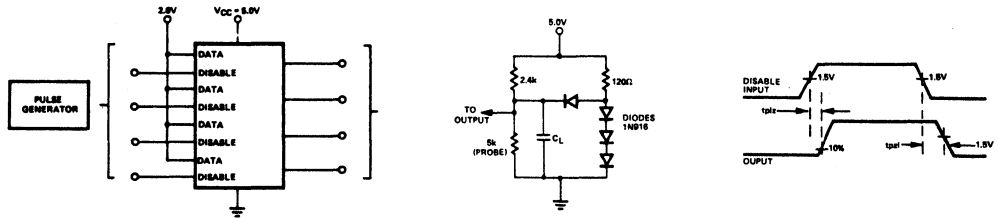
PROPAGATION DELAY (DATA TO OUTPUT)



INPUT PULSE:
 $t_r = t_f = 5ns$ (10% TO 90%)
 FREQ. = 1MHz (50% DUTY CYCLE)
 AMP. = 2.6V

FIGURE 1

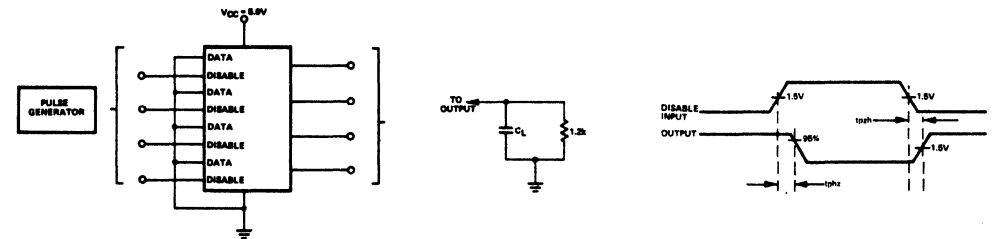
PROPAGATION DELAY ("0" TO HIGH Z, t_{pLz} ; HIGH Z TO 0, t_{pZL})



INPUT PULSE:
 $t_r = t_f = 5ns$ (10% TO 90%)
 FREQ. = 200kHz
 AMP. = 2.6V

FIGURE 2

PROPAGATION DELAY ("1" TO HIGH Z, t_{pHz} ; HIGH Z TO "1", t_{pZH})



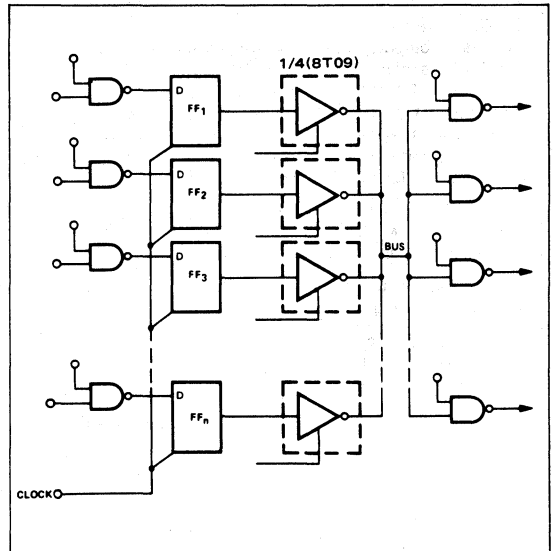
INPUT PULSE:
 $t_r = t_f = 5ns$ (10% TO 90%)
 FREQ. = 200kHz
 AMP. = 2.6V

FIGURE 3

5

The figure to right illustrates usage of the 8T09 in data processing logic. For example, FF_1 thru FF_n may represent bit X in each of several functions in a minicomputer (accumulators, MQ register, index registers, indirect address registers, etc.). Transfer from any source to any load, including transfers from one register to another, can take place along the single path labeled "BUS".

TYPICAL APPLICATION



BUS FLIP-FOP

8T10

3-State Quad D-Type Bus Flip-Flop

DESCRIPTION

The 8T10 is a high speed Quad D flip-flop with tri-state outputs for use in bus-organized systems. The high current sink capability permits up to 20 standard loads to be interconnected on a single bus. The outputs present a high impedance to the bus when disabled (Control Input "1") and active drive when enabled (Control Inputs "0").

All four D-type flip-flops operate from a common clock with data being transferred on the low-to-high transition of the pulse.

A master reset input resets all flip-flops upon application of a logic "1" level.

Data will be stored if either one or both inputs to the Input Disable NOR gate is a logic "1".

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T10	24 ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{cc} = 5V ± 5%; T _A = 0°C to + 70°C
Plastic DIP	N8T10N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
D _n , CP	Input	1 ul
E _n , MR, 0E _n	Input	1.2 ul
Q _n	Output	10 ul

NOTE

A unit load (ul) is 40μA I_{IH} and -1.6 mA I_{IL}.

FUNCTION TABLE

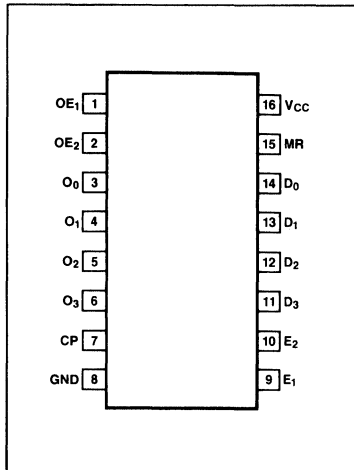
D _n	E	0E	Q _{n+1}
0	0	0	0
1	0	0	1
X	1	0	Q _n
X	X	1	High Z

NOTES:

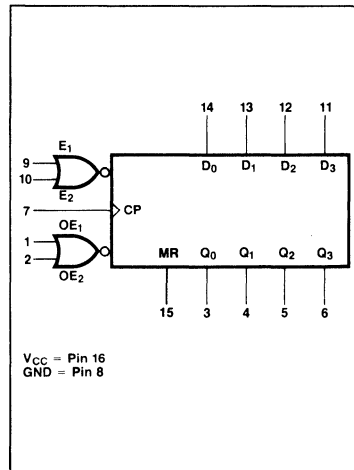
1. Q_n refers to the output state before a clock pulse.
2. Q_{n+1} refers to the output state after a clock pulse.

5

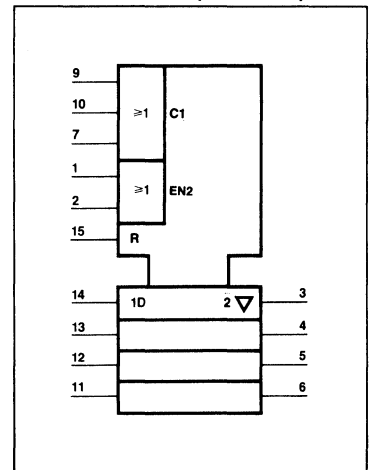
PIN CONFIGURATION



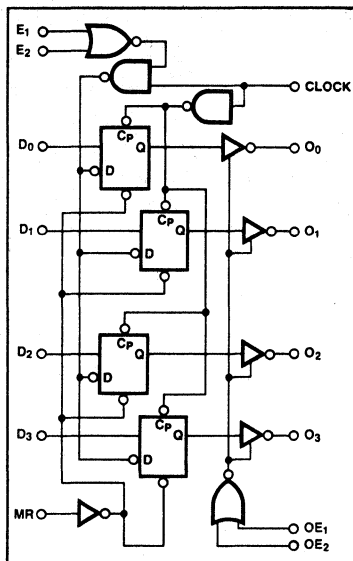
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			0.8	V
I _{IK}	Input clamp current			- 12	mA
I _{OH}	HIGH-level output current			- 5.2	mA
I _{OL}	LOW-level output current			32	mA
T _A	Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹	8T10		UNIT	
		Min	Max		
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		V	
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		V	
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12 mA		V	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = - 5.2 mA		V	
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 32 mA		V	
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5 V	Dn	40	μA
			Cp	40	μA
			Others	50	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V	Dn	- 3.2	mA
			Cp	- 3.2	mA
			Others	- 2.0	mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX		mA	
I _{CC}	Supply current (total)	V _{CC} = 5.25V		mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8T		UNIT	
		Min	Max		
t _{MAX}	Maximum clock frequency	Figure 1		MHz	
t _{PLH}	Propagation delay	Figure 1	CL = 30 pF	25	ns
t _{PHL}	Clock to output		CL = 300 pF	35	
t _{PHL}	Propagation delay, MR to output	Figure 2	CL = 30 pF	22	ns
			CL = 300 pF	30	
t _{PZH}	Output enable to HIGH level			ns	
t _{PZL}	Output enable to LOW level	Figure 4	CL = 300 pF	30	ns
t _{PHZ}	Output disable from HIGH level			ns	
t _{PLZ}	Output disable from LOW level	Figure 4	CL = 300 pF	30	ns

NOTE

For industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	8T10		UNIT
		Min	Max	
t _w (CP)	Clock pulse width	Figure 1		ns
t _w (MR)	MR pulse width	Figure 2		ns
t _s	Setup time, Data to Clock	Figure 1		ns
t _h	Hold time, Data to Clock	Figure 3		ns

AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY t_{PHL} t_{PLH} (CLOCK TO OUTPUT)

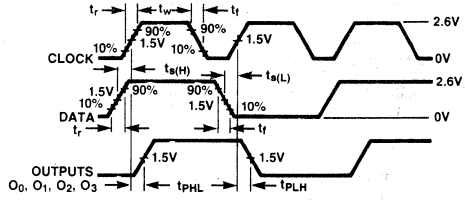
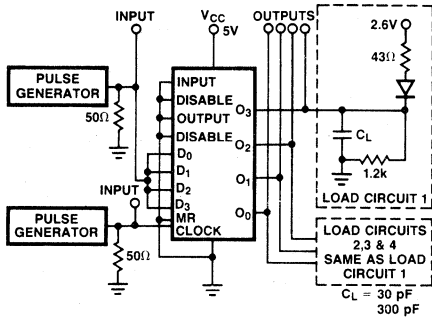


Figure 1

PROPAGATION DELAY t_{PHL} (MASTER RESET TO OUTPUT)

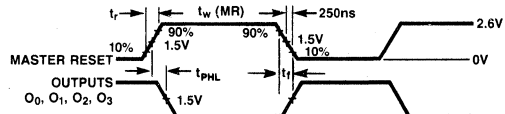
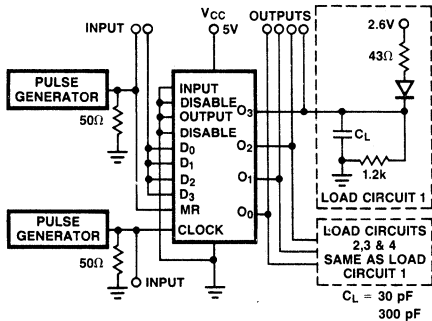


Figure 2

PROPAGATION DELAY (DATA HOLD TIME)

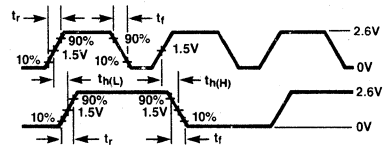
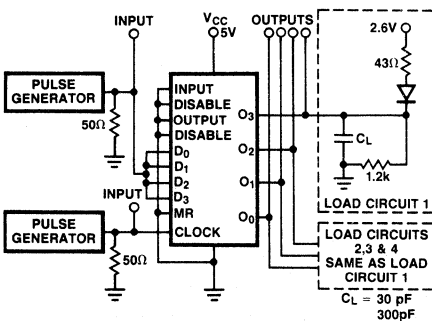
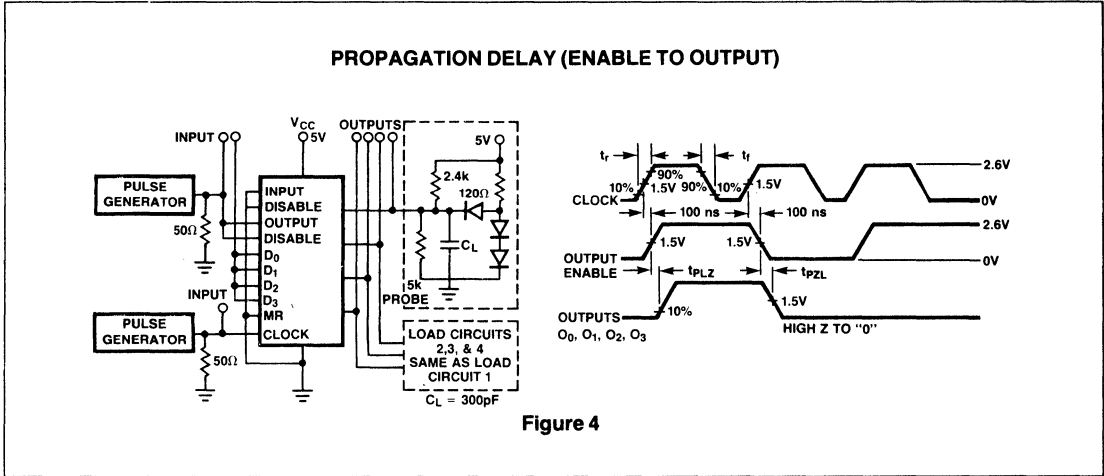
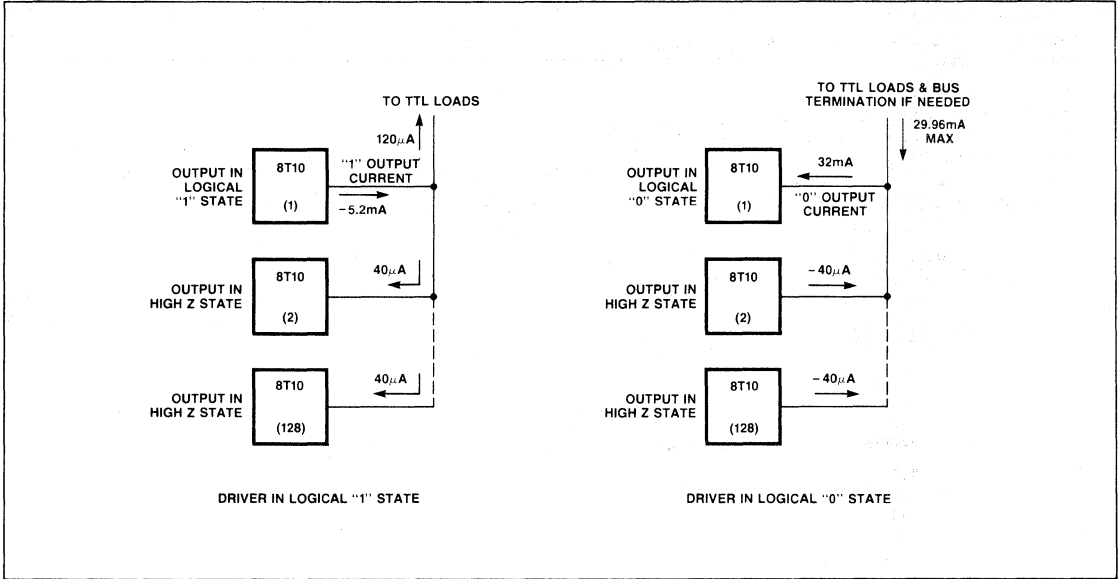


Figure 3

AC TEST FIGURES AND WAVEFORMS (Cont'd)



TYPICAL APPLICATIONS



Dual Line Driver

KEY DESIGN BENEFITS

- High-Power Drive Capability: Specified at - 75 mA source current rating at 2.4 volts.
- Party-Line Operation: Emitter-follower outputs enable two or more drivers to drive the same line. This permits multiple time-shared terminal connections since these drivers have no effect upon the transmission line unless activated.
- Input gating structure allows employment of the "OR" as well as the "AND" function.
- High Speed: Propagation Delay = 20 ns (max).
- Input Clamp Diodes: Protects inputs from line ringing.
- Single 5 Volt power supply.
- Short Circuit Protection: Incorporates a latch-back short circuit protection feature which protects the device by limiting the current it may source when operating under conditions of zero load resistance.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8T13	32 ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{cc} = 5V ± 5%; T _A = 0°C to + 70°C
Plastic DIP	N8T13N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

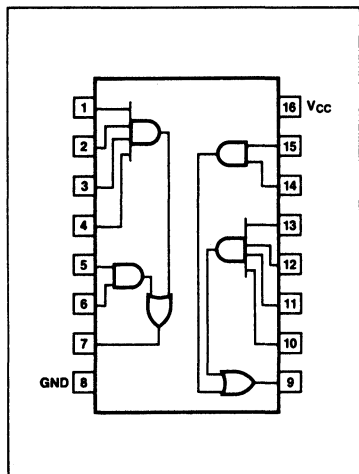
PINS	DESCRIPTION	8T
All Inputs	Input	1 ul
7,9	Output	46 ul

NOTE
A unit load (ul) is 40 μA I_{IH} and -1.6 mA I_{IL}.

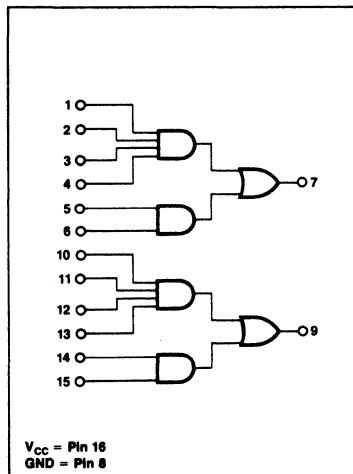
DESCRIPTION

The 8T13 is a monolithic Dual Line Driver designed to drive 50 ohm or 75 ohm coaxial transmission lines. TTL multiple emitter inputs allow this line driver to interface with stand- and TTL or DTL systems. The outputs are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with impedances of 50Ω to 500Ω.

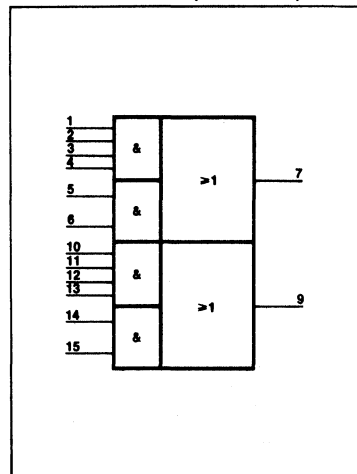
PIN CONFIGURATION



LOGIC SYMBOL



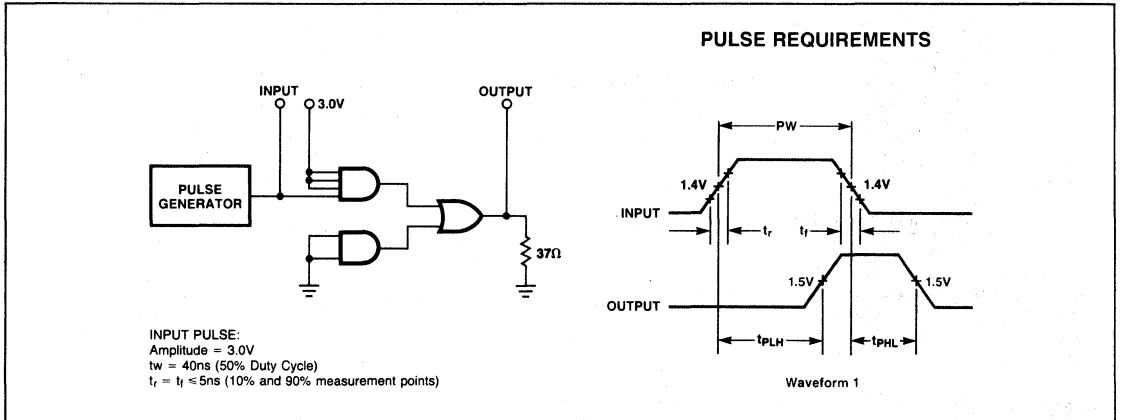
LOGIC SYMBOL (IEEE/IEC)



AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8T13		UNIT
		$R_L = 37\Omega$		
		Min	Max	
t_{PLH} t_{PHL} Propagation delay	Waveform 1		20 20	ns

TEST FIGURE AND AC WAVEFORMS



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			0.8	V
I _{IK}	Input clamp current			- 12	mA
I _{OH}	HIGH-level output current			75	mA
T _A	Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹	8T13		UNIT	
		Min	Max		
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12 mA		- 1.5	V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = 75 mA	2.4		V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		40	μA
		V _{CC} = 0V, V _I = 4.5V			
I _{IL}	LOW-level input current	V _{CC} = MAX, V _{IN} = 0.4V		- 1.6	mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX		- 30	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V		60	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC}MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

DESCRIPTION

The 8T15 Dual Communications Line Driver provides line driving capability for data transmission between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, Mil std-188B and CCITT V24.

This dual 4-input NAND driver will accept standard TTL logic level inputs and will drive interface lines with nominal data levels of $\pm 6V$ and $-6V$. Output slew rate may be adjusted by attaching an external capacitor from the output terminal to ground. The outputs are protected against damage caused by accidental shorting to as high as $\pm 25V$.

Dual Communications EIA/MIL Line Driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8T15	4 ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^{\circ}C$ to $+70^{\circ}C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^{\circ}C$ to $+125^{\circ}C$
Plastic DIP	N8T15	

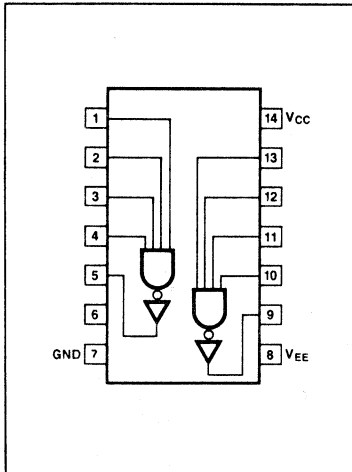
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
All	Inputs	1 ul
All	Outputs	10 ul

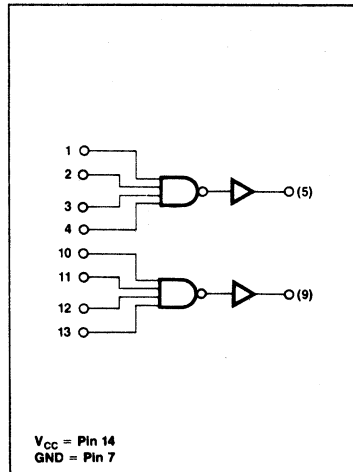
NOTE:

Where unit load (ul) is $40 \mu A I_{IH}$ and $-1.6 mA I_{IL}$.

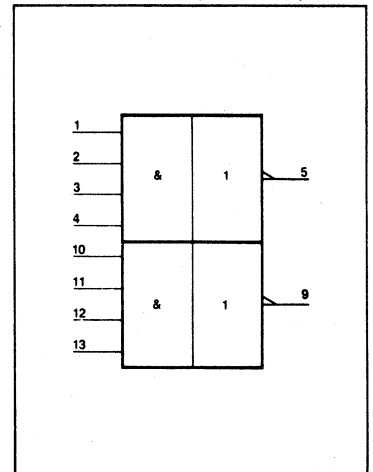
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage, positive	+ 15	V
V _{EE}	Supply voltage, negative	- 15	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage, positive	11	12	13	V
V _{EE}	Supply voltage, negative	- 11	- 12	- 13	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			0.8	V
I _{IK}	Input clamp current			12	mA
I _{OH}	HIGH-level output current			- 4	mA
I _{OL}	LOW-level output current			4	mA
T _A	Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER		TEST CONDITIONS ¹	8T15		UNIT
			Min	Max	
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage			V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12 mA		1.5	V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = - 4 mA	- 5.0	- 7.0	V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 4 mA	- 5.0	- 7.0	V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		40	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V		- 1.6	mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX	- 25	+ 25	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V		16	mA
I _{EE}	Supply current (total)	V _{CC} = 5.25V		- 28	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC}MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

LINE DRIVER

8T15

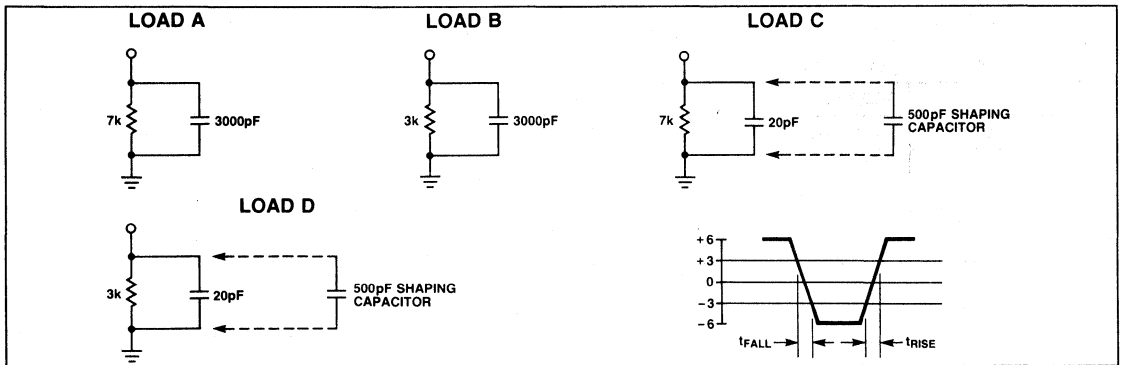
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 12.0\text{V}$, $V_{EE} = -12.0\text{V}$

PARAMETER	TO	8T15			UNIT
		Min	Typ	Max	
Output rise time ¹	Load A	200		4	ns
	Load C			ns	
Output fall time ¹	Load B	200		4	ns
	Load D			ns	
Current ²					
Positive supply				16	mA
Negative supply				28	mA

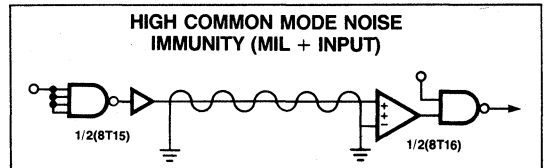
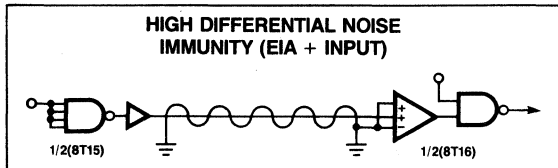
NOTES:

- Rise and fall times are measured between the +3V and -3V points on the output waveform.
- $V_{CC} = 12.6\text{V}$, $V_{EE} = -12.6\text{V}$.

AC TEST FIGURES & WAVEFORMS



TYPICAL APPLICATION



LINE DRIVER

8T15

Table 1 provides a summary of the specific requirements of EIA Standard RS-232B and C, MIL STD-188B and CCITT V24 for Communications Line Drivers along with the electrical characteristics of the Signetics 8T15.

TABLE 1					
SPECIFICATION	EIA RS-232B, C	MIL-STD-188B	CCITT V24	SIGNETICS 8T15	
				(LIMIT)	(TYPICAL)
Output Voltage "1"	-5V min. (R _L = 3000Ω) -15V max. (R _L = 7000Ω)	-6 ± 1V	-5V min. (R _L = 3000Ω) -15V max. (R _L = 7000Ω)	-5V min. -7V max. at 4 mA	-6V at 4 mA
Output Voltage "0"	+5V min. (R _L = 3000Ω) +15V max. (R _L = 7000Ω)	+6 ± 1V	+5V min. (R _L = 3000Ω) +15V max. (R _L = 7000Ω)	+5V min. 7V max. at -4 mA	+6V at -4 mA
Source Impedance (power on)	Not Specified	100Ω max for 1 < 10 mA	Not Specified		95Ω for ± (0.5 to 4.0 mA)
Source Impedance (power off)	300 min. at ±2V	N/A	300 min. at ±2V	300 min. at ±2V	2.5 MΩ
Max. Short Circuit Current	±500 mA max. (to ±25V)	100 mA max. (to ground)	±500 mA max. (to ±25V)	±25 mA max. (to ±25V)	±5 mA (to ±25V)
Wave Shape (rise and fall time)	±4% of pulse Interval (max.)	±5% of pulse Interval (min.)		4 μs-3000 pF 200 ns-20 pF	2 μs-3000 pF 25 ns-20 pF
Bit Rate	0-20 KHz	4 KHz normal	20 KHz max.		3 MHz
Open Circuit Drive	±25V max.	±6V ±1V		±6V ±1V	±6V
Signal Characteristics	1 ms max. transition		1 ms max. transition		2 μs with C _L = 3000 pF
	30V/μs max. dV/dt		30V/μs max. dV/dt		20V/μs with C _L = 500 pF

LINE RECEIVER

8T16

Dual Communications EIA/MIL Line Receiver with Hysteresis

DESCRIPTION

The 8T16 Dual Communications Line Receiver provides receiving capability for data lines between Data Communication and Terminal Equipment. The device meets or exceeds the requirements of EIA Standard RS-232B and C, MIL-STD-188B and CCITT V24 and operates from a single 5 volt power supply.

The receivers accept single (EIA) or double ended (MIL) inputs and are provided with an output strobing control. Both EIA and MIL input standards are accommodated.

When using the EIA input terminal (with the Hysteresis terminal open), input voltage threshold levels are typically +2V and -2V with a guaranteed minimum Hysteresis of 2.4V. By grounding the "Hysteresis" terminal, the EIA input voltage threshold levels may be shifted to typically +1.0V and +2.1V with a minimum guaranteed Hysteresis of 0.75V. (Note that when using the EIA inputs, the MIL inputs — both positive and negative — must be grounded.)

The MIL input voltage threshold levels are typically +0.6V and -0.6V with a minimum guaranteed Hysteresis of 0.7V. A MIL negative terminal is provided on each receiver per specification MIL-STD-188B to provide for common mode noise rejection.

- Each receiver includes a strobe input so that:
- A "1" on the strobe input allows data transfer.
 - A "0" on the strobe input holds the output high.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T16	100 ns	

ORDERING CODE

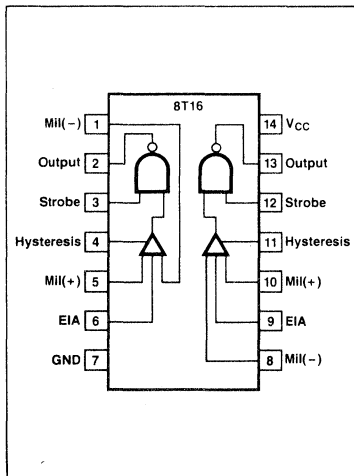
PACKAGES	COMMERCIAL RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^{\circ}C$ to $+70^{\circ}C$
Plastic DIP	N8T16

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

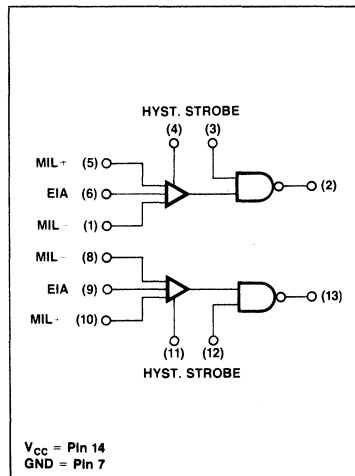
PINS	DESCRIPTION	8T
MIL(+), MIL(-), EIA	Input	1 ul
HYST, STROBE	Input	1 ul
2, 13	Output	10 ul

NOTE:
A unit load (ul) is 40 μA I_{IH} and -1.6 mA I_{IL} .

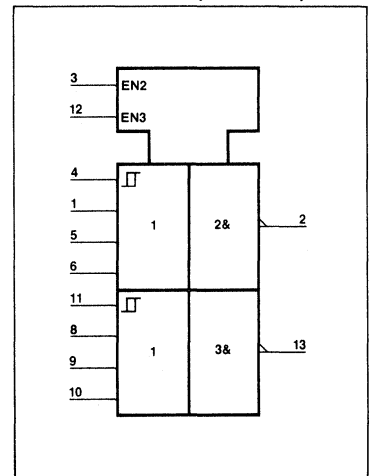
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LINE RECEIVER**8T16****ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0		2.5	V
V _{IL}	LOW-level input voltage	1.1		1.5	V
I _{IK}	Input clamp current			- 12	mA
I _{OH}	HIGH-level output current			- 800	μA
I _{OL}	LOW-level output current			9.6	mA
T _A	Operating free-air temperature	0		70	°C

LINE RECEIVER

8T16

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

PARAMETER	TO	FROM	TEST CONDITIONS	8T16			UNIT
				Min	Typ	Max	
V_{OH} Output voltage (EIA) Hysteresis open ^{8,12}	Outputs -800 μ A	EIA, MIL(+), MIL(-), STROBE	EIA = 3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V	2.6	3.5		V
Hysteresis open	Outputs -800 μ A	EIA, MIL(+) MIL(-), STROBE	EIA = +1.2V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V	2.8	3.5		V
Hysteresis grounded ^{8,10}	Outputs -800 μ A	EIA, MIL(+), MIL(-), HYS, STROBE	EIA = +0.3V, MIL(+) = 0V, MIL(-) = 0V, HYS = 0V, STROBE = 2.0V	2.6	3.5		V
V_{OH} Output voltage (MIL) ^{8,11}	Outputs -800 μ A	MIL(+), MIL(-), STROBE	MIL(+) = -0.1 mA, MIL(-) = 0V, STROBE = 2.0V	2.6	3.5		V
Output voltage (MIL) ^{8,11}	Outputs -800 μ A	MIL(+), MIL(-) STROBE	MIL(+) = -0.9V, MIL(-) = 0V STROBE = 2.0V	2.6	3.5		V
Output voltage (MIL) ^{8,13}	Outputs -800 μ A	MIL(+), MIL(-), STROBE	MIL(+) = +0.35V, MIL(-) = 0V, STROBE = 2.0V	2.8	3.5		V
V_{OH} Output voltage (STROBE) ⁸	Outputs -800 μ A	EIA, MIL(+), MIL(-), STROBE	EIA = 3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V	2.6	3.5		V
V_{OL} Output voltage (EIA)							
Hysteresis open ^{9,12}	Outputs 9.6 mA	EIA, MIL(+), MIL(-), STROBE	EIA = +3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V			0.4	V
Hysteresis open ^{9,10}	Outputs 9.6 mA	EIA, MIL(+), MIL(-), STROBE	EIA = -1.2V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 2.0V		0.2	0.4	V
Hysteresis grounded ^{9,12}	Outputs 9.6 mA	EIA, MIL(+), MIL(-), HYS, STROBE	EIA = +3.0V, MIL(+) = 0V, MIL(-) = 0V, HYS = 0V, STROBE = 2.0V			0.4	V
Output voltage (MIL) ^{9,13}	Outputs 9.6 mA	MIL(+), MIL(-), STROBE	MIL(+) = +0.1 mA, MIL(-) = 0V, STROBE = 2.0V			0.4	V
Output voltage (MIL)	Outputs 9.6 mA	MIL(+), MIL(-), STROBE	MIL(+) = +0.9V, MIL(-) = 0V, STROBE = 2.0V			0.4	V
Output voltage (MIL) ^{9,11}	Outputs 9.6 mA	MIL(+), MIL(-), STROBE	MIL(+) = -0.35V, MIL(-) = 0V, STROBE = 2.0V		0.2	0.4	V
Input resistance (EIA)		EIA, MIL(+), MIL(-)	EIA = \pm 25V, MIL(+) = 0V, MIL(-) = 0V	3	5	7	k Ω
Input resistance (MIL)		EIA, MIL(+), MIL(-)	EIA = 0V, MIL(+) = \pm 25V, MIL(-) = 0V	7.5	11.4		k Ω
Power consumption (per receiver) ¹⁷		EIA, MIL(+), MIL(-)	EIA = 3.0V, MIL(+) = 0V, MIL(-) = 0V		44	75	mW
I_{OS} Output short circuit current ^{16,17}	Outputs 0V	EIA, MIL(+), MIL(-)	EIA = -3.0V, MIL(+) = 0V, MIL(-) = 0V, STROBE = 5.0V	-10		-70	mA
Propagation delay ^{14,15}		STROBE	STROBE = 5.0V		100	150	ns
Signal switching acceptance ¹⁵		STROBE	STROBE = 5.0V	20			kHz

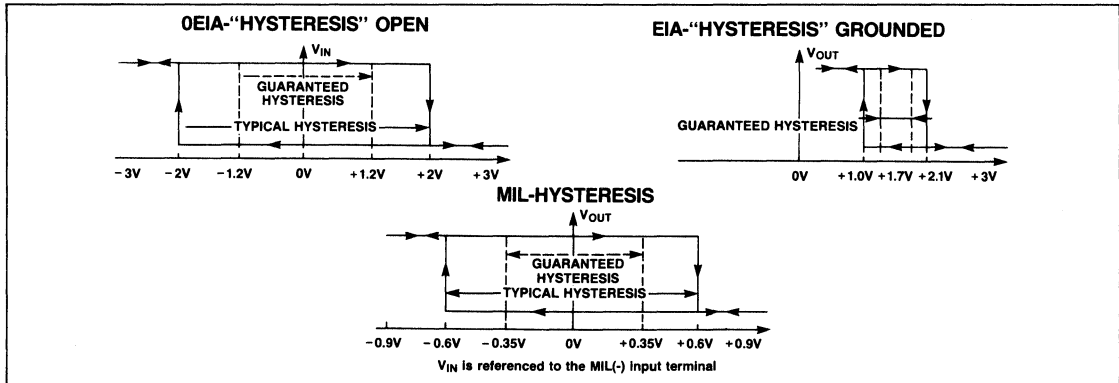
- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- All measurements are taken with ground pin tied to zero volts.
- Positive current is defined as into the terminal referenced.
- Positive logic definition: "UP" Level = H, "DOWN" Level = L.
- Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings.
- Manufacturer reserves the right to make design and process changes and improvements.
- This test guarantees operation free of latch-up over the specified input voltage range.
- Output source current is supplied through a resistor to ground.
- Output sink current is supplied through a resistor to V_{CC} .
- Previous EIA Input: +3V (See hysteresis curve).
- Previous MIL input: +0.9V (See hysteresis curve).
- Previous EIA input: -3.0V (See hysteresis curve).
- Previous MIL input: -0.9V (See hysteresis curve).
- Reference AC Test Figures.
- This test guarantees transfer of signals of up to 20 kHz. Connect 1000 pF between the output terminal and ground.
- Each receiver to be tested separately.
- $V_{CC} = 5.25V$.

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	FROM	TEST CONDITIONS	8T16			UNIT
			Min	Typ	Max	
Input resistance	EIA, MIL(+), MIL(-)	EIA = $\pm 25\text{V}$, MIL(+) = 0.0V, MIL(-) = 0.0V	3	5	7	k Ω
	MIL	EIA = 0.0V, MIL(+) = $\pm 25\text{V}$, MIL(-) = 0.0V	7.5	11.4		k Ω
Propagation delay	Strobe	Strobe = 5.00V		100	150	ns
Signal switching acceptance	Strobe	Strobe = 5.00V	20			kHz

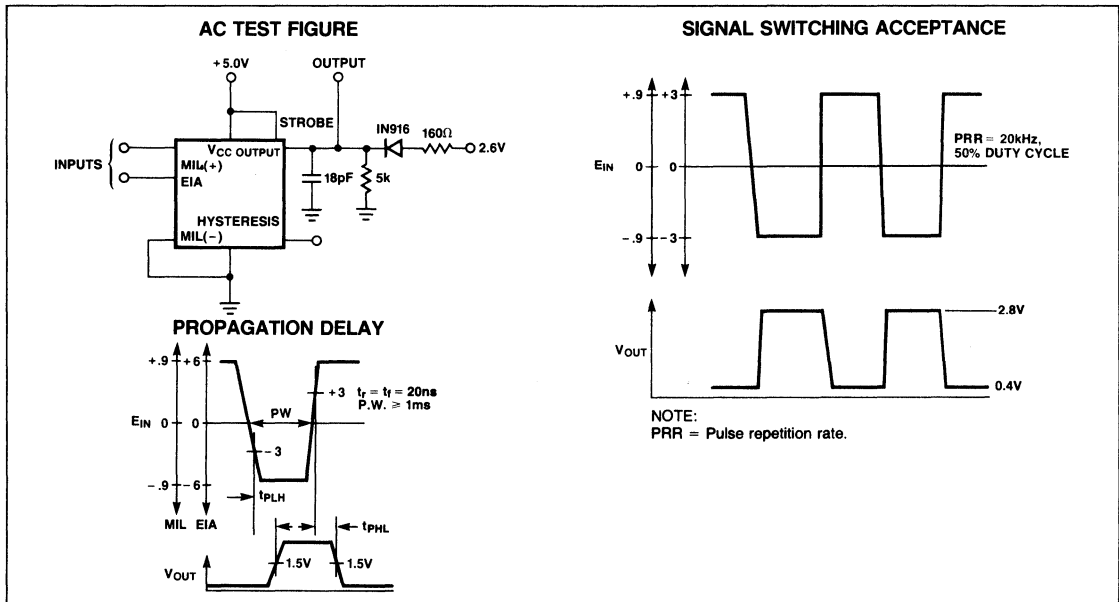
NOTE:
This test guarantees transfer of signals of up to 20 kHz. Correct 1000 pF between the output terminal and ground.

HYSTERESIS CURVES

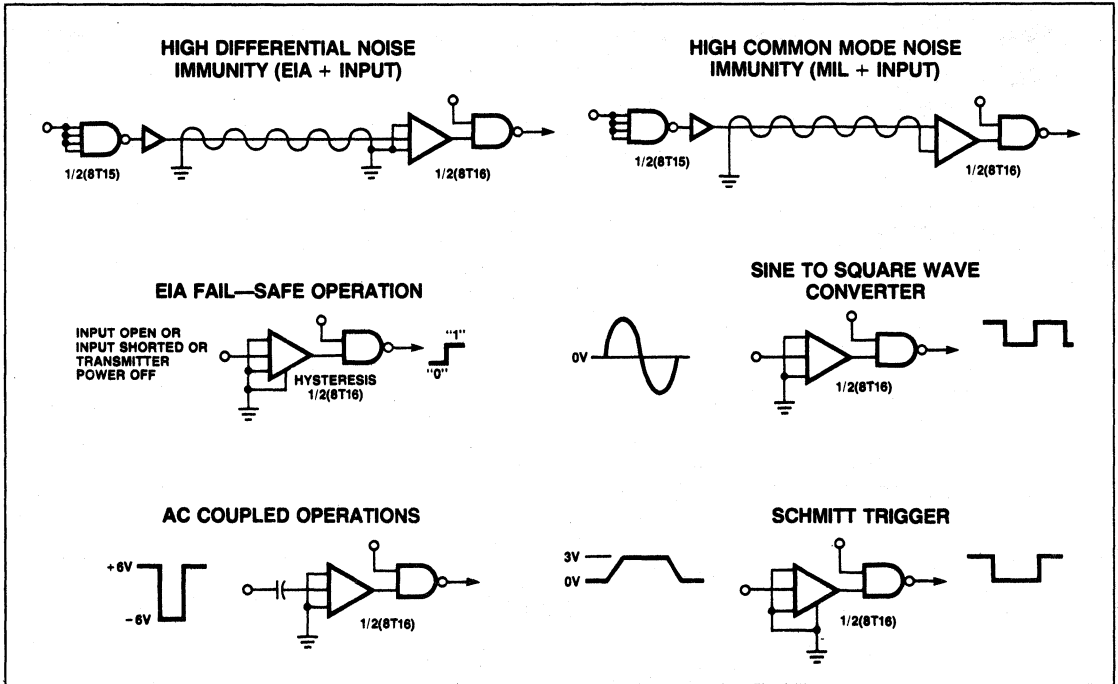


5

AC TEST FIGURES AND WAVEFORMS



TYPICAL APPLICATIONS



MULTIVIBRATOR

8T20

Bidirectional One-Shot

FEATURES

- **Differential Input Threshold = ±4 mV**
- **Pulse Position Error = Typically < 3 ns**
- **Max. Input Frequency = 8 MHz**
- **Triggers on Positive and/or Transitions**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T20	30 ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T20N

APPLICATIONS

- **Disc, Tape and Drum Readers**
- **Digital Communications Receivers**
- **Signal Conditioners**
- **Transition Detectors**

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
PEC, NEC	Input	1 ul
MR	Input	1 ul
A, A; Q, Q	Output	10 ul

NOTE:

A unit load (ul) is 40 μA I_{IH} and - 1.6 mA I_{IL} .

DESCRIPTION

The Bidirectional One Shot is intended for applications where high speed low level signal processing is required.

The 8T20 is a Monolithic Building Block, consisting of a high speed analog comparator, digital control circuitry, and a precision monostable multivibrator. The differential input threshold voltage is between ± 4 mV with respect to the input reference level which may range from -3.2V to +4.2V. For input frequen-

cies up to 8 MHz, the device may be conditioned to act as a frequency doubler since it can trigger on both positive and negative input transitions.

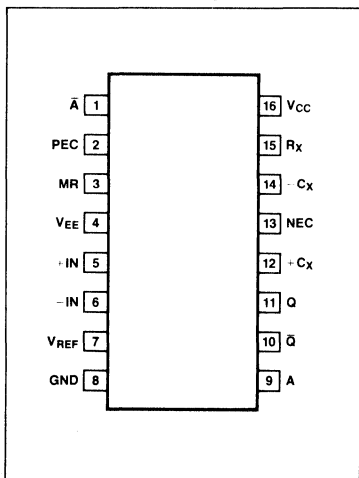
Timing pins permit using this device in a variety of applications where external control over pulse width is desirable. Pulse width (t_W) is defined by the relationship $t_W = C_X R_X \text{Loge } 2$. Pulse width stability is internally compensated and virtually independent of temperature and

V_{CC} variations, thus only limited by the accuracy of external timing components.

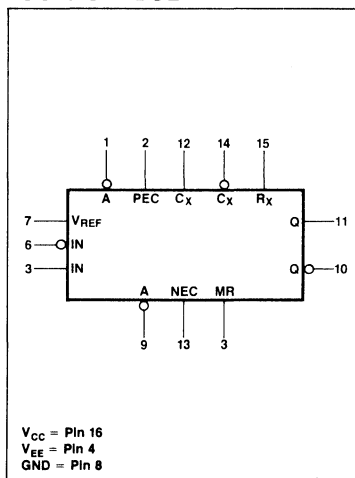
An internal resistive divider is available on the chip to provide a voltage of 1.4V (typ.). This output can be connected directly to either of the comparator inputs as a reference voltage when interfacing with TTL outputs.

5

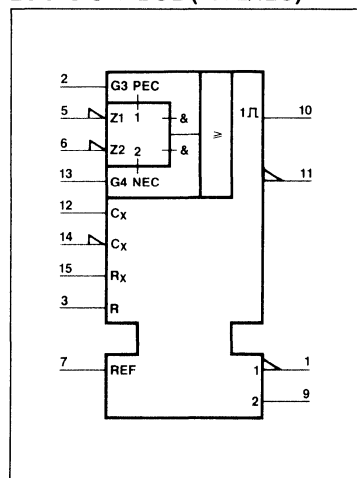
PIN CONFIGURATION



LOGIC SYMBOL



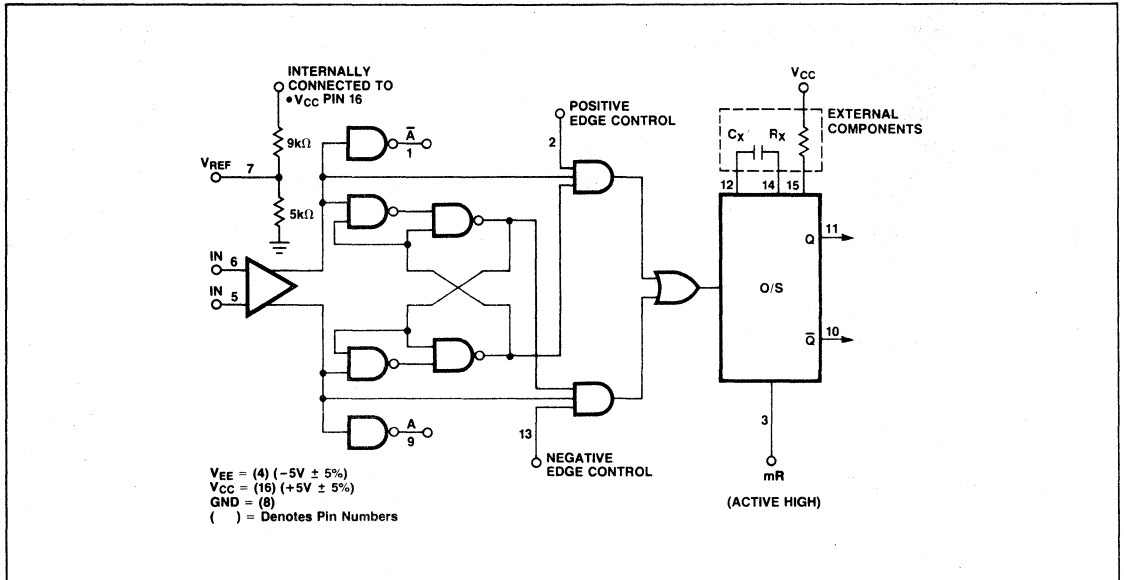
LOGIC SYMBOL (IEEE/IEC)



MULTIVIBRATOR

8T20

LOGIC DIAGRAM



MULTIVIBRATOR

8T20

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage, positive	7.0	V
V _{EE}	Supply voltage, negative	- 7.0	V
V _{DIF}	Differential input voltage	± 5.5	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT
		Min	Nom	Max	
V _{CC}	Supply voltage, positive	4.75	5.0	5.25	V
V _{EE}	Supply voltage, negative	- 4.75	5.0	- 5.25	V
V _{IH}	HIGH-level input voltage	2.0			V
V _{IL}	LOW-level input voltage			0.8	V
I _{IK}	Input clamp current			- 12	mA
I _{OH}	HIGH-level output current			- 800	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹	8T20		UNIT
		Min	Max	
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0	V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage	0.8	V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12 mA	- 1.5	V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = - 800 μA	2.4	V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 16 mA	0.4	V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5 V	40	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V PEC, NEC	- 2.4	mA
I _{IL}	Low level input current	V _{CC} = MAX, V _I = 0.4V mR	- 1.6	mA
I _{OS}	Short-circuit output current ³	V _{CC} = MAX	- 20	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V	55	mA
I _{EE}	Supply current (total)	V _{CC} = 5.25V	- 20	mA

DIFFERENTIAL INPUTS

PARAMETER				UNIT
V _T	Input Threshold Voltage ⁴		±4	mV
I _B	Input Bias Current ⁵	V _{CC} = +5V, V _{EE} = - 5V	125	μA
I _{OS}	Input Offset Current		2	μA
V _{CM}	Common Mode Input Volt, Range ⁶		- 3.2	+ 4.2

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- The differential input threshold voltage (V_T) is defined as the maximum DC voltage from the reference level necessary to trigger the one-shot.
- Refer to Figure 5.
- Common mode voltages that are confined within the dynamic range as specified will not cause false triggering of the one-shot.

5

MULTIVIBRATOR**8T20****AC CHARACTERISTICS** $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$, $V_{EE} = -5.0\text{V}$

CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS
	Min.	Typ.	Max.		
Output Frequency	16			MHz	Fig. 1, $f_{in} = 8\text{ MHz}$
Propagation Delay					
Input to Q, \bar{Q}		30	50	ns	Fig. 2
Input to A, \bar{A}		30	50	ns	Fig. 4
MR to Q, \bar{Q}		20	30	ns	
Reference Voltage (V_{REF})	0.8	1.4	2.0	V	Pin 7 tied to Pin 6
Output Pulse Width, Fig. 1	10		40	ns	$R_x = 10\text{K}$, $C_x = \text{Open}$
Output Pulse Width, Fig. 3	600		800	ns	$R_x = 10\text{K}$, $C_x = 100\text{ pF}$

AC TEST CIRCUITS

MINIMUM OUTPUT PULSE WIDTH ($C_{X2} = \text{OPEN}$)

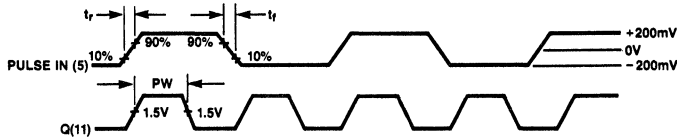
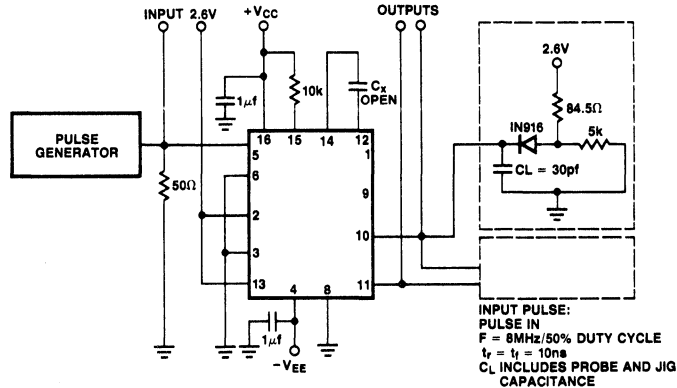


Figure 1

PROPAGATION DELAY (INPUT TO Q, \bar{Q} OUTPUTS)

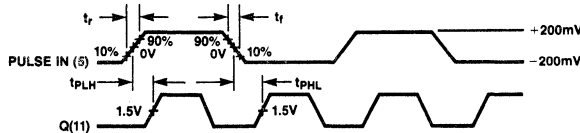
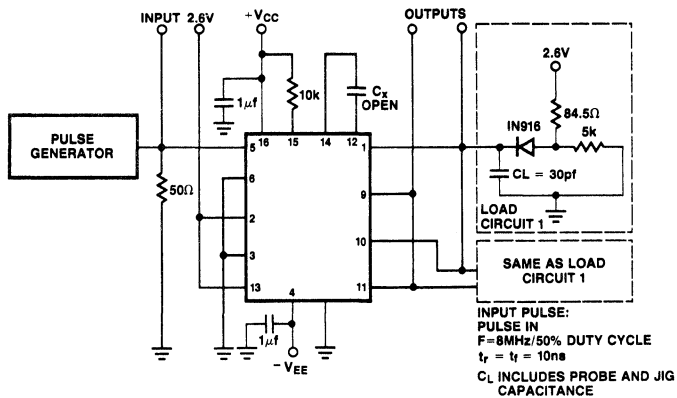
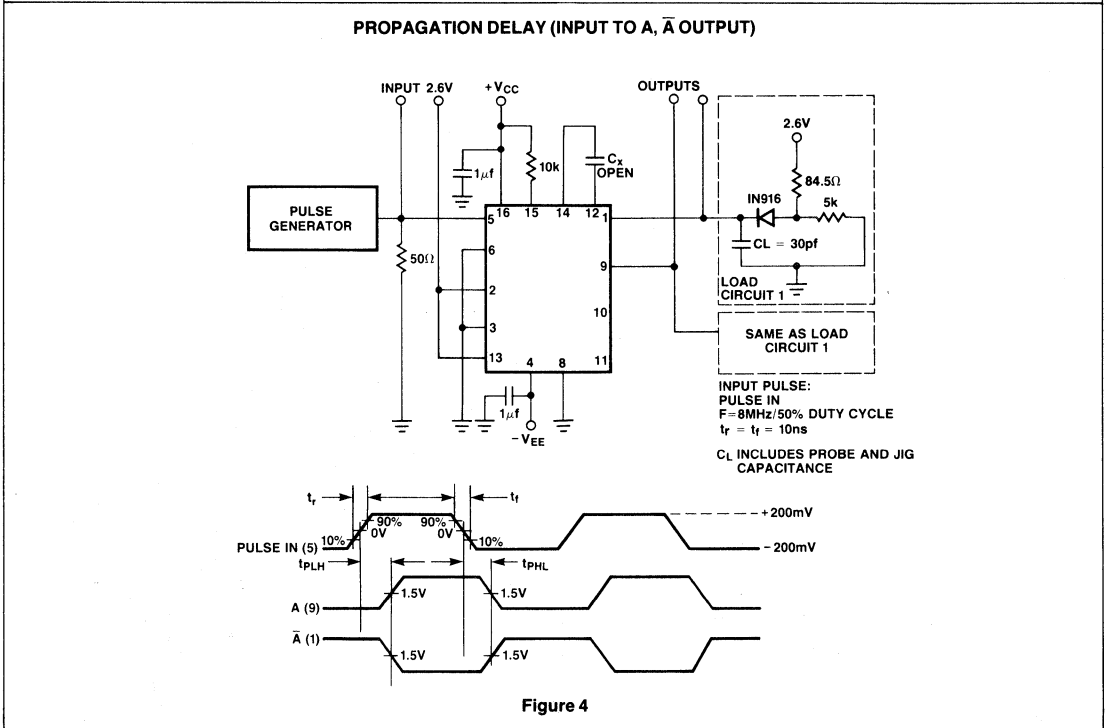
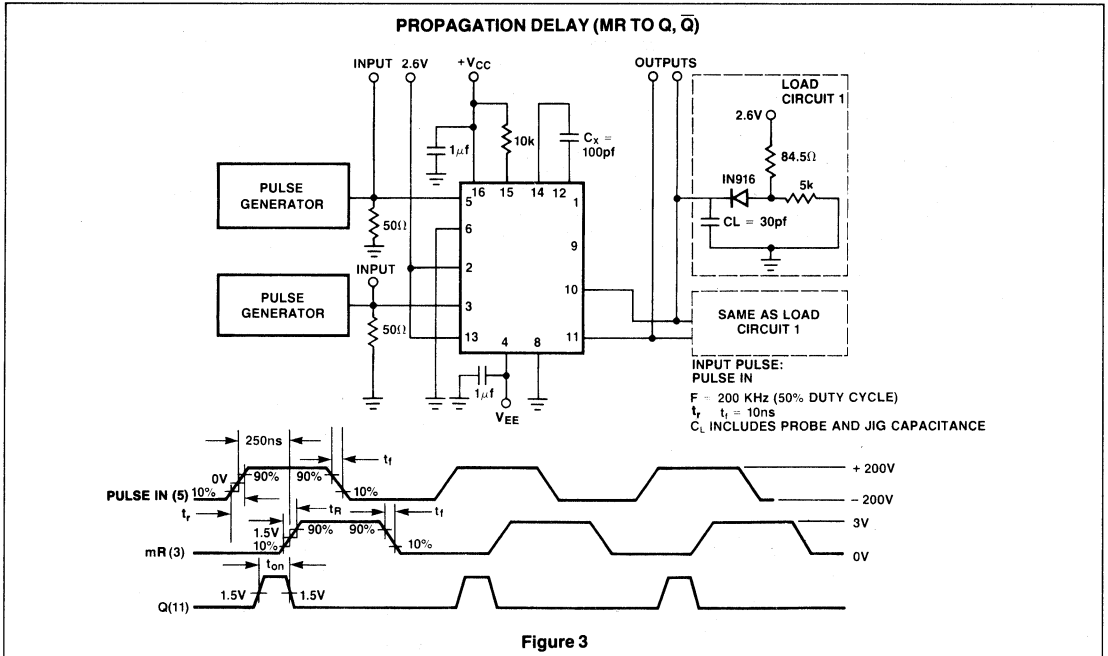


Figure 2

AC TEST CIRCUITS (Cont'd)



INPUT BIAS CURRENT TEST CIRCUIT

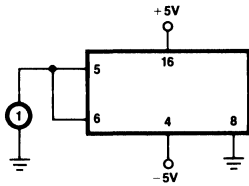


Figure 5

INPUT/OUTPUT WAVEFORMS

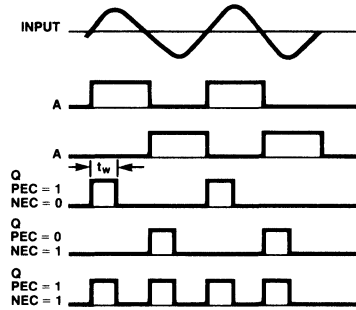


Figure 6

Retriggerable One Shot

DESCRIPTION

The 8T22 is a direct pin-for pin replacement for the 9601 retriggerable one-shot. Triggering can be performed on either the leading or falling edge of the input signal through selection of the proper input terminal.

The inputs are level-sensitive making triggering independent of signal transition times. Output pulse width is determined by external timing components (R_x and C_x) with each trigger pulse initiating a complete new timing cycle.

For those applications where a dual retriggerable one-shot is required the Signetics 9602 should be considered.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T22	20 ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{cc} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N8T22N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
An, Bn	Input	1.5 ul
Cx, Rx	Input	1.5 ul
Q, Q	Output	8 ul

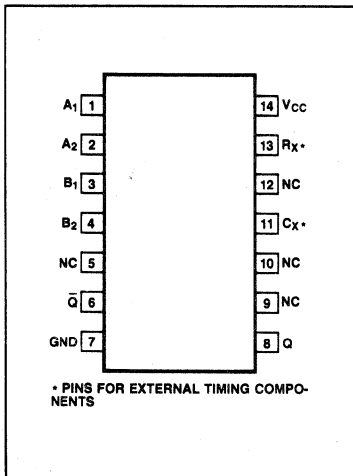
NOTE:

A unit load (ul) is $40 \mu A I_{IH}$ and $-1.6 mA I_{IL}$.

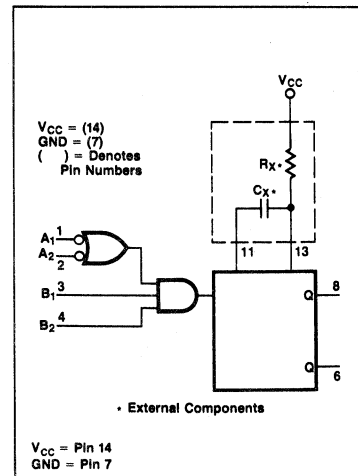
FUNCTION TABLE

PIN NUMBER			
1	2	3	4
H-L	H	H	H
H	H-L	H	H
L	X	L-H	H
X	L	L-H	H
L	X	H	L-H
X	L	H	L-H

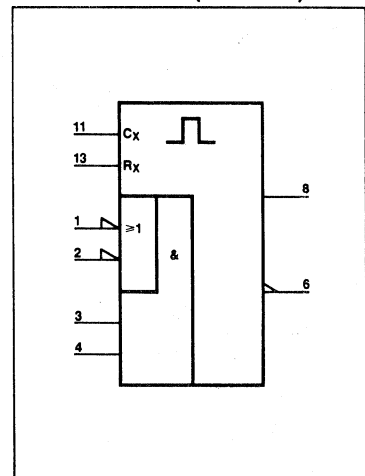
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MULTIVIBRATOR

8T22

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	1.9		2.5	V
V _{IL}	LOW-level input voltage			0.9	V
I _{IK}	Input clamp current			- 12	mA
I _{OH}	HIGH-level output current			960	μA
I _{OL}	LOW-level output current			12.8	mA
T _A	Operating free-air temperature	0		70	°C

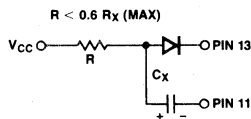
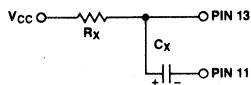
DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹	8T22		UNIT	
		Min	Max		
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	1.9		V
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		0.9	V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12 mA		- 1.5	V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = - 960 μA	2.4		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 12.8 mA		0.4	V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		60	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V		- 1.6	mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX, V _O = 0	- 10	- 40	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V		25	mA
I _{EE}	Supply current (total)	V _{CC} = 5.25V		- 28	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

OPERATION RULES



1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 to 50 k Ω (0 to 75°).
3. C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μ A or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. If electrolytic capacitors are to be used, the following configurations are recommended:

A. For use with low leakage electrolytic capacitors.

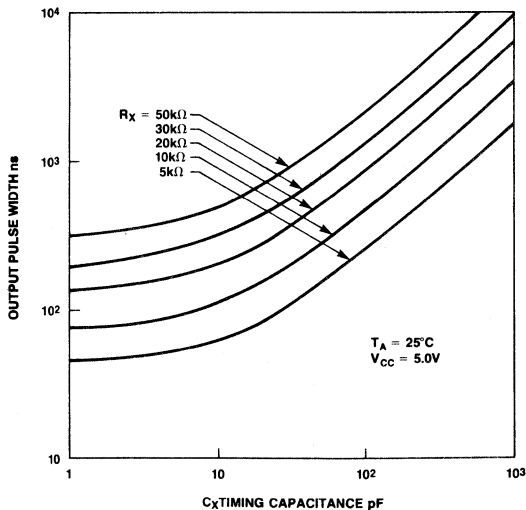
The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3 μ A, and the inverse capacitor leakage at 1.0 volt is less than 5 μ A over the operational temperature range, and Rule 3 above is satisfied.

B. Use with high inverse leakage current electrolytic capacitors. The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.

$$t \approx 0.3 RC_X$$

The output pulse with (t) is defined as follows:

$$t = 0.32 R_X C_X \left[1 + \frac{0.7}{R_X} \right] \text{ Where } R_X \text{ is in k}\Omega, C_X \text{ is in pF, } t \text{ is in ns; for } C_X < 10^3 \text{ pF.}$$



Typical output pulse width versus timing resistance and capacitance for $C_X < 10^3$ pF is shown in the above graph.

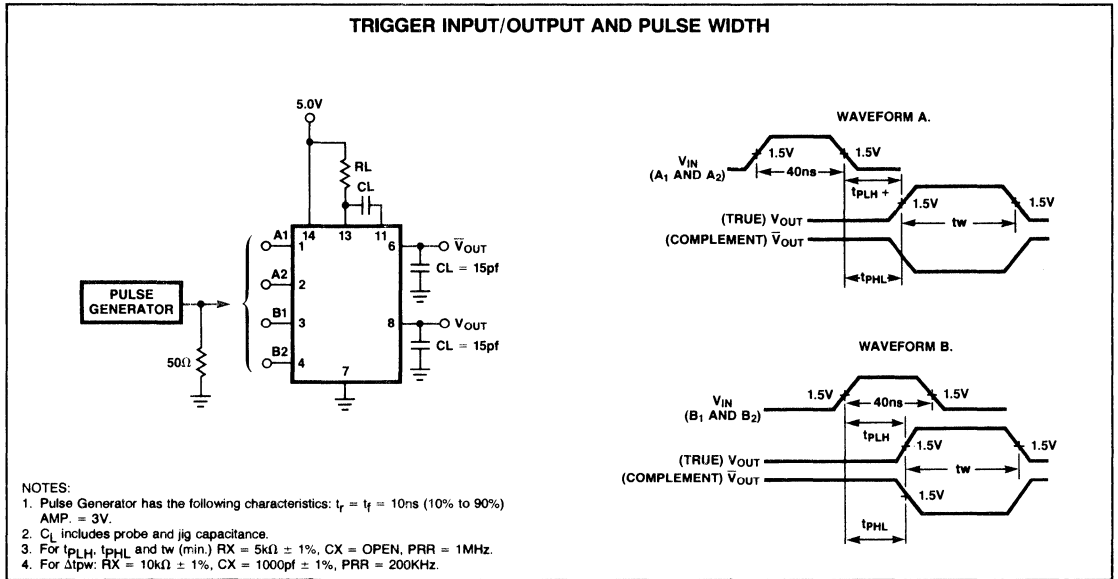
AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8T22			UNIT
		Min	Typ	Max	
Propagation Delay Negative Trigger Input to True Output (t_{PLH})	$R_x = 5.0\text{ k}\Omega$, $C_x = 0$		25	40	ns
Negative Trigger Input to False Output (t_{PHL})	$R_x = 5.0\text{ k}\Omega$, $C_x = 0$		25	40	ns
Min. True Output Pulse Width	$R_x = 5.0\text{ k}\Omega$, $C_x = 0$ $C_L = 15\text{ pF}$		45	65	ns
Pulse Width Variation	$R_x = 10\text{ k}\Omega$, $C_x = 1000\text{ pF}$	3.08	3.42	3.76	μs
Timing Resistor		5.0		50	$\text{k}\Omega$
C_{Stray} —Maximum allowable wiring capacitance	P13 to Ground			50	pF

NOTES:

1. Positive current is defined as into the pin referenced.
2. Unless otherwise note, 10 k Ω resistor placed between Pin 13 and V_{CC} (R_x).

AC TEST FIGURE AND WAVEFORMS



Triple Line Receiver with Hysteresis

FEATURES

- Built-in input threshold hysteresis*
- High speed: $t_{PHL} = t_{PLH} = 20 \text{ ns (typical)}$
- Each channel can be strobed independently
- Fanout of ten (10) with standard TTL integrated circuits
- Input gating is included with each line receiver for increased application flexibility
- Operation from a single +5V Power Supply

*Hysteresis is defined as the difference between the input thresholds for the "1" and "0" output states. Hysteresis is specified at 0.4V typically and 0.2V minimum over the operating temperature range.

DESCRIPTION

The 8T24 is a Triple Line Receiver designed specifically to meet the IBM System (360, System/370 I/O Interface Specification [IBM Specification GA 22-6974-0]). Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the driver circuit.

An input voltage of 1.7 volts or more is interpreted as a logical one; an input of 0.70 volts

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T24	20 ns (t_{PLH})	
	20 ns (t_{PHL})	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES
Plastic DIP	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ\text{C to } +70^\circ\text{C}$
	N8T24N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
R	Input	4.3 uI
S, A, B	Input	1 uI
f	Output	8 uI

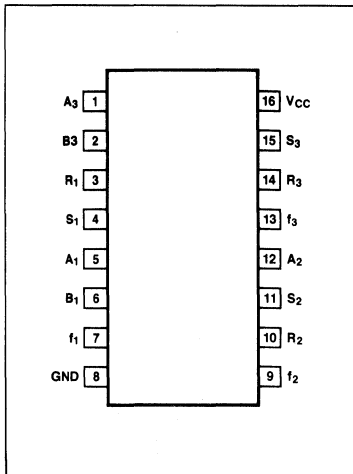
NOTE:
A unit load (uI) is 40 $\mu\text{A } I_{IH}$ and -1.6 mA I_{IL} .

or less is interpreted as a logical zero as is an open circuited input.

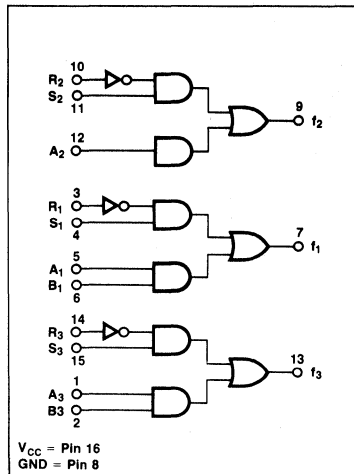
The receiver input (R) of the 8T24 will not be damaged by a DC input of +7.0 volts with power on or by a DC input of +6.0 volts with power off in the receiver. The 8T24 will also withstand an input of -0.15V with power on or off.

The 8T24 is fully compatible with TTL and DTL systems and operates from a single 5 volt power supply.

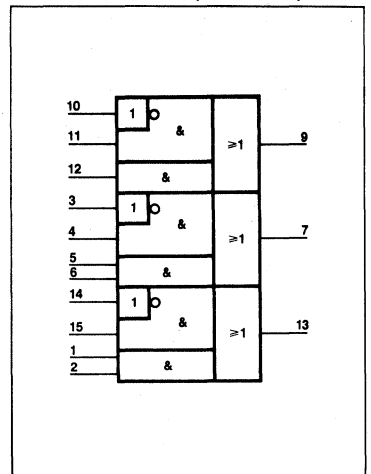
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0		2.5	V
V _{IL}	LOW-level input voltage	1.1		1.5	V
I _{IK}	Input clamp current			- 12	mA
I _{OH}	HIGH-level output current			- 800	μA
I _{OL}	LOW-level output current			16	mA
T _A	Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹	8T24		UNIT		
		Min	Max			
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		1.7	V	
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage			0.7	V
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12 mA			- 1.5	V
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = - 800 μA		2.6		V
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 16 mA			0.4	V
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 4.5V, Pins S, A, B			40	μA
		Pin R			170	μA
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.4V			- 1.6	mA
I _{OS}	Short-circuit output current ²	V _{CC} = MAX		- 50	- 100	mA
I _{CC}	Supply current (total)	V _{CC} = 5.25V			80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

1. Hysteresis is defined as the voltage difference between the R input level at which the output begins to go from "0" to "1" state and the level at which the output begins to go from "1" to "0".

SWITCHING CHARACTERISTICS $V_{CC} = 5.0V$ and $T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS				LIMITS			UNITS
	R	S	A	B	Min	Typ	Max	
t_{PHL}						20	30	ns
t_{PLH}						20	30	ns
Hysteresis ¹		4.5V	0V	0V	0.2	0.4		V

AC TEST CIRCUIT AND WAVEFORMS

Input Pulse:
Amplitude = 2.6V
Pulse width = 200ns
(50% Duty Cycle)
 $t_r = t_f = 5ns$ (10% to 90%)

3 Receivers in the package.
Test each Receiver using switch positions as shown in Table 1.

RECEIVER NO.	POSITION	
	Switch 1	Switch 2
Receiver 1	1	1
Receiver 2	2	2
Receiver 3	3	3

HYSTERESIS TEST CIRCUIT

Verify in each of three (3) position of S_1 (Figure 1) that the following occurs per Figure 2.

- V_1 and V_2 must be between 0.7V minimum and 1.7 maximum.
- Hysteresis = $V_1 - V_2$

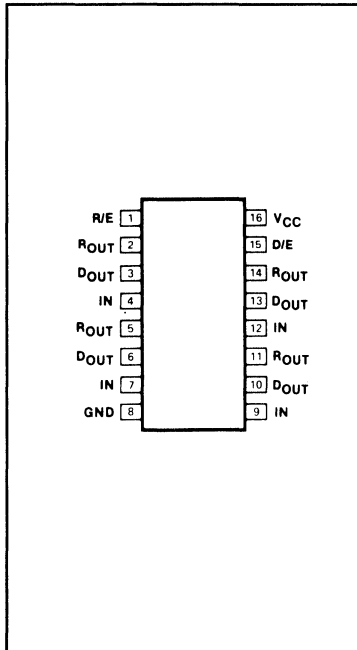
3-State Quad Bus Transceiver

- High speed Schottky quad transceivers
- 48mA LOW-state drive
- 200 μ A bus loading
- Ideal for:
 - Half-duplex data transmission
 - Memory interface buffers
 - Data routing in bus oriented systems
 - High current drivers
 - MOS/CMOS-to-TTL interface

DESCRIPTION

The 8T26A/28 consists of four pairs of 3-state logic elements configured as quad bus drivers/receivers, along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the 8T26A/28 from conventional multi-IC implementations. In addition, the 8T26/28's ultra high speed while driving heavy bus capacitance (300pF) makes these devices particularly

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T26A	7ns	48mA
N8T28	10ns	67mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N8T26AN • N8T28N	
Ceramic DIP		S8T26AF • S8T28F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	N8T	S8T
I_N	Input	0.5Sul	0.5Sul
D/E, R/E	Inputs	0.5Sul	0.5Sul
D_{OUT}	Output	24Sul	16Sul
R_{OUT}	Output	10Sul	6Sul

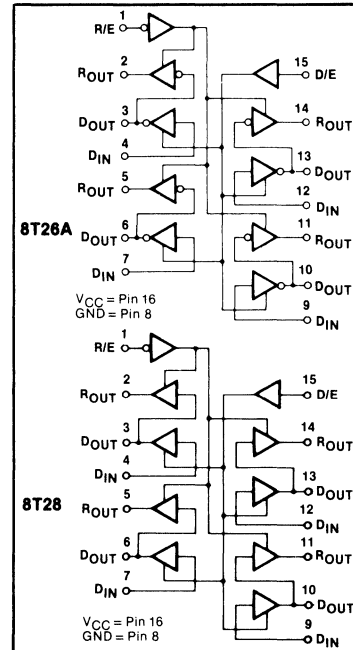
NOTE
A unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} .

suitable for memory systems and bidirectional data buses.

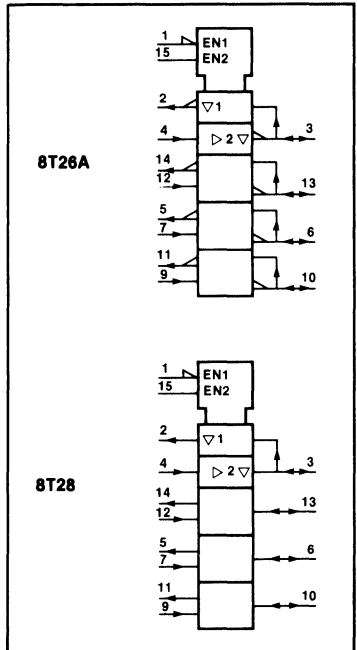
Both the driver and receiver gates have 3-State outputs and low-current PNP in-

puts. 3-State outputs provide the high switching speeds of totem-pole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200 μ A maximum.

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUS TRANSCEIVERS**8T26A, 28****ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	N8T	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I_{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
I_{OL}	Continuous	100	100	mA
V_{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			8T			UNIT	
			Min	Nom	Max		
V_{CC}	Supply Voltage	Mil	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	V	
V_{IH}	HIGH-level input voltage		2.0			V	
V_{IL}	LOW-level input voltage	Mil			+ 0.8	V	
		Com'l			+ 0.8	V	
I_{IK}	Input clamp current				- 18	mA	
I_{OH}	HIGH-level output current	Driver	Mil			- 2	mA
			Com'l			- 10	mA
I_{OL}	LOW-level output current	Driver	Mil			32	mA
			Com'l			48	mA
		Receiver	Mil			12	mA
			Com'l			20	mA
T_A	Operating free-air temperature	Mil	- 55		+ 125	°C	
		Com'l	0		70	°C	

BUS TRANSCEIVERS

8T26A, 28

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	N8T26A, N8T28		S8T26A, S8T28		UNIT	
		Min	Max	Min	Max		
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		2.0		V	
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage		0.8		0.8	V	
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 18mA		-1.2		-1.2	V	
V _{BD} Input breakdown voltage	V _{CC} = MAX, I _I = 1mA	5.5		5.5		V	
V _{OH} HIGH-level output voltage, Driver outputs	V _{CC} = MIN	I _{OH} = - 10mA	2.4			V	
		I _{OH} = - 2mA			2.4	V	
V _{OH} HIGH-level output voltage, Receiver outputs	V _{CC} = MIN, I _{OH} = - 100μA	3.25				V	
	V _{CC} = 5.0V, I _{OH} = - 100μA			3.0		V	
V _{OL} LOW-level output voltage, Driver outputs	V _{CC} = MIN	I _{OL} = 48mA		0.5		V	
		I _{OL} = 32mA			0.5	V	
V _{OL} LOW-level output voltage, Receiver outputs	V _{CC} = MIN	I _{OL} = 20mA		0.5		V	
		I _{OL} = 12mA			0.5	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.4V		100		100	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _O = 0.5V		-100		-100	μA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 4.5V		25		25	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V	Driver, Receiver		-200		-200	μA
		Disabled		-25		-25	μA
I _{OS} Short-circuit output current ²	V _{CC} = MAX	Driver	-50	-150	-50	-150	mA
		Receiver	-30	-100	-30	-100	mA
I _{CC} Supply current	V _{CC} = MAX	8T26A		87		87	mA
		8T28		110		110	mA

NOTES

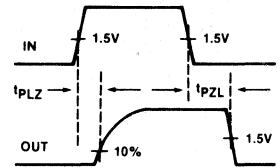
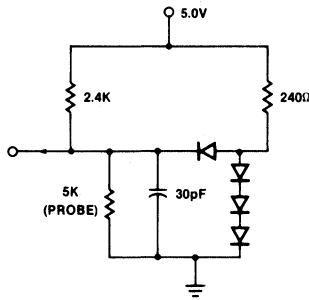
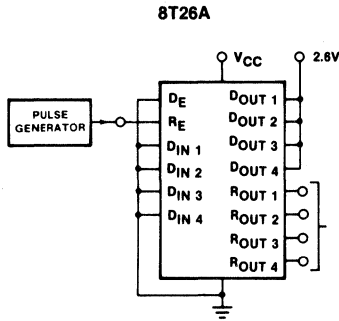
- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

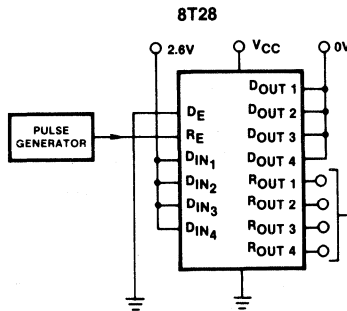
PARAMETER	TEST CONDITIONS	8T26A		8T28		UNIT
		Min	Max	Min	Max	
t _{PHL} Propagation delay, D _{OUT} to R _{OUT}	C _L = 30pF		14		17	ns
t _{PHL} Propagation delay, D _{IN} to D _{OUT}	C _L = 300pF		14		17	ns
t _{PLH} Propagation delay, D _{OUT} to R _{OUT}	C _L = 30pF		14		17	ns
t _{PLH} Propagation delay, D _{IN} to D _{OUT}	C _L = 300pF		14		17	ns
t _{PZL} Data enable to Data output, High Z to 0	C _L = 300pF		25		28	ns
t _{PLZ} Data enable to Data output, 0 to High Z	C _L = 300pF		20		23	ns
t _{PZL} Receive enable to Receive output, High Z to 0	C _L = 30pF		20		23	ns
t _{PLZ} Receive enable to Receive output, 0 to High Z	C _L = 30pF		15		18	ns

TEST CIRCUITS AND WAVEFORMS

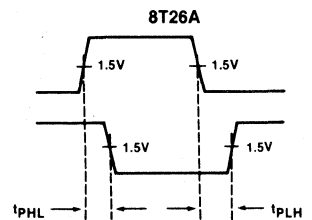
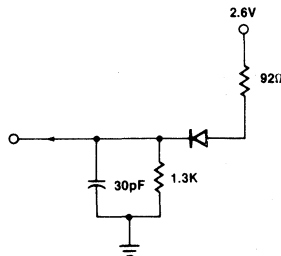
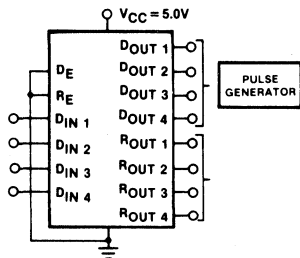
**DISABLE AND ENABLE TIME
RECEIVE ENABLE TO RECEIVE OUTPUT**



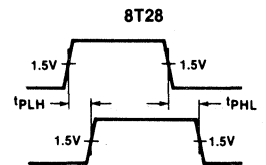
Input pulse:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 $f_{req} = 5\text{MHz}$ (50% duty cycle)
 Amplitude = 2.6V



**PROPAGATION DELAY
D_{OUT} TO R_{OUT}**

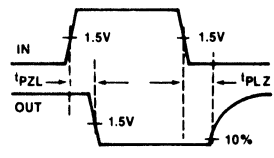
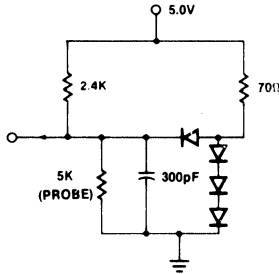
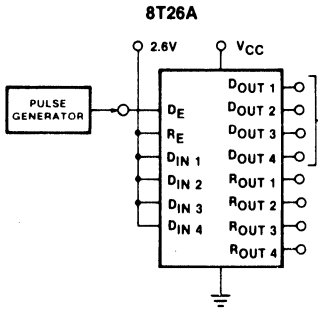


Input pulse:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 $f_{req} = 10\text{MHz}$ (50% duty cycle)
 Amplitude = 2.6V



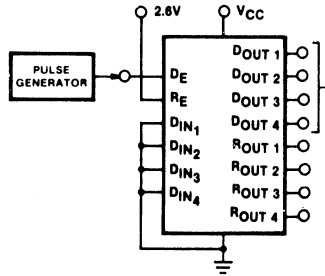
TEST CIRCUITS AND WAVEFORMS (Continued)

DISABLE AND ENABLE TIME
DATA ENABLE TO DATA OUTPUT



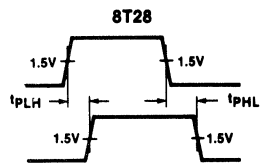
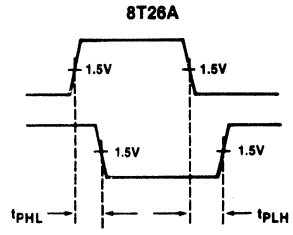
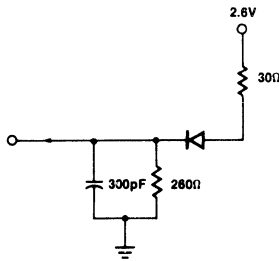
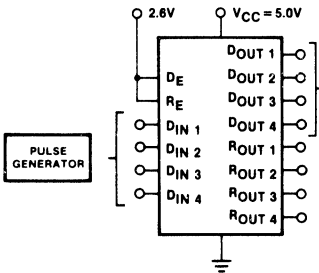
Input pulse:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 freq = 5MHz (50% duty cycle)
 Amplitude = 2.6V

8T28



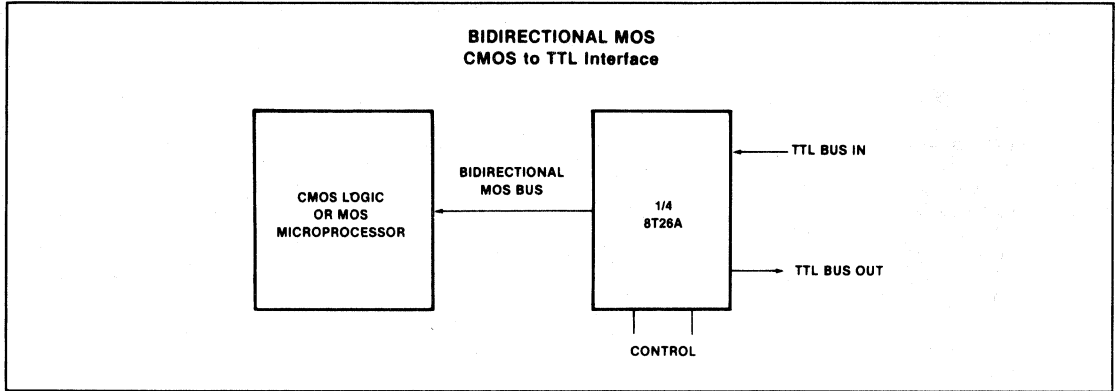
5

PROPAGATION DELAY
D_{IN} TO D_{OUT}

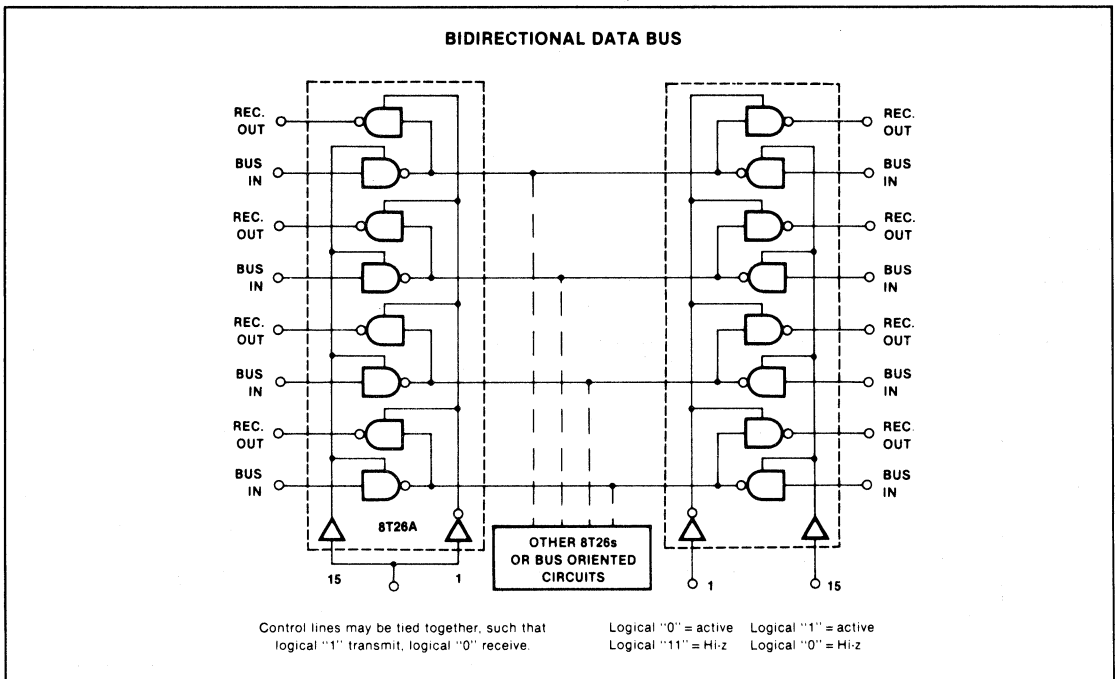


Input pulse:
 $t_r = t_f = 5\text{ns}$ (10% to 90%)
 $f_{req} = 10\text{MHz}$ (50% duty cycle)
 Amplitude = 2.6V

TYPICAL APPLICATION



TYPICAL APPLICATION



Hex Bus Receiver with Hysteresis — Schmitt Trigger

DESCRIPTION

The 8T37 is a hex bus receiver with hysteresis organized as two triple receivers with separate disable lines for each group. Typically the devices may be used in bus organized data transmission systems interconnected by terminated lines. The low input current requirement allows several drivers and receivers to communicate over a common bus in "party line" fashion. A power-up or power-down sequence of the receiver will not affect the bus. Built in hysteresis provides maximum noise immunity and makes the 8T37 also an ideal Schmitt trigger in those applications where the non-linear input characteristics of standard TTL are undesirable.

Low input current requirements make the nex-inverter inputs compatible with MOS/CMOS in addition to DTL/TTL. All inputs have clamping diodes to simplify systems design. The receiver outputs as well as the disable inputs are TTL/DTL compatible.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T37	10 ns	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{cc} = 5V ± 5%; T _A = 0°C to + 70°C
Plastic DIP	N8T37N

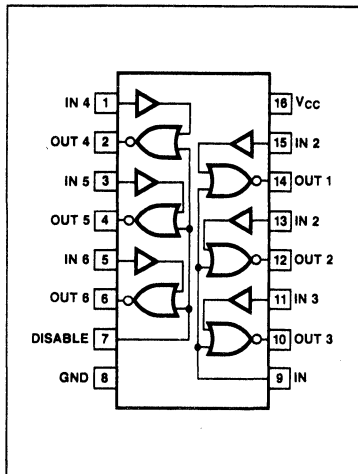
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
Disable	Input	2 ul
1N (Receiver)	Input	1.3 ul
OUT	Output	8 ul

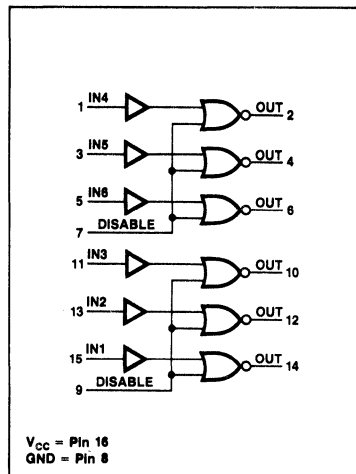
NOTE:

A unit load (ul) is 40 μA I_{IH} and - 1.6 mA I_{IL}.

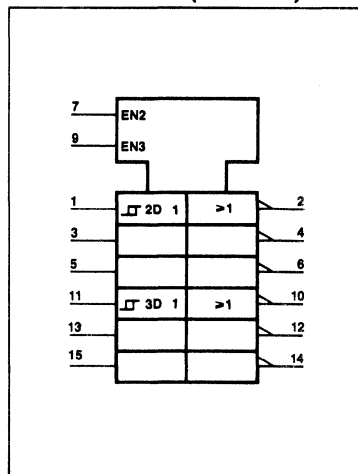
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUS RECEIVER**8T37****ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
I _{OL}	Continuous		mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
HIGH-level input voltage, Receiver	1.8		2.5	V
Disable	2.0			
LOW-level input voltage, Receiver	1.1		1.5	V
Disable			0.8	
I _{IK} Input clamp current			- 12	
I _{OH} HIGH-level output current			- 400	μA
I _{OL} LOW-level output current			16	mA
T _A Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹		8T37		UNIT
			Min	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	Receiver	1.8	2.5	V
		Disable	2.0		
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage	Receiver	1.1	1.5	V
		Disable		0.8	
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12 mA			- 1.5	V
V _{OH} HIGH-level output voltage	V _{CC} = MIN, I _{OH} = - 400 μA		2.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, I _{OL} = 16 mA			0.4	V
I _{IH} HIGH-level input current	V _{CC} = MAX	Receiver		50	μA
	V _{IN} = 2.4V	Disable		80	
	V _{CC} = 0	Others		50	
I _{IL} LOW-level input current	V _{CC} = MAX	Receiver		-50	μA
	V _{IN} = 0.4V	Disable		-3.2	mA
I _{OS} Short-circuit output current ²	V _{CC} = MAX		- 18	- 55	mA
I _{CC} Supply current (total)	V _{CC} = 5.25V			60	mA

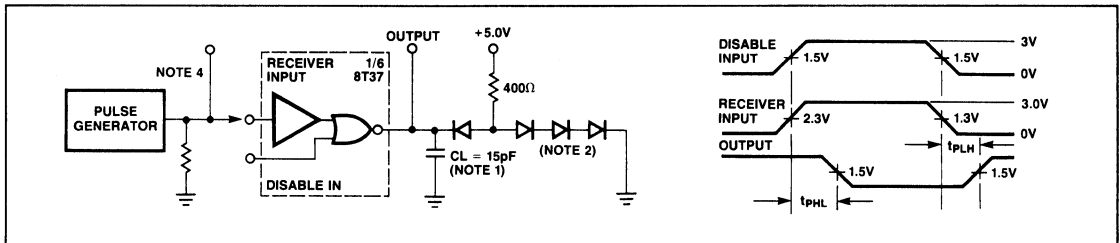
NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITION	LIMITS			UNIT
		MIN	TYP	MAX	
Propagation Delays					
Receiver	$R_L = 400\Omega$		10	30	ns
		$C_L = 15\text{pF}$		20	30
Disable	$C_L = 15\text{pF}$		9	15	ns
				11	15

AC TEST FIGURE AND WAVEFORMS



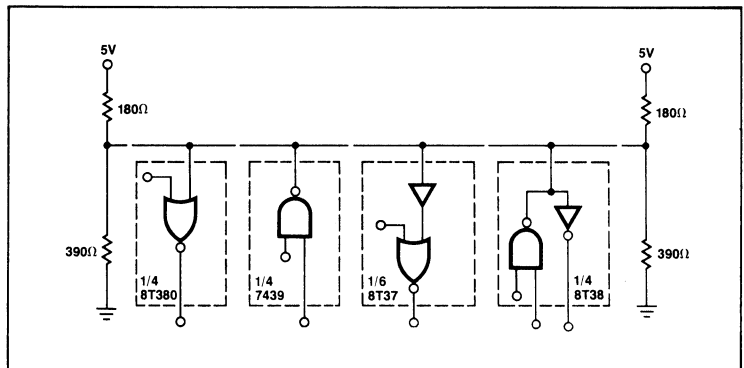
NOTES:

- Including probe and jib capacitance
- All diodes are 1N3064
- Pulse generator characteristics P.A. = 3.5V
 $Z_{OUT} = 50\Omega$
 $F_{RR} = 1\text{MHz}$
 $t_r = t_f \leq 10\text{ ns (10\% to 90\%)}$
 Duty Cycle = 50%
- When testing receiver, Disable = 0; when testing disable, Receiver = 0.

*TO BE ANNOUNCED

EACH TERMINATOR IS 120 OHMS THE VENINS EQUIVALENT CIRCUIT. USING FLAT RIBBON A MAXIMUM REASONABLE LENGTH IS 50 FT. FROM WHICH THE COMBINED LENGTH OF ALL TAPS OR STUBS SHOULD BE SUBTRACTED.

TYPICAL APPLICATION



5

Quad Bus Transceiver (Open Collector)

DESCRIPTION

The 8T38 is a quad bus transceiver with a common two input disable control for the drivers. Open collector driver outputs together with low input requirements for the receivers offer extreme versatility in low cost bus organized systems.

Busses may be terminated at both ends such that up to 100 driver/receiver pairs can utilize a common data bus. The receiver incorporates hysteresis to provide maximum noise immunity. In addition the receiver does not load the bus when $V_{CC} = 0$.

In those applications where only bus receiver are required the 8T380 quad bus receiver should be considered.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T38	19 ns (t _{PHL}) 23 ns (t _{PLH})	

ORDERING CODE

PACKAGES	COMMERCIAL RANGES
Plastic DIP	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C \text{ to } +70^\circ C$ N8T38N

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

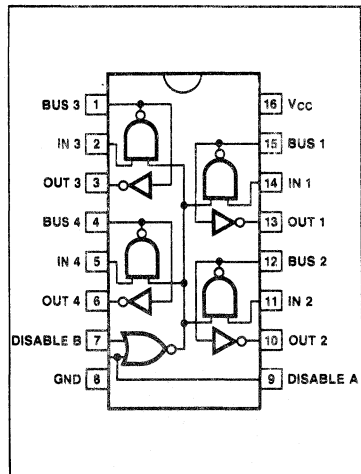
PINS	DESCRIPTION	8T
BUS	Receiver Input	1.2 uI
DISABLE	Disable Input	2.5 uI
BUS	Driver Output	31 uI
OUT	Receiver Output	10 uI

NOTE:
A unit load (uI) is 40 μA I_{IH} and -1.6 mA I_{IL} .

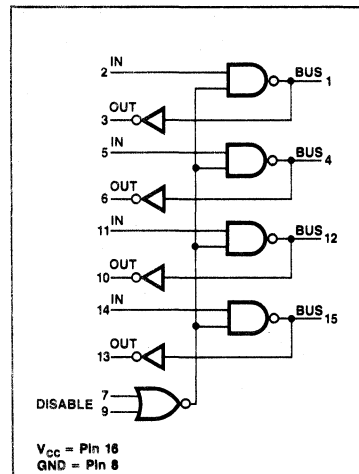
FUNCTION TABLE

MODE	DISABLE	DISABLE	DRIVER	BUS	RECEIVER
	A	B	IN	OUT	OUT
RECEIVE	1	X	X	1	0
RECEIVE	X	1	X	1	0
DRIVE	0	0	1	0	1
DRIVE	0	0	0	1	0

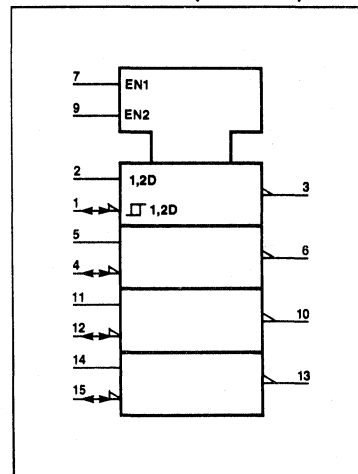
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V _{CC}	Supply voltage	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	V
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT	
	Min	Nom	Max		
V _{CC}	Supply voltage	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage, Disable	2.0		2.5	V
V _{IH}	HIGH-level input voltage, Receiver	1.8		2.5	V
V _{IL}	LOW-level input voltage, Disable			0.8	V
V _{IL}	LOW-level input voltage, Receiver	1.1		1.5	V
I _{IK}	Input clamp current			- 12	mA
I _{OH}	HIGH-level output current, Receiver			- 100	mA
I _{OL}	LOW-level output current, Driver			50	mA
I _{OL}	LOW-level output current, Receiver			16	mA
T _A	Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹	8T38		UNIT	
		Min	Max		
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	Receiver	1.8	2.5	V
		Disable	2.0		
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage	Receiver	1.1	1.5	V
		Disable		0.8	
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12 mA			- 1.5	V
V _{OH} HIGH-level output voltage	V _{CC} = MIN, I _{OH} = - 5.2 mA	2.4			V
V _{OL} LOW-level output voltage	V _{CC} = MIN	I _{OL} = 50 mA	Driver	0.5	V
		I _{OL} = 16 mA	Receiver	0.5	
I _{IH} HIGH-level input current	V _{CC} = MAX V _{IN} = 2.4V V _{CC} = 0	Receiver		50	μA
		Disable		100	
		Others		100	
I _{IL} LOW-level input current	V _{CC} = MAX V _{IN} = 0.5V	Receiver		- 50	μA
		Disable			mA
I _{OS} Short-circuit output current ²	V _{CC} = MAX	- 18	- 55		mA
I _{CC} Supply current (total)	V _{CC} = 5.25V		60		mA

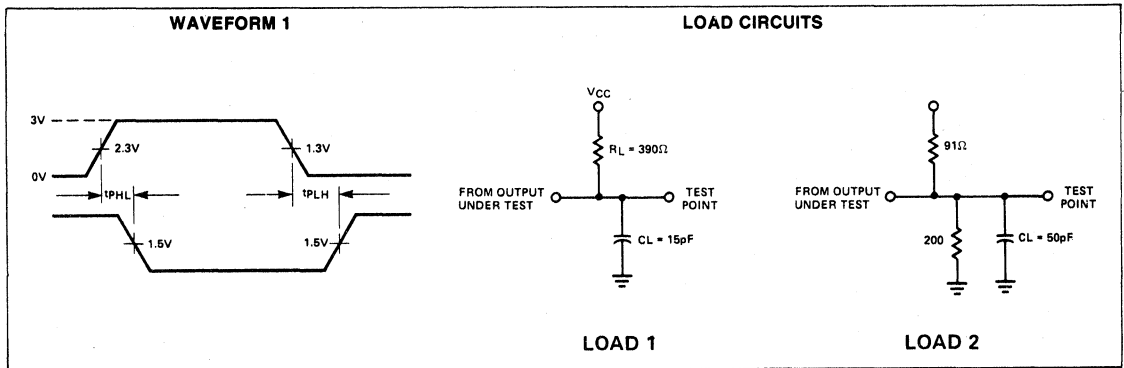
NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

PARAMETER	TEST CONDITIONS	8T			UNIT
		Min	Typ	Max	
t_{PHL} Disable Bus	Load 2 $V_{IN} = 0\text{V to } 3\text{V}$	11	19	30	ns
t_{PLH} Disable to Bus	Measured from $V_{IN} = 1.5\text{V to } V_{bus} = 1.5\text{V}$	15	23	35	ns
t_{PHL} Driver to Bus	Load 1 Waveform 1	5	12	20	ns
t_{PLH} Driver to Bus		5	12	25	ns
t_{PHL} Bus to Receiver		5	14	25	ns
t_{PLH} Bus to Receiver		12	27	40	ns

SWITCHING PARAMETERS MEASUREMENT INFORMATION



HEX BUFFERS/INVERTERS

8T95, 96, 97, 98

High Speed Hex 3-State Buffers High Speed Hex 3-State Inverters

DESCRIPTION

Each of the 3-state bus interface elements described herein has low current PNP inputs and is designed with Schottky TTL technology for ultra high speed. The devices are used to convert TTL/DTL or MOS/CMOS to 3-state TTL bus levels. For maximum systems flexibility, the 8T95 and 8T97 do so without logic inversion, whereas the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six devices, whereas the 8T97 and 8T98 have control lines for four devices from one input and two from another input.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T95	8ns	65mA
N8T96	6.5ns	59mA
N8T97	8ns	65mA
N8T98	6.5ns	59mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	
Plastic DIP	N8T95N • N8T96N N8T97N • N8T98N	
Plastic SO	N8T97D • N8T98D	
Ceramic DIP		S8T95F • S8T98F S8T97F

FUNCTION TABLE—8T95

INPUTS			OUTPUT
DIS ₁	DIS ₂	I	Y
L	L	L	L
L	L	H	H
X	H	X	(Z)
H	X	X	(Z)

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
DIS	Input	1Sul
I	Input	1Sul
Y	Output	24Sul

NOTE
A unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} .

FUNCTION TABLE—8T96

INPUTS			OUTPUT
DIS ₁	DIS ₂	I	\bar{Y}
L	L	L	H
L	L	H	L
X	H	X	(Z)
H	X	X	(Z)

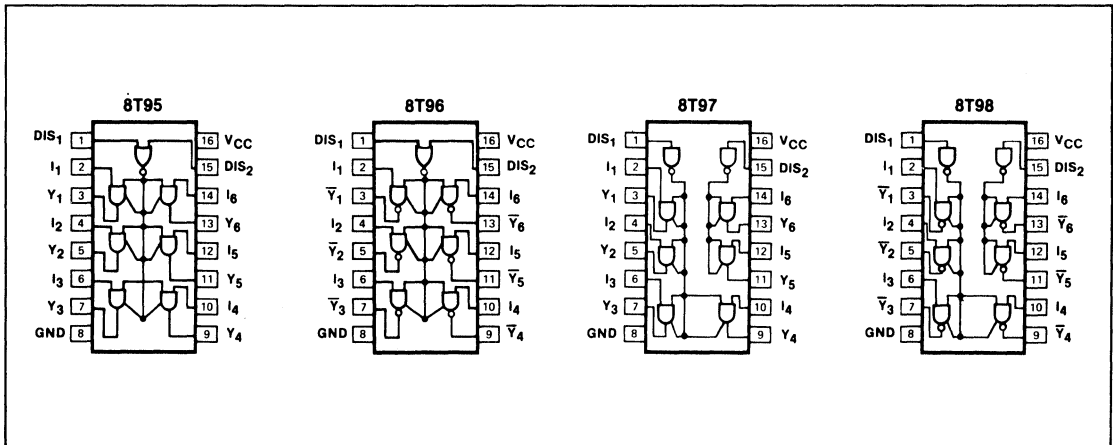
FUNCTION TABLE—8T97

INPUTS		OUTPUT
DIS	I	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE—8T98

INPUTS		OUTPUT
DIS	I	\bar{Y}
L	L	H
L	H	L
H	X	(Z)

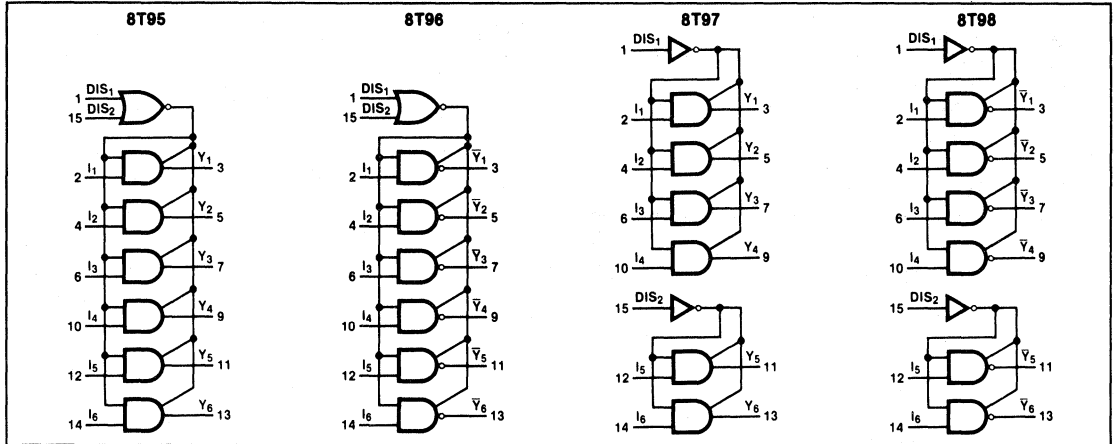
PIN CONFIGURATION



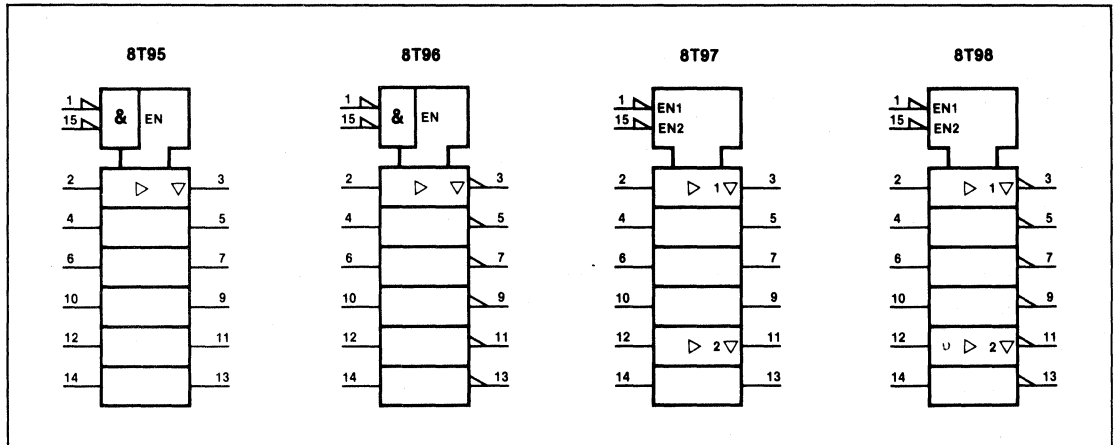
HEX BUFFERS/INVERTERS

8T95, 96, 97, 98

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	S8T	N8T	UNIT
V _{CC} Supply voltage	7.0	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	-30 to +5	mA
I _{OL} Continuous	100	100	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	-55 to +125	0 to 70	°C

HEX BUFFERS/INVERTERS

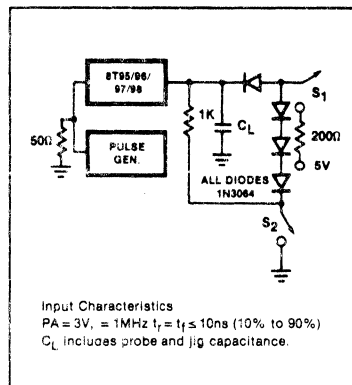
8T95, 96, 97, 98

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			V	
V _{IL}	LOW-level input voltage	Mil		+ 0.8	V	
		Com'l		+ 0.8	V	
I _{IH}	Input clamp current			- 18	mA	
I _{OH}	HIGH-level output current			- 5.2	mA	
I _{OL}	LOW-level output current	Mil		48	mA	
		Com'l		48	mA	
T _A	Operating free-air temperature	Mil	- 55	+ 125	°C	
		Com'l	0	70	°C	

NOTE
V_{IL} = + 0.7V for S8T only.

TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T95/97		8T96/98		UNIT				
		Min	Max	Min	Max					
V _{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage				2.0	2.0	V		
V _{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage					0.8	0.8	V	
V _{IK}	Input clamp diode voltage	V _{CC} = MIN, I _{IK} = - 12mA					- 1.5	- 1.5	V	
V _{BD}	Input breakdown voltage	V _{CC} = MAX, I _I = 1mA				5.5		5.5	V	
V _{OH}	HIGH-level output voltage	V _{CC} = MIN, I _{OH} = - 5.2mA				2.4		2.4	V	
V _{OL}	LOW-level output voltage	V _{CC} = MIN, I _{OL} = 48mA					0.5 ³	0.5 ³	V	
I _{ozH}	Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.4V					40	40	μA	
I _{ozL}	Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _O = 0.5V					- 40	- 40	μA	
I _{IH}	HIGH-level input current	V _{CC} = MAX, V _I = 2.4V					40	40	μA	
I _{IL}	LOW-level input current	V _{CC} = MAX, V _I = 0.5V		Disable = 0.5V			- 400	- 400	μA	
				Disable = 2.0V			- 40	- 40	μA	
I _{OS}	Short-circuit output current ²	V _{CC} = MAX				- 40	- 115	- 40	- 115	mA
I _{CC}	Supply current (total)	V _{CC} = MAX					98		89	mA

- NOTES
 1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
 2. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
 3. V_{OL} = + 0.45V MAX for S8T at T_A = + 125°C only.

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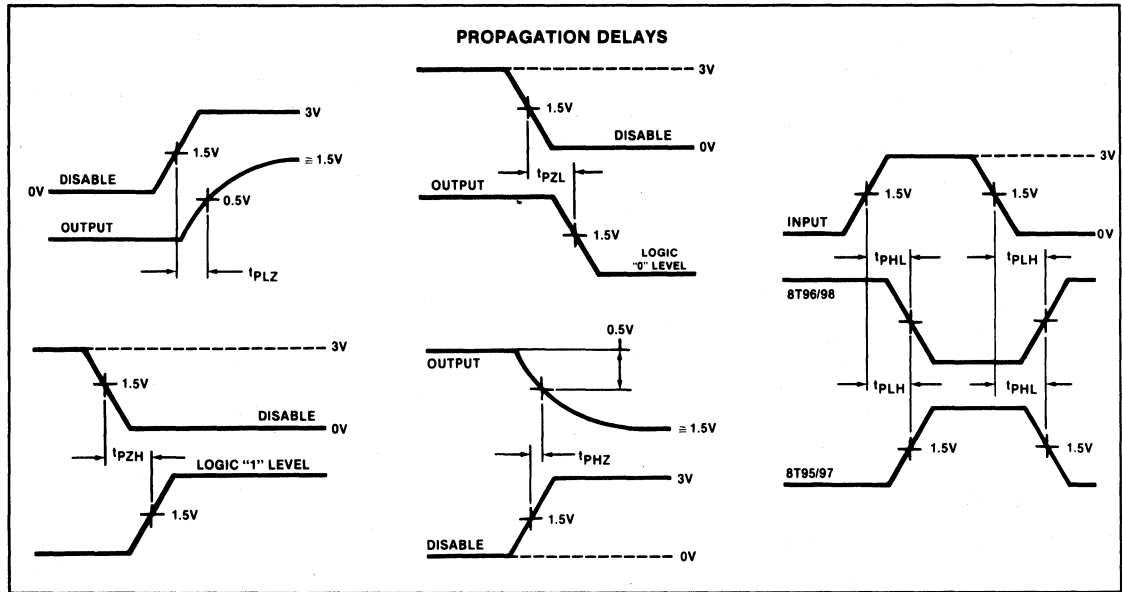
HEX BUFFERS/INVERTERS

8T95, 96, 97, 98

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8T95/97		8T96/98		UNIT
		$R_L = 200\Omega$		$R_L = 200\Omega$		
		Min	Max	Min	Max	
t_{PLH} Propagation delay Data inputs to Data outputs	S_1, S_2 are closed, $C_L = 50\text{pF}$		12		11	ns
t_{PHL} Propagation delay Data inputs to Data outputs	S_1, S_2 are closed, $C_L = 50\text{pF}$		13		10	ns
t_{PZH} Disable to outputs High Z to Logic "1"	S_1 is open, S_2 is closed, $C_L = 50\text{pF}$		25		22	ns
t_{PZL} Disable to outputs High Z to Logic "0"	S_1 is closed, S_2 is open, $C_L = 50\text{pF}$		25		24	ns
t_{PHZ} Disable to outputs Logic "1" to High Z	S_1, S_2 are closed, $C_L = 5\text{pF}$		10		10	ns
t_{PLZ} Disable to outputs Logic "0" to High Z	S_1, S_2 are closed, $C_L = 5\text{pF}$		12		16	ns

AC WAVEFORMS



TRANSCEIVER

8T125

Octal 3-State Transceiver

- Octal bidirectional bus interface
- 3-State buffer outputs
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- Pin compatible with 54LS/74LS245

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T125	7.5ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%; T_A = 0^\circ C \text{ to } +70^\circ C$	$V_{CC} = 5V \pm 10\%; T_A = -55^\circ C \text{ to } +125^\circ C$
Plastic DIP	N8T125N	
Ceramic DIP		S8T125F

DESCRIPTION

The 8T125 is an octal transceiver featuring inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable input for easy cascading and a Send/Receive input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{CE}	S/R	A_n	B_n
L	L	$A = \overline{B}$	INPUTS
L	H	INPUT	$B = \overline{A}$
H	X	(Z)	(Z)

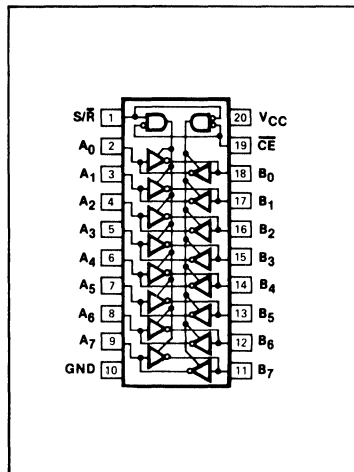
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 (Z) = HIGH impedance "off" state

INPUT AND OUTUT LOADING AND FAN-OUT TABLE

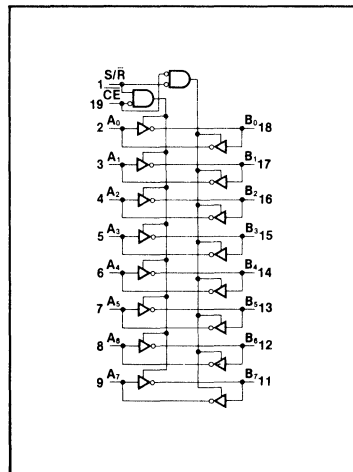
PINS	DESCRIPTION	8T125
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
 A unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

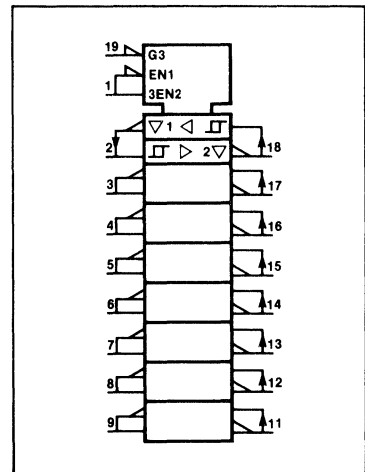
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVER

8T125

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		8T	N8T	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	Transceiver Inputs	- 0.5 to +5.5	V
		Non-Transceiver Inputs	- 0.5 to +7.0	V
I _{OL}	Continuous	50	50	mA
I _{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT		
		Min	Nom	Max			
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	V	
V _{IH}	HIGH-level input voltage	2.0			V		
V _{IL}	LOW-level input voltage	Mil			+ 0.7	V	
		Com'l			+ 0.8	V	
I _{IK}	Input clamp current				- 18	mA	
I _{OH}	HIGH-level output current	Mil			- 12	mA	
		Com'l			- 15	mA	
I _{OL}	LOW-level output current	Mil			12	mA	
		Com'l			24	mA	
T _A	Operating free-air temperature	Mil	- 55			+ 125	°C
		Com'l	0			70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
t _{pZH}	Open	Closed
t _{pZL}	Closed	Open
t _{pHZ}	Closed	Closed
t _{pLZ}	Closed	Closed

DEFINITIONS
 R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 R_X = 1kΩ for 54/74, 54S/74S; R_X = 5kΩ for 54LS/74LS.
 t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

INPUT PULSE REQUIREMENTS

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t _{TLH}	t _{THL}
8T	3.0V	1MHz	500ns	15ns	6ns

TRANSCEIVER

8T125

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T125		UNIT	
		Min	Max		
ΔV_T Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = \text{MIN}$	0.2		V	
V_{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		V	
V_{IL} Input LOW voltage	Guaranteed input LOW threshold voltage		0.8	V	
V_{IK} Input clamp diode voltage	$V_{CC} = \text{MIN}, I_{IK} = -18\text{mA}$		-1.5	V	
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -2.0\text{mA}$ Mil	2.4	V	
		$I_{OH} = -3.0\text{mA}$ Com'l	2.4	V	
		$I_{OH} = -12\text{mA}$ Mil	2.0	V	
		$I_{OH} = -15\text{mA}$ Com'l	2.0	V	
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 12\text{mA}$	Mil	0.4	V
			Com'l	0.4	V
		$I_{OL} = 24\text{mA}$ Com'l		0.5	V
I_{OZH} Off-state output current, HIGH-level voltage applied	$V_{CC} = \text{MAX}, V_O = 2.4\text{V}$		20	μA	
I_{OZL} Off-state output current, LOW-level voltage applied	$V_{CC} = \text{MAX}, V_O = 0.4\text{V}$		-200	μA	
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.4\text{V}$		20	μA	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	$V_I = 5.5\text{V}$ Transceiver inputs		100	μA
		$V_I = 7.0\text{V}$ Non-Transceiver inputs		100	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.4\text{V}$			-200	μA
I_{OS} Short-circuit output current ²	$V_{CC} = \text{MAX}$	-40	-120	mA	
I_{CCH} Supply current HIGH	$V_{CC} = \text{MAX}$, outputs HIGH			70	mA
I_{CCL} Supply current LOW	$V_{CC} = \text{MAX}$, outputs LOW			90	mA
I_{CCZ} Supply current "off"	$V_{CC} = \text{MAX}$, outputs "off"			95	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.

2. I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC\text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

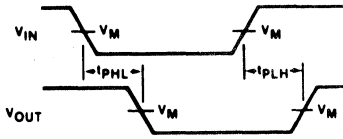
AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8T		UNIT
		$R_L = 667\Omega$		
		Min	Max	
t_{PLH} Propagation delay t_{PHL} Input to output	Waveform 1, $C_L = 45\text{pF}$		12 12	ns
t_{PZH} Enable to HIGH	Waveform 2, $C_L = 45\text{pF}$		40	ns
t_{PZL} Enable to LOW	Waveform 3, $C_L = 45\text{pF}$		40	ns
t_{PHZ} Disable from HIGH	Waveform 2, $C_L = 5\text{pF}$		25	ns
t_{PLZ} Disable from LOW	Waveform 3, $C_L = 5\text{pF}$		25	ns

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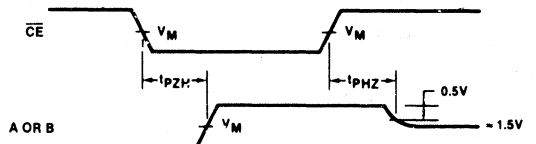
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

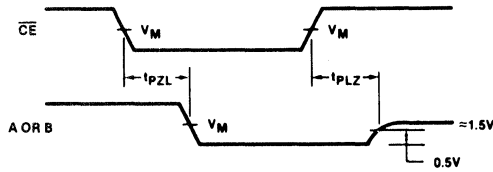
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

$V_M = 1.3V$

3-STATE EN'ABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

TRANSCEIVERS

8T126, 127, 128, 129

Quad, 3-State Transceivers

DESCRIPTION

The 8T126 through 8T129 are quad transceivers designed to handle many bus interface applications. The devices feature 3-State outputs on both send and receive buffers, and pnp transistors on all inputs to reduce input LOW loading requirements.

The 8T126 and 8T128 feature a 3.4V minimum V_{OH} level on the receiver for MOS interface applications. The send and receive buffers have separate Enable inputs for independent control.

The 8T127 and 8T129 feature full 24mA drive in both send and receive buffers. These devices have a common Chip Enable input for easy cascading and a Send/Receive input for direction control.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T126	10ns (Data)	17mA
N8T127	9ns (Data)	21mA
N8T128	10ns (Data)	17mA
N8T129	9ns (Data)	21mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N8T126N • N8T127N N8T128N • N8T129N	
Ceramic DIP		S8T126F • S8T127F S8T128F • S8T129F
Flatpack		S8T126W • S8T127W S8T128W • S8T129W

FUNCTION TABLES

8T126

INPUTS			RECV. OUT	BUS I/O
SE	\overline{RE}	D_n	A_n	B_n
L	L	X	$A = \overline{B}$	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	H
H	H	H	(Z)	L
H	L	L	L	H
H	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(X) = HIGH impedance "off" state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
ALL	Input	1 ul
ALL	Output	60 ul

NOTE:
A unit load (ul) is $20 \mu A$ I_{IH} and $-0.4 mA$ I_{IL} .

8T127

INPUTS			RECV. OUT	BUS I/O
\overline{CE}	S/\overline{R}	D_n	A_n	B_n
L	L	X	$A = \overline{B}$	INPUTS
L	H	L	(Z)	H
L	H	H	(Z)	L
H	X	X	(Z)	(Z)

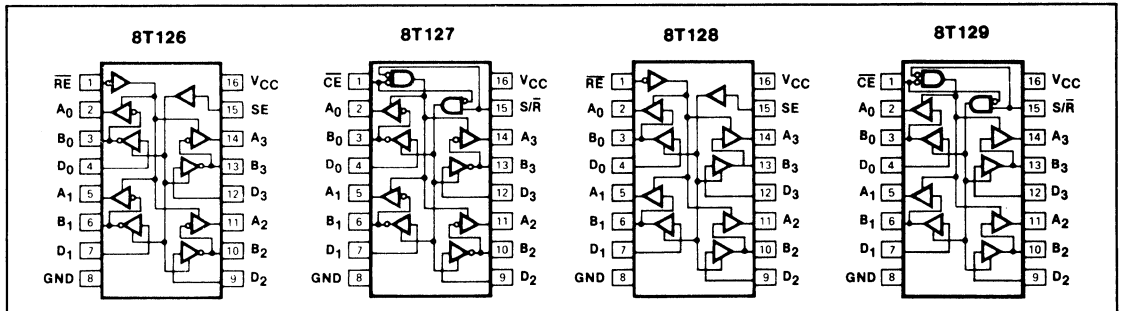
8T128

INPUTS			RECV. OUT	BUS I/O
SE	\overline{RE}	D_n	A_n	B_n
L	L	X	$A = B$	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	L
H	H	H	(Z)	H
H	L	L	L	L
H	L	H	H	H

8T129

INPUTS			RECV. OUT	BUS I/O
\overline{CE}	S/\overline{R}	D_n	A_n	B_n
L	L	X	$A = B$	INPUTS
L	H	L	(Z)	L
L	H	H	(Z)	H
H	X	X	(Z)	(Z)

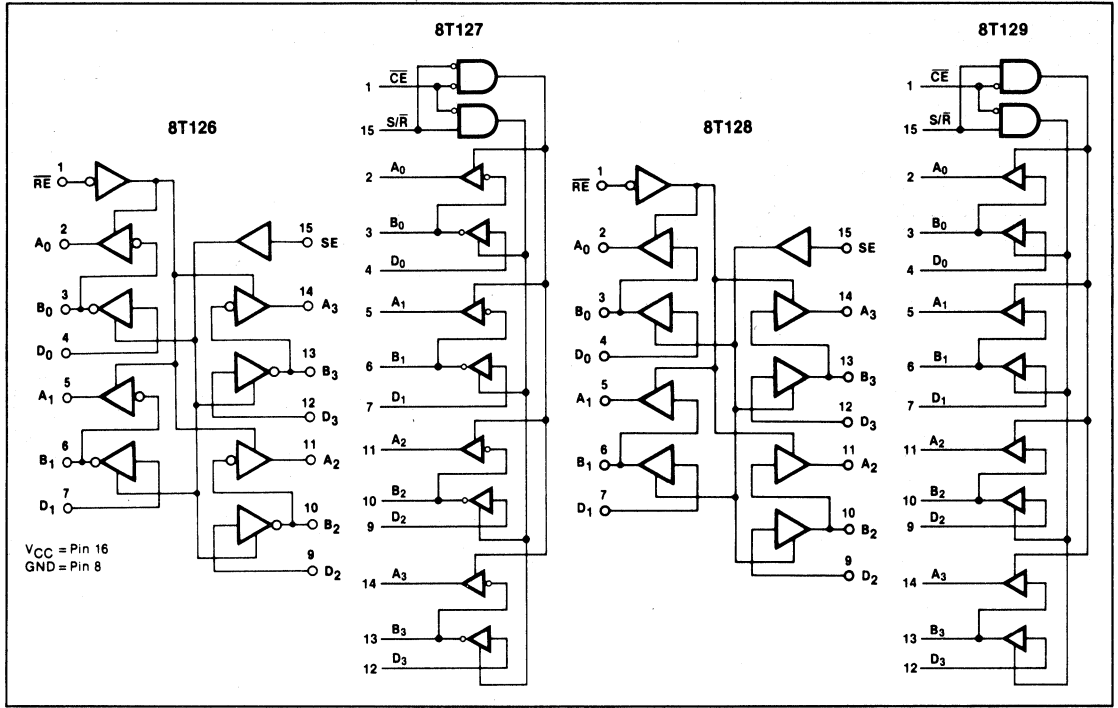
PIN CONFIGURATION



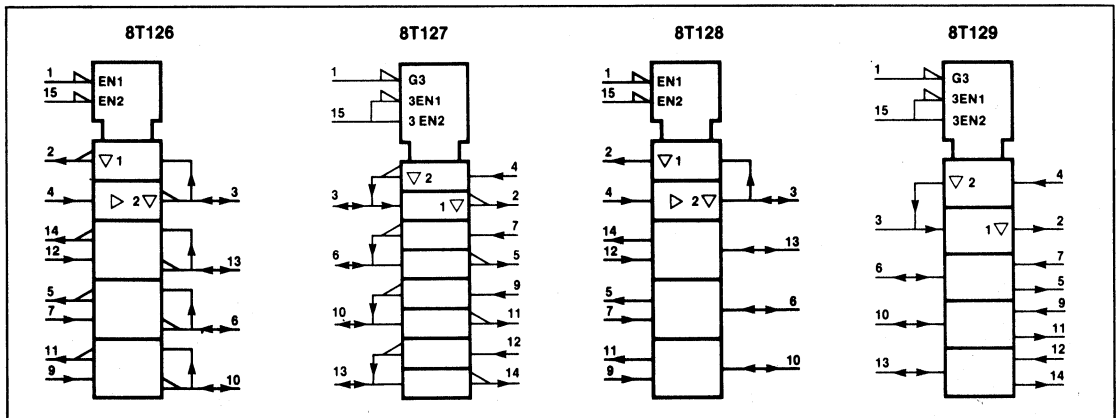
TRANSCEIVERS

8T126, 127, 128, 129

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVERS

8T126, 127, 128, 129

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8T	N8T	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Transceiver inputs	- 0.5 to +5.5	- 0.5 to +5.5	V
	Non-Transceiver inputs	- 0.5 to +7.0	- 0.5 to +7.0	V
I _{IN}	Input current	- 30 to + 1	- 30 to + 1	mA
I _{OL}	Continuous	50	50	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETERS			8T126/8T128			8T127/8T129			UNIT	
			Min	Nom	Max	Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V	
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V	
V _{IH}	HIGH-level input voltage		2.0			2.0		V		
V _{IL}	LOW-level input voltage	Mil			0.7			0.7	V	
		Com'l			0.8			0.8	V	
I _{IK}	Input clamp current			- 18			- 18	mA		
I _{OH}	HIGH-level output current	Bus	Mil		- 2.0			- 2.0	mA	
			Com'l			- 5.2			- 5.2	mA
		Receiver	Mil			- 1.0			- 2.0	mA
			Com'l			- 2.6			- 5.2	mA
I _{OL}	LOW-level output current	Bus	Mil		12			12	mA	
			Com'l			24			24	mA
		Receiver	Mil			6			12	mA
			Com'l			12			24	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	- 55		+ 125	°C	
		Com'l	0		70	0		70	°C	

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TRANSCEIVERS

8T126, 127, 128, 129

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8T126/8T128		8T127/8T129		UNIT
		Min	Max	Min	Max	
V _{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0		2.0		V
V _{IL} Input LOW voltage	Guaranteed input LOW threshold voltage	Mil	0.7		0.7	V
		Com'l	0.8		0.8	V
V _{IK} Input clamp diode voltage	V _{CC} = MIN, I _{IK} = -18mA		-1.5		-1.5	V
V _{OH} HIGH-level output voltage, Bus outputs	V _{CC} = MIN	I _{OH} = -2.0mA	Mil	2.4	2.4	V
		I _{OH} = -5.2mA	Com'l	2.4	2.4	V
V _{OH} HIGH-level output voltage, Receiver outputs	V _{CC} = MIN, V _{IN} = V _{IL} , or V _{IH} per Function Table	I _{OH} = -100μA	Mil	3.1		V
		I _{OH} = -100μA	Com'l	3.4		V
		I _{OH} = -1.0mA	Mil	2.4		V
		I _{OH} = -2.0mA	Mil		2.4	V
		I _{OH} = -2.6mA	Com'l	2.4		V
		I _{OH} = -5.2mA	Com'l		2.4	V
V _{OL} LOW-level output voltage, Bus outputs	V _{CC} = MIN	I _{OL} = 12mA	Mil & Com'l	0.4	0.4	V
		I _{OL} = 24mA	Com'l	0.5	0.5	V
V _{OL} LOW-level output voltage, Receiver outputs	V _{CC} = MIN	I _{OL} = 6mA	Mil & Com'l	0.4		V
		I _{OL} = 12mA	Mil & Com'l		0.4	V
		I _{OL} = 12mA	Com'l	0.5		V
		I _{OL} = 24mA	Com'l		0.5	V
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _O = 2.4V		20		20	μA
I _{OZL} Off-state output current, LOW-level voltage applied, Receiver outputs	V _{CC} = MAX, V _O = 0.4V		-20		-20	μA
I _{OZL} Off-state output current, LOW-level voltage applied, Bus outputs	V _{CC} = MAX, V _O = 0.4V		-100		-200	μA
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V		20		20	μA
I _I Input current at maximum input voltage	V _{CC} = MAX	Bus inputs	V _I = 5.5V	100	100	μA
		Others	V _I = 7.0V	100	100	μA
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.4V		-100		-200	μA
I _{OS} Short-circuit output current ²	V _{CC} = MAX	-40	-120	-40	-120	mA
I _{CCH} Supply current HIGH	V _{CC} = MAX, outputs HIGH		26		36	mA
I _{CCL} Supply current LOW	V _{CC} = MAX, outputs LOW		30		42	mA
I _{CCZ} Supply current "off"	V _{CC} = MAX, outputs "off"		36		44	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

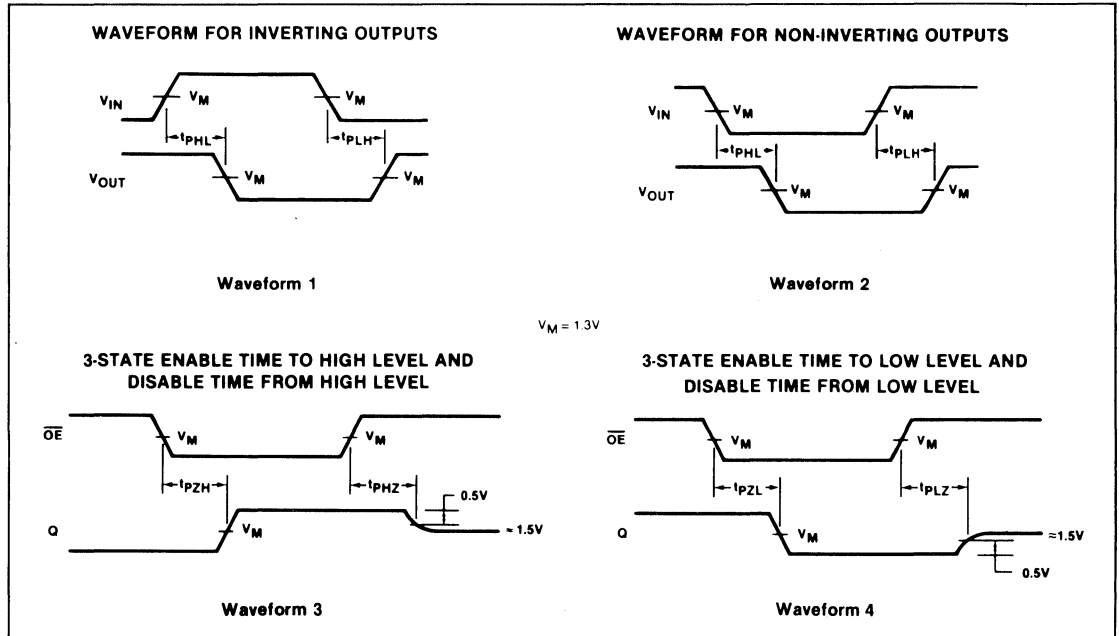
TRANSCEIVERS

8T126, 127, 128, 129

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

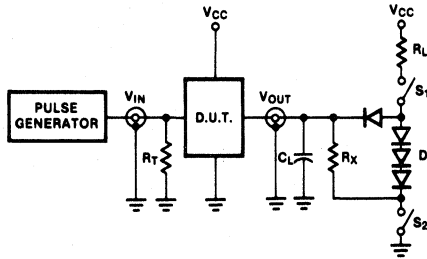
PARAMETER	TEST CONDITIONS	8T126/8T128		8T127/8T129		UNIT
		Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Bus output		20 30		20 30	ns
t_{PLH} t_{PHL}	Propagation delay Bus to Receiver output		20 30		20 25	ns
t_{PZH}	Enable to HIGH for Bus output		30		35	ns
t_{PZH}	Enable to HIGH for Receiver output		25		30	ns
t_{PZL}	Enable to LOW for Bus output		35		35	ns
t_{PZL}	Enable to LOW for Receiver output		30		30	ns
t_{PHZ}	Disable from HIGH	Waveform 3, $C_L = 5\text{pF}$, $R_L = 667\Omega$, Com'l	25		25	ns
		Waveform 3, $C_L = 50\text{pF}$, $R_L = 667\Omega$, Mil	63		63	ns
		Waveform 3, $C_L = 100\text{pF}$, $R_L = 667\Omega$, Mil	102		102	ns
t_{PLZ}	Disable from LOW	Waveform 4, $C_L = 5\text{pF}$, $R_L = 667\Omega$, Com'l	25		25	ns
		Waveform 4, $C_L = 50\text{pF}$, $R_L = 667\Omega$, Mil	29		29	ns
		Waveform 4, $C_L = 100\text{pF}$, $R_L = 667\Omega$, Mil	33		33	ns

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



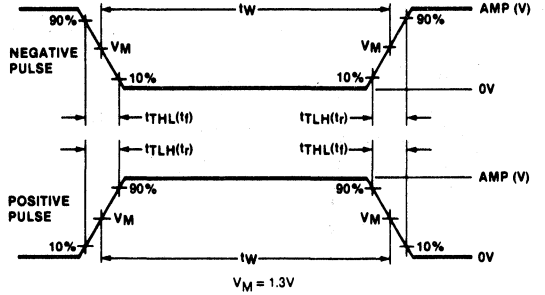
SWITCH POSITION

Test	Switch 1	Switch 2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pHZ}	Closed	Closed
t_{pLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 $R_X = 1k\Omega$ for 54/74, 54S/74S, $R_X = 5k\Omega$ for 54LS/74LS.
 t_{TLH} - t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8T	3.0V	1MHz	500ns	15ns	6ns

Quad Bus Receiver with Hysteresis-Schmitt Trigger

DESCRIPTION

The 8T380 is a quad 2-input bus receiver with hysteresis for use in I/O, data, and memory busses. Built-in hysteresis provides maximum noise immunity and a power-up or power-down sequence on the receiver will not affect the bus. LOW input current allows several drivers and receivers to communicate over a common bus in "Party line" fashion. The 8T380 is ideal as a Schmitt Trigger in analog interfaces that cannot tolerate the non-linear input impedance characteristics of standard TTL. Further, the LOW input requirements allow the 8T380 to be used as a CMOS to TTL interface. All inputs have clamping diodes to simplify systems design.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T380	20ns (t _{PLH}) 16ns (t _{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{CC} = 5V ± 5%; T _A = 0°C to + 70°C
Plastic DIP	N8T380N
Plastic SO	N8T380D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
ALL	Input	1.2 ul
ALL	Output	10 ul

NOTE:

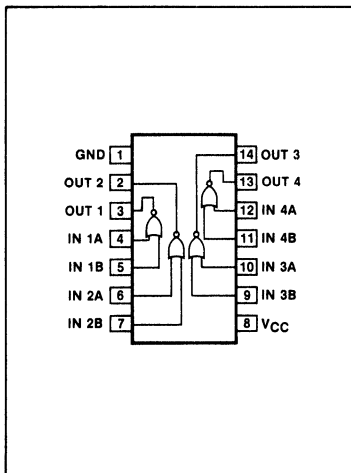
A unit load (ul) is 40 μA I_{IH} and - 1.6 mA I_{IL}.

FUNCTION TABLE

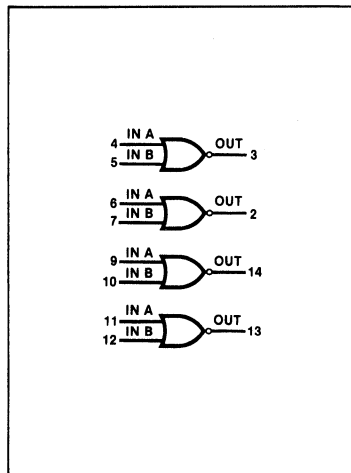
INPUTS		OUTPUT
A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

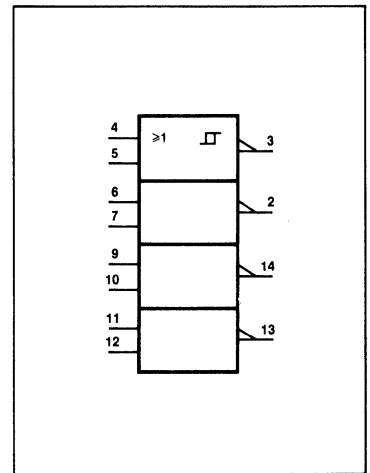
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUS RECEIVER**8T380****ABSOLUTE MAXIMUM RATINGS** (Over operating free-air temperature range unless otherwise noted).

PARAMETER	8T	UNIT
V_{CC} Supply voltage	7.0	V
V_{IN} Input voltage	- 0.5 to + 5.5	V
I_{OL} Continuous	30	mA
V_{OUT} Voltage applied to output in HIGH output state	- 0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT
	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0		2.5	V
V_{IL} LOW-level input voltage	1.1		1.5	V
I_{IK} Input clamp current			- 12	mA
I_{OH} HIGH-level output current			- 400	μ A
I_{OL} LOW-level output current			16	mA
T_A Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹	8T380		UNIT
		Min	Max	
V_{IH} Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0	2.5	V
V_{IL} Input LOW voltage	Guaranteed input LOW threshold voltage	1.1	1.5	V
V_{IK} Input clamp diode voltage	$V_{CC} = \text{MIN}$, $I_{IK} = - 12\text{mA}$		- 1.5	V
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $I_{OH} = - 400\mu\text{A}$	2.4		V
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $I_{OL} = 16\text{mA}$		0.4	V
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$, $V_I = 4.5\text{V}$		50	μ A
	$V_{CC} = 0\text{V}$, $V_I = 4.5\text{V}$		50	μ A
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$, $V_I = 0\text{V}$		- 25	μ A
I_{OS} Short-circuit output current ²	$V_{CC} = \text{MAX}$	- 18	- 55	mA
I_{CC} Supply current (total)	$V_{CC} = 5.25\text{V}$		40	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- I_{OS} is tested with $V_{OUT} = + 0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

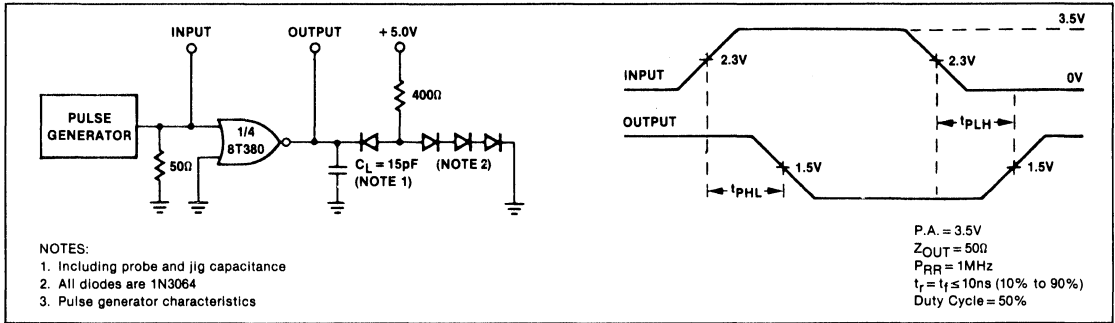
BUS RECEIVER

8T380

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8T		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		
		Min	Max	
t_{PLH} Propagation delay	See Test Circuits and Waveforms		35	ns
t_{PHL} Input to output			35	

TEST CIRCUITS AND WAVEFORMS



TYPICAL APPLICATIONS

A generalized "Party Line" bus interface is shown in Figure 1. Each driver/receiver combination can communicate with any other pair or all. Open collector NAND Gates such as the Signetics 7439 have adequate drive capability for the bus terminations as well as 20 driver/receiver pairs. In addition the bussing scheme is non-inverting as shown and bus drivers are activated by a logic "1" whereas bus receivers are activated by a Logic "0."

Each termination consisting of a 180 ohm resistor to V_{CC} and 390 ohm to ground is a 120 ohm Thevenin's equivalent circuit. The maximum length of cable that can be driven is a complex relationship involving the type of cable used as well as the distribution of drivers and receivers on the bus. Using flat ribbon cable, a maximum reasonable length is 50 ft. minus the combined length of all taps or stubs.

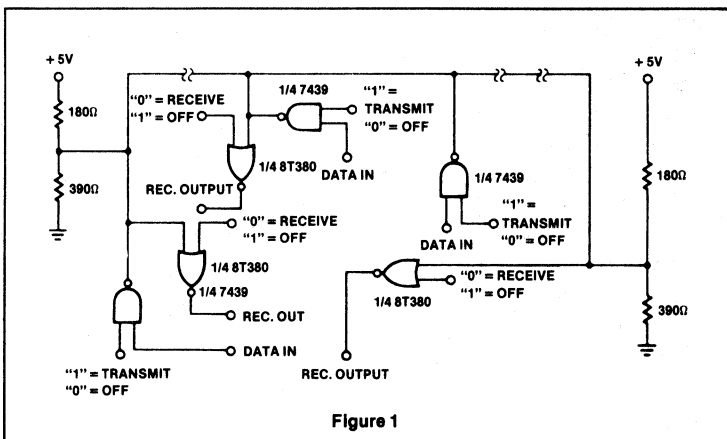


Figure 1

SCHMITT TRIGGER

The receiver transfer curve shown in Figure 2a makes the 8T380 ideal in a variety of Schmitt Trigger and waveshaping applications such as Figure 2b.

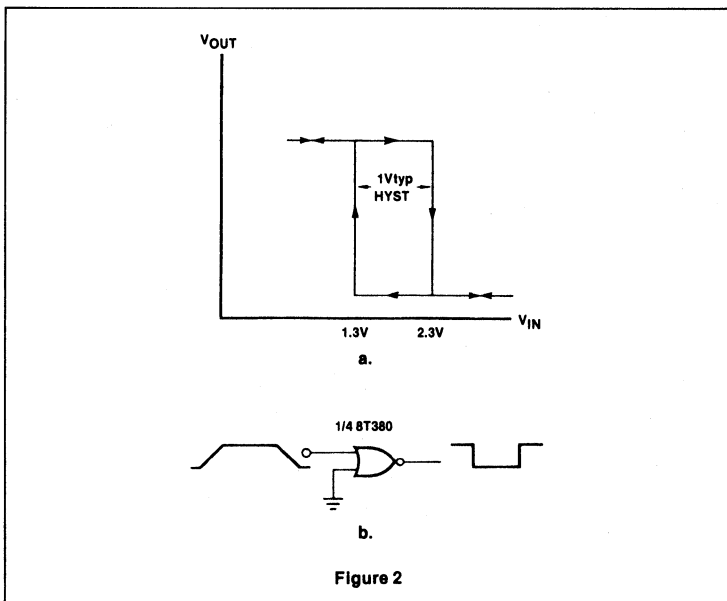


Figure 2

MOS/C-MOS INTERFACE

The input current which is only 50μA MAX in the logical "1" state and no current in the logical "0" state marks the 8T380 an ideal MOS/C-MOS interface element.

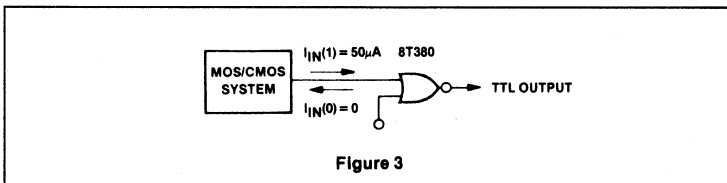


Figure 3

LATCH

8T3404

High Speed 6-Bit Latch

- Low Input load current: .25mA max., 1/6 standard TTL input load
- Minimum line reflection: low voltage diode input clamp
- Outputs sink 10mA min.
- 16-pin dual in-line package
- Simple expansion: enable Inputs
- 12ns max. data to output delay over 0°C to 75°C temperature
- Directly compatible with DTL and TTL logic circuits

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T3404	6ns (Data) 8ns (Write Enable)	47mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V _{CC} = 5V ± 5%; T _A = 0°C to + 75°C
Plastic DIP	N8T3404N

FUNCTION TABLE

MODE	INPUTS		OUTPUTS
	\bar{W}	D	\bar{Q}
Write Latches	L	L	H
	L	H	L
Latch Inputs	H	l	H
	H	h	L

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH \bar{W} transition.
 L = LOW voltage level
 l = LOW voltage level one setup time prior to the LOW-to-HIGH \bar{W} transition.

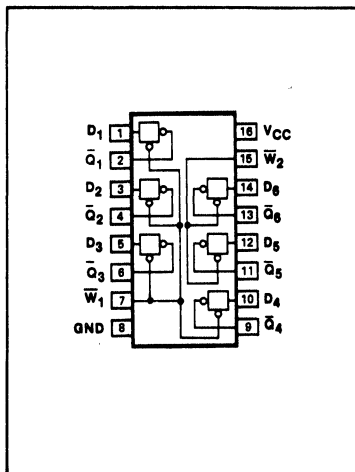
DESCRIPTION

The Signetics 8T3404 contains six high speed latches organized as independent 2-bit and 4-bit latches. They are designed for use as memory address registers, data registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low."

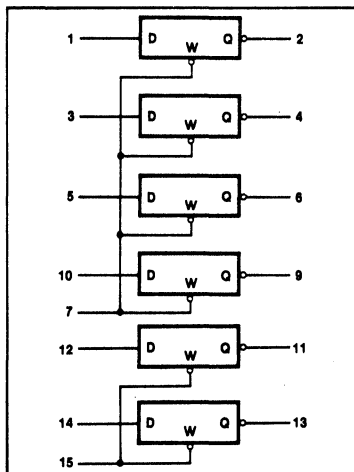
The 8T3404 is packaged in a standard 16-pin dual in-line package; and its performance is specified over the temperature range of 0°C to + 75°C, ambient. To obtain fast switching speeds resulting in

higher performance than equivalent devices made with a gold diffusion process, Schottky barrier diode clamped transistors are used.

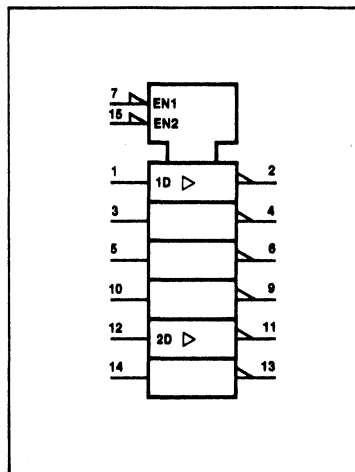
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



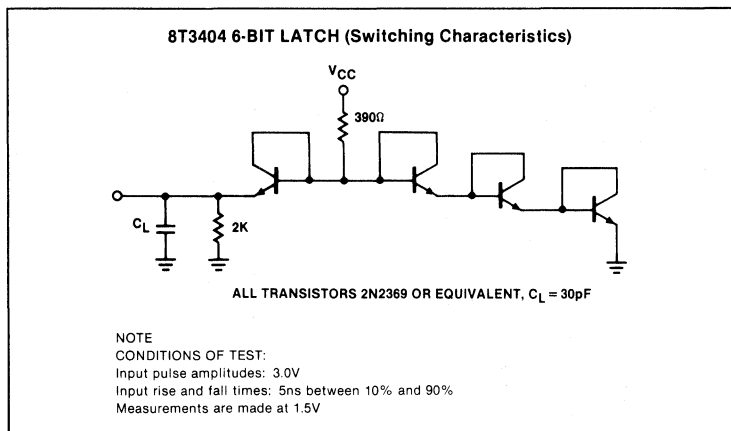
ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

PARAMETER	N8T	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	- 0.5 to +5.5	V
I _{IN} Input current	- 30mA to +100 μ A	
I _{OL} Continuous	100	mA
V _{OUT} Voltage applied to output in HIGH output state	- 0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 75	$^{\circ}$ C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	8T			UNIT
	Min	Nom	Max	
V _{CC} Supply voltage	4.75	5.0	5.25	V
V _{IH} HIGH-level output voltage	2.0			V
V _{IL} LOW-level input voltage			+ 0.8	V
I _C Input clamp current			- 5.0	mA
I _{OH} HIGH-level output current			- 1.5	mA
I _{OL} LOW-level output current			40	mA
T _A Operating free-air temperature	0		75	$^{\circ}$ C

TEST LOAD CIRCUIT



LATCH

8T3404

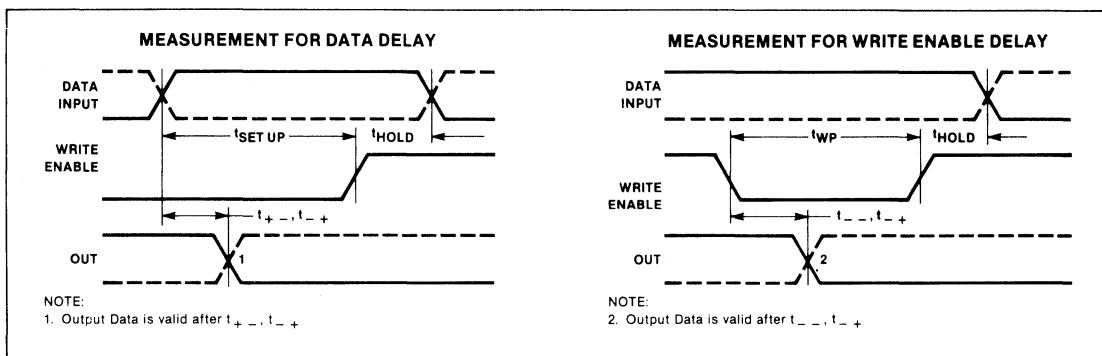
DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

PARAMETER	TEST CONDITIONS ¹	8T3404			UNIT
		Min	Typ	Max	
V _{IL} Low level input current	V _{CC} = 5.25V, V _I = 0.45V			- 0.25	mA
V _{IH} High level input current	V _{CC} = 5.25V, V _I = 5.25V			10	μA
V _{IK} Input clamp diode voltage	V _{CC} = 4.75V, I _C = - 5.0 mA			- 1.0	V
V _{OL} Output LOW voltage	V _{CC} = 4.75V, I _{OL} = 10.0 mA			0.45	V
V _{OH} Output HIGH voltage	V _{CC} = 4.75V, I _{OH} = - 1.5 mA	2.4			V
V _{IL} Input LOW voltage	V _{CC} = 5.0V			0.85	V
V _{IH} Input HIGH voltage	V _{CC} = 5.0V	2.0			V
I _{OS} Short-circuit output current ²	V _{CC} = 5.0V	- 40		- 120	mA
V _{OL} Output LOW voltage @ HIGH current	V _{CC} = 5.0V, I _{OL} = 40 mA			0.8	V
I _{CC} Supply current (total)	V _{CC} = 5.25V			75	mA
I _{IL} Low level input current at Pin 7	V _{CC} = 5.25V, V _I = 0.45V			- 1.00	mA
I _{IL} Low level input current at Pin 15	V _{CC} = 5.25V, V _I = 0.45V			- 0.50	mA
I _{IH} High level input current at Pin 7 and Pin 15	V _I = 5.25V			10	μA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 0°C to + 75 °C, V_{CC} = 5.0V ± 5%; unless otherwise specified.

PARAMETER	TEST CONDITIONS	8T			UNIT
		Min	Typ	Max	
t _{+ - t₊} Data to output delay				12	ns
t _{- - t₊} Write enable to output delay				17	ns
t _{set-up} Time data must be present before rising edge of write enable		12			ns
t _{hold} Time data must remain after rising edge of write enable		8			ns
t _{WP} Write enable pulse width		15			ns
C _{IND} Data input capacitance	3404N		f = 1MHz, V _{CC} = 0V	4	pF
	3404F		V _{BIAS} = 2.0V, T _A = 25 °C	5	pF
C _{INW} Write enable capacitance	3404N		f = 1MHz, V _{CC} = 0V	7	pF
	3404F		V _{BIAS} = 2.0V, T _A = 25 °C	8	pF

LATCHES/FLIP-FLOPS

8TS805, 806

8TS805 Octal Transparent Latch With 3-State Outputs
8TS806 Octal D Flip-Flop With 3-State Outputs

- 8-bit transparent latch — 8TS805
- 8-bit positive, edge-triggered register — 8TS806
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8TS805	10ns	105mA
8TS806	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N8TS805N • N8TS806N	
Ceramic DIP		S8TS805F • S8TS806F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
An 8TS unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$.

DESCRIPTION

The 8TS805 is an octal, transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D Inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The

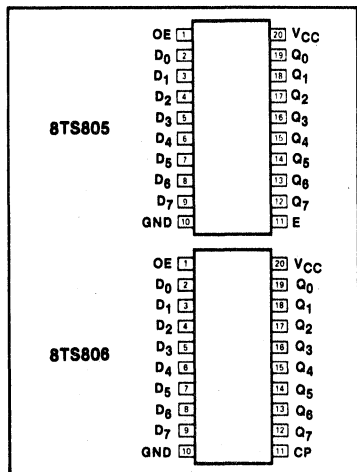
active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the latch operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

The 8TS806 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are

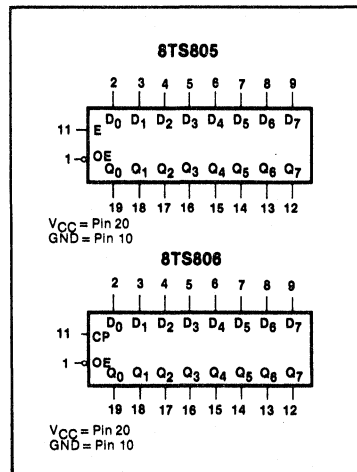
controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

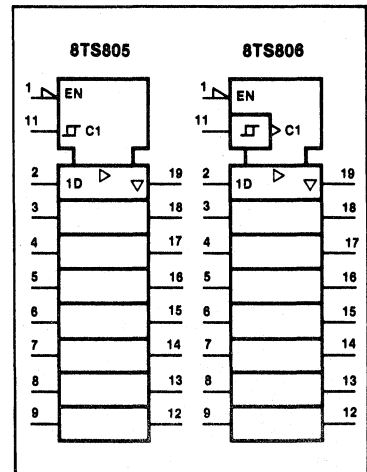
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LATCHES/FLIP-FLOPS

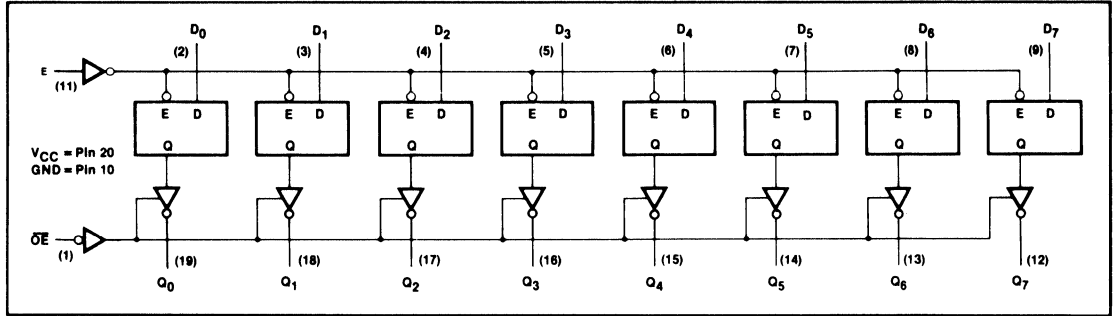
8TS805, 806

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls

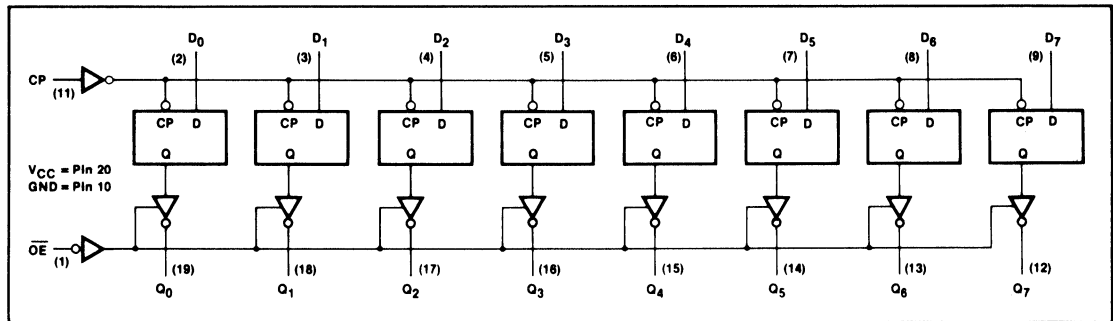
all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW, the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in

the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 8TS805



LOGIC DIAGRAM, 8TS806



5

MODE SELECT—FUNCTION TABLE, 8TS805

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	E	D_n		Q_0-Q_7
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

MODE SELECT—FUNCTION TABLE, 8TS806

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		Q_0-Q_7
Load and read register	L	l	l	L	L
	L	l	h	H	H
Load register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition
 L = LOW voltage level

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition
 (Z) = HIGH impedance "off" state
 l = LOW-to-HIGH clock transition
 X = Don't care

LATCHES/FLIP-FLOPS

8TS805, 806

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I_{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state.	- 0.5 to + V_{CC}	- 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8TS			UNIT	
		Min	Nom	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage	Mil		+ 0.8	V	
		Com'l		+ 0.8	V	
I_{IK}	Input clamp current			- 18	mA	
I_{OH}	HIGH-level output current	Mil		- 2.0	mA	
		Com'l		- 6.5	mA	
I_{OL}	LOW-level output current	Mil		20	mA	
		Com'l		20	mA	
T_A	Operating free-air temperature	Mil	- 55	+ 125	°C	
		Com'l	0	70	°C	

NOTE

 $V_{IL} = + 0.7V$ MAX for S8TS at $T_A = + 125^{\circ}C$ only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		8TS805, 806			UNIT	
			Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		Mil	2.4	3.0	V	
			Com'l	2.4	3.1	V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX		I _{OL} = MAX	Mil		0.5 ⁴	V
				Com'l		0.5	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.2	V	
I _{OZH} Off-state output current, HIGH-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 2.4V				50	μA	
I _{OZL} Off-state output current, LOW-level voltage applied	V _{CC} = MAX, V _{IH} = MIN, V _O = 0.5V				-50	μA	
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5V				1.0	mA	
I _{IH} HIGH-level input current	V _{CC} = MAX, V _I = 2.7V				50	μA	
I _{IL} LOW-level input current	V _{CC} = MAX, V _I = 0.5V				-0.25	mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-40		-100	mA	
I _{CC} Supply current (total)	V _{CC} = MAX	I _{CCL}	8TS805		105	160	mA
		I _{CCL}	All inputs grounded, 8TS806		102	140	mA
		I _{CCZ}	CP, OE = 4.5V D inputs = GND		131	180	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = +0.45V MAX for 8TS at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

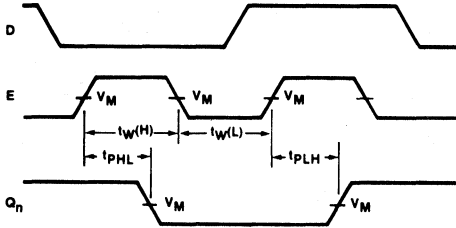
PARAMETER	TEST CONDITIONS	8TS		UNIT
		C _L = 15pF, R _L = 280Ω		
		Min	Max	
f _{MAX} Maximum clock frequency	Waveform 6, 8TS806	75		MHz
t _{PLH} Propagation delay t _{PHL} Latch Enable to output	Waveform 1, 8TS805		14 18	ns
t _{PLH} Propagation delay t _{PHL} Data to output	Waveform 4, 8TS805		9 13	ns
t _{PLH} Propagation delay t _{PHL} Clock to output	Waveform 6, 8TS806		15 17	ns
t _{PZH} Enable time to HIGH level	Waveform 2		15	ns
t _{PZL} Enable time to LOW level	Waveform 3 8TS805 8TS806		18 18	ns
t _{PHZ} Disable time from HIGH level	Waveform 2, C _L = 5pF		9	ns
t _{PLZ} Disable time from LOW level	Waveform 3, C _L = 5pF		12	ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

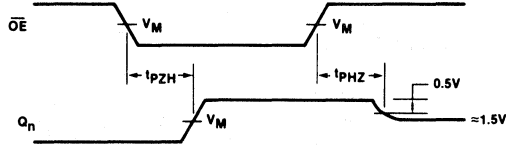
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



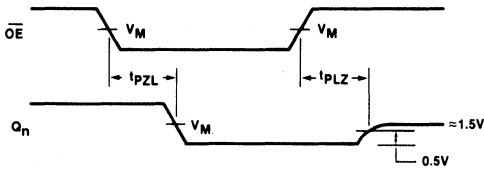
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



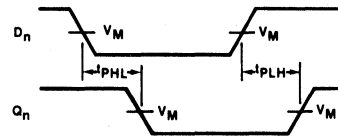
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



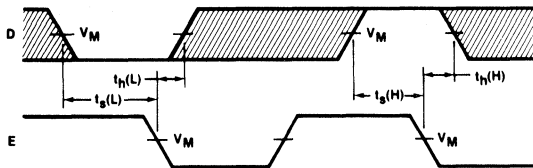
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



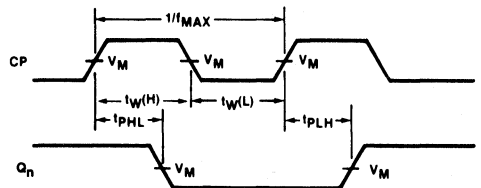
Waveform 4

DATA SETUP AND HOLD TIMES



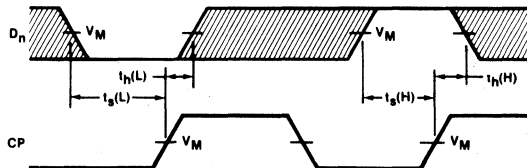
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8TS		UNIT
		Min	Max	
$t_{w(H)}$ $t_{w(L)}$ Latch Enable pulse width	Waveform 1, 8TS805	6 7.3		ns
t_s Setup time, Data to Latch Enable	Waveform 5, 8TS805	5		ns
t_h Hold time, Data to Latch Enable	Waveform 5, 8TS805	10		ns
$t_{w(H)}$ $t_{w(L)}$ Clock pulse width	Waveform 6, 8TS806	6 7.3		ns
t_s Setup time, Data to Clock	Waveform 7, 8TS806	5		ns
t_h Hold time, Data to Clock	Waveform 7, 8TS806	4		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
 D = Diodes are 1N916, 1N3064, or equivalent.
 $R_X = 1k\Omega$ for 54/74, 54S/74S, $R_X = 5k\Omega$ for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

5

LATCHES/FLIP-FLOPS

8TS807, S808

'807 Octal Transparent Latch With 3-State Outputs
'808 Octal D Flip-Flop With 3-State Outputs

- 8-bit transparent latch — 8TS807
- 8-bit positive, edge-triggered register — 8TS808
- 3-State inverting output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8TS807	10ns	105mA
8TS808	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES	MILITARY RANGES
	$V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$	$V_{CC} = 5V \pm 10\%$; $T_A = -55^\circ C$ to $+125^\circ C$
Plastic DIP	N8TS807N • N8TS808N	
Ceramic DIP		S8TS807F • S8TS808F

DESCRIPTION

The 8TS807 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable (\overline{OE}) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable (\overline{OE}) controls

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
 An 8TS unit load (Sul) is 50 μ A I_{IH} and -2.0mA I_{IL} .

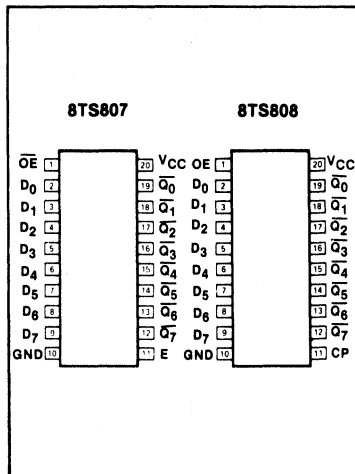
all eight 3-State buffers independent of the latch operation. When \overline{OE} is LOW, the latched or transparent data appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

The 8TS808 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable (\overline{OE}) control gates.

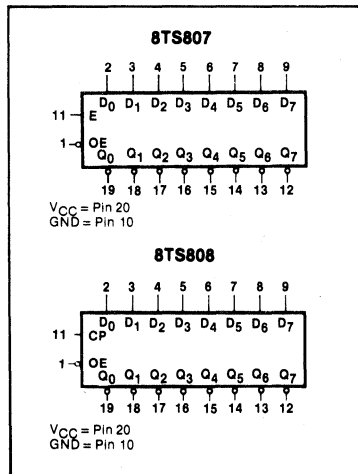
The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The

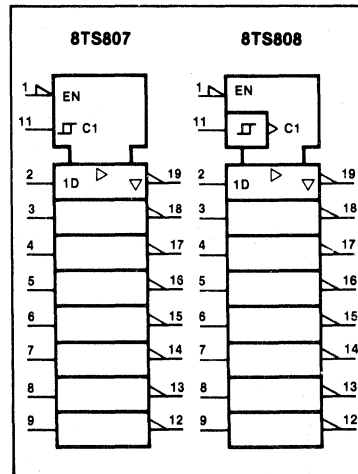
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LATCHES/FLIP-FLOPS

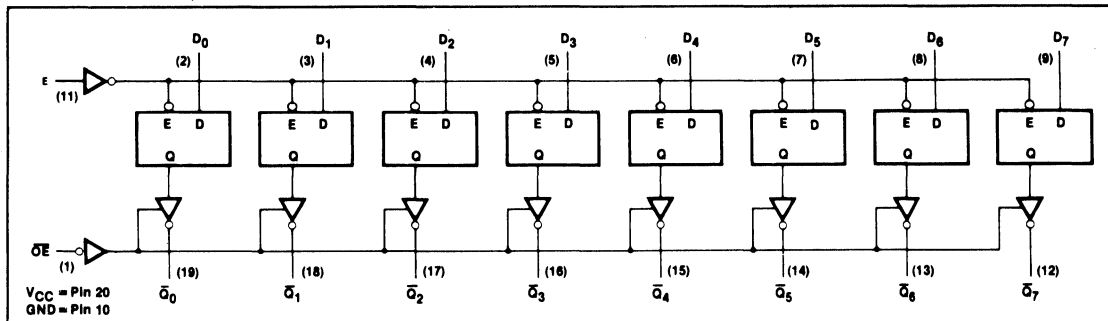
8TS807, S808

active LOW Output Enable (\overline{OE}) controls all eight 3-State buffers independent of the register operation. When \overline{OE} is LOW,

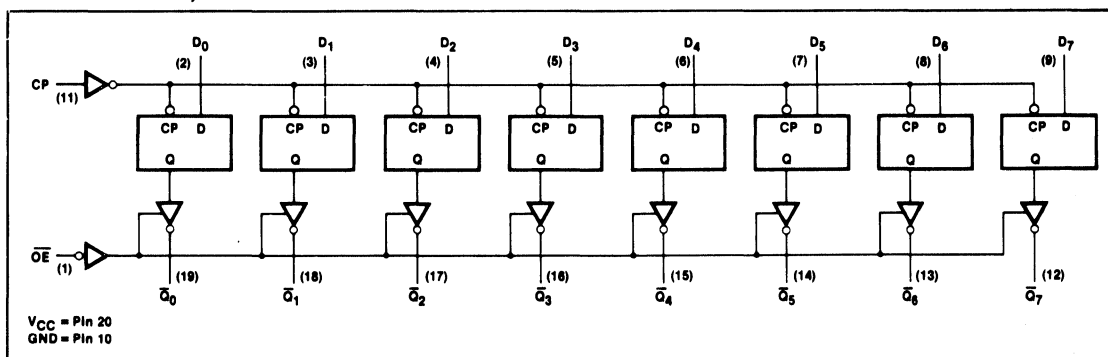
the data in the register appears at the outputs. When \overline{OE} is HIGH, the outputs are in the HIGH impedance "off" state, which

means they will neither drive nor load the bus.

LOGIC DIAGRAM, 8TS807



LOGIC DIAGRAM, 8TS808



5

MODE SELECT—FUNCTION TABLE, 8TS807

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	E	D_n		Q_0-Q_7
Enable and read register	L	H	L	L	H
	L	H	H	H	L
Latch and read register	L	L	l	L	H
	L	L	h	H	L
Disable outputs	H	X	X	X	(Z)

MODE SELECT—FUNCTION TABLE, 8TS808

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	\overline{OE}	CP	D_n		Q_0-Q_7
Load and read register	L	l	l	L	H
	L	l	h	H	L
Load register and disable outputs	H	X	X	X	(Z)
	H	X	X	X	(Z)

H = HIGH voltage level
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 L = LOW voltage level

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 (Z) = HIGH impedance "off" state
 l = LOW-to-HIGH clock transition
 X = Don't care

LATCHES/FLIP-FLOPS

8TS807, S808

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V _{CC}	Supply voltage	7.0	7.0	V
V _{IN}	Input voltage	- 0.5 to + 5.5	- 0.5 to + 5.5	V
I _{IN}	Input current	- 30 to + 5	- 30 to + 5	mA
V _{OUT}	Voltage applied to output in HIGH output state	- 0.5 to + V _{CC}	- 0.5 to + V _{CC}	V
T _A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8TS			UNIT	
		Min	Nom	Max		
V _{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage		2.0			V
V _{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I _{IK}	Input clamp current				- 18	mA
I _{OH}	HIGH-level output current	Mil			- 2.0	mA
		Com'l			- 6.5	mA
I _{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T _A	Operating free-air temperature	Mil	- 55		+ 125	°C
		Com'l	0		70	°C

NOTE

V_{IL} = + 0.7V MAX for S8TS at T_A = + 125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	8TS807, 808			UNIT	
		Min	Typ ²	Max		
V _{OH}	HIGH-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	Mil	2.4	3.0	V	
		Com'l	2.4	3.1	V	
V _{OL}	LOW-level output voltage V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OL} = MAX	Mil		0.5 ⁴	V	
		Com'l		0.5	V	
V _{IK}	Input clamp voltage V _{CC} = MIN, I _I = I _{IK}			- 1.2	V	
I _{OZH}	Off-state output current, HIGH-level voltage applied V _{CC} = MAX, V _{IH} = MIN, V _O = 2.4V			50	μA	
I _{OZL}	Off-state output current, LOW-level voltage applied V _{CC} = MAX, V _{IH} = MIN, V _O = 0.5V			- 50	μA	
I _I	Input current at maximum input voltage V _{CC} = MAX, V _I = 5.5V			1.0	mA	
I _{IH}	HIGH-level input current V _{CC} = MAX, V _I = 2.7V			50	μA	
I _{IL}	LOW-level input current V _{CC} = MAX, V _I = 0.5V			- 0.25	mA	
I _{OS}	Short-circuit output current ³ V _{CC} = MAX		- 40	- 100	mA	
I _{CC}	Supply current (total) V _{CC} = MAX	I _{CCL}	8TS807	105	160	mA
		I _{CCL}	All inputs grounded, 8TS808	102	140	mA
		I _{CCZ}	CP, OE = 4.5V D inputs = GND	131	180	mA

NOTES

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- V_{OL} = + 0.45V MAX for S8TS at T_A = + 125°C only.

LATCHES/FLIP-FLOPS

8TS807, S808

AC CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8TS		UNIT
		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	
f_{MAX} Maximum clock frequency	Waveform 6, 8TS808	75		MHz
t_{PLH} Propagation delay t_{PHL} Latch Enable to output	Waveform 1, 8TS807		14 18	ns
t_{PLH} Propagation delay t_{PHL} Data to output	Waveform 4, 8TS807		9 13	ns
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 6, 8TS808		15 17	ns
t_{PZH} Enable time to HIGH level	Waveform 2		15	ns
t_{PZL} Enable time to LOW level	Waveform 3 8TS807 8TS808		18 18	ns
t_{PHZ} Disable time from HIGH level	Waveform 2, $C_L = 5\text{pF}$		9	ns
t_{PLZ} Disable time from LOW level	Waveform 3, $C_L = 5\text{pF}$		12	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	8TS		UNIT
		Min	Max	
$t_{W(H)}$ Latch Enable pulse width $t_{W(L)}$	Waveform 1, 8TS807	6 7.3		ns
t_s Setup time, Data to Latch Enable	Waveform 5, 8TS807	5		ns
t_h Hold time, Data to Latch Enable	Waveform 5, 8TS807	10		ns
$t_{W(H)}$ Clock pulse width $t_{W(L)}$	Waveform 6, 8TS808	6 7.3		ns
t_s Setup time, Data to Clock	Waveform 7, 8TS808	5		ns
t_h Hold time, Data to Clock	Waveform 7, 8TS808	4		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
 R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
 $R_X = 1k\Omega$ for 54/74, 54S/74S, $R_X = 5k\Omega$ for 54LS/74LS.
 t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

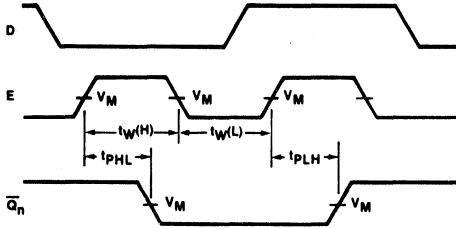
$V_M = 1.3\text{V}$ for 54LS/74LS; $V_M = 1.5\text{V}$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8TS	3.0V	1MHz	500ns	2.5ns	2.5ns

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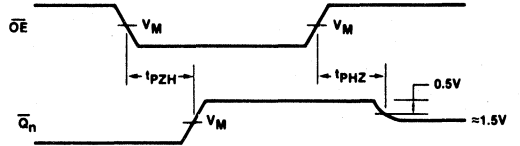
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



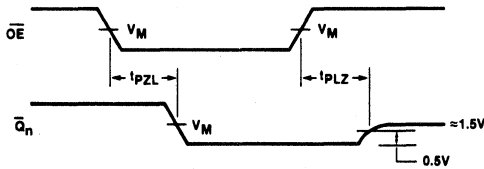
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



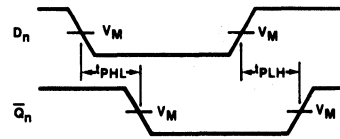
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



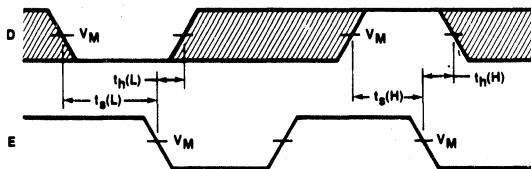
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



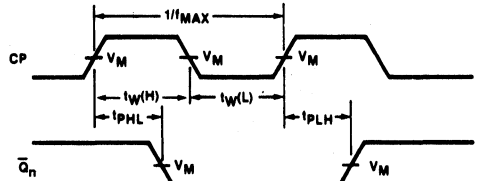
Waveform 4

DATA SETUP AND HOLD TIMES



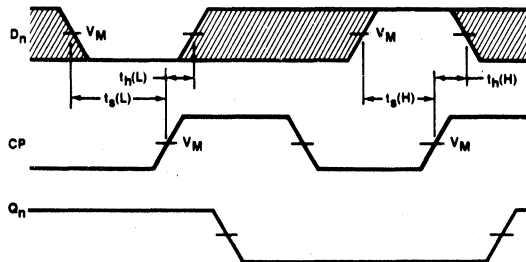
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Section 6
54F/74F Fast TTL

PRODUCT DESCRIPTION

Signetics has combined advanced oxide-isolated fabrication techniques with standard TTL functions to create a new family designed for the 80's. The high operating speeds of FAST can push system operating speeds into areas previously reserved for 10K ECL, but with simple TTL design rules and single 5V power supplies. Low input loading allows the user to mix LS, ALS, and HCMOS in the same system without the need for translators and restrictive fanout requirements.

FAST circuits are pin-for-pin replacements for 74S types, but offer power dissipation 3-4 times lower and higher operating speeds. Existing systems can achieve much lower power by replacing the 74S types with the corresponding FAST devices, with no changes other than reducing the size of the power supply.

The input structure provides better noise immunity because of higher thresholds, while the oxide-isolation and new circuit techniques create devices that have less variation with temperature or supply voltage than existing TTL logic families. Signetics guarantees all ac parameters under realistic system conditions—across the supply voltage spread and the temperature range, and with heavy 50pF output loads.

The use of high-capacitance PNP inputs has been avoided, and clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unused inputs to be tied directly to V_{CC} without pullup resistors.

Multiple sources and a complete family of powerful circuits combine to make Signetics FAST the logic choice of the 80's!

FEATURES

- 3ns propagation delays
- 4mW/gate power dissipation
- Guaranteed AC performance over temperature and supply voltage spreads
- Improved input and output structures
- Standard TTL functions and pinouts
- Replacement for "S" types . . . 1/4 the power
- Designer's choice for new system designs

For full specifications of the FAST TTL circuits see our Data Manual "FAST TTL"

THE SPEED/POWER SPECTRUM

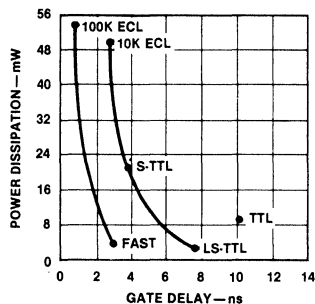


Figure 1

BASIC FAST GATE

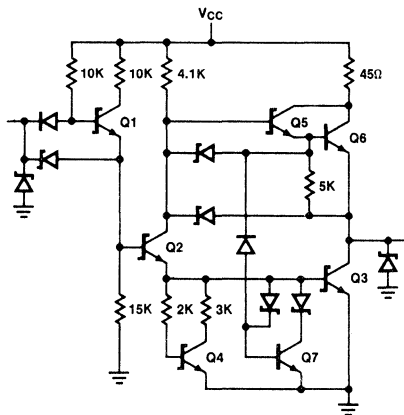


Figure 2

TRANSFER FUNCTIONS AT ROOM TEMPERATURE

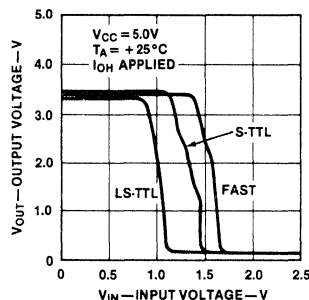


Figure 3

THE HIGH-SPEED LOGIC OF THE 80'S

ABSOLUTE MAXIMUM RATINGS (Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
V_{IN}	input voltage	- 0.5 to + 7.0	- 0.5 to + 7.0	V
I_{IN}^2	Input current	- 30 to + 5	- 30 to + 5	mA
V_{OUT}^1	Voltage applied to output in HIGH output state	- 0.5 to V_{CC}	- 0.5 to V_{CC}	V
I_{OUT}^3	Current applied to output in LOW output state	40	40	mA
T_A	Operating free-air temperature range	- 55 to + 125	0 to 70	°C

NOTES

1. For 3-state outputs, $V_{OUT} = -0.5V$ to $5.5V$ with $V_{CC} = 0V$.
2. For NPN input parts, input current above 1 mA is clamped.
3. I_{OUT} is specified at twice the rated I_{OL} for buffer line driver functions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		54/74F			UNIT	
		Min	Typ	Max		
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V	
V_{IL}	LOW-level input voltage			0.8	V	
I_{IK}	Input clamp current			- 18	mA	
I_{OH}	HIGH-level output current			- 1	mA	
I_{OL}	LOW-level output current			20	mA	
T_A	Operating free-air temperature	Mil	- 55		125	°C
		Com'l	0		70	°C

*Trademark of Fairchild Camera and Instrument Corporation.

THE HIGH-SPEED LOGIC OF THE 80's

54F/74F FAMILY CHARACTERISTICS¹

SYMBOL	PARAMETER	LIMITS ²			UNITS	V _{CC} ⁴	CONDITIONS ²	
		Min	Typ ³	Max				
V _{IH}	Input HIGH voltage	2.0			V		Recognized as a HIGH signal over recommended V _{CC} and T _A range	
V _{IL}	Input LOW voltage			0.8	V		Recognized as a LOW signal over recommended V _{CC} and T _A range	
V _{IK}	Input clamp diode voltage			-1.2	V	Min	I _{IN} = -18 mA	
V _{OH}	Output HIGH voltage	Std ⁵ Mil	2.5	3.4		V	Min	I _{OH} = 20 μA multiplied by output HIGH U.L. shown on data sheet
		Std ⁵ Com'l	2.7	3.4				
V _{OL}	Output LOW voltage		0.35	0.5	V	Min	I _{OL} = -0.6 mA multiplied by output LOW U.L. shown on data sheet	
I _{IH}	Input HIGH current	1.0 U.L.		1	20	μA	Max	I _{IH} = 20 μA multiplied by input HIGH U.L. shown on data sheet; V _{IH} = 2.7V
		2.0 U.L.		2	40			
		n U.L.			n(40)			
I _I	Input HIGH current, breakdown test, all inputs			5	100	μA	Max	V _{IN} = 7.0V
	NPN inputs: ⁶ Input clamp current			500	1000			
I _{IL}	Input LOW current	1.0 U.L.		-0.4	-0.6	mA	Max	I _{IL} = -0.6 mA multiplied by input LOW U.L. shown on data sheet; V _{IN} = 0.5V
		2.0 U.L.		-0.8	-12			
		n U.L.			n(-0.6)			
		0.033 U.L.			-0.02			
I _{OZH}	3-state output OFF current HIGH		2	50	μA	Max	V _{OUT} = 2.4V	
I _{OZL}	3-state output OFF current LOW		2	-50	μA	Max	V _{OUT} = 0.5V	
I _{OS} ⁷	Output short-circuit current	Standard ⁵ / 3-State	-60	-80	-150	μA	Max	V _{OUT} = 0V
		Buffers/Line Drivers	-100	-150	-225			

NOTES

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0V.
4. Min and Max refer to the values listed in the table of recommended operating conditions.
5. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.
6. Used as an input clamp current test at maximum input voltage for parts with an NPN input structure. This is not a leakage test.
7. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

PROPAGATION DELAY VS LOAD CAPACITANCE 'F00

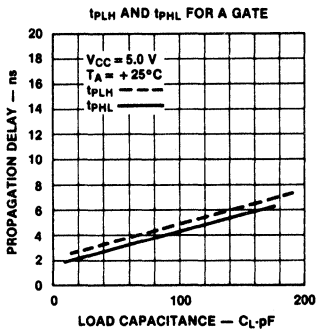


Figure 4

OUTPUT LOW CHARACTERISTICS 'F00

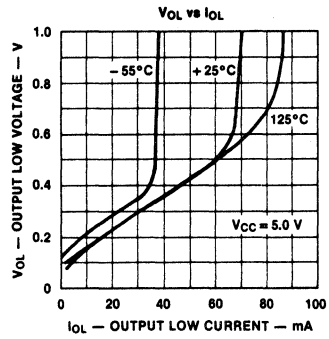


Figure 5

FALL TIME VS LOAD CAPACITANCE 'F00

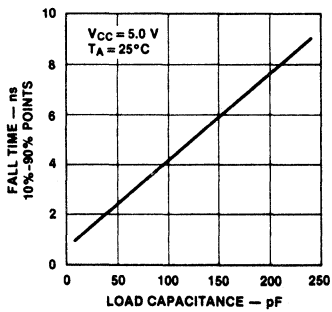


Figure 6

OUTPUT HIGH CHARACTERISTICS 'F00

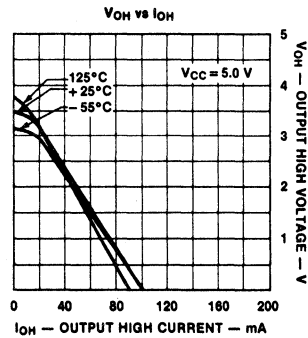


Figure 7

Section 7 Surface Mounted Devices

SMD PACKAGE INFORMATION

INTRODUCTION

A Surface-Mounted Device (SMD) is an electronic device which, due to advances in packaging technology, is mounted on the surface of a circuit board instead of being inserted through plated-through holes drilled in the surface. SMDs are soldered directly to bonding pads on the board. In some cases, e.g., leadless chip carriers, they must be socketed.

Throughout the years there have been rapid advances in IC design and manufacturing resulting in faster, more dense, and more reliable die. IC packaging and PC board assembly technology has finally caught up, offering much smaller packages which reduce signal paths, resulting in lower capacitance and impedance.

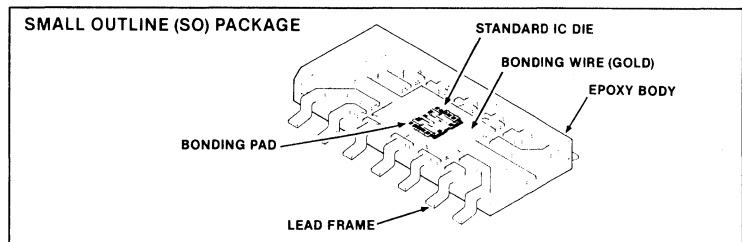
Surface-mounted PC boards are more dense and more reliable than their predecessors. Further, the automated assembly processes reduce process time, improve yields, and reduce board rework. These benefits add up to a better product at a lower price.

COMPARISON OF BASIC SMD PACKAGES

NAME	MATERIAL	SHAPE	LOCATION OF LEADS	LEAD* SPACING	LEAD CONFIGURATION	JEDEC REGISTRATION	SIGNETICS AVAILABILITY
Small Outline (SO)	Plastic	Rectangle	2 Sides	0.050 in.	Down and Out	Yes	Yes
Plastic Leaded Chip Carrier (PLCC)	Plastic	Square	4 Sides	0.050 in.	Down and Under/ J-Hook	Yes	Yes
Flatpack	Ceramic	Rectangle	2 Sides	0.050 in.	Straight out	Yes	Yes
Leadless Chip Carrier (Type C)	Ceramic	Square	4 Sides	0.050 in.	None	Yes	Yes

SO — THE WORLD'S SMALLEST PLASTIC DIP

As you can see below, there is very little difference between the assembly SO and a DIP. The major difference is that the SO is much smaller and has a different lead bend. Both DIPs and SO packages use the same materials and assembly technology.



THERMAL CHARACTERISTICS

Junction Temperature (T_J)

Actual junction temperature can be calculated using the following:

$$T_J = (P_D \times R_{\theta JA}) + T_A$$

where:

- T_J = Actual Junction Temperature
- P_D = Power Dissipation (V_{CC} Max) × (I_{CC} Max)
- R_{θJA} = Thermal Resistance Junction to Ambient

Example:

A device is operated at +55°C with a power dissipation of 145 mW and a R_{θJA} of 100 °C/W.

$$T_J = (0.145 \times 100) + 55$$

$$T_J = (15) + 55$$

$$T_J = 70^\circ\text{C}$$

Power Dissipation (P_D)

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_D(T_A) = \frac{T_J(\text{Max}) - T_A}{R_{\theta JA}(\text{Typ})}$$

where:

- P_D(T_A) = Power dissipation allowable at a given operating ambient temperature. This must be **greater** than the sum of the products of the supply voltages and supply currents at the worst case operating condition.
- T_J(Max) = Maximum operating junction temperature.
- T_A = Maximum desired operating ambient temperature.
- R_{θJA} = Typical thermal resistance junction to ambient.

Example:

The maximum allowable power dissipation for a 14-pin device mounted on a ceramic substrate with maximum junction temperature T_J = 150°C and maximum temperature T_A = 70°C.

$$P_D(70^\circ) = \frac{150^\circ - 70^\circ}{130^\circ/\text{W}}$$

$$P_D(70^\circ) = \frac{80}{130} = 615 \text{ mW}$$

SMD PACKAGE INFORMATION

RELIABILITY

This section summarizes the activities undertaken by Reliability Engineering to evaluate and qualify the SO package. The evaluation demonstrated that the stress performance of the SO package is equivalent to the larger standard molded epoxy dual-in-line package in all aspects, and mounted, the package thermal resistance characteristics are exceptional considering the reduced size and mass of the package.

Evaluation Program

The evaluation/qualification program conducted in 1979 included three Analog products: LM311 Voltage Comparator, μ A747 Dual Op Amp, and NE532 Dual Op Amp.

These devices encompass three wafer fabrication processes and both 8-pin and 14-pin package configurations.

All products were assembled on Alloy 42 lead frames, die attached utilizing conventional gold-silicon eutectic and molded in our standard Morton 410B epoxy Novalac compound. The devices were subjected to a series of accelerated stresses and tested to conventional data sheet parameters. Variables data were taken and drift analysis was performed.

The stress conditions employed were as follows:

- High Temperature Bias Life
 $T_A = 125^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$
- High Temperature Storage Life
 $T_A = 150^\circ\text{C}$
- Temperature/Humidity Bias Life
 $T_A = 85^\circ\text{C}$, $\text{RH} = 85\%$, $V_{CC} = \pm 15\text{V}$
- Temperature/Humidity/Pressure (Pressure Cooker) $T_A = 121^\circ\text{C}$, 15 PSIG 100%, Sat. Steam

- Thermal Shock (Liquid-to-Liquid)
- 65°C to 150°C

Program Results

The small dimensions of the SO package raised questions on its reliability, particularly in high humidity environments. The test results, however, compare favorably to the standard dual-in-line product. Our corporate requirements for product qualification were met or exceeded. The detailed results are presented in the Reliability Evaluation Results table.

SO packaging materials are being improved. As qualification evaluations are completed, results will be made available through the SURE III program.

RELIABILITY EVALUATION RESULTS

RELIABILITY ENGINEERING PROJECT ID	SIGNETICS PRODUCT TYPE	STRESS	STRESS CONDITIONS	STRESS DURATION	CUMULATIVE RESULT	ANALYSIS
79070	LM311 (14-Lead "SO")	HTOL	125°C	2,000 hrs	1/49	1 @ 168 hrs: ball bond to trace short
		HTSL	150°C	2,000 hrs	0/50	
		Bias/temperature/humidity	85°C @ 85% RH $V_{CC} = 5.5\text{V}$	2,000 hrs	2/50	2 @ 2,000 hrs: internal metal corrosion
		Pressure pot	121°C 14 PSIG	432 hrs	2/51	1 @ 192 hrs: output leakage = 68 nA 1 @ 432 hrs: output leakage = 100 nA Both internal metal corrosion
		Thermal shock	-65°C to $+150^\circ\text{C}$	1,000 ~	0/45	
790708	μ A747 (14-Lead "SO")	HTOL	125°C to $\pm 15\text{V}$	2,000 hrs	2/50	1 @ 168 hrs: $V_{OS} = 10\text{ mV}$, $V_{OS} = 7.4\text{ mV}$ @ 2K hrs 1 @ 1,500 hrs: $V_{OS} = -80\text{ mV}$, $I_B = 8\text{ }\mu\text{A}$ Suspect static damage
		HTSL	150°C	2,000 hrs	0/50	
		Bias/temperature/humidity	85°C @ 85% RH $V_{CC} = 5.5\text{V}$	2,000 hrs	1/50	V_{OS} rejects @ 500 hrs (-80 mV) Suspect static damage
		Pressure pot	121°C 15 PSIG	312 hrs	3/50	3 V_{OS} rejects @ 312 hrs ($\sim 8\text{ mV}$)
		Thermal shock	-65°C to $+150^\circ\text{C}$	1,000 ~	1/48	V_{OS} rejects @ 700 ~ (-170 mV , $I_B = 14\text{ }\mu\text{A}$) Suspect static damage
795003	NE532 (8-Lead "SO")	HTOL	150°C	2,000 hrs	0/45	To 500 hrs, 0/18 from 500 to 2,000 hrs (due to capacity limitations)
		HTSL	150°C	2,000 hrs	0/46	
		Bias/temperature/humidity	85°C @ 85% RH	2,000 hrs	2/49	1 @ 1,500, 1 @ 2,000 hrs Both output sink current failures due to corrosion
		Pressure pot	121°C 15 PSIG	456 hrs	1/43	Output sink current @ 288 hrs
		Thermal shock	-65°C to $+150^\circ\text{C}$	1,000 ~	1/45	V_{OS} rejects @ 200 ~ (15 mV)

SMD PACKAGE INFORMATION

SO PACKAGE THERMAL DATA

PACKAGE TYPE	PACKAGE MOUNTING TECHNIQUE*	MAX. ALLOWABLE POWER DISSIPATION (mW) AT 25°C	MAX. ALLOWABLE POWER DISSIPATION (mW) AT 70°C	THERMAL RESISTANCE (θ_{JA} °C/Watt)	
				Average	Maximum
SO-14	PCB	658	421	190	225
	Ceramic	962	615	130	165
	Ceramic w/H.S.	1471	941	85	110
SO-16	PCB	862	551	145	170
	Ceramic	1250	800	100	125
	Ceramic w/H.S.	1923	1231	65	85
SO-16L	PCB	1250	800	100	140
	Ceramic	1743	1143	70	100
	Ceramic w/H.S.	2500	1600	50	65
SO-20	PCB	1471	941	85	115
	Ceramic	2273	1454	55	85
	Ceramic w/H.S.	3572	2286	35	55
SO-24	PCB	1563	1000	80	110
	Ceramic	2000	1600	50	80
	Ceramic w/H.S.	4167	2667	30	50

NOTES

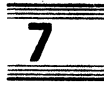
1. PCB = Printed circuit board
 2. Ceramic = Alumina substrate
 3. Ceramic w/H.S. = Alumina substrate with heat sink and/or thermal compound
- *Air gap between package and surface is 0.006-inch unless thermal compound is used.

PACKAGE AVAILABILITY

COMMERCIAL PACKAGES				MILITARY (CERAMIC) PACKAGES	
Pin Count	SO 0.150 Wide	SOL 0.300 Wide	PLCC	Leadless Chip Carrier	Flatpack
8	Available	—	—	—	—
14	Available	—	—	—	Available
16	Available	Available	—	—	Available
20	—	Available	—	Available	—
24	—	Available	—	Available	Available
28	—	Available	—	Available	—
44	—	—	1984	Available	—
52	—	—	—	Available	Available
68	—	—	—	Available	Available
84	—	—	—	—	—

TECHNOLOGIES AVAILABLE IN SIGNETICS SURFACE-MOUNTED PACKAGES

PACKAGE TYPE	PRODUCT TYPES	AVAILABILITY
SO-14	CMOS-4000, TTL-S, TTL-LS, TTL-Std.	Now
SO-14	High-Speed CMOS, TTL-Fast	1984
SO-16	CMOS-4000, TTL-S, TTL-LS, TTL-Std.	Now
SO-16	High-Speed CMOS, TTL-Fast	1984
SO-16L	TTL-S, TTL-LS, TTL-Std.	Now
SO-16L	TTL-Fast	1984
SO-20	TTL-S, TTL-LS	Now
SO-20	TTL-Fast, High-Speed CMOS	1984
SO-24	TTL-Fast, High-Speed CMOS	1984
SO-28	TTL-Fast	1984



SMD PACKAGE INFORMATION

PACKAGE OUTLINE/JEDEC REGISTRATION

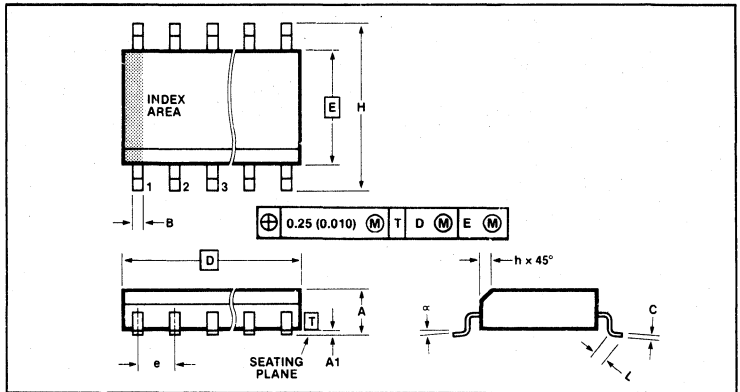
The following SO package outlines have been registered with the JC11.3 committee of the Joint Electronic Devices Engineering Council of the Electronics Industry Association:

- SO-8 SO-20
- SO-14 SO-24
- SO-16 SO-28
- SO-16L

Outlines and dimensions for each package are shown below:

- A. Dimensions and tolerancing per ANSI Y14.5-1973.
- B. "T" is a reference datum.
- C. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006 in.).
- D. The chamfer on the body is used to designate pin 1. The beveled side to the left denotes lead number 1.

- E. "L" is the length of terminal for soldering to a substrate.
- F. Controlling dimension: Millimeter.



MILLIMETERS

Symbol	SO						SOL								Notes
	8-PIN		14-PIN		16-PIN		16L-PIN		20-PIN		24-PIN		28-PIN		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
A	1.35	1.75	1.35	1.75	1.35	1.75	2.35	2.65	2.35	2.65	2.35	2.65	2.35	2.65	
A ₁	0.10	0.25	0.10	0.25	0.10	0.25	0.10	0.30	0.10	0.30	0.10	0.30	0.10	0.30	
B	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49	0.35	0.49	
C	0.19	0.25	0.19	0.25	0.19	0.25	0.23	0.32	0.23	0.32	0.23	0.32	0.23	0.32	
D	4.80	5.00	8.55	8.75	9.80	10.00	10.1	10.5	12.6	13.0	15.2	15.6	17.7	18.1	C
E	3.80	4.00	3.80	4.00	3.80	4.00	7.4	7.6	7.4	7.6	7.4	7.6	7.4	7.6	C
e	1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC		1.27 BSC		
H	5.80	6.20	5.80	6.20	5.80	6.20	10.00	10.65	10.00	10.65	10.00	10.65	10.00	10.65	
L	0.40	1.27	0.40	1.27	0.40	1.27	0.40	1.27	0.40	1.27	0.40	1.27	0.40	1.27	E
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	
h	0.25	0.50	0.25	0.50	0.25	0.50	0.25	0.75	0.25	0.75	0.25	0.75	0.25	0.75	D

INCHES

Symbol	SO						SOL								Notes
	8-PIN		14-PIN		16-PIN		16L-PIN		20-PIN		24-PIN		28-PIN		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
A	0.053	0.069	0.053	0.069	0.053	0.069	0.093	0.104	0.093	0.104	0.093	0.104	0.093	0.104	
A ₁	0.004	0.010	0.004	0.010	0.004	0.010	0.004	0.012	0.004	0.012	0.004	0.012	0.004	0.012	
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	
C	0.007	0.010	0.007	0.010	0.007	0.010	0.009	0.013	0.009	0.013	0.009	0.013	0.009	0.013	
D	0.189	0.197	0.337	0.344	0.386	0.394	0.398	0.413	0.496	0.512	0.598	0.614	0.647	0.713	C
E	0.150	0.157	0.150	0.157	0.150	0.157	0.2914	0.2992	0.2914	0.2992	0.2914	0.2992	0.2914	0.2992	C
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		
H	0.228	0.244	0.228	0.244	0.228	0.244	0.394	0.419	0.394	0.419	0.394	0.419	0.394	0.419	
h	0.010	0.02	0.010	0.02	0.010	0.02	0.010	0.30	0.010	0.30	0.010	0.30	0.010	0.30	D
L	0.016	0.050	0.016	0.050	0.016	0.050	0.016	0.050	0.016	0.050	0.016	0.050	0.016	0.050	E
α	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	0°	8°	

Section 8 Military Products

MILITARY PRODUCT GUIDE

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL-M-38510 and MIL-STD-883 Programs are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. These programs are designed to provide our customers:

- Fully compliant 883/M5004 flows on all products.
- Standard processing flows to help minimize the need for custom specifications.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allow customers to buy products off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specifications.

The following explains the different processing options available. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2 and 3.

JAN QUALIFIED (JS and JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M-38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL 38510).

Quality conformance inspection testing, per MIL-STD-883, Method 5005, is performed according to Mil-M-38510 as follows:

- Group A; each subplot. (Alternate Group A)
- Group B; one subplot for each package type every week. (Alternate Group B)
- Group C; one subplot for each microcircuit group every 13 weeks.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES					
	CERAMIC					
	8-PIN	14-PIN	16-PIN	18-PIN	20-PIN	24-PIN
PB	FE	—	—	—	—	—
CB	—	F	—	—	—	—
EB	—	—	F	—	—	—
JB	—	—	—	—	—	F
DB	—	W	—	—	—	—
FB	—	—	W	—	—	—
RB	—	—	—	—	F	—
VB	—	—	—	F	—	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JS	JB	RB
	JAN Qualified		883B
	54	X	X
54LS	X	X	X
54S	X	X	X
54F	—	—	X
82	—	—	X
8T	—	—	X
93XX	—	X	X
96XX	—	—	X
Analog	—	X	X
Bipolar Memory	—	X	X
Microprocessor	—	—	X

Table 2 MILITARY SUMMARY

- Group D; one subplot for each package type every 26 weeks.

NOTE: This category of part conforms to Quality Level B ($\pi_0 = 1.0$) of MIL-HDBK-217D.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

By implementing this government standardization program, Signetics complies with the trend of reducing the numerous similar Source Control Drawings (SCD's). This standardized trend results in a single complete and comprehensive specification, a single product flow, and a single administrative effort—for both the aerospace community and for Signetics. Because the list of Signetics' qualified products will change periodically, you may wish to contact your nearest Signetics' Sales Office or refer to the *Products Qualified* under Military Specification from DESC for our current update.

JAN Class S products are quoted on a unit price basis only (similar to present Class B programs). There will be no lot charges for SEM inspection, electrical testing, or Group B or D quality conformance inspection. All additional charges are amortized in the unit price.

- Package types currently qualified are:
- 1) Cerdip—ceramic dual-in-line
 - 2) Cerpac—ceramic flat pack

Government Source Inspection (GSI) is a requirement of the JAN 38510 Class S specification. No alterations to this specification may be instituted. Therefore, the only allowed customer source inspection option is at pre-ship (verification only).

Additional program data options (such as wafer lot acceptance, attributes, Group B, D, and others) are available upon request for a nominal fee.

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to MIL-STD-883 Method 5004, and is 100% electrically tested to Signetics data sheets.

Quality conformance inspection per MIL-STD-883, Method 5005, Group A, is performed on each subplot. Group A subgroup electrical parameters are those included in the detailed Signetics data book. Contact the factory for parametric subgroup assignments.

Generic quality conformance data per Method 5005, Groups B, C, and D, is generally available on popular device types and packages, but availability is not guaranteed. The factory must be consulted



MILITARY PRODUCT GUIDE

prior to ordering generic data. When available, generic data is defined as follows:

- Group B: Performed once per package type every six weeks of seal.
- Group C: Performed once per microcir-

cuit group every 52 weeks of seal.

- Group D: Performed once per package type every 52 weeks of seal.

Quality conformance endpoint electrical parameters for Groups C and D are the

Group A subgroups 1, 2, and 3.

Copies of generic data, Groups A, B, C, and D, may be ordered by customers at a nominal charge.

NOTE: This category of part conforms of Quality Level B-2 ($\pi_0=6.5$) of MIL-HDBK-217D.

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 and MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS		
			JAN CLASS S	JAN QUALIFIED (B)	883
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program B. Manufacturer's Certification	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity.	—	X	X	N/A
2. Certification	Received after manufacturer has completed a successful DESC survey.	—	X	X	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to Groups A, B, C, and D of Method 5005.	—	X	X	N/A
4. Traceability	Traceability maintained back to wafer production lots.	—	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories.	—	X	X	N/A
Screening Per Method 5004 of Mil-Std-883					
6. Non-Destructive Bond Pull	2023	100%	x	N/A	N/A
7. Internal Visual (Precap)	2010, Cond. A or B	100%	A	B	B
8. Stabilization Bake	1008, Cond. C Min	100%	x	x	x
9. Temperature Cycling	1010, Cond. C; (10 cycles, -65°C to +150°C)	100%	x	x	x
10. Constant Acceleration	2001 Cond. E; Y1 (30 kg in Y1 Plane)	100%	x	x	x
11. Visual Inspection	There is no test method for this screen; it is intended only for the removal of Catastrophic Failures defined as Missing Leads, Broken Packages or Lids Off.	100%	x	x	x
12. Seal (Hermeticity) A. Fine B. Gross	1014 Cond. A or B; (5.0 x 10 ⁸ CC/Sec) 1014 Cond. C.	100% 100%	x x	x x	x x
13. Marking	Fungus inhibiting ink	100%	X	x	x
14. Particle Impart Noise Test	2020, Cond. A	100%	x	N/A	N/A
15. Radiographic	2012; two views	100%	x	N/A	N/A
16. Interim Electricals (Pre Burn-In)	Per applicable device specification	100%	x	Optional	Optional
17. Burn-In	1015, Cond. as specified (160 hrs. Min at 125°C Min)	100%	240 hrs.	x	x

Table 3. REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

MILITARY PRODUCT GUIDE

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 and MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS		
			JAN CLASS S	JAN QUALIFIED (B)	883
18. Final Electricals	Per applicable device specification	100%	100% Read & Record	Slash Sheet	Data Sheet
a. Static Tests @ 25°C	Subgroup 1		x	x	x
b. Static Tests @ + 125°C	Subgroup 2		x	x	x
c. Static Tests @ - 55°C	Subgroup 3		x	x	x
d. Dynamic Test @ 25°C	Subgroup 4 (for Linear Products only)		x	x	x
e. Functional Test @ 25°C	Subgroup 7		x	x	x
f. Switching Test @ 25°C	Subgroup 9		x	x	x
g. Switching Test @ temperature	Subgroup 10, 11, (as applicable)		x	x	x
19. Percent Defective Allowable (PDA)	A PDA of 10% is a requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JAN products. For RB, 10% is standard.	10%	5%	x	x
20. External Visual	2009	100%	x	x	x
Quality Conformance Inspection per Method 5005 of Mil-Std 883	ATTRIBUTE DATA ONLY				
21. Group A	Electrical Tests — Final Electricals (#18 above) repeated on a sample basis (Subgroups 1 through 12 as specified) performed in line with final electricals.	Each subplot	x	x	x
22. Group B	Package functional and constructional related test (package dimensions; resistance to solvents; internal, visual, and mechanical bond strength; and solderability).	Each pkg. type	Each subplot	Each week of seal	Generic
23. Group C	Die related tests (1,000 hour operating life, temperature cycling, and constant acceleration.	Each μ circuit group	N/A	Each 13 weeks of seal	Generic
24. Group D.	Package related tests (physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration, variable frequency, constant acceleration, and salt atmosphere).	Each pkg. type	Each 26 weeks of seal	Each 26 weeks of seal	Generic

Table 3. REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Continued)

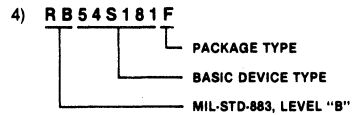
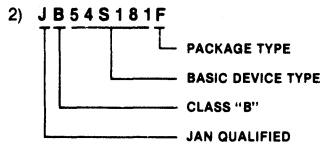
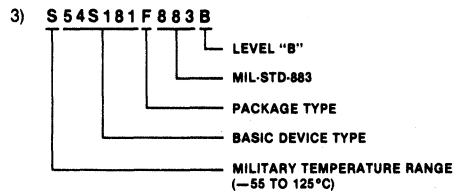
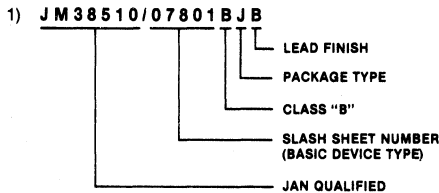
MILITARY PRODUCTS GUIDE

ORDERING INFORMATION

The Signetics Military Products are available in a variety of different process levels and several different packages. The correct ordering code or part number for the devices is an alphanumeric sequence as explained below. Not all devices are available in all

the packages. The ordering codes on the individual data sheets indicate the present or planned availability of the products. However, availability of specific part numbers can be obtained from your local sales office or franchised distributor.

Ordering Code



NOTE:

- 1) and 2) JAN qualified products.
- 3) and 4) Non-JAN MIL-STD-883 products.

For minimum quantity orders, contact your local Signetics sales representative.

PACKAGES AVAILABLE*

- F = Ceramic DIP
- I = Ceramic DIP
- G = Ceramic Leadless Chip Carrier
- W = Ceramic Flatpack

* See Package Outlines section for more information

For the latest military product information, please request a Military Products Guide from Publications Services, 408/746-2111.

Section 9

Package Outlines

PACKAGE OUTLINES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
 - a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power applications across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

9. Lead material
 - a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
 - b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated, or solder dipped.
 - c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
10. Body Material
 - a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
 - b. Ceramic with glass seal at leads.
 - c. BeO ceramic with glass seals at leads.
 - d. Ceramic with ASTM alloy F-30 or equivalent.

11. Lid Material
 - a. Nickel or tin plated nickel, weld seal.
 - b. Ceramic, glass seal.
 - c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
 - d. BeO ceramic with glass seal.
12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb 0.010 inches.
15. Maximum glass cimb or lid skew is 0.010 inches.
16. Typical four places.
17. Dimension also applied to seating plane.

PACKAGE OUTLINES

PLASTIC PACKAGES			
NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc} (°C/W) ²	DESCRIPTION
SO Packages			
14-Pin	D	NA	SO-14
16-Pin	D	NA	SO-16
16L-Pin	D	NA	SO-16L
20-Pin	D	NA	SO-20
24-Pin	D	NA	SO-24
28-Pin	D	NA	SO-28
Standard Dual-In-Line Packages			
14-Pin	N	86/48	
16-Pin	N	83/42	
20-Pin	N	61/24	
24-Pin	N	52/23	
28-Pin	N	85/23	

NOTE

1. For SO packages θ_{ja} (°C/W) only

HERMITIC PACKAGES FOR MILITARY ONLY			
NO. OF LEADS	PACKAGE CODE	Q_{ja}/Q_{jc} (°C/W)	DESCRIPTION
Cerdip Family			
14-Pin	F	110/30	Dual-In-Line Ceramic
16-Pin	F	100/30	Dual-In-Line Ceramic
20-Pin	F	90/25	Dual-In-Line Ceramic
24-Pin	F	60/26	Dual-In-Line Ceramic
Flat Packs			
14-Pin	W	205/50	Flat Ceramic
16-Pin	W	200/50	Flat Ceramic
28-Pin	W	107/22	Flat Ceramic, BEO
Leadless Chip Carrier			
20-Pin	G		Laminated Ceramic Side Brazed Lead

Package Type

D = Small Outline Plastic DIP

F = Cerdip

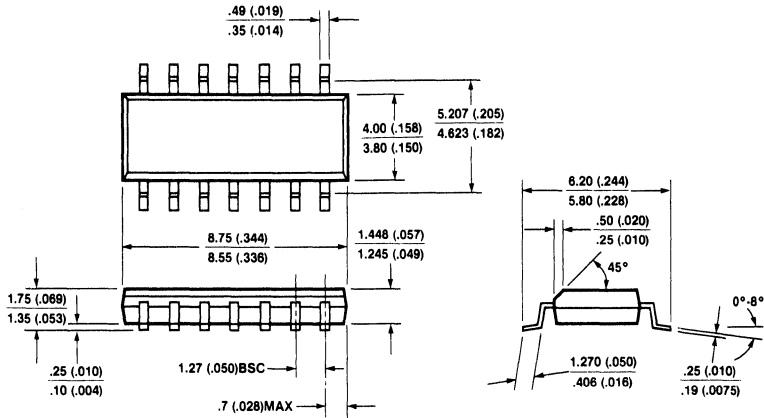
G = Hermetic Leadless

N = Plastic DIP

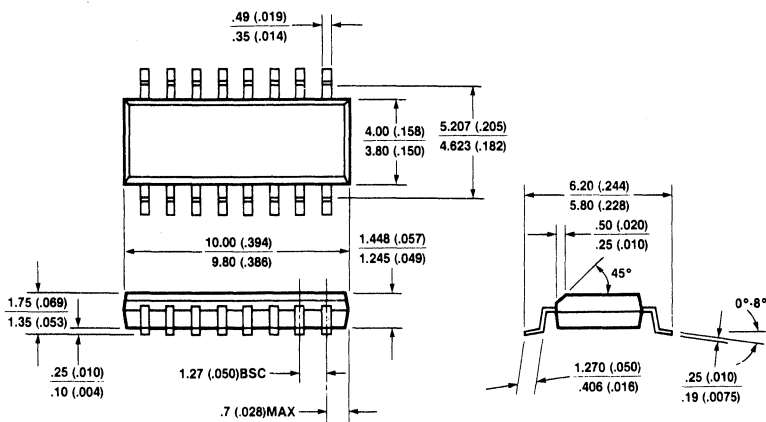
W = Ceramic Flatpack

PACKAGE OUTLINES

**SO-14 PACKAGE
(14-PIN)**

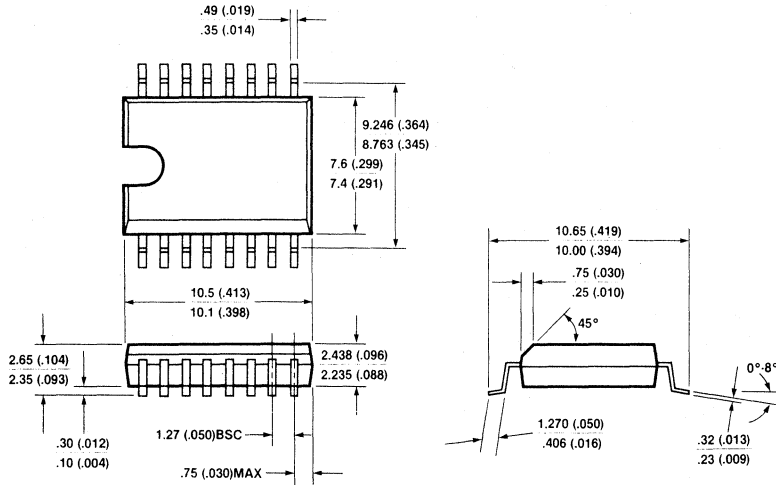


**SO-16 PACKAGE
(16-PIN)**

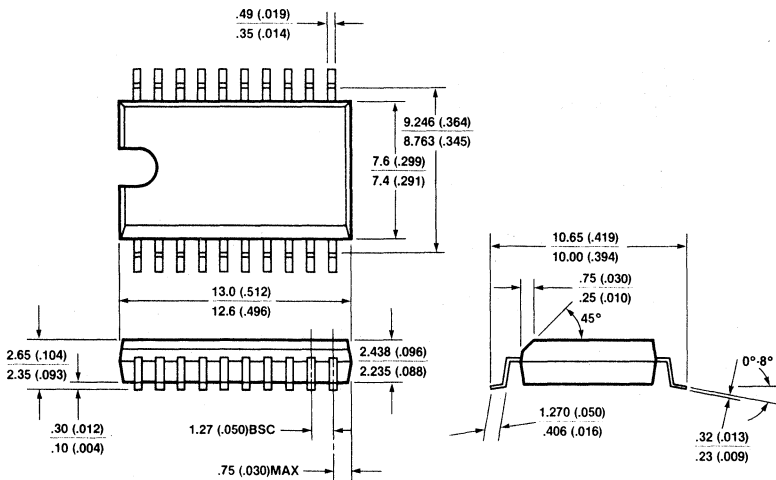


PACKAGE OUTLINES

SO-16L PACKAGE
(16-PIN)

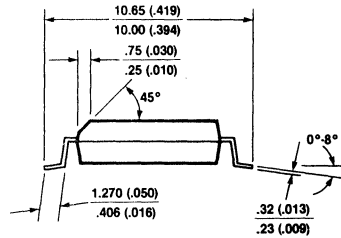
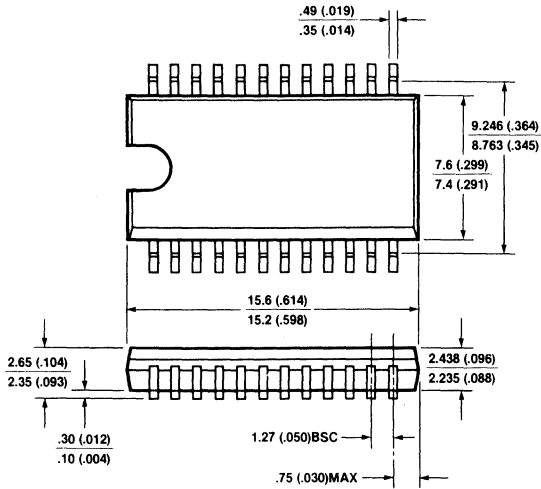


SO-20L PACKAGE
(20-PIN)

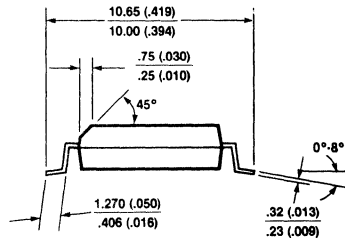
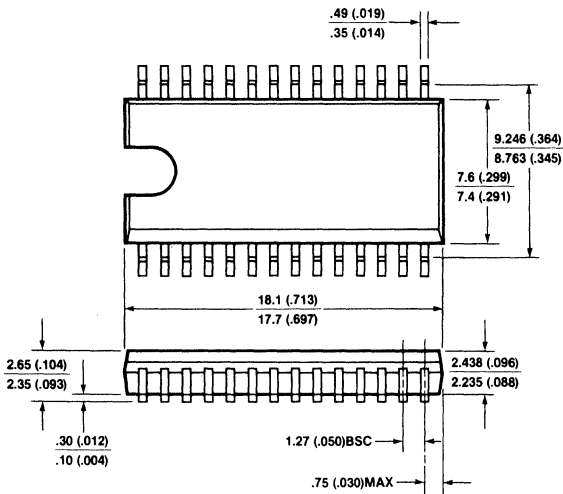


PACKAGE OUTLINES

SO-24 PACKAGE
(24-PIN)

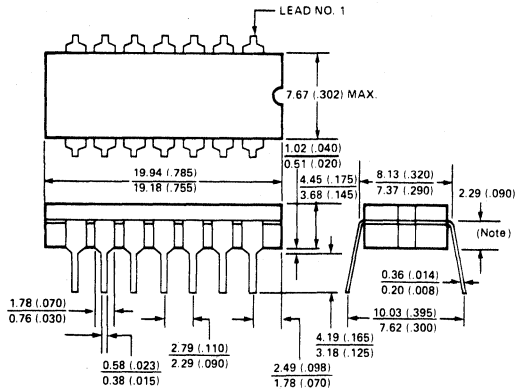


SO-28L PACKAGE
(28-PIN)

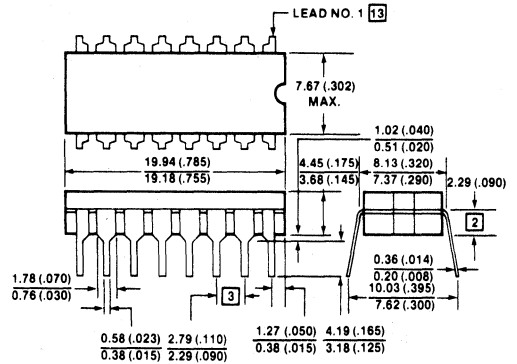


PACKAGE OUTLINES

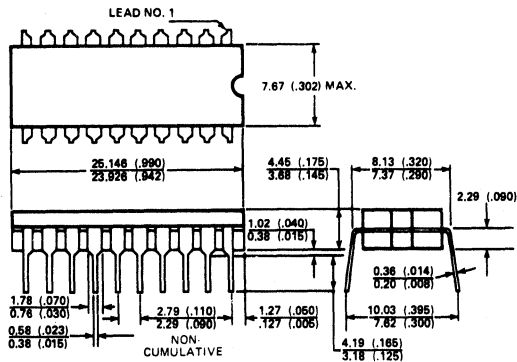
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(14-PIN DIP)



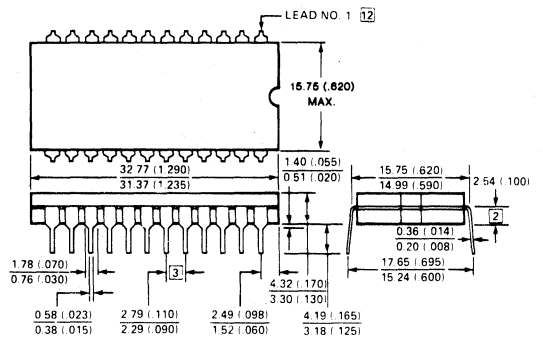
F PACKAGE CERAMIC
(16-PIN DIP)



F PACKAGE CERAMIC
(20-PIN DIP)

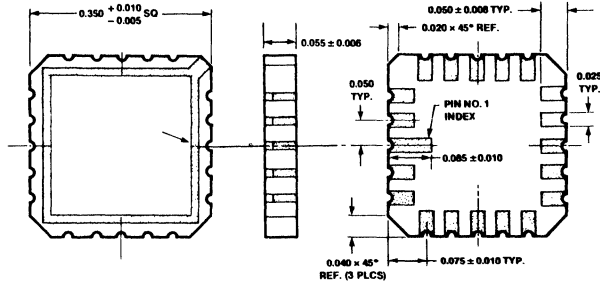


F PACKAGE CERAMIC
(24-PIN DIP)

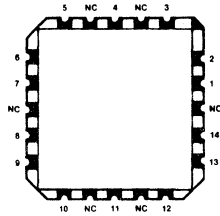


PACKAGE OUTLINES

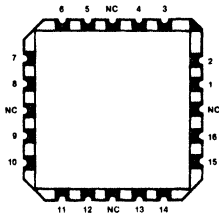
G PACKAGE



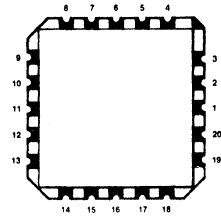
G PACKAGE
(14-PIN)



G PACKAGE
(16-PIN)

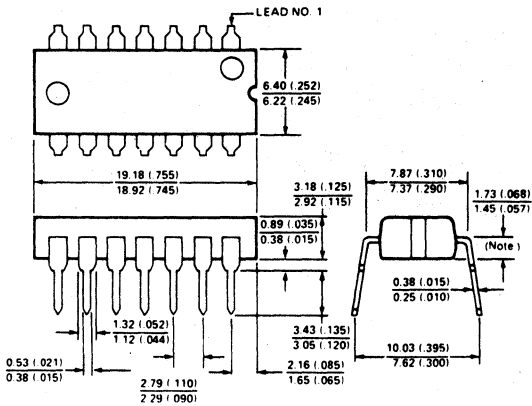


G PACKAGE
(20-PIN)

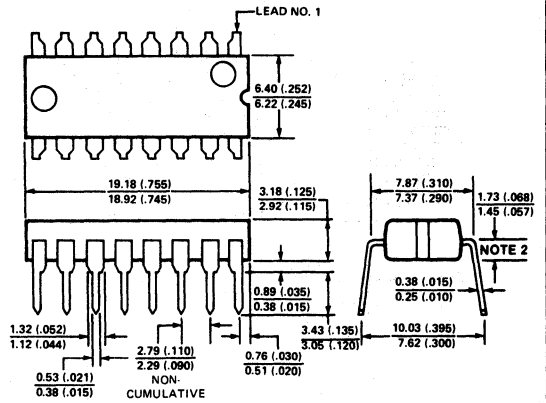


PACKAGE OUTLINES

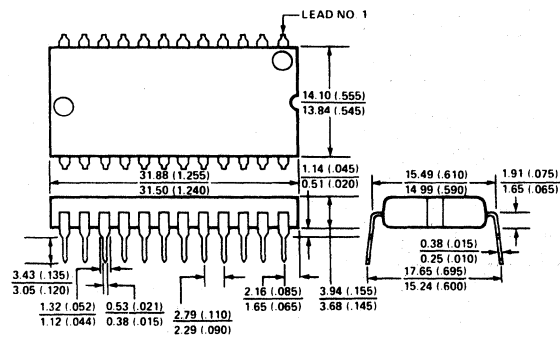
**N PACKAGE PLASTIC
(14-PIN DIP)**



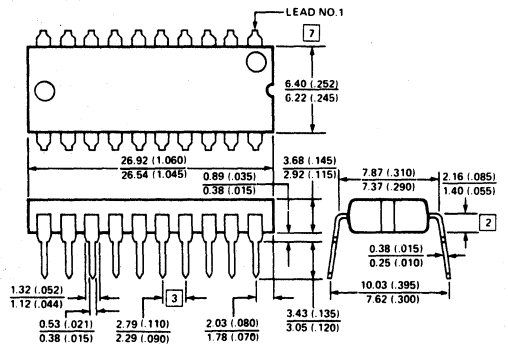
**N PACKAGE PLASTIC
(16-PIN DIP)**



**N PACKAGE PLASTIC
(20-PIN DIP)**

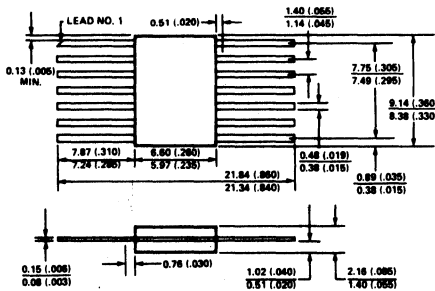


**N PACKAGE PLASTIC
(24-PIN DIP)**

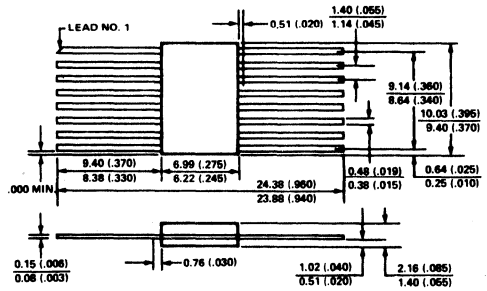


PACKAGE OUTLINES

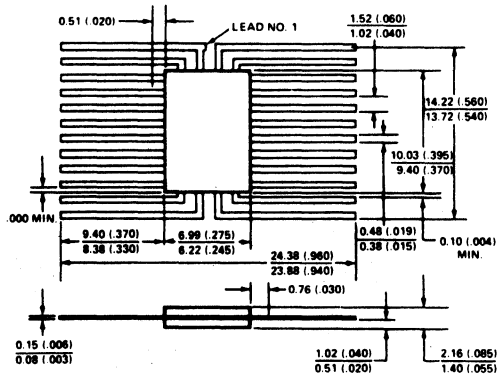
**W PACKAGE CERAMIC
(14-PIN FLATPACK)**



**W PACKAGE CERAMIC
(16-PIN FLATPACK)**



**W PACKAGE CERAMIC
(24-PIN FLATPACK)**



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