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Assemblies

C1

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Data handbook

Electronic components and materials

Components and materials

Part 1 May 1983

PLC modules

PC20 modules

HNIL FZ/30-series

NORbits 60-series, 61-series, 90-series

Input devices

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COMPONENTS AND MATERIALS

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DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of four series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

May 1980

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks is comprised of the following parts:

T1 **Tubes for r.f. heating**

T2 **Transmitting tubes for communications**

T3 **Klystrons, travelling-wave tubes, microwave diodes**

ET3 **Special Quality tubes, miscellaneous devices** (will not be reprinted)

T4 **Magnetrons**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T7 **Gas-filled tubes**
Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories

T8 **Picture tubes and components**
Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display

T9 **Photo and electron multipliers**
Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates

T10 **Camera tubes and accessories, image intensifiers**

T11 **Microwave components and assemblies**

January 1982

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks is comprised of the following parts:

S1 **Diodes**
Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes(< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes

S2 **Power diodes, thyristors, triacs**
Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs

S3 **Small-signal transistors**

S4 **Low-frequency power transistors and hybrid IC modules**

S5 **Field-effect transistors**

S6 **R.F. power transistors and modules**

S7 **Microminiature semiconductors for hybrid circuits**

S8 **Devices for optoelectronics**
Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.

S9 Taken into handbook T11 of the blue series

S10 **Wideband transistors and wideband hybrid IC modules**

January 1982

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks is comprised of the following parts:

IC1 **Bipolar ICs for radio and audio equipment**

IC2 **Bipolar ICs for video equipment**

IC3 **ICs for digital systems in radio, audio and video equipment**

IC4 **Digital integrated circuits**
LOCMOS HE4000B family

IC5 **Digital integrated circuits – ECL**
ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs

IC6 **Professional analogue integrated circuits**

IC7 **Signetics bipolar memories**

IC8 **Signetics analogue circuits**

IC9 **Signetics TTL logic**

IC10* **Signetics Integrated Fuse Logic (IFL)**

IC11* **Microprocessors, microcomputers and peripheral circuitry**

* This handbook will be available later this year.

February 1983

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks is comprised of the following parts:

C1 **Assemblies for industrial use**
PLC modules, PC20 modules, HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs

C2 **Television tuners, video modulators, surface acoustic wave filters**

C3 **Loudspeakers**

C4 **Ferroxcube potcores, square cores and cross cores**

C5 **Ferroxcube for power, audio/video and accelerators**

C6 **Electric motors and accessories**
Permanent magnet synchronous motors, stepping motors, direct current motors

C7 **Variable capacitors**

C8 **Variable mains transformers**

C9 **Piezoelectric quartz devices**
Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements

C10 **Connectors**

C11 **Non-linear resistors**
Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)

C12 **Variable resistors and test switches**

C13 **Fixed resistors**

C14 **Electrolytic and solid capacitors**

C15 **Film capacitors, ceramic capacitors**

C16 **Piezoelectric ceramics, permanent magnet materials**

January 1983

PLC MODULES

MODULES FOR PROGRAMMABLE LOGIC CONTROLLERS

INTRODUCTION

The programmable logic controller (PLC) is used for the controlling of machines or processes. It can be easily programmed and re-programmed as required.

The modular design of the PLC enables a user to build a PLC which is 'tailor-made' for his control task. By specifying the number and the types of PLC modules that he requires, he avoids purchasing more of the expensive electronic capability than he needs.

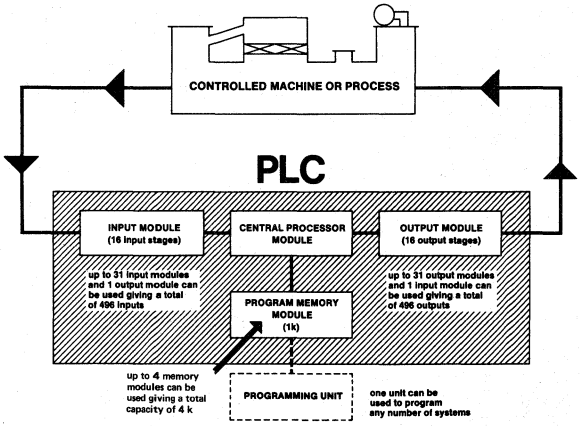
The PLC modules are formed on standard double Eurocards. Optically coupled interface circuits, specifically designed for an industrial environment, provide excellent noise immunity and a high degree of isolation. The internationally accepted machine signal level of 24 V is used and generous tolerances on operational margins and thresholds ease compatibility headaches.
Besides the PLC modules, the PLC comprises back panels, a frame (19 in rack) and a standard power supply. The frame must conform to IEC297 or DIN41494 (for racks) and IEC130-14 or DIN41612 (for connectors). The adoption of these standards means that the frame and the power supply should be easily obtainable.

The following PLC modules are available.

type	description	catalogue no.
CP10	central processor, 32 registers	4322 027 90420
CP11	central processor, without registers	4322 027 90390
IM10	input module, 16 inputs, 24 V d.c.	4322 027 90434
IM11	input module, 16 inputs, 24 V a.c.	4322 027 90403
LX10	load external interface module	4322 027 91600
MM10	program memory module, 1 k, non-volatile core RAM	4322 027 91400
MM11	program memory module, non-volatile, UV-erasable PROMs, 1 k 13 or 2 k 13 capacity; for program copying or read-out	4322 027 91630
MM12	program memory module, non-volatile, UV-erasable PROMs, 1 k 13 or 2 k 13 capacity: for read-out only	4322 027 91640
OM10	output module, 16 outputs, max. 0,1 A each, 24 V d.c.	4322 027 90440
OM12	output module, 8 outputs max. 2 A each, 24 V d.c.	9360 011 50112
PI10*	punch and teletype interface module	8222 412 41572
PU10	programming unit	4322 027 90410
BP11 to BP16	back panels	9390 269 .0112

* Development type.

The diagram shows, in a simplified form, the function of each of the PLC modules. In operation the PLC cycles continuously through a data input/output cycle and a data processing cycle.



The input module converts the signals from the plant into a binary form acceptable to the central processor.

The central processor reads the data from the input module, performs logic equations on it in accordance with the program instructions and transfers the results to the output module.

The output module converts the binary data from the central processor to electrical signals suitable for the control of the plant.

The program memory is the store in which the set of instructions that comprise the program are stored. These instructions dictate the actions which must be taken in response to the condition of each input.

The programming unit is the means by which an operator can write a program, or changes to a program, into the program memory. The unit is portable and thus one may be used to serve any number of PLCs. It is also sufficiently inexpensive to make the permanent location of one in each PLC for monitoring or test purposes, a realistic and useful proposition.

GENERAL CHARACTERISTICS

Operating temperature range	0 to +60 ^{o}C
Storage temperature range	-40 to +70 ^{o}C
Dimensions	160 mm x 233 mm (double Eurocard) according to IEC297 or DIN41494
Supply voltage (d.c.)	V_P = 5 V ±5%; $\frac{dV_P}{dt} \leq$ 5 V/ms
Maximum number of input + output signals	512
Maximum program length	4 x 1024 words
Cycle time	0,029 ($n_{IM} + n_{OM}$) + 1,85 n_{MM} ms n_{IM} = number of input modules n_{OM} = number of output modules n_{MM} = number of memory modules

TESTS AND REQUIREMENTS

All modules are designed to meet the tests below.

Vibration test

IEC68-2, test method Fc: 5 to 55 Hz, amplitude 1,5 mm or 5 g (whichever is less).

Shock test

IEC68-2, test method Ea: 3 shocks in 6 directions, pulse duration 11 ms, peak acceleration 50 g.

Rapid change of temperature test

IEC68-2, test method Na: 5 cycles of 2 h at -40 ^{o}C and 2 h at +70 ^{o}C.

Damp heat test

IEC68-2, test method Ca: 21 days at 40 ^{o}C, R.H. 90 to 95%.

CENTRAL PROCESSORS

DESCRIPTION

These central processors are modules intended for use in combination with the input module IM10 (or IM11), memory module MM10 (or MM11 or MM12), output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC). The central processor is the heart of the logic controller; it asks the input modules for data and the program memory for instructions, processes the data according to these instructions, and applies the result to the output modules. It also generates the internal timing of the controller.

The processor actions take place in two distinct cycles: an input/output cycle and a data processing cycle.
During the input/output cycle the processor addresses each input stage in turn (counter/buffer register) and transfers the present data to the corresponding scratch-pad memory location, see Fig. 1. In the same cycle the processed data of the previous data processing cycle are clocked out from the scratch-pad memory into the latch flip-flops of the output modules. As the scratch-pad memory can hold up 512 bits of data the central processor can handle a maximum combination of 512 inputs, outputs, and intermediate results. Provision is made to prevent loss of information of the scratch-pad memory in the case of power failure.

During the data processing cycle the processor applies an address and a cycle initiate signal to the program memory, which in turn then apply a program word to the processor. The program word contains an instruction and an address, which comprise 13 data bits. An instruction consists of 4 bits of data; these are applied to the logic processing unit and the register processing unit. [1]) The other 9 bits of data form the scratch-pad memory address and are used to select the data bit at this memory location, and also one of the 32 8-bit registers. [1]) The logic processing unit only processes data from the scratch-pad memory. The register processing unit processes the data stored in one of the 8-bits registers, in conjunction with a working register (A-register). Due to the fact that a register is always selected when a scratch-pad memory address is selected, the results of register processing will be stored in the corresponding scratch-pad memory location (condition register). Data for the registers can be supplied by the program memory or by an external source. These data are stored in the registers during the data processing cycle.

[1]) Only present in the CP10.

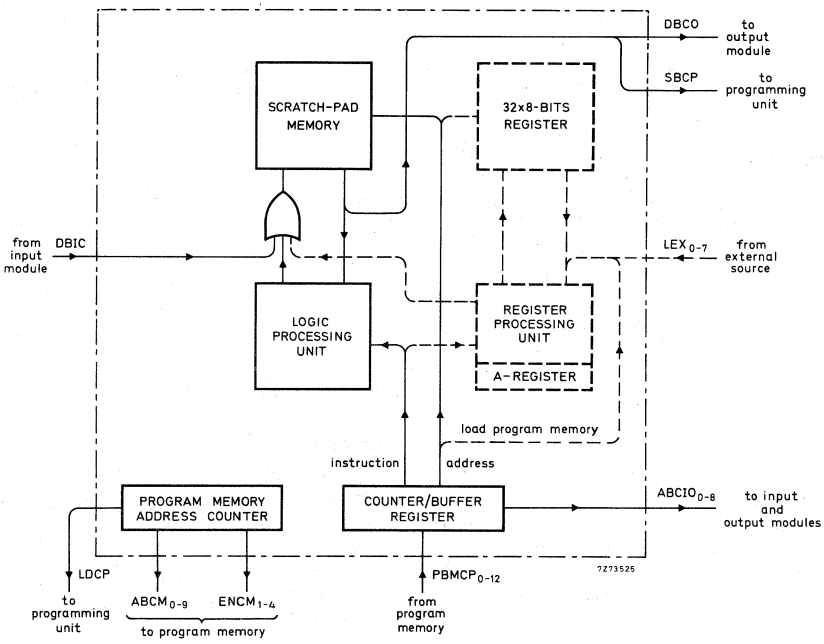


Fig. 1. Simplified block diagram of the central processor. Blocks drawn with broken lines are only extant in the CP10.

The central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card system). The board is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 2422 025 89288 (pins for wire wrap), 2422 025 89298 (pins for dip soldering) or 2422 025 89326 (solder tags) [1]. The board has a metal screen at the components side, which is connected to the 0 V line.

[1]) For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	5 V ± 5%
current	I_P	max. 2,1 A
		typ. 1,9 A

Battery back-up requirements to save contents of the scratch-pad memory in case of power failure.

Battery voltage	V_B	4,5 to 7,5 V
Battery current (V_P = 0 V)	I_B	typ. 3,5 mA at V_B = 5 V
Trickle charge current (V_P = 5 V)		typ. 2 mA at V_B = 5 V

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig. 4)	
			connector 1	connector 2
$PBMCP_0$	Program word bits from program memory.	1 TTL		a2, c2
$PBMCP_1$		1 TTL		a3, c3
$PBMCP_2$		1 TTL		a4, c4
$PBMCP_3$		1 TTL		a5, c5
$PBMCP_4$		1 TTL		a6, c6
$PBMCP_5$		1 TTL		a7, c7
$PBMCP_6$		1 TTL		a8, c8
$PBMCP_7$		1 TTL		a9, c9
$PBMCP_8$		1 TTL		a10, c10
$PBMCP_9$		1 TTL		a11, c11
$PBMCP_{10}$		1 TTL		a12, c12
$PBMCP_{11}$		1 TTL		a13, c13
$PBMCP_{12}$		1 TTL		a14, c14
MICC	Memory identification signal; this signal is connected to one of the four ENCM-outputs of the central processor.	2 TTL	a5	
SCPC	Store command from programming unit; initiates SCCM (see output data) when the central processor is in a data processing cycle.	2 TTL		a15, c15
DBIC	Data bit from input stage; data is stored in scratch-pad memory during input/output cycle.	3 TTL	c20	
CLCP	Clear signal from external source. When CLCP is LOW the central processor is kept in the start position of an input/output cycle; when CLCP is HIGH the central processor is running (see also SPCE).	2 TTL	a20	

input	function	load	terminations (Fig. 4)	
			connector 1	connector 2
SPCE	Scratch-pad clear enable line from external source. When SPCE is HIGH and CLCP goes from LOW to HIGH all scratch-pad places (except those which are addressed as an input) are set to zero in the first input/output cycle; when SPCE is LOW and CLCP goes from LOW to HIGH the central processor starts with a normal input/output cycle.	2 TTL	a22	
IDIC	Identification signal from input module; prepares central processor for data on DBIC to be written in the scratch-pad memory.	3 TTL	c24	
IDLC	Identification signal from last input or output module; indicates that the last input or output module has been selected.	2 TTL	c26	
LEX_0	Data inputs from an external source; eight data bits from an external source can be loaded into the A-register.	1 TTL	a6	
LEX_1		1 TTL	a7	
LEX_2		1 TTL	a8	
LEX_3		1 TTL	a9	
LEX_4		1 TTL	a10	
LEX_5		1 TTL	a11	
LEX_6		1 TTL	a12	
LEX_7		1 TTL	a13	

Output data

All outputs meet the standard TTL specifications.

output	function	loadability	terminations (Fig. 4)	
			connector 1	connector 2
$ABCIO_0$	Address bits to input and output modules. $ABCIO_{0-3}$ select the input or output stage, $ABCIO_{4-8}$ select the input or output modules.	32 TTL	c2	
$ABCIO_1$		32 TTL	c4	
$ABCIO_2$		32 TTL	c6	
$ABCIO_3$		32 TTL	c8	
$ABCIO_4$		32 TTL	c10	
$ABCIO_5$		32 TTL	c12	
$ABCIO_6$		32 TTL	c14	
$ABCIO_7$		32 TTL	c16	
$ABCIO_8$		32 TTL	c18	

output	function	loadability	terminations (Fig. 4)	
			connector 1	connector 2
$ABCM_0$	Address bits to program memory, initiated by program address counter.	10 TTL		a20, c20
$ABCM_1$		10 TTL		a21, c21
$ABCM_2$		10 TTL		a22, c22
$ABCM_3$		10 TTL		a23, c23
$ABCM_4$		10 TTL		a24, c24
$ABCM_5$		10 TTL		a25, c25
$ABCM_6$		10 TTL		a26, c26
$ABCM_7$		10 TTL		a27, c27
$ABCM_8$		10 TTL		a28, c28
$ABCM_9$		10 TTL		a29, c29
$ENCM_1$	Enable signal to program memory; four lines are necessary when program memory capacity is extended to 4 k	8 TTL	a1, c1	
$ENCM_2$		8 TTL	a2	
$ENCM_3$		8 TTL	a3	
$ENCM_4$		8 TTL	a4	
SCCM	Store command to program memory; level determines whether a program word is read out from program memory to central processor (LOW) or a new program word is written into the program memory (HIGH). SCCM = $\overline{SCPC}$.	10 TTL		a17, c17
CICM	Cycle initiate signal to program memory; depending on the level of SCCM, CICM starts read/restore or clear/write cycle (bipolar to reduce noise sensitivity).	9 TTL		a19, c19
$\overline{CICM}$				a18, c18
$\overline{CL_{23}}$	Inverted clock signal to programming unit.	10 TTL	a15	
CLCO	Clock signal to output module, stores data on DBCO into output stage during input/output cycle.	32 x OM10	a28	
DBCO	Data bit to output module; data is stored in output stage by CLCO.	31 TTL	c22	
SBCP	Status bit to programming unit; clocked by ϕ_{57} it indicates "1" or "0" at selected scratch-pad memory address.	1 TTL	a16	
LDCP	Synchronization signal to programming unit, synchronizes auxiliary address counter in programming unit with address counter in central processor.	10 TTL	a14	
ϕ_{57}	Clock signal for state indication on programming unit; occurs only during data processing cycle.	10 TTL		a16, c16

Alarm output (a26 of connector 1): open collector output, which indicates a LOW level when $V_P < 4,75$ V. V_{alarm}, LOW level < 0,4 V at $I_C = 3$ mA.

Time data

Scan time per input or output module	0,029 ms
Read time per 1 k memory module	1,85 ms
Total cycle time	$0,029\ (n_{IM} + n_{OM}) + 1,85\ n_{MM}$ ms

n_{IM} = number of input modules
n_{OM} = number of output modules
n_{MM} = number of memory modules

Note - By removing a wire jump, marked "A", on the central processor board the scan time per input or output module is set to 7,4 ms.

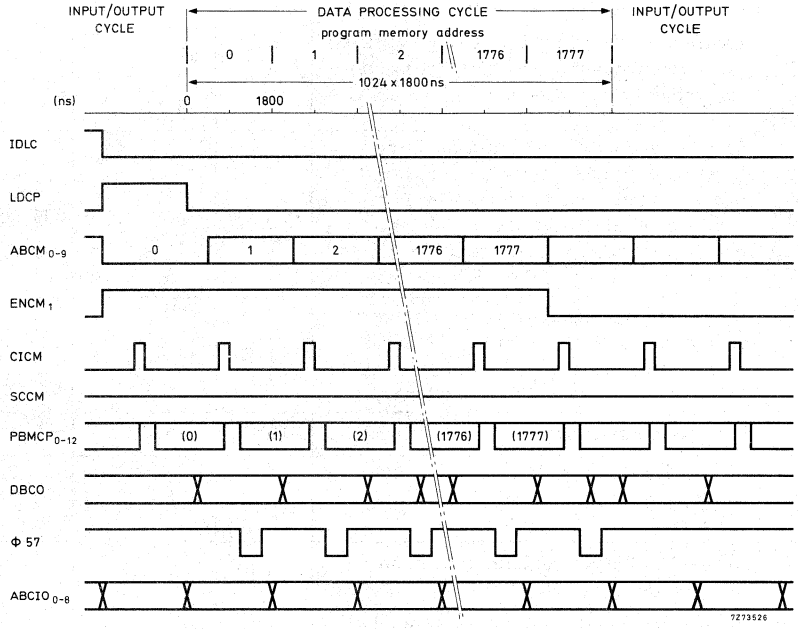


Fig. 2. Timing diagram of data processing cycle.

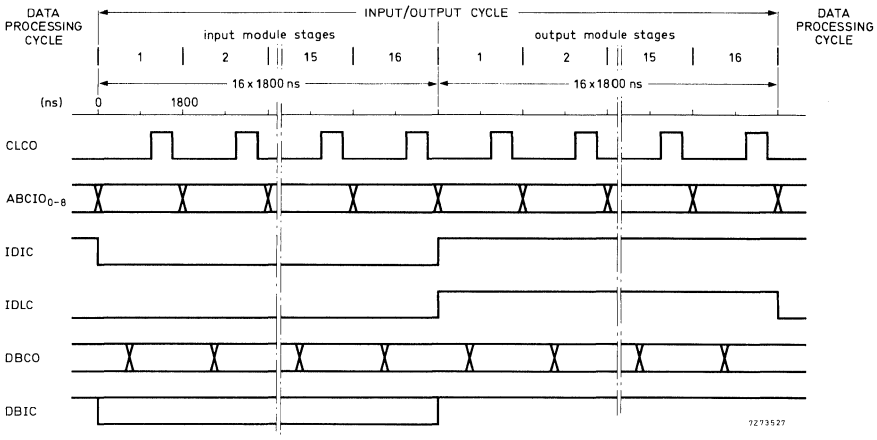


Fig. 3. Timing diagram of input/output cycle.

MECHANICAL DATA

Dimensions in mm

Outlines

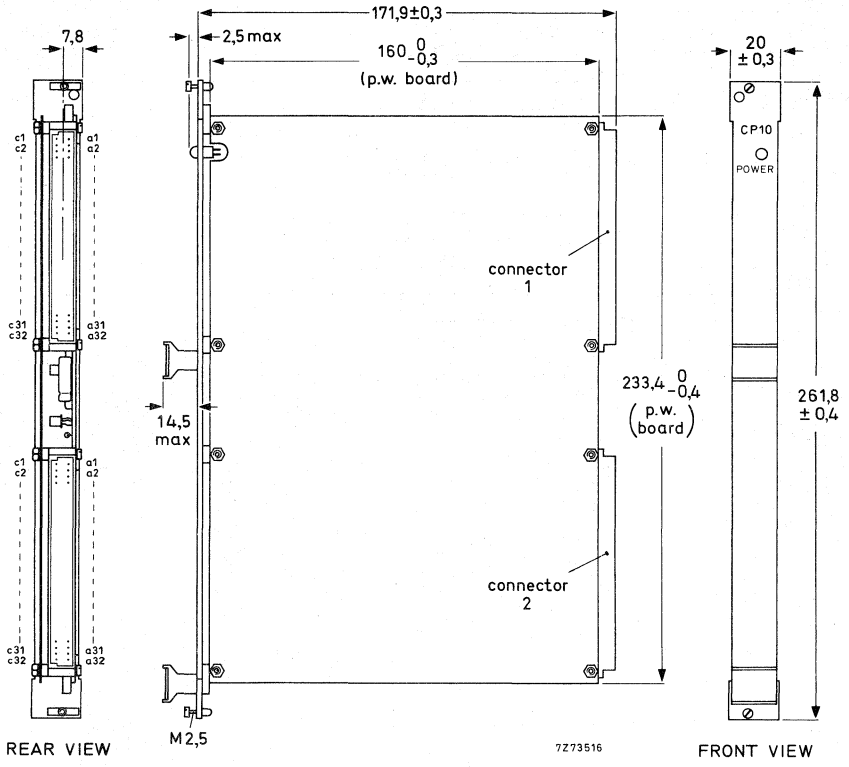


Fig. 4

Mass 400 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
$ENCM_1$	1	$ENCM_1$	i.c.	1	i.c.
$ABCIO_0$	2	$ENCM_2$	$PBMCP_0$	2	$PBMCP_0$
n.c.	3	$ENCM_3$	$PBMCP_1$	3	$PBMCP_1$
$ABCIO_1$	4	$ENCM_4$	$PBMCP_2$	4	$PBMCP_2$
n.c.	5	MICC	$PBMCP_3$	5	$PBMCP_3$
$ABCIO_2$	6	LEX_0	$PBMCP_4$	6	$PBMCP_4$
n.c.	7	LEX_1	$PBMCP_5$	7	$PBMCP_5$
$ABCIO_3$	8	LEX_2	$PBMCP_6$	8	$PBMCP_6$
n.c.	9	LEX_3	$PBMCP_7$	9	$PBMCP_7$
$ABCIO_4$	10	LEX_4	$PBMCP_8$	10	$PBMCP_8$
n.c.	11	LEX_5	$PBMCP_9$	11	$PBMCP_9$
$ABCIO_5$	12	LEX_6	$PBMCP_{10}$	12	$PBMCP_{10}$
n.c.	13	LEX_7	$PBMCP_{11}$	13	$PBMCP_{11}$
$ABCIO_6$	14	$\overline{LDCP}$	$PBMCP_{12}$	14	$PBMCP_{12}$
n.c.	15	$\overline{CL_{23}}$	SCPC	15	SCPC
$ABCIO_7$	16	SBCP	$\phi 57$	16	$\phi 57$
n.c.	17	n.c.	$\overline{SCCM}$	17	$\overline{SCCM}$
$ABCIO_8$	18	n.c.	$\overline{CICM}$	18	$\overline{CICM}$
n.c.	19	n.c.	CICM	19	CICM
DBIC	20	CLCP	$ABCM_0$	20	$ABCM_0$
n.c.	21	n.c.	$ABCM_1$	21	$ABCM_1$
DBCO	22	SPCE	$ABCM_2$	22	$ABCM_2$
n.c.	23	n.c.	$ABCM_3$	23	$ABCM_3$
IDIC	24	n.c.	$ABCM_4$	24	$ABCM_4$
n.c.	25	n.c.	$ABCM_5$	25	$ABCM_5$
IDLC	26	alarm	$ABCM_6$	26	$ABCM_6$
n.c.	27	n.c.	$ABCM_7$	27	$ABCM_7$
0 V[1])	28	CLCO	$ABCM_8$	28	$ABCM_8$
n.c.	29	n.c.	ABCM9	29	ABCM9
n.c.	30	n.c.	V_B	30	V_B
V_P	31	V_P	V_P	31	V_P
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.
i.c. = internal connection.

[1]) No supply line; only to be used as a ground connection for CLCO.

INPUT MODULES

DESCRIPTION

These input modules are intended for use in combination with the central processor CP10 (or CP11), memory module MM10 (or MM11 or MM12), output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The IM10 and IM11 are identical in many respects, but the IM10 is designed for d.c. inputs, whereas the IM11 is designed for a.c. and unsmoothed rectified inputs. Each input module contains 16 addressable input stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. Each input stage has a LED for status indication: it is lit when the input is active. A delay circuit (symmetrical delay time typ. 1 ms) is incorporated in each input stage of the IM10, to increase the noise immunity. The delay time can be increased by adding extra capacitance (approx. 0,068 μF/ms). A rectifying and smoothing circuit is incorporated in each input stage of the IM11.

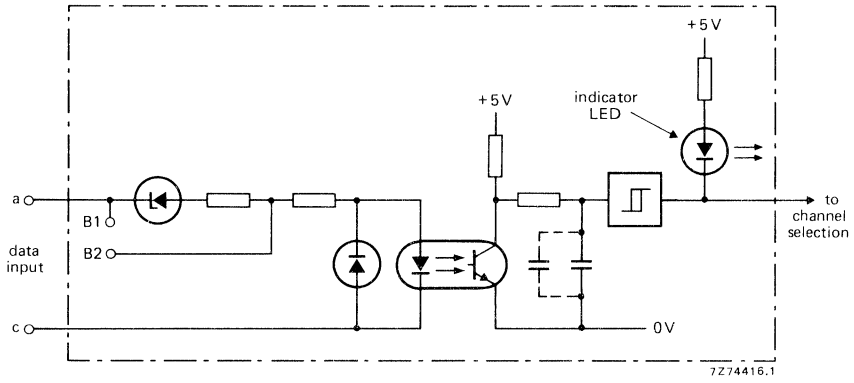


Fig. 1a Circuit diagram of an input stage (IM10).

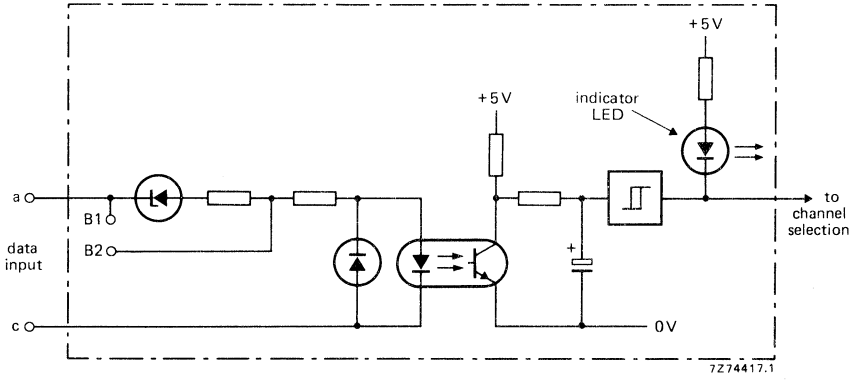


Fig. 1b Circuit diagram of an input stage (IM11).

Each input module has nine address inputs ($ABCIO_{0-8}$) and five module identification inputs ($\overline{MID}_{0-4}$), which are accessible on the connectors at the rear (Fig. 2).

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card system). The board is provided with two F068-1 connectors (board parts); the corresponding rack parts are available on the back panels BP11 to BP16 or separately under catalogue number 2422 025 89291 (pins for wire wrapping), 2422 025 89299 (pins for dip soldering) or 2422 025 89327 (solder tags).*

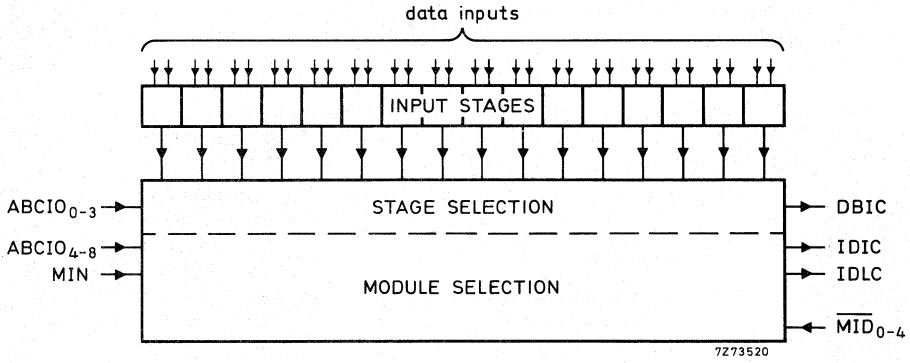


Fig. 2 Block diagram of the input modules.

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	5 V ± 5%
current	I_P	max. 0,5 A
		typ. 0,45 A

Input data

The data inputs are DI_{XY0} to DI_{XY7} and DI_{XZ0} to DI_{XZ7}. They are accessible on connector 2, see "Terminal location".

	5 V level**	24 V level
Active voltage (V_{a-c})*	3,5 to 6 V▲	17 to 30 V▲
Non-active voltage (V_{a-c})*	0 to 0,8 V or floating▲	0 to 7 V or floating▲
Input current, active at V_{a-c} = 5 V or 24 V resp.	typ. 10 mA	typ. 10 mA

The inputs mentioned below meet the standard TTL specifications.

input	function	load	terminations of connector 1 (Fig. 3)
$ABCIO_0$	Address bits from central processor; $ABCIO_{0-3}$ select the input stage, $ABCIO_{4-8}$ selection the input module.	1 TTL	a2, c2
$ABCIO_1$		1 TTL	a4, c4
$ABCIO_2$		1 TTL	a6, c6
$ABCIO_3$		1 TTL	a8, c8
$ABCIO_4$		1 TTL	a10
$ABCIO_5$		1 TTL	a12
$ABCIO_6$		1 TTL	a14
$ABCIO_7$		1 TTL	a16
$ABCIO_8$		1 TTL	a18
MIN	Module inhibit signal from external source; a low level applied to this input inhibits data on DBIC to be stored in the scratch-pad memory of the central processor.	2 TTL	c26
$\overline{MID}_0$	Module identification inputs; provide module with individual identity.	2 TTL	c10
$\overline{MID}_1$		2 TTL	c12
$\overline{MID}_2$		2 TTL	c14
$\overline{MID}_3$		2 TTL	c16
$\overline{MID}_4$		2 TTL	c18

* Voltage between terminal of row a and terminal of row c of connector 2.
** By short-circuiting terminals B1 and B2 (see Figs 1a and 1b).
▲ D.C. (for IM10) or a.c. values (for IM11).

Output data

All outputs (open collector) meet the standard TTL specifications.

output	function	loadability	terminations of connector 1 (Fig. 3)
DBIC	Data bit to central processor; data is stored in scratch-pad memory of central processor.	10 TTL	a20
IDIC	Identification signal to central processor (active LOW); prepares central processor for data on DBIC to be written in the scratch-pad memory.	10 TTL	c24
IDLC	Identification signal from last input module to central processor (active HIGH); only the IDLC output of the last input module has to be connected with the IDLC input of the central processor.	2 TTL	a26

MECHANICAL DATA

Dimensions in mm

Outlines

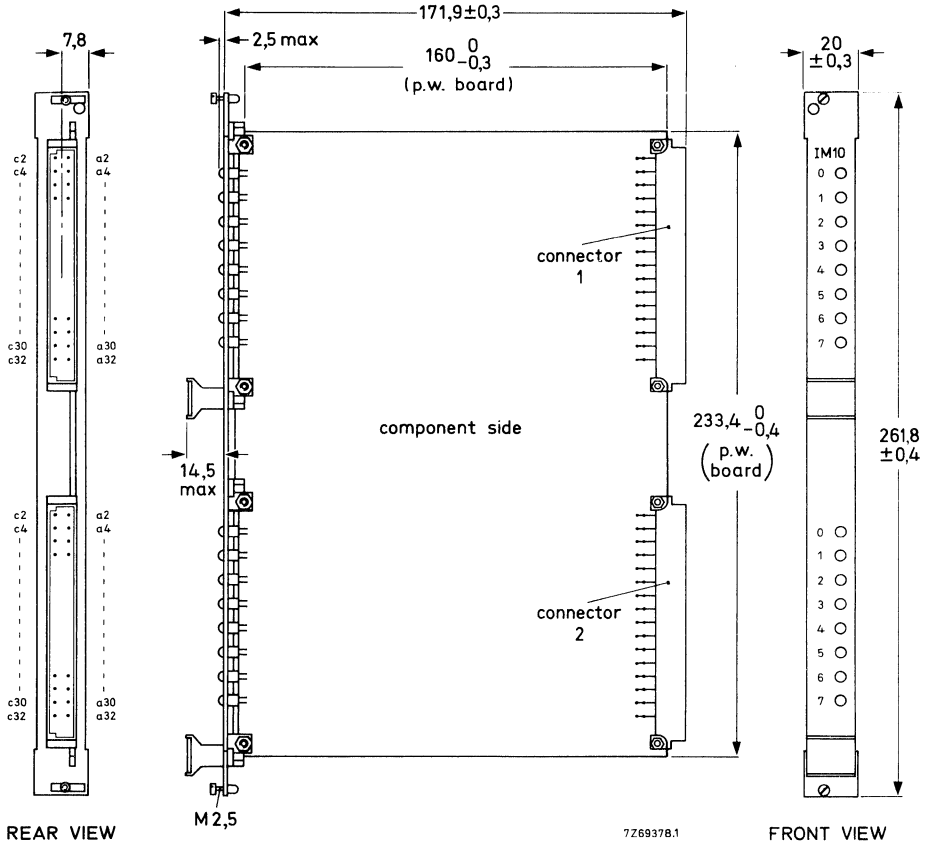


Fig. 3.

Mass 250 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
$ABCIO_0$	2	$ABCIO_0$	DI_{XY0}	2	DI_{XY0}
$ABCIO_1$	4	$ABCIO_1$	DI_{XY1}	4	DI_{XY1}
$ABCIO_2$	6	$ABCIO_2$	DI_{XY2}	6	DI_{XY2}
$ABCIO_3$	8	$ABCIO_3$	DI_{XY3}	8	DI_{XY3}
$\overline{MID}_0$	10	$ABCIO_4$	DI_{XY4}	10	DI_{XY4}
$\overline{MID}_1$	12	$ABCIO_5$	DI_{XY5}	12	DI_{XY5}
$\overline{MID}_2$	14	$ABCIO_6$	DI_{XY6}	14	DI_{XY6}
$\overline{MID}_3$	16	$ABCIO_7$	DI_{XY7}	16	DI_{XY7}
$\overline{MID}_4$	18	$ABCIO_8$	DI_{XZ0}	18	DI_{XZ0}
0 V*	20	DBIC	DI_{XZ1}	20	DI_{XZ1}
0 V*	22	n.c.	DI_{XZ2}	22	DI_{XZ2}
IDIC	24	n.c.	DI_{XZ3}	24	DI_{XZ3}
MIN	26	IDLC	DI_{XZ4}	26	DI_{XZ4}
n.c.	28	n.c.	DI_{XZ5}	28	DI_{XZ5}
V_P	30	V_P	DI_{XZ6}	30	DI_{XZ6}
0 V	32	0 V	DI_{XZ7}	32	DI_{XZ7}

n.c. = not connected.

* No supply line; only to be used for coding of the $\overline{MID}_{0\text{-}4}$ lines.

LOAD EXTERNAL INTERFACE

DESCRIPTION

This load external interface is intended for use in combination with the central processor CP10, input module IM10 or IM11, output module OM10 or OM12, memory module MM10, MM11 or MM12 and programming unit PU10 to assemble a programmable logic controller (PLC). The module can be used as an interface between the load external inputs LEX_0 to LEX_7 on the CP10 and a number of 8-bit data sources. The data outputs of the different data sources have to be connected to one 8-bit data bus. The LX10 has 16 enable outputs $\overline{EN}_0$ to $\overline{EN}_{17}$, which are to enable the different data sources. The 8-bit data bus has to be connected to the data inputs DB_0 to DB_7. The data applied to the data inputs can be inverted on the LX10 by activating the data bit invert input DBI (see the truth table on the next page). The applied data can have a 5 V or a 24 V level. A block diagram is given in Fig. 1. The data inputs and enable outputs are electrically isolated from the 5 V logic circuitry by means of photocouplers. All data inputs are floating with respect to each other. Reading data from the data sources will only occur during the input/output cycle. The data are then stored in a 16 x 8 random-access memory (RAM) on the LX10. The data can be read out of the RAM during the data processing cycle. Storing data into the RAM can be inhibited by applying a 0 V level to the module inhibit input (MIN). Reading data out of the RAM cannot be inhibited. The module has 6 address inputs $ABCIO_3$ to $ABCIO_8$. This means that a total number of 64 data sources of 8-bits can be connected to the PLC system via 4 LX10 modules. Therefore the module is provided with 2 module identification inputs ($\overline{MID}_3$, $\overline{MID}_4$) which are accessible on the connector. Irrespective of the number of LX10 modules used, a complete input/output cycle of 0,924 ms will occur.

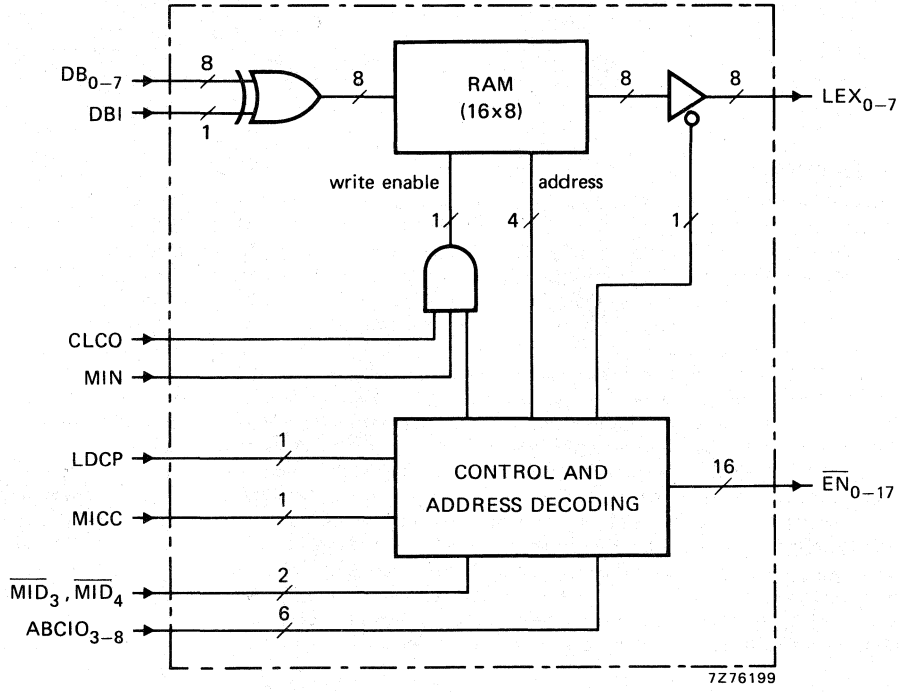


Fig. 1.

Truth Table

data inputs DB_0 to DB_7	data input DBI	data ouput LEX_0 to LEX_7
active	active	0
non-active	active	1
active	non-active	1
non-active	non-active	0

ELECTRICAL DATA

Supply

Logic supply voltage (d.c.)	V_P	5 V ± 5%
Logic supply current (d.c.)	I_P	max. 0,7 A typ. 0,6 A
Supply voltage (d.c.) to drive enable outputs		5 V ± 5% 24 V ± 25%
Supply current (d.c.) to drive enable outputs		max. 3 mA typ. 2,5 mA

Input data

The data inputs are DB_0 to DB_7 and DBI. They are accessible on connector 2 (see "Terminal location" and Fig. 2 for connection).

	5 V level	24 V level
Active voltage (V_{a-c})*	3,5 to 6 V	18 to 30 V
Non-active voltage (V_{a-c})*	0 to 0,8 V	0 to 0,8 V
Input current, active at V_{a-c} = 5 V or 24 V resp.	typ. 10 mA	typ. 10 mA

Connector 2

row a, terminals 1, 3, 5, 7, 9, 11, 13, 15, 17

row a, terminals 2, 4, 6, 8, 10, 12, 14, 16, 18

row c, terminals (1,2), (3,4), (5,6), (7,8), (9,10), (11,12), (13,14), (15,16), (17,18)

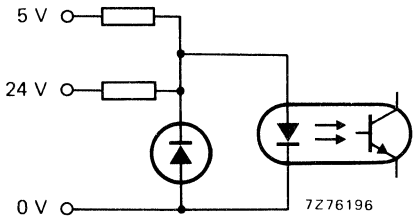


Fig. 2 Input circuit DB_0 to DB_7 and DBI.

All other inputs are connected to the CP10 and meet the standard TTL specification except the CLCO-input.

* Voltage between terminal of row a and terminal of row c of connector 2.

input	function	load	terminations (Fig. 4)	
			connector 1	connector 2
$ABCIO_3$	Address bits from central processor.	1 TTL	a8	
$ABCIO_4$		1 TTL	a10	
$ABCIO_5$		1 TTL	a12	
$ABCIO_6$		1 TTL	a14	
$ABCIO_7$		1 TTL	a16	
$ABCIO_8$		1 TTL	a18	
LDCP	Signal from central processor indicating the beginning of data processing cycle.	2 TTL	c15	
MICC	Signal from central processor; trailing edge indicates the end of the data processing cycle.	1 TTL	c5	
MIN	Module inhibit signal from external source; a LOW level applied to this input inhibits data on DB_0 to DB_7 to be stored in the RAM on the LX10.	2 TTL	c26	
$\overline{MID}_3$	Module identification inputs.	2 TTL	c16	
$\overline{MID}_4$		2 TTL	c18	
CLCO *	Clock signal from central processor.	*	a28	

* Input with relatively high input resistance (typ. 40 kΩ).
CLCO-input, LOW level: max. 1 V;
HIGH level: min. 2,4 V.

Output data

The enable outputs are $\overline{EN}_0$ to $\overline{EN}_{17}$; they are open-collector outputs.

Output voltage LOW, with respect to COMMON
at $I_{\overline{EN}}$ = 80 mA $\leqslant$ 0,5 V

Output voltage HIGH $\leqslant$ 30 V

output	function	loadability	terminations (Fig. 4)	
			connector 1	connector 2
LEX_0	Data outputs to be connected to LEX_0 to LEX_7 inputs of CP10.	10 TTL	a7	
LEX_1		10 TTL	c7	
LEX_2		10 TTL	a9	
LEX_3		10 TTL	c9	
LEX_4		10 TTL	a11	
LEX_5		10 TTL	c11	
LEX_6		10 TTL	a13	
LEX_7		10 TTL	c13	
IDLC	Identification signal from the LX10 to the CP10. This connection forces a complete input/output cycle. This terminal is direct connected to 0 V on the LX10.		a25	

Time data

Time that a data source is enabled
when CP10 is used with non-extended input/output cycle t_{en} 58 μs

when CP10 is used with extended input/output cycle t_{en} 14,8 ms

Time that data have to be present on DB_0 to DB_7 before end of enable signal
with non-extended input/output cycle t_{ds} 12 μs
with extended input/output cycle t_{ds} 2 ms

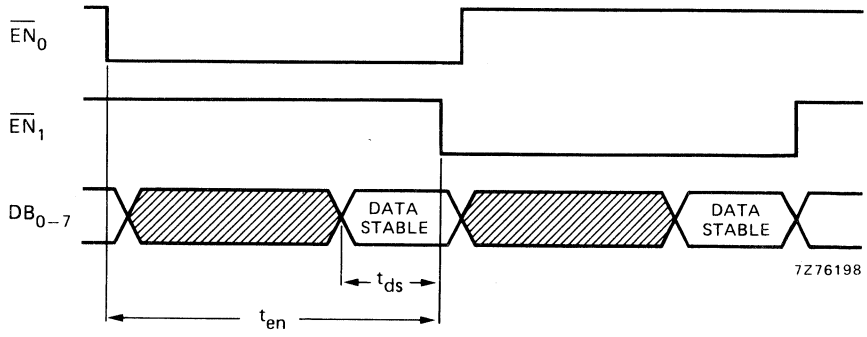


Fig. 3.

MECHANICAL DATA

Dimensions in mm

Outlines

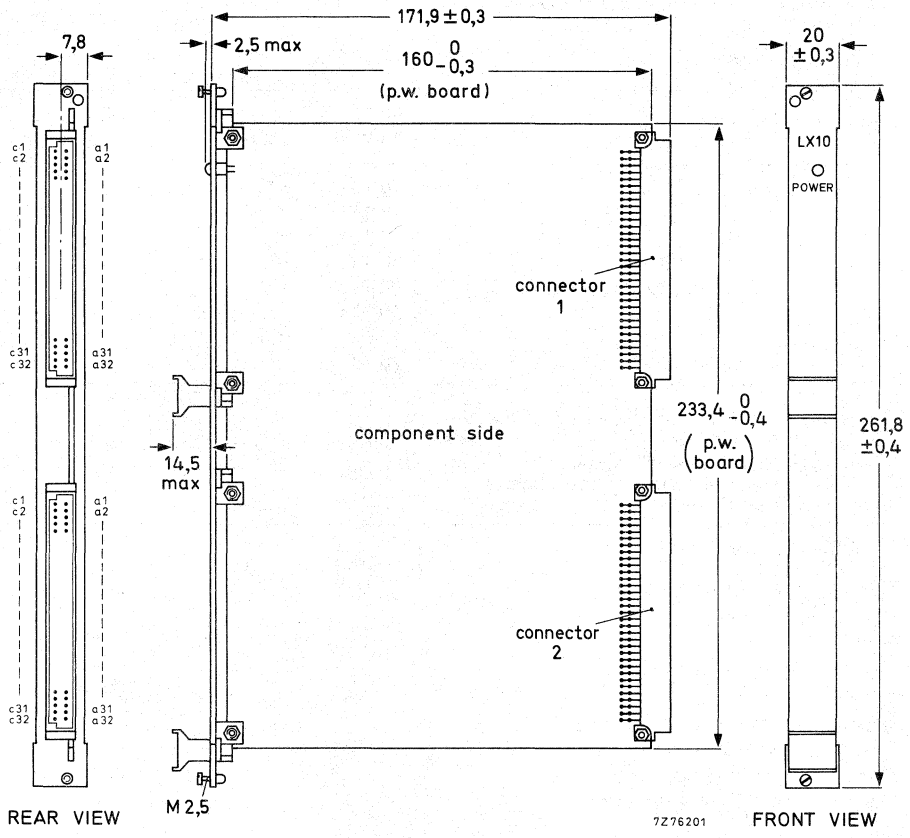


Fig. 4.

Mass 270 g

Terminal location

connector 1					connector 2				
	row c		row a			row c		row a	
	n.c.	1	n.c.		(note 4) DB0	1	DB0	(5 V)	
	n.c.	2	n.c.		(note 4) DB0	2	DB0	(24 V)	
	n.c.	3	n.c.		(note 4) DB1	3	DB1		
	n.c.	4	n.c.		(note 4) DB1	4	DB1		
	MICC	5	n.c.		(note 4) DB2	5	DB2		
	n.c.	6	n.c.		(note 4) DB2	6	DB2		
	LEX_1	7	LEX_0		(note 4) DB3	7	DB3		
	n.c.	8	$ABCIO_3$		(note 4) DB3	8	DB3		
	LEX_3	9	LEX_2		(note 4) DB4	9	DB4		
	n.c.	10	$ABCIO_4$		(note 4) DB4	10	DB4		
	LEX_5	11	LEX_4		(note 4) DB5	11	DB5		
	n.c.	12	$ABCIO_5$		(note 4) DB5	12	DB5		
	LEX_7	13	LEX_6		(note 4) DB6	13	DB6		
	n.c.	14	$ABCIO_6$		(note 4) DB6	14	DB6		
	LDCP	15	n.c.		(note 4) DB7	15	DB7		
	$\overline{MID}_3$	16	$ABCIO_7$		(note 4) DB7	16	DB7		
	n.c.	17	n.c.		(note 4) DBI	17	DBI	(5 V)	
	$\overline{MID}_4$	18	$ABCIO_8$		(note 4) DBI	18	DBI	(24 V)	
	n.c.	19	n.c.		n.c.	19	n.c.		
	0 V (note 1)	20	n.c.		$\overline{EN}_0$	20	$\overline{EN}_1$		
	n.c.	21	n.c.		$\overline{EN}_2$	21	$\overline{EN}_3$		
	0 V (note 1)	22	n.c.		$\overline{EN}_4$	22	$\overline{EN}_5$		
	n.c.	23	n.c.		$\overline{EN}_6$	23	$\overline{EN}_7$		
	n.c.	24	n.c.		$\overline{EN}_{10}$	24	$\overline{EN}_{11}$		
	n.c.	25	IDLC		$\overline{EN}_{12}$	25	$\overline{EN}_{13}$		
	MIN	26	n.c.		$\overline{EN}_{14}$	26	$\overline{EN}_{15}$		
	n.c.	27	n.c.		$\overline{EN}_{16}$	27	$\overline{EN}_{17}$		
	0 V (note 2)	28	CLCO		n.c.	28	n.c.		
	n.c.	29	n.c.		n.c.	29	n.c.		
	n.c.	30	n.c.		24 V	30	24 V		
(note 3)	5 V	31	5 V	(note 3)	(note 5) 5 V	31	5 V		(note 5)
	0 V	32	0 V		COMMON	32	COMMON		

n.c. = not connected

Notes
1. No supply line; only to be used for coding of the $\overline{MID}_{3,4}$ lines.
2. No supply line; only to be used as a ground connection for CLCO.
3. Logic supply.
4. Interconnected.
5. Enable output drive.

MEMORY MODULE

DESCRIPTION

This memory module is intended for use in combination with the central processor CP10 (or CP11), input module IM10, output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC). The control program is stored in the memory module.

The memory module is a random access magnetic core memory system with a basic capacity of 1024 words of 13 bits (1 k 13) and a cycle time of 1 µs. The memory is complete in itself; it consists of a 3 D, 3-wire stack, timing selecting and inhibit circuitry, address and data registers, and a memory retention circuit including the 5 V sensing.

The memory module is built on three epoxy-glass printed-wiring boards. The module is provided with two F068-1 connectors (board parts, Euro-card system); the corresponding panel parts are available under catalogue number 2422 025 89288 (pins for wire wrap), 2422 025 89298 (pins for dip soldering) or 2422 025 89326 (solder tags) [1]).

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	5 V ± 5%	
current (cycle time 1,8 µs)	I_P	operating	max. 5,1 A
			typ. 4 A
		standby	max. 3,6 A
			typ. 3,3 A

Note: The memory is in standby position when ENCM is LOW.

Cooling

An air velocity of 0,2 m/s is required.

[1]) For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19 in racks and IEC 130-14 or DIN 41612 for connectors.

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig. 3) connector 1	connector 2
CICM	Cycle initiate signal from central processor to program memory (bipolar to reduce noise sensitivity).	1 TTL		a19, c19
$\overline{\text{CICM}}$		1 TTL		a18, c18
SCCM	Store command from central processor; determines read/restore and clear/write cycle.	2 TTL		a17, c17
$ABCM_0$	Address bits from central processor.	2 TTL		a20, c20
$ABCM_1$		2 TTL		a21, c21
$ABCM_2$		2 TTL		a22, c22
$ABCM_3$		2 TTL		a23, c23
$ABCM_4$		2 TTL		a24, c24
$ABCM_5$		2 TTL		a25, c25
$ABCM_6$		2 TTL		a26, c26
$ABCM_7$		2 TTL		a27, c27
$ABCM_8$		2 TTL		a28, c28
$ABCM_9$		2 TTL		a29, c29
$ENCM_1$	Enable signal from central processor to select one out of four memory modules.	3 TTL	a1	
$ENCM_2$		3 TTL	a2	
$ENCM_3$		3 TTL	a3	
$ENCM_4$		3 TTL	a4	
$PBPM_0$	Program word bits from programming unit.	1 TTL	c1	
$PBPM_1$		1 TTL	c2	
$PBPM_2$		1 TTL	c3	
$PBPM_3$		1 TTL	c4	
$PBPM_4$		1 TTL	c5	
$PBPM_5$		1 TTL	c6	
$PBPM_6$		1 TTL	c7	
$PBPM_7$		1 TTL	c8	
$PBPM_8$		1 TTL	c9	
$PBPM_9$		1 TTL	c10	
$PBPM_{10}$		1 TTL	c11	
$PBPM_{11}$		1 TTL	c12	
$PBPM_{12}$		1 TTL	c13	
ENPB	Enables outputs $\overline{\text{PBMCP}}_0$-12; when LOW these outputs are enabled, when HIGH these outputs are disabled.	2 TTL	a6	

Output data

All outputs meet the standard TTL specifications.

output	function	loadability	terminations (Fig. 3) connector 1	terminations (Fig. 3) connector 2
$PBMCP_0$	Program word bits from program memory to central processor and programming unit. Open collector output with pull-up resistor (3,9 kΩ).	9 TTL		a2, c2
$PBMCP_1$		9 TTL		a3, c3
$PBMCP_2$		9 TTL		a4, c4
$PBMCP_3$		9 TTL		a5, c5
$PBMCP_4$		9 TTL		a6, c6
$PBMCP_5$		9 TTL		a7, c7
$PBMCP_6$		9 TTL		a8, c8
$PBMCP_7$		9 TTL		a9, c9
$PBMCP_8$		9 TTL		a10, c10
$PBMCP_9$		9 TTL		a11, c11
$PBMCP_{10}$		9 TTL		a12, c12
$PBMCP_{11}$		9 TTL		a13, c13
$PBMCP_{12}$		9 TTL		a14, c14
$\overline{PBMCP}_0$	Inverted $PBMCP_{0-12}$ enabled by ENPB (three-state outputs).	10TTL	c17	
$\overline{PBMCP}_1$		10TTL	c18	
$\overline{PBMCP}_2$		10TTL	c19	
$\overline{PBMCP}_3$		10TTL	c20	
$\overline{PBMCP}_4$		10TTL	c21	
$\overline{PBMCP}_5$		10TTL	c22	
$\overline{PBMCP}_6$		10TTL	c23	
$\overline{PBMCP}_7$		10TTL	c24	
$\overline{PBMCP}_8$		10TTL	c25	
$\overline{PBMCP}_9$		10TTL	c26	
$\overline{PBMCP}_{10}$		10TTL	c27	
$\overline{PBMCP}_{11}$		10TTL	c28	
$\overline{PBMCP}_{12}$		10TTL	c29	
DA	Data available signal. This signal becomes LOW max. 150 ns after CICM (or $\overline{CICM}$), and goes HIGH as soon as the data become available at the outputs (max. 500 ns after CICM or $\overline{CICM}$). Open collector output with pull-up resistor (3,9 kΩ).	9 TTL		a16, c16

Time data

The relationship between the different input and output signals are given when the memory module is operating in a programmable logic controller system.

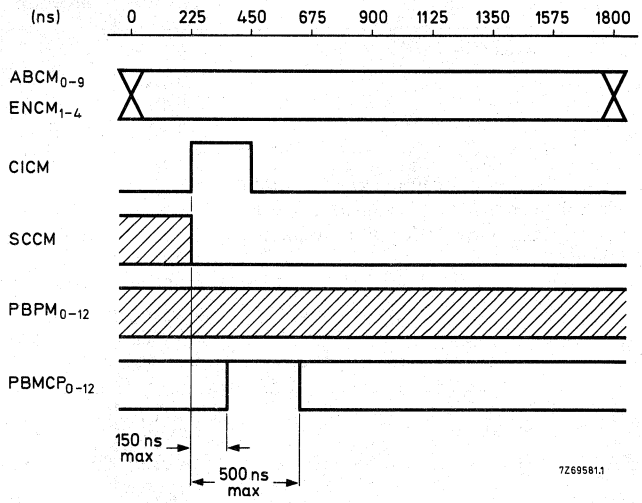


Fig. 1. Timing of read/restore mode.

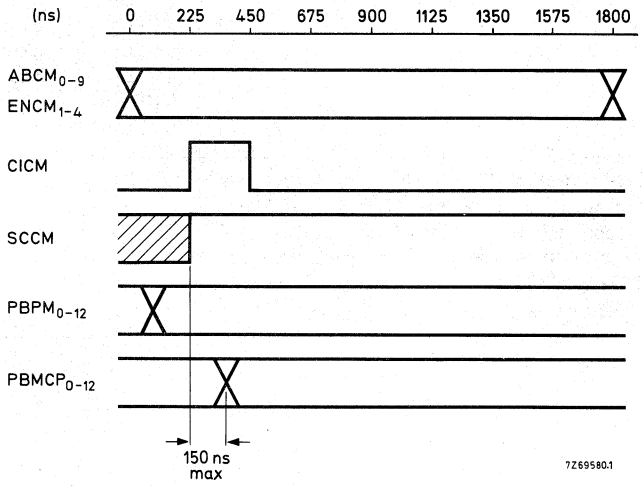


Fig. 2. Timing of clear/write mode.

MECHANICAL DATA

Dimensions in mm

Outlines

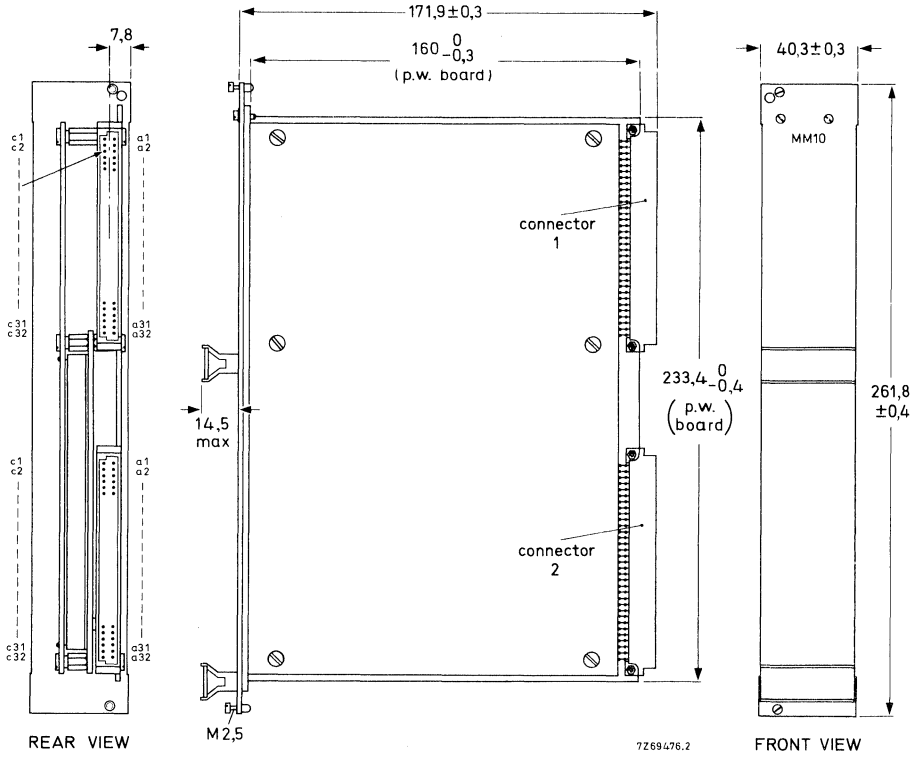


Fig. 3

Mass 780 g

Terminal location

connector 1

row c		row a
$PBPM_0$	1	$ENCM_1$
$PBPM_1$	2	$ENCM_2$
$PBPM_2$	3	$ENCM_3$
$PBPM_3$	4	$ENCM_4$
$PBPM_4$	5	n.c.
$PBPM_5$	6	ENPB
$PBPM_6$	7	n.c.
$PBPM_7$	8	n.c.
$PBPM_8$	9	n.c.
$PBPM_9$	10	n.c.
$PBPM_{10}$	11	n.c.
$PBPM_{11}$	12	n.c.
$PBPM_{12}$	13	n.c.
n.c.	14	n.c.
n.c.	15	n.c.
n.c.	16	n.c.
$\overline{PBMCP_0}$	17	n.c.
$\overline{PBMCP_1}$	18	n.c.
$\overline{PBMCP_2}$	19	n.c.
$\overline{PBMCP_3}$	20	n.c.
$\overline{PBMCP_4}$	21	n.c.
$\overline{PBMCP_5}$	22	n.c.
$\overline{PBMCP_6}$	23	n.c.
$\overline{PBMCP_7}$	24	n.c.
$\overline{PBMCP_8}$	25	n.c.
$\overline{PBMCP_9}$	26	n.c.
$\overline{PBMCP_{10}}$	27	n.c.
$\overline{PBMCP_{11}}$	28	n.c.
$\overline{PBMCP_{12}}$	29	n.c.
n.c.	30	n.c.
V_P	31	V_P
0 V	32	0 V

connector 2

row c		row a
n.c.	1	n.c.
$PBMCP_0$	2	$PBMCP_0$
$PBMCP_1$	3	$PBMCP_1$
$PBMCP_2$	4	$PBMCP_2$
$PBMCP_3$	5	$PBMCP_3$
$PBMCP_4$	6	$PBMCP_4$
$PBMCP_5$	7	$PBMCP_5$
$PBMCP_6$	8	$PBMCP_6$
$PBMCP_7$	9	$PBMCP_7$
$PBMCP_8$	10	$PBMCP_8$
$PBMCP_9$	11	$PBMCP_9$
$PBMCP_{10}$	12	$PBMCP_{10}$
$PBMCP_{11}$	13	$PBMCP_{11}$
$PBMCP_{12}$	14	$PBMCP_{12}$
i.c.	15	i.c.
DA	16	DA
$\overline{SCCM}$	17	$\overline{SCCM}$
CICM	18	CICM
CICM	19	CICM
$ABCM_0$	20	$ABCM_0$
$ABCM_1$	21	$ABCM_1$
$ABCM_2$	22	$ABCM_2$
$ABCM_3$	23	$ABCM_3$
$ABCM_4$	24	$ABCM_4$
$ABCM_5$	25	$ABCM_5$
$ABCM_6$	26	$ABCM_6$
$ABCM_7$	27	$ABCM_7$
$ABCM_8$	28	$ABCM_8$
$ABCM_9$	29	$ABCM_9$
i.c.	30	i.c.
V_P	31	V_P
0 V	32	0 V

n.c. = not connected.
i.c. = internal connection.

MEMORY MODULE

DESCRIPTION

The memory module MM11 is intended for use in the PLC system as a program memory or as an auxiliary unit for programming EPROMs (2708); see also Remark below. It contains 4 IC sockets in which 4 UV-erasable EPROMs can be plugged. The MM11 also contains an address buffer, output buffers, and 3 d.c./d.c. converters (5 V to 12 V, 5 V to −5 V and 5 V to 27 V).
The MM11 has three operation modes which can be selected by two mode-selection inputs MSI_1 and MSI_2 (see also truth table under "Input data"):

- Read mode (RD): the module can be used as a read only memory (ROM), that is the situation when the module is used in an operating PLC system.
- Write into master mode (WIM): data from MM10, MM11 or MM12* can program the EPROMs in the IC sockets.
- Write into RAM mode (WIR): the contents of the EPROMs on the MM11 can be written into an MM10*.

The last two modes will be started after pressing a push button, to be connected between terminal 24a of connector 1 and 0 V, or by applying a LOW level to that terminal.

When the MM11 is in the WIM mode the data flow will be as follows:

- the MM11 sends an address ($ABCM_0$ to $ABCM_9$), an enable signal ($ENCM_1$ or $ENCM_2$) and a cycle initiate signal (CICM/$\overline{CICM}$) to the data source which may be an MM10, MM11 or MM12 (the MM12 does not need a CICM signal);
- the data source will send the data to be programmed into the EPROMs on the MM11.

When the MM11 is in the WIR mode the data flow will be:

- the MM11 sends an address ($ABCM_0$ to $ABCM_9$), an enable signal ($ENCM_1$ or $ENCM_2$), a cycle initiate signal (CICM/$\overline{CICM}$) and a store command to the MM10;
- data from MM11 will go via $PBPM_0$ to $PBPM_{12}$ to the MM10 and be stored into the MM10.

The MM11 has a capacity of 1k13 or 2k13 depending on whether there are 2 or 4 EPROMs on the module.

The enable input $ENCM_1$ or $ENCM_3$ (addresses 0000 to 1777 and 4000 to 5777 respectively) corresponds with the EPROMs in sockets 1A and 1B. The enable input $ENCM_2$ or $ENCM_4$ (addresses 2000 to 3777 and 6000 to 7777 respectively) corresponds with the EPROMs in sockets 2A and 2B. This means that one program word is stored into 2 EPROMs, A and B, of which EPROMs A contain the instruction and the most significant digit of the address (address part of the program word), and EPROMs B contain the remaining two digits.

The MM11 is supplied with two empty EPROMs 2708.

Remark

Correct programming of EPROMs is only guaranteed, when completely erased EPROMs are used; for the correct erase procedure consult the relevant data sheet of the 2708 EPROMs.

* The connections between these modules have to be done in a separate module set-up, outside the system. No special programming apparatus is required.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	5 V ± 5%
Supply current	I_P	max. 2,4 A typ. 2 A

Remark

There are several terminals on the connectors which act as inputs or outputs depending on the mode in which the MM11 is operating (see below). These terminals are described under "Input data" and "Output data".

terminal	operation mode		
	WIM	WIR	RD
CICM/$\overline{\text{CICM}}$	output	output	input
$ENCM_1$ to $ENCM_4$	output	output	input
$ABCM_0$ to $ABCM_9$	output	output	input
$PBMCP_0$ to $PBMCP_{12}$	input	output	output

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig.1)	
			connector 1	connector 2
$ABCM_0$	Address inputs (RD mode).	1 TTL		a20, c20
$ABCM_1$		1 TTL		a21, c21
$ABCM_2$		1 TTL		a22, c22
$ABCM_3$		1 TTL		a23, c23
$ABCM_4$		1 TTL		a24, c24
$ABCM_5$		1 TTL		a25, c25
$ABCM_6$		1 TTL		a26, c26
$ABCM_7$		1 TTL		a27, c27
$ABCM_8$		1 TTL		a28, c28
$ABCM_9$		1 TTL		a29, c29
CICM	Cycle initiate signal; bipolar to reduce noise sensitivity (RD mode).	2 TTL		a19, c19
$\overline{\text{CICM}}$		2 TTL		a18, c18
$ENCM_1$	Enable inputs; memory is enabled when ENCM is HIGH (RD mode).	2 TTL	a1	
$ENCM_2$		2 TTL	a2	
$ENCM_3$		2 TTL	a3	
$ENCM_4$		2 TTL	a4	
$PBMCP_0$	Data inputs for data to be programmed into the EPROMs (WIM mode).	1 TTL		a2, c2
$PBMCP_1$		1 TTL		a3, c3
$PBMCP_2$		1 TTL		a4, c4
$PBMCP_3$		1 TTL		a5, c5
$PBMCP_4$		1 TTL		a6, c6
$PBMCP_5$		1 TTL		a7, c7

input	function	load	terminations (Fig.1)	
			connector 1	connector 2
$PBMCP_6$	Data inputs for data to be programmed into the EPROMs (WIM mode).	1 TTL		a8, c8
$PBMCP_7$		1 TTL		a9, c9
$PBMCP_8$		1 TTL		a10, c10
$PBMCP_9$		1 TTL		a11, c11
$PBMCP_{10}$		1 TTL		a12, c12
$PBMCP_{11}$		1TTL		a13, c13
$PBMCP_{12}$		1 TTL		a14, c14
START	Input to start the WIM or the WIR mode (active LOW).	2 TTL	a24	
REST	Input to restart the stopped WIM or WIR mode (active LOW)	1 TTL	a19	
INH	Inhibit and stop input; when LOW the start input is inoperative.	2 TTL	a25	
MSI_1	Mode selection inputs.	6 TTL	a26	
MSI_2		6 TTL	a27	

Operation mode truth table

mode	mode selection inputs	
	MSI_1	MSI_2
RD	HIGH (floating)	HIGH (floating)
WIM	active LOW	arbitrary level
WIR	HIGH (floating)	active LOW

Output data

All outputs meet the standard TTL specifications.

output	function	loadability	terminations (Fig.1)	
			connector 1	connector 2
$PBMCP_0$	Program word bits to central processor (RD mode) or MM10 (WIR mode).	10 TTL		a2, c2
$PBMCP_1$		10 TTL		a3, c3
$PBMCP_2$		10 TTL		a4, c4
$PBMCP_3$		10 TTL		a5, c5
$PBMCP_4$		10 TTL		a6, c6
$PBMCP_5$		10 TTL		a7, c7
$PBMCP_6$		10 TTL		a8, c8
$PBMCP_7$		10 TTL		a9, c9
$PBMCP_8$		10 TTL		a10, c10
$PBMCP_9$		10 TTL		a11, c11
$PBMCP_{10}$		10 TTL		a12, c12
$PBMCP_{11}$		10 TTL		a13, c13
$PBMCP_{12}$		10 TTL		a14, c14
$ABCM_0$	Address bits to MM10, MM11 or MM12 (WIM mode) or to MM10 (WIR mode).	10 TTL		a20, c20
$ABCM_1$		10 TTL		a21, c21
$ABCM_2$		10 TTL		a22, c22
$ABCM_3$		10 TTL		a23, c23
$ABCM_4$		10 TTL		a24, c24
$ABCM_5$		10 TTL		a25, c25
$ABCM_6$		10 TTL		a26, c26
$ABCM_7$		10 TTL		a27, c27
$ABCM_8$		10 TTL		a28, c28
$ABCM_9$		10 TTL		a29, c29
$\overline{CICM}$	Cycle initiate signal to MM10 or MM11 (WIM mode) or to MM10 (WIR mode).	9 TTL		a19, c19
CICM		9 TTL		a18, c18
SCCM	Read-write output (three-state) to MM10. The output is LOW in the WIM mode, HIGH in the WIR mode, floating in the RD mode.	10 TTL		a17, c17
$ENCM_1$	Enable signal to MM10, MM11 or MM12 (WIM mode) or to MM10 (WIR mode).	9 TTL	a1	
$ENCM_2$		9 TTL	a2	
$ENCM_3$		9 TTL	a3	
$ENCM_4$		9 TTL	a4	
PRB	Program busy output signal to external equipment. When LOW it indicates that WIM mode or WIR mode is active and becomes HIGH as soon as these actions are finished.	10 TTL	a23	

output	function	loadability	terminations (Fig.1)	
			connector 1	connector 2
$PBPM_0$		10 TTL	c1	
$PBPM_1$		10 TTL	c2	
$PBPM_2$		10 TTL	c3	
$PBPM_3$		10 TTL	c4	
$PBPM_4$		10 TTL	c5	
$PBPM_5$		10 TTL	c6	
$PBPM_6$	Program word bits to MM10 (WIR mode).	10 TTL	c7	
$PBPM_7$	These three-state outputs are only	10 TTL	c8	
$PBPM_8$	active in the WIR mode.	10 TTL	c9	
$PBPM_9$		10 TTL	c10	
$PBPM_{10}$		10 TTL	c11	
$PBPM_{11}$		10 TTL	c12	
$PBPM_{12}$		10 TTL	c13	

Time data

RD mode

Time between leading edges of CICM/$\overline{\text{CICM}}$ and data valid $PBMCP_0$ to $PBMCP_{12}$ — max. 550 ns

Time between address changes on $ABCM_0$ to $ABCM_9$ and leading edges of CICM/$\overline{\text{CICM}}$ — min. 0 ns

WIM mode

Time to program 1k or 2k EPROM memory — max. 18 min, typ. 15 min

WIR mode

Time to read-out MM11 and store into MM10 — max. 4,2 s, typ. 3,5 s

MECHANICAL DATA

Dimensions in mm

Outlines

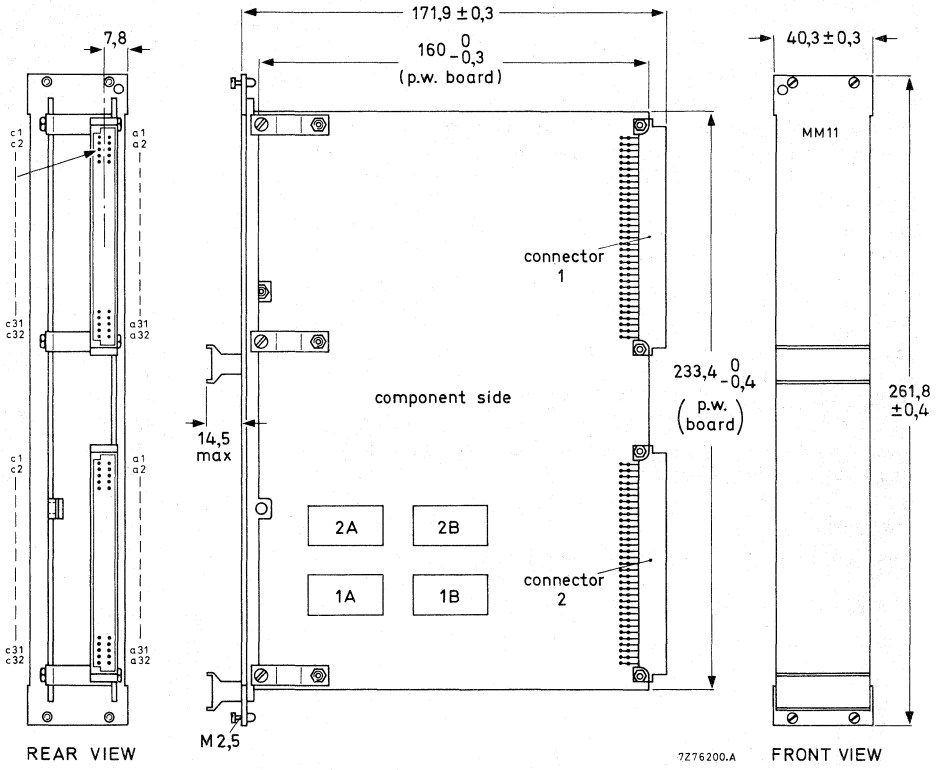


Fig.1.

Mass 350 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
$PBPM_0$	1	$ENCM_1$	n.c.	1	n.c.
$PBPM_1$	2	$ENCM_2$	$PBMCP_0$	2	$PBMCP_0$ (O_{5A}*)
$PBPM_2$	3	$ENCM_3$	$PBMCP_1$	3	$PBMCP_1$ (O_{6A})
$PBPM_3$	4	$ENCM_4$	$PBMCP_2$	4	$PBMCP_2$ (O_{7A})
$PBPM_4$	5	n.c.	$PBMCP_3$	5	$PBMCP_3$ (O_{8A})
$PBPM_5$	6	n.c.	$PBMCP_4$	6	$PBMCP_4$ (O_{1B})
$PBPM_6$	7	n.c.	$PBMCP_5$	7	$PBMCP_5$ (O_{2B})
$PBPM_7$	8	n.c.	$PBMCP_6$	8	$PBMCP_6$ (O_{3B})
$PBPM_8$	9	n.c.	$PBMCP_7$	9	$PBMCP_7$ (O_{5B})
$PBPM_9$	10	n.c.	$PBMCP_8$	10	$PBMCP_8$ (O_{6B})
$PBPM_{10}$	11	n.c.	$PBMCP_9$	11	$PBMCP_9$ (O_{7B})
$PBPM_{11}$	12	n.c.	$PBMCP_{10}$	12	$PBMCP_{10}$ (O_{1A})
$PBPM_{12}$	13	n.c.	$PBMCP_{11}$	13	$PBMCP_{11}$ (O_{2A})
n.c.	14	n.c.	$PBMCP_{12}$	14	$PBMCP_{12}$ (O_{3A})
n.c.	15	n.c.	n.c.	15	n.c.
n.c.	16	n.c.	n.c.	16	n.c.
n.c.	17	n.c.	$\overline{SCCM}$	17	$\overline{SCCM}$
n.c.	18	n.c.	$\overline{CICM}$	18	$\overline{CICM}$
n.c.	19	REST	CICM	19	CICM
n.c.	20	n.c.	$ABCM_0$	20	$ABCM_0$
n.c.	21	n.c.	$ABCM_1$	21	$ABCM_1$
n.c.	22	n.c.	$ABCM_2$	22	$ABCM_2$
n.c.	23	PRB	$ABCM_3$	23	$ABCM_3$
n.c.	24	START	$ABCM_4$	24	$ABCM_4$
n.c.	25	INH	$ABCM_5$	25	$ABCM_5$
n.c.	26	MSI_1	$ABCM_6$	26	$ABCM_6$
n.c.	27	MSI_2	$ABCM_7$	27	$ABCM_7$
n.c.	28	n.c.	$ABCM_8$	28	$ABCM_8$
n.c.	29	n.c.	$ABCM_9$	29	$ABCM_9$
n.c.	30	n.c.	n.c.	30	n.c.
V_P	31	V_P	V_P	31	V_P
0 V	32	0 V	0 V	32	0 V

n.c. = not connected

* Corresponding output number of EPROM.

MEMORY MODULE

DESCRIPTION

The memory module MM12 is intended for use in the PLC system as a program memory. It contains 4 IC sockets in which 4 UV-erasable PROMs (2708) can be plugged. The MM12 also contains 10 buffered address inputs, 4 enable inputs, 16 buffered outputs and 2 d.c./d.c. converters (5 V to 12 V and 5 V to −5 V).

The MM12 has a capacity of 2k16. Although the PLC system operates with program words of 13 bits, the remaining 3 bits are also brought out (Q_{4A}, Q_{4B}, Q_{8B}), so that the module can be used in other applications which require 16 bits.

The enable input $ENCM_1$ or $ENCM_3$ (addresses 0000 to 1777 and 4000 to 5777 respectively) corresponds with the EPROMs in sockets 1A and 1B. The enable input $ENCM_2$ or $ENCM_4$ (addresses 2000 to 3777 and 6000 to 7777 respectively) corresponds with the EPROMs in sockets 2A and 2B. This means that one program word is stored into 2 EPROMs, A and B, of which EPROMs A contain the instruction and the most significant digit of the address (address part of the program word), and EPROMs B contain the remaining two digits.

Programming of the EPROMs cannot be done on the MM12: this has to be done on the MM11or by existing programming equipment.

The MM12 is supplied with two empty EPROMs 2708.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	5 V ± 5%
Supply current	I_P	max. 1,2 A typ. 1 A

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig. 2)	
			connector 1	connector 2
$ABCM_0$	Address bits from central processor	1 TTL		a20, c20
$ABCM_1$		1 TTL		a21, c21
$ABCM_2$		1 TTL		a22, c22
$ABCM_3$		1 TTL		a23, c23
$ABCM_4$		1 TTL		a24, c24
$ABCM_5$		1 TTL		a25, c25
$ABCM_6$		1 TTL		a26, c26
$ABCM_7$		1 TTL		a27, c27
$ABCM_8$		1 TTL		a28, c28
$ABCM_9$		1 TTL		a29, c29
$ENCM_1$	Enable inputs from central processor	1 TTL	a1	
$ENCM_2$		1 TTL	a2	
$ENCM_3$		1 TTL	a3	
$ENCM_4$		1 TTL	a4	

Output data

All outputs are three-state outputs and meet the standard TTL specifications.

output	function	loada-bility	terminations (Fig. 2)	
			connector 1	connector 2
$PBMCP_0$	Program word bits from memory module to central processor	10 TTL		a2, c2
$PBMCP_1$		10 TTL		a3, c3
$PBMCP_2$		10 TTL		a4, c4
$PBMCP_3$		10 TTL		a5, c5
$PBMCP_4$		10 TTL		a6, c6
$PBMCP_5$		10 TTL		a7, c7
$PBMCP_6$		10 TTL		a8, c8
$PBMCP_7$		10 TTL		a9, c9
$PBMCP_8$		10 TTL		a10, c10
$PBMCP_9$		10 TTL		a11, c11
$PBMCP_{10}$		10 TTL		a12, c12
$PBMCP_{11}$		10 TTL		a13, c13
$PBMCP_{12}$		10 TTL		a14, c14
Q_{4A}	Buffered output from output O4 of EPROM A.	10 TTL		a1, c1
Q_{4B}	Buffered output from output O4 of EPROM B.	10 TTL		a15, c15
Q_{8B}	Buffered output from output O8 of EPROM B.	10 TTL		a16, c16

Time data

The relationship between the different input and output signals are given when the memory module is operating in the PLC system.

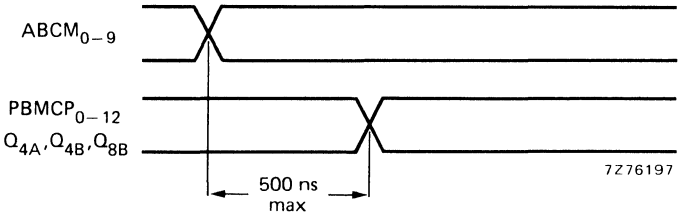


Fig. 1.

MECHANICAL DATA

Dimensions in mm

Outlines

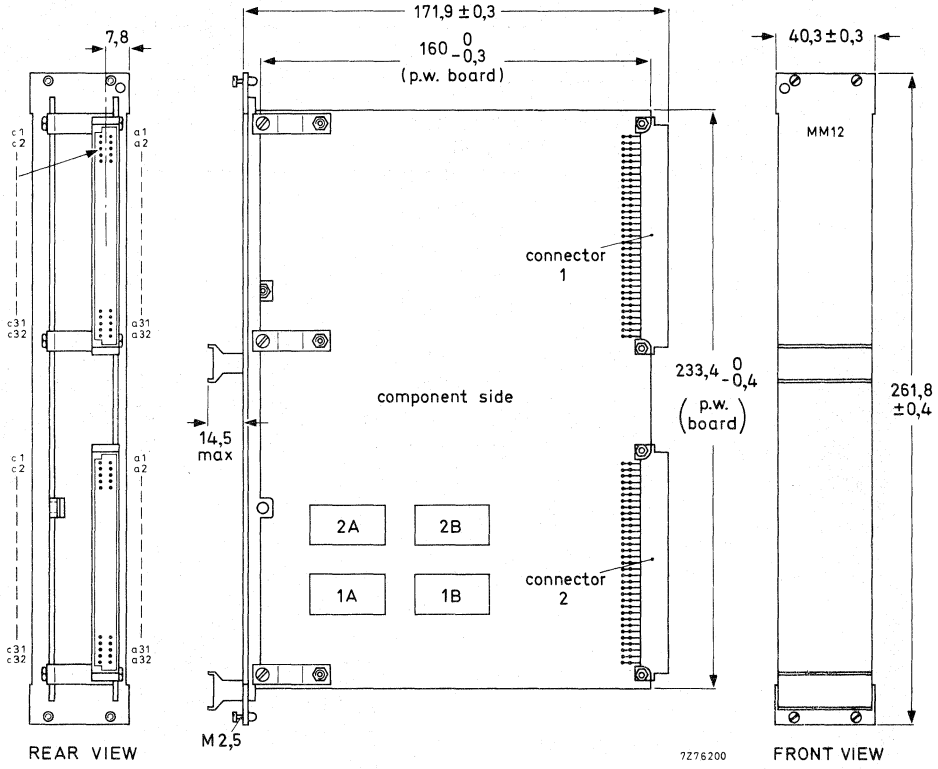


Fig. 2.

Mass 290 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
n.c.	1	$ENCM_1$	Q_{4A}	1	$Q_{4A}(O_{4A}*)$
n.c.	2	$ENCM_2$	$PBMCP_0$	2	$PBMCP_0(O_{5A})$
n.c.	3	$ENCM_3$	$PBMCP_1$	3	$PBMCP_1(O_{6A})$
n.c.	4	$ENCM_4$	$PBMCP_2$	4	$PBMCP_2(O_{7A})$
n.c.	5	n.c.	$PBMCP_3$	5	$PBMCP_3(O_{8A})$
n.c.	6	n.c.	$PBMCP_4$	6	$PBMCP_4(O_{1B})$
n.c.	7	n.c.	$PBMCP_5$	7	$PBMCP_5(O_{2B})$
n.c.	8	n.c.	$PBMCP_6$	8	$PBMCP_6(O_{3B})$
n.c.	9	n.c.	$PBMCP_7$	9	$PBMCP_7(O_{5B})$
n.c.	10	n.c.	$PBMCP_8$	10	$PBMCP_8(O_{6B})$
n.c.	11	n.c.	$PBMCP_9$	11	$PBMCP_9(O_{7B})$
n.c.	12	n.c.	$PBMCP_{10}$	12	$PBMCP_{10}(O_{1A})$
n.c.	13	n.c.	$PBMCP_{11}$	13	$PBMCP_{11}(O_{2A})$
n.c.	14	n.c.	$PBMCP_{12}$	14	$PBMCP_{12}(O_{3A})$
n.c.	15	n.c.	Q_{4B}	15	$Q_{4B}(O_{4B})$
n.c.	16	n.c.	Q_{8B}	16	$Q_{8B}(O_{8B})$
n.c.	17	n.c.	n.c.	17	n.c.
n.c.	18	n.c.	n.c.	18	n.c.
n.c.	19	n.c.	n.c.	19	n.c.
n.c.	20	n.c.	$ABCM_0$	20	$ABCM_0$
n.c.	21	n.c.	$ABCM_1$	21	$ABCM_1$
n.c.	22	n.c.	$ABCM_2$	22	$ABCM_2$
n.c.	23	n.c.	$ABCM_3$	23	$ABCM_3$
n.c.	24	n.c.	$ABCM_4$	24	$ABCM_4$
n.c.	25	n.c.	$ABCM_5$	25	$ABCM_5$
n.c.	26	n.c.	$ABCM_6$	26	$ABCM_6$
n.c.	27	n.c.	$ABCM_7$	27	$ABCM_7$
n.c.	28	n.c.	$ABCM_8$	28	$ABCM_8$
n.c.	29	n.c.	$ABCM_9$	29	$ABCM_9$
n.c.	30	n.c.	n.c.	30	n.c.
V_P	31	V_P	V_P	31	V_P
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

* Corresponding output number of EPROM.

OUTPUT MODULE

DESCRIPTION

The output module is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The output module contains 16 addressable output stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All outputs are floating with respect to each other.
Each output stage has a suppressor diode, to allow it to switch inductive loads.
Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

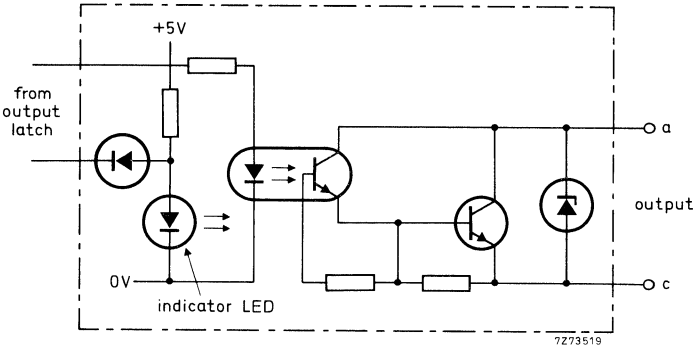


Fig. 1. Circuit diagram of an output stage.

The output module has nine address inputs ($ABCIO_{0-8}$) and five module identification inputs ($\overline{MID}_{0-4}$), which are accessible on the connectors at the rear (Fig. 2).

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card sytem). The board is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 2422 025 89291 (pins for wire wrap), 2422 025 89299 (pins for dip soldering) or 2422 025 89327 (solder tags) [1]).

[1]) For a general description of the Euro-card system see IEC297 or DIN41494 for 19-in racks and IEC 130-14 or DIN41612 for connectors.

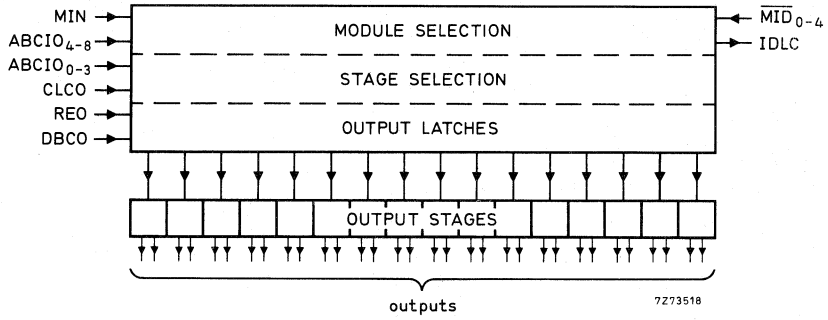


Fig. 2. Block diagram of the output module.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	5 V ± 5%
current	I_P	max. 1 A (all stages "ON")
		typ. 0,75 A (8 stages "ON", 8 stages "OFF")

Input data

All inputs meet the standard TTL specification except the CLCO-input.

input	function	load	terminations of connector 1 (Fig. 3)
$ABCIO_0$	Address bits from central processor; $ABCIO_{0-3}$ select the output stage, $ABCIO_{4-8}$ select the output module.	1 TTL	a2, c2
$ABCIO_1$		1 TTL	a4, c4
$ABCIO_2$		1 TTL	a6, c6
$ABCIO_3$		1 TTL	a8, c8
$ABCIO_4$		1 TTL	a10
$ABCIO_5$		1 TTL	a12
$ABCIO_6$		1 TTL	a14
$ABCIO_7$		1 TTL	a16
$ABCIO_8$		1 TTL	a18
DBCO	Data bit from central processor; data is stored in output stage by CLCO.	1 TTL	a22
MIN	Module inhibit signal from external source; a low level applied to this input inhibits data on DBCO to be stored in the output stage.	2 TTL	c26
REO	Reset output module line; a low level on this input will reset all output latches (output transistor non-conducting).	1 TTL	a24
$\overline{MID_0}$	Module identification inputs; provide module with individual identity.	2 TTL	c10
$\overline{MID_1}$		2 TTL	c12
$\overline{MID_2}$		2 TTL	c14
$\overline{MID_3}$		2 TTL	c16
$\overline{MID_4}$		2 TTL	c18
CLCO*	Clock signal from central processor to output module, stores data on DBCO into output stage during input/output cycle.	*	a28

*) Input with relatively high input resistance (typ. 40 kΩ).
CLCO-input, LOW level: max. 1 V;
HIGH level: min. 2,4 V.

Output data

The data outputs are DO_{XY0} to DO_{XY7} and DO_{XZ0} to DO_{XZ7}. They are accessible on connector 2, see "Terminal location".

Output transistor conducting : output current = max. 100 mA at V_{a-c}[1]) = max. 1,5 V

Output transistor non-conducting: output current = max. 10 µA at V_{a-c}[1]) = max. 30 V

Each data output has a suppressor diode, which allows the switching of loads with an inductance of max. 10 H.

[1]) Voltage between terminal of row a and terminal of row c of connector 2.

The output (open collector) below meets the standard TTL specifications.

output	function	loadability	terminations of connector 1 (Fig. 3)
IDLC	Identification signal from last output module to central processor (active HIGH); only the IDLC output of the last output module has to be connected with the IDLC input of the central processor.	2 TTL	a26

MECHANICAL DATA

Dimensions in mm

Outlines

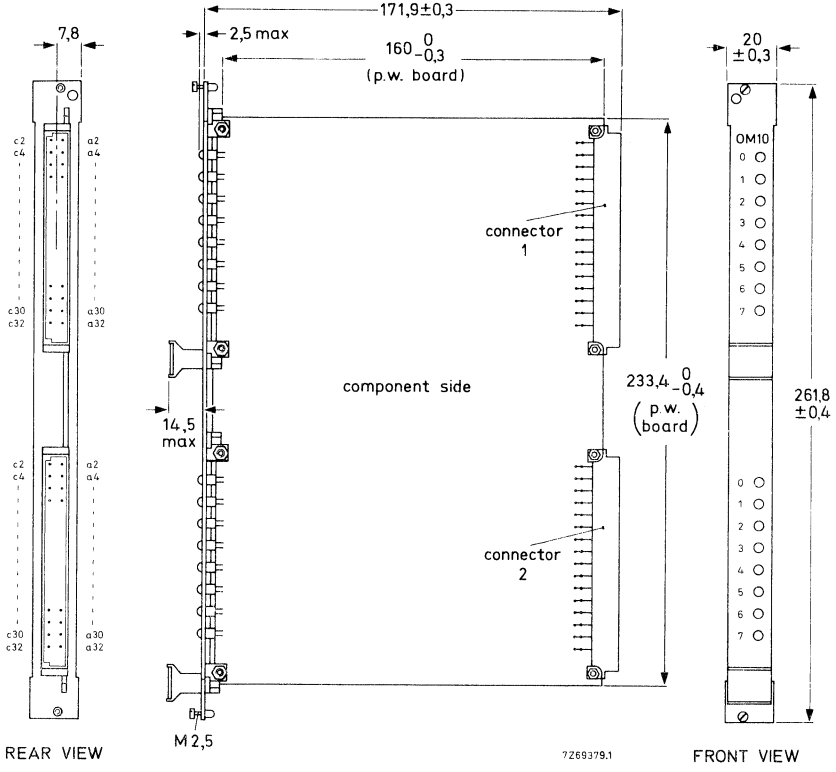


Fig. 3

Mass 230 g

Terminal location

connector 1

row c		row a
$ABCIO_0$	2	$ABCIO_0$
$ABCIO_1$	4	$ABCIO_1$
$ABCIO_2$	6	$ABCIO_2$
$ABCIO_3$	8	$ABCIO_3$
$\overline{MID_0}$	10	$ABCIO_4$
$\overline{MID_1}$	12	$ABCIO_5$
$\overline{MID_2}$	14	$ABCIO_6$
$\overline{MID_3}$	16	$ABCIO_7$
$\overline{MID_4}$	18	$ABCIO_8$
0V[1])	20	n.c.
0V[1])	22	DBCO
n.c.	24	REO
MIN	26	IDLC
0V[2])	28	CLCO
V_p	30	V_p
0V	32	0V

connector 2

row c		row a
DO_{XY0}	2	DO_{XY0}
DO_{XY1}	4	DO_{XY1}
DO_{XY2}	6	DO_{XY2}
DO_{XY3}	8	DO_{XY3}
DO_{XY4}	10	DO_{XY4}
DO_{XY5}	12	DO_{XY5}
DO_{XY6}	14	DO_{XY6}
DO_{XY7}	16	DO_{XY7}
DO_{XZ0}	18	DO_{XZ0}
DO_{XZ1}	20	DO_{XZ1}
DO_{XZ2}	22	DO_{XZ2}
DO_{XZ3}	24	DO_{XZ3}
DO_{XZ4}	26	DO_{XZ4}
DO_{XZ5}	28	DO_{XZ5}
DO_{XZ6}	30	DO_{XZ6}
DO_{XZ7}	32	DO_{XZ7}

n.c. = not connected.

[1]) No supply line; only to be used for coding of the $\overline{MID}_{0-4}$ lines.

[2]) No supply line; only to be used as a ground connection for CLCO.

OUTPUT MODULE

DESCRIPTION

The output module is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The output module contains 8 addressable output stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All outputs are open-collector outputs. Each output stage has a suppressor diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages feature electronic short-circuit protection which can only be de-activated by resetting the input signal. Short-circuit indication is provided by the lower row of LEDs on the front panel. If the status indicator LED and the short-circuit indicator LED with the same number are both lit, these output stages are working correctly. If the former LED is lit and the latter extinguished, this will indicate a short-circuit condition.

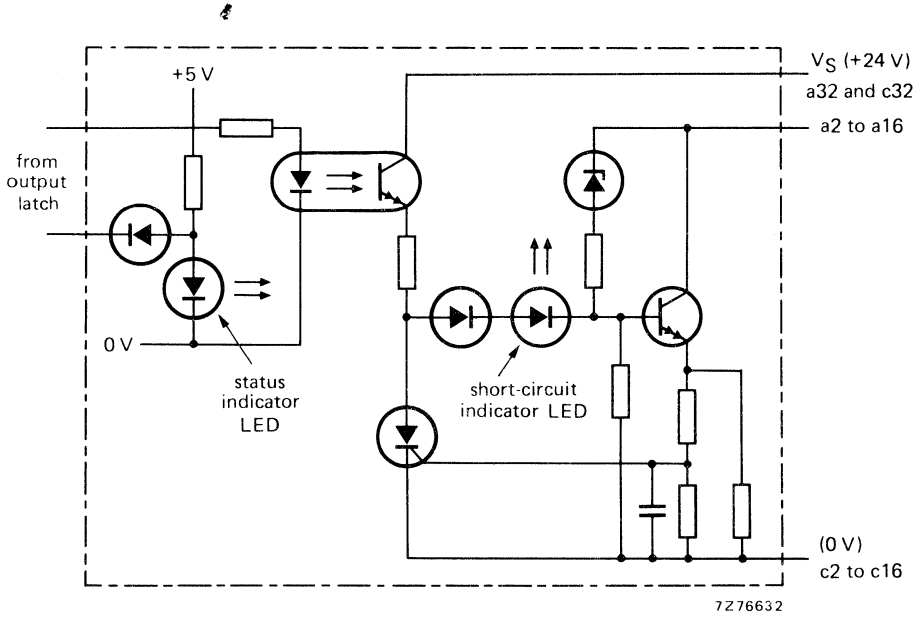


Fig. 1 Circuit diagram of an output stage.

The output module has 9 address inputs ($ABCIO_{0-8}$) and 5 module identification inputs ($\overline{MID}_{0-4}$) at the rear, for selecting 16 addresses. Because 8 are used as output stages (with even second digit e.g. 162), the remaining 8 addresses can be used as internal places (with odd second digit e.g. 172).

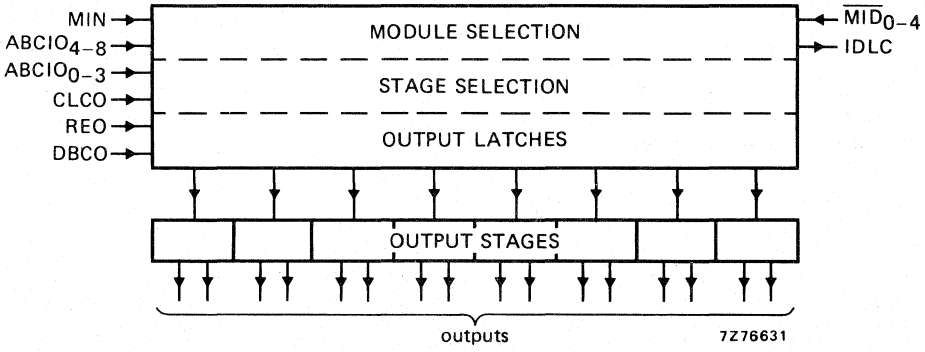


Fig.2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card system). The board is provided with two F068-I connectors (board parts), the corresponding panel parts are available too, but should be ordered additionally: 2422 025 89291 (with wire-wrap pins), 2422 025 89299 (with dip-solder pins), or 2422 025 89327 (with solder tags). For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130–14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	logic	V_P	5 V ± 5%
Supply current	logic	I_P	typ 0,75 A
Supply voltage (d.c.)	for output circuitry	V_S	24 V ± 25%
Supply current (excluding load current)	for output circuitry	I_S	typ 0,1 A

Input data

All inputs meet the standard TTL specification except the CLCO-input.

input	function	load	terminations of connector 1 (Fig.3)
$ABCIO_0$	address bits from central processor; $ABCIO_{0-3}$ select the output stage, $ABCIO_{4-8}$ select the output module.	1 TTL	a2, c2
$ABCIO_1$		1 TTL	a4, c4
$ABCIO_2$		1 TTL	a6, c6
$ABCIO_3$		1 TTL	a8, c8
$ABCIO_4$		1 TTL	a10
$ABCIO_5$		1 TTL	a12
$ABCIO_6$		1 TTL	a14
$ABCIO_7$		1 TTL	a16
$ABCIO_8$		1 TTL	a18
DBCO	Data bit from central processor; data are stored in output stage by CLCO.	1 TTL	a22
MIN	Module inhibit signal from external source; a low level applied to this input inhibits data on DBCO to be stored in the output stage.	2 TTL	c26
REO	Reset output module line; a low level on this input will reset all output latches (output transistor non-conducting).	1 TTL	a24
$\overline{MID}_0$	Module identification inputs; provide module with individual identity.	2 TTL	c10
$\overline{MID}_1$		2 TTL	c12
$\overline{MID}_2$		2 TTL	c14
$\overline{MID}_3$		2 TTL	c16
$\overline{MID}_4$		2 TTL	c18
CLCO *	Clock signal from central processor to output module, stores data on DBCO into output stage during input/output cycle.	*	a28

* Input with relatively high input resistance (typical 40 kΩ). CLCO-input: LOW level, maximum 1 V; HIGH level, minimum 2,4 V.

Output data

The data outputs are DO_{XY0} to DO_{XY7} (Y is always even). They are accessible on connector 2, see terminal location.
Output transistor conducting: $V_{a\text{-}c}$ * = max. 2,53 V at output current (I_O) is 2 A.
Output transistor non-conducting: I_O = max. 10 μA at $V_{a\text{-}c}$ * is 30 V.

Maximum load inductance (L_{max}) — see Table 1

Maximum switching frequency at maximum output current (I_{Omax}) — see Table 2

Table 1

I_O A	L_{max} mH
2,0	50
1,8	60
1,6	80
1,4	100
1,2	140
1,0	200
0,8	310
0,6	560
0,4	1300
0,2	5000
0,1	20000

Table 2

duty cycle %	max. switching frequency Hz
$\leqslant$ 40	3
$\leqslant$ 60	2
$\leqslant$ 80	1
$\leqslant$ 90	0,5

Output current at operation with forced air cooling of 1 m/s, for all stages — max. 2 A per stage

Output current at operation without forced air cooling
- for all stages — max. 0,915 A per stage
- for maximum 4 stages — max. 2 A per stage

Short-circuit protection trip level — 2,16 A

The output (open collector) meets the standard TTL specifications

output	function	loadability	terminations of connector 1 (Fig.3)
IDLC	Identification signal from last output module to central processor (active HIGH); only the IDLC output of the last output module has to be connected with the IDLC input of the central processor.	2 TTL	a26

* Voltage between terminal of row a and terminal of row c of connector 2.

MECHANICAL DATA

Dimensions in mm

Outlines

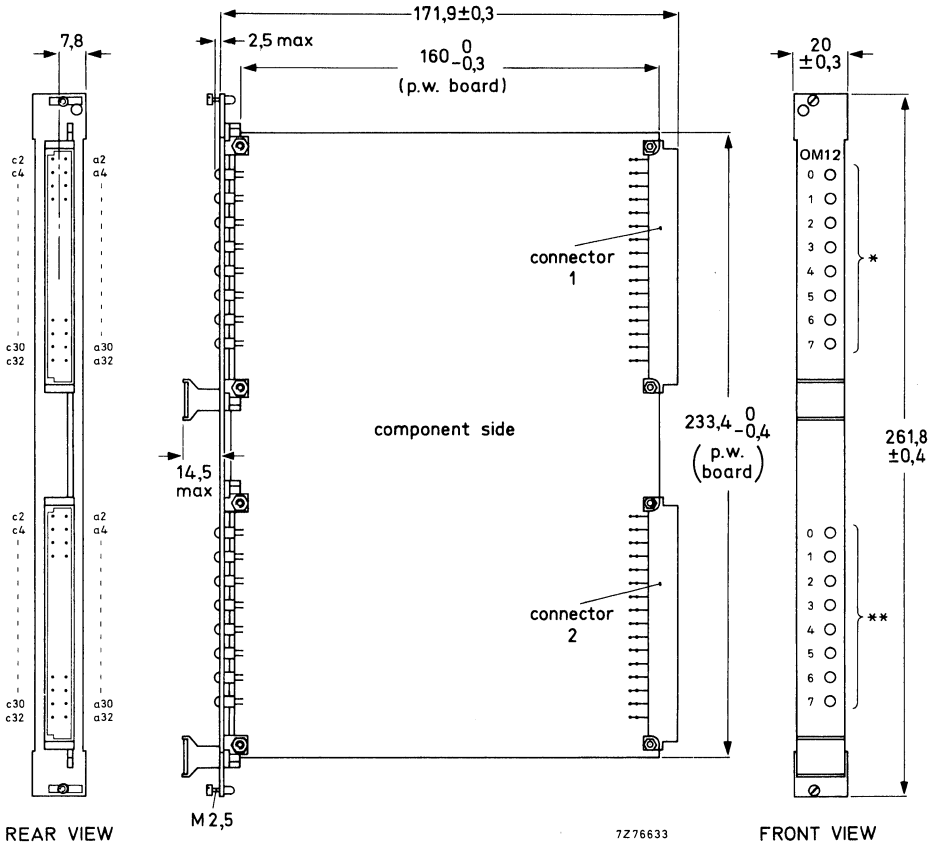


Fig.3 The LEDs identified with * are for status indication, those identified with ** are for short-circuit indication.

Mass 260 g

Terminal location

connector 1			connector 2			
row c		row a	row c			row a
$ABCIO_0$	2	$ABCIO_0$	0 V		2	DO_{XY0}
$ABCIO_1$	4	$ABCIO_1$	0 V		4	DO_{XY1}
$ABCIO_2$	6	$ABCIO_2$	0 V		6	DO_{XY2}
$ABCIO_3$	8	$ABCIO_3$	0 V	(note 3)	8	DO_{XY3}
$\overline{MID}_0$	10	$ABCIO_4$	0 V		10	DO_{XY4}
$\overline{MID}_1$	12	$ABCIO_5$	0 V		12	DO_{XY5}
$\overline{MID}_2$	14	$ABCIO_6$	0 V		14	DO_{XY6}
$\overline{MID}_3$	16	$ABCIO_7$	0 V		16	DO_{XY7}
$\overline{MID}_4$	18	$ABCIO_8$	i.c.		18	i.c.
0 V (note 1)	20	n.c.	i.c.		20	i.c.
0 V (note 1)	22	DBCO	i.c.		22	i.c.
n.c.	24	REO	n.c.		24	n.c.
MIN	26	IDLC	i.c.		26	n.c.
0 V (note 2)	28	CLCO	n.c.		28	n.c.
V_p	30	V_p	n.c.		30	n.c.
0 V	32	0 V	V_S		32	V_S

n.c. = not connected.
i.c. = internally connected.

Notes
1. No supply line; only to be used for coding of the $\overline{MID}_{0-4}$ lines.
2. No supply line; only to be used as a ground connection for CLCO.
3. 0-line of V_S.

PROGRAMMING UNIT

DESCRIPTION

The programming unit is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and output module OM10 (or OM12) to assemble a programmable logic controller (PLC). The control program is written into the program memory with the aid of this unit, by means of the built-in keyboard, or from a punched tape.
The unit can also be used to read the contents of the program memory: eight seven-segments LED displays show the program line number (memory address) and the program word belonging to it. Each program word contains a scratch-pad memory address; the content of this address (1 or 0) is indicated by the status indicator LED.

Programming a system by means of the keyboard (or a punched tape) is only possible when the key switch of the programming unit is set to the on position. The key switch determines the authority of the unit: with a key the user has the complete command of the PLC, without a key he can only monitor its actions.

The keyboard comprises 13 keys (Fig. 3):
- 9 keys, marked 0 to 7 and *, with which the program word is typed in;
- 1 key, marked ENTER; by pressing this key the displayed program word is transferred to the program memory. As soon as the key is released the program memory is set to the read mode; the programming unit reads the contents of the program memory and the program word is again displayed as a check that it is written correctly into the program memory.
- 1 key marked STEP; by pressing this key the next memory address is selected. Each time this key is pressed the line number is incremented by one.
- 1 key, marked CIRC, a repetitive STEP key; by pressing this key the line number is incremented continuously with a frequency of approx. 50 Hz.
- 1 key, marked DECR; by pressing this key simultaneously with either the STEP or CIRC keys, the line number is decremented by one or continuously respectively.

When the key switch is in the off position only the STEP, CIRC and DECR keys are operative. When selecting a particular address by means of these keys, the program word is displayed and the status of the scratch-pad memory address specified in the program word is indicated. In this way the PLC can be monitored without disrupting the working system.

If a punched tape is used, it must be coded according to the ASCII code. The characters to be used for the ENTER and the STEP commands are > and < respectively.

The unit is so constructed that it can be plugged into the PLC; after loading the program into the memory module the PU10 can be removed to be used in another PLC system.

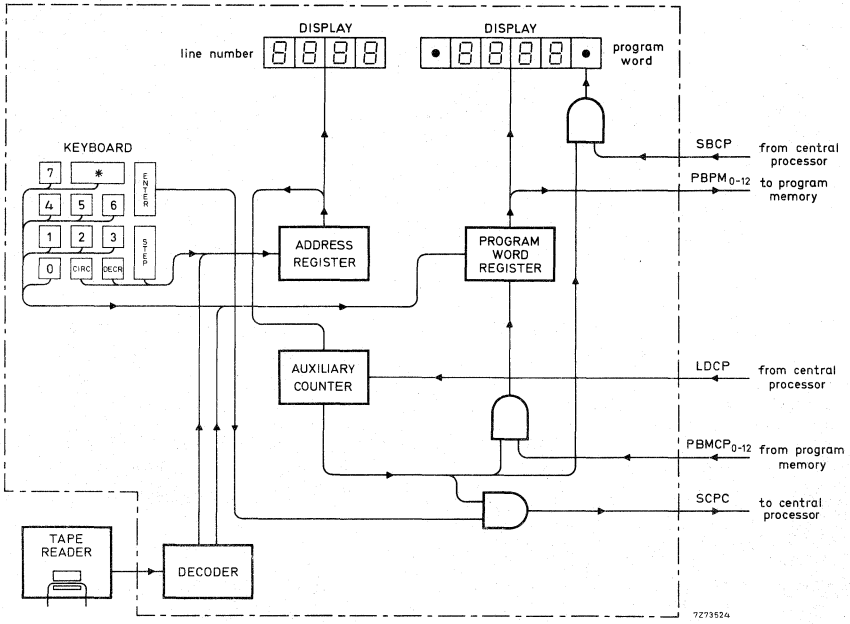


Fig. 1. Simplified block diagram of the programming unit.

The circuit is built on two epoxy-glass printed-wiring boards, mounted in a metal housing, which fits into the Euro-card system. The unit is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 2422 025 89291 (pins for wire wrap), 2422 025 89299 (pins for dip soldering) or 2422 025 89327 (solder tags) [1].

[1] For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_p	5 V ± 5%
current	I_p	max. 2 A
		typ. 1,8 A

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig. 2)	
			connector 1	connector 2
$PBMCP_0$	Program word bits from program memory.	1 TTL		c2
$PBMCP_1$		1 TTL		a2
$PBMCP_2$		1 TTL		c4
$PBMCP_3$		1 TTL		a4
$PBMCP_4$		1 TTL		c6
$PBMCP_5$		1 TTL		a6
$PBMCP_6$		1 TTL		c8
$PBMCP_7$		1 TTL		a8
$PBMCP_8$		1 TTL		c10
$PBMCP_9$		1 TTL		a10
$PBMCP_{10}$		1 TTL		c12
$PBMCP_{11}$		1 TTL		a12
$PBMCP_{12}$		1 TTL		c14
LDCP	Synchronization input from central processor; synchronizes auxiliary address counter in programming unit with address counter in central processor.	1 TTL	a14	
$\overline{CL}_{23}$	Inverted clock input from central processor.	1 TTL	c16	
ϕ_{57}	Clock signal for status indication from central processor.	1 TTL		c16
SBCP	Status bit from central processor; clocked by ϕ_{57} it indicates state 1 or 0 at selected scratch-pad memory address.	1 TTL	a16	
TB_1	Tape bits (ASCII code) from tape reader	2 TTL	c18	
TB_2			a18	
TB_3			c20	
TB_4			a20	
TB_5			c22	
TB_6			a22	
TB_7			c24	

input	function	load	terminations (Fig. 2)	
			connector 1	connector 2
STROBE	Signal from tape-reader sprocket.	2 TTL	a24	
SLTP	Selection signal from tape reader or external switch; if tape reader is used the input must be connected to the logic LOW level.	2 TTL	c28	

Output data

All outputs meet the standard TTL specifications.

output	function	loadability	terminations (Fig. 2)	
			connector 1	connector 2
$PBPM_0$	Program word bits to program memory.	9 TTL	c2	
$PBPM_1$		9 TTL	a2	
$PBPM_2$		9 TTL	c4	
$PBPM_3$		9 TTL	a4	
$PBPM_4$		9 TTL	c6	
$PBPM_5$		9 TTL	a6	
$PBPM_6$		9 TTL	c8	
$PBPM_7$		9 TTL	a8	
$PBPM_8$		9 TTL	c10	
$PBPM_9$		9 TTL	a10	
$PBPM_{10}$		9 TTL	c12	
$PBPM_{11}$		9 TTL	a12	
$PBPM_{12}$		9 TTL	c14	
$\overline{ABP}_0$	Inverted address bits (line number bits to external printer).	10 TTL		c18
$\overline{ABP}_1$		10 TTL		a18
$\overline{ABP}_2$		10 TTL		c20
$\overline{ABP}_3$		10 TTL		a20
$\overline{ABP}_4$		10 TTL		c22
$\overline{ABP}_5$		10 TTL		a22
$\overline{ABP}_6$		10 TTL		c24
$\overline{ABP}_7$		10 TTL		a24
$\overline{ABP}_8$		10 TTL		c26
$\overline{ABP}_9$		10 TTL		a26
$\overline{ABP}_{10}$		10 TTL		c28
$\overline{ABP}_{11}$		10 TTL		a28
READY	Signal indicating that contents of program memory address counter agrees with line number.	10 TTL		a16

output	function	loadability	terminations (Fig. 2)	
			connector 1	connector 2
SCPC	Store command to central processor.	10 TTL		a14
BSP	Busy signal to external tape reader; the output becomes LOW when a correct code has been recognized, and becomes HIGH when this code has been stored.	10 TTL	c26	
$\overline{BSP}$	Inverted BSP.	10 TTL	a26	

Time data

If a tape reader is used for loading the control program into the program memory the following considerations have to be taken in account.

Delay time between the level changes on TB_{1-7} and strobe signal	t_1	min.	0 ns
Delay time between leading edge of strobe pulse and code recognition on BSP	t_2	max.	500 ns
Strobe pulse duration	t_s	min.	2 µs
		max.	10 ms

BSP becomes LOW when a correct code has been recognized and HIGH when this code has been stored. At this moment the tape reader can be started to give the next code.

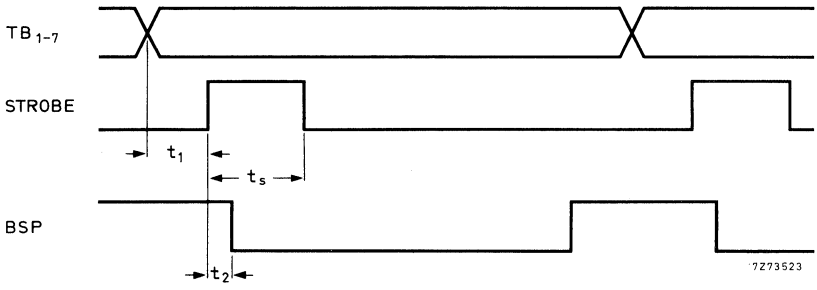


Fig. 2

MECHANICAL DATA

Dimensions in mm

Outlines

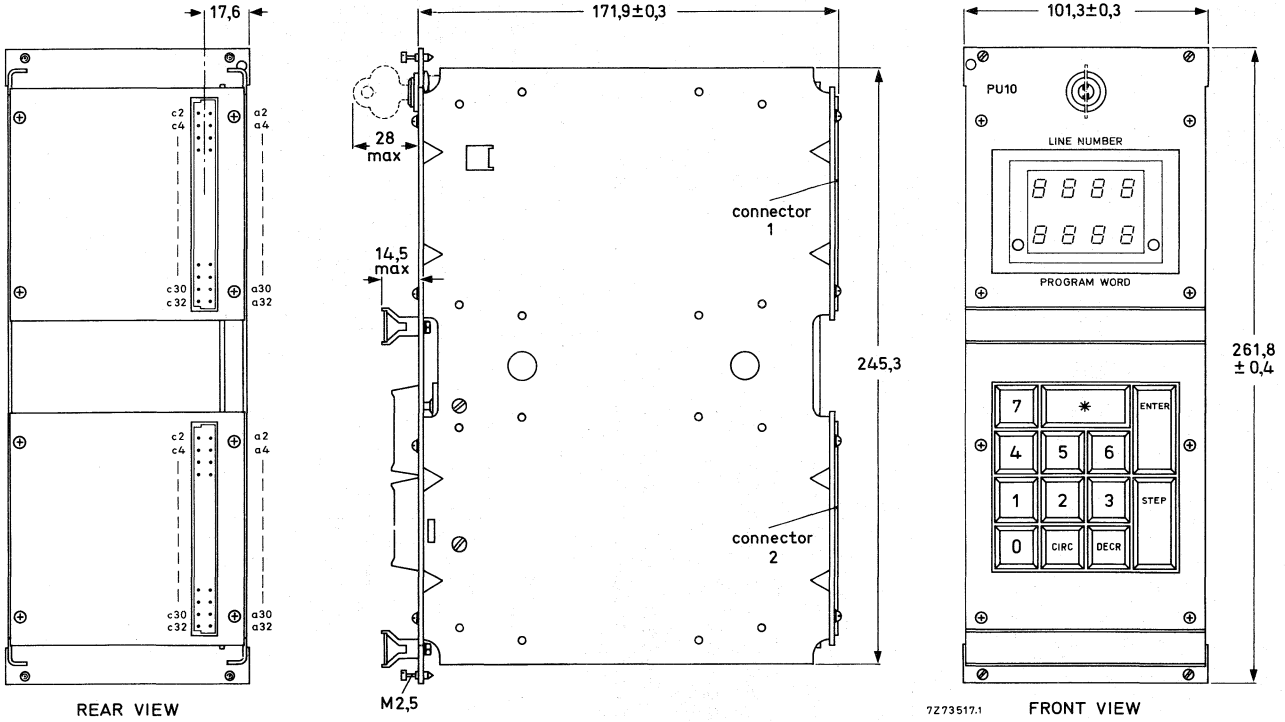


Fig. 3

Mass 1140 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
$PBPM_0$	2	$PBPM_1$	$PBMCP_0$	2	$PBMCP_1$
$PBPM_2$	4	$PBPM_3$	$PBMCP_2$	4	$PBMCP_3$
$PBPM_4$	6	$PBPM_5$	$PBMCP_4$	6	$PBMCP_5$
$PBPM_6$	8	$PBPM_7$	$PBMCP_6$	8	$PBMCP_7$
$PBPM_8$	10	$PBPM_9$	$PBMCP_8$	10	$PBMCP_9$
$PBPM_{10}$	12	$PBPM_{11}$	$PBMCP_{10}$	12	$PBMCP_{11}$
$\overline{PBPM}_{12}$	14	LDCP	$PBMCP_{12}$	14	SCPC
$\overline{CL}_{23}$	16	SBCP	ϕ_{57}	16	READY
TB_1	18	TB_2	$\overline{ABP}_0$	18	$\overline{ABP}_1$
TB_3	20	TB_4	$\overline{ABP}_2$	20	$\overline{ABP}_3$
TB_5	22	TB_6	$\overline{ABP}_4$	22	$\overline{ABP}_5$
TB_7	24	STROBE	$\overline{ABP}_6$	24	$\overline{ABP}_7$
BSP	26	$\overline{BSP}$	$\overline{ABP}_8$	26	$\overline{ABP}_9$
SLTP	28	n.c.	$\overline{ABP}_{10}$	28	$\overline{ABP}_{11}$
Vp	30	Vp	Vp	30	Vp
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

BACK PANELS

APPLICATION

Back panels BP11 to BP16 are designed for use as mother boards in 19-inch racks in the PLC system. Use of these panels removes the work of wiring separate connectors to receive the modules. The range avoids system redundancy and allows the rack space to be fully utilized.

DESCRIPTION

The back panels are equipped with female connectors, matching the male counterparts of the PLC modules. They have solder bridges for determining the addresses of an input/output/LX10 module (MID), the addresses of the MM modules (ENCM), the last IM/OM module or cycle time (IDLC), the last MM module (MICC), and connecting blocks for external connections.

Types BP11 to BP14 each consist of two back panels. The upper panel provides the required interconnections for connector 1 of each PLC module. The lower panel provides the interconnections for connector 2 of each MM, PU and CP module (see Figs 1 to 4). External connections are made to the lower connectors of the IM, OM and LX10 modules; these must be received by the separately mounted female connectors.

As the layout of the panels depends on the number of MM modules used, four different types have been developed. Table 1 surveys the various back panels and the type and number of each module which can be placed in the rack. Since a greater number of MM modules generally requires a greater number of IM/OM modules, need will be felt for an extension rack to accommodate these extra modules. Two back panel types are available for this purpose: the BP15 is for 15 IM/OM modules; the BP16 is for 21. These, of course, are only upper back panels.

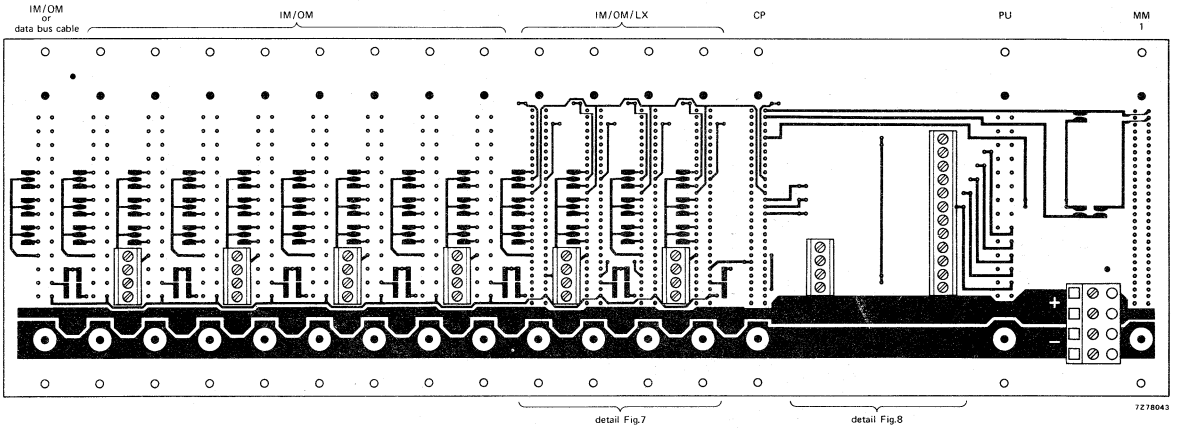
Table 1 Back panels

no. of MM modules	no. of IM/OM/LX* modules	no. of CP modules	no. of PU modules	type of back panel	catalogue number 9390 269 .....
1	13	1	1	BP11	30112
2	11	1	1	BP12	40112
3	9	1	1	BP13	50112
4	7	1	1	BP14	60112
–	15**	–	–	BP15	70112
–	21**	–	–	BP16	80112

The back panels are screwed to the rack by M2,5 screws, using threaded rails and isolation strips.

* A maximum of 4 LX modules can be inserted at positions IM/OM1 to IM/OM4. If an extension rack is used, one place in each rack must be reserved for data bus cable, thus the number of modules is one less than the number stated in this column.

** Back panels type BP15 and BP16 are extension panels for use in a second rack to accommodate additional IM/OM modules.



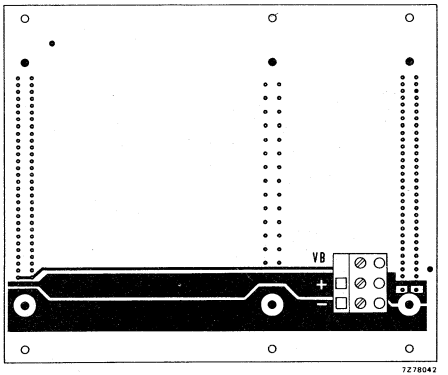
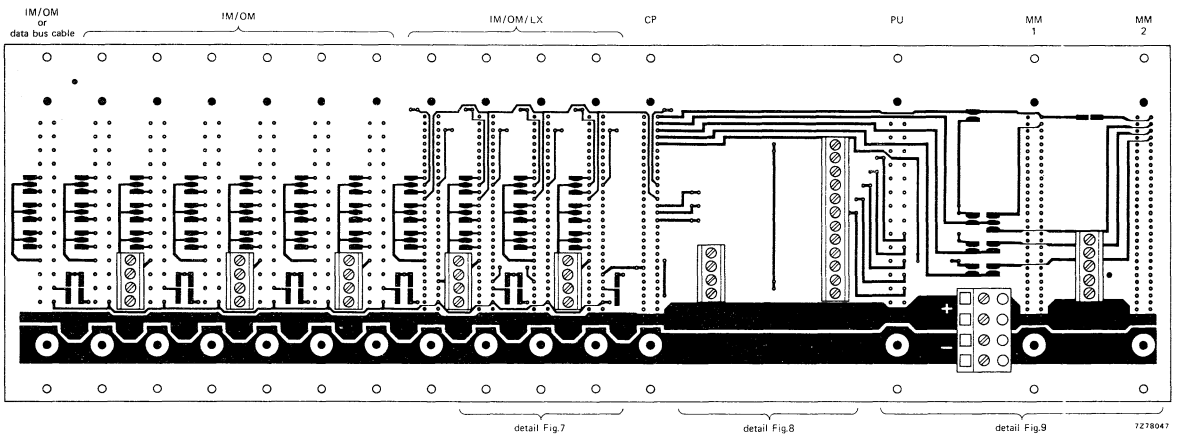


Fig. 1 Back panel BP11.

IM = input module
OM = output module
LX = load external interface module
CP = central processor
PU = programming unit
MM = program memory module
+ = +5 V ± 5%
– = 0 V
} supply voltage
V_B = +4,5 V to +7,5 V (battery voltage)
Data bus cable is only used for connecting a BP15 or BP16 panel.



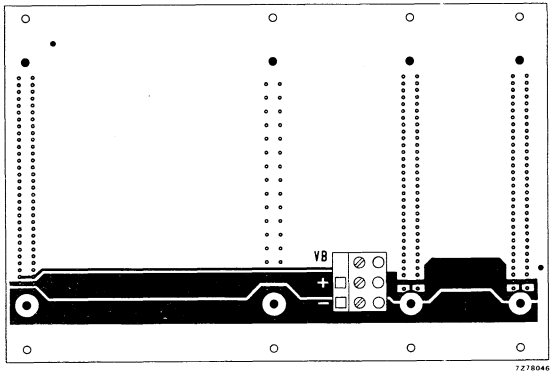
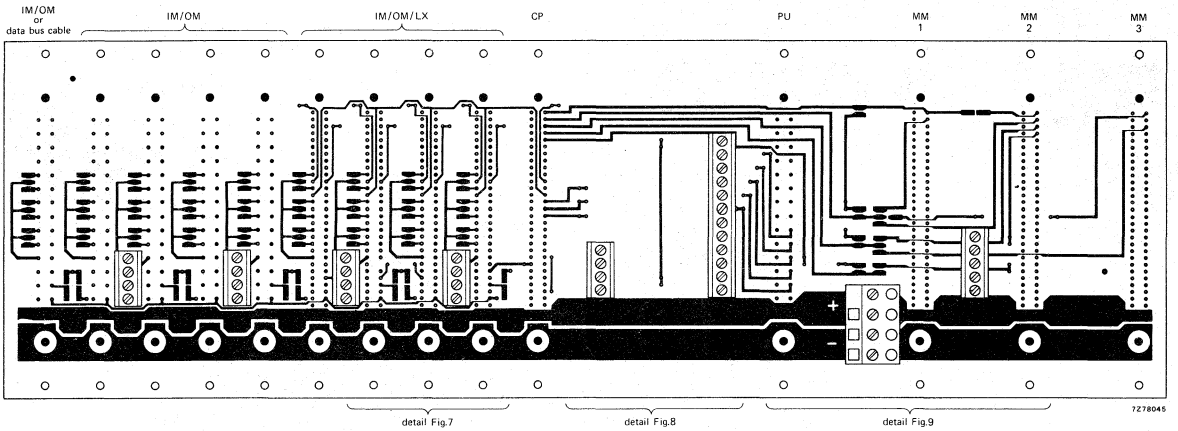


Fig. 2 Back panel BP12.

IM = input module
OM = output module
LX = load external interface module
CP = central processor
PU = programming unit
MM = program memory module
+ = +5 V ± 5%
– = 0 V
} supply voltage
V_B = +4,5 V to +7,5 V (battery voltage)
Data bus cable is only used for connecting a BP15 or BP16 panel.



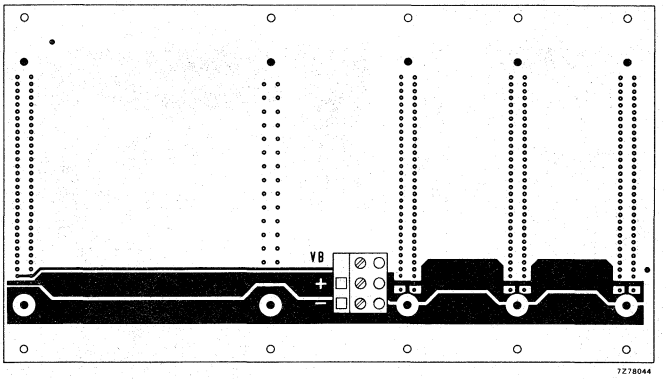
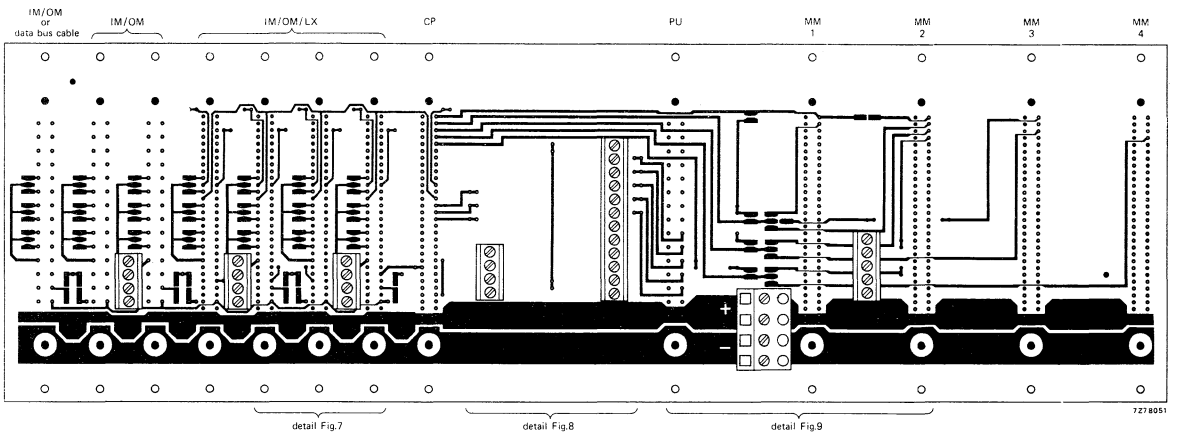


Fig. 3 Back panel BP13.

IM = input module
OM = output module
LX = load external interface module
CP = central processor
PU = programming unit
MM = program memory module
+ = +5 V ± 5%
– = 0
} supply voltage
V_B = +4,5 V to +7,5 V (battery voltage)
Data bus cable is only used for connecting a BP15 or BP16 panel.



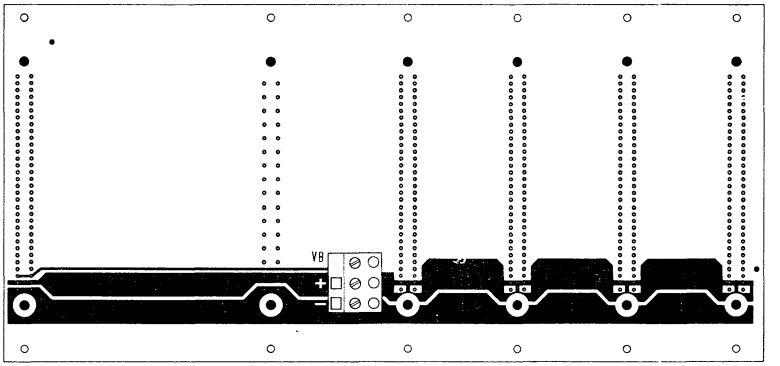


Fig. 4 Back panel BP14.

IM = input module
OM = output module
LX = load external interface module
CP = central processor
PU = programming unit
MM = program memory module
+ = +5 V ± 5% } supply voltage
– = 0 V }
V_B = +4,5 V to +7,5 V (battery voltage)
Data bus cable is only used for connecting a BP15 or BP16 panel.

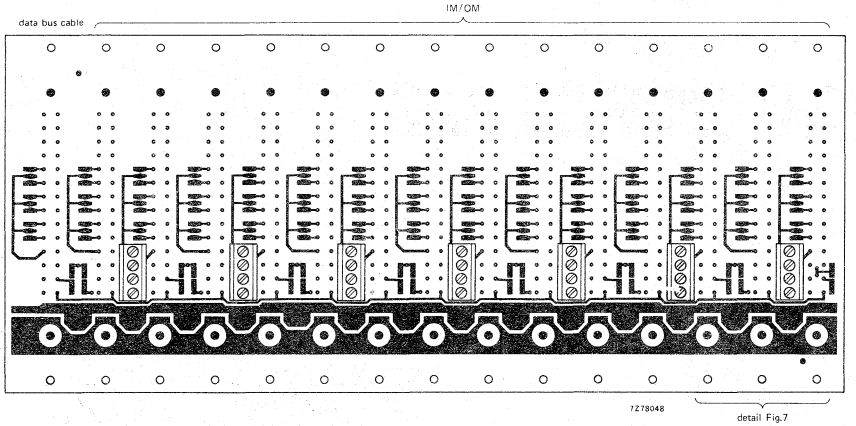


Fig. 5 Back panel BP15.
IM = input module
OM = output module

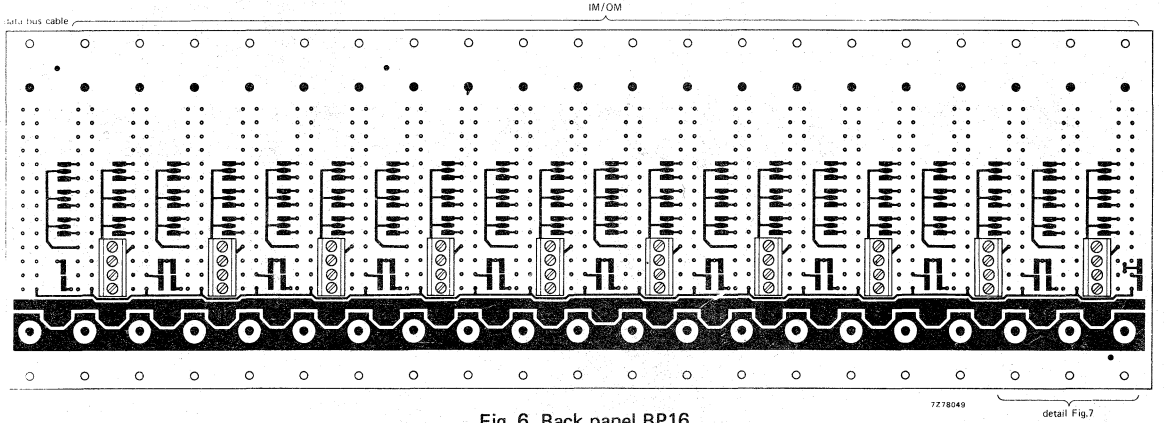


Fig. 6 Back panel BP16.
IM = input module
OM = output module

Each of the IM and OM modules has a discrete address so that the central processor can address each in turn during an input/output cycle. This address is formed by bridging the appropriate MID pad ($\overline{MID}_{0-4}$) and the adjacent 0 V pad (connected to connector 1, pin c22). Table 2 gives the address codes for the IM and OM modules. The $\overline{MID}_5$ pad is not used.

If no LX modules are used, it is important to assign the $\overline{MID}$ addresses to the IM and OM modules, so that the spare addresses, if any, are of a higher order than the used addresses. If this is not done, the input/output cycle will take longer than necessary. If no LX modules are inserted, the IDLC pad of the last IM/OM module (the one with the highest address) must be bridged to the adjacent r or n-shaped pad. If output modules are inserted at places IM/OM/LX2 and IM/OM/LX3, for instance, a logic LOW level applied via wires, connected to REO_2 and REO_3 of the connector block between places IM/OM/LX2 and IM/OM/LX1, will reset all the output latches in the relevant modules. Consequently the output transistors are driven in the non-conductive state. A logic LOW (inhibit) applied via wires connected to MIN_1 or MIN_2 of the same connector block, causes data from input modules (IM/LX) inserted at places IM/OM/LX1 or IM/OM/LX2 respectively, to be ignored by the central processor. It also prevents data stored during the preceding input/output cycle in output modules, inserted in the same places, from changing. If one or more LX modules are inserted, pin a25 automatically connects the IDLC line of the central processor to zero (maximum cycle time of 0,924 ms). Removal of all LX modules will affect the 0,924 ms cycle time. As the maximum number of LX modules in any one PLC system is 4, only two MID pads are used for addressing (see Table 3).

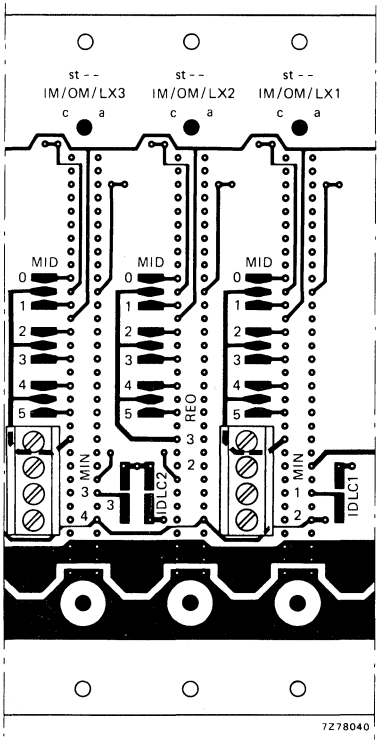


Fig. 7 Detail of back panels BP11 to BP16.
Note: $\overline{MID}_5$ is normally not used.

Table 2 IM and OM module address codes

$\overline{MID}_0$	$\overline{MID}_1$	$\overline{MID}_2$	$\overline{MID}_3$	$\overline{MID}_4$	input/output stage address – scratch-pad locations
–	–	–	–	–	000 to 017
0 V	–	–	–	–	020 to 037
–	0 V	–	–	–	040 to 057
0 V	0 V	–	–	–	060 to 077
–	–	0 V	–	–	100 to 117
0 V	–	0 V	–	–	120 to 137
–	0 V	0 V	–	–	140 to 157
0 V	0 V	0 V	–	–	160 to 177
–	–	–	0 V	–	200 to 217
0 V	–	–	0 V	–	220 to 237
–	0 V	–	0 V	–	240 to 257
0 V	0 V	–	0 V	–	260 to 277
–	–	0 V	0 V	–	300 to 317
0 V	–	0 V	0 V	–	320 to 337
–	0 V	0 V	0 V	–	340 to 357
0 V	0 V	0 V	0 V	–	360 to 377
–	–	–	–	0 V	400 to 417
0 V	–	–	–	0 V	420 to 437
–	0 V	–	–	0 V	440 to 457
0 V	0 V	–	–	0 V	460 to 477
–	–	0 V	–	0 V	500 to 517
0 V	–	0 V	–	0 V	520 to 537
–	0 V	0 V	–	0 V	540 to 557
0 V	0 V	0 V	–	0 V	560 to 577
–	–	–	0 V	0 V	600 to 617
0 V	–	–	0 V	0 V	620 to 637
–	0 V	–	0 V	0 V	640 to 657
0 V	0 V	–	0 V	0 V	660 to 677
–	–	0 V	0 V	0 V	700 to 717
0 V	–	0 V	0 V	0 V	720 to 737
–	0 V	0 V	0 V	0 V	740 to 757
0 V	0 V	0 V	0 V	0 V	760 to 777

Table 3 LX module address codes

$\overline{MID}_3$	$\overline{MID}_4$	address of eight-bit data source
–	–	00o to 17o
0 V	–	20o to 37o
–	0 V	40o to 57o
0 V	0 V	60o to 77o

Notes to Tables 2 and 3.

1. 0 V indicates that the $\overline{MID}$ terminal is connected to connector 1, pin c22 (0 V).
2. – indicates that the $\overline{MID}$ terminal is floating.
3. The least significant digit of each LX address is always 0, e.g. 00o to 17o in the table signifies addresses 00o, 01o, 02o, 03o etc., up to 17o.

Fig. 8 shows the connector blocks on the back panels BP11 to BP14. The left-hand block contains connections for the REO_1 wire and the MIN wire with the number of the highest IM/OM place (13, 11, 9 or 7). A CLCP wire can be connected to the upper terminal, carrying a disable signal from external source (switch) to central processor (active LOW). The operation of this signal in combination with the SPCE signal, carried by a wire connected to the lower terminal, is given in Table 4.

The right-hand connector block contains the output connection ALARM, which will become LOW when the supply voltage drops below 4,75 V. The tape reader connections TB_1 to TB_7 and STROBE can be connected to the corresponding tape bit outputs of a tape reader. Connection BSP or $\overline{BSP}$ must then be connected to the start/stop input of the tape reader. Connection SLTP must be switched to 0 V during tape reader programming and left floating during keyboard programming.

Fig. 8 Detail of back panels BP11 to BP14.

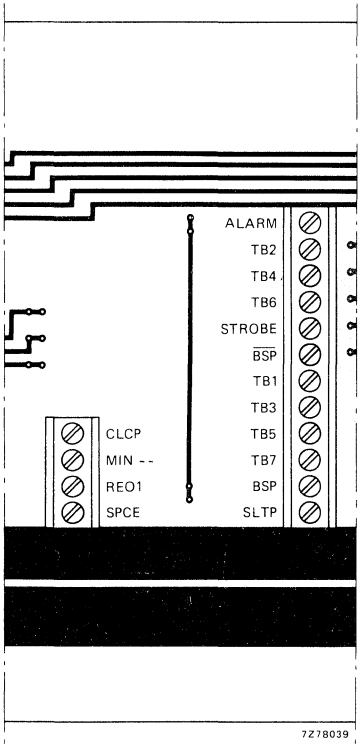


Table 4 Operation of CLCP and SPCE

CLCP	SPCE	operation
0	X*	The central processor is held at the beginning of an input/output cycle.
1	X*	The central processor is running.
0 → 1	1	The central processor starts running at the beginning of an input/output cycle. All scratch-pad locations, except those corresponding to inputs are reset to '0' during the first input/output cycle. All outputs from the PLC output modules are passive after the first input/output cycle.
0 → 1	0	The central processor starts running at the beginning of an input/output cycle. Any data existing in the scratch-pad locations corresponding to outputs determine the state of the output stages in the output modules during the first input/output cycle.

* X indicates either 0 or 1.

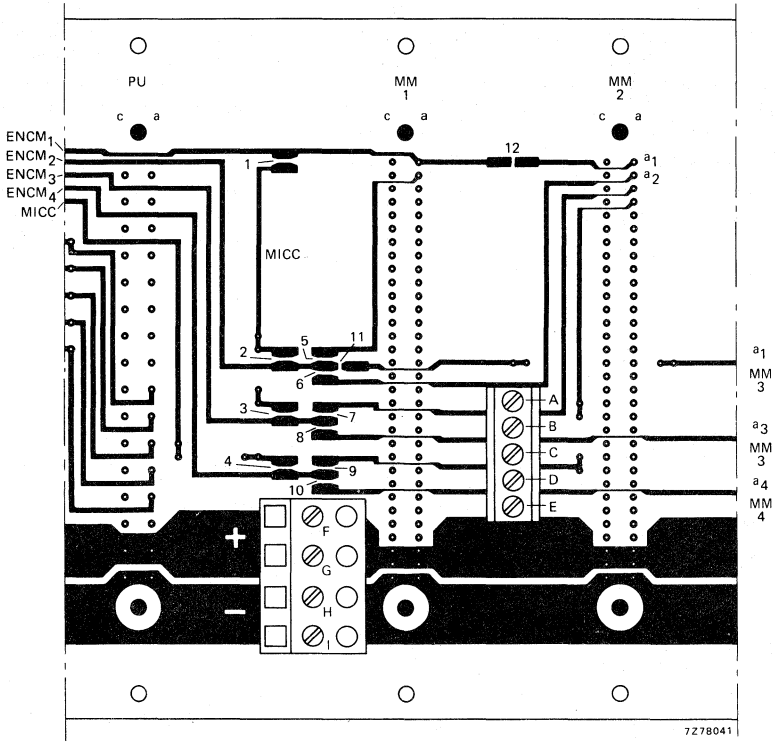


Fig. 9 Detail of back panels BP12 to BP14.

A = PRB; B = START; C = INH; D = MSI_1; E = MSI_2; F = +5 V, ± 5%; G = +5 V, ± 5%; H = 0 V; I = 0 V.

Pads 11 and 12 and connections A to E are used for program copying with the MM11 module.

$ENCM_{1-4}$ = enable signal from central processor to program memory;

MICC = memory identification signal derived from MM module in highest position;

PRB = program busy output signal to external equipment;

INH = inhibit input, when LOW the start input is inoperative;

MSI = mode selection inputs (see data sheets MM11).

Table 5 MM module address codes

total byte content	number and type of MM modules	MM module position 1	2	3	4	pad pairs to be bridged MICC	ENCM	module position in which a_1 must be connected with a_2
1k	1 MM10	■				1		
	1 MM12	▭				1		
2k	2 MM10	■	■			2	6	
	2 MM12	▭	▭			2	6	1 2
	1 MM12	■				2	5	
3k	3 MM10	■	■	■		3	6 8	
	3 MM12	▭	▭	▭		3	6 8	1 2 3
	2 MM12	■	▭			3	5 7 9	
4k	4 MM10	■	■	■	■	4	6 8 10	
	4 MM12	▭	▭	▭	▭	4	6 8 10	1 2 3 4
	2 MM12	■	■			4	5 7 9	

Note

▭ = MM12 equipped with 1 k only (PROMs in position 1A and 1B).

■ = MM12 equipped with 2 k.

PC20 MODULES

MODULES FOR PROGRAMMABLE CONTROLLERS

GENERAL

The programmable controller PC20 is used for controlling machines and/or processes. It can be easily programmed and re-programmed.

The modular design of the PC20 enables a user to build a programmable controller which is 'tailor-made' for his control task. By specifying the number and the types of PC20 modules that he requires he only has to purchase the electronic capability he needs.

The PC20 modules are on standard double Eurocards.* Optically isolated interface circuits, specifically designed for an industrial environment, provide excellent noise immunity and a high degree of isolation. The internationally accepted machine signal level of 24 V is used and generous tolerances on operational margins and thresholds ensures good compatibility.

Besides these modules, the PC20 comprises back panels, frames (19 in racks), input and output cables, and a standard power supply. The frames and modules conform to IEC 297 or DIN 41494 (for racks) and IEC 130-14 or DIN 41612 (for connectors). For smaller controllers the special frame SC20 and power supply SO20 are available.

The microcontroller MC20 is suited for controlling small systems. This controller is based on the same principles as the PC20 system, however it is built on a single printed board** with sufficient inputs and outputs for the general run of machine tool and process controls.

Software modules are available e.g. for communication in hierarchical systems.

Tables 1 to 5 give a survey of the available modules, accessories and cables.

Table 1 Modules

type	description	catalogue number
AD20	analogue to digital module	4322 027 94200
AI20	analogue input module	9360 023 90112
AO20	analogue output module	9360 024 00112
CP20	central processor with program memory (2 k (E) PROM)	4322 027 92040
CP21	central processor with program mempry (1 k RAM)	4322 027 92050
CP22	central processor without program memory	4322 027 92060
CP24	central processor with program memory (2 k RAM)	4322 027 94140
DA20	digital to analogue module	4322 027 94210
IM20	input module (16 inputs)	4322 027 92000
MM20	program memory module (8 k (E) PROM)	4322 027 92070
MM21	program memory module (8 k RAM)	4322 027 92080
MM22	program memory module (4 k RAM)	4322 027 94160
OM20	output module (16 x 0,5 A)	4322 027 92010
OM21	output module (8 x 2 A)	4322 027 92020
OM22	output module (32 x 0,1 A)	4322 027 94100
RP20	bidirectional parallel interface	4322 027 92170
RS20	bidirectional serial interface	4322 027 92180
SO20	supply and output module (8 x 0,5 A)	4322 027 92030
VI20	bidirectional serial interface	4322 027 92200
MC20	microcontroller	4322 027 23000

* Except programming unit PU20, which is a desk-top apparatus.

** Different from standard Eurocards.

Table 2 Programming aids

type	description	catalogue number
MI20	microcontroller interface for MC20	4322 027 94190
PU20	programming unit for PC20 and MC20	4322 027 92090
PU21	programming unit interface for PC20	4322 027 92100
PU23	programming unit interface for PC20 and MC20	4322 027 94180

Table 3 Accessories

type	description	catalogue number
BI20	bus interface	4322 027 94170
BP22	terminal strip for inputs/outputs in controller cabinet SC20	4322 027 92140
BP23	back panel for Eurorack	4322 027 94010
BP25	back panel for half extension rack	4322 027 94030
BP26	back panel for full extension rack	4322 027 94040
BP27	terminal strip for output module OM22 in controller cabinet SC20	4322 027 93950
FP20	front plate, 15 mm width, in controller cabinet SC20	4322 027 92150
FP21	front plate, 20 mm width (standard module width)	4322 027 92160
MB20	mounting clip for microcontroller MC20	4322 027 23080
RA23	main rack assembly	9390 294 10000
RA25	half extension rack assembly (for 15 I/O modules)	9390 294 20000
RA26	full extension rack assembly (for 21 I/O modules)	9390 294 30000
SC20	small controller cabinet	4322 027 92110
	CP front panel kit (one LED hole)	4322 027 91440
	IM/OM front panel kit (16 LED holes)	4322 027 91450
	AI/AO front panel kit (double width; no holes)	4322 027 91460

Table 4 Cables

type	description	catalogue number
BC21	bus extension cable for one extension rack	9390 293 90000
BC22	bus extension cable for two extension racks	9390 294 00000
BC23	bus extension cable for three extension racks	9390 298 90000
CC20	connecting cable for module OM21	9390 293 50000
CC21	connecting cable for module SO20	9390 293 60000
CC22	connecting cable for module IM20	9390 293 70000
CC23	connecting cable for modules IM20 and OM20	9390 293 80000

Table 5 Software modules

type	description	catalogue number
PVI1	message program	4322 027 99011
PVI2	data terminal program	4322 027 99021
PVI3	mass memory program	4322 027 99031
PVI4	communication program A	4322 027 99041
PVI5	communication program B	4322 027 99051
PVI6	arithmetic program	4322 027 99061
PVI7	communication program C	4322 027 99071
PVI8	PID control loop	4322 027 99081
PDS1	program documentation system	4322 027 99911
PDS2	program development system	4322 027 99921

Figure 1 shows, in a simplified form, the function of each of the PC20 modules. In operation the PC20 cycles continuously through a data input/output cycle and a data processing cycle.

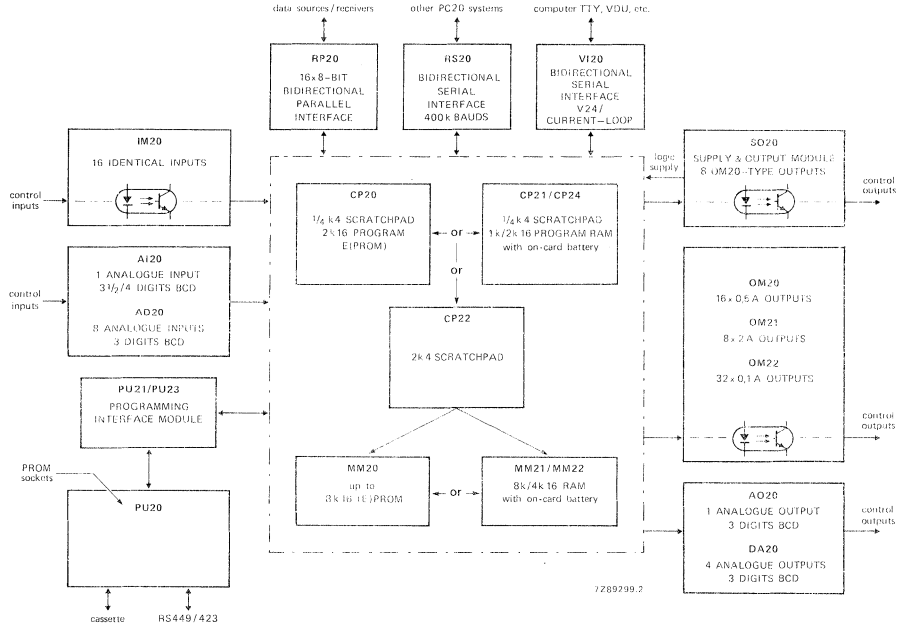


Fig. 1 Diagram of PC20 system.

The input module converts the signals from the plant into a binary form acceptable to the central processor.

The central processor reads the data from the input module, performs logic equations on it in accordance with the program instructions and transfers the results to the output module.

The output module converts the binary data from the central processor to electrical signals suitable for the control of the plant.

The program memory is the store in which the set of instructions that comprise the program are stored. These instructions dictate the actions which must be taken in response to the condition of each input.

The programming unit PU20 is the means by which an operator can write a program, or changes to a program, into the program memory. The unit is a portable desk-top apparatus so that only one is required to serve any number of PC20 systems. It is connected to the PC20 system via the programming unit interface PU21 or PU23, which is not too expensive to leave in the PC20 system.

For programming and monitoring the MC20 system, the same programming unit (PU20) as for the PC20 system is used, however this unit has to be used in conjunction with microcontroller interface MI20 and programming unit interface PU23, see Fig. 2.

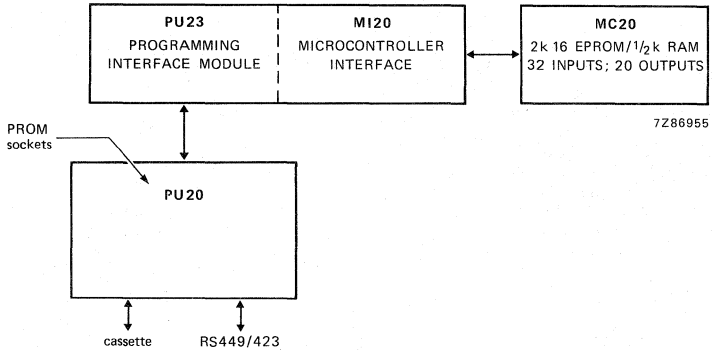


Fig. 2 Diagram of MC20 system.

GENERAL CHARACTERISTICS

Operating temperature range	0 to +60 °C (0 to +45 °C*)
Storage temperature range	–40 to +70 °C
Dimensions	160 mm x 233 mm (double Eurocard) according to IEC 297 or DIN 41494**
Supply voltage (d.c.)	V_P = 10 V ± 10%; 24 V ± 25%**
Number of input + output signals	2000
Maximum program length	8 k instructions
Cycle time	1 ms for a typical program of 1 k instructions

TESTS AND REQUIREMENTS

All modules are designed to meet the tests below.

Vibration test

IEC 68-2-6, test method Fc; 10 to 55 Hz, amplitude 0,75 mm (0,35 mm*) or 5g (whichever is less).

Shock test

IEC 68-2-27, test method Ea; 3 shocks in 6 directions, pulse duration 11 ms, peak acceleration 50g(30g*).

Rapid change of temperature test

IEC 68-2-14, test method Na: 5 cycles of 2 h at –40 °C and 2 h at +85 °C.

Damp heat test

IEC 68-2-3, test method Ca: 21 days at 40 °C, R.H. 90 to 95%.

Note

For detailed information refer to the PC20 User Manual, catalogue number 9398 609 60011.

* Valid for PU20.
** For PU20 and MC20 see the relevant data sheet.

CENTRAL PROCESSOR

DESCRIPTION

The central processor CP20 is for use with other PC20 modules, to assemble a programmable controller.

The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.

The central processor block diagram is given in Fig. 1. The *data processor* controls the system and the complete timing. It includes the instruction decoder, the 1-bit logic processor, the 4-bit arithmetic processor and the data control.

The *address processor* generates addresses for the program memory under program control. It also generates addresses for the input and output modules.

The *program memory* consists of 2 EPROMs 2716 (2k), for which 2 sockets (A and B, Fig. 5) are provided. The CP20 is supplied with 2 empty EPROMs, which can be programmed on the programming unit PU20.

The capacity of the *scratchpad memory* is ¼k4. Depending on the instruction, the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3). In the latter case the address notation is, for example, 147.2 or 076.0. The CP20 has no on-board battery back-up; provisions for an external battery for data retention in the scratchpad memory are present.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.

The *reset scratchpad memory circuit* allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.

The *timer clock circuit* provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).

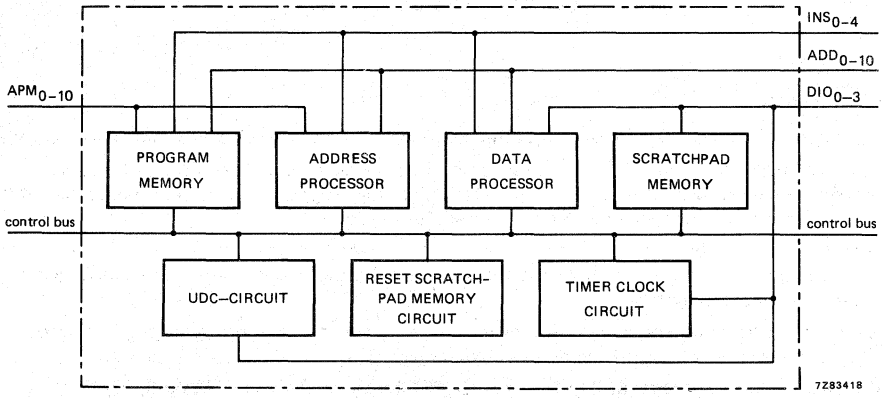


Fig. 1 Block diagram.

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC_0 and PHC_1, are:

- up-date and check phase (UDC): $PHC_0 = 0$, $PHC_1 = 0$;
- reset scratchpad memory (RSM): $PHC_0 = 1$, $PHC_1 = 0$;
- data processing (DP): $PHC_0 = 0$; $PHC_1 = 1$;
- up-date input/output (I/O): $PHC_0 = 1$, $PHC_1 = 1$.

Each central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

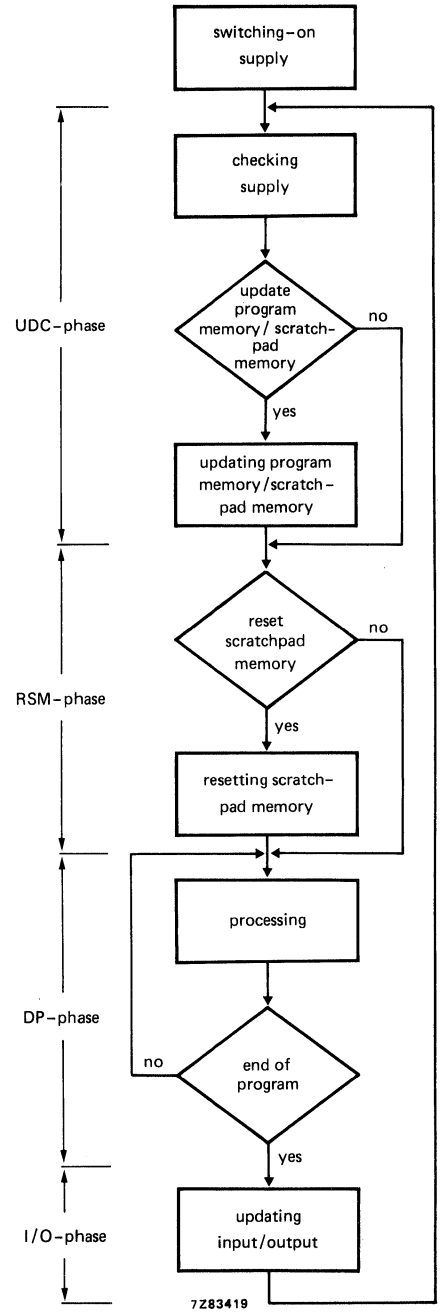


Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	10 V ± 10%	
current	I_P	max. 270	mA

Requirements of the external battery to retain the contents of the scratchpad memory during power failure.

Battery voltage	V_B	3 to 4,5	V
Battery current (V_P = 0 V)	I_B	max. 2	mA
Trickle charge current (V_P = 10 V)		typ. −6	mA

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations (Fig. 5) connector 1	connector 2
BI-DIRECTIONAL BUSSES			
ADD_0	Address bus interconnected with PU21 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, c6	
ADD_1		a7, c7	
ADD_2		a8, c8	
ADD_3		a9, c9	
ADD_4		a10, c10	
ADD_5		a11, c11	
ADD_6		a12, c12	
ADD_7		a13, c13	
ADD_8		a14, c14	
ADD_9		a15, c15	
ADD_{10}		a16, c16	
APM_0	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).		a16, c16
APM_1			a17, c17
APM_2			a18, c18
APM_3			a19, c19
APM_4			a20, c20
APM_5			a21, c21
APM_6			a22, c22
APM_7			a23, c23
APM_8			a24, c24
APM_9			a25, c25
APM_{10}			a26, c26
APM_{11}	Pseudo address bits connected via resistor to 0 V.		a27, c27
APM_{12}			a28, c28
DIO_0	Data bus; receives data for scratchpad memory from input modules and PU21, transmits data from scratchpad memory to output modules and PU21; data bus is controlled by WEPC or by R/$\overline{W}$SM.	a19, c19	
DIO_1		a20, c20	
DIO_2		a21, c21	
DIO_3		a22, c22	

	function	terminations (Fig. 5)	
		connector 1	connector 2
INS_0 INS_1 INS_2 INS_3 INS_4	Instruction bus, interconnected with PU21; commanded by PDBE.	a1, c1 a2, c2 a3, c3 a4, c4 a5, c5	
INPUTS			
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29, c29	
CPSD	Central processor slow down; input commanded by PU21.		a3, c3
CPSI	Central processor stop initiate; command from PU21 stops central processor in UDC-phase (active HIGH).		a4, c4
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored.	a25	
HOLD	Command from PU21 to stop central processor in DP-phase (active LOW).		a6, c6
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input.		a1, c1
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs.		a2, c2
PRF	Preparation input/output modules finished.	a24	
$\overline{RCP}$	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 2 mA.		a12, c12
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.		a10, c10

	function	terminations (Fig. 5)	
		connector 1	connector 2
R/$\overline{W}$SM	Read-write level from input and output modules; only effective during I/O-phase.	c24	
WEPC	Write enable signal from PU21; prepares central processor to store data from PU21 into scratch-pad memory.	c28	
WPSM	Write pulse for scratchpad memory; signal from PU21 to store data on DIO_{0-3} into scratchpad memory.		a13, c13
OUTPUTS			
APF	Address processing for input and output modules finished; address stable.	a26	
CLOCK	Clock output to PU21.		a7, c7
CPSC	Central processor stop completed; command (HIGH) to PU21 indicating that central processor has been stopped in UDC-phase.		a5, c5
PB_0 PB_1	Page bits, connected to 0 V.	a17 c17	
PHC_0 PHC_1	Phase control to PU21 and input and output modules.	c23 a23	
$\overline{RCO}$	Reset output to output modules; becomes LOW during switch-on of the system, or if $\overline{RCP}$ is LOW. When a wire jump has been inserted between the $\overline{RCO}$ points on the module (Fig. 3), $\overline{RCO}$ output will also become LOW if $V_P < 9$ V or > 11 V.	c27	
RR	Result Register.	a18, c18	
SBI	Storage command to store data on data bus into output modules and PU21.	c26	
SRI + SRI −	System run indication; Darlington transistor output, galvanically isolated by means of opto-coupler. SRI + = collector, SRI − = emitter. When the system runs the transistor is non conducting; when the system stops the transistor switches on and off (see for circuit diagram, Fig. 4).	a30 c30	

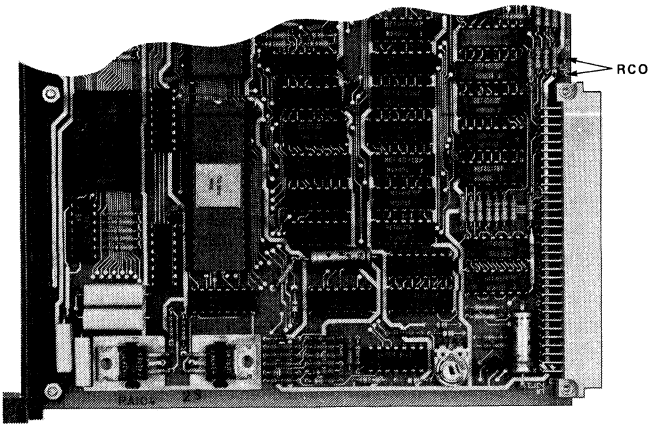


Fig. 3 Location of RCO points.

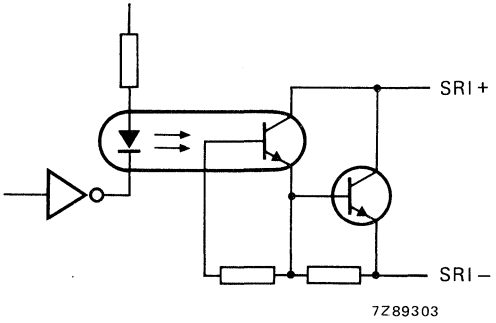


Fig. 4 Circuit diagram of SRI output. Transistor conducting: I_Q = max. 100 mA, $V_{CE} < 1{,}5$ V; transistor non-conducting: I_Q = max. 10 μA; $V_{CE} \leqslant 30$ V; in case of system stop the output stage switches on and off with a cycle time of 0,4 s.

Fixed scratchpad memory addresses

address	description
000.0	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
000.2	24 V alarm output (becomes 1 if $V_S \leqslant 17{,}5$ V).
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.

MECHANICAL DATA

Dimensions in mm

Outlines

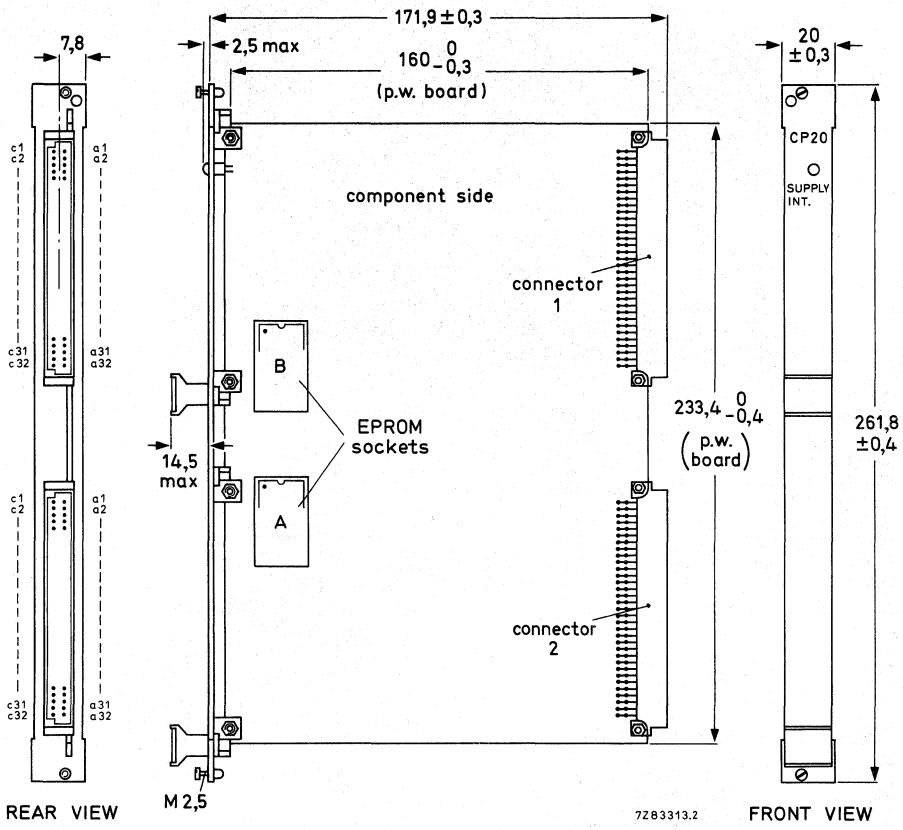


Fig. 5.

Mass approx. 270 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
INS_0	1	INS_0	PABE	1	PABE
INS_1	2	INS_1	PDBE	2	PDBE
INS_2	3	INS_2	CPSD	3	CPSD
INS_3	4	INS_3	CPSI	4	CPSI
INS_4	5	INS_4	CPSC	5	CPSC
ADD_0	6	ADD_0	HOLD	6	HOLD
ADD_1	7	ADD_1	CLOCK	7	CLOCK
ADD_2	8	ADD_2	n.c.	8	n.c.
ADD_3	9	ADD_3	n.c.	9	n.c.
ADD_4	10	ADD_4	RSME	10	RSME
ADD_5	11	ADD_5	n.c.	11	n.c.
ADD_6	12	ADD_6	$\overline{RCP}$	12	$\overline{RCP}$
ADD_7	13	ADD_7	WPSM	13	WPSM
ADD_8	14	ADD_8	n.c.	14	n.c.
ADD_9	15	ADD_9	n.c.	15	n.c.
ADD_{10}	16	ADD_{10}	APM_0	16	APM_0
PB_1	17	PB_0	APM_1	17	APM_1
RR	18	RR	APM_2	18	APM_2
DIO_0	19	DIO_0	APM_3	19	APM_3
DIO_1	20	DIO_1	APM_4	20	APM_4
DIO_2	21	DIO_2	APM_5	21	APM_5
DIO_3	22	DIO_3	APM_6	22	APM_6
PHC_0	23	PHC_1	APM_7	23	APM_7
$R/\overline{WSM}$	24	PRF	APM_8	24	APM_8
0 V *	25	DEF	APM_9	25	APM_9
$\overline{SBI}$	26	APF	APM_{10}	26	APM_{10}
$\overline{RCO}$	27	n.c.	APM_{11}	27	APM_{11}
WEPC	28	n.c.	APM_{12}	28	APM_{12}
ALI	29	ALI	n.c.	29	n.c.
SRI –	30	SRI +	VB	30	VB
V_p	31	V_p	V_p	31	V_p
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

* No supply line; is used as return line for control signals.

CENTRAL PROCESSOR

DESCRIPTION

The central processor CP21 is for use with other PC20 modules, to assemble a programmable controller.

The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.

The central processor block diagram is given in Fig. 1. The *data processor* controls the system and the complete timing. It includes the instruction decoder, the 1-bit logic processor, the 4-bit arithmetic processor and the data control.

The *address processor* generates addresses for the program memory under program control. It also generates addresses for the input and output modules.

The *program memory* is a C-MOS RAM (1 k16). The CP21 has on-board battery back-up and a provision to connect an external battery for longer memory retention.

The capacity of the *scratchpad memory* is ¼k4. Depending on the instruction, the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3). In the latter case, the address notation is, for example, 147.2 or 076.0. The on-board battery for data retention in the program memory RAM, is also used for data retention of the scratchpad memory.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.

The *reset scratchpad memory circuit* allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.

The *timer clock circuit* provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).

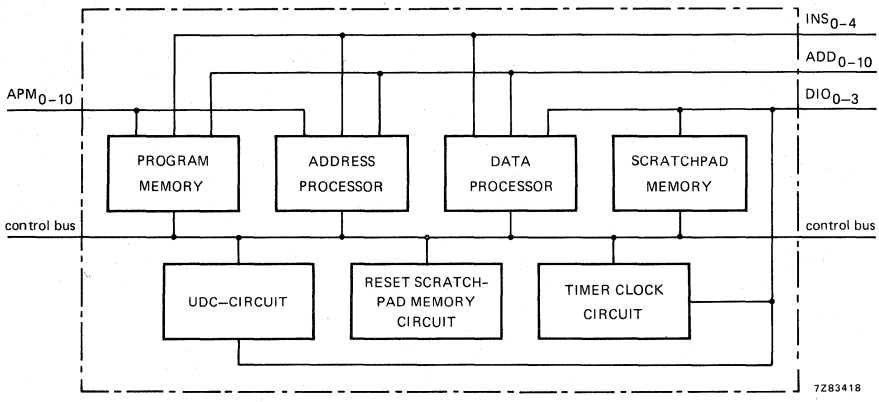


Fig. 1 Block diagram.

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC_0 and PHC_1, are:

- up-date and check phase (UDC): $PHC_0 = 0$, $PHC_1 = 0$;
- reset scratchpad memory (RSM): $PHC_0 = 1$, $PHC_1 = 0$.
- data processing (DP): $PHC_0 = 0$, $PHC_1 = 1$.
- up-date input/output (I/O): $PHC_0 = 1$, $PHC_1 = 1$.

Each central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130–14 or DIN 41612 for connectors.

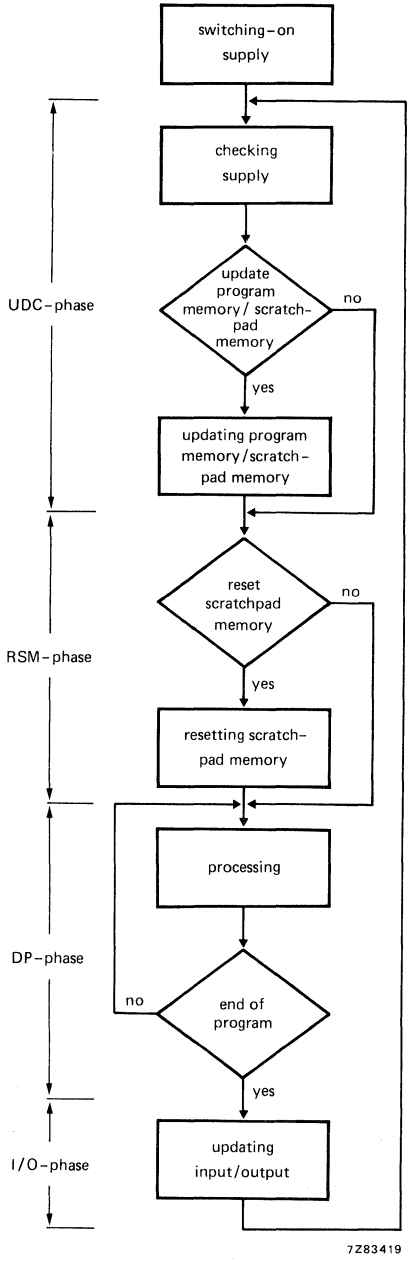


Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	10 V ± 10%
current	I_P	max. 160 mA

Requirements of the external battery to retain the contents of the program memory and the scratchpad memory during power failure.

Battery voltage	V_B	3 to 4,5 V
Battery current (V_P = 0 V)	I_B	max. 2 mA
Trickle charge current (V_P = 10 V)		typ. −6 mA
Data retention with on-board battery at 40 °C		typ. 40 h, provided the module is in operation for at least 20 h

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations (Fig. 4) connector 1	connector 2
BI-DIRECTIONAL BUSSES			
ADD_0	Address bus interconnected with PU21 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, c6	
ADD_1		a7, c7	
ADD_2		a8, c8	
ADD_3		a9, c9	
ADD_4		a10, c10	
ADD_5		a11, c11	
ADD_6		a12, c12	
ADD_7		a13, c13	
ADD_8		a14, c14	
ADD_9		a15, c15	
ADD_{10}		a16, c16	
APM_0	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).		a16, c16
APM_1			a17, c17
APM_2			a18, c18
APM_3			a19, c19
APM_4			a20, c20
APM_5			a21, c21
APM_6			a22, c22
APM_7			a23, c23
APM_8			a24, c24
APM_9			a25, c25
APM_{10}			a26, c26
APM_{11}	Pseudo address bits connected via resistor to 0 V.		a27, c27
APM_{12}			a28, c28
DIO_0	Data bus; receives data for scratchpad memory from input modules and PU21, transmits data from scratchpad memory to output modules and PU21; data bus is controlled by WEPC or by R/$\overline{W}$SM.	a19, c19	
DIO_1		a20, c20	
DIO_2		a21, c21	
DIO_3		a22, c22	

	function	terminations (Fig. 4)	
		connector 1	connector 2
INS_0 INS_1 INS_2 INS_3 INS_4	Instruction bus, interconnected with PU21; commanded by PDBE,	a1, c1 a2, c2 a3, c3 a4, c4 a5, c5	
INPUTS			
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29, c29	
CPSD	Central processor slow down; input commanded by PU21.		a3, c3
CPSI	Central processor stop initiate; command from PU21 stops central processor in UCD-phase (active HIGH).		a4, c4
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored.	a25	
HOLD	Command from PU21 to stop central processor in DP-phase (active LOW).		a6, c6
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input.		a1, c1
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs.		a2, c2
PRF	Preparation input/output modules finished.	a24	
$\overline{RCP}$	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 2 mA.		a12, c12
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.		a10, c10
$\overline{R}$/WPM	Write signal from PU21 to CP21, to store data in program memory (active HIGH).		a14, c14

	function	terminations (Fig. 4)	
		connector 1	connector 2
R/$\overline{W}$SM	Read-write level from input and output modules; only effective during I/O-phase.	c24	
WEPC	Write enable signal from PU21; prepares central processor to store data from PU21 into scratch-pad memory.	c28	
WPSM	Write pulse for scratchpad memory; signal from PU21 to store data on DIO_{0-3} into scratchpad memory.		a13, c13
OUTPUTS			
APF	Address processing for input and output modules finished; address stable.	a26	
CLOCK	Clock output to PU21.		a7, c7
CPSC	Central processor stop completed; command (HIGH) to PU21 indicating that central processor has been stopped in UDC-phase.		a5, c5
PB_0 PB_1	Page bits, connected to 0 V.	a17 c17	
PHC_0 PHC_1	Phase control to PU21 and input and output modules.	c23 a23	
$\overline{RCO}$	Reset output to output modules; becomes LOW during switch-on of the system, or if $\overline{RCP}$ is LOW. When a wire jump has been inserted between the RCO points on the module (Fig. 3), $\overline{RCO}$ output will also become LOW if $V_P < 9$ V or > 11 V.	c27	
RR	Result Register	a18, c18	
SBI	Storage command to store data on data bus into output modules and PU21.	c26	

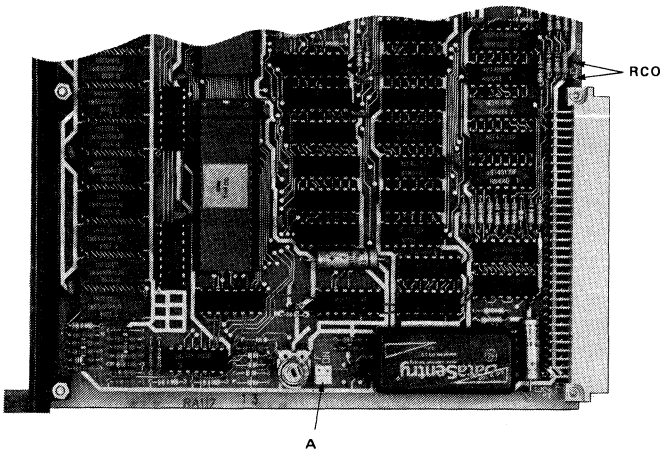


Fig. 3 Location of RCO points and switch (jumper A) of on-board battery.

Fixed scratchpad memory addresses

address	description
000.0	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
000.2	24 V alarm output (becomes 1 if $V_S \leqslant 17{,}5$ V).
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.

MECHANICAL DATA

Dimensions in mm

Outlines

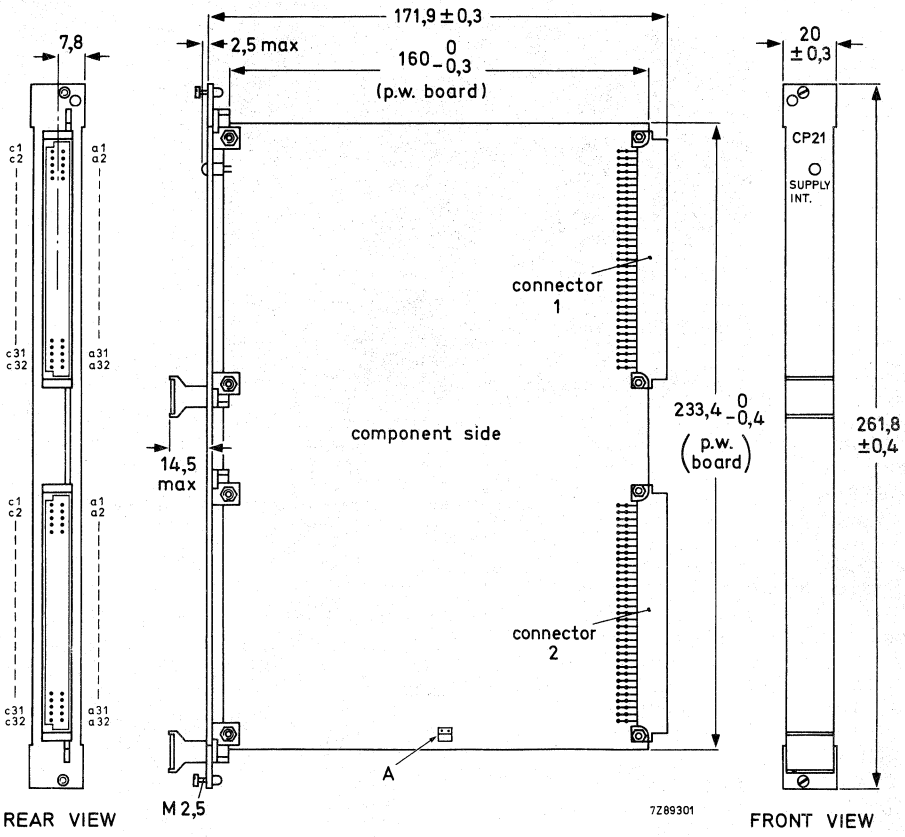


Fig. 4.

Mass approx. 270 g

Notes

1. At delivery of the central processor the on-board battery is switched off (jumper A, Figs 3 and 4, in off-position).
2. If the central processor is removed from the rack, ensure that it is put on an insulated surface to prevent short-circuiting of the on-board battery.

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
INS_0	1	INS_0	PABE	1	PABE
INS_1	2	INS_1	PDBE	2	PDBE
INS_2	3	INS_2	CPSD	3	CPSD
INS_3	4	INS_3	CPSI	4	CPSI
INS_4	5	INS_4	CPSC	5	CPSC
ADD_0	6	ADD_0	HOLD	6	HOLD
ADD_1	7	ADD_1	CLOCK	7	CLOCK
ADD_2	8	ADD_2	n.c.	8	n.c.
ADD_3	9	ADD_3	n.c.	9	n.c.
ADD_4	10	ADD_4	RSME	10	RSME
ADD_5	11	ADD_5	n.c.	11	n.c.
ADD_6	12	ADD_6	$\overline{RCP}$	12	$\overline{RCP}$
ADD_7	13	ADD_7	WPSM	13	WPSM
ADD_8	14	ADD_8	$\overline{R}$/WPM	14	$\overline{R}$/WPM
ADD_9	15	ADD_9	n.c.	15	n.c.
ADD_{10}	16	ADD_{10}	APM_0	16	APM_0
PB_1	17	PB_0	APM_1	17	APM_1
RR	18	RR	APM_2	18	APM_2
DIO_0	19	DIO_0	APM_3	19	APM_3
DIO_1	20	DIO_1	APM_4	20	APM_4
DIO_2	21	DIO_2	APM_5	21	APM_5
DIO_3	22	DIO_3	APM_6	22	APM_6
PHC_0	23	PHC_1	APM_7	23	APM_7
R/$\overline{WSM}$	24	PRF	APM_8	24	APM_8
0 V*	25	DEF	APM_9	25	APM_9
$\overline{SBI}$	26	APF	APM_{10}	26	APM_{10}
$\overline{RCO}$	27	n.c.	APM_{11}	27	APM_{11}
WEPC	28	n.c.	APM_{12}	28	APM_{12}
ALI	29	ALI	n.c.	29	n.c.
n.c.	30	n.c.	VB	30	VB
V_p	31	V_p	V_p	31	V_p
0 V	32	0 V	0 V	32	0 V

n.c. = not connected

* No supply line; is used as return line for control signals.

CENTRAL PROCESSOR

DESCRIPTION

The central processor CP22 is for use with other PC20 modules, to assemble a programmable controller.

The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates the clock pulses for the controller.

The central processor block diagram is given in Fig. 1.

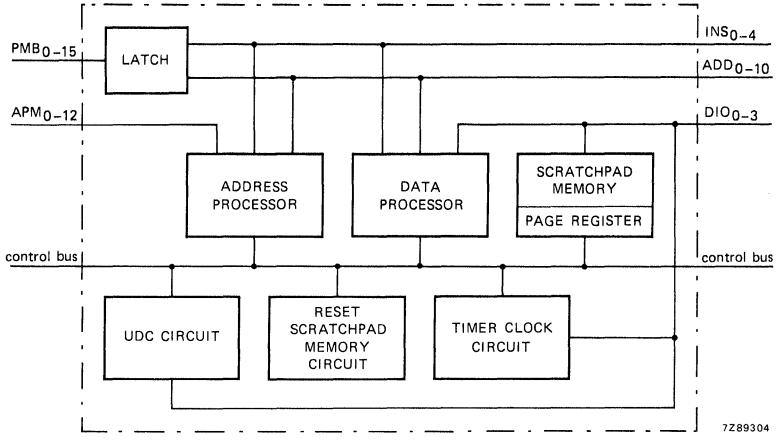


Fig. 1 Block diagram.

The *data processor* performs the control of the system and the complete timing. It includes the instruction decoder, the logic processor, the arithmetic processor and the control of the internal data traffic.

The *address processor* generates addresses for the program memory. It also generates addresses for the input and output modules. It has an address range for an 8 k program memory.

In the *scratchpad memory* the data from the inputs are stored as are the processed data for transfer to the outputs; for this purpose the inputs and outputs each have their own, individual place in the scratchpad. The capacity of the scratchpad memory, including the page register, is 2k4, divided in 4 pages of 512 words each; for details see para. "Organization of scratchpad memory and page register". The CP22 has provisions for an external battery for data retention in the scratchpad memory.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system about power failures. It also controls the access of the programming unit to the system memories.

The *reset scratchpad memory circuit* provides the central processor with the possibility to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after the switch-on of the system.

The *timer clock circuit* provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC_0 and PHC_1, are:

- up-date and check phase (UDC): $PHC_0 = 0$, $PHC_1 = 0$.
- reset scratchpad memory (RSM): $PHC_0 = 1$, $PHC_1 = 0$.
- data processing (DP): $PHC_0 = 0$, $PHC_1 = 1$.
- up-date input/output (I/O): $PHC_0 = 1$, $PHC_1 = 1$.

Each central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board is provided with two F068-I connectors (male parts); the corresponding female parts are on the back panels.

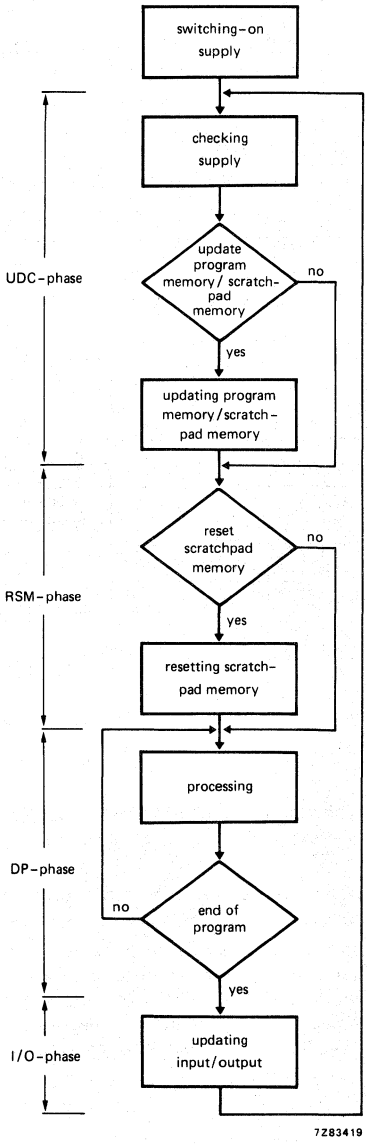


Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	10 V ± 10%
current	I_P	typ. 90 mA max. 110 mA

Requirements of the external battery to retain the contents of the scratchpad memory during power failure.

Battery voltage	V_B	3 to 4,5 V
Battery current (V_P = 0 V)	I_B	typ. 1,5 mA
Trickle charge current (V_P = 10 V)		typ. –5 mA

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications

	function	terminations (Fig. 7) connector 1	connector 2
BI-DIRECTIONAL BUSSES			
ADD_0 ADD_1 ADD_2 ADD_3 ADD_4 ADD_5 ADD_6 ADD_7 ADD_8 ADD_9 ADD_{10}	Address bus interconnected with PU21 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, a7, a8, a9, a10, a11, a12, a13, a14, a15, a16,	
APM_0 APM_1 APM_2 APM_3 APM_4 APM_5 APM_6 APM_7 APM_8 APM_9 APM_{10} APM_{11} APM_{12}	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).		a16, c16 a17, c17 a18, c18 a19, c19 a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28
DIO_0 DIO_1 DIO_2 DIO_3	Data bus; receives data for scratchpad memory from input modules and PU21, transmits data from scartchpad memory to output modules and PU21; data bus is controlled by WEPC or by R/$\overline{WSM}$.	a19, c19 a20, c20 a21, c21 a22, c22	

	function	terminations (Fig. 7)	
		connector 1	connector 2
INS_0 INS_1 INS_2 INS_3 INS_4	Instruction bus, interconnected with PU21; commanded by PDBE.	a1 a2 a3 a4 a5	
INPUTS			
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29, c29	
CPSI	Central processor stop initiate; command from PU21 stops central processor in UDC-phase (active HIGH).		a4, c4
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored.	a25	
HOLD	Command from PU21 to stop central processor in DP-phase (active LOW).		a6, c6
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus is in high-impedance state.		a1, c1
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, ADD-bus function as input, and INS-bus is in high-impedance state.		a2, c2
PMB_0 PMB_1 PMB_2 PMB_3 PMB_4 PMB_5 PMB_6 PMB_7 PMB_8 PMB_9 PMB_{10} PMB_{11} PMB_{12} PMB_{13} PMB_{14} PMB_{15}	Program memory bits from memory module.	c1 c2 c3 c4 c5 c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c16	

	function	terminations (Fig. 7)	
		connector 1	connector 2
PRF	Preparation input/output module finished.	a24	
PRFP	Preparation memory module finished.	a27	
$\overline{RCP}$	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 2 mA		a12, c12
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory locations 002.2 and 002.3.		a10, c10
R/$\overline{W}$SM	Read-write level from input and output modules; only effective during I/O-phase.	c24	
WEPC	Write enable signal from PU21; prepares central processor to store data from PU21 into scratch-pad memory.	c28	
WPSM	Write pulse for scratchpad memory; signal from PU21 to store data on DIO_{0-3} into scartchpad memory		a13, c13
OUTPUTS			
APF	Address processing for input and output modules finished.	a26	
APFP	Address processing for memory modules finished.	a28	
CLOCK	Clock output to PU21.		a7, c7
CPSC	Central processor stop completed; command (HIGH) to PU21 indicating that central processor has been stopped in UDC-phase.		a5, c5
PB_0 PB_1	Page bits, contents of page register, interconnected with PU21.	a17 c17	
PHC_0 PHC_1	Phase control to PU21, memory module and input and output modules.	c23 a23	
$\overline{RCO}$	Reset output to output modules; becomes LOW during switch-on of the system, or if $\overline{RCP}$ is LOW. When a wire jump has been inserted between the RCO points on the module (Fig. 3), $\overline{RCO}$ output will also become LOW if $V_P < 9$ V or > 11 V.	c27	

	function	terminations (Fig. 7)	
		connector 1	connector 2
RR	Result Register, interconnected with PU21.	a18, c18	
SBI	Storage command to store data on data bus into output modules and PU21.	c26	
SRI + SRI –	System run indication; Darlington transistor output, galvanically isolated by means of opto coupler. SRI + = collector, SRI – = emitter. When the system runs the transistor is non conducting; when the system stops the transistor switches on and off (see for circuit diagram, Fig. 4).	a30 c30	

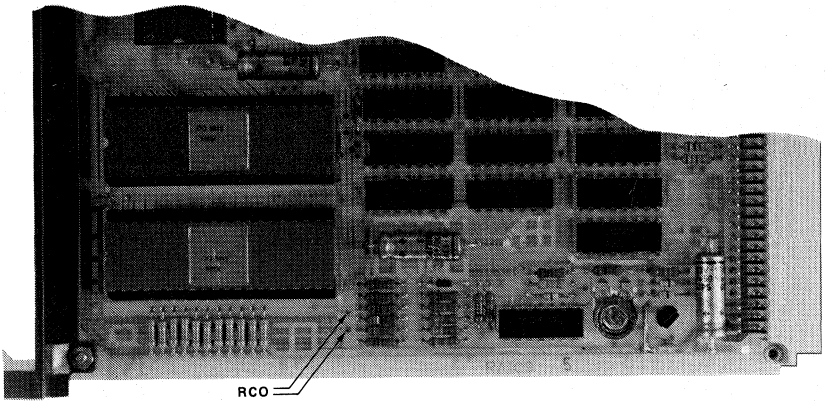


Fig. 3 Location of RCO points.

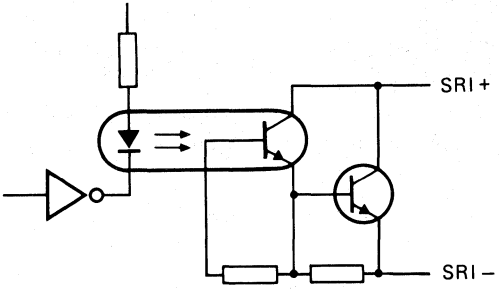


Fig. 4 Circuit diagram of SRI output. Transistor conducting: I_Q = max. 100 mA, $V_{CE} < 1{,}5$ V; transistor non-conducting: I_Q = max. 10 μA; $V_{CE} \leqslant 30$ V; in case of system stop the output stage switches on and off with a cycle time of 0,4 s.

Organization of scratchpad memory and page register

The capacity of the scratchpad memory is 2k4, divided into 4 pages of 512 words each, see Fig. 5. Depending on the instruction the scratchpad memory is addressed word by word or bit by bit. The page numbers run from 0 to 3 and the addresses within a page from 000 to 511. When addressing word by word the address notation is 0000 to 0511, 1000 to 1511, 2000 to 2511 or 3000 to 3511. When addressing bit by bit the addresses run from 000.0 to 511.3. This bit by bit addressing can, basically, only be done on page 0; addressing on other pages is possible by using the page register. This register, which has the fixed address 0002, is connected in parallel with the scratchpad memory and is enabled by inserting a wire jump between points PBE on the module, see Fig. 6. When a number 1, 2 or 3 has been stored in this register, the succeeding bit by bit addressing is then carried out on the page indicated by the contents of the page register.
At the end of a DP-phase the contents of the page register is always set to zero, independent of whether the wire jump PBE has been inserted or not.

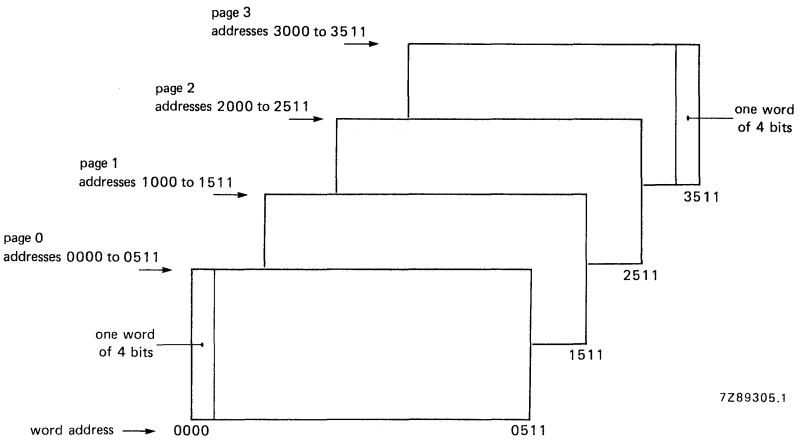


Fig. 5 Schematic presentation of the scratchpad memory.

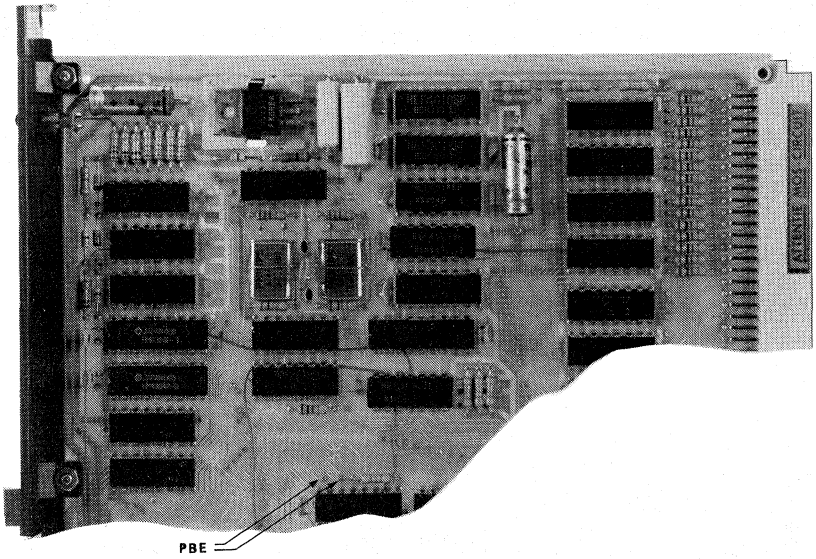


Fig. 6 Location of PBE points.

Fixed scratchpad memory addresses

address	description
000.0	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
→ 000.2	24 V alarm output (becomes 1 if $V_S \leqslant 17{,}5$ V).
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.
002.0 002.1	} Page register.

MECHANICAL DATA

Dimensions in mm

Outlines

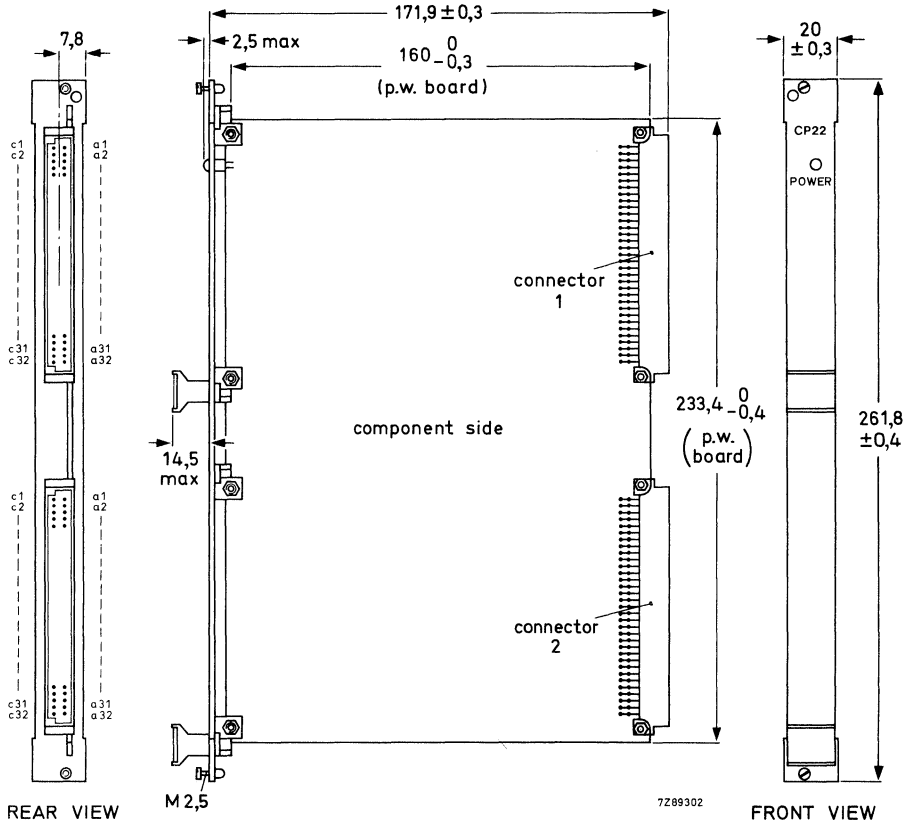


Fig. 7.

Mass approx. 270 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
PMB_0	1	INS_0	PABE	1	PABE
PMB_1	2	INS_1	PDBE	2	PDBE
PMB_2	3	INS_2	n.c.	3	n.c.
PMB_3	4	INS_3	CPSI	4	CPSI
PMB_4	5	INS_4	CPSC	5	CPSC
PMB_5	6	ADD_0	HOLD	6	HOLD
PMB_6	7	ADD_1	CLOCK	7	CLOCK
PMB_7	8	ADD_2	n.c.	8	n.c.
PMB_8	9	ADD_3	n.c.	9	n.c.
PMB_9	10	ADD_4	RSME	10	RSME
PMB_{10}	11	ADD_5	n.c.	11	n.c.
PMB_{11}	12	ADD_6	$\overline{RCP}$	12	$\overline{RCP}$
PMB_{12}	13	ADD_7	WPSM	13	WPSM
PMB_{13}	14	ADD_8	n.c.	14	n.c.
PMB_{14}	15	ADD_9	n.c.	15	n.c.
PMB_{15}	16	ADD_{10}	APM_0	16	APM_0
PB_1	17	PB_0	APM_1	17	APM_1
RR	18	RR	APM_2	18	APM_2
DIO_0	19	DIO_0	APM_3	19	APM_3
DIO_1	20	DIO_1	APM_4	20	APM_4
DIO_2	21	DIO_2	APM_5	21	APM_5
DIO_3	22	DIO_3	APM_6	22	APM_6
PHC_0	23	PHC_1	APM_7	23	APM_7
R/$\overline{WSM}$	24	PRF	APM_8	24	APM_8
0 V*	25	DEF	APM_9	25	APM_9
$\overline{SBI}$	26	APF	APM_{10}	26	APM_{10}
$\overline{RCO}$	27	PRFP	APM_{11}	27	APM_{11}
WECP	28	APFP	APM_{12}	28	APM_{12}
ALI	29	ALI	n.c.	29	n.c.
SRI −	30	SRI +	VB	30	VB
V_p	31	V_p	V_p	31	V_p
0 V	32	0 V	0 V	32	0 V

n.c. = not connected

* No supply line; is used as return line for control signals.

CENTRAL PROCESSOR

DESCRIPTION

The central processor CP24 is for use with other PC20 modules, to assemble a programmable controller. The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.

The central processor block diagram is given in Fig. 1. The *data processor* controls the system and the complete timing. It includes the instruction decoder, the 1-bit logic processor, the 4-bit arithmetic processor and the data control.

The *address processor* generates addresses for the program memory under program control. It also generates addresses for the input and output modules.

The *program memory* is a C-MOS RAM (2k16). The CP24 has on-board battery back-up and a provision to connect an external battery for longer memory retention.

The capacity of the *scratchpad memory* is ¼k4. Depending on the instruction the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3). In the latter case the address notation is, for example, 147.2 or 076.0. The on-board battery for data retention in the program memory RAM, is also used for data retention of the scratchpad memory.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.

The *reset scratchpad memory circuit* allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.

The *timer clock circuit* provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).

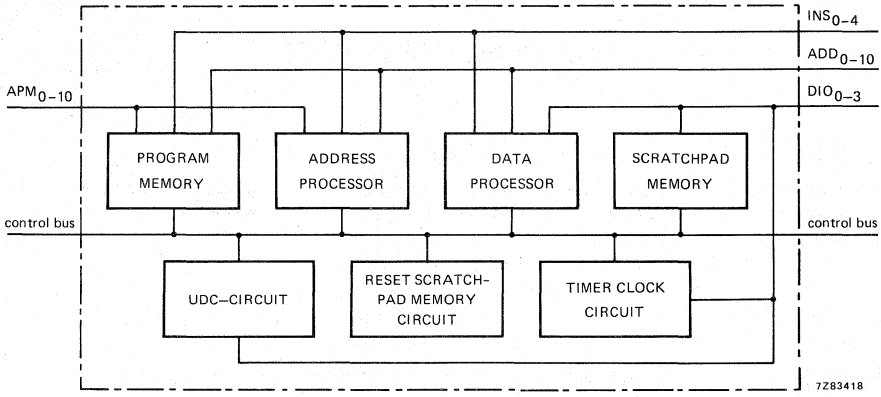


Fig. 1 Block diagram.

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC_0 and PHC_1, are:
- up-date and check phase (UDC): $PHC_0 = 0$, $PHC_1 = 0$;
- reset scratchpad memory (RSM): $PHC_0 = 1$, $PHC_1 = 0$;
- data processing (DP): $PHC_0 = 0$, $PHC_1 = 1$;
- up-date input/output (I/O): $PHC_0 = 1$, $PHC_1 = 1$.

Each central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

* For a general description of the Euro-card system see IEC297 or DIN41494 for 19-in racks and IEC130-14 or DIN41612 for connectors.

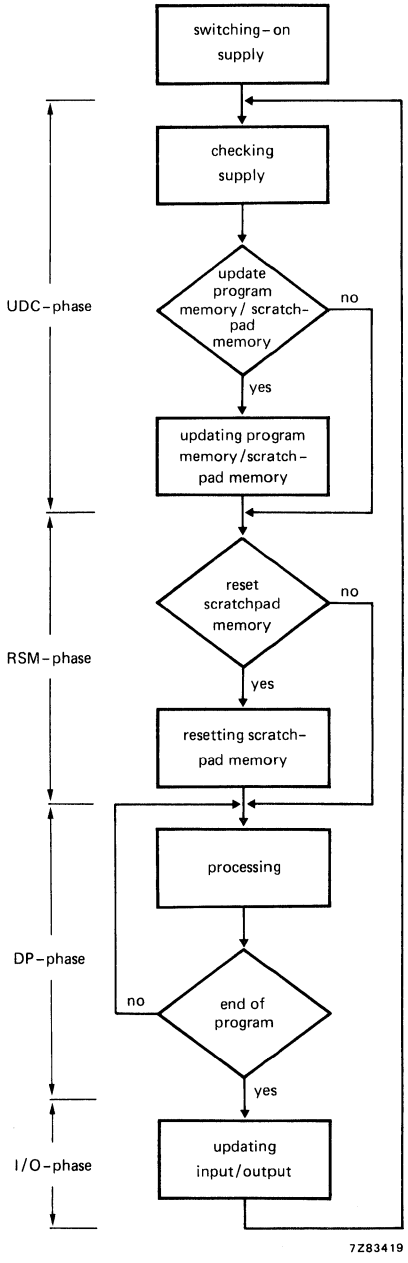


Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	10 V ± 10%
current	I_P	max. 250 mA

Requirements of the external battery to retain the contents of the program memory and the scratch-pad memory during power failure.

Battery voltage	V_B	3 to 4,5 V
Battery current (V_P = 0 V)	I_B	typ. 1,5 mA
Trickle charge current (V_P = 10 V)		typ. −5 mA
Data retention with on-board battery at 40 °C		typ. 30 h, provided the module is in operation for at least 20 h

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations (Fig. 5) connector 1	connector 2
BI-DIRECTIONAL BUSSES			
ADD_0	Address bus interconnected with PU21 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, c6	
ADD_1		a7, c7	
ADD_2		a8, c8	
ADD_3		a9, c9	
ADD_4		a10, c10	
ADD_5		a11, c11	
ADD_6		a12, c12	
ADD_7		a13, c13	
ADD_8		a14, c14	
ADD_9		a15, c15	
ADD_{10}		a16, c16	
APM_0	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).		a16, c16
APM_1			a17, c17
APM_2			a18, c18
APM_3			a19, c19
APM_4			a20, c20
APM_5			a21, c21
APM_6			a22, c22
APM_7			a23, c23
APM_8			a24, c24
APM_9			a25, c25
APM_{10}			a26, c26
APM_{11}	Pseudo address bits connected via resistor to 0 V.		a27, c27
APM_{12}			a28, c28
DIO_0	Data bus; receives data for scratchpad memory from input modules and PU21, transmits data from scratchpad memory to output modules and PU21; data bus is controlled by WEPC or by R/$\overline{W}$SM.	a19, c19	
DIO_1		a20, c20	
DIO_2		a21, c21	
DIO_3		a22, c22	

	function	terminations (Fig. 5)	
		connector 1	connector 2
INS_0 INS_1 INS_2 INS_3 INS_4	Instruction bus, interconnected with PU21; commanded by PDBE.	a1, c1 a2, c2 a3, c3 a4, c4 a5, c5	
INPUTS			
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29, c29	
CPSD	Central processor slow down; input commanded by PU21.		a3, c3
CPSI	Central processor stop initiate; command from PU21 stops central processor in UDC-phase (active HIGH).		a4, c4
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored (input current = −5 mA).	a25	
HOLD	Command from PU21 to stop central processor in DP-phase (active LOW).		a6, c6
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input.		a1, c1
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs.		a2, c2
PRF	Preparation input/output modules finished.	a24	
$\overline{RCP}$	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 4 mA.		a12, c12
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.		a10, c10
$\overline{R}$/WPM	Write signal from PU21 to central processor, to store data in program memory (active HIGH).		a14, c14

	function	terminations (Fig. 5)	
		connector 1	connector 2
R/$\overline{W}$SM	Read-write level from input and output modules; only effective during I/O-phase.	c24	
WEPC	Write enable signal from PU21; prepares central processor to store data from PU21 into scratchpad memory.	c28	
WPSM	Write pulse for scratchpad memory; signal from PU21 to store data on DIO_{0-3} into scratchpad memory.		a13, c13
OUTPUTS			
APF	Address processing for input and output modules finished; address stable.	a26	
CLOCK	Clock output to PU21.		a7, c7
CPSC	Central processor stop completed; command (HIGH) to PU21 indicating that central processor has been stopped in UDC-phase.		a5, c5
PB_0 PB_1	Page bits, connected to 0 V.	a17 c17	
PHC_0 PHC_1	Phase control to PU21 and input and output modules.	c23 a23	
$\overline{RCO}$	Reset output to output modules; becomes LOW during switch-on of the system, or if $\overline{RCP}$ is LOW. When a wire jump has been inserted between the RCO points on the module (Fig. 3), $\overline{RCO}$ output will also become LOW if $V_P < 9$ V or > 11 V.	c27	
RR	Result Register, interconnected with PU21.	a18, c18	
SBI	Storage command to store data on data bus into output modules and PU21.	c26	
SRI + SRI −	System run indication; Darlington transistor output, galvanically isolated by means of opto-coupler. SRI + = collector, SRI − = emitter. When the system runs the transistor is non conducting; when the system stops the transistor switches on and off (see for circuit diagram, Fig. 4).	a30 c30	

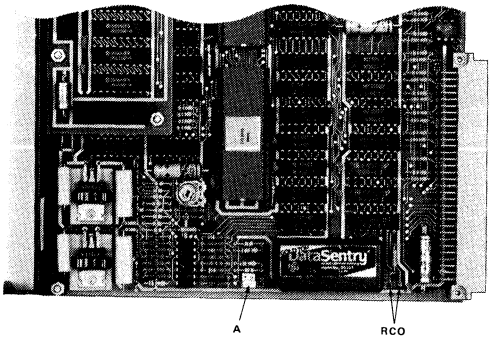


Fig. 3 Location of RCO points and jumper A of the on-board battery.

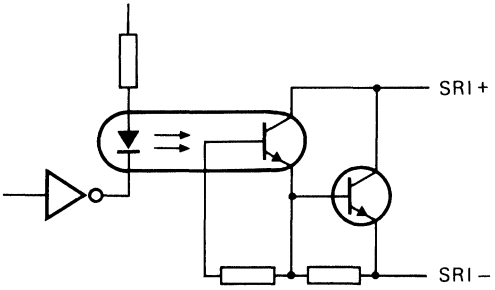


Fig. 4 Circuit diagram of SRI output. Transistor conducting: I_Q = max. 100 mA, $V_{CE} < 1{,}5$ V; transistor non-conducting: I_Q = max. 10 μA; $V_{CE} \leqslant 30$ V; in case of system stop the output stage switches on and off with a cycle time of 0,4 s.

Fixed scratchpad memory addresses

address	description
000.0	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
000.2	24 V alarm output (becomes 1 if $V_S \leqslant 17{,}5$ V).
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.

MECHANICAL DATA

Dimensions in mm

Outlines

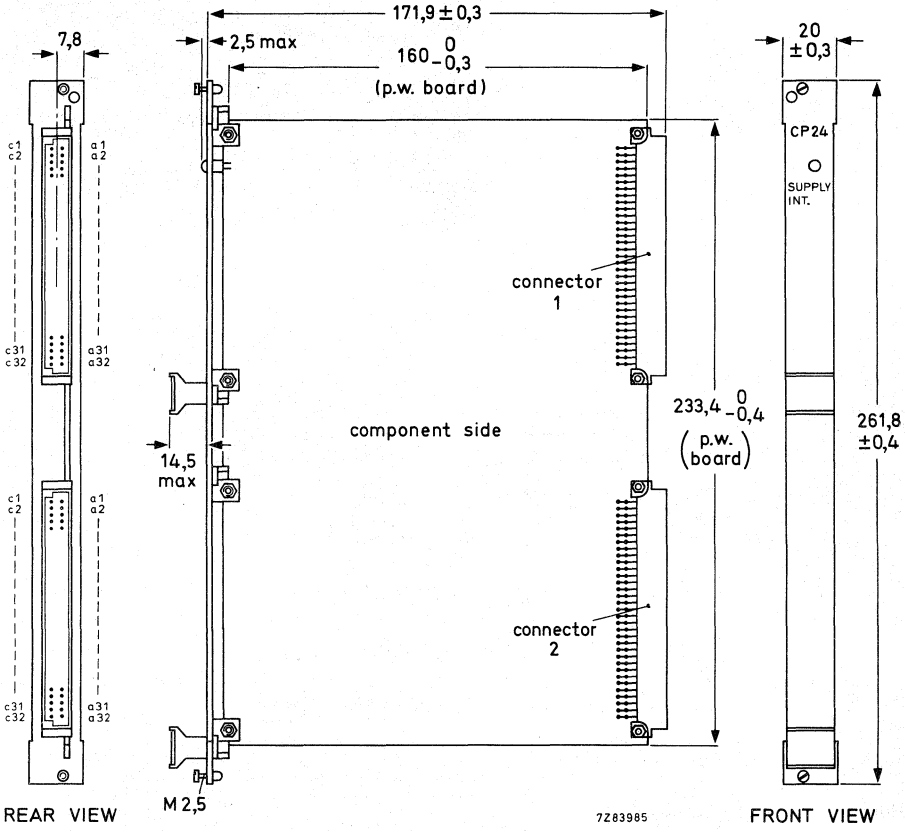


Fig. 5.

Mass approx. 270 g

Notes

1. At delivery of the central processor the on-board battery is switched off (jumper A, Fig. 3, in off-position).
2. If the central processor is removed from the rack, ensure that it is put on an insulated surface to prevent short-circuiting of the on-board battery.

Terminal location

connector 1		
row c		row a
INS_0	1	INS_0
INS_1	2	INS_1
INS_2	3	INS_2
INS_3	4	INS_3
INS_4	5	INS_4
ADD_0	6	ADD_0
ADD_1	7	ADD_1
ADD_2	8	ADD_2
ADD_3	9	ADD_3
ADD_4	10	ADD_4
ADD_5	11	ADD_5
ADD_6	12	ADD_6
ADD_7	13	ADD_7
ADD_8	14	ADD_8
ADD_9	15	ADD_9
ADD_{10}	16	ADD_{10}
PB_1	17	PB_0
RR	18	RR
DIO_0	19	DIO_0
DIO_1	20	DIO_1
DIO_2	21	DIO_2
DIO_3	22	DIO_3
PHC_0	23	PHC_1
R/$\overline{W}$SM	24	PRF
0 V*	25	DEF
SBI	26	APF
$\overline{RCO}$	27	n.c.
WEPC	28	n.c.
ALI	29	ALI
SRI–	30	SRI +
V_p	31	V_p
0 V	32	0 V

connector 2		
row c		row a
PABE	1	PABE
PDBE	2	PDBE
CPSD	3	CPSD
CPSI	4	CPSI
CPSC	5	CPSC
HOLD	6	HOLD
CLOCK	7	CLOCK
n.c.	8	n.c.
n.c.	9	n.c.
RSME	10	RSME
n.c.	11	n.c.
$\overline{RCP}$	12	$\overline{RCP}$
WPSM	13	WPSM
$\overline{R}$/WPM	14	$\overline{R}$/WPM
n.c.	15	n.c.
APM_0	16	APM_0
APM_1	17	APM_1
APM_2	18	APM_2
APM_3	19	APM_3
APM_4	20	APM_4
APM_5	21	APM_5
APM_6	22	APM_6
APM_7	23	APM_7
APM_8	24	APM_8
APM_9	25	APM_9
APM_{10}	26	APM_{10}
APM_{11}	27	APM_{11}
APM_{12}	28	APM_{12}
n.c.	29	n.c.
VB	30	VB
V_p	31	V_p
0 V	32	0 V

n.c. = not connected.

* No supply line; is used as return line for control signals.

INPUT MODULE

DESCRIPTION

This input module is used with the other PC20 modules to assemble a programmable controller.

The input module contains 16 addressable input stages, with photo-isolators between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. Each input stage has a LED for status indication: it is lit when the input is active. Furthermore, to limit power consumption, these LEDs can be switched-off. A delay circuit (symmetrical delay time typ. 1 ms) is incorporated in each input stage to increase the noise immunity. The delay time can be increased by adding extra capacitance.

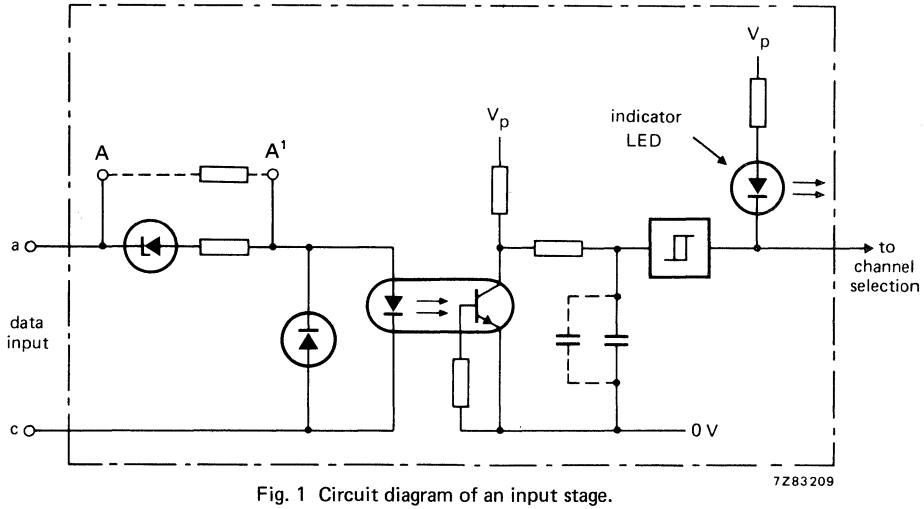


Fig. 1 Circuit diagram of an input stage.

Each input module has 11 address inputs (ADD_{0-10}) and 9 module identification inputs (MID_{1-9}), which are accessible on the connectors at the rear (Fig. 2).

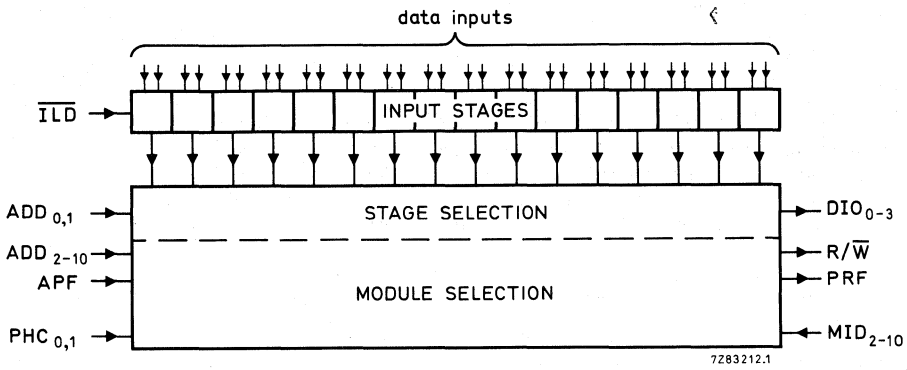


Fig. 2 Block diagram of the input module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard).

The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89291 (pins for wire wrapping), 2422 025 89299 (pins for dip-soldering) or 2422 025 89327 (solder tags).*

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	10	V ± 10%
current	I_P	typ. 45	mA (all inputs inactive)
		typ. 175	mA (all inputs active)
		max. 200	mA (all inputs active)

Input data

The data inputs are $DI_{W.0}$ to $DI_{W.3}$, $DI_{X.0}$ to $DI_{X.3}$, $DI_{Y.0}$ to $DI_{Y.3}$ and $DI_{Z.0}$ to $DI_{Z.3}$. They are accessible on connector 2, see "Terminal location".

		5 V level (note 2)	24 V level
Active voltage (V_{a-c})	note 1	3,5 to 6 V	17 to 30 V
Non-active voltage (V_{a-c})	note 1	0 to 0,8 V or floating	0 to 7 V or floating
Input current, active at V_{a-c} = 5 V or 24 V resp.		typ. 10 mA	typ. 10 mA

The delay time of the delay circuit can be increased by inserting capacitors (approx. 0,015 μF/ms) between connecting points B and B' (Fig. 3).

Notes

1. V_{a-c} is the voltage between terminal of row a and terminal of row c of connector 2.
2. For 5 V-level operation a resistor of 360 Ω ± 5%, style CR25, has to be connected to each input stage between connecting points A and A' (Fig. 3).

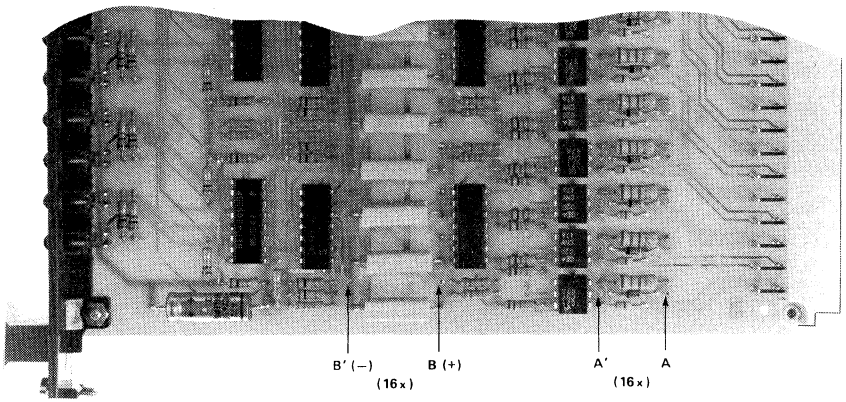


Fig. 3 Part of the printed-wiring board, showing the connecting points for the additional delay capacitors and the resistors for 5 V-level operation.

The inputs mentioned below meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 4)
ADD_0	Address bits from central processor: ADD_{0-1} select a group of 4 input stages, ADD_{2-10} select the input module.	c11
ADD_1		a11
ADD_2		c12
ADD_3		a12
ADD_4		c13
ADD_5		a13
ADD_6		c14
ADD_7		a14
ADD_8		c15
ADD_9		a15
ADD_{10}		c16
MID_2	Module identification inputs; provide module with individual identity.	c2
MID_3		c3
MID_4		c4
MID_5		c5
MID_6		c6
MID_7		c7
MID_8		c8
MID_9		c9
MID_{10}		c10
APF	Handshake signal; input/output address correct.	a26
PHC_0	Phase control signals.	c23
PHC_1		a23
$\overline{ILD}$	Indication LED disable; input current LOW: 0,1 mA	c28

Output data

All outputs meet the standard LOCMOS specifications, except the R/$\overline{W}$ and PRF outputs.

output	function	terminations of connector 1 (Fig. 4)
DIO_0	Data bits to central processor; data is stored in scratchpad memory of central processor.	c21
DIO_1		a21
DIO_2		c22
DIO_3		a22
R/$\overline{W}$	Signal to central processor (active LOW); prepares central processor for data on DIO_{0-3} to be written in the scratchpad memory (open collector output).	c24
PRF	Preparation of input module finished (open collector output).	a24

MECHANICAL DATA

Dimensions in mm

Outlines

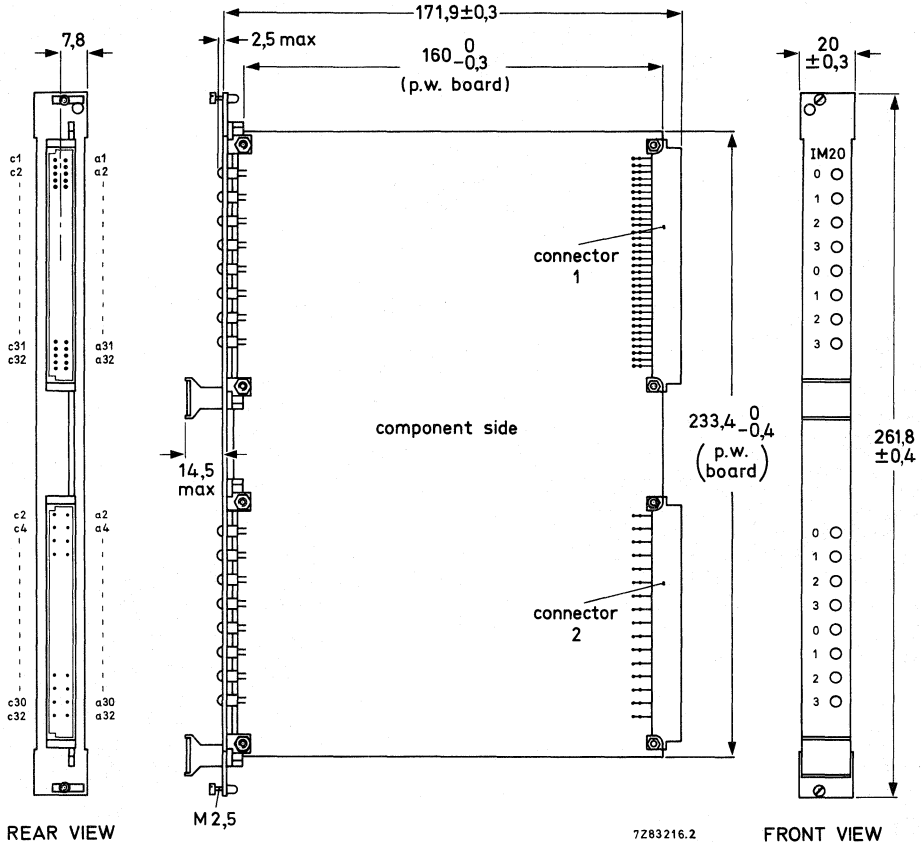


Fig. 4.

Mass 250 g

Terminal location

connector 1				connector 2		
row c		row a		row c		row a
n.c.	1	HIGH level	**	$DI_{W.0}$	2	$DI_{W.0}$
MID_2	2	HIGH level		$DI_{W.1}$	4	$DI_{W.1}$
MID_3	3	HIGH level		$DI_{W.2}$	6	$DI_{W.2}$
MID_4	4	HIGH level		$DI_{W.3}$	8	$DI_{W.3}$
MID_5	5	HIGH level		$DI_{X.0}$	10	$DI_{X.0}$
MID_6	6	HIGH level		$DI_{X.1}$	12	$DI_{X.1}$
MID_7	7	HIGH level		$DI_{X.2}$	14	$DI_{X.2}$
MID_8	8	HIGH level		$DI_{X.3}$	16	$DI_{X.3}$
MID_9	9	HIGH level		$DI_{Y.0}$	18	$DI_{Y.0}$
MID_{10}	10	HIGH level		$DI_{Y.1}$	20	$DI_{Y.1}$
ADD_0	11	ADD_1		$DI_{Y.2}$	22	$DI_{Y.2}$
ADD_2	12	ADD_3		$DI_{Y.3}$	24	$DI_{Y.3}$
ADD_4	13	ADD_5		$DI_{Z.0}$	26	$DI_{Z.0}$
ADD_6	14	ADD_7		$DI_{Z.1}$	28	$DI_{Z.1}$
ADD_8	15	ADD_9		$DI_{Z.2}$	30	$DI_{Z.2}$
ADD_{10}	16	n.c.		$DI_{Z.3}$	32	$DI_{Z.3}$
n.c.	17	n.c.				
n.c.	18	n.c.				
n.c.	19	n.c.				
n.c.	20	n.c.				
DIO_0	21	DIO_1				
DIO_2	22	DIO_3				
PHC_0	23	PHC_1				
R/$\overline{W}$	24	PRF				
0 V *	25	n.c.				
n.c.	26	APF				
n.c.	27	n.c.				
$\overline{ILD}$	28	n.c.				
n.c.	29	n.c.				
n.c.	30	n.c.				
V_P	31	V_P				
0 V	32	0 V				

n.c. = not connected.

* No supply line; is used as return line for control signals.
** For coding MID lines.

PROGRAM MEMORY MODULE

DESCRIPTION

This memory module is for use with central processor CP22 and other PC20 modules to assemble a programmable controller.

The MM20 is an 8 k 16 EPROM memory. It is supplied with 8 empty EPROMs, type 2716, which can be programmed on the programming unit PU20.

The 8 IC-sockets for the EPROMs are marked 0-1, 2-3, 4-5, or 6-7, for A and B type EPROMs, indicating the address range of the socket.

EPROMs should be inserted into the sockets as follows:
EPROMs (A and B) with addresses 0000 to 2047 into sockets 0-1 (A and B);
EPROMs (A and B) with addresses 2048 to 4095 into sockets 2-3 (A and B);
EPROMs (A and B) with addresses 4096 to 6143 into sockets 4-5 (A and B);
EPROMs (A and B) with addresses 6144 to 8191 into sockets 6-7 (A and B).

The memory module is built on a glass-epoxy double Euro-card* (233,4 mm x 160 mm) with two F068-1 connectors (male parts); the corresponding female parts are on the back panels.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P 10 V ± 10%
current	I_P max. 550 mA (module filled with 8 EPROMs)

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations (Fig. 2)	
		connector 1	connector 2
INPUTS			
APFP	Address processing finished; when LOW addresses may change.	a28	
APM_0	Address bits for program memory.		a16, c16
APM_1			a17, c17
APM_2			a18, c18
APM_3			a19, c19
APM_4			a20, c20
APM_5			a21, c21
APM_6			a22, c22
APM_7			a23, c23
APM_8			a24, c24
APM_9			a25, c25
APM_{10}			a26, c26
APM_{11}			a27, c27
APM_{12}			a28, c28
PHC_0	Phase control line.	c23	
OUTPUTS			
PMB_0	03 EPROM A	c1	
PMB_1	04 EPROM A	c2	
PMB_2	05 EPROM A	c3	
PMB_3	06 EPROM A	c4	
PMB_4	07 EPROM A	c5	
PMB_5	00 EPROM B	c6	
PMB_6	01 EPROM B	c7	
PMB_7	02 EPROM B	c8	
PMB_8	03 EPROM B	c9	
PMB_9	04 EPROM B	c10	
PMB_{10}	05 EPROM B	c11	
PMB_{11}	06 EPROM B	c12	
PMB_{12}	07 EPROM B	c13	
PMB_{13}	00 EPROM A	c14	
PMB_{14}	01 EPROM A	c15	
PMB_{15}	02 EPROM A	c16	
	Program memory data bits; n-p-n transistor outputs with pull-up resistor (4,7 kΩ)		
PRFP	Output indicating that preparation for reading data has been finished and data is available on outputs $PMB_{0\text{-}15}$ (active when PHC_0 is LOW).	a27	

Time data

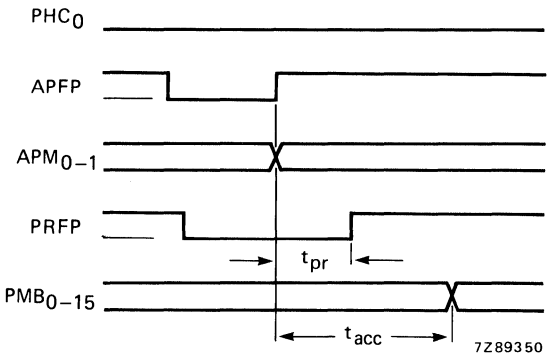


Fig. 1 Read-out of program memory during DP-phase.

Preparation time	t_{pr}	max.	350 ns
Access time	t_{acc}	max.	525 ns

MECHANICAL DATA

Dimensions in mm

Outlines

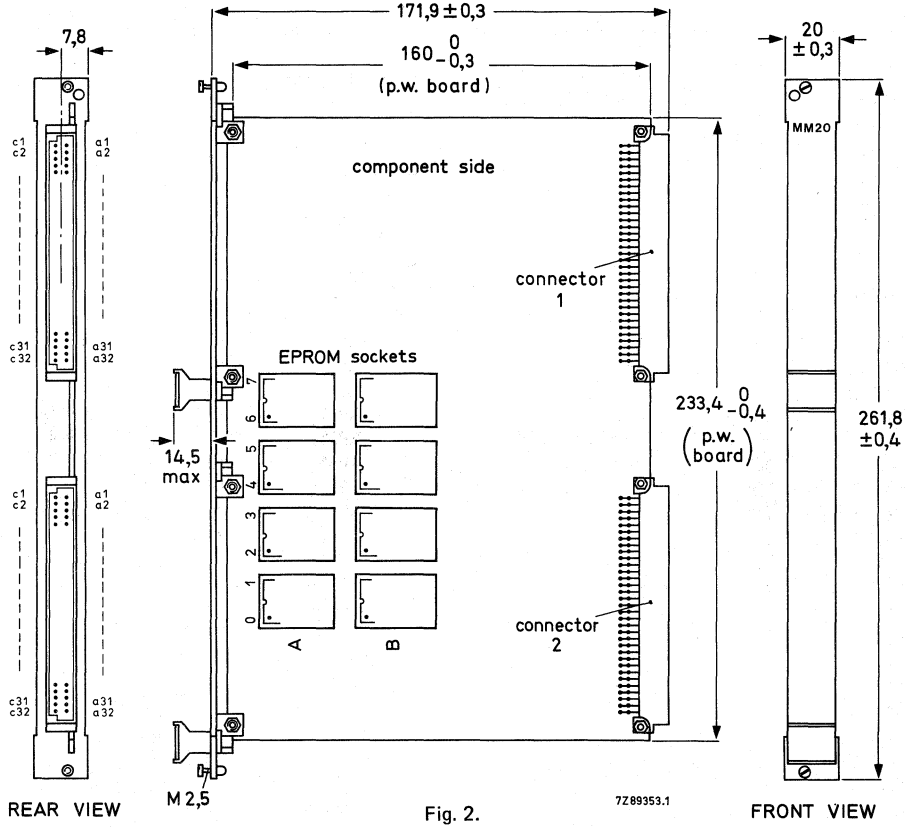


Fig. 2.

Mass approx. 310 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
PMB_0	1	n.c.	n.c.	1	n.c.
PMB_1	2	n.c.	n.c.	2	n.c.
PMB_2	3	n.c.	n.c.	3	n.c.
PMB_3	4	n.c.	n.c.	4	n.c.
PMB_4	5	n.c.	n.c.	5	n.c.
PMB_5	6	n.c.	n.c.	6	n.c.
PMB_6	7	n.c.	n.c.	7	n.c.
PMB_7	8	n.c.	n.c.	8	n.c.
PMB_8	9	n.c.	n.c.	9	n.c.
PMB_9	10	n.c.	n.c.	10	n.c.
PMB_{10}	11	n.c.	n.c.	11	n.c.
PMB_{11}	12	n.c.	n.c.	12	n.c.
PMB_{12}	13	n.c.	n.c.	13	n.c.
PMB_{13}	14	n.c.	n.c.	14	n.c.
PMB_{14}	15	n.c.	n.c.	15	n.c.
PMB_{15}	16	n.c.	APM_0	16	APM_0
n.c.	17	n.c.	APM_1	17	APM_1
n.c.	18	n.c.	APM_2	18	APM_2
n.c.	19	n.c.	APM_3	19	APM_3
n.c.	20	n.c.	APM_4	20	APM_4
n.c.	21	n.c.	APM_5	21	APM_5
n.c.	22	n.c.	APM_6	22	APM_6
PHC_0	23	n.c.	APM_7	23	APM_7
n.c.	24	n.c.	APM_8	24	APM_8
n.c.	25	n.c.	APM_9	25	APM_9
n.c.	26	n.c.	APM_{10}	26	APM_{10}
n.c.	27	PRFP	APM_{11}	27	APM_{11}
n.c.	28	APFP	APM_{12}	28	APM_{12}
n.c.	29	n.c.	n.c.	29	n.c.
n.c.	30	n.c.	n.c.	30	n.c.
V_p	31	V_p	V_p	31	V_p
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

PROGRAM MEMORY MODULES

DESCRIPTION

These memory modules are for use with central processor CP22 and other PC20 modules to assemble a programmable controller.

The two modules are identical, except for the program memory capacity: 8 k 16 C-MOS RAM for the MM21, 4 k 16 C-MOS RAM for the MM22. The modules have an on-board battery for data retention (30 h) in case the supply voltage is switched off. An external battery can be connected for longer memory retention.

Each module is built on a glass-epoxy double Euro-card* (233,4 mm x 160 mm) with two F068-I connectors (male parts); the corresponding female parts are on the back panels.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_P	10 V ± 10%
current	I_P	typ. 110 mA max. 150 mA
Requirements of the back-up battery		
Battery voltage	V_B	3 to 4,5 V
Battery current (V_P = 0 V)	I_B	typ. 1,5 mA
Trickle charge current (V_P = 10 V)		typ. –5 mA
Data retention with on-board battery at 40 °C		typ. 30 h, provided the module has been in operation for at least 20 h.

Note

When the supply voltage drops below 7 V the C-MOS RAM memory is automatically switched to the stand-by position, so that the battery can take over the supply of the memory as soon as V_P falls below V_B.

* For a general description of the Euro-card system see IEC 127 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations (Fig. 3)	
		connector 1	connector 2
INPUTS			
APFP	Address processing finished; when LOW addresses may change, when goes HIGH address on APM_{0-12} is clocked into the address latch in the RAM (active when PHC_0 is LOW).	a28	
APM_0	Address bits for program memory.		a16, c16
APM_1			a17, c17
APM_2			a18, c18
APM_3			a19, c19
APM_4			a20, c20
APM_5			a21, c21
APM_6			a22, c22
APM_7			a23, c23
APM_8			a24, c24
APM_9			a25, c25
APM_{10}			a26, c26
APM_{11}			a27, c27
APM_{12}			a28, c28
PABE	Input to clock address on APM_{0-12} into the address latch in the RAM.		a1, c1
PHC_0	Phase control lines	c23	
PHC_1		a23	
$PMBI_0$	Data inputs for program memory bits.	a1	
$PMBI_1$		a2	
$PMBI_2$		a3	
$PMBI_3$		a4	
$PMBI_4$		a5	
$PMBI_5$		a6	
$PMBI_6$		a7	
$PMBI_7$		a8	
$PMBI_8$		a9	
$PMBI_9$		a10	
$PMBI_{10}$		a11	
$PMBI_{11}$		a12	
$PMBI_{12}$		a13	
$PMBI_{13}$		a14	
$PMBI_{14}$		a15	
$PMBI_{15}$		a16	
$\overline{R}/W$	Read/write input. When HIGH data on $PMBI_{0-15}$ is written into the RAM only when PHC_0 and PHC_1 are LOW.		a14, c14

	function	terminations (Fig. 3)	
		connector 1	connector 2
OUTPUTS			
PMB_0	Data output of program memory. The output stage is built-up with transistor drive circuit with pull-up resistor (2,2 kΩ). The sink capability is max. 3 mA.	c1	
PMB_1		c2	
PMB_2		c3	
PMB_3		c4	
PMB_4		c5	
PMB_5		c6	
PMB_6		c7	
PMB_7		c8	
PMB_8		c9	
PMB_9		c10	
PMB_{10}		c11	
PMB_{11}		c12	
PMB_{12}		c13	
PMB_{13}		c14	
PMB_{14}		c15	
PMB_{15}		c16	
PRFP	Output indicating that preparation for reading data has been finished and data is available on outputs $PMB_{0\text{-}15}$ (active when PHC_0 is LOW).	a27	

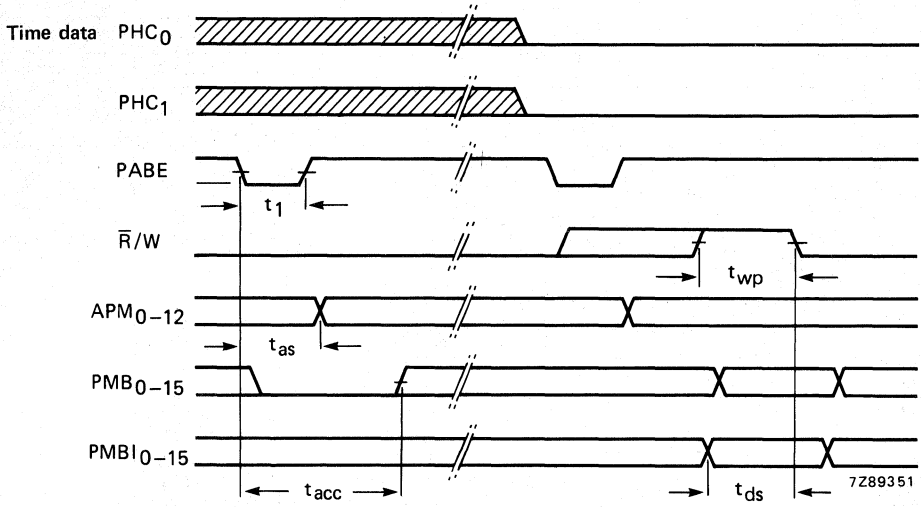


Fig. 1 Read/write cycle during UDC-phase.

Pulse width for RAM address latch	t_1	min.	50 ns
Address setting time	t_{as}	max.	200 ns
Access time	t_{acc}	max.	1 µs
Write pulse width	t_{wp}	min.	600 ns
Data stable	t_{ds}	min.	500 ns

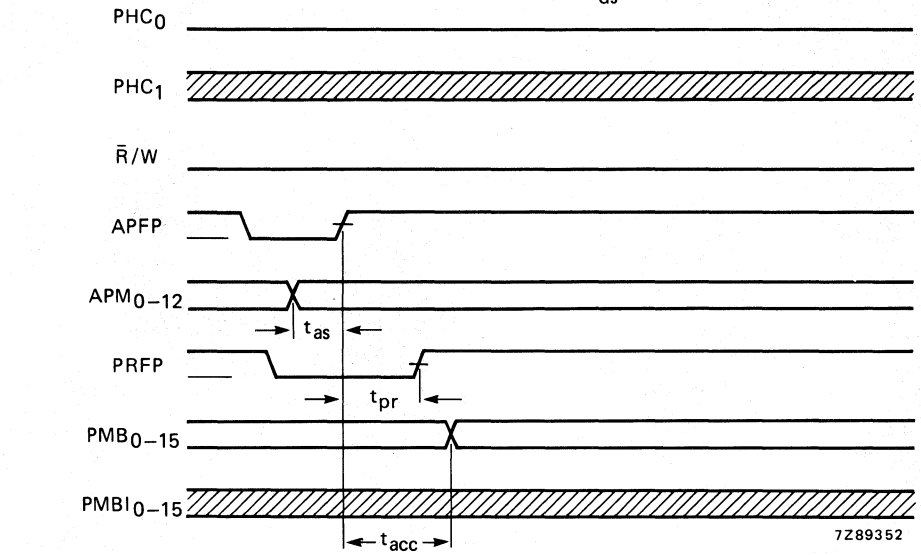


Fig. 2 Read cycle during DP-phase.

Address setting time	t_{as}	min.	0 ns
Preparation time	t_{pr}	max.	350 ns
Access time	t_{acc}	max.	600 ns

MECHANICAL DATA

Dimensions in mm

Outlines

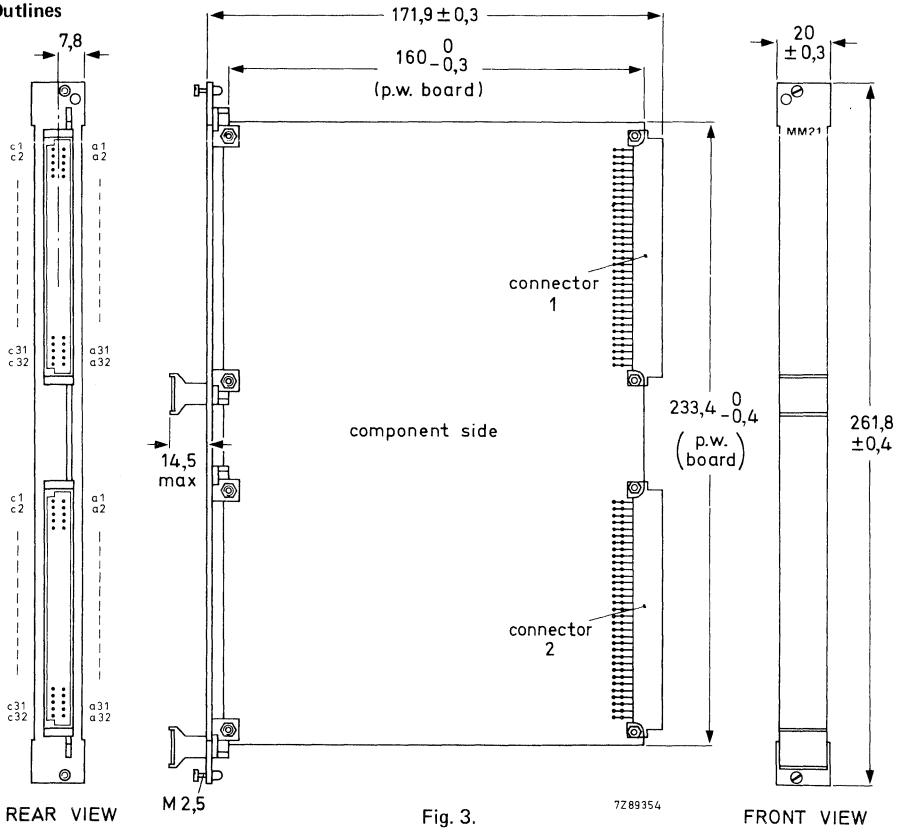


Fig. 3.

Mass approx. 270 g

Notes

1. When the program memory module is delivered, the on-board battery is switched off (jumper A, Fig. 4).

2. If the program memory module is removed from the rack, ensure that it is placed on an insulated surface to prevent short-circuiting of the on-board battery.

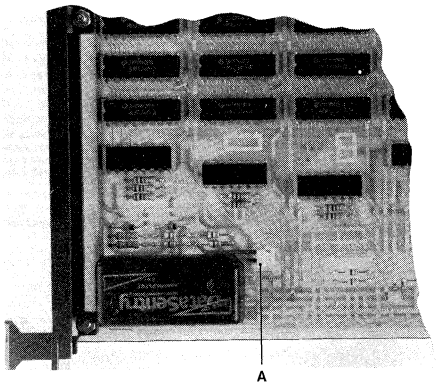


Fig. 4.

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
PMB_0	1	$PMBI_0$	PABE	1	PABE
PMB_1	2	$PMBI_1$	n.c.	2	n.c.
PMB_2	3	$PMBI_2$	n.c.	3	n.c.
PMB_3	4	$PMBI_3$	n.c.	4	n.c.
PMB_4	5	$PMBI_4$	n.c.	5	n.c.
PMB_5	6	$PMBI_5$	n.c.	6	n.c.
PMB_6	7	$PMBI_6$	n.c.	7	n.c.
PMB_7	8	$PMBI_7$	n.c.	8	n.c.
PMB_8	9	$PMBI_8$	n.c.	9	n.c.
PMB_9	10	$PMBI_9$	n.c.	10	n.c.
PMB_{10}	11	$PMBI_{10}$	n.c.	11	n.c.
PMB_{11}	12	$PMBI_{11}$	n.c.	12	n.c.
PMB_{12}	13	$PMBI_{12}$	n.c.	13	n.c.
PMB_{13}	14	$PMBI_{13}$	$\overline{R}/W$	14	$\overline{R}/W$
PMB_{14}	15	$PMBI_{14}$	n.c.	15	n.c.
PMB_{15}	16	$PMBI_{15}$	APM_0	16	APM_0
n.c.	17	n.c.	APM_1	17	APM_1
n.c.	18	n.c.	APM_2	18	APM_2
n.c.	19	n.c.	APM_3	19	APM_3
n.c.	20	n.c.	APM_4	20	APM_4
n.c.	21	n.c.	APM_5	21	APM_5
n.c.	22	n.c.	APM_6	22	APM_6
PHC_0	23	PHC_1	APM_7	23	APM_7
n.c.	24	n.c.	APM_8	24	APM_8
n.c.	25	n.c.	APM_9	25	APM_9
n.c.	26	n.c.	APM_{10}	26	APM_{10}
n.c.	27	PRFP	APM_{11}	27	APM_{11}
n.c.	28	APFP	APM_{12}	28	APM_{12}
n.c.	29	n.c.	n.c.	29	n.c.
n.c.	30	n.c.	VB	30	VB
V_p	31	V_p	V_p	31	V_p
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

OUTPUT MODULE

DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.

The output module contains 16 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs have grounded loads. Each output stage has a flywheel diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages have electronic short-circuit protection with automatic reset.

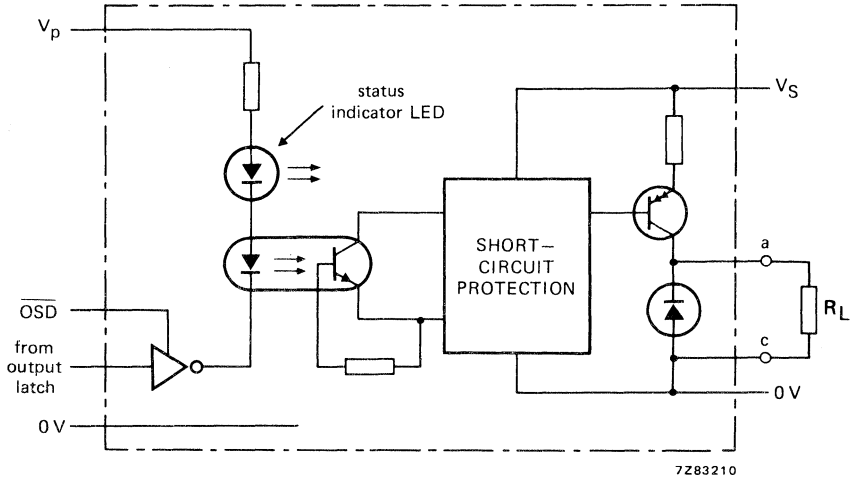


Fig. 1 Circuit diagram of an output stage.

→ The output module has 11 address inputs (ADD_{0-10}) and 9 module identification inputs (MID_{2-10}), which are accessible on the connectors at the rear (Fig. 2).

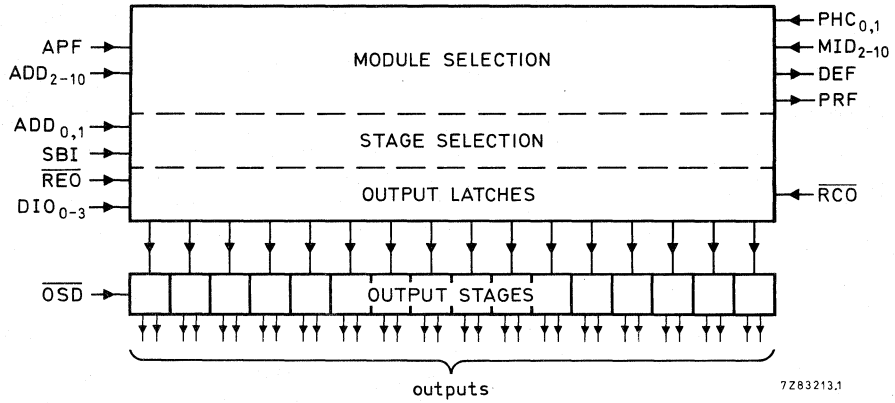


Fig. 2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard).

The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	logic	V_P	10 V ± 10%
Supply current	logic	I_P	typ. 120 mA (all stages ON)
			max. 150 mA (all stages ON)
			typ. 25 mA (all stages OFF)
Supply voltage (d.c.)	for output circuitry	V_S	24 ± 25%**
Supply current (excluding load current)	for output circuitry	I_S	typ. 75 mA (all stages ON)
			max. 110 mA (all stages ON)
			typ. 50 mA (all stages OFF)

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

** If V_S drops below 16 V, all output stages are forced into the non-conducting state for protection of the output circuitry.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 3)
ADD_0	Address bits from central processor; ADD_{0-1} select a group of four output stages, ADD_{2-10} select the output module.	c11
ADD_1		a11
ADD_2		c12
ADD_3		a12
ADD_4		c13
ADD_5		a13
ADD_6		c14
ADD_7		a14
ADD_8		c15
ADD_9		a15
ADD_{10}		c16
DIO_0	Data bits from central processor; data are stored in output stages by SBI.	c21
DIO_1		a21
DIO_2		c22
DIO_3		a22
$\overline{REO}$	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current LOW: 10 mA.	a27
$\overline{RCO}$	Reset from central processor (low level) during switch-on.	c27
MID_2	Module identification inputs; provide module with individual identity.	c2
MID_3		c3
MID_4		c4
MID_5		c5
MID_6		c6
MID_7		c7
MID_8		c8
MID_9		c9
MID_{10}		c10
SBI	Clock signal from central processor to output module, stores data on DIO_{0-3} into output stages during input/output cycle.	c26
PHC_0	Phase control signals.	c23
PHC_1		a23
APF	Handshake signal; input/output address correct.	a26
$\overline{OSD}$	Output stage disable for all stages; input current LOW: 10 mA.	a28

Output data

The data outputs are $DO_{W.0}$ to $DO_{W.3}$, $DO_{X.0}$ to $DO_{X.3}$, $DO_{Y.0}$ to $DO_{Y.3}$ and $DO_{Z.0}$ to $DO_{Z.3}$. They are accessible on connector 2, see "Terminal location".

Minimum load resistance $R_L = 48\ \Omega$.

Output transistor conducting: $R_L = 48\ \Omega$; $V_{a\text{-}c}$* = min. $V_S - 1{,}5$ V.
Output transistor non-conducting: I_o = max. 2 mA at $V_S = 30$ V.

The outputs are continuously tested for short-circuiting. As soon as the short-circuiting is removed, the output stage is automatically reset to normal operation.

Output current (limited to 6A per module)
for all stages — max. 0,375 A per stage
for maximum 12 stages — max. 0,5 A per stage

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 3)
PRF	Preparation of output module finished.	a24
DEF	Data exchange finished.	a25

* Voltage between terminal of row a and terminal of row c of connector 2.

MECHANICAL DATA

Dimensions in mm

Outlines

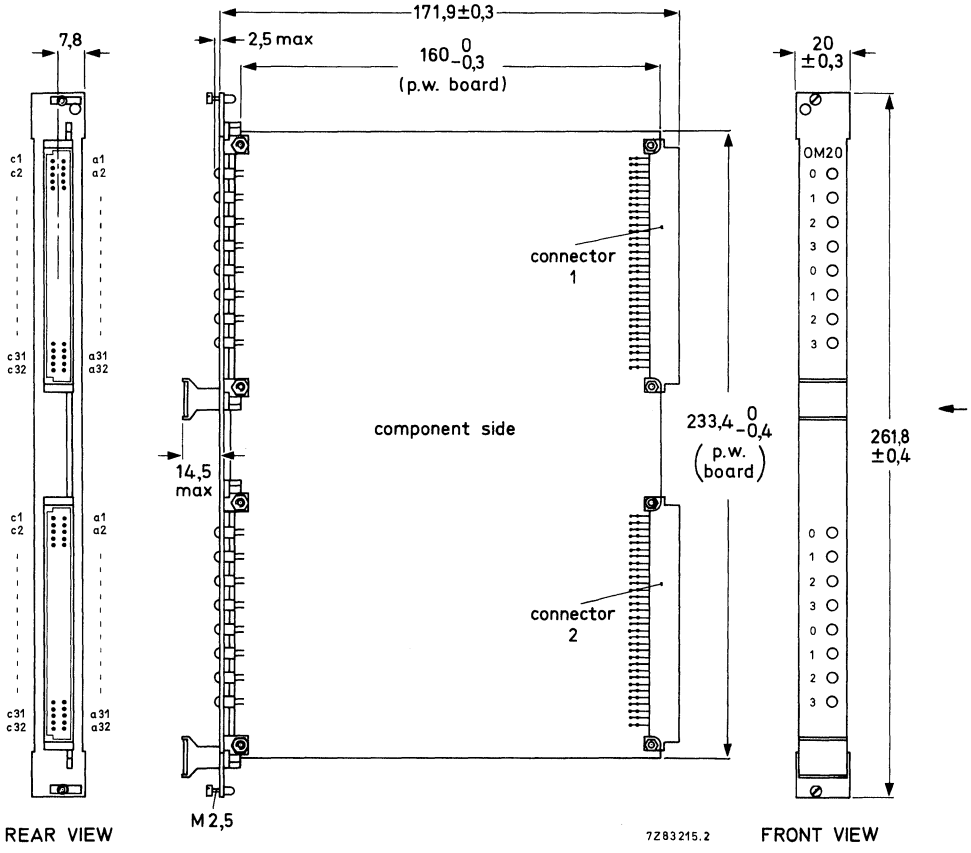


Fig. 3.

Mass 230 g

Terminal location

connector 1				connector 2		
row c		row a		row c		row a
n.c.	1	HIGH level	**	0 V	1	V_S
MID_2	2	HIGH level		$DO_{W.0}$	2	$DO_{W.0}$
MID_3	3	HIGH level		0 V	3	V_S
MID_4	4	HIGH level		$DO_{W.1}$	4	$DO_{W.1}$
MID_5	5	HIGH level		0 V	5	V_S
MID_6	6	HIGH level		$DO_{W.2}$	6	$DO_{W.2}$
MID_7	7	HIGH level		0 V	7	V_S
MID_8	8	HIGH level		$DO_{W.3}$	8	$DO_{W.3}$
MID_9	9	HIGH level		0 V	9	V_S
MID_{10}	10	HIGH level		$DO_{X.0}$	10	$DO_{X.0}$
ADD_0	11	ADD_1		0 V	11	V_S
ADD_2	12	ADD_3		$DO_{X.1}$	12	$DO_{X.1}$
ADD_4	13	ADD_5		0 V	13	V_S
ADD_6	14	ADD_7		$DO_{X.2}$	14	$DO_{X.2}$
ADD_8	15	ADD_9		0 V	15	V_S
ADD_{10}	16	n.c.		$DO_{X.3}$	16	$DO_{X.3}$
n.c.	17	n.c.		0 V	17	V_S
n.c.	18	n.c.		$DO_{Y.0}$	18	$DO_{Y.0}$
n.c.	19	n.c.		0 V	19	V_S
n.c.	20	n.c.		$DO_{Y.1}$	20	$DO_{Y.1}$
DIO_0	21	DIO_1		0 V	21	V_S
DIO_2	22	DIO_3		$DO_{Y.2}$	22	$DO_{Y.2}$
PHC_0	23	PHC_1		0 V	23	V_S
n.c.	24	PRF		$DO_{Y.3}$	24	$DO_{Y.3}$
0 V *	25	DEF		0 V	25	V_S
$\overline{SBI}$	26	APF		$DO_{Z.0}$	26	$DO_{Z.0}$
$\overline{RCO}$	27	$\overline{REO}$		0 V	27	V_S
n.c.	28	$\overline{OSD}$		$DO_{Z.1}$	28	$DO_{Z.1}$
n.c.	29	n.c.		0 V	29	V_S
n.c.	30	n.c.		$DO_{Z.2}$	30	$DO_{Z.2}$
V_P	31	V_P		0 V	31	V_S
0 V	32	0 V		$DO_{Z.3}$	32	$DO_{Z.3}$

n.c. = not connected.

Note
Supply-voltage lines (V_S) have to be connected to each group of 4 outputs.

* No supply line; is used as return line for control signals.
** For coding MID lines.

OUTPUT MODULE

DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.

The output module contains 8 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs are grounded load outputs. Each output stage has a voltage regulator diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages feature electronic short-circuit protection, i.e. when a short circuit occurs the relevant output stage is switched off automatically, and is indicated via the short-circuit indication output (SCI). After removing the short circuit the output stage can be reactivated via the REO input.

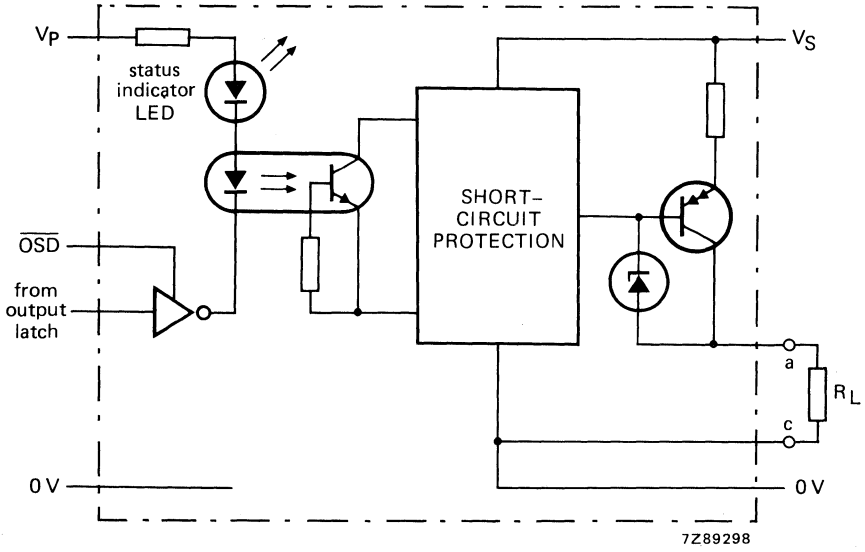


Fig. 1 Circuit diagram of an output stage.

The output module has 11 address inputs (ADD_{0-10}) and 10 module identification inputs (MID_{1-10}) which are accessible on the connectors at the rear (Fig. 2).

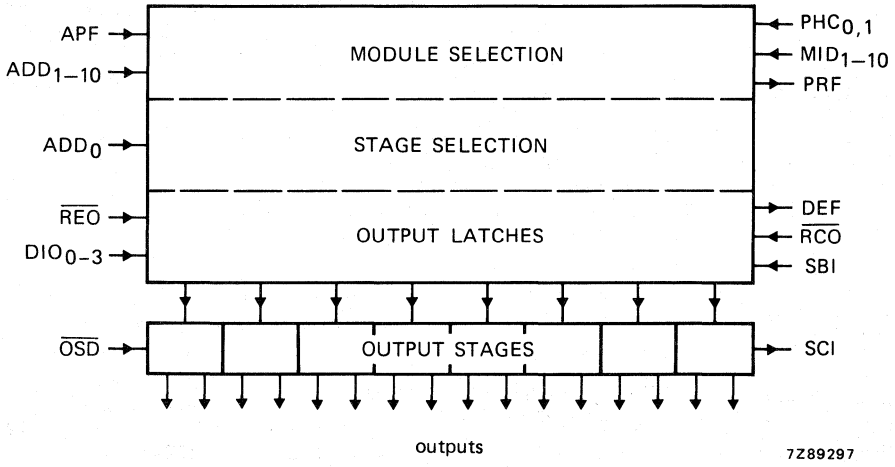


Fig. 2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard).

The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	logic	V_P	10 V ± 10%
Supply current	logic	I_P	typ. 65 mA (all stages ON)
			max. 75 mA (all stages ON)
			typ. 5 mA (all stages OFF)
Supply voltage (d.c.)	for output circuitry	V_S	24 ± 25%**
Supply current (excluding load current)	for output circuitry	I_S	typ. 115 mA (all stages ON)
			max. 160 mA (all stages ON)
			typ. 35 mA (all stages OFF)

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

** If V_S drops below 16 V, all output stages are forced into the non-conducting state for protection of the output circuitry.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 4)
ADD_0	Address bits from central processor; ADD_0 select a group of four output stages, $ADD_{1\text{-}10}$ select the output module.	c11
ADD_1		a11
ADD_2		c12
ADD_3		a12
ADD_4		c13
ADD_5		a13
ADD_6		c14
ADD_7		a14
ADD_8		c15
ADD_9		a15
ADD_{10}		c16
DIO_0	Data bits from central processor; data are stored in output stages by SBI.	c21
DIO_1		a21
DIO_2		c22
DIO_3		a22
$\overline{REO}$	Reset output module input; a low level on this input will reset all output latches and the short-circuit protection circuitry (output transistor non-conducting; input current LOW: 10 mA).	a27
$\overline{RCO}$	Reset from central processor (low level) during switch-on.	c27
MID_1	Module identification inputs; provide module with individual identity.	c1
MID_2		c2
MID_3		c3
MID_4		c4
MID_5		c5
MID_6		c6
MID_7		c7
MID_8		c8
MID_9		c9
MID_{10}		c10
SBI	Clock signal from central processor to output module, stores data on $DIO_{0\text{-}3}$ into output stages during input/output cycle.	c26
PHC_0	Phase control signals.	c23
PHC_1		a23
APF	Handshake signal; input/output address correct.	a26
$\overline{OSD}$	Output stage disable for all stages; input current LOW: 10 mA.	a28

Output data

The data outputs are $DO_{Y.0}$ to $DO_{Y.3}$ and $DO_{Z.0}$ to $DO_{Z.3}$.
They are accessible on connector 2, see "Terminal location".

Minimum load resistance $R_L = 12\ \Omega$.

Output transistor conducting: $R_L = 12\ \Omega$; $V_{a\text{-}c}$* = min. $V_S - 1{,}5$ V.
Output transistor non-conducting: I_o = max. 2 mA at $V_S = 30$ V.

For load inductance, see Fig. 3.

Output current (limited to 8 A per module)

for all stages	max. 1 A per stage
for maximum 4 stages	max. 2 A per stage

Output SCI is an open-collector output; drive capability max. 20 mA.
In case of a short circuit in one of the output stages, the output transistor is conducting: V_{SCI} = max. 0,5 V (with respect to 0 V - line);
transistor non-conducting: $V_{SCI} = 30$ V.

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 4)
PRF	Preparation of output module finished.	a24
DEF	Data exchange finished.	a25

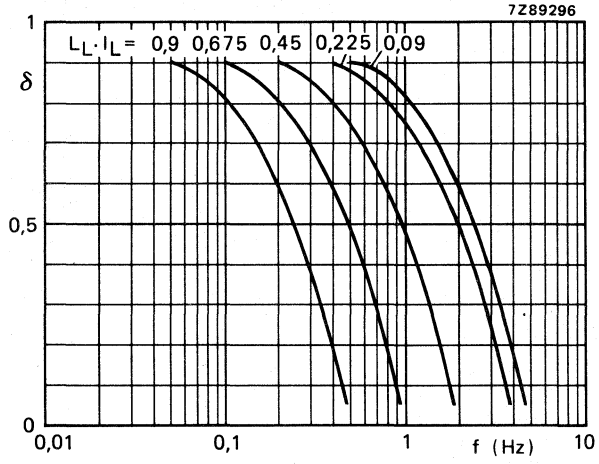


Fig. 3 Maximum duty factor (δ) as a function of switching frequency at different $L_L I_L$ - products (L_L = load inductance; I_L = load current).

* Voltage between terminal of row a and terminal of row c of connector 2.

MECHANICAL DATA

Dimensions in mm

Outlines

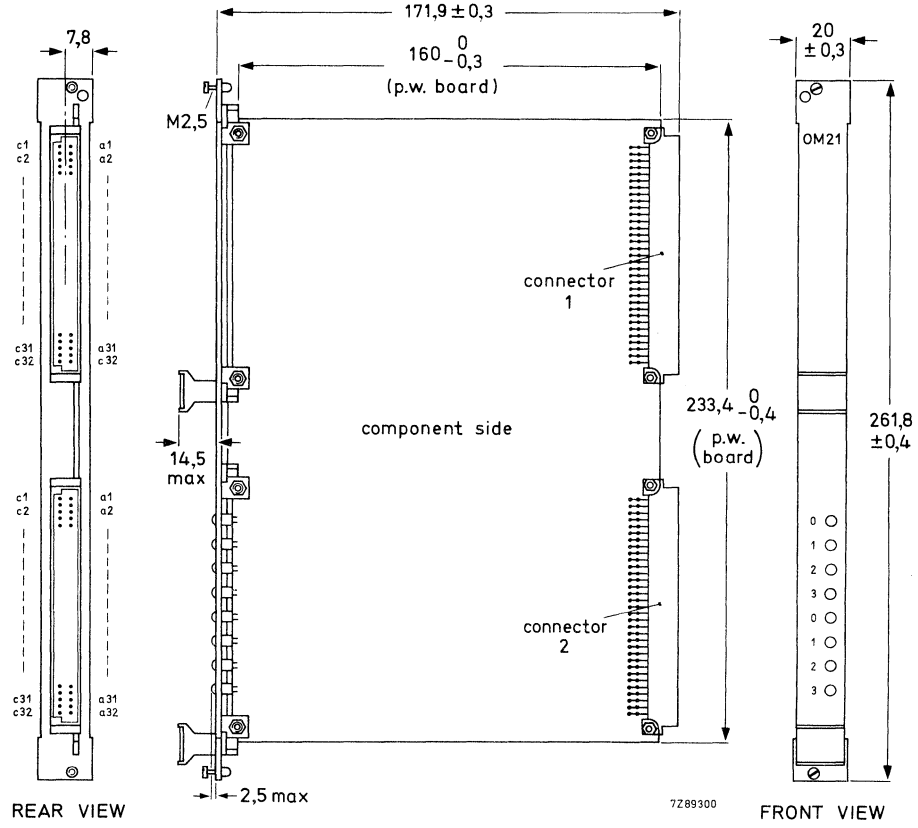


Fig. 4.

Mass 230 g

Terminal location

connector 1				connector 2		
row c		row a		row c		row a
MID_1	1	HIGH level	**	0 V	1	V_S
MID_2	2	HIGH level		0 V	2	SCI
MID_3	3	HIGH level		0 V	3	V_S
MID_4	4	HIGH level		$DO_{Y.0}$	4	$DO_{Y.0}$
MID_5	5	HIGH level		0 V	5	V_S
MID_6	6	HIGH level		$DO_{Y.1}$	6	$DO_{Y.1}$
MID_7	7	HIGH level		0 V	7	V_S
MID_8	8	HIGH level		$DO_{Y.1}$	8	$DO_{Y.1}$
MID_9	9	HIGH level		0 V	9	V_S
MID_{10}	10	HIGH level		$DO_{Y.2}$	10	$DO_{Y.2}$
ADD_0	11	ADD_1		0 V	11	V_S
ADD_2	12	ADD_3		$DO_{Y.2}$	12	$DO_{Y.2}$
ADD_4	13	ADD_5		0 V	13	V_S
ADD_6	14	ADD_7		$DO_{Y.3}$	14	$DO_{Y.3}$
ADD_8	15	ADD_9		0 V	15	V_S
ADD_{10}	16	n.c.		$DO_{Y.3}$	16	$DO_{Y.3}$
n.c.	17	n.c.		0 V	17	V_S
n.c.	18	n.c.		$DO_{Z.0}$	18	$DO_{Z.0}$
n.c.	19	n.c.		0 V	19	V_S
n.c.	20	n.c.		$DO_{Z.0}$	20	$DO_{Z.0}$
DIO_0	21	DIO_1		0 V	21	V_S
DIO_2	22	DIO_3		$DO_{Z.1}$	22	$DO_{Z.1}$
PHC_0	23	PHC_1		0 V	23	V_S
n.c.	24	PRF		$DO_{Z.1}$	24	$DO_{Z.1}$
0 V *	25	DEF		0 V	25	V_S
SBI	26	APF		$DO_{Z.2}$	26	$DO_{Z.2}$
$\overline{RCO}$	27	$\overline{REO}$		0 V	27	V_S
n.c.	28	OSD		$DO_{Z.2}$	28	$DO_{Z.2}$
n.c.	29	n.c.		0 V	29	V_S
n.c.	30	n.c.		$DO_{Z.3}$	30	$DO_{Z.3}$
V_P	31	V_P		0 V	31	V_S
0 V	32	0 V		$DO_{Z.3}$	32	$DO_{Z.3}$

n.c. = not connected.

Note
Supply-voltage lines (V_S) have to be connected to each output.

* No supply line; is used as return line for control signals.
** For coding MID lines.

OUTPUT MODULE

DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.

The output module contains 32 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs are floating with respect to each other. Each output stage has a suppressor diode, to allow it to switch inductive loads.

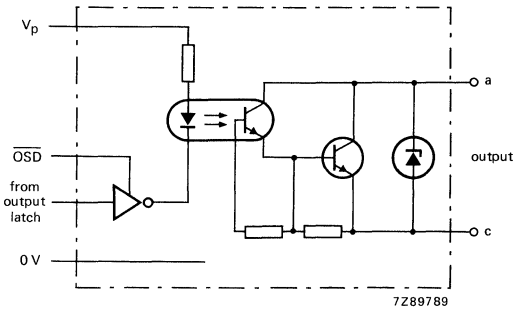


Fig. 1 Circuit diagram of an output stage.

To obtain a pull-down facility for the first 16 output stages, e.g. to drive TTL circuitry, the module has two 16-pin sockets (S_3 and S_4, Fig. 5), to provide insertion of adapter headers to which pull-down resistors are soldered. (See also Output Data.)

The output module has 11 address inputs (ADD_{0-10}) and 8 module identification inputs (MID_{3-10}), which are accessible on the connectors at the rear (Fig. 2).

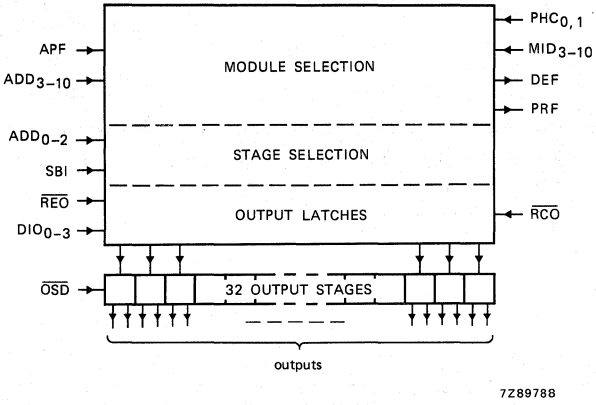


Fig. 2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard).

The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	logic	V_P	10 V ± 10%
Supply current	logic	I_P	typ. 340 mA (all stages ON)
			max. 400 mA (all stages ON)
			typ. 1 mA (all stages OFF)

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 5)
ADD_0	Address bits from central processor; ADD_{0-2} select a group of four output stages, ADD_{3-10} select the output module.	c11
ADD_1		a11
ADD_2		c12
ADD_3		a12
ADD_4		c13
ADD_5		a13
ADD_6		c14
ADD_7		a14
ADD_8		c15
ADD_9		a15
ADD_{10}		c16
APF	Handshake signal; input/output address correct.	a26
DIO_0	Data bits from central processor; data are stored in output stages by SBI.	c21
DIO_1		a21
DIO_2		c22
DIO_3		a22
MID_3	Module identification inputs; provide module with individual identity.	c3
MID_4		c4
MID_5		c5
MID_6		c6
MID_7		c7
MID_8		c8
MID_9		c9
MID_{10}		c10
$\overline{OSD}$	Output stage disable for all stages; input current LOW: 10 mA.	a28
PHC_0	Phase control signals.	c23
PHC_1		a23
$\overline{RCO}$	Reset from central processor (low level) during switch-on.	c27
$\overline{REO}$	Reset output module input; a low level on this input will reset all outputs latches (output transistor non-conducting); input current LOW: 10 mA.	a27
SBI	Clock signal from central processor to output module, stores data in DIO_{0-3} into output stages during input/output cycle.	c26

Output data

The data outputs are $DO_{S.0}$ to $DO_{S.3}$, $DO_{T.0}$ to $DO_{T.3}$, $DO_{U.0}$ to $DO_{U.3}$, $DO_{V.0}$ to $DO_{V.3}$, $DO_{W.0}$ to $DO_{W.3}$, $DO_{X.0}$ to $DO_{X.3}$, $DO_{Y.0}$ to $DO_{Y.3}$ and $DO_{Z.0}$ to $DO_{Z.3}$. They are accessible on connector 2, see Terminal location.

Output transistor conducting: output current = max. 100 mA at $V_{a\text{-}c}$* = max. 1,5 V.
Output transistor non-conducting: output current = max. 10 μA at $V_{a\text{-}c}$* = max. 30 V.

Each output has a suppressor diode, which allows the switching of loads with an inductance of max. 10 H.

Note: If a supply voltage of 5 V is required, e.g. to drive TTL circuitry, pull-down resistors (R, Figs 3 and 4) must be used. These resistors can be soldered to adapter headers, which have to be inserted into sockets S_3 and S_4 (Figs 3 and 5). The emitter-output on terminal c31 of connector 2 must be connected to the 0 V-line of the external supply voltage V_S (Fig. 4); this output can then only be used in common emitter configuration.

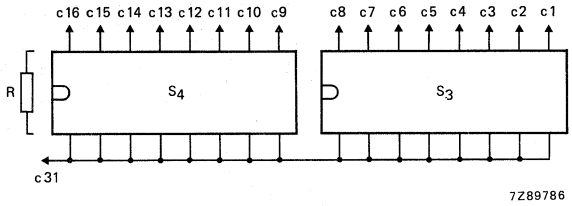


Fig. 3.

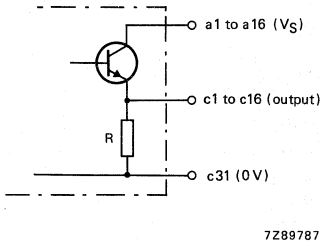


Fig. 4.

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 5)
DEF	Data exchange finished.	a25
PRF	Preparation of output module finished.	a24

MECHANICAL DATA

Dimensions in mm

Outlines

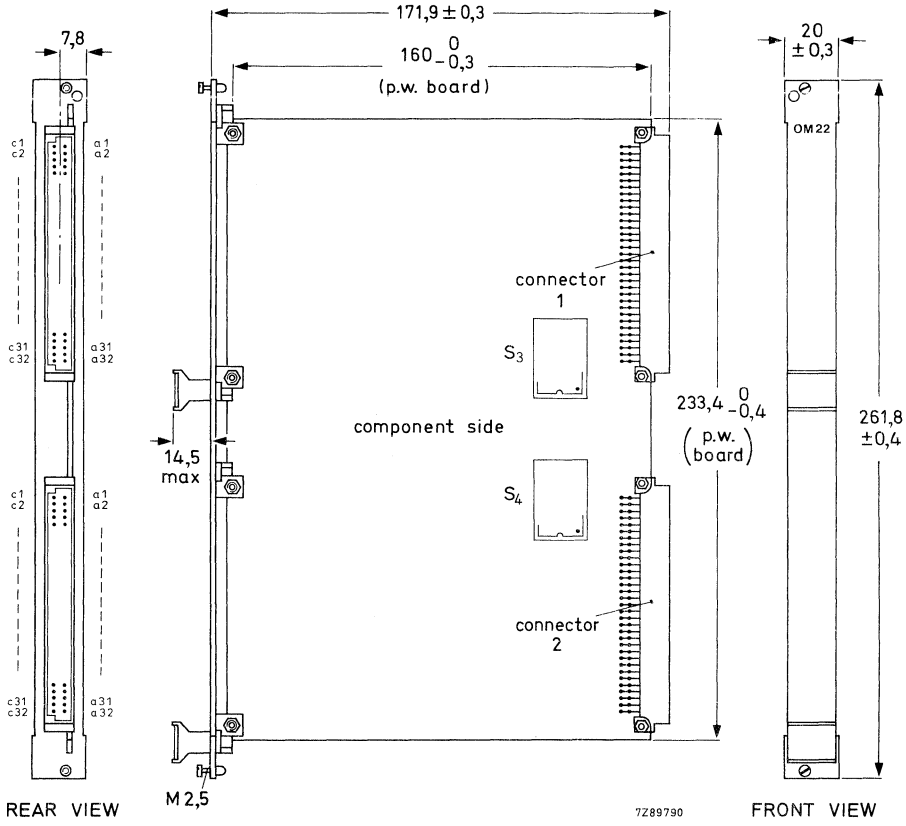


Fig. 5.

Mass approx. 230 g

Terminal location

connector 1				connector 2		
row c		row a		row c		row a
n.c.	1	HIGH level		$DO_{S.0}$	1	$DO_{S.0}$
n.c.	2	HIGH level		$DO_{S.1}$	2	$DO_{S.1}$
MID_3	3	HIGH level		$DO_{S.2}$	3	$DO_{S.2}$
MID_4	4	HIGH level		$DO_{S.3}$	4	$DO_{S.3}$
MID_5	5	HIGH level	**	$DO_{T.0}$	5	$DO_{T.0}$
MID_6	6	HIGH level		$DO_{T.1}$	6	$DO_{T.1}$
MID_7	7	HIGH level		$DO_{T.2}$	7	$DO_{T.2}$
MID_8	8	HIGH level		$DO_{T.3}$	8	$DO_{T.3}$
MID_9	9	HIGH level		$DO_{U.0}$	9	$DO_{U.0}$
MID_{10}	10	HIGH level		$DO_{U.1}$	10	$DO_{U.1}$
ADD_0	11	ADD_1		$DO_{U.2}$	11	$DO_{U.2}$
ADD_2	12	ADD_3		$DO_{U.3}$	12	$DO_{U.3}$
ADD_4	13	ADD_5		$DO_{V.0}$	13	$DO_{V.0}$
ADD_6	14	ADD_7		$DO_{V.1}$	14	$DO_{V.1}$
ADD_8	15	ADD_9		$DO_{V.2}$	15	$DO_{V.2}$
ADD_{10}	16	n.c.		$DO_{V.3}$	16	$DO_{V.3}$
n.c.	17	n.c.		$DO_{W.0}$	17	$DO_{W.0}$
n.c.	18	n.c.		$DO_{W.1}$	18	$DO_{W.1}$
n.c.	19	n.c.		$DO_{W.2}$	19	$DO_{W.2}$
n.c.	20	n.c.		$DO_{W.3}$	20	$DO_{W.3}$
DIO_0	21	DIO_1		$DO_{X.0}$	21	$DO_{X.0}$
DIO_2	22	DIO_3		$DO_{X.1}$	22	$DO_{X.1}$
PHC_0	23	PHC_1		$DO_{X.2}$	23	$DO_{X.2}$
n.c.	24	PRF		$DO_{X.3}$	24	$DO_{X.3}$
0 V*	25	DEF		$DO_{Y.0}$	25	$DO_{Y.0}$
$\overline{SBI}$	26	$\overline{APF}$		$DO_{Y.1}$	26	$DO_{Y.1}$
$\overline{RCO}$	27	$\overline{REO}$		$DO_{Y.2}$	27	$DO_{Y.2}$
n.c.	28	$\overline{OSD}$		$DO_{Y.3}$	28	$DO_{Y.3}$
n.c.	29	n.c.		$DO_{Z.0}$	29	$DO_{Z.0}$
n.c.	30	n.c.		$DO_{Z.1}$	30	$DO_{Z.1}$
V_P	31	V_P		$DO_{Z.2}$ (0 V)▲	31	$DO_{Z.2}$
0 V	32	0 V		$DO_{Z.3}$	32	$DO_{Z.3}$

n.c. = not connected.

* No supply line; is used as return line for control signals.
** For coding MID lines.
▲ 0-line of V_S when pull-down resistors are used.

BIDIRECTIONAL PARALLEL INTERFACE

DESCRIPTION

The RP20 is intended for use as an interface between a PC20-system and data input and output devices, e.g. thumbwheel switches, seven-segment displays, etc.

The module has 16 enable outputs, each of which can select an eight-bit input or output device, so it has a capacity of 16 x 8 bits and therefore it occupies 32 four-bit places in the input/output field. When an enable output selects an input device, this device will put 8 bits of information on the data lines. This data information is stored in the buffer memory of the RP20. When an output device is selected, data is transferred from the buffer memory to this device. The lower enable lines always select outputs; inputs are selected by the remaining lines. Separation between these two groups is done by means of the SCIO inputs, which determine the number of outputs that are scanned.

Enabling always starts at EN_0 and finishes at EN_{15}. The scanning rate can be chosen by means of switches on the module.

After having activated successively all enable outputs the RP20 stops scanning, activates its $\overline{\text{READY}}$ output and enables the central processor to get access to the buffer memory. Data exchange between central processor and RP20 takes place during the I/O-phase in which the RP20 is scanned. As soon as the central processor finishes this I/O-phase, the RP20 disables the central processor access to its memory and starts scanning the inputs and outputs, provided the START input is at the high level. If the START input is at the low level, scanning is postponed until this level is high again. During scanning the RP20 ignores the addressing of the central processor; this does not influence the cycle time of the PC20-system.

The start procedure is initiated by a low level on the RCO input. First all buffer memory locations of the RP20 are set to 0, then there will be a data exchange between the scratchpad memory of the central processor and the buffer memory of the RP20. At the moment central processor finishes the I/O-phase, the RP20 starts scanning the input and output devices.

Data lines, enable lines, $\overline{\text{READY}}$ output and START input are electrically isolated from the PC20 circuitry by means of photocouplers.

Although the system is designed for use in combination with input and output devices requiring 24 V supply, the RP20 can be adapted for use with devices for 5 V supply by means of a jumper on the printed-wiring board.

The RP20 is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 7) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)		V_P	10 V ± 10%
Supply current		I_P	max. 150 mA (V_P = 10 V, all outputs used, all data 0)
Supply voltage (d.c.)	for output circuitry	V_S*	24 V ± 25%
Supply current	for output circuitry	I_S	max. 250 mA (all data lines at low level) min. 20 mA (all data lines at high level)
Supply voltage (d.c.)	for output circuitry	V_S*	5 V ± 5%**
Supply current	for output circuitry	I_S	max. 250 mA (all data lines and inverting inputs at low level, 4 enable lines inverted) min. 20 mA (all data lines at high level)

* The value of V_S depends on the supply voltage and signal levels required for the input and output devices.

** To be adjusted by means of a jumper; see 'ADJUSTMENTS'.

Input and output data

The inputs at connector 1 meet the standard LOCMOS specifications; the inputs and outputs at connector 2 are electrically isolated from the logic part by means of photocouplers.

	function	terminations (Fig. 7)	
		connector 1	connector 2
INPUTS			
ADD_0 ADD_1 ADD_2 ADD_3 ADD_4 ADD_5 ADD_6 ADD_7 ADD_8 ADD_9 ADD_{10}	Address bits from central processor; ADD_{0-4} select the memory position on the module, ADD_{5-10} select the module.	c11 a11 c12 a12 c13 a13 c14 a14 c15 a15 c16	
APF	Handshake signal, indicates that addresses are correct.	a26	
INVI	Input that inverts input information; input current LOW: 10 mA.		a24
$\overline{INVO}$	Input that inverts output information; input current LOW: 10 mA.		c24
MID_5 MID_6 MID_7 MID_8 MID_9 MID_{10}	Module identification inputs; provide module with individual identity.	c5 c6 c7 c8 c9 c10	
PHC_0 PHC_1	Phase control signals from central processor.	c23 a23	
RCO	Reset from central processor.	c27	
$SCIO_0$ $SCIO_1$ $SCIO_2$ $SCIO_3$	Input/output separation code inputs, control the R/$\overline{W}$ line to central processor, and determine whether data is received or sent on DB_{0-7}.	c17 c18 c19 c20	
START	A high level (24 V) starts a scanning cycle of the RP20; if this input is kept HIGH permanently, scanning starts immediately after the I/O cycle during which data was exchanged; input current high: 10 mA. For 5 V-level operation, see 'ADJUSTMENTS'.		c20

	function	terminations (Fig. 7) connector 1	connector 2
BI-DIRECTIONAL BUSES			
DIO_0 DIO_1 DIO_2 DIO_3	Data bits to and from central processor.	c21 a21 c22 a22	
DB_0 DB_1 DB_2 DB_3 DB_4 DB_5 DB_6 DB_7	These external data bus terminals form outputs when the enable outputs of the first group are activated, and inputs during activation of the second group. A "1" in the scratchpad memory of the central processor will be represented as a high level at these outputs, provided $\overline{INVO}$ input is at high level (or floating). If $\overline{INVO}$ input is at low level a "1" will be represented as a low level. A high level at these inputs will be represented in the scratchpad memory as a "0" when the INVI input is at the high level (or floating). A low level of the INVI input causes a high level to become a "1". DB_{0-7} occupy two four-bit places in the scratchpad memory; DB_{0-3} occupy the lower place, DB_{4-7} occupy the higher place. Input current low (I_{il}): 10 mA; output current low (I_{ol}): max. 15 mA; see Fig. 1.		a26 c26 a28 c28 a30 c30 a32 c32
OUTPUTS			
$\overline{EN}_0$ $\overline{EN}_1$ $\overline{EN}_2$ $\overline{EN}_3$ $\overline{EN}_4$ $\overline{EN}_5$ $\overline{EN}_6$ $\overline{EN}_7$ $\overline{EN}_8$ $\overline{EN}_9$ $\overline{EN}_{10}$ $\overline{EN}_{11}$ $\overline{EN}_{12}$ $\overline{EN}_{13}$ $\overline{EN}_{14}$ $\overline{EN}_{15}$	Enable outputs (open collector); select an input or output device. During the scanning period of the RP20, these outputs go successively to the low level, enabling an input device to put its information on DB_{0-7}, or an output device to store the information from this bus. For devices requiring a high level for enabling, see 'ADJUSTMENTS'. Each enable output corresponds with two four-bit places; the lower enable lines refer to the lower scratchpad places. Output current: max. 80 mA at 0,5 V.		a2 c2 a4 c4 a6 c6 a8 c8 a10 c10 a12 c12 a14 c14 a16 c16

	function	terminations (Fig. 7)	
		connector 1	connector 2
DEF	Data exchange finished (open collector output)	a25	
PRF	Preparation of RP20 finished (open collector output)	a24	
$\overline{\text{READY}}$	A low level indicates that RP20 finished I/O scanning (open collector output); output current low: max. 20 mA at 0,5 V.		a20
R/$\overline{\text{W}}$	A low level indicates that the central processor has to receive data (open collector output).	c24	

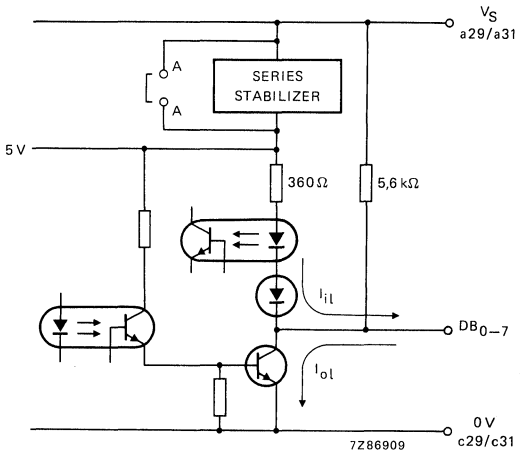


Fig. 1 External data bus circuit. Points A to be bridged for 5 V supply, see "ADJUSTMENTS".

Time data (see also Figs 2 and 3)

Scanning time for one input or output	t_o
Time that scanning pulse is active	$t_{sc} = 0{,}8\ t_o$
Time that input information must become stable	$t_v = \text{max. } 0{,}7\ t_o - 50\ \mu s$
Time between two scanning pulses	$t_1 = 0{,}2\ t_o$
Time between enable output active and output data valid	$t_2 = \text{max. } 40\ \mu s$
Time that output data remains valid	$t_3 = 0{,}1\ t_o$
Total scanning time	$t_s = 16\ t_o$

To be adjusted with switches on the module, see 'ADJUSTMENTS'.

t_s ms	t_o μs
5,12	320
10,24	640
20,48	1280
40,96	2560

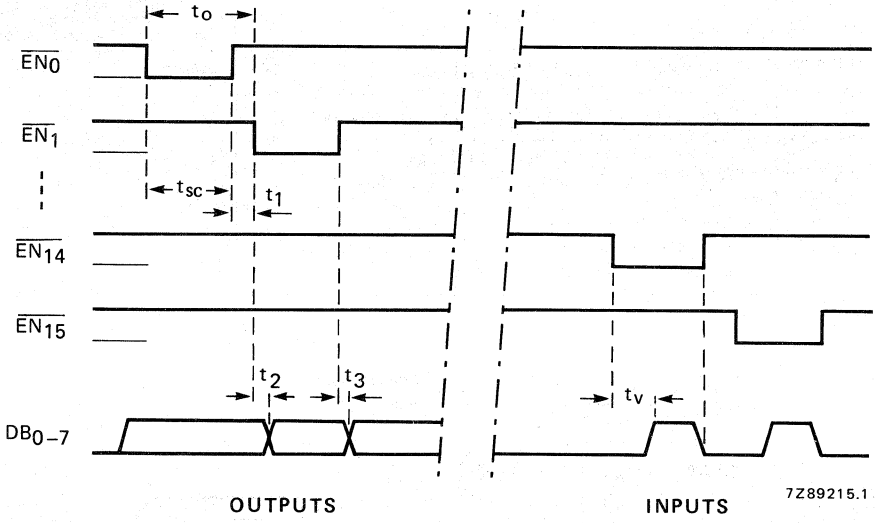

t_o
$\overline{EN_0}$
$\overline{EN_1}$
t_{sc}
t_1
$\overline{EN_{14}}$
$\overline{EN_{15}}$
t_2
t_3
t_v
DB_{0-7}
OUTPUTS
INPUTS
7Z89215.1

Fig. 2.

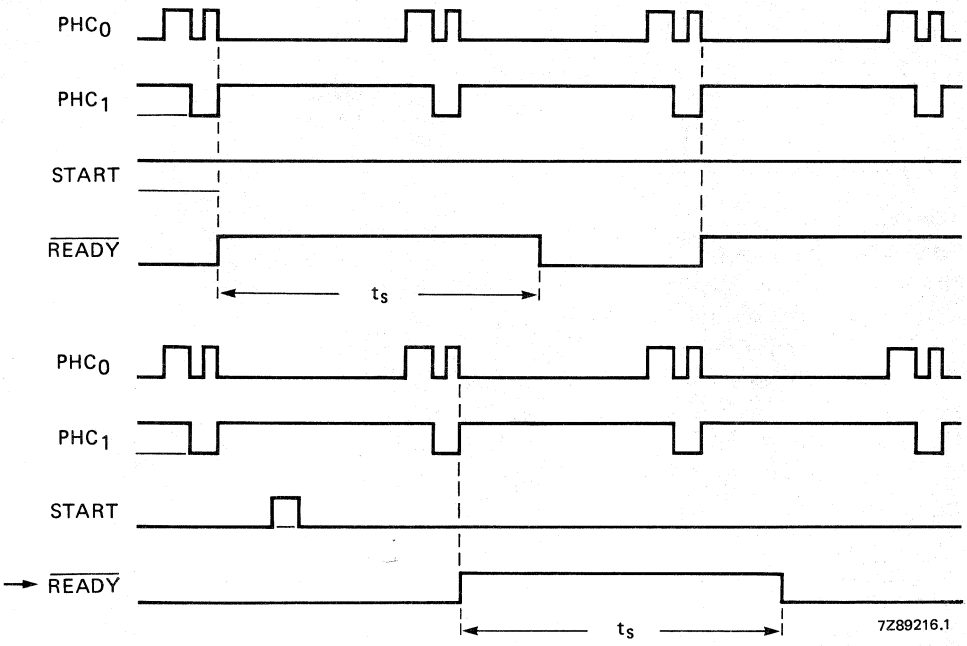

PHC_0
PHC_1
START
$\overline{READY}$
t_s
PHC_0
PHC_1
START
$\overline{READY}$
t_s
7Z89216.1

Fig. 3.

ADJUSTMENTS

Adjustment for use with devices requiring 5 V supply

If the input and output devices require 5 V levels, the supply voltage (V_S) should be 5 V. By bridging the points A (Figs 1 and 5) with a jumper, the module is adapted for 5 V supply.

Adjustment for 5 V level operation on START input

For 5 V level operation on the START input, a resistor of 360 Ω should be connected between the points B (Figs. 4 and 5).

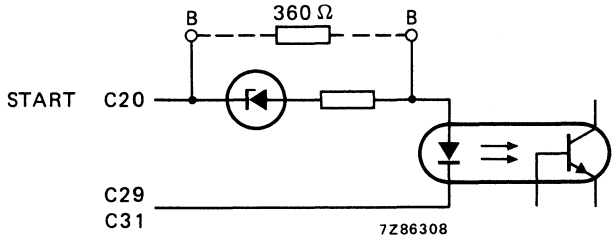


Fig. 4.

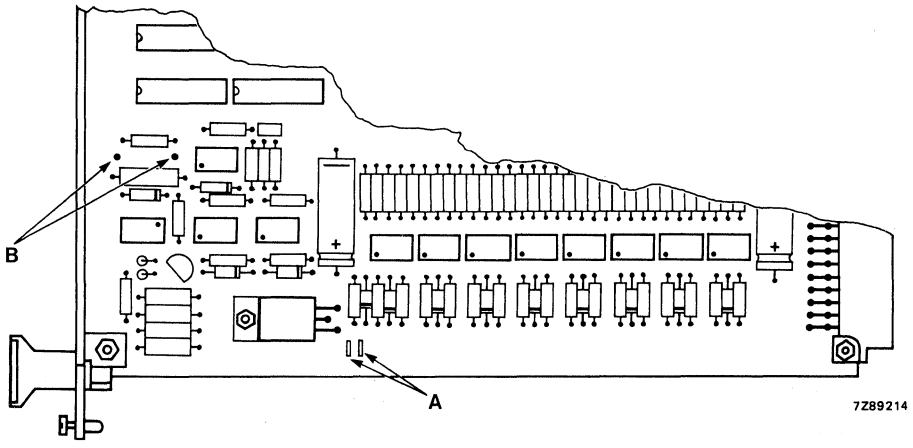


Fig. 5.

Adjustment for use with devices requiring a high level for enabling

For devices which require a high level for enabling, it is necessary to invert the outputs $\overline{EN}_0$, $\overline{EN}_1$, $\overline{EN}_{14}$ and $\overline{EN}_{15}$ by means of switches on the printed-wiring board (Fig. 6). The following points have to be connected:
point 1 to point 16: EN_{14} is inverted;
point 2 to point 15: EN_1 is inverted;
point 3 to point 14: EN_{15} is inverted;
point 4 to point 13: EN_0 is inverted.
Proper functioning is only possible if the 5 V-jumper is used (Fig. 5).

For inverting purposes a transistor BC337 with common emitter and a resistor of 4700 Ω between base and emitter have been added; the collector has been connected to output CT (termination c18, connector 2), the base to input BT (termination a18, connector 2).

Adjustment of scanning time

The total scanning time (t_s, Fig. 3) can be adjusted with switches on the printed-wiring board (Fig. 6). A choice can be made of the following connections:
point 5 to point 12: t_s = 40,96 ms;
point 6 to point 11: t_s = 10,24 ms;
point 7 to point 10: t_s = 20,48 ms;
point 8 to point 9: t_s = 5,12 ms.

Note: Only one connection should be made.

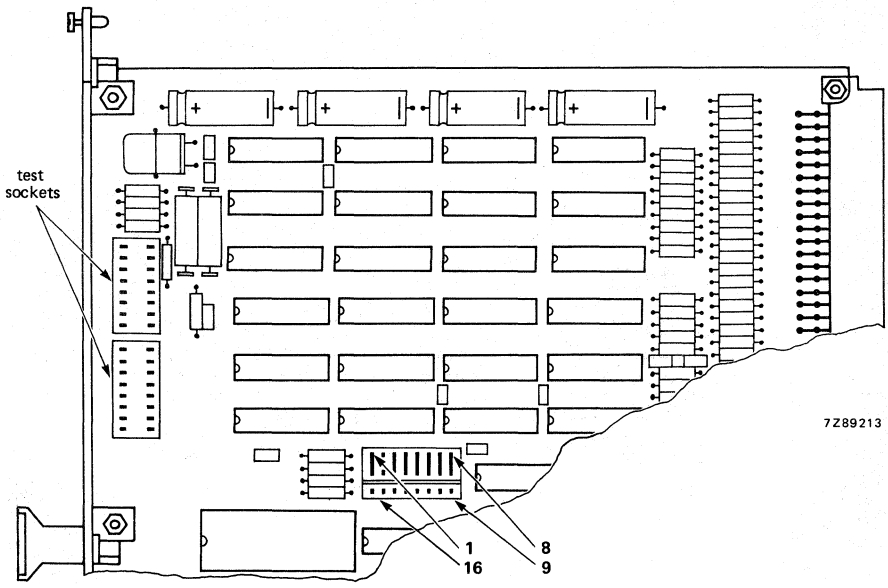


Fig. 6.

MECHANICAL DATA

Dimensions in mm

Outlines

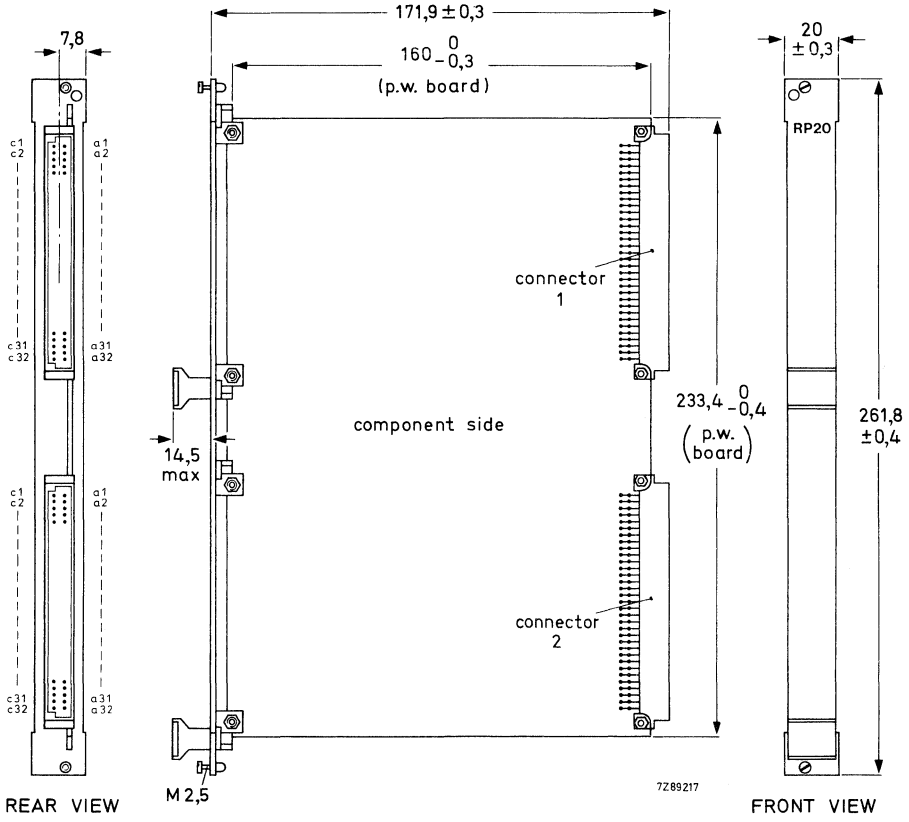


Fig. 7.

Mass approx. 270 g

Terminal location

connector 1		
row c		row a
n.c.	1	n.c.
n.c.	2	n.c.
n.c.	3	n.c.
n.c.	4	n.c.
MID_5	5	HIGH level
MID_6	6	HIGH level
MID_7	7	HIGH level
MID_8	8	HIGH level
MID_9	9	HIGH level
MID_{10}	10	HIGH level
ADD_0	11	ADD_1
ADD_2	12	ADD_3
ADD_4	13	ADD_5
ADD_6	14	ADD_7
ADD_8	15	ADD_9
ADD_{10}	16	n.c.
$SCIO_0$	17	HIGH level
$SCIO_1$	18	HIGH level
$SCIO_2$	19	HIGH level
$SCIO_3$	20	HIGH level
DIO_0	21	DIO_1
DIO_2	22	DIO_3
PHC_0	23	PHC_1
$R/\overline{W}$	24	PRF
0 V	25	DEF
SBI	26	APF
RCO	27	n.c.
n.c.	28	n.c.
n.c.	29	n.c.
n.c.	30	n.c.
V_P	31	V_P
0 V	32	0 V

connector 2		
row c		row a
n.c.	1	n.c.
$\overline{EN}_1$	2	$\overline{EN}_0$
n.c.	3	n.c.
$\overline{EN}_3$	4	$\overline{EN}_2$
n.c.	5	n.c.
$\overline{EN}_5$	6	$\overline{EN}_4$
n.c.	7	n.c.
$\overline{EN}_7$	8	$\overline{EN}_6$
n.c.	9	n.c.
$\overline{EN}_9$	10	$\overline{EN}_8$
n.c.	11	n.c.
$\overline{EN}_{11}$	12	$\overline{EN}_{10}$
n.c.	13	n.c.
$\overline{EN}_{13}$	14	$\overline{EN}_{12}$
n.c.	15	n.c.
$\overline{EN}_{15}$	16	$\overline{EN}_{14}$
n.c.	17	n.c.
CT	18	BT
n.c.	19	n.c.
START	20	$\overline{READY}$
n.c.	21	n.c.
n.c.	22	n.c.
n.c.	23	n.c.
$\overline{INVO}$	24	INVI
n.c.	25	n.c.
DB_1	26	DB_0
n.c.	27	n.c.
DB_3	28	DB_2
0V	29	V_S*
DB_5	30	DB_4
0V	31	V_S*
DB_7	32	DB_6

* V_S = 24 V: points A (Fig. 5) **not** bridged;
V_S = 5 V: points A to be bridged with a jumper.

BIDIRECTIONAL SERIAL INTERFACE

The RS20 is for remote control of input and output modules of a PC20-system (passive slave). Furthermore it allows two PC20-systems to be connected to each other in a master/slave configuration, for data exchange between the systems (active slave); see Fig. 1.

Both master and slave station must have an RS20 module and they must be connected to each other via a coaxial cable or a shielded twisted pair of wires.

The RS20 performs three modes of operation, which are selected by the levels on inputs BMS and CMS, as shown in Table INPUTS, paragraph ELECTRICAL DATA.

Mode A (master mode): when used in the master PC20-system for communication with one slave station.

Mode B (active slave mode): when used in the slave PC20-system with a central processor.

Mode C (passive slave mode): when used in the slave PC20-system, which includes only input and output modules, to transfer data without further processing.

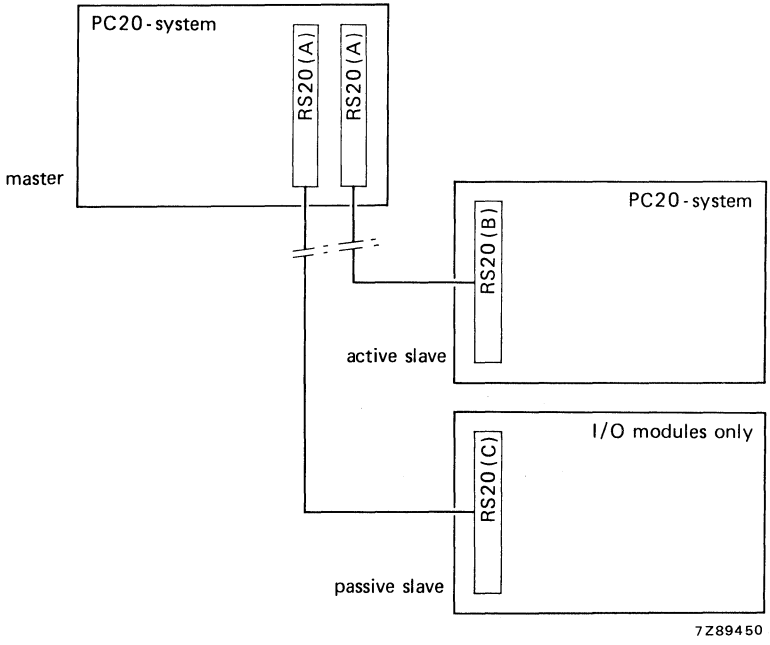


Fig. 1.

Master/slave communication takes place via the 256-bit RAM buffer memories of the RS20 modules. The data transfer rate is 256 bits in 0,75 ms. Within this time all control and data is transferred and checked.

Whether data are handled as inputs or outputs is established by the setting of the SCIO coding inputs.

Error detection is accomplished by Cyclic Redundancy Checking. The $\overline{\text{ERROR}}$ output is set to 0 if an error has been detected on received data at either or both ends of the external data line. This output is also set to 0 during the first 120 ms after switching on the supply voltage, and after 60 ms if no communication has taken place. During this period continuous testing takes place to restore communication. If the $\overline{\text{ERROR}}$ output is set to 0, the LED at the front of the module is lit.

After data exchange between the PC20-systems, the $\overline{\text{READY}}$ output is set to 0, and the RS20 is ready for internal data exchange between its buffer memory and the scratchpad memory of the PC20-system of which it forms part, or the connected input and output modules. This internal data exchange takes place during the I/O phase in which the RS20 is scanned. The sequence of the various data flows is shown in Fig. 2.

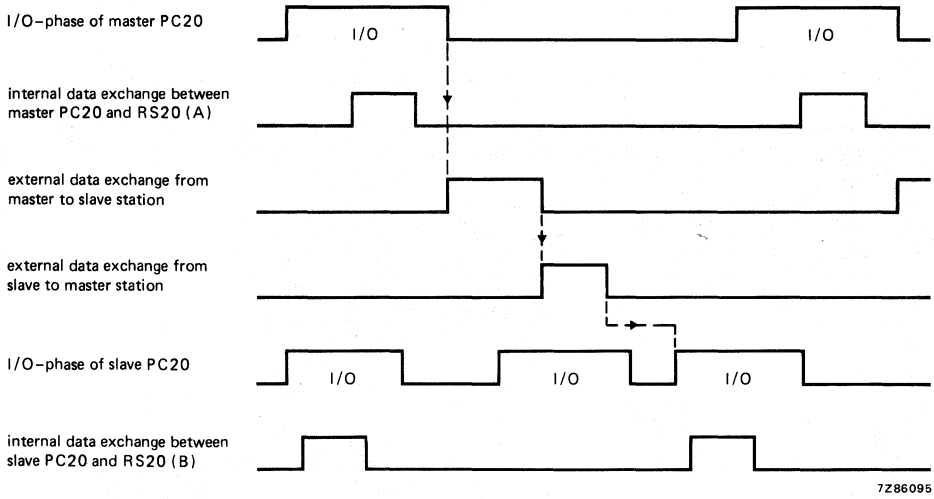


Fig. 2.

The RS20 is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 7) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19 in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply voltage (d.c.)	logic	V_P	10 V ± 10%	
Supply current	logic	I_P	typ. 160	mA
Supply voltage (d.c.)	for input/output circuitry	V_S	24 V ± 25%	
Supply current	for input/output circuitry	I_S	typ. 5	mA
Output voltage between TR_1 and TR_3*		$V_{o(p-p)}$	min. 5,66	V
Input voltage between TR_1 and TR_3*		$V_{i(p-p)}$	min. 4,24	V
Input impedance between TR_1 and TR_3*		Z_i	approx. 75	Ω
Data transfer rate			400	kbaud

Connection between master and slave station

For distances up to 250 m a shielded twisted pair of wires, max. loop resistance 50 Ω, with polythene insulation can be used (Fig. 4). For larger distances a coaxial cable has to be used (Fig. 3), e.g. COAX-12** for max. 750 m, or BAMB00-SIX** for max. 2000 m.

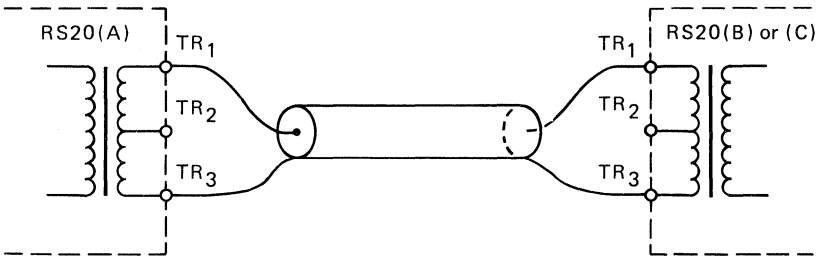


Fig. 3 Connection of bidirectional busses via a coaxial cable.

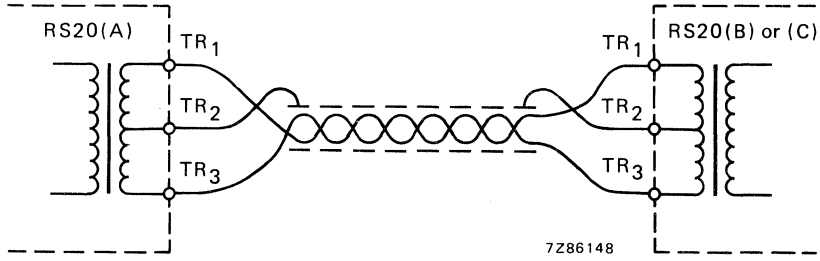


Fig. 4 Connection of bidirectional busses, via a shielded twisted pair of wires.

* Bidirectional busses for the external data line.
** Trade name of NKF (Nederlandse Kabel Fabrieken).

Input and output data

All inputs and outputs meet the standard LOCMOS specifications, unless otherwise specified.

	function	terminations (Fig. 7)	
		connector 1	connector 2
BI-DIRECTIONAL DATA BUSSES			
ADD_0	Address bits. Inputs in A and B modes, outputs in C mode.	c11	
ADD_1		a11	
ADD_2		c12	
ADD_3		a12	
ADD_4		c13	
ADD_5		a13	
ADD_6		c14	
ADD_7		a14	
ADD_8		c15	
ADD_9		a15	
ADD_{10}		c16	
APF	Handshake signal, indicates that addresses are correct. Input in A and B modes, output in C mode.	a26	
DIO_0	Data exchange between RS20 and PC20 system.	c21	
DIO_1		a21	
DIO_2		c22	
DIO_3		a22	
PHC_0	Phase control. Inputs in A and B modes, outputs in C mode.	c23	
PHC_1		a23	
SBI	Store command; Stores data in buffer memory during I/O cycle. Input in A and B modes, output in C mode.	c26	
TR_1	Transmit/receive terminals for connection of external data line (TR_2 common); via transformer coupled to the inner circuitry of the RS20, (Figs 3 and 4).		c26
TR_2			c28
TR_3			c30

	function	terminations (Fig. 7)	
		connector 1	connector 2
INPUTS			
BMS CMS	Mode select inputs. Mode A: BMS and CMS are LOW. Mode B: BMS is HIGH, CMS is LOW. Mode C: BMS is HIGH or LOW, CMS is HIGH.	c1 c2	
MID_6 MID_7 MID_8 MID_9 MID_{10}	Module identification inputs; provide module with individual identity.	c6 c7 c8 c9 c10	
$SCIO_0$ $SCIO_1$ $SCIO_2$ $SCIO_3$	Input/output separation coding inputs. Numbers smaller than code are outputs (seen from PC20 master system); other numbers are inputs.	c17 c18 c19 c20	
START	Enables external data exchange. Input is isolated from the internal circuitry with photo-isolator (Fig. 5), to be connected to an OM20 output. LOW input level: 0 to 7 V; HIGH input level: 18 to 30 V.		c20

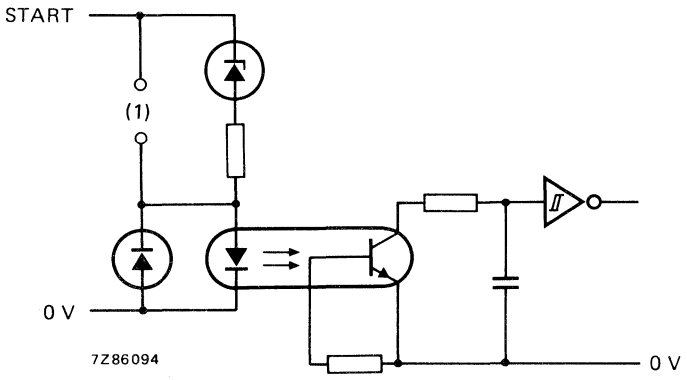


Fig. 5 Circuit diagram of START input.

(1) For 5 V-level operation a resistor of 360 Ω ± 5%, style CR25, has to be connected.

	function	terminations (Fig. 7)	
		connector 1	connector 2
OUTPUTS			
DEF	Signal to central processor, indicating that data from central processor has been stored.	a25	
$\overline{\text{DER}}$ *	Detected error output, indicating an error has been detected on data received from the other RS20 module.		c14
$\overline{\text{ERROR}}$ *	Error output, indicating data exchange along the external data line did not happen errorless or did not happen at all		c16
PRF	Preparation of RS20 finished (open collector output)	a24	
$\overline{\text{READY}}$ *	Output, indicating RS20 has finished external data exchange.		a20
R/$\overline{\text{W}}$	Read-write level PC20-system. Only active during I/O-phase.	c24	
$\overline{\text{TER}}$*	Transmitted error output, indicating the RS-20 at the other side of the external data line has detected an error on the received data.		c12

* Open-collector output; isolated from the internal circuitry with photo-isolator (Fig. 6). To be connected to IM20 inputs.
Maximum sink current: 25 mA; maximum collector voltage in off-position: 30 V.

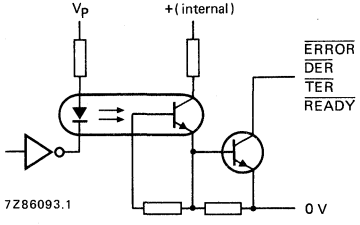


Fig. 6 Circuit diagram of $\overline{\text{ERROR}}$, $\overline{\text{DER}}$, $\overline{\text{TER}}$ and $\overline{\text{READY}}$ outputs.

MECHANICAL DATA

Dimensions in mm

Outlines

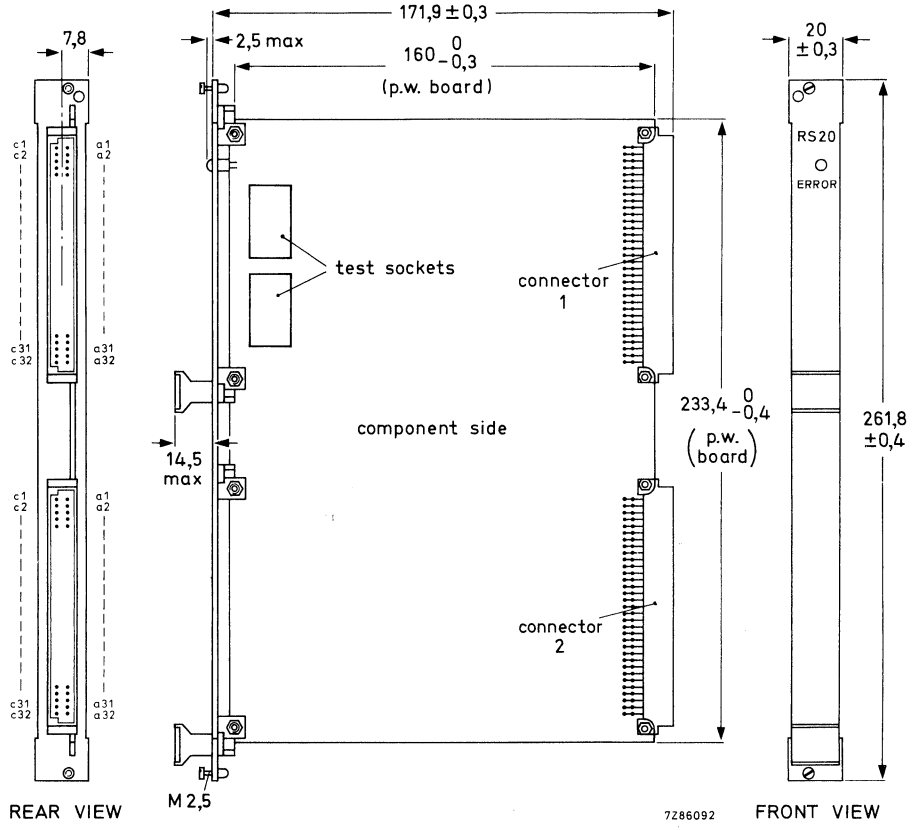


Fig. 7.

Mass approx. 270 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
BMS	1	HIGH level	n.c.	1	n.c.
CMS	2	HIGH level	n.c.	2	n.c.
n.c.	3	n.c.	n.c.	3	n.c.
n.c.	4	n.c.	n.c.	4	n.c.
n.c.	5	n.c.	n.c.	5	n.c.
MID_6	6	HIGH level	n.c.	6	n.c.
MID_7	7	HIGH level	n.c.	7	n.c.
MID_8	8	HIGH level	n.c.	8	n.c.
MID_9	9	HIGH level	n.c.	9	n.c.
MID_{10}	10	HIGH level	n.c.	10	n.c.
ADD_0	11	ADD_1	n.c.	11	n.c.
ADD_2	12	ADD_3	$\overline{TER}$	12	n.c.
ADD_4	13	ADD_5	n.c.	13	n.c.
ADD_6	14	ADD_7	$\overline{DER}$	14	n.c.
ADD_8	15	ADD_9	n.c.	15	n.c.
ADD_{10}	16	n.c.	$\overline{ERROR}$	16	n.c.
$SCIO_0$	17	HIGH level	n.c.	17	n.c.
$SCIO_1$	18	HIGH level	n.c.	18	n.c.
$SCIO_2$	19	HIGH level	n.c.	19	n.c.
$SCIO_3$	20	HIGH level	START	20	$\overline{READY}$
DIO_0	21	DIO_1	n.c.	21	n.c.
DIO_2	22	DIO_3	n.c.	22	n.c.
PHC_0	23	PHC_1	n.c.	23	n.c.
$R/\overline{W}$	24	PRF	0 V	24	n.c.
0 V*	25	DEF	n.c.	25	n.c.
SBI	26	APF	TR_1	26	n.c.
n.c.	27	n.c.	n.c.	27	n.c.
n.c.	28	n.c.	TR_2	28	n.c.
n.c.	29	n.c.	0 V	29	Vs
n.c.	30	n.c.	TR_3	30	n.c.
V_p	31	V_p	0 V	31	Vs
0 V	32	0 V	0 V	32	n.c.

n.c. = not connected

* No supply line; is used as return line for control signals.

SUPPLY AND OUTPUT MODULE

DESCRIPTION

This supply and output module is used with the other PC20 modules to assemble a programmable controller.

The module contains 8 addressable output stages, a 24 V/10 V d.c.-d.c. converter and an alarm circuit for the 24 V supply. The output stages have photo-isolators between external and internal circuitry (Fig. 1). All outputs have a grounded load. Each output stage has a flywheel diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages have electronic short-circuit protection with automatic reset.

The 24 V/10 V d.c.-d.c. converter provides the logic supply voltage for a small controller system with galvanic isolation from the external 24 V supply. Furthermore, it is short-circuit protected and two or more of these modules may be connected in parallel for higher current demands in larger systems.

The alarm circuit monitors the 24 V supply (V_{ic}), providing two alarm outputs. One of these is accessible for external use (hardware); the other can be used internally for processing (software). Furthermore, a LED on the front panel indicates that V_{ic} is above its minimum specified level.

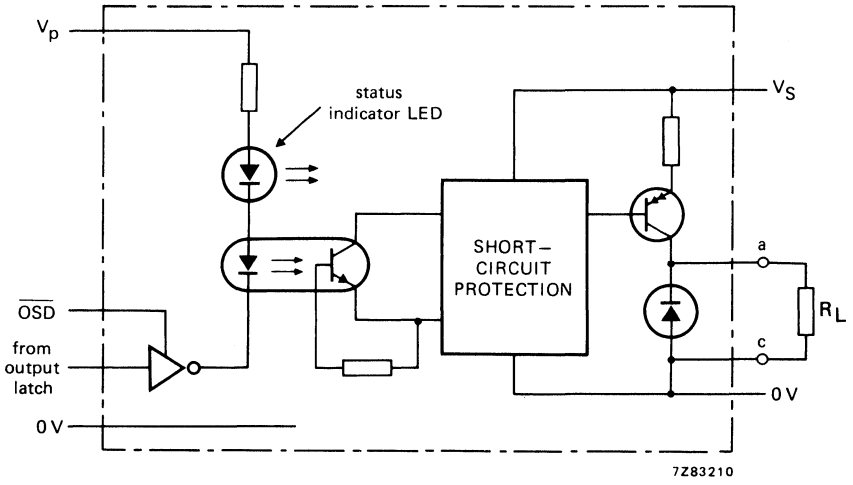


Fig. 1 Circuit diagram of an output stage.

→ The output part has 11 address inputs (ADD_{0-10}) and 10 module identification inputs (MID_{1-10}), which are accessible on the connectors at the rear (Fig. 2).

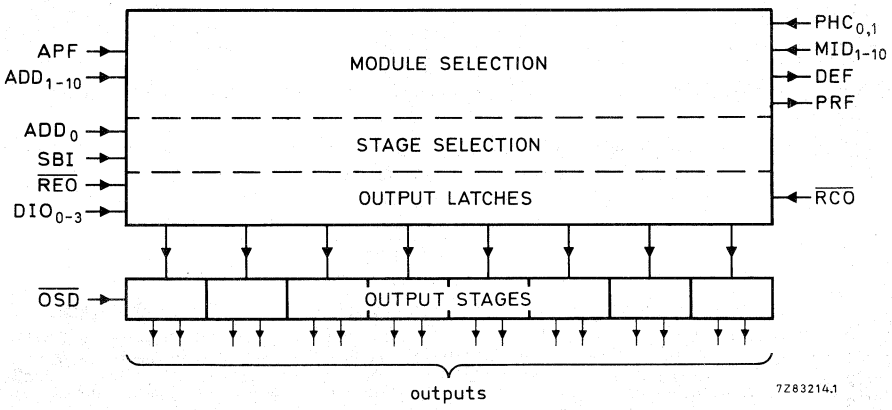


Fig. 2 Block diagram of the output part.

The circuits are built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard).

The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	for output circuitry	V_S	24 V ± 25%**
Supply current (excluding load current)		I_S	typ. 50 mA (all stages (ON) max. 60 mA (all stages ON) typ. 30 mA (all stages OFF)
Supply voltage (d.c.)	for 24 V/10 V d.c.-d.c. converter	V_{ic}	24 V ± 25%
Supply current, at V_{ic} = 24 V and output current I_p = 1,7 A		I_{ic}	typ. 1,1 A

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

** If V_S drops below 16 V, all output stages are forced into the non-conducting state for protection of the output circuitry.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 3)
ADD_0	Address bits from central processor; ADD_0 selects a group of four output stages, $ADD_{1\text{-}10}$ select the (output) module.	c11
ADD_1		a11
ADD_2		c12
ADD_3		a12
ADD_4		c13
ADD_5		a13
ADD_6		c14
ADD_7		a14
ADD_8		c15
ADD_9		a15
ADD_{10}		c16
DIO_0	Data bits from central processor; data are stored in output stages by SBI.	c21
DIO_1		a21
DIO_2		c22
DIO_3		a22
$\overline{REO}$	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current LOW: 0,1 mA.	a27
$\overline{RCO}$	Reset from central processor (low level) during switch-on.	c27
MID_1	Module identification inputs; provide module with individual identity.	c1
MID_2		c2
MID_3		c3
MID_4		c4
MID_5		c5
MID_6		c6
MID_7		c7
MID_8		c8
MID_9		c9
MID_{10}		c10
SBI	Clock signal from central processor to output module, stores data on $DIO_{0\text{-}3}$ into output stages during input/output cycle.	c26
PHC_0	Phase control signals.	c23
PHC_1		a23
APF	Handshake signal; input/output address correct.	a26
$\overline{OSD}$	Output stage disable for all stages; input current LOW: 0,1 mA.	a28

Output data

The data outputs are $DO_{Y.0}$ to $DO_{Y.3}$ and $DO_{Z.0}$ to $DO_{Z.3}$. They are accessible on connector 2, see "Terminal location".

Minimum load resistance $R_L = 48\ \Omega$.

Output transistor conducting: $R_L = 48\ \Omega$; $V_{a\text{-}c}$* = min. $V_S - 1{,}5$ V.
Output transistor non-conducting: I_o = max. 2 mA at $V_S = 30$ V.

The outputs are continuously tested for short-circuiting. As soon as the short-circuiting is removed, the output stage is automatically reset to normal operation.

Output current (limited to 3 A per module)
for all stages — max. 0,375 A per stage
for maximum 6 stages — max. 0,5 A per stage

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 3)
PRF	Preparation of output module finished.	a24
DEF	Data exchange finished.	a25
ALI	Alarm internal; active LOW as long as V_{ic} is above 17,5 V; with opto-coupler isolation between internal and external supply.	a29 c29

The external alarm output ALE (connector 2, a2) has a similar function as ALI. It is an open collector output and can sink a current of 10 mA ($V_{ALE\ LOW} = 1{,}3$ V).

Converter output

Output voltage	V_P	10 V ± 10%
Output current	I_P	max. 1,7 A; short-circuit proof **

V_P: on terminals a31, c31 of connector 1

0 V: on terminals a32, c32 of connector 1

* Voltage between terminal of row a and terminal of row c of connector 2.
** If two or more modules are connected in parallel the output current per module is max. 1,5 A.

MECHANICAL DATA

Dimensions in mm

Outlines

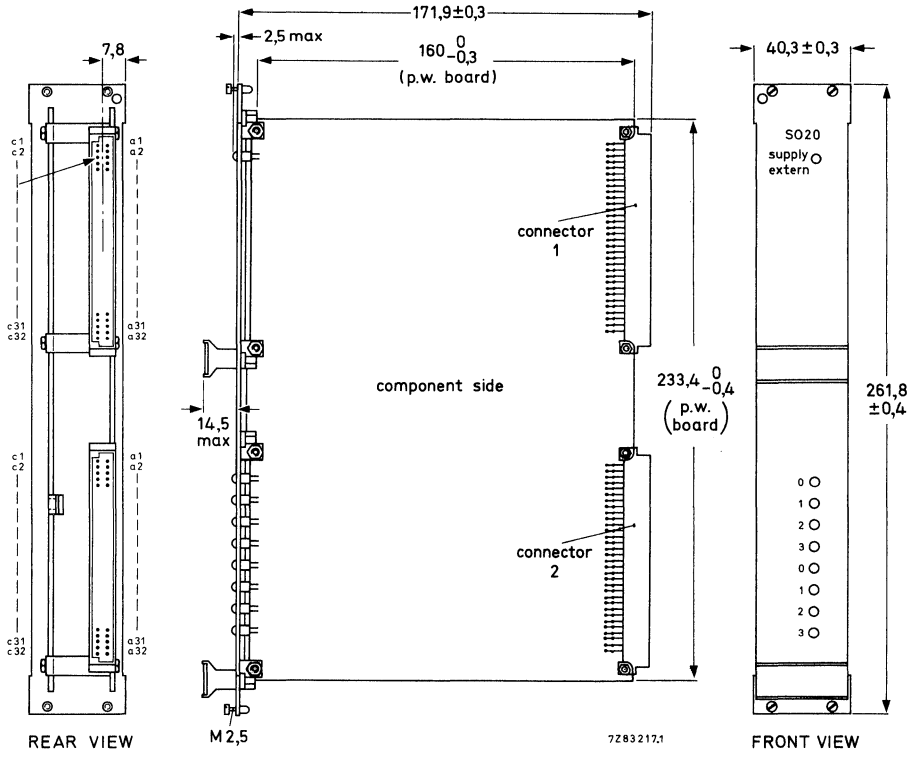


Fig. 3.

Mass 400 g

Terminal location

connector 1				connector 2		
row c		row a		row c		row a
MID_1	1	HIGH level		n.c.	1	n.c.
MID_2	2	HIGH level		0 V **	2	ALE
MID_3	3	HIGH level		n.c.	3	n.c.
MID_4	4	HIGH level		0 V **	4	V_{ic}
MID_5	5	HIGH level	***	n.c.	5	n.c.
MID_6	6	HIGH level		0 V **	6	V_{ic}
MID_7	7	HIGH level		n.c.	7	n.c.
MID_8	8	HIGH level		0 V **	8	V_{ic}
MID_9	9	HIGH level		0 V*	9	V_S
MID_{10}	10	HIGH level		0 V*	10	n.c.
ADD_0	11	ADD_1		0 V*	11	V_S
ADD_2	12	ADD_3		0 V*	12	n.c.
ADD_4	13	ADD_5		0 V*	13	V_S
ADD_6	14	ADD_7		0 V*	14	n.c.
ADD_8	15	ADD_9		0 V*	15	V_S
ADD_{10}	16	n.c.		0 V*	16	n.c.
n.c.	17	n.c.		0 V *	17	V_S
n.c.	18	n.c.		$DO_{Y.0}$	18	$DO_{Y.0}$
n.c.	19	n.c.		0 V *	19	V_S
n.c.	20	n.c.		$DO_{Y.1}$	20	$DO_{Y.1}$
DIO_0	21	DIO_1		0 V *	21	V_S
DIO_2	22	DIO_3		$DO_{Y.2}$	22	$DO_{Y.2}$
PHC_0	23	PHC_1		0 V *	23	V_S
n.c.	24	PRF		$DO_{Y.3}$	24	$DO_{Y.3}$
0 V ****	25	DEF		0 V *	25	V_S
$\overline{SBI}$	26	$\overline{APF}$		$DO_{Z.0}$	26	$DO_{Z.0}$
$\overline{RCO}$	27	$\overline{REO}$		0 V *	27	V_S
n.c.	28	$\overline{OSD}$		$DO_{Z.1}$	28	$DO_{Z.1}$
ALI	29	ALI		0 V *	29	V_S
n.c.	30	n.c.		$DO_{Z.2}$	30	$DO_{Z.2}$
V_P	31	V_P		0 V *	31	V_S
0 V	32	0 V		$DO_{Z.3}$	32	$DO_{Z.3}$

n.c. = not connected.

Note
Supply-voltage lines (V_S) have to be connected to each group of 4 outputs.

* 0 V for V_S.
** 0 V for V_{ic}.
*** For coding MID-lines.
**** No supply line; is used as return line for control signals.

BIDIRECTIONAL SERIAL INTERFACE

The VI20 bidirectional serial interface is used in PC20 systems to communicate with TTYs, VDUs, minicomputers and other equipment handling serial data. It has V24/RS232C/RS423 and current-loop inputs and outputs for this purpose. Furthermore, the VI20 can be used to advantage as a satellite processor for handling complex and time-consuming operations thus maintaining rapidity of system response. Its address and data processors are identical to those used in the PC20 central processor modules. Having a 2k16 EPROM *program memory* and a ¼k4 *data memory* it resembles most the CP20 central processor; see Fig. 1. Figure 8 shows the location of the two type 2716 EPROMs (sockets A and B). As with all other I/O modules the VI20 uses photo-isolators between its logic circuitry and the outside world.

For communication with the PC20, the VI20 has a 16-bit (4 x 4 bits) *control register* to exchange control data, and a 128-bit (32 x 4 bits) *buffer register* (part of data memory) to transfer process data. The control register is identified in the PC20 scratchpad memory using the MID_{2-9} code on the back panel: *hardware addressing*. The buffer register is identified by six bits, A_{5-10}, generated in the PC20 program and accumulated in the control register: *software addressing*. Utmost flexibility is achieved through free selection of the software addressing code allowing the entire area of a 2k4 scratchpad memory to be covered for storing and retrieving the process data.

In contrast to the PC20 system, the VI20 is intermittent in operation. When started by the PC20 it completes one data processing phase (active state) then stops and waits until the next start signal (idle state). During the processing phase the VI20 inputs and outputs are directly accessible.

Basically, there are three PC20 I/O operations (Fig. 2):
- for communication between the PC20 and its process (marked '1' in Fig. 2);
- for communication between the PC20 and the VI20 via the control register (marked '2');
- for transfer of process data between PC20 scratchpad memory and buffer register (hatched).

Transfer of process data occurs upon request; the VI20 must be in the idle state to allow this.

The VI20 instruction set is identical to that of the PC20 system. Intermittent operation of the VI20 is clear from the flow chart, Fig. 3. Upon switch-on or reset the CONDITION is set to '1' level. Also, in the first cycle after switch-on or reset, all 4-bit data memory locations are set to 1001.

The VI20 has been built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts). The corresponding rack part of connector 1 (Fig. 8) is available on the back panel. That of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-inch racks and IEC 130-14 or DIN 41612 for connectors.

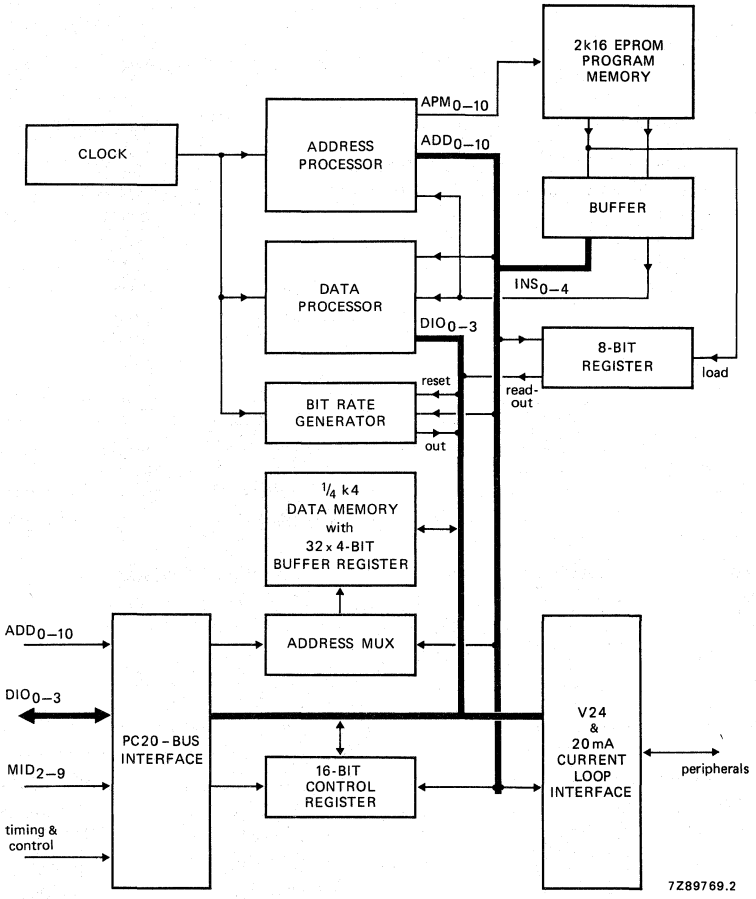


Fig. 1 Block diagram.

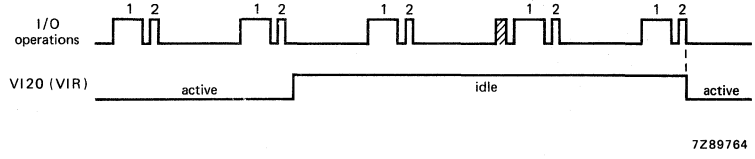


Fig. 2 Basic PC20 I/O operations and VI20 states.

The 4 x 4-bit *control register*, Fig. 4, contains four outputs (one-bit places) to and ten inputs (one-bit places) from the PC20 scratchpad memory. Addressing of the control register can only occur on pages 0 and 1 of the CP22 scratchpad (MID_{10} internally connected to 0 V).

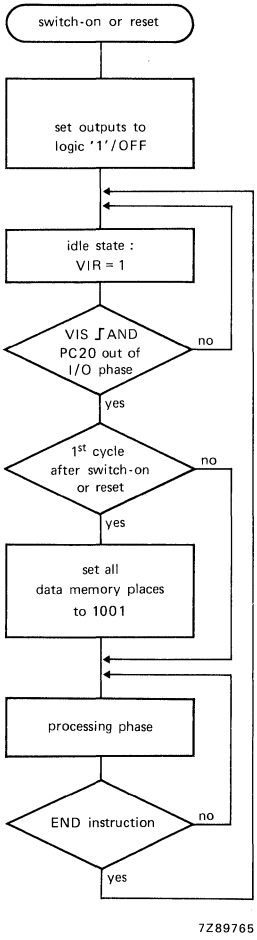


Fig. 3 Flow chart.

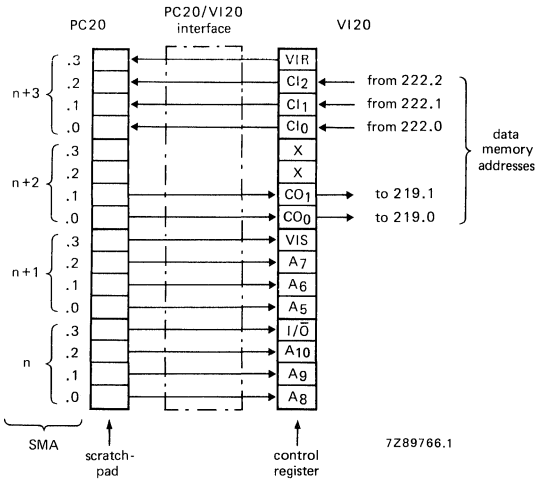


Fig. 4 Control Register.

The control register bit functions are:

VIR — VIR = 1: VI20 in idle state;
VIR = 0: VI20 in active state.

$CI_{0, 1, 2}$ — General-purpose control bits originating in VI20 program.

XX — No assignment.

$CO_{0, 1}$ — General-purpose control bits originating in PC20 program.

VIS — Provided VIR = 1 (VI20 idle) a positive change of this bit will cause the VI20 to become active and start with line 0000 of its program; VI20 will not become active before the end of the PC20 I/O phase in which the positive transition of VIS has been detected.

$I/\overline{O}$ — $I/\overline{O}$ = 0: data transfer from scratchpad memory to buffer register;
$I/\overline{O}$ = 1: data transfer from buffer register to scratchpad memory.

$A_{5\text{-}10}$ — Software addressing bits originating in the PC20 program (A_5 = least significant bit; A_{10} = most significant bit).

In the table below the occupation of the *data memory* is specified. Locations 0 to 215 are free for storing data generated in the VI20 program. Locations 216 and 217 form the eight-bit register that can be loaded by the LSTI0 instruction only. The highest locations, 224 to 255, form the *buffer register*.

The bit-rate generator is used in asynchronous data transmission. It can be adjusted to a variety of bit rates by means of jumpers (S, Fig. 5) on the printed-wiring board; see table below.

Mark/space ratio is 1 : 1 (50% duty factor). Reset to start of LOW phase is done using the 'STRD 221' execute instruction.

Bit-rate selection. Upper jumper position = 1, lower jumper position = 0. Jumper positioning shown in Fig. 5 for 300 bits/s.

Assignment of data memory addresses.

address	function
0 to 215	no assignment
216, 217	read-only eight-bit register
218 . 0/ . 1/ . 2/ . 3	V24 inputs
219 . 0/ . 1	$CO_{0,1}$ control bits
219 . 2	arithmetic overflow
219 . 3	bit-rate generator output
220 . 0/ . 1/ . 2/ . 3	V24 outputs
221	reset bit-rate generator
222 . 0/ . 1/ . 2	$CI_{0,1,2}$ control bits
223	no assignment
224 to 255	buffer register

bits/s	jumper positions S_3 S_2 S_1 S_0
50	□□□□
75	□□□□
110	□□□□
150	□□□□
300	□□□□
600	□□□□
1200	□□□□
2400	□□□□
4800	□□□□
9600	□□□□

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	logic	V_P	10 V ± 10%
Supply current	logic	I_P	typ. 160 mA max. 170 mA
Supply voltage (d.c.)	d.c.-d.c. converter*	V_S	24 V ± 25%
Supply current	d.c.-d.c. converter*	I_S	max. 110 mA

Inputs

Data inputs. The data inputs I_0 (218.0), I_1 (218.1), I_2 (218.2) and I_3 (218.3) are zener-diode protected and meet V24 standards. The bit level is '1' when input voltage $V_i \leqslant -1$ V and '0' when $V_i \geqslant +1$ V. They are accessible via connector 2; see 'Terminal location'. The inputs are commoned through V_C.

Input resistance	R_i	see Fig. 6
Max. permissible input voltage (positive or negative)	$V_{i\,max}$	30 V

The first input (corresponding to address 218.0) can be made to act as a 20 mA current loop by changing the position of two jumpers (A, Fig. 5) on the printed-wiring board. Current flow is from CLI_0 to CLI_1, see Fig. 6. The bit level is '1' when input current $I_i \leqslant 0{,}1$ mA and '0' when $I_i \geqslant 10$ mA.

Max. permissible input current	$I_{i\,max}$	20 mA

* Used to supply V24 interface circuitry.

Individual reset. The VI20 can either be reset via $\overline{RCO}$ together with the PC20 system using the $\overline{RCP}$ input to the central processor or it can be individually reset using input $\overline{RVI}$ (table below).

Individual reset.

$\overline{RVI}$	voltage	typ current
active	0 V to + 1 V	0,5 mA
not active	+ 10 V or floating	–

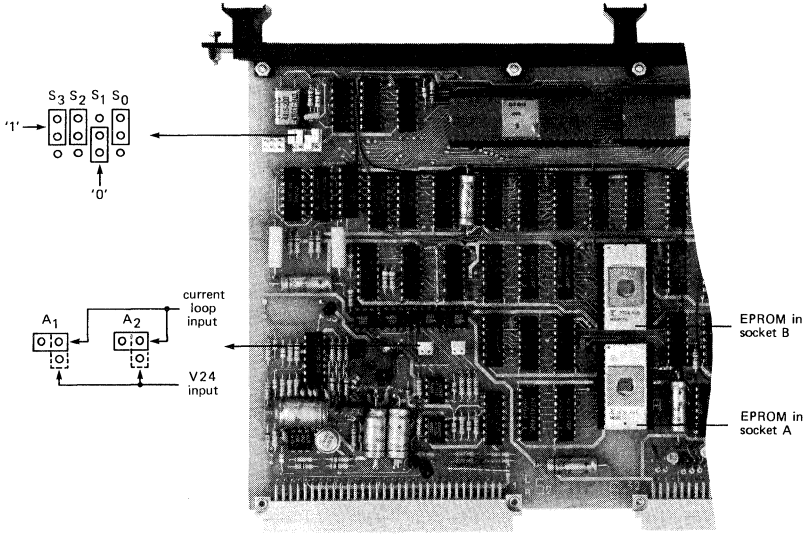


Fig. 5 VI20 adjustments.

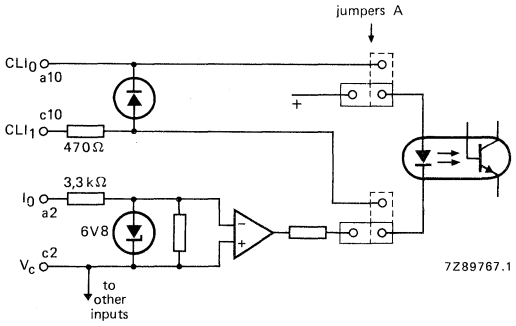


Fig. 6 Circuit diagram for input 218.0; for jumpers A see Fig. 5.

input	function	termination of connector 1 (Fig. 8)
ADD_0	Address bits from central processor. *Control register* ADD_{0-1} select a group of four bits in the control register. ADD_{2-9} select the control register. *Buffer register* ADD_{0-4} address both the buffer register and its address field in the scratchpad memory. ADD_{5-10} select the buffer register.	c11
ADD_1		a11
ADD_2		c12
ADD_3		a12
ADD_4		c13
ADD_5		a13
ADD_6		c14
ADD_7		a14
ADD_8		c15
ADD_9		a15
ADD_{10}		c16
APF	Handshake signal indicating that address for VI20 is stable.	a26
DIO_0*	Data bits from and to central processor.	c21
DIO_1*		a21
DIO_2*		c22
DIO_3*		a22
MID_2	Control register identification inputs; provide control register with individual identity.	c2
MID_3		c3
MID_4		c4
MID_5		c5
MID_6		c6
MID_7		c7
MID_8		c8
MID_9		c9
PHC_0	Phase control signals from central processor.	c23
PHC_1		a23
$\overline{RCO}$	Reset from central processor during switch-on (active LOW)	c27
$\overline{RVI}$	Individual VI20 reset (active LOW)	a27
SBI	Store command to store data from central processor in control register or buffer register.	c26

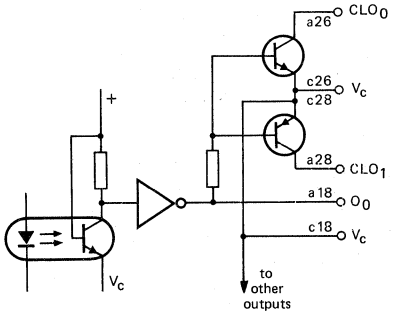


Fig. 7 Circuit diagram for output 220.0.

* Either input or output.

Outputs

Data outputs. The data outputs O_0 (220.0), O_1 (220.1), O_2 (220.2) and O_3 (220.3) conform to V24 standards. The bit level is '1' when output voltage V_o is −4 to −6 V and '0' when V_o is + 4 to + 6 V. Access is via connector 2; see 'Terminal location'. All outputs are commoned through V_c.

Min. permissible load resistance	R_{Lmin}	450 Ω

Output O_0 (address 220.0) drives 20 mA current-loop outputs CLO_0 and CLO_1 for two-line and four-line transmission (open collector outputs): see Fig. 7. Current flow is from CLO_0 to V_c (NPN transistor) and from V_c to CLO_1 (PNP transistor) respectively.

Specifications of current-loop outputs CLO_0 and CLO_1.

bit level in data memory address 220.0	NPN transistor between CLO_0 and V_c	PNP transistor between V_c and CLO_1
'1'	not conducting	conducting
'0'	conducting	not conducting

Max. permissible collector current	I_{Cmax}	30 mA
Collector-emitter voltage	V_{CE}	$\leqslant$ 0,5 V at I_{Cmax}
Max. permissible collector-emitter voltage	V_{CEmax}	30 V
Collector-emitter leakage current	I_{CEO}	$\leqslant$ 100 μA at V_{CEmax}

Reference outputs. Reference outputs V_+ and V_- are available (+ 12 V and −12 V) to bias any one of the inputs. These outputs are commoned via V_c.

Minimum permissible load resistance is 1 kΩ for each output.

output	function	termination of connector 1 (Fig. 8)
DEF	Data exchange — scratchpad memory to buffer register — finished (open collector output).	a25
PRF	Preparation of VI20-addressing finished (open collector output).	a24
R/$\overline{W}$	Signal to central processor (active LOW); prepares central processor for data on DIO_{0-3} to be written in scratchpad memory (open collector output).	c24

Note: All V24 inputs and outputs as well as V_+ and V_- are commoned to V_c and floating with respect to V_P and V_S.

MECHANICAL DATA

Outlines

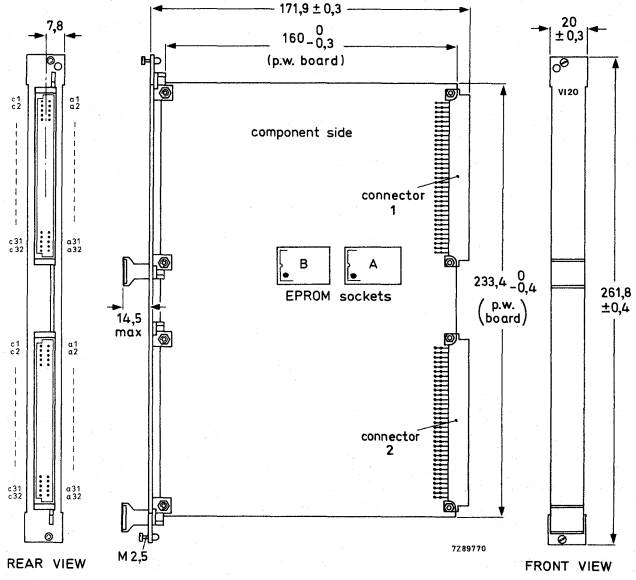


Fig. 8.

Mass approx. 300 g

Terminal location

connector 1				connector 2		
row c		row a		row c		row a
n.c.	1	n.c.		n.c.	1	n.c.
MID_2	2	HIGH level	*	V_c	2	I_0
MID_3	3	HIGH level		n.c.	3	n.c.
MID_4	4	HIGH level		V_c	4	I_1
MID_5	5	HIGH level		n.c.	5	n.c.
MID_6	6	HIGH level		V_c	6	I_2
MID_7	7	HIGH level		n.c.	7	n.c.
MID_8	8	HIGH level		V_c	8	I_3
MID_9	9	HIGH level		n.c.	9	n.c.
n.c.	10	n.c.		CLI_1	10	CLI_0
ADD_0	11	ADD_1		n.c.	11	n.c.
ADD_2	12	ADD_3		n.c.	12	n.c.
ADD_4	13	ADD_5		n.c.	13	n.c.
ADD_6	14	ADD_7		V_+	14	n.c.
ADD_8	15	ADD_9		n.c.	15	n.c.
ADD_{10}	16	n.c.		V_-	16	n.c.
n.c.	17	n.c.		n.c.	17	n.c.
n.c.	18	n.c.		V_c	18	O_0
n.c.	19	n.c.		n.c.	19	n.c.
n.c.	20	n.c.		V_c	20	O_1
DIO_0	21	DIO_1		n.c.	21	n.c.
DIO_2	22	DIO_3		V_c	22	O_2
PHC_0	23	PHC_1		n.c.	23	n.c.
$R/\overline{W}$	24	PRF		V_c	24	O_3
0 V**	25	DEF		0 V	25	V_S
$\underline{SBI}$	26	$\underline{APF}$		V_c	26	CLO_0
$\overline{RCO}$	27	$\overline{RVI}$		0 V	27	V_S
n.c.	28	n.c.		V_c	28	CLO_1
n.c.	29	n.c.		0 V	29	V_S
n.c.	30	n.c.		n.c.	30	n.c.
V_P	31	V_P		0 V	31	V_S
0 V	32	0 V		n.c.	32	n.c.

n.c. = not connected.

* For coding MID lines only.
** No supply line; is used as return line for control signals.

MICROCONTROLLER

The MC20 is a programmable controller for small systems. It uses the same address and data processors as the PC20 system.
The controller is on one printed-wiring board, and contains the following functions:

- 32 inputs;
- 20 outputs;
- 2k16 EPROM program memory;
- ½k4 scratchpad memory;
- 8 adjustments for software timers/counters;
- 5 internal clock references;
- 24 V/5 V d.c.-d.c. converter;
- automatic reset when power switched-on.

The microcontroller is protected by a plastic cover. External connections are made via screw terminals.

The controller can be mounted to a panel by means of screws, or to Euro-rails (DIN 46277, Blatt 3) by means of mounting clips (see "Accessories").

Inputs

The 32 inputs are arranged in 8 groups of 4, each input being galvanically isolated by photo-isolators (Fig. 1). A delay circuit (delay time typ. 1 ms) is incorporated in each input to increase noise immunity.

Active voltage ('1' level)	16 to 30 V
Non-active voltage ('0' level)	0 to 7 V
Input current, active at 24 V	typ. 10 mA

The input terminals are marked 8.0 to 15.3, in accordance with their fixed addresses in the scratchpad memory.

Outputs

The 20 outputs are arranged according to Fig. 2.

Supply voltage, V_{S2}	18 to 30 V
Minimum load resistance, R_L	120 Ω
Maximum output current at 24 V	200 mA

The output terminals are marked 3.0 to 7.3, in accordance with their fixed addresses in the scratchpad memory.

NOTE

Since the inputs and outputs have fixed addresses 3 to 15 in the scratchpad memory, the relevant I/O-phase should only be specified within this field (to be programmed as LST!015, END3).

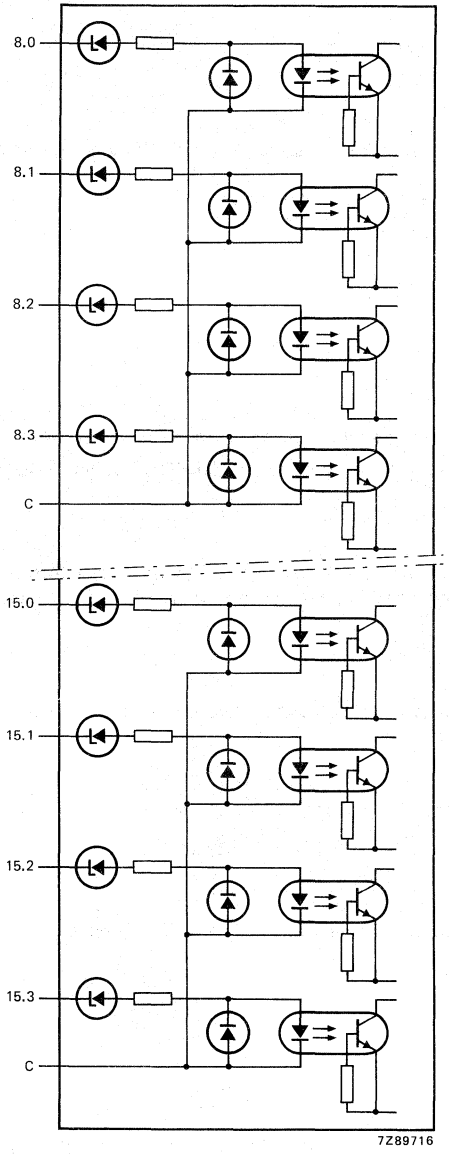


Fig. 1 Configuration of input stages.

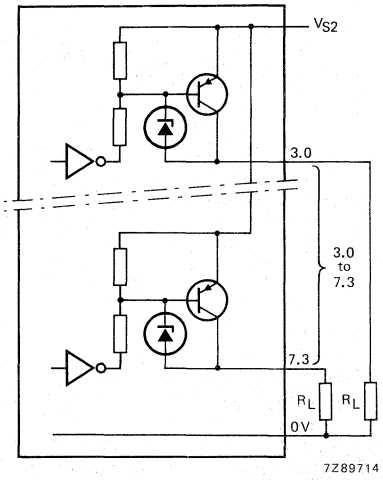


Fig. 2 Configuration of output stages.

Program memory

Two empty EPROMs (2716) are supplied with the MC20 (inside the cover) having a capacity of 2048 instructions. For programming instructions, see "Programming and monitoring".
The programmed EPROMs (A and B) should be inserted into the sockets as shown in Fig. 3.

Scratchpad memory

The scratchpad memory has a capacity of ½k4 (512 words of 4 bits).

Fixed scratchpad memory addresses are:

0.0 – overflow bit
0.1 – constant '1' level
0.2 – alarm supply voltage ($V_{S1} < 18$ V)
0.3 – timer clock 10 ms
1.0 – timer clock 100 ms
1.1 – timer clock 1 s
1.2 – timer clock 10 s
1.3 – timer clock 1 ms
3.0 to 7.3 – outputs
8.0 to 15.3 – inputs
240 to 255 – potentiometer settings

No battery back-up is provided for the scratchpad memory.

Adjustments of software timers

Eight potentiometers (P, Fig. 3) provide adjustment of software timers. The potentiometer setting is converted into a two-decade BCD-value (0 to 99), and stored in the scratchpad memory at two consecutive addresses when the system is in the UDC-phase. The potentiometer settings are scanned sequentially and each time a conversion is completed and the system is in the UDC-phase the scratchpad memory is updated. The conversion of one potentiometer setting takes a maximum of 0,5 ms.

The results of the conversions are stored at the scratchpad memory addresses 240 to 255; the setting of potentiometer 1 being stored at the two lowest number addresses 240 and 241 (LSD).

Internal clock periods

The MC20 has 5 crystal-controlled timer clocks, which are accessible at fixed scratchpad memory addresses 0.3 to 1.3.

24 V/5 V d.c.-d.c. converter

The logic part of the controller has a supply voltage of 5 V. To allow the controller to be directly operated in a machine control system with a supply of 24 V, the MC20 has a 24 V/5 V d.c.-d.c. converter. If the supply voltage to the converter, V_{S1} (24 V), falls below 18 V the alarm input (scratchpad memory address 0.2) becomes '1'.

Automatic reset

When the supply voltage is switched on, the control system generates an automatic reset. This resets the whole system, including setting all locations in the scratchpad memory to '0'. A system reset also occurs if the supply voltage (V_{S1}) falls below 16 V.

The system has a pushbutton (R, Fig. 3) for manual reset (cover to be removed).

System speed

The system execute time depends on the types of instructions used. The execute time of read instructions and all conditional instructions of which the condition is false is 2,5 μs/instruction. For an average program of 1k instructions the cycle time is typically 3 ms.

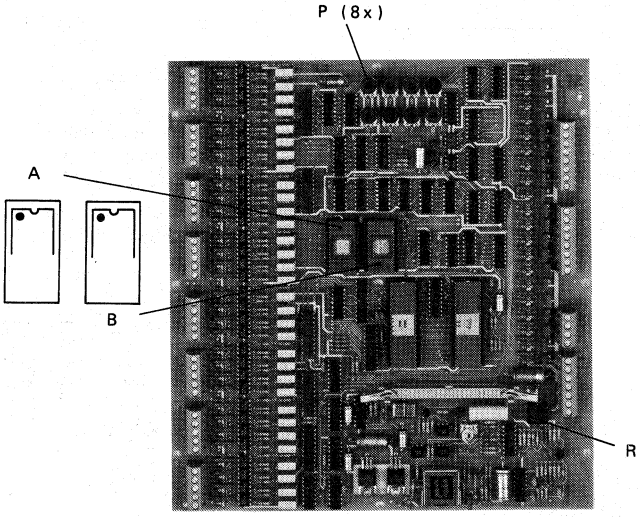


Fig. 3 Microcontroller; cover removed.

Supply

Supply voltage	for 24 V/5 V d.c.-d.c. converter	V_{S1}	24 V ± 25%
Supply current		I_{S1}	typ. 100 mA max. 130 mA
Supply voltage	for output circuitry, exclusive load current	V_{S2}	24 V ± 25%
Supply current		I_{S2}	max. 250 mA

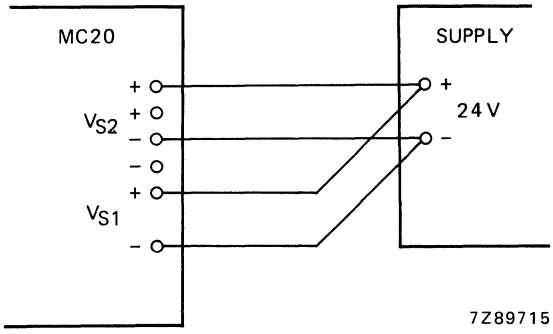


Fig. 4 Connection of supply voltages.

Programming and monitoring

Programming unit PU20, in conjunction with microcontroller interface MI20, can be used to program and monitor the MC20. The MI20 contains an RI20 module (2k16 CMOS RAM + interface) and a PU23* module. The MC20 can be connected to the RI20 with a 50-core flat cable.

The program can also be developed with a PC20-system.

Note that an MC20-program in the EPROMs cannot be monitored when the PU20 is in the EDIT-mode, or in the MONITOR CONT-mode when the UDC-key is operated.

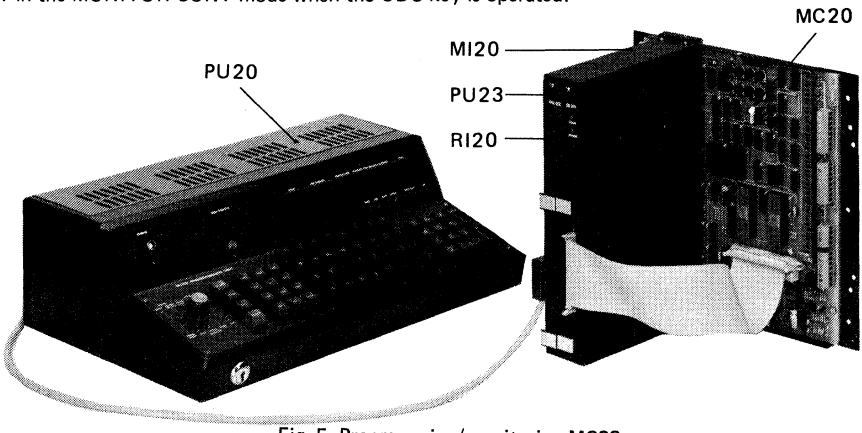


Fig. 5 Programming/monitoring MC20.

* To be ordered separately.

MECHANICAL DATA

Dimensions in mm

Outlines

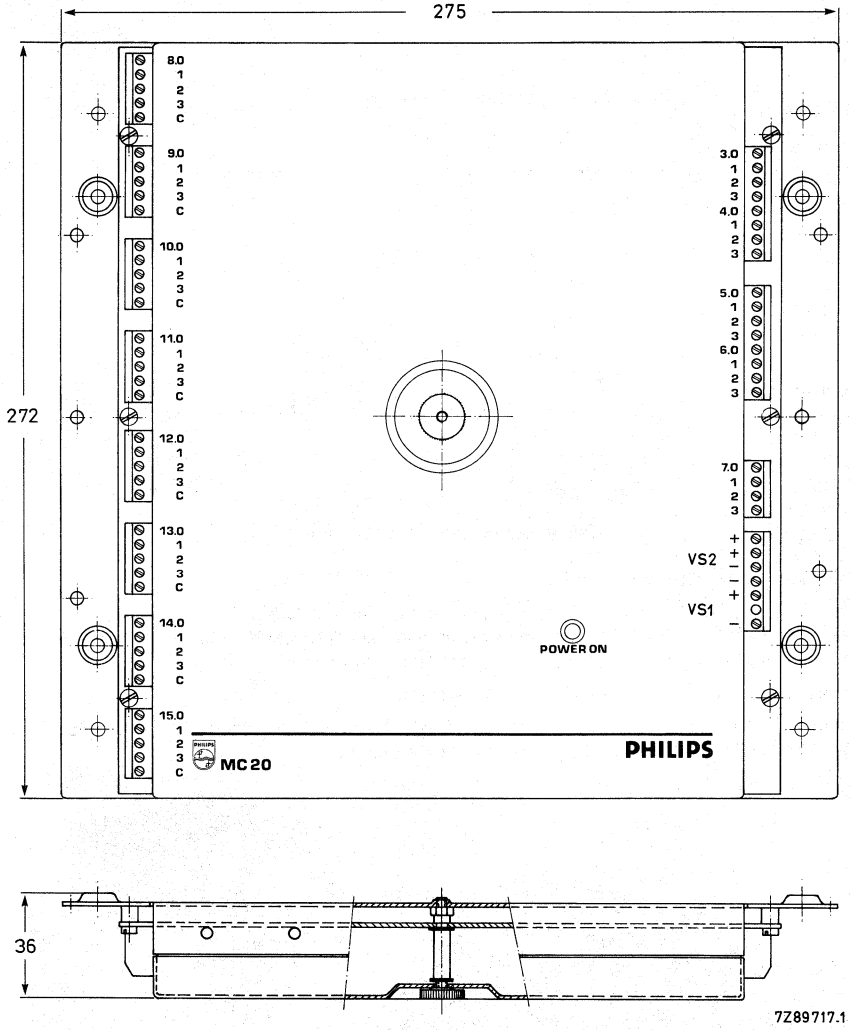


Fig. 6.

ACCESSORIES

For mounting the microcontroller to Euro-rails, snap-on mounting clips MB20 can be supplied; catalogue number of set of 4 clips: 4322 027 23080.

ENVIRONMENTAL DATA

Operating temperature range	0 to + 60 °C
Storage temperature range	−40 to + 70 °C

TESTS AND REQUIREMENTS

The MC20 is designed to meet the tests below.

Vibration test

IEC 68-2-6, test method Fc: 10 to 55 Hz, amplitude 0,75 mm or 5g (whichever is less).

Shock test

IEC 68-2-27, test method Ea: 3 shocks in 6 directions, pulse duration 11 ms, peak acceleration 50g.

Rapid change of temperature test

IEC 68-2-14, test method Na: 5 cycles of 2 h at −40 °C and 2 h at + 85 °C.

Damp heat test

IEC 68-2-3, test method Ca: 21 days at 40 °C, R.H. 90 to 95%.

MICROCONTROLLER INTERFACE

This microcontroller interface is used between an MC20 system and the programming unit PU20. Via this interface the PU20 obtains access to the system for programming and monitoring.

The MI20 is a metal housing, containing a RAM/interface unit RI20 and a programming unit interface PU23; the PU23 has to be ordered separately under catalogue number 4322 027 94180. The RI20 forms an interface between the PU23 and the MC20; it has a 2k16 C-MOS RAM program memory for programming the MC20 system.

The metal housing MI20 can be fitted to the MC20 by means of a quick-coupling system. A 50-pole male header F303 at the front of the RI20 provides electrical connection to the MC20 via a 50-core flat cable, which is supplied with the MI20.

The MI20 performs two modes of operation for programming and monitoring the MC20 system, which are indicated by LEDs at the front panel of the RI20.

PROM mode (PROM LED is on): for the MC20 system, operating on a program that is stored in its EPROM memory. The MI20 is automatically set to this mode when the system is switched on.

RAM mode (RAM LED in on): for the MC20 system, operating on a program that is stored in the program memory of the RI20. The MI20 is set to this mode by pushing the button at the front of the RI20; the actual setting takes place when the MC20 comes in the UDC phase.

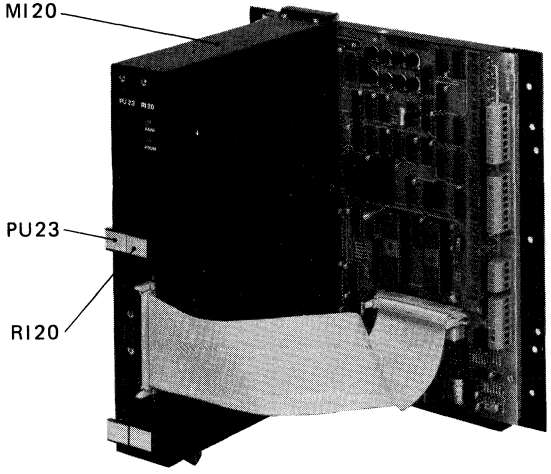


Fig. 1.

In the PROM mode an MC20 program cannot be monitored when the PU20 is in the EDIT mode, or in the MONITOR CONT mode when the UDC key is operated. In the latter case the END instruction also cannot be monitored.

When the EPROM sockets on the MC20 are empty and a program has to be written into the RAMs of the MI20 the following procedure has to be followed.

- Switch on the PU20, select EDIT mode and line number 0, and push ENTER key.
- Switch on the MC20/MI20 system; the PROM LED on the front plate of the RI20 lights and the PU20 displays 27 0000.
- Push the button on the front plate of the RI20; the RAM LED lights and the system is ready for RAM programming.

ELECTRICAL DATA

Supply voltage Supply current	from MC20 via flat cable	V_P I_P	5 V + 5% typ. 80 mA
Data retention with on-board battery			min. 7 days, provided the module is in operation for at least 10 h.

Input and output data

	function	terminations of male header at the front of RI20
BI-DIRECTIONAL BUSSES		
ADD_0	Scratchpad memory address bus.	21
ADD_1		22
ADD_2		29
ADD_3		30
ADD_4		31
ADD_5		32
ADD_6		33
ADD_7		20
ADD_8		19
ADD_9		18
ADD_{10}		34
APM_0	Program memory address bus.	36
APM_1		37
APM_2		38
APM_3		39
APM_4		40
APM_5		41
APM_6		42
APM_7		43
APM_8		44
APM_9		45
APM_{10}		46

	function	terminations of male header at the front of RI20
DIO_0	Scratchpad memory data bus.	9
DIO_1		8
DIO_2		10
DIO_3		11
INS_0	Instruction bus	14
INS_1		13
INS_2		12
INS_3		16
INS_4		17
INPUTS		
APF	Timing signal from MC20 to PU23	1
CLOCK	Clock signal to PU23	48
CPSI	Signal from PU23 to stop MC20 in UDC phase	4
PHC_0	Phase control outputs from MC20	7
PHC_1		6
$\overline{RESET}$	Reset output from MC20 (active low).	23
RR	Output Result Register from MC20.	35
SBI	Clock signal from MC20 to RI20 and PU23.	15
OUTPUTS		
CPDC	Timing pulse to clock data in program memory data latch on MC20 during UDC phase.	2
CPSC	Signal from MC20 to PU23 indicating that MC20 has been stopped.	50
HOLD	Signal from PU23 to hold MC20.	5
PDLE	Program memory data latch enable.	49
WDSM	Signal from PU23 to write data on DIO bus into scratchpad memory.	47

MECHANICAL DATA

Dimensions in mm

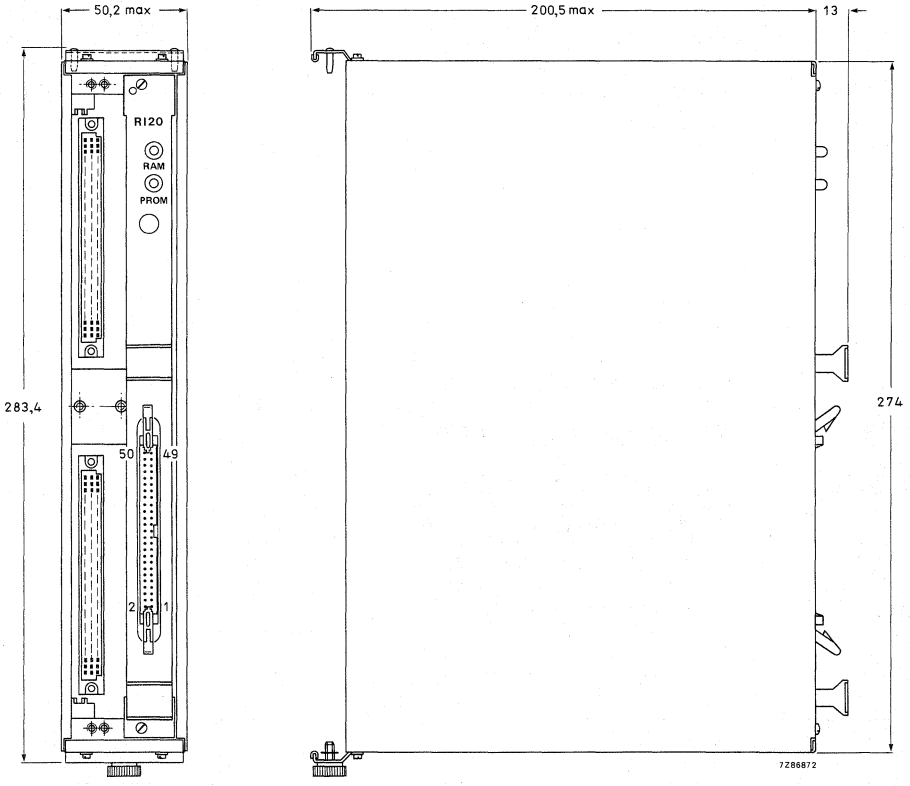


Fig. 2.

Mass: 1,5 kg

TERMINAL LOCATION

Terminations of male header at the front of RI20

APF	1	2	CPDC
n.c.	3	4	CPSI
HOLD	5	6	PHC_1
PHC_0	7	8	DIO_1
DIO_0	9	10	DIO_2
DIO_3	11	12	INS_2
INS_1	13	14	INS_0
SBI	15	16	INS_3
INS_4	17	18	ADD_9
ADD_8	19	20	ADD_7
ADD_0	21	22	ADD_1
$\overline{\text{RESET}}$	23	24	n.c.
0V	25	26	0V
V_P	27	28	V_P
ADD_2	29	30	ADD_3
ADD_4	31	32	ADD_5
ADD_6	33	34	ADD_{10}
RR	35	36	APM_0
APM_1	37	38	APM_2
APM_3	39	40	APM_4
APM_5	41	42	APM_6
APM_7	43	44	APM_8
APM_9	45	46	APM_{10}
WDSM	47	48	CLOCK
$\overline{\text{PDLE}}$	49	50	CPSC

n.c. = not connected.

PROGRAMMING UNIT

DESCRIPTION

This mains-powered programming unit is for loading, checking, dumping and monitoring the control program of the PC20-system. It provides access to the program memory and the scratchpad memory. The programming unit is a desk-top apparatus. The program is written into the program memory via the keyboard (Fig. 1) or other sources e.g. tape readers, cassette recorders, program developing systems. The program is monitored by the display or, for example, by an external VDU.

The programming unit must be used in conjunction with the programming unit interface PU21/PU23 (placed in the PC rack), to which it is connected via an 8-core cable. The circuits of the PU20 and the PU21/PU23 are galvanically isolated from each other by means of photo-isolators. The data transport via the data-in and data-out lines is serial.

After loading the program into the program memory, the programming unit can be removed to be used in another PC-system. If necessary, for monitoring purposes for example, it is very easy to connect the PU20 to the system again.

The programming unit is provided with two sockets for EPROMs, type 2716 (2k bytes). Programming of the EPROMs is done in such a way that each program word is distributed over two EPROMs, A and B (Fig. 1). EPROM A contains the instruction and the most significant digit of the address and EPROM B contains the remaining digits. The programmed EPROMs can be used in central processor CP20, program memory module MM20 and microcontroller MC20.

The programming unit has the following 10 modes of operation.

1. EDIT: creating a new program or changing an existing program.
2. MONITOR CONT: continuous monitoring the PC20-system in operation; on-line change facilities.
3. MONITOR CYCLE: monitoring the PC20-system, which operates on command for one cycle.
4. MONITOR STEP: monitoring the PC20-system, which executes on command one program line.
5. PROM PROG: dumping the program from the PC20-system into the EPROMs in the sockets of the programming unit.
6. DUMP CASS: dumping the program from the PC20-system onto cassette tape.
7. DUMP RS449/423: dumping the program from the PC20-system into peripheral equipment with EIA-standard specification RS449/423.
8. LOAD PROM SOCK: loading the program from the EPROMs in the sockets of the programming unit into the PC20-system.
9. LOAD CASS: loading the program from cassette tape into the PC20-system.
10. LOAD RS449/423: loading the program from peripheral equipment with EIA-standard specification RS449/423 into the PC20-system.

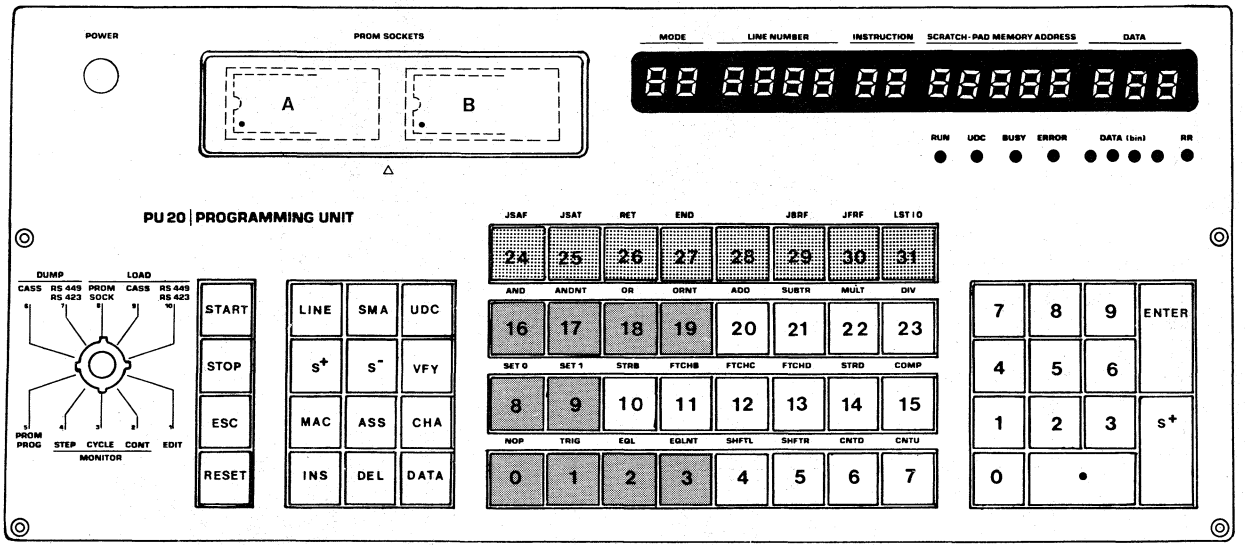
A keyswitch is provided. Without the key a user can only monitor system operation and check the states of scratchpad memory locations; a user with a key has full command over all functions.

MECHANICAL DATA

Dimensions	see Fig. 2
Mass	approx. 6,3 kg

ENVIRONMENTAL DATA

Operating temperature range	0 to 45 °C
Storage temperature range	−40 to + 70 °C



7Z80140.1

Fig. 1 Keyboard and display lay-out.

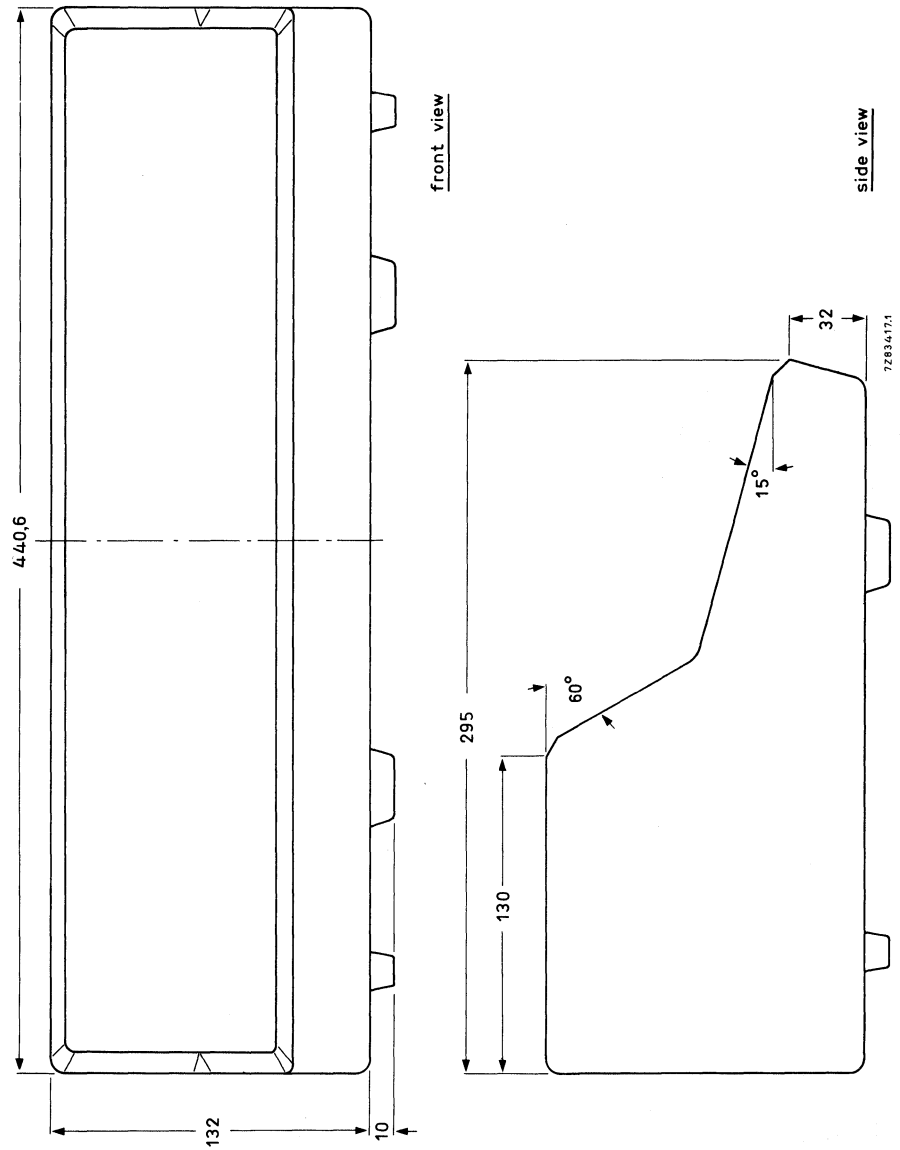


Fig. 2 Outline dimensions (in mm).

ELECTRICAL DATA

Mains voltage	110, 127, 220 or 240 V; tolerance + 10%, −15%
Mains frequency	46 to 65 Hz
Fusing	
for 110 or 127 V mains	200 mA (delayed action fuse)
for 220 or 240 V mains	100 mA (delayed action fuse)
Power consumption	20 VA

On delivery the programming unit is adjusted to 220 V mains voltage. If the local voltage is different, the switch at the rear must be set to the required position and the fuse must be replaced.

CONNECTING FACILITIES (see Fig. 4)

- Fixed mains cable (1) with plug with side earth-contact; length 2,4 m.
- Fixed 8-core cable (2) with 9-pole female plug F161, for connection to programming unit interface PU21/PU23; length 2,5 m. For terminal location see Table 1.
- EIA-standard interface connector plug (3), according to RS449/423, for connecting data terminal equipment (DTE), like CRT terminals, punchers, printers, readers. The pins 4, 6 and 19 are operational, along which data exchange can take place. For data terminal equipment, which requires more interconnections, Table 2 should be consulted.

  Note: The programming unit is data circuit terminating equipment (DCE), configuration type DT (Data and Timing only).
- DIN-socket (4) for connecting a normal audio cassette recorder (see also Fig. 3). To avoid drop-outs it is recommended that C60 Super Quality Ferrochromium cassette tape be used.
- Two sockets for EPROMs, type 2716 (2k bytes) or 2758 (1k bytes).

  Note: At the rear of the programming unit provisions (5) are made for stowage of the mains cable and the 8-core cable during transport.

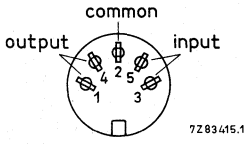


Fig. 3 DIN audio socket.

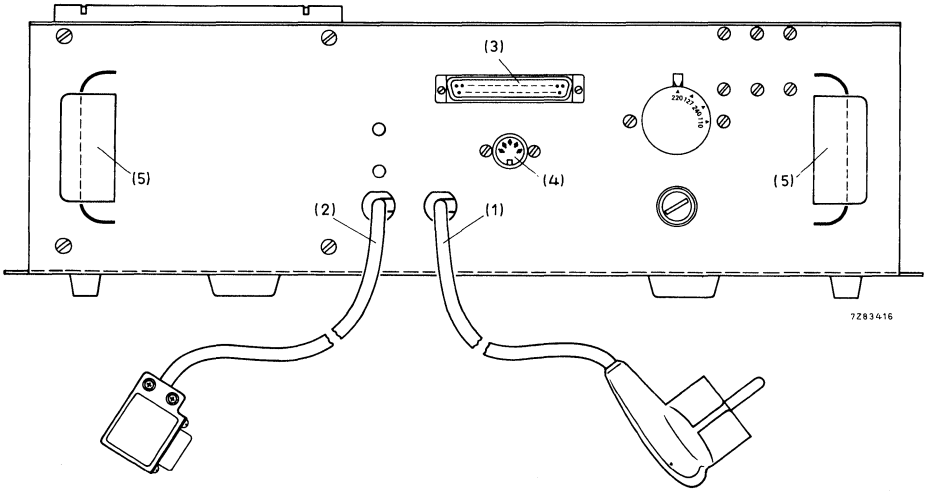


Fig. 4 Rear view.

Table 1 Terminal location of connecting cable to PU21/PU23

terminal	function
1.	connected to terminal 6
2. $\overline{\text{CLDT}}$	clock signal for data transfer between PU20 and PU21/PU23
3. $\overline{\text{TRANSFER}}$	data transfer required by PU20
4. $\overline{\text{SSE}}$	system stop enable
5.	+ 5 V *
6.	connected to terminal 1
7. $\overline{\text{DPI}}$	data from PU20 to PU21/PU23
8. DIP	data from PU21/PU23 to PU20
9. READY	ready signal to PU20, indicating that PU21/PU23 is available for data transfer

* No supply line; is used as a common line for the control signals.

Table 2 Terminal location of RS449/423 plug

terminal	function	operational	dummy ON	dummy OFF	jumper 1	jumper 2
2	SI – signalling route indicator		X			
4	SD – send data	X				
6	RD – receive data	X				
9	CS – clear to send					X
11	DM – data mode					X
12	TR – terminal ready					X
13	RR – receiver ready					X
15	IC – incoming call			X		
18	TM – test mode			X		
19	SG – signal ground	X			X	
20	RC – receive common				X	
33	SQ – signal quality		X			
36	SB – stand-by indicator			X		
37	SC – send common				X	

PROGRAMMING UNIT INTERFACES

DESCRIPTION

The programming unit interface can be used between a PC20-system or MC20-system (in conjunction with microcontroller interface MI20) and the programming unit PU20 which obtains access to the system via this interface*. The programming unit interface does not form an essentail part of an operating system which can function normally without it.

Figure 1 is a block diagram of the programming unit interface which has direct access to the data, address and control lines of the PC20/MC20-system. Furthermore it is connected to the PU20 via an 8-core cable, which contains a data-in, transfer, clock, ready, system stop enable and a common line. These lines are galvanically isolated from the PU21/PU23 circuitry by photo-isolators. The data transport via the data-in and data-out lines is serial. All actions to be executed are commanded by the PU20 through a 4-bit function mode code. This code is transmitted, with the other data to the programming unit interface, in both normal and inverted form so that correct reception can be verified.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card**). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels. At the front of the unit a 9-pole male connector F161 allows connection of the cable from the programming unit.

* The PU21 can only be used with a PC20-system.

** For a general description of the Euro-card system see IEC 297 or DIN41494 for 19-in racks and IEC 130-14 or DIN41612 for connectors.

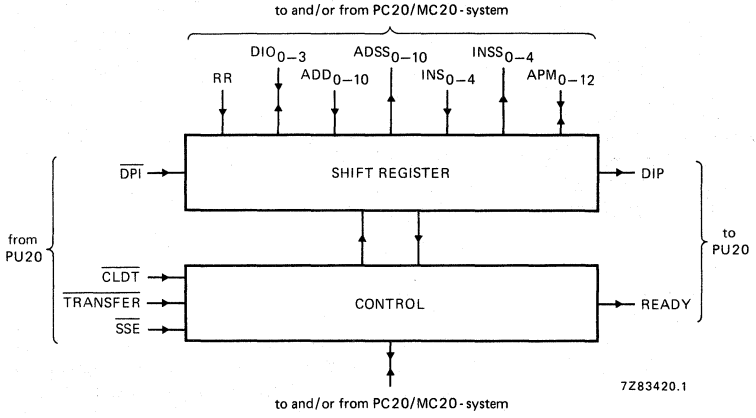


Fig. 1 Simplified block diagram.

ELECTRICAL DATA

Supply

		PU21	PU23
→ Supply voltage (d.c.)	V_p	10 V ± 10%	5 or 10 V ± 10%
current	I_p	max. 20 mA	max. 20 mA

Input and output data

All inputs and outputs meet the standard LOCMOS specifications.

	function	terminations (Fig. 2)	
		connector 1	connector 2
BI-DIRECTIONAL DATA BUSSES			
APM_0 APM_1 APM_2 APM_3 APM_4 APM_5 APM_6 APM_7 APM_8 APM_9 APM_{10} APM_{11} APM_{12}	Program memory address bus; $APM_{0\text{-}12}$ act as outputs when PABE is LOW (only during UDC-phase).		a16, c16 a17, c17 a18, c18 a19, c19 a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28
DIO_0 DIO_1 DIO_2 DIO_3	Data to or from scratchpad memory, controlled by WEPC.	a19, c19 a20, c20 a21, c21 a22, c22	
INPUTS			
ADD_0 ADD_1 ADD_2 ADD_3 ADD_4 ADD_5 ADD_6 ADD_7 ADD_8 ADD_9 ADD_{10}	Program memory data bits from central processor (address bus).	a6 a7 a8 a9 a10 a11 a12 a13 a14 a15 a16	
CLOCK	Clock input from central processor for timing purposes.		a7, c7
CPSC	Input that indicates that the central processor has been stopped (HIGH) in the UDC-phase.		a5, c5
INS_0 INS_1 INS_2 INS_3 INS_4	Program memory data bits from central processor (instruction bus).	a1 a2 a3 a4 a5	

	function	terminations (Fig. 2)	
		connector 1	connector 2
PB_0 PB_1	Page bits.	a17, c17	
PHC_0 PHC_1	Phase control from central processor.	c23 a23,	
RR	Result register.	a18, c18	
SBI	Store command.	c26	
OUTPUTS			
$ADDS_0$ $ADDS_1$ $ADDS_2$ $ADDS_3$ $ADDS_4$ $ADDS_5$ $ADDS_6$ $ADDS_7$ $ADDS_8$ $ADDS_9$ $ADDS_{10}$	Program memory data bits (address bus) to be stored in the program memory on CP21/CP24, MM21/MM22 or RI20*, or address bits for scratch-pad memory to read data from or to write data in the scratchpad memory. Three-state outputs, enabled when PDBE is LOW (only during UDC-phase).	c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c16	
CPSD	Central processor slow down; command to central processor is only effective when the PU20 has been connected to the PU21/PU23.		a3, c3
CPSI	Central processor stop initiate; command to central processor (active HIGH) to stop in UDC-phase.		a4, c4
HOLD	Command to stop the central processor during the DP-phase (active LOW).		a6, c6
$INSS_0$ $INSS_1$ $INSS_2$ $INSS_3$ $INSS_4$	Program memory data bits (instruction bus) to be stored in the program memory of CP21/CP24, MM21/MM22 or RI20*. Three-state outputs, enabled when PDBE is LOW (only during UDC-phase).	c1 c2 c3 c4 c5	
PABE	Program memory address bus enable to central processor; APM_{0-12} terminals of PU21/PU23 act as outputs when PABE is LOW (only during UDC-phase).		a1, c1
PDBE	Program memory data bus enable. $INSS_{0-4}$ and $ADDS_{0-10}$ act as outputs when PDBE is LOW (only during UDC-phase).		a2, c2

* Not for PU21.

	function	terminations (Fig. 2)	
		connector 1	connector 2
$\overline{R}$/WPM	Write signal to CP21/CP24, M21/M22 or RI20* to store data in program memory (active HIGH).		a14, c14
WEPC	Write enable signal to central processor; prepares central processor to store data on DIO_{0-3} in scratchpad memory (active LOW, only during UDC-phase).	c28	
WPSM	Write pulse for scratchpad memory; signal to store data on DIO_{0-3} into scratchpad memory.		a13, c13

Connection to programming unit PU20

line	function	terminations (Fig. 2) connector 3
$\overline{CLDT}$	clock signal for data transfer between PU20 and PU21/PU23.	2
DIP	data from PU21/PU23 to PU20.	8
$\overline{DPI}$	data from PU20 to PU21/PU23.	7
READY	ready signal to PU20, indicating that PU21/PU23 is available for data transfer.	9
$\overline{SSE}$	system stop enable.	4
$\overline{TRANSFER}$	data transfer required by PU20.	3

* Not for PU21.

MECHANICAL DATA

Dimensions in mm

Outlines

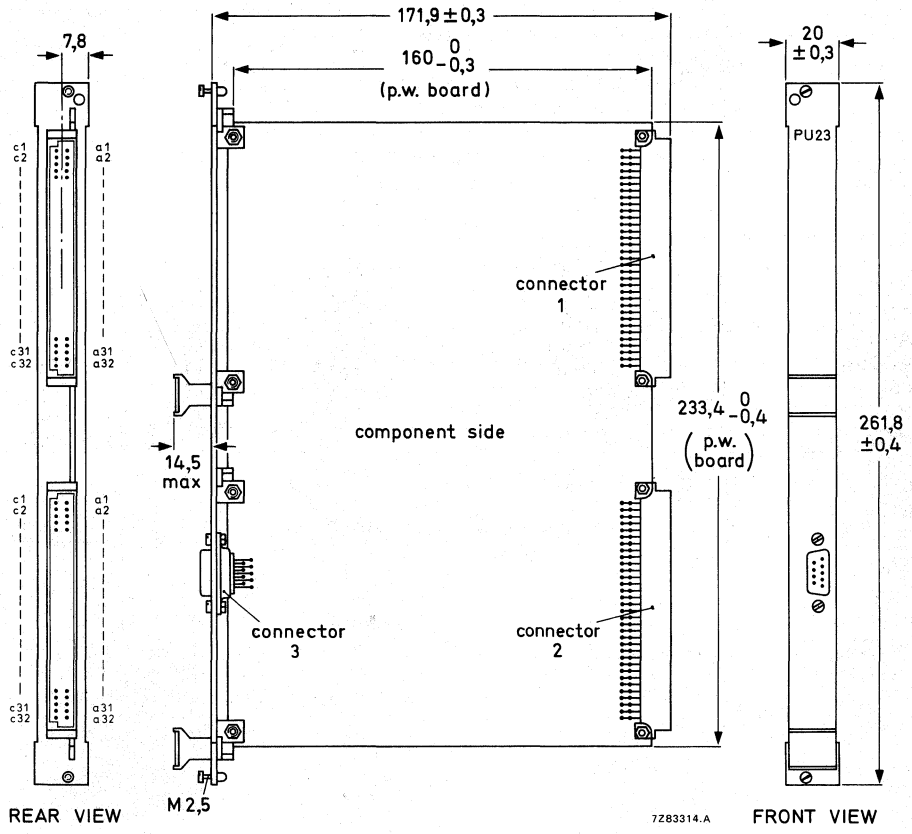


Fig. 2.

Mass approx. 270 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
$INSS_0$	1	INS_0	PABE	1	PABE
$INSS_1$	2	INS_1	PDBE	2	PDBE
$INSS_2$	3	INS_2	CPSD	3	CPSD
$INSS_3$	4	INS_3	CPSI	4	CPSI
$INSS_4$	5	INS_4	CPSC	5	CPSC
$ADDS_0$	6	ADD_0	HOLD	6	HOLD
$ADDS_1$	7	ADD_1	CLOCK	7	CLOCK
$ADDS_2$	8	ADD_2	n.c.	8	n.c.
$ADDS_3$	9	ADD_3	n.c.	9	n.c.
$ADDS_4$	10	ADD_4	n.c.	10	n.c.
$ADDS_5$	11	ADD_5	n.c.	11	n.c.
$ADDS_6$	12	ADD_6	n.c.	12	n.c.
$ADDS_7$	13	ADD_7	$\overline{WPSM}$	13	$\overline{WPSM}$
$ADDS_8$	14	ADD_8	$\overline{R}$/WPM	14	$\overline{R}$/WPM
$ADDS_9$	15	ADD_9	n.c.	15	n.c.
$ADDS_{10}$	16	ADD_{10}	APM_0	16	APM_0
PB_1	17	PB_0	APM_1	17	APM_1
RR	18	RR	APM_2	18	APM_2
DIO_0	19	DIO_0	APM_3	19	APM_3
DIO_1	20	DIO_1	APM_4	20	APM_4
DIO_2	21	DIO_2	APM_5	21	APM_5
DIO_3	22	DIO_3	APM_6	22	APM_6
PHC_0	23	PHC_1	APM_7	23	APM_7
n.c.	24	n.c.	APM_8	24	APM_8
n.c.	25	n.c.	APM_9	25	APM_9
SBI	26	n.c.	APM_{10}	26	APM_{10}
n.c.	27	n.c.	APM_{11}	27	APM_{11}
WEPC	28	n.c.	APM_{12}	28	APM_{12}
n.c.	29	n.c.	n.c.	29	n.c.
n.c.	30	n.c.	n.c.	30	n.c.
V_p	31	V_p	V_p	31	V_p
0 V	32	0 V	0 V	32	0 V

Connector 3 (front panel)

1	i.c.
2	$\overline{CLDT}$
3	$\overline{TRANSFER}$
4	$\overline{SSE}$
5	+ 5 V*
6	i.c.
7	$\overline{DPI}$
8	DIP
9	READY

n.c. = not connected
i.c. = internal connected

* No supply line; is used as a common line for the control signals.

BACK PANELS

APPLICATION

These back panels are for use in 19 inch racks, to accommodate the modules of the PC20 system. Use of these panels eliminates the need to wire separate connectors to receive the modules.

DESCRIPTION

The back panels incorporate female connectors which mate with the male counterparts of the PC20 modules. Type BP23 consists of two back panels. The upper panel (BP23A) provides the required interconnections for connector 1 of a PU21/PU23, MM module, CP module and of eighteen input/output modules. It has solder pads for allocation of the addresses of the input/output modules. The lower panel (BP23B) provides the interconnections for connector 2 of a PU21/PU23, MM module and CP module. External connections to the lower connectors of the input/output modules must be made individually; for this purpose connecting cables are available, see Table 1. Back panels BP25 and BP26 are used in extension racks to accommodate additional input/output modules. Type BP25 is for 15 input/output modules, type BP26 for 21. These types, of course, are only upper back panels.

The back panels carry a four-terminal block for external connection of the 10 V supply. Interconnection between the panels can be made via a ribbon cable (see Table 2); for this purpose, the panels incorporate an F303 male header.

The back panels are fixed to the rack with M2,5 x 10 screws, using threaded rails and isolation strips.

Table 1 Connecting cables

type	description	catalogue number
CC20	connecting cable for module OM21	9390 293 50000
CC21	connecting cable for module SO20	9390 293 60000
CC22	connecting cable for module IM20	9390 293 70000
CC23	connecting cable for modules IM20 and OM20	9390 293 80000

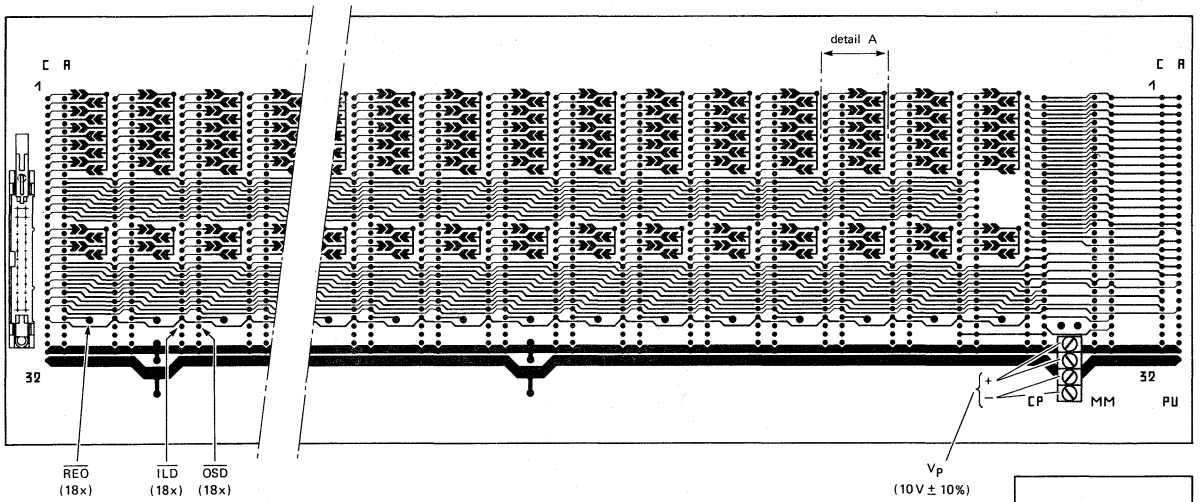
Table 2 Bus extension cables

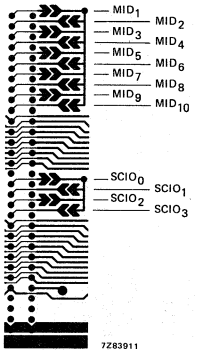
type	description	catalogue number
BC21	bus extension cable for one extension rack	9390 293 90000
BC22	bus extension cable for two extension racks	9390 294 00000
BC23	bus extension cable for three extension racks	9390 298 90000

Note: When more than two extension racks are used, it is advisable to use bus interface BI20 * between back panel BP23 and the first extension rack.

* Catalogue number 4322 027 94170.

4322 027 94010
4322 027 94030
4322 027 94040





detail A

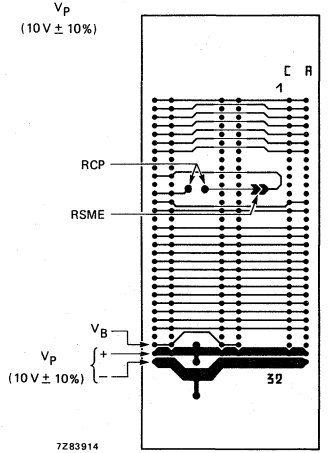


Fig. 1 Back panels BP23A (upper) and BP23B (lower), seen from rear of rack.
CP = central processor;
MM = memory module;
PU = programming unit interface (PU21/PU23).

For terminal location of the male header, see last page of this data sheet.

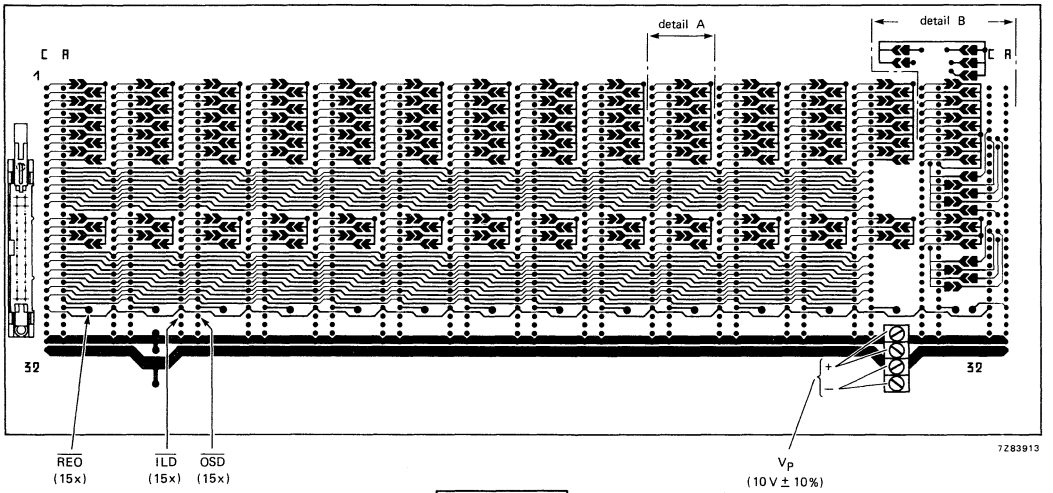
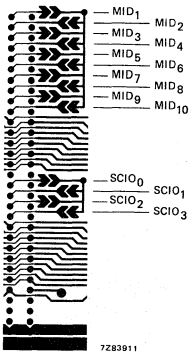
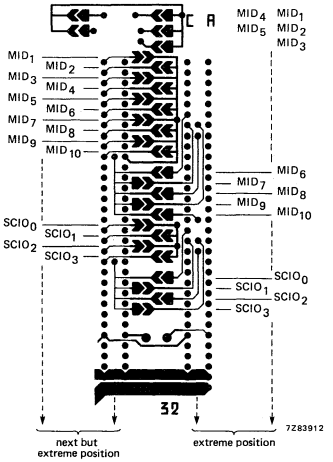


Fig. 2 Back panel BP25, see from rear of rack.

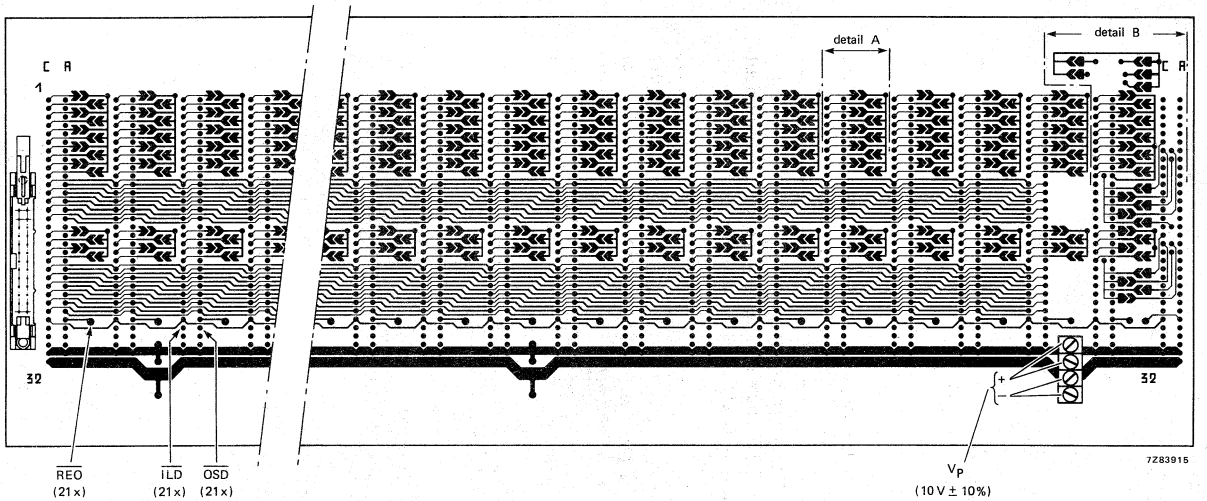
For terminal location of the male header, see last page of this data sheet.

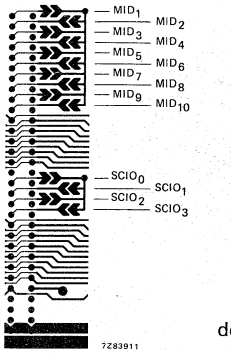


detail A

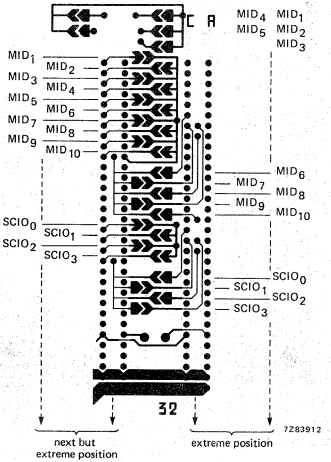


detail B





detail A



detail B

Fig. 3 Back panel BP26, seen from rear of rack.

For terminal location of the male header, see last page of this data sheet.

Connection of control signals and external battery

Control signals can be connected to the connecting points on the rear side of the back panels (see Figs 1, 2 and 3. The functions of the control signals are indicated in the table below.
RCP and RSME signals are only applicable to panel BP23A.

connecting points	function
$\overline{ILD}$	Indication LED disable; input current low: 0,1 mA.
$\overline{REO}$	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current low: 0,1 mA.
$\overline{OSD}$	Output stage disable for all stages; input current low: 0,1 mA.
RCP	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active low: input current = 2 mA.
RSME	Reset scratchpad memory enable. When high or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When low (input current is 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.
V_B	External battery connection for saving the contents of the program memory and/or the scratchpad memory, in case of power failure. If central processor CP21/CP24 or memory module MM21/MM22 is used, this battery is parallel to the on-board battery and the retention time is lengthened.

Allocation of addresses of input/output modules

Each group of four inputs and outputs of an input/output module has a discrete address in the scratch-pad memory of the central processor. This address is allocated by bridging the appropriate MID-pads (MID_1 to MID_{10}) on the back panels.

Separation of inputs and outputs of modules RP20 and RS20

Inputs and outputs are separated by bridging the appropriate SCIO-pads ($SCIO_0$ to $SCIO_3$) on the back panels.

Connection for logic supply voltage

The logic voltage (V_p) is 10 V ± 10%. It can be connected to the four-terminal connecting block on the back panels. This connection is only applicable if there is no SO20 module provided.

Note: For full information see PC20 user manual.

→ **Terminal location of F303 male header**

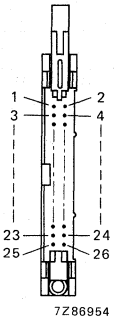


Fig. 4 Male header, seen from rear of rack.

ADD_0	1	2	ADD_1
ADD_2	3	4	ADD_3
ADD_4	5	6	ADD_5
ADD_6	7	8	ADD_7
ADD_8	9	10	ADD_{10}
V_P	11	12	ADD_9
DIO_1	13	14	DIO_0
DIO_3	15	16	DIO_2
PHC_1	17	18	PHC_0
PRF	19	20	$R/\overline{W}$
DEF	21	22	0 V
APF	23	24	SBI
0 V	25	26	RCO

SMALL CONTROLLER CABINET

APPLICATION

This cabinet is designed for accommodating PC20 modules, for easy assembling of small controller systems.

DESCRIPTION

This metal cabinet houses a programming unit interface PU21/PU23, a central processor CP20 or CP21/CP24, a supply and output module SO20 and six input/output modules.

The cabinet has back panels, so the work of wiring separate connectors to receive the male connectors of the modules is eliminated.

The upper panel BP20 provides the required interconnections for connector 1 of a PU21/PU23, CP20 or CP21/CP24 and an SO20 module, and of six input/output modules. It has solder bridges for allocating the addresses of the input/output modules.

The lower panel BP21 provides the interconnections for connector 2 of a PU21/PU23, CP20 or CP21/CP24 and an SO20 module; type BP22 provides for connector 2 of an input/output module, type BP27 provides for connector 2 of output module OM22. These panels have connecting blocks with screw terminals for connection of supply voltages and input and output circuits. Furthermore, panel BP21 has connecting points for the control signals.

The cabinet is supplied with one panel BP22 but space is provided for another five BP22 or BP27 panels, which must be ordered separately.

The connections to the outside world are protected by the sloping cover on the lower part of the cabinet. Openings in the underside provide entry of the input/output cables. The cabinet is intended for wall mounting.

Note: For larger controller systems, back panels PB23, BP25 and PB26 are available, to be used in 19 inch racks; see the relevant data sheet.

MECHANICAL DATA

Dimensions in mm

Outlines

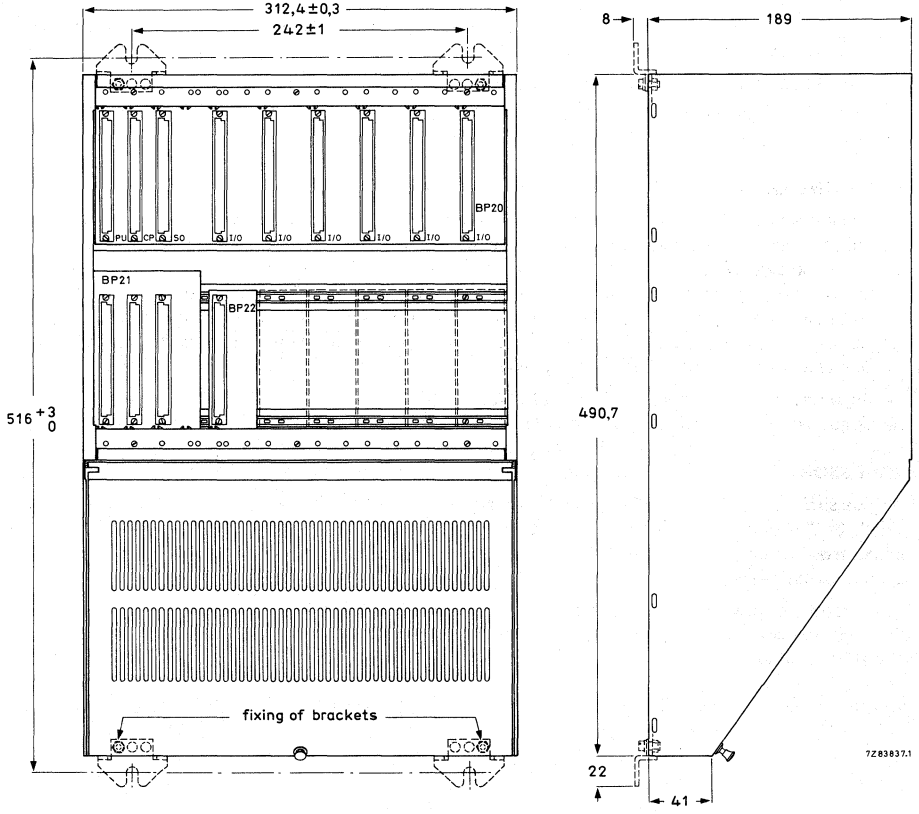


Fig. 1 Small controller cabinet.

Cabinet, material	steel
colour	black
Mass	5,2 kg

ENVIRONMENTAL DATA

Maximum permissible temperature, measured 5 cm above the cabinet 60 °C

MOUNTING OF THE CABINET

Four mounting brackets can be fitted to the cabinet (Fig. 1). They are supplied with bolts and washers with the cabinet.

The cabinet can be fixed to a wall with M6 bolts. In some cases, e.g. if the wall is not flat, it is sufficient to use three mounting brackets (one at the top and two at the bottom of the cabinet).

The cabinet must be positioned so that air has free access.

MOUNTING OF ADDITIONAL BACK PANELS BP22 AND BP27

The back panel BP22 or BP27 has to be positioned through the openings in the bottom of the cabinet, to avoid bending of the panel. It is fitted to the mounting strip in the cabinet by means of the four M2,5 x 10 screws, which are supplied with the cabinet. Two of these screws also secure the female connector. Before tightening the screws, the panel has to be aligned. To this end an input/output module has to be slid carefully into the cabinet, so that its connectors are fully mated with their counterparts on the back panel. The lower two screws can then be tightened and, after removing the module, the fixing screws of the connector can be tightened.

Catalogue number of back panel BP22: 4322 027 92140.
Catalogue number of back panel BP27: 4322 027 93950.

ACCESSORIES

To give sufficient space for connection of the input/output cables to the connecting blocks on back panels BP22 and BP27, the various input/output modules in the cabinet are 15 mm apart. To cover these spaces front plates FP20 are available.
Unused module spaces, can be covered with a front plate FP21.

Catalogue number of front plate FP20 (15 mm width): 4322 027 92150.
Catalogue number of front plate FP21 (20 mm width): 4322 027 92160.

INSTALLATION

Connection of control signals and external battery

Control signals can be connected to the connecting points on the lower end of back panel BP21 (see Fig. 2). The functions of the control signals are indicated in the table below.

Note: Use of control signals $\overline{ILD}$, $\overline{REO}$ and $\overline{OSD}$ requires interconnections between back panels BP20 and BP21 (see Fig. 2).

connecting points	function
$\overline{ILD}$	Indication LED disable; input current low: 0,1 mA.
$\overline{REO}$	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current low: 10 mA.
$\overline{OSD}$	Output stage disable for all stages; input current low: 10 mA.
RCP	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active low: input current = 2 mA.
RSME	Reset scratchpad memory enable. When high or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When low (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.
±BATT	External battery connection for saving the contents of the program/scratchpad memories, in case of power failure. If central processor CP21/CP24 is used, this battery is parallel to the on-board battery and the retention time is lengthened.
ALE	Alarm external; active low as long as V_{ic} is above 17,5 V; with opto-isolater between internal and external supply.

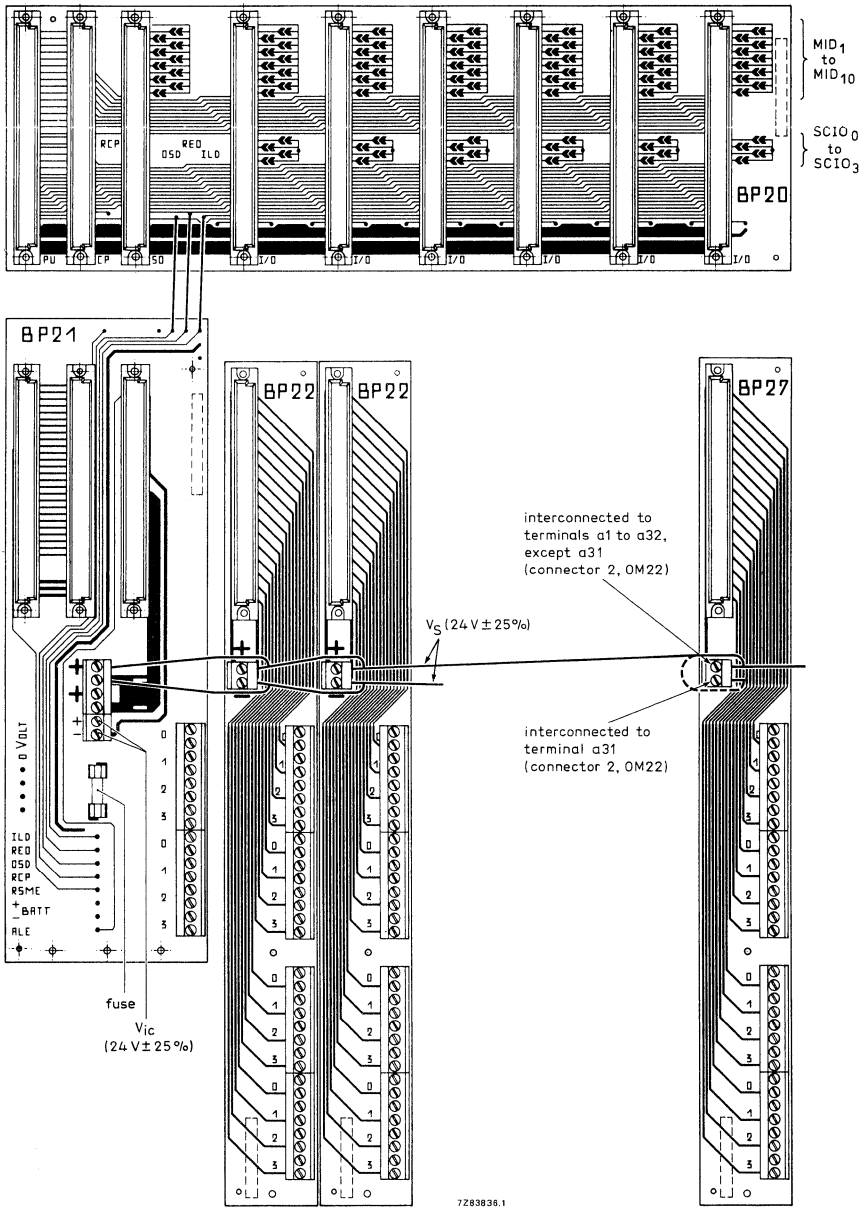


Fig. 2 Back panel arrangement. See also note at the top of the next page.

Note to Fig. 2 on the preceding page: If all outputs of the OM22 are used in grounded load configuration, an interconnection between the two connecting points of the small connecting block of back panel BP27 has to be used (indicated with a dashed line). This interconnection has not to be made if the first 16 output stages of the OM22 are used with pull-down resistors, e.g. to drive TTL circuitry. See also data sheet OM22.

Allocation of addresses of input/output modules

Each group of four inputs and outputs of an input/output module has a discrete address in the scratch-pad memory of the central processor. This address is allocated by bridging the appropriate MID-pads (MID_1 to MID_{10}) on back panel BP20, see Fig. 2.

Coding of inputs and outputs on modules RP20 and RS20

The coding of inputs and outputs is done by bridging the appropriate SCIO-pads ($SCIO_0$ to $SCIO_3$) on back panel BP20, see Fig. 2.

Connection of input and output circuits

The input circuits of the input modules and the output circuits of the output modules should be connected to the large connecting blocks on back panel(s) BP22. The output circuits of the OM22 module should be connected to the large connecting blocks on back panel(s) BP27, those of the SO20 module should be connected to the large connecting block on back panel BP21, see Fig. 2.

Connection of supply voltage for 24 V/10 V d.c.-d.c. converter of module SO20

The supply voltage for the converter (V_{ic}) is 24 V ± 25%. It should be connected to the terminals of the small connecting block on back panel BP21, see Fig. 2. A fuse (I_n = 1,6 A, delayed action) protects the supply against short-circuit in the converter.

Connection of supply voltage for output modules

The supply voltage for the output modules (V_S) is 24 V ± 25%. It should be connected to the double connecting block on back panel BP21 and the small connecting block on the panel(s) BP22 and BP27 (only + connection), see Fig. 2.

Note: For full information see PC20 Manual.

HIGH NOISE IMMUNITY LOGIC

INTRODUCTION

In noisy environments - in data handling and processing, in industrial control, in computer peripherals - you need High Noise Immunity Logic. You need the FZ/30-Series. It gives you a comprehensive range of logic elements - plus such indispensable ancillaries as timers, power amplifiers, lamp or relay drive modules, and interface modules. And they have one outstanding advantage, by adding a capacitor you can slow-down the system response and raise the a.c. noise threshold to meet your needs.

The modules are small, over a hundred would fit on this page, and have an operating temperature range up to 70 °C. Wide voltage tolerances make these circuits first choice for a host of industrial and professional applications. And they're easy to use - a simple loading table tells you what each unit can drive, and what's needed to drive it. And we supply a full set of bits to go round them - input/output devices - printed-wiring boards - connectors - sticker symbols - name it - its in the FZ/30-Series range of auxiliaries.

Check with us for full details of the FZ/30-Series. You get fast, reliable deliveries, attractive quotations, and an applications service that is second to none.

SURVEY OF TYPES

type	description	catalogue number
FZH101/4.NAND32	Quad 2-input NAND gate	2722 006 01081
FZH111/4.NAND30	Quad 2-input NAND gate Two gates can be slowed down	2722 006 01001
FZH121/2.NAND30	Dual 5-input NAND gate	2722 006 01061
FZH131/2.NAND31	Dual 5-input NAND gate Both gates can be slowed down	2722 006 01011
FZH141/2.NAND32	Dual 5-input power NAND gate Both gates can be slowed down	2722 006 01021
FZH151/2.AOR30	Dual 5-input AND-AND-OR gate One gate can be slowed down	2722 006 02001
FZH161/4.LI31	Quad logic interface gate HNIL to 5 V logic; all gates can be slowed down	2722 006 04011
FZH171/2.NAND33	Dual 4-input NAND gate With expandable inputs; both gates can be slowed down	2722 006 01091

SURVEY OF TYPES (continued)

type	description	catalogue number
FZH181/4.LI30	Quad logic interface gate 5 V logic to HNIL	2722 006 04001
FZH191/3.NAND33	Triple 3-input NAND gate Two gates can be slowed down	2722 006 01031
FZH201/6.IN30	Sextuple inverter with strobe input	2722 006 07001
FZH211/4.NAND34	Quad 2-input NAND gate Two gates can be slowed down, outputs have open collectors	2722 006 01041
FZH231/2.NAND35	Dual 5-input NAND gate Both outputs can be slowed down, outputs have open collectors	2722 006 01051
FZH241/2.AST30	Dual 4-input NAND Schmitt trigger with expandable inputs; output can be slowed down	2722 006 12001
FZH251/4.AND30	Quad 2-input AND gate Two gates can be slowed down	2722 006 13001
FZH261/2.N-4.I30	Dual NAND gate/quad inverter	2722 006 08001
FZH271/4.EO30	Quad EXCLUSIVE-OR gate Two gates can be slowed down	2722 006 11001
FZH281/4.NOR30	Quad NOR gate Two gates can be slowed down	2722 006 10001
FZH291/4.OR30	Quad OR gate Two gates can be slowed down	2722 006 09001
FZJ101/FF30	Single JK flip-flop Slave can be slowed down	2722 006 00001
FZJ111/FF31	Single JK flip-flop Master and slave can be slowed down	2722 006 00011
FZJ121/2.FF32	Dual JK master-slave flip- flop	2722 006 00021
FZJ131/4.FF33	Quad D-type latch flip-flop	2722 006 00031

SURVEY OF TYPES (continued)

type	description	catalogue number
FZJ141/FF34	Single synchronous decimal counter Has parallel-set and common reset inputs	2722 006 00041
FZJ151/FF35	Single synchronous 4-bit binary counter. Has parallel-set and common reset inputs	2722 006 00051
FZJ161/FF36	Single synchronous 4-bit shift register. Two gates can be slowed down	2722 006 00061
FZK101/OS30	Single monostable multivibrator Input can be slowed down	2722 006 03001
FZL101/ND30	Single BCD-decimal decoder numerical indicator tube driver	2722 006 06021
FZL111/SD30	BCD 7-segment decoder-driver with open collector outputs	2722 006 14001
FZL121/PA31	Short-circuit-proof power stage with open collector output	2722 032 00121
FZL131/PA32	Short-circuit-proof power stage with open collector output	2722 032 00131
FZL141/PA33	Short-circuit-proof power driver for transistor stages	2722 032 00141
2.LRD30	Dual lamp/relay driver Can be slowed down	2722 006 06011
PA30	Power amplifier Can be slowed down	2722 032 00091
TU30	Single timer unit	2722 006 05001

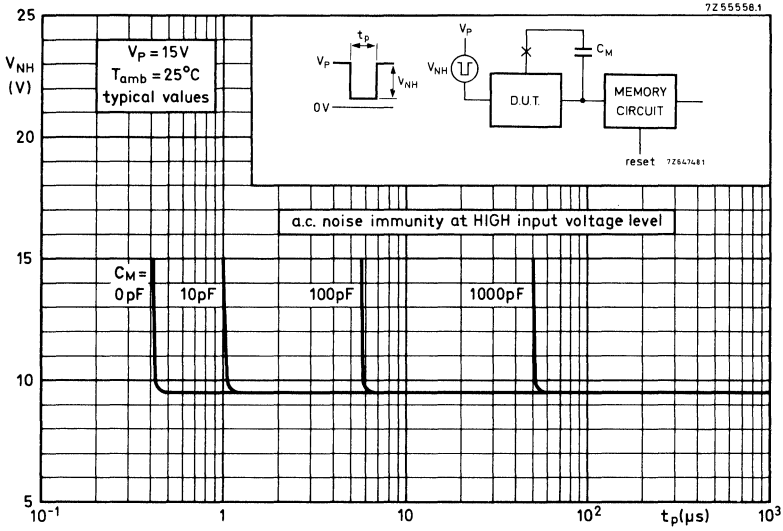
MAIN CHARACTERISTICS

Operating ambient temperature (range I)			0 to +70	°C	
Storage temperature			−65 to +150	°C	
Package outline			dual in-line		
Supply voltage : range I			12 $^{+12\frac{1}{2}\%}_{-5\%}$	V	1)
range II			15 $^{+13\%}_{-10\%}$	V	1)
Power consumption (per gate)	typ.		30	mW	
(per flip-flop)	typ.		165	mW	
Counting rate (flip-flops) can be slowed down	<		500	kHz	
Fan-out (in gate loads) : NAND gates and flip-flops	N_{aL}		10		
POWER-NAND gates	N_{aL}		30		
for all units	N_{aH}		100		
Propagation delay : (gates)	typ.		150	ns	2)
(flip-flops)	typ.		430	ns	2)
Output short circuit duration non-repetitive value	$t_{Q_{sc}}$	max.	1	s	3)
D.C. noise margin	typ.		5	V	
A.C. noise threshold (With an external capacitor the response time of a function can be slowed down, resulting in an increased a.c. noise threshold.)			see curves next page		

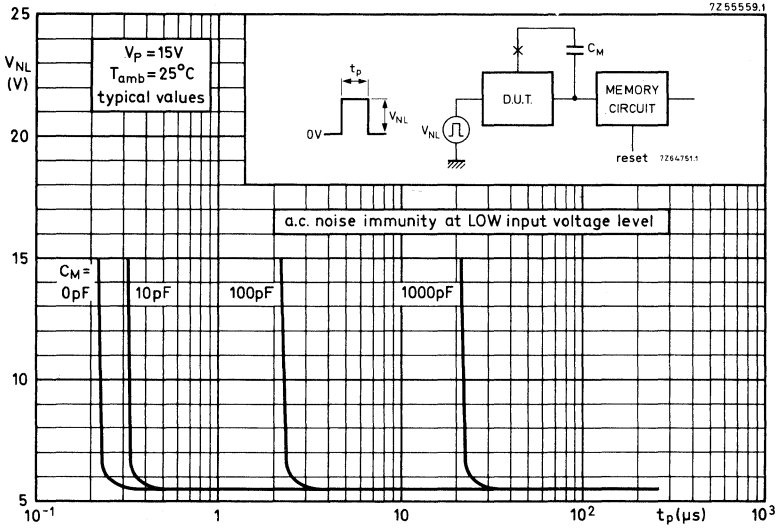
1) Voltage steps within the specified supply limits are allowed.

2) Can be increased to raise a.c. noise threshold.

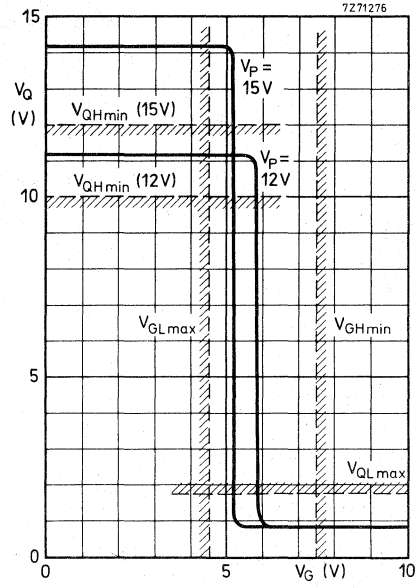
3) Only one output may be shorted at a time.

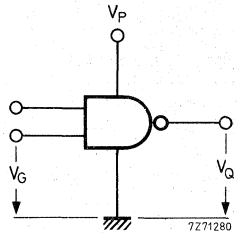


Typical curves for HIGH-input voltage level.

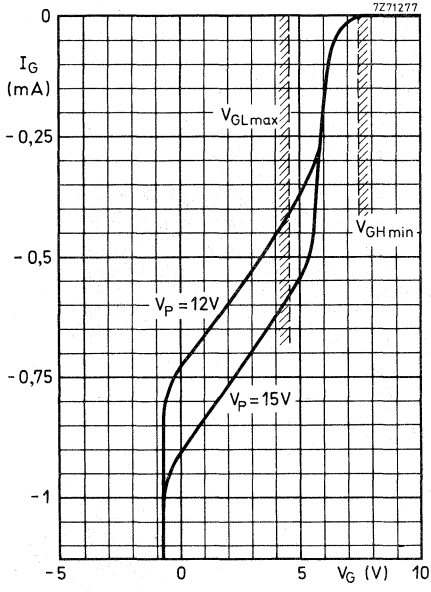


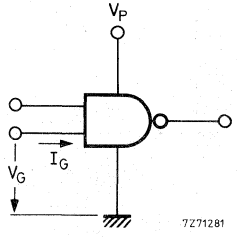
Typical curves for LOW-input voltage level.



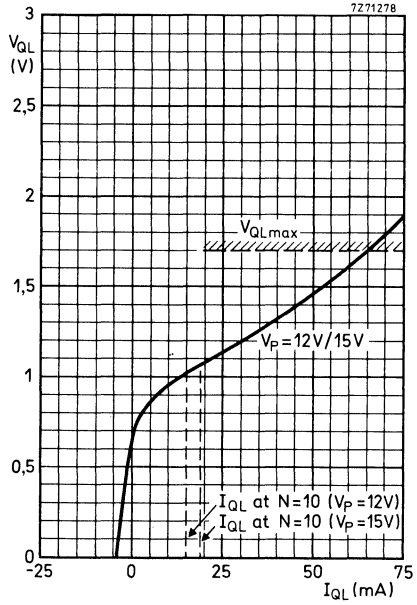


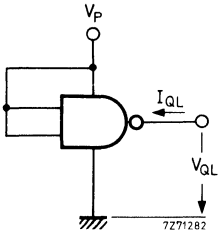
Typical transfer function of NAND gates at V_P = 12 V and V_P = 15 V.



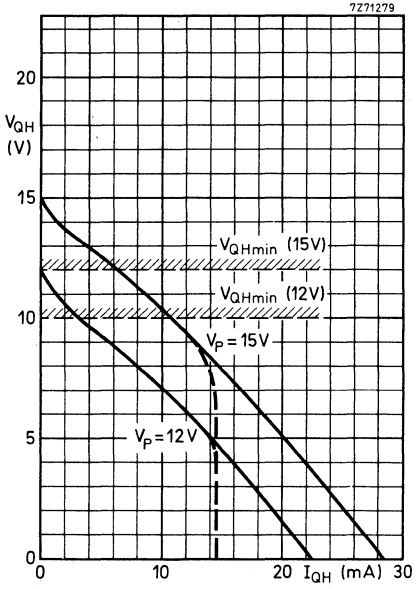


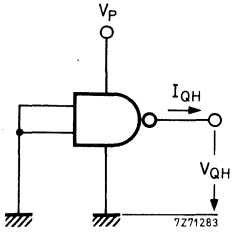
Typical input characteristic of NAND gates.





Typical output characteristic of the LOW-state outputs at V_P = 12 V, 15 V.





Typical output characteristic of the HIGH-state
—— FZH101 to FZH171, FZJ101 and FZJ111
---- FZH191 to FZH291, FZJ121 to FZJ161, and FZK101.

LOADING TABLE (T_{amb} = 0 to +70 °C; V_P = 15 V)

type	function	input (D.U.)		output (D.U.)	
		terminal	required	terminal	available
FZH101/4. NAND32	Quad 2-input NAND	G_1 - G_8	1	Q_1 - Q_4	10
FZH111/4. NAND30	Quad 2-input NAND	G_1 - G_8	1	Q_1 - Q_4	10
FZH121/2. NAND30	Dual 5-input NAND	G_1 - G_{10}	1	Q_1 ; Q_2	10
FZH131/2. NAND31	Dual 5-input NAND	G_1 - G_{10}	1	Q_1 ; Q_2	10
FZH141/2. NAND32	Dual 5-input power NAND	G_1 - G_{10}	1	Q_1 ; Q_2	30
FZH151/2. AOR30	Dual AND-AND-OR	G_2, G_3, G_9, G_{10} other gates	1, 5 1	Q_1 ; Q_2	16
FZH161/4. LI31	Quad logic interface HNIL to 5 V logic	G_2 - G_5 G_1, G_6	1 2	Q_1 - Q_4	$V_{QL} \leq 0,4$ V I_{QL} = 20 mA V_P = 13,5 V
FZH171/2. NAND33	Dual 4-input NAND	G_1 - G_8	1	Q_1 ; Q_2	10
FZH181/4. LI30	Quad logic interface 5 V to HNIL	G_1 - G_8	1	Q_1 - Q_4	27
FZH191/3. NAND33	Triple 3-input NAND	G_1 - G_9	1	Q_1 - Q_3	10
FZH201/6. IN30	Sextuple inverter with strobe input	G_1 - G_6	1	Q_1 - Q_6	10
FZH211/4. NAND34	Quad 2-input NAND	G_1 - G_8	1	Q_1 - Q_4	10
FZH231/2. NAND35	Dual 5-input NAND	G_1 - G_{10}	1	Q_1 ; Q_2	10
FZH241/2. AST30	Dual 4-input NAND Schmitt trigger	G_1 - G_8	1	Q_1 ; Q_2	10
FZH251/4. AND30	Quad 2-input AND	G_1 - G_8	1	Q_1 - Q_4	10
FZH261/2. N-4. I30	Dual NAND/Quad inverter	G_1 - G_8	1	Q_1 - Q_6	10
FZH271/4. EO30	Quad EXCLUSIVE-OR	G_1 - G_8	1	Q_1 - Q_4	10

LOADING TABLE (continued)

type	function	input (D.U.)		output (D.U.)	
		terminal	required	terminal	available
FZH281/4.NOR30	Quad NOR	G_1-G_8	1	Q_1-Q_4	10
FZH291/4.OR30	Quad OR	G_1-G_8	1	Q_1-Q_4	10
FZJ101/FF30	Single JK master-slave flip-flop	J_1;J_2;K_1;K_2	1	Q_1;Q_2	10
		T	2		
		S_1;S_2	1,5		
FZJ111/FF31	Single JK master-slave flip-flop	J_1;J_2;K	1	Q_1;Q_2	10
		T	2		
		S_1;S_2	1,5		
FZJ121/2.FF32	Dual JK master-slave flip-flop	J_1;J_2;K_1;K_2	1	Q_1-Q_4	10
		T_1;T_2	2		
		S_1-S_4	1,5		
FZJ131/4.FF33	Quad D-type latch flip-flop	D_1-D_4	2	Q_1-Q_8	10
		T_1;T_2	4		
FZJ141/FF34	Single synchronous decimal counter	all inputs	1	Q_A;Q_B;Q_C;Q_D	10
FZJ151/FF35	Single synchronous 4-bit binary counter	all inputs	1	Q_A;Q_B;Q_C;Q_D	10
FZJ161/FF36	Single synchronous 4-bit shift register	C_S input	4	Q_A;Q_B;Q_C;Q_D	10
		all other inputs	1		
FZK101/OS30	Monostable multivibrator	G_1-G_4	1	Q	10
FZL101/ND30	Single BCD-decimal decoder N.I.T. driver	I_1;I_2;I_4;I_8	1	Q_0-Q_9	I_{QH} = 50 mA, V_{QH} = 70 V: input comb. 0 to 9 I_{QH} = 5 mA, V_{QH} = 60 V: input comb. 10 to 15

LOADING TABLE (continued)

type	function	input (D.U.)		output (D.U.)	
		terminal	required	terminal	available
2. LRD30	Dual lamp/relay driver	G_1;G_2 E_1;E_2	3 3 (max 15 Si-diodes)	Q_1;Q_2	$I_{QL} \leq 200$ mA $V_{Pmax} = 17$ V
PA30	Power amplifier	G	$I_{GL} = 5,1$ mA; $V_{GL} = 1,7$ V	Q	$I_{QL} = 2$ A $V_{QL} = 1,3$ V
TU	Timer unit	G	$I_{GL} = 0,95$ mA; V_{GL}= 1,7 V $V_P = 11,4$ V $I_{GL} = 1,6$ mA; V_{GL}= 1,7 V $V_P = 17$ V	Q	22

NOTE

The figures quoted above for the fan-out in Drive Units (D.U.) are calculated for worst-case conditions: input Drive Units are simply added together to find the output Drive Units that the driving stage should be capable of supplying. To interface with other sorts of circuit, Drive Units can be interpreted as having the values shown below. These values are not applicable to the table.

LOW level:

1 input D.U. : 1,8 mA at 0 to 1,7 V
1 output D.U. : 1,5 mA at 1,7 V

HIGH level:

input voltage = between 10 V and V_P
output voltage = between 0,75 x V_P and V_P

LETTER SYMBOLS

1. General

The voltages and currents are related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a letter relating to the function of the device or the function of the pertinent signal.
In order to avoid confusion by any ambiguity in logical conventions, signal levels are indicated by H (= HIGH, for the more positive potential) and L (= LOW, for the less positive potential). Where circuit functions or logical equations are involved, the logical convention is mentioned specifically (for positive logic: H = 1, and for negative logic: H = 0).

2. Terminal designations

CE = condition enable for output QE
C_Q = slow-down terminal
CT = condition enable trigger at input T
D = D input of D-type latch flip-flops
E = expander input (if necessary, this letter may be followed by a subscript, e.g. E_1 or E_2 or by one of the input letters, such as EG = gate expander input)
G = gate input
J, K = J, K input of JK flip-flops
N = negative supply
P = positive supply
Q = output
QE = output enable
R = direct Reset input
S = direct Set input
T = trigger (or toggle) input
ϕ = common supply return and voltage reference

3. Subscript sequence for voltages and currents

First subscript : terminal designation letter.
Second subscript : H (for HIGH) or L (for LOW), if applicable.
Third subscript : min or max, if applicable.
Examples : V_P, I_{QL}, V_{QHmin}, I_{PH} (in the latter case H denotes that the output level is HIGH).

4. Polarity of current and voltage

A current is defined as positive when its conventional direction of flow is into the device.
Unless otherwise specified, a voltage is measured with respect to the reference terminal (ϕ). Its polarity is defined as positive when the potential is higher than that of the reference terminal.

5. Time designations

If required for reasons of unambiguity, the related terminals may be included in the designations given below (e.g. t_{fQ1}).

t_f = fall time (transition from HIGH to LOW, see Fig. 1)

t_{hold} = hold time

t_H = signal HIGH duration (Fig. 1)

t_L = signal LOW duration (Fig. 1)

t_{pd} = average propagation delay time, defined as $\frac{t_{pdr} + t_{pdf}}{2}$

t_{pdf} = fall propagation delay time (output voltage falling, see Fig. 2)

t_{pdr} = rise propagation delay time (output voltage rising, see Fig. 2)

t_r = rise time (transition from LOW to HIGH, see Fig. 1)

t_{rec} = recovery time

t_{sc} = duration of short circuit (from relevant terminal to common return terminal)

t_{su} = set-up time

V_{pd} = reference voltage level for propagation delay measurement

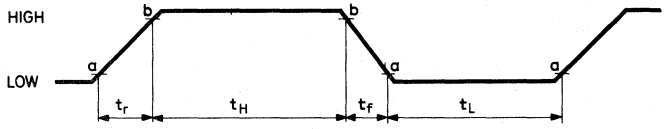


Fig. 1

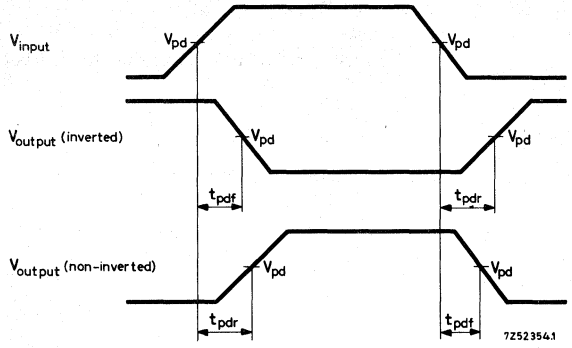


Fig. 2

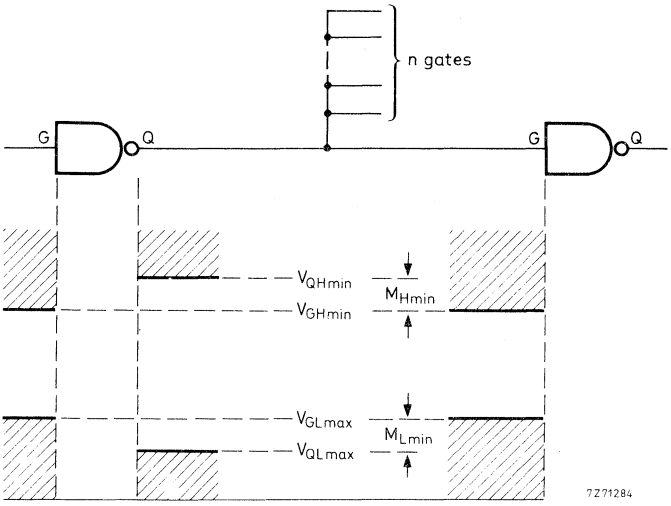
6. Other designations

i.c. = internally connected
Terminals with this indication should be left open. Otherwise correct working cannot be ensured; the device may even be damaged

I_P = supply current
The logic state of the device indicated by H of L is normally referred to the output level, unless otherwise specified

I_{Pmax} = supply current
Maximum d.c. value under defined conditions

M = d.c. noise margin



M_L = d.c. noise margin, signal level LOW
(defined as: $M_L = V_{GLmax} - V_{QLmax}$ under defined loading, temperature and supply voltage conditions)

M_H = d.c. noise margin, signal level HIGH
(calculated from: $M_H = V_{QHmin} - V_{GHmin}$ under defined loading, temperature and supply voltage conditions)

Na_L = available d.c. fan-out (defined as: $N_{aL} = \frac{I_{QLmax}}{-I_{GLmax}}$ under defined temperature and supply voltage conditions)

N_{aH} = available d.c. fan-out (defined as: $N_{aH} = \frac{-I_{QHmax}}{I_{GHmax}}$ under defined temperature and supply voltage conditions)

P_H;P_L = power consumption, defined as the product of the supply current(s) and of the corresponding supply voltage(s). The logical state of the device, indicated by a letter subscript H or L, is normally referred to the output level, unless otherwise specified

P_{av} = average power consumption at 50% duty cycle, unless otherwise specified. It is defined as: $P_{av} = V_P \cdot \frac{I_{PH} + I_{PL}}{2}$

P_{tot} = power dissipation, defined as the total power dissipated by the device. It is the sum of the products of all currents and voltages at each of the input, output and supply terminals, their polarities being taken into account. The logical state of the device indicated by a letter subscript H or L is normally referred to the output level, unless otherwise specified

T_{amb} = operating ambient temperature, i.e. the temperature of the free air in which the normally operating device is placed without external heat conduction, unless otherwise specified

T_{stg} = storage temperature, i.e. the temperature of the ambient medium in which the non-operating device is stored

V_{GLmax} = input voltage LOW at terminal G. With the specified level applied to the input of an inverting gate the output level will not be lower than the specified value V_{QHmin} at given I_{QH}.

V_{GHmin} = input voltage HIGH at terminal G. With the specified level applied to the input of an inverting gate the output level will not exceed the specified value V_{QLmax} at given I_{QL}.

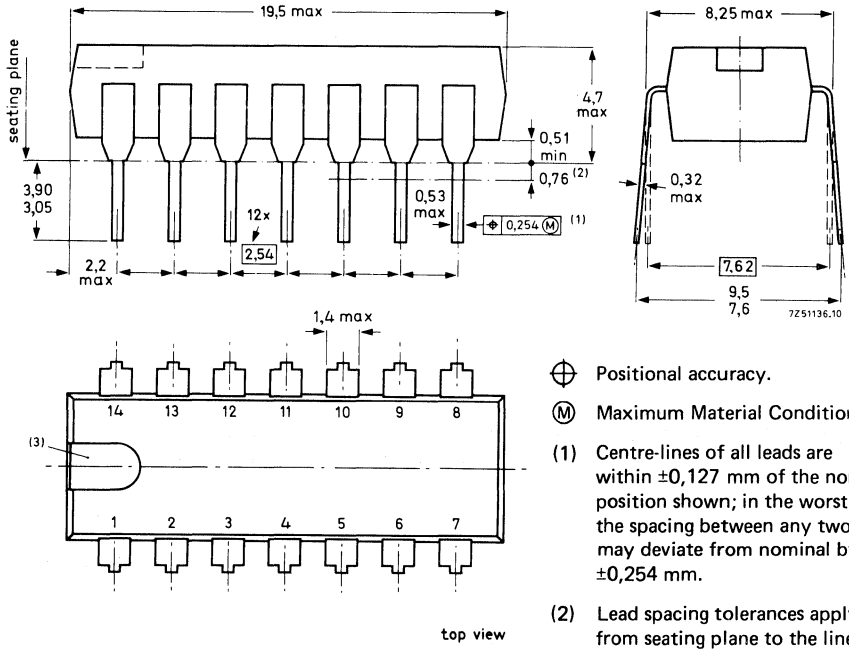
V_H = hysteresis ($V_H = V_{TP} - V_{TN}$)

V_{TP} = positive-going threshold voltage

V_{TN} = negative-going threshold voltage

ΔV_Q = change of output voltage caused by a specified change of output current

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27S, T, V)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

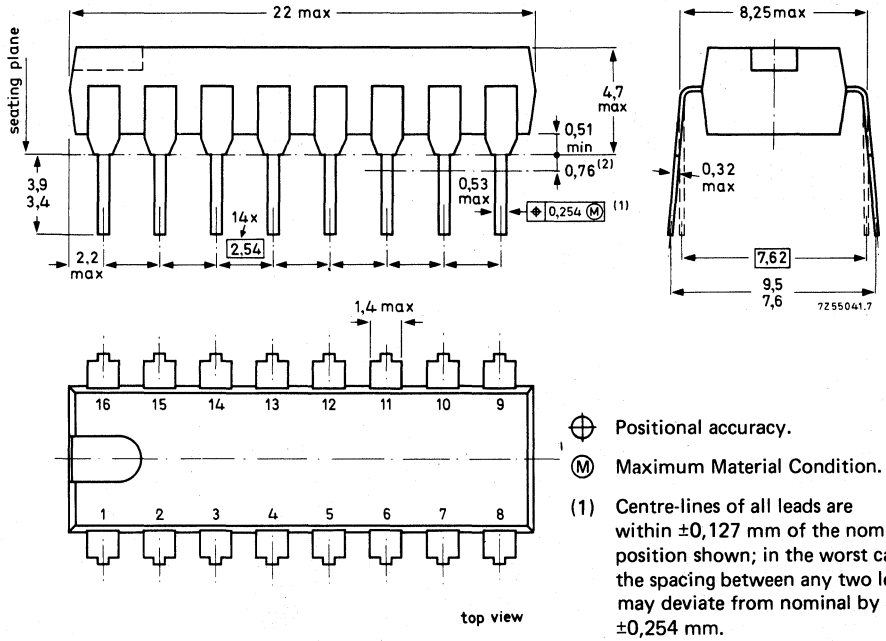
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

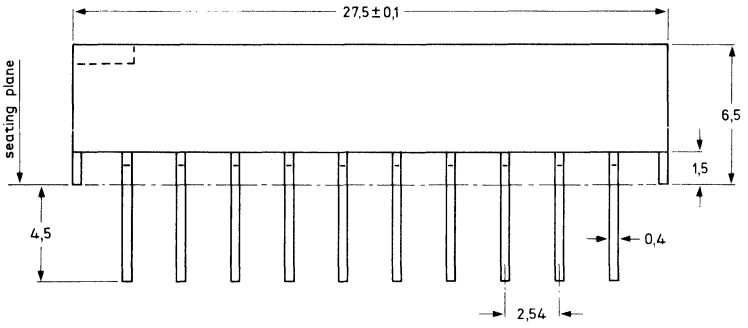
2. By dip or wave

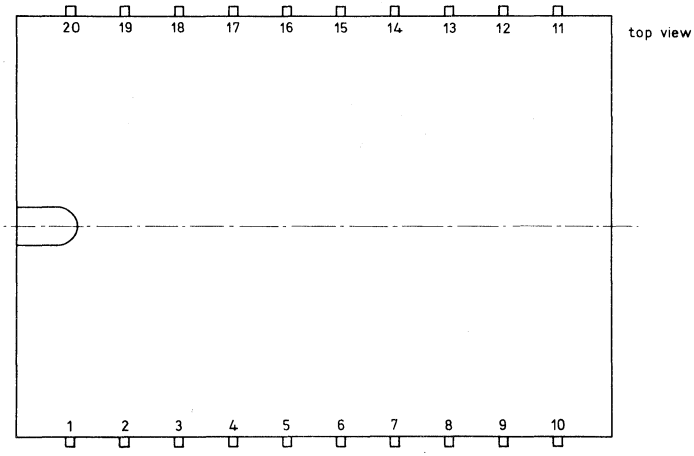
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

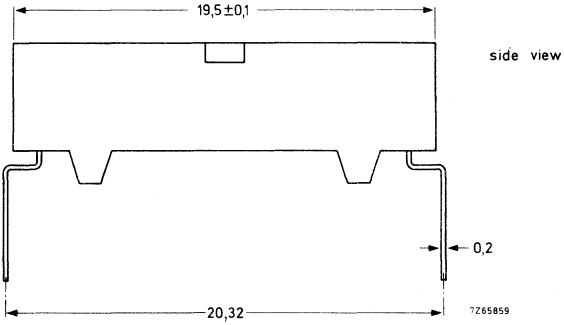
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

20 LEAD DUAL IN-LINE

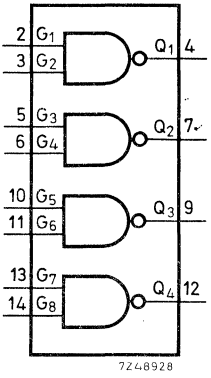




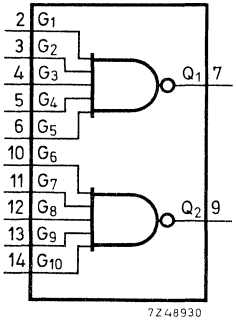


The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

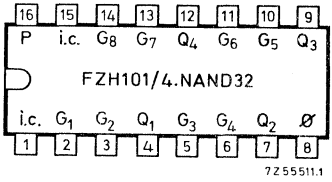
QUADRUPLE 2-INPUT NAND GATE
DUAL 5-INPUT NAND GATE

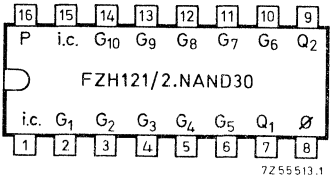


FZH101/4.NAND32



FZH121/2.NAND30





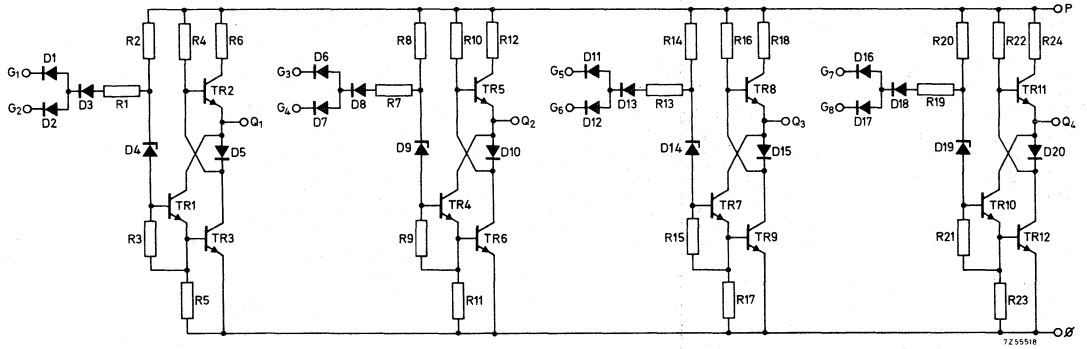
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

The FZH101/4.NAND32 and FZH121/2.NAND30 consists of a number of independent NAND gates without slow-down capability.

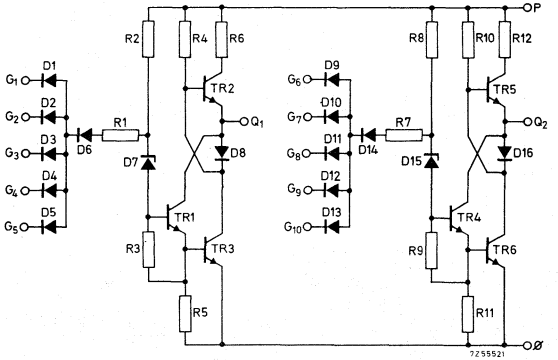
PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAMS

FZH101/4.NAND32



FZH121/2.NAND30



August 1975

QUADRUPLE 2-INPUT NAND GATE
DUAL 5-INPUT NAND GATE

2722 006 01081
2722 006 01061

LOGIC FUNCTION

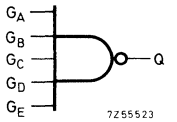
FZH101/4.NAND32

$Q = \overline{G_A \cdot G_B}$ (positive logic)

Function tables

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

FZH121/2.NAND30



$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$

(positive logic)

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature		T_{amb}	0 to	+70	°C
Uniform system supply voltage (range I)		V_P	11,4 to	13,5	V
(range II)		V_P	13,5 to	17	V
Available d.c. fan-out		N_{aL}	max.	10	
		N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	2,5	V
range II at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	4,5	V
Supply current per gate	range I ; output HIGH	I_{Pav}	typ.	0,9	mA
	output LOW	I_{Pav}	typ.	1,7	mA
	range II; output HIGH	I_{Pav}	typ.	1,2	mA
	output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}		P_{tot}	max.	31	mW
at range II; V_{Pmax}		P_{tot}	max.	52	mW
Thermal resistance from system to ambient		R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leqslant 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geqslant 10$ V; $-I_{QH}$ = 15 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited[2]	$-I_{Qsc}$	10	30	50 mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	0,9	1,6 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay:						
fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2] Short-circuit duration max. 1 s.

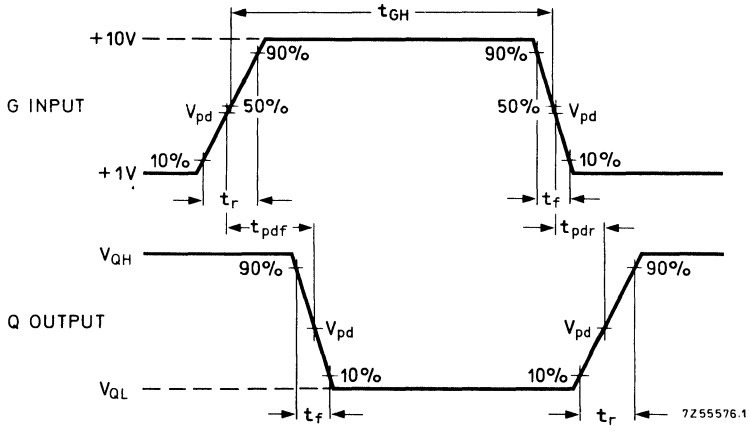
CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	$-I_{QL}$	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited[2]	$-I_{Qsc}$	15	37	60	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	1,2	2,1	mA	17	V_G = 0 V
at V_{QL}	I_P	–	2,3	4,0	mA	17	V_G = 17 V
Dynamic data							
Times							
Propagation delay:							
fall time	t_{pdf}	–	140	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	195	–	ns	15	
output rise time	t_r	–	410	–	ns	15	
output fall time	t_f	–	75	–	ns	15	

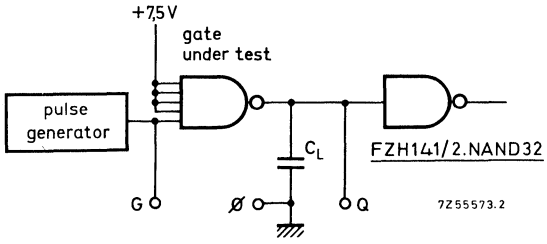
[1]) All typical values under test conditions : T_{amb} = 25 °C and V_P = 15 V.
[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = + 4,5 V
t_f = 120 ns
t_{GH} = 1 µs

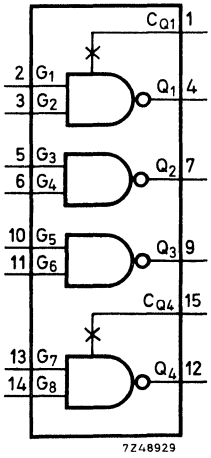


Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

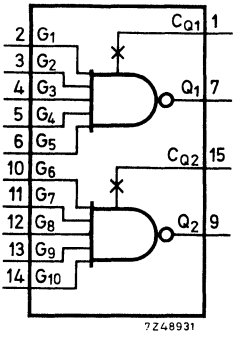
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

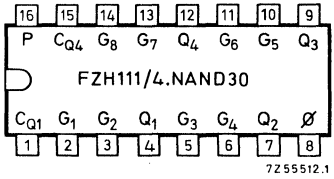
QUADRUPLE 2-INPUT NAND GATE
DUAL 5-INPUT NAND GATE
both having slow-down capability

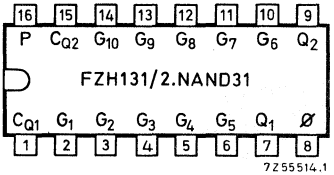


FZH111/4.NAND30



FZH131/2.NAND31





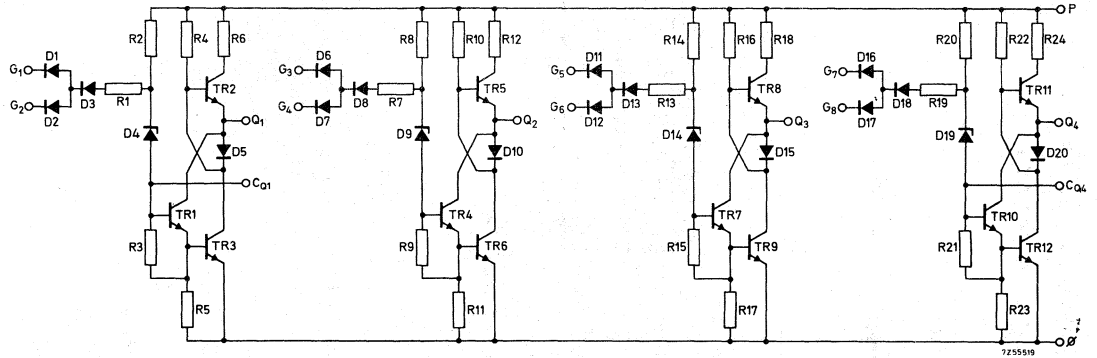
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I ; $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II; $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C				
(50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

The FZH111/4.NAND30 and FZH131/2.NAND31 consist of a number of independent NAND gates at which two NAND gates per type have a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

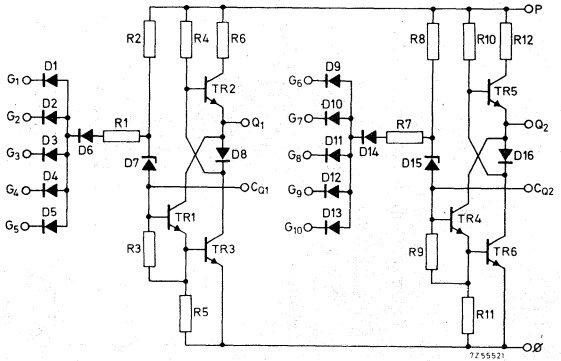
PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAMS

FZH111/4.NAND30



FZH131/2.NAND31



2722 006 01001
2722 006 01011

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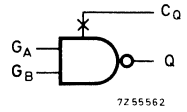
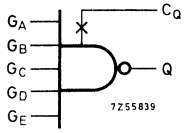
LOGIC FUNCTION

FZH111/4.NAND30



$Q = \overline{G_A \cdot G_B}$ (positive logic)

FZH131/2.NAND31



$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$
(positive logic)

Function tables

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to 17		V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I ; output HIGH	I_{Pav}	typ.	0,9	mA
output LOW	I_{Pav}	typ.	1,7	mA
range II; output HIGH	I_{Pav}	typ.	1,2	mA
output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	31	mW
at range II ; V_{Pmax}	P_{tot}	max.	52	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leqslant 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geqslant 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 μA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited[2]	$-I_{Qsc}$	10	30	50 mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	0,9	1,6 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay						
fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) Short-circuit duration max. 1 s.

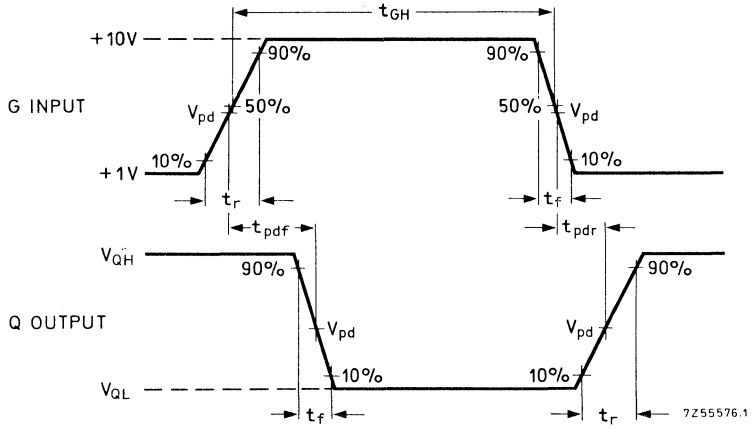
CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	13,5	$V_{QL} \leqslant 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5 V	13,5 and 17	$V_{QH} \geqslant 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	– V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7 V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	– V	13,5	
LOW	M_L	2,8	5,0	– V	13,5	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 μA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8 mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	– mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	15	37	60 mA	17	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	1,2	2,1 mA	17	V_G = 0 V
at V_{QL}	I_P	–	2,3	4,0 mA	17	V_G = 17 V
Dynamic data						
Times						
Propagation delay						
fall time	t_{pdf}	–	140	– ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{dp} = 4,5 V
rise time	t_{pdr}	–	195	– ns	15	
output rise time	t_r	–	410	– ns	15	
output fall time	t_f	–	75	– ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
[2] Short-circuit duration max. 1 s.

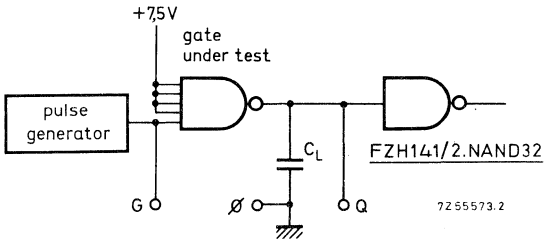
CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns
t_f = 120 ns
t_{GH} = 1 µs

V_{pd} = + 4,5 V



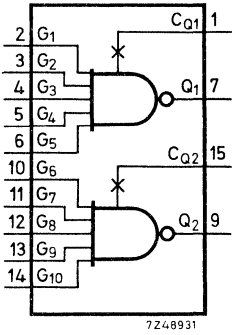
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

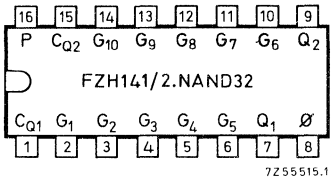
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL 5-INPUT POWER NAND GATE

with slow-down capability



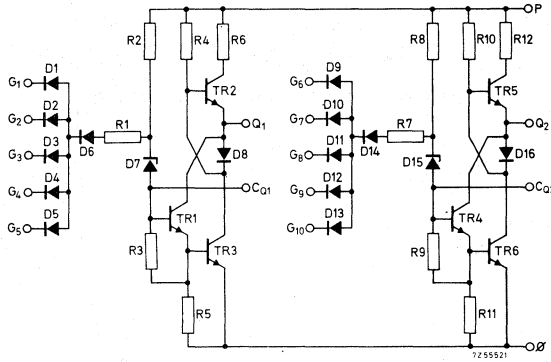


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state	N_{aL}	max.	30	
D.C. noise margin at $T_{amb} = 25$ °C range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

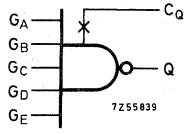
The FZH141/2.NAND32 is a dual 5-input power NAND gate with on each gate a special base connection (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$$
(positive logic)

Function table

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	-65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	°C	
Uniform system supply voltage (range I)	V_P	11,4 to 13,5	V	
(range II)	V_P	13,5 to 17	V	
Available d.c. fan-out	N_{aL}	max.	30	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I; output HIGH	I_{Pav}	typ.	0,9	mA
output LOW	I_{Pav}	typ.	1,7	mA
range II; output HIGH	I_{Pav}	typ.	1,2	mA
output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	31	mW
at range II ; V_{Pmax}	P_{tot}	max.	52	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 45 mA
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	-	1,3	1,7	V	11,4	V_{GH} = 7,5 V; I_{QL} = 45 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4	
LOW	M_L	2,8	5,0	-	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	-	-	1,0	µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	45	-	-	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	10	30	50	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	-	0,9	1,6	mA	13,5	V_G = 0 V
at V_{QL}	I_P	-	1,7	3,0	mA	13,5	V_G = 13,5 V
Dynamic data							
Times							
Propagation delay fall time	t_{pdf}	90	175	310	ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310	ns	12	
output rise rime	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) Short-circuit duration max. 1 s.

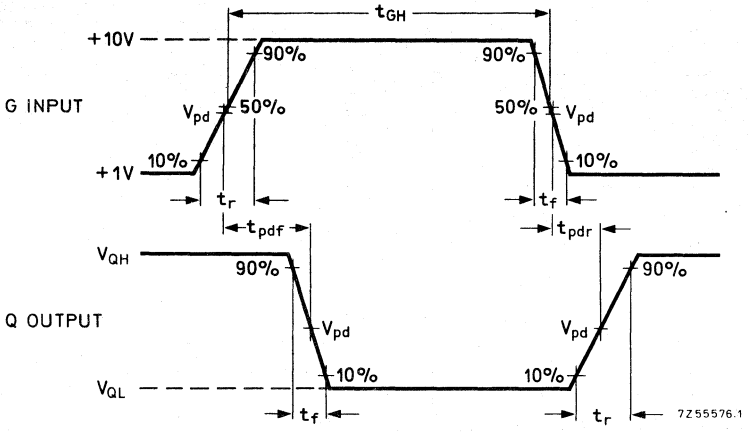
CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references: Vp (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	-	- V	13,5	$V_{QL} \leqslant 1,7$ V; I_{QL} = 54 mA
Input LOW	V_{GL}	-	-	4,5 V	13,5 and 17	$V_{QH} \geqslant 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	- V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	-	1,4	1,7 V	13,5	V_{GH} = 7,5 V; I_{QL} = 54 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	- V	13,5	
LOW	M_L	2,8	5,0	- V	13,5	
Currents (per gate)						
Input HIGH	I_{GH}	-	-	1,0 µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	-	-	1,8 mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	-	- mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	54	-	- mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	15	37	60 mA	17	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	-	1,2	2,1 mA	17	V_G = 0 V
at V_{QL}	I_P	-	2,3	4,0 mA	17	V_G = 17 V
Dynamic data						
Times						
Propagation delay fall time	t_{pdf}	-	140	- ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; Vdp = 4,5 V
rise time	t_{pdr}	-	195	- ns	15	
output rise time	t_r	-	410	- ns	15	
output fall time	t_f	-	75	- ns	15	

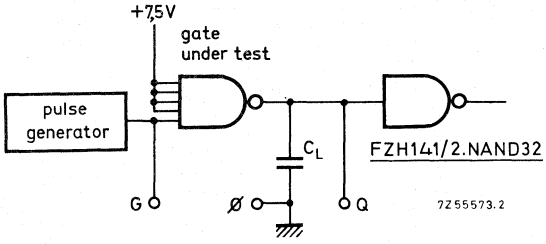
[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs

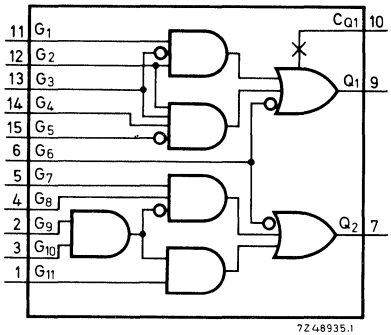


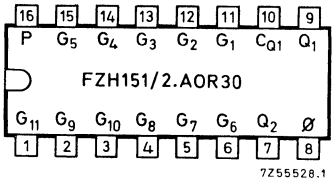
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL AND-AND-OR GATE
with slow-down capability





QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	380	ns
Available d.c. fan-out ($T_{amb} = 0$ to +70 °C) LOW state	N_{aL}	max.	20	1)
	N_{aL}	max.	16	2)
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	132	mW
range II: $V_P = 15$ V	P_{av}	typ.	225	mW

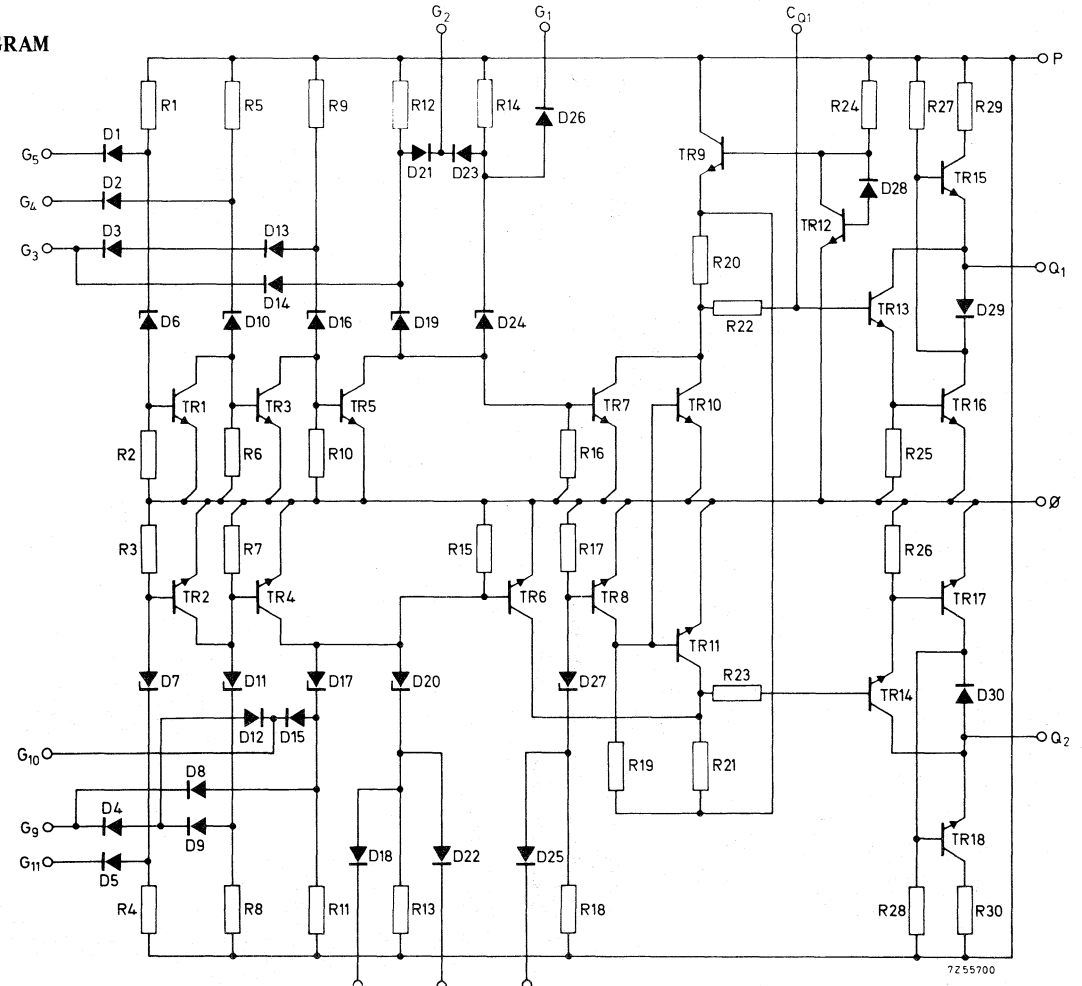
1) At FZH151/2.AOR30 load.
2) At HNIL gate load.

G_2, G_3, G_9 and G_{10} count for two inputs.

The FZH151/2.AOR30 consists of two combinations AND and OR gates with some common inputs to the AND gates and a common override input to the OR gates. One of the OR gates has a special terminal (C_{Q1}) to provide slow-down capability.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q_1 = G_1 \cdot G_2 \cdot \overline{G_3} + G_2 \cdot G_3 \cdot G_4 \cdot \overline{G_5} + \overline{G_6}$

$Q_2 = G_7 \cdot G_8 \cdot \overline{G_9 \cdot G_{10}} + G_9 \cdot G_{10} \cdot G_{11} + \overline{G_6}$

} for positive logic

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature		T_{amb}	0 to	70	°C
Uniform system supply voltage (range I)		V_P	11,4 to	13,5	V
(range II)		V_P	13,5 to	17	V
Available d.c. fan-out: at FZH151/2.AOR30		N_{aL}	max.	20	*)
at HNIL gate load		N_{aL}	max.	16	
		N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	2,5	V
range II at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	4,5	V
Supply current per gate	range I ; output HIGH	I_{Pav}	typ.	14	mA
	output LOW	I_{Pav}	typ.	8,0	mA
	range II; output HIGH	I_{Pav}	typ.	18	mA
	output LOW	I_{Pav}	typ.	12	mA
Power consumption per gate (50% duty cycle) at range I, V_{Pmax}		P_{tot}	max.	250	mW
at range II, V_{Pmax}		P_{tot}	max.	425	mW
Thermal resistance from system to ambient		R_{th}	max.	150	°C/W

*) G_2, G_3, G_9 and G_{10} count for two inputs.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	V_{QL} = max 1,7 V; I_{QL} = 30 mA
Input LOW	V_{GL}	–	–	4,5	V	11,4	V_{QH} = min 10 V; $-I_{GH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{GH} = 7,5 V; I_{QL} = 30 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V		
LOW	M_L	2,8	5,0	–	V		
Currents							
Input HIGH: $G_2;G_3;G_9;G_{10}$	I_{GH}	–	–	2	μA	13,5	V_{GH} = 13,5 V; other inputs 0 V
at other G inputs	I_{GH}	–	–	1	μA		
Input LOW: $G_2;G_3;G_9;G_{10}$	$-I_{GL}$	–	1,0	2,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5V
at other G inputs	$-I_{GL}$	–	0,5	1,25	mA		
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	30	–	–	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	10	30	50	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents							
at V_{QH}	I_P	–	14,0	22,0	mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	8,0	15,0	mA	13,5	V_{G11} = V_{GL}; other G inputs: V_{GH}

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	V_{QL} = max. 1,7 V; I_{QL} = 36 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5	V_{QH} = min. 12 V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 36 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents							
Input HIGH: G_2;G_3;G_9;G_{10}	I_{GH}	–	–	2,0	μA	17	V_{GH} = 17 V; other inputs 0 V
at other G inputs	I_{GH}	–	–	1,0	μA		
Input LOW: G_2;G_3;G_9;G_{10}	$-I_{GL}$	–	1,2	3,0	mA	17	V_{GL} = 1,7 V; other inputs 17 V
at other G inputs	$-I_{GL}$	–	0,6	1,5	mA		
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	30	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	15	37	60	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents							
at V_{QH}	I_P	–	18	29	mA	17	V_G = 0 V
at V_{QL}	I_P	–	12	21	mA	17	V_{G11} = V_{GL}; other G inputs: V_{GH}

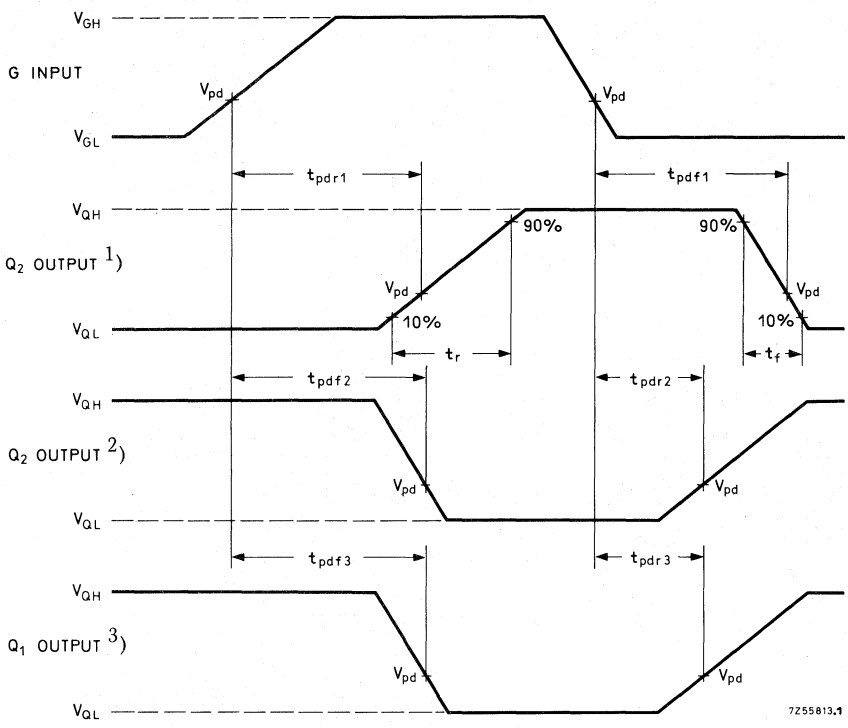
[1] All typical values under test condiotions: T_{amb} = 25 °C and V_P = 15 V.
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

	Symbol	min.	typ.[1]	max.		V_P (V)	Conditions and references
Dynamic data							
Times							
Propagation delay							
fall times at output Q	t_{pdf1}	–	230	–	ns	12	C_L = 10 pF N = 1 T_{amb} = 25 °C V_{pd} = 4,5 V
at output $\overline{Q}$	t_{pdf2}	–	300	–	ns	12	
at input G_5	t_{pdf3}	–	400	–	ns	12	
rise times at output Q	t_{pdr1}	–	340	–	ns	12	
at output $\overline{Q}$	t_{pdr2}	–	340	–	ns	12	
at input G_5	t_{pdr3}	–	270	–	ns	12	
Output rise time	t_r	–	330	–	ns	12	
Output fall time	t_f	–	200	–	ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)



Waveforms illustrating measurement of t_{pdr} and t_{pdf}

1) If G input = G_7, G_8, G_{11}.

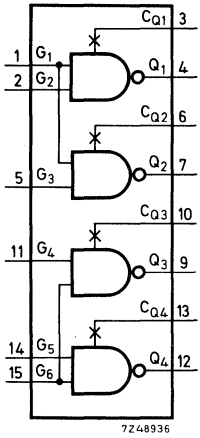
2) If G input = G_6.

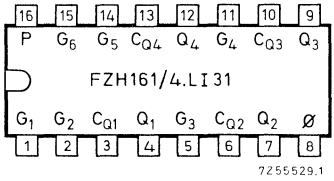
3) If G input = G_5.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE LOGIC INTERFACE GATE

HNIL to 5 V logic; with slow-down capability



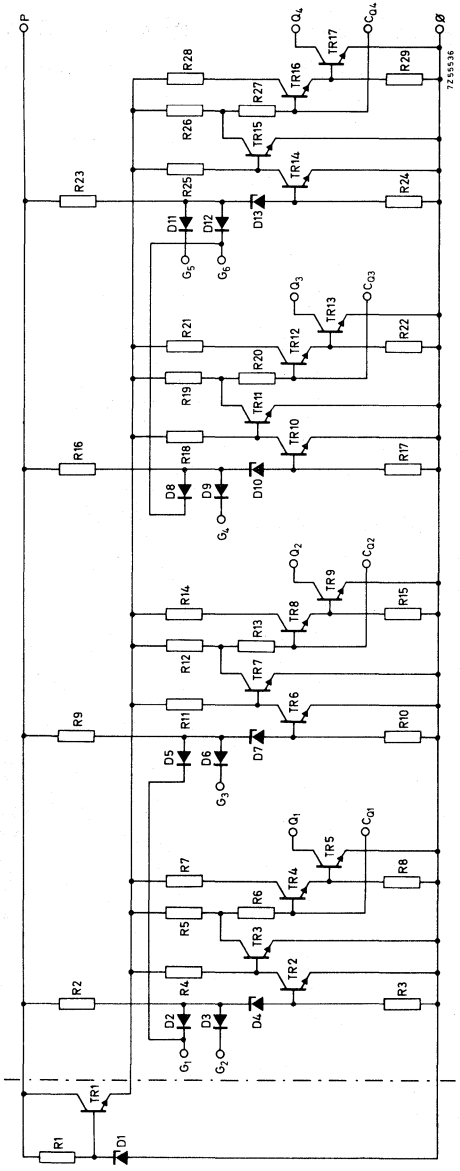


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay				
V_P = 12 V; N = 1; V_Q = 12 V	t_{pd1}	typ.	115	ns
V_{pd} = 4,5 V; T_{amb} = 25 °C; V_Q = 5 V	t_{pd2}	typ.	105	ns
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C (50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	39	mW
range II: V_P = 15 V	P_{av}	typ.	55	mW

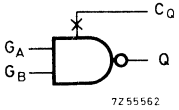
The FZH161/4. LI31 is a level converter with open-collector outputs for HNIL to TTL and consists of 4 gates and some common inputs.
Each gate has slow-down capability.

PACKAGE OUTLINE 16 leads plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = \overline{G_A \cdot G_B}$

(for positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage (HIGH state)	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA
Storage temperature	T_{stg}	-65 to +150		°C
Operating ambient temperature	T_{amb}	0 to + 70		°C

SYSTEM DESIGN DATA

Uniform system temperature		T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)		V_P		11,4 to 13,5	V
	(range II)	V_P		13,5 to 17	V
Available output current		I_{QL}	min.	20	mA
		I_{QH}	max.	50	µA
D.C. noise margin; range I at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	2,5	V
	range II at V_{Pmin}	M_L	min.	2,8	V
		M_H	min.	4,5	V
Supply current per gate	range I ; output HIGH	I_{Pav}	typ.	2,5	mA
	output LOW	I_{Pav}	typ.	4,0	mA
	range II; output HIGH	I_{Pav}	typ.	2,8	mA
	output LOW	I_{Pav}	typ.	4,5	mA
Power consumption per gate (50 % duty cycle) at range I ; V_{Pmax}		P_{tot}	max.	71	mW
	at range II; V_{Pmax}	P_{tot}	max.	98	mW
Average propagation delay					
at V_{pd1} = 4,5 V; (V_Q = 12 V)		t_{pd1}	max.	275	ns
at V_{pd2} = 1,5 V; (V_Q = 5 V)		t_{pd2}	max.	275	ns
Thermal resistance from system to ambient		R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C.

	Sym-bol	min.	typ. [1])	max.	Conditions and references: V_P (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	V_{QL} = 0,4 V; I_{QL} = 20 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4	V_{QH} = 13,5 V; I_{QH} = 40 µA
Output LOW	V_{QL}	–	–	0,4 V	11,4	V_{GH} = 7,5 V; I_{QL} = 20 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	11,4	
LOW	M_L	2,8	5,0	–	11,4	
Currents (per gate)						
Input HIGH; G_2; G_3; G_4; G_5	I_{GH}	–	–	1,0 µA	13,5	V_{GH} = 13,5 V; other inputs 0V
G_1; G_6	I_{GH}	–	–	2,0 µA		
Input LOW; G_2;G_3; G_4; G_5	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL}= 1,7 V; other inputs 13,5V
G_1; G_6	$-I_{GL}$	–	1,6	3,0 mA		
Output HIGH	I_{QH}	–	–	80 µA	11,4	V_{QH} = 13,5 V; V_{GH} = 4,5 V
Output LOW	I_{QL}	20	–	– mA	11,4	V_{QL} = 0,4 V; V_{GH} = 7,5 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	2,5	4,5 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	4,0	6,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay						
fall time: V_Q = 12 V	t_{pdf1}	80	130	300 ns		T_{amb} = 25 °C; C_L = 15 pF; R_L = 760 Ω at V_Q = 12 V; R_L = 320 Ω at V_Q = 5 V
V_Q = 5 V	t_{pdf2}	80	120	300 ns		
rise time: V_Q = 12 V	t_{pdr1}	80	250	500 ns		
V_Q = 5 V	t_{pdr2}	80	230	500 ns		

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
Static data							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	V_{QL} = 0,4 V; I_{QL} = 20 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5	V_{QH} = 17 V; I_{QH} = 40 µA
Output LOW	V_{QL}	–	–	0,4	V	13,5	V_{GH} = 7,5 V; I_{QL} = 20 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH: G_2;G_3;G_4;G_5	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
G_1;G_6	I_{GH}	–	–	2,0	µA		
Input LOW: G_2;G_3;G_4;G_5	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17V
G_1;G_6	$-I_{GL}$	–	2,0	3,6	mA		
Output HIGH	I_{QH}	–	–	80	µA	13,5	V_{QH} = 17 V; V_{GL} = 4,5 V
Output LOW	I_{QL}	20	–	–	mA	13,5	V_{QL} = 0,4 V; V_{GL} = 7,5 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	2,8	4,5	mA	17	V_G = 0 V
at V_{QL}	I_P	–	4,5	7,0	mA	17	V_G = 17 V

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Calculation of collector resistor R_Q

The collector resistor R_Q has to be calculated from voltages and input- and output currents of the gates.

$$R_{Qmax} = \frac{V_P - V_{QH} \quad (V)}{m \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)} \qquad R_{Qmin} = \frac{V_P - V_{QL} \quad (V)}{I_{QLmax} - N \cdot I_{GL} \quad (mA)}$$

m = number of interconnected outputs
N = number of used inputs
V_P = supply voltage of TTL-inputs
V_{QH} = output voltage HIGH of TTL-circuit
V_{QL} = output voltage LOW of TTL-circuit
I_{GH} = input current HIGH of TTL-circuit
I_{GL} = input current LOW of TTL-circuit

For interfacing HNIL to TTL:

$$R_{Qmax} = \frac{5 - 2,4 \quad (V)}{m \cdot 80 + N \cdot 80 \, (\mu A)} \qquad R_{Qmin} = \frac{5 - 0,4 \quad (V)}{20 - N \cdot 1,6 \quad (mA)}$$

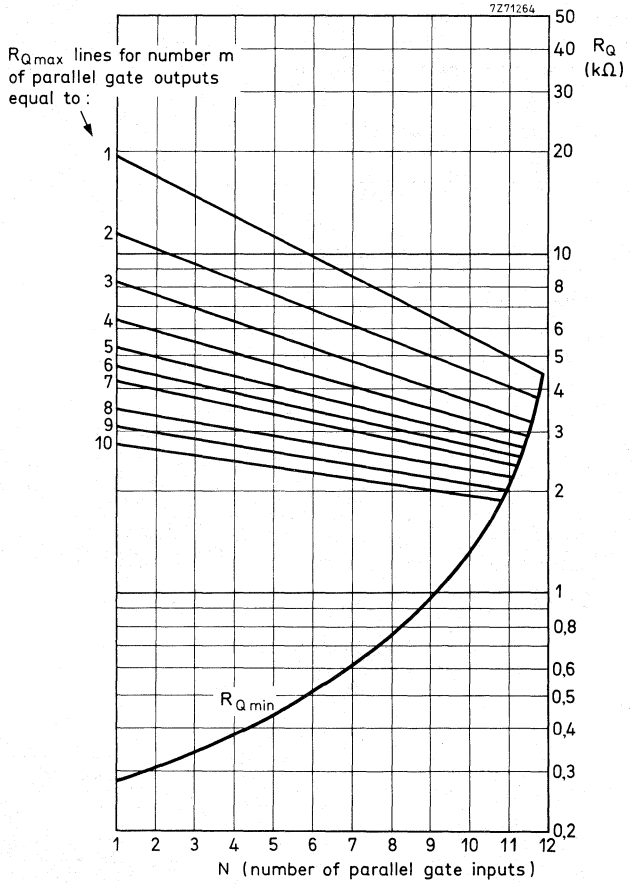
If FZH161/4. LI31 is used as wired-OR combination

for range I: $V_P = 12$ V

$$R_{Qmax} = \frac{12 - 10 \quad (V)}{m \cdot 80 + N \cdot 1 \, (\mu A)} \qquad R_{Qmin} = \frac{12 - 0,4 \quad (V)}{20 - N \cdot 1,5 \quad (mA)}$$

for range II: $V_P = 15$ V

$$R_{Qmax} = \frac{15 - 12 \quad (V)}{m \cdot 80 + N \cdot 1 \, (\mu A)} \qquad R_{Qmin} = \frac{15 - 0,4 \quad (V)}{20 - N \cdot 1,8 \quad (mA)}$$

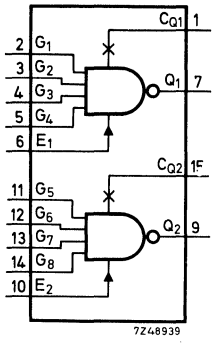


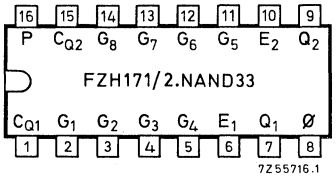
R_Q as a function of m and N loaded with TTL gates.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL 4-INPUT NAND GATE

with slow-down capability and expandable inputs



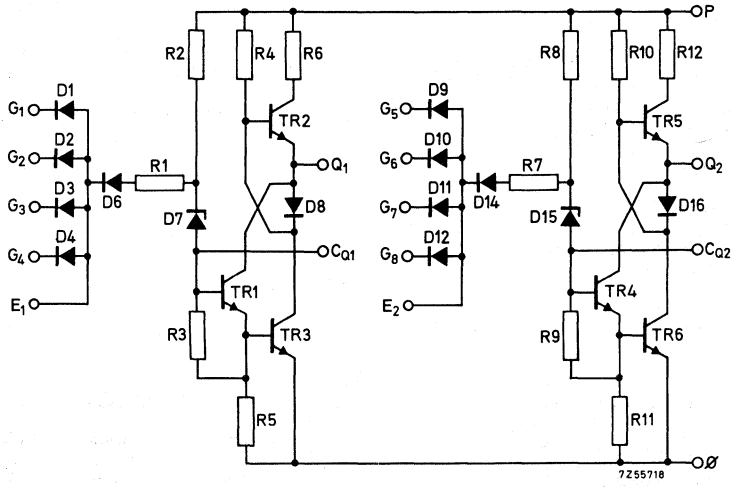


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to +70		°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

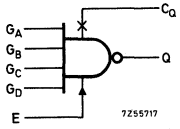
The FZH171/2.NAND33 consists of two independent NAND gates and each gate has a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.
Non-used expander inputs E_1 and E_2 must be left floating.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot E}\ ^{*})$$

(positive logic)

*) When provided with a diode

G_A	G_B	G_C	G_D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA
Expandable input voltage	V_E	min.	0	V
Expandable input current	$-I_E$	max.	25	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature		T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)		V_P	11,4 to 13,5		V
(range II)		V_P	13,5 to 17		V
Available d.c. fan-out		N_{aL}	max.	10	
		N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	2,5	V
range II at V_{Pmin}		M_L	min.	2,8	V
		M_H	min.	4,5	V
Supply current per gate	range I; output HIGH	I_{Pav}	typ.	0,9	mA
	output LOW	I_{Pav}	typ.	1,7	mA
	range II; output HIGH	I_{Pav}	typ.	1,2	mA
	output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax}		P_{tot}	max.	31	mW
at range II; V_{Pmax}		P_{tot}	max.	52	mW
Thermal resistance from system to ambient		R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1])	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2])	$-I_{Qsc}$	10	30	50	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	0,9	1,6	mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0	mA	13,5	V_G = 13,5 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) Short-circuit duration max. 1 s.

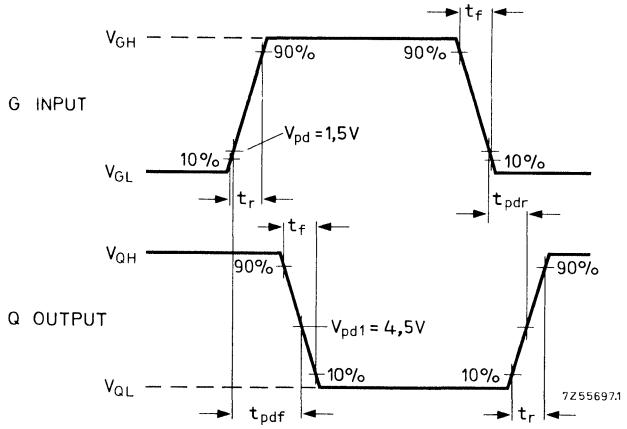
CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	15	37	60	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	1,2	2,1	mA	17	V_G = 0 V
at V_{QL}	I_P	–	2,3	4,0	mA	17	V_G = 17 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	–	140	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	195	–	ns	15	
output rise time	t_r	–	410	–	ns	15	
output fall time	t_f	–	75	–	ns	15	

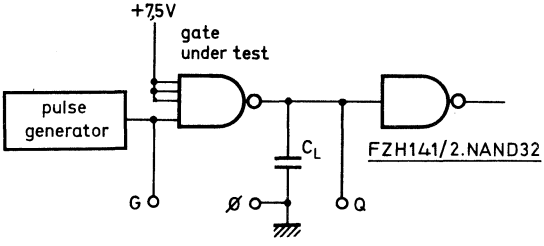
1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs



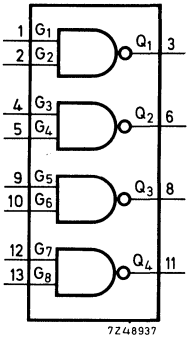
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

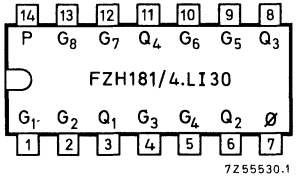
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE LOGIC INTERFACE GATE

5 V logic to HNIL



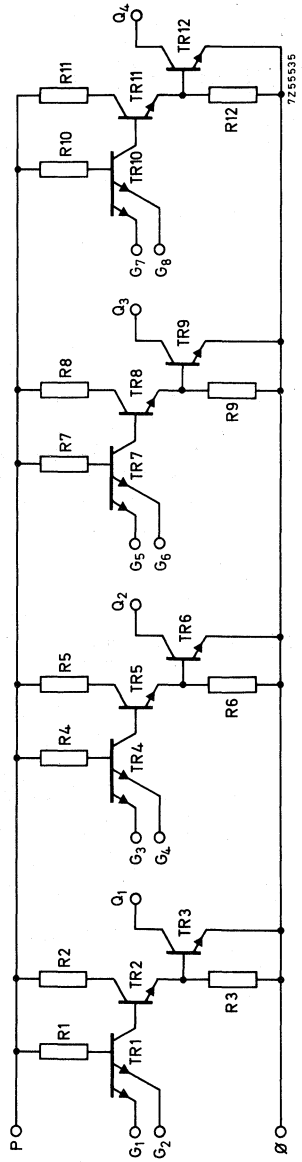


QUICK REFERENCE DATA				
Supply voltage	V_P		5±5%	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out (T_{amb} = 0 to +70 °C) LOW state	N_{aL}	max.	27	
Power consumption per gate at T_{amb} = 25 °C (50% duty cycle)	P_{av}	typ.	24	mW

The FZH181/4. LI30 is a level converter with open-collector outputs for interfacing TTL to HNIL and consists of 4 gates.

PACKAGE OUTLINE 14 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION

$Q = \overline{G_A \cdot G_B}$

(for positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7	V
Output voltage	V_Q	max.	V_P	1)
Input voltage	V_G	max.	5,5	V
Input current (V_P = 5 V)	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	5,5	V
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+70	°C
Uniform system supply voltage	V_P	4,75 to	5,25	V
Available d.c. fan-out	N_a	max.	27	
D.C. noise margin	M	min.	0,4	V
Supply current per gate; output HIGH (V_P = 5 V; V_G = 0 V)	I_{Pav}	max.	2,0	mA
output LOW (V_P = 5 V; V_G = 5 V)	I_{Pav}	max.	12,0	mA
Power consumption per gate at V_{Pmax} (50% duty cycle)	P_{tot}	max.	37	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

1) For HNIL.

CHARACTERISTICS Test conditions: V_P = 5 V; T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references V_P (V)	
Static data						
Voltages						
Input HIGH	V_{GH}	2,0	–	– V	4,75	V_{QL} = 1,0 V; I_{QL} = 50 mA
Input LOW	V_{GL}	–	–	0,8 V	4,75	V_{QH} = 18,0 V; I_{QH} = 250 µA
Output LOW	V_{QL}	–	–	0,4 V	4,75	V_{GH} = 2 V; I_{QL} = 16 mA
	V_{QL}	–	–	1,0 V	4,75	V_{GH} = 2 V; I_{QL} = 50 mA
D.C. noise margin: HIGH	M_H	0,4	–	– V		
LOW	M_L	0,4	–	– V		
Currents (per gate)						
Input HIGH	I_{GH}	–	–	40 µA	5,25	V_{GH} = 2,4 V
Input LOW	$-I_{GL}$	–	–	1,6 mA	5,25	V_{GL} = 0,4 V
Output HIGH	I_{QH}	–	–	250 µA	4,75	V_{QH} = 18 V; V_{GL} = 0,8 V
Output LOW	I_{QL}	50	–	– mA	4,75	V_{GH} = 2 V; V_{QL} = 1,0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	1,0	2,0 mA	5	V_{GL} = 0 V
at V_{QL}	I_P	–	8,5	12,0 mA	5	V_{GH} = 5 V
Dynamic data						
Times						
Propagation						
fall time	t_{pdf}	–	20	60 ns	12	V_Q = 12 V; R_L = 390 Ω
rise time	t_{pdr}	–	130	300 ns	12	V_Q = 12 V; R_L = 3,9 kΩ

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Calculation of collector resistor R_Q

The collector resistor R_Q has to be calculated from voltages and input- and output currents of the gates.

$$R_{Qmax} = \frac{V_P - V_{QH} \quad (V)}{m \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)} \qquad R_{Qmin} = \frac{V_P - V_{QL} \quad (V)}{I_{QLmax} - N \cdot I_{GL} \quad (mA)}$$

m = number of interconnected outputs
N = number of used inputs
V_P = supply voltage of HNIL inputs
V_{QH} = output voltage HIGH of HNIL-circuit
V_{QL} = output voltage LOW of HNIL-circuit
I_{GH} = input current HIGH of HNIL-circuit
I_{GL} = input current LOW of HNIL-circuit

For interfacing TTL to HNIL (range I; V_P = 12 V)

$$R_{Qmax} = \frac{12 - 10 \quad (V)}{m \cdot 250 + N \cdot 1 \quad (\mu A)} \qquad R_{Qmin} = \frac{12 - 1,0 \quad (V)}{50 - N \cdot 1,5 \quad (mA)}$$

For interfacing TTL to HNIL (range II; V_P = 15 V)

$$R_{Qmax} = \frac{15 - 12 \quad (V)}{m \cdot 250 - N \cdot 1 \quad (\mu A)} \qquad R_{Qmin} = \frac{15 - 1,0 \quad (V)}{50 - N \cdot 1,8 \quad (mA)}$$

If FZH181/4. LI30 is used as wired-OR combination

HIGH state

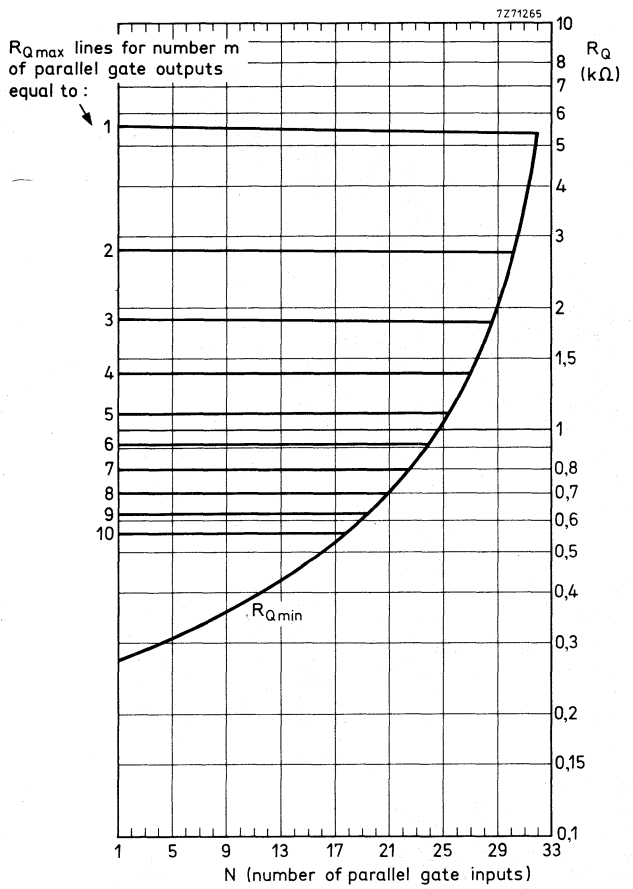
$$R_{Qmax} = \frac{V_P - 2,4 \quad (V)}{m \cdot 250 - N \cdot 40 \quad (\mu A)}$$

LOW state

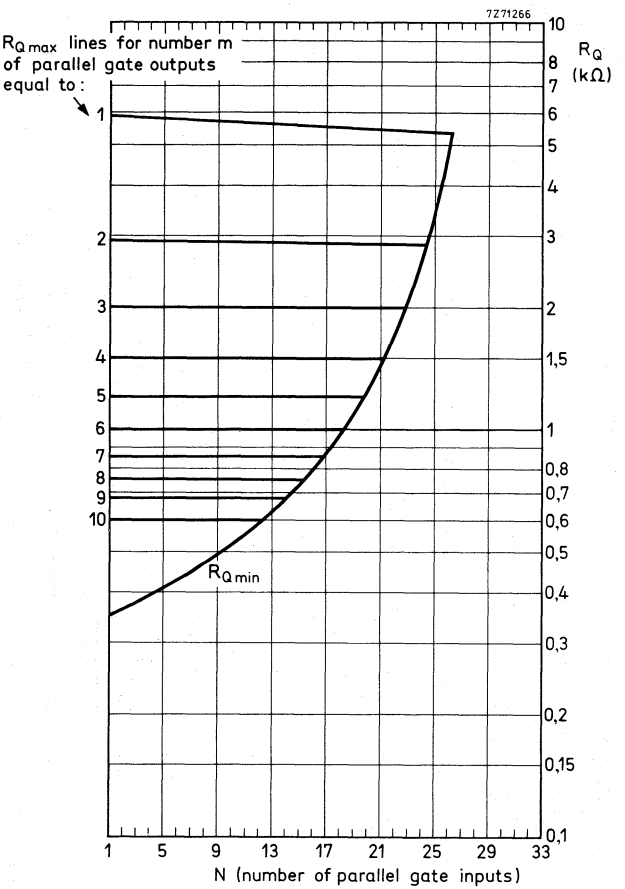
$$R_{Qmin} = \frac{V_P - 0,4 \quad (V)}{16 - N \cdot 1,6 \quad (mA)}$$

of which m = number of FZH181/4. LI30 OR combinations

N = number of used inputs



R_Q as a function of m and N at V_P = 12 V (range I).

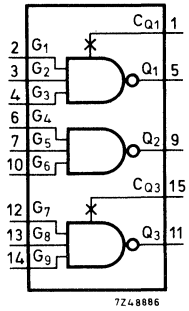


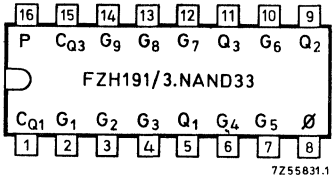
R_Q as a function of m and N at V_P = 15 V (range II).

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

TRIPLE 3-INPUT NAND GATE

with slow-down capability



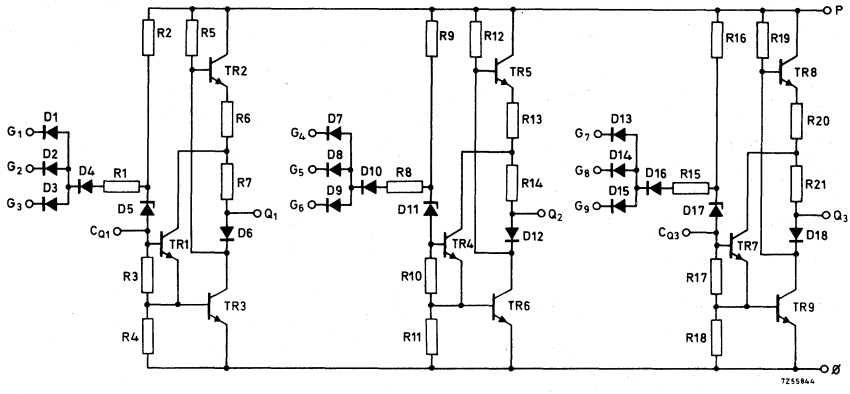


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}	0 to	+70	°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

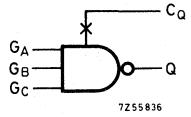
The FZH191/3.NAND33 consists of a number of independent NAND gates at which two NAND gates have a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A . G_B . G_C}$$

(positive logic)

Function table

G_A	G_B	G_C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current at range I ; output HIGH	I_{Pav}	typ.	0,9	mA
output LOW	I_{Pav}	typ.	1,7	mA
at range II ; output HIGH	I_{Pav}	typ.	1,2	mA
output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	31	mW
at range II ; V_{Pmax}	P_{tot}	max.	52	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1]) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 μA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	0,9	1,6 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay						
fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2]) Short-circuited duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

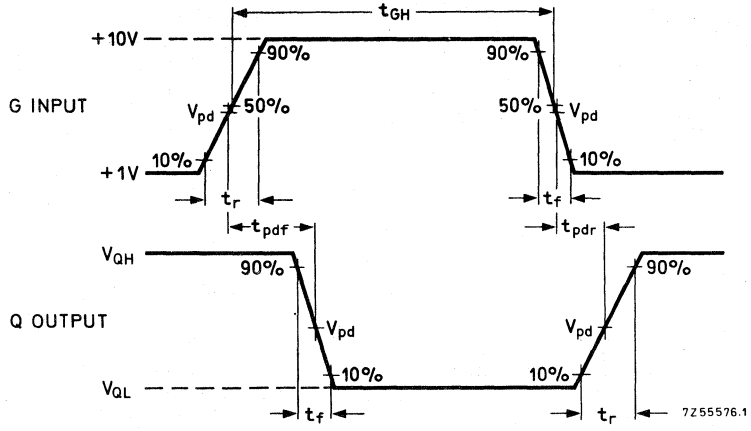
	Symbol	min.	typ.[1]	max.	Conditions and references: V_P (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	13,5	$V_{QL} \leqslant 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5 V	13,5 and 17	$V_{QH} \geqslant 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	– V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7 V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	– V	13,5	
LOW	M_L	2,8	5,0	– V	13,5	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 μA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8 mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	– mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	17	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	1,2	2,1 mA	17	V_G = 0 V
at V_{QL}	I_P	–	2,3	4,0 mA	17	V_G = 17 V
Dynamic data						
Times						
Propagation delay						
fall time	t_{pdf}	–	140	– ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{dp} = 4,5 V
rise time	t_{pdr}	–	195	– ns	15	
output rise time	t_r	–	410	– ns	15	
output fall time	t_f	–	75	– ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

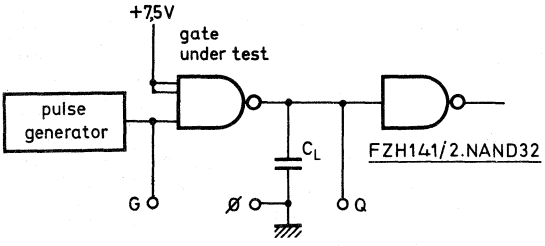
[2] Short-circuited duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = + 4,5 V
t_f = 120 ns
tGH = 1 µs

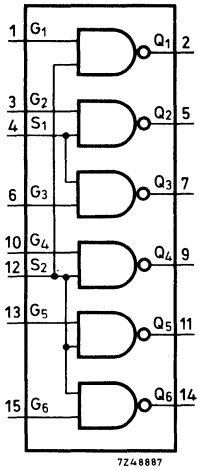


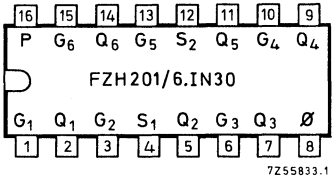
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SEXTUPLE INVERTER WITH STROBE INPUT



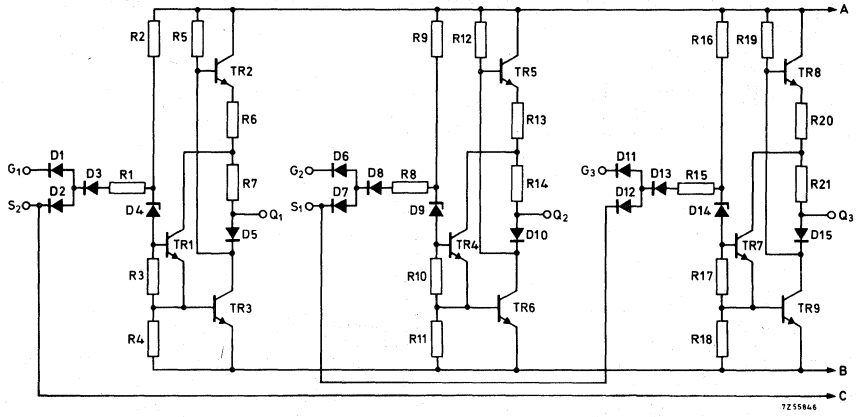


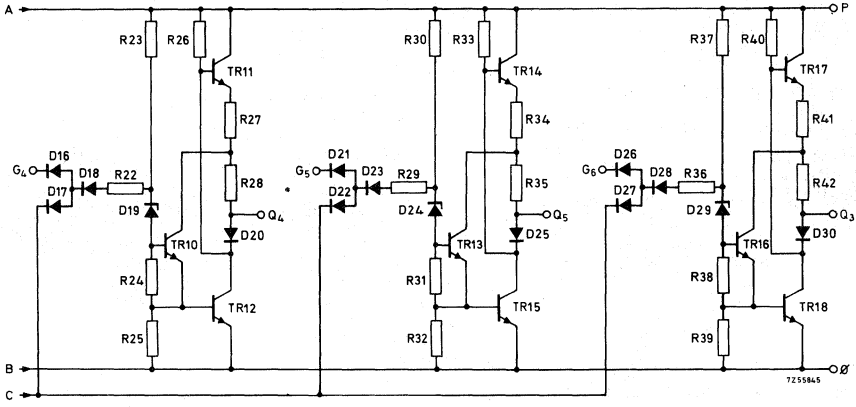
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay time ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170	ns
Available d.c. fan-out, $T_{amb} = 0$ to +70 °C; LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16	mW
range II: $V_P = 15$ V	P_{av}	typ.	27	mW

The FZH201/6.IN30 consists of a number of independent inverters without slow-down capability, but with a common strobe input.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM





LOGIC FUNCTION

$Q = \overline{G_A \cdot S}$ (positive logic)

Function table

G_A	S	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.		18	V
Output voltage	V_Q	max.		V_P	
Input voltage	V_G	max.		18	V
Input current at V_P = 17 V	$-I_{GL}$	max.		25	mA
Voltage difference between any two inputs		max.		18	V
Storage temperature	T_{stg}	−65	to	+150	°C
Operating ambient temperature	T_{amb}	0	to	+70	°C
Output short-circuit duration	t_{Qsc}	max.		1	s [1]

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to 17		V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate: range I ; output HIGH	I_{Pav}	typ.	0,9	mA
output LOW	I_{Pav}	typ.	1,7	mA
range II; output HIGH	I_{Pav}	typ.	1,2	mA
output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	31	mW
at range II; V_{Pmax}	P_{tot}	max.	52	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	0,9	1,6 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	1,7	3,0 mA	13,5	V_G = 13,5 V
Dynamic data						
Times						
Propagation delay: fall time	t_{pdf}	90	175	310 ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310 ns	12	
output rise time	t_r	200	340	570 ns	12	
output fall time	t_f	70	120	210 ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2]) Short-circuited duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

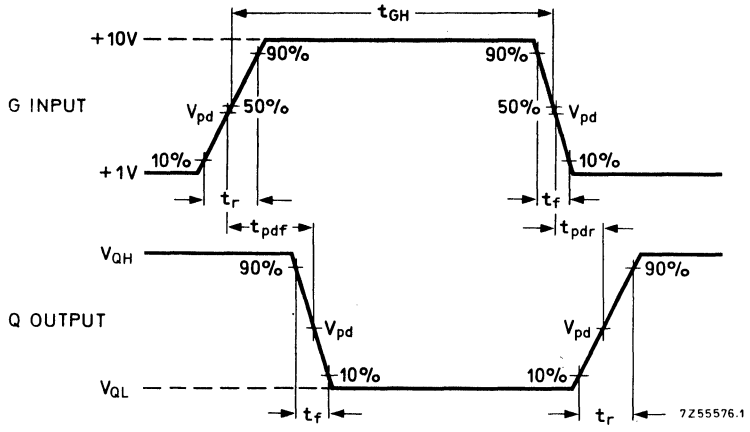
	Sym-bol	min.	typ.[1]	max.	Conditions and references	
					V_P (V)	
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	-	- V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	-	-	4,5 V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	- V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	-	1,0	1,7 V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	- V	13,5	
LOW	M_L	2,8	5,0	- V	13,5	
Currents (per gate)						
Input HIGH	I_{GH}	-	-	1,0 µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	-	1,0	1,8 mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	-	- mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	-	- mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	17	V_G = 0 V; V_Q = 0 V
Dynamic data						
Currents (per gate)						
at V_{QH}	I_P	-	1,2	2,1 mA	17	V_G = 0 V
at V_{QL}	I_P	-	2,3	4,0 mA	17	V_G = 17 V
Supply data						
Times						
Propagation delay:						
fall time	t_{pdf}	-	140	- ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	-	195	- ns	15	
output rise time	t_r	-	410	- ns	15	
output fall time	t_f	-	75	- ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

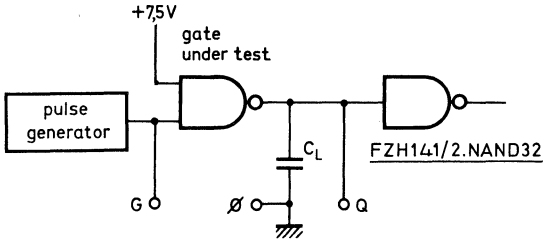
[2] Short-circuited duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = + 4,5 V
t_f = 120 ns
t_{GH} = 1 µs



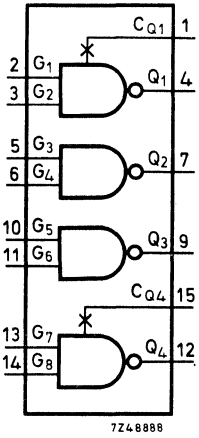
Measuring conditions: Vp = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

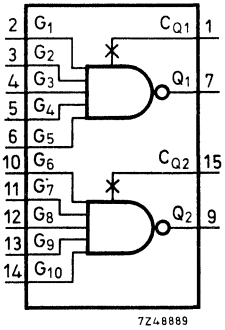
The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE 2-INPUT NAND GATE
DUAL 5-INPUT NAND GATE

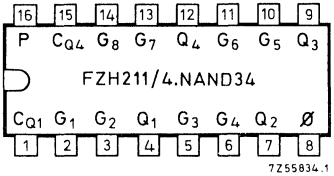
both having slow-down capability and open collector

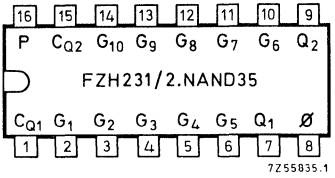


FZH211/4.NAND34



FZH231/2.NAND35





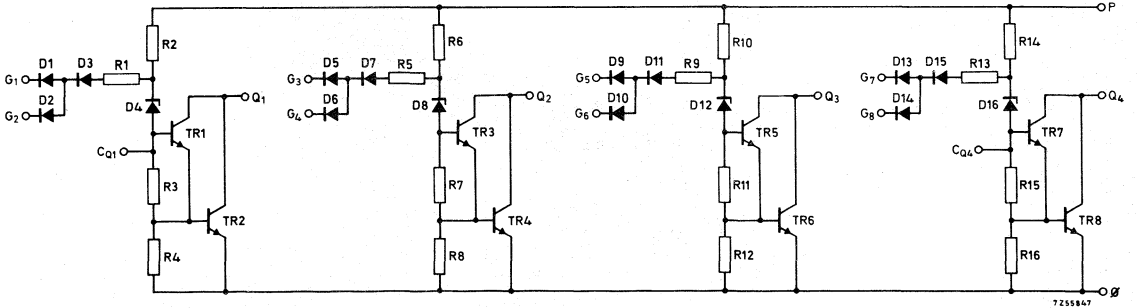
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C				
(50% duty cycle) range I: V_P = 12 V	P_{av}	typ.	8,5	mW
range II: V_P = 15 V	P_{av}	typ.	15	mW

The FZH211/4.NAND34 and FZH231/2.NAND35 consist of a number of independent NAND gates with open collector and two gates of each circuit have a slow-down terminal. It is possible to connect a capacitor between the output Q and the corresponding slow-down terminal C_Q to increase the propagation delay.
The outputs of these gates may be interconnected to perform the AND-OR-NOT function.

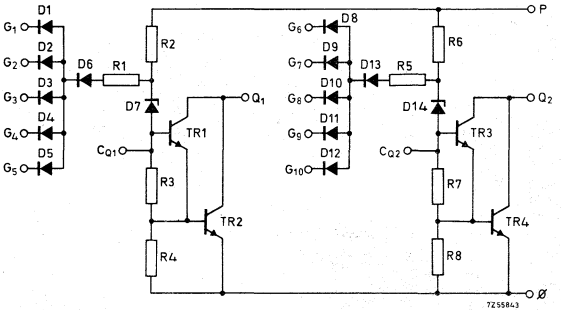
PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAMS

FZH211/4.NAND34



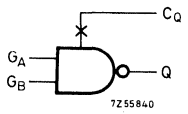
FZH231/2.NAND35



LOGIC FUNCTION

1. Individual gate operation

FZH211/4.NAND34



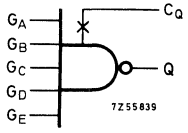
$$Q = \overline{G_A \cdot G_B}$$

(positive logic)

FUNCTION TABLES

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

FZH231/2.NAND35

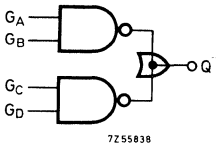


$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$$

(positive logic)

G_A	G_B	G_C	G_D	G_E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

2. Wired-OR combination



$$Q = \overline{(\overline{G_A \cdot G_B}) \cdot (\overline{G_C \cdot G_D})} = \overline{(G_A \cdot G_B) + (G_C \cdot G_D)}$$

(positive logic)

G_A	G_B	G_C	G_D	Q
L	X	L	X	H
L	X	X	L	H
X	L	X	L	H
X	L	L	X	H
H	H	X	X	L
X	X	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I; output HIGH	I_{Pav}	max.	2,1	mA
output LOW	I_{Pav}	max.	1,2	mA
range II; output HIGH	I_{Pav}	max.	2,1	mA
output LOW	I_{Pav}	max.	1,4	mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax}	P_{tot}	max.	18	mW
at range II; V_{Pmax}	P_{tot}	max.	30	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1])	max.	Conditions and references	
					V_P (V)	
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per gate)						
Input HIGH	I_{GH}	–	–	1,0 µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	I_{QH}	–	–	80 µA	11,4	V_{GL} = 4,5 V; V_{QH} = 18 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Supply data						
Currents (per gate)						
at V_{QH}	I_P	–	1,0	1,7 mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	0,4	1,0 mA	13,5	V_G = 13,5 V

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	I_{QH}	–	–	80	µA	13,5	V_{GL} = 4,5 V; V_{QH} = 18 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	1,3	2,1	mA	17	V_G = 0 V
at V_{QL}	I_P	–	0,7	1,4	mA	17	V_G = 17 V

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

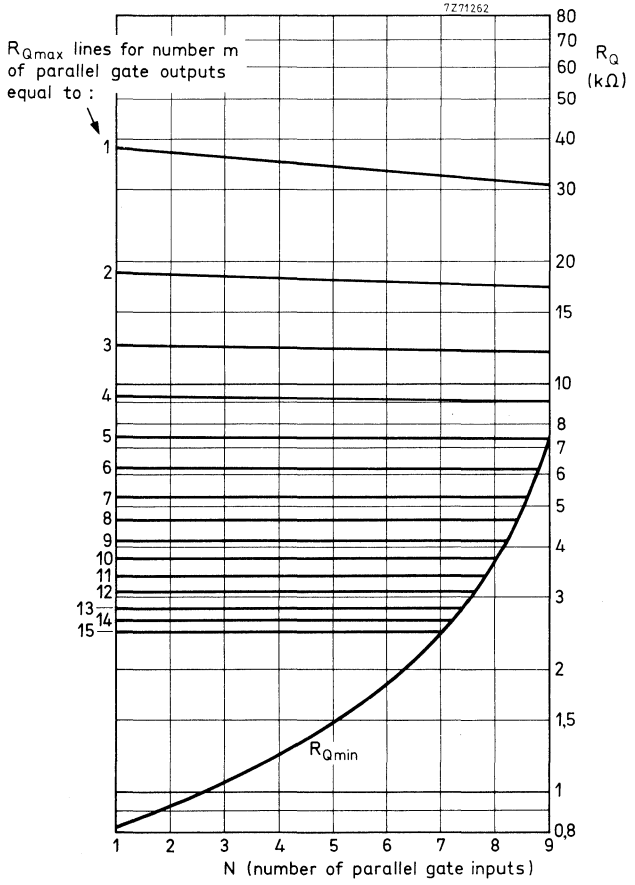
CHARACTERISTICS (continued)

Calculation of collector resistor R_Q

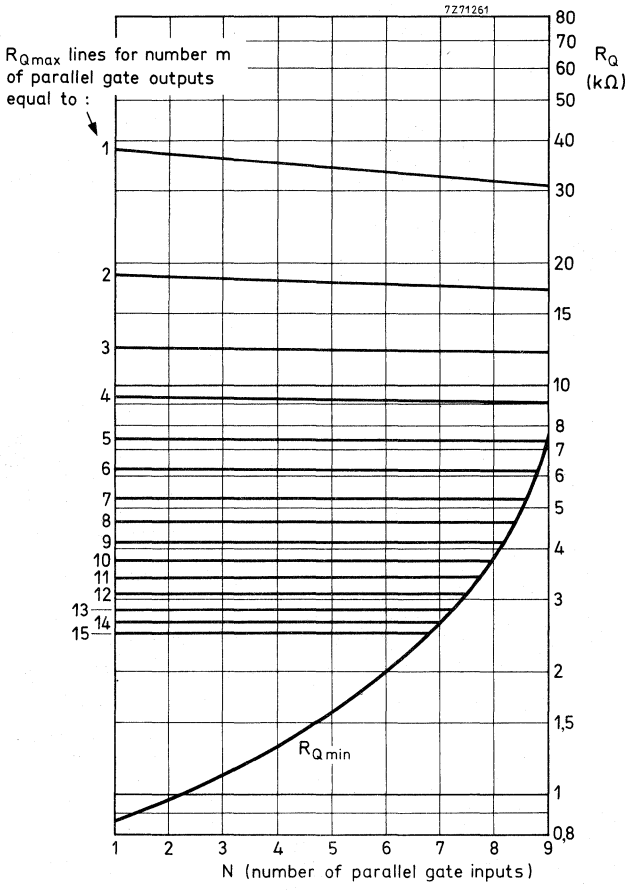
The collector resistor R_Q has to be calculated from voltages and input- and output currents of the gates.

$$R_{Qmax} = \frac{V_P - V_{QH} \quad (V)}{m \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)} \qquad R_{Qmin} = \frac{V_P - V_{QL} \quad (V)}{I_{QLmax} - N \cdot I_{GL} \quad (mA)}$$

m = number of interconnected outputs
N = number of used inputs
V_P = supply voltage of HNIL inputs
V_{QH} = output voltage HIGH of HNIL - circuit
V_{QL} = output voltage LOW of HNIL - circuit



R_Q as a function of m and N at V_P = 12 V (range I).

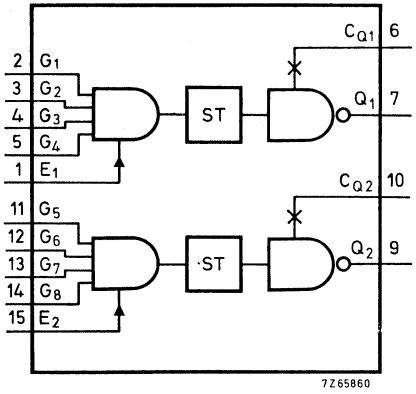


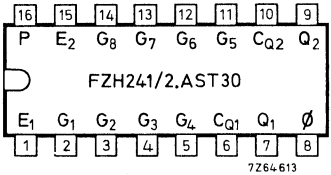
R_Q as a function of m and N at V_P = 15 V (range II).

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL 4-INPUT NAND SCHMITT TRIGGER

with slow-down capability and expandable inputs



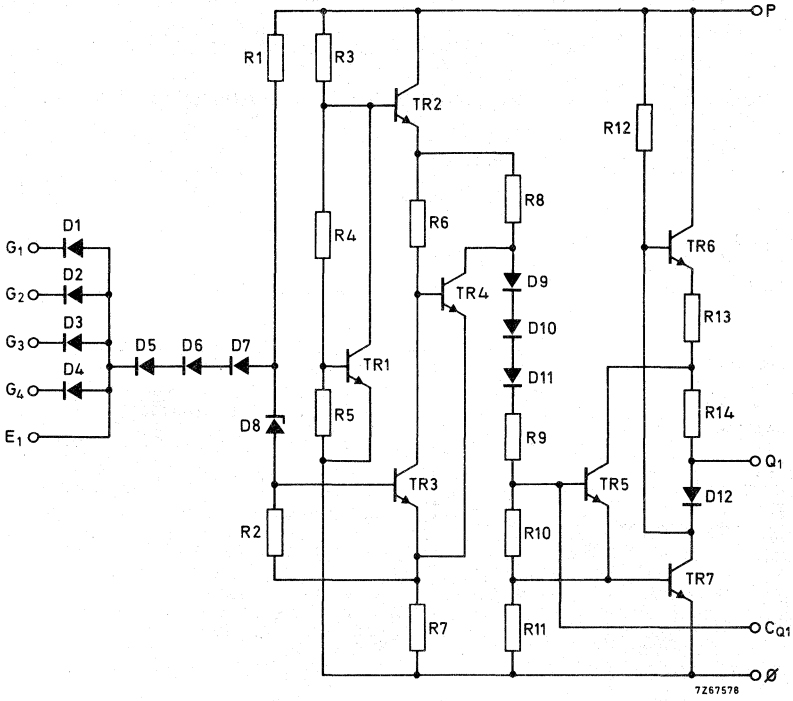


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C				
(50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	48	mW
range II: V_P = 15 V	P_{av}	typ.	72	mW

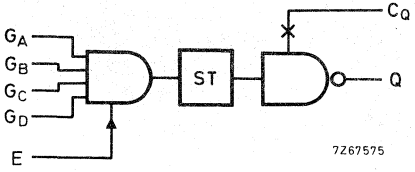
The FZH241/2.AST30 consists of two identical 4-input NAND SCHMITT triggers with slow-down capability and expandable inputs.
Each circuit functions as a 4-input NAND gate (without using the expandable input), but because of the SCHMITT action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, which is the difference between the two threshold levels, is typically 900 mV.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot E}$$

FUNCTION TABLE

G_A	G_B	G_C	G_D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out; LOW state	N_{aL}	max.	10	
HIGH state	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I : output HIGH	I_{Pav}	typ.	4,0	mA
output LOW	I_{Pav}	typ.	3,8	mA
range II: output HIGH	I_{Pav}	typ.	4,5	mA
output LOW	I_{Pav}	typ.	5,0	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	85	mW
at range II; V_{Pmax}	P_{tot}	max.	105	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1]) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	8,0	–	–	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	5,0	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	11,4	V_{GH} = 8,0 V; I_{QL} = 15 mA
Positive-going threshold voltage	V_{TP}	–	7,1	–	V	12	
Negative-going threshold voltage	V_{TN}	–	6,2	–	V	12	
Hysteresis [2]	V_H	–	0,9	–	V	12	
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	–	1,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	V_{GL} = 5,0 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{GH} = 8,0 V; V_{QL} = 1,7 V
Output short-circuited [3]	$-I_{Qsc}$	9	15	25	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	4,0	6,3	mA	13,5	V_G = 0 V
at V_{QL}	I_P	–	3,8	6,0	mA	13,5	V_G = 13,5 V

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) $V_H = V_{TP} - V_{TN}$.
[3]) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

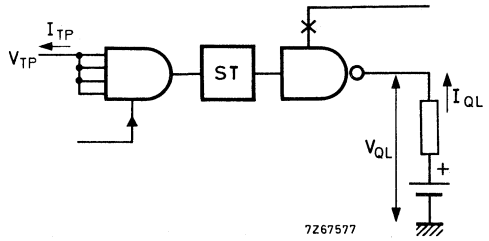
	Symbol	min.	typ. [1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	8,0	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	5,0	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,1	1,7	V	13,5	V_{GH} = 8,0 V; I_{QL} = 18 mA
Positive-going threshold voltage	V_{TP}	–	7,05	–	V	15	
Negative-going threshold voltage	V_{TN}	–	6,15	–	V	15	
Hysteresis [2])	V_H	–	0,9	–	V	15	
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	–	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 5,0 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 8,0 V; V_{QL} = 1,7 V
Output short-circuited [3])	$-I_{Qsc}$	9	15	25	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	4,5	7,3	mA	17	V_G = 0 V
at V_{QL}	I_P	–	5,0	8,0	mA	17	V_G = 17 V

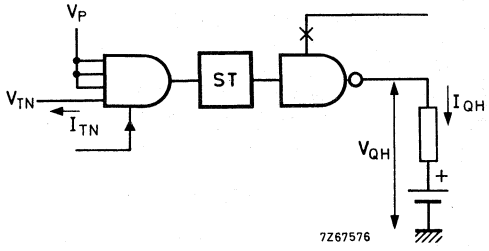
1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
2) $V_H = V_{TP} - V_{TN}$.
3) Short-circuit duration max. 1 s.

CHARACTERISTICS

D.C. test circuit for V_{TP}, V_{TN} and V_H

conditions: V_P = 12 V (range I); ϕ to earth;
V_P = 15 V (range II); T_{amb} = 25 °C

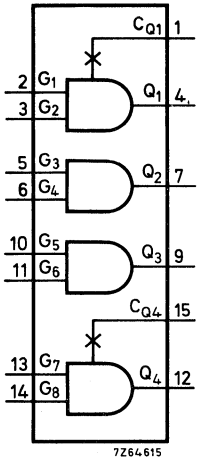


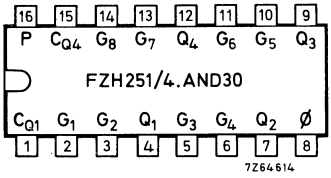


The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE 2—INPUT AND GATE

with slow-down capability



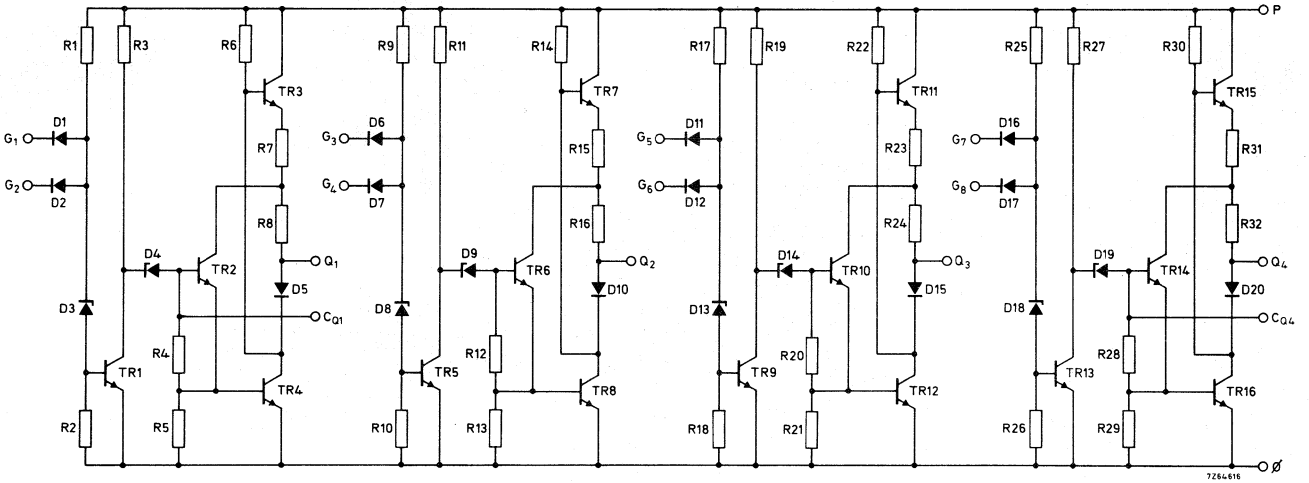


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay N = 1; C_L = 10 pF; T_{amb} = 25 °C; V_{pd} = 4,5 V	t_{pd}	typ.	260	ns
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II: V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C (50 % duty cycle) range I : V_P = 12 V	P_{av}	typ.	24	mW
range II: V_P = 15 V	P_{av}	typ.	42,8	mW

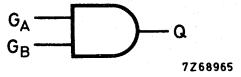
The FZH251/4.AND30 consists of four 2-input AND gates, two of which may be slowed down.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTIONS



Function table

G_A	G_B	Q
L	X	L
X	L	L
H	H	H

$Q = G_A \cdot G_B$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate: range I; output HIGH	I_{Pav}	typ.	1,6	mA
output LOW	I_{Pav}	typ.	2,4	mA
range II; output HIGH	I_{Pav}	typ.	2,2	mA
output LOW	I_{Pav}	typ.	3,5	mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax}	P_{tot}	max.	51,5	mW
at range II; V_{Pmax}	P_{tot}	max.	84	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1]) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; $I_{QL} = 15$ mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	$V_{GH} = 7,5$ V; $I_{QL} = 15$ mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	13,5	$V_{GH} = 13,5$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	$V_{GL} = 1,7$ V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	$V_{GL} = 4,5$ V; $V_{QH} = 10$ V
Output LOW	I_{QL}	15	–	–	mA	11,4	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	3	4,5	mA	13,5	$V_G = 0$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$C_L = 10$ pF; N = 1; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V
rise time	t_{pdr}	200	340	570	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2]) Short-circuit duration max. 1 s.

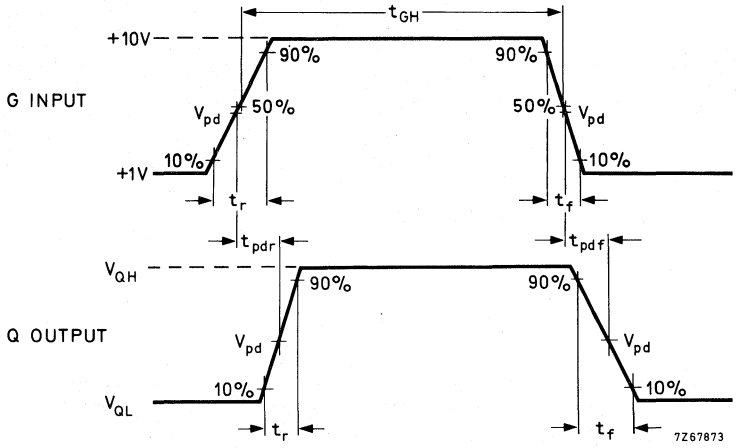
CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; $I_{QL} = 18$ mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	$V_{GH} = 7,5$ V; $I_{QL} = 18$ mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	$V_{GH} = 17$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	$V_{GL} = 1,7$ V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	$V_{GL} = 4,5$ V; $V_{QH} = 12$ V
Output LOW	I_{QL}	18	–	–	mA	13,5	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	3,7	6	mA	17	$V_G = 0$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	–	t.b.f.	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output all time	t_f	–	t.b.f.	–	ns	15	

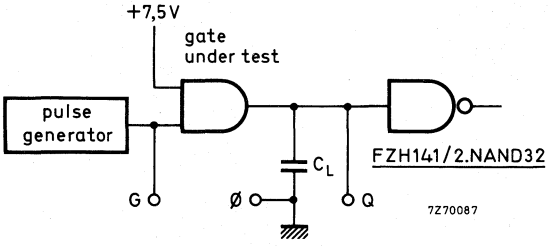
[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS

Dynamic data



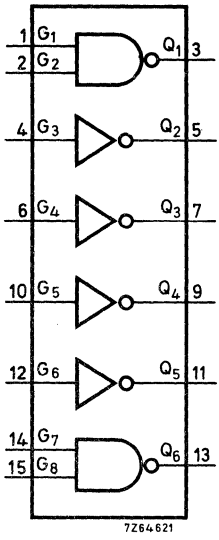
Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs



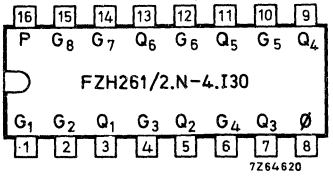
Measuring conditions: V_P = + 12 V; + 15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.



DUAL NAND GATE/ QUADRUPLE INVERTER

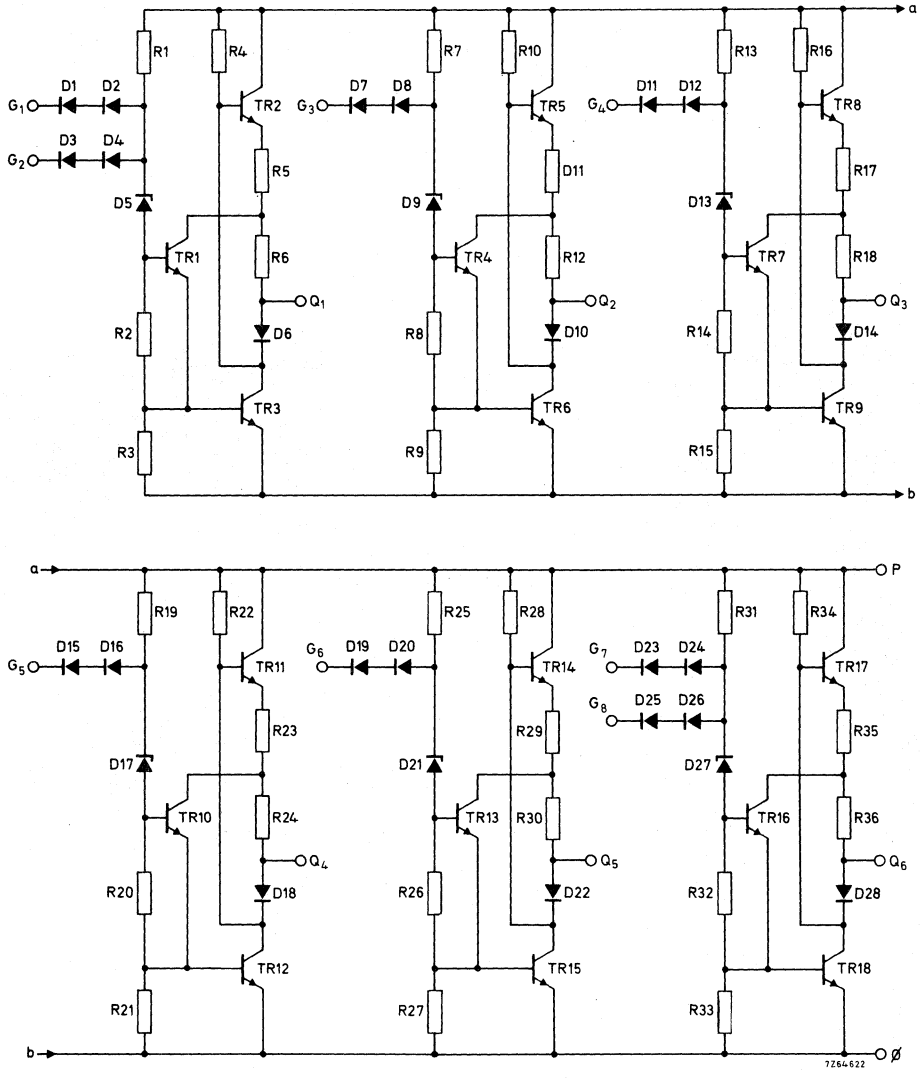


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	175	ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16,2	mW
range II: $V_P = 15$ V	P_{av}	typ.	28,5	mW

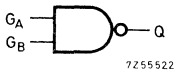
The FZH261/2.N-4.I30 consists of two 2-input NAND gates and four inverters, none of which have the slow-down facility.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

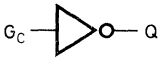
CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = \overline{G_A . G_B}$ (positive logic)



$Q = \overline{G_C}$ (positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min	2,8	V
	M_H	min	4,5	V
Supply current per gate; range I; output HIGH	I_{Pav}	typ.	1,0	mA
output LOW	I_{Pav}	typ.	1,7	mA
range II; output HIGH	I_{Pav}	typ.	1,4	mA
output LOW	I_{Pav}	typ.	2,4	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	34,3	mW
at range II; V_{Pmax}	P_{tot}	max.	56	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; $I_{QL} = 15$ mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	$V_{GH} = 7,5$ V; $I_{QL} = 15$ mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	1,7	3	mA	13,5	V_G = 13,5 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

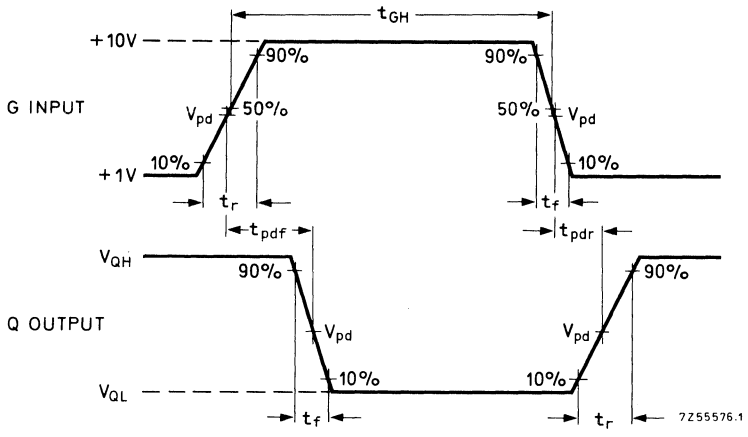
	Sym-bol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	2,4	4	mA	17	V_G = 17 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	–	t.b.f.	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output fall time	t_f	–	t.b.f.	–	ns	15	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

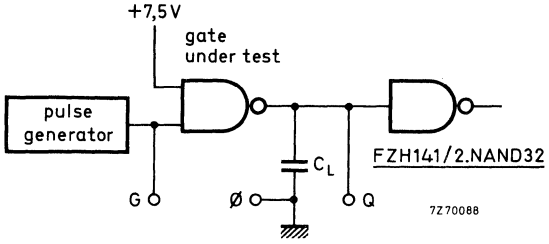
[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs

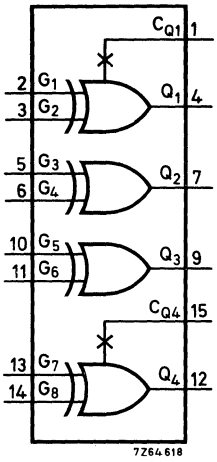


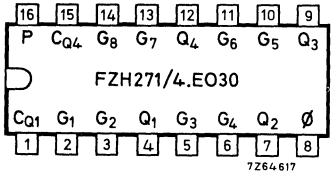
Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE EXCLUSIVE-OR GATE
with slow-down capability



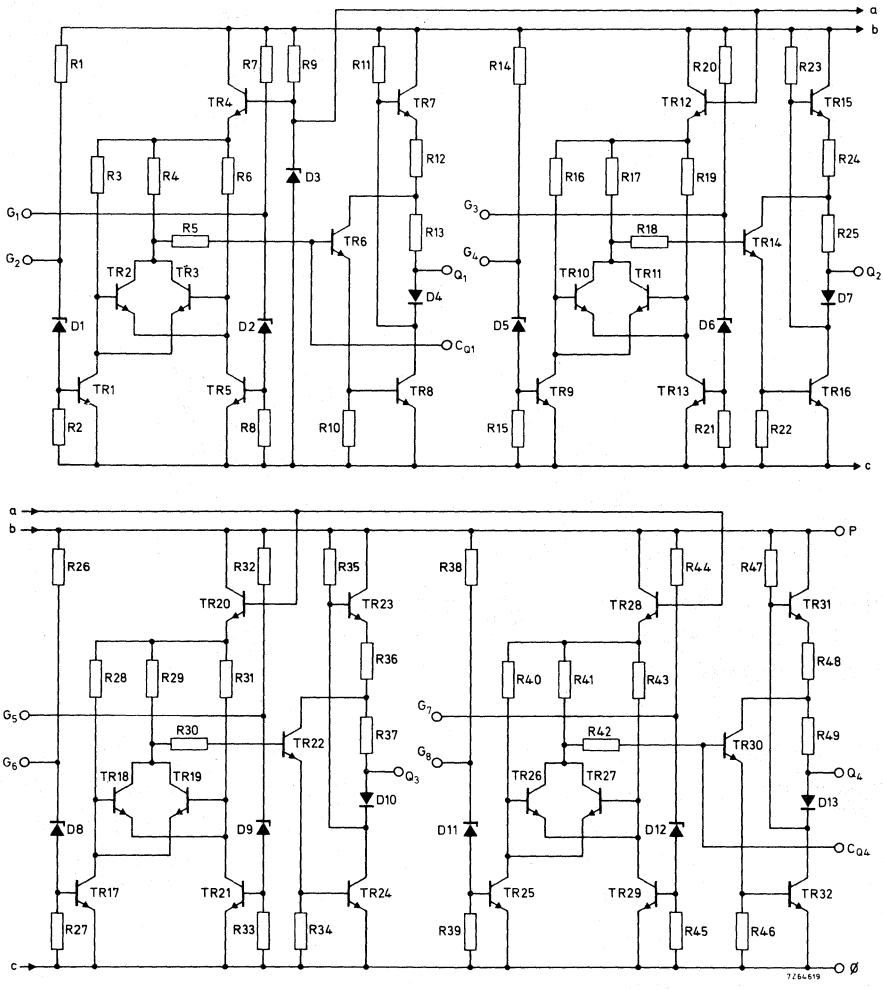


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay N = 1; C_L = 10 pF; T_{amb} = 25 °C; V_{pd} = 4,5 V	t_{pd}	typ.	260	ns
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : Vp = 12 V	$M_L = M_H$	typ.	5	V
range II: Vp = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at T_{amb} = 25 °C (50% duty cycle) range I : Vp = 12 V	P_{av}	typ.	43,5	mW
range II: Vp = 15 V	P_{av}	typ.	66,8	mW

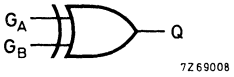
The FZH271/4.EO30 consists of four 2-input EXCLUSIVE-OR gates, two of which may be slowed down.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = G_A.\overline{G}_B + \overline{G}_A.G_B$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

Function table

G_A	G_B	Q
L	L	L
H	L	H
L	H	H
H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Suppy current per gate; range I ; output HIGH	I_{Pav}	typ.	3,45	mA
output LOW	I_{Pav}	typ.	3,8	mA
range II; output HIGH	I_{Pav}	typ.	4,1	mA
output LOW	I_{Pav}	typ.	4,8	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	76,8	mW
at range II; V_{Pmax}	P_{tot}	max.	114,8	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	3,8	6	mA	13,5	V_G = 13,5 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	200	340	570	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

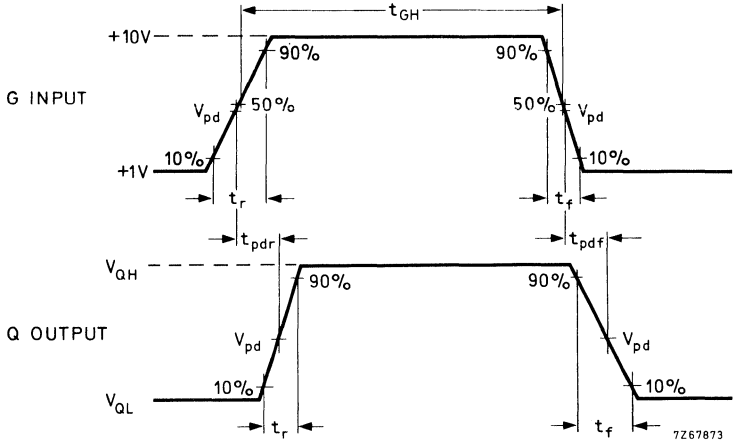
	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; $I_{QL} = 18$ mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	$V_{GH} = 7,5$ V; $I_{QL} = 18$ mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	17	$V_{GH} = 17$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	$V_{GL} = 1,7$ V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	$V_{GL} = 4,5$ V; $V_{QH} = 12$ V
Output LOW	I_{QL}	18	–	–	mA	13,5	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	4,8	7,5	mA	17	$V_G = 17$ V
Dynamic data							
Times							
Propagation delay fall time	t_{pdf}	–	t.b.f.	–	ns	15	$C_L = 10$ pF; N = 1; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V
rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output fall time	t_f	–	t.b.f.	–	ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

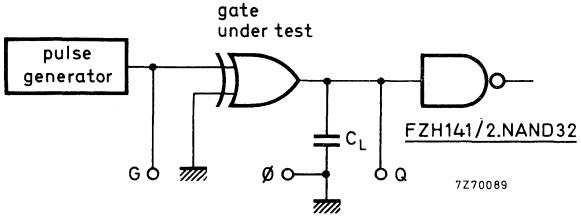
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs

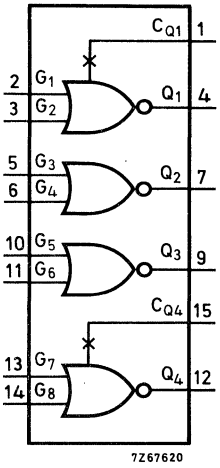


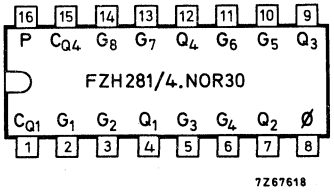
Measuring conditions: Vp = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE NOR GATE
with slow-down capability



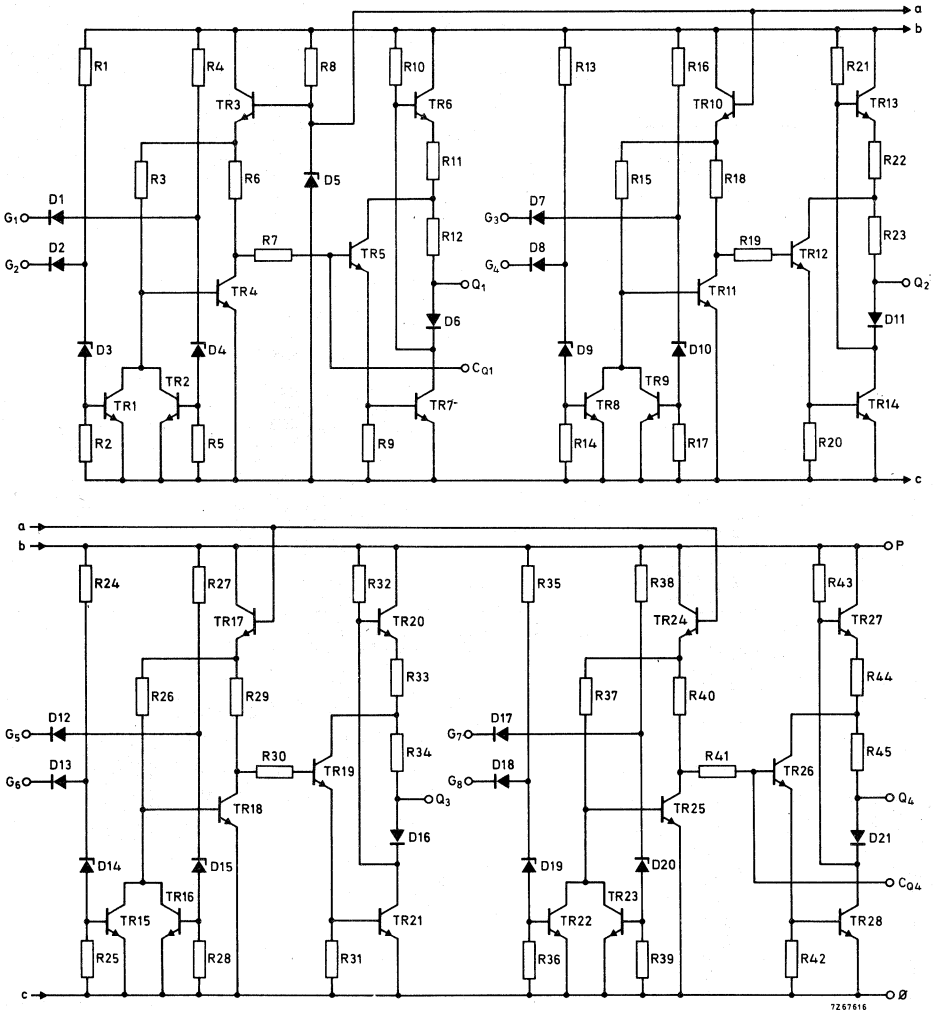


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	260	ns
Available d.c. fan-out, $T_{amb} = 0$ to +70 °C; LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	42	mW
range II: $V_P = 15$ V	P_{av}	typ.	63,8	mW

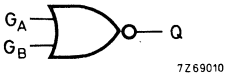
The FZH281/4.NOR30 consists of four 2-input NOR gates, two of which have the slow-down facility.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = \overline{G_A + G_B}$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

Function table

G_A	G_B	Q
L	L	H
H	X	L
X	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I ; output HIGH	I_{Pav}	typ.	3,3	mA
output LOW	I_{Pav}	typ.	3,7	mA
range II; output HIGH	I_{Pav}	typ.	3,8	mA
output LOW	I_{Pav}	typ.	4,7	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	76,8	mW
at range II; V_{Pmax}	P_{tot}	max.	114,8	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	13,5	V_{GH} = 13,5 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	V_{GL} = 1,7 V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	3,7	6	mA	13,5	V_G = 13,5 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	200	340	570	ns	12	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

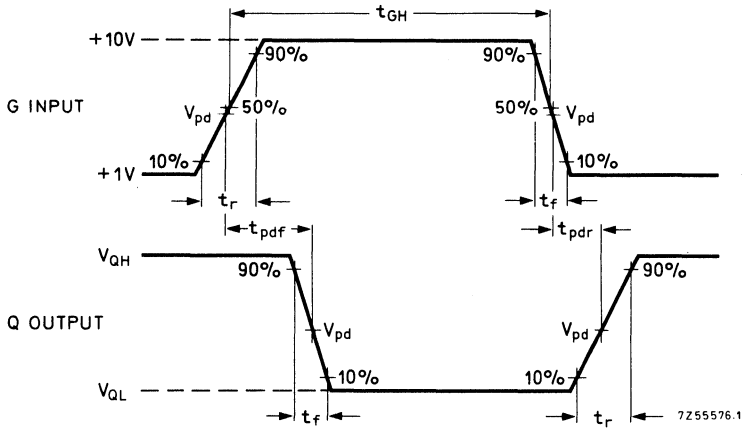
	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QL}	I_P	–	4,7	7,5	mA	17	V_G = 17 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	–	t.b.f.	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output fall time	t_f	–	t.b.f.	–	ns	15	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

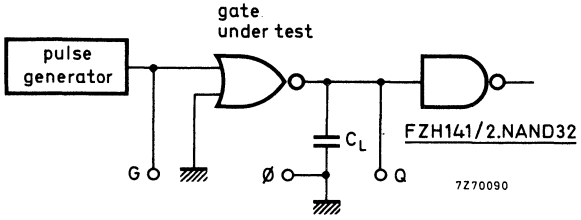
[2]) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs

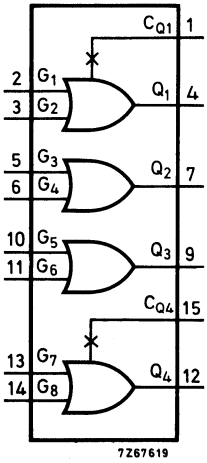


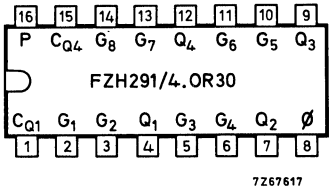
Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE OR GATE
with slow-down capability



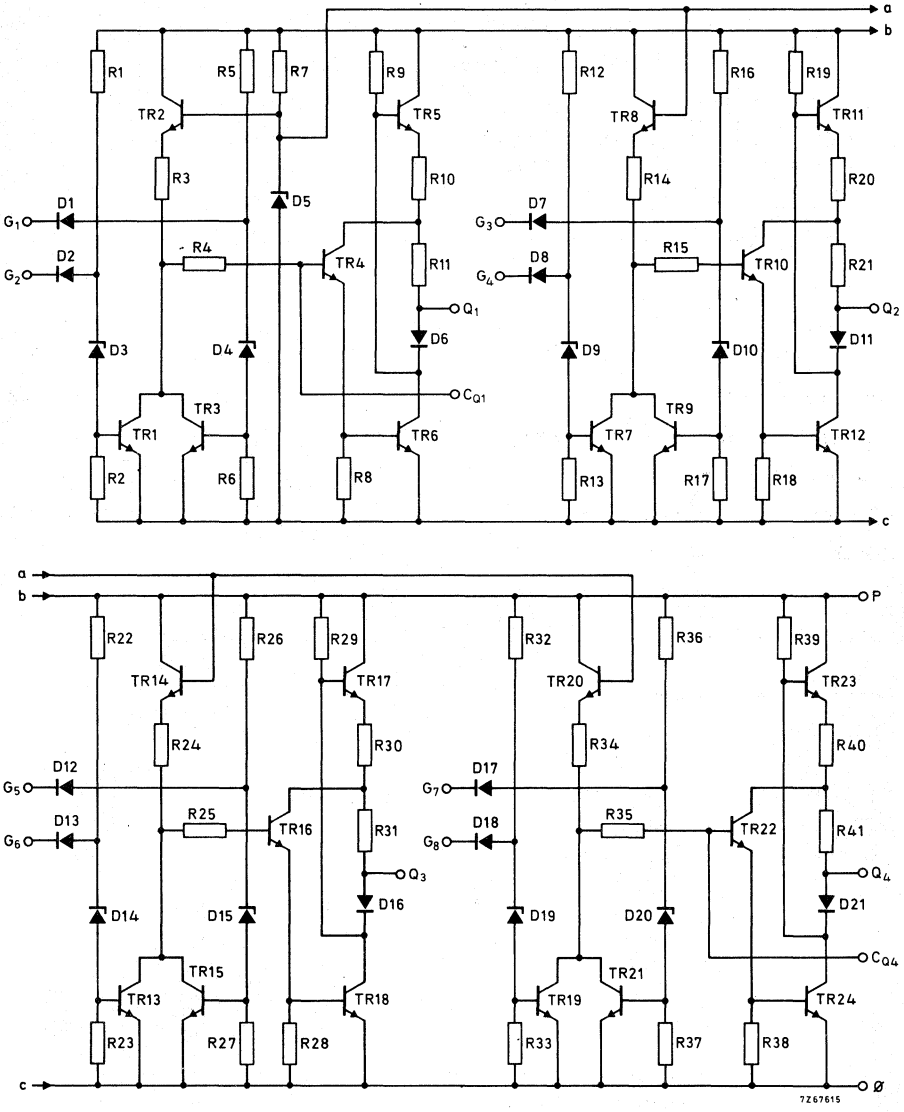


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	260	ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10	
D.C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II: $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	35,1	mW
range II: $V_P = 15$ V	P_{av}	typ.	54	mW

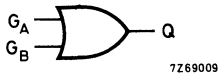
The FZH291/4.OR30 consists of four 2-input OR gates, two of which may be slowed down.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$Q = G_A + G_B$ (positive logic)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

Function table

G_A	G_B	Q
L	L	L
H	X	H
X	H	H

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at V_P = 17 V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

[1]) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current per gate; range I ; output HIGH	I_{Pav}	typ.	2,25	mA
output LOW	I_{Pav}	typ.	3,6	mA
range II; output HIGH	I_{Pav}	typ.	2,6	mA
output LOW	I_{Pav}	typ.	4,6	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	64,1	mW
at range II; V_{Pmax}	P_{tot}	max.	104,1	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4	$V_{QL} \leq 1,7$ V; $I_{QL} = 15$ mA
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	10,0	11,3	–	V	11,4 and 13,5	$V_{GL} = 4,5$ V; $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	$V_{GH} = 7,5$ V; $I_{QL} = 15$ mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	μA	13,5	$V_{GH} = 13,5$ V; other inputs 0 V
Input LOW	$-I_{GL}$	–	0,8	1,5	mA	13,5	$V_{GL} = 1,7$ V; other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	$V_{GL} = 4,5$ V; $V_{QH} = 10$ V
Output LOW	I_{QL}	15	–	–	mA	11,4	$V_{GH} = 7,5$ V; $V_{QL} = 1,7$ V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	3,6	5,8	mA	13,5	$V_G = 13,5$ V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$C_L = 10$ pF; N = 1; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V
rise time	t_{pdr}	200	340	570	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

[2] Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

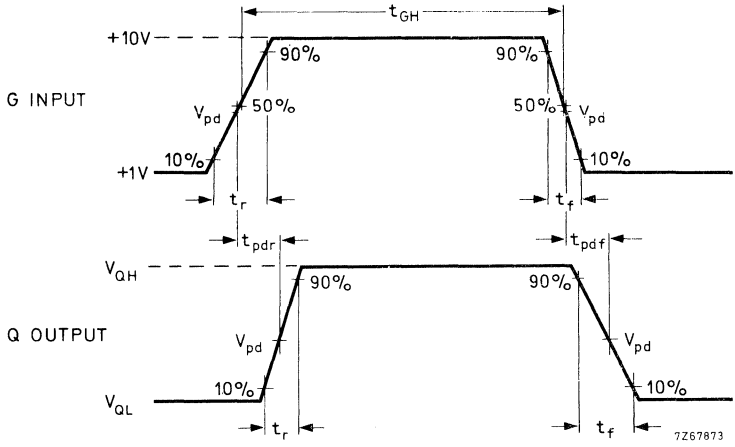
	Sym-bol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per gate)							
Input HIGH	I_{GH}	–	–	1,0	µA	17	V_{GH} = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25	mA	17	V_G = 0 V; V_Q = 0 V
Supply data							
Currents (per gate)							
at V_{QH}	I_P	–	4,6	7,3	mA	17	V_G = 17 V
Dynamic data							
Times							
Propagation delay							
fall time	t_{pdf}	–	t.b.f.	–	ns	15	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
rise time	t_{pdr}	–	t.b.f.	–	ns	15	
output rise time	t_r	–	t.b.f.	–	ns	15	
output fall time	t_f	–	t.b.f.	–	ns	15	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

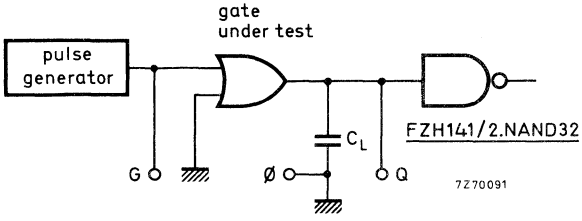
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns V_{pd} = +4,5 V
t_f = 120 ns
t_{GH} = 1 µs



Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C

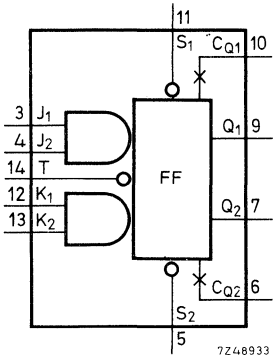
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

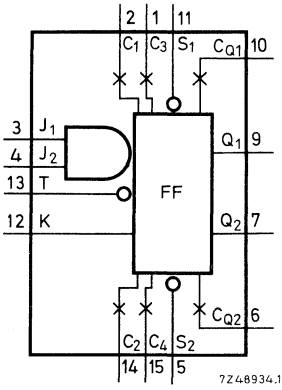
SINGLE JK MASTER-SLAVE FLIP-FLOPS

FZJ101/FF30: with slow-down capability on the slave

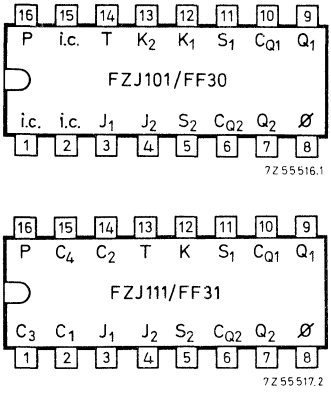
FZJ111/FF31: with slow-down capability on master and slave



FZJ101/FF30



FZJ111/FF31

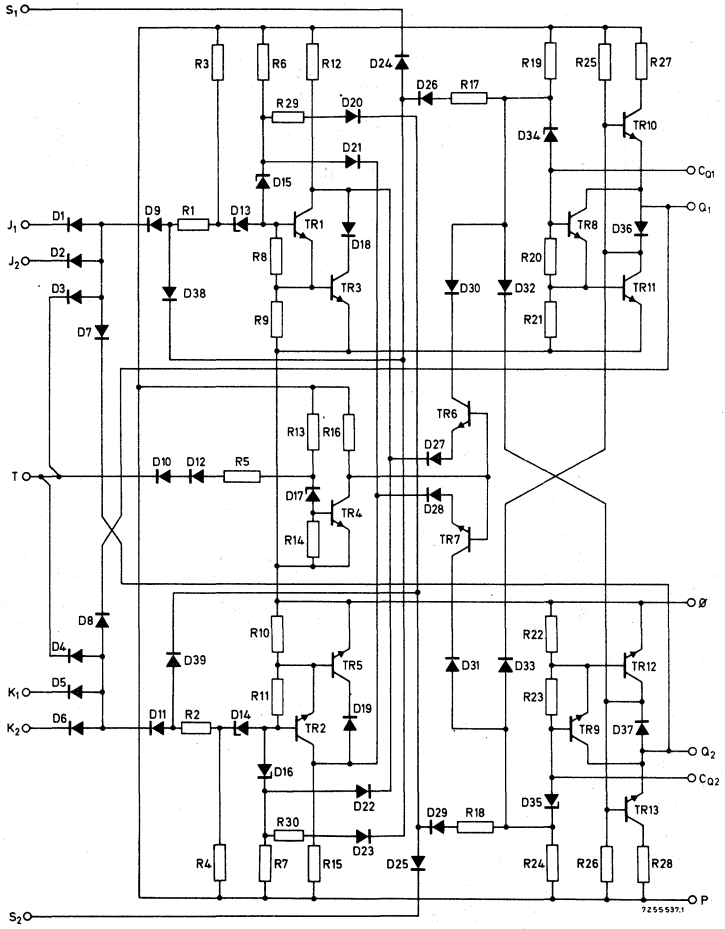


QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out (T_{amb} = 0 to +70 °C) } LOW state	N_{aL}	max.	10	
Operating frequency at T_{amb} = 25 °C; duty cycle 50%; range I/II	f_c	typ.	0,5	MHz
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	8	mA
V_P = 17 V	I_{Pav}	typ.	11	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V

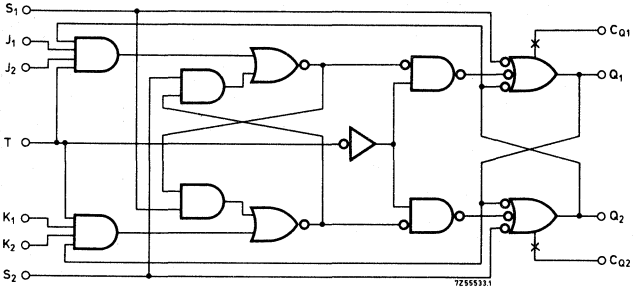
PACKAGE OUTLINE 16-lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM

FZJ101/FF30

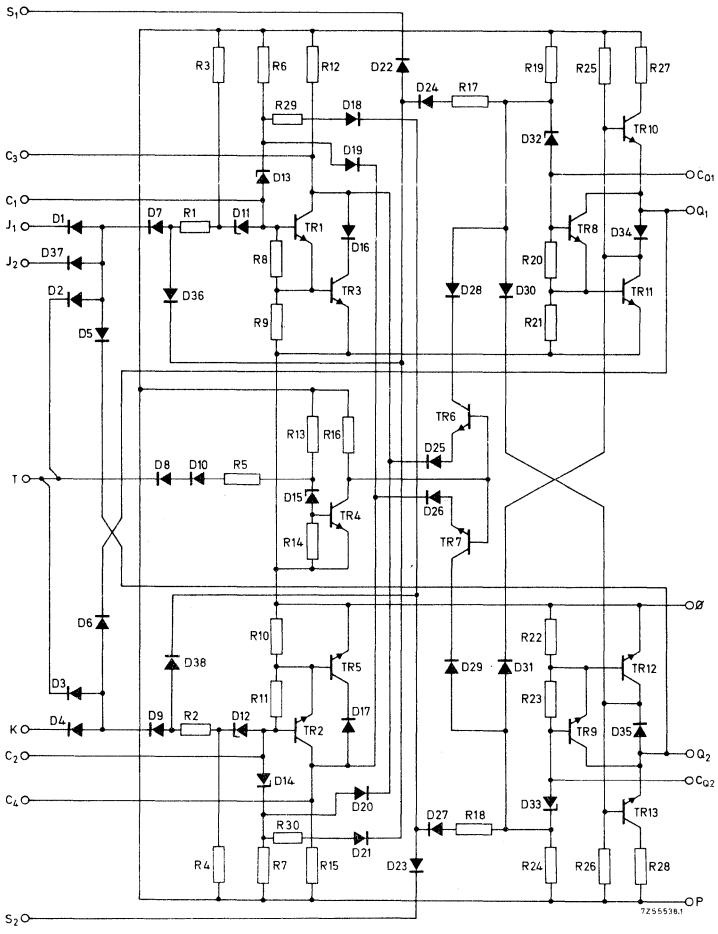


LOGIC DIAGRAM

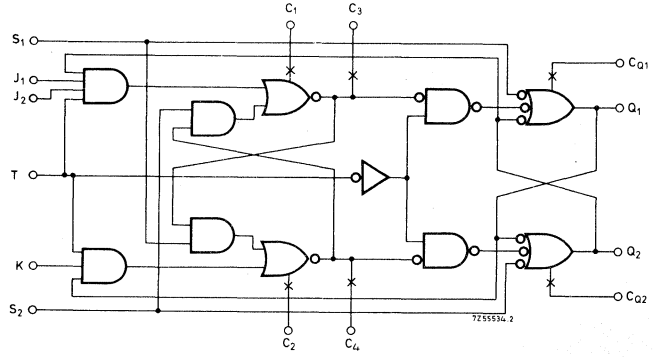


CIRCUIT DIAGRAM

FZJ111/FF31



LOGIC DIAGRAM



GENERAL DESCRIPTION

The FZJ101/FF30 consists of a single JK master-slave flip-flop with two J and K inputs and also has a slow-down capability on the slave of the flip-flop. So the reaction time of the slave to the negative-going clock-edge can be increased. This can be achieved by connecting external capacitors between the output terminals and their associated slow-down terminals.

The FZJ111/FF31 consists of a single JK master-slave flip-flop with two J inputs and one K input and has a slow-down capability both on the master and the slave of the flip-flop. For slowing down the slave see FZJ101/FF30.

The reaction time of the master to the positive-going clock-edge can be increased by connecting external capacitors between the slow-down terminals C_1, C_3 and C_2, C_4 respectively. Furthermore a minimum slope of the T-signal is required.

LOGIC FUNCTIONS

FZJ101/FF30

$J = J_1 \cdot J_2$

$K = K_1 \cdot K_2$

FZJ111/FF31

$J = J_1 \cdot J_2$

$K = K$

Function tables

t_n		t_{n+1}	
J	K	Q_1	Q_2
L	L	Q_{1n}	Q_{2n}
L	H	L	H
H	L	H	L
H	H	Q_{2n}	Q_{1n}
Q_2 is opposite Q_1			

The set inputs S_1 and S_2 override all the other inputs.

S_1	S_2	Q_1	Q_2
L	H	H	L
H	L	L	H
H	H	Q_1	Q_2 [1]
L	L	H	H [2]

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

1) Q_2 is opposite Q_1

2) If S_1 and S_2 return to HIGH simultaneously the Q-states will be indeterminate.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	12	V
Input voltage	V_J, V_K, V_T	max.	18	V
Input current at V_P = 17 V	$-I_{IL}$	max.	25	mA [1]
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C

1) All inputs except slow-down inputs.

NOTE

The slow-down terminals indicated by crosses are for slow-down purposes only; they are not to be connected to any other terminal.

RATINGS (continued)

Output short-circuit duration	t_{Qsc}	max.	1	s [1]
Slow-down input voltage	$+V_{CQ}$	max.	0;6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	V
	$-I_{CQ}$	max.	10,0	V

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Average propagation delay time at V_{pd} = 4,5 V				
T ⟶ Q: at range I ; V_P = 12 V	t_{pd}	max.	645	ns
at range II; V_P = 15 V	t_{pd}	typ.	400	ns
S ⟶ Q: at range I ; V_P = 12 V	t_{pd}	max.	455	ns
at range II; V_P = 15 V	t_{pd}	typ.	265	ns
Maximum clock rate at T_{amb} = 25 °C duty cycle 50%; range I/II	f_c	typ.	0,5	MHz
		min.	0,2	MHz
Supply current at range I : V_P = 12 V	I_P	typ.	8	mA
range II : V_P = 15 V	I_P	typ.	11	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1] Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references
Static data						
Voltages						
Input HIGH: J, K, T, S	V_{IH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW: J, K, S	V_{IL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$=0, 1mA
T	V_{TL}	–	–	4,0 V		
Output HIGH	V_{QH}	10	11,3	– V	11,4 and 13,5	V_{IL} = 4,5 V; $-I_{QH}$=0, 1mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{IH} = 7,5 V; I_{QL} =15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents						
Input HIGH: J, K, S	I_{IH}	–	–	1 µA	13,5	V_{IH} = 13,5 V (other inputs 0V)
T	I_{TH}	–	–	3 µA		
Input LOW: J, K	$-I_{IL}$	–	0,8	1,5 mA	13,5	$V_{JL}=V_{KL}=1,7$V
T	$-I_{TL}$	–	1,6	3,0 mA	13,5	V_{TL} = 1,7 V
S [2]	$-I_{SL}$	–	0,8	1,5 mA	13,5	V_{SL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	– mA	11,4 and 13,5	V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{QL} = 1,7 V
Output short-circuited [3]	$-I_{Qsc}$	10	30	50 mA	13,5	V_I=0V; V_Q=0V
Supply data						
Supply current	I_P	–	8,0	– mA	13,5	

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
2) For dynamic: $-I_{SL}$ = 1,5 x specified values.
3) Short-circuited duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T → Q						
fall time	t_{pdf}	270	450	770	ns	C_L = 10 pF
rise time	t_{pdr}	160	290	520	ns	
S → Q						N = 1
fall time	t_{pdf}	180	330	580	ns	
rise time	t_{pdr}	70	165	330	ns	T_{amb} = 25 °C
output rise time	t_r	200	340	570	ns	
output fall time	t_f	70	120	210	ns	V_{pd} = 4,5 V
Clock rate						
(duty cycle 50%)	f_c	0,2	0,5	–	MHz	
Input times						
T input	t_{TH}	0,6	–	–	µs	
	t_{TL}	0,6	–	–	µs	
S input	t_{SL}	1,0	–	–	µs	
J or K input						
hold time	t_{hold}	0	–	–	ns	
set-up time	t_{su}	0	–	–	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH: J, K, T, S	V_{IH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW: J, K, S	V_{IL}	–	–	4,5	V	13,5 and 17	$V_{QH} \leq 12$ V; $-I_{QH}$ = 0,1 mA
T	V_{TL}	–	–	4,0	V		
Output HIGH	V_{QH}	12	14,3	–	V	13,5 and 17	V_{IL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{IH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents							
Input HIGH: J, K, S	I_{IH}	–	–	1,0	μA	17	V_{IH} = 17 V; (other inputs 0 V)
T	I_{TH}	–	–	3,0	μA		
Input LOW: J, K	$-I_{IL}$	–	1,0	1,8	mA	17	V_{JL} = V_{KL} = 1,7 V
T	$-I_{TL}$	–	2,0	3,6	mA	17	V_{TL} = 1,7 V
S [2]	$-I_{SL}$	–	1,0	1,8	mA	17	V_{SL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5 and 17	V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$[3]	15	37	60	mA	17	V_I = 0 V; V_Q = 0 V
Supply data							
Supply current	I_P	–	11	–	mA	17	

[1] All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
[2] For dynamic: $-I_{SL}$ = 1,5 x specified values.
[3] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

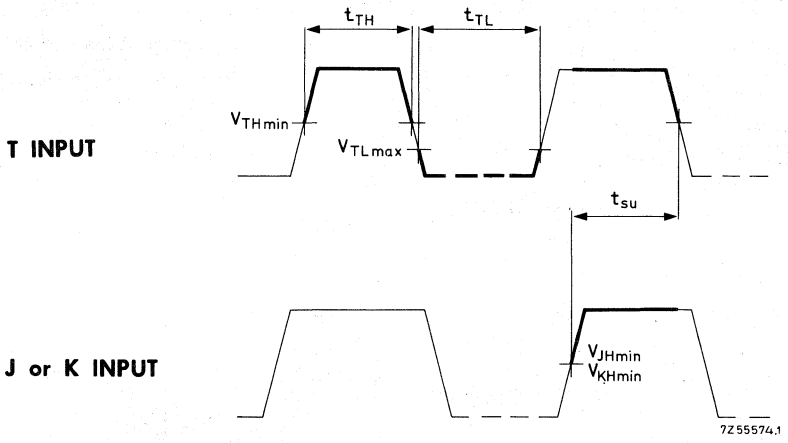
Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T ⟶ Q						
fall time	t_{pdf}	–	470	–	ns	
rise time	t_{pdr}	–	330	–	ns	
S ⟶ Q						
fall time	t_{pdf}	–	340	–	ns	
rise time	t_{pdr}	–	195	–	ns	
output rise time	t_r	–	410	–	ns	
output fall time	t_f	–	75	–	ns	C_L = 10 pF
Clock rate						N = 1
(duty cycle 50%)	f_c	–	0,5	–	MHz	T_{amb} = 25 °C
Input times						V_{pd} = 4,5 V
T input	t_{TH}	0,6	–	–	µs	
	t_{TL}	0,6	–	–	µs	
S input	t_{SL}	1,0	–	–	µs	
J or K input						
hold time	t_{hold}	0	–	–	µs	
set-up time	t_{su}	0	–	–	µs	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

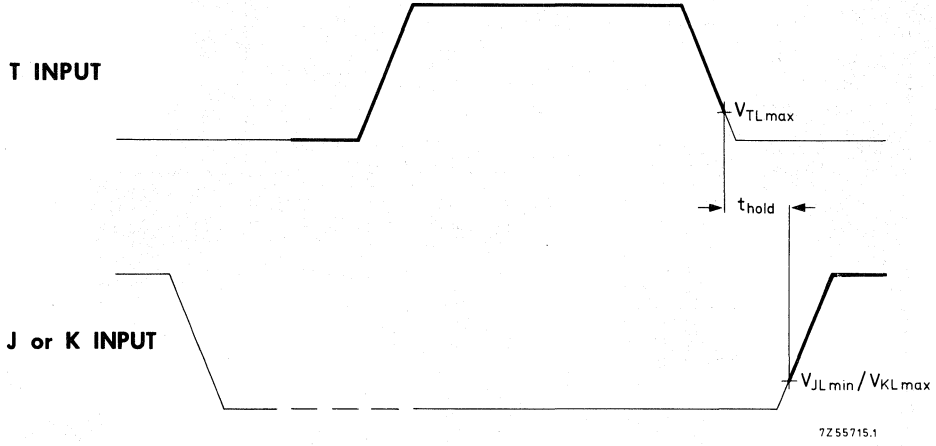
[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Dynamic data



Waveforms illustrating conditions for change of state



Waveforms illustrating conditions for no change of state

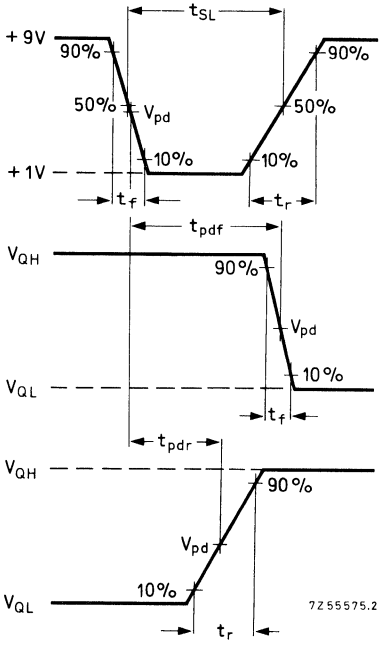
CHARACTERISTICS (continued)

Dynamic data

$S_2(S_1)$ INPUT

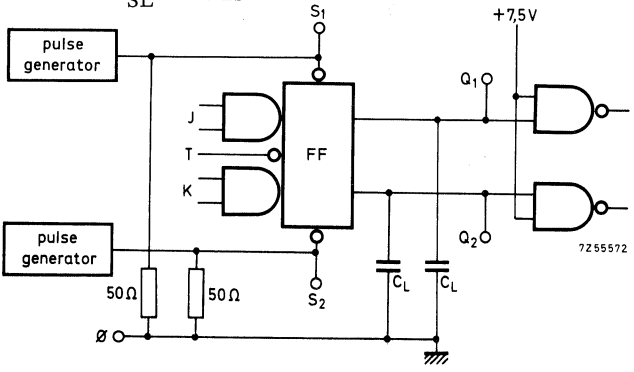
$Q_1(Q_2)$ OUTPUT

$Q_2(Q_1)$ OUTPUT



Pulse generator (S-input): t_r = 350 ns
t_f = 120 ns
t_{SL} = 700 ns

V_{pd} = +4,5 V

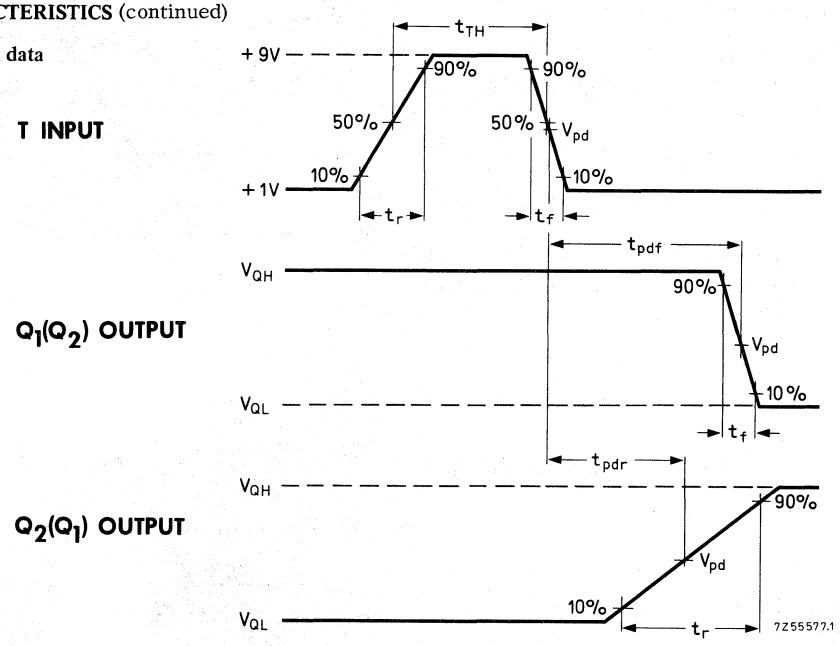


Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected
All other inputs are floating.

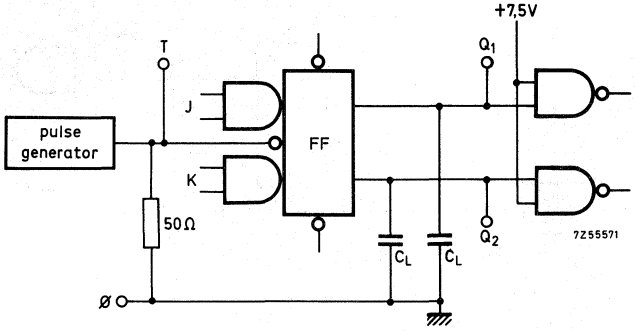
Waveforms illustrating conditions for set inputs. Set input signals are not supplied simultaneously.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (T-input): t_r = 350 ns V_{pd} = +4, 5 V
t_f = 120 ns
t_{TH} = 400 ns

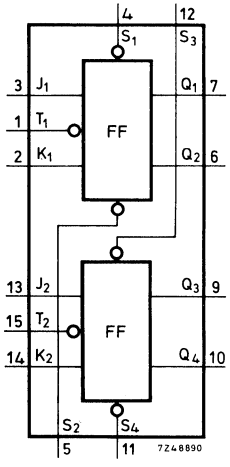


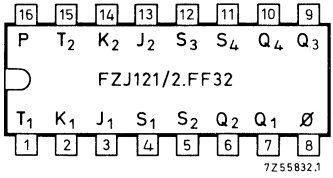
Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
Slow-down terminals are not connected
All other inputs are floating.

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL JK MASTER-SLAVE FLIP-FLOP





QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
Operating frequency at T_{amb} = 25 °C duty cycle 50%: range I/II	f_c	typ.	0,5	MHz
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	15	mA
V_P = 17 V	I_{Pav}	typ.	20	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V

PACKAGE OUTLINE 16-lead plastic dual in-line (see general section).

GENERAL DESCRIPTION

The FZJ121/2.FF32 comprises two independent JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, e.g. rise and fall times of all input signals including the trigger signals are immaterial.
The set and reset inputs (overriding any other input) are active at LOW level. There are no slow-down terminals.
Typical applications include counters and shift registers.

FUNCTION TABLES

t_n		t_{n+1}
J_1 J_2	K_1 K_2	Q_1 Q_3
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q_n}$
Q_2 is opposite Q_1 Q_4 is opposite Q_3		

S_1 S_3	S_2 S_4	Q_1 Q_3	Q_2 Q_4
L	H	H	L
H	L	L	H
H	H	$Q_1(Q_3)$	$Q_2(Q_4)$ 1)
L	L	X	X 2)

1) $Q_2(Q_4)$ is opposite $Q_1(Q_3)$
2) If S_1 (S_3) and S_2 (S_4) return to HIGH simultaneously the Q-states will be indeterminate.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_J, V_K, V_T	max.	18	V
Input current at V_P = 17 V	$-I_{IL}$	max.	25	mA
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1	s 1)

1) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0	to	+70	°C
Uniform system supply voltage (range I)	V_P	11,4	to	13,5	V
(range II)	V_P	13,5	to	17	V
Available d.c. fan-out	N_{aL}	max.		10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		2,5	V
range II at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		4,5	V
Supply current at range I : V_P = 12 V	I_P	typ.		15	mA
range II : V_P = 15 V	I_P	typ.		20	mA
Thermal resistance from system to ambient	R_{th}	max.		150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH: T	V_{TH}	6,5	-	-	V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
J; K	V_{IH}	8,0	-	-	V	11,4	
S	V_{SH}	7,5	-	-	V	11,4	
Input LOW: T	V_{TL}	-	-	4,0	V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
J; K	V_{IL}	-	-	5,5	V		
S	V_{SL}	-	-	4,5	V		
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$V_{IL} \leq 4,5$ V [2]; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	$V_{IH} \geq 7,5$ V [2]; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4	
LOW	M_L	2,8	5,0	-	V	11,4	
Currents							
Input HIGH: T	I_{TH}	-	-	3	μA	13,5	V_{IH} = 13,5 V (other inputs 0V)
J; K; S	I_{IH}	-	-	1	μA		
Input LOW: T	$-I_{TL}$	-	1,6	3,0	mA	13,5	V_{IL} = 1,7 V
J; K; S [3]	$-I_{IL}$	-	0,8	1,5	mA	13,5	V_{IL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	V_{QH} = 10 V
Output LOW	I_{QL}	15	-	-	mA	11,4	V_{QL} = 1,7 V
Supply data							
Supply current	I_P	-	15	24	mA	13,5	

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
2) Measured to S_2 and S_1.
3) For dynamic: $-I_{SL}$ = 1,5 x specified values.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T ⟶ Q						
fall time	t_{pdf}	270	450	770	ns	
rise time	t_{pdr}	160	290	520	ns	
R or S ⟶ Q						
fall time	t_{pdf}	180	330	580	ns	
rise time	t_{pdr}	70	165	330	ns	
output fall time	t_f	70	120	210	ns	
output rise time	t_r	200	340	570	ns	C_L = 10 pF
Clock rate						N = 1
(duty cycle 50%)	f_c	0,2	0,5	–	MHz	T_{amb} = 25 °C
Input times						V_{pd} = 4,5 V
T input	t_{TH}	0,6	–	–	µs	
R input	t_{RL}	1,0	–	–	µs	
S input	t_{SL}	1,0	–	–	µs	
J or K input						
hold time	t_{hold}	0	–	–	ns	
set-up time	t_{su}	0	–	–	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH: T	V_{TH}	6,5	-	-	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
J; K	V_{IH}	8,0	-	-	V	13,5	
S	V_{SH}	7,5	-	-	V	13,5	
Input LOW: T	V_{TL}	-	-	4,0	V	11,4 and 13,5	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
J; K	V_{IL}	-	-	5,5	V		
S	V_{SL}	-	-	4,5	V		
Output HIGH	V_{QH}	12,0	14,3	-	V	11,4 and 13,5	$V_{IL} \leq 4,5$ V [2]; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	-	1,1	1,7	V	13,5	$V_{IH} \geq 7,5$ V [2]; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5	
LOW	M_L	2,8	5,0	-	V	13,5	
Currents							
Input HIGH: T	I_{TH}	-	-	3,0	µA	17	V_{IH} = 17 V (other inputs 0V)
J; K; S	I_{IH}	-	-	1,0	µA		
Input LOW: T	$-I_{TL}$	-	2,0	3,6	mA	17	V_{IL} = 1,7 V
J; K; S [3]	$-I_{IL}$	-	1,0	1,8	mA	17	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	V_{QH} = 12 V
Output LOW	I_{QL}	18	-	-	mA	13,5	V_{QL} = 1,7 V
Supply data							
Supply current	I_P	-	20	32	mA	17	

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.
2) Measured to S_2 and S_1.
3) For dynamic: $-I_{SL}$ = 1,5 x specified values.

CHARACTERISTICS (continued)

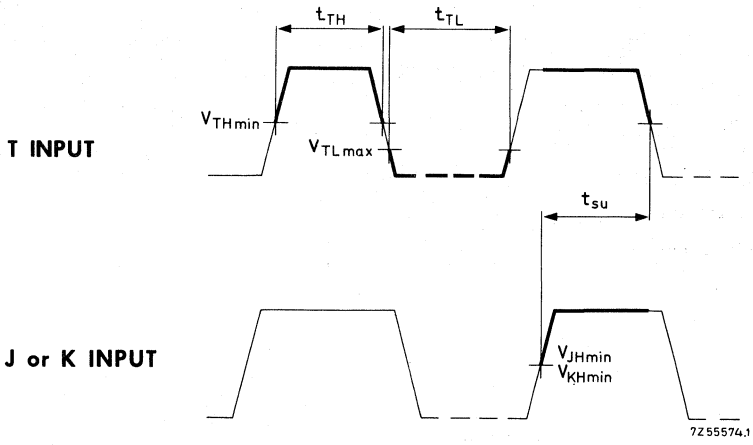
Test conditions at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T ⟶ Q						
fall time	t_{pdf}	–	470	–	ns	C_L = 10 pF
rise time	t_{pdr}	–	330	–	ns	N = 1
R or S ⟶ Q						T_{amb} = 25 °C
fall time	t_{pdf}	–	340	–	ns	V_{pd} = 4,5 V
rise time	t_{pdr}	–	195	–	ns	
output fall time	t_f	–	75	–	ns	
output rise time	t_r	–	410	–	ns	
Clock rate						
(duty cycle 50%)	f_c	0,2	0,5	–	MHz	
Input times						
T input	t_{TH}	0,6	–	–	µs	
R input	t_{RL}	0,6	–	–	µs	
S input	t_{SL}	1,0	–	–	µs	
J or K input						
hold time	t_{hold}	0	–	–	ns	
set-up time	t_{su}	0	–	–	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

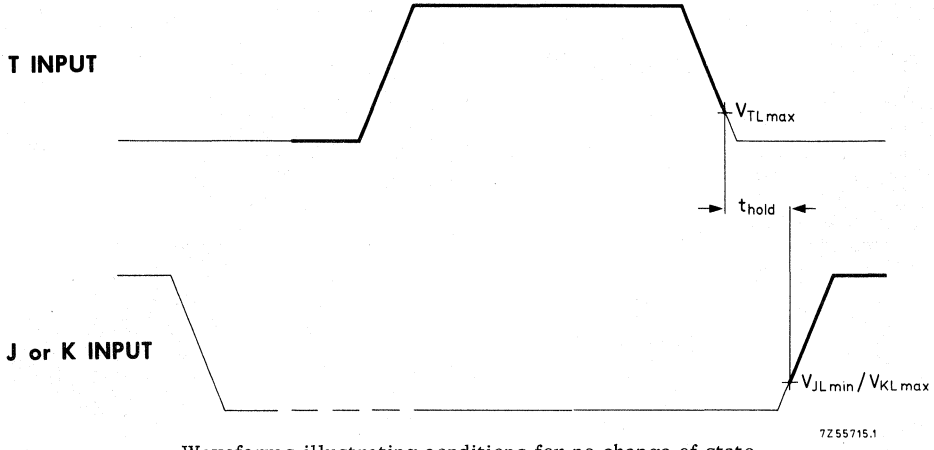
[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Dynamic data



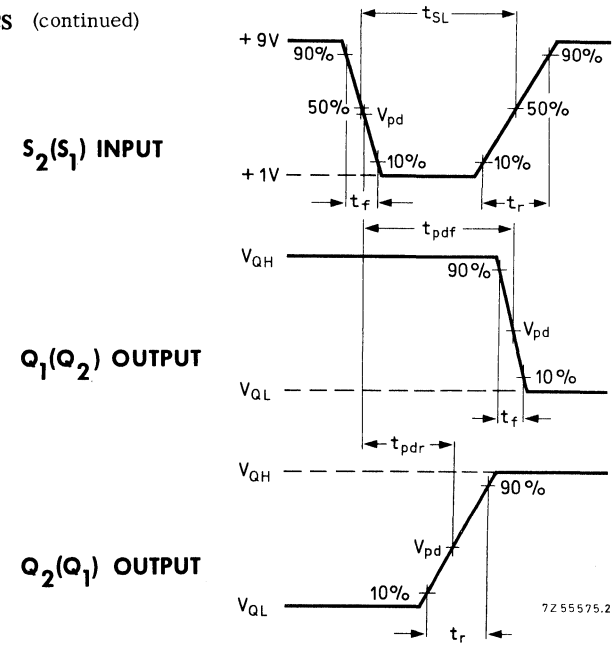
Waveforms illustrating conditions for change of state



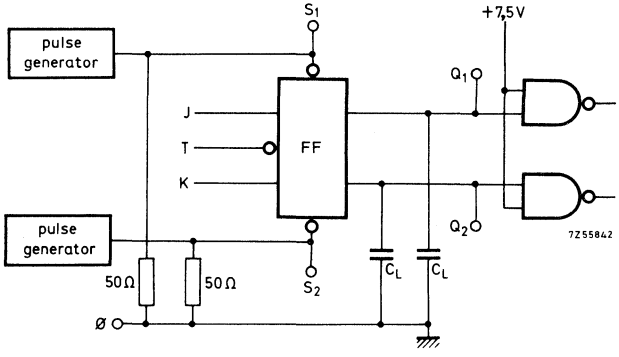
Waveforms illustrating conditions for no change of state

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (S-input): t_r = 350 ns; t_f = 120 ns; t_{SL} = 700 ns; V_{pd} = +4,5 V

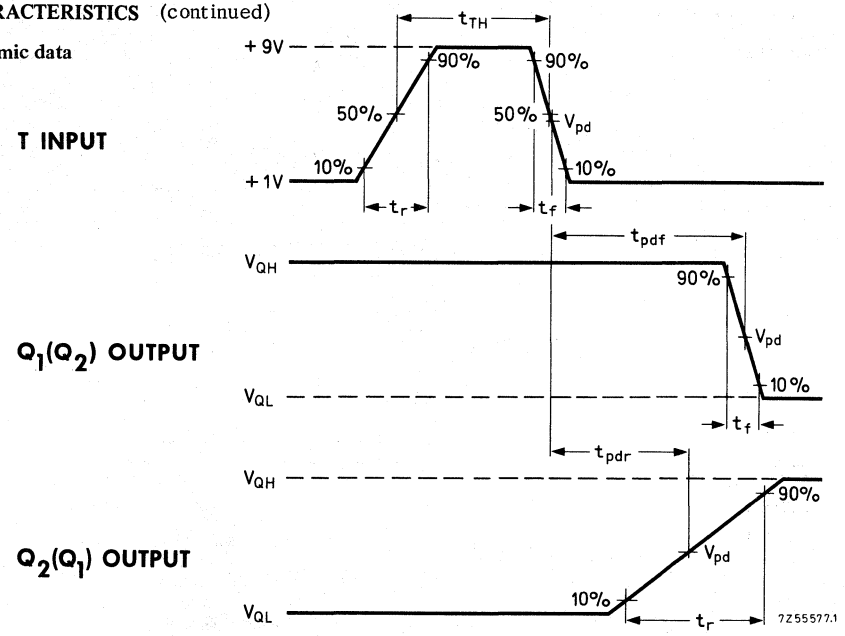


Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
All other inputs are floating.

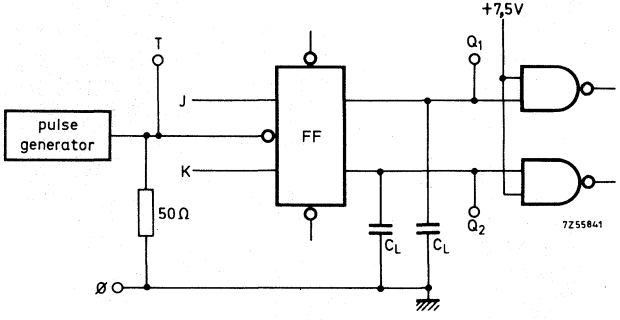
Waveforms illustrating conditions for set inputs. Set input signals are not supplied simultaneously.

CHARACTERISTICS (continued)

Dynamic data



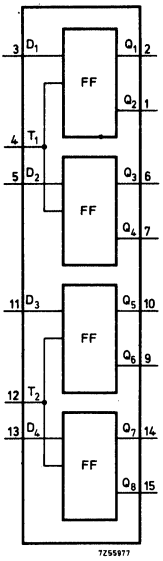
Pulse generator (T-input): t_r = 350 ns; t_f = 120 ns; t_{TH} = 400 ns; V_{pd} = +4,5 V



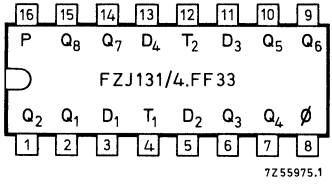
Measuring conditions: V_P = +12 V; +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = 25 °C
All other inputs are floating.

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.



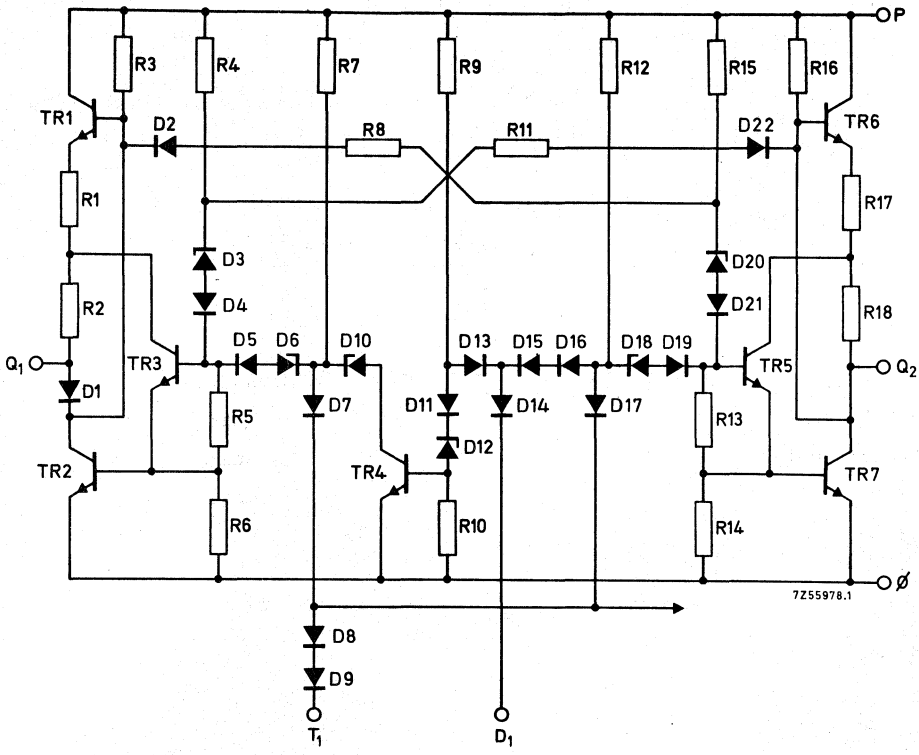
QUADRUPLE D-TYPE LATCH FLIP-FLOP



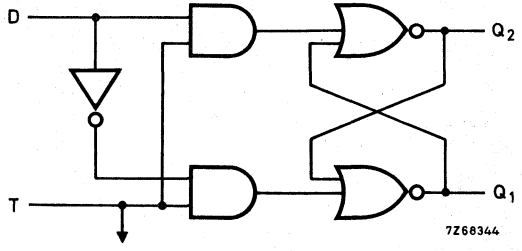
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	22	mA
V_P = 17 V	I_{Pav}	typ.	28	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Average power consumption				
(50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	264	mW
range II : V_P = 15 V	P_{av}	typ.	420	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTIONS

The FZJ131/4.FF33 comprises four D-type latch flip-flops. Information present at a data input D, is transferred to Q as long as T is HIGH.
When T is LOW, D does not affect Q.

Function table

input		output
T	D (t_n)	Q ($t_n + 1$)
L	L	Q_n
L	H	Q_n
H	L	L
H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

t_n = bit-time before trigger pulse
t_{n+1} = bit-time after trigger pulse

RATING Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_D, V_T	max.	18	V
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Power consumption (50% duty cycle) at range I : V_{Pmax}	P_{av}	max.	432	mW
at range II : V_{Pmax}	P_{av}	max.	720	mW
Supply surrent at range I : V_P = 12 V	I_P	max.	32	mA
range II : V_P = 15 V	I_P	max.	42	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

1) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH: D, T	V_{IH}	7,5	–	–	V		
Input LOW: D, T	V_{IL}	–	–	4,5	V		
Output HIGH	V_{QH}	10	11,3	–	V	11,4	V_I = 7,5 V $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{TH} = 7,5 V V_{DL} = 4,5 V I_{QL} = 15 mA
D.C. noise margin							
HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents							
Input HIGH: D, T	I_{IH}	–	–	1	µA	13,5	V_{IH} = 13,5 V other inputs 0 V
Input LOW: D	$-I_{DL}$	–	–	3	mA	13,5	V_{DL} = 1,7 V
T	$-I_{TL}$	–	–	6	mA	13,5	V_{TL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4	V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	13,5	V_I = 0; V_Q = 0
Supply data							
Supply current	I_P	–	22	32	mA	13,5	V_I = 0

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		conditions and references
Dynamic data						
Times						
Propagation delay:						
$T_1 \longrightarrow Q_1$						
fall time	t_{pdf}	70	120	210	ns	
rise time	t_{pdr}	90	160	310	ns	
$T_1 \longrightarrow Q_2$						
fall time	t_{pdf}	70	120	210	ns	
rise time	t_{pdr}	90	150	310	ns	
$D_1 \longrightarrow Q_1$						
fall time	t_{pdf}	30	70	150	ns	
rise time	t_{pdr}	90	175	310	ns	
$D_1 \longrightarrow Q_2$						
fall time	t_{pdf}	70	130	290	ns	
rise time	t_{pdr}	30	70	150	ns	C_L = 10 pF; N = 1; T_{amb} = 25 °C; V_{pd} = 4,5 V
output fall time	t_f	15	35	60	ns	
output rise time	t_r	50	90	170	ns	
Clock rate (duty cycle 50%)	f_c	0,5	-	-	MHz	
D input						
hold time	t_{holdH}	150	-	-	ns	
	t_{holdL}	50	-	-	ns	
set-up time	t_{suH}	300	-	-	ns	
	t_{suL}	500	-	-	ns	
T input	$(-dV/dt)_{Tmin}$			1	V/µs	

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH: D, T	V_{IH}	7,5	–	–	V		
Input LOW: D, T	V_{IL}	–	–	4,5	V		
Output HIGH	V_{QH}	12	14,3	–	V	13,5	V_I = 7,5 V $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{TH} = 7,5 V V_{DL} = 4,5 V I_{QL} = 18 mA
D.C. noise margin							
HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents							
Input HIGH: D, T	I_{IH}	–	–	1,0	µA	17	V_{IH} = 17 V (other inputs 0 V)
Input LOW: D	$-I_{DL}$	–	–	3,6	mA	17	V_{DL} = 1,7 V
T	$-I_{TL}$	–	–	7,2	mA	17	V_{TL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5	V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	17	V_I = 0; V_Q = 0
Supply data							
Supply current	I_P	-	28	42	mA	17	V_I = 0

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

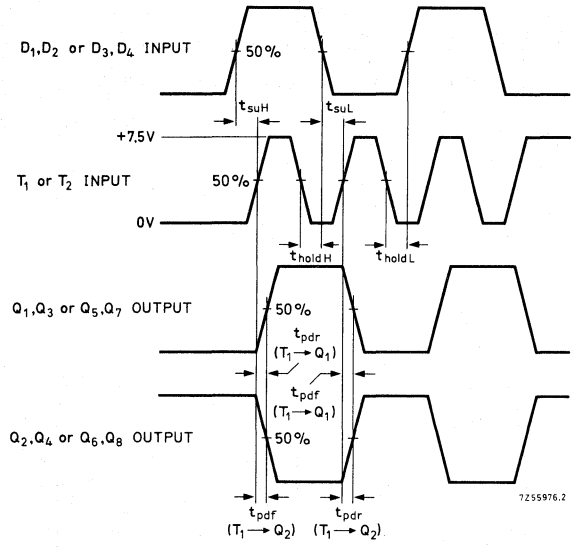
Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

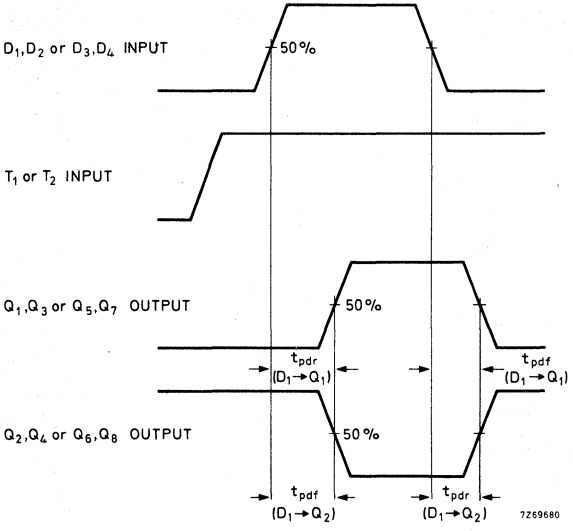
	Symbol	min.	typ. [1]	max	conditions and references
Dynamic data					
Times					
Propagation delay:					
$T_1 \longrightarrow Q_1$					
fall time	t_{pdf}				
rise time	t_{pdr}				
$T_1 \longrightarrow Q_2$					
fall time	t_{pdf}				
rise time	t_{pdr}				
$D_1 \longrightarrow Q_1$					
fall time	t_{pdf}				
rise time	t_{pdr}				
$D_1 \longrightarrow Q_2$					C_L = 10 pF N = 1 T_{amb} = 25 °C V_{pd} = 4,5 V
fall time	t_{pdf}				
rise time	t_{pdr}		t.b.f.		
output fall time	t_f				
output rise time	t_r				
Clock rate (duty cycle 50%)	f_c				
D input hold time					
set-up time					
T input slope	$(-dV/dt)_{Tmin}$	-	-	1 V/µs	

[1]) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Dynamic data

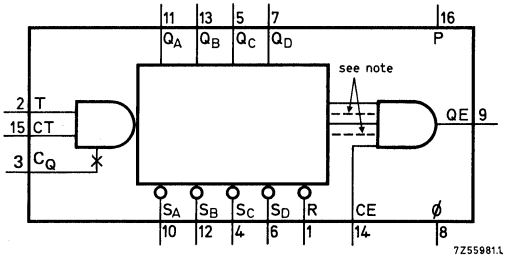


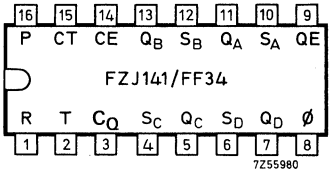


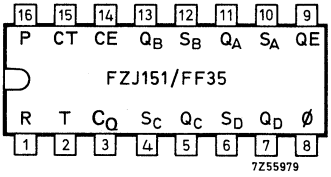
Waveforms illustrating measurement of t_{pdr} and t_{pdf} (T → Q); (D → Q)

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SINGLE SYNCHRONOUS DECIMAL COUNTER
SINGLE SYNCHRONOUS 4-BIT BINARY COUNTER







Note

FZJ141/FF34: without connections indicated by dotted line
FZJ151/FF35: with connections indicated by dotted line

QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
Operating frequency at T_{amb} = 25 °C duty cycle 50%: range I/II	f_c	max.	1,5	MHz
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V at V_{QL}	I_{Pav}	typ.	20	mA
V_P = 17 V at V_{QL}	I_{Pav}	typ.	23	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

GENERAL DESCRIPTION

The FZJ141/FF34 and FZJ151/FF35 are synchronous counters consisting of 4 master-slave flip-flops.
The FZJ141/FF34 is a decimal counter with common T and R input and a set (S) input for each bit. The condition input (CE) and output (QE) are for coupling these circuits.
The FZJ151/FF35 is a 4-bit binary counter with a common T and R input and a set input per bit. The direct reset inhibits the count and simultaneously all flip-flops return to LOW. The output information of each flip-flop of both circuits changes when T goes from HIGH to LOW.

LOGIC FUNCTIONS

Count condition: $S_A = S_B = S_C = S_D = CT = CE = R = HIGH$

FZJ141/FF34

count	outputs				
	Q_A	Q_B	Q_C	Q_D	QE
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	H

FZJ151/FF35

count	outputs				
	Q_A	Q_B	Q_C	Q_D	QE
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	H

Pin description

CT = condition enable trigger at input T
CE = condition enable for output QE
QE = output enable

Set and reset conditions

inputs					outputs			
R	S_A	S_B	S_C	S_D	Q_A	Q_B	Q_C	Q_D
L	H	H	H	H	L	L	L	L
L	L	X	X	X	H	X	X	X
L	X	L	X	X	X	H	X	X
L	X	X	L	X	X	X	H	X
L	X	X	X	L	X	X	X	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

All set and reset inputs, when LOW, override the count input signal and set the flip-flops corresponding to the table at the left.
Set and reset terminals may not be left floating but must be connected to the supply voltage V_P.

LOGIC FUNCTIONS (continued)

Enable conditions

input CT	
L	no count
H	count

input CE	enable output QE
L	L
H	X *)

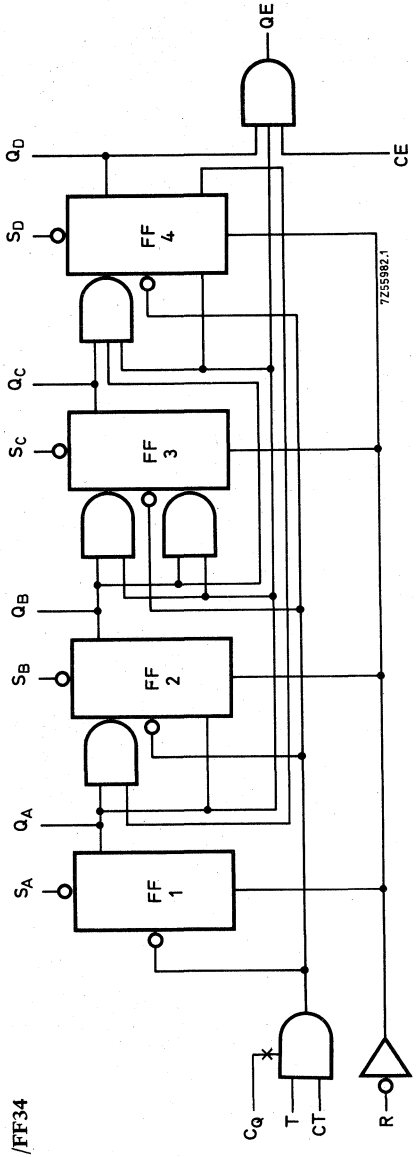
*) Depends on logic state of other inputs of the final gate.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

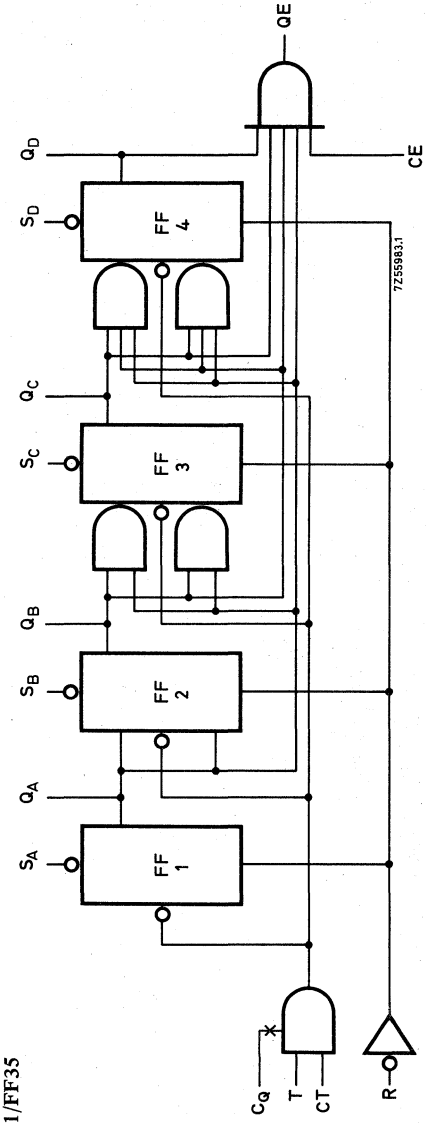
Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_I	max.	18	V
Input current at V_P = 17 V	$-I_{IL}$	max.	25	mA
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C

LOGIC DIAGRAMS

FZJ141/FF34



FZJ151/FF35



SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+70	°C
Uniform system supply voltage (range I)	V_P	11, 4 to	13, 5	V
(range II)	V_P	13, 5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2, 8	V
	M_H	min.	2, 5	V
range II at V_{Pmin}	M_L	min.	2, 8	V
	M_H	min.	4, 5	V
Clock rate at T_{amb} = 25 °C duty cycle 50%; range I/II	f_c	min.	0, 5	MHz
	f_c	typ.	1, 5	MHz
Supply current at range I : V_P = 12 V				
at V_{QH}	I_P	typ.	12	mA
at V_{QL}	I_P	typ.	20	mA
at range II : V_P = 15 V				
at V_{QH}	I_P	typ.	15	mA
at V_{QL}	I_P	typ.	23	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{IH}	7,5	–	–	V	11,4	
Input LOW	V_{IL}	–	–	4,5	V	13,5	
Output HIGH	V_{QH}	10	11,3	–	V	11,4	V_{IL} = 4,5 V $-I_Q$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7	V	11,4	V_{IH} = 7,5 V I_Q = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents							
Input HIGH	I_{IH}	–	–	1	µA	13,5	V_{IH} = 13,5 V
Input LOW	$-I_{IL}$	–	0,8	1,5	mA	13,5	V_{IL} = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	11,4 and 13,5	V_{QH} = 10 V
Output LOW	I_{QL}	15	–	–	mA	11,4	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	13,5	V_I = 0; V_Q = 0
Supply data							
Supply current at V_{QH}	I_P	–	12	–	mA	13,5	V_I = 13,5 V
at V_{QL}	I_P	–	20	–	mA	13,5	V_R = 0 V other inputs 13,5 V

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V)

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay: T → Q_A; Q_B; Q_C; Q_D						
fall time	t_{pdf}	90	200	450	ns	V_{pd} = 4,5 V; N = 1; C_L = 10 pF; T_{amb} = 25 °C
rise time	t_{pdr}	90	200	450	ns	
T → QE						
fall time	t_{pdf}	150	300	500	ns	
rise time	t_{pdr}	200	400	700	ns	
CE → QE						
fall time	t_{pdf}	25	60	200	ns	
rise time	t_{pdr}	90	200	450	ns	
R → Q_A; Q_B; Q_C; Q_D						
fall time	t_{pdf}	70	150	310	ns	
S_A → Q_A; S_B → Q_B; S_C → Q_C; S_D → Q_D						
rise time	t_{pdr}	30	120	210	ns	
Clock pulse duration	t_T	0,5	–	–	µs	V_{pd} = 4,5 V; N = 1
Clock rate	f_c	0,5	–	–	MHz	duty cycle 50%
Reset pulse duration	t_{RL}	0,5	–	–	µs	V_{pd} = 4,5 V; N = 1; T_{amb} = 25 °C
Reset recovery time (T input)	$t_{R\,rec}$	–	–	2	µs	
Reset pulse duration during set operation	t_{RLS}	1	–	–	µs	
Set inputs (S_A; S_B; S_C; S_D) set-up time	t_{su}	1	–	–	µs	
Set inputs (S_A; S_B; S_C; S_D) hold time	t_{hold}	1	–	–	µs	
Output fall time (at Q)	t_f	5	20	60	ns	
Output rise time (at Q)	t_r	90	250	450	ns	
Output fall time (at QE)	t_f	30	60	210	ns	
Output rise time (at QE)	t_r	70	140	310	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{IH}	7,5	–	–	V	13,5	
Input LOW	V_{IL}	–	–	4,5	V	17,0	
Output HIGH	V_{QH}	12	14,3	–	V	13,5	V_{IL} = 4,5 V $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1	1,7	V	13,5	V_{IH} = 7,5 V I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8	–	V	13,5	
LOW	M_L	2,8	5	–	V	13,5	
Currents							
Input HIGH	I_{IH}	–	–	1	µA	17,0	V_I = 17,0 V
Input LOW	$-I_{IL}$	–	1,0	1,8	mA	17,0	V_I = 1,7 V
Output HIGH	$-I_{QH}$	0,1	–	–	mA	13,5	V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	17,0	V_I = 0; V_Q = 0
Supply data							
Supply current at V_{QH}	I_P	–	15	23	mA	17,0	V_I = 17,0 V
at V_{QL}	I_P	–	23	36,5	mA	17,0	V_R = 0 V other inputs 17,0 V

1) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

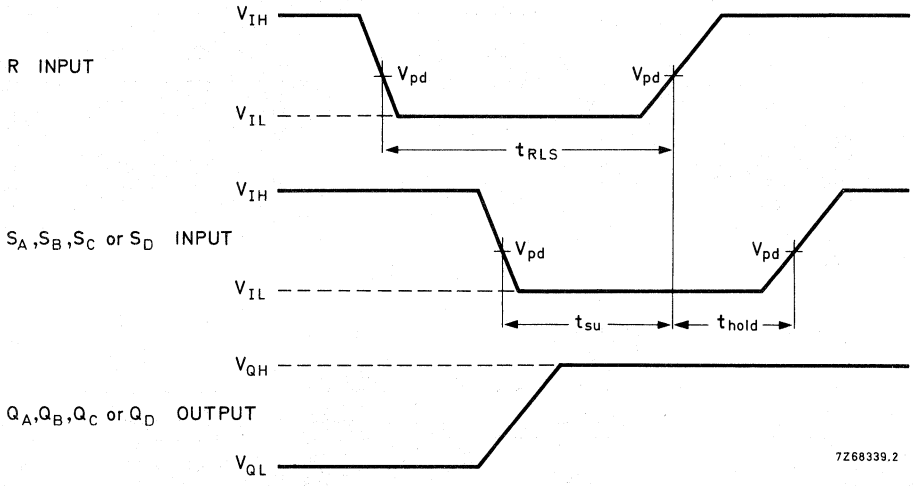
CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T → Q						
fall time	t_{pdf}				ns	C_L = 10 pF N = 1 T_{amb} = 25 °C V_{pd} = 4,5 V
rise time	t_{pdr}				ns	
T → QE						
fall time	t_{pdf}				ns	
rise time	t_{pdr}				ns	
C_E → QE						
fall time	t_{pdf}				ns	
rise time	t_{pdr}				ns	
R → Q						
fall time	t_{pdf}		t.b.f.		ns	
S_A → Q_A, S_B → Q_B						
rise time	t_{pdr}				ns	
S_C → Q_C, S_D → Q_D						
fall time	t_{pdf}				ns	
output fall time } at Q	t_f				ns	
output rise time } at Q	t_r				ns	
output fall time } at QE						
output rise time } at QE						
T input slope	$(-dV/dt)_{Tmin}$		1		V/µs	

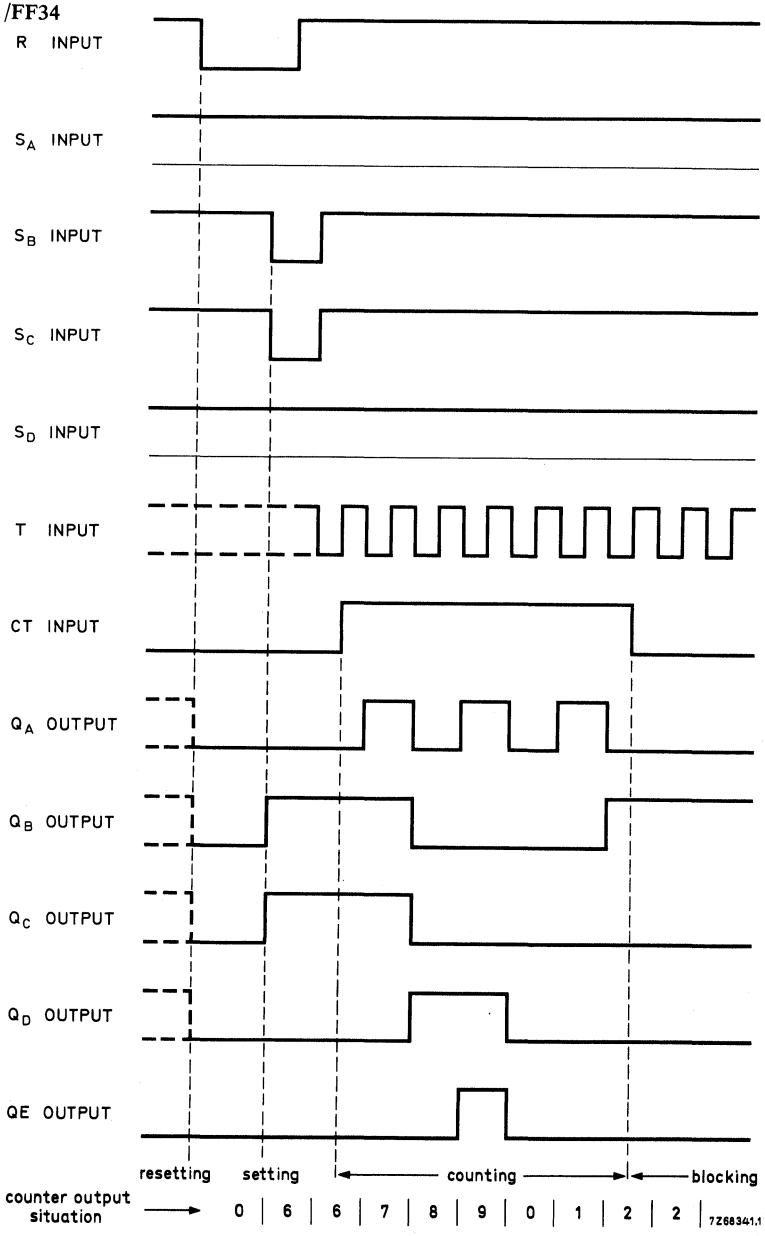
[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTIC (continued)



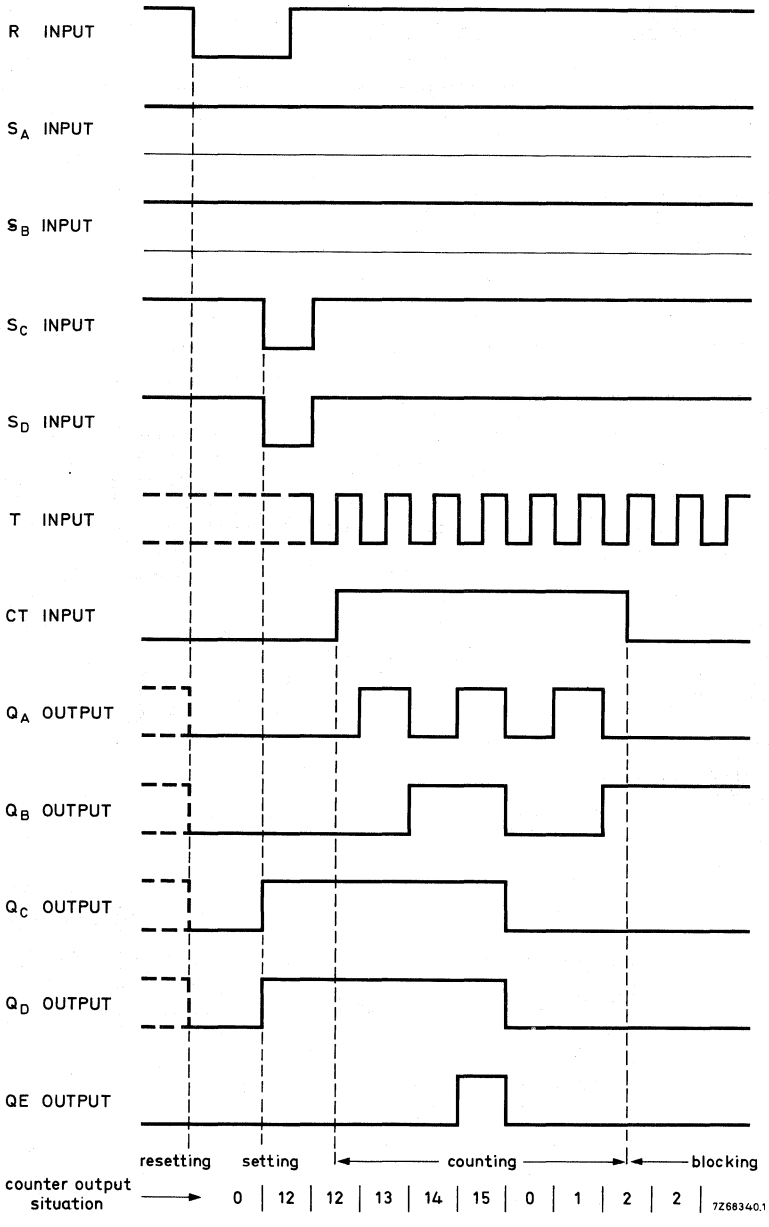
CHARACTERISTICS (continued)

FZJ141/FF34



CHARACTERISTICS (continued)

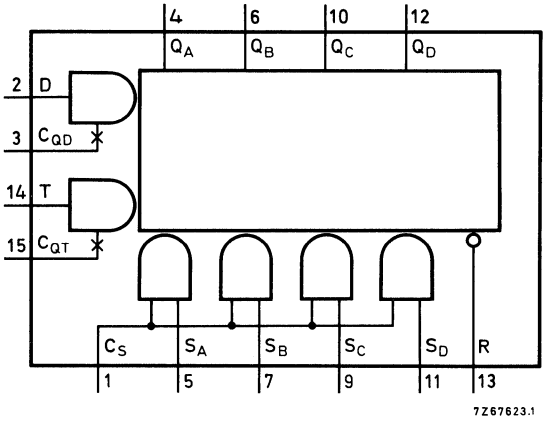
FZJ151/FF35

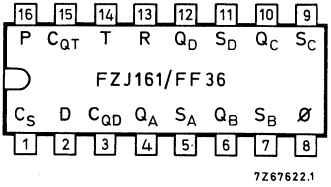


The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SINGLE SYNCHRONOUS 4-BIT SHIFT REGISTER

with slow-down capability





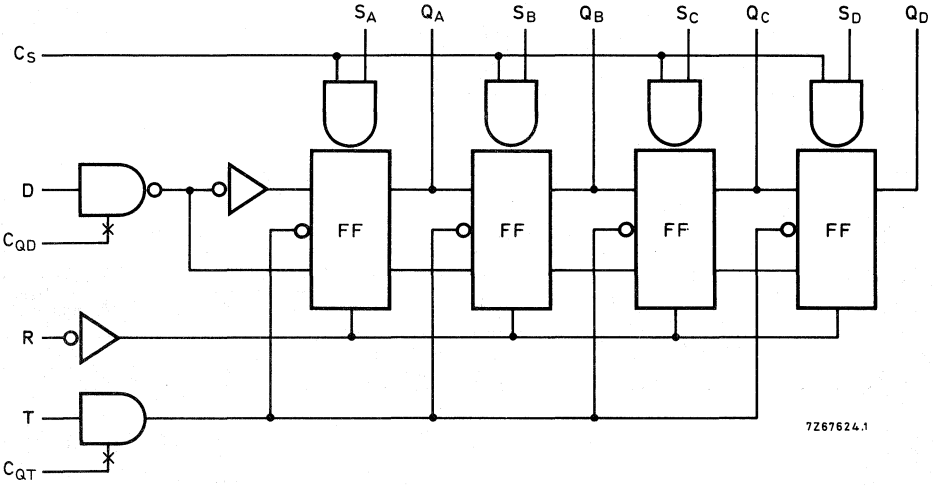
QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d.c. fan-out T_{amb} = 0 to +70 °C } LOW state	N_{aL}	max.	10	
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	21	mA
V_P = 17 V	I_{Pav}	typ.	26	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5	V
range II : V_P = 15 V	M_L	typ.	5	V
	M_H	typ.	8	V
Average power consumption				
(50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	180	mW
range II : V_P = 15 V	P_{av}	typ.	390	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

GENERAL DESCRIPTION

The FZJ161/FF36 consists of a synchronous 4-bit shift register with serial or parallel inputs and serial or parallel outputs.
It is used as serial to parallel or parallel to serial converter, register and memory.
The device has slow-down inputs (C_{QD} and C_{QT}).

LOGIC DIAGRAM



Pin description

C_S = condition set input
D = data input
C_{QD} = slow-down data input
R = reset input
T = trigger input
C_{QT} = slow-down trigger input
S = set input
Q = output

FUNCTION TABLE

inputs						outputs			
C_S	R	S_A	S_B	S_C	S_D	Q_A	Q_B	Q_C	Q_D
L	L	X	X	X	X	L	L	L	L
H	L	H	L	H	H	H	L	H	H
L	H	X	X	X	X	shift			

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_I	max.	18	V
Input current at V_P = 17 V	$-I_{IL}$	max.	25	mA
Storage temperature	T_{stg}	−65 to	+150	°C
Operating ambient temperature	T_{amb}	0 to	+70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s [1]

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to	+70	°C
Uniform system supply voltage (range I)	V_P	11,4 to	13,5	V
(range II)	V_P	13,5 to	17	V
Available d.c. fan-out	N_{aL}	max.	10	
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Power consumption (50% duty cycle) at range I : V_{Pmax}	P_{av}	max.	340	mW
at range II : V_{Pmax}	P_{av}	max.	715	mW
Supply current at range I : V_P = 12 V	I_P	max.	33	mA
range II : V_P = 15 V	I_P	max.	42	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

[1] Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references: V_P (V)	Conditions and references:
Static data						
Voltages						
Input HIGH	V_{IH}	7,5	–	– V	11,4	
Input LOW	V_{IL}	–	–	4,5 V	11,4 and 13,5	
Output HIGH	V_{QH}	10	11,3	– V	11,4	V_{IL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{IH} = 7,5 V; I_{QL} = 15 mA
D.C. noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents						
Input HIGH	I_{IH}	–	–	1 µA	13,5	V_{IH} = 13,5 V
Input LOW						
C_S-input	$-I_{CSL}$	–	–	6 mA	13,5	V_{IL} = 1,7 V
other inputs	$-I_{IL}$	–	–	1,5 mA	13,5	V_{IL} = 1,7 V
Output short-circuited [2]	$-I_{Qsc}$	9	15	25 mA	13,5	V_I = 0; V_Q = 0
Supply data						
Supply current	I_P	–	21	33 mA	13,5	V_I = 0

1) All typ. values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C.

	Symbol	min.	typ. [1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T → Q						
fall time	t_{pdf}	90	140	450	ns	
rise time	t_{pdr}	90	140	450	ns	
R → Q						
fall time	t_{pdf}	0,6	0,85	1,3	µs	V_{pd} = 4,5 V
$C_S \rightarrow Q$, $S_A \rightarrow Q_A$, $S_B \rightarrow Q_B$, $S_C \rightarrow Q_C$, $S_D \rightarrow Q_D$						N = 1
fall time	t_{pdf}	90	140	450	ns	C_L = 10 pF
rise time	t_{pdr}	100	240	500	ns	T_{amb} = 25 °C
output fall time	t_f	5	20	60	ns	
output rise time	t_r	70	150	290	ns	
Clock pulse duration	t_T	0,5	–	–	µs	V_{pd} = 4,5 V; N = 1
Clock rate	f_c	0,5	1,5	–	MHz	duty cycle 50%
Reset pulse duration	t_{RL}	0,5	–	–	µs	
Reset pulse duration during set operation	t_{RLS}	1	–	–	µs	
Set-up times at						V_{pd} = 4,5 V
S_A; S_B; S_C; S_D; C_S	t_{su}	1	–	–	µs	N = 1
D	t_{su}	0	–	–	µs	T_{amb} = 25 °C
Hold times at						
S_A; S_B; S_C; S_D; C_S	t_{hold}	1	–	–	µs	
D	t_{hold}	0,5	–	–	µs	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{IH}	7,5	–	–	V	13,5	
Input LOW	V_{IL}	–	–	4,5	V	13,5 and 17,0	
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5	V_{IL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{IH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents							
Input HIGH	I_{IH}	–	–	1	µA	17,0	V_I = 17,0 V
Input LOW							
C_S-input	$-I_{CSL}$	–	–	7,2	mA	17,0	V_I = 1,7 V
other inputs	$-I_{IL}$	–	–	1,8	mA	17,0	V_I = 1,7 V
Output short-circuited [2]	I_{Qsc}	9	15	25	mA	17,0	V_I = 0; V_Q = 0
Supply data							
Supply current	I_P	–	26	42	mA	17,0	V_I = 0

[1] All typ. values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

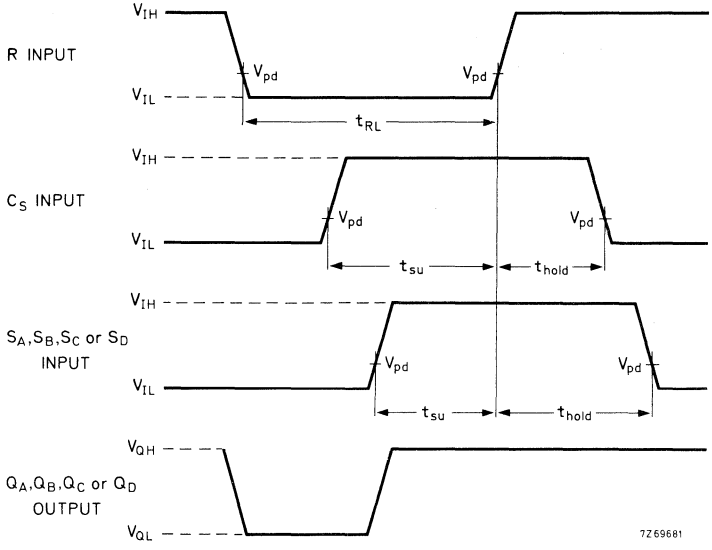
[2] Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
T → Q						
fall time	t_{pdf}				ns	C_L = 10 pF N = 1 T_{amb} = 25 °C V_{pd} = 4,5 V
rise time	t_{pdr}				ns	
R → Q						
fall time	t_{pdf}				µs	
C_S → Q, S_A → Q_A, S_B → Q_B, S_C → Q_C, S_D → Q_D			t.b.f.			
rise time	t_{pdr}				ns	
fall time	t_{pdf}				ns	
output fall time	t_f				ns	
output rise time	t_r				ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

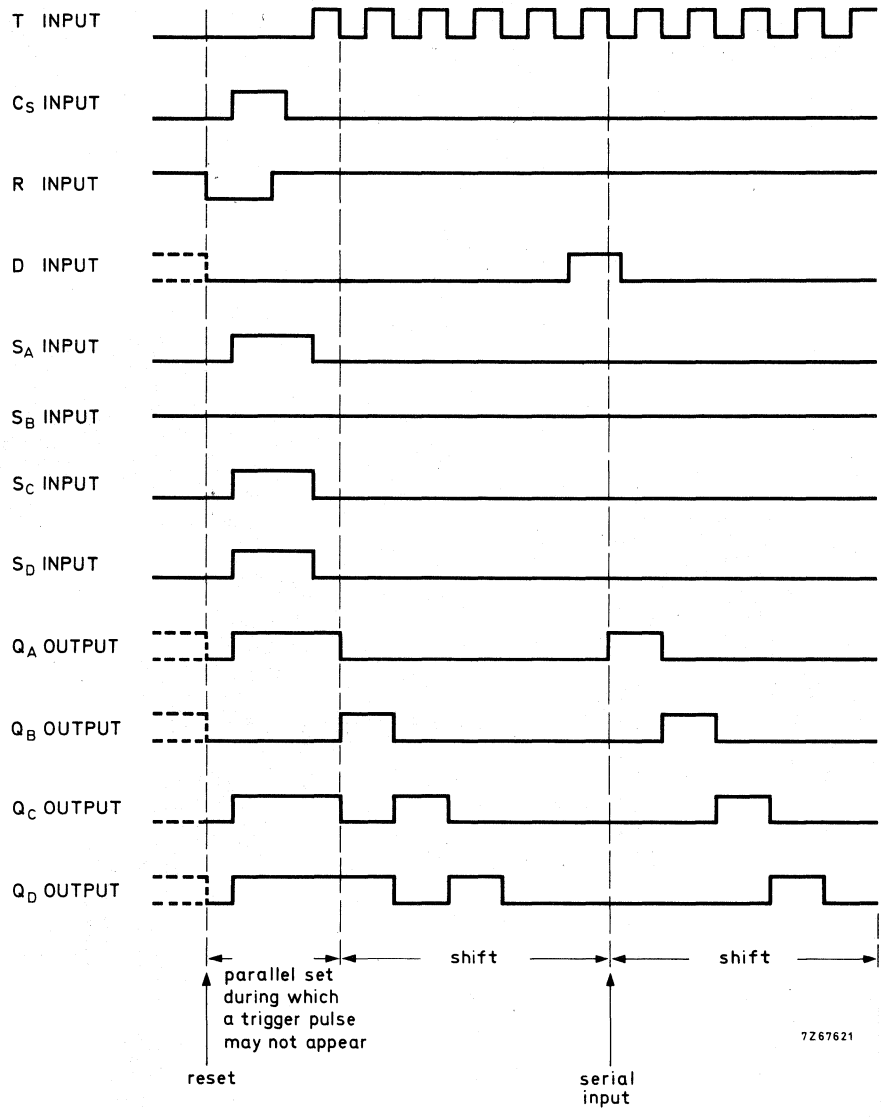
Waveforms for set operation



[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

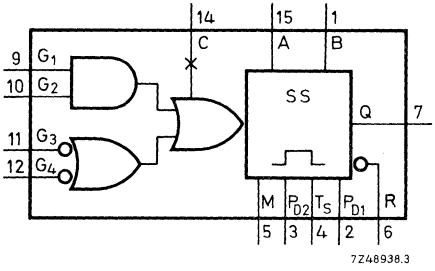
Dynamic data

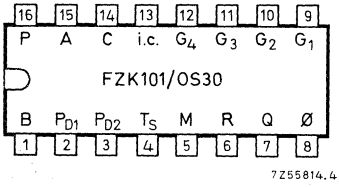


The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

MONOSTABLE MULTIVIBRATOR

with slow-down capability

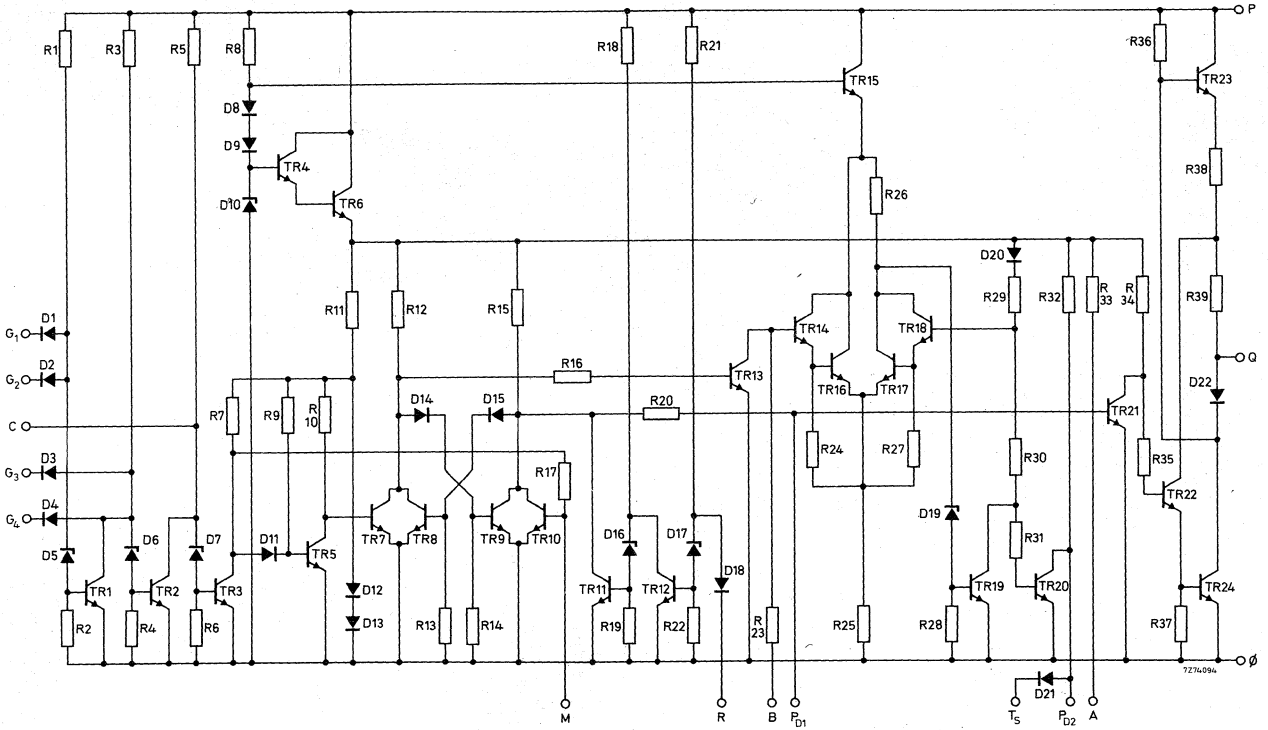




QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay: T_{amb} = 25 °C; V_{pd} = 4,5 V (ranges I and II)	t_{pdr}	typ.	270	ns
Available d.c. fan-out: LOW state	N_{aL}	max.	10	
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	M_L=M_H	typ.	5	V
	M_L	typ.	5	V
range II : V_P = 15 V	M_H	typ.	8	V
Average power consumption				
(50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	145	mW
range II: V_P = 15 V	P_{av}	typ.	180	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



GENERAL DESCRIPTION

The FZK101/OS30 has the following electrical functions and properties.

If the FZK101/OS30 is used as :

a. Monostable multivibrator: P_{D2}, T_S and M have to be interconnected
b. Pulse delaying circuit : P_{D1} and P_{D2} have to be interconnected
c. Pulse shortening circuit : T_S and M have to be interconnected.
d. Delay switch : P_{D1} with P_{D2} and M with ϕ have to be interconnected.

The output-pulse duration and pulse-delaying duration depend upon a resistor R_t which is externally connected between A and B and a capacitor C_t between B and ϕ. Output pulse durations and propagation delay are very stable with temperature and supply voltage changes.
The LOW state of output Q can be obtained by a LOW signal at input R.
The noise immunity of the G-inputs will be increased by connecting a capacitor (max. 500 pF) between slow-down terminal C and ϕ.
To the terminals P_{D1}, P_{D2}, T_S and M no voltages or currents may be applied.
External interconnections between these terminals have to be as short as possible.
If input signals are applied to the inputs G_3 and G_4, inputs G_1 and/or G_2 have to be LOW.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Slow-down input voltage	$+V_C$	max.	0,6	V
	$-V_C$	max.	1,0	V
Slow-down input current	$+I_C$	max.	2,0	mA
	$-I_C$	max.	10,0	mA
Output short-circuit duration	t_{Qsc}	max.	1	s 1)

1) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0	to	+70	°C
Uniform system supply voltage (range I)	V_P	11,4	to	13,5	V
(range II)	V_P	13,5	to	17	V
D.C. noise margin; range I at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		2,5	V
range II at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		4,5	V
Supply current at range I; output HIGH	I_{Pav}	typ.		12	mA
output LOW	I_{Pav}	typ.		13	mA
at range II; output HIGH	I_{Pav}	typ.		14	mA
output LOW	I_{Pav}	typ.		15	mA
Power consumption (50% duty cycle) at range I = V_{Pmax}	P_{av}	max.		257	mW
at range II = V_{Pmax}	P_{av}	max.		391	mW
Slow-down capacitor	C_M	max.		500	pF
Thermal resistance from system to ambient	R_{th}	max.		150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1])	max.	Conditions and references V_P (V)	
Static data						
Voltages						
Input HIGH	V_{GH}	7,5	–	– V	11,4	$V_{QL} \leq 1,7$ V; I_{QL} = 15 mA
Input LOW	V_{GL}	–	–	4,5 V	11,4 and 13,5	$V_{QH} \geq 10$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	10,0	11,3	– V	11,4 and 13,5	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	0,9	1,7 V	11,4	V_{GH} = 7,5 V; I_{QL} = 15 mA
D.C.noise margin: HIGH	M_H	2,5	5,0	– V	11,4	
LOW	M_L	2,8	5,0	– V	11,4	
Currents (per input)						
Input HIGH	I_{GH}	–	–	1,0 µA	13,5	V_G = 13,5 V (other inputs 0 V)
Input LOW	$-I_{GL}$	–	0,8	1,5 mA	13,5	V_{GL} = 1,7 V other inputs 13,5V
Output HIGH	$-I_{QH}$	–	–	0,1 mA	11,4 and 13,5	V_{GL} = 4,5 V; V_{QH} = 10 V
Output LOW	I_{QL}	15	–	– mA	11,4	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	10	30	50 mA	13,5	V_G= 0 V; V_Q= 0 V
Supply data						
Currents						
at V_{GL}	I_P	–	13,0	18,5 mA	13,5	
at V_{GH}	I_P	–	12,0	17,0 mA	13,5	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	symbol	min.	typ. [1]	max.		conditions and references
Dynamic data						
Times						
Propagation delay:						
G → Q						
fall time	t_{pdf}	110	180	450	ns	C_L = 10 pF
rise time	t_{pdr}	220	270	740	ns	N = 1
R → Q						
fall time	t_{pdf}	150	300	550	ns	T_{amb} = 25 °C
Output fall time	t_f	30	80	150	ns	V_{pd} = 4,5 V
Output rise time	t_r	50	100	200	ns	
Input pulse duration	t_{GH}	0,5	-	-	µs	
Reset pulse duration	t_{RL}	0,5	-	-	µs	
Recovery time	t_{rec}		$(C_o + C_t) \times 10^3$		s/F	C_o = 10 pF
Set-up time						between B and ϕ
at G_1, G_2	t_{su}	0	-	-	µs	
at G_3, G_4	t_{su}	0,5	-	-	µs	
Output pulse duration	t_{QHmin}	400			ns	V_P = 11,4 V
Output pulse duration	t_{QH}	650	700	780	µs	R_t = 0,5 MΩ
Capacitor	C_t	0	-	∞	µF	C_t = 2 nF
Resistor	R_t	5	-	500	kΩ	see note 2
Input slope, G_1, G_2	$(dV/dt)_T$	0,1			V/µs	
G_3, G_4		1			V/µs	

[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.
[2] For higher accuracy R_t = 40 to 200 kΩ.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.[1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	13,5	$V_{QL} \leq 1,7$ V; I_{QL} = 18 mA
Input LOW	V_{GL}	–	–	4,5	V	13,5 and 17	$V_{QH} \geq 12$ V; $-I_{QH}$ = 0,1 mA
Output HIGH	V_{QH}	12,0	14,3	–	V	13,5 and 17	V_{GL} = 4,5 V; $-I_{QH}$ = 0,1 mA
Output LOW	V_{QL}	–	1,0	1,7	V	13,5	V_{GH} = 7,5 V; I_{QL} = 18 mA
D.C. noise margin: HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents (per input)							
Input HIGH	I_{GH}	–	–	1,0	μA	17	V_G = 17 V; other inputs 0 V
Input LOW	$-I_{GL}$	–	1,0	1,8	mA	17	V_{GL} = 1,7 V; other inputs 17V
Output HIGH	$-I_{QH}$	–	–	0,1	mA	13,5 and 17	V_{GL} = 4,5 V; V_{QH} = 12 V
Output LOW	I_{QL}	18	–	–	mA	13,5	V_{GH} = 7,5 V; V_{QL} = 1,7 V
Output short-circuited	$-I_{Qsc}$	15	37	50	mA	17	V_G = 0 V; V_Q = 0V
Supply data							
Currents							
at V_{GH}	I_P	–	14,0	20,0	mA	17	
at V_{GL}	I_P	–	15,0	21,5	mA	17	

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	symbol	min.	typ. [1]	max.		conditions and references
Dynamic data						
Times						
Propagation delay:						
G ⟶ Q						
fall time	t_{pdf}				ns	C_L = 10 pF
rise time	t_{pdr}				ns	N = 1
R ⟶ Q			t.b.f.			T_{amb} = 25 °C
fall time	t_{pdf}				ns	V_{pd} = 4,5 V
Output fall time	t_f				ns	
Output rise time	t_r				ns	
Input pulse duration	t_{GH}	0,5	–	–	µs	
Reset pulse duration	t_{RL}	0,5	–	–	µs	
Recovery time	t_{rec}		$(C_o + C_t) \times 10^3$		s/F	C_o = 10 pF
Set-up time						between B and ϕ
at G_1, G_2	t_{su}	0	–	–	µs	
at G_3, G_4	t_{su}	0,5	–	–	µs	
Output pulse duration	t_{QHmin}	400	700		ns	V_P = 13,5 V
Output pulse duration	t_{QH}	650	700	780	µs	R_t = 0,5 MΩ
Capacitor	C_t	0	–	∞	µF	C_t = 2 nF
Resistor	R_t	5	–	500	kΩ	see note 2
Input slope, G_1, G_2	$(dV/dt)_T$	0,1			V/µs	
G_3, G_4		1			V/µs	

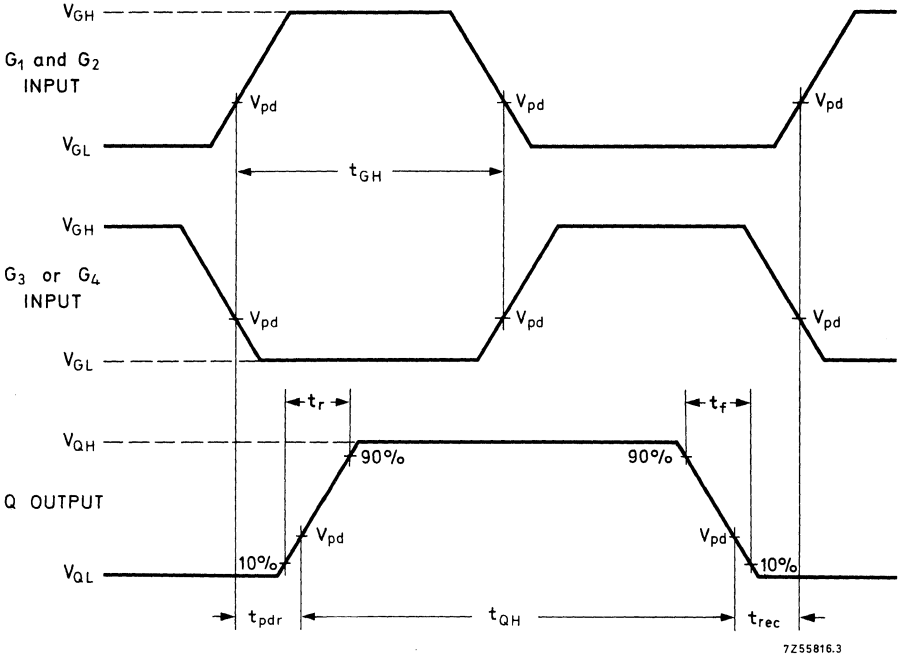
[1] All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

[2] For higher accuracy R_t = 40 to 200 kΩ.

CHARACTERISTICS (continued)

Dynamic data

FZK101/OS30 used as monostable multivibrator

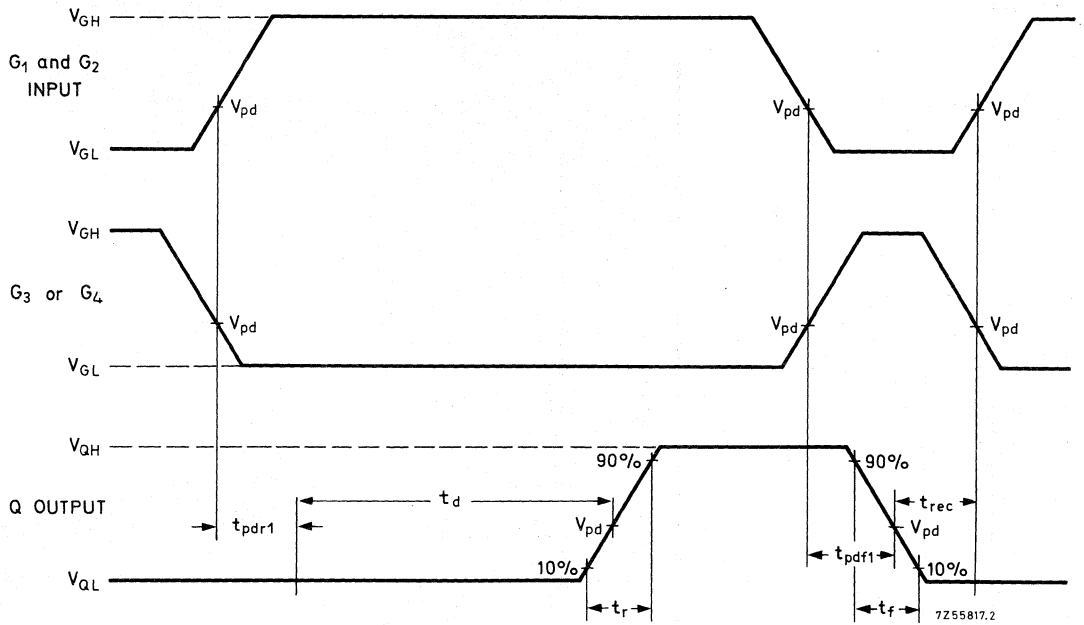


Conditions: P_{D2} and M interconnected
$t_{QH} = 0,7 \times R_t \ (C_o + C_t)$

CHARACTERISTICS (continued)

Dynamic data

FZK101/OS30 used as pulse delayed circuit

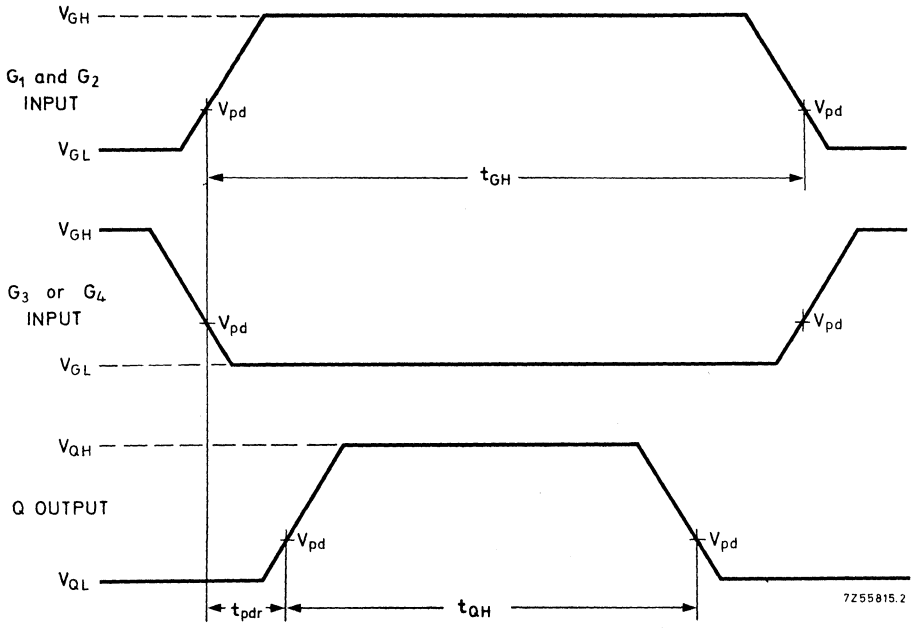


Conditions: P_{D1} and P_{D2} interconnected
$t_d = 0,7 \times R_t \ (C_o + C_t)$

CHARACTERISTICS (continued)

Dynamic data

FZK101/OS30 used as pulse shortened circuit



Conditions: T_S and M interconnected

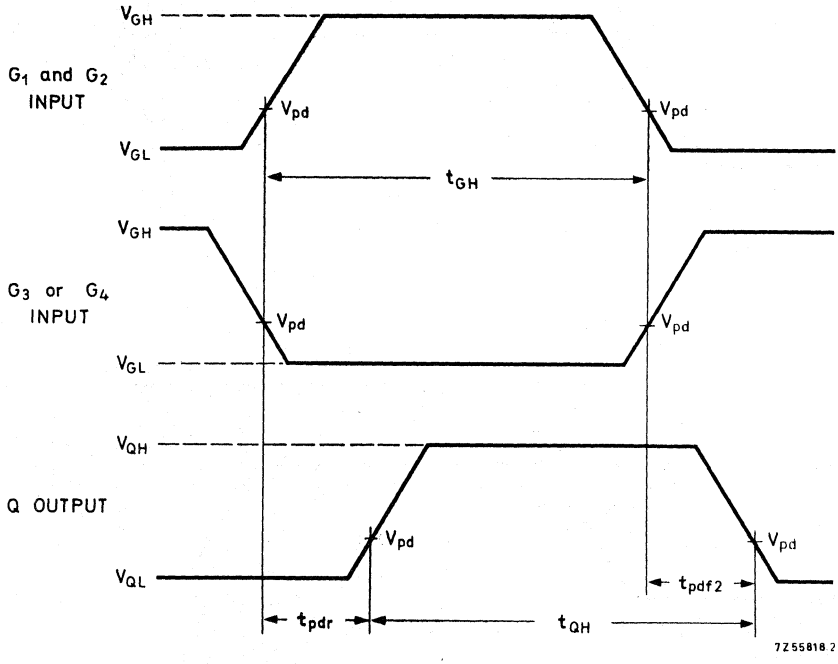
$t_{GH} > 0,7 \times R_t (C_o + C_t)$

$t_{QH} = 0,7 \times R_t (C_o + C_t)$

CHARACTERISTICS (continued)

Dynamic data

FZK101/OS30 used as pulse shortened circuit

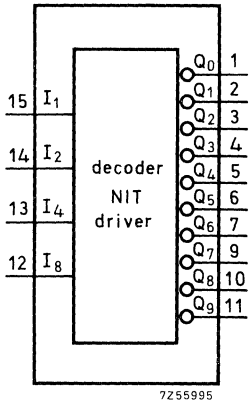


Conditions: T_S and M interconnected

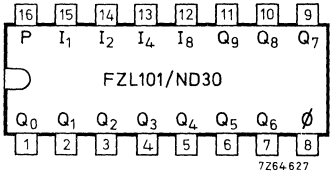
$t_{GH} \leq 0,7 \times R_t (C_o + C_t)$

$t_{QH} = t_{GH}$

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.



SINGLE BCD-DECIMAL DECODER N.I.T.[1] DRIVER



QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Output current (per output):				
output transistor in off-state	I_Q	max.	2	mA
output transistor in on-state	I_Q	max.	20	mA
Output voltage at any output (output transistor in cut-off)	V_Q	max.	80	V
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	typ.	17	mA
V_P = 17 V	I_{Pav}	typ.	18	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	M_L	typ.	5,5	V
	M_H	typ.	4,5	V
range II : V_P = 15 V	M_L	typ.	5,5	V
	M_H	typ.	7,5	V
Average power consumption (50% duty cycle) range I : V_P = 12 V	P_{av}	typ.	205	mW
range II : V_P = 15 V	P_{av}	typ.	270	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

[1] N.I.T. = numerical indicator tube.

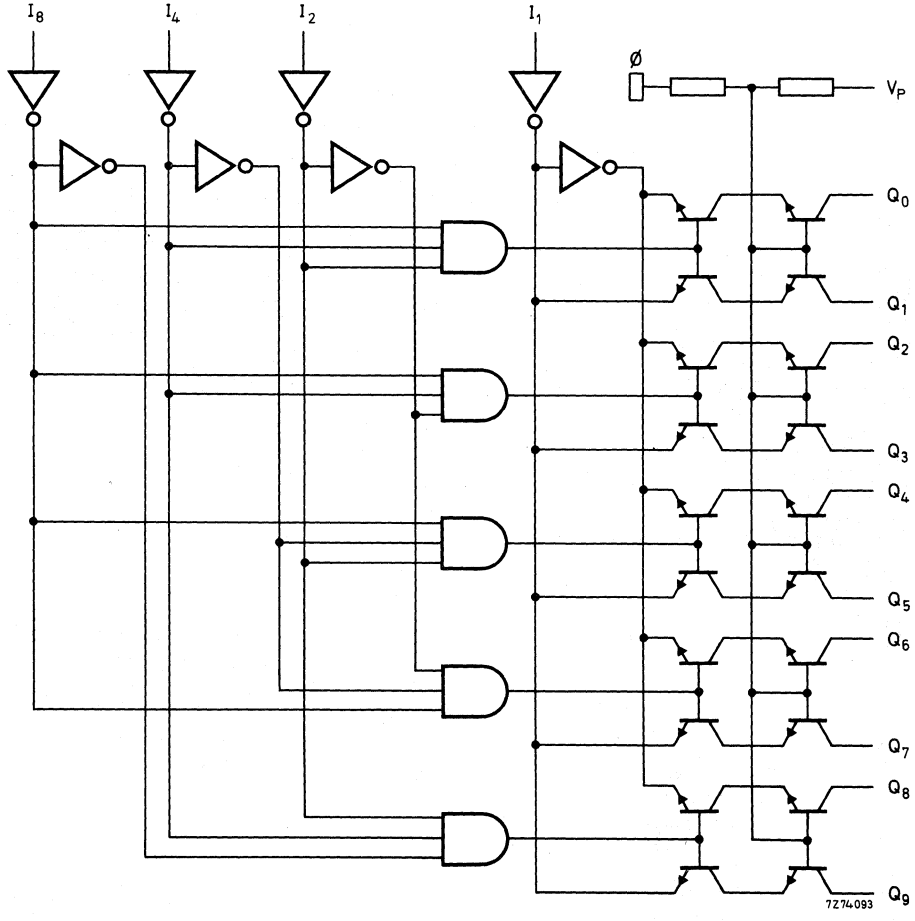
GENERAL DESCRIPTION

The FZL101/ND30 is a BCD (1-2-4-8 code) to decimal decoder incorporating high voltage output transistors for driving numerical indicator tubes.

Note

When used as HNIL decoder for every output a 10 kΩ resistor, connected to V_P, is required. At the outputs hazard pulses can appear during transition stages.

LOGIC DIAGRAM



FUNCTION TABLE

inputs				outputs (on-state = L)									
I_1	I_2	I_4	I_8	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage (at any output)	V_Q	max.	80	V
Input voltage	V_I	max.	18	V
Current into any output (off-state)	I_Q	max.	2	mA
Current into any output (on-state)	I_Q	max.	20	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	3,3	V
	M_H	min.	2,0	V
range II at V_{Pmin}	M_L	min.	3,3	V
	M_H	min.	4,0	V
Power consumption (50% duty cycle) at range I : V_{Pmax}	P_{av}	max.	340	mW
at range II : V_{Pmax}	P_{av}	max.	460	mW
Supply current at range I : V_P = 12 V	I_P	max.	25	mA
range II : V_P = 15 V	I_P	max.	27	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ.[1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{IH}	8,0	–	–	V		
Input LOW	V_{IL}	–	–	5,0	V		
Output HIGH	V_{QH}	80	–	–	V	13,5	$-I_{QH}$ = 1 mA
Output LOW	V_{QL}	–	–	2,5	V	11,4	I_{QL} = 9 mA
D.C. noise margin							
HIGH	M_H	2,0	4,5	–	V	11,4	
LOW	M_L	3,3	5,5	–	V	11,4	
Currents							
Input HIGH	I_{IH}	–	–	1,0	µA	13,5	V_{IH} = 13,5 V
Input LOW	$-I_{IL}$	–	0,8	1,5	mA	13,5	V_{IL} = 0 V
Output HIGH: input combination 0 to 9	$-I_{QH}$	–	–	50	µA	13,5	V_{QH} = 70 V
input combination 10 to 15	$-I_{QH}$	–	–	5	µA	13,5	V_{QH} = 60 V
Supply data							
Supply current	I_P	–	17	25	mA	13,5	input voltage at I_1, I_4, I_8 = 0 V and at I_2 = 13,5 V

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C.

	Symbol	min.	typ. [1])	max.		Conditions and references
Dynamic data						
Times						
Propagation delay:						
$I_2 \longrightarrow Q_2$						
fall time	t_{pdf}	60	150	280	ns	C_L = 10 pF
rise time	t_{pdr}	30	70	210	ns	N = 1
$I_2 \longrightarrow Q_0$						T_{amb} = 25 °C
fall time	t_{pdf}	30	70	210	ns	V_L = 12 V
rise time	t_{pdr}	60	150	280	ns	R_L = 1 kΩ

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)

Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

	Symbol	min.	typ. [1]	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{IH}	8,0	–	–	V		
Input LOW	V_{IL}	–	–	5,0	V		
Output HIGH	V_{QH}	80	–	–	V	17,0	$-I_{QH}$ = 1 mA
Output LOW	V_{QL}	–	–	2,5	V	13,5	I_{QL} = 9 mA
D.C. noise margin							
HIGH	M_H	4,0	7,5	–	V	13,5	
LOW	M_L	3,3	5,5	–	V	13,5	
Currents							
Input HIGH	I_{IH}	–	–	1,0	µA	17,0	V_I = 17,0 V
Input LOW	$-I_{IL}$	–	1,0	1,8	mA	17,0	V_I = 0 V
Output HIGH:							
input combination 0 to 9	$-I_{QH}$	–	–	50	µA	17,0	V_{QH} = 70 V
input combination 10 to 15	$-I_{QH}$	–	–	5	µA	17,0	V_{QH} = 60 V
Supply data							
Supply current	I_P	–	18	27	mA	17,0	input voltage at I_1, I_4, I_8 = 0 V and at I_2 = 13,5 V

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

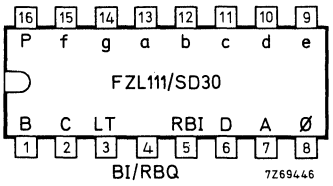
CHARACTERISTICS (continued)

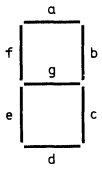
	Symbol	min. typ. [1] max.	Conditions and references
Dynamic data			
Propagation delay:			
$I_2 \longrightarrow Q_2$			
fall time	t_{pdf}	t.b.f.	
rise time	t_{pdr}		
$I_2 \longrightarrow Q_0$			
fall time	t_{pdf}		
rise time	t_{pdr}		

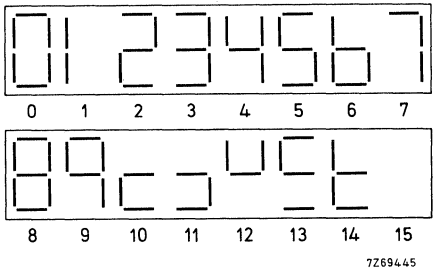
[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

BCD 7-SEGMENT DECODER-DRIVER
with open collector outputs







QUICK REFERENCE DATA				
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Output current per output				
output transistor in off-state	I_Q	max.	25	µA
output transistor in on-state	I_Q	max.	20	mA
Output voltage at any output (output transistor in off-state)	V_Q	max.	16,5	V
Average supply current at T_{amb} = 25 °C				
V_P = 13,5 V	I_{Pav}	<	40	mA
V_P = 16,5 V	I_{Pav}	<	44	mA
D.C. noise margin at T_{amb} = 25 °C				
range I : V_P = 12 V	$M_L = M_H$	typ.	5,0	V
range II: V_P = 15 V	M_L	typ.	5,0	V
	M_H	typ.	8,0	V
Average power consumption				
(50% duty cycle) range I : V_P = 13,5 V	P_{av}	max.	540	mW
range II: V_P = 16,5 V	P_{av}	max.	725	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section)

GENERAL DESCRIPTION

The FZL111/SD30 transforms 4-bit BCD-words at the inputs A, B, C, D into the 7-segment code. Control functions are provided by means of three auxiliary inputs; BI, RBI, LT. A LOW signal at the ripple-blanking input (RBI) suppresses the decimal 0-signal at the outputs. The ripple-blanking output (RBQ; internally connected with BI) provides an automatic 0-suppression over several decades. When the blanking input (BI) is supplied with a LOW signal, all outputs are blocked. A LOW signal at the lamp-test input (LT) forces all outputs into conduction.

FUNCTION TABLE

function	inputs						BI or RBQ	segment outputs (on-state = L)						
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g
0 [1]	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	H	H	H	L	L	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
BI [2]	X	X	X	X	X	X	L	H	H	H	H	H	H	H
RBI [3]	H	L	L	L	L	L	L	H	H	H	H	H	H	H
LT [4]	L	X	X	X	X	X	H	L	L	L	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

1) If 0-indication is desired, RBI must be supplied with a HIGH signal.

2) A LOW signal at BI forces all segment outputs into HIGH state independent of the other input conditions.

3) If a LOW signal is supplied to RBI and A, B, C, D; HIGH signals result at all outputs and LOW signal at RBQ (zero condition).

4) A LOW signal at LT switches all outputs to L only if BI/RBQ is supplied with a HIGH signal regardless of the input condition at A, B, C, D and RBI.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage (outputs a to g; off-state)	V_Q	max.	16,5	V
Output current (outputs a to g; off-state)	I_Q	max.	25	μA
Output current (outputs a to g; on-state)	I_Q	max.	20	mA
with 50% duty cycle	I_Q	max.	40	mA
Storage temperature	T_{stg}	−65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70		°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5		V
(range II)	V_P	13,5 to 16,5		V
D.C. noise margin to all inputs: range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Power consumption (50% duty cycle) at range I : V_{Pmax}	P_{av}	max.	540	mW
at range II: V_{Pmax}	P_{av}	max.	725	mW
Supply current at range I : V_P = 12 V	I_P	max.	40	mA
at range II: V_P = 15 V	I_P	max.	44	mA
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditons: at range I (V_P = 12 V); T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ. [1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{IH}	7,5	–	–	V	11,4	
Input LOW	V_{IL}	–	–	4,5	V	11,4 and 13,5	
Outputs a to g	V_Q	–	–	16,5	V	11,4	I_Q = 25 µA
Output HIGH at BI/RBQ	V_{QH}	10	11,3	–	V	13,5	$-I_{QH}$ = 0,1 mA
Output LOW							
at outputs a to g	V_{QL}	–	0,4	0,7	V	11,4	I_{QL} = 20 mA
	V_{QL}	–	0,7	1,0	V	11,4	I_{QL} = 40 mA
at outputs BI/RBQ	V_{QL}	–	–	1,7	V	11,4	I_{QL} = 7,5 mA
D.C. noise margin							
HIGH	M_H	2,5	5,0	–	V	11,4	
LOW	M_L	2,8	5,0	–	V	11,4	
Currents							
Input HIGH							
at A, B, C, D, RBI	I_{IH}	–	–	10	µA	13,5	V_{IH} = 13,5 V
at BI/RBQ	I_{IH}	–	–	20	µA	13,5	
at LT	I_{IH}	–	–	30	µA	13,5	
Input LOW							
at A, B, C, D, RBI	I_{IL}	–	1,0	2,1	mA	13,5	V_{IL} = 1,7 V
at BI/RBQ	I_{IL}	–	2,0	4,2	mA	13,5	
at LT	I_{IL}	–	3,0	5,3	mA	13,5	
Supply data							
Supply current	I_P	–	–	40	mA	13,5	outputs open

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS Test conditions: at range II (V_P = 15 V); T_{amb} = 0 to +70 °C

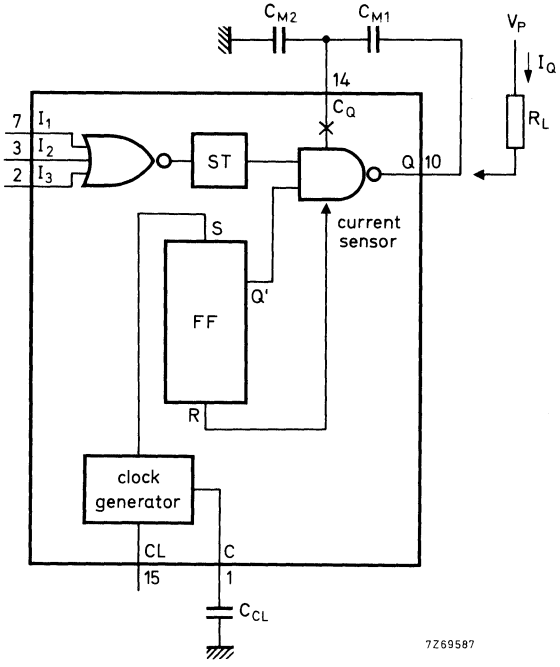
	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{IH}	7,5	–	–	V	13,5	
Input LOW	V_{IL}	–	–	4,5	V	13,5 and 16,5	
Outputs a to g	V_Q	–	–	16,5	V	13,5	I_Q = 25 µA
Output HIGH at BI/RBQ	V_{QH}	12	14,3	–	V	16,5	$-I_{QH}$ = 0,1 mA
Output LOW							
at outputs a to g	V_{QL}	–	0,4	0,7	V	13,5	I_{QL} = 20 mA
	V_{QL}	–	0,7	1,0	V	13,5	I_{QL} = 40 mA
at output BI/RBQ	V_{QL}	–	–	1,7	V	13,5	I_{QL} = 9 mA
D.C. noise margin							
HIGH	M_H	4,5	8,0	–	V	13,5	
LOW	M_L	2,8	5,0	–	V	13,5	
Currents							
Input HIGH							
at A, B, C, D, RBI	I_{IH}	–	–	10	µA	16,5	V_{IH} = 16,5 V
at BI/RBQ	I_{IH}	–	–	20	µA	16,5	
at LT	I_{IH}	–	–	30	µA	16,5	
Input LOW							
at A, B, C, D, RBI	I_{IL}	–	–	2,6	mA	16,5	V_{IL} = 1,7 V
at BI/RBQ	I_{IL}	–	–	5,2	mA	16,5	
at LT	I_{IL}	–	–	7,8	mA	16,5	
Supply data							
Supply current	I_P	–	–	44	mA	16,5	outputs open

[1]) All typical values under test conditions: T_{amb} = 25 °C and V_P = 15 V.

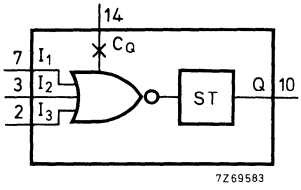
The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SHORT-CIRCUIT-PROOF POWER STAGE

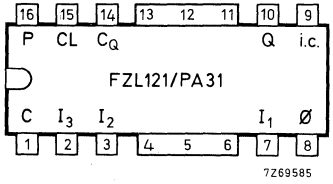
with open collector output



Logic diagram for short-circuit operation



Logic diagram for normal operation



pins 4 to 6 and 11 to 13 are connected to provide a heatsink

QUICK REFERENCE DATA				
Supply voltage range	V_P		11,4 to 20	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Output current	I_Q	max.	400	mA
Supply current	I_P	typ.	5	mA
Capacitance at CL	C_{CL}	typ.	39	nF
Capacitance at C_Q	C_{M1}	typ.	500	pF
	C_{M2}	typ.	1,8	nF

PACKAGE OUTLINE 16 lead plastic dual in-line (see page 218).

GENERAL DESCRIPTION

The FZL121/PA31 is a power stage for output currents up to 400 mA. It has 3-NOR gate inputs with Schmitt trigger characteristics.
The load is connected between the output Q (open collector) and the supply terminal P.
If a short circuit occurs the current is turned off and the circuit checks periodically whether the short circuit is still present.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	20	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_{IH}	max.	V_P	
Output current	I_Q	max.	400	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

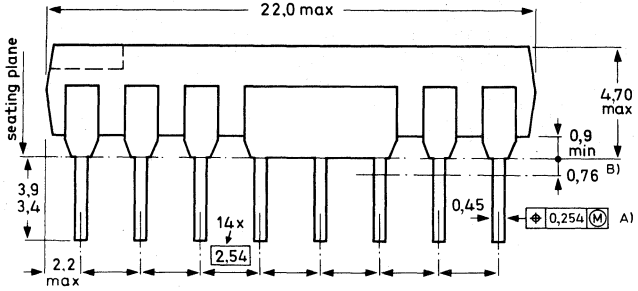
CHARACTERISTICS Test conditions: T_{amb} = 0 to +70 °C

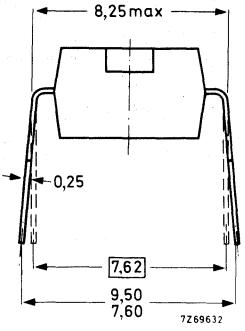
	Symbol	min.	typ.	max.		Conditions and references: V_P (V)	Conditions and references:
Voltages							
Input HIGH	V_{IH}	8	–	–	V	11,4	
Input LOW	V_{IL}	–	–	6	V	20	
Hysteresis	V_H	–	0,4	–	V	15	
Output LOW	V_{QL}	–	1,6	2,6	V		I_Q = 0,4 A; V_I = V_P
Currents							
Input current	I_I	0,1	–	0,2	mA		V_I = 2 V to V_P
Output current	I_Q	–	–	400	mA	20	
Supply current	I_P	–	5	–	mA	15	I_Q = 0
Nominal lamp current	I_Q	–	–	150	mA	20	
Capacitors							
Capacitance at CL	C_{CL}	–	39	–	nF		f = 0,5 kHz
Capacitance at C_Q	C_{M1}	–	500	–	pF		
	C_{M2}	–	1,8	–	nF		
Capacitive loads	C_L	–	–	each C_M	nF		

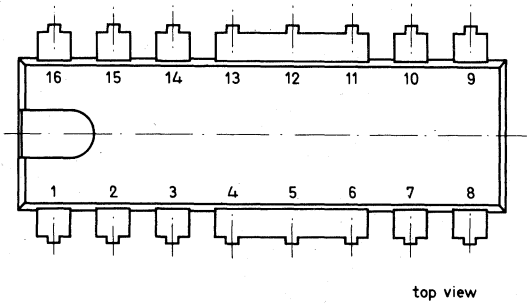
OPERATING NOTES (see also logic diagram on page 215)

To avoid oscillations during a short circuit it is necessary to connect two capacitors to the C_Q-terminal (C_{M1}, C_{M2}). The transition at the output Q can be varied by means of C_{M1}. A capacitor C_{CL} between the C-terminal and ground is required for the clock generator. Up to 8 clock terminals CL of the types FZL121/PA31, FZL131/PA32 may be connected in parallel so that only one capacitor C_{CL} is required. The C-terminals of the remaining circuits must then be connected to V_P.
Inductive loads must be provided with a flywheel diode.

16 LEAD PLASTIC DUAL IN-LINE







top view

A) Centre-lines of all leads are within ±0,127 mm of the nominal positions shown; in the worst case, the spacing between adjacent leads may deviate from nominal by ±0,254 mm.

B) Tolerances of note A within this distance

⊕ Locational truth

Ⓜ Maximum Material Condition

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

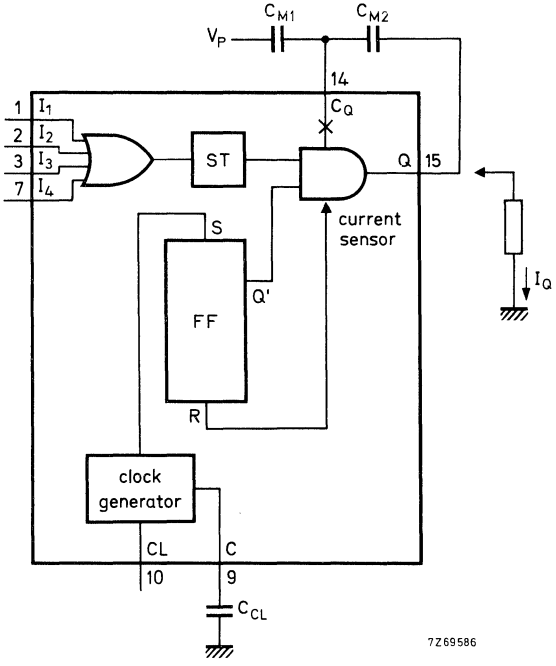
3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

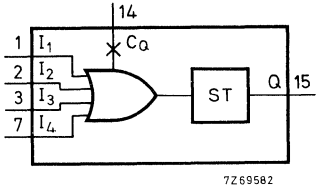
The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SHORT-CIRCUIT-PROOF POWER STAGE

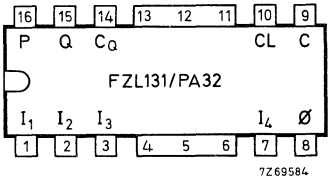
with open collector output



Logic diagram for short circuit operation



Logic diagram for normal operation



pins 4 to 6 and 11 to 13 are connected to provide a heatsink

QUICK REFERENCE DATA				
Supply voltage range	V_P		11,4 to 20	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Output current	I_Q	max.	400	mA
Supply current	I_P	typ.	5	mA
Capacitance at CL	C_{CL}	typ.	39	nF
Capacitance at C_Q	C_{M1}	typ.	500	pF
	C_{M2}	typ.	1,8	nF

PACKAGE OUTLINE 16 lead plastic dual in-line (see page 222).

GENERAL DESCRIPTION

The FZL131/PA32 is a power stage for output currents up to 400 mA and for nominal lamp currents of up to 150 mA. It has 4-OR gate inputs with Schmitt trigger characteristics. The load is connected between the output Q (open emitter) and the ground terminal ϕ. If a short circuit occurs the current is turned off and the circuit checks periodically whether the short circuit is still present.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	20	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_{IH}	max.	V_P	
Output current	I_Q	max.	400	mA
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

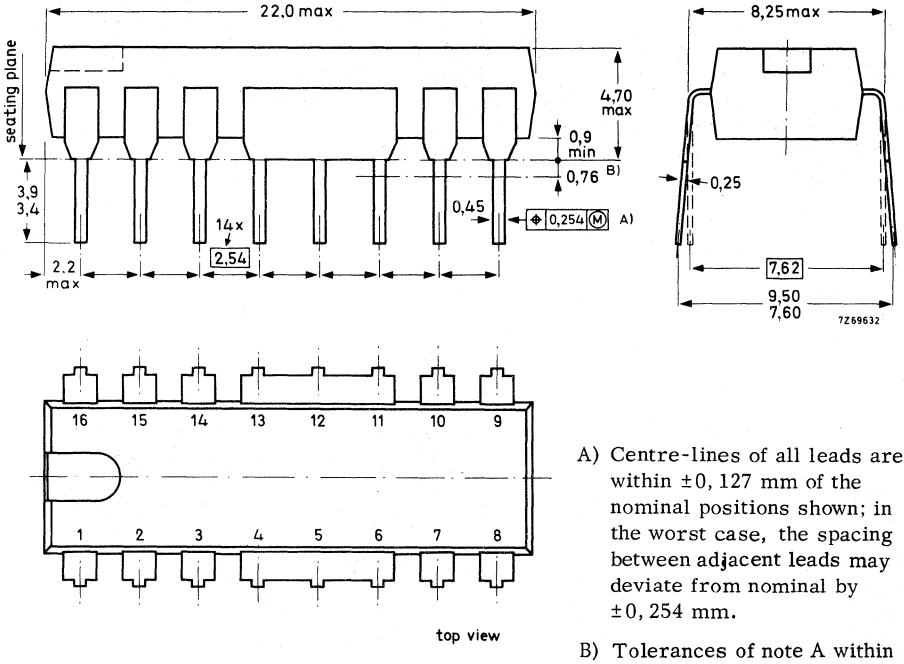
CHARACTERISTICS Test conditions: T_{amb} = 0 to +70 °C

	Symbol	min.	typ.	max.		Conditions and references: V_P (V)	
Voltages							
Input HIGH	V_{IH}	8	–	–	V	11,4	
Input LOW	V_{IL}	–	–	6	V	20	
Hysteresis	V_H	–	0,4	–	V	15	
Output HIGH	V_{QH}	V_P-3	V_P-1,8	–	V		$-I_Q$ = 0,4 A
Currents							
Input current	I_I	0,1	–	0,2	mA		V_I = 2 V to V_P
Output current HIGH	$-I_{QH}$	–	–	400	mA	20	
Supply current	I_P	–	5	–	mA	15	I_Q = 0
Nominal lamp current	I_Q	–	–	150	mA	20	
Capacitors							
Capacitance at CL	C_{CL}	–	39	–	pF		f = 0,5 kHz
Capacitance at C_Q	CM1	–	500	–	pF		
	CM2	–	1,8	–	nF		

OPERATING NOTES (see also logic diagram on page 219)

To avoid oscillations during a short circuit it is necessary to connect two capacitors to the C_Q-terminal (C_{M1}, C_{M2}). The transition at the output Q can be varied by means of C_{M1}. A capacitor C_{CL} between the C-terminal and ground is required for the clock generator. Up to 8 clock terminals CL of the types FZL121/PA31, FZL131/PA32 may be connected in parallel so that only one capacitor C_{CL} is required. The C-terminals of the remaining circuits must then be connected to V_P.
Inductive loads must be provided with a flywheel diode.

16 LEAD PLASTIC DUAL IN-LINE



A) Centre-lines of all leads are within ±0,127 mm of the nominal positions shown; in the worst case, the spacing between adjacent leads may deviate from nominal by ±0,254 mm.

B) Tolerances of note A within this distance

⊕ Locational truth

Ⓜ Maximum Material Condition

SOLDERING

1. By hand

   Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

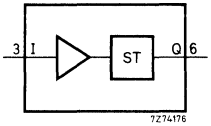
   260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
   The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

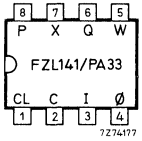
3. Repairing soldered joints

   The same precautions and limits apply as in (1) above.

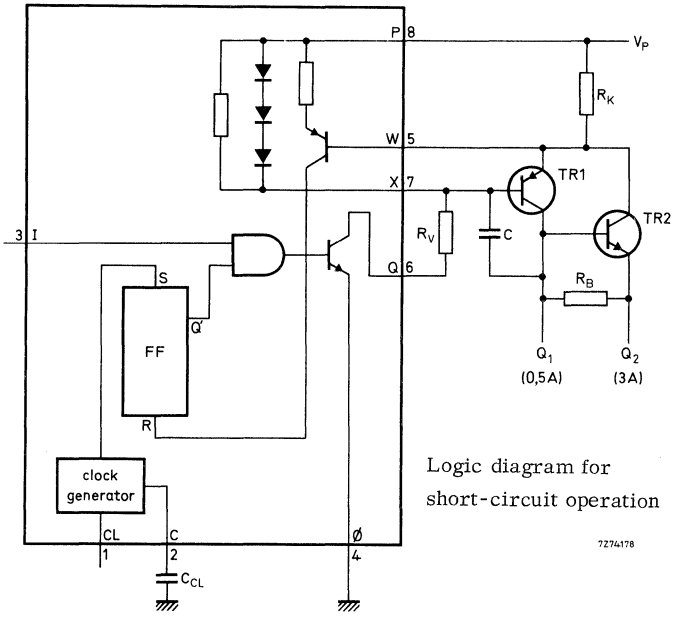
The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SHORT-CIRCUIT-PROOF POWER DRIVER FOR TRANSISTOR STAGES





Logic diagram for normal operation



Logic diagram for short-circuit operation

QUICK REFERENCE DATA				
Supply voltage range	V_P		11,4 to 20	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Output current at Q	$-I_Q$	max.	25	mA
at Q_1	I_{Q1}	max.	500	mA
at Q_2	I_{Q2}	max.	3	A

PACKAGE OUTLINE 8 lead plastic dual in-line (see page 225).

GENERAL DESCRIPTION

The FZL141/PA33 is a driver for transistor power stages with output currents up to 3 A and it has a SCHMITT trigger input. The output (Q_2) of the controlled power stage is short-circuit-proof. If a short circuit occurs the current is turned off and the circuit checks periodically whether the short circuit is still present. The load is connected between output Q_1 (or Q_2) and the ground terminal ϕ.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	20	V
Output voltage at Q_1	V_{Q1}	max.	V_P	
at Q_2	V_{Q2}	max.	V_P	
Output current at Q	$-I_Q$	max.	25	mA
at Q_1	I_{Q1}	max.	500	mA
at Q_2	I_{Q2}	max.	3	A
Input voltage	V_I	max.	V_P	
Storage temperature	T_{stg}		−65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

CHARACTERISTICS Test conditions : T_{amb} = 0 to +70 °C

	Sym-bol	min.	typ.	max.		Conditions and references: V_P (V)	
Voltages							
Input HIGH	V_{IH}	8	–	–	V	11, 4	
Input LOW	V_{IL}	–	–	6	V	20	
Hysteresis	V_H	–	0, 4	–	V		
Output at Q_1	V_{Q1}	V_P−1, 8	V_P−1	–	V		I_{Q1} = 0, 5 A
Output at Q_2	V_{Q2}	V_P−3, 2	V_P−2	–	V		I_{Q2} = 3 A
Turn-off voltage for overload	V_W	–	V_P−0, 8	–	V		
Currents							
Input current	I_I	0, 1	–	0, 2	mA		V_I = 2 V to V_P
Input current at X	I_X	–	–	25	mA		
Output current at Q	$-I_Q$	–	–	25	mA		
at Q_1	I_{Q1}	–	–	500	mA		R_K = 1, 6 Ω
at Q_2	I_{Q2}	–	–	3	A		R_K = 0, 33 Ω
Resistance	R_v	$\frac{V_P-1\,(V)}{I_Q\,(mA)}$	–	–	kΩ		
	R_B	–	68	–	Ω		TR2 = 2N3055

OPERATING NOTES (see also logic diagram on page 223)

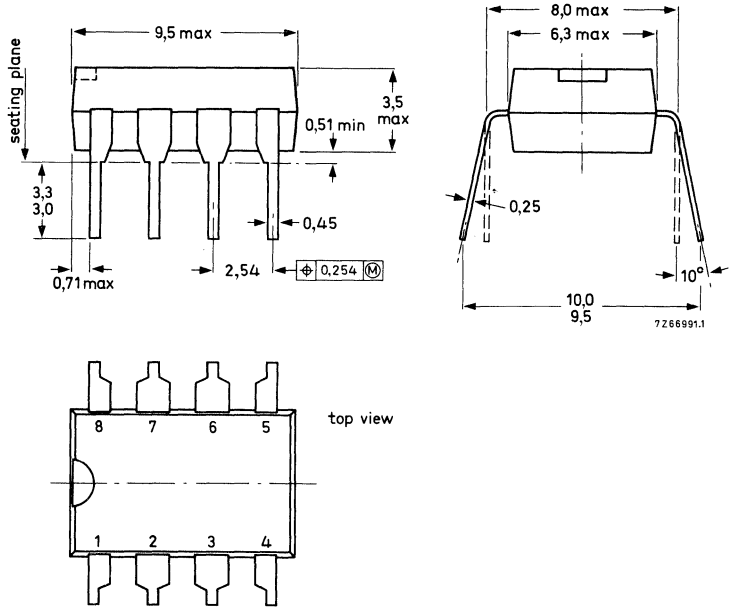
To avoid oscillations during a short-circuit it is necessary to connect a capacitor (C) between the base and collector of transistor TR1. A capacitor C_{CL} between the C-terminal and ground is required for the clock generator. Up to 8 clock terminals CL of the types FZL121/PA31, FZL131/PA32 and FZL141/PA33 may be combined in parallel so that only one capacitor C_{CL} is required. The C-terminals of the remaining circuits must then be connected to V_P. Inductive loads must be provided with a flywheel diode.

APPLICATION INFORMATION

A recommended type for TR1 is the BD227 (if only 0,5 A is required). If 3 A-output current is required, the BD227 for TR1 and the 2N3055 for TR2 are recommended, R_B is then 68 Ω.
The 2N3055 must be mounted on a heatsink of 50 x 50 x 1 mm Al.
Recommended value for $R_V = V_P/20$ kΩ.

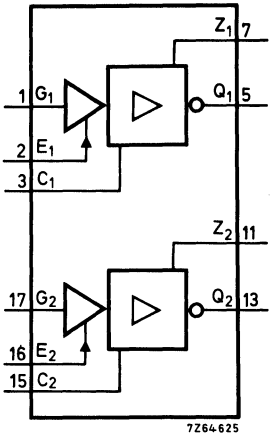
8 LEAD PLASTIC DUAL IN-LINE

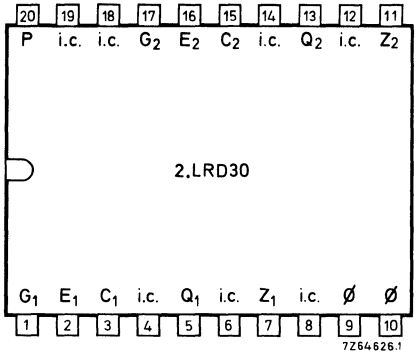
Dimensions in mm



The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL LAMP/RELAY DRIVER





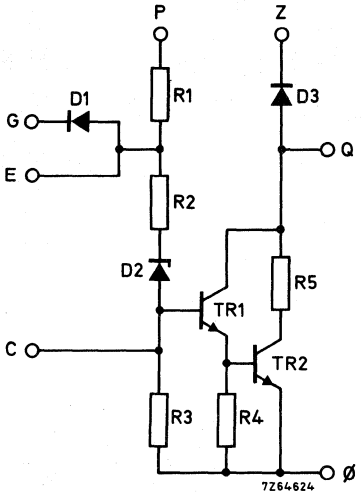
QUICK REFERENCE DATA				
Supply voltage	V_P	11,4 to 17,0		V
when loaded	V_{Pload}	max.	30	V
Operating ambient temperature	T_{amb}	−30 to + 75		°C
Output current (d.c.) T_{amb} = − 35 to +75 °C; V_{Pload} = 30 V	I_{QL}	max.	200	mA
Non-repetitive peak output current t_{max} = 20 ms	I_{QLM}	max.	400	mA
D.C. noise margin at T_{amb} = 25 °C	M_L	typ.	6	V
	M_H	typ.	7	V
Average power consumption T_{amb} = 25 °C; V_P = 15 V; Q = unloaded	P_{av}	typ.	40	mW

Note

Necessary input drive equal to 3 gate loads.

PACKAGE OUTLINE 20 lead dual in-line (see general section).

CIRCUIT DIAGRAM



GENERAL DESCRIPTION

The 2.LRD30 is a dual driver for output currents up to 200 mA at a supply voltage of maximum 30 V; it is used for driving lamps and relays.
The number of gate inputs can be extended by connecting up to 15 Si diodes to the expander terminal E (connect anodes of diodes to E) *).
With inductive loads the built-in clamping diode D3 must be used. This is done by connecting terminal Z to the load supply voltage, to protect the output transistor against damage caused by high inductive voltages.
To improve the a.c. noise immunity by increasing the propagation delay time, a capacitor has to be connected between terminals C and ϕ.
With a resistive load, the capacitor is connected between C and Q.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage	V_P	max.	20 V
when loaded	V_{Pload}	max.	30 V
Output voltage	V_{QH}	max.	30 V
Input voltage	V_{GH}	max.	30 V
Negative input voltage	$-V_G$	max.	4 V
Storage temperature	T_{stg}		−30 to + 85 °C
Operating ambient temperature	T_{amb}		−30 to + 75 °C

*) Diode leads should be kept as short as possible.

CHARACTERISTICS

Test conditions: T_{amb} = −30 to +70 °C

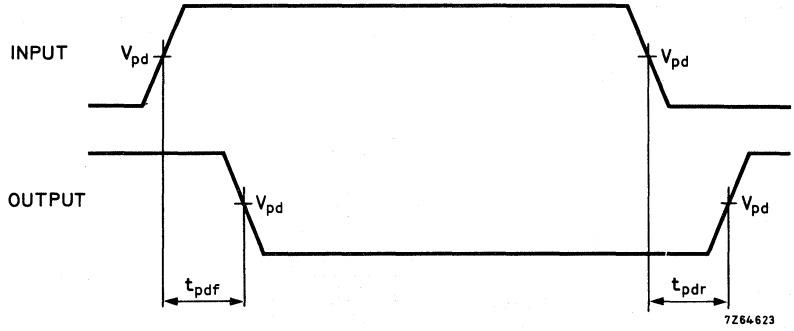
	sym-bol	min.	typ.[1])	max.		Conditions and references	
						V_P (V)	
Static data							
Voltages							
Input HIGH	V_{GH}	8,0	–	–	V	11,4 and 17,0	V_Q = LOW
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 17,0	I_Q = 0,5 mA
Output LOW	V_{QL}	–	0,9	1,3	V	11,4	$V_{GH} \geq 8,0$ V; I_Q = 200 mA
D.C. noise margin: HIGH	M_H	2,0	7	–	V	11,4	
LOW	M_L	2,8	6	–	V	11,4 and 17,0	
Currents							
Input HIGH	I_{GH}	–	0,1	10	µA	11,4 and 17,0	V_G = 17,0 V
Input LOW	$-I_{GL}$	–	–	5,4	mA	17,0	V_{GL} = 1,7 V
Output HIGH	I_{QH}	–	–	0,5	mA	11,4 and 17,0	$V_{GL} \leq 4,5$ V; V_{Pload} = 30 V
Output LOW	I_{QL}	–	–	200	mA	11,4 and 17,0	$V_G \geq 8,0$ V
Non-repetitive peak value; t_{max} = 20 ms	I_{QLM}	–	–	400	mA	11,4 and 17,0	$V_{GH} \geq 8,0$ V
Supply data							
Currents							
at V_{QH}	I_P	–	4,2	4,9	mA	17,0	V_G = 1,7 V
at V_{QL}	I_P	–	2,2	3,4	mA	17,0	$V_G \geq 8,0$ V
Dynamic data							
Input rise time	t_r	0,1	–	–	V/µs		
Input fall time	t_f	0,1	–	–	V/µs		

[1]) Typical values specified at V_P = 15 V and T_{amb} = 25 °C.

CHARACTERISTICS (continued)

Dynamic data

Loading capacitor connected between C and ϕ.



Waveforms illustrating measurement of t_{pdr} and t_{pdf}.

Measuring conditions: V_P = 15 V
I_{QL} = 200 mA
C_L = 10 pF
resistive load

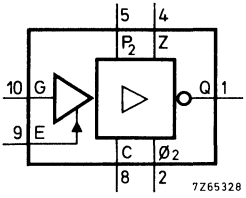
input waveform: $V_{pd} = \frac{1}{2} V_P$
output waveform: $V_{pd} = \frac{1}{2} V_{Pload}$

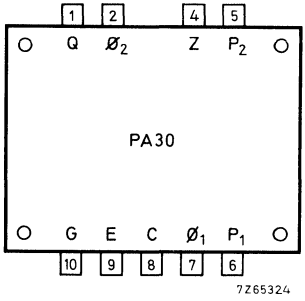
$t_{pdf} = (0,55 + 0,55 \times C_L)$ ns
$t_{pdr} = (0,30 + 0,30 \times C_L)$ ns

C_L in nF; C_L is 10 to 1000 nF

The 30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

POWER AMPLIFIER





top view

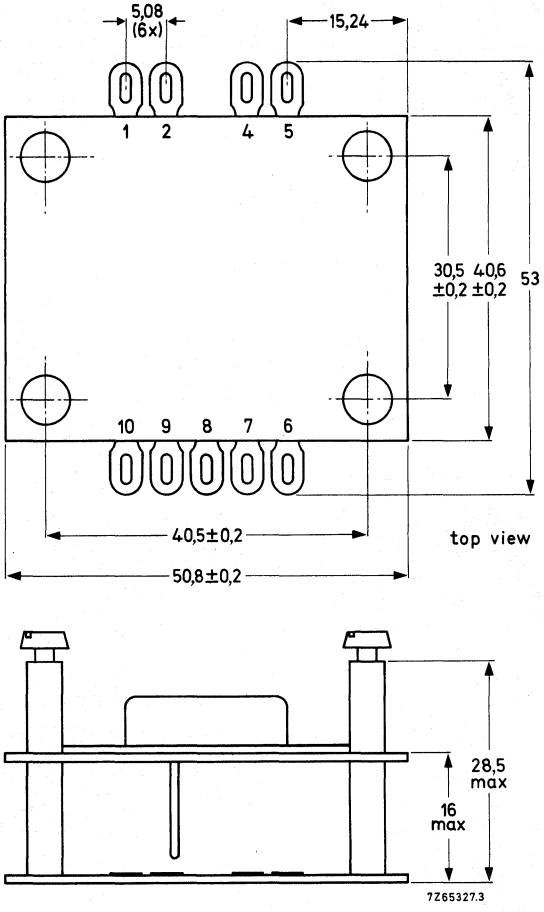
QUICK REFERENCE DATA				
Supply voltage	V_{P1}		11,4 to 17,0	V
	V_{PS}		11,4 to 55	V
Operating ambient temperature	T_{amb}		−30 to +75	°C
Output current (t_{av} = 20 ms)	I_{QL}	max.	2	A
Repetitive peak output current	I_{QLM}	max.	5	A
D.C. noise margin at T_{amb} = 25 °C	M_L	typ.	5	V
	M_H	typ.	8	V
Average power consumption at T_{amb} = 25 °C V_{P1} = 15 V; Q = unloaded; V_{PS} = 15 V; R_V = 0	P_{av}	typ.	240	mW

PACKAGE OUTLINE 9 leads special execution (see next page).

PACKAGE OUTLINE

Dimensions in mm

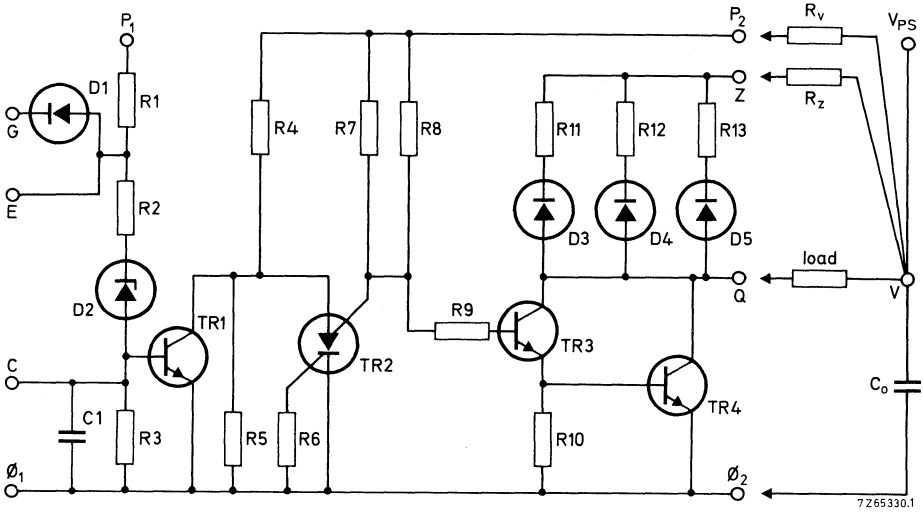
9 leads special execution



GENERAL DESCRIPTION

The PA30 is a power amplifier for output currents up to 2 A and output voltages up to 55 V, intended for driving heavy resistive and inductive loads.
The number of gate inputs can be extended by connecting up to 15 diodes (type BAW62) to the expander terminal E (connect anode of diode to E). *)
To increase the a.c. noise immunity, a capacitor can be connected between terminals C and $\phi 1$ (see also "Operating notes"). The load has to be connected between Q and point V. For inductive loads, terminal Z must also be connected to V, if necessary via a series resistor R_Z (see note 3 of "Operating notes").
Dependent on the V_{PS} value, a resistor R_V must be connected between terminal P_2 and point V (see note 1 of "Operating notes").
When the wire connection between V and supply voltage unit V_{PS} has some inductance, it is necessary to connect a capacitor C_o ($\approx 10\ \mu F$ per metre of wire) between V and $\phi 2$ as close as possible to the unit.

CIRCUIT DIAGRAM



*) Diode leads should be kept as short as possible.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages	V_{P1}	max.	20	V	[1]
	V_{PS}	max.	55	V	
Output voltage	V_{QH}	max.	55	V	
Input voltage	V_{GH}	max.	30	V	
Negative input voltage	$-V_{GL}$	max.	4	V	
Output current (average; t_{av} = 20 ms)	I_{QL}	max.	2	A	
Output current (peak value)	I_{QLM}	max.	5	A	
Storage temperature	T_{stg}		−40 to +85	°C	
Operating ambient temperature	T_{amb}		−30 to +75	°C	

[1]) See note 1 of "Operating notes".

CHARACTERISTICS Test conditions: T_{amb} = −30 to +75 °C

	Symbol	min.	typ. [1]	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	7,5	–	–	V	11,4 and 17,0	V_Q = LOW
Input LOW	V_{GL}	–	–	4,5	V	11,4 and 17,0	V_Q = HIGH
Output HIGH	V_{QH}	–	–	55	V	11,4 and 17,0	I_Q = 5 mA $V_G \leq 4,5$ V
Output LOW	V_{QL}	–	0,9	1,3	V	11,4 and 17,0	I_Q = 2 A $V_G \geq 7,5$ V
D.C. noise margin: LOW	M_L	2,8	5	–	V	11,4 and 17,0	
HIGH	M_H	2,5	8	–	V	11,4	
Currents							
Input HIGH	I_{GH}	–	0,1	10	μA	17,0	V_G = 17 V
Input LOW	$-I_{GL}$	–	–	5,1	mA	17,0	V_G = 1,7 V
Output HIGH	I_{QH}	–	1 μA	5	mA	11,4 and 17,0	V_{QH} = 55 V $V_G \leq 4,5$ V
Output LOW (t_{av} = 20 ms)	I_{QL}	–	–	2	A	11,4 and 17,0	V_{QL} = 1,3 V $V_G \geq 7,5$ V
(peak value)	I_{QLM}	–	–	5	A	11,4 and 17,0	V_{QL} = 1,3 V

[1]) All typical values under test conditions: V_{P1} = 15 V; V_{PS} = 15 V; R_v = 0; T_{amb} = 25 °C.

CHARACTERISTICS (continued) Test conditions: T_{amb} = −30 to +75 °C

	Sym-bol	min.	typ. [1]	max.	Conditions and references	
					V_P (V)	
Supply data						
Currents	I_{P1}	–	4,3	– mA	15	V_G = 1,7 V
	I_{P1}	–	2,6	– mA	15	V_G ≥ 7,5 V
	I_{P2}	–	14,5	– mA	15	V_G ≤ 4,5 V
	I_{P2}	–	12,5	– mA	15	V_G ≥ 7,5 V

[1]) All typical values under test conditions: V_{P1} = 15 V; V_{PS} = 15 V; R_V = 0; T_{amb} = 25 °C.

OPERATING NOTES

1. Supply voltage V_{PS}

When terminal P_2 is directly connected to point V the value of V_{PS} must be between 11,4 V and 19 V (15,2 V ± 25%).
By connecting a suitable resistor (R_V) between P_2 and V, any supply voltage V_{PS} between 11,4 and 55 V may be used, having a tolerance of ± 25%.
The values of R_V can be calculated from:

$$R_V = 75\ (V_{PSnom} - 15)\ \Omega \pm 8\%$$

2. For capacitor C_o see "General description"

3. Unit loaded with an inductive load

When an inductive load is switched, the built-in diodes (which protect the output transistor against voltage transients) have to be connected (Z to point V).
This protection is realized at the expense of a very long decay time of the current in the load.
At V_{PS} below 55 V a resistor R_Z may be connected in series with the protection diodes to decrease this decay time.

The maximum permissible value of R_Z can be calculated from:

$$R_Z < \frac{1}{I_Q}\ (55 - V_{PSmax})\ \Omega$$

Where: I_Q = the load current at switching-off.

The decay time of the load current can be calculated from:

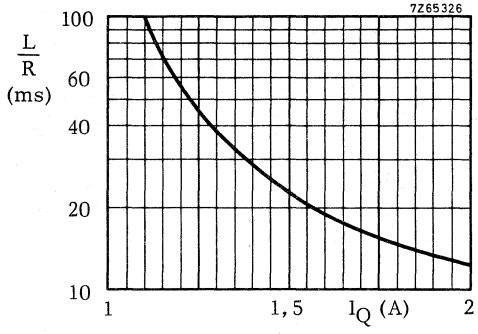
$$I_L = I_Q \exp - \frac{t}{L/R}$$

Where: I_Q = the load current at switching-off in amperes
L = inductance of the load in henrys
R = sum resistance of load and possible applied R_Z in ohms

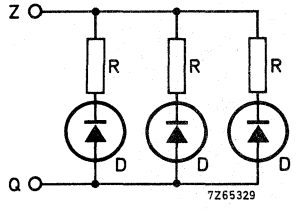
Note: V may be connected directly to Z ($R_Z = 0$) if there are no problems with decay time.

OPERATING NOTES (continued)

4. Inductance of the load



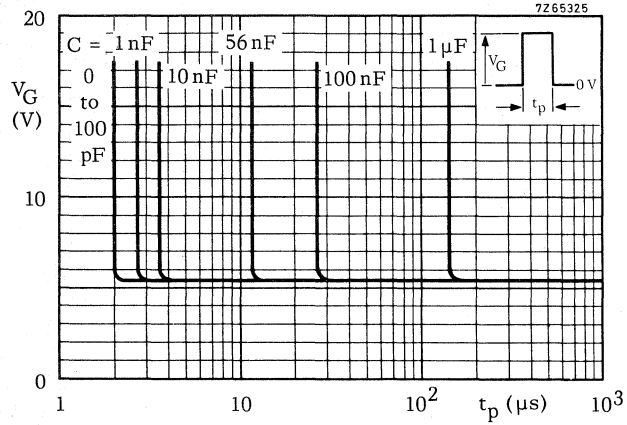
The maximum allowable inductance of the load can be calculated from the maximum permissible value of L/R as follows from the graph above.
I_Q = the load current at switching-off.
R = sum resistance of load and possible applied R_Z.



R = 1,5 Ω
D = BAX12

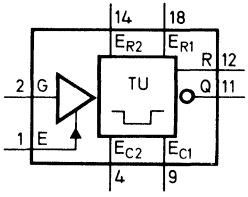
When the above circuit is connected between the terminals Z and Q, loads with any inductance value and currents up to 2 A can be applied.

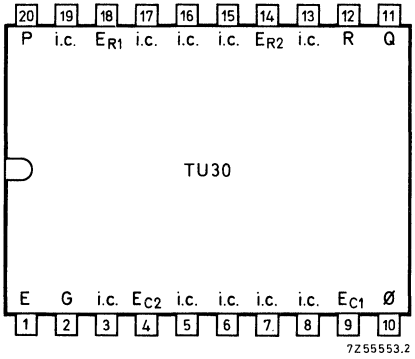
5. Input voltage versus input pulse duration as a function of a capacitor between terminals C and ϕ_1.



The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

TIMER UNIT

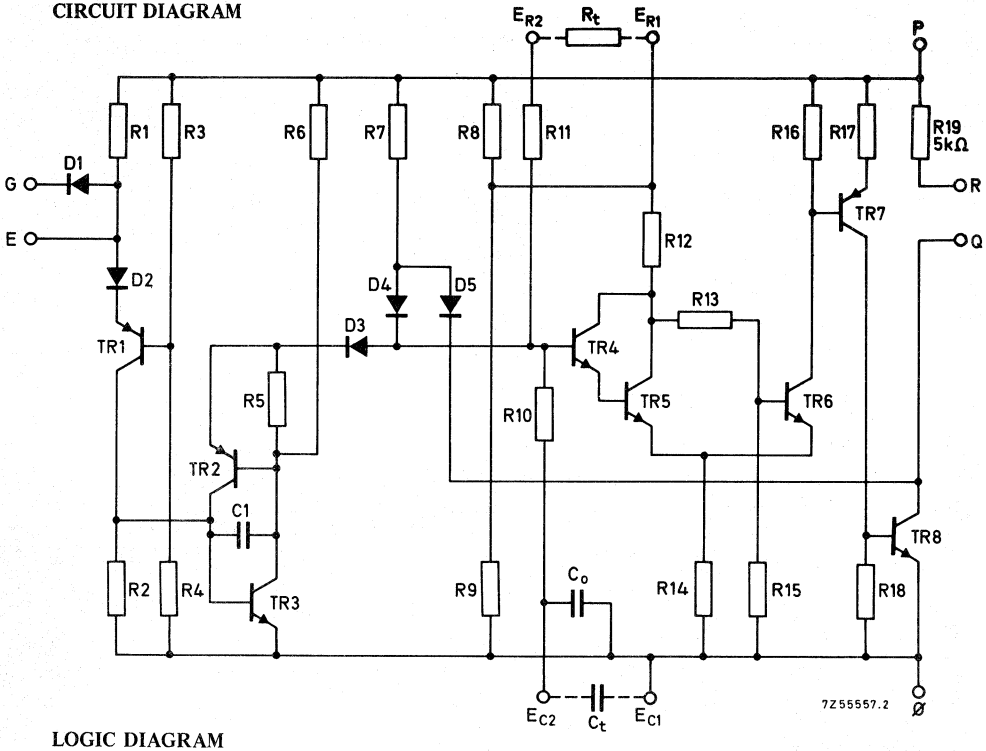




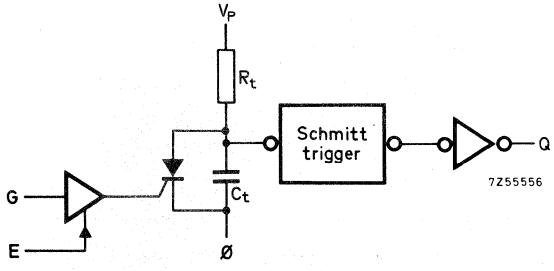
QUICK REFERENCE DATA				
Supply voltage	V_P	11,4 to 17,0		V
Operating ambient temperature	T_{amb}	−30 to +75		°C
Delay time; T_{amb} = 25 °C	t_d	max.	10	s/µF
Available d.c. fan-out (T_{amb} = −25 to +70 °C) LOW state	N_aL	max.	22	
D.C. noise margin at T_{amb} = 25 °C; V_P = 15 V	M_L	typ.	6,5	V
	M_H	typ.	6,5	V
Power consumption at T_{amb} = 25 °C	P_{av}	typ.	300	mW

PACKAGE OUTLINE 20 lead dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC DIAGRAM



GENERAL DESCRIPTION

The TU30 is a direct-coupled timer that gives a constant delay irrespective of the duration of the gate input signal. The delay begins when the gate input changes from HIGH to LOW (see timing diagram). When the gate input changes from LOW to HIGH, the output goes LOW. A gate input signal during a delay cycle wili restart the delay.

The length of the delay is determined by an external capacitor connected across terminals E_{C1} and E_{C2}, and an external resistor connected across terminals E_{R1} and E_{R2}.

The number of gate inputs can be extended by connecting up to 15 diodes (BAW62) to the expander input terminal E (connect anode of diode to terminal E). *)
To prevent capacitive coupling with other lines the connection between the diodes and expander inputs must be as short as possible.

When using the TU30 to drive other members of the FZ/30-Series, interconnect terminals Q and R.

When using it to drive a small relay, connect the relay across terminals Q and P, and leave terminal R unconnected (floating).

When driving an inductive load (also relays), connect a clamping diode (such as a BAW62) across terminals Q and P (anode of diode to terminal Q). *)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_{QH}	max.	V_P	
Output current (Q and R not interconnected)	I_{QL}	max.	46	mA
Input voltages	V_G	max.	18	V
	$-V_G$	max.	1	V
Input current (for negative input voltage)	$-I_G$	max.	2,0	mA
Output capacitance	C_L	max.	500	pF
Storage temperature	T_{stg}	−25 to +85		°C
Operating ambient temperature	T_{amb}	−25 to +70		°C

*) Diode leads should be kept as short as possible.

CHARACTERISTICS Test conditions: T_{amb} = −25 to +70 °C.

	Sym-bol	min.	typ[1])	max.		Conditions and references: V_P (V)	Conditions and references
Static data							
Voltages							
Input HIGH	V_{GH}	6,8	–	–	V	11,4	I_{QL} = 43 mA *)
	V_{GH}	9,3	–	–	V	17,0	I_{QL} = 46 mA **)
Input LOW	V_{GL}	–	–	4,5	V	11,4	V_{QHmin} = 0,9 V_P
	V_{GL}	–	–	7,3	V	17,0	$-I_{QH}$ = 0,25 mA
Output HIGH	V_{QH}	10	13	–	V	11,4	V_{GL} = 4,5 V; $-I_{QH}$ = 0,25 mA
	V_{QH}	15,3	–	–	V	17,0	
Output LOW	V_{QL}	–	–	0,5	V	11,4	V_{GH} = 6,8 V; I_{QL} = 43 mA *); I_{QL} = 46 mA **)
D.C. noise margin: HIGH	M_H	3,2	–	–	V	11,4	V_{GH} = 10 V
LOW	M_L	2,8	–	–	V	11,4	V_{GL} = 1,7 V
HIGH	M_H	–	6,5	–	V	15,0	V_{GH} = 1,4 V
LOW	M_L	–	6,5	–	V	15,0	V_{GL} = 1,0 V
Currents							
Input HIGH	I_{GH}	–	–	1	µA	17,0	V_{GH} = 17,0 V
Input LOW	$-I_{GL}$	–	–	0,95	mA	11,4	V_{GL} = 1,7 V
	$-I_{GL}$	–	–	1,6	mA	17,0	
Output HIGH	$-I_{QH}$	–	–	0,50	mA	11,4	V_{GL} = 4,5 V; V_{QH} = 10 V *)
	$-I_{QH}$	–	–	0,50	mA	17,0	V_{GL} = 7,3 V; V_{QH} = 15,3 V *)
Output LOW	I_{QL}	–	–	43	mA	11,4 and 17,0	V_{GH} = 0,6 V_P; V_{QL} = 0,5 V *)
	I_{QL}	–	–	46		11,4 and 17,0	V_{GH} = 0,6 V_P; V_{QL} = 0,5 V **)
Supply data							
Currents							
Output HIGH	I_P	–	6,5	7,5	mA	17,0	V_G = 0 V
Output LOW	I_P	–	17	20	mA	17,0	V_G = 17 V

1) Typ. values specified at V_P = 15 V and T_{amb} = 25 °C.
*) Terminal R connected to terminal Q.
**) Terminal R not connected.

CHARACTERISTICS at V_P = 15 V; T_{amb} = 25 °C

Dynamic data

Gate input HIGH duration	T_{GH}	>	5	µs	
Output rise time for C_L = 10 pF	t_{Qr}	typ.	110	ns	1)
Output fall time for R_C = 5 kΩ; C_L = 10 pF	t_{Qf}	typ.	50	ns	
Fall propagation delay time	t_{pdf}	typ.	3	µs	
Delay time (C_t in F; R_t in Ω)	t_d	>	1	ms	
		typ.	$C_t(R_t + 10\,k\Omega)$	s	
Timing resistor	R_t		0 Ω to 10	MΩ	
Timing capacitor	C_t		no limit		2)
Change in delay time versus temperature (R_t = 1 MΩ; V_P = 15 V)		typ.	−0,1	%/°C	
Change in delay time versus supply voltage (T_{amb} = 25 °C; R_t = 1 MΩ)		typ.	−0,5	%/°C	

1) t_{Qr} = (11 x C_L) ns. C_L is the wiring capacitance in pF with a maximum permissible value of 500 pF.

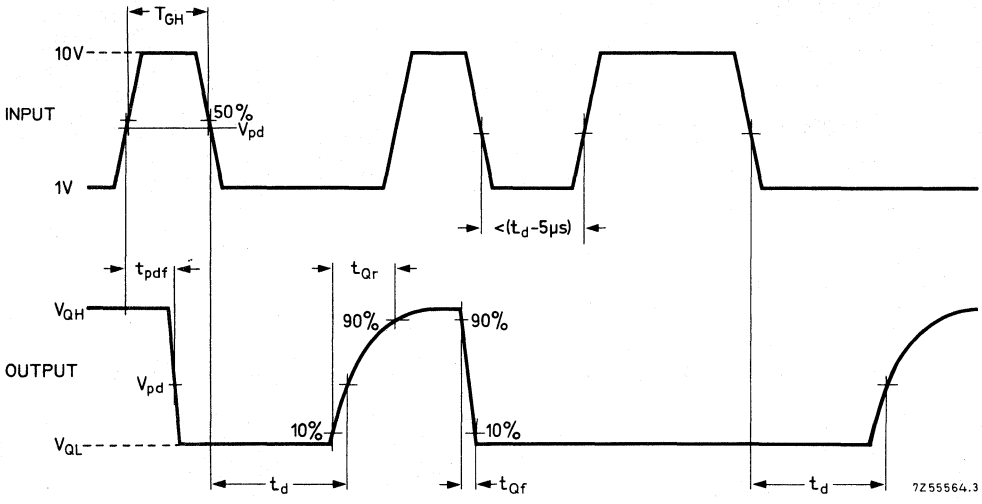
2) Preferred value for C_t: > 1 nF.
The circuit is not developed for electrolytic capacitors because of their high leakage currents. However, electrolytic capacitors may be used (+ side connected to terminal E_{C2}), provided that the charge current is large compared to the leakage current of the capacitor e.g.:

$$I_{charge} > 10.I_{leakage}$$

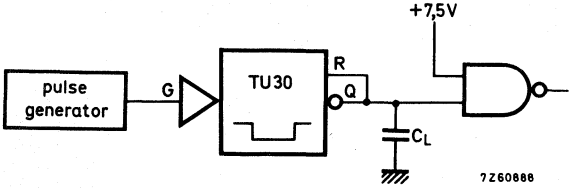
$$\text{where } I_{charge} = \frac{0,3\,V_P}{R_t + 10\,k\Omega}$$

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns
t_f = 120 ns
t_{GH} = 5 µs
V_{pd} = 4,5 V



Measuring conditions: V_P = +15 V
C_L = 10 pF (including probe and jig capacitance)
T_{amb} = +25 °C

Waveforms and loading circuit illustrating measurement of t_{Qr}, t_{Qf} and t_{pdf}.

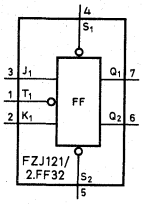
Accessories for HNIL FZ/30-Series

STICKERS

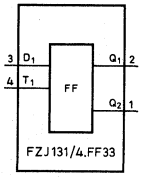
The drawing of circuit diagrams is simplified by the use of stickers of the drawing symbols of the FZ/30-Series. These stickers, printed on self-adhesive transparant material, are available in sheets. Each sticker can be separately detached from the sheet without cutting.

sheets with symbols for type	catalogue number for 25 sheets	symbols per sheet
FZH101/4.NAND32 FZH111/4.NAND30 FZH121/2.NAND30 FZH131/2.NAND31 FZH141/2.NAND32	4322 026 75420	5 x NAND 10 x NAND* 10 x OR* ● 5 x OR ●
FZH151/2.AOR30	4322 026 75460	12 x
FZH161/4.LI31 FZH171/2.NAND33 FZH181/4.LI30 FZH191/3.NAND33 FZH201/6.IN30 FZH211/4.NAND34 FZH231/2.NAND35	4322 026 75420	5 x NAND 10 x NAND* 10 x OR* ● 5 x OR ●
FZH241/2.AST30	4322 026 74350	9 x
FZH251/4.AND30 FZH261/2.N-4.I30 FZH271/4.EO30 FZH281/4.NOR30 FZH291/4.OR30	4322 026 74380	5 x AND 5 x OR 5 x NOR 5 x EXCLUSIVE-OR 5 x INVERTER
FZJ101/FF30	4322 026 75430	15 x
FZJ111/FF31	4322 026 75440	15 x
FZJ121/2.FF32	4322 026 74100	8 x
FZJ131/4.FF33	4322 026 74110	4 x
FZJ141/FF34 FZJ151/FF35	4322 026 74120	12 x
FZJ161/FF36	4322 026 74360	12 x
FFK101/OS30	4322 026 75450	6 x
FZL101/ND30	4322 026 74370	12 x
TU30	4322 026 75450	10 x
2.LRD30	4322 026 75490	12 x
PA30	4322 026 75480	16 x

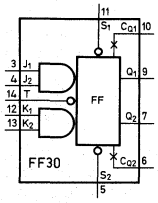
*With slow-down terminal.
●With inverted inputs.



4322 026 74100



4322 026 74110



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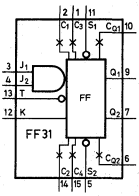

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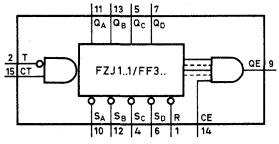

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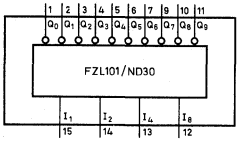

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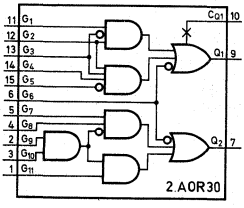
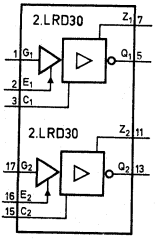


4322 026 75460



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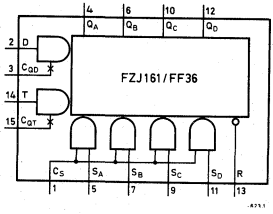
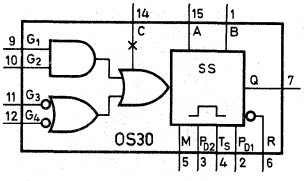
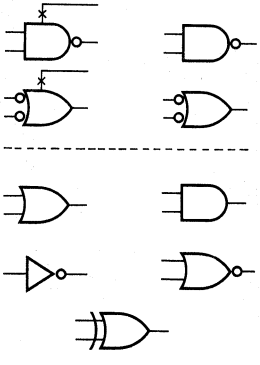


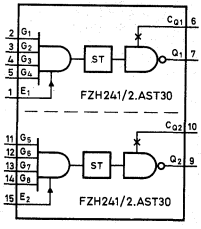
4322 026 74370

4322 026 75450

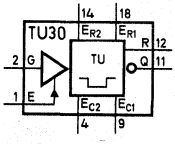


4322 026 75420





4322 026 74350



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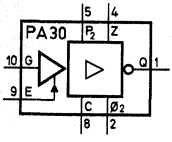


4322 026 75480

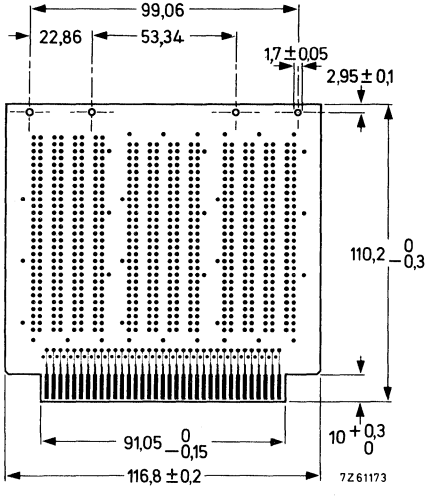
4322 026 74380

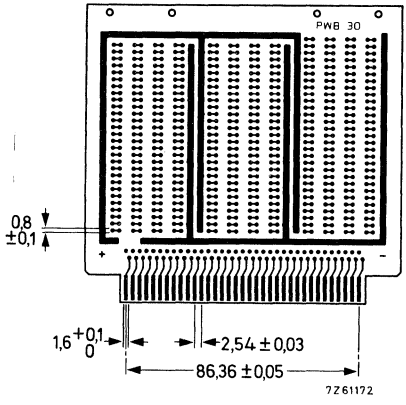
EXPERIMENTERS' PRINTED-WIRING BOARD

for integrated circuits in dual-in-line package

This printed-wiring board has been designed for dual-in-line packages with a different number of pins; the packages are connected with each other and with the connector by means of insulated wires. The packages are mounted perpendicular to the connector, so the wires to the connector can run parallel to the rows of pins of the packages, instead of between the pins.
The maximum number of packages which can be mounted is given below:

number of pins of the package	max. number of packages per board
2 x 7	24
2 x 8	18
2 x 9	18
2 x 10	12
2 x 11	12





Material	glass-epoxy
Board thickness	1,6 mm
Holes	plated-through, 0,8 mm diameter, provided with soldering lands
Contact pads	2 x 35, gold-plated

OBSOLESCENT

All types mentioned in this chapter are obsolescent. They are available until present stocks are exhausted.

NORBITS 60-SERIES, 61-SERIES, 90-SERIES

INTRODUCTION

Our NORbits which use NOR logic as a basis of operation, represent an important advance in static switching devices for industrial control systems. The units of the 61-series facilitate using NORbits in thyristorized power control circuits; the units of the 90-series operate on the principle of trigger logic (that is, the units are driven by voltage transients in contrast with those of the 60-series which respond to voltage level), and the 90-series units allow the building of assemblies such as counters and shift registers simply and economically. They are so designed as to have a high noise immunity. However, care must be taken to avoid capacitive and inductive cross-talk between connecting wires.

The units have the following features in common:

- Single rail 24 V ± 25% supply, allowing the use of an inexpensive power supply — which helps to keep the cost down, particularly in small systems.
- Transfer moulded cases, giving optimum protection.
- Rigid terminals spaced at 0,2 in. pitch, permitting a variety of interconnection methods to be used (dip soldering, hand soldering, miniwire wrapping).
- Exceptionally good noise immunity.
- Easy to understand level logic, making it possible to carry out system tests with only a d.c. voltmeter.
- Silicon semiconductors throughout, ensuring reliable operation down to −10 °C and up to + 70 °C.
- Easy-to-use loading table for system design.

Compatible input and output devices as well as a full range of mounting accessories are available.

The following circuit blocks are available:

60-series *

2.NOR60	Dual 4-input NOR gate
4.NOR60	Quadruple 2 x 2 + 2 x 3 input NOR gate
2.IA60	Dual inverter amplifier
2.LPA60	Dual low power amplifier
TU60	Timer unit
2.ASF60	Dual active switch filter
HPA60	High power amplifier
GLD60	Grounded load driver

61-series *

2.NOR61	Dual NOR-gate with diode-resistor networks
RSA61	Rectifier and synchronization assembly
UPA61	Universal power amplifier
TT61	Dual thyristor trigger transformer

90-series

FF90	Flip-flop
2.TG90	Twin-trigger gate
PS90	Pulse shaper

* The types 2.SF60 (succeeded by 2.ASF60), and DOA61 are obsolete.

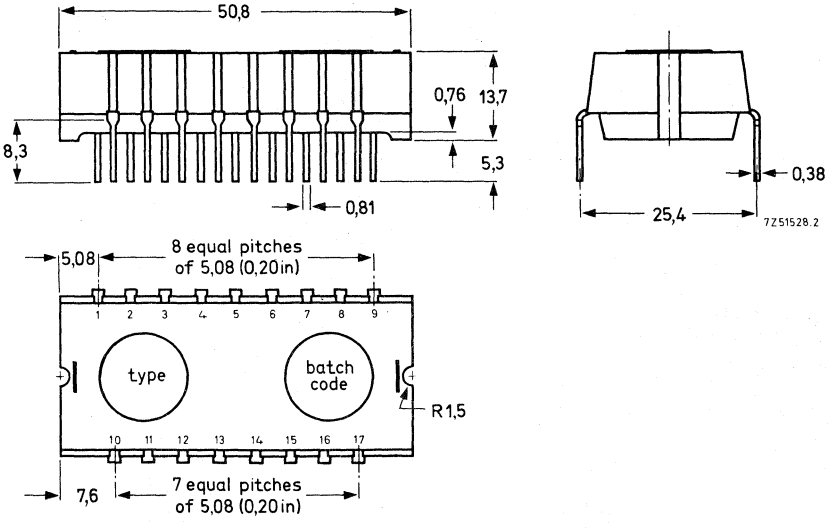
CONSTRUCTION

The circuit elements are housed in a transfer moulded encapsulation. The dimensions are as shown below. The pin connections for each unit are shown in the relevant data sheets. Pin numbering is moulded on both top and bottom of the unit. All pins are also accessible from the top of the unit to facilitate test requirements.

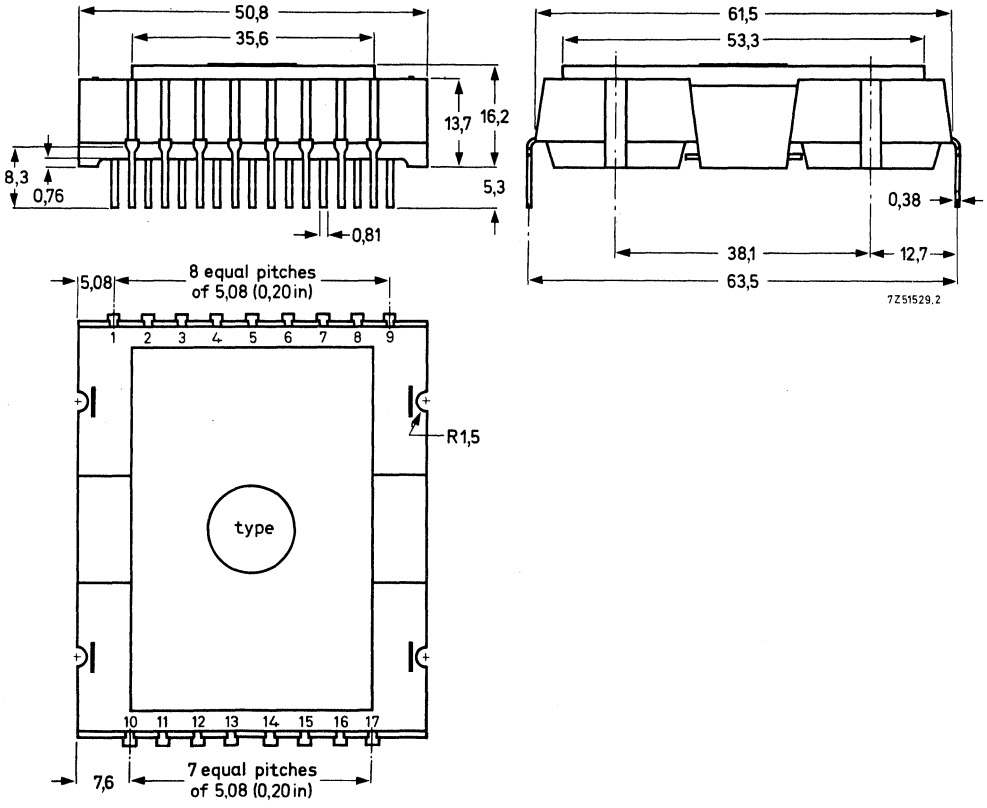
Mounting

The units may be mounted on printed-wiring boards, and a range of these is available with suitable metal mounting chassis. They may also be clamped in the moulded Universal Mounting Chassis UMC60 or fixed with 3 mm screws.

Dimensions in mm (inch equivalents within brackets).



Size A (all types except HPA60).



Size B (type HPA60).

Terminals	suitable for soldering and miniwrap
Wrap tool	Gardner Denver, bit number 506633
Wrap wire size	0,3 mm (0,012" = 28 U.S. gauge = 30 s.w.g.)
Mass	
size A	30 g approx.
size B	85 g approx.
Colour coding	see data sheets of the units

CHARACTERISTICS AND DEFINITIONS

AMBIENT TEMPERATURE LIMITS

Storage	T_{amb} = −40 °C to + 85 °C
Operating	T_{amb} = −10 °C to + 70 °C

SUPPLY VOLTAGE (V_S)

Single rail, + 24 V d.c. ± 25% (18 to 30 V) or
Single rail, + 12 V d.c. ± 5% (11,4 to 12,6 V) at reduced ratings (except 90-series).

LOGIC LEVELS

The operation of the NORbits is based on positive logic, i.e. "1" level is a positive voltage that is more positive than "0" level, and "0" level is independent of supply voltage. Logic "1" depends upon supply and loading of the output of the logic functional block.

Levels with V_S = 24 V ± 25%

0 V < "0" < + 0,3 V
11,4 V < "1" < V_S

Levels with V_S = 12 V ± 5% *

0 V < "0" < + 0,3 V
8,3 V < "1" < V_S

FAN OUT

Number of drive units that can be delivered by a logic function without exceeding the "1" level limits as defined above. The fan out actually indicates the number of NOR gates that can be driven into saturation (thereby bringing the respective outputs to "0" level).

60- AND 61-SERIES

D.C. NOISE IMMUNITY

"0" level immunity

A d.c. voltage of + 1 V with respect to the 0-volt line, applied to any one input (the other inputs floating) will not cause a change of output voltage.

"1" level immunity

a. With a supply voltage of 24 V ± 25%: A variation of 2 V of the "1" input level will not cause a unit to change its output voltage.

b. With a supply voltage of 12 V ± 5%: A variation of 0,25 V of the "1" input level will not cause a unit to change its output voltage.

DRIVE UNIT

Drive required on one input of a NOR60 (with all other inputs returned to the 0-volt line) to bring the output to "0" level (less than + 0,3 V).

* Not applicable to 90-series.

90-SERIES

TRIGGERING EDGE

The unit FF90 is driven by a negative-going transient (from "1" to "0" level). The maximum duration of the transient, unless specified otherwise, is 3 μs.

DRIVE UNIT (D.U.)

Drive required on reset input of FF90 to bring output Q1 to "1" level.*

ZERO UNIT (Z.U.)

Half the drive at "0" level required on one T terminal to trigger an FF90 unit.

* This drive unit has also been specified as the drive required on one input of a NOR60 (with all other inputs returned to the 0-volt line) to bring the output to "0" level.

INPUT AND OUTPUT DATA

EXTENSION OF THE DRIVE UNIT CONCEPT

System design is greatly simplified by expression of the input requirements and fan out capabilities of the various units in integral multiples of drive units (D.U.) and, for 90-series, circuit blocks also in zero units (Z.U.). To check that the loadability of a particular unit is not exceeded simply add the number of D.U.s (or Z.U.s) present at its output.

The table opposite shows the number D.U.s and Z.U.s that can be delivered by the different units of the 60 and 90-series.

LOADING TABLE

The data sheets of the units give impedances and current requirements for matching non-standard input signals to 60 and 61-series inputs as well as matching non-standard loads.

unit		input	output capability at V_s =		
			12 V ± 5%	24 V ± 25%	24 V ± 25%
			"1" level	"1" level	"0" level
2.NOR60,	per function *	1 D.U.	4 D.U.	6 D.U.	12 Z.U.
4.NOR60,	per function **	1 D.U.	4 D.U.	6 D.U.	0 Z.U.
2.IA60,	per function ▲	2 D.U.	13 D.U.	20 D.U.	50 Z.U.
2.IA60,	connected as Low Power Amp.	2 D.U.	$R_{load} \geqslant 150\ \Omega$	$R_{load} \geqslant 300\ \Omega$	–
2.LPA60	per function **	2 D.U.	$R_{load} \geqslant 150\ \Omega$	$R_{load} \geqslant 300\ \Omega$	0 Z.U.
HPA60		1 D.U.	$R_{load} \geqslant 6\ \Omega$	$R_{load} \geqslant 13{,}5\ \Omega$	–
TU60	**	1 D.U.	3 D.U.	5 D.U.	0 Z.U.
2.ASF60,	per filter **	100 $V_{d.c.}$	2 D.U.	2 D.U.	0 Z.U.
GLD60,	NOR function	1 D.U.	–	6 D.U.	
	GLD function	2 D.U.	–	900 D.U.	
PS90		–	–	6 D.U.	80 Z.U.
FF90		2 Z.U.	–	5 D.U.	7 Z.U.

* 2 inputs of the NOR must be connected in parallel. Signal must be derived from a chain of units that includes either a PS90, an FF90 or a TU60.

** No Z.U. available, therefore these units must not be used to drive an FF90 or 2.TG90 directly.

▲ IA60 driven by an IA60. Both the inverting and non-inverting connections can be used, but pins 5 and 6 must be interconnected. Signal must be derived from a chain of units that includes either a PS90, and FF90 or a TU60.

TEST SPECIFICATIONS

All units meet the following test specifications.

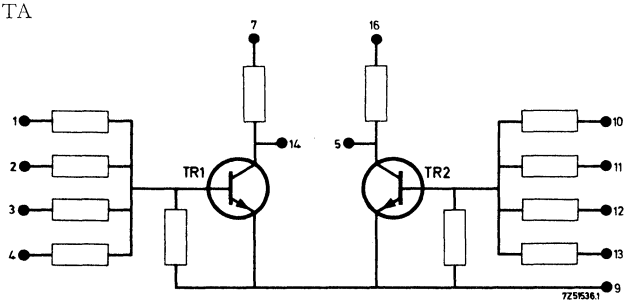
Test	IEC 68	MIL-STD-202C
Dry heat life test	56 days at max. diss. max. temp. check at: 0-10/14d-56d.	Method 108A, Cond. D; check at 0-10/14d-56d.
Long-term damp heat non-operating	Test C, 56 days check at 0-10/14d-56d.	Method 103B, Cond. D; check at 0-10/14d-56d.
Long-term damp heat operating	Test C, 56d. min., diss., check at 0-10/14d-56d.	Method 103B, Cond. D; check at 0-10/14d-56d.
Temp. cycle test	Test Na, 30 min., 2-3 min. in between; preferred: −40 °C; + 85 °C.	Method 107B, Cond. A; moderate temp.
Vibration	Test Fb; 10-500-10 Hz, 1 octave/min.; amplitude 0,75 mm max.; 10g max. 3 x 3 h.	Method 204A, Cond. A; 10-500-10 Hz, 15 min.; amplitude 0,75 max.; 10g max., 3 x 3 h.
Shock	–	Method 202B, 3 blows 50g.
Robustness of terminations	Test $U_A + U_B$.	Method 211A + (B or C).
Solderability + solder heat	Test T; at 0 h and at 56d; no electrial test.	Method 210, at 0 h and at 56d; no electrical test.
Corrosion resistance	1% SO_2 solution, 95% R.H., 35 °C, 1 day. Recovery 27 days.	

DUAL FOUR INPUT NOR GATE

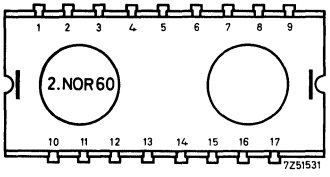
Function: dual NOR (positive logic)

Case: size: A; colour: black

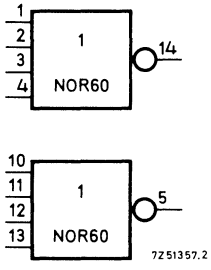
CIRCUIT DATA



Circuit diagram



Terminal location



Drawing symbols

1, 2, 3, 4	= input NOR 1
5	= output NOR 2
6	= n.c.
7	= for supply NOR 1 (V_S)
8	= n.c.
9	= 0 V common
10, 11, 12, 13	= input NOR 2
14	= output NOR 1
15	= n.c.
16	= for supply NOR 2 (V_S)
17	= n.c.

The unit contains two identical transistor-resistor NOR circuits. Each circuit has 4 inputs. If any input of a NOR is at "1" level the output of that NOR will be at "0" level.

CHARACTERISTICS

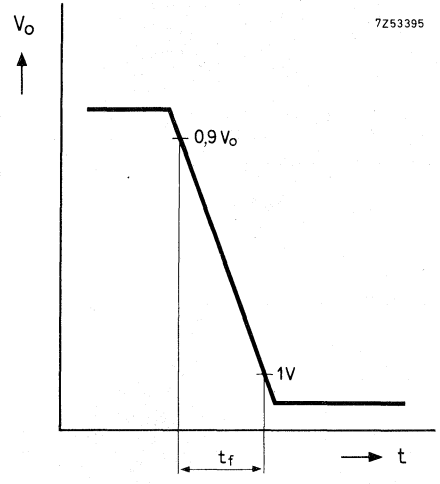
	at V_S = 24 V ± 25%	at V_S = 12 V ± 5%
Supply current at V_S nom	3,5 mA	1,75 mA
at V_S max	≤ 4,8 mA	≤ 1,95 mA
Input requirement	1 D.U.	1 D.U.
Output capability	6 D.U.	4 D.U.

	single input	two paralleled inputs	three paralleled inputs	four paralleled inputs
Input impedance [1]	90 kΩ	50 kΩ	35 kΩ	30 kΩ
Input current for "0" output [1][2]	0,13 mA	0,125 mA	0,.11 mA	0,1 mA

Switching speed

Fall time defined below $t_f \leq 1,25\ \mu s$

Fall delay time defined below $t_{fd} \leq 6\ \mu s$



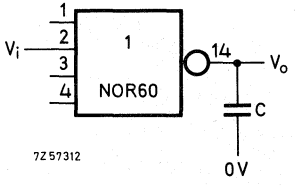
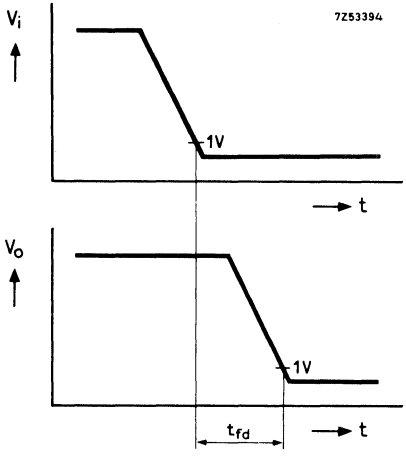


Fig. A

The fall time t_f is defined as the time required for the output voltage V_o to change from 90% of its full value to 1 V after application of a step input, the output being loaded with C = 200 pF (see Fig. A).

1) Unused inputs returned to 0-volt line.
2) At V_S = 30 V,



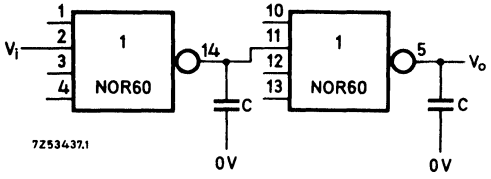


Fig.B

The fall delay time t_{fd} is defined as the time between the 1 V points of the negative-going input and output voltages of two cascaded NORs, each being loaded with C = 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur when these values are exceeded)

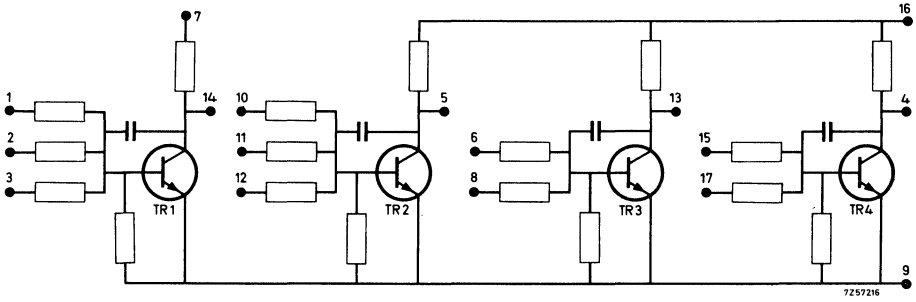
Supply voltage	V_S	max. 30	$V_{d.c.}$
		min. 0	V
Positive transient on V_S		max. 10	V during 10 μs
Positive input voltage	$+V_i$	max. 90	V
Negative input voltage	$-V_i$	max. 18	V

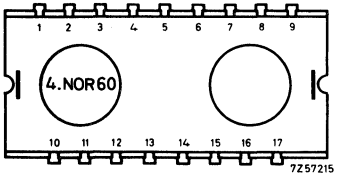
QUADRUPLE 2×2 + 2×3 INPUT NOR GATE

Function: quadruple NOR (positive logic)

Case: size: A; colour: black

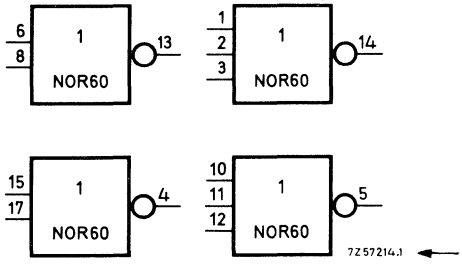
CIRCUIT DATA





Terminal location

1, 2, 3 = input NOR 1
4 = output NOR 4
5 = output NOR 2
6, 8 = input NOR 3
7 = for supply NOR 1 (V_S)
9 = 0 V common
10, 11, 12 = input NOR 2
13 = output NOR 3
14 = output NOR 1
15, 17 = input NOR 4
16 = for supply NOR 2, 3, 4 (V_S)



Drawing symbols

The unit contains two identical 2-input and two identical 3-input NOR circuits. If any input of a NOR is at "1" level the output of that NOR will be at "0" level.

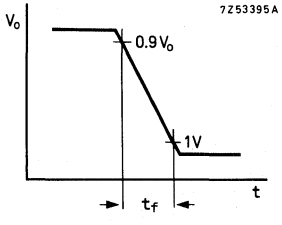
CHARACTERISTICS

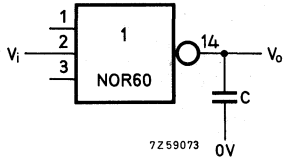
	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$	3,5 mA	1,75 mA
at $V_{S\,max}$	≤ 4,8 mA	≤ 1,95 mA
Input requirement	1 D.U.	1 D.U.
Output capability	6 D.U.	4 D.U.

	single input	two paralleled inputs	three paralleled inputs
Input impedance [1])	90 kΩ	50 kΩ	35 kΩ
Input current for "0" output [1][2])	0,13 mA	0,125 mA	0,11 mA

Switching speed

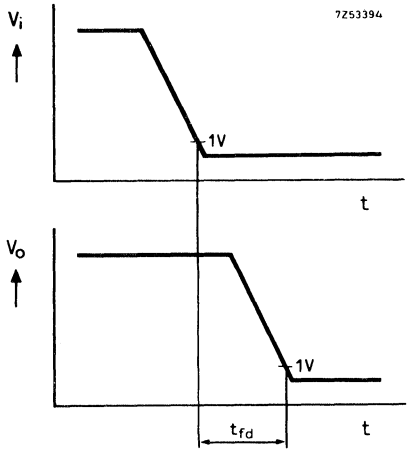
Fall time defined below	t_f ≤ 14 μs
Fall delay time defined below	t_{fd} ≤ 26 μs





The fall time t_f is defined as the time required for the output voltage V_O to change from 90% of its full value to 1 V after application of a step input, the output being loaded with C = 200 pF (see Fig. A).

[1]) Not used inputs returned to 0-volt line.
[2]) At V_S = 30 V.



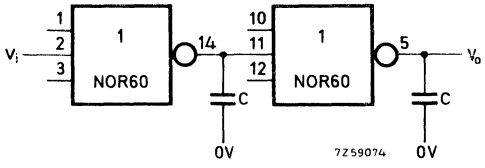


Fig.B

The fall delay time t_{fd} is defined as the time betweeb the 1 V points of the negative-going input and output voltages of two cascaded NORs, each being loaded with C = 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur when these values are exceeded)

Supply voltage	V_S	max. 30 V min. 0 V	$V_{d.c.}$
Positive transient on V_S		max. 10 V for 10 μs	
Positive input voltage	$+V_i$	max. 90 V	
Negative input voltage	$-V_i$	max. 24 V	

DUAL INVERTER AMPLIFIER

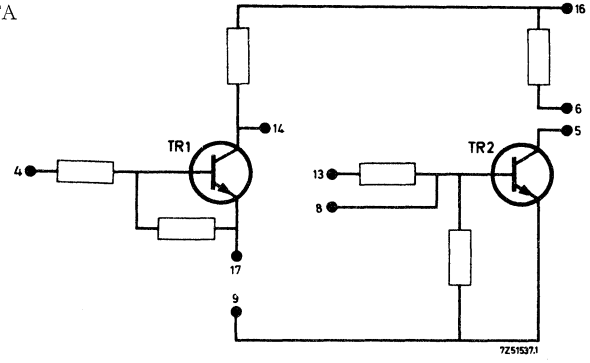
Function

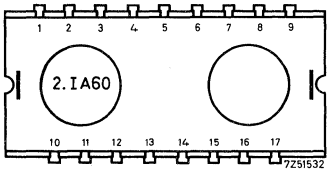
The unit comprises two identical Inverter Amplifiers. Use as a single inverting Low Power Amplifier is feasible.

Case

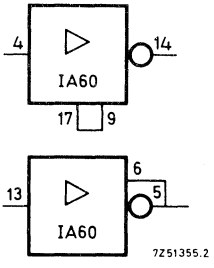
Size:A; colour: blue

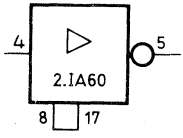
CIRCUIT DATA





Terminal location





Drawing symbols with important connections

1, 2, 3 = n.c.
4 = input IA 1
5 = output IA 2
6 = collector resistor IA 2
7 = n.c.
8 = base of IA 2 transistor
9 = 0 V common
10, 11, 12 = n.c.
13 = input IA 2
14 = output IA 1
15 = n.c.
16 = for supply (V_S)
17 = emitter of IA 1 transistor

To obtain the dual I.A., pin 17 should be connected to pin 9 and pin 6 to pin 5. A "1" level input (pin 4 or 13) will cause a "0" level output (pin 14 or 5-6 respectively).
To obtain the inverting L.P.A., pin 17 should be connected to pin 8 and the load connected between pins 5 and 16. When pin 4 is at "1" level, pin 5 will be at "0" level.

Notes to the load of the L.P.A.

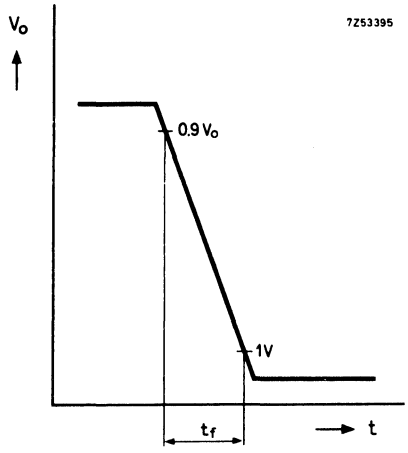
1. Care should be taken that the value of a varying load should not drop below the specified minimum.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks upon switching off. To avoid destruction the load should be provided with a flywheeling diode, type BAX12. The anode should be connected to pin 5, the cathode to pin 16 (positive supply).

CHARACTERISTICS

	at V_S = 24 V ±25%		at V_S = 12 V ±5%	
	per I.A.	as L.P.A.	per I.A.	as L.P.A.
Supply current at $V_{S\,nom}$	10,9 mA	10,9 mA + I_{load}	5,5 mA	5,5 mA + I_{load}
Supply current at V_S max and "1" input	≤ 15,5 mA	≤ 114 mA R_{load} = 300 Ω	≤ 6,5 mA	≤ 89,9 mA R_{load} = 150 Ω
Input requirement	2 D.U.	2 D.U.	2 D.U.	2 D.U.
Output capability	20 D.U.	140 D.U. [1]	13 D.U.	
Minimum load resistance		300 Ω [1]		150 Ω [1]

Input impedance		45 kΩ
Input current for "0" output of I.A. at V_S = 30 V		0,285 mA
Switching speed		
Fall time defined below	t_f	≤ 1 μs
Fall delay time defined below	t_{fd}	≤ 3 μs

[1]) This load is permissible only if the input switched between "0" and "1" levels by a preceding 60 Series unit or other true digital input, avoiding excessive dissipation during transitions.



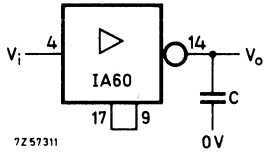
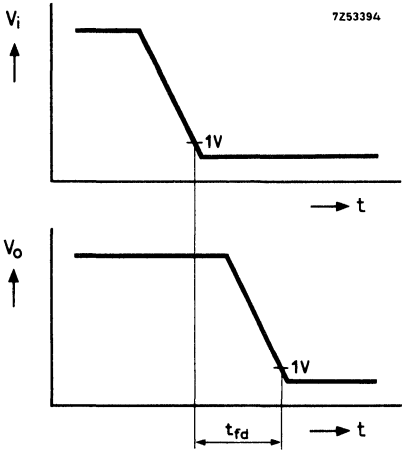


Fig.A

The fall time t_f is defined as the time required for the output voltage V_O to change from 90% of its full value to 1 V, after application of a step input, the output being loaded with C = 200 pF (see Fig.A).



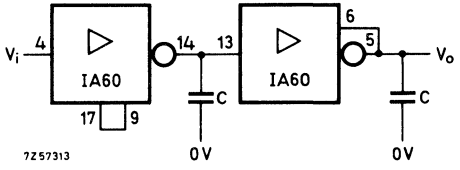


Fig.B

The fall delay time t_{fd} is defined as the time between the 1 V points of the negative-going input and output voltages of two cascaded Inverter Amplifiers, each being loaded with 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur if these values are exceeded)

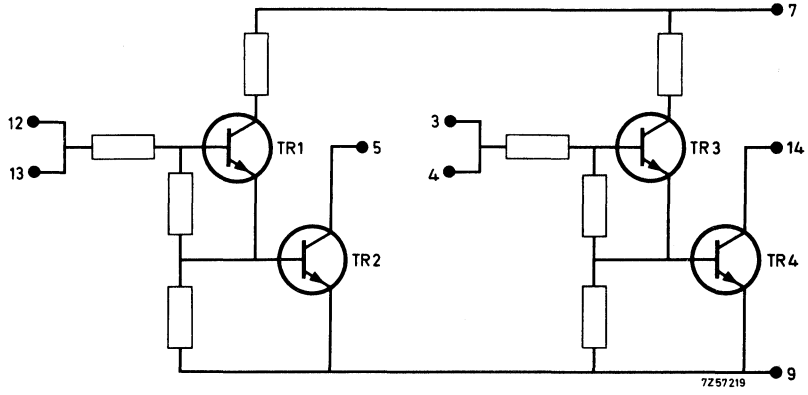
Supply voltage	V_s	max.	30	$V_{d.c.}$
		min.	0	V
Positive transient on V_s		max.	10	V during 10 μs
Positive input voltage	$+V_4$, $+V_{13}$	max.	70	V
Negative input voltage	$-V_4$, $-V_{13}$	max.	16	V
Positive voltage at pin 8	$+V_8$	max.	4	V via min. 500 Ω
Negative voltage at pin 8	$-V_8$	max.	5	V

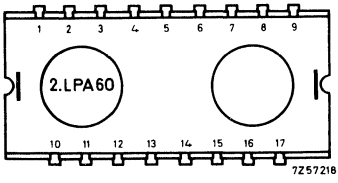
DUAL LOW POWER AMPLIFIER

Function — The unit comprises two identical inverting Low Power Amplifiers

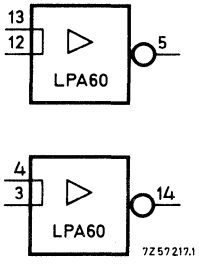
Case — size: A; colour: blue

CIRCUIT DATA





Terminal location



Drawing symbols

1, 2	= n.c.
3, 4	= input LPA2
5	= output LPA1
6	= n.c.
7	= for supply (V_S)
8	= n.c.
9	= 0 V common
10, 11	= n.c.
12, 13	= input LPA1
14	= output LPA2
15, 16, 17	= n.c.

The load should be connected between pins 5 and 7 for LPA1 and between pins 14 and 7 for LPA2.
When the input (12/13 or 3/4) is at "1" level, the output (5 or 14) will be at less than 1 V. This being no true "0" level, it is not recommended to use an LPA as a logic operator.

Notes to the loading

1. Care should be taken that the value of a varying load should not drop below the specified minimum.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks upon switching off. To avoid destruction the load should be provided with a flywheeling diode, type BAX12. The anode should be connected to pin 5 (14), the cathode to pin 7 (positive supply).

CHARACTERISTICS

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$, I_{load} = 0 mA	8 mA	4 mA
Supply current at $V_{S\,max}$ and "1" input, R_{load} = 300 Ω	≤ 108 mA	–
R_{load} = 150 Ω	–	≤ 89.9 mA
Input requirement	2 D.U.	2 D.U.
Output capability	100 mA	80 mA
Min. load resistance	300 Ω	150 Ω

Input impedance		45	kΩ
Input current for "0" output at V_S = 30 V		0.285	mA
Output voltage at "1" input		< 1	V
► Switching speed			
Fall time (Fig.A)	t_f	≤ 0.4	μs
Rise time (Fig.B and Fig.C)	t_r	≤ 2	μs
Storage time (Fig.B and Fig.C)	t_s	≤ 10	μs

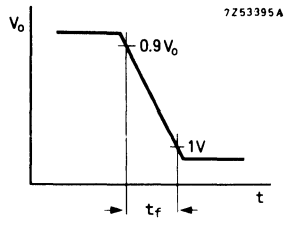


Fig.A

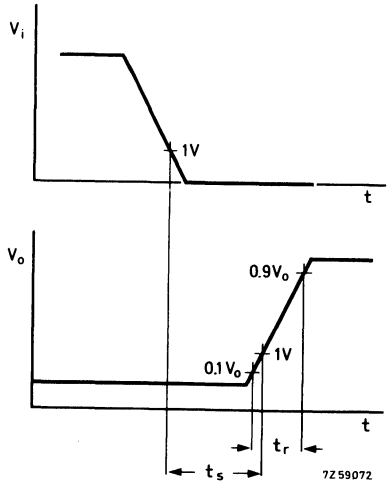


Fig.B

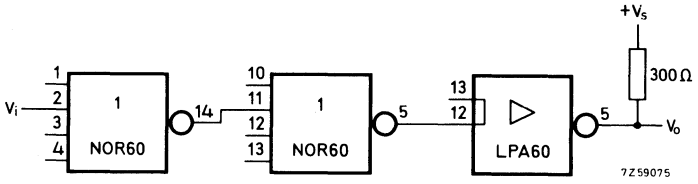


Fig.C

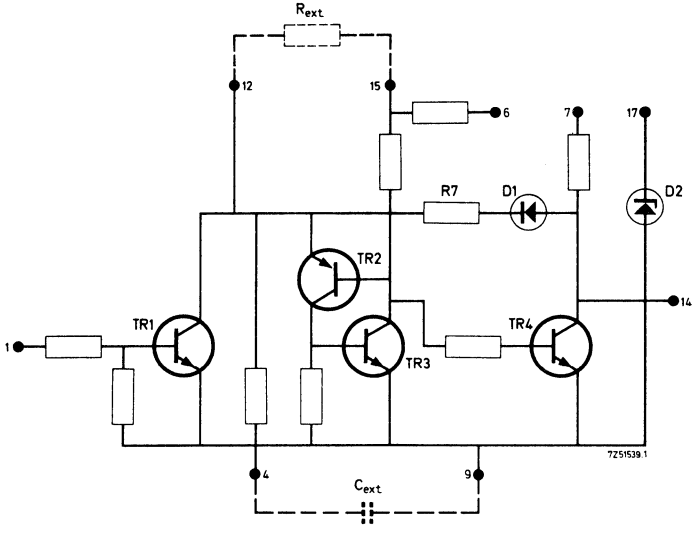
LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage	V_S	max. 30	$V_{d.c}$
		min. 0	V
Positive transient on V_S		max. 10	V for 10 μs
Positive input voltage	$+V_i$	max. 70	V
Negative input voltage	$-V_i$	max. 16	V

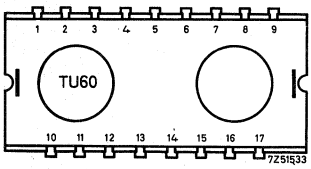
TIMER

Function	Gives an inverted output. The output of a "1" is delayed following a "0" input. No delay occurs when the input returns to "1"
Case	Size: A; colour: red

CIRCUIT DATA

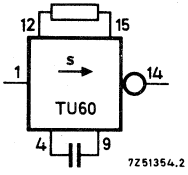


With the input at "1" the capacitor (C_{ext}) is discharged. When the input goes to "0", TR_1 ceases to conduct so that the capacitor is allowed to slowly charge until the base potential of TR_2 is exceeded. TR_2 starts to conduct and provides base current for TR_3, which speeds the turn-on of TR_2. TR_4 ceases to conduct and the output level changes from "0" to "1". Positive feedback is provided via D_1 and R_7.



Terminal location

1	= input	10, 11	= n.c.
2, 3	= n.c.	12	= for external resistor
4	= for external capacitor	13	= n.c.
5	= n.c.	14	= output
6	= see instructions below	15	= for external resistor
7	= positive supply	16	= n.c.
8	= n.c.	17	= see instructions below
9	= 0 V common		



Drawing symbol with significant connections

Instructions for connection of the supply

When V_S = 24 V ±25% : connect 6 and 7, connect 15 and 17.

When V_S = 12 V ±5% : connect 15 and 7, do not connect 6 and 7.

CHARACTERISTICS

	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at $V_{S\,nom}$	6.9 mA	1.9 mA
at $V_{S\,max}$	10.1 mA	2.1 mA
Input requirement	1 D.U.	1 D.U.
Output capability	5 D.U.	3 D.U.

Input impedance	90 kΩ
Input current for "0" output, at V_S = 30 V	0.125 mA
External resistance	R_{ext} min. 100 kΩ, max. 1 MΩ
Leakage current of external capacitor when connected between	
pins 4 and 9	max. 100 nA at 10 V
pins 15(+) and 4	max. 100 µA at 25 V

Delay time (see Fig.A)	t_{delay}	about R_{ext} C_{ext} s ($M\Omega$ x μF) [1]
Max. change of delay time with temperature (C_{ext} pins 4 and 9)		- 0,14 %/°C
Switching speed		
Fall time as defined below	t_f	$\leq$ 1 μs
Rise time as defined below	t_r	$\leq$ 6 μs
Timing requirements (see Fig.A)		
Set time	t_{set}	min. 11,9 C_{ext} ms (C_{ext} in μF)
Recovery time	t_{sec}	min. 11,9 C_{ext} ms
Start inhibit before end of delay	$t_{st\ inh}$	min. 18,9 C_{ext} ms
Inhibit duration	t_{inh}	min. 18,9 C_{ext} ms (A shorter t_{inh} gives a shorter delay)

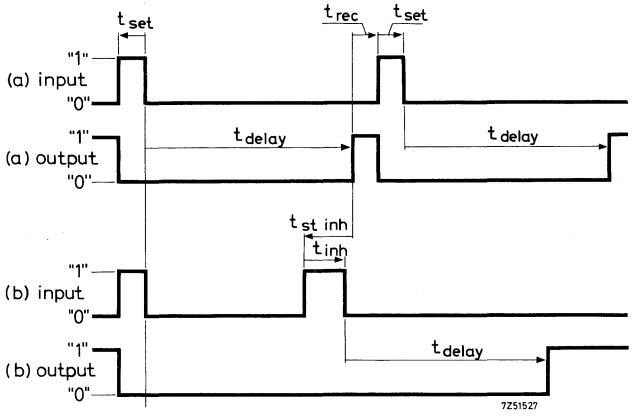


Fig.A

[1]) For long delay times the 25 μF, 160 V_{rms} film capacitor, catalogue number 2222 325 50256 is recommended.

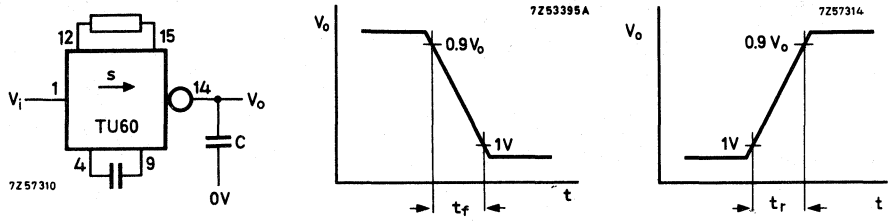


Fig.B

The fall time t_f is defined as the time required for the output voltage V_O to change from 90% of its full value to 1 V, after application of a step input and being loaded with C = 200 pF (see Fig.B).

The rise time t_r is defined as the time required for the output voltage V_O to change from 1 V to 90% of its full value, after application of a step input and being loaded with C = 200 pF (see Fig.B).

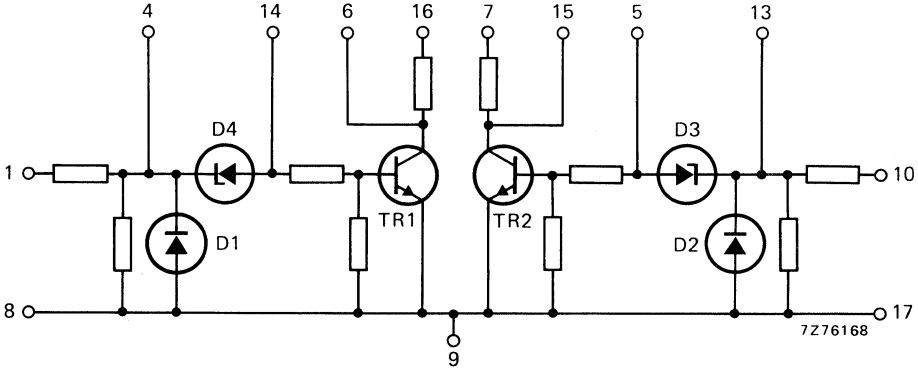
LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply	V_s	max. 30 $V_{d.c.}$ min. 0 V
Positive transient on V_s		max. 10 V for 10 µs
Positive input voltage	$+V_I$	max. 70 V
Negative input voltage	$-V_I$	max. 16 V
External resistance	R_{ext}	min. 820 Ω

DUAL ACTIVE SWITCH FILTER

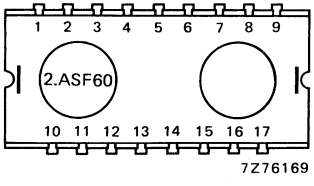
Function	For suppression of interference and to eliminate the effects of contact bounce occurring on mechanical switches.
Case	size: A; colour: black.

CIRCUIT DATA

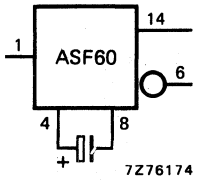


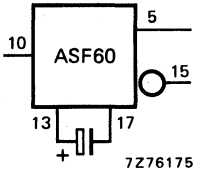
The unit consists of two identical, electrically independent filter circuits, both using an external capacitor. A high voltage is used to break down the contact film resistance of external switches. Non-inverted and inverted outputs are available from each filter, the latter with an increased drive capability.

Terminal location



1	= input ASF1	10	= input ASF2
2, 3	= not connected	11, 12	= not connected
4	= for external capacitor of ASF1	13	= for external capacitor of ASF2
5	= output ASF2	14	= output ASF1
6	= inverted output ASF1	15	= inverted output ASF2
7	= supply (V_S) ASF2	16	= supply (V_S) ASF1
8	= 0 V for external C	17	= 0 V for external C
9	= 0 V common		





Drawing symbols with external capacitor

CHARACTERISTICS (per filter)

Supply voltage (V_S)	+24 V ± 25% or +12 V ± 5%
current	max. 4,8 mA and max. 2,0 mA respectively
Input voltage, logic 1	+100 V ± 25%
logic 0	max. +7,5 V, nom. 0 V
Input current, steady	max. 3,5 mA
surge peak	max. 4,8 mA
Output capability,	
- non-inverting outputs (pin 5 or 14)	2 D.U.
- inverting outputs (pin 15 or 6)	6 D.U.
pin(s) 7 and/or 16 not connected	10 mA sink

The output will switch when the input has been applied for longer than the time shown under "Operation" on next page.

LIMITING VALUES (Destruction may occur if these values are exceeded)

Positive input voltage	+max. 125 V
Negative input voltage	−max. 125 V

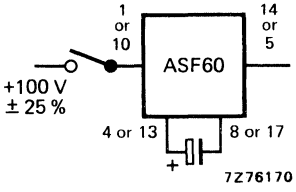
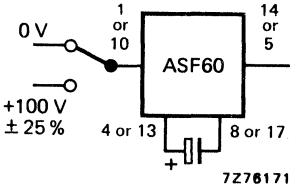
INSTRUCTIONS

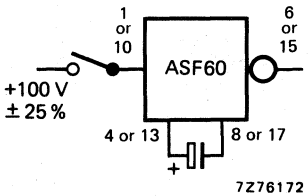
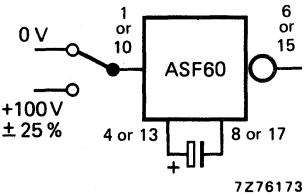
a. Mount the unit as close as possible to the logic system input.

b. The common 0-volt line (pin 9) must be returned to the central earth point of the system to avoid common impedance coupling.

OPERATION

The external capacitor (C) should be connected between the appropriate terminals 4 or 13 and the 0 V terminals 8 or 17. The use of a 100 V electrolytic capacitor is recommended, and its value C in μF may be obtained from the formulae below.

	Non-inverted outputs		Non-inverted outputs	
				
type of contact	single pole/single throw		single pole/double throw	
Tolerable contact bounce time	max.	1,4C ms	max.	1,4C ms
Frequency of operation with 1: 1 mark/space ratio	max.	$\frac{6,3}{C}$ Hz	max.	$\frac{10,6}{C}$ Hz
Time for which input must be at logic '1' to ensure '1' out	min.	42C ms	min.	42C ms
Time for which input must be disconnected (or at 0 V) to ensure '0' out	min.	26C ms	min.	18C ms

Inverted outputs		
type of contact	single pole/single throw	single pole/double throw
Tolerable contact bounce time	max. 1,4C ms	max. 1,4C ms
Frequency of operation with 1 : 1 mark/space ratio	max. $\frac{5,7}{C}$ Hz	max. $\frac{10,6}{C}$ Hz
Time for which input must be at logic '1' to ensure '0' out	min. 29C ms	min. 29C ms
Time for which input must be disconnected (or at 0 V) to ensure '1' out	min. 87C ms	min. 45C ms

HIGH POWER AMPLIFIER

Function	Power Amplifier for load switching
Case	Size: B; colour: black

CIRCUIT DATA

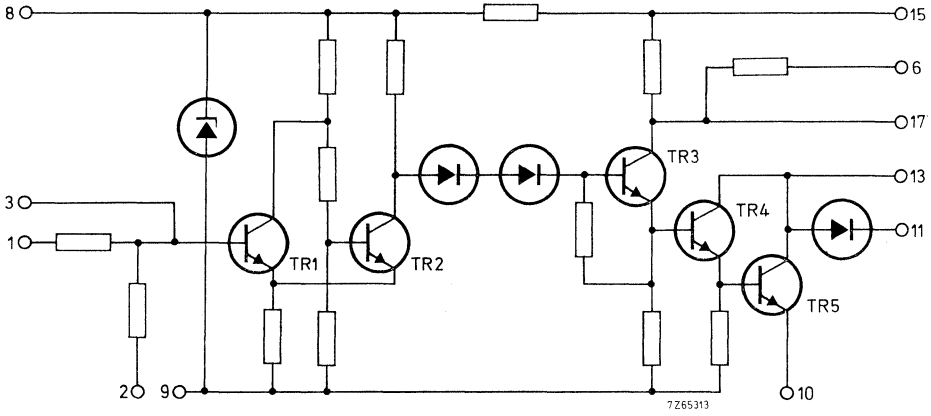


Fig. 1

The power amplifier consists of a Schmitt trigger followed by a buffer + driver stage, which provides adequate drive to the power transistor under all conditions of permissible supply voltage and input signal. The load should be connected between pin 13 and + of power supply. A "1" input will switch on the load current.

Notes:

1. Observe rules for $R_{load\ min}$.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from voltage and current so that turning on of a lamp may cause a current surge. It is often advisable to use a preheating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks at switching off. To avoid destruction of output transistor the load should be shunted by a damping diode. By connecting terminal 11 to the supply line inductive loads up to a certain value can be handled by the internal diode.

4. Pin 10 serves to make a separate connection between a 0 V load supply line and the power supply unit to avoid common wire impedance with the 0 V logic supply line. Also, if a second supply unit is used for the HPA 60, common impedance with the 0 V logic supply line should be avoided in the interconnection between pins 9 (0 V logic supply) and 10 (0 V output stage).

Terminal location

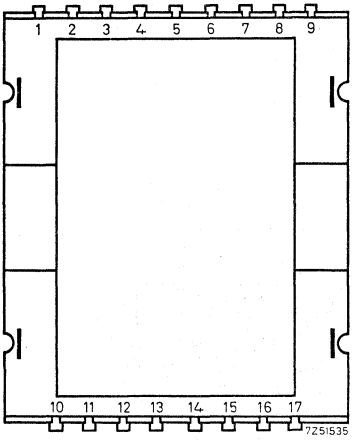
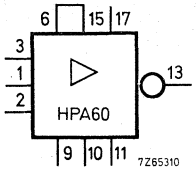


Fig. 2

1	= input
2	= base resistor of input transistor
3	= base of input transistor
4	= n.c.
5	= n.c.
6	= + supply, connect to 15
7	= n.c.
8	= zener diode
9	= 0 V logic supply
10	= 0 V output stage, see note 4
11	= damping diode
12	= n.c.
13	= output (load between 13 and supply)
14	= n.c.
15	= + supply, connect to 6
16	= n.c.
17	= collector of TR3

Fig. 3
Drawing symbol (one necessary interconnection indicated).



Additional instructions

a. If the input (pin 1) is driven by a standard "1" level from NOR 60, etc., connect pins 2 and 9.

b. If the supply voltage is 12 V ± 5%, connect a resistor of 330 Ω between pin 6 and 8, and a resistor of 1.5 kΩ between 15 and 17; both resistors ± 5%, $\frac{1}{4}$ W.

c. Wiring to pin 3 must be kept remote from the output circuitry.

d. When using pin 3 as a second input, the input resistor should be connected direct to the pin.

CHARACTERISTICS

	V_S = 24 V ± 25%	V_S = 12 V ± 5%
Supply current at V_S nom excluding I_{load}	18.8 mA	15.1 mA
Supply current at V_S max excluding I_{load}	< 26.2 mA	< 28.8 mA
Required load resistance at T_{amb} = 45 to 70 °C	> 13.5 Ω	> 6 Ω
at T_{amb} < 45 °C	> 12 Ω	> 5 Ω
Required input	1 D.U.	1 D.U.
Voltage on pin 13, TR5 conducting	max. 2.V	max. 2 V

	at pin 1	at pin 3
For switching on load current		
input voltage, 2–9 connected	> 6 V	> 1.6 V [1]
input current, 2–9 connected	75 µA	75 µA
2–9 not connected [2]	30 µA	30 µA
For switching off load current		
input voltage, 2–9 not connected [2]	< 1.15 V	< 1.15 V
On-off input voltage difference 2–9 not connected [2]	–	> 0.5 V

Switching speed	maximum	typical
Fall time, t_f	0.2 µs	0.05 µs
Rise time, t_r	4.2 µs	0.3 µs

The fall time t_f is defined as the time required for the output voltage to change from 90% to 10% of its full value, after application of a step input, under conditions as shown in Fig. 4 (See also Fig. 5).

The rise time t_r is defined as the time required for the output voltage to change from 10% to 90% of its full value, after application of a step input, under conditions as shown in Fig. 4 (See also Fig. 6).

1) Via min. 500 Ω.
2) Source resistance must not exceed 56 kΩ.

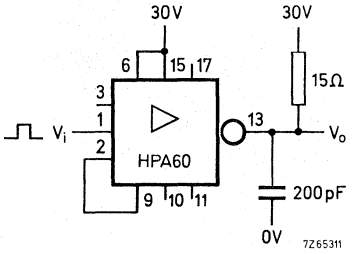


Fig. 4

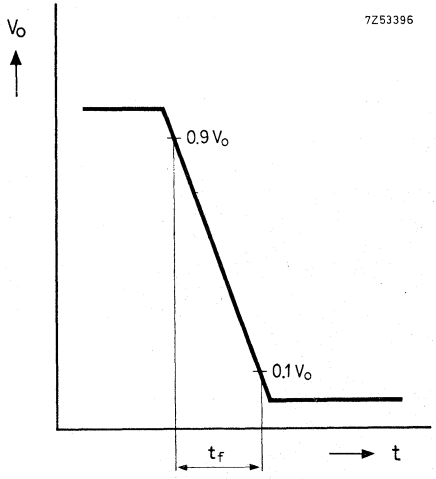


Fig. 5

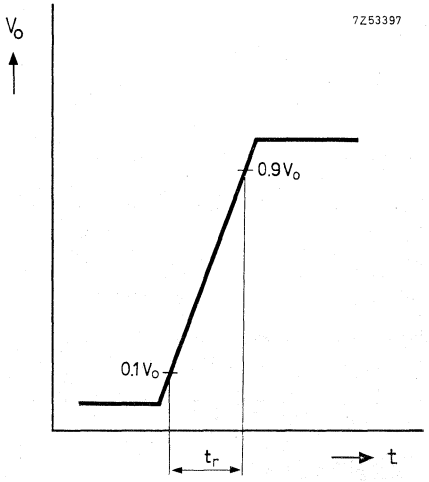


Fig. 6

By connecting terminal 11 to the supply line the following inductive loads can be handled by the internal damping diode:

R_L = 15 Ω	$L_L \leq$ 10 H
R_L = 20 Ω	$L_L \leq$ 14 H
R_L = 30 Ω	no restriction

Switch-off delay time for R_L = 30 Ω and L_L = 10 H is 770 ms.

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage, V_S	max. 30 V d.c.
Positive transient on driver stage (pin 6 and 15)	max. 10 V for 10 μs
Positive voltage on power stage, pin 13	max. 55 V
Voltage at pin 1 (2–9 connected)	
positive	max. 100 V
negative	max. 15 V
Voltage at pin 3	
positive	max. 5 V via min. 500 Ω
negative	max. 4.5 V
Output current	5 A for 20 ms

OVERLOAD PROTECTION

Protection measures must be taken in applications in which overloading of the HPA 60 may occur, e.g. short circuiting of the load. The operating time of a fuse is far too slow to provide adequate protection in such cases, therefore another method must be used. The protection circuit described here uses a 2.IA 60 connected as a memory element, and serves well in many HPA 60 applications.
It will operate at a load current of 3 A. Removing one of two series-connected diodes will bring the "fault" condition of load current down to 2 A. Finer control of the load current level at which the protection circuit will operate may be achieved by replacing the resistor R by a wire-wound potentiometer.

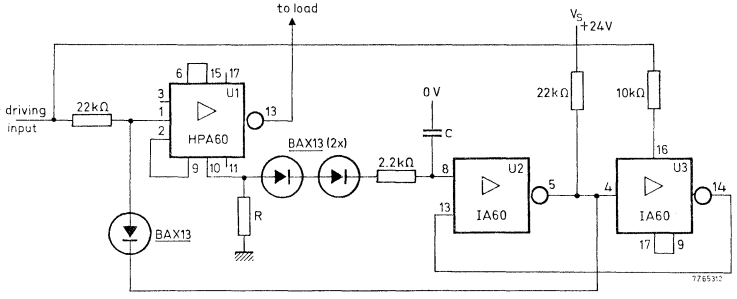


Fig.7

R = 0,39 Ω (2 W)
C = 100 nF

Load current information is provided by resistor R, and is fed to U2 (pin 8) via the series-connected diodes.
The capacitor C prevents the circuit from operating on transient currents of up to 5 A. If the load current is too high for the HPA 60, the output of U2, at pin 5, goes LOW. This LOW is fed back to U1, pin 1 , via the BAX13 diode. A LOW at the input of the HPA 60 switches it off.

When the overload is removed, the protection circuit remains in the fault condition because the memory element is still "set". The protection circuit can only be "reset" by removing the logic signal from the driving input, since U3 is fed with the HPA 60 driving input via pin 16.

The circuit shown here requires 6 D.U.

GROUNDED LOAD DRIVER

Function: - a 2 input power amplifier for switching d.c. loads, connected with one side to ground (GLD)
- a 2 input NOR gate
- monitor circuit for twin channel logic systems with fault display.

Case: Norbit block size A, colour black.

CIRCUIT DATA

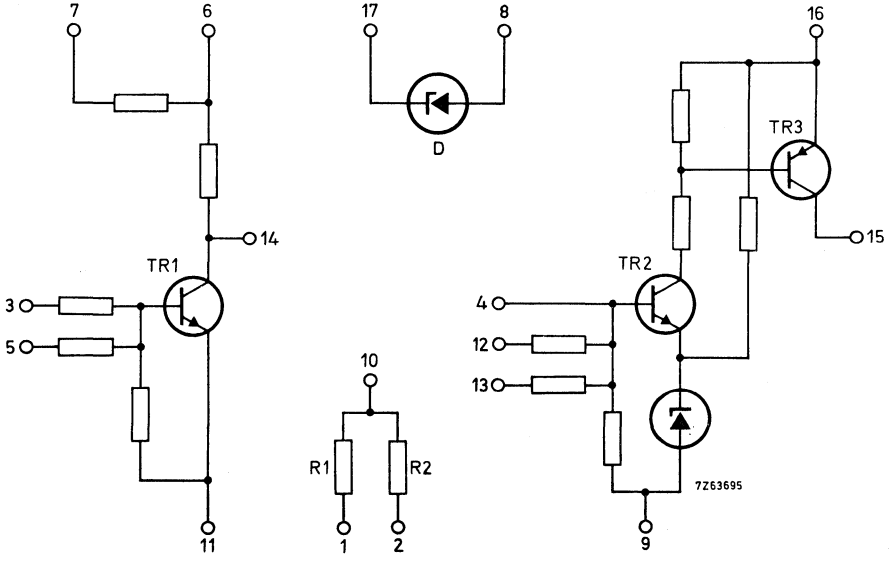


Fig. 1

The unit comprises two main circuits and auxiliary networks:
- A NOR gate with two inputs each requiring 1 D.U.. The output capability is 6 D.U..
- A grounded load driver (GLD) consisting of an input stage with two inputs and a PNP output stage. The load should be connected between the output terminal and 0 V common. A "1" input signal will switch on the load current.
- A voltage regulator diode (D) to couple the NOR to the GLD, or to isolate the load of the GLD from the resistance network (R1 and R2) when the complete unit is applied as a monitor circuit for twin channel logic systems with fault display.

Terminal location

1 = R1
2 = R2
3 = input NOR
4 = auxiliary input GLD
5 = input NOR
6 = positive supply V_S for NOR
7 = auxiliary supply
8 = voltage regulator diode, anode
9 = 0 V common GLD
10 = R1, R2
11 = emitter TR1, 0 V if used as NOR
12 = input GLD
13 = input GLD
14 = output NOR
15 = output GLD
16 = positive supply V_S for GLD
17 = voltage regulator diode, cathode

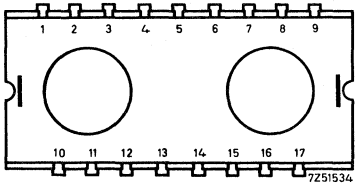


Fig. 2

Drawing symbols

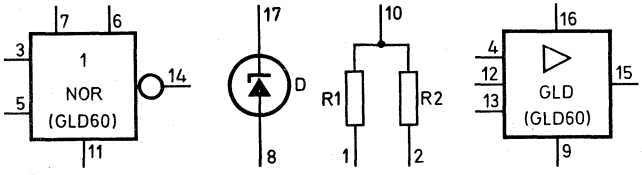


Fig. 3 NOR function auxiliary circuits GLD function

CHARACTERISTICS

7Z63686

	NOR (supply to pin 6)	GLD
Power supply voltage (V_S)	+24 V ±25%	+24 V ±25%
current	nom. 3,2 mA max. 4,1 mA	nom. 14,2 mA + I_{load} max. 19,1 mA + I_{load}
Input requirements, per terminal	1 D.U.	2 D.U.
Output capability	6 D.U.	900 D.U.
at maximum load resistance		3 kΩ
Minimum load resistance,		
- driven by signal on pins 12 and 13		75 Ω *) at T_{amb} = 45 °C 86 Ω *) at T_{amb} = 70 °C
- driven by NOR via D on pin 4 (supply to pins 7 and 16, connect pin 8 to 4, pin 14 to 17, pin 11 to 10, pin 12 or 13 to 0 V)		120 Ω *)

*) For use with incandescent lamps, series and/or bleed resistors might be required to avoid high inrush currents in connection with their "cold" resistance.
To limit large voltage peaks at switching of inductive loads these loads should be shunted by a damping diode, e.g. BAX12 (cathode to pin 15).

Resistor network

R1	3010 Ω
R2	1500 Ω

Voltage regulator diode

V_D	12 V

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage V_S	max. +30 V d.c. min. 0 V d.c.
Positive transient on V_S	max. +10 V for 10 µs
Input voltage	
NOR (pins 3, 5)	max. +70 V min. −15 V
GLD (pins 12, 13)	max. +70 V min. − 4 V
Input current GLD (pin 4)	max. +20 mA *)
Output surge current	max. 1 A for 20 ms

APPLICATION INFORMATION

A GLD60 as a grounded load amplifier

1. The GLD 60 makes it possible to drive loads (relays, magnetic valves etc.) of which one side has been connected to ground, Fig. 4 illustrates also the suitability of the unit for systems which from the point of safety require that the load is not activated in case of short circuit to ground of the output.

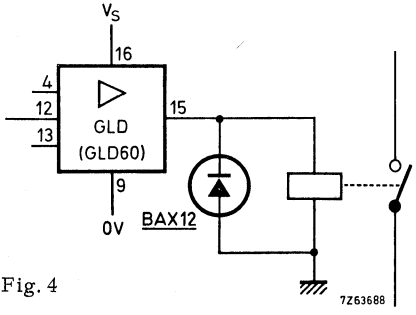


Fig. 4

2. High power grounded load drive. Fig. 5 shows how higher loads can be driven. This circuit permits load resistances down to 8,6 Ω (corresponding to a load current of 3,5 A at V_S = 30 V). The BDY60 is mounted on an aluminium heatsink of 150 cm^2, thickness 2 mm. For inductive loads a flywheel diode D (BYX30/50) is required.

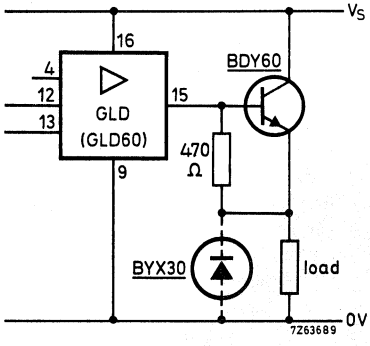


Fig. 5

*) Care should be taken not to apply a voltage > 1 V without current limiting resistance.

3. Short circuit protection of the GLD60.
If the load is short-circuited, the output transistor of the GLD60 can be damaged. This is prevented if the circuit depicted in Fig. 6 is applied. Too high a load current starts the BRY39 conducting. Consequently the input of the NOR goes "high" and its output "low", biasing input 4 of the GLD "low", in this way overruling the existing "high" on the system inputs. Once the BRY39 has started conducting, it will continue to do so until the push button is pressed.

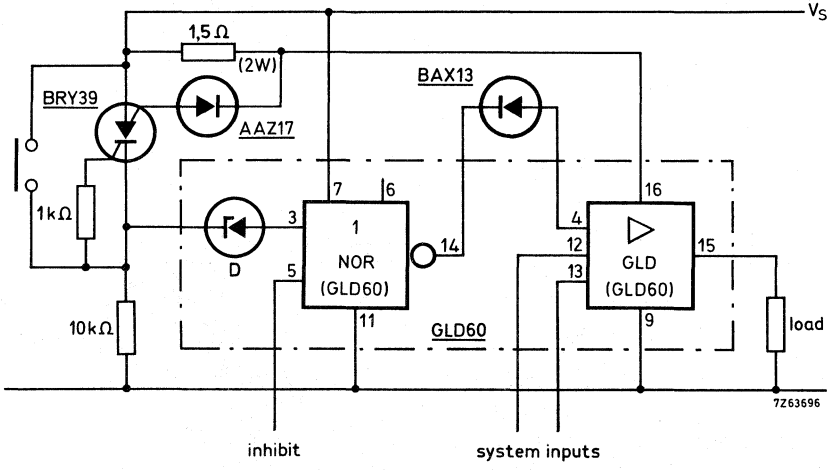


Fig. 6

B Monitoring and safeguarding twin channel systems

Fig. 7 shows the circuit build-up of a process control in which malfunctioning of one of the parallel identical logic systems or of the monitoring/safeguarding circuit causes an indication or switching to safe condition of the process to be controlled.
When the identical logic systems function properly their outputs are equal because their input conditions are identical. The equality of the outputs is monitored by the combination "2 x GLD60". Where parts of this monitoring combination are used in the channels before the point of comparison, they should be completely independent so that malfunction of one part in one channel cannot cause malfunction of the other part in the other channel. Consequently malfunction in this part of the monitoring combination will occur in one channel only and will have the same effect as malfunction of one of the logic systems. Similar considerations apply to the input connections of both logic systems.
Output V_{oA} can be used for power switching, and as an input condition for additional twin-channels (e.g. B_1 and B_2) in case the total control system comprises more twin channels.

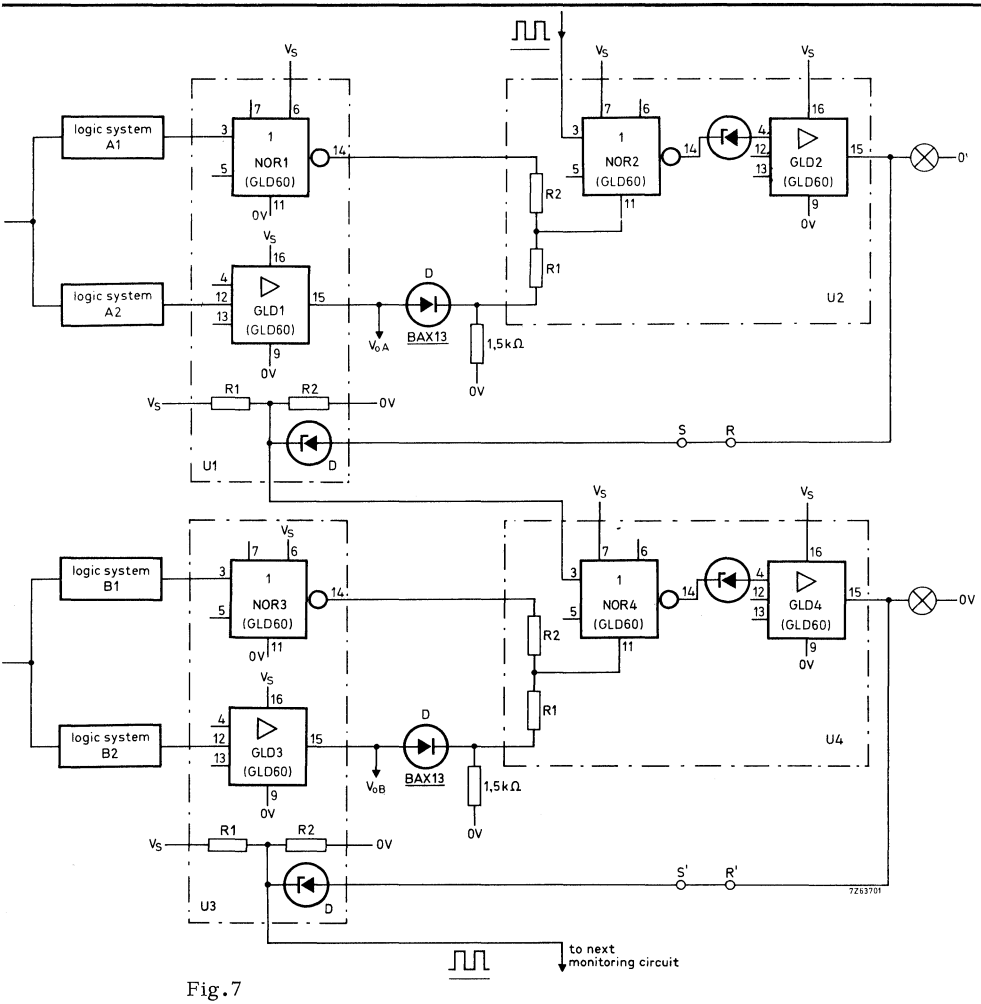


Fig.7

The actual circuit for comparing the outputs should be self-safeguarding which means that a malfunction should cause a fault indication, i.e. the part of the monitoring circuit between comparison circuit and pilot lamp has also to be monitored for malfunction. This is done by feeding a square wave to the input of this part, which is therefore monitored in a dynamic way. The output will alternate between on and off at the frequency of the square wave.

Malfunction of one of the components will cause a continuous on or off at the output. This also means that the pilot lamp is continuously monitored. Correct functioning of the whole system causes the pilot lamp to flicker (low square wave frequency e.g. 2 Hz) or to burn dimly (high square wave frequency e.g. 10 kHz).

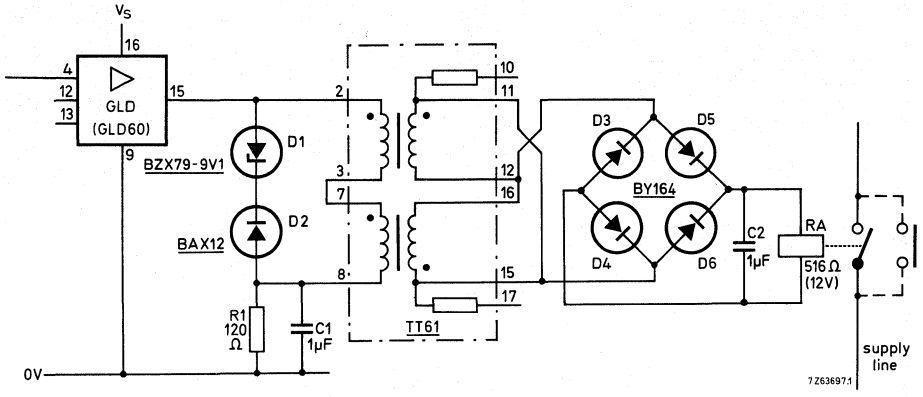


Fig. 8

The high frequency square wave output can also be fed via a transformer to a rectifier, see Fig. 8. Thus only a square wave output will cause a d.c. voltage which can be used to activate a relay. Any malfunction in the whole system will cause the relay to fall off and thereby switch the system to be controlled to a safe condition.

Note that if only one twin channel system has to be monitored or safeguarded the resistor of 1,5 kΩ and external diode BAX13 (Fig. 7) can be replaced by R2 and the voltage regulator diode inside unit U1.

The square wave interrogating signal fed to the monitor circuit should be symmetrical and vary between $V_S/3$ and V_S. Fig. 9 shows a suitable generator. The symmetry and the frequency are adjusted by means of the 10 kΩ potentiometer and the capacitor C respectively. Cycle time T = 1,5C ms approximately (C in µF).

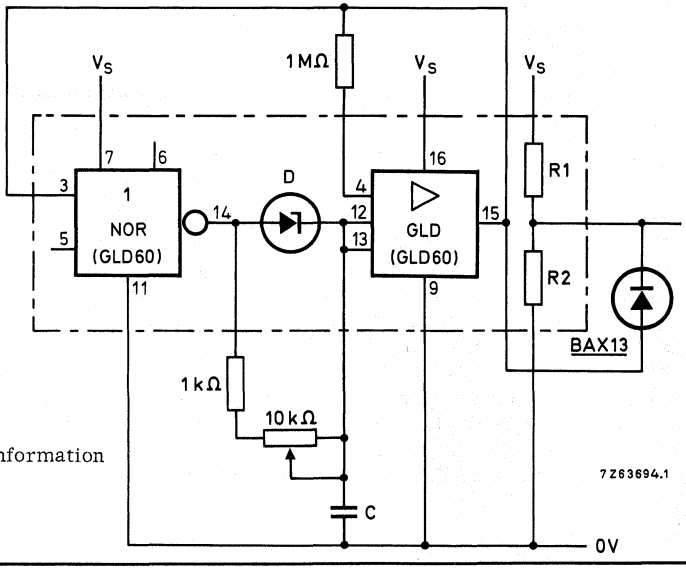


Fig. 9
Extended application information is given in A.I. 348.

UNIVERSAL POWER AMPLIFIER

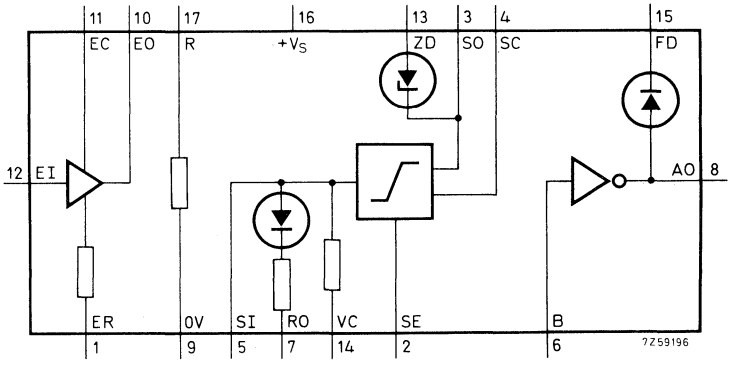
Function

1. D.C. switching amplifier.
2. Power oscillator for driving thyristor trigger transformers.
3. Phase shift module.
4. Current source for linear capacitor discharging.

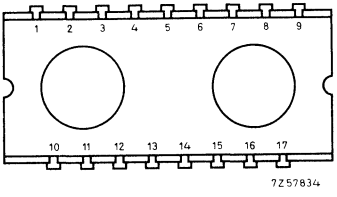
Case

Size: A; Colour: black.

CIRCUIT DATA



Quick reference circuit diagram

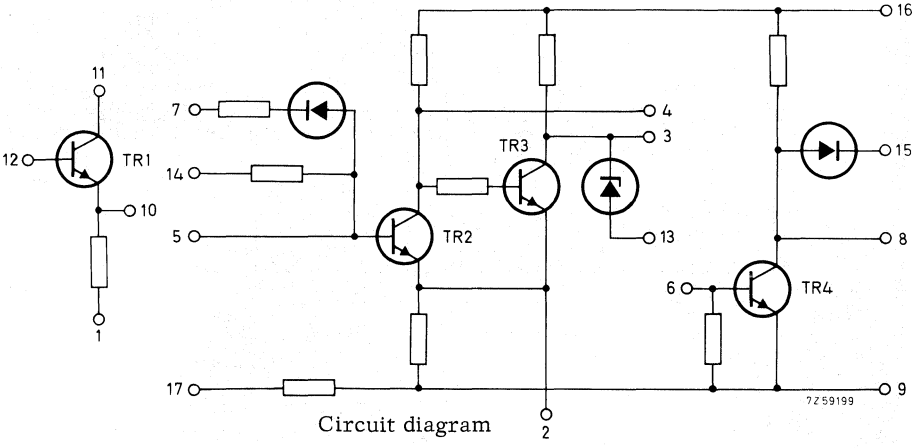


Terminal location

1 = emitter resistance follower
2 = emitter output Schmitt trigger
3 = output Schmitt trigger
4 = complementary output Schmitt trigger
5 = Schmitt trigger base input
6 = power stage base input
7 = oscillator feedback input
8 = power stage output
9 = 0 V common
10 = output emitter follower
11 = collector emitter follower
12 = base emitter follower
13 = restored "0" output Schmitt trigger
14 = input Schmitt trigger
15 = damping diode power stage
16 = supply voltage $+V_S$
17 = auxiliary resistor

Notes

1. For applications as a power amplifier with a min. permissible load resistance of 90 Ω, connect pin 13 to pin 6. A "1" at pin 14 will switch on the load between pins 8 and 16.
2. For applications as a power amplifier with a min. permissible load resistance of 30 Ω, connect pin 12, 13, 17 and 1 together, connect pin 10 to 6, and connect pin 11 to V_S via a resistor of 330 Ω, (2,5 W).
   A "1" at pin 14 will switch on the load between pin 8 and 16.
3. The load should be connected between pins 8 and 16. To avoid destruction resulting from large voltage peaks occurring at switching off of inductive loads, the damping diode in the circuit block has to be connected across the load (15 to 16).
4. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.



Circuit diagram

CHARACTERISTICS

Pins 6 and 13 connected, unless otherwise specified.

Supply	at V_S = +24 V ± 25%	at V_S = +12 V ± 5%
Supply current at I_{load} = 0 mA	≤ 110 mA	≤ 9 mA
Supply current at "1" input (pin 14) *) V_S = 30 V, R_{load} = 30 Ω	1100 mA	

*) Connections as in Note 2 above.

Input	at V_S = +24 V ± 25%	at V_S = +12 V ± 5%
Drive at pin 14 for switching on load current	2 D.U.	2 D.U.
Input impedance at pin 14	92 kΩ	92 kΩ
Input voltage for switching on load current at pin 5 **)	≥ 8.2 V	≥ 4 V
at pin 14	≥ 11.4 V	≥ 5.3 V
Input voltage for switching off load current at pin 5 **)	≤ 1.6 V	≤ 1 V
at pin 14	≤ 1.8 V	≤ 1.2 V
On-off input voltage difference, R_{source} = 2200 Ω, at pin 5	≤ 4.8 V	≤ 2.0 V
at pin 14	≤ 4.9 V	≤ 2.1 V
Max. source resistance for pin 5	250 kΩ	
for pin 14	200 kΩ	
Output		
Min. load resistance - connections Note 1	90 Ω	
- connections Note 2	30 Ω	
Output voltage at "1" input at min. load resistance - connections Note 1	≤ 0.3 V	
- connections Note 2	≤ 1.3 V	

Switching speed.

Switch off delay at 625 mA and 10 H with pin 15 connected to 16: t_d 480 ms

Fall time / Rise time, connected as in Note 2, R_L = 30 Ω, V_S = 30 V: t_f ≤ 0.5 µs, t_r ≤ 10 µs

LIMITING VALUES

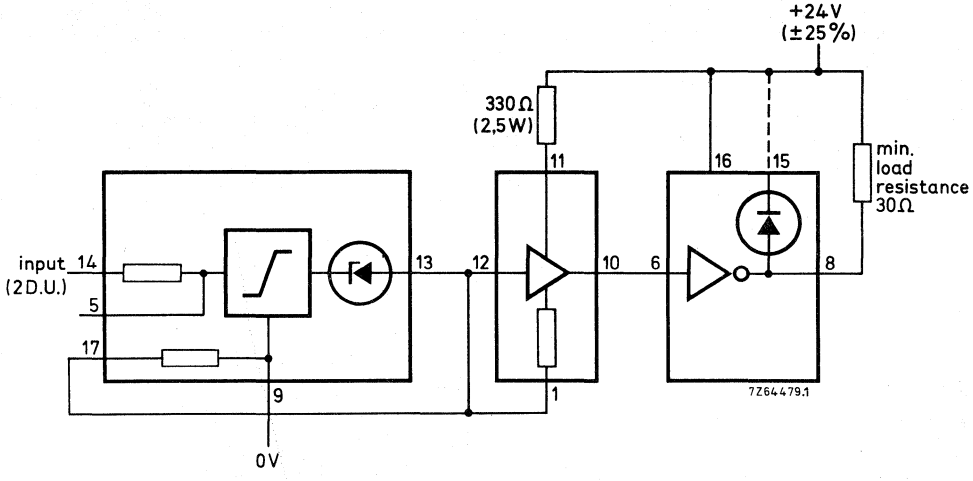
Supply voltage	V_S	max.	30 V
		min.	0 V
Positive transient on V_S, for 10 µs		max.	10 V
Input voltage at pin 14	$+V_{14}$	max.	70 V
	$-V_{14}$	min.	0 V
Input voltage at pin 5 via min. 2200 Ω	$+V_5$	max.	30 V
	$-V_5$	min.	0 V
Output current for 20 ms		max.	5 A
for 20 ms each second		max.	2 A

*) Connections as in Note 2

**) Via min. 2200 Ω

APPLICATION INFORMATION

UPA61 as 30 ohms load power amplifier.



DUAL TRIGGER TRANSFORMER

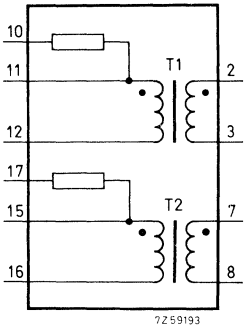
Function

Matching the pulse output from a power amplifier (e.g. UPA61) to thyristor gates.

Case

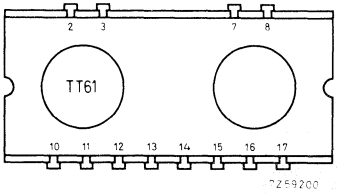
Size A; colour: black

CIRCUIT DATA



Circuit diagram

2. Secondary winding T_1 (cathode thyristor)
3. Secondary winding T_1 (gate thyristor)
7. Secondary winding T_2 (cathode thyristor)
8. Secondary winding T_2 (gate thyristor)
10. Resistance connected to primary winding T_1
11. Primary winding T_1 (driving source)
12. Primary winding T_1 ($+V_S$)
13. Not connected
14. Not connected
15. Primary winding T_2 (driving source)
16. Primary winding T_2 ($+V_S$)
17. Resistance connected to primary winding T_2



Terminal location

CHARACTERISTICS

Frequency range	3 to 50 kHz [1]
Turns ratio primary: secondary	3 : 1
Inductance of primary winding	≥2, 2 mH
Leakage inductance referred to primary (secondary short-circuited)	≤ 65 µH
Primary winding resistance at T_{amb} = 25 °C	≤ 4 Ω
Primary series resistor	82 Ω
Secondary winding resistance at T_{amb} = 25 °C	≤ 0, 6 Ω
Output pulse in response to step input, circuit of Fig. 3, R_{eq} = 15 Ω: rise time (from 0, 3 to 3 V) pulse duration, V_{pulse} = 3 V [1]	 ≤ 0, 6 µs ≥ 20 µs
Output current[2] at pins 2/3 (7/8) at T_{amb} = 25 °C in response to step input at pins 10/12 (16/17) (see Fig. 3): V_S = 18 V, R_{eq} = 15 Ω R_{eq} = 22 Ω V_S = 30 V, R_{eq} = 10 Ω R_{eq} = 15 Ω	 ≥200 mA ≥135 mA ≥425 mA ≥320 mA

LIMITING VALUES

Primary switched voltage across pins 10/12 (17/16)	max. 30 V [3]
Primary switched current no series resistor, duty cycle 1 : 3 max. 82 Ω internal, duty cycle 1 : 3 max. 39 Ω external, duty cycle 1 : 2 max.	 max. 800 mA max. 170 mA max. 200 mA
ET product per transformer primary at pins 11, 12 or 15, 16	600 Vµs
Peak pulse power per transformer for duty cycle 1:3, and T_{amb} = 25 °C [1]	17 W
D.C. test voltage between any pair of windings for 1 minute	4 kV
Continuous r.m.s. working voltage	max. 500 V

1) The minimum frequency has been specified with a view to core losses.
2) Minimum mean pulse magnitude over 20 µs.
3) If the UPA61 ceases to oscillate with the output transistor conducting, the primary series resistor may be damaged; circuit design must safeguard against this condition.

APPLICATION INFORMATION

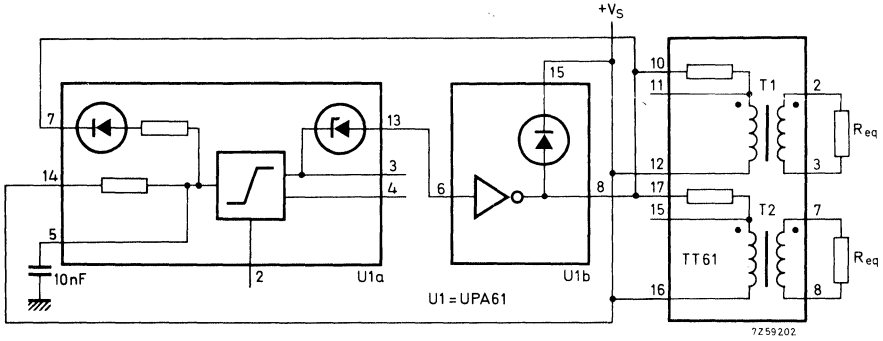


Fig. 3 Low power relaxation oscillator circuit (10 kHz)

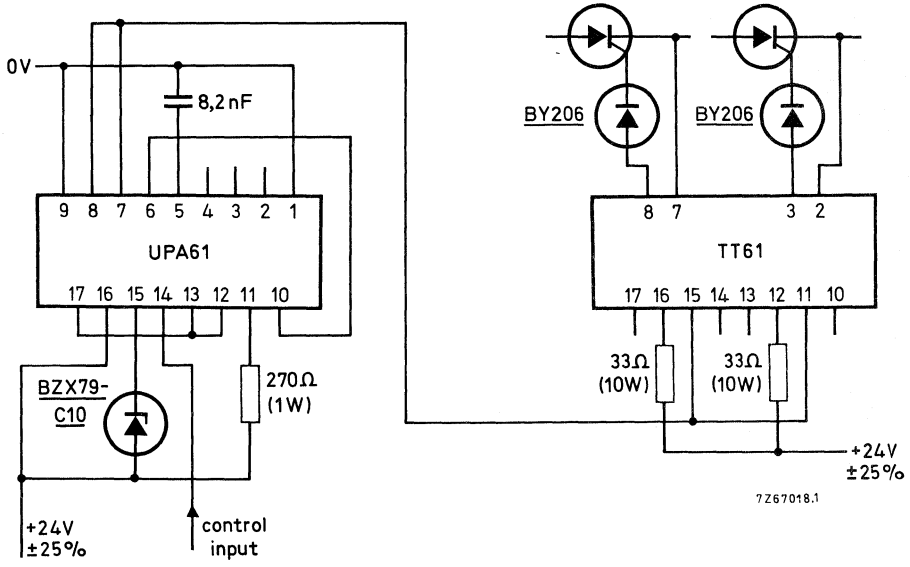


Fig. 4a High power relaxation oscillator circuit (10 kHz)

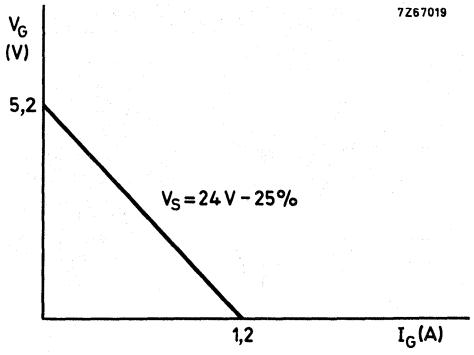


Fig. 4b Gate cathode thyristor voltage versus gate thyristor current

RECTIFIER AND SYNCHRONIZATION ASSEMBLY

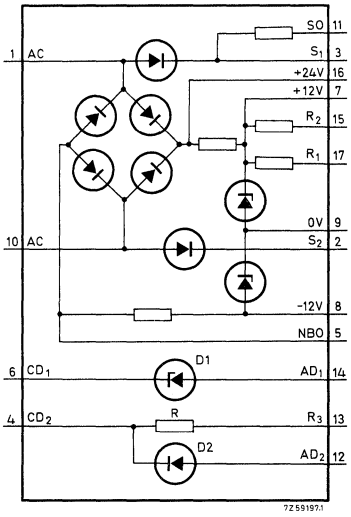
Function

- To provide an unregulated voltage of +24 V for Norbit systems
- To provide synchronization signals.
- To provide +12 V and −12 V (zener stabilized) for servo amplifiers.

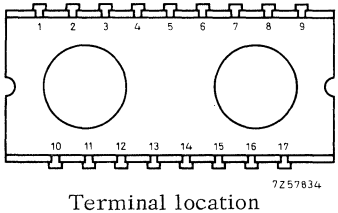
Case

Size: A; colour: black

CIRCUIT DATA



Circuit diagram



Terminal location

1 = A.C. input from supply transformer
2 = Synchronization voltage
3 = Synchronization voltage
4 = Cathode D_2
5 = Output rectifier bridge
6 = Cathode D_1
7 = +12 V output voltage
8 = −12 V output voltage
9 = 0 V from common supply
10 = A.C. input from supply transformer
11 = Synchronizing resistor output
12 = Anode D_2
13 = Resistor output cathode D_2
14 = Anode D_1
15 = +12 V, 150 kΩ source
16 = +24 V output voltage
17 = +12 V, 100 kΩ source

CHARACTERISTICS

Input

A.C. input voltage (r.m.s.)	2 x 20 V (+10, −15%)
A.C. input current	375 mA max.
Frequency	50 - 60 Hz
Source resistance	1 Ω min.
	4 Ω max.

Outputs

Pin number (9 connected to c.t. transformer)	Voltage	Current
16	+18 to +30 V	≤ 220 mA
7	+11 to +15 V	≤ 8 mA
8	−11 to −15 V	≤ 4 mA

In order to obtain the outputs specified, smoothing capacitors are required:

1. a 680 μF (−10, +50%), 40 V, capacitor connected between pins 16 and 9 to smooth the +24 V and +12 V.
2. a 100 μF (−10, +50%), 40 V, capacitor connected between pins 5 and 9 to smooth the −12 V.

Additional components

R : 2.2 kΩ; max. voltage 30 V r.m.s.

D_2 : max. reverse voltage 30 V;
max. forward current 200 mA

D_1 : nom. zener voltage 6.8 V;
max. dissipation 60 mW

LIMITING VALUES

Input voltage	2 x 22 V r.m.s.

APPLICATION INFORMATION

1. The output current of the −12 V output can be increased to 7 mA by connecting pin 4 to 5 and pin 8 to 13.
2. A mains synchronization signal is available at pin 11 when pins 3 and 2 are joined. The output at pins 2 and 3 takes the form of a zero voltage when the a.c. driving voltage passes through zero. At all other times a positive voltage is present on pins 2 and 3.

DUAL NOR-GATE WITH DIODE-RESISTOR NETWORKS

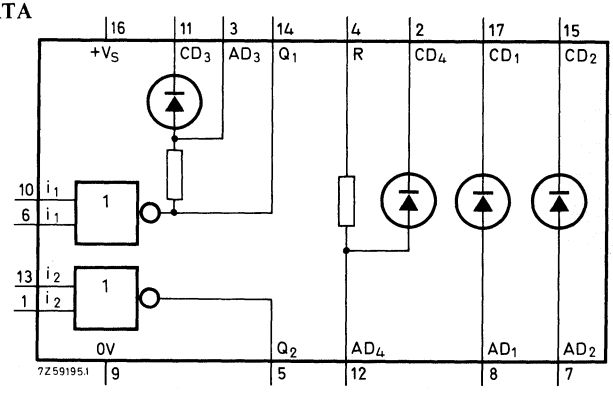
Function

Dual two-input transistor-resistor NOR-gate with diode gating facilities incorporated; specifically applicable as a d.c. counting/shifting stage.

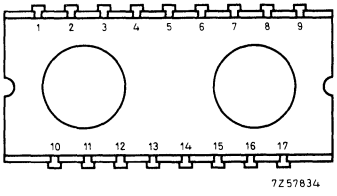
Case

Size: A; colour: black.

CIRCUIT DATA

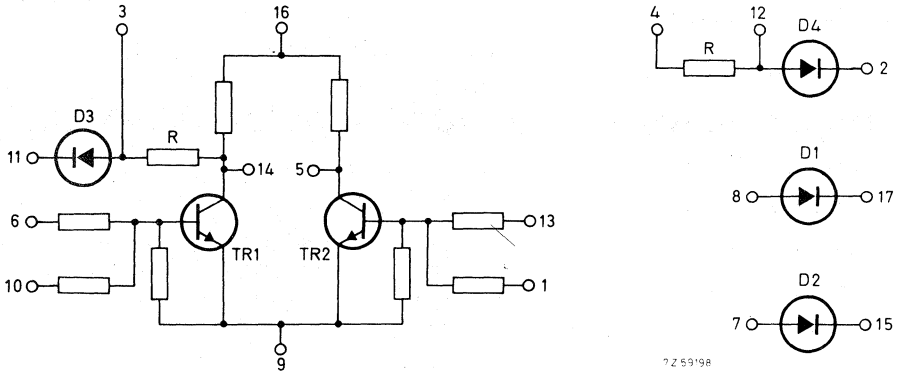


Quick reference circuit diagram



Terminal location

1 = Input NOR 2
2 = Cathode diode D_4
3 = Anode diode D_3
4 = Gate resistor
5 = Output NOR 2
6 = Input NOR 1
7 = Anode diode D_2
8 = Anode diode D_1
9 = 0 V common supply
10 = Input NOR 1
11 = Cathode diode D_3
12 = Anode diode D_4
13 = Input NOR 2
14 = Output NOR 1
15 = Cathode diode D_2
16 = $+V_S$ supply for NOR 1 and NOR 2
17 = Cathode diode D_1



Circuit diagram

CHARACTERISTICS

NOR-gate	at V_S = 24 V ±25%	at V_S = 12 V ±5%
Supply current at V_S nom	5.6 mA	2.8 mA
at V_S max	7.2 mA	3.1 mA
Input requirement	2 D.U.	2 D.U.
Output capability	10 D.U.	6 D.U.

	pins 6, 13	pins 10, 1	pins 6, 10 and 13, 1 in parallel
Input impedance [1]	63 kΩ	47 kΩ	32 kΩ
Input current for "0" output [1] [2]	92 μA	86 μA	75 μA

Switching speed

Fall time $t_f \leq 1.5\ \mu s$

Fall delay time $t_{fd} \leq 6\ \mu s$

Diode-resistor networks

Resistors R (22 kΩ) can be used as a load of 4 D.U. in a logic Norbit system.

[1]) Not used inputs returned to 0-volt line .
[2]) At V_S = 30 V

LIMITING VALUES

Supply voltage	V_S	max.	+30	V
		min.	0	V
Positive transient on V_S		max.	10	V for 10 μs
Positive input voltage	$+V_i$	max.	70	V
Negative input voltage	$-V_i$	max.	15	V
Reverse voltage of diodes		max.	50	V
Forward current of diodes		max.	75	mA
Repetitive peak forward current of diodes		max.	150	mA
Dissipation of resistor R		max.	50	mW

FLIP-FLOP

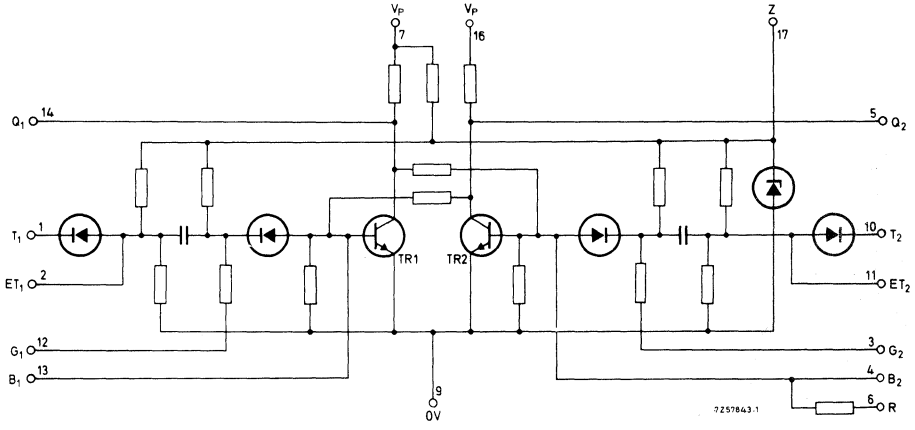
QUICK REFERENCE DATA	
Function	set-reset bistable multivibrator with trigger gates
Encapsulation	size: A block; colour: red
Max. counting speed (worst case)	5 kHz
Output capability	5 D.U., 7 Z.U.
Trigger input requirement	"1"-"0" edge of max. 3 μs; 2 Z.U.

APPLICATION

The FF90 has been intended to be used in counters, shift registers, etc.

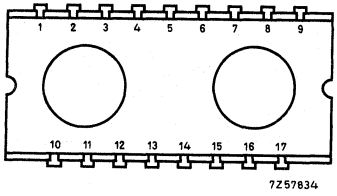
DESCRIPTION

Circuit

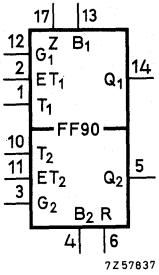


The unit comprises a set-reset bistable multivibrator which incorporates trigger gates. Switching is performed by applying a "1"-"0" edge of max. 3 μs at the trigger terminals (T_1 and T_2) which are controlled by gates (G_1 and G_2). The trigger inputs may be extended by the addition of external diodes to the extension terminals (ET_1 and ET_2) to provide an OR or inhibit facility. In addition, the circuit may be reset by applying a "1" level to the reset terminal (R) and may be set by applying a "1" level to the base of transistor 1 (B_1) via a resistor.

Terminal location



Drawing symbol



1 = T_1 = Trigger input 1
2 = ET_1 = Extension trigger input 1
3 = G_2 = Gate input 2
4 = B_2 = Transistor TR_2 base
5 = Q_2 = Output 2
6 = R = Reset
7 = V_p = For positive supply (connect to pin 16)
8 = Not connected
9 = 0 V = 0 V common
10 = T_2 = Trigger input 2
11 = ET_2 = Extension trigger input 2
12 = G_1 = Gate input 1
13 = B_1 = Transistor TR_1 base
14 = Q_1 = Output 1
15 = Not connected
16 = V_p = For positive supply (connect to pin 7)
17 = Z = Zener diode*

* Caution: With the supplies connected ensure that pin 16 is not accidentally connected to pin 17, otherwise the zener diode will be damaged.

ELECTRICAL DATA

Power supply

Voltage	+24 V ± 25%
Current	< 21 mA

Input requirements (see also "Switching times")

function	input terminal	input requirement		notes and instructions
		'1' level (D.U.)	'0' level (Z.U.)	
reset (put Q1 to '1')	R	1	0	The Set and Reset inputs may be expanded by using up to 3 suitable diodes at each input. Ensure that the cathode of each diode is connected to the input. If the Set or Reset facilities are used, inputs must be held at '0' (and not left open-circuited) except during the command period.
set (put Q2 to '1')	B1 via 82 kΩ resistor 2)	1	0	
gate	G_1, G_2	2	1	'1' or open-circuit closes gate. '0' opens gate.
gate	G_1, G_2 via a diode 1) 2)	0	1	'1' or open-circuit closes gate. '0' opens gate. Ensure that the anode of the diode is connected to the input.
trigger	T_1, T_2	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop. If T_1 and T_2 are interconnected, 4 Z.U. are required.
trigger	ET_1, ET_2 via a diode 1) 2)	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop. If ET_1 and ET_2 are interconnected, 4 Z.U. are required. Ensure that the anode of each diode is connected to the input.

1) Diodes type BAX 13, BAX 16 or BAX 78 can be used.

2) If external components are used, ensure that they are mounted as close as possible to the appropriate input.

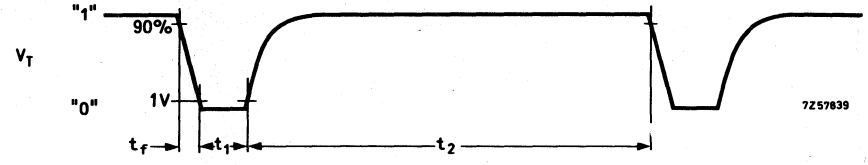
Output data

Output capability	5 D.U. and 7 Z.U.
Max. capacitive load	200 pF

Account must be taken of the load imposed by the gates when they are connected to the output terminals (Q_1, Q_2).

Switching times

Trigger



Max. fall time	t_{fmax}		3 μs
Min. pulse duration	t_{1min}		5 μs
Trigger recovery time	t_2	max.	99 μs
		typ.	73 μs

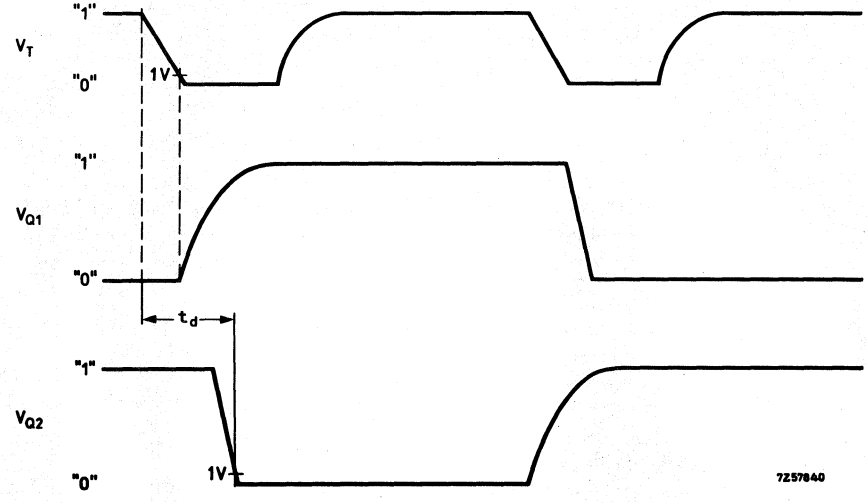
Gate

Gate recovery time	max.	137 μs
	typ.	100 μs

The signal at the gate must be present at least 137 μs (worst case) before the triggering edge is applied to T_1 or T_2. It is permitted to change the gate signal simultaneously with the triggering edge.

Switching delay

Delay between triggering edge and negative-going output.	t_d	max.	8 μs
		typ.	3 μs



Reset of Set: The appropriate terminal should be at a logical '1' for a minimum of 50 μs to reset or set the flip-flop.

Maximum Counting Speed (1 : 1 mark: space ratio) 5 kHz (worst case)

The worst case figure is related to the most disadvantageous connection or input condition that can be made.

APPLICATION INFORMATION

For connection as a divider of two connect pin 3 to pin 5 and pin 12 to pin 14.

More information is given in "Application Information 849, Counting and Shifting with 90-Series Modules."

TWIN-TRIGGER GATE

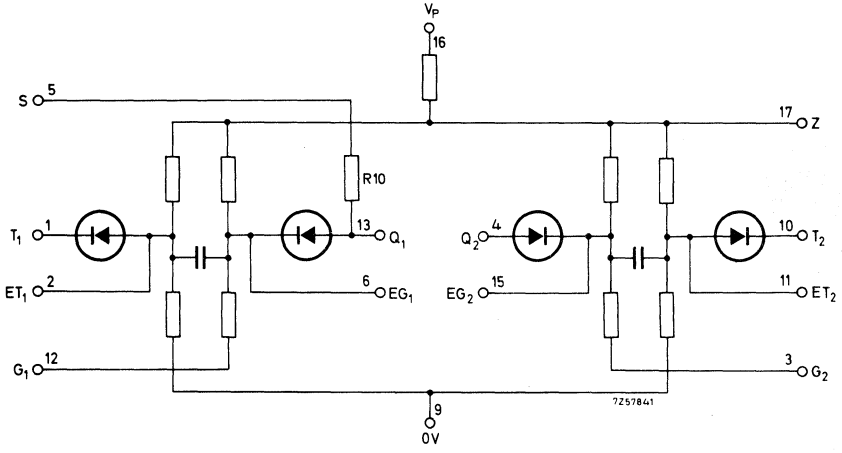
QUICK REFERENCE DATA	
Function	two trigger gates for use with FF90 only
Encapsulation	size: A block; colour: red
Output signal	suitable for triggering direct on transistor base of FF90 (B_1 and B_2)
Trigger input requirement	'1'-'0' edge of max. 3 μs; 2 Z.U.

APPLICATION

The 2.TG90 has been intended to provide two extra independent trigger gates for the FF90.

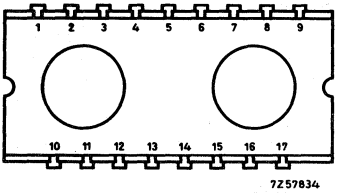
DESCRIPTION

Circuit

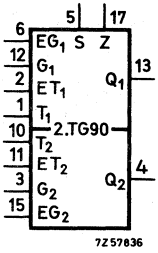


The unit comprises two gating circuits to perform extra independent trigger functions. The mode of operation is the same as for the trigger functions of the FF90. Switching is performed by applying a '1'-'0' edge of max. 3 μs at the trigger terminals (T1 and T2) which are controlled by gates (G_1 and G_2). The trigger inputs may be expanded by the addition of external diodes to the extension terminals (ET_1 and ET_2) to provide an OR or inhibit facility. The extra resistor (R_{10}), connected to terminal Q_1, provides the 'set' facility for the FF90.

Terminal location



Drawing symbol



1 = T_1 = Trigger input
2 = ET_1 = Extension trigger input 1
3 = G_2 = Gate input 2
4 = Q_2 = Output to B_2 (pin 4) of FF90
5 = S = Set terminal
6 = EG_1 = Extension gate input
8 = Not connected
9 = Not connected
9 = 0 V = 0 V common

10 = T_2 = Trigger input 2
11 = ET_2 = Extension trigger input 2
12 = G_1 = Gate input 1
13 = Q_1 = Output to B_1 (pin 13) of FF90
14 = Not connected
15 = EG_2 = Extension gate input
16 = V_P = For positive supply
17 = Z = Voltage reference terminal, connect to Z (pin 17) on FF90

ELECTRICAL DATA

Power supply

Voltage	+24 V ± 25%
Current	7.5 mA

Input requirements

function	input terminal	input requirement		notes and instructions
		'1' level (D.U.)	'0' level (Z.U.)	
set (put Q_2 of associated FF90 to '1')	S	1	0	The Set input may be expanded by using up to 3 suitable diodes on each input. Ensure that the cathode of each diode is connected to the input. If the Set facility is used, the input must be held at '0' (and not left open-circuited), except during the input period.
gate	G_1, G_2	2	1	'1' or open-circuit closes gate. '0' opens gate
gate	G_1, G_2 via diode 1) 2)	0	1	'1' or open-circuit closes gate. '0' opens gate. Ensure that the anode of the diode is connected to the input.
trigger	T_1, T_2	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop 3). If T_1 and T_2 are interconnected, 4 Z.U. are required.
trigger	ET_1, ET_2 via diode 1) 2)	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop 3). If ET_1 and ET_2 are interconnected, 4 Z.U. are required. A maximum of two diodes may be connected to each ET terminal. Ensure that the anode of each diode is connected to the input.

For notes see page 4.

Output data

The outputs Q_1, Q_2 are suitable only for use with one FF90; Q_1, Q_2 and Z of the 2.TG90 should be connected to B_1, B_2 and Z respectively of the FF90.
The inter-wiring capacitance should be limited at 50 pF (maximum). This capacitance will not be exceeded when a 2.TG90 is mounted next to an FF90.

1) Diodes type BAX 13, BAX 16 or BAX 78 can be used. Max. 2 diodes may be added.
2) If external components are used, ensure that they are mounted as close as possible to the appropriate input.
3) Switching times of the triggering signal are the same as for the FF90.

PULSE SHAPER

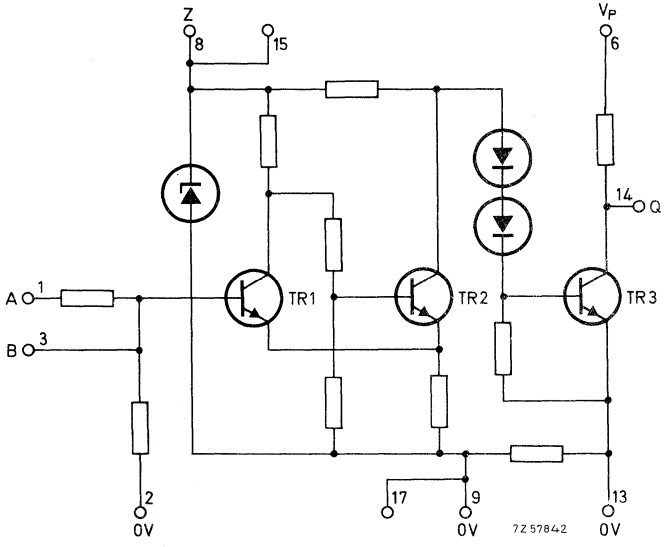
QUICK REFERENCE DATA	
Function	a. Driving the trigger inputs of one or more FF90 or 2.TG90 units b. Shaping signals to produce NORBIT 60 drive levels
Encapsulation	size: A block; colour: green
Output capability	6 D.U.; 40 Z.U.

APPLICATION

The PS90 has been intended to produce the triggering edge required for the FF90. The output levels are conforming to '1' and '0' of 60-Series logic.

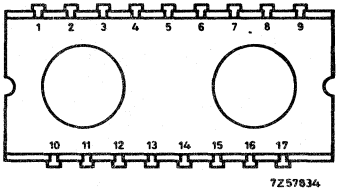
DESCRIPTION

Circuit

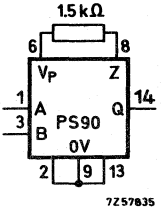


The unit contains a Schmitt trigger circuit followed by an inverting amplifier.

Terminal location



Drawing symbol



1 = A = Input via resistor
2 = 0 V = 0 V common (connect to pins 9 and 13)
3 = B = Input direct to base
4 = Not connected
5 = Not connected
6 = Vp = For positive supply (connect also to pin 8 via 1.5 kΩ resistor*)
7 = Not connected
8 = Z = Zener diode ** internally connected to pin 15 (connect to pin 6 via 1.5 kΩ resistor *)
9 = 0 V = 0 V common, internal connection to pin 17 (connect also to pins 2 and 13)
10 = Not connected
11 = Not connected
12 = Not connected
13 = 0 V = 0 V common (connect also to pins 2 and 9)
14 = Q = Output
15 = Z = Internally connected to pin 8
16 = Not connected
17 = 0 V = Internally connected to pin 9.

* The 1.5 kΩ ± 10% resistor connected between pins 6 and 8 (15) has a dissipation of 0.35 W maximum.

** When the PS90 is mounted on PWB60 or PWB61, pins 7 and 16 are connected to the positive supply Vp. Ensure therefore, that neither pins 7 and 8 nor pins 15 and 16 are interconnected. Otherwise, the Zener diode will be damaged.

ELECTRICAL DATA

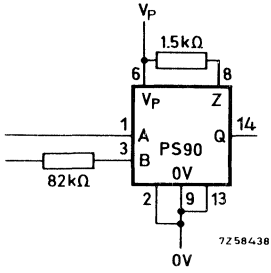
Power supply

Voltage	+24 V ± 25%
Current	< 21 mA

Input Data

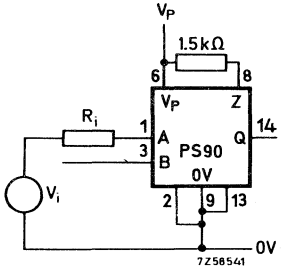
1. Unit driven by circuit block of 60 Series or 90 Series

The input requirement at pin 1 (pin 3 not connected) for '0' output is 1 D.U. One input may be added, namely an 82 kΩ resistor connected to pin 3 (input requirement is 1 D.U.). The circuit then performs as a 2-input NOR function. The 82 kΩ resistor should be mounted as close as possible to the unit.



2. Unit driven by any other circuit at pin 1 with pin 3 not connected.

	Operating	Limiting value
Input voltage to give '0' output	min. +6 V	+30 V
Input voltage to give '1' output	max. +1.5 V	−15 V



Hysteresis

ΔV_i min. = 0.55 + 0.003 Ri V (Ri in kΩ)
ΔV_i max. = 1.5 + 0.012 Ri V (Ri in kΩ)

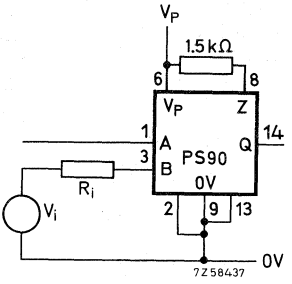
See also "Switching speed".

3. Unit driven by any other circuit at pin 3 with pin 1 not connected

	Operating	Limiting values
Input current to give '0' output	min. 50 μA	5 mA
Input current to give '1' output	max. 15 μA	0 mA

If driven by a voltage source, the source resistance should be minimum 500 Ω.

Max. positive voltage with R_i = 500 Ω +5 V
Max. positive voltage with R_i = 6,8 kΩ +30 V
With pin 2 not connected the max. source resistance is 50 kΩ and the max. negative voltage is 4 V.



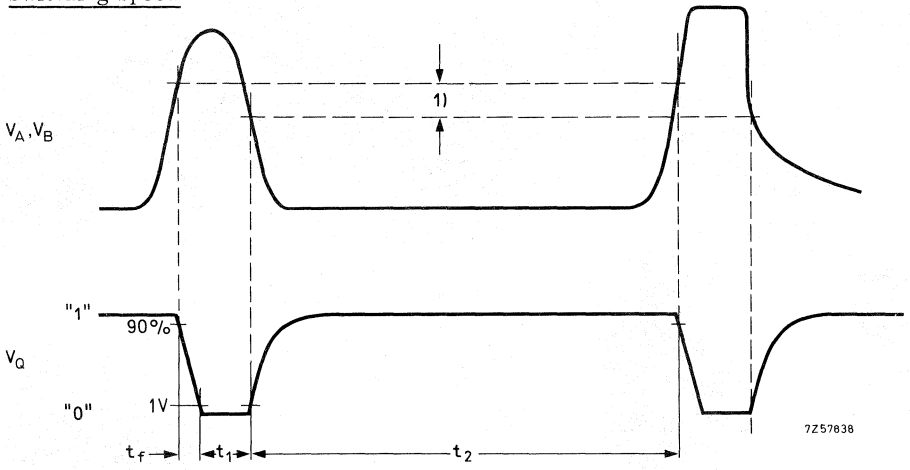
Hysteresis
ΔV_i min. = 0,32 + 0,003 R_i V (R_i in kΩ)
ΔV_i max. = 0,45 + 0,012 R_i V (R_i in kΩ)

See also "Switching speed".

Output Data

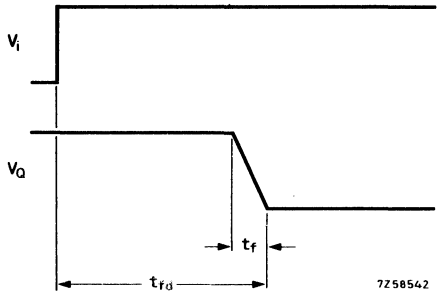
Output capability	6 D.U.
	40 Z.U.
Max. capacitive load	200 pF

Switching Speed



$t_f \leq 3\ \mu s$
t_1 and t_2 depend on input waveforms.
1) Hysteris ΔV_A or ΔV_B

If a step function is applied to the input and the output is loaded with 200 pF the output signal is given by:



Fall time	$t_f < 0.25\ \mu s$
Fall delay time	$t_{fd} < 2.5\ \mu s$

OBSOLESCENT

All types mentioned in this chapter are obsolescent. They are available until present stocks are exhausted.

Accessories for NORbits

SURVEY

MODULES

TT60 2722 032 00051	Dual thyristor trigger transformer for producing, in conjunction with a UPA60, two pulse currents of up to 400 mA.	
	Turns ratio pr. : sec. : sec.	3 : 1 : 1
	Dimensions (incl. pins)	34 x 34 x 49 mm
SIM60 4322 026 38301	Logic simulator for 60-Series NORbits.	
	Supply voltage	117/220/240 V; 50 or 60 Hz
	Housing	attaché case, 415 x 310 x 95 mm

POWER SUPPLY UNITS

LSU60 4322 000 01000 4322 000 01010	Power supply unit for small logic systems with 60-Series NORbits, to be built in chassis UMC60.	
	Input 01000 version	220 V, 45-400 Hz
	Input 01010 version	110 V, 45-400 Hz
	Output (d.c.)	150 mA, >18 V; 0 mA, <30 V
	Board dimensions	90 x 83 mm
PSU60 2722 151 00041 PSU61 2722 151 00051	Power supply units for 60-Series NORbits.	
	Input	240 V, 47-440 Hz
	Output (d.c.)	500 mA, >18 V; 0 mA, <30 V
	Extra d.c. output PSU61	100 V, 25 mA
	Dimensions	146 x 76 x 77 mm

MAINS FILTERS

MF 0,5 A 9390 213 00002	Mains filter for control systems consuming less than 0,5 A a.c.	
	Attenuation 0,1 - 10 MHz	50 dB
	A.C. limits	250 V, 0,5 A
	Dimensions	88 x 38 x 39 mm
MF 2,4 A 9390 253 30142	Mains filter for control systems consuming less than 2,4 A a.c.	
	Attenuation 0,5 - 10 MHz	40 dB
	A.C. limits	250 V, 2,4 A
	Dimensions	105 x 62 x 44 mm

CHASSIS AND HOLDERS

BB60 9390 198 00002	Breadboard block to hold 1 size A unit and to interlock with other BB60 blocks for easy assembly of circuits for teaching purposes.	
	Dimensions	56 x 38 x 14 mm
UMC60 4322 026 38330	Universal mounting chassis for 6 size A or 3 size B blocks or combination.	
	Material	plastic
	Dimensions	245 x 95 x 28 mm

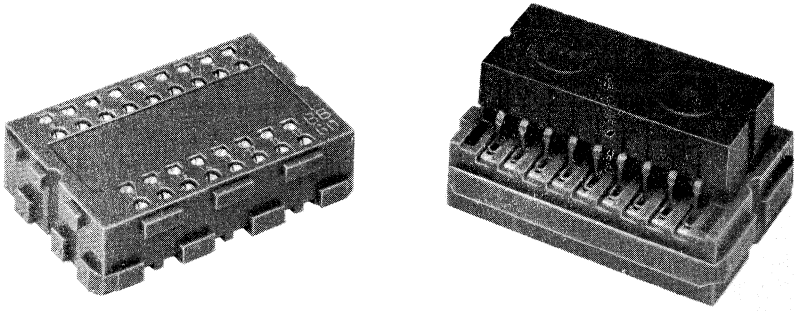
PRINTED–WIRING BOARDS

GPB60 4322 026 38600 GPB60/P 4322 026 38610	Experimenters' printed-wiring boards	
	Material GPB60	glass-epoxy
	Material GPB60/P	phenol paper
	Accommodation	10 size A or 4 size B blocks
	Mating connector	F045 (0.2")
PWB60 4322 026 38790 PWB60/P 4322 026 38800	Experimenters' printed-wiring board provided with 0 V tracks	
	Material PWB60	glass-epoxy
	Material PWB60/P	phenol paper
	Accommodation	10 size A blocks
	Mating connector	F047, F050, F053 (0.156")
PWB61 4322 026 38810	Experimenters' printed-wiring board provided with 0 V tracks	
	Material PWB61	glass-epoxy
	Material PWB61/P	phenol paper
	Accommodation	10 size A blocks
	Mating connector	F045 (0.2")
PWB62 4322 026 38780	Printed-wiring board with complete F054 connector, with 0 V and + tracks	
	Material	glass-epoxy
	Accommodation	4 size A or 2 size B blocks
PWB63 4322 026 73750	Printed-wiring board for use in UMC60.	
	Material	glass-epoxy
	Accommodation	6 size A or 3 size B blocks

STICKERS (drawing symbols on self-adhesive transparent material)

4322 026 36481	50 sheets of stickers for 60-Series Norbits (without 4.NOR60).
4322 026 71941	50 sheets of stickers for 60-Series Norbits (without 4.NOR60).
4322 026 71961	50 sheets of stickers for 60-Series Norbits (incl. TT60).
4322 026 71971	50 sheets of wiring layout stickers for 60-Series Norbits. Actual-size pin distances.
4322 026 71981	50 sheets of wiring layout stickers for 61-Series Norbits. Actual-size pin distances.

BREADBOARD BLOCK
for 60-series NORBITS

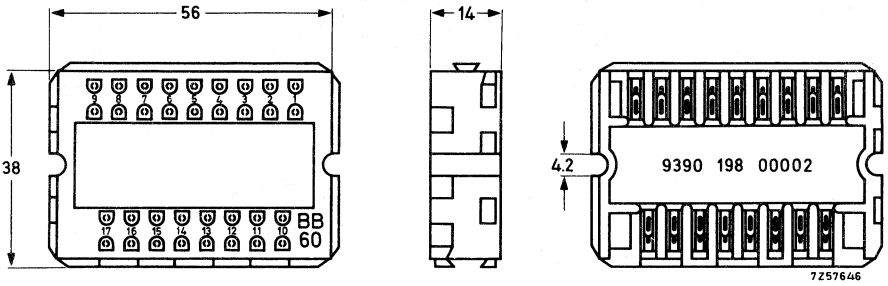


RZ 27447-18

APPLICATION

The "Breadboard Block", BB60, has been produced as an aid to 60-Series logic system design. Each block takes one size A unit from the 60-Series, and each block can be firmly locked on any of its edges to another BB60 block, thus a breadboard base can be built up to accommodate any size and complexity of logic circuit, interconnections being simply made with hook-up wire plugged into cup-shaped contacts. The BB60 blocks are ideal as experimenting and teaching aids. For instance, with four units 4. NOR60, one unit TU60 and one unit 2. LPA60 mounted on a base of six blocks BB60, it is easy to realize a large number of instructive logic circuits. Such a base of six blocks can be mounted in the Universal Mounting Chassis UMC60.

DESCRIPTION



(Dimensions in mm)

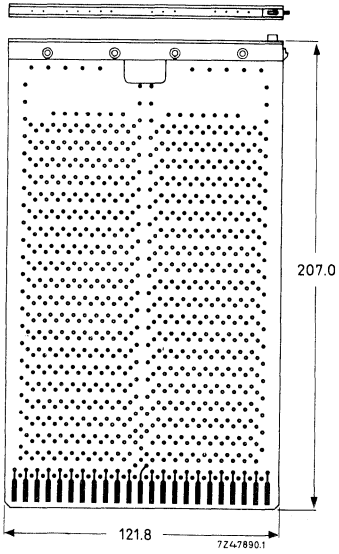
The right figure shows the underneath of the block with the 2 x 17 soldering lugs; the 60-Series units can be soldered directly onto these lugs. In the top view the cup-shaped contacts are visible; interconnecting wires or discrete components such as resistors can be plugged in on this side. There are two contacts for each terminal of a 60-Series unit, which facilitates multiple connections.

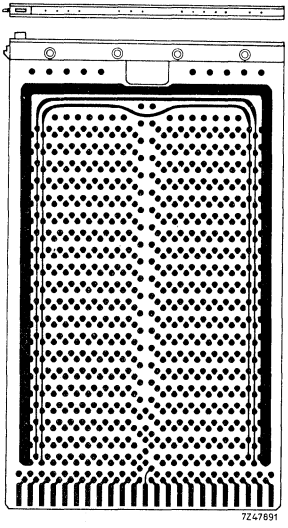
Body material	rigid grey plastic
Contacts	cup shaped, silver plated, suited for wires up to 1 mm diameter
Weight	20 g
Delivery	in packs of six, plus six sheets of wiring lay-out stickers for the 60-Series units.

The stickers are drawing symbols on self-adhesive transparent material, and they can be stuck to the top side of the breadboard blocks or be used for circuit drawings. The catalogue No. of a sheet is 9399 269 15301.

EXPERIMENTERS' PRINTED-WIRING BOARD

Experimenters' printed-wiring board (with extractor) with plated-through holes suitable for 60-Series NORbits. It fits mounting chassis 4322 026 38240.





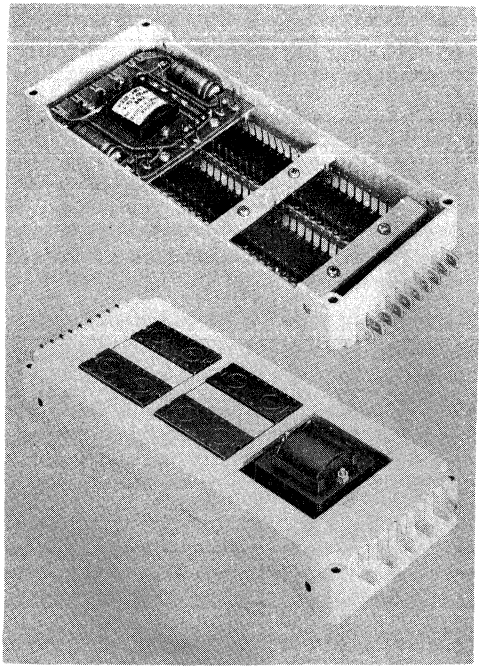
Accommodation of NORbits

size A	+ size B (HPA60)
10	0
8	1
6	2
3	3
0	4

Material of version GPB60	glass-epoxy
of version GPB60/P	phenol paper
Hole diameter	1,2 mm
Contacts	2x23, gold plated, pitch 0,2"
Mating connector	2422 020 52591 (type F045)

For more information, see Application Note "Printed-wiring boards for 60-Series Norbit Assemblies", No. 32/522/BE.

LOGIC SUPPLY UNIT



LSU60 mounted in UMC60

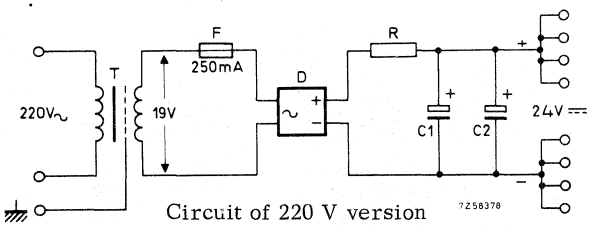
APPLICATION

The LSU60 is a power supply unit for small systems with 60-series NORbits. It is intended to be mounted in the universal mounting chassis UMC60. There is a version for 220 V mains (4332 000 01000) and one for 110 V mains (4332 000 01010).

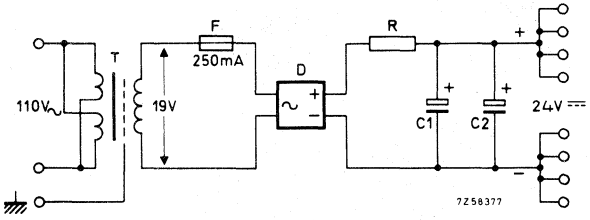
DESCRIPTION

The unit takes the same place as a size B Norbit block (HPA60). To mount the unit in the UMC60, the material between the two adjacent size A holes in the chassis should be removed, after which the unit can be fixed with 4 self-tapping screws.
Slots in the board of the LSU60 facilitate the connection of the input voltage and the output voltage to the Fastons of the UMC60, for external connection to the chassis. The other three pairs of output terminals are soldering tags intended for connection to Norbit blocks on the chassis. A 250 mA fuse (F) is inserted in the secondary part of the circuit. Its catalogue number is 4822 253 20011.

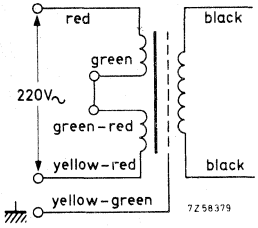
Circuit



Circuit of 220 V version



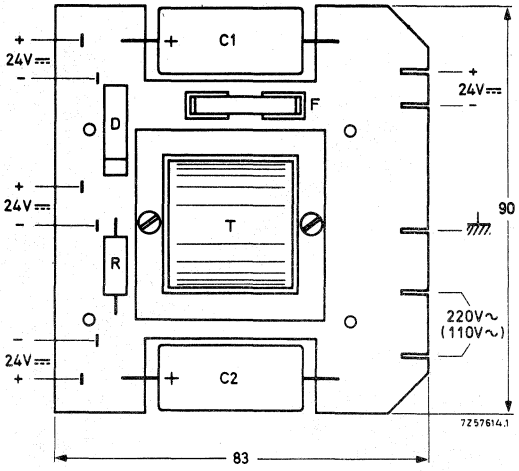
Circuit of 110 V version



Transformer of 110 V version changed for 220 V.

Outline and connections

Dimensions in mm



→ Weight approx 250 g

ELECTRICAL DATA

Input voltage	
version 4332 000 01000	220 V a.c., +10%, −15%
version 4332 000 01010	110 V a.c., +10%, −15%
Input frequency	45 to 400 Hz
Output voltage at 0 mA	< 30 V d.c.
at 150 mA	> 18 V d.c.
Temperature range	−10 to +70 °C
Test voltage for 1 min,	
across input terminals and earth	2 kV r.m.s.
across output terminals and earth	2 kV r.m.s.

0,5 A MAINS FILTER

APPLICATION

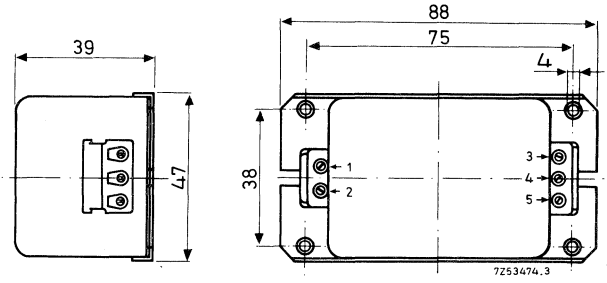
This mains filter can be used:
- either between mains supply connection terminals and the mains inputs of control systems, to suppress malfunctioning by transients,
- or between transient-generating equipment and its supply, to prevent high-frequency interference entering into the mains.

The attenuation for frequencies between 0,1 and 10 MHz, at 0,5 A supply current is 50 dB.

CONSTRUCTION

Unit is potted in a metal housing.

Dimensions in mm



Weight: 280 g

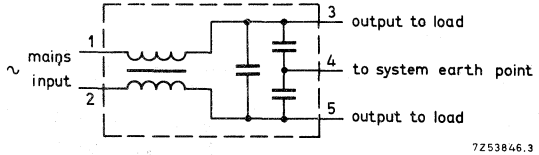
ELECTRICAL DATA

Maximum input voltage	250 V a.c.
Maximum current at T_{amb} = 40 °C	0,75 A a.c.
at T_{amb} = 70 °C	0,5 A a.c.
Repetitive peak current, 50 Hz	≤ 2,5 A
Non-repetitive peak current for 2 s	≤ 2,5 A
Insulation resistance between terminals and case	> 5 MΩ

Test voltages

a) for 1 min, across terminals and case	2000 V, 50 Hz
b) for 2 s across terminals 1 and 2, or 3 and 5	1625 V d.c.
c) for 2 s across terminals 3 and 4, or 4 and 5	1800 V, 50 Hz
Attenuation between 0,1 and 10 MHz	> 50 dB

Circuit diagram



Operating temperature range	−25 to + 70 °C
Storage temperature range	−25 to + 85 °C

TEST SPECIFICATIONS

The filter meets the tests of MIL-STD-202E

1. Thermal shock test according to method 107D, 5 cycles from −25 to + 85 °C
2. Moisture resistance test according to method 106D
3. Humidity test according to method 103B, condition D40 °C, 90 to 95% R.H.

2,4 A MAINS FILTER

APPLICATION

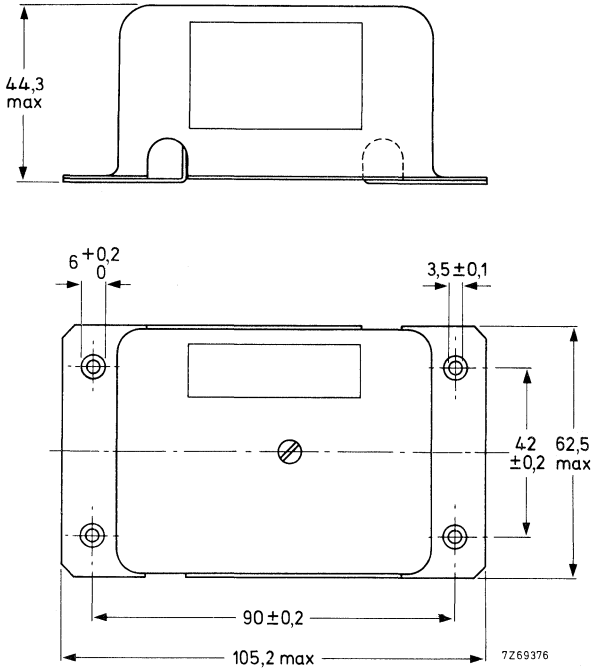
This mains filter can be used:
- either between mains supply connection terminals and the mains inputs of control systems, to suppress malfunctioning by transients,
- or between transient-generating equipment and its supply, to prevent high-frequency interference entering into the mains.

The attenuation for frequencies between 0,5 and 10 MHz, at 2,4 A supply current is 40 dB.

CONSTRUCTION

The unit is encapsulated in a metal housing.

Dimensions in mm

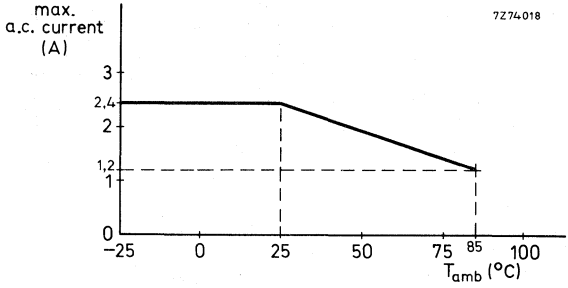


Weight: 275 g

ELECTRICAL DATA

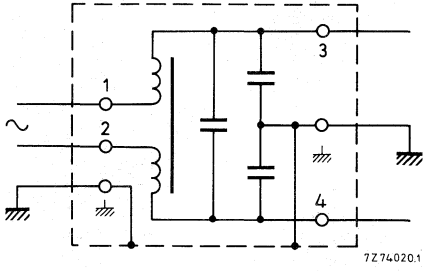
The values given below apply only to filters which are used in earthed installations.

Maximum input voltage	250 V a.c.
Maximum current at T_{amb} = 25 °C	2,4 A a.c.
at T_{amb} = 85 °C	1,2 A a.c.



Repetitive peak current, 50 Hz	≤ 10 A
Non-repetitive peak current for 2 s	≤ 10 A
Impedance at 2,4 A	0,925 Ω
Insulation resistance between terminals and case	> 5 MΩ
Test voltage	
for 2 s between terminals and case	2700 V d.c.
for 2 s between input or output terminals	1625 V d.c.
Attenuation between 0,5 and 10 MHz	> 40 dB

Circuit diagram



Operating and storage temperature range	−25 to + 85 °C

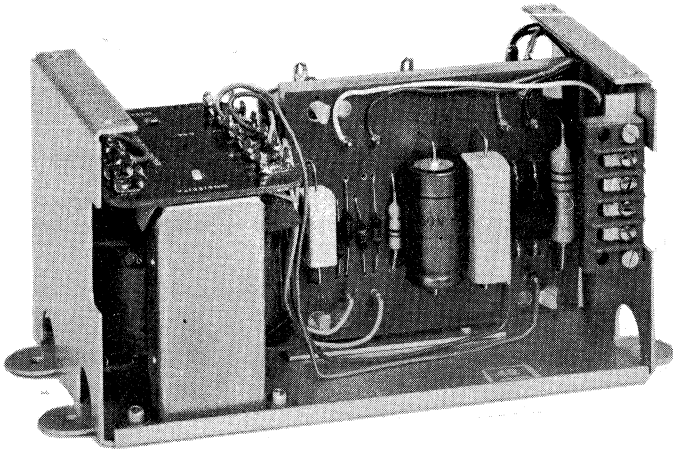
TEST SPECIFICATIONS

The filter meets the tests of MIL-STD-202E:

- thermal shock test according to method 107D, 5 cycles from −25 to + 85 °C
- moisture resistance test according to method 106D

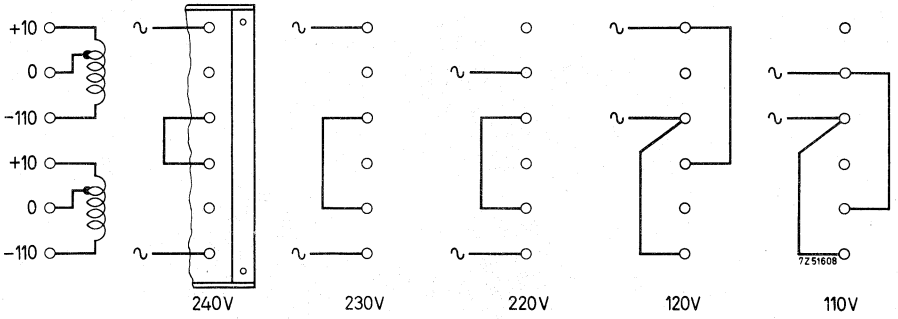
The capacitor used meets the requirements of VDE 0560-7.

POWER SUPPLY UNITS
for 60-series NORBITS

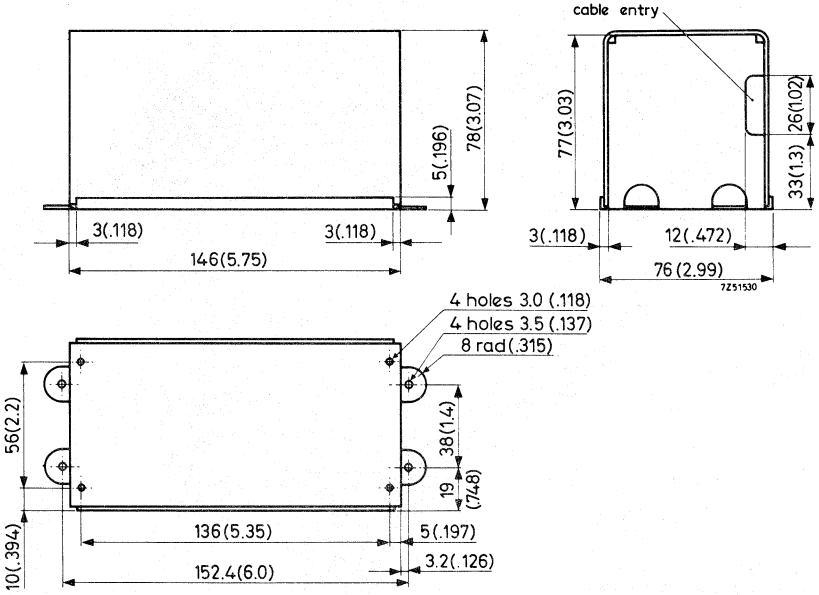


(Cap removed from unit.) RZ 23469-1

Input voltage	240, 230, 220, 120 or 100 V_{ac}, +10%, -15%
Input frequency	47 to 440 Hz
Output	< 30 V at 0 mA, > 18 V at 500 mA (for logic supply)
Additional output PSU 61	+100 V ±25% at 0 to 25 mA (for Switch Filters)
Operating ambient temperature	-10 to +60 °C
Test voltage between windings	2 kV



Input facilities of mains transformer



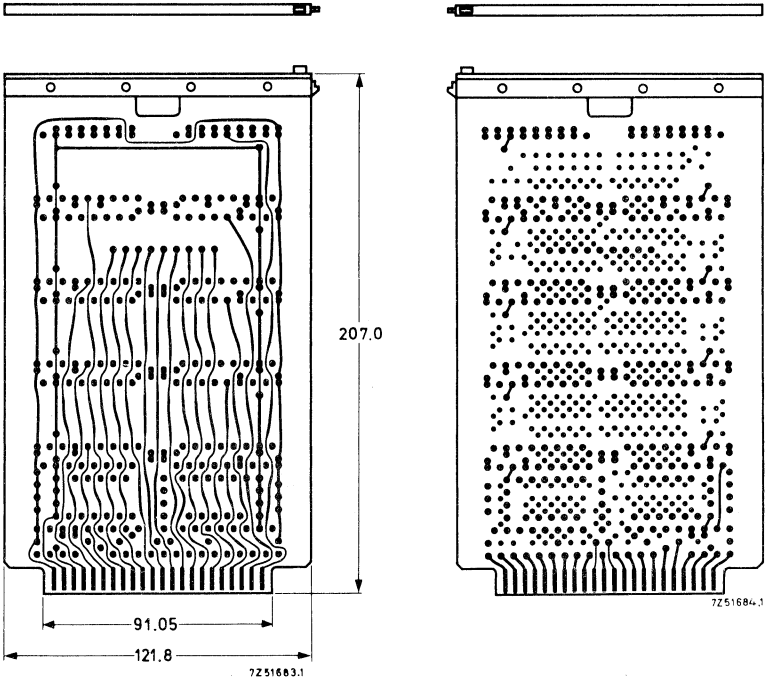
Dimensions in mm, inch values between brackets.

Case: aluminium

Weight: approx. 1000 g

EXPERIMENTERS' PRINTED-WIRING BOARDS for 60-series NORBITS

Experimenters' printed-wiring boards (with extractor) with plated-through holes, and 0-volt supply line tracks for pins 9 and 16. They fit mounting chassis 4322 026 38230.

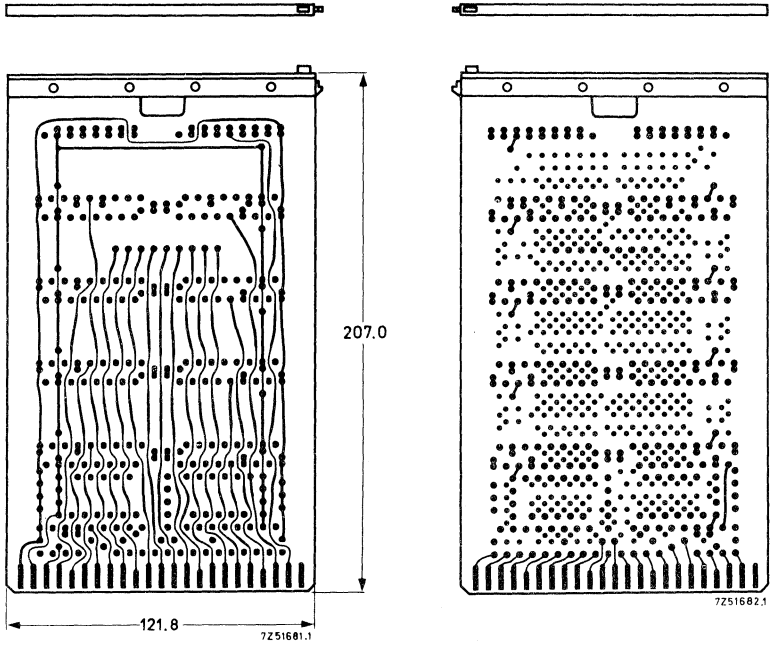


Accommodation	ten blocks size A
Material of version 4322 026 38790 of version 4322 026 38800	glass-epoxy (PWB 60) phenol paper (PWB 60/P)
Hole diameter	1.3 mm
Contacts	2x22, gold plated, pitch 0.156"
Mating connector	types F047, F050, F053

For more information, see Application Note "Printed-wiring boards for 60-series Norbit Assemblies", No. 32/522/BE.

EXPERIMENTERS' PRINTED-WIRING BOARDS for 60-series NORBITS

Experimenters' printed-wiring boards (with extractor) with plated-through holes, and 0-volt supply line tracks for pins 9 and 16. They fit mounting chassis 4322 026 38240.

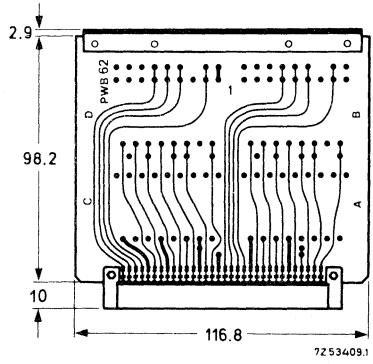


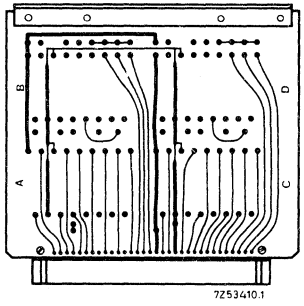
Accommodation	ten blocks size A
Material of version 4322 026 38810 of version 4322 026 38820	glass-epoxy (PWB 61) phenol paper (PWB 61/P)
Hole diameter	1.3 mm
Contacts	2x23, gold plated, pitch 0.2"
Mating connector	2422 020 52591 (type F045)

For more information, see Application Note "Printed-wiring boards for 60-series Norbit Assemblies", No. 32/522/BE.

PRINTED–WIRING BOARD
for 60–series NORBITS

Printed-wiring board with plated-through holes, extractor and complete F054 connector, of which the female part has been soldered to the board. All terminals of any Norbit mounted on the board are brought out. The 0-volt pins and the positive supply pins have been tracked together for all Norbits.
The board fits the miniature mounting chassis 4322 026 38250.
The board is especially useful for systems where a small number of types (board + blocks) is essential with a view to replacement.





Accommodation	size A + size B (HPA60)
	4 | 0
	2 | 1
	0 | 2
Material	glass-epoxy
Hole diameter	1.2 mm
Connector	
type	F054 (2422 025 89082)
contacts	2 x 32
contact pitch	2,54 mm (0,1")
terminations	suitable for mini wire-wrapping

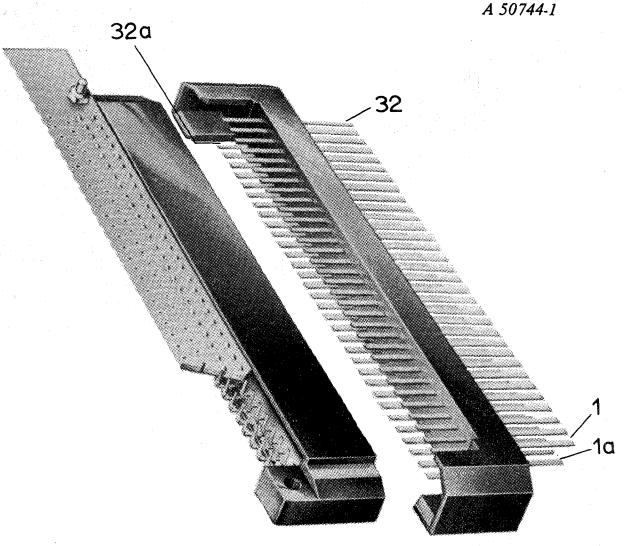
INTERCONNECTION DIAGRAM

The designer of an electronic circuit with Norbits mounted on PWB62 boards, can easily derive the necessary connecting instructions from the diagram depicted on the next page. With this diagram he can indicate the connections that are to be made. The diagram gives the numbers of the terminals of the circuit block, its position on the PWB62 and the numbers of the connector terminals (see photograph below).
The thin lines in the diagram represent the tracks of the printed circuit on the PWB62, so they indicate the interconnections between the Norbit terminals, and the connector pins.

All the designer has to do is to draw the connections which should be made by the wire man (see thick lines on the second diagram).

As an example we give an alarm circuit of which the designer has drawn the diagram in the upper part, and has indicated for the wire man on the lower part the external interconnections to be made. Moreover, outside the diagram the necessary connections to be made the supply with unit, the oscillator, switches, and so on, are indicated by the arrows.

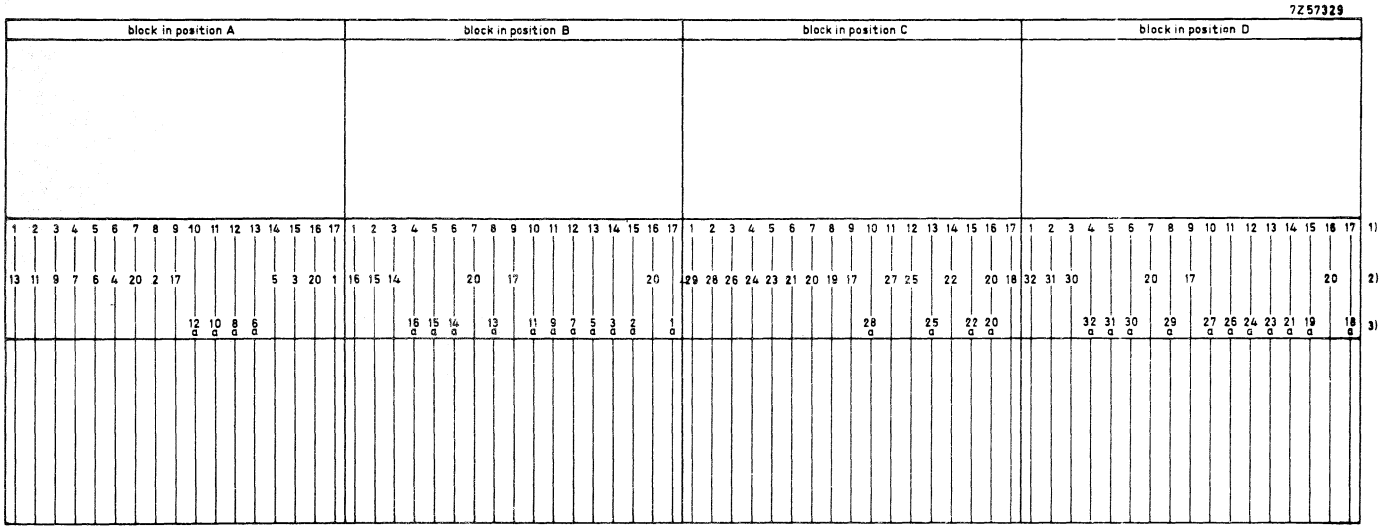
In this way the design engineer can draw the electronic circuit and the associated assembly instructions in one diagram.



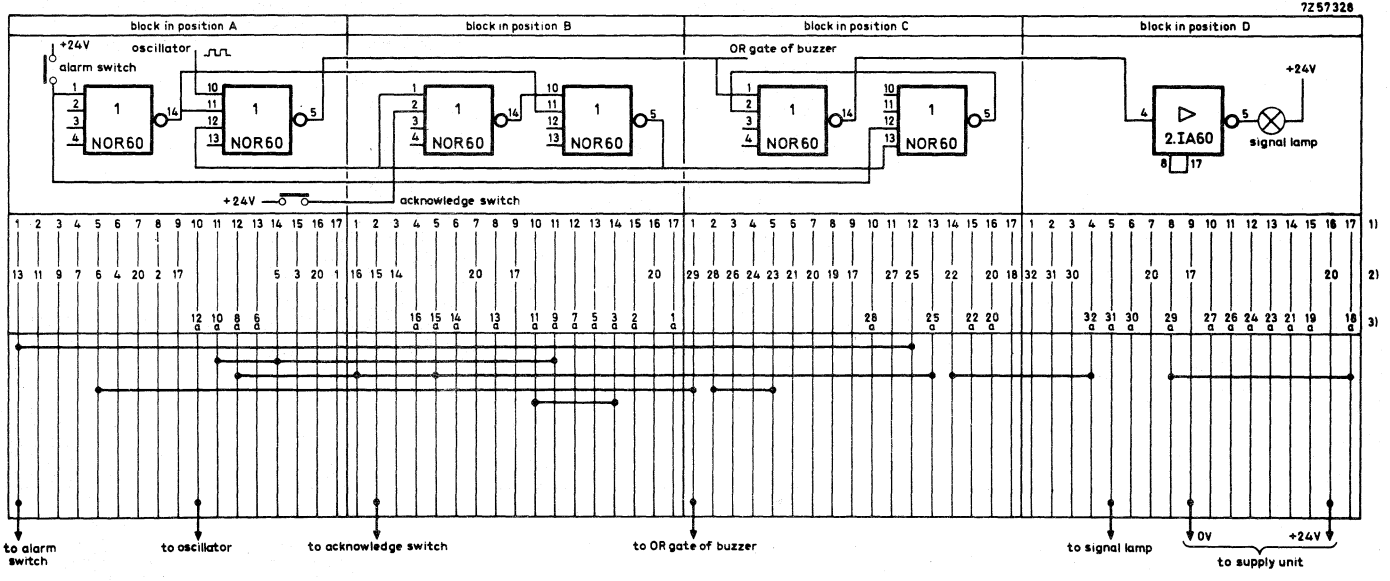
Connector pin numbering as used in Interconnection Diagram.

Interconnection diagram (containing track data)

See example next page.



Example

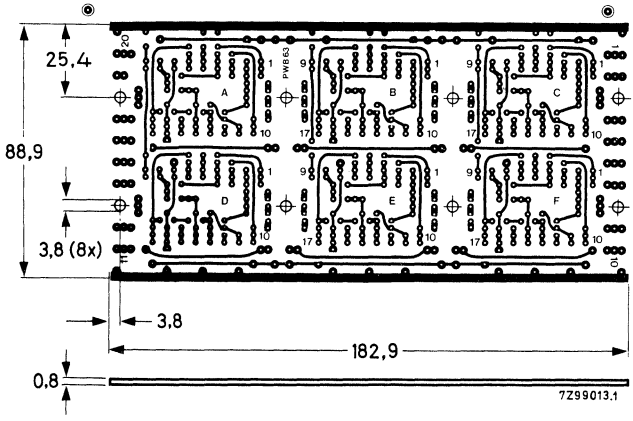


1) Terminal number of circuit block inserted in PWB62

2) Pin number of male F054 connector (se photograph) to which track on the "solder side" (bearing no type number) is connected

3) Pin number of male F054 connector (see photograph) to which track on the "components side" (bearing type number) is connected.

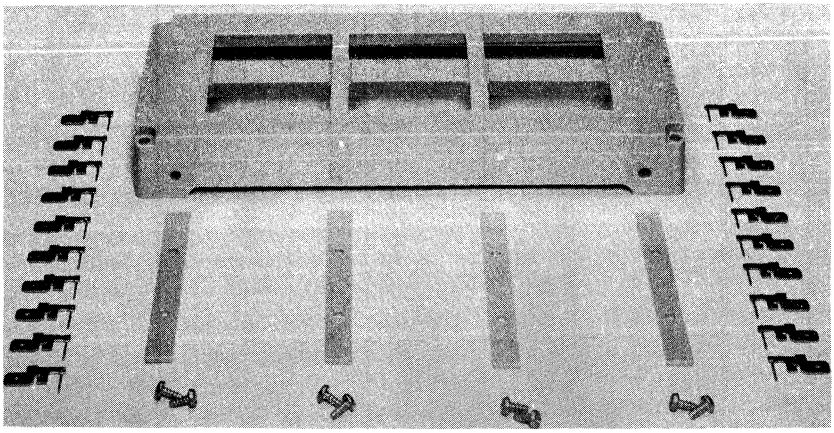
PRINTED-WIRING BOARD for UMC60



Single-sided printed-wiring board (with holes) intended for use in a Universal Mounting Chassis UMC 60.
Tracks have been laid such that only short jumpers need be used to obtain all kinds of logic functions with Norbits.

Accommodation (60-series blocks)	6 size A or 4 size A + 1 size B (HPA60) or 2 size A + 2 size B or 3 size B
Material	glass-epoxy
Board thickness	0,8 mm
Hole diameter	1,2 mm

UNIVERSAL MOUNTING CHASSIS
for 60-series NORBITS



RZ 26441-7

APPLICATION

Low cost mounting facility for:

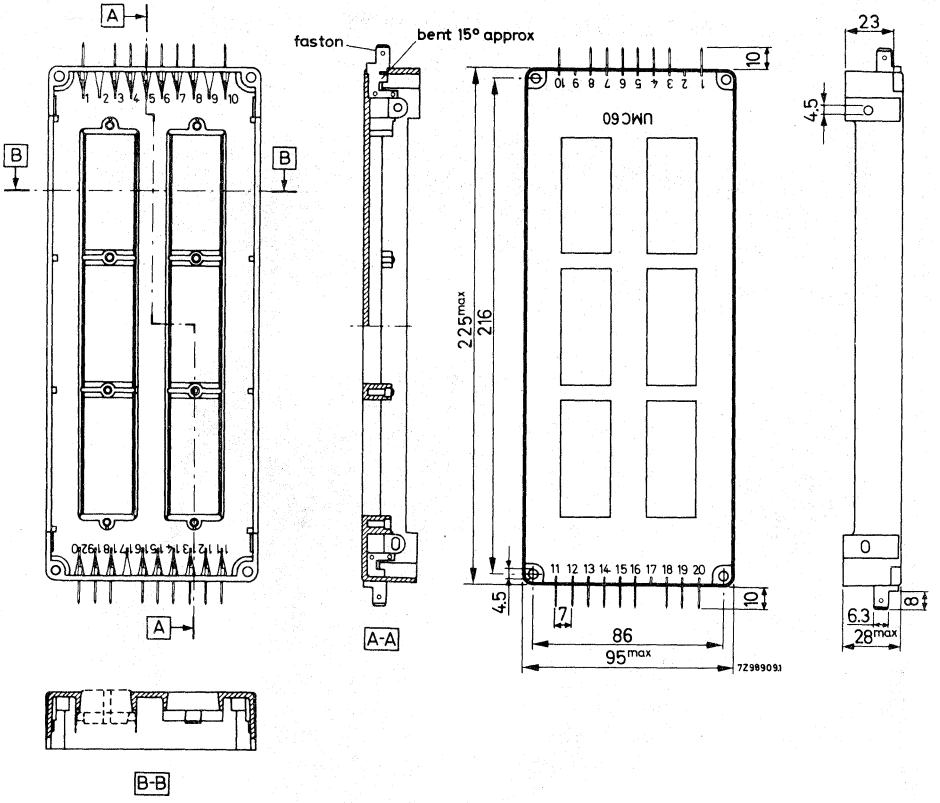
6 size A blocks,
or 4 size A blocks and 1 size B block (HPA60)
or 2 size A blocks and 2 size B blocks
or 3 size B blocks.

The chassis provides an alternative for mounting 60-series blocks on a printed-wiring board with connector.
Chassis can be bolted together side by side (Fig.4); they may also be stacked (Fig.5 and Fig.6) or hinged.

DESCRIPTION

The delivery includes a moulded polycarbonate chassis body, 4 moulded polycarbonate strips, 8 self-tapping screws and 20 standard 0.25 inch Fastons. Strips and screws are for clamping the circuit blocks into the holes in the chassis. The Fastons are for connections to the circuitry in the chassis.

To accommodate a size B block, it is necessary to remove the material between two size A holes, see Fig.1.
Interconnections between the terminal pins of the circuit blocks can be made by means of hand soldering or mini wire-wrapping; it is also feasible to use printed-wiring board PWB63 (catal. No. 4322 026 73750) in the chassis (see Fig.3).



Colour: grey

Dimensions in mm

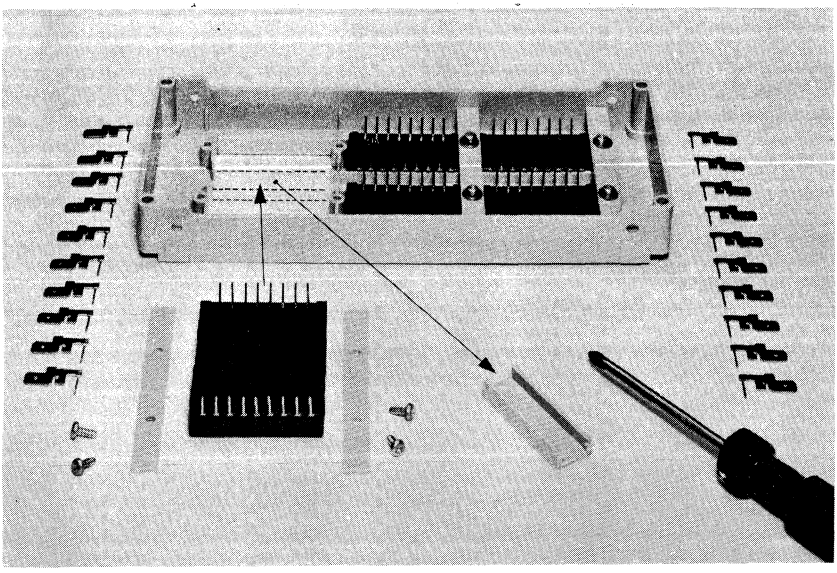
Weight: 150 g approx.

ASSEMBLY AND USE

The Fastons are brought in from the outside of a chassis and then fixed by bending the slotted part on the inside over about 15°

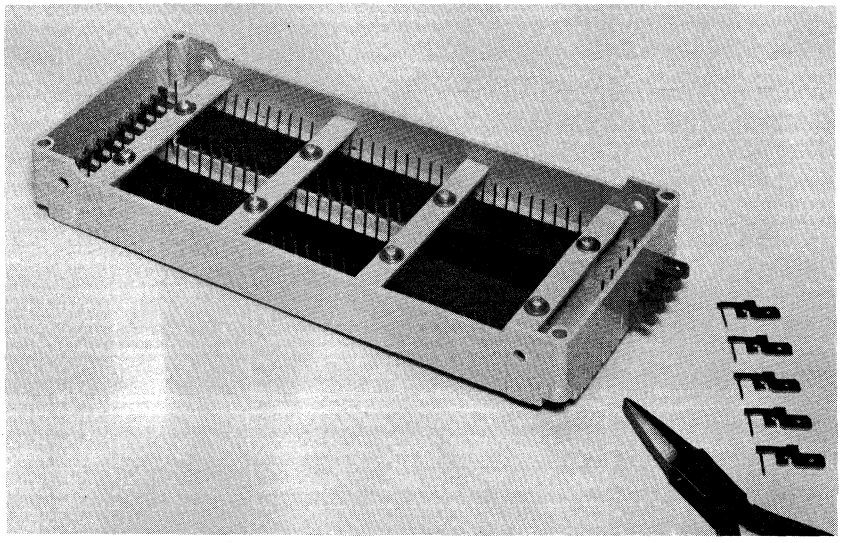
The blocks are clamped into the chassis with the strips and the self-tapping screws.

For fixing two or more chassis together, 4 mm bolts and nuts may be used.



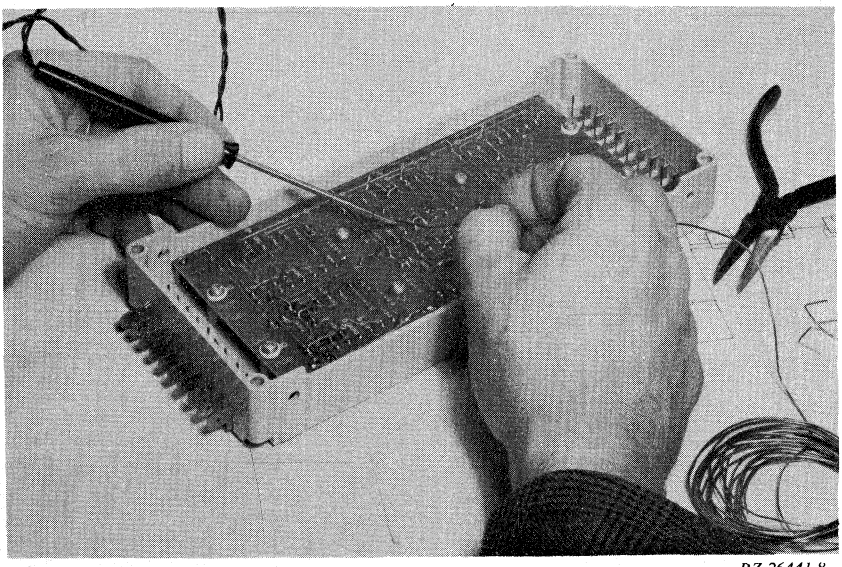
RZ 26441-6

Fig.1



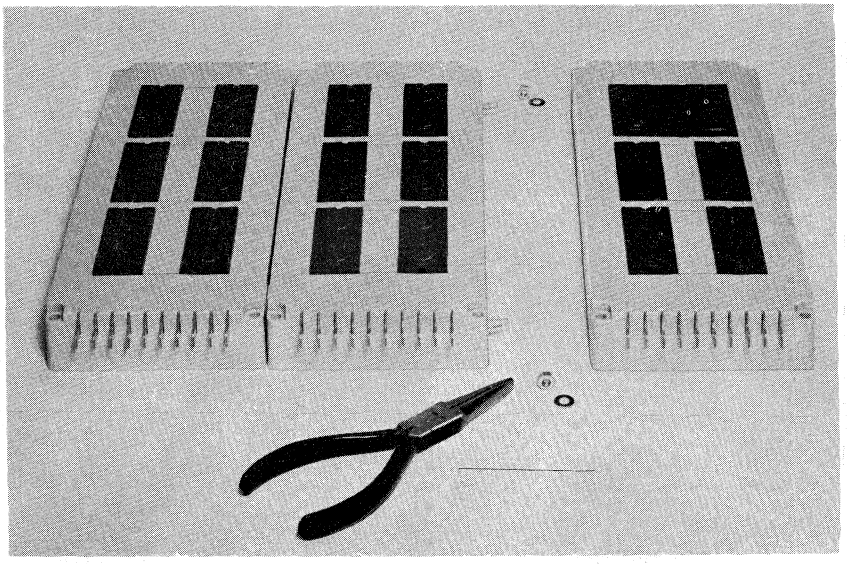
RZ 26441-3

Fig.2



RZ 26441-8

Fig.3



RZ 26441-4

Fig.4

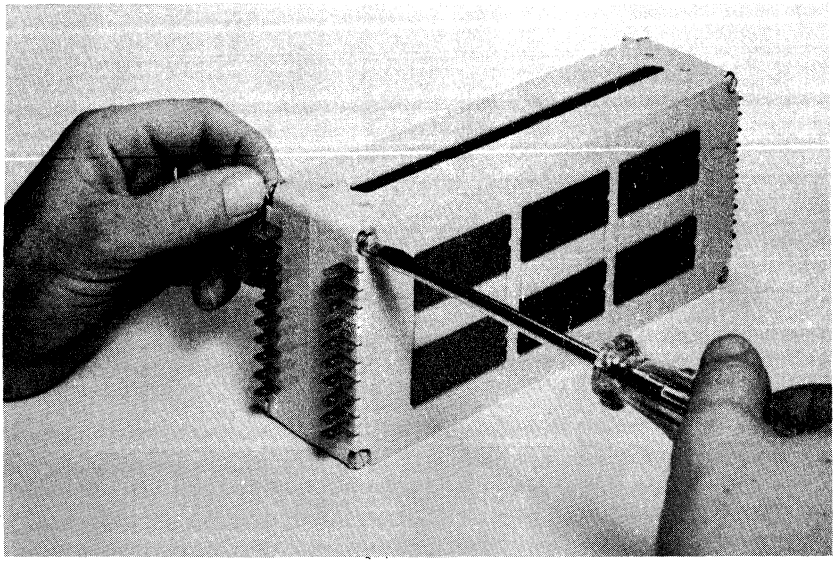


Fig.5 RZ 26441-9

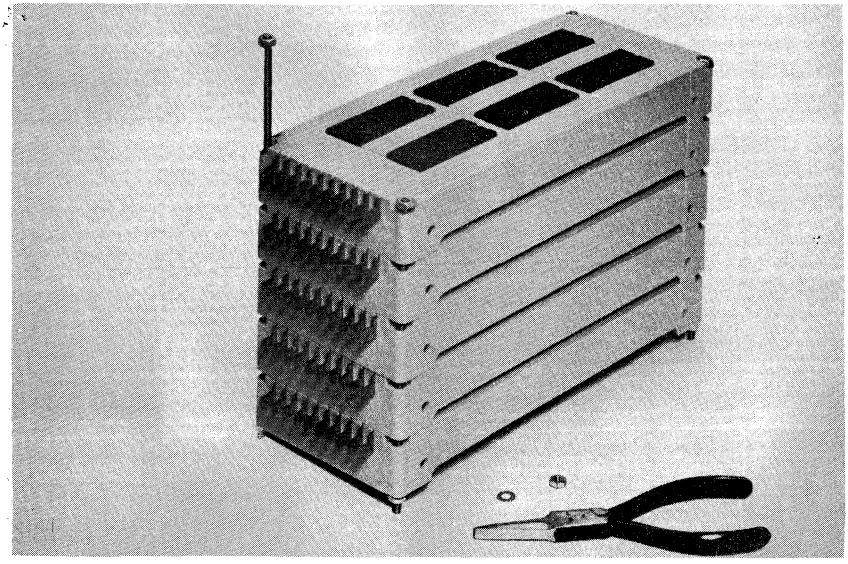
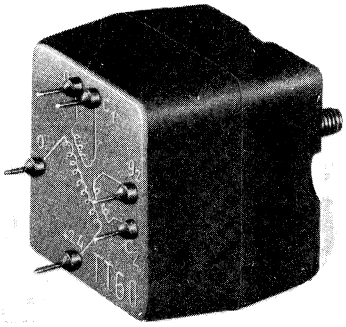


Fig.6 RZ 26441-10

THYRISTOR TRIGGER TRANSFORMER



A 51993

APPLICATION

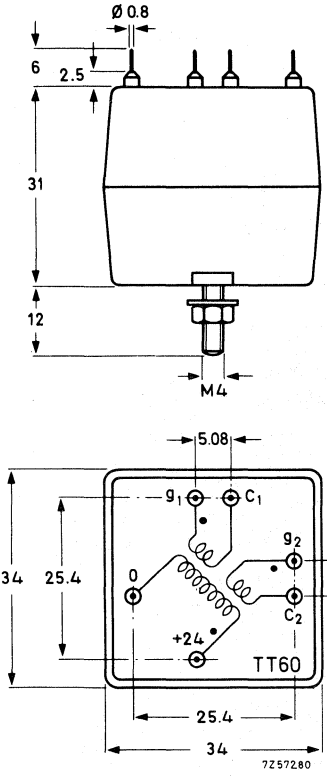
The TT60 can produce, in conjunction with the power amplifier UPA61, two pulse currents of up to 400 mA. This is sufficient gate current to trigger a pair of practically any type of thyristor.

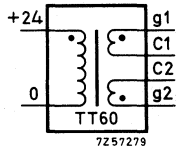
DESCRIPTION

The transformer has been encapsulated in a mould.
A threaded stud permits the unit to be fixed to a support (This may be the thyristor heat sink, to obtain short gate and cathode leads).

For the hand soldering of wires to the pins 7 wire spirals, catal.No. 4022 220 64781, are packed with the transformer.

Dimensions in mm





Drawing symbol

Weight: 80 g approx.

TECHNICAL PERFORMANCE

Turns ratio primary : sec_1 : sec_2	3 : 1 : 1
Inductance of primary winding	≥ 6 mH
Leakage inductance referred to primary (both secondaries short-circuited)	≤ 18 μH
Primary winding resistance at T_{amb} = 25 °C	≤ 0.5 Ω
Secondary winding resistance at T_{amb} = 25 °C	≤ 0.1 Ω
Test voltage between the windings for 1 minute	5 kV

Output pulse in response to step input, circuit of Fig.A, R_{eq} = 13 Ω:	
rise time	≤ 0,75 μs
pulse duration	≥ 20 μs
Primary current (r.m.s.)	max. 600 mA
Primary switched current, duty cycle 1:4	max. 1800 mA
ET product primary	900 μVs
Operating ambient temperature	-10 to +85 °C
Storage temperature	-40 to +85 °C

APPLICATION INFORMATION

Pulse amplifier circuit

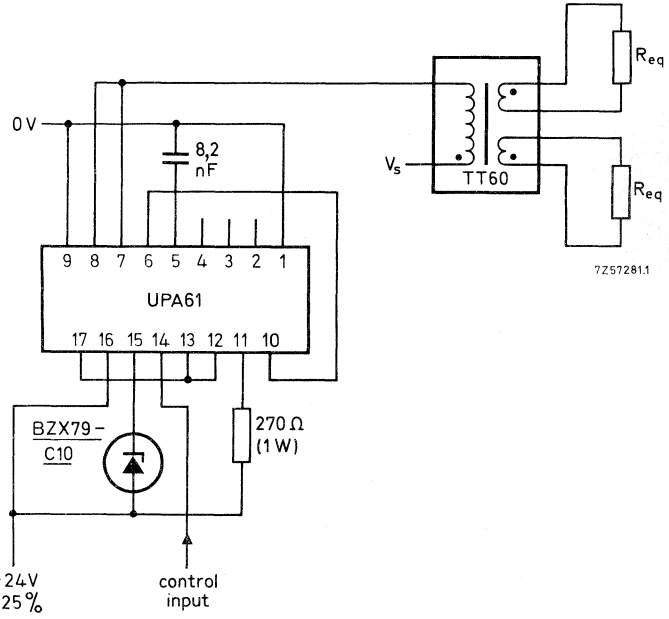


Fig. A

Power oscillator circuit

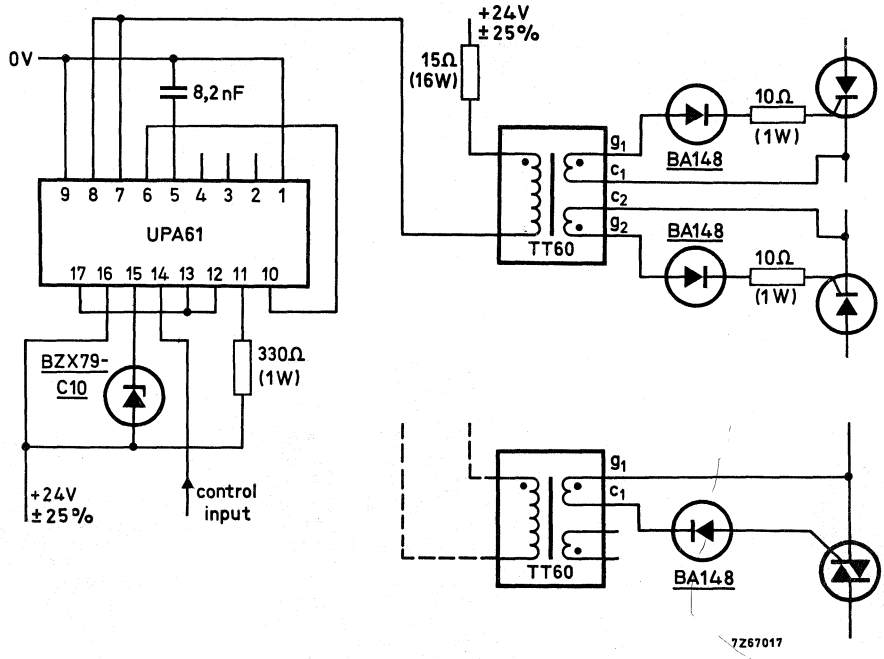
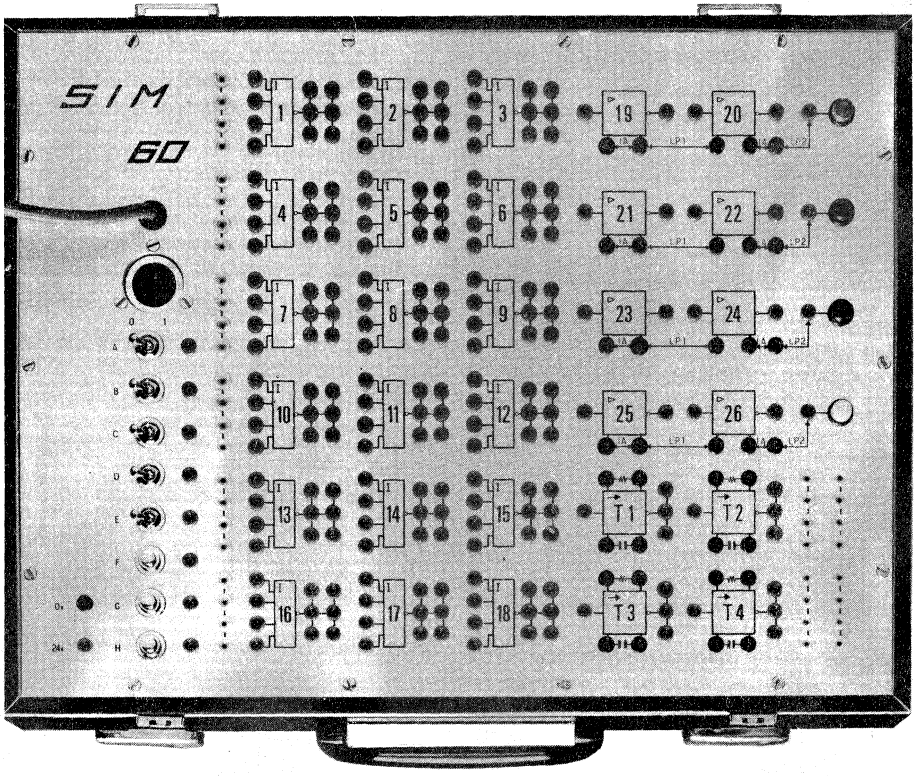


Fig. B shows the UPA61 as a 10 kHz power oscillator to trigger via TT60 a pair of thyristors or a triac.
Oscillation commences with a "high" (+ 12 V) on the control input (terminal 14 of the UPA61) ceasing when it becomes "low" (0 V).

LOGIC SIMULATOR
for 60-Series NORbits

Purpose	logic system design simulation (breadboarding) and instruction
Supply voltage	117/220/240 V, 50 or 60 Hz
Housing	attaché case 415 x 310 x 95 mm
Weight	5,5 kg

730806 - 19 - 01



DESCRIPTION

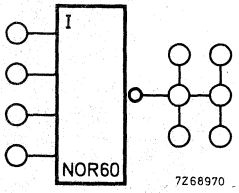
The SIM60 is a self-contained portable logic simulator, housed in a small light-weight attaché case, containing the following parts:

9 x	2. NOR60	5 x	toggle switch
4 x	2. IA60	3 x	push button
4 x	TU60	302 x	socket
1 x	power supply	10 x	patchcord, length 50 cm
4 x	indicator lamp	20 x	patchcord, length 30 cm
		10 x	patchcord, length 20 cm

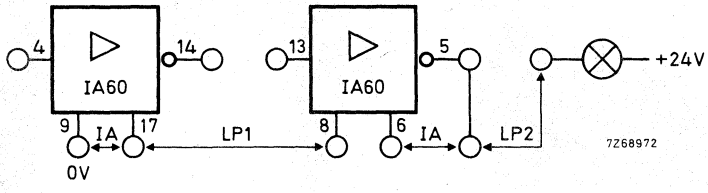
The circuit blocks are symbolized by rectangles and squares with adjoining input, output and auxiliary terminal sockets for patchcords. The fan-out of each block corresponds to the number of output sockets provided. Six groups of four auxiliary sockets (yellow) at the left and four groups at the right of the panel provide for concurrent application of signals to various control inputs.

Part description

2. NOR60 (see also relevant data sheet)
Units 1 to 18
18 NOR functions, each with 4 identical inputs and 6 paralleled output sockets.

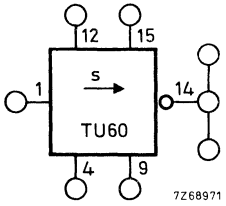


2. IA60 (see also relevant data sheet)
Units 19 to 26
8 inverting amplifiers;
Each 2. IA60 can be connected as an LPA60 to drive a load of 3 W at 24 V.



- To use the 2. IA60 as two inverting amplifiers, make the connections indicated by the arrows IA.
- To use the 2. IA60 as a single LPA60, make the connections indicated by the arrows LP1 and LP2.

TU 60 (see also relevant data sheet)
Units T1 to T4
Timer unit with 1 input and 3 paralleled output sockets. The time constant is determined by the resistance and capacitance connected externally between terminals 12-15 and 4-9, respectively.



Power supply (0 V, 24 V)

Suitable for operation from 117 V, 220 V or 240 V, 50 or 60 Hz, mains. Includes input cable and plug. Provides system 0 V and 24 V d.c. supply rails.

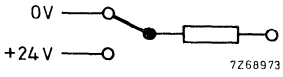
Indicator lamps

1 red
1 yellow
1 white
1 green

} can be used as output indicators for LPA60, one side connected to +24 V

Toggle switches (A to E) and push buttons (F toH)

To sumulate 1 or 0 input conditions and temporary 1 input signals, respectively.



output via internal current limiting resistance of 12 kΩ

Sockets

Colour indicates function:
Green = inputs
Red = outputs and 24 V
Black = other unit terminals and 0 V
Yellow = auxiliary sockets to multiply various signals

Note: The terminal socket marked '24 V' on the panel is connected directly to the +24 V supply rail, without current limiting resistor.

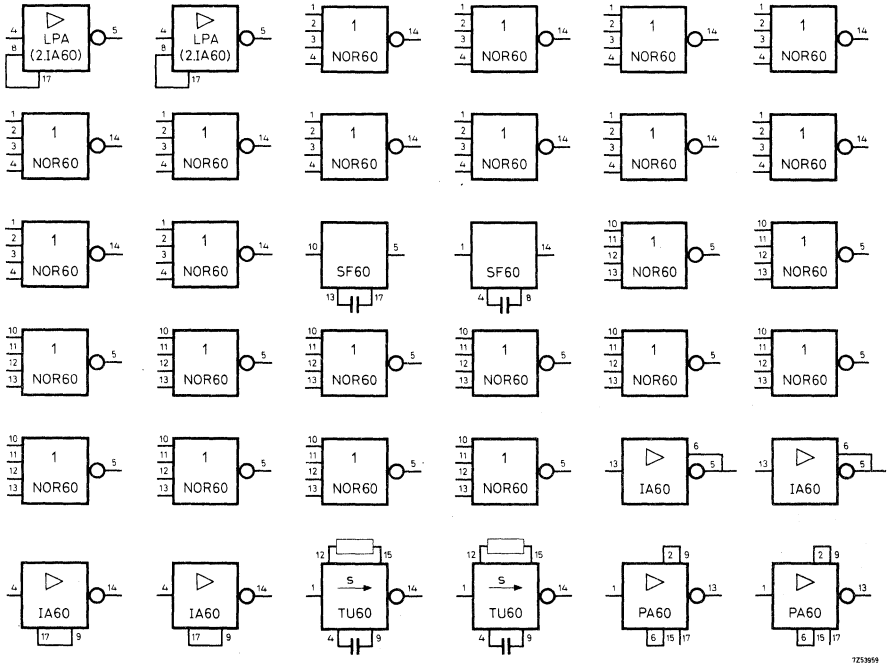
Application

Circuits for training purposes are given in Application Book "Control System Design Manual for 60-Series NORbits" under various headings.

CAUTION: Before plugging the SIM60 into the mains, be sure that the mains voltage selector on the panel is turned to the appropriate voltage.

STICKERS FOR THE 60-SERIES NORBITS

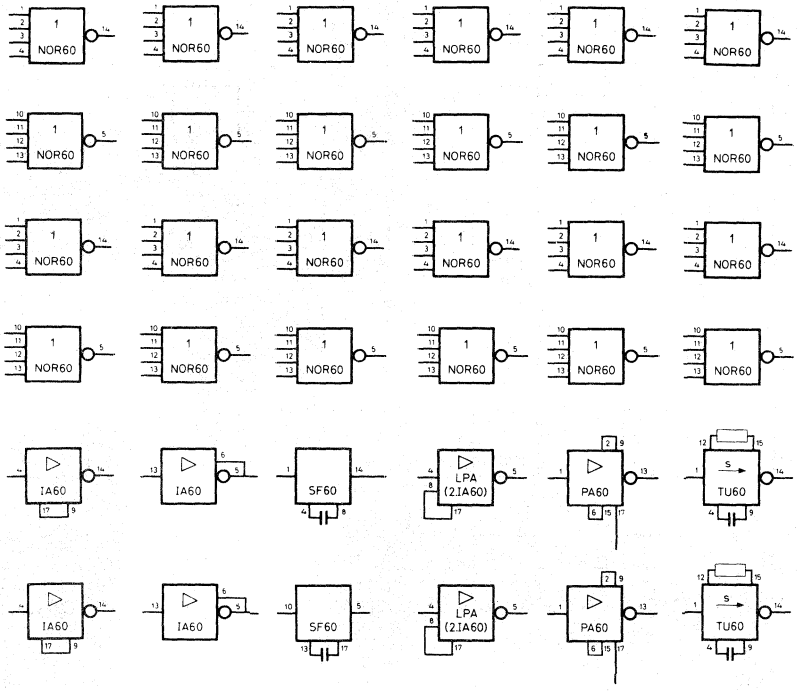
These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number of 50 sheets: 4322 026 36481.



Sticker sheet without 4. NOR60 or TT60

STICKERS FOR THE 60-SERIES NORBITS

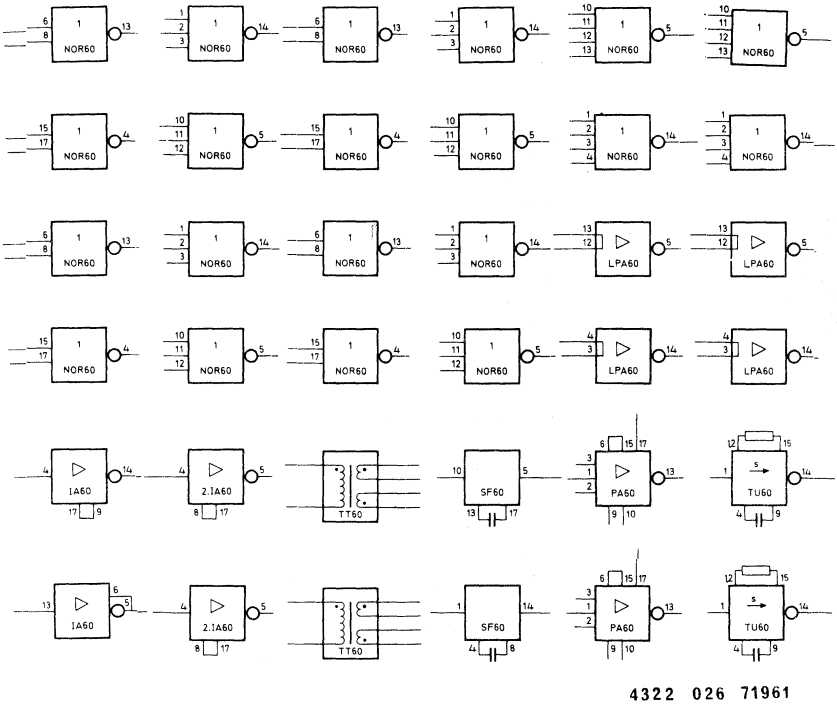
These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71941.



Sticker sheet without 4.NOR60 or TT60

STICKERS FOR THE 60-SERIES NORBITS

These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71961.

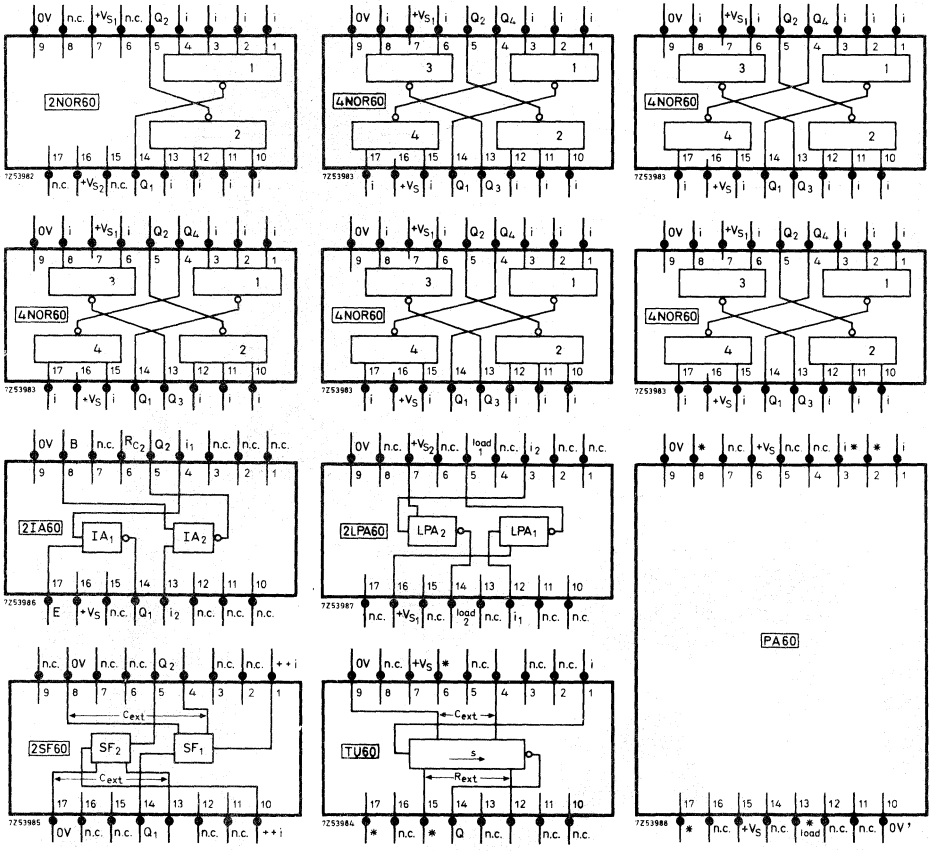


Sticker sheet with 4. NOR60 and TT60

WIRING LAYOUT STICKERS for the 60-series NORBITS

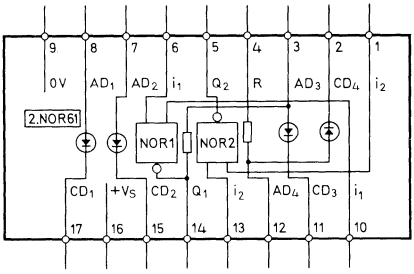
These are drawing symbols of 60-series blocks printed on self-adhesive, transparent material. They can be used for fast preparation of wiring layouts. All pin distances are actual size.

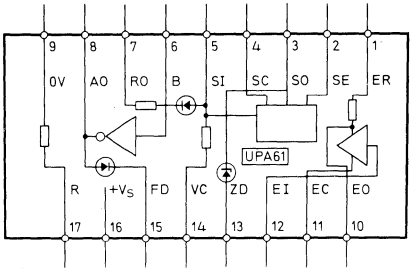
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71971.

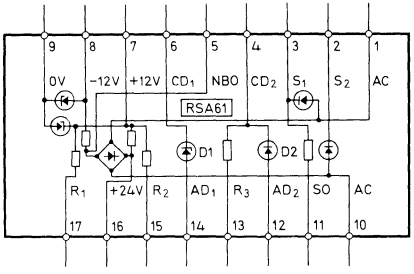


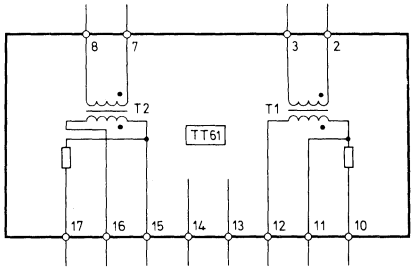
WIRING LAYOUT STICKERS for the 61-Series NORBITS

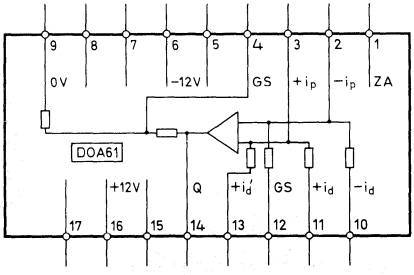
These are drawing symbols of 61-series blocks printed on self-adhesive,transparent material. They can be used for fast preparation of wiring layouts. All pin distances are actual size.
The stickers are available in sheets, each containing the five drawings shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71981.





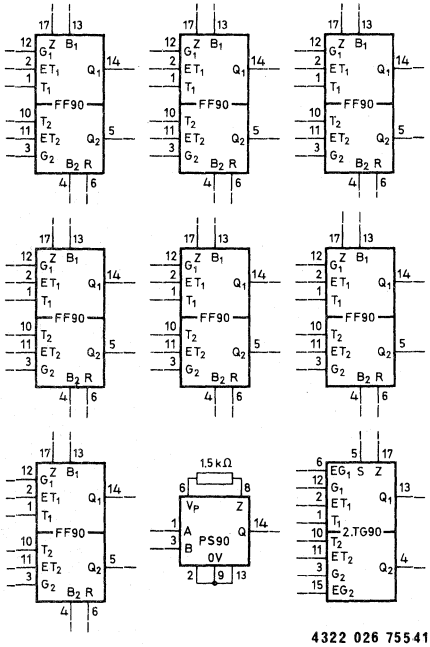






STICKERS FOR THE 90-SERIES CIRCUIT BLOCKS

These are drawing symbols of CIRCUIT BLOCKS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings.
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 75541.



OBSOLESCENT

All types mentioned in this chapter are obsolescent. They are available until present stocks are exhausted.

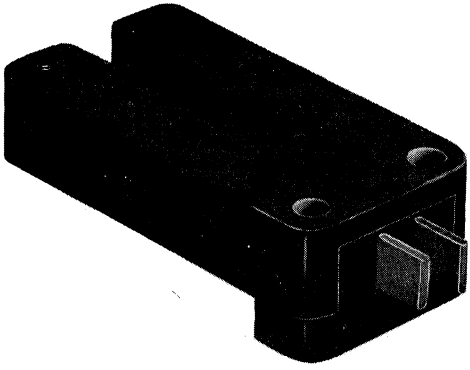
INTRODUCTION

Industrial control systems require compatible input devices that are capable of deriving signals representative of controlled or otherwise pertinent conditions. Though the information to be dealt with may take a variety of forms - e.g. presence, position, movement, rotation etc. - many different situations can be covered by a comparitively small selection of input devices.
The requirements of each situation determine the physical principle to be employed in the input device. For reasons of speed and reliability it is preferable to avoid mechanical contact in deriving the input signal, and often an all-static method of derivation is required. Experience with input devices has made it clear that skilful use of them can greatly improve machine output and reliability.

In this series the following units are available:

Data on input devices, and on output devices which are available for equipment production and for use in existing equipment, but are not recommended for equipment design (status C), are given in handbook CM7a.

IRON VANE SWITCHED REED



RZ21773-3

Maximum switching frequency	100 Hz
Operating-temperature range	−25 to +70 °C

APPLICATION

The iron vane switched reed can be applied as a limit switch, position indicator or as a signal source for low counting speeds.
In conjunction with d.c. amplifiers (UPA61, TT61 or TT60), the IVSR can be used for power switching.
As the IVSR is free from most of the difficulties encountered with mechanical switches, it can succesfully replace micro switches.

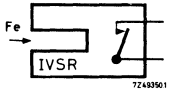
CONSTRUCTION

The IVSR consists of a magnet and a reed switch encapsulated in an U-shaped plastic housing.
When there is no piece of iron (vane) in the gap between the reed switch and the magnet, the reed switch is closed. Inserting a piece of iron of suitable dimensions in the gap reduces the magnetic flux through the reed to such an extent that the reed switch opens.
In this way it is possible to obtain signals that indicate the position of the iron vane.

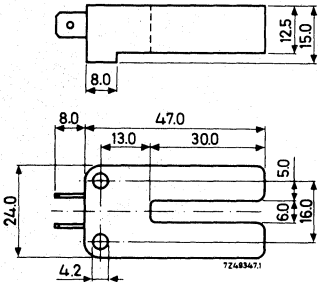
The weight is approximately 20 g.

The IVSR can be mounted in any position. Two mounting holes allow the use of 4 mm bolts. When IVSR's are mounted on a common support, the minimum distance between the housings is 36 mm, to avoid interaction. For mounting IVSR's over each other, this distance is 60 mm.

Connection can be made by means of 0,250" Fastons or by soldering.



Drawing symbol



Dimensions in mm

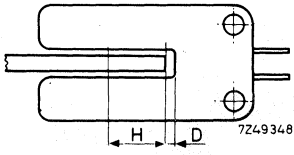
TECHNICAL PERFORMANCE

Load switching capacity (non inductive)	$\leq$ 1.2 VA
Voltage switching capacity	$\leq$ 32 V_{dc}
	$\leq$ 50 V_{ac}
Current switching capacity (non inductive)	$\leq$ 0.1 A_{dc}
Switching frequency	$\leq$ 100 Hz
Contact resistance, measured at 10 mV at open circuit	< 150 mΩ
Contact capacitance	$\leq$ 5 pF
Insulation resistance, measured at 250 V_{dc} at open circuit	$\geq 10^8$ Ω
Test voltage, measured at open circuit for 1 min	500 V_{dc}
Permissible operating-temperature range	−25 to +70 °C
Permissible storage-temperature range	−40 to +85 °C

APPLICATION INFORMATION (typical values)

Vane material: mild steel

The data given are based upon a movement of a mild steel vane 30 x 10 x 4 mm, placed centrally in the gap, in longitudinal direction.



The operating distance (D) is the distance between the front edge of the vane and the rear of the gap at which the reed switch opens.
The hysteresis (H) is defined as the distance between the vane position at which the reed switch opens and that at which the reed switch closes.

Operating distance	4 ± 3 mm
Hysteresis	10 ± 3 mm

APPLICATION SUGGESTIONS

As the reed switch is normally closed, the following two modes of operation can be distinguished:
- output voltage is present when there is no vane in the gap (Fig.a)
- output voltage is present when there is a vane in the gap (Fig.b)

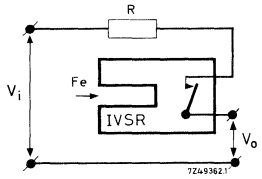


Fig.a

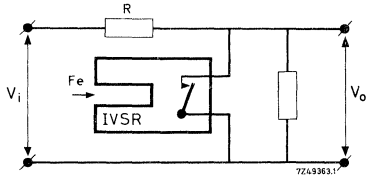


Fig.b

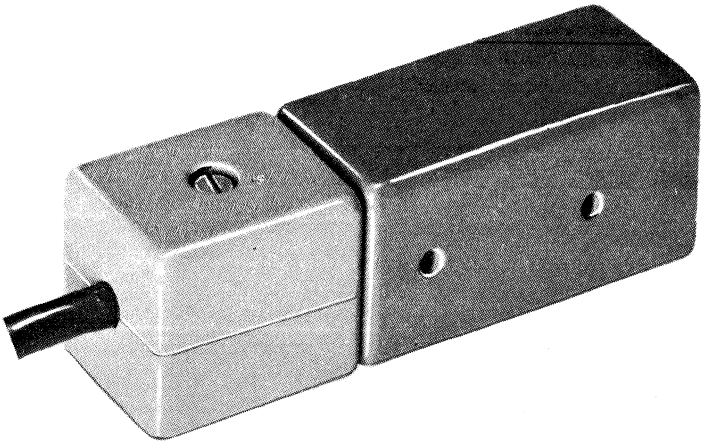
Notes

It is obvious that the IVSR should not be used in environments where iron dust or scraps might impair its operation.

It should be realised that capacitance directly across the switch terminals can be the cause of high currents through the switch at the moment of closing the contacts. This should be avoided by having sufficient resistance in the proper contact circuit.

In case the switch is used with electronic circuitry in which bounce might give rise to malfunctioning of the equipment, appropriate circuitry should be added to get rid of the bounce effect. The safe way out is the use of a one shot multivibrator.
Another solution that sometimes can be used, is applying a low pass RC network between the IVSR and the input of the equipment.

ELECTRONIC PROXIMITY DETECTOR



Supply voltage	12 V_{dc}
Maximum detection frequency	1 kHz
Operating-temperature range	−25 to +85 °C

GENERAL

The electronic proximity detector is a static switching device, the switching action being determined by the presence of a metallic object. The metal can be any electrically conducting material of rather arbitrary shape.
It can be applied as a detector for the presence, passage or position of metal parts and is a versatile tool in various industrial automation set-ups.

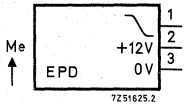
The EPD contains an oscillator which is link coupled to a detector. The detector is followed by an amplifier.
The oscillator coils and the coupling link are placed in a potcore half. In this way a well-defined field is set up in front of the open side of the potcore, located at the front side of the EPD. Bringing a piece of metal in this field the oscillator output and subsequently the output of the amplifier decreases, due to the loading effect of the eddy current losses in the metal.
When no piece of metal is near, the output voltage of the EPD is approximately 12 V. It will decrease in proportion to the reduction of the oscillator output, resulting from a metal object coming nearer.

The complete circuit is epoxy encapsulated in a polycarbonate housing.

The mass is approximately 120 g.

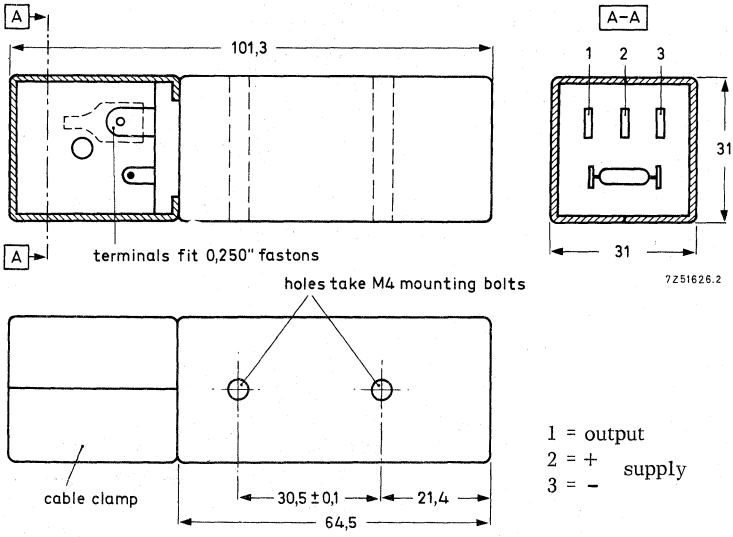
The unit may be mounted in any position. Two mounting holes allow the use of 4 mm bolts.

Connection can be made by 0,250" Fastons or by soldering. A cable clamp consisting of two equal caps is supplied with each EPD. This clamp permits either end or top entrance of a 3-core cable of 7 mm diameter.



Drawing symbol

Dimensions in mm



Note

The resistor between the two 0,110" Fastons is an adjustment resistor for the oscillator loop gain; it should not be changed.

TECHNICAL PERFORMANCE

Supply voltage, V_S (d.c.)	12 V ± 5% or +6 V ± 5% and −6 V ± 5% (with common 0 V) or 24 V via series resistor and 12 V zener diode, giving a stabilized supply voltage of 12 V. (See also Application Suggestions.)
limiting value	abs. max. 15 V* (destructive at $T_{amb} \geqslant 40\ ^{o}C$)
Consumed current	max 17 mA
Output voltage,	
no object being detected	approximately $V_S - 0{,}5$ V
object being detected	max 100 mV
Output resistance	
no object being detected	700 Ω
object being detected	3,4 kΩ
Hysteresis for output voltages of 100 mV – 11 V	0 mm
Output current	
no object being detected	max 14 mA
object being detected	max 3,7 mA
Maximum detection frequency, mark to space ratio 1 : 1	1 kHz
Noise (over supply lines)	< 10 mV
Ambient temperature range	
operating	−25 to +85 °C
storage	−40 to +85 °C

APPLICATION INFORMATION (typical values)

Detection graphs

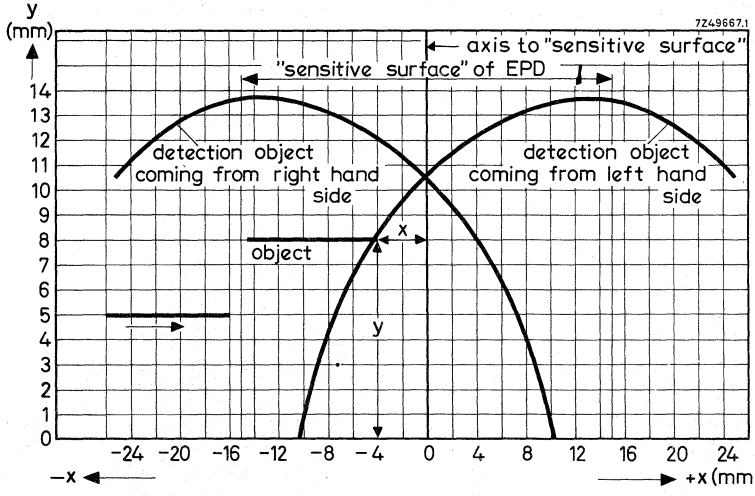
Detection of a rectangular mild steel reference object, 50 x 25 x 1 mm

Sensitive surface	surface of 31 x 31 mm at the opposite end of the EPD to the terminals
Axis	line perpendicular to the centre of the sensitive surface
Operating point	point at which the output voltage of the EPD is reduced to 100 mV (moment of detection)

* Reversal of supply voltage will damage the detector.

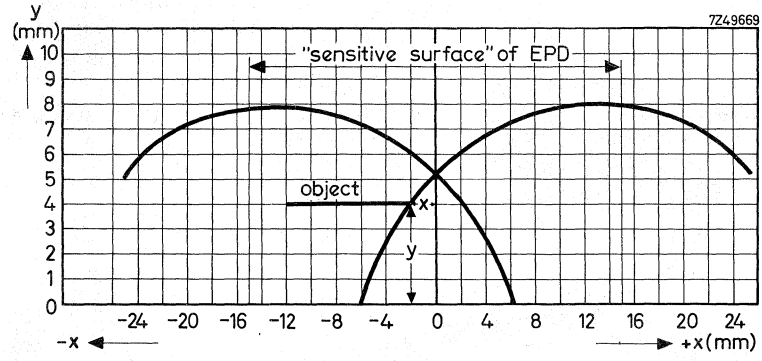
Operating distance — distance of the leading edge of the reference object to the axis at the operating point (x-operating distance)

Detection range — distance of the reference object to the sensitive surface (y-operating distance)



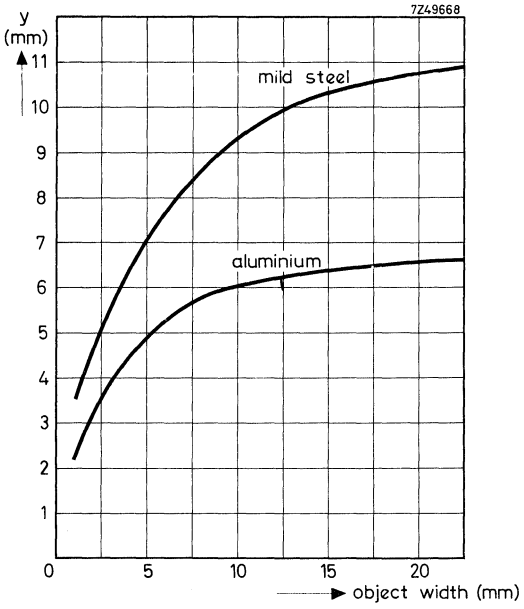
From the graph it can be seen that the object is detected before the axis is reached if it passes at a distance of < 10 mm from the sensitive surface. If it passes at a distance of e.g. 13.5 mm, the object is detected after the axis has been passed.

Detection of a rectangular aluminium reference object, 50 x 25 x 1 mm

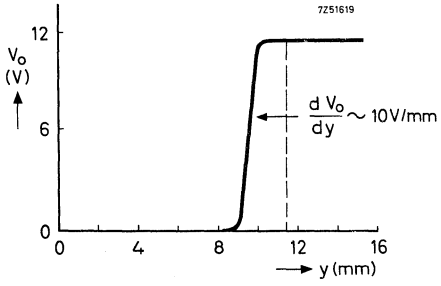


Detection of rectangular mild steel and aluminium reference objects (50 x 1 mm) with different widths

Object approaches the centre of the sensitive surface perpendicularly from in front.



Output voltage as a function of the position of a rectangular mild steel reference object, 50 x 25 x 1 mm



Upon frontal approach of the object to the sensitive surface, the output voltage of the EPD will change from over 11 V to 100 mV within 1 mm from the position in which the output voltage starts to change.
This characteristic is extremely important when the EPD is used as a position detector.

Notes:

The detection graphs may differ slightly from unit to unit.

Quite small objects can be detected when brought close to the sensitive surface. Thickness is relatively unimportant as eddy currents occur in penetration layer only.

Influence of supply voltage variations

A supply voltage variation of ±5% produces a change of ±0.1 mm in y-operating distance, at 10 mm from the sensitive surface.

Influence of temperature

With the reference object at a y-operating distance of 10 mm (at −25 °C) a change in temperature of both EPD and object will cause the y-operating distance to change less than 2 mm over the range from −25° to +85 °C.

Direction of approach

As the exterior field is rotation symmetrical the path along which the detection position is reached is immaterial.

Distance from metallic surroundings

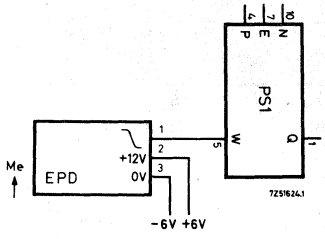
Clearance from metallic surrounding: 30 mm (this applies for sensitive front part of unit).

Spacing required between two detector axes with sensitive surface in the same plane: 60 mm.

Spacing required between two reference objects to give discrete detection: 50 mm. (This property can be put to use in feeder systems, a gap being used to initiate part supply restart.)

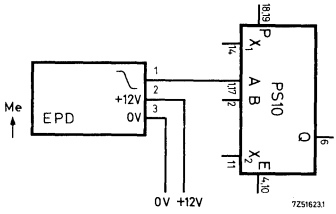
APPLICATION SUGGESTIONS *)

EPD in conjunction with 100 kHz-Series circuit blocks

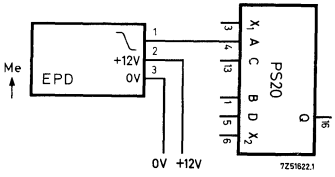


*) With long cables between EPD and subsequent electronics RC decoupling of interference can be employed.

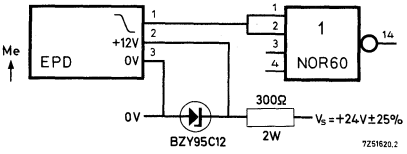
EPD in conjunction with 10-Series circuit blocks

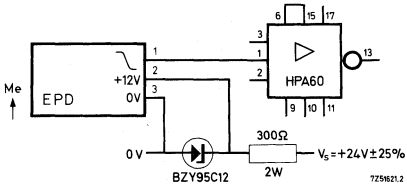


EPD in conjunction with 20-Series circuit blocks



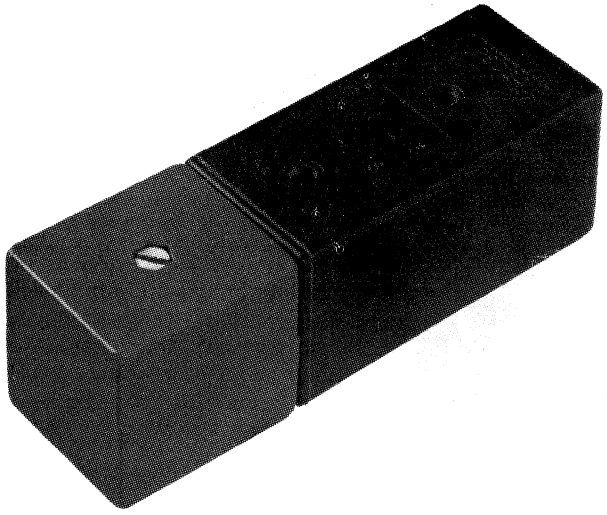
EPD in conjunction with 60-Series Norbits





PROXIMITY SWITCHED DETECTOR

770617-18-01



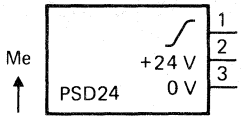
Supply voltage	24 V (d.c.)
Maximum detection frequency	1 kHz
Operating temperature range	–25 to +85 °C

GENERAL

The proximity switched detector is a static switching device, the switching action being determined by the presence of a metallic object. The metal can be any electrically conducting material of rather arbitrary shape. It can be applied as a detector for the presence, passage or position of metal parts and is a versatile tool in various industrial automation set-ups.

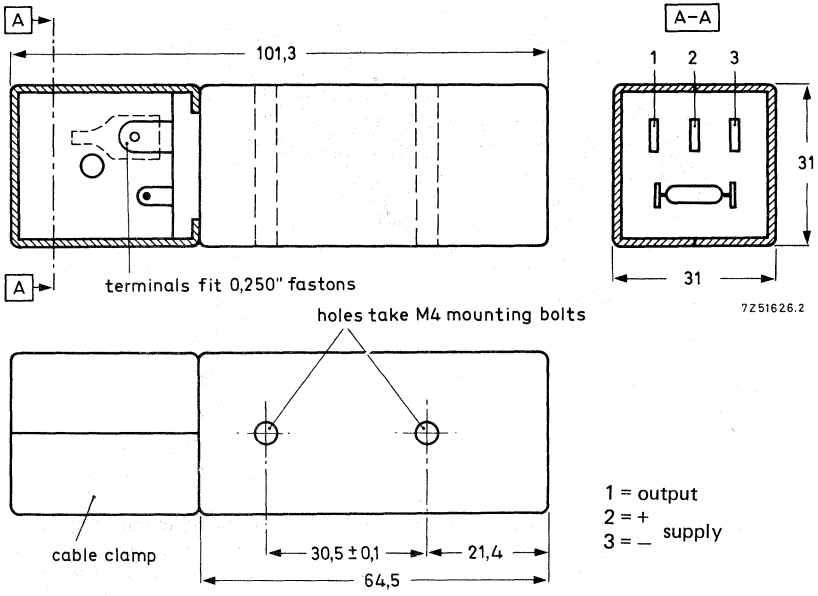
The unit contains an oscillator which is link coupled to a detector. The detector is followed by an amplifier. The oscillator coils and the coupling link are placed in a potcore half. In this way a well-defined field is set up in front of the open side of the potcore, located at the front of the PSD24. Bringing a piece of metal in this field decreases the oscillator output, and subsequently the output of the amplifier, due to the loading effect of the eddy current losses in the metal. When no piece of metal is near, the output voltage of the unit is maximum 300 mV (LOW). It will increase in proportion to the reduction of the oscillator output, resulting from a metal object coming nearer. When the piece of metal is close to the unit, the output voltage will be equal to the supply voltage (HIGH). The complete circuit is epoxy encapsulated in a polycarbonate housing. The mass is approximately 120 g. The unit may be mounted in any position. Two mounting holes allow the use of 4 mm bolts.

Connection can be made by 0,250" Fastons or by soldering. A cable clamp consisting of two equal caps is supplied with each PSD24. This clamp permits either end or top entrance of a 3-core cable of 7 mm diameter.



Drawing symbol

Dimensions in mm



Note

The resistor between the two 0,110" Fastons is an adjustment resistor for the oscillator loop gain; it should not be changed.

TECHNICAL PERFORMANCE

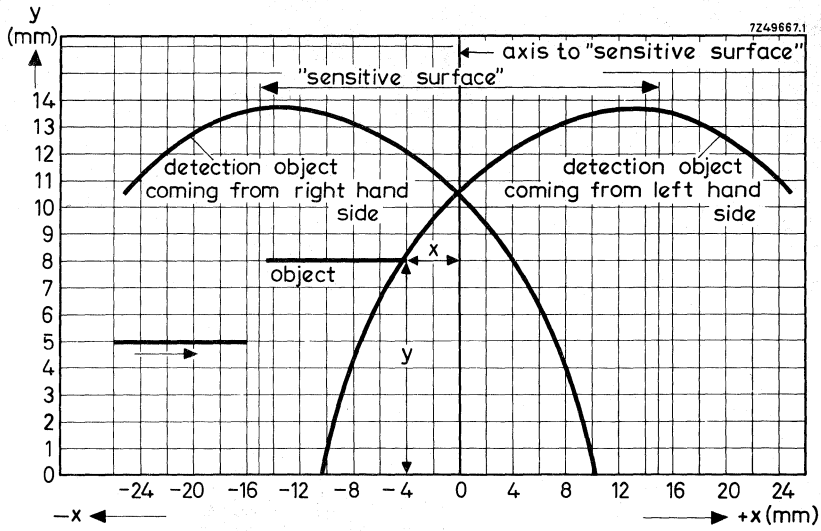
Supply voltage, V_S (d.c.)	24 V ± 25%
Consumed current	max 24 mA
Output voltage,	
no object being detected	max 300 mV
object being detected	$\leqslant V_S$
Output impedance	
no object being detected	400 Ω
object being detected	8 kΩ
Hysteresis	0 mm
Output current	
no object being detected	−max 8 mA
object being detected	3 mA
Maximum detection frequency	
mark to space ratio 1 : 1	1 kHz
Noise (over supply lines)	< 10 mV
Ambient temperature range	
operating	−25 to +85 °C
storage	−40 to +85 °C

APPLICATION INFORMATION (typical values)

Detection graphs

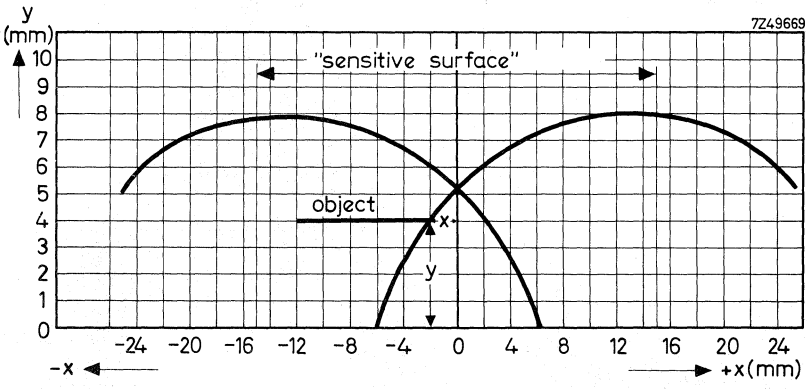
Detection of a rectangular mild steel reference object, 50 x 25 x 1 mm

Sensitive surface	surface of 31 x 31 mm at the opposite end of the PSD24 to the terminals
Axis	line perpendicular to the centre of the sensitive surface
Operating point	point at which the open circuit output voltage of the PSD24 is switched to V_S (moment of detection)
Operating distance	distance of the leading edge of the reference object to the axis at the operating point (x-operating distance)
Detection range	distance of the reference object to the sensitive surface (y-operating distance)



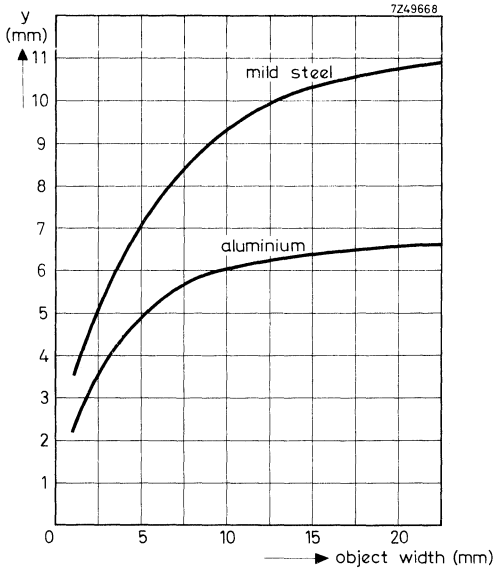
From the graph it can be seen that the object is detected before the axis is reached if it passes at a distance of < 10 mm from the sensitive surface. If it passes at a distance of e.g. 13,5 mm, the object is detected after the axis has been passed.

Detection of a rectangular aluminium reference object, 50 x 25 x 1 mm



Detection of rectangular mild steel and aluminium reference objects (50 x 1 mm) with different widths.

Object approaches the centre of the sensitive surface perpendicularly from in front.



Notes

The detection graphs may differ slightly from unit to unit.

Quite small objects can be detected when brought close to the sensitive surface. Thickness is relatively unimportant as eddy currents occur in penetration layer only.

The unit is sensitive to small movements and vibrations of the object when the output voltage is at an intermediate level.

Influence of supply voltage variations

A supply voltage variation of ±25% produces a change of ±0,1 mm in y-operating distance, at 10 mm from the sensitive surface.

Influence of temperature

With the reference object at a y-operating distance of 10 mm (at −25 °C) a change in temperature of both PSD24 and object will cause the y-operating distance to change less than 2 mm over the range from −25° to +85 °C.

Direction of approach

As the exterior field is radially symmetrical the path along which the detection position is reached is immaterial.

Distance from metallic surroundings

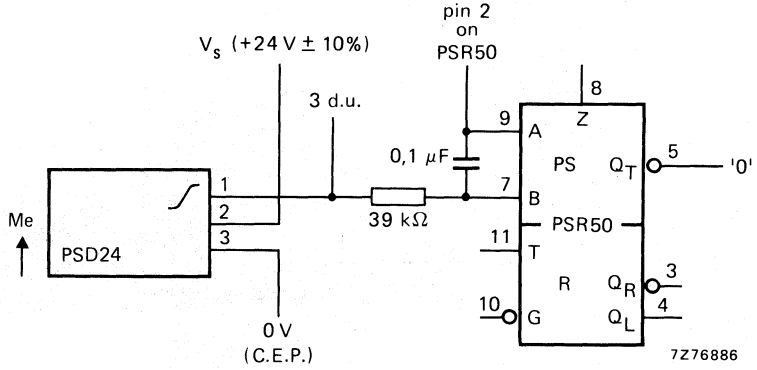
Clearance from metallic surrounding: 30 mm (this applies for sensitive front part of unit).

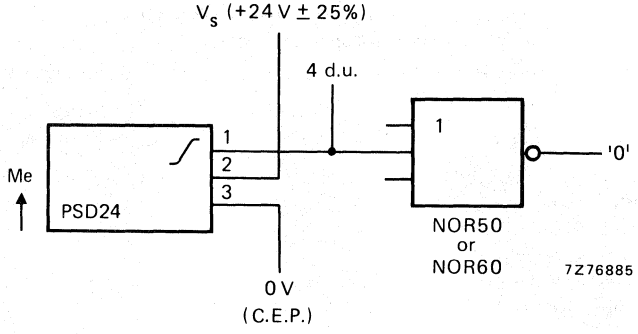
Spacing required between two detector axes with sensitive surface in the same plane: 60 mm.

Spacing required between two reference objects to give discrete detection: 50 mm. (This property can be put to use in feeder systems, a gap being used to initiate part supply restart.)

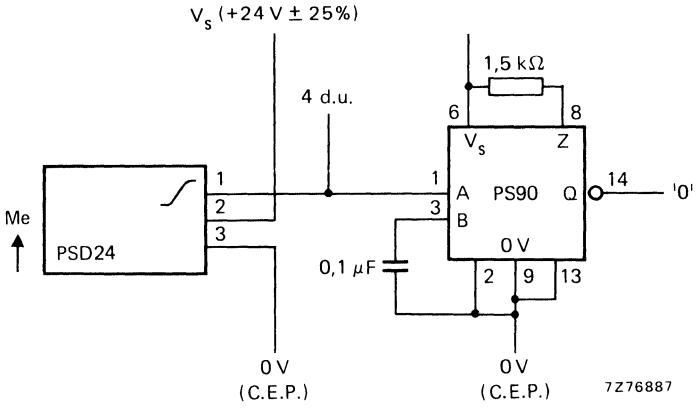
APPLICATION SUGGESTIONS *

PSD24 in conjunction with a PSR50, a NOR50 or NOR 60 and a PS90 respectively. Outputs are shown for object being detected. C.E.P. = central earth point.





* With long cables between PSD24 and subsequent electronics RC decoupling of interference can be employed.


V_S (+24 V ± 25%)
4 d.u.
1,5 kΩ
6
8
V_S
Z
1
2
3
Me
PSD24
1
A
B
PS90
Q
14
'0'
3
0 V
0,1 μF
2
9
13
0 V
(C.E.P.)
0 V
(C.E.P.)
7Z76887

HYBRID INTEGRATED CIRCUITS

HYBRID INTEGRATED CIRCUITS FOR INDUCTIVE PROXIMITY DETECTORS

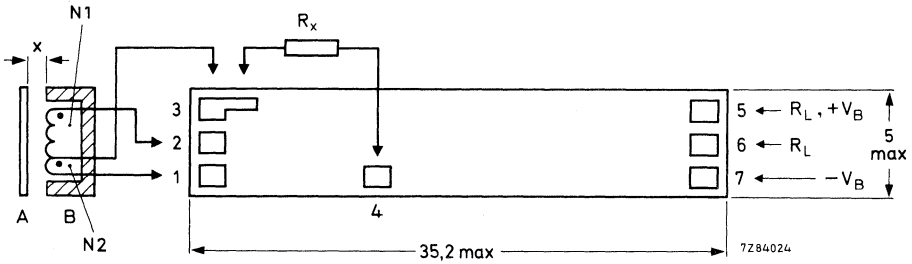
Hybrid integrated circuits intended for inductive proximity detectors in tubular construction, especially the M8 hollow stud. The OM286 is for positive and the OM287 for negative supply voltage. The circuit consists of an oscillator, a rectifier stage, a level switch and an output stage, which is suitable, e.g. for driving the coil of an electromagnetic relay. The output transistor is protected against transients from the inductive load by a voltage regulator diode. The circuit is protected against false polarity connection of the supply voltage. The device is a thick-film circuit deposited on a ceramic substrate. It may be potted, together with the oscillator coil and a resistor (R_x), in a non-magnetic tube.

QUICK REFERENCE DATA

D.C. supply voltage range	V_B	4,5 to 30	V
Output current at $V_B > 24$ V	I_O	max. 250	mA
Switching distance; depends on R_x and oscillator coil	x	typ. 1 to 5	mm
Hysteresis in switching distance	Δx	3 to 10	%
Switching frequency	f	< 5	kHz
Operating ambient temperature range	T_{amb}	−40 to + 85	°C*

MECHANICAL DATA

Dimensions in mm



A = metal actuator
B = open potcore or potcore half with coil

Fig. 1 Mechanical outline and connections. Note that the supply polarities to points 5 and 7 are given for the OM286; for OM287 the polarities are, point 5 $-V_B$ and point 7 $+V_B$. x is the switching distance. The maximum height of the circuits including the substrate thickness is 1,7 mm.

* The tube potting material and connection material are the main limiting factors for the operating ambient temperature range of the complete module.

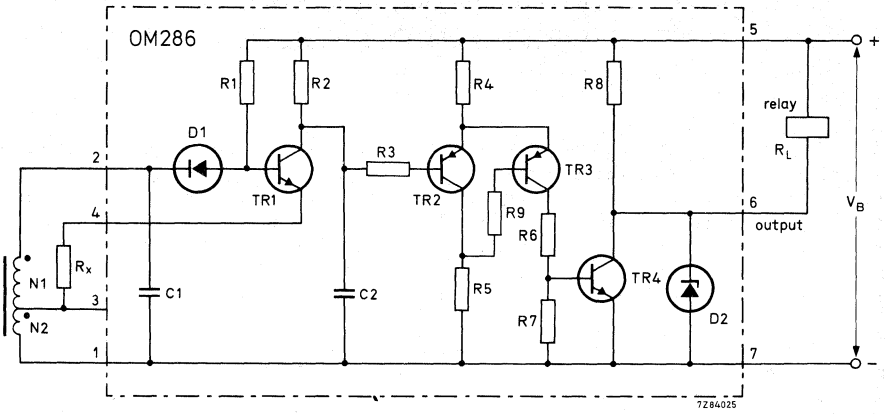


Fig. 2 Circuit diagram of OM286.

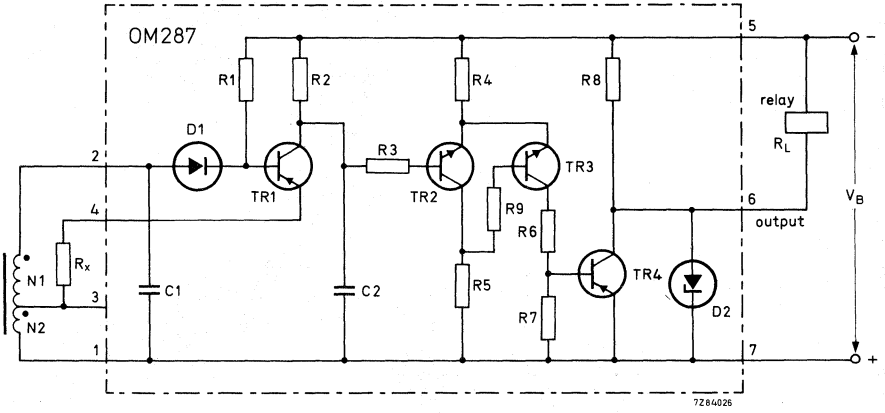


Fig. 3 Circuit diagram of OM287.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

D.C. supply voltage	V_B	max.	30 V
Output current	I_O	max.	250 mA
Storage temperature range	T_{stg}	−40 to + 125	°C
Operating ambient temperature range	T_{amb}	−40 to + 85	°C

CHARACTERISTICS

Conditions (unless otherwise specified)

D.C. supply voltage	V_B	4,5 to 30	V
Output current	see Fig. 4		
External resistance of oscillator	R_X	see switching distance below	
Operating ambient temperature range (potted)	T_{amb}	−25 to + 65	°C

Performance

Supply current (output current not included) V_B = 24 V	I_B	typ.	7 mA
Output voltage low (attenuated)			
V_B = 24 V; R_L = 120 Ω	V_{OL}	<	1 V
V_B = 5 V; R_L = 500 Ω	V_{OL}	<	0,25 V
Output voltage high (non-attenuated)	V_{OH}	≈	V_B

Switching distance *

type	oscillator coil number of turns N1	N2	average switching distance x (mm) at R_X (Ω) 200	250	300	recommended potcore	oscillator frequency kHz
M8	32	16	1	1,5	–	ϕ 5,8 mm (Neosid)	≈ 800
M12	40	10	2	3	–	P9-3B7/3H1	≈ 600
M18	46	4	3	4	5	P14-3B7/3H1	≈ 600

Hysteresis in switching distance	Δx		3 to 10 %
Switching frequency	f	<	5 kHz

* The switching distance x depends on the oscillator coil, the material of the metal actuator and R_X. For measuring purposes a square steel sheet with dimensions such that a circle with the diameter of the core can be inscribed, and 1 mm thickness can be used. R_X must not be chosen outside the range 180 to 400 Ω. Influence of supply voltage: 1 μm/V.
Temperature coefficient:
M8: 0,2 %/°C
M12: 0,17%/°C
M18: 0,1 %/°C.

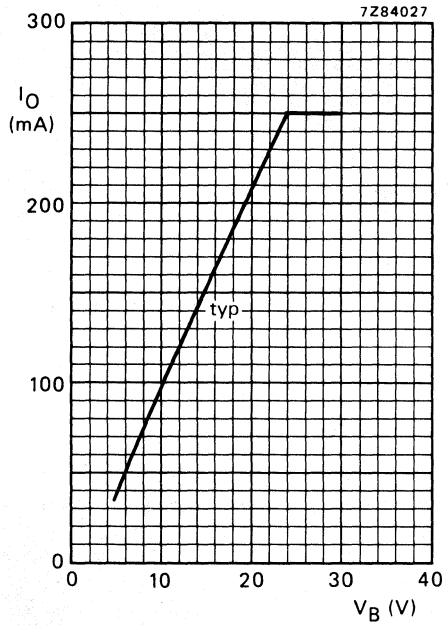
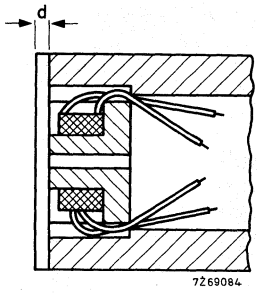


Fig. 4 Maximum allowable output current as a function of supply voltage.

MOUNTING RECOMMENDATIONS



If a protective plastic cap is incorporated, it should be as thin as possible, because its thickness d forms part of the switching distance x.

The brass stud wall should not extend beyond the potcore. If no brass tube is used, the switching distances increase by at least 25%. The exact value with its spread is determined by a number of variables, e.g.

- value of the adjustment resistor R_X
- the oscillator coil
- hysteresis
- the metal of the actuator
- the stud housing (if any).

Fig. 5 Insertion of potcore in brass tube.

Soldering recommendations

Use normal 60/40 solder with 2 to 4% silver; use solder-iron with a fine point; soldering time as short as possible.

Potting recommendations

First cover the hybrid IC with about 0,5 mm of DC3140 (Dow Corning), let it harden and then, when the parts are inserted in the tube, fill up the tube with Stycast 2850 (Emerson and Cuming).

Heat transfer

The module may be used at maximum voltage/current conditions at a substrate temperature of 85 °C. When potted the heat transfer improves slightly.

HYBRID INTEGRATED CIRCUITS FOR INDUCTIVE PROXIMITY DETECTORS

GENERAL DESCRIPTION

Hybrid integrated circuits intended for inductive proximity detectors in tubular construction, especially the M8 hollow stud. The OM386 is for positive supply voltage and the OM387 for negative. The circuit consists of an oscillator, a rectifier stage, a Schmitt-trigger, an output stage and a protection circuit.

Features

- Output current 400 mA at V_B = 10 to 30 V
- Protection against short circuit and overload
- Protection of output transistor against transients by a voltage regulator diode
- Protection against false polarity of the three connection leads
- Choice of two methods to adjust the switching distance (trimming a resistor integrated on the substrate or mounting a discrete resistor)
- Possibility of connecting a LED for function control

The device is a thick-film circuit deposited on a ceramic substrate. It may be potted, together with the oscillator coil in a non-magnetic tube.

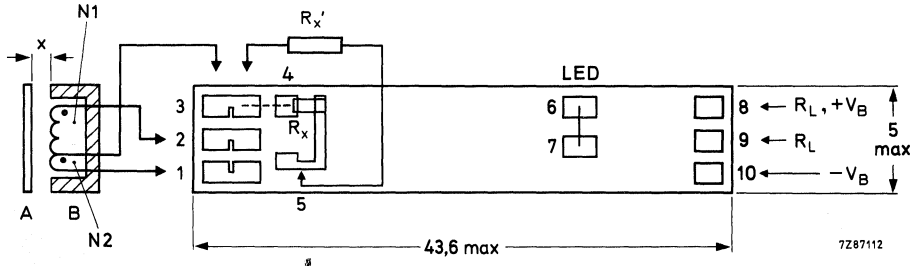
QUICK REFERENCE DATA

D.C. supply voltage range	V_B		10 to 30	V
Output current at V_B = 10 to 30 V	I_O	max.	400	mA
Switching distance; depends on R_X and oscillator coil	x	typ.	1 to 5	mm
Hysteresis in switching distance	Δx		3 to 10	%
Switching frequency	f	<	5	kHz
Operating ambient temperature range	T_{amb}		−40 to +75	°C*

* The tube potting material and connection material are the main limiting factors for the operating ambient temperature range of the complete module.

MECHANICAL DATA

Dimensions in mm



A = metal actuator; B = open potcore or potcore half with coil.

Fig. 1 Mechanical outline and connections. Note that the supply polarities to points 8 and 10 are given for the OM386; for OM387 the polarities are, point 8 $-V_B$ and point 10 $+V_B$; x is the switching distance. The maximum height of the circuits including the substrate thickness is 1,7 mm.

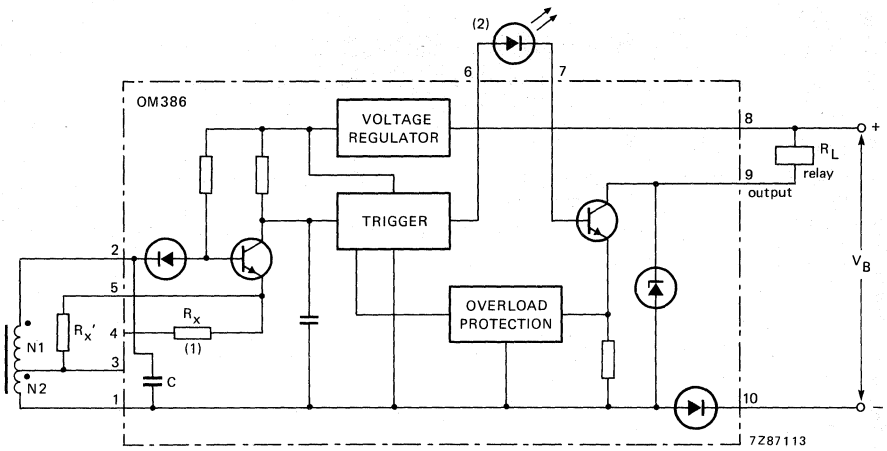


Fig. 2 Circuit diagram of OM386.

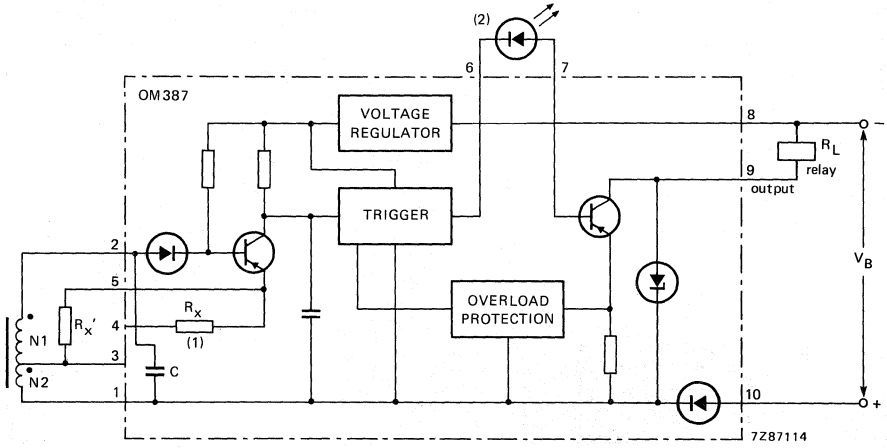


Fig. 3 Circuit diagram of OM387.

(1) R_X is integrated on the substrate and suitable for trimming (laser or sandblasting). To use integrated resistor R_X it is necessary to connect point 3 to 4.

(2) If a LED is to be connected, the coupling between points 6 and 7 should be removed.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

D.C. supply voltage	V_B	max.	30 V
Output current	I_O	max.	400 mA
Storage temperature range	T_{stg}	−40 to	+125 °C
Operating ambient temperature range	T_{amb}	−40 to	+ 75 °C

CHARACTERISTICS

Conditions (unless otherwise specified)

D.C. supply voltage	V_B	10 to 30 V
External resistance of oscillator	R_x	see switching distance below
Operating tube temperature range (potted)	T_{tube}	−25 to +65 °C

Performance

Supply current (output current not included)	I_B	typ.	6 mA
Output voltage low (attenuated) I_O = 400 mA	V_{OL}	<	2,2 V
Output voltage high (non-attenuated)	V_{OH}	≈	V_B

Switching distance*

type	oscillator coil number of turns N1	N2	average switching distance x (mm) at R_x or R_x' (Ω) 200	250	300	recommended potcore	oscillator frequency kHz
M8	32	16	1	1,5	–	ϕ 5,8 mm (Neosid)	≈ 800
M12	40	10	2	3	–	P9-3B7/3H1	≈ 600
M18	46	4	3	4	5	P14-3B7/3H1	≈ 600

Hysteresis in switching distance	Δx		3 to 10 %
Switching frequency	f	<	5 kHz

* The switching distance x depends on the oscillator coil, the material of the metal actuator and R_x or R_x'. For measuring purposes a square steel sheet with dimensions such that a circle with the diameter of the core can be inscribed, and 1 mm thickness can be used. R_x or R_x' must not be chosen outside the range 180 to 400 Ω.

MOUNTING RECOMMENDATIONS

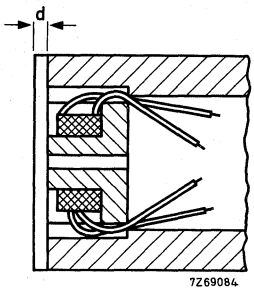


Fig. 4 Insertion of potcore in brass tube.

If a protective plastic cap is incorporated, it should be as thin as possible, because its thickness d forms part of the switching distance x.

The brass stud wall should not extend beyond the potcore. If no brass tube is used, the switching distances increase by at least 25%. The exact value with its spread is determined by a number of variables, e.g.

- value of the adjustment resistor R_X or R_X'
- the oscillator coil
- hysteresis
- the metal of the actuator
- the stud housing (if any).

Soldering recommendations

Use normal 60/40 solder with 2 to 4% silver; use solder-iron with a fine point; soldering time as short as possible.

Potting recommendations

First cover the hybrid IC with about 0,5 mm of DC3140 (Dow Corning), let it harden and then, when the parts are inserted in the tube, fill up the tube with Stycast 2850 (Emerson and Cuming).

Heat transfer

The module may be used at voltage/current conditions equivalent to a substrate temperature of 90 °C. When potted the heat transfer improves slightly, especially in a metal tube.

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PC20 MODULES

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PLC MODULES

PC20 MODULES

HNIL FZ/30-SERIES

NORBITS 60-SERIES, 61-SERIES, 90-SERIES

INPUT DEVICES

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