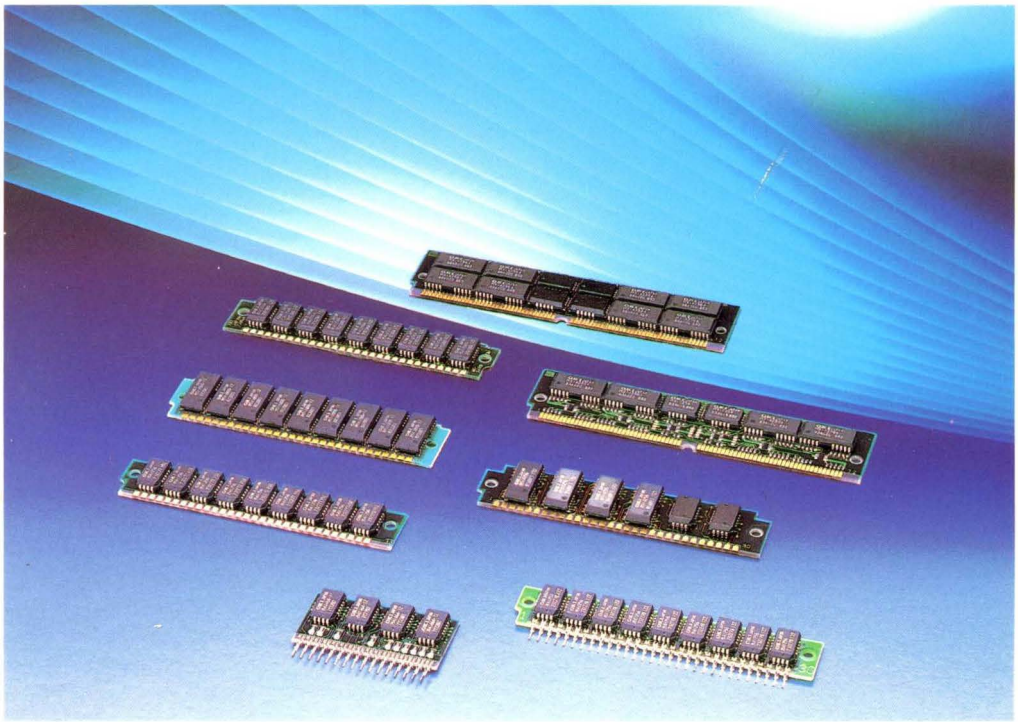
DATA BOOK

OKI

MEMORY MODULE



OKI Semiconductor

FIRST EDITION
ISSUE DATE: JUL., 1990

OKI MEMORY MODULE DATA BOOK ('90-'91)

MEMORY MODULE DATABOOK 1990/1991

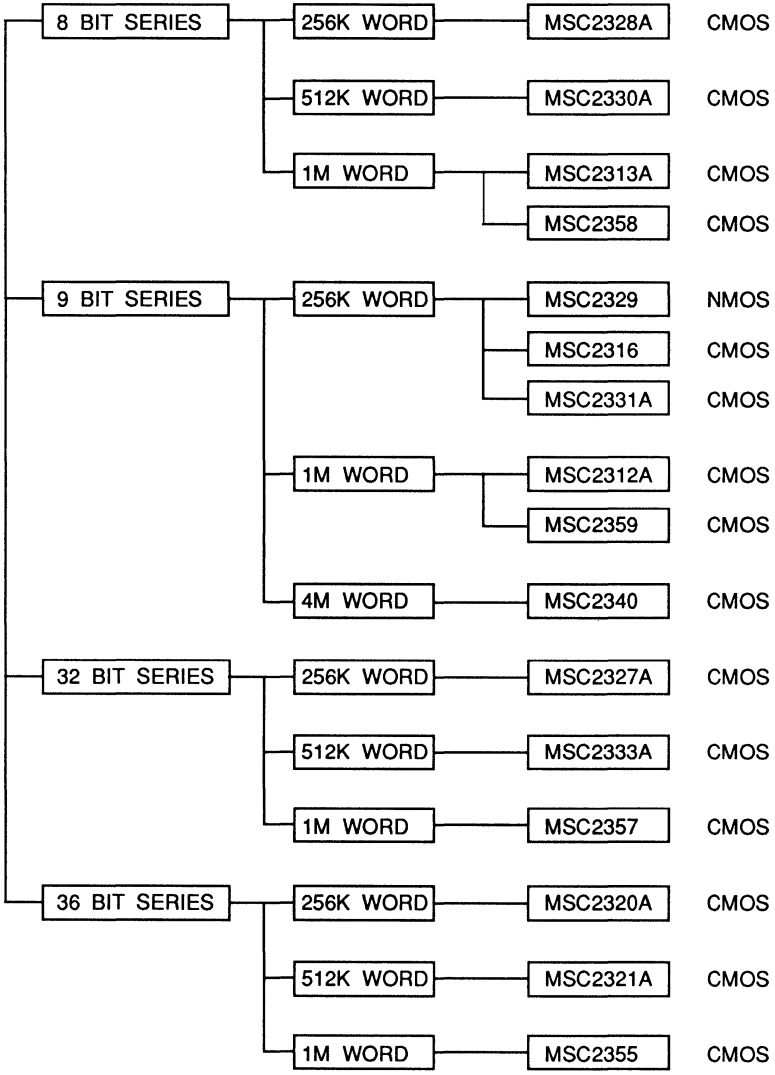
CONTENTS

INTRODUCTION

1

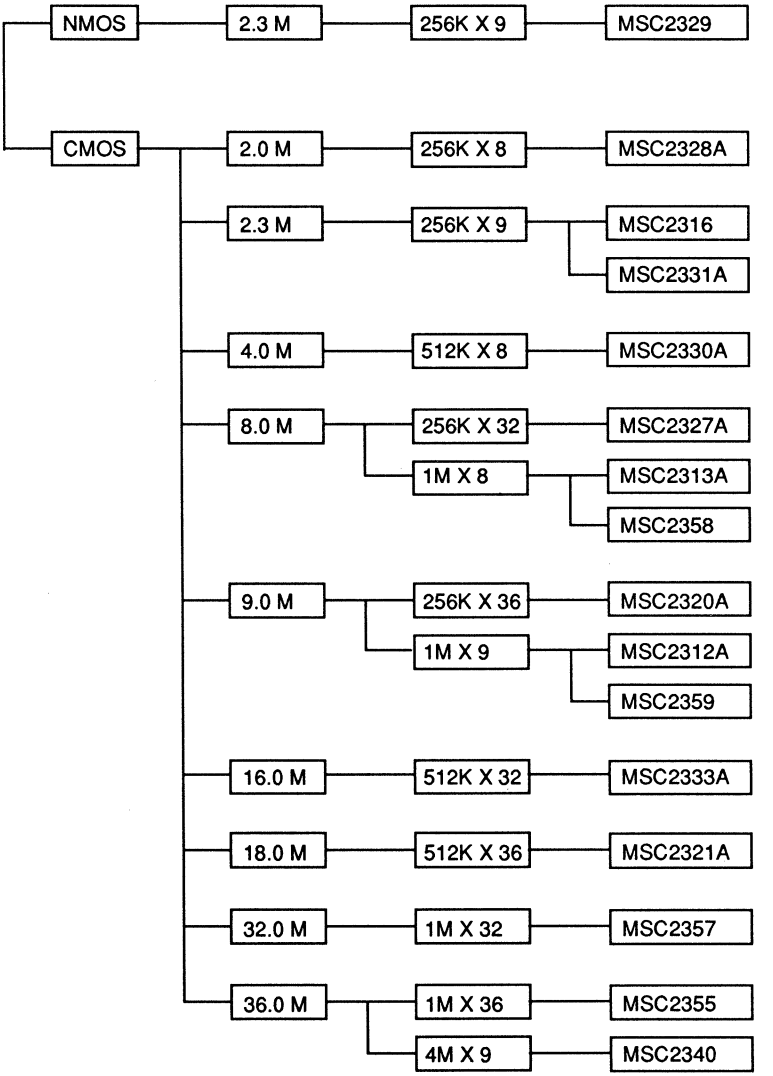
1

PRODUCT LINE-UP (1)



1

PRODUCT LINE-UP (2)



TYPICAL CHARACTERISTICS

Model Name	Memory Capacity (bit)	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mW) Operating/ Standby	Power Supply Voltage (V)
MSC2328A-80 YS2/KS2	2 M	Socket Insertable Module	262,144x8	30	80	160	825/11	+5
MSC2328A-10 YS2/KS2					100	190	715/11	
MSC2330A-80 YS4/KS4	4 M	Socket Insertable Module	524,288x8	30	80	160	847/22	+5
MSC2330A-10 YS4/KS4					100	190	737/22	
MSC2313A-70 YS8/KS8	8 M	Socket Insertable Module	1,048,576x8	30	70	140	3740/44	+5
MSC2313A-80 YS8/KS8					80	160	3300/44	
MSC2313A-10 YS8/KS8					100	190	2860/44	
MSC2358-80 KS2	8M	Socket Insertable Module	1,048,576x8	30	80	160	990/11	+5
MSC2358-10 KS2					100	190	880/11	
MSC2329-10 YS3/KS3	2.3 M	Socket Insertable Module	262,144x9	30	100	200	1155/50	+5
MSC2329-12 YS3/KS3					120	220	1073/50	
MSC2316-80 YS9	2.3 M	Socket Insertable Module	262,144x9	30	80	160	2970/124	+5
MSC2316-10 YS9					100	190	2475/124	
MSC2331A-80 YS3/KS3	2.3 M	Socket Insertable Module	262,144x9	30	80	160	1155/25	+5
MSC2331A-10 YS3/KS3					100	190	990/25	

1

TYPICAL CHARACTERISTICS (cont'd)

Model Name	Memory Capacity (bit)	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mW) Operating/ Standby	Power Supply Voltage (V)
MSC2312A-70 YS9/KS9	9 M	Socket Insertable Module	1,048,576x9	30	70	140	4208/50	+5
MSC2312A-80 YS9/KS9					80	160	3713/50	
MSC2312A-10 YS9/KS9					100	190	3218/50	
MSC2359-80 YS3	9 M	Socket Insertable Module	1,048,576x9	30	80	160	1403/17	+5
MSC2359-10 YS3					100	190	1238/17	
MSC2340-80 YS9/KS9	36 M	Socket Insertable Module	4,194,304x9	30	80	160	4455/50	+5
MSC2340-10 YS9/KS9					100	190	3960/50	
MSC2327A-80 YS8	8 M	Socket Insertable Module	262,144x32	72	80	160	3150/42	+5
MSC2327A-10 YS8					100	190	2730/42	
MSC2333A-80 YS16	16 M	Socket Insertable Module	524,288x32	72	80	160	3234/84	+5
MSC2333A-10 YS16					100	190	2814/84	
MSC2357-80 YS8	32 M	Socket Insertable Module	1,048,576x32	72	80	160	3780/42	+5
MSC2357-10 YS8					100	190	3360/42	
MSC2320A-80 YS9	8 M	Socket Insertable Module	262,144x36	72	80	160	4410/95	+5
MSC2320A-10 YS9					100	190	3780/95	

TYPICAL CHARACTERISTICS (cont'd)

Model Name	Memory Capacity (bit)	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mW) Operating/ Standby	Power Supply Voltage (V)
MSC2321A-80 YS18	16 M	Socket Insertable Module	524,288x36	72	80	160	4568/189	+5
MSC2321A-10 YS18					100	190	3938/189	
MSC2355-80 YS12	36 M	Socket Insertable Module	1,048,576x36	72	80	160	5355/63	+5
MSC2355-10 YS12					100	190	4725/63	

TERMINOLOGY AND SYMBOLS

1. PIN TERMINOLOGY

Term	Dynamic RAM
Power Supply Voltage	V_{CC}
Address Input Pin	A0 ~ A10
Data Input Pin	D_{IN}, D8
Data Output Pin	D_{OUT}, Q8
Data Input/Output Pin	DQ0 ~ DQ35
Output Enable Pin	$\overline{OE}$
Write Enable Pin	$\overline{WE}$
Row Address Strobe Pin	$\overline{RAS}$, $\overline{RAS0}$ ~ $\overline{RAS3}$
Column Address Strobe Pin	$\overline{CAS}$, $\overline{CAS0}$ ~ $\overline{CAS3}$
Ground Pin	V_{SS}

2. ABSOLUTE MAXIMUM RATINGS

Term	Dynamic RAM
Power Supply Voltage	V_{CC}, V_{SS}
Terminal Voltage	V_T
Input Voltage	V_{IN}
Output Voltage	V_{OUT}
Output Shoft Circuit Current	I_{OS}
Power Dissipation	P_D
Operating Temperature	Topr
Storage Temperature	Tstg

3. RECOMMENDED OPERATING CONDITIONS

Term	Dynamic RAM
Power Supply Voltage	V_{CC}, V_{SS}
"H" Input Voltage	V_{IH}
"L" Input Voltage	V_{IL}
Operating Temperature	Topr

4. DC CHARACTERISTICS

Term	Dynamic RAM
"H" Output Voltage	V_{OH}
"L" Output Voltage	V_{OL}
"H" Output Current	I_{OH}
"L" Output Current	I_{OL}
Input Leakage Current	I_{LI}
Output Leakage Current	I_{LO}
Power Supply Current	I_{CC1}, I_{CC5} I_{CC2}, I_{CC6} I_{CC3}, I_{CC7} I_{CC4}

5. AC CHARACTERISTICS

(1) Read Cycle

Term	Dynamic RAM
Read Cycle Time	t_{RC}
Address Access Time	t_{AA}
Output Enable Access Time	t_{OEA}
Output Disable Time	t_{OFF}, t_{OEZ}
Address Set-up Time	t_{ASR}, t_{ASC}
Address Hold Time	t_{RAH}, t_{CAH}
Clock Pulse Width	t_{RAS}, t_{CAS}, t_{WP}
Clock Delay Time	t_{RCD}, t_{RAD}

(2) Write Cycle

Term	Dynamic RAM
Write Cycle Time	t_{RC}
Address Set-up Time	t_{ASR}, t_{ASC}
Write Pulse Width	t_{WP}
Data Set-up Time	t_{DS}
Data Hold Time	t_{DH}
Output Off-time	t_{OFF}
Address Hold Time	t_{RAH}, t_{CAH}

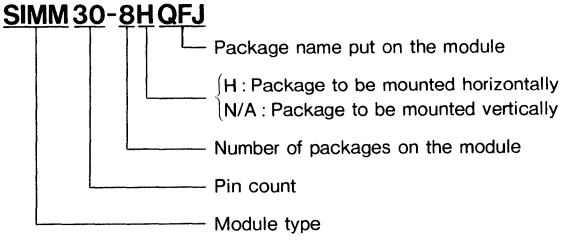
PACKAGING

PACKAGING

PRODUCT NAME	PACKAGE CODE
MSC2328A-xxYS2	SIMM30-2HSOJ
MSC2328A-xxKS2	SIMP 30 - 2HSOJ
MSC2330A-xxYS4	SIMM30-4HSOJ
MSC2330A-xxKS4	SIMP 30 - 4HSOJ
MSC2313A-xxYS8	SIMM30-8SOJ
MSC2313A-xxKS8	SIMP 30 - 8SOJ
MSC2358-xxKS2	SIMP 30 - 2HSOJ
MSC2329-xxYS3	SIMM30-2HSOJ 1HQFJ
MSC2329-xxKS3	SIMP 30 - 2HSOJ 1HQFJ
MSC2316-xxYS9	SIMM30-9QFJ
MSC2331A-xxYS3	SIMM30-2HSOJ 1HQFJ
MSC2331A-xxKS3	SIMP 30 - 2HSOJ 1HQFJ
MSC2312A-xxYS9	SIMM30-9SOJ
MSC2312A-xxKS9	SIMP 30 - 9SOJ
MSC2359-xxYS3	SIMM30-3HSOJ
MSC2340-xxYS9	SIMM30-9HSOJ
MSC2340-xxKS9	SIMP 30 - 9HSOJ
MSC2327A-xxYS8	SIMM72-8HSOJ -1
MSC2333A-xxYS16	SIMM72-16HSOJ
MSC2357-xxYS8	SIMM72-8HSOJ
MSC2320A-xxYS9	SIMM72-8HSOJ 4HQFJ
MSC2321A-xxYS18	SIMM72-16HSOJ 8HQFJ
MSC2355-xxYS12	SIMM72-12SOJ

(NOTE)

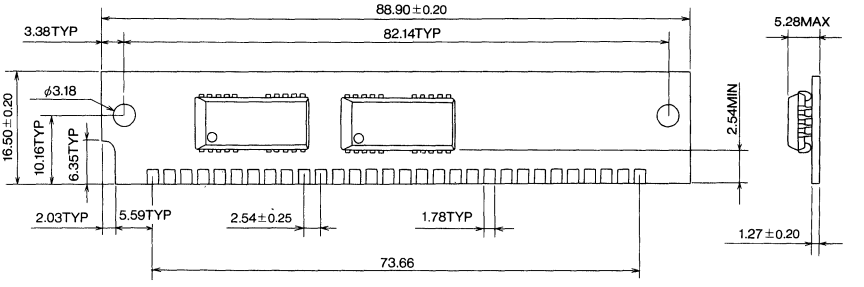
Typical Description of Package Code:



2

30PIN	SIMM30-2HSOJ

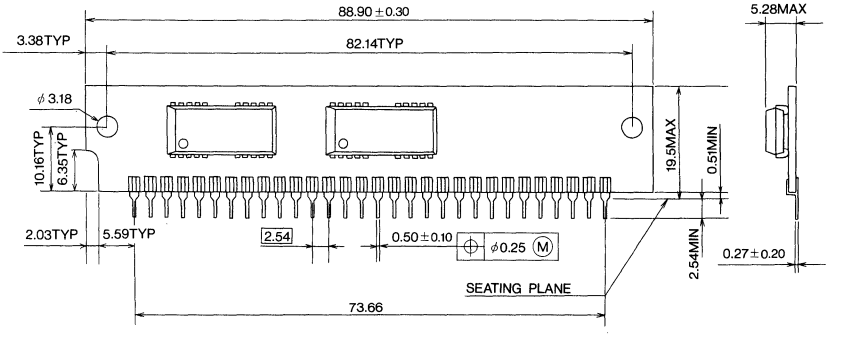
(UNIT : mm)



PRODUCT NAME
MSC2328A-xxYS2

30PIN	SIMP30-2HSOJ

(UNIT : mm)

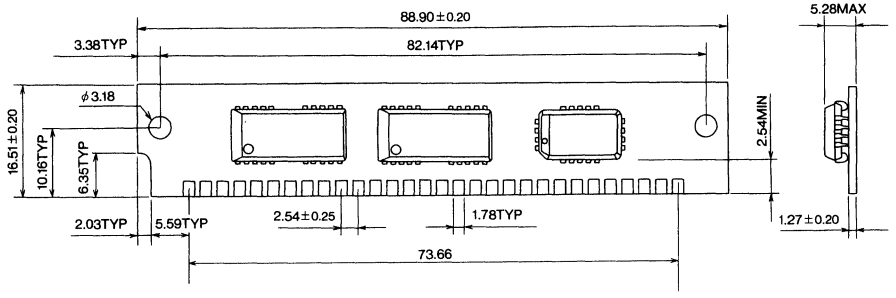


PRODUCT NAME
MSC2328A-xxKS2
MSC2358-xxKS2

2

30PIN	SIMM30-2HSOJ 1HQFJ

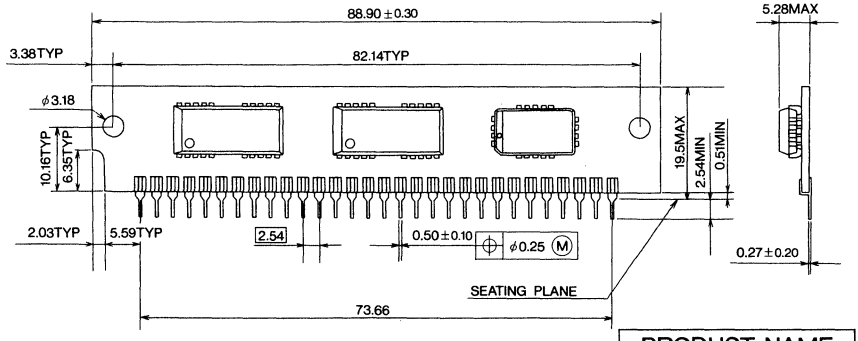
(UNIT : mm)



PRODUCT NAME
MSC2329-xxYS3
MSC2331A-xxYS3

30PIN	SIMP30-2HSOJ 1HQFJ

(UNIT : mm)

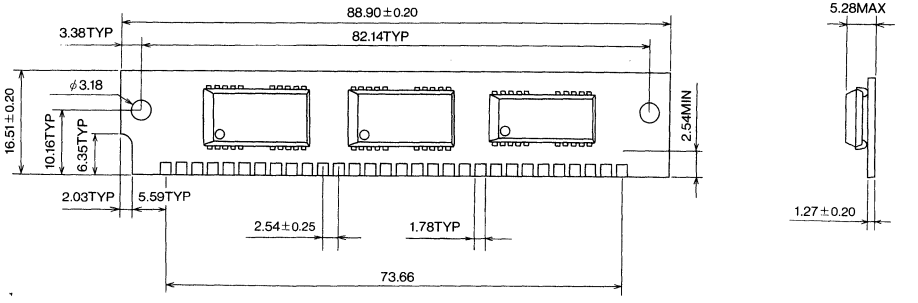


PRODUCT NAME
MSC2329-xxKS3
MSC2331A-xxKS3

2

30PIN	SIMM30-3HSOJ

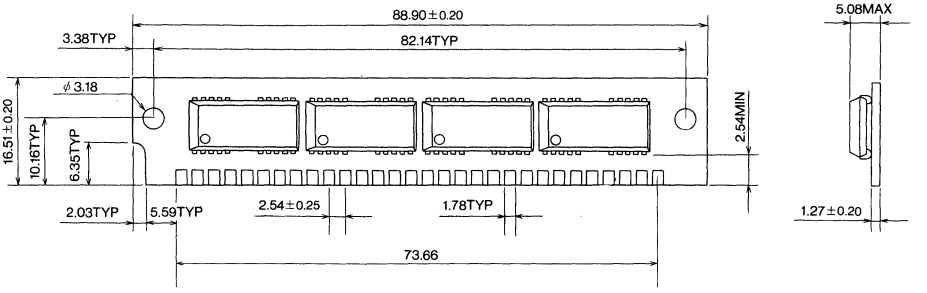
(UNIT : mm)



PRODUCT NAME
MSC2359-xxYS3

30PIN	SIMM30-4HSOJ

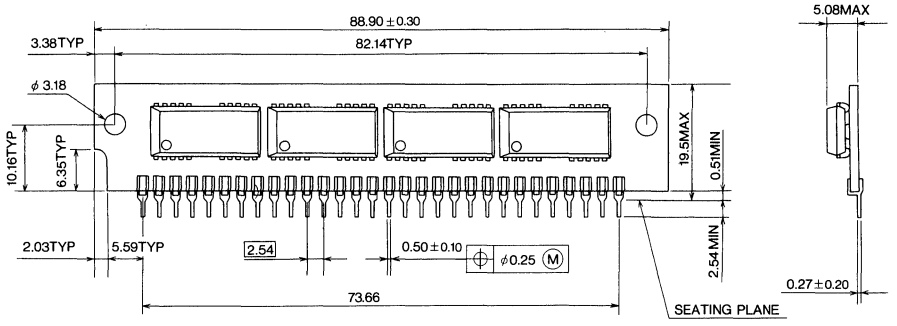
(UNIT : mm)



PRODUCT NAME
MSC2330A-xxYS4

30PIN	SIMP30-4HSOJ

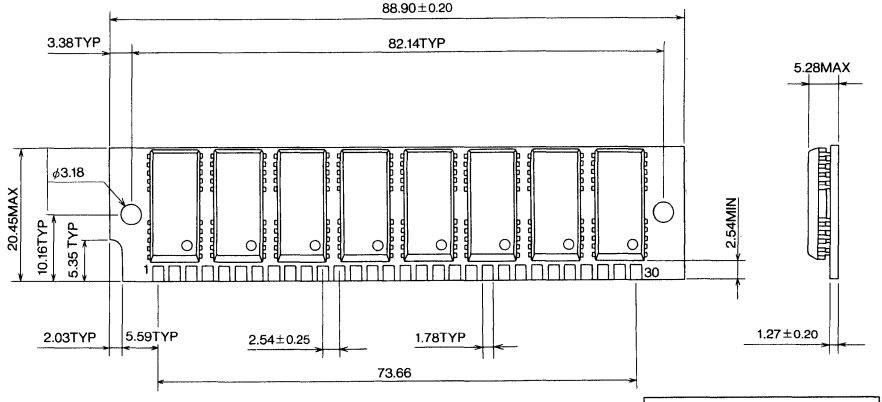
(UNIT : mm)



PRODUCT NAME
MSC2330A-xxKS4

30PIN	SIMM30-8SOJ

(UNIT : mm)

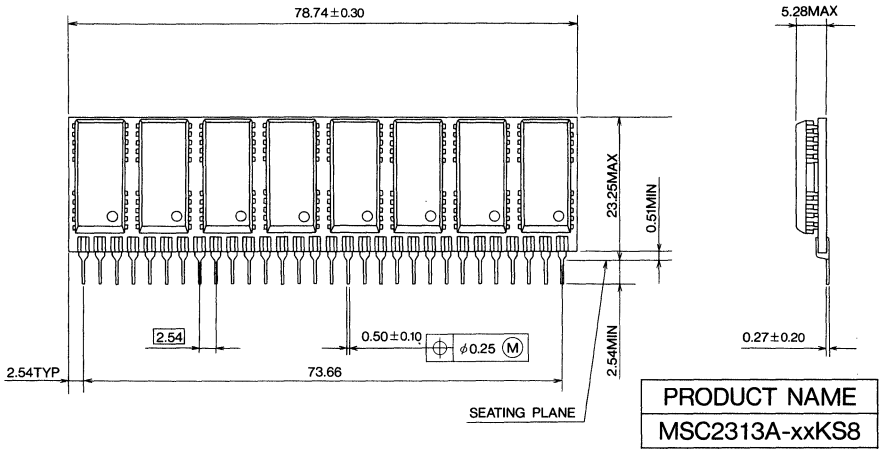


PRODUCT NAME
MSC2313A-xxYS8

2

30PIN	SIMP30-8SOJ

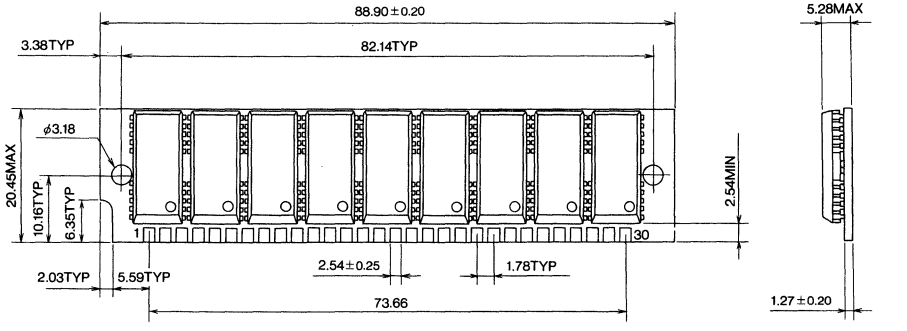
(UNIT : mm)



PRODUCT NAME
MSC2313A-xxKS8

30PIN	SIMM30-9SOJ

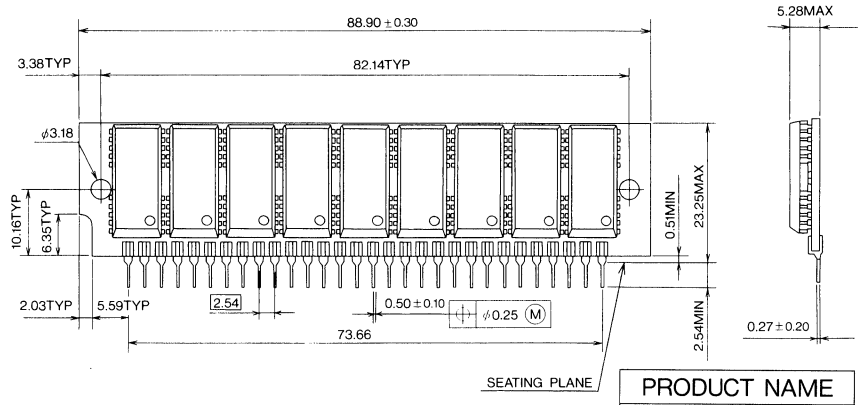
(UNIT : mm)



PRODUCT NAME
MSC2312A-xxYS9

30PIN	SIMP30-9SOJ

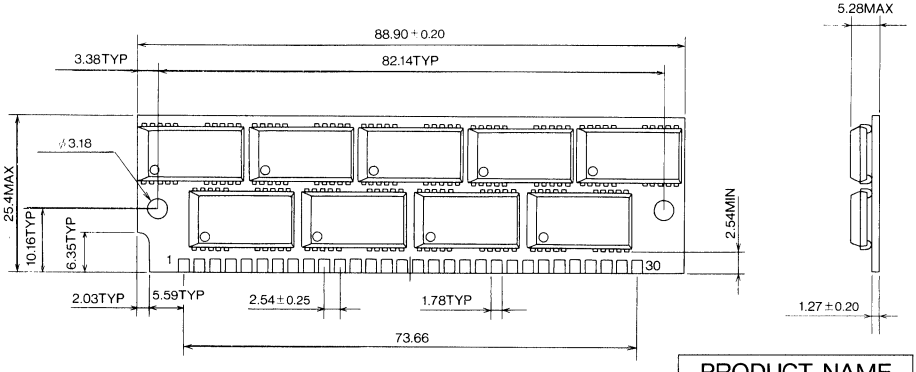
(UNIT : mm)



PRODUCT NAME
MSC2312A-xxKS9

30PIN	SIMM30-9HSOJ

(UNIT : mm)

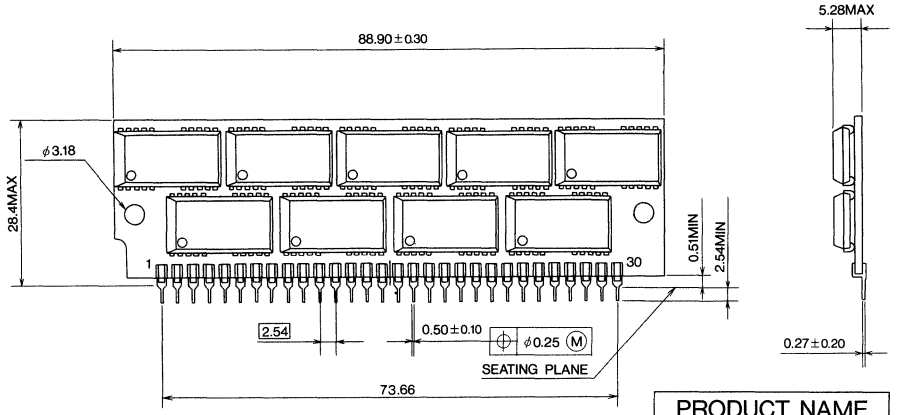


PRODUCT NAME
MSC2340-xxYS9

2

30PIN	SIMP30-9HSOJ

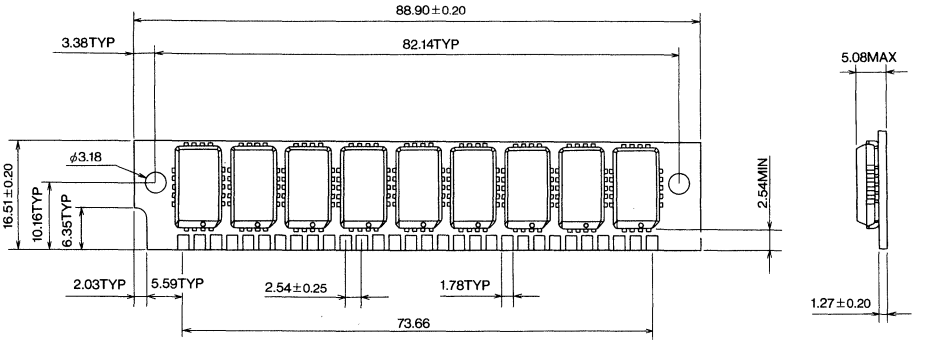
(UNIT : mm)



PRODUCT NAME
MSC2340-xxKS9

30PIN	SIMM30-9QFJ

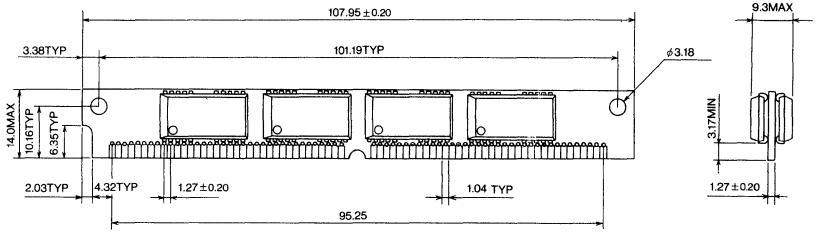
(UNIT : mm)



PRODUCT NAME
MSC2316-xxYS9

72PIN	SIMM72-8HSOJ

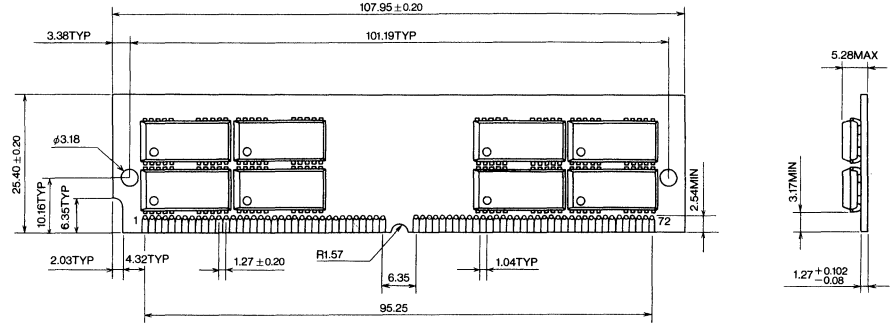
(UNIT : mm)



PRODUCT NAME
MSC2357-xxYS8

72PIN	SIMM72-8HSOJ-1

(UNIT : mm)

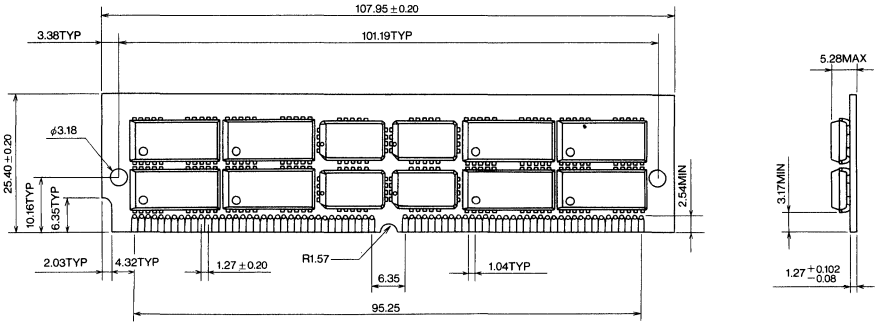


PRODUCT NAME
MSC2327A-xxYS8

2

72PIN	SIMM72-8HSOJ 4HQFJ

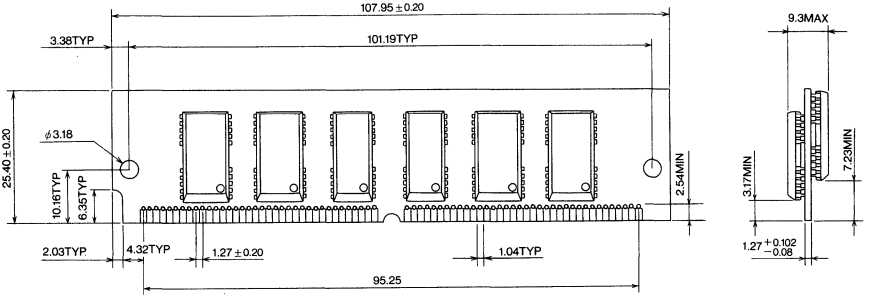
(UNIT : mm)



PRODUCT NAME
MSC2320A-xxYS9

72PIN	SIMM72-12SOJ

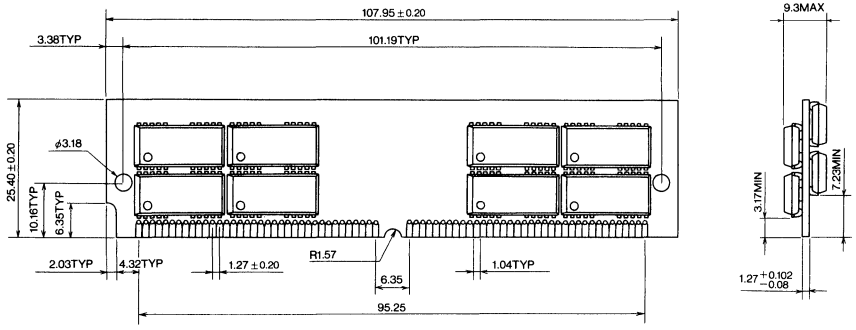
(UNIT : mm)



PRODUCT NAME
MSC2355-xxYS12

72PIN	SIMM72-16HSOJ

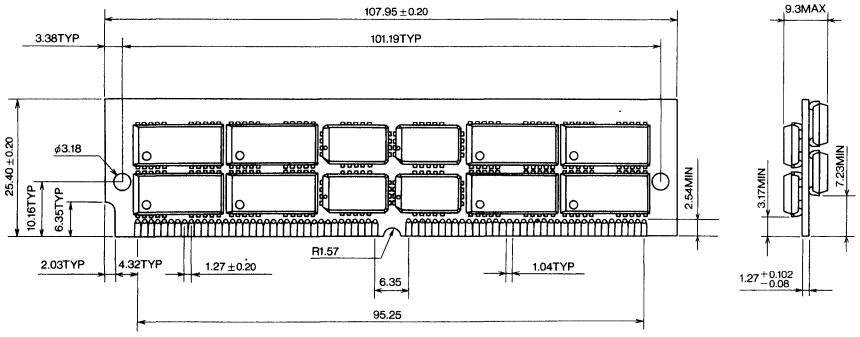
(UNIT : mm)



PRODUCT NAME
MSC2333A-xxYS16

72PIN	SIMM72-16HSOJ 8HQFJ

(UNIT : mm)



PRODUCT NAME
MSC2321A-xxYS18

RELIABILITY INFORMATION

RELIABILITY INFORMATION

1. INTRODUCTION

Semiconductor devices play a leading role in the explosive progress of semiconductor technology. They use some of the most advanced design and manufacturing technology developed to date. With greater integration, diversity and reliability, their applications have expanded enormously. Their use in large scale computers, control equipment, calculators, electronic games and in many other fields has increased at a fast rate.

A failure in electronic banking or telephone switching equipment, for example, could have far reaching effects and can cause incalculable losses. So, the demand, for stable high quality memory devices is strong.

We, at Oki are fully aware of this demand. So we have adopted a comprehensive quality assurance system based on the concept of consistency in development, manufacturing and sales.

With the increasing demand for improvement in function, capability and reliability, we will expand our efforts in the future. Our quality assurance system and the underlying concepts are outlined briefy below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

The quality assurance system employed by Oki can be divided into four major stages: device planning, developmental prototype, production prototype, and mass production. This system is outlined in the following block diagram (Fig. 1).

1) Device planning stage

To manufacture devices that meet market demands and satisfy customer needs, we carefully consider functional and failure rate requirements, utilization form, environment and other conditions. Once we determine the proper type, material and structure, we check the design and manufacturing techniques, and the line processing capacity. Then we prepare the development planning and time schedule.

2) Developmental prototype stage

We determine circuits, pattern design, process settings, assembly techniques and structural requirements during this stage. At the same time, we carry out actual prototype reliability testing.

Since device quality is largely determined during the designing stage, Oki pays careful attention to quality confirmation during this stage.

This is how we do it:

(1) After completion of circuit design (or pattern design), personnel from the design, process technology, production technology, installation technology and reliability departments get together for a thorough review to ensure design quality and to anticipate problems that may occur during mass production. Past experience and know-how guide these discussions.

(2) Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.

Note: TEG (Test Element Group) refers to the device group designed for stability evaluation of MOS transistors, diodes, resistors, capacitors and other circuit component element used in LSI memories.

(3) Prototypes are subjected to repeated reliability and other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Production prototype stage

During this stage, various tests check the reliability and other special features of the production prototype at the mass production factory level. After confirming the quality of a device, we prepare the various standards required for mass production, and then start production. Although reliability and other special tests performed on the production prototype are much the same as those performed on the developmental prototype, the personnel, facilities and production site differ for the two prototypes, necessitating repeated confirmation tests.

4) Mass production

During the mass production stage, careful management of purchased materials, parts and facilities used during the manufacturing process, measuring equipment, manufacturing conditions and environment is necessary to ensure device quality first stipulated during the designing stages. The manufacturing process (including inspection of the completed device) is followed by a lot guarantee inspection to check that the specified quality is maintained under conditions identical to those under which a customer would actually use the device. This lot guarantee inspection is performed in three different forms as shown below.

(1) Group A tests: appearance, labels, dimensions and electrical characteristics inspection

(2) Group B tests: check of durability under thermal and mechanical environmental stresses, and operating life characteristics

(3) Group C tests: performed periodically to check operational life, etc., on a long term basis.

Note: Like the reliability tests, the group B tests conform to the following standards.
MIL-STD-883B, JIS C 7022, EIAJ-IC-121

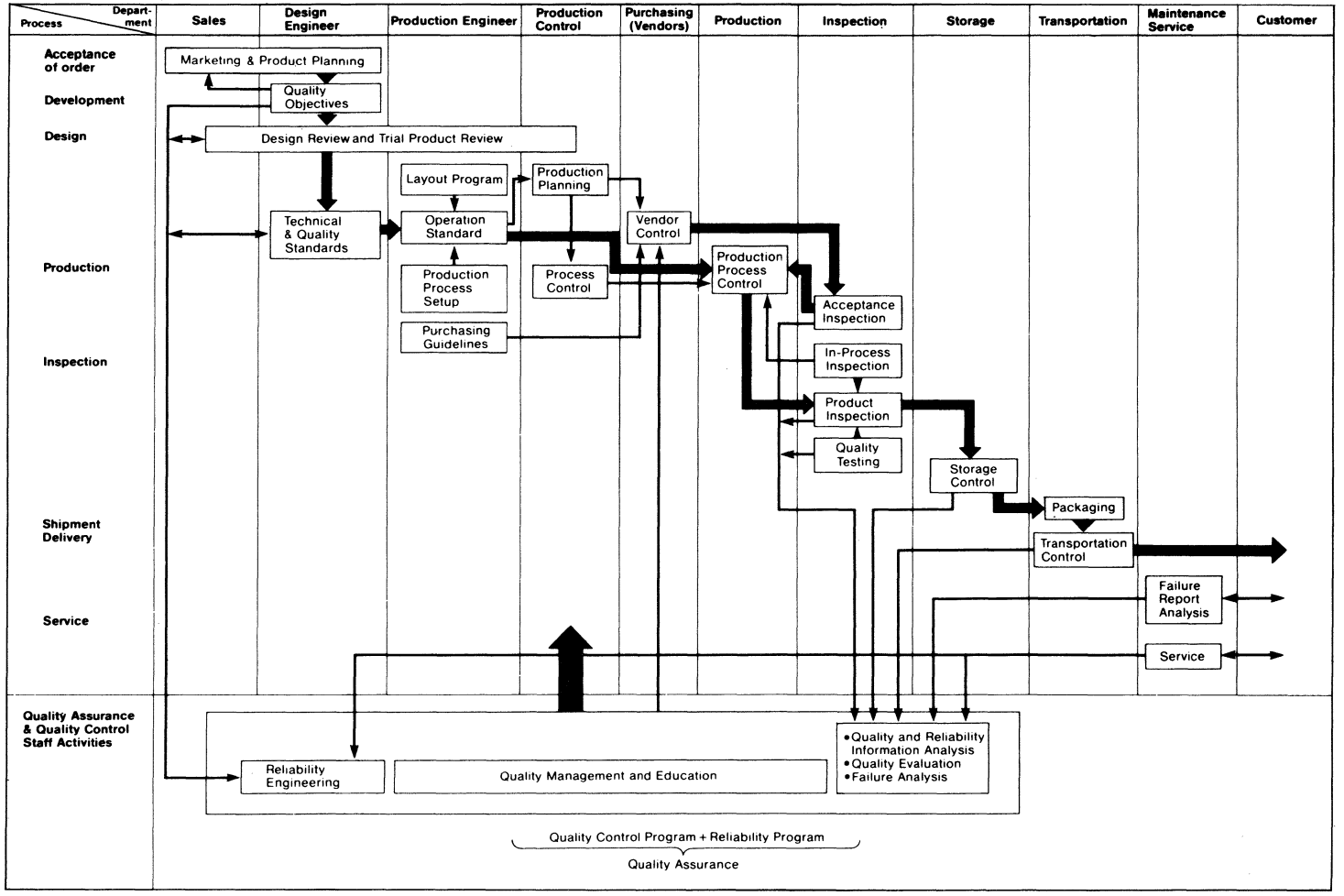


Figure 1 Quality Assurance System

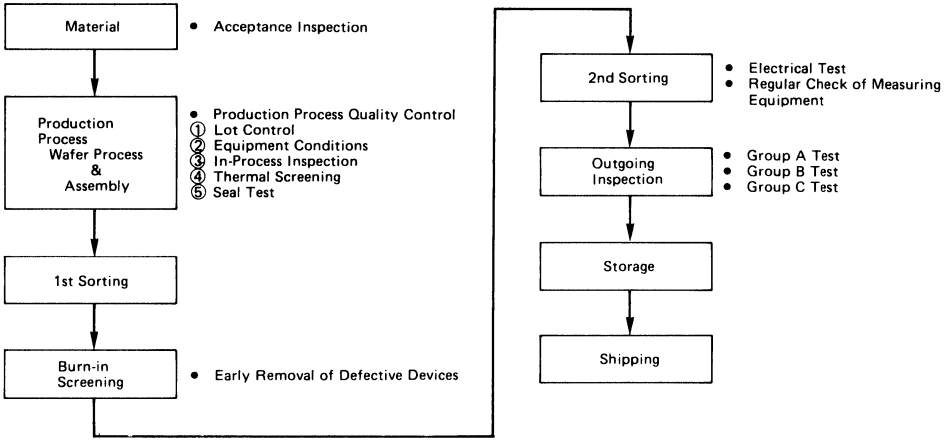


Figure 2 Manufacturing Process

Devices which pass these lot guarantee inspections are stored in a warehouse awaiting shipment to customers. Standards are also set up for handling, storage and transportation during this period, thereby ensuring quality prior to delivery. Figure 2 shows the manufacturing flow of the completed device.

5) At Oki, all devices are subjected to thorough quality checks. If, by chance, a failure does occur after delivery to the customer, defective devices are processed and the problem rectified immediately to minimize the inconvenience to the customer in accordance with the following flowchart.

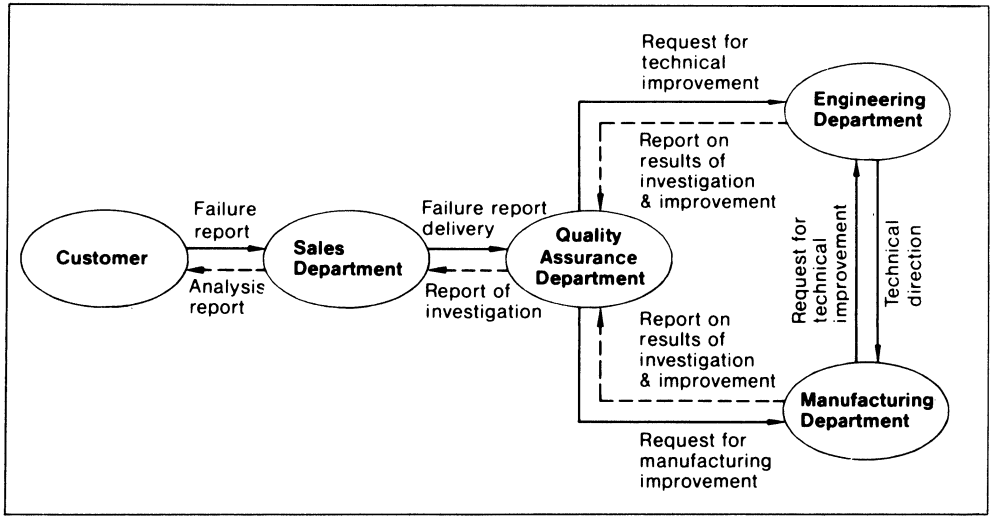
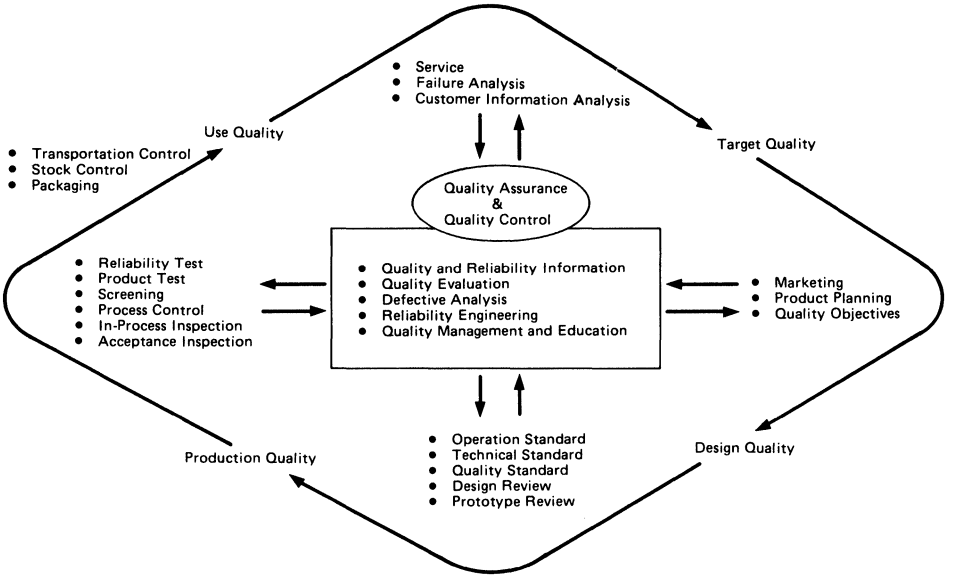


Figure 3 Failure report process

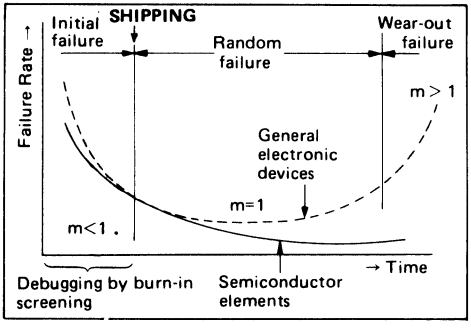

• Service
• Failure Analysis
• Customer Information Analysis
Use Quality
Target Quality
• Transportation Control
• Stock Control
• Packaging
Quality Assurance
&
Quality Control
• Reliability Test
• Product Test
• Screening
• Process Control
• In-Process Inspection
• Acceptance Inspection
• Quality and Reliability Information
• Quality Evaluation
• Defective Analysis
• Reliability Engineering
• Quality Management and Education
• Marketing
• Product Planning
• Quality Objectives
• Operation Standard
• Technical Standard
• Quality Standard
• Design Review
• Prototype Review
Production Quality
Design Quality

3

3. SEMICONDUCTOR MEMORY FAILURES

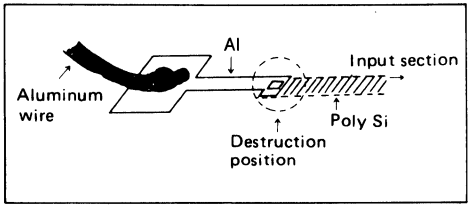
The life-span characteristics of semiconductor elements in general (not only semiconductor IC devices) is described by the curve shown in the diagram below. Although semiconductor memory failures are similar to those of ordinary integrated circuits, the degree of integration (miniaturization), manufacturing complexity and other circuit element factors influence their incidence.

Semiconductor Element Failure Rate Curve



1) Surge Destruction

This is destruction of the input/output stage circuits by external surge currents or static electricity. The accompanying photograph shows a point of contact between aluminum and polysilicon that has been dissolved by a surge current. A hole has formed in the substrate silicon, leading to a short circuit. This kind of failure is traceable in about 30% of defective devices returned to the manufacturer. Despite miniaturization of semiconductor memory component elements (which means the elements themselves are less resistant), these failures usually occur during assembly and other handling operations.
At Oki, all devices are subjected to static electricity intensity tests (under simulated operational conditions) in the development stage to reduce this type of failure. In addition to checking endurance against surge currents, special protective circuits are incorporated in the input and output sections.



2) Oxide Film Insulation Destruction (Pin Holes)

Unlike surge destruction, this kind of failure is caused by manufacturing defects. Local weakened sections are ruptured when subjected to external electrical stress. Although this problem is accentuated by the miniaturization of circuit elements, it can be resolved by maintaining an ultra-clean manufacturing environment and through 100% burn-in screening.

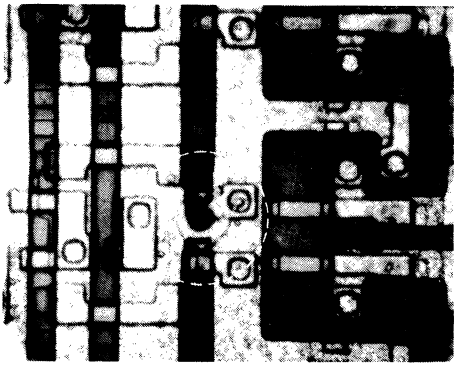
3) Surface Deterioration due to Ionic Impurities

Under some temperature and electric field conditions, charged ionic impurities moving within the oxide film previously resulted in occasional deterioration of silicon surfaces. This problem has been eliminated by new surface stabilization techniques.

4) Photolithographic Defects

Integrated circuits are formed by repeated photographic etching processes. Dust and scratches on the mask (which corresponds to a photographic negative) can cause catastrophic defects. At present, component elements have been reduced in size to the order of 10 cm through miniaturization. However, the size of dust and scratches stays the same. At Oki, a high degree of automation, minimizing human intervention in the process, and unparalleled cleanliness, solves this problem.

Example of surge destruction



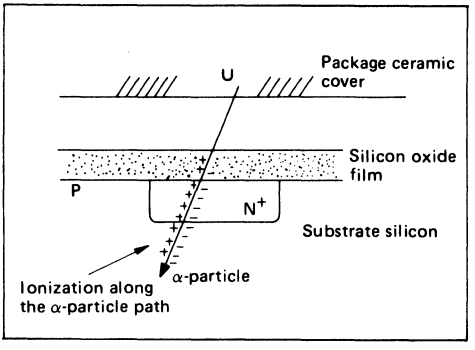
Photolithographic Defect

5) Aluminum Corrosion

Aluminum corrosion is due to electrolytic reactions caused by the presence of water and minute impurities. When aluminum dissolves, lines break. This problem is unique to the plastic capsules now used widely to reduce costs. Oki has carefully studied the possible cause and effect relationship between structure and manufacturing conditions on the one hand, and the generation of aluminum corrosion on the other. Refinements incorporated in Oki LSIs permit superior endurance to even the most severe high humidity conditions.

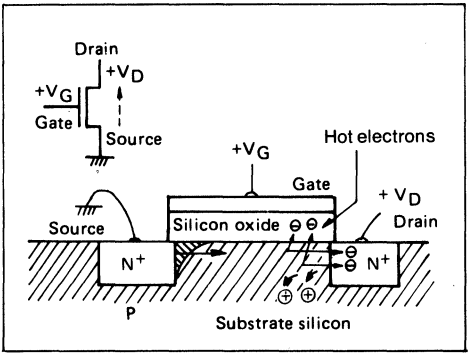
6) Alpha-Particle Soft Failure

This problem occurs when devices are highly miniaturized, such as in 1 megabit RAMs. The inversion of memory cell data by alpha-particle generated by radio-active elements like uranium and thorium (present in minute quantities, measured in ppb) in the ceramic package material causes defects. Since failure is only temporary and normal operation restored quickly, this is referred to as a "soft" failure. At Oki we have eliminated the problem by coating the chip surface of 1 megabit RAMs with a resin which effectively screens out these alpha-particles.



7) Degradation in Performance Characteristics Due to Hot Electrons

With increased miniaturization of circuit elements, internal electric field strength in the channels increases since the applied voltage remains the same at 5V. As a result, electrons flowing in the channels, as shown in the accompanying diagram, tend to enter into the oxide film near the drain, leading to degradation of performance. Although previous low-temperature operation tests have indicated an increase of this failure, we have confirmed by our low-temperature acceleration tests, including checks on test element groups, that no such problem exists in Oki LSIs.



Characteristic deterioration caused by hot electrons

With further progress in the miniaturization of circuit components, failures related to pin hole oxide film destruction and photolithography have increased. To eliminate these defects during manufacturing, Oki has been continually improving its production processes based on reliability tests and information gained from the field. And we subject all devices to high-temperature burn-in screening for 48 to 96 hours to ensure even greater reliability.

DATA SHEET

8 Bit Series 4

MSC2328A-xxYS2/KS2

262,144 Word BY 8 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2328A-xxYS2/KS2 is a fully decoded, 262,144 word × 8 bit CMOS dynamic random access memory composed of two 1Mb DRAMs in SOJ (MSM514256AJS). The mounting of two SOJs together with two 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2328A-xxYS2/KS2 are same as the original MSM514256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

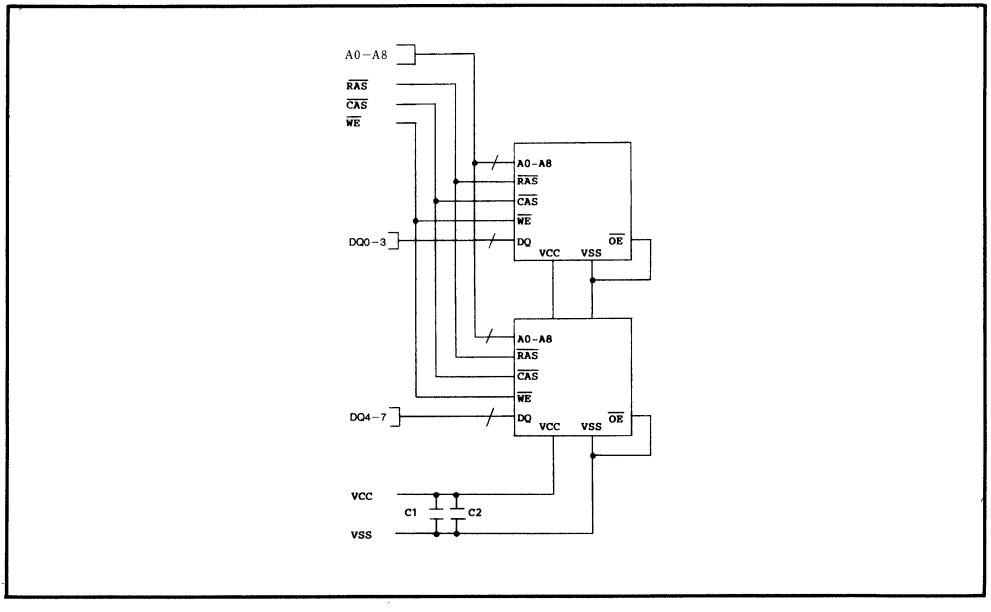
- 262,144 word × 8 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2328A-80YS2/KS2	80ns	40ns	20ns	160ns	825mW	11mW (MOS level)
MSC2328A-10YS2/KS2	100ns	50ns	25ns	190ns	715mW	

- Single + 5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms

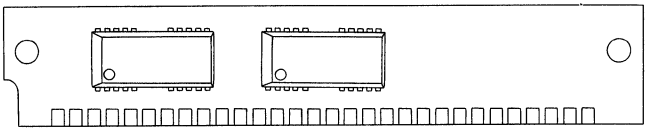
4

FUNCTIONAL BLOCK DIAGRAM

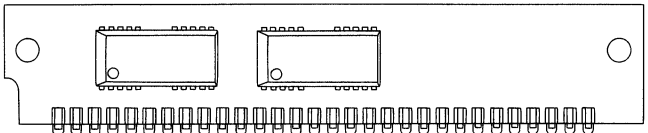


PIN CONFIGURATION

MSC2328A-xxYS2



MSC2328A-xxKS2



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	NC
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	NC
9	VSS	19	NC	29	NC
10	DQ2	20	DQ5	30	Vcc

4

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ 125	°C
Power dissipation	P_D	2	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	-1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0~+70°C)

Parameter	Symbol	Condition		MSC2328A-80YS2/KS2 Min.	MSC2328A-80YS2/KS2 Max.	MSC2328A-10YS2/KS2 Min.	MSC2328A-10YS2/KS2 Max.	Unit	Note
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.5V : All other pins not under test=0V		−20	20	−20	20	μA	
Output Leakage Current	I_{LO}	Data out is disable 0V≤V_{OUT}≤5.5V		−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA		2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA		—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$ cycling, $\overline{CAS}$ cycling, t_{RC}=min		—	150	—	130	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$=V_{IH}	TTL	—	4	—	4	mA	
			MOS	—	2	—	2	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min		—	150	—	130	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.		—	150	—	130	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min.		—	130	—	120	mA	1, 3

Note : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

4

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (A0—A8)	C_{IN1}	30	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	30	pF
Data Input/Output Capacitance (DQ0 — DQ7)	C_{DQ}	20	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 ~ +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2328A-80YS2/KS2		MSC2328A-10YS2/KS2		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	ns	
Fast page mode cycle time	t_{PC}	50	–	55	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4, 5, 6
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	50	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	

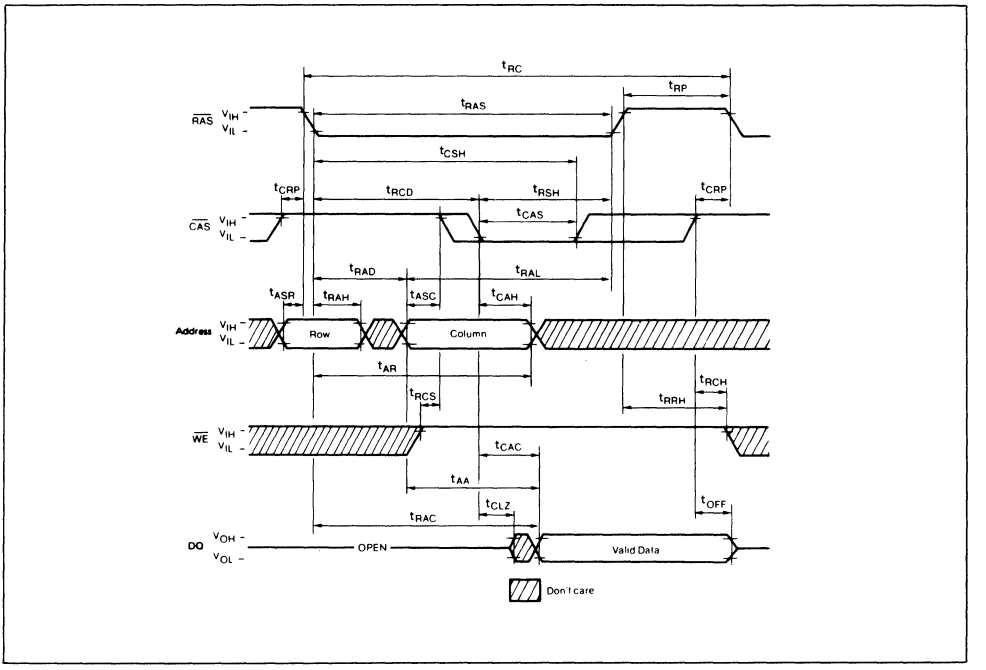
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2328A-80YS2/KS2		MSC2328A-10YS2/KS2		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	ns	
Date-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Date-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	ns	

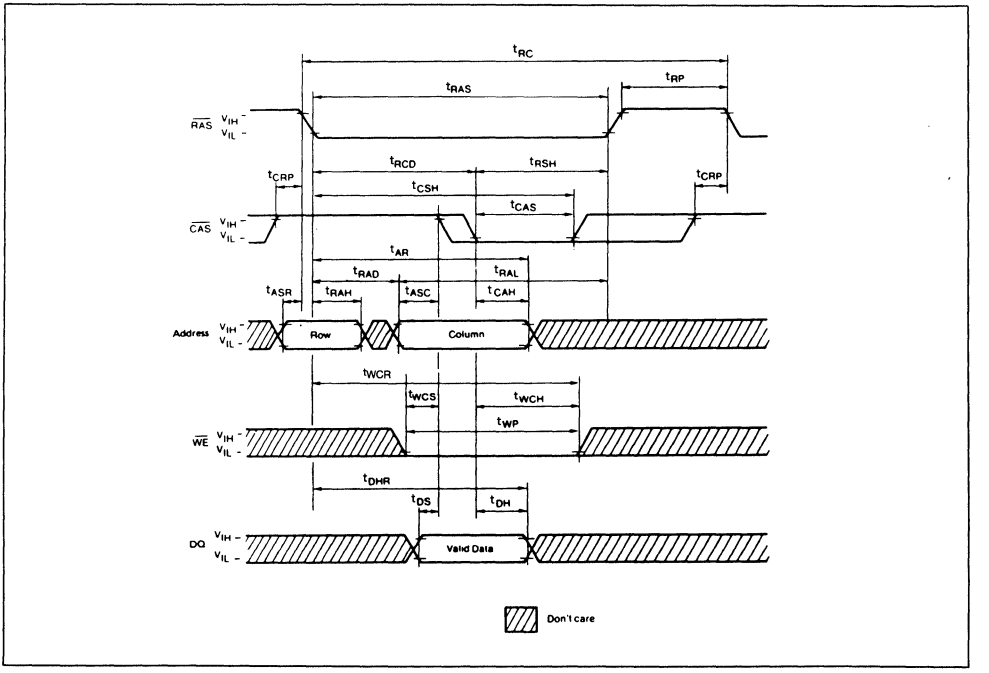
Notes:

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example : $\overline{RAS}$ only refresh cycle) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

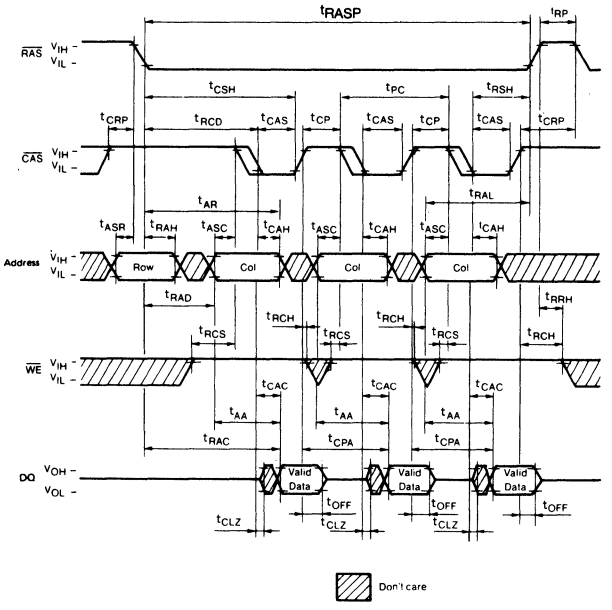
READ CYCLE



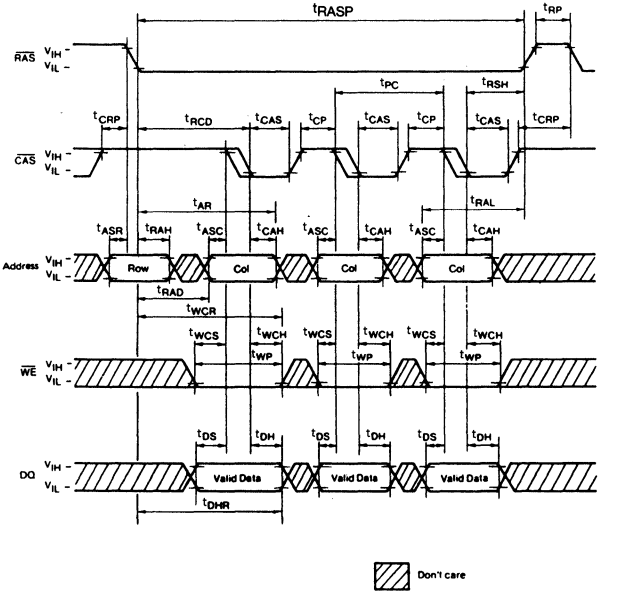
WRITE CYCLE(EARLY WRITE)



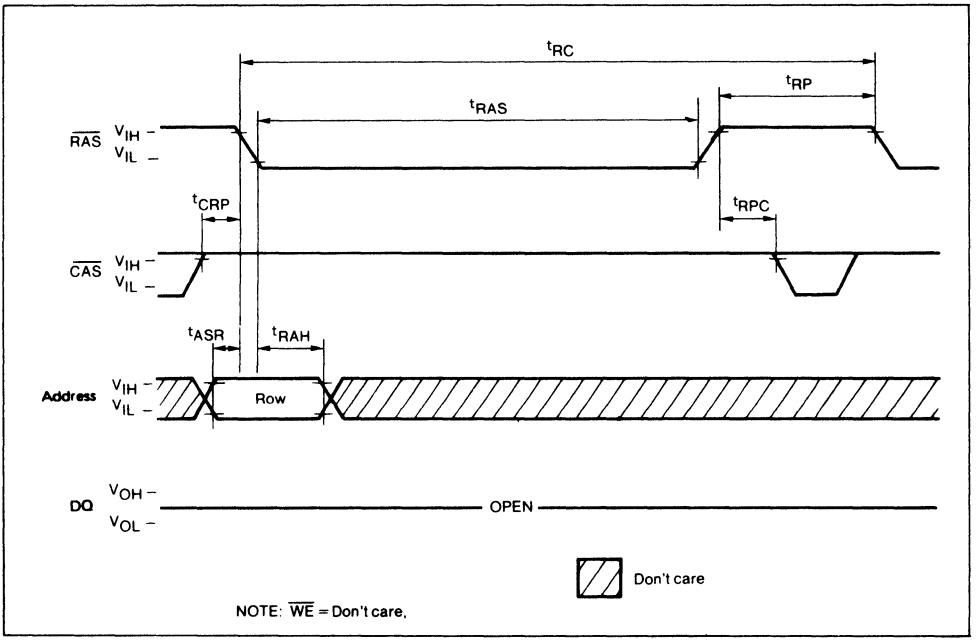
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

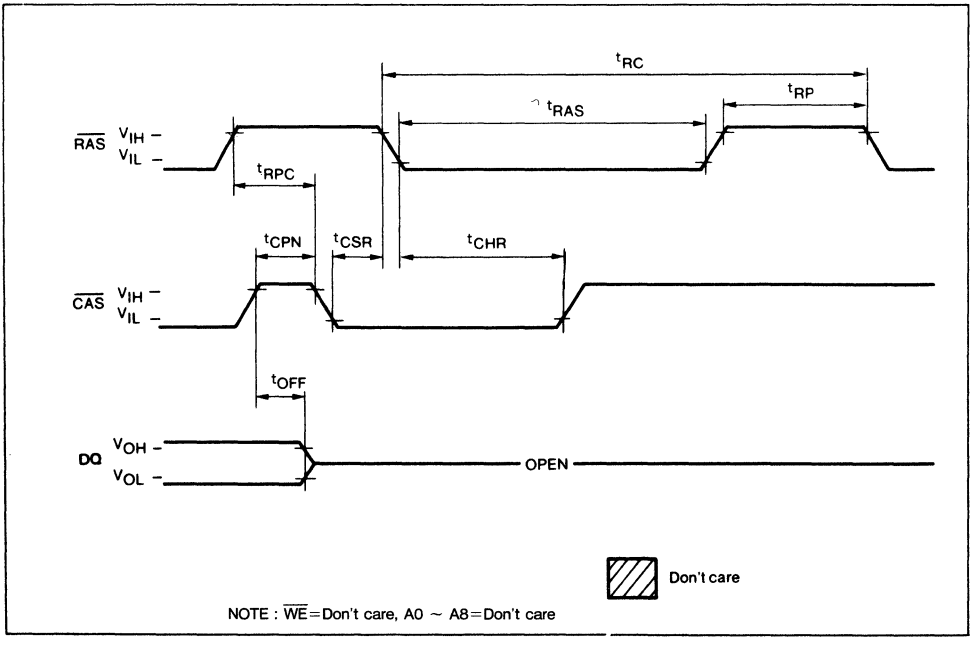


$\overline{RAS}$ ONLY REFRESH CYCLE



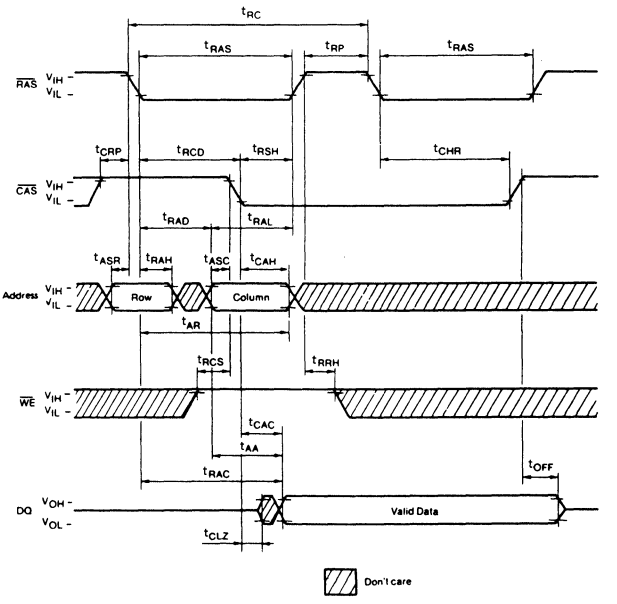
NOTE: $\overline{WE}$ = Don't care.

$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

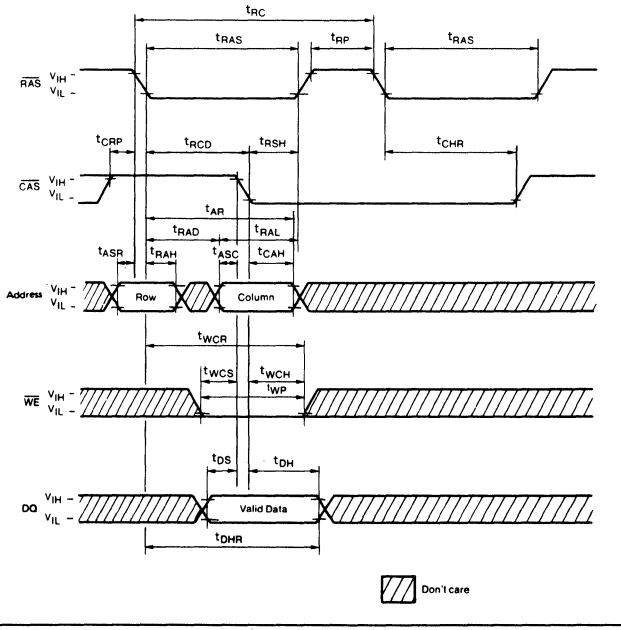


NOTE : $\overline{WE}$=Don't care, A0 ~ A8=Don't care

HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



MSC2330A-xxYS4/KS4

524,288 Word BY 8 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2330A-xxYS4/KS4 is a fully decoded, 524,288 word × 8 bit CMOS dynamic random access memory composed of four 1Mb DRAMs in SOJ (MSM514256AJS). The mounting of four SOJs together with four 0.2μF decoupling capacitors on a 30pin glass epoxy Single-in-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2330A-xxYS4/KS4 are same as the original MSM514256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

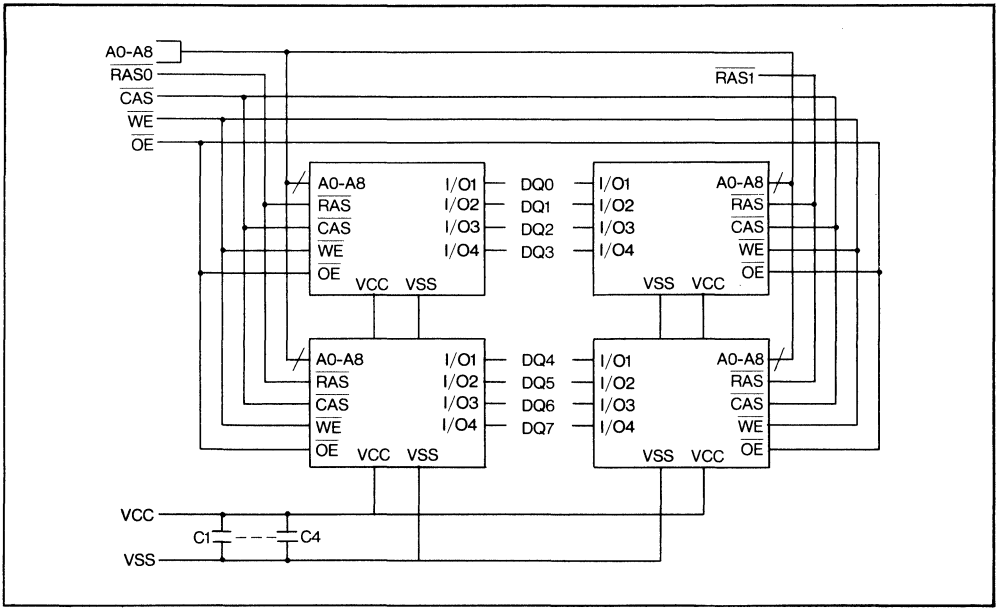
FEATURES

- 524,288 word × 8 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2330A-80YS4/KS4	80ns	40ns	20ns	160ns	847mW	22mW (MOS level)
MSC2330A-10YS4/KS4	100ns	50ns	25ns	190ns	737mW	

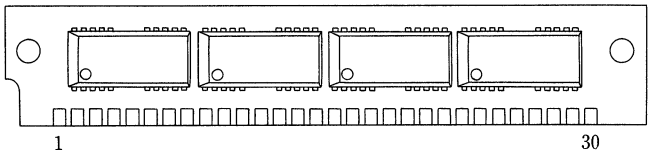
- Single + 5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms

FUNCTIONAL BLOCK DIAGRAM

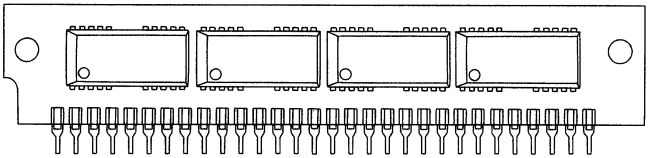


PIN CONFIGURATION

MSC2330A-xxYS4



MSC2330A-xxKS4



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	Vcc
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	VSS
7	A2	17	A8	27	$\overline{RAS0}$
8	A3	18	NC	28	$\overline{OE}$
9	VSS	19	$\overline{RAS1}$	29	NC
10	DQ2	20	DQ5	30	Vcc

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ 125	°C
Power dissipation	P_D	4	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0~+70°C)

Parameter	Symbol	Condition	MSC2330A-80YS4/KS4 Min.	MSC2330A-80YS4/KS4 Max.	MSC2330A-10YS4/KS4 Min.	MSC2330A-10YS4/KS4 Max.	Unit	Note
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.5V : All other pins not under test=0V	−40	40	−40	40	μA	
Output Leakage Current	I_{LO}	Data out is disable 0V≤V_{OUT}≤5.5V	−20	20	−20	20	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA	2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA	—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS0}$, $\overline{RAS1}$ cycling, $\overline{CAS}$ cycling, t_{RC}=min	—	154	—	134	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS0}$, $\overline{RAS1}$ =V_{IH} TTL	—	8	—	8	mA	
		$\overline{CAS}$=V_{IH} MOS	—	4	—	4	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS0}$, $\overline{RAS1}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min	—	154	—	134	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.	—	154	—	134	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS0}$, $\overline{RAS1}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min.	—	134	—	124	mA	1, 3

Note* : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (A0—A8)	C_{IN1}	30	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	40	pF
Data Input/Output Capacitance (DQ0 — DQ7)	C_{DQ}	30	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 ~ +70°C) Note 1, 2, 3

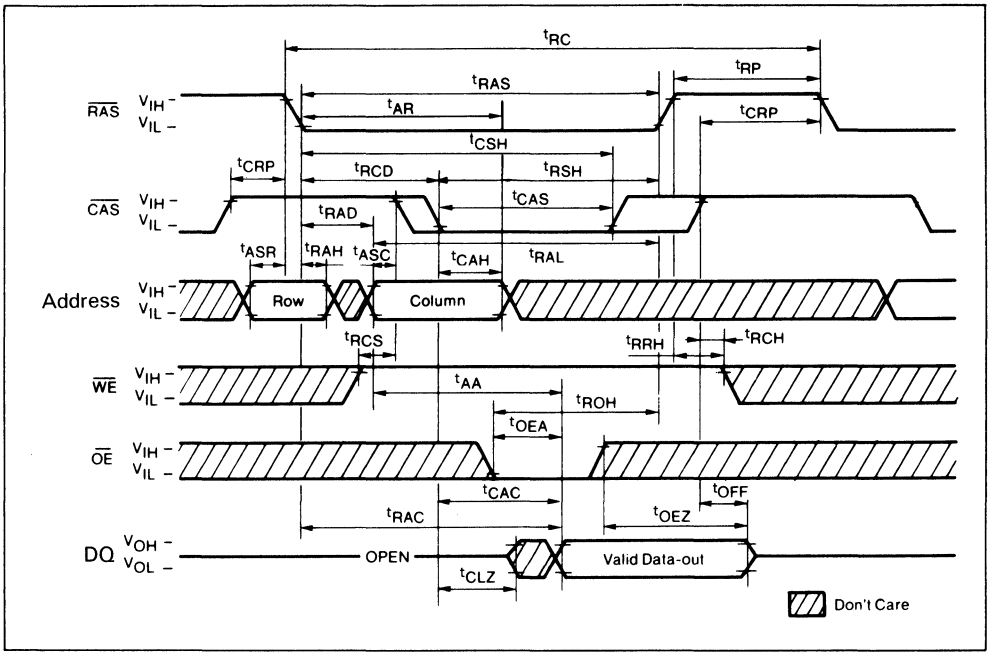
Parameter	Symbol	MSC2330A-80YS4/KS4		MSC2330A-10YS4/KS4		Unit	Note
		Min.	Max.	Min.	Max.		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	215	–	255	–	ns	
Fast page mode cycle time	t_{PC}	50	–	55	–	ns	
Fast page mode Read/write cycle time	t_{PRMW}	105	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4, 5, 6
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	50	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{RAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hole time	t_{RAH}	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	

AC CHARACTERISTICS (Continued)

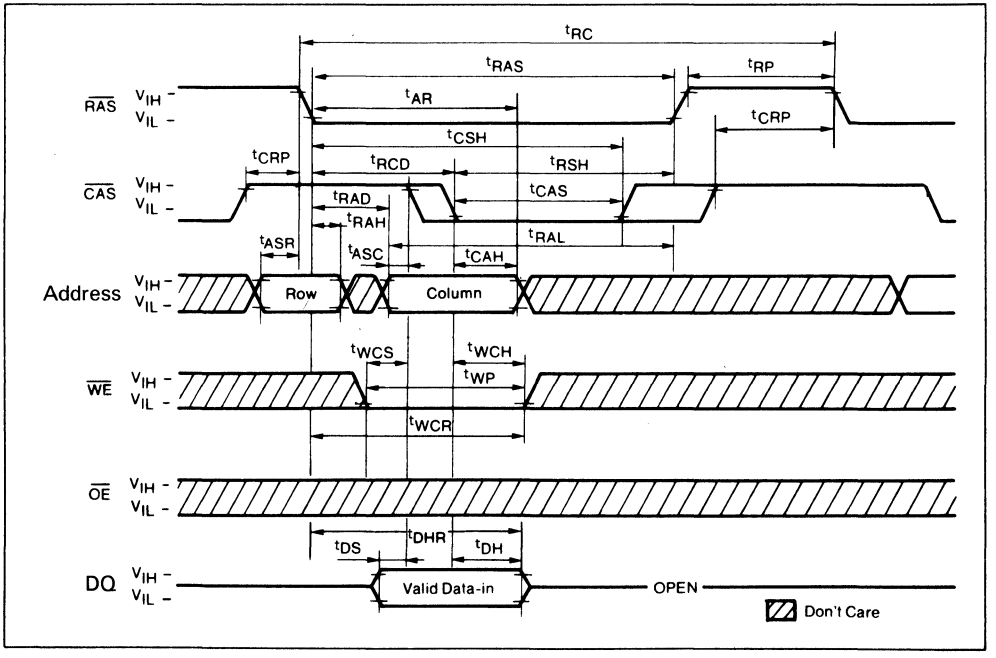
Parameter	Symbol	MSC2330A-80YS4/KS4		MSC2330A-10YS4/KS4		Unit	Note
		Min.	Max.	Min.	Max.		
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	50	–	60	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	110	–	135	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	70	–	85	–	ns	7
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	ns	
$\overline{RAS}$ hold time refemenced to $\overline{OE}$	t_{ROH}	20	–	20	–	ns	
Access time from $\overline{OE}$	t_{OEA}	–	20	–	25	ns	
$\overline{OE}$ delay time	t_{OED}	20	–	25	–	ns	
$\overline{OE}$ to data output buffer turn-on delay	t_{OEZ}	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	25	–	ns	

Notes:
1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example : $\overline{RAS}$ only Refresh cycle) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; it t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{CWD} (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

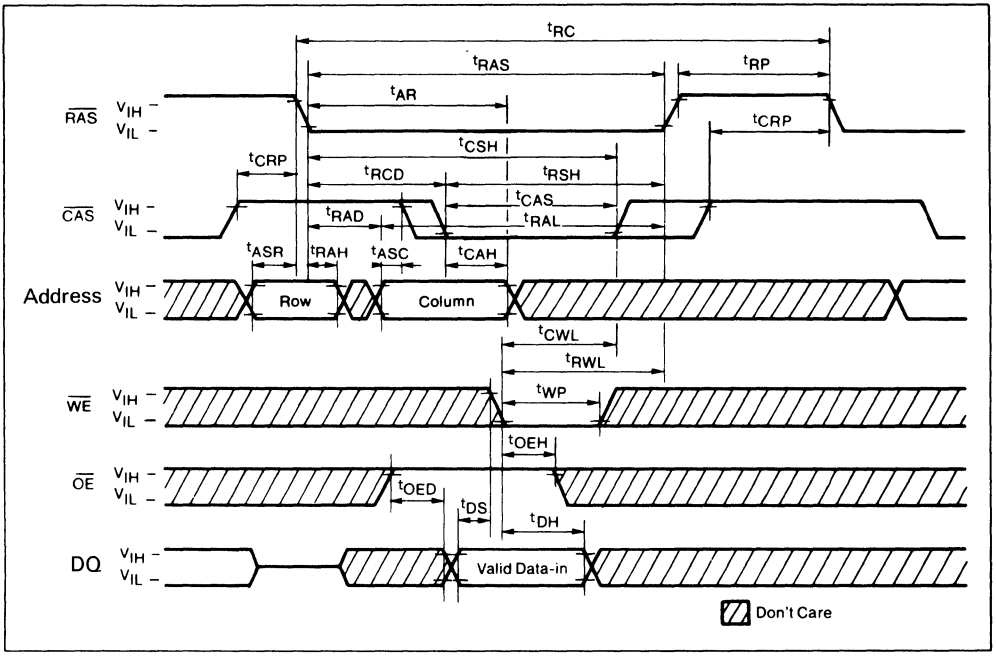
READ CYCLE



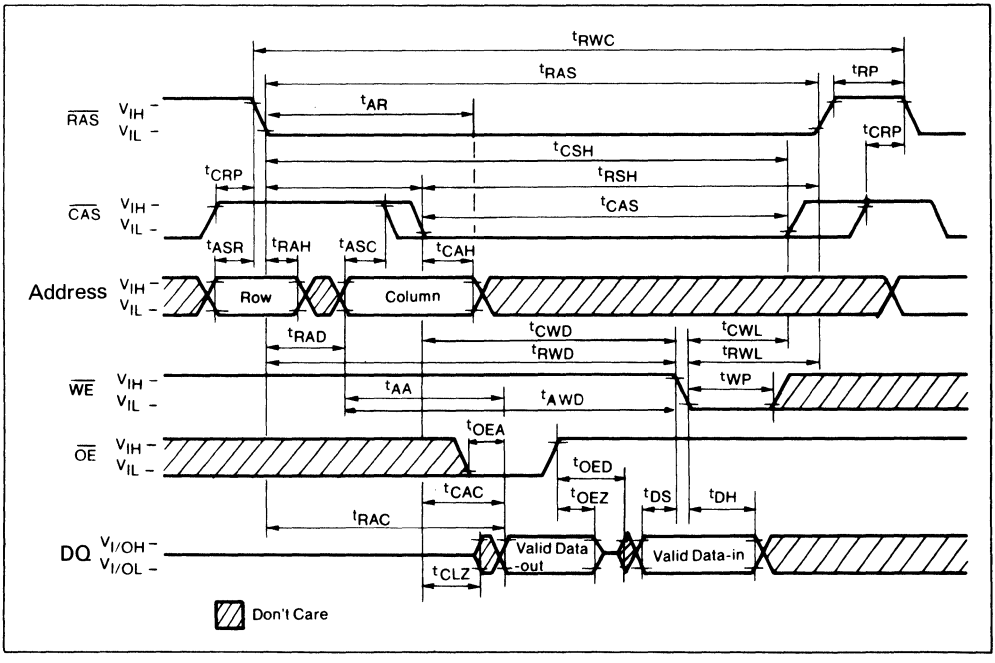
WRITE CYCLE (EARLY WRITE)



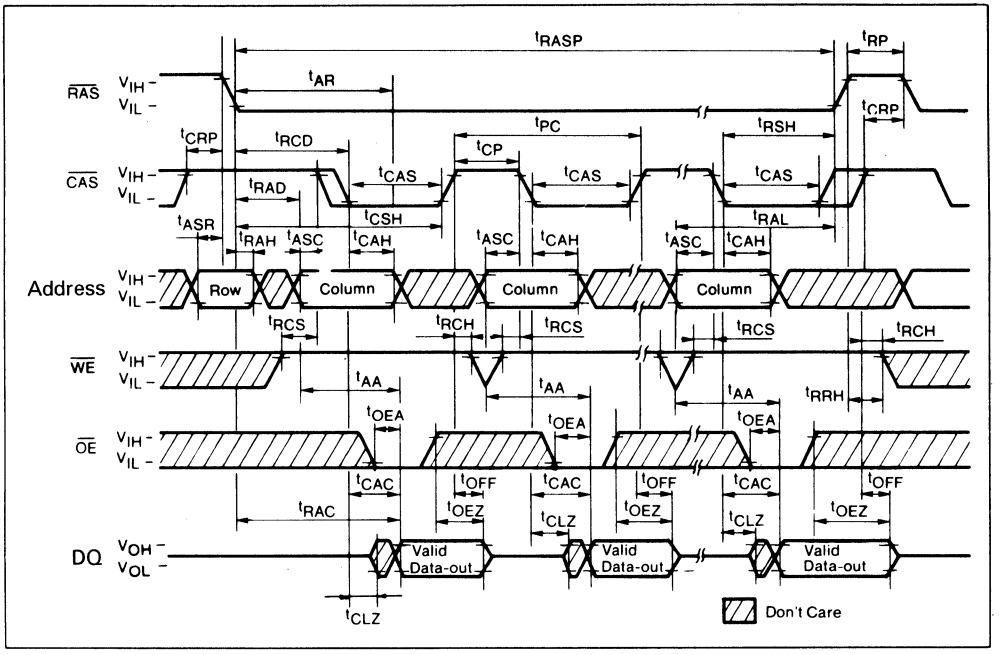
WRITE CYCLE ($\overline{OE}$ CONTROL WRITE)



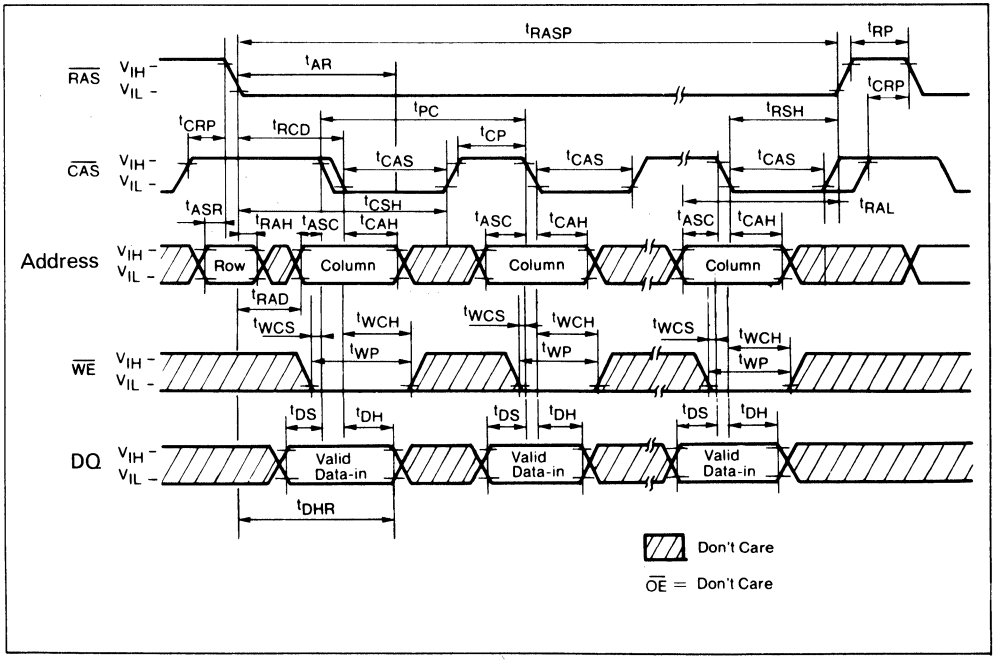
READ/WRITE CYCLE



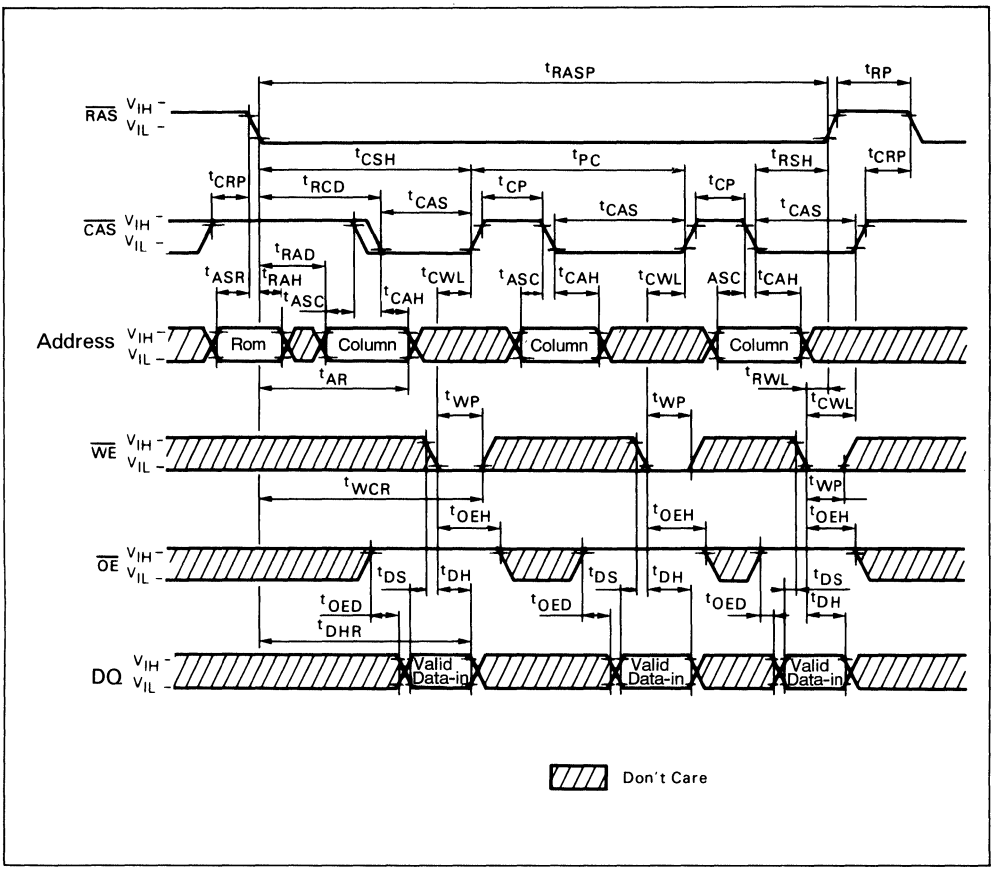
FAST PAGE MODE READ CYCLE



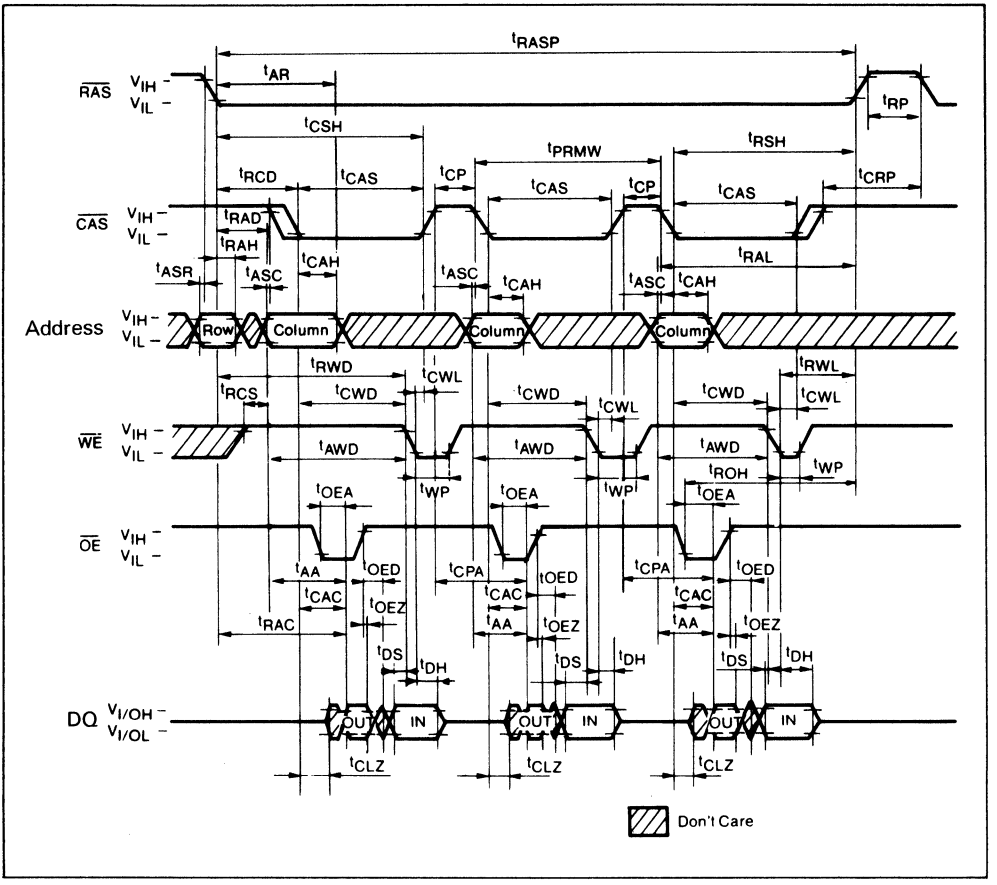
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



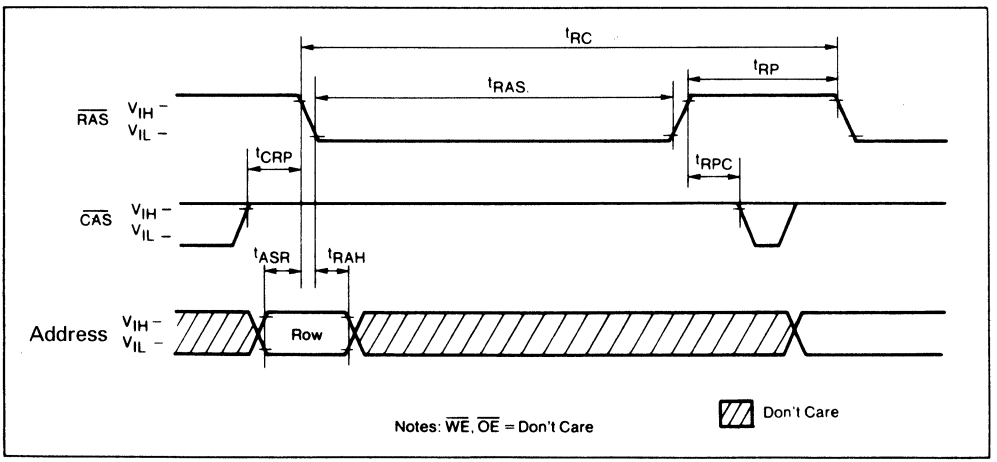
FAST PAGE MODE WRITE CYCLE($\overline{OE}$ CONTROL WRITE)



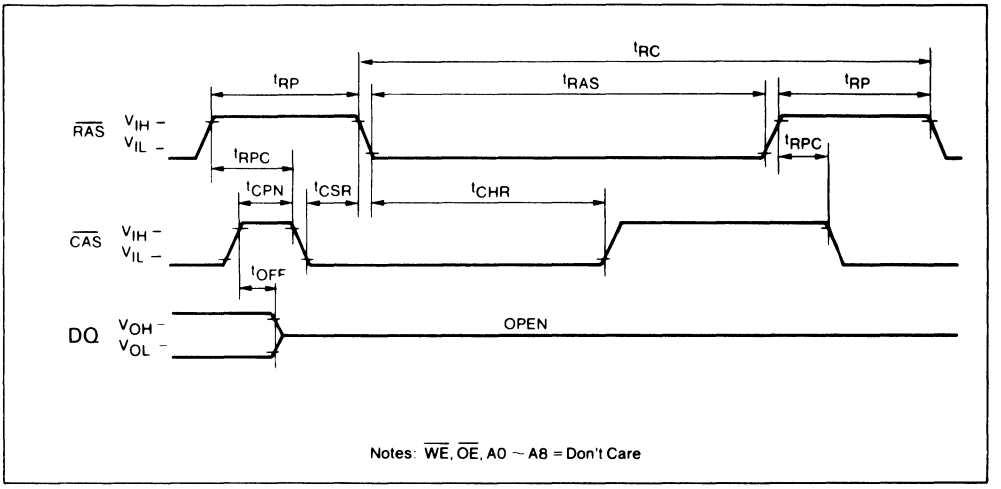
FAST PAGE MODE READ/WRITE CYCLE



RAS ONLY REFRESH CYCLE

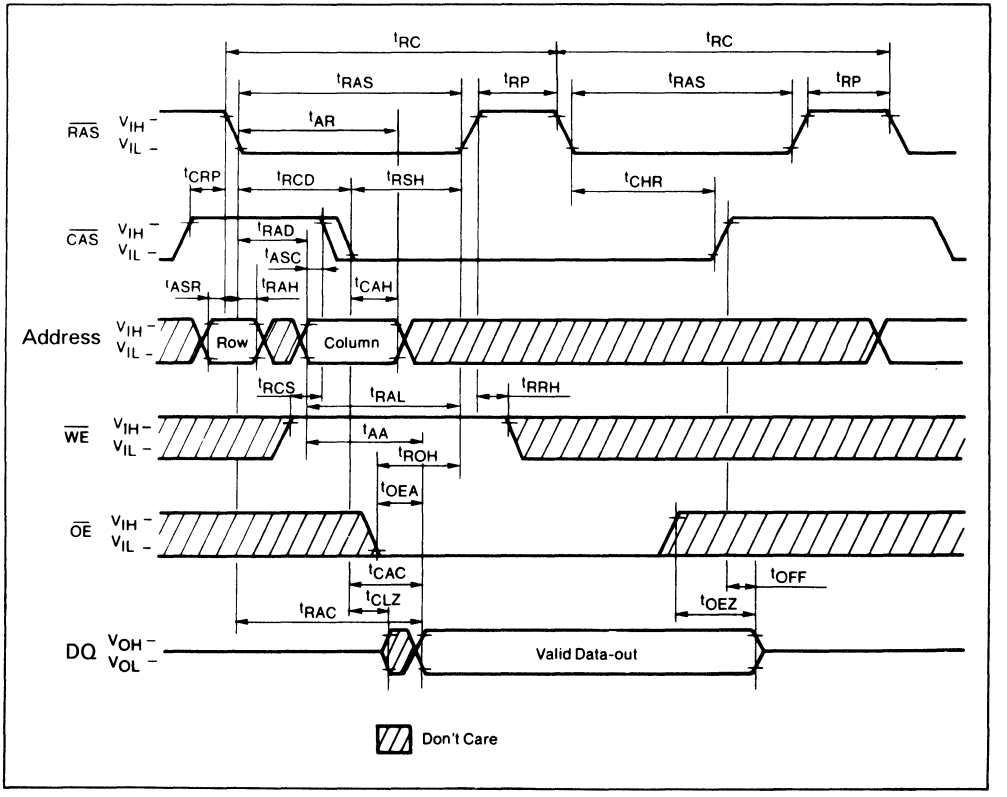


$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

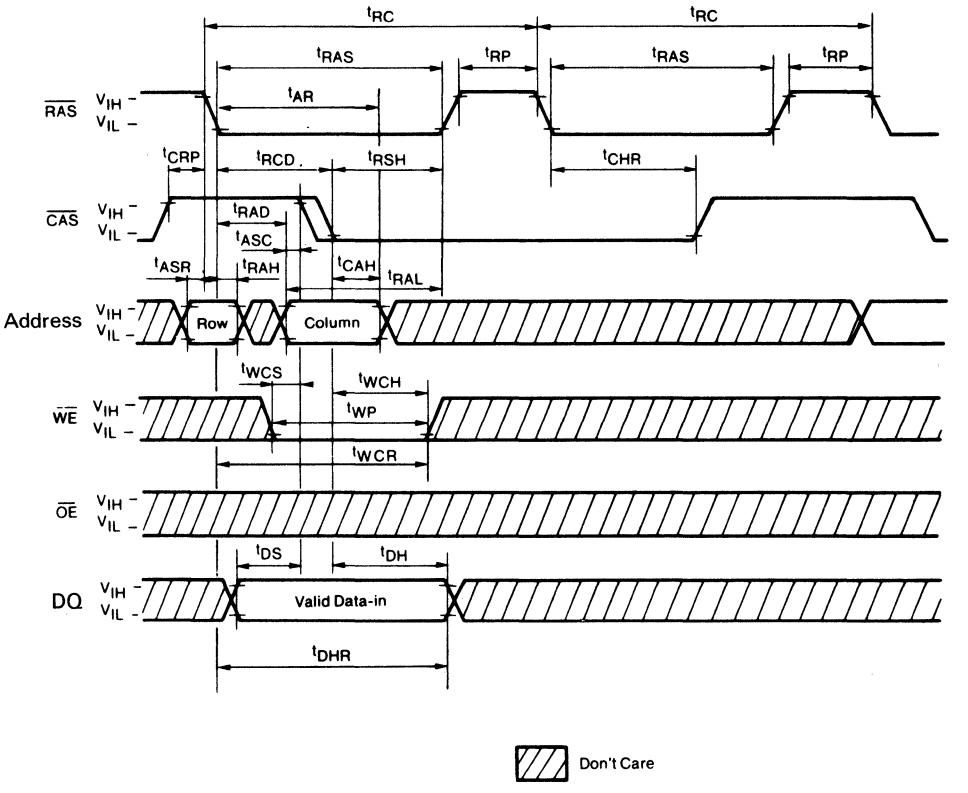


Notes: $\overline{WE}$, $\overline{OE}$, A0 ~ A8 = Don't Care

HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



MSC2313A-xxYS8/KS8

1,048,576 Word BY 8 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2313A-xxYS8/KS8 is a fully decoded, 1,048,576 word × 8 bit CMOS dynamic random access memory composed of eight 1Mb DRAMs in SOJ (MSM511000AJS). The mounting of eight SOJs together with eight 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2313A-xxYS8/KS8 are same as the original MSM511000AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

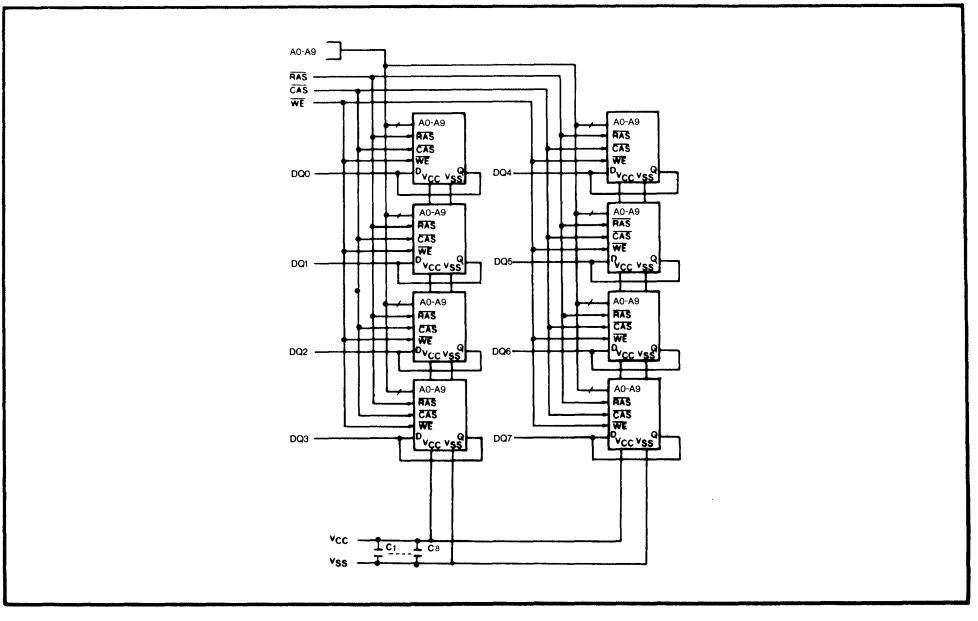
FEATURES

- 1,048,576 word × 8 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2313A-70YS8/KS8	70ns	35ns	20ns	140ns	3740mW	44mW (MOS level)
MSC2313A-80YS8/KS8	80ns	40ns	20ns	160ns	3300mW	
MSC2313A-10YS8/KS8	100ns	50ns	25ns	190ns	2860mW	

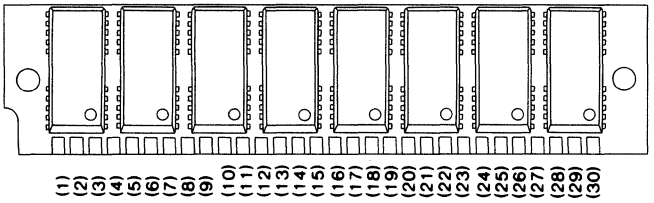
- Single + 5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms

FUNCTIONAL BLOCK DIAGRAM

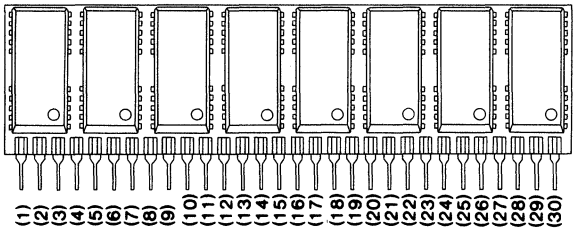


PIN CONFIGURATION

MSC2313A-xxYS8



MSC2313A-xxKS8



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	NC
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	NC
9	VSS	19	NC	29	NC
10	DQ2	20	DQ5	30	Vcc

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ 125	°C
Power dissipation	P_D	8	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0~+70°C)

Parameter	Symbol	Condition		MSC2313A-70YS8/KS8 Min.	MSC2313A-70YS8/KS8 Max.	MSC2313A-80YS8/KS8 Min.	MSC2313A-80YS8/KS8 Max.	MSC2313A-10YS8/KS8 Min.	MSC2313A-10YS8/KS8 Max.	Unit	Note
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.5V : All other pins not under test=0V		−80	80	−80	80	−80	80	μA	
Output Leakage Current	I_{LO}	Data out is disable 0V≤V_{OUT}≤5.5V		−10	10	−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA		2.4	—	2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA		—	0.4	—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$ cycling, $\overline{CAS}$ cycling, t_{RC}=min		—	680	—	600	—	520	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$=V_{IH}	TTL	—	16	—	16	—	16	mA	
			MOS	—	8	—	8	—	8	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min		—	680	—	600	—	520	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.		—	680	—	600	—	520	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min.		—	560	—	480	—	440	mA	1, 3

Note : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0—A9)	C_{IN1}	37	60	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	35	65	pF
Data Input/Output Capacitance (DQ0—DQ7)	C_{DQ}	7	20	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 ~ +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2313A-70YS8/KS8		MSC2313A-80YS8/KS8		MSC2313A-10YS8/KS8		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	140	–	160	–	190	–	ns	
Fast page mode cycle time	t_{PC}	45	–	50	–	55	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	70	–	80	–	100	ns	4, 5, 6
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	20	–	25	ns	4. 5
Access time from column address	t_{AA}	–	35	–	40	–	50	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	40	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	60	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10K	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	55	–	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	–	40	–	50	–	ns	

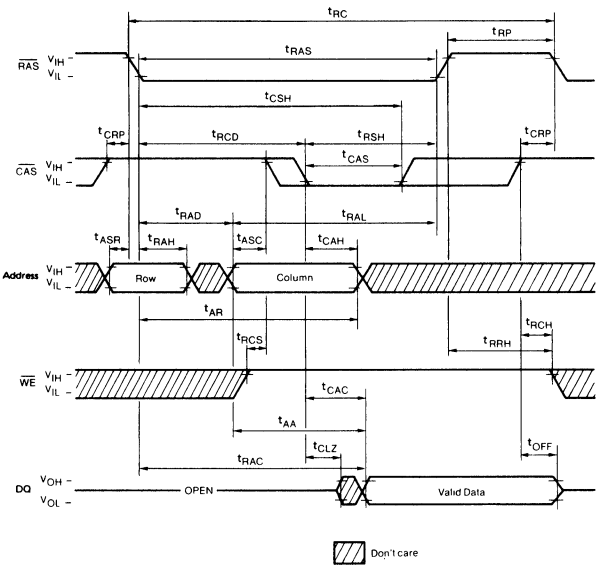
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2313A-70YS8/KS8		MSC2313A-80YS8/KS8		MSC2313A-10YS8/KS8		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	55	–	60	–	75	–	ns	
Write command se-up time	t_{WCS}	0	–	0	–	0	–	ns	
Write comman hold time	t_{WCH}	15	–	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	55	–	60	–	75	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	10	–	15	–	ns	

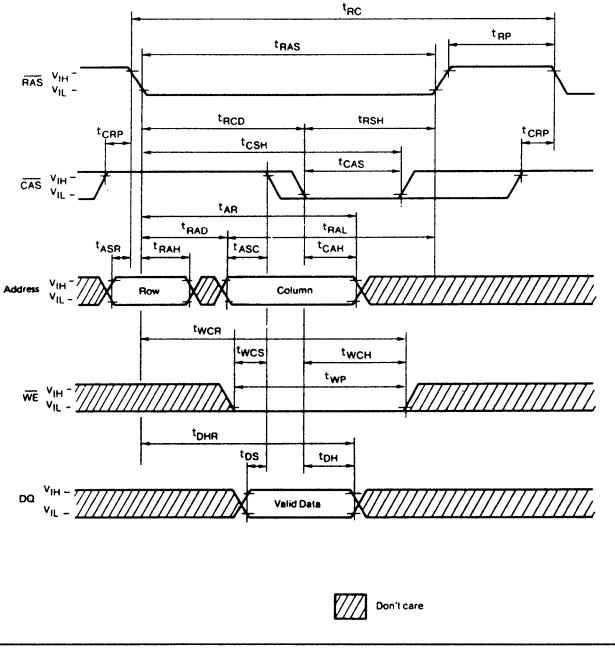
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example : $\overline{RAS}$ only refresh cycle) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL loads and 100pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

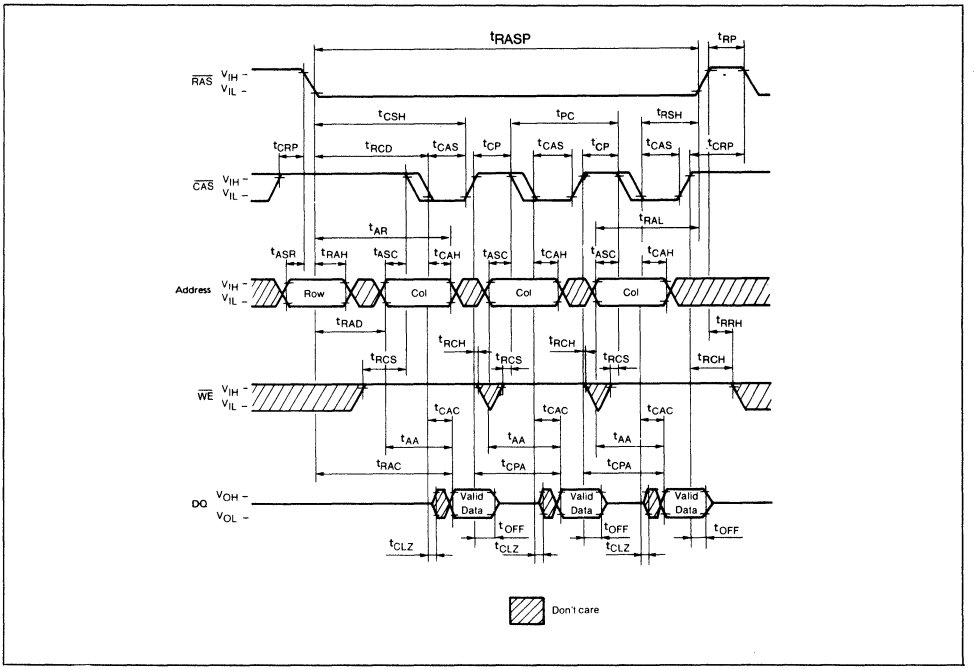
READ CYCLE



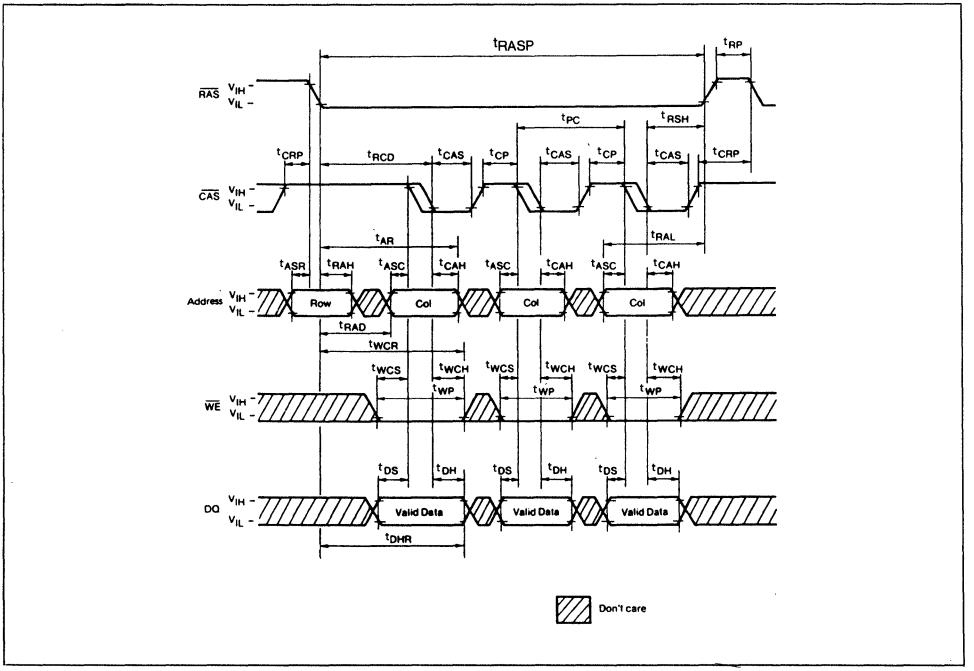
WRITE CYCLE(EARLY WRITE)



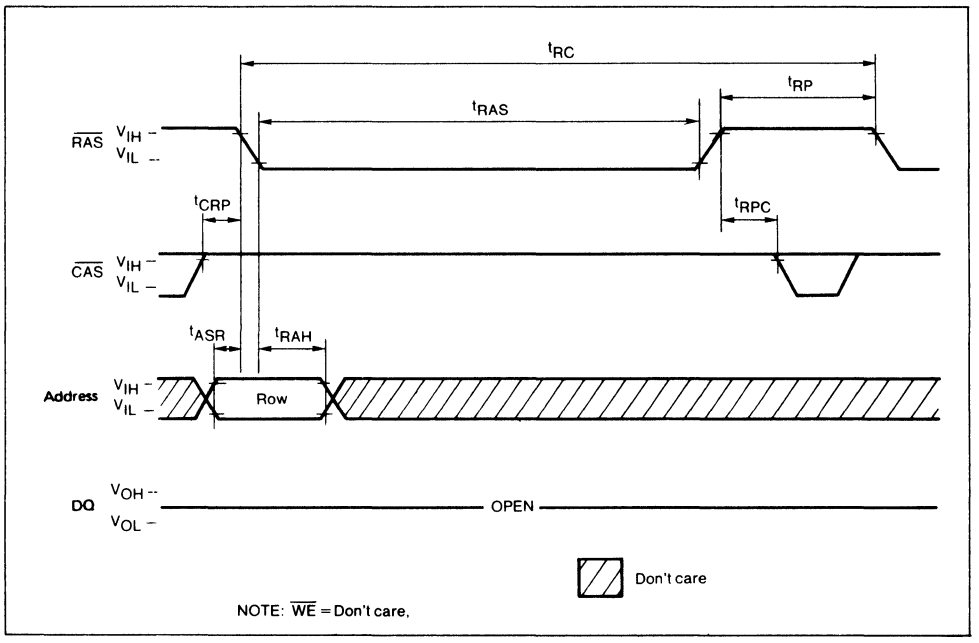
FAST PAGE MODE READ CYCLE



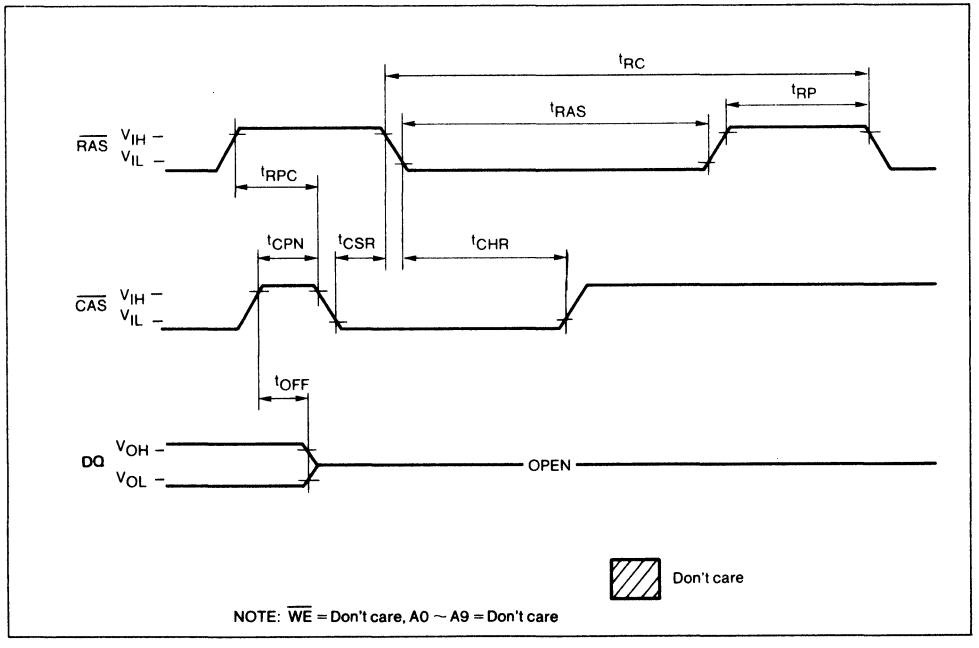
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



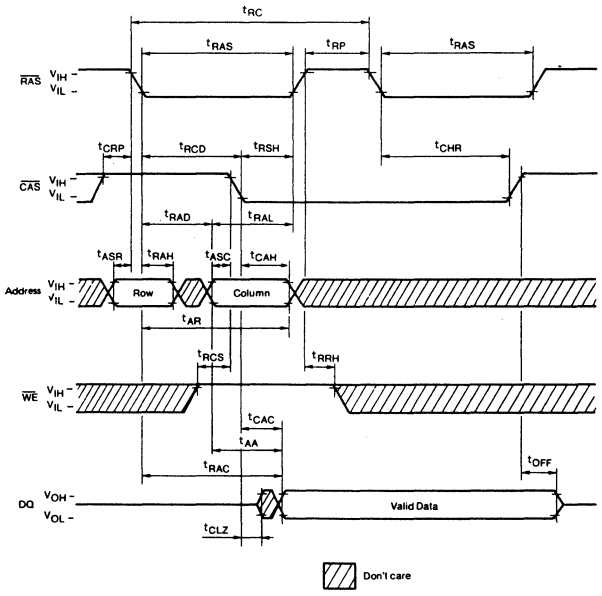
RAS ONLY REFRESH CYCLE



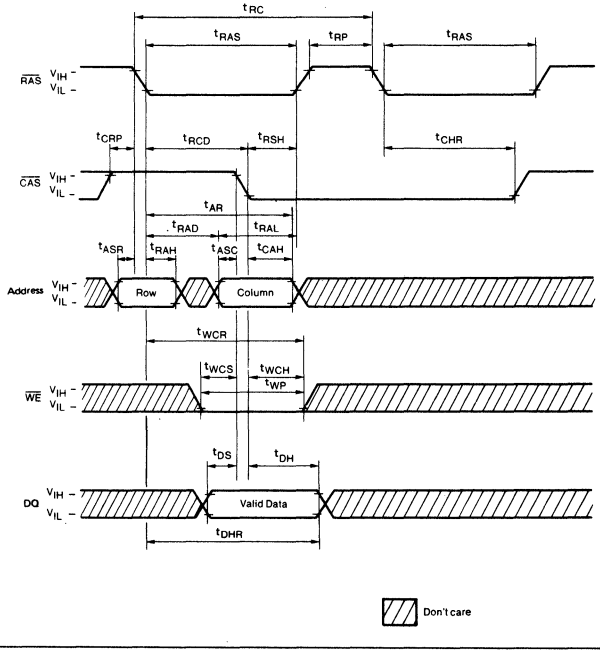
CAS BEFORE RAS AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



OKI semiconductor
MSC2358-xxKS2

PRELIMINARY

1,048,576 Word x 8 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2358-xxKS2 is a fully decoded, 1,048,576 word by 8 bit CMOS dynamic random access memory composed of two 4Mb DRAMs in SOJ (MSM514400JS). The mounting of two SOJs together with two 0.2 µF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2358-xxKS2 are same as the original MSM514400JS; each timing requirements are noncritical, and power supply tolerance is very wide.

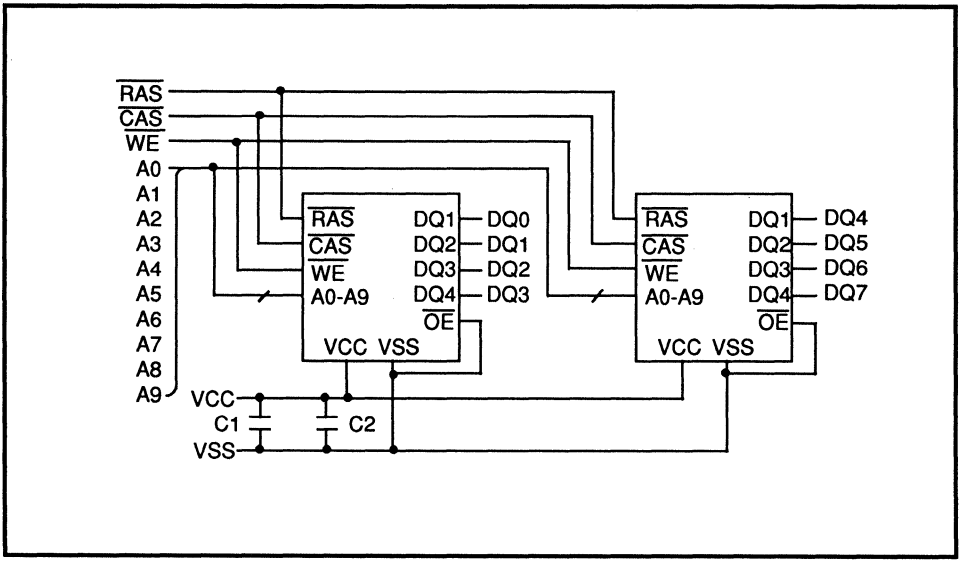
FEATURES

- 1,048,576 word x 8 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (MAX)	Standby (MAX)
MSC2358-80KS2	80 ns	40 ns	20 ns	160 ns	990 mW	11mW (MOS level)
MSC2358-10KS2	100 ns	50 ns	25 ns	190 ns	880 mW	

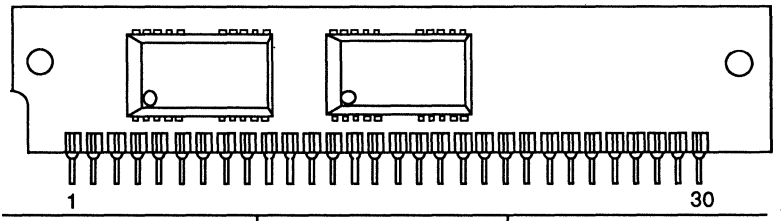
- Single +5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi-bit test mode capability

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

MSC2358-xxKS2



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	$\overline{VCC}$	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	N. C.
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	N. C.
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	N. C.
9	VSS	19	N. C.	29	N. C.
10	DQ2	20	DQ5	30	VCC

9 Bit Series 4

MSC2329-xxYS3/KS3

262,144 Word BY 9 Bit DYNAMIC RAM MODULE : PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2329-xxYS3/KS3 is a fully decoded, 262,144 word × 9 bit dynamic random access memory composed of two 1 Mb DRAMs in SOJ (MSM514256AJS) and one 256Kb DRAM in PLCC (MSM41256AJS). The mounting of two SOJs and one PLCC together with three 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2329-xxYS3/KS3 are same as the original MSM41256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

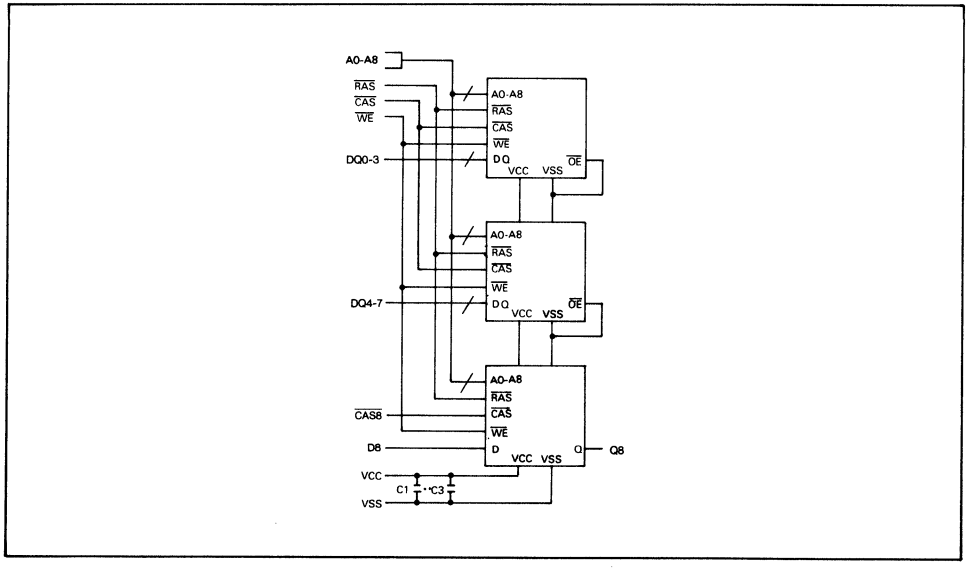
FEATURES

- 262,144 word × 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)		Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2329-10YS3/KS3	100ns	50ns	200ns	1155mW	50mW
MSC2329-12YS3/KS3	120ns	60ns	220ns	1073mW	

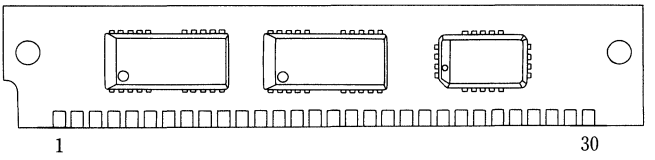
- Single + 5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms
- Common $\overline{CAS}$ Control for eight Common Data-in and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-in and Data-Out Lines

FUNCTIONAL BLOCK DIAGRAM

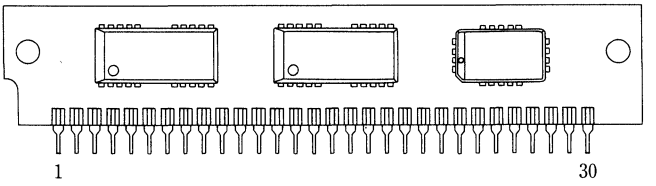


PIN CONFIGURATION

MSC2329-xxYS3



MSC2329-xxKS3



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	Q8
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS8}$
9	VSS	19	NC	29	D8
10	DQ2	20	DQ5	30	Vcc

4

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ +125	°C
Power dissipation	P_D	4	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	-1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0~+70°C)

Parameter	Symbol	Condition	MSC2329-10YS3/KS3		MSC2329-12YS3/KS3		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.5V : All other pins not under test=0V	−30	30	−30	30	μA	
Output Leakage Current	I_{LO}	DQ0-7, Q8=disable 0V≤V_{OUT}≤5.5V	−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA	2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA	—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$, $\overline{CAS8}$ cycling, t_{RC}=min	—	210	—	195	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$, $\overline{CAS8}$=V_{IH}	—	9	—	9	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$=V_{IH} t_{RC}=min	—	205	—	190	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.	—	205	—	190	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$=V_{IL} $\overline{CAS}$, $\overline{CAS8}$ cycling t_{PC}=min.	—	150	—	135	mA	1, 3

Note : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (A0 — A8)	C_{IN1}	40	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	pF
Data Input/Output Capacitance (DQ0 — DQ7)	C_{DQ}	20	pF
Input Capacitance ($\overline{CAS8}$)	C_{IN3}	10	pF
Input Capacitance (D8)	C_{IN4}	10	pF
Output Capacitance (Q8)	C_{OUT}	15	pF

Capacitance measured with Boonton Meter.

4

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 ~ +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2329-10YS3/KS3		MSC2329-12YS3/KS3		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	4	–	4	ms	
Random read or write cycle time	t_{RC}	200	–	220	–	ns	
Page mode cycle time	t_{PC}	100	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	100	–	120	ns	4, 5
Access time from $\overline{CAS}$	t_{CAC}	–	50	–	60	ns	4. 5
Output buffer turn-off delay	t_{OFF}	0	30	0	30	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	90	–	90	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	100	10K	120	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	50	–	60	–	ns	
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	40	–	50	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	50	10K	60	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	100	–	120	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	50	25	60	ns	5
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	20	–	25	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	20	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	75	–	90	–	ns	

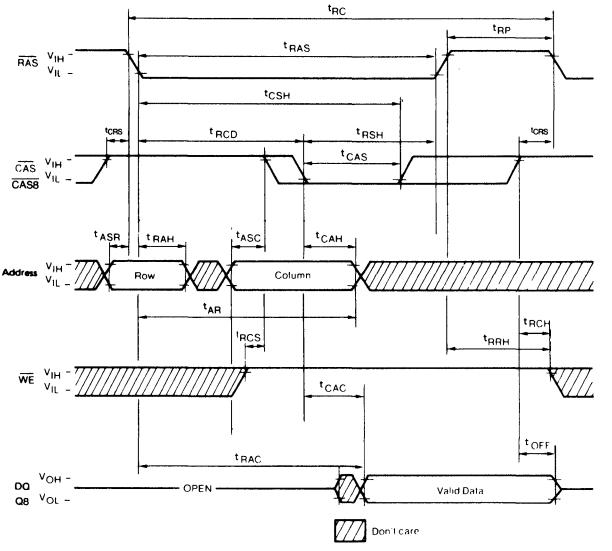
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2329-10YS3/KS3		MSC2329-12YS3/KS3		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	6
Write command hold time from $\overline{RAS}$	t_{WCR}	75	–	90	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	20	–	20	–	ns	
Write command pulse width	t_{WP}	20	–	20	–	ns	
Date-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	20	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	75	–	90	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20	–	20	–	ns	6
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	20	–	25	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$	t_{FCH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	20	–	25	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	20	–	20	–	ns	

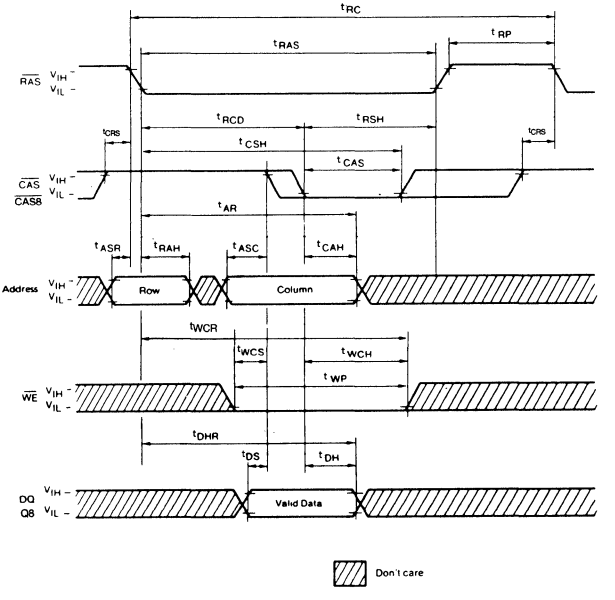
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example : $\overline{RAS}$ only refresh cycle) before proper device operation is acieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2 TTL loads and 100pF
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

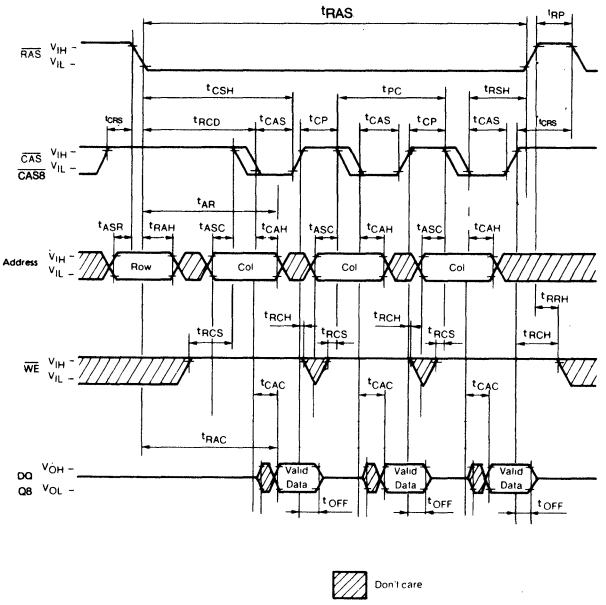
READ CYCLE



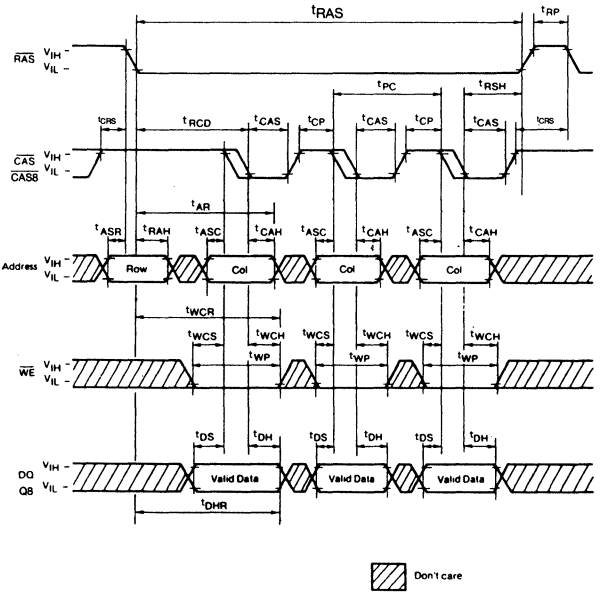
WRITE CYCLE (EARLY WRITE)



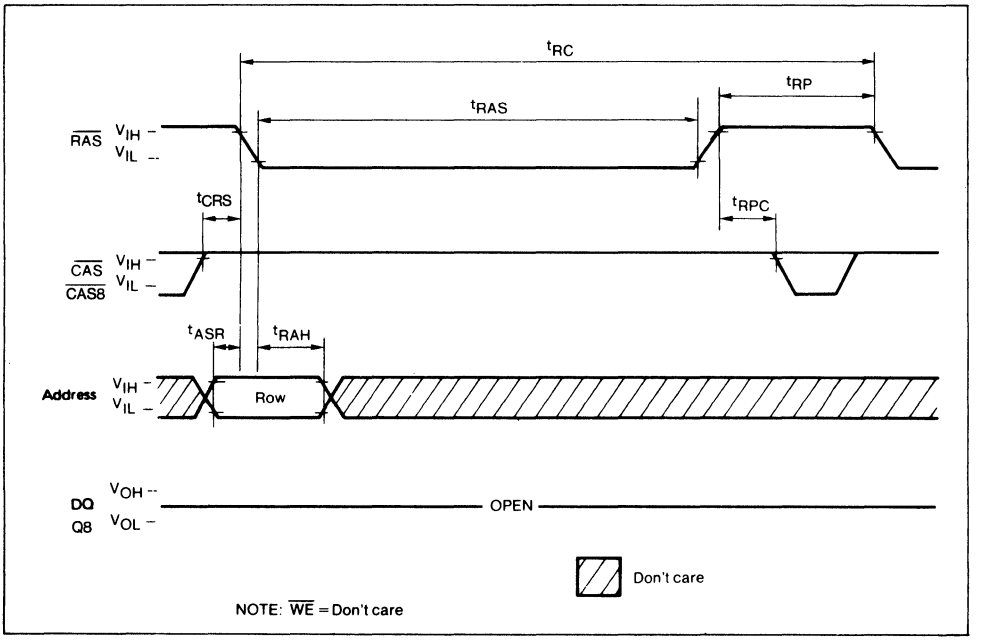
PAGE MODE READ CYCLE



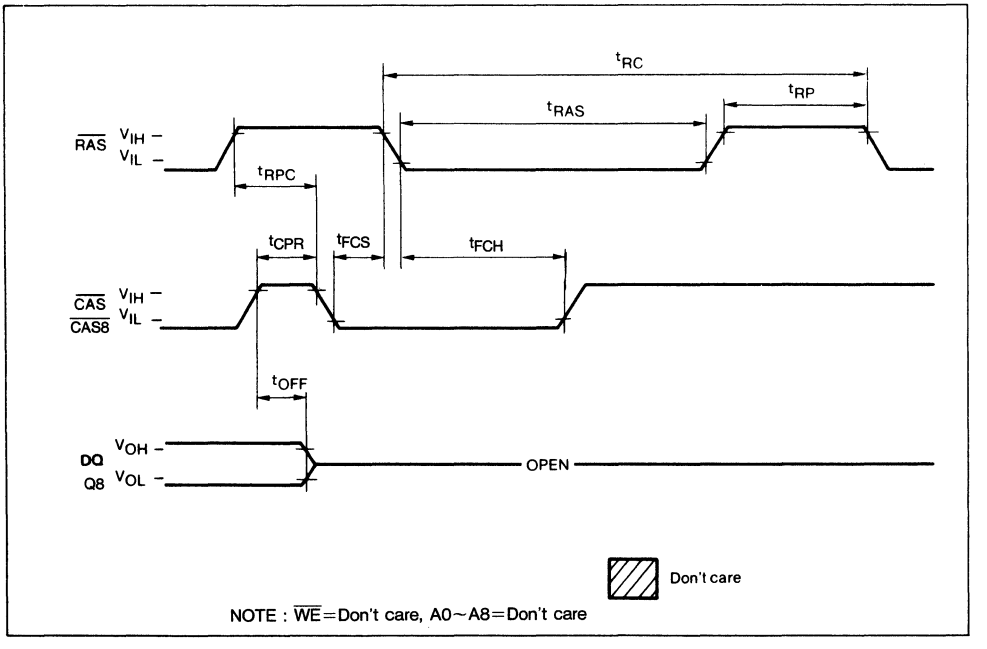
PAGE MODE CYCLE (EARLY WRITE)



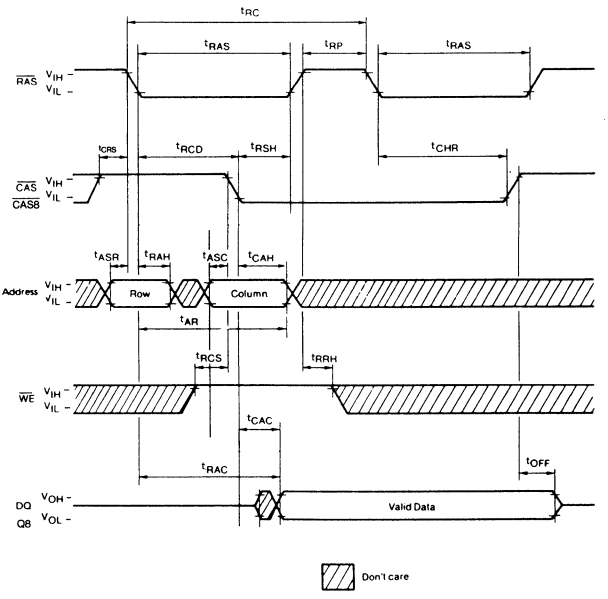
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



MSC2316-xxYS9

262,144 BY 9 BIT DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2316-xxYS9 is a fully decoded, 262,144 word × 9 bit CMOS dynamic random access memory composed of nine 256K DRAMs in plastic leaded chip carrier (MSM51C256JS). The mounting of nine PLCCs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-in-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2316-xxYS9 are same as the original MSM51C256JS; each timing requirements are noncritical, and power supply tolerance is very wide.

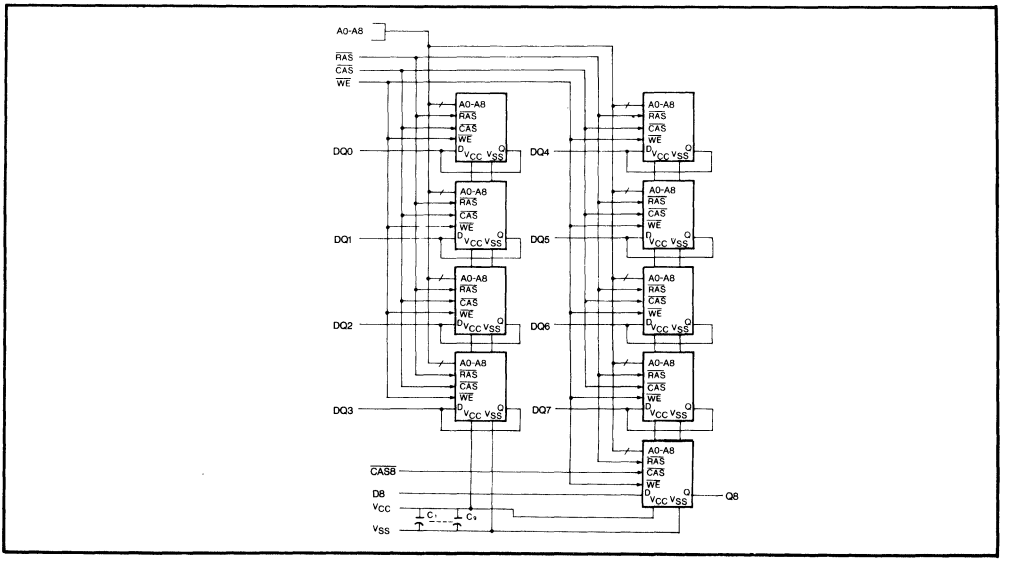
FEATURES

- 262,144 word × 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2316-80YS9	80ns	40ns	20ns	160ns	2970mW	124mW (MOS level)
MSC2316-10YS9	100ns	50ns	25ns	190ns	2475mW	

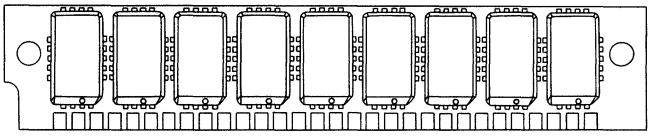
- Single + 5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 256 cycles/4 ms
- Common $\overline{CAS}$ control for eight common Data-in and Data-out lines.
- Separate $\overline{CAS}$ control for one separate pair of Data-in and Data-out lines.
- Fast Page Mode capability

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

MSC2316-xxYS9



1 30

PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	Q8
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS8}$
9	VSS	19	NC	29	D8
10	DQ2	20	DQ5	30	Vcc

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ 125	°C
Power dissipation	P_D	4	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	V_{CC}+1.0	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0~+70°C)

Parameter	Symbol	Condition		MSC2316-80YS9 Min.	MSC2316-80YS9 Max.	MSC2316-10YS9 Min.	MSC2316-10YS9 Max.	Unit	Note
Input Leakage Current	I_{LI}	0V≤V_{IN}≤V_{CC}+1V All other pins not under test=0V		−90	90	−90	90	μA	
Output Leakage Current	I_{LO}	DAta out is disable 0V≤V_{OUT}≤5.5V		−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA		2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA		—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$ cycling, t_{RC}=min		—	540	—	450	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$, $\overline{CAS8}$ =V_{IH}	TTL	—	31.5	—	31.5	mA	
			MOS	—	22.5	—	22.5	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$=V_{IH} t_{RC}=min		—	540	—	450	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.		—	540	—	450	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$, $\overline{CAS8}$ cycling t_{PC}=min.		—	360	—	315	mA	1, 3

Note* : 1. I_{CC} in dependent on out put loading and cycle rates.
Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 – A8)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ0 – DQ7)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS8}$)	C_{IN3}	5	10	pF
Input Capacitance (D8)	C_{IN4}	4	10	pF
Output Capacitance (Q8)	C_{OUT}	4	15	pF

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 ~ +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2316-80YS9		MSC2316-10YS9		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	4	–	4	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	ns	
Fast page mode cycle time	t_{PC}	55	–	55	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4, 5, 6
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	50	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	30	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	

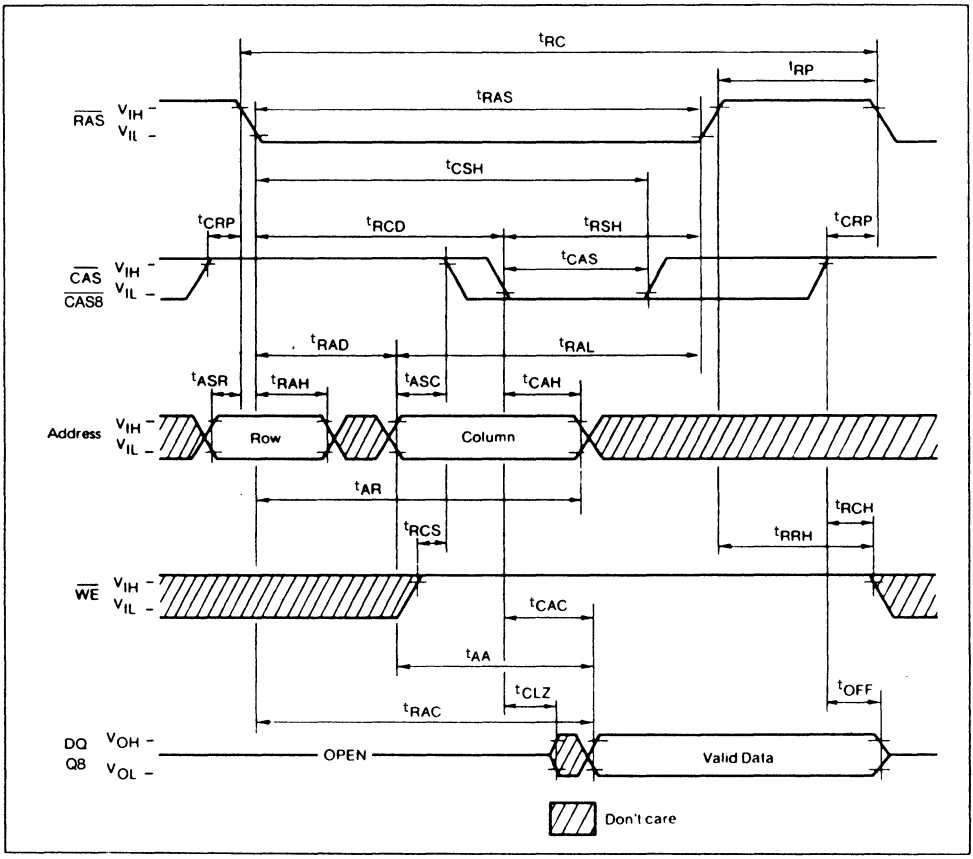
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2316-80YS9		MSC2316-10YS9		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	ns	

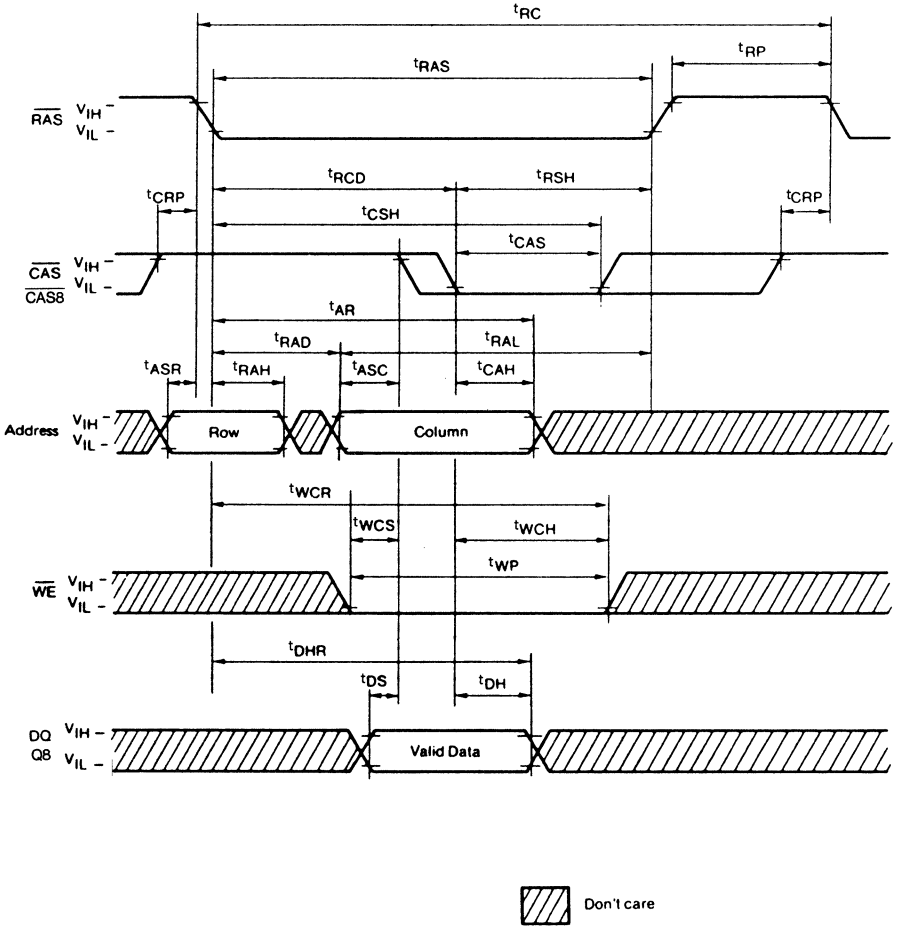
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example : $\overline{RAS}$ only refresh cycle) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD}(max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

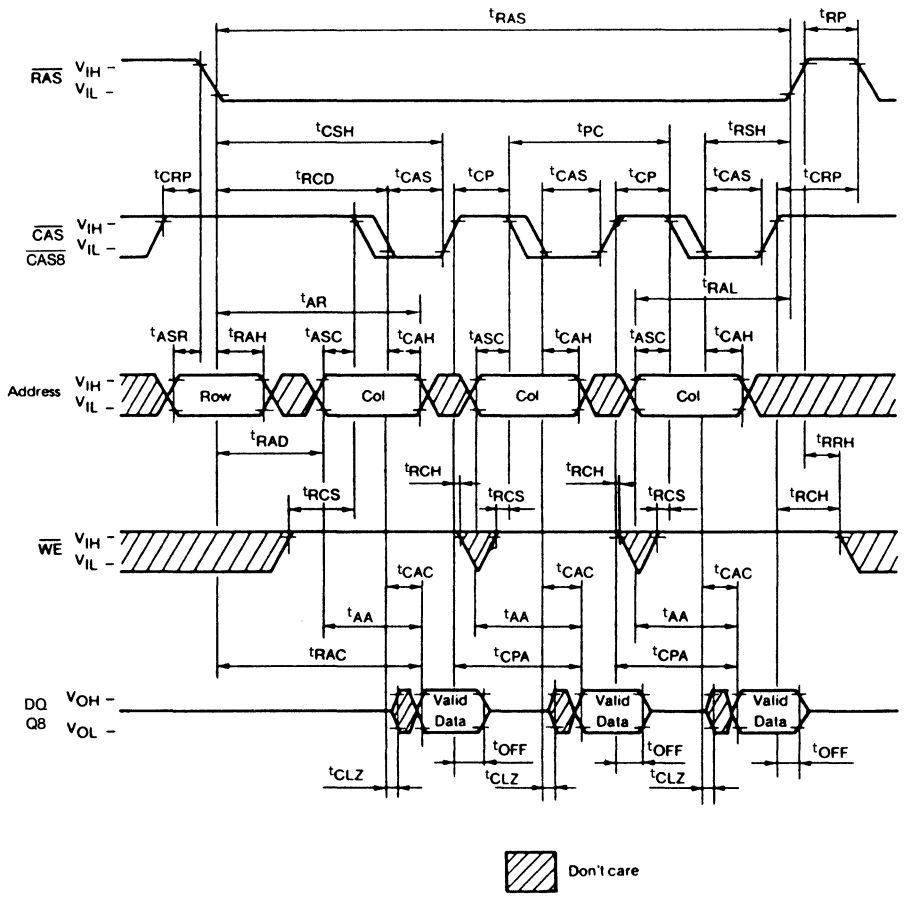
READ CYCLE


tRC
tRP
tRAS
RAS VIH VIL
tCSH
tCRP
tRCD
tRSH
tCRP
CAS VIH VIL
CAS8
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address VIH VIL
Row
Column
tAR
tRCS
tRCH
tRRH
WE VIH VIL
tCAC
tAA
tCLZ
tOFF
tRAC
DQ VOH
Q8 VOL
OPEN
Valid Data
Don't care

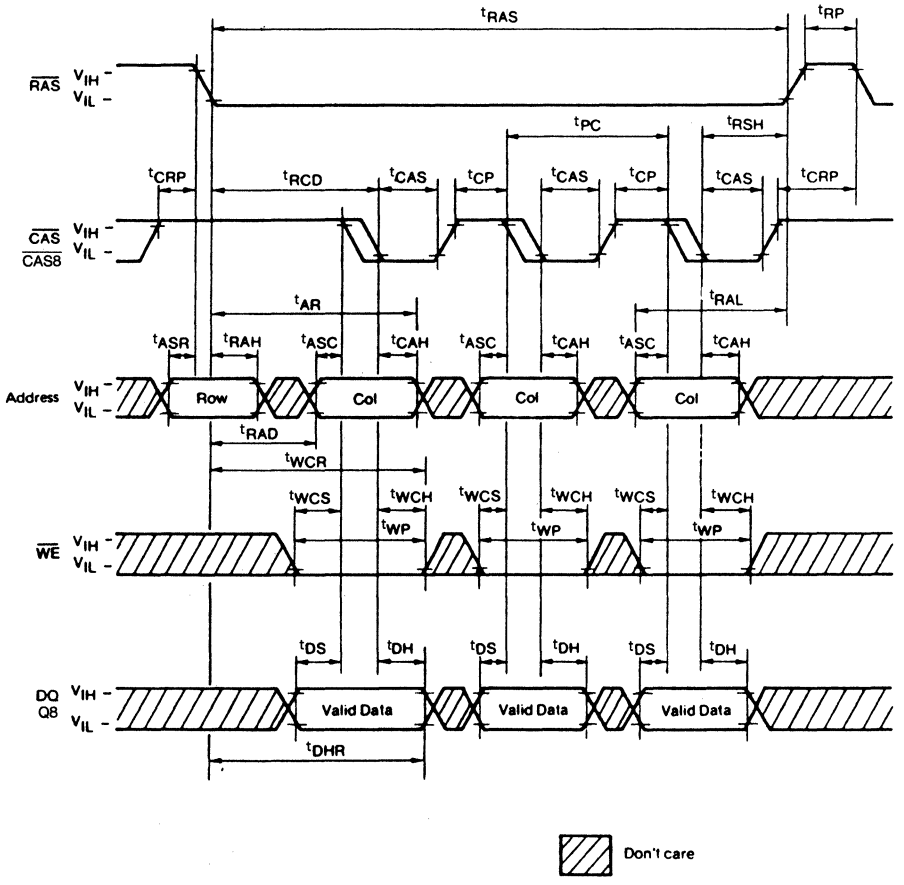
WRITE CYCLE (EARLY WRITE)



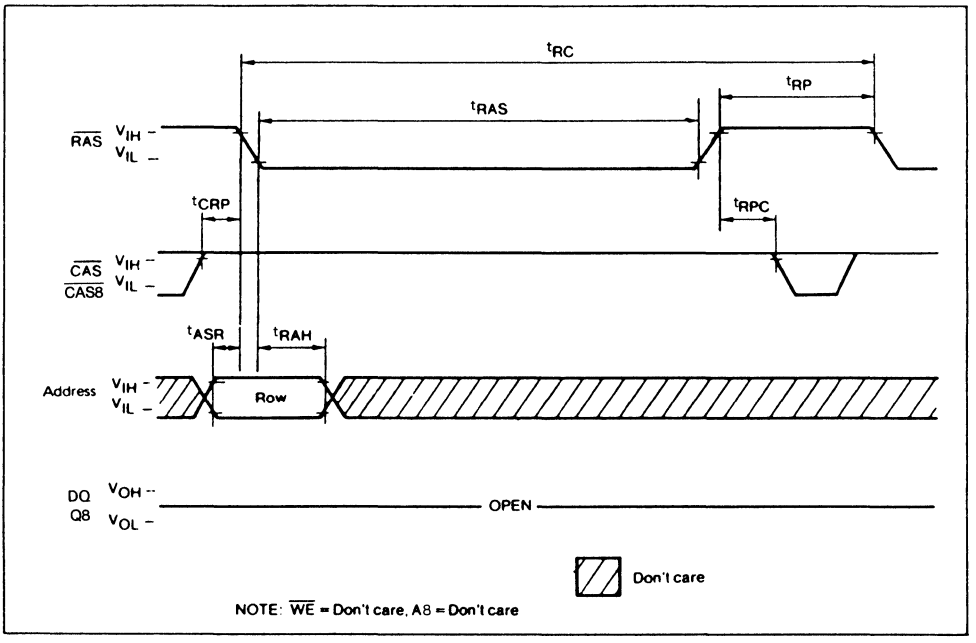
FAST PAGE MODE READ CYCLE



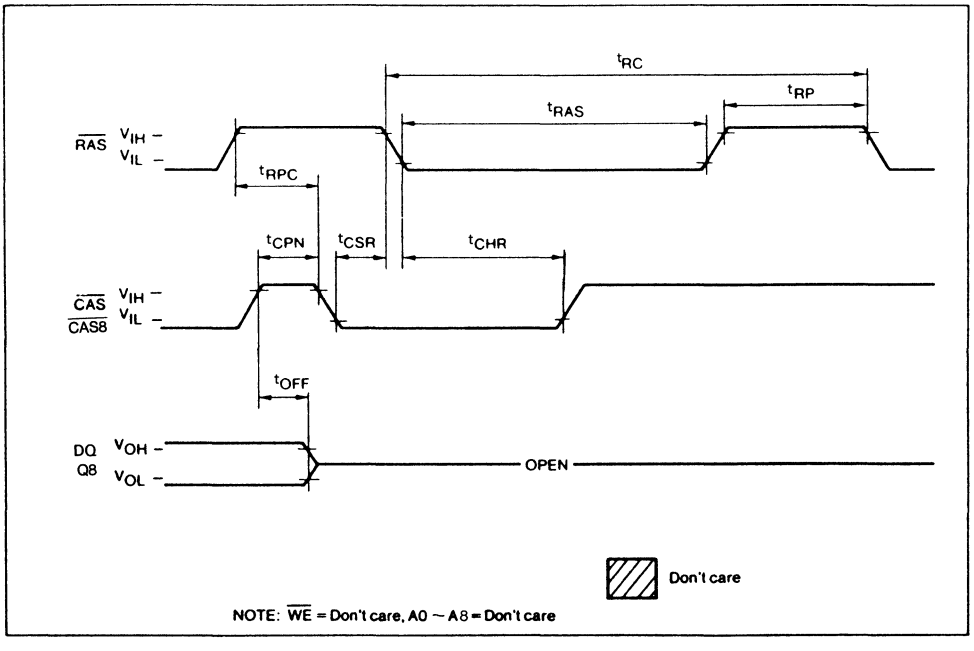
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



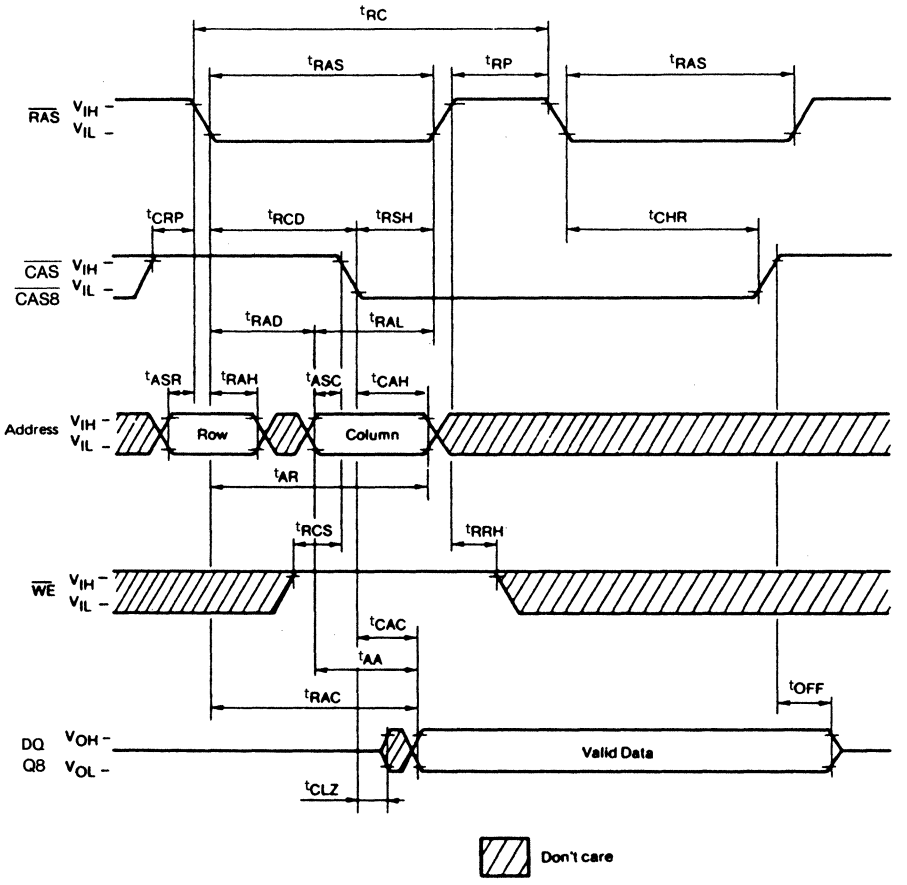
$\overline{RAS}$ ONLY REFRESH CYCLE



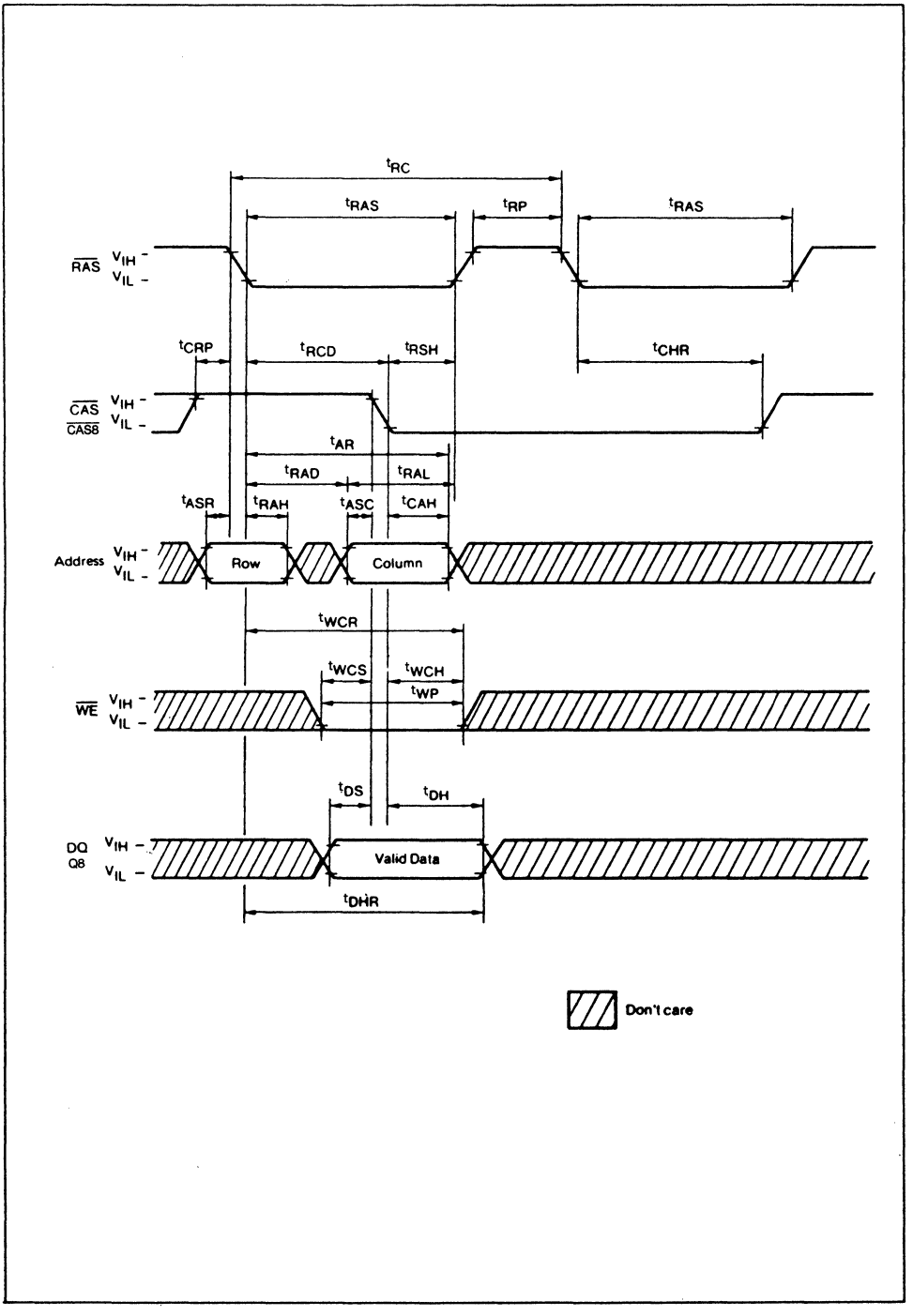
$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



MSC2331A-xxYS3/KS3

262,144 Word BY 9 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2331A-xxYS3/KS3 is a fully decoded, 262,144 word × 9 bit CMOS dynamic random access memory composed of two 1 Mb DRAMs in SOJ (MSM514256AJS) and one 256Kb DRAM in PLCC (MSM51C256JS). The mounting of two SOJs and one PLCC together with three 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-in-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2331A-xxYS3/KS3 are same as the original MSM514256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

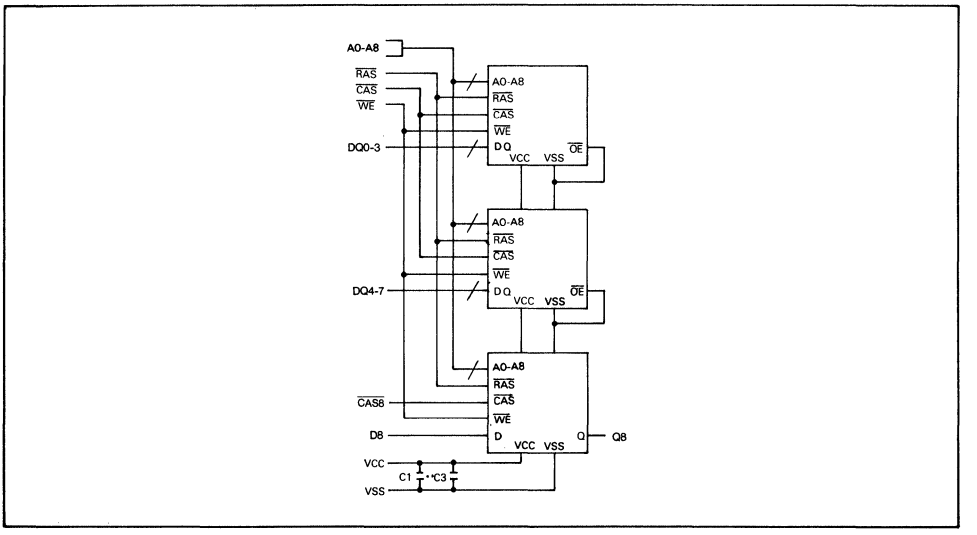
FEATURES

- 262,144 word × 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2331A-80YS3/KS3	80ns	40ns	20ns	160ns	1155mW	25mW (MOS level)
MSC2331A-10YS3/KS3	100ns	50ns	25ns	190ns	990mW	

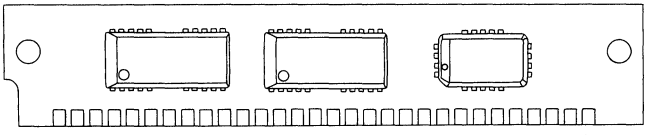
- Single + 5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms
- Common $\overline{CAS}$ control for eight common Data-in and Data-out lines.
- Separate $\overline{CAS}$ control for one separate pair of Data-in and Data-out lines.

FUNCTIONAL BLOCK DIAGRAM

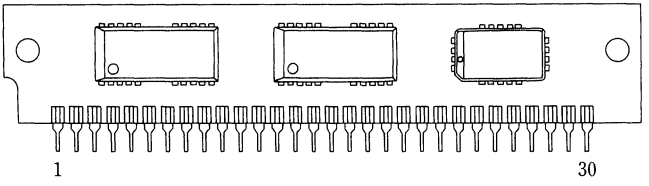


PIN CONFIGURATION

MSC2331A-xxYS3



MSC2331A-xxKS3



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	Q8
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS8}$
9	VSS	19	NC	29	D8
10	DQ2	20	DQ5	30	Vcc

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ 125	°C
Power dissipation	P_D	4	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0~+70°C)

Parameter	Symbol	Condition		MSC2331A-80YS3/KS3 Min.	MSC2331A-80YS3/KS3 Max.	MSC2331A-10YS3/KS3 Min.	MSC2331A-10YS3/KS3 Max.	Unit	Note
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.5V : All other pins not under test=0V		−30	30	−30	30	μA	
Output Leakage Current	I_{LO}	Data out is disable 0V≤V_{OUT}≤5.5V		−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA		2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA		—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$ cycling, t_{RC}=min		—	210	—	180	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$, $\overline{CAS8}$ =V_{IH}	TTL	—	7.5	—	7.5	mA	
			MOS	—	4.5	—	4.5	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$=V_{IH} t_{RC}=min		—	210	—	180	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.		—	210	—	180	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$, $\overline{CAS8}$ cycling t_{PC}=min.		—	170	—	155	mA	1, 3

Note : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance (A0 – A8)	C_{IN1}	40	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	pF
Data Input/Output Capacitance (DQ0 – DQ7)	C_{DQ}	20	pF
Input Capacitance ($\overline{CAS8}$)	C_{IN3}	10	pF
Input Capacitance (D8)	C_{IN4}	10	pF
Output Capacitance (Q8)	C_{OUT}	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 ~ +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2331A-80YS3/KS3		MSC2331A-10YS3/KS3		Unit	Note
		MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	ns	
Fast page mode cycle time	t_{PC}	50	–	55	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4, 5, 6
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	50	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	

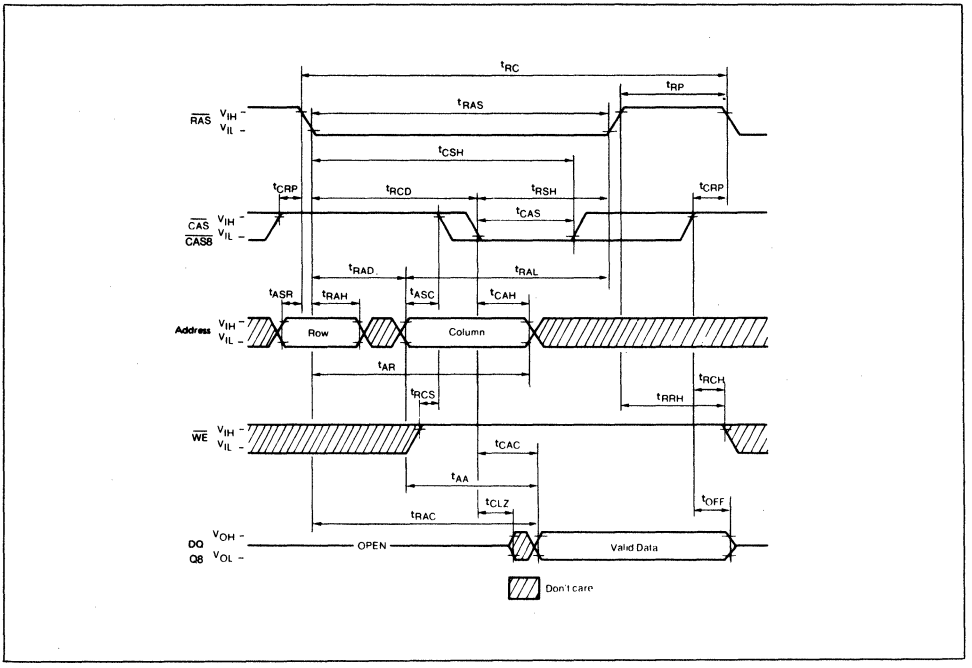
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2331A-80YS3/KS3		MSC2331A-10YS3/KS3		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	60	—	75	—	ns	
Write command set-up time	t_{WCS}	0	—	0	—	ns	
Write command hold time	t_{WCH}	15	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	ns	
Data-in hold time	t_{DH}	15	—	20	—	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	—	75	—	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	—	30	—	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	ns	

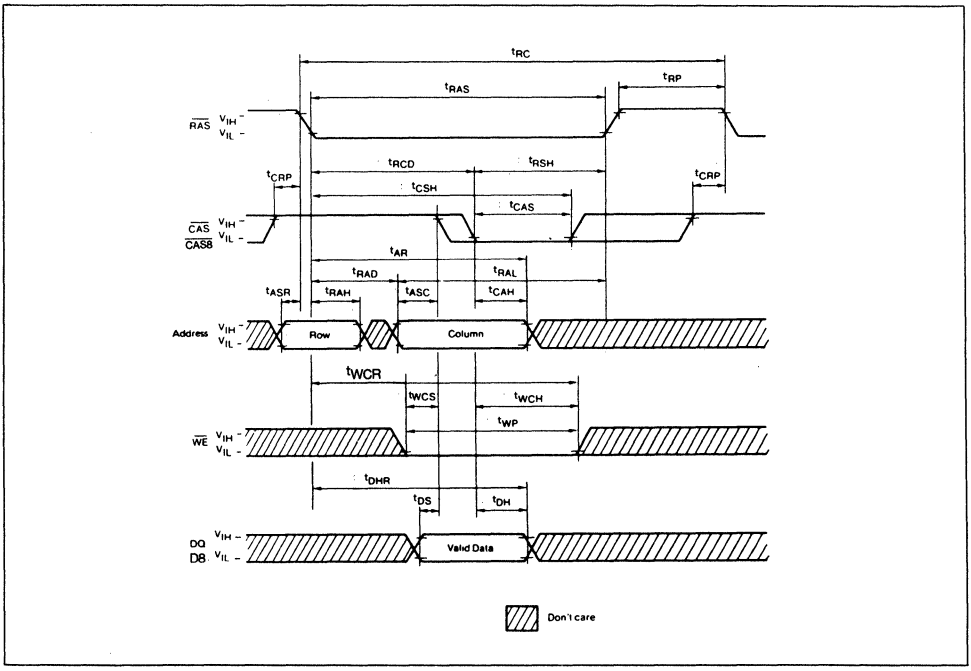
Notes:

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example : $\overline{RAS}$ only Refresh cycle) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

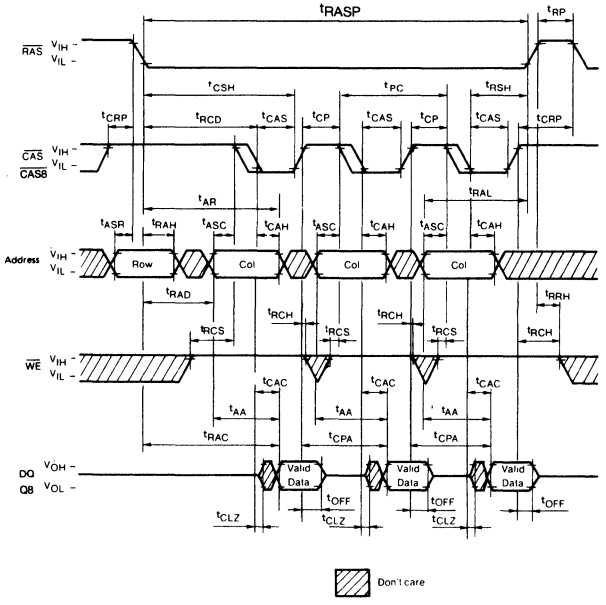
READ CYCLE



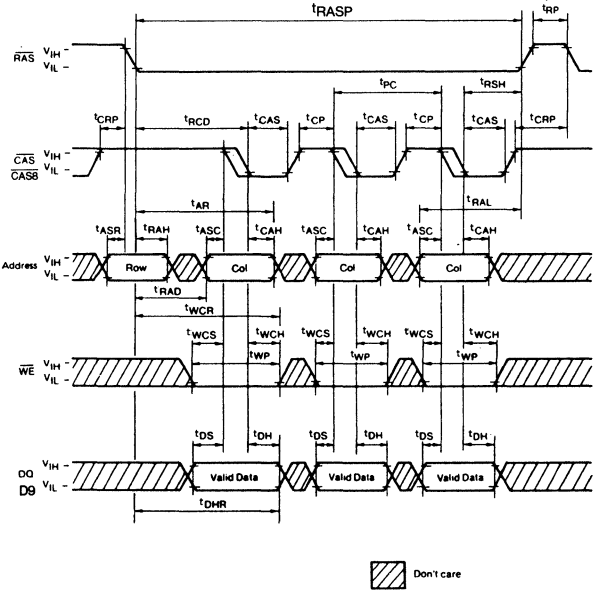
WRITE CYCLE(EARLY WRITE)



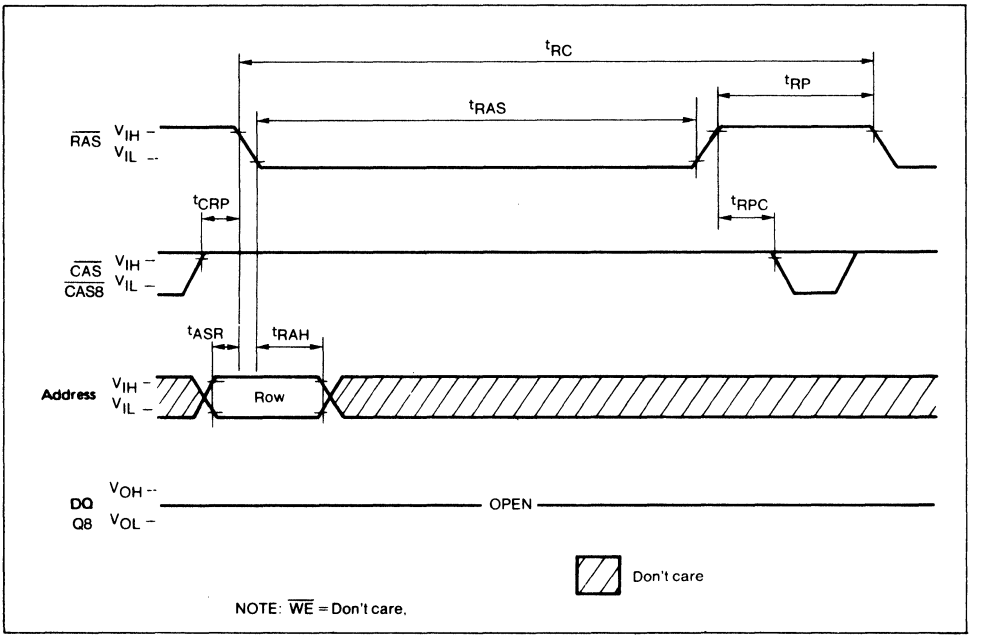
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)

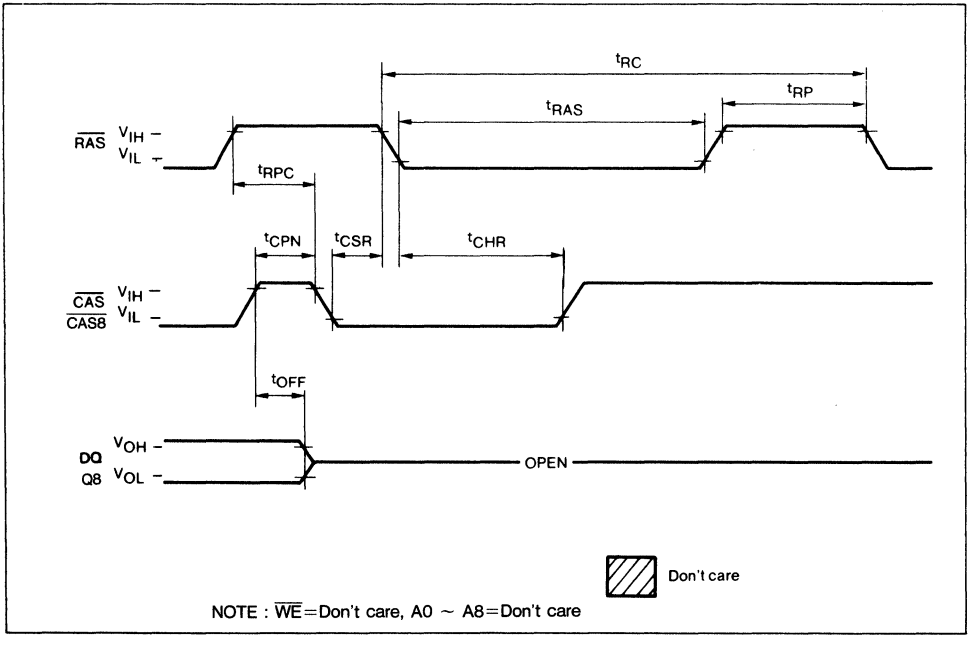


$\overline{RAS}$ ONLY REFRESH CYCLE



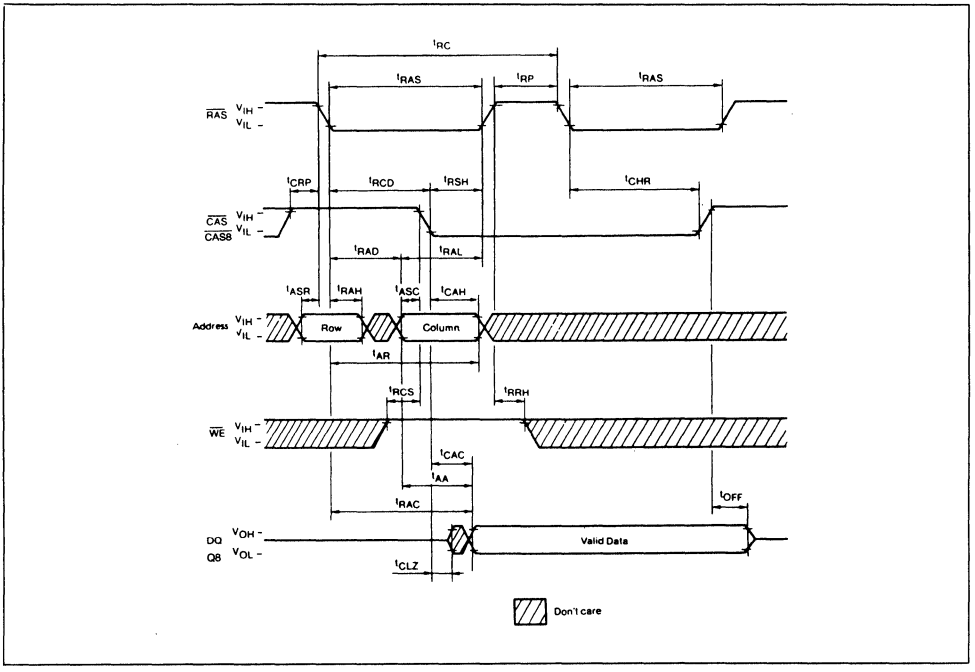
NOTE: $\overline{WE}$ = Don't care.

$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

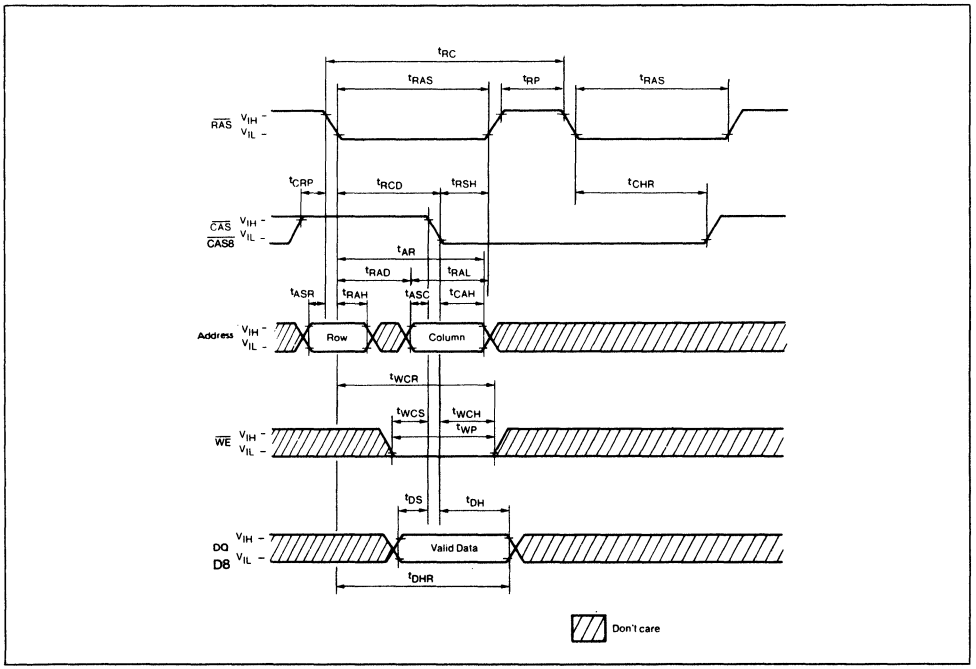


NOTE : $\overline{WE}$=Don't care, A0 ~ A8=Don't care

HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



MSC2312A-xxYS9/KS9

1,048,576 Word BY 9 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2312A-xxYS9/KS9 is a fully decoded, 1,048,576 word × 9 bit CMOS dynamic random access memory composed of nine 1Mb DRAMs in SOJ (MSM511000AJS). The mounting of nine SOJs together with nine 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2312A-xxYS9/KS9 are same as the original MSM511000AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

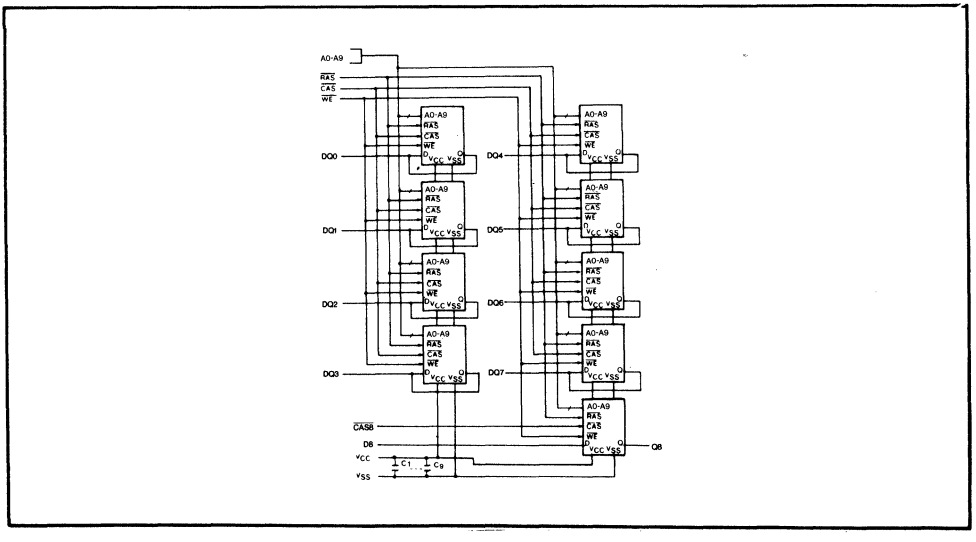
FEATURES

- 1,048,576 word × 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2312A-70YS9/KS9	70ns	35ns	20ns	140ns	4208mW	50mW (MOS level)
MSC2312A-80YS9/KS9	80ns	40ns	20ns	160ns	3713mW	
MSC2312A-10YS9/KS9	100ns	50ns	25ns	190ns	3218mW	

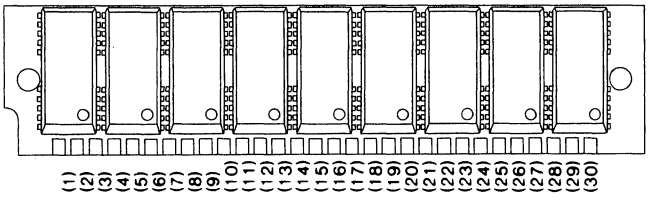
- Single + 5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms
- Common $\overline{CAS}$ Control for eight Common Data-in and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-in and Data-Out Lines

FUNCTIONAL BLOCK DIAGRAM

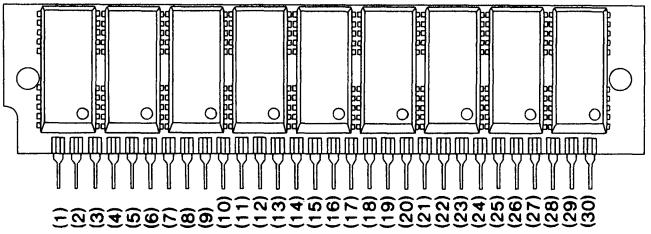


PIN CONFIGURATION

MSC2312A-xxYS9



MSC2312A-xxKS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	Vcc	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	Q8
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	$\overline{CAS8}$
9	VSS	19	NC	29	D8
10	DQ2	20	DQ5	30	Vcc

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ 125	°C
Power dissipation	P_D	9	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±10%, Ta=0~+70°C)

Parameter	Symbol	Condition	MSC2312A-70YS9/KS9 Min.	MSC2312A-70YS9/KS9 Max.	MSC2312A-80YS9/KS9 Min.	MSC2312A-80YS9/KS9 Max.	MSC2312A-10YS9/KS9 Min.	MSC2312A-10YS9/KS9 Max.	Unit	Note
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.5V : All other pins not under test=0V	−90	90	−90	90	−90	90	μA	
Output Leakage Current	I_{LO}	Data out is disable 0V≤V_{OUT}≤5.5V	−10	10	−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA	2.4	—	2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA	—	0.4	—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$ cycling, t_{RC}=min	—	765	—	675	—	585	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$, $\overline{CAS8}$ =V_{IH} TTL	—	18	—	18	—	18	mA	
		MOS	—	9	—	9	—	9	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$=V_{IH} t_{RC}=min	—	765	—	675	—	585	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.	—	765	—	675	—	585	mA	1
Average power supply current (Fast page)	I_{CC7}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$, $\overline{CAS8}$ cycling t_{PC}=min.	—	630	—	540	—	495	mA	1, 3

Note : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 — A9)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ0 — DQ7)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS8}$)	C_{IN3}	5	10	pF
Input Capacitance (D8)	C_{IN4}	4	10	pF
Output Capacitance (Q8)	C_{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ± 10%, Ta = 0 ~ +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2312A-70YS9/KS9		MSC2312A-80YS9/KS9		MSC2312A-10YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	–	8	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	140	–	160	–	190	–	ns	
Fast page mode cycle time	t_{PC}	45	–	50	–	55	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	70	–	80	–	100	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	20	–	25	ns	4.5
Access time from column address	t_{AA}	–	35	–	40	–	50	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	40	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	60	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10K	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	–	10	–	10	–	ns
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	55	–	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	–	40	–	50	–	ns	

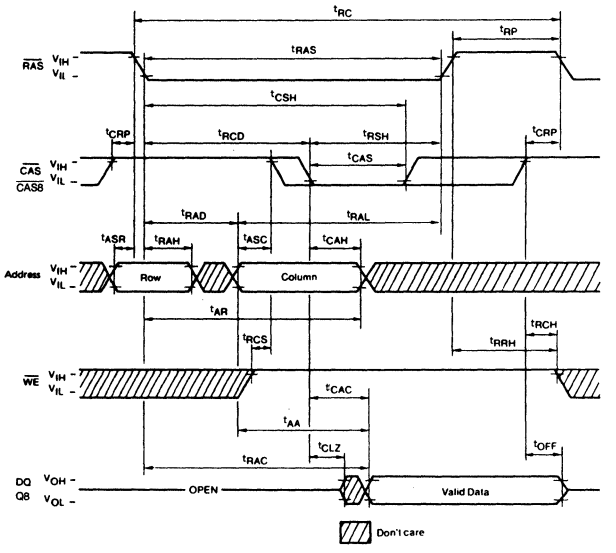
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2312A-70YS9/KS9		MSC2312A-80YS9/KS9		MSC2312A-10YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	55	—	60	—	75	—	ns	
Write command se-up time	t_{WCS}	0	—	0	—	0	—	ns	
Write comman hold time	t_{WCH}	15	—	15	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	15	—	20	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	0	—	ns	
Data-in hold time	t_{DH}	15	—	15	—	20	—	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	55	—	60	—	75	—	ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	—	30	—	30	—	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	10	—	15	—	ns	

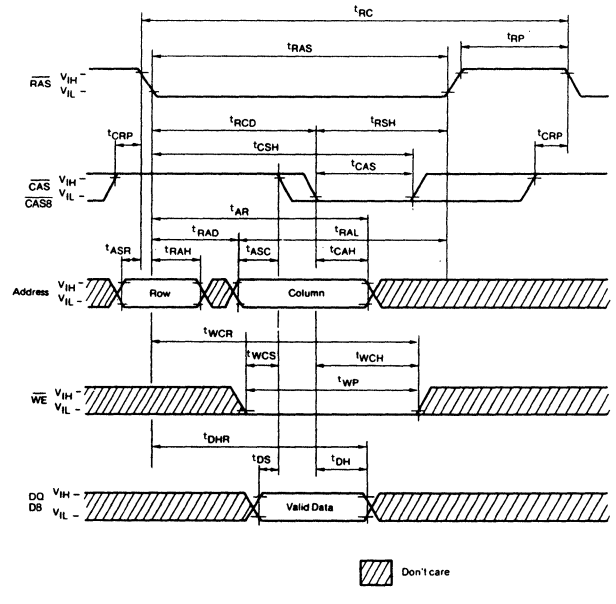
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example : $\overline{RAS}$ only refresh cycle) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL loads and 100pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

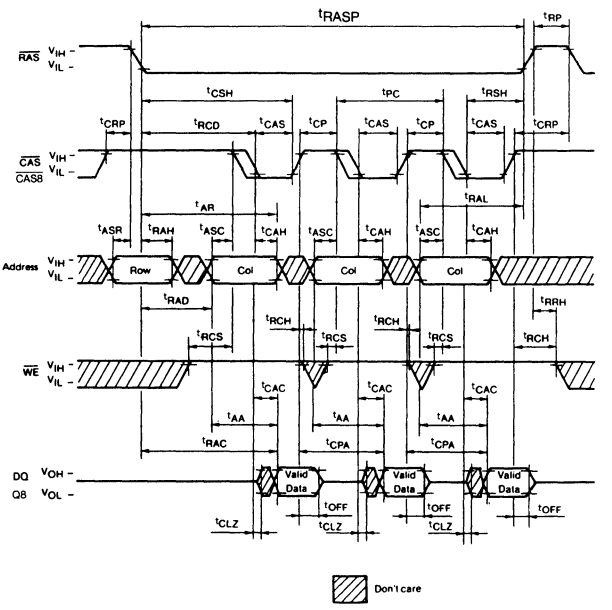
READ CYCLE



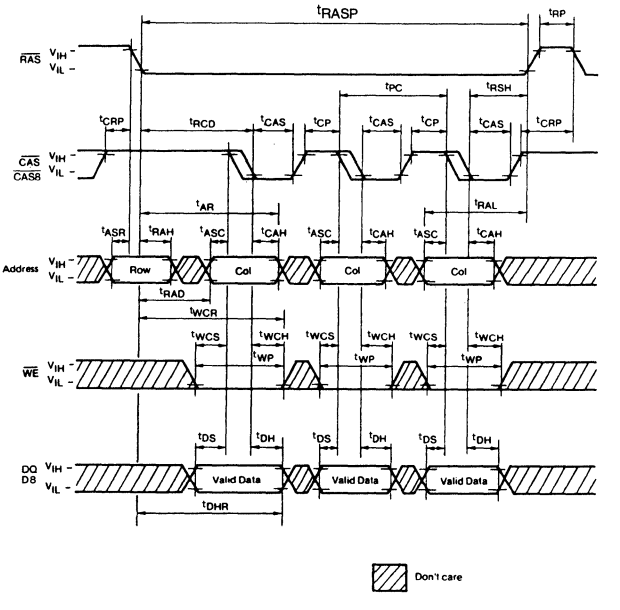
WRITE CYCLE(EARLY WRITE)



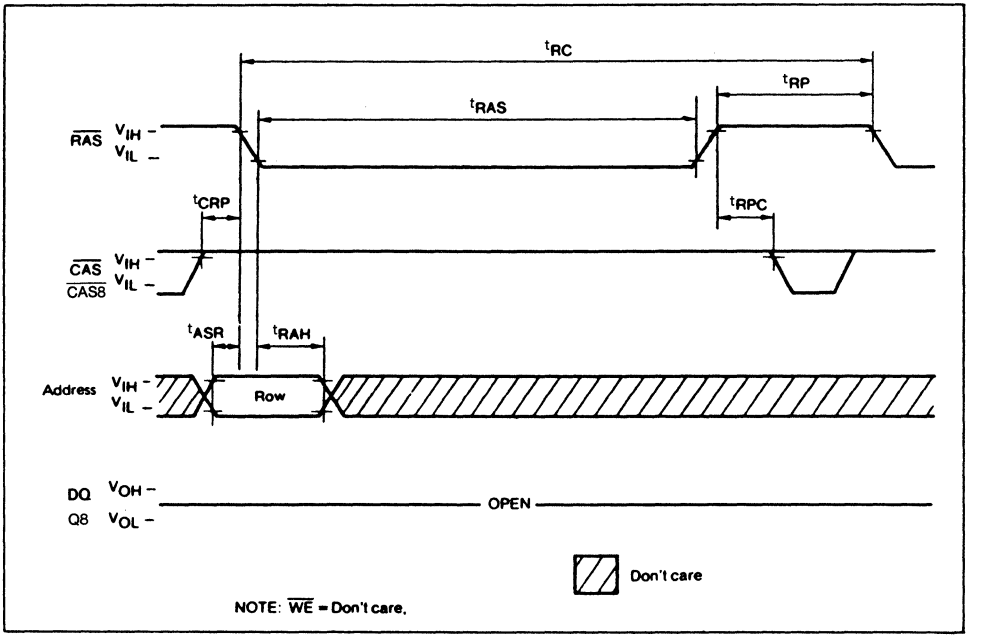
FAST PAGE MODE READ CYCLE



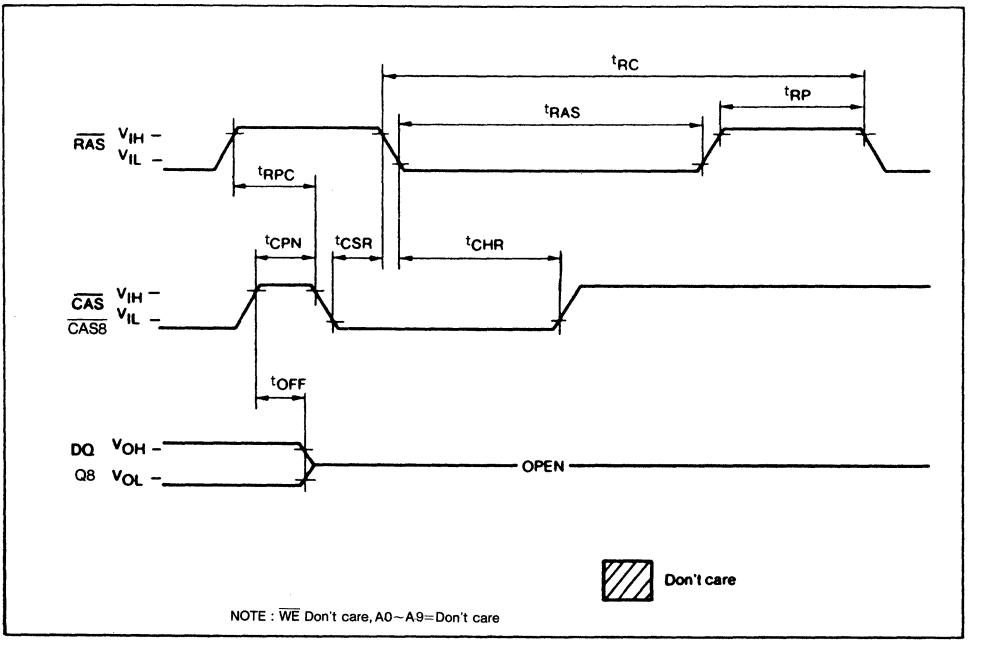
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



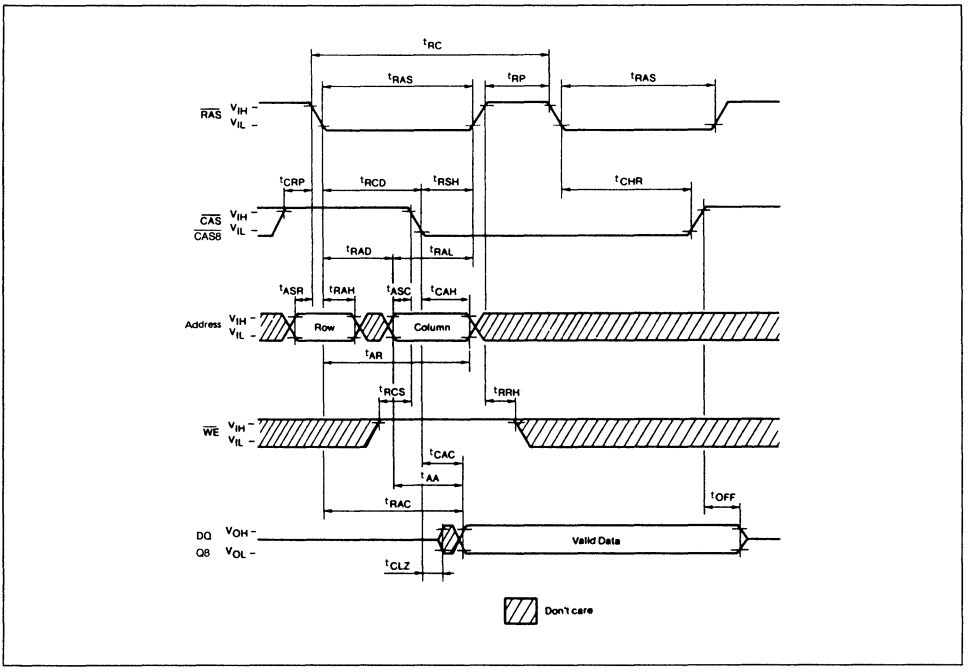
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



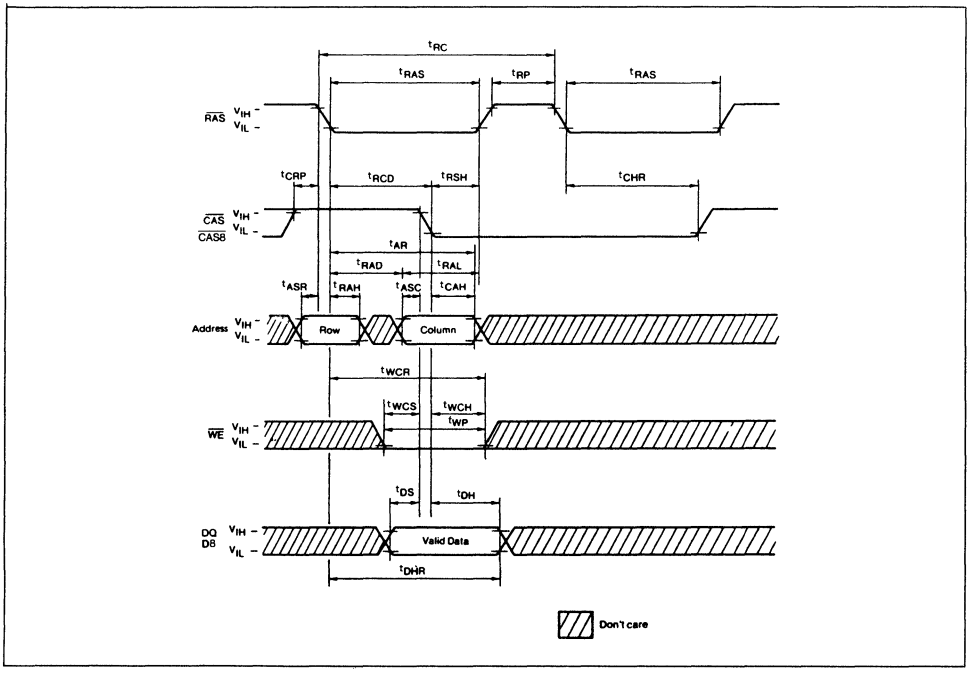
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



OKI semiconductor
MSC2359-xxYS3

PRELIMINARY

1,048,576 Word x 9 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2359-xxYS3 is a fully decoded, 1,048,576 word by 9 bit CMOS dynamic random access memory composed of two 4Mb DRAMs in SOJ (MSM514400JS) and one 1Mb DRAM in SOJ (MSM511000AJS). The mounting of three SOJs together with three 0.2 µF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2359-xxYS3 are same as the original MSM514400JS; each timing requirements are noncritical, and power supply tolerance is very wide.

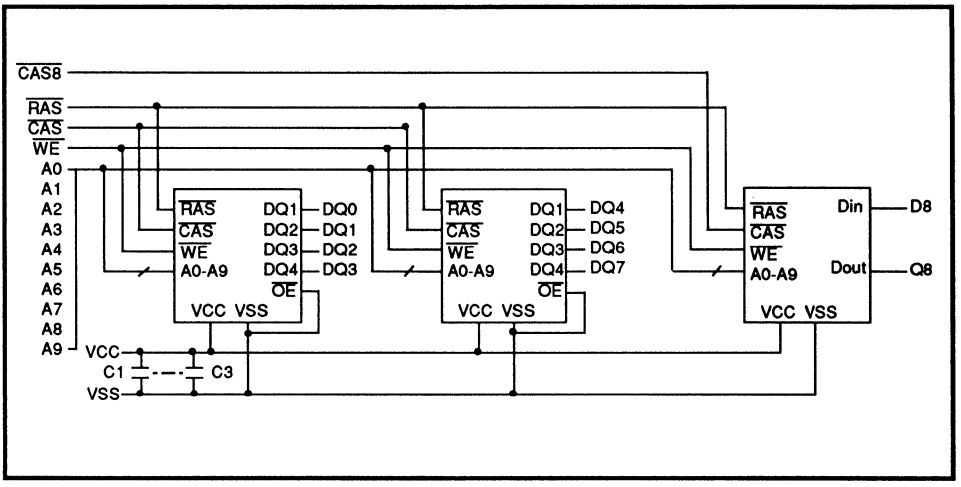
FEATURES

- 1,048,576 word x 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (MAX)	Standby (MAX)
MSC2359-80YS3	80 ns	40 ns	20 ns	160 ns	1403 mW	17mW (MOS level)
MSC2359-10YS3	100 ns	50 ns	25 ns	190 ns	1238 mW	

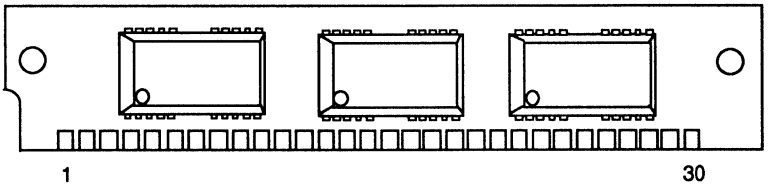
- Single +5V supply, ±10% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- Common $\overline{CAS}$ control for eight common Data-in and Data-out lines
- Separate $\overline{CAS}$ control for one separate pair of Data-in and Data-out lines
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi-bit test mode capability

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

MSC2359-xxYS3



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VCC	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	N. C.
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	$\overline{Q8}$
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	$\overline{CAS8}$
9	VSS	19	N. C.	29	D8
10	DQ2	20	DQ5	30	VCC

OKI semiconductor
MSC2340-xxYS9/KS9

4,194,304 Word x 9 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2340-xxYS9/KS9 is a fully decoded, 4,194,304 word by 9 bit CMOS dynamic random access memory composed of nine 4Mb DRAMs in SOJ (MSM514100JS). The mounting of nine SOJs together with nine 0.2µF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2340-xxYS9/KS9 are same as the original MSM514100JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

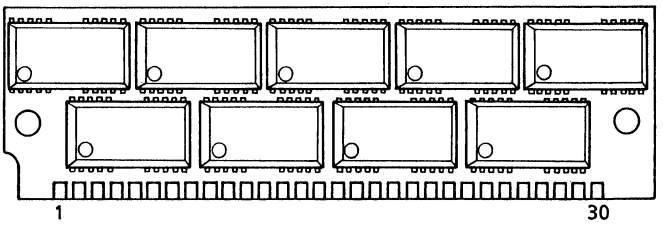
- 4,194,304 word x 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (MAX)	Standby (MAX)
MSC2340-80YS9/KS9	80 ns	40 ns	20 ns	160 ns	4455 mW	50 mW (MOS level)
MSC2340-10YS9/KS9	100 ns	50 ns	25 ns	190 ns	3960 mW	

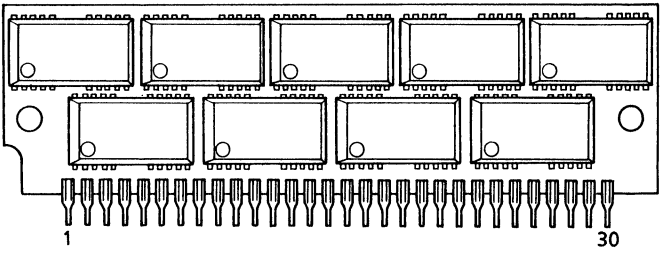
- Single + 5 V supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- Common $\overline{CAS}$ control for eight common Data-in and Data-out lines
- Separate $\overline{CAS}$ control for one separate pair of Data-in and Data-out lines
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi-bit test mode capability

PIN CONFIGURATION

MSC2340-xxYS9

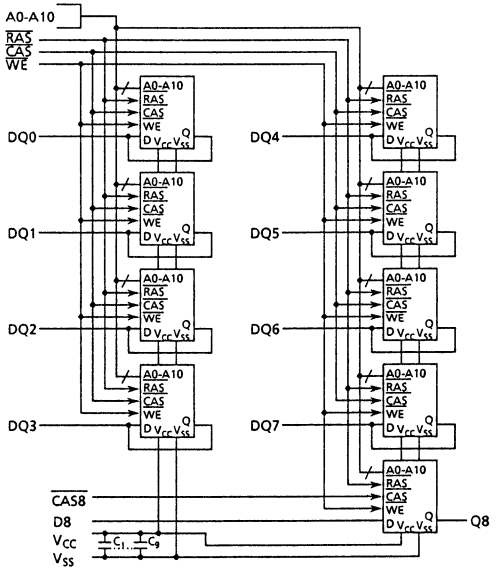


MSC2340-xxKS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	6	DQ1	11	A4	16	DQ4	21	$\overline{WE}$	26	$\overline{Q8}$
2	$\overline{CAS}$	7	A2	12	A5	17	A8	22	VSS	27	$\overline{RAS}$
3	DQ0	8	A3	13	DQ3	18	A9	23	DQ6	28	$\overline{CAS8}$
4	A0	9	VSS	14	A6	19	A10	24	NC	29	D8
5	A1	10	DQ2	15	A7	20	DQ5	25	DQ7	30	V_{CC}

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	Ta = 25 °C	− 1.0 ~ + 7.0	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	Ta = 25 °C	− 1.0 ~ + 7.0	V
Short circuit output current	Ios	Ta = 25 °C	50	mA
Power dissipation	P_D	Ta = 25 °C	9	W
Operating temperature	Topr	−	0 ~ + 70	°C
Storage temperature	Tstg	−	− 40 ~ + 125	°C

Notes: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	MIN	TYP	MAX	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C~ + 70°C
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	−	6.5	V	
Input low voltage	V_{IL}	− 1.0	−	0.8	V	

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	TYP	MAX	Unit
Input Capacitance (A0 - A10)	C_{IN1}	55	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	55	75	pF
Data Input/Output Capacitance (DQ0 - DQ7)	C_{DQ}	12	20	pF
Input Capacitance ($\overline{CAS8}$)	C_{IN3}	7	15	pF
Input Capacitance (D8)	C_{IN4}	7	15	pF
Output Capacitance (Q8)	C_{OUT}	8	15	pF

Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 ~ + 70°C)

Parameter	Symbol	Conditions		MSC2340-80 YS9/KS9		MSC2340-10 YS9/KS9		Unit	Note
				MIN	MAX	MIN	MAX		
Input leakage current	I_{LI}	0 V ≦ V_{IN} ≦ 6.5V; all other pins not under test = 0 V		– 90	90	– 90	90	μA	
Output leakage current	I_{LO}	DQ0 - 7,Q8 = disable 0 V ≦ V_{OUT} ≦ 5.5 V		– 10	10	– 10	10	μA	
Output high voltage	V_{OH}	I_{OH} = – 5.0 mA		2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$, $\overline{CAS8}$ cycling, t_{RC} = min		–	810	–	720	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$, $\overline{CAS8}$ = V_{IH} DQ0~7, Q8 = Hz	TTL	–	18	–	18	mA	
			MOS	–	9	–	9		
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS8}$ = V_{IH} t_{RC} = min		–	810	–	720	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$, $\overline{CAS8}$ = V_{IL} DQ0~7, Q8 = enable		–	45	–	45	mA	1
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling,		–	810	–	720	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, $\overline{CAS8}$ cycling t_{PC} = min		–	720	–	630	mA	1, 3

Note: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 ~ + 70°C) Note 1, 2, 3, 9, 10

Parameter	Symbol	MSC2340-80 YS9/KS9		MSC2340-10 YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	–	190	–	ns	
Fast page mode cycle time	t_{PC}	55	–	65	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4. 5
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	50	ns	4. 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	55	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay time	t_{OFF}	0	20	0	25	ns	7
Transition time	t_T	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2340-80 YS9/KS9		MSC2340-10 YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	–	20	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	50	–	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	20	–	20	–	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	20	–	20	–	ns	

Notes: 1. An initial pause of 200μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume $t_T = 5$ ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

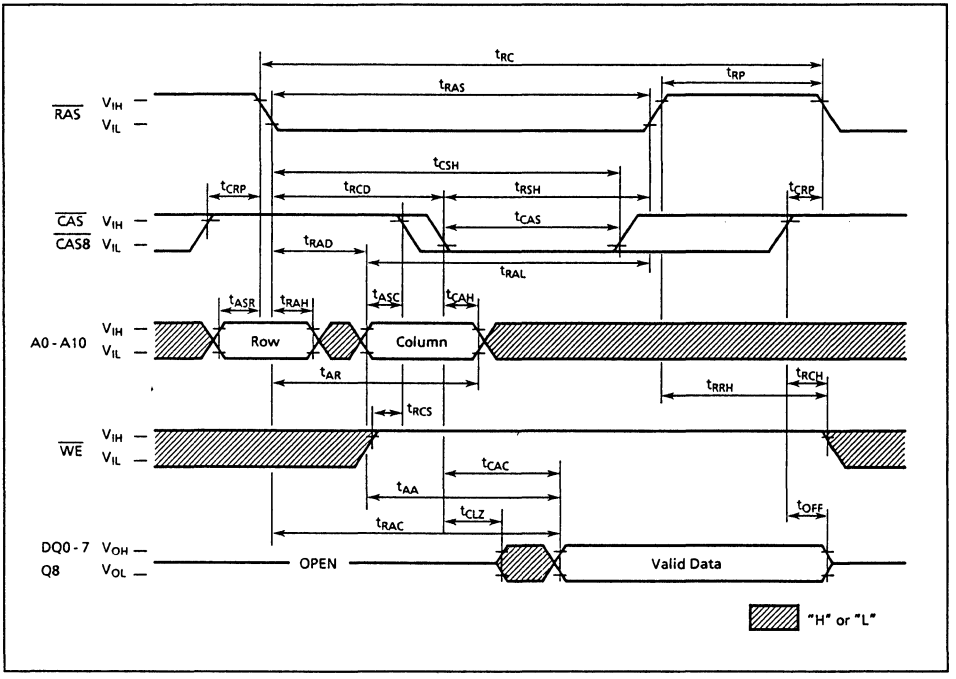
7. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

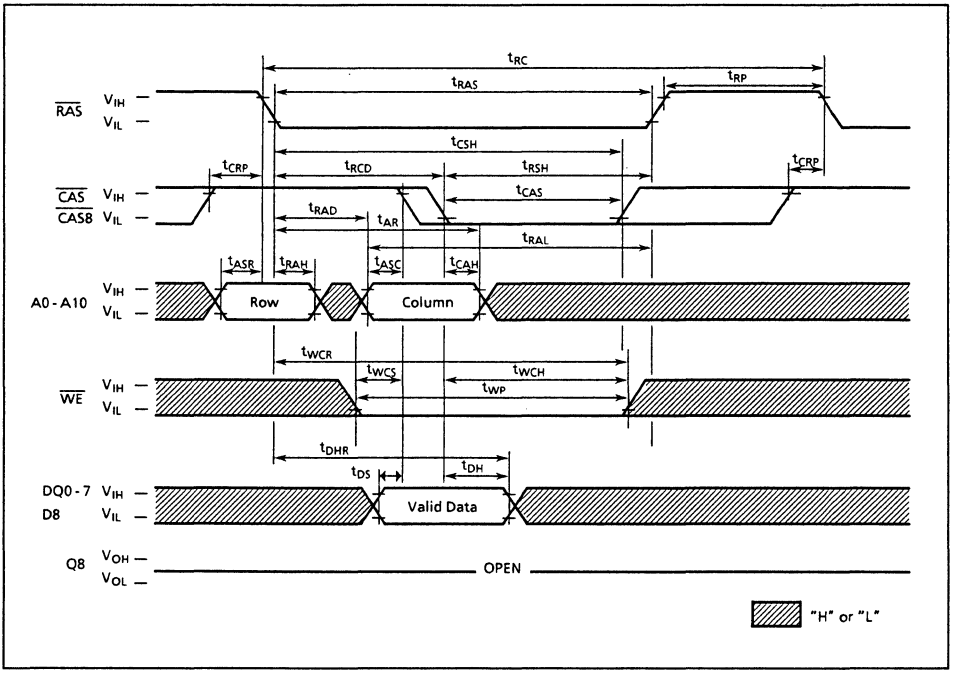
9. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect untill the exit cycle is generated.
The test mode specified in this data sheet is 8-bit parallel test function.
RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are not equal, then the data output pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

10. In a test mode read cycle, the value of an access time parameters is delayed by 5ns from the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

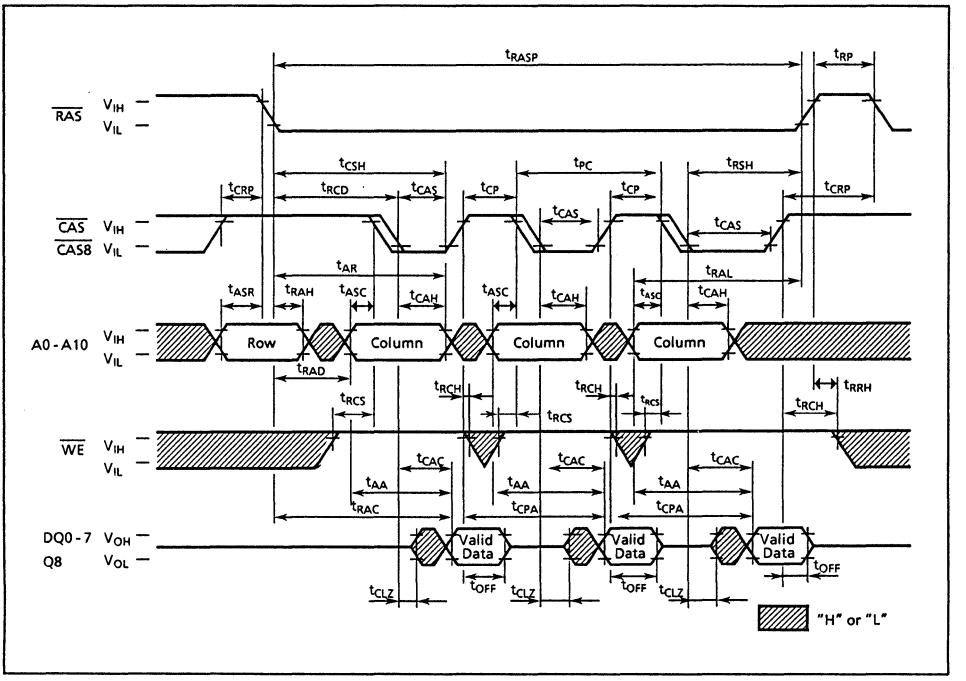
READ CYCLE



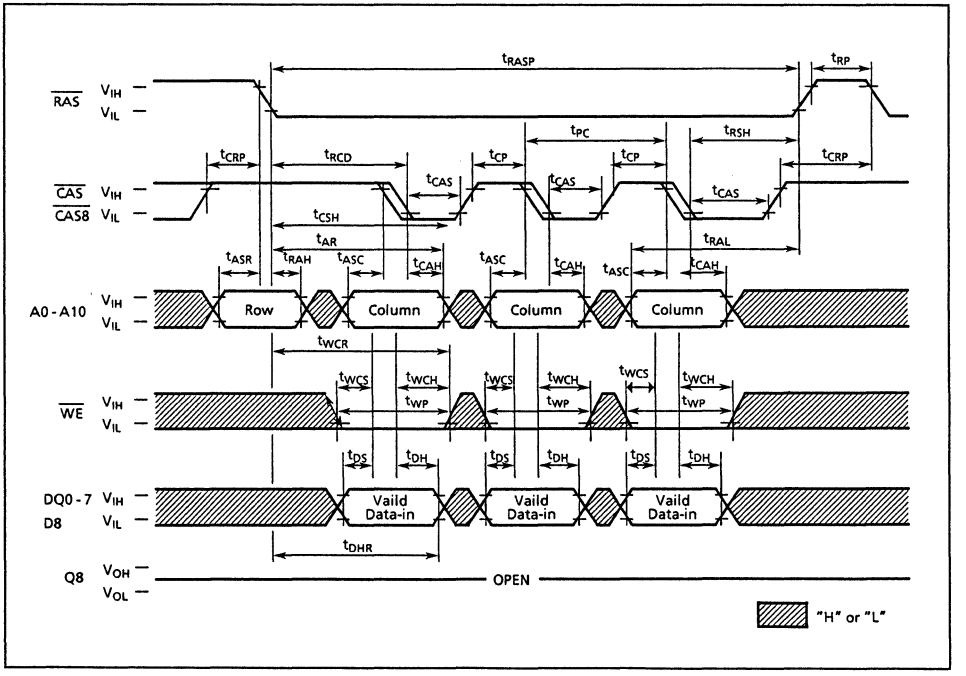
WRITE CYCLE (EARLY WRITE)



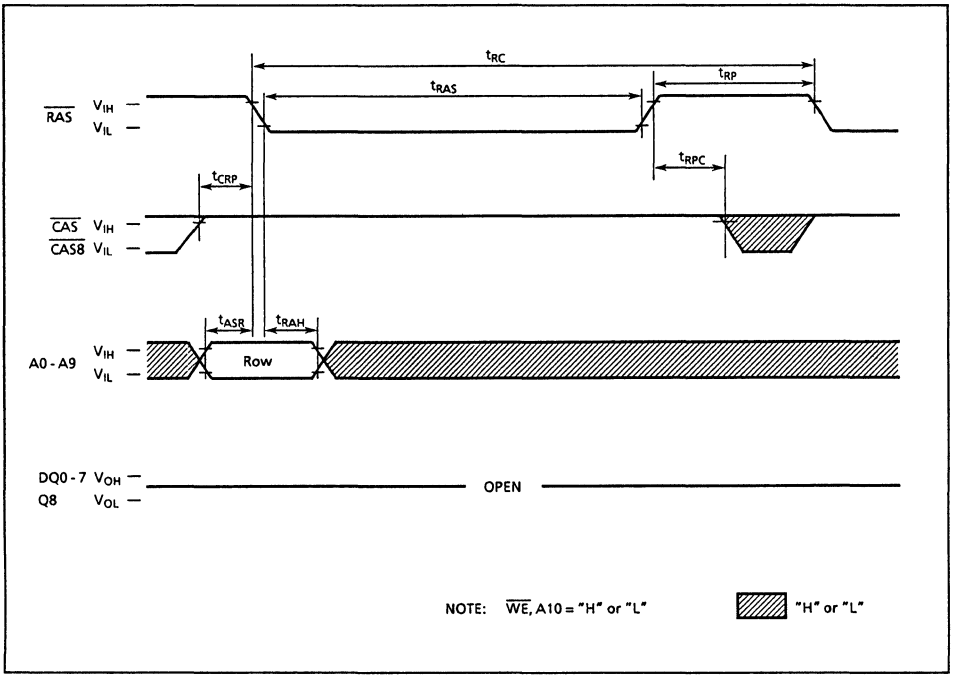
FAST PAGE MODE READ CYCLE



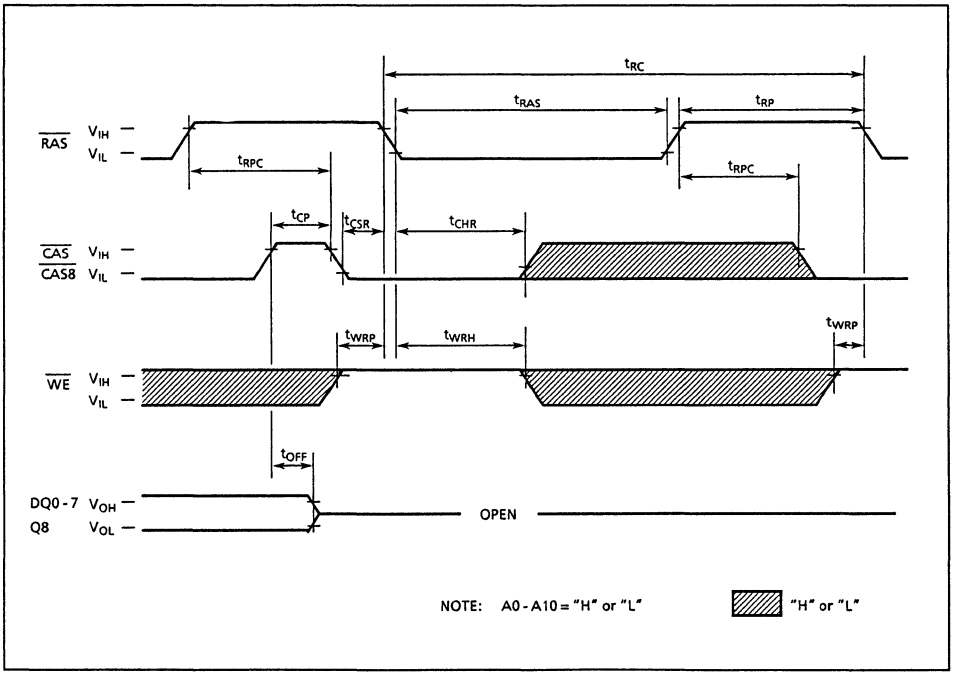
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



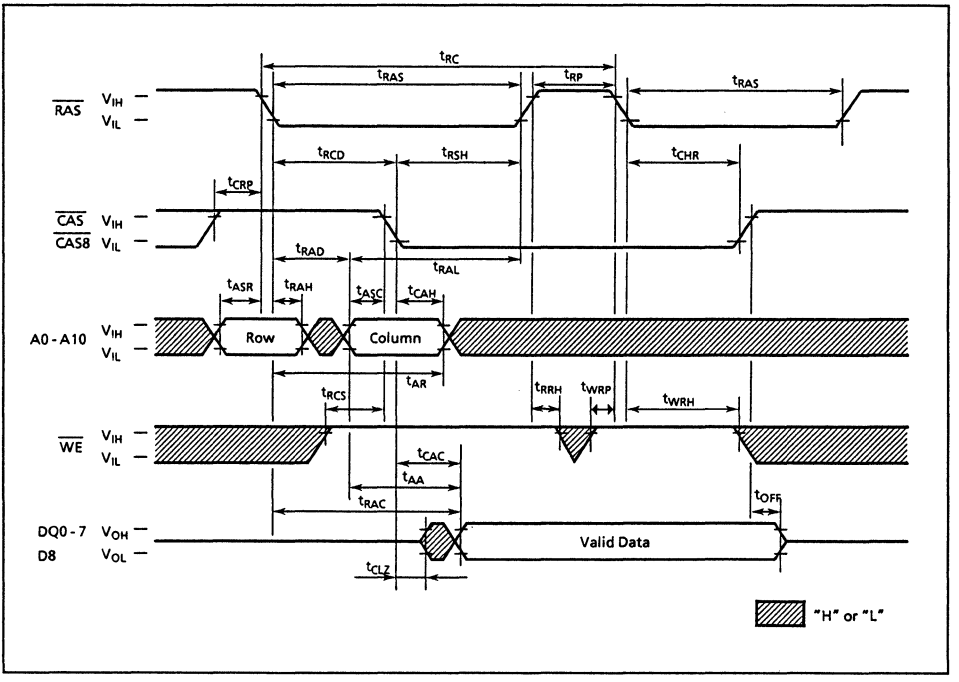
$\overline{RAS}$ ONLY REFRESH CYCLE



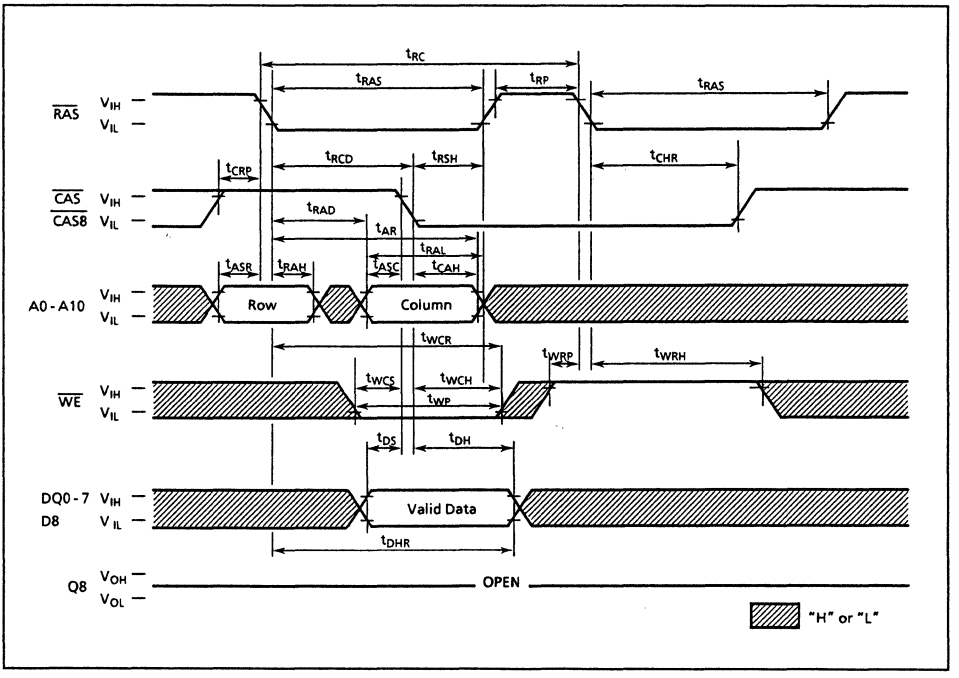
$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



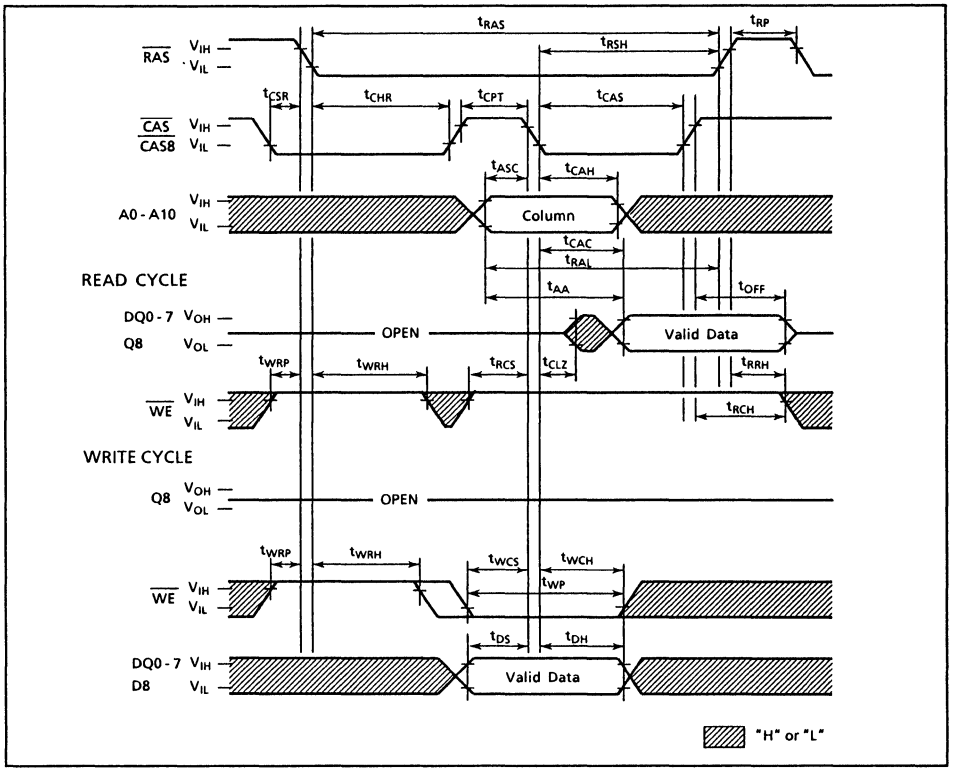
HIDDEN REFRESH READ CYCLE



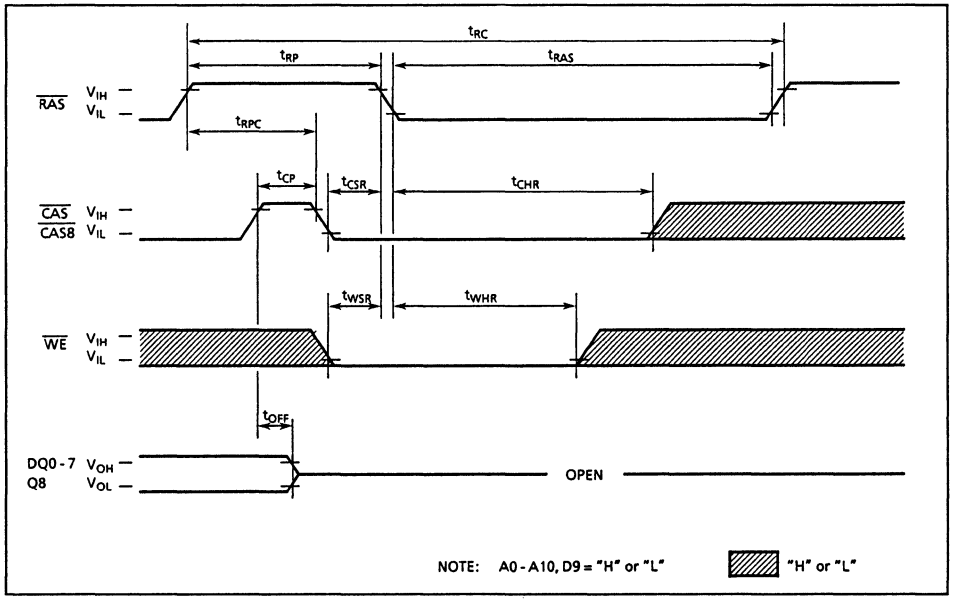
HIDDEN REFRESH WRITE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST



TEST MODE INITIATE CYCLE



32 Bit Series 4

OKI semiconductor
MSC2327A-xxYS8

262,144 Word BY 32 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2327A-xxYS8 is a fully decoded, 264,144 word x 32 bit CMOS dynamic random access memory composed of eight 1 Mb DRAMs in SOJ (MSM514256AJS). The mounting of eight SOJs together with eight 0.2 µF decoupling capacitors on a 72 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2327A-xxYS8 are same as the original MSM514256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

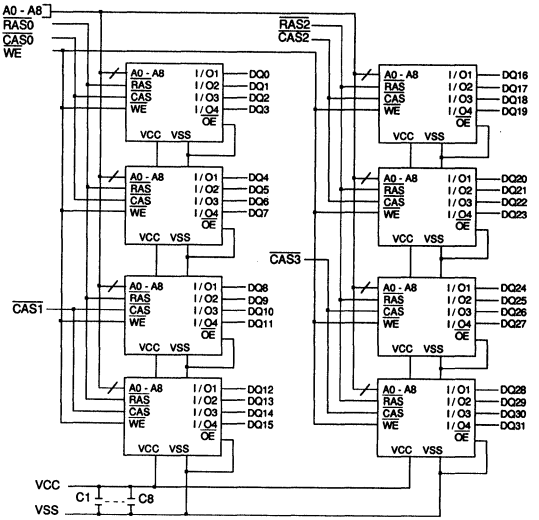
- 262,144 word x 32 bit organization
- JEDEC compatible dimensioning
- Family organization

Family	Access Time (MAX)			Cycle Time	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	(MIN)	Operating (MAX)	Standby (MAX)
MSC2327A-80YS8	80ns	40ns	20ns	160ns	3150mW	42mW
MSC2327A-10YS8	100ns	50ns	25ns	190ns	2730mW	(MOS level)

- Single +5V supply, ± 5% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Fast access and cycle times

4

FUNCTIONAL BLOCK DIAGRAM

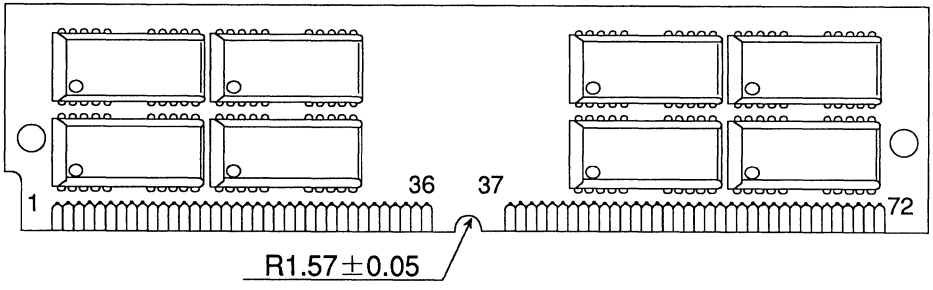


4

PIN CONFIGURATION

MSC2327A-xxYS8

TOP



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	VSS	16	A4	31	A8	46	$\overline{NC}$	61	DQ13
2	DQ0	17	A5	32	NC	47	$\overline{WE}$	62	DQ30
3	DQ16	18	A6	33	$\overline{NC}$	48	NC	63	DQ14
4	DQ1	19	NC	34	$\overline{RAS2}$	49	DQ8	64	DQ31
5	DQ17	20	DQ4	35	NC	50	DQ24	65	DQ15
6	DQ2	21	DQ20	36	NC	51	DQ9	66	NC
7	DQ18	22	DQ5	37	NC	52	DQ25	67	PD0
8	DQ3	23	DQ21	38	NC	53	DQ10	68	PD1
9	DQ19	24	DQ6	39	$\overline{VSS}$	54	DQ26	69	PD2
10	VCC	25	DQ22	40	$\overline{CAS0}$	55	DQ11	70	PD3
11	NC	26	DQ7	41	$\overline{CAS2}$	56	DQ27	71	NC
12	A0	27	DQ23	42	$\overline{CAS3}$	57	DQ12	72	VSS
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ28		
14	A2	29	NC	44	$\overline{RAS0}$	59	VCC		
15	A3	30	VCC	45	NC	60	DQ29		

Pin No.	Pin Name	MSC2327A-80YS8	MSC2327A-10YS8
67	PD0	VSS	VSS
68	PD1	N.C.	N.C.
69	PD2	N.C.	VSS
70	PD3	VSS	VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	–1 ~ +7	V
Operating temperature	T_{opr}	0 ~ +70	°C
Storage temperature	T_{stg}	–40 ~ +125	°C
Power dissipation	P_D	8	W
Short circuit output current	I_{os}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High voltage, all inputs	V_{IH}	2.4	-	6.25	V	
Input Low voltage, all inputs	V_{IL}	-1.0	-	0.8	V	

4

DC CHARACTERISTICS

(Vcc = 5V ±5%, Ta = 0 ~ +70°C)

Parameter	Symbol	Condition	MSC2327A-80YS8		MSC2327A-10YS8		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 6.25V : All other pins not under test = 0V)	–80	80	–80	80	μA	
Output Leakage Current	I_{LO}	Data out is disable, 0V ≤ V_{OUT} ≤ 5.25V	–20	10	–10	10	μA	
Output high voltage	V_{OH}	I_{OH} = –5mA	2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA	—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS0}$–$\overline{RAS2}$ cycling, $\overline{CAS0}$–$\overline{CAS3}$ cycling: t_{RC} = min.	—	600	—	520	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS0}$–$\overline{RAS2}$=V_{IH} TTL	—	16		16	mA	
		$\overline{CAS0}$–$\overline{CAS3}$=V_{IH} MOS	—	8	—	8	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS0}$–$\overline{RAS2}$ cycling, $\overline{CAS0}$–$\overline{CAS3}$ = V_{IH}, t_{RC} = min.	—	600	—	520	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC} = min	—	600	—	520	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS0}$–$\overline{RAS2}$ = V_{IL}, $\overline{CAS0}$–$\overline{CAS3}$ cycling, t_{PC} = min.	—	520	—	480	mA	1, 3

Note: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

CAPACITANCE

(V_{CC} = 5 V ±5%, f = 1MHz, Ta = 0 ~ +70°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 - A8)	C_{IN1}	—	60	pF
Input Capacitance ($\overline{WE}$)	C_{IN2}	—	76	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN3}	—	43	pF
Input Capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{IN4}	—	29	pF
I/O Capacitance ($\overline{DQ0}$ - $\overline{DQ31}$)	CDQ	—	17	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

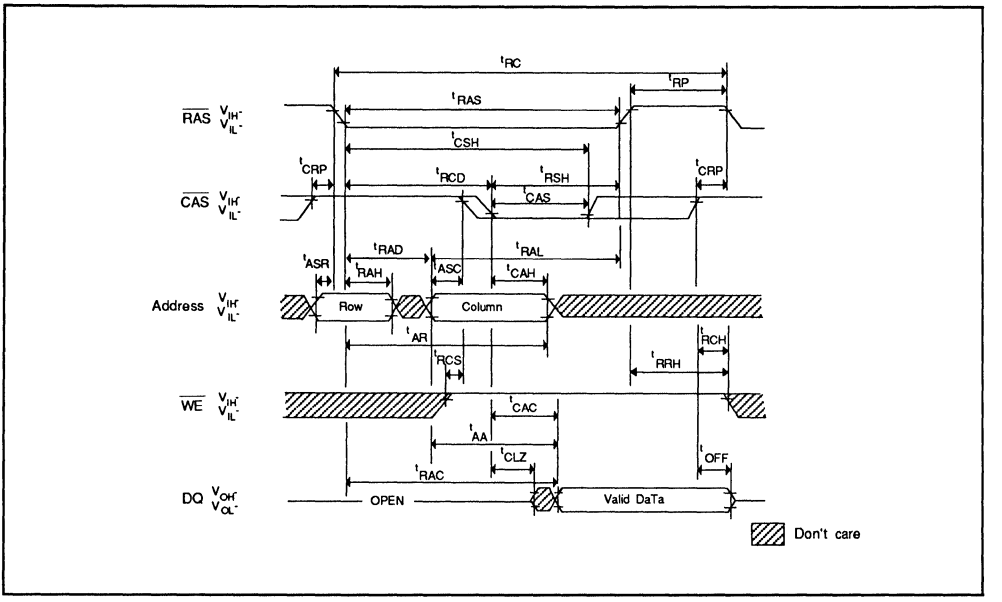
(V_{CC} = 5 V ±5%, Ta = 0 ~ +70°C)

Parameter	Symbol	MSC2327A-80YS8		MSC2327A-10YS8		Units	Notes
		Min.	Max.	Min.	Max.		
Random read or write cycle time	t_{RC}	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	2, 7
Access time from column address	t_{AA}	—	40	—	50	ns	2, 8
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	45	—	50	ns	2
$\overline{CAS}$ to output in Lo-Z	t_{CLZ}	0	—	0	—	ns	2
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	3
Transition time (Rise and Fall)	t_T	3	50	3	50	ns	1
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10k	100	10k	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100k	100	100k	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10k	25	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	7
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	8
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	ns	
Column address hold time refer. to $\overline{RAS}$	t_{AR}	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	ns	
Read command set-up	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	4
Read command hold time refer. to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	4
Write command hold time	t_{WCH}	15	—	20	—	ns	
Write command hold time refer. to $\overline{RAS}$	t_{WCR}	60	—	75	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	ns	
Date set-up time	t_{DS}	0	—	0	—	ns	5
Date hold time	t_{DH}	15	—	20	—	ns	5
Date hold time referenced to $\overline{RAS}$	t_{DHR}	60	—	75	—	ns	
Refresh period	t_{REF}	—	8	—	8	ms	
Write command set-up time	t_{WCS}	0	—	0	—	ns	6
$\overline{CAS}$ set-up time($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CHR}	30	—	30	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	ns	

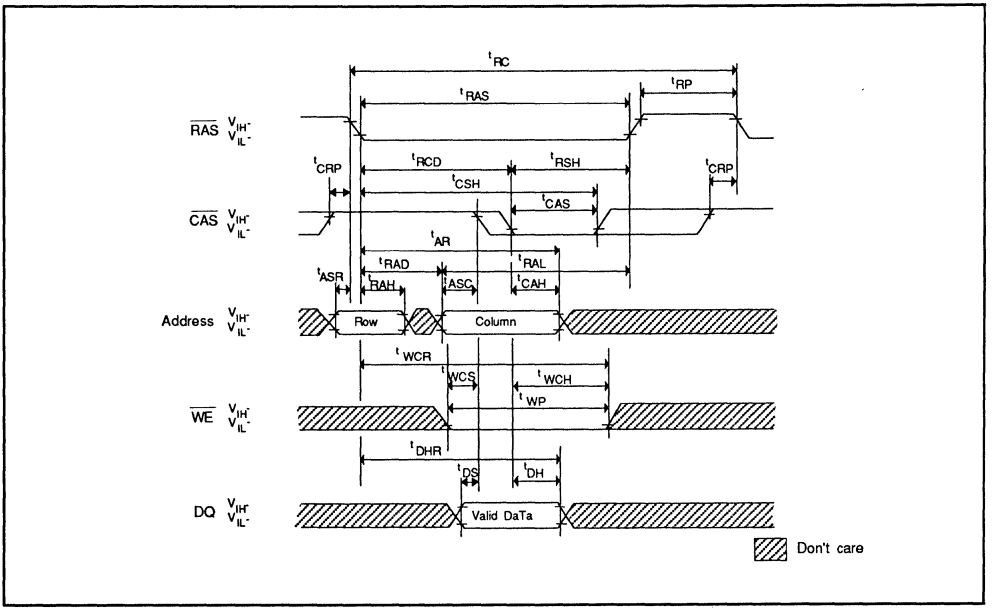
NOTES:

1) AC measurements assume t_T=5ns.
2) Measured wirth a load equivalent to 2 TTL loads and 100pF.
3) t_{OFF} (max) defines the time at which the output achieves an open circuit condition.
4) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5) These parameters are referenced to $\overline{CAS}$ leading edge.
6) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If t_{WCS}>t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain an open circuit (Hi-Z)
7) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
8) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

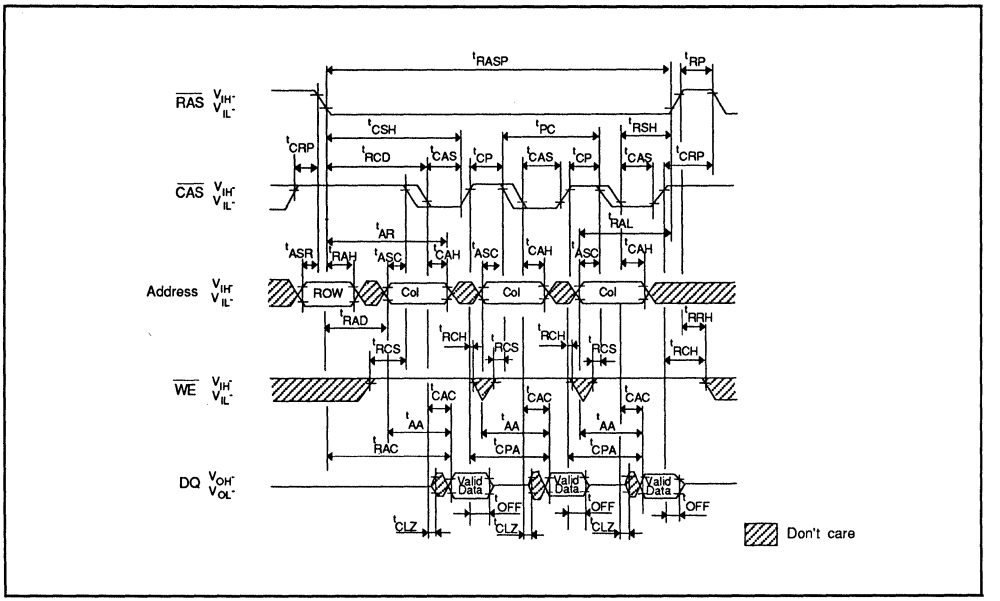
• READ CYCLE



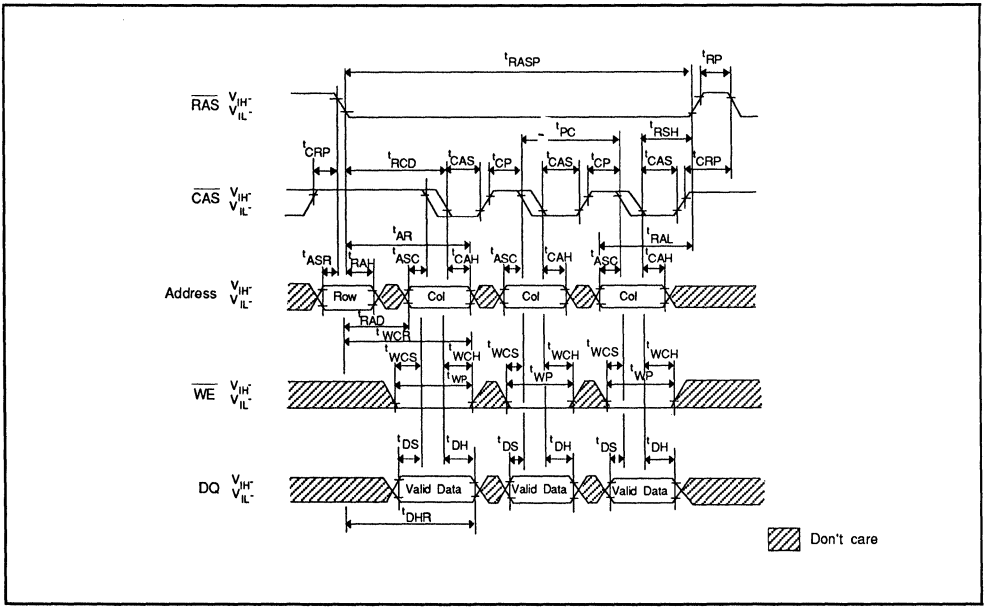
• WRITE CYCLE (EARLY WRITE)



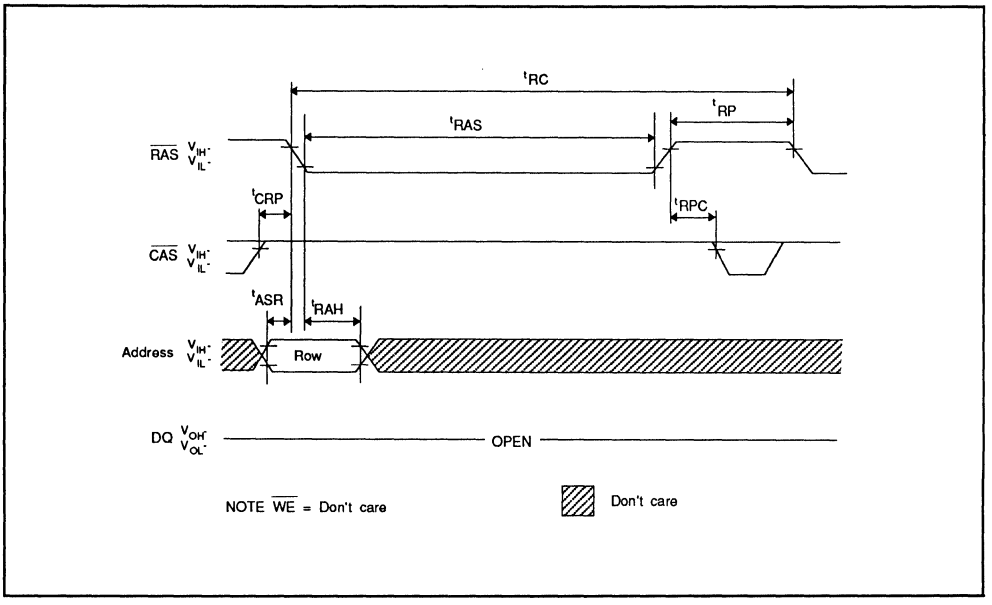
● FAST PAGE MODE READ CYCLE



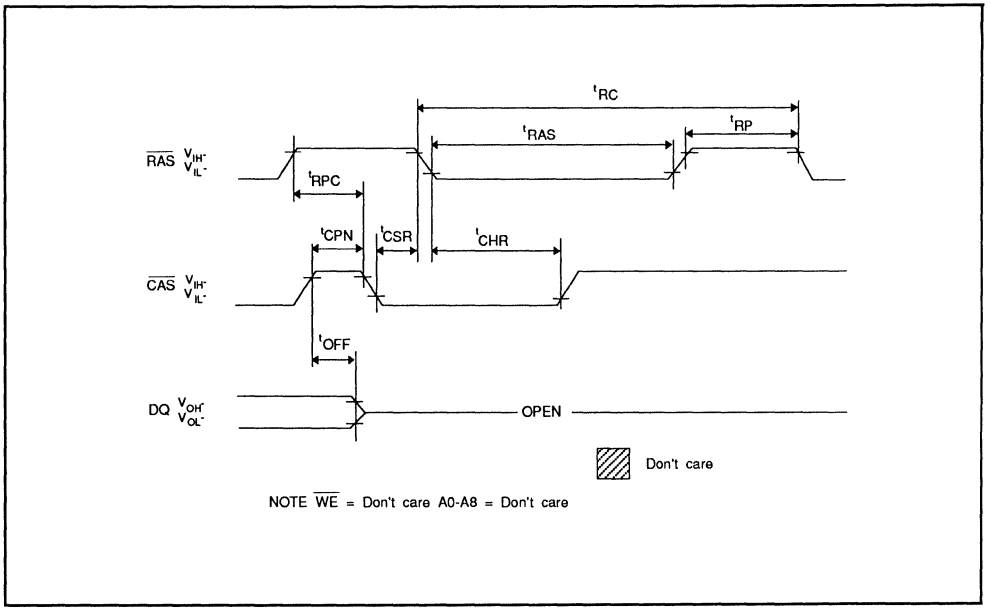
● FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



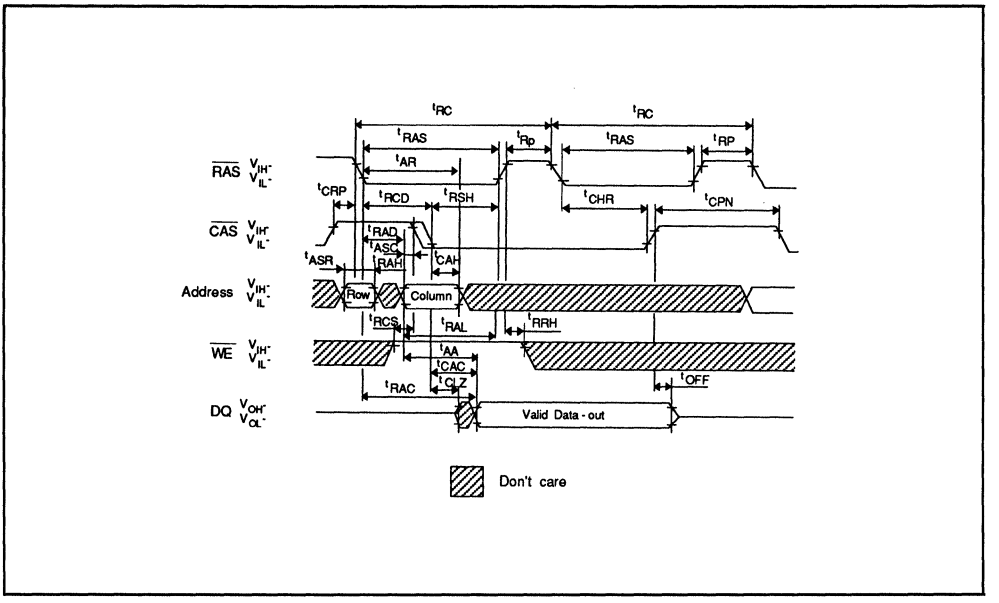
• $\overline{\text{RAS}}$ ONLY REFRESH CYCLE



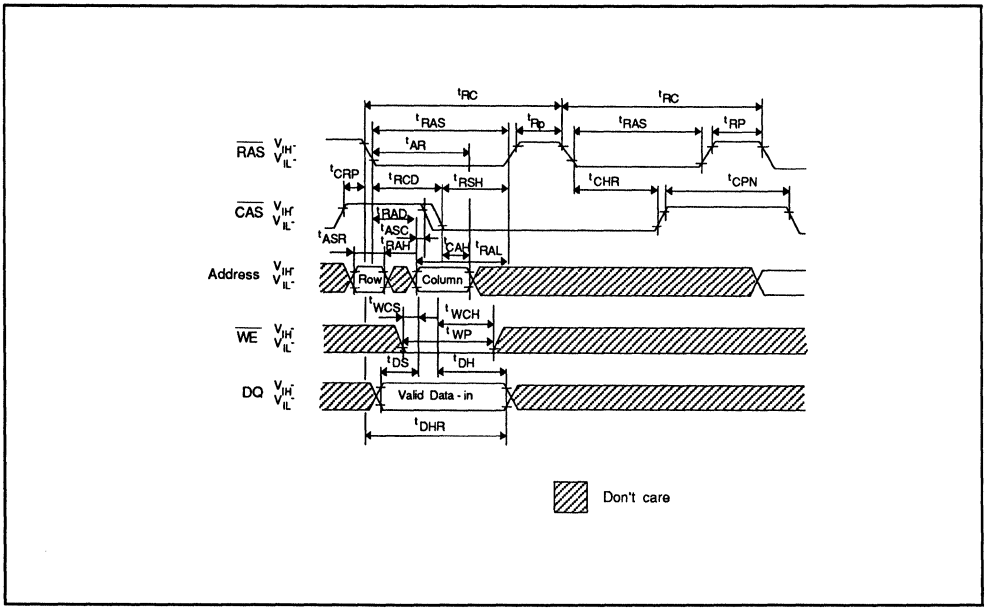
• $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



● HIDDEN REFRESH READ CYCLE



● HIDDEN REFRESH WRITE CYCLE



OKI semiconductor
MSC2333A-xxYS16

524,288 Word BY 32 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2333A-xxYS16 is a fully decoded, 524,288 word × 32 bit CMOS dynamic random access memory composed of sixteen 1 Mb DRAMs in SOJ (MSM514256AJS). The mounting of sixteen SOJs together with eight 0.2 μF decoupling capacitors on a 72 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2333A-xxYS16 are same as the original MSM514256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

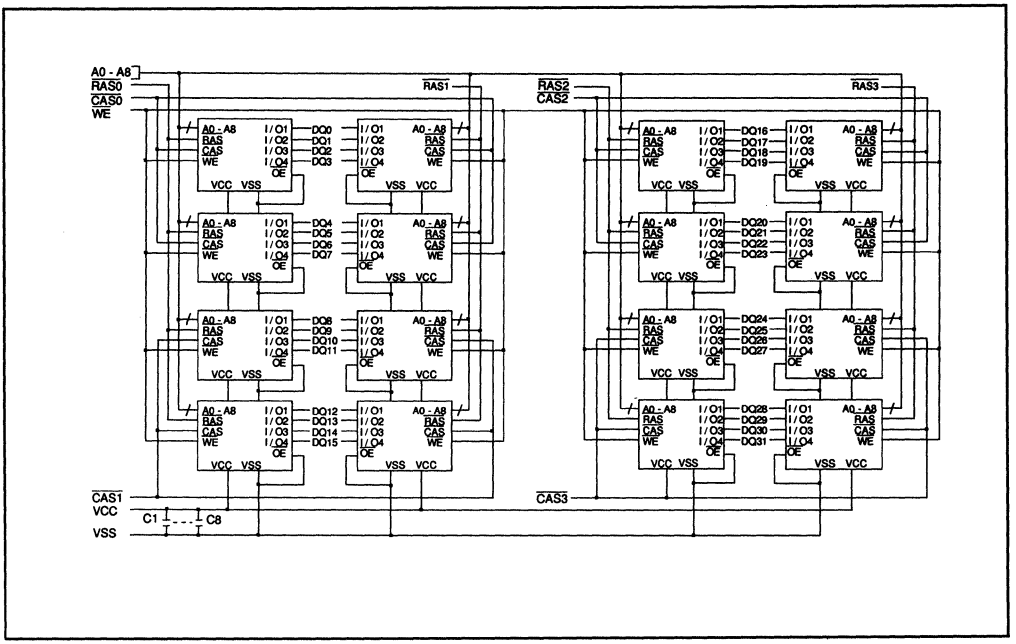
FEATURES

- 524.288 word × 32 bit organization
- JEDEC compatible dimensioning
- Family organization

Family	Access Time (MAX)			Cycle Time	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	(MIN)	Operating (MAX)	Standby (MAX)
MSC2333A-80YS16	80ns	40ns	20ns	160ns	3234mW	84mW
MSC2333A-10YS16	100ns	50ns	25ns	190ns	2814mW	(MOS level)

- Single +5V supply, ± 5% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Fast access and cycle times

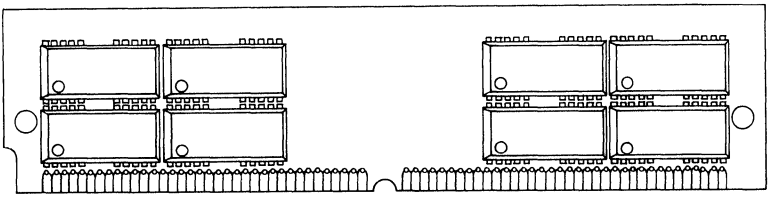
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

MSC2333A-xxYS16

TOP



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	VSS	16	A4	31	A8	46	NC	61	DQ13
2	DQ0	17	A5	32	NC	47	$\overline{WE}$	62	DQ30
3	DQ16	18	A6	33	$\overline{RAS3}$	48	NC	63	DQ14
4	DQ1	19	NC	34	$\overline{RAS2}$	49	DQ8	64	DQ31
5	DQ17	20	DQ4	35	NC	50	DQ24	65	DQ15
9	DQ19	21	DQ20	36	NC	51	DQ9	66	NC
6	DQ2	22	DQ5	37	NC	52	DQ25	67	PD0
7	DQ18	23	DQ21	38	NC	53	DQ10	68	PD1
8	DQ3	24	DQ6	39	VSS	54	DQ26	69	PD2
10	VCC	25	DQ22	40	$\overline{CAS0}$	55	DQ11	70	PD3
11	NC	26	DQ7	41	$\overline{CAS2}$	56	DQ27	71	NC
12	A0	27	DQ23	42	$\overline{CAS3}$	57	DQ12	72	VSS
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ28		
14	A2	29	NC	44	$\overline{RAS0}$	59	VCC		
15	A3	30	VCC	45	$\overline{RAS1}$	60	DQ29		

Pin No.	Pin Name	MSC2333A-80YS16	MSC2333A-10YS16
67	PD0	N.C.	N.C.
68	PD1	VSS	VSS
69	PD2	N.C.	VSS
70	PD3	VSS	VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	–1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	–1 ~ +7	V
Operating temperature	T_{opr}	0 ~ +70	°C
Storage temperature	T_{stg}	–40 ~ +125	°C
Power dissipation	P_D	16	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High voltage, all inputs	V_{IH}	2.4	—	6.25	V	
Input Low voltage, all inputs	V_{IL}	–1.0	—	0.8	V	

DC CHARACTERISTICS

(Vcc = 5V ±5%, Ta = 0 ~ +70°C)

Parameter	Symbol	Condition	MSC2333A-80YS16		MSC2333A-10YS16		Unit	Note
			Min.	Max.	Min.	Max.		
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ 6.25V : All other pins not under test = 0V	–160	160	–160	160	μA	
Output Leakage Current	I_{LO}	Data out is disable, 0V ≤ V_{OUT} ≤ 5.25V	–20	20	–20	20	μA	
Output high voltage	V_{OH}	I_{OH} = –5mA	2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA	—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS0}$–$\overline{RAS3}$ cycling, $\overline{CAS0}$–$\overline{CAS3}$ cycling: t_{RC} = min.	—	616	—	536	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS0}$–$\overline{RAS3}$=V_{IH} TTL	—	32		32	mA	
		$\overline{CAS0}$–$\overline{CAS3}$=V_{IH} MOS	—	16	—	16	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS0}$–$\overline{RAS3}$ cycling, $\overline{CAS0}$–$\overline{CAS3}$ = V_{IH}, t_{RC} = min.	—	616	—	536	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC} = min	—	616	—	536	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS0}$–$\overline{RAS3}$ = V_{IL}, $\overline{CAS0}$–$\overline{CAS3}$ cycling, t_{PC} = min.	—	536	—	496	mA	1, 3

Note: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

CAPACITANCE

(V_{CC} = 5 V ±5%, f = 1MHz, Ta = 0 ~ +70°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 - A8)	C_{IN1}	—	115	pF
Input Capacitance ($\overline{WE}$)	C_{IN2}	—	137	pF
Input Capacitance ($\overline{RAS0}$ - $\overline{RAS3}$)	C_{IN3}	—	48	pF
Input Capacitance ($\overline{CAS0}$ - $\overline{CAS3}$)	C_{IN4}	—	48	pF
I/O Capacitance ($\overline{DQ0}$ - $\overline{DQ31}$)	CDQ_1	—	29	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5 V ±5%, Ta = 0 ~ +70°C)

Parameter	Symbol	MSC2333A-80YS16		MSC2333A-10YS16		Units	Notes
		Min.	Max.	Min.	Max.		
Random read or write cycle time	t_{RC}	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	2, 7
Access time from column address	t_{AA}	—	40	—	50	ns	2, 8
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	45	—	50	ns	2
$\overline{CAS}$ to output in Lo-Z	t_{CLZ}	0	—	0	—	ns	2
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	3
Transition time (Rise and Fall)	t_T	3	50	3	50	ns	1
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10k	100	10k	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100k	100	100k	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10k	25	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	7
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	8
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	ns	
Column address hold time refer. to $\overline{RAS}$	t_{AR}	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	ns	
Read command set-up	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	4
Read command hold time refer. to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	4
Write command hold time	t_{WCH}	15	—	20	—	ns	
Write command hold time refer. to $\overline{RAS}$	t_{WCR}	60	—	75	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	ns	
Date set-up time	t_{DS}	0	—	0	—	ns	5
Date hold time	t_{DH}	15	—	20	—	ns	5
Date hold time referenced to $\overline{RAS}$	t_{DHR}	60	—	75	—	ns	
Refresh period	t_{REF}	—	8	—	8	ms	
Write command set-up time	t_{WCS}	0	—	0	—	ns	6
$\overline{CAS}$ set-up time($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CHR}	30	—	30	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	ns	

NOTES: 1) AC measurements assume t_T = 5ns.

2) Measured wirth a load equivalent to 2 TTL loads and 100pF.

3) t_{OFF} (max(defines the time at which the output achieves an open circuit condition.

4) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

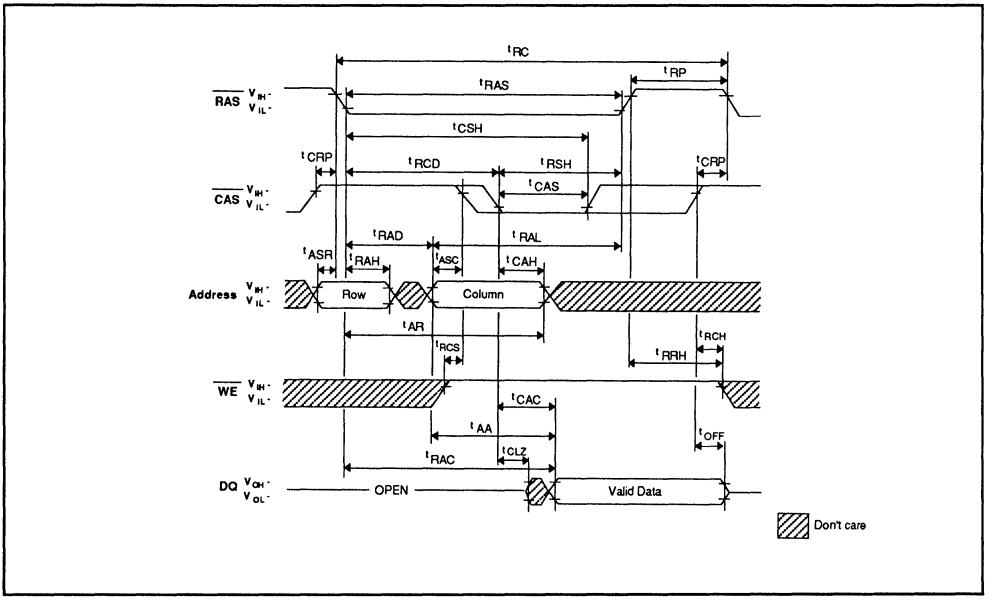
5) These parameters are referenced to $\overline{CAS}$ leading edge.

6) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If t_{WCS}>t_{WCS} (min), the cycle is an early write cycle and the data out pin will remain an open circuit (Hi-Z)

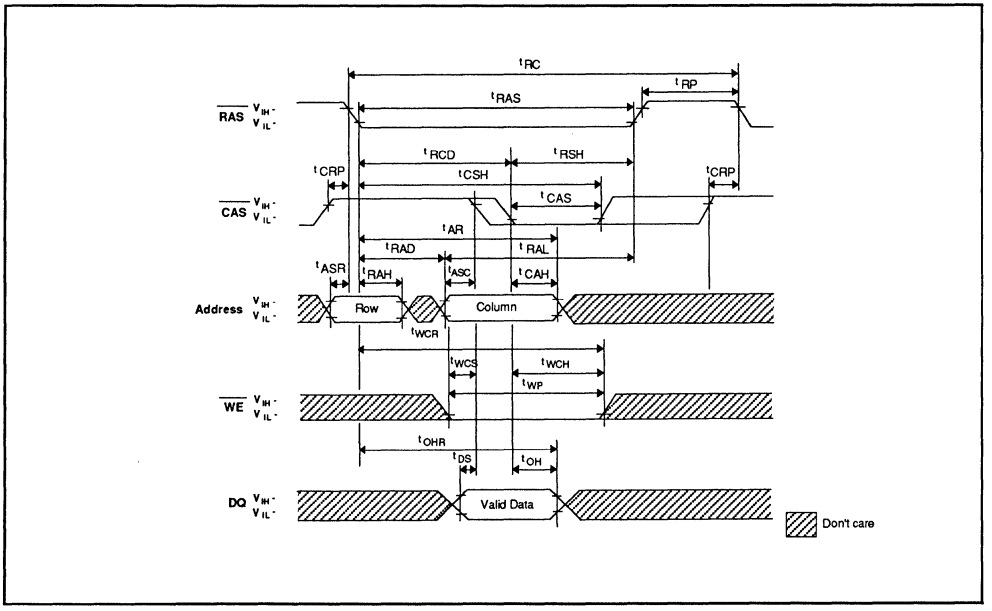
7) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.

8) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

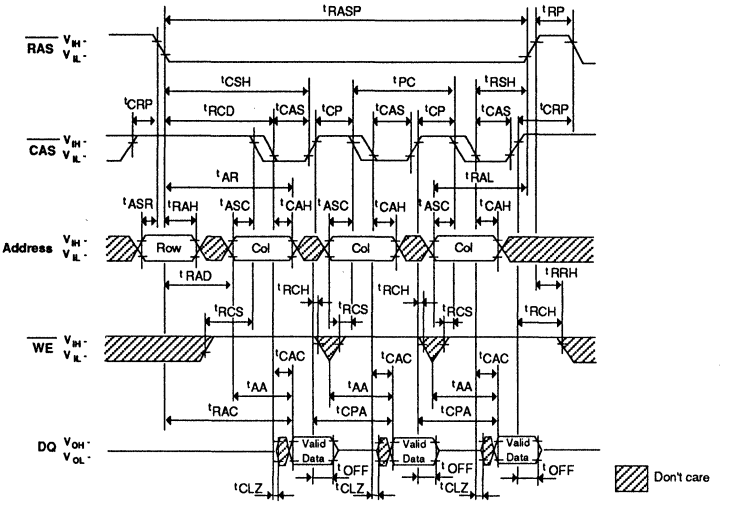
• READ CYCLE



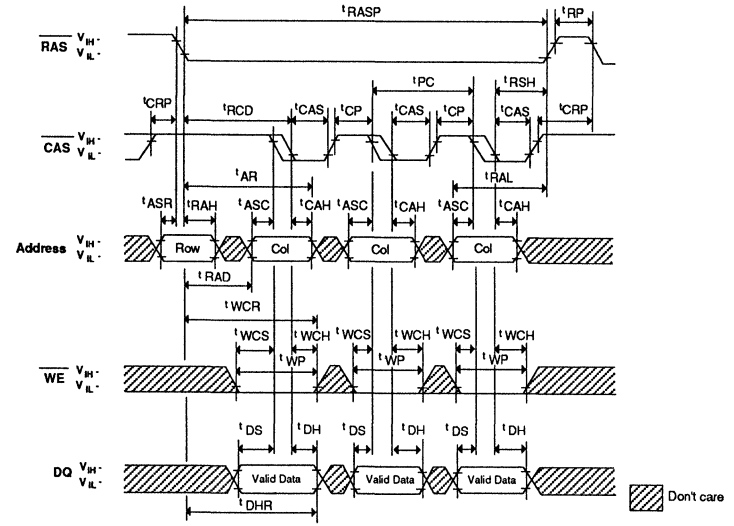
• WRITE CYCLE (EARLY WRITE)



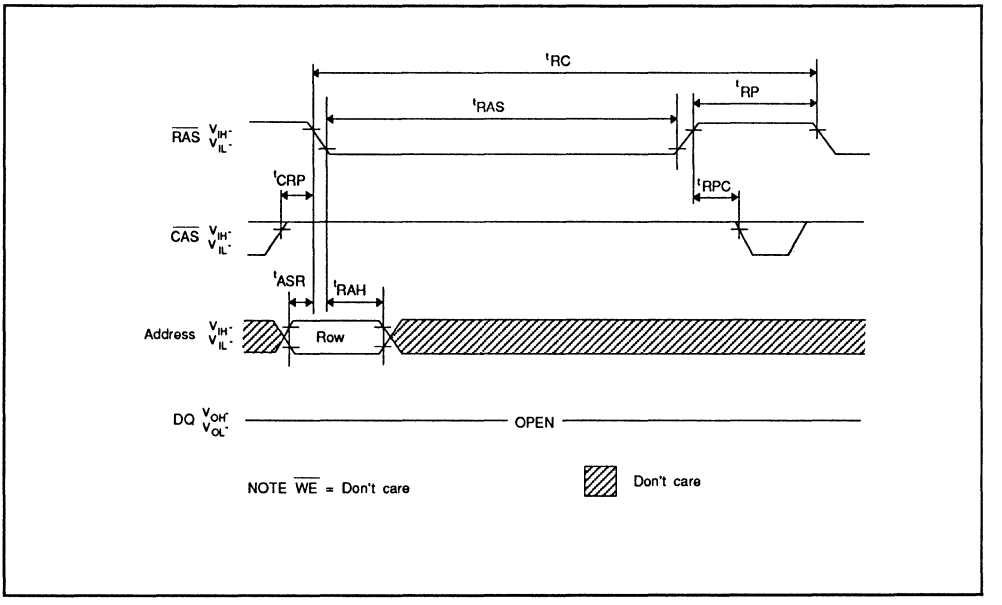
• FAST PAGE MODE READ CYCLE



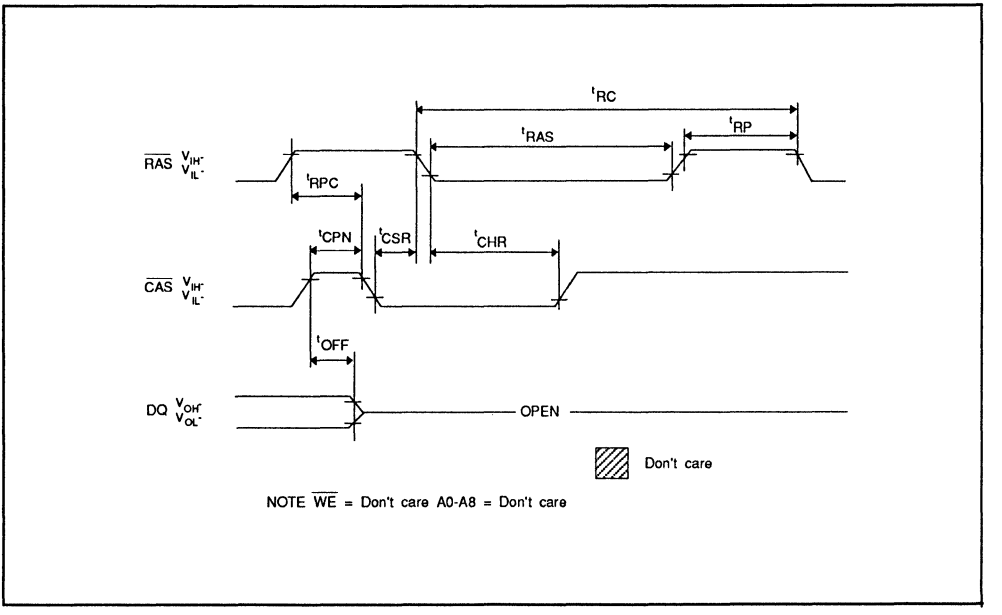
• FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



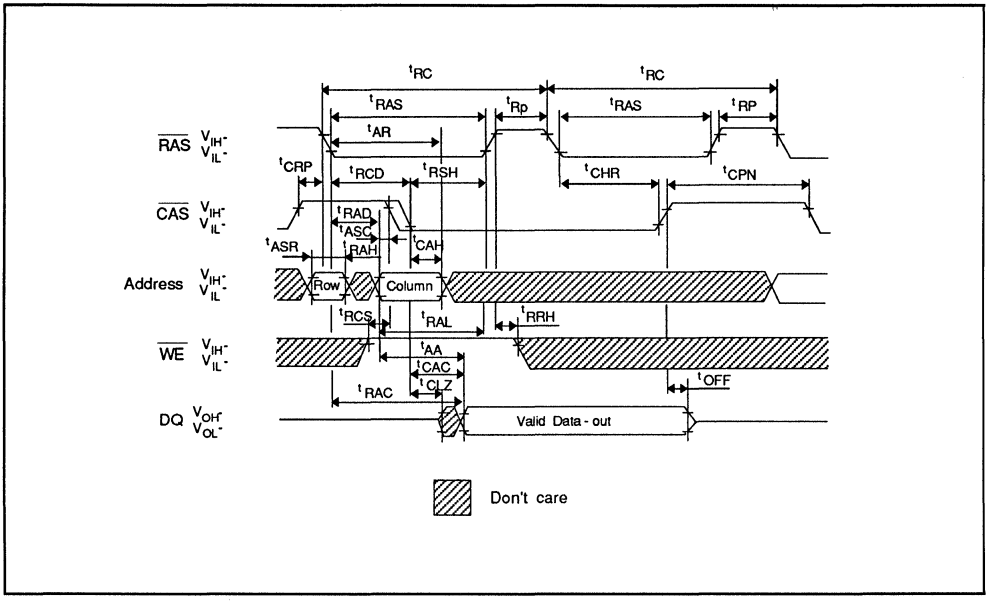
• $\overline{RAS}$ ONLY REFRESH CYCLE



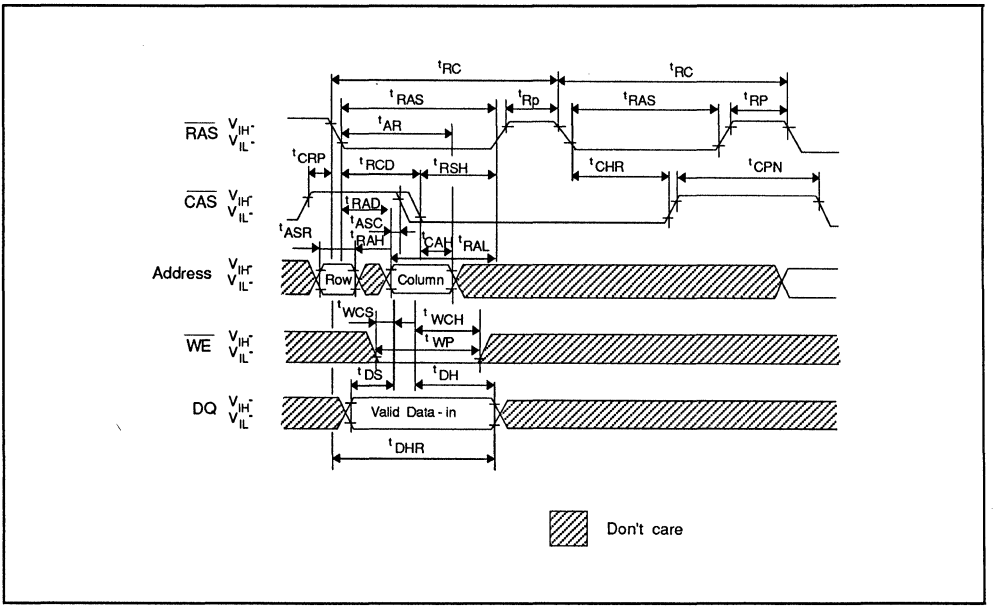
• $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



• HIDDEN REFRESH READ CYCLE



• HIDDEN REFRESH WRITE CYCLE



OKI semiconductor
MSC2357-xxYS8

PRELIMINARY

1,048,576 Word x 32 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2357-xxYS8 is a fully decoded, 1,048,576 word by 32 bit CMOS dynamic random access memory composed of eight 4Mb DRAMs in SOJ (MSM514400JS). The mounting of eight SOJs together with eight 0.2 µF decoupling capacitors on a 72 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2357-xxYS8 are same as the original MSM514400JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

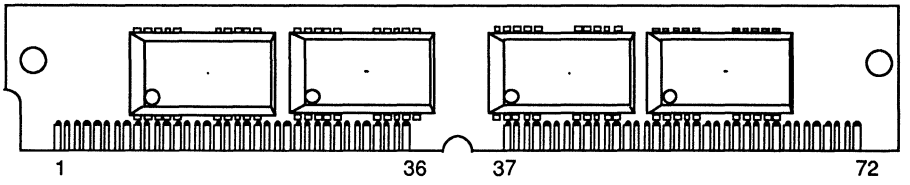
- 1,048,576 word x 32 bit organization
- 72-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (MAX)	Standby (MAX)
MSC2357-80YS8	80 ns	40 ns	20 ns	160 ns	3780 mW	42 mW (MOS level)
MSC2357-10YS8	100 ns	50 ns	25 ns	190 ns	3360 mW	

- Single +5V supply, ±5% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi-bit test mode capability

PIN CONFIGURATION

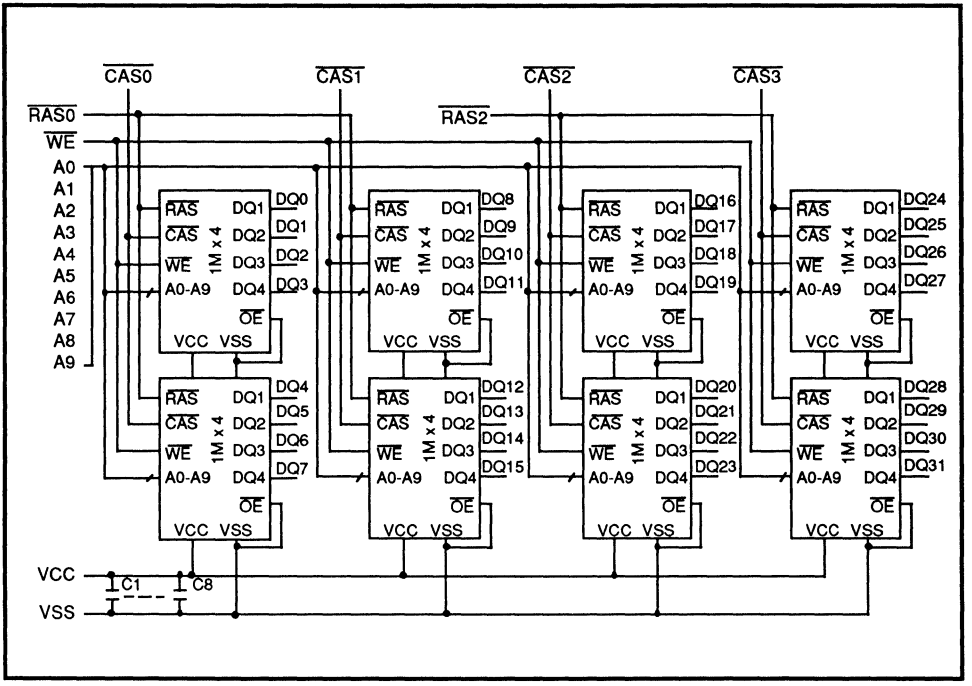
MSC2357-xxYS8



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	VSS	25	DQ22	49	DQ8
2	DQ0	26	DQ7	50	DQ24
3	DQ16	27	DQ23	51	DQ9
4	DQ1	28	A7	52	DQ25
5	DQ17	29	N. C.	53	DQ10
6	DQ2	30	VCC	54	DQ26
7	DQ18	31	A8	55	DQ11
8	DQ3	32	A9	56	DQ27
9	DQ19	33	N. C.	57	DQ12
10	VCC	34	$\overline{RAS2}$	58	DQ28
11	N. C.	35	N. C.	59	VCC
12	A0	36	N. C.	60	DQ29
13	A1	37	N. C.	61	DQ13
14	A2	38	N. C.	62	DQ30
15	A3	39	VSS	63	DQ14
16	A4	40	$\overline{CAS0}$	64	DQ31
17	A5	41	$\overline{CAS2}$	65	DQ15
18	A6	42	$\overline{CAS3}$	66	N. C.
19	N. C.	43	$\overline{CAS1}$	67	PD0
20	DQ4	44	$\overline{RAS0}$	68	PD1
21	DQ20	45	N. C.	69	PD2
22	DQ5	46	N. C.	70	PD3
23	DQ21	47	$\overline{WE}$	71	N. C.
24	DQ6	48	N. C.	72	VSS

Pin No.	Pin Name	MSC2357-80YS8	MSC2357-10YS8
67	PD0	N.C.	N.C.
68	PD1	N.C.	N.C.
69	PD2	N.C.	N.C.
70	PD3	N.C.	N.C.

FUNCTIONAL BLOCK DIAGRAM



36 Bit Series 4

MSC2320A-xxYS9

262,144 Word BY 36 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2320A-xxYS9 is a fully decoded, 262,144 word × 36 bit CMOS dynamic random access memory composed of eight 1Mb DRAMs in SOJ (MSM514256AJS) and four 256 Kb DRAMs in PLCC (MSM51C256JS). The mounting of eight SOJs and four PLCCs together with twelve 0.2 μF decoupling capacitors on a 72 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2320A-xxYS9 are same as the original MSM514256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

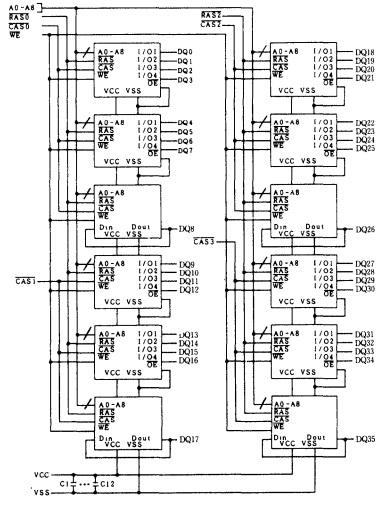
FEATURES

- 262,144 word × 36 bit organization
- JEDEC Compatible Dimensioning
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2320A-80YS9	80ns	40ns	20ns	160ns	4410mW	95mW (MOS level)
MSC2320A-10YS9	100ns	50ns	25ns	190ns	3780mW	

- Single + 5V supply, ±5% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh, and fast page mode capability
- Fast access and cycle times

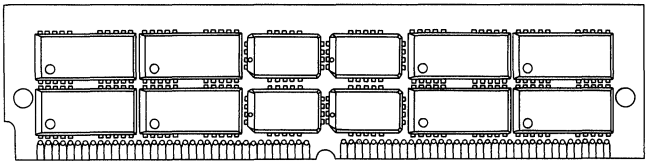
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

MSC2320A-xxYS9

TOP



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	VSS	16	A4	31	A8	46	NC	61	DQ14
2	DQ0	17	A5	32	NC	47	$\overline{WE}$	62	DQ33
3	DQ18	18	A6	33	NC	48	NC	63	DQ15
4	DQ1	19	NC	34	$\overline{RAS2}$	49	DQ9	64	DQ34
5	DQ19	20	DQ4	35	DQ26	50	DQ27	65	DQ16
6	DQ2	21	DQ22	36	DQ8	51	DQ10	66	NC
7	DQ20	22	DQ5	37	DQ17	52	DQ28	67	PD0
8	DQ3	23	DQ23	38	DQ35	53	DQ11	68	PD1
9	DQ21	24	DQ6	39	VSS	54	DQ29	69	PD2
10	VCC	25	DQ24	40	$\overline{CAS0}$	55	DQ12	70	PD3
11	NC	26	DQ7	41	$\overline{CAS2}$	56	DQ30	71	NC
12	A0	27	DQ25	42	$\overline{CAS3}$	57	DQ13	72	VSS
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ31		
14	A2	29	NC	44	$\overline{RAS0}$	59	VCC		
15	A3	30	VCC	45	NC	60	DQ32		

Pin No.	Pin Name	MSC2320A-80YS9	MSC2320A-10YS9
67	PD0	VSS	VSS
68	PD1	N.C.	N.C.
69	PD2	N.C.	VSS
70	PD3	VSS	VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ 125	°C
Power dissipation	P_D	12	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.25	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±5%, Ta=0~+70°C)

Parameter	Symbol	Condition	MSC2320A-80YS9 Min.	MSC2320A-80YS9 Max.	MSC2320A-10YS9 Min.	MSC2320A-10YS9 Max.	Unit	Note
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.25V : All other pins not under test=0V	−120	120	−120	120	μA	
Output Leakage Current	I_{LO}	Data out is disable 0V≤V_{OUT}≤5.25V	−10	10	−10	10	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA	2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA	—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS0}$, $\overline{RAS2}$ cycling, $\overline{CAS0}$−$\overline{CAS3}$ cycling, t_{RC}=min	—	840	—	720	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS0}$, $\overline{RAS2}$=V_{IH} TTL	—	30	—	30	mA	
		$\overline{CAS0}$−$\overline{CAS3}$=V_{IH} MOS	—	18	—	18	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS0}$, $\overline{RAS2}$ cycling, $\overline{CAS0}$−$\overline{CAS3}$=V_{IH} t_{RC}=min	—	840	—	720	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.	—	840	—	720	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS0}$, $\overline{RAS2}$=V_{IL}, $\overline{CAS0}$−$\overline{CAS3}$ cycling t_{PC}=min.	—	680	—	620	mA	1, 3

Note : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

4

CAPACITANCE

(V_{CC}=5V±5%, f=1MHz, Ta=0~+70°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 – A8)	C_{IN1}	–	88	pF
Input Capacitance ($\overline{WE}$)	C_{IN2}	–	104	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN3}	–	57	pF
Input Capacitance ($\overline{CAS0}$–$\overline{CAS3}$)	C_{IN4}	–	36	pF
I/O Capacitance (DQ0–7, 9–16, 18–25, 27–34)	CDQ_1	–	17	pF
I/O Capacitance (DQ8, 17, 26, 35)	CDQ_2	–	22	pF

Capacitance measured with Boonton Meter.

4

AC CHARACTERISTICS

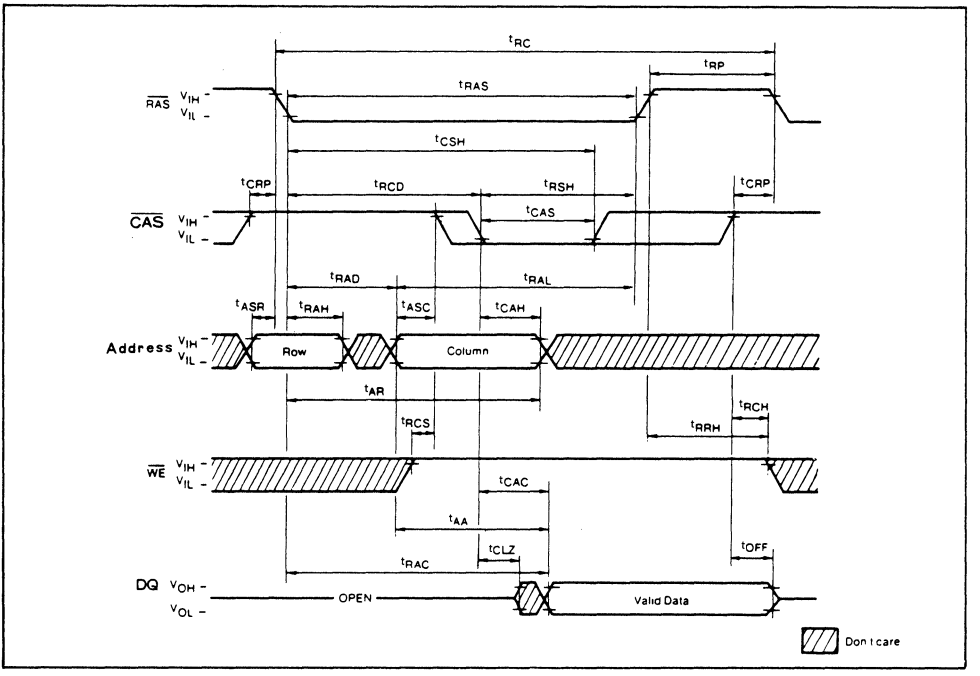
(V_{CC} = 5V ± 5%, Ta = 0 ~ +70°C)

Parameter	Symbol	MSC2320A-80YS9		MSC2320A-10YS9		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	2, 7
Access time from column address	t_{AA}	—	40	—	50	ns	2, 8
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	45	—	50	ns	2
$\overline{CAS}$ to output in Lo-Z	t_{CLZ}	0	—	0	—	ns	2
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	3
Transition time (Rise and Fall)	t_T	3	50	3	50	ns	1
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	7
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	8
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	ns	
Column address hold time refer. to $\overline{RAS}$	t_{AR}	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	ns	
Read command set-up	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	4
Read command hold time refer. to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	4
Write command hold time	t_{WCH}	15	—	20	—	ns	
Write command hold time refer. to $\overline{RAS}$	t_{WCR}	65	—	75	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	ns	
Date set-up time	t_{DS}	0	—	0	—	ns	5
Date hold time	t_{DH}	15	—	20	—	ns	5
Date hold time referenced to $\overline{RAS}$	t_{DHR}	65	—	75	—	ns	
Refresh period	t_{REF}	—	8	—	8	ms	
Write command set-up time	t_{WCS}	0	—	0	—	ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CHR}	30	—	30	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	ns	

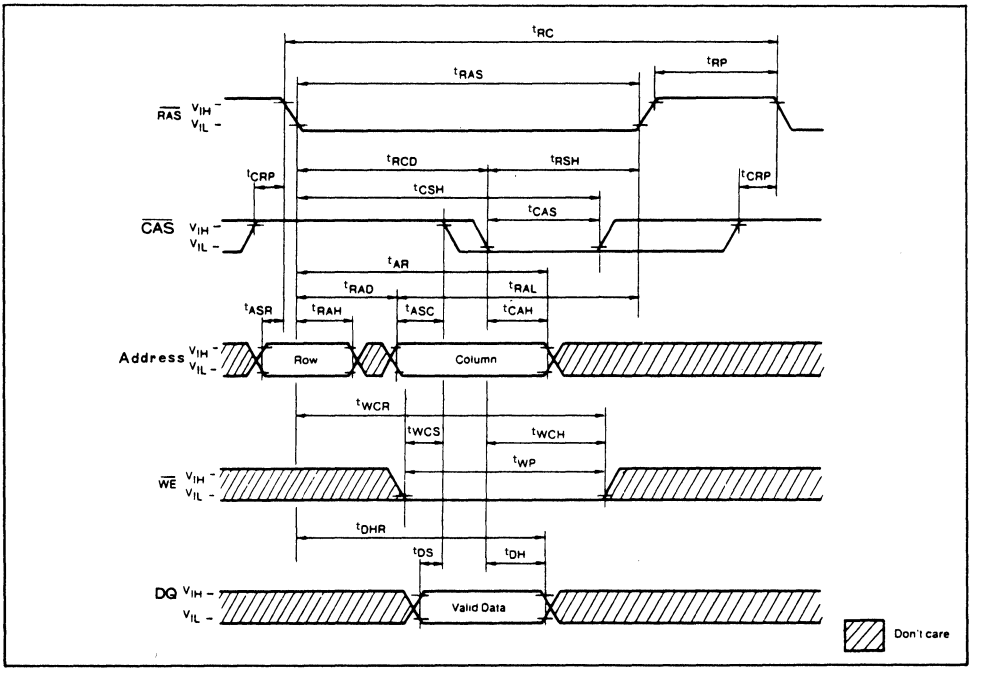
NOTES :

1) AC measurements assume t_T =5ns.
2) Measured with a load equivalent to 2 TTL loads and 100pf.
3) t_{OFF} (max) defines the time at which the output achieves an open circuit condition.
4) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5) These paramenters are referenced to $\overline{CAS}$ leading edge.
6) t_{WCS} is not a restictive operating parameter. This is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is and early write cycle and the data out pin will remain as open circuit (Hi-Z)
7) Operation within the t_{RCD} (max) limit, insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only : if t_{RCD} is greater than the specified t_{RCD} (max) limit, them access time is controlled by t_{CAC}.
8) Operation within the t_{RAD} (max) limit, insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only : if t_{RAD} is greater than the specified t_{RAD} (max) limit, them access time is controlled by t_{AA}.

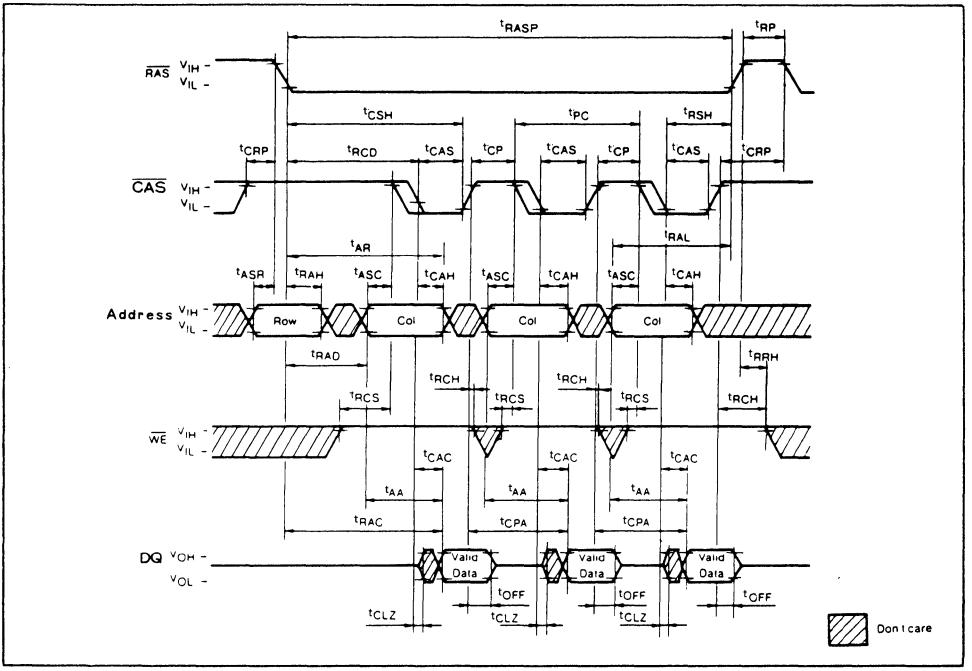
● READ CYCLE



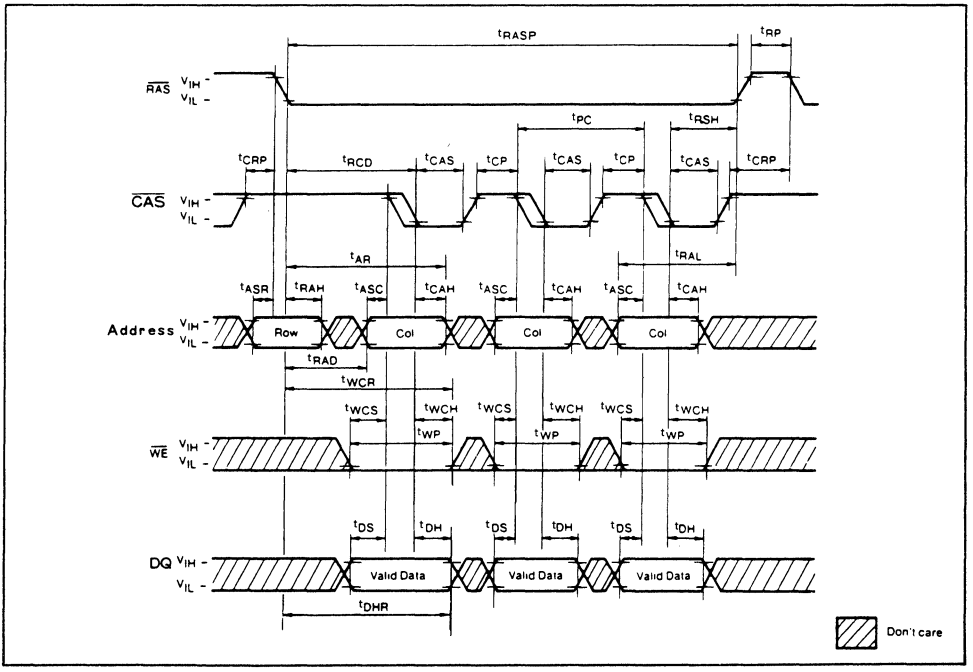
● WRITE CYCLE (EARLY WRITE)



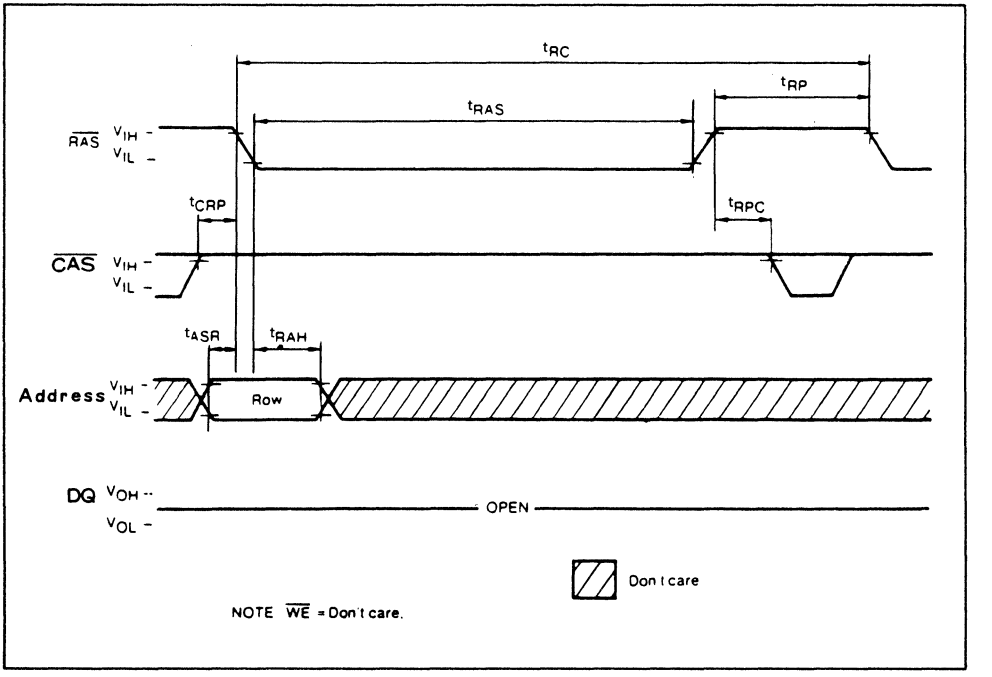
● FAST PAGE MODE READ CYCLE



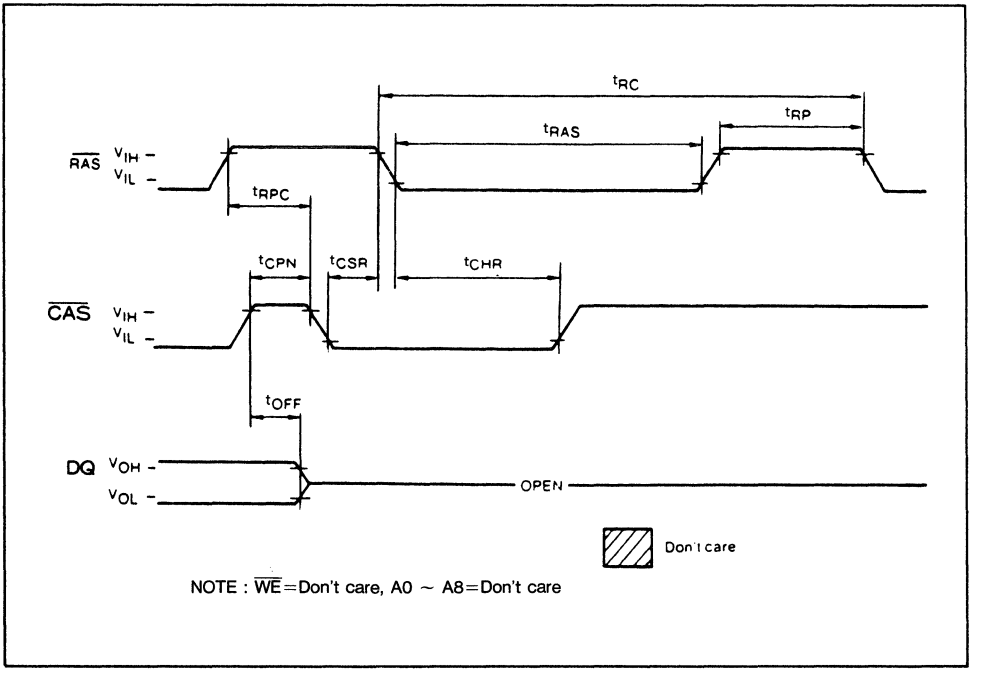
● FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



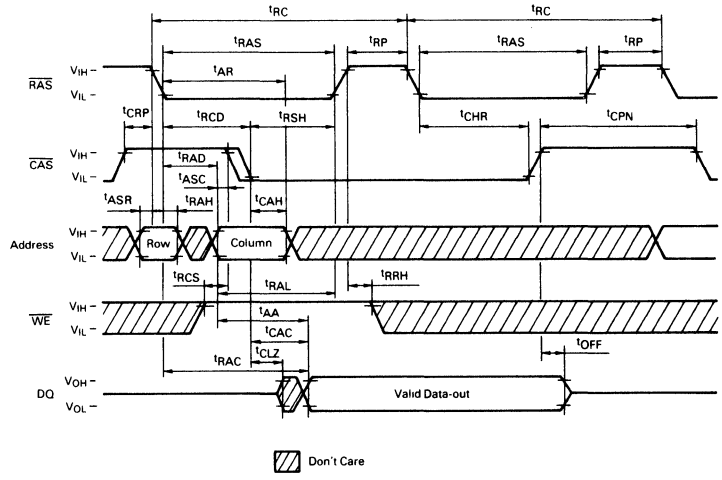
● $\overline{RAS}$ ONLY REFRESH CYCLE



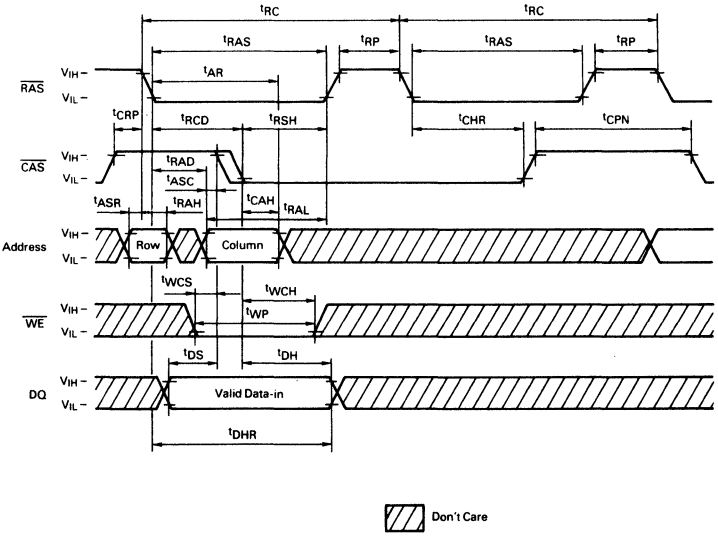
● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



● HIDDEN REFRESH READ CYCLE



● HIDDEN REFRESH WRITE CYCLE



MSC2321A-xxYS18

524,288 Word BY 36 Bit DYNAMIC RAM MODULE : FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2321A-xxYS18 is a fully decoded, 524,288 word × 32 bit CMOS dynamic random access memory composed of sixteen 1 Mb DRAMs in SOJ (MSM514256AJS) and eight 256 Kb DRAMs in PLCC (MSM51C256JS). The mounting of sixteen SOJs and eight PLCCs together with twelve 0.2 μF decoupling capacitors on a 72 pin glass epoxy Single-In-Line Package supports any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2321A-xxYS18 are same as the original MSM514256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

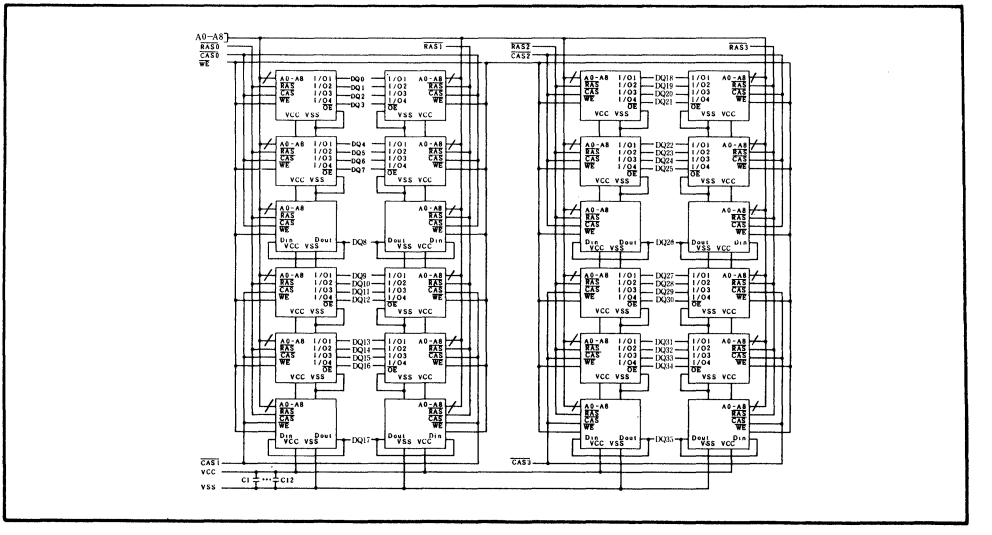
FEATURES

- 524,288 word × 36 bit organization
- JEDEC Compatible Dimensioning
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Oparating (MAX)	Standby (MAX)
MSC2321A-80YS18	80ns	40ns	20ns	160ns	4568mW	189mW (MOS level)
MSC2331A-10YS18	100ns	50ns	25ns	190ns	3938mW	

- Single + 5V supply, ±5% tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 512 cycles/8 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh, and fast page mode capability
- Fast access and cycle times

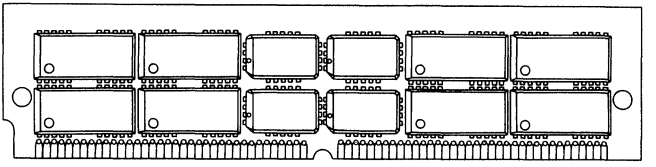
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

MSC2321A-xxYS18

TOP



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	VSS	16	A4	31	A8	46	NC	61	DQ14
2	DQ0	17	A5	32	NC	47	WE	62	DQ33
3	DQ18	18	A6	33	RAS3	48	NC	63	DO15
4	DQ1	19	NC	34	RAS2	49	DQ9	64	DQ34
5	DQ19	20	DQ4	h5	DQ26	50	DQ27	65	DQ16
6	DQ2	21	DQ22	36	DQ8	51	DQ10	66	NC
7	DQ20	22	DQ5	37	DQ17	52	DQ28	67	PD0
8	DQ3	23	DQ23	38	DQ35	53	DQ11	68	PD1
9	DQ21	24	DQ6	39	VSS	54	DQ29	69	PD2
10	VCC	25	DQ24	40	CAS0	55	DQ12	70	PD3
11	NC	26	DQ7	41	CAS2	56	DQ30	71	NC
12	A0	27	DQ25	42	CAS3	57	DQ3	72	VSS
13	A1	28	A7	43	CAS1	58	DQ31		
14	A2	29	NC	44	RAS0	59	VCC		
15	A3	30	VCC	45	RAS1	60	DQ32		

Pin No.	Pin Name	MSC2321A-80YS18	MSC2321A-10YS18
67	PD0	N.C.	N.C.
68	PD1	VSS	VSS
69	PD2	N.C.	VSS
70	PD3	VSS	VSS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 ~ +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 ~ +7	V
Operating temperature	Topr	0 ~ 70	°C
Storage temperature	Tstg	−40 ~ 125	°C
Power dissipation	P_D	4	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.25	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(V_{CC}=5V±5%, Ta=0~+70°C)

Parameter	Symbol	Condition	MSC2321A-80YS18 Min.	MSC2321A-80YS18 Max.	MSC2321A-10YS18 Min.	MSC2321A-10YS18 Max.	Unit	Note
Input Leakage Current	I_{LI}	0V≤V_{IN}≤6.25V : All other pins not under test=0V	−240	240	−240	240	μA	
Output Leakage Current	I_{LO}	Data out is disable 0V≤V_{OUT}≤5.25V	−20	20	−20	20	μA	
Output high voltage	V_{OH}	I_{OH}=−5.0mA	2.4	—	2.4	—	V	
Output low voltage	V_{OL}	I_{OL}=4.2mA	—	0.4	—	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS0}$−$\overline{RAS3}$ cycling, $\overline{CAS0}$−$\overline{CAS3}$ cycling, t_{RC}=min	—	870	—	750	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS0}$−$\overline{RAS3}$=V_{IH} TTL	—	60	—	60	mA	
		$\overline{CAS0}$−$\overline{CAS3}$=V_{IH} MOS	—	36	—	36	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS0}$−$\overline{RAS3}$ cycling, $\overline{CAS0}$−$\overline{CAS3}$=V_{IH} t_{RC}=min	—	870	—	750	mA	1, 2
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC}=min.	—	870	—	750	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS0}$−$\overline{RAS3}$=V_{IL}, $\overline{CAS0}$−$\overline{CAS3}$ cycling t_{PC}=min.	—	710	—	650	mA	1, 3

Note : 1. I_{CC} in dependent on out put loading and cycle rates. Specified value are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}.

CAPACITANCE

(V_{CC} = 5V ± 5%, f = 1MHz, Ta = 9 ~ +70°C)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (A0 – A8)	C_{IN1}	–	161	pF
Input Capacitance ($\overline{WE}$)	C_{IN2}	–	193	pF
Input Capacitance ($\overline{RAS0}$ – $\overline{RAS3}$)	C_{IN3}	–	62	pF
Input Capacitance ($\overline{CAS0}$ – $\overline{CAS3}$)	C_{IN4}	–	62	pF
I/O Capacitance (DQ0–7, 9–16, 18–25, 27–34)	C_{DQ1}	–	29	pF
I/O Capacitance (DQ8, 17, 26, 35)	C_{DQ2}	–	39	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

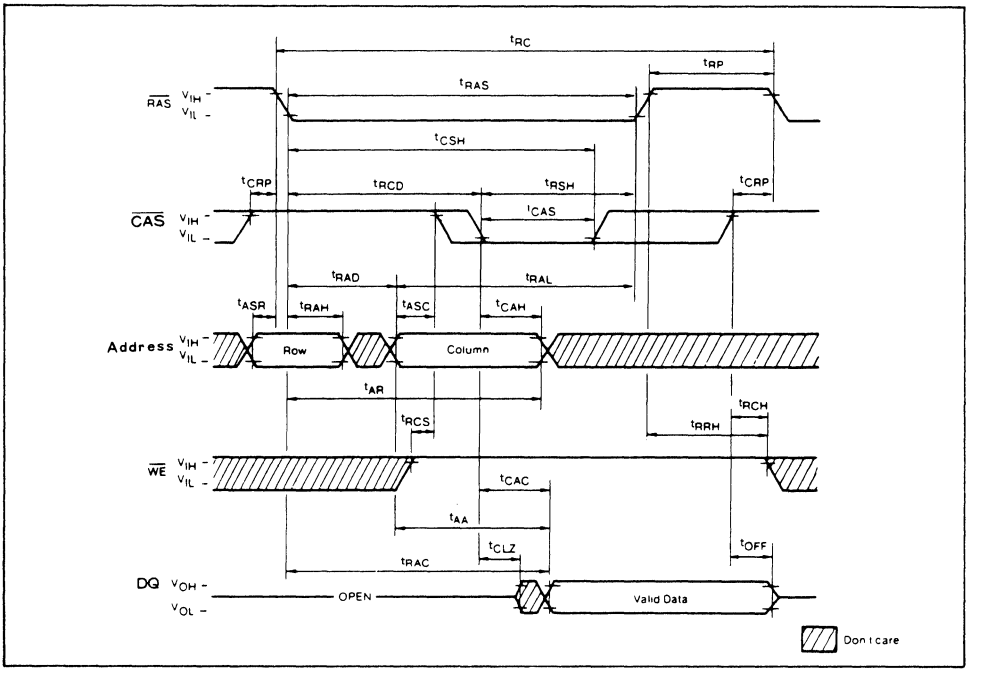
(V_{CC} = 5V ± 5%, Ta = 0 ~ +70°C)

Parameter	Symbol	MSC2321A-80YS18		MSC2321A-10YS18		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	ns	2, 7
Access time from $\overline{CAS}$	t_{CAC}	—	20	—	25	ns	2, 7
Access time from column address	t_{AA}	—	40	—	50	ns	2, 8
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	45	—	50	ns	2
$\overline{CAS}$ to output in Lo-Z	t_{CLZ}	0	—	0	—	ns	2
Output buffer turn-off delay	t_{OFF}	0	20	0	20	ns	3
Transition time (Rise and Fall)	t_T	3	50	3	50	ns	1
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	—	25	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	7
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	8
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	ns	
$\overline{CAS}$ precharge time (Fast page mode)	t_{CP}	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	12	—	15	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	ns	
Column address hold time refer. to $\overline{RAS}$	t_{AR}	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	ns	
Read command set-up	t_{RCS}	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	ns	4
Read command hold time refer. to $\overline{RAS}$	t_{RRH}	10	—	10	—	ns	4
Write command hold time	t_{WCH}	15	—	20	—	ns	
Write command hold time refer. to $\overline{RAS}$	t_{WCR}	60	—	75	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	ns	
Date set-up time	t_{DS}	0	—	0	—	ns	5
Date hold time	t_{DH}	15	—	20	—	ns	5
Date hold time referenced to $\overline{RAS}$	t_{DHR}	60	—	75	—	ns	
Refresh period	t_{REF}	—	8	—	8	ms	
Write command set-up time	t_{WCS}	0	—	0	—	ns	6
$\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CSR}	10	—	10	—	ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	t_{CHR}	30	—	30	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	ns	

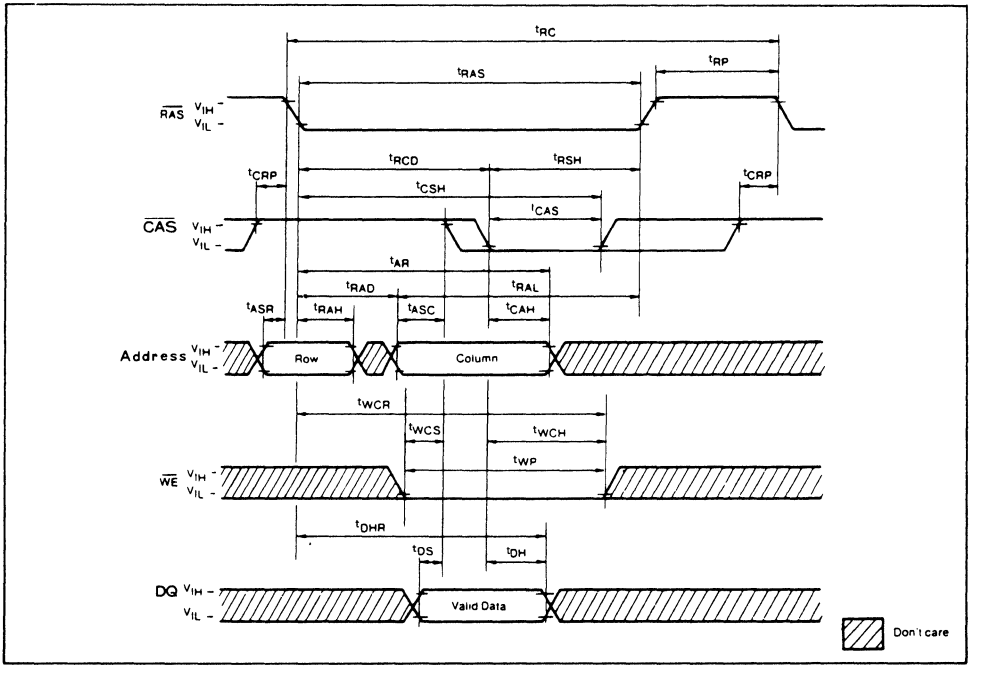
NOTES :

1) AC measurements assume t_T =5ns.
2) Measured with a load equivalent to 2 TTL loads and 100pF.
3) t_{OFF} (max) defines the time at which the output achieves an open circuit condition.
4) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5) These paramenters are referenced to $\overline{CAS}$ leading edge.
6) t_{WCS} is not a restrictive operating parameter. Tis is included in the data sheet as electrical characteristic only. If $t_{WCS} > t_{WCS}$ (min), the cycle is and early write cycle and the data out pin will remain as open circuit (Hi-Z)
7) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only : if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
8) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only : if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

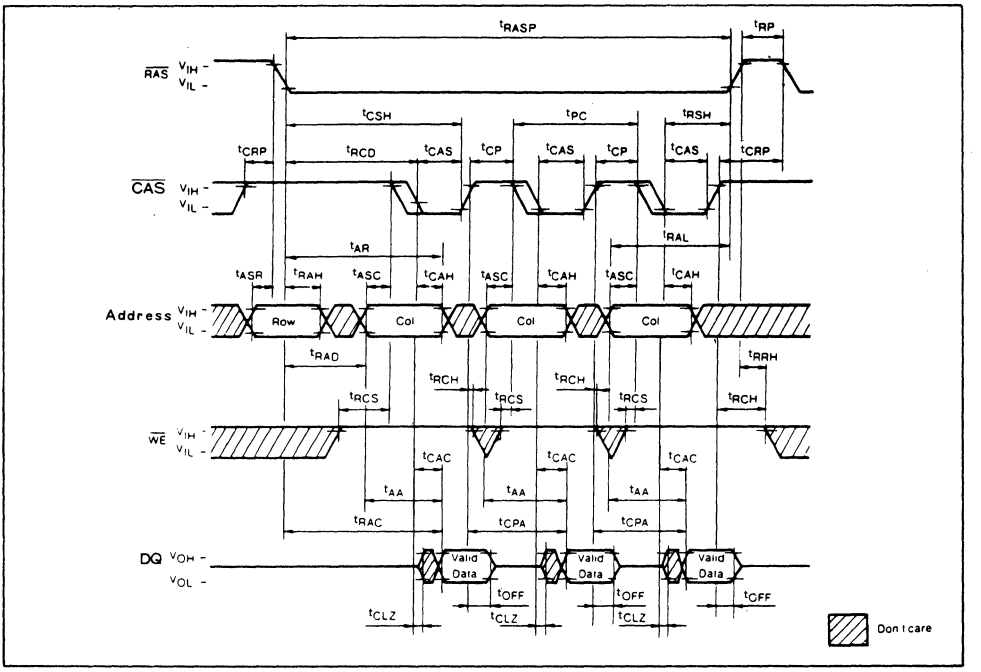
● READ CYCLE



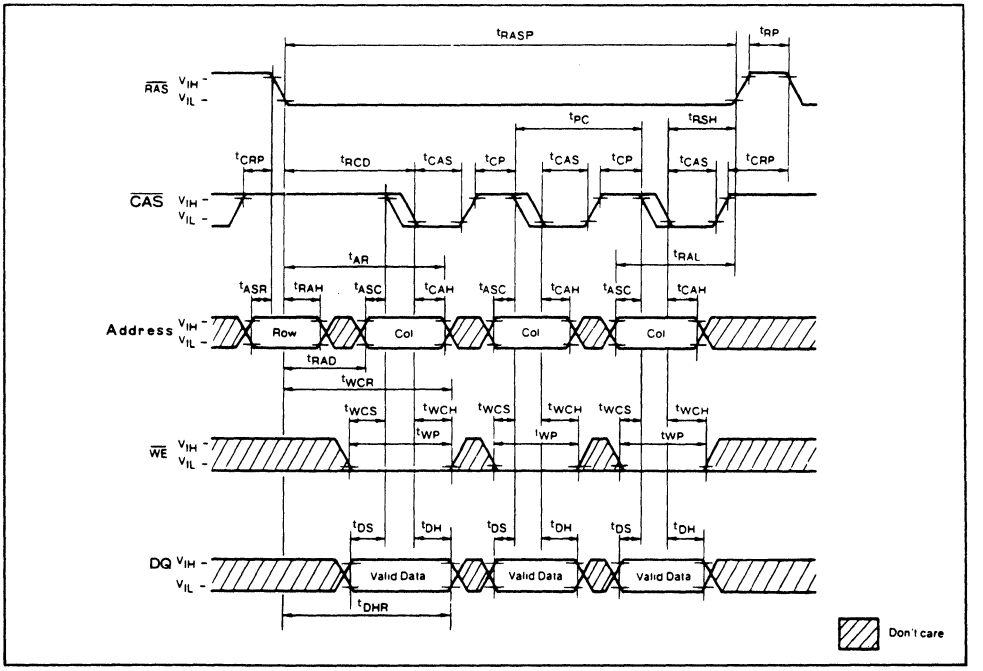
● WRITE CYCLE (EARLY WRITE)



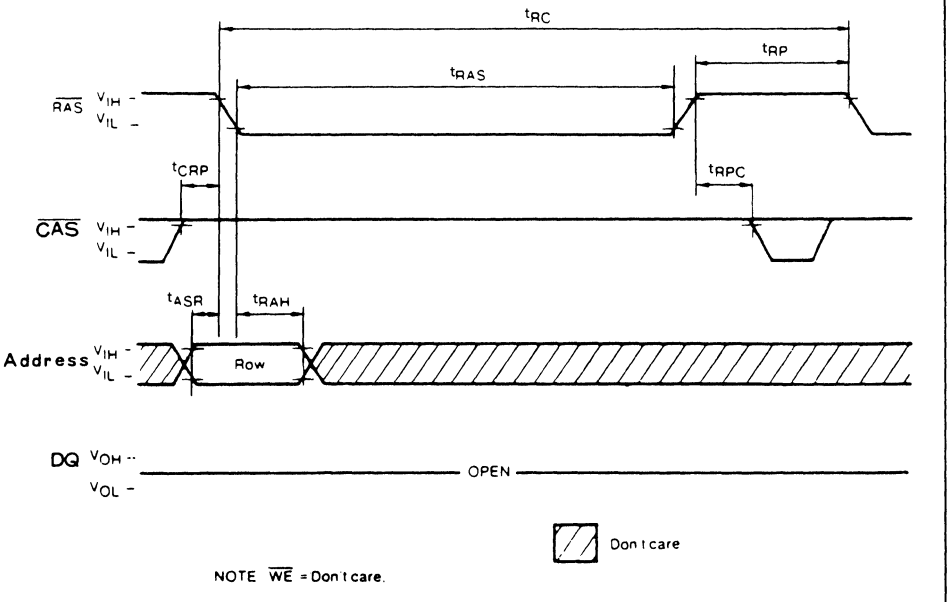
● FAST PAGE MODE READ CYCLE



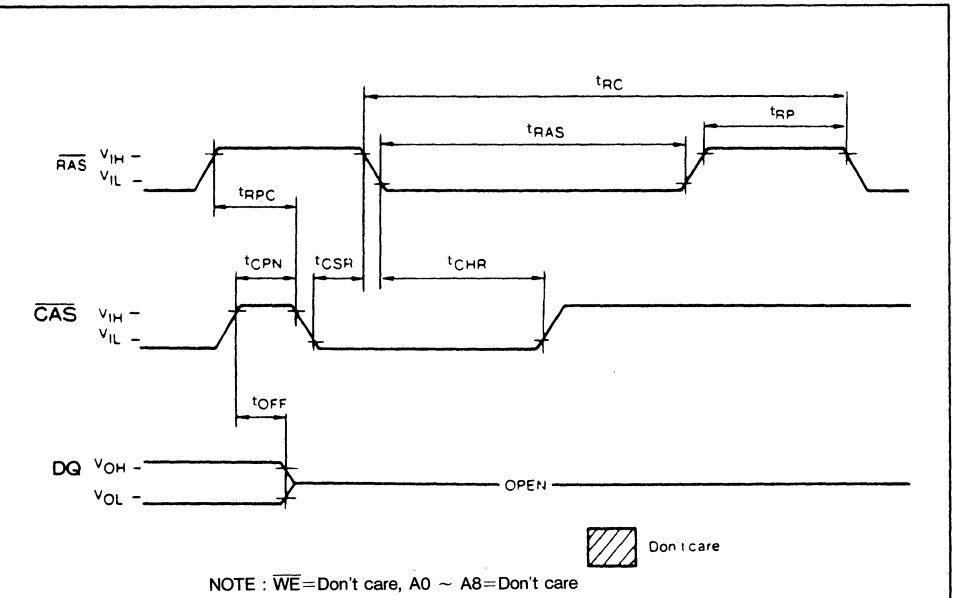
● FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



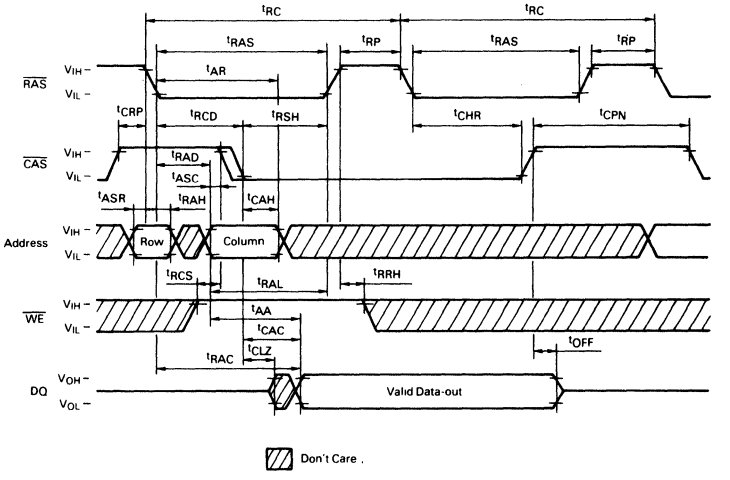
● $\overline{RAS}$ ONLY REFRESH CYCLE



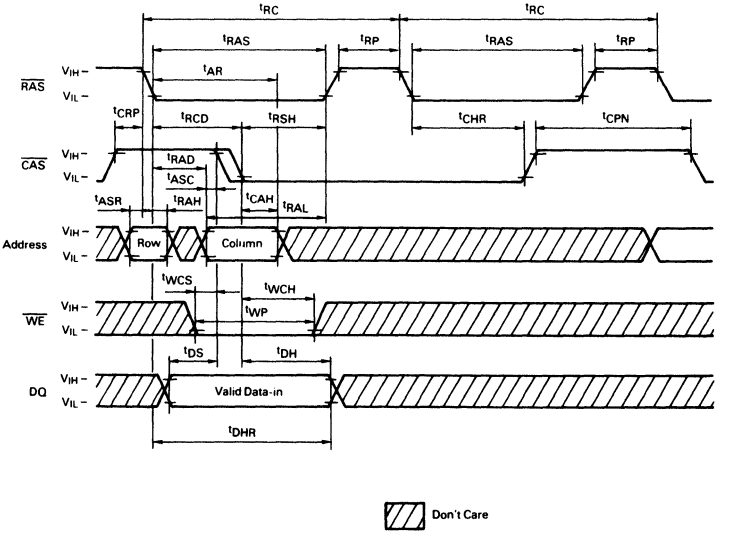
● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



● HIDDEN REFRESH READ CYCLE



● HIDDEN REFRESH WRITE CYCLE



OKI semiconductor
MSC2355-xxYS12

1,048,576 Word x 36 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2355-xxYS12 is a 1,048,576 word by 36 bit dynamic Random Access Memory (RAM) Module which is comprised of eight pieces of the MSM514400 and four pieces of the MSM511000A mounted on a SIMM printed circuit board. The MSC2355-xxYS12 is a fully decoded SIMM module constructed using Oki's proprietory silicon gate CMOS process. The MSC2355-xxYS12 has been designed for use in systems where high density, large capacity memory is required. This includes applications such as PC main memory, work stations and computer graphics.

FEATURES

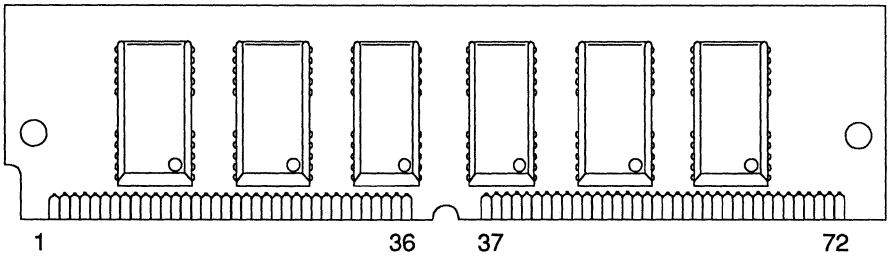
- 1,048,576 word × 36 bit organization
- 72-pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}		Operating (MAX)	Standby (MAX)
MSC2355-80YS12	80ns	40ns	20ns	160ns	5355mW	63mW
MSC2355-10YS12	100ns	50ns	25ns	190ns	4725mW	(MOS level)

- Single +5V supply, ± 5% tolerance
- Input : TTL compatible
- Output : TTL compatible, triastate, nonlatch
- Refresh : 1024 cycles/16mS
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability

PIN CONFIGURATION

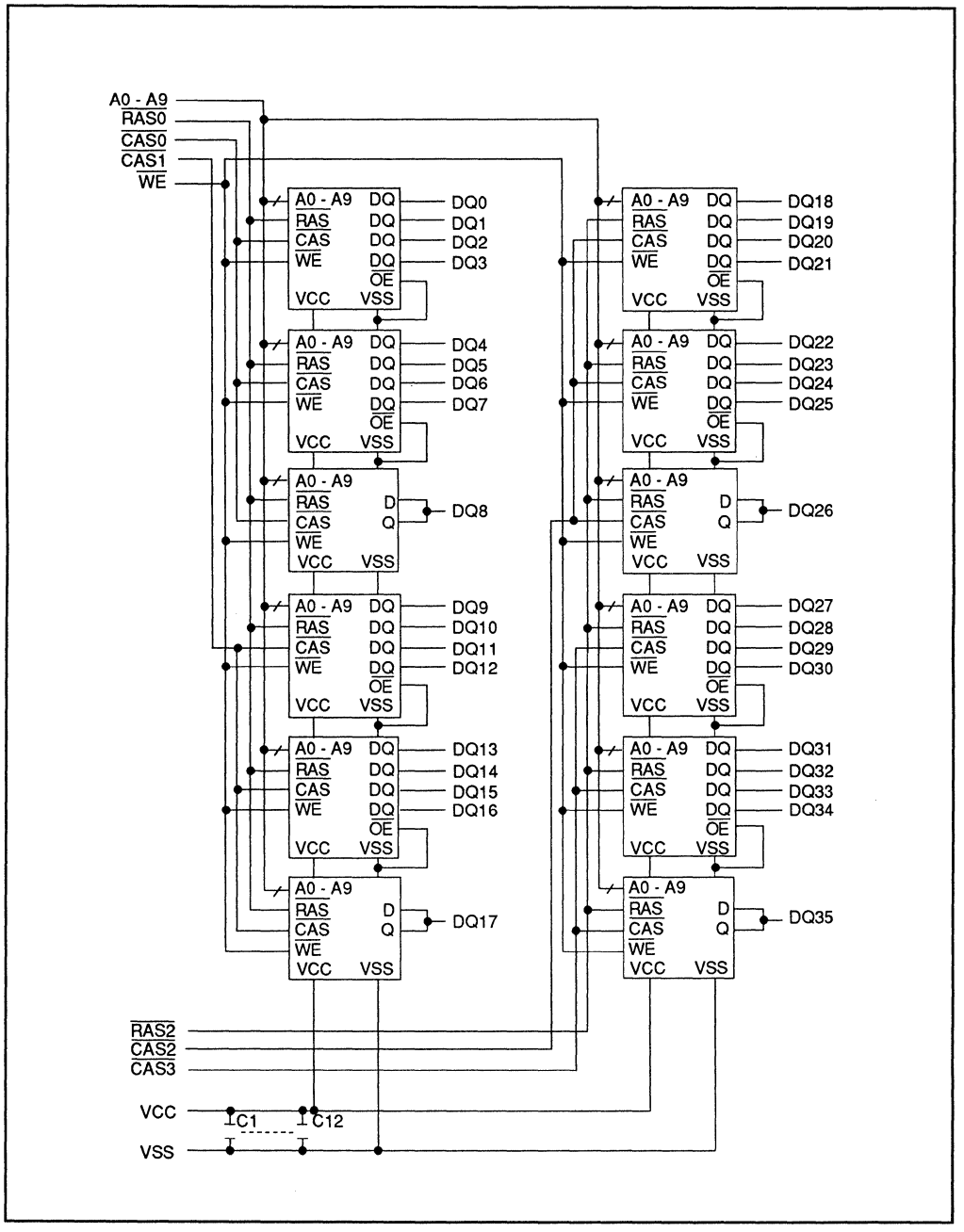
MSC2355-xxYS12



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	VSS	16	A4	31	A8	46	N.C.	61	DQ14
2	DQ0	17	A5	32	A9	47	$\overline{WE}$	62	DQ33
3	DQ18	18	A6	33	N.C.	48	N.C.	63	DQ15
4	DQ1	19	N.C.	34	$\overline{RAS2}$	49	DQ9	64	DQ34
5	DQ19	20	DQ4	35	DQ26	50	DQ27	65	DQ16
6	DQ2	21	DQ22	36	DQ8	51	DQ10	66	N.C.
7	DQ20	22	DQ5	37	DQ17	52	DQ28	67	PD0
8	DQ3	23	DQ23	38	DQ35	53	DQ11	68	PD1
9	DQ21	24	DQ6	39	VSS	54	DQ29	69	PD2
10	VCC	25	DQ24	40	$\overline{CAS0}$	55	DQ12	70	PD3
11	N.C.	26	DQ7	41	$\overline{CAS2}$	56	DQ30	71	N.C.
12	A0	27	DQ25	42	$\overline{CAS3}$	57	DQ13	72	VSS
13	A1	28	A7	43	$\overline{CAS1}$	58	DQ31		
14	A2	29	N.C.	44	$\overline{RAS0}$	59	VCC		
15	A3	30	VCC	45	N.C.	60	DQ32		

PIN No.	PIN NAME	MSC2355-80YS12	MSC2355-10YS12
67	PD0	N.C.	N.C.
68	PD1	N.C.	N.C.
69	PD2	N.C.	N.C.
70	PD3	N.C.	N.C.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	Ta = 25°C	−1.0 ~ +7.0	V
Voltage V_{CC} supply relative to V_{SS}	V_{CC}	Ta = 25°C	−1.0 ~ +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	12	W
Operating temperature	T_{opr}	–	0 ~ +70	°C
Storage temperature	T_{stg}	–	−40 ~ +125	°C

Notes: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Referenced to V_{SS}

Parameter	Symbol	MIN	TYP	MAX	Unit	Operating temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C ~ +70°C
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	–	6.25	V	
Input low voltage	V_{IL}	−1.0	–	0.8	V	

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	TYP	MAX	Unit
Input Capacitance (A0-A9)	C_{IN1}	65	80	pF
Input Capacitance ($\overline{WE}$)	C_{IN2}	60	75	pF
Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	C_{IN3}	35	50	pF
Input Capacitance ($\overline{CAS0}$-$\overline{CAS3}$)	C_{IN4}	20	30	pF
Input Capacitance (DQ0-7, 9-16, 18-25, 27-34)	C_{DQ1}	–	15	pF
I/O Capacitance (DQ8, 17, 26, 35)	C_{DQ2}	12	20	pF

Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

(Vcc = 5V ±5%, Ta = 0 ~ +70°C)

Parameter	Symbol	Conditions		MSC2355-80YS12 MIN.	MSC2355-80YS12 MAX.	MSC2355-10YS12 MIN.	MSC2355-10YS12 MAX	Unit	Note
Input leakage current	I_{LI}	0V ≤ V_{IN} ≤ 6.25V; all other pins not under text = 0V		–120	120	–120	120	µA	
Output leakage current	I_{LO}	DQ0–35 = disable 0V ≤ V_{OUT} ≤ 5.25V		–10	10	–10	10	µA	
Output high voltage	V_{OH}	I_{OH} = –5.0mA		2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA		0	0.4	0	0.4	V	
Average power supply current (operating)	I_{CC1}	$\overline{RAS0}$, $\overline{RAS2}$, $\overline{CAS0}$–$\overline{CAS3}$ cycling t_{RC} = min		–	1020	–	900	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS0}$, $\overline{RAS2}$ = V_{IH} $\overline{CAS0}$-$\overline{CAS3}$ = V_{IH}	TTL	–	24	–	24	mA	
		DQ0–35 = Hz	MOS	–	12	–	12		
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS0}$, $\overline{RAS2}$ cycling $\overline{CAS0}$–$\overline{CAS3}$ = V_{IH} t_{RC} = min		–	1020	–	900	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS0}$, $\overline{RAS2}$ = V_{IH} $\overline{CAS0}$–$\overline{CAS3}$ = V_{IL} DQ0-35 = enable		–	60	–	60	mA	1
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS0}$, $\overline{RAS2}$ cycling		–	1020	–	900	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS0}$, $\overline{RAS2}$ = V_{IL} $\overline{CAS0}$–$\overline{CAS3}$ = cycling t_{pc} = min		–	880	–	780	mA	1, 3

Note: 1. Icc is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC CHARACTERISTICS

(Vcc = 5V ±5%, Ta = 0 ~ +70°C)

Note 1, 2, 3

Parameter	Symbol	MSC2355-80YS12		MSC2355-10YS12		Unit	Notes
		Min.	Max.	Min.	Max.		
Random read or write cycle time	t_{RC}	160	–	190	–	ns	
Fast page mode cycle time	t_{PC}	55	–	65	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4.5
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4.5
Access time from column address	t_{AA}	–	40	–	50	ns	4.6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	55	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay time	t_{OFF}	0	20	0	25	ns	7
Transition time	t_T	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ prechage time	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2355-80YS12		MSC2355-10YS12		Unit	Notes
		Min.	Max.	Min.	Max.		
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
Write command set-up time	t_{WCS}	0	–	0	–	ns	
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	–	20	–	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	20	–	20	–	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	20	–	20	–	ns	

Notes: 1. An initial pause of 200 μs is required after power-up followed by a minimum of eight initializatiojn cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume t_T = 5 ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2 TTL loads and 100pF.

5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

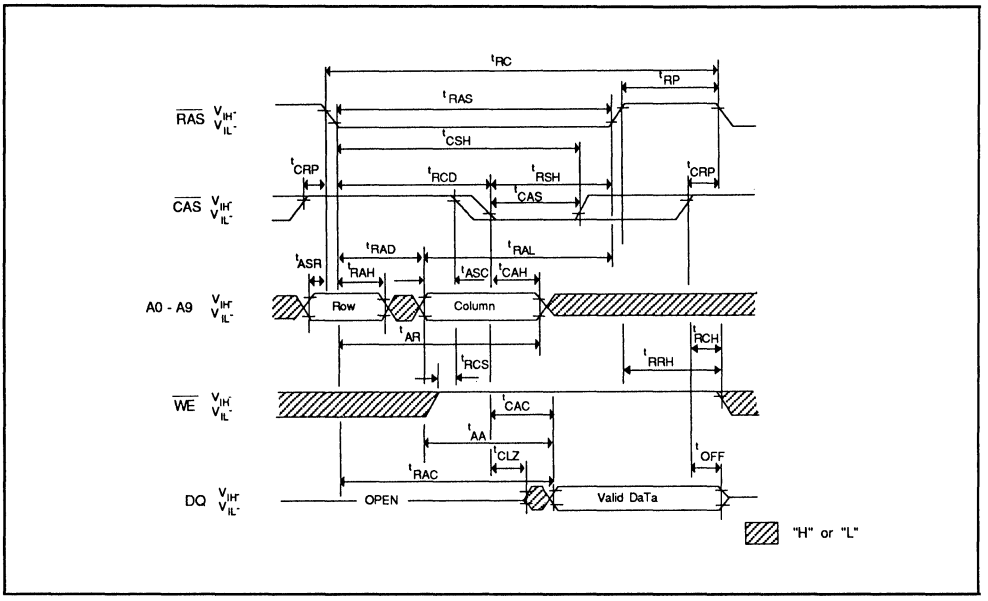
7. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levewls.

8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

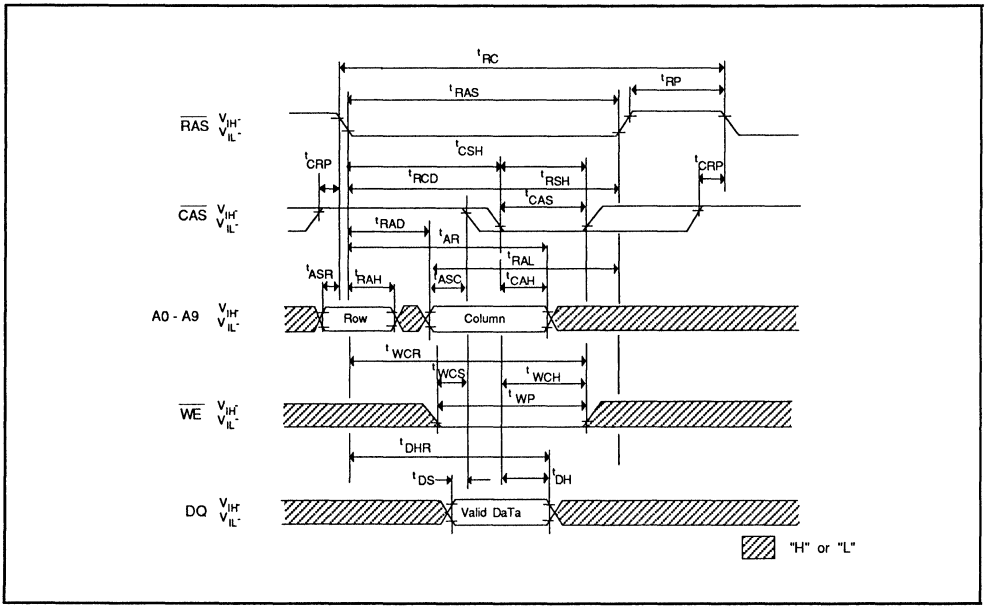
9. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remains in effect untill the exit cycle is generated.
The test mode specified in this data sheet is 8-bit parallel test function.
RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are not equal, then the data output pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

10. In a test mode read cycle, the value of an access time parameters is delayed by 5ns from the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

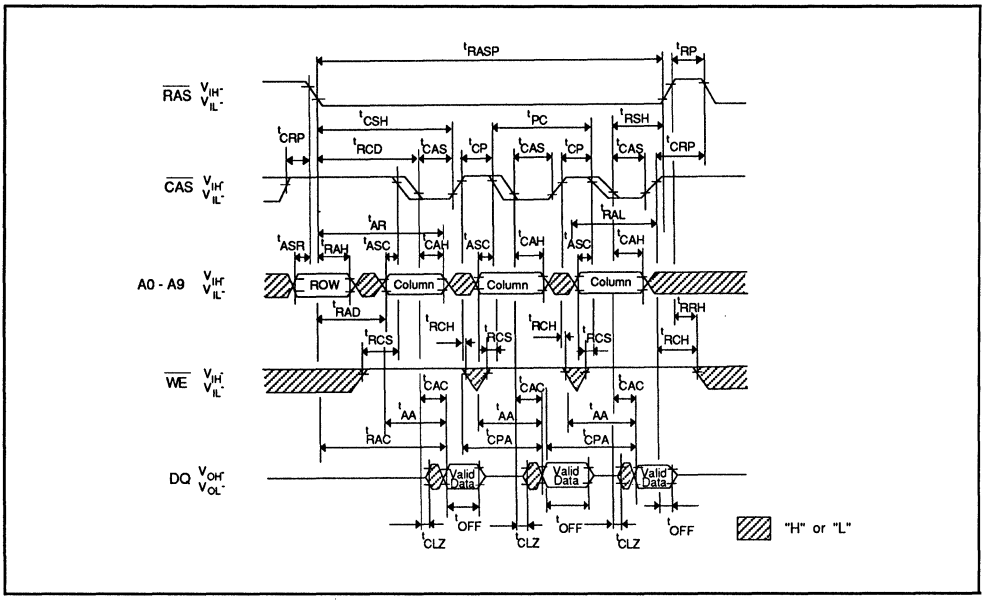
• READ CYCLE



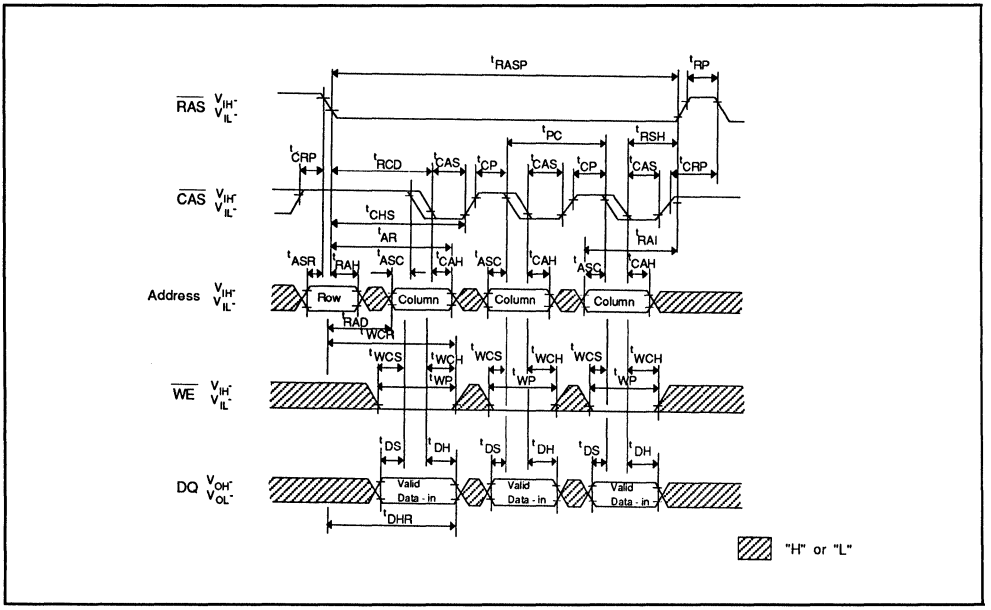
• WRITE CYCLE (EARLY WRITE)



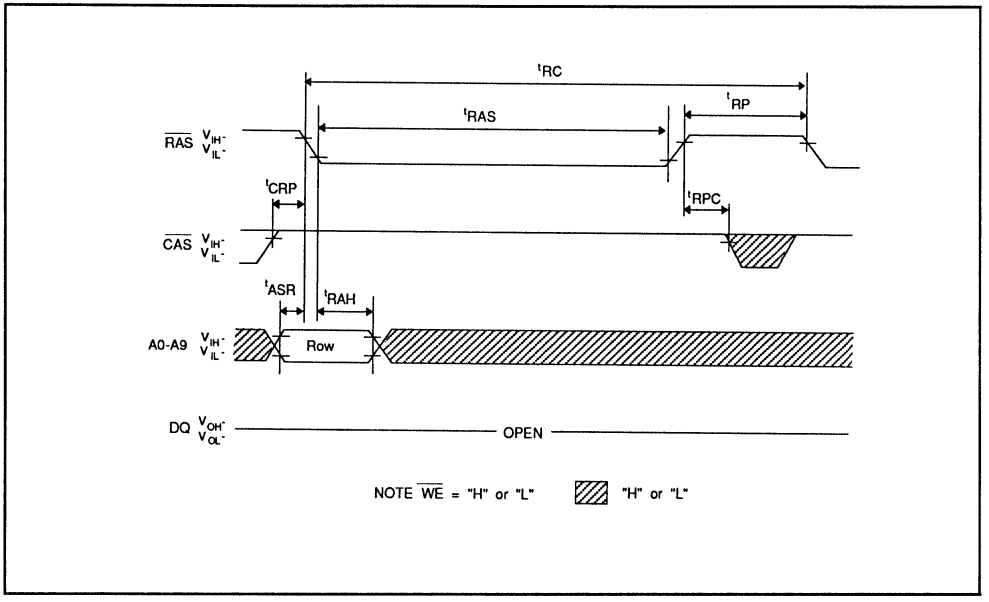
● FAST PAGE MODE READ CYCLE



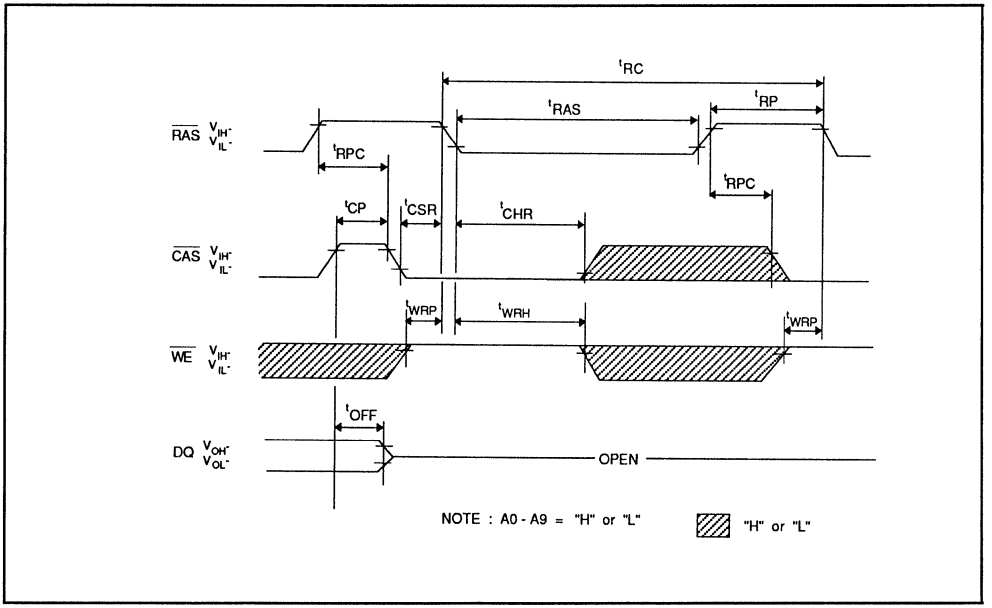
● FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



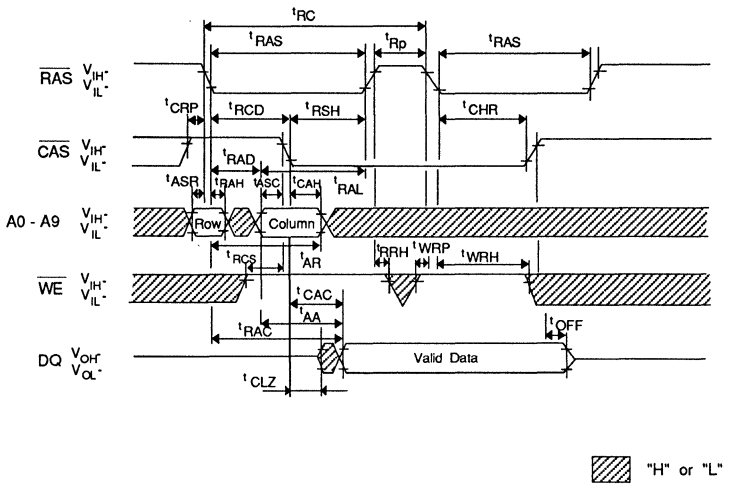
• $\overline{RAS}$ ONLY REFRESH CYCLE



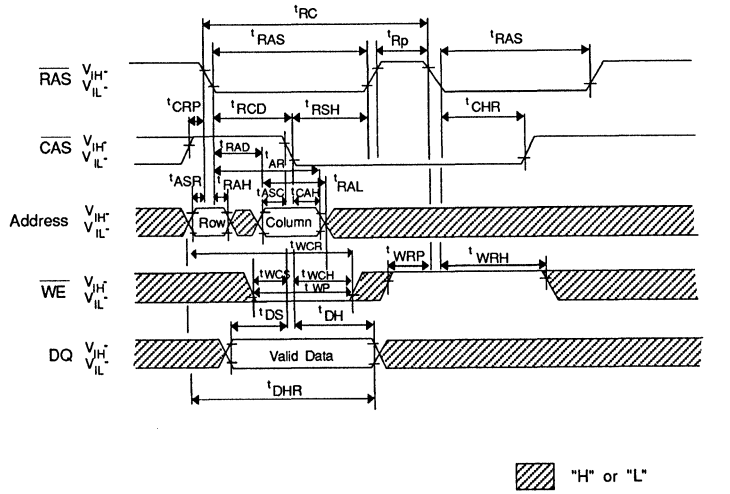
• $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



● HIDDEN REFRESH READ CYCLE



● HIDDEN REFRESH WRITE CYCLE



NOTICE

1. The information contained herein can change without notice owing to product and/or technical improvements. Please make sure before using the product that the information you are referring to is up-to-dated.

2. The outline of action and examples of application circuits described herein have been chosen as an explanation of the standard action and performance of the product. When you actually plan to use the product, please ensure that the outside conditions are reflected in the actual circuit and assembling designs.

3. NO RESPONSIBILITY IS ASSUMED BY US FOR ANY CONSEQUENCE RESULTING FROM ANY WRONG OR IMPROPER USE OR OPERATION, ETC. OF THE PRODUCT.

4. Neither indemnity against nor license of a third party's industrial and intellectual property right, etc. is granted by us in connection with the use of the product and/or the information and drawings contained herein. No responsibility is assumed by us for any infringement of a third party's right which may result from the use thereof.

5. The products described herein falls within the category of strategical goods, etc. under the Foreign Exchange and Foreign Trade Control Law. Accordingly, before exporting the product you are required under the Law to file the application for the export license by your local Government.

6. No part of the contents contained herein may be reprinted or reproduced without our prior permission.

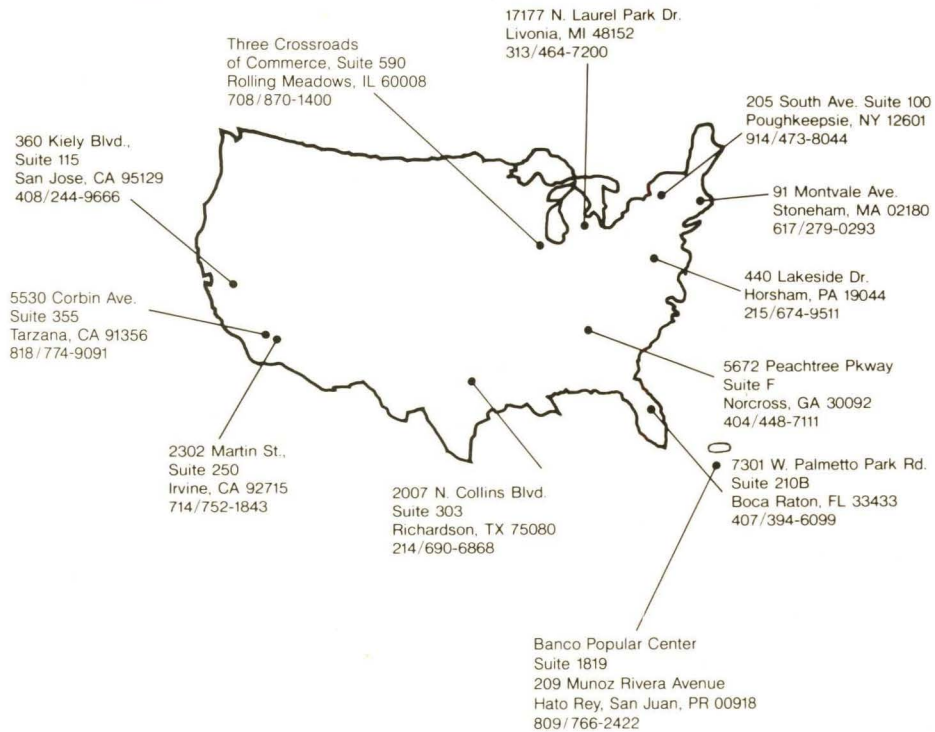
7. MS-DOS is a registered trademark of Microsoft Corporation.

OKI

Oki Semiconductor

785 North Mary Avenue, Sunnyvale, CA 94086, U.S.A. Tel: 408-720-1900 Fax: 408-720-1918

For further information please contact:



Oki Electric Industry Co., Ltd.
Head Office Annex
7-5-25 Nishishinjuku,
Shinjuku-ku, Tokyo 160, Japan
Tel: 3-5386-8100
Fax: 3-5386-8110
Telex: J27662 OKIDENED
Electronic Devices Group
Overseas Marketing Dept.

Oki Semiconductor
785 North Mary Avenue,
Sunnyvale, CA 94086, U.S.A.
Tel: 408-720-1900
Fax: 408-720-1918
Telex: 296687 OKI SNTA

Oki Electric Europe GmbH
Hellersbergstraße 2
D-4040 Neuss
Fed. Rep. of Germany
Tel: 2101-15960
Fax: 2101-103539
Telex: 8517427 OKI D

Oki Electronics (Hong Kong) Ltd.
Suite 1801-4, Tower 1,
China Hong Kong City,
33 Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: 3-7362336
Fax: 3-7362395
Telex: 45999 OKIHK HX

OKI SINCE 1881 REF NO.: E3S060061