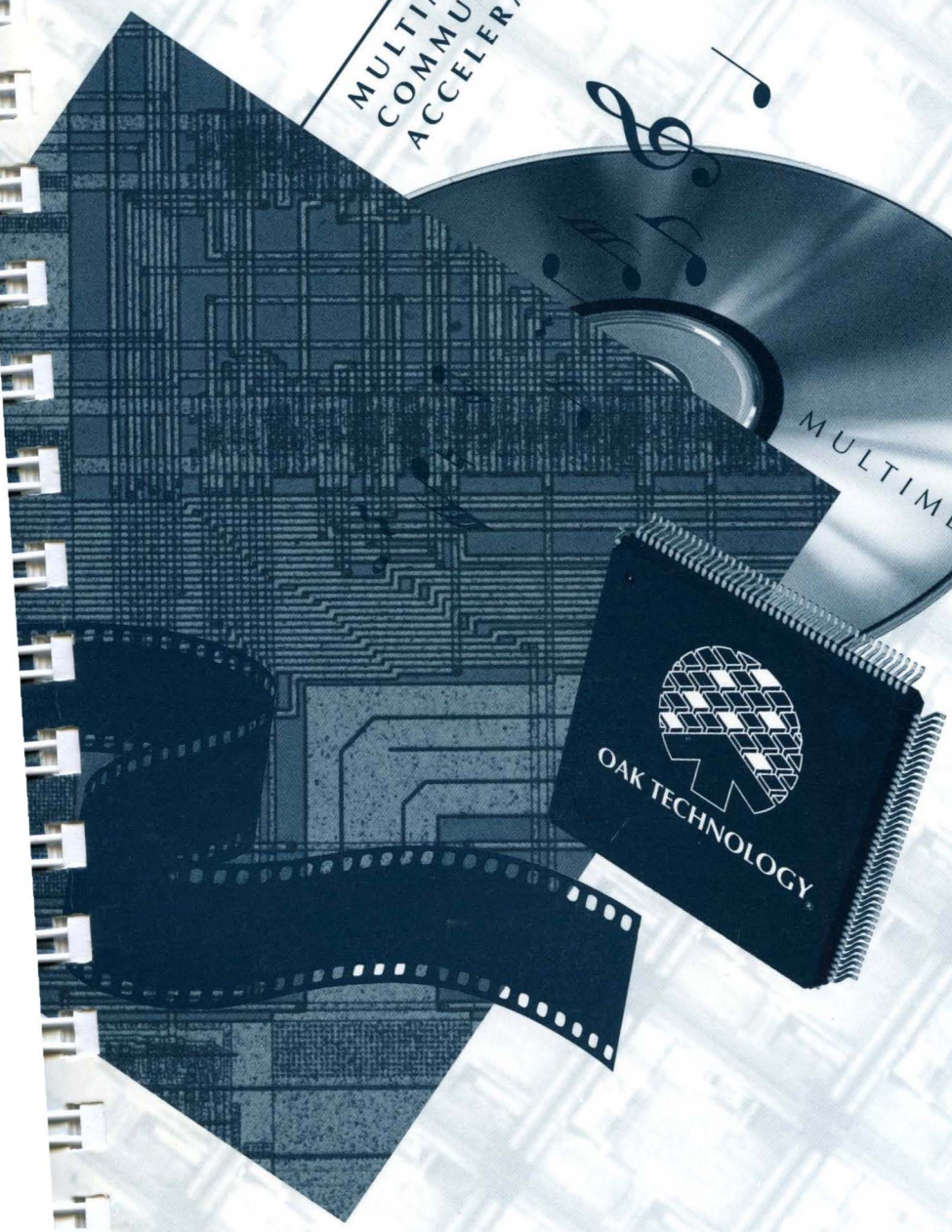
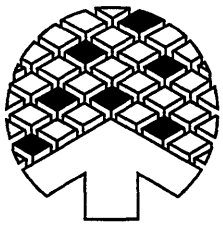
OAK TECHNOLOGY®

OTI-610
OTI-611

MULTIMEDIA AUDIO AND COMMUNICATIONS ACCELERATORS



MULTIMEDIA SOLUTIONS IN SILICON



OAK TECHNOLOGY®

OTI-610/OTI-611

Multimedia Audio and Communications Accelerators

Technical Specification

May 1997

Customer Feedback

Oak Technology welcomes your suggestions to improve the quality of our documentation. Please send your comments to:

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Printed in the U.S.A.

v. 003

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CHAPTER 1 OVERVIEW

1.1 FEATURES

1.1.1 OTI-610 FEATURES

- Provides high-performance multiple channel digital audio to Pentium-class systems
- Multiple digital audio channels with sample rate conversion on each channel
- Digital mixing of all channels
- Microsoft 2D DirectSound DSP-based hardware acceleration
- Supports multiple source DirectSound 3D positional sound (Head Related Transfer Function) using DSP hardware acceleration
- Sample rate conversion and mixing support of an I²S input port for uncompressed digital audio, such as MPEG-1 audio
- Meets the AC '97 (Audio Codec 1997) specification by meeting requirements for AC-Link
- Programmable DSP core for easy feature upgrades
- General MIDI wavetable music synthesizer with reverb and chorus
- MPU-401 MIDI port (IN and OUT)
- 32-bit PCI bus master support with scatter/gather

1.2 PRODUCT INTRODUCTION

The OTI-610 and OTI-611 controllers are PCI bus based audio and audio/communications devices designed to support multiple digital audio stream sample rate conversion, digital mixing, and playback. Both devices provide full duplex audio operation (simultaneous playback and record in stereo), and the OTI-611 has fax/data modem capability.

1.2.1 OTI-610 PCI AUDIO ACCELERATOR

The OTI-610, also known as the ***Audia3D™***, is a highly integrated audio accelerator that is suitable for motherboard and add-in card applications.

The OTI-610 supports major sound standards such as Microsoft Windows Sound System (WSS) software, Microsoft DirectSound, Microsoft DirectInput, and Microsoft's software emulated SoundBlaster Pro standards.

The OTI-610 DSP supports wavetable music synthesis (when used with external Sample Set ROM) or host signal processing (HSP) wavetable music synthesis. Both synthesizer types support the Musical Instrument Digital Interface (MIDI) interfaces. Both synthesizer types support the General MIDI (GM) compatible instrument set consisting of 128 instruments or sounds, each instrument or sound having its own instrument or "patch" number. The OTI-610 also supports a GM Drum Kit. Two audio effects, chorus and reverb, are also supported.

For the DSP synthesizer, up to 24 voices at 22.05 KHz are presented concurrently. Chorus and reverb operations require memory to delay the sample outputs to generate the effects. The OTI-610 implements a delay line memory by using system memory and the PCI bus. Chorus requires one delay buffer and reverb requires five.

For the HSP synthesizer, up to 32 voices at 22.05 KHz are presented concurrently. Chorus and reverb operations are implemented in system memory.

The OTI-610 incorporates direct interfaces to an audio codec, game and MIDI ports, external optional Wavetable Sample Set ROM, an I²S digital audio port for MPEG decoded digital audio, and the PCI bus.

1.1.2 OTI-611 FEATURES

- Provides high-performance multiple channel digital audio, modem, and fax capabilities to Pentium-class systems
- Multiple digital audio channels with sample rate conversion on each channel
- Digital mixing of all channels
- Microsoft 2D DirectSound DSP-based hardware acceleration
- Supports multiple source DirectSound 3D positional sound (Head Related Transfer Function) using DSP hardware acceleration
- Sample rate conversion and mixing support of an I²S input port for uncompressed digital audio, such as MPEG-1 audio
- V.34*bis*-compliant HSP fax/data modem
- Exceeds the AC '97 (Audio Codec 1997) specification by meeting requirements for AC-Link, plus providing an additional modem codec interface
- Programmable DSP core for easy feature upgrades
- General MIDI wavetable music synthesizer with reverb and chorus
- MPU-401 MIDI port (IN and OUT)
- 32-bit PCI bus master support with scatter/gather

1.2.2 OTI-611 PCI AUDIO AND COMMUNICATIONS ACCELERATOR

The OTI-611, also known as the ***TelAudia3D™***, is a highly integrated audio and communications accelerator suitable for motherboard and add-in card applications.

The OTI-611 supports major sound standards, including Microsoft Windows Sound System (WSS) software, Microsoft DirectSound, Microsoft DirectInput, and Microsoft's software-emulated SoundBlaster Pro standards.

The OTI-611 DSP supports wavetable music synthesis (when used with external sample set ROM) or host signal processing (HSP) wavetable music synthesis. Both synthesizer types support the Musical Instrument Digital Interface (MIDI) interfaces. Both synthesizer types support the General MIDI (GM) compatible instrument set consisting of 128 instruments or sounds, each instrument or sound having its own instrument or "patch" number. The OTI-611 also supports a GM Drum Kit. Two audio effects, chorus and reverb, are supported.

For the DSP synthesizer, up to 24 voices at 22.05 KHz are presented concurrently. Chorus and reverb operations require memory to delay the sample outputs to generate the effects. The OTI-611 implements a delay line memory by using system memory and the PCI bus. Chorus requires one delay buffer and reverb requires five.

For the HSP synthesizer, up to 32 voices at 22.05 KHz are presented concurrently. Chorus and reverb operations are implemented in system memory.

The OTI-611 supports an HSP-based, fully compliant V.34 (28.8 Kbps) and V.34+ (33.6 Kbps) data, and V.29, V.17, and V.27*ter* fax modem operation, including V.42 LAPM & MNP 2-4 error detection and correction and V.42*bis* & MNP 5 data compression.

The OTI-611 incorporates direct interfaces to an audio codec and/or modem codec, (or combination thereof), game and MIDI ports, external optional Wavetable Sample Set ROM, an I²S digital audio port (for MPEG decoded digital audio), and the PCI bus.

1.3 ARCHITECTURE

The OTI-610 and OTI-611 share a common PCI bus master interfaced, RAM-based DSP architecture for support of the features listed on pages 1-1 and 1-2. The OTI-610 and OTI-611 provide 10 bus master channels. Channels 0 through 7 are used for playback of digital audio. Channel 8 is used for recording of digital audio. Channel 9 is reserved for use with the DSP-based wavetable synthesizer.

The OTI-610 and OTI-611 also provide support for an HSP-based wavetable synthesizer and General MIDI Sound Sample Set, which utilizes one digital audio channel playback channel.

The ROM interface provides an interface to an optional external 2MB ROM, which is used for storing a GM Sound Sample Set if the optional DSP-based GM wavetable synthesizer is used.

The audio codec interface within the OTI-610 and OTI-611 provides direct connections to different types of audio codecs, depending upon external jumper settings, which are read during power up and stored in a status register.

The OTI-611 offers additional functionality over the OTI-610 by providing hardware support for an HSP-based V.34 fax/modem in the form of transmit and receive buffers, and modem codec and DAA interfaces. The OTI-611 also provides direct connections to different types of modem codecs, depending upon external jumper settings, which are read during power up and stored in a Status register.

Simplified block diagrams for the OTI-610 and OTI-611 are shown in Figures 1-1 and 1-2. More detailed block diagrams are shown in Figures 1-3 and 1-4.

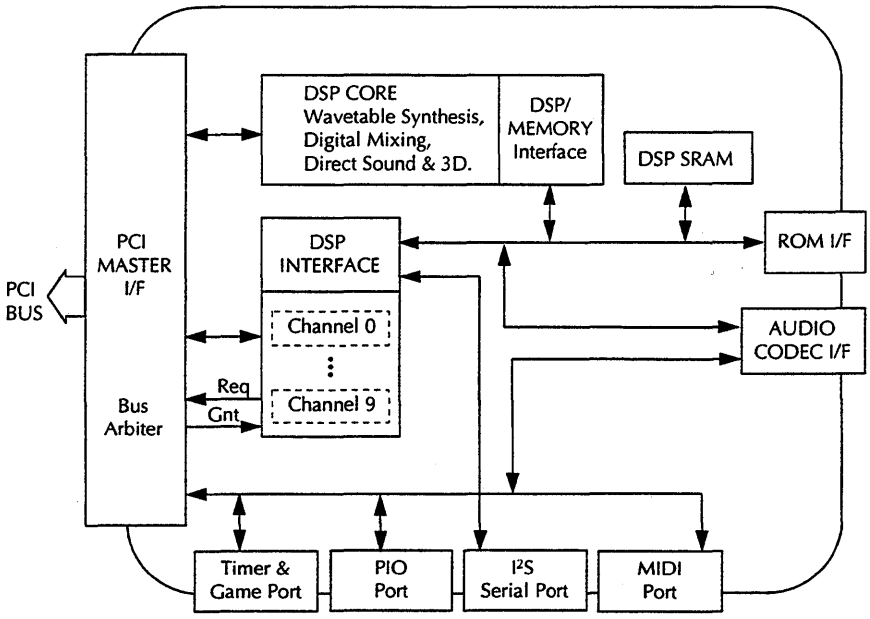

Figure 1-1: *OTI-610 Simplified Block Diagram*

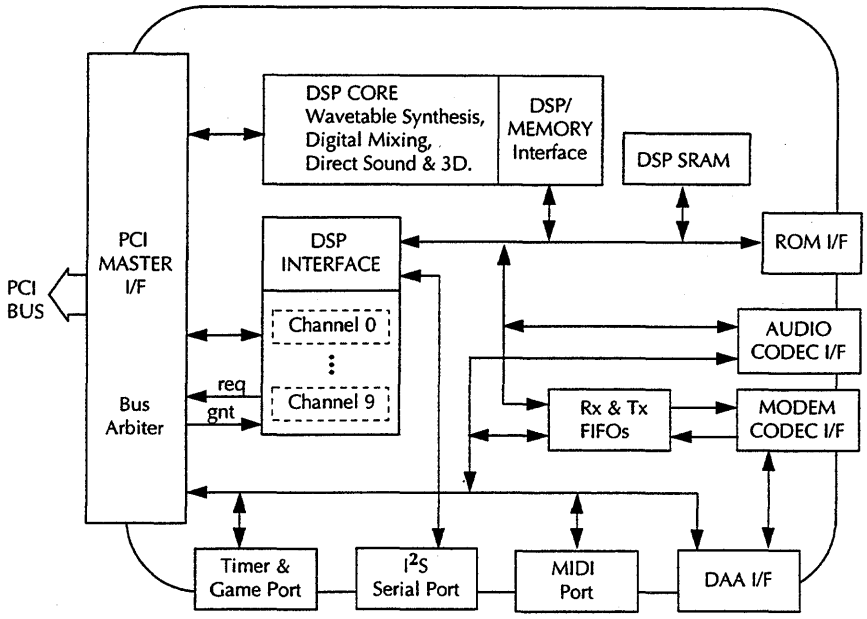

Figure 1-2: *OTI-611 Simplified Block Diagram*

1.4 BLOCK DIAGRAM DESCRIPTIONS

Figure 1-3 gives a more detailed block diagram of the OTI-610 audio accelerator, and Figure 1-4 gives a more detailed block diagram of the OTI-611 audio and communications accelerator.

1.4.1 DIGITAL SIGNAL PROCESSOR

The core of the OTI-610 and OTI-611 is a dedicated high-speed, RAM-based digital signal processor (DSP) tailored for audio applications. Its three-bus architecture and logic design allow program memory, data memory, and coefficient memory all to be accessed on a single cycle. The DSP of the OTI-610 and OTI-611 features all the instructions commonly used in other DSP chips, plus special instructions to speed up certain audio operations, such as wavetable synthesis with effects, sample rate conversion, and digital mixing.

The OTI-610 and OTI-611 DSPs have the following features:

- A tightly coupled interface between the DSP and PCI bus master
- Three sets of internal static random access memory (SRAM): 5Kx24 words, 4Kx16 words, and 2Kx16 words
- Single-cycle computation for all functions, including multiplier/accumulator (MAC)
- Single-cycle fetch of one opcode and two operands
- Single-cycle context switching
- Zero overhead looping and branching
- Three clock latency values to handle interrupts

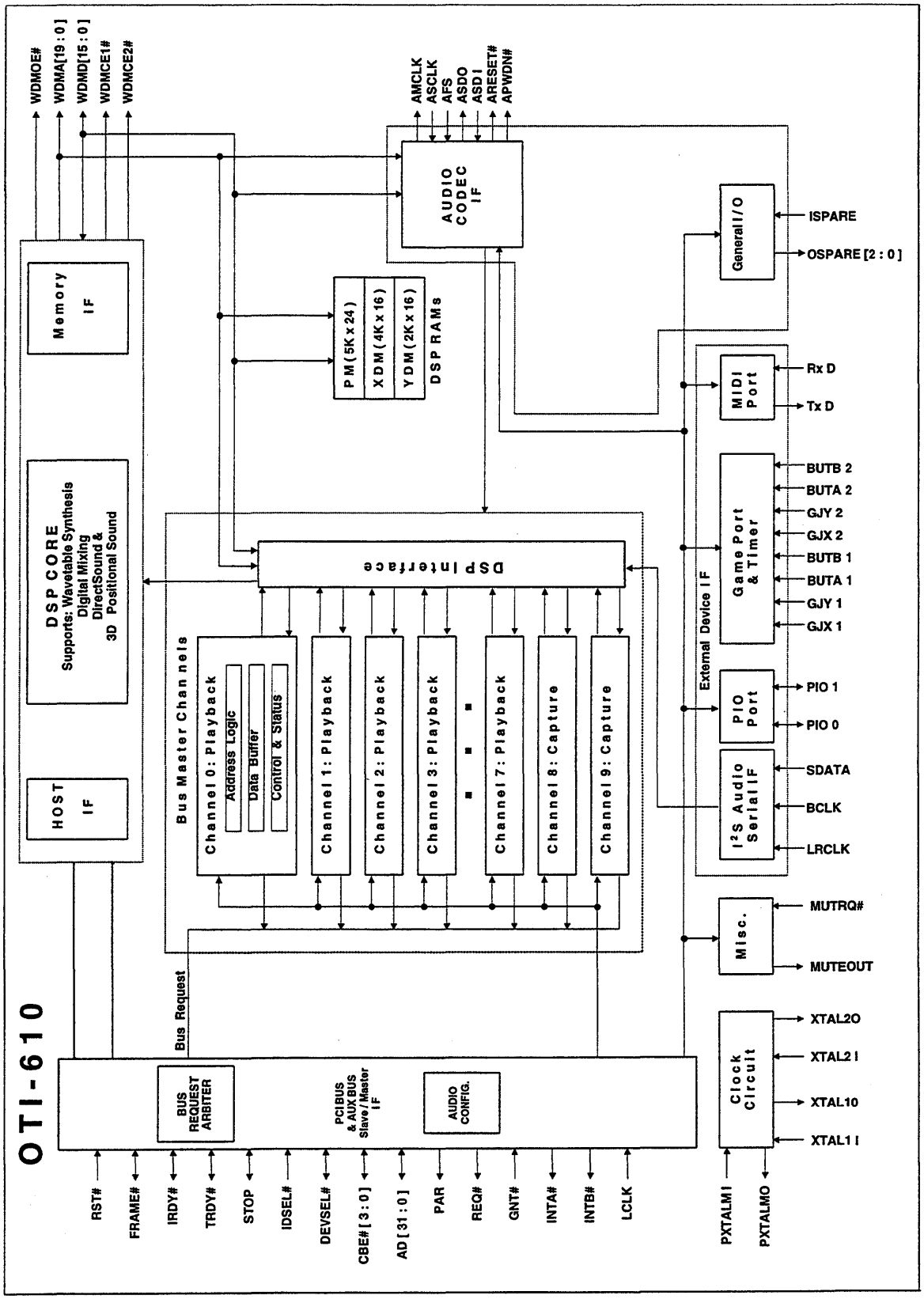

Figure 1-3: *OTI-610 Expanded Block Diagram*

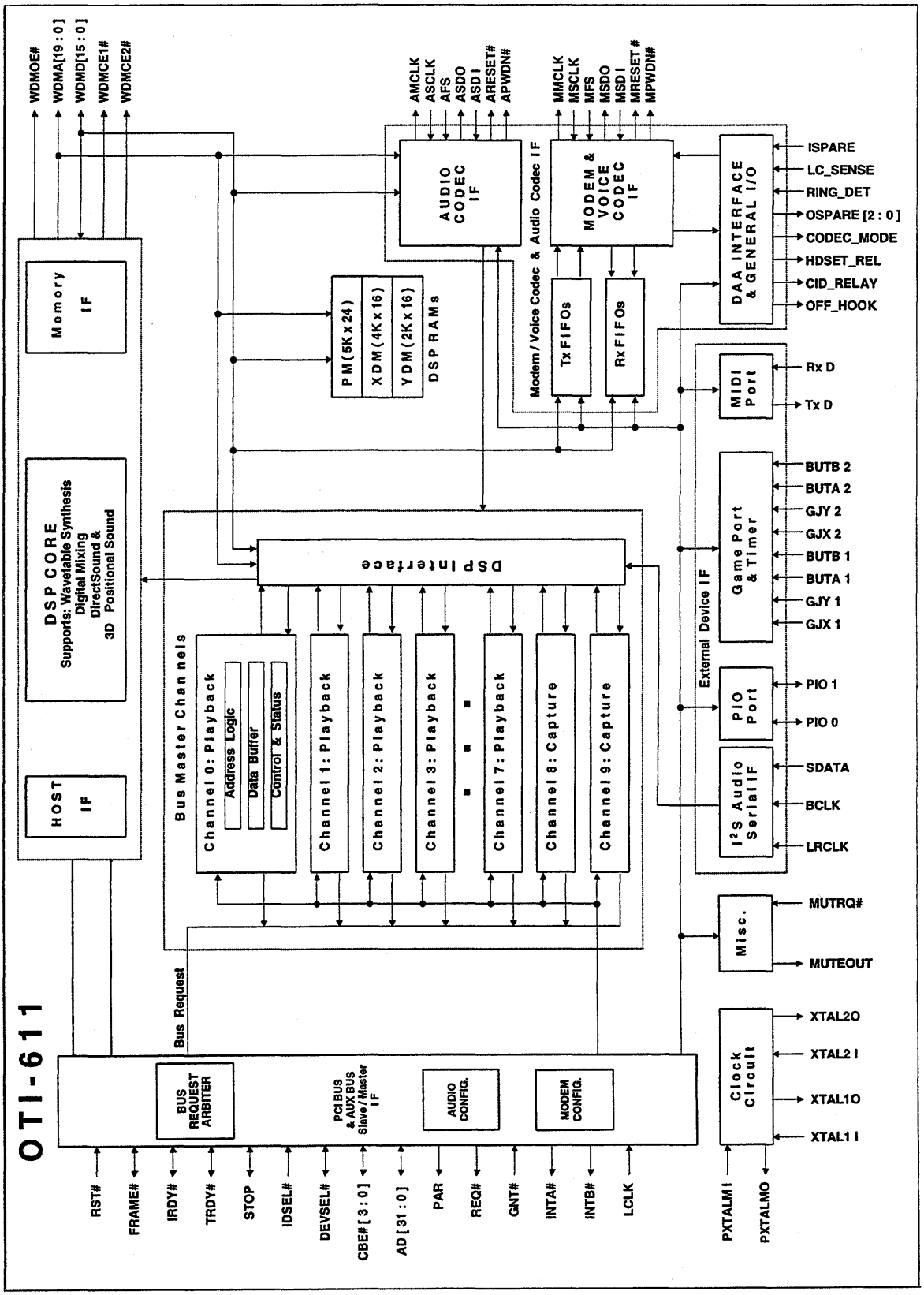

Figure 1-4: *OTI-611 Expanded Block Diagram*

- Extended dynamic range — includes 40-bit accumulator
- External ROM memory space support — up to 2MB — through an internal base address register
- Parallel host interface port (HIP) for faster and more flexible communications with the host system
- Timing-adjustable external memory interface
- 36 Mips speed performance
- Special instructions for commonly used audio operations
- Zero wait states for external memory access, if special coding rules are followed

1.4.2 EXTERNAL DEVICE INTERFACE

The OTI-610 and OTI-611 external device interface (EDI) includes the following sub-blocks:

- MIDI port
- Game port
- Digital, serial I^2S audio interface
- Programmable input/output port
- Audio codec interface
- Modem codec interface (OTI-611 only)
- DAA interface (OTI-611 only)

1.4.3 MIDI PORT

MIDI information is passed by using two pins connected to an internal universal asynchronous receiver transmitter (UART) — one pin for receiving and one for transmitting.

The hardware implementation is MPU-401 compatible when used with a standard MIDI adapter and game cable, and is capable of full duplex transmission and reception.

The transmission rate is fixed at 31.25 KHz, per the MIDI Specification.

Two 16x8 FIFOs are used for MIDI data buffering — one for receiving and one for transmitting.

For more information on the MIDI interface, refer to Chapter 4, Section 4.1.

1.4.4 GAME PORT

The game port interface uses an analog timer, which is NE558-compatible in operation. The port interfaces with analog joysticks, which are used for computer game programs.

A typical application constantly polls the game port, up to 90 times per second, when the analog joystick is selected. To conserve CPU power, the OTI-610/OTI-611 has hardware to check the game port for data and immediately puts the data into a register for the CPU to read. This speeds up the game port operation. Driver support is required to take advantage of this feature.

For more information on the game port interface, refer to Chapter 4, Section 4.2.

1.4.5 I^2S INPUT PORT

The OTI-610 and OTI-611 provide an interface to the external digital serial audio. The serial audio data, like decoded MPEG audio output, can be input and then mixed with all sound sources from the host.

For more information on the I^2S interface, refer to Chapter 4, Section 4.3.

1.4.6 PROGRAMMABLE INPUT/OUTPUT PORT

The OTI-611 provides two software-controlled PIO interface pins, which can be used as general I/O pins to interface with external devices. Alternatively, these pins may be software programmed to implement a simple I^2C serial bus protocol for communication to a single I^2C device.

For more information on the programmable I/O interface, refer to Chapter 4, Section 4.4.

1.4.7 MODEM/VOICE AND AUDIO CODEC INTERFACES

The modem/voice and audio codec interfaces provide the following functions for both the OTI-610 and OTI-611, except where noted:

- Transmit/receiving buffers (FIFO) management, including interrupt generation and modem codec interface for fax/modem operation (OTI-611 only).
- The OTI-610 provides one interface port for an external audio codec. The codec interface will convert the audio codec serial data to parallel data for digital audio data capture and will convert digital audio parallel data to serial data for playback through the audio codec. Chapter 3 provides complete information on codec support for the OTI-610.
- The OTI-611 provides two interface ports, one for an external audio codec and one for an external modem codec. Alternatively, by setting a Codec Selection register, these ports can be used in different configurations to support multiple types of audio and modem codecs. In either case, the codec interfaces receive data through their serial ports. The codec interface will convert the codec serial data to parallel data for capture/receiving and parallel data to serial data for playback/transmitting. Chapter 3 provides complete information on codec support for the OTI-611.
- AC-Link interface support (which is required for AC '97 compliant audio codecs, or AC '97 compliant dual audio and modem codecs): The OTI-610 and OTI-611 provide an AC-Link interface. The OTI-610 AC-Link interface will operate correctly only with AC '97 audio codecs. The OTI-611 AC-Link interface will operate correctly with either AC '97 audio codecs (audio data only to the codec) or an AC '97 audio/modem codec (audio and modem data to the codec).

For more information on the codec interface, refer to Chapter 4, Section 4.5.

1.4.8 DAA INTERFACE (OTI-611 ONLY)

The OTI-611 provides multiple signals for direct connection to fax/data modem DAA structures. When used with the HSP V.34/V.34+ fax/data modem software supplied with the OTI-611 and an appropriate modem codec, a complete fax/data modem may be built.

In addition, programmable, uncommitted input and output pins are also available for additional flexibility in the modem system design.

For more information on the DAA interface, refer to Chapter 4, Section 4.5.

1.5 THE OTI-610 SYSTEM

Figure 1-5 presents a simplified block diagram of a PCI audio system based on the OTI-610. The audio codec may be an AC '97 type with the AC-Link interface, or it may be the STLC7549AC Audio Codec from SGS Thomson.

Reference Design Schematics and a Bill of Materials for an OTI-610 audio system implementation are available.

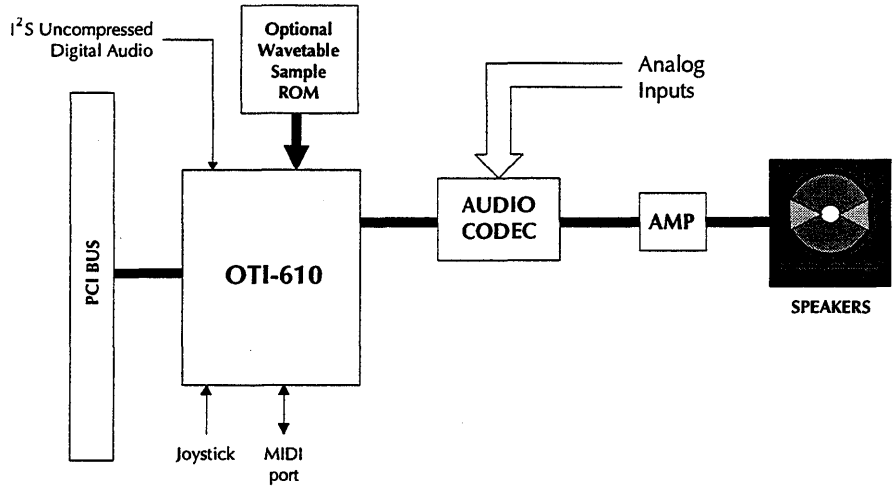

Figure 1-5: *OTI-610 Simplified System Block Diagram*

1.6 THE OTI-611 SYSTEM

Figure 1-6 below is a simplified block diagram of a PCI audio and communications system based on the OTI-611. The audio codec may be an AC '97 type with the AC-Link interface, or it may be the STLC7549AC Audio Codec from SGS Thomson. The modem codec may be the ST7546 from SGS Thomson. Alternatively, the audio and modem codec functions may be fulfilled by the Oak Technology OTI-612 AC '97 compliant dual codec, or any other AC '97 compliant dual codec. Other alternatives are the STLC7549 Dual Codec from SGS Thomson and the AD1843 Dual Codec from Analog Devices.

Refer to Chapter 3 for more information on interfacing to codecs.

The OTI-611 provides various interface signals to the DAA. For more details on the DAA interface, refer to Chapter 4. The DAA must be designed to meet the voltage isolation and connection approval regulations for the country or countries in which the resultant fax/data modem solution is to be sold. The DAA design may be a standard transformer and op-amp hybrid configuration, or may be all solid state design.

Reference Design Schematics and a Bill of Materials for various OTI-611 based audio and communications system implementations are available.

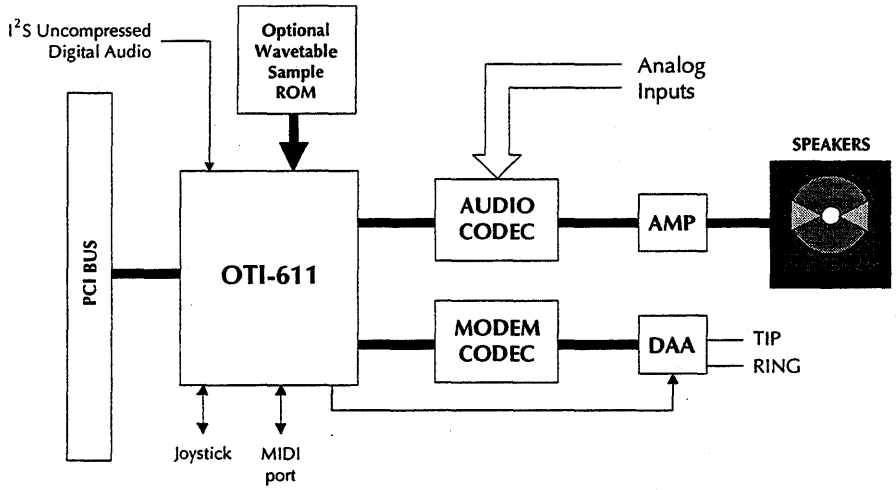

Figure 1-6: *OTI-611 Simplified System Block Diagram*

1.7 TECHNICAL SPECIFICATIONS

1.7.1 OTI-610 TECHNICAL SPECIFICATIONS

Physical Description

- 160-pin Plastic Quad Flat Pack (PQFP)
- 0.5µ triple-layer metal CMOS

Supported Multimedia Standards

- Microsoft DirectSound
- Microsoft DirectSound 3D
- Microsoft DirectInput
- Microsoft Windows Sound System
- SoundBlaster Pro software emulation via Windows 95 (for hardware-level compatibility a separate SB register compatible device is required).
- MPU-401 (UART mode)
- General MIDI synthesizer

DSP Specifications

- 36 Mips speed performance
- Tightly coupled interface between the DSP and PCI bus master
- Three sets of internal static random access memory (SRAM): 5Kx24 words, 4Kx16 words, and 2Kx16 words
- Single instruction/single data computation for all functions, including multiplier/accumulator (MAC)
- Single-cycle fetch of one opcode and two operands
- Single-cycle context switching
- Zero overhead looping and branching
- Three clock latency values for interrupts
- Extended dynamic range, including 40-bit accumulator
- External ROM memory space (up to 2MB)
- Parallel host interface port (HIP) for faster and more flexible communications with the host system
- Timing adjustable, external memory interface

- Special instructions for common audio operations
- Zero wait states for external memory access (when special coding rules are followed)

System Bus Interface

- 32-bit direct connection to PCI bus (33-MHz PCI 2.1 compliant)
- PCI burst and PCI bus mastering supported
- Scatter/gather functions supported
- Multiple interrupts supported

DSP Audio Processing

- DirectSound HRTF 3D positional audio
- Wavetable synthesis (optional)
- Sound buffer playback
- Sound buffer capture
- Digital audio mixing
- Sample rate conversions (8 KHz to 48 KHz)

Digital Mixing Capabilities

- Up to 8 mono or stereo channels of digital audio playback with sample rate conversion
- Two mono or stereo channels for audio capture and loopback

MIDI Interface

- MPU-401 UART mode
- 16-byte FIFOs for MIDI IN and OUT
- MIDI IN and OUT

Game Port Interface

- DirectInput support
- Digital mode
- Analog mode

Codec Interface Compatibility

- Any AC '97 audio codec
- STL7549AC audio-only Codec
- AD1843 Audio Codec

Microsoft DirectX Technology Accelerator

The OTI-610 supports the complete range of Microsoft's DirectSound and DirectSound 3D hardware acceleration functions.

The OTI-610 supports the complete range of Microsoft's DirectInput acceleration functions in hardware.

HSP Wavetable Synthesizer Specifications

- Available in Pentium class and Pentium MMX class software versions
- Up to 32-voice polyphony
- Full 16 MIDI channel multi-timbral support
- Complete General MIDI (GM) Sound Set
- GM Percussion Sound Set
- 4MB sample sets available
- Supports downloadable samples to system RAM
- User-defined maximum RAM cache, CPU utilization, and number of allowable voices
- Intelligent scaling and dynamic buffering to minimize CPU utilization

Optional DSP Wavetable Synthesizer Specifications

- Professional quality DSP-based wavetable synthesizer with 24-voice polyphony
- Full 16 MIDI channel multi-timbral support
- Complete 128-instrument GM Sound Sample Set, with GM Percussion Sound Set stored in external 2MB Sample ROM
- Programmable reverb and chorus effects control without additional SRAM

Minimum System Requirements

- 133-MHz Pentium CPU
- 16MB system memory
- 256KB cache

- PCI bus interface
- Windows 95 or Windows NT 4.0

Power Management

- Hardware and software power down and mute

Other Interfaces

- Programmable pin for peripheral control (software I^2C implementation)
- I^2S port for digital audio streams
- Wavetable sample ROM

AC '97 Codec Interface

- 5-pin digital serial interface — AC-Link
- Bi-directional, fixed data rate, serial PCM digital stream
- Supports 16-bit samples and sets the trailing 4 bits to zero (0) within the AC '97 20-bit data slots
- The AC-Link architecture divides each audio frame into 12 outgoing and 12 incoming datastreams, each with 20-bit sample resolution, allowing support of 16-bit, 18-bit, and 20-bit samples within each data slot of the datastream

Software and Manufacturing Support

Oak Technology offers comprehensive software support packages for Oak multimedia devices. The OTI-610 software package comes with drivers for popular operating systems such as Windows 95 and NT. In addition, Oak supplies complete manufacturing reference designs for the OTI-610, which facilitates early market entry.

Operating System Drivers

Windows 95	Windows NT 4.0
Windows Sound System	Windows Sound System
DirectSound and DirectSound 3D	MPU-401
DirectInput	Analog and Digital Joystick
Analog and Digital Joystick	
HSP Wavetable	
MPU-401	

1.7.2 OTI-611 TECHNICAL SPECIFICATIONS

Physical Description

- Integrated AC '97 compliant digital controller for audio and communications
- 160-pin Plastic Quad Flat Pack (PQFP)
- 0.5µ triple-layer metal CMOS

Supported Multimedia Standards

- Microsoft DirectSound
- Microsoft DirectSound 3D
- Microsoft DirectInput
- Microsoft Windows Sound System
- SoundBlaster Pro emulation in software via Windows (for hardware-level compatibility a separate SB register-compatible device is required)
- MPU-401 (UART mode)
- General MIDI synthesizer

DSP Specifications

- 36 Mips speed performance
- Tightly coupled interface between the DSP and PCI bus master
- Three sets of internal static random access memory (SRAM): 5Kx24 words, 4Kx16 words, and 2Kx16 words
- Single instruction/single data computation for all functions, including multiplier/accumulator (MAC)
- Single-cycle fetch of one opcode and two operands
- Single-cycle context switching
- Zero overhead looping and branching
- Three clock latency values for interrupts
- Extended dynamic range, including 40-bit accumulator
- External ROM memory space (up to 2MB)
- Parallel host interface port (HIP) for faster and more flexible communications with the host system
- Timing adjustable, external memory interface
- Special instructions for common audio operations
- Zero wait states for external memory access (when special coding rules are followed)

System Bus Interface

- 32-bit direct connection to PCI bus (33-MHz PCI 2.1 compliant)
- PCI burst and PCI bus mastering supported
- Scatter/gather functions supported
- Multiple interrupts supported

DSP Audio Processing

- Multiple digital audio channels
- DirectSound HRTF 3D positional audio
- Wavetable synthesis
- Sound buffer playback
- Sound buffer capture
- Digital audio mixing
- Sample rate conversions (8 KHz to 48 KHz)

Digital Mixing Capabilities

- Up to 8 mono or stereo channels of digital audio playback with sample rate conversion
- Two mono or stereo channels for audio capture and loopback

MIDI Interface

- MPU-401 UART mode
- 16-byte FIFOs for MIDI IN and OUT
- MIDI IN and OUT

Game Port Interface

- DirectInput support
- Digital mode
- Analog mode

Codec Interface Compatibility

- Any AC '97 audio/modem codec
- OTI-612 AC '97 audio/modem codec
- STLC7549 audio/modem codec

- AC '97 audio codec plus ST7546 modem codec
- AD1843 as audio/modem codec
- AD1843 as audio codec plus ST7546 modem codec

HSP/DAA Modem Interface

To support its host-based modem, the OTI-611 has the following Data Access Arrangement (DAA) functions and controls:

- RING_DET - Ring Detect
- LC_SENSE - Line Current Sense
- OFF_HOOK - Hook Relay Control
- CID_RELAY - Caller ID Relay Control
- HDSET_REL - Handset Relay Control
- CODEC_MODE - Codec Mode Select

Microsoft DirectX Technology Accelerator

The OTI-611 supports the complete range of Microsoft's DirectSound and DirectSound 3D hardware acceleration functions.

The OTI-611 supports the complete range of Microsoft's DirectInput acceleration functions in hardware.

HSP Wavetable Synthesizer Specifications

- Available in Pentium class and Pentium MMX class software versions
- Up to 32-voice polyphony
- Full 16 MIDI channel multi-timbral support
- Complete General MIDI (GM) Sound Set
- GM Percussion Sound Set
- 4MB sample sets available
- Supports downloadable samples to system RAM
- User-defined maximum RAM cache, CPU utilization, and number of allowable voices
- Intelligent scaling and dynamic buffering to minimize CPU utilization

Optional DSP Wavetable Synthesizer Specifications

- Professional quality DSP-based wavetable synthesizer with 24-voice polyphony
- Full 16 MIDI channel multi-timbral support
- Complete 128-instrument GM Sound Sample Set, with GM Percussion Sound Set stored in external 2MB sample ROM
- Programmable reverb and chorus effects control without additional SRAM

HSP Modem Specifications

- Industry-standard Hayes AT Command Set
- 28.8K/33.6K V.34+ modem (56K upgradeable)
- 14.4K V.29, V.17, and V.27ter fax
- V.42*bis* and MNP 5 compression
- V.42 LAPM and MNP 2-4 error detection/correction

Minimum System Requirements

- 133-MHz Pentium CPU (P166 required for simultaneous MIDI/modem operation)
- 16MB system memory (32MB recommended)
- 256KB cache
- PCI bus interface
- Windows 95 or Windows NT 4.0

Power Management

- Hardware and software power down and mute
- Modem wakeup on Ring Detect

Other Interfaces

- Programmable pin for peripheral control (software I^2C implementation)
- I^2S port for digital audio streams
- Wavetable sample ROM

AC '97 Codec Interface

- 5-pin digital serial interface — AC-Link.
- Bi-directional, fixed data rate, serial PCM digital stream

- Supports 16-bit samples and sets the trailing 4 bits to zero (0) within the AC '97 20-bit data slots
- The AC-Link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution, allowing support of 16-bit, 18-bit, and 20-bit samples within each data slot of the data stream

Software and Manufacturing Support

Oak Technology offers comprehensive software support packages for Oak multimedia devices. The OTI-611 software package comes with drivers for popular operating systems such as Windows 95 and NT. In addition, Oak supplies complete manufacturing reference designs for the OTI-611, which facilitates early market entry.

Operating System Drivers

Windows 95	Windows NT 4.0
Windows Sound System	Windows Sound System
DirectSound and DirectSound 3D	MPU-401
DirectInput	Analog and Digital Joystick
Analog and Digital Joystick	HSP Modem
HSP Modem	
HSP Wavetable	
MPU-401	

1.8 WAVETABLE SYNTHESIZER TECHNICAL SPECIFICATIONS

The OTI-610 or OTI-611 systems optionally support two types of wavetable synthesizers:

- Host signal processing (HSP) based
- Digital signal processor (DSP) based

The HSP type is Pentium class or Pentium MMX class based software only and produces a digital audio data stream that is sent to the OTI-610/OTI-611, similar to data contained in a .WAV file. The OTI-610/OTI-611 mixes this digital audio data along with any other incoming digital audio data streams and sends the resultant digital mix to the audio codec for playback.

The DSP type is implemented in firmware running on the internal DSP engine within the OTI-610/OTI-611. The DSP wavetable synthesizer engine produces a digital audio data stream that is mixed internally in the DSP along with other incoming digital audio data streams. The resultant digital audio mix is sent to the audio codec for playback.

Appendix B contains the following additional information about each type of wavetable synthesizer supported for OTI-610/OTI-611 based systems.

- General MIDI Sound Sample Set chart
- GM Percussion Sound Set chart
- MIDI implementation chart
- General information on MIDI

1.8.1 HSP WAVETABLE SYNTHESIZER TECHNICAL SPECIFICATIONS

When used with the OTI-610 or OTI-611 as the audio playback system with MPU-401 MIDI port support, the HSP wavetable synthesizer meets the following technical specifications:

- Professional quality software-based synthesizer with 32-voice polyphony
- Available in Pentium class and Pentium MMX class software versions
- Full 16 MIDI channel multi-timbral support
- Complete 128-instrument GM Sound Sample Set, with extended GM Percussion Sound Set
- Programmable reverb and chorus effects control using system RAM
- Supports downloadable samples to system RAM, extending instrument options beyond General MIDI instrument set
- User-selectable maximum RAM cache, CPU utilization, and number of allowable voices
- Intelligent scaling and dynamic buffering to minimize CPU utilization
- MIDI IN, MIDI OUT hardware MPU-401 interface to external MIDI sequencers, MIDI sound modules, and MIDI keyboards for recording and playback.
- Real-time instrument selection when used with CyberSound Keyboard application
- Works with standard Windows 95 software sequencers (Media Player, Sound Recorder [play mode], Cakewalk Pro, Voyetra Orchestrator, Netscape Navigator MIDI playback plug-ins, and others) for MIDI file playback and real-time user control of the synthesizer.

1.8.2 OPTIONAL DSP WAVETABLE SYNTHESIZER TECHNICAL SPECIFICATIONS

The OTI-610 or OTI-611 will support an optional DSP-based wavetable synthesizer, which will meet the following technical specifications:

- Professional-quality DSP-based wavetable synthesizer with 24-voice polyphony
- Full 16 MIDI channel multi-timbral support
- Complete 128-instrument GM Sound Sample Set, with GM Percussion Sound Set stored in external 2MB sample ROM
- Programmable reverb and chorus effects control without additional SRAM

- MIDI IN, MIDI OUT hardware MPU-401 interface to external MIDI sequencers, MIDI sound modules, and MIDI keyboards for recording and playback
- Real-time instrument selection when used with CyberSound Keyboard application
- Works with standard Windows 95 software sequencers (Media Player, Sound Recorder [play mode], Cakewalk Pro, Voyetra Orchestrator, Netscape Navigator MIDI playback plug-ins, and others) for MIDI file playback and real-time user control of the synthesizer

1.8.3 HSP FAX/DATA MODEM TECHNICAL SPECIFICATIONS

The HSP V.34/V.34+ fax/data modem software supplied with the OTI-611 will, when combined with appropriate modem codec and approved DAA, result in a fully functional fax/data modem capable of meeting the following specifications listed below.

Appendix A contains the supported AT Command Set, along with other details.

COMMAND SET
DATA STANDARDS Industry Standard Hayes AT Command Set

ITU-T V.21	0-300 bps
ITU-T V.22	1,200 bps
ITU-T V.22*bis*	2,400 bps
ITU-T V.23	1,200/75 bps
ITU-T V.32	9,600 bps
ITU-T V.32*bis*	14,400 bps
ITU-T V.34	28,800 bps
V.34+	33,600 bps
Bell 103	0-300 bps
Bell 212A	1,200 bps

FACSIMILE STANDARDS

ITU-T V.21	300 bps Channel 1
ITU-T V.17	14,400 bps
ITU-T V.27*ter*	4,800 bps
ITU-T V.29	9,600 bps

ASYNCHRONOUS DATA

Start Bits	Data Bits	Parity Bits	Stop Bits
1	7	odd or even	1 or 2
1	7	mark or space	1 or 2
1	8	none	2
1	8	none	1 or 2

ERROR CORRECTION ITU-T V.42 LAPM and MNP 2-4
DATA COMPRESSION ITU-T V.42*bis* and MNP 5
COMMUNICATIONS

Receive Sensitivity:	-43 dBm
Transmit Level:	-10 dBm (± 1 dBm) Adj. if allowed by PTT

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CHAPTER 2 PCI BUS INTERFACE

2.1 PCI BUS INTERFACE DESCRIPTION

The OTI-610 and OTI-611 support direct connections to the PCI bus. The PCI interface is compliant with the PCI Local Bus Specification Revision 2.1.

Each logical device within the OTI-610/OTI-611 circuits (audio and game port devices for the OTI-610 and audio, game port, and modem devices for the OTI-611) has its own configuration read and write registers to meet PCI plug and play requirements, as well as I/O base address registers to meet the need for programmable control registers to control the functions of each device.

To increase the audio data transfer rate, the OTI-610 and OTI-611 also perform as bus masters to take memory read/write burst cycles and directly capture or fill system memory as required.

Refer to Chapter 6 for pin names and descriptions for the PCI bus interface.

Refer to Chapter 7 for register descriptions of the OTI-610/OTI-611.

PCI Bus Interface

- The 32-bit PCI bus is supported up to 33 MHz.
- Bus master memory read/write cycles can be programmed to be either 0 or 1 wait state on the OTI-610/OTI-611 side. The default value is 1 wait state. The typical bus master transfer is done as 4 double words in a burst cycle.
- The configuration cycle is run at 1 wait state.
- I/O cycles run at 2-5 wait states.

2.2 PCI BUS FUNCTION INFORMATION

The following tables show the PCI bus interface command cycles that the OTI-610 and OTI-611 support.

Command	Supported Mode	Description
I/O Read	Target	No burst cycle, no back-back I/O, medium DEVSEL#, any enable bytes combination.
I/O Write	Target	No burst cycle, no back-back I/O, medium DEVSEL#, any enable bytes combination.
Interrupt Acknowledge	Not supported	
Special Cycle	Not supported	
Configuration Read	Target	Any enable bytes combination, medium DEVSEL#. Burst cycle not supported.
Configuration Write	Target	Any enable bytes combination, medium DEVSEL#. Burst cycle not supported.
Memory Read	Master	4 DWORD, burst cycle transfer depends on buffer request.
Memory Write	Master	4 DWORD, burst cycle transfer depends on buffer request.
Memory Read Multiple	Not supported	
Dual Address Cycle	Not supported	
Memory Read Line	Not supported	
Memory Write and Invalidate	Not supported	

Unsupported Special Bus Interface Signals:

PERR#	Not supported
SERR#	Not supported
LOCK#	Not supported
SBO#	Not supported
SDONE#	Not supported

Termination and Special Functions in Master Mode:

Fast Back-to-Back Transaction	Not supported
Target Abort	Master mode can handle this
Disconnect	Master mode can handle this
Retry	Master mode can handle this
Master Abort	Wait up to six PCI clocks to detect DEVSEL# in master cycle
Latency Timer	Not supported
Cache Line Size	Not supported
Address/Data Stepping	Does not happen

Termination and Special Functions in Slave/Target Mode:

Delay Transaction	Not supported
Fast Back-to-Back Transaction	Not supported
Target Abort	Supported when illegal address detected
Disconnect	Supported when burst cycle occurs
Retry	Does not happen
Master Abort	Does not happen
Address/Data Stepping	Does not happen

Note: In Slave mode, the OTI-610 and OTI-611 do not support burst cycle in order to avoid any errors occurring in transfer cycle. Slave mode should implement disconnect target termination when burst cycle occurs. That is, if both FRAME# and IRDY# are detected and asserted at the same rising CLK, the OTI-610 and OTI-611 will assert TRDY#, STOP#, and DEVSEL# until the current data phase transfer completes.

2.2.1 CONFIGURATION READ/WRITE CYCLE

Configuration read/write commands support (decoding cmd = 1010 or 1011).

If IDSEL# is asserted, the configuration commands are latched and AD[1:0] are 00 (indicating Type 0 configuration header), and then the configuration cycle is started.

When FRAME# is asserted (sampled on the rising CLK), the AD bus must be latched and decode the offset configuration space (if the configuration cycle is on at the same time). Data read/write occurs after the second CLK rising edge (sends TRDY# out). The second CLK means IRDY# has been sampled.

When FRAME# is sampled and the second rising CLK also samples both FRAME# and IRDY#, the burst cycle occurs. Because the OTI-610/OTI-611 does not support a burst cycle, the PCI interface should assert STOP# and TRDY# at the same time.

2.2.2 I/O READ/WRITE CYCLE

The OTI-610 and OTI-611 have an internal 32-bit wide data bus. By using I/O mapped registers, the device drivers can directly control internal functions and get information about the OTI-610 and OTI-611 peripheral devices.

At the CLK rising edge, if FRAME# is asserted , the OTI-610 and OTI-611 will latch the AD bus and CMD bus data. After decoding the content, if the address bus value equals the I/O base register address, and the command is *I/O read/write* (0010 or 0011), then the OTI-610/OTI-611 Slave mode is entered and DEVSEL# will be sent out until the transaction is completed.

At the next rising CLK , the OTI-610 and OTI-611 will detect the IRDY# assertion. If it is true, the OTI-610/ OTI-611 will receive the data or send out the data that is associated with the registers' decoded address and byte enable at the following rising edge CLK. TRDY# will be sent out when the IRDY# is sampled at rising edge CLK.

2.2.3 GAME PORT REGISTERS

PCI Game Port Configuration registers are supported along with Standard Game addresses. Consult Chapter 7, Section 7.6 for complete details. The default state for the OTI-610/OTI-611 is disabled.

2.2.4 BUS MASTER OPERATION AND MEMORY READ/WRITE BURST CYCLE

Bus Master Mode

When operating in the WSS or DirectSound modes, the device drivers enable the bus master cycle and the burst line buffer is empty. The OTI-610/OTI-611 will request the bus from the system arbiter. The bus request will continue to be asserted when buffer is empty until the disable command is received from OTI-610/OTI-611 device drivers.

Buffer Architecture for the Bus Master

Two 4-DWORD-sized line buffers are dedicated to each capture and playback function in the bus master mode. This buffer is used for the memory burst command. The physical memory address and counter will increment at each DWORD transfer. When the counter matches the Data Length register, an interrupt will be generated. The address must auto-increment one DWORD until 2x the data length offset is met, then the Memory address will reload from the Memory address registers.

Command Select and Memory Burst Cycle

The OTI-610 and OTI-611 support bus master operation to issue a memory burst cycle, and the command could be selected by device drivers. The supported commands include Memory Read, Memory Read Line, Memory Write, Memory Write, and Invalidate to complete a burst cycle. The memory burst line buffer size is 4 DWORD.

When the OTI-610 and OTI-611 bus master is active and the request bus has been granted (GNT# asserted), the OTI-610 and OTI-611 will continue to detect both FRAME# and IRDY# de-asserted (IDLE state). If IDLE state has been detected, the bus master starts a bus cycle and sends FRAME#, burst start address, and command out first. On the following CLK, IRDY# is sent out and the circuitry detects DEVSEL#, if it is asserted. If DEVSEL# is asserted, the following rising CLK will transfer data as each TRDY# is sampled. Before the next data transfer (the fourth DWORD), FRAME# is de-asserted and IRDY# continues to be asserted until completion of the last data transfer. When the last data has been transferred, the line buffer should be full. The OTI-610 and OTI-611 will request the bus when the buffer is empty and bus master is still enabled.

CHAPTER 3 CODEC INTERFACES

3.1 CODEC SELECTION

The OTI-610 and OTI-611 require information specifying which type of codec or combinations of codecs will be used. This information is obtained during the Power Up sequence by reading the state of three signals, according to the table below. Internally the pins are pulled up to Vdd. **The logic state (1) may be set using pull-down resistors on the appropriate pins.** Refer to the OTI-610/OTI-611 Reference Schematics for component values.

After the Codec Selection data is read during Power Up, it is also stored in the OTI-610/OTI-611 Internal Status register 40h, where it may be read by the OTI-610/OTI-611 software driver and used to set up the codecs for proper operation.

Codec Supported	OTI-610/OTI-611 Signal Name		
	WDMA[7] (MCODEC bit 2)	WDMA[6] (MCODEC bit 1)	WDMA[5] (MCODEC bit 0)
AD1843 as Audio/Modem Codec[1]	0	0	0
Reserved	0	0	1
AD1843 as Audio Codec plus ST7546 Modem Modec[1]	0	1	0
Reserved Audio Codec plus ST7546 Modem Codec[1]	0	1	1
STLC7549 Audio/Modem Codec[1]	1	0	0
OTI-612 AC '97 Audio/Modem Codec[1] or Any AC '97 Audio/Modem Codec[1]	1	0	1
AC '97 Audio Codec plus ST7546 Modem Codec[1]	1	1	1
Reserved	1	1	0

Note: [1]Modem Codec Selection is used by the OTI-611 only. Modem codec functions cannot be accessed by the OTI-610, and the bit selections used with the OTI-610 will only affect audio codec selection.

3.2 CODEC INTERFACES

The OTI-610 is designed to support audio functions, while the OTI-611 is designed to support both audio and communications functions. Both devices will support a variety of codecs, as listed in the table below.

In the sections that follow, details will be provided on interfacing to each type of codec.

Codecs Supported by the OTI-610 and OTI-611:

Codec	Description	Support	Notes
OTI-612	AC '97 Compliant (AC-Link) Dual Audio and Communications Codec	OTI-611	1,2,3
AC '97 Codec (AC-Link)	Audio Codec (basic specifications) Dual Audio and Communications Codec (basic specification + modem support)	OTI-610 OTI-611	1 1,2,4
STLC7549	Dual Audio and Communications Codec	OTI-611	5
STLC7549AC	Audio Codec	OTI-610 (audio only) OTI-611 (audio port)	5
ST7546	Modem Codec (master mode, software mode, or hardware mode for data transmit	OTI-611 (modem port)	5
AD1843	Dual Audio and Communications Codec (master mode, 16/32 slots per frame)	OTI-610 (audio only) OTI-611	6

Notes (notes from AC '97 Specification in *italics*):

1. *AC '97 controller/AC '97 pair interoperability can only be guaranteed for non-optional AC '97 audio features.*
2. *Modem interoperability is not expected between AC '97 controller/AC '97 pairs that aren't sourced as a matched set by the same vendor. Given this, each vendor's AC '97 controller implicitly knows what the Modem DAC/ADC resolution is in the AC '97 version w/ modem support by inspecting the vendor ID registers.*
3. Oak Technology part number
4. Future products from other manufacturers of AC '97 compliant codecs provided modem 16-bit outgoing and incoming data is in time slot 5. See note on modem interoperability.
5. SGS Thomson part number
6. Analog Devices part number

Throughout the discussion of interfacing with the various codecs in this chapter, codec signal names will be given along with the equivalent OTI-610 and OTI-611 signal names. Codec signal names appearing in descriptive text will be printed in italics and will be enclosed within parentheses.

Tables containing signal names will show both the OTI-610/OTI-611 and codec signal names in the same way. Example:

OTI-610/OTI-611 Signal Name	**AC-Link Signal Name**
ARESET#	*(RESET#)*

Timing diagrams will be presented with the OTI-610 and/or OTI-611 signal name in the illustration.

3.3 OTI-610/OTI-611 TO AC '97 CODEC INTERFACE

The OTI-610 or OTI-611 communicates with the OTI-612 AC '97 compatible dual audio and communications codec (or any other AC '97 compatible audio or dual audio and communications codec) via a digital serial link called "AC-Link."

AC-Link is a 5-pin, bi-directional, fixed data rate, serial PCM digital stream. It handles multiple input and output audio streams, as well as control register accesses to the AC '97 Codec device employing a time division multiplexed (TDM) scheme. The AC-Link architecture divides each audio frame into 12 outgoing and 12 incoming datastreams, each with 20-bit sample resolution. Support is also available for 16-bit and 18-bit data samples within the 20-bit slot. The OTI-610 and OTI-611 support 16-bit sample data within an AC '97 data slot. See Chapter 8 for further information on AC-Link, including DC and AC timing characteristics.

All digital audio streams, optional modem line codec streams, and command/status information are communicated over the AC-Link point-to-point serial interconnect interface. A breakout of the signals connecting the two is shown in the table below. The signals listed in the table connect the OTI-610/OTI-611 to an AC '97 compatible codec.

OTI-610/OTI-611 Signal Name	Type	OTI-612 or AC '97 Codec Signal Name-AC-Link Signal Name	Type	Description
ARESET#	O	RESET#	I	Master H/W Reset to AC '97 Codec from OTI-610 or OTI-611
AFS	O	SYNC	I	48-KHz fixed rate sample sync from OTI-610 or OTI-611
ASCLK	I	BIT_CLK	O	12.288-MHz serial data clock (Fx/2 from AC '97 Codec) to OTI-610 or OTI-611. Fx=24.576 MHz
ASDO	O	SDATA_OUT	I	Serial, time division multiplexed output stream to AC '97 Codec from OTI-610 or OTI-611
ASDI	I	SDATA_IN	O	Serial, time division multiplexed input stream from AC '97 Codec to OTI-610 or OTI-611

Throughout the discussion of interfacing with AC '97 type codecs in this chapter, AC-Link signal names will be given along with the equivalent OTI-610 and OTI-611 signal names. AC-Link signal names appearing in descriptive text will be printed in italics and will be enclosed within parentheses.

Tables containing signal names will show both the OTI-610/OTI-611 and AC-Link signal names in the same way.

Example:

OTI-610/OTI-611 Signal Name	**AC-Link Signal Name**
ARESET#	*(RESET#)*

Timing diagrams will be presented with the AC-Link signal name in the illustration.

3.3.1 AC '97 CODEC TYPES

The AC '97 Codec is specified at minimal functionality as an **audio-only** codec. Optional support for modem functions may also be provided, in which case the AC '97 Codec is an **audio/communications** codec, or a dual codec.

The OTI-610 is an audio accelerator, and when used in an AC '97 system will support audio-only versions of the AC '97 Codec. The OTI-611 is an audio/communications accelerator, and when used in an AC '97 system will support audio/communications versions of the AC '97 Codec, such as the OTI-612.

The AC '97 Codec is specified in two package types — 48 pins and 64 pins. The audio-only or the audio/communications version of the AC '97 Codec could be supplied in either a 48-pin or a 64-pin package. Connections to the various types of AC '97 Codecs and the OTI-610 and OTI-611 are shown in the figures below.

OTI-610 Connections to AC '97 Audio Codecs

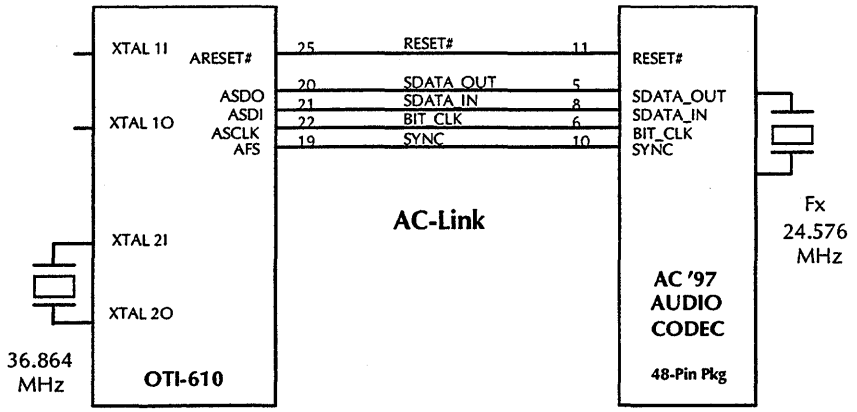

Figure 3-1: *OTI-610 AC-Link Connection to AC '97 Audio Codec, 48-pin Package*

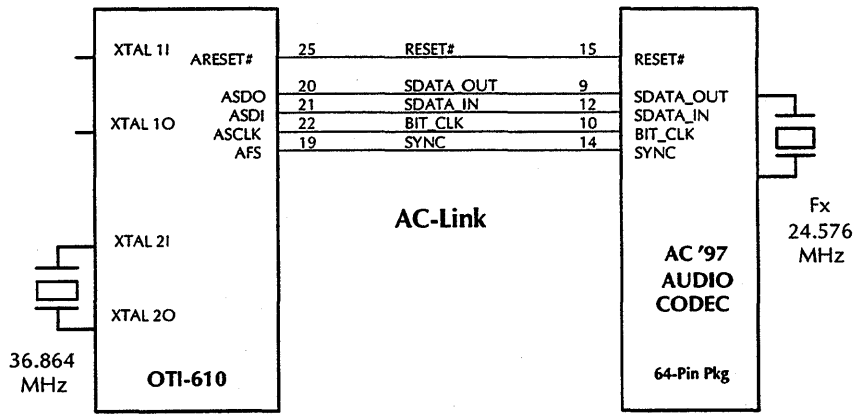

Figure 3-2: *OTI-610 AC-Link Connection to AC '97 Audio Codec, 64-pin Package*

OTI-611 Connections to AC '97 Audio/Communications Codecs

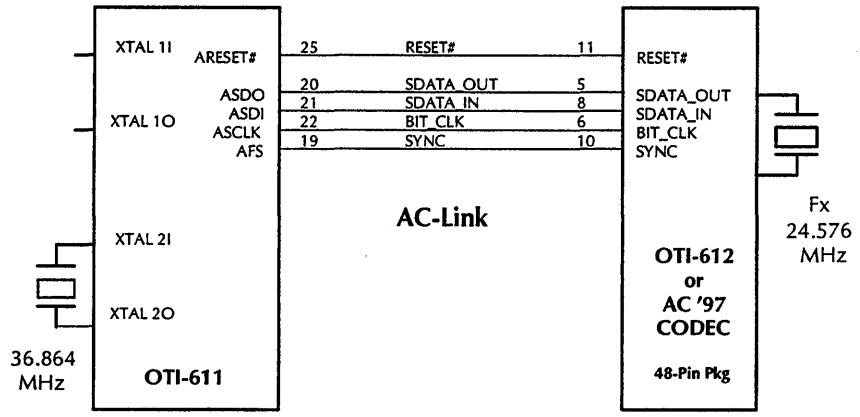

Figure 3-3: *OTI-611 AC-Link Connection to AC '97 Audio/Communications Codec, 48-pin Package*

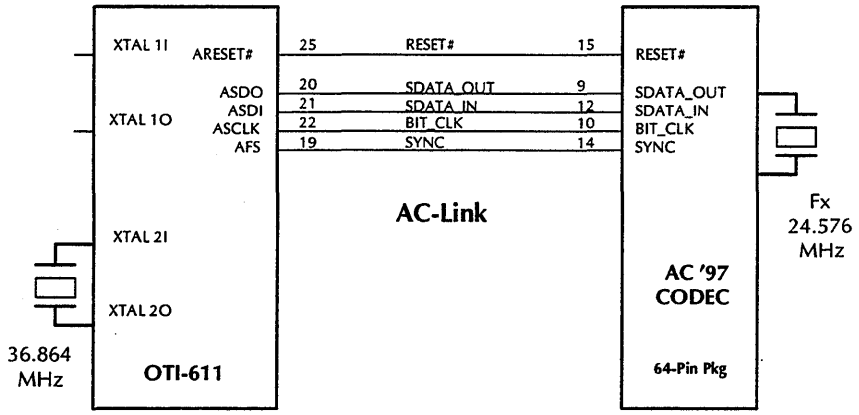

Figure 3-4: *OTI-611 AC-Link Connection to AC '97 Audio/Communications Codec, 64-pin Package*

3.3.2 AC '97 CODEC CLOCKING

Synchronization of all AC-Link data transactions is signaled by the OTI-610/OTI-611. The OTI-612 or other AC '97 compatible codecs drive the serial bit clock (BIT_CLK) onto AC-Link, which the OTI-610/OTI-611 then qualifies with a synchronization signal AFS *(SYNC)* to construct audio frames.

The OTI-612 or other AC '97 compatible codecs derive their clocks from an external 24.576-MHz (Fx) crystal and drive a buffered and divided-by-2 clock (Fx/2) to the OTI-610/OTI-611 over AC-Link under the AC-Link signal name "BIT_CLK." The use of a crystal is recommended, but an external oscillator may also be input to AC '97. Clock jitter at the DACs and ADCs is a fundamental impediment to high-quality output, and the internally generated clock provides a clean clock that is independent of the physical proximity of the OTI-610 or OTI-611.

The beginning of all audio sample packets, or "audio frames," transferred over AC-Link is synchronized to the rising edge of the AFS *(SYNC)* signal. AFS *(SYNC)* is driven by the OTI-610 or OTI-611. The OTI-610 or OTI-611 takes ASCLK *(BIT_CLK)* as an input and generates AFS *(SYNC)* by dividing ASCLK *(BIT_CLK)* by 256 and applying some conditioning to tailor its duty cycle. This yields a 48-KHz AFS *(SYNC)* signal whose period defines an audio frame. Data is transitioned on AC-Link on every rising edge of ASCLK *(BIT_CLK)* and subsequently sampled on the receiving side of AC-Link on each immediately following falling edge of ASCLK *(BIT_CLK)*.

3.3.3 RESETTING THE AC '97 CODEC

There are three types of AC '97 Codec resets:

1. a "cold" reset where all AC '97 Codec logic (registers included) is initialized to its default state
2. a "warm" reset where the contents of the AC '97 Codec register set are left unaltered
3. a "register" reset which only initializes the AC '97 Codec registers to their default states

After signaling a reset to AC '97, the OTI-610/OTI-611 will attempt to play or capture audio data until it has sampled a "Codec Ready" indication from the AC '97 Codec. (Refer to Chapter 8 for detailed explanations and timing diagrams.)

3.3.4 AC-LINK AUDIO OUTPUT FRAME *(SDATA_OUT)*

The audio output frame datastreams correspond to the multiplexed bundles of all digital output data targeting the OTI-612 or any AC '97 compliant codec DAC inputs and control registers. Each audio output frame supports up to 12 20-bit outgoing data time slots with either 16-bit, 18-bit, or 20-bit data in each time slot.

In the AC '97 mode, the OTI-610/OTI-611 supports only 16-bit data for slot 0 and 16-bit MSB justified data, with trailing zeroes for 20-bit audio and modem data slots.

Slot 0 is a special reserved time slot containing 16 bits used for AC-Link protocol infrastructure.

Within slot 0 the first bit is a global bit (ASDO *(SDATA_OUT)* slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by the AC '97 Codec indicate which of the corresponding 12 time slots contain valid data. In this way, datastreams of differing sample rates can be transmitted across AC-Link at its fixed 48-KHz audio frame rate. Control/Status as well as optional extensions of the baseline AC '97 specification, such as the modem line codec, may take advantage of this feature. AC '97 specified audio functionality **must always** sample rate convert to and from a fixed 48 kilo samples/second on the AC '97 controller. This requirement is necessary to ensure that interoperability between AC '97 controller/AC '97 Codec pairs, among other things, can be guaranteed by definition for baseline specified AC '97 features.

The following diagram illustrates the time slot based AC-Link protocol.

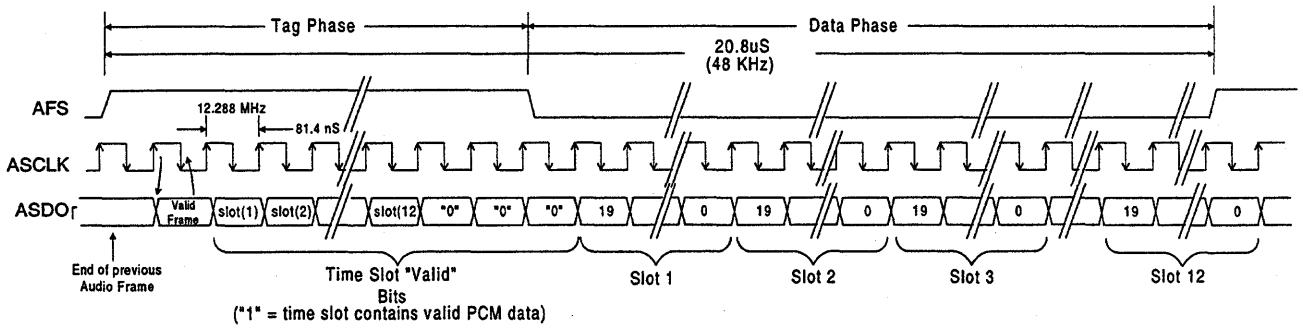

Figure 3-5: *AC-Link Audio Output Frame*

A new audio output frame begins with a low to high transition of AFS *(SYNC)*. AFS *(SYNC)* is synchronous to the rising edge of ASCLK *(BIT_CLK)*. On the immediately following falling edge of ASCLK *(BIT_CLK)*, the AC '97 Codec samples the assertion of AFS *(SYNC)*. This falling edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising of ASCLK *(BIT_CLK)*, the OTI-610 or OTI-611 transitions ASDO *(SDATA_OUT)* into the first bit position of slot 0 (Valid Frame bit). Each new bit position is

presented to AC-Link on a rising edge of ASCLK *(BIT_CLK)* and subsequently sampled by the AC '97 Codec on the following falling edge of ASCLK *(BIT_CLK)*. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing datastreams are time aligned.

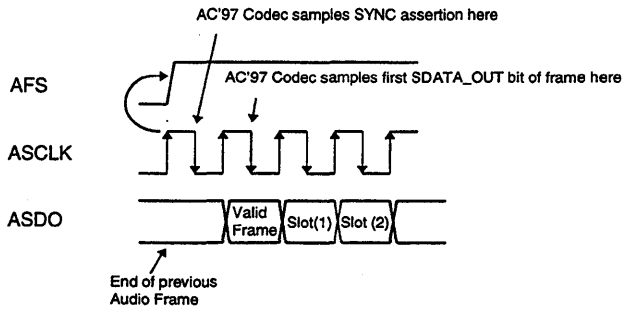

Figure 3-6: *Start of an Audio Output Frame*

The ASDO *(SDATA_OUT)* composite stream is MSB justified (MSB first) with all non-valid slots' bit positions set with 0s by the OTI-610 or OTI-611. In the event that there are less than 20 valid bits within an assigned and valid time slot, the OTI-610/OTI-611 always sets all trailing non-valid bit positions of the 20-bit slot with 0s.

For example, consider an 8-bit sample stream that is being played out to one of the AC '97 Codec's DACs. The first 8-bit positions are presented to the DAC (MSB justified), followed by the next 12 bit positions, which are set with 0s by the OTI-610 or OTI-611. This ensures that regardless of the resolution of the implemented DAC (16-, 18-, or 20-bit), no DC biasing will be introduced by the least significant bits.

When monophonic audio sample streams are output from the OTI-610 or OTI-611, it is necessary that **both** left and right sample stream time slots be filled with the same data.

3.3.5 AC-LINK AUDIO INPUT FRAME *(SDATA_IN)*

The audio input frame datastreams correspond to the multiplexed bundles of all digital input data targeting the OTI-610/OTI-611. As is the case for audio output frame, each AC-Link audio input frame consists of 12 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits used for AC-Link protocol infrastructure.

Within slot 0 the first bit is a global bit (ASDI *(SDATA_IN)* slot 0, bit 15) that flags whether the AC '97 Codec is in the "Codec Ready" state or not. If the "Codec Ready" bit is a 0, this indicates that the AC '97 Codec is not ready for normal operation. This condition is normal, for example, following the de-assertion of Power On Reset, while the AC '97 Codec's voltage references settle. When the AC-Link "Codec Ready" indicator bit is a 1, it indicates that the AC-link and AC '97 control and status registers are in a fully operational state. The OTI-610/OTI-611 must further probe the Power Down Control/Status register of the AC '97 Codec to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting the AC '97 Codec into operation, the OTI-610/OTI-611 should poll the first bit in the audio input frame (ASDI *(SDATA_IN)* slot 0, bit 15) for an indication that the AC '97 Codec has gone "Codec Ready." Once the AC '97 Codec is sampled Codec Ready2, then the next 12 bit positions sampled by the OTI-610/OTI-611 indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data.

There are several subsections within AC '97 Codec that can independently go busy/ready. It is the responsibility of the OTI-610/OTI-611 software drivers to probe more deeply into the AC '97 Codec register file to determine which AC '97 Codec subsections are actually ready.

The following diagram illustrates the time slot based AC-Link protocol.

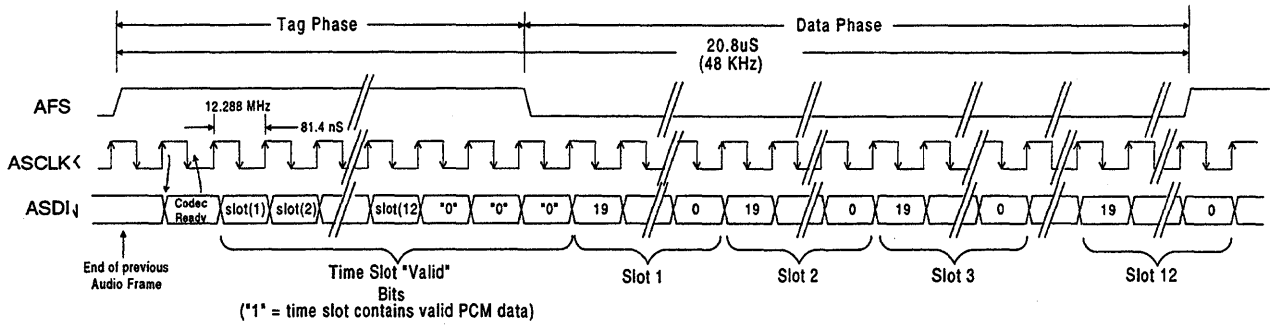

Figure 3-7: *AC-Link Audio Input Frame*

A new audio input frame begins with a low to high transition of AFS *(SYNC)*. AFS *(SYNC)* is synchronous to the rising edge of ASCLK *(BIT_CLK)*. On the immediately following falling edge of ASCLK *(BIT_CLK)*, the AC '97 Codec samples the assertion of AFS *(SYNC)*. This falling edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising of ASCLK *(BIT_CLK)*, the AC '97 Codec transitions ASDI *(SDATA_IN)* into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-Link on a rising edge of ASCLK *(BIT_CLK)*, and subsequently sampled by the OTI-610/OTI-611 on the following falling edge of ASCLK *(BIT_CLK)*. This sequence ensures that data transitions and subsequent sample points for both incoming and outgoing datastreams are time-aligned.

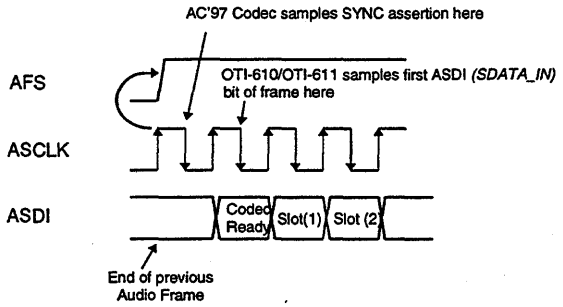

Figure 3-8: *Start of an Audio Input Frame*

The ASDI *(SDATA_IN)* composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) set with 0s by the AC '97 Codec. ASDI *(SDATA_IN)* data is sampled on the falling edges of ASCLK *(BIT_CLK)*.

For more complete data and information on AC '97, consult the Audio Codec '97 component specification.

3.4 DUAL CODEC (AUDIO AND MODEM) INTERFACE (OTI-611 TO STLC7549)

The STLC7549 is a 16-bit ΣΔ-type dual audio and communications codec manufactured by SGS Thomson. For audio functions it supports a variety of analog inputs and various hardware controls, as well as software register controls.

The AC timing diagram and parameter table for the OTI-611 interface to the STLC7549 are given in Section 9.5 (Chapter 9).

The OTI-611 provides a direct interface to the STLC7549 for both audio and fax/data modem functions.

For audio, the data transfer and clocking interface consists of five signals: AMCLK *(MCLKA)*, AFS *(FSYNC1)*, ASCLK *(SCLK1)*, ASDI *(SIN1)*, and ASDO *(SOUT1)*. AMCLK is an audio master clock derived from the OTI-611 internal clock generation circuitry. It is sent to the STLC7549AC master clock — *MCLKA* — input. No external crystal on the STLC7549 is required. From the AMCLK *(MCLKA)* signal, all internal sampling frequencies for the audio functions of the STLC7549 are generated, as well as the audio serial bit clock — ASCLK *(SCLK1)* — and the audio frame sync signal — AFS *(FSYNC1)*.

An audio data frame consists of four time slots in the ASDI *(SIN1)* direction and four time slots in the ASDO *(SOUT1)* direction. For the outgoing audio frame to the STLC7549, two time slots are assigned for audio Left and Right data, and two time slots are assigned for STLC7549 register control data (if any) that may be written to control registers. For the incoming audio frame from the STLC7549, two time slots are assigned for digitized analog audio Left and Right data, and two time slots are assigned for STLC7549 status information and register content data.

The fax/data modem register control data and status information is also carried on the audio frame, as described below.

By placing data into the appropriate outgoing audio frame time slot, the OTI-611 software driver is able to configure the STLC7549 to the requirements of the audio as well as the fax/data modem subsystem. Conversely, by reading the data in the appropriate incoming audio frame time slot, the OTI-611 software driver is able to determine the audio and fax/data modem configuration status of the STLC7549 and modify either accordingly during the next frame (if necessary).

For fax/data modem functions, the data transfer and clocking interface consists of five signals: MMCLK *(MCLKM)*, MFS *(FSYNC2)*, MSCLK *(SCLK2)*, MSDI *(SIN2)*, and MSDO *(SOUT2)*.

MMCLK is an modem master clock derived from the OTI-611 internal clock generation circuitry. It is sent to the STLC7549 modem master clock — *MCLKM* — input. From the MMCLK *(MCLKM)* signal, all internal sampling frequencies for the modem functions of the STLC7549 are generated, as well as the modem serial bit clock — MSCLK *(SCLK2)* — and the modem frame sync signal — MFS *(FSYNC2)*.

A fax/modem data frame consists of four time slots in the MSDI *(SIN2)* direction and four time slots in the ASDO *(SOUT2)* direction. For the outgoing fax/data modem frame to the STLC7549, two time slots are assigned for modem data and telephony data, and two time slots are reserved. For the incoming fax/data modem frame from the STLC7549, two time slots are assigned for modem data and telephony data, and two time slots are reserved.

For complete specification and implementation details for the STLC7549, please consult the STLC7549 data sheet or contact SGS Thomson.

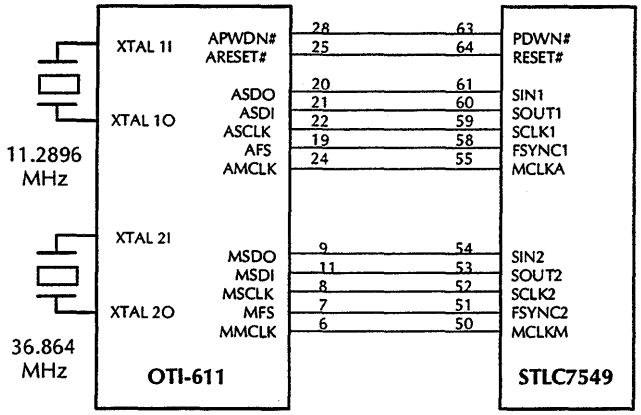

Figure 3-9: *Dual Codec (Audio and Modem) Interface (OTI-611 to STLC7549)*

3.5 AUDIO CODEC INTERFACE (OTI-610 TO STLC7549AC)

The STLC7549AC is a 16-bit SD-type audio codec manufactured by SGS Thomson. It supports a variety of analog inputs and various hardware controls, as well as software register controls.

The AC timing diagram and parameter table for the OTI-610 interface to the STLC7549AC are given in Chapter 9, Section 9.6.

The OTI-610 provides a direct interface to the STLC7549AC. The data transfer and clocking interface consists of five signals: AMCLK *(MCLKA)*, AFS *(FSYNC1)*, ASCLK *(SCLK1)*, ASDI *(SIN1)*, and ASDO *(SOUT1)*. AMCLK is an audio master clock derived from the OTI-610 internal clock generation circuitry. It is sent to the STLC7549AC master clock — *MCLKA* — input. No external crystal on the STLC7549AC is required. From the AMCLK *(MCLKA)* signal, all internal sampling frequencies for the STLC7549AC are generated, as well as the serial bit clock — ASCLK *(SCLK1)* — and the frame sync signal — AFS *(FSYNC1)*.

An audio data frame consists of four time slots in the ASDI *(SIN1)* direction and four time slots in the ASDO *(SOUT1)* direction. For the outgoing audio frame to the STLC7549AC, two time slots are assigned for audio Left and Right data, and two time slots are assigned for register control data (if any) that may be written to control registers. For the incoming audio frame from the STLC7549AC, two time slots are assigned for digitized analog audio Left and Right data, and two time slots are assigned for status information and register content data.

By placing data into the appropriate outgoing audio frame time slot, the OTI-610 software driver is able to configure the STLC7549AC to the requirements of the audio subsystem. Conversely, by reading the data in the appropriate incoming audio frame time slot, the OTI-610 software driver is able to determine the status of the STLC7549AC and modify it accordingly during the next frame (if necessary).

For complete specification and implementation details for the STLC7549AC, please consult the STLC7549AC data sheet or contact SGS Thomson.

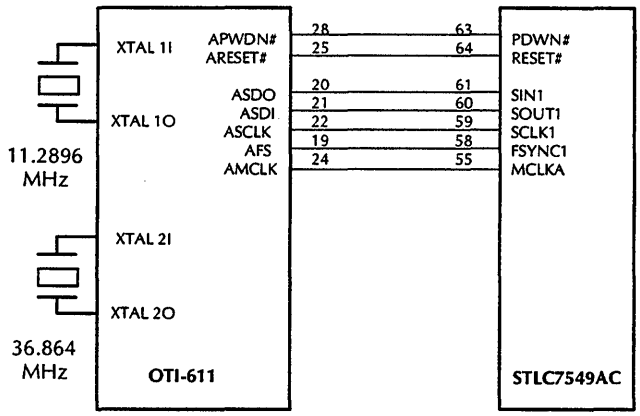

Figure 3-10: *Audio Codec Interface (OTI-610 to SG7549AC)*

3.6 DUAL CODEC (AUDIO AND MODEM) INTERFACE (OTI-611 TO AD1843)

The AD1843 Serial Port 16-bit SoundComm Codec from Analog Devices, Inc. is a SD-type dual audio and modem codec device with a TDM interface similar to AC-Link. It is available in the 80-pin PQFP package or the 100-pin TQFP package. For this discussion, it is assumed that the pin numbers used in the illustrations are for the 80-pin PQFP package.

AC timing diagrams and the timing parameter table for the OTI-611 connection to the AD1843 are found in Section 9.8 (Chapter 9).

The AD1843 can operate in two modes: bus master and bus slave. The mode is controlled by the BM pin. When tied to Vdd (+3.3V or +5.0V), the AD1843 is a bus master. When tied to Vss (0V), the AD1843 is a bus slave. If used in the bus slave mode, two other pins, *TSI* [time slot in] and *TSO* [time slot out], may be required.

The BM pin selected mode of the AD1843 also controls the direction of the AD1843 *(SCLK)* and *(SDFS)* signals. In the bus master mode, these signals are outputs to the OTI-611. In the bus slave mode, these signals are inputs from the OTI-611.

The OTI-611 is designed to work with the AD1843 in the bus master mode only.

The TDM data and clocking interface consists primarily of the signals ARESET# *(RESET#)*, ASCLK *(SCLK)*, AFS *(SDFS)*, ASDO *(SDO)*, and ASDI *(SDI)*. Both audio and modem data are carried on this interface, with particular time slots assigned to each data type.

The AD1843 also provides three conversion clock outputs which may be individually controlled by register programming. When used with the AD1843, the OTI-611 software driver configures conversion clocks 1 and 2 to support the generation of the modem master clock (via the ACONV1 input pin on the OTI-611) and frame sync (the MFS input pin) requirement of the OTI-611 when performing modem functions. Serial bit clock input — MSCLK — is shared with ASCLK *(SCLK)*. In this fashion, a direct interface between the OTI-610 and AD1843 is achieved with the required sample rates for high-quality audio (up to 48 KHz) and for support of V.34/V.34+ fax/data modem communications, which have lower sample rates.

For complete specification and implementation details for the AD1843, consult the AD1843 data sheet or contact Analog Devices, Inc.

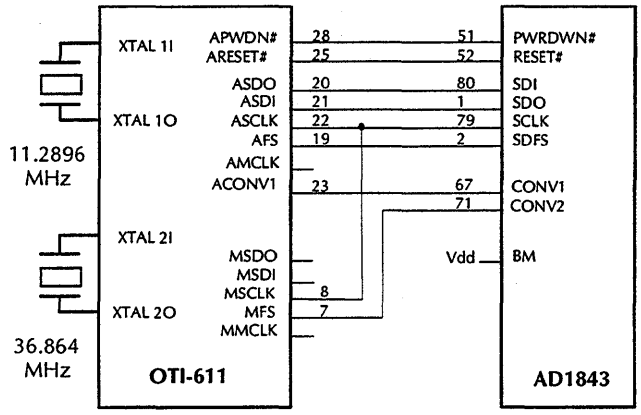

Figure 3-11: *Dual-Codec (Audio and Modem) Interface — OTI-611 to AD1843*

CHAPTER 4 PERIPHERAL INTERFACES

4.1 MUSICAL INSTRUMENT DIGITAL INTERFACE (MIDI) PORT

The fundamental function of the MIDI interface is to convert parallel data bytes from the computer data bus into the serial MIDI datastream (MIDI OUT) and serial MIDI formatted datastream (MIDI IN) into parallel data for use by the computer (a UART function).

The de facto standard for a PC-based MIDI interface is the Roland MPU-401 interface. The OTI-610 and OTI-611 MIDI interface meets the MPU-401 standard requirements for UART mode operation.

The MIDI IN or MIDI OUT datastream is a unidirectional asynchronous serial bitstream at 31.25 Kbits/sec with 10 bits transmitted per byte (1 start bit, 8 data bits, and 1 stop bit). The MIDI data consists of MIDI messages which control functions of the musical synthesizer such as Note On, Aftertouch, Modulation, and many others. Typical MIDI messages consist of 3 bytes each, although there are variations.

The MIDI 1.0 Specification published by the International MIDI Association provides detailed information on the MIDI protocol and a list of MIDI messages, along with the number of bytes for each MIDI message.

Additional information may be obtained from the MIDI Manufacturers Association.

For both the OTI-610 and OTI-611, MIDI data is passed without alteration — that is, without MIDI Filtering.

Not all MIDI messages will affect the synthesizer to which they are directed due to the many different types of synthesis used on, and the features provided by, music synthesizers on the market. For that reason, a MIDI implementation chart is published for each synthesizer detailing its responses to received MIDI messages, and detailing which MIDI messages it can transmit.

A MIDI implementation chart is published for the OTI-610/OTI-611 supported wavetable synthesizer types. For both the OTI-610 and OTI-611, the optional DSP-based wavetable synthesizer or the HSP-based wavetable synthesizer will respond to MIDI messages according to MIDI implementation charts given for each type. See Appendix B for details.

The MIDI Specification provides for three different MIDI connections, labeled MIDI IN, MIDI OUT, and the optional MIDI THRU. The OTI-610 and OTI-611 provide support for MIDI OUT and MIDI IN data transfer. The OTI-610 or OTI-611 **do not internally provide support for MIDI THRU functions.** External interfaces are commercially available that can provide MIDI THRU capability, if required.

The OTI-610 and OTI-611 MIDI port is implemented with two signals — TXD for MIDI OUT and RXD for MIDI IN. These pins use TTL logic voltage levels. The DC characteristics for these signals are provided in Chapter 9.

IMPORTANT NOTE:

The TXD and RXD signals are intended to be connected to the PC game port connector through a noise suppression RC network.

For proper operation of the MIDI port it is necessary to use an industry-standard MIDI adapter and game port cable that plugs into the game port connector and converts the TTL level signal into a current loop signal for MIDI OUT data. When receiving MIDI IN data, it converts the current loop signal to a TTL level signal. The current loop operation is a requirement of the MIDI Specification for physical electrical connections between MIDI capable devices. The game controller then plugs into the MIDI adapter and game port cable assembly.

If a game controller is plugged directly into the game port connector, be sure that the game controller does not make any connections to the MIDI IN and OUT pin assignments on the game port connector.

The OTI-610/OTI-611 internal port interface includes a 16-byte FIFO memory buffer for both MIDI IN and MIDI OUT data. Incoming MIDI data may be read in register 60h. Outgoing MIDI data is written in register 60h. The MIDI port may be turned on and off by programming register 61h. See Chapter 7, Register Definitions, for more details.

A noise suppression RC network is recommended on the TXD and RXD signals as shown in Figure 4-1 below. Consult the OTI-610/OTI-611 Reference Schematics for component values.

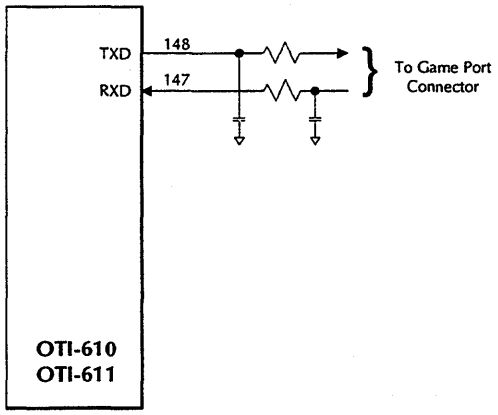

Figure 4-1: *OTI-610/OTI-611 MIDI Interface Simplified Diagram*

4.2 GAME PORT

The OTI-610 and OTI-611 game port interface is designed to work in two modes: 1) hardware polling digital mode and 2) analog mode. The game port control signals include four button signals and four position signals. For both modes, the processing of the button signals are the same. They are not latched, but the switch states are just passed to the data bus when they are required. The position signals are handled differently, depending upon the mode being used.

4.2.1 HARDWARE POLLING DIGITAL MODE

In the hardware polling digital mode, the joystick position information is represented by a time delay value and a digital counter. In this mode, when the OTI-610/OTI-611 Polling Enable bit is set (register 0Ch[7] = 1), a 12-bit internal counter starts counting but will be reset after a fixed time period (9c4h=2500d, 2500ms). This period is the game port sampling frequency.

Time delay signals sent from the NE558-compatible timing circuitry of the OTI-610 and OTI-611 are processed and used to latch the counter value, which is the corresponding joystick position information.

The OTI-610 and OTI-611 support two game controllers, each with two buttons, and one group of positional data containing X and Y 12-bit direction information. The two groups of X,Y positional data are latched into four register addresses: 08h, 09h, 0Ah, and 0Bh. When this information is needed, stable and accurate position data can be read out from these registers.

Button state information may be read from register 0Ch (bits [3:0]).

4.2.2 ANALOG MODE

In the analog mode, game control information can be acquired by either reading the PCI-mapped register 00h (or register 01h, which presents the same information as 00h), or the fixed game port address 200h and 201h. Button signals and unprocessed position signals are passed to the data bus. Software will keep polling these registers for information and does the time delay calculation.

Software polling in the analog mode is slower than for the hardware polled digital mode.

4.2.3 GAME PORT INTERFACE DESCRIPTION

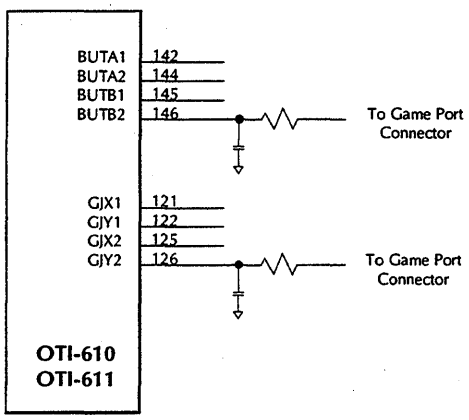

Figure 4-2: *OTI-610/OTI-611 Game Port Interface Simplified Diagram*

The GJX and GJY input pins are for analog voltage inputs from the joystick. Interfacing to the joystick requires an RC timing network at each input. Consult the OTI-610/OTI-611 Reference Schematics available from Oak Technology for component values.

The Joystick Button input pins are internally pulled up to Vdd. A contact de-bounce circuit is recommended on each button signal. Consult the OTI-610/OTI-611 Reference Schematics available from Oak Technology for component values.

Control of the game port is obtained through the game port registers, as listed below. Further details about these registers and the degree of control are available in Chapter 7.

The Standard Game Port register implements the standard analog game port functions. It is accessible from either the Standard Game Port I/O address of 200h/201h or the PCI Offset address of 00h/01h.

Game Port Registers:

Host Offset	Size	Description
00h	8 bit	Standard Game Port
01h	8 bit	Standard Game Port
08h-09h	16 bit	Digital Game Port I & II X Position
0Ah-0Bh	16 bit	Digital Game Port I & II Y Position
0Ch	8 bit	Game Port Control
Address	**Size**	**Description**
200h	8 bit	Standard Game Port
201h	8 bit	Standard Game Port

Standard Game Port

Host Offset: 00h, 01h, 200h, and 0201h

Bit	7	6	5	4	3	2	1	0
R/W	PBB2	PBB1	PAB2	PAB1	PBY	PBX	PAY	PAX
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
PBB2	Port B Button 2	1 - button pressed; 0 - button unpressed
PBB1	Port B Button 1	1 - button pressed; 0 - button unpressed
PAB2	Port A Button 2	1 - button pressed; 0 - button unpressed
PAB1	Port A Button 1	1 - button pressed; 0 - button unpressed
PBY	Port B Y-axis	1 - timer active; 0 - timer inactive
PBX	Port B X-axis	1 - timer active; 0 - timer inactive
PAY	Port A Y-axis	1 - timer active; 0 - timer inactive
PAX	Port A X-axis	1 - timer active; 0 - timer inactive

A write to this port will generate a trigger pulse to the internal 558-like timer. A read from this port will get the current Game Port Button and position status.

At Power On reset, the game port with no hardware polling enabled is set. To use the hardware polling mode, the driver needs to write a value of "1" into register 0Ch, bit position 7.

To use port 200h/201h, register 0Ch, bit position 6 needs to be set to a value of "1." The two modes cannot be activated at the same time. The Power On default value is "0."

4.3 DECODED AUDIO INPUT PORT (I²S PORT)

The I²S port is intended for use as an input for digital audio serial data in the I²S format. An example of digital audio data that may be input to this port is decoded MPEG digital audio serial data.

The I²S port interface consists of three signals:

BCLK - Digital Audio Bit Clock
LRCLK - Left/Right Channel (L/R) Clock
SDATA - Digital Audio Serial Data

These signals may be connected directly the Digital Audio Bit Clock, Left/Right Channel Clock, and Digital Audio Serial Data pins of an I²S bus.

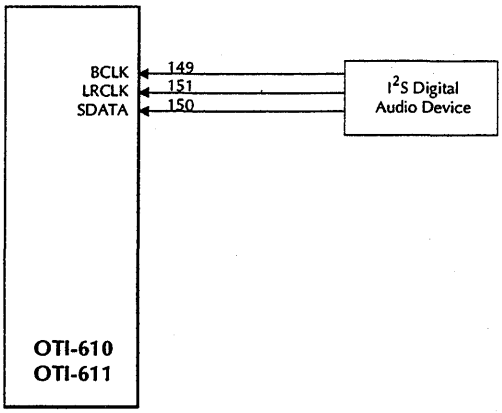

Figure 4-3: *OTI-610/OTI-611 I²S Interface Simplified Diagram*

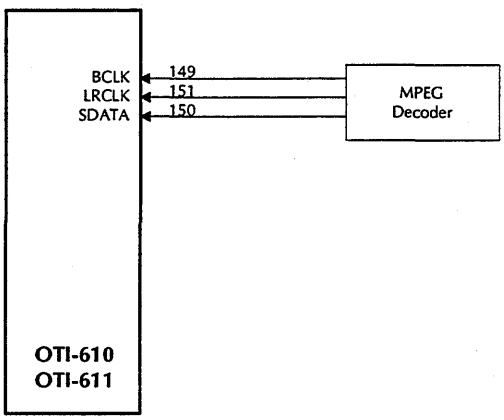

Figure 4-4: *OTI-610/OTI-611 MPEG Decoder Interface Simplified Diagram*

The different modes of operation of the I²S port are controlled by five bits in the OTI-610/OTI-611 Host Offset register 004Fh (see Chapter 7 for more details). The format set in this register must match the input source type for correct operation.

I²S Port

Host Offset Register: 004Fh

Bit	7	6	5	4	3	2	1	0
R/W	Reserved	Reserved	Reserved	ORDER	PACK	LRPOL	EDGE	CYCDLY
Initial	0	0	0	1	0	1	1	0

Bit	Description	Comment
ORDER	Bit Order	1 - MSB first on the data stream; 0 - LSB first on the data stream
PACK	Packing Direction	1 - Forward Packing: Collect data from the start point of L/R signal; 0 - Backward Packing: Collect data from the end point of L/R signal
LRPOL	Left/Right Channel Polarity	1 - HIGH indicates LEFT channel when LRCLK is HIGH; 0 - LOW indicates LEFT channel when LRCLK is LOW
EDGE	Edge Control	1- Latch on RISING edge 0 - Latch on FALLING edge
CYCDLY	Clock Cycle Delay	1 - One clock delay relative to L/R 0 - No delay relative to L/R

The example in Figure 4-5 shows the Right Justified mode. Data is valid on the rising edge of the BCLK signal. The MSB of the data is delayed 16 BCLK cycles from an LRCLK transition. Since there are 64 BCLK cycles per LRCLK period, the LSB of the data is right justified to the next LRCLK transition. This mode may be set with a value of 16h in register 4Fh.

The default mode set by the OTI-610/OTI-611 is 16h in register 4Fh.

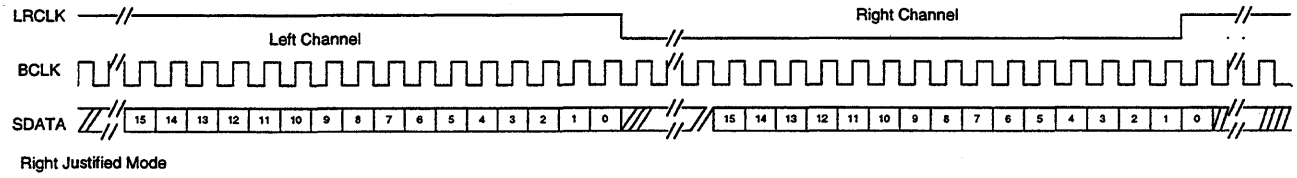

Figure 4-5: *I²S Right Justified Data Input Format*

The example in Figure 4-6 shows the I²S Justified mode. Data is valid on the rising edge of BLCK. LRCLK is high for the Left Channel. In this mode, the MSB is left justified to an LRCLK transition, but with a single BCLK period delay. This mode may be set with a value of 1Bh in register 4Fh.

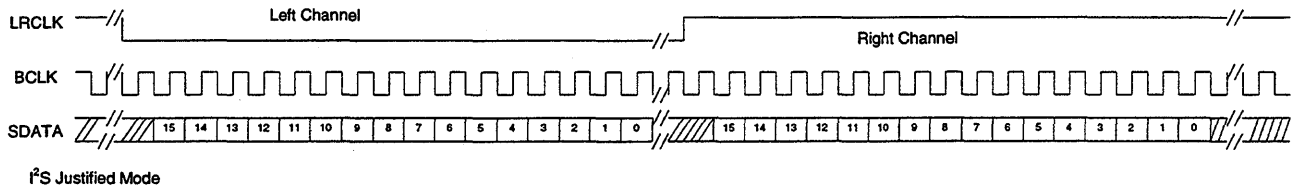

Figure 4-6: *I²S Justified Data Input Format*

The example in Figure 4-7 shows the Left Justified mode. Data is valid on the rising edge of BCLK. This is similar to the I²S Justified mode, but with no BCLK period delay. Also, LRCLK is high for the Left Channel. This mode may be set with a value of 1Dh in register 4Fh.

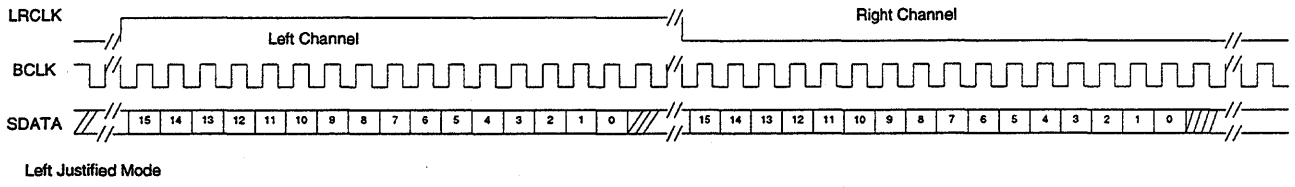

Figure 4-7: *I²S Left Justified Data Input Format*

Digital audio serial data in the I²S format consists of digital audio samples at either a 32-KHz, 44.1-KHz, or 48-KHz rate. The OTI-610/OTI-611 samples the incoming data in register 4Eh to determine the sample rate, and writes a sample rate selection into bits[1:0] of register 49h as follows:

11 = 44.1 KHz
10 = 48 KHz
0X = 32 KHz

The OTI-610/OTI-611 will perform sample rate conversion on the incoming digital audio serial data stream and add it to the digital mix of other digital audio channels.

In the case where the OTI-610/OTI-611 is operating in an AC '97 system (see table in Chapter 3, Section 3.1), the output sample rate of the digital mixer would be set at 48 KHz. If the incoming I²S data were 48 KHz, no conversion would be necessary.

If the OTI-610/OTI-611 were not operating in an AC '97 system, the output sample rate of the digital mixer would be set at 22.05 KHz. Sample rate conversion would be done between the incoming I²S sample rate and the outgoing sample rate.

4.4 PROGRAMMABLE INPUT/OUTPUT PORT

The OTI-610/OTI-611 provides two general purpose, TTL-compatible programmable input/output pins — PIO0 and PIO1. The pin direction is set by programming register 43h in the OTI-610/OTI-611.

Host Offset: 0043h

Bit	7	6	5	4	3	2	1	0
R/W	SRESET	SSIDWR	MCLKSR	Reserved	DC1	PIO1	DC0	PIO0
Initial	0	0	0	0	0	X	0	X

Bit	Description	Comment
SRESET	Software Reset	1 - Reset of OTI-611 similar to use of PCI Reset Signal RST# TOGGLE from 0 to 1 and back to 0
SSIDWR	Subsystem ID Subsystem Vendor ID Write Control	1 - Enable Write of Subsystem ID and Subsystem Vendor ID Registers 0 - Disable Write
MCLKSR	Main Clock (MCLK) source control	1- External MCLK Crystal 0 - Modem Clock Source (36.864 MHz)
PIO[1:0]	General Purpose I/O	Read/Write data to/from external PIO pins
DC1	Direction Control 1	1 - PIO1 is output 0 - PIO1 is input
DC0	Direction Control 0	1 - PIO0 is output 0 - PIO0 is input

I²C is an acronym for Inter-IC bus. The I²C bus is an inexpensive, 2-wire communications link developed by Philips Semiconductors as a simple means for connecting a CPU to peripheral chips or as a link between integrated circuits. The user may program these pins to implement a simple software-controlled I²C interface to one I²C compatible peripheral device. I²C has a fairly low bandwidth, so it is usually used as a control bus, not a high-speed data transfer bus.

The bus physically consists of two active wires and a ground connection. The active wires, SDA and SCL, are bi-directional. SDA is the serial data line and SCL is the serial clock line. Every component hooked up to the bus has its own unique address. Each of these chips can act as a receiver and/or transmitter depending upon its functionality.

More information on the I²C bus can be obtained by contacting Philips Semiconductor. A useful FAQ on the I²C bus also exists at http://www.ecn.uoknor.edu/~jspatric/faqs/i2c.fac

Either PIO0 or PIO1 may be software controlled and used to implement either of the SDA and SCL signals of the I²C protocol.

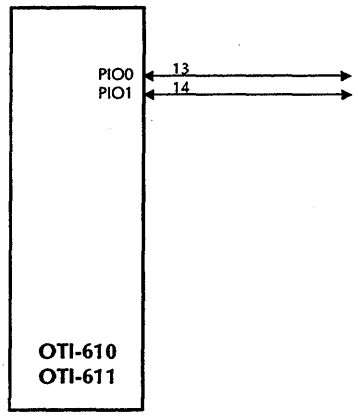

Figure 4-8: *OTI-610/OTI-611 I²C Interface Simplified Diagram*

4.5 DAA INTERFACE

The function of the Data Access Arrangement (DAA) is to interface a fax/data modem and its modem codec to the analog public switched telephone system (PSTN). In many countries, the DAA is required to be approved by the government authorities in a process known as "homologation." The approval requirements dictate the components, and possibly the actual design, that may be used to construct an approved DAA. The OTI-611 provides pre-defined pin functions to support the majority of DAA designs that may be approved throughout the world.

The pins listed in the following table are intended to support the HSP fax/data modem DAA functions, and as such are available only on the OTI-611.

In addition to the pre-defined pin function support, there are three spare output pins and one spare input pin that may be used in support of additional DAA functions or other special system functions.

DAA Interface - 10 pins: 3 inputs, 7 outputs:

Pin Name	Pin #	Type	Description
RING_DET	158	I	**Ring Detect** - OTI-611 only TTL level pulsed DC signal derived from AC Ringing Signal and equal to it in frequency
LC_SENSE	160	I	**Line Current Sense** - OTI-611 only TTL level (High) when line current is sensed
OFF_HOOK	159	O	**Hook Relay Control** - OTI-611 only TTL level (High) to operate OFF HOOK relay
CID_RELAY	1	O	**Caller ID Relay Control** - OTI-611 only TTL level (High) to operate CID relay
HDSET_REL	2	O	**Handset Relay Control** - OTI-611 only TTL level (High) to operate HANDSET relay
CODEC_MODE	3	O	**Codec Mode Select** - OTI-611 only Selects data mode for ST7546 Modem Codec
ISPARE	153	I	**Spare Input Pin** - TTL level input **Modem Wake Up Enable** - This pin is internally pulled up (enabled) and may be tied to Ground to disable the modem wake up feature following a Power Down operation.
OSPARE 0	155	O	**Spare Output Pin** - TTL level output
OSPARE 1	156	O	**Spare Output Pin** - TTL level output
OSPARE 2 MONIT	157	O	**Spare Output Pin** - TTL level output **DSP Monitor** (Diagnostic only)

The DAA interface output lines may be programmed via the OTI-611 Modem Index 2 register (External Outputs register 2h) [15:0] bits.

The DAA interface input state is available by reading the appropriate bits in OTI-611 Index Register 7h.

The bit maps for these registers are given on the following page.

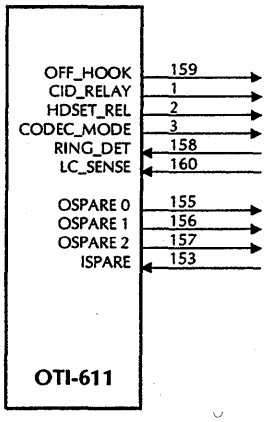

Figure 4-9: *OTI-611 DAA Interface Simplified Diagram*

Modem Index 2 Register: (External Outputs Register 2h) [15:0]

Bit	15	14	13	12	11	10	9	8
R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SPOUT2	SPOUT1
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	SPOUT0	ST7546	HDSTRLY	CODPWR	SPKRMT	CODRST	CID	OHRLY
Initial	0	0	0	0	0	1	1	1

Bit	Description	Comment
SPOUT[2:0]	Spare Output Pins	Software-controlled outputs
ST7546	ST7546 Mode Select	Controls CODEC_PIN on OTI-611. Connects to HC0 pin on ST7546 Modem Codec.
HDSTRLY	Headset (Voice) Relay Control	
CODPWR	Codec Power Down	
SPKRMT	Speaker Mute Control	
CODRST	Codec Reset	0 = Codec Reset
CID	Caller ID Relay Control	Active low
OHRLY	Off-Hook Relay Control	Active low

Default value is 0007h.

Modem Index Register 7h (Low Byte) Read: (External Input Register) [7:0]

Bit	7	6	5	4	3	2	1	0
Read	Reserved	Reserved	Reserved	Reserved	Reserved	ISPARE	LCSNS	RGDET
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
ISPARE	Spare Input Pin	Reads the state of ISPARE pin of OTI-610/OTI-611
LCSNS	Line Current Sense	
RGDET	Ring Detect	

WARNING!

All OTI-611 DAA Interface signal pins either produce or require TTL logic levels, and must be isolated from the DAA connections to the PSTN.

Input signals are typically isolated from the DAA circuits by using optical couplers (opto-isolators).

Output signals are typically connected to transistor-controlled relay driver circuits. The DAA circuit being controlled is isolated by the relay contacts.

DAA design is beyond the scope of this chapter. Consult the OTI-611 Reference Design Schematics for examples of DAA design suitable for use with the OTI-611.

The defined DAA pin functions on the OTI-611 support the host signal processing based V.34/V.34+ fax/data modem software supplied with the OTI-611, provided appropriate hardware is in the DAA circuit. The DAA and HSP V.34/V.34+ software are used together to build a completely functional and approvable V.34/V.34+ fax/data modem, similar to that in Figure 4-10 below.

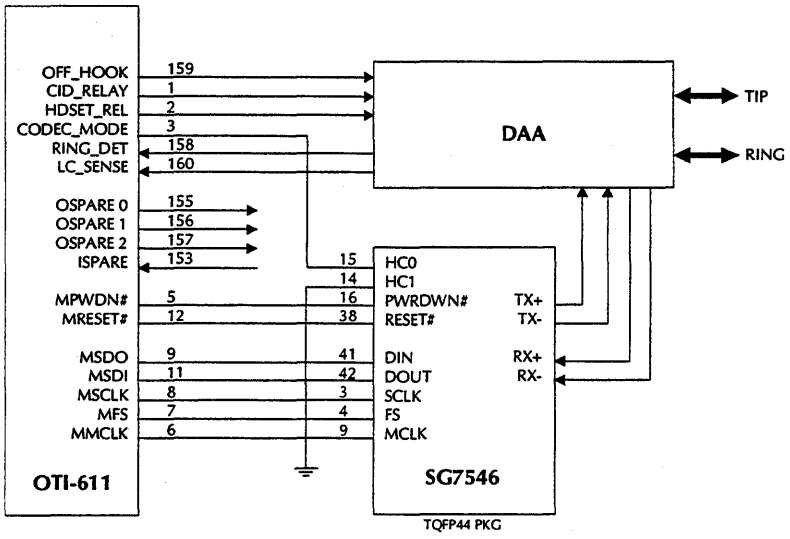

Figure 4-10: *OTI-611 Fax/Data Modem Hardware Implementation Simplified Example*

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CHAPTER 5 MEMORY INTERFACE

The OTI-610 and OTI-611 support an external memory interface to either 2MB of ROM or 2MB of SRAM. Data is transferred to the internal DSP 16 bits at a time (word transfer).

This interface is typically used for the optional DSP-based wavetable synthesizer Sound Sample Set ROM.

5.1 EXTERNAL WAVETABLE SAMPLE SET ROM INTERFACE

The optional DSP wavetable synthesizer uses a 2MB (1Mx16) ROM (UM23C16100M in the example below) to store samples of the 128 General MIDI (GM) instruments sounds and 47 percussion, or drum kit, sounds. In use, the DSP wavetable synthesizer generates musical sounds by reading the samples contained in the ROM, processing those samples within the DSP-based synthesizer engine, and then sending the processed samples to the digital mixer of the OTI-610 and OTI-611. From there, the digitally mixed data is sent to the audio codec for playback.

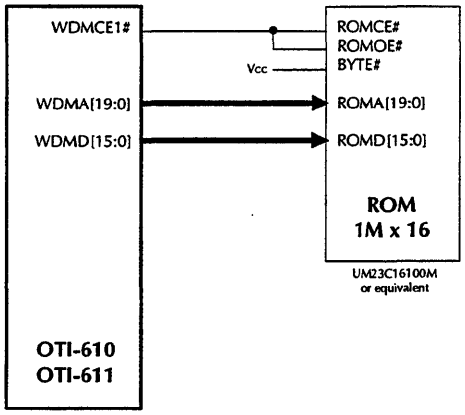

Figure 5-1: *OTI-610/OTI-611 ROM Simplified Interface Diagram*

Sound Sample Set ROM data to the DSP-based synthesizer is obtained 16 bits at a time. Therefore, the BYTE mode of the ROM has been disabled by connecting BYTE# to Vcc. Otherwise, interfacing to the ROM is direct.

Oak Technology provides the Sound Sample Set data patterns required for the ROM as part of the OTI-610 or OTI-611 software drivers to customers who choose to use the optional DSP-based wavetable synthesizer.

Alternatively, the wavetable Sound Sample Set could be stored in SRAM. See Section 5.2 below.

ROM interface timing information is provided in Chapter 10.

The Sound Sample Set data has been specifically developed for use with the OTI-610 and OTI-611 and is not suitable for use with any other wavetable synthesizer.

5.2 SRAM MEMORY INTERFACE TIMING

The SRAM interface capability permits flexibility in the use of the OTI-610 and OTI-611 for a variety of future applications that may be offered or developed for the OTI-610 and OTI-611.

Figure 5.2 below show the basic connections. The implementation is shown for two 512Kx16 SRAM devices. The OTI-610/OTI-611 provides two Chip Enables (WDMCE1# and WDMCE2#) and uses the high-order bit WDMA[19] as a Write Enable (SRAM WE#) to the SRAM. Data is transferred 16 bits at a time.

SRAM interface timing information is provided in Chapter 10.

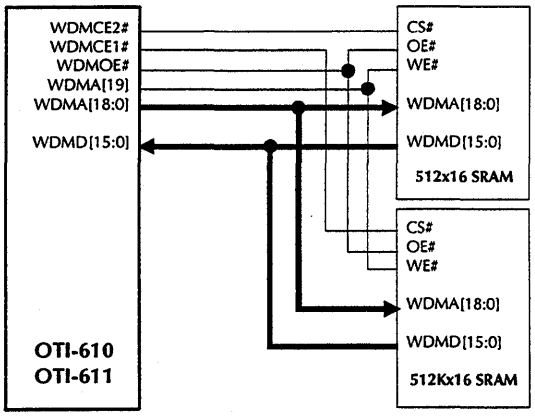

Figure 5-2: *OTI-610/OTI-611 SRAM Simplified Interface Diagram*

CHAPTER 6 PIN DESCRIPTIONS

6.1 OTI-610 PINOUT DIAGRAM

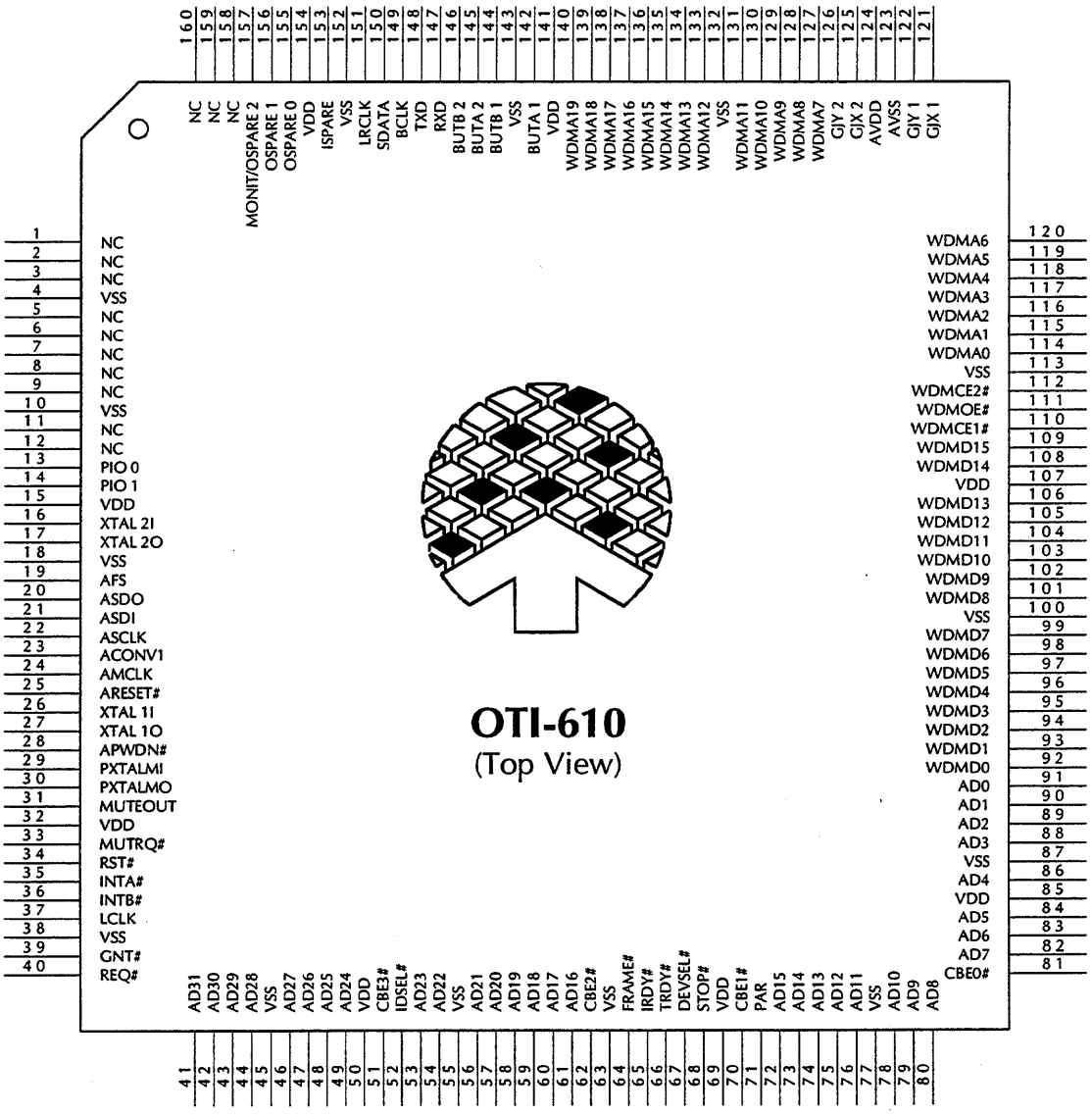

Figure 6-1: *OTI-610 Pinout*

6.2 OTI-611 PINOUT DIAGRAM

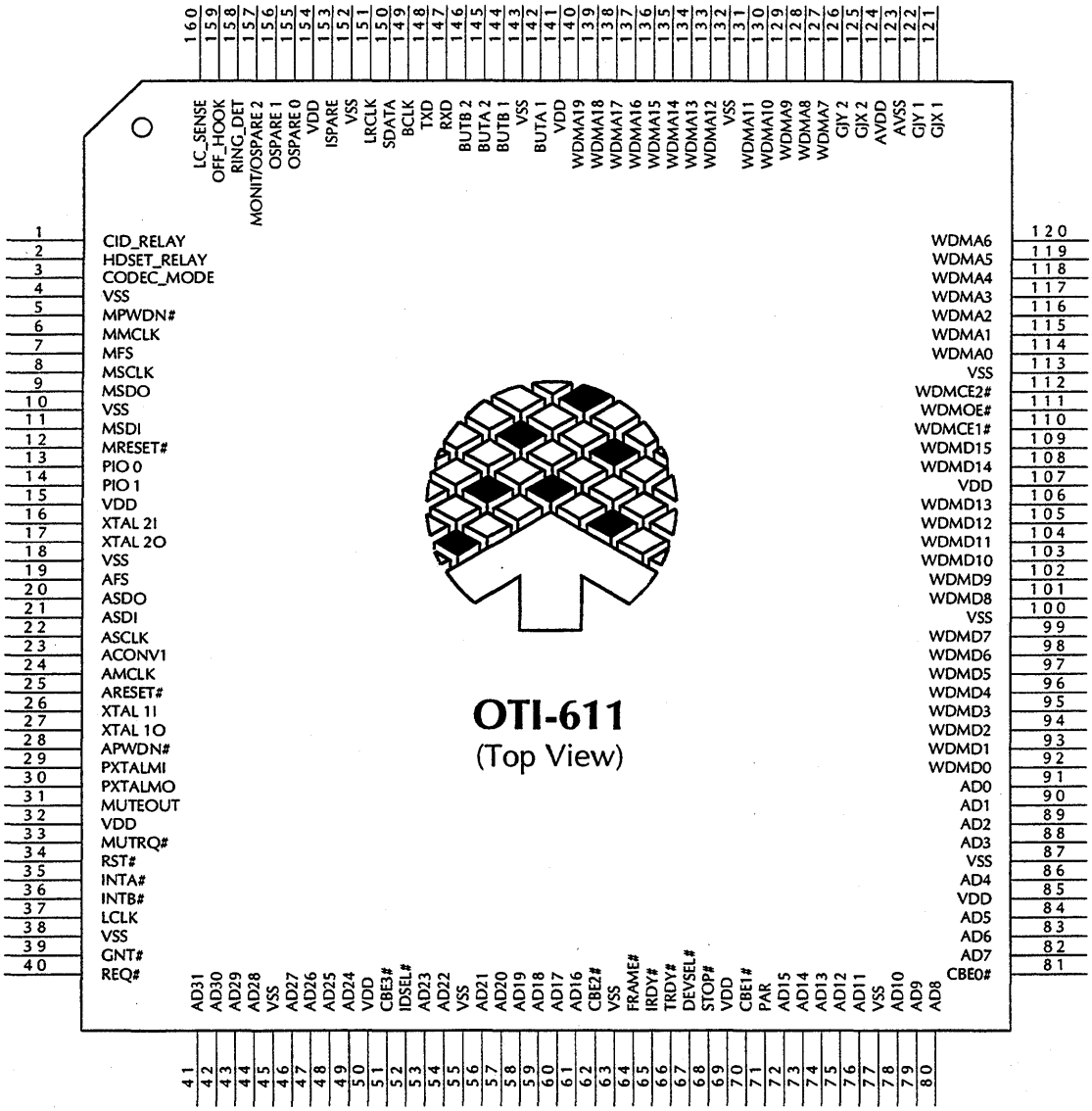

Figure 6-2: *OTI-611 Pinout*

6.3 PIN GROUPING BY FUNCTION

6.3.1 PIN NAMES BY PIN NUMBER

Signal Name	Pin #	Type*	Function
CID_RELAY	1	O	Caller ID Relay control - OTI-611
HDSET_REL	2	O	Handset Relay control - OTI-611
CODEC_MODE	3	O	Mode select for ST7546 Modem Codec - OTI-611
Vss	4	I	Ground input
MPWDN#	5	O	Modem Codec Power Down - OTI-611
MMCLK	6	O	Modem Codec Main Clock - OTI-611
MFS	7	I	Modem Codec Frame Sync - OTI-611
MSCLK	8	I	Modem Codec Serial Clock - OTI-611
MSDO	9	O	Modem Codec Serial Data Out - OTI-611
Vss	10	I	Ground input
MSDI	11	I	Modem Codec Serial Data In - OTI-611
MRESET#	12	O	Modem Codec Reset - OTI-611
PIO0	13	I/O	PIO0 (I^2C clock - programmed output)
PIO1	14	I/O	PIO1 (I^2C data - programmed output)
Vdd	15	I	Voltage input
XTAL2I	16	I	Crystal 2 In (36.864 MHz) - Modem/DSP **Required - Power on default for DSP clock**
XTAL2O	17	O	Crystal 2 Out (36.864 MHz) - Modem/DSP **Required - Power on default for DSP clock**
Vss	18	I	Ground input
AFS	19	I/O	Audio Codec Frame Sync Output for AC '97 Codecs Input for all other Codecs
ASDO	20	O	Audio Codec Serial Data Out
ASDI	21	I	Audio Codec Serial Data In
ASCLK	22	I	Audio Codec Serial Clock
ACONV1	23	I	Audio Codec Conversion Clock 1

Note: * The pins are classified as Input (I), Output (O), or Input/Output (I/O)
# Indicates an active level low signal pin

PIN NAMES BY PIN NUMBER (Cont'd)

Signal Name	Pin #	Type*	Function
AMCLK	24	O	Audio Codec Main Clock
ARESET#	25	O	Audio Codec Reset
XTAL1I	26	I	Crystal 1 In (11.2896 MHz) - Audio Codec clock **Not required when using AC '97 Codec**
XTAL1O	27	O	Crystal 1 Out (11.2896 MHz) - Audio Codec**Clock** **Not required when using AC '97 Codec**
APWDN#	28	O	Audio Codec Power Down
PXTALMI	29	I	Crystal Main In - DSP (optional 33.0 - 40.0 MHz) **If used, SW must change default selection (see XTAL2I)**
PXTALMO	30	O	Crystal Main Out - DSP (optional 33.0 - 40.0 MHz) **If used, SW must change default selection (see XTAL2O)**
MUTEOUT	31	O	Mute Output
Vdd	32	I	Voltage Input
MUTRQ#	33	I	Mute Request
RST#	34	I	Reset Input from PCI Bus
INTA#	35	O	Audio Interrupt
INTB#	36	O	Modem Interrupt - OTI-611 only
LCLK	37	I	PCI Clock
Vss	38	I	Ground input
GNT#	39	I	Bus Grant
REQ#	40	O	Bus Request
AD31-AD28	41-44	I/O	Address/Data bus
Vss	45	I	Ground input
AD27-AD24	46-49	I/O	Address/Data bus
Vdd	50	I	Voltage input
CBE3#	51	I/O	Command/Byte_Enable 3
IDSEL#	52	I	Initialization Device Select
AD23-AD22	53-54	I/O	Address/Data bus
Vss	55	I	Ground input

Note: * The pins are classified as Input (I), Output (O), or Input/Output (I/O)
# Indicates an active level low signal pin

PIN NAMES BY PIN NUMBER (Cont'd)

Signal Name	Pin #	Type*	Function
AD21-AD16	56-61	I/O	Address/Data bus
CBE2#	62	I/O	Command/Byte_Enable 2
Vss	63	I	Ground input
FRAME#	64	I/O	Frame, start of cycle
IRDY#	65	I/O	Initiator Ready
TRDY#	66	I/O	Target Ready
DEVSEL#	67	I/O	Device Select
STOP#	68	I/O	Stop the current cycle
Vdd	69	I	Voltage input
CBE1#	70	I/O	Command/Byte_Enable 1
PAR	71	O	Parity Even
AD15-AD11	72-76	I/O	PCI Address/Data bus
Vss	77	I	Ground input
AD10-AD8	78-80	I/O	PCI Address/Data bus
CBE0#	81	I/O	Command/Byte_Enable 0
AD7-AD5	82-84	I/O	PCI Address/Data bus
Vdd	85	I	Voltage input
AD4	86	I/O	PCI Address/Data bus
Vss	87	I	Ground input
AD3-AD0	88-91	I/O	PCI Address/Data bus
WDMD0-WDMD7 VENDID0-VENDID7	92-99	I/O I	External SRAM/ROM Data Power Up: Subsystem Vendor ID[0:7]
Vss	100	I	Ground input
WDMD8-WDMD13 VENDID8-VENDID13	101-106	I/O I	External SRAM/ROM Data Power Up: Subsystem Vendor ID[8:13]
Vdd	107	I	Voltage input
WDMD14-WDMD15 VENDID14-VENDID15	108-109	I/O I	External SRAM/ROM Data Power Up: Subsystem Vendor ID[14:15]

Note: * The pins are classified as Input (I), Output (O), or Input/Output (I/O)
# Indicates an active level low signal pin

PIN NAMES BY PIN NUMBER (Cont'd)

Signal Name	Pin #	Type*	Function
WDMCE1#	110	O	External SRAM/ROM Chip Enable 1
WDMOE#	111	O	External SRAM/ROM Output Enable
WDMCE2#	112	O	External SRAM/ROM Chip Enable 2
Vss	113	I	Ground input
WDMA0 BUS_MODE	114	O I	External SRAM/ROM Address Power Up: 1 = PCI Bus; 0 = AuxBus
WDMA1	115	O I	External SRAM/ROM Address Power UP: Game Port Enable/Disable Selection 1 = Game Port Enabled (no internal pullup); 0 = Game Port, including configuration, Disabled
WDMA2-WDMA4 BODID[0:2]	116-118	O I	External SRAM/ROM Address Power Up: Board ID[0:2]
WDMA5 MCODEC (0)	119	O I	External SRAM/ROM Address Power Up: Codec Selection bit 0
WDMA6 MCODEC (1)	120	O I	External SRAM/ROM Address Power Up: Codec Selection bit 1
GJX1, GJY1	121-122	I	Joystick 1 location: X,Y
AVss	123	I	Analog Ground input
AVdd	124	I	Analog Voltage input
GJX2, GJY2	125-126	I	Joystick 2 location: X,Y
WDMA7 MCODEC (2)	127	O I	External SRAM/ROM Address Power Up: Codec Selection bit 2
WDMA8-WDMA11 SSYSID0-SSYSID3	128-131	O I	External SRAM/ROM Address Power Up: Subsystem ID[0:3]
Vss	132	I	Ground input
WDMA12-WDMA18 SSYSID4-SSYSID10	133-139	O I	External SRAM/ROM Address Power Up: Subsystem ID[4:10]
WDMA[19] WEMWE#	140	O O	External ROM Address External SRAM Write Enable Diagnostic
Vdd	141	I	Voltage input
BUTA1	142	I	Game Port I Button A
Vss	143	I	Ground input

Note: * The pins are classified as Input (I), Output (O), or Input/Output (I/O)
# Indicates an active level low signal pin

PIN NAMES BY PIN NUMBER (Cont'd)

Signal Name	Pin #	Type*	Function
BUTB1	144	I	Game Port I Button B
BUTA2	145	I	Game Port II Button A
BUTB2	146	I	Game Port II Button B
RxD	147	I	MIDI Receive data
TxD	148	O	MIDI Transmit data
BCLK	149	I	I^2S Bit Clock
SDATA	150	I	I^2S Serial data
LRCLK	151	I	I^2S Left/Right Clock
Vss	152	I	Ground input
ISPARE	153	I	Spare Input pin Enable Modem Wake-Up - via internal Ring Detect This feature set by external connection to ground
Vdd	154	I	Voltage input
OSPARE [1:0]	155-156	O	Spare Output pins 0 and 1
MONIT/OSPARE2	157	O	DSP MIPS Monitor (diagnostic only) Spare Output pin 2
RING_DET	158	I	Ring Detect - OTI-611 only
OFF_HOOK	159	O	Hook Relay control - OTI-611 only
LC_SENSE	160	I	Line Current detect - OTI-611 only

Note: * The pins are classified as Input (I), Output (O), or Input/Output (I/O)
# Indicates an active level low signal pin

6.4 PIN DESCRIPTIONS BY INTERFACE

6.4.1 PCI INTERFACE

PCI Interface - 49 pins: 4 inputs, 4 outputs, 41 I/O

Pin Name	Pin #	Type	I/O	Description
LCLK	37	TTL	I	**PCI CLOCK.** Used to provide timing for all transactions on PCI. All other PCI signals are sampled on the rising edge of LCLK, and all timing parameters are defined with respect to the rising edge of LCLK.
RST#	34	TTL Schmidt	I	**RESET.** This signal resets all internal state machines and default registers. Also used to latch-in configuration register values.
FRAME#	64	PCI	I/O	**CYCLE FRAME.** Used to indicate the beginning and duration of an access. This signal is an input during Slave mode and an output during Master mode.
IRDY#	65	PCI	I/O	**INITIATOR READY.** Used to indicate the initiating agent's ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. This signal is an input during Slave mode and an output during Master mode.
TRDY#	66	PCI	I/O	**TARGET READY.** Used to indicate the target agent's ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#.
STOP#	68	PCI	I/O	**STOP.** Active low signal used by the current Slave to request the current Master to stop the current transaction. This signal is an output during Slave mode and an input during Master mode.
IDSEL#	52	TTL	I	**INITIALIZATION DEVICE SELECT.** Active high chip select in lieu of the upper 24 address lines during configuration Read and Write transactions.
DEVSEL#	67	PCI	I/O	**DEVICE SELECT**
PAR	71	PCI	O	**PARITY.** Active high even parity across AC[31:0] and CBE#[3:0]
AD[31:0]	Refer to pin table	PCI	I/O	**Address/Data Bus**
CBE#[3:0]	Refer to pin table	PCI	I/O	**Command/Byte_Enable**
REQ#	40	PCI	O	**REQUEST.** Output to the PCI bus arbiter to request for the bus.
GNT#	39	TTL Pullup	I	**GRANT.** Input from the bus arbiter to indicate that the bus has been granted.
INTA#	35	PCI	O	**Audio Interrupt**
INTB#	36	PCI	O	**Modem Interrupt**

6.4.2 MPEG AND MIDI INTERFACE

MPEG/MIDI Interface - 5 pins: 4 inputs, 1 output

Pin Name	Pin #	Type	I/O	Description
BCLK	149	TTL	I	I²S Digital Audio Bit Clock
LRCLK	151	TTL	I	I²S Left/Right Channel (L/R) Clock
SDATA	150	TTL	I	I²S Digital Audio Serial Data
RxD	147	TTL Schmidt	I	MIDI Receive Serial Data
TxD	148	18mA	O	MIDI Transmit Serial Data

6.4.3 EXTERNAL MEMORY INTERFACE

Memory Interface (for ROM or RAM) - 39 pins: 23 outputs, 16 I/Os

Pin Name	Pin #	Type	I/O	Description
WDMCE1#	110	4mA	O	External SRAM/ROM Chip Enable 1
WDMCE2#	112	4mA	O	External SRAM/ROM Chip Enable 2
WDMOE#	111	4mA	O	External SRAM/ROM Output Enable
WDMA[19] WEMWE#	140	4mA	O O	External ROM Address External SRAM Write Enable
WDMD[15:0] VENDID[15:0]	Refer to pin table	4mA pullup	I/O I	External SRAM/ROM Data Power Up: Subsystem Vendor ID[15:0]
WDMA[0] BUS_MODE	114	4mA	O I	External SRAM/ROM Address 1 = PCI, 0 = AuxBus
WDMA[1]	115	4mA	O I	External SRAM/ROM Address Power Up: Game Port Enable/Disable Selection 1 = Game Port Enabled (Internal pullup) 0 = Game Port, and configuration, Disabled
WDMA[4:2] BODID[2:0]	Refer to pin table	4mA	O I	External SRAM/ROM Address Power Up: Board ID
WDMA[5] MCODEC (0)	119	4mA	O I	External SRAM/ROM Address Refer to Codec Support Table
WDMA[6] MCODEC (1)	120	4mA	O I	External SRAM/ROM Address Refer to Codec Support Table
WDMA[7] MCODEC (2)	127	4mA	O I	External SRAM/ROM Address Refer to Codec Support Table
WDMA[18:8] SSYSID[10:0]	Refer to pin table	4mA	O I	External SRAM/ROM Address Power Up: Subsystem ID[10:0]

The input data on WDMA[7:5] pins is used at Power Up to inform the OTI-610/OTI-611 what codec or codec combination is attached to the codec interface. The data is also placed in the OTI-610/OTI-611 Status register 42h. This data is then used by the software driver to configure the attached codec(s).

The table below presents the codec options supported.

Codec Supported	OTI-610/OTI-611 Signal Name		
	WDMA[7] (MCODEC bit 2)	WDMA[6] (MCODEC bit 1)	WDMA[5] (MCODEC bit 0)
AD1843 as Audio/Modem Codec	0	0	0
Reserved	0	0	1
AD1843 as Audio Codec plus ST7546 Modem Modec	0	1	0
Reserved Audio Codec plus ST7546 Modem Codec	0	1	1
STLC7549 Audio/Modem Codec	1	0	0
OTI-612 AC '97 Audio/Modem Codec or Any AC '97 Audio/Modem Codec	1	0	1
AC '97 Audio Codec plus ST7546 Modem Codec	1	1	0
Reserved	1	1	1

6.4.4 AUDIO CODEC INTERFACE

Audio Codec Interface - 8 pins: 4 inputs, 4 outputs

Pin Name	Pin #	Type	I/O	Description
AMCLK	24	4mA	O	Audio Codec Main Clock
ASCLK	22	TTL	I	Audio Codec Serial Clock
AFS	19	TTL	O I	Audio Codec Frame Sync Output for AC '97 Codecs Input for all other Codecs
ASDI	21	TTL pullup	I	Audio Codec Serial Data In
ACONV1	23	TTL	I	Audio Codec Conversion Clock (for AD1843 Codec)
ASDO	20	4mA	O	Audio Codec Serial Data Out
ARESET#	25	4mA	O	Audio Codec Reset
APWDN#	28	4mA	O	Audio Codec Power Down

6.4.5 CLOCKS AND MISCELLANEOUS INTERFACE

Clock and Miscellaneous Interface - 8 pins: 4 inputs, 4 outputs

Pin Name	Pin #	Type	I/O	Description
PXTALMI	29	TTL	I	Crystal Main In (33 - 40 MHz) - DSP **Optional**
PXTALMO	30	2mA	O	Crystal Main Out (33 - 40 MHz) - DSP **Optional**
XTAL1I	26	TTL	I	Crystal 1 In (11.2896 MHz) - Audio **Not required when using AC '97 Codec**
XTAL1O	27	2mA	O	Crystal 1 Out (11.2896 MHz) - Audio **Not required when using AC '97 Codec**
XTAL2I	16	TTL	I	Crystal 2 In (36.864 MHz) - Modem/DSP **Required - Power on default for DSP clock**
XTAL2O	17	2mA	O	Crystal 2 Out (36.864 MHz) - Modem/DSP **Required - Power on default for DSP clock**
MUTRQ#	33	TTL Schmidt	I	Mute Request
MUTEOUT	31	4mA	O	Mute Output

6.4.6 DAA INTERFACE

DAA Interface - 8 pins: 3 inputs, 5 outputs

Pin Name	Pin #	Type	I/O	Description
RING_DET	158	TTL	I	Ring Detect - OTI-611
LC_SENSE	160	TTL	I	Line Current Sense - OTI-611
ISPARE	153	TTL	I	Spare Input Pin Modem Wake Up - via internal Ring Detect Set to ground to enable this feature
OFF_HOOK	159	4mA	O	Hook Relay Control - OTI-611
CID_RELAY	1	4mA	O	Caller ID Relay Control - OTI-611
HDSET_REL	2	4mA	O	Handset Relay Control - OTI-611
OSPARE[1:0]	156,155	4mA	O	Spare Output Pins
MONIT/OSPARE2	157	4mA	O	DSP Monitor (diagnostic only) Spare Output Pin

6.4.7 MODEM CODEC INTERFACE

Modem Codec Interface - 8 pins: 3 inputs, 5 outputs

Pin Name	Pin #	Type	I/O	Description
MMCLK	6	4mA	O	Modem Codec Main Clock - OTI-611
MSCLK	8	TTL	I	Modem Codec Serial Clock - OTI-611 only
MFS/ACONV2	7	TTL	I I	Modem Codec Frame Sync - OTI-611 Modem Codec Conversion Clock II (For AD1843 Codec)
MSDI	11	TTL	I	Modem Codec Serial Data In - OTI-611
MSDO	9	4mA	O	Modem Codec Serial Data Out - OTI-611
MRESET#	12	4mA	O	Modem Codec Reset - OTI-611
MPWDN#	5	4mA	O	Modem Codec Power Down - OTI-611
CODEC_MODE	3	4mA	O	Mode Select for ST7546 Modem Codec

6.4.8 PIO AND GAME PORT INTERFACE

PIO/Game Interface - 10 pins: 8 inputs, 2 I/Os

Pin Name	Pin #	Type	I/O	Description
PIO0	13	TTL Pullup 4mA	I O	PIO0 - Input PIO0 - (I^2C clock) - Programmed Output
PIO1	14	TTL Pullup 4mA	I O	PIO1 - Input PIO1 - (I^2C clock) - Programmed Output
BUTA1, BUTB1	142,144	TTL Pullup	I	Game Port 1 buttons
GJX1, GJY1	121-122	Analog	I	Joystick 1 location: X,Y
BUTA2, BUTB2	145-146	TTL Pullup	I	Game Port 2 buttons
GJX2, GJY2	125-126	Analog	I	Joystick 2 location: X,Y

6.4.9 POWER

Power - 24 pins

Pin Name	Pin #	Type	I/O	Description
Avdd	124		I	Analog Voltage input
Avss	123		I	Analog Ground input
Vss[13:0]	Refer to pin table		I	Ground input
Vdd[7:0]	Refer to pin table		I	Voltage input

Note: All input pins, excluding the clock inputs, have pull up resistors

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CHAPTER 7 REGISTER DEFINITIONS

The register structure of the OTI-610 and OTI-611 consists of a base address within the PCI configuration register structure to which an offset address is added to obtain the address of the control registers of the OTI-610/ OTI-611. There is a default base address upon Power On, but the operating system may change the base address.

Each logical device within the OTI-610 and OTI-611 has its own Base Address register within the PCI configuration space. Thus, each logical device has its own group of offset registers. In cases where the Offset Register Number may be duplicated, it actually belongs to a different logical device unless there is a specific notation that the register is shared across one or more logical devices. Not all possible register numbers are used. Only those listed are valid Offset Register Numbers. The remaining possible numbers are either not implemented or reserved.

The logical devices referred to are: Game Port Device, Audio Device, and Modem Device.

Modem Control Function registers are applicable to the OTI-611 only.

7.1 NUMERICAL LISTINGS OF REGISTERS

7.1.1 GAME PORT FUNCTION REGISTERS

Game Port Register Number	Register Name	Page Number
00h	PCI Game Port	7-52
01h	PCI Game Port (Same as 00h)	7-52
08h-09h	Game Port I & II - X position	7-53
0Ah-0Bh	Game Port I & II - Y position	7-53
0Ch	Game Port Control	7-54
200h	Standard Game Port	7-52
201h	Standard Game Port	7-52

Note: Host Offset relative to Game Port Base Address register

7.1.2 AUDIO FUNCTION REGISTERS

Audio Register Number	Register Name	Page Number
30h-33h	Channel 9 Base Address	7-47
38h-39h	Channel 9 Segment Length	7-48
3Ah-3Bh	Channel 9 Interrupt Count	7-51
3Ch-3Dh	Channel 9 Command	7-49
3Eh-3Fh	Channel 9 Segment Position	7-50
40h	610/611 Status Register	7-20
41h	Miscellaneous Mode	7-21
42h	Codec Control	7-22
43h	General Purpose I/O & Crystal Source for Main Clock	7-23
44h-45h	Interrupt Status	7-24
46h-47h	Interrupt Mask	7-25
48h	Codec Sample Rate Control	7-26
49h	I^2S Control and Status	7-27
4Ah	DSP General Control Register 1	7-28
4Bh	DSP General Control Register 2	7-29
4Ch	Miscellaneous Channel Control	7-30

AUDIO FUNCTION REGISTERS (Cont'd)

Audio Register Number	Register Name	Page Number
4Dh	Power Down Control	7-31
4Eh	I^2S Input Rate Control and Status	7-31
4Fh	I^2S Serial Port Format Control	7-32
50h-51h	Host Interface Register HDR0	7-32
54h-55h	Host Interface Register HDR1	7-33
58h-59h	Host Interface Register HDR2	7-33
5Ch-5Dh	Host Interface Command and Status	7-33
60h	MIDI Data Port	7-34
61h	MIDI Port Command and Status	7-35
62h	MIDI Port Baud Rate Divisor/Loopback	7-35
6Ch	Audio Codec Index Register 2	7-36
6Dh	Audio Codec Index Register 1 Same as 43h in Modem I/O Space	7-37
6Eh-6Fh	Audio Codec Data Same as 44h-45h in Modem I/O Space	7-37
70h-7Fh	Channel 0 Playback Registers	7-42 to 7-45
80h-8Fh	Channel 1 Playback Registers	7-42 to 7-45
90h-9Fh	Channel 2 Playback Registers	7-42 to 7-45
A0h-AFh	Channel 3 Playback Registers	7-42 to 7-45
B0h-BFh	Channel 4 Playback Registers	7-42 to 7-45
C0h-CFh	Channel 5 Playback Registers	7-42 to 7-45
D0h-DFh	Channel 6 Playback Registers	7-42 to 7-45
E0h-EFh	Channel 7 Playback Registers	7-42 to 7-45
F0h-F3h	Channel 8 Base Address	7-47
F4h-F5h	Channel 7 Interrupt Count for Modem	7-46
F8h-F9h	Channel 8 Segment Length	7-48
FCh-FDh	Channel 8 Command	7-49
FEh-FFh	Command 8 Segment Position	7-50

Note: Host Offset relative to Audio Function Base Address register

7.1.3 MODEM CONTROL FUNCTION REGISTERS

The names provided in the following table are provided for reference only. Some registers may have different names and functions depending upon whether or not data is written to or read from the register. **These registers are applicable to the OTI-611 only.**

Modem Control Register Number	Register Name	Page Number
31h	STLC7549 Codec GPIO Data	7-38
40h	Data[7:0]	7-55
41h	Data[15:8]	7-55
42h	Index[7:0]	7-56
43h	Codec Index[7:0] Same as 6Dh in Audio IO space	7-37 7-56
44h	Codec Data[7:0] Same as 6Eh in Audio IO space	7-37 7-57
45h	Codec Data[15:8] Same as 6Fh in Audio IO space	7-37 7-57
46h	ID Same as Index 2 Extout[7:0] register	7-58
47h	IO Space Control	7-58

Note: Host Offset relative to Modem Function Base Address register

7.2 ALPHABETICAL LISTINGS OF REGISTERS

The register names in sections 7.2.1 through 7.2.3 are listed alphabetically and are provided to help the user find the page number on which complete register descriptions are provided.

Note: The register number is relative to the Base Address Register value placed in the Base Address Register (10h) of the PCI configuration space for each type of device. Thus, audio register names are relative to the Audio Configuration Base Address Register value, while game port register names are relative to the Game Port Configuration Base Address Register value. Likewise, modem register names are relative to the Modem Configuration Base Address Register value.

Logically, the OTI-610 is two devices: an audio device and a game port device. Each device has its own configuration space.

Logically, the OTI-611 is three devices: an audio device, a game port device, and a modem device. Each device has its own configuration space.

7.2.1 AUDIO REGISTERS

Register Name	Register Number	Device Type	Page Number
610/611 Status Register	40h	A	7-20
Audio Codec Index Register 2	6Ch	A	7-36
Audio Codec Index Register 1	6Dh	A	7-37
	Same as 43h in Modem I/O space	M	7-56
Audio Codec Data	6Eh-6Fh	A	7-37
	Same as 44h, 45h in Modem I/O space	M	7-57
Channel 0 Playback Registers	70h-7Fh	A	7-42 to 7-45
Channel 1 Playback Registers	80h-8Fh	A	7-42 to 7-45
Channel 2 Playback Registers	90h-9Fh	A	7-42 to 7-45
Channel 3 Playback Registers	A0h-AFh	A	7-42 to 7-45
Channel 4 Playback Registers	B0h-BFh	A	7-42 to 7-45
Channel 5 Playback Registers	C0h-CFh	A	7-42 to 7-45
Channel 6 Playback Registers	D0h-DFh	A	7-42 to 7-45
Channel 7 Playback Registers	E0h-EFh	A	7-42 to 7-45
Channel 7 Interrupt Count	F4h-F5h	A	7-46
Channel 8 Base Address	F0h-F3h	A	7-47
Channel 8 Command	FCh-FDh	A	7-49
Channel 8 Position	FEh-FFh	A	7-50
Channel 8 Segment Length	F8h-F9h	A	7-48
Channel 9 Base Address	30h-33h	A	7-47
Channel 9 Command	3Ch-3Dh	A	7-49
Channel 9 Interrupt Count	3Ah-3Bh	A	7-51
Channel 9 Segment Length	38h-39h	A	7-48
Channel 9 Position	3Eh-3Fh	A	7-50
Codec Control	42h	A	7-22
DSP Interface Codec Sample Rate Control	48h	A	7-26
DSP General Control 1	4Ah	A	7-28

AUDIO REGISTERS (Cont'd)

Register Name	Register Number	Device Type	Page Number
DSP General Control 2	4Bh	A	7-29
General Purpose I/O	43h	A	7-23
Host Interface Register HDR0	50h-51h	A	7-32
Host Interface Register HDR1	54h-55h	A	7-33
Host Interface Register HDR2	58h-59h	A	7-33
Host Interface Command and Status	5Ch-5Dh	A	7-33
I^2S Control and Status	49h	A	7-27
I^2S Input Rate Control and Status	4Eh	A	7-31
I^2S Serial Port Format Control	4Fh	A	7-32
Interrupt Mask	46h-47h	A	7-25
Interrupt Status	44h-45h	A	7-24
MIDI Data Port	60h	A	7-34
MIDI Port Command and Status	61h	A	7-35
MIDI Port Baud Rate Divisor/Loopback	62h	A	7-35
Miscellaneous Channel Control	4Ch	A	7-36
Miscellaneous Mode	41h	A	7-21
Power Down Control	4Dh	A	7-31

Note: Host Offset relative to Audio Base Address register
A = Audio; GP = Game Port; M = Modem

7.2.2 GAME PORT REGISTERS

Register Name	Register Number	Device Type	Page Number
Game Port I & II - X position	08h-09h	GP	7-53
Game Port I & II - Y position	0Ah-0Bh	GP	7-53
Game Port Control	0Ch	GP	7-54
PCI Game Port	00h	GP	7-52
PCI Game Port (Same as 00h)	01h	GP	7-52
Standard Game Port	200h	GP	7-52
Standard Game Port	201h	GP	7-52

Note: Host Offset relative to Game Port Base Address register
A = Audio; GP = Game Port; M = Modem

7.2.3 MODEM REGISTERS

Register Name	Register Number	Device Type	Page Number
CODEC_DATA[7:0]	44h	M	7-57
	Same as 6Eh in Audio IO space		7-37
CODEC_DATA[15:8]	45h	M	7-57
	Same as 6Fh in Audio IO space		7-37
CODEC_INDEX[7:0]	43h	M	7-56
	Same as 6Dh in Audio IO space		7-37
Data[7:0]	40h	M	7-55
Data[15:8]	41h	M	7-55
ID Same as Index 2 ID[7:0] register	46h	M	7-58
Index[7:0]	42h	M	7-56
IO Space Control	47h	M	7-58
STLC7549 Codec GPIO Data	31h	M	7-38

Note: Host Offset relative to Modem Base Address register
A = Audio; GP = Game Port; M = Modem

7.3 PCI CONFIGURATION REGISTERS

7.3.1 AUDIO CONFIGURATION REGISTERS

The OTI-610 and OTI-611 share a common architecture for the audio and game port functions. The PCI configuration registers for audio and game port functions are identical.

The OTI-610 and OTI-611 are logical multi-function devices. The OTI-610 is an audio and a game port device and the OTI-611 is an audio, game port, and modem device.

The table below lists the audio configuration registers common to both the OTI-610 and OTI-611.

Byte 3	Byte 2	Byte 1	Byte 0	Address
06	11	10	4E	00000000h
Status : 0200		Command : 0000		00000004h
04h	01h	00h	B2h	00000008h
00h	80h	Latency Timer	00h	0000000Ch
I/O Base Address Registers (Default 00003Dxx)			01	00000010h
00000000h				00000014h
00000000h				00000018h
00000000h				0000001Ch
00000000h				00000020h
00000000h				00000024h
00000000h				00000028h
Subsystem ID		Subsystem Vendor ID		0000002Ch
00000000h				00000030h
reserved 00000000h				00000034h
reserved 00000000h				00000038h
00h	00h	01h	Interrupt Line	0000003Ch

Note: Values in bold are set to zero.

The Power On default value of the I/O Base Address register (10h-13h) is 00003D01h. Byte 0 is hardwired to 01h to indicate I/O Base. The operating system will overwrite bytes 1, 2, and 3. All audio function registers are offset from the final address value written into bytes 1, 2, and 3 (registers 11h, 12h, 13h) by the operating system.

The configuration space address range is from 00h to 3Fh, but not all addresses are used.

Descriptions of Audio Configuration Registers

Vendor ID **Offset = 00h-01h** **RO**

The Oak Technology Vendor ID is 104Eh.

Device ID **Offset = 02h-03h** **RO**

Device ID is 0611h. The OTI-610 is derived from the OTI-611 and can be identified by checking bit 4 of register 40h of the Audio Configuration Register Space. Refer to the description of register 40h.

Command **Offset = 04h-05h** **R/W**

Bit	Description
15-10	Reserved. Hardwired to 0.
9	Fast Back-to-Back Enable. Hardwired to 0.
8	System Error Enable. Hardwired to 0.
7	Address/Data Stepping. Hardwired to 0.
6	Parity Error Response. OTI-610/OTI-611 ignores this bit. Hardwired to 0.
5	For VGA compatible. Hardwired to 0.
4	Allows OTI-610/OTI-611 to use Memory write and invalidate when acting as bus master. Power on value = 0.
3	For special cycle device. Hardwired to 0.
2	Value of 1 allows OTI-610/OTI-611 to behave as a bus master. Power On value 0.
1	Value of 0 disables the device response, value of 1 allows device to respond to memory space access. OTI-610/OTI-611 has no memory space access. Power On value is 0.
0	Value of 0 disables the device response; value of 1 allows device to respond to I/O space access. Power on value is 0.
13-0	Device ID is 0611h. The OTI-610 is derived from the OTI-611 and can be identified by checking bit 4 of register 40h of the Audio Configuration Register Space. Refer to the description of register 40h.

Status **Offset = 06h-07h** **R/W**

Bit	Description
15	Parity Error Status. No matter command register bit 6. Write a '1' to this location will clear this status. Hardwired to 0.
14	System Error Status. Hardwired to 0.
13	Receive Master Abort. If Master Abort occurs in OTI-610/OTI-611 master mode, the status bit will respond. Writing a "1" to this bit location will reset this status.
12	Receive Target Abort. OTI-610/OTI-611 in Master mode should return the status. Writing a "1" to this bit location will reset the status.
11	Signaled Target Abort. Hardwired to 0.
10-9	Medium DEVSEL#. Hardwired to 01.
8	Parity Error. Hardwired to 0.
7	Fast Back-to-Back. The OTI-610/OTI-611 does not support this function. Hardwired to 0.
6	UDF (User-Defined Features). Hardwired to 0.
5	33-MHz PCICLK. Hardwired to 0.
4-0	Reserved. Hardwired to 0.

Revision ID **Offset = 08h** **RO**

OTI-610/OTI-611 revision ID is B2h

Class and Subclass Code Register **Offset = 09h-0Bh** **RO**
OTI-610/OTI-611 is **Multimedia Class** (Address 0Bh); **Audio Subclass** (Address 0Ah); the interface of audio device (Address 09h)
Class Code = 04h, Subclass Code = 01h, Interface = 00h.

Latency Timer **Offset = 0Dh** **R/W**

Header Type **Offset = 0Eh** **RO**
Read Only = 80h, multi-function device.

IO Base Registers **Offset = 10h-13h** **R/W**
OTI-610/OTI-611 mapped I/O base address registers. OTI-610/OTI-611 I/O decoding logic will compare the content of the I/O base registers (11h, 12h and 13h) and bit 0 of command registers.

Bit	Description
31-8	OS assigned the I/O base.
7-1	Hardwired to 0.
0	Hardwired to 1 to indicate this range is for I/O Base assignment.

Power On value = 00003D01h

Subsystem Vendor ID **Offset = 2Ch** **R/W**
Required by PC '97. For system manufacturer of OTI-610/OTI-611 system. This register will read external pull-up/pull-down values of WDMD[15:0] pins as its initial value during power up. It also can be programmed by BIOS or SW after power up if register 43h, bit 6 (SSIDWR) has been set.

Subsystem ID **Offset = 2Eh** **R/W**
Required by PC '97. For system manufacturer of OTI-610/OTI-611 system. This register will read external pull-up/pull-down values of WDMA[18:8] pins as its initial value during power up. It also can be programmed by BIOS or SW after power up if register 43h, bit 6 (SSIDWR) has been set.

Interrupt Line **Offset = 3Ch** **R/W**
This register is assigned by OS after interrupt rerouting algorithm to tell the device driver which input of the system interrupt controller the device's interrupt pin is connected to.

Interrupt Pin **Offset = 3Dh** **R/W**
Audio function in OTI-610/OTI-611 uses a single interrupt. The interrupt is internal Wired-Or and connected to INTA#.
INTA# = 01h.

The other registers of configuration space are reserved and hardwired to 00h.

7.3.2 GAME PORT CONFIGURATION REGISTERS

The OTI-610 and OTI-611 are logical multi-function devices. The OTI-610 is an audio and a game port device, and the OTI-611 is an audio, game port, and modem device.

The table below lists the game port configuration registers common to both the OTI-610 and OTI-611.

Byte 3	Byte 2	Byte 1	Byte 0	Address
16	11	10	4E	00000000h
Status : 0200		Command : 0000		00000004h
09h	04h	10h	B2h	00000008h
00h	80h	Latency: 00h	00h	0000000Ch
I/O Base Address Registers (Default 00003F0x)			01	00000010h
00000000h				00000014h
00000000h				00000018h
00000000h				0000001Ch
00000000h				00000020h
00000000h				00000024h
00000000h				00000028h
Subsystem ID		Subsystem Vendor ID		0000002Ch
00000000h				00000030h
reserved 00000000h				00000034h
reserved 00000000h				00000038h
00h	00h	00h	Interrupt: 00h	0000003Ch

Note: Values in bold are set to zero.

The Power On default value of the I/O Base Address register (10h-13h) is 00003F01h. The high-order Nibble of byte 0 is part of the I/O Base Address. The low-order Nibble of byte 0 is hardwired to 1h. The operating system will overwrite the high-order Nibble of byte 0, and all of bytes 1, 2, and 3. All audio function registers are offset from the final address value written into the high-order Nibble of byte 0 and bytes 1, 2, and 3 by the operating system.

Configuration space address range is from 00h to 3Fh, but not all addresses are used.

Descriptions of Game Port Configuration Registers

Vendor ID **Offset = 00h-01h** **RO**

The Oak Technology Vendor ID is 104Eh.

Device ID **Offset = 02h-03h** **RO**

Device ID is 1611h. The OTI-610 is derived from the OTI-611 and can be identified by checking bit 4 of register 40h of the audio configuration register space. Refer to the description of register 40h.

Command Register **Offset = 04h-05h** **R/W**

Bit	Description
15-10	Reserved. Hardwired to 0.
9	Fast Back-to-Back Enable. Hardwired to 0.
8	System Error Enable. Hardwired to 0.
7	Address/Data Stepping. Hardwired to 0.
6	Parity Error Response. The OTI-610/OTI-611 ignores this bit. Hardwired to 0.
5	For VGA compatibility. Hardwired to 0.
4	Allows OTI-610/OTI-611 to use memory write and invalidate when acting as bus master. Hardwired to 0.
3	For special cycle device. Hardwired to 0.
2	Value of 1 allows OTI-610/OTI-611 to behave as a bus master. Hardwired to 0.
1	Value of 0 disables the device response; value of 1 allows device to respond to memory space access. The OTI-610/OTI-611 has no memory space access. Power On value is 0.
0	Value of 0 disables the device response; value of 1 allows device to response to I/O space access. Power On value is 0.

Status Register **Offset = 06h-07h** **R/W**

Bit	Description
15	Parity Error Status. No matter command register bit 6. Writing a "1" to this location will clear this status. Hardwired to 0.
14	System Error Status. Hardwired to 0.
13	Receive Master Abort. Hardwired to 0.
12	Receive Target Abort. Hardwired to 0.
11	Signaled Target Abort. Hardwired to 0.
10-9	Medium DEVSEL#. Hardwired to 01.
8	Parity error. Hardwire to 0.
7	Fast back-to-back. OTI-610/OTI-611 does not support this function. Hardwired to 0.
6	UDF (user-defined features). Hardwired to 0.
5	33-MHz PCICLK. Hardwired to 0.
4-0	Reserved. Hardwired to 0.

Revision ID **Offset = 08h** **RO**

OTI-610/OTI-611 revision ID is B2h.

Class and Subclass Code **Offset = 09h-0Bh** **RO**

OTI-610/OTI-611 is **Input device** Class (address 0Bh); **Game Port/Joystick** Subclass (address 0Ah); interface programming interface defined (address 09h)
Class Code = 09h, Subclass Code = 04h, Interface = 10h.

Latency Timer **Offset = 0Dh** **RO**
Read Only registers = 00h

Header Type **Offset = 0Eh** **RO**
Read Only = 80h, multi-function device.

IO Base Registers **Offset = 10h-13h** **R/W**
OTI-610/OTI-611 mapped I/O base address registers.. OTI-610/OTI-611 I/O decoding logic will compare the content of the IO base registers (high-order Nibble of 10h, 11h, 12h, and 13h) and bit 0 of command registers.

Bit	Description
31-4	OS assigned the I/O base.
3-1	Hardwired to 0.
0	Hardwired to 1 to indicate this range is for I/O Base assignment.

Power-on value = 00003F01h

Subsystem Vendor ID **Offset = 2Ch** **R/W**
Required by PC '97. For system manufacturer of OTI-610/OTI-611 system. This register will read external pull-up/pull-down values of WDMD[15:0] pins as its initial value during power up. It also can be programmed by BIOS or SW after power up if register 43h, bit 6 (SSIDWR) has been set (**shared with audio configuration**).

Subsystem ID **Offset = 2E** **R/W**
Required by PC '97. For system manufacturer of OTI-610/OTI-611 system. This register will read external pull-up/pull-down values of WDMA[18:8] pins as its initial value during power up. It also can be programmed by BIOS or SW after power up if register 43h, bit 6 (SSIDWR) has been set **(shared with audio configuration).**

Interrupt Line **Offset = 3Ch** **RO**
Read Only registers = 00h

Interrupt Pin **Offset = 3Dh** **RO**
Read Only registers = 00h

The other registers of configuration space are reserved and hardwired to 00h.

7.3.3 FAX/MODEM CONFIGURATION REGISTERS

The OTI-611 is a multi-function device — an audio, game port, and modem device.

The table below lists the modem configuration registers for the OTI-611.

Byte 3	Byte 2	Byte 1	Byte 0	Address
02	88	10	4E	00000000h
Status : 0200		Command : 0000		00000004h
07h	00h	02h	B2h	00000008h
00h	80h	00h	00h	0000000Ch
I/O Base Address Registers (Default 00003Exx)			01	00000010h
00000000h				00000014h
00000000h				00000018h
00000000h				0000001Ch
00000000h				00000020h
00000000h				00000024h
00000000h				00000028h
Subsystem ID		Subsystem Vendor ID		0000002Ch
00000000h				00000030h
reserved 00000000h				00000034h
reserved 00000000h				00000038h
00h	00h	02h	Interrupt Line	0000003Ch

Note: Values in bold are set to zero.

The power on default value of the I/O Base Address Register (10h-13h) is 00003E01h. Byte 0 is hardwired to 01h to indicate I/O Base. The operating system will overwrite bytes 1, 2, and 3. All audio function registers are offset from the final address value written into bytes 1, 2, and 3 (registers 11h, 12h, and 13h) by the operating system.

Configuration space address range is from 00h to 3Fh, but not all addresses are used.

Descriptions of Fax/Modem Configuration Registers

Vendor ID **Offset = 00h-01h** **RO**
The Oak Technology Vendor ID is 104Eh.

Device ID **Offset = 02h-03h** **RO**
Device ID is 0288h.

Command Register **Offset = 04h-05** **R/W**

Bit	Description
15-10	Reserved. Hardwired to 0.
9	Fast Back-to-Back Enable. Hardwired to 0.
8	System Error Enable. Hardwired to 0.
7	Address/Data Stepping. Hardwired to 0.
6	Parity Error Response. OTI-611 ignores this bit. Hardwired to 0.
5	For VGA compatible. Hardwired to 0.
4	Allow OTI-611 to use memory write and invalidate when acting as bus master. Power On value is 0.
3	For special cycle device. Hardwired to 0.
2	Value of 1 allows OTI-611 to behave as a bus master. Power On value is 0.
1	Value of 0 disables the device response; value of 1 allows device to respond to memory space access. The OTI-611 has no memory space access. Power On value is 0.
0	Value of 0 disable the device response; value of 1 allows device to response to I/O space access. Power On value is 0.

Status Register **Offset = 06h-07h** **R/W**

Bit	Description
15	Parity Error Status. No matter command register bit 6. Writing a "1" to this location will clear this status. Hardwired to 0.
14	System Error Status. Hardwired to 0.
13	Receive Master Abort. If master abort occurs in OTI-611 master mode, the status bit will respond. Writing a "1" to this bit location will reset this status.
12	Receive Target Abort. OTI-611 in master mode should respond with status. Writing a "1" to this bit location will reset the status.
11	Signaled Target Abort. Hardwired to 0.
10-9	Medium DEVSEL#. Hardwired to 01.
8	Parity error. Hardwired to 0.
7	Fast Back-to-Back. The OTI-611 does not support this function. Hardwired to 0.
6	UDF (user-defined features). Hardwired to 0.
5	33-MHz PCICLK. Hardwired to 0.
4-0	Reserved. Hardwired to 0.

Revision ID **Offset = 08h** **RO**
OTI-611 revision ID is B2h

Class and Subclass Code **Offset = 09h-0Bh** **RO**
OTI-611 is **Simple Communication device Class** (address 0Bh), **16550-compatible serial controller.**
Class Code = 07h , Subclass Code = 00h , Interface = 02h.

Latency Timer **Offset = 0Dh** **R/W**

Header Type **Offset = 0Eh** **RO**
Read Only = 80h, multi-function device.

IO Base Registers **Offset = 10h-13h** **R/W**
OTI-611 mapped I/O base address registers. OTI-611 I/O decoding logic will compare the content of the IO base registers (11h, 12h and 13h) and bit 0 of command registers.

Bit	Description
31-8	OS assigned the I/O base.
7-1	Hardwired to 0.
0	Hardwired to 1 to indicate this range is for I/O Base assignment.

Power on value = 00003E01h

Subsystem Vendor ID **Offset = 2Ch** **R/W**
Required by PC '97. For system manufacturers of OTI-611 systems. This register will read external pull-up/pull-down values of WDMD[15:0] pins as its initial value during power up. It also can be programmed by BIOS or SW after power up if register 43h, bit 6 (SSIDWR) has been set (**shared with audio configuration**).

Subsystem ID **Offset = 2Eh** **R/W**
Required by PC '97. For system manufacturers of OTI-611 systems. This register will read external pull-up/pull-down values of WDMA[18:8] pins as its initial value during power up. It also can be programmed by BIOS or SW after power up if register 43h, bit 6 (SSIDWR) has been set **(shared with audio configuration).**

Interrupt Line **Offset = 3Ch** **R/W**
This register is assigned by OS after interrupt rerouting algorithm to tell device driver which input of the system interrupt controller the device's interrupt pin is connected to.

Interrupt Pin **Offset = 3Dh** **RO**
The fax/modem function in the OTI-611 uses a single interrupt. The interrupt is internal Wire-Or and connected to INTB#.
INTB# = 02h.

The other registers of configuration space are reserved and hardwired to 00h.

7.4 GENERAL CONTROL REGISTERS

The registers' locations are linear and byte addresses are Audio I/O Base Address + host offset.

Description of registers are provided by register number and are identified by group in the corresponding section heading.

From the General Control Register Group, certain registers pertain to codec operation. The tables below and on the next page provide a list of those registers.

Host Offset	Size	Description
040h	8 bit	Status Register
041h	8 bit	Miscellaneous Mode
042h	8 bit	Codec Control
043h	8 bit	General Purpose I/O Control
044h-045h	16 bit	Interrupt Status Register
046h-047h	16 bit	Interrupt Mask Register
048h	8 bit	DSP Interface & Codec Sample Rate Control Register
049h	8 bit	MPEG Control and Status
04Ah	8 bit	DSP General Control 1 and DSP Memory Access
04Bh	8 bit	DSP General Control 2
04Ch	8 bit	Miscellaneous Channel Control
04Dh	8 bit	Power Down Control (write only)
04Eh	8 bit	I^2S Input Rate Control and Status
04Fh	8 bit	Digital Audio Serial Port (I^2S) Format Control
50h-51h	16 bit	HDR0 [15:0] - Dual Port Data Register I
54h-55h	16 bit	HDR1 [15:0] - Dual Port Data Register II
58h-59h	16 bit	HDR2 [15:0] - Dual Port Data Register III
5Ch-5Dh	16 bit	HCSR [15:0] - HIP Command/Status Register
060h	8 bit	MPU-401 Data Port
061h	8 bit	MPU-401 Command/Status Port
062h	8 bit	MPU-401 Baud Rate Divisor/Loopback
06Ch	8 bit	Audio Codec Index Register 2
06Dh	8 bit	Audio Codec Index Register 1 Same as 43h in Modem I/O space
06Eh-06Fh	16 bit	Audio Codec Data Register Same as 44h, 45h in Modem I/O space

Access to the external codecs used by the OTI-610 and OTI-611 is via a serial interface. The OTI-610 and OTI-611 translate this internally to a 16-bit parallel interface.

All OTI-610/OTI-611 external codecs use the same index register technique for reading and writing internal codec registers. The individual codec reference must be consulted for register offsets and configurations. The following describes typical codec access sequences for reading and writing codec registers.

Write Codec register:

1) Poll Codec Busy (CB) bit until NOT busy. If time out, reset codec.
2) Write the *Codec Index* register with Codec Read (CRD) bit cleared.
3) Write data to *Codec Data* register.

Read Codec register:

1) Poll Codec Busy (CB) bit until NOT busy. If time out, reset codec.
2) Write the *Codec Index* register with Codec Read (CRD) bit set.
3) Poll Codec Data Valid (CDV) bit until set. If time out, reset codec.
4) Read data from *Codec Data* Register.

Codec Control Register Offsets:

Host Offset	Size	Description
042h	8 bit	Codec Control
048h	8 bit	Codec I/O Sample Rate Control
06Ch	8 bit	Audio Codec Index Register 2
06Dh	8 bit	Audio Codec Index Register 1 Same as 43h in Modem I/O space
06Eh-06Fh	16 bit	Audio Codec Data Register Same as 44h, 45h in Modem I/O space

7.4.1 OTI-610/OTI-611 STATUS REGISTER (READ ONLY)

Host Offset: 0040h

Bit	7	6	5	4	3	2	1	0
Read	CT2	CT1	CT0	PCTel	HI	BID2	BID1	BID0
Initial	0[1]	0[1]	0[1]	X	1	0[1]	0[1]	0[1]

Bit	Description	Comment
CT[2:0]	Codec Type	See table below - State is set by pulldown or pullup values on the following signal pins during Power Up: WDMA[7], WDMA[6], WDMA[5], CT2, CT1, CT0
PCTel	PCTel Present	1 = PCTel H/W (OTI-611) 0 = No PCTel H/W (OTI-610)
HI	Host Interface	Read from WDMA[0] input pins (BUS_MODE) upon Power Up 1 = PCI Bus; 0= AuxBus. Should always be "1".
BID[2:0]	Board ID	Value is board implementation-specific. State is set by pulldown or pullup values on the following signal pins upon Power Up: WDMA[4], WDMA[3], WDMA[2], BID[2], BID[1], BID[0]

Note: [1] Initial value for CT[2:0] bits and BID[2:0] bits is determined by hardware jumpers. If the jumper is pulled down, the logic level in the register is 0 for those bit positions. If the jumper is pulled up, the logic level in the register is 1 for those bit positions. The initial value for these bits if no jumper is present is undetermined.

Codec Type Selection Table:

CT[2:0]	Audio Codec	Modem Codec
0 0 0	AD1843	AD1843
0 0 1	Reserved	Reserved
0 1 0	AD1843	ST7546
0 1 1	Reserved	ST7546
1 0 0	ST7549	ST7549
1 0 1	OTI-612 or AC '97 Dual	OTI-612 or AC '97 Dual
1 1 1	AC '97 Audio	ST7546
1 1 0	Reserved	Reserved

This register describes the hardware configuration of the OTI-610 or OTI-611 implementation.

The HI, PCTel, CT[2:0], and BID[2:0] bits are latched into the register upon Hardware Reset or initial Power Up.

The HI bit is an external pull-down, jumper-selectable, function enable reserved for future use with AuxBus functions. The default value is 1, indicating PCI bus functions. AuxBus functions are not documented and should not be chosen.

The PCTel bit is set to 0 on the OTI-610 and set to 1 on the OTI-611.

The CT[2:0] and BID[2:0] bits are board implementation-specific external pull-down or pull-up jumpers available to the hardware designer to identify a particular board design.

7.4.2 MISCELLANEOUS MODES CONTROL REGISTER

Host Offset: 0041h

Bit	7	6	5	4	3	2	1	0
R/W	AM	SRC2	SRC1	SRC0	OM	Reset	PSM	TM
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
AM	Addressing Mode	Reserved
SRC[2:0]	Observe Mode Signal Source	View Internal signals for Debug purposes
OM	Observe Mode	1 - Enter Observe Mode 0 - Exit Observe Mode
RESET	DSP Software Reset Control	1 - Enter Reset Mode 0 - Exit Reset Mode
PSM	DSP Memory Power Save Mode	1 - Enter Power Save Mode, turn off DSP SRAM clock 0 - Exit Power Save Mode
TM	Internal Test Mode	1 - Enter Test Mode; 0 - Exit Test Mode

Power On default value is 00h.

Power Save Mode causes the OTI-611 to stop the DSP SRAM internal clock and disable all internal circuitry except the host interface to reduce the power consumption of the device for power down mode.

The TM bit will be reset to "0" when the RESET bit is set to "0" in this register.

CAUTION:

Except for the *Power Save Mode* (PSM) bit, this register is used for chip debug and test purposes only. Use carefully to avoid abnormal operation of the OTI-611.

7.4.3 CODEC CONTROL

Host Offset: 0042h

Bit	7	6	5	4	3	2	1	0
R/W	Reserved	Reserved	Reserved	ATE	WRESET	APD	ARESET	AMUTE
Initial	0	0	0	0	0	0	0	1

Bit	Description	Comment
ATE	AC '97 ATE Mode	1 - Enter AC '97 Codec ATE Mode 0 - Exit AC '97 Codec ATE Mode
WRESET	AC '97 Codec Warm Reset	1 - Warm Reset
APD	Audio Codec Power Down	1 - Audio Codec Power Down
ARESET	Audio Codec Reset	Audio Codec Reset: TOGGLE this bit from '0' to '1' and back to '0'
AMUTE	Audio Mute Control	1 - Mute Audio Codec 0 - Unmute Audio Codec

Power On default value is 01h.

This register is dedicated to codec control.

7.4.4 GENERAL PURPOSE I/O CONTROL

Host Offset: 0043h

Bit	7	6	5	4	3	2	1	0
R/W	SRESET	SSIDWR	MCLKSR	Reserved	DC1	GPIO1	DC0	GPIO0
Initial	0	0	0	0	0	X	0	X

Bit	Description	Comment
SRESET	Software Reset	1 - Reset of OTI-611 similar to use of PCI Reset Signal RST# TOGGLE from 0 to 1 and back to 0
SSIDWR	Subsystem ID Subsystem Vendor ID Write Control	1 - Enable Write of Subsytem ID and Subsystem Vendor ID Registers 0 - Disable Write of Subsytem ID and Subsystem Vendor ID Registers
MCLKSR	Main Clock Crystal Source Control	1 - Use External Crystal on PXTALM pins - (33 MHz to 40 MHz) 0 - Use Modem Clock Source (36.864 MHz) on XTAL1 pins only
GPIO[1:0]	General Purpose I/O	Read/Write data to/from external GPIO pins
DC1	Direction Control 1	1 - GPIO1 is output 0 - GPIO1 is input
DC0	Direction Control 0	1 - GPIO0 is output 0 -GPIO0 is input

This register is dedicated to certain control functions of the OTI-610 and OTI-611.

Power On default value is 00000X0X binary.

The General Purpose I/O pins (GPIO[1:0], DC[0:1]) can be used to implement an I²C interface bus.

MCLKSR permits the OTI-610/OTI-611 to run from a single crystal source. The default condition is for using a single crystal — in this case, the crystal used for modem functions. Internally, the modem functions and internal DSP clocking are derived from this source. For the OTI-611, which contains modem functions, this is the most desirable mode. For the OTI-610, which does not contain modem functions, the clocking mechanism for modem functions has been removed, but clocking to the internal DSP has been retained so that the default condition for the OTI-610 is the same as for the OTI-611.

MCLKSR may be set to 1 by software. In this case, the internal DSP clocking is separated from the modem function clocking. The internal DSP may then be run separately from a 33-MHz to 40-MHz crystal attached to the XTAL1 pins. However, for the OTI-611, the modem crystal (36.864 MHz) is still required. It is not required for the OTI-610.

7.4.5 INTERRUPT STATUS REGISTER

Host Offset: 0044h (0044h and 0045h)

Bit	15	14	13	12	11	10	9	8
R/W	Reserved	MUTEI	DSPI	MPU401I	CI1	CI0	Reserved	Reserved
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
MUTEI	H/W Mute Interrupt	1 - H/W Mute state change triggered an interrupt
DSPI	DSP Interrupt	1 - DSP triggered an interrupt
MPU401I	MPU401 Interrupt	1 - MPU401 device caused an interrupt
CI1-CI0	Capture Interrupt	1 - Interrupt occurred on corresponding capture channel (CI1 = Channel 1, CI0 = Channel 0)
PI7-PI0	Playback Interrupt	1 - Interrupt occurred on corresponding playback channel (PI7 = Channel 7 to PI0 = Channel 0)

Power On default value is 0000h.

This is the Interrupt Status register for the host and is written by the OTI-610/OTI-611 hardware to generate host interrupts for each channel.

A "1" read from any bit indicates a pending interrupt request from the corresponding OTI-610/OTI-611 hardware.

Each bit can be RESET to "0" from the Host by writing "1" to each bit location.

Physical host interrupts are enabled and disabled by the **Interrupt Mask** register. The status bits in this register will be active regardless of the state of the corresponding mask bits in the **Interrupt Mask** register.

7.4.6 INTERRUPT MASK REGISTER

Host Offset: 0046h (0046h and 0047h)

Bit	15	14	13	12	11	10	9	8
R/W	Reserved	MUTEIM	DSPIM	MPU401IM	CIM1	CIM0	Reserved	Reserved
Initial	0	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
R/W	PIM7	PIM6	PIM5	PIM4	PIM3	PIM2	PIM1	PIM0
Initial	1	1	1	1	1	1	1	1

Bit	Description	Comment
MUTEIM	Hardware MUTE Interrupt Mask	1 - Mask Mute Interrupt 0 - Allow Mute Interrupt
DSPIM	DSP Interrupt Mask	1 - Mask DSP triggered interrupt 0 - Allow DSP triggered interrupt
MPU401IM	MPU401 Port Interrupt Mask	1 - Mask MPU401 device interrupt 0 - Allow MPU401 device interrupt
CIM1-CIM0	Capture Interrupt Mask	1 - Mask interrupt on corresponding capture channel 0 - Allow interrupt on corresponding capture channel
PIM7-PIM0	Playback Interrupt Mask	1 - Mask interrupt on corresponding playback channel 0 - Allow interrupt on corresponding playback channel

Power On default value is 7FFFh.

This register is used to inhibit external interrupts from being generated by an OTI-610/OTI-611 interrupt source. Only the physical interrupt is masked. The OTI-610/OTI-611 **Interrupt Status** register may be polled to determine if an internal interrupt was generated.

7.4.7 DSP INTERFACE AND CODEC SAMPLE RATE CONTROL REGISTER

Host Offset: 0048h

Bit	7	6	5	4	3	2	1	0
R/W	CPFMT	CPENA	DSPWT	Reserved	Reserved	Reserved	SRC1	SRC0
Initial	1	0	0	0	0	0	1	0

Bit	Description	Comment
CPFMT	Capture Input Format	1 - Stereo 0 - Mono
CPENA	Capture Enable	1 - Capture data will write to internal capture FIFOs 0 - Capture data will be discarded
DSPWT	DSP Memory Interface Wait State Control	1 - Disable. DSP will wait until current memory access cycle is finished. 0 - Force DSP H/W to execute the next instruction without waiting for current external memory access to finish.
SRC[1:0]	Codec Sample Rate Control	See table below.

SRC[1:0]	Sample Rate Control
0 x	11.025 KHz
1 0	22.05 KHz
1 1	44.1 KHz

Power On default value is 82h.

This register is used to control capture data, set external memory interface wait state control, and set the codec sample rate control.

7.4.8 I²S CONTROL AND STATUS

Host Offset: 0049h

Bit	7	6	5	4	3	2	1	0
R/W	MPENA	MUTEST	Reserved	Reserved	Reserved	Reserved	MR1	MR0
Initial	0	0	0	0	0	0	1	0

Bit	Description	Comment
MPENA	I²S Enable	1 - Mix I²S audio input with OTI-610/OTI-611 audio output 0 - Disable I²S audio input mixing
MUTEST	H/W Mute Status	1 - On 0 - Off Set by H/W only, TOGGLED by external 'MUTE' button
MR[1:0]	I²S Sample Rate	See table below. Set by H/W only by sampling external (I²S) audio clock

MR[1:0]	I²S Sample Rate
0 x	32.0 KHz
1 0	48.0 KHz
1 1	44.1 KHz

Power On default value is 02h.

This register is used to enable/disable I²S input source and detect the I²S data sample rate.

The OTI-610/OTI-611 determines the sample rate of the incoming I²S audio data and reports it in this register.

7.4.9 DSP GENERAL CONTROL 1

Host Offset: 004Ah

Bit	7	6	5	4	3	2	1	0
R/W	DIINT	DOINT	DEBUG	PMS	XMS	YMS	WTRAM	WTROM
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
DIINT	DEBUG_IN Interrupt to DSP	Active high
DOINT	DEBUG_OUT Interrupt to DSP	Active high
DEBUG	Debug Enable	1 - OTI-610/OTI-611 DSP is in debug mode 0 - OTI-610/OTI-611 DSP is in normal mode
PMS	Program Memory Select	1 - Select DSP program memory for access 0 - DSP program memory access disabled.
XMS	Register Memory Select	1 - Select DSP data memory ('X' data memory) for access 0 - DSP 'X' data memory access disabled
YMS	Data Memory Select	1 - Select DSP data memory ('Y' data memory) for access 0 - DSP 'Y' data memory access disabled
WTRAM	External SRAM Access	1 - Select external SRAM for access 0 - External SRAM access disabled
WTROM	Specify Wavetable Memory Type	1 - Select memory type as ROM 0 - Select memory type as SRAM

Power On default value is 00h.

The OTI-610/OTI-611 supports direct access to the OTI-610/OTI-611 DSP memory space. The DSP memory space includes internal SRAM, as well as external SRAM or ROM.

To access this memory from the host computer, set one of the four memory select bits (PMS, XMS, YMS, or WTRAM). The memory select bits are mutually exclusive. Operation is undefined if more than one of these bits are set simultaneously.

Setting any of the memory select bits suspends normal operation of the DSP. When all the memory select bits are cleared, the DSP continues where it left off. Care must be taken not to modify data or program memory that the DSP may be utilizing. Failure to do so may result in unstable operation of the OTI-610/OTI-611.

7.4.10 DSP GENERAL CONTROL 2

Host Offset: 004Bh

Bit	7	6	5	4	3	2	1	0
R/W	Reserved	Reserved	Reserved	Reserved	Reserved	MONIT	FIDLE	Reserved
Initial	0	0	0	0	0	0	1	0

Bit	Description	Comment
MONIT	Monitor Select	1 - MONIT/OSPARE3 pin provides DSP monitor ouput 0 - MONIT/OSPARE3 pin used as OSPARE3 output for the DAA interface
FIDLE	Force Idle	1 - Force DSP into idle state 0 - Allow DSP to run normally **See Programming Note**

Power On default is 02h.

PROGRAMMING NOTE:

The FIDLE bit is also set during Power On Reset. Since the OTI-610/OTI-611 firmware is RAM-based, the host must clear this bit after downloading the firmware.

7.4.11 MISCELLANEOUS CHANNEL CONTROL

Host Offset: 004Ch

Bit	7	6	5	4	3	2	1	0
R/W	PCIWS	MID1	MID0	Reserved	Reserved	Reserved	Reserved	MM
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
PCIWS	PCI Interface Wait State Select	1 - 0 wait state 0 - 1 wait state
MID[1:0]	Memory Interface Delay Setting	See table below
MM	MODEM Mode	1 - channel 7 and channel 9 are assigned to MODEM. Interrupt will be directed to INTB. 0 - channel 7 and channel 9 are assigned as audio channels. Interrupt will be directed to INTA.

MID[1:0]	Approximate Delay Length
0 0	5ns
0 1	6ns
1 0	7ns
1 1	9ns

Power On default value is 00h.

The OTI-611 supports bus master communication with the modem codec. In this mode, channel 7 (playback) and channel 9 (capture) cannot be used as audio channels.

When MM is set (modem mode), channel 7 and 9 interrupts are directed to PCI hardware INTB. When MM is cleared (audio mode), channel 7 and 9 interrupts are directed to PCI hardware INTA.

7.4.12 POWER DOWN CONTROL (WRITE ONLY)

Host Offset: 004Dh

Bit	7	6	5	4	3	2	1	0
W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PDWN
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
PDWN	OTI-610/OTI-611 Power Down Mode	1 - Turn off internal 'MCLK' and channel 'LCLK' to reduce steady state current consumption 0 - Return to chip state prior to Power Down

Power On default value is 00h.

This register is write only and activates the OTI-610/OTI-611 Power Down mode. When active ("1"), the OTI-610/OTI-611 goes into a "sleep" mode and will not function normally. It will only respond to PCI configuration cycles and the R/W cycle of this register.

7.4.13 I²S INPUT RATE CONTROL AND STATUS

Host Offset: 004Eh

Bit	7	6	5	4	3	2	1	0
Write	CNTOF7	CNTOF6	CNTOF5	CNTOF4	CNTOF3	CNTOF2	CNTOF1	CNTOF0
Read	SCNT7	SCNT6	SCNT5	SCNT4	SCNT3	SCNT2	SCNT1	SCNT0
Initial	X	X	X	X	X	X	X	X

Bit	Description	Comment
CNTOF[7:0]	Write Only	Offset to LRCLK sampled count in 2's complement form
SCNT[7:0]	Read Only	Sampled Count. LRCLK sampled by MCLK * 8.

Power On default value is XXh (unknown) and depends upon LRCLK state.

This register is used to determine the incoming I²S sample rate. The sum of Count and Offset are used. Offset value = 2's complement value of ROUND(93.54 - 2.83*MCLK).

MCLK in the table and formula is the main crystal frequency (33 MHz or 36.864 MHz)

7.4.14 DIGITAL AUDIO SERIAL PORT (I²S) FORMAT CONTROL (WRITE ONLY)

Host Offset: 004Fh

Bit	7	6	5	4	3	2	1	0
Write	Reserved	Reserved	Reserved	ORDER	PACK	LRPOL	EDGE	CYCDLY
Initial	0	0	0	1	0	1	1	0

Bit	Description	Comment
ORDER	Bit Order	1 - MSB first on the data stream 0 - LSB first on the data stream
PACK	Packing Direction	1 - Forward Packing: Collect data from the start point of L/R signal 0 - Backward Packing: Collect data from the end point of L/R signal
LRPOL	Left/Right Channel Polarity	1 - L/R HIGH indicates LEFT channel 0 - L/R LOW indicates LEFT channel
EDGE	Edge Control	1 - Latch on RISING edge 0 - Latch on FALLING edge
CYCDLY	Clock Cycle Delay	1 - One clock delay relative to L/R 0 - No delay relative to L/R

Power On default value is 16h.

This register is used to set the various possible I²S formats which may be used by the I²S interface of the OTI-610/OTI-611.

7.4.15 HOST INTERFACE PORT (HIP) INTERFACE REGISTERS

This section lists hardware HIP interface registers. The HIP registers are used to transfer information to and from the OTI-610/OTI-611 DSP.

HDR0 - Dual Data Port Register I

Host Offset: 0050h-0051h

Bit	15	14	13	12	11	10	9	8
R/W	D15	D14	D13	D12	D11	D10	D9	D8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	D7	D6	D5	D4	D3	D2	D1	D0
Initial	0	0	0	0	0	0	0	0

HDR1- Dual Data Port Register II

Host Offset: 0054h-0055h

Bit	15	14	13	12	11	10	9	8
R/W	D15	D14	D13	D12	D11	D10	D9	D8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	D7	D6	D5	D4	D3	D2	D1	D0
Initial	0	0	0	0	0	0	0	0

HDR2 - Dual Data Port Register III

Host Offset: 0058h-0059h

Bit	15	14	13	12	11	10	9	8
R/W	D15	D14	D13	D12	D11	D10	D9	D8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	D7	D6	D5	D4	D3	D2	D1	D0
Initial	0	0	0	0	0	0	0	0

HIP Command/Status Register

Host Offset: 005Ch-005Dh

Bit	15	14	13	12	11	10	9	8
R/W	D15	D14	D13	D12	D11	D10	D9	D8
Initial	1	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	D7	D6	D5	D4	D3	D2	D1	D0
Initial	0	0	0	0	0	0	0	0

7.4.16 MPU-401 CONTROL REGISTERS

The MPU-401 compatible MIDI port is controlled with three registers, as shown below.

Host Offset	Size	Description
060h	8 bit	MPU-401 Data Port
061h	8 bit	MPU-401 Command/Status Port
062h	8 bit	MPU-401 Baud Rate Divisor/Loopback

MPU-401 Data Port

Host Offset: 0060h

Bit	7	6	5	4	3	2	1	0
R/W	D7	D6	D5	D4	D3	D2	D1	D0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
D[7:0]	MPU401 Data	Read: MIDI_IN (MPU-401 port) data Write: MIDI_OUT (MPU-401 port) data

This register implements the standard MPU-401 data port functions. It is not, however, accessible at the standard MPU-401 port addresses of 3x0h.

MPU-401 Command/Status Port

Host Offset: 0061h

Bit	7	6	5	4	3	2	1	0
Read	DRR	DTR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Write	D7	D6	D5	D4	D3	D2	D1	D0
Initial	1	1	0	0	0	0	0	0

Bit	Description	Comment
D[7:0]	MPU401 Command	Write: 0FFh - Reset MPU401 UART 03Fh - Enter MPU401 UART mode
DRR	Data Receive Ready (Read)	1 - No data ready 0 - Data ready
DTR	Data Transmit Ready (Read)	1 - Transmitter not ready 0 - Ready to receive command or transmit data

This register implements the standard MPU-401 command/status port functions. It is not, however, accessible at the standard MPU-401 port addresses of 3x1h.

MPU-401 Baud Rate Divisor

Host Offset: 0062h

Bit	7	6	5	4	3	2	1	0
R/W	LB	D6	D5	D4	D3	D2	D1	D0
Initial	0	1	0	0	0	0	1	0

Bit	Description	Comment
LB	Loop Back	1 - Connect TXD output to RXD internally for testing purposes 0 - Normal Operation, RXD connected to external port pin
D[6:0]	Clock Divider	Hexadecimal number, which when multiplied by 16 and divided into MCLK will produce MPU-401 baud rate = 31250 Hz +/- 1% or less

This register sets the internal loopback connections for testing the MPU-401 port.

This register also sets the divisor for the MPU-401 transmit/receive baud rate clock. The Power On default value is 42h. This value corresponds to the divisor needed when using a 33-MHz crystal applied to the PXTALM pins.

PROGRAMMING NOTE:

This register's default value of 42h must be changed by software to the value 49h, which corresponds to using a 36.864-MHz crystal on the modem crystal inputs, XTAL1 pins. This is the default crystal setting for the OTI-610/OTI-611. If the user intends to use a 33-MHz crystal on the PXTALM pins and sets the selection bit 5 in register 43h, then the default value of 42h does not need to be changed.

The baud rate is determined using the following formula applied against the main clock crystal frequency being used by the OTI-610/OTI-611:

MPU-401 baud rate = MCLK / (16 * divisor) = 31.25 KHz

MCLK = OTI-610/OTI-611 Main Clock

divisor = Hexadecimal number to be programmed in register 62h

Register 62h Divisor Value vs. Main Clock Frequency Table:

Main Clock	Divisor (Decimal)	MPU-401 Baud Rate	Divisor (Hex)
30.000 MHz	60	31250	3C
33.333 MHz	66	31250	42
36.864 MHz	73	31562 (+.998% error)	49

7.4.17 CODEC INDEX REGISTER 2

Host Offset: 006Ch

Bit	7	6	5	4	3	2	1	0
R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	INX6	INX5
Initial	X	X	X	X	X	X	0	0

Bit	Description	Comment
INX[6:5]	Codec Register Index Value	MSB[6:5] of Codec Index address. These bits are concatenated with bits INX[4:0] of register 006Dh, Codec Index Register 1 operation.

Power On default value is XXXXXX00 binary.

This register is used in conjunction with register 006Dh to control CODEC index register addressing.

INX[6:5] supports the extended addressing space requirements of the AC '97 Specification.

7.4.18 CODEC INDEX REGISTER 1

Host Offset: 006Dh

Bit	7	6	5	4	3	2	1	0
R/W	CB	DV	CRD	INX4	INX3	INX2	INX1	INX0
Initial	0	0	0	X	X	X	X	X

Bit	Description	Comment
CB	Command Busy Status	1 - Current Index access not yet complete. Set by H/W only 0 - Current Index access complete
DV	Data Valid Status	1 - Current Index register can be read. Set by H/W only. 0 - Current Index register cannot be read
CRD	Codec Read	1 - Codec Write access 0 - Codec Read access
INX[4:0]	Codec Register Index	Codec Register Indexed Address

Power On default value is 000XXXXX binary.

This register is used to control codec operation and codec index address.

7.4.19 CODEC DATA REGISTER

Host Offset: 006Eh-006Fh

Bit	15	14	13	12	11	10	9	8
R/W	CD15	CD14	CD13	CD12	CD11	CD10	CD9	CD8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
CD[15:0]	Codec Register Data	Data from/to register specified in previous Codec Index Register 1 Write: Data for output to Codec Read: Data from Codec

Power On default value is 00h.

7.4.20 STLC7549 GPIO DATA REGISTER

Host Offset: 6D = 31h

Bit	7	6	5	4	3	2	1	0
R/W	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
GPIO[7:0]	GPIO Data	STLC7549 Dual Codec GPIO port control

This is a special register to support ST7549 GPIO pins. The content of this register will pass to ST7549 through the serial data stream on a dedicated GPIO slot.

7.5 CHANNEL REGISTERS

The OTI-610/OTI-611 supports eight individual playback channels and two capture channels. All playback channels operate alike and all capture channels operate alike. The only difference is the host offset. The tables below list the host offset of each register for all capture channels and all playback channels.

Playback channels can operate in two addressing modes — sequential and random. Sequential mode is used by host-driven playback and is so named because the OTI-610/OTI-611 receives a sequential stream of audio data without any knowledge of its position in the audio stream. The host can initiate random access of the sequential stream by stopping playback and restarting from a different buffer location. Playback channel random mode is used solely by the OTI-610/OTI-611 to access Chorus and Reverb delay buffers for the DSP-based wavetable synthesizer.

Capture Channel Register Offsets

Host Offset	Mode	Size	Name	Description
0F0h-0F3h	Capture	32 bit	Channel 8 Base Address	Physical system memory address
0F8h-0F9h		16 bit	Channel 8 Segment Length	# of samples to fetch
0FCh-0FDh		16 bit	Channel 8 Command	Start/stop, reset control, status data format (8/16, mono/stereo)
0FEh-0FFh		16 bit	Channel 8 Position	Current length counter (buffer pointer)
030h-033h	Effects/ MODE M	32 bit	Channel 9 Base Address	Physical system memory address
038h-039h		16 bit	Channel 9 Segment Length	# of samples to fetch
03Ah-03Bh		16 bit	Channel 9 Interrupt Count	IRQ count: for modem operation as Overrun/ Underrun count
03Ch-03Dh		16 bit	Channel 9 Command	Start/stop, reset control, status data format (8/16, mono/stereo)
03Eh-03Fh		16 bit	Channel 9 Position	Current length counter (buffer pointer)

Playback Registers

Host Offset	Mode	Size	Name	Description
070h-073h	Playback	32 bit	Channel 0 Base Address 0	Physical system memory address
074h-077h		32 bit	Channel 0 Base Address 1	Physical system memory address
078h-079h		16 bit	Channel 0 Segment Length 0	# of samples to fetch
07Ah-07Bh		16 bit	Channel 0 Segment Length 1	# of samples to fetch
07Ch-07Dh		16 bit	Channel 0 Command	Start/stop, reset control, status, data format (8/16, mono/stereo)
07Eh-07Fh		16 bit	Channel 0 Position	Current length counter (buffer pointer)
080h-083h	Playback	32 bit	Channel 1 Base Address 0	Physical system memory address
084h-087h		32 bit	Channel 1 Base Address 1	Physical system memory address
088h-089h		16 bit	Channel 1 Segment Length 0	# of samples to fetch
08Ah-08Bh		16 bit	Channel 1 Segment Length 1	# of samples to fetch
08Ch-08Dh		16 bit	Channel 1 Command	Start/stop, reset control, status, data format (8/16, mono/stereo)
08Eh-08Fh		16 bit	Channel 1 Position	Current length counter (buffer pointer)
090h-093h	Playback	32 bit	Channel 2 Base Address 0	Physical system memory address
094h-097h		32 bit	Channel 2 Base Address 1	Physical system memory address
098h-099h		16 bit	Channel 2 Segment Length 0	# of samples to fetch
09Ah-09Bh		16 bit	Channel 2 Segment Length 1	# of samples to fetch
09Ch-09Dh		16 bit	Channel 2 Command	Start/stop, reset control, status, data format (8/16, mono/stereo)
09Eh-09Fh		16 bit	Channel 2 Position	Current length counter (buffer pointer)
0A0h-0A3h	Playback	32 bit	Channel 3 Base Address 0	Physical system memory address
0A4h-0A7h		32 bit	Channel 3 Base Address 1	Physical system memory address
0A8h-0A9h		16 bit	Channel 3 Segment Length 0	# of samples to fetch
0AAh-0ABh		16 bit	Channel 3 Segment Length 1	# of samples to fetch
0ACh-0ADh		16 bit	Channel 3 Command	Start/stop, reset control, status, data format (8/16, mono/stereo)
0AEh-0AFh		16 bit	Channel 3 Position	Current length counter (buffer pointer)

Playback Registers (Cont'd)

Host Offset	Mode	Size	Name	Description
0B0h-0B3h	Playback	32 bit	Channel 4 Base Address 0	Physical system memory address
0B4h-0B7h		32 bit	Channel 4 Base Address 1	Physical system memory address
0B8h-0B9h		16 bit	Channel 4 Segment Length 0	# of samples to fetch
0BAh-0BBh		16 bit	Channel 4 Segment Length 1	# of samples to fetch
0BCh-0BDh		16 bit	Channel 4 Command	Start/stop, reset control, status, data format (8/16, mono/stereo)
0BEh-0BFh		16 bit	Channel 4 Position	Current length counter (buffer pointer)
0C0h-0C3h	Playback	32 bit	Channel 5 Base Address 0	Physical system memory address
0C4h-0C7h		32 bit	Channel 5 Base Address 1	Physical system memory address
0C8h-0C9h		16 bit	Channel 5 Segment Length 0	# of samples to fetch
0CAh-0CBh		16 bit	Channel 5 Segment Length 1	# of samples to fetch
0CCh-0CDh		16 bit	Channel 5 Command	Start/stop, reset control, status, data format (8/16, mono/stereo)
0CEh-0CFh		16 bit	Channel 5 Position	Current length counter (buffer pointer)
0D0h-0D3h	Playback	32 bit	Channel 6 Base Address 0	Physical system memory address
0D4h-0D7h		32 bit	Channel 6 Base Address 1	Physical system memory address
0D8h-0D9h		16 bit	Channel 6 Segment Length 0	# of samples to fetch
0DAh-0DBh		16 bit	Channel 6 Segment Length 1	# of samples to fetch
0DCh-0DDh		16 bit	Channel 6 Command	Start/stop, reset control, status, data format (8/16, mono/stereo)
0DEh-0DFh		16 bit	Channel 6 Position	Current length counter (buffer pointer)
0E0h-0E3h	Playback	32 bit	Channel 7 Base Address 0	Physical system memory address
0E4h-0E7h		32 bit	Channel 7 Base Address 1	Physical system memory address
0E8h-0E9h		16 bit	Channel 7 Segment Length 0	# of samples to fetch
0EAh-0EBh		16 bit	Channel 7 Segment Length 1	# of samples to fetch
0ECh-0EDh		16 bit	Channel 7 Command	Start/stop, reset control, status, data format (8/16, mono/stereo)
0EEh-0EFh		16 bit	Channel 7 Position	Current length counter (buffer pointer)
0F4h-0F5h		16 bit	Channel 7 Interrupt Count	IRQ count: for modem operation as Overrun/Underrun count

7.5.1 PLAYBACK BASE ADDRESS 0 AND 1 - CHANNEL *N* (WHERE *N* = 0~7)

Host Offset: See table below for corresponding entry for ***n***

Bit	31	30	29	28	27	26	25	24
R/W	BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24
Initial	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
R/W	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16
Initial	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
R/W	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
BA[31:0]	Base Address	Host physical memory address of the channel buffer

Two 32-bit host physical base address registers. The *Base Address 0* register is used in both sequential and random access modes (See *Playback Channel Command Registers*). The *Base Address 0* register is used in sequential access mode.

PROGRAMMING NOTE:

These registers must be programmed with the *physical* address of a segment of the host buffer. In random mode, this address must be aligned on a 128KB boundary. In sequential mode, this address must be aligned on a DWORD boundary.

7.5.2 PLAYBACK SEGMENT LENGTH 0 AND 1 - CHANNEL *N* (WHERE *N* = 0~7)

Host Offset: See table below for corresponding entry for ***n***

Bit	15	14	13	12	11	10	9	8
R/W	SL15	SL14	SL13	SL12	SL11	SL10	SL9	SL8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
SL[15:0]	Segment Length	Length in bytes of the associated host buffer segment. Actual transfer is length +1.

Two 16-bit host buffer segment length registers. These registers specify the length in *bytes* of the physical memory segment pointed to by the corresponding *Playback Base Address 0* or *1* register.

PROGRAMMING NOTES:

1. Note that the actual number of bytes transferred is the programmed length +1. This allows true 64KB transfers with a 16-bit register.
2. Since this register allows a maximum of 64KB per segment, it may be necessary to break large host memory segments into smaller units.
3. In random mode, this register is typically programmed by the OTI-610/OTI-611 DSP.

7.5.3 PLAYBACK CHANNEL COMMAND - CHANNEL *N* (WHERE *N* = 0~7)

Host Offset: See table at beginning of this section for corresponding entry for ***n***

Bit	15	14	13	12	11	10	9	8
R/W	START	RFIFO	RANDOM	MONO	DO	DREADY	LS1	LS0
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	Segment Status	Reserved	Reserved	VDC4	VDC3	VDC2	VDC1	VDC0
Initial	-	-	-	0	0	0	0	0

Bit	Description	Comment
START	Enable Channel	1 - Enable bus master operation starting with base register set 0. 0 - Disable bus master operation
RFIFO	Reset FIFO	1 - Reset Data FIFO R/W pointers, start bit, valid data count 0 - Normal operation
RANDOM	Random Mode Select	1 - Random addressing mode 0 - Sequential addressing mode
MONO	MONO Enable	1 - Monophonic format data (1-channel) 0 - Stereophonic format data (2-channel)
DS	Data Size	1 - 8-bit samples 0 - 16-bit samples
DREADY	Data Ready	1 - FIFO contains valid data (used by OTI-610/OTI-611 DSP only)
LS1	Last Segment Flag 1	1 - Segment specified by base address 1 is the last segment 0 - Normal operation
LS0	Last Segment Flag 0	1 - Segment specified by base address 0 is the last segment 0 - Normal operation
VDC[1:0]	Valid Data Count	Number of valid samples in the FIFO. Range 0-16 (used by OTI-610/OTI-611 DSP only).
Segment Status	Current Segment	0 = Segment 0 1 = Segment 1

Setting the START bit will enable the bus master. If the channel FIFO is empty, the bus master will request the bus and memory transfer will begin. When the START bit is cleared, the bus master will stop after finishing the current bus cycle.

PROGRAMMING NOTE:

Setting the START bit *always* resets the hardware to base register 0. Pause/Resume and Set Position programming should take this behavior into account.

The random addressing mode (RANDOM bit set) uses base and length 0 registers only. In addition, the OTI-610/OTI-611 DSP expects the base register address to be modular 128K, and physically contiguous in memory. These restrictions force a maximum length of 64K WORDS in random mode.

The sequential addressing mode is designed to allow the host to implement scatter/gather control. The OTI-610/OTI-611 will automatically switch between the base address registers 0 and 1 when it reaches the end of the current register length. It will then send an interrupt to the host, whereupon the host may reload the used segment registers. When the last segment of a page table is encountered, the appropriate LSx bit (LS0 or LS1) must be set to indicate that the OTI-610/OTI-611 should stop fetching data at the end of that segment.

7.5.4 PLAYBACK SEGMENT POSITION - CHANNEL *N* (WHERE *N* = 0~7)

Host Offset: See table below for corresponding entry for ***n***

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Read	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8
Initial	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Read	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Initial	0	0	0	0	0	0	0	0

Bit	**Description**	**Comment**
SP[15:0]	Segment Position	Current byte position in active position

Specifies the offset in *bytes* of the next datum to be fetched by the OTI-610/OTI-611 bus master from the segment pointed to by the corresponding *Playback Base Address 0* or *1* register.

PROGRAMMING NOTE:

Host driver must keep track of active segment, based on the number of segment switch interrupts received. Remember that every time the START bit is set (*Playback Channel Command*), the OTI-610/OTI-611 starts from base address register 0.

7.5.5 PLAYBACK CHANNEL 7 INTERRUPT COUNT

Host Offset: 00F4h-00F5h

Bit	15	14	13	12	11	10	9	8
Read	IC15	IC14	IC13	IC12	IC11	IC10	IC9	IC8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Read	IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
IC[15:0]	Interrupt Count	Number of interrupts generated by playback channel 7 since the last time this register was read.

Counts the number of interrupts generated by the effects/modem playback channel. The register is reset every time it is read. This register is generally used as an overrun detector when the channel is used for modem operation.

Note that this register only exists for playback channel 7. Channels 0 through 6 do not support interrupt counting.

7.5.6 CAPTURE BASE ADDRESS - CHANNEL *N* (WHERE *N* = 8 OR 9)

Host Offset: See table on page 7-39 below for corresponding entry for ***n***

Bit	31	30	29	28	27	26	25	24
R/W	BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24
Initial	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
R/W	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16
Initial	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
R/W	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
BA[31:0]	Base Address	Host physical memory address of the channel buffer

The host physical base address register. The register is used in both sequential and random access modes (see *Capture Channel Command*).

PROGRAMMING NOTE:

These registers must be programmed with the **physical** address of a segment of the host buffer. In random mode, this address must be aligned on a 128KB boundary. In sequential mode, this address must be aligned on a DWORD boundary.

7.5.7 CAPTURE SEGMENT LENGTH - CHANNEL *N* (WHERE *N* = 8 OR 9)

Host Offset: See table on page 7-39 below for corresponding entry for ***n***

Bit	15	14	13	12	11	10	9	8
R/W	SL15	SL14	SL13	SL12	SL11	SL10	SL9	SL8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
R/W	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
SL[15:0]	Segment Length	Length in bytes of the associated host buffer segment. Actual transfer is length +1.

This register specifies the length in *bytes* of the physical memory segment pointed to by the *Capture Base Address* register. For random address mode (See *Capture Channel Command*), the range is 0 - 16, in WORD increments.

PROGRAMMING NOTES:

1. Note that the actual number of bytes transferred is the programmed length + 1. This allows true 64KB transfers with a 16-bit register.
2. In random mode, this register is typically programmed by the OTI-610/OTI-611 DSP.

3.5.8 CAPTURE CHANNEL COMMAND - CHANNEL *N* (WHERE *N* = 8 OR 9)

Host Offset: See table on page 7-39 below for corresponding entry for *n*

Bit	15	14	13	12	11	10	9	8
R/W	START	RFIFO	RANDOM	MONO	DS	FREADY	LS	Reserved
Initial	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	Reserved	Reserved	PAUSE	VDC4	VDC3	VDC2	VDC1	VDC0
VInitial	0	0	0	0	0	0	0	0

Bit	Description	Comment
START	Enable Channel	1 - Enable bus master operation starting with base register set 0 0 - Disable bus master operation
RFIFO	Reset FIFO	1 - Reset Data FIFO R/W pointers, start bit, valid data count 0 - Normal operation
RANDOM	Random Mode Select	1 - Random addressing mode 0 - Sequential addressing mode
MONO	MONO Enable	1 - Monophonic format data (1-channel) 0 - Stereophonic format data (2-channel)
DS	Data Size	1 - 8-bit samples 0 - 16-bit samples ready to accept
FREADY	FIFO Ready	1 - FIFO has valid data (used by OTI-610/OTI-611 DSP only)
LS	Last Segment Flag	1 - Segment specified by base address is the last segment 0 - Normal operation
PAUSE	Pause Flag	1 - Pause capture operation 0 - Normal operation
VD[4:0]	Valid Data Count	Number of valid samples in the FIFO. Range 0-16 (used by OTI-610/OTI-611 DSP only).

Setting the START bit will enable the bus master. If the channel FIFO is not empty, the bus master will request the bus and memory transfer will begin. When the START bit is cleared, the bus master will stop after finishing the current bus cycle.

PROGRAMMING NOTE:

Setting the START bit **always** resets the hardware to base register 0. Pause/Resume and Set Position programming should take this behavior into account.

In the random addressing mode (RANDOM bit set), the OTI-610/OTI-611 DSP expects the base register address to be modulo 128K, and physically contiguous in memory. These restrictions force a maximum length of 64K WORDS in random mode.

Unlike the playback channels, the capture channel sequential addressing mode uses a single base register to implement a *ping-pong* (double buffer) buffer scheme. The *Capture Segment Length* register should be set to half the host buffer size. The first time the segment length is reached, the OTI-610/OTI-611 sends an interrupt to the host, then reloads the *length counter only*. Host buffer writes continue with the next sequential address. When the segment length is reached for the second time, the host interrupt is sent, and the OTI-610/OTI-611 reloads *both the length counter and the base address* from the corresponding registers. This sequence repeats until the START bit is cleared or the appropriate LSx bit is encountered.

7.5.9 CAPTURE SEGMENT POSITION - CHANNEL *N* (WHERE *N* = 8 OR 9)

Host Offset: See table on page 7-39 below for corresponding entry for ***n***

Bit	15	14	13	12	11	10	9	8
Read	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Read	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
SP[15:0]	Segment Position	Current byte position in active position

Specifies the offset in bytes of the next datum to be written by the OTI-610/OTI-611 bus master to the segment pointed to by the Capture Base Address register.

7.5.10 CAPTURE INTERRUPT COUNT - CHANNEL 9

Host Offset: 003Ah-003Bh

Bit	15	14	13	12	11	10	9	8
Read	IC15	IC14	IC13	IC12	IC11	IC10	IC9	IC8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Read	IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
IC[15:0]	Interrupt Count	Number of interrupts generated by channel 9 (capture channel 1) since the last time this register was read.

Counts the number of interrupts generated by the effects/modem capture channel. The register is reset every time it is read. This register is generally used as an overrun detector when the channel is used for modem operation.

Note that this register only exists for capture channel 1. Capture channel 0 does not support interrupt counting.

7.6 GAME PORT REGISTERS

The registers' locations are linear and byte addresses are Game Port Configuration I/O Base Address + host offset.

Host Offset	Size	Description
00h-01h	8 bit	Standard Game Port
08h-09h	16 bit	Digital Mode Game Port I & II X Position
0Ah-0Bh	16 bit	Digital Mode Game Port I & II Y Position
0Ch	8 bit	Game Port Control
200h	8 bit	Standard Game Port
201h	8 bit	Standard Game Port (duplicate)

7.6.1 STANDARD GAME PORT

Host Offset: 0000h, 0001h, and 0200h, 0201h

Bit	7	6	5	4	3	2	1	0
R/W	PBB2	PBB1	PAB2	PAB1	PBY	PBX	PAY	PAX
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
PBB2	Port B Button 2	1 - Button pressed 0 - Button not pressed
PBB1	Port B Button 1	1 - Button pressed 0 - Button not pressed
PAB2	Port A Button 2	1 - Button pressed 0 - Button not pressed
PAB1	Port A Button 1	1 - Button pressed 0 - Button not pressed
PBY	Port B Y-axis	1 - Timer active 0 - Timer inactive
PBX	Port B X-axis	1 - Timer active 0 - Timer inactive
PAY	Port A Y-axis	1 - Timer active 0 - Timer inactive
PAX	Port A X-axis	1 - Timer active 0 - Timer inactive

This register implements the standard analog game port functions. It is accessible from either the standard game port I/O address of 200h/201h or the PCI offset address of 00h/01h.

A write to this port will generate a trigger pulse to the internal 558-like timer. A read from this port will get the current game port button and position status.

PROGRAMMING NOTE:

The standard game port addresses of 200h and 201h may be disabled using the SPEN bits in register 0Ch, Game Port Control. The Power On default condition disables the standard game port addresses.

7.6.2 DIGITAL MODE GAME PORT I & II X POSITION

Host Offset: 08h-09h

Bit	15	14	13	12	11	10	9	8
Read	Reserved	Reserved	Reserved	XA12	XA11	XA10	XA9	XA8
Initial	-	-	-	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Read	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
XA[12:0]	Game Port X-axis Position	

This register contains the current X-axis position of Digital Mode Game Port selected by the DGPSEL bit of the Game Port Control (0Ch) register.

Valid only if the POLLEN bit of the Game Port Control register is set.

7.6.3 DIGITAL MODE GAME PORT I & II Y POSITION

Host Offset: 0Ah-0Bh

Bit	15	14	13	12	11	10	9	8
Read	Reserved	Reserved	Reserved	YA12	YA11	YA10	YA9	YA8
Initial	-	-	-	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Read	YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
YA[12:0]	Game Port Y-axis Position	

This register contains the current Y-axis position of Digital Mode Game Port selected by the DGPSEL bit of the Game Port Control (0068h) register.

Valid only if the POLLEN bit of the Game Port Control register is set.

7.6.4 GAME PORT CONTROL

Host Offset: 0Ch

Bit	7	6	5	4	3	2	1	0
Read	POLLEN	SPEN	Reserved	DGPSEL	PBB2	PBB1	PBA2	PBA1
Write	POLLEN	SPEN	Reserved	DGPSEL	Reserved	Reserved	Reserved	Reserved
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
POLLEN	Hardware Poll Enable	1 - Enable hardware polling of analog game port 0 - Disable hardware polling of analog game port
SPEN	Standard Port Enable	1 - Enable standard game port response at 200h/201h
DGPSEL	Digital Mode Game Port Select	1 - Access Digital Mode Game Port II using *Game Port Position* registers 0 - Access Digital Mode Game Port I using *Game Port Position* registers
PBB2	Port B Button 2	1 Button pressed 0 - Button not pressed
PBB1	Port B Button 1	1 Button pressed 0 - Button not pressed
PAB2	Port A Button 2	1 Button pressed 0 - Button not pressed
PAB1	Port A Button 1	1 Button pressed 0 - Button not pressed

This register contains miscellaneous game port control functions for both the analog and digital game port implementations.

The POLLEN bit enables the OTI-611 auto-polling of the analog joystick position. The OTI-610/OTI-611 utilizes hardware counters to measure the trigger time period of each axis of the analog joystick in a manner similar to the method normally used by software joystick routines. This hardware polling relieves the software of the task of waiting for the joystick time-out, thus reducing the CPU load.

The DGPSEL bit is used to control which digital game port values are read when the Game Port I & II X Position and Game Port I & II Y Position registers are read.

7.7 OTI-611 FAX/MODEM I/O REGISTER DEFINITIONS

The registers' locations are linear and byte addresses are Modem Configuration I/O Base Address + host offset.

Host Offset	Size	Description
40h-41h	16 bit	Modem Data [15:0] Input and Output
42h	8 bit	Index Register Address [7:0]
43h	8 bit	Codec Index Register Address [7:0]
44h-45h	16 bit	Codec Data [15:0] Input and Output
46h	8 bit	ID
47h	8 bit	Modem I/O Space Control

7.7.1 MODEM DATA REGISTERS

Host Offset: 40h-41h

Bit	15	14	13	12	11	10	9	8
Read	IMD15	IMD14	IMD13	IMD12	IMD11	IMD10	IMD9	IMD8
Write	OMD15	OMD14	OMD13	OMD12	OMD11	OMD10	OMD9	OMD8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Read	IMD7	IMD6	IMD5	IMD4	IMD3	IMD2	IMD1	IMD0
Write	OMD7	OMD6	OMD5	OMD4	OMD3	OMD2	OMD1	OMD0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
IMD[15:0]	Incoming Modem Data	
OMD[15:0]	Outgoing Modem Data	

7.7.2 INDEX ADDRESS REGISTER

Host Offset: 42h

Bit	7	6	5	4	3	2	1	0
R/W	MINDX7	MINDX6	MINDX5	MINDX4	MINDX3	MINDX2	MINDX1	MINDX0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
MINDX[7:0]	Modem Index Register Address	

7.7.3 CODEC INDEX REGISTER

Host Offset: 43h

Bit	7	6	5	4	3	2	1	0
R/W	CMDBSY	DVS	CACC	CINDX4	CINDX3	CINDX2	CINDX1	CINDX0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
CINDX[4:0]	Codec Index Register Address	
CACC	Codec Access Type	1 = Write Access 0 = Read Access
DVS	Data Valid Status	1 = Current indexed register can be read
CMDBSY	Command Busy Status	1 = Current index address is not yet complete

This register is the same as register 6Ch in the audio function registers. This allows codec access from both configuration spaces.

7.7.4 CODEC DATA REGISTERS

Host Offset: 44h-45h

Bit	15	14	13	12	11	10	9	8
Read	ICD15	ICD14	ICD13	ICD12	ICD11	ICD10	ICD9	ICD8
Write	OCD15	OCD14	OCD13	OCD12	OCD11	OCD10	OCD9	OCD8
Initial	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Read	ICD7	ICD6	ICD5	ICD4	ICD3	ICD2	ICD1	ICD0
Write	OCD7	OCD6	OCD5	OCD4	OCD3	OCD2	OCD1	OCD0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
ICD[15:0]	Incoming Codec Data	
OCD[15:0]	Outgoing Codec Data	

These register is the same as register 6Ch-6Dh in the audio function registers. This allows codec access from both configuration spaces.

7.7.5 EXTERNAL OUTPUTS REGISTER

Host Offset: 46h

Bit	7	6	5	4	3	2	1	0
R/W	SPOUT0	ST7546	HDSTRLY	CODPWR	SPKRMT	CODRST	CID	OHRLY
Initial	0	0	0	0	0	1	1	1

Bit	Description	Comment
SPOUT[2:0]	Spare Output Pins	Software-controlled outputs
ST7546	ST7546 Mode Select	Controls CODEC_PIN on OTI-611. Connects to HC0 pin on ST7546 Modem Codec.
HDSTRLY	Headset (Voice) Relay Control	
CODPWR	Codec Power Down	
SPKRMT	Speaker Mute Control	
CODRST	Codec Reset	0 = Codec Reset
CID	Caller ID Relay Control	Active low
OHRLY	Off-Hook Relay Control	Active low

Default value = 0007

Same as Index 2 Extout[7:0] register.

7.7.6 MODEM I/O SPACE CONTROL

Host Offset: 47h

Bit	7	6	5	4	3	2	1	0
R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IOC1	IOC0
Initial	0	0	0	0	0	0	0	0

Bit	Description	Comment
IOC[1:0]	I/O Space Control	"00": Use PCI assigned I/O space only "10": Decode both PCI I/O space and COM3 space (3E8h-3EFh) "11": Decode both PCI I/O space and COM4 space (2E8h-2EFh)

CHAPTER 8

AC-LINK CHARACTERISTICS

8.1 AUDIO CODEC '97 COMPONENT SPECIFICATION OVERVIEW

The Audio Codec '97 Component Specification was created by Intel Corporation, National Semiconductor Corporation, Creative Laboratories, Inc., Yamaha Corporation, and Analog Devices, Inc., and was first published by Intel Corporation on May 17,1996.

Consult the Audio Codec '97 Component Specification for complete details on:

- AC-Link operation
- Register control and register bit definition of the AC '97 Codec
- AC-Link slot definitions

Throughout this chapter, the Audio Codec '97 Component Specification may also be referred to as "AC '97 Codec Specification," or simply as "AC '97." The codec device discussed in the Audio Codec '97 Component Specification may be referred to as "AC '97 Codec." The term AC-Link referenced in the Audio Codec '97 Component Specification may also be referred to as "AC-Link."

The Audio Codec '97 Component Specification defines the codec component of an audio or audio/ communications system, as well as the communications link between it and its companion digital controller.

The AC '97 digital controller and the AC '97 Codec together comprise the AC '97 System.

8.2 AC '97 AC-LINK DIGITAL SERIAL INTERFACE PROTOCOL

A 5-pin digital serial interface called AC-Link connects the OTI-610/OTI-611 to any AC '97 Codec. AC-Link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-Link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution, allowing support of 16-bit, 18-bit, and 20-bit samples within each data slot of the data stream.

The OTI-610 and OTI-611 support 16-bit samples and set the trailing 4 bits set to 0 within the AC '97 20-bit data slots.

Note: Throughout the rest of this chapter, AC-Link signal names will be given along with the equivalent OTI-610 and OTI-611 signal names. AC-Link signal names appearing in descriptive text will be printed in italics and will be enclosed within parentheses.

Tables containing signal names will show both the OTI-610/OTI-611 and AC-Link signal names in the same way.

Example:

OTI-610/OTI-611 Signal Name	**AC-Link Signal Name**
ARESET#	*(RESET#)*

Timing diagrams will be presented with the OTI-610/OTI-611 signal name in the illustration.

Synchronization of all AC-Link data transactions is signaled by the OTI-610 or OTI-611. The AC '97 Codec functions as a slave to the OTI-610 or OTI-611.

The AC '97 Codec drives a fixed 12.288-MHz serial bit clock, ASCLK *(BIT_CLK)* [derived from the AC '97 Codec crystal clock frequency source] onto AC-Link, which the OTI-610 or OTI-611 controller then qualifies with a synchronization signal, AFS *(SYNC)*, to construct audio frames.

AFS *(SYNC)*, fixed at 48 KHz, is derived by dividing down ASCLK *(BIT_CLK)*. ASCLK *(BIT_CLK)* provides the necessary clocking granularity to support twelve 20-bit outgoing and incoming time slots. AC-Link serial data is transitioned on each rising edge of ASCLK *(BIT_CLK)*.

The receiver of AC-Link data (the AC '97 Codec for outgoing data from the OTI-610/OTI-611 or the OTI-610/OTI-611 for incoming data from the AC '97 Codec), samples each serial bit on the falling edges of ASCLK *(BIT_CLK)*.

The AC-Link protocol provides for a special 16-bit (13 bits defined, with 3 reserved trailing bit positions) time slot (slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream and contains valid data. If a slot is "tagged" invalid, it is the responsibility of the source of the data (the AC '97 Codec for the input stream to the OTI-610/OTI-611 or the OTI-610 or OTI-611 for the output stream to the AC '97 Codec), to set all bit positions with 0s during that slot's active time.

AFS *(SYNC)* remains high for a total duration of 16 ASCLKs *(BIT_CLKs)* at the beginning of each audio frame. The portion of the audio frame where AFS *(SYNC)* is high is defined as the "Tag Phase." The remainder of the audio frame where AFS *(SYNC)* is low is defined as the "Data Phase."

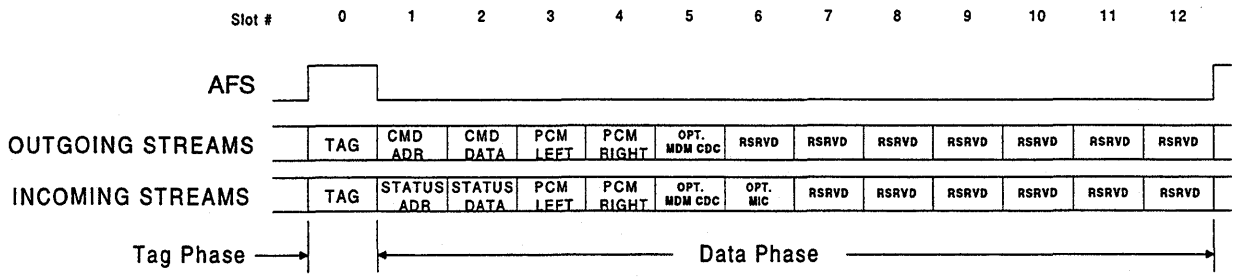


Figure 8-1: *AC '97 Standard Bi-directional Audio Frame*

The table below shows the data streams currently defined by the AC '97 Specification and the support provided by either the OTI-610 or the OTI-611. Slot directions are given relative to the OTI-610 or OTI-611 and should be reversed if referenced to the AC '97 Codec.

AC' 97 Data Stream	Slots/Slot #	Support		
		OTI-610	OTI-611	Notes
Control Control Register Write Port	2 output Slot 1,2	Yes	Yes	1
Status Status Register Read Port	2 input Slot 1,2	Yes	Yes	1
PCM Playback Data 2-channel composite PCM output stream (L/R)	2 output Slot 3L, 4R	Yes	Yes	1
PCM Record Data 2-channel composite PCM input stream (L/R)	2 input Slot 3L, 4R	Yes	Yes	1
Optional Modem Line Codec Output Stream Modem line Codec DAC output stream to OTI-612 or AC '97 Codec	1 output Slot 5	Filled with 0s	Yes	2
Optional Modem Line Codec Input Stream Modem line Codec DAC input stream to OTI-612 or AC '97 Codec	1 input Slot 5	Filled with 0s	Yes	2
Optional Dedicated Microphone Input Microphone input stream in support of Acoustic Echo Cancellations and/or other voice applications	1 input Slot 6	Filled with 0s	No Filled with 0s	3
RESERVED - Undefined. Filled with 0s by OTI-610/OTI-611	6 output Slot 6-12	Filled with 0s	Filled with 0s	
RESERVED - undefined Filled with 0s by OTI-612 or AC '97 Codec	5 input Slot 7-12	Filled with 0s	Filled with 0s	

Notes (from the AC '97 Specification):

1. AC '97 controller/AC '97 Codec pair interoperability can only be guaranteed for non-optional AC '97 audio features.
2. Modem interoperability is not expected between AC '97 controller/AC '97 Codec pairs that aren't sourced as a matched set by the same vendor. Given this, each vendor's AC '97 controller implicitly knows what the modem DAC/ADC resolution are in the AC '97 Codec version w/ modem support by inspecting the vendor ID registers.
3. An audio component vendor who develops an AC '97 Codec with optional dedicated microphone channel support should also offer an AC '97 controller to fully support this feature with a matched set solution.

Software Driver Support and AC '97 Controller/AC '97 Interoperability

The software driver written for the OTI-610/OTI-611 is responsible for exposing and managing the AC '97 Codec analog features. Interoperability requires that every AC '97 controller and AC '97 driver support the basic AC '97 Codec features.

Mono PCM output always translates in the AC '97 controller to two mono channels (L and R) on the AC-Link.

The following optional AC '97 features should also be supported by all AC '97 controller drivers when determined to be present:

- Tone control
- Loudness
- Simulated stereo
- 3D stereo enhancement
- Headphone out

Other features may not make sense to support unless there is also support in the AC '97 controller. In these cases, interoperability may be limited to an AC '97 controller/AC '97 analog pair sourced by the same vendor:

- Modem ADC and DAC
- Third ADC input channel
- Vendor-specific features

8.3 OTI-610/OTI-611 IN THE AC '97 SYSTEM

The OTI-610 and OTI-611 support the AC-Link, which is defined in the Audio Codec '97 Component Specification, as a peer-to-peer communications link between a digital audio controller and an Audio Codec, or as a digital audio/communications controller and a dual audio/modem codec.

The OTI-610 and OTI-611 support multiple codec types, including the AC '97 type. The OTI-610 or OTI-611 therefore can function as the "AC '97 Digital Controller" referred to in the Audio Codec '97 Component Specification.

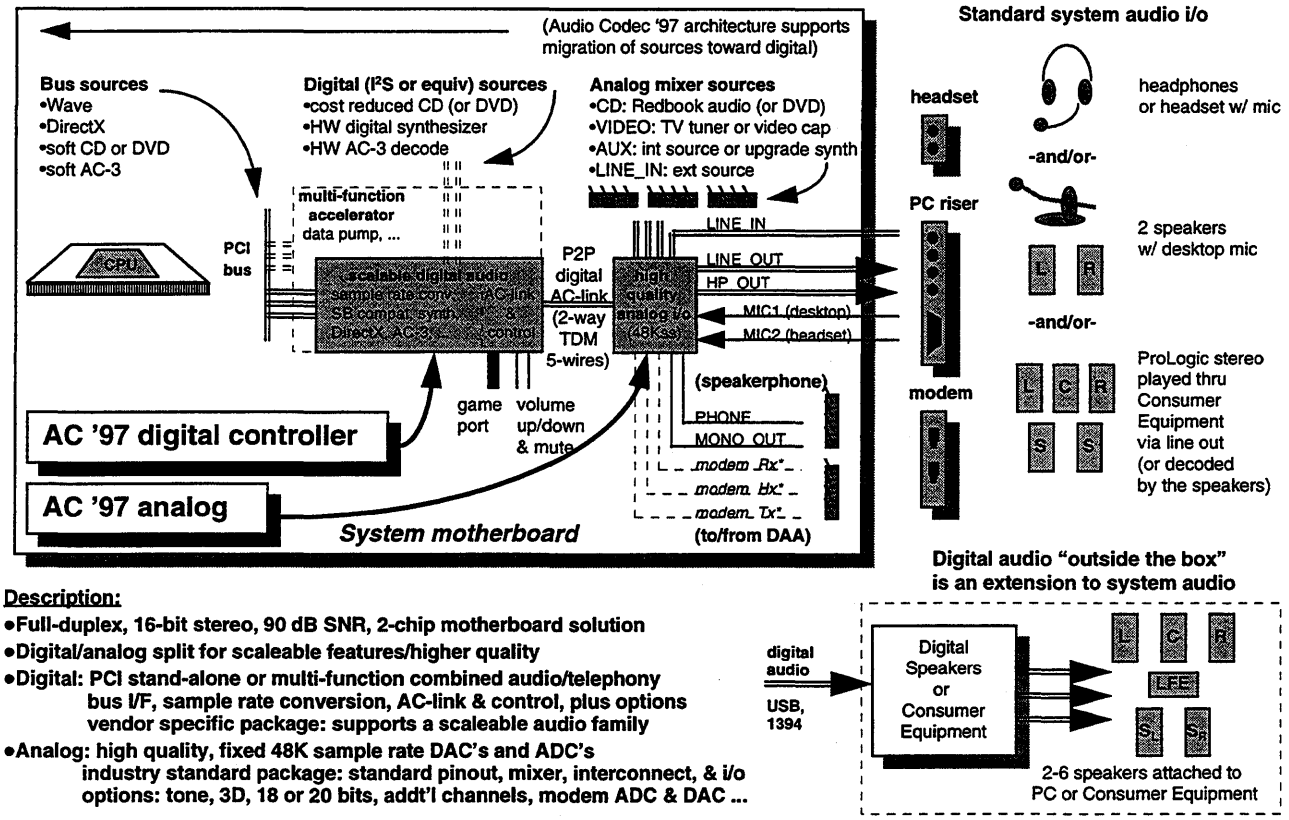
The OTI-610 supports multiple codecs. If the codec type selected is AC '97, then the OTI-610 functions as an audio-only AC '97 digital controller, and would be typically used in an AC '97 system with an audio-only AC '97 Codec.

The OTI-611 supports multiple codecs. If the codec type selected is AC '97, then the OTI-611 functions as an audio and communications AC '97 digital controller and would be typically used in an AC '97 system with the OTI-612 dual audio and communications AC '97 compliant Codec, or any dual audio and communications AC '97 Codec supporting modem outgoing and incoming 16-bit data in time slot 5.

See Chapter 3 for more details on codecs supported by the OTI-610 and OTI-611.

8.4 AC '97 SYSTEM IMPLEMENTATION

The AC '97 System Diagram in Figure 8-2 and the immediately following text is reproduced directly from the AC '97 Codec Specification.



Description:

- **Full-duplex, 16-bit stereo, 90 dB SNR, 2-chip motherboard solution**
- **Digital/analog split for scaleable features/higher quality**
- **Digital: PCI stand-alone or multi-function combined audio/telephony bus I/F, sample rate conversion, AC-link & control, plus options vendor specific package: supports a scaleable audio family**
- **Analog: high quality, fixed 48K sample rate DAC's and ADC's industry standard package: standard pinout, mixer, interconnect, & i/o options: tone, 3D, 18 or 20 bits, addt'l channels, modem ADC & DAC ...**

Figure 8-2: *AC '97 System Diagram*

Figure 8-2 "...shows the essential features of an AC '97 audio design. The AC '97 analog component performs fixed 48K sample rate DAC & ADC conversions, mixing, and analog processing (tone, 3D stereo enhancement, etc.). It always functions as a slave to an AC '97 digital controller which must be implemented in the digital portion of any AC '97 audio system."

"The AC '97 controller, primarily targeted for PCI, can be as simple as a stand-alone design which supports high quality sample rate conversions to/from 48Kss, Sound Blaster compatibility, FM and/or wavetable synthesis, with optional DirectSound* acceleration, AC-3 decode, etc. The AC '97 controller may also be embedded within a PCI multifunction accelerator, offering higher levels of integration by combining audio with telephony or graphics. However, nothing precludes ISA, USB, or 1394 designs based on the AC '97 architecture."*

"The digital link, "AC-link", connecting the AC `97 controller to the AC `97 analog component is a bi-directional, 5-wire, serial TDM format interface, designed for dedicated point to point interconnect on a circuit board."

"The diagram shows the most common (high attach rate) connections, some digital and some analog. PC audio today requires that a number of analog sources be supported in the analog mixer. Over time, it will become attractive from both cost and functionality perspectives to move these sources toward dedicated digital connections or onto the bus[2]. The AC '97 architecture facilitates this migration."

"The AC '97 architecture is designed primarily to support stereo 2-speaker PC audio. However, two multi-channel extensions are shown in the system diagram, one utilizing the AC '97 architecture and one independent of it:"

- *"Multi-channel encoded stereo (such as Dolby* ProLogic*) can be played out through the 2-channel AC '97 audio subsystem. This type of signal can be played on normal stereo speakers, decoded into 4 channels by the speakers, or sent to consumer equipment via a stereo analog line out connection."*
- *"True 2/4/6 channel digital audio output (such as 5.1 channel Dolby AC-3*) can bypass the 2-channel AC '97 audio subsystem and be transmitted via a digital link (such as USB or 1394) to digital speakers or digital ready consumer equipment which drives a multi-speaker arrangement such as the home theater[3]."*

Note: The support for dedicated digital connections requires frequency locking and sample rate conversion capabilities in the AC '97 controller in order to reconcile independent time bases, the digital source, and AC '97's fixed 48Kss.

There are many PC audio sources that are not currently bus independent, such as DOS games, H/W accelerated Windows 95 games, CD Redbook audio, and DVD-ROM movies w/HW AC-3 decode. In order to hear ALL PC audio sources through one set of digitally connected speakers, backwards compatibility must be addressed.

8.5 OTI-610/OTI-611 CONNECTION TO THE AC '97 CODEC

The OTI-610 or OTI-611 communicates with the OTI-612 AC '97 compatible dual audio and communications codec (or any other AC '97 compatible audio codec, or dual audio and communications codec) via a digital serial link called AC-Link. AC-Link is a 5-pin, bi-directional, fixed data rate, serial PCM digital stream. It handles multiple input and output audio streams, as well as control register accesses to the AC '97 Codec device employing a time division multiplexed (TDM) scheme. The AC-Link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution.

All digital audio streams, optional modem line codec streams, and command/status information are communicated over this point-to-point serial interconnect interface.

See Chapter 3 for specific details on physical connections between the OTI-610 and OTI-611 and the various types of AC '97 Codec packages.

A breakout of the signals connecting the OTI-610/OTI-611 to an AC '97 Codec is shown in the following table and figure.

OTI-610/OTI-611 Signal Name	Type	OTI-612 or AC '97 Codec Signal Name-AC-Link Signal Name	Type	Description
ARESET#	O	RESET#	I	Master H/W Reset to AC '97 Codec from OTI-610 or OTI-611
AFS	O	SYNC	I	48-KHz fixed rate sample sync from OTI-610 or OTI-611
ASCLK	I	BIT_CLK	O	12.288-MHz serial data clock (Fx/2 from AC '97 Codec) to OTI-610 or OTI-611. Fx=24.576 MHz
ASDO	O	SDATA_OUT	I	Serial, time division multiplexed output stream to AC '97 Codec from OTI-610 or OTI-611
ASDI	I	SDATA_IN	O	Serial, time division multiplexed output stream from AC '97 Codec to OTI-610 or OTI-611

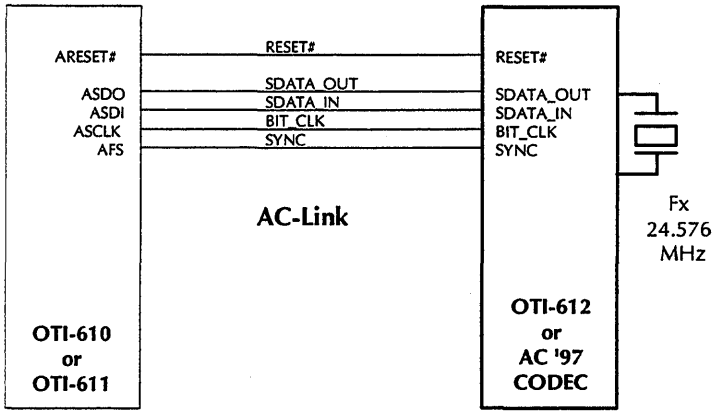


Figure 8-3: *AC-Link Connection to AC '97 Compatible Codec*

8.6 RESETTING THE AC '97 CODEC

The AC '97 Codec Specification provides for three types of AC '97 Codec reset:

1. a *Cold AC '97 Reset* where all AC '97 Codec logic (registers included) is initialized to its default state
2. a *Warm AC '97 Reset* where the contents of the AC '97 Codec register set are left unaltered
3. a *Register Reset,* which only initializes the AC '97 Codec registers to their default states

The current Power Down state would ultimately dictate which form of AC '97 reset is appropriate.

Unless a "cold" or "register" reset (a write to the Reset register) is performed, wherein the AC '97 Codec registers are initialized to their default values, the AC '97 Codec registers are required to keep state during all Power Down modes.

After signaling a reset to AC '97 Codec, the OTI-610/OTI-611 will not attempt to play or capture audio data until it has sampled a "Codec Ready" indication from the AC '97 Codec.

8.6.1 COLD AC '97 RESET

A Cold Reset activates AC-Link as well as resets the AC '97 Codec.

A Cold Reset of the AC '97 Codec is achieved by the OTI-610/OTI-611 driver asserting ARESET# *(RESET#)* low for the minimum specified time, or by the OTI-610/OTI-611 asserting ARESET# *(RESET#)* low for the minimum specified time during its Power On sequence.

By driving ARESET# *(RESET#)* low ASCLK *(BIT_CLK),* and ASDO *(SDATA_OUT)* will be activated, or re-activated as the case may be, by the AC '97 Codec. All AC '97 Codec control registers will be initialized to their default Power On reset values.

ARESET# *(RESET#)* is an asynchronous input to the AC '97 Codec.

8.6.2 WARM AC '97 CODEC RESET

A warm AC '97 Codec reset will re-activate the AC-Link without altering the current AC '97 Codec register values.

A Warm Reset is signaled by the OTI-610/OTI-611 driver setting AFS *(SYNC)* high for a minimum of 1uS in the absence of ASCLK *(BIT_CLK)*.

Within normal audio frames, AFS *(SYNC)* is a synchronous AC '97 Codec input. However, in the absence of ASCLK *(BIT_CLK)*, AFS *(SYNC)* is treated as an asynchronous input used in the generation of a warm reset to the AC '97 Codec.

The AC '97 Codec will not respond with the activation of ASCLK *(BIT_CLK)* until AFS *(SYNC)* has been driven low by the OTI-610/OTI-611 and has been sampled low again by the AC '97 Codec. This prevents the false detection of a new audio frame.

8.6.3 REGISTER RESET OF AC '97 CODEC

A register reset of the AC '97 Codec is achieved by writing any value to the AC '97 Codec Reset register (Index 00h), which causes all registers to revert to their default values.

8.7 AC-LINK LOW POWER MODE

The AC-Link signals can be placed in a low-power mode. When the AC '97 Codec General Purpose register (20h) is programmed to the appropriate value, both AC-Link signals, ASCLK *(BIT_CLK)* and ASDI *(SDATA_IN)*, will be brought to and held at a logic low-voltage level.

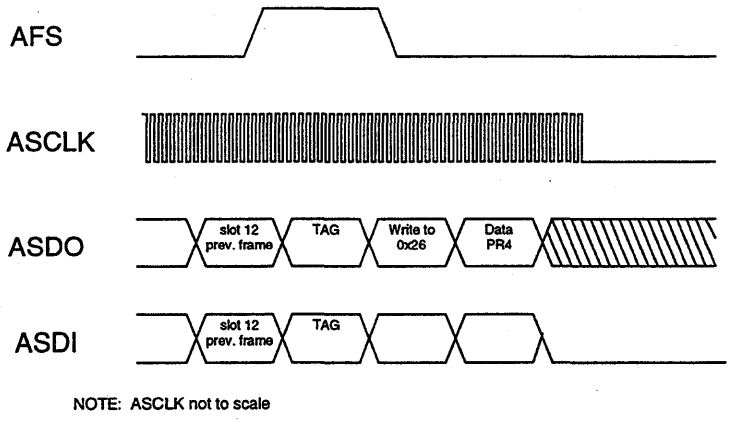


Figure 8-4: *AC-Link Power Down Operation*

ASCLK *(BIT_CLK)* and ASDI *(SDATA_IN)* from the AC '97 Codec to the OTI-610/OTI-611 are transitioned low immediately (within the maximum specified time) following the decode of the write to the General Purpose register (26h) with PR4. When the OTI-610/OTI-611 driver is ready to program the AC-Link into its low-power mode, slots 1 and 2 **are assumed to be** the only valid stream in the audio output frame. At this point in time it is assumed that all sources of audio input have also been neutralized.

The OTI-610/OTI-611 driver should also drive the OTI-610/OTI-611 AC-Link signals, AFS *(SYNC)* and ASDO *(SDATA_OUT)*, low after programming AC '97 to this low-power, "halted" mode.

8.7.1 WAKING UP AC-LINK

Once the AC '97 Codec has been instructed to halt BIT_CLK, a special "wake up" protocol must be used to bring the AC-Link to the active mode since normal audio output and input frames cannot be communicated in the absence of BIT_CLK.

There are two methods for bringing the AC-Link out of a low power, halted mode: Cold AC '97 Reset and Warm AC '97 Reset. The current Power Down state would ultimately dictate which form of AC '97 reset is appropriate. Regardless of the method used, the OTI-610/OTI-611 will perform the wake-up task.

Once powered down, re-activation of the AC-Link via re-assertion of the AFS *(SYNC)* signal (Warm AC '97 Reset method) must not occur for a minimum of four audio frame times following the frame in which the Power Down was triggered. When AC-Link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

8.7.2 EXAMPLES OF AC-LINK POWER DOWN OPERATIONS

The following illustrations and text are taken directly from the Audio Codec '97 Component Specification.

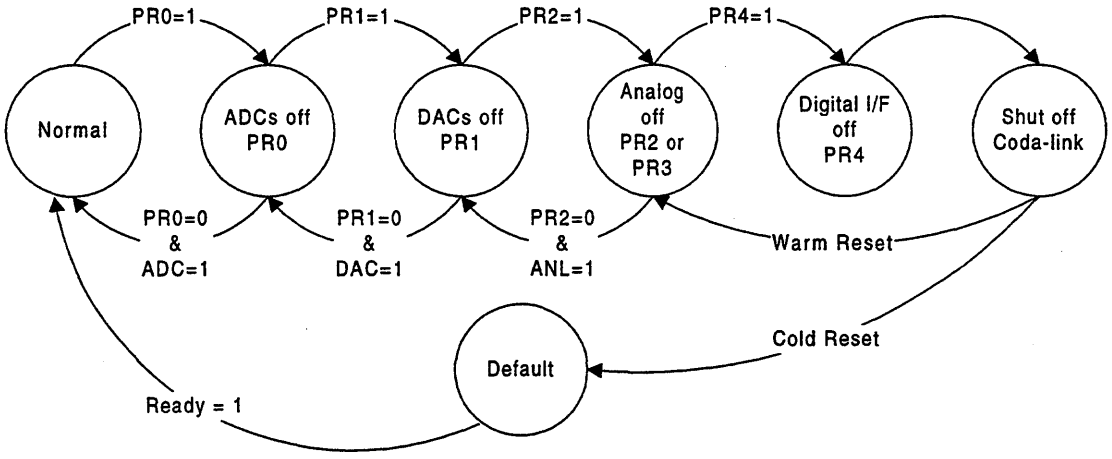


Figure 8-5: *One Example of AC '97 Power Down & Power Up Flow*

The above figure illustrates one example procedure to do a complete power down of AC '97. From normal operation, sequential writes to the General Purpose Register are performed to power down AC '97 a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC '97's digital interface (AC-Link). The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC '97 controller will send pulse on the sync line issuing a warm reset. This will restart AC '97's digital interface (resetting PR4 to zero). AC '97 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers as a cold reset will set them to their default states. When a section is powered back on the Power Down Control/Status register (index 26h) should be read to verify that the section is ready (i.e., stable) before attempting any operation that requires it.

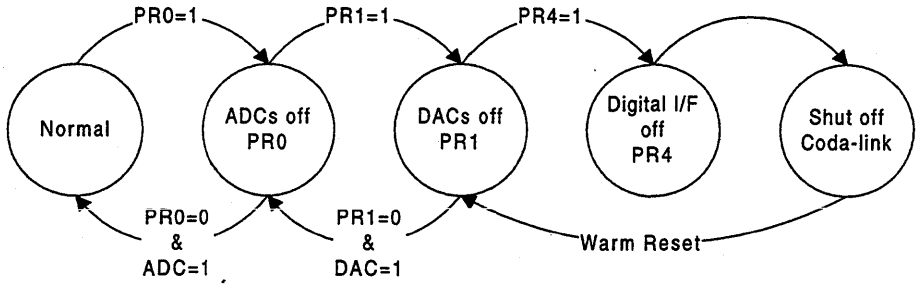


Figure 8-6: *AC '97 Power Down & Power Up Flow with Analog Still Alive*

The above figure illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINE_IN source) through AC '97 to the speakers but have most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

8.8 TESTABILITY

The AC '97 Specification lists two test modes. One is for ATE in-circuit tests and the other is optional for vendor-specific tests. Regardless of the test mode, the OTI-610/OTI-611 must issue a "cold" reset to resume normal operation of the AC '97 Codec.

All AC-Link signals are normally low through the trailing edge of ARESET# *(RESET#)*.

When the AC '97 Codec is placed in the ATE in-circuit test mode, its digital AC-Link outputs (i.e., BIT_CLK and SDATA_IN) are driven to a high-impedance state. This allows ATE in-circuit testing of the OTI-610/OTI-611 digital controller.

The AC '97 Codec enters the ATE in-circuit test mode when the OTI-610/OTI-611 drives ASDO *(SDATA_OUT)* high at the trailing edge of ARESET# *(RESET#)* and the AC '97 Codec samples ASDO *(SDATA_OUT)* as high at the trailing edge of ARESET# *(RESET#)*.

8.9 AC-LINK DC AND AC CHARACTERISTICS

The AC '97 Specification recommends that the digital AC-Link interface portion of the AC '97 Codec component be capable of operating at either 5V or 3.3V, depending on which DVdd is supplied to it. The AC '97 Specification lists DVdd for the AC '97 Codec at DVdd = 5V or DVdd = 3.3V, or alternatively, DVdd=5V or DVdd=3V (recommended). Consult the Audio Codec '97 Component Specification for complete details on the AC '97 Codec DC characteristics.

The AC '97 Specification also states that when designed into an AC '97 system, the AC '97 digital controller and AC '97 Codec should always run off the same DVdd voltage level.

The OTI-610 and OTI-611 digital controllers operate only at Vdd = +5VDC. Therefore, when interfaced to an AC '97 Codec, the AC '97 Codec DVdd must also operate at +5VDC.

8.9.1 DC CHARACTERISTICS

The table below represents the DC characteristics of the OTI-610 and OTI-611 for AC-Link signals ARESET# *(RESET#)*, AFS *(SYNC)*, ASCLK *(BIT_CLK)*, ASDI *(SDATA_IN)*, and ASDO *(SDATA_OUT)*.

Parameter	Symbol	Min	Type	Max	Units
Input Voltage Range	V_{in}	-0.30	-	DVdd + 0.30	V
Low Level Input Voltage	V_{il}	-	-	0.30 x Vdd	V
High Level Input Voltage	V_{ih}	0.40 x Vdd	-	-	V
High Level Output Voltage	V_{oh}	0.50 x Vdd	-	-	V
Low Level Output Voltage	V_{ol}	-	-	0.20 x Vdd	V
Input Leakage Current (RESET#, SYNC, SDATA_OUT, AC-Link Inputs)	-	-10	-	10	uA
Input Leakage Current (BIT_CLK, SDATA_IN, AC-Link Outputs)	-	-10	-	10	uA
Output Buffer Drive Current	-	-	5	-	mA

Note: $T_{ambient}$ = 25°C, AVdd = Vdd = 5VDC; AVss = Vss = 0V; 50pF external load)

8.9.2 AC TIMING CHARACTERISTICS

$T_{ambient}$ = 25°C, AVdd = Vdd = 5VDC; AVss = Vss = 0V; 50pF external load)

8.9.3 RESET

Cold Reset

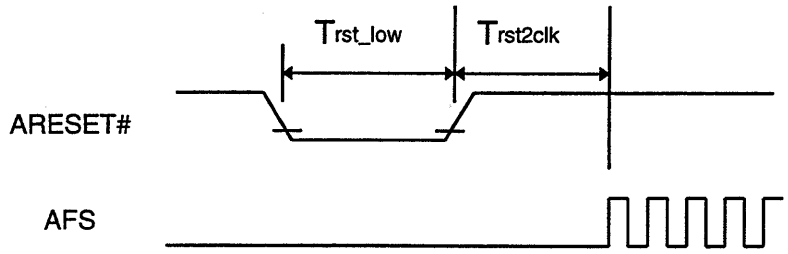


Figure 8-7: *Cold AC '97 Reset Timing*

Parameter	Symbol	Min	Type	Max	Units
ARESET *(RESET#)* active low pulse width	T_{rst_low}	1.0	-	-	uS
ARESET *(RESET#)* inactive to ASCLK *(BIT_CLK)* startup delay	$T_{rst2clk}$	162.8	-	-	nS

Warm Reset

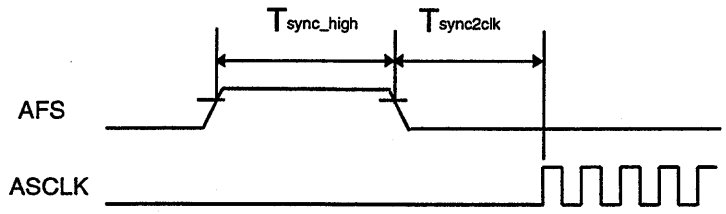


Figure 8-8: *Warm AC '97 Reset Timing*

Parameter	Symbol	Min	Type	Max	Units
AFS *(SYNC)* active high pulse width	T_{sync_high}	-	1.3	-	uS
AFS *(SYNC)* inactive to ASCLK *(BIT_CLK)* startup delay	$T_{sync2clk}$	162.8	-	-	nS

8.10 CLOCKS

(50pF external load)

Parameter	Symbol	Min	Type	Max	Units
ASCLK *(BIT_CLK)* frequency		-	12.288	-	MHz
ASCLK *(BIT_CLK)* period	T_{clk_period}	-	81.4	-	nS
ASCLK *(BIT_CLK)* output jitter		-	-	750	pS
ASCLK *(BIT_CLK)* high pulse width (note 1)	T_{clk_high}	32.56	40.7	48.84	nS
ASCLK *(BIT_CLK)* low pulse width (note 1)	T_{clk_low}	32.56	40.7	48.84	nS
AFS *(SYNC)* frequency		-	48.0	-	KHz
AFS *(SYNC)* period	T_{sync_period}	-	20.8	-	uS
AFS *(SYNC)* high pulse width	T_{sync_high}	-	1.3	-	uS
AFS *(SYNC)* low pulse width	T_{sync_low}	-	19.5	-	uS

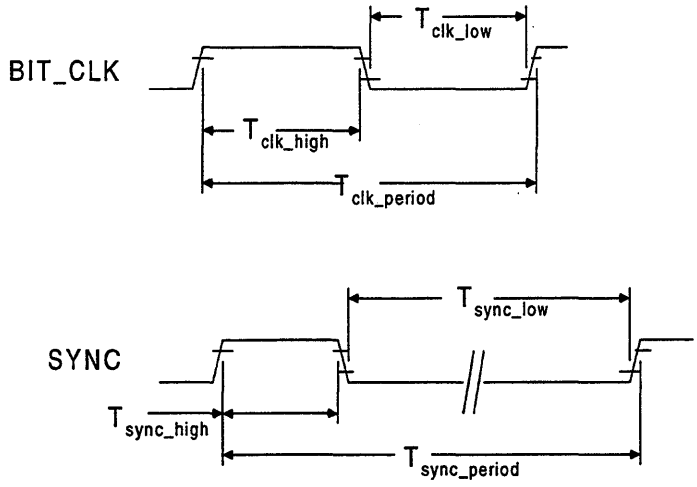


Figure 8-9: *Clock Timing*

8.11 DATA SETUP AND HOLD

(50pF external load)

Parameter	Symbol	Min	Type	Max	Units
Setup to falling edge of ASCLK *(BIT_CLK)*	T_{setup}	15.0	-	-	nS
Hold from falling edge of ASCLK *(BIT_CLK)*	T_{hold}	5.0	-	-	nS

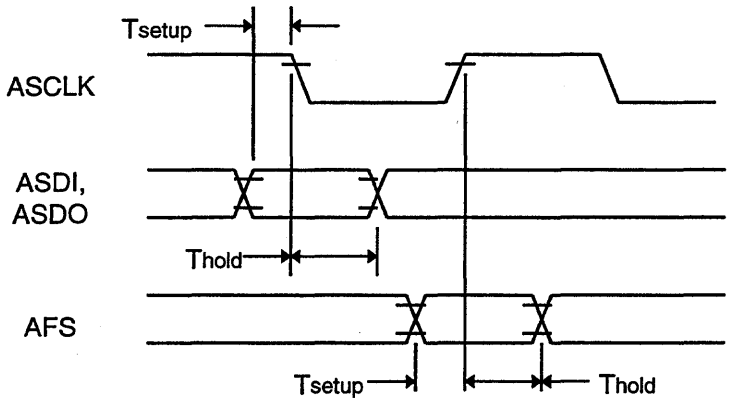


Figure 8-10: *Data Setup and Hold Timing*

8.12 SIGNAL RISE AND FALL TIMES

(50pF external load)

Parameter	Symbol	Min	Type	Max	Units
ASCLK *(BIT_CLK)* rise time	$Trise_{clk}$	2	-	-	nS
ASCLK *(BIT_CLK)* fall time	$Tfall_{clk}$	2	-	-	nS
AFS *(SYNC)* rise time	$Trise_{sync}$	2	-	-	nS
AFS *(SYNC)* fall time	$Tfall_{sync}$	2	-	-	nS
ASDI *(SDATA_IN)* rise time	$Trise_{din}$	2	-	-	nS
ASDI *(SDATA_OUT)* fall time	$Tfall_{din}$	2	-	-	nS
ASDO *(SDATA_OUT)* rise time	$Trise_{dout}$	2	-	-	nS
ASDO *(SDATA_OUT)* fall time	$Tfall_{dout}$	2	-	-	nS

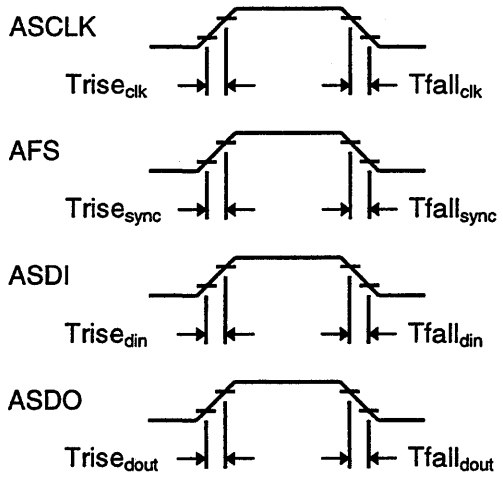


Figure 8-11: *AC '97 Signals Rise and Fall Times*

8.13 AC-LINK LOW-POWER MODE TIMING

Parameter	Symbol	Min	Type	Max	Units
End of Slot 2 to ASCLK *(BIT_CLK)*, ASDI *(SDATA_IN)* low	T_{s2_pdown}	-	-	1.0	uS

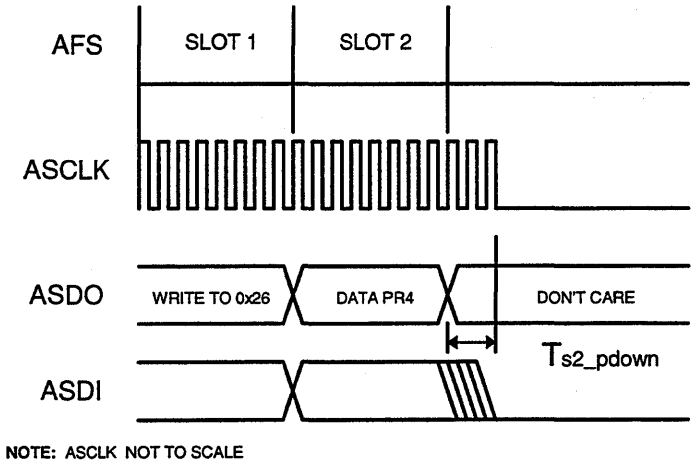


Figure 8-12: *AC-Link Low-Power Mode Timing*

8.14 ATE IN-CIRCUIT TEST MODE TIMING

Parameter	Symbol	Min	Type	Max	Units
Setup to trailing edge of ARESET# *(RESET#)*	$T_{setup2rst}$	15.0	-	-	nS
Rising edge of ARESET# *(RESET#)* to Hi-Z delay	T_{off}	-	-	25.0	nS

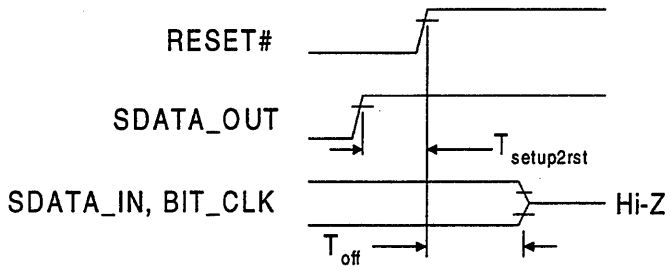


Figure 8-13: *ATE In-Circuit Test Mode Timing*

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CHAPTER 9

ELECTRICAL CHARACTERISTICS

9.1 ABSOLUTE MAXIMUM RATINGS

The values listed below are stress ratings only. Functional operation at the maximum ratings is not recommended or guaranteed. The device's reliability is affected if the device is operated for extended periods at maximum ratings.

Electrostatic discharge damage may result from high static voltages or electric fields.

Symbol	Parameter	Min.	Max.	Unit
AV_{DD}	Analog Power Supply	-0.3	7.0	V
DV_{DD}	Digital Power Supply	-0.3	7.0	V
V_{IA}	Analog Input Voltage	-0.3	7.0	V
V_{ID}	Digital Input Voltage	-0.3	7.0	V
V_{ESD}	ESD Tolerance (Human Body Model per Method 3015.2 of MIL-STD-883B)		2	KV
T_{OPER}	Operating Temperature	0	+70	°C
T_{STG}	Storage Temperature	-65	+150	°C
P_{DMAX}	Maximum Power Dissipation at T_J = 125°C		1800	mW

9.2 DC SPECIFICATIONS

Unless otherwise noted, electrical characteristics of the OTI-610/OTI-611 are specified over the operation range.

Typical values for :

VDD = AVDD = +5VDC ± 5%
VSS = AVSS = 0VDC

The table below lists the DC specifications of the OTI-610 and OTI-611, except for five signals specifically used as the AC-Link connection to AC '97 Codecs.

DC Specifications (except AC-Link Signals):

Symbol	Parameter	Min.	Max.	Unit	Condition	Notes
V_{oh}	Output High Voltage	2.4		V	I_{oh} = 400 uA	
V_{ol}	Output Low Voltage		0.4	V	I_{ol} = 18 mA	TxD pin
V_{ol}	Output Low Voltage		0.4	V	I_{ol} = 4 mA	All other output pins except PCI types
V_{ol}	Output Low Voltage		0.4	V	I_{ol} = 2 mA	PCI Interface pins
V_{ih}	Input High Voltage	2.0	DV_{dd} +0.5	V	TTL	
V_{il}	Input Low Voltage	-0.5	0.8	V	TTL	
V_{is}	Schmidt Input Voltage	2.4	DV_{dd} +0.5	V	Schmidt	
V_{ic}	CMOS Input Voltage	3.8	DV_{dd} +0.5	V	CMOS	
I_{LI}	Input Leakage Current	-10	10	uA		
O_{LI}	Output Leakage Current	-10	10	uA		
I_{CC}	Operating Supply Current		245 270	mA mA	DV_{dd} = 5V DV_{dd} = 5.25V	
I_{CC-PD}	Operating Supply Current Power Down Mode		33	mA		
I_{avdd}	AV_{dd} Current		500	uA	AV_{dd} = 5V	
C_I	Input Capacitance		8	pF		
C_O	Output Capacitance		8	pF		
C_{IO}	I/O Capacitance		8	pF		

Note: TA = 0°C to 70°C; VDD = AVDD = 5V +/1 5%; VSS = AVSS = 0V
For complete details, consult Chapter 6.

AC-Link Signal List:

OTI-610/OTI-611 Signal Name	Type	OTI-612 or AC '97 Codec Signal Name- AC-Link Signal Name	Type	Description
ARESET#	O	RESET#	I	Master H/W Reset to AC '97 Codec from OTI-610 or OTI-611
AFS	O	SYNC	I	48-KHz fixed rate sample sync from OTI-610 or OTI-611
ASCLK	I	BIT_CLK	O	12.288-MHz serial data clock (Fx/2 from AC '97 Codec) to OTI-610 or OTI-611. Fx=24.576 MHz
ASDO	O	SDATA_OUT	I	Serial, time division multiplexed output stream to AC '97 Codec from OTI-610 or OTI-611
ASDI	I	SDATA_IN	O	Serial, time division multiplexed output stream from AC '97 Codec to OTI-610 or OTI-611

Data from the table below applies to the following OTI-610/OTI-611 signals when used as an AC-Link connection to the OTI-612 or an AC '97 compatible codec in an AC '97 system design.

AC-Link Signals DC Characteristics:

Symbol	Parameter	Min.	Max.	Units	Condition	Notes
V_{IN}	Input Voltage Range	-0.30	5.3	V		
V_{IL}	Low Level Input Voltage	-	0.8	V		
V_{IH}	High Level Input Voltage	2.0	-	V		
V_{OH}	High Level Output Voltage	2.4	-	V		
V_{OL}	Low Level Output Voltage	-	0.55	V	I_{OL} = 5.0 mA	Typ
-	Input Leakage Current (AC-Link inputs)	-10	10	uA		
-	Output Leakage Current (Hi-Z'd AC-Link outputs)	-10	10	uA		

Note: TA = 0°C to 70°C; VDD = AVDD = 5V +/1 5%; VSS = AVSS = 0V

9.3 AC SPECIFICATIONS

Unless otherwise noted, electrical characteristics are specified over the operation range.

Typical value for VDD = AVDD = +5VDC ± 5%, VSS = AVSS = 0VDC

AC specifications for AC-Link signals when used in an AC '97 system are given in Chapter 8 and in Section 9.4.

9.3.1 RESET TIMING

Symbol	Parameter	Min.	Typ	Max	Units	Notes
$t_{RESET\# L}$	RST# Low Time	1			LCLK	
t_{WDMV}	WDM Valid Time from RST# Rising Edge		32		nS	
t_{WDMVH}	WDM Valid Hold Time	5			nS	

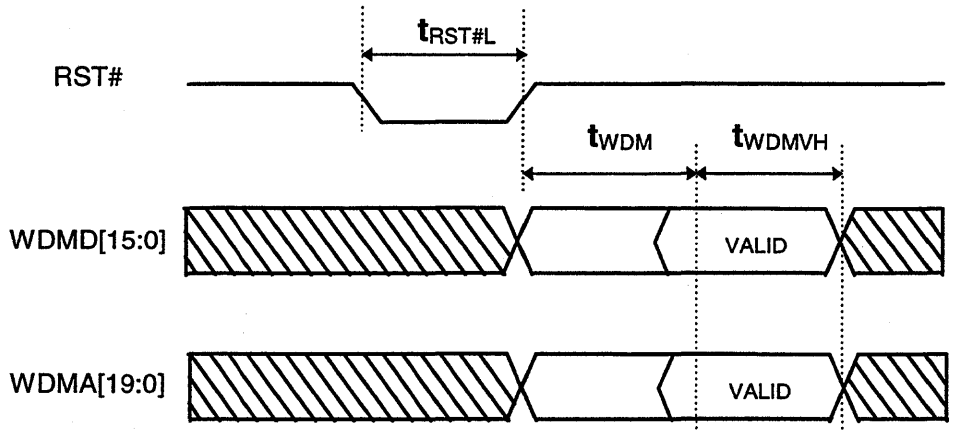


Figure 9-1: *PCI Reset and Jumper Latch Timing*

9.3.2 PCI CLOCK REQUIREMENT

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{PCKP}	PCI Bus Clock Period	30			nS	
t_{PCKL}	PCI Bus Clock Low Time	12			nS	
t_{PCKH}	PCI Bus Clock High Time	12			nS	

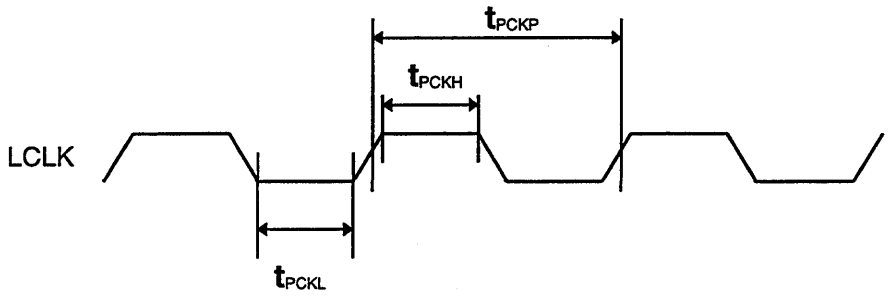


Figure 9-2: *PCI Clock Timing*

9.3.3 PCI BUS TIMING (I/O READ OPERATION)

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{SPCI}	Input Setup Time to LCLK	7			nS	
t_{HPCI}	Input Hold Time to LCLK	0	20		nS	
t_{PPCI}	Output Propagation Delay Time from LCLK	2		11	nS nS	0 pF Load 50 pF Load

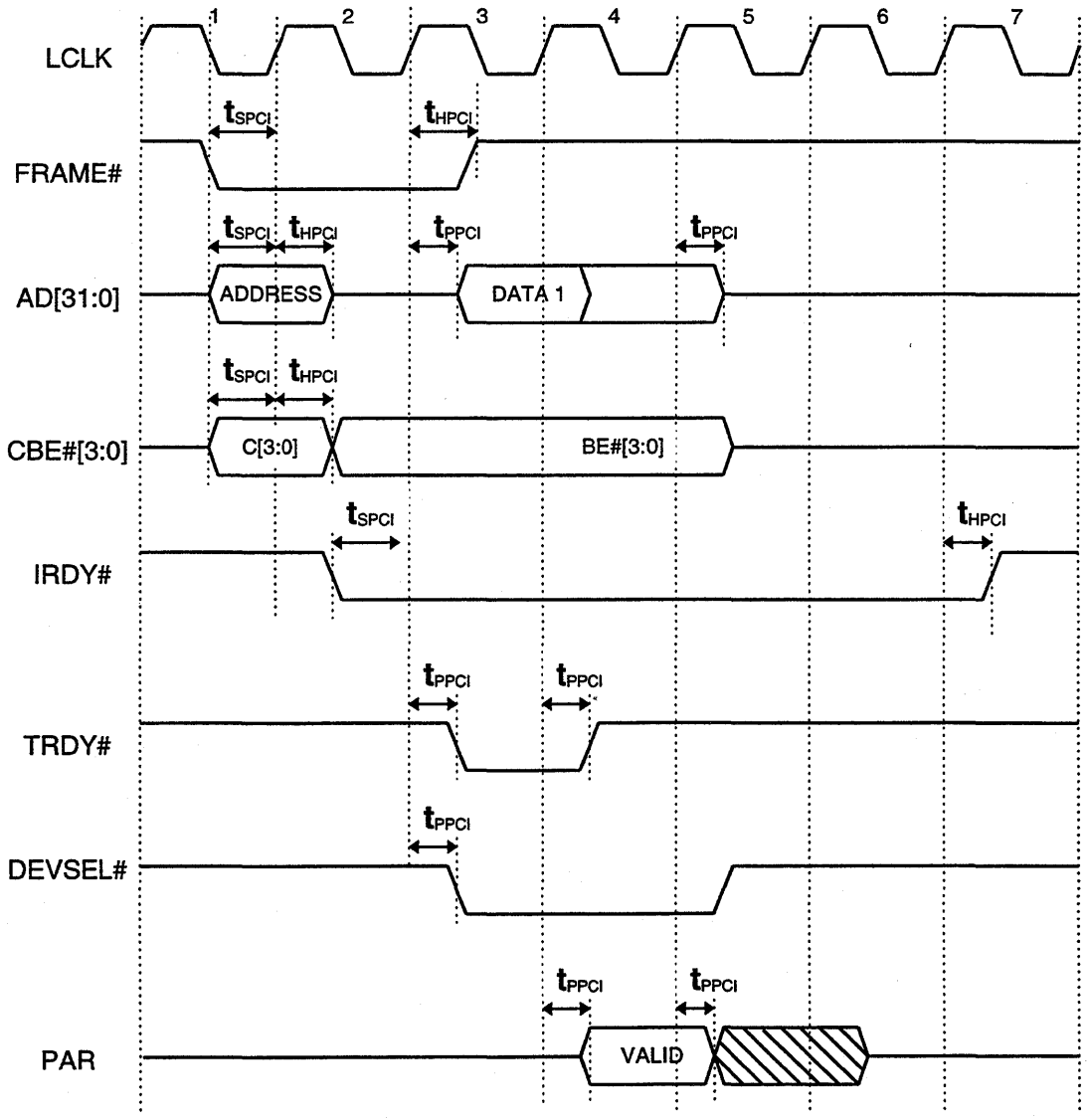


Figure 9-3: *PCI Bus Timing (I/O Read Operation)*

9.3.4 PCI BUS TIMING (I/O WRITE OPERATION)

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{SPCI}	Input Setup Time to LCLK	7			nS	
t_{HPCI}	Input Hold Time to LCLK	0			nS	
t_{PPCI}	Output Propagation Delay Time from LCLK	2		11	nS nS	0 pF Load 50 pF Load

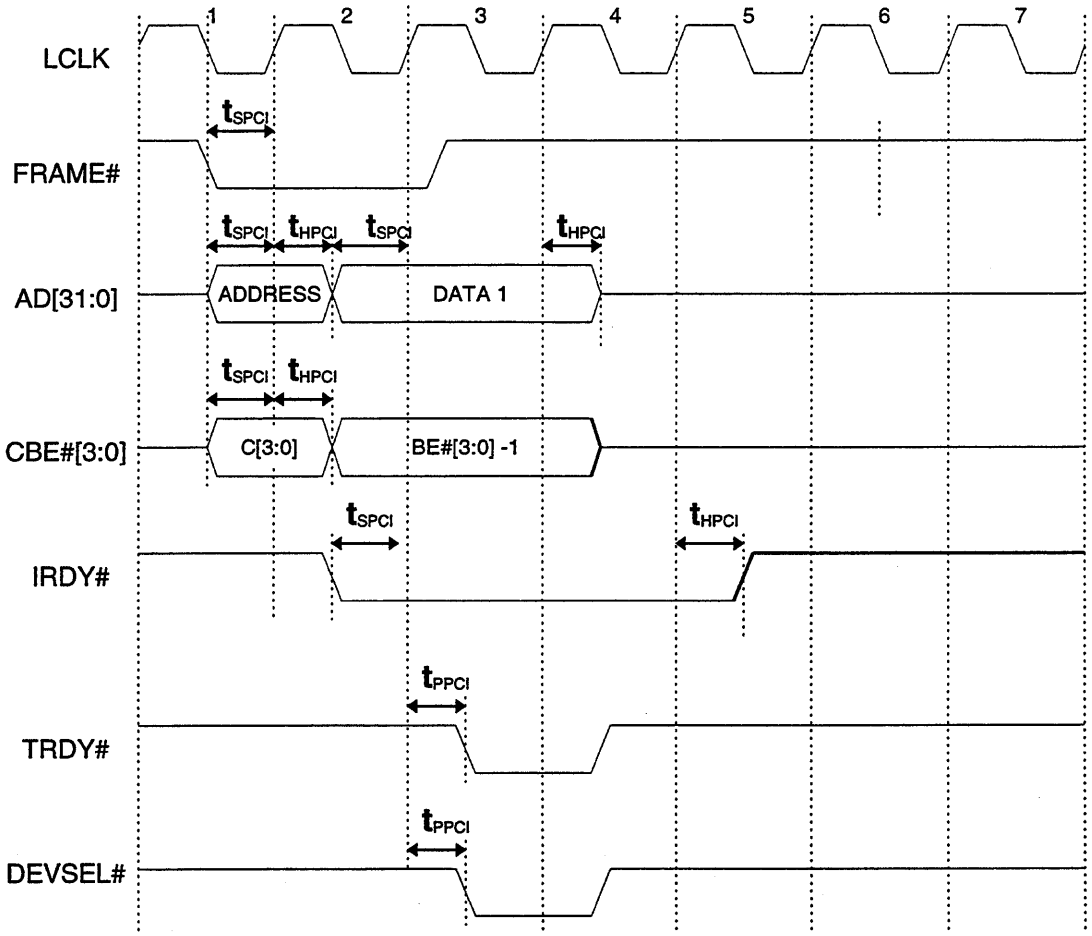


Figure 9-4: *PCI Bus Timing (I/O Write Operation)*

9.3.5 PCI BUS MASTER REQUEST TIMING

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{SPCI}	Input Setup Time to LCLK	7			nS	
t_{HPCI}	Input Hold Time to LCLK	0			nS	
t_{PPCI}	Output Propagation Delay Time from LCLK	2		11	nS nS	0 pF Load 50 pF Load

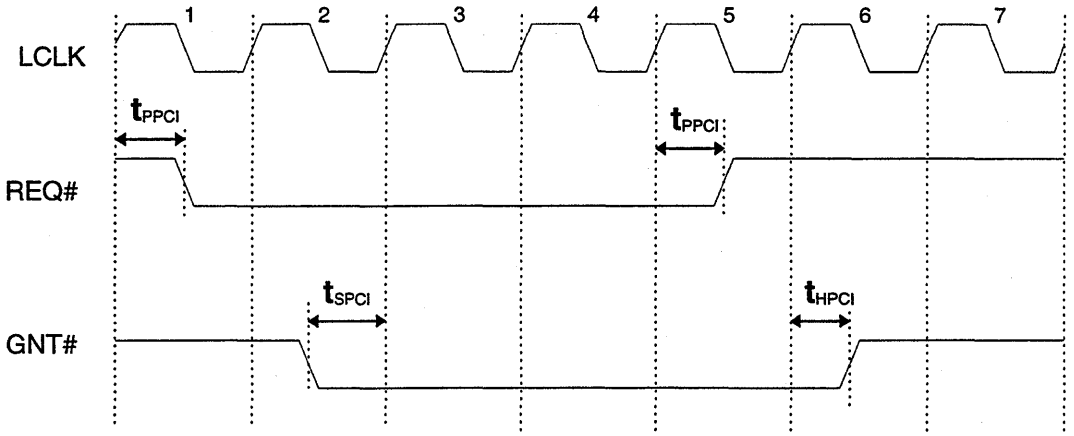


Figure 9-5: *PCI Bus Master Request*

9.3.6 PCI BUS MASTER READ/WRITE TIMING

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{SPCI}	Input Setup Time to LCLK	7			nS	
t_{HPCI}	Input Hold Time to LCLK	0			nS	
t_{PPCI}	Output Propagation Delay Time from LCLK	2		11	nS nS	0 pF Load 50 pF Load

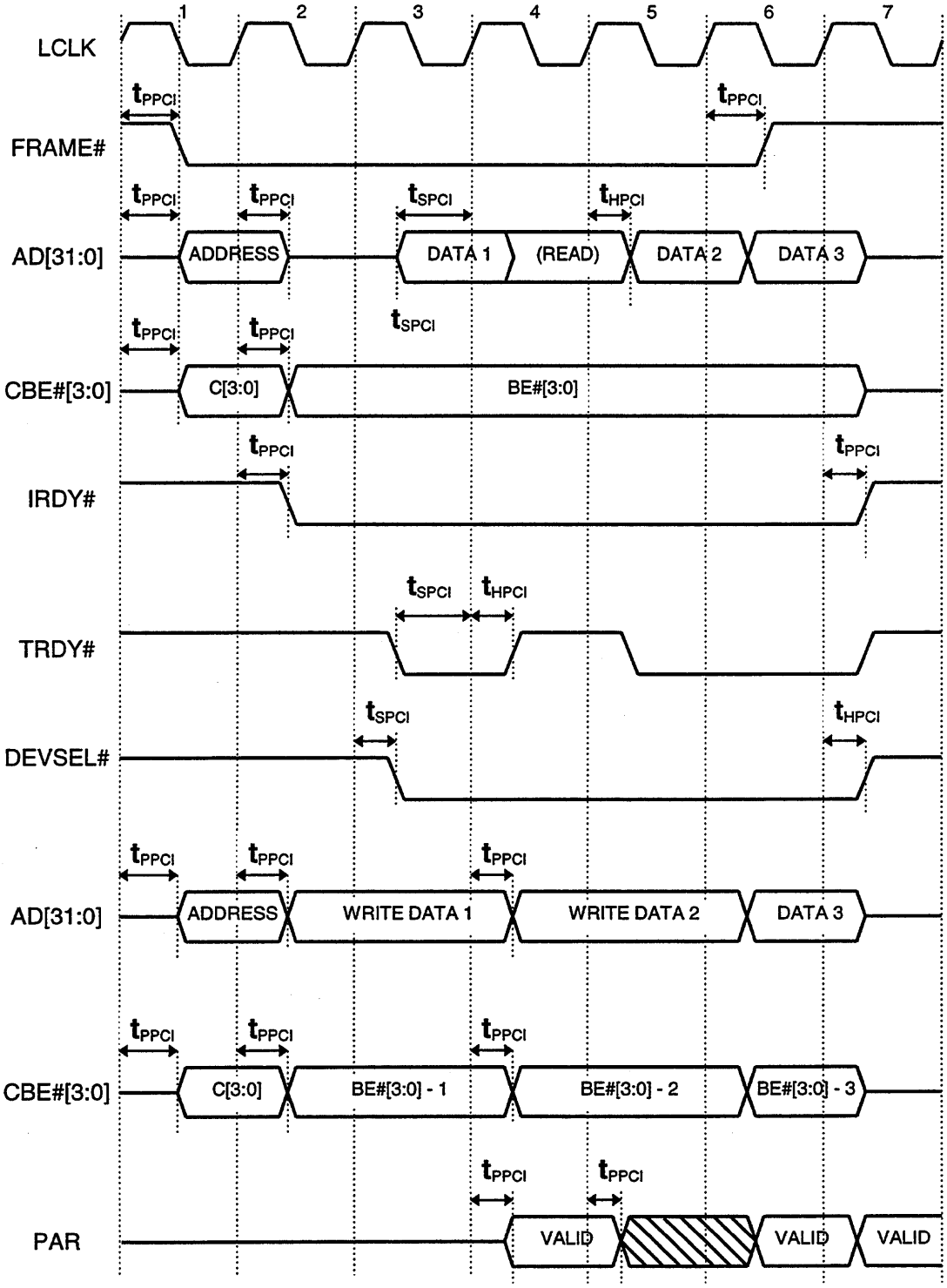
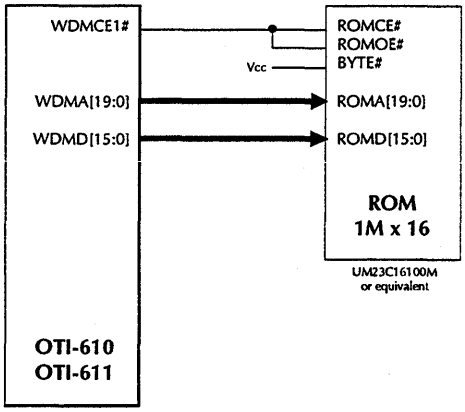


Figure 9-6: *PCI Bus Master Read/Write Timing*

9.3.7 ROM MEMORY INTERFACE TIMING



Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{CEW}	Chip Enable Pulse Width			150	nS	

ROM Requirements:

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{ACE}	Chip Enable Access Time			70	nS	
t_{AOE}	Output Enable Access Time			70	nS	
t_{HZ}	Data Hold Time to Hi-Z			30	nS	

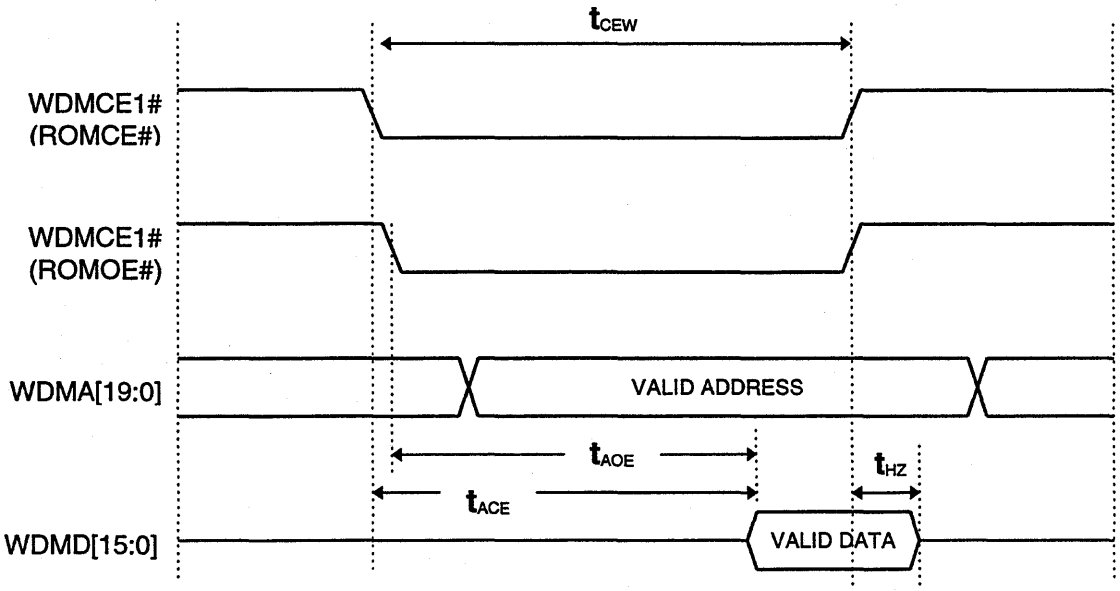
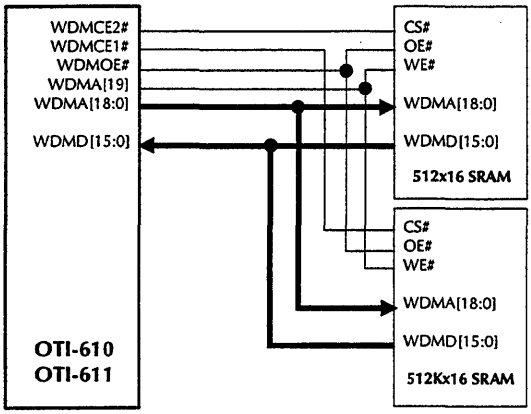


Figure 9-7: *External CMOS Mask ROM Interface Timing Requirements*

9.3.8 SRAM MEMORY INTERFACE TIMING



Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{CEW}	Chip Enable Pulse Width			150	nS	

SRAM Requirements (maximum):

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
t_{ACE}	Chip Enable Access Time			70	nS	
t_{AOE}	Output Enable Access Time			70	nS	
t_{HZ}	Data Hold Time to Hi-Z			30	nS	

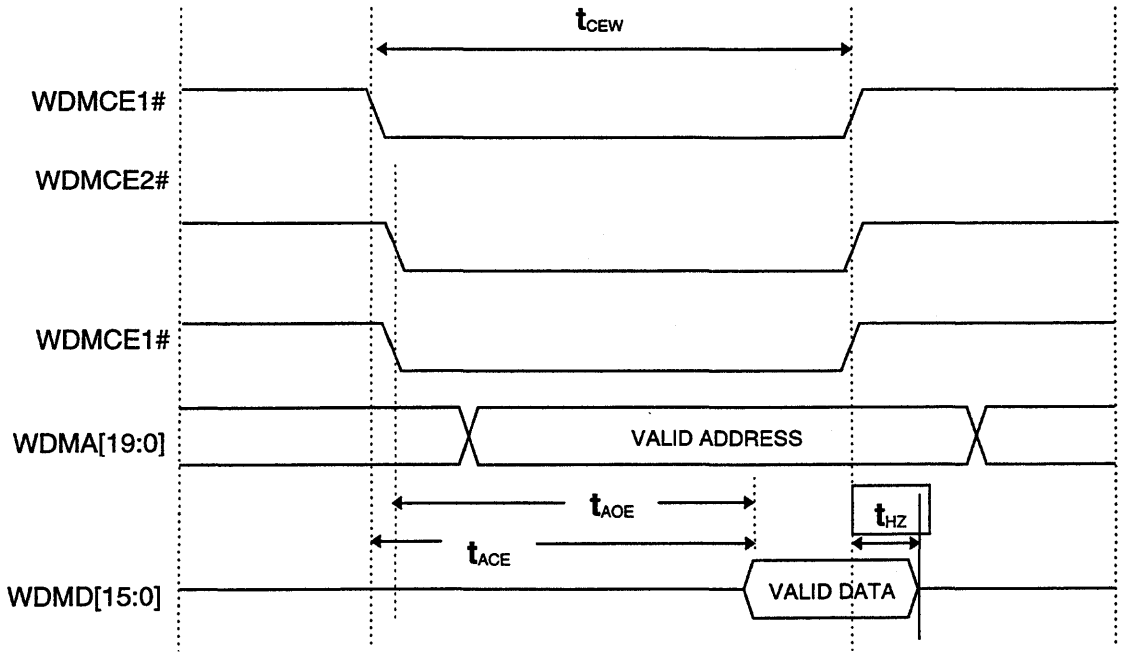


Figure 9-8: *External SRAM Memory Interface Timing Requirements*

9.4 AC-LINK TIMING CHARACTERISTICS

A breakout of the signals connecting the OTI-610/OTI-611 to an AC '97 Codec is shown in the table and figure below.

OTI-610/OTI-611 Signal Name	Type	OTI-612 or AC '97 Codec Signal Name- AC-Link Signal Name	Type	Description
ARESET#	O	RESET#	I	Master H/W Reset to AC '97 Codec from OTI-610 or OTI-611
AFS	O	SYNC	I	48-KHz fixed rate sample sync from OTI-610 or OTI-611
ASCLK	I	BIT_CLK	O	12.288-MHz serial data clock (Fx/2 from AC '97 Codec) to OTI-610 or OTI-611. Fx=24.576 MHz
ASDO	O	SDATA_OUT	I	Serial, time division multiplexed output stream to AC '97 Codec from OTI-610 or OTI-611
ASDI	I	SDATA_IN	O	Serial, time division multiplexed output stream from AC '97 Codec to OTI-610 or OTI-611

Note: Unless otherwise noted, $T_{ambient}$ = 25°C, AVdd = DVdd = 5VDC; AVss = DVss = 0V; 50pF external load

Throughout the rest of this section on AC-Link timing, AC-Link signal names will be given along with the equivalent OTI-610 and OTI-611 signal names. AC-Link signal names appearing in descriptive text will be printed in italics and will be enclosed within parentheses.

Tables containing signal names will show both the OTI-610/OTI-611 and AC-Link signal names in the same way.

Example:

OTI-610/OTI-611 Signal Name	**AC-Link Signal Name**
ARESET#	*(RESET#)*

Timing diagrams will be presented with the OTI-610/OTI-611 signal name in the illustration.

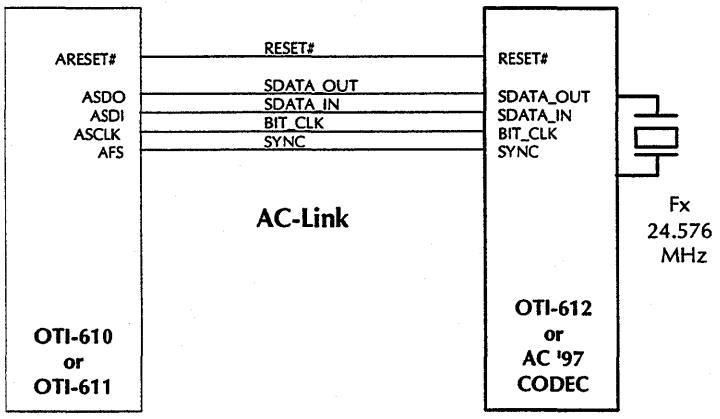


Figure 9-9: *OTI-610/OTI-611 AC-Link Connection to an AC '97 Compatible Codec*

9.4.1 AC-LINK RESET TIMING

Cold Reset

Parameter	Symbol	Min	Typ	Max	Units
ARESET *(RESET#)* Active Low Pulse Width	T_{rst_low}	1.0	-	-	uS
ASCLK *(BIT_CLK)* Startup Delay from ARESET# *(RESET#)* high	$T_{rst2clk}$	162.8	-	-	uS

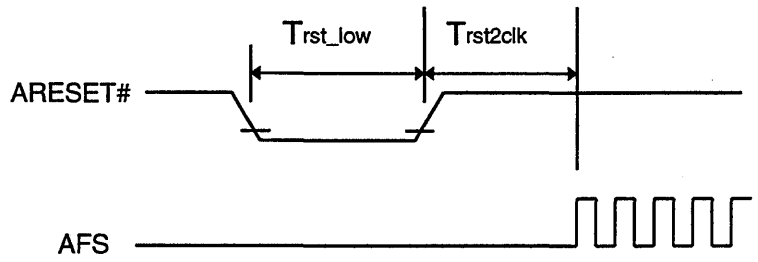


Figure 9-10: *AC-Link Cold Reset Timing*

Warm Reset

Parameter	Symbol	Min	Typ	Max	Units
AFS *(SYNC)* active High Pulse Width	T_{sync_high}	-	1.3	-	uS
AFS *(SYNC)* Inactive to ASCLK *(BIT_CLK)* Startup Delay	$T_{sync2clk}$	162.8	-	-	uS

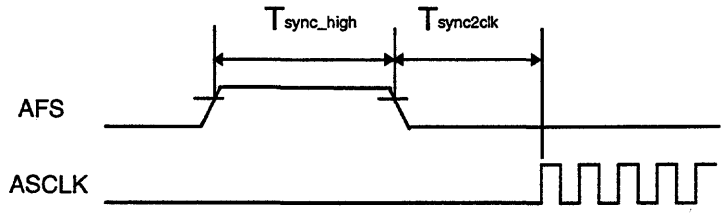


Figure 9-11: *AC-Link Warm Reset Timing*

9.4.2 CLOCKS

(50pF external load)

Parameter	Symbol	Min	Typ	Max	Units
[1]ASCLK *(BIT_CLK)* Frequency		-	12.288	-	MHz
ASCLK *(BIT_CLK)* Period	T_{clk_period}	-	81.4	-	nS
ASCLK *(BIT_CLK)* Output Jitter		-	-	750	pS
ASCLK *(BIT_CLK)* High Pulse Width[1]	T_{clk_high}	32.56	40.7	48.84	nS
ASCLK *(BIT_CLK)* Low Pulse Width[1]	T_{clk_low}	32.56	40.7	48.84	nS
AFS *(SYNC)* Frequency		-	48.0	-	KHz
AFS *(SYNC)* Period	T_{sync_period}	-	20.8	-	uS
AFS *(SYNC)* High Pulse Width	T_{sync_high}	-	1.3	-	uS
AFS *(SYNC)* Low Pulse Width	T_{sync_low}	-	19.5	-	uS

Note: [1]Worst case duty cycle restricted to 40/60.

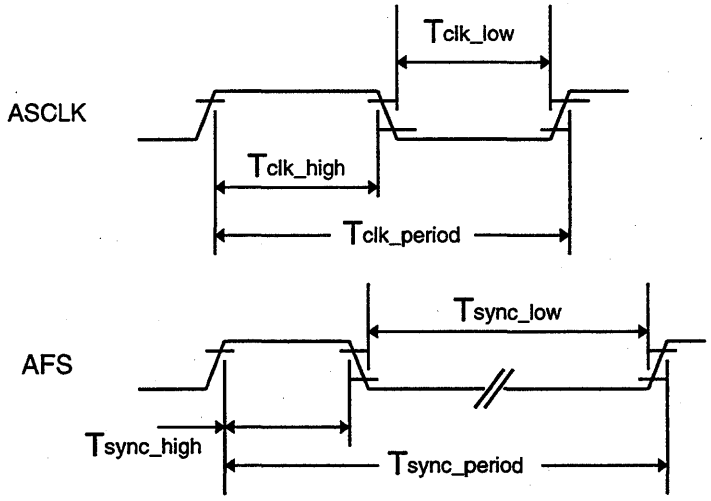


Figure 9-12: *AC-Link Clock Timing*

9.4.3 DATA SETUP AND HOLD

(50pF external load)

Parameter	Symbol	Min	Typ	Max	Units
Setup to Falling Edge of ASCLK *(BIT_CLK)*	T_{setup}	15.0	-	-	nS
Hold from Falling Edge of ASCLK *(BIT_CLK)*	T_{hold}	5.0	-	-	nS

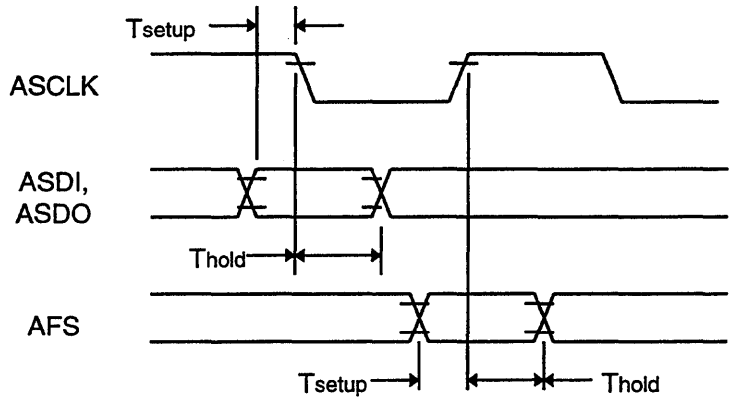


Figure 9-13: *AC-Link Data Setup and Hold Timing*

9.4.4 SIGNAL RISE AND FALL TIMES

(50pF external load)

Parameter	Symbol	Min	Typ	Max	Units
ASCLK *(BIT_CLK)* Rise Time	$Trise_{clk}$	2	-	-	nS
ASCLK *(BIT_CLK)* Fall Time	$Tfall_{clk}$	2	-	-	nS
AFS *(SYNC)* Rise Time	$Trise_{sync}$	2	-	-	nS
AFS *(SYNC)* Fall Time	$Tfall_{sync}$	2	-	-	nS
ASDI *(SDATA_IN)* Rise Time	$Trise_{din}$	2	-	-	nS
ASDI *(SDATA_IN)* Fall Time	$Tfall_{din}$	2	-	-	nS
ADSO *(SDATA_OUT)* Rise Time	$Trise_{dout}$	2	-	-	nS
ADSO *(SDATA_OUT)* Tall Time	$Tfall_{dout}$	2	-	-	nS

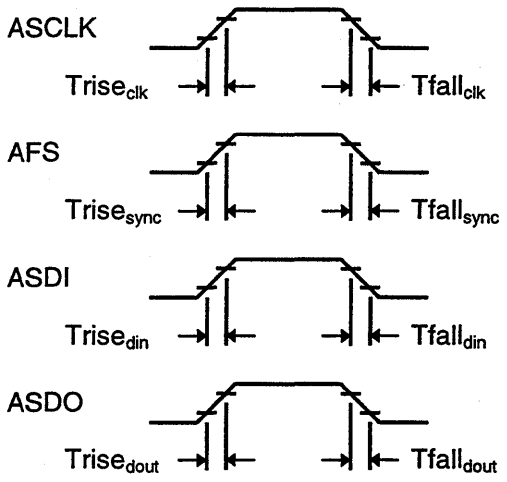


Figure 9-14: *AC-Link Signal Rise and Fall Timing*

9.4.5 AC-LINK LOW POWER MODE TIMING

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to ASCLK *(BIT_CLK)*, ASDI *(SDATA_IN)* Low	T_{s2_pdown}	-	-	1.0	uS

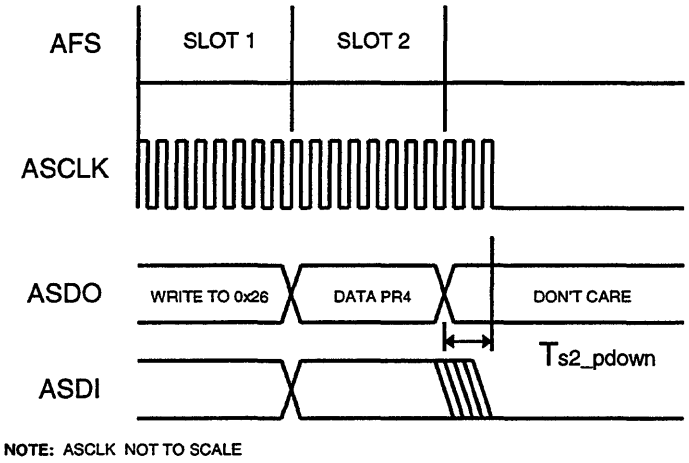


Figure 9-15: *AC-Link Low Power Mode Timing*

9.4.6 ATE IN-CIRCUIT TEST MODE

Parameter	Symbol	Min	Typ	Max	Units
Setup to Trailing Edge of ARESET# *(RESET#)*	$T_{setup2rst}$	15.0	-	-	nS
Rising Edge of ARESET# *(RESET#)* to Hi-Z Delay	T_{off}	-	-	25.0	nS

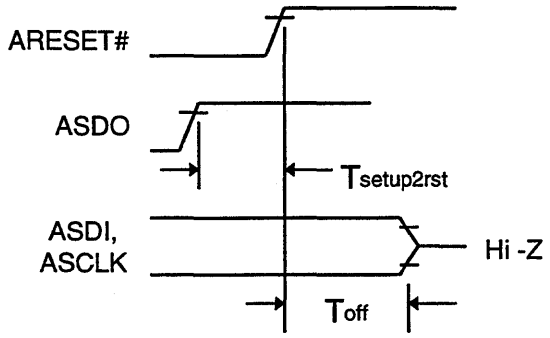


Figure 9-16: *AC-Link ATE Test Mode Timing*

9.5 AUDIO/MODEM CODEC PORT TIMING (STLC7549)

Throughout the rest of this section on STLC7549 Audio/Modem Codec timing, STLC7549 signal names will be given along with the equivalent OTI-611 signal names. STLC7549 signal names appearing in descriptive text will be printed in italics and will be enclosed within parentheses.

Tables containing signal names will show both the OTI-611 and STLC7549 signal names in the same way.

Example:

OTI-611 Signal Name	**STLC7549 Signal Name**
ARESET#	*(RESET#)*

Timing diagrams will be presented with the OTI-611 signal name in the illustration.

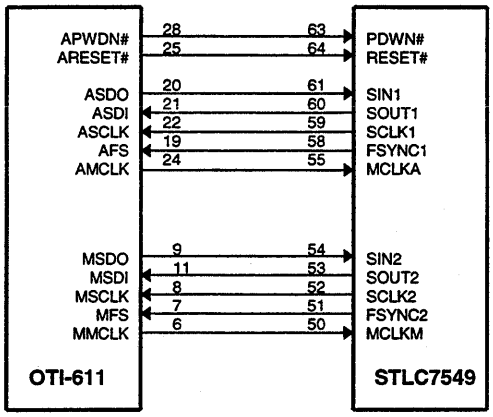


Figure 9-17: *Simplified Connection Diagram — OTI-611 to STLC7549*

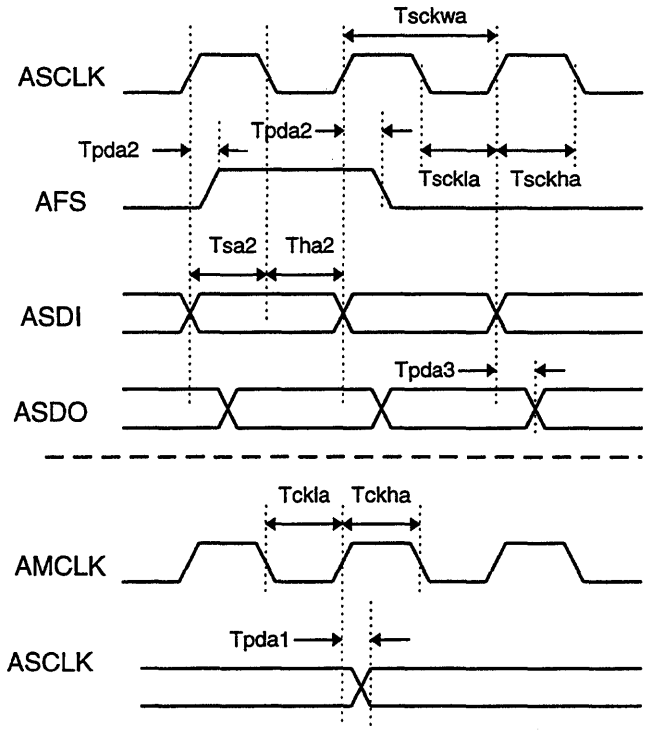


Figure 9-18: *OTI-611 to STLC7549 Timing*

OTI-611 to STLC7549 Timing Chart:

Symbol	Parameter	Min.	Typ	Max.	Units
MCLKA	STLC7549 Master Clock Input Range - Audio Codec	6.144	11.2896	12.288	MHz
AMCLK	Master Clock - Audio Codec		11.2896		MHz
MCLKM	STLC7549 Master Clock Input Range - Modem Codec	1.8432	2.4576	3.84	MHz
MMCLK	Master Clock - Modem Codec		2.4576		MHz
Tpwa	Master Clock Period - Audio		1/AMCLK		-
Tpwm	Master Clock Period - Modem		1/MMCLK		-
Tpda1	ASCLK *(SCLK1)* Output Delay from AMCLK Rising Edge			10	nS
Tpda2	AFS *(FSYNC1)* Delay Time			10	nS
Ts2	ASDI Setup Time to ASCLK *(SCLK1)* Falling Edge	10			nS
Th2	ASDI Hold Time from ASCLK *(SCLK1)* Falling Edge	5			nS
Tpda3	ASDO Delay from ASCLK *(SCLK1)* Rising Edge			15	nS
Tsckw1	ASCLK *(SCLK1)* Period		1/[64xFSA]		S
Tsckh1	ASCLK *(SCLK1)* High Time	142			nS
Tsckl1	ASCLK *(SCLK1)* Low Time	142			nS
Tsckw1	MSCLK *(SCLK2)* Period		1/[64xFSM]		S
Tsckh1	MSCLK *(SCLK2)* High Time	851			nS
Tsckl1	MSCLK *(SCLK2)* Low Time	851			nS
FSA	Audio Sample Frequency		AMCLK/[4xNx64] N=1, FSA=44.1 N=2, FSA=22.05		 KHz KHz
FSM	Modem Sample Frequency		MMCLK/[4x64]		Hz

Note: AMCLK and MMCLK depend upon software programming

9.6 AUDIO CODEC PORT TIMING (STLC7549AC)

Throughout the rest of this section on STLC7549AC Audio Codec timing, STLC7549AC signal names will be given along with the equivalent OTI-610 signal names. STLC7549AC signal names appearing in descriptive text will be printed in italics and will be enclosed within parentheses.

Tables containing signal names will show both the OTI-610 and STLC7549AC signal names in the same way.

Example:

OTI-610 Signal Name	**STLC7549AC Signal Name**
ARESET#	*(RESET#)*

Timing diagrams will be presented with the OTI-610 signal name in the illustration.

Note: Consult SGS Thomson STLC7549AC data sheet for complete technical specifications and applications information.

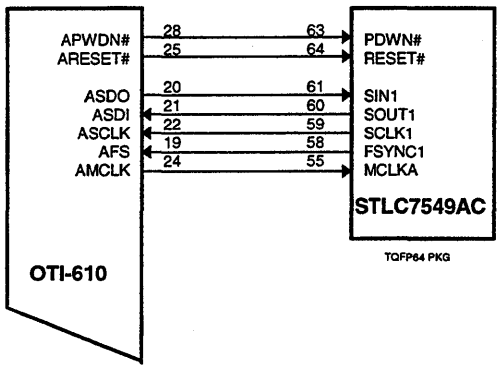


Figure 9-19: *Simplified Connection Diagram — OTI-610 to STLC7549AC*

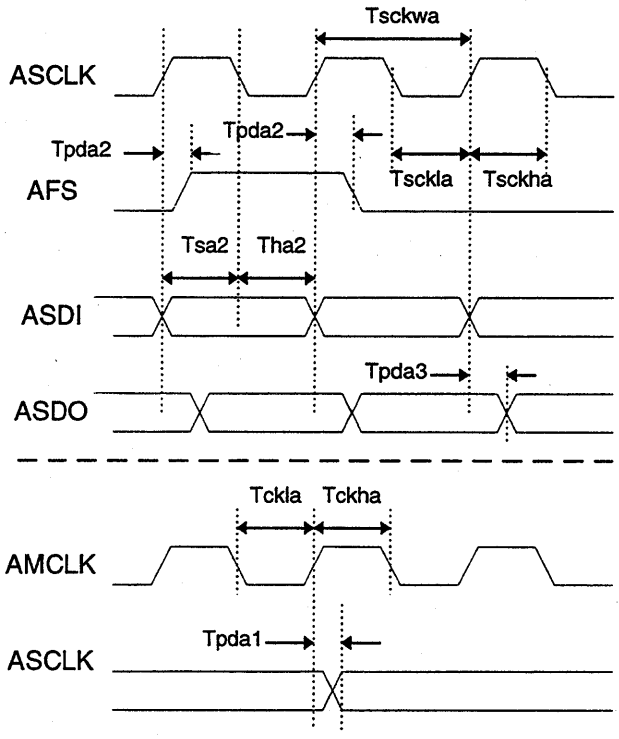


Figure 9-20: *OTI-610 to STLC7549AC Timing*

OTI-610 to STLC7549AC Timing Chart:

Symbol	Parameter	Min.	Typ	Max.	Units
MCLKA	STLC7549AC Master Clock Input Range	6.144	11.2896	12.288	MHz
AMCLK	Master Clock		11.2896		MHz
Tpwa	Master Clock Period		1/AMCLK		-
Tpda1	ASCLK *(SCLK1)* Output Delay from AMCLK Rising Edge			10	nS
Tpda2	AFS *(FSYNC1)* Delay Time			10	nS
Tsa2	ASDI Setup Time to ASCLK *(SCLK1)* Falling Edge	10			nS
Tha2	ASDI Hold Time from ASCLK *(SCLK1)* Falling Edge	5			nS
Tpda3	ASDO Delay from ASCLK *(SCLK1)* Rising Edge			15	nS
Tsckwa	ASCLK *(SCLK1)* Period		1/[64xAFS] 1/[64x(FSYNC1)]		S
Tsckha	ASCLK *(SCLK1)* High Time	142			nS
Tsckla	ASCLK *(SCLK1)* Low Time	142			nS
FSA	Audio Sample Frequency		AMCLK/[4xNx64] N=1, FSA=44.1 N=2, FSA=22.05		 KHz KHz

Note: AMCLK depends upon software programming

9.7 MODEM CODEC PORT TIMING (ST7546)

Throughout the rest of this section on ST7546 Modem Codec timing, ST7546 signal names will be given along with the equivalent OTI-611 signal names. ST7546 signal names appearing in descriptive text will be printed in italics and will be enclosed within parentheses.

Tables containing signal names will show both the OTI-611 and ST7546 signal names in the same way.

Example:

OTI-611 Signal Name	**ST7546 Signal Name**
MRESET#	*(RESET#)*

Timing diagrams will be presented with the OTI-611 signal name in the illustration.

Note: Consult SGS Thomson ST7546 data sheet for complete technical specifications and applications information.

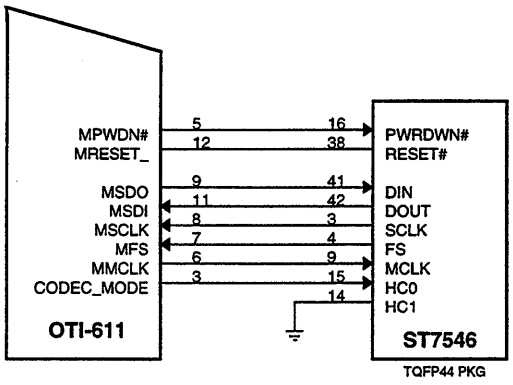


Figure 9-21: *OTI-611 to ST7546 Simplified Connection Diagram*

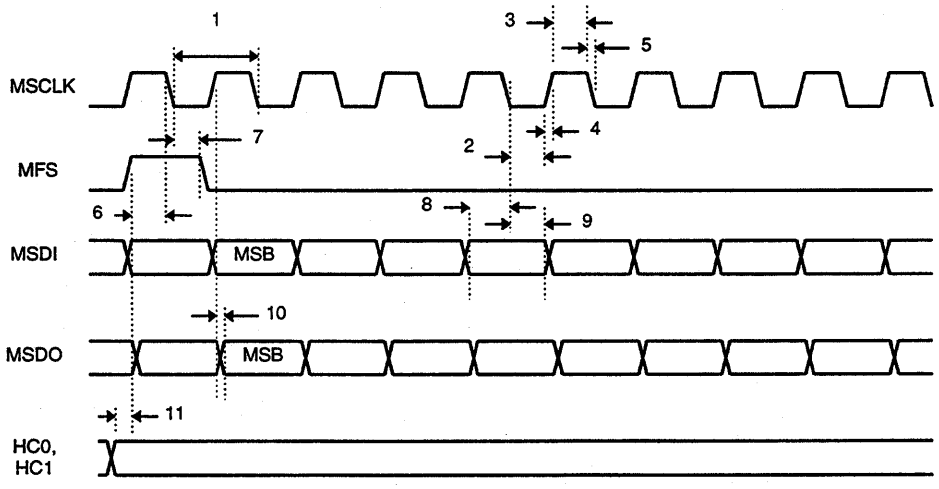


Figure 9-22: *OTI-611 to ST7546 Serial Interface Timing Diagram*

OTI-611 to ST7546 Timing Chart:

Symbol	N	Parameter	Min.	Typ	Max.	Units
	1	MSCLK *(SCLK)* Period	300			nS
	2	MSCLK *(SCLK)* Width Low	150			nS
	3	MSCLK *(SCLK)* Width High	150			nS
	4	MSCLK *(SCLK)* Rise Time			10	nS
	5	MSCLK *(SCLK)* Fall Time			10	nS
	6	MFS *(FS)* Setup Time	20			nS
	7	MFS *(FS)* Hold Time	20			nS
	8	MDSI *(DIN)* Setup Time	20			nS
	9	MDSI *(DIN)* Hold Time	0			nS
	10	MSDO *(DOUT)* Valid Time			15	nS
	11	*HC0, HC1* Setup Time	20			nS
MCLK		ST7546 Master Clock Input Range	0.92	1.54	2.8	MHz
MMCLK		*Modem Master Clock, Derived from OTI-611 MCLK (Main Clock) For MCLK = 36.864 MHz		*MCLK/32 1.152		MHz MHz
Tpw		Modem Master Clock Cycle		868		nS
Tph		Pulse Width High	45		55	%
Tpl		Pulse Width Low	45		55	%

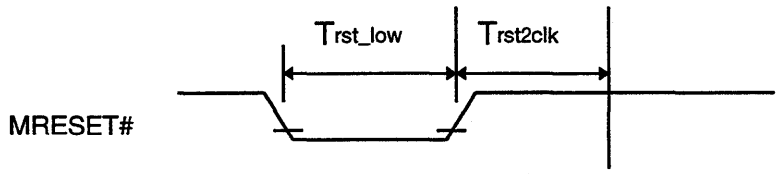


Figure 9-23: *OTI-611 to ST7546 Reset Timing*

OTI-611 to ST7546 Reset Timing Chart:

Symbol	Parameter	Min.	Typ	Max.	Units	Notes
T_{rst_low}	MRESET# *(RESET#)* active low pulse width	100	-	-	nS	-

9.8 TDM AUDIO/MODEM CODEC PORT TIMING (AD1843)

Throughout the rest of this section on AD1843 Modem Codec timing, AD1843 signal names will be given along with the equivalent OTI-611 signal names. AD1843 signal names appearing in descriptive text will be printed in italics and will be enclosed within parentheses.

Tables containing signal names will show both the OTI-611 and AD1843 signal names in the same way.

Example:

OTI-611 Signal Name	**AD1843 Signal Name**
ARESET#	*(RESET#)*

Timing diagrams will be presented with the OTI-611 signal name in the illustration.

Note: Consult Analog Devices AD1843 data sheet for complete technical specifications and applications information.

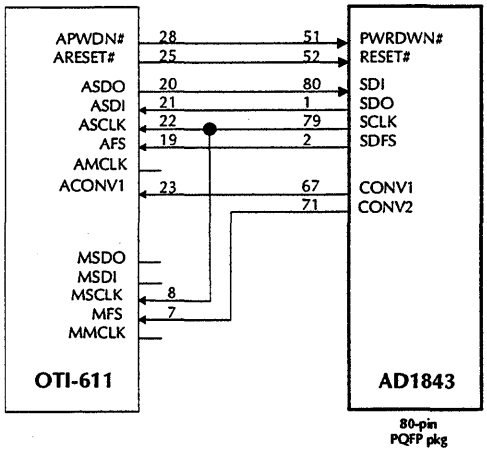


Figure 9-24: *OTI-611 to AD1843 Simplified Connection Diagram*

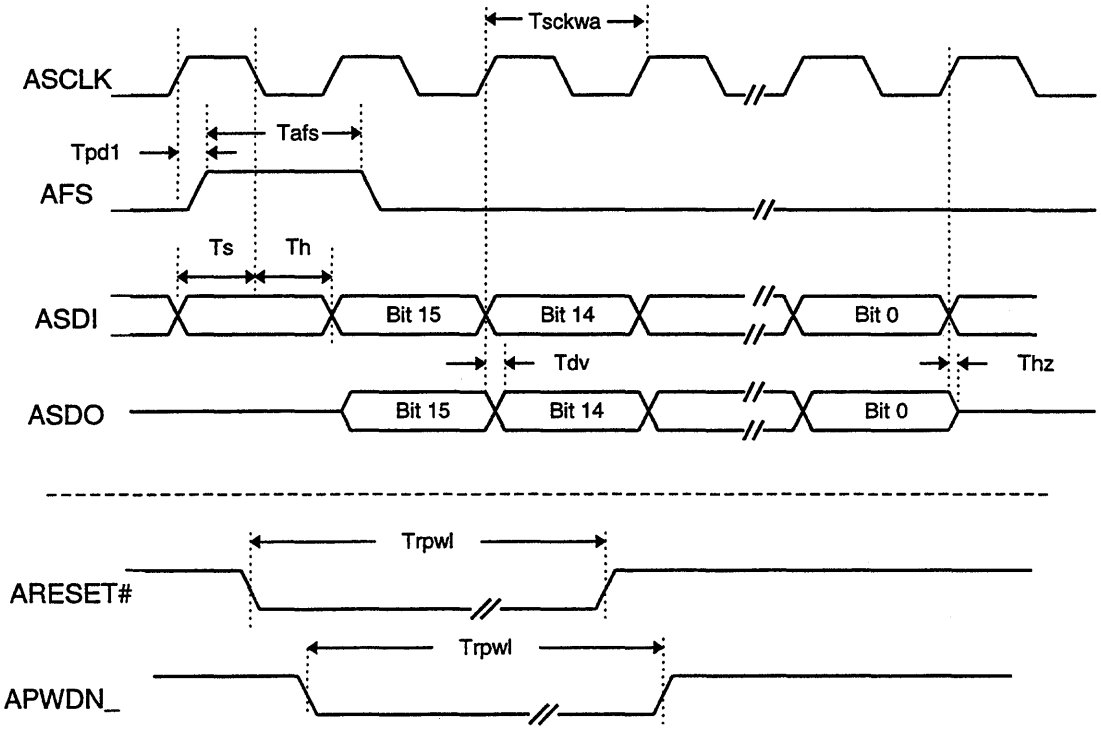


Figure 9-25: *OTI-611 to AD1843 Timing Diagram*

OTI-611 to AD1843 Timing Chart:

Symbol	Parameter	Min.	Typ	Max	Units
SCLK	AD1843 Master Clock Output Master Mode Only		12.288	16.384	MHz
ASCLK	Master Clock Input - Audio		12.288	16.384	MHz
MSCLK	Master Clock Input - Modem		12.288		MHz
Tpwa	Master Clock Period		1/ASCLK		-
Tpd1	AFS *(SDFS)* Delay Time from ASCLK Rising Edge			15	nS
Tafs	AFS *(SDFS)* Pulse Width High		80		nS
Ts	ASDI Setup Time to ASCLK *(SCLK)* Falling Edge	5			
Th	ASDI Hold Time from ASCLK *(SCLK)* Falling Edge	5			
Tpda3	(SDO) Delay from ASCLK *(SCLK)* Rising Edge			10	nS
Tdv	ASDO Valid Delay from ASCLK (SCLK) Rising Edge			15	nS
Tsckwa	ASCLK *(SCLK)* Period		1/[64xAFS] 1/[64x(FSYNC1)]		S
Trpwl	ARESET# *(RESET#)* and APWDN_ *(PWRDWN#)* Low Pulse Width	100			nS
Thz	*(SDO)* Hi-Z State Delay from ASCLK *(SCLK)*			15	nS

9.9 I²S PORT TIMING

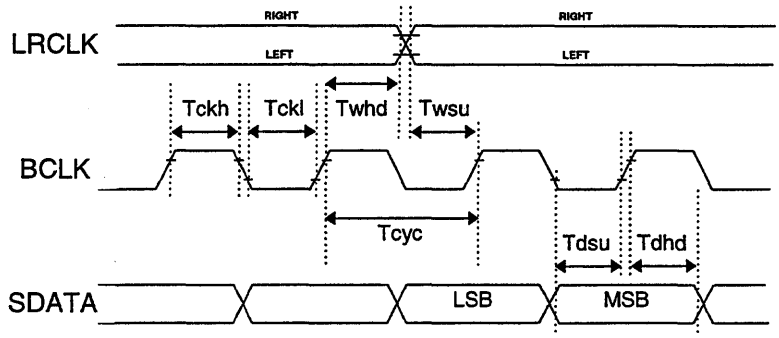


Figure 9-26: *OTI-611 I²S Port Timing Diagram*

OTI-611 I²S Port Timing Chart:

Symbol	Parameter	Min.	Typ	Max.	Units
Fbck	BCLK Frequency			18.4	MHz
Tcyc	BCLK Cycle Time	54			nS
Tckh	BCLK HIGH Time	15			nS
Tckl	BCLK LOW Time	15			nS
Tdsu	SDATA Setup Time	12			nS
Tdhd	SDATA Hold Time	2			nS
Twsu	LRCLK Setup Time	12			nS
Twhd	LRCLK Hold Time	2			nS

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CHAPTER 10 THERMAL SPECIFICATIONS

The OTI-611 device operates properly when the Case Temperature (T_c) is within the specified temperature range of 0°C to 70°C.

Symbol	Parameter	Min.	Max.	Unit	Condition
θ_{JA}	Package Junction-to-Ambient Thermal Resistance		25	°C/Watt	No airflow, with internal heat spreader in the package
T_{OPER}	Operating Temperature, Case (T_C)	0	+70	°C	DVdd = 5.25V maximum
T_{STG}	Storage Temperature	-65	+150	°C	
T_J	Junction Temperature (at ambient temperature = 25°C)		55.6 60.4	°C °C	DVdd = 5.0V P_D = 1220 mW DVdd = 5.25V P_D = 1410 mW
T_J	Junction Temperature (at ambient temperature = 70°C)		107 116	°C °C	DVdd = 5.0V DVdd = 5.25V
P_{DMAX}	Absolute Maximum Power Dissipation		2200	mW	T_J = 125°C

Note: $T_J = T_A + \theta_{JA} * P_D$
Oak Technology specification for T_J = 125°C maximum

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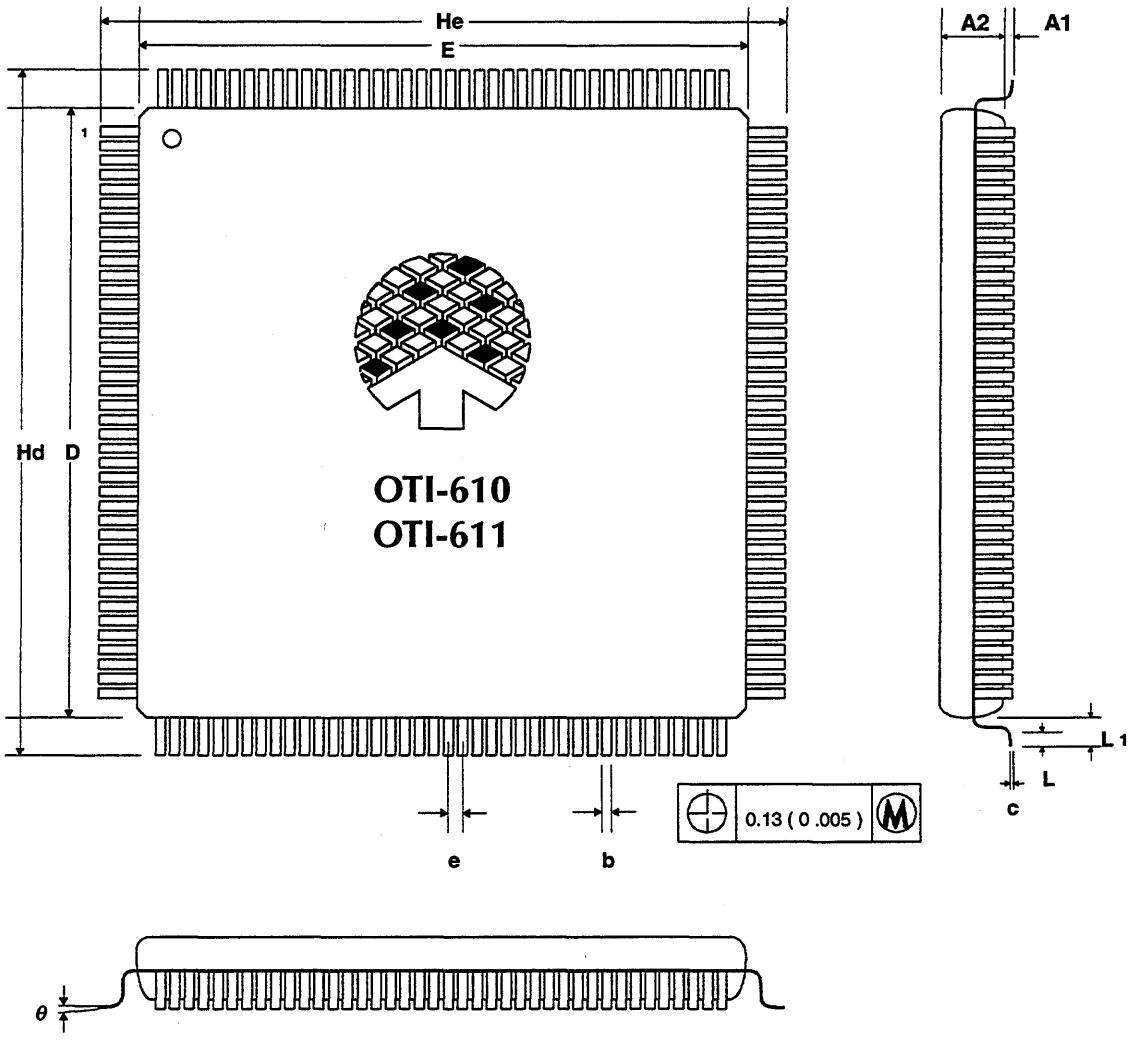
CHAPTER 11

MECHANICAL SPECIFICATIONS

The OTI-610 and OTI-611 are packaged in the 160-pin PQFP plastic package.



Symbol	Millimeter			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A_1	0.05	0.25	0.50	0.002	0.010	0.020
A_2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e	-	0.65	-	-	0.026	-
Hd	30.95	31.20	31.45	1.218	1.228	1.238
He	30.95	31.20	31.45	1.218	1.228	1.238
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	-	1.60	-	-	0.063	-
Y	-	-	0.08	-	-	0.003
θ	0	-	10	0	-	10

APPENDIX A

OTI-611 HSP FAX/DATA MODEM

A.1 HSP FAX/MODEM

The Host Signal Processing (HSP) based fax/modem software is supplied with and only works with the OTI-611 TelAudia3D audio/communications accelerator.

The HSP-based fax/modem software supplied with the OTI-611 is fully compliant to International Telecommunications Union (ITU) V.34 and V.34+ (sometimes known as V.34*bis*) specifications and well as ITU Group 3 facsimile standards. It also conforms to the industry-standard AT Command Set for fax/data modems.

The HSP fax/modem currently supports V.34/V.34+, but can be upgraded to support 56 Kbps at the time the ITU publishes its final 56-Kbps standard specification.

A.1.1 SOFTWARE ENVIRONMENT

All modem data pump and controller functions are performed in software, utilizing the power of the computer central processing unit (CPU) and system memory (RAM). The HSP V.34 fax/modem is supplied as executable code, and is part of the OTI-611 installation software.

The executable code is designed to work with the hardware support structures within the OTI-611 to interface between the HSP software and external hardware modem codec and Data Acquisition Answer (DAA) structure which connects to the public switched telephone network (PSTN), thus forming a completely functional data and fax modem.

The HSP V.34 executable code is intended to operate in a Windows 95 software environment and functions as a legitimate Windows 95 application when used with the OTI-611 in an audio and communications design.

A.1.2 HARDWARE ENVIRONMENT

The HSP V.34 fax/modem code is available for Pentium class and Pentium MMX class based computer systems. Minimum system recommendations in the OTI-611 environment are:

- Operating System - Windows 95 and Windows NT 4.0
- CPU - 166-MHz Pentium class or Pentium MMX class
- Total System RAM - 32MB
- Free Hard Disk Space - 2MB

A.2 STANDARD FEATURES

- V.34 (28.8 Kbps)/V.34+ (33.6 Kbps) data modem, capable for upgrading to 56 Kbps
- Group 3 fax modem to 14,400 bps
- Industry-standard AT Commands
- EIA Class 1 Fax Commands
- V.42 LAPM & MNP 2-4 Error Correction
- V.42*bis* & MNP 5 Data Compression
- Tone or pulse dial support

A.3 TECHNICAL SPECIFICATIONS

Data Standards:

ITU-T V.21	0-300 bps
ITU-T V.22	1,200 bps
ITU-T V.22*bis*	2,400 bps
ITU-T V.23	1,200/75 bps
ITU-T V.32	9,600 bps
ITU-T V.32*bis*	14,400 bps
ITU-T V.34	28,800 bps
ITU-T V.34+	33,600 bps
Bell 103	0-300 bps
Bell 212A	1,200 bps

Facsimile Standards:

ITU-T V.21	300 bps Channel 1
ITU-T V.17	14,400 bps
ITU-T V.27*ter*	4,800 bps
ITU-T V.29	9,600 bps

Asynchronous Data:

Start Bits	Data Bits	Parity Bits	Stop Bits
1	7	odd or even	1 or 2
1	7	mark or space	1 or 2
1	8	none	2
1	8	none	1 or 2

Error Correction:

ITU-T V.42 LAPM and MNP 2-4

Data Compression:

ITU-T V.42*bis* and MNP 5

Communications:

Receive Sensitivity:	-43 dBm
Transmit Level:	-10 dBm (± 1 dBm) Adj. if allowed by PTT

Dialing:

Pulse:	Mark	33 or 39 mSec
	Space	67 or 61 mSec (decadic)
Tone:	Duration	90 mSec DTMF
	Spacing	90 mSec DTMF

A.4 AT COMMAND SET

The HSP V.34 fax/modem supplied with the OTI-611 responds to the AT Commands listed in the table below. Parameters in **bold type** are the default values.

Command	Function
AT	Attention - this precedes all commands except A/
A/	Execute previous command - does not require a <CR>
A	Causes the modem to go off hook. If a call is coming in, the modem will try to answer it. The procedure for answering a call is a short silence and then an answer tone. Sending a character to the modem during this procedure will abort the answer procedure. The amount of time the modem will wait for a carrier is programmable by modifying the S7 register.
B0 **B1** B2	Select CCITT V.22 (1200 bps) **Select Bell 212A (1200 bps)** Select CCITT V23 Originate mode will transmit data at 75 bps and receive data at 1200 bps. Answer mode will transmit data at 1200 bps and receive data at 75 bps. The command NO (Disable Auto Mode) must be selected.
D	D alone will take the modem off-hook and wait for a dial tone (see X command for exceptions). The length of time to wait for a dial tone before dialing is programmable in register S6.
Dmn L W , ; @ ! S=(0-9) ^	ATDmn will dial a phone number where m is a modifer: L, W, ,, ;, @, !, or S. It will dial the telephone number n. Dial last number. Wait for dial tone. If you have selected X0 or X1 (disable dial tone detection), then you can use this modifier to override that setting. Pause during dial. The amount of time to pause is determined in register S8. Return to command mode after dialing. It doesn't wait for carrier or hang up. Wait for 5 seconds of silence. This is used to access systems that do not provide a dial tone. Hook flash. Causes the modem to go on-hook for 0.5 seconds. This is used in PBX systems and for voice features like call waiting. Dials a stored number. Up to ten numbers can be stored, and the addresses are from 0 to 9. To store a number into one of these addresses, use the &Z command. Turns on 1300-Hz calling tone.
E0 **E1**	Commands issued to the modem are not echoed to the local terminal. This only matters in the command mode. It does not affect the modem's ability to send response codes. **Commands are echoed to the local terminal.**

AT COMMAND SET (Cont'd)

Command	Function
H0 H1	Force modem on-hook (hang-up) Force modem off-hook (to answer or dial)
i0 I1 I2 I3 I4	Return numeric product code Return hardware variation code Report internal code Report software revision number Report product feature listing
L0 **L1** L2 L3	Speaker volume zero **Speaker volume low** Speaker volume low Speaker volume low (hardware currently limits volume adjustment to on/off)
M0 **M1** M2 M3	Speaker always off **Speaker on until carrier detected** Speaker always on Speaker on during answering only
N0 **N1**	Disable auto-mode. This forces the modem to connect at the speed specified in register S37. **Enable auto-mode. The modem will answer at the highest available line speed and ignore any ATBn command.**
O0 O1	Return to data mode. If you have entered the command mode using the time-independent escape sequence, this will put you back in data mode without going on-hook. Retrain the modem. If the line condition has changed since the original connection, retraining the modem will cause it to reconnect at the most efficient speed for the current line condition.
P	Pulse dialing allows the modem to work on telephone networks where tone is not supported.
Q0 Q1	**Enable response to DTE.** Disable response to DTE. The modem does not respond to the terminal. Issuing a command will not produce a response (unless the command is something like ATZ, which will restore this setting to default.)
Sn	Set default S-register. Any subsequent = or ? commands will modify the default S register.
Sn=m	Set register n to value m
T	**Tone dialing**
V0 **V1**	Result codes will be sent in numeric form. (See the result code table) **Result codes will be sent in word form. (See the result code table)**
W0 W1 W2	**Report DTE speed only. After connection, there will be no message about what Error Correction or Data Compression protocol is in use.** Report DCE speed, Error Correction/Data Compression protocol, and DTE speed. Report DCE speed only.
X0 X1 X2 X3 **X4**	Send OK, CONNECT, RING, NO CARRIER, ERROR, and NO ANSWER. Busy and Dial Tone Detection are disabled. Send X0 messages and CONNECT speed. Send X1 message and NO DIAL TONE. Send X2 messages except NO DIAL TONE, BUSY, and RING BACK **Send all responses**

AT COMMAND SET (Cont'd)

Command	Function
Y0 Y1	**Disable long space disconnect** Enable long space disonnect; with error correction, hang up after sending 1.6-second long space; without error correction, hang up after 4-second long space.
Z0 Z1	Reset modem to profile 0 Reset modem to profile 1
=n	**Sets the value of the default S register**
?	**Reports the value stored in the default S register**
&C0 &C1	**Force DCD on** DCD follows remote carrier
&D0 &D1 &D2 &D3	**DTR is assumed on** DTR drop causes modem back to command mode without disconnecting DTR drop causes modem to hang up DTR drop causes modem to be initialized; &Y determines which profile is loaded.
&F	Load factory profile
&G0 &G1 &G2	**Disable guard tone** Enable 550-Hz guard tone Enable 1800-Hz guard tone on answering modem
&K0 **&K3** &K4 &K5 &K6	Disable flow control **Enable RTS/CTS flow control** Enable XON/XOFF flow control Enable transparent software flow control Enable both RTS/CTS and XON/XOFF flow control
&P0 &P1 &P2 &P3	**Selects 39%-61% make/break ratio at 10 pulses per second** Selects 33%-67% make/break ratio at 10 pulses per second Selects 39%-61% make/break ratio at 20 pulses per second Selects 33%-67% make/break ratio at 20 pulses per second
&S0 &S1	**Force DSR on** DSR on at the start of handshaking and off after carrier loss
&T0 &T1	Terminate test Start ALB test
&U0 &U1	**Enable trellis coding** Disable trellis coding
&V0 &V1 &V2	Display active profile Display stored profiles Display stored telephone numbers
&W0 &W1	Save active profile to profile 0 Save active profile to profile 1
&Y0 &Y1	**Use profile 0 on power up** Use profile 1 on power up

AT COMMAND SET (Cont'd)

Command	Function
&Zn=m	Save telephone number (up to 36 digits) into memory location n (0-9)
%	Percent Commands
%C0	Disable data compression
%C1	Enable MNP5 compression
%C2	Enable V.42bis compression
%C3	**Enable both V.42bis and MNP5**
%E0	Disable auto-retain
%E1	Enable auto-retain
%E2	**Enable auto-retrain and fallback**
%E3	Enable auto-retrain and fast hang up
%N0	Dynamic CPU loading disabled
%N1	Dynamic CPU loading not to exceed 10%
%N2	Dynamic CPU loading not to exceed 20%
%N3	Dynamic CPU loading not to exceed 30%
%N4	Dynamic CPU loading not to exceed 40%
%N5	Dynamic CPU loading not to exceed 50%
%N6	Dynamic CPU loading not to exceed 60%
%N7	**Dynamic CPU loading not to exceed 70%**
%N8	Dynamic CPU loading not to exceed 80%
%N9	Dynamic CPU loading not to exceed 90%
%Q	Report line signal quality
\	Backslash Commands
\A0	64-character max. MNP block size
\A1	**128-character max. MNP block size**
\A2	192-character max. MNP block size
\A3	256-character max. MNP block size
\Bn	In non-error correction mode, transmit break in 100ms units (1-9 with default 3)
\G0	**Disable XON/XOFF flow control (modem to modem)**
\G1	Enable XON/XOFF flow control (modem to modem)
\Kn	Define break type
\L0	**Use stream mode for MNP**
\L1	Use interactive block mode for MNP
\N0	Normal mode; speed control without error correction
\N1	Plain mode; no speed control and no error correction
\N2	Reliable mode
\N3	**Auto-reliable mode**
\N4	LAPM error correction only
\N5	MNP error correction only
***Q0**	**Send the "CONNECT xxxx" result codes to the DTE when an invalid TIES escape sequence is detected after the "OK" response has already been sent.**
*Q1	Does NOT send the "CONNECT xxxx" result codes to the DTE when an invalid TIES escape sequence is detected after the "OK" response has already been sent.

A.5 AT/Kn COMMAND SET

\Kn	Local DTE send break during normal or reliable mode	Local modem sends break during plain mode	Remote modem sends break during normal mode
\K0	Enter command state; no break or remote	Break to remote; and enter command state	Empty data buffers; and send break to DTE
\K1	Empty data buffers; break to remote	Same as\K0	Same as\K0
\K2	Same as\K0	Send break to remote	Immediately send break to DTE
\K3	Immediately send break to remote	Same as\K0	Same as\K2
\K4	Same as\K0	Same as\K2	Send break to DTE with buffered RXD data
\K5	Send break to remote with TXD data	Same as\K2	Same as\K4

A.6 RESULTS CODES

Long Form	Short Form	Description
OK	0	Modem successfully executed an AT command
CONNECT	1	A connection established
RING	2	Modem detected an incoming call
NO CARRIER	3	Modem lost or could not detect a remote carrier signal within the register S7 time
ERROR	4	Modem detected an error in an AT command
CONNECT 1200	5	Connection at 1200 bps
NO DIALTONE	6	Modem did not detect a dial tone within 5 seconds after off-hook
BUSY	7	Modem detected a busy tone
NO ANSWER	8	Modem did not detect 5 seconds of silence when using the @ dial modifier in the dial command
CONNECT 0600	9	Connection at 600 bps
CONNECT 2400	10	Connection at 2400 bps
CONNECT 4800	11	Connection at 4800 bps
CONNECT 9600	12	Connection at 9600 bps
CONNECT 7200	13	Connection at 7200 bps
CONNECT 12000	14	Connection at 12000 bps
CONNECT 14400	15	Connection at 14400 bps

RESULTS CODES (Cont'd)

Long Form	Short Form	Description
CONNECT 19200	16	Connection to 19200 bps
CONNECT 38400	17	Connection to 38400 bps
CONNECT 57600	18	Connection to 57600 bps
CONNECT 115200	19	Connection to 115200 bps
CONNECT 28800	20	Connection to 28800 bps
CONNECT 300	21	Connection to 300 bps
CONNECT 1200TX/75RX	22	Connection to transmit 1200/receive 75 bps
CONNECT 75TX/1200RX	23	Connection to transmit 75/receive 1200 bps
CONNECT 110	24	Connection to 110 bps
RING BACK	25	Ring Back signal detected
+FCERROR	+F4	Error occurred in Class 1 fax operation
FAX	33	Fax modem connection established
DATA	35	Data modem connection established
CARRIER 300	40	Carrier rate or 300 bps
CARRIER 1200/75	44	Carrier rate of transmit 1200/receive 75 bps
CARRIER 75/1200	45	Carrier rate of transmit 75/receive 1200 bps
CARRIER 1200	46	Carrier rate of 1200 bps
CARRIER 2400	47	Carrier rate of 2400 bps
CARRIER 4800	48	Carrier rate of 4800 bps
CARRIER 7200	49	Carrier rate of 7200 bps
CARRIER 9600	50	Carrier rate of 9600 bps
CARRIER 12000	51	Carrier rate of 12000 bps
CARRIER 14400	52	Carrier rate of 14400 bps
CARRIER 16800	53	Carrier rate of 16800 bps
CARRIER 19200	54	Carrier rate of 19200 bps
CARRIER 21600	55	Carrier rate of 21600 bps
CARRIER 24000	56	Carrier rate of 24000 bps
CARRIER 26400	57	Carrier rate of 26400 bps
COMPRESSION: CLASS 5	58	MNP Class 5 data compression connection established

RESULTS CODES (Cont'd)

Long Form	Short Form	Description
CONNECT 16800	59	Connection at 16800 bps
CONNECT 21600	61	Connection at 21600 bps
CONNECT 24000	62	Connection at 24000 bps
CONNECT 26400	63	Connection at 26400 bps
COMPRESSION: CLASS 5	66	MNP Class 5 data compression connection established
COMPRESSION: V.42bis	67	V.42bis data compression connection established
COMPRESSION: NONE	69	Connection established without data compression
PROTOCOL: NONE	76	Connection established without error correction
PROTOCOL: LAPM	77	V.42/LAPM error correction connection established
PROTOCOL: ALT	80	MNP 3-4 error correction connection established
CARRIER 31200	90	Carrier rate of 31200 bps
CARRIER 33600	91	Carrier rate of 33600 bps
CONNECT 31200	95	Connection at 31200 bps
CONNECT 33600	96	Connection at 33600 bps

A.7 S REGISTERS

Register	Function
0	**Rings to auto-answer** Set the number of rings required before the modem answers. 0 setting disables auto-answer. Range: 0 - 255 rings Default: **0** (auto-answer disabled)
1	**Ring counter** Count the number of rings before the modem answers. Range 0 -255 rings Default: **0**
2	**Escape character** Define the character used for the three-characer escape code sequence. 0 setting disables the escape code character. Range 0 -127 Default: **43** (+)
3	**Carriage return character** Define the character for carriage return Range 0 - 127 Default: **13** (carriage return)

S REGISTERS (Cont'd)

Register	Function
4	**Line feed character** Define the character for line feed. Range 0 -127 Default: **10** (line feed)
5	**Backspace character** Define the character for backspace. Range 0 -127 Default: **8** (backspace)
6	**Wait before dialing** Set the length of time to pause after off hook before dial. Range 2 - 255 seconds Default: **2** seconds
7	**Wait for carrier after dial** Set the length of time that the modem waits for a carrier from the remote modem before hanging up. Range 1- 255 seconds. Default: **50** seconds
8	**Pause time for dial delay** Set the length of time to pause for the pause dial modifier ",". Range 0 - 255 seconds Default: **2** seconds
9	**Carrier detect response time** Define the length of time a signal is detected and qualified as a carrier. Range: 1 - 255 tenths of a second Default: Default **6** (0.6 second)
10	**Lost carrier hang up delay** Set the length of time the modem waits before hanging up for a carrier loss. Range: 1 - 255 tenths of a second Default: **14** (6 seconds)
11	**DTMF speed control** Set the length of tone and the time between tones for the tone dialing. Range: 50 - 255 milliseconds Default: **95** milliseconds
12	**Escape Prompt Delay (EPD) timer** Set the time from detection of the last character of the three character escape sequence until the "OK" is returned to the DTE Range: 0 -255 fiftieths of a second Default: **50** (1 second)
13	Reserved
14	Reserved
15	Reserved
16	Reserved
17	Reserved

S REGISTERS (Cont'd)

Register	Function
18	**Test timer** Set the length of loopback test. Range: 0 - 255 seconds Default: **0** (disable timer)
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	**Delay to DTR** Set the length of time the modem ignores DTR before hanging up. Range: 0 - 255 hundredths of a second Default: **5** (0.05 second)
26	Reserved
27	Reserved
28	Reserved
30	**Disconnect inactivity timer** Set the length of time allowed for inactivity before the connection is hung up. Range: 0 - 255 in 10 seconds Default: **0** (disabled)
32	**XON character** Set the value of XON character. Range: 0 - 255 Default: **17**
33	**XOFF character** Set the value of XOFF character. Range: 0 - 255 Default: **19**
34	**V.34 data rate (bit-rate)** Set the maximum bit rate for V.34 Range: 0 - 8 (2400 baud) 1-10 (3000 baud) 1-11 (3200 baud) 1-13 (3429 baud) bit rate = ((S34)+1) * 2400 bps Default: **13** (33600 bps)

S REGISTERS (Cont'd)

Register	Function
35	**V.34 symbol rate (baud-rate)** Set the maximum baud rate for V.34 Range: 0 - 5 0 - 2400 baud 1 - 2743 baud (N/A) 2 - 2800 baud (N/A) 3 - 3000 baud 4 - 3200 baud 5 - 3429 baud (N/A until V.34bis) Default: **0** (2400 baud)
36	Reserved
37	**Line connection speed** 0 - Attempt to connect at the highest speed 3 - Attempt to connect at 300 bps 4 - Attempt to connect at 1200 bps 6 - Attempt to connect at 2400 bps 7 - Attempt to connect at 4800 bps 8 - Attempt to connect at 7200 bps 9 - Attempt to connect at 9600 bps 10 - Attempt to connect at 12000 bps 11 - Attempt to connect at 14400 bps 12 - Attempt to connect at V.34 Default: **0**
38	**Delay before forced hang up** Set the delay to hang up after the disconnecting command is received. Range: 0 - 255 seconds Default: **20** seconds
39	Reserved
40	Reserved
41	Reserved
42	Reserved
43	Reserved
44	Reserved
45	Reserved
46	Reserved
47	Reserved
48	Reserved
82	Reserved

S REGISTERS (Cont'd)

Register	Function
86	**Call failure reason code** 0 - Normal disconnect; no error 4 - Loss of carrier 5 - V.42 negotiation failed to detect an error correction modem at remote end 6 - No response to complete negotation 9 - No common protocol 12 - Remote initiated a normal disconnect 13 - Remote modem did not respond after 10 message retransmissions 14 - Protocol violation 15 - Compression failure 20 - Hang up by inactivity time out
91	**Transmit level** Set the transmit level in -dBm. Range: 0 - 15 (-dBm) Default: **11** (-11 dBm)

A.8 FAX CLASS 1 COMMAND SET

Fax Class 1 Command Set:

Command	Function
+FCLASS=0 +FCLASS=1	**Select data mode** Select facsimile Class 1 mode
+FAE?	Report active adaptive answer setting: 0 for disabled; 1 for enabled
+FAE=?	Report adaptive answer capability
+FAE=0 +FAE=1	**Disable adaptive answer** Enable adaptive answer
+FCLASS=?	Report service classes supported
+FTS=n	Stop transmission and pause, 0-255 in 10 ms
+FRS=n	Wait for silence, 0-255 in 10 ms
+FTM=?	Report Class 1 transmit capabilities
+FRM=?	Report Class 1 receive capabilities
+FTH=n	Transmit data with carrier n, n=3, 24, 48, 72, 73, 74, 96, 97, 98, 121, 122, 145, 146
+FRH=n	Receive data with carrier n, n=3, 24, 48, 72, 73, 74, 96, 97, 98, 121, 122, 145, 146

Oak Class 8 (Voice Mode) AT Commands Summary:

Command	Function
ATA	Answering in voice mail
ATD	Dial command in voice mode
ATH	Hang up in voice mode
ATZ	Reset from voice mode
AT#BDR	Select baud rate (turn off autobaud)
AT#CID	Enable Caller ID detection and select reporting format
AT#CLS	Select data, fax, or voice
AT#MDL?	Identify model
AT#MFR?	Identify manufacturer
AT#TL	Transmit level control
AT#REV?	Identify revision level
AT#RG	Record gain control
AT#SPK	Change the setting of speakerphone
AT#VBS	Bits per sample (ADPCM)
AT#VBT	Beep tone timer
AT#VLS	Voice line select (ADPCM)
AT#VRA	Ringback goes away timer (originate)
AT#VRX	Voice Receive Mode (ADPCM)
AT#VSD	Silence deletion tuner (voice receive, ADPCM)
AT#VSP	Silence detection period (voice receive, ADPCM)
AT#VSS	Silence sensitivity tuner (voice receive)
AT#VTX	Voice Transmit Mode (ADPCM)
AT#VBQ?	Query buffer size
AT#VCI?	Identify compression method (ADPCM)
AT#VRN	Ringback never came timer (originate)
AT#VSK	Buffer skid setting
AT#VSR	Sampling rate selection (ADPCM)
AT#VTD	DTMF/tone reporting capability
AT#VTS	Play tone string (online voice command)

A.9 CALL PROGRESS

The table below shows Call Progress codes sent to the Data Terminal Equipment (DTE).

Code Sent to DTE	Meaning
<DLE>0 to <DLE>9, <DLE>*, <DLE>#, <DLE>A to <DLE>D	**DTMF** Digits 0 through 9, *, #, or A through D detected by the modem.
<DLE>a	**Answer Tone (CCITT)** Send to the DTE when the V.25/T.30 2100-Hz Answer Tone (Data or Fax) is detected. If the DTE fails to react to the code, and the modem continues to detect Answer tone, the code is repeated as often as once every 0.5 seconds.
<DLE>b	**Busy** Send to DTE when the busy cadence is detected. The modem sends the busy <DLE>b code every 4 seconds if busy continues to be detected and the DTE does not react. This allows the DTE the flexibility of ignoring what could be a false busy detection.
<DLE>c	**Calling Tone** Send when the T.30 1100-Hz Calling Tone (Fax Modem) is detected. The modem assumes the calling tone is valid and sends this code only after 4 seconds of proper cadence has been detected. If the DTE does not react to this code, the code is repeated as often as once every 4 seconds.
<DLE>d	**Dial Tone** Sent in Voice Receive Mode when dial tone is detected after any remaining data in the voice receive buffer. The modem sends this code every 3 seconds if dial tone continues to be detected and the DTE does not react. This allows the DTE the flexibility of ignoring what could be a false dial tone detection.
<DLE>e	**European Data Modem Calling Tone** Send when the V.25 1300-Hz Calling Tone (Data Modem) is detected. The modem assumes that the calling tone is valid, and sends this code only after 4 seconds or proper cadence has been detected. If the DTE does not react to the code and the modem continues, the code is sent again as often as once every 4 seconds.
<DLE>f	**Bell Answer Tone** Sent when Bell 2225-Hz Answer Tone (Data) is detected. If the DTE fails to react to the code and the modem continues to detect Answer tone, the code is repeated as often as every 0.5 seconds.
<DLE>h	**Hung Up Handset** Sent immediately when the modem detects that the local handset has hung up.
<DLE>q	**Quiet** Sent in Voice Receive Mode after any remaining data in the receive voice buffer when the silence detection timer (#VSP) expires and the voice data has been passed to the DTE.
<DLE>s	**Silence** Sent in Voice Receive Mode after the silence detection timer (#VSP) expires and if valid voice has not been detected (#VSS).
<DLE>t	**Handset Off-Hook** Sent one time when the local handset transition goes off-hook.
<DLE><ETX>	**End of Stream** This code is sent to denote the end of a voice data stream.

The table below shows Call Progress codes sent to the modem.

Code Sent to Modem	Meaning
<DLE><ETX>	**Terminate** Sent during Voice Transmit Mode to indicate that the DTE has finished transmitting a voice message. The Modem complete transmission of any remaining data in the voice transmit buffer before responding with the VCON message and entering Online Voice Command Mode.
<DLE><CAN>	**Cancel** Sent during Voice Transmit Mode to indicate that the DTE has finished transmitting a voice message and wants the modem to discard any remaining data in the voice transmit buffer. The modem immediately purges its buffer, and then responds with the VCON message entering Online Voice Command Mode.
<DLE>p	**Pause** Send during Voice Transmit Mode to force the modem to suspend sending voice data to the selected output device. Any data currently in the voice transmit buffer is saved until either a resume (<DLE>r) or cancel (<DLE><CAN>) is received, in which case the data is lost. If a <DLE><ETX> is received during the paused state, the modem processes it normally, and also automatically resumes transmission of the data left in the buffer (appended with <DLE><ETX>). Any other data received from the DTE while in this paused state is placed in the transmit buffer according to available space, with flow control active.
<DLE>r	**Resume** Sent during Voice Transmit Mode to force the modem to resume sending voice data to the selected output device. Any data currently in the voice transmit buffer is now played.

A.10 AT VOICE COMMAND DESCRIPTIONS

ATA - Answering in Voice
This command works similarly to the way it works in Data and Fax Modes.
Result Code:
VCON

ATD - Dial Command in Voice
This command will perform the dial action in Voice Mode.
Result Codes:
VCON - Issued in Voice Mode when the modem determines that the remote modem or handset has gone off-hook.
NO ANSWER - Issues in Voice Mode when the modem determines that the remote has not picked up the line before the S7 timer expires.

ATH - Hang Up in Voice
This command works the same as in Data and Fax modes by hanging up the phone line.
1. This command forces the #CLS=0, but does not destroy any of the voice parameter settings such as #VBS, #VSP, etc.
2. The #BDR setting is forced back to 0.

ATZ - Reset from Voice Mode
This command works the same as in Data and Fax modes. In addition, it will also reset all voice related parameters to default states, force the #BDR=0 condition, and force the telephone line to be selected with the handset on-hook.

#BDR - Select Baud Rate (Turn Off Autobaud)
This command selects a specific DTE/modem baud rate.
Parameters: n = 0 - 48 (Baud Rate = n * 2400 bps)
Default: 0
Result Codes:

OK	if n is between 0 and 48
ERROR	Otherwise

Command options:

#BDR?	Return the current setting
#BDR=?	Return a message indicating the speeds that are supported
#BDR=0	Enable autobaud detection on the DTE interface
#BDR=n	Select the baud rate

#CID - Enable Caller ID Detection and Select Reporting Format
This command enables or disables Caller ID recognition and reporting in any mode.
Parameters: n = 0, 1, or 2
Default: 0
Result Codes:

OK	n = 0, 1, or 2
ERROR	Otherwise

Command Options:

#CID?	Return the current setting (0, 1, or 2)
#CID=?	Return the message, "0-2"
#CID=0	Disables Caller ID
#CID=1	Enable formatted Caller ID reporting of SDM (single data message) and MDM (multiple data message) packets.
#CID=2	Enable unformatted Caller ID reporting

#CLS - Select Data, Fax, or Voice
This command selects Data, Fax, or Voice Mode
Parameters: n=0, 1, 2, or 8
Default: 0
Result Codes:

OK	if n = 0, 1, 2, or 8
ERROR	Otherwise

Command options:

#CLS?	Return the current setting (0, 1, 2, or 8)
#CLS=?	Return the message, "0, 1, 2, 8"
#CLS=0	Select Data Mode
#CLS=1	Select Class 1 Fax Mode
#CLS=2	Select Class 2 Fax Mode
#CLS=8	Select Voice Mode

#MDL - Identify Model
This command identifies the model number of the modem.
Command option:

#MDL?	"OAK288DFV"

#MFR? - Identify Manufacturer
This command identifies the modem manufacturer.
Command option:

#MFR?	"Oak Technology"

#REV? - Request Revision Level
This command requests the revision number of Oak driver.

#REV?	"Oak 2.00"

#RG - Record Gain Control
This command sets the record gain.
Parameters: n = 0000 - 7FFF
Default: 7FFF
Result Codes:

OK	if n = 0000 - 7FFF
ERROR	Otherwise

Command options:

#RG?	Return the current setting
#RG=?	Return the message, "0000-7FFF"
#RG=n	Set the record gain to n

#SPK - Change the setting of Speakerphone
This command set the parameters for the speakerphone.
Parameters: #SPK=<mute>, <spk>, <mic>

<mute> 0 - microphone mute
1 - microphone on (default)
2 - Room Monitor mode (mic on max. AGC, speaker off)

<spk> Speaker Output Level
Range: 0 to 15 (speaker attenuation in 2 dB steps)
Default: 5 (10 dB attenuation)
Speaker mute is achieved by a value of 16

<mic> 0 - 0 dB
1 - 6 dB gain (default)
2 - 9.5 dB gain
3 - 12 dB gain

Command options:
It is not necessary to enter all three parameters,
#SPK=,<spk>,<mic>
#SPK=,,<mic>

#TL - Transmit Level Control
This command sets the transmit level.
Parameters: n = 0000 - 7FFF
Default: 3FFF
Result Codes:

OK	if n = 0000 - 7FFF
ERROR	Otherwise

Command options:

#TL?	Return the current setting
#TL=?	Return the message, "0000-7FFF"
#TL=n	Set the record gain to n

#VBQ? - Query Buffer Size
This command queries the modem's voice transmit and voice receive buffers size.
Parameters: None
Command option:

#VBQ?	Return the size of buffers.

#VBS - Bits Per Sample (Compression Factor)
This command selects the degree of ADPCM voice compression to be used.
Parameters: n = 4 (Only 4 bits per sample compression ratio is supported)
Default: 4
Result Codes:

OK	if n = 4
ERROR	Otherwise

Command options:

#VBS?	Return the current setting
#VBS=?	Return "4"
#VBS=4	Selects 4 bits per samples

#VBT - Beep Tone Timer
This command sets the duration for DTMF tone generation.
Parameters: n = 0 - 40 (duration = n /10 seconds)
Default: 10
Result Codes:

OK	if n = 0 - 40
ERROR	Otherwise

Command options:

#VBT?	Return the current setting
#VBT=?	Returns the message, "0-40"
#VBT=0	Disables the tone generation capability
#VBT=n	Sets tone duration

#VCI? - Identify Compression Method
This command identifies the compression method used by the modem.
Parameter: None
Command option:

#VCI?	Returns the message, "Oak;ADPCM;32"

#VLS - Voice Device Selection
This command selects which devices is routed through the modem.
Parameter: n = 0, 1, 2, 3, 4, or 6
Default: 0
Result Codes:

OK	if n = 0, 1, 2, 3, 4, or 6
ERROR	Otherwise

Command options:

#VLS?	Return current setting
#VLS=?	Return the device types supported by the modem
#VLS=n	Select Device Type
	0 Phone Line with Telephone handset
	1 Handset
	2 On-Board Speaker
	3 Microphone
	4 Telephone line with on-board speaker ON and handset
	6 Speaker Phone

#VRA - Ringback Goes Away Timer (Originate)
When originating a voice call, this command can set the "Ringback Goes Away" timer value, an amount of time measured from when the ringback cadence stops once detected. If ringback is not detected within this period, the modem assumes that the remote has picked up the line and switches to Online Voice Command Mode. Every time a ringback cadence is detected, this timer is reset.
Parameters: n = 0 - 255 (0 - 2.55 seconds)
Default: 70
Result Codes:

OK	if n = 0 - 255
ERROR	Otherwise

Command options:

#VRA?	Return the current setting
#VRA=?	Return the message, "0-255"
#VRA=0	Turn off the timer. The dialing modem sends VCON and enters Online Voice Command Mode after one ringback.
#VRA=n	Set the timer (timer = n * 0.01 seconds)

#VRN - Ringback Never Came Timer (Originate)
When originating a voice call, this command sets the "Ringback Never Came" timer value, an amount of time measured from completion of dialing. If a ringback is not detected within this period, the modem assumes the remote has picked up the line and switches to Online Voice Command Mode.
Parameters: n = 0 - 255 (0 - 2.55 seconds)
Result Codes:

OK	if n = 0 - 255
ERROR	Otherwise

Command option:

#VRN?	Return the current setting
#VRN=?	Return the message, "0-255"
#VRN=0	Turn off the "Ringback Never Came timer." After dialing, the modem sends VCON and enters Online Voice Command Mode immediately.
#VRN=n	Set the timer (duration = n * 0.01 second)

#VRX - Voice Receive
This command sets the modem in Voice Receive Mode.
Parameters: None
Result Codes:

CONNECT	When voice transfer from modem to DTE can begin
ERROR	if #VLS=0 and not connected to any input device

#VSD - Silence Deletion Tuner (Voice Receive)
This command can enable/disable Voice Receive Mode silence detection. Silence Deletion is not supported in Oak HSP Modem.
Parameters: n = 0
Default: 0
Result Codes:

OK	if n = 0
ERROR	Otherwise

Command options:

#VSD?	Return current setting
#VSD=?	Return the message, "0"
#VSD=0	Disable Silence Deletion

#VSK - Buffer Skid Setting
This command queries and sets the number of bytes of spare space, after the XOFF threshold is reached, in the modem's buffer during Voice Transmit Mode. This equates to the "skid" spare buffer space, or the amount of data the DTE can continue to send after being told to stop sending data by the modem, before the modem voice transmit buffer overflows.
Parameters: n = 0 - 255
Default: 255
Result Code:

OK	if n = 0 - 255
ERROR	Otherwise

Command options:

#VSK?	Return the current setting
#VSK=?	Return the message, "0-255"
#VSK=n	Set the skid buffer size to n bytes

#VSP - Silence Detection Period (Voice Receive)
This command sets the Voice Receive Mode silence detection period value. If the modem does not receive any ADPCM data after the timer expired, it will cause the modem to send <DLE>s or <DLE>q codes.
Parameters: n = 0 - 255 (0 - 25.5 seconds)
Default: 55
Result Code:

OK	if n = 0 - 255
ERROR	Otherwise

Command options:

#VSP?	Return current setting
#VSP=?	Return the message, "0-255"
#VSP=0	Disable the silence period detection timer
#VSP=n	timer = n * 0.1 second

#VSR - Sampling Rate Selection
This command sets the audio codec sampling rate.
Parameters: n = 8000 (8000 Hz sampling rate)
Default: 8000
Result Codes:

OK	if n = 8000
ERROR	Otherwise

Command options:

#VSR?	Return the current setting
#VSR=?	Return the message, "8000"
#VSR=8000	Set the sample rate to 8000

#VSS - Silence Sensitivity Tuner (Voice Receive)
This command sets the sensitivity in Voice Receive Mode silence detection.
Parameters: n = 0 - 3
Default: 2
Result Codes:

OK	if n = 0 - 3
ERROR	Otherwise

Command options:

#VSS?	Return current setting
#VSS=?	Return the message, "0-3"
#VSS=0	Disable silence detection by the modem in Voice Receive Mode
#VSS=1	Least sensitive setting
#VSS=2	Medium sensitive setting
#VSS=3	Most sensitive setting

#VTD - Tone Reporting Capability
This command sets which types of tones can be detected and reported to the DTE via shielded codes in Voice Transmit, Voice Receive, and Online Voice Command Modes.
Parameters: i, j, k
Default: 3F, 3F, 3F
Result Codes:

OK	If settings are supported by the modem
ERROR	Otherwise

Command options:

#VTD?	Return current setting
#VTD=?	Returns the tone reporting capabilities of the modem.
#VTD=i,j,k	Where i, j, k corresponds to the desired capabilities (see table below), i for Voice Transmit, j for Voice Receive, and k for Online Voice Command Modes.

Bit	Description
0	0/1 = Disable/Enable DTMF tone capability
1	0/1 = Disable/Enable V.25 1300-Hz Calling tone capability
2	0/1 = Disable/Enable V.30 1100-Hz Facsimile Calling tone capability
3	0/1 = Disable/Enable V.25/T.30 2100-Hz Answer tone capability
4	0/1 = Disable/Enable 2225-Hz Answer tone capability
5	0/1 = Disable/Enable call progress tone and cadence tone capability

#VTS - Play Tone String (Online Voice Command Mode)
This command can play one or more DTMF or other tones. No key abort is allowed.
Dual or Single Tones: These are represented by a substring enclosed in square brackets ("[ ]") within the parameter. Each such sub-string consists of three subelements corresponding to two frequencies in Hertz (0, or 2000-3000) and a duration (ASCII decimal in units of 100ms).
Varying DTMF Digits: This is represented by a substring enclosed in curly braces ("{ }") within the parameter. Each such sub-string consists of two subelements corresponding to a DTMF digits (0-9, A-D, *, #), and alternate duration in units of 100ms.
Parameters: The tone generation consists of elements in a list with each element separated by commas.
Result Codes:

OK	Command to play tones on currently selected device is accepted.
ERROR	Command was not issued in Online Voice Command Mode or string is grammatically incorrect.

#VTX - Voice Transmit
This command sets the modem in Voice Transmit Mode. The #VLS command should have been previously issued correctly.
Parameters: None
Result Codes:

CONNECT	When voice transmission by DTE can begin.
ERROR	If #VLS=0 and output device is not connected.

A.11 %P - PTT TESTING UTILITIES

This facility testing of signal levels provides a continuous signal when the modem is in IDLE mode. This allows the user to initiate a series of signal that are necessary for PTT approval. These signals are answer tone, carriers, modulation, and other pertinent signals. A selected test will be terminated when any keyboard character is entered. The following are command descriptions.

Note: For DTMF, the transmit level is -10dBm for low band and -8dBm for high band; inter-digit delay is fixed at 70ms. All other transmit level is adjustable according to the setting of register S91 (from -10 to -15dBm). Speaker control initiates by command ATLn.

%P00 - %P09	DTMF tone digits from 0 to 9.
%P10	DTMF digit A.
%P11	DTMF digit B.
%P12	DTMF digit C.
%P13	DTMF digit D.
%P14	DTMF digit *.
%P15	DTMF digit #.
%P16	V.21 Channel 1 mark 980 Hz.
%P17	V.21 Channel 2 mark 1650 Hz.
%P18	V.23 Reversed channel mark 390 Hz.
%P19	V.23 Forward channel mark 1300 Hz.
%P20	V.22 Originate.
%P21	V.22bis originate.
%P22	V.22 Answer.
%P23	V.22bis Answer.
%P24	V.21 Channel 1 space 1180 Hz.
%P25	V.21 Channel 2 space 1850 Hz.
%P26	V.23 Reversed channel space 450 Hz.
%P27	V.23 Forward channel space 2100 Hz.
%P28	V.32 at 9600 bps.
%P29	V.32bis 14400 bps.
%P30	Silence, off-hook.
%P31	V.25 Answer tone 2100 Hz.
%P32	Guard tone 1800 Hz.
%P33	V.25 Calling tone 1300 Hz.
%P34	Fax calling tone 1100 Hz.
%P35	V.21 Channel 2 1650 Hz.
%P36	V.27ter 2400 bps.
%P37	V.27ter 4800 bps.
%P38	V.29 7200 bps.
%P39	V.29 9600 bps.
%P40	V.17 7200 bps long train.
%P41	V.17 7200 bps short train.
%P42	V.17 9600 bps long train..
%P43	V.17 9600 bps short train.
%P44	V.17 12000 bps long train.
%P45	V.17 12000 bps short train.
%P46	V.17 14400 bps long train.
%P47	V.17 14400 bps short train.
%P48	V.34, 2400 bps modulation.
%P49	V.34, 4800 bps modulation.
%P50	V.34, 7200 bps modulation.

%P51	V.34, 9600 bps modulation.
%P52	V.34, 12000 bps modulation.
%P53	V.34, 14400 bps modulation.
%P54	V.34, 16800 bps modulation.
%P55	V.34, 19200 bps modulation.
%P56	V.34, 21600 bps modulation.
%P57	V.34, 24000 bps modulation.
%P58	V.34, 26400 bps modulation.
%P59	V.34, 28800 bps modulation.
%P60	V.32bis 9600 bps modulation.
%P61	V.32bis 12000 bps modulation.
%P62	Bell 212A originate 1200 bps
%P63	Bell 212A answer 1200 bps
%P64	Bell 103 originate mark 1270 Hz
%P65	Bell 103 originate space 1070 Hz
%P66	Bell 103 answer mark 2225 Hz
%P67	Bell 103 answer space 2025 Hz

%P99,n

where 0<= n <=23

f(Hz) = n * (150Hz)

n	f(Hz)	
0	0	modem goes off hook and reports power level of incoming signal if present
1	150	
2	300	
3	450	
4	600	
5	750	
6	900	
7	1050	
8	1200	
9	1350	
10	1500	
11	1650	
12	1800	
13	1950	
14	2100	
15	2250	
16	2400	
17	2550	
18	2700	
19	2850	
20	3000	
21	3150	
22	3300	
23	3450	

%I or %I? Country Code Selection and Identification

This command provides the ability of selection the desired country telephony Central Office. When the selection is correct, a set of the selected country parameters will be loaded for the current operation.

Command format : **AT%In**

Country	n	Comment
USA	1	Factory default
France	2	
Germany	3	
Italy	4	
Sweden	5	
UK	6	
Japan	7	
Australia	8	
Spain	9	
Taiwan	10	
Singapore	11	
Korea	12	
Switzerland	13	
Norway	14	
Netherlands	15	
Belgium	16	
Canada	17	
Ireland	18	
Portugal	19	
Poland	20	
Hungary	21	
Finland	22	
Denmark	23	

Result Codes:

OK	If correct selection.
ERROR	Otherwise.

Command format: **AT%I?**

Result Codes:

country name CO	(Central Office)
ERROR	Otherwise.

APPENDIX B HOST SIGNAL PROCESSING (HSP) BASED WAVETABLE SYNTHESIZER

The OTI-610 and OTI-611 provide the user with two wavetable synthesizer options: 1) DSP-based with external 2MB ROM which contains the General MIDI (GM) sample set, or 2) an HSP-based software wavetable synthesizer wherein the synthesizer engine and GM sample set are contained in system memory. This appendix discusses the HSP-based wavetable synthesizer.

B.1 HSP WAVETABLE SYNTHESIZER SPECIFICATIONS

- Extensible, professional-quality software synthesizer up to 32-voice polyphony
- Full 16 MIDI channel multi-timbral support
- Complete GM sample set
- Programmable reverb and chorus effects control
- Supports downloadable samples to extend instrument options beyond General MIDI
- User-selectable maximum RAM cache, CPU utilization, and number of allowable voices
- Intelligent scaling and dynamic buffering to minimize CPU utilization
- Real-time instrument selection changes when used with CyberSound Keyboard application
- Works with standard Windows 95 software sequencers (Cakewalk, Voyetra, etc.)

Minimum System Recommendations		
	OTI-611 Environment	**OTI-610 Environment**
Operating System	Windows 95	Windows 95
CPU	166-MHz Pentium class 166-MHz Pentium MMX class	133-MHz Pentium class 166-MHz Pentium MMX class
Total System RAM	12 Megabytes	12 Megabytes
Free Hard Disk Space	5.0 Megabytes	5.0 Megabytes

B.2 HSP WAVETABLE SYNTHESIZER DESCRIPTION

The OTI-610 and OTI-611 use an HSP-based wavetable synthesizer and General MIDI sample set known as CyberSound GM. CyberSound GM is a programmable General MIDI synthesizer implemented in software for Windows 95. CyberSound GM for the OTI-610 and OTI-611 is available in two code versions supporting either Pentium class or Pentium MMX class CPUs.

CyberSound GM offers all of the functionality of a stand-alone General MIDI module or wavetable synthesizer on a PC sound card. CyberSound GM provides programmable effects processing and customizable system performance settings and monitoring. Coupled with CyberSound Keyboard, the user has a complete, high-quality, MIDI controllable, wavetable synthesizer for music playback at significantly lower cost.

CyberSound GM utilizes both traditional and revolutionary music synthesis techniques — digital and analog synthesis, wavetable sounds, and physical modeling.

B.3 GENERAL MIDI DESCRIPTION

The General MIDI Specification, published by the International MIDI Association, defines a set of general capabilities for GM Instruments. The GM Specification includes the definition of a GM sound set (a patch number or program number map), a GM percussion map (mapping of percussion sounds to note numbers), and a set of GM performance capabilities (number of voices, types of MIDI messages recognized, etc.).

A MIDI sequence which has been generated for use on a General MIDI instrument should play correctly on any General MIDI synthesizer or sound module. The numbers in the table on page B-4 refer to the program change number, which is called within a sequence to select a particular instrument or voice. In synthesizers or sound modules designed to conform to the General MIDI Standard, Program Change Number 1 will always be Acoustic Grand Piano, while Program Change Number 47 is always the Orchestral Harp, and so on. Any of these instrument voices can be selected by issuing its appropriate program change number on any of the 16 MIDI channels, except for channel 10. For General MIDI compatibility among GM instruments or sound modules, MIDI Channel 10 is always reserved for the program change number, which selects the percussion sounds, or drum kit, of the GM-compliant synthesizer or rack style sound module.

The General MIDI sound set is grouped into "sets" of related sounds. For example, program numbers 1-8 are piano sounds, 9-16 are chromatic, or tonal, percussion sounds, 17-24 are organ sounds, 25-32 are guitar sounds, etc. The General MIDI system utilizes MIDI channels 1-9 and 11-16 for chromatic, or tonal, instrument sounds, while channel number 10 is utilized for "key-based" non-tonal, percussion sounds. For the instrument sounds on channels 1-9 and 11-16, the note number in a MIDI Note On message is used to select the pitch of the sound to be played. For example, if the vibraphone instrument (program number 12) has been selected on channel 3, then playing note number 60 on channel 3 would play the middle C note (this would be the default note to pitch assignment on most instruments), and note number 59 on channel 3 would play B below middle C. Both notes would be played using the vibraphone sound.

The General MIDI percussion map used for channel 10 is given in the table on page B-11. For these "key-based" non-tonal percussion sounds, the note number data in a MIDI Note On message is used to trigger the percussion sounds.

There are 47 note numbers in the General MIDI percussion map. However, the HSP wavetable synthesizer provided with the OTI-610/OTI-611 provides 61 percussion sounds, including the 47 required by the General MIDI Standard.

Note numbers on channel 10 are used to select which drum or percussion sound will be played. For example, a Note On message on channel 10 with note number 60 will play a hi bongo drum sound. Note number 59 on channel 10 will play the Ride Cymbal 2 sound.

It should be noted that the General MIDI system specifies sounds using program numbers 1 through 128. The MIDI Program Change message used to select these sounds uses an 8-bit byte, which corresponds to decimal numbering from 0 through 127, (or 00H through 7FH hexadecimal) to specify the desired program number. Thus, to select GM sound number 10, the glockenspiel, the Program Change message will have a data byte with the decimal value 9.

The GM system specifies which instrument or sound corresponds with each program/patch number, but General MIDI does not specify how these sounds are produced. Thus, program number 1 should select the acoustic grand piano sound on any General MIDI instrument. However, the acoustic grand piano sound on two General MIDI synthesizers that use different synthesis techniques may sound quite different. Thus, the quality of the synthesizer is based on the quality of the synthesis technique for a particular instrument sound. For some instruments, the sounds may be rendered better using an FM synthesis technique, while other instruments may be rendered better using wavetable (recorded instrument samples) playback, or physical modeling synthesis, which not only models the instrument but the method of playing it.

There are other requirements of General MIDI, such as the synthesizer or sound module being capable of responding to 16 MIDI channels with voice polyphony (16 pitched sounds and 8 percussion sounds at once), resulting in 24-voice polyphony.

B.4 GENERAL MIDI SOUND SAMPLE SET DESCRIPTION

The high-quality GM sample set is derived from professional music sample libraries, and is customized for use with the OTI-610 and OTI-611. A complete listing of the GM sample set provided with the OTI-610 and OTI-611 is given in the table below. A complete listing of the GM Percussion Map (percussion sounds) provided with the OTI-610 and OTI-611 is given in the table on page B-11.

Since CyberSound GM is capable of downloadable samples, the user is not limited to the GM sample set. Additional sounds, even complete sound libraries, can be used with CyberSound GM.

General MIDI Sound Set Sample Set (All Channels Except 10):

Prog #	Instrument	Prog #	Instrument	Prog #	Instrumnet	Prog #	Instrument
1	Acoustic Grand Piano	33	Acoustic Bass	65	Soprano Sax	97	FX 1 (rain)
2	Bright Acoustic Piano	34	Electric Bass (finger)	66	Alto Sax	98	FX 2 (soundtrack)
3	Electric Grand Piano	35	Electric Bass (pick)	67	Tenor Sax	99	FX 3 (crystal)
4	Honky-tonk Piano	36	Fretless Bass	68	Baritone Sax	100	FX 4 (atmosphere)
5	Electric Piano 1	37	Slap Bass 1	69	Oboe	101	FX 5 (brightness)
6	Electric Piano 2	38	Slap Bass 2	70	English Horn	102	FX 6 (goblins)
7	Harpsichord	39	Synth Bass 1	71	Bassoon	103	FX 7 (echoes)
8	Clavi	40	Synth Bass 2	72	Clarinet	104	FX 8 (sci-fi)
9	Celesta	41	Violin	73	Piccolo	105	Sitar
10	Glockenspiel	42	Viola	74	Flute	106	Banjo
11	Music Box	43	Cello	75	Recorder	107	Shamisen
12	Vibraphone	44	Contrabass	76	Pan Flute	108	Koto
13	Marimba	45	Tremolo Strings	77	Blown Bottle	109	Kalimba
14	Xylophone	46	Pizzicato Strings	78	Shakuhachi	110	Bag pipe
15	Tubular Bells	47	Orchestral Harp	79	Whistle	111	Fiddle
16	Dulcimer	48	Timpani	80	Ocarina	112	Shanai
17	Drawbar Organ	49	String Ensemble 1	81	Lead 1 (square)	113	Tinkle Bell
18	Percussive Organ	50	String Ensemble 2	82	Lead 2 (sawtooth)	114	Agogo
19	Rock Organ	51	SynthStrings 1	83	Lead 3 (calliope)	115	Steel Drums
20	Church Organ	52	SynthStrings 2	84	Lead 4 (chiff)	116	Woodblock
21	Reed Organ	53	Choir Aahs	85	Lead 5 (charang)	117	Taiko Drum
22	Accordion	54	Voice Oohs	86	Lead 6 (voice)	118	Melodic Tom
23	Harmonica	55	Synth Voice	87	Lead 7 (fifths)	119	Synth Drum
24	Tango Accordion	56	Orchestra Hit	88	Lead 8 (bass + lead)	120	Reverse Cymbal
25	Acoustic Guitar - nylon	57	Trumpet	89	Pad 1 (new age)	121	Guitar Fret Noise
26	Acoustic Guitar - steel	58	Trombone	90	Pad 2 (warm)	122	Breath Noise
27	Electric Guitar (jazz)	59	Tuba	91	Pad 3 (polysynth)	123	Seashore
28	Electric Guitar (clean)	60	Muted Trumpet	92	Pad 4 (choir)	124	Bird Tweet
29	Electric Guitar (muted)	61	French Horn	93	Pad 5 (bowed)	125	Telephone Ring
30	Overdriven Guitar	62	Brass Section	94	Pad 6 (metallic)	126	Helicopter
31	Distortion Guitar	63	SynthBrass 1	95	Pad 6 (halo)	127	Applause
32	Guitar Harmonics	64	SynthBrass 2	96	Pad 7 (sweep)	128	Gunshot

The following charts break down the MIDI sound sample set by type of instrument sound.

Piano:

Prog #	Program Description
0	Acoustic Grand Piano
1	Bright Acoustic Piano
2	Electric Grand Piano
3	Honky-tonk Piano
4	Rhodes Piano
5	Chorused Piano
6	Harpsichord
7	Clavinet Chromatic

Tonal Percussion:

Prog #	Program Description
8	Celesta
9	Glockenspiel
10	Music Box
11	Vibraphone
12	Marimba
13	Xylophone
14	Tubular Bells
15	Dulcimer

Organ:

Prog #	Program Description
16	Hammond Organ
17	Percussive Organ
18	Rock Organ
19	Church Organ
20	Reed Organ
21	Accordion
22	Harmonica
23	Tango Accordion

Guitar:

Prog #	Program Description
24	Acoustic Guitar (nylon)
25	Acoustic Guitar (steel)
26	Electric Guitar (jazz)
27	Electric Guitar (clean)
28	Electric Guitar (muted)
29	Overdriven Guitar
30	Distortion Guitar
31	Guitar Harmonics

Bass:

Prog #	Program Description
32	Acoustic Bass
33	Electric Bass (finger)
34	Electric Bass (pick)
35	Fretless Bass
36	Slap Bass 1
37	Slap Base 2
38	Synth Bass 1
39	Synth Bass 2

Strings:

Prog #	Program Description
40	Violin
41	Viola
42	Cello
43	Contrabass
44	Tremolo Strings
45	Pizzicato Strings
46	Orchestral Harp
47	Timpani

Ensemble:

Prog #	Program Description
48	String Ensemble 1
49	String Ensemble 2
50	SynthStrings 1
51	SynthStrings 2
52	Choir Aahs
53	Voice Oohs
54	Synth Voice
55	Orchestra Hit

Brass:

Prog #	Program Description
56	Trumpet
57	Trombone
58	Tuba
59	Muted Trumpet
60	French Horn
61	Brass Section
62	Synth Brass 1
63	Synth Brass 2

Reed:

Prog #	Program Description
64	Soprano Sax
65	Alto Sax
66	Tenor Sax
67	Baritone Sax
68	Oboe
69	English Horn
70	Bassoon
71	Clarinet

Pipe:

Prog #	Program Description
72	Piccolo
73	Flute
74	Recorder
75	Pan Flute
76	Bottle Blow
77	Shakuhachi
78	Whistle
79	Ocarina

Synthesizer Lead:

Prog #	Program Description
80	Synth Lead 1 (Square)
81	Synth Lead 2 (Sawtooth)
82	Synth Lead 3 (Caliope Lead)
83	Synth Lead 4 (Chiff Lead)
84	Synth Lead 5 (Charang)
85	Synth Lead 6 (Voice)
86	Synth Lead 7 (Fifths)
87	Synth Lead 8 (Brass + Lead)

Synthesizer Pad:

Prog #	Program Description
88	Pad 1 (new age)
89	Pad 2 (warm)
90	Pad 3 (polysynth)
91	Pad 4 (choir)
92	Pad 5 (bowed)
93	Pad 6 (metallic)
94	Pad 7 (halo)
95	Pad 8 (sweep)

Synthesizer Effects:

Prog #	Program Description
96	FX 1 (rain)
97	FX 2 (soundtrack)
98	FX 3 (crystal)
99	FX 4 (atmosphere)
100	FX 5 (brightness)
101	FX 6 (goblins)
102	FX 7 (echoes)
103	FX 8 (sci-fi)

Ethnic:

Prog #	Program Description
104	Sitar
105	Banjo
106	Shamisen
107	Koto
108	Kalimba
109	Bagpipe
110	Fiddle
111	Shanai

Non-tonal Percussive:

Prog #	Program Description
112	Tinkle Bell
113	Apogo
114	Steel Drums
115	Woodblock
116	Taiko Drum
117	Melodic Tom
118	Synth Drum
119	Reverse Cymbal

Sound Effects:

Prog #	Program Description
120	Guitar Fret Noise
121	Breath Noise
122	Seashore
123	Bird Tweet
124	Telephone
125	Helicopter
126	Applause
127	Gunshot

The following table gives the General MIDI percussion map:

MIDI Note		Percussion Sound	MIDI Note		Percussion Sound
#	Name		#	Name	
27	D#1	*High Q*	58	A#3	**Vibraslap**
28	E1	*Slap*	59	B3	**Ride Cymbal 2**
29	F1	*Scratch Push*	60	C4	**High Bongo**
30	F#1	*Scratch Pull*	61	C#4	**Low Bongo**
31	G1	*Sticks*	62	D4	**Mute High Conga**
32	G#1	*Click Square*	63	D#4	**Open High Conga**
33	A1	*Metronome Click*	64	E4	**Low Conga**
34	A#1	*Metronome Bell*	65	F4	**High Timbale**
35	B1	**Acoustic Bass Drum**	66	F#4	**Low Timbale**
36	C2	**Bass Drum 1**	67	G4	**High Agogo**
37	C#2	**Side Stick**	68	G#4	**Low Agogo**
38	D2	**Acoustic Snare**	69	A4	**Cabasa**
39	D#2	**Hand Clap**	70	A#4	**Maracas**
40	E2	**Electric Snare**	71	B4	**Short Whistle**
41	F2	**Low Floor Tom**	72	C5	**High Whistle**
42	F#2	**Closed High Hat**	73	C#5	**Short Guiro**
43	G2	**High Floor Tom**	74	D5	**Long Guiro**
44	G#2	**Pedal High Hat**	75	D#5	**Claves**
45	A2	**Low Tom**	76	E5	**High Wood Block**
46	A#2	**Open High Hat**	77	F5	**Low Wood Block**
47	B2	**Low-Mid Tom**	78	F#5	**Mute Cuica**
48	C3	**High-Mid Tom**	79	G5	**Open Cuica**
49	C#3	**Crash Cymbal 1**	80	G#5	**Mute Triangle**
50	D3	**High Tom**	81	A5	**Open Triangle**
51	D#3	**Ride Cymbal 1**	82	A#5	*Shaker*
52	E3	**Chinese Cymbal**	83	B5	*Jingle Bell*
53	F3	**Ride Bell**	84	C6	*Belltree*
54	F#3	**Tambourine**	85	C#6	*Castanets*
55	G3	**Splash Cymbal**	86	D6	*Mute Surdo*
56	G#3	**Cowbell**	87	D#6	*Open Surdo*
57	A3	**Crash Cymbal 2**			

Note: All percussion sounds listed in bold type are the required General MIDI percussion sounds. Those listed in italics are the extra ones provided with the OTI-610/OTI-611.

B.5 CYBERSOUND KEYBOARD DESCRIPTION

CyberSound Keyboard is an interactive software MIDI keyboard application that works in conjunction with the CyberSound GM wavetable synthesizer. The application permits the user to play musical notes and change instrument settings in real time.

Basic specifications are:

- PC QWERTY keyboard input with three-octave range
- One-finger/mouse-click chord input
- Multiple style arpeggiator

B.6 WAVETABLE SYNTHESIZER KEY/NOTE RANGE

In the General MIDI Specification, the MIDI note number range is given as 0 through 127, corresponding to Key Name C-1 through G9. Not all synthesizers are able to generate tones over the entire MIDI note range. It is necessary to consult the MIDI implementation chart for the particular synthesizer to determine the note range that is covered.

A standard piano keyboard layout consists of 88 keys, from Key Name A0 to Key Name C120. Those 88 keys cover 7 octaves (1 through 8) plus 4 keys (A0, A#0, B0 at the low end, and C9 at the high end), and correspond to MIDI Note Numbers 21 through 120.

An octave consists of 12 notes. For example, the notes within Octave 2 would be:
C2, C2#, D2, D2#, E2, F2, F2#, G2, G2#, A2, A2#, B2
in ascending order, where the pitch of C2 is lower than the pitch of B2.

Key Name C4 is also known as Middle C in a standard 88-key piano keyboard layout.

The table below summarizes the comparison between a standard piano keyboard layout and MIDI note numbers and note key names.

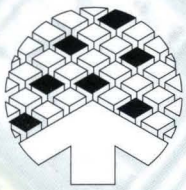
Octave #	-1	0	1	2	3	4	5	6	7	8	9	9
Key Name Range	C-1 - B-1	C0 - B0	C1 - B1	C2 - B2	C3 - B3	C4 - B4	C5 - B5	C6 - B6	C7 - B7	C8 - B7	C9 - B9	
Key Name	C-1	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	G9
MIDI Note #	0	12	24	36	48	60	72	84	96	108	120	127
Standard 88 Piano Keys	-	A0	C1	C2	C3	C4 Mid C	C5	C6	C7	C8	C9	-
MIDI Note #	-	21	24	36	48	60	72	84	96	108	120	-

The CyberSound GM HSP-based synthesizer provided with the OTI-610/OTI-611 responds to MIDI Note Numbers (Key Name) 12 (C0) through 120 (C9).

OTI-610/OTI-611 HSP-Based Wavetable Synthesizer (CyberSound GM) MIDI Implementation Table:

Function	Transmitted	Received	Remarks
MIDI Channels		1-16	
Basic Channel		1	
Mode Default			Multi-polyphonic
Note Number		C0 - C9	
Velocity		0 -127	
After Touch Keys Channel		 X X	
Pitch Bend		0	+/- 1 note +/- 8192
Control 1,2 7 10 11 64 121	 X X X X X X	 O O O O O O	 Modulation Volume Pan Expression Sustain Reset All Controls
Program Change #	X	0 - 127	
System Exclusive	X	X	

Note: O = Yes; X = No



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