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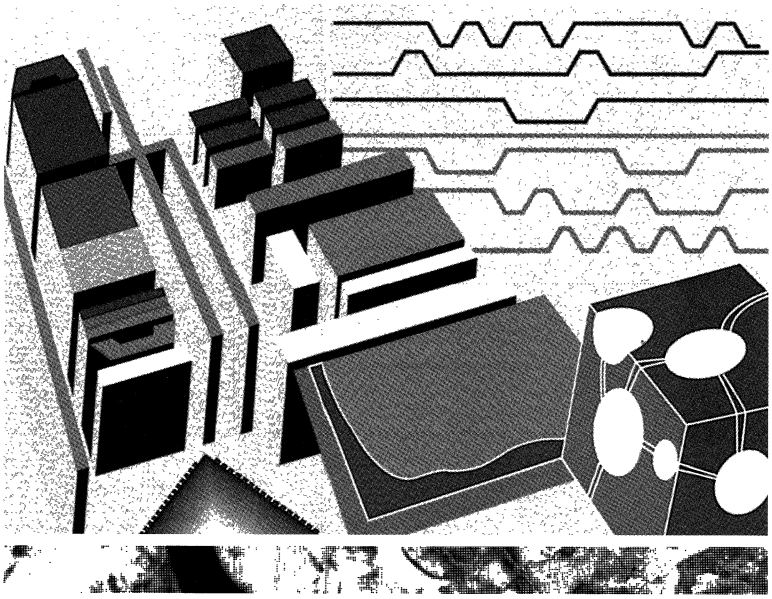

μPD72611
SCSI-2 Controller

Preliminary User's Manual

NEC

uPD72611

SCSI-2 CONTROLLER

PRELIMINARY USER'S MANUAL

Document Pro.

Microcomputer & Memory Engineering Dept.

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PREFACE

Intended Readership : This manual is intended for users' engineers who require an understanding of the functions of uPD72611 and wish to design application systems using this device.

Purpose : The purpose of this manual is to give users an understanding of the hardware functions of the uPD72611 listed below.

Organization : This manual is broadly organized as follows:

- General Description
- Pin Functions
- Internal Block Functions
- Commands
- Control
- System Configuration

Using this Manual : Readers require a general understanding of electrical and logic circuits and microcomputers.

For users with previous experience of a different SCSI controller:

→ Check the differences between the uPD72611 and the other SCSI controller in 1.4 "Features", and focus on the relevant descriptions.

To check the function of a command:

→ Check the contents to find the description of that command.

To check the function of a command when the command name is not known but the function is generally understood:

→ Find the command name in 1.3 "Commands", then consult 5.2 "Command Functions" for the function.

For a general idea of the functions of the uPD72611:

→ Read in accordance with the contents.

Legend : Significance in

data notation	:	High-order digit on left, low-order digit on right
Active-low notation:		$\overline{\text{xxx}}$ (Line above pin or signal name)
*	:	Explanation of item marked with an asterisk in the text
NOTE	:	Item to be especially noted
Remarks	:	Supplementary information
Numeric notations	:	Binary ..... xxxx or xxxxB
		Decimal xxxx
		Hexadecimal ... xxxxH

Related Documentation: o Documentation on the uPD72611:

- Brochure (IF-6070A)
- Preliminary Data Sheet (ID-8343)
- Preliminary User's Manual (This manual)

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CHAPTER 1. GENERAL DESCRIPTION

The uPD72611 is an SCSI-2 (Small System Interface-2) controller compliant with ANSI X3T9.2/86-109 Rev.10c.

It incorporates bus phase sequence control functions, allowing the load on the host processor to be reduced. It is compatible with a 32-, 16- or 8-bit CPU data bus.

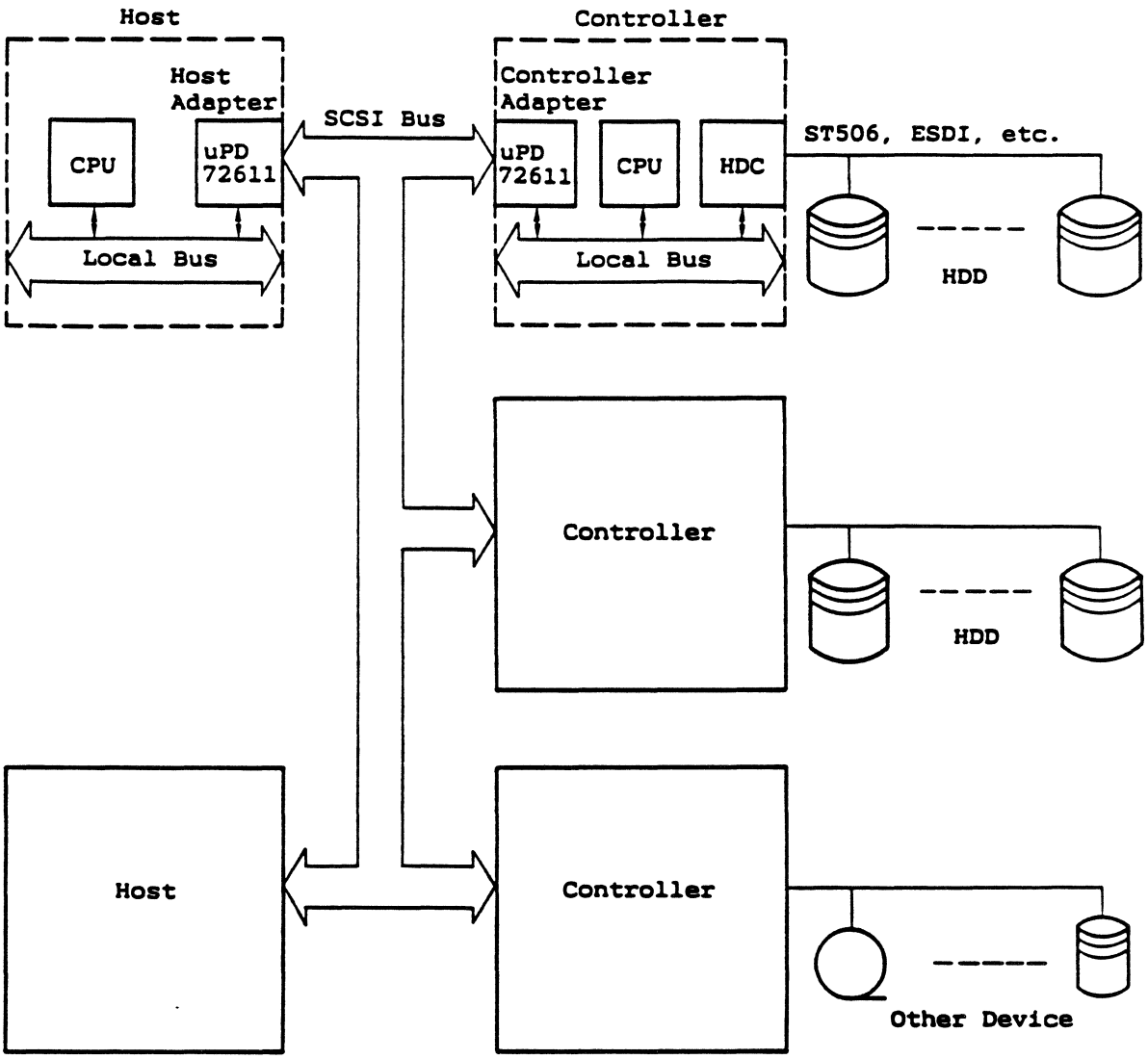
A single-end type driver/receiver is incorporated at the SCSI bus side, allowing direct connection with a SCSI bus. In addition, an external differential driver/receiver is supported.

1.1 SYSTEM OUTLINE

The position of uPD72611s in the configuration of an SCSI system is shown in Figure 1-1. Up to eight SCSI devices, including both hosts and controllers, can be connected to the SCSI bus. The uPD72611 functions as a host adapter/ controller adapter which interfaces with the SCSI bus. Each SCSI device is assigned a fixed ID number between 0 and 7.

On the SCSI bus, communication is carried out between two SCSI devices, specified as the initiator and the target.

Figure 1-1 System Configuration Example

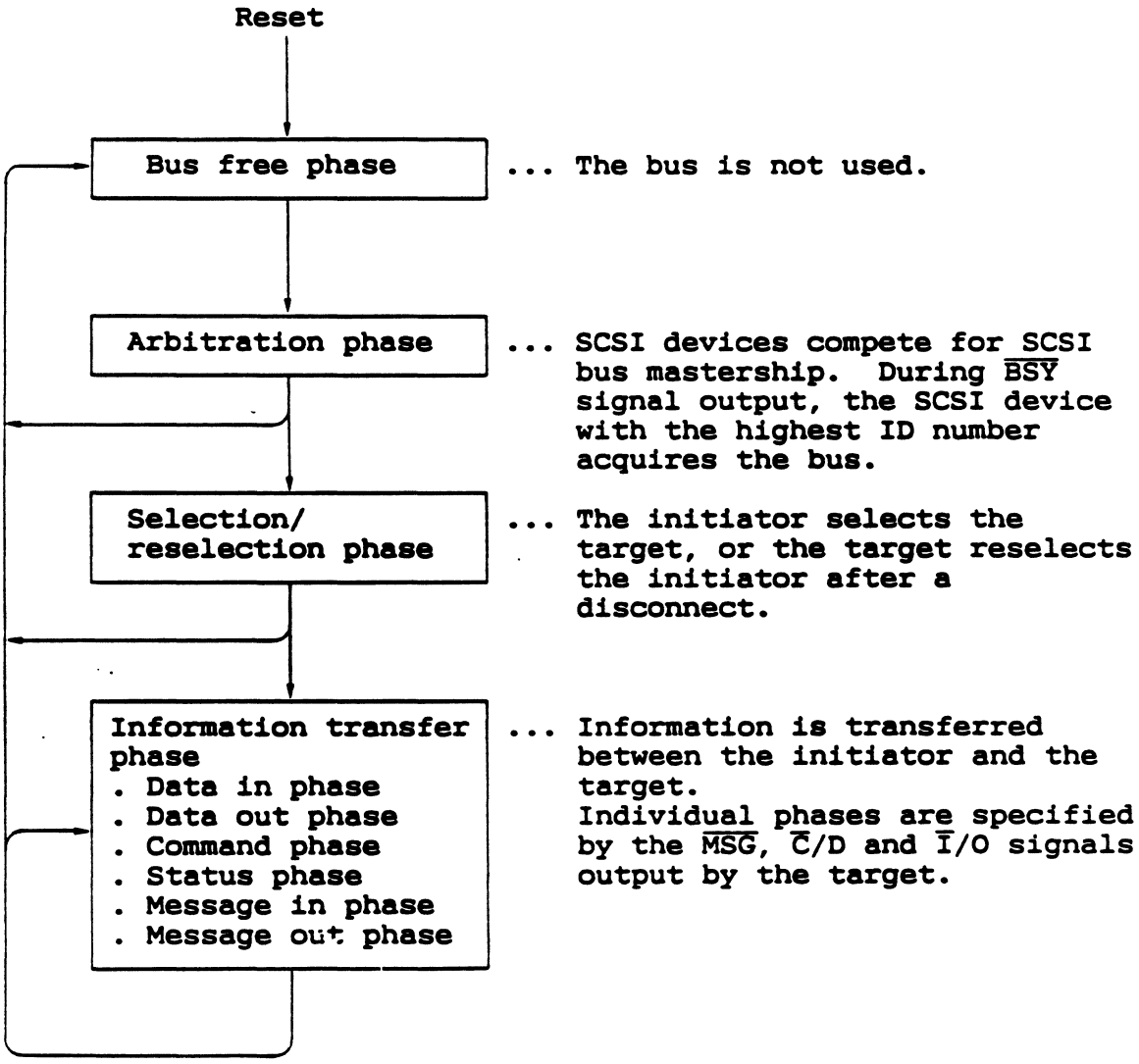


1.2 OUTLINE OF SYSTEM OPERATION

In an SCSI system, communication is performed between an SCSI device specified as the initiator and an SCSI device specified as the target.

SCSI bus phase transitions are shown in the figure below. Bus phase control in the information transfer phase is performed by the target.

Figure 1-2 SCSI Bus Phase Transitions



1.3 COMMANDS

The uPD72611 incorporates the 18 commands shown below.

Table 1-1 Commands

Type	Command Name	Mnemonic	Outline of Operation
Group I	CHIP RESET	CRST	Internal uPD72611 reset
	BREAK	BRK	Suspension of command execution
	DISCONNECT	DIS	SCSI bus release
	CLEAR FIFO	CLRF	FIFO buffer clearance
	SCSI RESET	SRST	SCSI bus reset
Group II	SET ATN	SETAT	$\overline{\text{ATN}}$ signal setting (0)
	RESET ACK	RSTAK	$\overline{\text{ACK}}$ signal reset (1)
	SELECT	SEL	Target selection
	TRANSFER	TFR	Information transmission/reception (initiator)
	AUTO INITIATOR	AINI	Automatic execution of initiator standard operation
	AUTO INITIATOR 2	AINI2	Automatic execution of initiator standard operation after reselection
Group III	RESELECT	RSEL	Initiator reselection
	RECEIVE	REC	Information reception (target)
	SEND	SND	Information transmission (target)
	AUTO TARGET	ATGT	Automatic execution of target standard operation
	AUTO TARGET 2	ATGT2	Automatic execution of target standard termination operation
	RE-RECEIVE	RREC	Reselection → data reception consecutive execution (target)
	RE-SEND	RSND	Reselection → data transmission consecutive execution (target)

Remarks: A group is a set of commands classified by use.
This is different from the SCSI command group.

1.4 FEATURES

- o Conforms to ANSI X3T9.2/86-109 Rev.10c (SCSI-2 standard)
- o System clock: Max. 20 MHz
- o Data transfer rate
  - . Asynchronous (5.0M bytes/sec or above)
  - . Synchronous (Max. 5.0M bytes/sec: Programmable in 7 steps)
  - . High-speed synchronous (Max. 10.0M bytes/sec: Programmable in 7 steps)
- o Operable as initiator or target
- o CPU-side bus width selectable (32/16/8 bits)
- o On-chip single-end type SCSI bus driver and Schmitt type receiver
- o Supports external differential driver and receiver.
- o Supports 6 compound commands which alleviate the host CPU interrupt handling load.
- o Command queuing function

  3-byte message transfer supported for each compound command
- o Parity through supported
- o Synchronization offset value specifiable (1 to 8)
- o On-chip 24-bit transfer counter

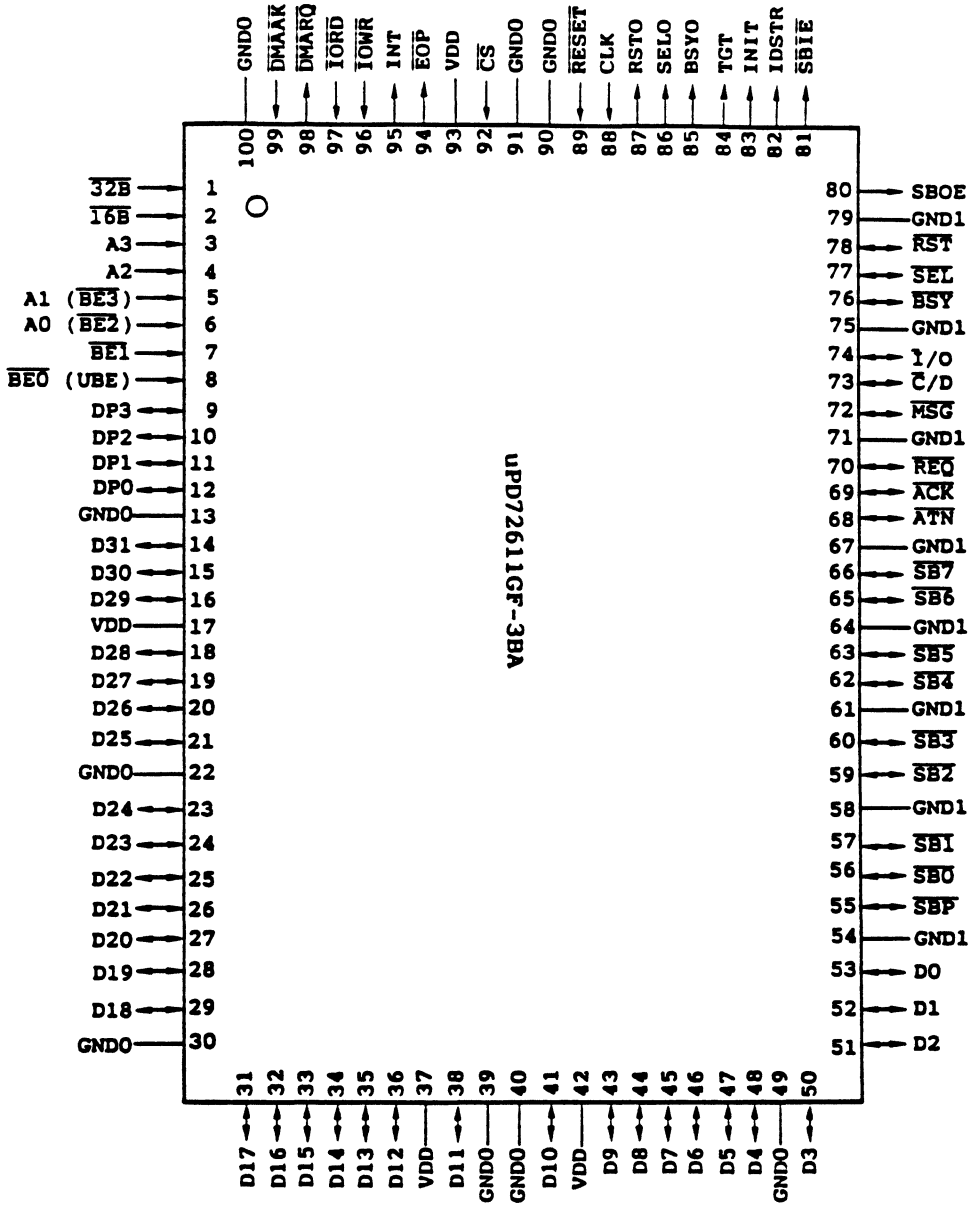
1.5 ORDERING INFORMATION

Product Name	Package	Quality Grade
uPD72611GF-3BA	100-pin plastic QFP	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

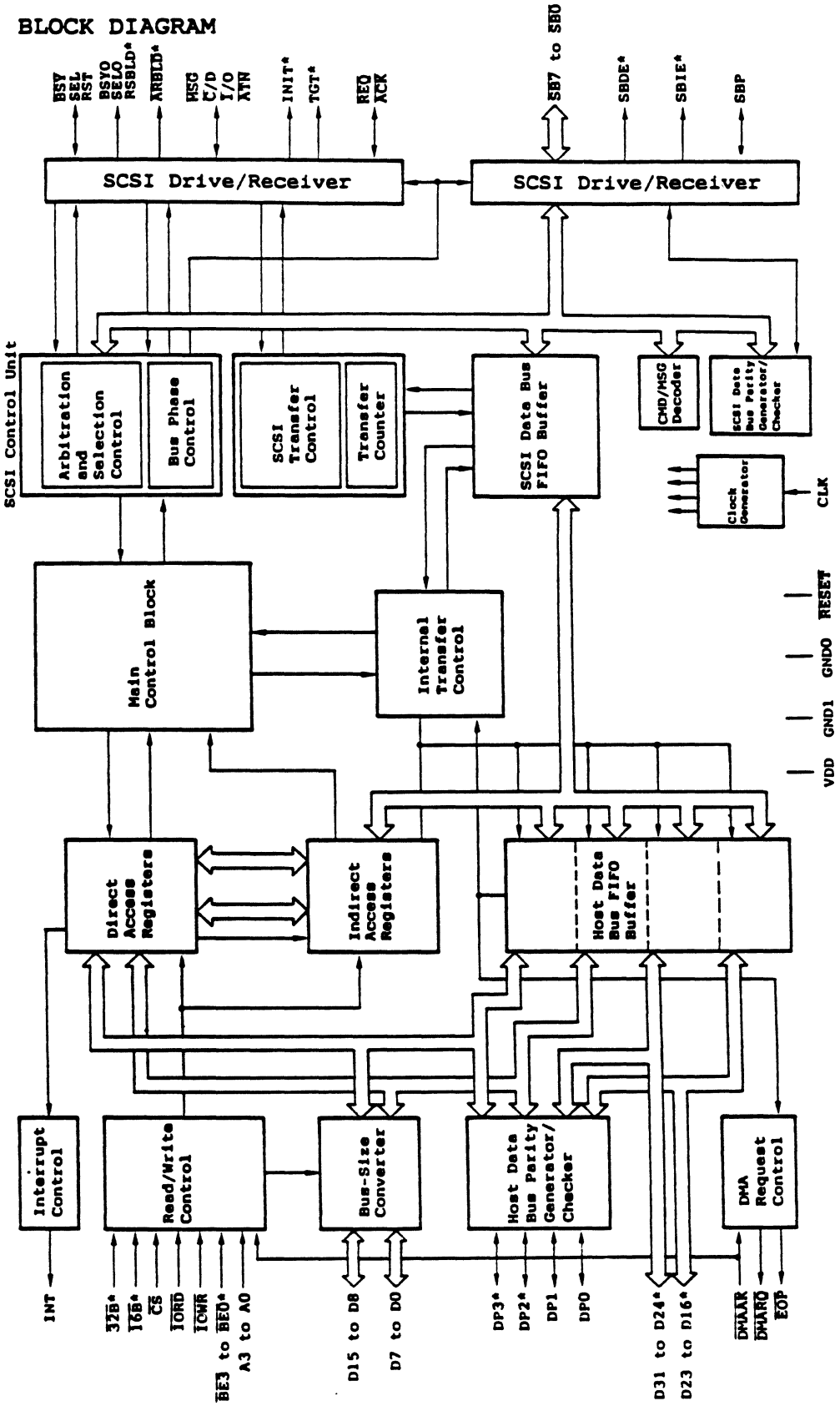
1.6 PIN CONFIGURATION (TOP VIEW)

100-pin plastic QFP



$\overline{SB0}$ to $\overline{SB7}$	:	SCSI Buses 0 to 7
$\overline{SBP}$	:	SCSI Bus Parity
$\overline{ANT}$	:	Attention
$\overline{ACK}$	:	Acknowledge
$\overline{REQ}$	:	Request
$\overline{MSG}$	:	Message
$\overline{C}$/D	:	Command/Data
$\overline{I}$/O	:	Input/Output
$\overline{BSY}$	:	Busy
$\overline{SEL}$	:	Select
$\overline{RST}$	:	Reset
RSTO	:	Reset Out
BSYO	:	Busy Out
SELO	:	Select Out
IDSTR	:	ID Strobe
INIT	:	Initiator
TGT	:	Target
SBOE	:	SCSI Bus Out Enable
$\overline{SBIE}$	:	SCSI Bus In Enable
INT	:	Interrupt Request
$\overline{IORD}$	:	I/O Read
$\overline{IOWR}$	:	I/O Write
A2 & A3	:	Addresses 2 & 3
A0/$\overline{BE2}$ & A1/$\overline{BE3}$	:	Address 0 & 1/Byte Enable 2 & 3
$\overline{BE0}$/$\overline{UBE}$	:	Byte Enable 0/Upper Byte Enable
$\overline{BE1}$	:	Byte Enable 1
$\overline{CS}$	:	Chip Select
D0 to D31	:	Data Buses 0 to 31
DP0 to DP3	:	Data Parity 0 to 3
$\overline{DMARQ}$	:	DMA Request
$\overline{DMAAK}$	:	DMA Acknowledge
$\overline{EOP}$	:	End of Process
$\overline{RESET}$	:	Reset
$\overline{16B}$	:	16-bit Bus
$\overline{32B}$	:	32-bit Bus

1.7 BLOCK DIAGRAM



Remarks: * indicates a new signal not present in the uPD72111.

CHAPTER 2. PIN FUNCTIONS

uPD72611 pins are divided into those on the CPU interface side and those on the SCSI interface side.

2.1 CPU INTERFACE PINS

Name	Input/ Output	Pin No.	Function
INT (Interrupt Request)	Output	95	Pin which outputs interrupt request signal to the CPU Activated when an internal interrupt source is generated.
$\overline{\text{IROD}}$ (I/O Read)	Input	97	Read signal input pin for reading from uPD72611 internal registers by the CPU
$\overline{\text{IOWR}}$ (I/O Write)	Input	96	Write signal input pin for writing to uPD72611 internal registers by the CPU
A2 & A3 (Addresses 2 & 3)	Input	4, 3	Input pins for high-order 2 bits of address Specify the direct access register to be accessed.
A0/$\overline{\text{BE2}}$ & A1/$\overline{\text{BE3}}$ (Addresses 0 & 1/ Byte Enable 2 & 3)	Input	6, 5	. In 32-bit bus mode Input pins for signals indicating valid bus in a data access together with $\overline{\text{BE1}}$ & $\overline{\text{BE0}}$ signals . In 16-/8-bit bus mode Input pins for low-order 2 bits of address
$\overline{\text{BE1}}$ (Byte Enable 1)	Input	7	. In 32-bit bus mode Input pin for signal indicating valid bus in a data access together with $\overline{\text{BE3}}$, $\overline{\text{BE2}}$ & $\overline{\text{BE0}}$ signals
$\overline{\text{BE0}}$/$\overline{\text{UBE}}$ (Byte Enable 0/ Upper Byte Enable)	Input	8	. In 32-bit bus mode Input pin for signal indicating valid bus in a data access together with $\overline{\text{BE3}}$, $\overline{\text{BE2}}$ & $\overline{\text{BE1}}$ signals . In 16-bit bus mode Input pin for upper byte data input/output enable signal Only valid in 32-/16-bit bus mode.

(to be continued)

(cont'd)

<table>
<tr><th>Name</th><th>Input/ Output</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>$\overline{BE0}/\overline{UBE}$ (Byte Enable 0/ Upper Byte Enable) (cont'd)</td><td>Input</td><td>8</td><td>
<table>
<tr><th>A0</th><th>$\overline{UBE}$</th><th>Internal Register Access</th></tr>
<tr><td>L</td><td>L</td><td>Internal register D15 to D0 (16 bits)</td></tr>
<tr><td>L</td><td>H</td><td>Internal register D7to D0 (8 bits)</td></tr>
<tr><td>H</td><td>L</td><td>Internal register D15 to D8 (8 bits)</td></tr>
<tr><td>H</td><td>H</td><td>Use prohibited</td></tr>
</table>
</td></tr>
<tr><td>$\overline{CS}$ (Chip Select)</td><td>Input</td><td>92</td><td>Chip select signal input pin. Enables access to internal register.</td></tr>
<tr><td>D0 to D31 (Data 0 to 31)</td><td>Input/ output</td><td>53, 52, 51, 50, 48, 47, 46, 45, 44, 43, 41, 38, 36, 35, 34, 33, 32, 31, 29, 28, 27, 26, 25, 24, 23, 21, 20, 19, 18, 16, 15, 14</td><td>32-bit data input/output pins
These pins function as follows according to the bus mode specification:
. In 32-bit bus mode
D0 to D7 : Input/output pins for lower byte of low-order 16 bits of 32-bit data
D8 to D15 : Input/output pins for upper byte of low-order 16 bits of 32-bit data
D16 to D31: Input/output pins for high-order 16 bits of 32-bit data
. In 16-bit bus mode
D0 to D7 : Input/output pins for lower byte of 16-bit data
D8 to D15 : Input/output pins for upper byte of 16-bit data
D16 to D31: High-impedance (input) state. Should be fixed high or low.
. In 8-bit bus mode
D0 to D7 : 8-bit data input/output pins
D8 to D31 : High-impedance (input) state. Should be fixed high or low.</td></tr>
<tr><td>DP0 to DP3 (Data Parity 0 to 3)</td><td>Input/ output</td><td>12, 11, 10, 9</td><td>Input/output pins for parity signals added to data bus
. In 32-bit bus mode
D0 to D7 : DP0
D8 to D15 : DP1
D16 to D23: DP2
D24 to D31: DP3</td></tr>
</table>

(to be continued)

(cont'd)

Name	Input/ Output	Pin No.	Function
DP0 to DP3 (Data Parity 0 to 3) (cont'd)	Input/ output	12, 11, 10, 9	. In 16-bit bus mode D0 to D7 : DP0 D8 to D15 : DP1 The DP2 & DP3 pins are in the high-impedance (input) state and should be fixed high or low. . In 8-bit data mode D0 to D7 : DP0 The DP1, DP2 & DP3 pins are in the high-impedance (input) state and should be fixed high or low.
$\overline{\text{DMARQ}}$ (DMA Request)	Output	98	DMA service request signal output pin. In the data in/data out phase when DMA mode has been specified, outputs a low-level signal when the FIFO buffer is in the following state: Write to FIFO buffer : When there are only 6 or fewer levels of data in the FIFO buffer. Read from FIFO buffer: When there are 2 or more levels of data in the FIFO buffer. However, when the last transfer data is left in the FIFO buffer, this pin also outputs a low-level signal when only one level of data is left in the FIFO buffer.
$\overline{\text{DMAAK}}$ (DMA Acknowledge)	Input	99	DMA service enable signal input pin. When this pin is activated, the data FIFO register is specified as the object of the access irrespective of the status of the $\overline{\text{CS}}$ and A0 to A2 signals. When DMA mode is not specified, this pin should be fixed high.
$\overline{\text{EOP}}$ (End of Process)	Output	94	Output pin for signal indicating end of data transfer. Activated in case of uPD72611 abnormal termination or break operation. Open-drain output.

2.2 SCSI INTERFACE PINS

Name	Input/ Output	Pin No.	Function
$\overline{SB0}$ to $\overline{SB7}$ *1 (SCSI Buses 0 to 7)	Input/ output	56, 57, 59, 60, 62, 63, 65, 66	SCSI data bus input/output pins
$\overline{SBP}$ *1 (SCSI Bus Parity)	Input/ output	55	Input/output pins for parity signals added to SCSI data bus
$\overline{BSY}$ *1 (Busy)	Input/ output	76	Input/output pin connected to SCSI control bus $\overline{BSY}$ signal. Indicates the another SCSI device is using the SCSI bus.
$\overline{SEL}$ *1 (Select)	Input/ output	77	Input/output pin connected to SCSI control bus $\overline{SEL}$ signal. Indicates that a select/reselect operation is being executed in the selection/ reselection phase.
$\overline{REQ}$ *1 (Request)	Input/ output	70	Input/output pin connected to SCSI control bus $\overline{REQ}$ signal. Indicates a target information transfer request.
$\overline{ACK}$ *1 (Acknowl- edge)	Input/ output	69	Input/output pin connected to SCSI control bus $\overline{ACK}$ signal. Indicates initiator has accepted a target information transfer request.
$\overline{ATN}$ *1 (Attention)	Input/ output	68	Input/output pin connected to SCSI control bus $\overline{ATN}$ signal. Indicates initiator is requesting message out phase.
$\overline{MSG}$ *1 (Message)	Input/ output	72	Input/output pins connected to SCSI control bus $\overline{MSG}$, $\overline{C}$/D & $\overline{I}$/O signals. The SCSI bus phase is indicated by a combination of these signals as shown below.
$\overline{C}$/D *1 (Command/ Data)	Input/ output	73	
$\overline{I}$/O *1 (Input/ Output)	Input/ output	74	

(to be continued)

(cont'd)

<table>
<tr><th>Name</th><th>Input/ Output</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>$\overline{MSG}$ *1 (Message) (cont'd)</td><td>Input/ output</td><td>72</td><td rowspan="3"><table>
<tr><th>$\overline{MSG}$</th><th>$\overline{C}$/D</th><th>$\overline{I}$/O</th><th>Bus Phase</th></tr>
<tr><td>H</td><td>H</td><td>H</td><td>Data out phase</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>Data in phase</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>Command phase</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>Status phase</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>Message out phase</td></tr>
<tr><td>L</td><td>L</td><td>L</td><td>Message in phase</td></tr>
</table></td></tr>
<tr><td>$\overline{C}$/D *1 (Command/ Data) (cont'd)</td><td>Input/ output</td><td>73</td></tr>
<tr><td>$\overline{I}$/O *1 (Input/ Output) (cont'd)</td><td>Input/ output</td><td>74</td></tr>
<tr><td>$\overline{RST}$ *1 (Reset)</td><td>Input/ output</td><td>78</td><td>Input/output pin connected to SCSI control bus $\overline{RST}$ signal. When this signal is detected, the uPD72611 immediately releases the bus, activates the INT signal and assumes the idle status.</td></tr>
<tr><td>RSTO *2 (Reset Out)</td><td>Output</td><td>87</td><td>Outputs a high-level signal while the $\overline{RST}$ signal is active, and makes the $\overline{RST}$ signal driver output-enabled.</td></tr>
<tr><td>BSYO *2 (Busy Out)</td><td>Output</td><td>85</td><td>Outputs a high-level signal while the $\overline{BSY}$ signal is active, and makes the $\overline{BSY}$ signal driver output-enabled.</td></tr>
<tr><td>SELO *2 (Select Out)</td><td>Output</td><td>86</td><td>Outputs a high-level signal while the $\overline{SEL}$ signal is active, and makes the $\overline{SEL}$ signal driver output-enabled.</td></tr>
<tr><td>IDSTR *2 (ID Strobe)</td><td>Output</td><td>82</td><td>Output pin for strobe signal which maintains its own SCSI ID when arbitration is executed when differential bus is used. Outputs a high-level signal during the arbitration period and makes the data bus signal driver of the SCSI corresponding to its own ID output-enabled.</td></tr>
<tr><td>INIT *2 (Initiator)</td><td>Output</td><td>83</td><td>Outputs a high-level signal during initiator operation and makes the drivers of the signals ($\overline{ANT}$, $\overline{ACK}$) used during initiator operation output-enabled.</td></tr>
</table>

(to be continued)

(cont'd)

Name	Input/ Output	Pin No.	Function
TGT *2 (Target)	Output	84	Outputs a high-level signal during target operation and makes the drivers of the signals ($\overline{MSG}$, $\overline{C}/D$, $\overline{I}/O$, $\overline{REQ}$) used during target operation output-enabled.
SBOE *2 (SCSI Bus Out Enable)	Output	80	Outputs a high-level signal during data transfer mode and makes the SCSI data bus driver output-enabled.
$\overline{SBIE}$ *2 (SCSI Bus In Enable)	Output	81	In arbitration, outputs a low-level signal during data reception mode and makes the SCSI data bus receiver input-enabled.

*1: An output open-drain type driver and input Schmitt type receiver are incorporated, allowing direct connection to a single-end type SCSI bus.

2: TTL level output pin which outputs an enable signal for an external differential driver. Leave open if an external differential driver is not used.

2.3 OTHER PINS

<table>
<tr><th>Name</th><th>Input/
Output</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>$\overline{\text{RESET}}$</td><td>Input</td><td>89</td><td>System reset input pin</td></tr>
<tr><td>$\overline{16B}$</td><td>Input</td><td>2</td><td rowspan="2">Bus mode setting input pins
The bus mode is changed according to the status of these pins as shown below.

<table><tr><th>$\overline{16B}$</th><th>$\overline{32B}$</th><th>Bus Mode</th></tr><tr><td>H</td><td>H</td><td>8-bit bus mode</td></tr><tr><td>L</td><td>H</td><td>16-bit bus mode</td></tr><tr><td>H</td><td>L</td><td>32-bit bus mode</td></tr><tr><td>L</td><td>L</td><td>Use prohibited</td></tr></table></td></tr>
<tr><td>$\overline{32B}$</td><td>Input</td><td>1</td></tr>
<tr><td>CLK (Clock)</td><td>Input</td><td>88</td><td>External clock input pin</td></tr>
<tr><td>V_{DD}</td><td>—</td><td>17, 37,
42, 93</td><td>Positive power supply pin</td></tr>
<tr><td>GNDO</td><td>—</td><td>13, 22,
30, 39,
40, 49,
90, 91,
100</td><td>Main ground pin</td></tr>
<tr><td>GND1</td><td>—</td><td>54, 58,
61, 64,
67, 71,
75, 79</td><td>Driver/receiver system ground pin</td></tr>
</table>

2.4 STATUS OF OUTPUT AND INPUT/OUTPUT PINS AFTER RESET

Pin Name	Status After Reset
$\overline{SB0}$ to $\overline{SB7}$, $\overline{SBP}$	High impedance (input)
$\overline{ATN}$, $\overline{ACK}$, $\overline{REQ}$, $\overline{MSG}$, $\overline{C}$/D, $\overline{I}$/O, $\overline{BSY}$, $\overline{SEL}$, $\overline{RST}$	High impedance (input)
D0 to D31, DP0 to DP3	High impedance (input)
INT	Low level
$\overline{DMARQ}$	High level
$\overline{EOP}$	High impedance (open-drain output)

CHAPTER 3. INTERNAL BLOCK FUNCTIONS

3.1 SCSI DRIVER/RECEIVER

Comprises open-drain type drivers (48 mA sink current) for driving a single-end SCSI bus conforming to the SCSI-2 specification, Schmitt type receivers with hysteresis characteristics. This block outputs signals to control an external differential driver.

3.2 ARBITRATION AND SELECTION CONTROL

Controls the execution sequence for the arbitration phase, selection phase and relation phase. Consists of a timing generator and sequencer.

3.3 BUS PHASE CONTROL

Controls and monitors the SCSI bus phases. Outputs signals which stipulate the bus phase, and also monitors the bus phase and detects bus phase transitions.

3.4 SCSI TRANSFER CONTROL

Controls data transfers on the SCSI bus in each information transfer phase (data in, data out, command, status, message in, and message out). Performs transfer protocol control by means of the $\overline{REQ}$ and $\overline{ACK}$ signals, and data transfer execution/stoppage control according to the SCSI FIFO buffer status. Also incorporates a 24-bit transfer counter, and manages the number of transfer data bytes on the SCSI bus.

The transfer counter counts the number of transmit/receive data bytes transferred between the SCSI-side FIFO buffer and the SCSI bus. Thus, the time to output all the data stored in the FIFO buffer onto the SCSI bus is the only delay before the contents of the transfer counter become 0 after the last data has been written from the CPU to the uPD72611.

3.5 SCSI DATA BUS FIFO BUFFER (SCSI FIFO BUFFER)

This is a 9-bit x 8-level asynchronous FIFO buffer which absorbs the difference between data transfer timing on the SCSI bus and data transfer timing on the internal uPD72611 bus. it is also used for queuing receive data in a synchronous transfer.

In the parity through mode, the parity is shifted at the same time as the data.

3.6 CMD/MSG DECODER

Decodes a received SCSI-2 command or message, and generates a decode signal which stipulates the next sequence.

3.7 SCSI DATA BUS PARITY GENERATOR/CHECKER

When not in the parity through mode, this block generates the parity to be added to data to be sent onto the SCSI data bus and sends it onto the SCSI bus; in the parity through mode, it sends the parity added by the host CPU onto the SCSI bus. In addition, it checks the parity added to data read from the SCSI data bus.

3.8 MAIN CONTROL BLOCK

This is the microprogram control sequencer. It generalizes the operation of each block and generates a control sequence.

3.9 INTERNAL TRANSFER CONTROL

Controls data transfers between the SCSI FIFO buffer and the host FIFO buffer and indirect access registers. When the host CPU side is set to 16- or 32-bit mode, this block controls data 8-bit/16-bit conversion or 8-bit/32-bit conversion.

3.10 DIRECT ACCESS REGISTERS

Registers such as the command register, status register, etc., which can be directly accessed by the host CPU.

3.11 INDIRECT ACCESS REGISTERS

Registers which cannot be accessed directly by the host CPU, but are accessed via the WINDOW1 and WINDOW2 direct access registers.

3.12 HOST DATA BUS FIFO BUFFER (HOST FIFO BUFFER)

This is a 36-bit x 8-level asynchronous FIFO buffer which improves the utilization of the host bus. In the 8-bit mode it functions as a 9-bit x 8-level FIFO buffer, using only the low-order 9 bits, while in the 16-bit mode it functions as an 18-bit x 8-level FIFO buffer, using only the low-order 18 bits.

In the parity through mode, the parity is shifted at the same time as the data.

3.13 INTERRUPT CONTROL

Controls interrupt signal setting/resetting.

3.14 READ/WRITE CONTROL

Controls read/write operations on various internal registers. Also performs 8-bit access control in the 16-/32-bit mode.

3.15 BUS-SIZE GENERATOR

Performs bus width conversion in accordance with the bus mode.

3.16 HOST DATA BUS PARITY GENERATOR/CHECKER

When not in the parity through mode, this block generates the parity to be added to data to be sent onto the host bus and sends it onto the host bus; in the parity through mode, it sends the added parity onto the host bus. In addition, it checks the parity added to data read from the host bus.

3.17 DMA REQUEST CONTROL

Generates a DMA request signal ($\overline{\text{DMARQ}}$) in accordance with the FIFO buffer status. Also performs command operation termination control by means of the $\overline{\text{EOP}}$ signal.

3.18 CLOCK GENERATOR

Generates from the system clock input from the CLK pin a 2-phase clock of the same frequency as the system clock and a 2-phase clock of half the frequency of the system clock for internal block control.

CHAPTER 4. INTERNAL REGISTER CONFIGURATION

The uPD72611 incorporates 39 8-bit registers and an 8-/16-/32-bit host FIFO buffer. These registers can be classified into direct access registers which can be directly accessed by the host CPU, and indirect access registers which are accessed via an address pointer.

Valid registers when the uPD72611 is busy (controller status register CBSY bit = 1) are the direct access registers shown below:

- DF0 (DATA FIFO 0)
- DF1 (DATA FIFO 1)
- DF2 (DATA FIFO 2)
- CST (Controller Status)
- IST (Interrupt Status)
- CMD (Command Register)

However, when the uPD72611 is busy a write should not be performed on any register other than DF0, DF1, DF2 or CMD. Also, when the uPD72611 is busy a read on a register other than DF0, DF1, DF2, CST or IST is invalid.

4.1 DIRECT ACCESS REGISTERS

Direct access registers can be directly accessed by the CPU. These registers are listed below.

Table 4-1 Direct Registers

Address				R/W	Symbol	Name
A3	A2	A1	A0			
0	0	0	0	R/W	DF0	Data FIFO 0 register
0	0	0	1	R/W	DF1	Data FIFO 1 register
0	0	1	0	R	CST	Controller status register
0	0	1	1	R/W	ADR	Address register
0	1	0	0	R/W	WIN1	Window 1
0	1	0	1		WIN2	Window 2
0	1	1	0	R	TP	Terminated phase register
				W	DID	Destination ID register
0	1	1	1	R	IST	Interrupt status register
				W	CMD	Command register
1	0	0	0	R	EXST	Extended status register
1	0	0	1	——	——	Use prohibited
1	0	1	0			
1	0	1	1			
1	1	0	0	R/W	DF2	Data FIFO 2 register
1	1	0	1			
1	1	1	0			
1	1	1	1			

NOTE: When the uPD72611 is busy (when the CBSY bit of the CST register is 1), a register other than DF0, DF1, DF2 or CMD should not be written to.

(1) Data FIFO 0/1/2 registers (DF0/DF1/DF2)

These are 32-bit registers to/from which information (data or a command, status or message) accessed via the SCSI data bus is written or read. In the 8-bit bus mode, only the DF0 register is used and byte accesses are performed. In the 16-bit bus mode, the DF0 and DF1 registers are used and half-word accesses are performed. In the 32-bit bus mode, the DF0, DF1 and DF2 registers are used and word accesses are performed.

When a data word to be output to the SCSI bus is written to DF0, DF1 or DF2 in the 16- or 32-bit bus mode, output to the SCSI bus is performed in order starting with the low-order 8-bit data. And when data input from the SCSI bus is read, setting is performed starting with the lower byte, in order starting with the first 8 bits input from the SCSI bus.

In the 16-bit bus mode the registers function as 16-bit registers and byte accesses are not possible. Similarly, in the 32-bit bus mode the registers function as 32-bit registers and byte or half-word accesses are not possible.

These registers are emptied by $\overline{\text{RESET}}$ input or execution of the CHIP RESET or CLEAR FIFO command.

Figure 4-1 DF0 Format

Address	7	6	5	4	3	2	1	0	
00H	D7	D6	D5	D4	D3	D2	D1	D0	(R/W)

This register holds the 8-bit data in the 8-bit bus mode, and the lower byte of the 16-bit data in the 16-bit bus mode.

Figure 4-2 DF1 Format

Address	7	6	5	4	3	2	1	0	
01H	D15	D14	D13	D12	D11	D10	D9	D8	(R/W)

This register holds the upper byte of the 16-bit data in the 16-bit bus mode.

Figure 4-3 DF2 Format

Address	7	6	5	4	3	2	1	0	
0CH	D7	D6	D5	D4	D3	D2	D1	D0	(R/W)
0DH	D15	D14	D13	D12	D11	D10	D9	D8	(R/W)
0EH	D23	D22	D21	D20	D19	D18	D17	D16	(R/W)
0FH	D31	D30	D29	D28	D27	D26	D25	D24	(R/W)

This register holds the 32-bit data in the 32-bit bus mode.

(2) Controller status register (CST)

This is an 8-bit register which indicates the status of the uPD72611. It is a read-only register and a data write to this register is invalid.

This register is set to 82H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command, and is set to 42H on completion of a reset operation.

Figure 4-4 CST Format

Address	7	6	5	4	3	2	1	0	
02H	CBSY	INTRQ	CST1	CST0	ATNC	FFUL	FEMP	DRQ	(R)

CBSY	uPD72611 Command Execution Status
0	Idle status (command wait or type A command being executed)
1	Busy status (type B or type C command being executed)*

INTRQ	Presence/Absence of Interrupt Request to CPU
0	No interrupt request
1	Interrupt request present

CST1	CST0	uPD72611 Operating Status
0	0	Disconnected (D)
0	1	Initiator (I)
1	0	Target (T)

ANTC	$\overline{\text{ATN}}$ Pin Status
0	$\overline{\text{ATN}}$ signal inactive ($\overline{\text{ATN}}$ pin high)
1	$\overline{\text{ATN}}$ signal active ($\overline{\text{ATN}}$ pin low)

FFUL	FEMP	CPU-Side FIFO Buffer Status
0	0	Neither full nor empty of data
0	1	Empty
1	1	Full of data

DRQ	DF0/DF1/DF2 Register CPU Bus Access Request
0	DF0/DF1/DF2 access disabled
1	Request for transmit data write to or receive data read from DF0/DF1/DF2

*: When the uPD72611 is busy an access to direct access registers DF0, DF1, DF2, CST, IST and CMD and execution of a type A command are possible.

(3) Address register (ADR)

This is an 8-bit register in which the address of an indirect access register is set. When an indirect access register is accessed, its address is set in the ADR register and a window (WIN1/WIN2) is accessed.

Bit 7 specifies the mode when an indirect access register is accessed, and bits 5 to 0 specify the address of the indirect access register to be accessed.

In the auto-increment mode, the contents of the low-order 6 bits are incremented automatically each time an access is performed (+1 in the 8-bit bus mode, and +2 in the 16-/32-bit bus mode).

This register is reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-5 ADR Format

Address	7	6	5	4	3	2	1	0	
03H	AINC	0	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	(R/W)

AINC	Indirect Access Register Access Mode Specification
0	Normal mode (address not automatically updated)
1	Auto-increment mode (address automatically updated)

ADR5 to ADR0	Indirect Access Register Access Specification
0 0 0 0 0 0	00H
to	to
1 1 1 1 1 1	3FH

(4) Windows (WIN1, WIN2)

These are registers used for accessing an indirect access register.

When WIN1 is accessed, the indirect access register corresponding to the address of the ADR register is accessed.

When WIN2 is accessed, the indirect access register corresponding to the address of the ADR register plus 1 is accessed.

Figure 4-6 WIN1 & WIN2 Format

Address	7	6	5	4	3	2	1	0	
04H	WIN1								(R/W)
05H	WIN2								(R/W)

(5) Terminated phase register (TP)

This register shows the execution phase when command processing terminates.

This register is reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-7 TP Format

Address	7	6	5	4	3	2	1	0	
06H	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0	(R)

TP			Command	Execution Phase
7654	3210	HEX		
0000	0001	01H	SCSI RESET	SCSI reset phase
0001	0001	11H	SELECT	Arbitration phase
0001	0010	12H		Target selection phase
0010	0001	21H	TRANSFER	Information transfer phase
0011	0001	31H	AUTO INITIATOR	Arbitration phase
0011	0010	32H		Target selection phase
0011	0011	33H		Identify message transmission phase
0011	1000	38H		Queue tag message 1st byte transmission phase
0011	1001	39H		Queue tag message 2nd byte transmission phase
0011	0100	34H		Command transmission phase
0011	0101	35H		Data transmission/reception phase
0011	0110	36H		Status reception phase
0011	0111	37H		Command complete message reception phase

(to be continued)

(cont'd)

TP			Command	Execution Phase
7654	3210	HEX		
0011	0101	35H	AUTO INITIATOR 2	Data transmission/reception phase
0011	0110	36H		Status reception phase
0011	0111	37H		Command complete message reception phase
0100	0001	41H	RESELECT	Arbitration phase
0100	0010	42H		Initiator reselection phase
0101	0001	51H	RECEIVE	Information reception phase
0110	0001	61H	SEND	Information transmission phase
0111	0001	71H	AUTO TARGET	Selected waiting phase
0111	0010	72H		Identify message reception phase
0111	0011	73H		Command reception phase
0111	0100	74H		Parity error termination in SCSI-2 1st command reception
0111	0101	75H		Queue tag message 1st byte reception phase
0111	0110	76H		Queue tag message 2nd byte reception phase
0111	0111	77H		Command reception phase (in 3-byte message reception)
0111	1000	78H		Parity error termination in SCSI-2 1st command reception (in 3-byte message reception)
1010	0001	A1H	AUTO TARGET 2	Status transmission phase
1010	0010	A2H		Command complete message transmission phase

(to be continued)

(cont'd)

TP			Command	Execution Phase
7654	3210	HEX		
1000	0001	81H	RE-RECEIVE	Arbitration phase
1000	0010	82H		Initiator reselection phase
1000	0011	83H		Identify message transmission phase
1000	0101	85H		Queue tag message 1st byte reception phase
1000	0110	86H		Queue tag message 2nd byte reception phase
1000	0100	84H		Data reception phase
1001	0001	91H	RE-SEND	Arbitration phase
1001	0010	92H		Initiator reselection phase
1001	0011	93H		Identify message transmission phase
1001	0101	95H		Queue tag message 1st byte reception phase
1001	0110	96H		Queue tag message 2nd byte reception phase
1001	0100	94H		Data transmission phase

(6) Destination ID register (DID)

This is a write-only register in which the ID of the target to be selected or the ID of the initiator to be reselected is set. It can also specify masking of the interrupt request signal (INT). At this time, the presence or absence of an interrupt request can be checked by means of the INTRQ bit in the CST register.

This register is reset to 80H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-8 DID Format

Address	7	6	5	4	3	2	1	0	
06H	INTM	0	0	0	0	DID2	DID1	DID0	(W)

INTM	Interrupt Request Signal Mask Function Specification
0	Interrupt requests not masked (INT signal is output when an interrupt request is generated)
1	Interrupt request masked (INT signal is not output when an interrupt request is generated)

DID2 to DID0	Setting of ID Number of SCSI Device to be Selected/Reselected
0 0 0	0
to	to
1 1 1	7

NOTE: Ensure that 0 is written to bits 6 through 3.

(7) Interrupt status register (IST)

This is an 8-bit read-only register which indicates the interrupt request generation source.

Bit 7 (SRI) indicates the interrupt generation source group. The contents indicated by bits 6 to 0 depend on the value of this bit.

Figure 4-9 IST Format

Address	7	6	5	4	3	2	1	0	
07H	SRI	ISR6	IST5	IST4	IST3	IST2	IST1	IST0	(R)

SRI	Interrupt Input Generation Source Group
0	Interrupt request due to command termination (normal termination or abnormal termination)
1	Interrupt request due to service request from SCSI side to CPU

(a) Interrupt request signal and IST contents

- When an interrupt source is set in IST, the interrupt request signal (INT) is driven high and the INTRQ bit in the controller status register (CST) is set to 1 (referred to below as the INT status).

- The INT status is reset when the IST contents are read from the CPU side.

- The INT status is not reset by issuance of a type A command (except CHIP RESET and DISCONNECT).

- The INT status, with the exceptions described below, is reset by issuance of a type B or type C command or the DISCONNECT command.

  An INT status due to one of the following interrupt sources is not reset (remains held) by issuance of a command other than CHIP RESET.

- Reset
- SCSI reset condition
- Disconnected
- Selected
- Reselected
- Message reception

The IST format and interrupt source contents are shown in Tables 4-2 and 4-3.

NOTE: For command types, see Chapter 5 "Commands".

Table 4-2 IST Format and INT Status

SRI	IST *1							Interrupt Request Generation Source	INT Status *2
	6	5	4	3	2	1	0		
0	0	0	0	AT	0	0	0	Normal command termination	Reset
0	0	0	0	AT	0	0	1	Command break	Reset
0	0	0	1	AT	0	0	0	Invalid command	Reset
0	0	1	0	AT	0	0	0	FIFO buffer overrun/underrun	Reset
0	0	1	0	AT	0	0	1	Synchronous mode offset error	Reset
0	0	1	0	AT	0	1	0	SCSI bus parity error	Reset
0	0	1	0	AT	0	1	1	CPU bus parity error	Reset
0	0	1	0	0	1	0	0	Bus free timeout error	Reset
0	0	1	0	0	1	0	1	Selection/reselection timeout error	Reset
0	0	1	0	AT	1	1	0	$\overline{\text{REQ}}$/$\overline{\text{ACK}}$ timeout error	Reset
0	0	1	1	0	0	0	0	Data out phase error	Reset
0	0	1	1	0	0	0	1	Data in phase error	Reset
0	0	1	1	0	0	1	0	Command phase error	Reset
0	0	1	1	0	0	1	1	Status phase error	Reset

(to be continued)

Table 4-2 IST Format and INT Status (cont'd)

SRI	IST *1							Interrupt Request Generation Source	INT Status *2
	6	5	4	3	2	1	0		
0	0	1	1	0	1	1	0	Message out phase error	Reset
0	0	1	1	0	1	1	1	Message in phase error	Reset
0	1	0	0	AT	0	0	0	Unsupported group	Reset
1	0	0	0	0	0	0	0	Reset	Hold
1	0	0	0	0	0	0	1	SCSI reset condition	Hold
1	0	0	1	0	0	0	0	Disconnected	Hold
1	0	0	1	0	0	0	1	Reselected	Hold
1	0	0	1	AT	0	1	0	Selected	Hold
1	0	1	0	0	0	0	0	Data out phase start	Reset
1	0	1	0	0	0	0	1	Data in phase start	Reset
1	0	1	0	0	0	1	0	Command phase start	Reset
1	0	1	0	0	0	1	1	Status phase start	Reset
1	0	1	0	0	1	1	0	Message out phase start	Reset
1	0	1	0	0	1	1	1	Message in phase start	Reset
1	1	0	0	AT	0	0	0	Message reception	Hold

*1: When AT = 0: Non-attention condition
When AT = 1: Attention condition

2: Transition due to issuance of type B or type C command or DISCONNECT command.

NOTE: The AT bit is always 0 when the uPD72611 has initiator status.

Table 4-3 Interrupt Sources

Interrupt Request Generation Source	Description
Normal command termination	A type B or type C command has terminated normally.
Command break	A type B or type C command has been interrupted during execution by a break (by issuing a BREAK command).
Invalid command	The previously issued command is invalid.
FIFO buffer overrun/ underrun	Overrun/underrun has occurred during a write or read operation on the CPU-side FIFO buffer.
Synchronous mode offset error	During an SCSI synchronous transfer, the offset number has exceeded the value set in TMOD.
SCSI bus parity error	A parity error has been detected on the SCSI bus side.
CPU parity error	A parity error has been detected on the CPU bus side.
Bus free timeout error	The time set in BFTOUT has elapsed before detection of the SCSI bus free phase after issuance of a command including selection/reselection.
Selection/reselection timeout error	During selection/reselection execution, the time set in SRTOUT has elapsed after a low-to-high transition of the uPD72611 $\overline{\text{BSY}}$ signal without a response from the far-end SCSI terminal by means of a high-to-low transition of the $\overline{\text{BSY}}$ signal.
$\overline{\text{REQ}}/\overline{\text{ACK}}$ timeout error	The time set in RATOUT has elapsed before the next high-to-low transition of the $\overline{\text{REQ}}$ signal after a high-to-low transition of this signal when the device is the initiator, or before the next high-to-low transition of the $\overline{\text{ACK}}$ signal after a high-to-low transition of this signal when the device is the target.

(to be continued)

Table 4-3 Interrupt Sources (cont'd)

<table>
<tr><th>Interrupt Request Generation Source</th><th>Description</th></tr>
<tr><td>Phase error</td><td>A bus phase transition has occurred during execution of a transfer on the SCSI bus.

<table>
<tr><th>IST2</th><th>IST1</th><th>IST0</th><th>Status After Phase Transition</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Data out phase</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Data in phase</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Command phase</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Status phase</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Message out phase</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Message in phase</td></tr>
</table></td></tr>
<tr><td>Unsupported group</td><td>In type C command execution an unsupported CDB has been sent/received.</td></tr>
<tr><td>Reset</td><td>The uPD72611 has been reset by the $\overline{\text{RESET}}$ signal or the CHIP RESET command.</td></tr>
<tr><td>SCSI reset condition</td><td>A reset condition has been generated by another SCSI terminal.</td></tr>
<tr><td>Disconnect</td><td>Disconnected from the target side.</td></tr>
<tr><td>Reselected</td><td>Reselected from another SCSI terminal (target).</td></tr>
<tr><td>Selected</td><td>Selected from another SCSI terminal (initiator).</td></tr>
<tr><td>Phase start</td><td>A transfer phase has been started by control from the target side.

<table>
<tr><th>IST2</th><th>IST1</th><th>IST0</th><th>Started Phase</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Data out phase</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Data in phase</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Command phase</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Status phase</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Message out phase</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Message in phase</td></tr>
</table></td></tr>
<tr><td>Message reception</td><td>A message has been received ($\overline{\text{ACK}}$ signal retains active status).</td></tr>
</table>

(b) Commands and IST contents

IST contents when a uPD72611 command has terminated normally are shown below by command and type (see Chapter 5 "Commands").

Table 4-4 IST Contents After Normal Command Termination

Type	Command	IST Format	Interrupt
A	CHIP RESET	1 0 0 0 0 0 0 0	Reset
	BREAK	0 0 0 0 AT 0 0 1	Command break
	DISCONNECT	—	No interrupt
	CLEAR FIFO	—	No interrupt
	SET ATN	—	No interrupt
	RESET ACK	—	No interrupt
B	SCSI RESET	0 0 0 0 0 0 0 0	Normal termination of command
	SELECT	0 0 0 0 AT 0 0 0	Normal termination of command
	TRANSFER	0 0 0 0 AT 0 0 0 1 1 0 0 AT 0 0 0	Normal termination of command Message reception ... In case of message in
	RESELECT	0 0 0 0 AT 0 0 0	Normal termination of command
	SEND	0 0 0 0 AT 0 0 0	Normal termination of command

(to be continued)

Table 4-4 IST Contents After Normal Command Termination (cont'd)

Type	Command	IST Format	Interrupt
C	AUTO INITIATOR	0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0	Normal termination of command Message reception ... When messages in contents are other than "command complete"
	AUTO INITIATOR 2	0 0 0 0 0 0 0 0 1 1 0 0 0 0 0 0	Normal termination of command Message reception ... When messages in contents are other than "command complete"
	AUTO TARGET	0 0 0 0 AT 0 0 0	Normal termination of command
	AUTO TARGET 2	0 0 0 0 AT 0 0 0	Normal termination of command
	RE-RECEIVE	0 0 0 0 AT 0 0 0	Normal termination of command
	RE-SEND	0 0 0 0 AT 0 0 0	Normal termination of command

Remarks: Type A: Commands which perform uPD72611 status control

Type B: Commands which perform basic SCSI protocol control

Type C: Commands which automatically execute multiple type B commands in a sequence

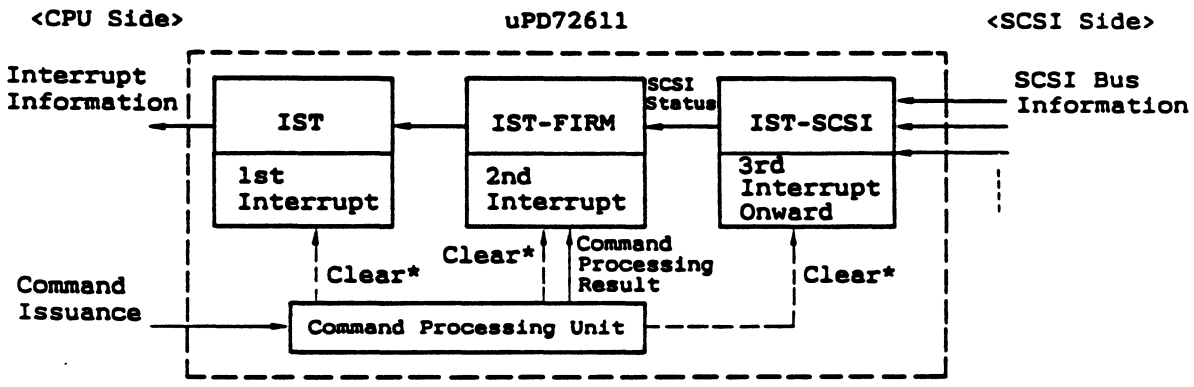
(c) When multiple interrupts are generated

In addition to interrupts due to the termination of a command (SRI = 0), the uPD72611 can also hold multiple interrupt sources when an interrupt (SRI = 1) is generated due to a service request from the SCSI bus.

There are three registers which hold interrupt sources in the uPD72611, configured as shown in Figure 4-10.

Figure 4-10 Registers for Holding Interrupt Sources and Register Configuration

Register	Function
IST	An interrupt request generation source can be read directly from the CPU side.
IST-FIRM	Used by internal uPD72611 firmware to hold an interrupt source temporarily. Cannot be accessed directly from the CPU side.
IST-SCSI	Latches the SCSI bus status. Cannot be accessed directly from the CPU side.



*: See Table 4-5 for the interrupt sources cleared.

When IST is read from the CPU side, IST contents are cleared and interrupt sources in IST-FIRM are shifted consecutively. Each time a new interrupt source is stored in IST the uPD72611 assumes the INT status.

Interrupt sources in IST and IST-FIRM may be cleared by issuance of a type B or type C command or the DISCONNECT command as well as by a read operation from the CPU (see Table 4-5 for details). When an interrupt source is cleared by issuance of a command, the interrupt sources in the other registers are shifted, as in the case of a read by the CPU.

If there is an interrupt source in IST-FIRM, the issued command is not executed. Also, if "command normal termination", "invalid command", "unsupported group" or "message reception" is held in IST-FIRM, the uPD72611 remains busy.

Table 4-5 Commands Which Clear Interrupt Source

Interrupt Request Generation Source	Register for Holding Interrupt Source		
	IST	IST-FIRM *1	IST-SCSI
Normal command termination *2	B, C, DIS	DIS	——
Command break	B, C, DIS	DIS	——
Invalid command *2	B, C, DIS	DIS	——
FIFO buffer overrun/underrun	B, C, DIS	DIS	——
Synchronous mode offset error	B, C, DIS	DIS	——
SCSI bus parity error	B, C, DIS	DIS	——
Host bus parity error	B, C, DIS	DIS	——

(to be continued)

Table 4-5 Commands Which Clear Interrupt Source (cont'd)

Interrupt Request Generation Source	Register for Holding Interrupt Source		
	IST	IST-FIRM *1	IST-SCSI
Bus free timeout error	B, C, DIS	DIS	—
Selection/reselection mode timeout error	B, C, DIS	DIS	—
$\overline{REQ}/\overline{ACK}$ timeout error	B, C, DIS	DIS	—
Data out phase error	B, C, DIS	DIS	—
Data in phase error	B, C, DIS	DIS	—
Command phase error	B, C, DIS	DIS	—
Status phase error	B, C, DIS	DIS	—
Message out phase error	B, C, DIS	DIS	—
Message in phase error	B, C, DIS	DIS	—
Unsupported group *2	B, C, DIS	DIS	—
Reset	Hold	—	—
SCSI reset condition	Hold	Hold	Hold
Disconnect	Hold	Hold	Hold
Reselected	Hold	Hold	Hold
Selected	Hold	Hold	Hold
Data out phase start	B, C, DIS	DIS	Hold
Data in phase start	B, C, DIS	DIS	Hold
Command phase start	B, C, DIS	DIS	Hold
Status phase start	B, C, DIS	DIS	Hold
Message out phase start	B, C, DIS	DIS	Hold
Message in phase start	B, C, DIS	DIS	Hold
Message reception *2	Hold	Hold	—

B, C: An interrupt source due to issuance of a type B or type C command is cleared.

DIS : An interrupt source due to issuance of the DISCONNECT command is cleared.

Hold: Not cleared by command issuance (except CHIP RESET).

—— : Interrupt is not held.

*1: When an interrupt source is stored in IST-FIRM, a type B or C command is not executed.

2: When this interrupt source is stored in IST-FIRM, the uPD72611 remains busy.

The INT-SCSI register latches the third and subsequent interrupt sources, and these interrupt sources are assigned priorities as described below. These priorities determine the order in which other interrupt sources are cleared or transferred to the IST-FIRM register, as shown in Table 4-6.

o Interrupt request generation sources latched in IST-SCSI, and their priority

① SCSI reset condition
② Disconnect
③ Selected/reselected
④ Individual information phase start

Table 4-6 Conditions for Holding Multiple Interrupt Sources (IST-FIRM)

n = 3 or more

nth Interrupt \ Interrupt (n + 1)	① SCSI Reset Condition	② Disconnect	③ Selected/ Reselected	④ Information Phase Start
① SCSI reset condition		—	Hold	—
② Disconnect	Clear		Hold	—
③ Selected/reselected	Clear	Clear		Parallel latch
④ Information phase start	Clear	Clear	—	Clear *

Clear : The nth interrupt source is cleared by interrupt source (n + 1).
→ Only interrupt source (n + 1) is held in IST-FIRM.

— : Not generated in SCSI standard. If generated, an interrupt is ignored by the uPD72611.

Hold : Not latched in IST-SCSI until the nth interrupt source is transferred to IST-FIRM.
→ If the SCSI status changes before latching, that information does not remain.

Parallel latch: Both latched, and transferred to IST-FIRM in order of priority.

*: Not generated in the SCSI standard, but if consecutively accessed from the target in the wrong phase ($\overline{REQ}$ signal: H → L), interrupt source (n + 1) is held.

(8) Command register (CMD)

This is an 8-bit register used by the CPU to write a command to the uPD72611. See Chapter 5 "Commands" for details of the commands.

Figure 4-11 CMD Format

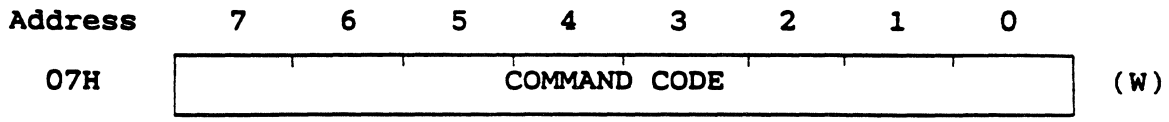


Table 4-7 Outline of Command Code

Command Code								Command	Outline of Operation
b7	b6	b5	b4	b3	b2	b1	b0		
0	0	0	0	0	0	0	0	CHIP RESET	Chip reset
0	0	0	0	0	0	0	1	BREAK	Command break
0	0	0	0	0	0	1	0	DISCONNECT	SCSI bus release
0	0	0	0	0	1	0	1	CLEAR FIFO	FIFO buffer clearance
0	0	0	0	1	0	0	0	SCSI RESET	SCSI bus reset
0	0	0	0	0	0	1	1	SET ATN	$\overline{\text{ATN}}$ signal setting
0	0	0	0	0	1	0	0	RESET ACK	$\overline{\text{ACK}}$ signal reset
0	0	0	1	AT	0	0	0	SELECT	Target selection
C1	C0	0	1	0	0	1	0	TRANSFER	Data transmission/reception (initiator)
C1	C0	0	1	AT	1	0	0	AUTO INITIATOR	Initiator standard sequence
C1	C0	0	1	0	1	0	1	AUTO INITIATOR 2	Initiator standard sequence (after reselection)
0	0	1	0	0	0	0	0	RESELECT	Initiator reselection
C1	C0	1	0	1	MG	CD	0	RECEIVE	Data reception (target)
C1	C0	1	0	1	MG	CD	1	SEND	Data transmission (target)

(to be continued)

Table 4-7 Outline of Command Code (cont'd)

Command Code								Command	Outline of Operation
b7	b6	b5	b4	b3	b2	b1	b0		
0	0	1	1	0	0	0	0	AUTO TARGET	Target standard sequence
0	0	1	1	0	0	0	1	AUTO TARGET 2	Target standard termination sequence
C1	C0	1	1	1	0	0	0	RE-RECEIVE	Reselect → data reception (target)
C1	C0	1	1	1	0	0	1	RE-SEND	Reselect → data transmission (target)

C1: Count Select 1
C0: Count Select 0
AT: Attention
MG: Message
CD: Command/$\overline{\text{Data}}$

(9) Extended status (EXST)

This is an 8-bit read-only register which indicates the operating status of the uPD72611.

This register is reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command, or by writing a DISCONNECT (type A), type B or type C command into the CMD register.

Figure 4-12 EXST Format

Address	7	6	5	4	3	2	1	0	
08H	0	0	0	0	0	0	HBPER	SBPER	(R)

HBPER	Detection of Parity Error in Data Received from CPU Bus
0	Parity error not detected
1	Parity error detected

SBPER	Detection of Parity Error in Data Received from SCSI Bus
0	Parity error not detected
1	Parity error detected

4.2 INDIRECT ACCESS REGISTERS

Indirect access registers cannot be accessed directly by the CPU, but are accessed via the WINDOW1 and WINDOW2 direct access registers. The address is specified by the low-order 6 bits of the ADR register. A list of indirect access registers is given below.

These registers are reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Table 4-8 Indirect Access Registers

Address	R/W	Symbol	Name
00H	R/W	TST	Target status register
01H	R	SBST	SCSI bus status register
02H	R	SID	Source ID register
03H	R/W	MSG	Message register
04H to 0FH	R/W	CDB00 to CDB11	Command descriptor block (CDB)
10H	R/W	TMCD	Transfer mode register
11H	R	CTCL	Current transfer counter (low-order 8 bits)
	W	BTCL	Base transfer counter (low-order 8 bits)
12H	R	CTCM	Current transfer counter (middle 8 bits)
	W	BTCM	Base transfer counter (middle 8 bits)
13H	R	CTCH	Current transfer counter (high-order 8 bits)
	W	BTCH	Base transfer counter (high-order 8 bits)
14H	R/W	MSG2	Message 2 register
15H	R/W	MSG3	Message 3 register
16H	R/W	EXOD	Extended mode register

(to be continued)

Table 4-8 Indirect Access Registers (cont'd)

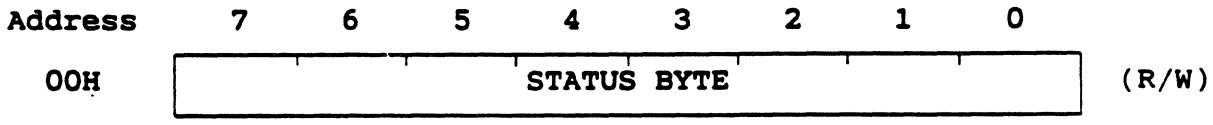
Address	R/W	Symbol	Name
17H to 1FH	-	——	Use prohibited
20H	R/W	BFTOUT	Bus free timeout register
21H	R/W	SRTOUT	Selection/reselection timeout register
22H	R/W	RATOUT	$\overline{REQ}$/$\overline{ACK}$ handshake timeout register
23H	R/W	CDBL	Command descriptor block length register
24H	R/W	MOD	Mode register
25H	R/W	PID	Physical ID register
26H to 3FH	-	——	Use prohibited

(1) Target status register (TST)

This is an 8-bit register which is used to store the target status received in the status phase during execution of the AUTO INITIATOR command or AUTO INITIATOR 2 command, or to set in advance the status to be sent in the status phase during execution of the AUTO TARGET 2 command.

This register is reset to 00H by $\overline{RESET}$ input or execution of the CHIP RESET command.

Figure 4-13 TST Format



(2) SCSI bus status register (SBST)

This is an 8-bit read-only register which indicates the status of each signal on the SCSI control bus. The status of control signals which indicate the bus phase ($\overline{BSY}$, $\overline{SEL}$, $\overline{MSG}$, $\overline{C}/D$, $\overline{I}/O$) and the control signal which indicates the bus condition ($\overline{ATN}$) can be read directly.

Figure 4-14 SBST Format

Address	7	6	5	4	3	2	1	0	
01H	BSY	SEL	REQ	ACK	ATN	MSG	C/D	I/O	(R)

	Status of Each Pin
0	Inactive (high)
1	Active (low)

(3) Source ID register (SID)

This is an 8-bit read-only register which stores the ID of the SCSI device which last selected the uPD72611. 0 is always read from bits 3 through 6.

This register is reset 00H by $\overline{RESET}$ input or execution of the CHIP RESET command.

Figure 4-15 SID Format

Address	7	6	5	4	3	2	1	0	
02H	S/R	0	0	0	0	SID2	SID1	SID0	(R)

S/B	Previous uPD72611 Selection/Reselection
0	Has not been selected or reselected (contents of SID2 to SID0 invalid)
1	Has been selected or reselected (contents of SID2 to SID0 valid)

SID2 to SID0	ID Number of Last SCSI Device Selected by uPD72611
000	0
to	to
111	7

(4) Message register (MSG)

This is an 8-bit register which sets or stores the message to be sent or received when a type C command which includes message transmission/ reception is executed.

When the AUTO INITIATOR command is executed, the message to be sent to the target after successful target selection must be set before the command is issued. The uPD72611 stores a message received during command execution.

When the AUTO INITIATOR 2 command is executed, this register stores the received message.

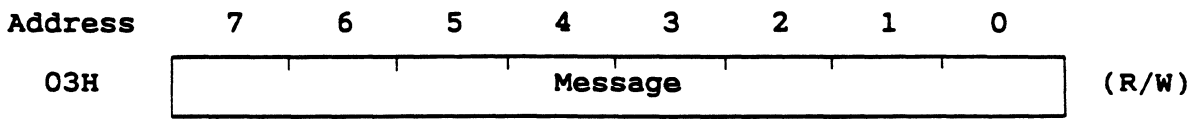
When the RE-RECEIVE or RESEND command is executed, the message to be sent after successful initiator reselection must be set before the command is issued.

When the AUTO TARGET command is executed, if the device is selected as the target by another SCSI device, this register stores the message received in the subsequent message in phase.

When the AUTO TARGET 2 command is executed, the message to be sent in the message in phase must be set before the command is issued.

This register is reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-16 MSG Format



(5) Command descriptor block registers (CDB00 to CDB11)

These are registers for setting or storing the CDB (Command Descriptor Block) of SCSI-2 commands.

In the command phase of the AUTO INITIATOR command, the contents of these registers are transmitted as the SCSI-2 command. In the command phase of the AUTO TARGET command, the SCSI-2 command received is stored in these registers.

These registers are reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-17 CDB Format

Address	7	6	5	4	3	2	1	0	
04H	CDB00								(R/W)
05H	CDB01								(R/W)
06H	CDB02								(R/W)
07H	CDB03								(R/W)
08H	CDB04								(R/W)
09H	CDB05								(R/W)
0AH	CDB06								(R/W)
0BH	CDB07								(R/W)
0CH	CDB08								(R/W)
0DH	CDB09								(R/W)
0EH	CDB10								(R/W)
0FH	CDB11								(R/W)

(6) Transfer mode register (TMOD)

This is an 8-bit register used to set the mode when a data transfer is performed.

This register is reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-18 TMOD Format

Address	7	6	5	4	3	2	1	0	
10H	SYNC	TPD2	TPD1	TPD0	HSYNC	TOF2	TOF1	TOF0	(R/W)

SYNC : Synchronous transfer mode specification bit

HSYNC: High-speed synchronous transfer mode specification bit

TPD : Data transfer period specification bits

TOF : $\overline{\text{REQ}}$/$\overline{\text{ACK}}$ pulse offset value specification

	SYNC	HSYNC	TPD2	TPD1	TPD0	Data Transfer Period (Clock Cycles)	Transfer Rate (Mbytes/s) at 20 MHz Operation
Synchronous transfer	1	0	0	0	0	16	1.25
					1		
				1	0	4	5.00
					1	6	3.33
			1	0	0	8	2.50
					1	10	2.00
				1	0	12	1.66
					1	14	1.42
High-speed synchronous transfer	1	1	0	0	0	8	2.50
					1		
				1	0	2	10.00
					1	3	6.66
			1	0	0	4	5.00
					1	5	4.00
				1	0	6	3.33
					1	7	2.85

NOTE: When SYNC = 0, asynchronous transfer is selected regardless of HSYNC and TPD0 to TPD2.

TOF2	TOF1	TOF0	$\overline{REQ}/\overline{ACK}$ Pulse Offset Value Specification in Synchronous/ High-Speed Synchronous Transfer Mode
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7
0	0	0	8

(7) Current transfer counter (CTCL, CTCM, CTCH)

This is a 24-bit transfer counter which counts the number of transfer data bytes in the information transfer phase. Its contents are decremented by 1 for each one-byte transfer on the SCSI data bus.

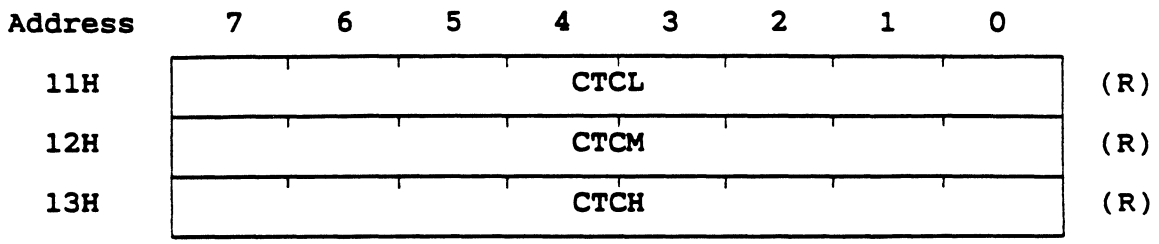
With a command which transfers information, the value set in the base transfer counter registers (BTCL/BTCM/BTCH) is placed in these registers. When a type C command is executed, however, a value automatically generated internally may be placed in these registers.

All commands which transmit information terminate the information transfer when the count value of this counter reaches zero. Similarly, all commands which receive information terminate the information transfer when the internal FIFO buffer becomes empty after the count of this counter reaches zero.

When information transfer is terminated by the BREAK command or due to the detection of an error, the number of untransmitted data bytes can be found by reading these registers.

These registers are set to FFH by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-19 CTCL/CTCM/CTCH Format



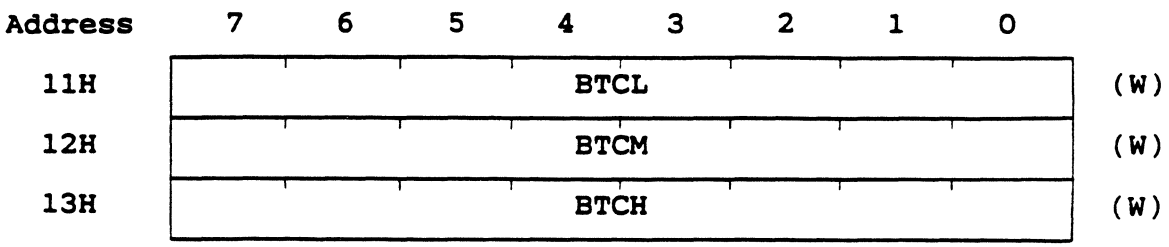
CTCL: Low-order 8 bits of current counter
CTCM: Middle 8 bits of current counter
CTCH: High-order 8 bits of current counter

(8) Base transfer counter (BTCL, BTCM, BTCH)

This is a 24-bit transfer counter used to set the number of transfer data bytes to be written to the current transfer counter (CTCL/CTCM/CTCH). The number of information bytes to be transferred by a TRANSFER command, SEND command or RECEIVE command are set (see Chapter 5 "Commands").

These registers are reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-20 BTCL/BTCM/BTCH Format



BTCL: Low-order 8 bits of base counter
BTCM: Middle 8 bits of base counter
BTCH: High-order 8 bits of base counter

BTCH	BTCM	BTCL	Transfer Bytes
00H	00H	00H	0
to	to	to	to
00H	00H	FFH	255
00H	01H	00H	256
to	to	to	to
00H	FFH	FFH	65,535
01H	00H	00H	65,536
to	to	to	to
FFH	FFH	FFH	16,777,215

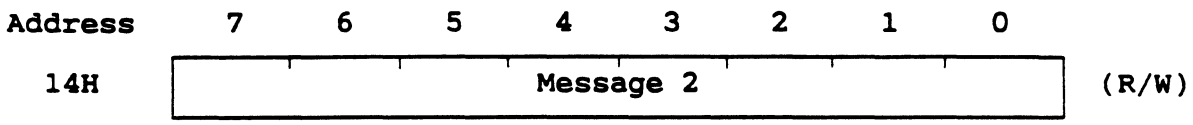
(9) Message 2 register (MSG2)

This is an 8-bit register for setting or storage of the first byte of the queue tag message sent/ received when a type C command which includes queue tag message transmission/reception is executed.

When a queue tag message is supported in the AUTO TARGET command, when the $\overline{ATN}$ signal is reactivated after the successful reception of an identify message, the queue tag message reception mode is entered automatically and the first byte of data received is stored in this register.

This register is reset to 00H by $\overline{RESET}$ input or execution of the CHIP RESET command.

Figure 4-21 MSG2 Format



(10) Message 3 register (MSG3)

This is an 8-bit register for setting or storage of the second byte (queue tag) of the queue tag message sent/received when a type C command which includes queue tag message transmission/reception is executed.

When a queue tag message is supported in the AUTO TARGET command, when the $\overline{ATN}$ signal is reactivated after the successful reception of an identify message, the queue tag message reception mode is entered automatically and the second data byte (queue tag) received is stored in this register.

This register is reset to 00H by $\overline{RESET}$ input or execution of the CHIP RESET command.

Figure 4-22 MSG3 Format

Address	7	6	5	4	3	2	1	0	
15H	Message 3								(R/W)

(11) Extended mode register (EXMOD)

This is an 8-bit register which sets the operating mode of functions which are extended in the uPD72611 as compared with the uPD72111.

0 must always be written to bits 4 through 7.

This register is reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-23 EXMOD Format

Address	7	6	5	4	3	2	1	0	
16H	0	0	0	0	MSG3	PTHR	PERP	BLKT	(R/W)

MSG3	Queuing Tag Message Supported/Not Supported
0	Queuing tag message not supported
1	Queuing tag message supported

PTHR	Parity Through Mode Specification
0	Parity through mode not specified
1	Parity through mode specified

PERP	Specification of Data Transfer Continuation after Parity Error Detection
0	Transfer discontinued on detection of parity error
1	Transfer continued despite detection of parity error

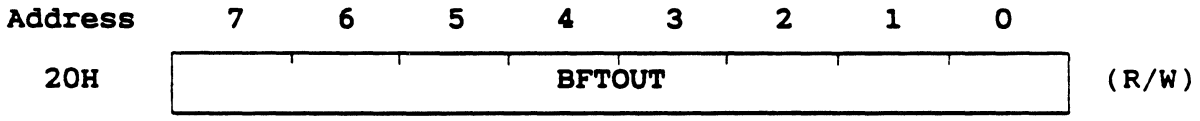
BLKT	DMA Transfer Mode Specification
0	Demand transfer mode
1	Block transfer mode (8-level FIFO buffer data transfer)

(12) Bus free timeout register (BFTOUT)

This is an 8-bit register used to set the decision time from issuance of a command including selection/reselection from the CPU side to detection of the SCSI bus free phase.

This register is reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-24 BFTOUT Format



BFTOUT	Bus Free Timeout Decision Time (20 MHz Operation)
00H	Timeout detection not performed
01H	6.553 mS
to	to (6.553 mS x BFTOUT set value) to
FFH	1,671,168 mS

(13) Selection/reselection timeout register (SRTOUT)

This is an 8-bit register used to set the timeout decision time for a selection/reselection operation. The decision time from a low-to-high transition of the uPD72611's own $\overline{BSY}$ signal during selection/reselection execution to a high-to-low transition of the $\overline{BSY}$ signal of the far-end SCSI terminal is set.

This register is reset to 00H by $\overline{RESET}$ input or execution of the CHIP RESET command.

Figure 4-25 SRTOUT Format

Address	7	6	5	4	3	2	1	0	
21H	SRTOUT								(R/W)

SRTOUT	Selection/Reselection Timeout Decision Time (20 MHz Operation)
00H	Timeout detection not performed
01H	6.553 mS
to	to (6.553 mS x SRTOUT set value) to
FFH	1,671,168 mS

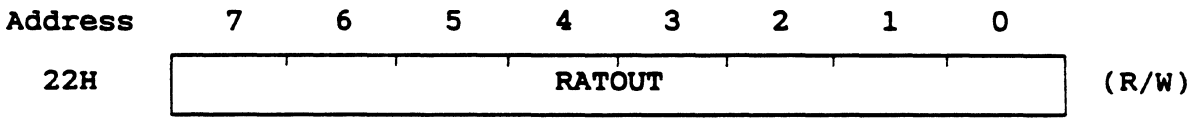
(14) $\overline{REQ}/\overline{ACK}$ timeout register (RATOUT)

This is an 8-bit register used to set the timeout decision time in the event of a hangup in handshaking using the $\overline{REQ}$ signal and $\overline{ACK}$ signal in an information transfer.

The decision time set is the period from a high-to-low transition of the $\overline{REQ}$ signal to the next high-to-low transition of the $\overline{REQ}$ signal in the initiator mode, or from a high-to-low transition of the $\overline{ACK}$ signal to the next high-to-low transition of the $\overline{ACK}$ signal in the target mode. If 00H is specified for the RATOUT register, the timeout detection function does not operate.

This register is reset to 00H by $\overline{RESET}$ input or execution of the CHIP RESET command.

Figure 4-26 RATOUT Format



RATOUT	$\overline{REQ}$/$\overline{ACK}$ Timeout Decision Time (16 MHz Operation)
00H	Timeout detection not performed
01H	410 uS
to	to (410 uS x RATOUT set value) to
FFH	104,448 uS

(15) Command descriptor block length register (CDBL)

This is an 8-bit register which is used to set parameters to support group 6 and group 7 SCSI-2 commands which are vendor-unique in the SCSI-2 specifications with the AUTO INITIATOR command and the AUTO TARGET command.

This register is reset to 00H by $\overline{RESET}$ input or execution of the CHIP RESET command.

Figure 4-27 CDBL Format

Address	7	6	5	4	3	2	1	0	
23H	CL73	CL72	CL71	CL70	CL63	CL62	CL61	CL60	(R/W)

CL73 to CL70	Group 7 SCSI Command CDB Length Specification
0 0 0 1	1 byte
to	to
1 1 0 0	12 bytes
1 1 0 1	Group 7 SCSI commands not supported (Unsupported Group Command error generated)
to	
1 1 1 1	
0 0 0 0	

CL63 to CL60	Group 6 SCSI Command CDB Length Specification
0 0 0 1	1 byte
to	to
1 1 0 0	12 bytes
1 1 0 1	Group 6 SCSI commands not supported (Unsupported Group Command error generated)
to	
1 1 1 1	
0 0 0 0	

(16) Mode register (MOD)

This is an 8-bit register which sets the uPD72611 operating mode.

This register is reset to 20H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-28 MOD Format

Address	7	6	5	4	3	2	1	0	
24H	DMA	HPS	HDP	DSP	NAM	SIM	RAEM	SAEM	(R/W)

DMA	Data Transfer Mode in Data In/Data Out Phase
0	Program I/O mode
1	DMA mode

HPS	DHP	Specification of Parity Added to CPU Bus
0	0	Odd parity
1	0	Even parity
x	1	Parity disabled

DSP	Specification of Parity Added to SCSI Bus
0	Parity enabled (fixed to odd parity)
1	Parity disabled

NAM	SIM	Bus Arbitration Execution Specification
0	x	Arbitration mode (non-single initiator mode)
1	0	Non-arbitration mode (non-single initiator mode)
1	1	Non-arbitration mode (single initiator mode)

RAEN	Response Specification in Case of Reselection as Initiator by Target
0	No response
1	Response

SAEN	Response Specification in Case of Selection as Target by Initiator
0	No response
1	Response

Remarks: x: Don't care

(17) Physical ID register (PID)

This is an 8-bit register which sets the uPD72611's own physical ID on the SCSI bus. 0 must always be written to bits 3 through 6.

This register is reset to 00H by $\overline{\text{RESET}}$ input or execution of the CHIP RESET command.

Figure 4-29 PID Format

Address	7	6	5	4	3	2	1	0	
25H	PEN	0	0	0	0	PID2	PID1	PID0	(R/W)

PEN	Operating Specification as SCSI Bus Controller
0	Does not operate as SCSI bus controller
1	Operates as SCSI bus controller

PID2 to PID0	uPD72611's Own ID Number
0 0 0	0
to	to
1 1 1	1

CHAPTER 5. COMMANDS

5.1 OUTLINE OF COMMANDS

The uPD72611 is provided with the 18 commands as shown in Table 5-1. These commands are used by the CPU to control the uPD72611.

(1) Command classification

Commands are classified by use into the following three groups:

- Group I ..... Commands used during operation as either the initiator or the target
- Group II .... Commands used during operation as the initiator
- Group III ... Commands used during operation as the target

Separately from the above groups, these commands can also be classified into the following three types according to their execution mode:

- Type A ... Commands which control the uPD72611 status
- Type B ... Commands which perform basic SCSI protocol control
- Type C ... Commands which automatically execute multiple type B commands in a standard sequence (compound commands)

A type A command is executed immediately it is issued (even if a type B or type C command is being executed). No interrupt is generated when processing ends (except for the CHIP RESET command).

Type B and type C commands notify the CPU of the end of processing by means of an interrupt request. During execution of a type B or type C command, the busy status is set. A type B or type C command issued while the uPD72611 is busy is ignored.

(2) Command operating status

There are three command operating statuses:

- DISCONNECT: D
- INITIATOR : I
- TARGET : T

A command may be valid or invalid depending on the status of the uPD72611 when the command is issued. If a command is issued when its status is invalid, it is processed as an invalid command. If a command is issued during internal uPD72611 processing initiated by a status transition on the SCSI bus side, the uPD72611 ignores that command. In this case an interrupt is generated due to this status transition, and therefore the contents of the IST register should be checked and processing performed accordingly. If the previously issued command is to be executed afterward, it must be reissued.

Table 5-1 Command Functions

Type	Command Name	Mnemonic	Outline of Operation	Status	Type
Group I	CHIP RESET	CRST	Internal uPD72611 reset	D, I, T	A
	BREAK	BRK	Suspension of command execution	D, I, T	A
	DISCONNECT	DIS	SCSI bus release	D, I, T	A
	CLEAR FIFO	CLRF	FIFO buffer clearance	D, I, T	A

(to be continued)

Table 5-1 Command Functions (cont'd)

Type	Command Name	Mnemonic	Outline of Operation	Status	Type
Group I (con-t'd)	SCSI RESET	SRST	SCSI bus reset	D, I, T	B
Group II	SET ATN	SETAT	$\overline{ATN}$ signal setting (0)	I	A
	RESET ACK	RSTAK	$\overline{ACK}$ signal reset (1)	I	A
	SELECT	SEL	Target selection	D	B
	TRANSFER	TFR	Information transmission/ reception (initiator)	I	B
	AUTO INITIATOR	AINI	Automatic execution of initiator standard operation	D	C
	AUTO INITIATOR 2	AINI2	Automatic execution of initiator standard operation after reselection	I	C
Group III	RESELECT	RSEL	Initiator reselection	D	B
	RECEIVE	REC	Information reception (target)	T	B
	SEND	SND	Information transmission (target)	T	B
	AUTO TARGET	ATGT	Automatic execution of target standard operation	D	C
	AUTO TARGET 2	ATGT2	Automatic execution of target standard termination operation	T	C
	RE-RECEIVE	RREC	Reselection → data reception consecutive execution (target)	D	C
	RE-SEND	RSND	Reselection → data transmission consecutive execution (target)	D	C

Remarks: "Information refers to data or a command, status or message.

5.2 COMMAND FUNCTIONS

Each command is described using the following format.

Command Name	Mnemonic
	Summary of Function

Type — Classification by command mode

Command Code — The command expressed as a binary code

Status Transition — A change of status is indicated in the following form:

Status in which command is valid → status after command execution

The meaning of the symbols is as follows:

- D: Disconnect status
- I: Initiator status
- T: Target status

Outline — Outline of the command function

Settings Required Before Issuing Command — Registers which must be set before issuing the command, and their contents

Operation — Detailed description of command operation

The following items may be omitted depending on the command:

Break Operation — Operation when the BREAK command is issued during execution of this command

Abnormal Termination — Conditions for abnormal termination of the command, and subsequent operation

Service Request — Service request made to the CPU after termination of command processing

Operation in Case of Parity Error Detection — Operation when a parity error is detected during execution of the command

Interrupts which may be Set at End of Execution (other than reset or break during execution) — Interrupts which may be set when execution of the command ends.

Execution Phase Code — Data held by the TP register when the command has terminated

CHIP RESET	CRST uPD72611 Reset

Type A

Command Code

7							0
0	0	0	0	0	0	0	0

Status Transition D, I, T → D

Outline Resets the uPD72611 internally.

Settings Required Before Issuing Command

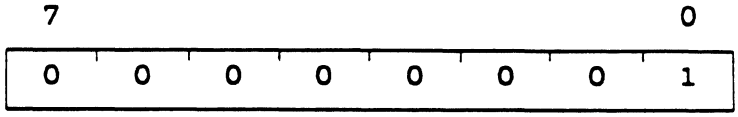
None

Operation The command being executed is discontinued immediately and the SCSI bus is released. All internal registers are then reset and the idle status is set.
On completion of the reset operation, an interrupt request to the host system is generated.

BREAK	BRK Command Break

Type A

Command Code



Status Transition D, I, T → D, I, T

Outline Discontinues type B or C command processing.

Settings Required Before Issuing Command

None

Operation

Processing is discontinued at the end of the operation cycle of a unit and the command wait status is set. The operation after the break depends on the command which was being executed: Refer to the "Break Operation" entry for the relevant command. After completion of the break operation, a termination interrupt request for the discontinued command is issued. At this time, an 8-bit code (execution phase code) indicating the break timing is stored in the TP register.

A BREAK command issued when the controller busy (CBSY = 1) status is not set is ignored.

DISCONNECT	DIS
	SCSI Bus Release

Type A

Command Code

7							0
0	0	0	0	0	0	1	0

Status Transition D, I, T → D

Outline Sets the disconnect status.

Settings Required Before Issuing Command

None

Operation The SCSI bus is released and the disconnect status is set. The command processing being executed is suspended immediately and the SCSI bus driver and SCSI controller are reset.
No action is taken if this command is issued while the disconnect status is set.

NOTE 1: This command cannot be used instead of the RESET ACK command.

2: The SCSI bus free status is not set if this command is issued in the initiator mode, since the target side is controlling the SCSI bus.

CLEAR FIFO	CLRF FIFO Buffer Clearance

Type A

Command Code

7							0
0	0	0	0	0	1	0	1

Status Transition D, I, T → D, I, T

Outline Clears the entire FIFO buffer and sets the empty status.

Settings Required Before Issuing Command

None

Operation The number of data bytes stored in the FIFO buffer becomes 0, and the empty status is set.
If the FIFO buffer is read after execution of this command, undefined data will be read.

SCSI RESET	SRST SCSI Bus Reset

Type B

Command Code

7							0
0	0	0	0	1	0	0	0

Status Transition D, I, T → D

Outline Resets the SCSI bus.

Settings Required Before Issuing Command

None

Operation The command being executed is discontinued immediately and the SCSI bus is released. The SCSI bus is the reset by outputting the $\overline{RST}$ signal, and at the same time the SCSI controller in the uPD72611 is reset and the idle status is set.

Break Operation At the following times command processing is discontinued, an interrupt request is generated, and the command wait mode is entered with the disconnect status set.

. Internal reset termination
. $\overline{RST}$ pulse output termination

Interrupts which may be Set at End of Execution (other than reset or break during execution)

- Command normal termination interrupt
  If the command has terminated normally.
- Invalid command interrupt
  If the command is not written correctly.
- CPU bus parity error interrupt
  If the parity attached to the command is not correct.
- SCSI reset condition, disconnect, reselected, selected, information phase start interrupt
  If already pending before the command is issued.

Execution Phase Code

- 01H: Reset phase

SET ATN	SETAT $\overline{\text{ATN}}$ Signal Setting

Type A

Command Code

7							0
0	0	0	0	0	0	1	1

Status Transition I → I

Outline Sets the $\overline{\text{ATN}}$ signal to L.

Settings Required Before Issuing Command

None

Operation Activates (drives low) the $\overline{\text{ATN}}$ pin. Used when the initiator issues a message out phase request to the target. The command being executed is not affected.

RESET ACK	RSTAK
	$\overline{\text{ACK}}$ Signal Reset

Type A

Command Code

7							0
0	0	0	0	0	1	0	0

Status Transition I → I

Outline Resets the $\overline{\text{ACK}}$ signal to H.

Settings Required Before Issuing Command

None

Operation Deactivates (drives high) the $\overline{\text{ACK}}$ pin. Used when the initiator resets the $\overline{\text{ACK}}$ pin: For example, when a receive operation is terminated with the $\overline{\text{ACK}}$ pin still active due to a receive data parity error or receive message rejection, etc. The command being executed is not affected.

SELECT	SEL Target Selection

Type B

Command Code

7							0
0	0	0	1	AT	0	0	0

AT	$\overline{\text{ATN}}$ Pin Control in Selection Phase
0	Not activated
1	Activated, message out phase request made to selected target

Status Transition D → D, I

Outline Selects the target as the initiator.

Settings Required Before Issuing Command

DID register ← ID number of target to be selected

Operation

The operation differs in arbitration mode and non-arbitration mode.

(1) Arbitration mode

(a) Bus free phase detection

The bus free timeout timer is started within a maximum of 12 clock cycles after the command is issued, and the device waits for bus free phase detection. If the bus free phase is detected before the timer overflows, processing moves on to step (b).

(b) Arbitration

After waiting for 16 clock cycles, the uPD72611 drives the $\overline{BSY}$ signal and only the SCSI data bus line ($\overline{SDB0}$ to $\overline{SDB7}$) corresponding to its own ID set in the PID register active.

After waiting for 48 clock cycles, the uPD72611 checks the SCSI data bus lines to see if an SCSI device with a higher priority (higher ID number) than its own is requesting the bus.

If the check of the SCSI data bus lines shows its own ID number to be the highest, the uPD72611 activates the $\overline{SEL}$ signal. Then after a further wait of 24 clock cycles, the arbitration phase is terminated and processing proceeds to step (c).

If the $\overline{SEL}$ signal is activated by an SCSI device with a higher priority (ID number) than its own, the uPD72611 immediately releases the SCSI bus and returns to step (a).

(c) Selection

The $\overline{ACK}$ signal is deactivated, and the $\overline{ATN}$ signal is activated if the AT bit in the command code is 1, or deactivated if 0. The next operation differs for the non-single initiator mode and the single initiator mode.

- Non-single initiator mode
  The uPD72611 outputs to the SCSI data bus lines the logical sum of the ID bits corresponding to its own ID set in the PID register and the ID bits corresponding to the ID, which is set in the DID register, of the target to be selected.
- Single initiator mode
  The uPD72611 outputs to the SCSI data bus lines only the ID bits corresponding to the ID, which is set in the DID register, of the target to be selected.

After a 2 clock cycle wait, the $\overline{\text{BSY}}$ signal is released and the selection timeout monitoring timer is started.

After a further 8 clock cycle wait, the $\overline{\text{BSY}}$ signal is checked.

If activation of the $\overline{\text{BSY}}$ signal is detected before the timer overflows, after a 6 clock cycle wait the $\overline{\text{SEL}}$ signal is released and the selection phase is terminated.

If the timer overflows before the $\overline{\text{BSY}}$ signal is activated, the uPD72611 immediately suspends output to the SCSI data bus lines and, with the $\overline{\text{SEL}}$ signal still active, monitors the $\overline{\text{BSY}}$ signal for another 4096 clock cycles.

If the $\overline{BSY}$ signal is activated within 4096 clock cycles, the uPD72611 waits for 6 clock cycles and then releases the $\overline{SEL}$ signal and terminates the selection phase. If the $\overline{BSY}$ signal is not activated before the elapse of 4096 clock cycles, the $\overline{SEL}$ signal is released and a selection/reselection timeout is generated.

(d) Termination

An interrupt request is generated and the command wait mode is entered with the initiator status set.

(2) Non-arbitration mode

(a) Bus free phase detection

The bus free timeout timer is started within a maximum of 12 clock cycles after the command is issued, and the device waits for bus free phase detection. If the bus free phase is detected before the timer overflows, processing moves on to step (b).

(b) Selection

After a 16 clock cycle wait, the $\overline{ACK}$ signal is deactivated, and the $\overline{ATN}$ signal is activated if the AT bit in the command code is 1, or deactivated if 0. From here on, the uPD72611 operates as the initiator. The next operation differs for the non-single initiator mode and the single initiator mode.

- Non-single initiator mode
  The uPD72611 outputs to the SCSI data bus lines the logical sum of its own ID bits and the ID bits of the target to be selected.
- Single initiator mode
  The uPD72611 outputs to the SCSI data bus lines the ID bits of the target to be selected.

After a 2 clock cycle wait, the $\overline{SEL}$ signal is activated and at the same time the selection timeout monitoring timer is started. After a further 8 clock cycle wait, checking of the $\overline{BSY}$ signal is started. If the $\overline{BSY}$ signal is detected before the timer overflows, after a 6 clock cycle wait the $\overline{SEL}$ signal is released and the selection phase is terminated.
if the timer overflows before the $\overline{BSY}$ signal is activated, the uPD72611 immediately releases output to the SCSI data bus lines and, with the $\overline{SEL}$ signal still active, monitors the $\overline{BSY}$ signal for another 4096 clock cycles.
If the $\overline{BSY}$ signal is activated within 4096 clock cycles, the uPD72611 waits for 6 clock cycles and then releases the $\overline{SEL}$ signal and terminates the selection phase.

(c) Termination
An interrupt request is generated and the command wait is entered with the initiator status set.

Break Operation

- Command processing during bus free phase detection and during arbitration is immediately discontinued, an interrupt request is generated, and the command wait mode is entered with the disconnect status set.
- During selection
  SCSI ID output to the SCSI bus is immediately discontinued and the $\overline{BSY}$ signal is monitored for 4096 clock cycles with the $\overline{SEL}$ signal still active.
  If the $\overline{BSY}$ signal is activated within 4096 clock cycles, the uPD72611 waits for 6 clock cycles and then releases the $\overline{SEL}$ signal, completes the selection phase, generates an interrupt request and enters the command wait mode with the initiator status set.
  If the $\overline{BSY}$ signal is not activated within 4096 clock cycles, the uPD72611 releases the SCSI bus due to a selection failure, generates an interrupt request, and enters the command wait mode with the disconnect status set.

Abnormal Termination

o Processing method
Command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the disconnect status set.

o Conditions for occurrence

. Invalid command
  If this command is issued with the initiator status or target status set.
. CPU bus parity error
  If a parity error is detected in the data written to the uPD72611 from the CPU bus.
. Bus free timeout error
  If the bus free phase is not detected within the time set in the BFTOUT register.
. Selection/reselection timeout error
  If there is no target response to selection within the time set in the SRTOUT register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

. Command normal termination interrupt
  If the command has terminated normally.
. Invalid command interrupt
  If the command is written other than when the uPD72611 status is "disconnect".
. CPU bus parity error interrupt
  If the parity attached to the command is not correct
. Bus free timeout error interrupt
  If the bus free phase is not detected within a given time.
. Selection/reselection timeout error interrupt
  If there is no response from the target within a given time.

- SCSI reset condition interrupt
  If already pending before the command is issued, or if a reset condition is generated during command execution. In the former case the command is acknowledged, and therefore another interrupt is generated following this interrupt.
- Reselected/selected interrupt
  If already pending before the command is issued, or if unsuccessful in arbitration during command execution, and conversely selected/reselected by another SCSI device. In the former case an invalid command interrupt is generated following this interrupt.

Execution Phase Code

- 11H: Arbitration phase
- 12H: Target selection phase

TRANSFER	TFR
Information Transmission/Reception (Initiator)	

Type B

Command Code

7							0
C1	C0	0	1	0	0	1	0

C1	C0	Data Setting Operation on Current Transfer Counter	Number of Transfer Bytes and Transfer Byte Unit
0	0	CTCH, CTCM, CTCL ← BTCH, BTCM, BTCL	0 to 16,777,215 bytes Set in 1-byte units
0	1	CTCH, CTCM ← BTCH, BTCM CTCL ← 00H	0 to 16,776,960 bytes Set in 256-byte units
1	0	CTCL ← BTCL CTCH, CTCM ← 0000H	0 to 255 bytes Set in 1-byte units
1	1	CTCH, CTCM, CTCL ← 000001H	Fixed value of 1 (not affected by BTCH, BTCM, BTCL contents)

Status Transition I → I

Outline Performs information transmission/reception as the initiator.

Settings Required Before Issuing Command

TMOD register ← Transfer mode

BTCL, BTCM, BTCH registers Number of transfer bytes

Operation

(1) Start

An information transfer phase in the transfer direction specified by the $\overline{I}$/O signal on the SCSI bus is started within a maximum of 16 clock cycles after the command is issued.

(2) Information transfer

Information is exchanged with the SCSI bus in accordance with the protocol stipulated in the SCSI-2 specifications. The transfer counter contents are decremented by 1 for each one-byte transfer.

The transfer counter coutdown timing is as follows:

- Asynchronous mode
  - Transmission: Rising edge of $\overline{REQ}$ pulse
  - Reception : Rising edge of $\overline{REQ}$ pulse
- Synchronous mode: Rising edge of $\overline{ACK}$ pulse

(3) Termination

- Transmission to SCSI bus

  When the contents of the transfer counter become 0, the transfer of information to the SCSI bus is terminated and the remaining data in the FIFO buffer is cleared, then the command operation is terminated.

. Reception from SCSI bus
When the contents of the transfer counter become 0, the transfer of information from the SCSI bus is terminated and data transfer requests are made to the CPU until the FIFO buffer is empty. When the FIFO buffer is empty, the command operation is terminated.

In both cases, when the command operation is terminated an interrupt request is generated and the command wait mode is entered with the initiator status set.

(4) Caution on transfer counter setting
When sending data, a certain interval is required between writing of the last data from the CPU to the uPD72611 and termination of the command operation (when the transfer counter contents become 0) (see 3.4 "SCSI Transfer Control").
In the case of DMA code the $\overline{\text{DMARQ}}$ signal remains active until the command operation terminates, and therefore if the DMA controller counter set value is larger than the uPD72611 transfer counter set value the DMA controller transfers excess data to the uPD72611 (although only the quantity of data set in the uPD72611 counter is output to the SCSI bus). At this time the excess data left in the FIFO buffer is cleared, but there is a discrepancy between the transfer data count on the CPU side and the SCSI side.

Therefore, discrepancy between the transfer data on the CPU side and the SCSI side should be avoided by aligning both counter set values and not having the transfer data quantity managed by the DMA controller counter.

Break Operation

Command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the initiator status set. After the break, the $\overline{EOP}$ signal is activated during the DMA service period.

Abnormal Termination

o Processing method
Command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the initiator status set.

o Conditions for occurrence
. Invalid command
If this command is issued with the disconnect status or target status set.

Also, in the following cases, if an error is detected command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the initiator status set. The $\overline{EOP}$ signal is activated during the DMA service period after error detection.

. FIFO buffer overrun/underrun
If a FIFO buffer overrun/underrun is detected during an information transfer.

- Synchronous transfer offset error
  If the offset between the $\overline{REQ}$ signal and $\overline{ACK}$ signal exceeds the set range (between 0 and the value set in the TMOD register) during synchronous data transfer on the SCSI bus.
- SCSI bus parity error
  If a parity error is detected in the data read from the SCSI bus. The $\overline{ATN}$ signal is automatically set when the parity error is detected.
- CPU bus parity error
  If a parity error is detected in the data written to the uPD72611 from the CPU bus. The $\overline{ATN}$ signal is automatically set when the parity error is detected.
- $\overline{REQ}/\overline{ACK}$ timeout error
  If handshaking in an information transfer pauses for longer than the time set in the RATOUT register.
- Information transfer phase error
  If there is a bus phase transition before the transfer counter value becomes 0.

Service Request

If the processing phase is the message in phase, when reception of a message consisting of the number of bytes set in the transfer counter has been executed and the final transfer byte has been read from the SCSI bus and transferred to the FIFO buffer, the transfer operation is terminated with the $\overline{ACK}$ signal still active and a service interrupt request to the CPU is generated. As interrupt servicing, the CPU must read and decode the receive message in the FIFO buffer, decide whether to accept or reject the message, and deactivate the $\overline{ACK}$ signal with the RESET ACK command and complete handshaking (immediately if the message is accepted, or after setting the attention condition status by activating the $\overline{ATN}$ signal with the SET ATN command if the message is rejected).

Operation in Case of Parity Error Detection

- When the PERP bit in the EXMOD register is not set

  When a parity error is detected, command execution is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the initiator status set, and also the $\overline{EOP}$ signal is activated during the DMA service period after error detection. The $\overline{ATN}$ signal is automatically set when the parity error is detected.

- When the PERP bit in the EXMOD register is set
  When a parity error is detected during an information transfer, the transfer is not discontinued immediately but instead continues until the command terminates. After command termination an interrupt request is generated, and the command wait mode is entered with the initiator status set.
  It is possible to check whether or not a parity error has been generated by reading the EXST register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

- Command normal termination interrupt
  If the command has terminated normally.
- Invalid command interrupt
  If the command is written other than when the uPD72611 status is "initiator".
- FIFO buffer overrun/underrun interrupt
  If a FIFO buffer overrun/underrun occurs during command execution.
- Synchronous transfer offset error interrupt
  If a synchronous transfer offset error occurs during command execution.
- SCSI bus parity error interrupt
  If a parity error is detected in the data received from the SCSI bus.
- CPU bus parity error interrupt
  If a parity error is detected in the data received from the CPU bus.
- $\overline{REQ}/\overline{ACK}$ timeout error interrupt
  If a $\overline{REQ}/\overline{ACK}$ timeout error occurs.

- Information transfer phase error interrupt
  If there is a phase transition during command execution.
- SCSI reset condition interrupt
  If already pending before the command is issued, or if a reset condition is generated during command execution. In the former case an invalid command interrupt is generated following this interrupt.
- Disconnected interrupt
  If already pending before the command is issued, or if the target releases the bus during command execution. In the former case an invalid command interrupt is generated following this interrupt.
- Message reception interrupt
  If the message in phase is executed and terminates normally.

Execution Phase Code

- 21H: Information transfer phase

AUTO INITIATOR	AINI
Automatic Execution of Initiator Standard Operation	

Type C

Command Code

7							0
C1	C0	0	1	AT	1	0	0

C1	C0	Data Setting Operation on Current Transfer Counter	Number of Transfer Bytes and Transfer Byte Unit
0	0	CTCH, CTCM, CTCL ← BTCH, BTCM, BTCL	0 to 16,777,215 bytes Set in 1-byte units
0	1	CTCH, CTCM ← BTCH, BTCM CTCL ← 00H	0 to 16,776,960 bytes Set in 256-byte units
1	0	CTCL ← BTCL CTCH, CTCM ← 0000H	0 to 255 bytes Set in 1-byte units
1	1	CTCH, CTCM, CTCL ← 000001H	Fixed value of 1 (not affected by BTCH, BTCM, BTCL contents)

AT	$\overline{\text{ATN}}$ Pin Control in Selection Phase
0	Not activated
1	Activated, message out phase request made to selected target (Identify message sent)

Status Transition D → D, I

Outline

Automatically executes standard operation as initiator.
This command consecutively executes a combination of the SELECT command and multiple TRANSFER commands. An interrupt request is not generated after execution of each command in the combination, but only when all the commands have been executed.
The SCSI-2 commands supported by this command are Groups 0, 1, 2, 5, 6 and 7.

Settings Required Before Issuing Command

DID register ← ID number of target to be selected
CDB register ← Command descriptor command
TMOD register ← Transfer mode
BTCL, BTCM, BTCH registers ← Number of transfer bytes

. Only when AT = 1:
MSG register ← Identify message
MSG2 register ← 1st byte of queue tag message
MSG3 register ← 2nd byte of queue tag message

Operation

The command processing sequence depends on the value of the AT bit in the command code and the MSG3 bit in the EXMOD register, as shown below (there are also cases in which data transmission/reception is not performed).

. When AT = 0 and MSG3 = 0, or AT = 0 and MSG3 = 1
(a) Bus arbitration
(b) Target selection
] SELECT

(c) Transmission of CDB register contents
(SCSI-2 command) TRANSFER-1

(d) Data transmission/reception TRANSFER-2

(e) Status reception TRANSFER-3

(f) Command complete message reception TRANSFER-4

. When AT = 1 and MSG3 = 0

(a) Bus arbitration
(b) Target selection — SELECT

(c) Transmission of Message register contents
(Identify message) TRANSFER-1

(d) Transmission of CDB register contents
(SCSI-2 command) TRANSFER-2

(e) Data transmission/reception TRANSFER-3

(f) Status reception TRANSFER-4

(g) Command complete message reception TRANSFER-5

. When AT = 1 and MSG3 = 1

(a) Bus arbitration
(b) Target selection — SELECT

(c) Transmission of Message register contents
(Identify message) TRANSFER-1

(d) Transmission of Message 2 register contents
(1st byte of queue tag message) TRANSFER-2

(e) Transmission of Message 3 register contents
(2nd byte of queue tag message) TRANSFER-3

(f) Transmission of CDB register contents (SCSI-2 command) TRANSFER-4

(g) Data transmission/reception TRANSFER-5

(h) Status reception TRANSFER-6

(i) Command complete message reception TRANSFER-7

The operation in each sequence is described below.

(1) Select operation (corresponding to SELECT command)
Processing corresponding to the SELECT command is started within a maximum of 12 clock cycles after the command is issued. If the select operation is successful, processing proceeds to step (2) if AT = 1, or to step (4) if AT = 0.

(2) Identify message transmission (corresponding to TRANSFER command)
Processing is started corresponding to a TRANSFER command which transmits a one-byte message consisting of the MSG register contents as an identify message. If the message transmission is successful, processing proceeds to step (3) if MSG3 = 1, or to step (4) if MSG3 = 0.

(3) Queue tag message transmission (2 bytes) (corresponding to TRANSFER command)
Processing is started corresponding to a TRANSFER command which transmits a one-byte message consisting of the MSG2 register contents as the first byte of a queue tag message. If the message transmission is successful, processing corresponding to a TRANSFER command is then started which transmits a one-byte message consisting of the MSG3 register contents as the second byte of the queue tag message. If this message transmission is also successful, processing proceeds to step (4).

(4) SCSI-2 command transmission (corresponding to TRANSFER command)
Processing is started corresponding to a TRANSFER command which transmits an SCSI-2 command with the CDB register contents as the SCSI-2 command (command descriptor block). The length of the CDB transmitted is determined automatically by referencing the operation code set in the CDB00 register.
If the SCSI-2 command transmission is successful, processing proceeds to step (6) if the number of transfer data bytes set by BTCL/BTCM/BTCH and C1 & C0 is 0, or otherwise to step (5).

(5) Data transmission/reception (corresponding to TRANSFER command)
Processing is started corresponding to a TRANSFER command which transmits/receives the number of transmission data bytes set by the BTCL/BTCM/BTCH registers and C1 & C0 via the FIFO buffer. The data transfer direction is determined automatically by the status of the I/O signal.
When the set number of bytes have been transferred, the CTCLH/CTCM/CTCH value becomes 0 and processing proceeds to step (6).

(6) SCSI-2 status reception (corresponding to TRANSFER command)
Processing is started corresponding to a TRANSFER command which receives a one-byte SCSI status. The received SCSI status is stored in the TST register. If the SCSI-2 status reception is successful, processing proceeds to step (7).

(7) Command complete message reception (corresponding to TRANSFER command)
Processing is started corresponding to a TRANSFER command which receives a one-byte message. If the command complete message reception is successful, processing proceeds to step (8).

(8) Termination

If the command complete message reception is successful and the series of processing sequences terminates normally, an interrupt request is generated and the command wait mode is entered with the disconnect status set.

(9) Caution on transfer counter setting

When sending data, a certain interval is required between writing of the last data from the CPU to the uPD72611 and termination of the command operation (when the transfer counter contents become 0) (see 3.4 "SCSI Transfer Control").

In the case of DMA mode the $\overline{\text{DMARQ}}$ signal remains active until the command operation terminates, and therefore if the DMA controller counter set value is larger than the uPD72611 transfer counter set value the DMA controller transfers excess data to the uPD72611 (although only the quantity of data set in the uPD72611 counter is output to the SCSI bus). At this time the excess data left in the FIFO buffer is cleared, but there is a discrepancy between the transfer data count on the CPU side and the SCSI side. Therefore, discrepancy between the transfer data on the CPU side and the SCSI side should be avoided by aligning both counter set values and not having the transfer data quantity managed by the DMA controller counter.

Break Operation

. During select operation
SCSI ID number output to the SCSI bus is immediately discontinued and the $\overline{BSY}$ signal is monitored for 4096 clock cycles with the $\overline{SEL}$ signal still active. If the $\overline{BSY}$ signal is activated within 4096 clock cycles, the uPD72611 waits for 6 clock cycles and then releases the $\overline{SEL}$ signal, completes the selection phase, generates an interrupt request and enters the command wait mode with the initiator status set.
If the $\overline{BSY}$ signal is not activated within 4096 clock cycles, the uPD72611 releases the SCSI bus due to a selection failure, generates an interrupt request, and enters the command wait mode with the disconnect status or initiator status set.

. During information transmission
When the BREAK command is written, command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the initiator status set. After the break, the $\overline{EOP}$ signal is activated during the DMA service period.

Abnormal Termination

o Processing method
Command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the disconnect status set.

o Conditions for occurrence
. Invalid command
If this command is issued with the initiator status or target status set.

- Bus free timeout error
  If the bus free phase is not detected within the time set by the BFTOUT register.
- Selection/reselection timeout error
  If there is no target response to selection within the time set in the SRTOUT register.

Also, in the following cases, if an error is detected command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the initiator status set. The $\overline{EOP}$ signal is activated during the DMA service period after error detection.

- Unsupported group
  If the SCSI-2 command group indicated by the operation code of the SCSI-2 command set in the CDB00 register is not a group supported on the uPD72611. In this case, the command terminates abnormally before SCSI-2 command transmission.
- FIFO buffer overrun/underrun
  If a FIFO buffer overrun/underrun is detected during an information transfer.
- Synchronous transfer offset error
  If the offset between the $\overline{REQ}$ signal and $\overline{ACK}$ signal exceeds the set range (between 0 and the value set in the TMOD register) during synchronous data transfer on the SCSI bus.

- SCSI bus parity error
  If a parity error is detected in the data, status or message read from the SCSI bus. The $\overline{ATN}$ signal is automatically set when the parity error is detected.
- CPU bus parity error
  If a parity error is detected in the data written from the CPU bus. The $\overline{ATN}$ signal is automatically set when the parity error is detected.
- $\overline{REQ}/\overline{ACK}$ timeout error
  If handshaking in an information transfer pauses for longer than the time set in the RATOUT register.
- Information transfer phase error
  If the bus phase changes during an information transfer, or if the bus phase is different from that expected from the command sequence.

Service Request

In the command complete message reception sequence, a one-byte message is received. The uPD72611 decodes this message simultaneously with reading of the message from the SCSI bus and transfer to the MSG register. In cases other than that of a command complete message, the transfer operation is terminated with the $\overline{ACK}$ signal still active and a service interrupt request to the CPU is generated. As interrupt servicing, the CPU reads and decodes the message stored in the MSG register and decides whether to accept or reject the message. If the message is accepted, the handshaking protocol must be concluded with the RESET ACK command. If the message is rejected, the handshaking protocol must be concluded with the RESET ACK command after first setting the attention condition status is set by activating the $\overline{ATN}$ signal with the SET ATN command.

Operation in Case of Parity Error Detection

- When the PERP bit in the EXMOD register is not set

  When a parity error is detected, command execution is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the initiator status set, and also the $\overline{EOP}$ signal is activated during the DMA service period after error detection. The $\overline{ATN}$ signal is automatically set when the parity error is detected.

. When the PERP bit in the EXMOD register is set
When a parity error is detected during an information transfer, the transfer is not discontinued immediately but instead continues until the command terminates. After transfer termination a parity error check is made, and if a parity error has been generated an interrupt request is generated, and the command wait mode is entered with the initiator status set.
It is possible to check whether or not a parity error has been generated by reading the EXST register, and to confirm the parity error generation phase by reading the TP register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

. Command normal termination interrupt
If the command has terminated normally, or if a parity error has been generated when the PERP bit is set.
. Invalid command interrupt
If the command is written other than when the uPD72611 status is "disconnect".
. FIFO buffer overrun/underrun interrupt
If a FIFO buffer overrun/underrun occurs during command execution.
. Synchronous transfer offset error interrupt
If a synchronous transfer offset error occurs during command execution.
. SCSI bus parity error interrupt
If a parity error is detected in the data received from the SCSI bus.

- CPU bus parity error interrupt
  If a parity error is detected in the data received from the CPU bus.
- Bus free timeout error interrupt
  If the bus free phase is not detected within a given time.
- Selection/reselection timeout error interrupt
  If there is no response from the target within a given time.
- $\overline{REQ}/\overline{ACK}$ timeout error interrupt
  If a $\overline{REQ}/\overline{ACK}$ timeout error occurs.
- Information transfer phase error interrupt
  If there is a phase transition during command execution, or if a phase different from the predicted phase has arisen.
- Unsupported group interrupt
  If an SCSI-2 command of an unsupported group has been set in the CDB register.
- SCSI reset condition interrupt
  If already pending before the command is issued, or if a reset condition is generated during command execution. As the command is acknowledged, in the former case, another interrupt is generated following this interrupt.
- Disconnected interrupt
  If the target release the bus during command execution.

- Reselected/selected interrupt
  If already pending before the command is issued, or if unsuccessful in arbitration during command execution, and conversely selected/reselected by another SCSI device. In the former case an invalid command interrupt is generated following this interrupt.
- Message reception interrupt
  If a message other than a command complete message is received in the message reception phase.

Execution Phase Code

- 31H: Arbitration phase
- 32H: Target selection phase
- 33H: Identify message transmission phase
- 38H: Queue tag message 1st byte transmission phase
- 39H: Queue tag message 2nd byte transmission phase
- 34H: Command transmission phase
- 35H: Data transmission/reception phase
- 36H: Status reception phase
- 37H: Command complete message reception phase

AUTO INITIATOR 2	AINI2
Reselect → Automatic Execution of Initiator Standard Operation	

Type C

Command Code

7							0
C1	C0	0	1	0	1	0	1

C1	C0	Data Setting Operation on Current Transfer Counter	Number of Transfer Bytes and Transfer Byte Unit
0	0	CTCH, CTCM, CTCL ← BTCH, BTCM, BTCL	0 to 16,777,215 bytes Set in 1-byte units
0	1	CTCH, CTCM ← BTCH, BTCM CTCL ← 00H	0 to 16,776,960 bytes Set in 256-byte units
1	0	CTCL ← BTCL CTCH, CTCM ← 0000H	0 to 255 bytes Set in 1-byte units
1	1	CTCH, CTCM, CTCL ← 000001H	Fixed value of 1 (not affected by BTCH, BTCM, BTCL contents)

Status Transition D → D, I

Outline Automatically executes standard operation of an initiator after it has been reselected. This command consecutively executes multiple TRANSFER commands in combination.

Settings Required Before Issuing Command

TMOD register ← Transfer mode
BTCL, BTCM, BTCH registers ← Number of transfer bytes

Operation

The command processing sequences are as follows:

(a) Data transmission/reception
TRANSFER command

(b) Status reception TRANSFER command-2

(c) Command complete message reception
TRANSFER command-3

An identify message is not received automatically. Therefore, when the reselected target requests the message in phase it is necessary , before this command is issued, to issue a TRANSFER command to the initiator, in order to receive the identify message and ascertain which logical unit has been selected. The operation in each sequence is described below.

(1) Data transmission/reception (corresponding to TRANSFER command)
Within a maximum of 16 clock cycles after the command is written, processing is started corresponding to a TRANSFER command which transmits/receives the number of transmission data bytes set by the BTCL/BTCM/BTCH registers and C1 & C0 via the host FIFO buffer. The data transfer direction is determined by the status of the $\overline{I}$/O signal. When the set number of bytes have been transferred, processing proceeds to step (2). Except when C1 = 1 and C0 = 1, when the number of data transfer bytes is set to 0 (BTCL/BTCM/BTCH = 000000H), data transmission/reception is not performed and processing proceeds to step (2).

(2) SCSI-2 status reception (corresponding to TRANSFER command)
Processing is started corresponding to a TRANSFER command which receives a one-byte SCSI status. The received SCSI status is stored in the TST register. If the SCSI-2 status reception is successful, processing proceeds to step (3).

(3) Command complete message reception (corresponding to TRANSFER command)
Processing is started corresponding to a TRANSFER command which receives a one-byte message. The received command complete message is stored in the MSG register. If the command complete message reception is successful, processing proceeds to step (4).

(4) Termination
If the command complete message reception is successful and the series of processing sequences terminates normally, an interrupt request is generated and the command wait mode is entered with the disconnect status set.

Break Operation

Command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the initiator status set. After the break, the $\overline{EOP}$ signal is activated during the DMA service period.

Abnormal Termination

- o Processing method
  Command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the initiator status set.
- o Conditions for occurrence
  - . FIFO buffer overrun/underrun
    If a FIFO buffer overrun/underrun is detected during a data transfer.
  - . Synchronous transfer offset error
    If the offset between the $\overline{REQ}$ signal and $\overline{ACK}$ signal exceeds the set range during synchronous data transfer.
  - . SCSI bus parity error
    If a parity error is detected in the data, status or message read from the SCSI bus. The $\overline{ATN}$ signal is automatically set when the parity error is detected.
  - . CPU bus parity error
    If a parity error is detected in the data written from the CPU bus. The $\overline{ATN}$ signal is automatically set when the parity error is detected.
  - . $\overline{REQ}/\overline{ACK}$ timeout error
    If handshaking in an information transfer pauses for longer than the time set in the RATOUT register.
  - . Information transfer phase error
    If the bus phase changes during an information transfer, or if the bus phase is different from that expected from the command sequence.

Service Request

In the command complete message reception sequence, a one-byte message is received. The uPD72611 decodes this message simultaneously with reading of the message from the SCSI bus and transfer to the MSG register. In cases other than that of a command complete message, the transfer operation is terminated with the $\overline{ACK}$ signal still active and a service interrupt request to the CPU is generated. As interrupt servicing, the CPU reads and decodes the message stored in the MSG register and decides whether to accept or reject the message. If the message is accepted, the handshaking protocol must be concluded with the RESET ACK command. If the message is rejected, the handshaking protocol must be concluded with the RESET ACK command after the $\overline{ATN}$ signal is activated with the SET ATN command.

Operation in Case of Parity Error Detection

. When the PERP bit in the EXMOD register is not set

When a parity error is detected, command execution is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the initiator status set, and also the $\overline{EOP}$ signal is activated during the DMA service period after error detection. The $\overline{ATN}$ signal is automatically set when the parity error is detected.

- When the PERP bit in the EXMOD register is set
  When a parity error is detected during an information transfer, the transfer is not discontinued immediately but instead continues until the phase terminates. After transfer termination a parity error check is made, and if a parity error has been generated an interrupt request is generated, and the command wait mode is entered with the initiator status set. It is possible to check whether or not a parity error has been generated by reading the EXST register, and to confirm the parity error generation phase by reading the TP register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

- Command normal termination interrupt
  If the command has terminated normally, or if a parity error has been generated when the PERP bit is set.
- Invalid command interrupt
  If the command is written other than when the uPD72611 status is "initiator".
- FIFO buffer overrun/underrun interrupt
  If a FIFO buffer overrun/underrun occurs during command execution.
- Synchronous transfer offset error interrupt
  If a synchronous transfer offset error occurs during command execution.
- SCSI bus parity error interrupt
  If a parity error is detected in the data received from the SCSI bus.

- CPU bus parity error interrupt
  If a parity error is detected in the data received from the CPU bus.
- $\overline{REQ}/\overline{ACK}$ timeout error interrupt
  If a $\overline{REQ}/\overline{ACK}$ timeout error occurs.
- Information transfer phase error interrupt
  If there is a phase transition during command execution, or if a phase different from the predicted phase has arisen.
- SCSI reset condition interrupt
  If already pending when the command is issued, or if a reset condition is generated during command execution. In the former case the command is acknowledged, and therefore another interrupt is generated following this interrupt.
- Disconnected interrupt
  If already pending before the command is issued, or if the target releases the bus during command execution. In the former case an invalid command interrupt is generated following this interrupt.
- Message reception interrupt
  If a message other than a command complete message is received in the message reception phase.

Execution Phase Code

- 35H: Data transmission phase
- 36H: Status reception phase
- 37H: Command complete message reception phase.

RESELECT	RSEL
	Initiator Reselection

Type B

Command Code

7							0
0	0	1	0	0	0	0	0

Status Transition D → D, T

Outline Reselects the initiator as the target.

Setting Required Before Issuing Command

DID register ← ID signal of target to be selected

Operation

This command is only valid in the arbitration mode; in the non-arbitration mode it is an invalid command and will result in an abnormal termination.

(1) Bus free phase detection
The bus free timeout detection wait mode is entered within a maximum of 12 clock cycles after the command is issued.
If the bus free phase is detected before the timer overflows, processing proceeds to step (2).

(2) Arbitration
After waiting for 16 clock cycles, the uPD72611 activates the $\overline{BSY}$ signal and only the SCSI data bus line corresponding to its own ID set in the PID register.

After waiting for 48 clock cycles, the uPD72611 checks the SCSI data bus lines to see if an SCSI device with a higher priority (higher ID number) than its own is requesting the bus.
If the check of the SCSI data bus lines shows its own ID number to be the highest, the uPD72611 activates the $\overline{SEL}$ signal. Then after a further wait of 24 clock cycles, processing proceeds to step (3).
If the bus is requested by an SCSI device with a higher priority (ID number) or the $\overline{SEL}$ signal is activated by another SCSI device, the uPD72611 immediately releases the SCSI bus and returns to step (1).

(3) Reselection

The uPD72611 operates as the target after deactivating the $\overline{C}$/D, $\overline{MSG}$ and $\overline{REQ}$ signals and activating the $\overline{I}$/O signal. At the same time, the uPD72611 outputs to the SCSI data bus lines the logical sum of its own ID number set in the PID register and the ID number of the initiator to be reselected which is set in the DID register.
Then, after a 2 clock cycle wait, the $\overline{BSY}$ signal is released and the selection timeout monitoring timer is started. After a further 8 clock cycle wait, checking of the $\overline{BSY}$ signal is started.

If activation of the $\overline{BSY}$ signal is detected before the timer overflows, the uPD72611 activates the $\overline{BSY}$ signal. Then, after a 6 clock cycle wait, the $\overline{SEL}$ signal is released and the reselection phase is terminated.
If the timer overflows before the $\overline{BSY}$ signal is activated, the uPD72611 immediately suspends output to the SCSI data bus lines and, with the $\overline{SEL}$ and I/O signals still active, monitors the $\overline{BSY}$ signal for another 4096 clock cycles. If the $\overline{BSY}$ signal is activated within 4096 clock cycles, the uPD72611 waits for 6 clock cycles and then releases the $\overline{SEL}$ signal and terminates the reselection phase.
If the $\overline{BSY}$ signal is not activated before the elapse of 4096 clock cycles, the $\overline{SEL}$ signal is released and a selection/reselection timeout is generated.

(4) Termination
An interrupt request is generated and the command wait mode is entered with the target status set.

Break Operation

. Command processing during bus free phase detection and during arbitration is immediately discontinued, an interrupt is generated, and the command wait mode is entered with the disconnect status set.

. During reselection
SCSI ID number output to the SCSI bus is immediately discontinued and the $\overline{BSY}$ signal is monitored for 4096 clock cycles with the $\overline{SEL}$ signal still active. If the $\overline{BSY}$ signal is activated within 4096 clock cycles, the uPD72611 waits for 6 clock cycles and then releases the $\overline{SEL}$ signal, concludes the selection phase, generates an interrupt request and enters the command wait mode with the target status set.
If the $\overline{BSY}$ signal is not activated within 4096 clock cycles, the uPD72611 releases the SCSI bus due to a selection failure, generates an interrupt request, and enters the command wait mode with the disconnect status set.

Abnormal Termination

o Processing method
Command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the disconnect status set.

o Conditions for occurrence
. Invalid command
If this command is issued with the initiator status or target status set.
. CPU bus parity error
If a parity error is detected in the data written to the uPD72611 from the CPU bus.
. Bus free timeout error
If the bus free phase is not detected within the time set in the BFTOUT register.

. Selection/reselection timeout error
If there is no initiator response to reselection within the time set in the SRTOUT register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

. Command normal termination interrupt
If the command has terminated normally.
. Invalid command interrupt
If the command is written other than when the uPD72611 status is "disconnect".
. Host bus parity error interrupt
If the parity attached to the command is not correct
. Bus free timeout error interrupt
If the bus free phase is not detected within a given time.
. Selection/reselection timeout error interrupt
If there is no response from the target within a given time.
. SCSI reset condition interrupt
If already pending before the command is issued, or if a reset condition is generated during command execution. In the former case the command is acknowledged, and therefore another interrupt is generated following this interrupt.

. Reselected/selected interrupt
  If already pending before the command is issued, or if unsuccessful in arbitration during command execution, and conversely selected/reselected by another SCSI device. In the former case an invalid command interrupt is generated following this interrupt.

Execution Phase Code

. 41H: Arbitration phase
. 42H: Initiator reselection phase

RECEIVE	REC
	Information Reception (Target)

Type B

Command Code

7							0
C1	C0	1	0	1	MG	CD	0

C1	C0	Data Setting Operation on Current Transfer Counter	Number of Transfer Bytes and Transfer Byte Unit
0	0	CTCH, CTCM, CTCL ← BTCH, BTCM, BTCL	0 to 16,777,215 bytes Set in 1-byte units
0	1	CTCH, CTCM ← BTCH, BTCM CTCL ← 00H	0 to 16,776,960 bytes Set in 256-byte units
1	0	CTCL ← BTCL CTCH, CTCM ← 0000H	0 to 255 bytes Set in 1-byte units
1	1	CTCH, CTCM, CTCL ← 000001H	Fixed value of 1 (not affected by BTCH, BTCM, BTCL contents)

MG	CD	Information Transfer Bus Phase Setting
0	0	Data out phase
0	1	Command phase
1	0	Use prohibited
1	1	Message out phase

Status Transition T → T

Outline Performs information reception as the target. The bus phase is set by the MG and CD bits in the command code.

Settings Required Before Issuing Command

TMOD register ← Transfer mode
BTCL, BTCM, BTCH registers ← Number of receive bytes

Operation

(1) Bus phase setting
Within a maximum of 12 clock cycles after the command is issued, the $\overline{I}$/O signal is deactivated, and the $\overline{MSG}$ and $\overline{C}$/D signals are output so that the bus phase set by the MG and CD bits is established. Then, after an 8 clock cycle wait, information reception is started.

Bus Phase	$\overline{MSG}$	$\overline{C}$/D
Data out phase	H	H
Command phase	H	L
Message out phase	L	L

(2) Information reception
Information is received from the SCSI bus in accordance with the protocol stipulated in the SCSI-2 specifications. The transfer counter contents are decremented by 1 for each byte received.
The transfer counter countdown timing is as follows:

. Asynchronous mode: Rising edge of $\overline{ACK}$ pulse
. Synchronous mode : Rising edge of $\overline{REQ}$ pulse

(3) Termination

When the contents of the transfer counter become 0, the reception of information from the SCSI bus is terminated and data reception requests are made to the CPU until the FIFO buffer is empty. When the FIFO buffer is empty, the command operation is terminated.
When the command operation is terminated an interrupt request is generated and the command wait mode is entered with the target status set.

Break Operation

Command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set. After the break, the $\overline{EOP}$ signal is activated during the DMA service period.

Abnormal Termination

- o Processing method
  Command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the target status set.
- o Conditions for occurrence
  - . Invalid command
    If this command is issued with the disconnect status or initiator status set.

Also, in the following cases, if an error is detected command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the target status set. The $\overline{EOP}$ signal is activated during the DMA service period after error detection.

- FIFO buffer overrun/underrun
  If a FIFO buffer overrun/underrun is detected during information reception.
- Synchronous transfer offset error
  If the offset between the $\overline{REQ}$ signal and $\overline{ACK}$ signal exceeds the set range (between 0 and the value set in the TMOD register) during a data transfer in the synchronous transfer mode.
- SCSI bus parity error
  If a parity error is detected in the data read from the SCSI bus.
- CPU bus parity error
  If a parity error is detected in the data written to the uPD72611 from the CPU bus during information transmission.
- $\overline{REQ}/\overline{ACK}$ timeout error
  If handshaking in an information transfer pauses for longer than the time set in the RATOUT register.

Operation in Case of Parity Error Detection

- When the PERP bit in the EXMOD register is not set
  When a parity error is detected, command execution is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set, and also the $\overline{EOP}$ signal is activated during the DMA service period after error detection.
- When the PERP bit in the EXMOD register is set
  When a parity error is detected during an information transfer, the transfer is not discontinued immediately but instead continues until the command terminates. After command termination an interrupt request is generated, and the command wait mode is entered with the target status set. It is possible to check whether or not a parity error has been generated by reading the EXST register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

- Command normal termination interrupt
  If the command has terminated normally.
- Invalid command interrupt
  If the command is written other than when the uPD72611 status is "target".
- FIFO buffer overrun/underrun interrupt
  If a FIFO buffer overrun/underrun occurs during command execution.
- Synchronous transfer offset error interrupt
  If a synchronous transfer offset error occurs during command execution.

- SCSI bus parity error interrupt
  If a parity error is detected in the data received from the SCSI bus.
- CPU bus parity error interrupt
  If a parity error is detected in the data received from the CPU bus.
- $\overline{REQ}/\overline{ACK}$ timeout error interrupt
  If a $\overline{REQ}/\overline{ACK}$ timeout error occurs.
- SCSI reset condition interrupt
  If already pending before the command is issued, or if a reset condition is generated during command execution. In the former case an invalid command interrupt is generated following this interrupt.

Execution Phase Code

- 51H: Information reception phase

SEND	SND
	Information Transmission (Target)

Type B

Command Code

7							0
C1	C0	1	0	1	MG	CD	1

C1	C0	Data Setting Operation on Current Transfer Counter	Number of Transfer Bytes and Transfer Byte Unit
0	0	CTCH, CTCM, CTCL ← BTCH, BTCM, BTCL	0 to 16,777,215 bytes Set in 1-byte units
0	1	CTCH, CTCM ← BTCH, BTCM CTCL ← 00H	0 to 16,776,960 bytes Set in 256-byte units
1	0	CTCL ← BTCL CTCH, CTCM ← 0000H	0 to 255 bytes Set in 1-byte units
1	1	CTCH, CTCM, CTCL ← 000001H	Fixed value of 1 (not affected by BTCH, BTCM, BTCL contents)

MG	CD	Information Transfer Bus Phase Setting
0	0	Data in phase
0	1	Status phase
1	0	Use prohibited
1	1	Message in phase

Status Transition T → T

Outline Performs information transmission as the target. The bus phase is set by the MG and CD bits in the command code.

Settings Required Before Issuing Command

TMOD register ← Transfer mode
BTCL, BTCM, BTCH registers ← Number of transmit bytes

Operation

(1) Bus phase setting
Within a maximum of 12 clock cycles after the command is issued, the $\overline{I}/O$ signal is deactivated, and the $\overline{MSG}$ and $\overline{C}/D$ signals are output so that the bus phase set by the MG and CD bits is established. Then, after an 8 clock cycle wait, information transmission is started.

Bus Phase	$\overline{MSG}$	$\overline{C}/D$
Data in phase	H	H
Status phase	H	L
Message in phase	L	L

(2) Information transmission
Information is transmitted from the SCSI bus in accordance with the protocol stipulated in the SCSI-2 specifications. The transfer counter contents are decremented by 1 for each byte transmitted.
The transfer counter countdown timing is as follows:

- Asynchronous mode: Rising edge of $\overline{ACK}$ pulse
- Synchronous mode : Rising edge of $\overline{REQ}$ pulse

(3) Termination

When the contents of the transfer counter become 0, the transmission of information from the SCSI bus is terminated, and the command operation is terminated after the remaining data in the FIFO buffer has been cleared.

When the command operation is terminated an interrupt request is generated and the command wait mode is entered with the target status set.

(4) Caution on transfer counter setting

When sending data, a certain interval is required between writing of the last data from the CPU to the uPD72611 and termination of the command operation (when the transfer counter contents become 0) (see 3.4 "SCSI Transfer Control").

In the case of DMA mode the $\overline{\text{DMARQ}}$ signal remains active until the command operation terminates, and therefore if the DMA controller counter set value is larger than the uPD72611 transfer counter set value the DMA controller transfers excess data to the uPD72611 (although only the quantity of data set in the uPD72611 counter is output to the SCSI bus). At this time the excess data left in the FIFO buffer is cleared, but there is a discrepancy between the transfer data count on the CPU side and the SCSI side.

Therefore, discrepancy between the transfer data on the CPU side and the SCSI side should be avoided by aligning both counter set values and not having the transfer data quantity managed by the DMA controller counter.

Break Operation

Command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set. After the break, the $\overline{EOP}$ signal is activated during the DMA service period.

Abnormal Termination

o Processing method
Command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the target status set.

o Conditions for occurrence
. Invalid command
If this command is issued with the disconnect status or initiator status set.

Also, in the following cases, if an error is detected command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the target status set. The $\overline{EOP}$ signal is activated during the DMA service period after error detection.

. FIFO buffer overrun/underrun
If a FIFO buffer overrun/underrun is detected during information transmission.

- Synchronous transfer offset error
  If the offset between the $\overline{REQ}$ signal and $\overline{ACK}$ signal exceeds the set range (between 0 and the value set in the TMOD register) during a data transfer in the synchronous transfer mode.
- CPU bus parity error
  If a parity error is detected in the data written to the uPD72611 from the CPU bus during information transmission.
- $\overline{REQ}/\overline{ACK}$ timeout error
  If handshaking in an information transfer pauses for longer than the time set in the RATOUT register.

Operation in Case of Parity Error Detection

- When the PERP bit in the EXMOD register is not set
  When a parity error is detected, command execution is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set, and also the $\overline{EOP}$ signal is activated during the DMA service period after error detection.
- When the PERP bit in the EXMOD register is set
  When a parity error is detected during an information transfer, the transfer is not discontinued immediately but instead continues until the command terminates. After command termination an interrupt request is generated, and the command wait mode is entered with the target status set. It is possible to check whether or not a parity error has been generated by reading the EXST register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

- Command normal termination interrupt
  If the command has terminated normally.
- Invalid command interrupt
  If the command is written other than when the uPD72611 status is "target".
- FIFO buffer overrun/underrun interrupt
  If a FIFO buffer overrun/underrun occurs during command execution.
- Synchronous transfer offset error interrupt
  If a synchronous transfer offset error occurs during command execution.
- CPU bus parity error interrupt
  If a parity error is detected in the data received from the CPU bus.
- $\overline{REQ}/\overline{ACK}$ timeout error interrupt
  If a $\overline{REQ}/\overline{ACK}$ timeout error occurs.
- SCSI reset condition interrupt
  If already pending before the command is issued, or if a reset condition is generated during command execution. In the former case an invalid command interrupt is generated following this interrupt.

Execution Phase Code

- 61H: Information phase

AUTO TARGET	ATGT
Automatic Execution of Target Standard Operation	

Type C

Command Code

7							0
0	0	1	1	0	0	0	0

Status Transition D → D, T

Outline

Automatically executes a standard sequence in the case of reception of a command from the initiator as the target.
This command executes consecutively two or four RECEIVE commands executed when selected from the initiator.
The SCSI-2 commands supported by this command are groups 0, 1, 2, 5, 6 and 7.

Settings Required Before Issuing Command

None

Operation

The command processing sequence depends on the status of the $\overline{ATN}$ signal at the time of selection, as shown below.

. When the $\overline{ATN}$ signal is inactive at the time of selection
  (a) Response to selection
  (b) SCSI-2 command (CDB) reception
      RECEIVE (MG = 0, CD = 1)
. When the $\overline{ATN}$ signal is active at the time of selection
  (a) Response to selection
  (b) Identify message reception
      RECEIVE-1 (MG = 1, CD = 1)

(c) SCSI-2 command reception

RECEIVE-2 (MG = 0, CD = 1)

. When the $\overline{ATN}$ signal is active and the MSG3 bit is 1 at the time of selection

(a) Response to selection

(b) Identify message reception

RECEIVE-1 (MG = 1, CD = 1)

(c) Queue tag message 1st byte reception

RECEIVE-2 (MG = 1, CD = 1)

(d) Queue tag message 2nd byte reception

RECEIVE-3 (MG = 1, CD = 1)

(e) SCSI-2 command reception

RECEIVE-4 (MG = 0, CD = 1)

The operation in each sequence is described below.

(1) Select wait

Automatic processing in response to a service request interrupt request due to a selected condition is possible within a maximum of 12 clock cycles after the command is issued.
Therefore, if selection is performed by the initiator after this command is written, a service request interrupt request due to a selected condition is not generated.
If the $\overline{ATN}$ signal is inactive when selection is performed processing proceeds to step (5), or if active, to step (2).

(2) Identify message reception (corresponding to RECEIVE command)
Processing is started corresponding to a RECEIVE command which receives a one-byte message, with the MSG register as the destination. If identify message reception is successful, the $\overline{ATN}$ signal is first sampled. If the $\overline{ATN}$ signal is inactive, processing proceeds to step (5); if the $\overline{ATN}$ signal is active, the MSG3 bit is sampled. If MSG3 = 1, processing proceeds to step (3); if MSG = 0, command execution is terminated and a command normal termination interrupt is generated.

(3) Queue tag message (first byte) reception (corresponding to RECEIVE command)
Processing is started corresponding to a RECEIVE command which receives a one-byte message, with the MSG2 register as the destination. If reception of the first byte of the queue tag message is successful, the $\overline{ATN}$ signal is first sampled. If the $\overline{ATN}$ signal is active, processing proceeds to step (4); if the $\overline{ATN}$ signal is inactive, command execution is terminated and a command normal termination interrupt is generated.

(4) Queue tag message (second byte) reception (corresponding to RECEIVE command)
Processing is started corresponding to a RECEIVE command which receives a one-byte message, with the MSG register as the destination. If reception of the second byte of the queue tag message is successful, the $\overline{ATN}$ signal is first sampled. If the $\overline{ATN}$ signal is inactive, processing proceeds to step (5); if the $\overline{ATN}$ signal is active, command execution is terminated and a command normal termination interrupt is generated.

(5) SCSI-2 command reception (corresponding to RECEIVE command)
Processing is started corresponding to a RECEIVE command which receives an SCSI-2 command with the CDB register contents as the SCSI-2 command (command descriptor block). The length of the CDB received is determined automatically by referencing the operation code received first and stored in the CDB00 register. If the SCSI-2 command reception is successful, processing proceeds to step (6).

(6) Termination
If SCSI-2 command reception is successful and the series of processing sequences terminates normally, an interrupt request is generated and the command wait mode is entered with the target status set.

Break Operation

. During select wait
  Command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the disconnect status set.
. During identify message reception, during queue tag message reception, and during command reception
  Command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set.

Abnormal Termination

o Processing method
  Command processing is discontinued, an interrupt request is generated, and the command wait mode is entered with the target status set.
o Conditions for occurrence
  . Invalid command
    If this command is issued with the initiator status or target status set.
  . Unsupported group
    If the SCSI-2 command group indicated by the operation code of the SCSI-2 command received first in the command phase is not a group supported on the uPD72611. In this case, the command terminates abnormally on reception of the first data in the command phase. The SCSI-2 command operation code is stored in the CDB00 register.
  . SCSI bus parity error
    If a parity error is detected in the message or SCSI-2 command read from the SCSI bus.

- CPU bus parity error
  If a parity error is detected in the data written from the CPU bus in information transmission.
- $\overline{REQ}/\overline{ACK}$ timeout error
  If handshaking in an information transfer pauses for longer than the time set in the RATOUT register.

Service Request

In the identify message reception phase and the queue tag message reception phase, a one-byte message receive operation is performed. The uPD72611 decodes this message simultaneously with reading of the message from the SCSI bus and transfer to the MSG register. If the message is not a relevant message a service interrupt request to the CPU is generated.
At this time the presence of continuous message output phase request from the initiator (continuation of the attention condition) is indicated by the AT bit.

Operation in Case of Parity Error Detection

- When the PERP bit in the EXMOD register is not set
  When a parity error is detected, command execution is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set, and also the $\overline{EOP}$ signal is activated during the DMA service period after error detection.

. When the PERP bit in the EXMOD register is set
When a parity error is detected during an information transfer, the transfer is not discontinued immediately but instead continues until the command terminates. After transfer termination a parity error check is made, and if a parity error has been generated an interrupt request is generated, and the command wait mode is entered with the target status set. In queue tag message reception a parity error check is performed for each one-byte message received. In SCSI-2 command reception, a parity check is also performed directly after successful reception of the first byte. It is possible to check whether or not a parity error has been generated by reading the EXST register, and to confirm the parity error generation phase by reading the TP register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

. Command normal termination interrupt
This interrupt is generated in the following cases. The different interrupts are distinguished by means of the EXST register and the TP register.
(1) If the command has terminated normally (EXST = 00H, TP = 73H/77H).
(2) If the $\overline{ATN}$ signal is active and the MSG3 bit is 0 after reception of the identify message (EXST = 00H, TP = 72H).

(3) If the $\overline{ATN}$ signal is inactive after reception of the first byte of the queue tag message (EXST = 00H, TP = 75H).

(4) If the $\overline{ATN}$ signal is active after reception of the second byte of the queue tag message (EXST = 00H, TP = 76H).

(5) If a parity error has been generated when the PERP bit is set (EXST = 01H/02H; TP register contents are the phase code of the phase in which the parity error was generated).

. Invalid command interrupt
If the command is written other than when the uPD72611 status is "disconnect".

. FIFO buffer overrun/underrun interrupt
If a FIFO buffer overrun/underrun occurs during command execution.

. SCSI bus parity error interrupt
If a parity error is detected in the data received from the SCSI bus.

. CPU bus parity error interrupt
If a parity error is detected in the data received from the CPU bus.

. $\overline{REQ}/\overline{ACK}$ timeout error interrupt
If a $\overline{REQ}/\overline{ACK}$ timeout error occurs.

. Unsupported group interrupt
If an SCSI-2 command of an unsupported group has been sent from an initiator.

. SCSI reset condition interrupt
  If already pending when the command is issued, or if a reset condition is generated during command execution. In the former case the command is acknowledged, and therefore another interrupt is generated following this interrupt.
. Reselected/selected interrupt
  If already pending when the command is issued. In this case an invalid command interrupt is generated following this interrupt.
. Message reception interrupt
  If a message other than a relevant message is received in the message reception phase.

Execution Phase Code

o When a queue tag message is not received
  . 71H: Selected waiting phase
  . 72H: Identify message reception phase
  . 74H: Command first byte reception phase

Only set when PERP = 1 and a parity error is generated in the first byte of the command.

  . 73H: Command reception phase

o When a queue tag message is received
  . 71H: Selected waiting phase
  . 72H: Identify message reception phase
  . 75H: Queue tag message first byte reception phase
  . 76H: Queue tag message second byte reception phase
  . 78H: Command first byte reception phase

Only set when PERP = 1 and a parity error is generated in the first byte of the command.

  . 77H: Command reception phase

AUTO TARGET 2	ATGT2
Automatic Execution of Target Standard Termination Operation	

Type C

Command Code

7							0
0	0	1	1	0	0	0	1

Status Transition T → D, T

Outline Automatically executes a standard sequence when the target terminates an SCSI-2 command received from the initiator. This command executes consecutively the processing of the two SEND commands to be executed when terminating an SCSI-2 command received from the initiator.

Settings Required Before Issuing Command

MSG register ← Command complete message
STS register ← Termination status

Operation The command processing sequence are as follows:

(a) Termination status transmission
SEND command-1 (MG = 0, CD = 1)

(b) Command complete message transmission
SEND command-2 (MG = 1, CD = 1)

The operation in each sequence is described below.

(1) Termination status transmission (corresponding to SEND command)
Within a maximum of 12 clock cycles after the command is issued, processing is started corresponding to a SEND command which sends a one-byte status. If the status transmission is successful, processing proceeds to step (2).

(2) Command complete message transmission (corresponding to SEND command)
Processing corresponding to a SEND command which sends a one-byte message is started. If the message transmission is successful, processing proceeds to step (3).

(3) Termination
If message transmission is successful and the series of processing sequences terminates normally, processing corresponding to a DISCONNECT command which releases the bus is executed, an interrupt request is generated, and the command wait mode is entered with the disconnect status set.

Break Operation

Command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set.

Abnormal Termination

o Processing method
Command processing is discontinued, an interrupt request is generated, and the command wait mode is entered with the target status set.

o Conditions for occurrence

. Invalid command
  If this command is issued with the disconnect status or initiator status set.

. CPU bus parity error
  If a parity error is detected in the command code written from the CPU bus.

. $\overline{REQ}/\overline{ACK}$ timeout error
  If handshaking in an information transfer pauses for longer than the time set in the RATOUT register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

. Command normal termination interrupt
  This interrupt is generated in the following cases. The different interrupts are distinguished by means of the TP register.
  (1) If the command has terminated normally (TP = A3H).
  (2) If the $\overline{ATN}$ signal is active after transmission of the termination status (TP = A1H).
  (3) If the $\overline{ATN}$ signal is activated after transmission of the command complete message (TP = A2H).

. Invalid command interrupt
  If the command is written other than when the uPD72611 status is "target".

. FIFO buffer overrun/underrun interrupt
  If a FIFO buffer overrun/underrun occurs during command execution.

. CPU bus parity error interrupt
  If a parity error is detected in the data received from the CPU bus.

- $\overline{REQ}/\overline{ACK}$ timeout error interrupt
  If a $\overline{REQ}/\overline{ACK}$ timeout error occurs.
- SCSI reset condition interrupt
  If already pending when the command is issued, or if a reset condition is generated during command execution. In the former case the disconnect status is set, and therefore an invalid command interrupt is generated following this interrupt.

Execution Phase Code

- A1H: Termination status transmission phase
- A2H: Command complete message transmission phase
- A3H: Disconnect status

RE-RECEIVE	RREC
Reselect → Data Reception Automatic Execution	

Type C

Command Code

7							0
C1	C0	1	1	1	0	0	0

C1	C0	Data Setting Operation on Current Transfer Counter	Number of Transfer Bytes and Transfer Byte Unit
0	0	CTCH, CTCM, CTCL ← BTCH, BTCM, BTCL	0 to 16,777,215 bytes Set in 1-byte units
0	1	CTCH, CTCM ← BTCH, BTCM CTCL ← 00H	0 to 16,776,960 bytes Set in 256-byte units
1	0	CTCL ← BTCL CTCH, CTCM ← 0000H	0 to 255 bytes Set in 1-byte units
1	1	CTCH, CTCM, CTCL ← 000001H	Fixed value of 1 (not affected by BTCH, BTCM, BTCL contents)

Status Transition D → D, T

Outline As the target, automatically executes sequences from initiator reselection to data reception.
This command consecutively executes one or three SEND commands and one RECEIVE command without a termination interrupt for each command.

Settings Required Before Issuing Command

DID register ← Initiator ID number
TMOD register ← Transfer mode
BTCL, BTCM, BTCH registers ← Number of receive bytes
MSG register ← Identify message

. Only when MSG3 = 1:
MSG2 register ← 1st byte of queue tag message
MSG3 register ← 2nd byte of queue tag message

Operation

The command processing sequences are as follows:

. When MSG3 = 0
  (a) Bus arbitration
  (b) Initiator reselection — RESELECT
  (c) Identify message transmission
      SEND (MG = 1, CD = 1)
  (d) Data reception
      RECEIVE (MG = 0, CD = 0)

. When MSG3 = 1
  (a) Bus arbitration
  (b) Initiator reselection — RESELECT
  (c) Identify message transmission
      SEND-1 (MG = 1, CD = 1)
  (d) Transmission of 1st byte of queue tag message
      SEND-2 (MG = 1, CD = 1)
  (e) Transmission of 2nd byte of queue tag message
      SEND-3 (MG = 1, CD = 1)
  (f) Data reception
      RECEIVE (MG = 0, CD = 0)

The operation in each sequence is described below.

(1) Reselect operation (corresponding to RESELECT command)
Processing corresponding to the RESELECT command is started with in a maximum of 12 clock cycles after the command is issued. If the reselect operation is successful, processing proceeds to step (2).

(2) Identify message transmission (corresponding to SEND command)
Processing is started corresponding to a SEND command which transmits a one-byte message with the MSG register as the identify message source. If the message transmission is successful, processing proceeds to step (3) if MSG3 = 1, or to step (4) if MSG3 = 0.

(3) Queue tag message transmission (2 bytes) (corresponding to SEND command)
Processing is started corresponding to a SEND command which transmits a one-byte message with the MSG2 register as the source of the first byte of a queue tag message. If the message transmission is successful, processing corresponding to a SEND command is then started which transmits a one-byte message with the MSG3 register as the source of the second byte of the queue tag message. If this message transmission is also successful, processing proceeds to step (4).

(4) Data reception (corresponding to RECEIVE command)
Processing is started corresponding to a RECEIVE command which receives the number of transfer data bytes set by the BTCL/BTCM/BTCH registers and C1 & C0 via the FIFO buffer. When the set number of bytes have been transferred and the CTCL/CTCM/CTCH value becomes 0, the reception of information from the SCSI bus is terminated and data reception requests are made to the CPU until the FIFO buffer is empty. When the FIFO buffer is empty, processing proceeds to step (5).

(5) Termination
If data reception is successful and the series of processing sequences terminates normally, an interrupt request is generated and the command wait mode is entered with the target status set.

Break Operation

. During reselect operation
SCSI ID number output to the SCSI bus is immediately discontinued and the $\overline{BSY}$ signal is monitored for 4096 clock cycles with the $\overline{SEL}$ signal still active. If the $\overline{BSY}$ signal is activated within 4096 clock cycles, the uPD72611 waits for 6 clock cycles and then releases the $\overline{SEL}$ signal, completes the selection phase, generates an interrupt request and enters the command wait mode with the target status set.

If the $\overline{BSY}$ signal is not activated within 4096 clock cycles, the uPD72611 releases the SCSI bus due to a selection failure, generates an interrupt request, and enters the command wait mode with the disconnect status set.

. During information transfer
Command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set. After the break, the $\overline{EOP}$ signal is activated during the DMA service period.

Abnormal Termination

o Processing method
Command execution is discontinued, an interrupt is generated, and the command wait mode is entered with the target status set.

o Conditions for occurrence
. Invalid command
If this command is issued with the initiator status or target status set.
. Bus free timeout error
If the bus free phase is not detected within the time set by the BFTOUT register.
. Selection/reselection timeout error
If there is no initiator response to selection within the time set in the SRTOUT register.

Also, in the following cases, if an error is detected command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the target status set. The $\overline{EOP}$ signal is activated during the DMA service period after error detection.

- FIFO buffer overrun/underrun
  If a FIFO buffer overrun/underrun is detected during data reception.
- Synchronous transfer offset error
  If the offset between the $\overline{REQ}$ signal and $\overline{ACK}$ signal exceeds the set range (between 0 and the value set in the TMOD register) during a data transfer in the synchronous transfer mode.
- SCSI bus parity error
  If a parity error is detected in the data read from the SCSI bus.
- $\overline{REQ}/\overline{ACK}$ timeout error
  If handshaking in an information transfer pauses for longer than the time set in the RATOUT register.

Operation in Case of Parity Error Detection

- When the PERP bit in the EXMOD register is not set
  When a parity error is detected, command execution is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set, and also the $\overline{EOP}$ signal is activated during the DMA service period after error detection.
- When the PERP bit in the EXMOD register is set
  When a parity error is detected during a data transfer, the transfer is not discontinued immediately but instead continues until command execution terminates. It is possible to check whether or not a parity error has been generated by reading the EXST register, and to confirm the parity error generation phase by reading the TP register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

- Command normal termination interrupt
  This interrupt is generated in the following cases. The different interrupts are distinguished by means of the EXST register and the TP register.
  (1) If the command has terminated normally (EXST = 00H, TP = 84H).
  (2) If the $\overline{ATN}$ signal is activated after transmission of the identify message (EXST = 00H, TP = 83H).
  (3) If the $\overline{ATN}$ signal is activated after transmission of the first byte of the queue tag message (EXST = 00H, TP = 85H).
  (4) If the $\overline{ATN}$ signal is activated after transmission of the second byte of the queue tag message (EXST = 00H, TP = 86H).
  (5) If a parity error has been generated when the PERP bit is set (EXST = 01H/02H; TP register contents are the phase code of the phase in which the parity error was generated).
- Invalid command interrupt
  If the command is written other than when the uPD72611 status is "disconnect".
- FIFO buffer overrun/underrun interrupt
  If a FIFO buffer overrun/underrun occurs during command execution.
- Synchronous transfer offset error interrupt
  If a synchronous transfer offset error occurs during command execution.

- SCSI bus parity error interrupt
  If a parity error is detected in the data received from the SCSI bus.
- CPU bus parity error interrupt
  If the parity added to the command is incorrect.
- Bus free timeout error interrupt
  If the bus free phase is not detected within a given time.
- Selection/reselection timeout error interrupt
  If there is no response from the target within a given time.
- $\overline{\text{REQ}}/\overline{\text{ACK}}$ timeout error interrupt
  If a $\overline{\text{REQ}}/\overline{\text{ACK}}$ timeout error occurs.
- SCSI reset condition interrupt
  If already pending when the command is issued, or if a reset condition is generated during command execution. In the former case the command is acknowledged, and therefore another interrupt is generated following this interrupt.
- Reselected/selected interrupt
  If already pending before the command is issued, or if unsuccessful in arbitration during command execution, and conversely selected/reselected by another SCSI device. In the former case an invalid command interrupt is generated following this interrupt.

Execution Phase Code

- 81H: Arbitration phase
- 82H: Initiator reselection phase
- 83H: Identify message transmission phase
- 85H: Queue tag message 1st byte transmission phase
- 86H: Queue tag message 2nd byte transmission phase
- 84H: Data reception phase

RE-SEND	RSND
Reselect → Data Transmission Automatic Execution	

Type C

Command Code

7							0
C1	C0	1	1	1	0	0	1

C1	C0	Data Setting Operation on Current Transfer Counter	Number of Transfer Bytes and Transfer Byte Unit
0	0	CTCH, CTCM, CTCL ← BTCH, BTCM, BTCL	0 to 16,777,215 bytes Set in 1-byte units
0	1	CTCH, CTCM ← BTCH, BTCM CTCL ← 00H	0 to 16,776,960 bytes Set in 256-byte units
1	0	CTCL ← BTCL CTCH, CTCM ← 0000H	0 to 255 bytes Set in 1-byte units
1	1	CTCH, CTCM, CTCL ← 000001H	Fixed value of 1 (not affected by BTCH, BTCM, BTCL contents)

Status Transition D → D, T

Outline

As the target, automatically executes sequences from initiator reselection to data transmission.
This command consecutively executes two or four SEND commands without a termination interrupt for each command.

Settings Required Before Issuing Command

DID register ← Initiator ID number
TMOD register ← Transfer mode
BTCL, BTCM, BTCH registers ← Number of receive bytes
MSG register ← Identify message

. Only when MSG3 = 1:
  MSG2 register ← 1st byte of queue tag message
  MSG3 register ← 2nd byte of queue tag message

Operation

The command processing sequences are as follows:

. When MSG3 = 0
  (a) Bus arbitration
  (b) Initiator reselection — RESELECT
  (c) Identify message transmission
      SEND (MG = 1, CD = 1)
  (d) Data transmission
      SEND (MG = 0, CD = 0)

. When MSG3 = 1
  (a) Bus arbitration
  (b) Initiator reselection — RESELECT
  (c) Identify message transmission
      SEND-1 (MG = 1, CD = 1)
  (d) Transmission of 1st byte of queue tag message
      SEND-2 (MG = 1, CD = 1)
  (e) Transmission of 2nd byte of queue tag message
      SEND-3 (MG = 1, CD = 1)
  (d) Data transmission
      SEND (MG = 0, CD = 0)

The operation in each sequence is described below.

(1) Reselect operation (corresponding to RESELECT command)
Processing corresponding to the RESELECT command is started with in a maximum of 12 clock cycles after the command is issued. If the reselect operation is successful, processing proceeds to step (2).

(2) Identify message transmission (corresponding to SEND command)
Processing is started corresponding to a SEND command which transmits a one-byte message. If the message transmission is successful, processing proceeds to step (3) if MSG3 = 1, or to step (4) if MSG3 = 0.

(3) Queue tag message transmission (2 bytes) (corresponding to SEND command)
Processing is started corresponding to a SEND command which transmits a one-byte message with the MSG2 register as the source of the first byte of a queue tag message. If the message transmission is successful, processing corresponding to a SEND command is then started which transmits a one-byte message with the MSG3 register as the source of the second byte of the queue tag message. If this message transmission is also successful, processing proceeds to step (4).

(4) Data transmission (corresponding to SEND command)
Processing is started corresponding to a SEND command which transmits the number of transmission data bytes set by the BTCL/BTCM/BTCH registers and C1 & C0 via the FIFO buffer. When the set number of data bytes have been transferred and the CTCL/CTCM/CTCH value becomes 0, the transmission of information on the SCSI bus is terminated, the FIFO buffer is cleared, and processing proceeds to step (5).

(5) Termination
If the data transmission is successful and the series of processing sequences terminates normally, an interrupt request is generated and the command wait mode is entered with the target status set.

(6) Caution on transfer counter setting
When sending data, a certain interval is required between writing of the last data from the CPU to the uPD72611 and termination of the command operation (when the transfer counter contents become 0) (see 3.4 "SCSI Transfer Control").

In the case of DMA code the $\overline{\text{DMARQ}}$ signal remains active until the command operation terminates, and therefore if the DMA controller counter set value is larger than the uPD72611 transfer counter set value the DMA controller transfers excess data to the uPD72611 (although only the quantity of data set in the uPD72611 counter is output to the SCSI bus). At this time the excess data left in the FIFO buffer is cleared, but there is a discrepancy between the transfer data count on the CPU side and the SCSI side. Therefore, discrepancy between the transfer data on the CPU side and the SCSI side should be avoided by aligning both counter set values and not having the transfer data quantity managed by the DMA controller counter.

Break Operation

. During reselection

SCSI ID number output to the SCSI bus is immediately discontinued and the $\overline{\text{BSY}}$ signal is monitored for 4096 clock cycles with the $\overline{\text{SEL}}$ signal still active. If the $\overline{\text{BSY}}$ signal is activated within 4096 clock cycles, the uPD72611 waits for 6 clock cycles and then releases the $\overline{\text{SEL}}$ signal, completes the selection phase, generates an interrupt request and enters the command wait mode with the target status set.

If the $\overline{BSY}$ signal is not activated within 4096 clock cycles, the uPD72611 releases the SCSI bus due to a selection failure, generates an interrupt request, and enters the command wait mode with the disconnect status set.

. During information transfer
Command processing is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set. After the break, the $\overline{EOP}$ signal is activated during the DMA service period.

Abnormal Termination

o Processing method
Command execution is discontinued, an interrupt is generated, and the command wait mode is entered with the disconnect status set.

o Conditions for occurrence
. Invalid command
If this command is issued with the initiator status or target status set.
. Bus free timeout error
If the bus free phase is not detected within the time set by the BFTOUT register.
. Selection/reselection timeout error
If there is no initiator response to reselection within the time set in the SRTOUT register.

Also, in the following cases, if an error is detected command execution is discontinued, an interrupt request is generated, and the command wait mode is entered with the target status set. The $\overline{EOP}$ signal is activated during the DMA service period after error detection.

- FIFO buffer overrun/underrun
  If a FIFO buffer overrun/underrun is detected during data transmission.
- Synchronous transfer offset error
  If the offset between the $\overline{REQ}$ signal and $\overline{ACK}$ signal exceeds the set range (between 0 and the value set in the TMOD register) during a data transfer in the synchronous transfer mode.
- CPU bus parity error
  When a parity error is detected in the data written from the CPU bus to the uPD72611 during information transmission.
- $\overline{REQ}/\overline{ACK}$ timeout error
  If handshaking in an information transfer pauses for longer than the time set in the RATOUT register.

Operation in Case of Parity Error Detection

- When the PERP bit in the EXMOD register is not set
  When a parity error is detected, command execution is discontinued immediately, an interrupt request is generated, and the command wait mode is entered with the target status set, and also the $\overline{EOP}$ signal is activated during the DMA service period after error detection.

- When the PERP bit in the EXMOD register is set
  When a parity error is detected during a data transfer, the transfer is not discontinued immediately but instead continues until command execution terminates. It is possible to check whether or not a parity error has been generated by reading the EXST register, and to confirm the parity error generation phase by reading the TP register.

Interrupts which may be Set at End of Execution (other than reset or break during execution)

- Command normal termination interrupt
  This interrupt is generated in the following cases. The different interrupts are distinguished by means of the EXSTS register and the TP register.
  (1) If the command has terminated normally (EXST = 00H, TP = 94H).
  (2) If the $\overline{ATN}$ signal is activated after transmission of the identify message (EXST = 00H, TP = 93H).
  (3) If the $\overline{ATN}$ signal is activated after transmission of the first byte of the queue tag message (EXST = 00H, TP = 95H).
  (4) If the $\overline{ATN}$ signal is activated after transmission of the second byte of the queue tag message (EXST = 00H, TP = 96H).

(5) If a parity error has been generated when the PERP bit is set (EXST = 01H/02H; TP register contents are the phase code of the phase in which the parity error was generated).

- Invalid command interrupt
  If the command is written other than when the uPD72611 status is "disconnect".
- FIFO buffer overrun/underrun interrupt
  If a FIFO buffer overrun/underrun occurs during command execution.
- Synchronous transfer offset error interrupt
  If a synchronous transfer offset error occurs during command execution.
- CPU bus parity error interrupt
  If there is a parity error in the data received from the CPU bus.
- Bus free timeout error interrupt
  If the bus free phase is not detected within a given time.
- Selection/reselection timeout error interrupt
  If there is no response from the target within a given time.
- $\overline{REQ}/\overline{ACK}$ timeout error interrupt
  If a $\overline{REQ}/\overline{ACK}$ timeout error occurs.
- SCSI reset condition interrupt
  If already pending when the command is issued, or if a reset condition is generated during command execution. In the former case the command is acknowledged, and therefore another interrupt is generated following this interrupt.

. Reselected/selected interrupt
If already pending before the command is issued, or if unsuccessful in arbitration during command execution, and conversely selected/reselected by another SCSI device. In the former case an invalid command interrupt is generated following this interrupt.

Execution Phase Code

. 91H: Arbitration phase
. 92H: Initiator reselection phase
. 93H: Identify message transmission phase
. 95H: Queue tag message 1st byte transmission phase
. 96H: Queue tag message 2nd byte transmission phase
. 94H: Data transmission phase

5.3 COMMAND CODES

Table 5-2 Command Codes

Type	Command Name	Command Code							
Group I	CHIP RESET	0	0	0	0	0	0	0	0
	BREAK	0	0	0	0	0	0	0	1
	DISCONNECT	0	0	0	0	0	0	1	0
	CLEAR FIFO	0	0	0	0	0	1	0	1
	SCSI RESET	0	0	0	0	1	0	0	0
Group II	SET ATN	0	0	0	0	0	0	1	1
	RESET ACK	0	0	0	0	0	1	0	0
	SELECT	0	0	0	1	AT	0	0	0
	TRANSFER	C1	C0	0	1	0	0	1	0
	AUTO INITIATOR	C1	C0	0	1	AT	1	0	0
	AUTO INITIATOR 2	C1	C0	0	1	0	1	0	1
Group III	RESELECT	0	0	1	0	0	0	0	0
	RECEIVE	C1	C0	1	0	1	MG	CD	0
	SEND	C1	C0	1	0	1	MG	CD	1
	AUTO TARGET	0	0	1	1	0	0	0	0
	AUTO TARGET 2	0	0	1	1	0	0	0	1
	RE-RECEIVE	C1	C0	1	1	1	0	0	0
	RE-SEND	C1	C0	1	1	1	0	0	1

Remarks: Meaning of command bits (See individual commands for details.)

C1, C0: Count selection bits
AT : $\overline{\text{ATN}}$ signal status specification bit
MG, CD: Transfer information specification bits

CHAPTER 6. CONTROL

6.1 uPD72611 OPERATIONS

uPD72611 operations can be broadly classified into command processing initiated by a command issued by the CPU, and processing in response to SCSI bus status transitions.

(1) Command processing

Command processing depends on the type of command.

(i) Type A commands (auxiliary commands) except CHIP RESET

The command is executed immediately. After execution of the command, the command wait mode is entered.

(ii) CHIP RESET command

A reset operation is started immediately. After the reset is completed, an interrupt request to the CPU is generated, indicating termination of command processing.

(iii) Type B and C commands

Command processing is started after command writing has been synchronized with the system clock. When individual processing ends, an interrupt request to the CPU is generated, indicating termination of command processing.

(2) Response processing

In the command wait mode, the uPD72611 monitors the SCSI bus phase. When selected/reselected by another SCSI device while the disconnect status is set, a response operation is performed.

Also, when there is a bus phase transition during the information transfer phase when the initiator status is set, a post-transition bus phase detection/ notification operation is performed.

When the uPD72611 is monitoring the $\overline{\text{RST}}$ signal on the SCSI bus and detects a reset condition, whatever status is set, the uPD72611 executes an operation to handle this and then notifies the CPU.

6.2 OUTLINE OF HOST CPU PROCESSING OPERATIONS

Processing performed by the CPU with respect to the uPD72611 can be broadly classified into command issuance processing by means of a CPU-side request, and interrupt servicing in response to termination of an operation specified by a command or a service request in response to an SCSI bus status transition.

6.2.1 COMMAND ISSUANCE PROCESSING

The processing flow depends on the type of command issued. The operation flow is outlined in Figure 6-1.

(1) Type A commands (auxiliary commands) except CHIP RESET

This type of command can be issued even when the uPD72611 is executing a type B or C command and has the busy status set. No settings are required before issuing the command. Command processing is completed when the command is written. Therefore, it is not necessary to wait for command completion, and the next processing can be proceeded to directly.

However, the BREAK command is only executed when the busy status is set, and is therefore ignored if issued when the status is non-busy.

(2) CHIP RESET command

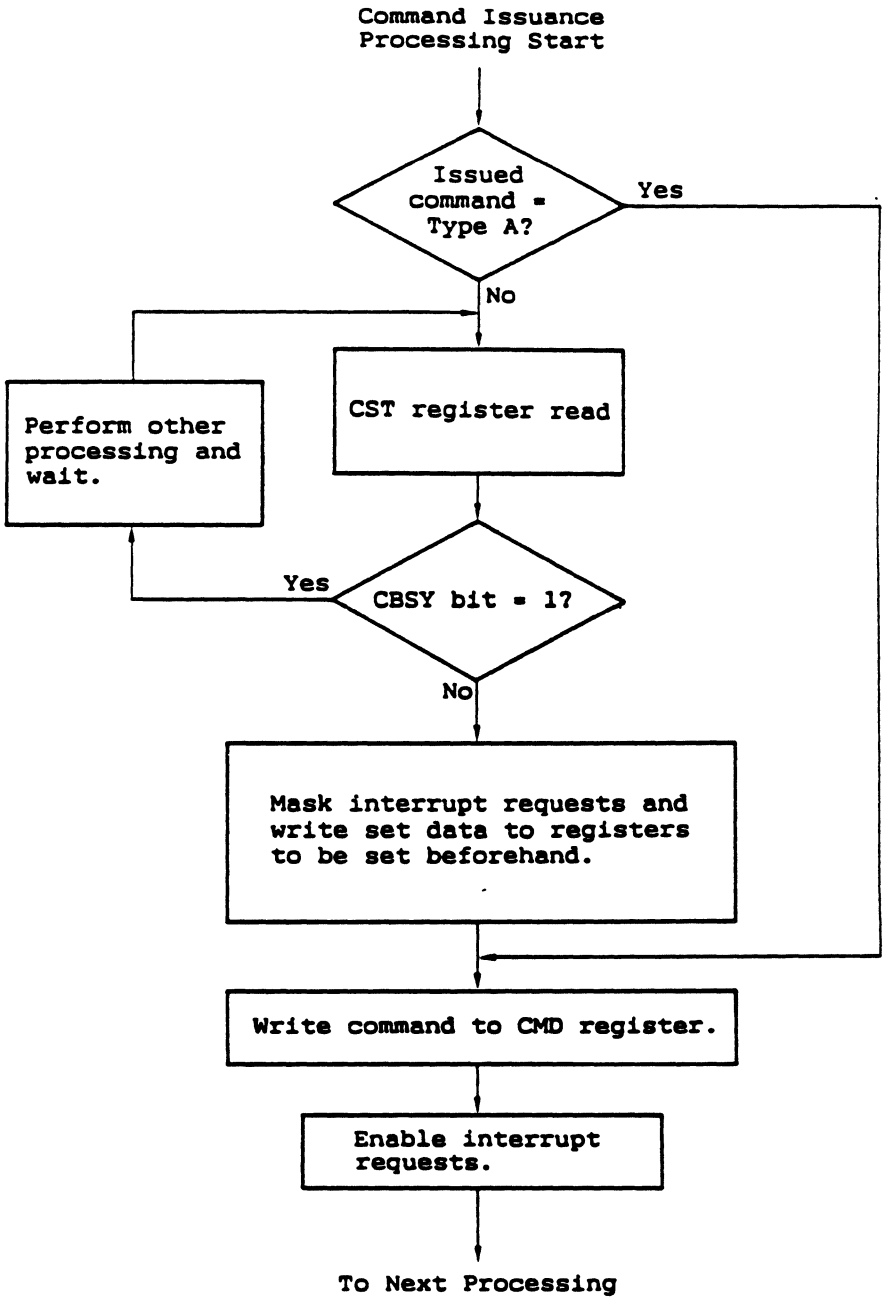
This command can be issued even when the uPD72611 is executing a type B or C command and has the busy status set. No settings are required before issuing the command. Command processing starts as soon as the command is written, and completion of the reset is indicated by an interrupt request. Command termination is thus detected by a command termination interrupt request.

(3) Type B and C commands

These commands can only be issued when the uPD72611 status is non-busy (when the CBSY bit of the CST register is 0). After the necessary registers for the command processing to be executed are first set, the CPU reads the CST register to check the status of the uPD72611, and issues the command after confirming that the status is non-busy. If the uPD72611 status is busy, the CPU waits until the status changes to non-busy or executes other processing and then waits for the status to become non-busy.

Command processing starts as soon as the command is written, and completion of the command is indicated by an interrupt request. Command termination is thus detected by a command termination interrupt request.

Figure 6-1 Command Issuance Processing Operation Flow



6.2.2 CAUTION ON uPD72611 INITIALIZATION

In the uPD72611 a reset interrupt is generated immediately after a reset ($\overline{\text{RESET}}$ signal or CHIP RESET command), and thus interrupt servicing is necessary.

All registers except CST, DID, IST, CTCL, CTCM, CTCH and MOD are reset to 00H, and must therefore be initialized. The following points should be noted in particular with regard to the mode register and physical ID register.

(1) Mode register (MOD)

- HPS and DHP bits
  Immediately after a reset, HPS = 0 and DHP = 1 (parity disabled). When parity is supported on the CPU side, a parity error is generated.
- RAEN and SAEN bits
  Immediately after a reset, RAEN = 0 and SAEN = 0 (no response to selection/reselection by another SCSI terminal). When the uPD72611 is used in a system in which there is a possibility of selection/reselection by another SCSI terminal during initialization, setting of these bits should be performed last.

(2) Physical ID register

- FEN bit
  Immediately after a reset this bit is 0 (no operation as the SCSI bus controller). When this bit is 0, the SCSI RESET command is not executed.

Remarks: In the uPD72111 the mode register is reset to 00H by a reset. Therefore, since the DHP bit is 0 (CPU bus odd parity check performed), a parity error is generated by a data write to a register when odd parity is not supported on the CPU side. Even if this error is ignored and writing is continued, the write to the register is performed correctly. However, the command issuance (data write to CMD) associated with the parity error is ignored. Also, the CHIP RESET command is not executed.

6.2.3 INTERRUPT SERVICING

The uPD72611 generates interrupts to the CPU resulting from the following two sources:

- Command termination
- Generation of a service request to the CPU

The CPU must detect and service these interrupt requests. The operation flow for this is outlined in Figure 6-2.

When an interrupt request is acknowledged, the CPU first reads the IST register and checks the type of interrupt. It then performs the following processing.

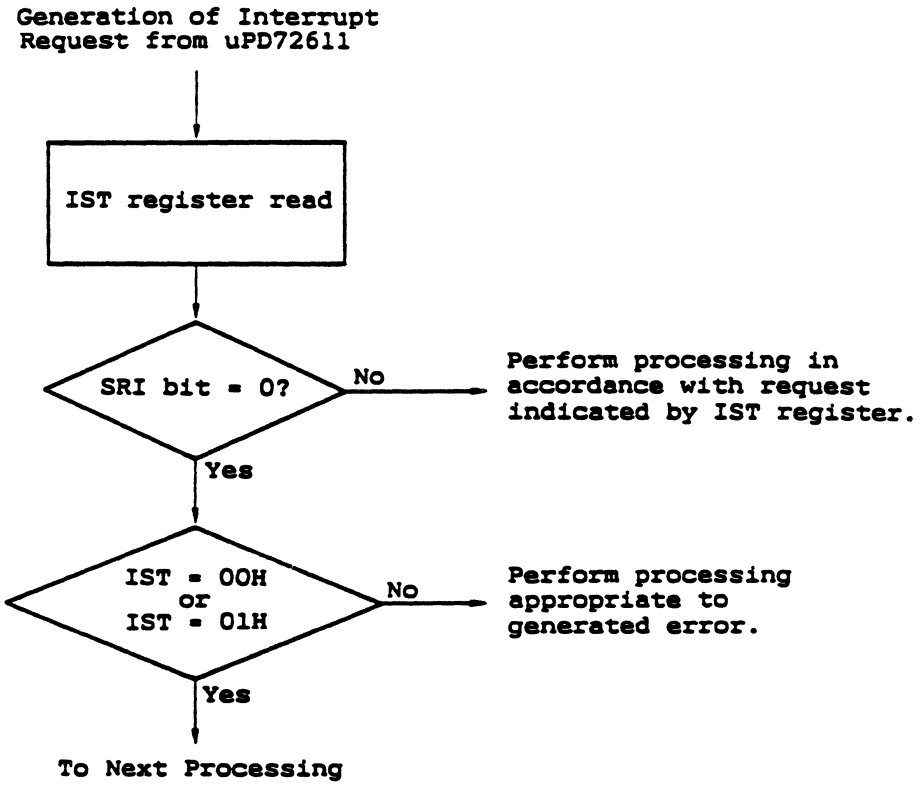
(1) For an interrupt due to command termination (either normal termination or abnormal termination)

The CPU performs processing appropriate to the executed command or generated error in accordance with the contents of the IST register read.

(2) For an interrupt due to a service request to the CPU

The CPU performs processing required by the uPD72611 in accordance with the contents of the IST register read.

Figure 6-2 Interrupt Service Operation Flow



6.3 CONTROL SEQUENCE

6.3.1 HOST ADAPTER CONTROL

When an SCSI-2 host adapter is configured using the uPD72611, the control procedure which should be performed by the CPU is as follows:

(1) uPD72611 initialization

When an interrupt request is acknowledged, the host reads the contents of the IST register to determine the interrupt source. If this indicates a reset interrupt, the host performs internal register initialization as shown in the table below. Actual set values are given in Chapter 4 "Internal Registers".

Register Name	Setting
BFTOUT	Bus free monitoring time
SRTOUT	Selection/reselection response wait time
RATOUT	$\overline{REQ}$/$\overline{ACK}$ handshake response wait time
CDBL	Command descriptor block length
XEMOD	Operating mode
MOD	Operating mode
PID	Own ID number and enabling of operation as controller

(2) Target selection

(a) Setting of ID number of target to be selected

The ID number of the target to be selected is set in the DID register.

(b) Issuance of SELECT command

When the identify message is sent in the following sequence the AT bit in the command code is set to 1, and otherwise to 0, and the SELECT command is issued.

(c) Wait for termination interrupt request

(3) Message transmission

When an interrupt request is acknowledged, the host reads the contents of the IST register to determine the interrupt source. If this indicates a message out phase start interrupt, the host performs the following processing.

(a) Setting of number of transfer bytes

The transfer counter is set with the message length as the number of transfer bytes. If the message is one byte in length, the setting can be performed using the C1 and C0 bits in the command code.

(b) Issuance of TRANSFER command

(c) Writing message to data FIFO registers

The message to be sent is written in order to the DF0/1/2 registers in accordance with the request of the DRQ bit of the CST register.

(d) Wait for termination interrupt request

(4) SCSI-2 command transmission

When an interrupt request is acknowledged, the host reads the contents of the IST register to determine the interrupt source. If this indicates a command phase start interrupt, the host performs the following processing.

(a) Setting of number of transfer bytes

The CDB length is set in the transfer counter as the number of transfer bytes.

(b) Issuance of TRANSFER command

(c) Writing SCSI-2 command to data FIFO registers

The CDB of the SCSI-2 command to be sent is written in order to the DF0/1/2 registers in accordance with the request of the DRQ bit of the CST register.

(d) Wait for termination interrupt request

(5) Data transmission

When an interrupt request is acknowledged, the host reads the contents of the IST register to determine the interrupt source. If this indicates a data out phase start interrupt, the host performs the following processing.

(a) Setting of number of transfer bytes

The transfer data length is set in the transfer counter as the number of transfer bytes.

(b) Issuance of TRANSFER command

(c) Writing send data to data FIFO registers

The means of control depends on the transfer mode. The transfer mode is specified by the DMA bit of the MOD register.

In the DMA mode, a DMA transfer is performed and the send data is written in order to the DFO/1/2 registers in accordance with the $\overline{\text{DMARQ}}$ signal.

In the program I/O mode, the send data is written in order to the DFO/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(d) Wait for termination interrupt request

(6) Data reception

When an interrupt request is acknowledged, the host reads the contents of the IST register to determine the interrupt source. If this indicates a data in phase start interrupt, the host performs the following processing.

(a) Setting of number of transfer bytes

The transfer data length is set in the transfer counter as the number of transfer bytes.

(b) Issuance of TRANSFER command

(c) Reading receive data from data FIFO registers

The means of control depends on the transfer mode. The transfer mode is specified by the DMA bit of the MOD register.

In the DMA mode, a DMA transfer is performed and the receive data is read in order from the DF0/1/2 registers in accordance with the $\overline{\text{DMARQ}}$ signal.

In the program I/O mode, the receive data is read in order from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(d) Wait for termination interrupt request

(7) Status reception

When an interrupt request is acknowledged, the host reads the contents of the IST register to determine the interrupt source. If this indicates a status phase start interrupt, the host performs the following processing.

(a) Issuance of TRANSFER command

The C1 and C0 bits in the command code are both set to 1, and a one-byte transfer TRANSFER command is issued.

(b) Reading status from data FIFO registers

The receive status is read from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(c) Wait for termination interrupt request

(8) Message reception

When an interrupt request is acknowledged, the host reads the contents of the IST register to determine the interrupt source. If this indicates a message in phase start interrupt, the host performs the following processing.

(a) Issuance of TRANSFER command

The C1 and C0 bits in the command code are both set to 1, and a one-byte transfer TRANSFER command is issued.

(b) Reading message from data FIFO registers

The receive message is read from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(c) Wait for message reception interrupt request

(d) Determination of message type

(e) Issuance of RESET ACK command

A RESET ACK command is issued to conclude the message reception protocol.

If the receive message is not an extended message, processing is terminated at this point. If the receive message is an extended message, the following processing is performed.

(f) Issuance of TRANSFER command

The C1 and C0 bit sin the command code are both set to 1, and a one-byte transfer TRANSFER command is issued.

(g) Reading message from data FIFO registers

The receive message is read from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(h) Wait for message reception interrupt request

(i) Issuance of RESET ACK command

A RESET ACK command is issued to conclude the message reception protocol.

(j) Setting of number of transfer bytes

The length of the extended message read from the DF0/1/2 registers is set in the transfer counter as the number of transfer bytes.

(k) Issuance of TRANSFER command

(l) Reading extended message from data FIFO registers

The receive message is read from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(m) Wait for message reception interrupt request

(n) Issuance of RESET ACK command

A RESET ACK command is issued to conclude the extended message reception protocol.

(9) Disconnect

When an interrupt request is acknowledged, the host reads the contents of the IST register to determine the interrupt source. If this indicates a disconnected interrupt, the host prepares for reselection without performing any particular processing.

(10) Reselection

When an interrupt request is acknowledged, the host reads the contents of the IST register to determine the interrupt source. If this indicates a reselected interrupt, the host performs the following processing.

(a) Reading target ID

The ID of the reselecting target is read from the SID register in preparation for the subsequent identify message reception and data transmission/reception.

(11) Automatic execution of host adapter sequence (from target selection to reception of command completed message)

The processing procedure is as follows:

(a) Internal register setting

Register Name	Setting
DID	ID number of target to be selected
MSG	Identify message to be sent to target
MSG2	1st byte of queue tag message to be sent to target
MSG3	2nd byte of queue tag message to be sent to target
CDB	SCSI-2 command descriptor block to be sent target
Transfer counter	Transfer data length

(b) Issuance of AUTO INITIATOR command

(c) Send/receive data transfer via data FIFO registers

The means of control depends on the transfer mode. The transfer mode is specified by the DMA bit of the MOD register.

In the DMA mode, a DMA transfer is performed and the send/receive data is transferred to/from the DF0/1/2 registers in accordance with the $\overline{\text{DMARQ}}$ signal.

In the program I/O mode, the send/receive data is transferred to/from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(d) Wait for termination interrupt request

(e) Reading SCSI-2 command execution status

The SCSI-2 command execution status is read from the TST register to confirm termination of the SCSI-2 command.

(12) Automatic execution of host adapter sequence (from data phase after reselection to reception of command completed message)

(a) Setting of number of transfer bytes

The transfer data length is set in the transfer counter as the number of transfer bytes.

(b) Issuance of AUTO INITIATOR 2 command

(c) Send/receive data transfer via data FIFO registers

The means of control depends on the transfer mode. The transfer mode is specified by the DMA bit of the MOD register.

In the DMA mode, a DMA transfer is performed and the send/receive data is transferred to/from the DF0/1/2 registers in accordance with the $\overline{\text{DMARQ}}$ signal.

In the program I/O mode, the send/receive data is transferred to/from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(d) Wait for termination interrupt request

(e) Reading SCSI-2 command execution status and command completed message

The SCSI-2 command execution status and command completed message are read from the TST and MSG registers to confirm termination status of the SCSI-2 command.

6.3.2 DEVICE ADAPTER CONTROL

The control procedure when an SCSI-2 device adapter is configured using the uPD72611 is shown below.

(1) uPD72611 initialization

When an interrupt request is acknowledged, the contents of the IST register to determine the interrupt source. If this indicates a reset interrupt, the following processing is performed.

(a) Internal register initialization

Register Name	Setting
BFTOUT	Bus free monitoring time
SRTOUT	Selection/reselection response wait time
RATOUT	$\overline{REQ}$/$\overline{ACK}$ handshake response wait time
CDBL	Command descriptor block length
XEMOD	Operating mode
MOD	Operating mode
PID	Own ID number and enabling of operation as controller

(2) Selection

When an interrupt request is acknowledged, the contents of the IST register are read to determine the interrupt source. If this indicates a selected interrupt, the following processing is performed.

(a) Reading source ID

The ID of the selected SCSI-2 device is read from the SID register in preparation for the subsequent reselect operation, etc.

(3) Message reception

(a) Issuance of RECEIVE command

The C1, C0, MSG and C/D bits in the command code are all set to 1, and a one-byte RECEIVE command is issued.

(b) Reading message from data FIFO registers

The receive message is read from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(c) Determination of message type

The receive message is decoded and the message type determined.

(d) Wait for termination interrupt request

If the receive message is not an extended message, processing is terminated at this point. If the receive message is an extended message, the following processing is performed.

(e) Issuance of RECEIVE command

The C1, C0, MSG and C/D bits in the command code are all set to 1, and a one-byte transfer RECEIVE command is issued.

(f) Reading message from data FIFO registers

The receive message is read from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(g) Wait for termination interrupt

(h) Setting of number of transfer bytes

The length of the extended message read from the DF0/1/2 registers is set in the transfer counter as the number of transfer bytes.

(i) Issuance of RECEIVE command

The MSG and C/D bits in the command code are both set to 1, and a RECEIVE command is issued.

(j) Reading extended message from data FIFO registers

The receive message is read from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(k) Wait for termination interrupt request

(4) SCSI-2 command reception

(a) Issuance of RECEIVE command

The C1 and C0 bits in the command code are both set to 1, the MSG bit to 0 and the C/D bit to 1, and a one-byte RECEIVE command is issued.

(b) Reading operation code from data FIFO registers

The operation code of the received SCSI-2 command is read from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(c) Wait for termination interrupt request

(d) Setting of number of transfer bytes

The group of the SCSI-2 command is decoded from the operation code read, and CDB length - 1 is set in the transfer counter as the number of transfer bytes.

(e) Issuance of RECEIVE command

The MSG and C/D bits in the command code are set to 0 and 1 respectively, and a RECEIVE command is issued.

(f) Reading SCSI-2 command from data FIFO registers

The CDB of the SCSI-2 command to be sent is read in order from the DF0/1/2 registers in accordance with the request of the DRQ bit of the CST register.

(g) Wait for termination interrupt request

(5) Data transmission

(a) Setting of number of transfer bytes

The transfer data length is set in the transfer counter as the number of transfer bytes.

(b) Issuance of SEND command

The MSG and C/D bits in the command code are both set to 0, and a SEND command is issued.

(c) Writing send data to data FIFO registers

The means of control depends on the transfer mode. The transfer mode is specified by the DMA bit of the MOD register.

In the DMA mode, a DMA transfer is performed and the send data is written in order to the DFO/1/2 registers in accordance with the $\overline{\text{DMARQ}}$ signal.

In the program I/O mode, the send data is written in order to the DFO/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(d) Wait for termination interrupt request

(6) Data reception

(a) Setting of number of transfer bytes

The transfer data length is set in the transfer counter as the number of transfer bytes.

(b) Issuance of RECEIVE command

The MSG and C/D bits in the command code are both set to 0, and a RECEIVE command is issued.

(c) Reading receive data from data FIFO registers

The means of control depends on the transfer mode. The transfer mode is specified by the DMA bit of the MOD register.

In the DMA mode, a DMA transfer is performed and the receive data is read in order from the DF0/1/2 registers in accordance with the $\overline{\text{DMARQ}}$ signal.

In the program I/O mode, the receive data is read in order from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(d) Wait for termination interrupt request

(7) Status transmission

(a) Issuance of SEND command

The C1 and C0 bits in the command code are both set to 1, the MSG bit to 0 and the C/D bit to 1, and a one-byte SEND command is issued.

(b) Writing status to data FIFO registers

The send status is written to the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(c) Wait for termination interrupt request

(8) Message transmission

(a) Setting of number of transfer bytes

The transfer counter is set with the message length as the number of transfer bytes. If the message is one byte in length, the setting can be performed using the C1 and C0 bits in the command code.

(b) Issuance of SEND command

The MSG and C/D bits in the command code are both set to 1, and a SEND command is issued.

(c) Writing message to data FIFO registers

The message to be sent is written in order to the DF0/1/2 registers in accordance with the request of the DRQ bit of the CST register.

(d) Wait for termination interrupt request

(9) Automatic execution of device adapter sequence (from selection to SCSI-2 command reception)

(a) Issuance of AUTO TARGET command

(b) Wait for termination interrupt request

When a termination interrupt request is acknowledged, the contents of the IST register, TP register and EXST register are read, and if these indicate a normal termination interrupt the following processing is executed.

(c) Reading identify message

The identify message is read from the MSG register.

(d) Reading queue tag message

The queue tag message is read from the MSG2, 3 registers.

(e) Reading SCSI command

The SCSI command descriptor block stored in registers CDB00 to CDB11 is read.

(10) Automatic execution of device adapter sequence (from termination status transmission to command complete message transmission)

(a) STS register setting

The termination status to be sent is set in the STS register.

(b) MSG register setting

The command complete message is set in the MSG register.

(c) Issuance of AUTO TARGET 2 command

(d) Wait for termination interrupt request

(11) Automatic execution of reselect sequence (transmission)

(a) MSG register setting

The identify message is set in the MSG register.

(b) MSG2 register setting

The first byte of the queue tag message to be sent to the target is set in the MSG2 register.

(c) MSG3 register setting

The second byte of the queue tag message to be sent to the target is set in the MSG3 register.

(d) Setting of number of transfer bytes

The transfer data length is set in the message counter as the number of transfer bytes.

(e) Issuance of RE-SEND command

(f) Writing send data to data FIFO registers

The means of control depends on the transfer mode. The transfer mode is specified by the DMA bit of the MOD register.

In the DMA mode, a DMA transfer is performed and the send data is written in order to the DF0/1/2 registers in accordance with the $\overline{\text{DMARQ}}$ signal.

In the program I/O mode, the send data is written in order to the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(g) Wait for termination interrupt request

(12) Automatic execution of reselect sequence (reception)

(a) MSG register setting

The identify message is set in the MSG register.

(b) MSG2 register setting

The first byte of the queue tag message to be sent to the target is set in the MSG2 register.

(c) MSG3 register setting

The second byte of the queue tag message to be sent to the target is set in the MSG3 register.

(d) Setting of number of transfer bytes

The transfer data length is set in the message counter as the number of transfer bytes.

(e) Issuance of RE-RECEIVE command

(f) Reading receive data from data FIFO registers

The means of control depends on the transfer mode. The transfer mode is specified by the DMA bit of the MOD register.

In the DMA mode, a DMA transfer is performed and the receive data is read in order from the DF0/1/2 registers in accordance with the $\overline{\text{DMARQ}}$ signal.

In the program I/O mode, the receive data is read in order from the DF0/1/2 registers in accordance with the request of the DRQ bit in the CST register.

(g) Wait for termination interrupt request

CHAPTER 7. SYSTEM CONFIGURATION

This chapter shows examples of host adapter/device adapter configurations using the uPD72611.

Figure 7-1 System Configuration Example

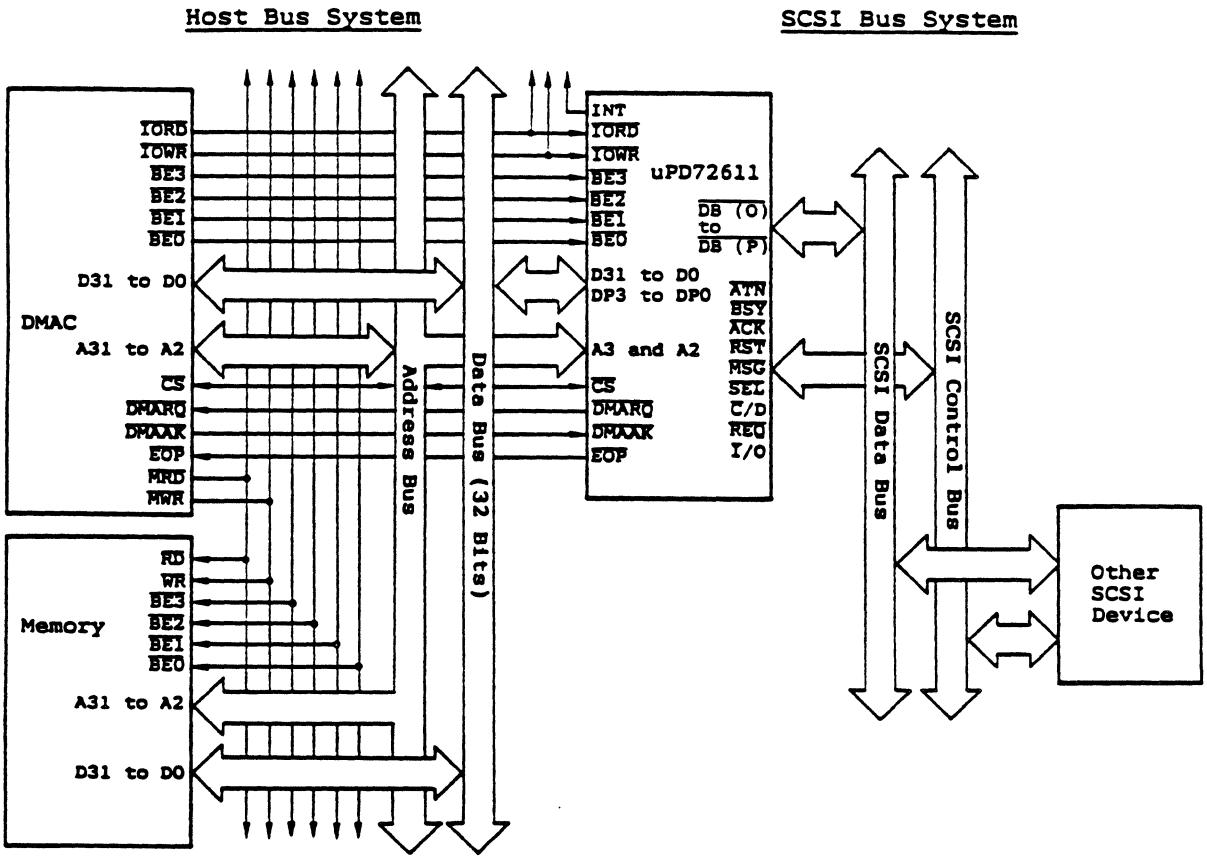


Figure 7-2 Example of External Differential Driver Configuration (SCSI Control Bus)

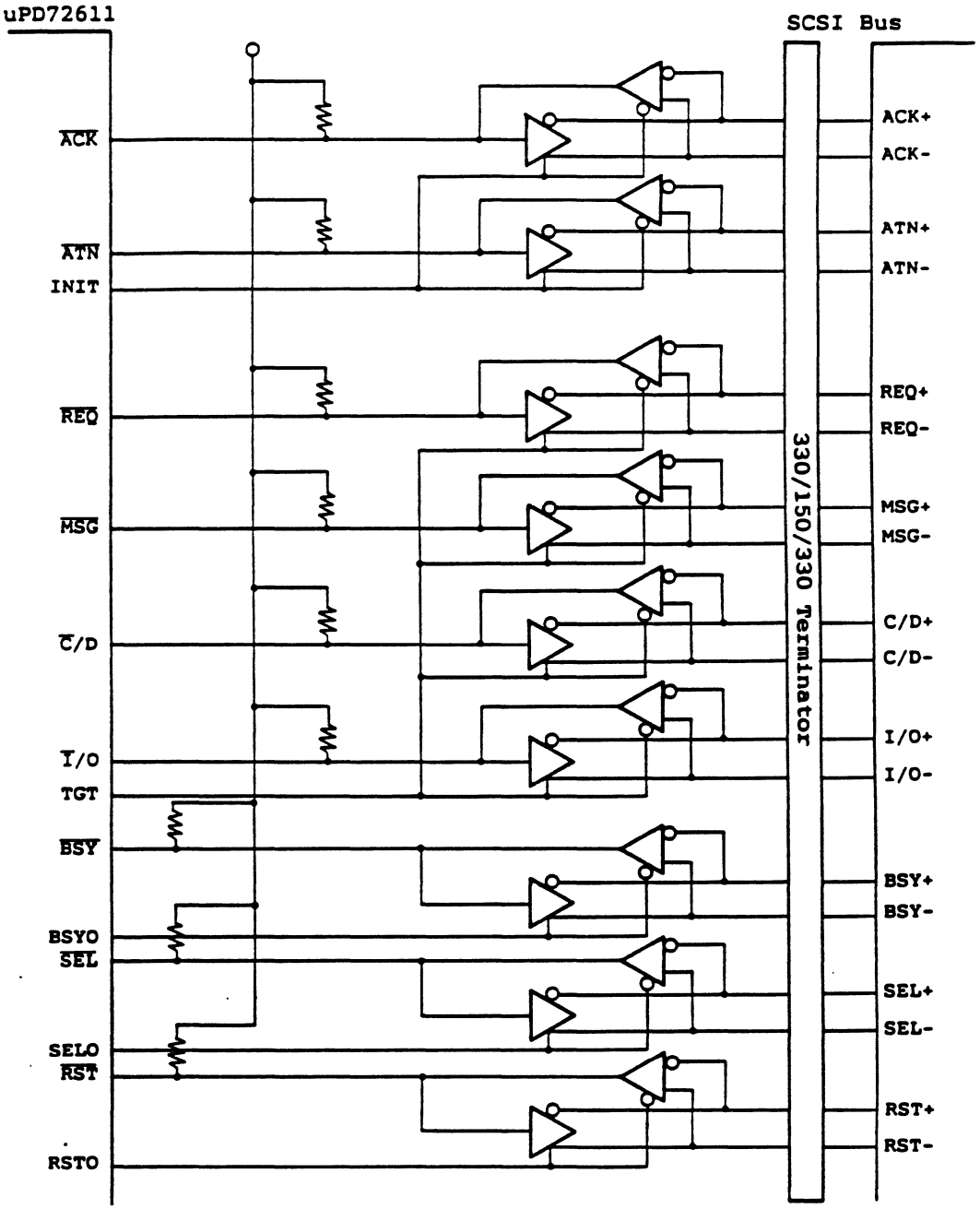
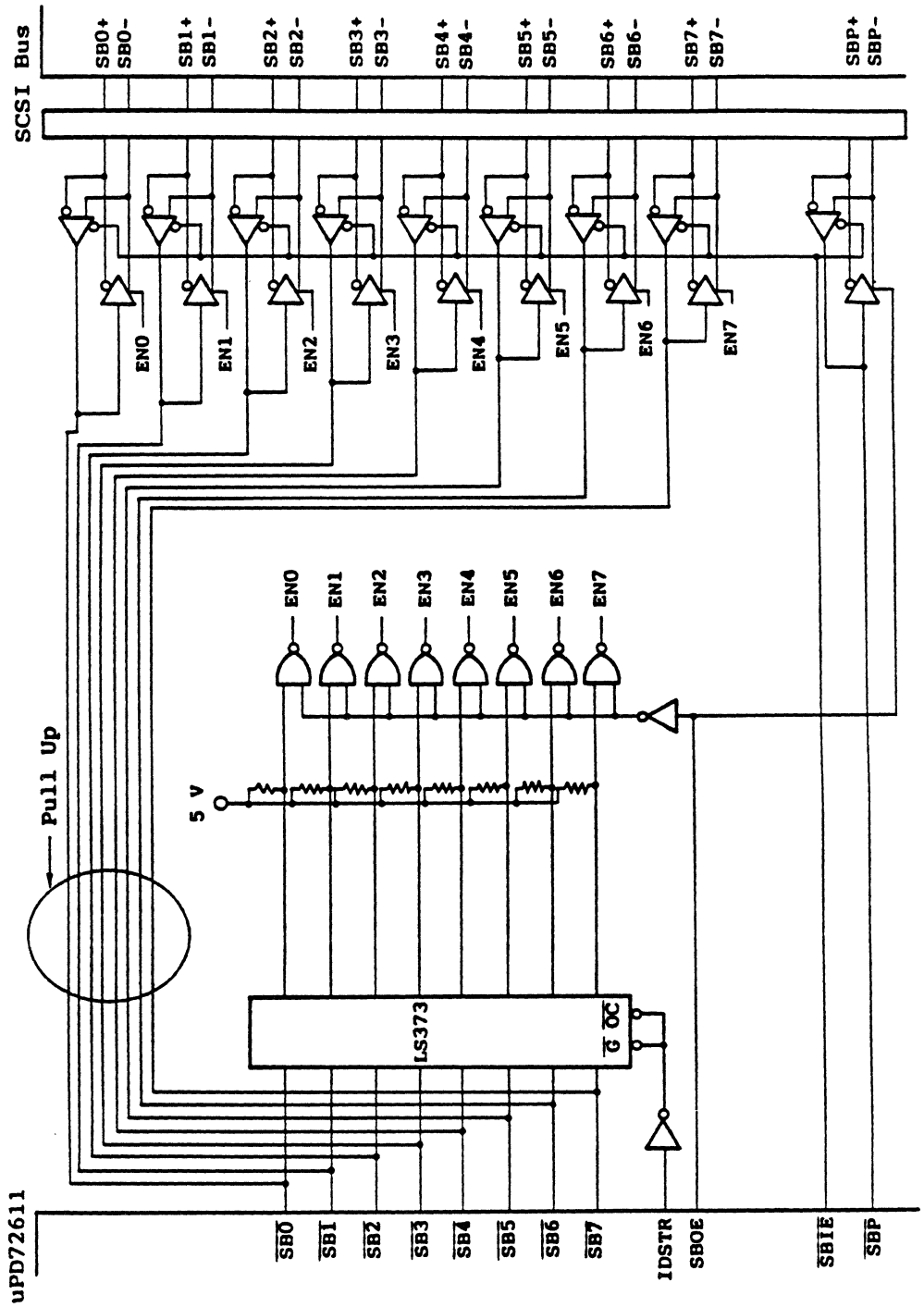


Figure 7-3 Example of External Differential Driver Configuration (SCSI Data Bus)



NEC

NEC Electronics Inc.

CORPORATE HEADQUARTERS

401 Ellis Street
P.O. Box 7241
Mountain View, CA 94039
TEL 415-960-6000
TLX 3715792

For literature, call toll-free 8 a.m. to 4 p.m. Pacific time:
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