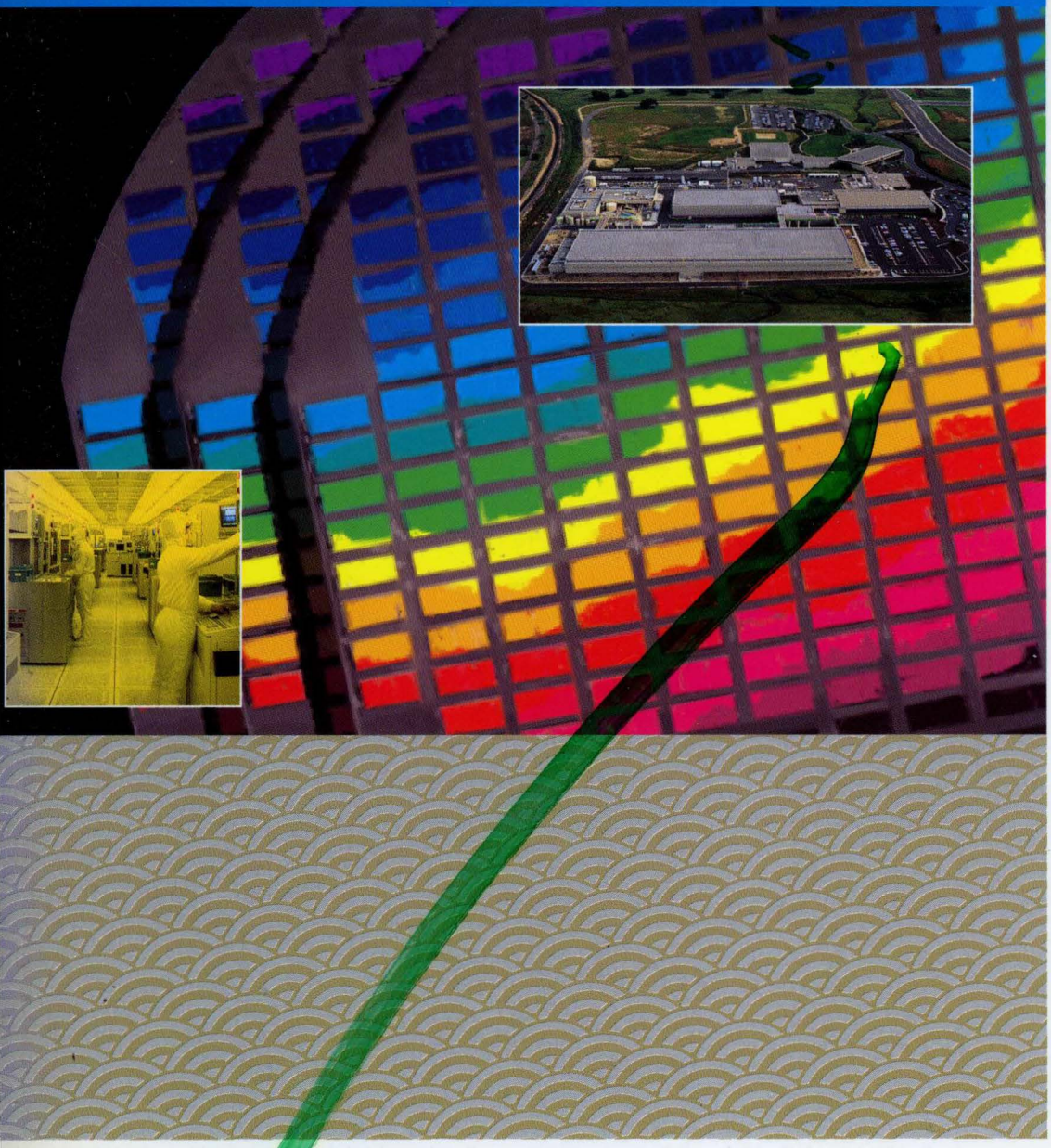

MEMORY PRODUCTS DATA BOOK

Volume 2 of 2

SRAMs, ASMs, EEPROMs

NEC

1993
MEMORY PRODUCTS
DATA BOOK

Volume 2 of 2
SRAMs, ASMs, EEPROMs

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NEC

Volume 1

Section 1. General Information

Section 2. Reliability and Quality Control

Section 3. 256K DRAMs

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Section 4. 1M DRAMs

Section 5. 4M DRAMs (4M x 1 and 1M x 4)

Volume 1 (cont)

Section 6. 4M DRAMs (512K x 8/9)

Section 7. 4M DRAMs (256K x 16/18)

Volume 1 (cont)

Section 7. 4M DRAMs (256K x 16/18) (cont)

Section 8. 16M DRAMs

Volume 1 (cont)

Section 8. 16M DRAMs (cont)

μPD	Organization	Features	
4216900	2M x 9	Fast-page; 4K refresh	8j
4216900L	2M x 9	Fast-page; 4K refresh; 3.3-volt	
42S16900	2M x 9	Fast-page; 4K refresh; self-refresh	
42S16900L	2M x 9	Fast-page; 4K refresh; self-refresh; 3.3-volt	
4217900	2M x 9	Fast-page; 2K refresh	
4217900L	2M x 9	Fast-page; 2K refresh; 3.3-volt	
42S17900	2M x 9	Fast-page; 2K refresh; self-refresh	
42S17900L	2M x 9	Fast-page; 2K refresh; self-refresh; 3.3-volt	
4216902	2M x 9	Static-column	8k
4216160	1M x 16	Fast-page; 4K refresh	8l
4216160L	1M x 16	Fast-page; 4K refresh; 3.3-volt	
42S16160	1M x 16	Fast-page; 4K refresh; self-refresh	
42S16160L	1M x 16	Fast-page; 4K refresh; self-refresh; 3.3-volt	
4217160	1M x 16	Fast-page; 2K refresh	
4217160L	1M x 16	Fast-page; 2K refresh; 3.3-volt	
42S17160	1M x 16	Fast-page; 2K refresh; self-refresh	
42S17160L	1M x 16	Fast-page; 2K refresh; self-refresh; 3.3-volt	
4218160	1M x 16	Fast-page; 1K refresh	
4218160L	1M x 16	Fast-page; 1K refresh; 3.3-volt	
42S18160	1M x 16	Fast-page; 1K refresh; self-refresh	
42S18160L	1M x 16	Fast-page; 1K refresh; self-refresh; 3.3-volt	
4216180	1M x 18	Fast-page; 4K refresh	8m
4216180L	1M x 18	Fast-page; 4K refresh; 3.3-volt	
42S16180	1M x 18	Fast-page; 4K refresh; self-refresh	
42S16180L	1M x 18	Fast-page; 4K refresh; self-refresh; 3.3-volt	
4217180	1M x 18	Fast-page; 2K refresh	
4217180L	1M x 18	Fast-page; 2K refresh; 3.3-volt	
42S17180	1M x 18	Fast-page; 2K refresh; self-refresh	
42S17180L	1M x 18	Fast-page; 2K refresh; self-refresh; 3.3-volt	
4218180	1M x 18	Fast-page; 1K refresh	
4218180L	1M x 18	Fast-page; 1K refresh; 3.3-volt	
42S18180	1M x 18	Fast-page; 1K refresh; self-refresh	
42S18180L	1M x 18	Fast-page; 1K refresh; self-refresh; 3.3-volt	

Volume 1 (cont)

Section 9. DRAM Modules (256K/512K x n)

Section 10. DRAM Modules (1M/2M x n)

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Section 18. Application Specific Devices (See App Notes 54 thru 58, 90-03, 90-06.)

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Section 19. Fast Static RAMs (64K)

Section 20. Fast Static RAMs (256K)

Section 21. Fast Static RAMs (1M)

Section 22. Fast Static RAMs (4M)

Section 23. Cache Data RAMs

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Volume 2 (cont)

Section 27. EEPROMs

Section 28. Application Notes

Section 29. Package Drawings

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Section 17
General Information

The 1993 MEMORY DATA BOOK is for your reference. The most complete information available at printing is included; however, several new devices will be available soon. The table below gives you a preview. For further assistance, contact one of the sales offices.

Upcoming Products

Description	Device Number	Comments
DRAM SIMM Modules		
4M x 8 DRAM Module	MC-424000A8BB/FB	Uses 16M devices
4M x 9 DRAM Module	MC-424000A9BB/FB	Uses 16M devices
16M x 8 DRAM Module	MC-4216000A8BH/FA/AA	Uses 16M devices
16M x 9 DRAM Module	MC-4216000A9BH/FA/AA	Uses 16M devices
4M x 40 DRAM Module	MC-424000AA40BH/FH	Uses 16M devices
8M x 40 DRAM Module	MC-428000AA40BH/FH	Uses 16M devices
Video RAMs		
4M Video RAM	μPD482445	256K x 16; RAM port access times to 60 ns; serial port access times to 15 ns; 64-pin SSOP, 70-pin TSOP
Standard SRAMs		
32K x 8	μPD43256A-10X, 12X	−25 to +85°C; speeds to 100 ns
32K x 8	μPD43256A-10Y, 12Y	−40 to +85°C; speeds to 100 ns
32K x 8	μPD43256B-A12	3.0 to 5.5 V; 120-ns access time
32K x 8	μPD43256B-B12	2.7 to 5.5 V; 120-ns access time
128K x 8	μPD431000A-70X, 85X, 100X	−25 to +85°C; speeds to 70 ns
128K x 8	μPD431000A-70Y, 85Y, 100Y	−40 to +85°C; speeds to 70 ns
128K x 8	μPD431000B-55L/LL, 70L/LL, 85L/LL	Low power; speeds to 55 ns
128K x 8	μPD431000B-B10, B12	2.7 to 5.5 V; speeds to 100 ns
128K x 9	μPD431003	Low power; speeds to 55 ns; two Chip Enables
128K x 9	μPD431003-B10, B12	2.7 to 5.5 V; speeds to 100 ns; two Chip Enables
512K x 8	μPD434000-B15	2.7 to 5.5 V; 150-ns access time; two Chip Enables
BiCMOS Fast SRAMs		
32K x 8	μPD46258	Speeds to 6 ns; 3.3- and 5-V versions
32K x 9	μPD46259	Speeds to 6 ns; 3.3- and 5-V versions
128K x 8	μPD461008	Speeds to 8 ns; 3.3- and 5-V versions
128K x 9	μPD461009	Speeds to 8 ns; 3.3- and 5-V versions
64K x 16	μPD461016	Speeds to 8 ns; 3.3- and 5-V versions
64K x 18	μPD461018	Speeds to 8 ns; 3.3- and 5-V versions

Upcoming Products (cont)

Description	Device Number	Comments
ECL RAMs (10K Interface)		
16K x 4	μPD10494	T_{AA} = 6, 7 ns; 28-pin PDIP/PFP
16K x 4	μPD10494LL	Tcycle = 10, 12 ns; 32-pin PDIP/PFP
32K x 9	μPD10509	Tcycle = 6, TDQ=3; registered I/O, scannable; 52-pin PLCC
64K x 4	μPD10504	T_{AA} = 8, 10 ns; 32-pin PDIP/PFP
ECL RAMs (101/100K Interface)		
16K x 4	μPD101/100494	T_{AA} = 6, 7 ns; 28-pin PDIP/PFP
16K x 4	μPD101/100494LL	Tcycle = 10, 12 ns; 32-pin PDIP/PFP
32K x 9	μPD101/100509	Tcycle = 6, TDQ=3; registered I/O, scannable; 52-pin PLCC
64K x 4	μPD101/100504	T_{AA} = 8, 10 ns; 32-pin PDIP/PFP

Manufacturing in Roseville, California

The planning was completed in 1981, ground was broken in 1982 and products were rolling off the line in 1984 at our semiconductor fabrication facility in Roseville, California. This milestone represented NEC's bold approach to "make products where the customer lives," and it was the first such venture by a Japanese semiconductor company in the United States. The foresight of this decision has paid off handsomely for NEC, its U.S. customers and for the community of greater Sacramento, the capital of California. The original facility has been manufacturing 256K DRAMs and VRAMs, 32K x 8 SRAMs, CMOS ASICs and single-chip microprocessors using 1.2-micron CMOS and NMOS technologies.

Now another milestone has been reached. In November 1991, production of the 4M DRAM began from a newly constructed 456,000-square-foot plant. Combined with the existing 220,000 square-foot facility, NEC Electronics (NECEL) in Roseville is one of the largest merchant fab lines in the world, according to industry source DataQuest.

In addition to the 4M DRAM, the new plant will be capable of producing advanced VLSI products including 16M DRAMs, 4M SRAMs as well as ASICs and microprocessors. The expanded facility will be able to produce 30,000 6-inch wafers per month using 0.55-micron CMOS technology.

The fab has been designed with the most sophisticated technology available, incorporating state-of-the-art environmental controls and efficiencies. A considerable amount of money has been invested for this purpose, as NEC regards environmental conservation as one of the most important international issues.

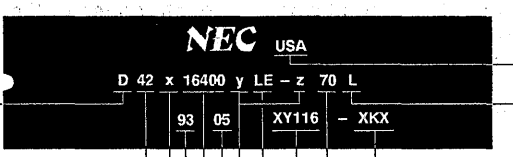
When running at full capacity, equipment in place will allow up to 60-percent of the water used for the DI process to be recycled—an important benefit for drought-ridden California. In addition, the new plant has eliminated the use of chlorofluorocarbons (CFC) in the manufacturing process. (The existing facility will eliminate all CFC usage by 1993.)

NECEL's manufacturing presence in Roseville is of significant benefit to the local community as well as the state of California. When running at full capacity, the plant will employ over 1,350 people, and nearly $5 million in tax revenue will be generated for the city, county and state.

As one of the biggest employers in the area, NECEL views itself as a partner with the local community and takes seriously its role as a good corporate citizen. Through numerous community relations activities, employees volunteer their time to support worthwhile educational and charitable causes. The company also has a generous policy for contributions and donations of equipment and money to help maintain a high quality of life for the area's residents.

In addition to the manufacturing facility in Roseville, NECEL has headquarter offices in Mountain View, California, in the heart of Silicon Valley. Sales offices are located throughout the United States so that customers have immediate access to qualified personnel. These national presences, combined with on-shore manufacturing capabilities, allow NEC Electronics to respond quickly to customer demand and to work closely with customers to meet their changing requirements. The company considers quality customer service to be a number one priority, a trademark of all NEC operations worldwide.

The NECEL facility in Roseville is an outstanding example of successful cultural meshing, offering the best of both worlds. The results are production yields and quality standards that are among the highest obtained by any NEC semiconductor manufacturing facility anywhere.



Country of Origin

Device Type
B = Digital bipolar
D = Digital MOS

Low-Power Indicator (Optional)
L = Low power
LL = Very low power

Date Code Year / Week

NEC Lot Code

TSOP Pinout Identifier
(Middle letter is significant)
J = Normal pinouts
K = Reverse pinouts

Product Class

10	10K ECL RAM
100	100K ECL RAM
23(H)C	CMOS ROM
27(H)C	CMOS EPROM
28C	CMOS EEPROM
28F	CMOS flash memory
41	NMOS dynamic RAM
42	CMOS dynamic RAM
43	CMOS static RAM
44	CMOS static RAM (6-T cell)
46	BiCMOS static RAM
48	CMOS application specific device

Speed Selection

–10	100 ns or 10 ns
–12	120 ns or 12 ns
–15	150 ns or 15 ns
–50	50 ns
–60	60 ns
–70	70 ns
–80	80 ns
–85	85 ns
–XX	Etc.

DRAM Option
S = Self-refresh and low-power devices

DRAM Power Supply

y	z	
–	–	5V ±10%
A	–	5V ±10% (with internal voltage regulator)
–	A	3.0 – 5.5V
–	B	2.7 – 5.5V
L	A	3.3V ±10%
L	B	3.0V ±10%

Device Identifier

Package

B or BH	Ceramic flatpack
C, CR or CZ	Plastic DIP (dual inline package)
D, DH, DX or DZ	Cerdip or ceramic DIP
G (≤ 40 pins), GU or GW	Plastic SOP (small-outline package)
G (> 40 pins) or GF	Plastic QFP (quad flatpack)
G5, GX or GZ	Plastic TSOP (thin small-outline package)
K	Ceramic LCC (leadless chip carrier)
L	PLCC (plastic leaded chip carrier)
LA, LB or LE	Plastic SOJ (small-outline J-lead package)
R	Ceramic PGA (pin grid array)
V	Plastic ZIP (zigzag inline package)

Notes:
(1) The marking location and format may vary among package types.
(2) Regardless of the format, the device number does not change.
(3) The "μP" in NEC part numbers does not appear on the package.

83SL-7321B

DRAMs

Size	Organ-ization	μPD	Features	Row Access Time (ns)	Package and Pins				Sect.
					SOJ	TSOP	ZIP	Other	
256K	256K x 1	41256	Page	80, 85, 100				16-DIP, 18-PLCC	3a
	64K x 4	41464	Page	80, 100, 120				16-DIP 18-PLCC	3b
1M	1M x 1	421000	FP	60, 70, 80, 100	26/20	24/20	20	18-DIP	4a
	256K x 4	424256	FP	60, 70, 80, 100	26/20	24/20	20	20-DIP	4b
4M	4M x 1	424100	FP	60, 70, 80, 100	26/20	26/20	20		5a
	4M x 1	424100A	FP	50, 60, 70, 80	26/20	26/20	20		
	4M x 1	424100L	FP; 3.3 V	70, 80	26/20	26/20	20		
	4M x 1	42S4100A	FP; SR	50, 60, 70, 80	26/20	26/20	20		
	4M x 1	42S4100L	FP; SR; 3.3 V	70, 80	26/20	26/20	20		
	4M x 1	424101	Nibble	60, 70, 80, 100	26/20	26/20	20		5b
	4M x 1	424102	SC	60, 70, 80, 100	26/20	26/20	20		5c
	1M x 4	424400	FP	60, 70, 80	26/20	26/20	20		5d
	1M x 4	424400A	FP	50, 60, 70, 80	26/20	26/20	20		
	1M x 4	424400L	FP; 3.3 V	70, 80	26/20	26/20	20		
	1M x 4	42S4400A	FP; SR	50, 60, 70, 80	26/20	26/20	20		
	1M x 4	42S4400L	FP; SR; 3.3 V	70, 80	26/20	26/20	20		
	1M x 4	424402	SC	60, 70, 80, 100	26/20	26/20	20		5e
	1M x 4	424410	FP; WPB	60, 70, 80, 100	26/20	26/20	20		5f
	1M x 4	424412	SC; WPB	60, 70, 80, 100	26/20	26/20	20		5g
	1M x 4	424440	FP; 4 $\overline{\text{CAS}}$	60, 70, 80	26/24				5h
	1M x 4	424440L	FP; 4 $\overline{\text{CAS}}$; 3.3 V	60, 70, 80	26/24				
	1M x 4	42S4440	FP; 4 $\overline{\text{CAS}}$; SR	60, 70, 80	26/24				
	1M x 4	42S4440L	FP; 4 $\overline{\text{CAS}}$; SR; 3.3 V	60, 70, 80	26/24				

FP Fast page
SR Self-refresh
SC Static column
WPB Write-per-bit

DRAMs (cont)

Size	Organ-ization	μPD	Features	Row Access Time (ns)	Package and Pins			Sect.
					SOJ	TSOP	ZIP	
4M (cont)	512K x 8	424800A	FP	60, 70, 80	28	28	28	6a
	512K x 8	424800L	FP; 3.3V	60, 70, 80	28	28	28	
	512K x 8	42S4800A	FP; SR	60, 70, 80	28	28	28	
	512K x 8	42S4800L	FP; SR; 3.3 V	60, 70, 80	28	28	28	
	512K x 8	424810A	FP; WPB	60, 70, 80	28	28	28	6b
	512K x 8	424810L	FP; WPB; 3.3 V	60, 70, 80	28	28	28	
	512K x 8	42S4810A	FP; WPB; SR	60, 70, 80	28	28	28	
	512K x 8	42S4810L	FP; WPB; SR; 3.3 V	60, 70, 80	28	28	28	
	512K x 9	424900A	FP	60, 70, 80	28	28	28	6c
	512K x 9	424900L	FP; 3.3 V	60, 70, 80	28	28	28	
	512K x 9	42S4900A	FP; SR	60, 70, 80	28	28	28	
	512K x 9	42S4900L	FP; SR; 3.3 V	60, 70, 80	28	28	28	
	256K x 16	424170A	FP; 2 $\overline{WE}$; 1K ref	60, 70, 80	40	44/40	40	7a
	256K x 16	424170L	FP; 2 $\overline{WE}$; 1K ref; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	42S4170A	FP; 2 $\overline{WE}$; 1K ref; SR	60, 70, 80	40	44/40	40	
	256K x 16	42S4170L	FP; 2 $\overline{WE}$; 1K ref; SR; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 18	424190A	FP; 2 $\overline{WE}$; 1K ref	60, 70, 80	40	44/40	40	7b
	256K x 18	424190L	FP; 2 $\overline{WE}$; 1K ref; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 18	42S4190A	FP; 2 $\overline{WE}$; 1K ref; SR	60, 70, 80	40	44/40	40	
	256K x 18	42S4190L	FP; 2 $\overline{WE}$; 1K ref; SR; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	424260A	FP; 2 $\overline{CAS}$; 512 ref	60, 70, 80	40	44/40	40	7c
	256K x 16	424260L	FP; 2 $\overline{CAS}$; 512 ref; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	42S4260A	FP; 2 $\overline{CAS}$; 512 ref; SR	60, 70, 80	40	44/40	40	
	256K x 16	42S4260L	FP; 2 $\overline{CAS}$; 512 ref; SR; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	424263A	FP; 2 $\overline{CAS}$; 512 ref; WPB	60, 70, 80	40	44/40	40	7d
	256K x 16	424263L	FP; 2 $\overline{CAS}$; 512 ref; WPB; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 16	42S4263A	FP; 2 $\overline{CAS}$; 512 ref; WPB; SR	60, 70, 80	40	44/40	40	
	256K x 16	42S4263L	FP; 2 $\overline{CAS}$; 512 ref; WPB; SR; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 18	424280A	FP; 2 $\overline{CAS}$; 512 ref	60, 70, 80	40	44/40	40	7e
	256K x 18	424280L	FP; 2 $\overline{CAS}$; 512 ref; 3.3 V	60, 70, 80	40	44/40	40	
	256K x 18	42S4280A	FP; 2 $\overline{CAS}$; 512 ref; SR	60, 70, 80	40	44/40	40	
	256K x 18	42S4280L	FP; 2 $\overline{CAS}$; 512 ref; SR; 3.3 V	60, 70, 80	40	44/40	40	

FP Fast page
SR Self-refresh
WPB Write-per-bit
ref Refresh
$\overline{WE}$ Write enable

DRAMs (cont)

Size	Organ-ization	μPD	Features	Row Access Time (ns)	Packages and Pins			Sect.
					SOJ	TSOP	ZIP	
16M	16M x 1	4216100	FP; 4K ref	60, 70, 80, 100	28/24	28/24	24	8a
	16M x 1	4217100	FP; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	16M x 1	4216101	Nibble; 4K ref	60, 70, 80, 100	28/24	28/24	24	8b
	16M x 1	4217101	Nibble; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	16M x 1	4216102	SC; 4K ref	60, 70, 80, 100	28/24	28/24	24	8c
	16M x 1	4217102	SC; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	4M x 4	4216400	FP; 4K ref	60, 70, 80, 100	28/24	28/24	24	8d
	4M x 4	4217400	FP; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	4M x 4	4216402	SC; 4K ref	60, 70, 80, 100	28/24	28/24	24	8e
	4M x 4	4217402	SC; 2K ref	60, 70, 80, 100	28/24	28/24	24	
	4M x 4	4216410	FP; 4K ref; WPB	60, 70, 80, 100	28/24	28/24	24	8f
	4M x 4	4217410	FP; 2K ref; WPB	60, 70, 80, 100	28/24	28/24	24	
	4M x 4	4216412	SC; 4K ref; WPB	60, 70, 80, 100	28/24	28/24	24	8g
	4M x 4	4217412	SC; 2K ref; WPB	60, 70, 80, 100	28/24	28/24	24	
	2M x 8	4216800	FP; 4K ref	50, 60, 70, 80	28	28		8h
	2M x 8	4216800L	FP; 4K ref; 3.3 V	60, 70, 80	28	28		
	2M x 8	42S16800	FP; 4K ref; SR	50, 60, 70, 80	28	28		
	2M x 8	42S16800L	FP; 4K ref; SR; 3.3 V	60, 70, 80	28	28		
	2M x 8	4217800	FP; 2K ref	50, 60, 70, 80	28	28		
	2M x 8	4217800L	FP; 2K ref; 3.3 V	60, 70, 80	28	28		
	2M x 8	42S17800	FP; 2K ref; SR	50, 60, 70, 80	28	28		
	2M x 8	42S17800L	FP; 2K ref; SR; 3.3 V	60, 70, 80	28	28		
	2M x 8	4216802	SC; 4K ref	50, 60, 70, 80	28	28		8i

FP Fast page
SR Self-refresh
SC Static column
WPB Write-per-bit
ref Refresh

DRAMs (cont)

Size	Organ-ization	μPD	Features	Row Access Time (ns)	Packages and Pins			Sect.
					SOJ	TSOP	ZIP	
16M (cont)	2M x 9	4216900	FP; 4K ref	50, 60, 70, 80	32	32		8j
	2M x 9	4216900L	FP; 4K ref; 3.3 V	60, 70, 80	32	32		
	2M x 9	42S16900	FP; 4K ref; SR	50, 60, 70, 80	32	32		
	2M x 9	42S16900L	FP; 4K ref; SR; 3.3 V	60, 70, 80	32	32		
	2M x 9	4217900	FP; 2K ref	50, 60, 70, 80	32	32		
	2M x 9	4217900L	FP; 2K ref; 3.3 V	60, 70, 80	32	32		
	2M x 9	42S17900	FP; 2K ref; SR	50, 60, 70, 80	32	32		
	2M x 9	42S17900L	FP; 2K ref; SR; 3.3 V	60, 70, 80	32	32		
	2M x 9	4216902	SC; 4K ref	50, 60, 70, 80	32	32		8k
	1M x 16	4216160	FP; 4K ref	50, 60, 70, 80	42	50/44		8l
	1M x 16	4216160L	FP; 4K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	42S16160	FP; 4K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 16	42S16160L	FP; 4K ref; SR; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	4217160	FP; 2K ref	50, 60, 70, 80	42	50/44		
	1M x 16	4217160L	FP; 2K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	42S17160	FP; 2K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 16	42S17160L	FP; 2K ref; SR; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	4218160	FP; 1K ref	50, 60, 70, 80	42	50/44		
	1M x 16	4218160L	FP; 1K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 16	42S18160	FP; 1K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 16	42S18160L	FP; 1K ref; SR; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	4216180	FP; 4K ref	50, 60, 70, 80	42	50/44		8m
	1M x 18	4216180L	FP; 4K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	42S16180	FP; 4K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 18	42S16180L	FP; 4K ref; SR; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	4217180	FP; 2K ref	50, 60, 70, 80	42	50/44		
	1M x 18	4217180L	FP; 2K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	42S17180	FP; 2K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 18	42S17180L	FP; 2K ref; SR; 3.3.V	60, 70, 80	42	50/44		
	1M x 18	4218180	FP; 1K ref	50, 60, 70, 80	42	50/44		
	1M x 18	4218180L	FP; 1K ref; 3.3 V	60, 70, 80	42	50/44		
	1M x 18	42S18180	FP; 1K ref; SR	50, 60, 70, 80	42	50/44		
	1M x 18	42S18180L	FP; 1K ref; SR: 3.3 V	60, 70, 80	42	50/44		

FP Fast page
SC Static column
ref Refresh

DRAM SIMM Modules

Organization	Pins	MC	Operation	Access Time (ns)	Module Size (inch)		DRAM Devices		Sect.
					Thickness	Height	Qty	μPD	
256K x 8	30	-42256AB8	Fast page	60, 70, 80, 100	.200	.661	2	424256LA	9a
256K x 9	30	-42256AB9	Fast page	60, 70, 80, 100	.200	.661	2 1	424256LA 42256L	9b
256K x 32	72	-42256A32	Fast page	70, 80, 100	.200	1.000	2	424260LE	9c
256K x 36	72	-42256A36	Fast page	70, 80, 100	.200	1.000	2	424280LE	9d
256K x 40	72	-42256AA40	Fast page	60, 70, 80, 100	.200	1.000	10	424256LA	9e
512K x 32	72	-42512A32	Fast page	70, 80, 100	.354	1.000	4	424260LE	9f
512K x 36	72	-42512A36	Fast page	70, 80, 100	.366	1.000	4	424280LE	9g
512K x 40	72	-42512AA40	Fast page	60, 70, 80, 100	.366	1.000	20	424256LA	9h
		-42512AB40	Fast page	70, 80, 100	.200	1.000	5	424800LE	
1M x 8	30	-421000A8	Fast page	60, 70, 80, 100	.200	.661	2	424400LA	10a
1M x 9	30	-421000A9	Fast page	60, 70, 80, 100	.200	.661	2 1	424400LA 421000LA	10b
1M x 32	72	-421000A32	Fast page	60, 70, 80, 100	.200	1.000	8	424400LA	10c
					.106	1.000	8	424400GS	
					.200	1.250	8	424400LA	
1M x 36	72	-421000A36	Fast page	60, 70, 80, 100	.200	1.000	8 4	424400LA 421000GX	10d
					.106	1.000	8 4	424400GS 421000GX	
					.208	1.250	8 4	424400LA 421000LA	
			Fast page	60, 70, 80	.366	1,000	8 4	424400LA 421000LA	
1M x 40	72	-421000AA40	Fast page	60, 70, 80, 100	.200	1.000	10	424400LA	10e
		-421000AB40	Fast page	60, 70, 80, 100	.354	.799	10	424800LE	
2M x 32	72	-422000A32	Fast page	60, 70, 80, 100	.354	1.000	16	424400LA	10f
					.161	1.000	16	424400GS	
					.354	1.250	16	424400LA	

DRAM SIMM Modules (cont)

Organization	Pins	MC	Operation	Access Time (ns)	Module Size (inch)		DRAM Devices		Sect.
					Thickness	Height	Qty	μPD	
2M x 36	72	-422000A36	Fast page	60, 70, 80	.366	1.000	16 8	424400LA 421000GX	10g
					.161	1.000	16 8	424400GS 421000GX	
					.366	1.250	16 8	424400LA 421000LA	
2M x 40	72	-422000AA40	Fast page	70, 80	.354	1.000	20	424400LA	10h
4M x 8	30	-424000A8	Fast page	60, 70, 80, 100	.208	.799	8	424100LA	11a
4M x 9	30	-424000A9	Fast page	60, 70, 80, 100	.200	.799	9	424100LA	11b
4M x 32	72	-424000A32	Fast page	60, 70, 80	.200	1.250	8	4217400LE	11c
					.366	1.000	8	4217400LE	
4M x 36	72	-424000A36	Fast page	60, 70, 80	.200	1.250	8 4	4217400LE 424100LA	11d
					.366	1.000	8 4	4217400LE 424100LA	
8M x 32	72	-428000A32	Fast page	60, 70, 80	.366	1.250	16	4217400LE	11e
8M x 36	72	-428000A36	Fast page	60, 70, 80	.366	1.250	16 8	4217400LE 424100LA	11f

Video RAMs

Size	Organ-ization	μPD	Row Access Time (ns)	Serial Access Time (ns)	Mode	Packages and Pins				Sect.
						DIP	SOJ	TSOP	ZIP	
256K	64K x 4	41264	120, 150	40, 60		24			24	12a
	64K x 4	42264	100	25		24	24		24	12b
1M	256K x 4	42273	100, 120	30, 40	FP		28		28	12c
	256K x 4	42274	100, 120	30, 40	FP		28		28	12d
	256K x 4	42274-80	80	25	FP		28		28	12e
	128K x 8	42275	80, 100, 120	25, 40	FP		40			12f
2M	256K x 8	482234	70, 80	17, 20	FP		40	44	40	12g
		482235	70, 80	17, 20	HP					

FP Fast page
HP Hyper page (extended data out)

Synchronous DRAM

Size	Organ-ization	μPD	Clock Rate (MHz)	Row Access Time (ns)	Burst Access Time (ns)	Packages and Pins				Sect.
						DIP	SOJ	TSOP	ZIP	
16M	4M x 4	42116420	66 100	70 50	15 10			44		13a
	2M x 8	42116820						44		
	2M x 9	42116920						44		
	1M x 16	42116162						50		
	1M x 18	42116182						50		

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RAMBUS DRAM

Size	Organ-ization	μPD	Read Hit Access Time (ns)	Burst Access Time (ns)	Packages and Pins				Sect.
					DIP	SOJ	TSOP	SVP	
16M	2M x 8	488130	40	2				32	14a
	2M x 9	488170	40	2				32	

Application Specific Devices

Description	μPD	Access Time (ns)	Packages and Pins					Sect.
			DIP	SOJ	TSOP	ZIP	Other	
910 x 8-bit line buffer for NTSC TV	42101	27, 49	24				24-SOP	18a
1134 x 8-bit line buffer for PAL TV	42102	18, 21, 40	24				24-SOP	18b
263 lines of 910 x 4 bits NTSC field buffer	42270	40	28					18c
Picture-in-picture generator	42271 42272	6 MHz input sampling					64-QFP	18d
256K x 8-bit field buffer	42280	25, 30, 40				28	28-SOP	18e
5048 x 8-bit line buffer for communications	42505	40, 55	24			28		18f
5048 x 8-bit line buffer	485505	18, 25				24	24-SOP	18g
5048 x 16 line buffer	485506	18, 25			44			18h
32K x 8 bidirectional data buffer	42532	50	40					18i
1M x 1 silicon file	42601	600		26/20		20		18j
4M x 1 silicon file	42641	80		26/20	26/20			18k
1M x 4 silicon file	42644	80		26/20	26/20			18l
256K x 16 graphics DRAM	481440	70, 80		40				18m

Fast Static RAMs

Size	Organization	μPD	Access Time (ns)	Packages and Pins						Sect
				DIP	SOJ	SOP	TSOP	ZIP	Other	
64K	64K x 1	4361B	12, 15, 20	22	24					19a
	16K x 4	4362B	12, 15, 20	22	24					19b
	16K x 4	4363B	12, 15, 20	24	24					19c
	8K x 8	4368	15, 20	28	28					19d
	8K x 9	4369	15, 20	28	28					19e
256K	256K x 1	43251B	15, 20, 25	24	24					20a
	64K x 4	43253B	15, 20, 25	28	28					20b
	64K x 4	43254B	15, 20, 25	24	24					20c
	32K x 8	43258A	15, 20, 25	28	28					20d
	32K x 9	43259A	15, 20, 25	32	32					20e
1M	1M x 1	431001	20, 25, 35		28					21a
	256K x 4	431004	20, 25, 35		28					21b
	128K x 8	431008	15, 17, 20		32					21c
	128K x 9	431009	15, 17, 20		36					21d
	64K x 16	431016	15, 17, 20		44		44			21e
	64K x 18	431018	15, 17, 20		44		44			21f
4M	4M x 1	434001	20, 25		32					22a
	1M x 4	434004	20, 25		32					22b
	512K x 8	434008	20, 25		36					22c

Cache Data RAMs

Size	Organization	μPD	Access Time (ns)	Packages and Pins					Sect.
				DIP	SOJ	SOP	TSOP	PLCC	
256K	16K x 10 bit x 2	46710A	12, 15					52	23a
	8K x 20 bit x 2	46741A	12, 15					68	23b

Standard Static RAMs

Size	Organization	μPD	Access Time (ns)	Packages and Pins					Sect.
				DIP	SOJ	SOP	TSOP	ZIP	
256K	32K x 8	43256A	85, 100, 120, 150	28		28	32		24a
	32K x 8	43256B	55, 70, 85	28		28			24b
1M	128K x 8	431000A	70, 85, 100	32		32	32		24c
4M	512K x 8	434000	55, 70, 85, 100	32		32	32		24d
	512K x 8	MC-434000	85, 100	32					24e

ECL RAMs (10K Interface)

Size	Organization	μPB	Access Time (ns)	Packages and Pins			Sect.
				DIP	LCC	Flatpack	
1K	256 x 4	10422	7, 10	24			25a
4K	4K x 1	10470	10, 15	18			25b
	1K x 4	10474	8, 10, 15	24			25c
	1K x 4	10474A	5, 6	24			25d
	1K x 4	10474E	3, 4	24		24	25e
	1K x 4	10476LL	6	28		28	25f
16K	16K x 1	10480	10, 15	20		20	25g
	4K x 4	10484	10, 15	28		28	25h
	4K x 4	10484A	5, 7	28		28	25i
	4K x 4	10A484	5, 7	28		28	25j
256K	256K x 1	μPD10500	15, 20	24			25k

ECL RAMs (100K Interface)

Size	Organization	μPB	Access Time (ns)	Packages and Pins			Sect.
				DIP	LCC	Flatpack	
1K	256 x 4	100422	7, 10	24		24	26a
4K	4K x 1	100470	10, 15	18			26b
	1K x 4	100474	4.5, 6, 8, 10, 15	24	24	24	26c
	1K x 4	100474A	5, 6	24		24	26d
	1K x 4	100474E	3, 4	24		24	26e
	1K x 4	100476LL	6	28		28	26f
16K	16K x 1	100480	10, 15	20		20	26g
	4K x 4	100484	10, 15	28		28	26h
	4K x 4	100484A	5, 7	28		28	26i
	4K x 4	100A484	5, 7	28		28	26j
256K	256K x 1	μPD100500	15, 20	24			26k

EEPROMs

Size	Organization	μPD	Access Time (ns)	Packages and Pins						Sect.
				DIP	SOJ	SOP	TSOP	ZIP	Other	
4K	512 x 8	28C04	200, 250	24		24				27a
	512 x 8	28C05	200, 250	24		24				27b
64K	8K x 8	28C64	200, 250	28						27c
256K	32K x 8	28C256	200, 250	28						27d

NEC

Section 18
Application Specific Devices (See App Notes 54 thru 58, 90-03, 90-06.)

μPD	Description	
42101	910 x 8-bit line buffer for NTSC TV	18a
42102	1134 x 8-bit line buffer for PAL TV	18b
42270	263 lines of 910 x 4 bits NTSC field buffer	18c
42271	Picture-in-picture generator	18d
42272	Picture-in-picture generator with color border	
42280	256K x 8-bit field buffer	18e
42505	5048 x 8-bit line buffer for communications systems	18f
485505	5048 x 8-bit line buffer	18g
485506	5048 x 16 line buffer	18h
42532	32K x 8 bidirectional data buffer	18i
42601	1M x 1 silicon file	18j
42641	4M x 1 silicon file	18k
42644	1M x 4 silicon file	18l
481440	256K x 16 graphics DRAM; hyper-page	18m

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Description

The μPD42101 is a 910-word by 8-bit line buffer fabricated with a CMOS silicon-gate process. The device helps to create an NTSC flicker-free television picture (noninterlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD42101 can also be used as a digital delay line. The delay length is variable from 10 bits (at maximum clock speed) to 910 bits.

Features

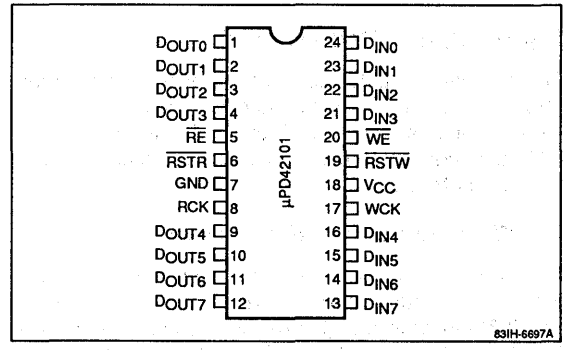
- 910-word x 8-bit organization
- Line buffer for NTSC, $4f_{SC}$ digital television systems
- Asynchronous, simultaneous read/write operation
- 1H (910-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- 24-pin plastic DIP and miniflat packaging

Ordering Information

Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD42101C-3	34 ns	34 ns	24-pin plastic DIP
C-2	34 ns	69 ns	
C-1	69 ns	69 ns	
μPD42101G-3	34 ns	34 ns	24-pin plastic miniflat
G-2	34 ns	69 ns	
G-1	69 ns	69 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
$\overline{RSTW}$	Write address reset input
$\overline{RSTR}$	Read address reset input
$\overline{WE}$	Write enable input
$\overline{RE}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

PIN FUNCTIONS

D_{IN0} - D_{IN7} (Data Inputs)

In a digital television application, the digital composite signal, luminance, chrominance, etc. information is written into these inputs.

D_{OUT0} - D_{OUT7} (Data Outputs)

The tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ (Write Address Reset Input)

Bringing this signal low when $\overline{WE}$ is also low resets the internal write address to 0. If $\overline{WE}$ is at a high level when the $\overline{RSTW}$ input is brought low, the internal write address is set to 909. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ (Read Address Reset Input)

This signal is strobed by the rising edge of RCK and resets the internal read address to 0 if $\overline{RE}$ is also low. If $\overline{RE}$ is at a high level when the $\overline{RSTR}$ input is brought low, the internal read address is set to 909.

$\overline{WE}$ (Write Enable Input)

This input controls write operation. If $\overline{WE}$ is low, all write cycles proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ (Read Enable Input)

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the data outpus become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK (Write Clock Input)

All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 909 to 0 and begin increasing again.

RCK (Read Clock Input)

All read cycles are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 909 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltages on any input pin, V_I	−1.5 to + 7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

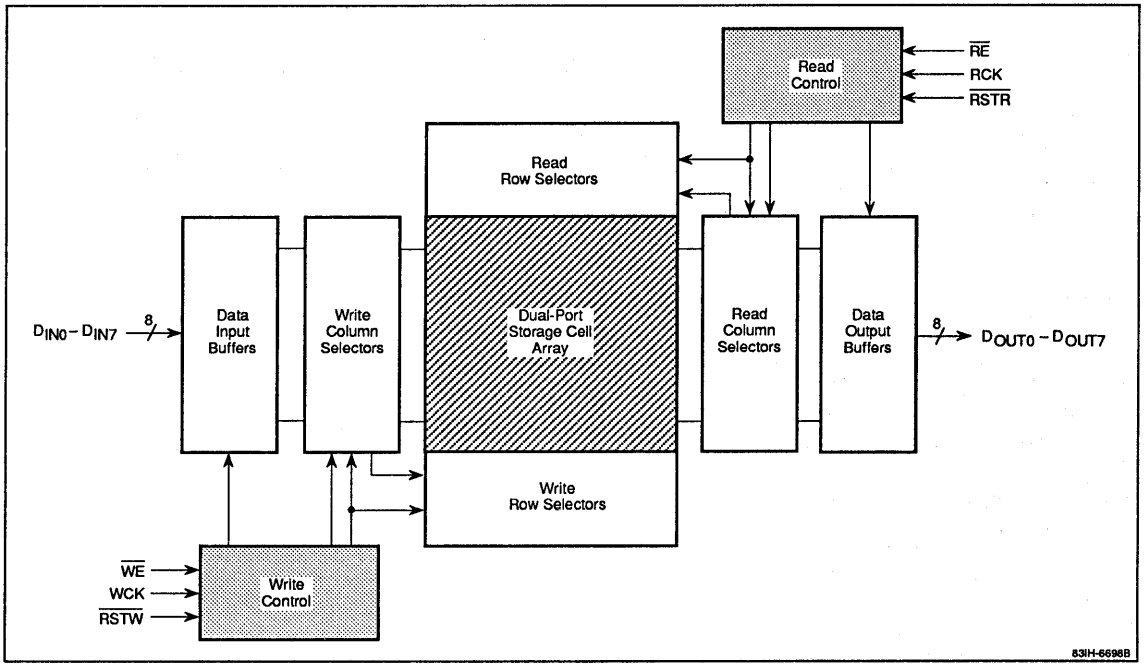
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Pins Under Test
Input capacitance	C_I		5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O		7	pF	D_{OUT0} - D_{OUT7}

Block Diagram



DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_I	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD42101-3		μPD42101-2		μPD42101-1			
Parameter	Symbol	min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}		70		60		35	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)
Write clock cycle time	t_{WCK}	34	1090	69	1090	69	1090	ns	
WCK pulse width	t_{WCW}	14		25		25		ns	
WCK precharge time	t_{WCP}	14		25		25		ns	
Read clock cycle time	t_{RCK}	34	1090	34	1090	69	1090	ns	
RCK pulse width	t_{RCW}	14		14		25		ns	
RCK precharge time	t_{RCP}	14		14		25		ns	
Access time	t_{AC}		27		27		49	ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42101-3 min	μPD42101-3 Max	μPD42101-2 Min	μPD42101-2 Max	μPD42101-1 Min	μPD42101-1 Max	Unit	Test Conditions
Output hold time	t_{OH}	5		5		5		ns	
Output active time	t_{LZ}	5	27	5	27	5	49	ns	(Note 5)
Output disable time	t_{HZ}	5	27	5	27	5	49	ns	(Note 5)
Data-in setup time	t_{DS}	14		18		18		ns	
Data-in hold time	t_{DH}	5		5		5		ns	
Reset active setup time	t_{RS}	14		14		20		ns	(Note 7)
Reset active hold time	t_{RH}	5		5		5		ns	(Note 7)
Reset inactive hold time	t_{RN1}	5		5		5		ns	(Note 8)
Reset inactive setup time	t_{RN2}	14		14		20		ns	(Note 8)
Write enable setup time	t_{WES}	14		20		20		ns	(Note 9)
Write enable hold time	t_{WEH}	5		5		5		ns	(Note 9)
Write enable high delay from WCK	t_{WEN1}	5		5		5		ns	(Note 10)
Write enable low delay to WCK	t_{WEN2}	14		20		20		ns	(Note 10)
Read enable setup time	t_{RES}	14		14		20		ns	(Note 9)
Read enable hold time	t_{REH}	5		5		5		ns	(Note 9)
Read enable high delay from RCK	t_{REN1}	5		5		5		ns	(Note 10)
Read enable low delay to RCK	t_{REN2}	14		14		20		ns	(Note 10)
Write disable pulse width	t_{WEW}	0		0		0		ns	(Note 6)
Read disable pulse width	t_{REW}	0		0		0		ns	(Note 6)
Write reset time	t_{RSTW}	0		0		0		ns	(Note 6)
Read reset time	t_{RSTR}	0		0		0		ns	(Note 6)
Transition time	t_T	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) After power-up, a read reset cycle and a write reset cycle must be executed before proper device operation is achieved.

(3) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V. See figure 1.

(4) Input timing reference levels = 1.5 V. Output timing reference levels are 0.8 and 2.0 V. See figure 2.

(5) This delay is measured at 200 mV from the steady-state voltage with the load specified in figure 4. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1-line cycle operation:
$t_{WEW} + t_{RSTW} + 910\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 910\ (t_{RCK}) \leq 1$ ms

(7) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(8) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(9) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(10) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(11) Data is guaranteed to remain valid for a minimum of 1 ms after it is written. After this time, the data stored may be discharged, since this device uses a dynamic storage element.

Figure 1. Input Timing

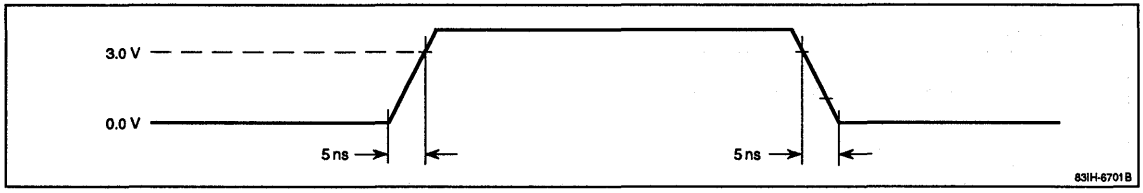


Figure 2. Output Timing

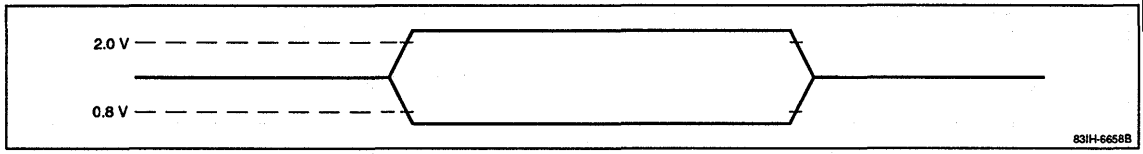


Figure 3. Output Load for t_{AC} and t_{OH}

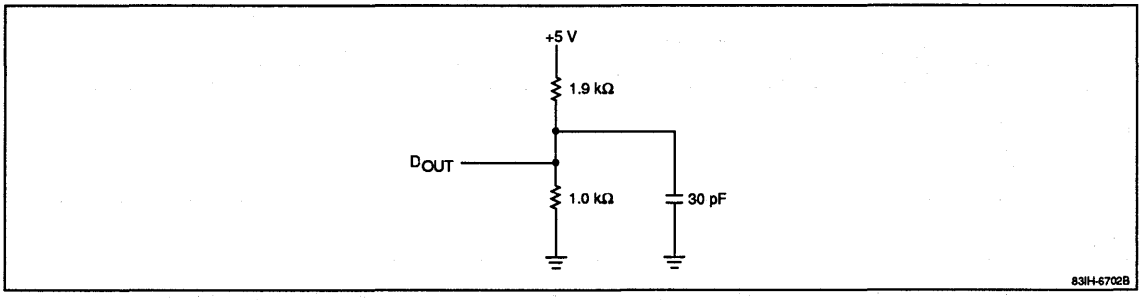
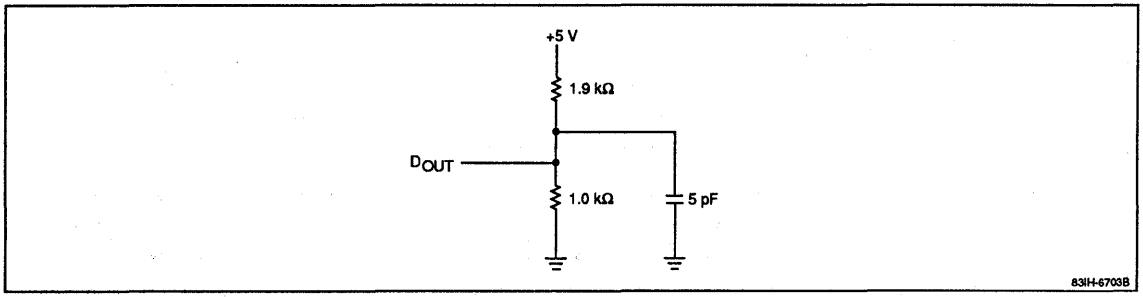
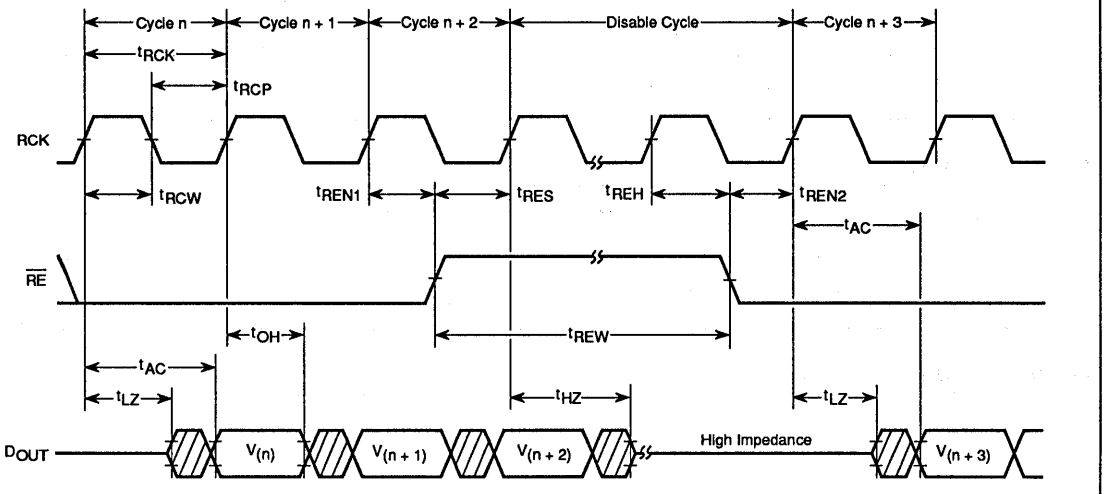


Figure 4. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

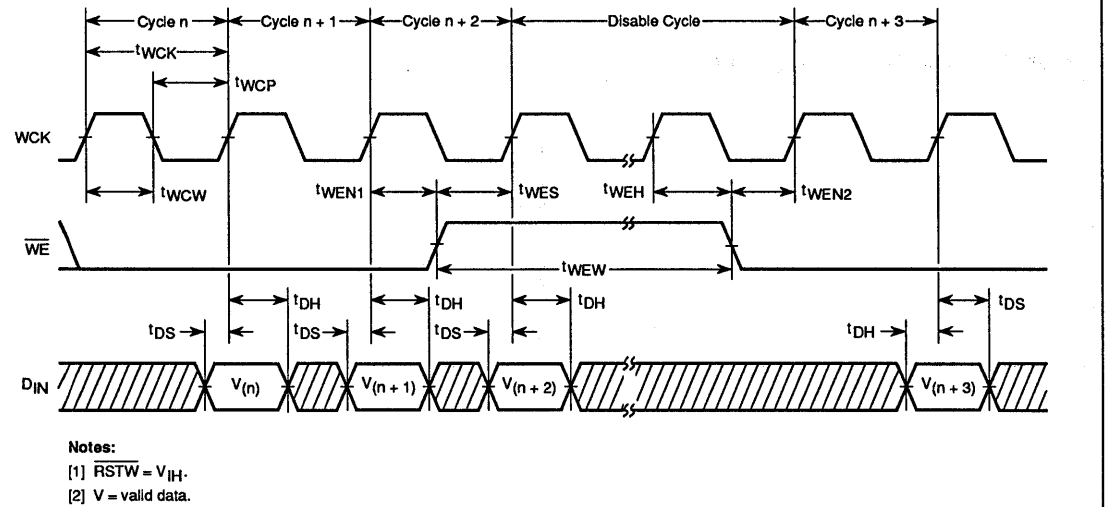
Read Cycle



Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.

83IH-6705B

Write Cycle

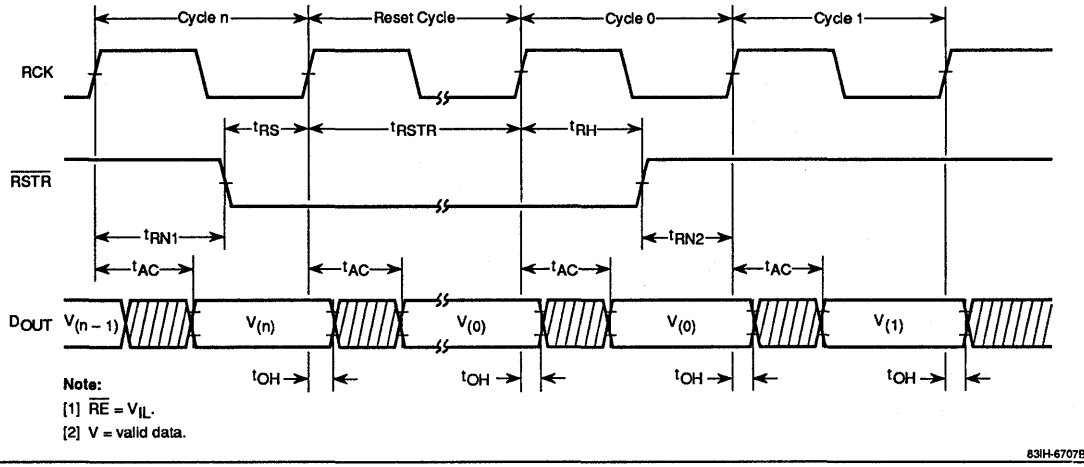


Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

83IH-6704B

Timing Waveforms (cont)

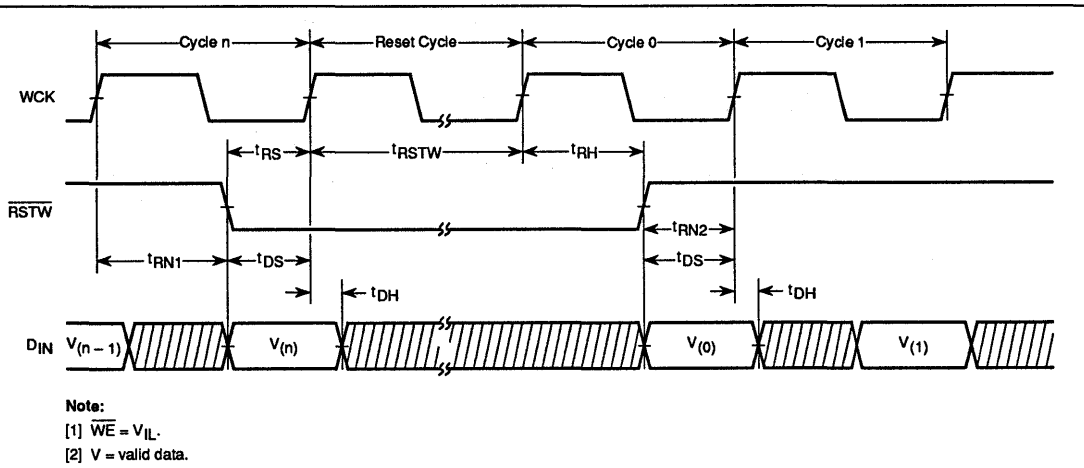
Read Reset Cycle



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

83IH-6707B

Write Reset Cycle



Note:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

83IH-6706B

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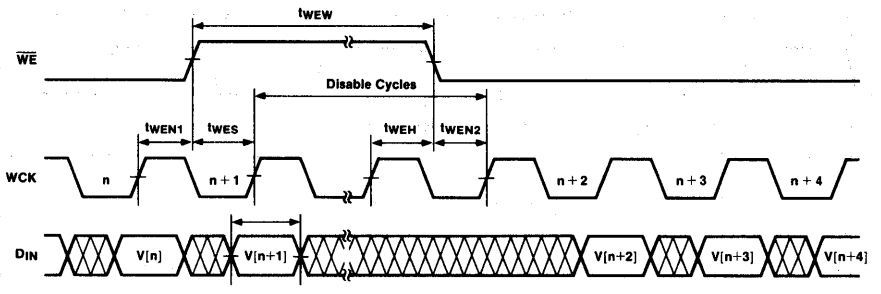
Timing Waveforms (cont)

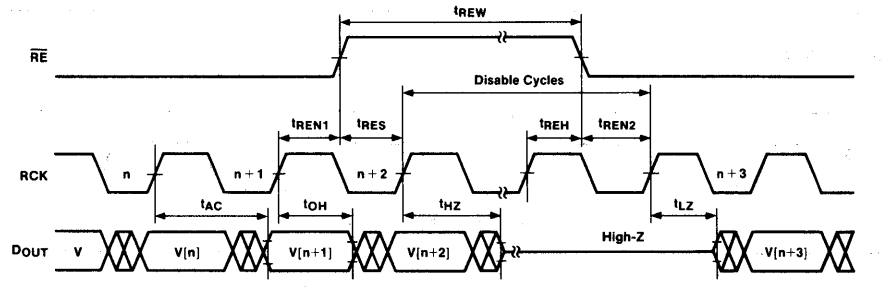
Write Disable Cycle



Note:
[1] V = Valid Data.

83-003723B

Read Disable Cycle

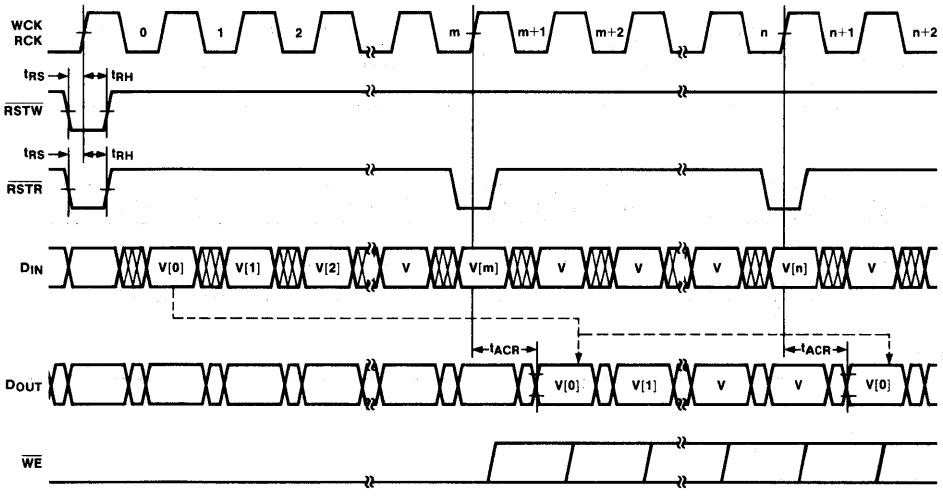


Note:
[1] V = Valid Data.

83-003646B

Timing Waveforms (cont)

Re-Read Cycle



Note:

[1] $\overline{RE} = V_{IL}$.

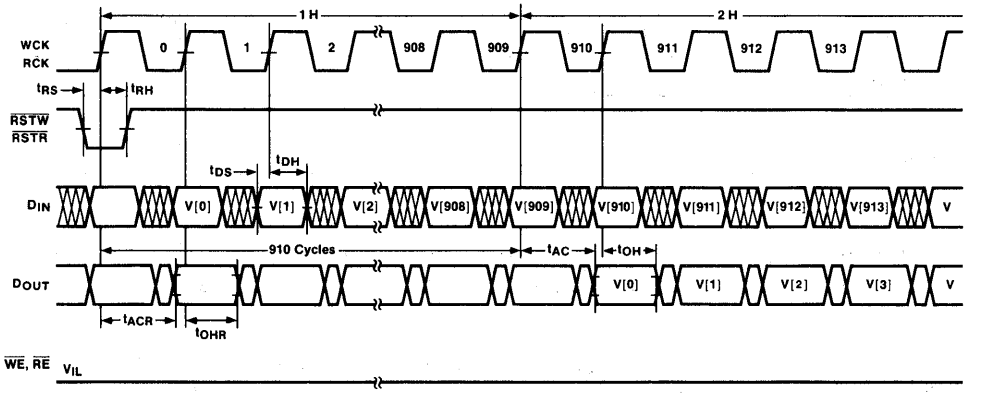
[2] V = Valid Data.

[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

Timing Waveforms (cont)

910-Bit Delay Line Cycle



Note:

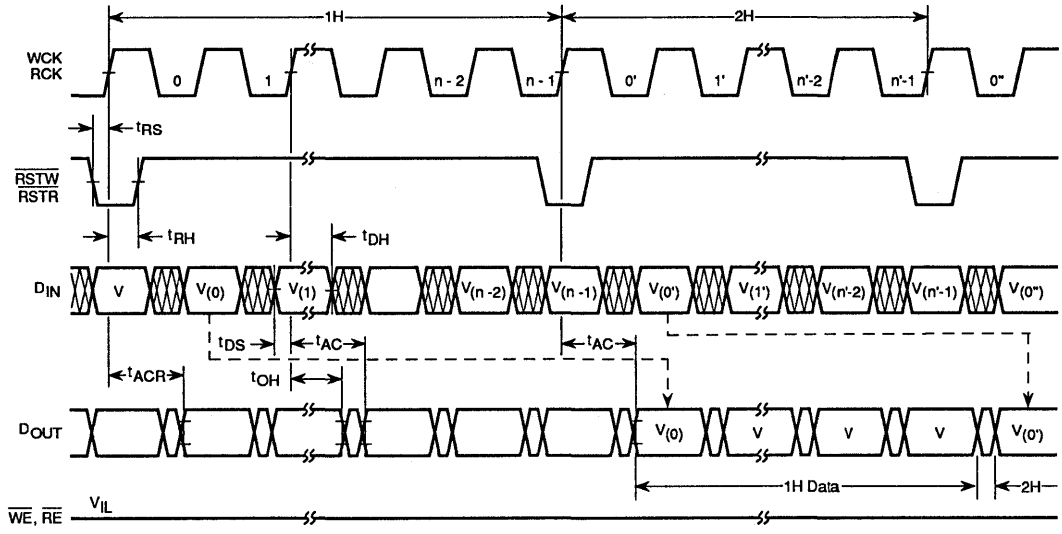
[1] V = Valid Data.

[2] 1H = the first group of 910 bits. 2H = the second group of 910 bits.

83-003657B

Timing Waveforms (cont)

n-Bit Delay Line Cycle



Notes:

[1] V = valid data

[2] 1H = the first group of bits. 2H = the second group of n' bits.

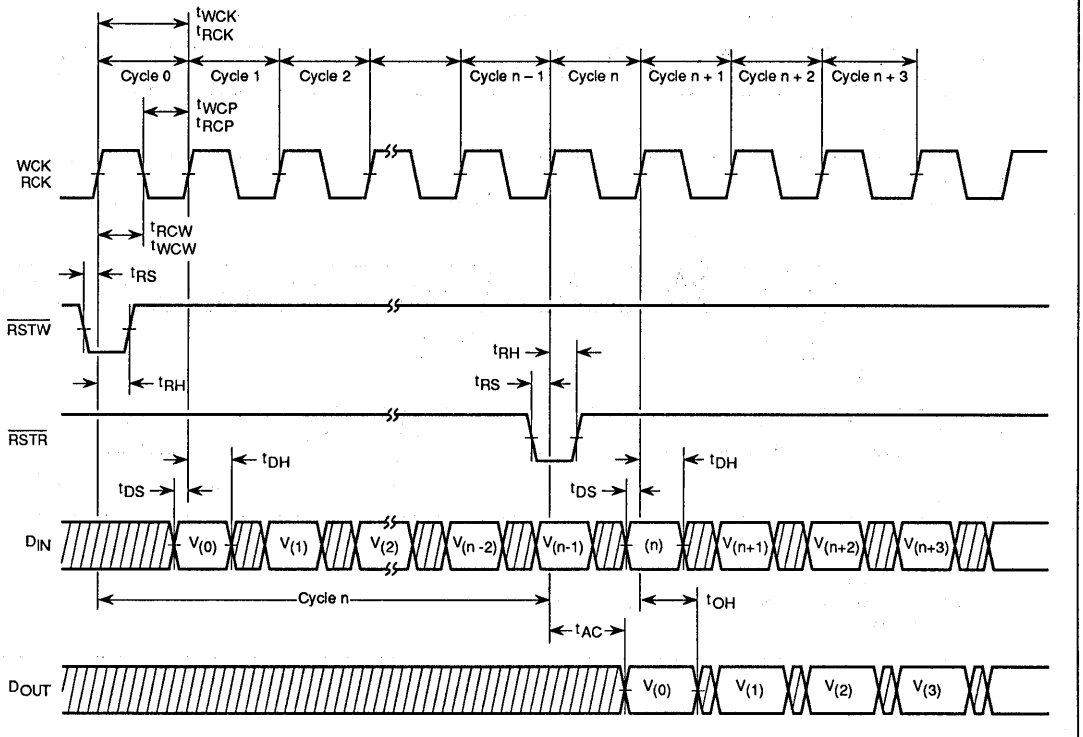
[3] $\overline{RE} = \overline{WE} = V_{IL}$.

83IH-6717B

18a

Timing Waveforms (cont)

n-Bit Delay Line Timing Cycle (1)



Notes:

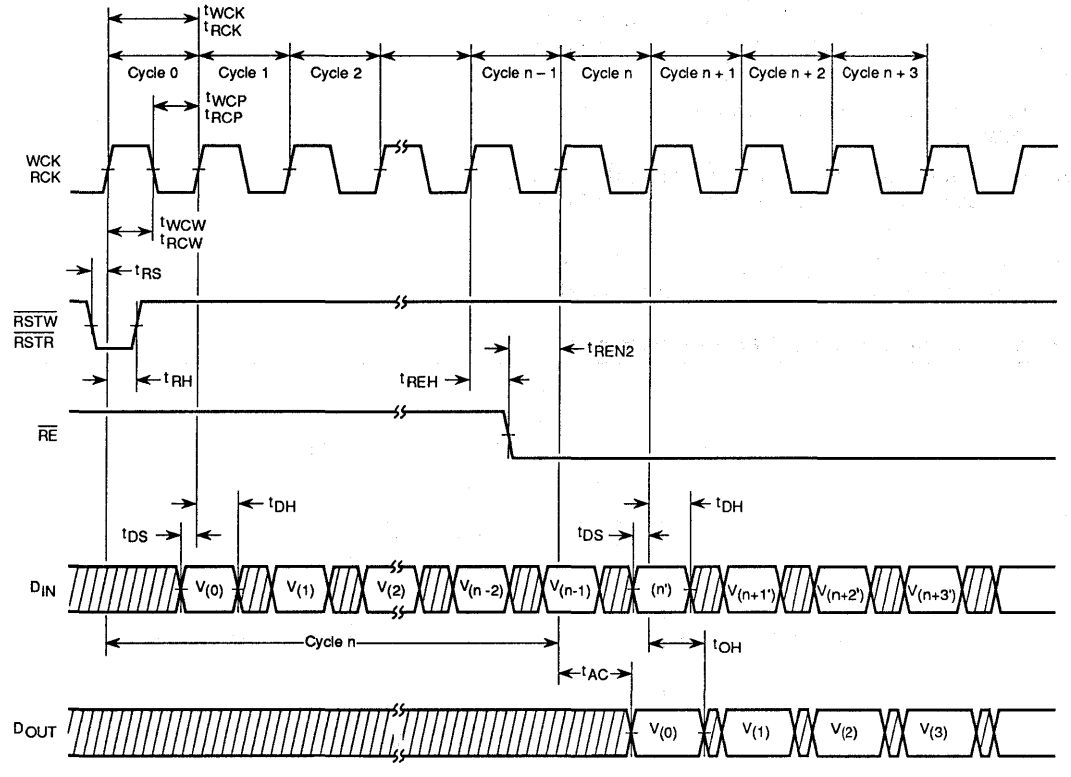
[1] $\overline{RE}$ and $\overline{WE}$ =V_{IL}.

[2] V = valid data.

83IH-6709B

Timing Waveforms (cont)

n-Bit Delay Line Timing Cycle (2)



Notes:

[1] $\overline{WE} = V_{IL}$.

[2] V = valid data.

83IH-6710B

18a

Applications

1H (910-bit) Delay Line

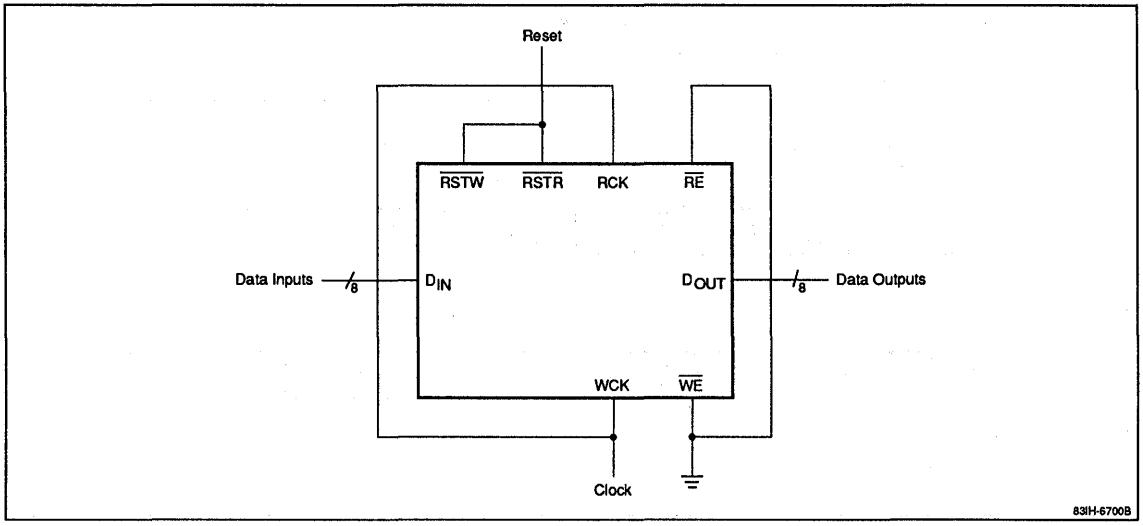
Any one of the following methods may be used to configure a 1H (910-bit) delay line, or to vary the number of delay bits from a minimum of 5 (when operating at $4f_{SC}$) to a maximum of 910 (figure 5).

(1) Execute a reset cycle proportionate to the desired delay length.

(2) Adjust the input timing of $\overline{RSTW}$ and $\overline{RSTR}$ to the desired delay length (see waveform for n-bit Delay Line Timing 1).

(3) Adjust the address by disabling $\overline{WE}$ or $\overline{RE}$ for a period proportionate to the desired delay length.

Figure 5. Connection of a 1H (910-bit) Delay Line

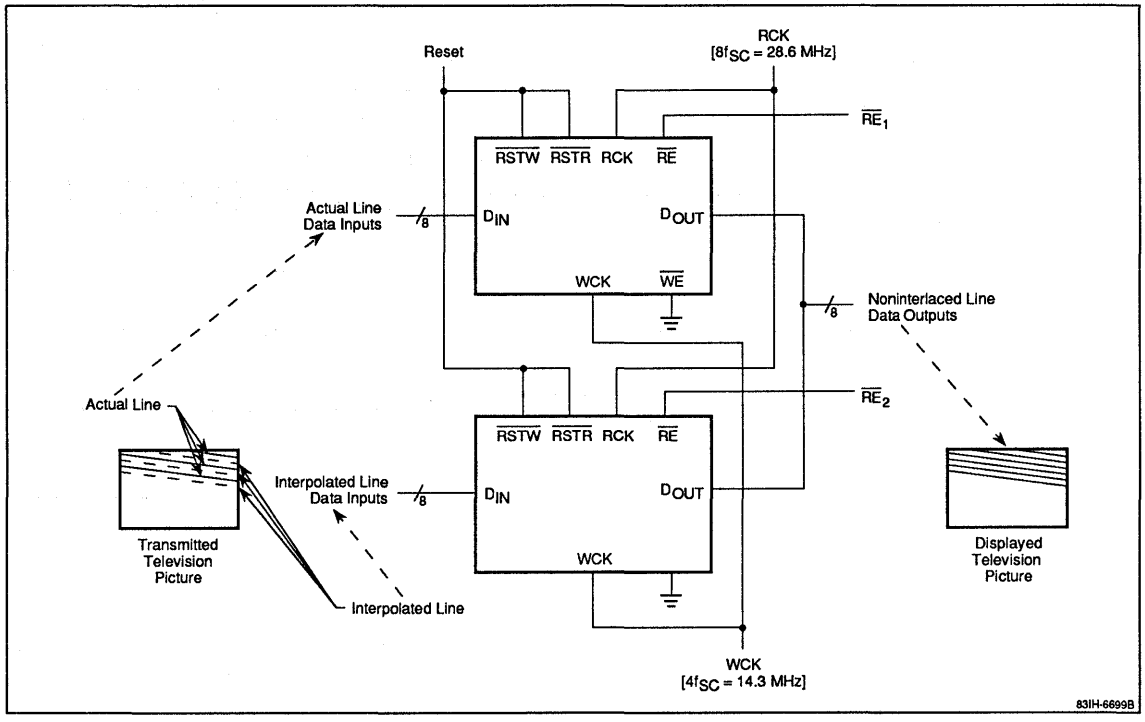


Applications (cont)

Noninterlaced Scan Conversion

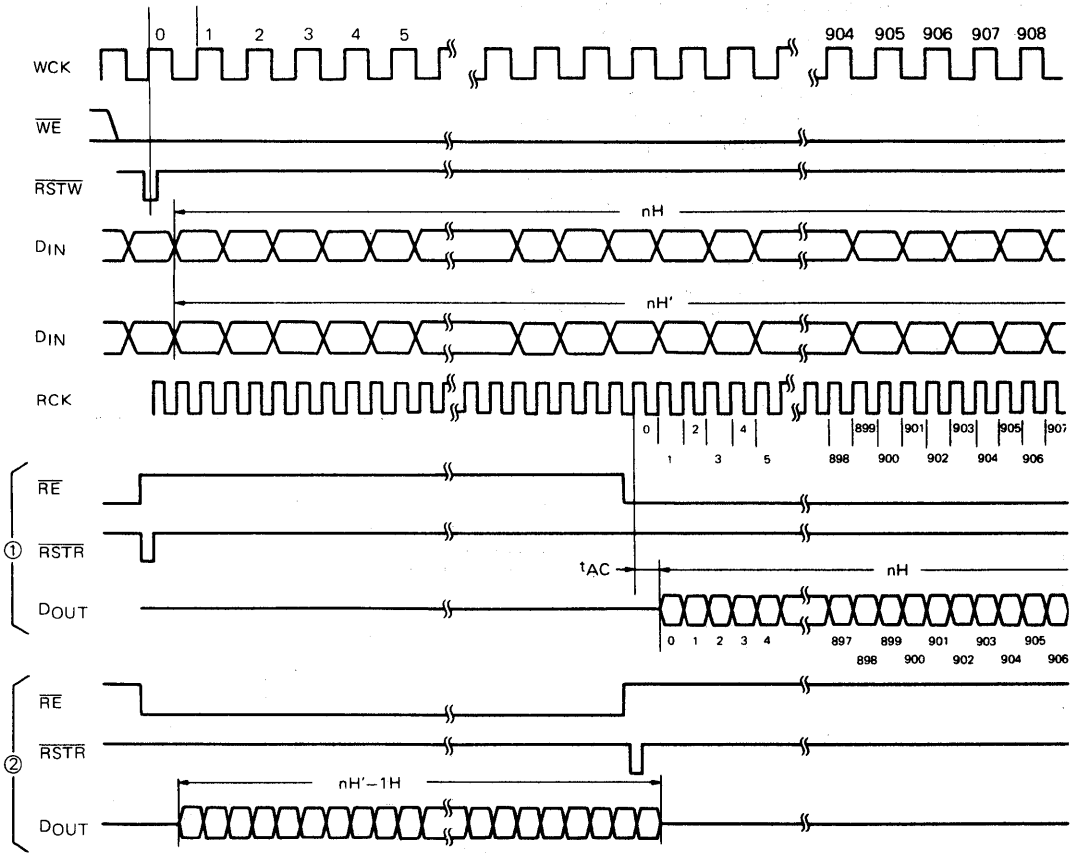
It is also possible to use either one or two μPD42101s for noninterlaced scan conversion. If one device is used, the same data is read twice at 28.6 MHz ($8f_{SC}$) to prepare it for writing at 14.3 MHz ($4f_{SC}$). If two devices are used as shown in figure 6, data input at 14.3 MHz is read alternately at 28.6 MHz with $\overline{RE}$. Actual line signals and complement line signals are entered as input data. Complement signals can also be obtained using the μPD42101 if resetting is performed for each line. A single signal type is assumed in this case. In actual applications, noninterlaced scan conversion with brightness (Y) and color difference (C) and RGB signals will require as many as two or three times the number of μPD42101 devices shown in this example.

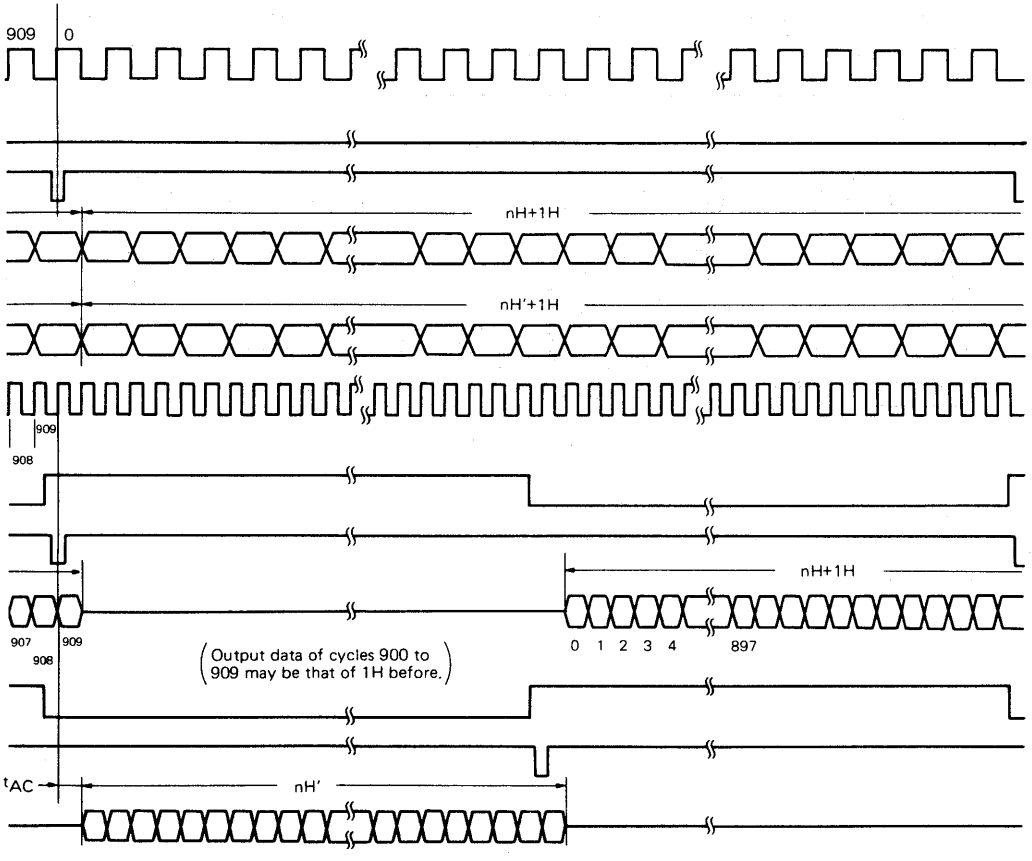
Figure 6. Example of Noninterlaced Scan Conversion



Timing Waveforms (cont)

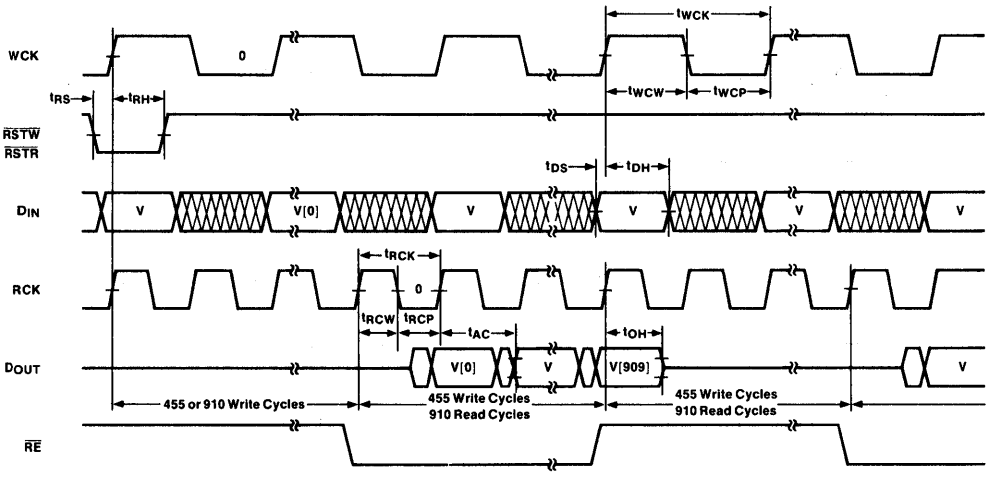
Application Timing for Noninterlaced Scan Conversion




909
0
nH+1H
nH'+1H
909
908
907
909
908
nH+1H
0 1 2 3 4
897
(Output data of cycles 900 to 909 may be that of 1H before.)
tAC
nH'
83-005018B

Timing Waveforms (cont)

Basic Timing for Noninterlaced Scan Conversion



Note:

[1] $\overline{WE} = V_{IL}$.

[2] V = Valid Data.

[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

83-003655B

μPD42102
Line Buffer for PAL TV

Description

The μPD42102 is a 1,135-word by 8-bit line buffer fabricated with a CMOS silicon-gate process. The device helps to create a PAL flicker-free television picture (non-interlaced scan conversion) by providing intermediate storage and very high-speed read and write operation.

The μPD42102 can also be used as a digital delay line. The delay length is variable from 2 bits (at maximum clock speed) to 1,135 bits.

Features

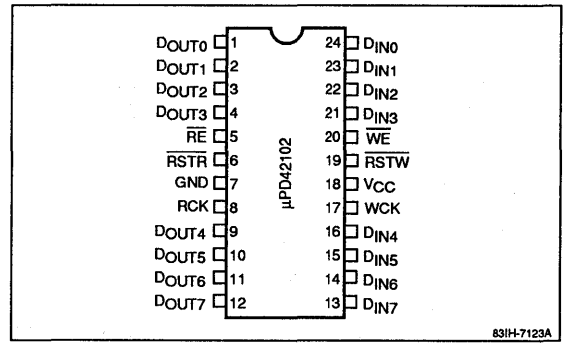
- 1,135-word x 8-bit organization
- Line buffer for PAL, $4f_{SC}$ digital television systems
- Asynchronous, simultaneous read/write operation
- 1H (1,135-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- 24-pin plastic DIP and miniflat packaging

Ordering Information

Part Number	Read Cycle Time (min)	Write Cycle Time (min)	Package
μPD42102C-5	25 ns	25 ns	24-pin plastic DIP
C-3	34 ns	34 ns	
C-2	34 ns	69 ns	
C-1	69 ns	69 ns	
μPD42102G-5	25 ns	25 ns	24-pin plastic miniflat
G-3	34 ns	34 ns	
G-2	34 ns	69 ns	
G-1	69 ns	69 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
$\overline{RSTW}$	Write address reset input
$\overline{RSTR}$	Read address reset input
$\overline{WE}$	Write enable input
$\overline{RE}$	Read enable input
WCK	Write clock input
RCK	Read clock input
GND	Ground
V_{CC}	+5-volt power supply

PIN FUNCTIONS

D_{IN0} - D_{IN7} (Data Inputs)

In a digital television application, the digital composite signal, luminance, chrominance, etc. information is written into these inputs.

D_{OUT0} - D_{OUT7} (Data Outputs)

The tri-state outputs are used to access the stored information. In a simple digital delay line application, a delay of one-half write clock cycle plus a maximum of 300 ns is required to move data from the data inputs to the data outputs.

$\overline{RSTW}$ (Write Address Reset Input)

Bringing this signal low when $\overline{WE}$ is also low resets the internal write address to 0. If $\overline{WE}$ is at a high level when the $\overline{RSTW}$ input is brought low, the internal write address is set to 1,134. The state of this input is strobed by the rising edge of WCK.

$\overline{RSTR}$ (Read Address Reset Input)

This signal is strobed by the rising edge of RCK and resets the internal read address to 0 if $\overline{RE}$ is also low. If $\overline{RE}$ is at a high level when the $\overline{RSTR}$ input is brought low, the internal read address is set to 1,134.

$\overline{WE}$ (Write Enable Input)

This input controls write operation. If $\overline{WE}$ is low, all write cycles proceed. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{RE}$ (Read Enable Input)

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the data outpus become high impedance and the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

WCK (Write Clock Input)

All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 1,134 to 0 and begin increasing again.

RCK (Read Clock Input)

All read cycles are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 1,134 to 0 and begin increasing again.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltages on any input pin, V_I	−1.5 to + 7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

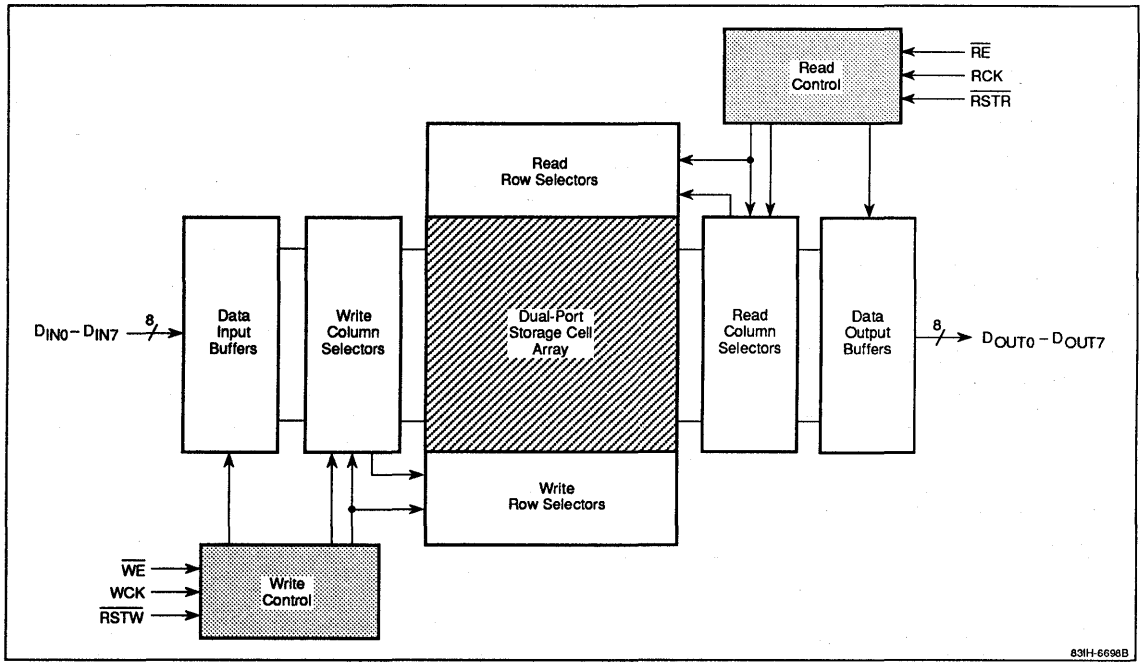
Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Operating temperature	T_A	−20		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Min	Max	Unit	Pins Under Test
Input capacitance	C_I		5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O		7	pF	D_{OUT0} - D_{OUT7}

Block Diagram



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DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_I	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD42102-5		μPD42102-3		μPD42102-2		μPD42102-1			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}		80		80		70		40	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)
Write clock cycle time	t_{WCK}	25	880	28	880	56	880	56	880	ns	
WCK pulse width	t_{WCW}	10		12		20		20		ns	
WCK precharge time	t_{WCP}	10		12		20		20		ns	
Read clock cycle time	t_{RCK}	25	880	28	880	28	880	56	880	ns	
RCK pulse width	t_{RCW}	10		12		12		20		ns	
RCK precharge time	t_{RCP}	10		12		12		20		ns	
Access time	t_{AC}		18		21		21		40	ns	
Output hold time	t_{OH}	5		5		5		5		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD42102-5 Min	μPD42102-5 Max	μPD42102-3 Min	μPD42102-3 Max	μPD42102-2 Min	μPD42102-2 Max	μPD42102-1 Min	μPD42102-1 Max	Unit	Test Conditions
Access time after a reset cycle	t_{ACR}		18		21		21		40	ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		5		ns	
Output active time	t_{LZ}	5	18	5	21	5	21	5	40	ns	(Note 4)
Output disable time	t_{HZ}	5	18	5	21	5	21	5	40	ns	(Note 4)
Data-in setup time	t_{DS}	7		12		15		15		ns	
Data-in hold time	t_{DH}	3		5		5		5		ns	
Reset active setup time	t_{RS}	7		12		12		20		ns	(Note 7)
Reset active hold time	t_{RH}	3		5		5		5		ns	(Note 7)
Reset inactive hold time	t_{RN1}	3		5		5		5		ns	(Note 8)
Reset inactive setup time	t_{RN2}	7		12		12		20		ns	(Note 8)
Write enable setup time	t_{WES}	7		12		20		20		ns	(Note 9)
Write enable hold time	t_{WEH}	3		5		5		5		ns	(Note 9)
Write enable high delay from WCK	t_{WEN1}	3		5		5		5		ns	(Note 10)
Write enable low delay to WCK	t_{WEN2}	7		12		20		20		ns	(Note 10)
Read enable setup time	t_{RES}	7		12		12		20		ns	(Note 9)
Read enable hold time	t_{REH}	3		5		5		5		ns	(Note 9)
Read enable high delay from RCK	t_{REN1}	3		5		5		5		ns	(Note 10)
Read enable low delay to RCK	t_{REN2}	7		12		12		20		ns	(Note 10)
Write disable pulse width	t_{WEW}	0		0		0		0		ns	(Note 5)
Read disable pulse width	t_{REW}	0		0		0		0		ns	(Note 5)
Write reset time	t_{RSTW}	0		0		0		0		ns	(Note 5)
Read reset time	t_{RSTR}	0		0		0		0		ns	(Note 5)
Transition time	t_T	3	35	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.
For the -5 version only, t_T = 3 ns; input pulse levels = 0.4 to 2.4 V; transition times are measured between 0.4 and 2.4 V. See figures 1 and 2.

(3) Input timing reference levels = 1.5 V. Output timing reference levels are 0.8 and 2.0 V. See figure 3.

(4) This delay is measured at 200 mV from the steady-state voltage with the load specified in figure 5. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) t_{WEW} (max) and t_{REW} (max) must be satisfied by the following equations in 1-line cycle operation:
$t_{WEW} + t_{RSTW} + 1{,}135\ (t_{WCK}) \leq 1$ ms
$t_{REW} + t_{RSTR} + 1{,}135\ (t_{RCK}) \leq 1$ ms

(6) This parameter applies when $t_{RCK} \geq t_{ACR}$ (max).

(7) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(8) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(9) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(10) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(11) Data is guaranteed to remain valid for a minimum of 1 ms after it is written. After this time, the data stored may be invalid, since this device uses a dynamic storage element.

Figure 1. Input Timing

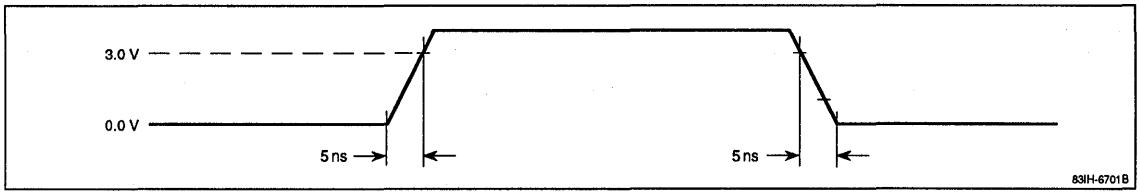

Figure 2. Input Timing for μPD42102-5

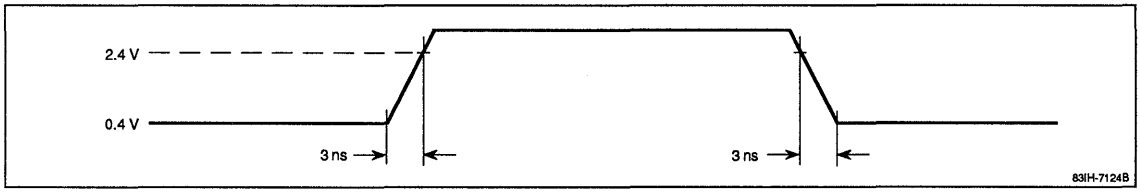

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Figure 3. Output Timing

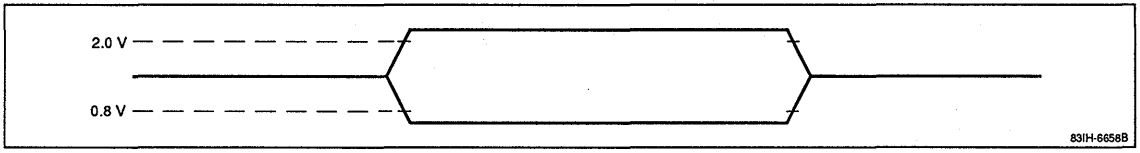


Figure 4. Output Load for t_{AC}, t_{ACR}, t_{OH} and t_{OHR}

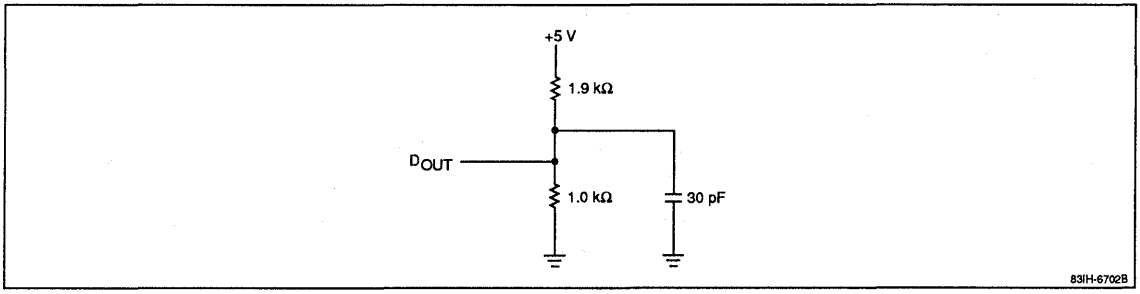
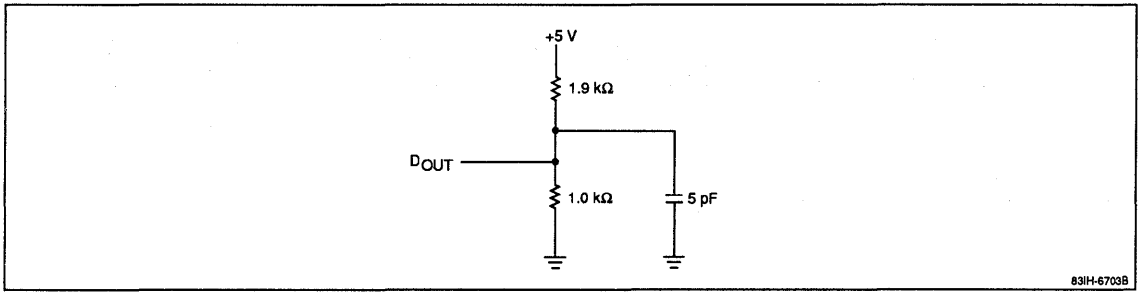
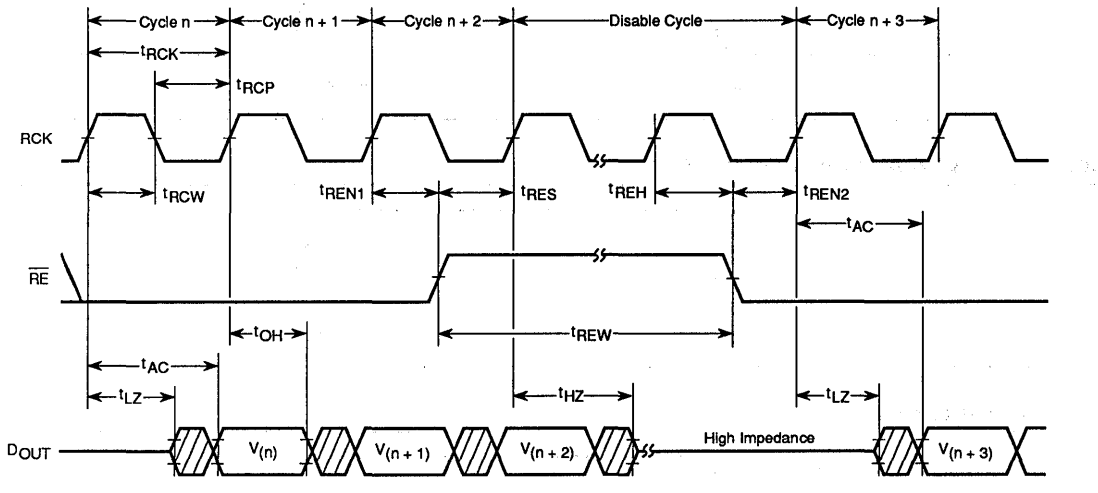


Figure 5. Output Load for t_{LZ} and t_{HZ}



Timing Waveforms

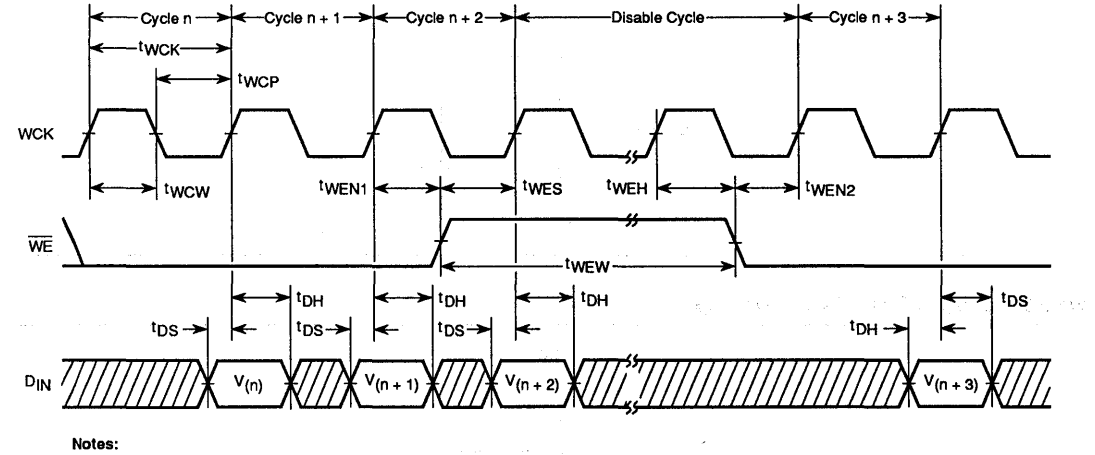
Read Cycle



Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.

83IH-6705B

Write Cycle

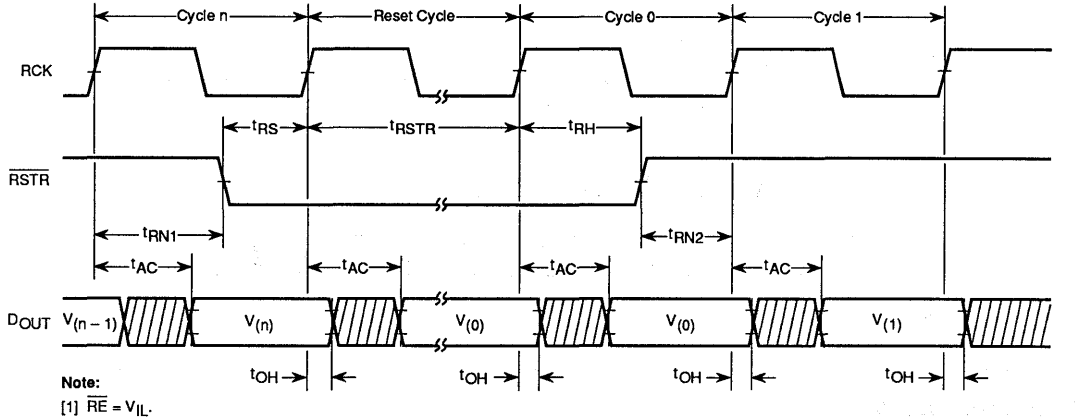


Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

83IH-6704B

Timing Waveforms (cont)

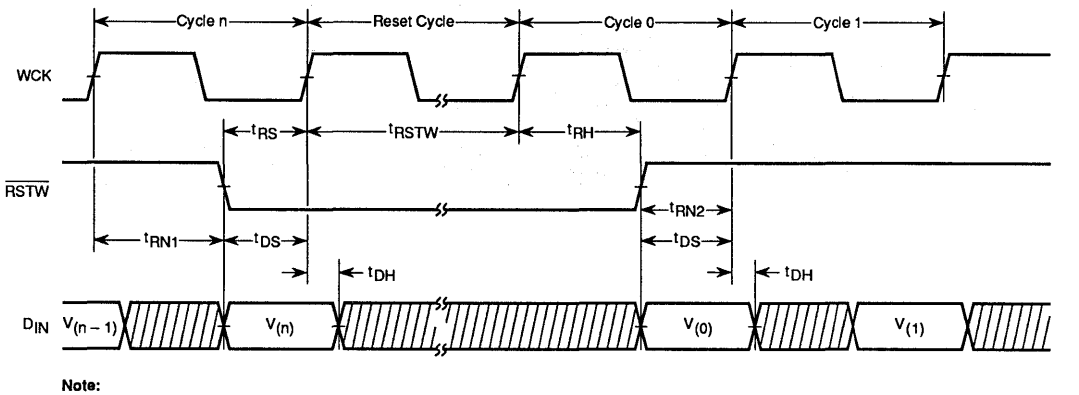
Read Reset Cycle



Note:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

83IH-6707B

Write Reset Cycle



Note:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

83IH-6706B

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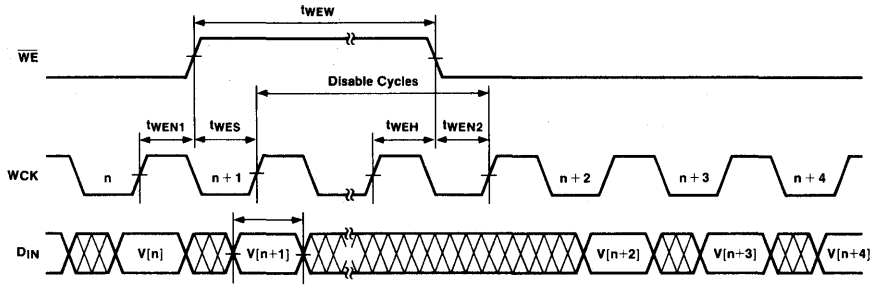
Timing Waveforms (cont)

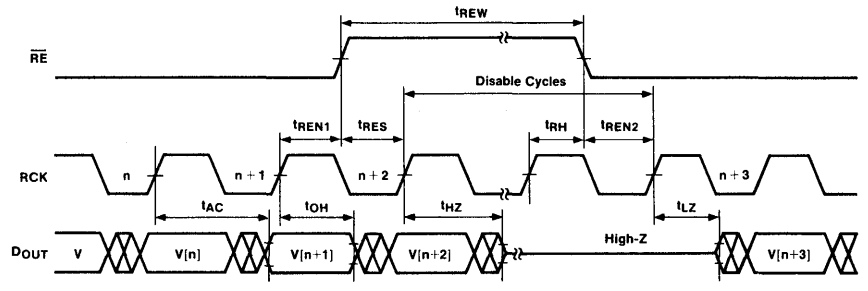
Write Disable Cycle



Note:
[1] V = Valid Data.

83-003723B

Read Disable Cycle

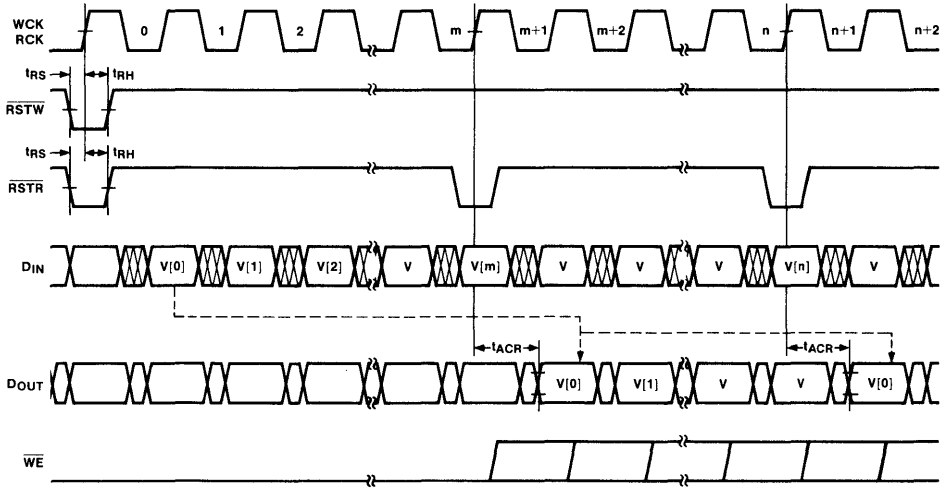


Note:
[1] V = Valid Data.

83-003646B

Timing Waveforms (cont)

Re-Read Cycle



Note:

[1] $\overline{RE} = V_{IL}$.

[2] V = Valid Data.

[3] The data stored in any location can be re-read as many times as desired within a period of 1 ms following the writing of data into that location provided that a second write operation has not re-written new data into that location.

83-003644B

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μPD42270
NTSC Field Buffer

June 1990

Description

The μPD42270 is a field buffer designed for NTSC TV applications and for other applications where serial data is needed. Equipped with four planes of 263-line by 910-bit storage, the μPD42270 can execute serial write and read cycles on any of the 263 lines. Within a line, four planes of 910 bits each may be written or read at the NTSC sampling rate of $4f_{SC}$.

Each of the four planes in the μPD42270 is equipped with two ports, one each for the write and read data registers. Each of the registers is split into two 455-bit segments but functions as if it were organized as one scan line of 910 bits. Independent control of write and read operation makes it possible for the device to operate synchronously or asynchronously at a clock frequency of 14.3 MHz or higher.

The synchronous option simplifies interframe luminance (Y) and chrominance (C) separation and interfield noise reduction and makes it easy to obtain a one-field delay line for digital TV and VCR applications requiring NTSC $4f_{SC}$ sampling. To obtain a very long delay, field length can be configured from 260 to 263 lines and line length of the last line from 896 to 910 bits.

The asynchronous option is useful in applications such as frame synchronization and time base correction, where line jump, line hold, line reset and pointer clear functions are required to support special effects in TV field processing.

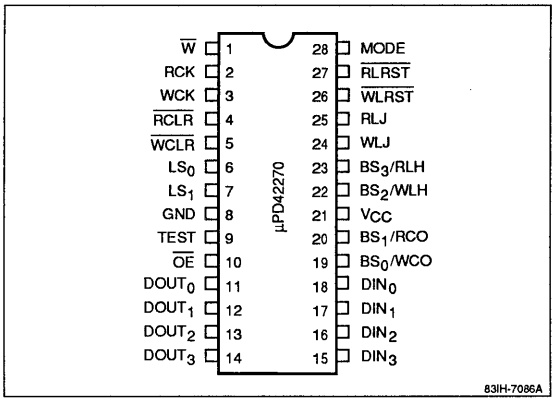
Regular refreshing of the device's dynamic storage cells is performed automatically by an internal circuit. All inputs and outputs, including clocks, are TTL-compatible. The μPD42270 is packaged in a 400-mil, 28-pin plastic DIP and is guaranteed for operation at −20 to +70°C.

Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42270C-60	40 ns	60 ns	28-pin plastic DIP

Pin Configuration

28-Pin Plastic DIP



Features

- Three functional blocks
  - — Four 263-line x 910-bit storage planes
  - — Four 910-bit write registers, one for each plane
  - — Four 910-bit read registers, one for each plane
- Two data ports: serial write and serial read
- Asynchronous operation
  - — Dual-port accessibility
  - — Carry-out feature to indicate position of scan line
  - — Line jump, line hold, line reset, and pointer clear functions
- Synchronous operation
  - — Variable field length: from 260 to 263 lines
  - — Variable last line length: from 896 to 910 bits
- Automatic refreshing
- CMOS technology
- Fully TTL-compatible inputs, outputs, and clocks
- Three-state outputs
- Single + 5-volt power supply
- On-chip substrate bias generator
- Standard 400-mil, 28-pin plastic DIP packaging

Pin Identification

Symbol	Function
D_{IN0} - D_{IN3}	Write data inputs
D_{OUT0} - D_{OUT3}	Read data outputs
$\overline{W}$	Write enable
$\overline{OE}$	Output enable
WCK	Write clock input
RCK	Read clock input
$\overline{WCLR}$	Write pointer clear
$\overline{RCLR}$	Read pointer clear
$\overline{WLRST}$	Write line reset
$\overline{RLRST}$	Read line reset
WLJ	Write line jump
RLJ	Read line jump
WLH	Write line hold
RLH	Read line hold
WCO	Write data register carry output
RCO	Read data register carry output
LS_0 - LS_1	Line select inputs
BS_0 - BS_3	Bit select inputs
MODE	Synchronous/asynchronous control
GND	Ground
V_{CC}	+5-volt power supply
TEST	Test pin (connect to GND in system)

Pin Functions

D_{IN0} - D_{IN3}. These pins function as write data inputs, e.g., for $4f_{SC}$ composite color or brightness signals.

D_{OUT0} - D_{OUT3}. These pins are three-state read data outputs.

$\overline{W}$. A low level on $\overline{W}$ enables write operation. $\overline{W}$ must be kept low throughout the entire scan line to ensure that data is stored serially; if $\overline{W}$ goes high any time during the WCK clock sequencing for a line, write operation will be disabled for the half of the line (455 bits) being written. The write address pointer increments in synchronization with WCK, regardless of $\overline{W}$.

$\overline{OE}$. This signal controls read data output. When $\overline{OE}$ is low, read data is output on D_{OUT0}-D_{OUT3}. When $\overline{OE}$ is high, D_{OUT0} - D_{OUT3} are in a state of high impedance. The read address pointer is incremented by RCK, regardless of the signal level of $\overline{OE}$.

WCK The rising edge of WCK latches write data from D_{IN0} - D_{IN3}. Each time this signal is activated, the write bit pointer increments sequentially and 4 bits of data are sampled and loaded into the write register. Although the register functions as one scan line of 910 bits, data is moved into and out of it in blocks of 455 x 4 bits. While 455 serial write cycles are being executed in one-half of the register, the 455 addresses previously written to the other half are simultaneously transferred to storage. Writing continues in this manner, alternating between the two halves of the register. Automatic refreshing and data transfer timing decisions are made by the internal arbitration circuit after each block of 455 addresses has been written.

RCK. The rising edge of RCK initiates read operation. Each time this signal is activated, the bit pointer increments by 1 and serial read cycles are executed in the read register. Although the register functions as one scan line of 910 bits, data is moved into and out of it in blocks of 455 x 4 bits. While 455 serial read cycles are being executed in one-half of the register, the 455 addresses previously read out of the other half are replaced by data from the storage array. Reading continues in this manner, alternating between the two halves of the register. Automatic refreshing and data transfer timing decisions are made by the arbitration circuit after each block of 455 addresses has been read. In synchronous operation, WCK controls read cycles and RCK is not used.

$\overline{WCLR}$. When $\overline{WLRST}$ is high, $\overline{WCLR}$ can be brought low to clear the write pointers to address 0 of the data register and scan line 0 of the storage array. At least one rising edge of WCK must occur while $\overline{WCLR}$ is held low for a minimum of 3 μs to ensure clearing of both pointers. The clear function ends when $\overline{WCLR}$ goes high. If $\overline{WLRST}$ is still high, the next rising edge of WCK writes the data on D_{IN0} - D_{IN3} into address 0 of the write register.

$\overline{RCLR}$. When $\overline{RLRST}$ is high, $\overline{RCLR}$ can be brought low to clear the read pointers to address 0 of the data register and scan line 0 of the storage array (asynchronous operation only). At least one rising edge of RCK must occur while $\overline{RCLR}$ is held low for a minimum of 3 μs to ensure clearing of both pointers. The clear function ends when $\overline{RCLR}$ goes high. If $\overline{RLRST}$ is still high, the data from address 0 is read out on D_{OUT0} - D_{OUT3} and the next rising edge of RCK initiates data access from address 1.

$\overline{WLRST}$. This pin is used in synchronous or asynchronous operation to reset the bit pointer to address 0 of the line following the one to which the signal is applied. In standard write operation, the scan line pointer increments by 1 whenever the bit pointer reaches the last address of a line. If $\overline{WCLR}$ is high, $\overline{WLRST}$ can be brought low for a minimum of 3 μs to force an end-of-

line condition, whereby write cycles begin executing from address 0 of the next sequential scan line. When used in conjunction with WLH, $\overline{\text{WLRST}}$ resets the current scan line; when combined with WLJ, $\overline{\text{WLRST}}$ begins writing from address 0 of the line to which the scan line pointer is jumped.

$\overline{\text{RLRST}}$. This pin is valid in asynchronous operation and can be used to reset the bit pointer to address 0 of the read line following the one to which the signal is applied. In standard read operation, the scan line pointer increments by 1 whenever the bit pointer reaches the last address of a line. If $\overline{\text{RCLR}}$ is high, $\overline{\text{RLRST}}$ can be brought low for a minimum of 3 μs to force an end-of-line condition, whereby read cycles begin executing from address 0 of the next sequential scan line. When used in conjunction with RLH, $\overline{\text{RLRST}}$ resets the current scan line; when combined with RLJ, $\overline{\text{RLRST}}$ begins reading from address 0 of the line to which the scan line pointer is jumped.

WLJ. Each positive pulse of this signal increments the write scan line pointer by one line (asynchronous operation only). WLJ is sampled at the rising edge of WCK. If WLJ is high, a single jump is executed. If WLJ remains high, no further jumps occur. To jump again, WLJ must go low for at least one rising edge of WCK before going high again. It takes a minimum of two WCK cycles to complete a line jump. The first cycle senses the high level of WLJ and increments the scan line pointer. An additional WCK cycle with WLJ low is required to complete the function. If more than one line jump is needed, then the sequence must be repeated. A line jump occurs either when the current line has been completely filled or after $\overline{\text{WLRST}}$ has reset the write address. The new scan line can be calculated by n+11+1x (where "n" is the current line and "x" equals the number of positive WLJ pulses). Changes in the level of WLJ must be made when the bit pointer is between locations 229 and 909 of the current line and when $\overline{\text{WCLR}}$ and $\overline{\text{WLRST}}$ are high and WLH is low.

RLJ. Each positive pulse of this signal increments the read scan line pointer by one line (asynchronous operation only). RLJ is sampled at the rising edge of RCK. If RLJ remains high, a single line jump is executed. To jump again, RLJ must go low for at least one rising edge of RCK before going high again. It takes a minimum of two RCK cycles to complete a line jump. The first cycle senses the high level of RLJ and increments the scan line pointer. An additional RCK cycle with RLJ low is required to complete the function.If more than one line jump is needed, then this sequence must be repeated.

A line jump occurs either when the current line has been completely read or after $\overline{\text{RLRST}}$ has reset the read address. The new scan line can be calculated by n+1+x (where "n" is the current line and "x" equals the number of positive RLJ pulses).

Changes in the level of RLJ must be made when the bit pointer is between locations 682 and 909 of the previous line, or between 0 and 452 of the current line, and when $\overline{\text{RCLR}}$ and $\overline{\text{RLRST}}$ are high and RLH is low.

WLH. Once this input is applied, the write scan line pointer will hold its position even if successive write clocks are applied. The level of WLH is sampled at the rising edge of WCK and must be applied between locations 229 and 909 of the line to be held. The held line is released after 910 addresses have been rewritten or after $\overline{\text{WLRST}}$ resets the write line address. WLH is multiplexed with BS_2 and is valid in asynchronous operation only. WLH (high) must be input only when $\overline{\text{WCLR}}$ and $\overline{\text{WLRST}}$ are high and WLJ is low.

RLH. Once this input is applied, the read scan line pointer will hold its position even if successive read clocks are applied. The level of RLH is sampled at the rising edge of RCK and must be clocked between locations 682 and 909 of the line preceding the line to hold, or between locations 0 and 452 of the line to hold. The held line is released after 910 addresses have been read or after $\overline{\text{RLRST}}$ resets the read line address. RLH (high) must be input only when $\overline{\text{RCLR}}$ and $\overline{\text{RLRST}}$ are high and RLJ is low. RLH is multiplexed with BS_3 and is valid in asynchronous operation only.

WCO. When the bit pointer reaches address 909 of the write data register, this signal goes high for one WCK cycle. WCO is multiplexed with BS_0 and is valid in asynchronous operation only.

RCO. When the bit pointer reaches address 909 of the read data register, this signal goes high for one RCK cycle. RCO is multiplexed with BS_1 and is valid in asynchronous operation only.

BS_0 - BS_3. These pins control the number of bits in the last line of the field. The combined signals of BS_0-BS_3 set the line length from 896 to 910 bits in one-bit steps (table 1). The length of the last line can change for each field, but all four pins should not be set low. BS_0, BS_1, BS_2 and BS_3 are multiplexed with WCO, RCO, WLH and RLH, respectively, and are valid in synchronous operation only. In asynchronous operation, the line length is fixed at 910 bits.

LS_0 - LS_1. These pins control the number of lines for one field in either synchronous or asynchronous operation. The combined signals of LS_0 and LS_1 set the number of lines to 260, 261, 262, or 263 (table 2). The number of lines can be changed for each field.

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MODE. This pin selects the operating mode. A low signal selects synchronous operation and a high signal selects asynchronous operation. If MODE is changed after power has been applied to the μPD42270, it is necessary to clear the address pointers by bringing $\overline{WCLR}$ and $\overline{RCLR}$ low. MODE can be changed at any time; however, data input in one mode may be unreliable in the other (see table 3 for valid pin functions).

Table 1. Line Length Adjustment

BS_3	BS_2	BS_1	BS_0	Number of Bits in the Last Line
L	L	L	L	Prohibited
L	L	L	H	896
L	L	H	L	897
L	L	H	H	898
L	H	L	L	899
L	H	L	H	900
L	H	H	L	901
L	H	H	H	902
H	L	L	L	903
H	L	L	H	904
H	L	H	L	905
H	L	H	H	906
H	H	L	L	907
H	H	L	H	908
H	H	H	L	909
H	H	H	H	910

Notes:

(1) LS_0 - LS_1 and BS_0 - BS_3 must be held at a stable high or low level to maintain the number of bits per scan line and the number of scan lines per field while the line pointer indicates the position between lines 258 and 262.

Table 2. Line Number Adjustment

LS_1	LS_0	Number of Lines
L	L	260
L	H	261
H	L	262
H	H	263

Notes:

(1) LS_0 - LS_1 and BS_0 - BS_3 must be held at a stable high or low level to maintain the number of bits per scan line and the number of scan lines per field while the line pointer indicates a position between lines 258 and 262.

Table 3. Valid Pin Functions According to Mode

Pin Name	Synchronous Mode (Note 1)	Asynchronous Mode (Note 2)
MODE	0	1
BS_0/WCO	BS_0	WCO
BS_1/RCO	BS_1	RCO
BS_2/WLH	BS_2	WLH
BS_3/RLH	BS_3	RLH
$\overline{RCLR}$	Invalid	Valid
RCK	Invalid	Valid
$\overline{RLRST}$	Invalid	Valid
$\overline{WCLR}$	Valid	Valid
WCK	Valid	Valid
$\overline{WLRST}$	Valid	Valid
WLJ	Invalid	Valid
RLJ	Invalid	Valid

Notes:

(1) Write and read cycles are controlled by $\overline{WCLR}$, WCK, and $\overline{WLRST}$ in synchronous operation.

(2) In asynchronous operation, write and read cycles are controlled independently.

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; GND = 0 V; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	D_{IN0} - D_{IN3}, $\overline{W}$, $\overline{OE}$, WCK, RCK, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$, WLJ, RLJ, LS_0 - LS_1, BS_2/WLH, BS_3/RLH, MODE
I/O capacitance	$C_{I/O}$			8	pF	BS_0/WCO, BS_1/RCO
Output capacitance	C_O			7	pF	D_{OUT} - D_{OUT}

DEVICE OPERATION

The μPD42270 supports two operating modes to accommodate various NTSC TV applications. Depending on the logic level of the MODE pin, the device will execute either synchronous or asynchronous write and read cycles on the addresses specified by the internal address pointers. When selecting the mode after power-on, it is necessary to reset these pointers to starting address 0 using $\overline{WCLR}$ and $\overline{RCLR}$. The level of MODE may be changed at any time.

Synchronous Mode

In synchronous mode, write and read cycles are executed simultaneously by $\overline{WCLR}$, $\overline{WLRST}$, WCK, $\overline{W}$ and $\overline{OE}$ to create a delay line, which means that write and read addresses always coincide. After all lines within a field have been written, they then are read out as the device begins overwriting new data to the same addresses again. Field length may be configured from 260 to 263 lines and last line length from 896 to 910 bits by means of the LS and BS pins, respectively. Synchronous operation is useful in applications where a very long delay line is required and may be selected by setting MODE low.

Asynchronous Mode

In asynchronous mode, $\overline{WCLR}$, $\overline{WLRST}$, WCK and $\overline{W}$ control write cycles, while read cycles are controlled independently by $\overline{RCLR}$, $\overline{RLRST}$, RCK and $\overline{OE}$. Field length may be configured from 260 to 263 lines using LS_0 - LS_1. Line length remains fixed at 910 bits and BS_0-BS_3 are disabled to provide for the register carry out, line hold, and line jump functions. Asynchronous operation is useful for frame synchronization or time base correction and may be selected by setting MODE high.

Address Clear. Setting $\overline{WCLR}$ and $\overline{RCLR}$ low for a minimum of 3 μs during successive WCK and RCK cycles initializes the internal pointers to starting address 0 of the first scan line ($\overline{RCLR}$ is disabled in synchronous mode). Although address clear signals must meet the specifications for setup and hold times as measured from the rising edges of WCK and RCK, they are not dependent on the status of $\overline{W}$ or $\overline{OE}$. An address clear cycle cannot occur in conjunction with $\overline{WLRST}$ or $\overline{RLRST}$ line reset cycles.

Write Operation. Write cycles are executed in synchronization with WCK as $\overline{W}$ is held low. Bits are input sequentially into one of the two halves of the data register before being transferred to the storage array. Since data is transferred into the array in blocks of 455 x 4 bits, no data transfer occurs if $\overline{W}$ goes high to disable write operation before all 455 bits are written. Despite write operation being disabled, the internal bit pointer continues to increment with each successive write clock.

Read Operation. Read cycles are executed in synchronization with RCK (asynchronous operation only) or WCK (synchronous operation only) as $\overline{OE}$ is held low. If $\overline{OE}$ goes high any time during a cycle, the outputs are in a state of high impedance until OE returns low. Since the internal bit pointer increments by 1 in spite of read operation being disabled, it is always important to reset the write and read pointers using $\overline{WCLR}$ and $\overline{RCLR}$ prior to beginning or resuming operation at the first address location in the array.

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Special Functions

Line Reset. A line reset is similar to an address clear cycle, except that it only affects the bit pointers within a line. While $\overline{WCLR}$ and $\overline{RCLR}$ are held high, $\overline{WLRST}$ or $\overline{RLRST}$ can be brought low for a minimum of 3 μs during successive WCK or RCK cycles to reset the bit pointer to address 0 of the scan line. At the completion of the reset cycle, the next sequential scan line will be selected unless line hold (WLH or RLH) or line jump (WLJ or RLJ) are also used. See $\overline{WLRST}$ and $\overline{RLRST}$ for more detail.

A combination of line reset and an address clear cycle must be separated by at least one serial clock cycle. The timing relationship of WCLR, $\overline{WLRST}$ and WCK (or RCLR, $\overline{RLRST}$ and RCK) is shown in figure 1.

In asynchronous operation, $\overline{WLRST}$ and $\overline{RLRST}$ independently reset the write and read bit pointers. During synchronous operation, $\overline{WLRST}$ resets both pointers.

Line Jump. With the line jump function, it is possible to advance the current write or read line position according to the number of positive WLJ or RLJ pulses applied (see descriptions for the WLJ and RLJ pins). In this cycle, which is valid in asynchronous mode only, the scan line pointer resets to address 0 if the number of positive pulses causes the resulting line number (n+11+1x, where "n" is the current line number and "x" is the number of positive WLJ or RLJ pulses) to exceed the maximum line number (number of lines minus 1) specified by the LS_0 and LS_1 pins (table 2).

Line Hold. The line hold feature is available in asynchronous mode only and can be used to prevent the internal scan line pointers from incrementing to the next sequential address. The read and write line pointers may be held independently; however, restrictions pertaining to when this function can be initiated, detailed in the descriptions for the WLH and RLH pins, should be carefully followed.

Block Diagram

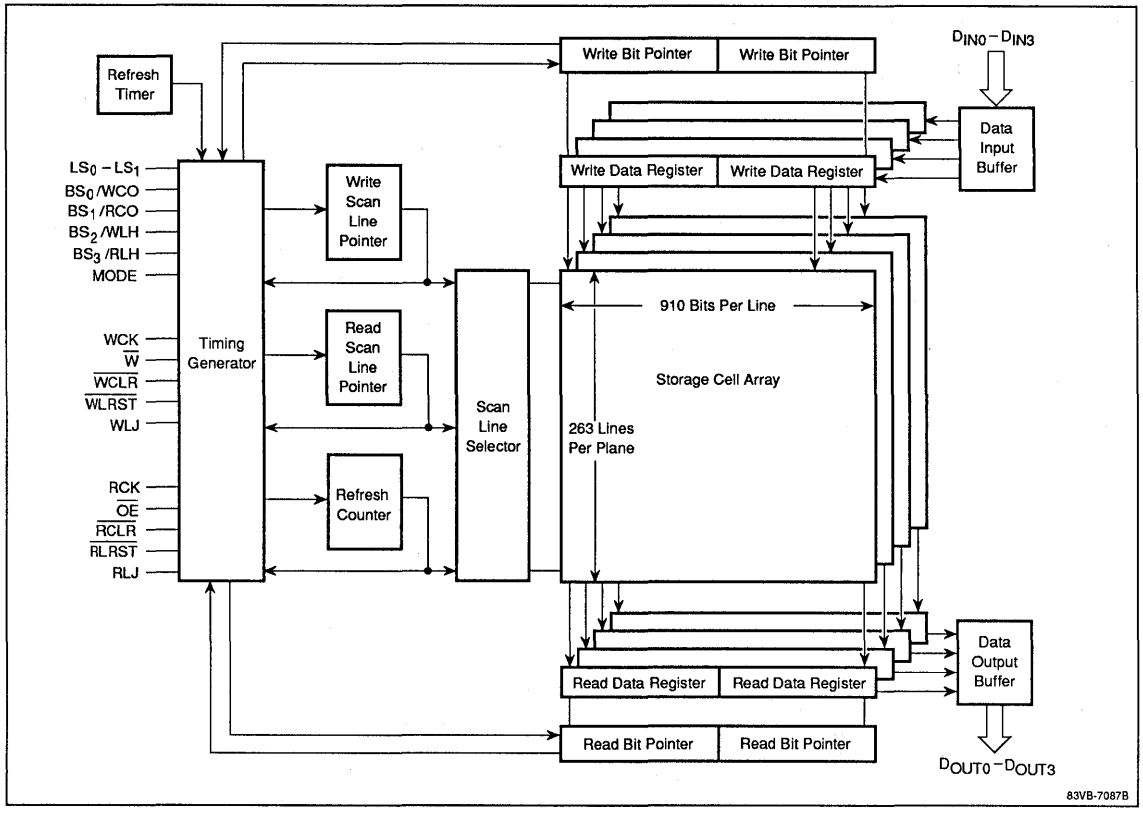
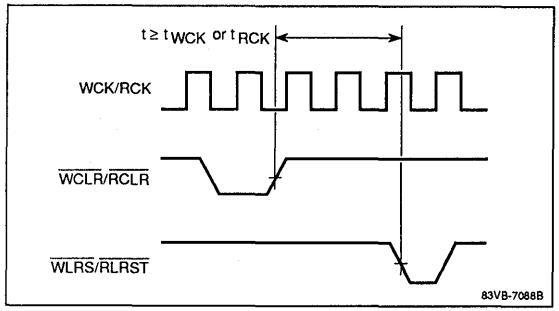


Figure 1. Separation of Clear and Reset Signals



Absolute Maximum Ratings

Supply voltage on any pin except V_{CC} relative to GND, V_{R1}	−1.5 to +7.0 V
Supply voltage on V_{CC} relative to GND, V_{R2}	−1.5 to +7.0 V
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.5 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Ambient temperature	T_A	−20		70	°C

DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{IL}	−10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_{OL}	−10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA
Standby current	I_{CC1}		6	20	mA	WCK, RCK = V_{IL}
Operating current	I_{CC2}		40	80	mA	t_{WCK} = t_{WCK} (min); t_{RCK} = t_{RCK} (min)

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Access time from RCK	t_{AC}		40	ns	
Write clock cycle time	t_{WCK}	60		ns	(Note 5)
Write clock active pulse width	t_{WCW}	20		ns	
Write clock precharge time	t_{WCP}	20		ns	
Read clock cycle time	t_{RCK}	60		ns	(Note 5)
Read clock active pulse width	t_{RCW}	20		ns	
Read clock precharge time	t_{RCP}	20		ns	
Output hold time	t_{OH}	5		ns	
Output low impedance delay	t_{LZ}	5	40	ns	(Note 6)
Data output buffer high impedance delay	t_{HZ}	5	40	ns	(Note 7)
Input data setup time	t_{DS}	15		ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input data hold time	t_{DH}	3		ns	
$\overline{WCLR}$ ($\overline{RCLR}$) setup time before the rising edge of WCK (RCK)	t_{CS}	20		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) hold time after the rising edge of WCK (RCK)	t_{CH}	3		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) invalid hold time after the rising edge of WCK (RCK)	t_{CN1}	5		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) invalid setup time before the rising edge of WCK (RCK)	t_{CN2}	20		ns	(Note 8)
$\overline{WCLR}$ ($\overline{RCLR}$) low level valid time	t_{CLR}	3		μs	
$\overline{WLRST}$ ($\overline{RLRST}$) setup time before the rising edge of WCK (RCK)	t_{LRS}	20		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) hold time after the rising edge of WCK (RCK)	t_{LRH}	3		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) invalid hold time after the rising edge of WCK (RCK)	t_{LRN}	5		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) invalid setup time before the rising edge of WCK (RCK)	t_{LRN}	20		ns	(Note 8)
$\overline{WLRST}$ ($\overline{RLRST}$) low level valid time	t_{LRST}	3		μs	
$\overline{W}$ setup time before the rising edge of WCK	t_{WS}	20		ns	(Note 9)
$\overline{W}$ hold time after the rising edge of WCK	t_{WH}	3		ns	(Note 9)
$\overline{W}$ valid hold time after subline (1/2) switch	t_{WN1}	5		ns	(Note 9)
$\overline{W}$ valid setup time before subline (1/2) switch	t_{WN2}	20		ns	(Note 9)
WLH (RLH) setup time before the rising edge of WCK (RCK)	t_{LHS}	20		ns	
WLH (RLH) hold time after the rising edge of WCK (RCK)	t_{LHH}	3		ns	
WLH invalid hold time measured from the end of write cycle 227	t_{WHN1}	5		ns	
WLH invalid setup time measured before write cycle 0	t_{WHN2}	20		ns	
RLH invalid hold time measured from the end of read cycle 681	t_{RHN1}	5		ns	
RLH invalid setup time measured before read cycle 453	t_{RHN2}	20		ns	
WLJ (RLJ) setup time before the rising edge of WCK (RCK)	t_{LJS}	20		ns	
WLJ (RLJ) hold time after the rising edge of WCK (RCK)	t_{LJH}	3		ns	
WLJ hold time measured from the end of write cycle 227	t_{WJN1}	5		ns	
WLJ setup time measured before write cycle 0	t_{WJN2}	20		ns	
RLJ hold time measured from the end of read cycle 681	t_{RJN1}	5		ns	
RLJ setup time measured before read cycle 453	t_{RJN2}	20		ns	
$\overline{OE}$ setup time before the rising edge of RCK (WCK)	t_{OES}	20		ns	(Note 9)
$\overline{OE}$ hold time after the rising edge of RCK (WCK)	t_{OEH}	3		ns	(Note 9)
$\overline{OE}$ valid hold time after the rising edge of RCK (WCK)	t_{OEN1}	5		ns	(Note 9)
$\overline{OE}$ valid setup time before the rising edge of RCK (WCK)	t_{OEN2}	20		ns	(Note 9)
LS, BS setup time before WCK (RCK), line 258	t_{FSS}	0		ns	
LS, BS hold time after WCK (RCK), line 0	t_{FSH}	3		μs	
Write carry output high level delay	t_{WCLH}		40	ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Write carry output low level delay	t_{WCHL}		40	ns	
Read carry output high level delay	t_{RCLH}		40	ns	
Read carry output low level delay	t_{RCHL}		40	ns	
Transition time	t_T	3	35	ns	(Note 4)

Notes:

(1) All voltages are referenced to GND

(2) Ac measurements assume t_T = 5 ns.

(3) Input timing reference levels = 1.5 V; input levels are measured between GND and 3.0 V; output levels are measured between 0.8 and 2.0 V. See figures 2 and 3.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = −20 to 70°C) is assured.

(6) This delay is measured at −200 mV from the steady-state voltage with the load specified in figure 5.

(7) This delay is measured at the maximum steady-state output high voltage −200 mV or the minimum steady-state output low voltage +200 mV with the load specified in figure 5.

(8) For proper execution of the pointer clear and line reset functions, specifications for t_{CS}, t_{CH}, t_{CN1}, t_{CN2}, t_{LRS}, t_{LRH}, t_{LRN1} and t_{LRN2} must be met; otherwise, these functions may not affect the desired cycles or may affect adjacent cycles erroneously.

(9) If a $\overline{W}$ (or $\overline{OE}$) pulse does not satisfy the specifications for t_{WS}, t_{WH}, t_{WN1} and t_{WN2} (or t_{OES}, t_{OEH}, t_{OEN1} and t_{OEN2}), the write disable function (output high impedance) being executed may not affect the desired cycles or may affect adjacent cycles erroneously.

(10) For the μPD42270 to read new data, read operation must be delayed from write operation by at least 920 cycles. In those cases where the delay is less than 920 cycles, read data will vary as shown below:

Source of Read Data	Delay Between Write and Read Operation
Old data	0 to 450 cycles
Indeterminate (either old or new data)	451 to 919 cycles
New data	920 or more cycles

Figure 2. Input Timing

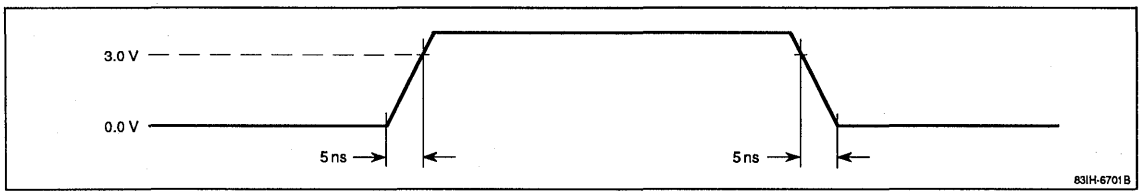


Figure 3. Output Timing

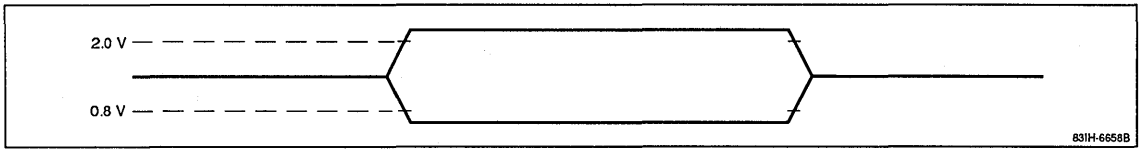


Figure 4. Output Loading for t_{AC}, t_{OH}, t_{WCLH}, t_{WCHL}, t_{RCLH}, t_{RCHL}

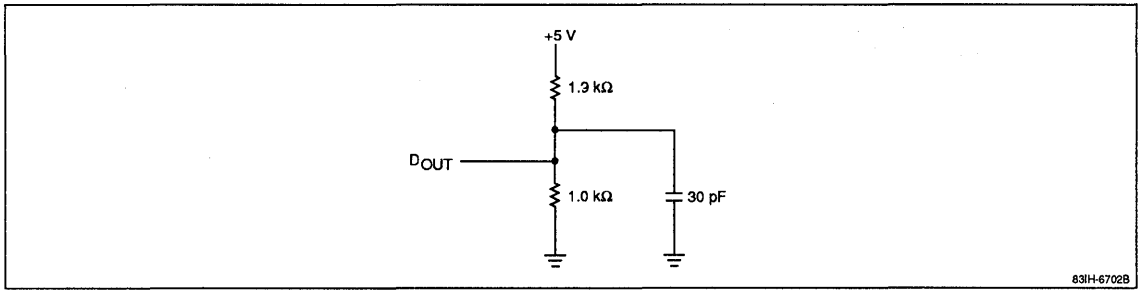
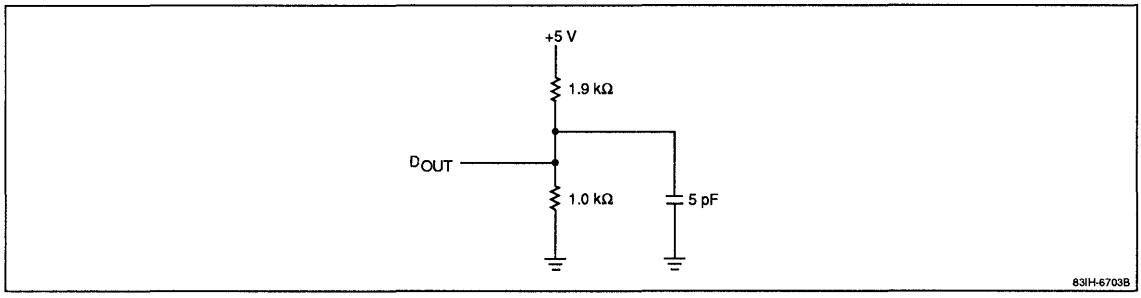
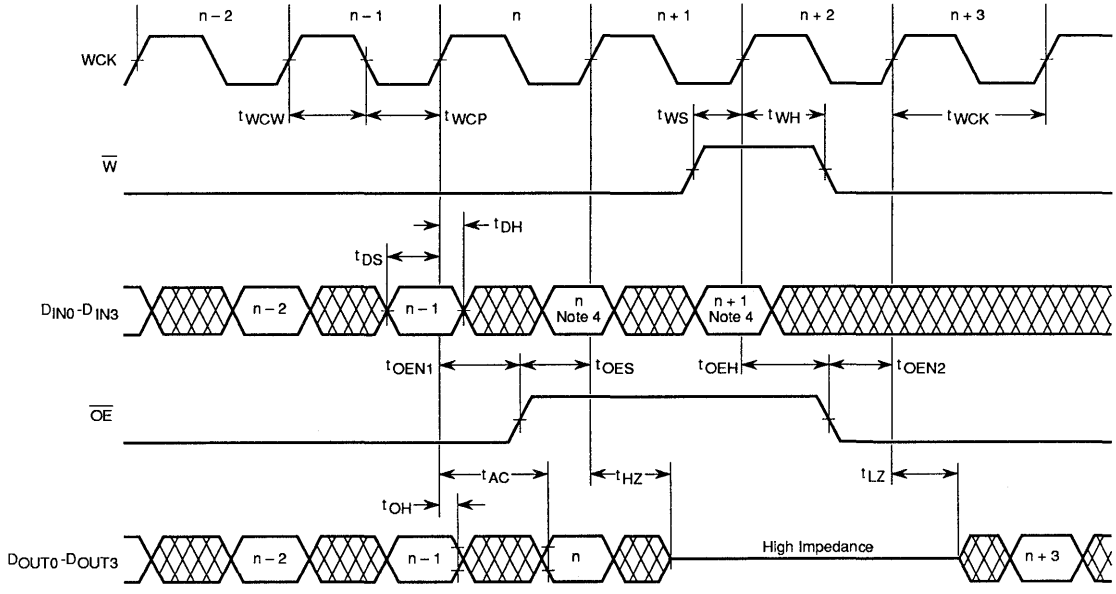


Figure 5. Output Loading for t_{LZ} and t_{HZ}



Timing Waveforms

Synchronous Write/Read Cycle



Notes:

[1] In synchronous mode, output data is delayed by one field from the input data.

[2] $\overline{WLRST}$ = $\overline{WCLR}$ = V_{IH}. MODE = V_{IL}. LS_0 and LS_1 = V_{IH} or V_{IL}. $\overline{RLRST}$, $\overline{RCLR}$, and RCK are "don't care" inputs.

[3] BS_0 - BS_3 = V_{IH} or V_{IL}.

[4] Data is transferred into and out of the data registers in blocks of 455 x 4 bits. When $\overline{W}$ goes high before all 455 words are input, write operation is disabled and none of the words are transferred to the storage array.

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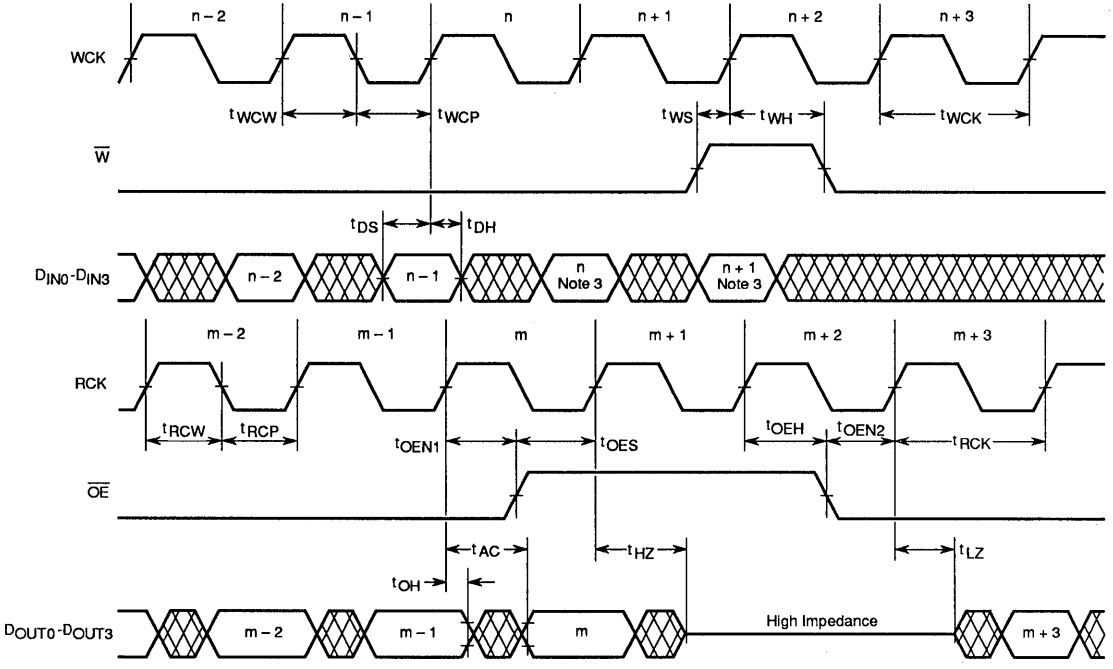
Timing Waveforms (cont)

Asynchronous Write and Read Cycles



Notes:

[1] $\overline{WCLR} = \overline{RCLR} = V_{IH}$. $\overline{WLRST} = \overline{RLRST} = V_{IH}$. MODE = V_{IH}.

[2] RLJ, WLJ, WLH, and RLH = V_{IH} or V_{IL}. LS_0 and LS_1 = V_{IH} or V_{IL}.

[3] Data is transferred into and out of the data registers in blocks of 455 x 4 bits. When $\overline{W}$ goes high before all 455 words are input, write operation is disabled and none of the words are transferred to the storage array.

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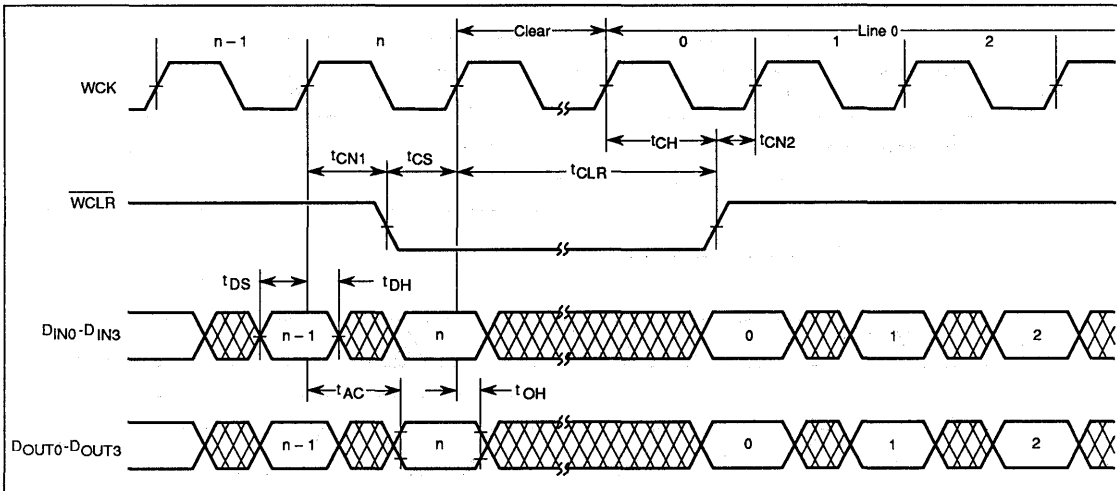
Timing Waveforms (cont)

Synchronous Pointer Clear Cycle



Notes:

[1] $\overline{W} = \overline{OE} = V_{IL}$. MODE = V_{IL}.

[2] LS_0 and $LS_1 = V_{IH}$ or V_{IL}. BS_0, BS_1, BS_2 and $BS_3 = V_{IH}$ or V_{IL}.

[3] $\overline{RLRST}$, $\overline{RCLR}$, and RCK = don't care.

[4] $\overline{WLRST} = V_{IH}$ during the clear cycle.

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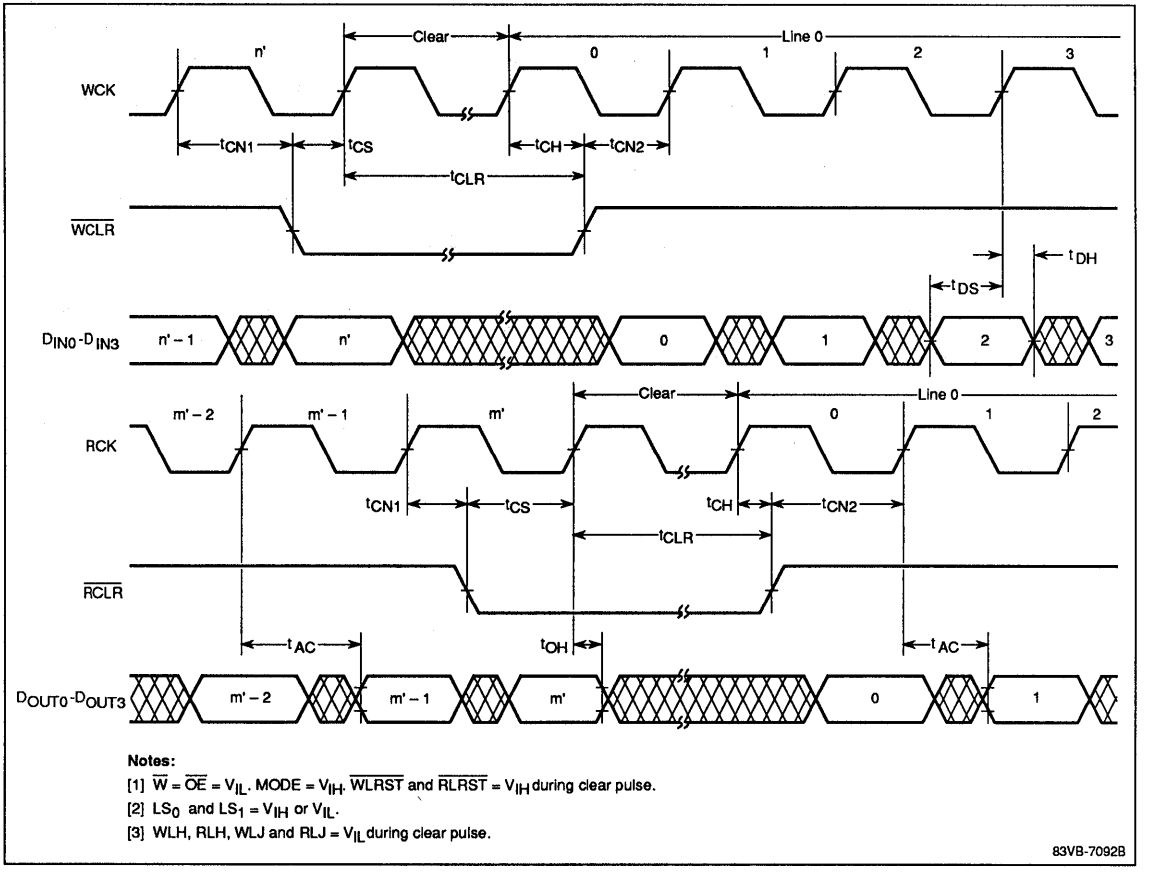
Timing Waveforms (cont)

Asynchronous Pointer Clear Cycle



Notes:

[1] $\overline{W} = \overline{OE} = V_{IL}$. MODE = V_{IH}. $\overline{WLRST}$ and $\overline{RLRST} = V_{IH}$ during clear pulse.

[2] LS_0 and $LS_1 = V_{IH}$ or V_{IL}.

[3] WLH, RLH, WLJ and RLJ = V_{IL} during clear pulse.

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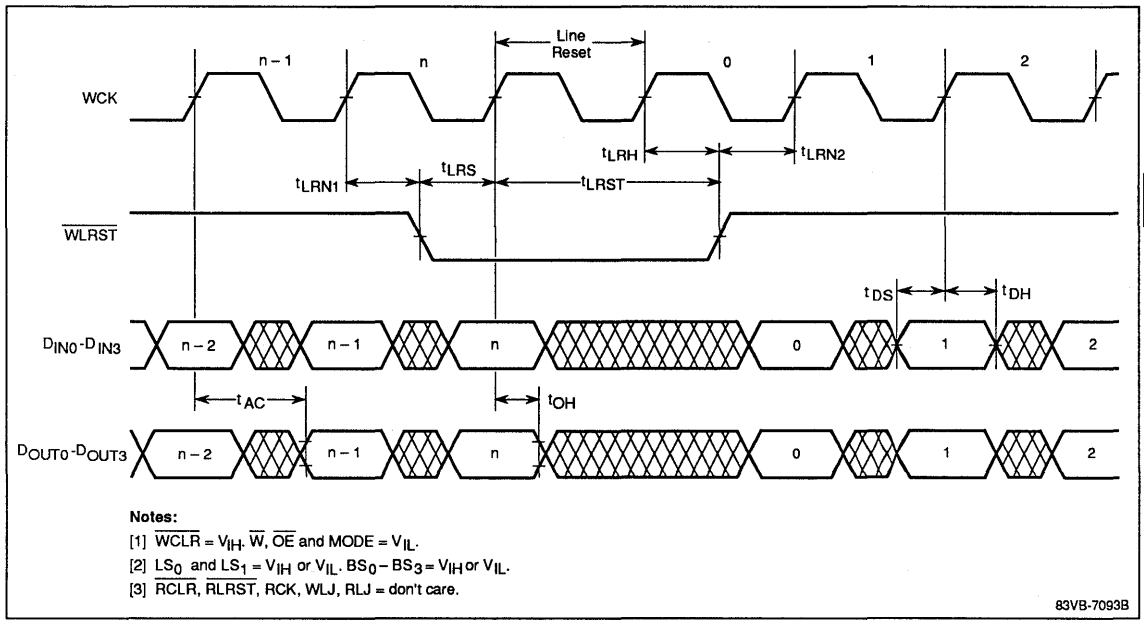
Timing Waveforms (cont)

Synchronous Line Reset Cycle



Notes:

[1] $\overline{WCLR}$ = V_{IH}. $\overline{W}$, $\overline{OE}$ and MODE = V_{IL}.

[2] LS_0 and LS_1 = V_{IH} or V_{IL}. $BS_0 - BS_3$ = V_{IH} or V_{IL}.

[3] $\overline{RCLR}$, $\overline{RLRST}$, RCK, WLJ, RLJ = don't care.

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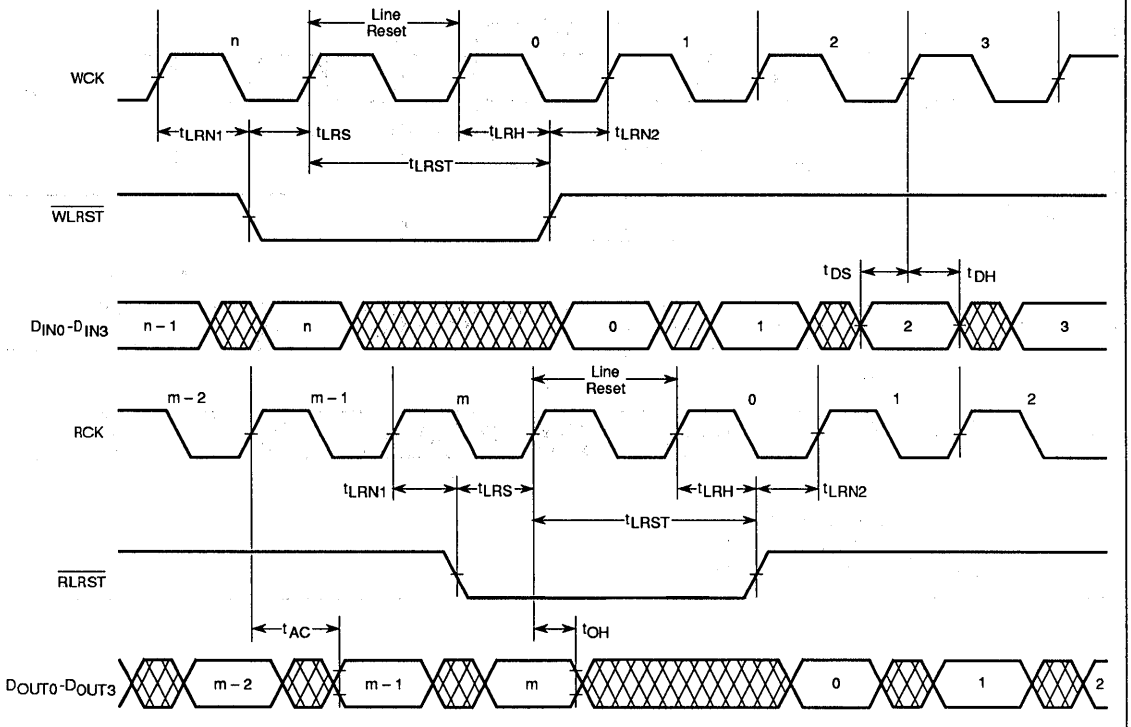
Timing Waveforms (cont)

Asynchronous Line Reset Cycle



Notes:

[1] $\overline{WCLR}$, $\overline{RCLR}$ and MODE = V_{IH}, WLH, RLH, WLJ, and RLJ = V_{IL} during a reset cycle.

[2] LS_0 and $LS_1 = V_{IL}$.

[3] $\overline{W} = \overline{OE} = V_{IL}$.

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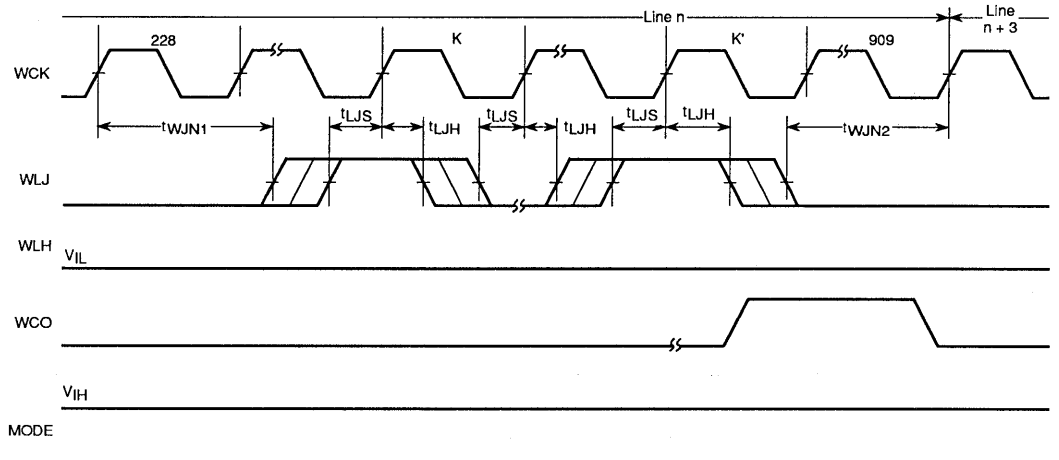
Timing Waveforms (cont)

Write Line Jump Cycle



Notes:

[1] $\overline{RCLR}$, $\overline{RLRST}$, RCK, RLH, RLJ, $\overline{W}$, and $\overline{OE}$ = don't care.

[2] K and K' = 229 to 909 of line n.

[3] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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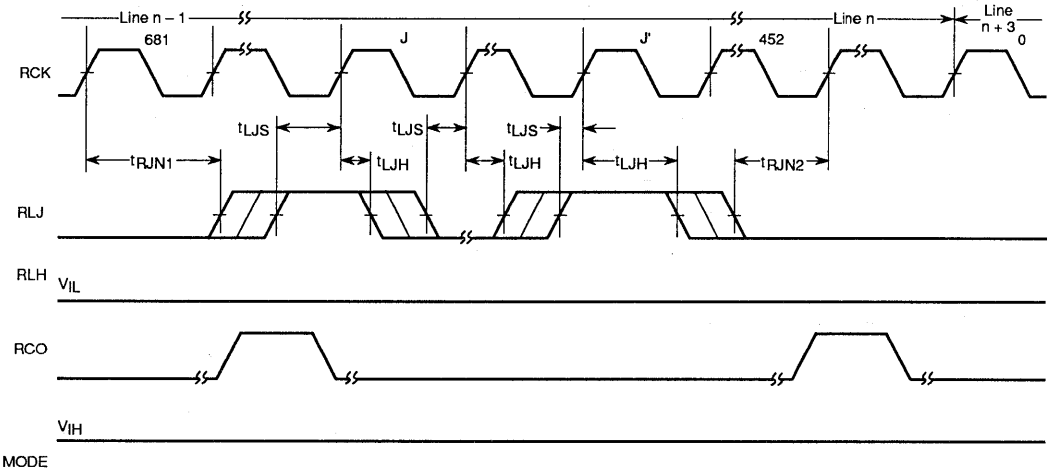
Read Line Jump Cycle



Notes:

[1] $\overline{WCLR}$, $\overline{WLRST}$, WCK, WLH, WLJ, $\overline{W}$, and $\overline{OE}$ = don't care.

[2] J and J' = 0 to 452 of line n or 682 to 909 of line n – 1.

[3] $\overline{RLRST}$ and $\overline{RCLR}$ = V_{IH}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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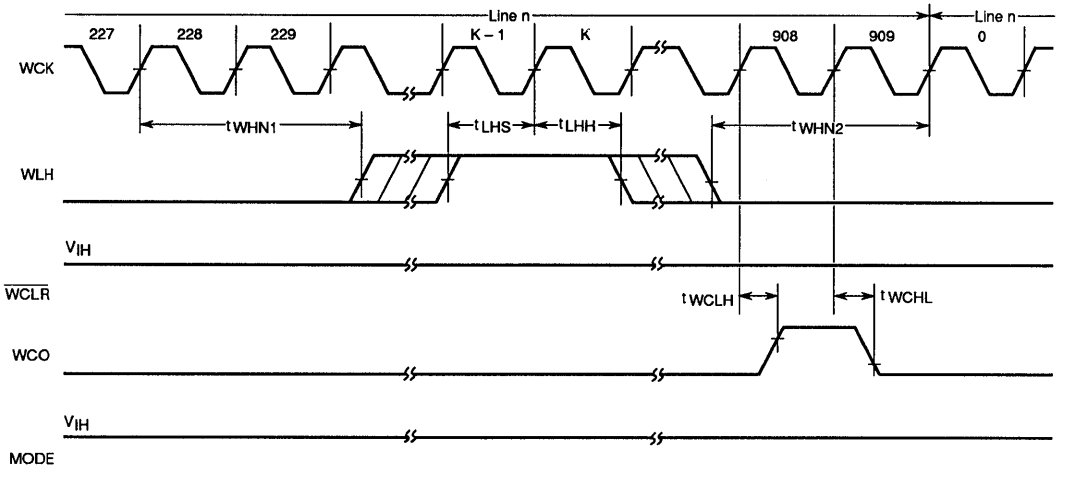
Timing Waveforms (cont)

Write Line Hold Cycle



Notes:

[1] $\overline{RLRST}$, RLJ, $\overline{W}$, RLH, $\overline{OE}$, $\overline{RCLR}$, and RCK = don't care.

[2] K = 229 to 909.

[3] $\overline{WLRST}$ = V_{IH}, WLJ = V_{IL}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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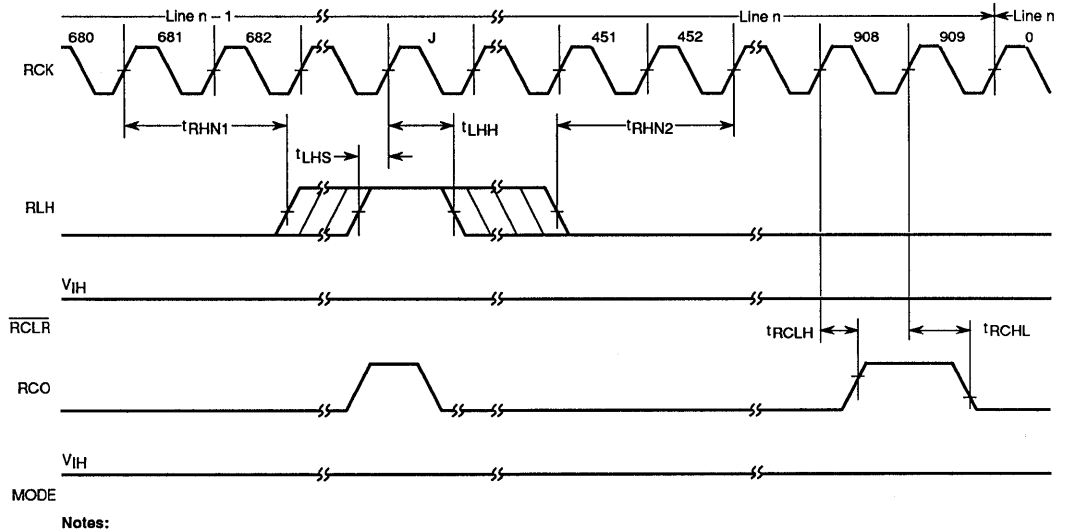
Read Line Hold Cycle



Notes:

[1] $\overline{WLRST}$, WLJ, $\overline{W}$, WLH, $\overline{OE}$, $\overline{WCLR}$, and WCK = don't care.

[2] J = 682 to 909 in $(n-1)^{th}$ or 0 to 452 in n^{th} line.

[3] $\overline{RLRST}$ = V_{IH}, RLJ = V_{IL}.

[4] LS_0 and LS_1 = V_{IH} or V_{IL}.

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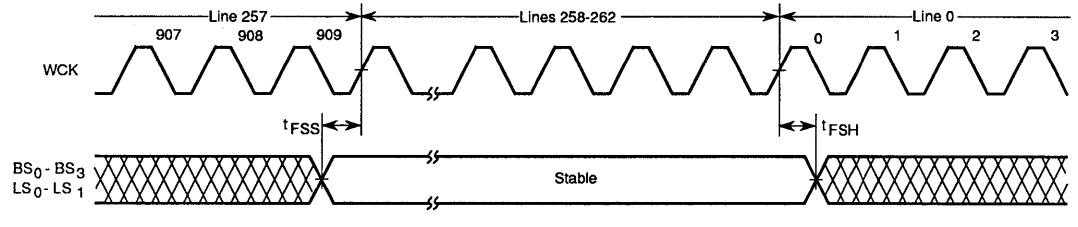
Timing Waveforms (cont)

Synchronous Field Buffer Size Adjustment



Notes:
[1] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.
[2] MODE = V_{IL}.
[3] $\overline{RLRST}$, $\overline{W}$, RCK, $\overline{RCLR}$, and $\overline{OE}$ = don't care.

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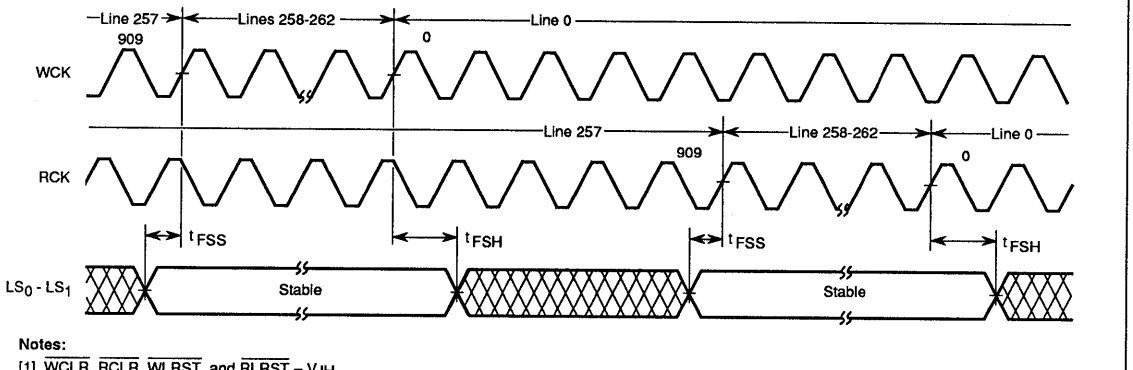
Asynchronous Field Buffer Size Adjustment



Notes:
[1] $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.
[2] MODE = V_{IH}. WLJ and RLJ = V_{IL}.
[3] $\overline{W}$, $\overline{OE}$, WLH, and RLH = don't care.

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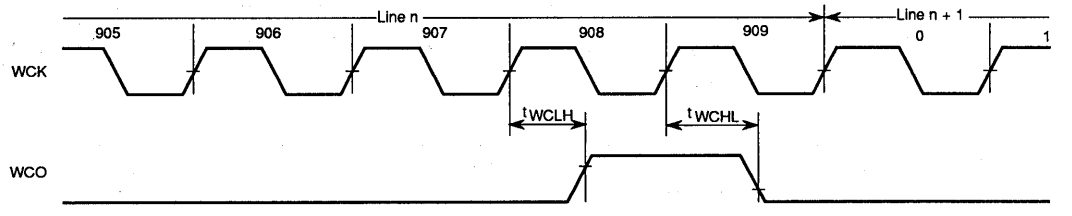
Timing Waveforms (cont)

Write Register Carry Out



Notes:

[1] MODE, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$ = V_{IH}

[2] LS_0 and LS_1 = V_{IH} or V_{IL}

[3] $\overline{OE}$, $\overline{W}$, WLH, RLH, WLJ, RLJ = don't care.

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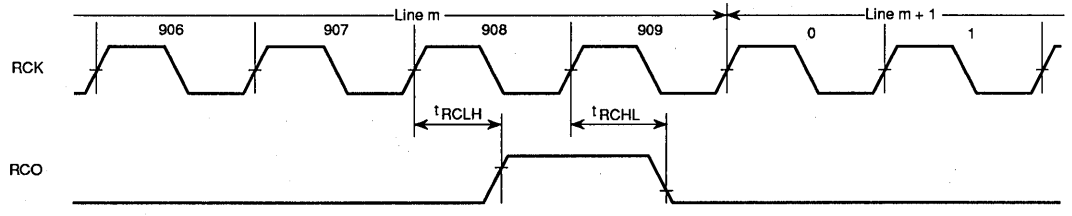
Read Register Carry Out



Notes:

[1] MODE, $\overline{WCLR}$, $\overline{RCLR}$, $\overline{WLRST}$, $\overline{RLRST}$ = V_{IH}.

[2] LS_0 and LS_1 = V_{IH} or V_{IL}

[3] $\overline{OE}$, $\overline{W}$, WLH, RLH, WLJ, RLJ = don't care.

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APPLICATION EXAMPLES

Delay Line

The synchronous mode may be used to create a full-field delay line with a fixed length (figures 6 and 7). Useful video applications include field interpolation, interframe noise reduction, and separation of luminance (Y) and chrominance (C) signals. In these applications, field buffer size is determined by the logic levels applied to pins LS_0 - LS_1 and BS_0 - BS_3. The former allows variation of the number of lines from 260 to 263, while the latter controls the actual line length at 896 to 910 bits for the last line. The actual delay between data being written into D_{IN} and read on D_{OUT} is controlled by the WCK clock period and the con figured size of the buffer.

Frame Synchronization or Time Base Correction

The μPD42270 has the capability of executing asyn chronous write and read cycles by independently clocking WCK and RCK, respectively. The feature is useful in applications requiring frame synchronization, time base correction or buffering, where WCK, RCK, $\overline{WCLR}$ and $\overline{RCLR}$ may all have variable time periods. In addition, the write carry out (WCO) and read carry out (RCO) options give a positive indication when the bit pointer reaches the end of the line.

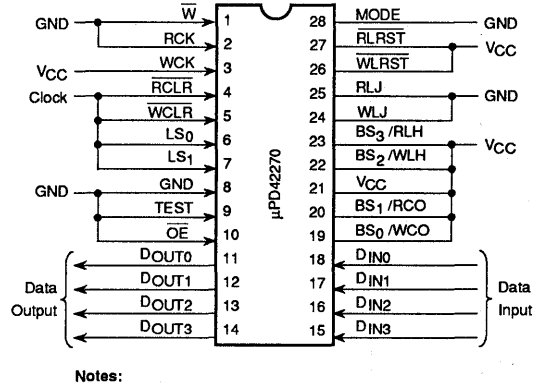
Vertical or Horizontal Image Compression and Expansion

Vertical compression and expansion of the video image may be accomplished by means of the line jump or line hold functions. Compression occurs when WLJ or RLJ are used to jump over lines that are not to be displayed. Expansion occurs when the WLH or RLH line hold signals are used to display a line multiple times.

Horizontal compression and expansion can be achieved by modifying the cycle time of the WCK and RCK clocks, and by using the $\overline{WLRST}$ and $\overline{RLRST}$ line reset signals.

18c

Figure 6. Example of Delay Line



Notes:

(1) $\overline{W}$, $\overline{OE}$, MODE, WLJ, and RLH = V_{IL}.

(2) BS_0 – BS_3, LS_0 – LS_1, $\overline{WCLR}$, and $\overline{WLRST}$ = V_{IH}.

(3) RCK, RCLR, and RLRST = don't care.

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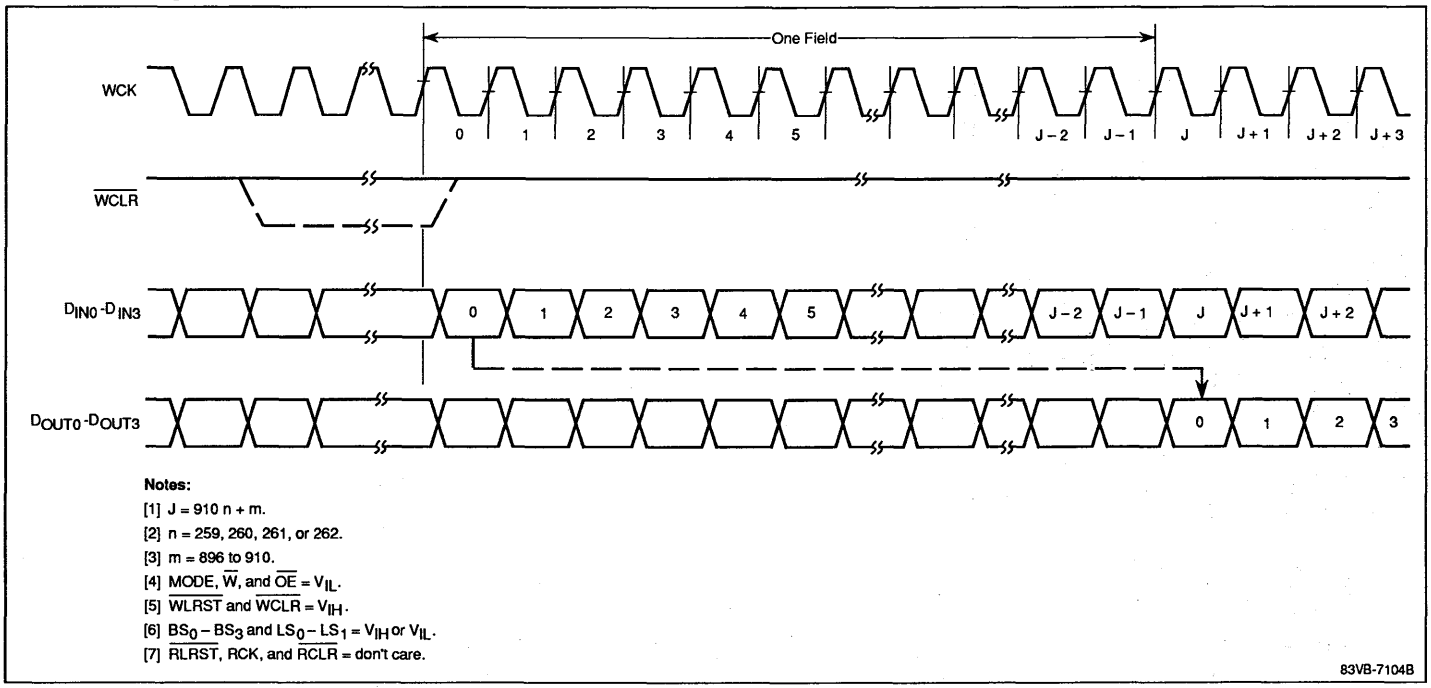
Figure 7. Delay Line Timing



Notes:

[1] J = 910 n + m.

[2] n = 259, 260, 261, or 262.

[3] m = 896 to 910.

[4] MODE, $\overline{W}$, and $\overline{OE}$ = V_{IL}.

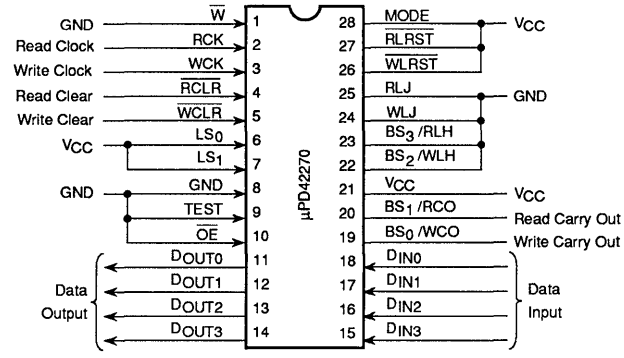
[5] $\overline{WLRST}$ and $\overline{WCLR}$ = V_{IH}.

[6] $BS_0 - BS_3$ and $LS_0 - LS_1$ = V_{IH} or V_{IL}.

[7] $\overline{RLRST}$, RCK, and $\overline{RCLR}$ = don't care.

83VB-7104B

Figure 8. Example of Frame Synchronization/Time Base Correction



Notes:
(1) $\overline{W}$, $\overline{OE}$, WLJ, RLJ, WLH, and RLH = V_{IL}.
(2) LS_0–LS_1, MODE, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.

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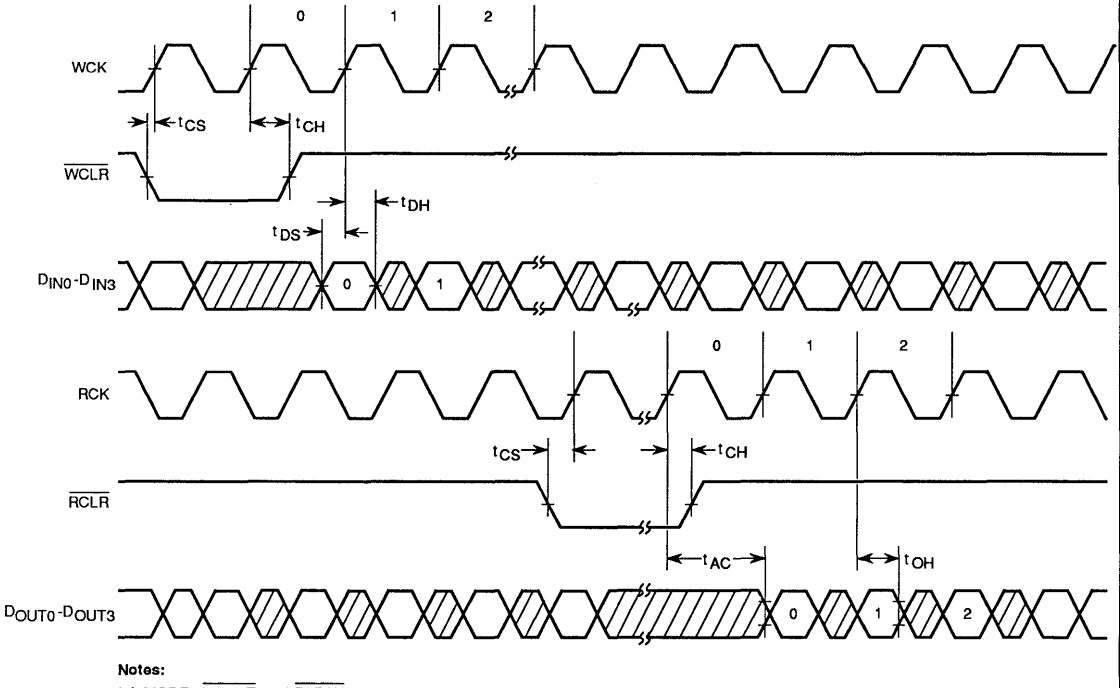
Figure 9. Asynchronous Read/Write Timing for Frame Synchronization or Time Base Correction



Notes:
[1] MODE, $\overline{WLRST}$, and $\overline{RLRST}$ = V_{IH}.
[2] $\overline{W}$ and $\overline{OE}$ = V_{IL}.
[3] LS_0 and LS_1 = V_{IH} or V_{IL}.
[4] WLH, RLH, RLJ, and WLJ = V_{IL}.

83VB-7106B

μPD42271, 42272
Picture-in-Picture Generator

October 1991

Description

The μPD4227x (42271 and 42272) is a picture-in-picture generator designed for use in NTSC and PAL broadcasting systems. Picture-in-picture describes the device's ability to combine multiple video signals into a single signal for display on a television monitor, for input to a VCR, or for use in any manner that a single video signal is used. The format may be selected so that one primary picture is displayed over the entire picture area. The other subpicture(s) can then be superimposed onto the primary one to allow multiple picture sources to be viewed simultaneously.

The picture-in-picture generator is available in two versions. The μPD42272 is the full-featured version that can display a border in one of four colors around the subpicture. The μPD42271 has exactly the same features except that it is not able to display a border around the subpicture.

The μPD4227x has an onboard controller, field storage, buffer storage, two line buffers, and two oscillators. The controller sets the timing, performs vertical filtering, and stores and retrieves subpicture signal(s) for insertion into the primary picture signal. A line of the subpicture signal is placed in buffer storage before being written into field storage, which contains that portion of the signal to be displayed. The line buffers store a weighted average of three lines of the subpicture signal to provide vertical filtering, while the onboard oscillators facilitate interfacing to the μPD4227x.

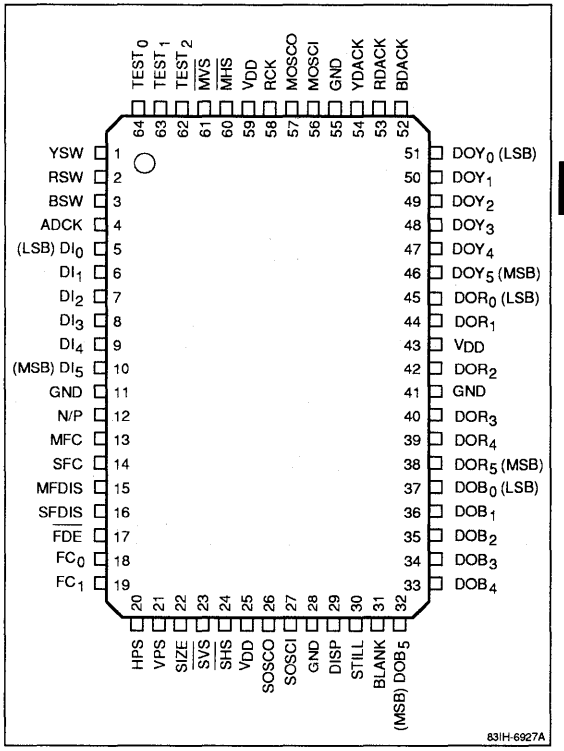
The level of integration provided by the μPD4227x means that picture-in-picture can be achieved more quickly and easily than with standard video buffers and control circuitry.

Ordering Information

Part Number	Subpicture Frame Border	Package
μPD42271AGF-3BE	No	64-pin plastic quad flatpack
μPD42272AGF-3BE	Yes	

Pin Configuration

64-Pin Plastic QFP



Features

- NTSC and PAL compatibility
- Built-in vertical filter
- Selectable subpicture display size
- 134,676-bit field buffer and two line buffers
- Built-in input and output oscillators
- Four selectable screen positions
- Four-color selection of subpicture frame border (μPD42272 only)
- Selectable freeze-frame display
- Automatic self-refreshing
- 6-bit resolution of Y, R-Y and B-Y signals
- Low power consumption of 75 mA max
- CMOS silicon-gate fabrication process
- Three-state outputs; TTL-compatible I/O
- Single + 5-volt power supply

Absolute Maximum Ratings

T_A = 25°C

Pin voltage, V_T	−0.1 to V_{DD} + 0.5 V
Supply voltage, V_{DD}	−0.1 to +7.0 V
Output current, I_O	50 mA
Operating temperature, T_{OPT}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Table 1. Description of Features

Feature	Description
Field memory capacity	7,568 words by 8 bits (86 x 88)
Quantization	6 bits
Frame colors	White, yellow, light blue, green (μPD42272 only)
Screen positions	Top left, bottom left, top right, bottom right
Field-to-field line offset sampling processing	Adjusts the starting location of the first line of a field to increase vertical resolution
Line array correction	Adjusts lines between even and odd fields
Display ON/OFF switching	Allows insertion or removal of subpicture
Still picture display	Freezes the subpicture display

Table 2. Subpicture Display Area

Video Standard	Full Screen Display (1/9)	80% Screen Display (1/12)
NTSC	49.3 μs x 74 lines	41.3 μs x 62 lines
PAL	49.3 μs x 87 lines	41.3 μs x 73 lines

Table 3. Sampling Rate

Signal	Input	Output
Y	3 MHz	9 MHz
R–Y	0.75 MHz	2.25 MHz
B–Y	0.75 MHz	2.25 MHz

Table 4. Sampling Sequence

—(Y)—(R–Y)—(Y)—(–)—(Y)—(B–Y)—(Y)—(–)—

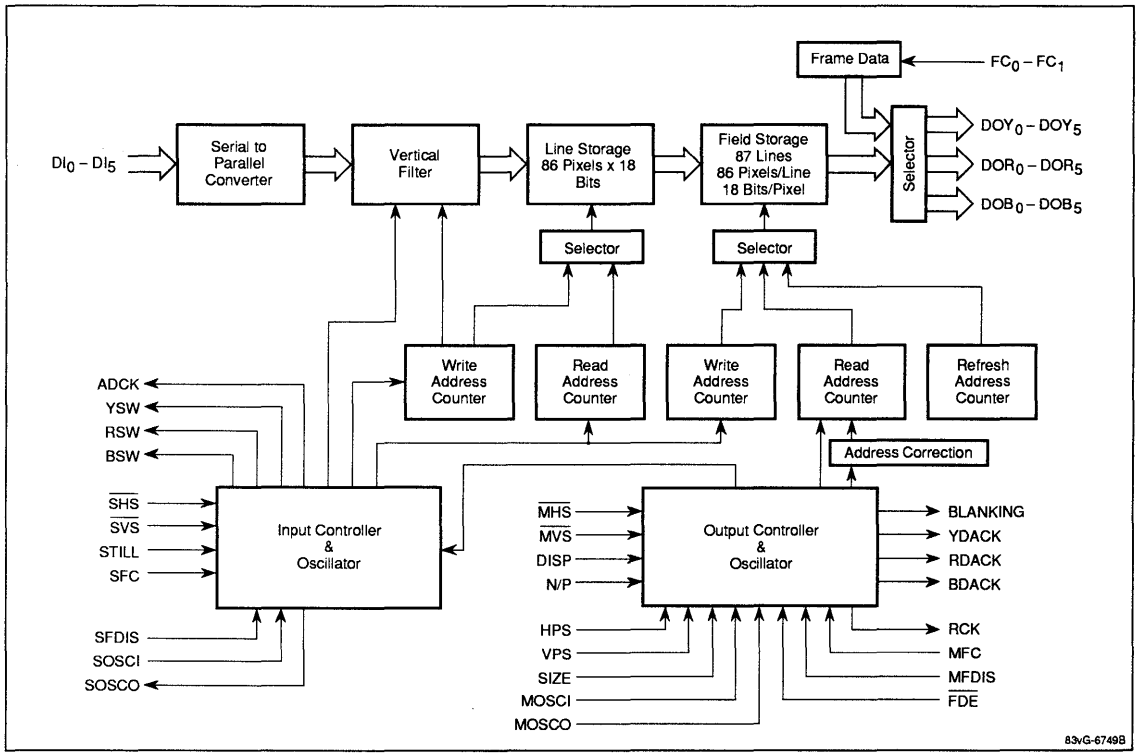
Table 5. Average Vertical Filtering

Line Number	Coefficient
n − 1	1/4
n	1/2
n + 1	1/4

Notes:

(1) n = line to be sampled.

Block Diagram



Pin Identification

Symbol	Function
ADCK	Analog/digital clock output
BDACK	Digital/analog clock for B-Y component signal output
BLANK	Main picture blanking output
BSW	DI_0 - DI_5 output enable for B-Y component signals
DI_0 - DI_5	Multiplexed B-Y, R-Y, and Y data inputs
DISP	Subpicture on/off input
DOB_0 - DOB_5	B-Y data outputs
DOR_0 - DOY_5	R-Y data outputs
DOY_0 - DOY_5	Y data outputs
FC_0 and FC_1	Frame color selection input
$\overline{FDE}$	Field distinction data enable input
HPS	Horizontal position input
MFC	Main picture field correction input
MFDIS	Main picture field distinction input
$\overline{MHS}$	Main picture horizontal synchronous input
MOSCI	Main picture oscillator input
MOSCO	Main picture oscillator output
$\overline{MVS}$	Main picture vertical synchronous input
$N/\overline{P}$	NTSC/PAL switching input
RCK	Read clock output
RDACK	Digital/analog clock for R-Y component signal output
RSW	DI_0 - DI_5 output enable for R-Y component signals
SFC	Subpicture field correction input
SFDIS	Subpicture field distinction input
$\overline{SHS}$	Subpicture horizontal synchronous input
SIZE	Size selection input
SOSCI	Subpicture oscillator clock input
SOSCO	Subpicture oscillator clock output
STILL	Freeze frame input
$\overline{SVS}$	Subpicture vertical synchronous input
$TEST_0$ - $TEST_2$	Test terminals
VPS	Vertical position input
YDACK	Digital/analog clock for Y component signal output
YSW	DI_0 - DI_5 output enable for Y component signals
V_{DD}	+5-volt power supply
GND	Ground

Pin Functions

ADCK. Y, R-Y and B-Y component signals selected with the analog switch are converted from analog to digital data in synchronization with this 6 MHz sampling clock. Digitized component signals are sequentially input to the DI_0 - DI_5 pins, also in synchronization with this clock.

BDACK. Digitized B-Y component signals are output from the DOB_0 - DOB_5 pins in synchronization with this 2.25 MHz sampling clock.

BLANK. When high, this output signal blanks the main picture, enabling the subpicture to be displayed.

BSW. A high logic level on BSW (while RSW and YSW are low) enables the DI_0 - DI_5 pins to be used for receiving 6-bit B-Y data from the A/D converter.

DI_0 through DI_5. These multiplexed pins are used for 6-bit digitized subvideo input, either B-Y, R-Y or Y, depending on the levels of BSW, RSW and YSW. DI_0 is the least significant bit and DI_5 is the most significant bit.

DISP. This pin controls the BLANK signal. A high logic level enables BLANK, while DISP low inhibits it. The level of DISP has no effect on the DOB_0 - DOB_5, DOR_0 - DOR_5, and DOY_0 - DOY_5 pins.

DOB_0 through DOB_5. These pins are used for 6-bit B-Y color difference output and depend on the status of BDACK. When no B-Y data is being output, the pins are in high impedance.

DOR_0 through DOR_5. These pins are used for 6-bit R-Y color difference output and depend on the status of RDACK. When no R-Y data is being output, the pins are in high impedance.

DOY_0 through DOY_5. These pins are used for 6-bit Y luminance output and depend on the status of YDACK. When no Y data is being output, the pins are in high impedance.

FC_0 and FC_1. The combination of signals from these pins is used to specify subvideo frame color, as shown below:

Pin	White	Light Blue	Yellow	Green
FC_0	high	low	high	low
FC_1	high	high	low	low

FDE. This pin is used to select external or internal field distinction. FDE high enables external field distinction, while FDE low inhibits the MFDIS and SFDIS pins and causes field distinction to be executed internally.

HPS and VPS. These horizontal and vertical input pins specify positioning of the subpicture. One of the four corners on the main picture can be selected by combining the input levels on HPS and VPS, as shown below.

Pin	Top Left	Bottom Left	Top Right	Bottom Right
HPS	high	high	low	low
VPS	high	low	high	low

MFC. Fields of the main picture are distinguished by the μPD4227x based on the phase relationship of the $\overline{MHS}$ and $\overline{MVS}$ signals. Field distinction may therefore be distorted if the signals are not in proper phase. In these cases, a high logic level on MFC can be used to reverse field distinction. MFC low has no effect on field distinction.

MFDIS. The even and odd fields of the main picture signal are distinguished based on the phase relationship of $\overline{MHS}$ and $\overline{MVS}$. MFDIS can be used to provide an external signal indicating either an odd (high) or even (low) field.

$\overline{MHS}$. This pin is used to input a horizontal synchronization signal for the main picture. The internal read clock oscillator is synchronized to the rising edge of $\overline{MHS}$ and increments the field buffer's read address counter, which is used to determine the horizontal display size and position of the sub picture.

MOSCI. This pin is used as an oscillator input for the main picture read clock. To use the internal oscillator, an external coil and capacitor must be installed. Alternatively, an 18 MHz external clock may be input to MOSCI.

MOSCO. This pin is used as an output for the feedback circuit of the main picture's internal oscillator.

$\overline{MVS}$. This pin is used to input a vertical synchronization signal for the main picture. The falling edge of $\overline{MVS}$ resets the field buffer's internal read address counter, which is used to determine the vertical display size and position of the subpicture.

N/$\overline{P}$. A high logic level on this pin selects NTSC compatibility and a low selects PAL.

RCK. This pin is used as an output for the subpicture read clock, which is derived from MOSCI and MOSCO.

RDACK. Digital R-Y component signals are output from the DOR_0 - DOR_5 pins in synchronization with this 2.25 MHz sampling clock.

RSW. A high logic level on RSW (while BSW and YSW are low) enables the DI_0 - DI_5 pins to be used for receiving 6-bit R-Y data from the A/D converter.

SFC. The μPD4227x distinguishes subpicture fields based on the phase relationship of the $\overline{SHS}$ and $\overline{SVS}$ signals. Field distinction of the subpicture may therefore be distorted if the signals are not in phase. SFC high can be used to reverse field distinction. SFC low has no effect on field distinction.

SFDIS. The even and odd fields of the subpicture signal(s) are distinguished based on the phase relationship of the $\overline{SHS}$ and $\overline{SVS}$ signals. This pin can be used to provide an external signal indicating either an odd (high) or even (low) field.

$\overline{SHS}$. This pin is used to input the horizontal synchronization for the subpicture. The rising edge of this clock is used to synchronize the internal write clock oscillator which is then used to increment the write address counters for the line buffers and the field buffer.

SIZE. This input is used to specify size of the subpicture display area. SIZE high sets a full screen display and occupies 1/9 of the main picture. SIZE low displays 80% of the subpicture and occupies 1/12 of the main picture.

SOSCI. This pin is used as an oscillator input for the subpicture write clock. To use the internal oscillator, an external coil and capacitor must be installed. Alternatively, an 6 MHz external clock may be input to SOSCI.

SOSCO. This pin is used as an output for the feedback circuit of the subpicture's internal oscillator.

STILL. A high logic level selects a still picture, while STILL low selects a moving picture.

$\overline{SVS}$. This pin is used to input the vertical synchronization signal for the subpicture. The falling edge of this signal resets the internal write address counters for the line buffers and the field buffer.

$TEST_0$ - $TEST_2$. These are test pins and must be open.

YDACK. Digital Y component signals are output from the DOY_0 - DOY_5 pins in synchronization with this 9 MHz sampling clock.

YSW. A high logic level on YSW (while BSW and RSW are low) enables the DI_0 - DI_5 pins to be used for receiving 6-bit Y data from the A/D converter.

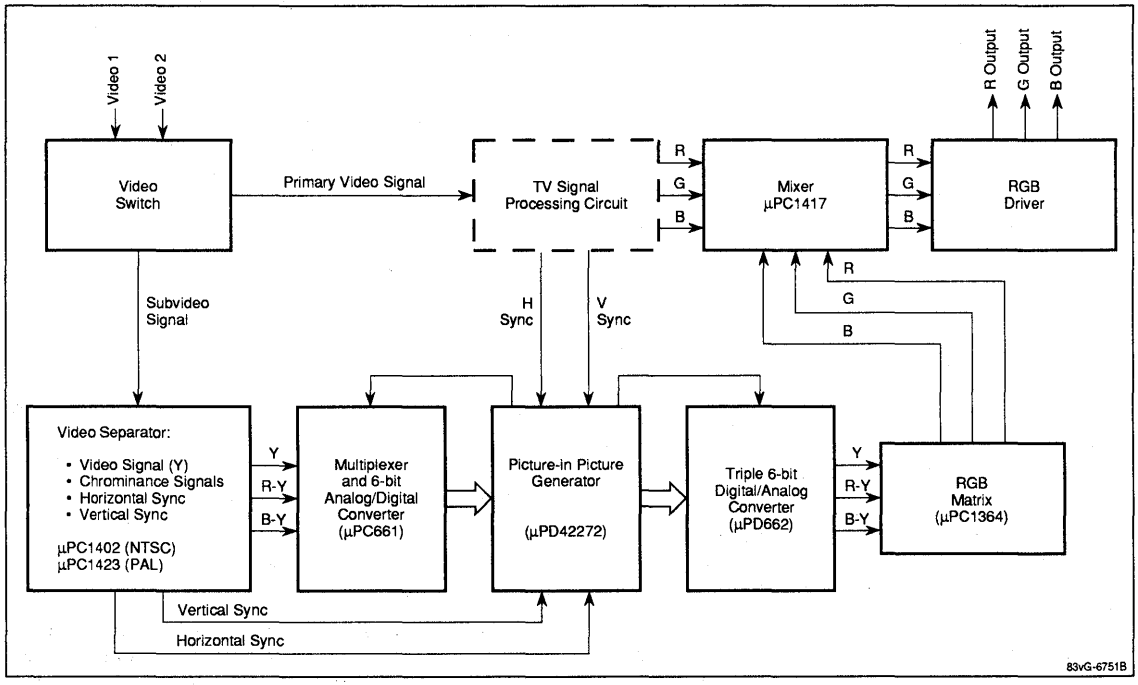
Application

The following block diagram illustrates one application for the μPD4227x in an NTSC television system.

The video signals for the subpicture are separated into Y, B-Y, and R-Y component signals and horizontal and vertical synchronization signals by the μPC1402 decoder. The Y, B-Y, and R-Y component signals are input in parallel to the μPC661 A/D converter, after which they are switched to the sequence Y, R-Y, Y, -, Y, B-Y, Y, - using time-division multiplexing and converted to digital signals. In this instance, timing for the Y, R-Y, and B-Y conversion process is regulated by the μPD4227x.

After the μPD4227x receives the 6-bit digital data output by the μPC661, it compresses the subpicture data and stores one field. The output signals are sent by the μPD4227x to the μPC662, which contains three D/A converters assigned respectively to the Y, R-Y, and B-Y signals. If the analog component signals output by the D/A converters are to be used by the TV, they then are converted to an RGB signal by the μPC1364 matrix circuit. If they are to be used by the VCR, they are combined with the main picture signal after being converted into composite signals in the encoder circuit.

Application Example



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	V_{DD}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{DD} + 0.5	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Input oscillation frequency	$f_{OSC\ IN}$		6		MHz	
Output oscilllation frequency	$f_{OSC\ OUT}$		18		MHz	
Horizontal synchronizing pulse width	f_{HSYNC}		4.8		μs	$\overline{SHS}$ and $\overline{MHS}$ pins
Ambient temperature	T_A	−20		70	°C	

DC Characteristics

T_A = −20 to +70°C; V_{DD} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Supply current	I_{DD}			75	mA	$f_{OSC\ IN}$ = 6 MHz; $f_{OSC\ OUT}$ = 18 MHz
Input leakage current	I_I	−10		10	μA	V_{IN} = 0 V to V_{DD}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	Outputs disabled; V_{OUT} = 0 V to V_{DD}
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			5	pF	All inputs except SOSCI and MOSCI
Output capacitance	C_O			7	pF	All outputs except SOSCO and MOSCO
Oscillator input capacitance	C_{SOSCI}		8		pF	SOSCI
	C_{MOSCI}		10		pF	MOSCI
	C_{SOSCO}		8		pF	SOSCO
	C_{MOSCO}		10		pF	MOSCO

AC Characteristics

T_A = −20 to +70°C; V_{DD} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
ADCK pulse width, low	t_{ADL}	70			ns	
ADCK pulse width, high	t_{ADH}	70			ns	
YDACK pulse width, low	t_{YDAL}	50			ns	
YDACK pulse width, high	t_{YDAH}	50			ns	
RDACK pulse width, low	t_{RDAL}	200			ns	(Note 7)
RDACK pulse width, high	t_{RDAH}	200			ns	(Note 7)
BDACK pulse width, low	t_{BDAL}	200			ns	(Note 7)
BDACK pulse width, high	t_{BDAH}	200			ns	(Note 7)
RCK pulse width, low	t_{RCKL}	25			ns	
RCK pulse width, high	t_{RCKH}	25			ns	
Data input setup time	t_{DS}	25			ns	
Data input hold time	t_{DH}	30			ns	

AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Y data access time	t_{ACY}			5	ns	
Y data hold time	t_{OHY}	20			ns	
R–Y data access time	t_{ACR}			7(RCK) + 25	ns	
R–Y data hold time	t_{OHR}	20			ns	
B–Y data access time	t_{ACB}			7(RCK) + 25	ns	
B–Y data hold time	t_{OHB}	20			ns	
Output low impedance time	t_{LZ}	5		100	ns	(Note 4)
Output high impedance time	t_{HZ}	5		100	ns	(Note 4)
YSW, RSW, BSW low hold time from ADCK	t_{SW1}	5		30	ns	
YSW, RSW, BSW high hold time from ADCK	t_{SW2}	5		30	ns	
Rise and fall transition time	t_T	3		35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Ac measurements assume t_T = 5 ns.

(3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(4) t_{OFF} (max) defines the time at which the output becomes open-circuit and is not referenced to V_{OH} or V_{OL}.

(5) The input/output signal reference level is 1.5 V.

(6) $f_{OSC\ IN}$ equals 6 MHz; $f_{OSC\ OUT}$ is 18 MHz.

(7) The frame border output period is either 0.5 or 1.5 times as large as the standard value.

(8) $t_{LZ} \geq t_{HZ}$.

Figure 1. Input Timing

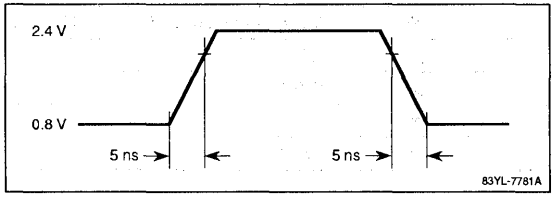


Figure 2. Output Timing

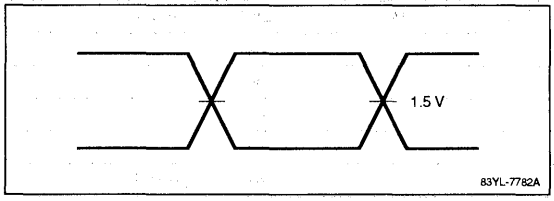


Figure 3. Output Load

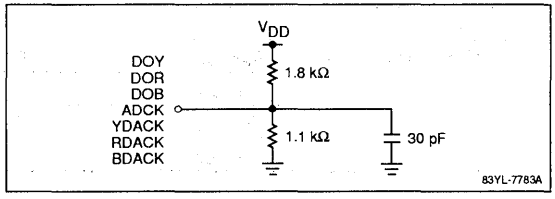
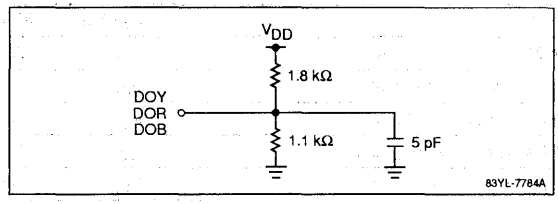


Figure 4. Output Load (t_{LZ} and t_{HZ})



Description

Serial/Parallel Converter (S → P). Converts the serially input 6-bit Y, R–Y, and B–Y subpicture signals into 18-bit parallel Y • R–Y • Y or Y • B–Y • Y signals, and then outputs them.

Vertical Filter. Executes averaging cycles and consists of two sets of line memory and an arithmetic circuit. If any one of the three lines is extracted to compress the screen vertically, the lines may become distorted on the screen. By averaging the data of the appropriate line with the preceding and succeeding lines, the filter prevents distortion.

Buffer Memory. Stores subpicture signals input during read operation and has a one-line capacity of 86 words by 18 bits.

Field Memory. Stores one 7,568-word by 18-bit field of a subpicture. Data is written into field memory when no subpicture is being displayed.

Buffer Memory Write Address Counter. Supplies write addresses to the buffer memory.

Buffer Memory Read Address Counter. Supplies read addresses to buffer memory in synchronization with the field memory write address counter and remains in standby during a field memory read cycle.

Buffer Memory Address Selector. Alternately outputs write and read addresses to buffer memory.

Field Memory Write Address Counter. Supplies write addresses to field memory and consists of horizontal and vertical address counters, the former of which is synchronized with the buffer memory read address counter. The counter remains in standby during a memory read cycle. When the address reaches its maximum value, the counter stops counting.

Field Memory Read Address Counter. Supplies read addresses to field memory and consists of horizontal and vertical address counters. Data read from field memory always takes priority over data written to it. Thus, the counter never enters standby in normal operation. When the address reaches its maximum value, the counter stops counting.

Refresh Address Counter. Supplies refresh addresses to field memory. When write/read operation to field memory terminates, this counter refreshes the memory location corresponding to its current value. The 6 MHz input clock is frequency-divided and supplied to the counter. It remains in standby while data is being read from or written into field memory. When the address reaches its maximum value, this counter stops counting and the address returns to the initial address.

Field Memory Address Selector. Alternately supplies the write, read, and refresh addresses.

Output Data Selector. Switches the subpicture signal read from field memory with the frame color signal selected by FC_0 and FC_1 and outputs the signal. This selector also concurrently executes parallel/serial conversion (12 bits → 6 bits) of the Y subpicture signal.

Input Controller and Oscillator. Controls the subpicture signal until it is written into field memory. This circuit oscillates the 6 MHz input clock synchronously with $\overline{SHS}$. Using this clock as the reference, the circuit controls vertical filtering, i.e., buffer memory write/read operation, and field memory write operation. This circuit also generates the ADCK, YSW, RSW, and BSW control signals transmitted to the 6-bit A/D converter.

Output Controller and Oscillator. Controls the subpicture signal during the time in which the signal is read and then output from field memory. This circuit oscillates the 18 MHz output clock synchronously with $\overline{MHS}$. Using this clock as the reference, the circuit controls field memory read operation and the data selector, and also generates the YDACK, RDACK and BDACK control signals transmitted to the 6-bit D/A converter. The BLANK and RCK signals are also generated by this circuit.

OPERATION

Writing the Subpicture Signals

Subpicture signals are converted by the 6-bit μPC661 A/D converter into digital data, and then input from DI. At this time, the subpicture signals are sequentially switched with the YSW, RSW, and BSW data switching signals and serially sampled as shown in table 4.

The (–) data is not actually transferred. Subpicture signals are converted by the serial/parallel converter into 18-bit Y • R–Y • Y or Y • B–Y • Y data. They are then averaged by the vertical filter, whose configuration is shown in figure 5.

After being averaged by the vertical filter, the subpicture signals are extracted line by line from the three lines. They are then written into buffer memory. Once field memory read operation terminates, the subpicture signals are subsequently read from buffer memory and written into field memory at a rate of 1.5 MHz.

Two types of subpicture write areas, one for NTSC applications and the other for PAL, are shown in figures 6 and 7. The odd and even fields deviate by one line in the vertical write area to enable field-to-field line offset sampling and improve vertical resolution.

Figure 5. Vertical Filter Configuration

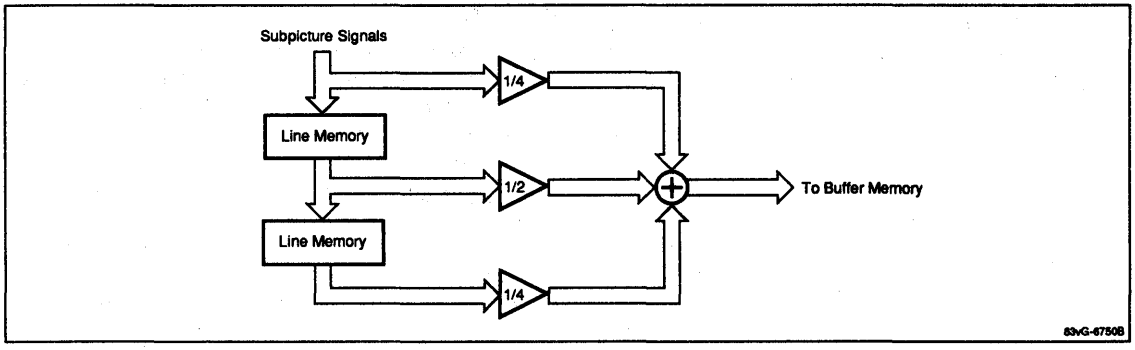
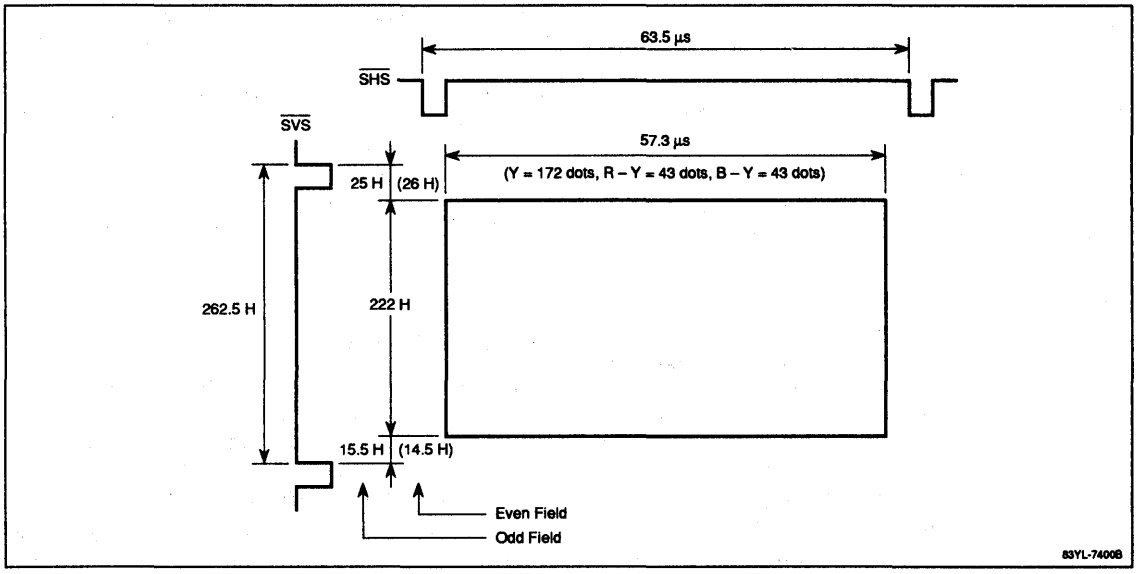


Figure 6. NTSC Subpicture Write Area



Reading the Subpicture Signals

After being written into field memory, subpicture signals are read synchronously with the signals from $\overline{MHS}$ and $\overline{MVS}$. Reading of subpicture signals is executed for all data written (the 4.5 MHz reading rate is three times as high as the writing rate). Subpicture signals then pass the selector and are output through DOY, DOR, and DOB. In addition to switching and outputting the subpicture and frame signals, the selector executes 12 to 6 bit, parallel to serial conversion of the Y signal.

The playback area is determined by the blanking signal and not by the write area. The display position is controlled by changing the timing of the read address counter according to the state of the HPS and VPS input pins. The playback area and display position vary with the NTSC/PAL method and screen size (full versus 80% full) as shown in figures 8 through 15. Any value in the display position includes the frame signal, which has a 220 ns (horizontal) x 1 line (vertical) area.

Figure 7. PAL Subpicture Write Area

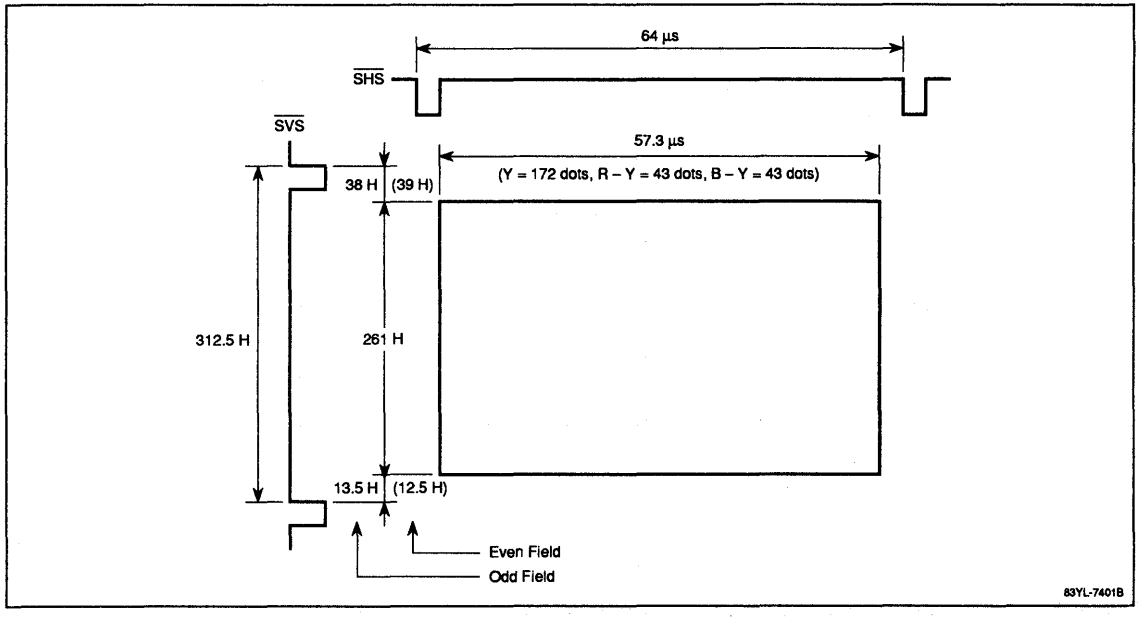
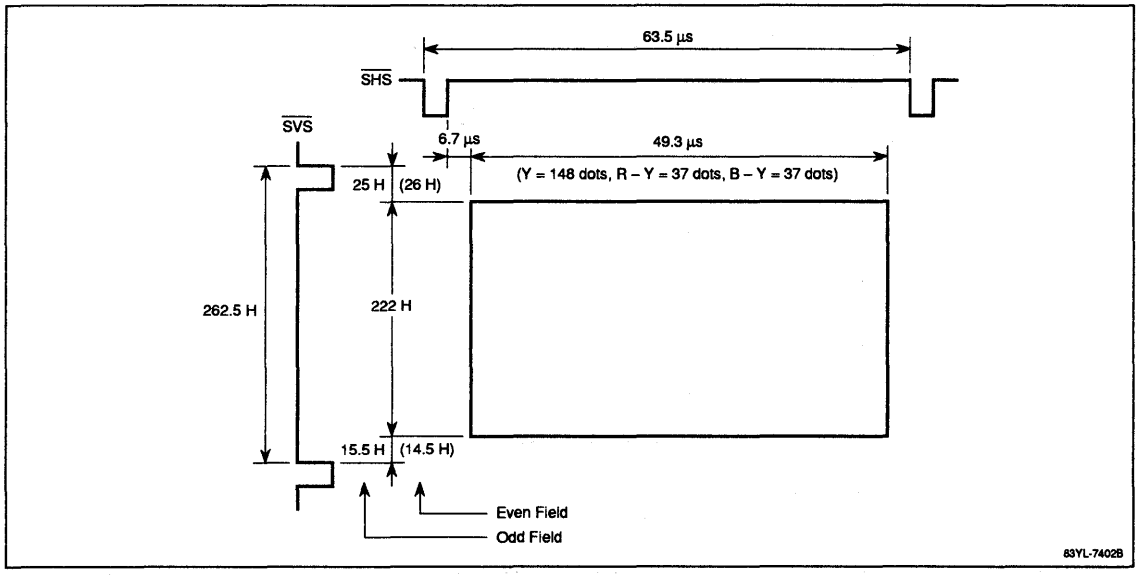


Figure 8. Subpicture Playback Area in NTSC Applications with Full Screen Display



18d

Figure 9. Subpicture Playback Area in NTSC Applications with 80% Screen Display

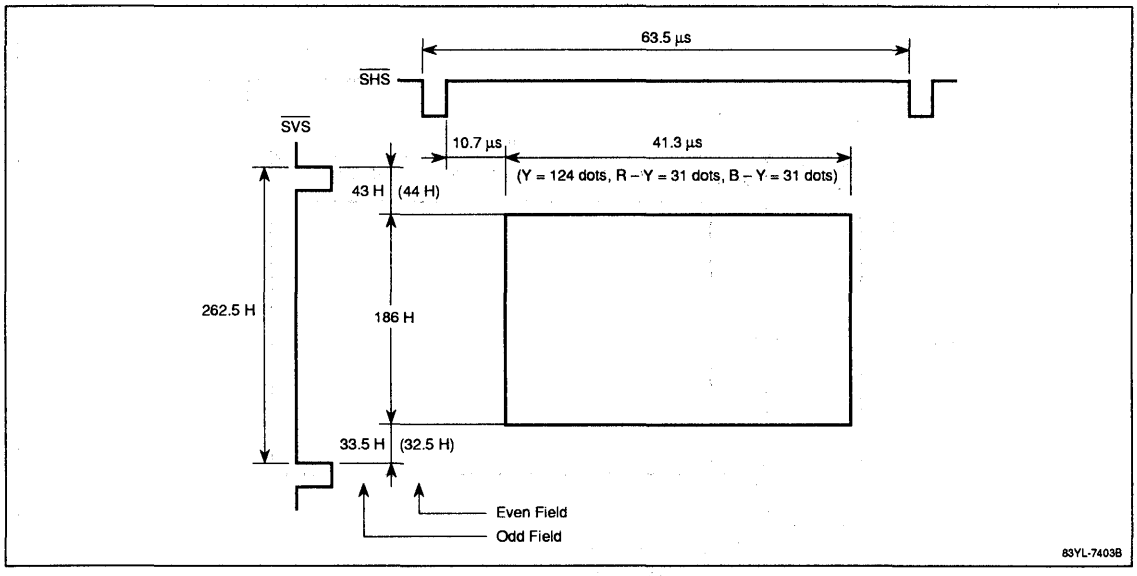


Figure 10. Subpicture Playback Area in PAL Applications with Full Screen Display

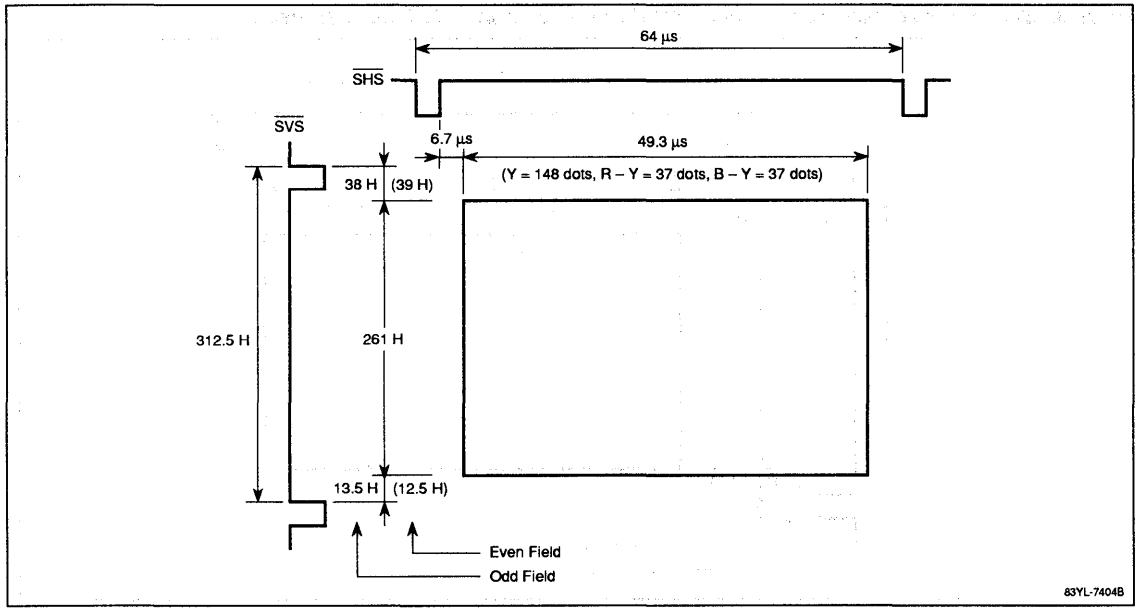


Figure 11. Subpicture Playback Area in PAL Applications with 80% Screen Display

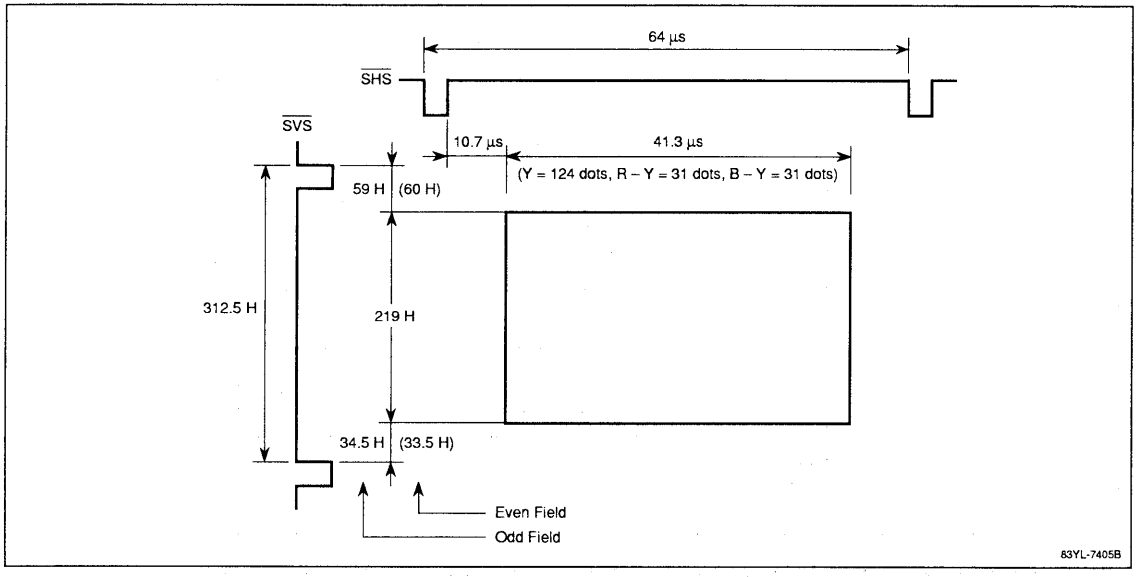
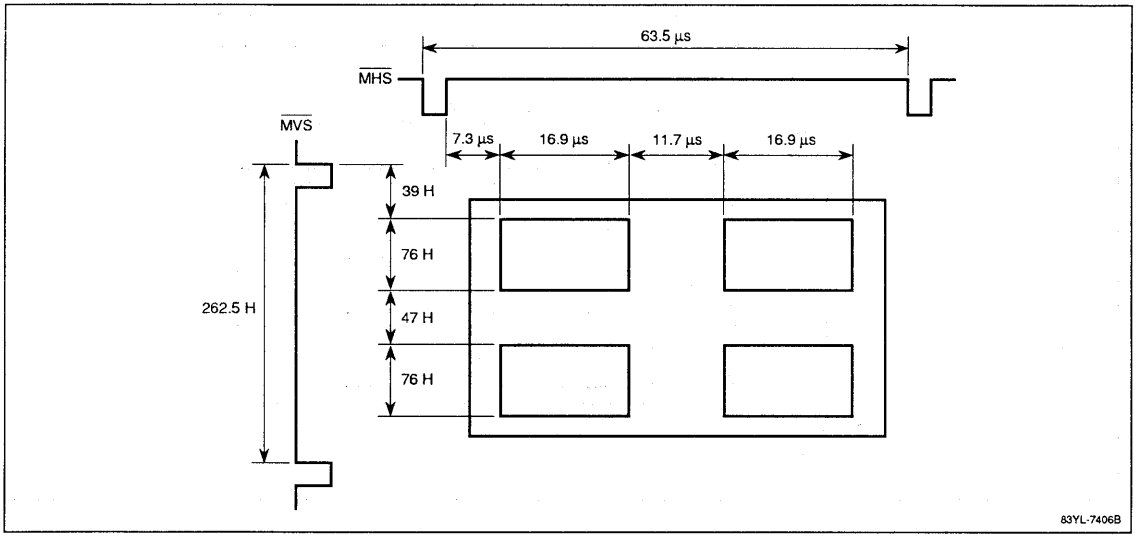


Figure 12. Subpicture Display Position in NTSC Applications with Full Screen Display



18d

Figure 13. Subpicture Display Position in NTSC Applications with 80% Screen Display

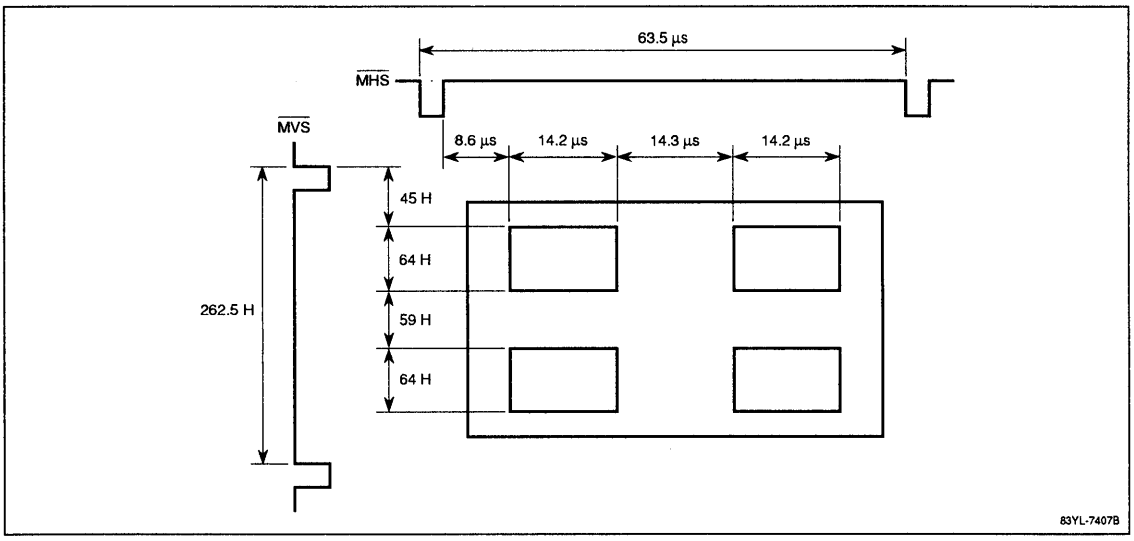


Figure 14. Subpicture Display Position in PAL Applications with Full Screen Display

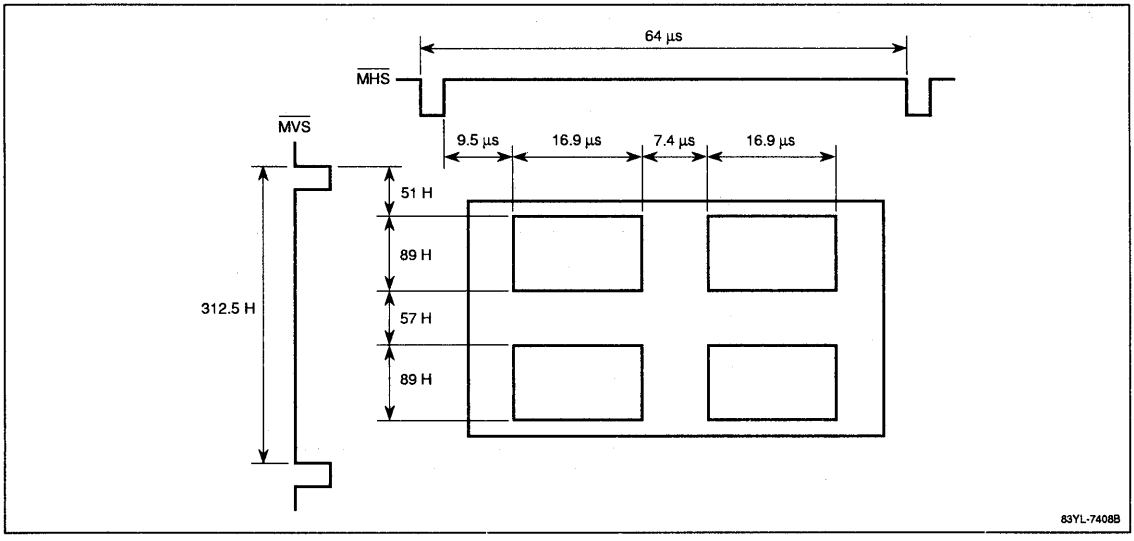
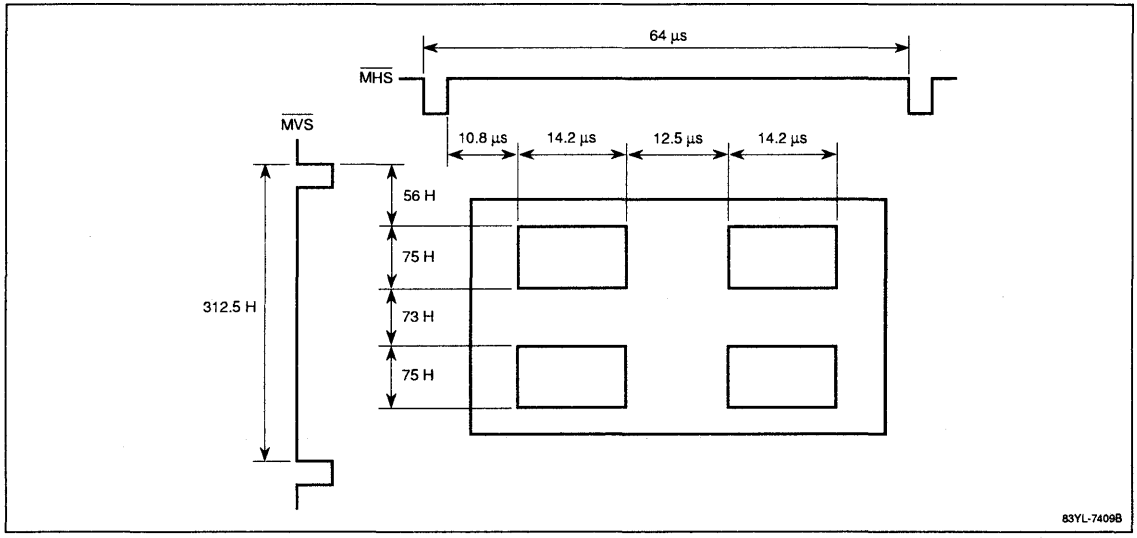


Figure 15. Subpicture Display Position with 80% Screen Display



Line Array Correction

Subpicture processing executes screen compression, in which the output data rate of the field memory is three times as high as the input data rate. A read cycle will catch up to, and then pass, a write cycle about midway on the screen. Afterward, old fields are read, and a field seam is produced where the two fields meet.

This problem is corrected during an old field read cycle by advancing the vertical address counter to its regular value and then incrementing it by one. The correction cycle varies depending on whether a main picture or subpicture field (odd versus even) field is involved (tables 6 and 7).

Table 6. Outrunning When the Main Picture and Subpicture Have the Same Fields

	Subpicture	
Main Picture	**Odd**	**Even**
Odd	— (before outrunning)	— (after outrunning)
Even	+1 (after outrunning)	— (before outrunning)

Notes:

(1) + = address counter is incremented to its normal value plus 1.

(2) — = no operation.

Table 7. Outrunning When the Main Picture and Subpicture Have Different Fields

	Subpicture	
Main Picture	**Odd**	**Even**
Odd	+1 (after outrunning)	— (before outrunning)
Even	+1 (before outrunning)	+1* (after outrunning)

Notes:

(1) + = address counter is incremented to its normal value plus 1.

(2) — = no operation.

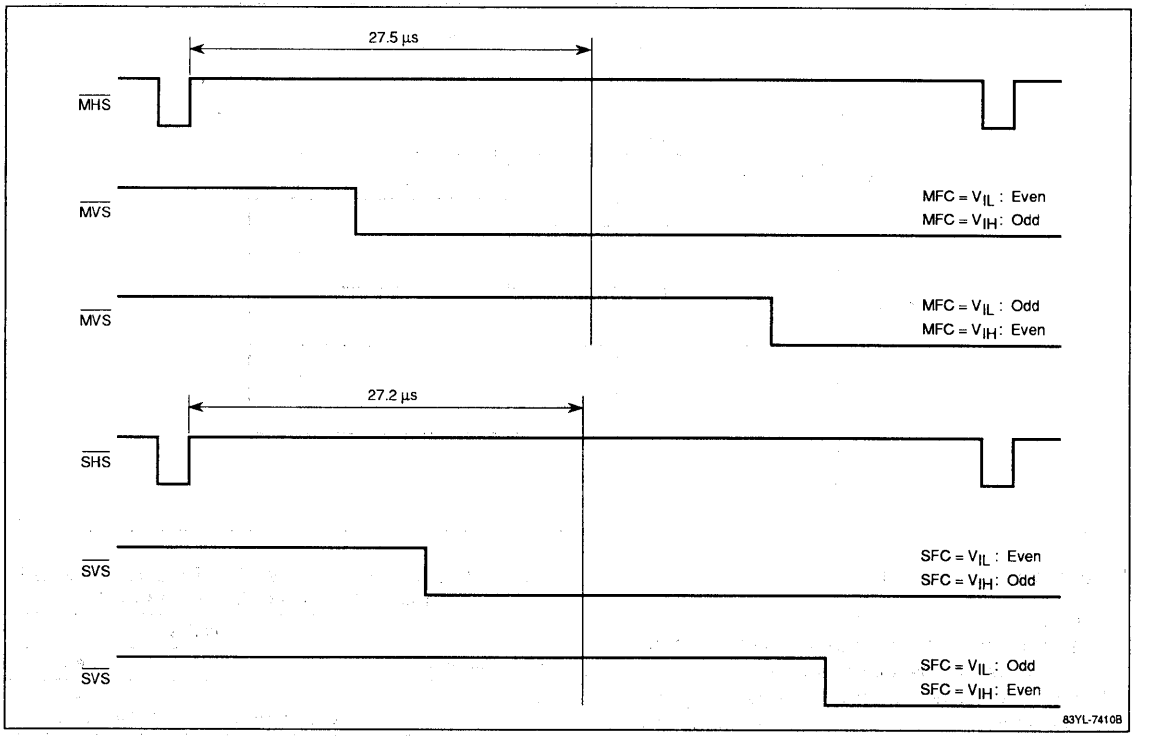
(3) * indicates that the address counter holds its status and is not incremented.

Field Distinction

The μPD4227x executes line offset sampling and line array correction. The former offsets write lines between the even and odd fields by one line. The latter advances the vertical read address counter to its normal value plus one by combining the main picture and subpicture fields. This prevents a seam line from appearing on the subpicture when part of it is displaying one field and the rest is displaying the other field.

In both cases, the μPD4227x executes field distinction to learn the status (odd or even) of the main picture and subpicture signals. The result is determined by the phase differences between $\overline{\text{MHS}}$/$\overline{\text{SHS}}$ and $\overline{\text{MVS}}$/$\overline{\text{SVS}}$ and by the state of MFC and SFC (figure 16).

Figure 16. Field Distinction



Frame Signal Generation

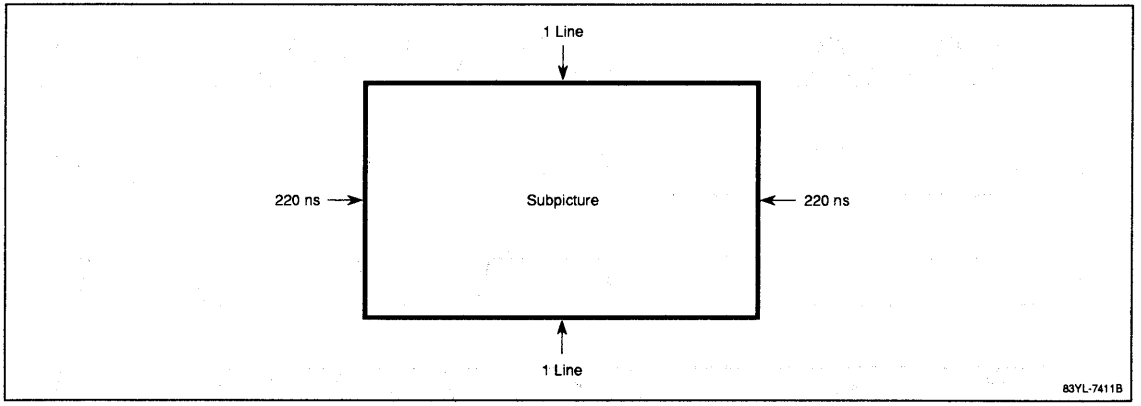
The μPD42272 contains the data for four colors: white, yellow, light blue, and green. These colors are used for frame signals and are selected by the FC_0 and FC_1 frame color selection input signals. The data selector switches the subpicture to the frame signal and then outputs it. The vertical width of the frame signal is one line; the horizontal width of 220 ns is determined by the YDACK, RDACK, and BDACK D/A clocks and the blanking signal (figure 17).

Table 8. Frame Signal Generation

	Signal																	
	Y						R–Y						B–Y					
Color	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0	DO_5	DO_4	DO_3	DO_2	DO_1	DO_0
White	1	0	1	0	1	1	1	0	0	0	0	0	1	0	0	0	0	0
Yellow	1	0	0	1	1	0	1	0	0	0	1	1	0	0	1	1	0	1
Light blue	0	1	1	1	1	0	0	0	1	1	0	1	1	0	0	1	1	1
Green	0	1	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1	1

The μPD4227x writes the Y, R–Y, B–Y subpicture signals serially using the μPC661, a six-bit A/D converter with analog switching. For read operation, the R–Y and B–Y signal sampling phases are reversed. For the output signals, there is a 180° phase difference between the R–Y and B–Y signals. Frame signals containing phase differences that are similarly output cause gradation because the frame signals deviate at the edges. To prevent this deviation, the μPD42272 aligns the edges of the frame signal by adjusting RDACK and BDACK during the frame signal output period (figure 18).

Figure 17. Frame Signal



Data Output

Subpicture signals are compressed to the scale of 1:9 (horizontal = 1:3 and vertical = 1:3) and then output through the DOY, DOR, and DOB output pins. The output period is about one-ninth of one field period of the main picture, or 16.7 ms. DOY, DOR, and DOB are in high impedance for the remaining eight-ninths of the period and no data is output (figure 19).

The signal level of the high impedance period must meet the pedestal level, i.e., the level of the initial input signal. The signal level is determined by resistors that pull up or down the DOY, DOR, and DOB pins. In the μPD4227x, the D/A converter clocks are output cyclically (every 2.25 MHz) during the no signal period. The μPD6901 six-bit D/A converter converts into analog data the data determined by pull-up or pull-down resistors, enabling the signal to be at a constant level.

The input signal pedestal level is determined at clamp levels of the μPC661 six-bit A/D converter. For the μPD661, the Y signal clamp output is the R–Y and B–Y output. All Y outputs are thus pulled down. For R–Y and B–Y output, only DOR_5 and DOB_5 are pulled up, respectively, and the other outputs are pulled down (figures 20 and 21).

Outside Control

Specified Frame Color. The μPD42272 can generate one of four frame colors (white, yellow, light blue, and green) depending on the levels of FC_0 and FC_1 (table 9).

Table 9. Frame Color Input Levels

Pin	White	Light Blue	Yellow	Green
FC0	H	L	H	L
FC1	H	H	L	L

Specified Subpicture Size. The μPD4227x can select one of two subpicture sizes using the SIZE subpicture selection input. When its input level is high, the display area is set to one-ninth of the main picture (full screen display). A low level sets the display area to one-twelfth, or 80%, of the main picture.

Specified Subpicture Position. The μPD4227x can select one of four subpicture display positions (one of the four corners on the main picture) using a combination of signals from the VPS and HPS position selection input pins (table 10).

Table 10. VPS and HPS Input Levels

Pin	Top Left	Bottom Left	Top Right	Bottom Right
VPS	H	L	H	L
HPS	H	H	L	L

Specified Still Picture. The μPD4227x can display a still subpicture using the still picture request input. When the level of STILL is high, a freeze frame picture is displayed. When the input level is low, the moving picture is selected.

Figure 18. Frame Signal Alignment

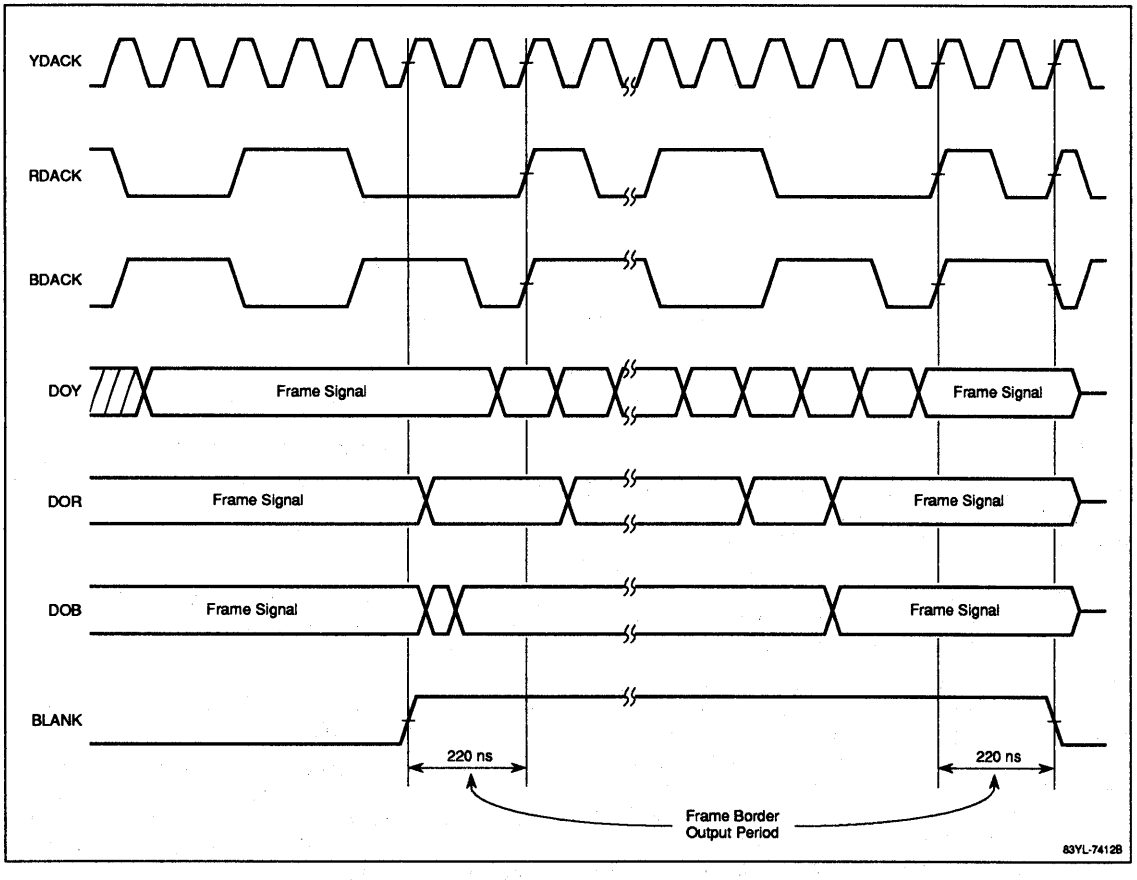


Figure 19. Subpicture Data Output

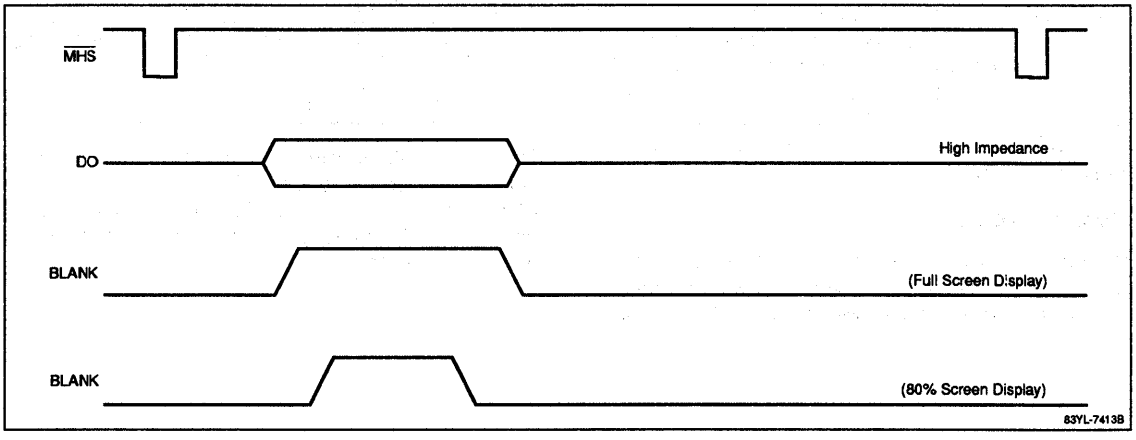


Figure 20. Data Output Signal Adjustment

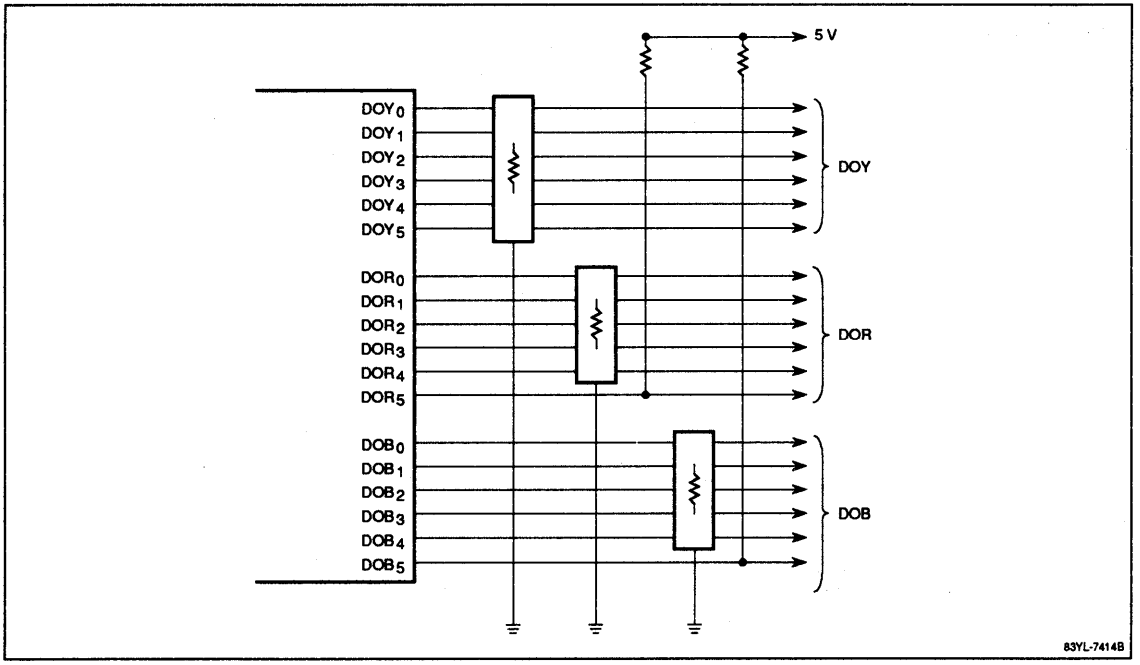
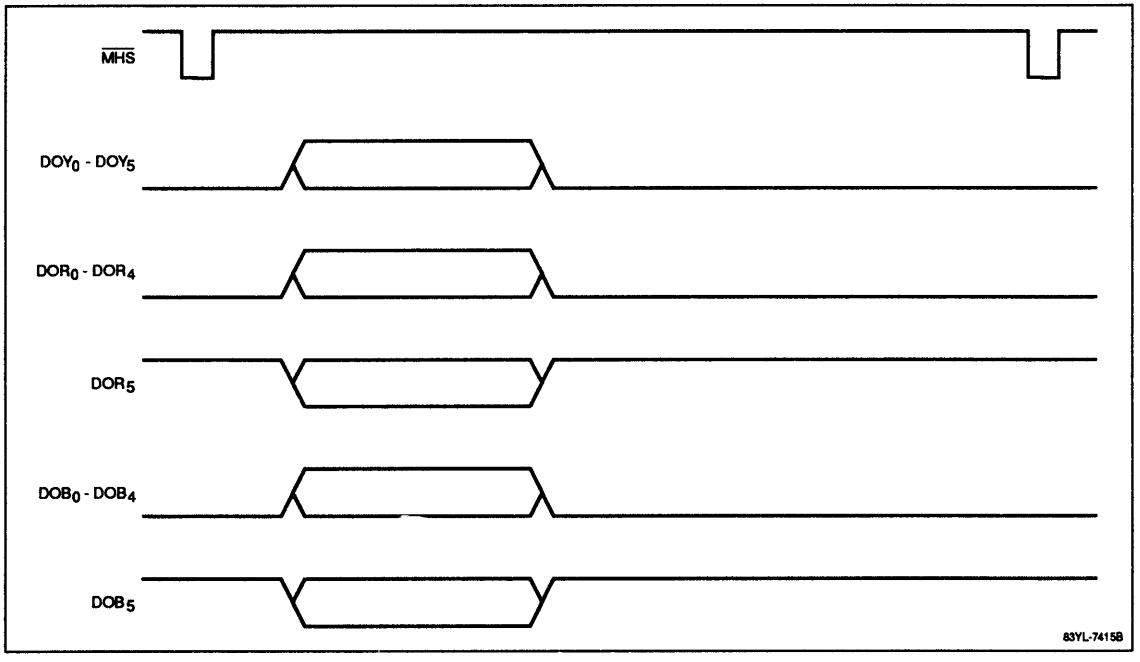
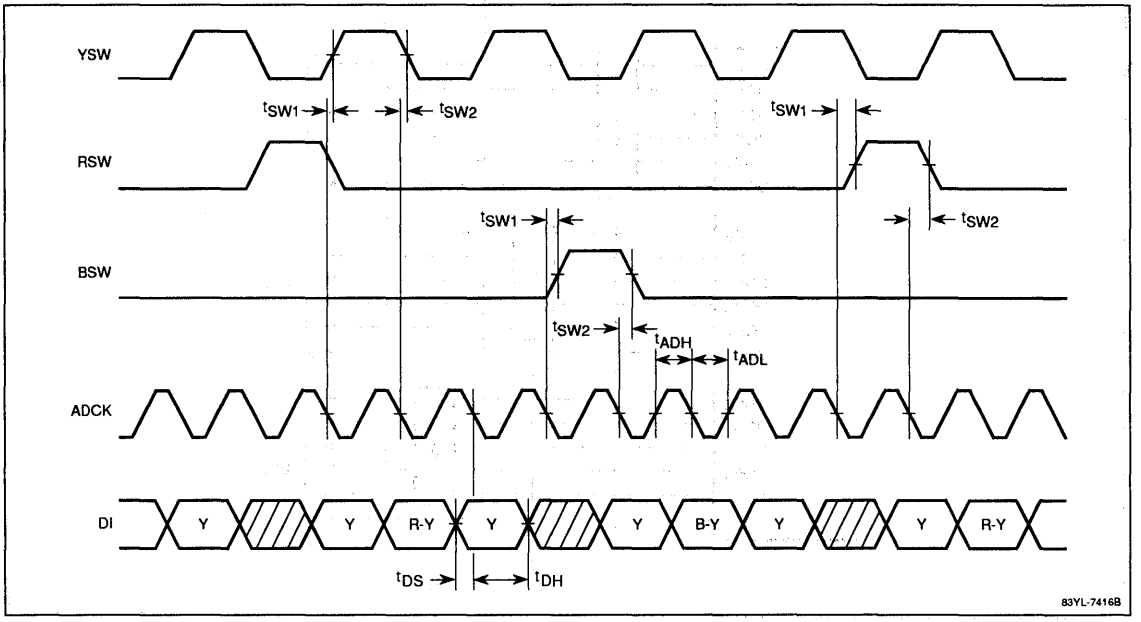


Figure 21. R–Y and B–Y Output Signal Adjustment



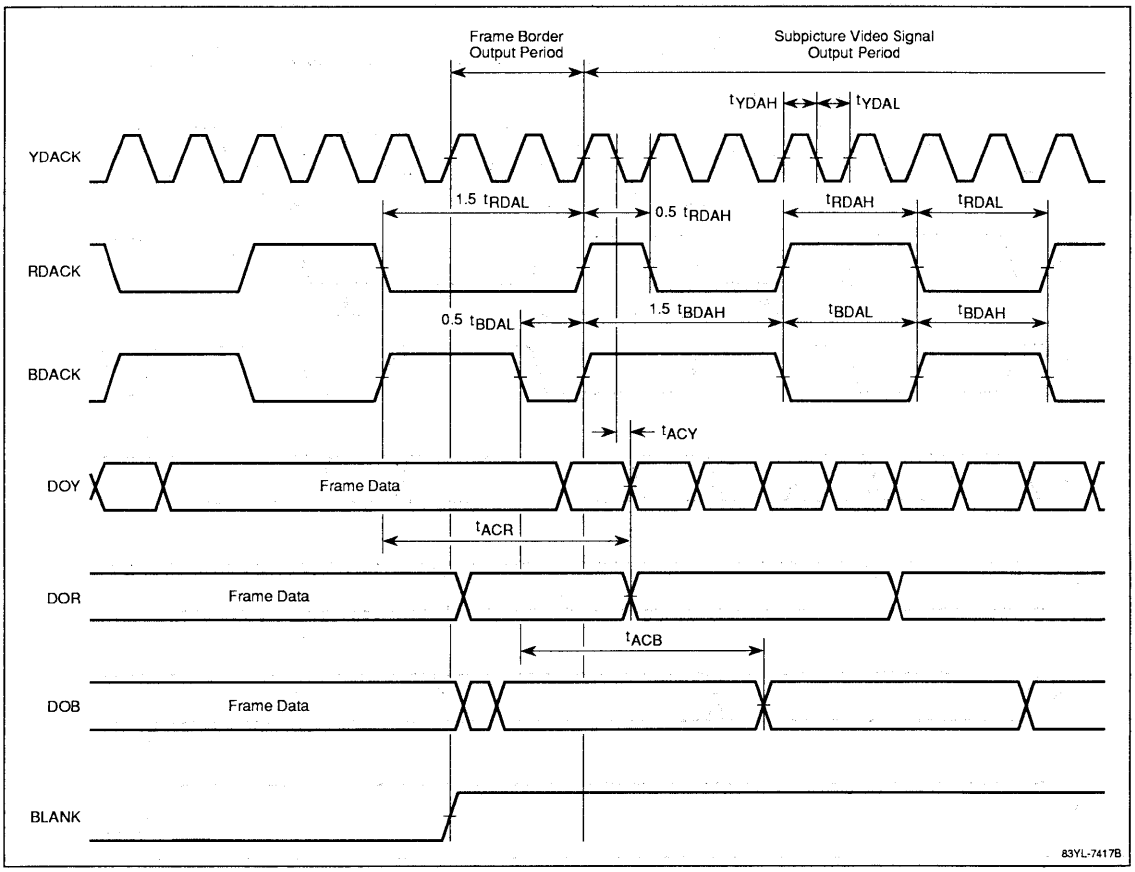
Timing Waveforms

Input Timing



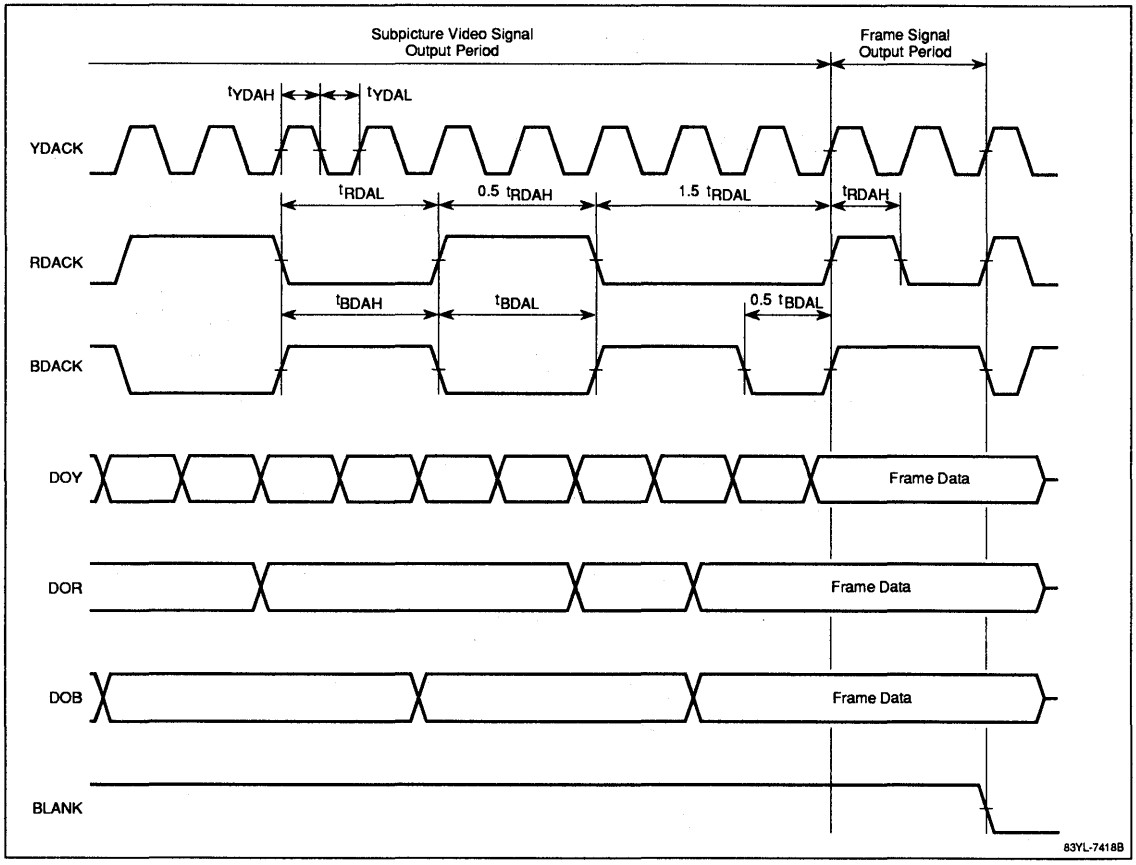
Timing Waveforms (cont)

Output Timing



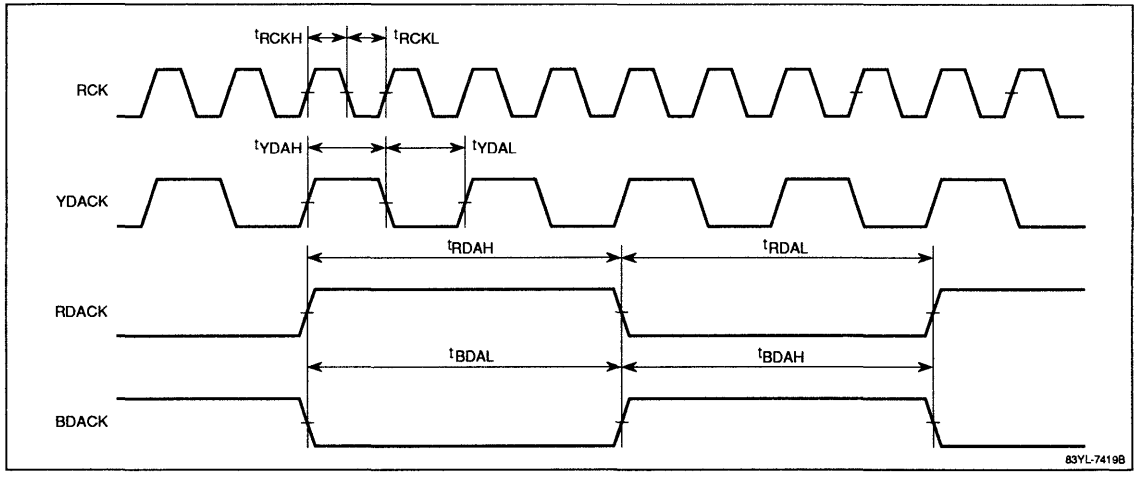
Timing Waveforms (cont)

Output Timing 2

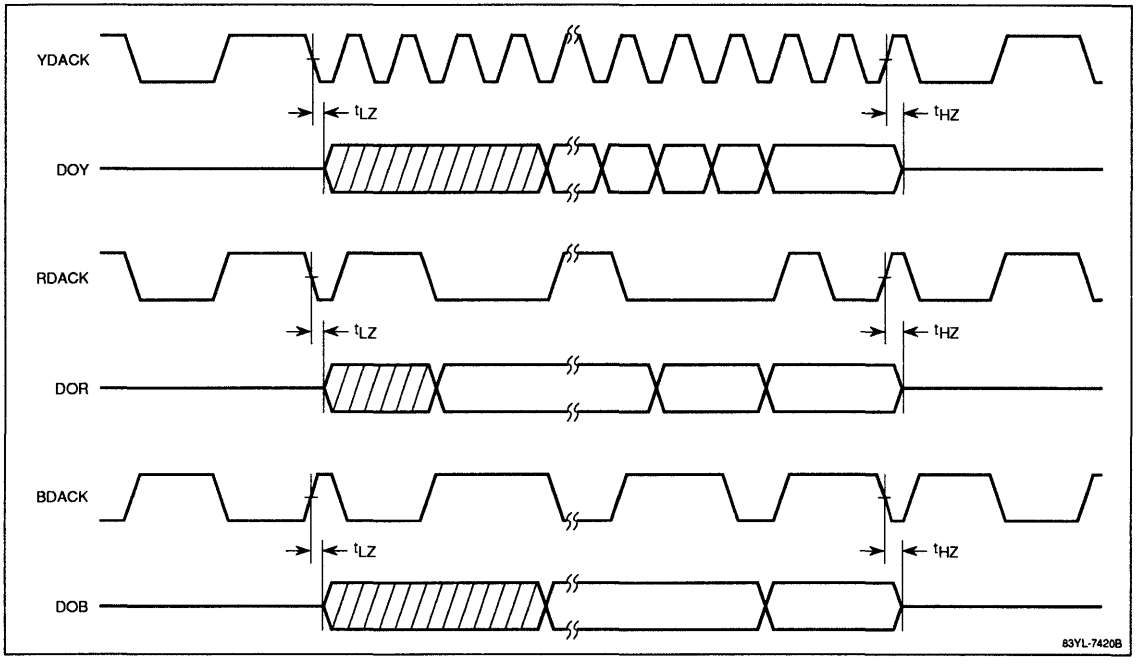


Timing Waveforms (cont)

Output Timing 3



Output Timing 4



18d

μPD42280
NTSC and PAL Field Buffer

Description

The μPD42280 is a 262,224-word by 8-bit dual-port field buffer fabricated with a silicon-gate CMOS process. The device can execute synchronous and asynchronous serial write and serial read operation at a 33.3-MHz clock frequency. In asynchronous mode, the device can be used as a data storage (communication) buffer, a time axis converter, and a digital delay line of up to 262,224 bits (200 bits minimum at any frequency). In synchronous mode, the minimum delay is 3 bits at any frequency when used as a fixed-length delay line.

Applications include NTSC/PAL TV/VCR systems, video processing, digital plain paper copiers, and systems requiring serial data streams like printers, optical scanners, and local area networks.

The serial write and read function simplifies interframe luminance (Y) and chrominance (C) separation, interfield noise reduction, frame synchronization, and time base correction. Refreshing is performed automatically by an internal circuit, so the device operates like a static RAM.

All inputs and outputs, including clocks, are TTL compatible. The plastic package is a 28-pin SOP (450-mil) or ZIP (400-mil), and operation is guaranteed in an ambient temperature range of −20 to +70°C.

Features

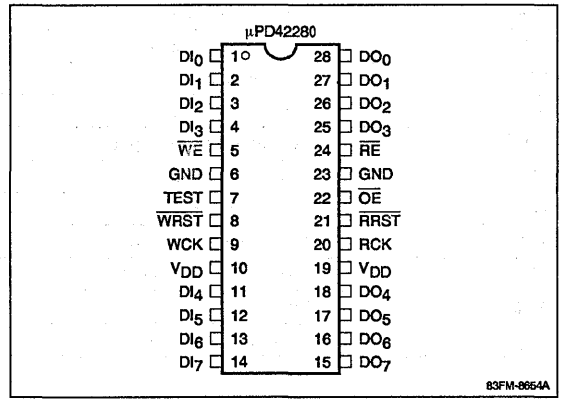
- 262,224-word x 8-bit organization
- Dual-port operation
- Asynchronous, simultaneous reading/writing
- Output enable function
- Variable field length
  - — 200 to 262,224 bits as an elastic (asynchronous) delay line
  - — 3 to 262,224 bits as a fixed-length (full synchronous) delay line
- One-cycle address pointer reset and immediate write/read access function
- Automatic refreshing (full static interface)
- Direct connection with NEC line buffers (μPD42101/42102/42505)
- 4M-bit DRAM COMS technology
- Full TTL-compatible inputs, outputs, and clocks
- Three-state outputs
- Single +5-volt power supply
- On-chip substrate bias generator
- 28-pin SOP (450-mil) and ZIP (400-mil) plastic packaging

Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42280GU-30	25 ns	30 ns	28-pin plastic SOP
GU-40	30 ns	40 ns	
GU-60	40 ns	60 ns	
μPD42280V-30	25 ns	30 ns	28-pin plastic ZIP
V-40	30 ns	40 ns	
V-60	40 ns	60 ns	

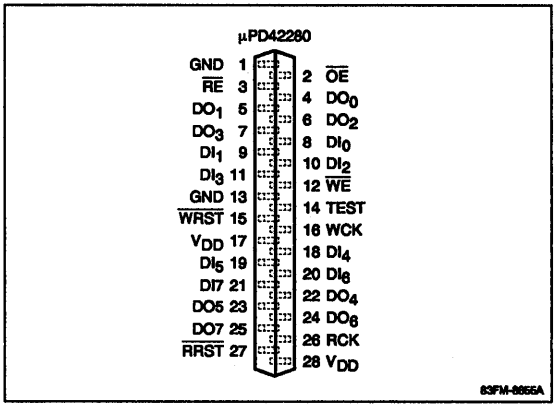
Pin Configurations

28-Pin Plastic SOP



Pin Configurations

28-Pin Plastic ZIP



Pin Identification

Symbol	Function
DI_0 - DI_7	Write data inputs
DO_0 - DO_7	Read data outputs
$\overline{OE}$	Output enable input
RCK	Read clock input
$\overline{RE}$	Read enable input
$\overline{RRST}$	Read address reset input
WCK	Write clock input
$\overline{WE}$	Write enable input
$\overline{WRST}$	Write address reset input
TEST	Test pin (connect to GND in system)
GND	Ground
V_{DD}	+5-volt power supply

PIN FUNCTIONS

DI_0 - DI_7 (Data Inputs)

These pins function as write data inputs; for example, for $4f_{SC}$ composite color or brightness signals.

DO_0 - DO_7 (Data Outputs)

These pins are three-state read outputs.

$\overline{OE}$ (Output Enable Input)

This signal controls read data output. When $\overline{OE}$ is low, read data is output on DO_0 - DO_7. When $\overline{OE}$ is high, DO_0 - DO_7 are in a state of high impedance. The read address pointer is incremented by RCK, regardless of the signal level of $\overline{OE}$. The state of $\overline{OE}$ is strobed by the rising edge of RCK.

RCK (Read Clock Input)

All read cycles are executed synchronously with RCK. The states of both $\overline{RRST}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increases with each RCK cycle unless $\overline{RE}$ is at a high level to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 262,223 to 0 and begin increasing again.

$\overline{RE}$ (Read Enable Input)

This signal is similar to $\overline{WE}$ but controls read operation. If $\overline{RE}$ is at a high level, the internal read address stops increasing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

$\overline{RRST}$ (Read Address Reset Input)

This signal is strobed by the rising edge of RCK and resets the internal read address to 0.

WCK (Write Clock Input)

All write cycles are executed synchronously with WCK. The states of both $\overline{WRST}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increases with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 262,223 to 0 and begin increasing again.

$\overline{WE}$ (Write Enable Input)

This input controls write operation. If $\overline{WE}$ is low, all write cycles proceed. If $\overline{WE}$ is at a high level, no data is written to the register and the write address stops increasing. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

$\overline{WRST}$ (Write Address Reset Input)

Bringing this signal low resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

18e

OPERATION

Reset

The μPD42280 requires initialization of internal circuits using the $\overline{WRST}$/$\overline{RRST}$ reset signals before starting operation (after power on). A reset cycle can be executed at any time and does not depend on the state of $\overline{WE}$, $\overline{RE}$, and $\overline{OE}$. However, $\overline{WRST}$ and $\overline{RRST}$ must satisfy required setup and hold times as measured from the rising edges of WCK and RCK.

After the reset cycle, write and read operation can be started immediately.

Write

Write cycles are executed in synchronization with WCK as $\overline{WE}$ is held low. In the write cycle operation, the internal write address pointer is automatically incremented. When $\overline{WE}$ is high at the rising edge of WCK, write operation is disabled and the internal write address pointer does not increment with successive write clocks.

Write data must satisfy setup and hold times as specified from the rising edge of WCK.

After the reset operation, bits are input sequentially into an 80 x 8-bit SRAM buffer. Then, new bits are input sequentially into one of the two halves of the 128 x 8-bit data register before being transfered to the storage array. The register data is transferred into the array in blocks of 64 x 8 bits.

Read

Read cycles are executed in synchronization with RCK while $\overline{RE}$ and $\overline{OE}$ are held low.

In the read cycle operation, the internal read address pointer is automatically incremented as $\overline{RE}$ is held low. When $\overline{RE}$ is high at the rising edge of RCK, the internal read address pointer does not increment with successive read clocks.

The $\overline{OE}$ input controls the output state of DO_0 - DO_7 pins. When $\overline{OE}$ is low at the rising edge of RCK, the DO_0 - DO_7 pins are low-impedance state. When $\overline{OE}$ is high at the rising edge of RCK, the DO_0 - DO_7 pins are high-impedance state with successive read clocks.

The access time of a read cycle is measured from the rising edge of RCK by t_{AC} for an access of any internal read address. Stored data is read nondestructively; data can be read repeatedly at any time (cell data hold time is endless).

New data written to a particular internal address is available for reading after 200 write cycles maximum. This value depends on write cycle time and the write/read operation control method.

DIGITAL DELAY LINE

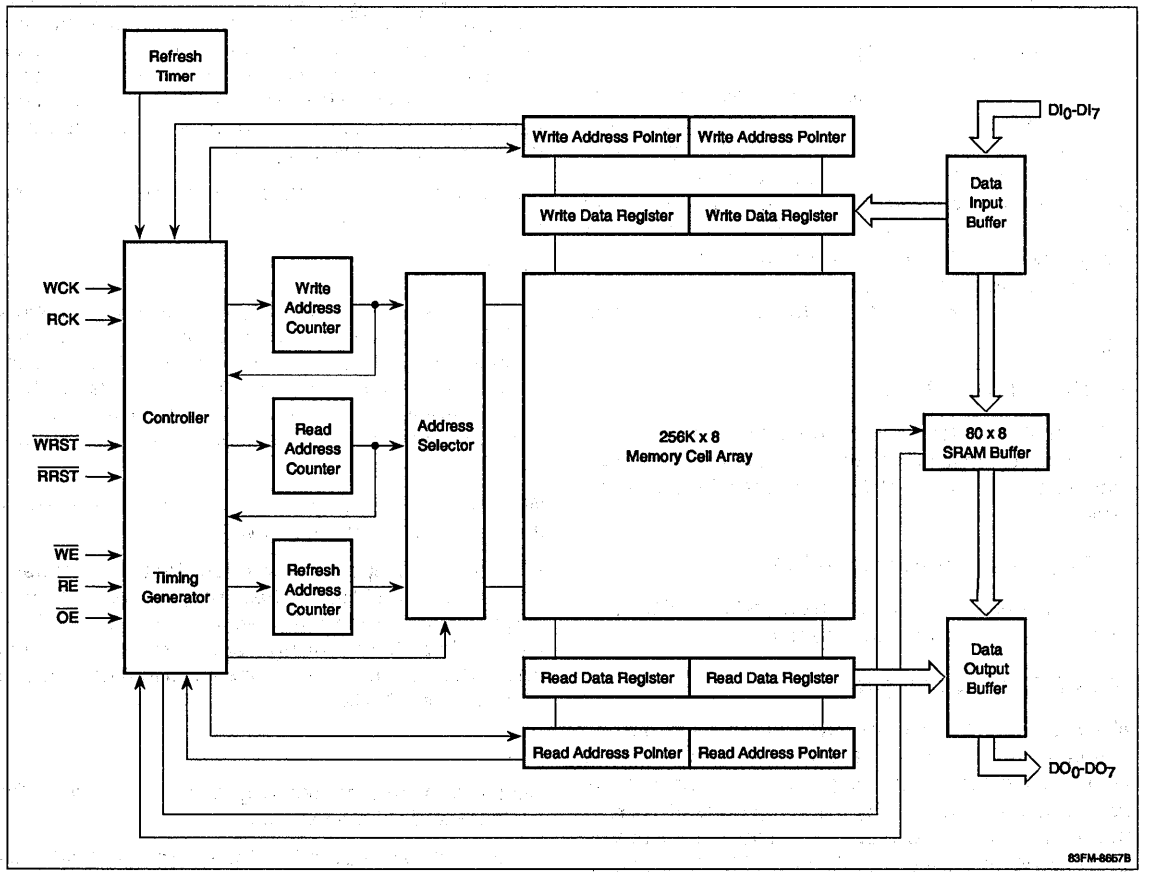
The μPD42280 can be easily used as a digital delay line of 262,224 bits or less. The two operating modes are elastic (asynchronous) and fixed-length (full-synchronous).

Elastic (Asynchronous) Delay Line

Delay length of the elastic delay line is from 200 bits minimum (at any frequency) to 262,224 bits maximum. The minimum delay length does not depend on clock frequency.

Figures 1 and 2 show control timings for the elastic delay line. Write and read cycles are synchronized to

μPD42280 Block Diagram



their respective WCK/RCK inputs and executed individually. The difference (n) between the internal write address pointer and the internal read address pointer must fall between 199 and 262,223.

Fixed-Length (Full-Synchronous) Delay Line

The length of the delay line is specified as 3 to 262,224 bits. It does not depend on clock frequency

FIgure 3 shows control timing for the fixed-length delay line. The same signal is used for WCK and RCK so that $\overline{WRST}$ and $\overline{RRST}$ are controlled together. The data, written after a reset signal, is read out after the next reset signal in the order it was written. This interval determines the delay length. For example, if the reset signal is input every 239,330 (263 x 910) cycles, the delay length is 239,330 cycles.

Figure 1. Elastic Delay Line No. 1

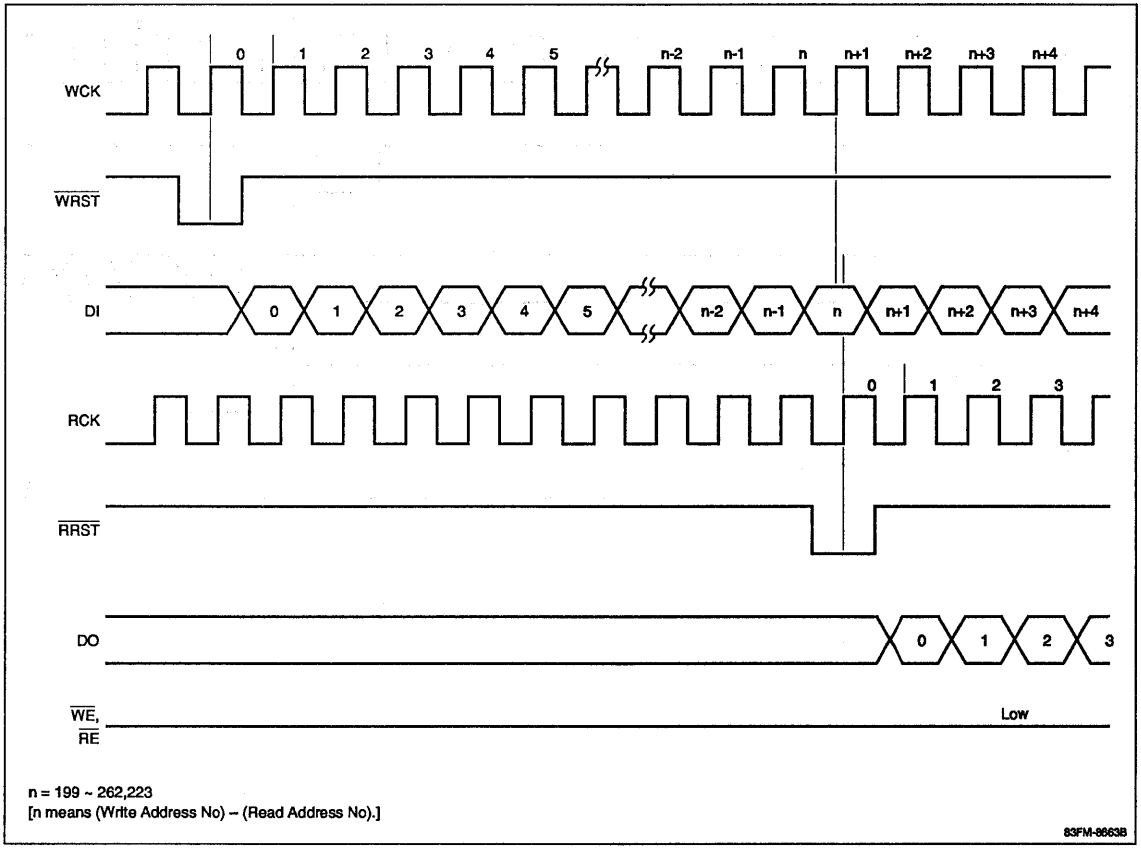
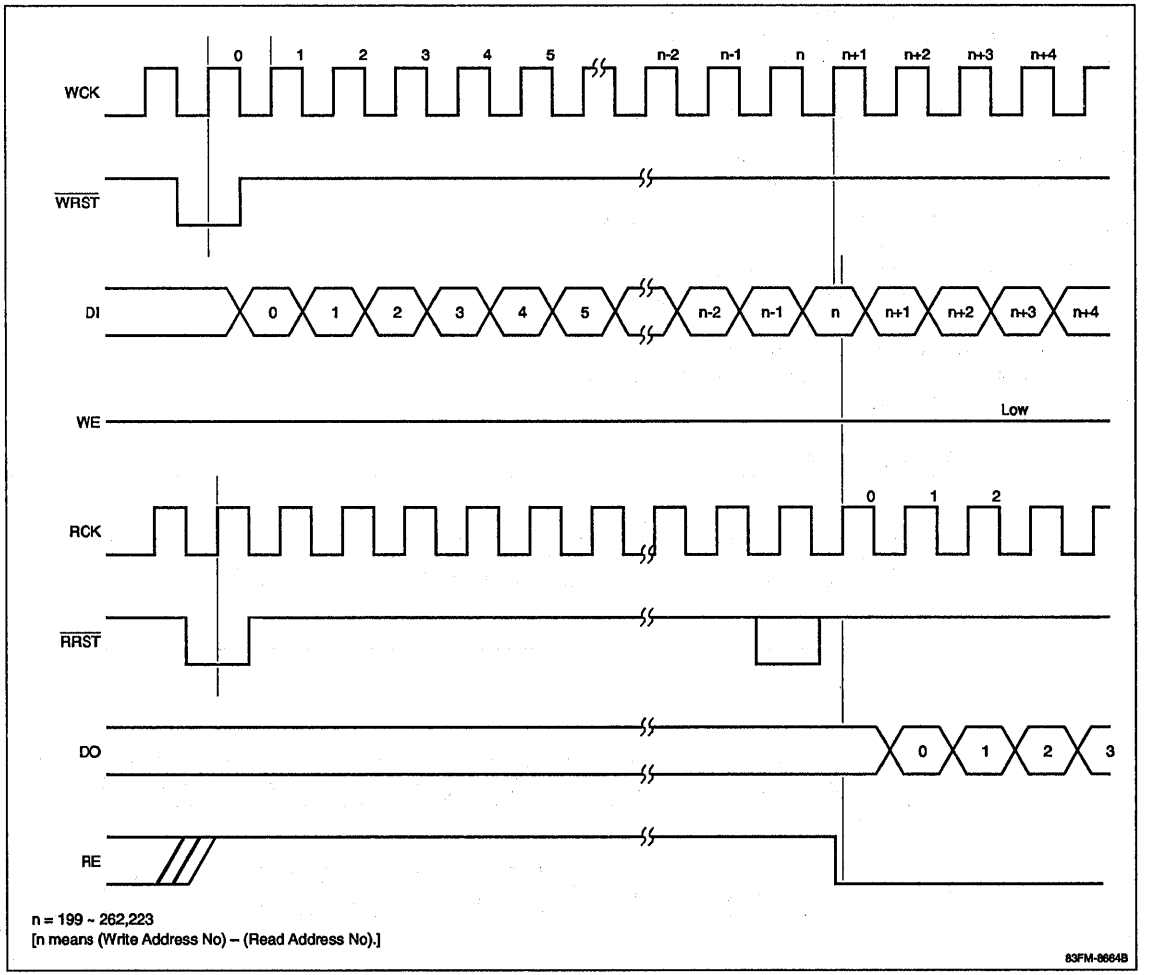


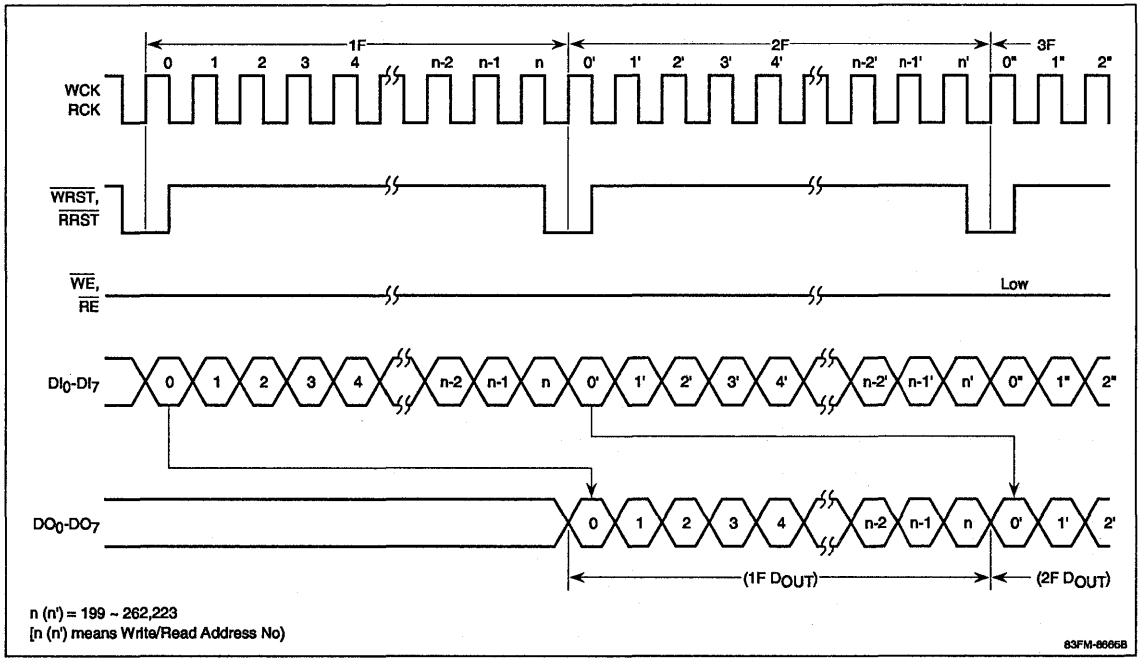
Figure 2. Elastic Delay Line No. 2



n = 199 ~ 262,223
[n means (Write Address No) – (Read Address No).]

83FM-8664B

Figure 3. Fixed-Length Delay Line



SPECIFICATIONS

Absolute Maximum Ratings

Supply voltage, V_{DD}	−1.0 to +7.0 V
Voltage on any input pin, V_I	−1.0 to V_{DD} + 0.5 V (+7.0 V max)
Voltage on any output pin, V_O	−1.0 to V_{DD} + 0.5 V (+7.0 V max)
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{DD} + 0.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	−20		+70	°C

Capacitance

T_A = 25°C; V_{DD} = +5.0 V ±10%; f = 1 MHz

Parameter †	Symbol	Min	Max	Unit	Pins Under Test
Input capacitance	C_I		5	pF	$\overline{WE}$, $\overline{RE}$, $\overline{OE}$ WCK, RCK, $\overline{WRST}$, $\overline{RRST}$, DI_0 - DI_7
Output capacitance	C_O		7	pF	DO_0 - DO_7

† Capacitance is sampled and not 100% tested.

DC Characteristics

T_A = −20 to +70°C; V_{DD} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Operating current	I_{CC1}		50	90	mA	t_{WCK}, t_{RCK} = 30 ns
Standby current	I_{CCS}		4	10	mA	WCK, RCK = V_{IL}
Input leakage current	I_I	−10		10	μA	V_I = 0 to V_{DD}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_O disabled; V_O = 0 to V_{DD}
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.0 mA

* Voltages are referenced to GND.

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD42280-30		μPD42280-40		μPD42280-60			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Access time	t_{AC}		25		30		40	ns	
Data-in hold time	t_{DH}	3		3		3		ns	
Data-in setup time	t_{DS}	7		10		12		ns	
Output disable time	t_{HZ}	5	25	5	30	5	40	ns	(Note 4)
Output active time	t_{LZ}	5	25	5	30	5	40	ns	(Note 4)
Output enable hold time	t_{OEH}	3		3		3		ns	(Note 9)
Output enable high delay from RCK	t_{OEN1}	3		3		3		ns	(Note 10)
Output enable low delay from RCK	t_{OEN2}	7		10		12		ns	(Note 10)
Output enable setup time	t_{OES}	7		10		12		ns	(Note 9)
Output hold time	t_{OH}	5		5		5		ns	
Read clock cycle time	t_{RCK}	30		40		60		ns	
RCK precharge time	t_{RCP}	12		14		20		ns	
RCK pulse width	t_{RCW}	12		14		20		ns	
Read enable hold time	t_{REH}	3		3		3		ns	(Note 7)
Read enable high delay from RCK	t_{REN1}	3		3		3		ns	(Note 8)
Read enable low delay to RCK	t_{REN2}	7		10		12		ns	(Note 8)
Read enable setup time	t_{RES}	7		10		12		ns	(Note 7)
Read disable pulse width	t_{REW}	0		0		0		ns	
Reset active hold time	t_{RH}	3		3		3		ns	(Note 5)
Reset inactive setup time	t_{RN1}	3		3		3		ns	(Note 6)
Reset inactive hold time	t_{RN2}	7		10		12		ns	(Note 6)
Read reset time	t_{RRST}	0		0		0		ns	
Reset active setup time	t_{RS}	7		10		12		ns	(Note 5)
Transition time	t_T	3	35	3	35	3	35	ns	
Write clock cycle time	t_{WCK}	30		40		60		ns	
WCK precharge time	t_{WCP}	12		14		20		ns	
WCK pulse width	t_{WCW}	12		14		20		ns	
Write enable hold time	t_{WEH}	3		3		3		ns	(Note 7)

AC Characteristics (cont)

Parameter	Symbol	μPD42280-30 Min	μPD42280-30 Max	μPD42280-40 Min	μPD42280-40 Max	μPD42280-60 Min	μPD42280-60 Max	Unit	Test Conditions
Write enable high delay from WCK	t_{WEN1}	3		3		3		ns	(Note 8)
Write enable low delay to WCK	t_{WEN2}	7		10		12		ns	(Note 8)
Write enable setup time	t_{WES}	7		10		12		ns	(Note 7)
Write disable pulse width	t_{WEW}	0		0		0		ns	
Write reset time	t_{WRST}	0		0		0		ns	

18e

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns. Input pulse levels = 0.4 to 2.4 V. Transition times are measured between 2.4 and 0.4 V. See figure 4.

(3) Input timing reference levels = 1.5 V. Output timing reference levels are 0.8 and 2.0 V. See figure 4.

(4) This delay is measured at 200 mV from the steady-state voltage with the load specified in figure 4. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(6) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(7) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(8) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(9) If either t_{OES} or t_{OEH} is less than the specified value, output disable operations are not guaranteed.

(10) If either t_{OEN1} or t_{OEN2} is less than the specified value, internal output disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(11) To read new data just written, the write address must precede the read address by at least 200 addresses.

(12) During a reset operation, the levels of $\overline{WE}$ and $\overline{RE}$ are "dont care."

(13) Addresses 0-79 (80 words x 8 bits) are stored in an SRAM buffer. Addresses 80-262,223 are stored in dynamic cells and transferred in 64 x 8-bit increments. The "143" in the equation below comes from 79 + 64 = 143.

When $\overline{WRST}$ goes low (active) at address n, the write data from address n to address m is not guaranteed because partial data stored in the write registers (< 64 bits) will not be transferred to the DRAM array.

(13 cont)

$$m = 143 + \frac{n-80}{64} \times 64$$

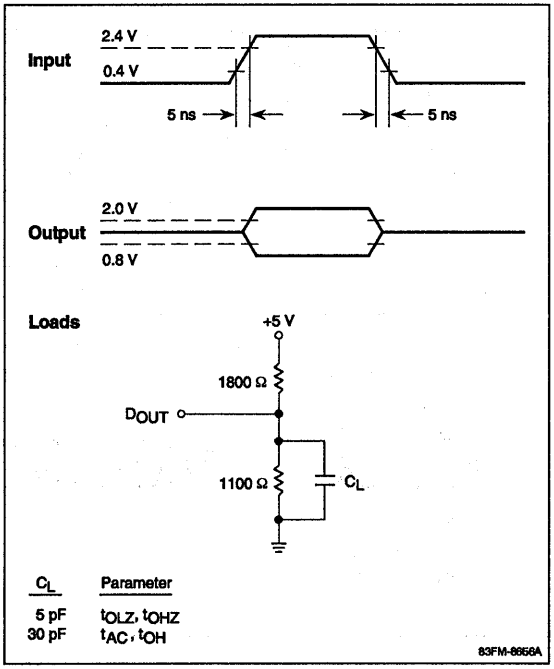
$\frac{n-80}{64}$ means the nearest whole number

For example, if n = 280, then $\frac{n-80}{64} = 3.125 = 3$

$$m = 143 + (3 \times 64)$$
$$= 143 + 192$$
$$= 335$$

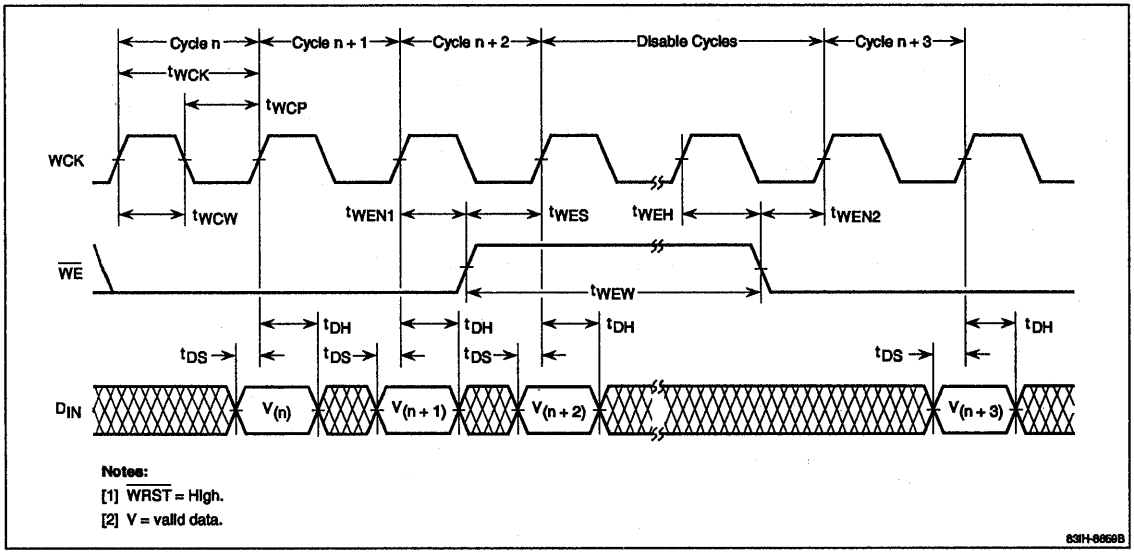
So, data transfer from address 280 to address 335 is not guaranteed.

Figure 4. AC Test Conditions



Timing Waveforms

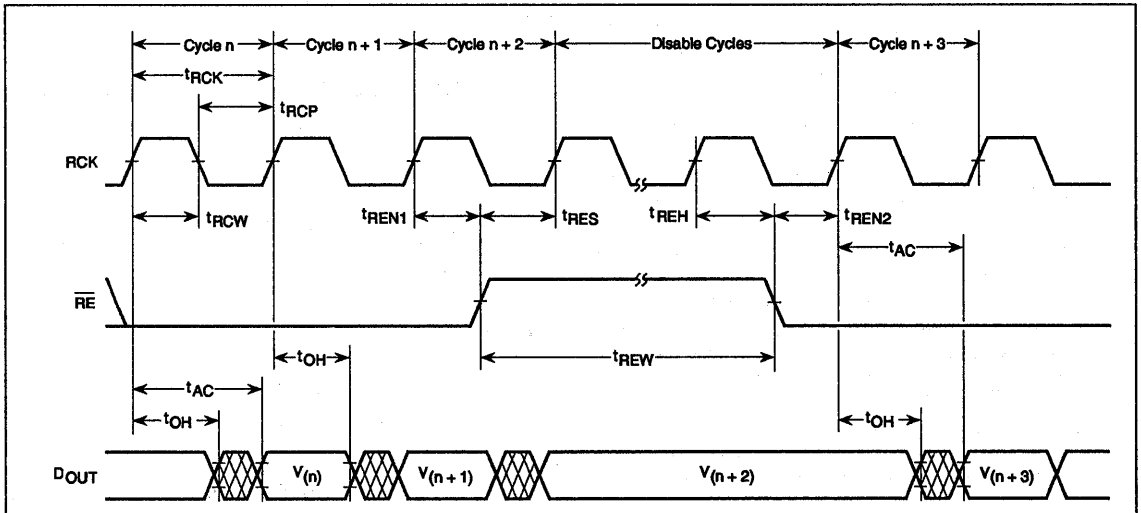
Write Cycle



Notes:
[1] $\overline{WRST}$ = High.
[2] V = valid data.

83IH-8659B

Read Cycle ($\overline{RE}$ Control)

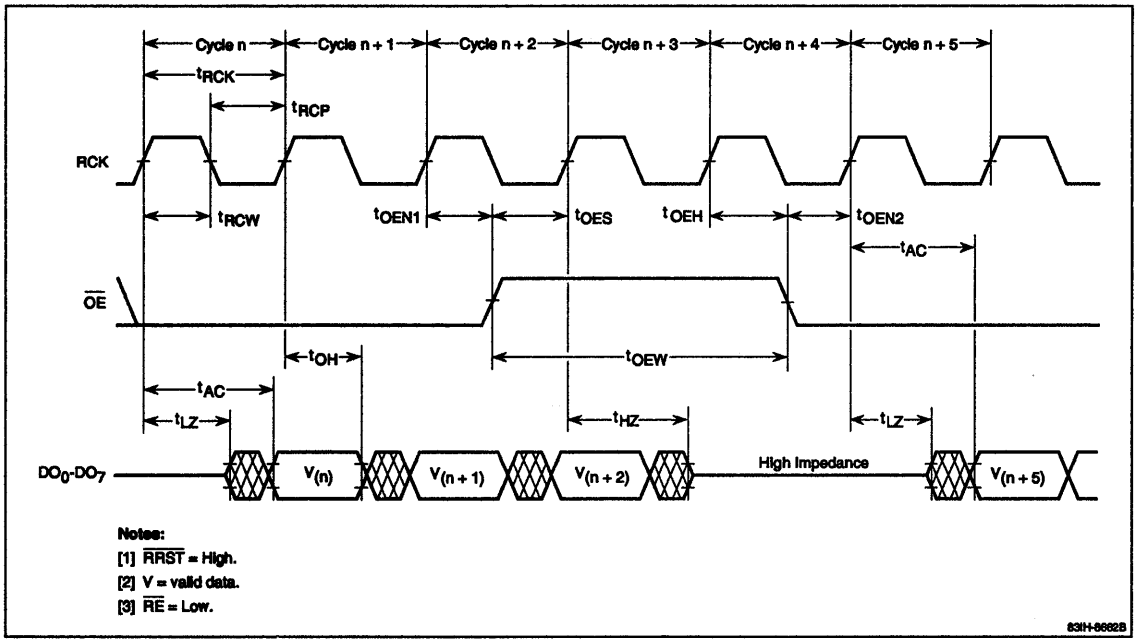


Notes:
[1] $\overline{RRST}$ = High.
[2] V = valid data.
[3] $\overline{OE}$ = Low.

83IH-8658B

Timing Waveforms (cont)

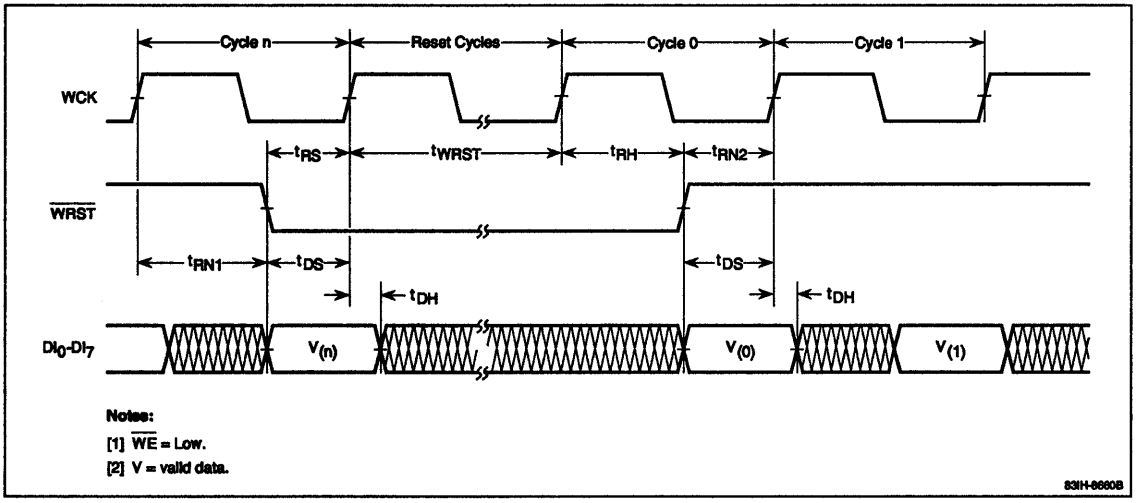
Read Cycle ($\overline{OE}$ Control)



Notes:
[1] $\overline{RRST}$ = High.
[2] V = valid data.
[3] $\overline{RE}$ = Low.

83IH-8662B

Write Reset Cycle

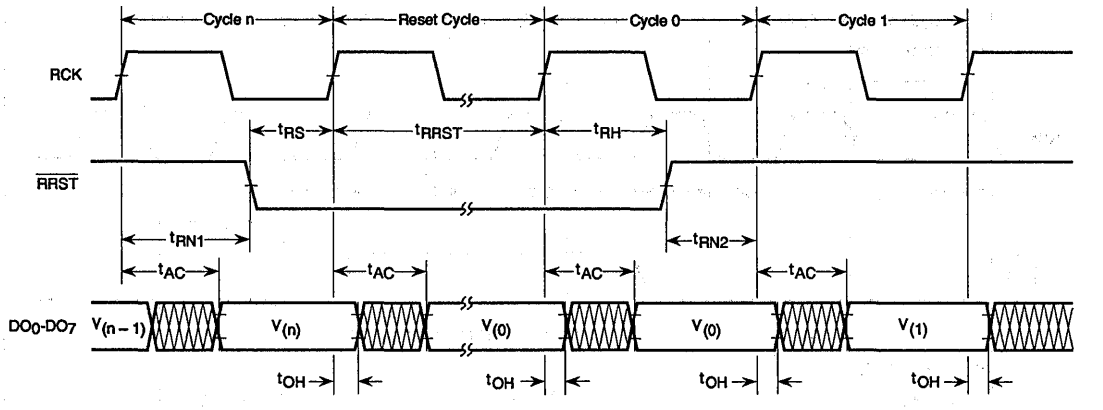


Notes:
[1] $\overline{WE}$ = Low.
[2] V = valid data.

83IH-8660B

Timing Waveforms (cont)

Read Reset Cycle



Notes:
[1] $\overline{RE}$, $\overline{OE}$ = Low.
[2] V = valid data.

83IH-8661B

Description

The μPD42505 is a 5048-word by 8-bit dual-port line buffer fabricated with a silicon-gate CMOS process. The device is capable of asynchronous read and write operation at high speed, and can be used as a time axis converter or a digital delay line of up to 5048 bits (10 bits minimum at maximum frequency).

Applications include image processing in facsimile machines, plain paper copiers, video systems, and other optical scanners; time base correction in video playback systems; and data communication buffering in multiprocessor systems and local area networks.

Features

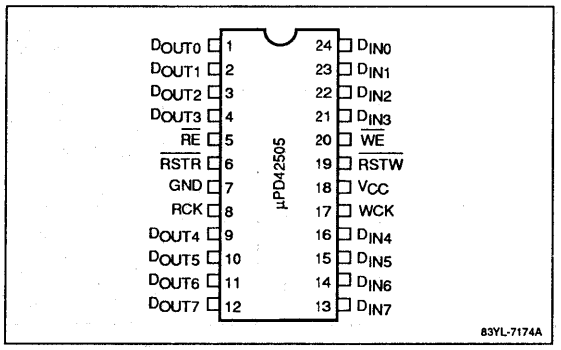
- 5048-word x 8-bit organization
- Dual-port operation
- Image processing and data communications applications
- Asynchronous and simultaneous reading/writing
- 1H (5048-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single + 5-volt power supply
- 24-pin plastic DIP and 28-pin plastic ZIP packaging

Pin Identification

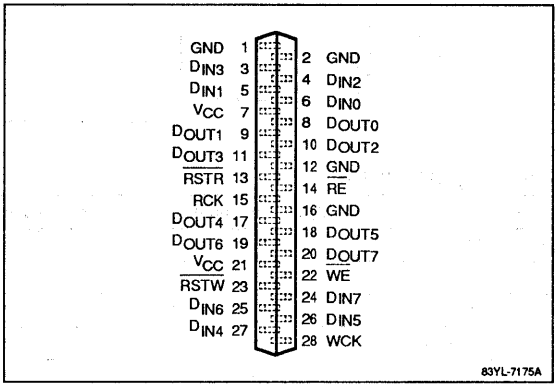
Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
RCK	Read clock input
$\overline{RE}$	Read enable input
$\overline{RSTR}$	Read address reset input
$\overline{RSTW}$	Write address reset input
WCK	Write clock input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply

Pin Configurations

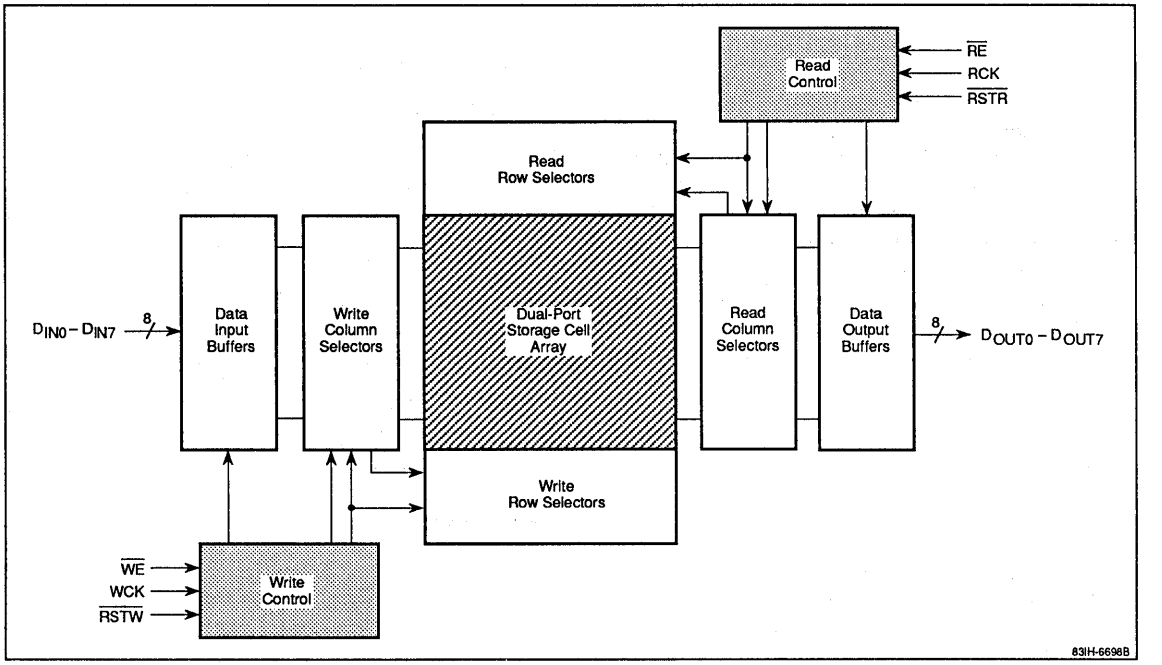
24-Pin Plastic DIP



28-Pin Plastic ZIP



Block Diagram



Ordering Information

Device	Cycle Time (min)	Read Access Time (max)	Hold Time (min)	Package
μPD42505C-50	50 ns	40 ns	5 ms	24-pin plastic DIP
C-75	75 ns	55 ns		
C-50H	50 ns	40 ns	20 ms	
C-75H	75 ns	55 ns		
μPD42505V-50	50 ns	40 ns	5 ms	28-pin plastic ZIP
V-75	75 ns	55 ns		
V-50H	50 ns	40 ns	20 ms	
V-75H	75 ns	55 ns		

Pin Functions

D_{IN0} through D_{IN7} (Data Inputs). New data is entered on these pins.

D_{OUT0} through D_{OUT7} (Data Outputs). These tri-state outputs are used to access stored information. In a simple digital delay line application, a minimum delay of 10 clock cycles is required to move data from the input pins to the output pins.

RCK (Read Clock Input). All read cycle are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are strobed by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge. The internal read address increments with each RCK cycle, unless $\overline{RE}$ is high to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 5047 to 0 and begin incrementing again.

$\overline{RE}$ (Read Enable Input). This signal controls read operation. If $\overline{RE}$ is low, all read cycles proceed. If $\overline{RE}$ is at a high level, the data outputs become high impedance and the internal read address stops incrementing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

$\overline{RSTR}$ (Read Address Reset Input). This signal is strobed by the rising edge of RCK and resets the internal read address to 0.

$\overline{RSTW}$ (Write Address Reset Input). Bringing this signal low resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

WCK (Write Clock Input). All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle. The internal write address increments with each WCK cycle, unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 5047 to 0 and begin incrementing again.

$\overline{WE}$ (Write Enable Input). This input is similar to $\overline{RE}$ but controls write operation. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address does not increment. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

Operation

Reset Cycle. The μPD42505 requires the initialization of internal circuits using the $\overline{RSTW}/\overline{RSTR}$ reset signals before starting operation as a time axis converter or a digital delay line.

A reset cycle can be executed at any time and does not depend on the state of $\overline{RE}$ or $\overline{WE}$. However, $\overline{RSTW}$ and $\overline{RSTR}$ must satisfy required setup and hold times as measured from the rising edges of WCK and RCK.

Write/Read Cycles. Write and read cycles are synchronized to their respective WCK/RCK inputs and executed individually when WCK or RCK is high and $\overline{WE}$ or $\overline{RE}$ is low. Write data must satisfy setup and hold times as specified from the rising edge of WCK. New data written to a particular address is available for reading after 1/2 write cycle + 500 ns (maximum).

The access time of a read cycle is measured from the rising edge of RCK, either by t_{ACR} for an access during the first cycle directly after a reset begins, or by t_{AC} for an access under other conditions. Stored data is read nondestructively; data can be read repeatedly within a prescribed time of 5 ms maximum (20 ms maximum for -H versions).

Time Axis Conversion. To use the μPD42505 as a time axis converter, write and read cycles must be controlled independently. Write and read ports must be initialized separately using the reset signals. Write cycles can then be executed in synchronization with WCK and write data can be stored sequentially from address 0 of this device. Afterward, when a read cycle is executed in synchronization with RCK, stored data can be read sequentially from address 0.

Since write and read cycles can be executed independently, data loaded at one arbitrary drive frequency can be read at another arbitrary drive frequency. In this sense, the μPD42505 functions as a time axis converter.

Digital Delay Line. The μPD42505 can be easily used as a digital delay line of 5,048 bits or less. After the internal circuits are initialized using simultaneous $\overline{RSTW}/\overline{RSTR}$ signals, write/read cycles also may be executed simultaneously by supplying the same pulse to the write (WCK) and read (RCK) clocks. Write data is always read after the full 5,048-bit delay if neither write nor read operation has been inhibited. This is the essential delay line function.

If either $\overline{WE}$ or $\overline{RE}$ is set at a nonselected (high) level for several cycles while the other is maintained in a selected (low) level, the delay line length can differ from 5,048 bits.

For example, if only $\overline{WE}$ is a set to a high level (write disable) for a small number of cycles, read cycles are executed continuously and the delay line length is large (see the waveform for "(5048-m)-Bit Delay Line No. 2"). Alternatively, if only $\overline{RE}$ is set to a high level (read disable) for a small number of cycles, write cycles are executed continuously and the delay line length is small. Note that the minimum delay line length is 10 bits (for maximum frequency operation) and the maximum is 5,048 bits.

A data delay of 5,048 bits or less can also be obtained by applying the $\overline{RSTW}$ and $\overline{RSTR}$ signals at different times. For example, data loaded for "m" cycles after $\overline{RSTW}$ can then be read after supplying $\overline{RSTR}$. In this case, since write data can be read from the beginning after a delay of "m" cycles, the device can be used as an "m-bit" digital delay line.

The $\overline{RSTW}/\overline{RSTR}$ reset signals can also be simultaneously loaded at every 1H (horizontal line) period. In this case, write data loaded in the previous line cycle is read out from the beginning as read data after the reset. Therefore, a delay line length ranging from 10 to 5,048 bits can be obtained according to the length of the reset signals supplied. Refer to the timing waveform for an "n-Bit Delay Line."

Absolute Maximum Ratings

Supply voltage, V_{CC}	−1.5 to +7.0 V
Voltage on any input pin, V_I	−1.5 to +7.0 V
Voltage on any output pin, V_O	−1.5 to +7.0 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	−20 to +70 °C
Storage temperature, T_{STG}	−55 to +125 °C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.5		0.8	V
Ambient temperature	T_A	−20		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter	Symbol	Max	Unit	Test Conditions
Input capacitance	C_I	5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O	7	pF	D_{OUT0} - D_{OUT7}

Notes:

(1) These parameters are sampled and not 100% tested.

DC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}			60	mA	
Input leakage current	I_I	−10		10	μA	V_I = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%

		μPD42505-50		μPD42505-75		μPD42505-50H		μPD42505-75H			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Write clock cycle time	t_{WCK}	50	990	75	990	50	3960	75	3960	ns	
WCK pulse width	t_{WCW}	20		30		20		30		ns	
WCK precharge time	t_{WCP}	20		30		20		30		ns	
Read clock cycle time	t_{RCK}	50	990	75	990	50	3960	75	3960	ns	
RCK pulse width	t_{RCW}	20		30		20		30		ns	
RCK precharge time	t_{RCP}	20		30		20		30		ns	
Access time	t_{AC}		40		55		40		55	ns	
Access time after a reset cycle	t_{ACR}		40		55		40		55	ns	
Output hold time	t_{OH}	5		5		5		5		ns	
Output hold time after a reset cycle	t_{OHR}	5		5		5		5		ns	(Note 7)
Output active time	t_{LZ}	5	40	5	55	5	40	5	55	ns	(Note 4)
Output disable time	t_{HZ}	5	40	5	55	5	40	5	55	ns	(Note 4)
Data-in setup time	t_{DS}	15		20		15		20		ns	

AC Characteristics

T_A = −20 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD42505-50		μPD42505-75		μPD42505-50H		μPD42505-75H		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Data-in hold time	t_{DH}	5		5		5		5		ns	
Reset active setup time	t_{RS}	15		20		15		20		ns	(Note 8)
Reset active hold time	t_{RH}	5		5		5		5		ns	(Note 8)
Reset inactive hold time	t_{RN1}	5		5		5		5		ns	(Note 9)
Reset inactive setup time	t_{RN2}	15		20		15		20		ns	(Note 9)
Write enable setup time	t_{WES}	15		20		15		20		ns	(Note 10)
Write enable hold time	t_{WEH}	5		5		5		5		ns	(Note 10)
Write enable high delay from WCK	t_{WEN1}	5		5		5		5		ns	(Note 11)
Write enable low delay to WCK	t_{WEN2}	15		20		15		20		ns	(Note 11)
Read enable setup time	t_{RES}	15		20		15		20		ns	(Note 10)
Read enable hold time	t_{REH}	5		5		5		5		ns	(Note 10)
Read enable high delay from RCK	t_{REN1}	5		5		5		5		ns	(Note 11)
Read enable low delay to RCK	t_{REN2}	15		20		15		20		ns	(Note 11)
Write disable pulse width	t_{WEW}	0		0		0		0		ms	(Note 6)
Read disable pulse width	t_{REW}	0		0		0		0		ms	(Note 6)
Write reset time	t_{RSTW}	0		0		0		0		ms	(Note 6)
Read reset time	t_{RSTR}	0		0		0		0		ms	(Note 6)
Transition time	t_T	3	35	3	35	3	35	3	35	ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ±200 mv from the steady-state voltage with the load specified in figure 2. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

(6) t_{WEW} (max) and t_{REW} (max) must be satisfied by the next equations in one line cycle operation:
$t_{WEW} + t_{RSTW} + 5048t_{WCK} \leq 5$ ms (20 ms for -H versions)
$t_{REW} + t_{RSTR} + 5048t_{RCK} \leq 5$ ms (20 ms for -H versions)

(7) This parameter applies when $t_{RCK} \geq t_{ACR}$ (max)

(8) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(9) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(10) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) disable operations are not guaranteed.

(11) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 1. Output Load for t_{AC}, t_{ACR}, t_{OH}, and t_{OHR}

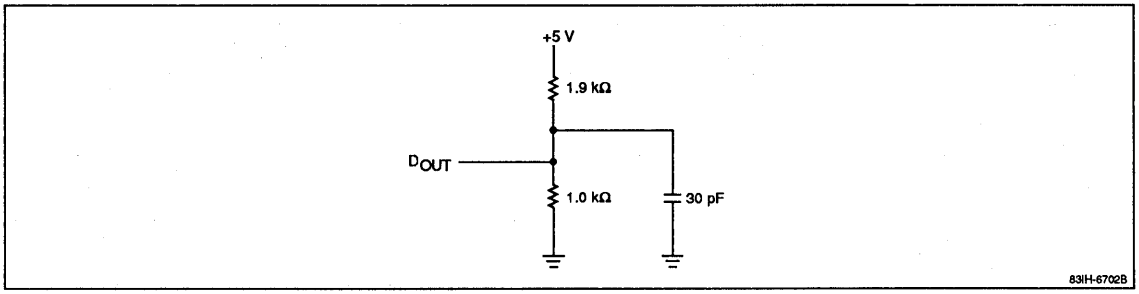


Figure 2. Output Load for t_{LZ} and t_{HZ}

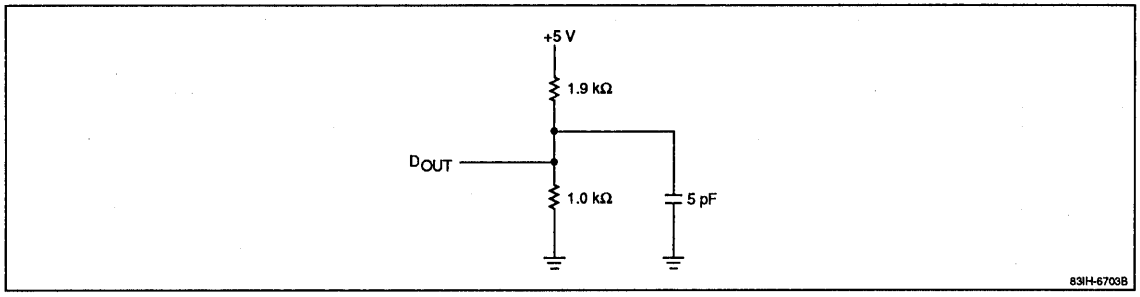


Figure 3. Input Timing

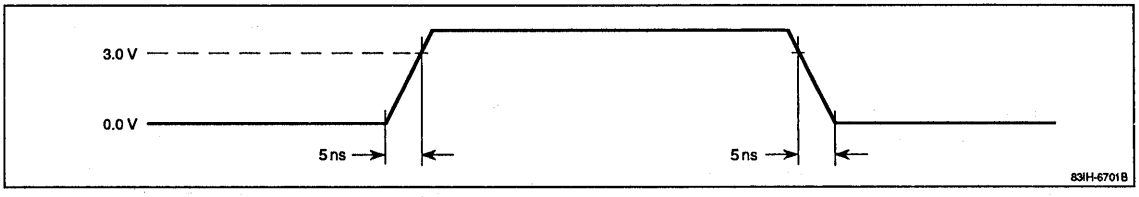
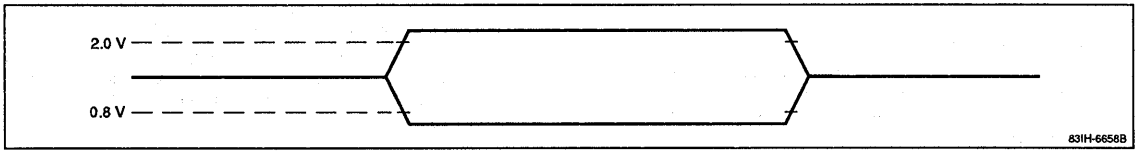
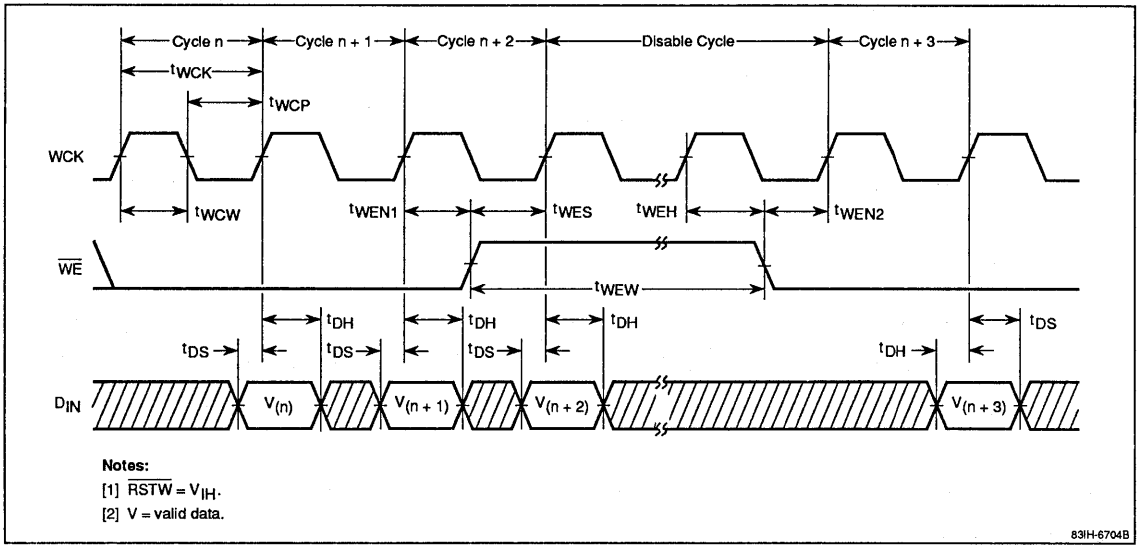


Figure 4. Output Timing



Timing Waveforms

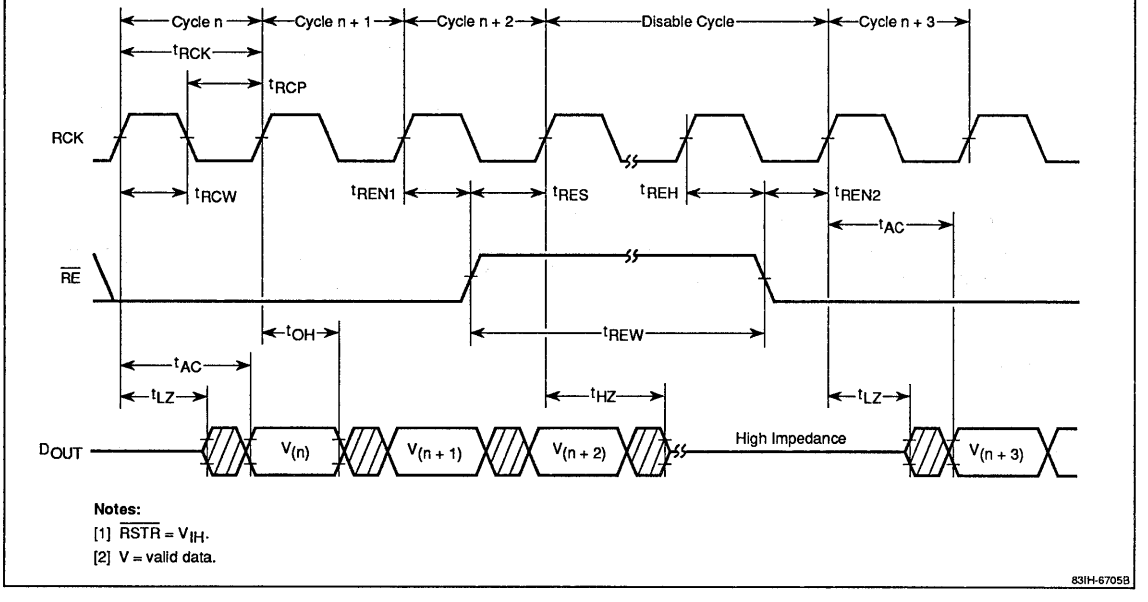
Write Cycle



Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

83IH-6704B

Read Cycle



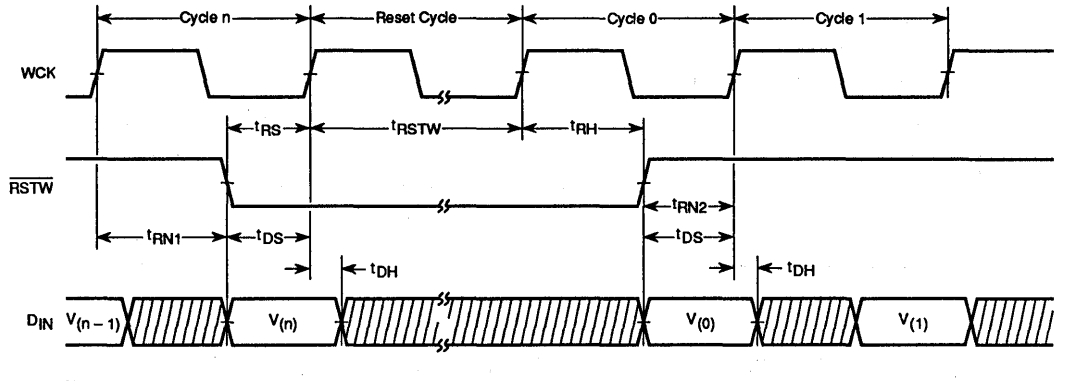
Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.

83IH-6705B

18f

Timing Waveforms (cont)

Write Reset Cycle



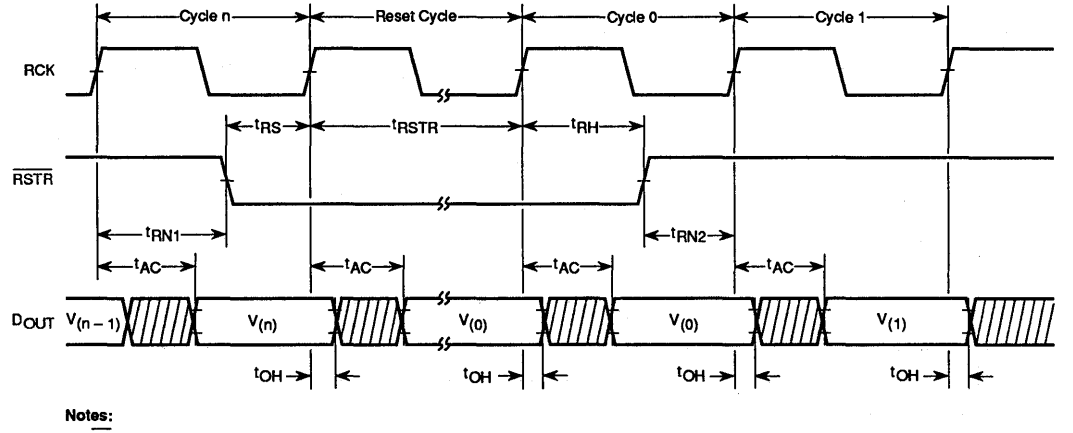
Notes:

[1] $\overline{WE} = V_{IL}$.

[2] V = valid data.

83IH-6706B

Read Reset Cycle



Notes:

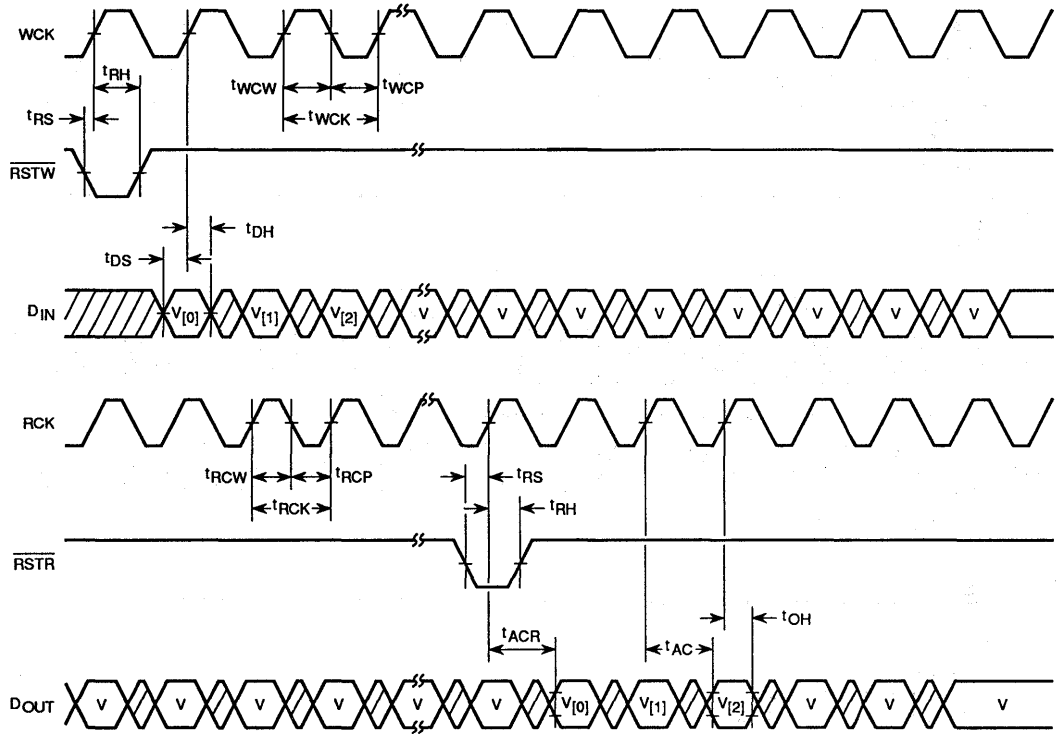
[1] $\overline{RE} = V_{IL}$.

[2] V = valid data.

83IH-6707B

Timing Waveforms (cont)

Time Axis Conversion Cycle



Notes:

[1] $\overline{WE} = \overline{RE} = V_{IL}$

[2] V = valid data.

[3] Read cycles commence from the rising edge of RCK. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

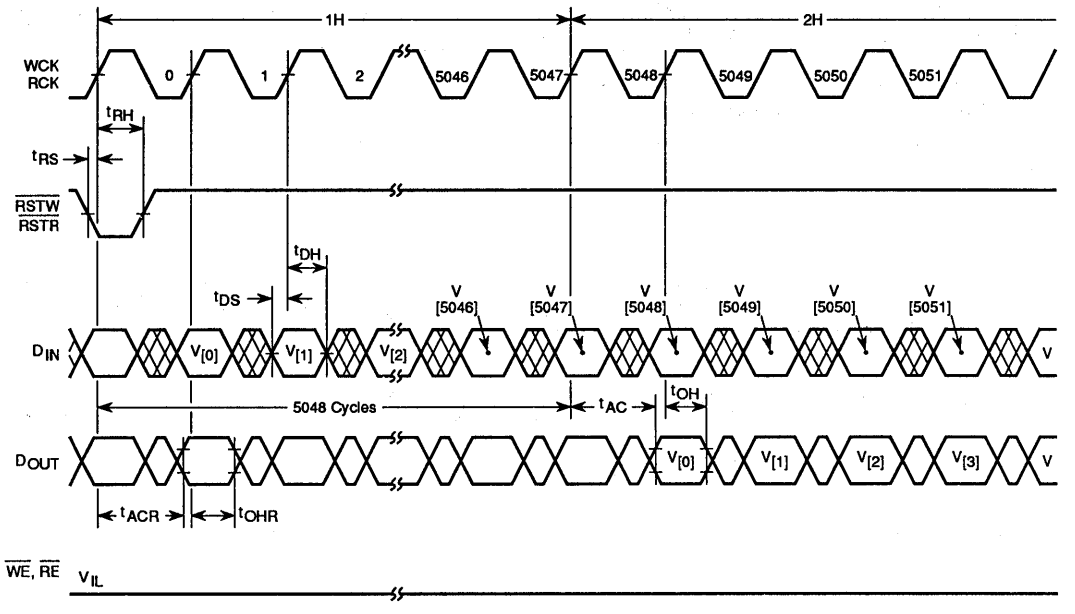
[4] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83vG-7177B

18f

Timing Waveforms (cont)

5048-Bit Delay Line Cycle



Notes:

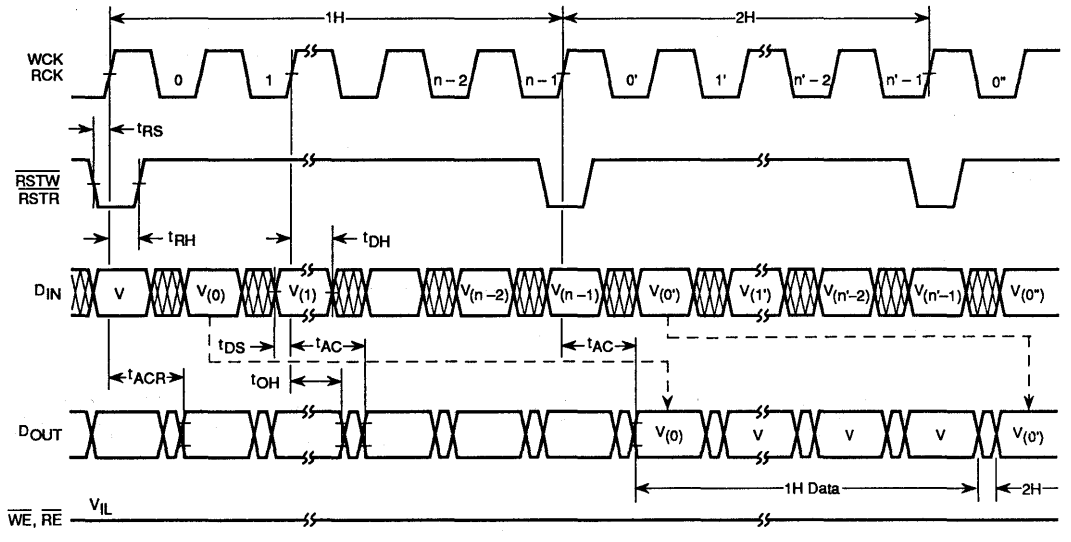
[1] V = valid data.

[2] 1H = the first group of 5048 bits.
2H = the second group of 5048 bits.

83vG-7178B

Timing Waveforms (cont)

n-Bit Delay Line Cycle



Notes:

[1] V = valid data

[2] 1H = the first group of bits. 2H = the second group of n' bits.

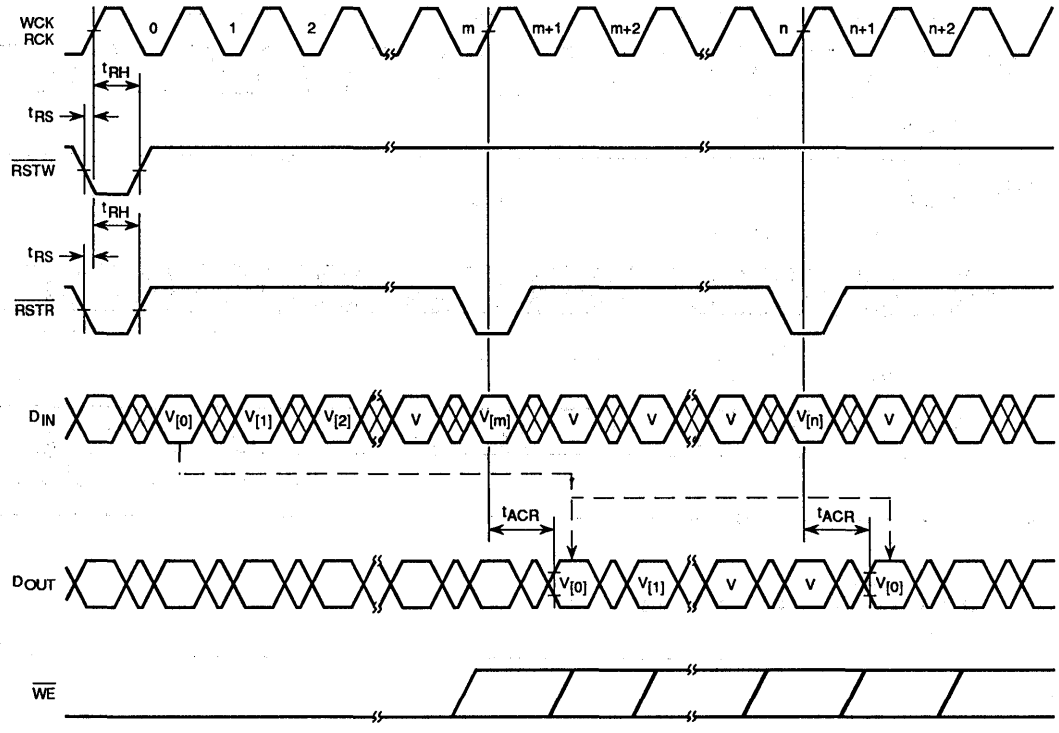
[3] $\overline{RE} = \overline{WE} = V_{IL}$.

83IH-6717B

18f

Timing Waveforms (cont)

Re-Read Cycle



Notes:

[1] $\overline{RE} = V_{IL}$

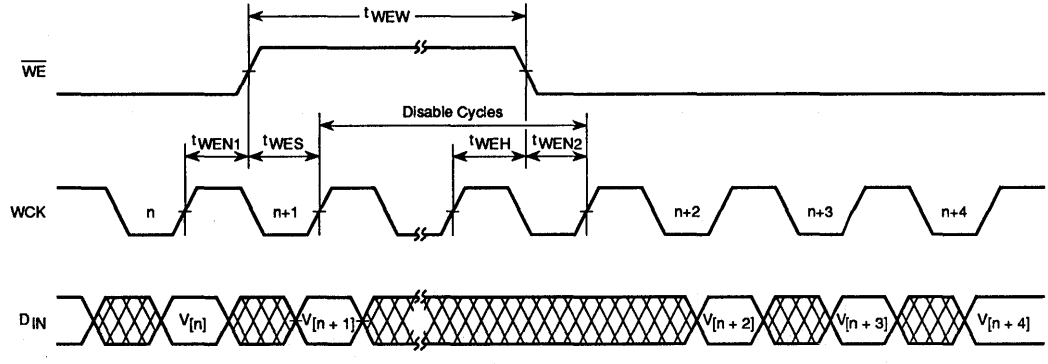
[2] V = valid data.

[3] The data stored in any location can be re-read as many times as desired, within a period of 5 ms following the writing of data into that location, provided that a second write cycle has not rewritten new data into that location.

83vG-7176B

Timing Waveforms (cont)

Write Disable Cycle

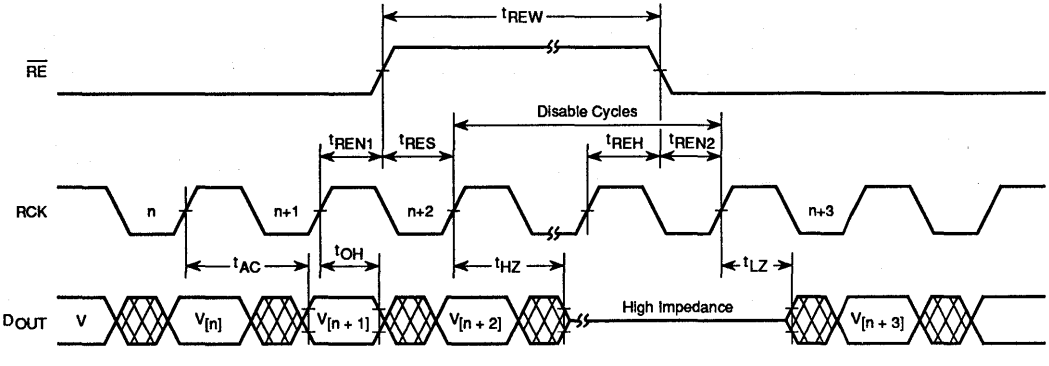


Notes:

[1] V = valid data.

83vG-7181B

Read Disable Cycle



Notes:

[1] V = valid data.

83vG-7182B

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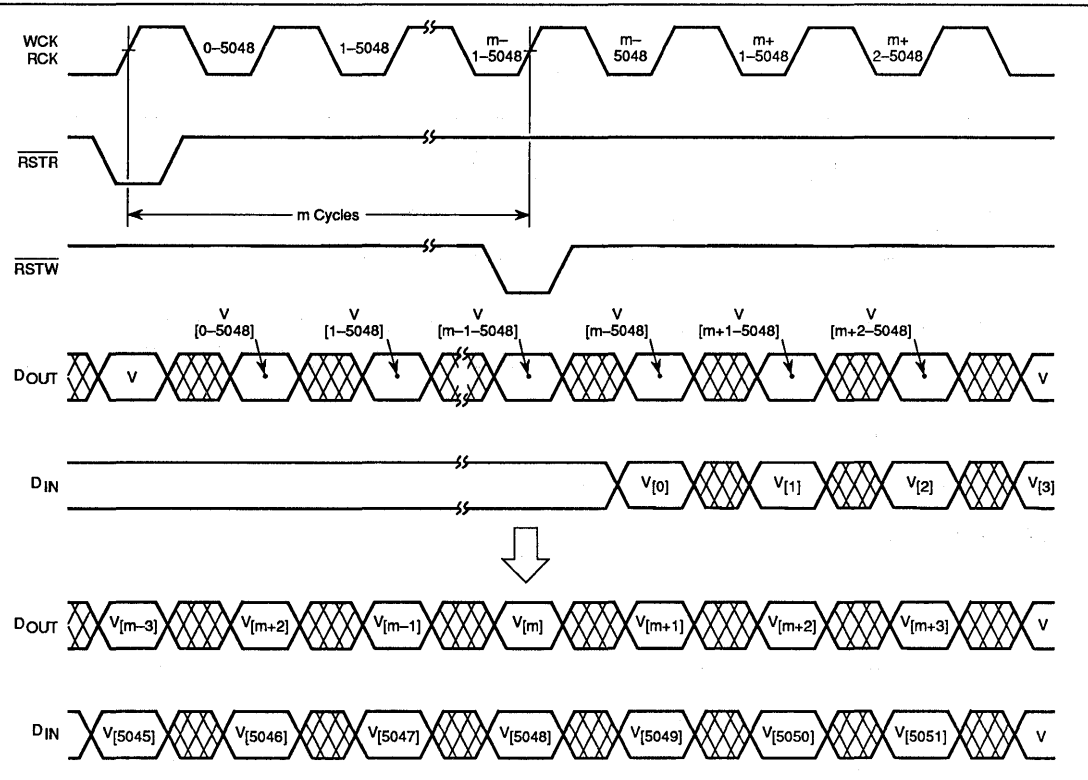
Timing Waveforms (cont)

(5048-m)-Bit Delay Line No. 1



Notes:

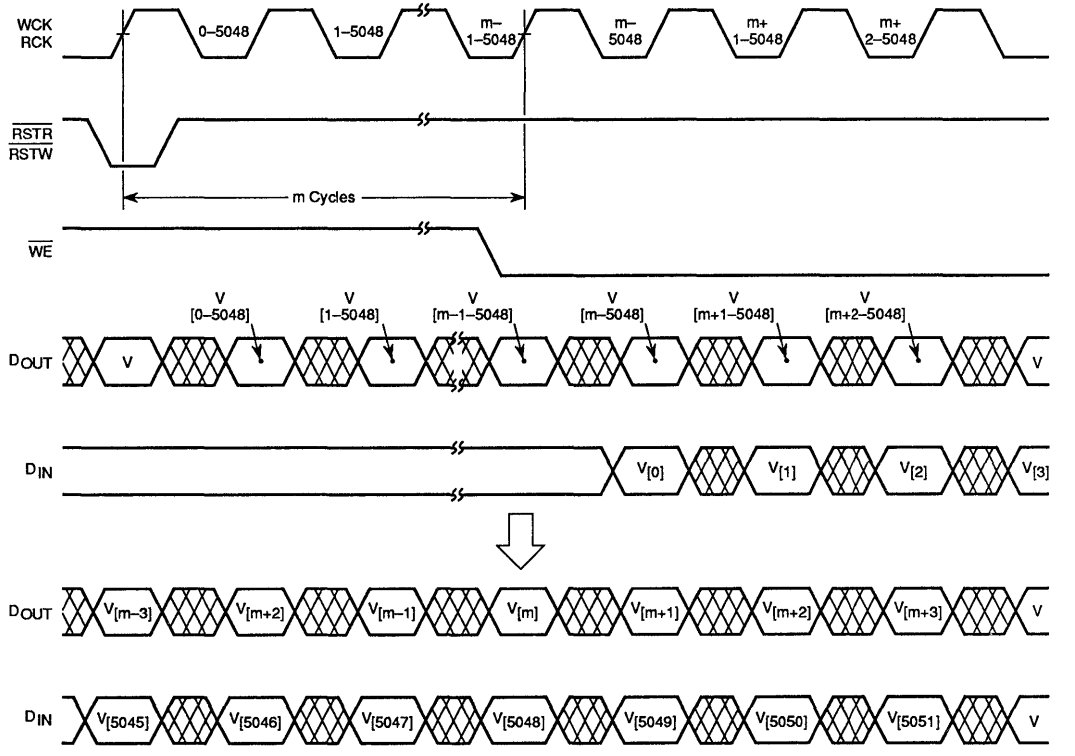
[1] $\overline{RE} = V_{IL}$.

[2] V = valid data.

83vG-7179B

Timing Waveforms (cont)

(5048-m)-Bit Delay Line No. 2



Notes:

[1] $\overline{RE} = V_{IL}$.

[2] V = valid data.

83vG-7180B

18f

μPD485505
Line Buffer for Communications Systems

Description

The μPD485505 is a 5048-word by 8-bit dual-port line buffer fabricated with a silicon-gate CMOS process. The device is capable of asynchronous read and write operation at high speed and can be used as a time axis converter or a digital delay line of up to 5048 bits (21 bits minimum at maximum frequency).

Applications include image processing in facsimile machines, plain paper copiers, video systems, and other optical scanners; time base correction in video playback systems; and data communication buffering in multiprocessor systems and local area networks.

Features

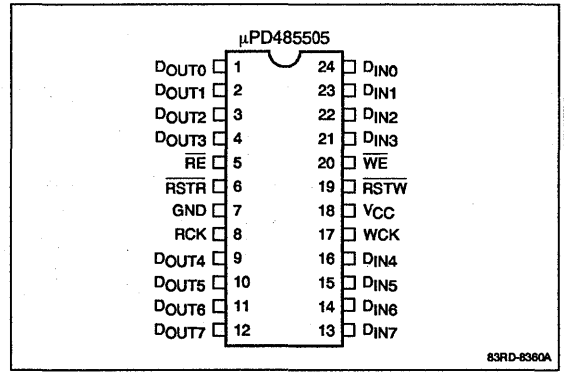
- 5048-word x 8-bit organization
- Fully static operation
- Dual-port operation
- Image processing and data communications applications
- Asynchronous and simultaneous reading/writing
- 1H (5048-bit) delay line capability
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- 24-pin plastic SOP and 24-pin plastic ZIP packaging

Ordering Information

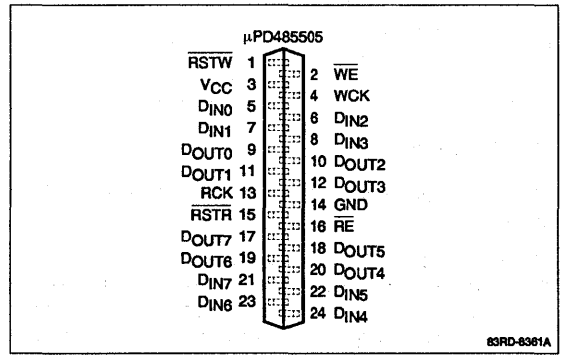
Part No.	Cycle Time (min)	Read Access Time (max)	Package
μPD485505GU-25	25 ns	18 ns	24-pin plastic SOP
GU-35	35 ns	25 ns	
μPD485505V-25	25 ns	18 ns	24-pin plastic ZIP
V-35	35 ns	25 ns	

Pin Configurations

24-Pin Plastic SOP



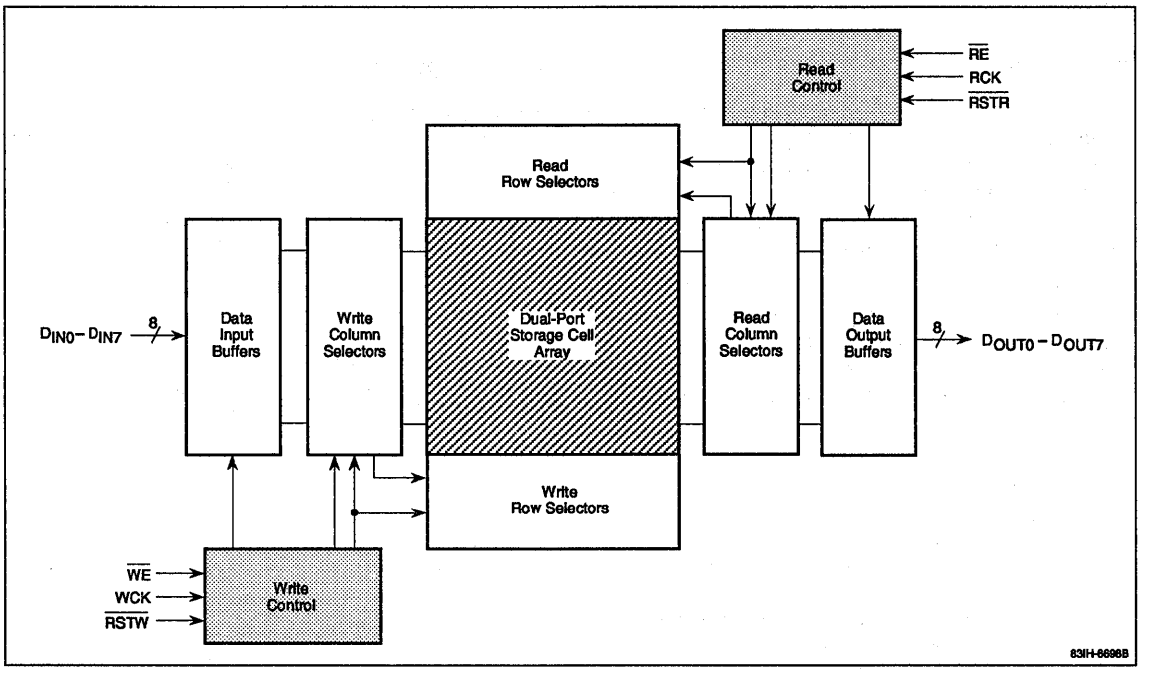
24-Pin Plastic ZIP



Pin Identification

Symbol	Function
D_{IN0} - D_{IN7}	Write data inputs
D_{OUT0} - D_{OUT7}	Read data outputs
RCK	Read clock input
$\overline{RE}$	Read enable input
$\overline{RSTR}$	Read address reset input
$\overline{RSTW}$	Write address reset input
WCK	Write clock input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply

Block Diagram



Pin Functions

D_{IN0} - D_{IN7} (Data Inputs). New data is entered on these pins.

D_{OUT0} - D_{OUT7} (Data Outputs). These three-state outputs are used to access stored information. In a simple digital delay line application, a minimum delay of 21 clock cycles is required to move data from the input pins to the output pins.

RCK (Read Clock Input). All read cycle are executed synchronously with RCK. The states of both $\overline{RSTR}$ and $\overline{RE}$ are latched by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge.

The internal read address increments with each RCK cycle unless $\overline{RE}$ is high to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 5047 to 0 and begin incrementing again.

$\overline{RE}$ (Read Enable Input). This signal controls read operation. If $\overline{RE}$ is low, all read cycles proceed. If $\overline{RE}$ is at a high level, the data outputs remain valid for that address and the internal read address stops incrementing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

$\overline{RSTR}$ (Read Address Reset Input). This signal is strobed by the rising edge of RCK and resets the internal read address to 0.

$\overline{RSTW}$ (Write Address Reset Input). Bringing this signal low resets the internal write address to 0. The state of this input is strobed by the rising edge of WCK.

WCK (Write Clock Input). All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are strobed by the rising edge of WCK at the beginning of a cycle, and the data inputs are strobed by the rising edge of WCK at the end of a cycle.

The internal write address increments with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 5047 to 0 and begin incrementing again.

$\overline{WE}$ (Write Enable Input). This input is similar to $\overline{RE}$ but controls write operation. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address does not increment. The state of $\overline{WE}$ is strobed by the rising edge of WCK.

Operation

Reset Cycle. The μPD485505 requires the initialization of internal circuits using the $\overline{RSTW}/\overline{RSTR}$ reset signals before starting operation as a time axis converter or a digital delay line.

A reset cycle can be executed at any time and does not depend on the state of $\overline{RE}$ or $\overline{WE}$. However, $\overline{RSTW}$ and $\overline{RSTR}$ must satisfy required setup and hold times as measured from the rising edges of WCK and RCK.

Write/Read Cycles. Write and read cycles are synchronized to their respective WCK/RCK inputs and executed individually when WCK or RCK is high and $\overline{WE}$ or $\overline{RE}$ is low. Write data must satisfy setup and hold times as specified from the rising edge of WCK. New data written to a particular address is available for reading after one-half write cycle plus 500 ns (maximum).

The access time of a read cycle is measured from the rising edge of RCK by t_{AC}. Stored data is read nondestructively; data can be read repeatedly because data hold time is infinite.

Time Axis Conversion. To use the μPD485505 as a time axis converter, write and read cycles must be controlled independently. Write and read ports must be initialized separately using the reset signals. Write cycles can then be executed in synchronization with WCK and write data can be stored sequentially from address 0 of this device. Afterward, when a read cycle is executed in synchronization with RCK, stored data can be read sequentially from address 0.

Since write and read cycles can be executed independently, data loaded at one arbitrary drive frequency can be read at another arbitrary drive frequency. In this sense, the μPD485505 functions as a time axis converter.

Digital Delay Line. The μPD485505 can be easily used as a digital delay line of 5048 bits or less. After the internal circuits are initialized using simultaneous $\overline{RSTW}/\overline{RSTR}$ signals, write/read cycles also may be executed simultaneously by supplying the same pulse to the write (WCK) and read (RCK) clocks. Write data is always read after the full 5048-bit delay if neither write nor read operation has been inhibited. This is the essential delay line function.

If either $\overline{WE}$ or $\overline{RE}$ is set at a nonselected (high) level for several cycles while the other is maintained in a selected (low) level, the delay line length can differ from 5048 bits.

For example, if only $\overline{WE}$ is a set to a high level (write disable) for a small number of cycles, read cycles are executed continuously and the delay line length is large. Alternatively, if only $\overline{RE}$ is set to a high level (read disable) for a small number of cycles, write cycles are executed continuously and the delay line length is small. Note that the minimum delay line length is 21 bits (for maximum frequency operation) and the maximum is 5048 bits.

A data delay of 5048 bits or less can also be obtained by applying the $\overline{RSTW}$ and $\overline{RSTR}$ signals at different times. For example, data loaded for "m" cycles after $\overline{RSTW}$ can then be read after supplying $\overline{RSTR}$. In this case, since write data can be read from the beginning after a delay of "m" cycles, the device can be used as an m-bit digital delay line.

The $\overline{RSTW}/\overline{RSTR}$ reset signals can also be simultaneously loaded at every 1H (horizontal line) period. In this case, write data loaded in the previous line cycle is read out from the beginning as read data after the reset. Therefore, a delay line length ranging from 21 to 5048 bits (depending on cycle time) can be obtained according to the length of the reset signals supplied. Refer to the timing waveform for an "n-Bit Delay Line."

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Voltage on any input pin, V_I	−0.5 to V_{CC} + 0.5 V
Voltage on any output pin, V_O	−0.5 to V_{CC} + 0.5 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter *	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_I	5	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN7}
Output capacitance	C_O	7	pF	D_{OUT0} - D_{OUT7}

* These parameters are sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}			80	mA	
Input leakage current	I_I	−10		10	μA	V_I = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD485505-25 Min	μPD485505-25 Max	μPD485505-35 Min	μPD485505-35 Max	Unit	Test Conditions
Access time	t_{AC}		18		25	ns	
Data-in hold time	t_{DH}	3		3		ns	
Data-in setup time	t_{DS}	7		10		ns	
Output disable time	t_{HZ}	5	18	5	25	ns	(Note 4)
Output active time	t_{LZ}	5	18	5	25	ns	(Note 4)
Output hold time	t_{OH}	5		5		ns	
Read clock cycle time	t_{RCK}	25		35		ns	
RCK precharge time	t_{RCP}	9		12		ns	
RCK pulse width	t_{RCW}	9		12		ns	
Read enable hold time	t_{REH}	3		3		ns	(Note 8)
Read enable high delay from RCK	t_{REN1}	3		3		ns	(Note 9)
Read enable low delay to RCK	t_{REN2}	7		10		ns	(Note 9)
Read enable setup time	t_{RES}	7		10		ns	(Note 8)
Read disable pulse width	t_{REW}	0		0		ns	
Reset active hold time	t_{RH}	3		3		ns	(Note 6)
Reset inactive hold time	t_{RN1}	3		3		ns	(Note 7)
Reset inactive setup time	t_{RN2}	7		10		ns	(Note 7)
Reset active setup time	t_{RS}	7		10		ns	(Note 6)
Read reset time	t_{RSTR}	0		0		ns	
Write reset time	t_{RSTW}	0		0		ns	
Transition time	t_T	3	35	3	35	ns	
Write clock cycle time	t_{WCK}	25		35		ns	
WCK precharge time	t_{WCP}	9		12		ns	
WCK pulse width	t_{WCW}	9		12		ns	
Write enable hold time	t_{WEH}	3		3		ns	(Note 8)
Write enable high delay from WCK	t_{WEN1}	3		3		ns	(Note 9)
Write enable low delay to WCK	t_{WEN2}	7		10		ns	(Note 9)
Write enable setup time	t_{WES}	7		10		ns	(Note 8)
Write disable pulse width	t_{WEW}	0		0		ns	

18g

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume t_T = 5 ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ±200 mV from the steady-state voltage with the load specified in figure 1. Under any conditions, $t_{LZ} \geq t_{HZ}$.

(5) Input timing reference levels = 1.5 V.

(6) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(7) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(8) If either t_{WES} or t_{WEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) output disable operations are not guaranteed.

(9) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}) is less than the specified value, internal write (read) output disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

Figure 1. Output Loads for Timing Measurements

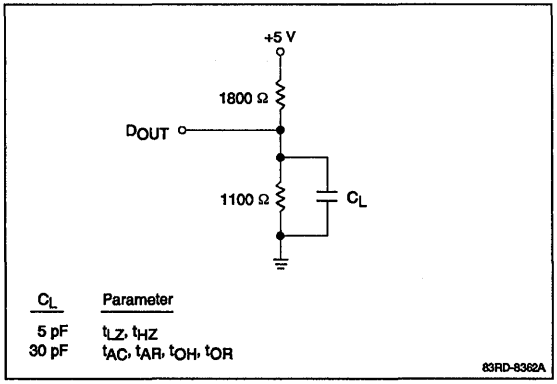
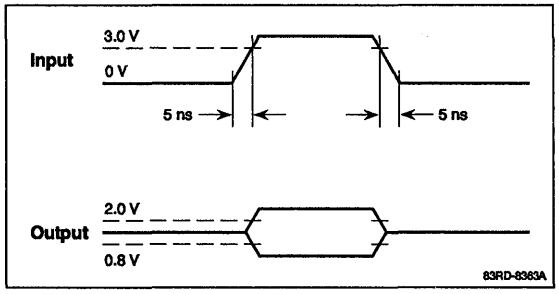
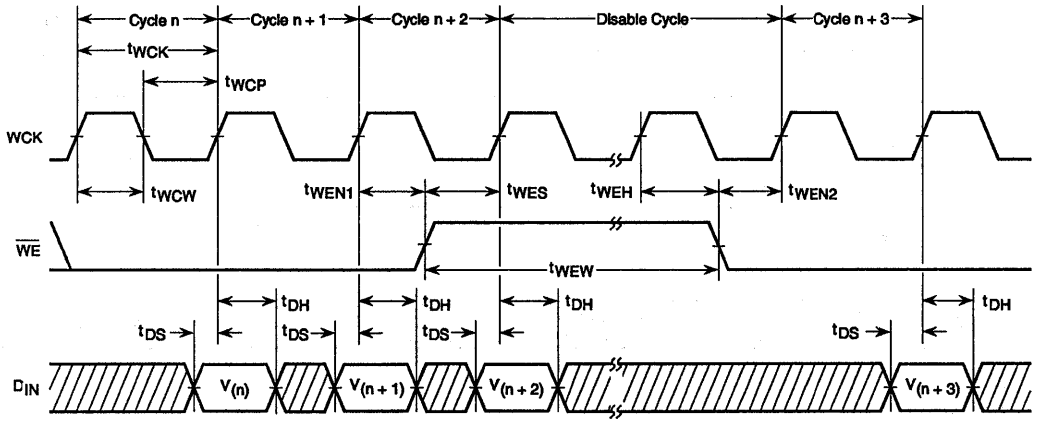


Figure 2. Voltage Thresholds for Timing Measurements



Timing Waveforms

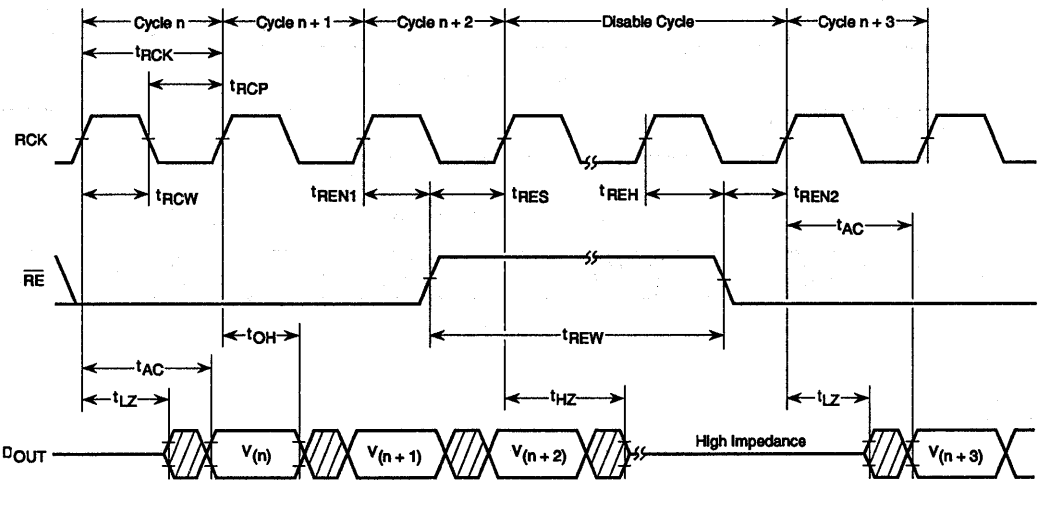
Write Cycle



Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

83IH-6704B

Read Cycle



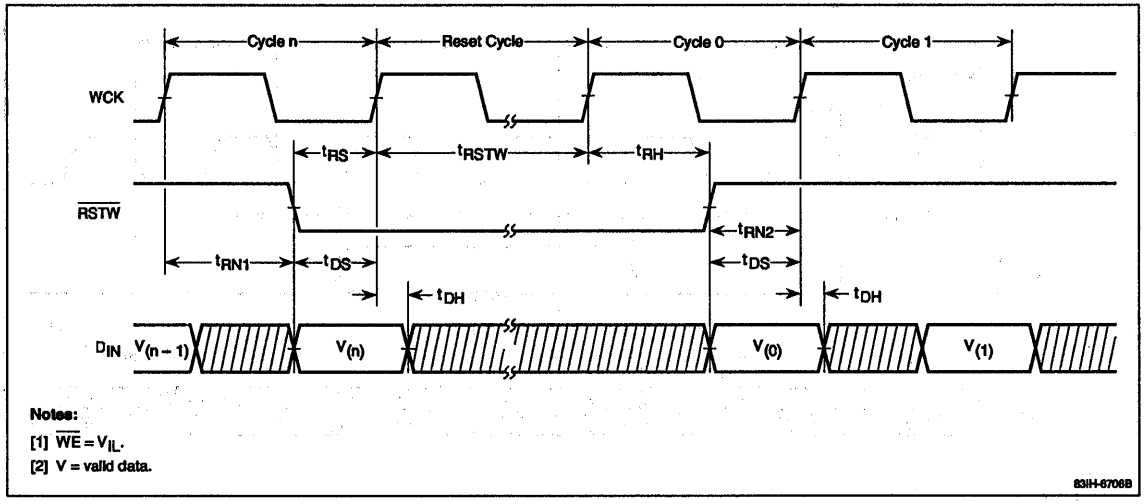
Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.

83IH-6705B

18g

Timing Waveforms (cont)

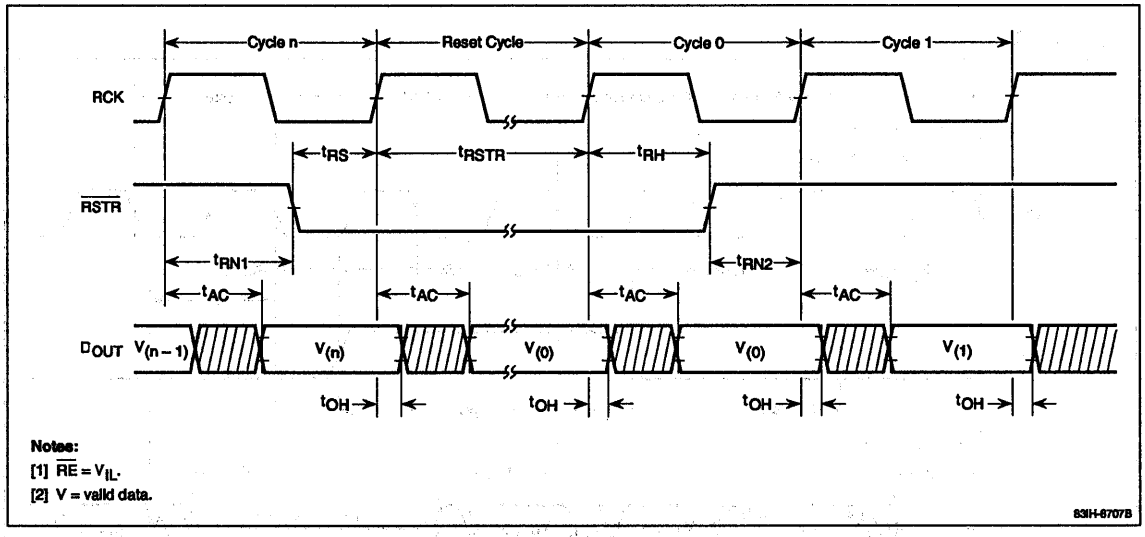
Write Reset Cycle



Notes:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

83IH-6706B

Read Reset Cycle

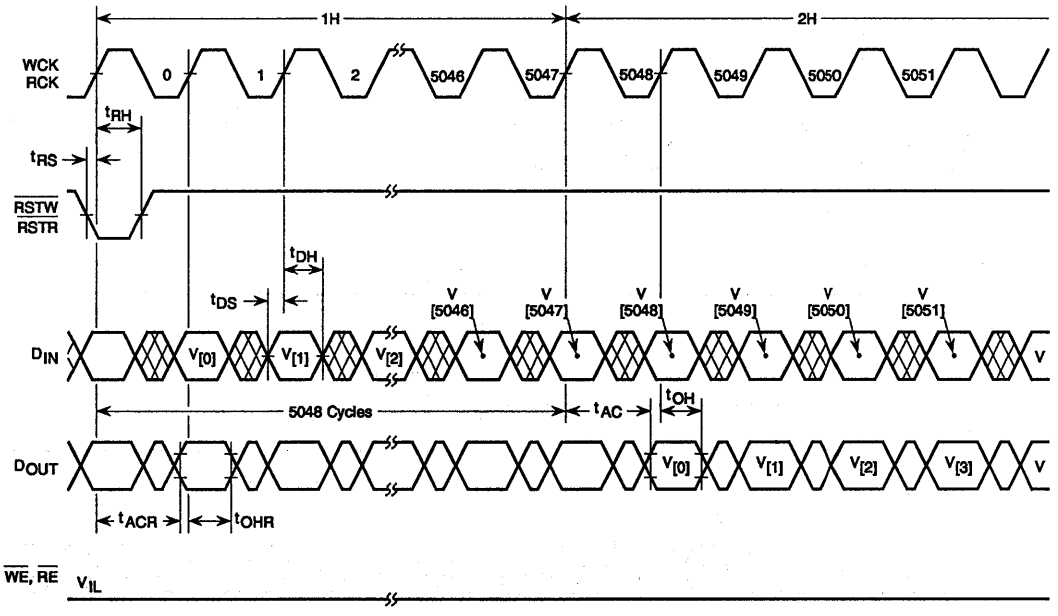


Notes:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

83IH-6707B

Timing Waveforms (cont)

5048-Bit Delay Line Cycle



Notes:

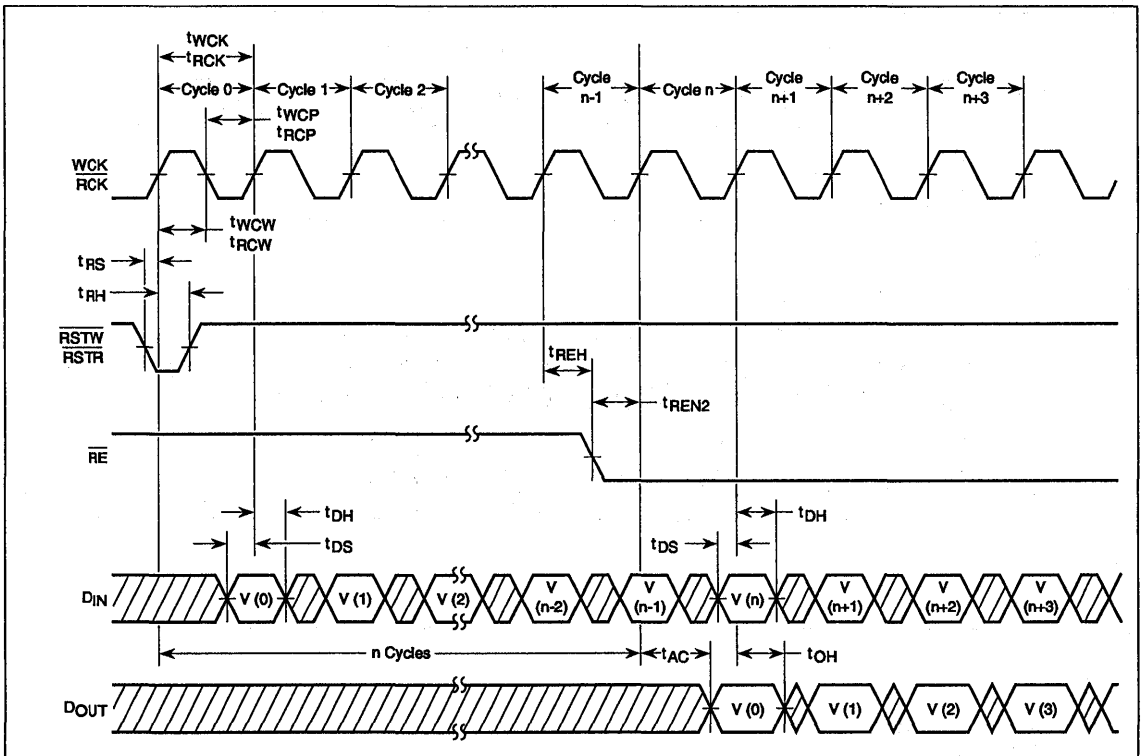
[1] V = valid data.

[2] 1H = the first group of 5048 bits.
2H = the second group of 5048 bits.

83vG-7178B

Timing Waveforms (cont)

n-Bit Delay Line Cycle 3

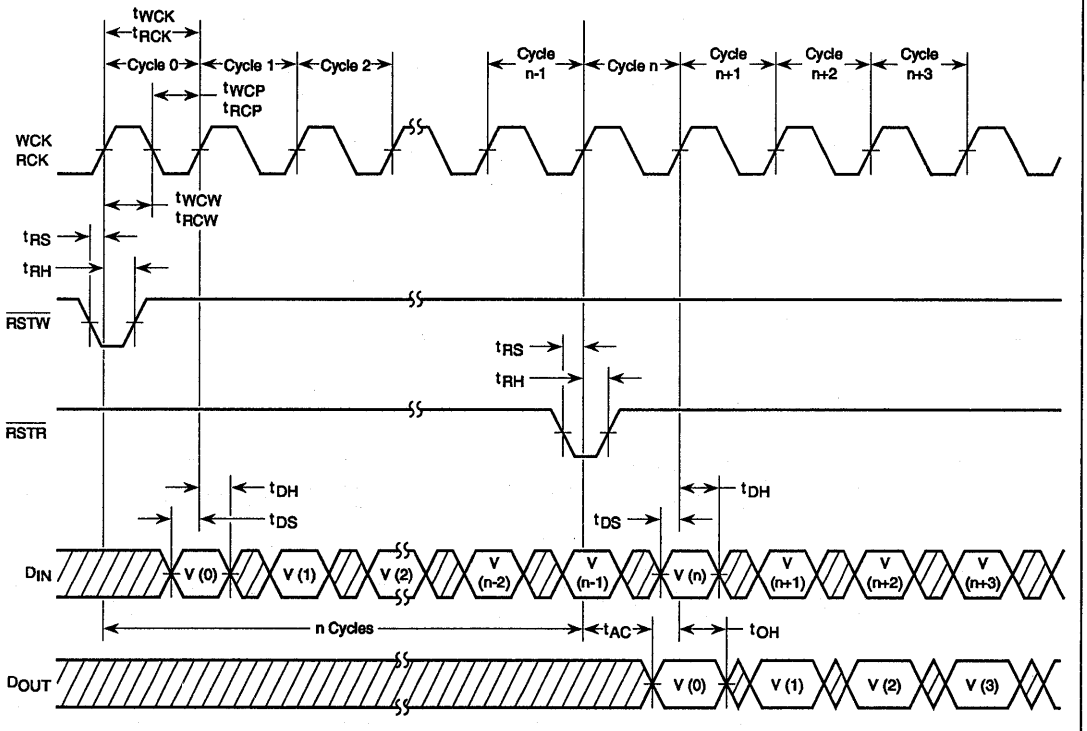


Notes:
(1) $\overline{WE} = V_{IL}$.
(2) V = valid data.

83RD-8364B

Timing Waveforms (cont)

n-Bit Delay Line Cycle 2



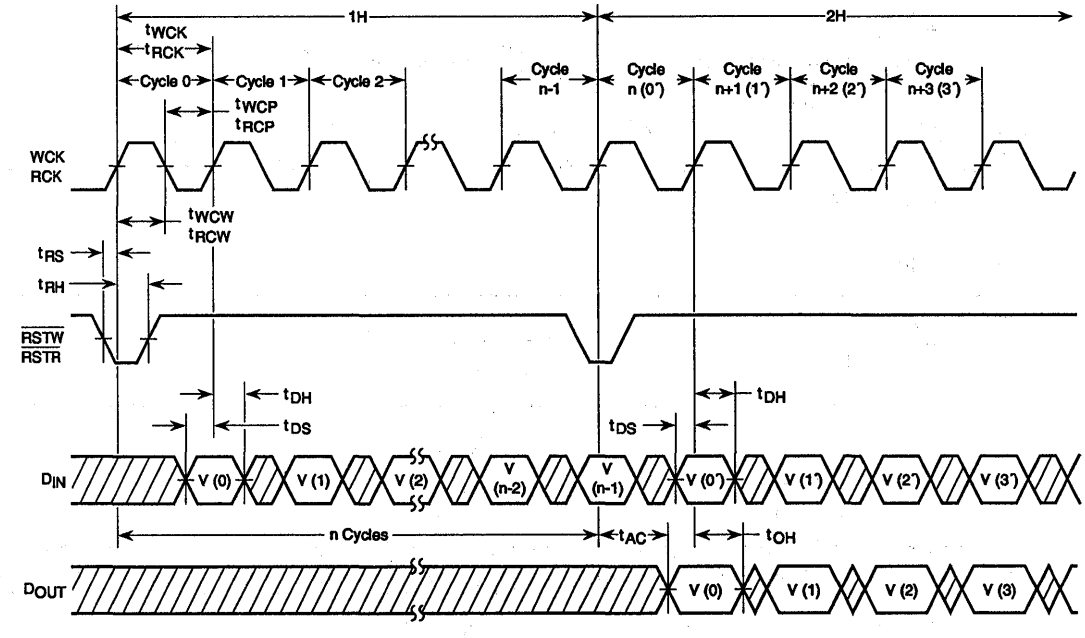
Notes:
(1) $\overline{RE} = \overline{WE} = V_{IL}$.
(2) V = valid data.

83RD-8366B

18g

Timing Waveforms (cont)

n-Bit Delay Line Cycle 1

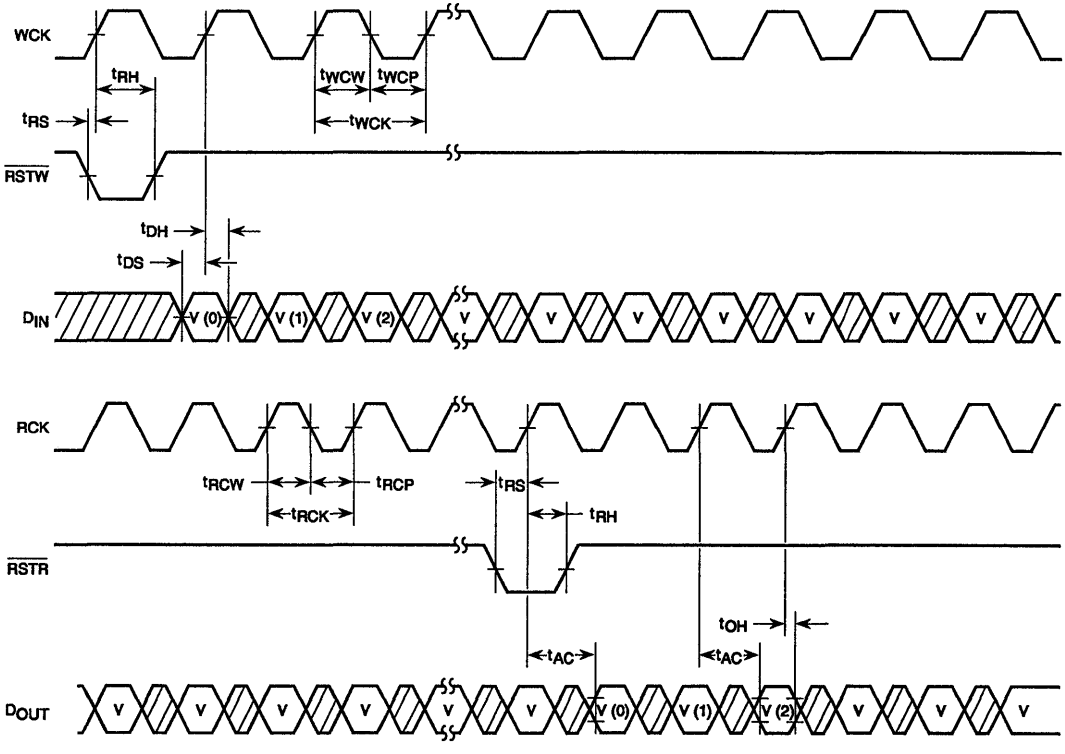


Notes:
(1) $\overline{RE} = \overline{WE} = V_{IL}$.
(2) V = valid data.

83RD-8368B

Timing Waveforms (cont)

Time Axis Conversion Cycle



Notes:
(1) $\overline{WE} = \overline{RE} = V_{IL}$.
(2) V = valid data.
(3) Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83RD-8367B

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μPD485506
Line Buffer for Communications Systems

Description

The μPD485506 is a 5048-word by 16-bit dual-port line buffer fabricated with a silicon-gate CMOS process. The device is capable of asynchronous read and write operation at high speed, and can be used as a time axis converter or a digital delay line of up to 5048 bits (21 bits minimum at maximum frequency).

Applications include image processing in facsimile machines, plain paper copiers, video systems, and other optical scanners; time base correction in video playback systems; and data communication buffering in multiprocessor systems and local area networks.

Features

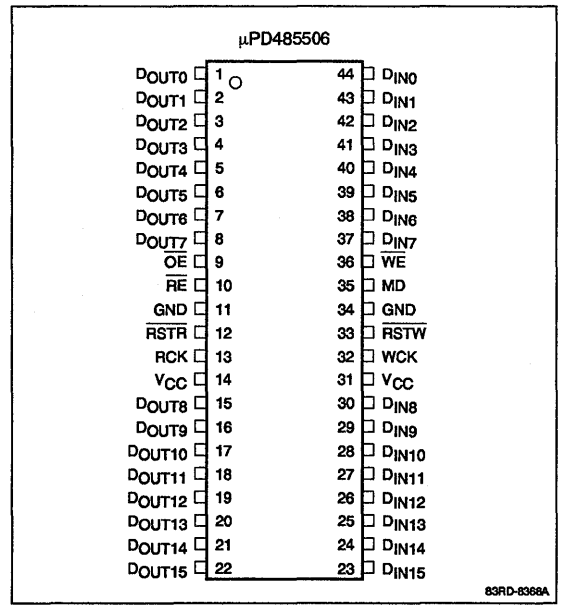
- 5048-word x 16-bit or 10,096-word x 8-bit organization
- Fully static operation; data hold time = infinity
- Dual-port operation
- Image processing and data communications applications
- Asynchronous and simultaneous reading/writing
- 1H (5048-bit) delay line capability for 5048 x 16-bit mode
- 1H (10,096-bit) delay line capability for 10,096 x 8-bit mode
- TTL-compatible inputs and outputs
- Three-state outputs
- Single +5-volt power supply
- 44-pin plastic TSOP (400-mil)

Ordering Information

Part No.	Cycle Time (min)	Read Access Time (max)	Package
μPD485506G5-25	25 ns	18 ns	44-pin plastic TSOP
G5-35	35 ns	25 ns	

Pin Configurations

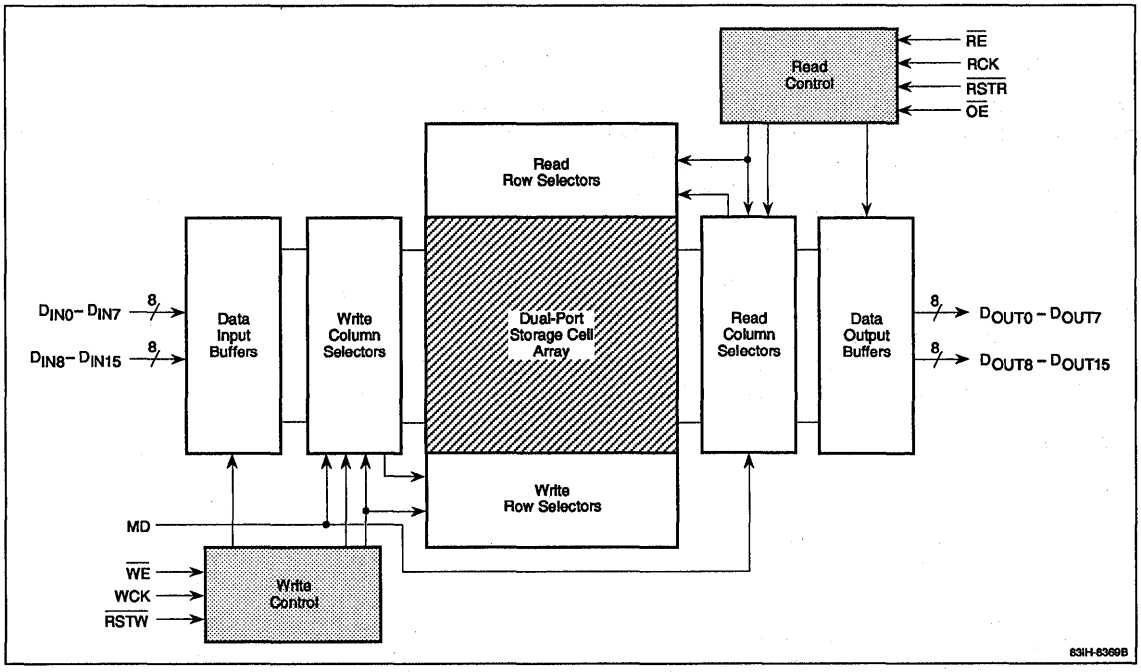
44-Pin Plastic TSOP



Pin Identification

Symbol	Function
D_{IN0} - D_{IN15}	Write data inputs
D_{OUT0} - D_{OUT15}	Read data outputs
MD	Mode set input
$\overline{OE}$	Output enable
RCK	Read clock input
$\overline{RE}$	Read enable input
$\overline{RSTR}$	Read address reset input
$\overline{RSTW}$	Write address reset input
WCK	Write clock input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply

Block Diagram



Pin Functions

D_{IN0} - D_{IN15} (Data Inputs). New data is entered on these pins.

D_{OUT0} - D_{OUT15} (Data Outputs). These three-state outputs are used to access stored information. In a simple digital delay line application, a minimum delay of 21 clock cycles is required to move data from the input pins to the output pins.

MD (Mode Set Input). The level of this signal gives the operation mode. A low level enables 5048-word by 16-bit memory configuration with D_{IN0} - D_{IN15} and D_{OUT0} - D_{OUT15}. On the other hand, a high level enables 10,096-word by 8-bit memory configuration with D_{IN0} - D_{IN7} and D_{OUT0} - D_{OUT7}. This signal is latched by the rising edge of WCK (RCK) when $\overline{RSTW}$ ($\overline{RSTR}$) is low level. Mode setting can be done Write/Read separately.

$\overline{OE}$ (Output Enable Input). This signal controls output operation. The state of $\overline{OE}$ is latched by the rising edge of RCK. If $\overline{OE}$ is at a high level, the data outputs become high impedance.

RCK (Read Clock Input). All read cycle are executed synchronously with RCK. The states of $\overline{RSTR}$, $\overline{RE}$, and $\overline{OE}$ are latched by the rising edge of RCK at the beginning of a cycle. This same edge of RCK starts internal read operation, and access time is referenced to this edge.

The internal read address increments with each RCK cycle unless $\overline{RE}$ is high to hold the read address constant. Unless inhibited by $\overline{RE}$, the internal read address will automatically wrap around from 5047 to 0 or 10,095 to 0 and begin incrementing again.

$\overline{RE}$ (Read Enable Input). This signal controls read operation. If $\overline{RE}$ is low, all read cycles proceed. If $\overline{RE}$ is at a high level, the data outputs remain valid for that address and the internal read address stops incrementing. The state of $\overline{RE}$ is strobed by the rising edge of RCK.

$\overline{RSTR}$ (Read Address Reset Input). This signal is latched by the rising edge of RCK and resets the internal read address to 0.

$\overline{RSTW}$ (Write Address Reset Input). Bringing this signal low resets the internal write address to 0. The state of this input is latched by the rising edge of WCK.

WCK (Write Clock Input). All write cycles are executed synchronously with WCK. The states of both $\overline{RSTW}$ and $\overline{WE}$ are latched by the rising edge of WCK at the beginning of a cycle, and the data inputs are latched by the rising edge of WCK at the end of a cycle.

The internal write address increments with each WCK cycle unless $\overline{WE}$ is at a high level to hold the write address constant. Unless inhibited by $\overline{WE}$, the internal write address will automatically wrap around from 5047 to 0 (5048-word by 16-bit mode) or 10,095 to 0 (10,096-word by 8-bit mode) and begin incrementing again.

$\overline{WE}$ (Write Enable Input). This signal controls write operation. If $\overline{WE}$ is at a high level, no data is written to storage cells and the write address does not increment. The state of $\overline{WE}$ is latched by the rising edge of WCK.

Operation

Reset Cycle. The μPD485506 requires the initialization of internal circuits using the $\overline{RSTW}/\overline{RSTR}$ reset signals before starting operation as a time axis converter or a digital delay line.

A reset cycle can be executed at any time and does not depend on the state of $\overline{OE}$, $\overline{RE}$, or $\overline{WE}$. However, $\overline{RSTW}$ and $\overline{RSTR}$ must satisfy required setup and hold times as measured from the rising edges of WCK and RCK.

Write/Read Cycles. Write and read cycles are synchronized to their respective WCK/RCK inputs when $\overline{WE}$ or $\overline{RE}$ is low. Write data must satisfy setup and hold times as specified from the rising edge of WCK. New data written to a particular address is available for reading synchronously with the RCK clock after one-half write cycle plus 500 ns (maximum).

The access time of a read cycle is measured from the rising edge of RCK by t_{AC}. Stored data is read nondestructively; data can be read repeatedly because data hold time is infinite.

Time Axis Conversion. To use the μPD485506 as a time axis converter, write and read cycles must be controlled independently. Write and read ports must be initialized separately using the reset signals. Write cycles can then be executed in synchronization with WCK and write data can be stored sequentially from address 0 of this device. Afterward, when a read cycle is executed in synchronization with RCK, stored data can be read sequentially from address 0.

Since write and read cycles can be executed independently, data loaded at one arbitrary drive frequency can be read at another arbitrary drive frequency. In this sense, the μPD485506 functions as a time axis converter.

Digital Delay Line. The μPD485506 can be easily used as a digital delay line of 5048 bits in the case of 5048-word by 16-bit mode or 10,096 bits in the case of 10,096-word by 8-bit mode. After the internal circuits are initialized using simultaneous $\overline{RSTW}/\overline{RSTR}$ signals, write/read cycles also may be executed simultaneously by supplying the same pulse to the write (WCK) and read (RCK) clocks. Write data is always read after the full 5048-bit or 10,096-bit delay if neither write nor read operation has been inhibited. This is the essential delay line function.

If either $\overline{WE}$ or $\overline{RE}$ is set at a disabled (high) level for several cycles while the other is maintained in a selected (low) level, the delay line length can differ from 5048 bits or 10,096 bits. For example, if only $\overline{WE}$ is set to a high level (write disable) for a small number of cycles, read cycles are executed continuously and the delay line length is large . Alternatively, if only $\overline{RE}$ is set to a high level (read disable) for a small number of cycles, write cycles are executed continuously and the delay line length is small. Note that the minimum delay line length is 21 bits (for maximum frequency operation) and the maximum is 5048 bits or 10,096 bits.

A data delay of 5048 bits or less or 10,096 bits or less can also be obtained by applying the $\overline{RSTW}$ and $\overline{RSTR}$ signals at different times. For example, data loaded for "m" cycles after $\overline{RSTW}$ can then be read after supplying $\overline{RSTR}$. In this case, since write data can be read from the beginning after a delay of "m" cycles, the device can be used as an m-bit digital delay line.

The $\overline{RSTW}/\overline{RSTR}$ reset signals can also be simultaneously loaded at every 1H (horizontal line) period. In this case, write data loaded in the previous line cycle is read out from the beginning as read data after the reset. Therefore, a delay line length ranging from 21 to 5048 bits (or 10,096 bits) in the case of 25-ns cycle time and from 15 to 5048 bits (or 10,096 bits) in the case of 35-ns cycle time can be obtained according to the length of the reset signals supplied. Refer to the timing waveform for an "n-Bit Delay Line."

Mode Set Cycle. The μPD485506 has a capability of changing the memory configuration by judging the MD level latched by the rising edge of RCK/WCK at the Reset cycle ($\overline{RSTR}/\overline{RSTW}$ is low). If MD level is low, the memory is set to the 5048-word by 16-bit configuration, and if MD level is high, it is set to the 10,096-word by 8-bit configuration. The write mode set and read mode set can be done separately.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Voltage on any input pin, V_I	−0.5 to V_{CC} + 0.5 V
Voltage on any output pin, V_O	−0.5 to V_{CC} + 0.5 V
Short-circuit output current, I_{OS}	20 mA
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 0.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; V_{CC} = +5.0 V ±10%; f = 1 MHz

Parameter *	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_I	7	pF	$\overline{WE}$, $\overline{RE}$, WCK, RCK, MD $\overline{RSTW}$, $\overline{RSTR}$, D_{IN0} - D_{IN15}, $\overline{OE}$
Output capacitance	C_O	7	pF	D_{OUT0} - D_{OUT15}

* These parameters are sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Write/read cycle operating current	I_{CC}			140	mA	
Input leakage current	I_I	−10		10	μA	V_I = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_O	−10		10	μA	D_{OUT} disabled; V_O = 0 to 5.5 V
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1 mA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD485506-25		μPD485506-35			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Access time	t_{AC}		18		25	ns	
Data-in hold time	t_{DH}	3		3		ns	
Data-in setup time	t_{DS}	7		10		ns	
Output disable time	t_{HZ}	5	18	5	25	ns	(Note 4)
Output disable time at the mode change	t_{HZM}	5	18	5	25	ns	(Note 4)
Output active time	t_{LZ}	5	18	5	25	ns	(Note 4)
Output active time at the mode change	t_{LZM}	5	18	5	25	ns	(Note 4)
Mode set time	t_{MD}	0		0		ns	(Note 10)
Mode set hold time	t_{MH}	10		10		ns	(Note 10)
Mode set setup time	t_{MS}	20		20		ns	(Note 10)
Output enable hold time	t_{OEH}	3		3		ns	(Note 8)
Output enable high delay from RCD	t_{OEN1}	3		3		ns	(Note 9)

AC Characteristics (cont)

Parameter	Symbol	μPD485506-25 Min	μPD485506-25 Max	μPD485506-35 Min	μPD485506-35 Max	Unit	Test Conditions
Output enable low delay to RCK	t_{OEN2}	7		10		ns	(Note 9)
Output enable setup time	t_{OES}	7		10		ns	(Note 8)
Output disable pulse width	t_{OEW}	0		0		ns	
Output hold time	t_{OH}	5		5		ns	
Read clock cycle time	t_{RCK}	25		35		ns	
RCK precharge time	t_{RCP}	9		12		ns	
RCK pulse width	t_{RCW}	9		12		ns	
Read enable hold time	t_{REH}	3		3		ns	(Note 8)
Read enable high delay from RCK	t_{REN1}	3		3		ns	(Note 9)
Read enable low delay to RCK	t_{REN2}	7		10		ns	(Note 9)
Read enable setup time	t_{RES}	7		10		ns	(Note 8)
Read disable pulse width	t_{REW}	0		0		ns	
Reset active hold time	t_{RH}	3		3		ns	(Note 6)
Reset inactive hold time	t_{RN1}	3		3		ns	(Note 7)
Reset inactive setup time	t_{RN2}	7		10		ns	(Note 7)
Reset active setup time	t_{RS}	7		10		ns	(Note 6)
Read reset time	t_{RSTR}	0		0		ns	
Write reset time	t_{RSTW}	0		0		ns	
Transition time	t_T	3	35	3	35	ns	
Write clock cycle time	t_{WCK}	25		35		ns	
WCK precharge time	t_{WCP}	9		12		ns	
WCK pulse width	t_{WCW}	9		12		ns	
Write enable hold time	t_{WEH}	3		3		ns	(Note 8)
Write enable high delay from WCK	t_{WEN1}	3		3		ns	(Note 9)
Write enable low delay to WCK	t_{WEN2}	7		10		ns	(Note 9)
Write enable setup time	t_{WES}	7		10		ns	(Note 8)
Write disable pulse width	t_{WEW}	0		0		ns	

Notes:

(1) All voltages are referenced to ground.

(2) Input pulse rise and fall times assume $t_T = 5$ ns.

(3) Input pulse levels = GND to 3 V. Transition times are measured between 3 V and 0 V.

(4) This delay is measured at ±200 mV from the steady-state voltage with the load specified in figure 1. Under any conditions, $t_{LZ} \geq t_{HZ}$ and $t_{LZM} \geq t_{HZM}$.

(5) Input timing reference levels = 1.5 V.

(6) If either t_{RS} or t_{RH} is less than the specified value, reset operations are not guaranteed.

(7) If either t_{RN1} or t_{RN2} is less than the specified value, internal reset operations may extend to cycles immediately preceding or following the period of desired reset operations.

(8) If either t_{WES}, t_{WEH}, t_{OES} or t_{OEH} (t_{RES} or t_{REH}) is less than the specified value, write (read) output disable operations are not guaranteed.

(9) If either t_{WEN1} or t_{WEN2} (t_{REN1} or t_{REN2}, t_{OEN1} or t_{OEN2}) is less than the specified value, internal write (read) output disable operations may extend to cycles immediately preceding or following the period of desired disable operations.

(10) Mode Set signal (MD) must be input synchronously with Write Reset signal (t_{RSTW} period) or Read Reset signal (t_{RSTR} period).

18h

Figure 1. Output Loads for Timing Measurements

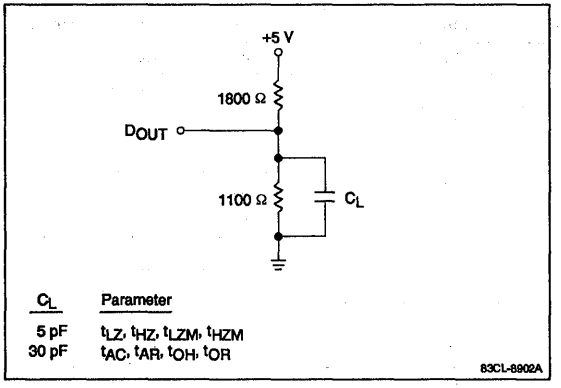
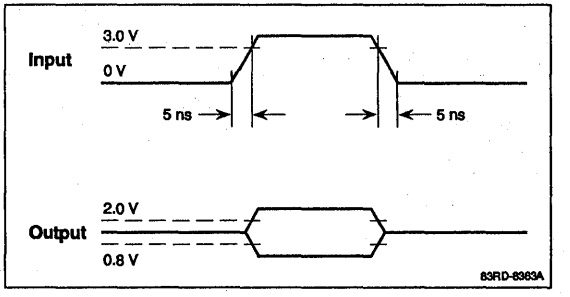
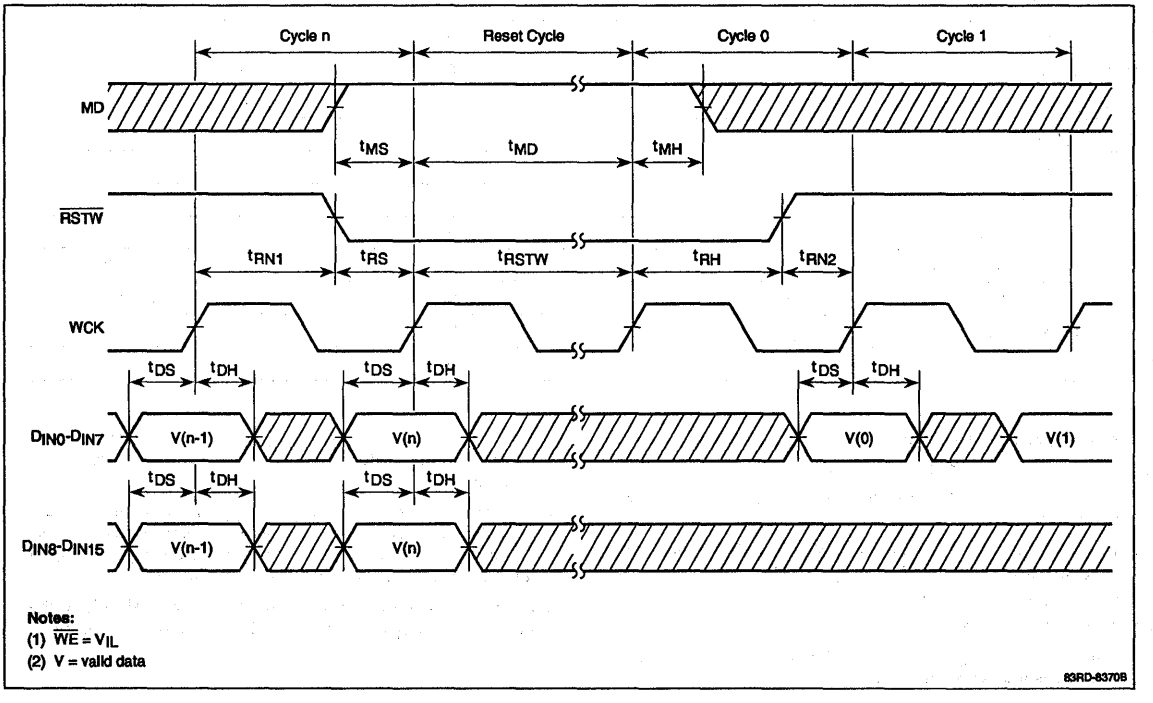


Figure 2. Voltage Thresholds for Timing Measurements



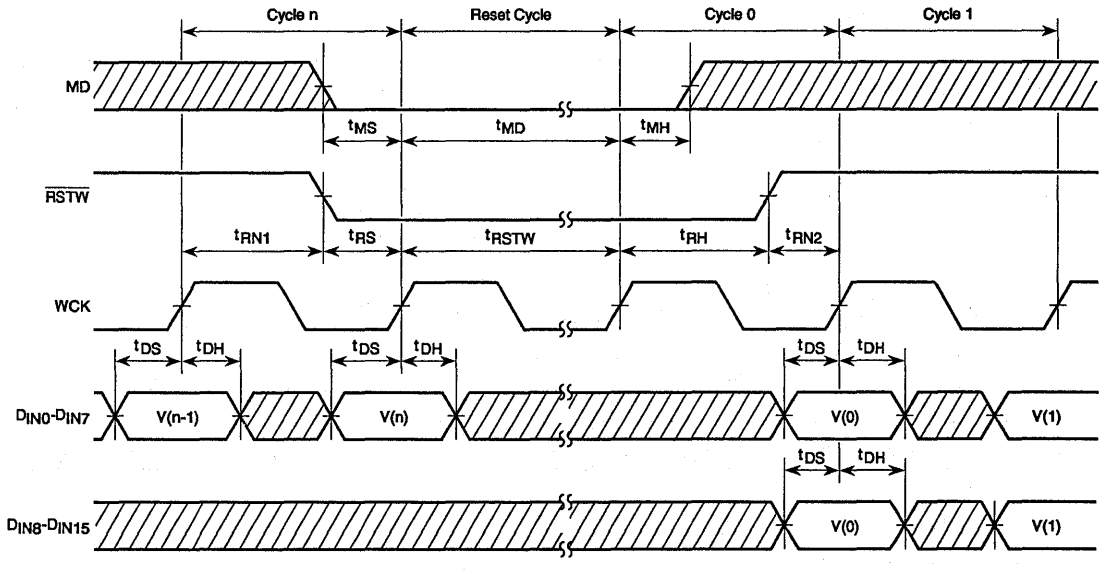
Timing Waveforms

Mode Set Cycle (Write) 1



Timing Waveforms (cont)

Mode Set Cycle (Write) 2

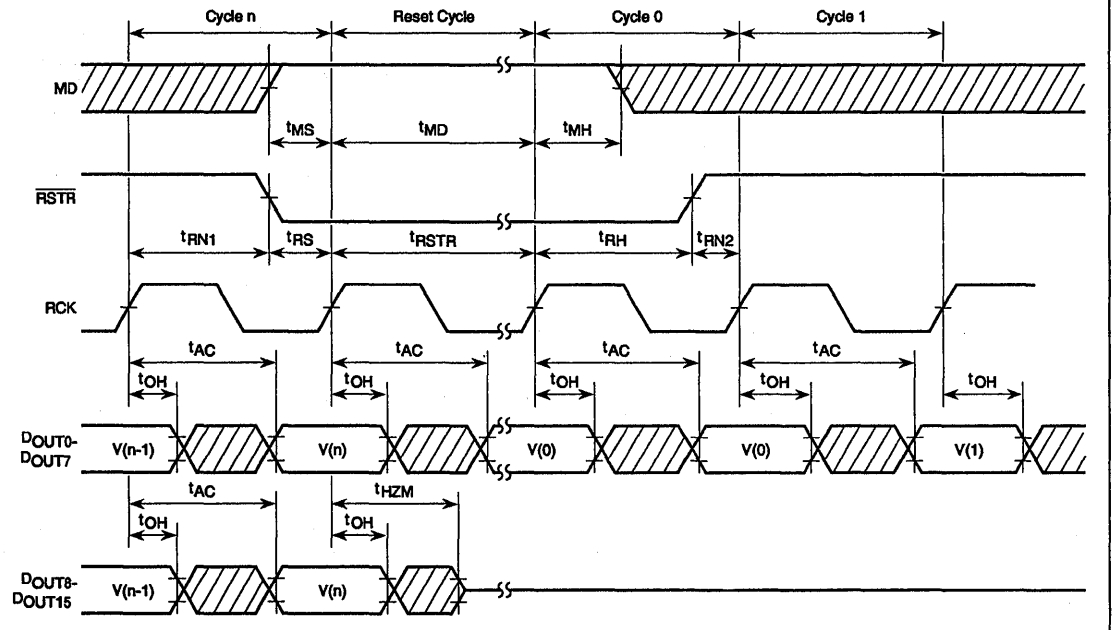


Notes:
(1) $\overline{WE}$ = V_{IL}
(2) V = valid data

83RD-6371B

Timing Waveforms (cont)

Mode Set Cycle (Read) 3

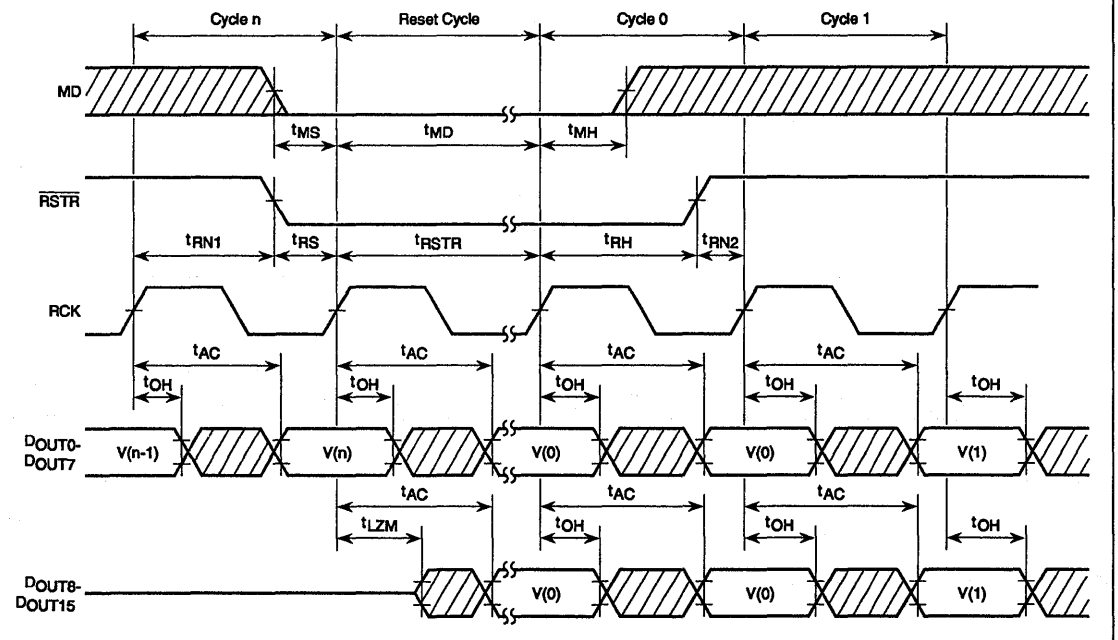


Notes:
(1) $\overline{RE} = \overline{OE} = V_{IL}$
(2) V = valid data

83RD-83728

Timing Waveforms (cont)

Mode Set Cycle (Read) 4

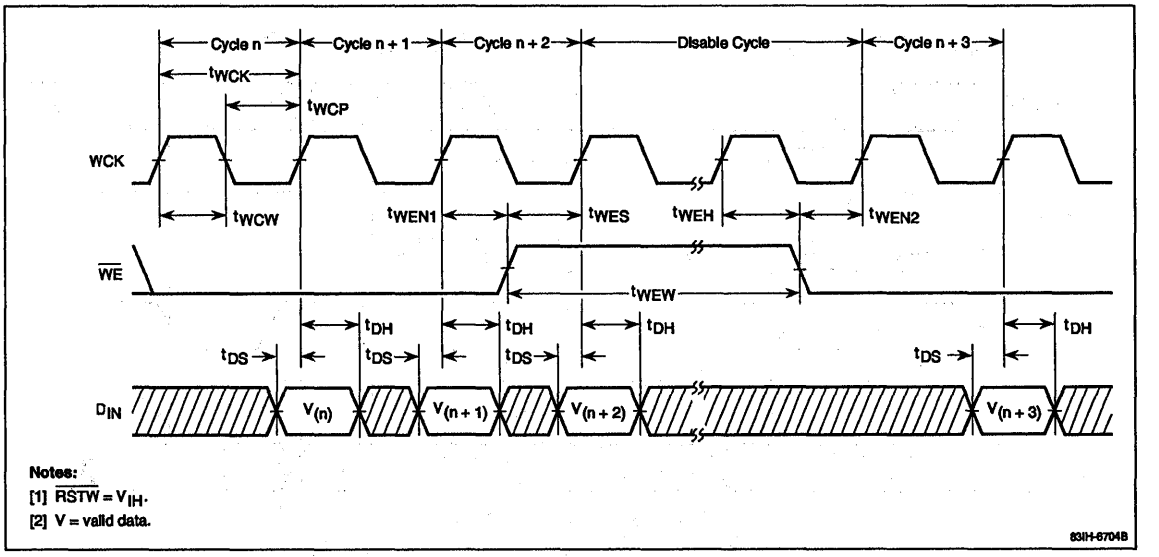


Notes:
(1) $\overline{RE} = \overline{OE} = V_{IL}$
(2) V = valid data

83RD-83738

Timing Waveforms (cont)

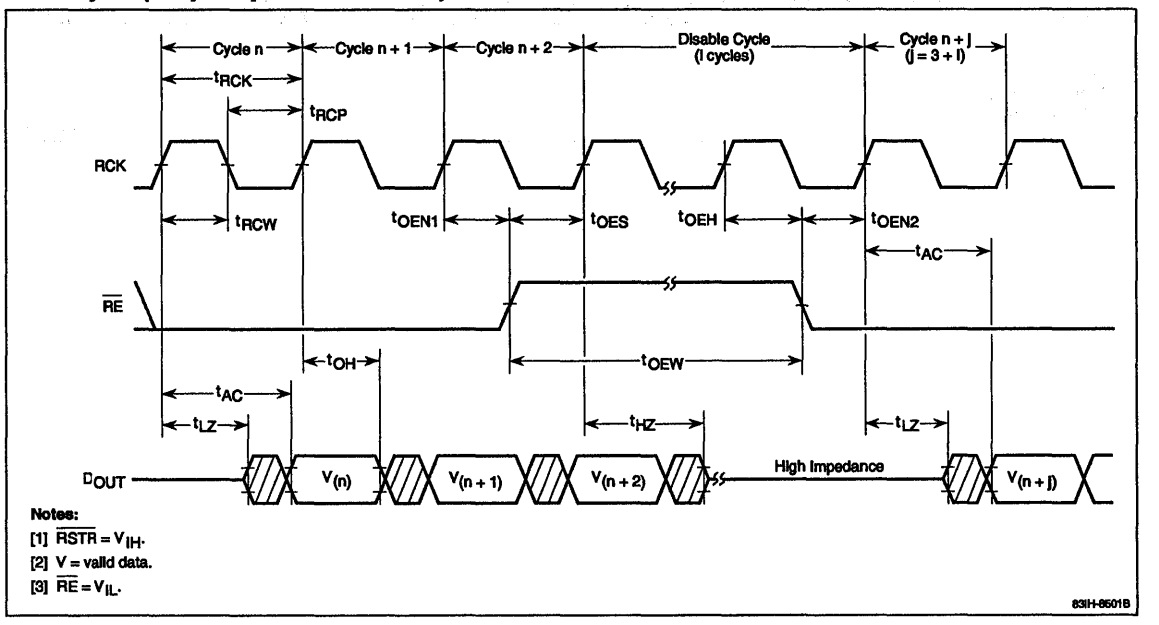
Write Cycle



Notes:
[1] $\overline{RSTW} = V_{IH}$.
[2] V = valid data.

83IH-6704B

Read Cycle (Output Operation Control)

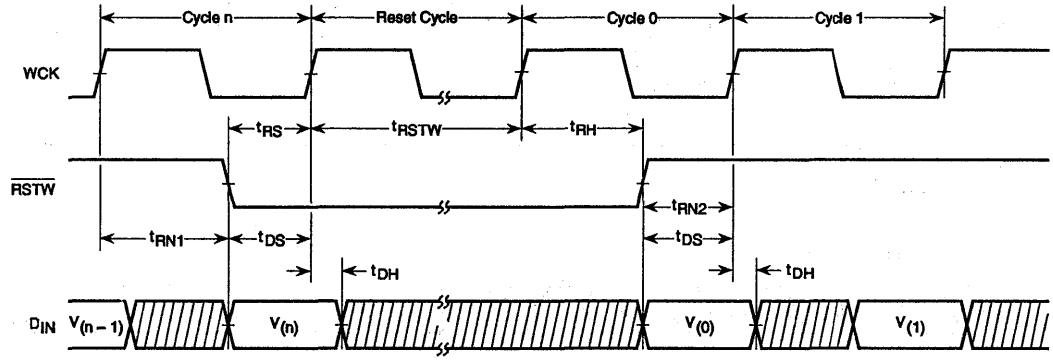


Notes:
[1] $\overline{RSTR} = V_{IH}$.
[2] V = valid data.
[3] $\overline{RE} = V_{IL}$.

83IH-8501B

Timing Waveforms (cont)

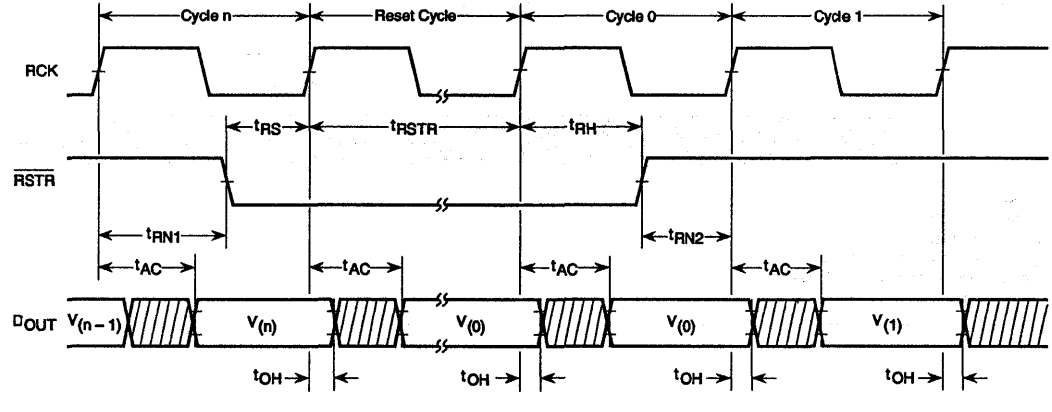
Write Reset Cycle



Notes:
[1] $\overline{WE} = V_{IL}$.
[2] V = valid data.

83IH-6706B

Read Reset Cycle



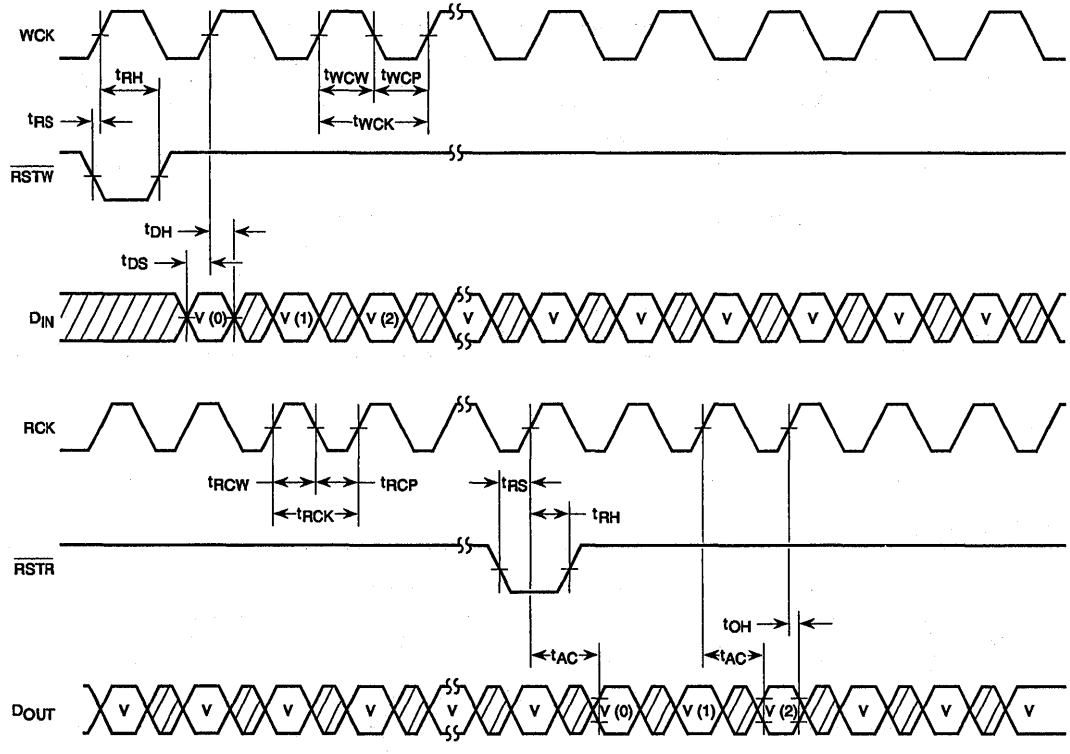
Notes:
[1] $\overline{RE} = V_{IL}$.
[2] V = valid data.

83IH-6707B

18h

Timing Waveforms (cont)

Time Axis Conversion Cycle

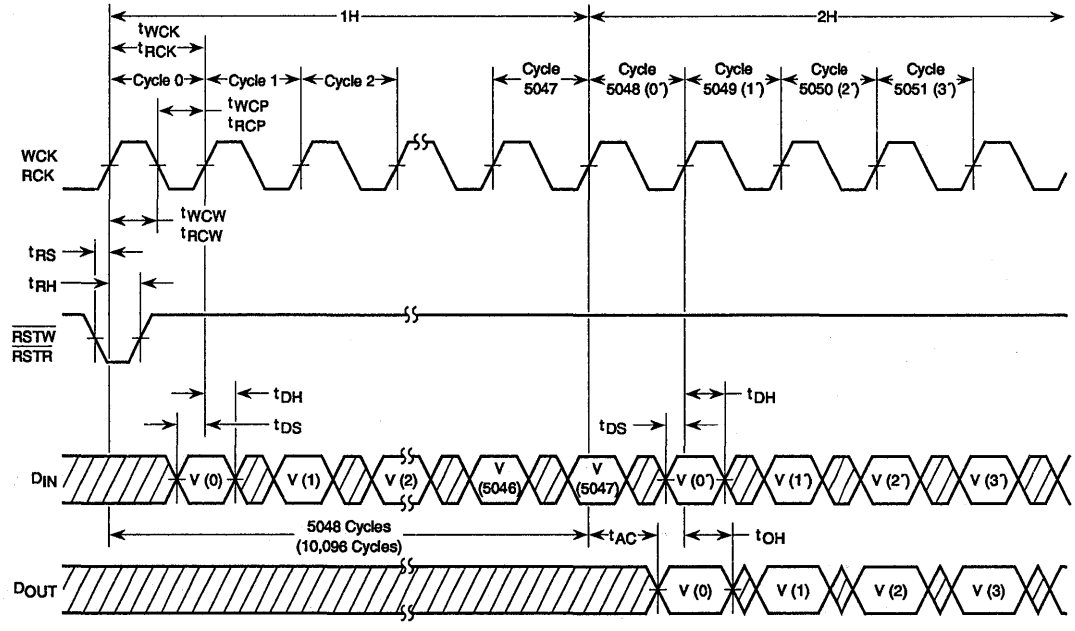


Notes:
(1) $\overline{WE} = \overline{RE} = \overline{OE} = V_{IL}$.
(2) V = valid data.
(3) Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

83RD-8374B

Timing Waveforms (cont)

1H Delay Line Cycle



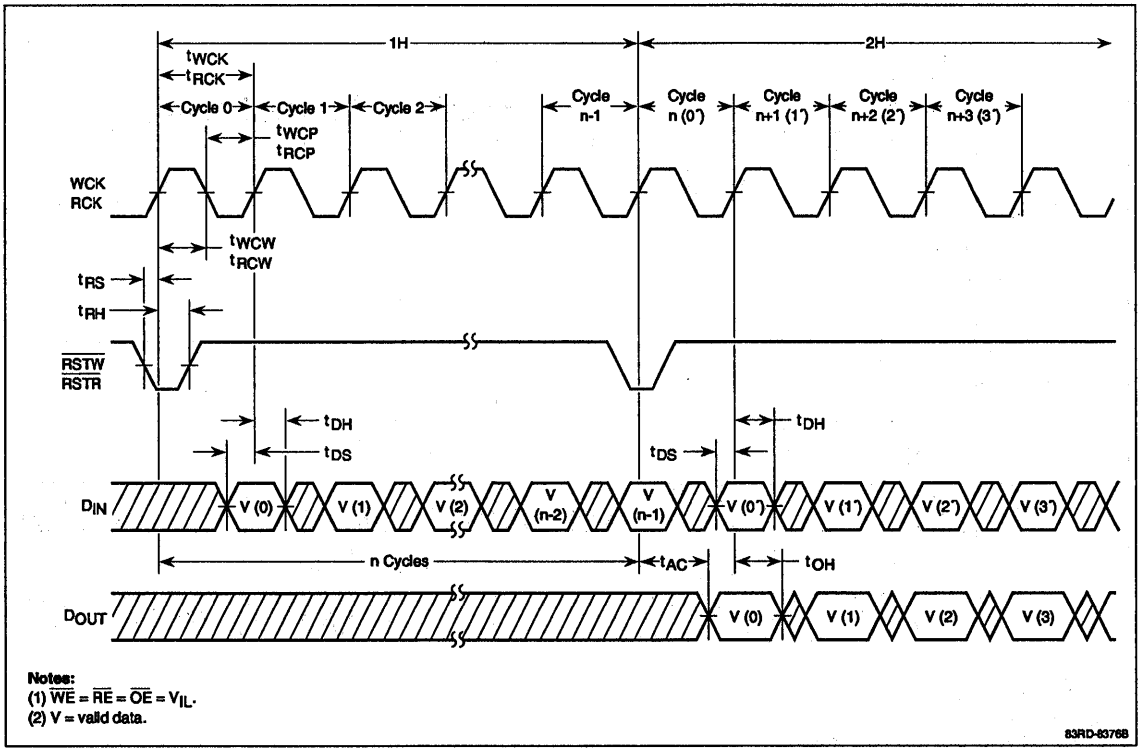
Notes:
(1) $\overline{WE} = \overline{RE} = \overline{OE} = V_{IL}$.
(2) V = valid data.
(3) H = 5048 bits (5048-word by 16-bit mode) or 10,096 bits (10,096-word by 8-bit mode)

83RD-8376B

18h

Timing Waveforms (cont)

n-Bit Delay Line Cycle 1

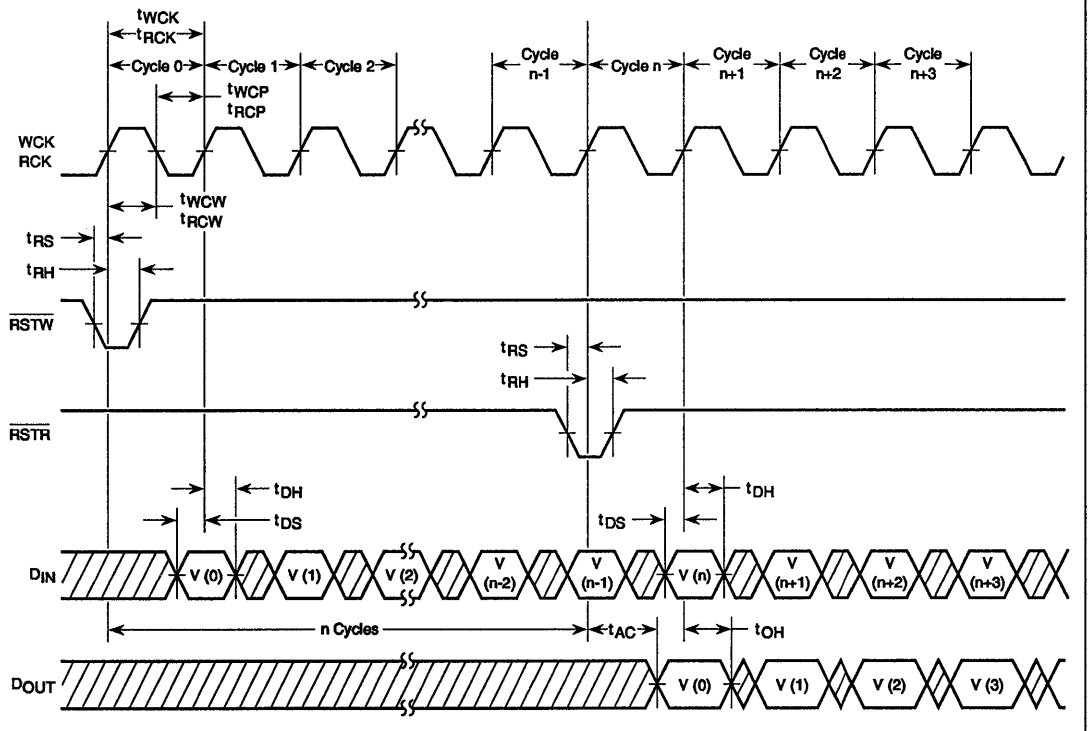


Notes:
(1) $\overline{WE} = \overline{RE} = \overline{OE} = V_{IL}$.
(2) V = valid data.

83RD-83768

Timing Waveforms (cont)

n-Bit Delay Line Cycle 2



Notes:
(1) $\overline{WE} = \overline{RE} = \overline{OE} = V_{IL}$.
(2) V = valid data.

83RD-6377B

18h

μPD42532
32,768 x 8-Bit
Bidirectional Data Buffer

Description

The μPD42532 bidirectional data buffer features 32,768-word by 8-bit organization and CMOS dynamic circuitry that provides for high-speed, asynchronous, simultaneous write and read operation at a minimum cycle time of 100 ns. Two sets of write and read registers between the I/O pins and the storage cells enable all data to be parallel-transmitted as a single register group when the registers are either full or empty. The device's main application is data transmission between devices having different processing speeds, such as between a central processor and a disk.

Automatic refreshing by means of an internal capability is performed regularly for the μPD42532—without any influence on write and read operation. A built-in arbitration circuit performs each required read, write, or refresh operation sequentially (even if transparent refreshing overlaps with the transmission of data) to simplify the device's external timing requirements.

The μPD42532 operates from a single +5-volt power supply and is packaged in a 600-mil, 40-pin plastic DIP. Four FLAG pins, plus $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ pins, are provided to monitor the amount of data accumulated in storage.

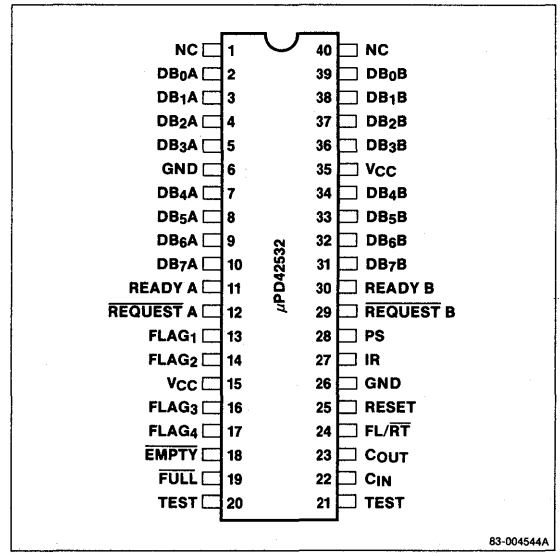
The μPD42532 is capable of bidirectional input/output by means of a port select function. Input and output pins are also supplied for cascade connection. Cascade connection allows any number of μPD42532s to be linked together so as to expand word width and length without limit.

Features

- ☐ 32,768-word by 8-bit organization
- ☐ CMOS technology
- ☐ Single +5-volt power supply
- ☐ Independent, asynchronous write/read operation
- ☐ Bidirectional transmission of input and output data (exchange of port functions)
- ☐ Automatic, regular refreshing
- ☐ Internal addressing
- ☐ Flag pin monitoring of accumulated data
- ☐ Unlimited expansion of word width and depth (cascade connection)
- ☐ Retransmit (re-read) function
- ☐ High-speed operation
  - — Access time: 50 ns maximum
  - — Cycle time: 100 ns minimum
- ☐ 600-mil, 40-pin plastic DIP packaging

Pin Configuration

40-Pin Plastic DIP



Ordering Information

Part Number	Access Time (max)	Cycle Time (min)	Package
μPD42532C-10	50 ns	100 ns	40-pin plastic DIP

Pin Identification

Symbol	Function
DB_0A-DB_7A	Port A input/output data buses
DB_0B-DB_7B	Port B input/output data buses
RESET	Reset input
$\overline{\text{REQUEST}}$ A/$\overline{\text{REQUEST}}$ B	Port A/Port B request input
READY A/READY B	Port A/Port B ready output
$\overline{\text{EMPTY}}$	Empty output
$FLAG_1$-$FLAG_4$	Flag outputs
$\overline{\text{FULL}}$	Full output
PS	Write/read port select input
IR	Interrupt read request input
FL/$\overline{\text{RT}}$	First load/retransmit input
C_{IN}	Cascade connection input
C_{OUT}	Cascade connection output
TEST	Test pin (connect to GND in system)
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Functions

DB_0A-DB_7A/DB_0B-DB_7B. These pins function as 8-bit data buses for write input or read output depending on the status of the PS pin. The output drivers are three-state outputs.

RESET. This pin initializes the internal counters and pointers.

$\overline{\text{REQUEST}}$ A/$\overline{\text{REQUEST}}$ B. Depending on the status of PS, one pin corresponds to the read port and the other to the write port. To initiate a write or read cycle, the signal goes low for the respective port (if READY A or READY B is low, the corresponding $\overline{\text{REQUEST}}$ input is ignored internally). These pins can be connected to the WR and RD pins of a CPU.

READY A/READY B. Depending on the status of PS, one pin corresponds to the read port and the other to the write port. When a write or read cycle is possible, the READY signal is high for the respective port. These pins can be connected to the READY pins of a CPU or DMA controller.

$\overline{\text{EMPTY}}$. The signal from this pin is low whenever the amount of data accumulated is exactly 0 bytes, and high in all other cases.

$FLAG_1$-$FLAG_4$. These pins reflect the amount of data accumulated in the storage array. By combining the output signals, it is possible to monitor (in 2K byte steps) data quantities of up to 32K bytes.

$\overline{\text{FULL}}$. The signal from this pin is low when the storage cells are full of accumulated data, and high in all other cases.

PS. This pin is used to specify the direction of data transfer. When PS is high, Port A serves as the write port and Port B as the read port. When PS is low, the functions of the two ports are reversed.

IR. If the data accumulated in storage is less than 64 bytes (i.e., one register's capacity), the READY signal for the read port goes low to inhibit reading. However, forcing IR high makes it possible to read all stored data.

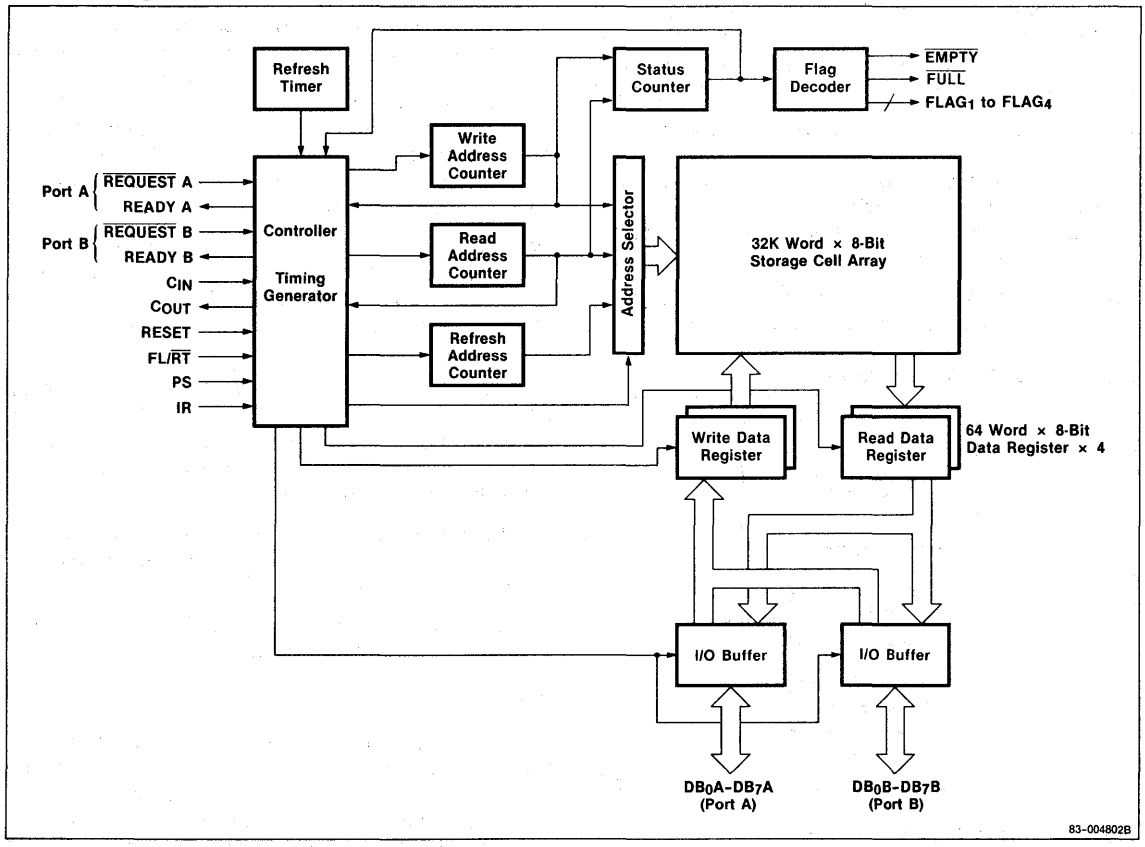
Read cycles are normally executed so as to maintain the stored data volume at levels above 2K bytes. If the data volume drops below 2K bytes for devices with process code K, all remaining data must be read using the interrupt read option.

FL/$\overline{\text{RT}}$. This pin designates the lead device when multiple devices are cascade connected. It is high only for that device and low for all others. If the device is not cascaded, a low FL/$\overline{\text{RT}}$ controls the retransmit (re-read) function; other than during retransmission, FL/$\overline{\text{RT}}$ must be high.

C_{IN}. This pin is used to expand word depth and is connected to the C_{OUT} pin of the device preceding it in cascade connections. If word depth is not expanded, C_{IN} is connected to C_{OUT} of the same device.

C_{OUT}. This pin is used to expand word depth and is connected to the C_{IN} pin of the device following it in cascade connections. If word depth is not expanded, C_{OUT} is connected to C_{IN} of the same device.

Block Diagram



18i

Operation

Reset Cycle

After power is applied to the μPD42532, it is necessary to clear the internal counters and initialize the write and read address pointers by executing a reset cycle. A reset cycle can be executed at any time by setting the RESET pin to a high logic level. However, once this cycle is initiated, RESET, $\overline{\text{REQUEST}}$, and FL/$\overline{\text{RT}}$ must be kept high for a minimum time of t_{SW} before the RESET signal goes low again (see waveform for "Reset Cycle"). The RESET, $\overline{\text{REQUEST}}$, and FL/$\overline{\text{RT}}$ signals are all high at the start of a reset, except in cascade connections, in which case a high FL/$\overline{\text{RT}}$ is required only in the first stage.

After a reset, the READY signal for the write port, READY (W), is driven high to prepare for a write cycle. Subsequently, the $\overline{\text{REQUEST}}$ signal for the write port, $\overline{\text{REQUEST}}$ (W), can be set low to commence writing.

A standard read cycle can be executed once data written to one of the 64-byte registers has filled that register and been transferred to the storage cells. The READY signal for the read port, READY (R), goes high to prepare for the cycle. Subsequently, the $\overline{\text{REQUEST}}$ signal for the read port, $\overline{\text{REQUEST}}$ (R), can be set low to commence reading.

Write Cycle

In a write cycle, data is written to one of two 64-byte write registers before being transferred to the storage cells. Whenever 64 bytes have been written into one register, write operation automatically shifts to the other and the contents of the first are transferred to storage. High-speed write cycles are thus executed continuously by alternating registers repeatedly. Write data must satisfy the requirements for setup and hold times as measured against the rising edge of $\overline{\text{REQUEST}}$ (W) [see waveform for "Write Cycle"].

A write cycle can be initiated any time READY (W) is high by setting $\overline{\text{REQUEST}}$ (W) low. To allow a write cycle to be executed in one port even while the other port may be executing a read cycle, READY (W) is always high after a reset, except in the following cases:

- Whenever the storage cells are full of accumulated data
- While the device is executing a forced read cycle (see **Interrupt Read Cycle**)
- When a retransmit operation is being performed (see **Retransmit Cycle**)

While READY (W) is off, the $\overline{\text{REQUEST}}$ (W) signal is ignored internally and no write cycle is executed.

Figure 1. Write Register Operation

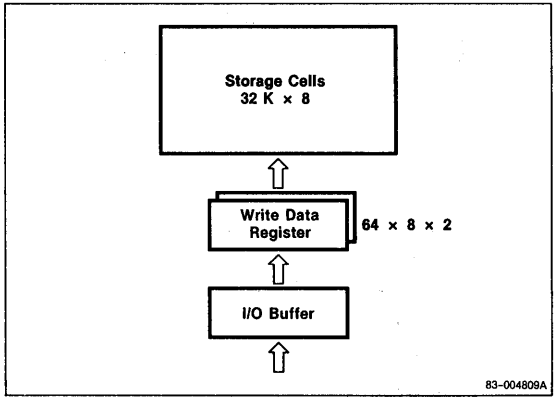
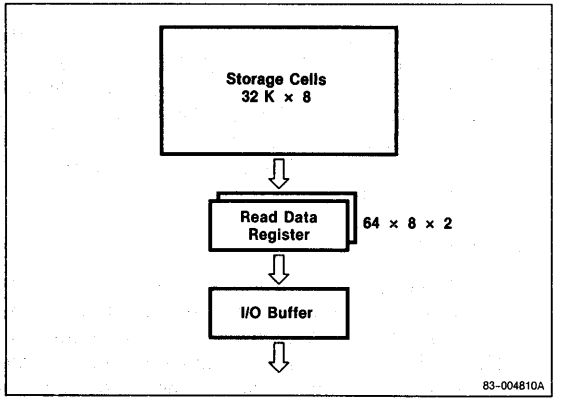


Figure 2. Read Register Operation



Read Cycle

In a read cycle, data is not read directly from the storage cells but rather from one of two 64-byte read registers. After 64 bytes of data have been read from one register, read operation automatically shifts to the other and the contents of the first are subsequently replaced by data from the storage cells. High-speed read cycles are thus executed continuously by alternating registers repeatedly.

Data is output after a maximum access time of t_{AC}, measured from the falling edge of $\overline{\text{REQUEST}}$ (R). When $\overline{\text{REQUEST}}$ (R) is high or READY (R) is low, the outputs are in a state of high impedance (see waveform for "Read Cycle").

A standard read cycle can be initiated any time READY (R) is high by setting $\overline{\text{REQUEST}}$ (R) low. To allow a read cycle to be executed in one port even while the other port may be executing a write cycle, the READY (R) signal is always high, except in the following cases:

- Whenever the data accumulated is less than 64 bytes
- While a retransmit operation is being performed (see **Retransmit Cycle**).

While READY (R) is low, $\overline{\text{REQUEST}}$ (R) is ignored internally and no read cycle is executed.

Flags

The μPD42532 supplies signals from the $\overline{\text{EMPTY}}$ pin, the $\overline{\text{FULL}}$ pin, and the four FLAG pins to indicate the amount of stored data in units of approximately 2K bytes. Accumulated data is reflected as the difference between the write address counter and the read address counter. Thus, if a total of 16K bytes have been read while 32K bytes have been written since the most recent reset, the amount of data in storage is 16K bytes.

The $\overline{\text{FULL}}$ and $\overline{\text{EMPTY}}$ pins are used to prevent overwriting and overreading. To control write operation on data units of register length (64 bytes), the $\overline{\text{FULL}}$ pin outputs a low signal when stored data reaches the 32,705- to 32,768-byte range. Whenever write cycles are executed continuously and the storage cells become full, $\overline{\text{REQUEST}}$ (W) is ignored and the signals of $\overline{\text{FULL}}$ and READY (W) are driven low to inhibit writing. Meanwhile if read cycles are executed and the data decreases to 32,704 bytes or less, READY (W) goes high again to enable write operation.

The $\overline{\text{EMPTY}}$ pin goes low whenever stored data is exactly 0 bytes. Since standard read cycles cannot be executed if the quantity of data drops below 64 bytes, READY (R) goes low to inhibit read operation. Whenever write cycles are executed and stored data increases to 64 bytes or more, READY (R) goes high again to enable read operation.

The status of the FLAG pins depends on the internal status of the write and read address counters. These counters are incremented as data is transferred to or from the storage array. Since the logic levels of the FLAG pins reflect movement of blocks of data on a 64-byte-register basis rather than on a single-byte basis, the status indicated by these pins can be in error by a maximum of 255 bytes with respect to the actual amount of data accumulated [i.e., the sum of the write register (63 bytes), the read registers (128 bytes), and the 64 bytes currently being transferred]. This discrepancy means that two adjacent ranges of stored data, as indicated by the FLAGs, can overlap by up to 191 bytes.

The following table shows the combination of signals output from these pins.

Table 1. Stored Data as Indicated by Flag Pins

Amount of Stored Data (bytes)	$\overline{\text{FULL}}$	$\overline{\text{EMPTY}}$	FLAG 1	FLAG 2	FLAG 3	FLAG 4
32705 to 32768	0	1	1	1	1	1
30721 to 32767	1	1	1	1	1	1
28673 to 30911	1	1	0	1	1	1
26625 to 28863	1	1	1	0	1	1
24577 to 26815	1	1	0	0	1	1
22529 to 24767	1	1	1	1	0	1
20481 to 22719	1	1	0	1	0	1
18433 to 20671	1	1	1	0	0	1
16385 to 18623	1	1	0	0	0	1
14337 to 16575	1	1	1	1	1	0
12289 to 14527	1	1	0	1	1	0
10241 to 12479	1	1	1	0	1	0
8193 to 10431	1	1	0	0	1	0
6145 to 8383	1	1	1	1	0	0
4097 to 6335	1	1	0	1	0	0
2049 to 4287	1	1	1	0	0	0
1 to 2239	1	1	0	0	0	0
0	1	0	0	0	0	0

Notes:

(1) 1 = high level

(2) 0 = low level

Interrupt Read Cycle

Whenever the amount of stored data drops below 64 bytes (i.e., one register's capacity), or 2K bytes for devices with process code K, READY (R) is driven low to inhibit reading. Any data remaining in a write register can only be read by means of an interrupt (or forced) read cycle.

An interrupt read cycle can be executed by forcing the IR pin high. At this point, data is transferred from the write register to one of the read registers via the storage array, and write operation is disabled until all stored data has been read. If this cycle is initiated after READY (R) goes low, read operation will be delayed until all data has been transferred to one of the read registers.

Once the device completes reading of its last address, the $\overline{\text{EMPTY}}$ and READY (R) signals are driven low and READY (W) goes high to enable write operation again (unless a retransmit cycle has been requested). Read cycles will be executed only after 64 bytes or more have been written and transferred to storage.

Retransmit Cycle

The μPD42532 will execute a retransmit cycle whenever a low-level pulse is applied to $\overline{\text{RT}}$. A retransmit cycle initializes the read address counter to starting address 0. Although retransmission can be executed at any time, $\overline{\text{REQUEST}}$ (W) and $\overline{\text{REQUEST}}$ (R) must be high before and after the low $\overline{\text{RT}}$ signal is applied.

During this cycle, the READY signals are pulsed low to temporarily inhibit writing and reading, and the FLAG and $\overline{\text{EMPTY}}$ signals vary in accordance with the amount of data in storage. After READY (W) goes high again, the retransmit preparation cycle is complete. Write operation can resume after an extra delay to ensure stability of the FLAG and $\overline{\text{EMPTY}}$ pins. If an interrupt read signal is applied during retransmission, the interrupt read cycle is executed after termination of the retransmit cycle.

The retransmit function is only useful in systems where less than 32K bytes of data are written between resets. If a retransmit cycle is executed after more than 32K bytes are written, old data cannot be retransmitted.

Since the $\overline{\text{RT}}$ pin is multiplexed as the first load (FL) pin in cascade connections, cascaded devices cannot be used for retransmission. In single-device configuration, this pin is always high except during a retransmit cycle.

Port Select Function

The μPD42532 is able to change the direction of data transfer according to the logical level of the signal applied to the PS pin. When a high-level input is applied to PS, Port A becomes the write port and Port B the read port. When PS is low, the functions of the two ports are reversed. While port functions are being assigned, the $\overline{\text{REQUEST}}$ signals must be kept high.

Since register and storage cell data are preserved during port selection, data written to a particular port can also be read from that same port.

Cascade Connection

The μPD42532 can be used in a single-device, 32K by 8-bit configuration or it can be cascade connected by means of the C_{IN} and C_{OUT} pins to allow unlimited expansion of word width and length.

Single-Device Configuration. When using the μPD42532 as a single 32K by 8-bit data buffer, connect C_{OUT} to C_{IN} and set the FL pin to a high logic level (see figure 3).

Expanded Word Width. When using multiple devices to expand word width, connect RESET, $\overline{\text{REQUEST}}$, PS, and IR to the corresponding pins of each μPD42532 in parallel and apply common control signals. Each C_{OUT} pin should be connected to its own C_{IN} pin (as in the single-device configuration) and a high-level input applied to each FL. The flag pins of a single μPD42532 can be used to represent the entire system (see figure 4).

Expanded Word Length. When using multiple devices to expand word length, set a high-level input to FL of the lead μPD42532 and a low-level input to FL of all the others. Each C_{OUT} pin should be connected to C_{IN} of the device following it; C_{OUT} on the last device should be connected to C_{IN} of the lead device. Connect RESET, $\overline{\text{REQUEST}}$, PS, and IR to the corresponding pins of each μPD42532 in parallel and apply common control signals.

The $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and READY pins of each device, respectively, can be ORed together by external logic. 'OR' outputs are composite $\overline{\text{EMPTY}}$, $\overline{\text{FULL}}$, and READY signals for all data buffers (see figure 5).

Operation. To enable operation of μPD42532s in cascade connection, set the RESET signal(s) high to clear the internal counters and initialize the write and read address pointers. When the reset is complete, start writing to the lead device. While data is being written to the first, all other devices output low READY signals and ignore the $\overline{\text{REQUEST}}$ signals. When write operation in the first μPD42532 (n) reaches the last address, its C_{OUT} pin outputs a high-level signal and forces C_{IN} of the next device high. Write operation shifts to the next device in succession (n + 1). The READY (W) signal of the first device (n) is driven low, and the READY (W) signal of the succeeding device (n + 1) goes high.

If only write cycles are being executed, each data buffer outputs a low $\overline{\text{FULL}}$ signal as writing is completed for that device. At the point where the last device finishes writing to its last address, all μPD42532s output low-level $\overline{\text{FULL}}$ and READY (W) signals. The ORed composite of these signals should be used to inhibit write operation.

If write and read cycles are being executed simultaneously, and the storage cells in the lead device are not full of accumulated data when the last device completes writing to its last address, write operation shifts to the lead μPD42532 again. Writing continues in this manner until every data buffer is full.

Read cycles also begin with the lead device (n) and shift to the next (n + 1) once the last address has been read. When all devices have been completely emptied of data, the ORed composite of the $\overline{\text{EMPTY}}$ signals is low. If the expanded word length configuration has less than 64 bytes of data in a write register, $\overline{\text{EMPTY}}$ will not be at a low level; READY (R) will be low to indicate that standard read operation may not proceed. Forced read or dummy write cycles will be required to continue reading any accumulated data of less than 64 bytes.

Figure 3. Single-Device Configuration Block Diagram

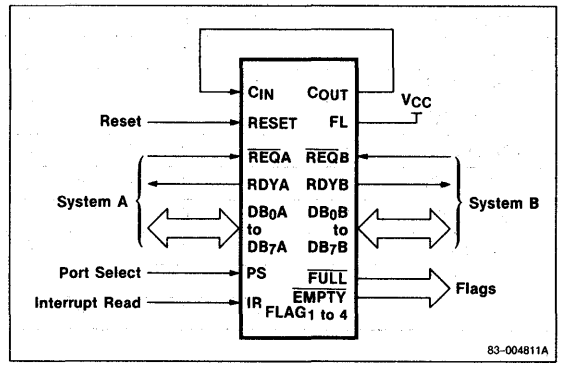


Figure 4. Expanded Word Width Block Diagram

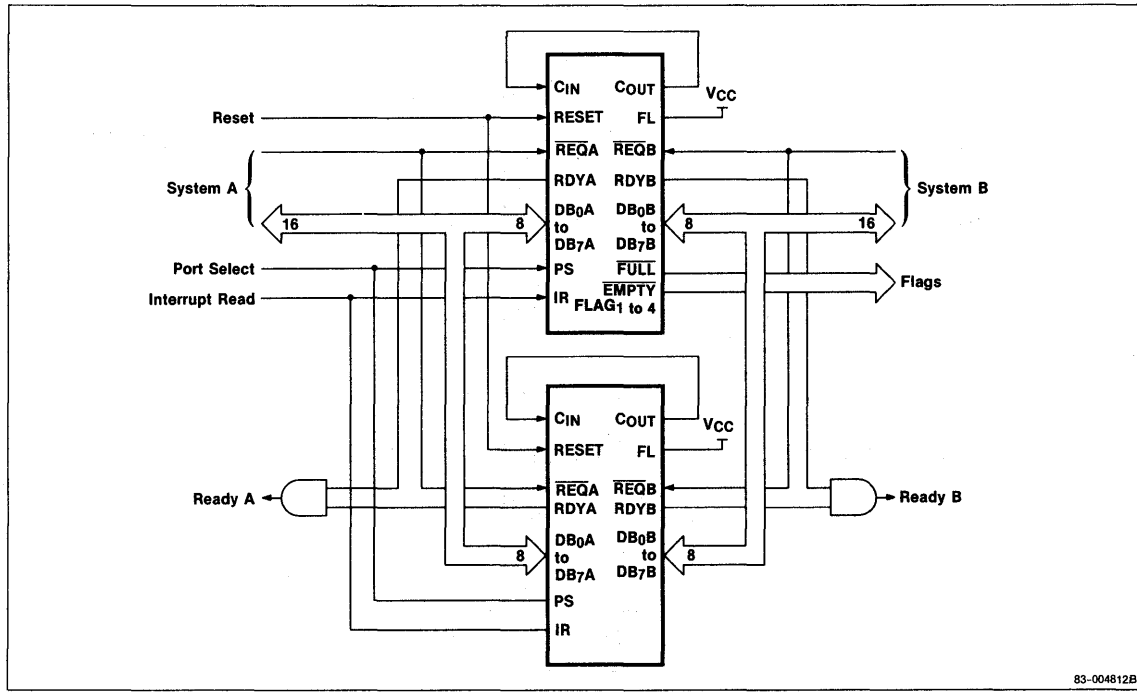
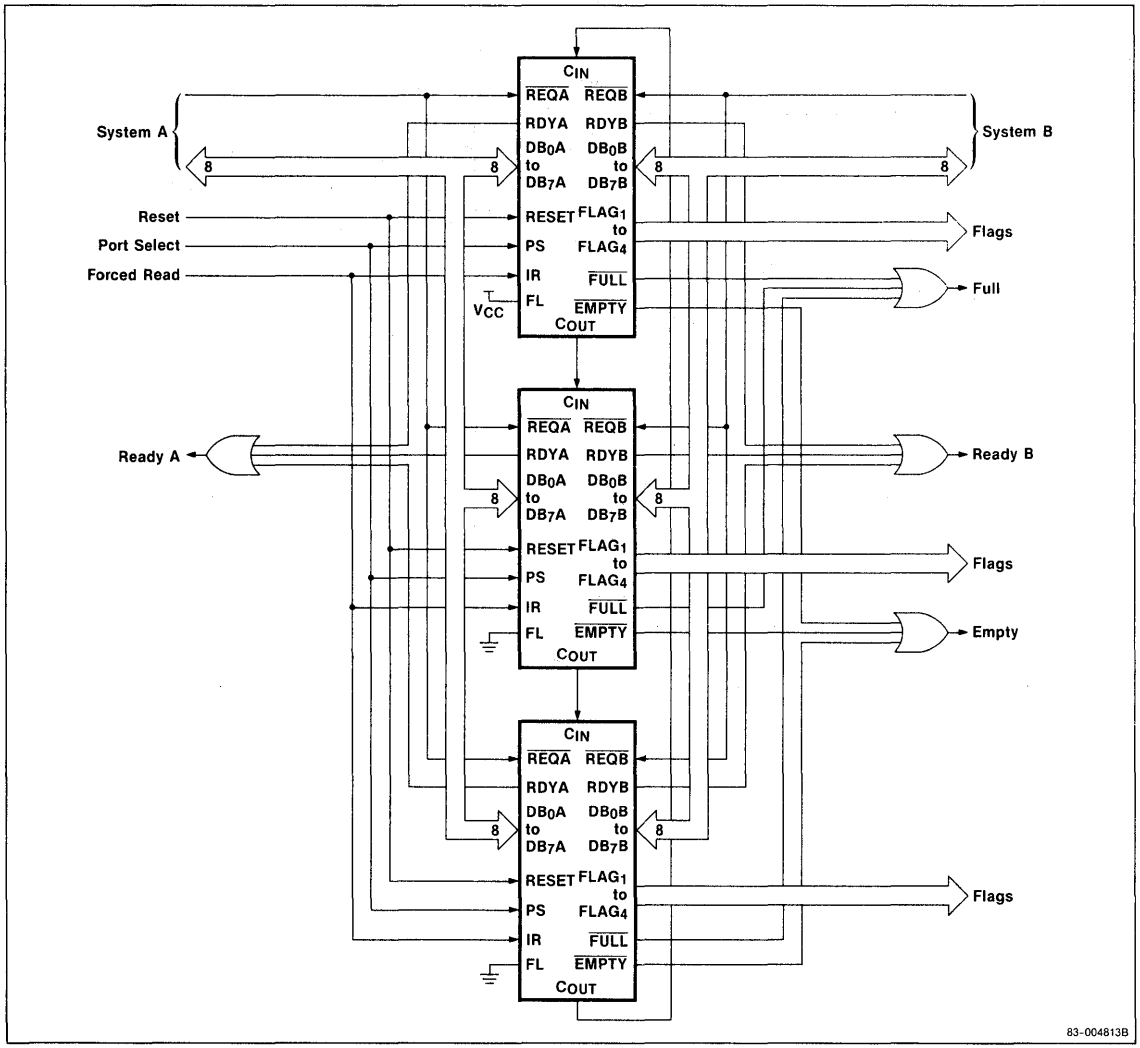


Figure 5. Expanded Word Length Block Diagram



Absolute Maximum Ratings

Terminal voltage, V_T	−1.5 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Output current, I_O	50 mA
Power supply voltage, V_{CC}	−1.5 to +7.0 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended DC Operating Conditions

$T_A = 0$ to +70°C; $V_{CC} = +5.0$ V ±10%

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC}	V
Input voltage, low	V_{IL}	−1.0		0.8	V

DC Characteristics

$T_A = 0$ to +70°C; $V_{CC} = +5.0$ V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby supply current	I_{CC1}			20	mA	$\overline{\text{REQUEST}}$ A, B = V_{IH}
Write/read cycle supply current	I_{CC2}			80	mA	$t_{WC} = 100$ ns; $t_{RC} = 100$ ns
Write cycle supply current	I_{CC3}			60	mA	$t_{WC} = 100$ ns; $\overline{\text{REQUEST}}$ (R) = V_{IH}
Read cycle supply current	I_{CC4}			60	mA	$t_{RC} = 100$ ns; $\overline{\text{REQUEST}}$ (W) = V_{IH}
Input leakage current	I_I	−10		10	μA	$V_I = 0$ to V_{CC}; other inputs = 0 V
Output leakage current	I_O	−10		10	μA	$V_O = 0$ to V_{CC}; output disabled
Output voltage, high	V_{OH}	2.4			V	$I_{OH} = -1$ mA
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 4$ mA

Capacitance

$T_A = 0$ to +70°C; $V_{CC} = +5.0$ V ±10%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Pins Under Test
Input capacitance	C_I			10	pF	$\overline{\text{REQUEST}}$, RESET, PS, C_{IN}, IR, FL/$\overline{\text{RT}}$
Output capacitance	C_O			10	pF	READY, $FLAG_1$-$FLAG_4$, C_{OUT}, $\overline{\text{FULL}}$, $\overline{\text{EMPTY}}$
Input/output capacitance	$C_{I/O}$			10	pF	DB_0-DB_7

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Read cycle time	t_{RC}	100		ns	
$\overline{\text{REQUEST}}$ (R) pulse width	t_{RQW}	50	10000	ns	(Note 5)
$\overline{\text{REQUEST}}$ (R) precharge time	t_{RQP}	30		ns	
$\overline{\text{REQUEST}}$ (R) low hold time after READY (R) high	t_{RQN}	50	10000	ns	(Note 6)
READY (R) low output time	t_{RRF}		30	ns	(Note 14)
Access time	t_{AC}		50	ns	
Access time after READY (R) high	t_{ACR}		50	ns	
Output data hold time	t_{OH}	10		ns	
Output data off time	t_{OFF}		40	ns	
Low-impedance output delay	t_{LZ}	5		ns	
Low-impedance output delay after READY (R) high	t_{LZR}	0		ns	
READY (R) low time when empty	t_{SRR}		4800 + 64 t_{WC}	ns	(Note 8)
READY (R) low time when almost empty	t_{EMR}	0	4800 + 63 t_{WC}	ns	(Note 8)
Write cycle time	t_{WC}	100		ns	
$\overline{\text{REQUEST}}$ (W) pulse width	t_{WQW}	50	10000	ns	(Note 5)
$\overline{\text{REQUEST}}$ (W) precharge time	t_{WQP}	30		ns	
$\overline{\text{REQUEST}}$ (W) low hold time after READY (W) high	t_{WQN}	50	10000	ns	(Note 6)
READY (W) low output time	t_{WRF}		30	ns	
Write data setup time	t_{DW}	30		ns	
Write data hold time	t_{DH}	10		ns	
$\overline{\text{REQUEST}}$ high setup time	t_{QRP}	t_T + 30		ns	(Note 6)
READY (W) low time when full	t_{FLW}	0	3200 + 64 t_{RC}	ns	
$FLAG_1$-$FLAG_4$ output times	t_{FLO}		4800	ns	
$\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ output valid times	t_{EFO}		40	ns	
$\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ output hold times	t_{EFH}	0		ns	
$\overline{\text{FULL}}$ output off time	t_{FOF}		3200	ns	(Note 9)
C_{OUT} output off time when read request is executed	t_{COR}		40	ns	
C_{OUT} output on time when write request is executed	t_{COW}		40	ns	
C_{IN} setup time for $\overline{\text{REQUEST}}$ (R)	t_{CIR}	10		ns	
C_{IN} setup time for $\overline{\text{REQUEST}}$ (W)	t_{CIW}	10		ns	
Reset pulse width	t_{SW}	100		ns	
READY, $\overline{\text{FULL}}$, and $\overline{\text{EMPTY}}$ output times after reset	t_{SWR}		80	ns	
$FLAG_1$-$FLAG_4$ output times after reset	t_{SSF}		100	ns	
$\overline{\text{REQUEST}}$ precharge hold time after reset	t_{SWQ}	30		ns	
$\overline{\text{RT}}$ disable hold time after reset	t_{SRT}	800		ns	

AC Characteristics (cont)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
C_{OUT} output low time after reset	t_{SWC}		100	ns	
READY (R) on time after interrupt read is executed	t_{FRR}	0	6400	ns	(Note 7)
READY (W) off time after interrupt read is executed	t_{FWR}		50	ns	(Note 7)
READY (W) on time after interrupt read	t_{IRW}		100	ns	(Note 11)
$\overline{\text{REQUEST}}$ (W) hold time after IR input	t_{FQA}	60		ns	(Note 13)
$\overline{\text{REQUEST}}$ (W) setup time before IR input	t_{FQB}	60		ns	
IR pulse width	t_{FW}	50	2000	ns	(Notes 4, 12, 13)
$\overline{\text{REQUEST}}$ hold time after PS input	t_{PAQ}	100		ns	
$\overline{\text{REQUEST}}$ setup time before PS input	t_{PBQ}	100		ns	
READY output time after port selection	t_{PSR}		50	ns	
$\overline{\text{RT}}$ pulse width	t_{RTW}	50	2000	ns	(Note 4)
$\overline{\text{REQUEST}}$ setup time before $\overline{\text{RT}}$ input	t_{BRT}	60		ns	(Note 10)
$\overline{\text{REQUEST}}$ hold time after $\overline{\text{RT}}$ input	t_{RTQ}	60		ns	
READY (R) on time after retransmit is executed	t_{RTR}		6400	ns	(Note 7)
READY (W) on time after retransmit is executed	t_{WRT}		4800	ns	(Note 7)
READY off time after retransmit is executed	t_{RRT}		50	ns	
$\overline{\text{EMPTY}}$ and $\overline{\text{FULL}}$ output hold times after retransmit is executed	t_{FSRT}	0		ns	
$\overline{\text{EMPTY}}$ reset time after retransmit is executed	t_{RTE}		3200	ns	
$FLAG_1$-$FLAG_4$ output valid times after retransmit is executed	t_{RTF}		8000	ns	
Input transition time	t_T	5	50	ns	

Notes:

(1) All voltages are referenced to GND.

(2) All ac measurements assume input pulse rise and fall times of 5 ns.

(3) The input voltage reference levels for timing ratings are V_{IH} (min) and V_{IL} (max). Transition time t_T is defined between V_{IH} and V_{IL}.

(4) IR and $\overline{\text{RT}}$ inputs cannot be applied simultaneously. A timing delay of at least 100 ns is required. See figures 6 and 7 for acceptable input methods.

(5) The maximum pulse width of 10,000 ns applies only when the READY signal is on.

(6) $\overline{\text{REQUEST}}$ cannot be raised to a high level during the t_{QRP} + t_{RQN} (or t_{WQN}) interval.

(7) If an $\overline{\text{RT}}$ (IR) pulse is applied during IR ($\overline{\text{RT}}$) operation, the $\overline{\text{RT}}$ (IR) operation is delayed until IR ($\overline{\text{RT}}$) operation is released.

(8) "Empty" is defined as the state where the amount of stored data is zero, and "almost empty" is defined as the state where the amount of data is 1 to 63 bytes.

(9) t_{FOF} is defined from the rising edge of the $\overline{\text{REQUEST}}$ (R) signal when the amount of stored data reaches the prescribed value (that is, the value at which the FULL signal changes from a low level to a high level as defined in Table 1).

(10) t_{BRT} = 4800 ns minimum for the devices with process code K.

Figure 6. Input Timing for IR and $\overline{\text{RT}}$: Method 1

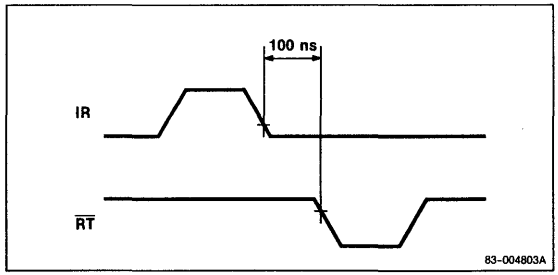
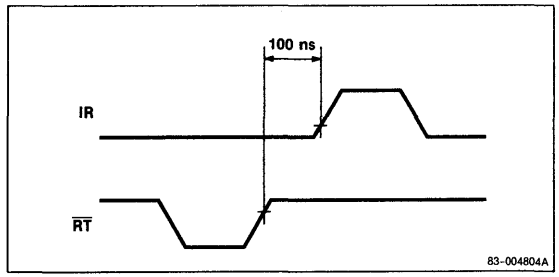


Figure 7. Input timing for IR and $\overline{\text{RT}}$: Method 2



AC Characteristics (cont)

Notes [cont]:

(11) After all data has been read in an IR cycle for devices with process code K, always input a $\overline{\text{RESET}}$ signal to initialize the internal circuitry before proceeding to the next operation. See figure 8.

(12) The IR signal is invalid whenever the $\overline{\text{EMPTY}}$ signal is low on devices with process code K.

(13) If an IR input signal is applied in a cascade connection for devices with process code K, the $\overline{\text{REQUEST}}$ (W) signal must stay at a high level until all data has been read.

(14) Read cycles are normally executed so as to maintain the stored data volume at levels above 2K bytes. If the data volume drops below 2K bytes for devices with process code K, read all of the remaining data using the interrupt read option.

Figure 8. Reset Pulse After IR Operation

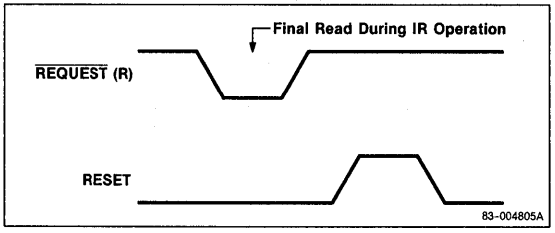


Figure 9. Input Timing

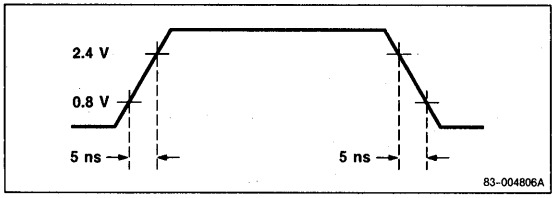


Figure 10. Output Timing

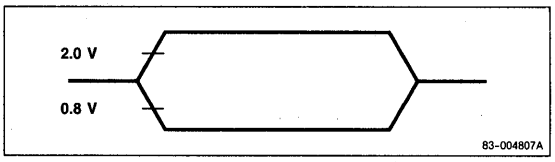
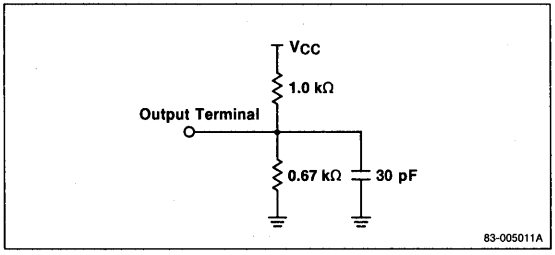
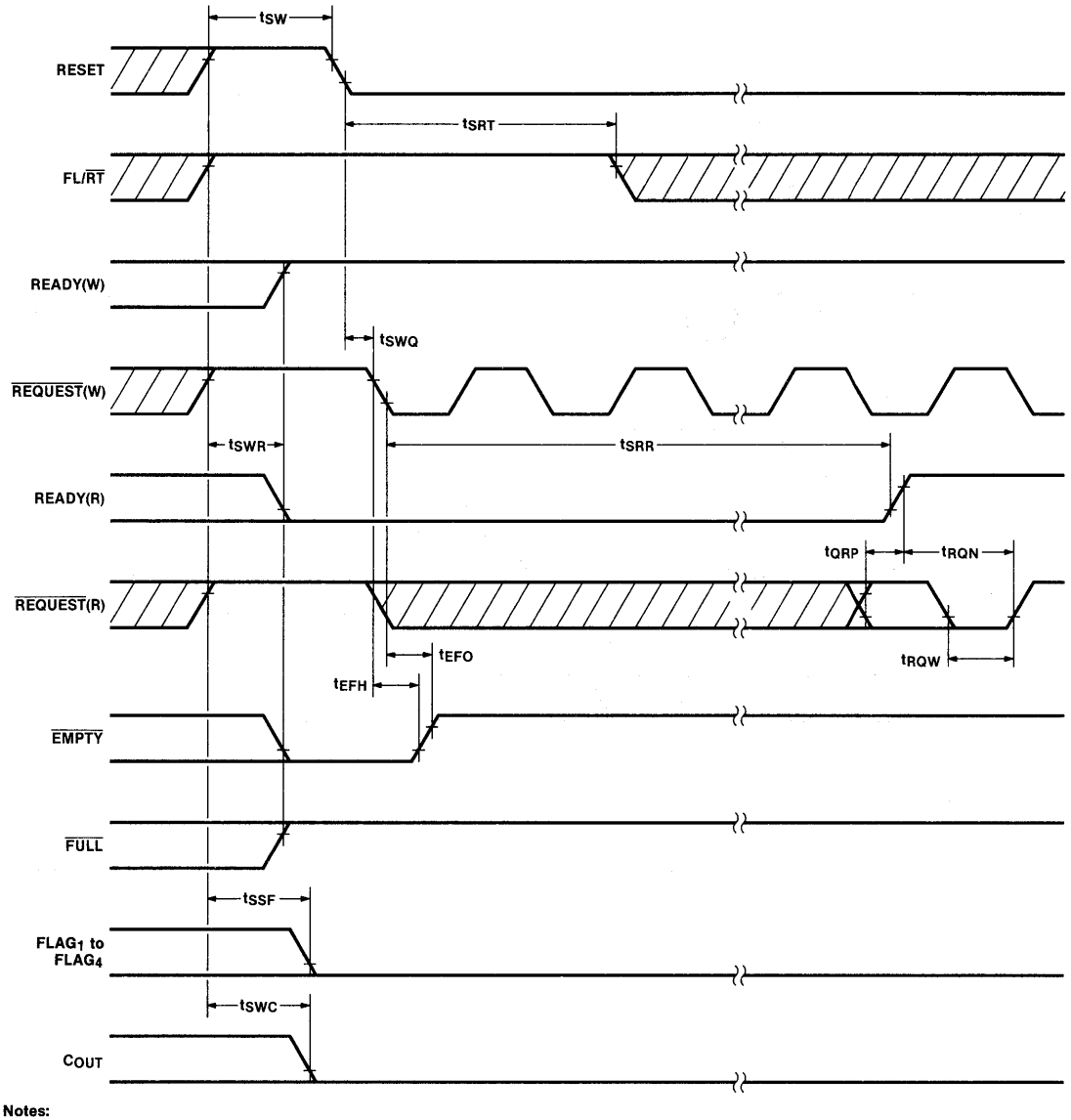


Figure 11. Output Loads



Timing Waveforms

Reset Cycle

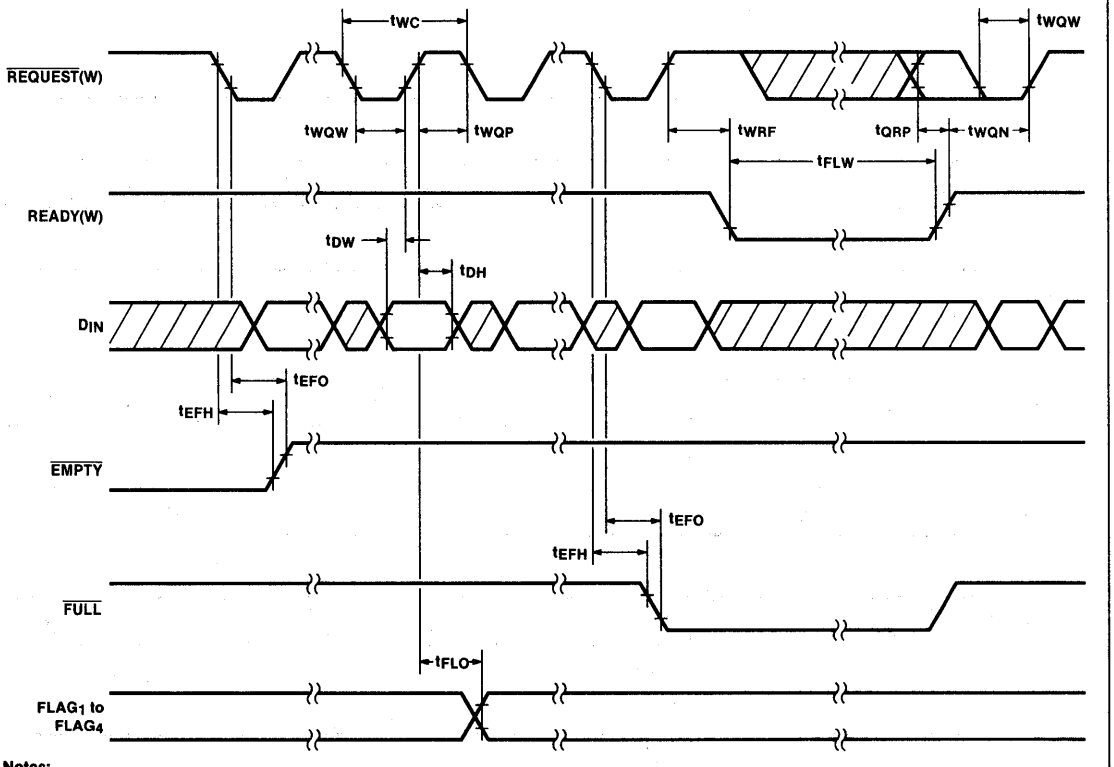


Notes:
(1) IR = low
(2) PS = high or low

83-004814B

Timing Waveforms (cont)

Write Cycle

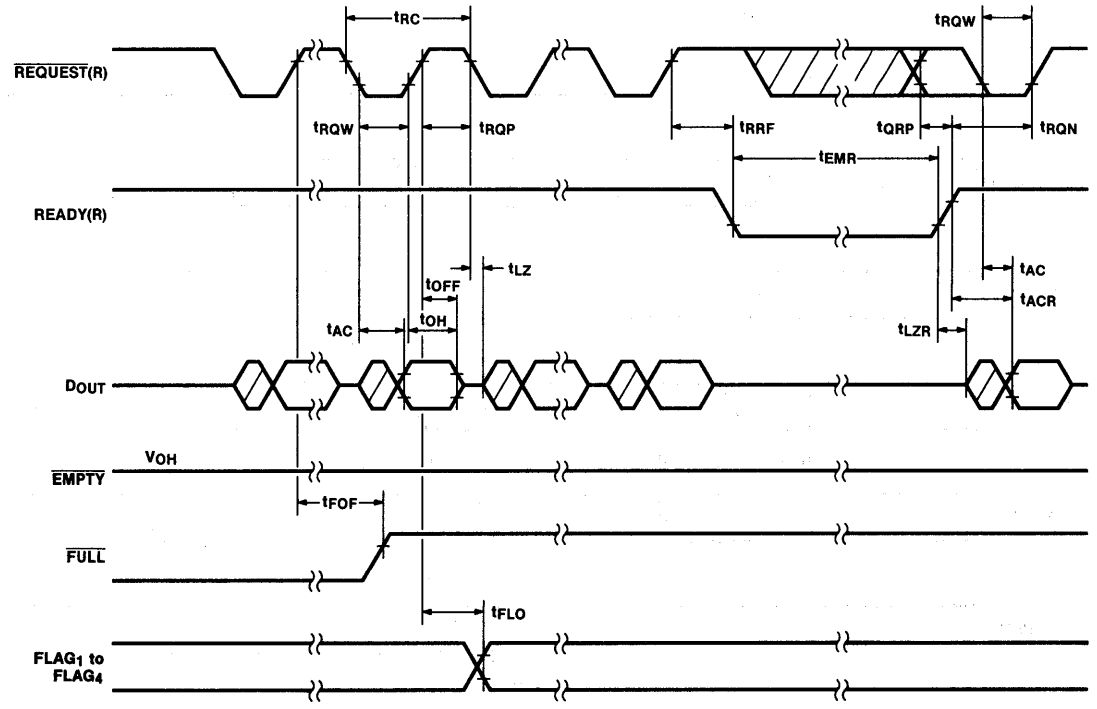


Notes:
(1) IR = low
(2) FL/$\overline{RT}$ = high
(3) PS = high or low
(4) RESET = low

83-004815B

Timing Waveforms (cont)

Read Cycle

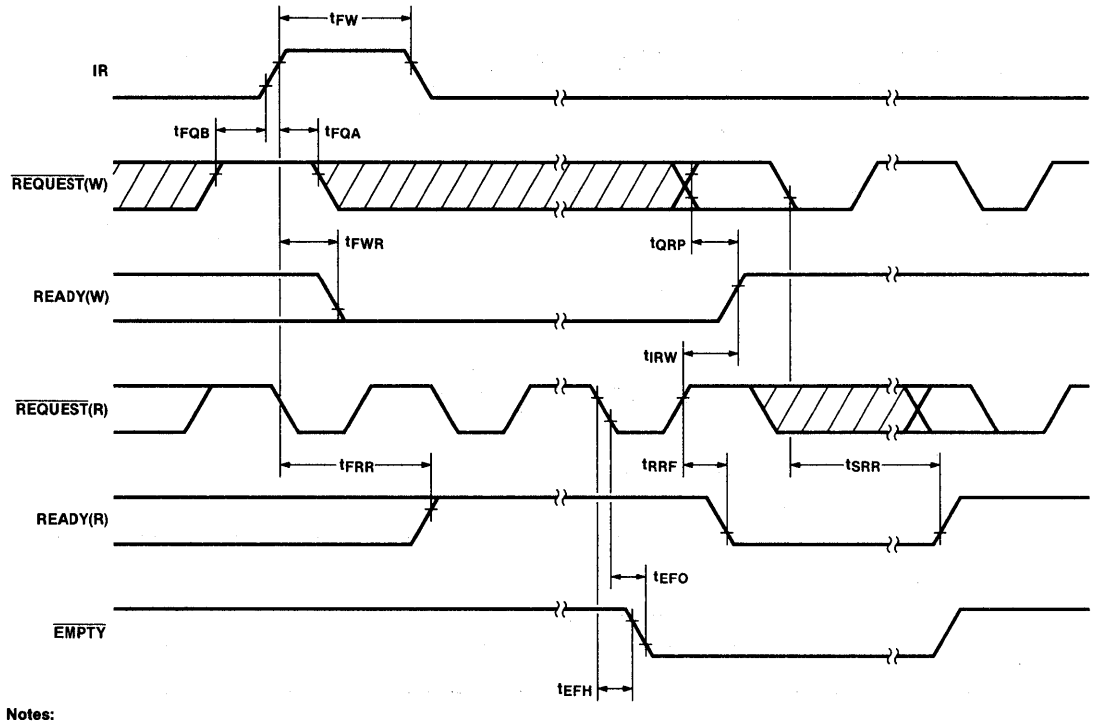


Notes:
(1) IR = low
(2) FL/$\overline{RT}$ = high
(3) PS = high or low
(4) RESET = low

83-004816B

Timing Waveforms (cont)

Interrupt Read Cycle

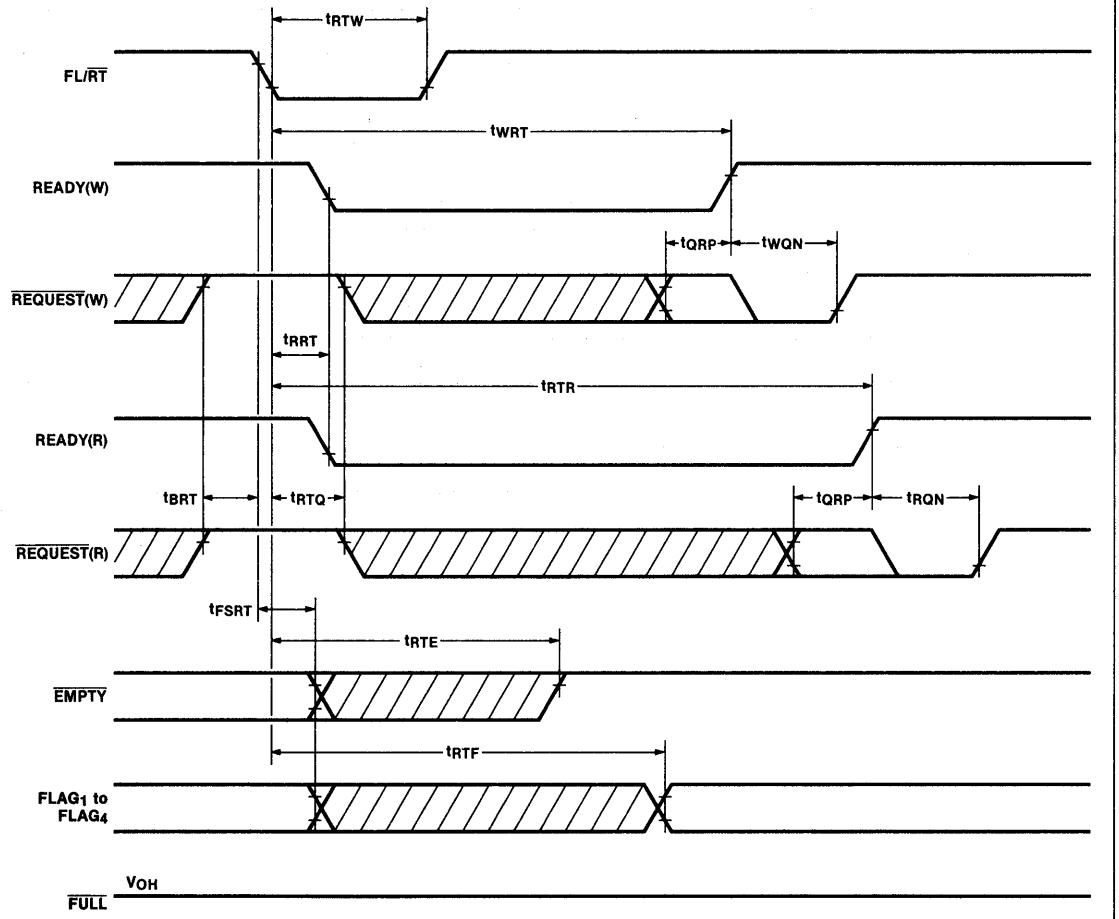


Notes:
(1) PS = high or low
(2) FL/$\overline{RT}$ = high
(3) RESET = low

83-004818B

Timing Waveforms (cont)

Retransmit Cycle

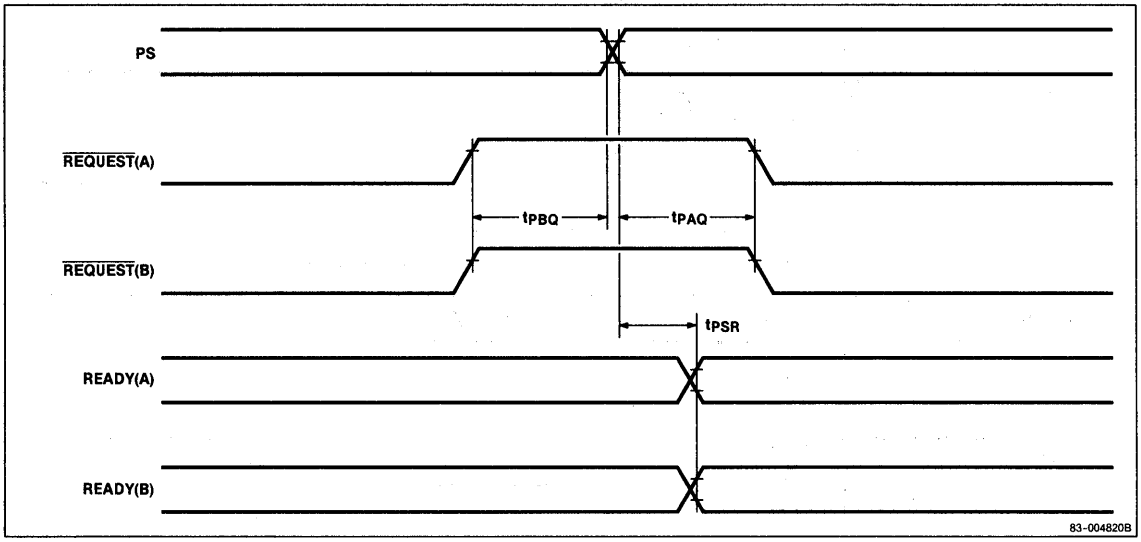


Notes:
(1) PS = high or low
(2) IR = low
(3) RESET = low

83-004819B

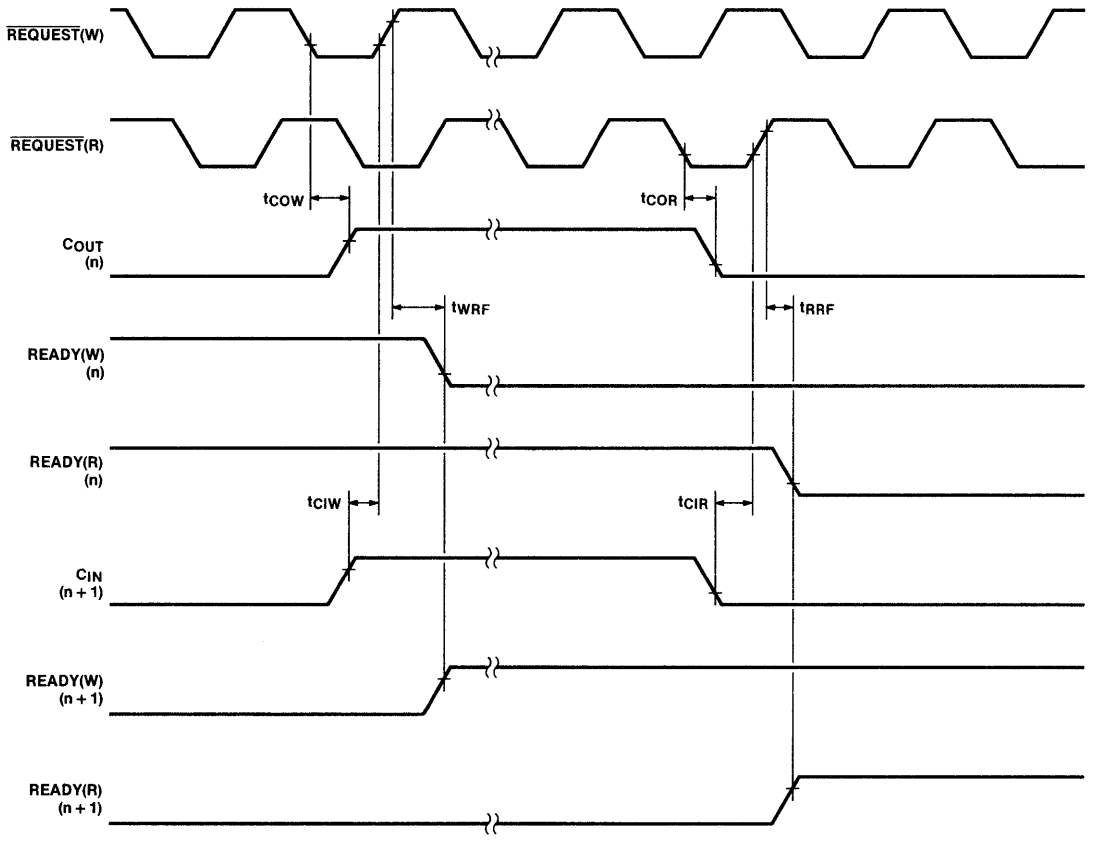
Timing Waveforms (cont)

Port Select Cycle



Timing Waveforms (cont)

Cascade Cycle



Notes:

(1) IR = low

(2) FL/$\overline{RT}$ = high or low

(3) PS = high or low

(4) RESET = low

83-004817B

Description

The μPD42601 silicon file is an economical mass storage device specifically designed to replace magnetic disk drives in silicon disk, solid-state recording, and system backup applications in a variety of computer systems. Organized as 1,048,576 words by 1 bit, the μPD42601 provides a battery backup feature for enhanced system performance and a substantial savings in power consumption.

The device is capable of executing standard access or page-mode write and read cycles. Refreshing is accomplished by means of $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, $\overline{RAS}$-only refresh cycles, self-refresh cycles, or by normal read or write cycles on the 512 address combinations of A_0 through A_8 during a 32-ms period.

The μPD42601 is uniquely suitable for battery backup systems because it requires a very low power supply current for extended periods of self-refresh operation. If ambient temperature is limited to 50 °C (max), as little as 30 μA (max) is required to maintain all data.

The μPD42601 is available in high-density 20-pin plastic ZIP or 26/20-pin plastic SOJ packaging.

Features

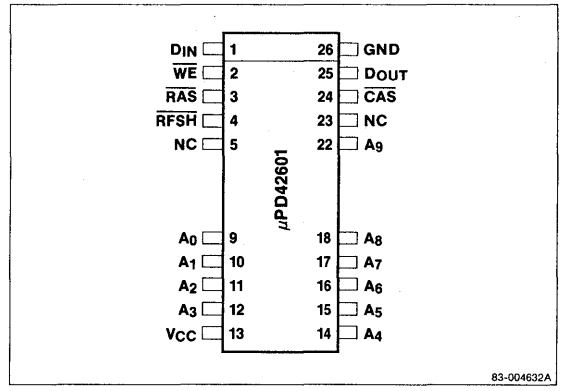
- ☐ 1,048,576-word by 1-bit organization
- ☐ Single +5-volt ±10% power supply
- ☐ CMOS technology
- ☐ Low operating power: 12 mA maximum
- ☐ 30 μA maximum self-refresh current at 0 to 50 °C
- ☐ Read or write cycle time: 1000 ns minimum
- ☐ Page-mode cycle time: 200 ns minimum
- ☐ $\overline{CAS}$ before $\overline{RAS}$ refreshing
- ☐ 512 refresh cycles during 32-ms period
- ☐ Automatic self-refreshing by $\overline{RAS}$ input cycling

Ordering Information

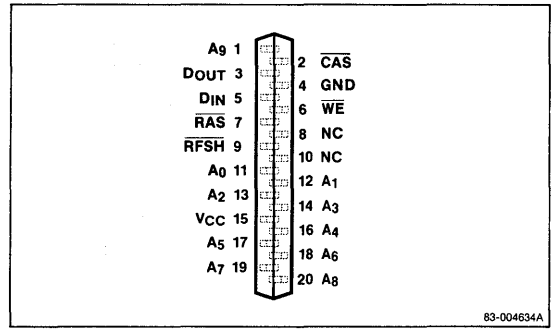
Part Number	Page-Mode Cycle (min)	Self-Refresh Current (max, 50 °C)	Package
μPD42601LA-60	200 ns	120 μA	26/20-pin plastic SOJ
LA-60L	200 ns	30 μA	
μPD42601V-60	200 ns	120 μA	20-pin plastic ZIP
V-60L	200 ns	30 μA	

Pin Configurations

26/20-Pin Plastic SOJ



20-Pin Plastic ZIP



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Pin Identification

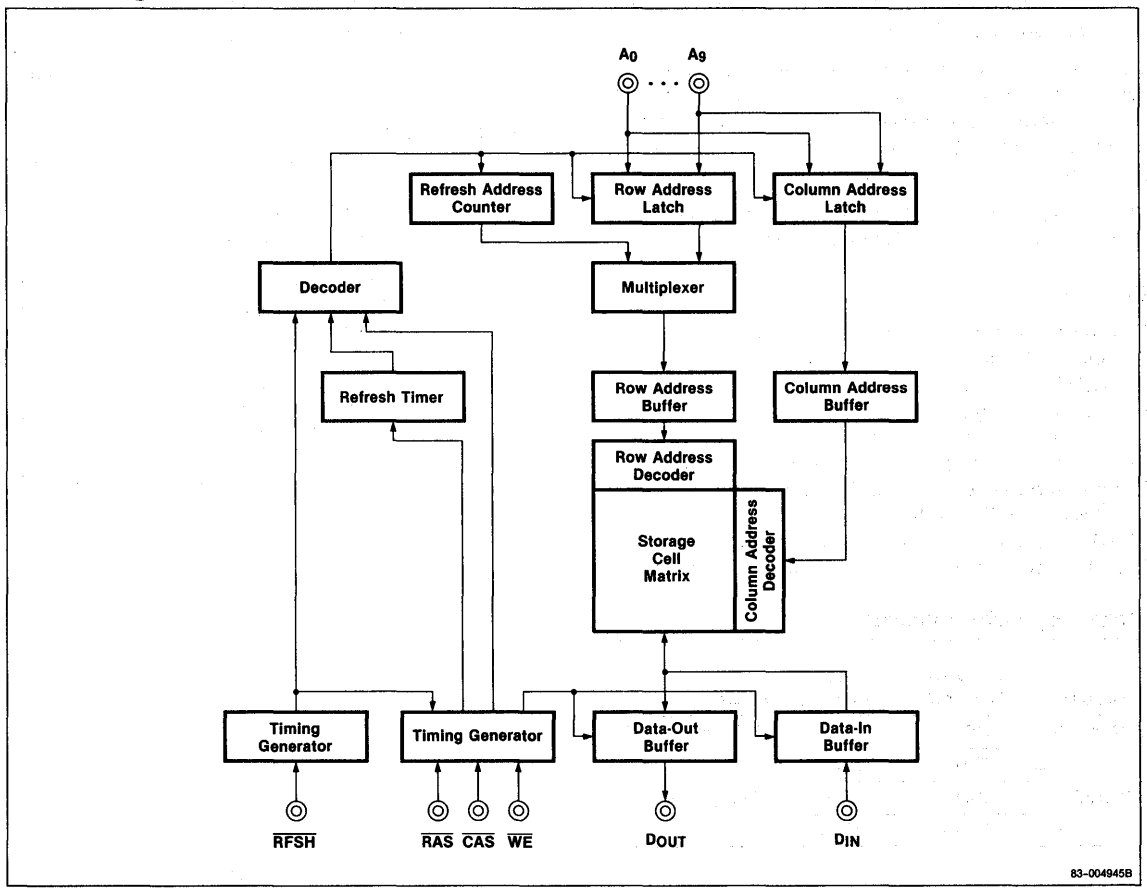
Name	Function
A_0 - A_9	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{RFSH}$	Self-refresh control
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W
Supply voltage, V_{CC}	−1.0 to +7.0 V

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



Operation

Write and Read Operation

The μPD42601 is capable of standard write and read operation as well as page-mode operation. The ten row address bits are set up on pins A_0 through A_9 and latched onto the chip by $\overline{RAS}$. Subsequently, ten column address bits are set up on pins A_0 through A_9 and latched onto the chip by $\overline{CAS}$. An appropriate write or read cycle is executed according to the logical level of $\overline{WE}$: a high $\overline{WE}$ initiates a read cycle and low $\overline{WE}$ initiates a write cycle.

Page-mode operation may be executed by pulsing $\overline{CAS}$ repeatedly while maintaining a low $\overline{RAS}$. The first word is accessed in the same manner as in standard write and read operation, with row addresses latched onto the chip by $\overline{RAS}$ and column addresses latched by $\overline{CAS}$. Subsequent column addresses are accessed for each $\overline{CAS}$ cycle, repeated during a period up to the maximum $\overline{RAS}$ pulse width.

Refresh Operation

$\overline{CAS}$ before $\overline{RAS}$ Refreshing. This cycle may be initiated by bringing $\overline{CAS}$ low before $\overline{RAS}$ and holding it low after $\overline{RAS}$ falls. A built-in address counter makes external addressing unnecessary.

$\overline{RAS}$-Only Refreshing. $\overline{RAS}$-only refreshing is executed by holding $\overline{CAS}$ high as the row addresses are latched onto the chip by $\overline{RAS}$. Using this cycle, all storage cells are refreshed by the 512 address combinations of A_0 through A_8 during a 32-ms period.

Self-Refreshing. A self-refresh cycle is initiated for the addresses generated by the internal counter whenever $\overline{RFSH}$ is active low and the $\overline{RAS}$ input is cycling (see figure 1). Since the minimum required $\overline{RAS}$ cycling frequency depends on ambient temperature, power consumption will also vary with temperature as shown in the AC and DC Characteristics. For extended periods of self-refresh operation, a low supply current is required; e.g., if ambient temperature is limited to 50°C (max), as little as 30 μA (max) is required to maintain all data.

18j

Recommended DC Operating Conditions

$T_A = 0$ to +70°C; GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		5.5	V
Input voltage, low	V_{IL}	−1.0		0.8	V

Capacitance

$T_A = 25$°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$
Output capacitance	C_D	7	pF	D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Operating current, average	I_{CC1}			12	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; I_O = 0 mA; $t_{RC} = t_{RC}$ (min)
Standby current	I_{CC2}			2.0	mA	$\overline{RAS} = \overline{CAS} = \overline{RFSH} = V_{IH}$
				0.5	mA	$\overline{RAS} = \overline{CAS} = \overline{RFSH} \geq V_{CC} - 0.4$; A_0-A_9, D_{IN} and $\overline{WE} \geq V_{CC} - 0.4$ or ≤ 0.4 V
Operating current, $\overline{RAS}$-only refresh, average	I_{CC3}			10	mA	$t_{RC} = t_{RC}$ (min); I_O = 0 mA
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh, average	I_{CC4}			10	mA	$t_{RC} = t_{RC}$ (min); I_O = 0 mA
Operating current, self-refresh mode, average	I_{CC5}			30	μA	$\overline{RAS}$ cycling at 50 kHz (Notes 1, 2, 3, 4)
				60	μA	$\overline{RAS}$ cycling at 100 kHz (Notes 1, 2, 3, 4)
				120	μA	$\overline{RAS}$ cycling at 200 kHz (Notes 1, 2, 3)
Operating current, page mode, average	I_{CC6}			12	mA	$t_{PC} = t_{PC}$ (min); I_O = 0 mA
Input leakage current	I_{IL}	−1		1	μA	V_{IN} = 0 to V_{CC}; all other pins not under test = 0 V
Output leakage current	I_{OL}	−1		1	μA	D_{OUT} disabled; V_{OUT} = 0 to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_O = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_O = −5 mA

Notes:

(1) When $t_{FAS} \leq 2.5$ ms, I_{CC5} does not depend on the $\overline{RAS}$ clock; I_{CC5} (max) = 500 μA. When $t_{FAS} \geq 2.5$ ms, I_{CC5} (max) = 500 μA in the first 2.5 ms after $\overline{RFSH}$ falls (it does not depend on the $\overline{RAS}$ clock). Subsequently, I_{CC5} is 120 μA for the μPD42601 or is as shown in the following table for the μPD42601-L.

Operating Temperature [T_A]	Clock Frequency [min]	Self-Refresh Current [max]
0 to 50°C	50 kHz	30 μA at 50 kHz
0 to 60°C	100 kHz	60 μA at 100 kHz
0 to 70°C	200 kHz	120 μA at 200 kHz

(2) t_{RCF} depends on operating temperature as reflected in the table below (see figures 2 and 3).

Operating Temperature [T_A]	t_{RCF} [max] μPD42601-L	μPD42601
0 to 50°C	20 μs	5 μs
0 to 60°C	10 μs	5 μs
0 to 70°C	5 μs	5 μs

(3) Average power supply current required for self refreshing is measured according to the following conditions: $\overline{RAS}$ is cycling at 50, 100 or 200 kHz; $V_{IH} \geq V_{CC} - 0.4$ V; $V_{IL} \leq 0.4$ V; $t_T \leq 50$ ns; A_0 to A_9, D_{IN}, $\overline{WE}$ and $\overline{CAS} = V_{CC}$ to GND; RFSH = V_{IL}. When $\overline{RFSH} = V_{IL}$ (≤ 0.4 V), the $\overline{RAS}$ input must be cycled at or exceeding the minimum frequency requirements.

(4) This specification applies to the μPD42601-L only. For the non-L version, I_{CC5} is 120 μA, maximum, at all T_A.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Random read or write cycle time	t_{RC}	1000		ns	(Note 5)
Page-mode cycle time	t_{PC}	200		ns	(Notes 5, 15)
Access time from $\overline{RAS}$	t_{RAC}		600	ns	(Notes 6, 7)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		100	ns	(Notes 6, 8)
Output buffer turnoff delay	t_{OFF}	0	100	ns	(Note 9)
Transition time (rise and fall)	t_T	3	50	ns	(Notes 3, 4)
$\overline{RAS}$ precharge time	t_{RP}	390		ns	
$\overline{RAS}$ pulse width	t_{RAS}	600	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	100	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	600		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	150	500	ns	(Note 10)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	30		ns	(Note 11)
$\overline{CAS}$ precharge time (non-page cycle)	t_{CPN}	90		ns	
$\overline{CAS}$ precharge time (page cycle)	t_{CP}	90		ns	(Note 15)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		ns	

AC Characteristics (cont)

$T_A = 0$ to +70°C; $V_{CC} = +5.0$ V ±10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Row address setup time	t_{ASR}	0		ns	
Row address hold time	t_{RAH}	90		ns	
Column address setup time	t_{ASC}	0		ns	
Column address hold time	t_{CAH}	90		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	590		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	75		ns	(Note 12)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	(Note 12)
Write command hold time	t_{WCH}	90		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	590		ns	
Write command pulse width	t_{WP}	90		ns	
Data-in setup time	t_{DS}	0		ns	(Note 14)
Data-in hold time	t_{DH}	90		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	590		ns	
Write command setup time	t_{WCS}	0		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	30		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	105		ns	
Refresh period	t_{REF}		32	ms	Addresses A_0-A_8
Self-Refresh Cycle					
$\overline{RFSH}$ pulse width	t_{FAS}	810		ns	(Note 13)
$\overline{RAS}$ to $\overline{RFSH}$ delay time	t_{RFD}	100		ns	
$\overline{RAS}$ setup time to $\overline{RFSH}$	t_{FRS}	200		ns	
$\overline{RAS}$ cycle time in self-refresh mode	t_{RCF}	1000		ns	(Note 16)
$\overline{RAS}$ precharge time in self-refresh mode	t_{RPF}	390		ns	
$\overline{RAS}$ pulse width in self-refresh mode	t_{RSF}	600		ns	
$\overline{RFSH}$ to $\overline{RAS}$ delay time	t_{FRD}	100		ns	
$\overline{RAS}$ hold time in self-refresh mode	t_{FRH}	200		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up (V_{CC} = +5.0 V ±10%), followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. $\overline{RAS}$, $\overline{CAS}$, and $\overline{RFSH}$ must equal V_{IH} during the initial pause.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(6) Load = 2 TTL loads and 100 pF (V_{OH} = 2.4 V, V_{OL} = 0.4 V).

(7) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown.

(8) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(9) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(10) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(11) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(12) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(13) When $t_{FAS} \leq 2.5$ ms, I_{CC5} does not depend on the $\overline{RAS}$ clock; I_{CC5} (max) = 500 μA. When $t_{FAS} \geq 2.5$ ms, I_{CC5} (max) = 500 μA for the first 2.5 ms after $\overline{RFSH}$ falls (it does not depend on the $\overline{RAS}$ clock). Subsequently, I_{CC5} is 120 μA for the μPD42601 or is as shown in the following table for the μPD42601-L.

Operating Temperature [T_A]	Clock Frequency [min]	Self-Refresh Current [max]
0 to 50°C	50 kHz	30 μA at 50 kHz
0 to 60°C	100 kHz	60 μA at 100 kHz
0 to 70°C	200 kHz	120 μA at 200 kHz

Notes [cont]:

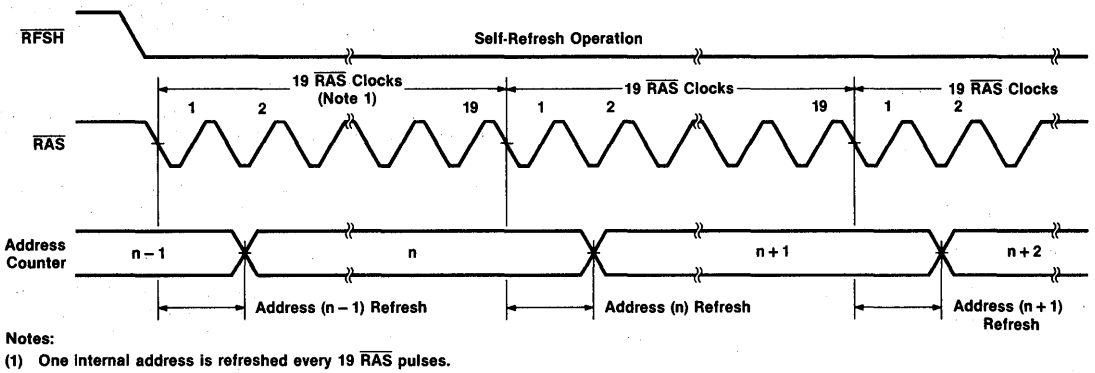
(14) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles.

(15) This parameter is applicable to page-mode operation.

(16) t_{RCF} depends on operating temperature as reflected in the table below (see figures 2 and 3).

Operating Temperature [T_A]	t_{RCF} [max]	
	μPD42601-L	μPD42601
0 to 50°C	20 μs	5 μs
0 to 60°C	10 μs	5 μs
0 to 70°C	5 μs	5 μs

Figure 1. Internal Address Generation in Self-Refresh Operation



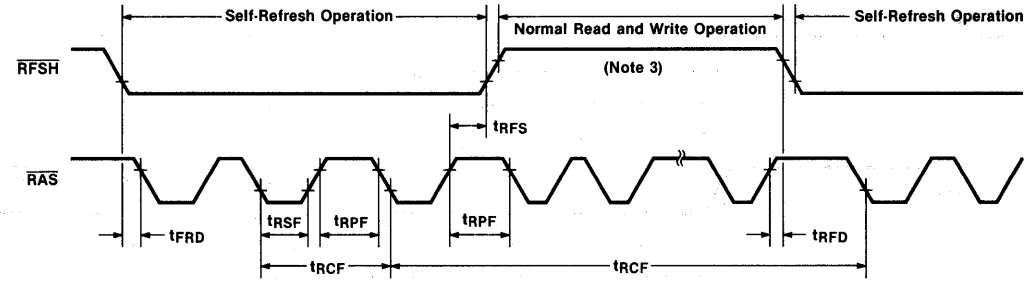
Notes:

(1) One internal address is refreshed every 19 $\overline{RAS}$ pulses.

(2) The self-refresh mode is intended primarily for long periods of refresh-only operation.

83-004503B

Figure 2. Special Requirement for t_{RCF} Near Periods of Limited Standard Refresh Cycles



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50°C	20 μs	5 μs
60°C	10 μs	5 μs
70°C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

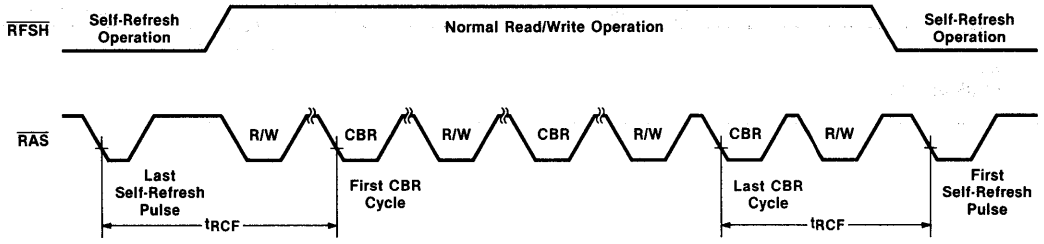
[3] In this period of normal read/write operation, there are no CBR refresh cycles or less than 512 RAS-only refresh cycles.

[4] The time delay between the last self-refresh pulse in one self-refresh cycle, and the first self-refresh pulse in the next cycle, is defined by t_{RCF} [max] when the intervening period of read and write operation meets the conditions in Note 3.

[5] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

83-004502B

Figure 3. Timing Restrictions for Entering and Exiting Self-Refresh Operation



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50°C	20 μs	5 μs
60°C	10 μs	5 μs
70°C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

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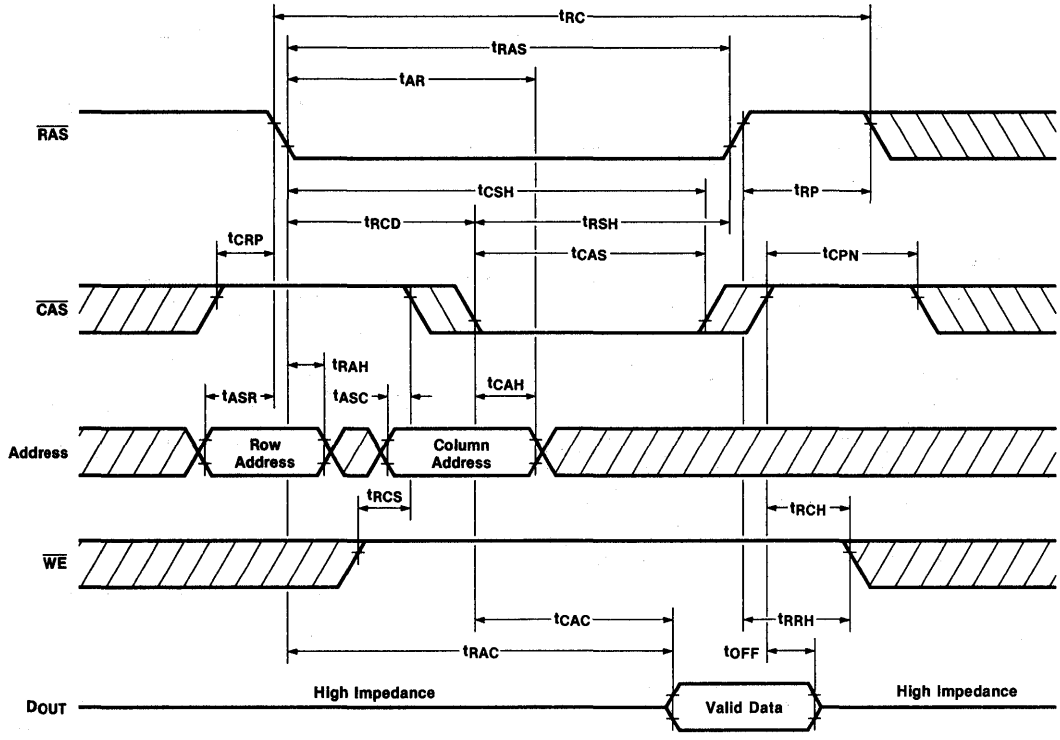
Timing Waveforms

Read Cycle

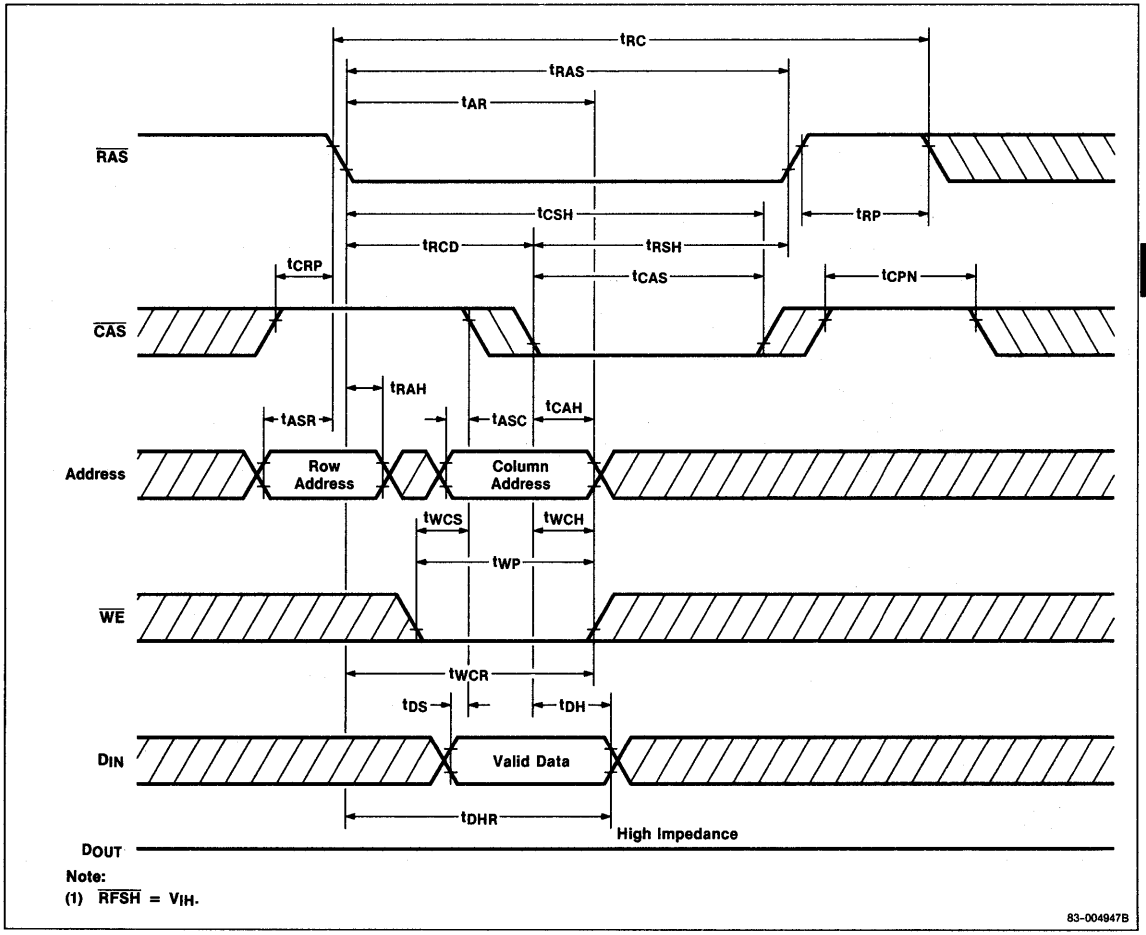


Note:
(1) $\overline{RFSH}$ = V_{IH}.

83-004946B

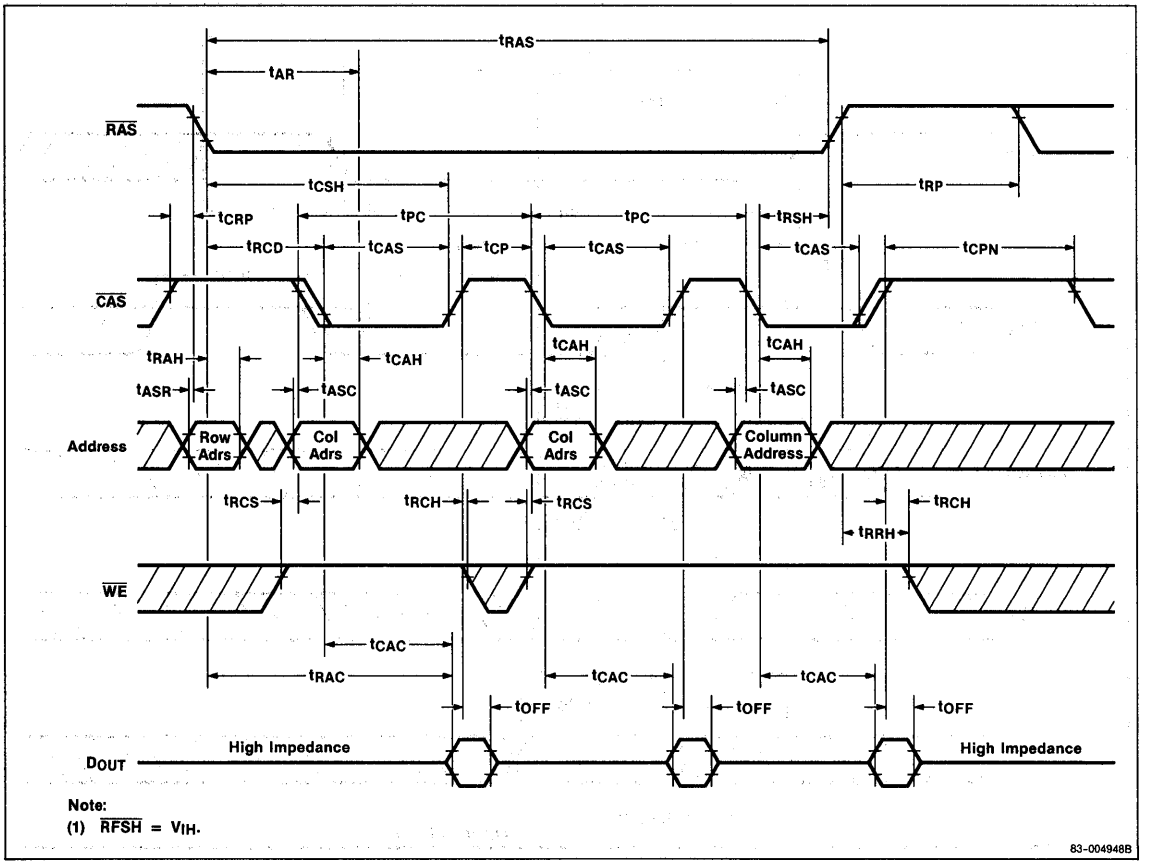
Timing Waveforms (cont)

Write Cycle (Early Write)



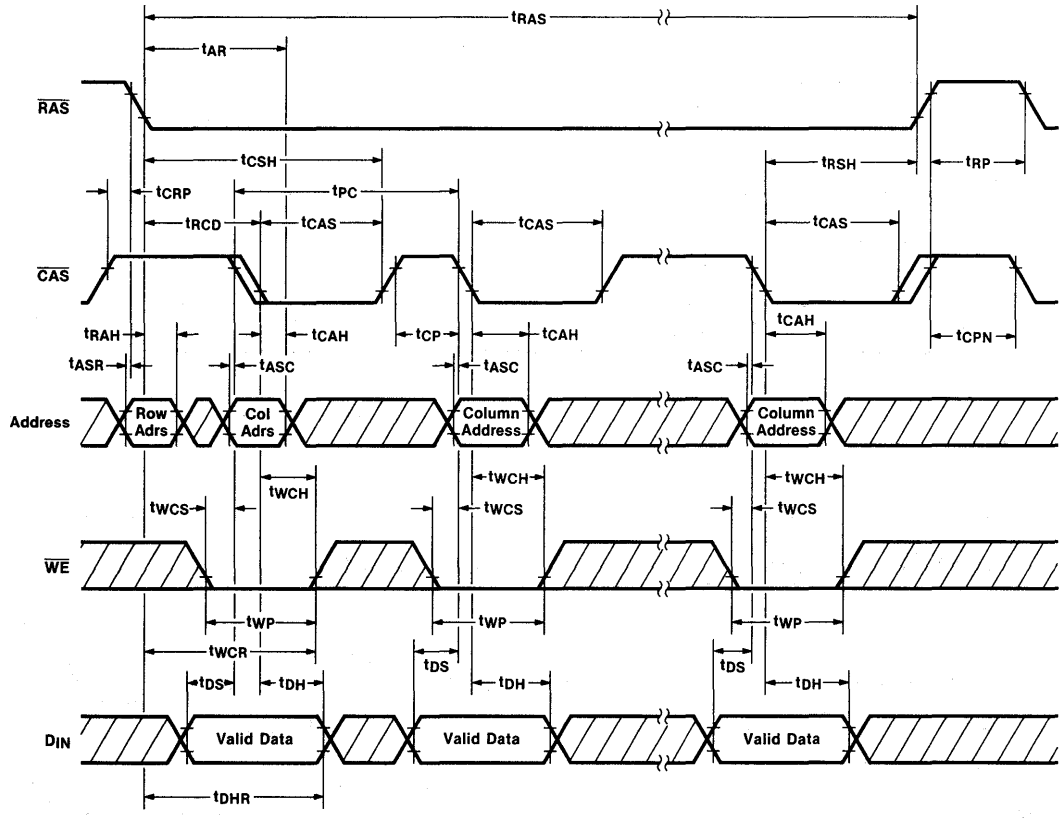
Timing Waveforms (cont)

Page-Mode Read Cycle



Timing Waveforms (cont)

Page-Mode Write Cycle (Early Write)



Note:
(1) $\overline{RFSH}$ = V_{IH}.

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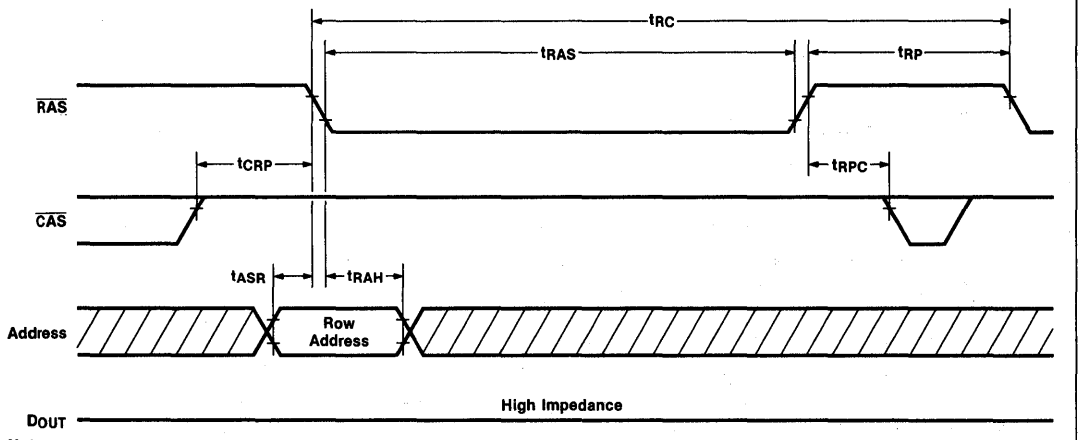
Timing Waveforms (cont)

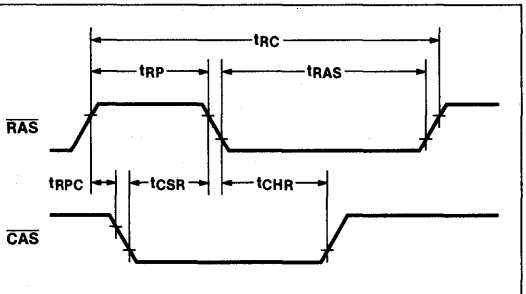
$\overline{RAS}$-Only Refresh Cycle



Notes:
(1) $\overline{RFSH}$ = V_{IH}.
(2) $\overline{WE}$ and D_{IN} = don't care.

83-004951B

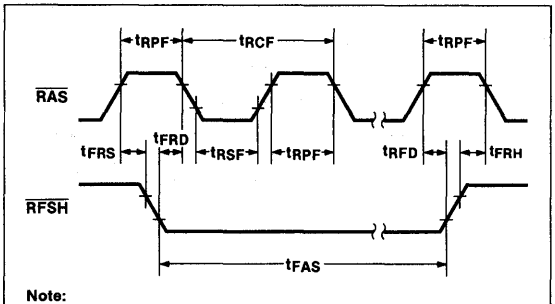
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Notes:
(1) $\overline{RFSH}$ = V_{IH}.
(2) $\overline{WE}$, D_{IN}, Addresses = don't care.

83-004950A

Self-Refresh Cycle



Note:
(1) $\overline{CAS}$, $\overline{WE}$, D_{IN}, Address = don't care.

83-004952A

Description

The μPD42641 is a fast-page, low-power dynamic RAM organized as 4,194,304 words by 1 bit and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and advanced CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing can also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1024 address combinations of A_0 - A_9 during a 16-ms refresh period.

In automatic self-refresh mode, the μPD42641 retains data for extended time periods with very-low power consumption (30 μA at 50°C). This feature is most useful in battery backup applications.

Features

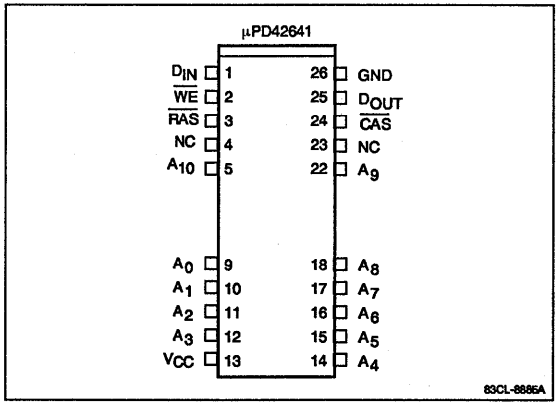
- 4,194,304-word by 1-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
  - —Active: 90 mA
  - —Standby: 1.0 mA (CMOS interface)
  - —Self-refresh: 30 μA (t_{RCE} = 3.2 μs, T_A = 50°C)
- $\overline{CAS}$ before $\overline{RAS}$ refresh cycles
- Multiplexed address inputs
- On-chip substrate bias generator
- Nonlatched, three-state outputs
- Low input capacitance
- TTL-compatible inputs and outputs
- Automatic self-refreshing by $\overline{RAS}$ input cycling
- 1024 refresh cycles every 16 ms
- 26/20-pin SOJ and TSOP plastic packages (300-mil)

Pin Identification

Name	Function
A_0 - A_{10}	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

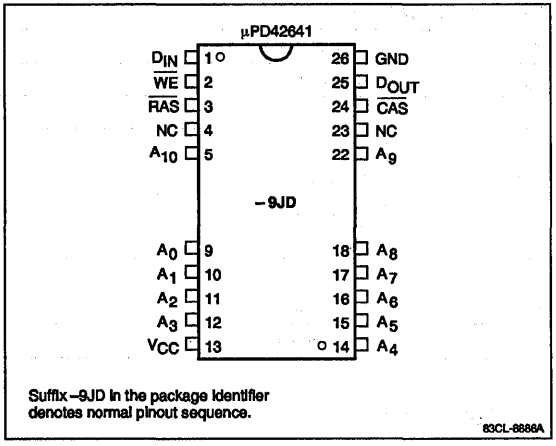
Pin Configurations

26/20-Pin Plastic SOJ



Pin Configurations (cont)

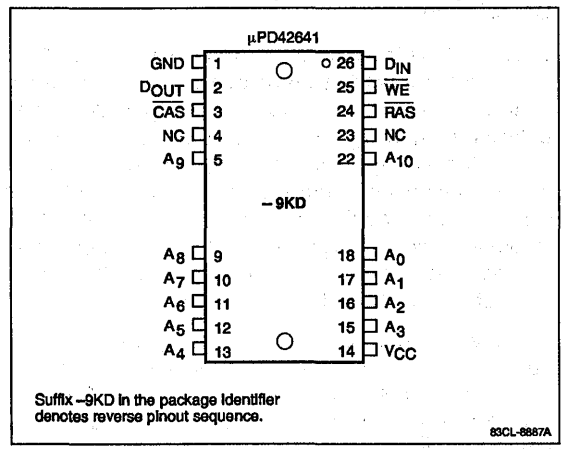
26/20-Pin Plastic TSOP (Normal Pinouts)



Suffix –9JD in the package identifier denotes normal pinout sequence.

83CL-8686A

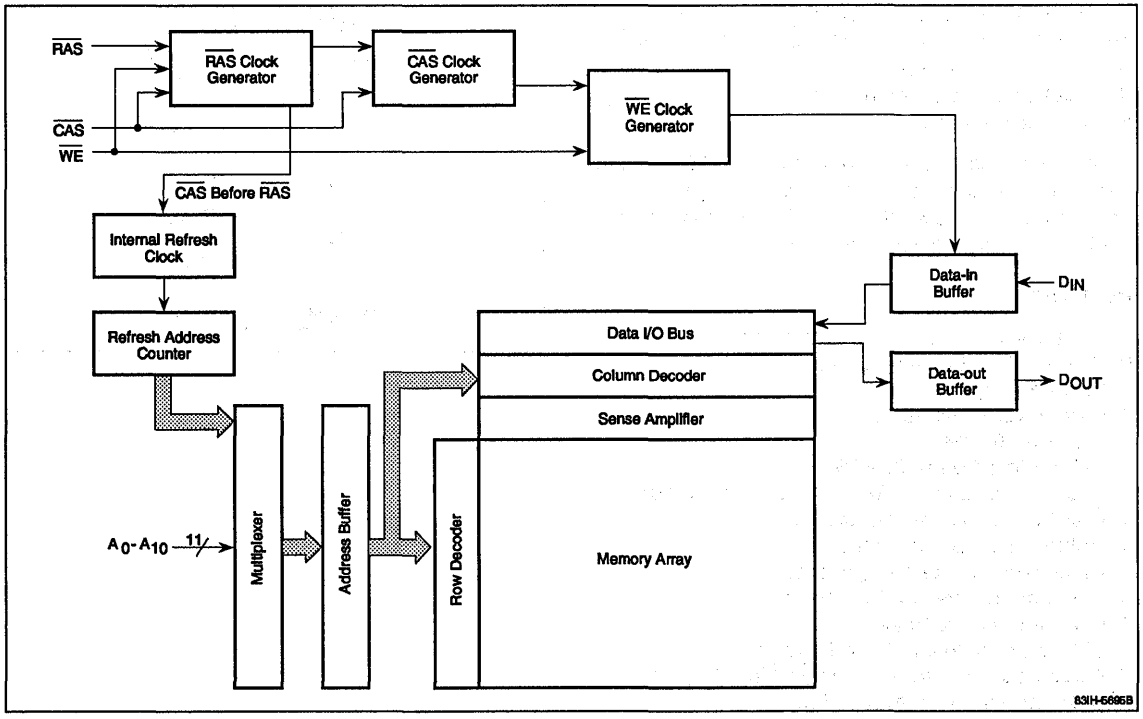
26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

83CL-8687A

Block Diagram



83IH-5686B

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD42641LA-80L	80 ns	160 ns	50 ns	26/20-pin plastic SOJ
μPD42641GS-80L	80 ns	160 ns	50 ns	26/20-pin plastic TSOP (normal pinouts)
μPD42641GSM-80L	80 ns	160 ns	50 ns	26/20-pin plastic TSOP (reverse pinouts)

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		+70	°C

18k

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Address
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, D_{IN}
Output capacitance	C_O	7	pF	D_{OUT}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby current	I_{CC2}		2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min)
			1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V; Address, D_{IN}, $\overline{WE}$ ≥ V_{CC} −0.2 V or ≤ 0.2 V
Input leakage current	$I_{I(L)}$	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OH} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD42641-80 Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC4}		90	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, fast-page cycle, average	I_{CC6}		90	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		40	ns	(Notes 7, 9)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45	ns	(Notes 7, 9)
Column address setup time	t_{ASC}	0		ns	
Row address setup time	t_{ASR}	0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	40		ns	(Note 16)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20	ns	(Notes 7, 9)
Column address hold time	t_{CAH}	15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		ns	(Note 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time, read-write mode	t_{CRP1}	10		ns	(Note 12)
$\overline{CAS}$ hold time	t_{CSH}	80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		ns	(Note 16)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		ns	
Data-in hold time	t_{DH}	15		ns	(Note 15)
Data-in setup time	t_{DS}	0		ns	(Note 15)
Output buffer turnoff delay	t_{OFF}	0	20	ns	(Note 10)
Fast-page cycle time	t_{PC}	50		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	80		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	ns	(Note 9)
Row address hold time	t_{RAH}	12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	80	125,000	ns	
Random read or write cycle time	t_{RC}	160		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	ns	(Note 11)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		ns	(Note 13)

AC Characteristics (cont)

Parameter	Symbol	μPD42641-80 Min	Max	Unit	Test Conditions
Read command setup time	t_{RCS}	0		ns	
Refresh period	t_{REF}		32	ms	Addresses A_0 - A_9
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	45		ns	
$\overline{RAS}$ precharge time	t_{RP}	70		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		ns	(Note 13)
$\overline{RAS}$ hold time	t_{RSH}	20		ns	
Read-write cycle time	t_{RWC}	185		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		ns	
Rise and fall transition time	t_T	3	50	ns	(Note 3)
Write command hold time	t_{WCH}	15		ns	
Write command setup time	t_{WCS}	0		ns	(Note 16)
$\overline{WE}$ hold time	t_{WHR}	15		ns	
Write command pulse width	t_{WP}	15		ns	(Note 14)
$\overline{WE}$ setup time	t_{WSR}	10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only refresh or a CAS before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) AC measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(15) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output pin (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(17) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertently be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

Self-Refresh Cycle

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Operating current, self-refresh mode (average)	I_{CC5}		30, 60, or 90	μA	$\overline{RAS}$ cycling (Note 1, 2, 3)
$\overline{CAS}$ precharge time in CBR refresh mode	t_{CPC1}	20		ns	
$\overline{CAS}$ precharge time from self-refresh mode to read-write mode	t_{CPC2}	100		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time from self-refresh mode to normal read-write mode	t_{CRP2}	200		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time in CBR refresh mode	t_{CRP3}	40		ns	
$\overline{CAS}$ pulse width in self-refresh mode	t_{CSF}	360		ns	(Note 1)
$\overline{RAS}$ cycle time in self-refresh mode	t_{RCF}	360		ns	(Note 2)
$\overline{CAS}$ to $\overline{RAS}$ precharge time from self-refresh to normal read-write mode	t_{RPC2}	100		ns	
$\overline{RAS}$ precharge time in self-refresh mode	t_{RPF}	200		ns	
$\overline{RAS}$ pulse width in self-refresh mode	t_{RSF}	150		ns	

Notes:

(1) With $\overline{RAS}$ cycling at 32 kHz, when $t_{CSF} \leq 35$ ms, I_{CC5} = 1.0 mA. When $t_{CSF} \geq 35$ ms, I_{CC5} = 1.0 mA during the first 35 ms after the self-refresh mode set cycle is applied. Subsequently, the maximum value is as follows.

T_A	Clock (min)	I_{CC5} (t_{CSF})	I_{CC5} (t_{CSF})
0 to 50°C	32 kHz	1.5 mA (< 35 ms)	30 μA (> 35 ms)
0 to 60°C	64 kHz	2 mA (< 18 ms)	60 μA (> 18 ms)
0 to 70°C	128 kHz	4 mA (< 9 ms)	120 μA (> 9 ms)

(2) The value of t_{RCF} depends on operating temperature (T_A).

T_A	t_{RCF} (max)
0 to 50°C	32 μs
0 to 60°C	16 μs
0 to 70°C	8 μs

(3) Average power supply current for self-refresh is measured according to the following conditions.
$\overline{RAS}$ cycling at 32, 64, or 128 kHz;
$\overline{CAS} \leq 0.2$ V; $\overline{WE} \geq V_{CC} - 0.2$ V;
$V_{IH} > V_{CC} - 0.2$ V; $V_{IL} < 0.2$ V;
$t_T \leq 50$ ns; A_0 - A_{10} and D_{IN} = V_{CC} to GND
During self-refresh operation, the $\overline{RAS}$ input must be cycled at or exceeding the minimum frequency requirement.

(4) When exiting self-refresh to a period of read and write operation that inlcudes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh cycle pulse and the first CBR cycle. When entering the self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

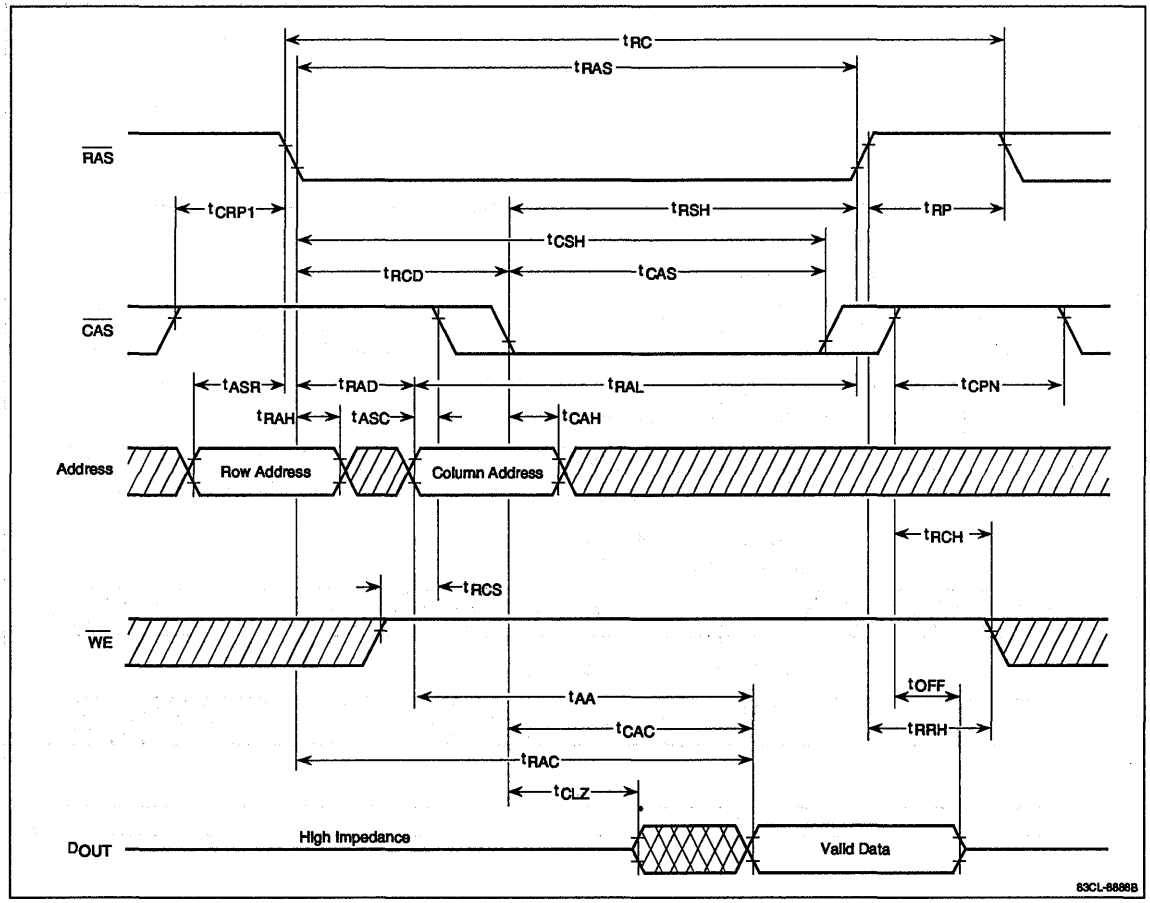
(5) In this period of normal read/write operation, there are no CBR refresh cycles less than 1024 RAS-only refresh cycles.

(6) The time delay between the last self-refresh pulse in one self-refresh cycle and the first self-refresh pulse in the next cycle is defined by t_{RCF} (max) when the intervening period of read and write operation meets the conditions in note 4.

(7) The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 32 μs or less. If some other means of refreshing is used, a burst refresh of all storage cells is necessary just before changing to and just after exiting self-refresh operation.

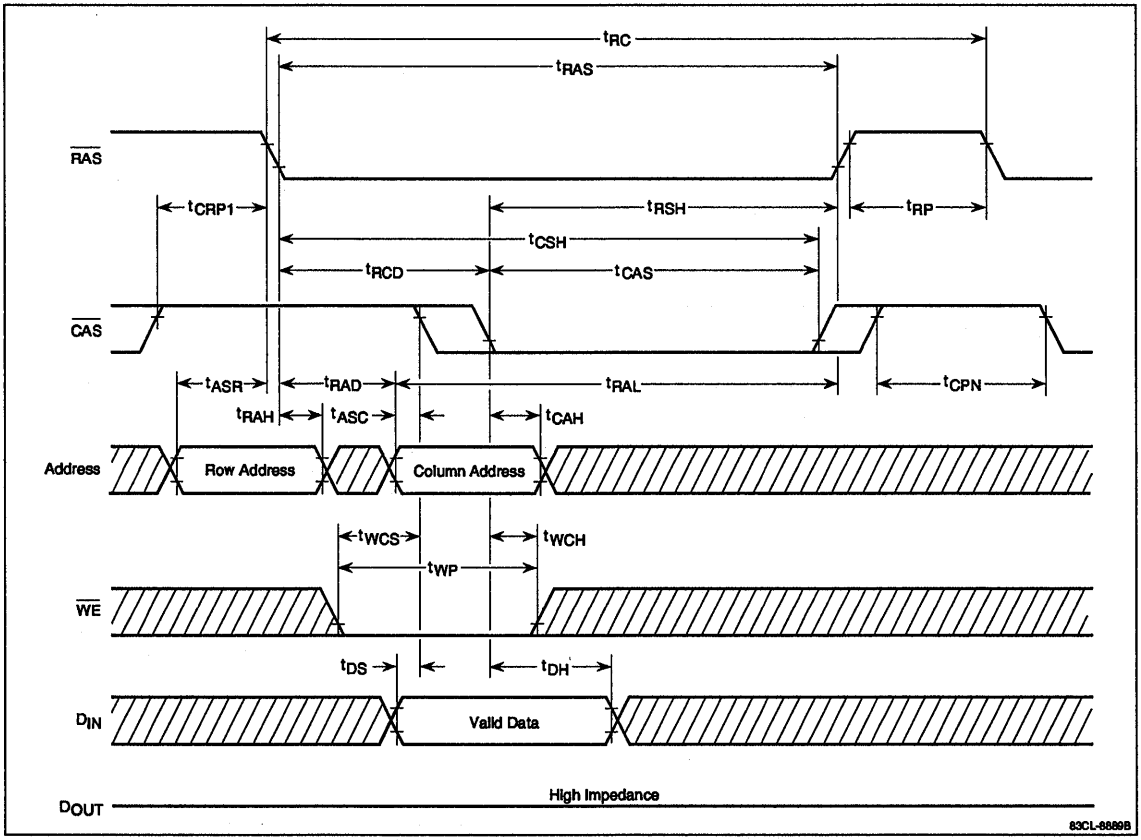
Timing Waveforms

Read Cycle



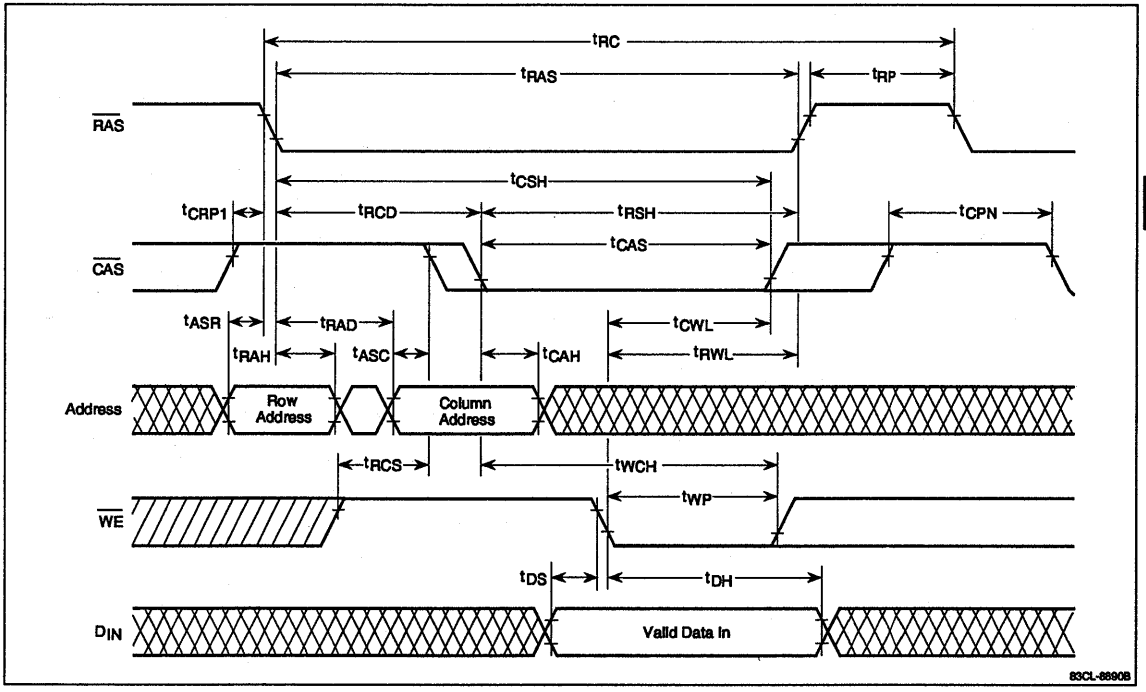
Timing Waveforms (cont)

Early Write Cycle



Timing Waveforms (cont)

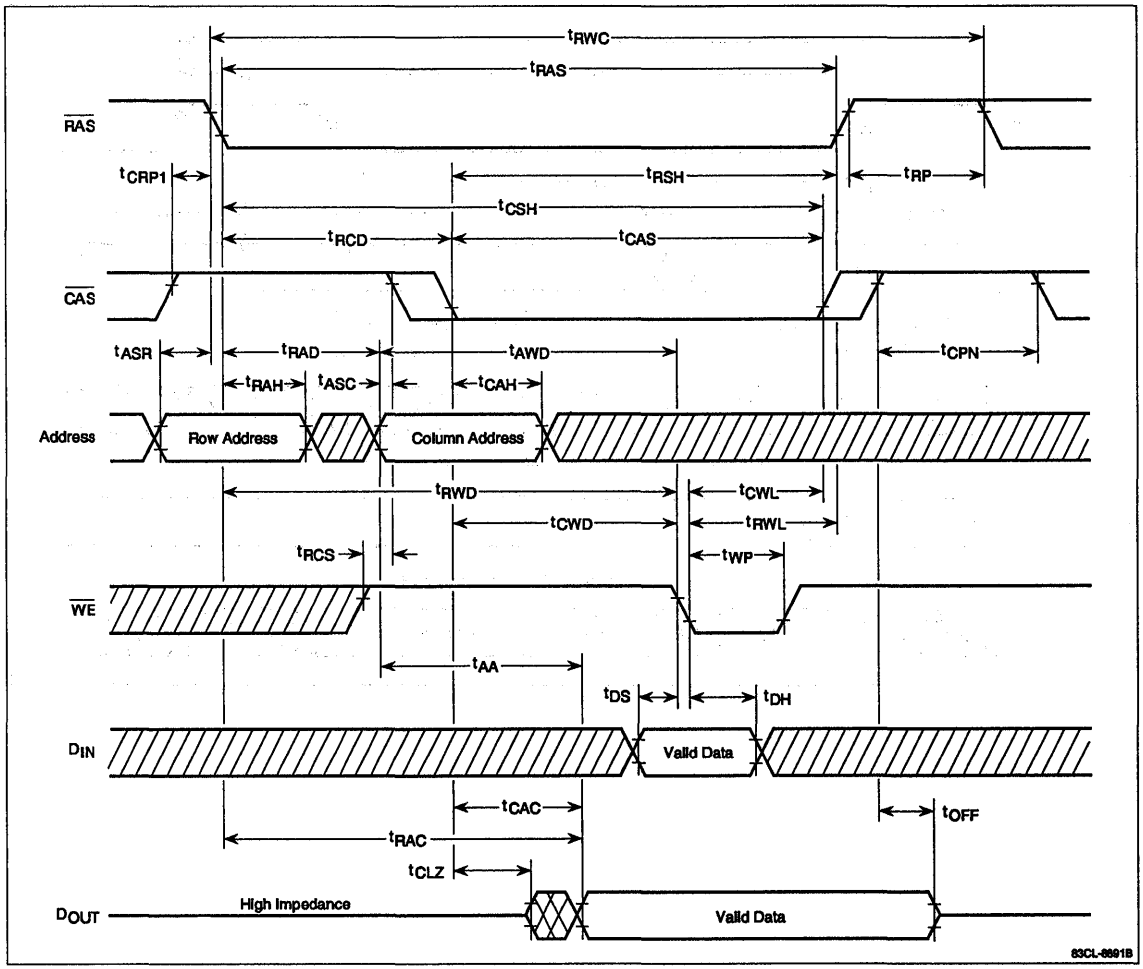
Late Write Cycle



18k

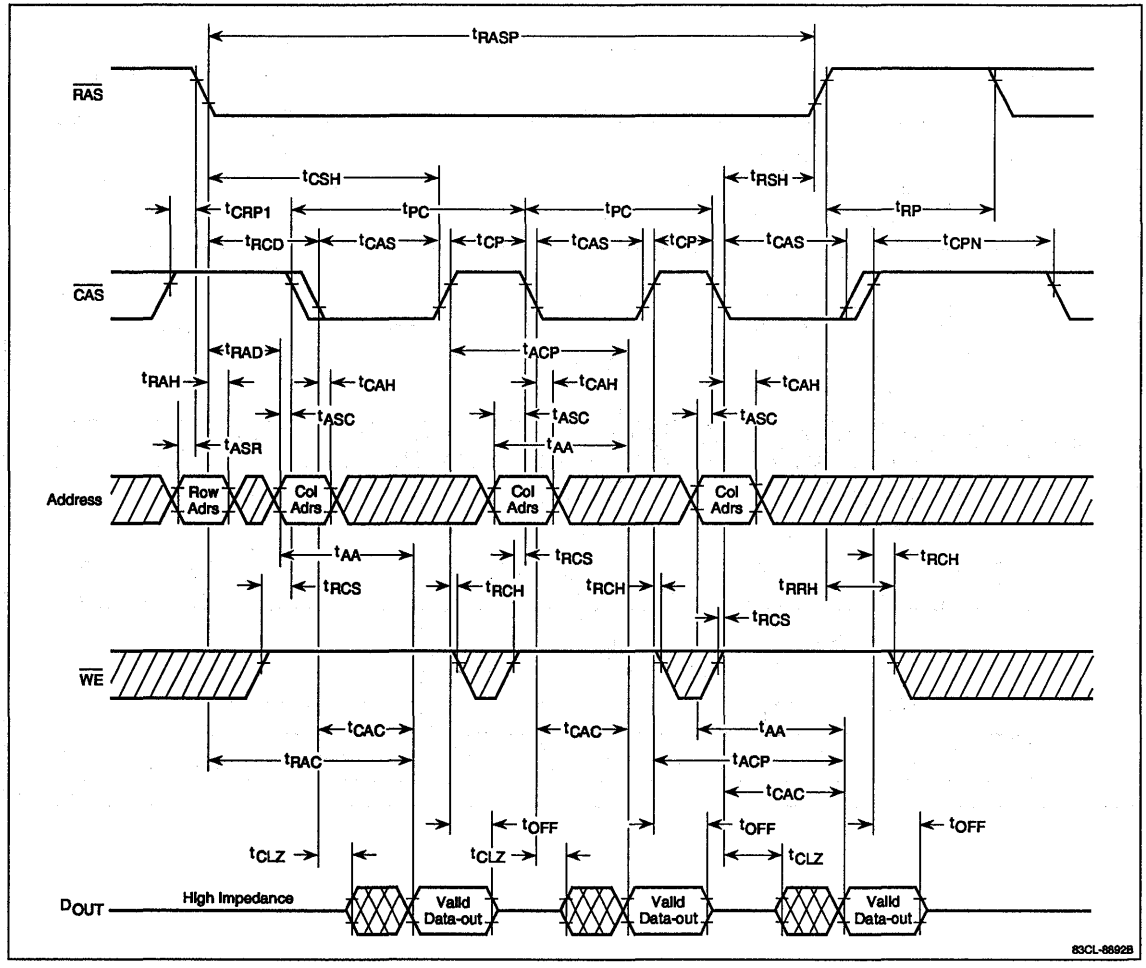
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

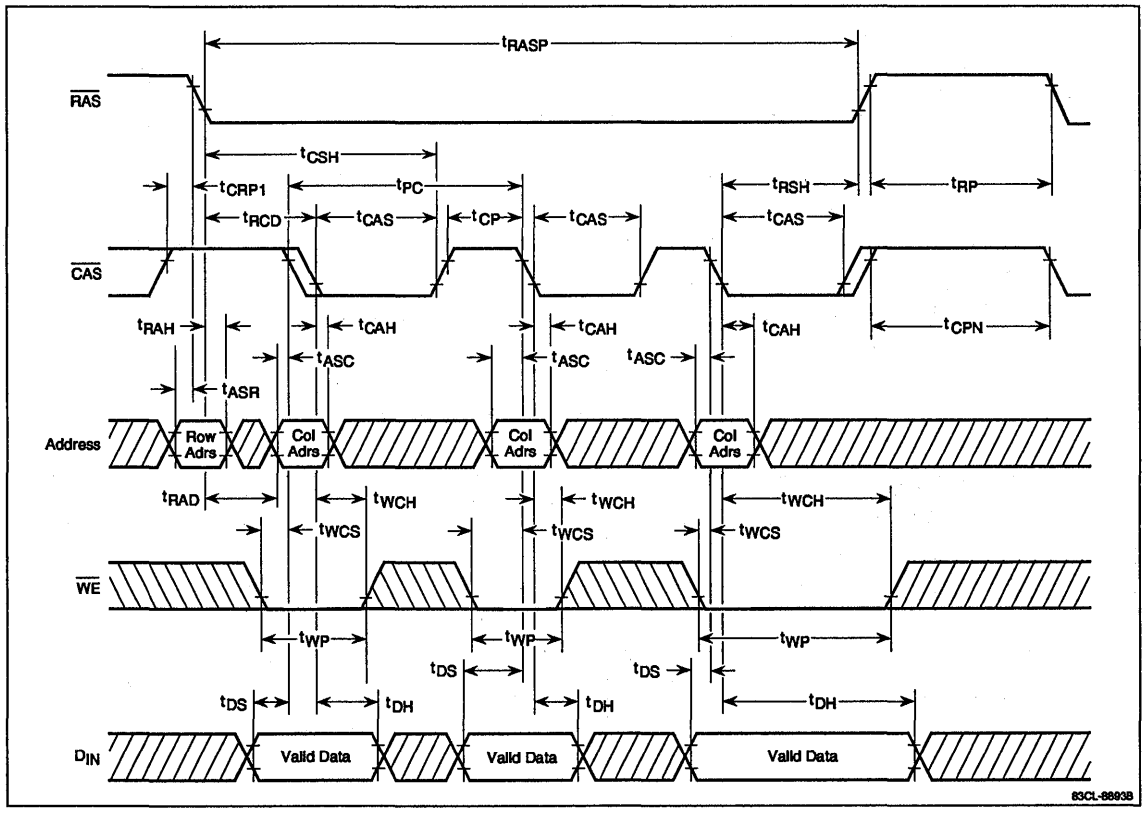
Fast-Page Read Cycle



18k

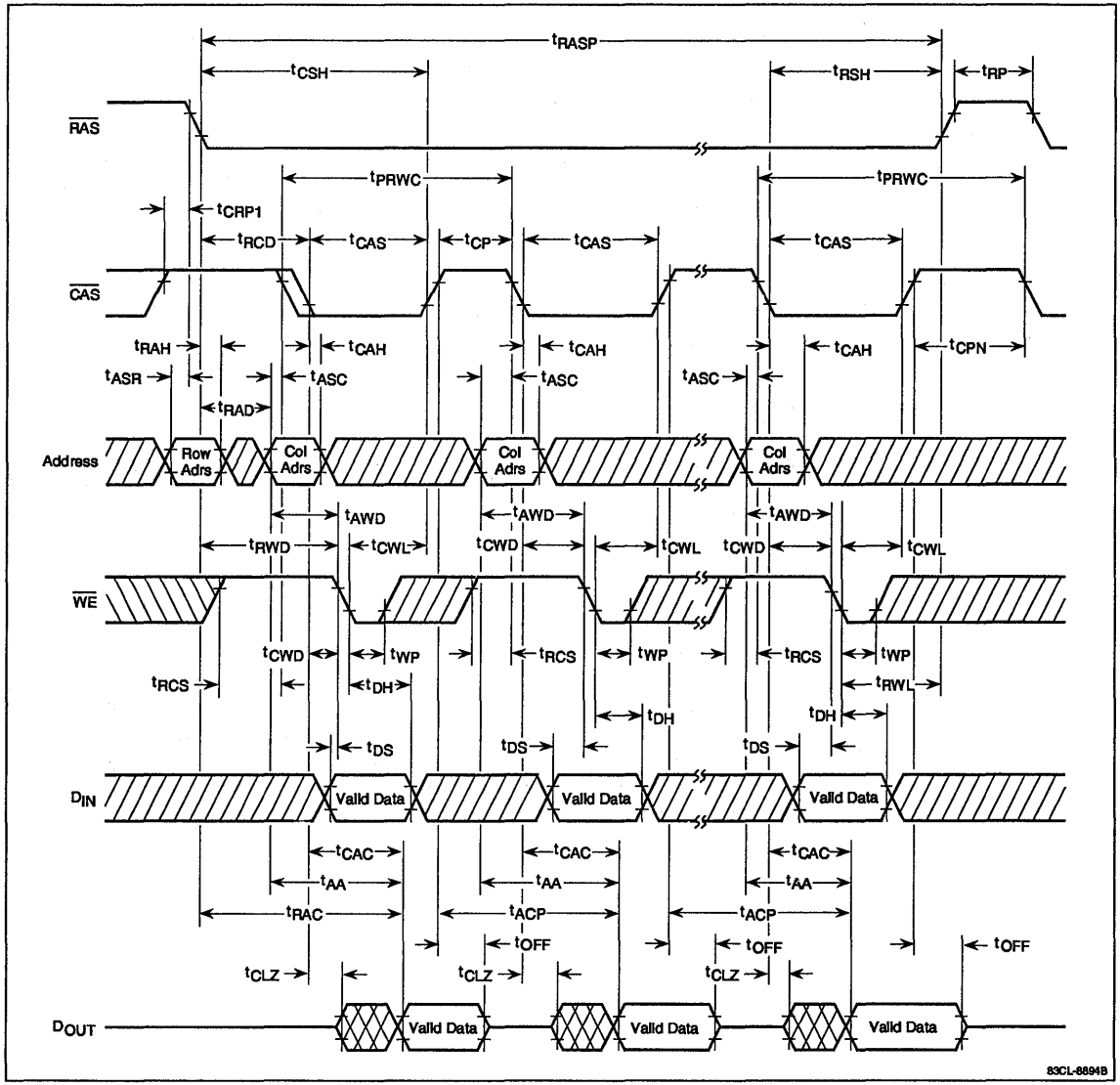
Timing Waveforms (cont)

Fast-Page Early Write Cycle



Timing Waveforms (cont)

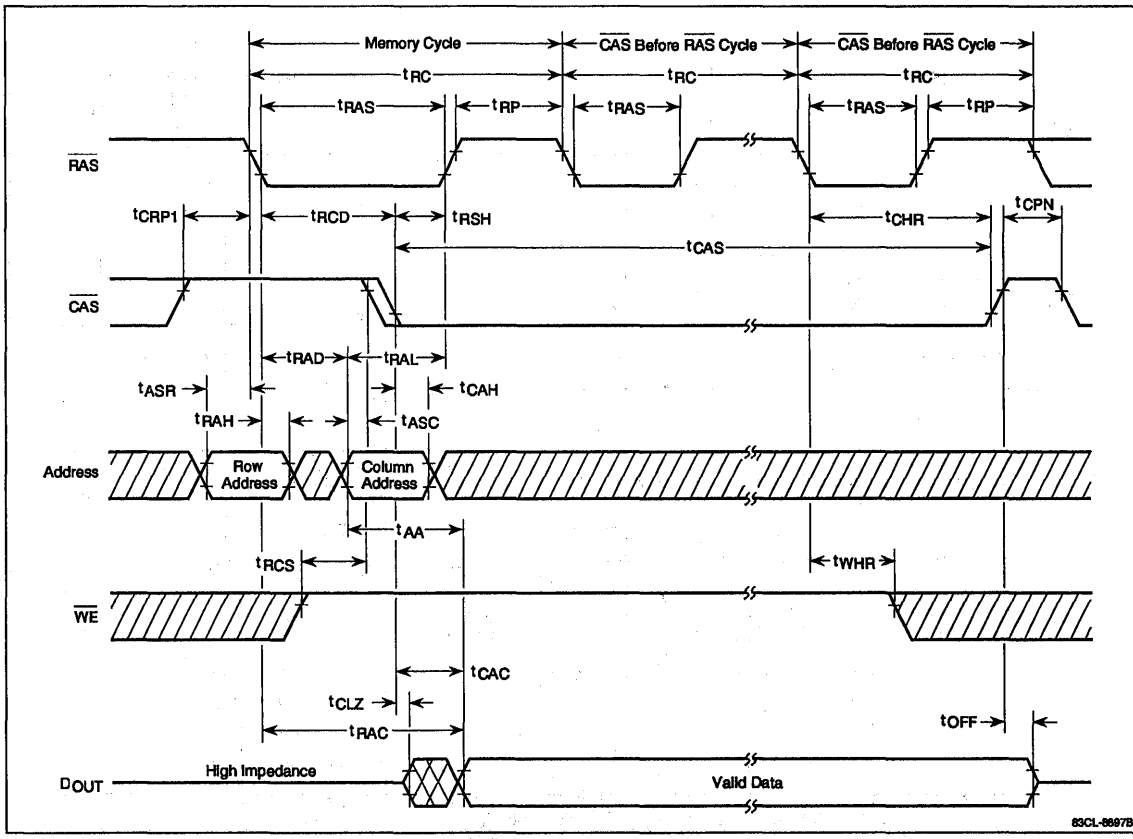
Fast-Page Read-Write/Read-Modify-Write Cycle



18k

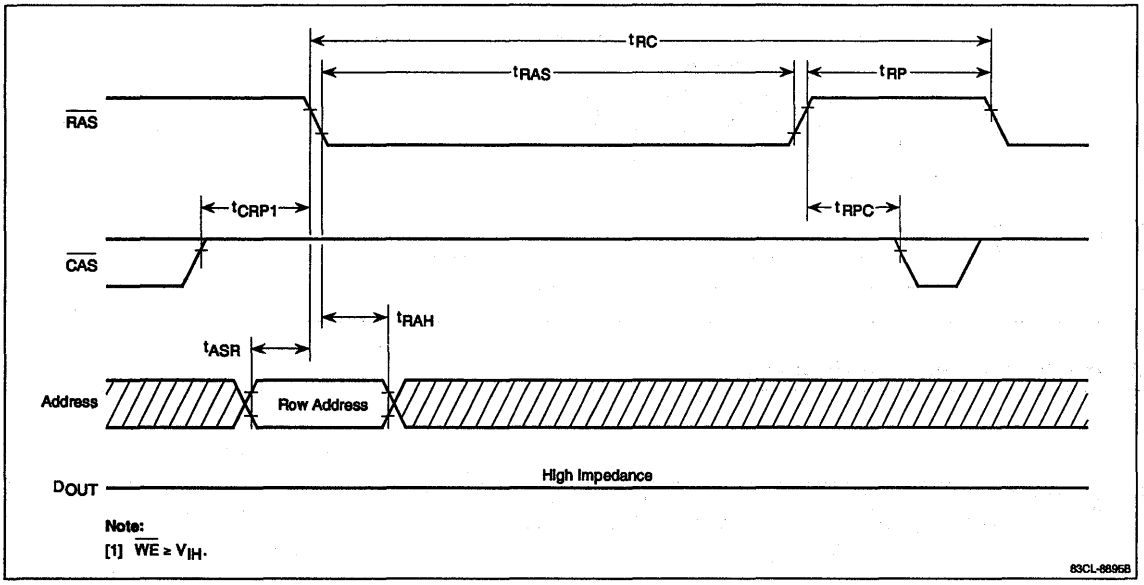
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

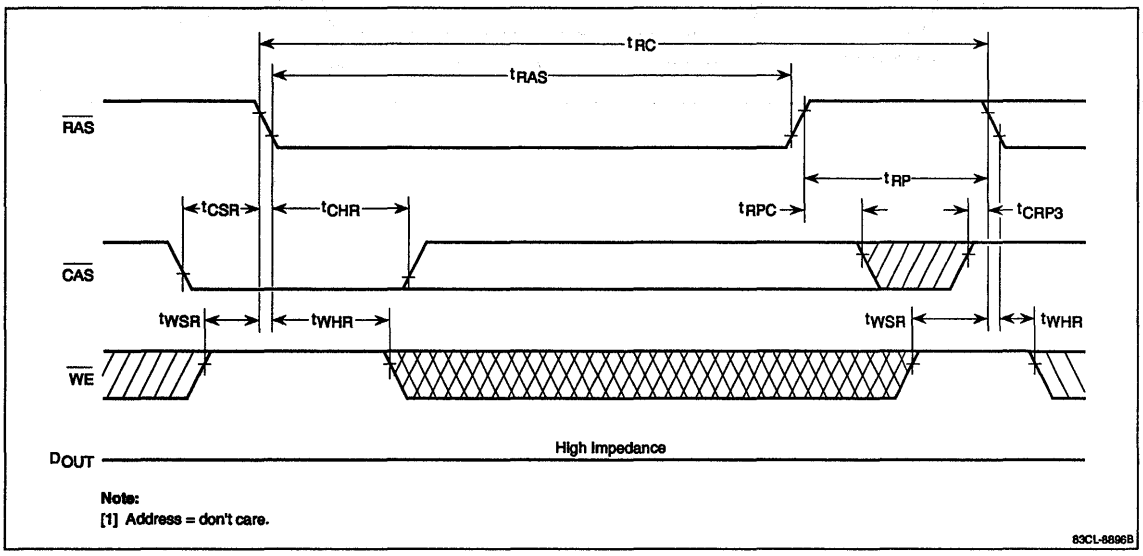
$\overline{RAS}$-Only Refresh Cycle



Note:
[1] $\overline{WE} \geq V_{IH}$.

83CL-8895B

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] Address = don't care.

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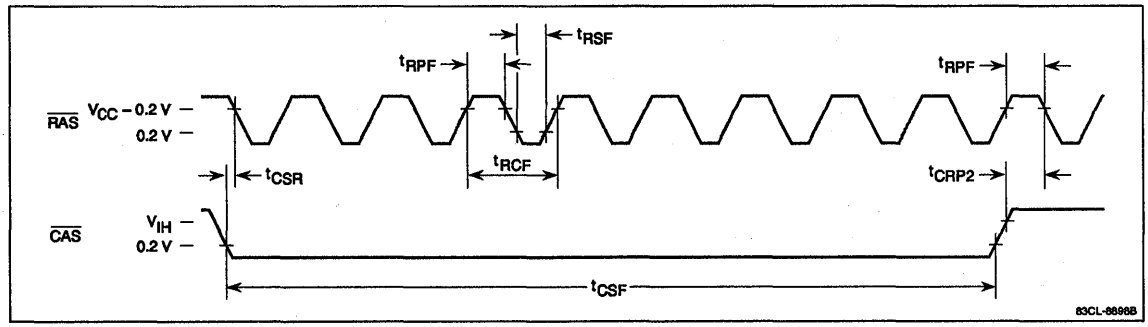
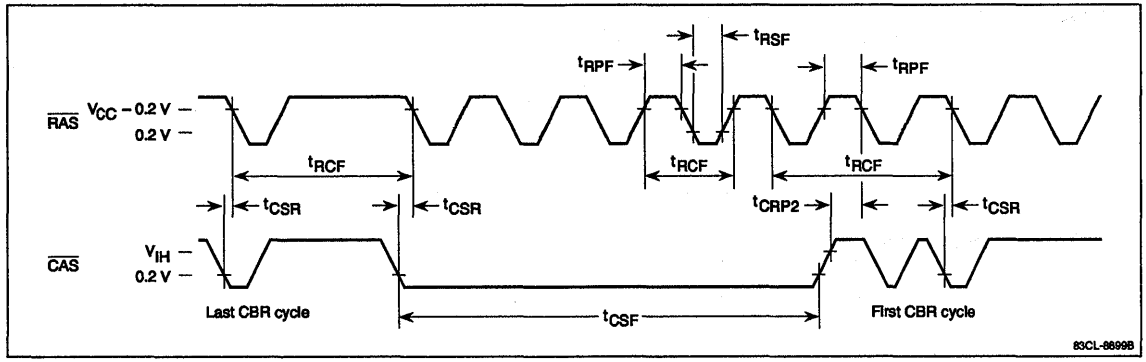
Timing Waveforms (cont)

Self-Refresh Cycle

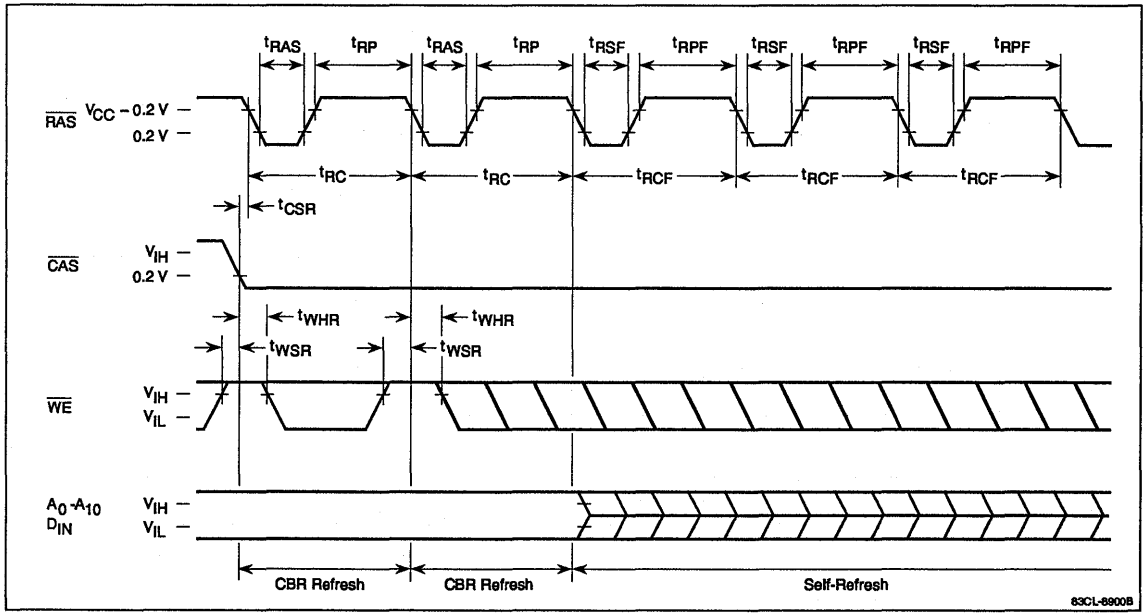


Normal Refresh/Self-Refresh Timing



Timing Waveforms (cont)

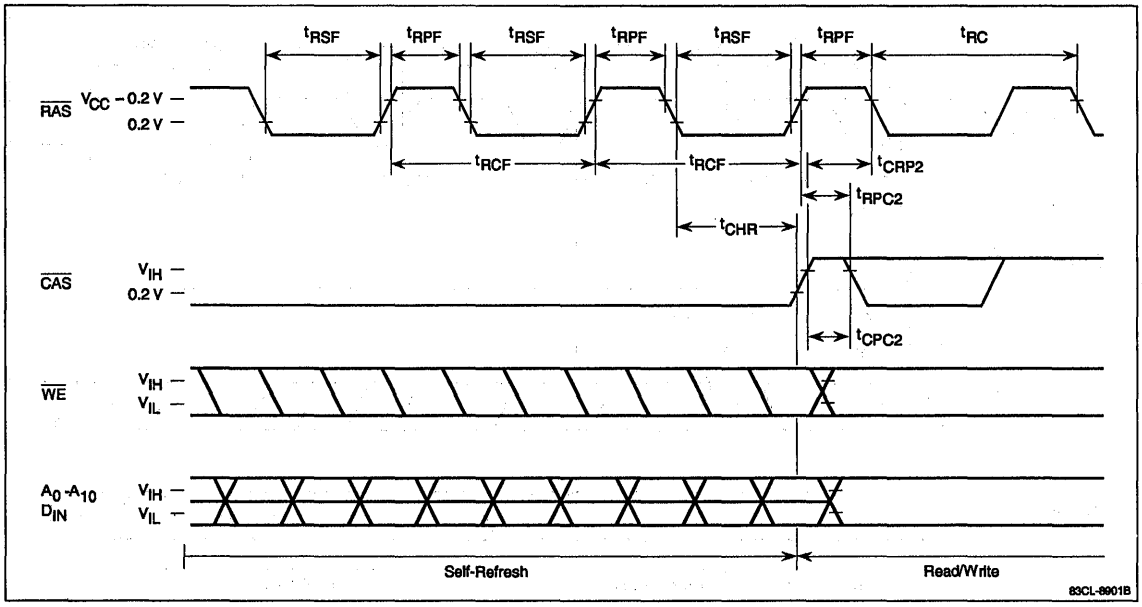
Self-Refresh Mode Set Cycle



18k

Timing Waveforms (cont)

Self-Refresh Mode Reset Cycle



Description

The μPD42644 is a fast-page, low-power dynamic RAM organized as 1,048,576 words by 4 bits and designed to operate from a single +5-volt power supply. Advanced polycide technology minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the outputs by maintaining $\overline{CAS}$ low. Data outputs return to high impedance when $\overline{CAS}$ goes high. Fast-page read and write cycles can be executed by cycling $\overline{CAS}$.

Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by means of $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 1,024 address combinations of A_0 - A_9 during a 16-ms refresh period.

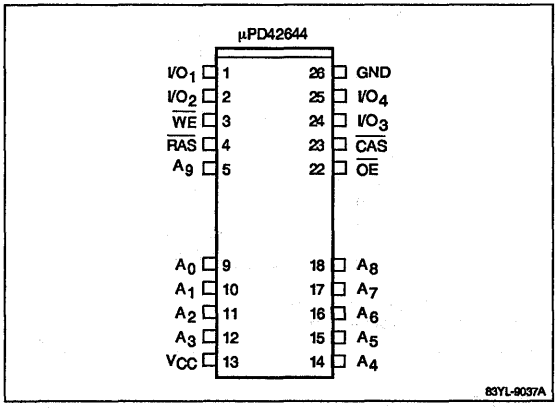
A low-power self-refresh cycle allows the μPD42644 to retain data for extended periods of time with very low power consuption (30 μA at 50°C). This feature allows the μPD42644 to be used in battery backup applications with greater savings in power consumption.

Features

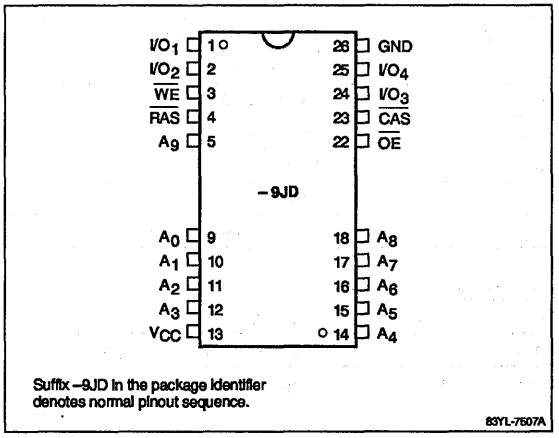
- 1,048,576 by 4-bit organization
- Single +5-volt power supply
- Fast-page option
- Low power dissipation
  - — 90 mA active
  - — 1.0 mA standby (CMSO interface)
  - — 30 μA self-refresh (t_{RCF} = 32 μs, T_A = 50°C)
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- Multiplexed address inputs
- On-chip substrate bias generator
- TTL-compatible inputs and outputs
- Automatic self-refreshing by $\overline{RAS}$ input cycling
- Nonlatched, three-state outputs
- Low input capacitance
- 1024 refresh cycles every 16 ms
- 26/20-pin plastic SOJ (300 mil), 20-pin plastic ZIP, and 26/20-pin plastic TSOP packaging

Pin Configurations

26/20-Pin Plastic SOJ

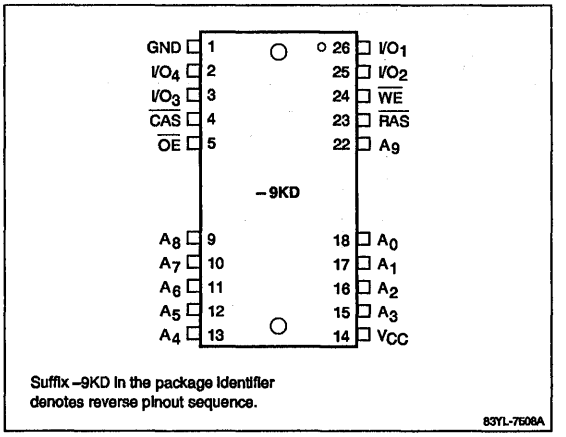


26/20-Pin Plastic TSOP (Normal Pinouts)



Pin Configurations (cont)

26/20-Pin Plastic TSOP (Reverse Pinouts)



Suffix –9KD in the package identifier denotes reverse pinout sequence.

83YL-7508A

Pin Identification

Name	Function
A_0 - A_9	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CAS}$	Column address strobe
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Voltage on any pin relative to GND	–1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	–55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	–1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

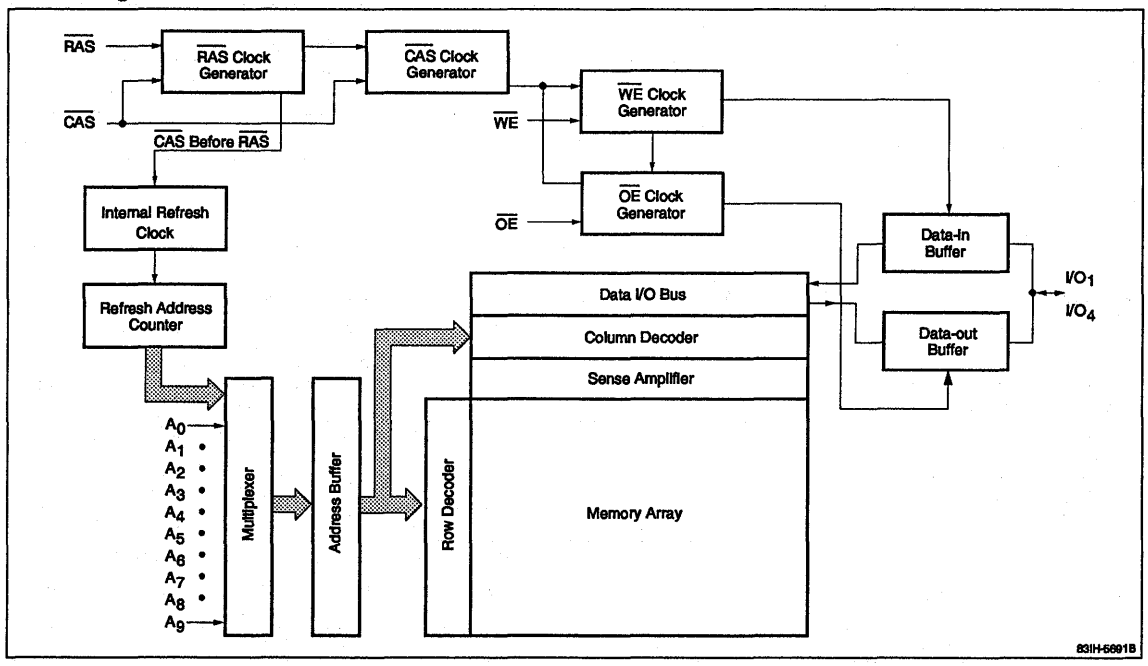
Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_4

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; A_0 - A_9, I/O and $\overline{WE}$ ≥ V_{CC} – 0.2 or ≤ 0.2 V; $I_{I/O}$ = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –5 mA

Block Diagram



Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Power Option	Package
μPD42644LA-80L	80 ns	160 ns	50 ns	Standard	26/20-pin plastic SOJ (300 mil)
μPD42644GS-80L	80 ns	160 ns	50 ns	Standard	26/20-pin plastic TSOP (normal pinouts)
μPD42644GSM-80L	80 ns	160 ns	50 ns	Standard	26/20-pin plastic TSOP (reverse pinouts)

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-80		-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		90		80	mA	$\overline{RAS}$ and $\overline{CAS}$ cycling; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH}; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC4}		90		80	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min; I_O = 0 mA (Note 5)
Operating current, self-refresh mode, average	I_{CC5}		30		30	μA	$\overline{RAS}$ cycling at 32 kHz (Notes 16, 17, 18)
			60		60	μA	$\overline{RAS}$ cycling at 64 kHz (Notes 16, 17, 18)
			120		120	μA	$\overline{RAS}$ cycling at 128 kHz (Notes 16, 17, 18)
Operating current, fast-page cycle, average	I_{CC6}		90		60	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; I_O = 0 mA (Note 5)
Access time from column address	t_{AA}		40		50	ns	(Notes 3, 4, 7, 8)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55	ns	(Notes 3, 4, 7, 8)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	65		80		ns	(Note 14)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25	ns	(Notes 3, 4, 7, 8)
Column address hold time	t_{CAH}	15		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		20		ns	
$\overline{CAS}$ to output in low impedance	t_{CLZ}	0		0		ns	(Notes 4, 7)
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		15		ns	
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP1}	10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		55		ns	(Note 14)

AC Characteristics (cont)

Parameter	Symbol	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		20		ns	(Note 13)
Data-in setup time	t_{DS}	0		0		ns	(Note 13)
Access time from $\overline{OE}$	t_{OEA}		20		25	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ delay data time	t_{OED}	20		25		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ to inactive setup time	t_{OES}	0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	20	0	25	ns	(Note 9)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	ns	(Note 9)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		ns	(Notes 6, 7)
Fast-page cycle time	t_{PC}	50		60		ns	(Note 6)
Fast-page read-modify-write cycle time	t_{PRWC}	100		120		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		100	ns	(Notes 3, 4, 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	17	50	ns	(Note 8)
Row address hold time	t_{RAH}	12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	40		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	80	125,000	100	125,000	ns	
Random read or write cycle time	t_{RC}	160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	70	ns	(Note 8)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		32		16	ms	Addresses A_0 - A_9
$\overline{RAS}$ precharge time	t_{RP}	70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	(Note 11)
$\overline{RAS}$ hold time	t_{RSH}	20		25		ns	
Read-write cycle time	t_{RWC}	210		250		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	105		130		ns	(Note 14)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		20		ns	(Note 12)
Write command setup time	t_{WCS}	0		0		ns	(Note 14)
$\overline{WE}$ hold time	t_{WHR}	15		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command pulse width	t_{WP}	15		20		ns	(Note 12)
$\overline{WE}$ setup time	t_{WSR}	10		10		ns	

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved. At the end of the initial power-up sequence, it is recommended that either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle be executed while $\overline{WE} \geq V_{IH}$ to ensure normal operation.

(3) Ac measurements assume $t_T = 5$ ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70 °C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V and V_{OL} = 0.8 V).

(8) If $t_{RCD} \leq t_{RCS}$ (max) and $t_{RAD} \leq t_{RAD}$ (max) access time is defined by t_{RAC} (max). If $t_{RCD} \geq t_{RCD}$ (max) access time is defined by t_{CAC} (max) and if $t_{RAD} \geq t_{RAD}$ (max) access time is defined by t_{AA} (max).

(9) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs become open-circuit and are not referenced to V_{OH} or V_{OL}.

(10) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(11) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(12) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write cycles, both t_{WCS} and t_{WCH} must be met.

(13) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(14) t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the I/O pins will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), then the cycle is a read-write cycle and the data I/O pins will contain data read from the selected cells. If neither of the above conditions is met, the condition of the data I/O pins (at access time and until $\overline{CAS}$ returns to V_{IH}) is indeterminate.

(15) A test mode may be initiated by executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at V_{IL}. This mode also may inadvertantly be initiated during power-up because external control of the signal lines is very difficult during this period. It is therefore recommended that while $\overline{WE}$ is held at V_{IH}, either a $\overline{RAS}$-only or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle should be executed at any time after the end of the initial power-up sequence to ensure normal device operation.

(16) When $t_{CSF} \leq 35$ ms, I_{CC5} depends on the $\overline{RAS}$ clock; I_{CC5} (typ) = 1.5 mA. When $t_{CSF} \geq 35$ ms, I_{CC5} (typ) = 1.5 mA in the first 35 ms after a self-refresh set cycle is applied (depending on the status of $\overline{RAS}$). Subsequently, I_{CC5} is 120 μA or as shown in the following table for the –L version.

Operating Temperature (T_A)	Clock Frequency (min)	Self-Refresh Current (max)
0 to 50°C	32 kHz	30 μA at 32 kHz
0 to 60°C	64 kHz	60 μA at 64 kHz
0 to 70°C	128 kHz	120 μA at 128 kHz

(17) t_{RCF} depends on operating temperature as reflected in the table below:

Operating Temperature (T_A)	t_{RCF} (max)
0 to 50°C	32 μs
0 to 60°C	16 μs
0 to 70°C	8 μs

(18) Average power supply current required for self-refreshing is measured according to the following conditions: $\overline{RAS}$ is cycling at 32, 64 or 128 kHz; $\overline{CAS} \leq 0.2$ V; $\overline{WE} \geq V_{CC} - 0.2$ V; $V_{IH} > V_{CC} - 0.2$ V; $V_{IL} < 0.2$ V; $t_T \leq 50$ ns; A_0 - A_9 and I/O = V_{CC} to GND. During self-refresh operation, the $\overline{RAS}$ input must be cycled at or exceeding the minimum frequency requirements.

Self-Refresh Cycle

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
$\overline{CAS}$ pulse width in self-refresh operation	t_{CSF}	360		ns	(Note 1)
$\overline{RAS}$ cycle time in self-refresh operation	t_{RCF}	360	(Note 2)	ns	
$\overline{RAS}$ precharge time in self-refresh operation	t_{RPF}	200		ns	
$\overline{RAS}$ pulse width in self-refresh operation	t_{RSF}	150	1000	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time from self-refresh operation to normal read/write operation	t_{CRP2}	200		ns	
$\overline{CAS}$ setup time for self-refresh operation	t_{CSR2}	10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time $\overline{CAS}$ before $\overline{RAS}$ refresh operation	t_{CRP3}	40		ns	
$\overline{CAS}$ precharge time in $\overline{CAS}$ before $\overline{RAS}$ refresh operation	t_{CPC}	20		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time from self-refresh operation to normal read/write operation	t_{RPC2}	100		ns	

Notes:

(1) When $t_{CSF} \leq 35$ ms, I_{CC5} depends on the $\overline{RAS}$ clock; I_{CC5} (typ) = 1.5 mA. When $t_{CSF} \geq 35$ ms, I_{CC5} (typ) = 1.5 mA in the first 35 ms after a self-refresh set cycle is applied (depending on the status of $\overline{RAS}$). Subsequently, I_{CC5} is 120 μA or as shown in the following table for the –L version.

Operating Temperature (T_A)	Clock Frequency (min)	Self-Refresh Current (max)
0 to 50°C	32 kHz	30 μA at 32 kHz
0 to 60°C	64 kHz	60 μA at 64 kHz
0 to 70°C	128 kHz	120 μA at 128 kHz

(2) The value for t_{RCF} (min) is specified in AC Characteristics. The value for t_{RCF} (max) is dependent upon temperature as shown in the table below:

Operating Temperature (T_A)	t_{RCF} (max)
0 to 50°C	32 μs
0 to 60°C	16 μs
0 to 70°C	8 μs

(3) When exiting self-refresh to a period of read and write operation that includes $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, t_{RCR} is delayed between the last self-refresh cycle pulse and the first $\overline{CAS}$ before $\overline{RAS}$ cycle. When entering self-refresh operation, t_{RCF} is the delay between the last $\overline{CAS}$ before $\overline{RAS}$ cycle and the first self-refresh pulse.

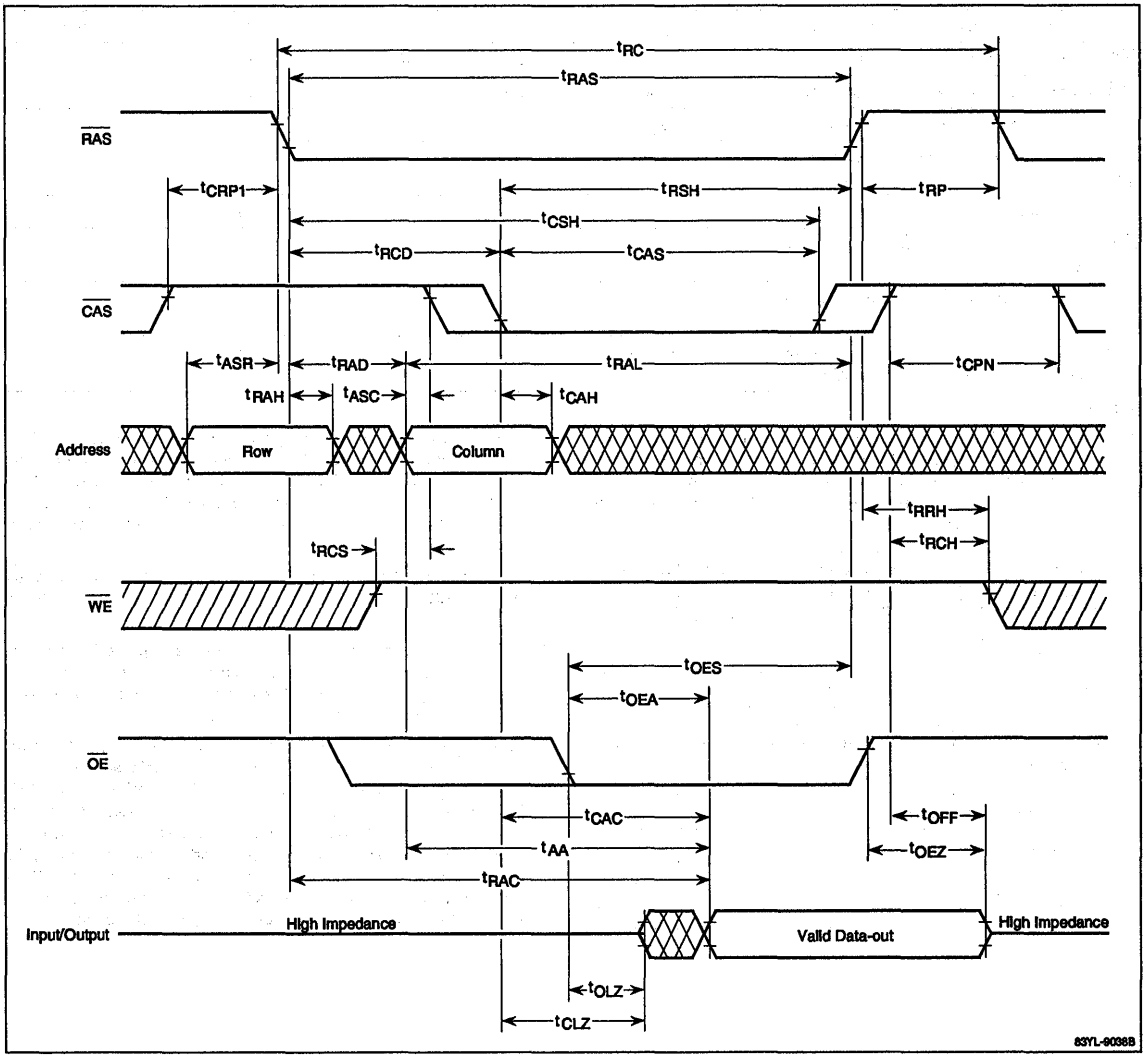
(4) In this period of normal read/write operation, there are no $\overline{CAS}$ before $\overline{RAS}$ refresh cycles or less than 1024 $\overline{RAS}$-only refresh cycles.

(5) The time delay beetween the last self-refresh pulse in one self-refresh cycle and the first self-refresh pulse in the next cycle is defined by t_{RCF} (max) when the intervening period of read and write operation meets the conditions in note 3.

(6) The bulit-in counter generates the refresh address in self-refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh cycles. Since this address increments sequentialy from the last cycle in either self-refresh or $\overline{CAS}$ before $\overline{RAS}$ operation to the first cycle in the alternate refresh mode, $\overline{CAS}$ before $\overline{RAS}$ refreshing should be used during normal read and write operation to refresh one address location every 32 μs or less. If some other means of refreshing is used, it is necessary to execute a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

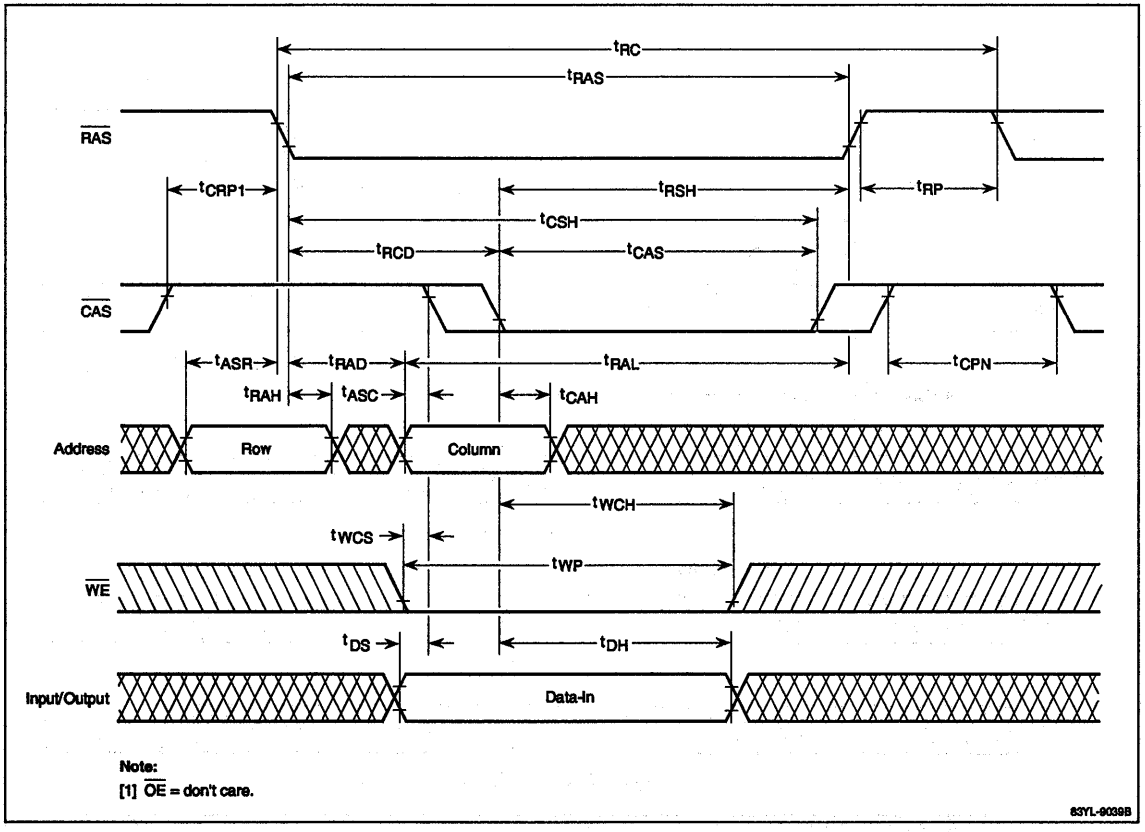
Timing Waveforms

Read Cycle



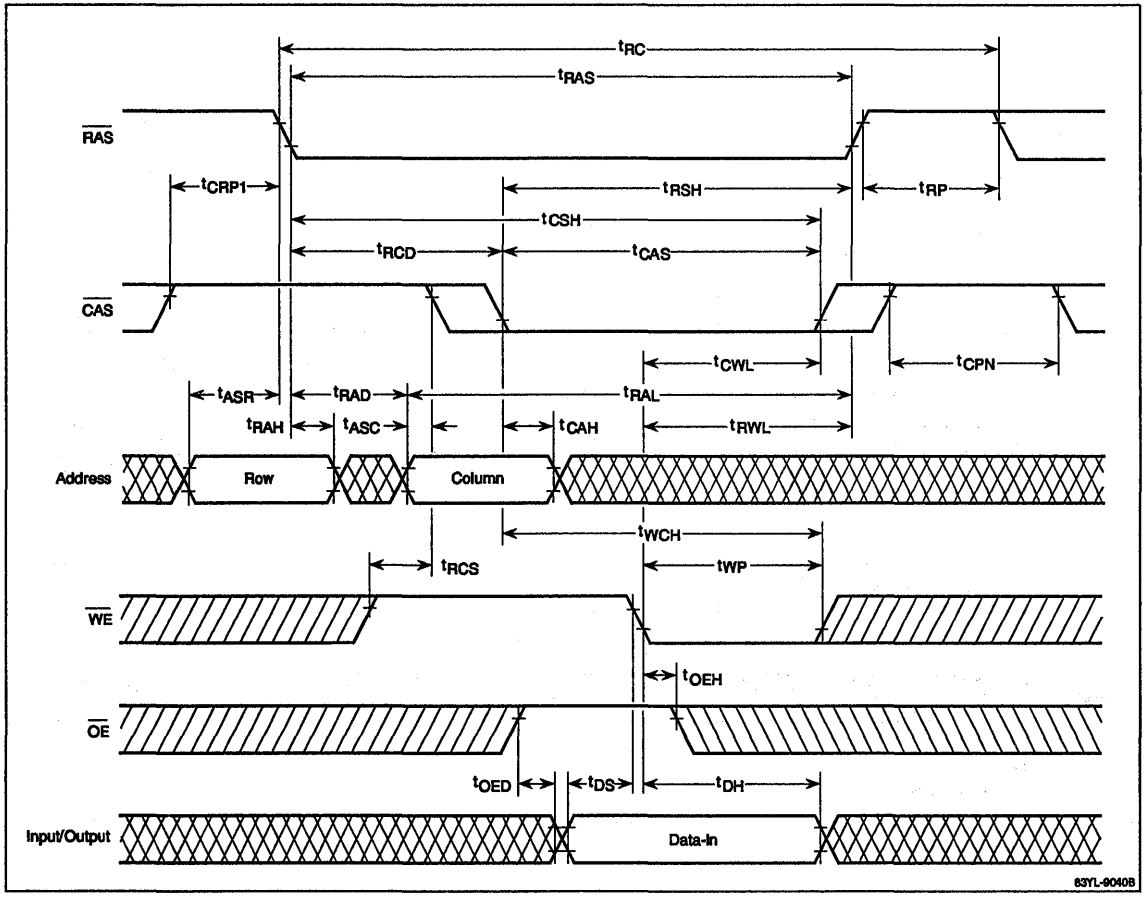
Timing Waveforms (cont)

Early Write Cycle



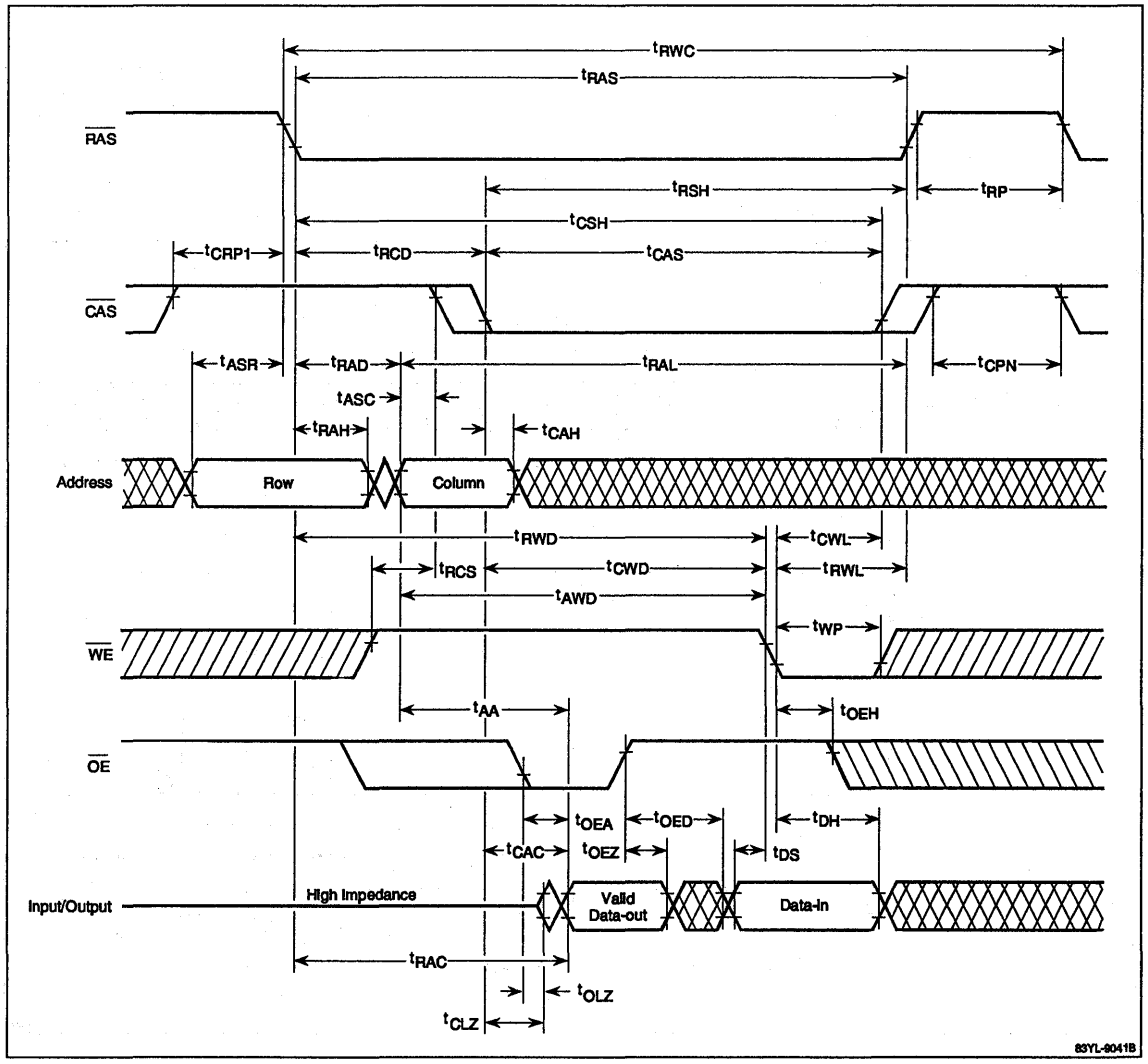
Timing Waveforms (cont)

Late Write Cycle



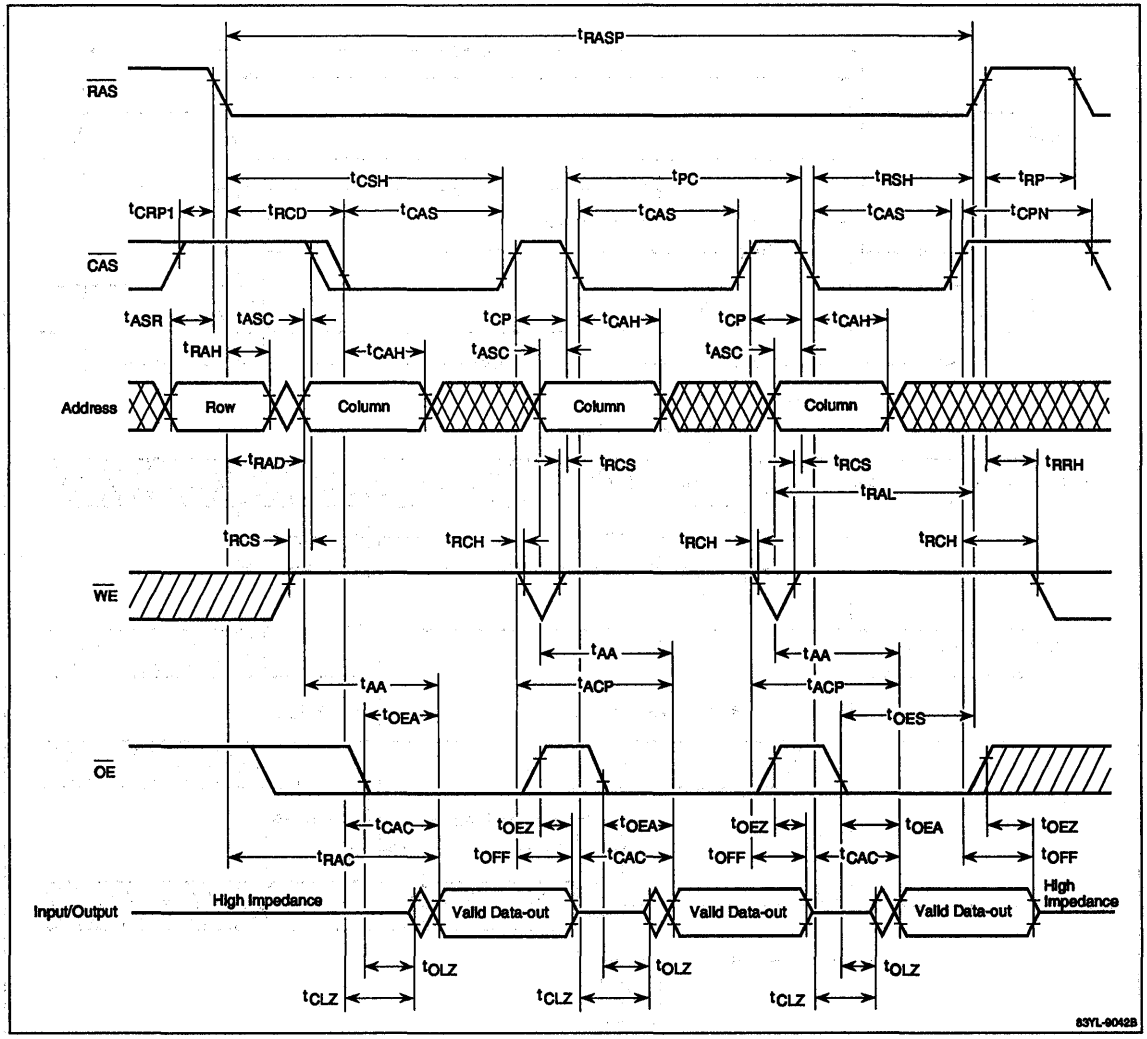
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



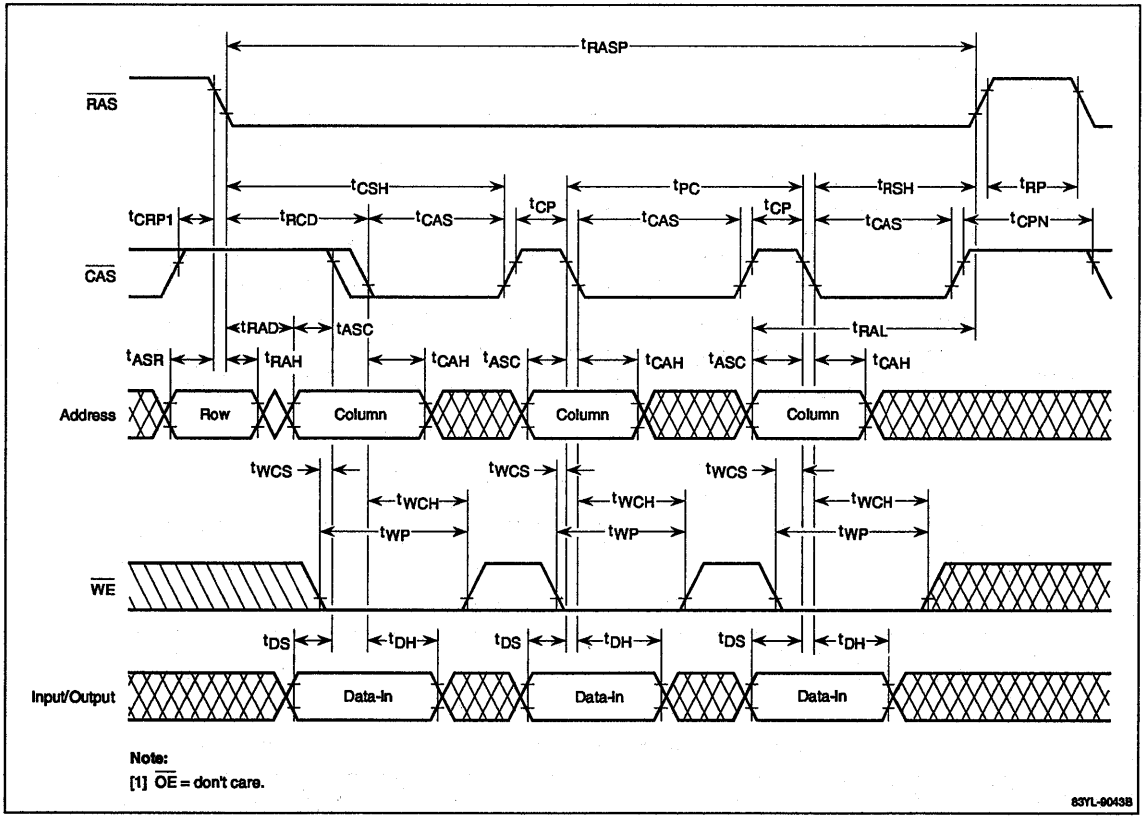
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Early Write Cycle

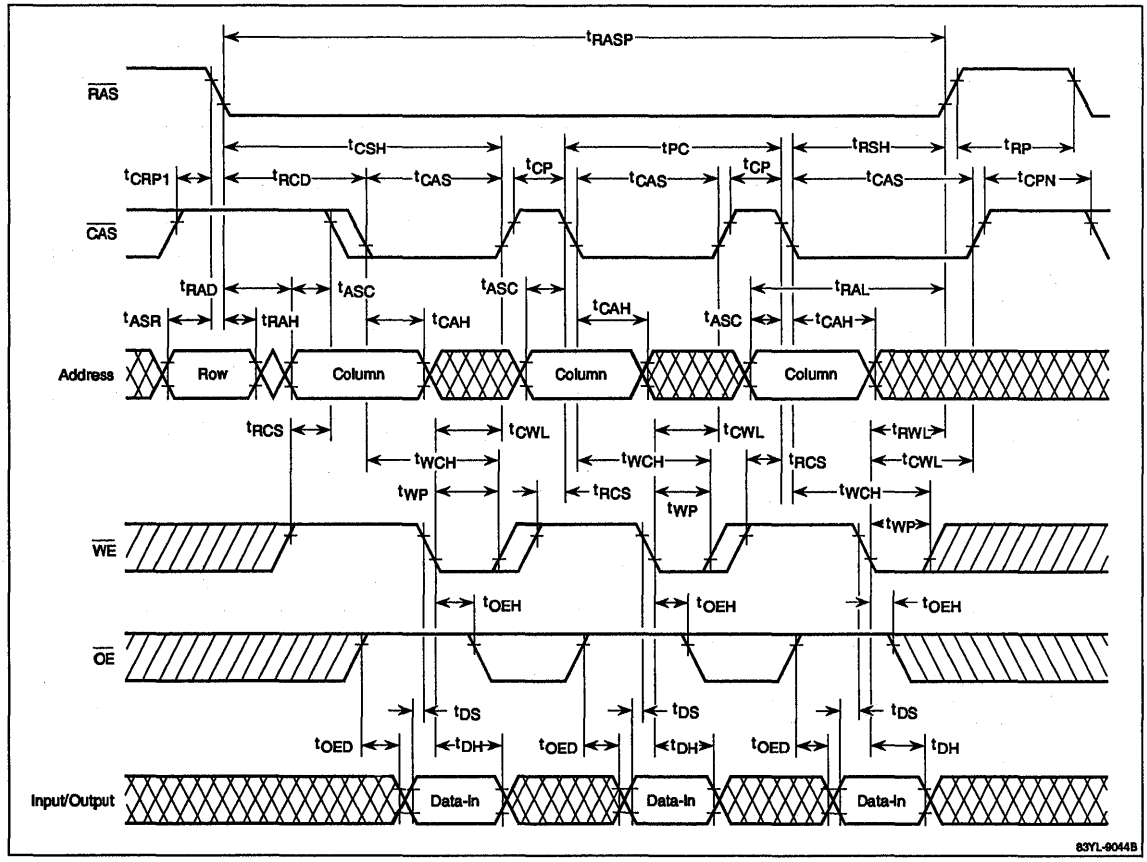


Note:
[1] $\overline{OE}$ = don't care.

83YL-9043B

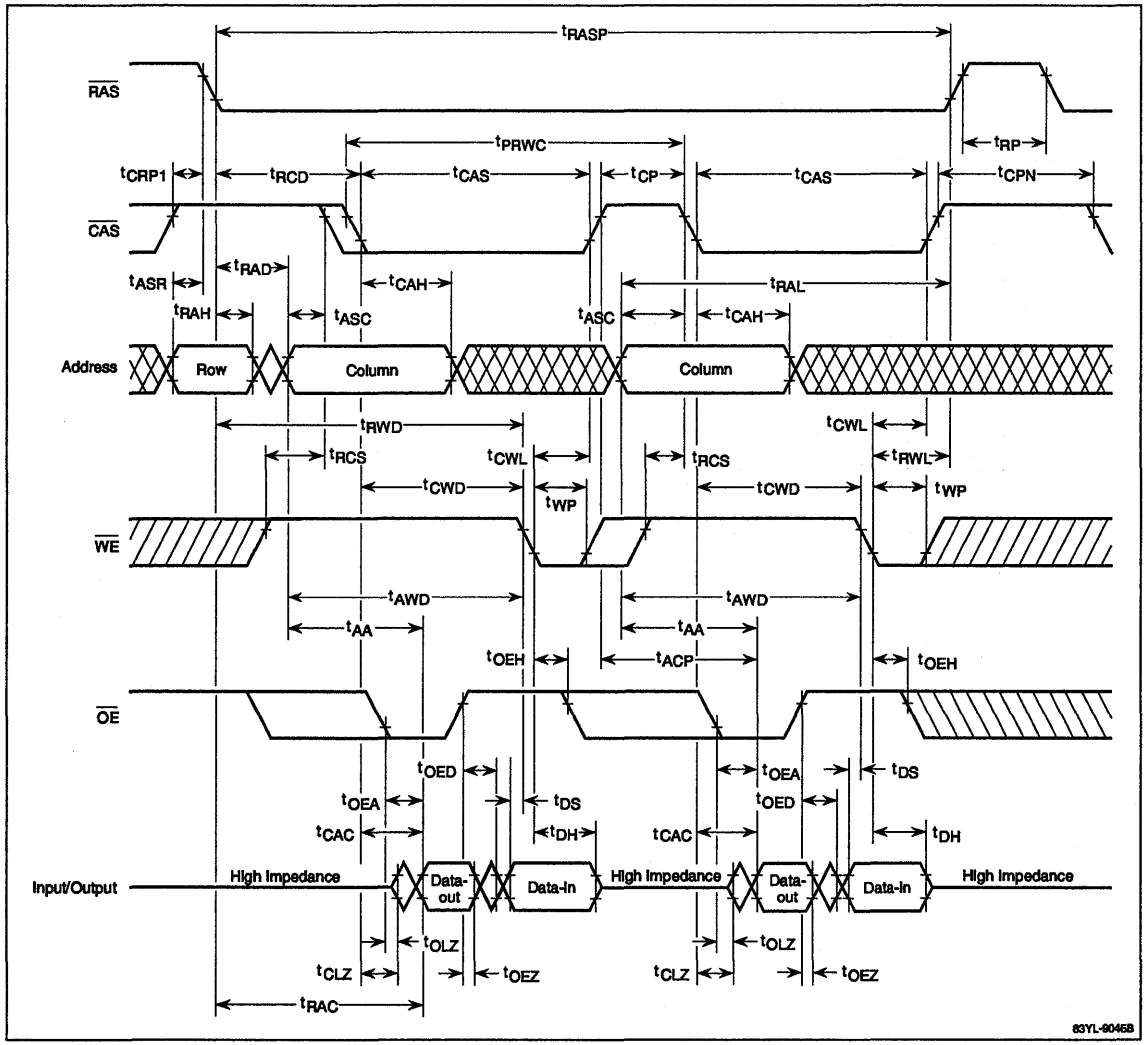
Timing Waveforms (cont)

Fast-Page Late Write Cycle



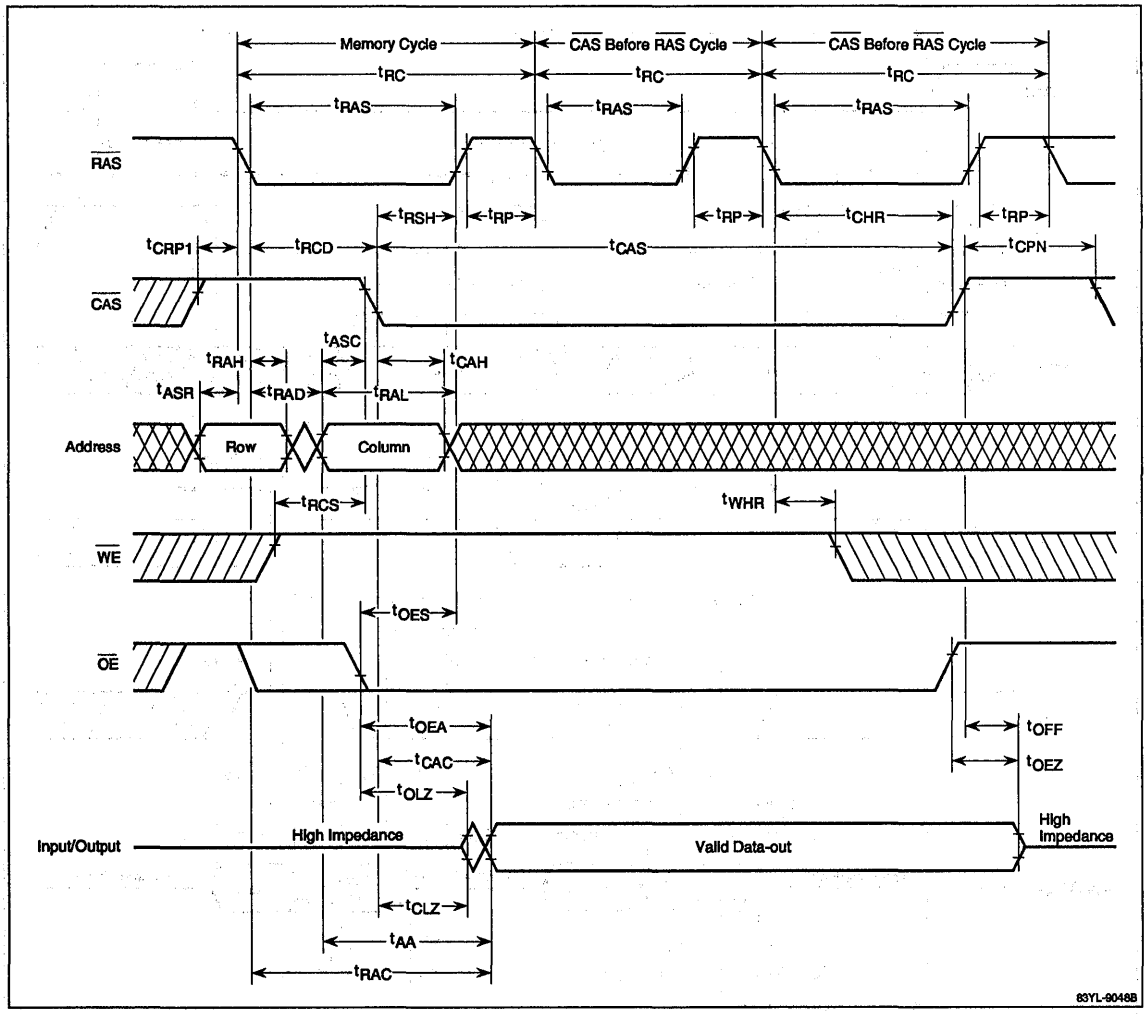
Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle



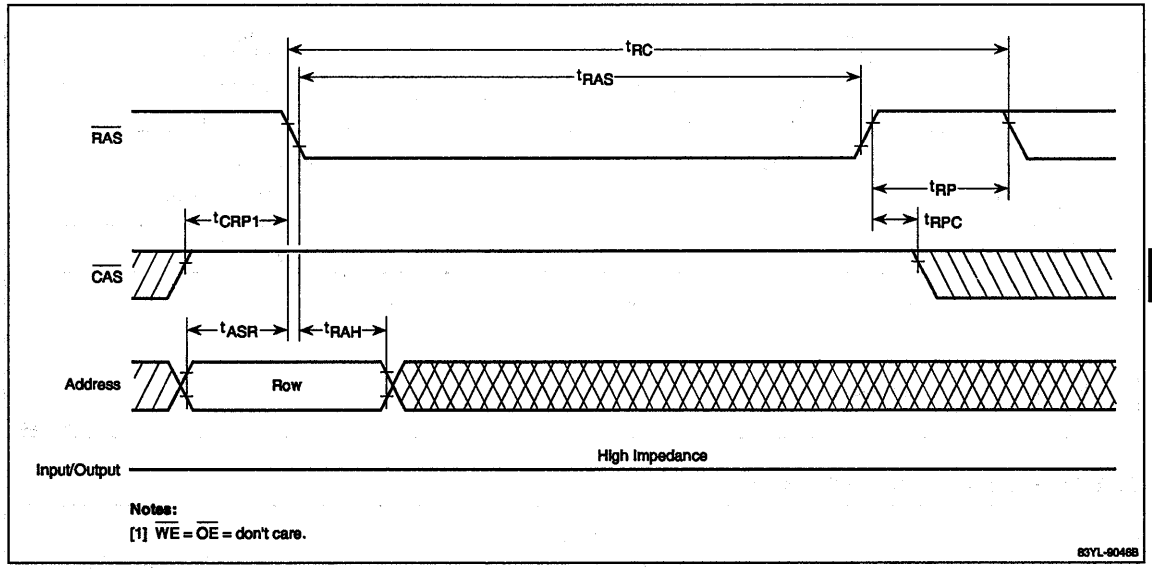
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

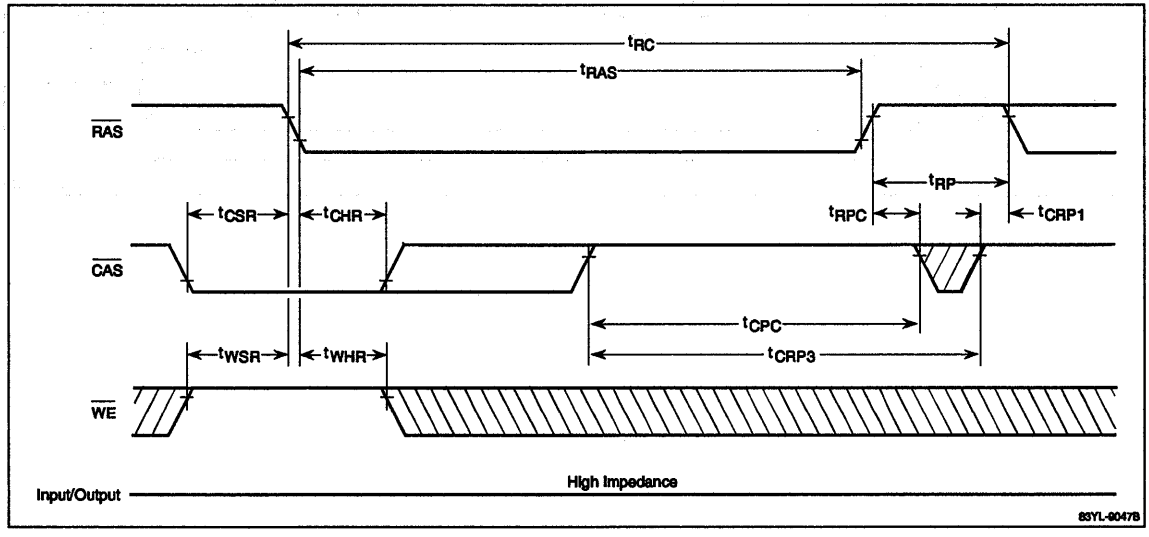
$\overline{RAS}$-Only Refresh Cycle



Notes:
[1] $\overline{WE}$ = $\overline{OE}$ = don't care.

83YL-9046B

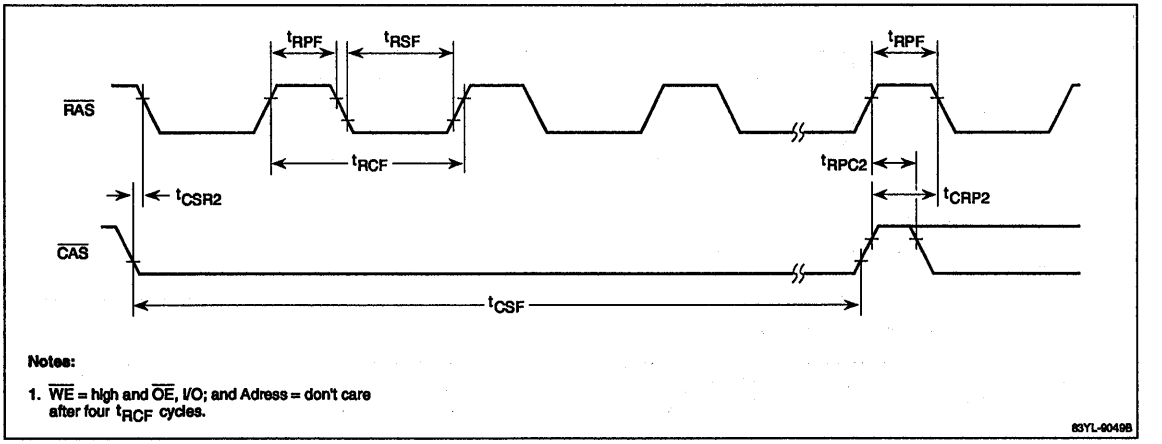
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



83YL-9047B

Timing Waveforms (cont)

Self-Refresh Cycle Followed by Read/WriteCycle

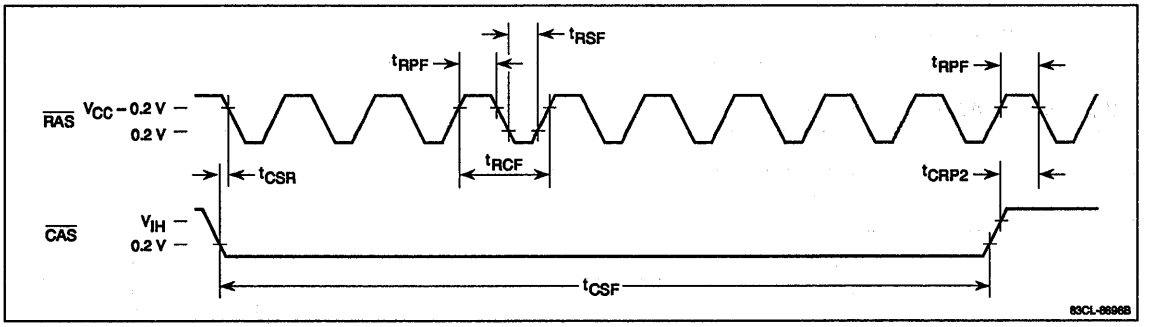


Notes:

1. $\overline{WE}$ = high and $\overline{OE}$, I/O; and Adress = don't care after four t_{RCF} cycles.

83YL-9049B

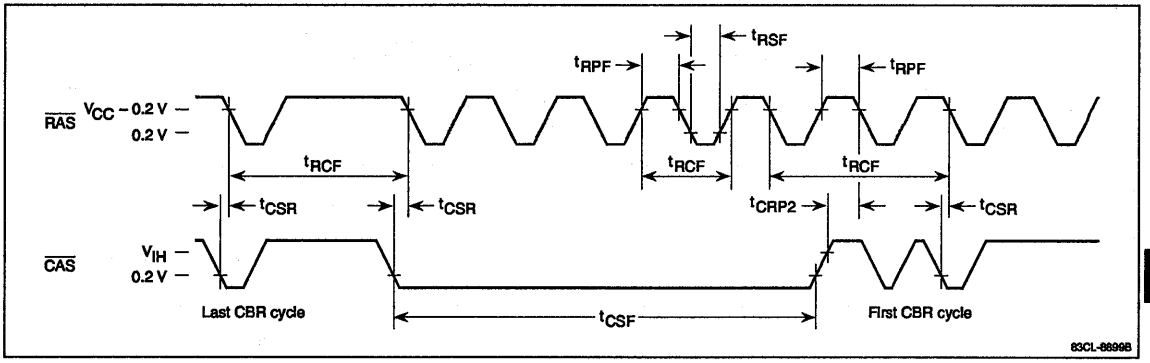
Self-Refresh Cycle with $\overline{RAS}$ Cycling



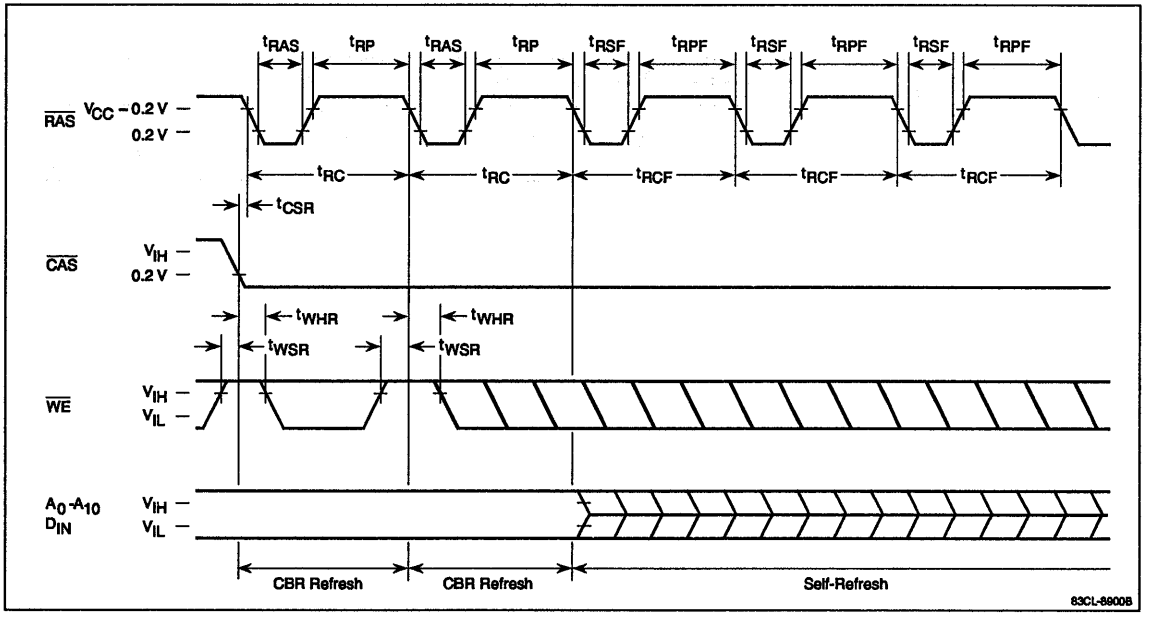
83CL-8696B

Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Followed by Self-Refresh Cycle

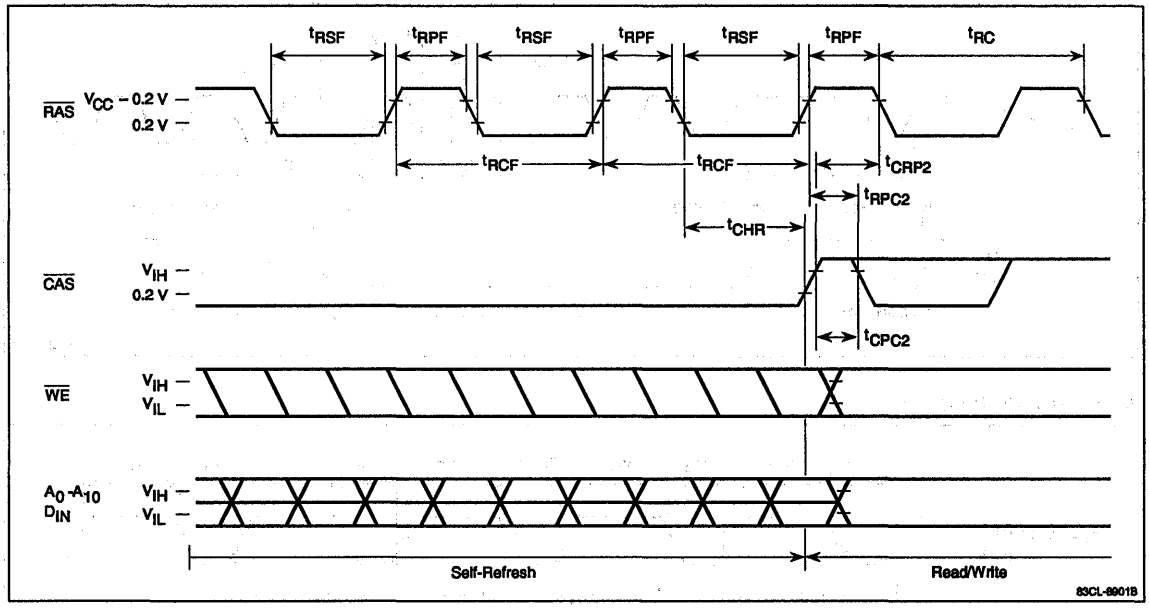


Self-Refresh Set Cycle



Timing Waveforms (cont)

Self-Refresh Set Cycle



NEC
NEC Electronics Inc.

μPD481440
262,144 x 16-Bit Graphics Memory

18m

Description

The μPD481440 is a fast-page memory with optional extended data output, organized as 262,144 words by 16 bits and designed to operate from a single +5-volt power supply. This graphics memory also incorporates powerful functions useful in video sytems, including write-per-bit, flash write, and block write. Advanced polycide technology using stacked capacitors minimizes silicon area and provides high storage cell capacity, high performance, and high reliability. A single-transistor dynamic storage cell and CMOS circuitry throughout ensure minimum power dissipation, while an on-chip circuit internally generates the negative-voltage substrate bias—automatically and transparently.

The three-state I/O pins are controlled by $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$. After a valid read, data is latched on the rising edge of $\overline{CAS}$ and remains valid until the next falling edge of $\overline{CAS}$. Data out will transition to the high-impedance state when both $\overline{RAS}$ and $\overline{CAS}$ or $\overline{OE}$ are inactive.

Word writing (I/O_1 - I/O_{16}), upper byte writing (I/O_9 - I/O_{16}), and lower byte writing (I/O_1 - I/O_8) are all possible using $\overline{UWE}$ and $\overline{LWE}$. If either $\overline{UWE}$ or $\overline{LWE}$ goes low during an early write cycle, all data outputs remain in high impedance. $\overline{UWE}$ or $\overline{LWE}$ going low causes a byte write cycle, while bringing both $\overline{UWE}$ and $\overline{LWE}$ low at the same time will result in a word write cycle. $\overline{UWE}$ and $\overline{LWE}$ cannot be staggered within the same write cycle.

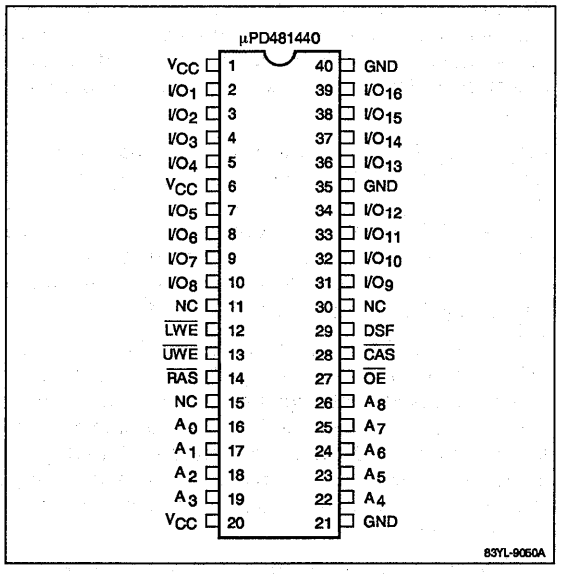
Refreshing may be accomplished by a $\overline{CAS}$ before $\overline{RAS}$ cycle that internally generates the refresh address. Refreshing may also be accomplished by $\overline{RAS}$-only refresh cycles or by normal read or write cycles on the 512 address combinations of A_0 - A_8 during an 8-ms refresh period.

Features

- 262,144 by 16-bit organization
- Single +5-volt power supply
- Fast-page option with extended data output
- Byte write control with $\overline{UWE}$ and $\overline{LWE}$
- Persistent and nonpersistent write-per-bit option, which provides I/O masking for 16 I/O's
- Block write option with write-per-bit control and column mask function
- Flash write option with byte masking control
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refreshing
- TTL-compatible inputs and outputs
- Low input capacitance
- 512 refresh cycles every 8 ms
- 40-pin plastic SOJ package

Pin Configurations

40-Pin Plastic SOJ



Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}$	Column address strobe
DSF	Special function pin
I/O_1 - I/O_{16}	Data inputs and outputs
$\overline{LWE}$, $\overline{UWE}$	Byte write enables
$\overline{OE}$	Output enable
$\overline{RAS}$	Row address strobe
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Ordering Information

Part Number	$\overline{RAS}$ Access Time (max)	R/W Cycle Time (max)	Fast-Page Cycle (max)	Package
μPD481440LE-70	70 ns	130 ns	45 ns	40-pin plastic SOJ
LE-80	80 ns	150 ns	50 ns	

Pin Functions

A_0 - A_8 (Address Inputs). These pins are multiplexed as row and column address inputs. Each of 16 data bits in the random access port corresponds to 262,144 storage cells, which means that 9-bit row addresses and 9-bit column addresses are required to decode one cell location. Row addresses are first used to select one of the 512 possible rows for a read, write, or refresh cycle.

I/O_1 - I/O_{16} (Common Data Inputs and Outputs). Each of the 16 mask bits can be individually latched at the falling edge of $\overline{RAS}$ in any write cycle and then updated at the next falling edge of $\overline{RAS}$. In a read cycle, these pins serve as outputs for the selected storage cells. In a write cycle, data input on these pins is latched by the falling edge of $\overline{CAS}$, $\overline{LWE}$, or $\overline{UWE}$.

$\overline{RAS}$ (Row Address Strobe). This pin is functionally equivalent to a chip enable signal in that whenever it is activated, the 8192 storage cells of a selected row are sensed simultaneously and the sense amplifiers restore all data. The 9 row address bits are latched by this signal and must be stable on or before its falling edge. $\overline{CAS}$, $\overline{LWE}$/ $\overline{UWE}$, and DSF are simultaneously latched to determine device operation.

$\overline{CAS}$ (Column Address Strobe). This pin serves as a chip selection signal to activate the column decoder and the input/output buffers. The 9 column address bits are latched at the falling edge of $\overline{CAS}$.

DSF (Special Function Control). At the leading edge of $\overline{RAS}$ and $\overline{CAS}$, the high or low level of DSF is latched to initiate one of the operations shown in table 1.

$\overline{LWE}$/$\overline{UWE}$ (Write-Per-Bit or Masked Write Control). At the falling edge of $\overline{RAS}$, the $\overline{LWE}$/$\overline{UWE}$ and DSF inputs must be low and $\overline{CAS}$ high to enable the write-per-bit option.

Either $\overline{LWE}$ or $\overline{UWE}$ must be low to initiate the lower or upper byte mask function. If both are low, then a word masking operation is performed.

$\overline{OE}$ (Output Enable). At the $\overline{RAS}$ falling edge, $\overline{CAS}$ and $\overline{LWE}$/$\overline{UWE}$ high and $\overline{OE}$ low initiate a data transfer. $\overline{OE}$ high initiates conventional read or write cycles and ontrols the output buffer in the random access port.

Addressing

The storage array is arranged in a 512-row by 512-column by 16 I/O matrix whereby each of 16 data bits in the random access port corresponds to 262,144 storage cells, and 18 address bits are required to decode one cell location. Nine row address bits are set up on pins A_0 - A_8 and latched onto the chip by $\overline{RAS}$. Nine column address bits then are set up on pins A_0 - A_8 and latched onto the chip by $\overline{CAS}$.

All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. Whenever $\overline{RAS}$ is activated, 8192 cells on the selected row are sensed simultaneously, and the sense amplifiers automatically restore the data. $\overline{CAS}$ serves as a chip selection signal to activate the column decoder and the input and output buffers.

Random Access Port

An operation in the random access port begins with a negative transition of $\overline{RAS}$. Both $\overline{RAS}$ and $\overline{CAS}$ have minimum pulse widths, as specified in the timing table, which must be maintained for proper device operation and data integrity. Once begun, a cycle must meet all specifications, including minimum cycle time. To reduce the number of pins, the following are multiplexed: $\overline{LWE}$, $\overline{UWE}$, I/O_n (n = 1 through 16).

Read Cycle. A read cycle is executed by activating $\overline{RAS}$, $\overline{CAS}$, and $\overline{OE}$ and by maintaining $\overline{LWE}$/$\overline{UWE}$ high (inactive) while $\overline{CAS}$ is active. The I/O_n pin remains in high impedance until valid data appears at the output at access time. Device access time t_{ACC} will be the longest of the following four calculated intervals:

- t_{RAC}
- $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD}) + t_{CAC}
- $\overline{RAS}$ to column address delay (t_{RAD}) + t_{AA}
- $\overline{RAS}$ to $\overline{OE}$ delay + t_{OEA}

Access times from $\overline{RAS}$ (t_{RAC}), from $\overline{CAS}$ (t_{CAC}), from the column addresses (t_{AA}), and from $\overline{OE}$ (t_{OEA}) are device parameters. The $\overline{RAS}$-to-$\overline{CAS}$, $\overline{RAS}$-to-column address, and $\overline{RAS}$-to-$\overline{OE}$ delays are system-dependent timing parameters. Output becomes valid after the access time has elapsed and it remains valid while both $\overline{CAS}$ and $\overline{OE}$ are low. Either $\overline{CAS}$ or $\overline{OE}$ high returns the output pins to high impedance. See explanation of "Extended Data Output."

Write Cycle. A write cycle is executed by bringing $\overline{LWE}/\overline{UWE}$ low during the $\overline{RAS}/\overline{CAS}$ cycle. The falling edge of $\overline{CAS}$ or $\overline{LWE}/\overline{UWE}$ strobes the data on I/O_n into the on-chip data latch. To make use of the write-per-bit option, $\overline{LWE}/\overline{UWE}$ must be low as $\overline{RAS}$ falls. In this case, write data bits can be specified by keeping I/O_n high, with setup and hold times referenced to the negative transition of $\overline{RAS}$.

Write-per-Bit-Cycle. A write-per-bit-cycle uses an I/O masking function to allow the system designer the flexibility of writing or not writing any combinations of I/O_1 - I/O_{16}. Two types of masking are possible: (1) new mask or the non-persistent mask that requires the user to provide the mask data each cycle and (2) old mask or the persistent mask. With the persistent mask option, an LMR or load mask register cycle is performed and the mask data is used during write, block write, and flash write cycles.

Early Write Cycle. An early write cycle is executed by bringing $\overline{LWE}/\overline{UWE}$ low before $\overline{CAS}$ falls. Data is strobed by $\overline{CAS}$, with setup and hold times referenced to this signal, and the output remains in high impedance for the entire cycle.

Read-Write/Read-Modify-Write Cycle. This cycle is executed by bringing $\overline{LWE}/\overline{UWE}$ low with the $\overline{RAS}$ and $\overline{CAS}$ signals low. I/O_n shows read data at access time. Afterward, in preparation for the upcoming write cycle, I/O_n returns to high impedance when $\overline{OE}$ goes high. The data to be written is strobed by $\overline{LWE}/\overline{UWE}$, with setup and hold times referenced to this signal.

Late Write Cycle. This cycle shows the timing flexibility of $\overline{OE}$, which can be activated just after $\overline{LWE}/\overline{UWE}$ falls, even when $\overline{LWE}/\overline{UWE}$ is brought low after $\overline{CAS}$.

Refresh Cycle. A cycle at each of the 512 row addresses (A_0 - A_8) will refresh all storage cells. Any cycle executed in the random access port (i.e., read, write, refresh, color register set, flash write, or block write) refreshes the 8192 bits selected by the $\overline{RAS}$ addresses or by the on-chip address counter.

$\overline{RAS}$-Only Refresh Cycle. A cycle having only $\overline{RAS}$ active refreshes all cells in one row of the storage array. A high $\overline{CAS}$ is maintained while $\overline{RAS}$ is active to keep I/O_n in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RAS}$-only refresh cycles are executed.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (CBRN). This cycle executes internal refreshing using the on-chip control circuitry. Whenever $\overline{CAS}$ is low as $\overline{RAS}$ falls, this circuitry automatically refreshes the row addresses specified by the internal counter. In this cycle, the circuit operation based on $\overline{CAS}$ is maintained in a reset state. When internal refreshing is complete, the address counter automatically increments in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ cycle. This CBR cycle has no effect on the mask mode.

$\overline{CAS}$ Before $\overline{RAS}$ Cycle (CBR). CBR has the same function as CBRN except the write-per-bit mask mode is changed to new mask mode.

Hidden Refresh Cycle. This cycle is executed after a read cycle without disturbing the read data output. Once valid, the data output is controlled by $\overline{CAS}$ and $\overline{OE}$. After the read cycle, $\overline{CAS}$ is held low while $\overline{RAS}$ goes high for precharge. A $\overline{RAS}$-only cycle is then executed (except that $\overline{CAS}$ is held at a low level instead of a high level) and the data output remains valid. Since hidden refreshing is the same as $\overline{CAS}$ before $\overline{RAS}$ refreshing, the data output remains valid during either operation.

Glossary of Special Functions

Table 1 is a truth table for implementing the functions described below.

Load Mask Register Cycle (LMR). In this cycle, data on I/O_n is written to a 16-bit write mask register, where it is retained and used by subsequent masked write and masked block write cycles.

Masked Write Cycle With New Mask (RWM new mask). When the write-per-bit function is enabled as shown below, mask data on the I/O_n pins is latched by $\overline{RAS}$ and loaded directly into the write mask register. A masked write cycle is then executed using $\overline{CAS}$ or $\overline{LWE}/\overline{UWE}$ to strobe the I/O_n data into the on-chip data latch.

Mask Register Data	Action
1	Write
0	Do not write

Masked Write Cycle With Old Mask (RWM old mask). This write-per-bit cycle, commonly referred to as a persistent mask write cycle, uses the mask data previously set by the last load mask register cycle.

Load Color Register Cycle (LCR). This cycle is executed in the same fashion as a conventional read or write cycle, with a read or write cycle available to the color register under the control of $\overline{LWE}/\overline{UWE}$. In read operation, color register data is read on the common I/O_n pins. In write operation, common I/O_n data can be written into the color register. $\overline{RAS}$-only refreshing is internally performed on the row selected by A_0 - A_8. This setup cycle precedes the first flash write or block write cycle supplying the 16 write data bits.

Block Write Cycle (BW no mask). In a block write cycle, A_1 and A_0 are ignored. I/O_1 - I/O_4 are used to select one or a combination of four column addresses for writing in an early lower-byte write, late lower-byte write, page early lower-byte write or page late lower-byte write cycle. I/O_9 - I/O_{12} are used for column selection on the upper-byte write cycles.

Block write data is previously stored in the color register using a set color register cycle. Column select data is latched by the I/O_n pins at the falling edge of $\overline{CAS}$ or $\overline{LWE}/\overline{UWE}$. Block write cycles are useful for clearing windows and for accelerating polygon fill operations.

Table 1. μPD481440 Function Truth Table

	$\overline{RAS}$ (Notes 1, 2)				$\overline{CAS}$	
Mnemonic Code	**$\overline{CAS}$**	**$\overline{UWE}$**	**$\overline{LWE}$**	**DSF**	**DSF**	**Available Function**
RW	H	H	H	L	L	Read/write cycle
BW	H	H	H	L	H	Read/block write cycle
FW	H	L	L	H	X	Flash write cycle
FW	H	L	H	H	X	Flash write cycle (upper byte)
FW	H	H	L	H	X	Flash write cycle (lower byte)
LCR	H	H	H	H	H	Color register set cycle
LMR	H	H	H	H	L	Load old mask register cycle
RWM	H	L	L	L	L	Read/masked write cycle
RWM	H	L	H	L	L	Read/masked write cycle (upper byte)
RWM	H	H	L	L	L	Read/masked write cycle (lower byte)
BWM	H	L	L	L	H	Read/masked block write cycle
BWM	H	L	H	L	H	Read/masked block write cycle (upper byte)
BWM	H	H	L	L	H	Read/masked block write cycle (lower byte)
CBR	L	H	H	L	X	CBR refresh with reset to new mask
CBRN	L	H	H	H	X	CBR refresh with no reset

Notes:

(1) An operation is started by the falling edge of $\overline{RAS}$. The level of $\overline{CAS}$, $\overline{UWE}/\overline{LWE}$, and DSF at this negative transition defines the memory operation according to this table.

(2) The $\overline{UWE}$ and $\overline{LWE}$ pins have the OR function. That is if either upper or lower write enable goes low, then depending on $\overline{CAS}$ and DSF, a byte-controlled FW, RW, or BW will be performed. The inactive write enable has no other function.

(3) X = Don't care.

Block Write Cycle (BWM new mask). This cycle allows for I/O_1 - I/O_{16} masking during a block write cycle. The masking function is identical to a standard masked write cycle with new mask. The column mask data on the I/O_n pins is latched by $\overline{CAS}$. See table 2.

Block Write Cycle (BWM old mask). This cycle uses the masked data previously set by the last LMR cycle to write four consecutive columns. See table 2 for column masking description.

Table 2. Block Write Addresses

Byte	Column Select		Column Address A_1	Column Address A_0	Write
Lower (I/O_8 - I/O_5 are Don't Care)	I/O_4	1	1	1	Yes
		0	1	1	No
	I/O_3	1	1	0	Yes
		0	1	0	No
	I/O_2	1	0	1	Yes
		0	0	1	No
	I/O_1	1	0	0	Yes
		0	0	0	No
Upper (I/O_{16} - I/O_{13} are Don't Care)	I/O_{12}	1	1	1	Yes
		0	1	1	No
	I/O_{11}	1	1	0	Yes
		0	1	0	No
	I/O_{10}	1	0	1	Yes
		0	0	1	No
	I/O_9	1	0	0	Yes
		0	0	0	No

Flash Write Cycle (FW.) A flash write cycle can clear or set each of the sixteen 512-bit data sets on the selected one of 512 possible rows according to data stored in the previously set color register. Only the byte masking function is provided. This cycle is useful in graphics processing applications when the screen should be cleared or set to some uniform value as quickly as possible.

Fast-Page Mode With Extended Data Output. In operation, this mode is the same as standard fast-page mode. A faster data rate is possible by keeping the same row address while successive column addresses are strobed onto the chip. Maintaining $\overline{RAS}$ low while CAS cycles are executed causes data to be transferred at a faster rate because row addresses are maintained internally and do not have to be reapplied. During fast-page mode, read, write, and read-modify-write cycles may be executed. Additionally, the write-per-bit control specified in the entry write cycle is maintained throughout the succeeding fast-page write cycle.

Extended Data Output

The introduction of the extended data output feature causes the output data to remain valid even after $\overline{CAS}$ goes high. This is made possible by the addition of a transparent latch to the data amplifier circuit. Extended data output eliminates the t_{OFF} parameter. The resulting longer data valid time allows for the speedup of the fast-page cycle time. Fast-page mode applications that try to run at minimum cycle times find that timing skews and propagation delays make the data valid time so narrow that reliable sampling is impossible. Extended data output is intended to solve this problem and permit faster page-mode cycle times.

In this operation, data pins I/O_1 - I/O_{16} remain in the low-impedance state and the valid data appears after the device access time. Device access time, t_{PAC} (page-mode access time), is the longest of these intervals: t_{AA}, t_{ACP}, t_{CAC}.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	Addresses
	C_{I2}	7	pF	$\overline{RAS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{OE}$, DSF
Input/output capacitance	C_O	7	pF	I/O_1 - I/O_{16}

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Standby current	I_{CC2}			2.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} (min); I_O = 0 mA
				1.0	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} – 0.2 V; I_O = 0 mA
Input leakage current	$I_{I(L)}$	–10		10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	–10		10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = –2.5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		-70		-80			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		170		155	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Notes 3, 4)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		170		155	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≥ V_{IH} min; t_{RC} = t_{RC} min (Notes 3, 4)
Operating current, fast-page cycle, average	I_{CC4}		170		155	mA	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Notes 3, 4)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		170		155	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ ≤ V_{IL} max; t_{RC} = t_{RC} min (Notes 3, 4)
Operating current (register set mode)	I_{CC6}		170		155	ns	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Notes 3, 4)
Operating current (flash write mode)	I_{CC7}		170		155	ns	$\overline{RAS}$ cycling; t_{RC} = t_{RC} min (Notes 3, 4)
Operating current (block write mode)	I_{CC8}		185		170	ns	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Notes 3, 4)
Operating current (fast page block write mode)	I_{CC9}		170		155	ns	$\overline{RAS}$ ≤ V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min; (Notes 3, 4)
Access time from column address	t_{AA}		35		40	ns	(Notes 9, 15)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		40		45	ns	(Note 9)
Column address setup time	t_{ASC}	0		0		ns	
Row address setup time	t_{ASR}	0		0		ns	
Column address to $\overline{UWE}$ delay time	t_{AWD}	55		65		ns	(Note 13)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20	ns	(Notes 9, 14)
Column address hold time	t_{CAH}	15		15		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		15		ns	(Note 15)

AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0		0		ns	(Note 9)
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10		10		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		ns	
Fast-page $\overline{CAS}$ precharge to $\overline{UWE}$ delay time	t_{CPWD}	60		70		ns	(Note 13)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		ns	(Note 10)
$\overline{CAS}$ hold time	t_{CSH}	70		80		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		ns	(Note 15)
$\overline{CAS}$ to $\overline{UWE}$ delay	t_{CWD}	40		45		ns	(Note 13)
Write command referenced to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	
Data-in hold time	t_{DH}	15		15		ns	(Note 12)
Output hold time from $\overline{CAS}$	t_{DHC}	5		5		ns	
Data-in setup time	t_{DS}	0		0		ns	(Note 12)
DSF setup time from $\overline{CAS}$	t_{FCS}	0		0		ns	
DSF hold timefrom $\overline{CAS}$	t_{FCH}	12		15		ns	
DSF hold time from $\overline{RAS}$	t_{FRH}	10		12		ns	
DSF setup time from $\overline{RAS}$	t_{FRS}	0		0		ns	
Mask write hold time referenced to $\overline{CAS}$ precharge	t_{MCH}	0		0		ns	
Mask write setup time	t_{MCS}	0		0		ns	
Masked byte hold time referenced to $\overline{RAS}$	t_{MRH}	0		0		ns	
Access time from $\overline{OE}$	t_{OEA}		20		20	ns	(Notes 3, 4, 7, 8)
$\overline{OE}$ data delay time	t_{OED}	15		20		ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		ns	
$\overline{OE}$ to $\overline{RAS}$ inactive setup time	t_{OES}	0		0		ns	
Output turnoff delay from $\overline{OE}$	t_{OEZ}	0	15	0	20	ns	(Note 10)
Output disable time from $\overline{CAS}$ high	t_{OFC}	0	15	0	20	ns	(Note 17)
Output disable time from $\overline{RAS}$ high	t_{OFR}	0	15	0	20	ns	(Note 17)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		ns	
Fast-page read or write cycle time	t_{PC}	35		40		ns	
Fast-page read-modify-write cycle time	t_{PRWC}	95		105		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80	ns	(Notes 9, 14, 15)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	ns	(Note 15)
Row address hold time	t_{RAH}	10		10		ns	

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AC Characteristics (cont)

Parameter	Symbol	-70 Min	-70 Max	-80 Min	-80 Max	Unit	Test Conditions
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	35		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	70	125,000	80	125,000	ns	
Random read or write cycle time	t_{RC}	130		150		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	ns	(Note 14)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	(Note 11)
Read command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		8		8	ms	Addresses A_0 - A_8
$\overline{RAS}$ hold time referenced to $\overline{CAS}$ precharge	t_{RHCP}	40		45		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	5		5		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	
Access time from DSF	t_{RSA}		25		30	ns	(Note 9)
$\overline{RAS}$ hold time	t_{RSH}	20		20		ns	
Read-modify-write cycle time	t_{RWC}	175		200		ns	
$\overline{RAS}$ to $\overline{UWE}$ delay	t_{RWD}	90		105		ns	(Note 13)
Write command referenced to $\overline{RAS}$ lead time	t_{RWL}	20		25		ns	
Rise and fall transition time	t_T	3	50	3	50	ns	(Note 8)
Write-per-bit hold time	t_{WBH}	10		12		ns	
Write-per-bit setup time	t_{WBS}	0		0		ns	
Write command hold time	t_{WCH}	15		15		ns	
Write command setup time	t_{WCS}	0		0		ns	(Note 13)
Output disable time from $\overline{WE}$ low	t_{WEZ}	0	15	0	20	ns	(Note 17)
Write bit selection hold time	t_{WH}	10		12		ns	
Write command pulse width	t_{WP}	15		15		ns	(Note 16)
Write command pulse width	t_{WPZ}	15		15		ns	(Note 18)
Write bit selection set-up time	t_{WS}	0		0		ns	

AC Characteristics (cont)

Notes:

(1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

(2) All voltages are referenced to GND.

(3) I_{CC1}, I_{CC3}, I_{CC4}, , I_{CC5}, I_{CC6}, I_{CC7}, I_{CC8}, and I_{CC9} depend on cycle rate

(4) I_{CC1}, I_{CC4}, I_{CC6}, I_{CC8}, and I_{CC9} depend on output loading. Specified values are obtained with outputs open.

(5) Column Address can be changed once while $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$

(6) An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.

(7) Ac measurements assume $t_T = 5$ ns.

(8) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(9) Measured with a load equivalent to TTL load and 100 pF.

(10) t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.

(11) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

(12) These parameters are referenced to $\overline{CAS}$ leading edge in early wirte cyles and to $\overline{LWE}$/$\overline{UWE}$ leading edge in late write cycles and in read-modify-write cycles.

(13) t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data I/O pins will remain open-circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither set of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

(14) Operation within the t_{RCD} (max) limit insures t_{RAC} (max) can be met. Delay time t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.

(15) Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. Delay time t_{RAD} (max) is specified as a reference point only. If t_{RAD} is longer than the specified t_{RAD} (max) limits, then access time is controlled by t_{AA}.

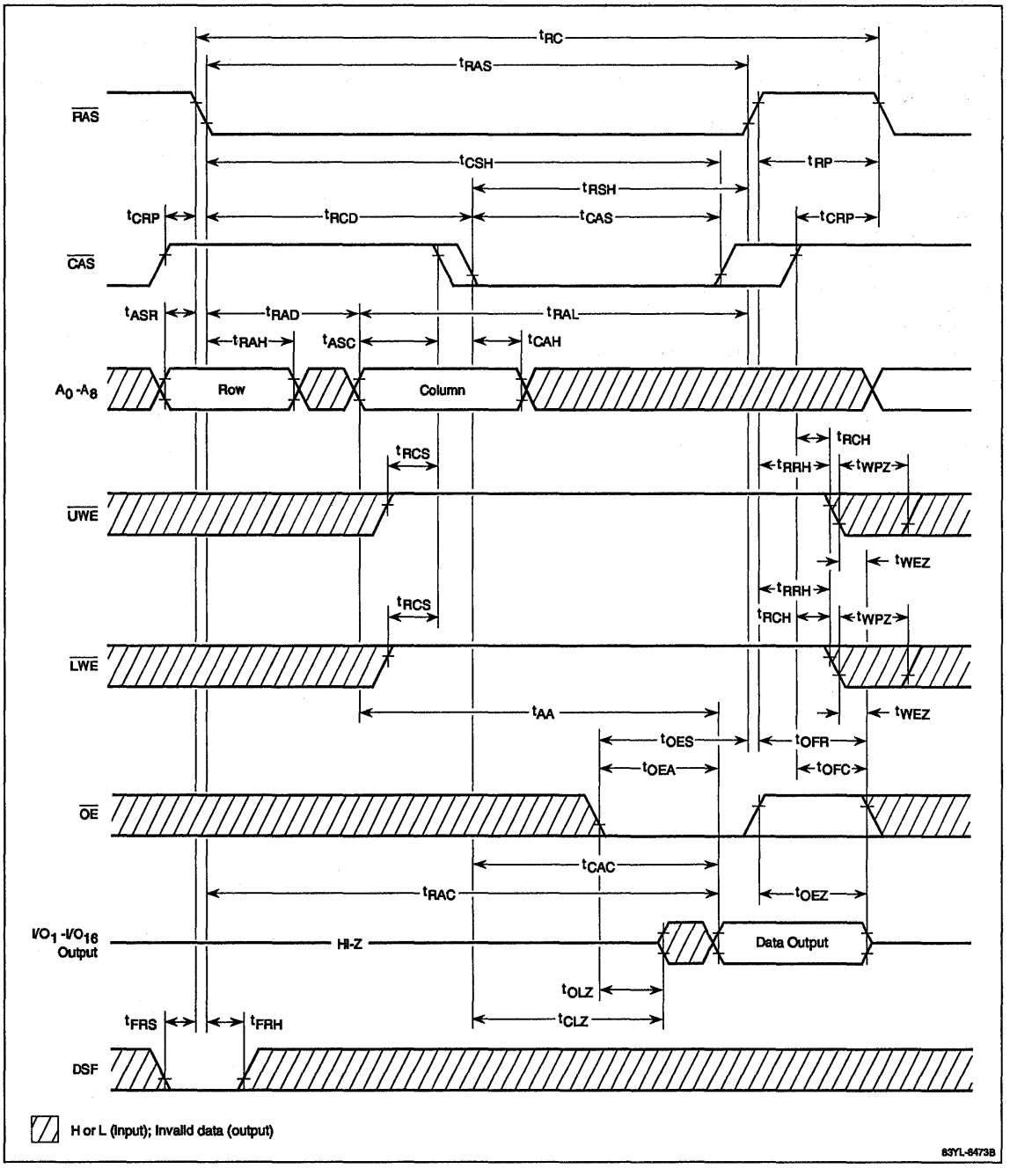
(16) t_{WP} is applicable for late write cycle or read-modify-write cycle. In early write cycle, t_{WCH} (min) should be satisfied.

(17) t_{WEZ}, t_{OFC}, and t_{OFR} define the time at which the outputs achieve the open circuit condition and output control dependence on $\overline{OE}$ becomes invalid. The effective time is "the earlier of t_{WEZ} and the later of t_{OFC} and t_{OFR}." In addition, to make t_{WEZ} effective, t_{WPZ} must be satisfied.

18m

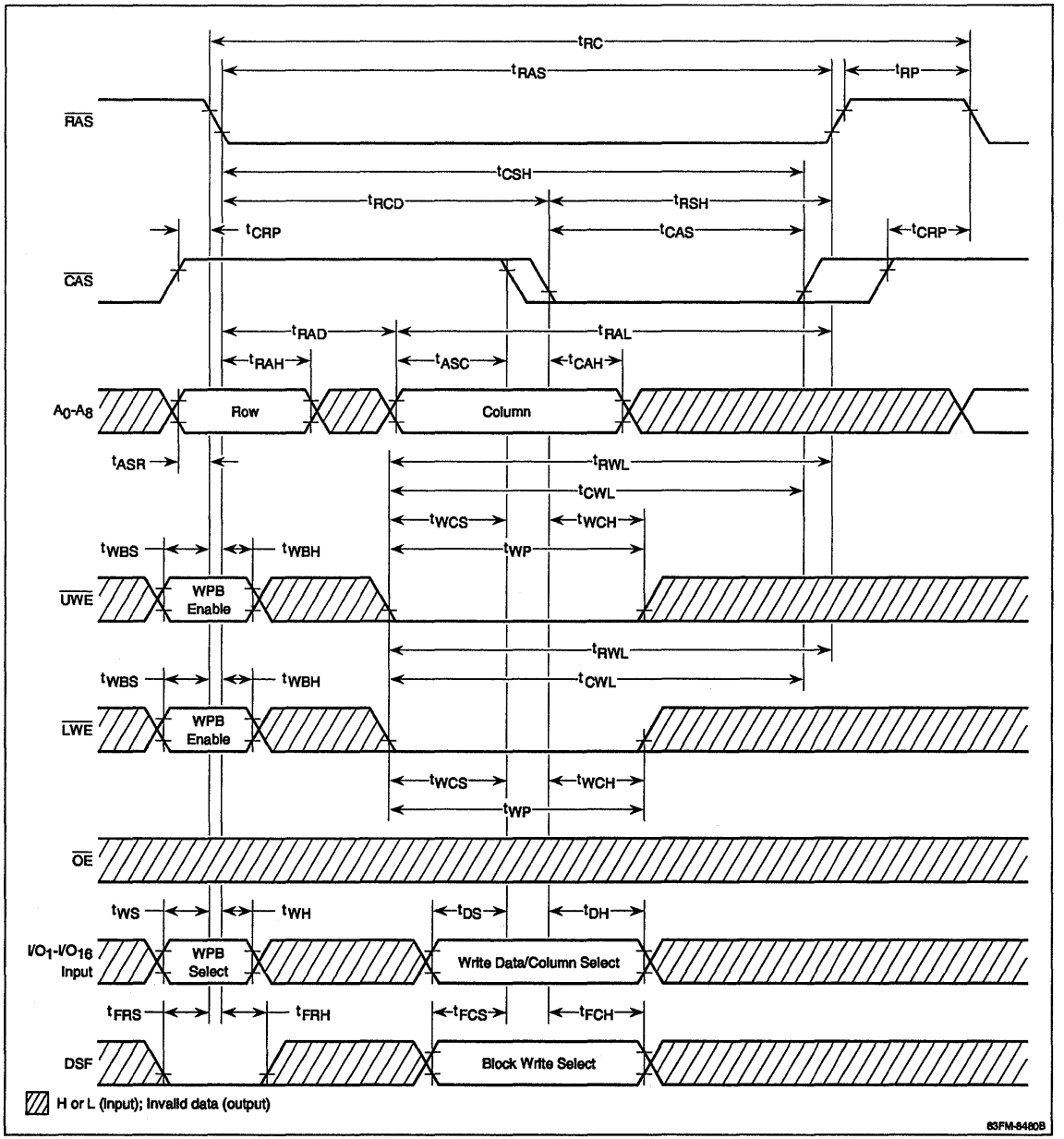
Timing Waveforms

Read Cycle (With exended output)



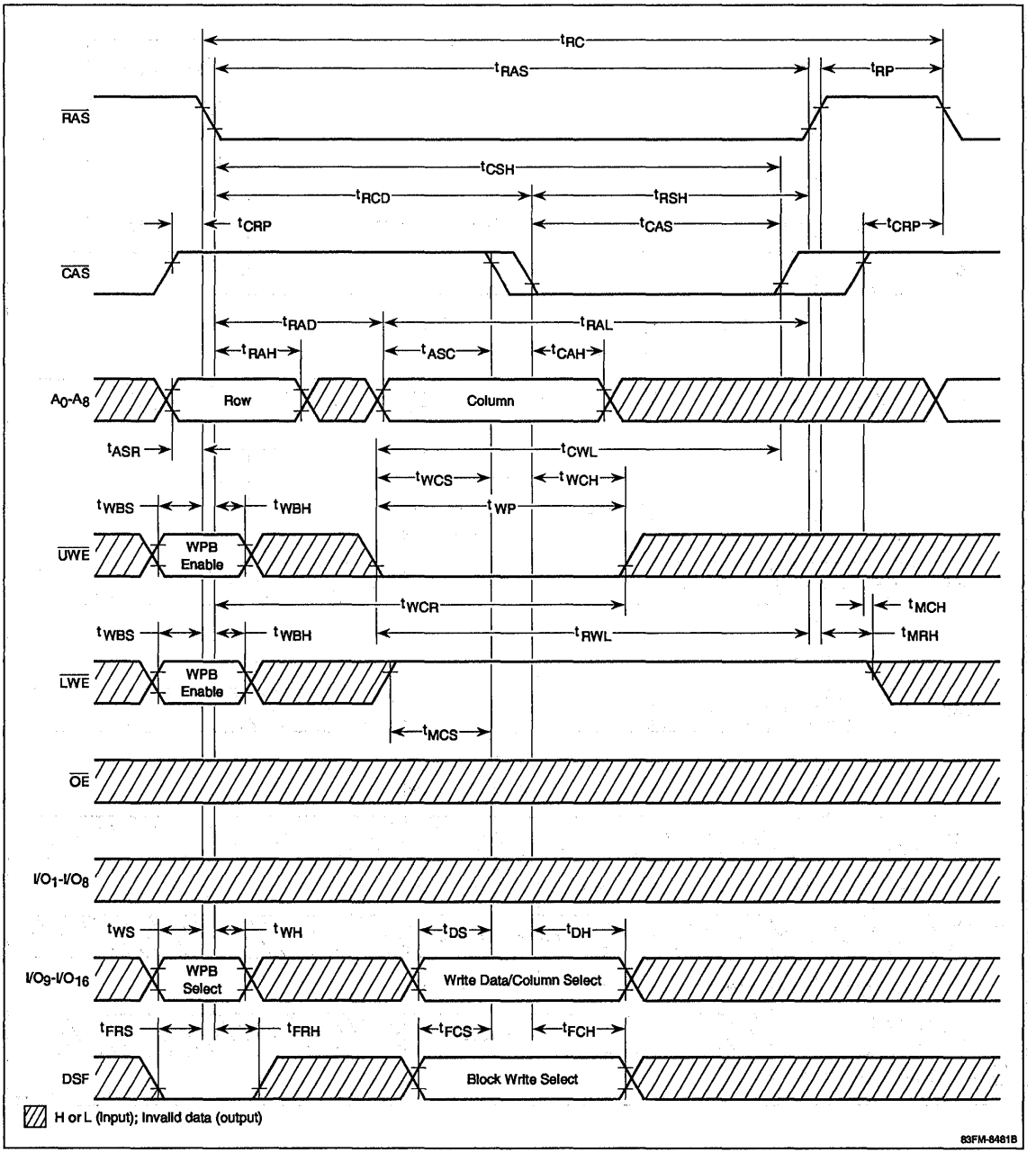
Timing Waveforms (cont)

Early-Write Cycle; Word and Word Block



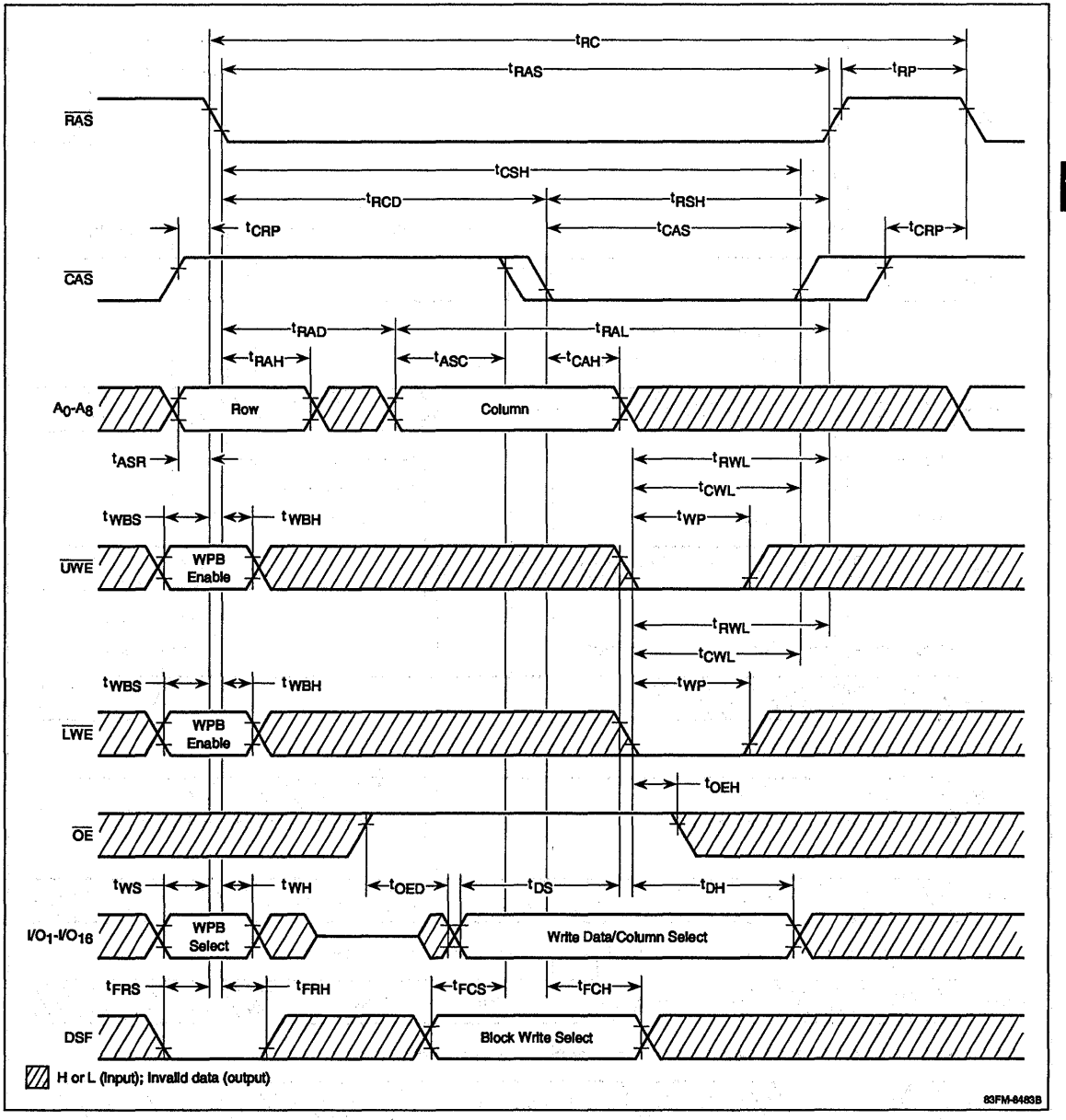
Timing Waveforms (cont)

Early-Write Cycle; Upper-Byte and Upper-Byte Block



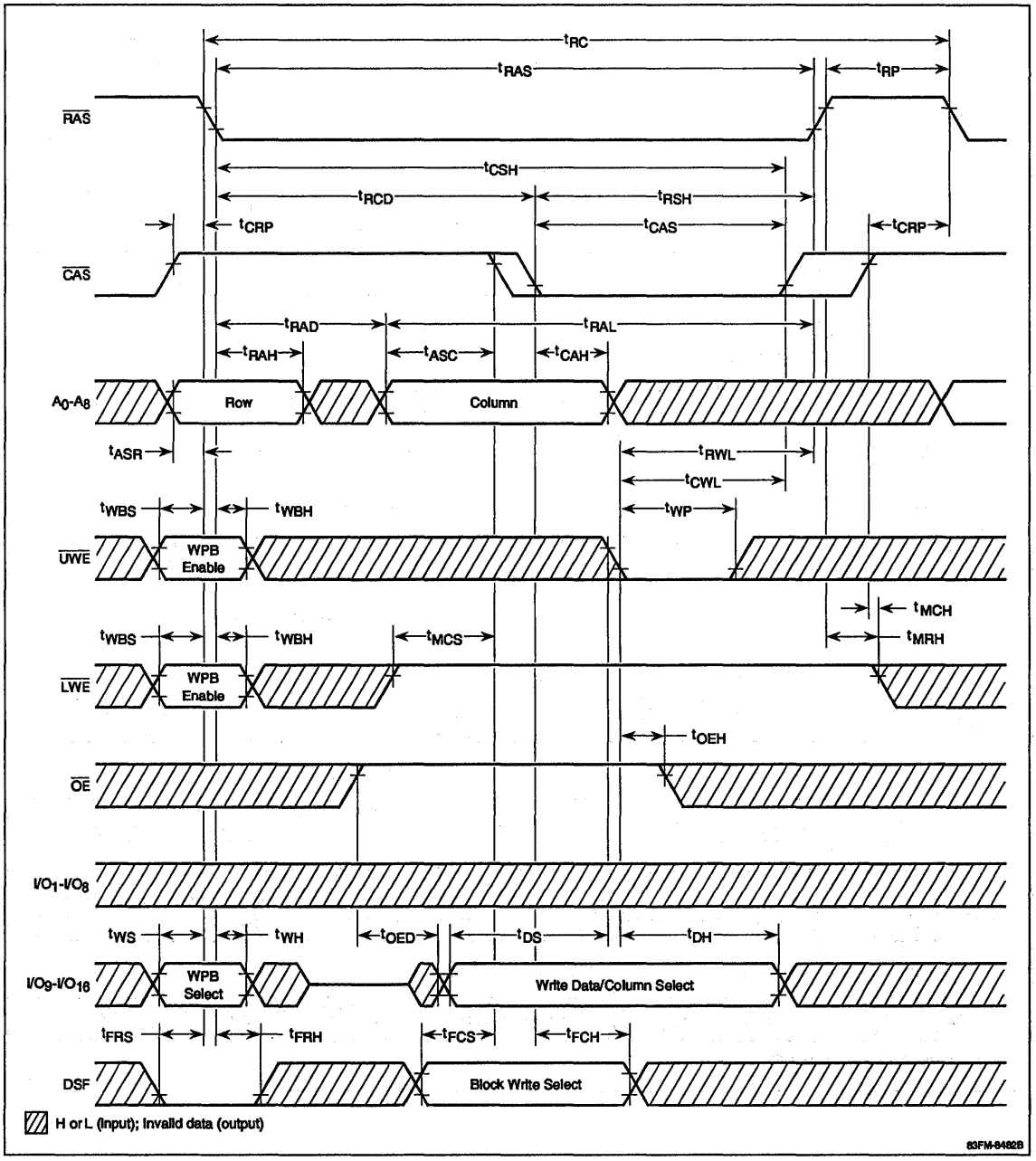
Timing Waveforms (cont)

Late-Write Cycle; Word and Word Block



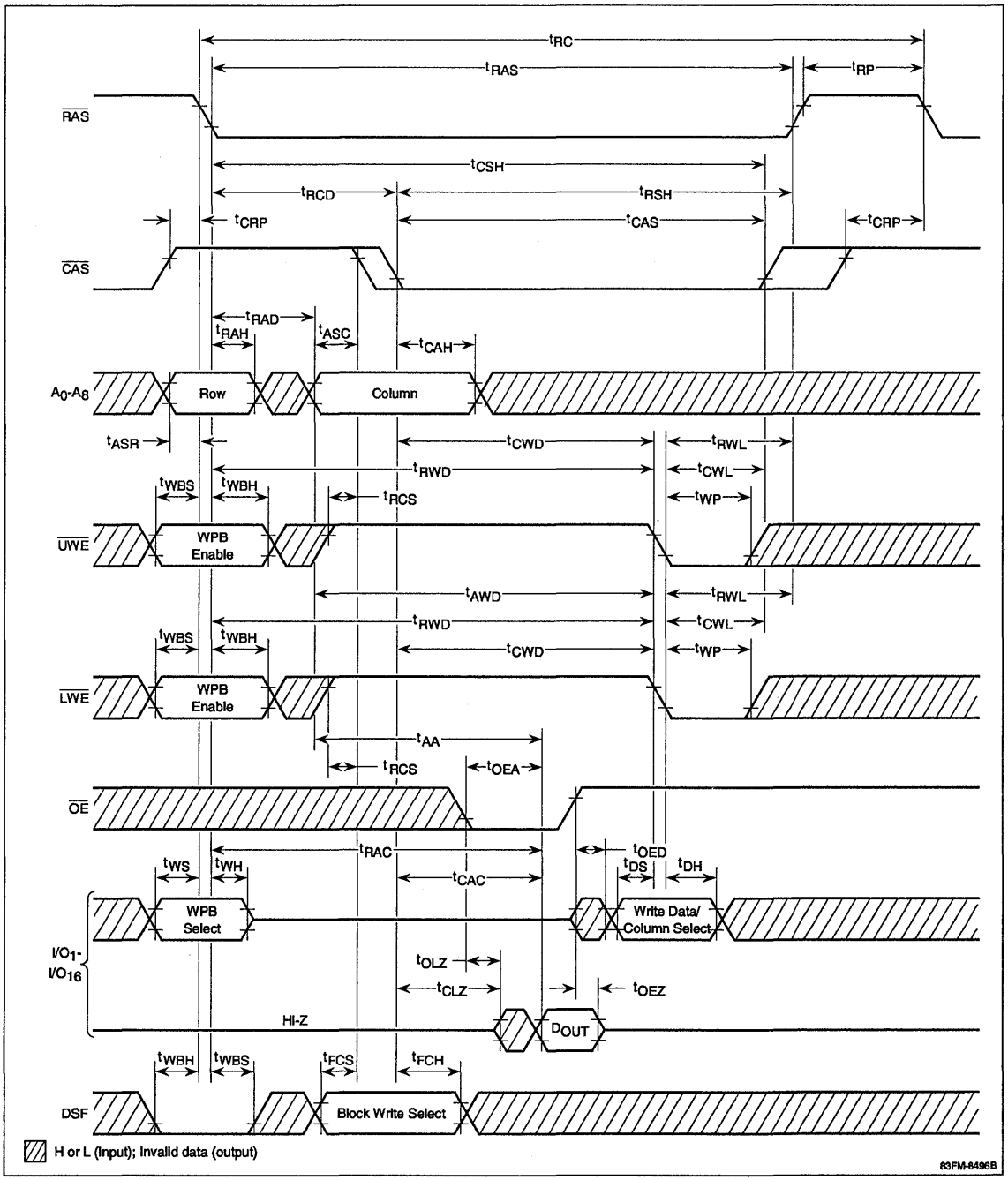
Timing Waveforms (cont)

Late-Write Cycle; Upper-Byte and Upper-Byte Block

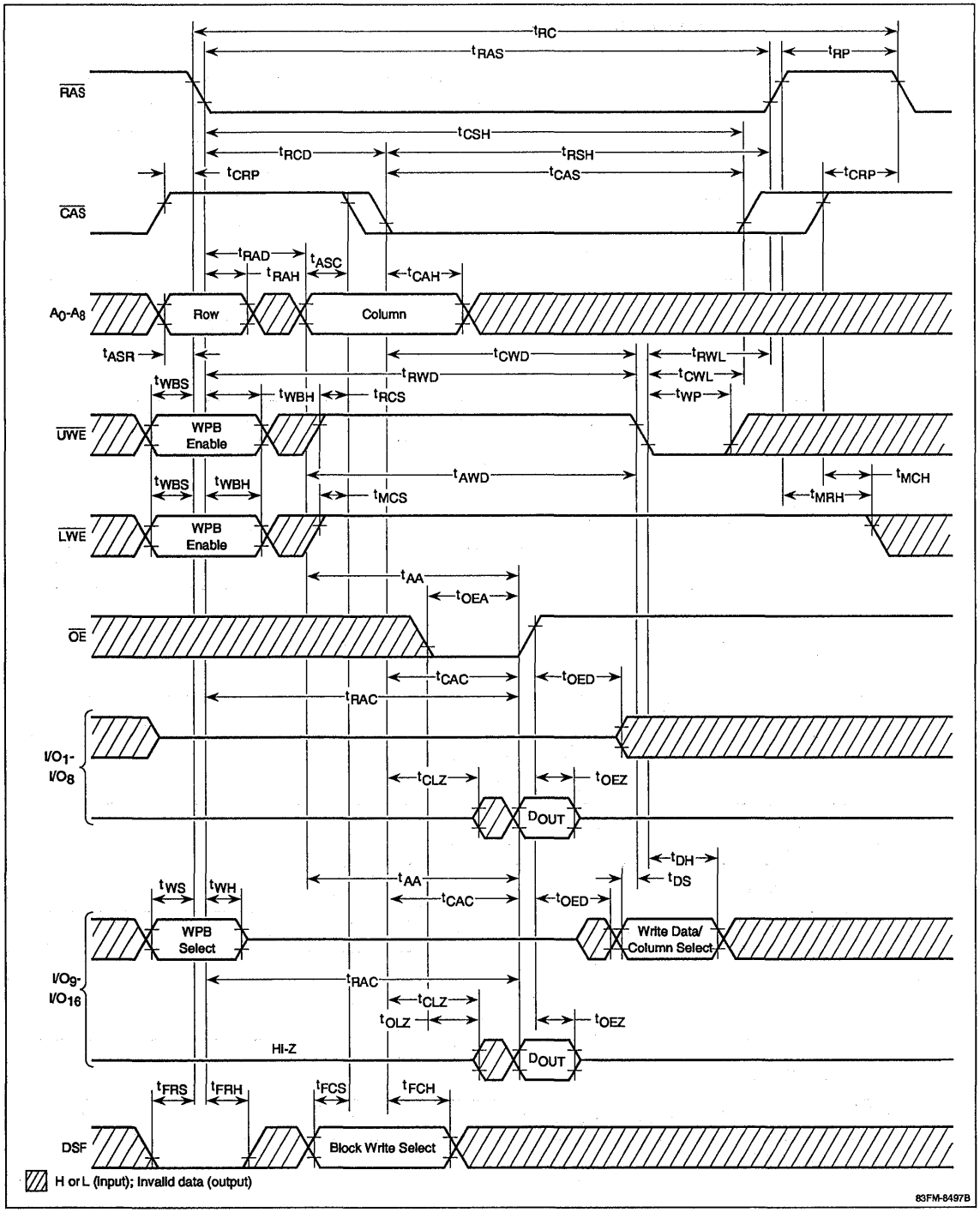


Timing Waveforms (cont)

Read-Modify-Write Cycle; Word and Word Block

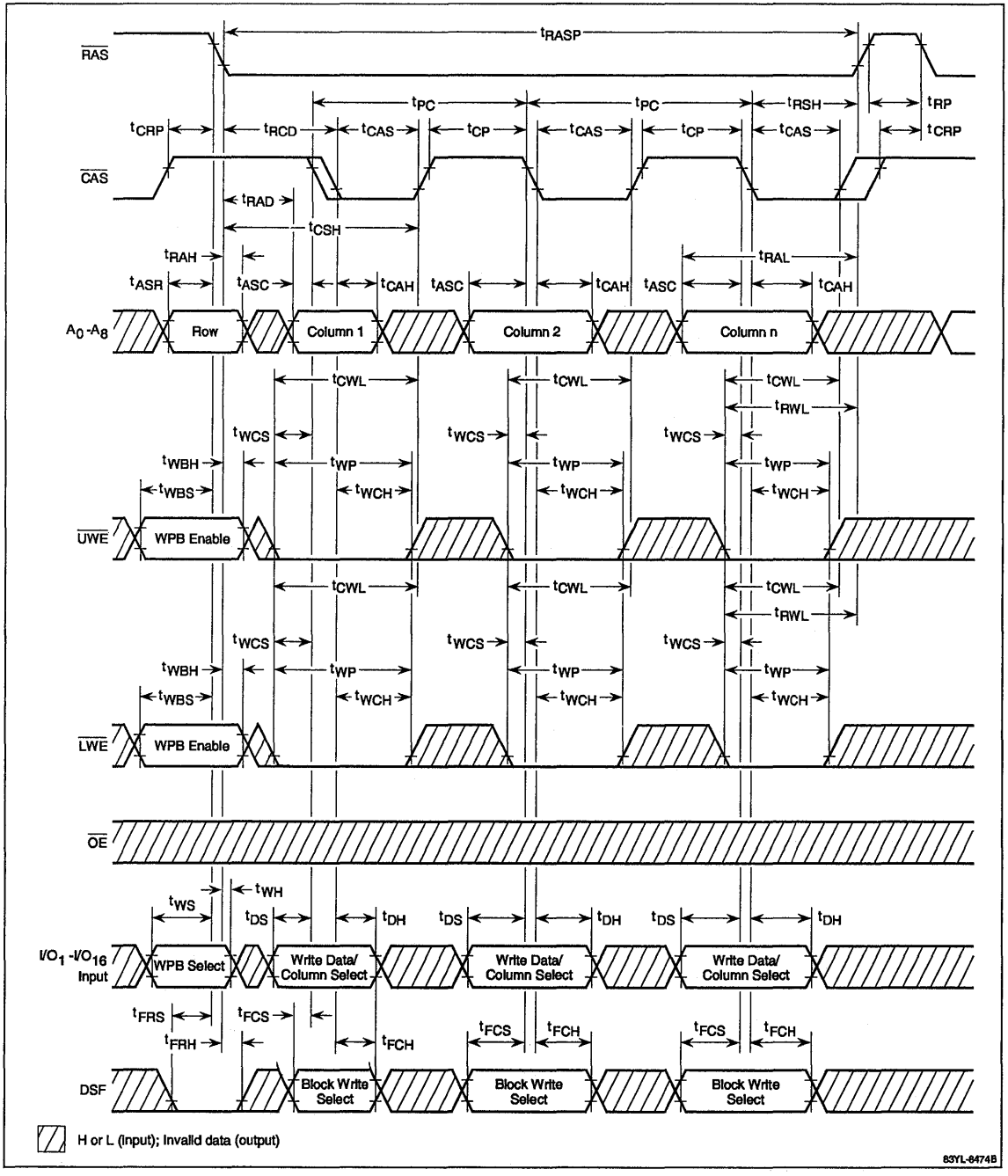


Read-Modify-Write Cycle; Upper-Byte and Upper-Byte Block



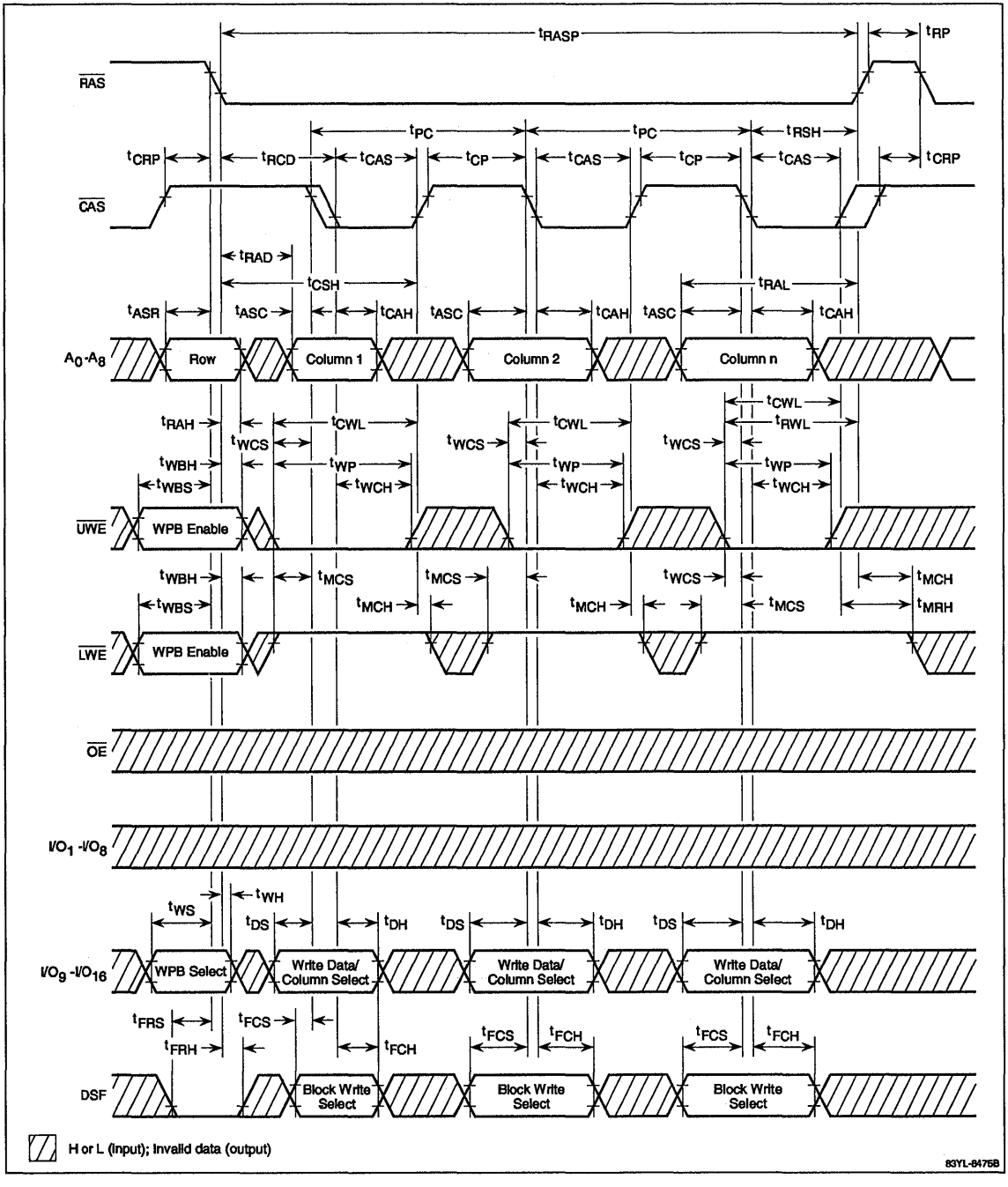
Timing Waveforms (cont)

Fast-Page, Early-Write Cycle; Word and Word Block



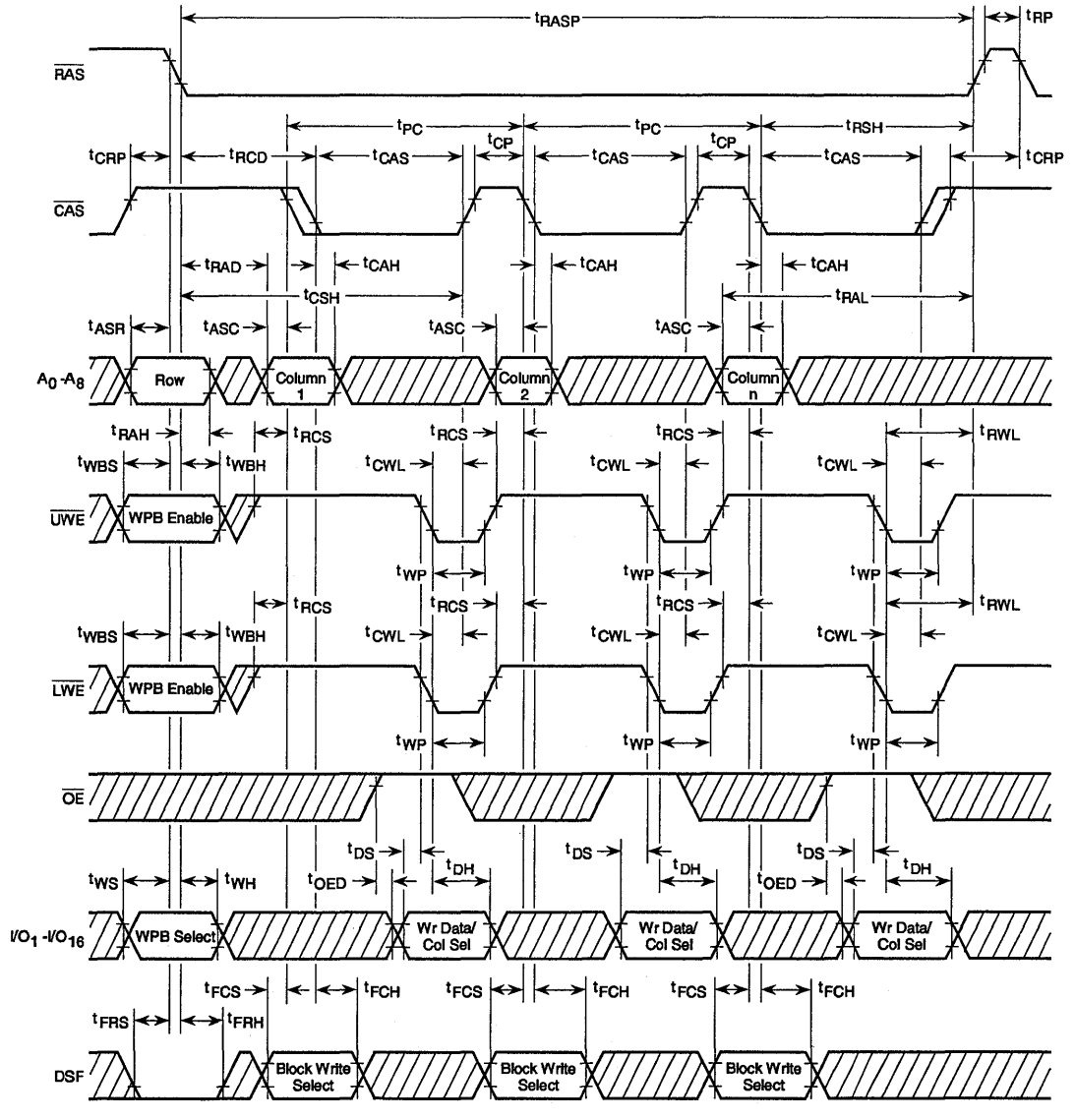
Timing Waveforms (cont)

Fast-Page, Early-Write Cycle; Upper-Byte and Upper-Byte Block



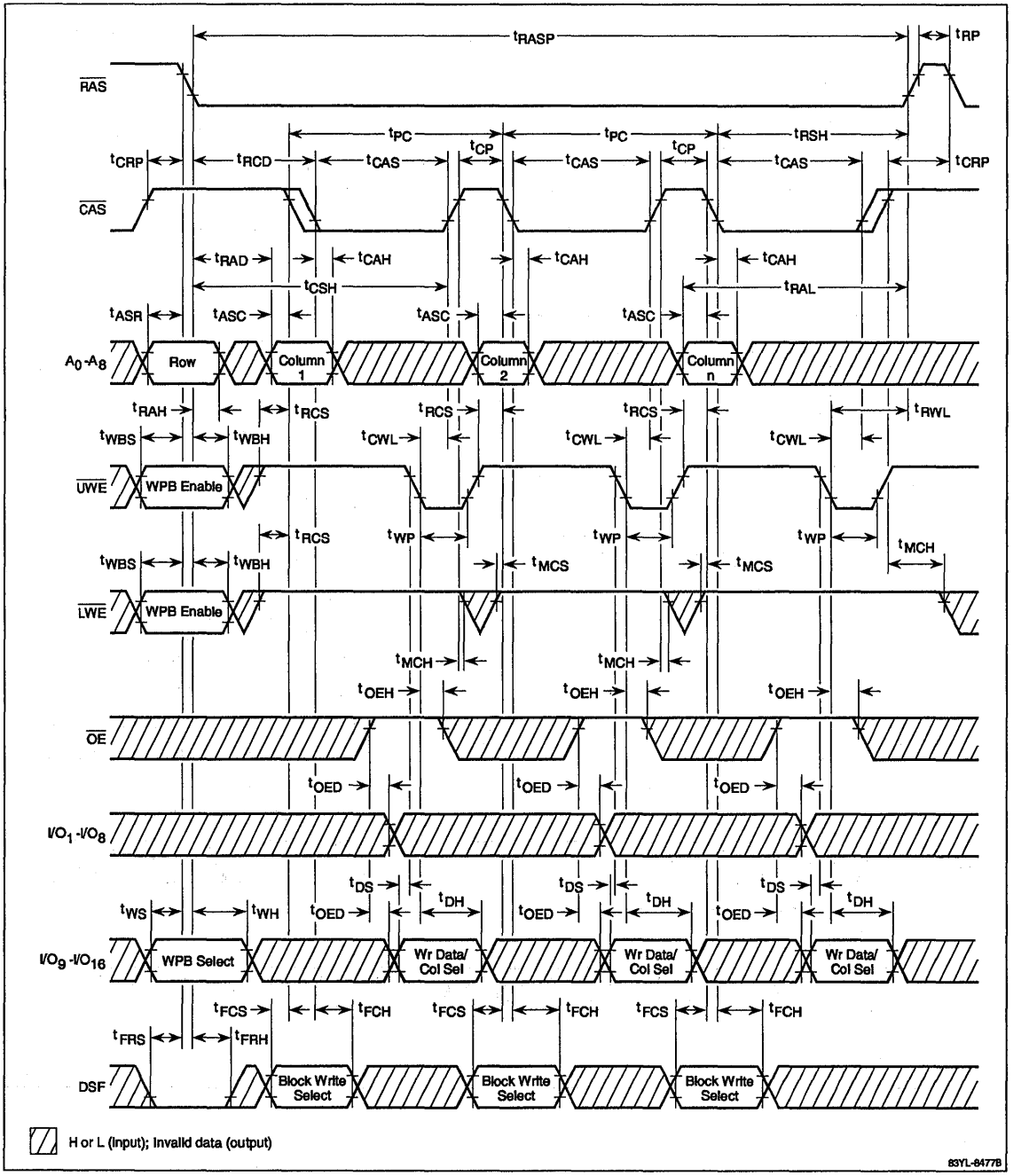
Timing Waveforms (cont)

Fast-Page, Late-Write Cycle; Word and Word Block



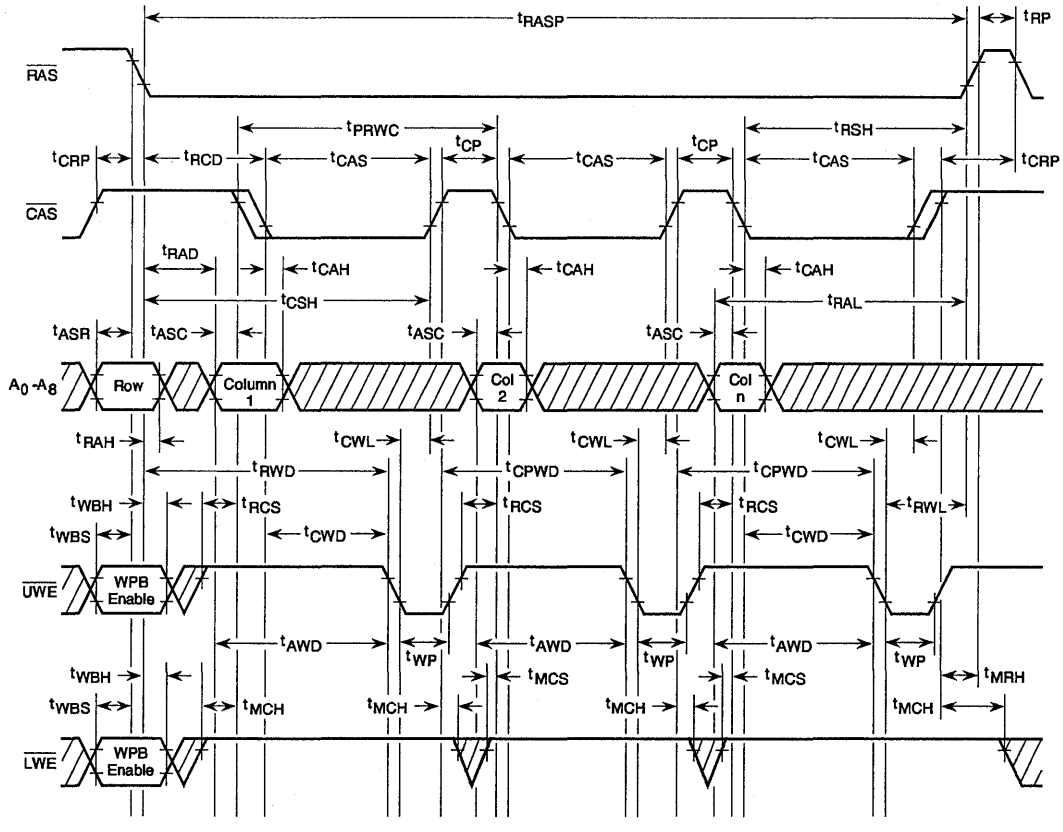
Timing Waveforms (cont)

Fast-Page, Late-Write Cycle; Upper-Byte and Upper-Byte Block



Timing Waveforms (cont)

Fast-Page, Read-Modify-Write Cycle (With exended output); Upper-Byte and Upper-Byte Block (Sheet 1 of 2)



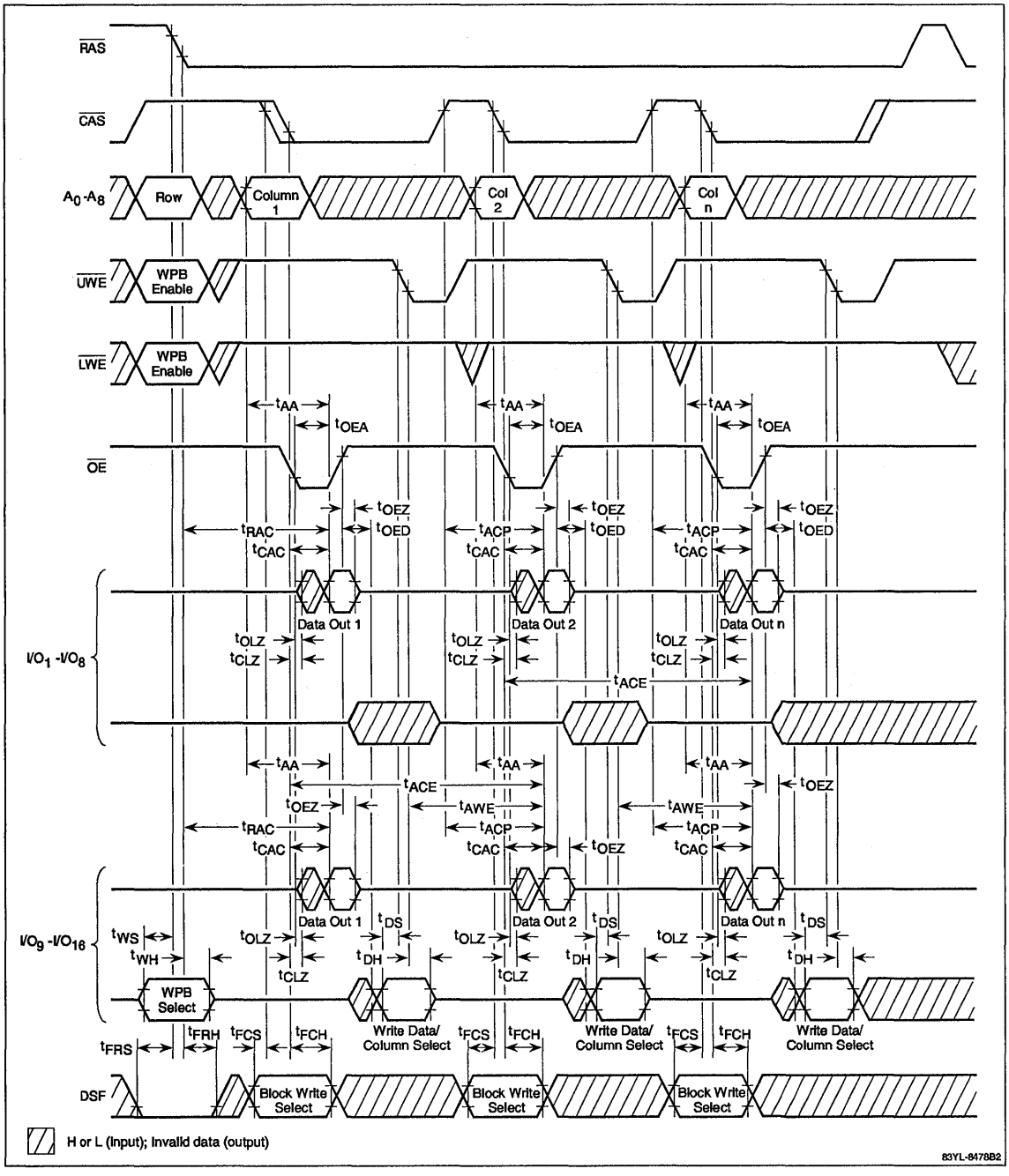
The waveforms above are repeated on sheet 2 but without the timing parameters.

83YL-8478B1

18m

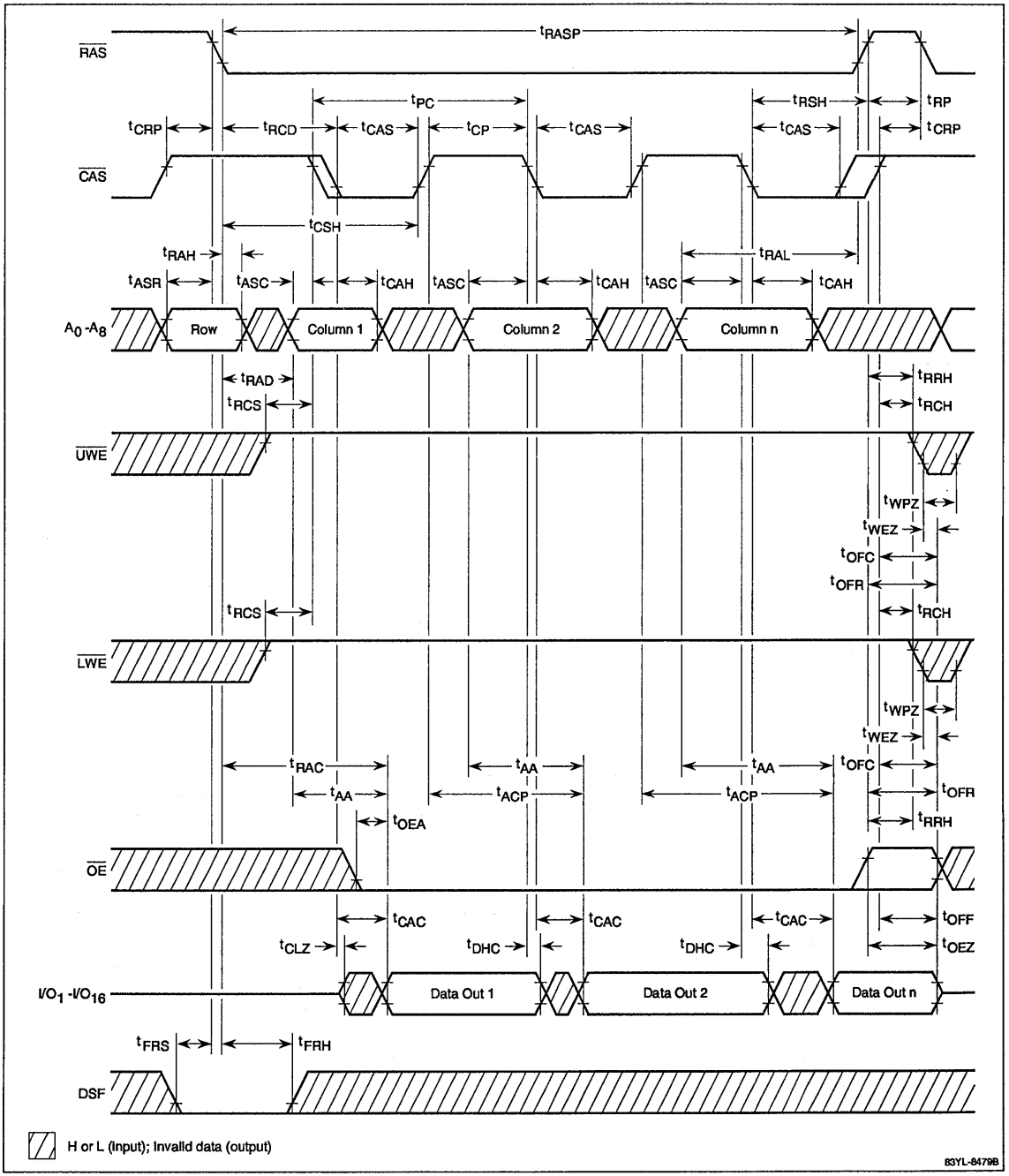
Timing Waveforms (cont)

Fast-Page, Read-Modify-Write Cycle (With exended output); Upper-Byte and Upper-Byte Block (Sheet 2 of 2)



Timing Waveforms (cont)

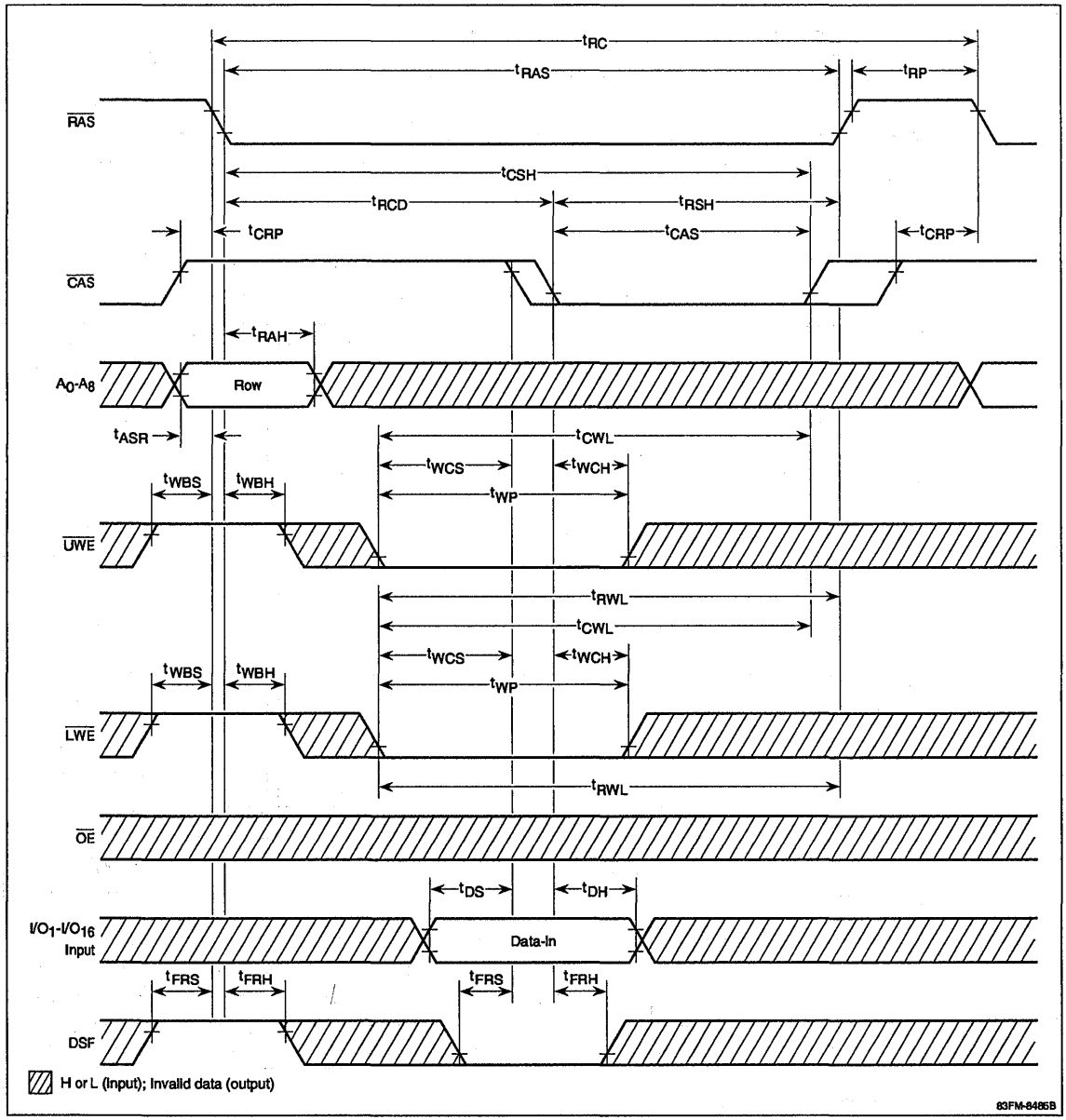
Fast-Page, Read Cycle (With extended output); Word



18m

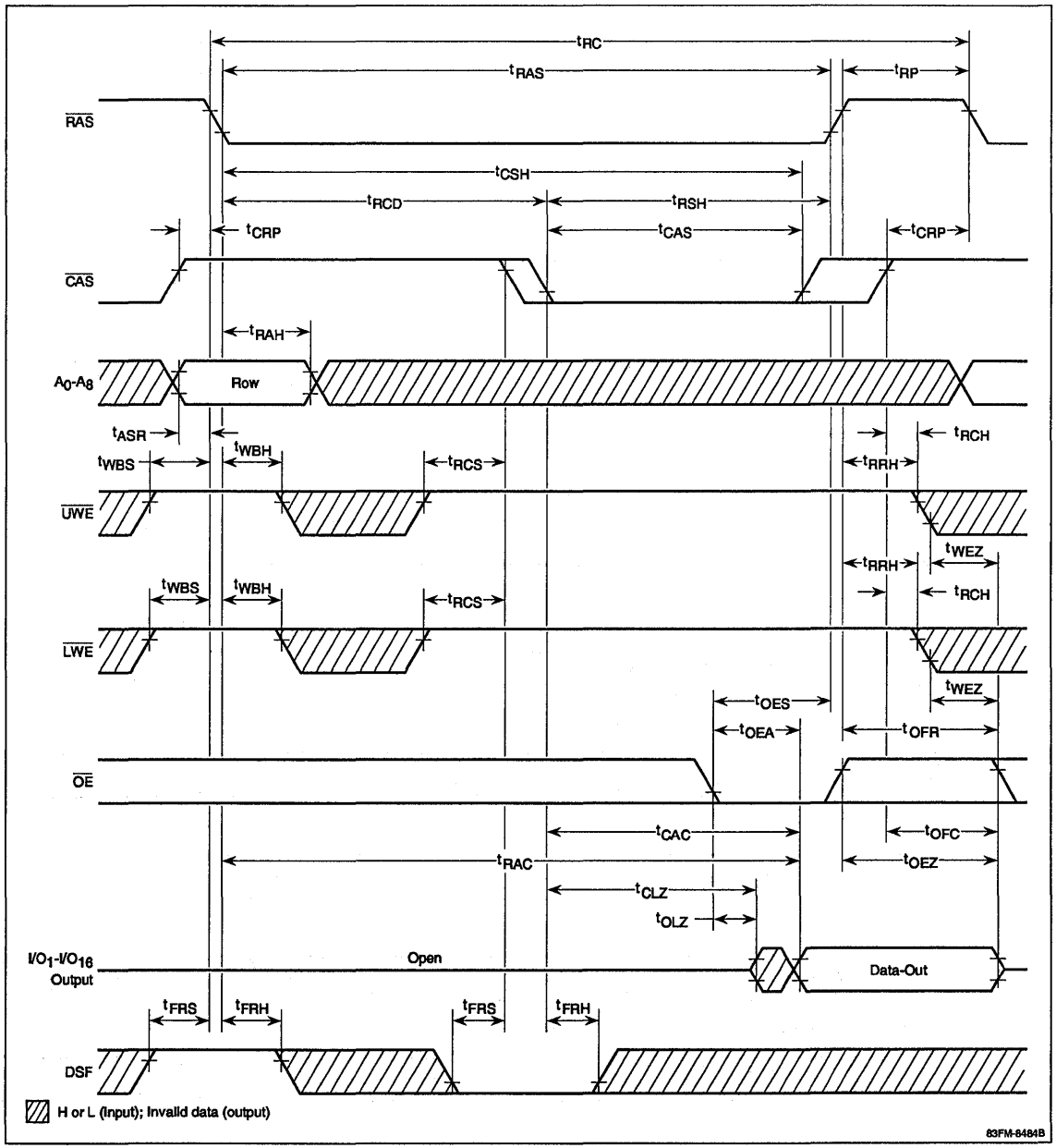
Timing Waveforms (cont)

Load Old Mask Register Cycle (Early-write)



Timing Waveforms (cont)

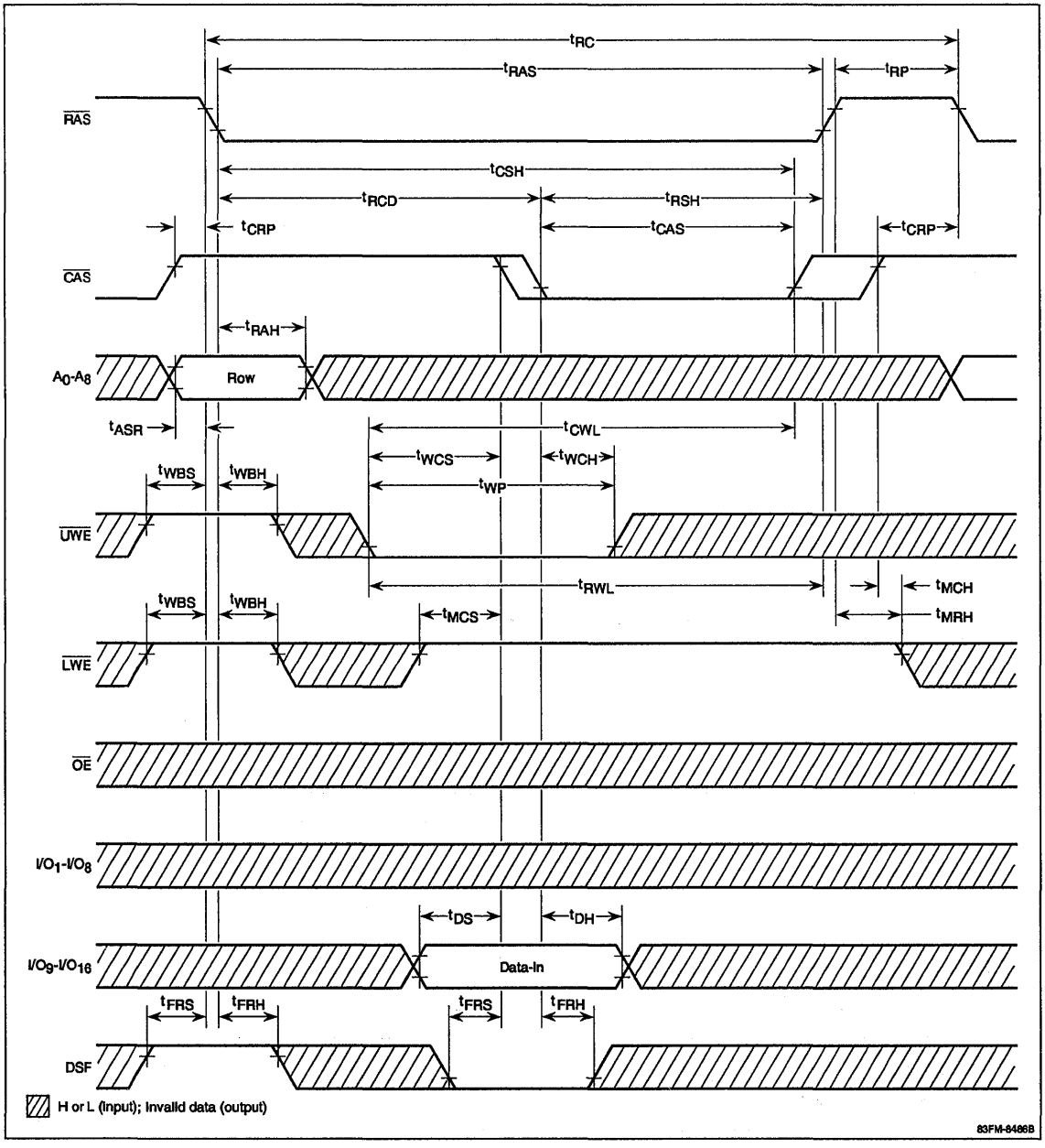
Load Old Mask Register Cycle (Read with extended output)



18m

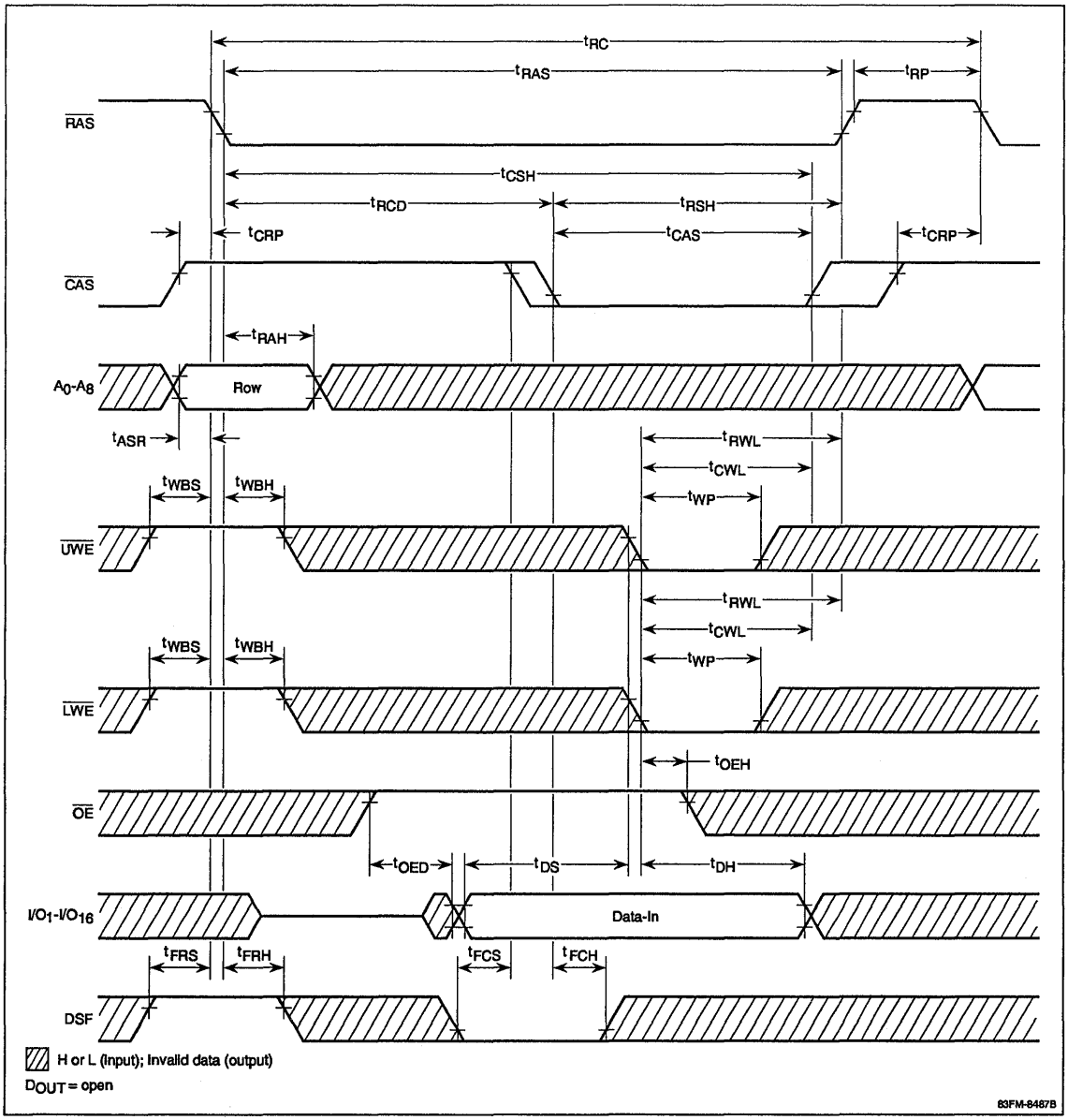
Timing Waveforms (cont)

Load Old Mask Register Cycle (Upper-byte, early-write)



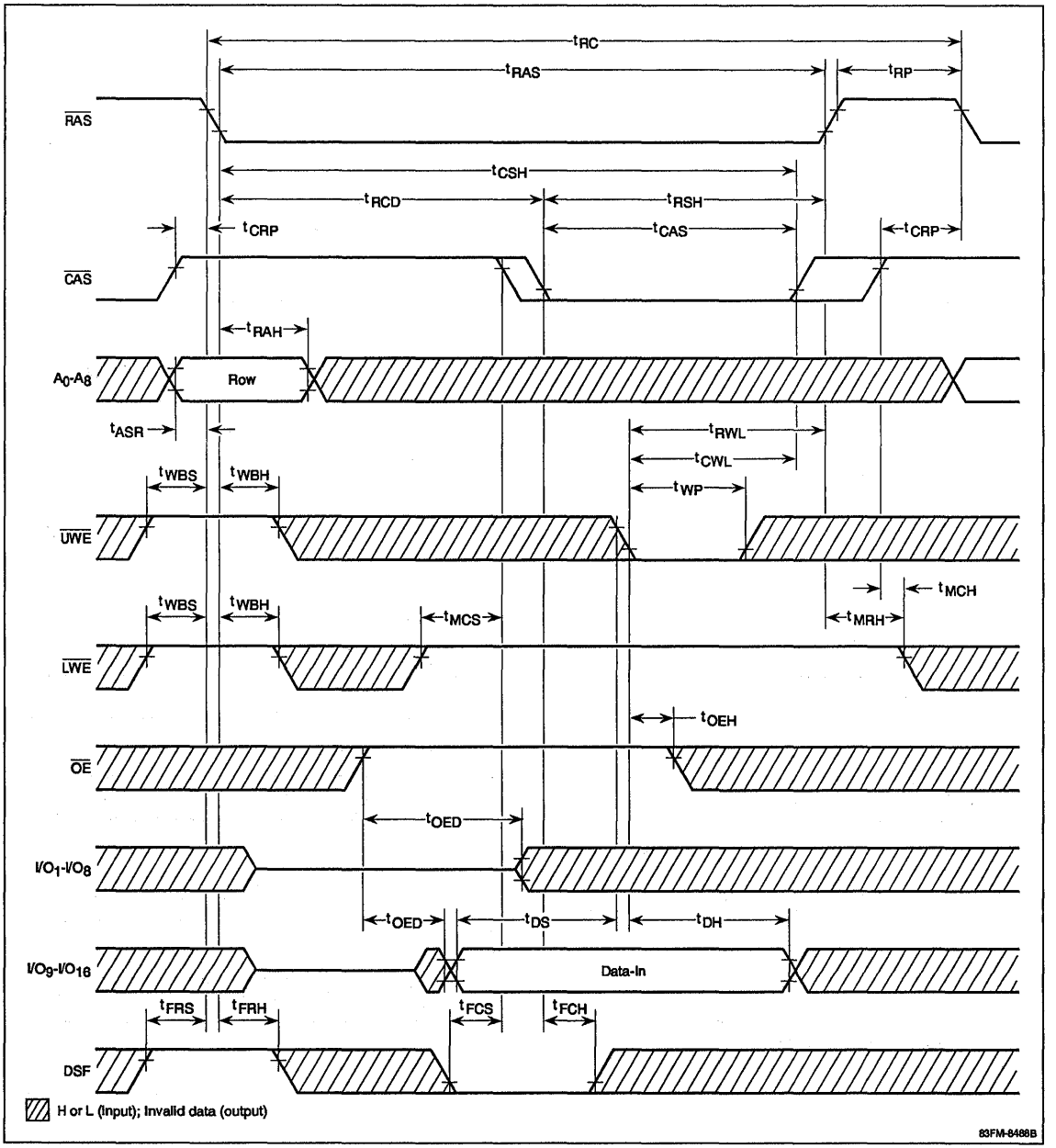
Timing Waveforms (cont)

Load Old Mask Register Cycle (Late-write)



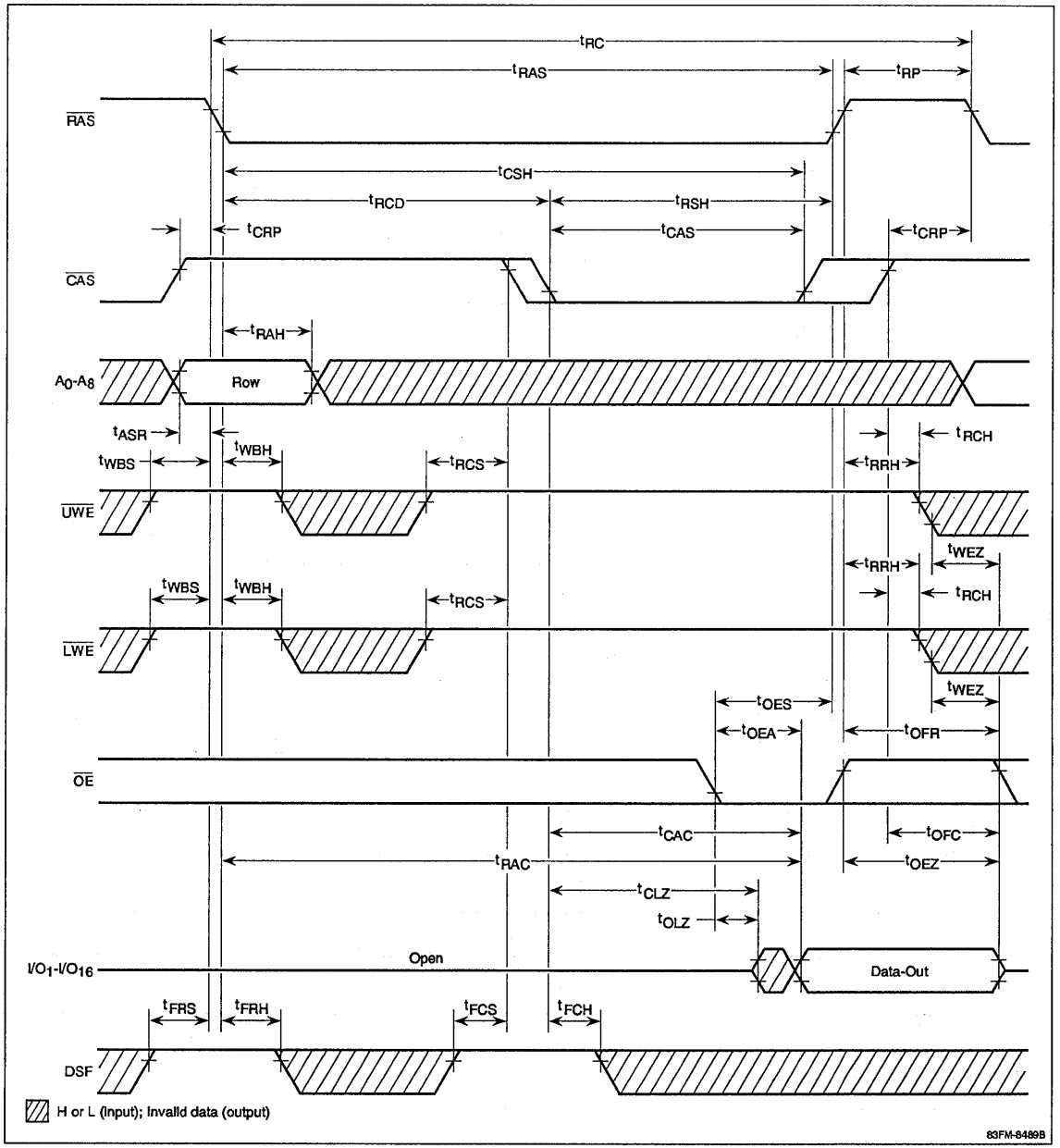
Timing Waveforms (cont)

Load Old Mask Register Cycle (Upper-byte, late-write)



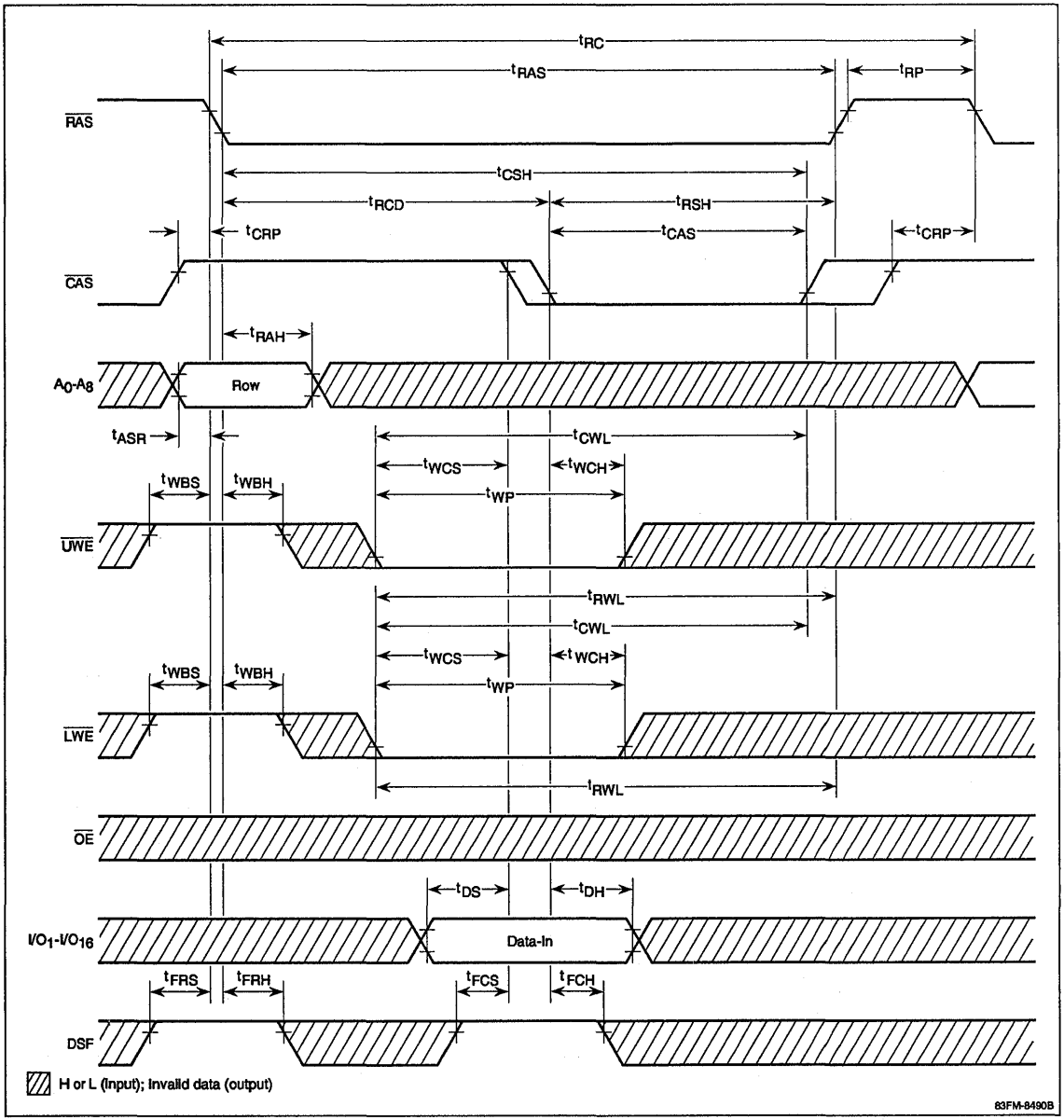
Timing Waveforms (cont)

Color Register Set Cycle (Read with extended output)



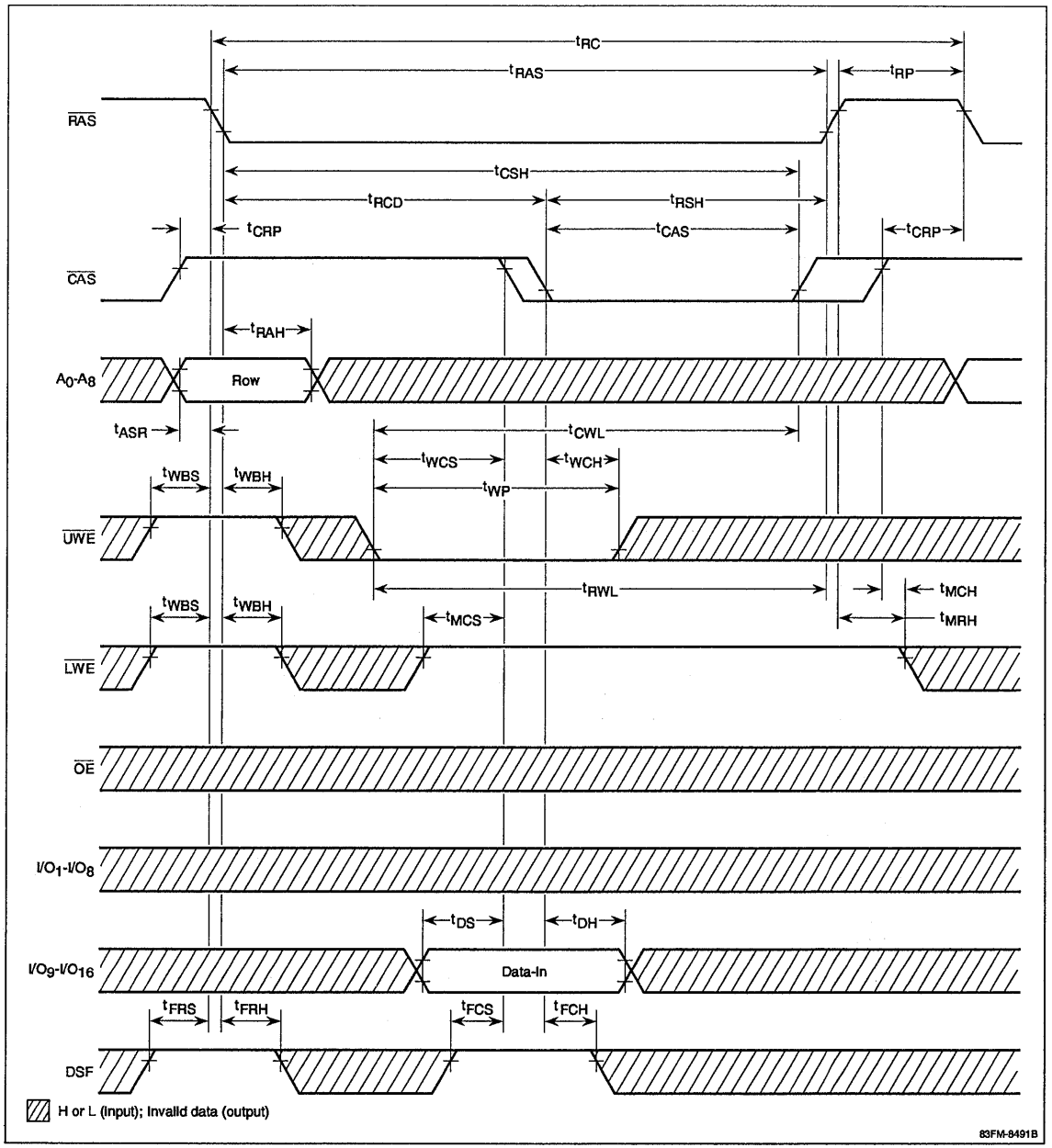
Timing Waveforms (cont)

Color Register Set Cycle (Early-write)



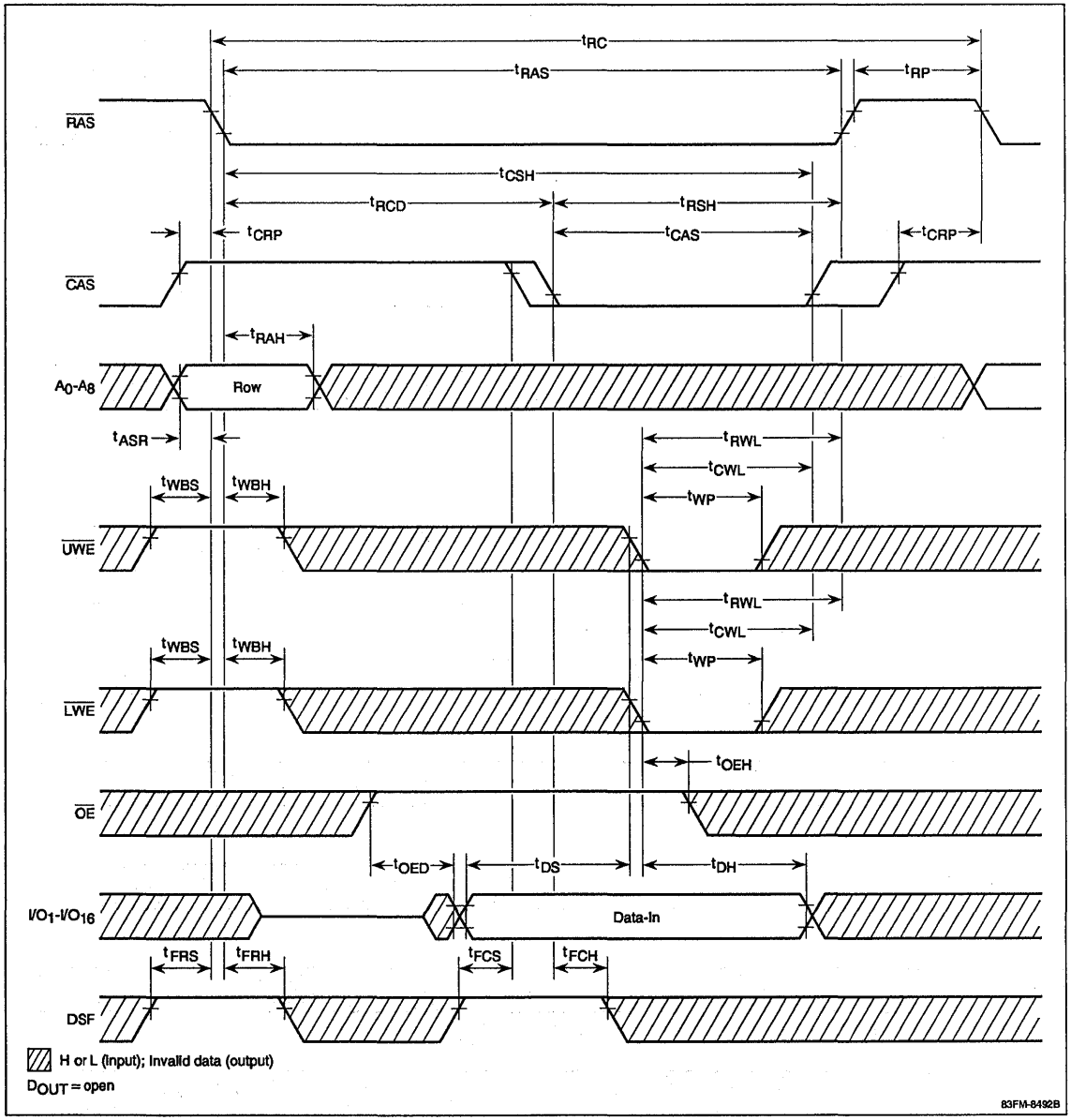
Timing Waveforms (cont)

Color Register Set Cycle (Upper-byte, early-write)



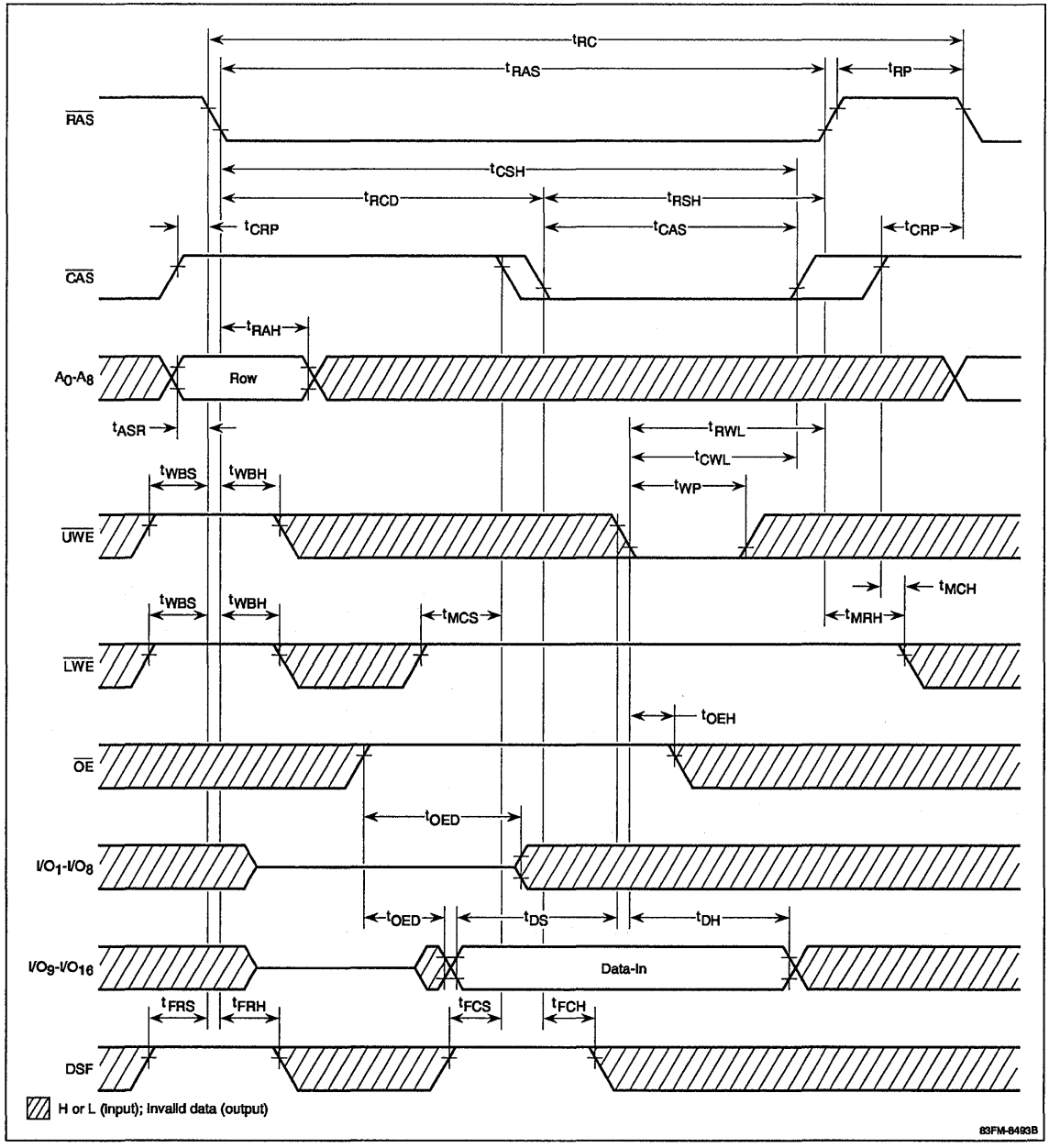
Timing Waveforms (cont)

Color Register Set Cycle (Late-write)



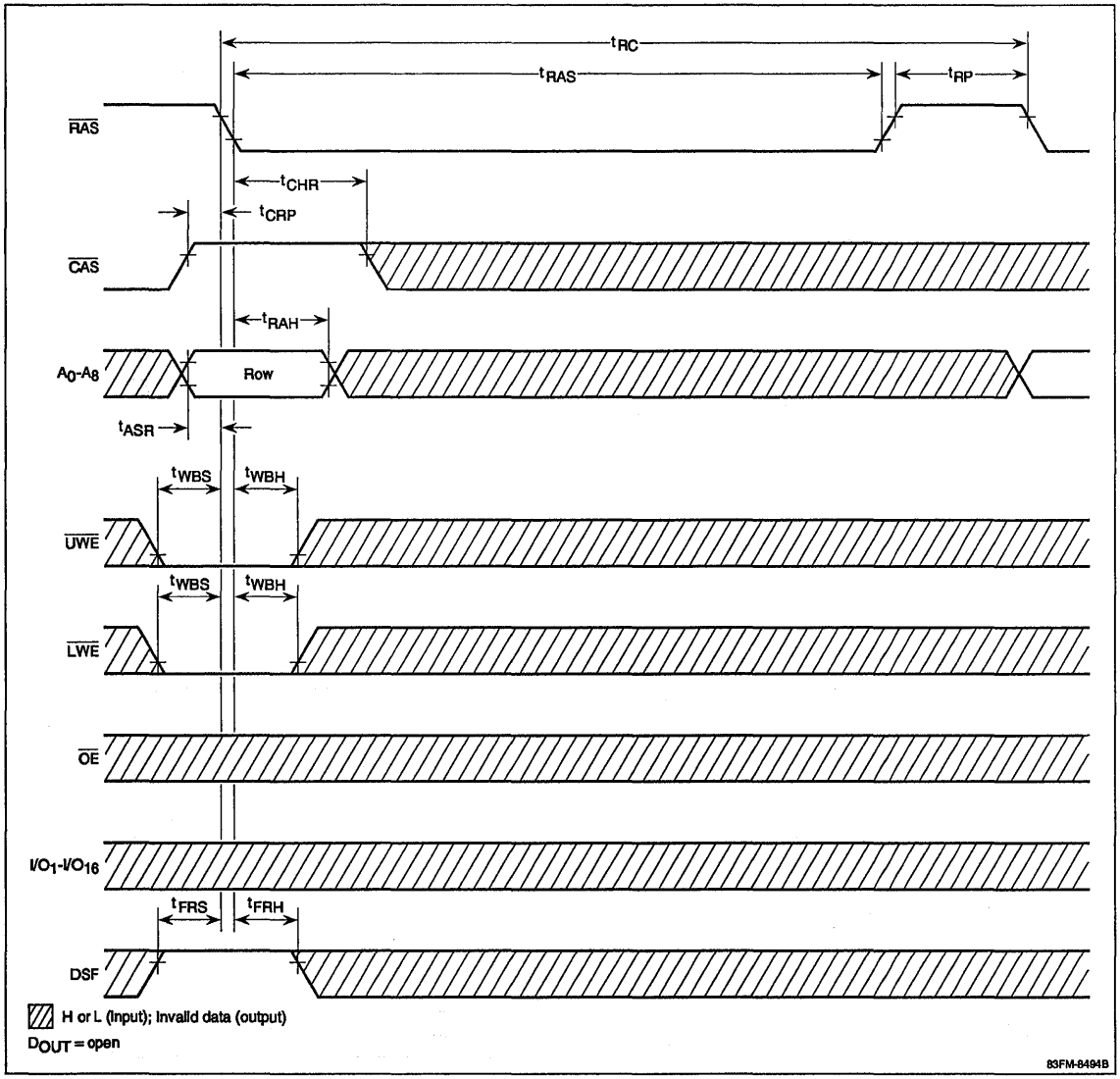
Timing Waveforms (cont)

Color Register Set Cycle (Upper-byte, late-write)



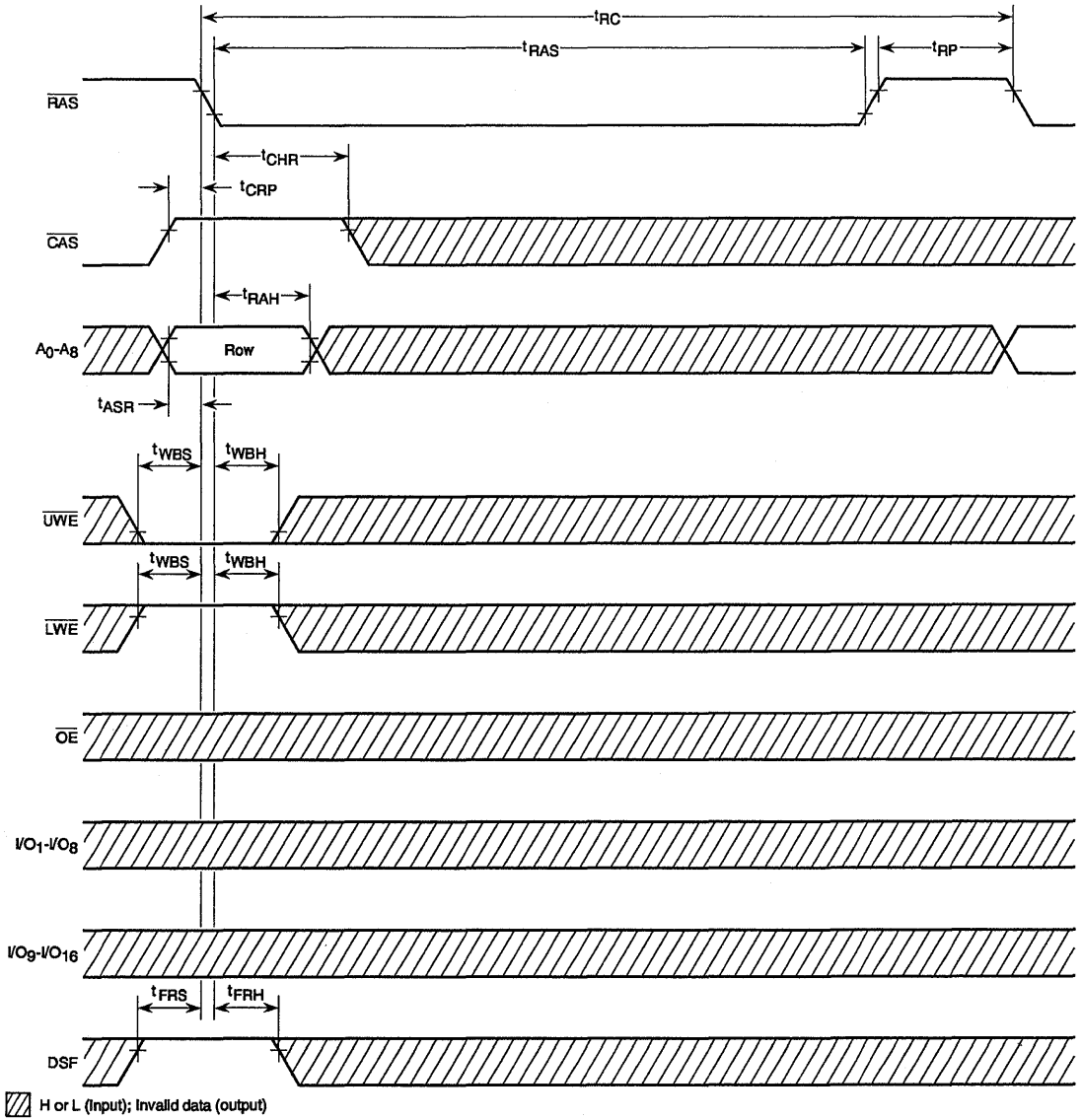
Timing Waveforms (cont)

Flash-Write Cycle



Timing Waveforms (cont)

Flash-Write Cycle (Upper-byte, flash-write)



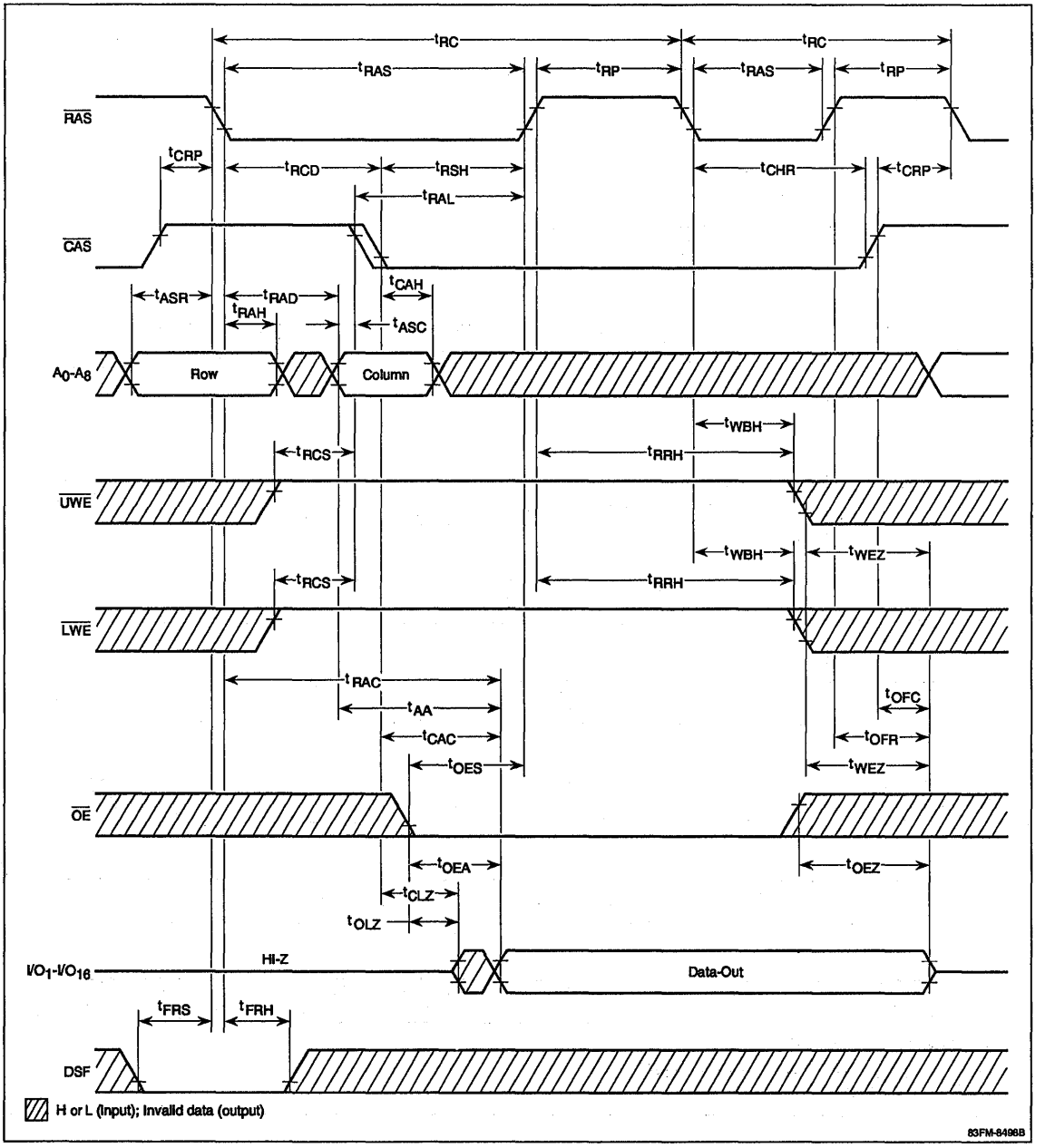
Note: The lower-byte color register data is not written even if $\overline{CAS}$ and $\overline{LWE}$ go active later in the cycle.

83FM-8496B

18m

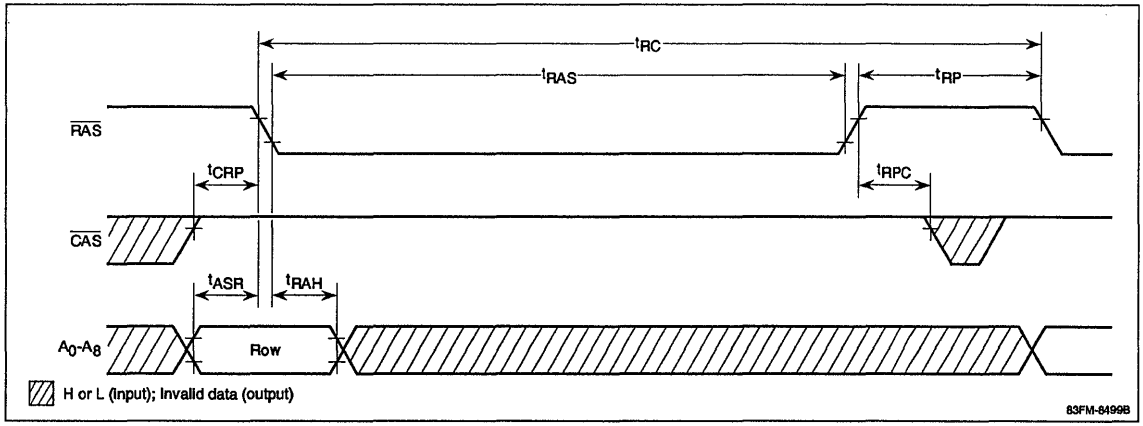
Timing Waveforms (cont)

Hidden Refresh Cycle (With exended output)

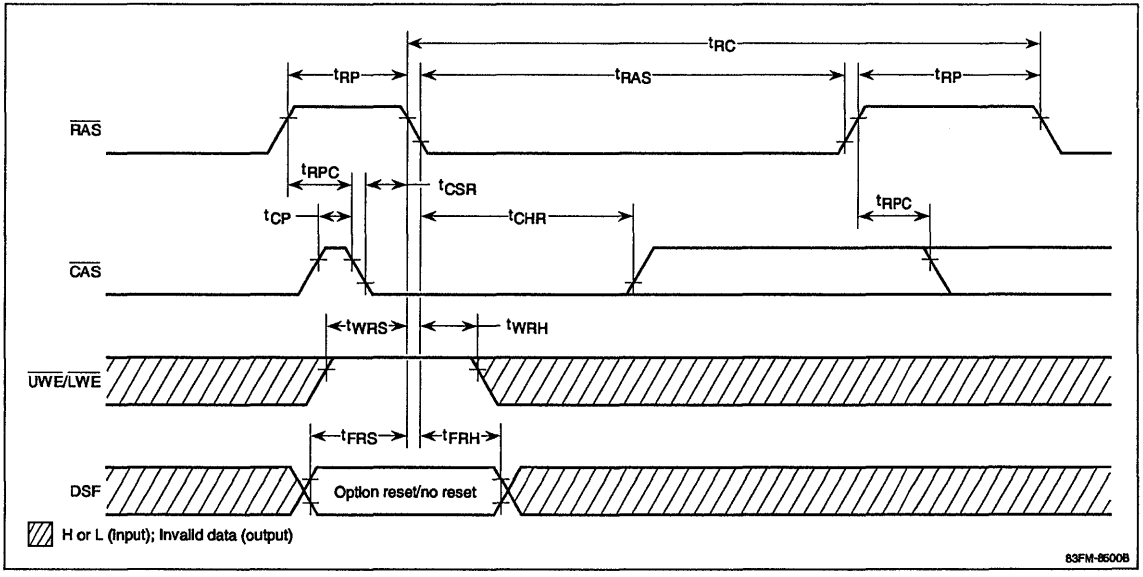


Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



NEC

Section 19
Fast Static RAMs (64K)

μPD	Org	Features	
4361B	64K x 1	12-ns	19a
4362B	16K x 4	12-ns	19b
4363B	16K x 4	12-ns; Output enable	19c
4368	8K x 8	15-ns; Output enable, two chip enables	19d
4369	8K x 9	15-ns; Output enable, two chip enables	19e

μPD4361B
65,536 x 1-bit
Static CMOS RAM

Description

The μPD4361B is a 65,536-word by 1-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD4361B a high-speed device that requires very low power and no clock or refreshing.

The device is packaged in a 22-pin plastic DIP and 24-pin plastic SOJ and has two types of access times, address and chip select.

Features

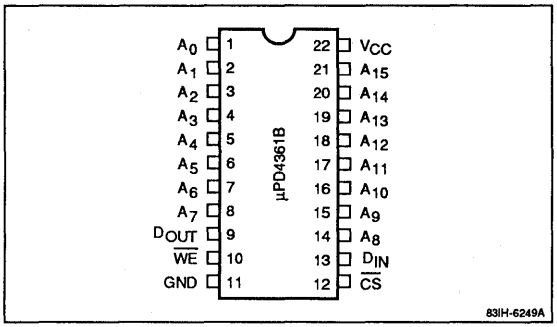
- 65, 536 x 1-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Standard 22-pin plastic DIP and 24-pin plastic SOJ

Ordering Information

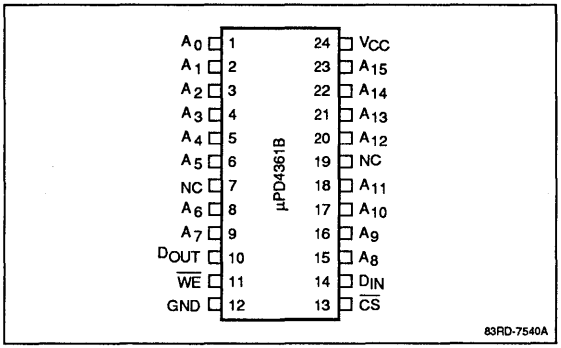
Part Number	Access Time (max)	Package
μPD4361BCR-12	12 ns	22-pin plastic DIP
CR-15	15 ns	
CR-20	20 ns	
μPD4361BLA-12	12 ns	24-pin plastic SOJ
LA-15	15 ns	
LA-20	20 ns	

Pin Configurations

22-Pin Plastic DIP



24-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage output voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V minimum for 10 ns maximum pulse.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	Input/Output	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High-Z	Active

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V minimum for 10 ns maximum pulse.

Capacitance

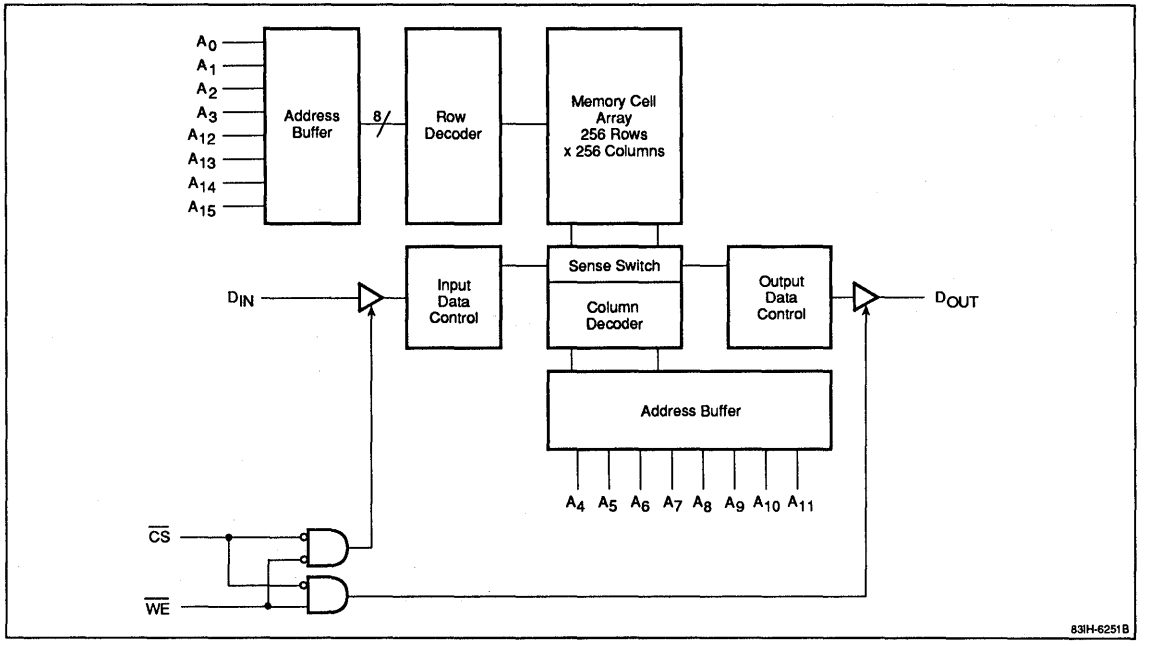
T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			6	pF
Output capacitance	C_{DOUT}			8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Standby supply current	I_{SB}			20	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD4361B-12		μPD4361B-15		μPD4361B-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		130		120		110	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Read cycle time	t_{RC}	12		15		20		ns	(Note 2)
Address access time	t_{AA}		12		15		20	ns	
Chip select access time	t_{ACS}		12		15		20	ns	
Output hold from address change	t_{OH}	2		3		3		ns	
Chip select to output in low-Z	t_{LZ}	2		3		3		ns	(Note 3)
Chip deselect to output in high-Z	t_{HZ}	0	7	0	7	0	8	ns	(Note 4)
Chip select to power-up time	t_{PU}	0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	7	0	8	0	15	ns	
Write Operation									
Write cycle time	t_{WC}	12		15		20		ns	(Note 2)
Chip select to end of write	t_{CW}	11		13		15		ns	
Address valid to end of write	t_{AW}	11		13		15		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	10		12		14		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	7		7		8		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WZ}	0	7	0	7	0	8	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

Figure 1. Output Load

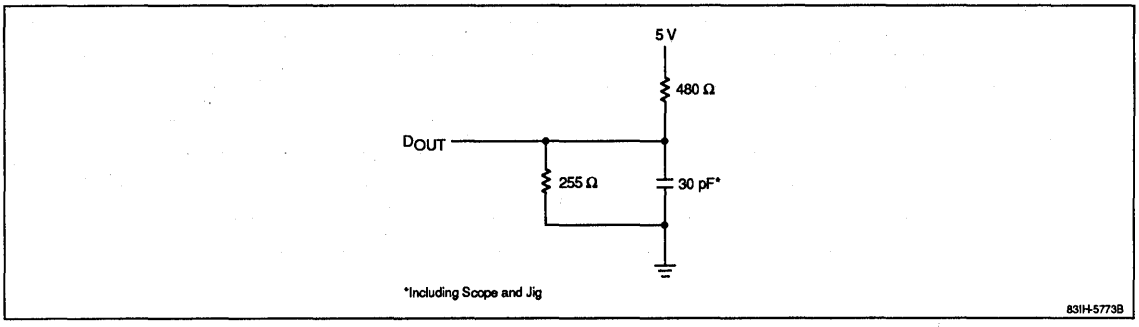
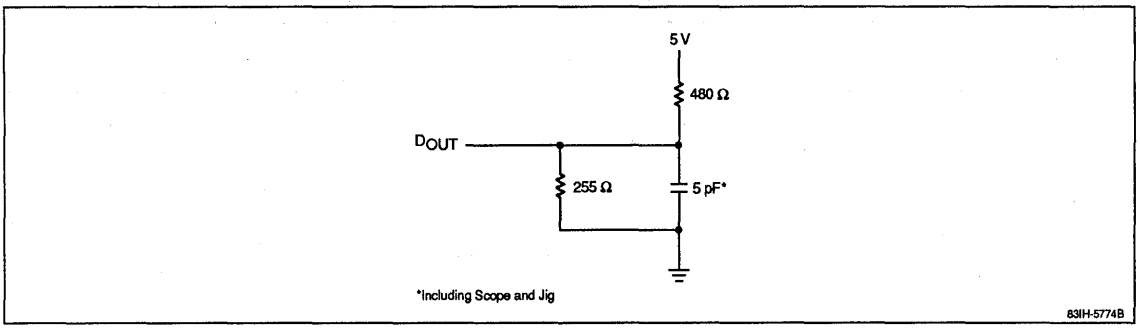
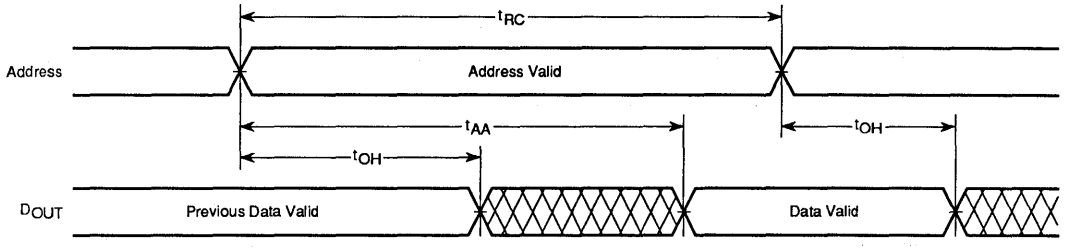


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW}



Timing Waveforms

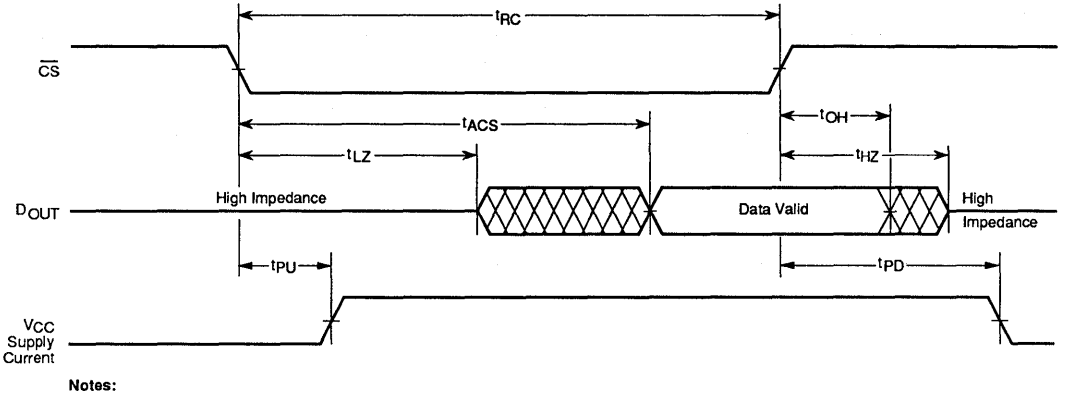
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle

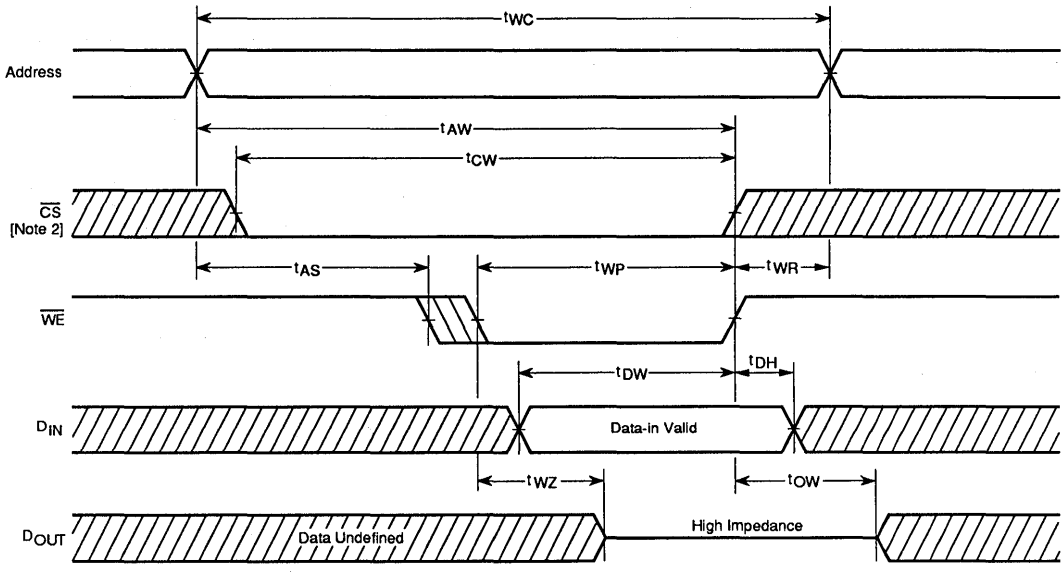


Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address is valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6252B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

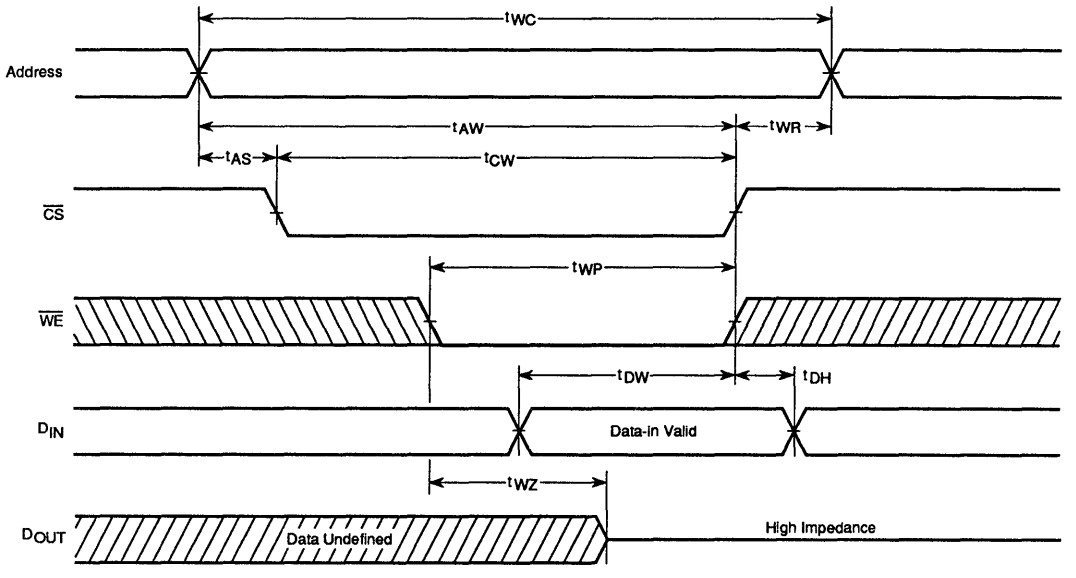
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{CS}$ and $\overline{WE}$ go high simultaneously, the outputs remain in high impedance.

83IH-6261B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83IH-6262B

μPD4362B
16,384 x 4-Bit
Static CMOS RAM

Description

The μPD4362B is a 16,384-word by 4-bit static RAM fabricated with advanced silicon-gate technology. A unique design using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD4362B a high-speed device that requires very low power and no clock or refreshing.

The μPD4362B is packaged in a standard 22-pin plastic DIP and 24-pin plastic SOJ.

Features

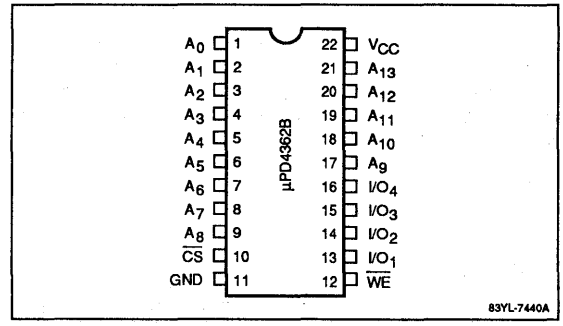
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Standard 300-mil, 22-pin plastic DIP and 24-pin plastic SOJ packaging

Ordering Information

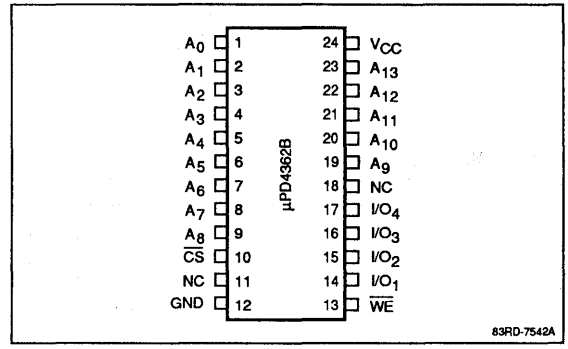
Part Number	Access Time (max)	Package
μPD4362BCR-12	12 ns	22-pin plastic DIP
CR-15	15 ns	
CR-20	20 ns	
μPD4362BLA-12	12 ns	24-pin plastic SOJ
LA-15	15 ns	
LA-20	20 ns	

Pin Configuration

22-Pin Plastic DIP



24-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{13}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V for 10 ns pulse.

Truth Table

Function	$\overline{CE}$	$\overline{WE}$	Input/Output	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

Notes:

(1) X = don't care.

Capacitance

T_A = 25°C; f = 1 MHz (Note 1); V_{IN} and V_{DOUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			6	pF
Output capacitance	C_{DOUT}			8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

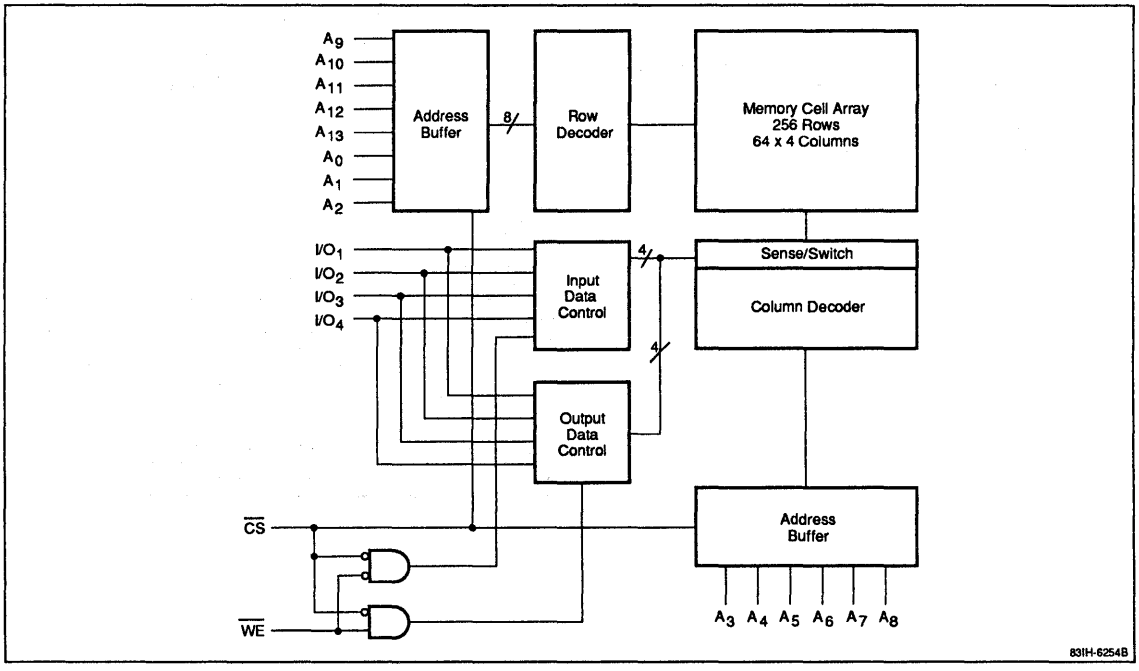
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V for 10 ns pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}; V_{CC} = max
Standby supply current	I_{SB}			20	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD4362B-12		μPD4362B-15		μPD4362B-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		130		120		110	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Read cycle time	t_{RC}	12		15		20		ns	(Note 2)
Address access time	t_{AA}		12		15		20	ns	
Chip selection access time	t_{ACS}		12		15		20	ns	
Output hold from address change	t_{OH}	2		3		3		ns	
Chip selection to output to low-Z	t_{LZ}	2		3		3		ns	(Note 3)
Chip deselection to output to high-Z	t_{HZ}	0	7	0	7	0	8	ns	(Note 4)
Chip selection to power-up time	t_{PU}	0		0		0		ns	
Chip deselection to power-down time	t_{PD}	0	7	0	15	0	20	ns	
Write Operation									
Write cycle time	t_{WC}	12		15		20		ns	(Note 2)
Chip selection to end of write	t_{CW}	11		13		15		ns	
Address valid to end of write	t_{AW}	11		13		15		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	10		12		14		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	7		7		8		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WZ}	0	7	0	7	0	8	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

Figure 1. Output Load

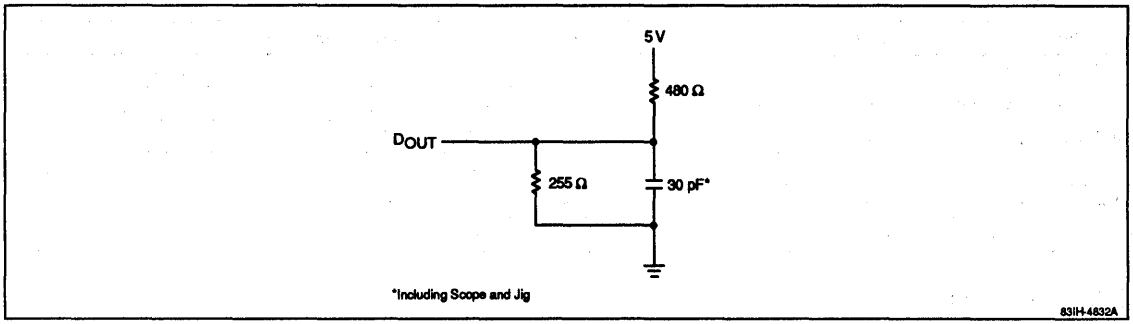
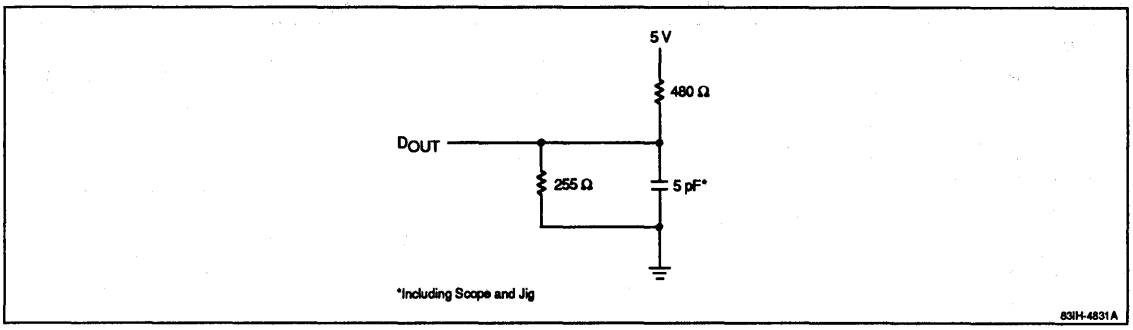
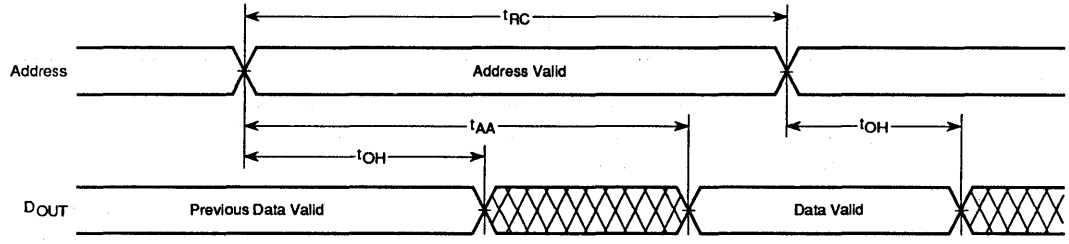


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW}



Timing Waveforms

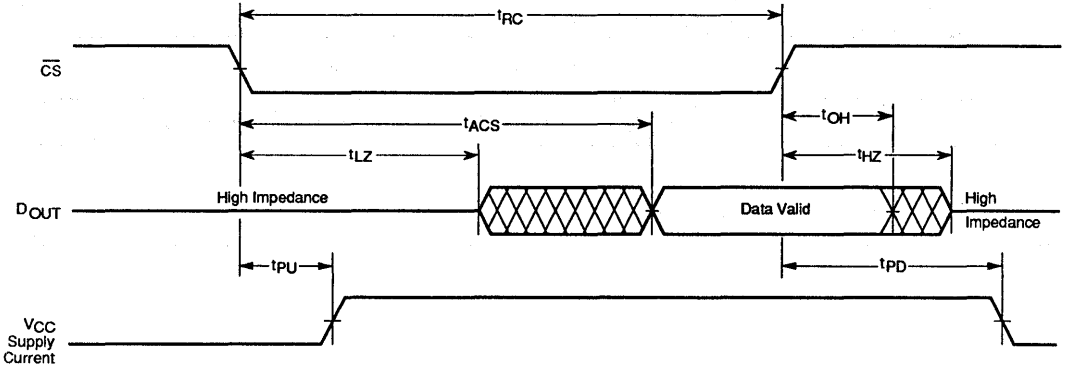
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle

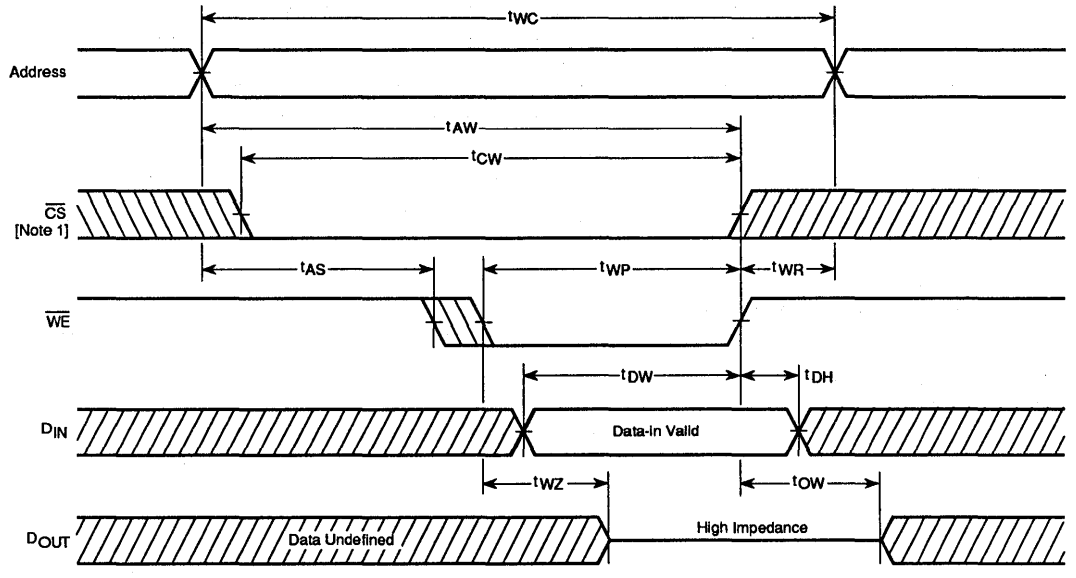


Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address is valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6252B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



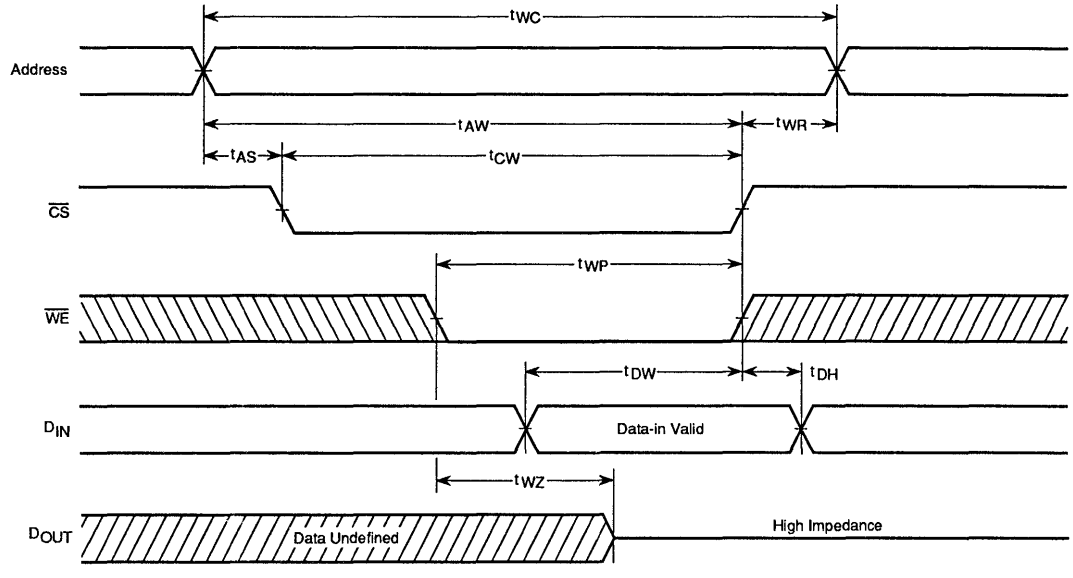
Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83IH-6268B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83IH-6262B

19b

μPD4363B
16,384 x 4-Bit
Static CMOS RAM

Description

The μPD4363B is a 16,384-word by 4-bit static RAM fabricated with advanced silicon-gate technology. A unique design using CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD4363B a high-speed device that requires very low power and no clock or refreshing.

The μPD4363B is packaged in a standard 300-mil, 24-pin plastic DIP and 24-pin plastic SOJ.

Features

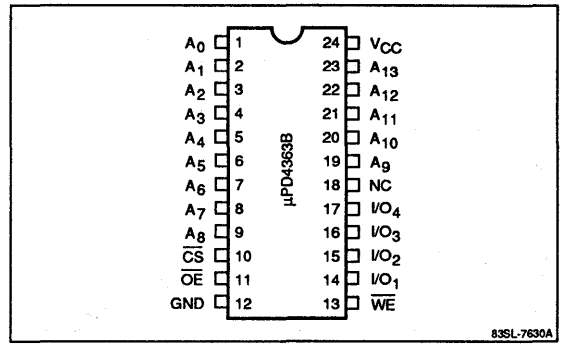
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- $\overline{OE}$ eliminates the need for external bus buffers
- Three-state outputs
- Low power dissipation
  - 130 mA max (active)
  - 2 mA max (standby)
- Standard 300-mil, 24-pin plastic DIP and 24-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD4363BCR-12	12 ns	24-pin plastic DIP
CR-15	15 ns	
CR-20	20 ns	
μPD4363BLA-12	12 ns	24-pin plastic SOJ
LA-15	15 ns	
LA-20	20 ns	

Pin Configuration

24-Pin Plastic DIP or SOJ



Pin Identification

Symbol	Function
A_0 - A_{13}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+ 5-volt power supply
NC	No connection

19c

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} (min) = −3.0 V for 10 ns pulse.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V (Note 1)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			6	pF
Output capacitance	C_{DOUT}			8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

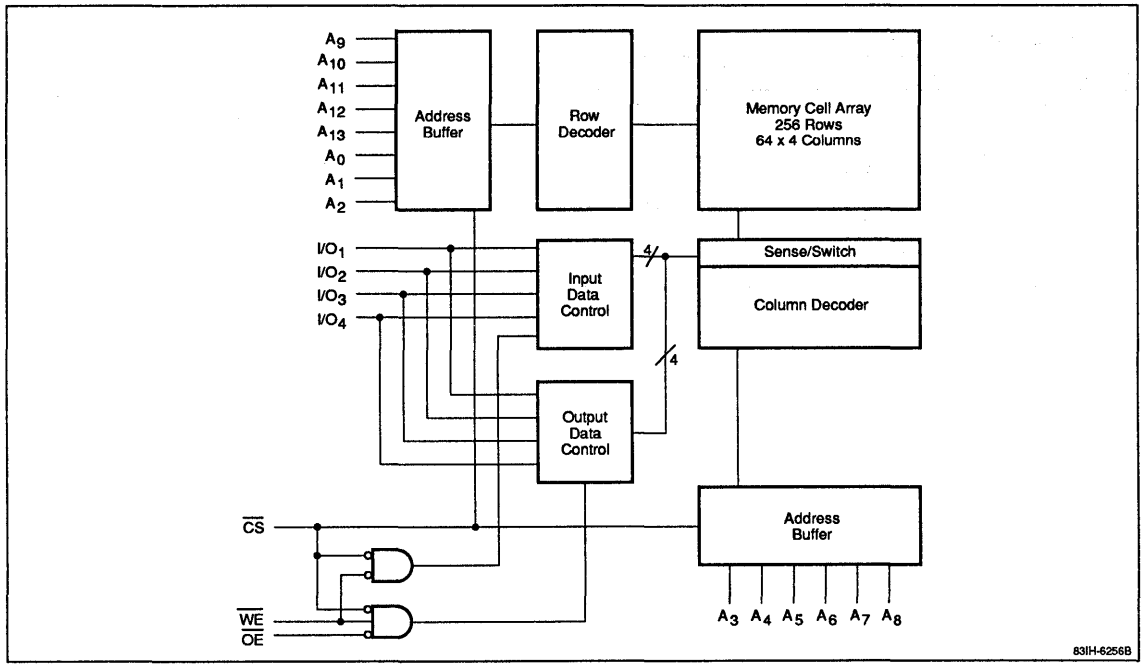
Notes:

(2) V_{IL} = −3.0 V for 10 ns pulse.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	I_{CC}
Not selected	H	X	X	High-Z	Standby
Read	L	H	L	D_{OUT}	Active
D_{OUT} disabled	L	H	H	High-Z	Active
Write	L	L	X	D_{IN}	Active

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}; V_{CC} = max
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ or $\overline{OE}$ = V_{IH}; V_{CC} = max
Standby supply current	I_{SB}			20	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ = V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD4363B-12		μPD4363B-15		μPD4363B-20			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		130		120		110	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Read cycle time	t_{RC}	12		15		20		ns	(Note 2)
Address access time	t_{AA}		12		15		20	ns	
Chip select access time	t_{ACS}		12		15		20	ns	
Output hold from address change	t_{OH}	2		3		3		ns	
Chip select to output in low-Z	t_{LZ}	2		3		3		ns	(Note 3)
Chip deselect to output in high-Z	t_{HZ}	0	7	0	7	0	8	ns	(Note 4)
Output enable access time	t_{OE}		8		9		10	ns	
Output enable to output in low-Z	t_{OLZ}	0		0		0		ns	(Note 3)
Output disable to output in high-Z	t_{OHZ}	0	7	0	7	0	8	ns	(Note 4)
Chip select to power-up time	t_{PU}	0		0		0		ns	
Chip deselect to power-down time	t_{PD}	0	7	0	10	0	12	ns	
Write Operation									
Write cycle time	t_{WC}	12		15		20		ns	(Note 2)
Chip select to end of write	t_{CW}	11		13		15		ns	
Address valid to end of write	t_{AW}	11		13		15		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	10		12		14		ns	
Write recovery time	t_{WR}	1		1		1		ns	
Data valid to end of write	t_{DW}	7		7		8		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WZ}	0	7	0	7	0	8	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

Figure 1. Output Load

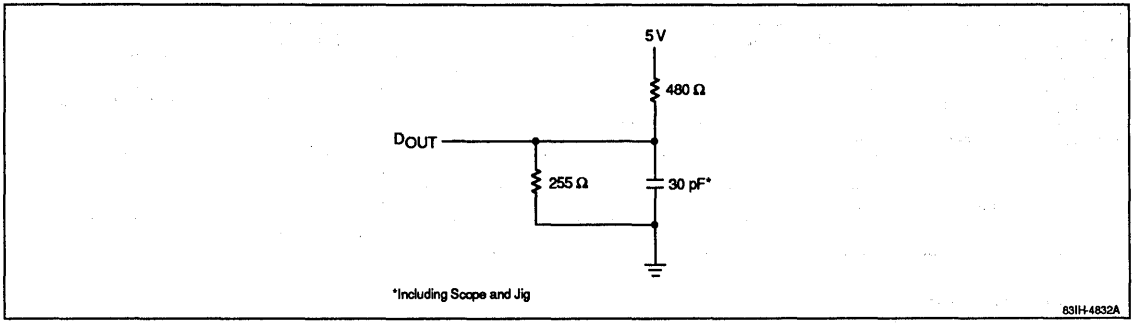
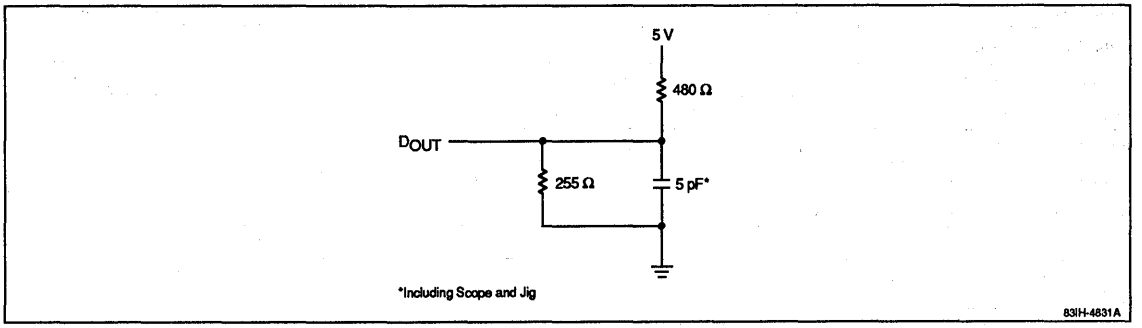
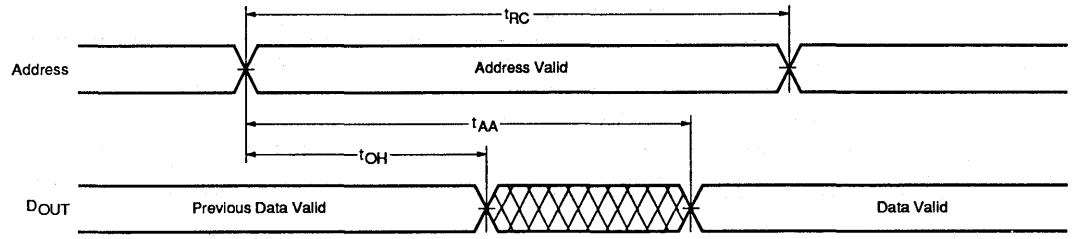


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ}, and t_{OW}



Timing Waveforms (cont)

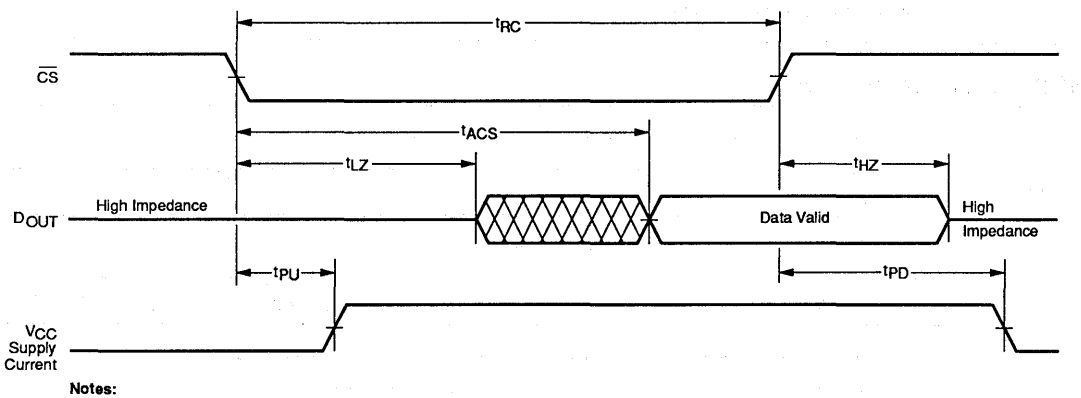
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6269B

Chip Select Access Cycle

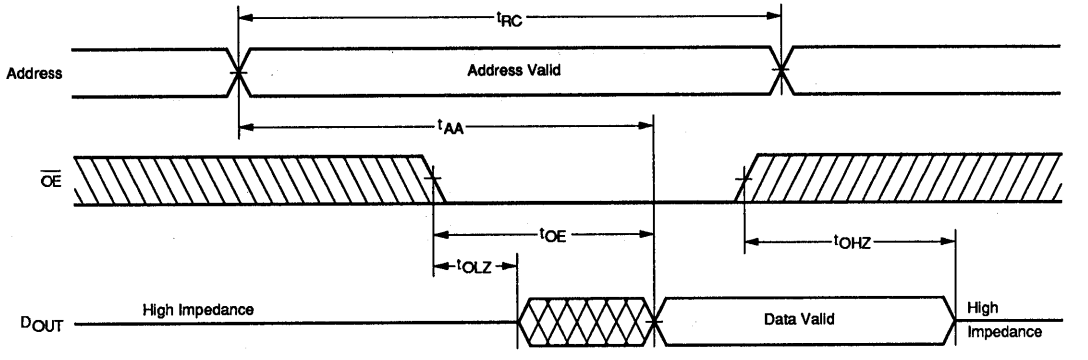


Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.
[3] $\overline{OE} = V_{IL}$.

83IH-6270B

Timing Waveforms (cont)

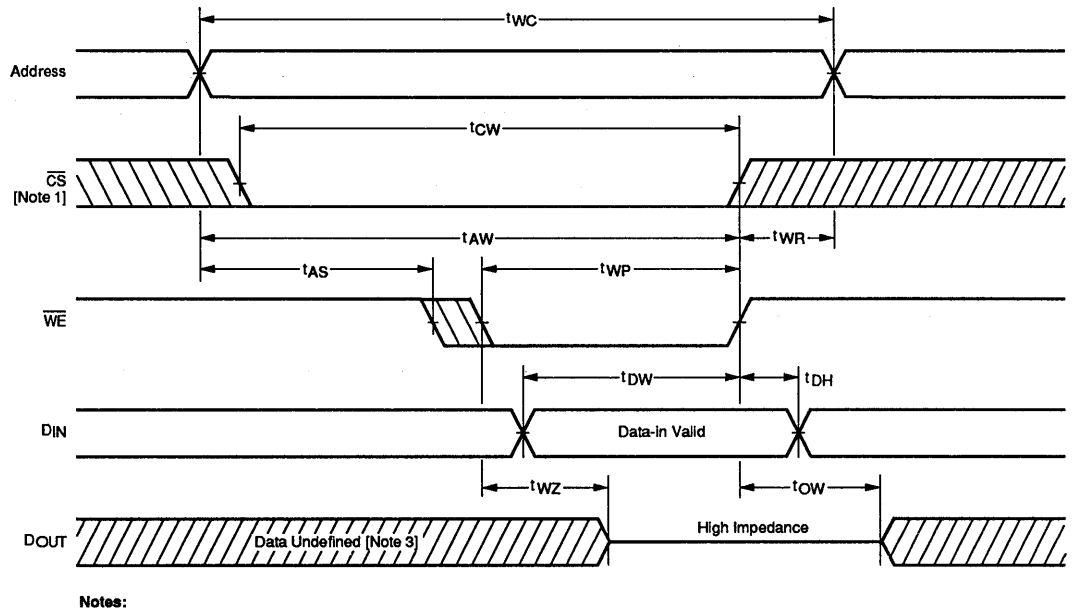
$\overline{OE}$-Controlled Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS}$ = V_{IL}.

83IH-6271B

$\overline{WE}$-Controlled Write Cycle

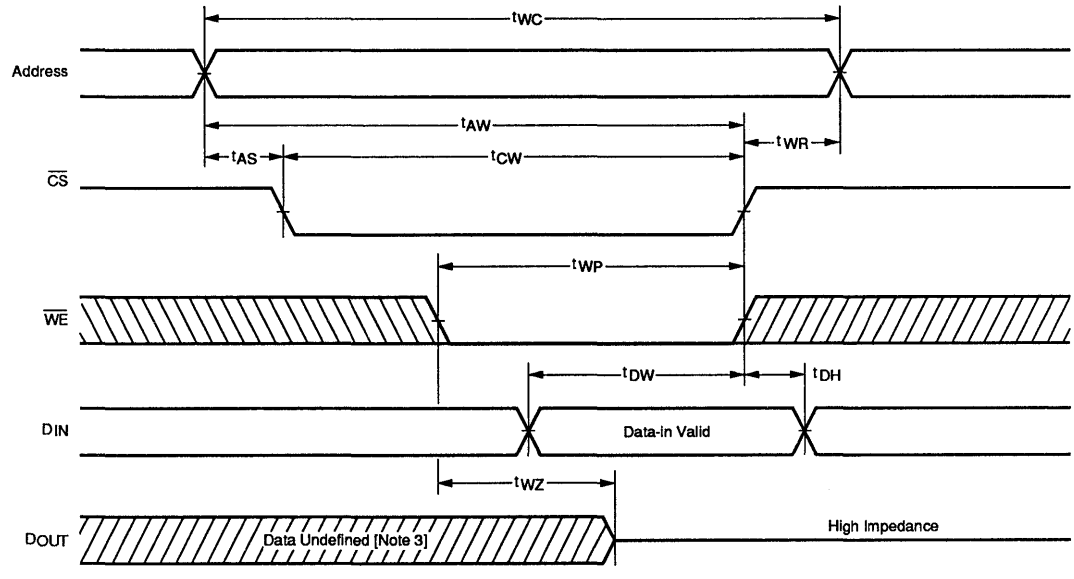


Notes:
[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.
[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

83IH-6272B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

83IH-6273B

19c

μPD4368
8,192 x 8-Bit
Static CMOS RAM

Description

The μPD4368 is a high-speed 8,192-word by 8-bit static RAM designed with CMOS peripheral circuits and N-channel memory cells with polysilicon resistors. Two chip enable pins are provided for battery backup application, and an output enable pin is provided for easy interface.

The μPD4368 is packaged in 28-pin plastic DIP and 28-pin plastic SOJ packaging.

Features

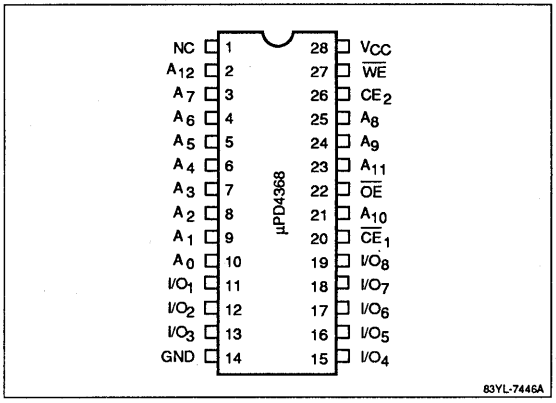
- 8,192 by 8-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{OE}$ and two $\overline{CE}$ pins for easy application
- Standard 28-pin plastic DIP, 28-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD4368CR-15	15 ns	28-pin plastic DIP
CR-20	20 ns	
μPD4368LA-15	15 ns	28-pin plastic SOJ
LA-20	20 ns	

Pin Configuration

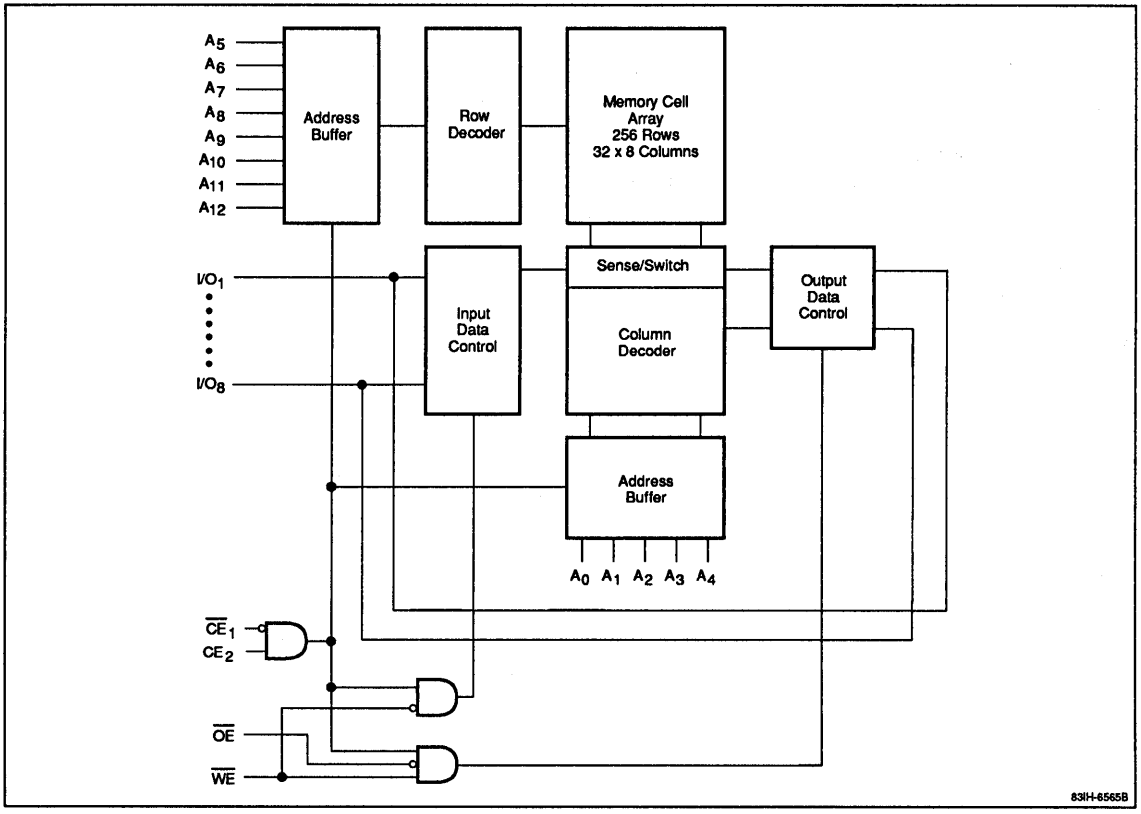
28-Pin Plastic DIP or SOJ



Pin Identification

Symbol	Function
A_0 - A_{12}	Address inputs
I/O_1 - I/O_8	Data inputs/outputs
$\overline{CE}_1$	Chip enable (active low)
CE_2	Chip enable (active high)
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 V to V_{CC} + 0.3 V
Output voltage, V_{OUT} (Note 1)	−0.5 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V min for 10 ns maximum pulse.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			6	pF
Input/output capacitance	$C_{I/O}$			8	pF

Truth Table

Function	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	X	High-Z	Standby
Not selected	X	L	X	X	High-Z	Standby
D_{OUT} disabled	L	H	H	H	High-Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V min for 10 ns maximum pulse.

19d

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Operating supply current	I_{CC}			120	mA	$\overline{CE}_1$ = V_{IL}; CE_2 = V_{IH}; $I_{I/O}$ = 0 mA (min cycle)
Standby supply current	I_{SB}			20	mA	$\overline{CE}_1$ ≥ V_{IH} or CE_2 = V_{IL}
	I_{SB1}			2	mA	$\overline{CE}_1$ ≥ V_{CC} − 0.2 V; CE_2 ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD4368-15 Min	μPD4368-15 Max	μPD4368-20 Min	μPD4368-20 Max	Unit	Test Conditions
Read Operation							
Read cycle time	t_{RC}	15		20		ns	
Address access time	t_{AA}		15		20	ns	
$\overline{CE}_1$ access time	t_{CO1}		15		20	ns	
CE_2 access time	t_{CO2}		15		20	ns	
Output enable to output valid	t_{OE}		9		10	ns	
Output hold from address change	t_{OH}	3		3		ns	
$\overline{CE}_1$ to output in low-Z	t_{LZ1}	3		3		ns	
CE_2 to output in low-Z	t_{LZ2}	3		3		ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		ns	
$\overline{CE}_1$ to output in high-Z	t_{HZ1}		8		9	ns	
CE_2 to output in high-Z	t_{HZ2}		8		9	ns	
$\overline{OE}$ to output in high-Z	t_{OHZ}		7		8	ns	
Write Operation							
Write cycle time	t_{WC}	15		20		ns	
Chip enable ($\overline{CE}_1$) to end of write	t_{CW1}	12		13		ns	
Chip enable (CE_2) to end of write	t_{CW2}	12		13		ns	
Address valid to end of write	t_{AW}	12		13		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	11		12		ns	
Write recovery time	t_{WR}	2		2		ns	
Data valid to end of write	t_{DW}	9		10		ns	
Data hold time	t_{DH}	0		0		ns	
Write enable to output in high-Z	t_{WHZ}		7		8	ns	
Output active from end of write	t_{OW}	0		0		ns	

Notes:

(1) Input pulse levels = 0.8 to 2.4 V; input pulse rise and fall times = 5 ns; timing reference level = 1.5 V; see figures 1 and 2 for output load.

Figure 1. Output Load (t_{RC}, t_{AA}, t_{CO1}, t_{CO2}, t_{OE}, t_{OH})

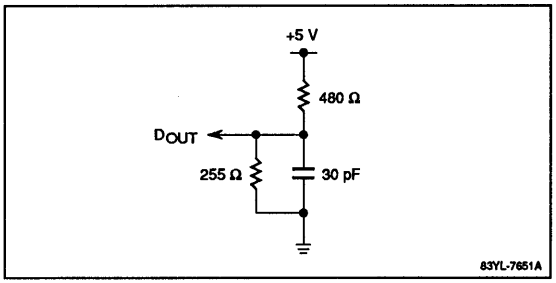
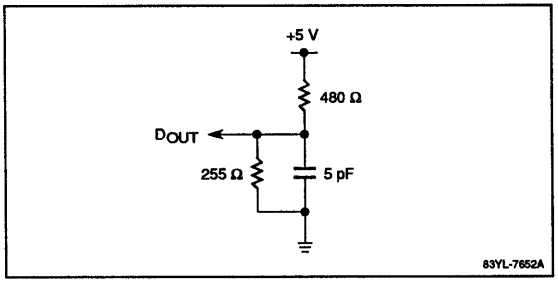
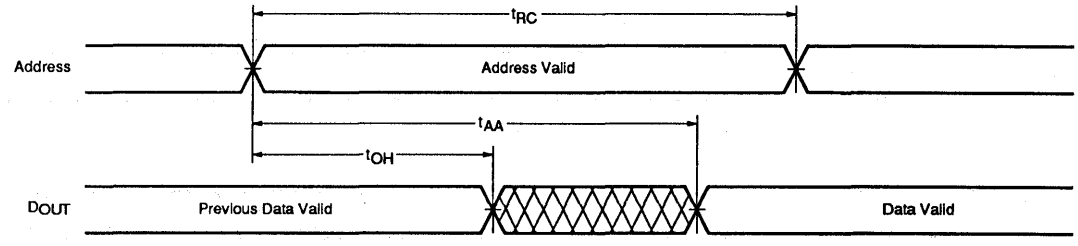


Figure 2. Output Load (t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{WHZ}, t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{OW})



Timing Waveforms

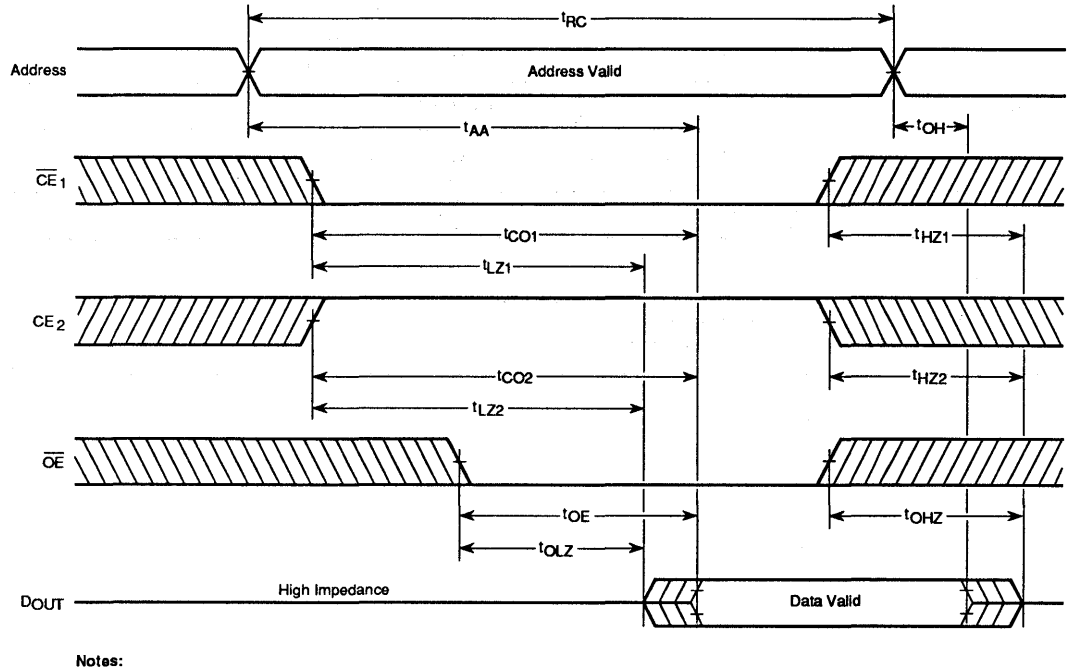
Address Access Cycle



Notes:
(1) $\overline{WE}$ is high for a read cycle.
(2) The device is continually selected, where $\overline{CE_1} = \overline{OE} = V_{IL}$ and $CE_2 = V_{IH}$.

83IH-5753B

Chip Enable Access Cycle

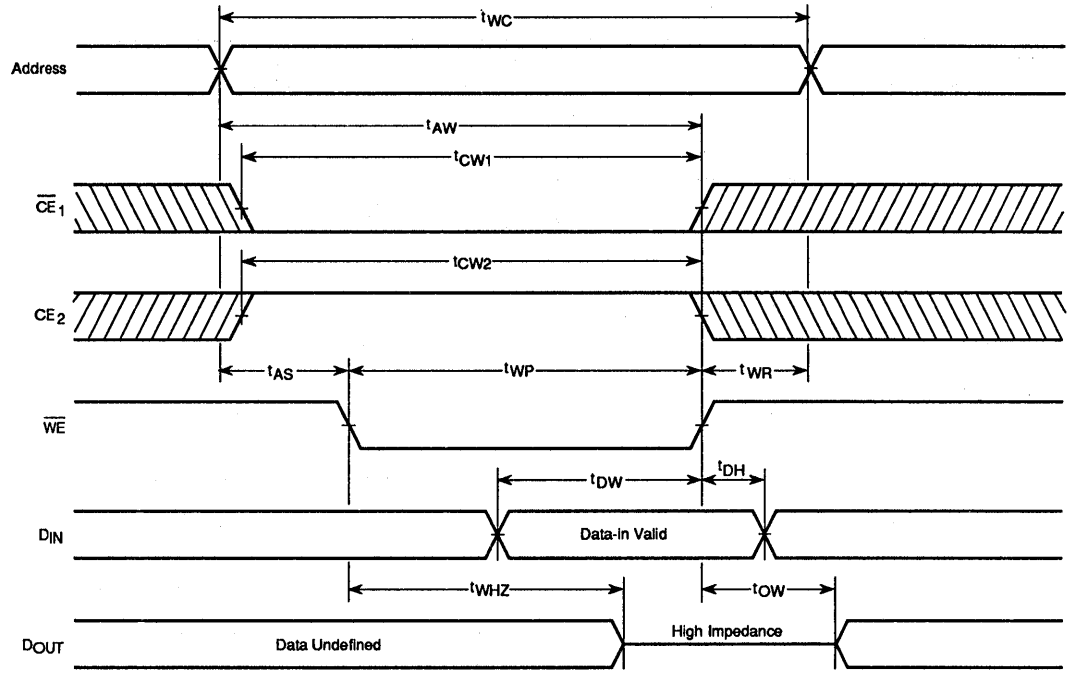


Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the latter of the low transition of $\overline{CE_1}$ or the high transition of CE_2.

83IH-5745B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

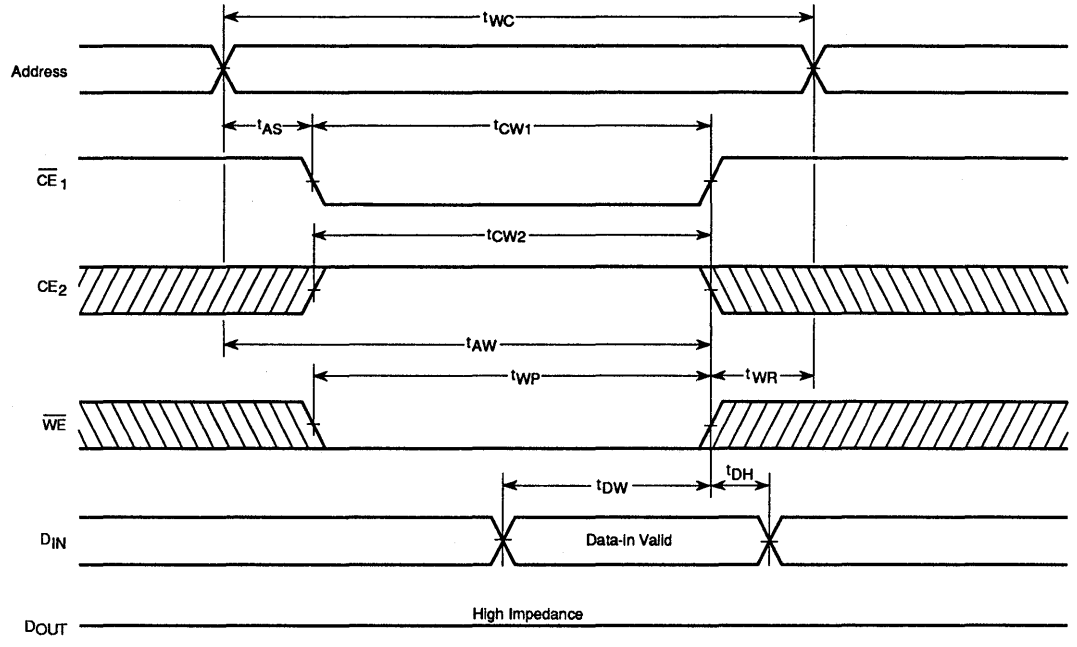
[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

83IH-6566B

Timing Waveforms (cont)

$\overline{CE_1}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE_1}$ and $\overline{WE}$ and a high CE_2.

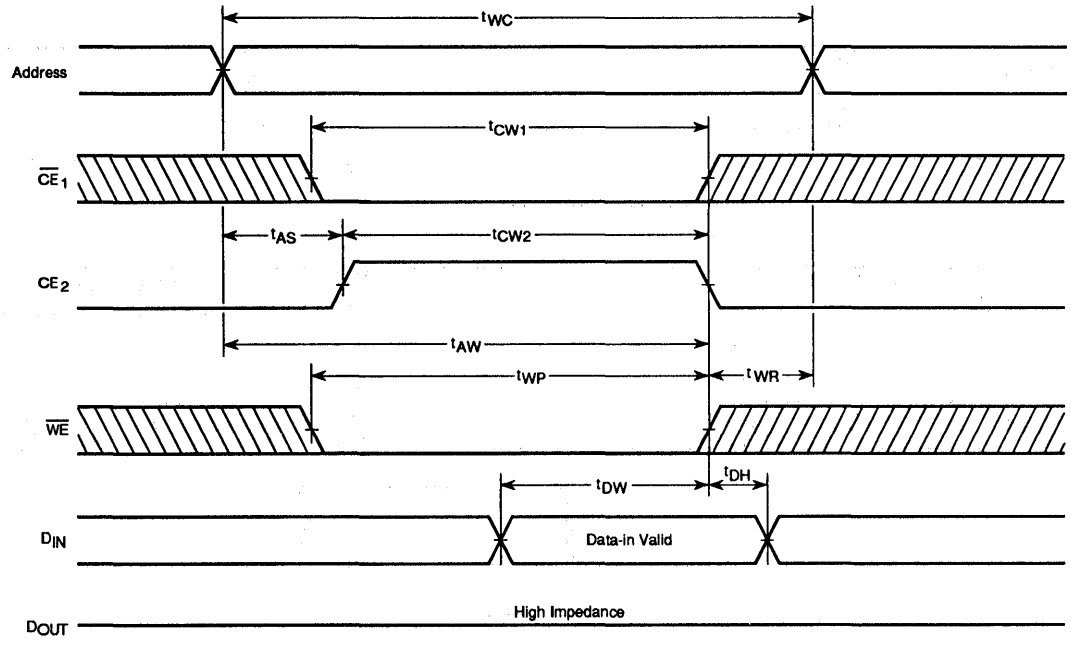
[2] $\overline{CE_1}$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

83IH-6568B

19d

Timing Waveforms (cont)

CE_2-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

83IH-6569B

Description

The μPD4369 is a high-speed 8,192-word by 9-bit static RAM fabricated with CMOS peripheral circuits and N-channel memory cells with polysilicon resistors. Two chip enable pins are provided for battery backup application, and an output enable pin is provided for easy interface.

The μPD4369 is packaged in standard 28-pin plastic DIP and 28-pin plastic SOJ packaging.

Features

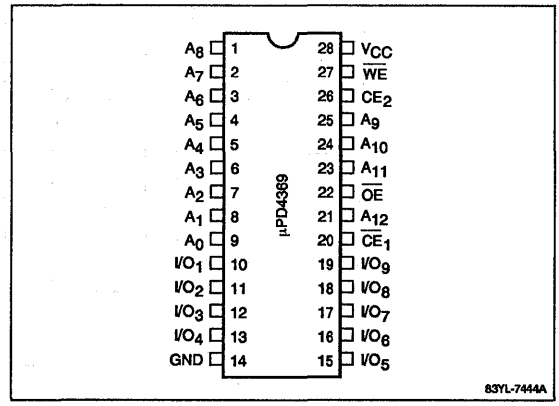
- 8,192 by 9-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{OE}$ and two $\overline{CE}$ pins for easy application
- Standard 28-pin plastic DIP and 28-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD4369CR-15	15 ns	28-pin plastic DIP
CR-20	20 ns	
μPD4369LA-15	15 ns	28-pin plastic SOJ
LA-20	20 ns	

Pin Configuration

28-Pin Plastic DIP or SOJ

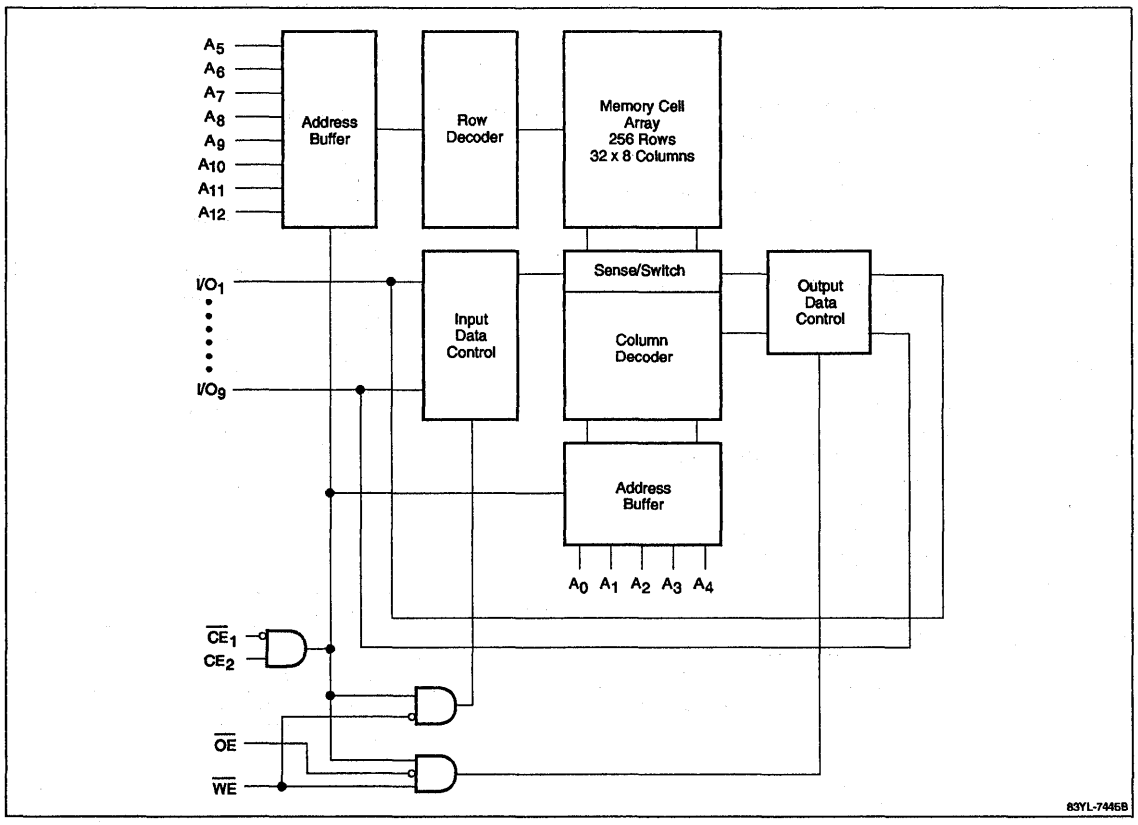


Pin Identification

Symbol	Function
A_0 - A_{12}	Address inputs
I/O_1 - I/O_9	Data inputs/outputs
$\overline{CE}_1$	Chip enable (active low)
CE_2	Chip enable (active high)
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

19e

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 V to V_{CC} + 0.3 V
Output voltage, V_{OUT} (Note 1)	−0.5 V to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V min for 10 ns maximum pulse.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			6	pF
Input/output capacitance	$C_{I/O}$			8	pF

Truth Table

Function	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	X	High-Z	Standby
Not selected	X	L	X	X	High-Z	Standby
D_{OUT} disabled	L	H	H	H	High-Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V min for 10 ns maximum pulse.

19e

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Operating supply current	I_{CCA}			120	mA	$\overline{CE}_1$ = V_{IL}; CE_2 = V_{IH}; $I_{I/O}$ = 0 mA (min cycle)
Standby supply current	I_{SB}			20	mA	$\overline{CE}_1$ ≥ V_{IH} or CE_2 = V_{IL}
	I_{SB1}			2	mA	$\overline{CE}_1$ ≥ V_{CC} − 0.2 V; CE_2 ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD4369-15 Min	μPD4369-15 Max	μPD4369-20 Min	μPD4369-20 Max	Unit	Test Conditions
Read Operation							
Read cycle time	t_{RC}	15		20		ns	
Address access time	t_{AA}		15		20	ns	
$\overline{CE}_1$ access time	t_{CO1}		15		20	ns	
CE_2 access time	t_{CO2}		15		20	ns	
Output enable to output valid	t_{OE}		9		10	ns	
Output hold from address change	t_{OH}	3		3		ns	
$\overline{CE}_1$ to output in low-Z	t_{LZ1}	3		3		ns	
CE_2 to output in low-Z	t_{LZ2}	3		3		ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		ns	
$\overline{CE}_1$ to output in high-Z	t_{HZ1}		8		9	ns	
CE_2 to output in high-Z	t_{HZ2}		8		9	ns	
OE to output in high-Z	t_{OHZ}		7		8	ns	
Write Operation							
Write cycle time	t_{WC}	15		20		ns	
Chip enable ($\overline{CE}_1$) to end of write	t_{CW1}	12		13		ns	
Chip enable (CE_2) to end of write	t_{CW2}	12		13		ns	
Address valid to end of write	t_{AW}	12		13		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	11		12		ns	
Write recovery time	t_{WR}	2		2		ns	
Data valid to end of write	t_{DW}	9		10		ns	
Data hold time	t_{DH}	0		0		ns	
Write enable to output in high-Z	t_{WHZ}		7		8	ns	
Output active from end of write	t_{OW}	0		0		ns	

Notes:

(1) Input pulse levels = 0.8 to 2.4 V; input pulse rise and fall times = 5 ns; see figures 1 and 2 for output load circuit.

Figure 1. Output Load (t_{RC}, t_{AA}, t_{CO1}, t_{CO2}, t_{OE}, t_{OH})

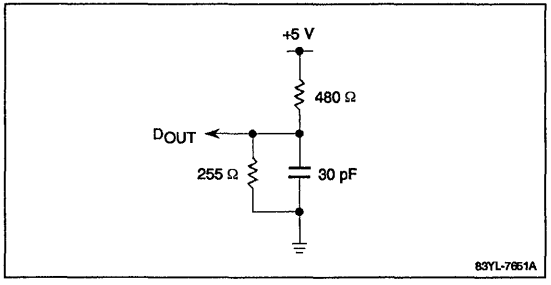
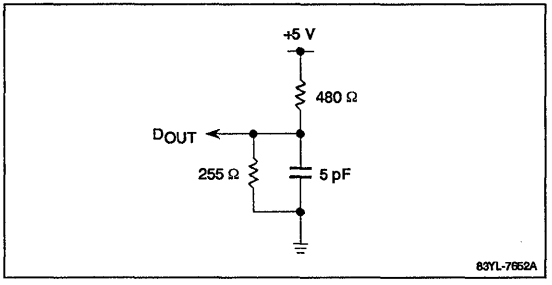
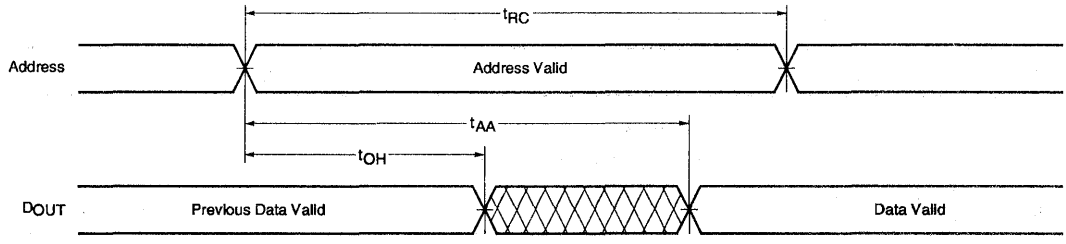


Figure 2. Output Load (t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{WHZ}, t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{OW})



Timing Waveforms

Address Access Cycle

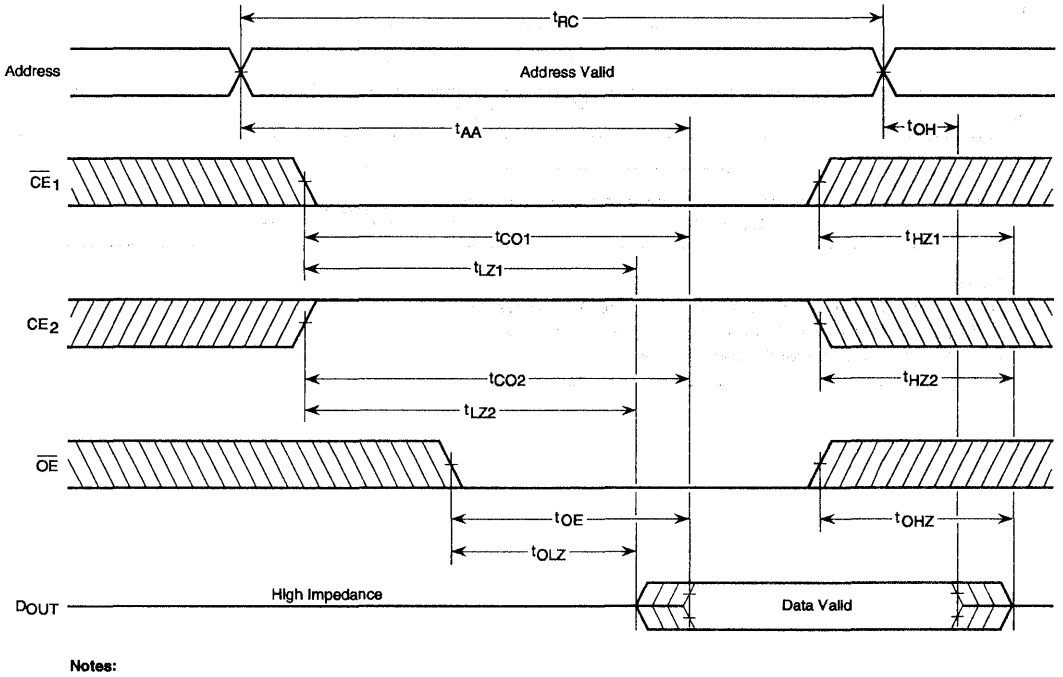


Notes:
(1) $\overline{WE}$ is high for a read cycle.
(2) The device is continually selected, where $\overline{CE}_1 = \overline{OE} = V_{IL}$ and $CE_2 = V_{IH}$.

83IH-5753B

19e

Chip Enable Access Cycle

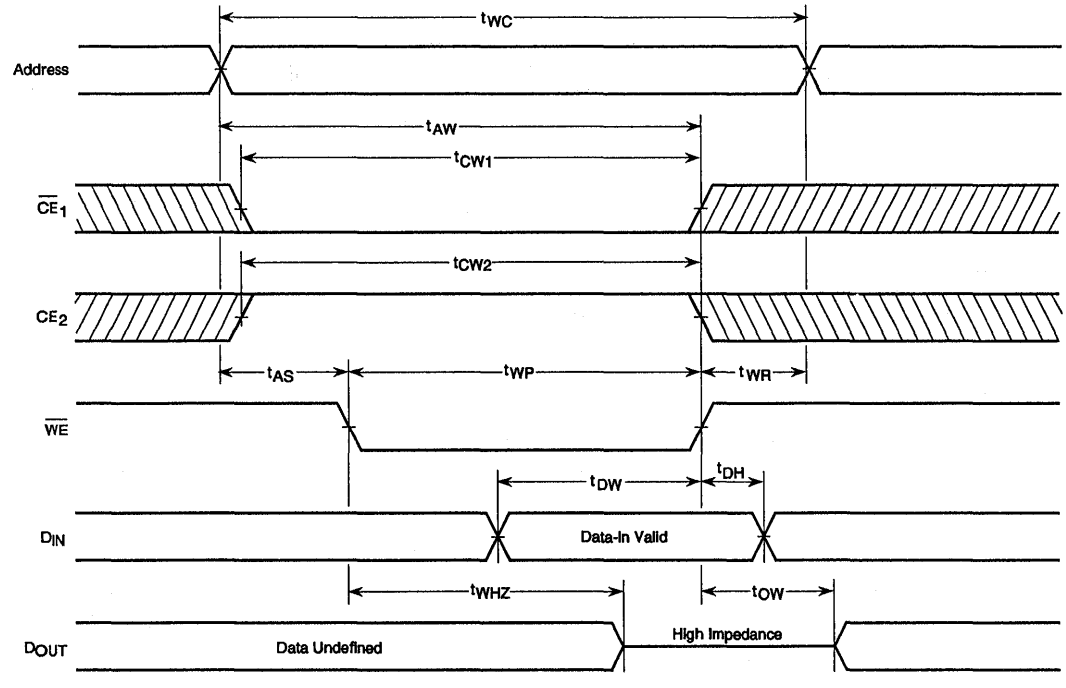


Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the latter of the low transition of $\overline{CE}_1$ or the high transition of CE_2.

83IH-6746B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE_1}$ and $\overline{WE}$ and a high CE_2.

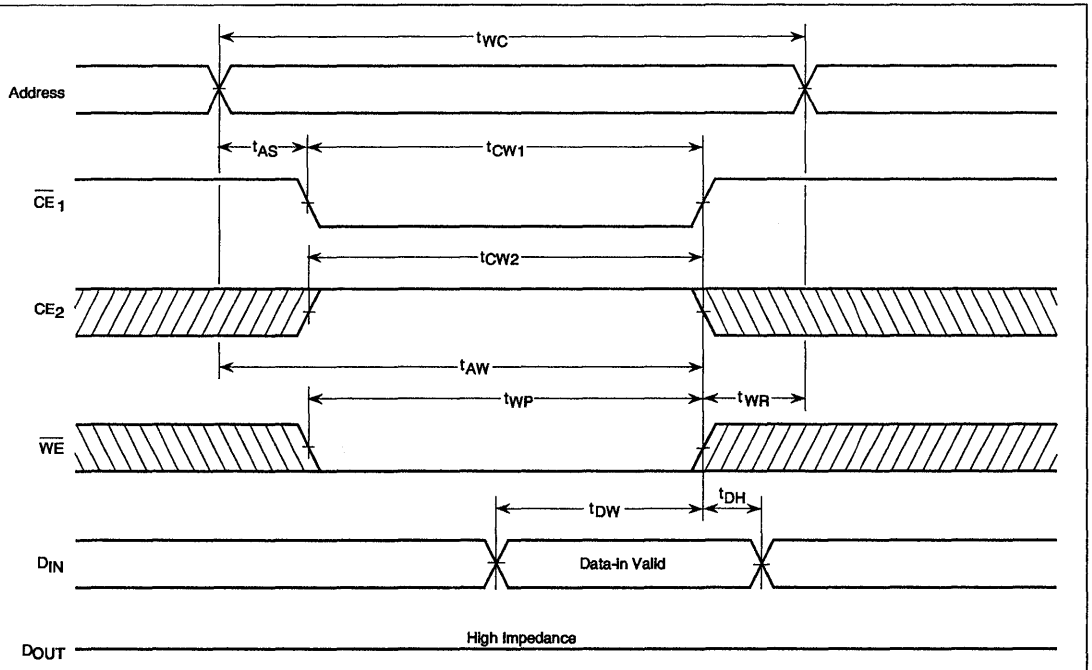
[2] $\overline{CE_1}$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

83IH-8566B

Timing Waveforms (cont)

$\overline{CE_1}$-Controlled Write Cycle



Notes:

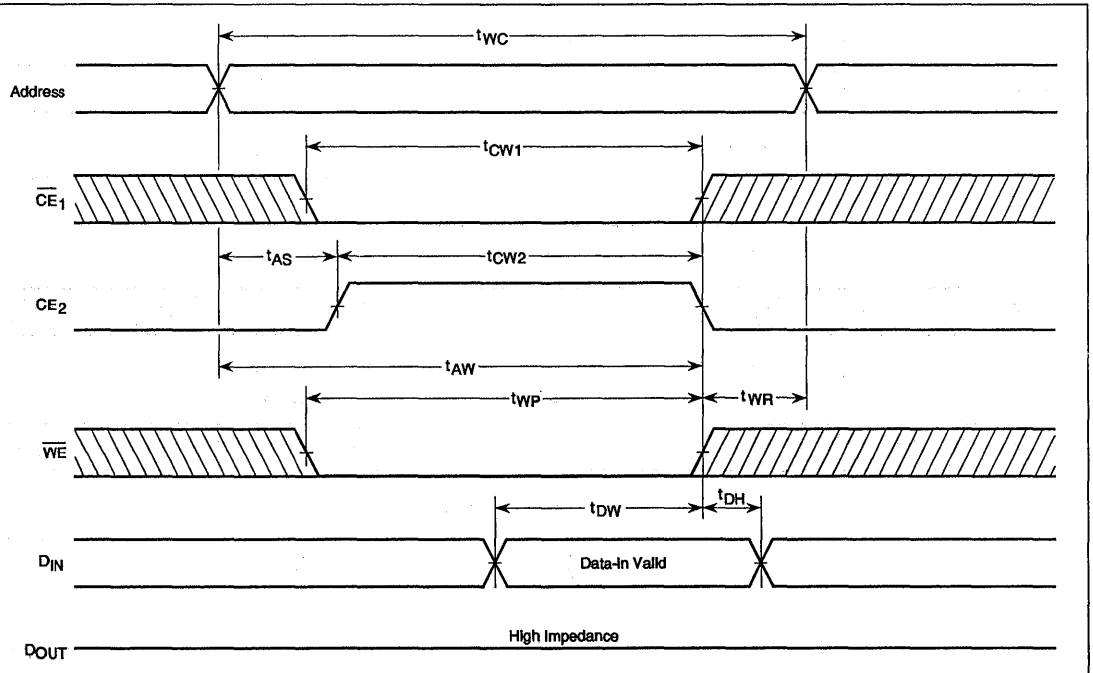
[1] A write cycle occurs during the overlap of a low $\overline{CE_1}$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE_1}$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

83IH-6568B

Timing Waveforms (cont)

CE_2-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE_1}$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE_1}$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

83IH-6669B

NEC

Section 20
Fast Static RAMs (256K)

μPD	Organization	Features	
43251B	256K x 1	15-ns	20a
43253B	64K x 4	15-ns; Output enable	20b
43254B	64K x 4	15-ns	20c
43258A	32K x 8	15-ns; Output enable	20d
43259A	32K x 9	15-ns; Output enable	20e

Upcoming Products

Description	Device Number	Comments
32K x 8	μPD46258	Speeds to 6 ns; 3.3- and 5-V versions
32K x 9	μPD46259	Speeds to 6 ns; 3.3- and 5-V versions

μPD43251B
262,144 x 1-Bit
Static CMOS RAM

Description

The μPD43251B is a 262,144-word by 1-bit static RAM fabricated with advanced silicon-gate technology. A unique design that uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD43251B a high-speed device that requires no clock or refreshing.

The μPD43251B is available in 24-pin plastic DIP or 24-pin plastic SOJ packaging.

Features

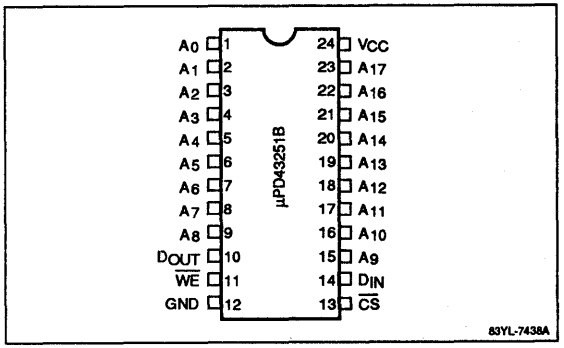
- 262,144-word x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Power dissipation
  - —120 mA max (active)
  - —2 mA max (standby)
- Standard 300-mil, 24-pin plastic DIP or 24-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD43251BCR-15	15 ns	24-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μPD43251BLA-15	15 ns	24-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configuration

24-Pin Plastic DIP or SOJ



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

20a

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to +V_{CC} + 0.3
Output voltage, V_{OUT}	−0.5 to +V_{CC} + 0.3
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V min for 10 ns maximum pulse.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	D_{OUT}	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	Output data	Active
Write	L	L	High-Z	Active

Capacitance

T_A = +25°C; f = 1 MHz (Note 1); V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Output capacitance	C_O			8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

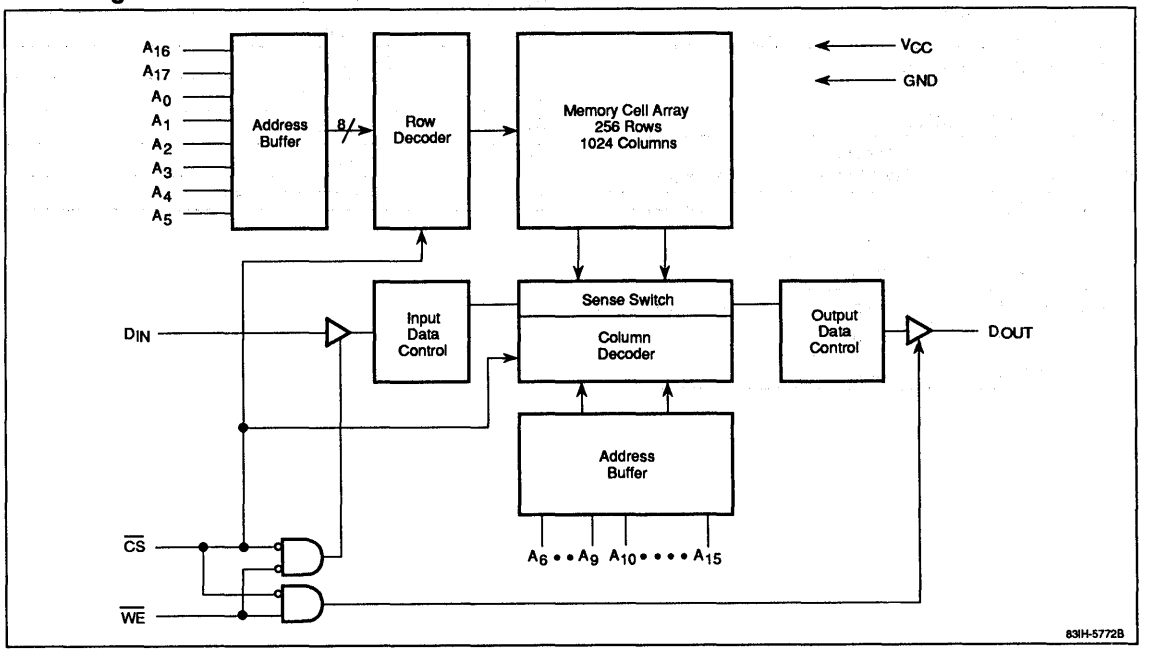
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V min for 10 ns maximum pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD43251B-15		μPD43251B-20		μPD43251B-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions (Note 1)
Read Operation									
Operating supply current	I_{CC}		120		100		100	mA	$\overline{CS}$ = V_{IL} (min cycle); I_{OUT} = 0 mA
Read cycle time	t_{RC}	15		20		25		ns	(Note 2)
Read access time	t_{AA}		15		20		25	ns	
Chip select access time	t_{ACS}		15		20		25	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
Chip select to output in low-Z	t_{CLZ}	3		3		3		ns	(Note 3)
Chip deselect to output in high-Z	t_{CHZ}	0	6	0	8	0	10	ns	(Note 4)
Write Operation									
Write cycle time	t_{WC}	15		20		25		ns	(Note 2)
Chip select to end of write	t_{CW}	13		15		20		ns	
Address valid to end of write	t_{AW}	13		15		20		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	12		14		18		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	10		12		14		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	6	0	8	0	10	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 5 ns; timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the loading shown in figure 2.

(4) The transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the loading shown in figure 2.

Figure 1. Output Load

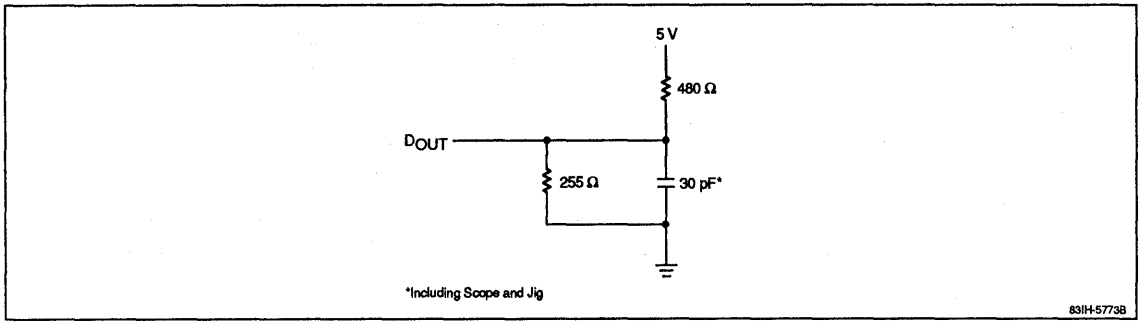
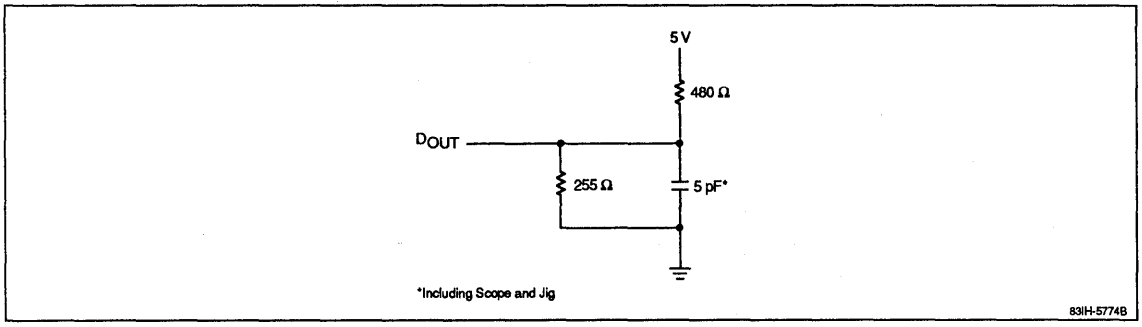
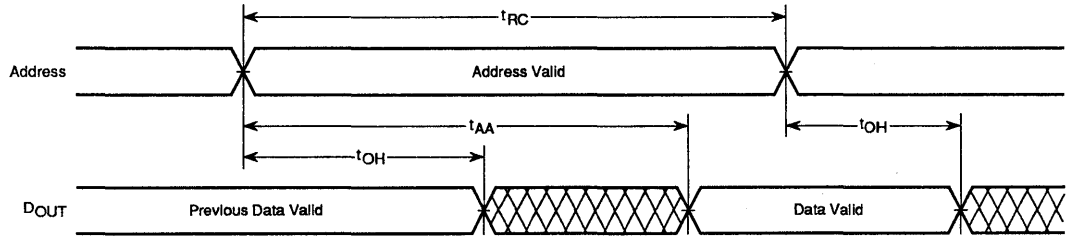


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{OW}, and t_{WHZ}



Timing Waveforms

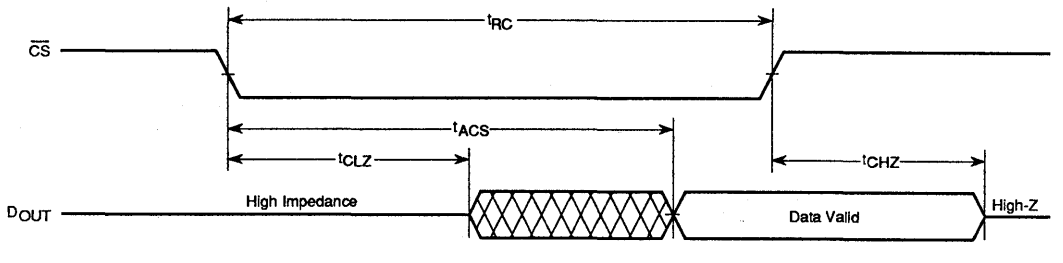
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle



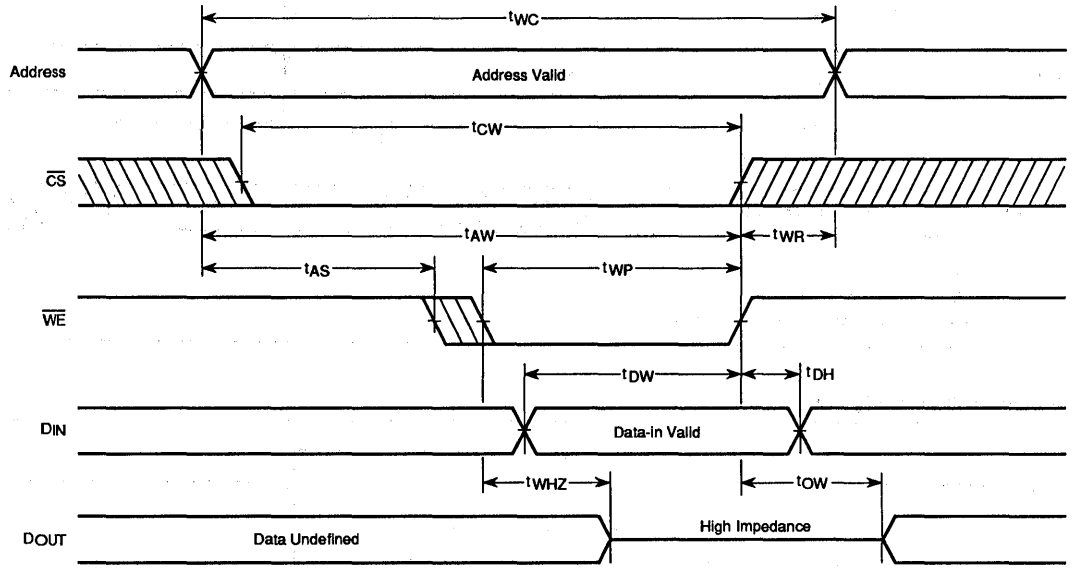
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-5776B

20a

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

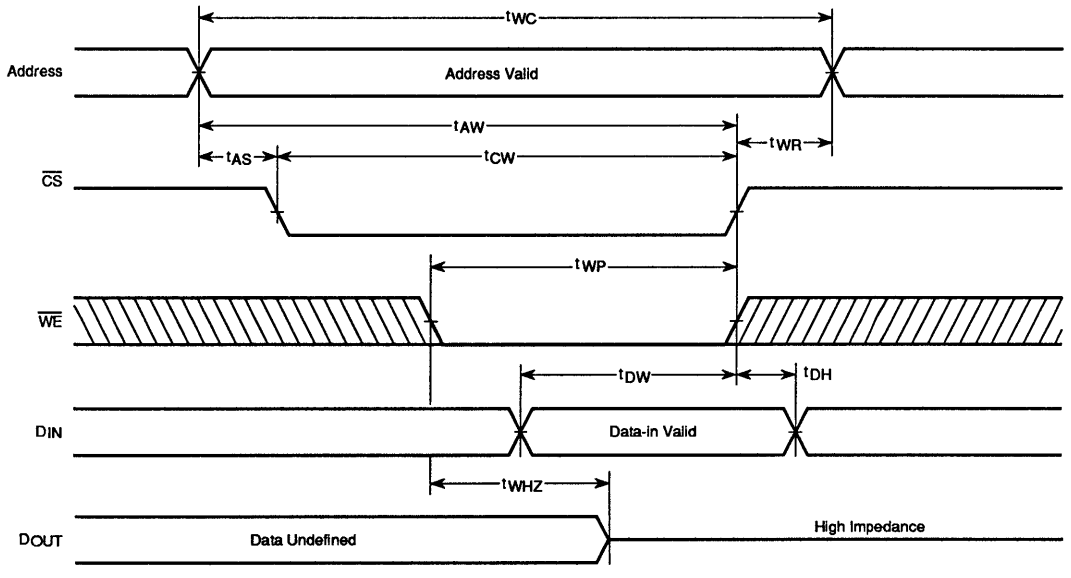
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5777B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5778B

20a

μPD43253B
65,536 x 4-Bit
Static CMOS RAM

Description

The μPD43253B is a 65,536-word by 4-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD43253B a high-speed device that requires very low power and no clock or refreshing.

The μPD43253B is available in standard 28-pin plastic DIP and SOJ packaging.

Features

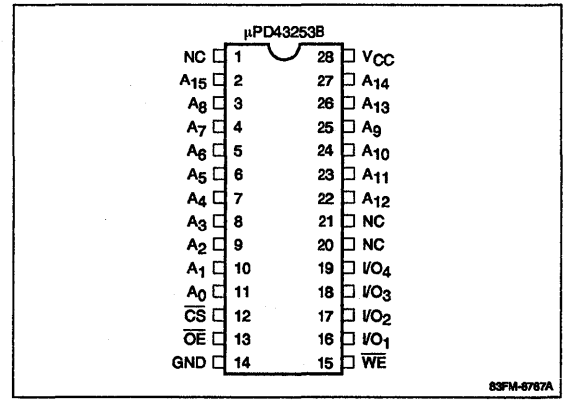
- 65,536-word x 4-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Output enable ($\overline{OE}$) control
- Low power dissipation
  - 140 mA max (active)
  - 2 mA max (standby)
- Standard 28-pin, 300-mil plastic DIP and SOJ packages

Ordering Information

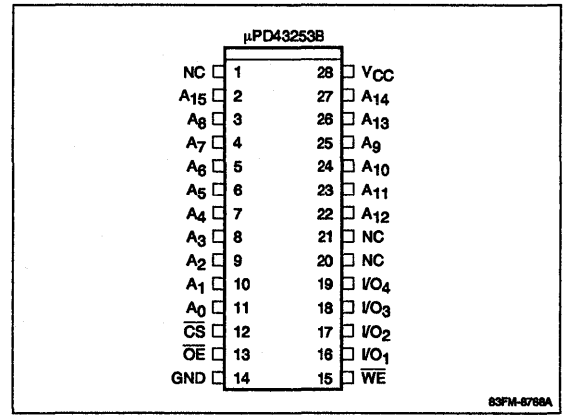
Part Number	Access Time (max)	Package
μPD43253BCR-15	15 ns	28-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μPD43253BLA-15	15 ns	28-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configurations

28-Pin Plastic DIP



28-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} (min) = −3.0 V for 10-ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		8	pF

Capacitance is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

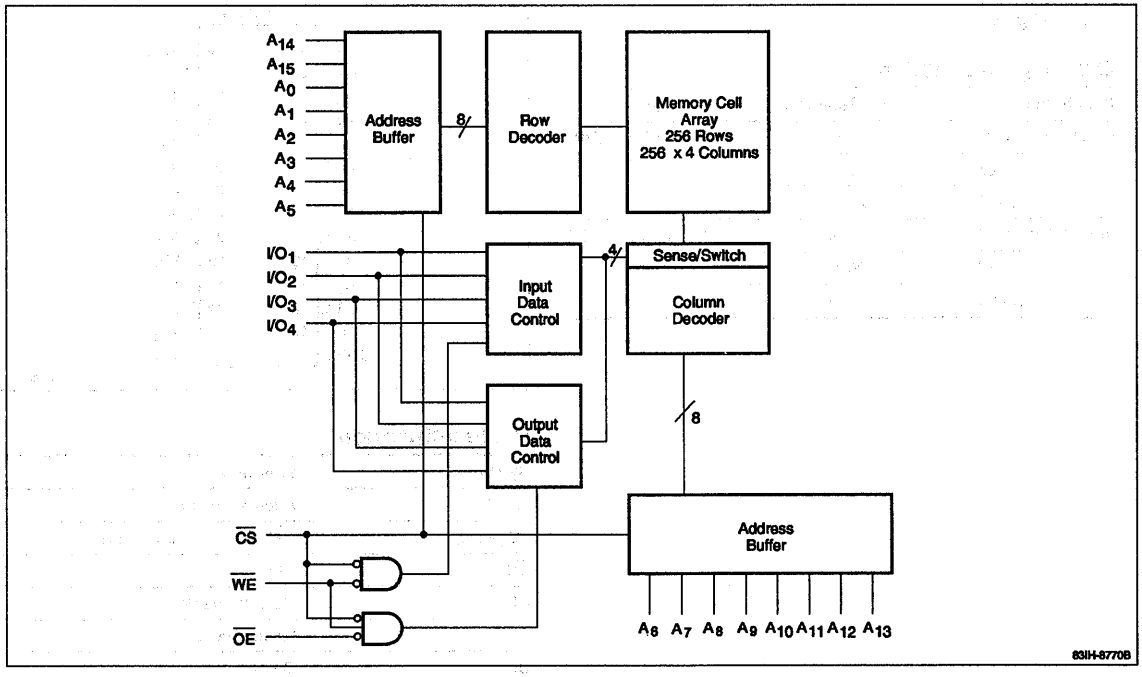
(1) V_{IL} = −3.0 V for 20-ns pulse.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	Output	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Output disable		Active
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	

X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD43253B-15		μPD43253B-20		μPD43253B-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		140		120		120	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Address access time	t_{AA}		15		20		25	ns	
Chip select access time	t_{ACS}		15		20		25	ns	
Chip deselection to output in high-Z	t_{CHZ}	0	6	0	8	0	10	ns	(Note 4)
Chip selection to output in low-Z	t_{CLZ}	3		3		3		ns	(Note 3)
Output enable access time	t_{OE}		8		10		12	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
Output enable to output in high-Z	t_{OHZ}		6		8		10	ns	
Output enable to output in low-Z	t_{OLZ}	0		0		0		ns	
Read cycle time	t_{RC}	15		20		25		ns	(Note 2)
Write Operation									
Address setup time	t_{AS}	0		0		0		ns	
Address valid to end of write	t_{AW}	13		15		20		ns	
Chip select to end of write	t_{CW}	13		15		20		ns	
Data hold time	t_{DH}	0		0		0		ns	
Data valid to end of write	t_{DW}	10		12		14		ns	
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)
Write cycle time	t_{WC}	15		20		25		ns	
Write enable to output in high-Z	t_{WHZ}	0	6	0	8	0	10	ns	(Note 4)
Write pulse width	t_{WP}	12		14		18		ns	
Write recovery time	t_{WR}	0		0		0		ns	

Notes:

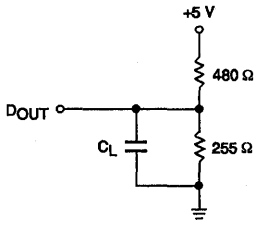
(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figure 1 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 1.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 1.

Figure 1. Output Loads

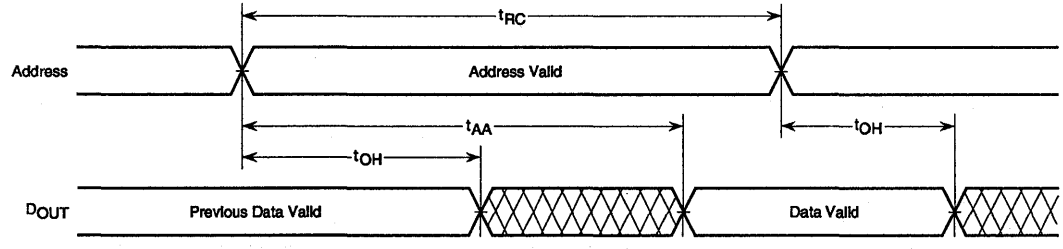


C_L = 30 pF (Including scope and test jig)
C_L = 5 pF for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}

83FM-8642A

Timing Waveforms

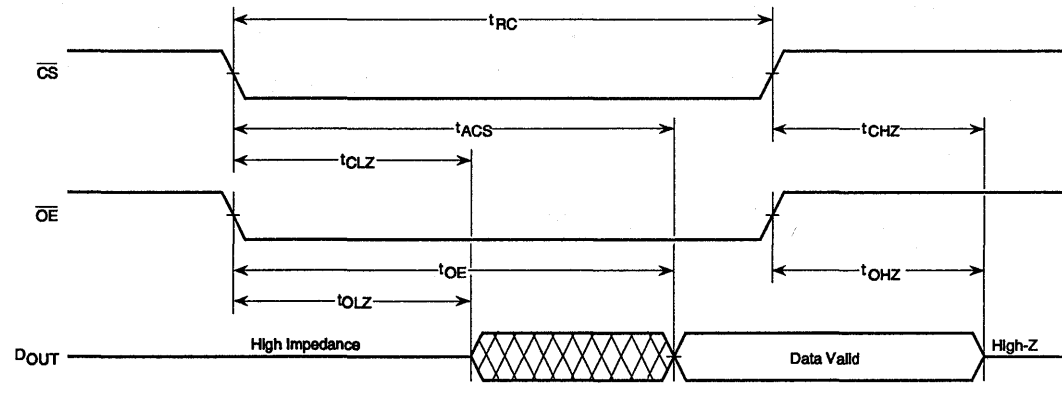
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-6776B

Chip Select Access Cycle



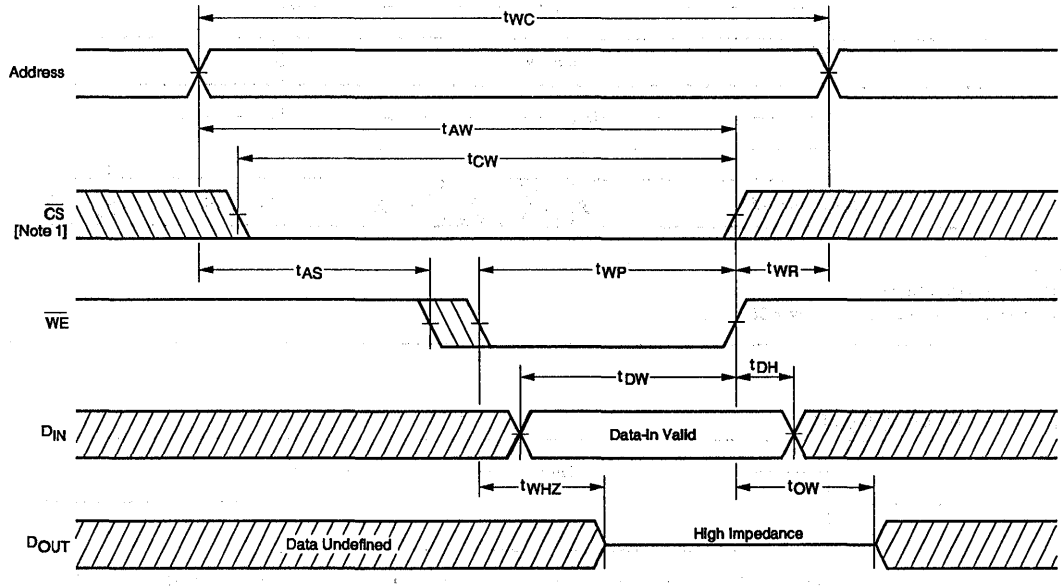
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Device is continuously selected: $\overline{CS} = \overline{OE}$ = Low
[3] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-8769B

20b

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

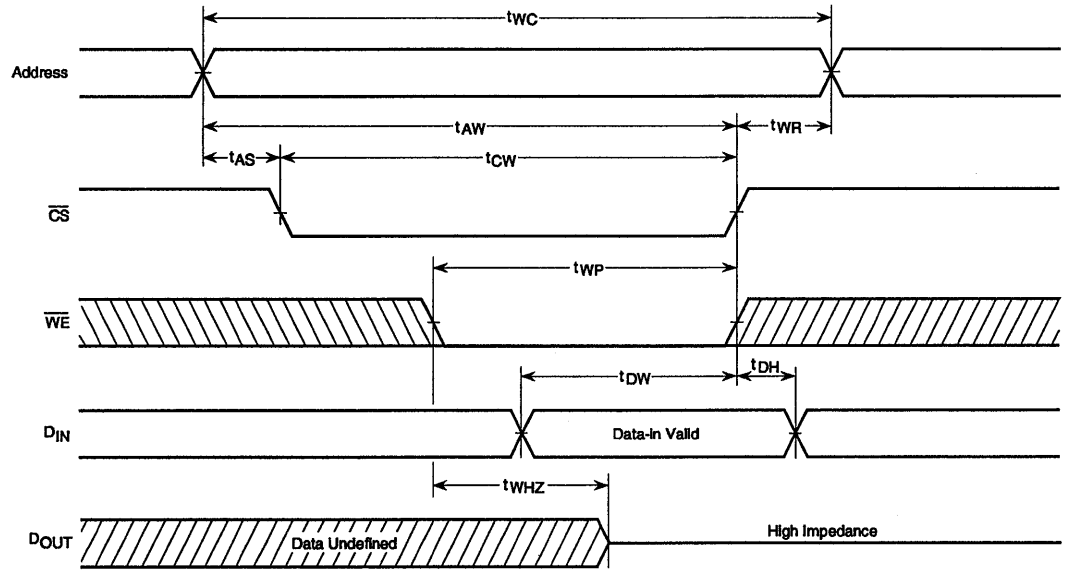
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and the end of t_{WC}.

83IH-6773B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
[3] t_{WR} is measured between the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and the end of t_{WC}.

83IH-6774B

20b

μPD43254B
65,536 x 4-Bit
Static CMOS RAM

Description

The μPD43254B is a 65,536-word by 4-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD43254B a high-speed device that requires very low power and no clock or refreshing.

The μPD43254B is available in standard 24-pin plastic DIP and SOJ packaging.

Features

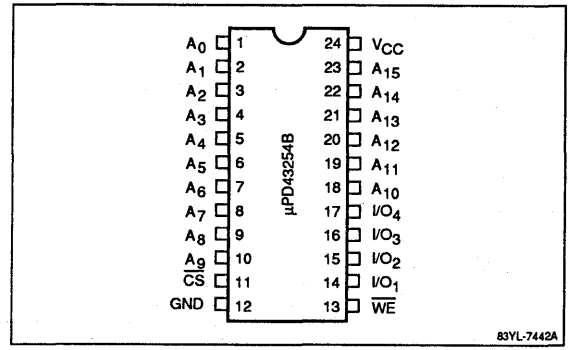
- 65,536-word x 4-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Low power dissipation
  - —140 mA max (active)
  - —2 mA max (standby)
- Standard 24-pin plastic DIP and SOJ packaging

Ordering Information

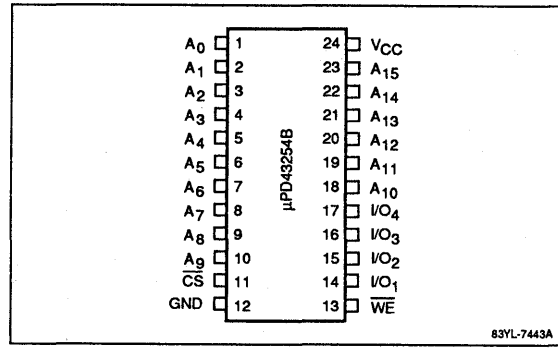
Part Number	Access Time (max)	Package
μPD43254BCR-15	15 ns	24-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μPD43254BLA-15	15 ns	24-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configurations

24-Pin Plastic DIP



24-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{15}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} (min) = −3.0 V for 10 ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz (Note 1)

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V for 20 ns pulse.

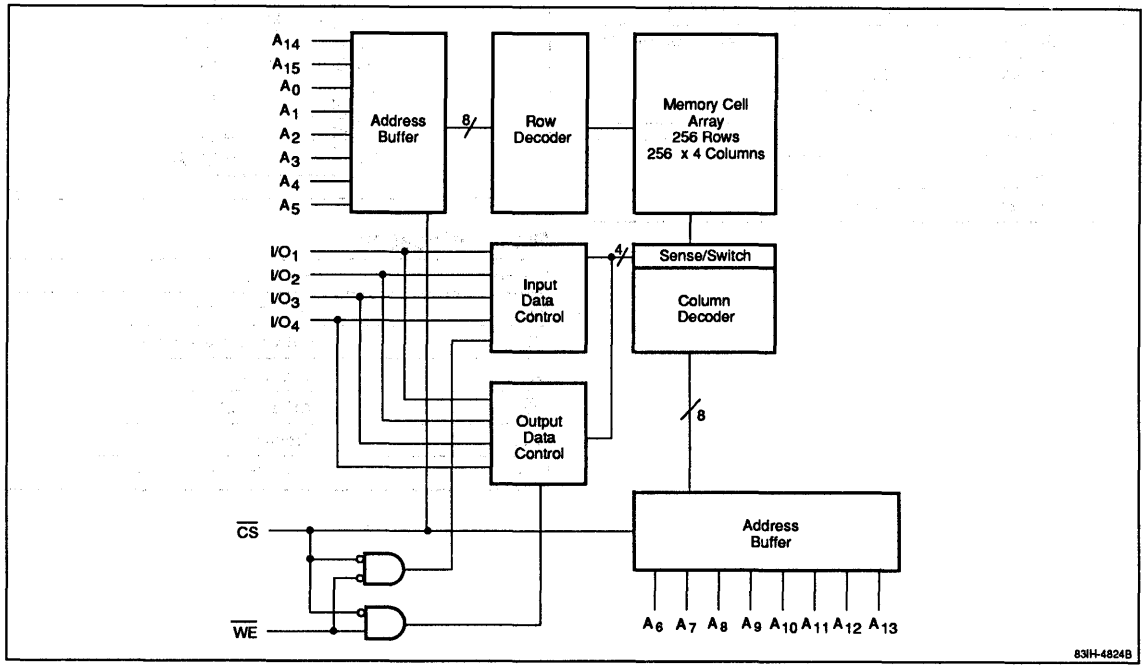
Truth Table

Function	$\overline{CS}$	$\overline{WE}$	Input/Output	I_{CC}
Not selected	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD43254B-15		μPD43254B-20		μPD43254B-25			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		140		120		120	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA
Read cycle time	t_{RC}	15		20		25		ns	(Note 2)
Address access time	t_{AA}		15		20		25	ns	
Chip select access time	t_{ACS}		15		20		25	ns	
Output hold from address change	t_{OH}	3		3		3		ns	
Chip selection to output in low-Z	t_{CLZ}	3		3		3		ns	(Note 3)
Chip deselection to output in high-Z	t_{CHZ}	0	6	0	8	0	10	ns	(Note 4)
Write Operation									
Write cycle time	t_{WC}	15		20		25		ns	(Note 2)
Chip select to end of write	t_{CW}	13		15		20		ns	
Address valid to end of write	t_{AW}	13		15		20		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	12		14		18		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	10		12		14		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	6	0	8	0	10	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 2.

Figure 1. Output Load

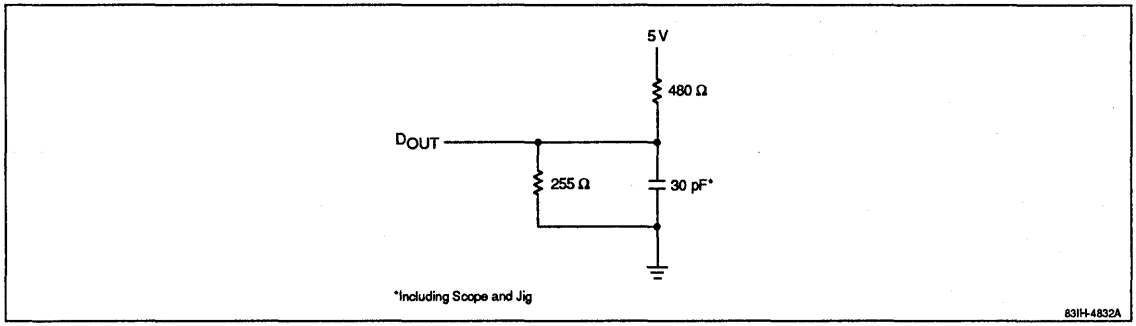
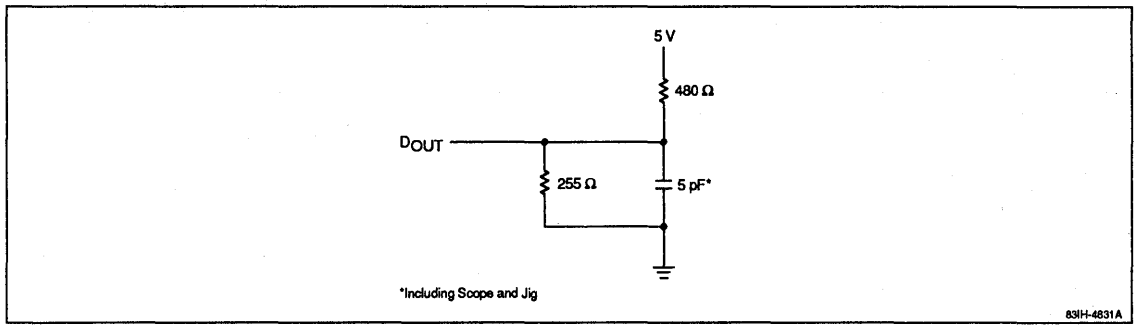
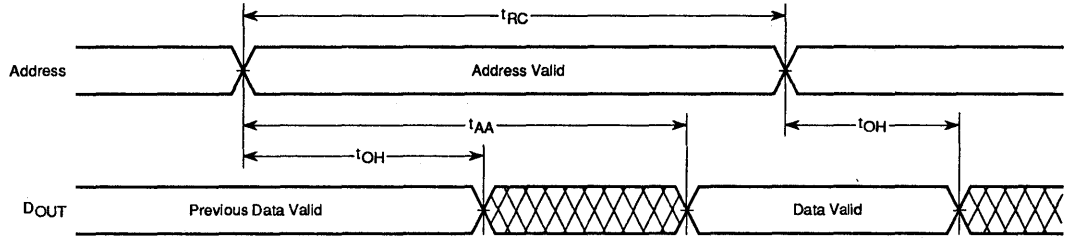


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

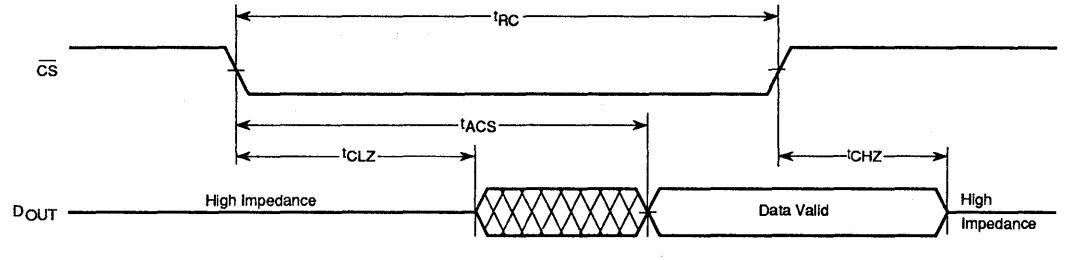
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle



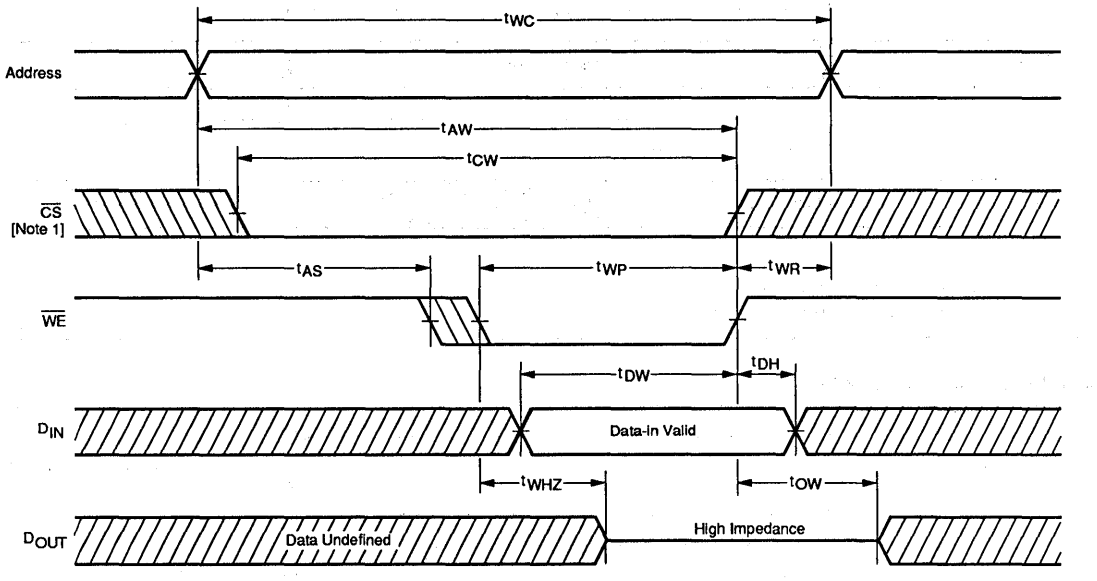
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6772B

20c

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

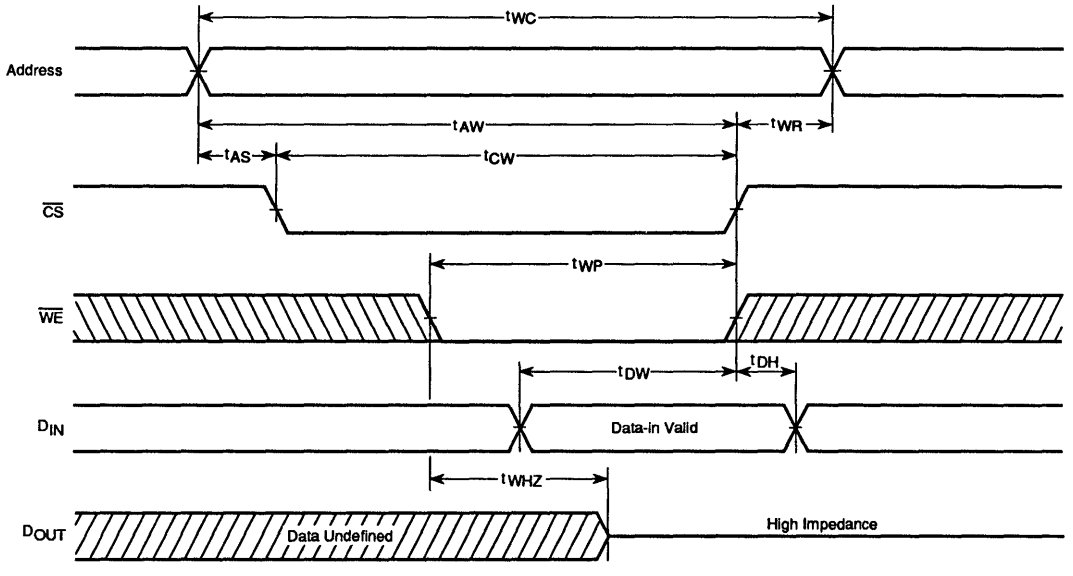
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and the end of t_{WC}.

83IH-6773B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first, and the end of t_{WC}.

83IH-6774B

20c

μPD43258A
32,768 x 8-Bit
Static CMOS RAM

Description

The μPD43258A is a 32,768-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors to make the μPD43258A a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when $\overline{CS}$ is high, independent of the other inputs' levels. The μPD43258A is available in standard 28-pin plastic DIP or SOJ packaging.

Features

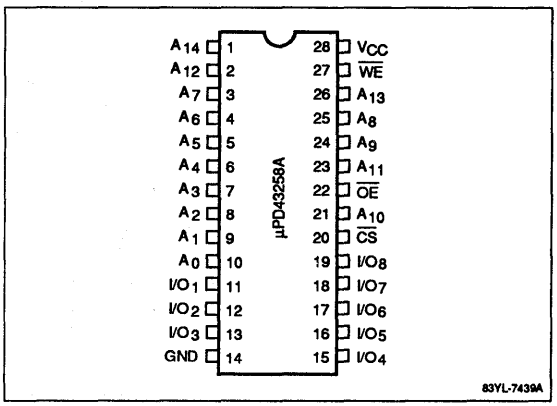
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Standard 28-pin plastic DIP and SOJ packaging
- Fast access time of 15 ns (max)

Ordering Information

Part Number	Access Time (max)	Package
μPD43258ACR-15	15 ns	28-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μPD43258ALA-15	15 ns	28-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configurations

28-Pin Plastic DIP or SOJ

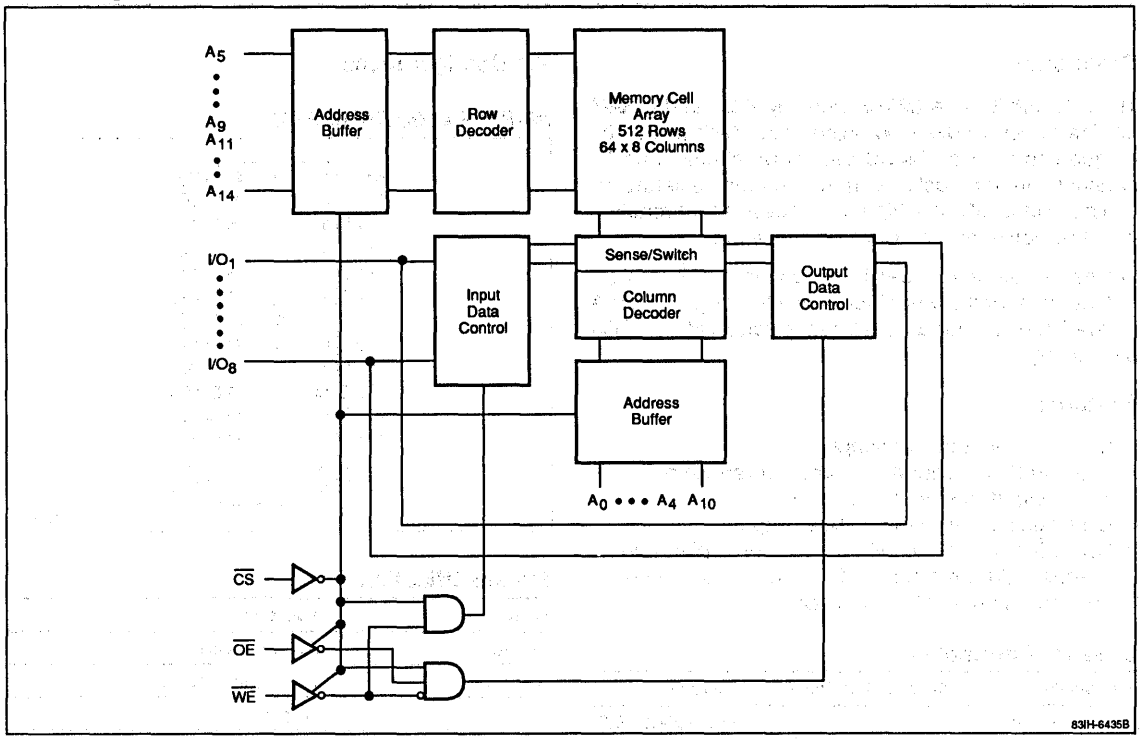


Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

20d

Block Diagram



Truth Table

Function	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	High-Z	Standby
Outputs disabled	L	H	H	High-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active

Notes:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 10 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−2		2	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Standby supply current	I_{SB}			30	ma	$\overline{CS} \geq V_{IH}$; $V_{IN} = V_{IH}$ or V_{IL}
	I_{SB1}			2	mA	$\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \leq 0.2$ V or $\geq V_{CC} - 0.2$ V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 10 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		6	pF
Input/output capacitance	$C_{I/O}$		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD43258A-15		μPD43258A-20		μPD43258A-25			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Operating supply current	I_{CC}		150		140		130	mA	$\overline{CS} \le V_{IL}$ (min cycle); $I_{I/O}$ = 0 mA
Read cycle time	t_{RC}	15		20		25		ns	(Note 2)
Address access time	t_{AA}		15		20		25	ns	(Note 2)
Chip select access time	t_{ACS}		15		20		25	ns	(Note 2)
Output enable to output valid	t_{OE}		9		10		12	ns	(Note 2)
Output hold from address change	t_{OH}	3		3		3		ns	(Note 2)
Chip select to output in low-Z	t_{CLZ}	3		3		3		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	0		0		0		ns	(Note 3)
Chip select to output in high-Z	t_{CHZ}		10		10		10	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		8		8		10	ns	(Note 3)
Write Operation									
Write cycle time	t_{WC}	15		20		25		ns	
Chip select to end of write	t_{CW}	12		13		15		ns	
Address valid to end of write	t_{AW}	12		13		15		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	12		13		15		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	9		10		12		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		8		8		10	ns	(Note 3)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = 0 to 3 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output load.

(3) See figure 2 for output load.

Figure 1. Output Load

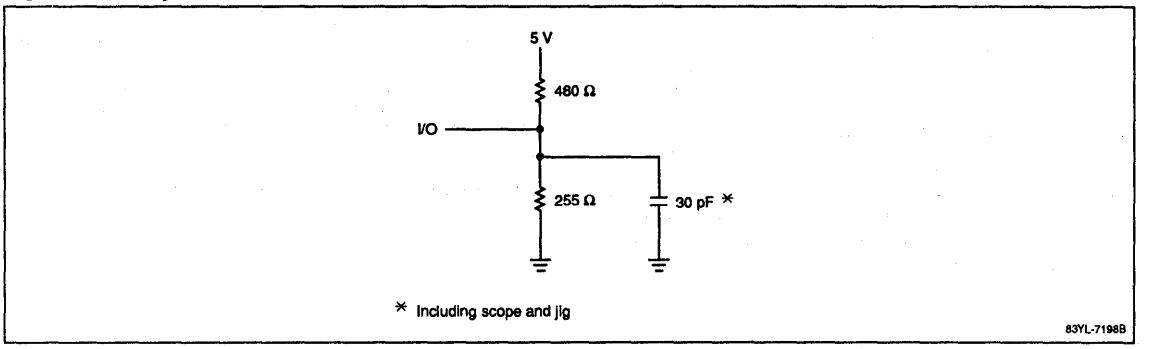
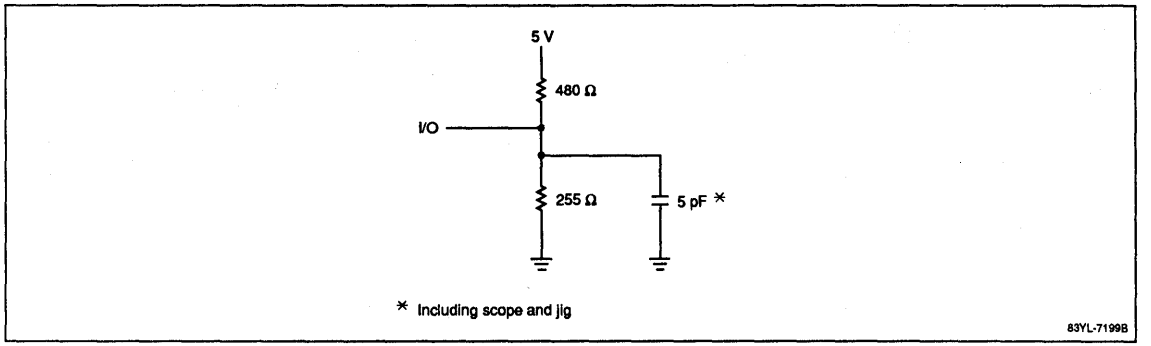
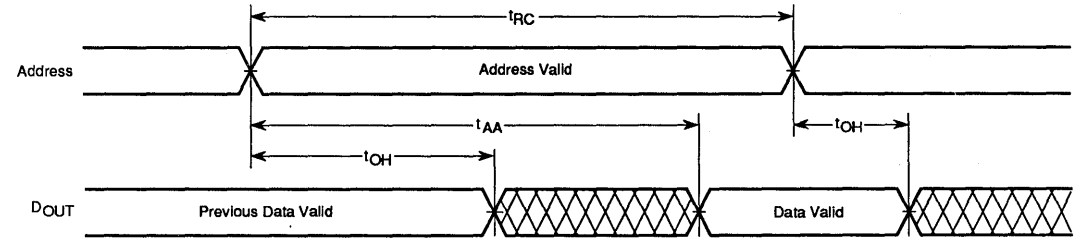


Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

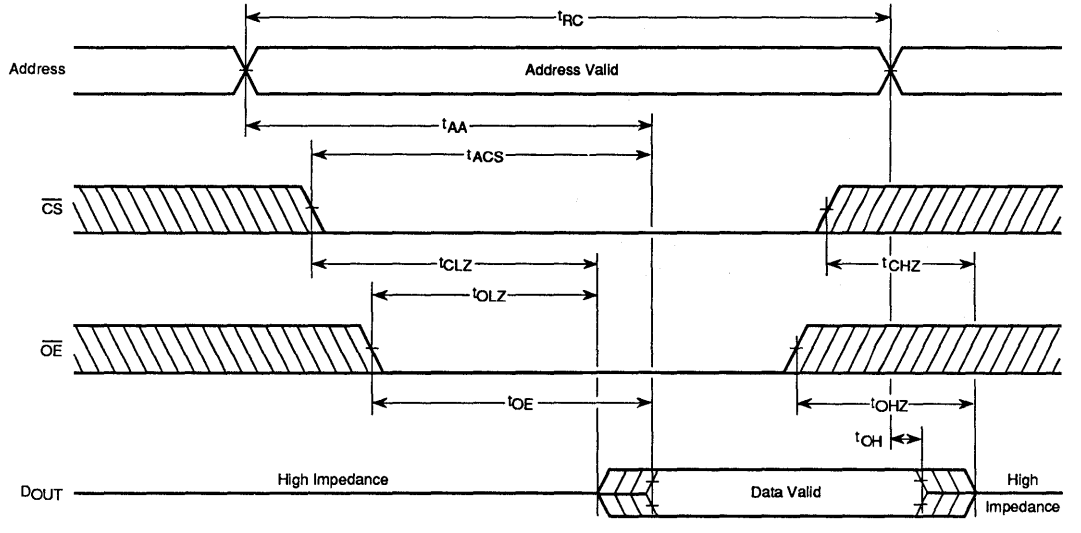
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6436B

Chip Select Access Cycle



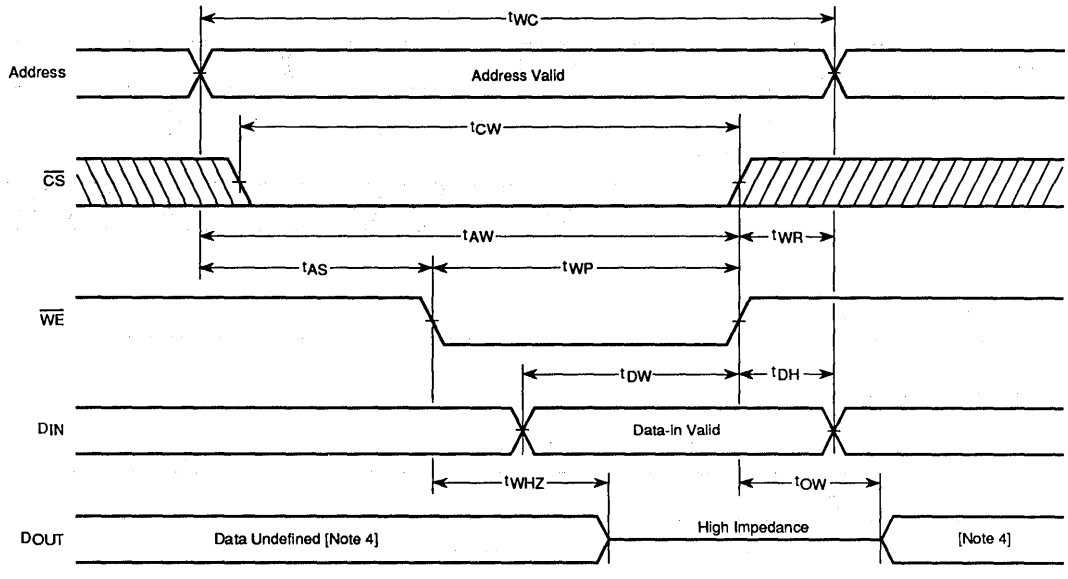
Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6437B

20d

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

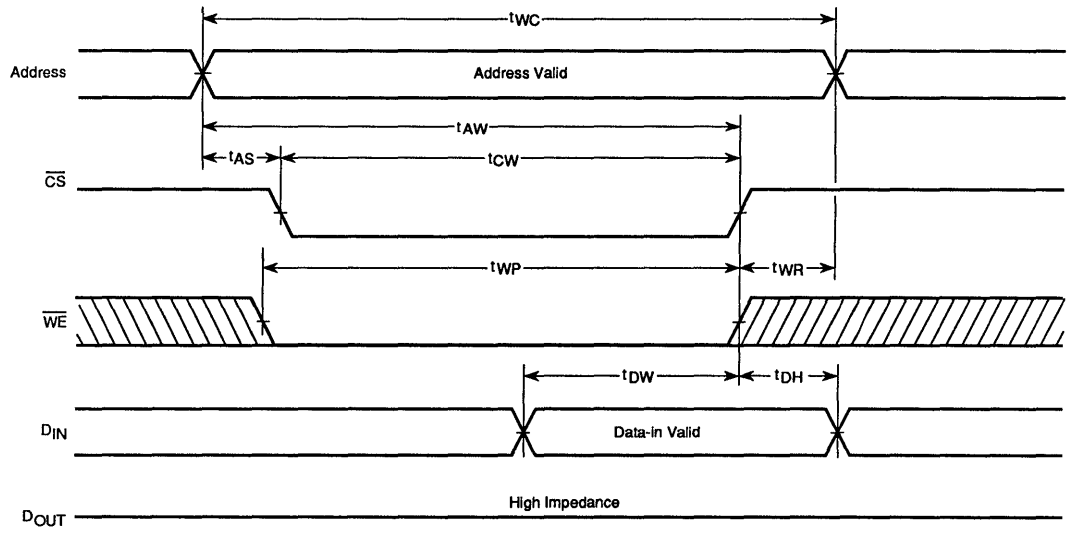
[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

[4] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

83IH-6438B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

83IH-6439B

20d

μPD43259A
32,768 x 9-Bit
Static CMOS RAM

Description

The μPD43259A is a 32,768-word by 9-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors to make the μPD43259A a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when $\overline{CS}$ is high, independent of the other inputs' levels. The μPD43259A is available in standard 32-pin plastic DIP or SOJ packaging.

Features

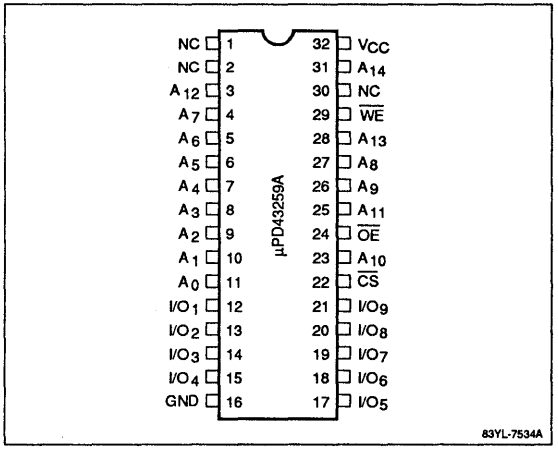
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Standard 32-pin plastic DIP and SOJ packaging
- Fast access time of 15 ns (max)

Ordering Information

Part Number	Access Time (max)	Package
μPD43259ACR-15	15 ns	32-pin plastic DIP
CR-20	20 ns	
CR-25	25 ns	
μPD43259ALA-15	15 ns	32-pin plastic SOJ
LA-20	20 ns	
LA-25	25 ns	

Pin Configuration

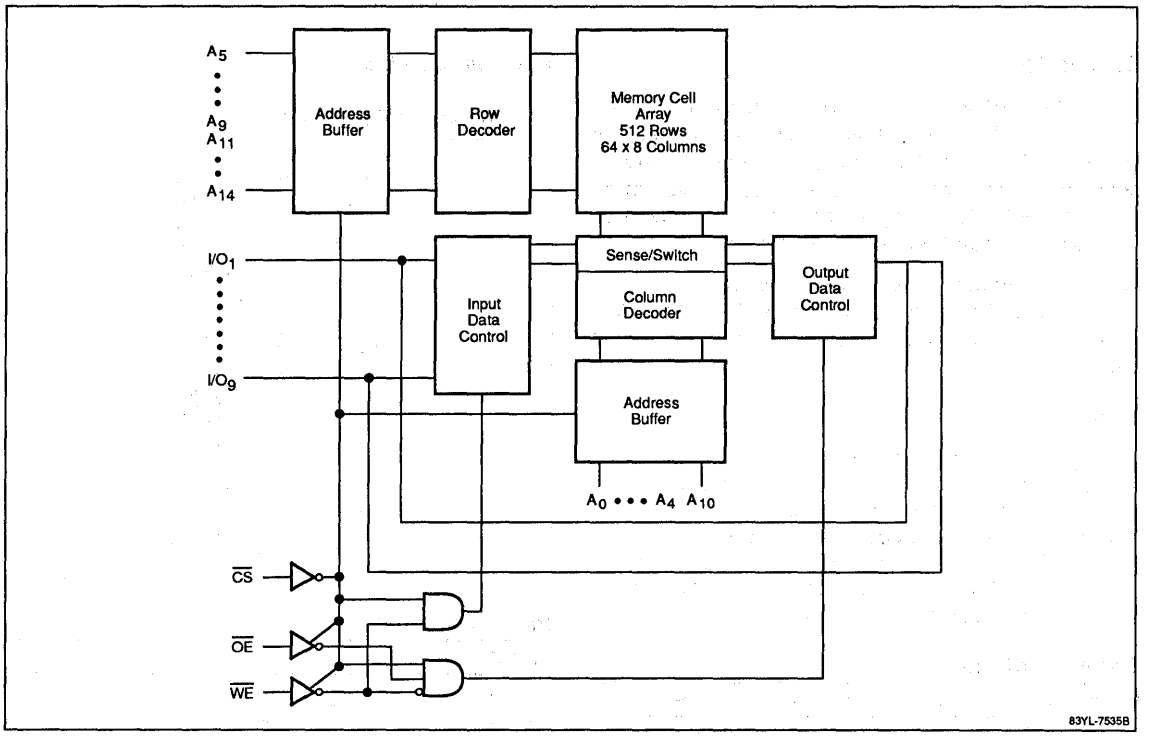
32-Pin Plastic DIP or SOJ



Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_1 - I/O_9	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Truth Table

Function	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	High-Z	Standby
Outputs disabled	L	H	H	High-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active

Notes:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 10 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−2		2	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Standby supply current	I_{SB}			30	ma	$\overline{CS} \geq V_{IH}$; $V_{IN} = V_{IH}$ or V_{IL}
	I_{SB1}			2	mA	$\overline{CS} \geq V_{CC} - 0.2$ V; $V_{IN} \leq 0.2$ V or $\geq V_{CC} - 0.2$ V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 10 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		6	pF
Input/output capacitance	$C_{I/O}$		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD43259A-15		μPD43259A-20		μPD43259A-25			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Operating supply current	I_{CC}		150		140		130	mA	$\overline{CS} \le V_{IL}$ (min cycle); $I_{I/O}$ = 0 mA
Read cycle time	t_{RC}	15		20		25		ns	(Note 2)
Address access time	t_{AA}		15		20		25	ns	(Note 2)
Chip select access time	t_{ACS}		15		20		25	ns	(Note 2)
Output enable to output valid	t_{OE}		9		10		12	ns	(Note 2)
Output hold from address change	t_{OH}	3		3		3		ns	(Note 2)
Chip select to output in low-Z	t_{CLZ}	3		3		3		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	0		0		0		ns	(Note 3)
Chip select to output in high-Z	t_{CHZ}		10		10		10	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		8		8		10	ns	(Note 3)
Write Operation									
Write cycle time	t_{WC}	15		20		25		ns	
Chip select to end of write	t_{CW}	12		13		15		ns	
Address valid to end of write	t_{AW}	12		13		15		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	12		13		15		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	9		10		12		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		8		8		10	ns	(Note 3)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = 0 to 3 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output load.

(3) See figure 2 for output load.

20e

Figure 1. Output Load

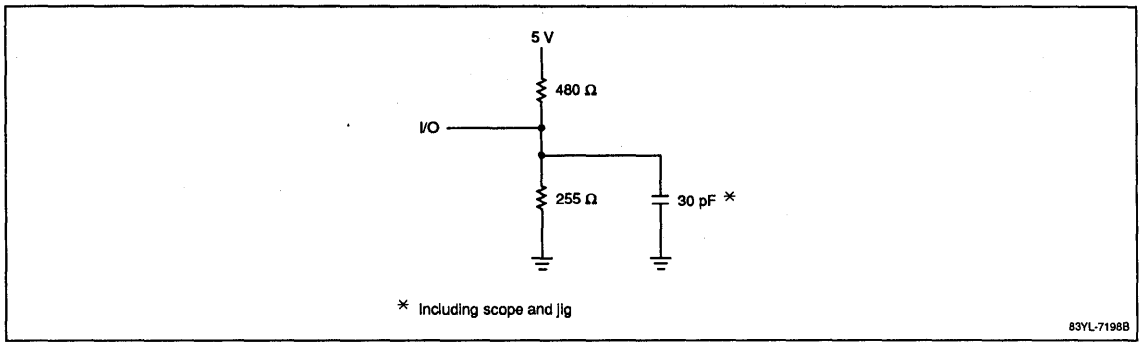
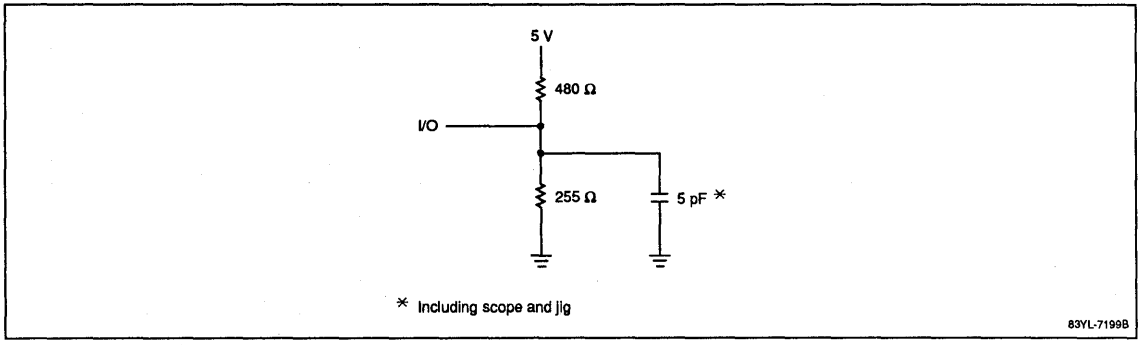
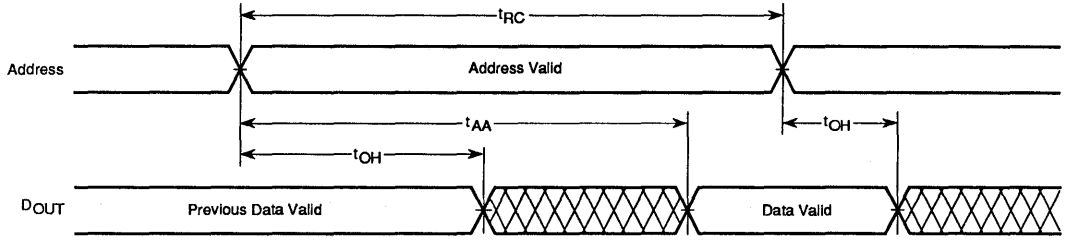


Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

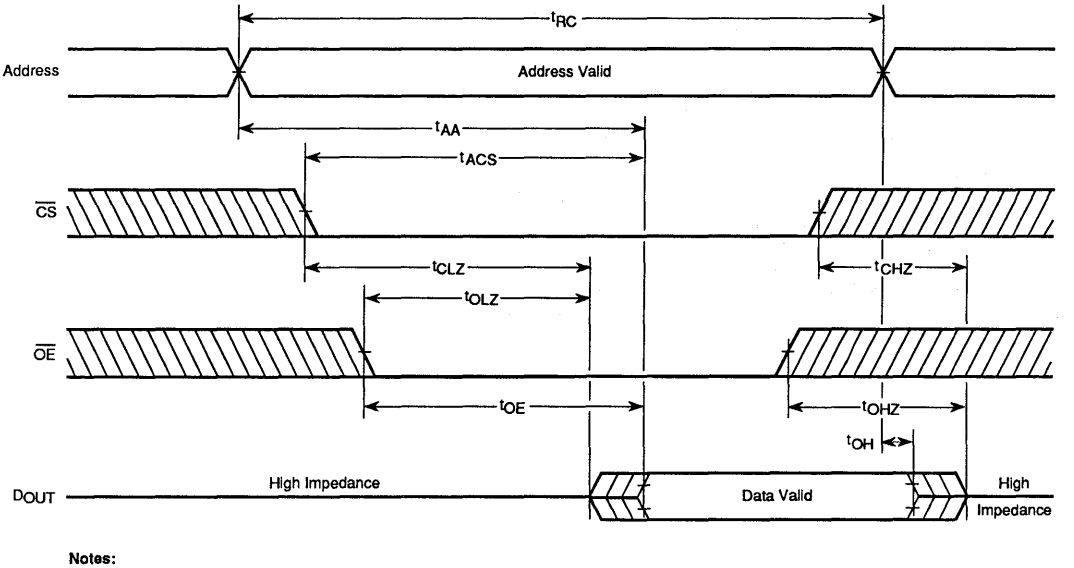
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6436B

Chip Select Access Cycle



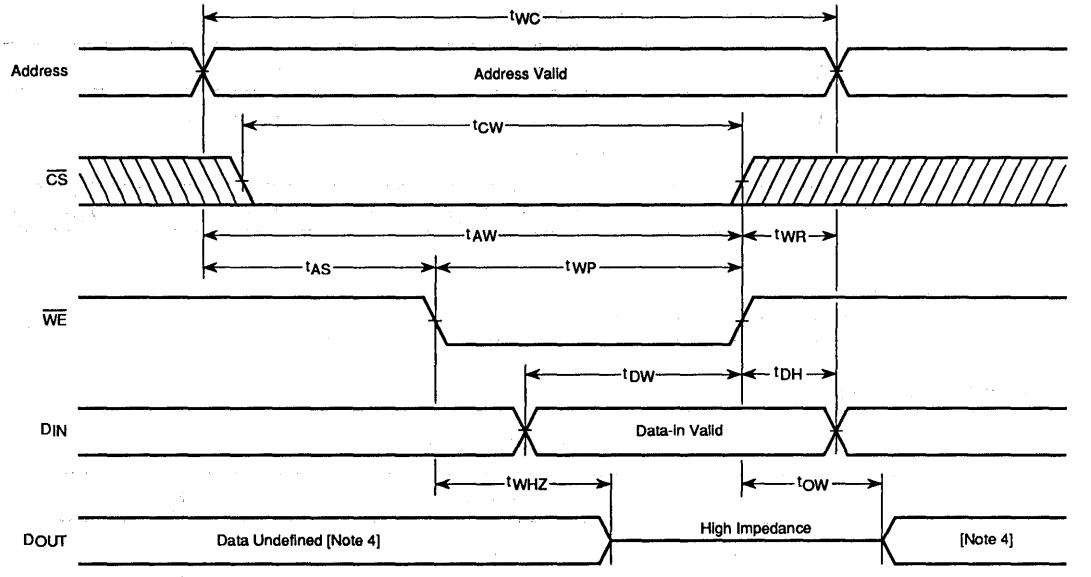
Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6437B

20e

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

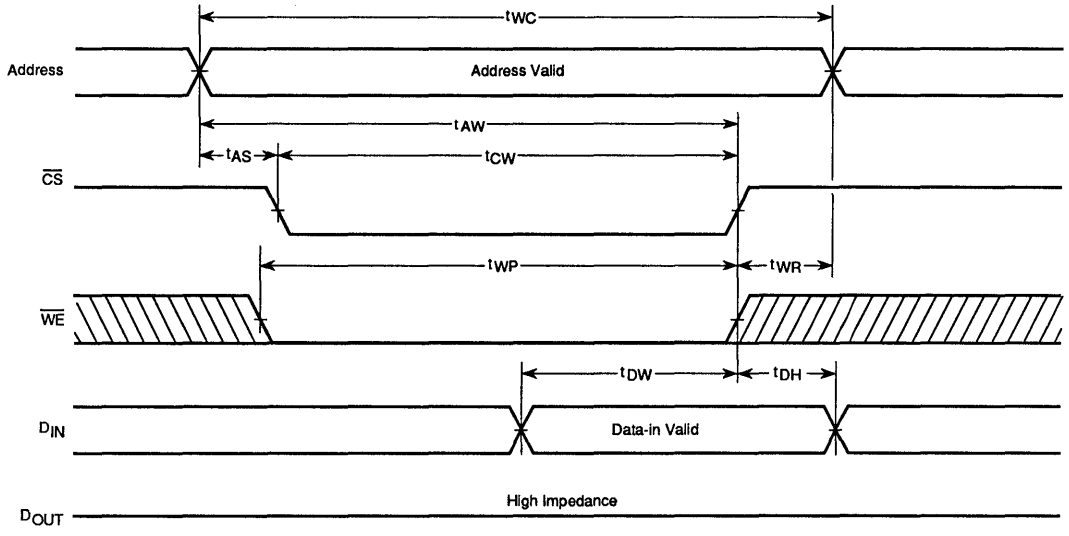
[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

[4] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

83IH-6438B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

83IH-6439B

20e

NEC

Section 21
Fast Static RAMs (1M)

μPD	Organization	Features	
431001	1M x 1	20-ns	21a
431004	256K x 4	20-ns	21b
431008	128K x 8	15-ns; Output enable	21c
431009	128K x 9	15-ns; Output enable	21d
431016	64K x 16	15-ns; Output enable	21e
431018	64K x 18	15-ns; Output enable	21f

Upcoming Products

Description	Device Number	Comments
128K x 8	μPD461008	Speeds to 8 ns; 3.3- and 5-V versions
128K x 9	μPD461009	Speeds to 8 ns; 3.3- and 5-V versions
64K x 16	μPD461016	Speeds to 8 ns; 3.3- and 5-V versions
64K x 18	μPD461018	Speeds to 8 ns; 3.3- and 5-V versions

μPD431001
1,048,576 x 1-Bit
Static CMOS RAM

Description

The μPD431001 is a 1,048,576-word by 1-bit static RAM fabricated with advanced silicon-gate technology. A unique design that uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors makes the μPD431001 a high-speed device that requires no clock or refreshing. The μPD431001 is available in 28-pin plastic SOJ packaging.

Features

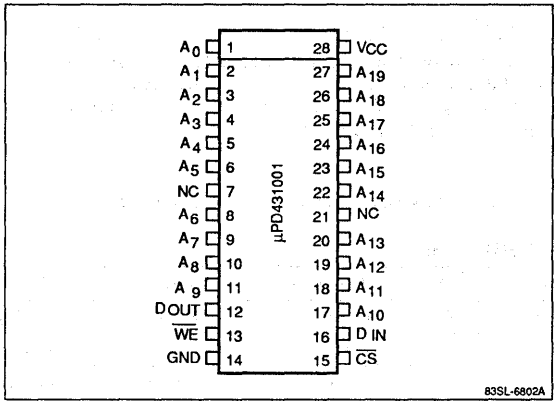
- 1,048,576-word x 1-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Power dissipation
  - —140 mA max (active)
  - —2 mA max (standby)
- Standard 400-mil, 28-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD431001LE-20	20 ns	28-pin plastic SOJ
LE-25	25 ns	
LE-35	35 ns	

Pin Configuration

28-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{19}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

21a

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.5 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V minimum for 10 ns maximum pulse.

Truth Table

$\overline{CS}$	$\overline{WE}$	Function	D_{OUT}	I_{CC}
H	X	Not selected	High-Z	Standby
L	H	Read	Output data	Active
L	L	Write	High-Z	Active

Note:

(1) X = don't care

Capacitance

T_A = +25°C; f = 1 MHz (Note 1); V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Output capacitance	C_O			10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

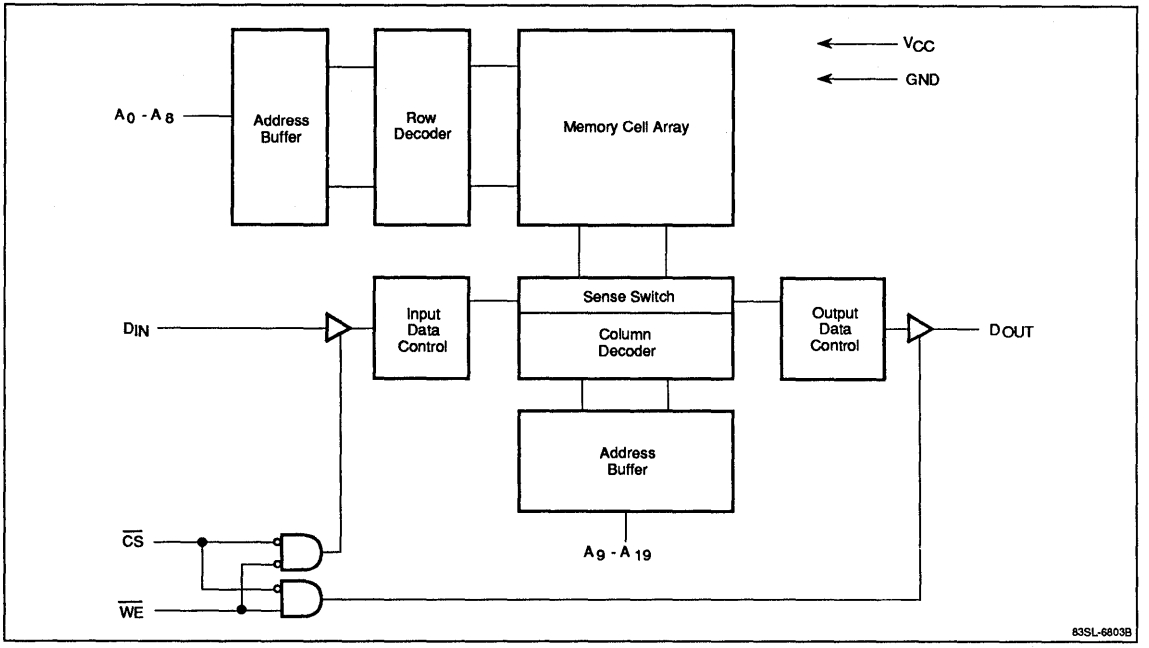
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Note:

(1) V_{IL} = −3.0 V minimum for 10 ns maximum pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD431001-20		μPD431001-25		μPD431001-35			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		140		120		100	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); I_{OUT} = 0 mA
Read cycle time	t_{RC}	20		25		35		ns	(Note 2)
Read access time	t_{AA}		20		25		35	ns	
Chip select access time	t_{ACS}		20		25		35	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in low-Z	t_{CLZ}	5		5		5		ns	(Note 3)
Chip deselect to output in high-Z	t_{CHZ}	0	8	0	10	0	15	ns	(Note 4)
Write Operation									
Write cycle time	t_{WC}	20		25		35		ns	(Note 2)
Chip select to end of write	t_{CW}	15		20		30		ns	
Address valid to end of write	t_{AW}	15		20		30		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	15		15		25		ns	
Write recovery time	t_{WR}	3		3		3		ns	
Data valid to end of write	t_{DW}	12		15		20		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		8	0	10	0	10	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 3 ns; timing reference levels = 1.5 V; see figures 1 and 2 for the output load.

(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the load shown in figure 2.

(4) The transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 2.

Figure 1. Output Load

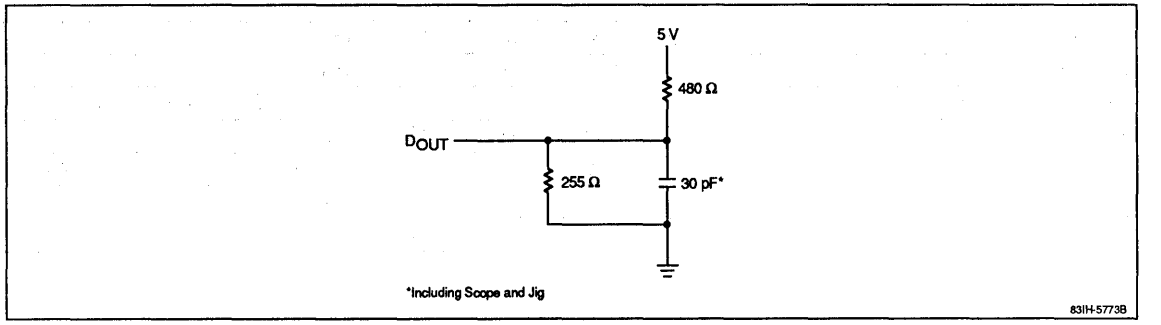
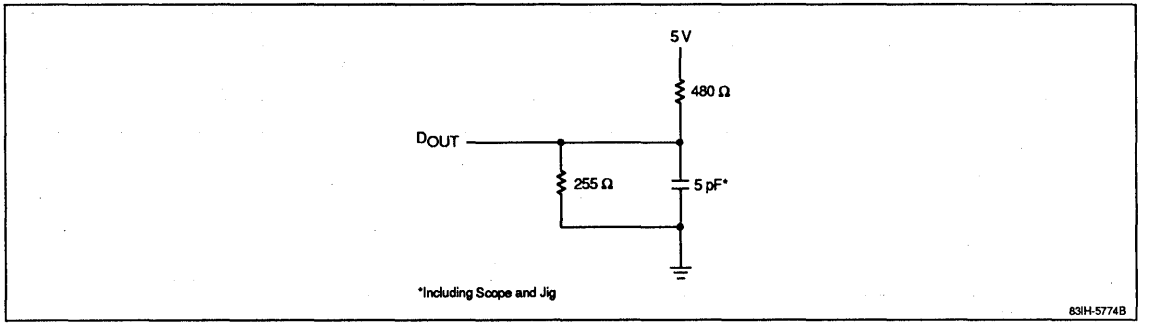
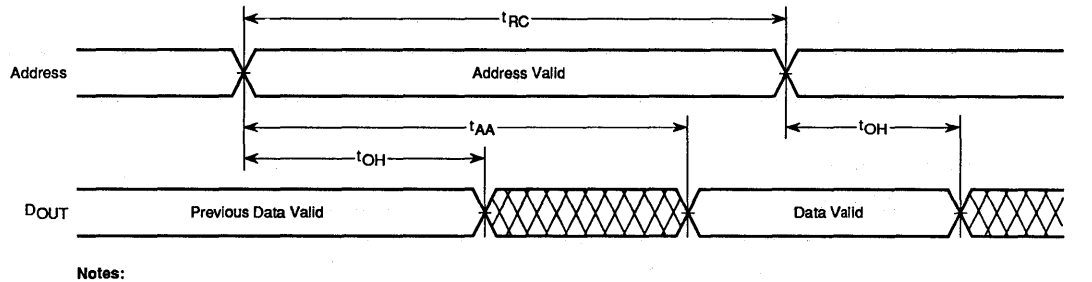


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{OW}, and t_{WHZ}



Timing Waveforms

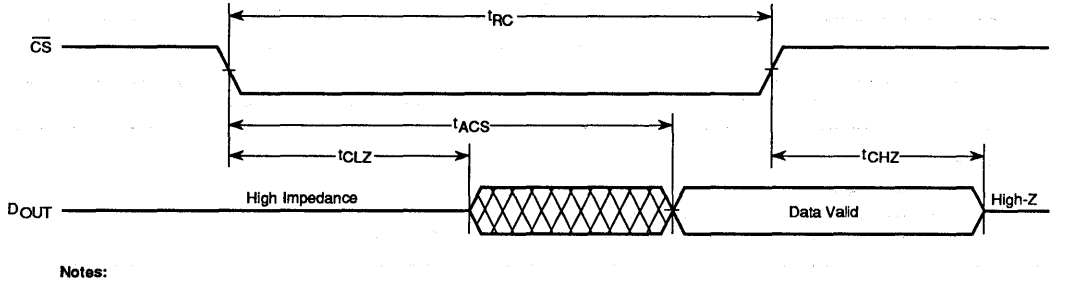
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle



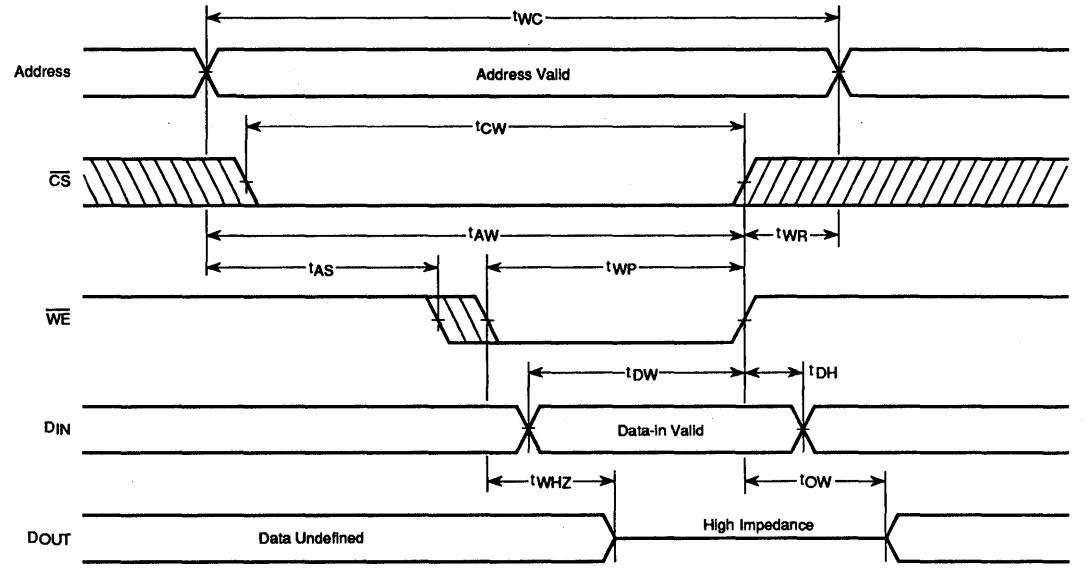
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-5776B

21a

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

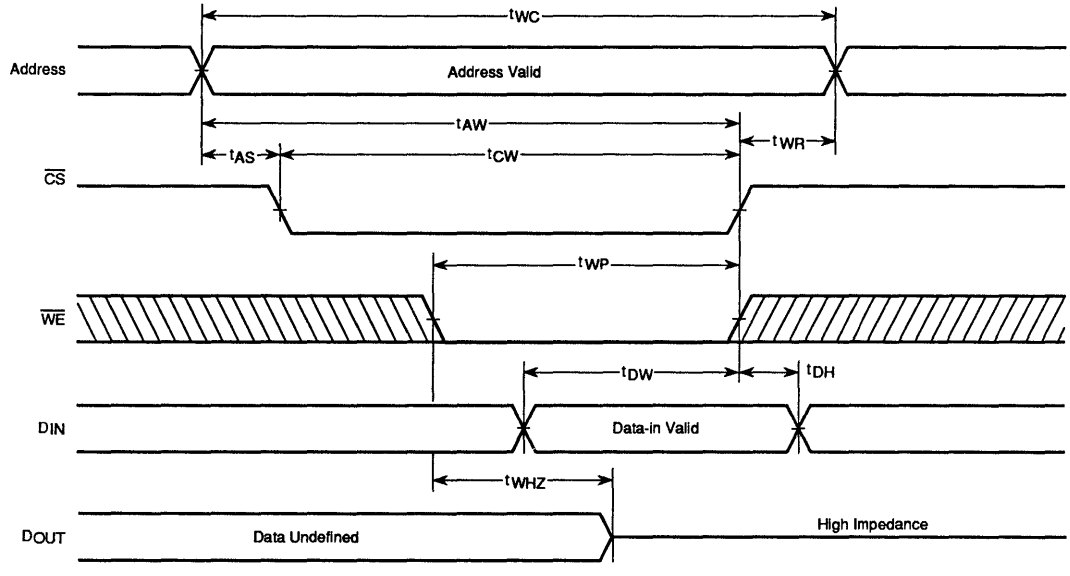
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

831H-5777B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5778B

21a

μPD431004
262,144 x 4-Bit
Static CMOS RAM

Description

The μPD431004 is a 262,144-word by 4-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD431004 a high-speed device that requires very low power and no clock or refreshing.

The μPD431004 is available in standard 28-pin plastic SOJ packaging.

Features

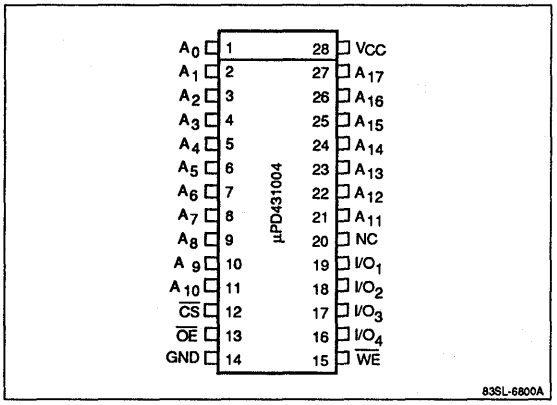
- 262,144-word x 4-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Low power dissipation
  - 150 mA max (active)
  - 2 mA max (standby)
- Standard 28-pin plastic SOJ packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD431004LE-20	20 ns	28-pin plastic SOJ
LE-25	25 ns	
LE-35	35 ns	

Pin Configuration

28-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
I/O_1 - I/O_4	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+ 5-volt power supply
NC	No connection

21b

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) V_{IN} = −3.0 V minimum for 10 ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz (Note 1)

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

Function	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	I_{CC}
Not selected	H	X	X	High-Z	Standby
Output disable	L	H	H	High-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

Notes:

(1) X = don't care.

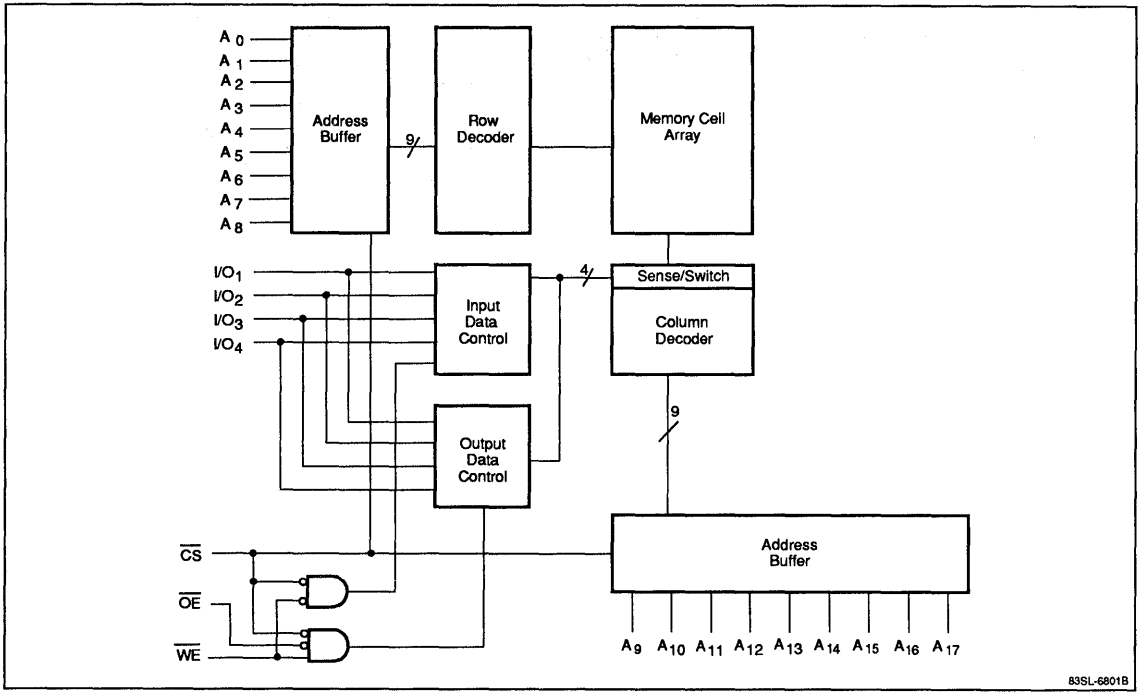
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Notes:

(1) V_{IL} = −3.0 V minimum for 10 ns pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			2	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD431004-20		μPD431004-25		μPD431004-35			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		150		140		120	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); I_{DOUT} = 0 mA
Read cycle time	t_{RC}	20		25		35		ns	(Note 2)
Address access time	t_{AA}		20		25		35	ns	
Chip select access time	t_{ACS}		20		25		35	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Output enable access time	t_{OE}		10		10		15	ns	
Output enable to output in low-Z	t_{OLZ}	0		0		0		ns	(Note 3)
Output disable to output in high-Z	t_{OHZ}	0	8	0	10	0	15	ns	(Note 4)
Chip selection to output in low-Z	t_{CLZ}	5		5		5		ns	(Note 3)
Chip selection to output in high-Z	t_{CHZ}	0	8	0	10	0	15	ns	(Note 4)
Write Operation									
Write cycle time	t_{WC}	20		25		35		ns	(Note 2)
Chip select to end of write	t_{CW}	15		20		30		ns	
Address valid to end of write	t_{AW}	15		20		30		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	15		20		30		ns	
Write recovery time	t_{WR}	3		3		3		ns	
Data valid to end of write	t_{DW}	12		12		20		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}	0	8	0	8	0	10	ns	(Note 4)
Output active from end of write	t_{OW}	0		0		0		ns	(Note 3)

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figures 1 and 2 for output load.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 2.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 2.

Figure 1. Output Load

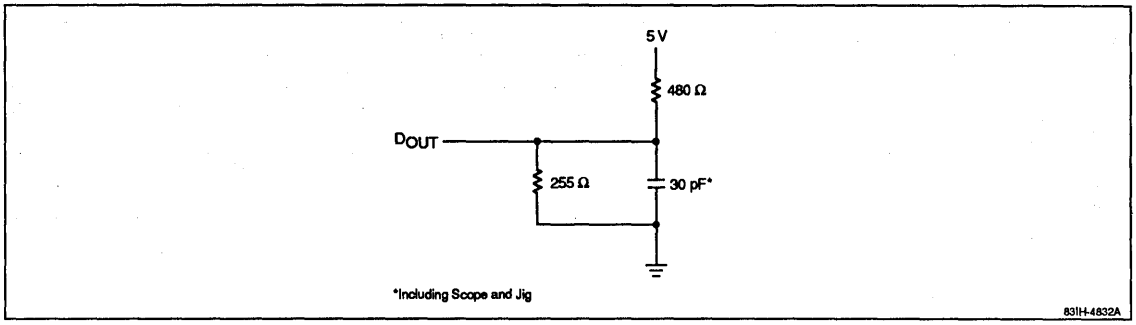
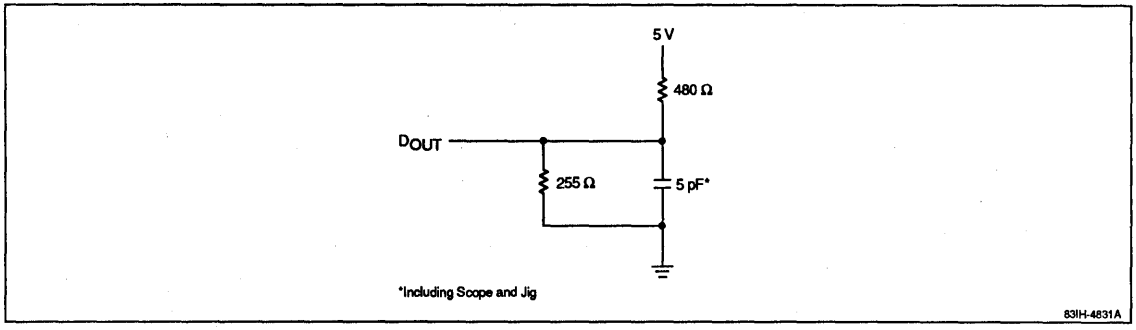
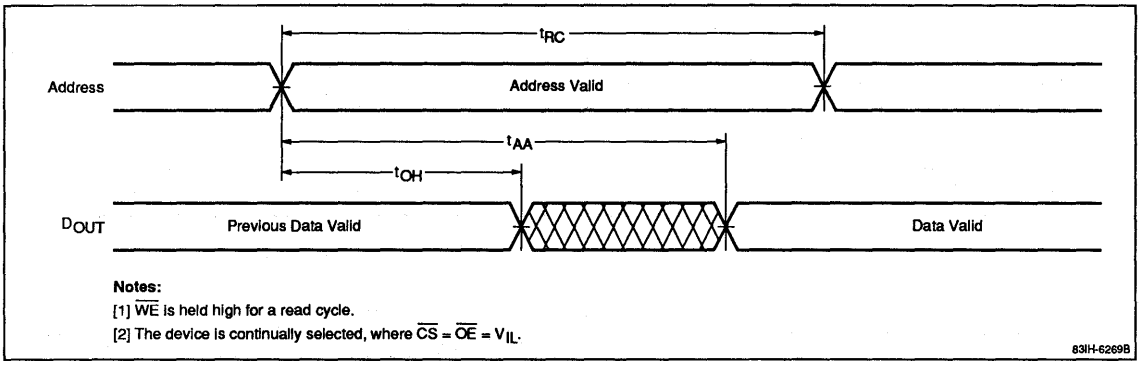


Figure 2. Output Load for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

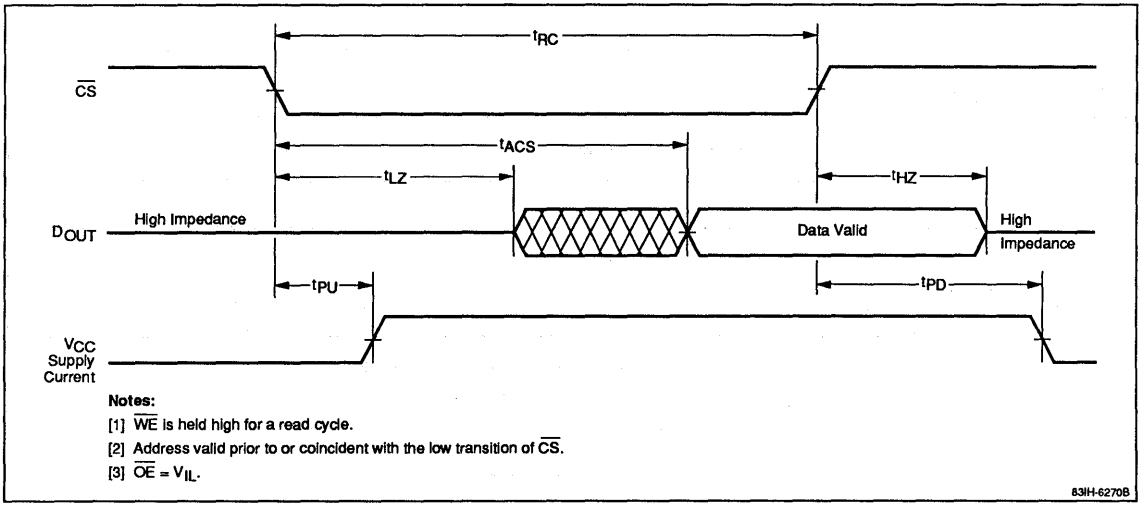
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6269B

Chip Select Access Cycle



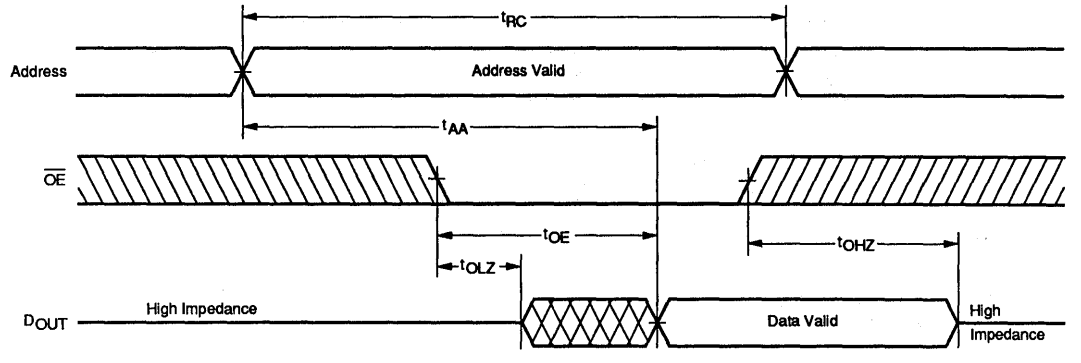
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.
[3] $\overline{OE} = V_{IL}$.

83IH-6270B

21b

Timing Waveforms (cont)

Output Enable Access Cycle



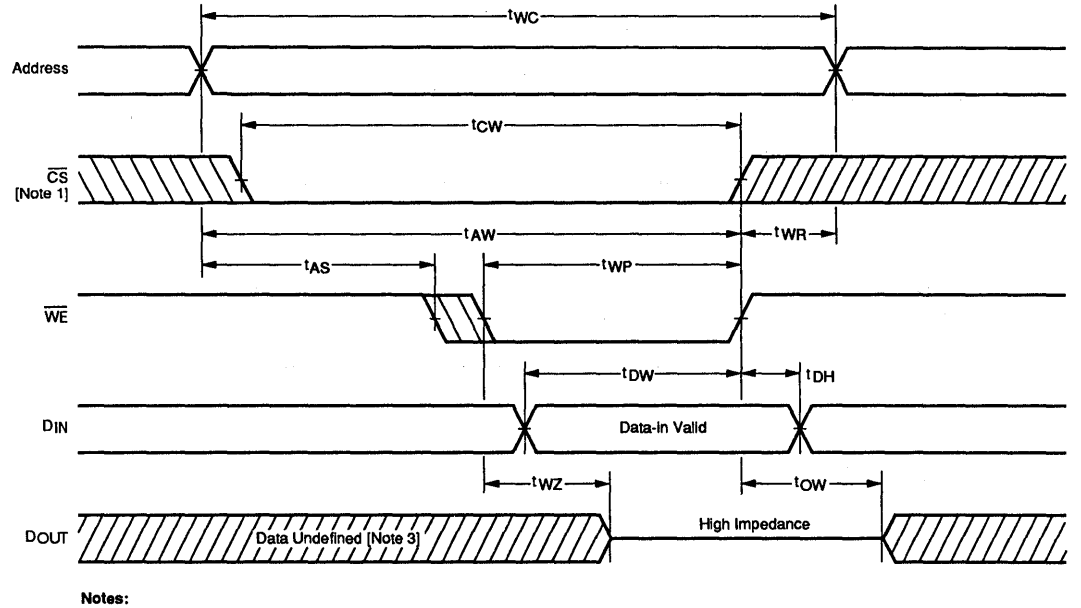
Notes:

[1] $\overline{WE}$ is held high for a read cycle.

[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-6271B

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

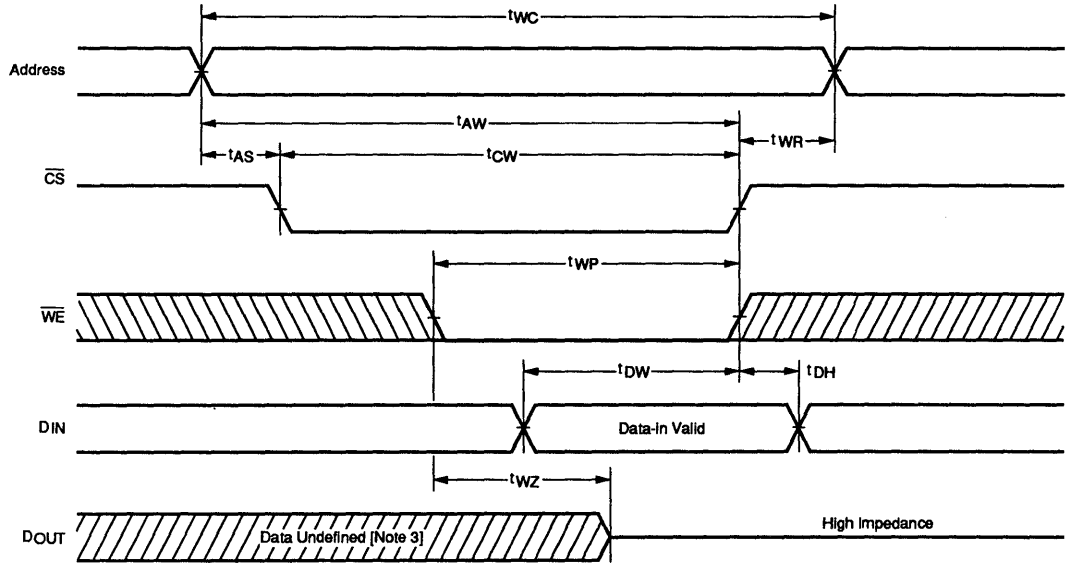
[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

83IH-6272B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[3] During this period, the I/O pins may be active ($\overline{OE}$ low). Therefore, data input signals of opposite polarity to the outputs must not be applied.

83IH-6273B

μPD431008
131,072 x 8-Bit
Static CMOS RAM

Description

The μPD431008 is a 131,072-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells to make the μPD431008 a high-speed device that requires no clock or refreshing. The μPD431008 is available in a standard 32-pin plastic SOJ.

Features

- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Standard 32-pin plastic SOJ packaging

Ordering Information

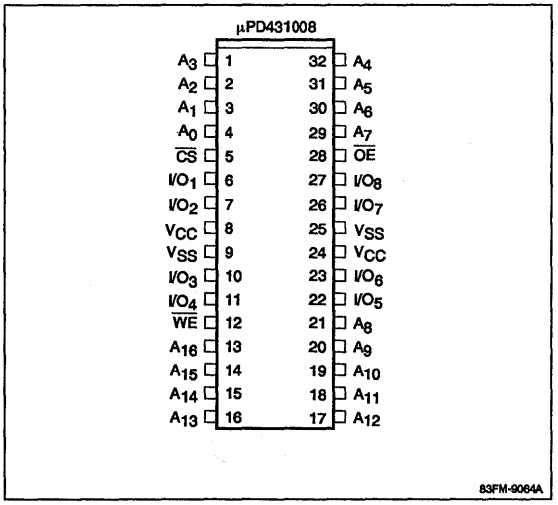
Part Number	Access Time (max)	Package
μPD431008LE-15	15 ns	32-pin plastic SOJ
LE-17	17 ns	
LE-20	20 ns	

Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

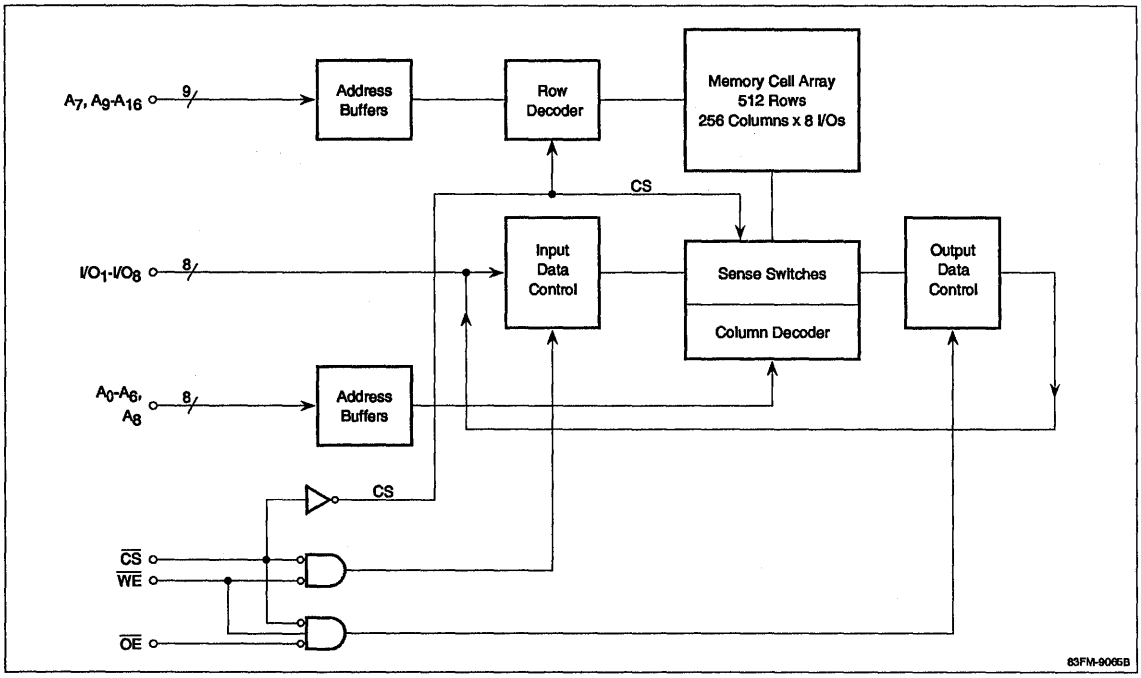
Pin Configuration

32-Pin Plastic SOJ



21c

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) −3.0 V minimum (pulse width = 10 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		6	pF
Input/output capacitance	$C_{I/O}$		8	pF

Note:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Outputs disabled	High-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Note:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Note:

(1) −3.0 V minimum (pulse width = 10 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

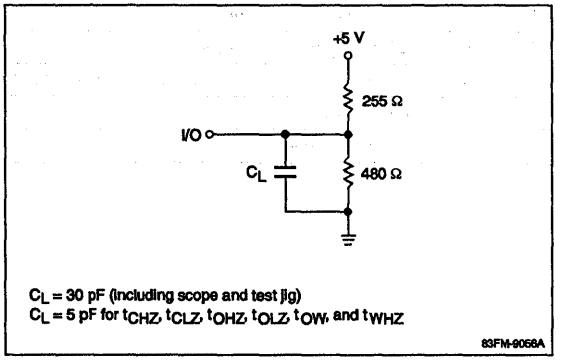
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−2		2	μA	$V_{I/O}$ = 0 V to V_{CC}
Operating supply current	I_{CC1} (t_{RC} = t_{WC}) = 15 ns)			160	mA	$\overline{CS}$ = V_{IL}; $I_{I/O}$ = 0 mA
	I_{CC2} (t_{RC} = t_{WC}) = 17 ns)			150	mA	$\overline{CS}$ = V_{IL}; $I_{I/O}$ = 0 mA
	I_{CC3} (t_{RC} = t_{WC}) = 20 ns)			140	mA	$\overline{CS}$ = V_{IL}; $I_{I/O}$ = 0 mA
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ ≥ V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB1}			10	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	μPD431008-15 Min	μPD431008-15 Max	μPD431008-17 Min	μPD431008-17 Max	μPD431008-20 Min	μPD431008-20 Max	Unit	Test Conditions
Read Operation									
Read cycle time	t_{RC}	15		17		20		ns	
Address access time	t_{AA}		15		17		20	ns	
Chip select access time	t_{ACS}		15		17		20	ns	
Output enable to output valid	t_{OE}		8		9		10	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in low-Z	t_{CLZ}	5		5		5		ns	
Output enable to output in low-Z	t_{OLZ}	1		1		1		ns	
Chip select to output in high-Z	t_{CHZ}		7		7		7	ns	
Output enable to output in high-Z	t_{OHZ}		7		7		7	ns	
Write Operation									
Write cycle time	t_{WC}	15		17		20		ns	
Chip select to end of write	t_{CW}	10		11		12		ns	
Address valid to end of write	t_{AW}	9		11		12		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	9		10		10		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	8		9		10		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		7		7		7	ns	
Output active from end of write	t_{OW}	3		3		3		ns	

Figure 1.Output Loads

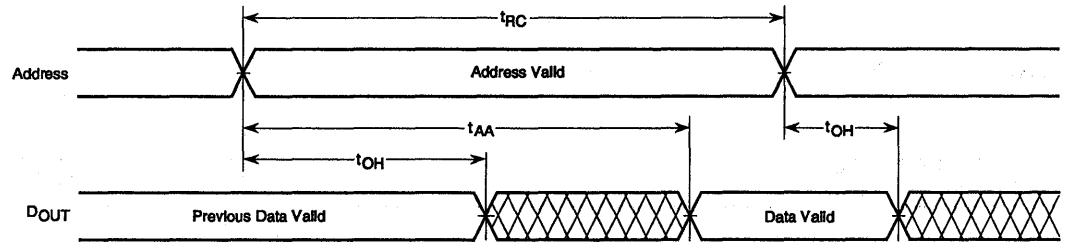


C_L = 30 pF (including scope and test jig)
C_L = 5 pF for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}

83FM-8056A

Timing Waveforms

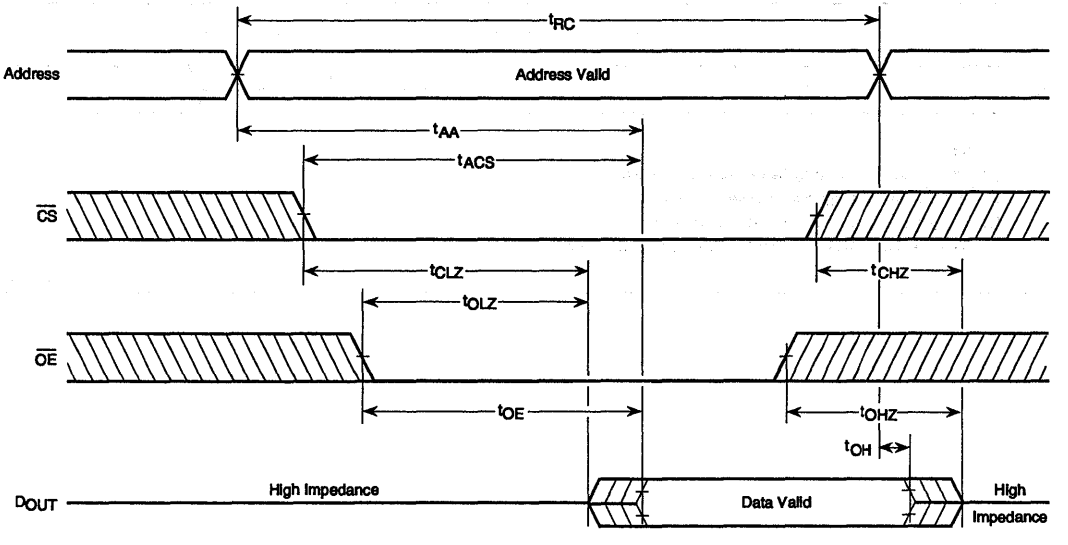
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6436B

Chip Select Access Cycle

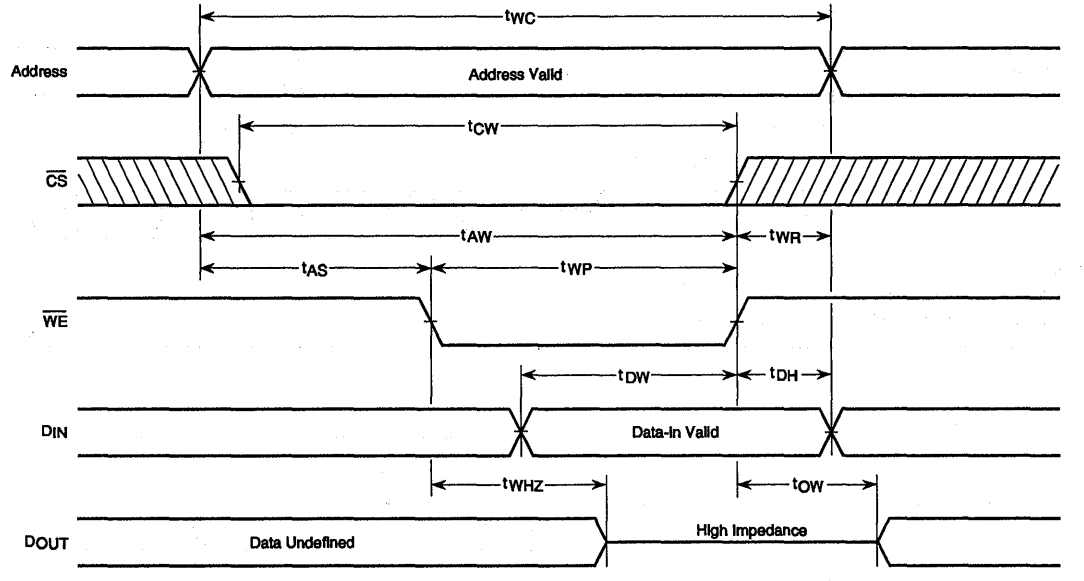


Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6437B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

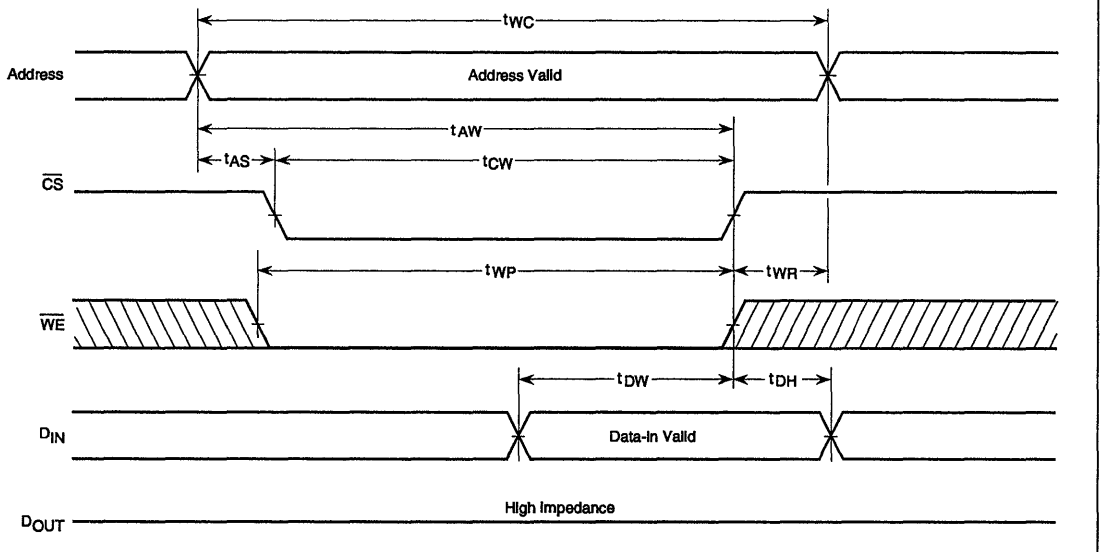
[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

83CL-9057B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83CL-90588

21c

μPD431009
131,072 x 9-Bit
Static CMOS RAM

Description

The μPD431009 is a 131,072-word by 9-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells to make the μPD431009 a high-speed device that requires no clock or refreshing. The μPD431009 is available in a standard 36-pin plastic SOJ.

Features

- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Standard 36-pin, 400-mil plastic SOJ packaging

Ordering Information

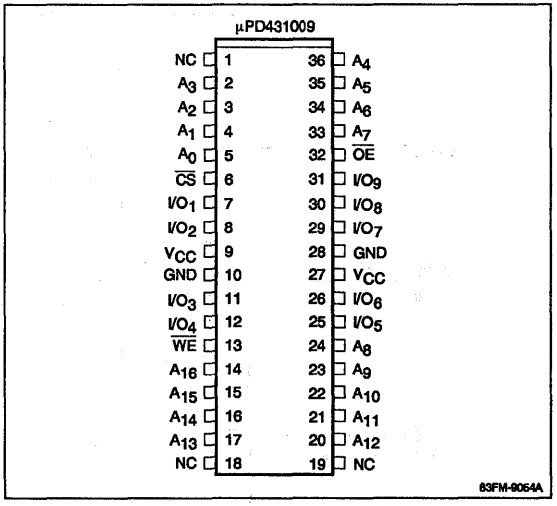
Part Number	Access Time (max)	Package
μPD431009LE-15	15 ns	36-pin plastic SOJ
LE-17	17 ns	
LE-20	20 ns	

Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
I/O_1 - I/O_9	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

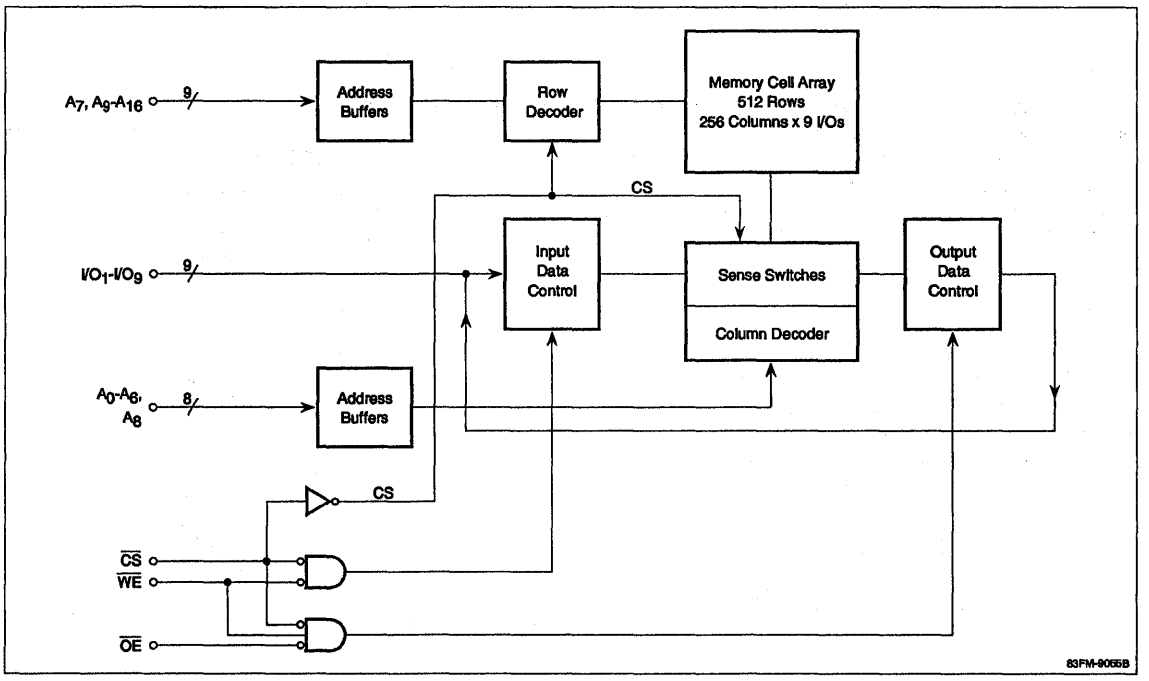
Pin Configuration

36-Pin Plastic SOJ



21d

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) −3.0 V minimum (pulse width = 10 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		6	pF
Input/output capacitance	$C_{I/O}$		8	pF

Note:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Outputs disabled	High-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Note:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Note:

(1) −3.0 V minimum (pulse width = 10 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

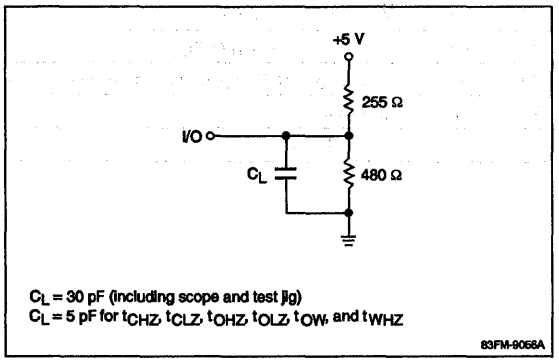
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−2		2	μA	$V_{I/O}$ = 0 V to V_{CC}
Operating supply current	I_{CC1} (t_{RC} = t_{WC} = 15 ns)			160	mA	$\overline{CS}$ = V_{IL}; $I_{I/O}$ = 0 mA
	I_{CC2} (t_{RC} = t_{WC} = 17 ns)			150	mA	$\overline{CS}$ = V_{IL}; $I_{I/O}$ = 0 mA
	I_{CC3} (t_{RC} = t_{WC} = 20 ns)			140	mA	$\overline{CS}$ = V_{IL}; $I_{I/O}$ = 0 mA
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ ≥ V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB1}			10	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

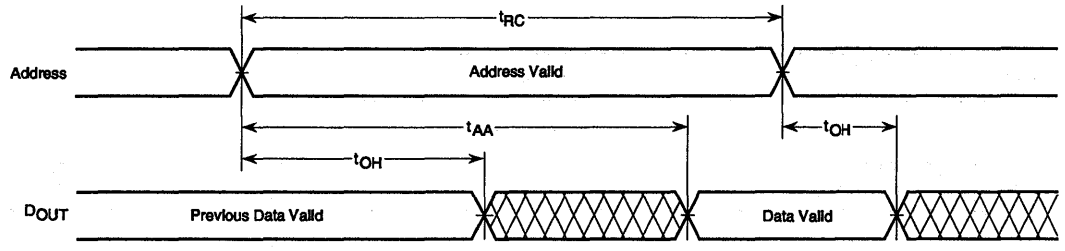
Parameter	Symbol	μPD431009-15 Min	μPD431009-15 Max	μPD431009-17 Min	μPD431009-17 Max	μPD431009-20 Min	μPD431009-20 Max	Unit	Test Conditions
Read Operation									
Read cycle time	t_{RC}	15		17		20		ns	
Address access time	t_{AA}		15		17		20	ns	
Chip select access time	t_{ACS}		15		17		20	ns	
Output enable to output valid	t_{OE}		8		9		10	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Chip select to output in low-Z	t_{CLZ}	5		5		5		ns	
Output enable to output in low-Z	t_{OLZ}	1		1		1		ns	
Chip select to output in high-Z	t_{CHZ}		7		7		7	ns	
Output enable to output in high-Z	t_{OHZ}		7		7		7	ns	
Write Operation									
Write cycle time	t_{WC}	15		17		20		ns	
Chip select to end of write	t_{CW}	10		11		12		ns	
Address valid to end of write	t_{AW}	9		11		12		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	9		10		10		ns	
Write recovery time	t_{WR}	0		0		0		ns	
Data valid to end of write	t_{DW}	8		9		10		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		7		7		7	ns	
Output active from end of write	t_{OW}	3		3		3		ns	

Figure 1. Output Loads



Timing Waveforms

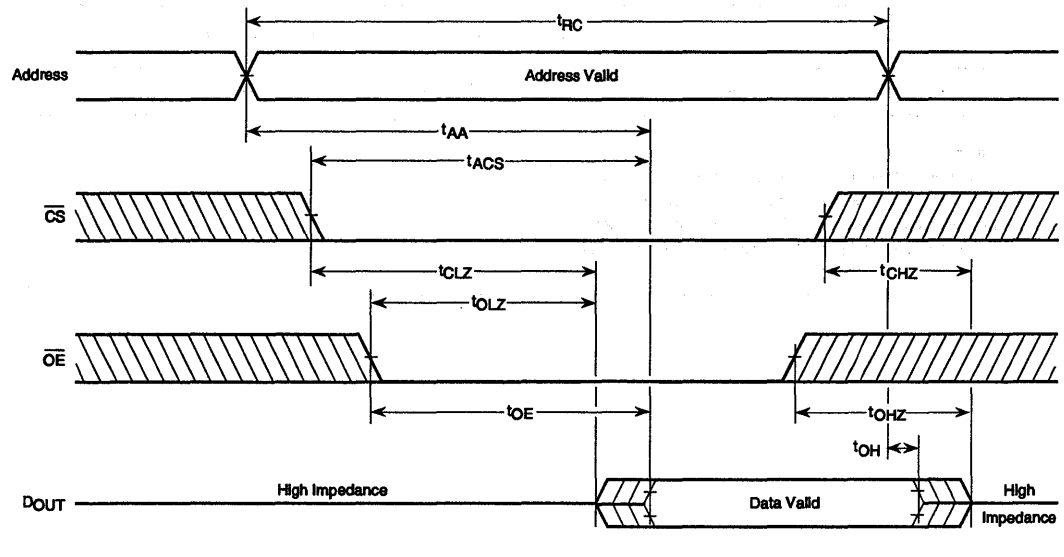
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6436B

Chip Select Access Cycle



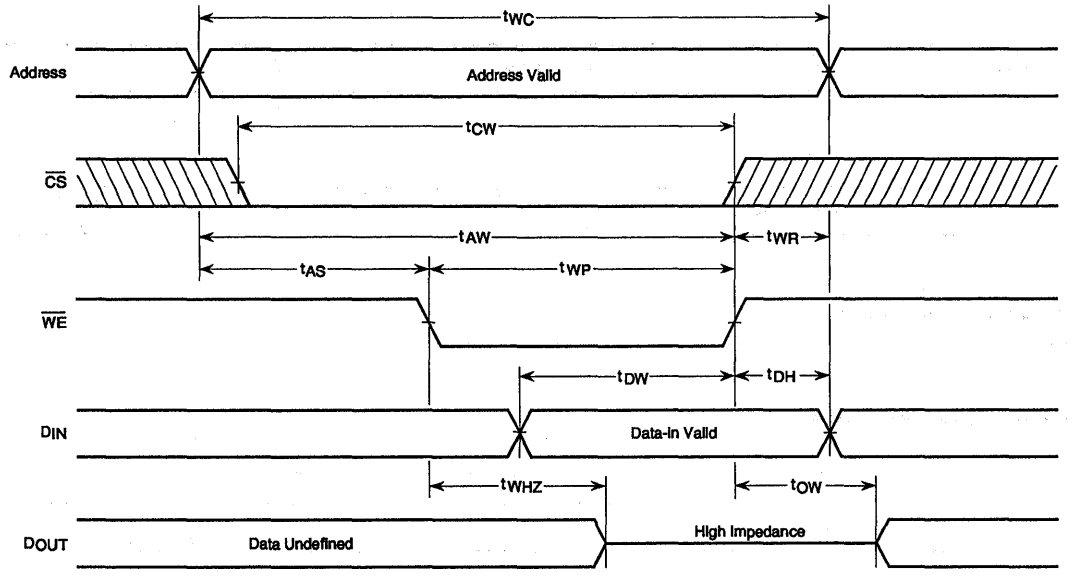
Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6437B

21d

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

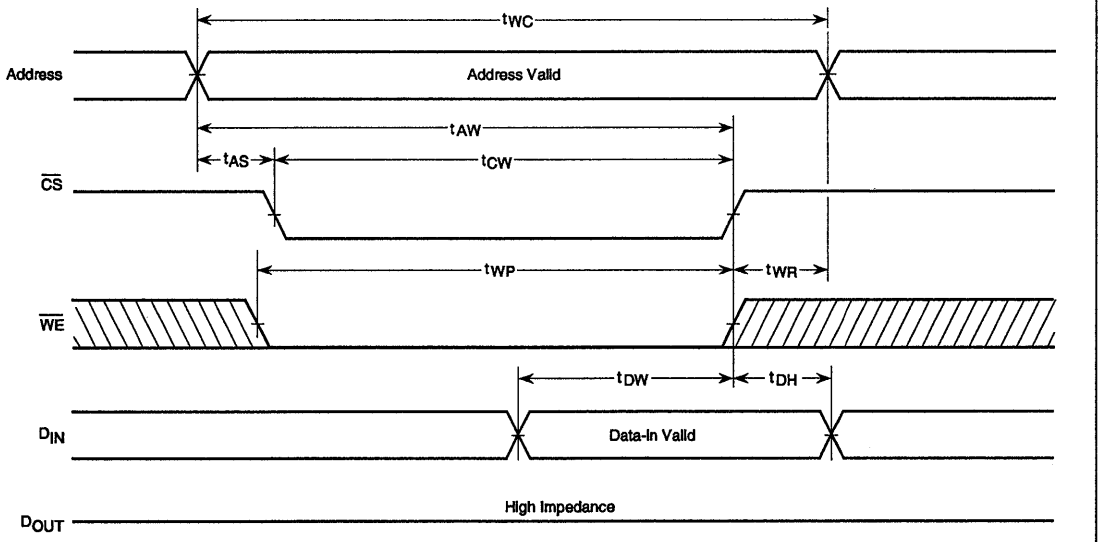
[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] During this period, the I/O pins may be in the output state.
Therefore, input signals of opposite phase must not be applied.

83CL-9057B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

83CL-9058B

21d

μPD431016
65,536 x 16-Bit
Static CMOS RAM

Description

The μPD431016 is a 65,536-word by 16-bit static RAM fabricated with advanced silicon-gate technology, unique CMOS peripheral circuits, and N-channel memory cells. It is suitable for cache memory and buffer memory applications where high speed, high density, and wide I/O SRAMs are required.

The μPD431016 operates with low power from a single +5-volt supply. No clock or refreshing is required. The plastic package is a standard 44-pin SOJ or TSOP.

Features

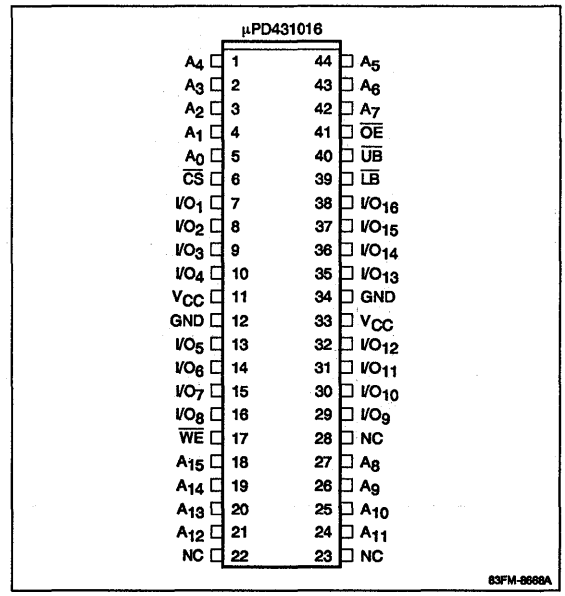
- 65,536-word x 16-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Output buffer control: $\overline{OE}$
- Data byte control: $\overline{LB}$, $\overline{UB}$
- Low power dissipation
  - 240 mA max (active)
  - 10 mA max (standby)
- Standard 44-pin, 400-mil plastic SOJ or TSOP package

Ordering Information

Part Number	Access Time (max)	Package
μPD431016LE-15	15 ns	44-pin plastic SOJ
LE-17	17 ns	
LE-20	20 ns	
μPD431016G5-15	15 ns	44-pin plastic TSOP
G5-17	17 ns	
G5-20	20 ns	

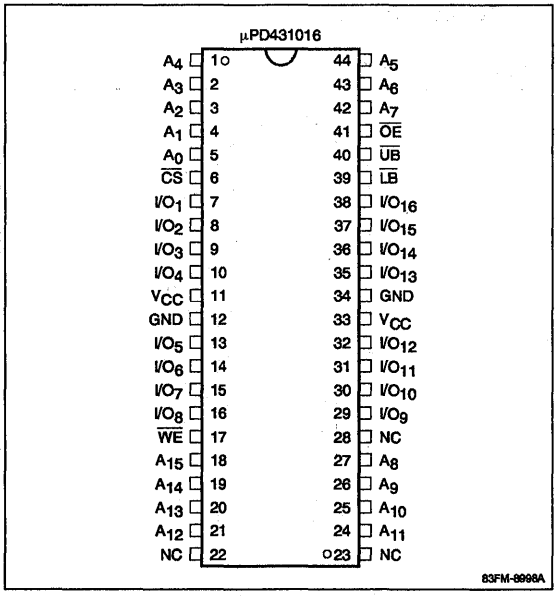
Pin Configurations

44-Pin Plastic SOJ



Pin Configurations (cont)

44-Pin Plastic TSOP



Pin Identification

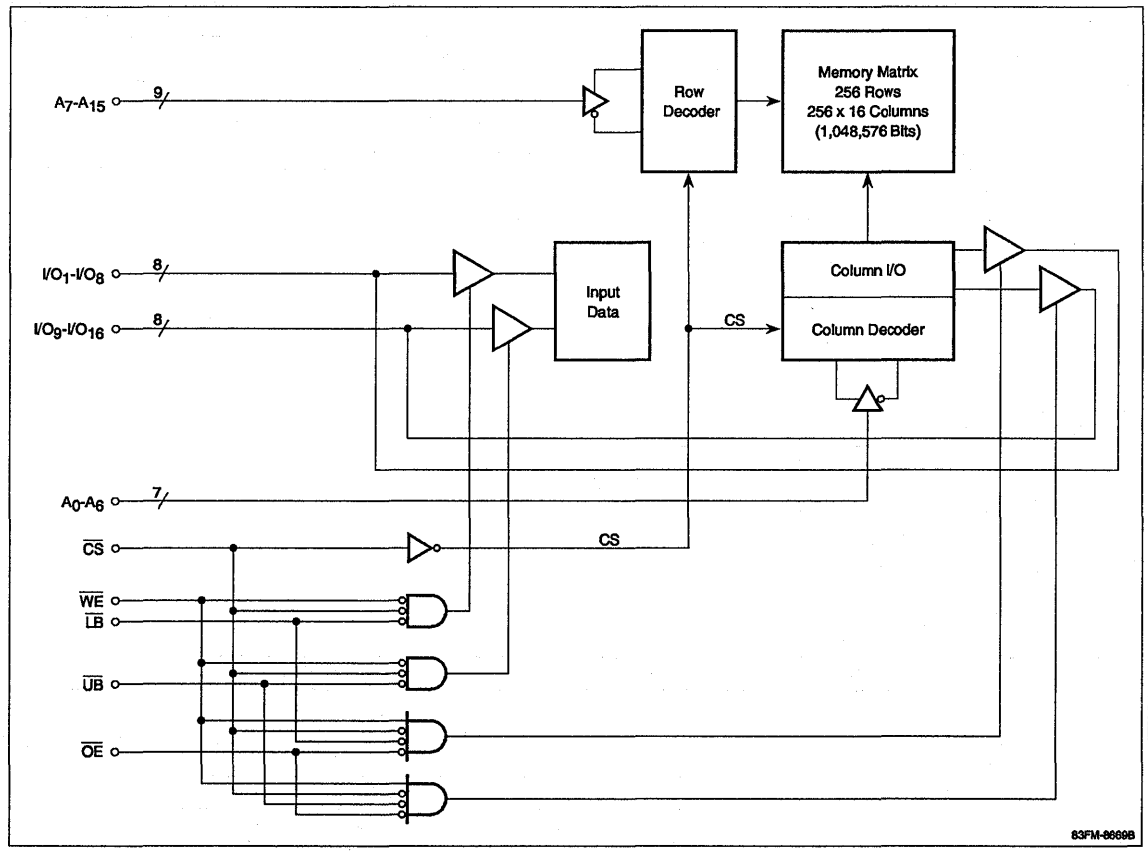
Symbol	Function
A_0 - A_{15}	Address inputs
I/O_1 - I/O_{16}	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{LB}$	Lower byte select (I/O_1 - I/O_8)
$\overline{OE}$	Output enable
$\overline{UB}$	Upper byte select (I/O_9 - I/O_{16})
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O_1 - I/O_8	I/O_9 - I/O_{16}	Power
H	X	X	X	X	Not selected	Hi-Z	Hi-Z	Standby
L	L	H	L	L	Read	D_{OUT}	D_{OUT}	Active
			L	H	Read	D_{OUT}	Hi-Z	
			H	L	Read	Hi-Z	D_{OUT}	
L	X	L	L	L	Write	D_{IN}	D_{IN}	
			L	H	Write	D_{IN}	Hi-Z	
			H	L	Write	Hi-Z	D_{IN}	
L	H	H	X	X	—	Hi-Z	Hi-Z	
L	X	X	H	H	—	Hi-Z	Hi-Z	

X = Don't care.

Block Diagram



21e

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) V_{IN} (min) = −3.0 V for 10-ns pulse.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Note:

(1) V_{IL} = −3.0 V for 10-ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		8	pF

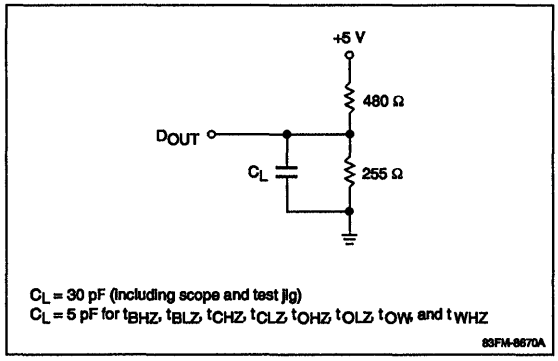
Capacitance is sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$, $\overline{OE}$, $\overline{LB}$, or UB = V_{IH} or $\overline{WE}$ = V_{IL}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			10	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Figure 1. Output Loads



AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD431016-15 Min	μPD431016-15 Max	μPD431016-17 Min	μPD431016-17 Max	μPD431016-20 Min	μPD431016-20 Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		240		230		220	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA (Note 5)
Address access time	t_{AA}		15		17		20	ns	
Chip select access time	t_{ACS}		15		17		20	ns	
Data byte select access time	t_{ADB}		8		9		10	ns	
Data byte select to output in high-Z	t_{BHZ}		7		7		7	ns	
Data byte select to output in low-Z	t_{BLZ}	1		1		1		ns	
Chip deselection to output in high-Z	t_{CHZ}	0	7	0	7	0	7	ns	(Note 4)
Chip selection to output in low-Z	t_{CLZ}	5		5		5		ns	(Note 3)
Output enable access time	t_{OE}		8		9		10	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Output enable to output in high-Z	t_{OHZ}		7		7		7	ns	
Output enable to output in low-Z	t_{OLZ}	1		1		1		ns	
Read cycle time	t_{RC}	15		17		20		ns	(Note 2)
Write Operation									
Address setup time	t_{AS}	0		0		0		ns	
Address valid to end of write	t_{AW}	9		11		12		ns	
Data byte select to end of write	t_{BW}	9		11		12		ns	
Chip select to end of write	t_{CW}	10		11		12		ns	
Data hold time	t_{DH}	0		0		0		ns	
Data valid to end of write	t_{DW}	8		9		10		ns	
Output active from end of write	t_{OW}	3		3		3		ns	(Note 3)
Write enable to output in high-Z	t_{WHZ}	0	7	0	7	0	7	ns	(Note 4)
Write cycle time	t_{WC}	15		17		20		ns	(Note 2)
Write pulse width	t_{WP}	9		10		10		ns	
Write recovery time	t_{WR}	0		0		0		ns	

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figure 1 for output loads.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 1.

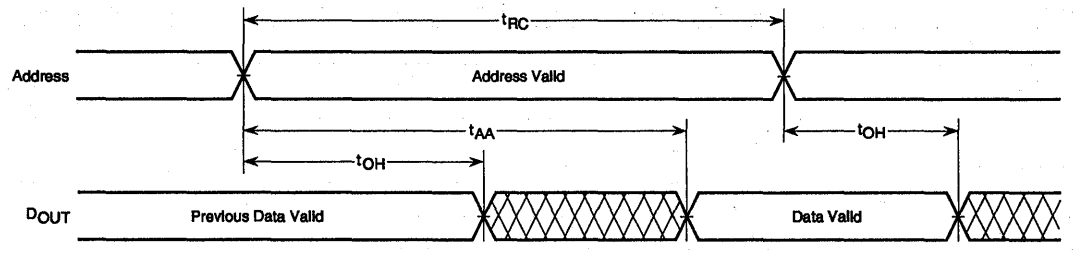
(4) Transition is measured at V_{OL} + 200 mV and V_{OH} – 200 mV with the load shown in figure 1.

(5) I_{CC} = 180 mA max at t_{AA} = 50 ns.

21e

Timing Waveforms

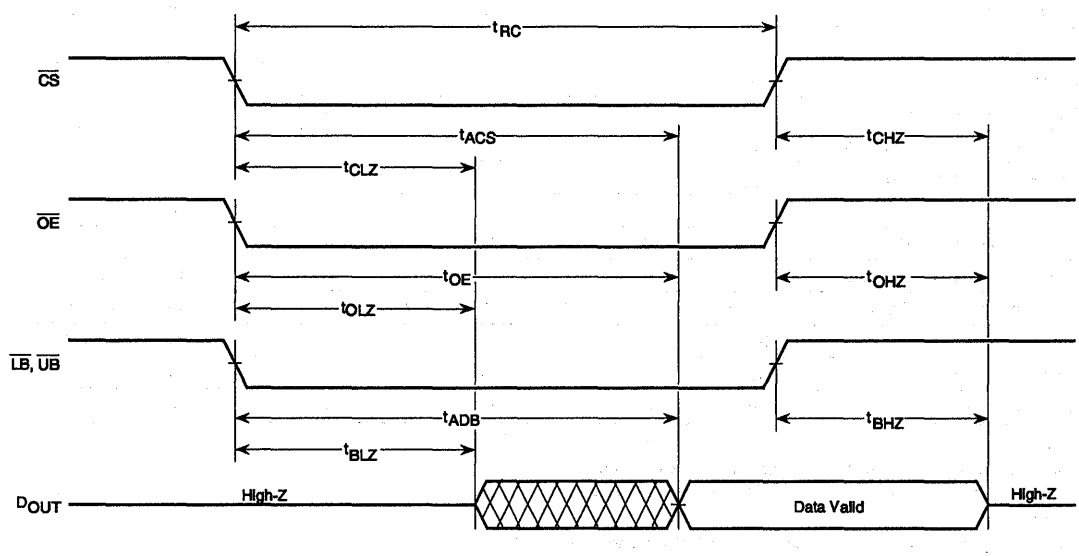
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle

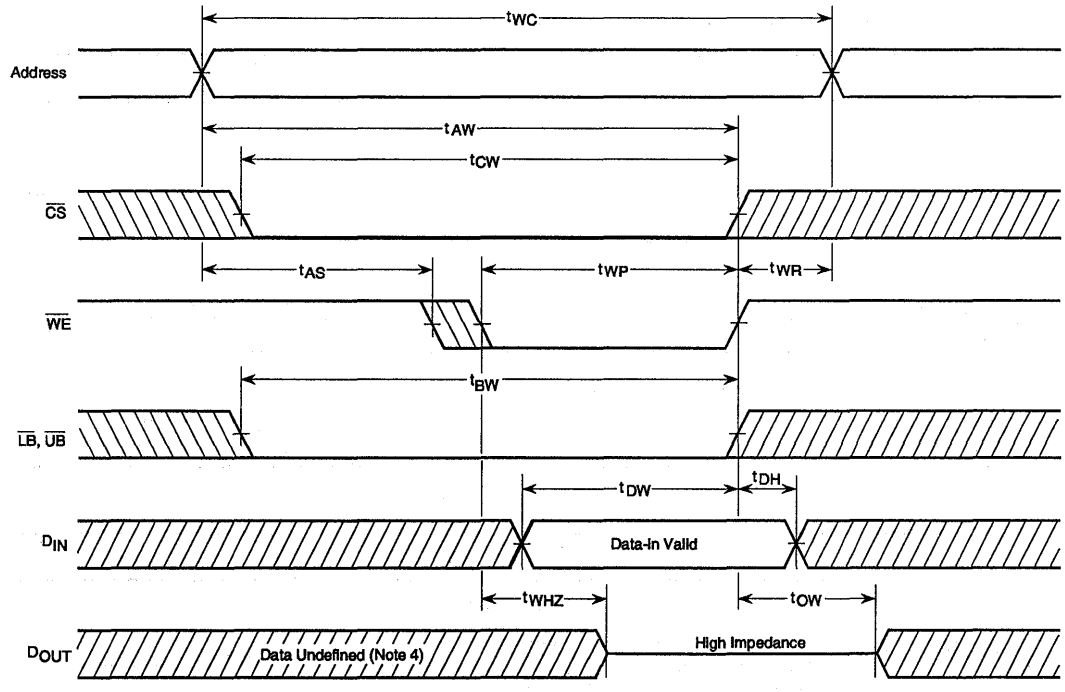


Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Device is continuously selected:
$\overline{CS} = \overline{OE} = \overline{LB} = Low$
$\overline{CS} = \overline{OE} = \overline{UB} = Low$
[3] Address valid prior to or coincident with $\overline{CS}$ transition low.

83IH-8671B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{LB}$ low.

[2] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{UB}$ low.

[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

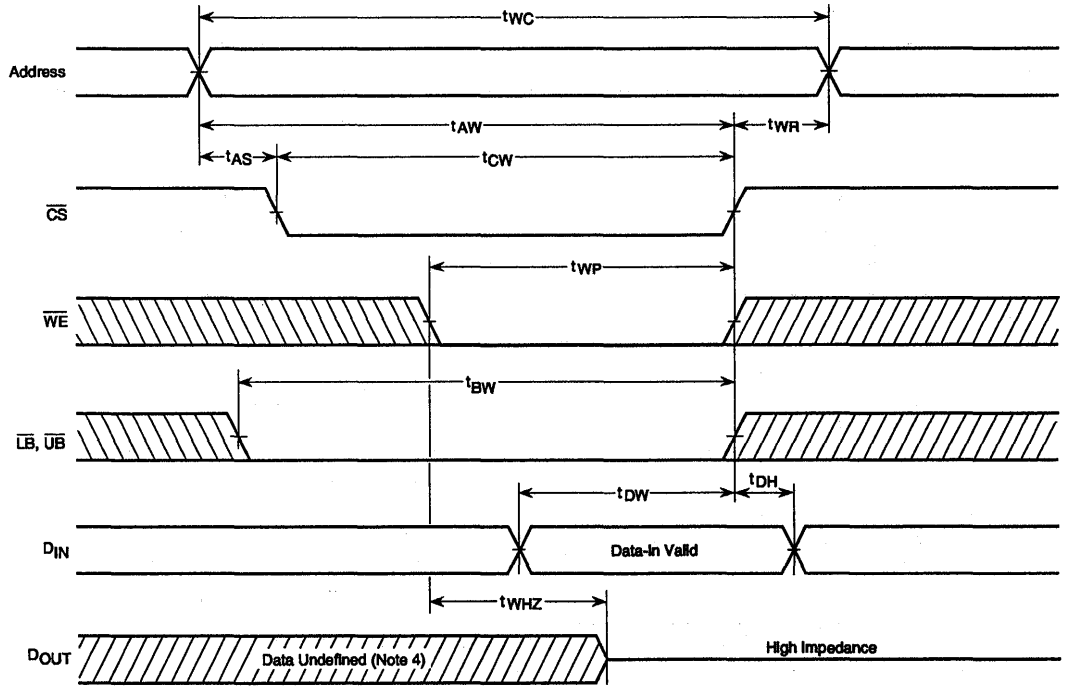
[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

83IH-8672B

21e

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle

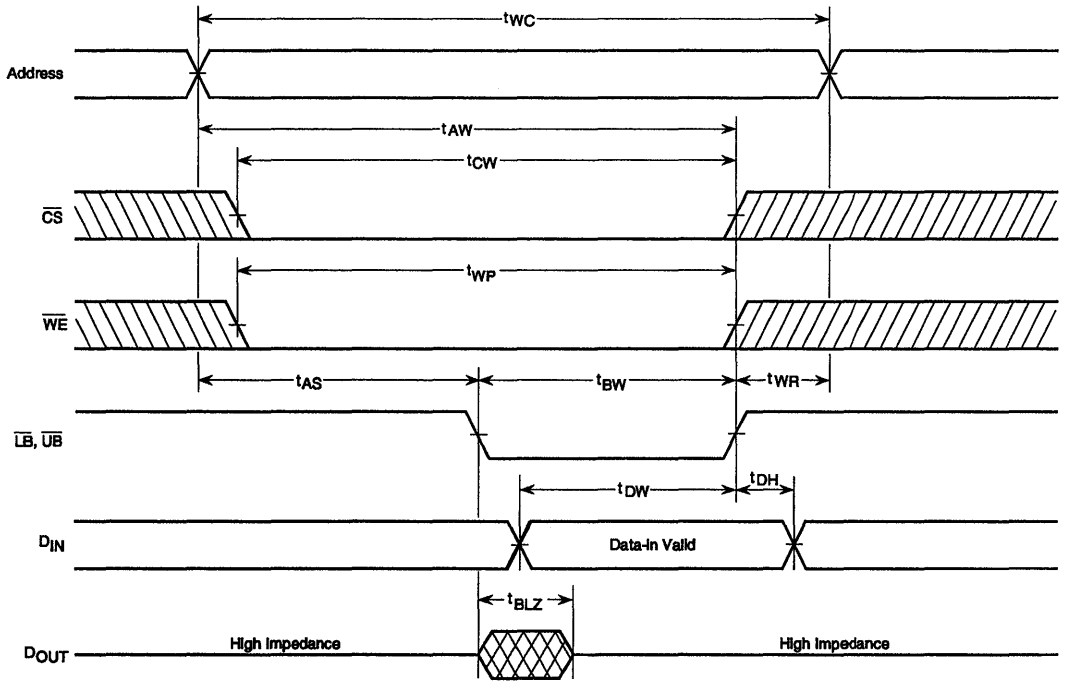


Notes:
[1] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{LB}$ low.
[2] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{UB}$ low.
[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

831H-8673B

Timing Waveforms (cont)

$\overline{LB}$/ $\overline{UB}$-Controlled Write Cycle



Notes:

[1] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{LB}$ low.

[2] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{UB}$ low.

[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

83IH-8674B

21e

μPD431018
65,536 x 18-Bit
Static CMOS RAM

Description

The μPD431018 is a 65,536-word by 18-bit static RAM fabricated with advanced silicon-gate technology, unique CMOS peripheral circuits, and N-channel memory cells. It is suitable for cache memory and buffer memory applications where high speed, high density, and wide I/O SRAMs are required.

The μPD431018 operates with low power from a single +5-volt supply. No clock or refreshing is required. The plastic package is a standard 44-pin SOJ or TSOP.

Features

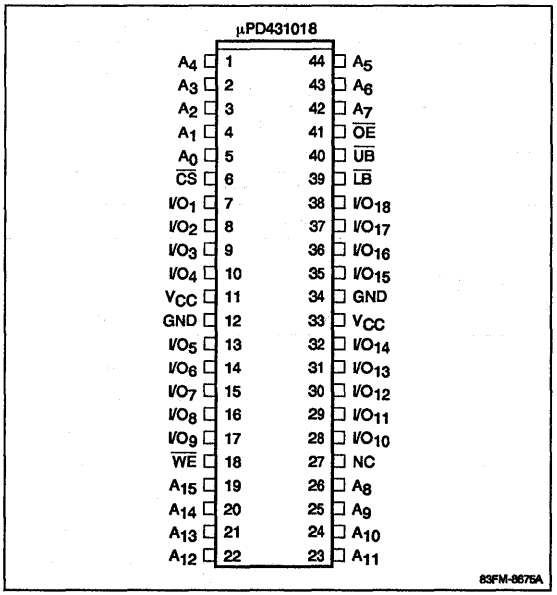
- 65,536-word x 18-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O capability
- Output buffer control: $\overline{OE}$
- Data byte control: $\overline{LB}$, $\overline{UB}$
- Low power dissipation
  - 260 mA max (active)
  - 10 mA max (standby)
- Standard 44-pin, 400-mil SOJ or TSOP plastic package

Ordering Information

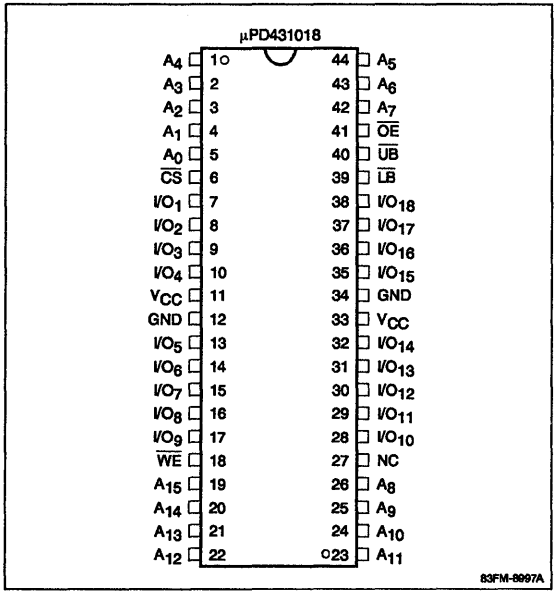
Part Number	Access Time (max)	Package
μPD431018LE-15	15 ns	44-pin plastic SOJ
LE-17	17 ns	
LE-20	20 ns	
μPD431018G5-15	15 ns	44-pin plastic TSOP
G5-17	17 ns	
G5-20	20 ns	

Pin Configurations

44-Pin Plastic SOJ



44-Pin Plastic TSOP



21f

Pin Identification

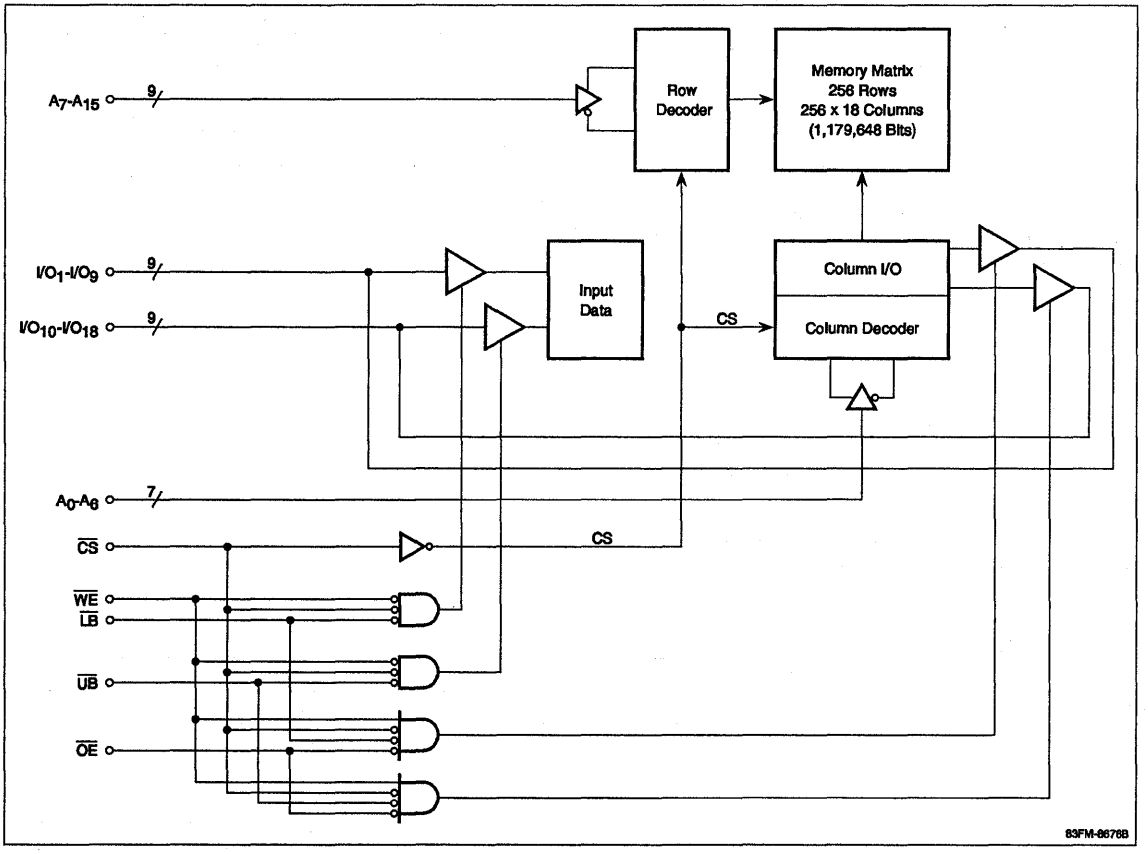
Symbol	Function
A_0 - A_{15}	Address inputs
I/O_1 - I/O_{18}	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{LB}$	Lower byte select (I/O_1 - I/O_9)
$\overline{OE}$	Output enable
$\overline{UB}$	Upper byte select (I/O_{10} - I/O_{18})
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O_1 - I/O_9	I/O_{10} - I/O_{18}	Power
H	X	X	X	X	Not selected	Hi-Z	Hi-Z	Standby
L	L	H	L	L	Read	D_{OUT}	D_{OUT}	Active
			L	H	Read	D_{OUT}	Hi-Z	
			H	L	Read	Hi-Z	D_{OUT}	
L	X	L	L	L	Write	D_{IN}	D_{IN}	
			L	H	Write	D_{IN}	Hi-Z	
			H	L	Write	Hi-Z	D_{IN}	
L	H	H	X	X	—	Hi-Z	Hi-Z	
L	X	X	H	H	—	Hi-Z	Hi-Z	

X = Don't care.

Block Diagram



21f

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input and output voltages, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) V_{IN} (min) = −3.0 V for 10-ns pulse.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Operating temperature	T_A	0		70	°C

Note:

(1) V_{IL} = −3.0 V for 10-ns pulse.

Capacitance

T_A = 25°C; V_{IN} and V_{DOUT} = 0 V; f = 1 MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_{IN}		6	pF
Output capacitance	C_{DOUT}		8	pF

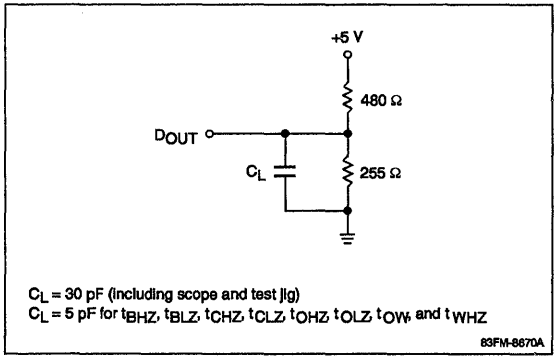
Capacitance is sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$, $\overline{OE}$, $\overline{LB}$, or UB = V_{IH} or $\overline{WE}$ = V_{IL}
Standby supply current	I_{SB}			30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}			10	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Figure 1. Output Loads



C_L = 30 pF (including scope and test jig)
C_L = 5 pF for t_{BHZ}, t_{BLZ}, t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}

83FM-8670A

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	μPD431018-15 Min	μPD431018-15 Max	μPD431018-17 Min	μPD431018-17 Max	μPD431018-20 Min	μPD431018-20 Max	Unit	Test Conditions
Read Operation									
Operating supply current	I_{CC}		260		220		200	mA	$\overline{CS}$ = V_{IL}; I_{DOUT} = 0 mA (Note 5)
Address access time	t_{AA}		15		17		20	ns	
Chip select access time	t_{ACS}		15		17		20	ns	
Data byte select access time	t_{ADB}		8		9		10	ns	
Data byte select to output in high-Z	t_{BHZ}		7		7		7	ns	
Data byte select to output in low-Z	t_{BLZ}	1		1		1		ns	
Chip deselection to output in high-Z	t_{CHZ}	0	7	0	7	0	7	ns	(Note 4)
Chip selection to output in low-Z	t_{CLZ}	5		5		5		ns	(Note 3)
Output enable access time	t_{OE}		8		8		10	ns	
Output hold from address change	t_{OH}	5		5		5		ns	
Output enable to output in high-Z	t_{OHZ}		7		7		7	ns	
Output enable to output in low-Z	t_{OLZ}	1		1		1		ns	
Read cycle time	t_{RC}	15		17		20		ns	(Note 2)
Write Operation									
Address setup time	t_{AS}	0		0		0		ns	
Address valid to end of write	t_{AW}	9		11		12		ns	
Data byte select to end of write	t_{BW}	9		11		12		ns	
Chip select to end of write	t_{CW}	10		11		12		ns	
Data hold time	t_{DH}	0		0		0		ns	
Data valid to end of write	t_{DW}	8		9		10		ns	
Output active from end of write	t_{OW}	3		3		3		ns	(Note 3)
Write enable to output in high-Z	t_{WHZ}	0	7	0	7	0	7	ns	(Note 4)
Write cycle time	t_{WC}	15		17		20		ns	(Note 2)
Write pulse width	t_{WP}	9		10		10		ns	
Write recovery time	t_{WR}	0		0		0		ns	

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall times = 3 ns; timing reference levels = 1.5 V; see figure 1 for output loads.

(2) All read cycle timings are referenced from the last valid address to the first transitioning address.

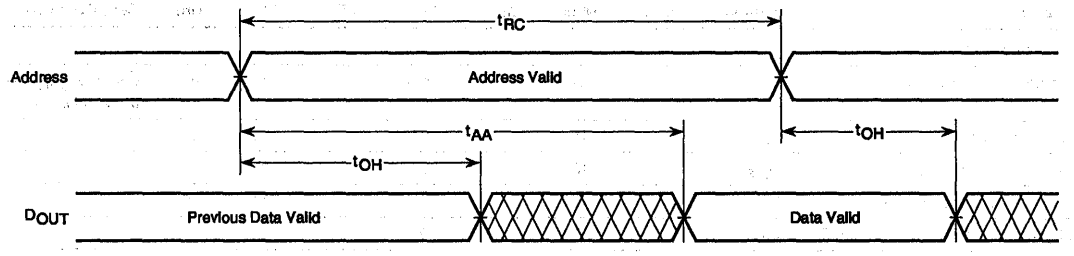
(3) Transition is measured at ±200 mV from steady-state voltage with the load shown in figure 1.

(4) Transition is measured at V_{OL} + 200 mV and V_{OH} – 200 mV with the load shown in figure 1.

(5) I_{CC} = 140 ma max at t_{AA} = 50 ns.

Timing Waveforms

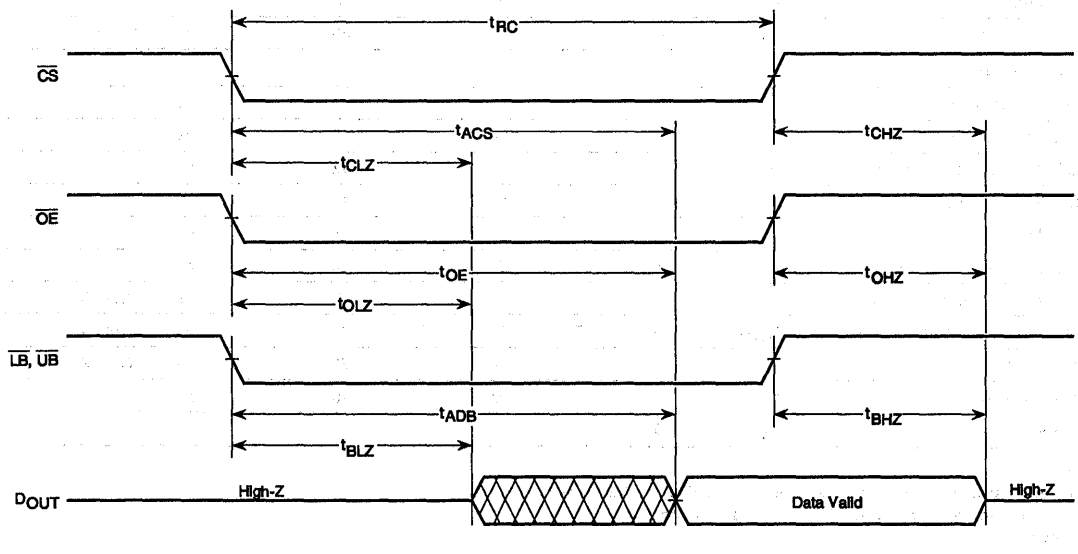
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-6776B

Chip Select Access Cycle

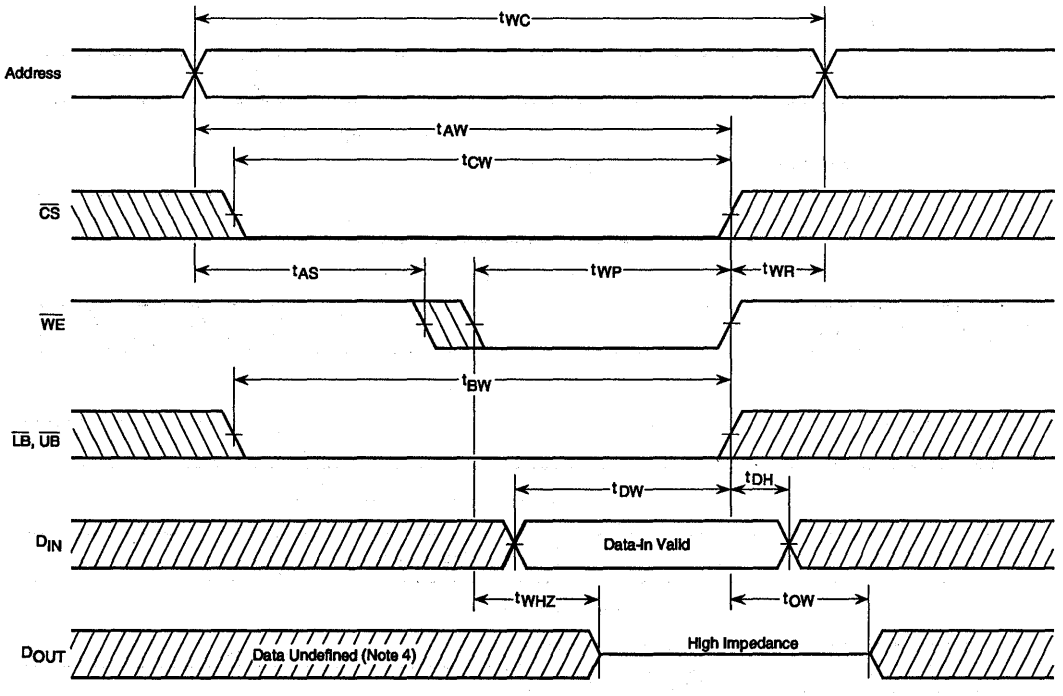


Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Device is continuously selected:
$\overline{CS} = \overline{OE} = \overline{LB} = Low$
$\overline{CS} = \overline{OE} = \overline{UB} = Low$
[3] Address valid prior to or coincident with $\overline{CS}$ transition low.

83IH-8677B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{LB}$ low.

[2] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{UB}$ low.

[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

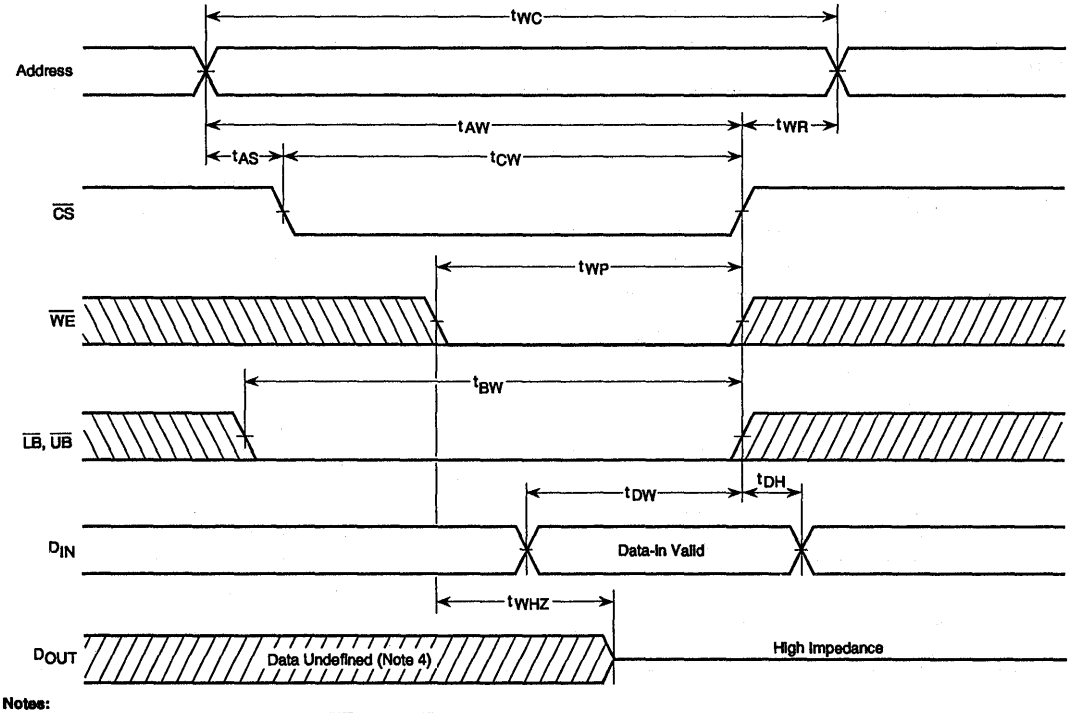
[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

83IH-8678B

21f

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle

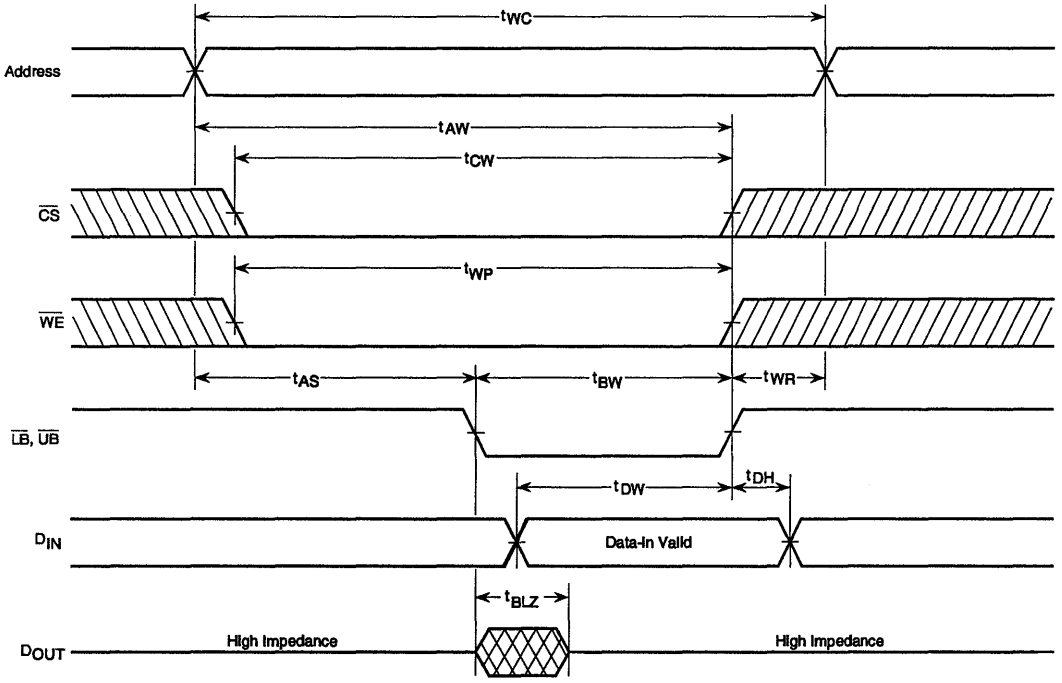


Notes:
[1] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{LB}$ low.
[2] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{UB}$ low.
[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.
[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

83IH-8679B

Timing Waveforms (cont)

$\overline{LB}$/ $\overline{UB}$-Controlled Write Cycle



Notes:

[1] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{LB}$ low.

[2] A write occurs during the overlap of $\overline{CS}$ low, $\overline{WE}$ low, and $\overline{UB}$ low.

[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

83IH-8680B

21f

NEC

Section 22
Fast Static RAMs (4M)

μPD	Organization	Features	
434001	4M x 1	20-ns	22a
434004	1M x 4	20-ns; Output enable	22b
434008	512K x 8	20-ns; Output enable	22c

μPD434001
4,194,304 x 1-Bit
Static CMOS RAM

Description

The μPD434001 is a 4,194,304-word by 1-bit static RAM fabricated with advanced silicon-gate technology. A unique design with CMOS peripheral circuits and N-channel memory cells, the μPD434001 is a high-speed device that requires no clock or refreshing.

Features

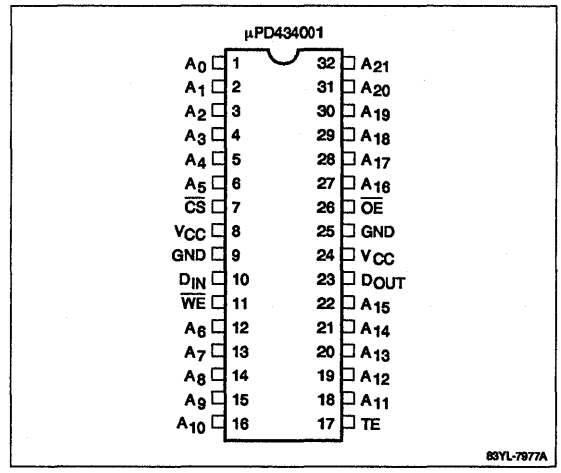
- 4,194,304-word x 1-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Separated data input and output
- Three-state outputs
- Power dissipation
  - — 140 mA max (active)
  - — 10 mA max (standby)
- Standard 400-mil, 32-pin plastic SOJ package

Ordering Information

Part Number	Access Time (max)	Package
μPD434001LE-20	20 ns	32-pin plastic SOJ
LE-25	25 ns	

Pin Configuration

32-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{21}	Address inputs
$\overline{CS}$	Chip select input
D_{IN}	Data input
D_{OUT}	Data output
$\overline{OE}$	Output enable input
TE	Test mode enable input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.5 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) V_{IN} = −3.0 V minimum for 10-ns maximum pulse.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	L	Read	Output data	Active
L	L	X	Write	Data in	Active
L	H	H	Output disable	High-Z	Active

X = don't care

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Output capacitance	C_O			10	pF

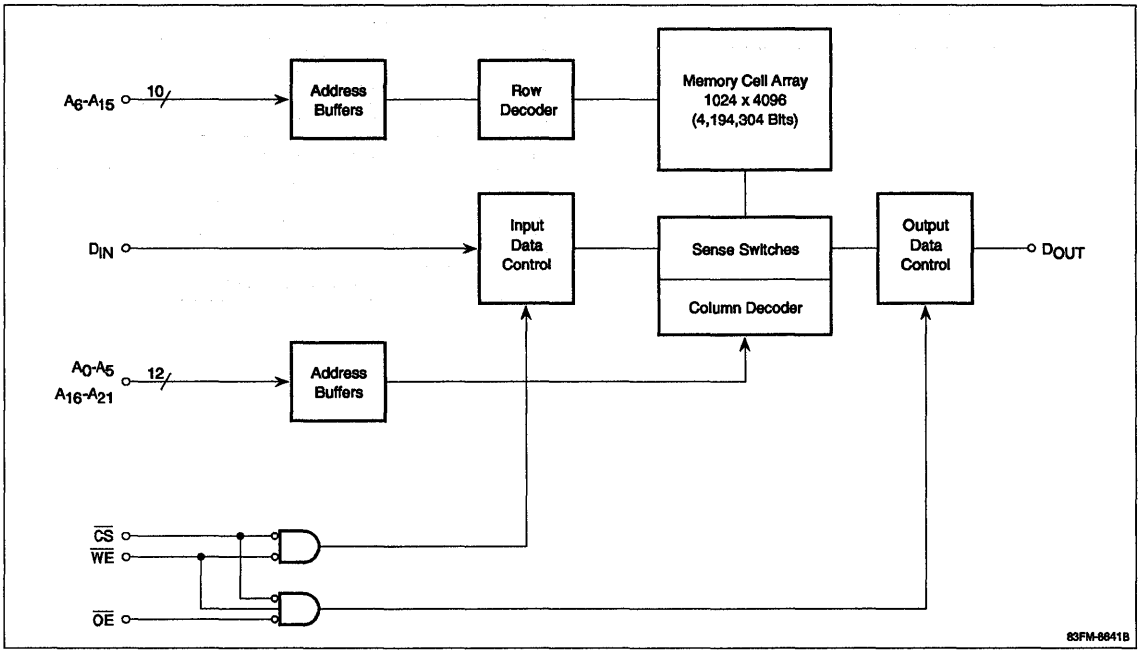
* Capacitance is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

V_{IL} = −2.0 V minimum for 10-ns maximum pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Standby supply current	I_{SB} (-20)			60	mA	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB} (-25)			50	mA	
	I_{SB1}	−25		10	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD434001-20		μPD434001-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating supply current	I_{CC}		140		130	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); I_{OUT} = 0 mA
Read Operation							
Read access time	t_{AA}		20		25	ns	
Chip select access time	t_{ACS}		20		25	ns	
Chip deselect to output in high-Z	t_{CHZ}	0	8	0	10	ns	(Note 4)
Chip select to output in low-Z	t_{CLZ}	3		3		ns	(Note 3)
Output enable access time	t_{OE}		10		12	ns	
Output hold from address change	t_{OH}	3		3		ns	
Output enable to output in high-Z	t_{OHZ}		8		10	ns	
Output enable to output in low-Z	t_{OLZ}		0		0	ns	
Read cycle time	t_{RC}	20		25		ns	(Note 2)
Write Operation							
Address setup time	t_{AS}	0		0		ns	
Address valid to end of write	t_{AW}	14		17		ns	
Chip select to end of write	t_{CW}	14		17		ns	
Data hold time	t_{DH}	0		0		ns	
Data valid to end of write	t_{DW}	10		12		ns	
Output active from end of write	t_{OW}	0		0		ns	(Note 3)
Write cycle time	t_{WC}	20		25		ns	(Note 2)
Write enable to output in high-Z	t_{WHZ}	0	8	0	10	ns	(Note 4)
Write pulse width	t_{WP}	12		15		ns	
Write recovery time	t_{WR}	3		3		ns	

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 5 ns; timing reference levels = 1.5 V; see figure 1 for the output load.

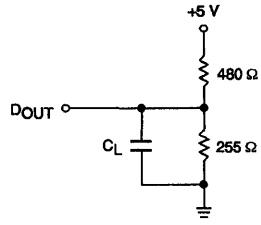
(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the load shown in figure 1.

(4) The transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 1.

22a

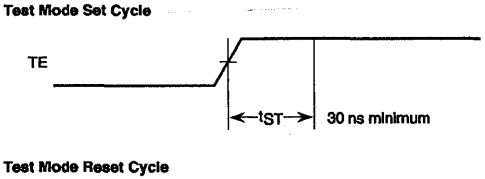
Figure 1. Output Loads



C_L = 30 pF (including scope and test jig)
C_L = 5 pF for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}

83FM-8842A

Figure 2. Test Mode



Notes:

(1) In test mode, the apparent internal memory organization is 512K words by 8 bits.

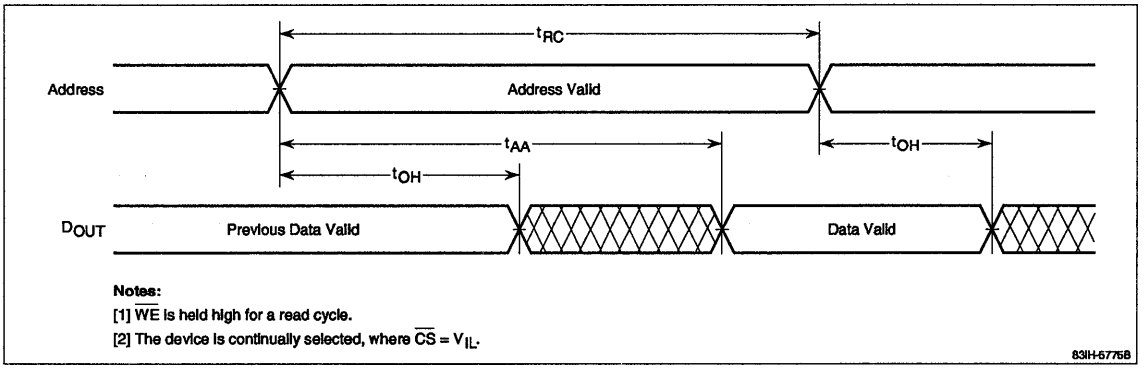
(2) Write the same data (1 or 0) on all 8 bits through pin D_{IN}, addressing pins A_0-A_{18}. Pins A_{19}-A_{21} are "Don't Care."

(3) Read data through pin D_{OUT}. Data output is 1 if correct, 0 if incorrect.

83FM-8843A

Timing Waveforms

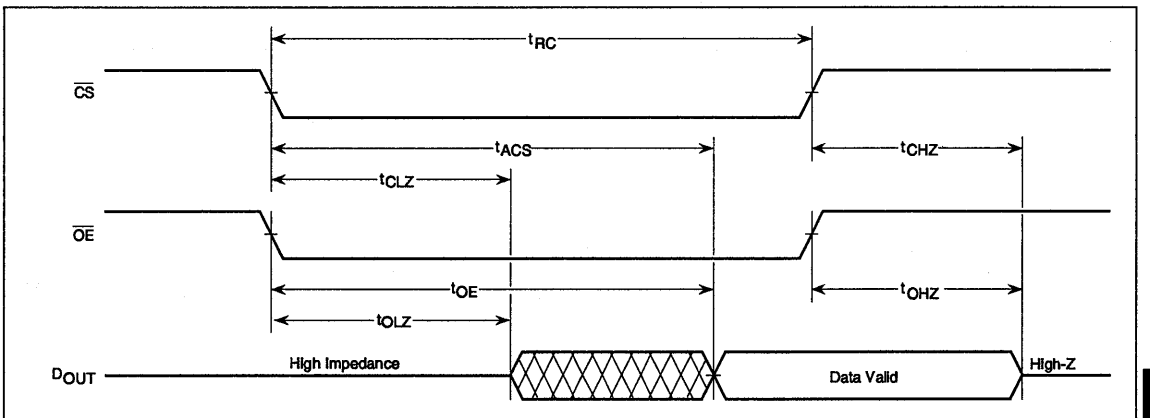
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS}$ = V_{IL}.

83IH-5776B

Chip Select Access Cycle



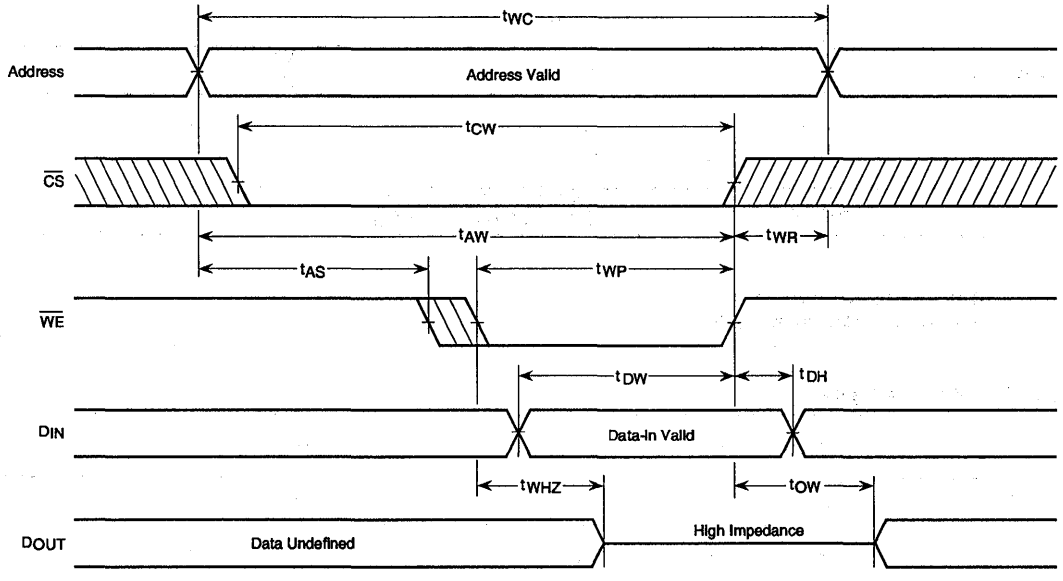
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Device is continuously selected: $\overline{CS}$ = $\overline{OE}$ = Low
[3] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-8644B

22a

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

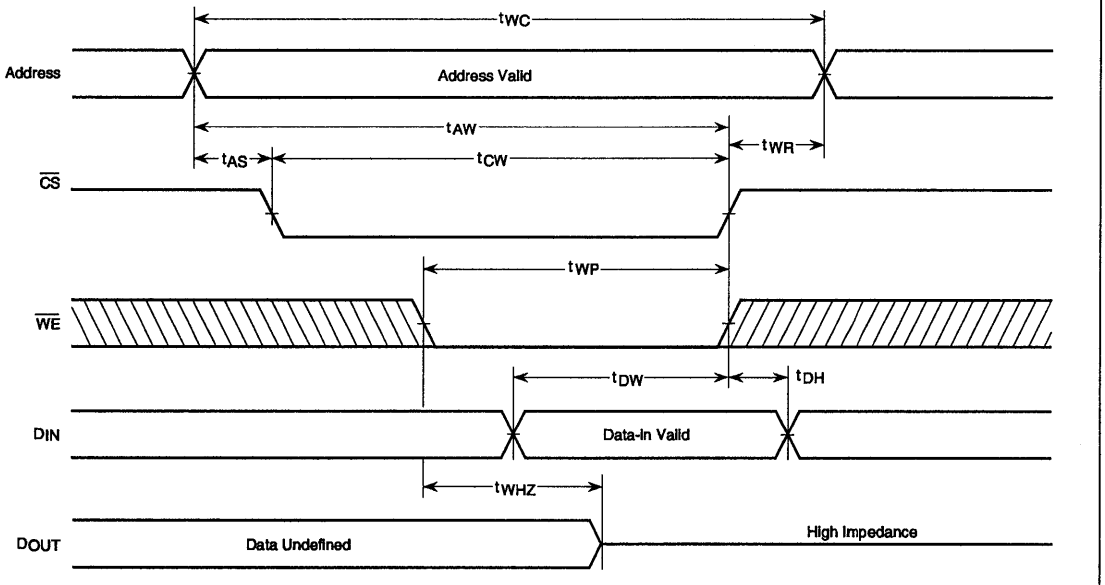
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5777B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5778B

22a

μPD434004
1,048,576 x 4-Bit
Static CMOS RAM

Description

The μPD434004 is a 1,048,576-word by 4-bit static RAM fabricated with advanced silicon-gate technology. A unique design with CMOS peripheral circuits and N-channel memory cells, the μPD434004 is a high-speed device that requires no clock or refreshing.

Features

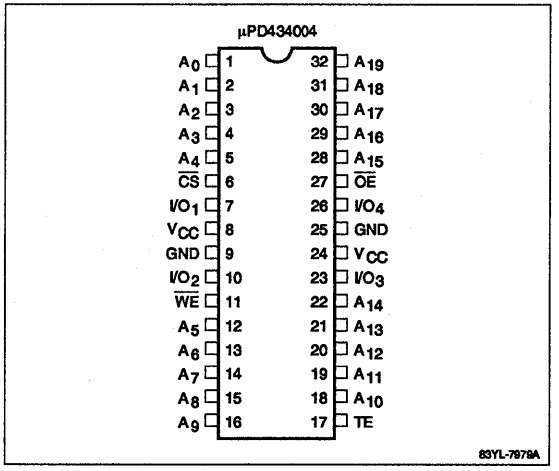
- 1,048,576-word x 4-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- $\overline{OE}$ signal for output control
- Common I/O with three-state outputs
- Power dissipation
  - —150 mA max (active)
  - —10 mA max (standby)
- Standard 400-mil, 32-pin plastic SOJ package

Ordering Information

Part Number	Access Time (max)	Package
μPD434004LE-20	20 ns	32-pin plastic SOJ
LE-25	25 ns	

Pin Configuration

32-Pin Plastic SOJ



Pin Identification

Symbol	Function
A_0 - A_{19}	Address inputs
$\overline{CS}$	Chip select input
I/O_1 - I/O_4	Data input/output
$\overline{OE}$	Output enable input
TE	Test mode enable input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN}	−0.5 to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.5 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

V_{IN} = −2.0 V minimum for 10-ns maximum pulse.

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	L	Read	Output data	Active
L	L	X	Write	Data in	Active
L	H	H	Output disable	High-Z	Active

X = don't care

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter*	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Output capacitance	C_O			10	pF

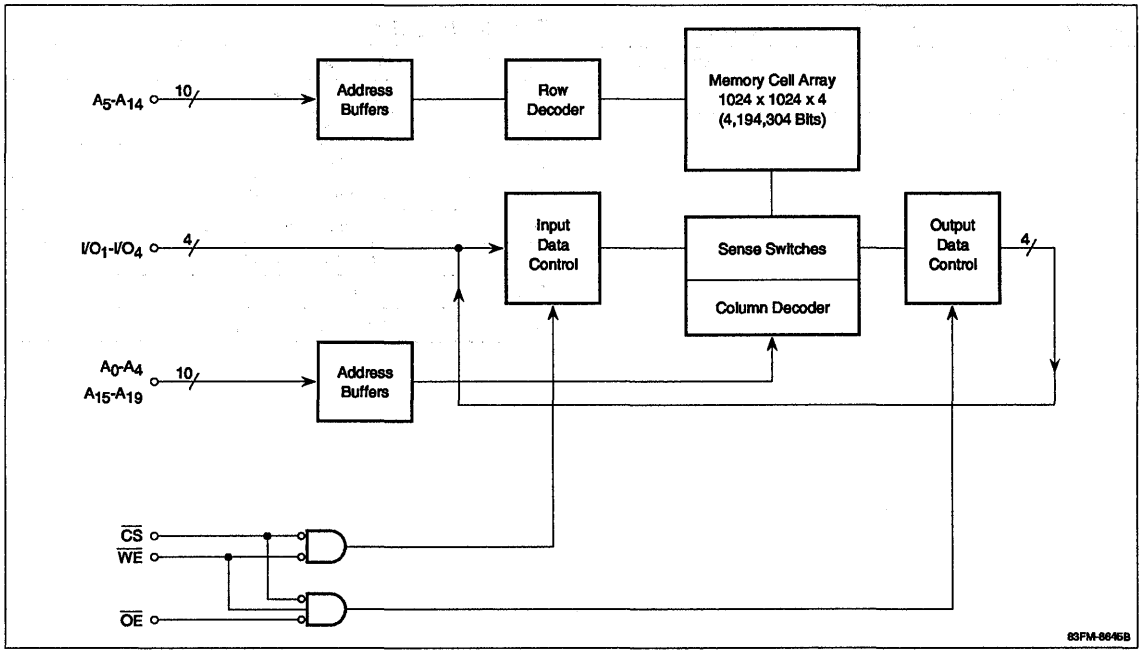
* Capacitance is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		+70	°C

V_{IL} = −2.0 V minimum for 10-ns maximum pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Standby supply current	I_{SB} (-20)			60	mA	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB} (-25)			50	mA	
	I_{SB1}			10	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD434004-20		μPD434004-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Operating supply current	I_{CC}		150		140	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); I_{OUT} = 0 mA
Read Operation							
Read access time	t_{AA}		20		25	ns	
Chip select access time	t_{ACS}		20		25	ns	
Chip deselect to output in high-Z	t_{CHZ}	0	8	0	10	ns	(Note 4)
Chip select to output in low-Z	t_{CLZ}	3		3		ns	(Note 3)
Output enable access time	t_{OE}		10		12	ns	
Output hold from address change	t_{OH}	3		3		ns	
Output enable to output in high-Z	t_{OHZ}		8		10	ns	
Output enable to output in low-Z	t_{OLZ}		0		0	ns	
Read cycle time	t_{RC}	20		25		ns	(Note 2)
Write Operation							
Address setup time	t_{AS}	0		0		ns	
Address valid to end of write	t_{AW}	14		17		ns	
Chip select to end of write	t_{CW}	14		17		ns	
Data hold time	t_{DH}	0		0		ns	
Data valid to end of write	t_{DW}	10		12		ns	
Output active from end of write	t_{OW}	0		0		ns	(Note 3)
Write cycle time	t_{WC}	20		25		ns	(Note 2)
Write enable to output in high-Z	t_{WHZ}	0	8	0	10	ns	(Note 4)
Write pulse width	t_{WP}	12		15		ns	
Write recovery time	t_{WR}	3		3		ns	

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 5 ns; timing reference levels = 1.5 V; see figure 1 for the output load.

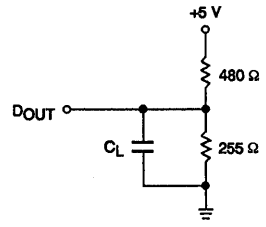
(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the load shown in figure 1.

(4) The transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 1.

22b

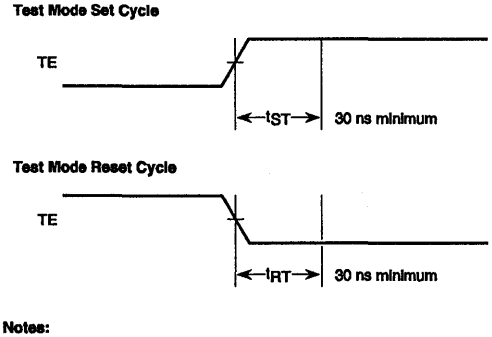
Figure 1. Output Loads



C_L = 30 pF (including scope and test jig)
C_L = 5 pF for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}

83FM-8642A

Figure 2. Test Mode



Notes:

(1) In test mode, the apparent internal memory organization is 512K words by 8 bits.

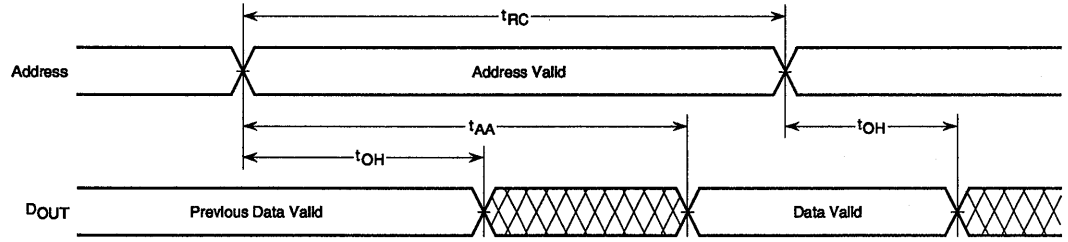
(2) Write the same data (1 or 0) on all 8 bits through pins I/O_1-I/O_4, writing 2 bits on each I/O and addressing pins A_0-A_{18}. Pin A_{19} is "Don't Care."

(3) Read data through pins I/O_1-I/O_4. Data output is 1 if 2 bits are correct, 0 if incorrect.

83FM-8903A

Timing Waveforms

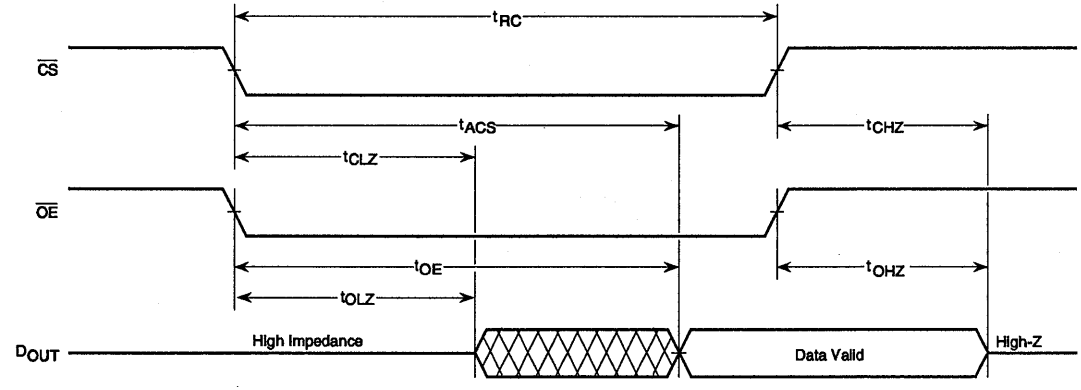
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-5775B

Chip Select Access Cycle



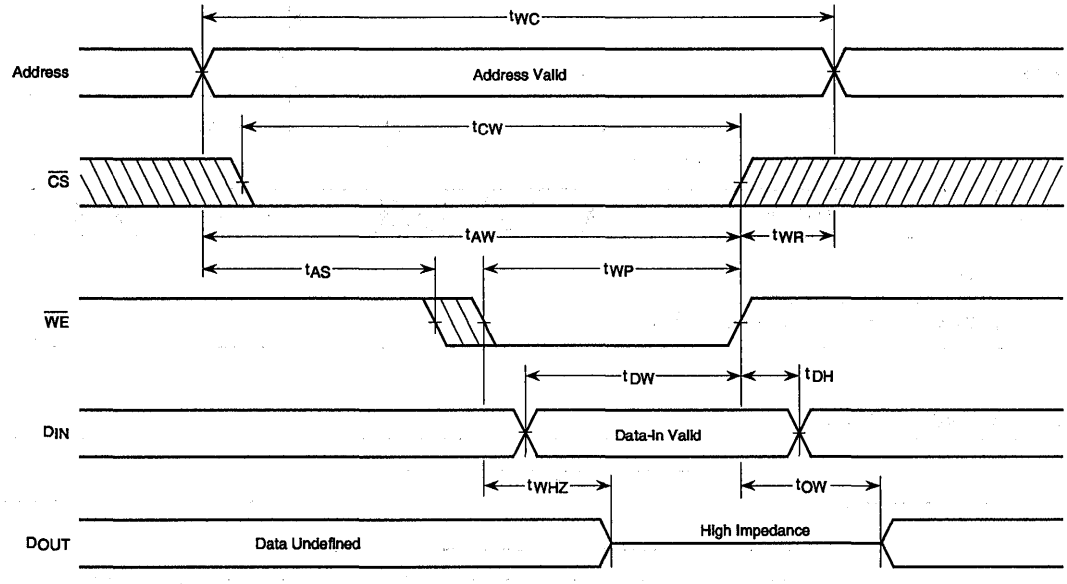
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Device is continuously selected: $\overline{CS} = \overline{OE}$ = Low
[3] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-8644B

22b

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

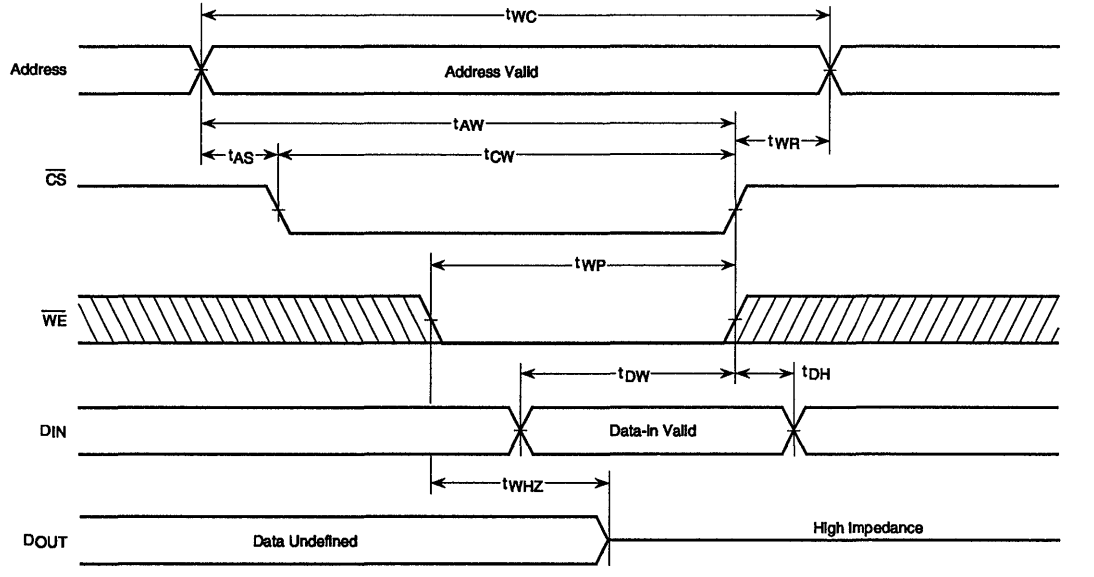
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-6777B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5778B

22b

μPD434008
524,288 x 8-Bit
Static CMOS RAM

Description

The μPD434008 is a 524,288-word by 8-bit static RAM fabricated with advanced silicon-gate technology. A unique design with CMOS peripheral circuits and N-channel memory cells, the μPD434008 is a high-speed device that requires no clock or refreshing. The device is available in a 36-pin plastic SOJ package.

Features

- 524,288-word x 8-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Chip select and output enable for easy application
- Common I/O with three-state outputs
- Power dissipation
  - — 190 mA max (active)
  - — 10 mA max (standby)
- Standard 400-mil, 36-pin plastic SOJ package

Ordering Information

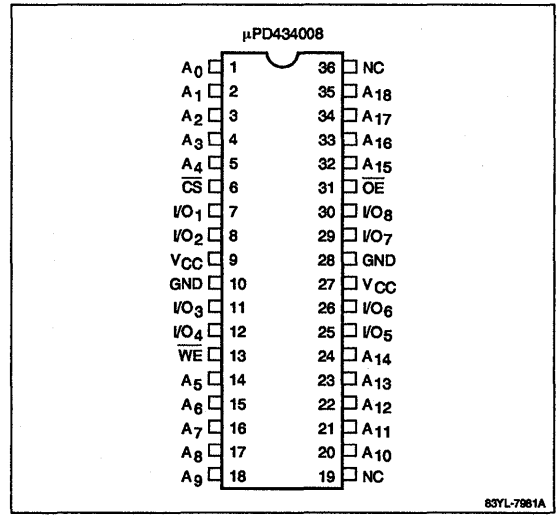
Part Number	Access Time (max)	Package
μPD434008LE-20	20 ns	36-pin plastic SOJ
LE-25	25 ns	

Pin Identification

Symbol	Function
A_0 - A_{18}	Address inputs
$\overline{CS}$	Chip select input
I/O_1 - I/O_8	Data input/output
$\overline{OE}$	Output enable input
$\overline{WE}$	Write enable input
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configuration

36-Pin Plastic SOJ



22c

Absolute Maximum Ratings

Power supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.3 V
Output voltage, V_{OUT}	−0.5 to V_{CC} + 0.3 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) V_{IN} = −2.0 V minimum for 10-ns maximum pulse.

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	L	Read	Output data	Active
L	L	X	Write	Data in	Active
L	H	H	Output disable	High-Z	Active

X = don't care

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Output capacitance	C_O			10	pF

Note:

(1) This parameter is sampled and not 100% tested.

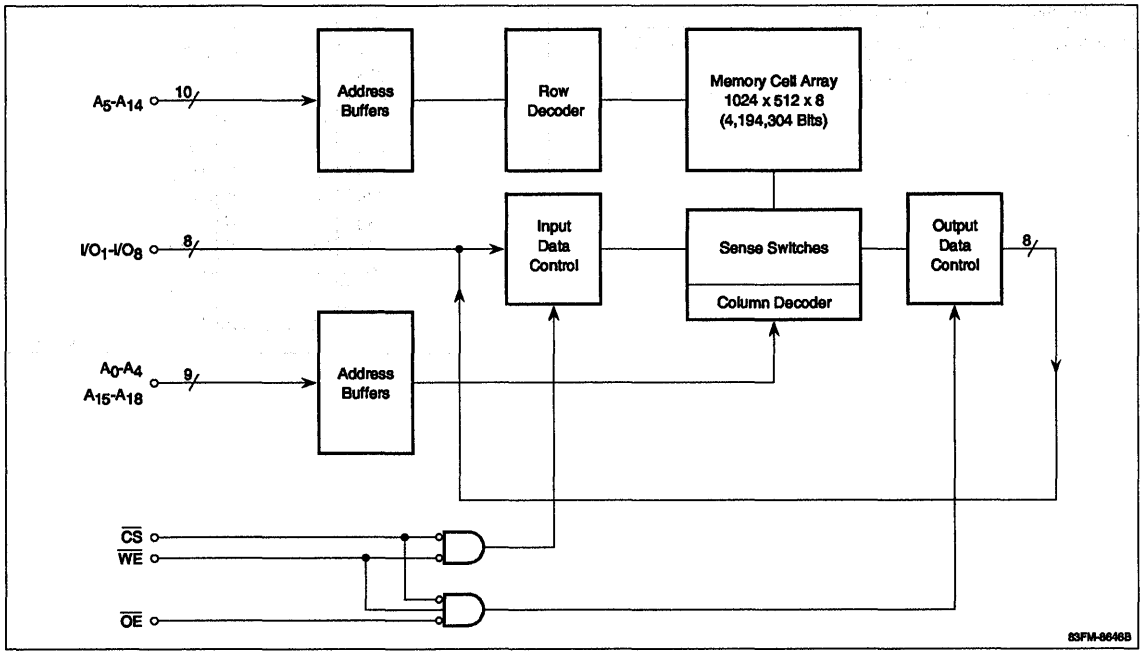
Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.5		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Note:

(1) V_{IL} = −2.0 V minimum for 10-ns maximum pulse.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Operating supply current	I_{CC} (Note 1)			190	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); I_{OUT} = 0 mA
Standby supply current	I_{SB} (Note 2)			60	mA	$\overline{CS}$ = V_{IH}; V_{IN} = V_{IH} or V_{IL}
	I_{SB1}			10	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V; V_{IN} ≤ 0.2 V or ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8.0 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA

Notes:

(1) I_{CC} = 170 mA (max) for the μPD434008-25.

(2) I_{SB} = 50 mA (max) for the μPD434008-25.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD434008-20		μPD434008-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Read access time	t_{AA}		20		25	ns	
Chip select access time	t_{ACS}		20		25	ns	
Chip deselect to output in high-Z	t_{CHZ}	0	8	0	10	ns	(Note 4)
Chip select to output in low-Z	t_{CLZ}	3		3		ns	(Note 3)
Output enable access time	t_{OE}		10		12	ns	
Output hold from address change	t_{OH}	3		3		ns	
Output enable to output in high-Z	t_{OHZ}		8		10	ns	
Output enable to output in low-Z	t_{OLZ}		0		0	ns	
Read cycle time	t_{RC}	20		25		ns	(Note 2)
Write Operation							
Address setup time	t_{AS}	0		0		ns	
Address valid to end of write	t_{AW}	14		15		ns	
Chip select to end of write	t_{CW}	14		15		ns	
Data hold time	t_{DH}	0		0		ns	
Data valid to end of write	t_{DW}	10		12		ns	
Output active from end of write	t_{OW}	0		0		ns	(Note 3)
Write cycle time	t_{WC}	20		25		ns	(Note 2)
Write enable to output in high-Z	t_{WHZ}	0	8	0	10	ns	(Note 4)
Write pulse width	t_{WP}	12		15		ns	
Write recovery time	t_{WR}	3		3		ns	

Notes:

(1) Input pulse levels = GND to 3.0 V; input pulse rise and fall time = 3 ns; timing reference levels = 1.5 V; see figure 1 for the output load.

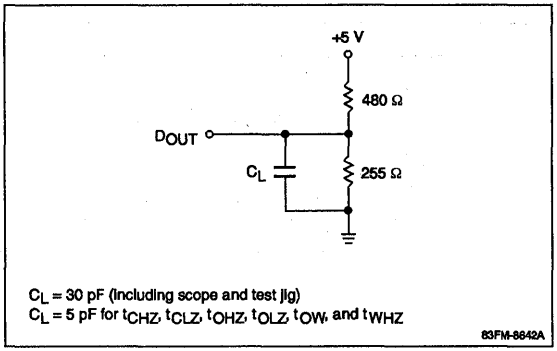
(2) All read and write cycle timings are referenced from the last valid address to the first transitioning address.

(3) The transition is measured ±200 mV from steady-state voltage with the load shown in figure 1.

(4) The transition is measured at V_{OL} + 200 mV and V_{OH} − 200 mV with the load shown in figure 1.

22c

Figure 1. Output Loads

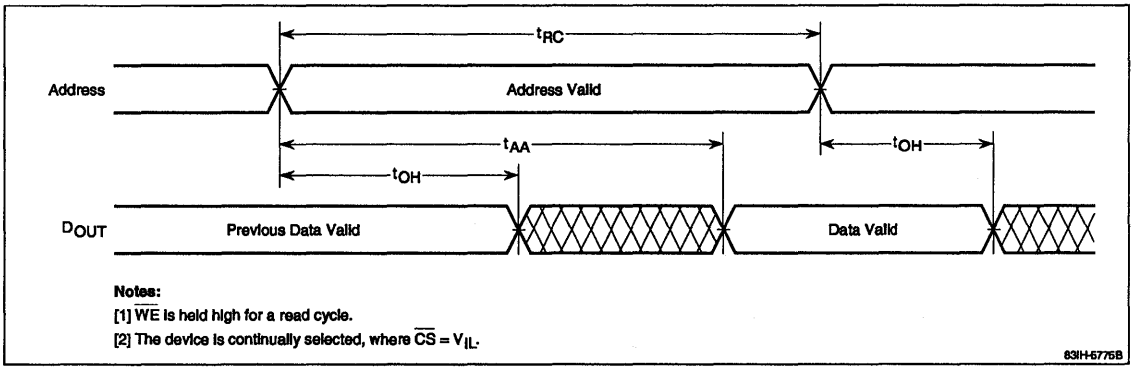


C_L = 30 pF (including scope and test jig)
C_L = 5 pF for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}

83FM-8642A

Timing Waveforms

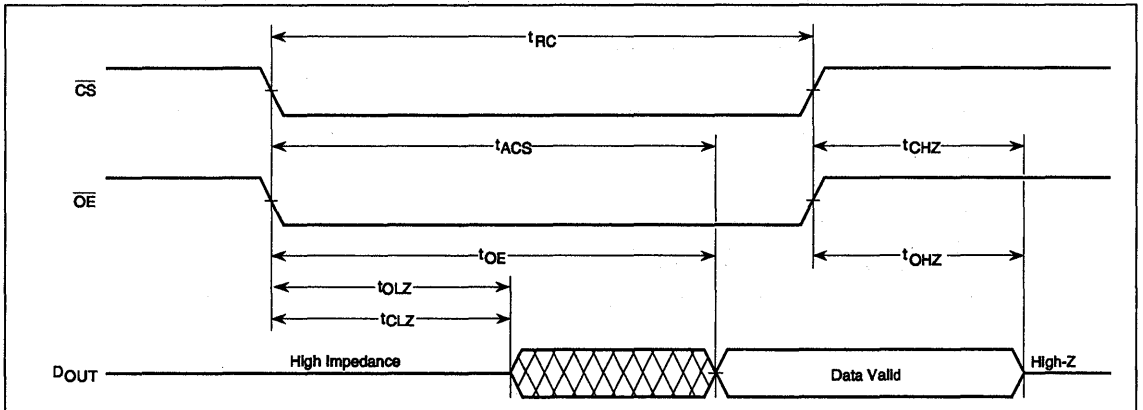
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = V_{IL}$.

83IH-6776B

Chip Select Access Cycle



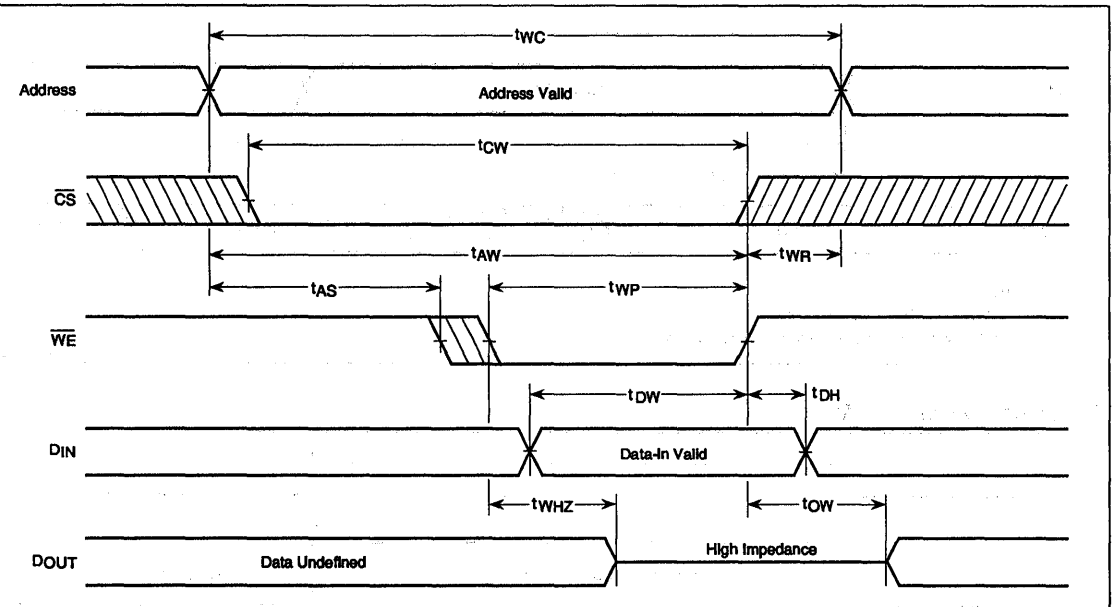
Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] Device is continuously selected: $\overline{CS} = \overline{OE}$ = Low
[3] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-8644B

22c

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

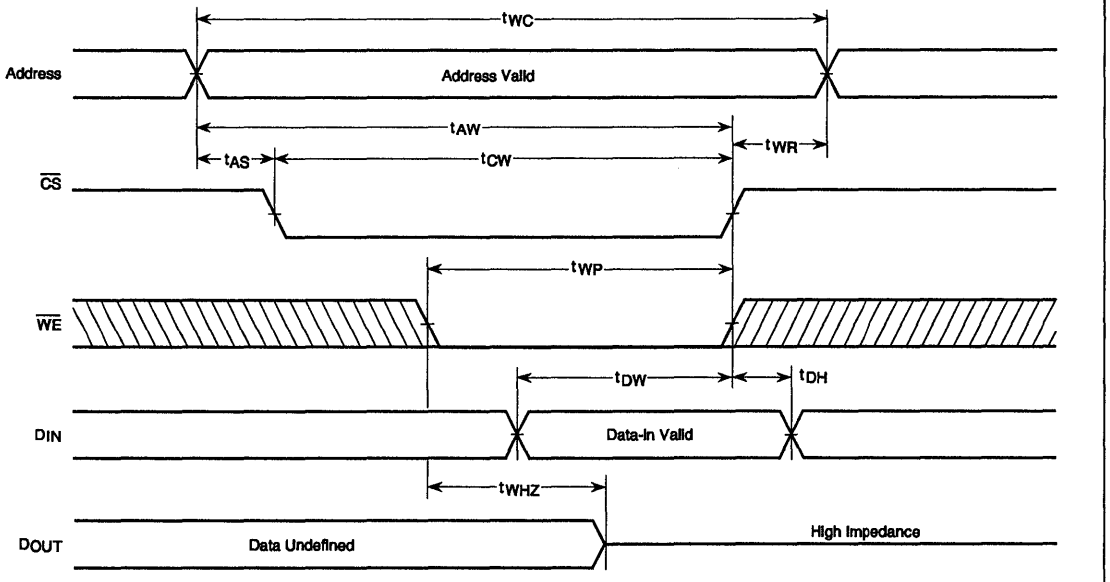
[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-6777B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[2] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[3] t_{WR} is measured between $\overline{CS}$ or $\overline{WE}$, whichever rising edge occurs first, and the end of t_{WC}.

83IH-5778B

22c

NEC

Section 23
Cache Data RAMs

μPD	Organization	Features	
46710A	16K x 10 bit x 2	Cache data; 12-ns	23a
46741A	8K x 20 bit x 2	Cache data; 12-ns	23b

μPD46710A
16,384 x 10-Bit x 2
Static BiCMOS RAM

Description

The μPD46710A is a high-performance static BiCMOS RAM organized as 16,384 x 10 bits x 2 and designed for use as a high-speed cache memory. The μPD46710A integrates two 16,384 x 10-bit SRAM cores with associated address latches and control signals that can be used to implement an instruction/data cache for 25- and 33-MHz VR3000™ RISC systems.

Features

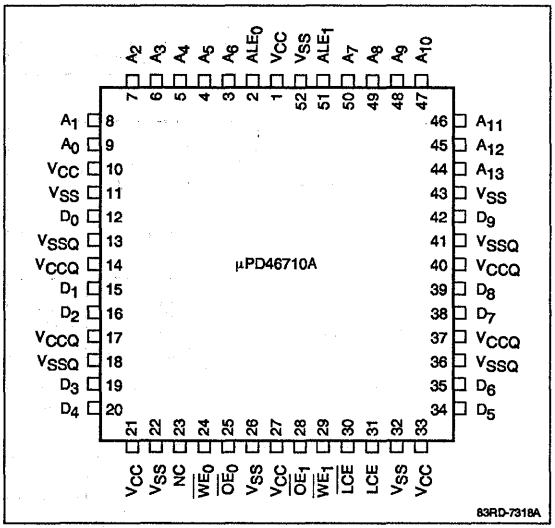
- Fast access time: 12 or 15 ns
- 16,384 x 10-bit x 2 organization
- On-chip address latches
- On-chip instruction/data caches
- Fully static read/write operation
- TTL-compatible inputs and outputs
- 52-pin PLCC package

Ordering Information

Part Number	Access Time	Output Enable Time	Package
μPD46710ALN-12	12 ns	4.5 ns	52-pin PLCC
LN-15	15 ns	7 ns	

Pin Configuration

52-Pin PLCC



Pin Identification

Symbol	Function
A_0 - A_{13}	Addresses
ALE_0 and ALE_1	Address latch enable inputs
D_0 - D_9	Data inputs/outputs
LCE and $\overline{LCE}$	Latch chip enable inputs
$\overline{OE}_0$ and $\overline{OE}_1$	Output enable inputs
$\overline{WE}_0$ and $\overline{WE}_1$	Write enable inputs
V_{CC} and V_{CCQ}	+5-volt power supply
V_{SS} and V_{SSQ}	Ground
NC	No connection

VR3000 is a trademark of NEC Corporation.

Block Diagram

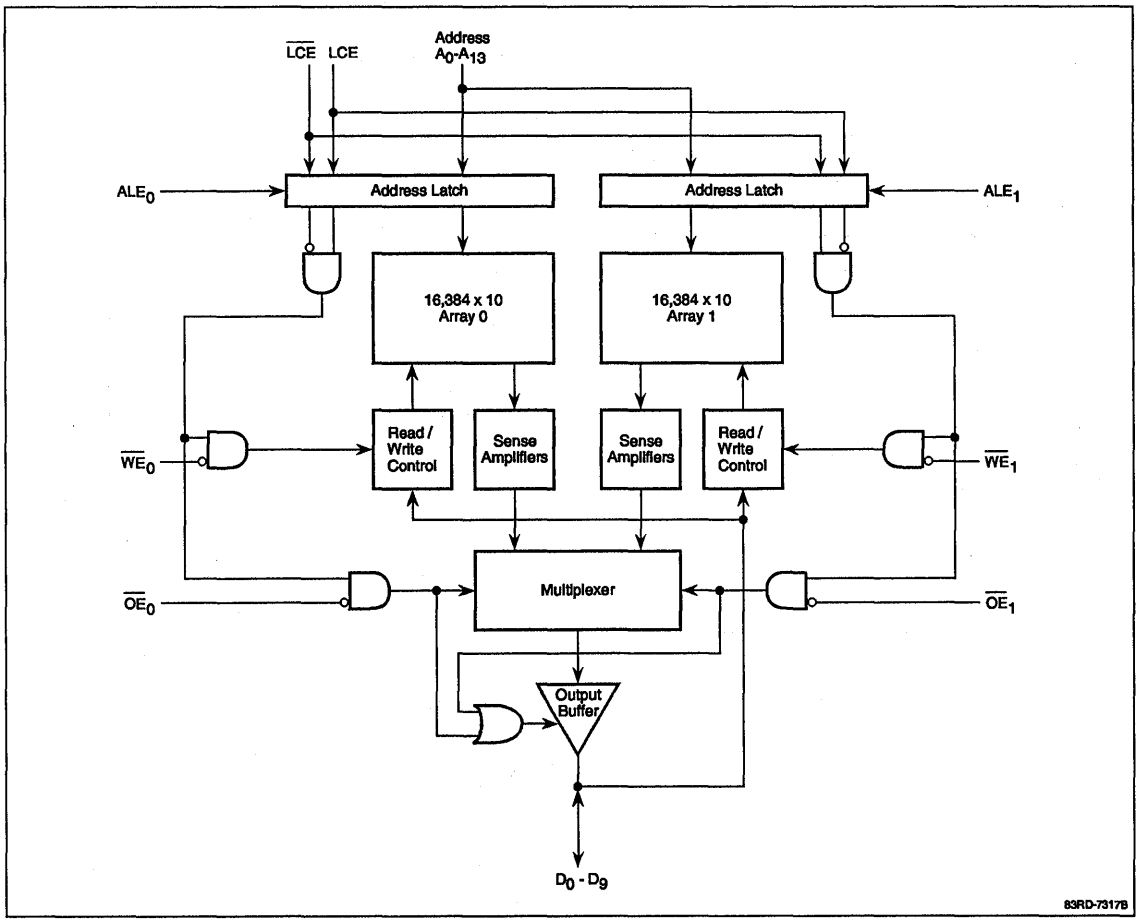
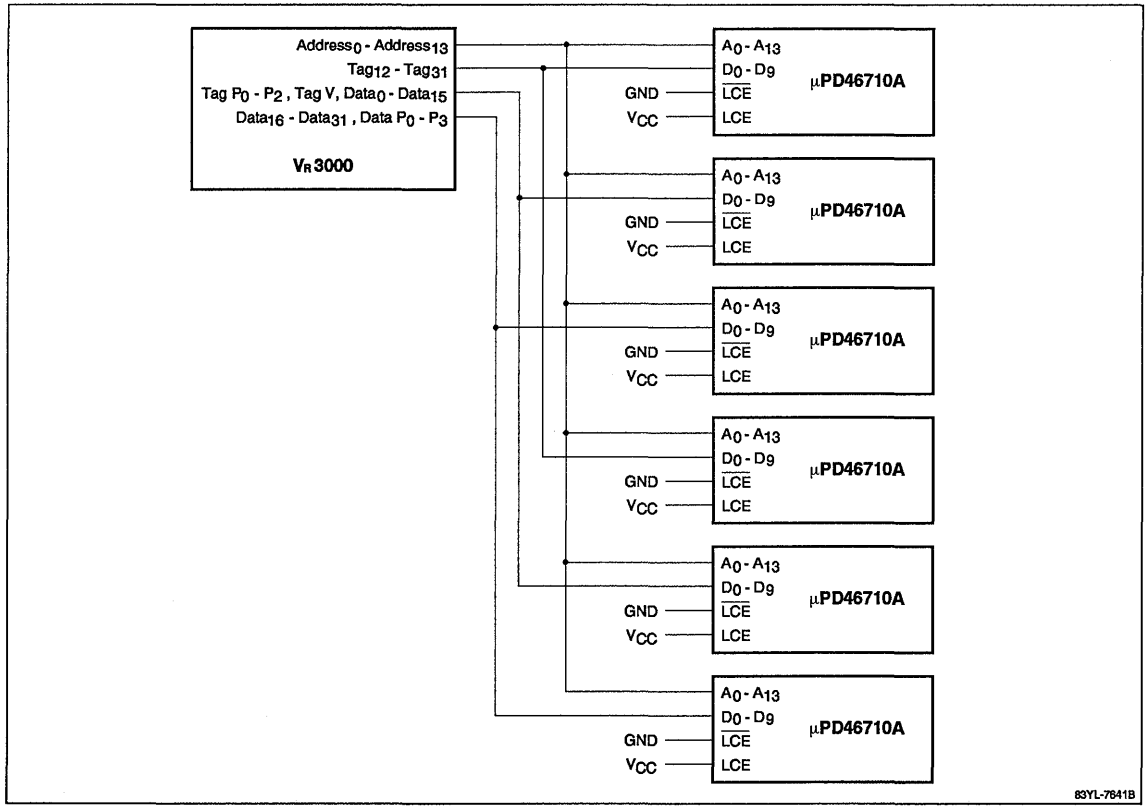


Figure 1. 64K-Byte Cache System



Functional Operation

The μPD46710A integrates two 16K x 10 SRAM cores with associated address latches and control logic to be used as an instruction/data cache in a high-speed VR3000 RISC processor. In this system, the CPU initiates a μPD46710A memory cycle by outputting an address to one of the two memory arrays. The signals on address lines A_0 - A_{13} are latched onto the address latch of array 0 at the rising edge of ALE_0 while ALE_1 is inactive low. The CPU executes a read cycle on array 0 and initiates the next memory operation. Memory array 1 is then accessed by latching the CPU address at the rising edge of ALE_1 with ALE_0 inactive low.

To read data from memory array 0, $\overline{OE}_0$ is driven active low while $\overline{WE}_0$, $\overline{WE}_1$, and $\overline{OE}_2$ remain inactive high. Data in memory array 1 is read by driving $\overline{OE}_1$ low with $\overline{OE}_0$, $\overline{WE}_0$, and $\overline{WE}_1$ inactive high.

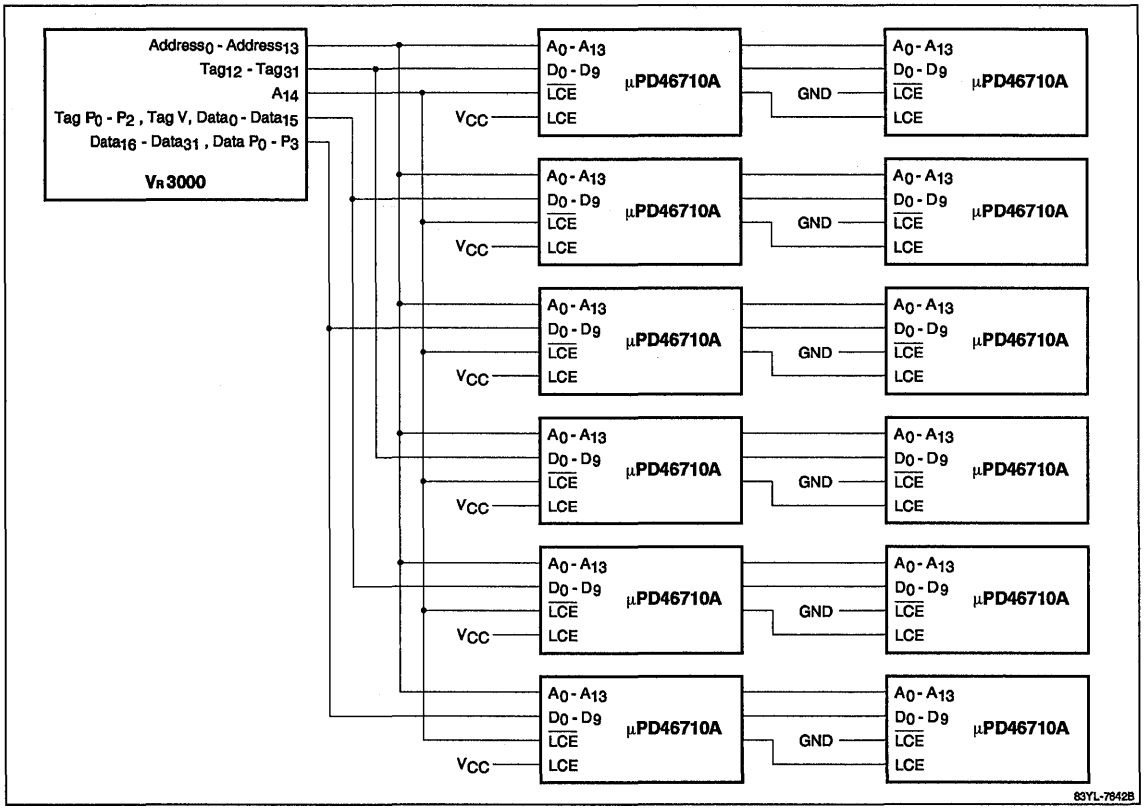
The $\overline{WE}_0$ and $\overline{WE}_1$ signals control write cycles into each of the two memory arrays. Data is written into memory array 0 by driving write data on data lines D_0 - D_9 with $\overline{WE}_0$ active low. In a similar manner, the $\overline{WE}_1$ signal controls write cycles into memory array 1.

The LCE and $\overline{LCE}$ latch chip enable signals provide a decoding function that can be used to increase the size of the VR3000 cache memory. A 64K-byte cache (figure 1) can be implemented using six μPD46710As with LCE and $\overline{LCE}$ connected to V_{CC} and GND, respectively.

Cache size can be increased to 128K bytes (figure 2) using two banks of six μPD46710As. In this case, address signal A_{14} is used to decode the two 64K-byte memory banks. $\overline{LCE}$ of the first bank is connected to address A_{14} and LCE is connected to V_{CC}. LCE of the second bank is connected to A_{14} with $\overline{LCE}$ grounded.

23a

Figure 2. 128K-Byte Cache System



Truth Table

Function	LCE	$\overline{LCE}$	$\overline{WE_0}$	$\overline{WE_1}$	$\overline{OE_0}$	$\overline{OE_1}$	Output
Not selected	L	L	X	X	X	X	High-Z
Not selected	L	H	X	X	X	X	High-Z
Not selected	H	H	X	X	X	X	High-Z
Read RAM array 0 data	H	L	H	H	L	H	Read data
Read RAM array 1 data	H	L	H	H	H	L	Read data
Output high-Z	H	L	H	H	H	H	High-Z
(Note 1)	H	L	H	H	L	L	High-Z
Write data into RAM array 0	H	L	L	H	X	X	Write data
Write data into RAM array 1	H	L	H	L	X	X	Write data
Write same data into both RAM arrays. (Note 2)	H	L	L	L	X	X	Write data

Notes:

(1) Not recommended for use because of multiselection in the multiplexer circuit.

(2) Not recommended for use because of increasing ac power during write operation.

(3) X = don't care.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN}	−0.5 to + 7.0 V
Output voltage, V_{OUT}	−0.5 to + 7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5 *		0.8	V
Ambient temperature	T_A	0		+70	°C

* V_{IL} = −2.0 V min for 20-ns maximum pulse.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter*	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			6	pF
Input/output capacitance	$C_{I/O}$			8	pF

* These parameters are sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_O = 0 V to V_{CC}
Operating supply current*	I_{CCA}			300	mA	V_O = open; V_{CC} = max; f = $2/t_{RC}$
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA; V_{CC} = min
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA; V_{CC} = min

* Applicable to two SRAM cores operating at maximum frequency.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD46710A-12		μPD46710A-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Address access time	t_{AA}		12		15	ns	
Address hold time for ALE_0 and ALE_1	t_{AHLL}	2		2		ns	(Note 3)
Latched chip enable access time	t_{ALCE}		12		15	ns	
ALE access time	t_{ALEA}	1	14	1	17	ns	
Address latch enable pulse width	t_{AP}	6		8		ns	
Address setup time for ALE_0 and ALE_1	t_{ASLL}	4		4		ns	(Note 4)
Latched chip enable to output in high-Z	t_{CHZ}	1	6	2	7	ns	(Note 1)
Latched chip enable to output in low-Z	t_{CLZ}	1		2		ns	(Note 1)
Output enable to output valid	t_{OE}		4.5		6	ns	(Note 5)
Output hold from address change	t_{OH}	3		3		ns	
$\overline{OE}$ to output in high-Z	t_{OHZ}	0	4	0	6	ns	(Note 1)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		ns	
Output enable overlap time	t_{OO}	1		1		ns	
Read cycle time	t_{RC}	15		20		ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD46710A-12 Min	μPD46710A-12 Max	μPD46710A-15 Min	μPD46710A-15 Max	Unit	Test Conditions
Write Operation							
Address hold time for ALE_0 and ALE_1	t_{AHLL}	2		2		ns	(Note 3)
ALE setup time prior to end of write	t_{ALES}	2		2		ns	
ALE setup time to end of write	t_{ALEW}	17		17		ns	
Address latch enable pulse width	t_{AP}	6		8		ns	
Address setup time	t_{AS}	2		2		ns	
Address setup time for ALE_0 and ALE_1	t_{ASLL}	4		4		ns	(Note 4)
Address valid to end of write	t_{AW}	12		15		ns	
Address latch enable hold time after write	t_{AWH}	0		0		ns	
Latched chip enable to end of write	t_{CW}	12		15		ns	
Data hold time	t_{DH}	0		0		ns	(Note 8)
Data valid to end of write	t_{DW}	5		7		ns	(Note 7)
Output enable to end of write	t_{OEW}	0		0		ns	(Note 6)
Output disable to write enable	t_{ODW}	2		2		ns	
Write cycle time	t_{WC}	12		15		ns	
Write pulse width	t_{WP}	7		10		ns	
Write recovery time	t_{WR}	2		3		ns	

Notes:

(1) This transition is measured ±200 mV from steady-state with the output load in figure 3.

(2) Input pulse levels = 0.8 to 2.4 V; input pulse rise and fall times ≤ 3 ns; see figure 3.

(3) t_{AHLL} = 1.5 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

(4) t_{ASLL} = 3 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

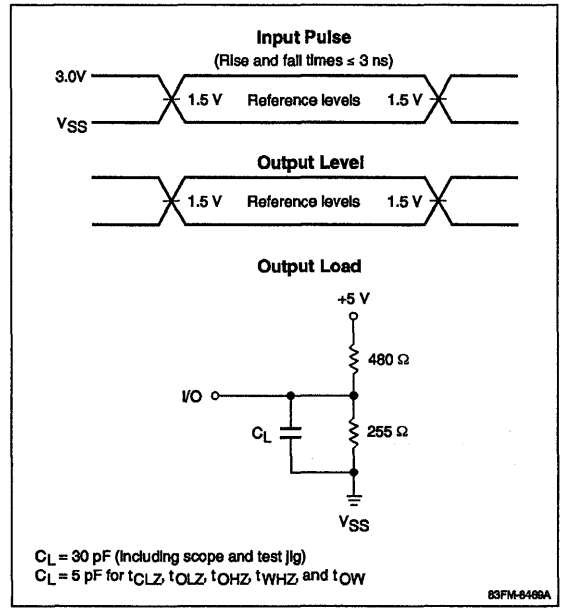
(5) t_{OE} = 4 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

(6) $\overline{OE}_n$, $\overline{WE}_m$ (n = 0 or 1, m = 0 or 1)
t_{OEW} = 0 ns min at n ≠ m
= 2 ns min at n = m

(7) t_{DW} = 4 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

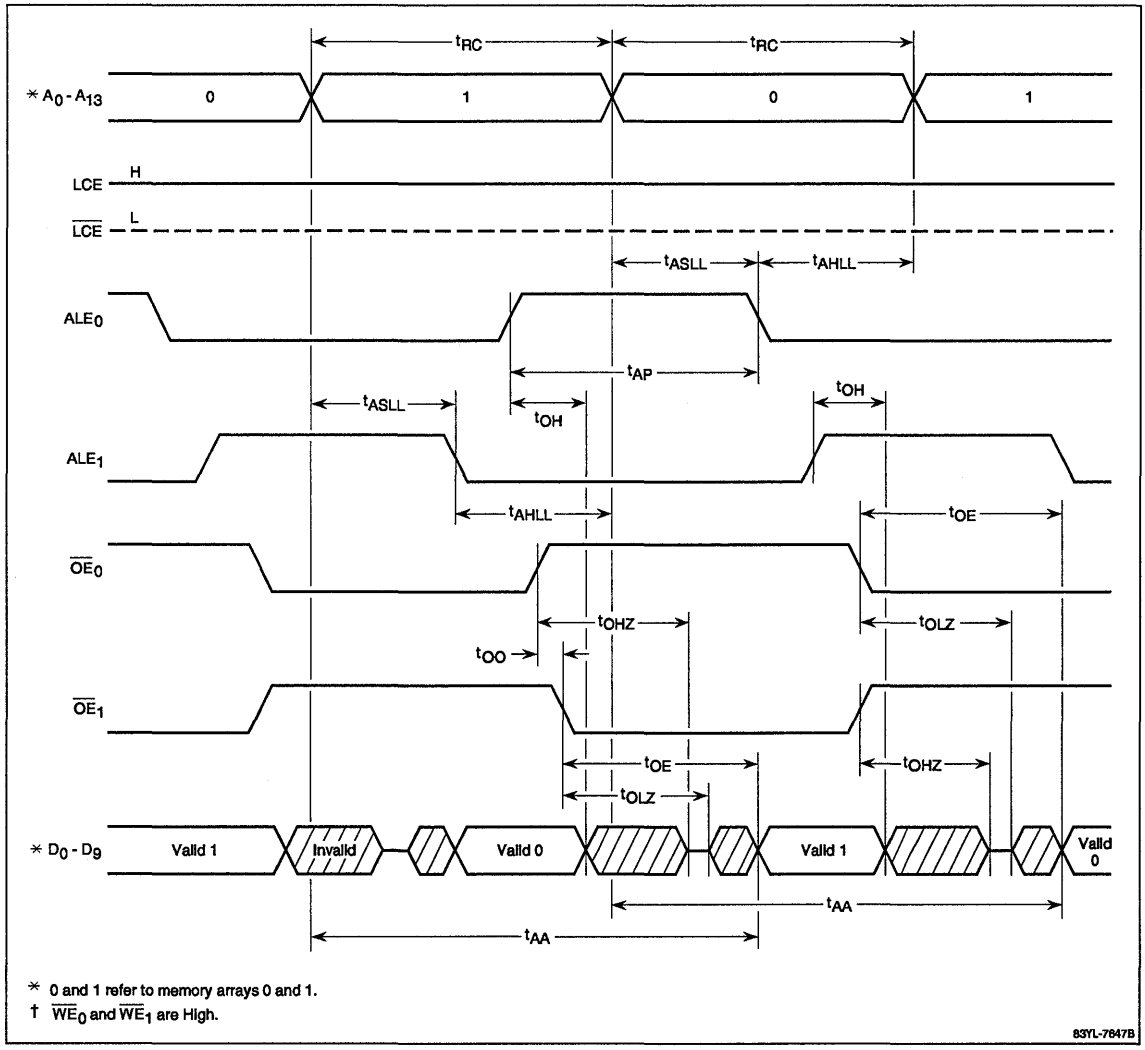
(8) t_{DH} = 0.5 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

Figure 3. AC Test Conditions



Timing Waveforms

Read Cycle (LCE High)



* 0 and 1 refer to memory arrays 0 and 1.

† $\overline{WE}_0$ and $\overline{WE}_1$ are High.

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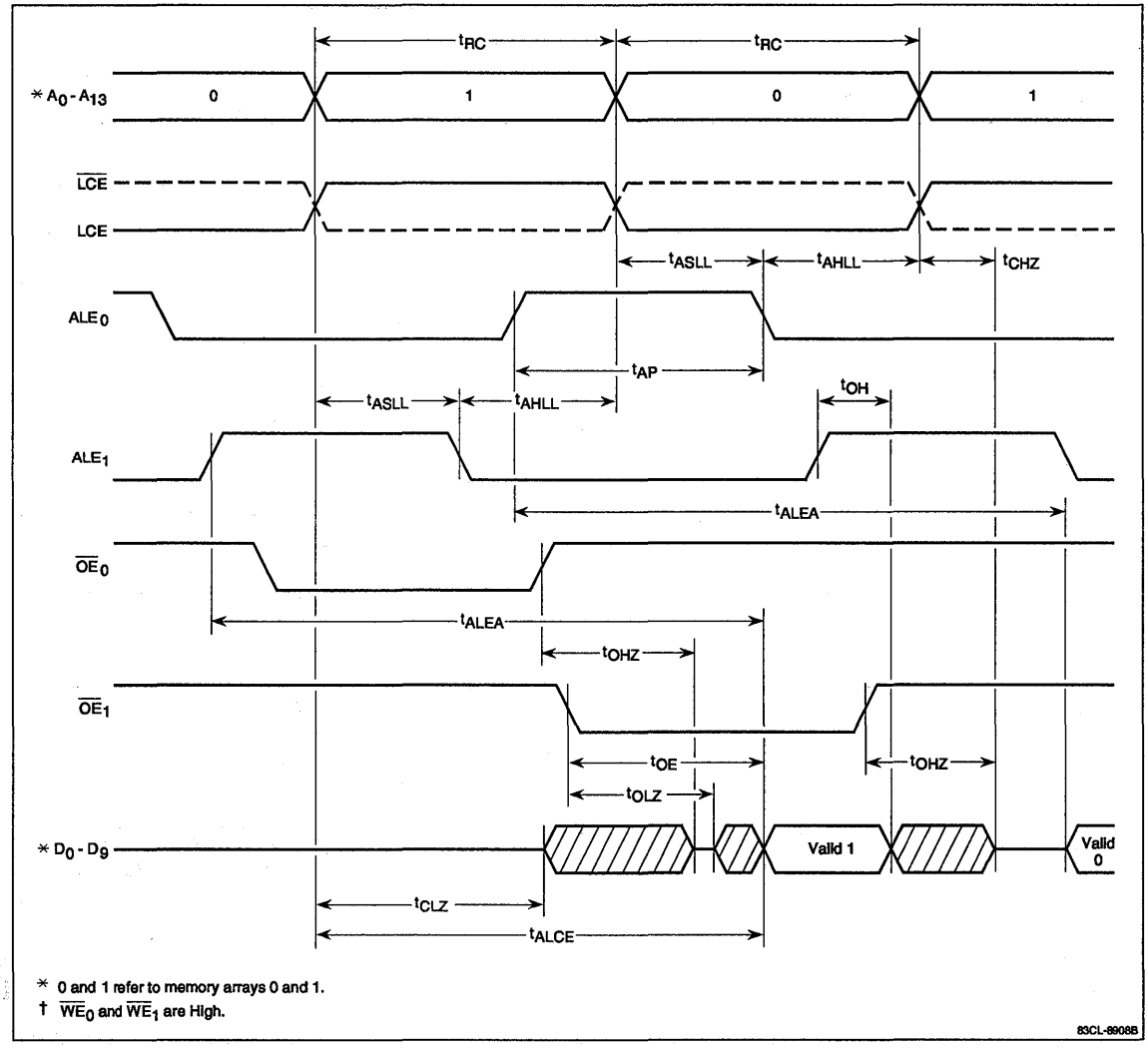
Timing Waveforms (cont)

Read Cycle (LCE = Address)



* 0 and 1 refer to memory arrays 0 and 1.
† $\overline{WE_0}$ and $\overline{WE_1}$ are High.

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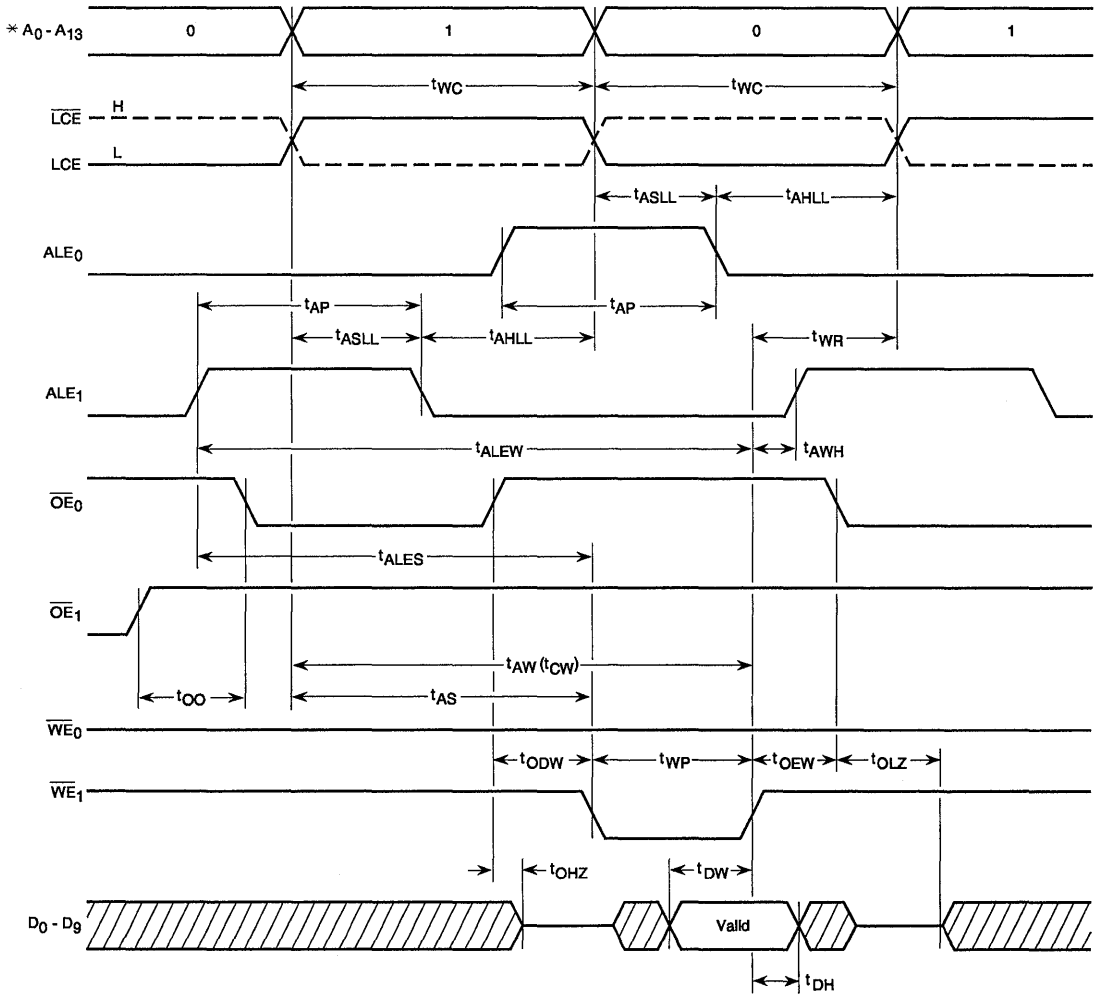
Timing Waveforms (cont)

Write Cycle (LCE = Address)



* 0 and 1 refer to memory arrays 0 and 1.

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23a

μPD46741A
8192 x 20-Bit x 2
Static BiCMOS RAM

Description

The μPD46741A is a high-performance BiCMOS static RAM organized as a 8192 x 20 bits x 2 and designed to be used as a high-speed cache memory. The μPD46741A integrates two 8192 x 20-bit SRAM cores with associated address latches and control signals that can be used to implement an instruction/data cache for 25- and 33-MHz VR3000™ RISC systems.

Features

- Fast access time: 12 or 15 ns
- 8192 x 20-bit x 2 organization
- On-chip address latches
- On-chip instruction/data caches
- Fully static read/write operation
- TTL-compatible inputs and outputs
- 68-pin PLCC package

VR3000 is a trademark of NEC Corporation.

Ordering Information

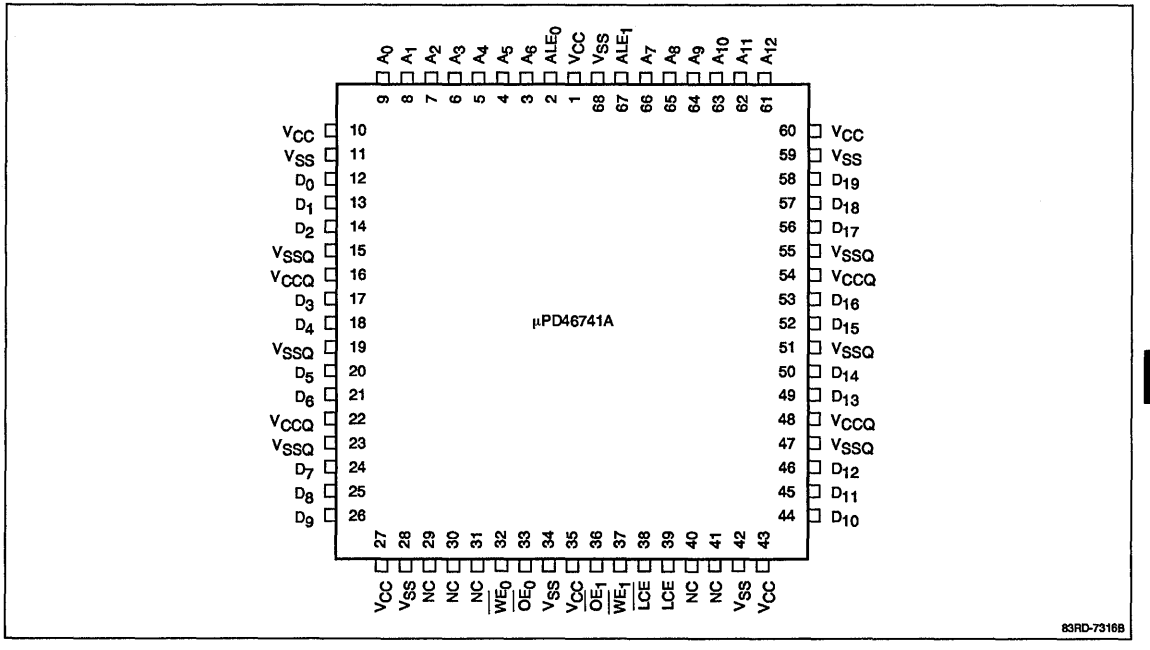
Part Number	Access Time	Output Enable Access Time	Package
μPD46741ALP-12	12 ns	4.5 ns	68-pin PLCC
LP-15	15 ns	7 ns	

Pin Identification

Symbol	Function
A_0 - A_{12}	Addresses
ALE_0 and ALE_1	Address latch enable inputs
D_0 - D_{19}	Data inputs/outputs
LCE and $\overline{LCE}$	Latch chip enable inputs
$\overline{OE}_0$ and $\overline{OE}_1$	Output enable inputs
$\overline{WE}_0$ and $\overline{WE}_1$	Write enable inputs
V_{CC} and V_{CCQ}	+5-volt power supply
V_{SS} and V_{SSQ}	Ground
NC	No connection

Pin Configuration

68-Pin PLCC



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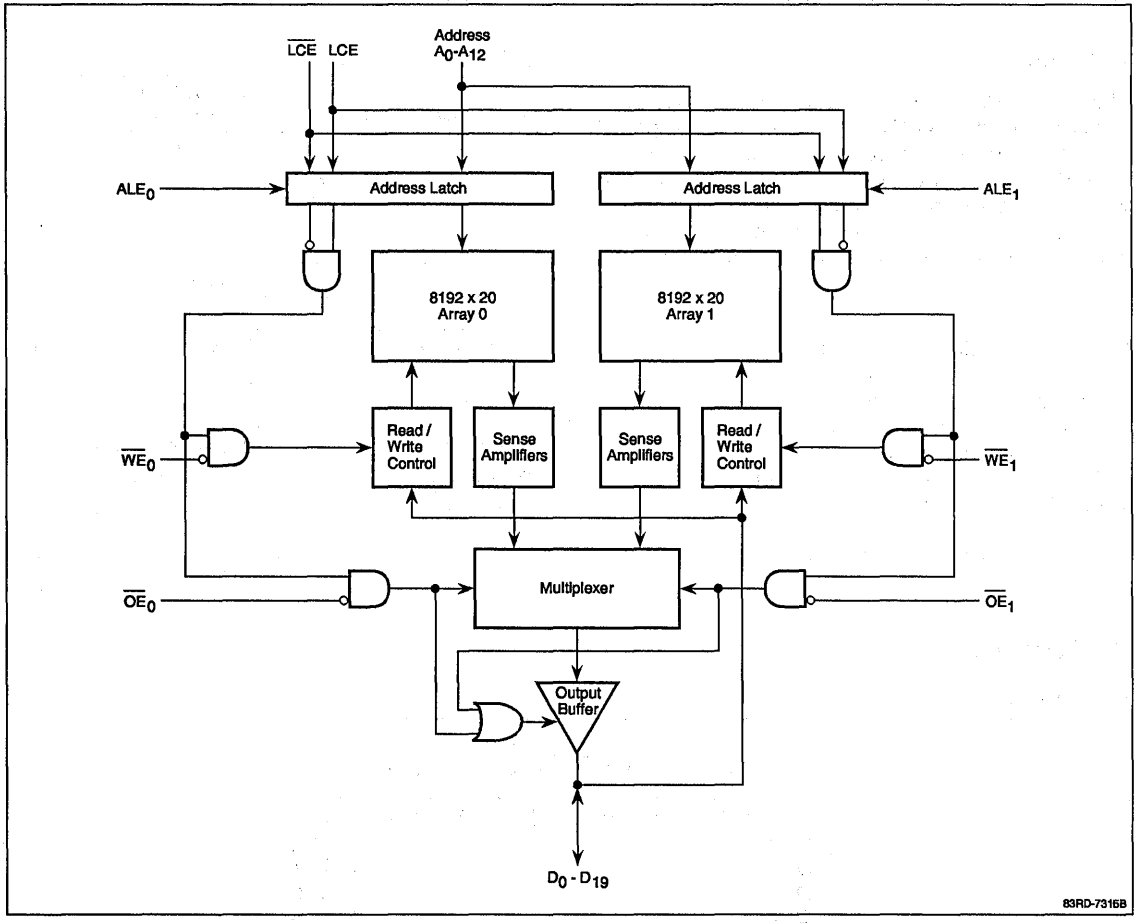
Block Diagram



Functional Operation

The μPD46741A integrates two 8K x 20 SRAM cores with associated address latches and control logic to be used as an instruction/data cache in a high-speed VR3000 RISC processor. In this system, the CPU initiates a μPD46741A memory cycle by outputting an address to one of the two memory arrays. The signals on address lines A_0 - A_{12} are latched into the address latch of array 0 at the rising edge of ALE_0 while ALE_1 is inactive low. The CPU executes a read cycle on array 0 and initiates the next memory operation. Memory array 1 is then accessed by latching the CPU address at the rising edge of ALE_1 with ALE_0 inactive low.

To read data from memory array 0, $\overline{OE}_0$ is driven active low while $\overline{WE}_0$, $\overline{WE}_1$, and $\overline{OE}_2$ remain inactive high. Data in memory array 1 is read by driving $\overline{OE}_1$ low with $\overline{OE}_0$, $\overline{WE}_0$, and $\overline{WE}_1$ inactive high.

The $\overline{WE}_0$ and $\overline{WE}_1$ signals control write cycles into each of the two memory arrays. Data is written into memory array 0 by driving write data on data lines D_0 - D_{19} with $\overline{WE}_0$ active low. In a similar manner, the $\overline{WE}_1$ signal controls write cycles into memory array 1.

The LCE and $\overline{LCE}$ latch chip enable signals provide a decoding function that can be used to increase the size of the VR3000 cache memory. A 32K-byte cache (figure 1) can be implemented using three μPD46741As with LCE and $\overline{LCE}$ connected to V_{CC} and GND, respectively.

Cache size can be increased to 64K bytes (figure 2) using two banks of three μPD46741As. In this case, address signal A_{13} is used to decode the two 32K-byte memory banks. $\overline{LCE}$ of the first bank is connected to address A_{13} and LCE is connected to V_{CC}. LCE of the second bank is connected to A_{13} with $\overline{LCE}$ grounded.

Figure 1. 32K-Byte Cache System

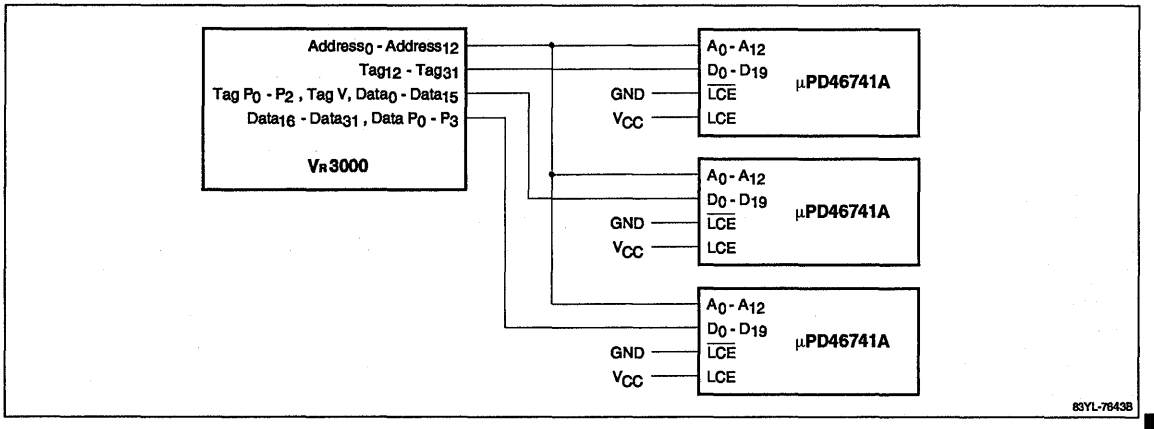
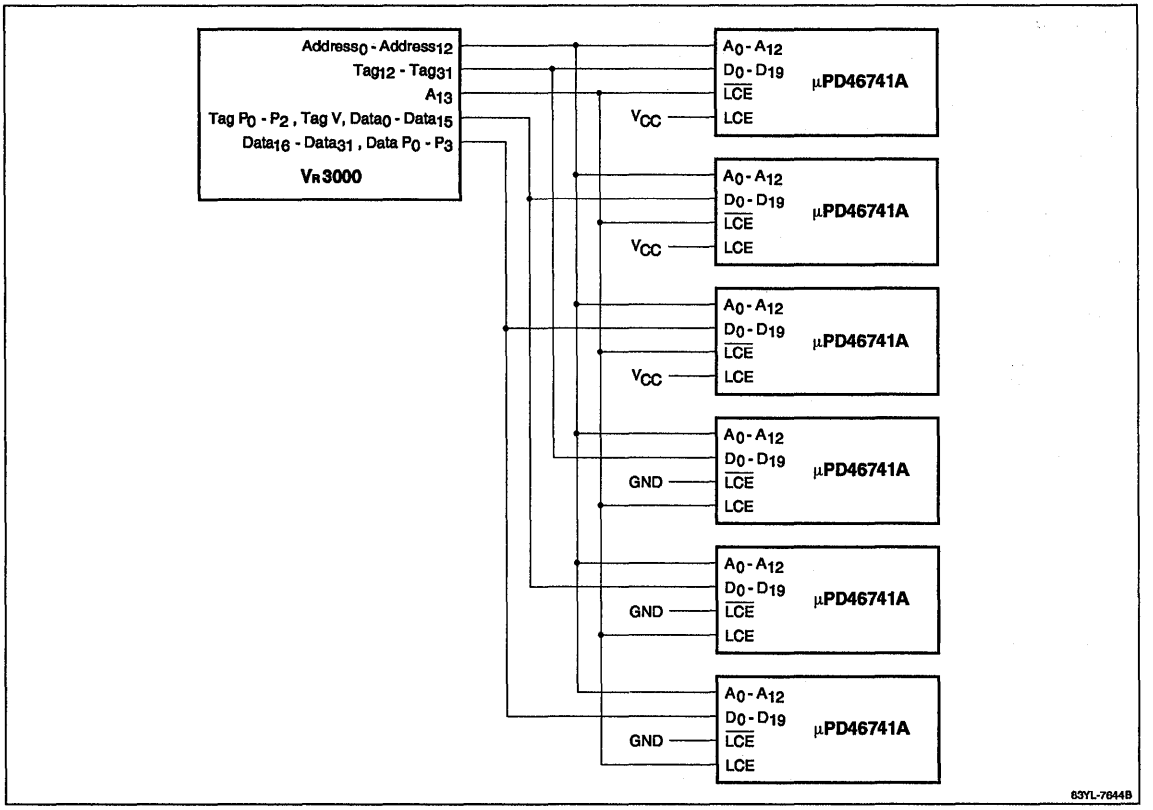


Figure 2. 64K-Byte Cache System



Truth Table

Function	LCE	$\overline{LCE}$	$\overline{WE_0}$	$\overline{WE_1}$	$\overline{OE_0}$	$\overline{OE_1}$	Output
Not selected	L	L	X	X	X	X	High-Z
Not selected	L	H	X	X	X	X	High-Z
Not selected	H	H	X	X	X	X	High-Z
Read RAM array 0 data	H	L	H	H	L	H	Read data
Read RAM array 1 data	H	L	H	H	H	L	Read data
Output high-Z	H	L	H	H	H	H	High-Z
(Note 1)	H	L	H	H	L	L	High-Z
Write data into RAM array 0	H	L	L	H	X	X	Write data
Write data into RAM array 1	H	L	H	L	X	X	Write data
Write same data into both RAM arrays. (Note 2)	H	L	L	L	X	X	Write data

Notes:

(1) Not recommended for use because of multiselection in the multiplexer circuit.

(2) Not recommended for use because of increasing ac power during write operation.

(3) X = don't care.

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.5 to +7.0 V
Input voltage, V_{IN}	−0.5 to + 7.0 V
Output voltage, V_{OUT}	−0.5 to + 7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.5 *		0.8	V
Ambient temperature	T_A	0		+70	°C

* V_{IL} = −2.0 V min for 20-ns maximum pulse.

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter*	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}			6	pF
Input/output capacitance	$C_{I/O}$			8	pF

* These parameters are sampled and not 100% tested.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−2		2	μA	V_{IN} = 0 V to V_{CC}
Output leakage current	I_{LO}	−2		2	μA	V_O = 0 V to V_{CC}
Operating supply current*	I_{CCA}			300	mA	V_O = open; V_{CC} = max; f = $2/t_{RC}$
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 8 mA; V_{CC} = min
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −4.0 mA; V_{CC} = min

* Applicable to two SRAM cores operating at maximum frequency.

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD46741A-12		μPD46741A-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Address access time	t_{AA}		12		15	ns	
Address hold time for ALE_0 and ALE_1	t_{AHLL}	2		2		ns	(Note 3)
Latched chip enable access time	t_{ALCE}		12		15	ns	
ALE access time	t_{ALEA}	1	14	1	17	ns	
Address latch enable pulse width	t_{AP}	6		8		ns	
Address setup time for ALE_0 and ALE_1	t_{ASLL}	4		4		ns	(Note 4)
Latched chip enable to output in high-Z	t_{CHZ}	1	6	2	7	ns	(Note 1)
Latched chip enable to output in low-Z	t_{CLZ}	1		2		ns	(Note 1)
Output enable to output valid	t_{OE}		4.5		6	ns	(Note 5)
Output hold from address change	t_{OH}	3		3		ns	
$\overline{OE}$ to output in high-Z	t_{OHZ}	0	4	0	6	ns	(Note 1)
$\overline{OE}$ to output in low-Z	t_{OLZ}	0		0		ns	
Output enable overlap time	t_{OO}	1		1		ns	

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AC Characteristics (cont)

Parameter	Symbol	μPD46741A-12 Min	μPD46741A-12 Max	μPD46741A-15 Min	μPD46741A-15 Max	Unit	Test Conditions
Read cycle time	t_{RC}	15		20		ns	
Write Operation							
Address hold time for ALE_0 and ALE_1	t_{AHLL}	2		2		ns	
ALE setup time prior to end of write	t_{ALES}	2		2		ns	
ALE setup time to end of write	t_{ALEW}	17		17		ns	
Address latch enable pulse width	t_{AP}	6		8		ns	
Address setup time	t_{AS}	2		2		ns	
Address setup time for ALE_0 and ALE_1	t_{ASLL}	4		4		ns	
Address valid to end of write	t_{AW}	12		15		ns	
Address latch enable hold time after write	t_{AWH}	0		0		ns	
Latched chip enable to end of write	t_{CW}	15		15		ns	
Data hold time	t_{DH}	0		0		ns	(Note 8)
Data valid to end of write	t_{DW}	5		7		ns	(Note 7)
Output enable to end of write	t_{OEW}	0		0		ns	(Note 6)
Output disable to write enable	t_{ODW}	2		2		ns	
Write cycle time	t_{WC}	12		15		ns	
Write pulse width	t_{WP}	7		10		ns	
Write recovery time	t_{WR}	2		3		ns	

Notes:

(1) This transition is measured ±200 mV from steady-state with the output load in figure 3.

(2) Input pulse levels = 0.8 to 2.4 V; input pulse rise and fall times ≤ 3 ns; see figure 3.

(3) t_{AHLL} = 1.5 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

(4) t_{ASLL} = 3 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

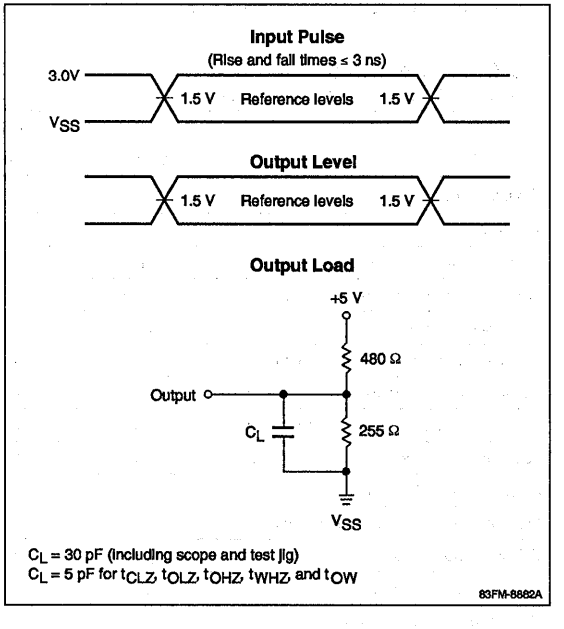
(5) t_{OE} = 4 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

(6) $\overline{OE}_n$, $\overline{WE}_m$ (n = 0 or 1, m = 0 or 1)
t_{OEW} = 0 ns min at n ≠ m
= 2 ns min at n = m

(7) t_{DW} = 4 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

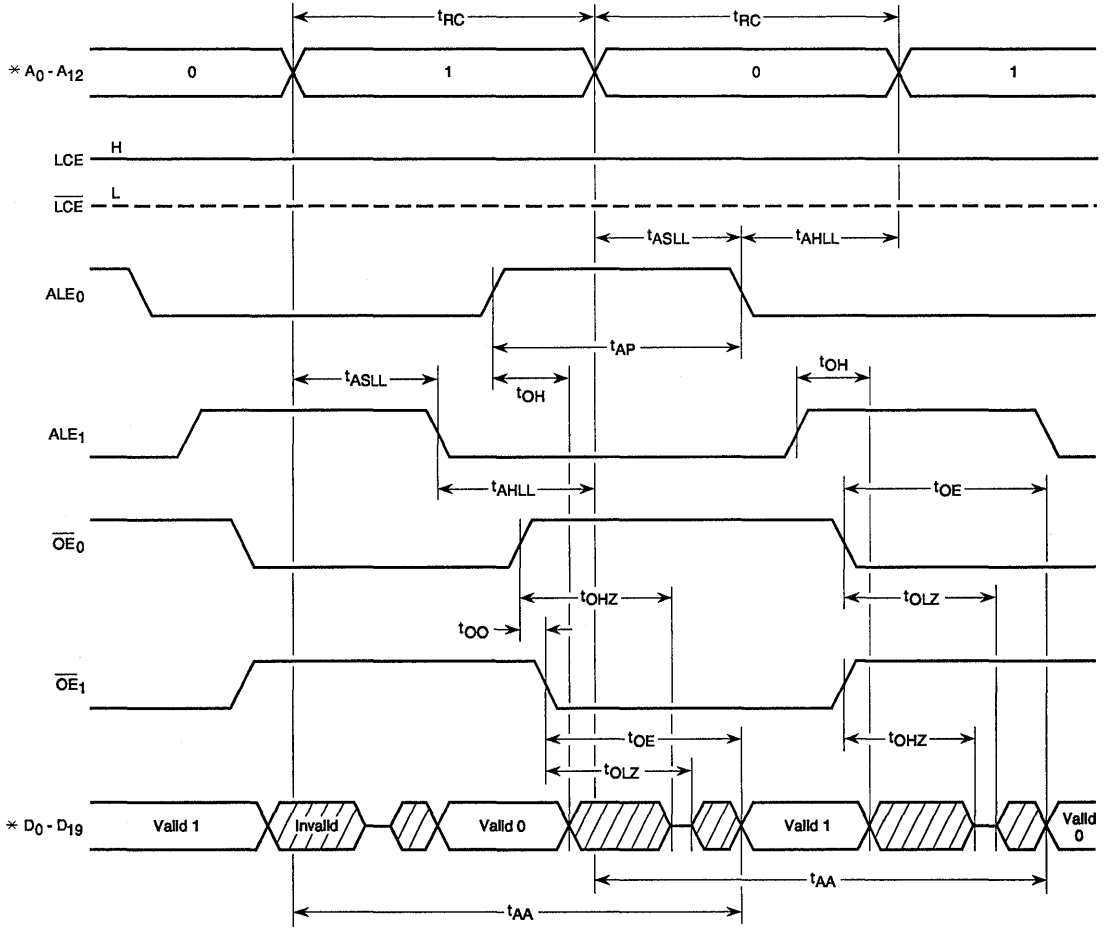
(8) t_{DH} = 0.5 ns for V_{CC} = +5 V ±5%, T_A = 0 to 50°C.

Figure 3. AC Test Conditions



Timing Waveforms

Read Cycle (LCE High)



* 0 and 1 refer to memory arrays 0 and 1.

† $\overline{WE}_0$ and $\overline{WE}_1$ are High.

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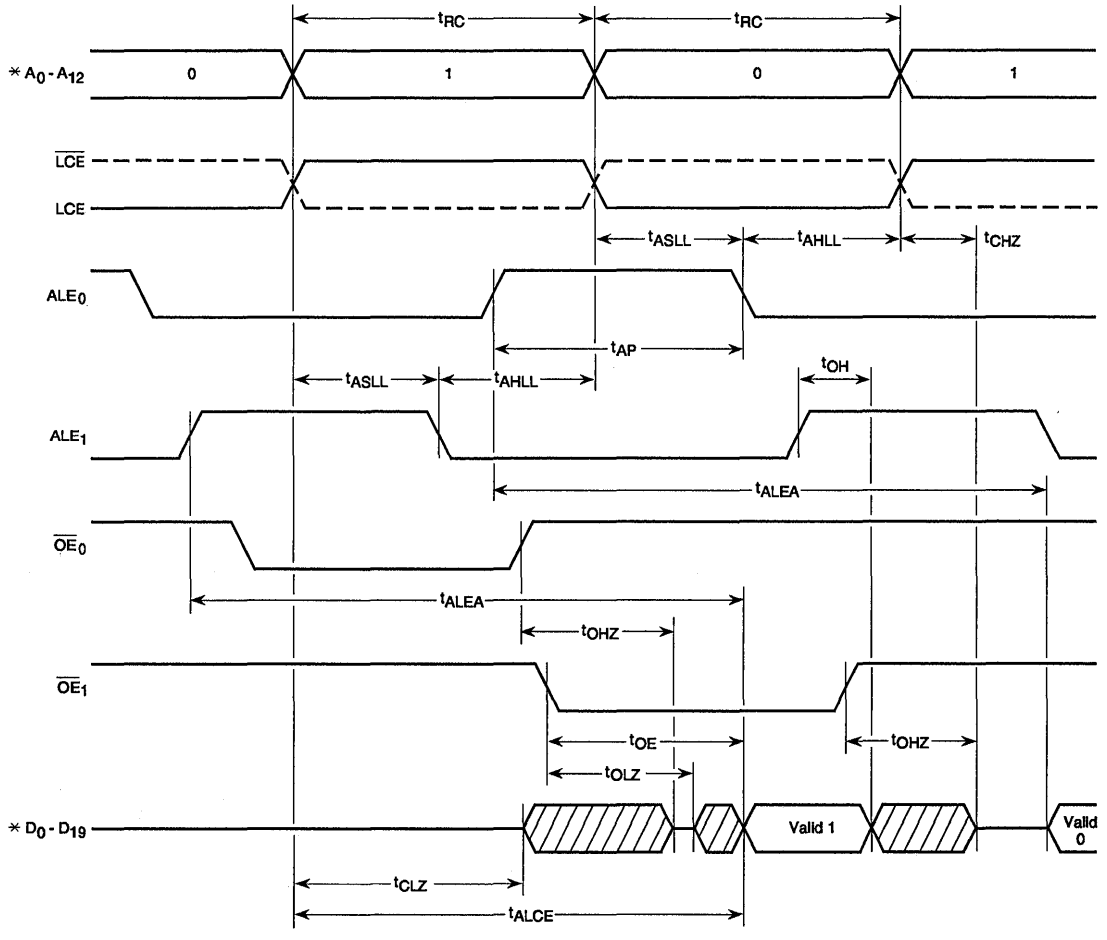
Timing Waveforms (cont)

Read Cycle (LCE = Address)



* 0 and 1 refer to memory arrays 0 and 1.

† $\overline{WE_0}$ and $\overline{WE_1}$ are High.

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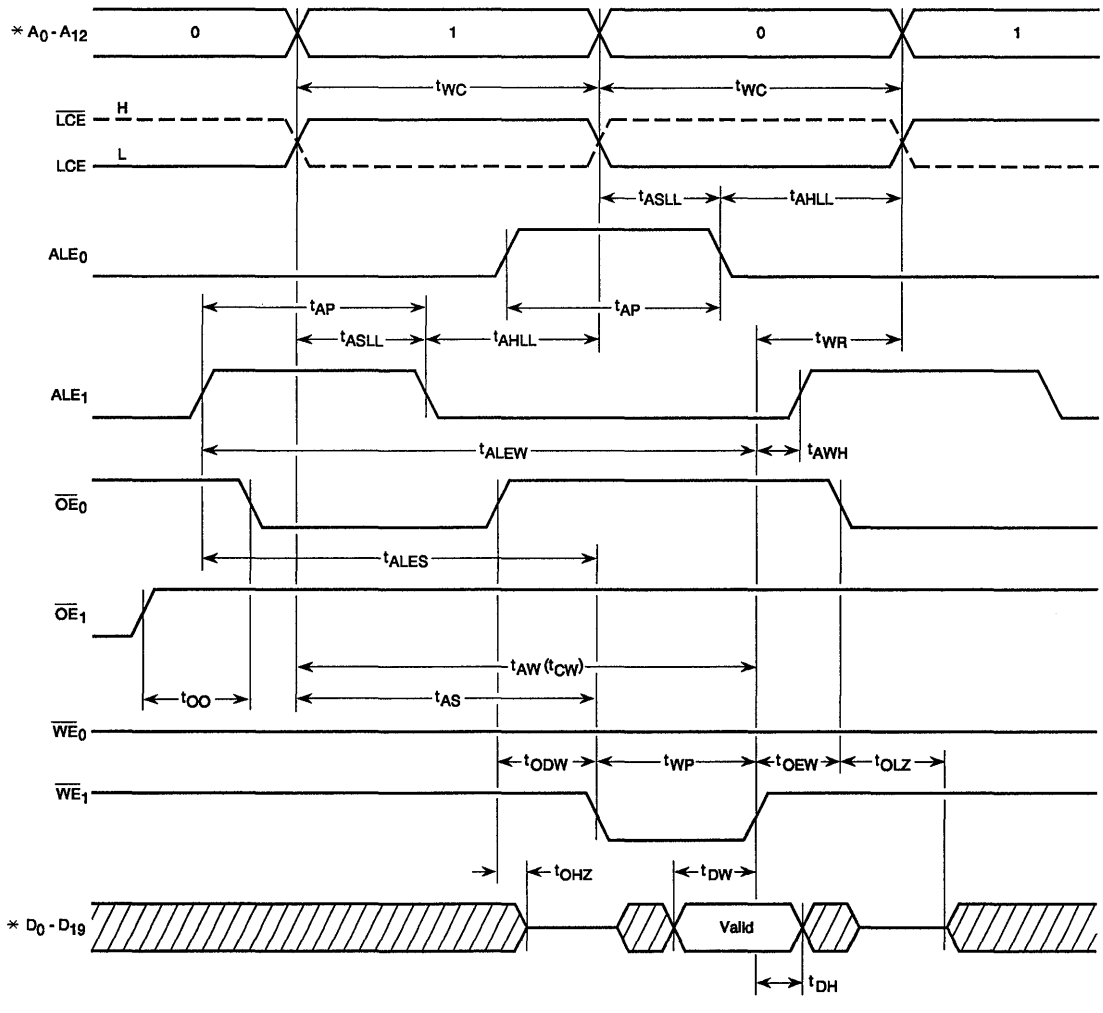
Timing Waveforms (cont)

Write Cycle (LCE = Address)



* 0 and 1 refer to memory arrays 0 and 1.

83CL-8861B

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NEC

Section 24
Standard Static RAMs

(See App Notes 50, 90-04.)

μPD	Org.	Features	
43256A	32K x 8	85-ns; Output enable	24a
43256B	32K x 8	55-ns; Output enable	24b
431000A	128K x 8	70-ns; Output enable, two chip enables	24c
434000	512K x 8	55-ns; Output enable	24d
MC-434000	512K x 8	Module; 85-ns; Output enable	24e

Upcoming Products

Description	Device Number	Comments
32K x 8	μPD43256A-10X, 12X	−25 to +85°C; speeds to 100 ns
32K x 8	μPD43256A-10Y, 12Y	−40 to +85°C; speeds to 100 ns
32K x 8	μPD43256B-A12	3.0 to 5.5 V; 120-ns access time
32K x 8	μPD43256B-B12	2.7 to 5.5 V; 120-ns access time
128K x 8	μPD431000A-70X, 85X, 100X	−25 to +85°C; speeds to 70 ns
128K x 8	μPD431000A-70Y, 85Y, 100Y	−40 to +85°C; speeds to 70 ns
128K x 8	μPD431000B-55L/LL, 70L/LL, 85L/LL	Low power; speeds to 55 ns
128K x 8	μPD431000B-B10, B12	2.7 to 5.5 V; speeds to 100 ns
128K x 9	μPD431003	Low power; speeds to 55 ns; two Chip Enables
128K x 9	μPD431003-B10, B12	2.7 to 5.5 V; speeds to 100 ns; two Chip Enables
512K x 8	μPD434000-B15	2.7 to 5.5 V; 150-ns access time; two Chip Enables

μPD43256A
32,768 x 8-Bit
Static CMOS RAM

Description

The μPD43256A is a 32,768-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors to make the μPD43256A a high-speed device that requires very low power and no clock or refreshing.

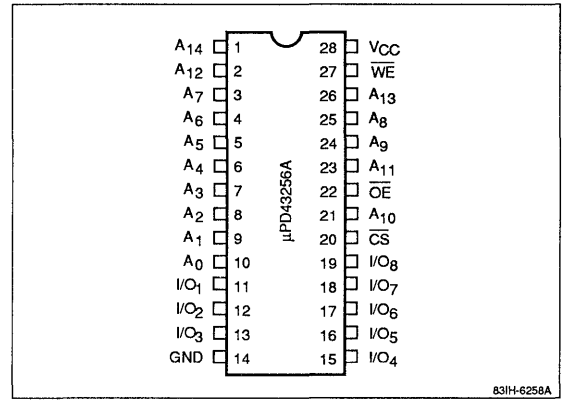
Minimum standby power is drawn when $\overline{CS}$ is high, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 V. The μPD43256A is available in standard 28-pin plastic DIP, 28-pin plastic miniflat, or 32-pin plastic TSOP packaging.

Features

- Single +5-volt power supply
- Fully static operation—no clock or refreshing required
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Data retention of 2 V minimum
- Standard 28-pin plastic DIP and miniflat packaging
- Standard 32-pin plastic TSOP packaging (with either normal or reverse bent leads)

Pin Configurations

28-Pin Plastic DIP or Miniflat

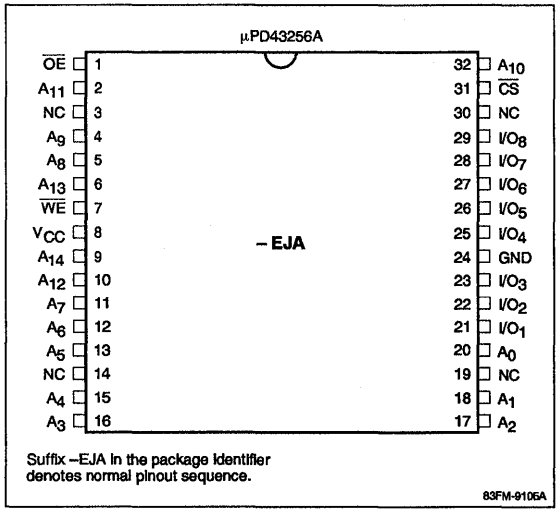


Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Pin Configurations (cont)

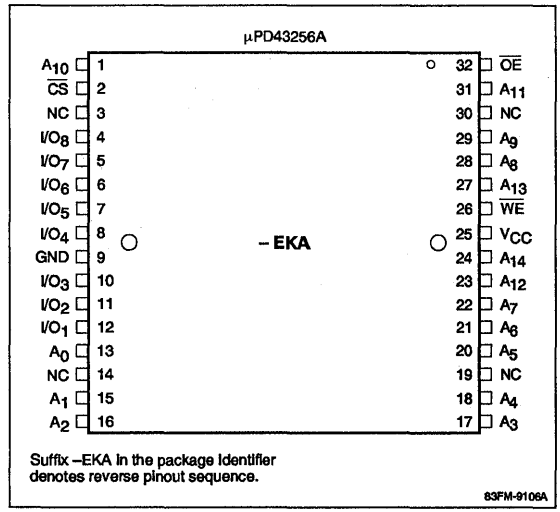
32-Pin Plastic TSOP (Normal Pinouts)



Suffix –EJA in the package identifier denotes normal pinout sequence.

83FM-9105A

32-Pin Plastic TSOP (Reserve Pinouts)



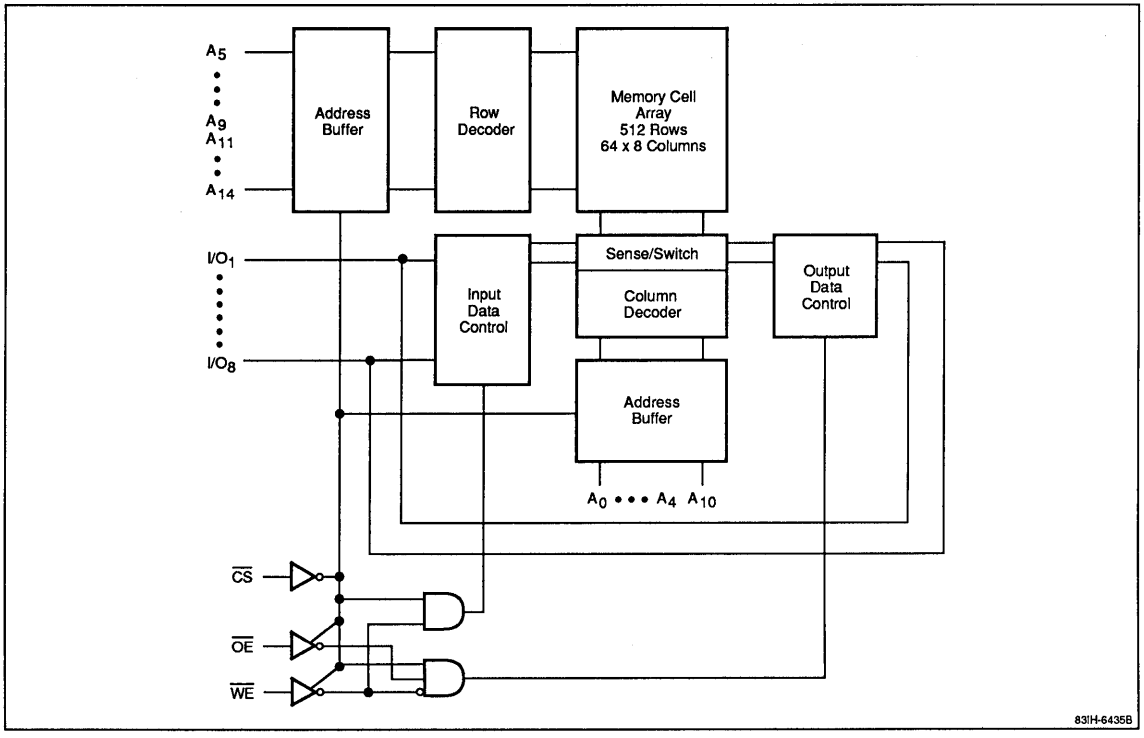
Suffix –EKA in the package identifier denotes reverse pinout sequence.

83FM-9106A

Ordering Information

Catalog Part Number	Access Time (max)	Data Retention Current (max) T_A = 0 to 70°C(max)	Package
μPD43256AC-85L	85 ns	50 μA	28-pin plastic DIP(600 mil)
C-10L	100 ns		
C-12L	120 ns		
C-15L	150 ns		
μPD43256AC-85LL	85 ns	20 μA	28-pin plastic DIP(600 mil)
C-10LL	100 ns		
C-12LL	120 ns		
C-15LL	150 ns		
μPD43256AGU-85L	85 ns	50 μA	28-pin plastic miniflat
GU-10L	100 ns		
GU-12L	120 ns		
GU-15L	150 ns		
μPD43256AGU-85LL	85 ns	20 μA	28-pin plastic miniflat
GU-10LL	100 ns		
GU-12LL	120 ns		
GU-15LL	150 ns		
μPD43256AGX-10L	100 ns	50 μA	32-pin plastic TSOP (normal pinouts)
GX-12L	1200 ns		
μPD43256AGX-10LL	100 ns	20 μA	
GX-12LL	120 ns		
μPD43256AGXM-10L	100 ns	50 μA	32-pin plastic TSOP (reverse pinouts)
GXM-12L	1200 ns		
μPD43256AGXM-10LL	100 ns	20 μA	
GXM-12LL	120 ns		

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		5	pF
Input/output capacitance	$C_{I/O}$		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Not selected	High-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Notes:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−1		1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Operating supply current	I_{CCA1}			45	mA	$\overline{CS} \leq V_{IL}$ (min cycle); $I_{I/O}$ = 0 V (Note 1)
	I_{CCA2}			10	mA	$\overline{CS} = V_{IL}$; $I_{I/O}$ = 0 V
	I_{CCA3}			10	mA	$\overline{CS} \leq 0.2$ V; f = 1 MHz; $I_{I/O}$ = 0 V; $V_{IL} \leq 0.2$ V; $V_{IH} \geq V_{CC} - 0.2$ V
Standby supply current	I_{SB}			3	ma	$\overline{CS} \geq V_{IH}$
	I_{SB1}		0.002	0.1	mA	$\overline{CS} \geq V_{CC} - 0.2$ V (Note 2)
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC} − 0.5			V	I_{OH} = −0.1 mA

Notes:

(1) μPD43256A-10L/-10LL/-12L/-12LL = 40 mA (max).
μPD43256A-15L/-15LL = 35 mA (max).

(2) μPD43256AGX-10LL/-12LL = 50 μA (max).

AC Characteristics (for L and LL Versions)

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	μPD43256A-85		μPD43256A-10		μPD43256A-12		μPD43256A-15		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Read Operation											
Read cycle time	t_{RC}	85		100		120		150		ns	
Address access time	t_{AA}		85		100		120		150	ns	(Note 2)
Chip select access time	t_{ACS}		85		100		120		150	ns	(Note 2)
Output enable to output valid	t_{OE}		40		50		60		70	ns	(Note 2)
Output hold from address change	t_{OH}	10		10		10		10		ns	
Chip select to output in low-Z	t_{CLZ}	10		10		10		10		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	5		5		5		5		ns	(Note 3)
Chip select to output in high-Z	t_{CHZ}		30		35		40		50	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		30		35		40		50	ns	(Note 3)
Write Operation											
Write cycle time	t_{WC}	85		100		120		150		ns	
Chip select to end of write	t_{CW}	70		80		85		100		ns	
Address valid to end of write	t_{AW}	70		80		85		100		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Write pulse width	t_{WP}	65		70		70		90		ns	
Write recovery time	t_{WR}	5		5		5		5		ns	
Data valid to end of write	t_{DW}	35		40		50		60		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		30		35		40		50	ns	(Note 3)
Output active from end of write	t_{OW}	10		10		10		10		ns	(Note 3)

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output load.

(3) See figure 2 for output load.

Low V_{CC} Data Retention Characteristics

T_A = 0 to 70°C

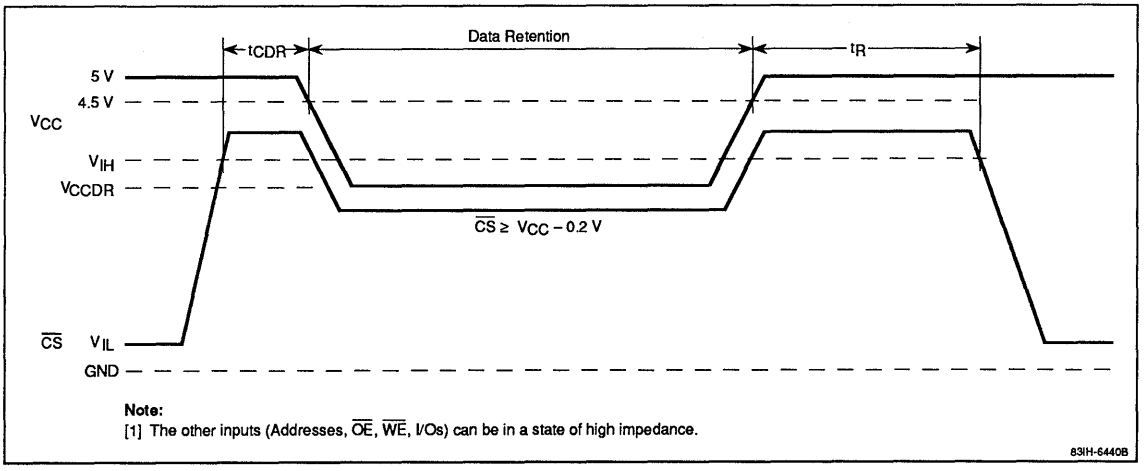
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	V_{CC} = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2$ V (Notes 1, 2)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) For μPD43256A-LL, I_{CCDR} = 20 μA (max) at T_A = 0 to 70°C and 3 μA (max) at T_A = 0 to 40°C.

(2) For μPD43256A-L, I_{CCDR} = 15 μA (max) at T_A = 0 to 40°C.

Data Retention Timing



Note:
[1] The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a state of high impedance.

83IH-6440B

Figure 1. Output Load

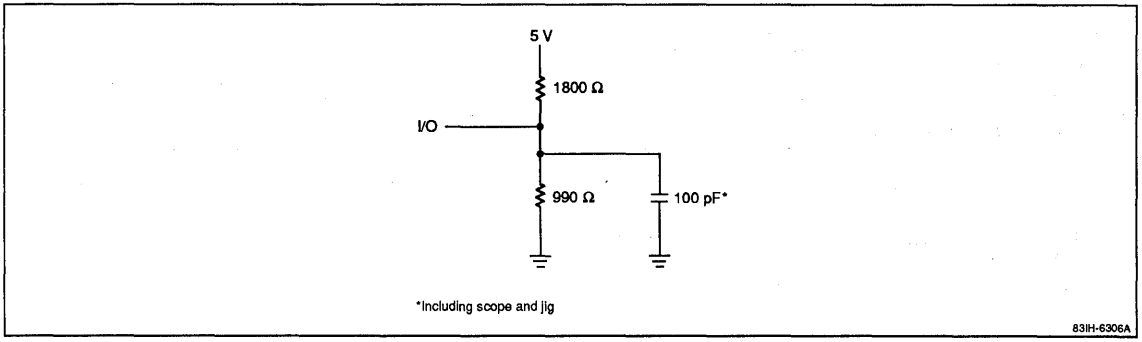
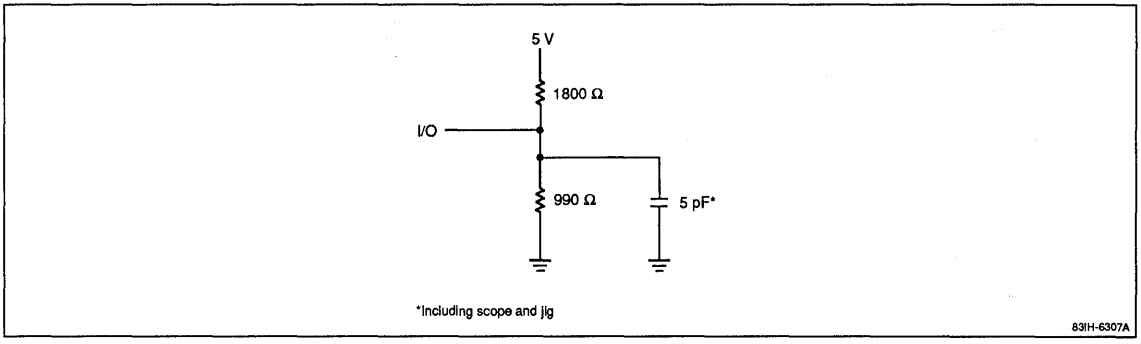
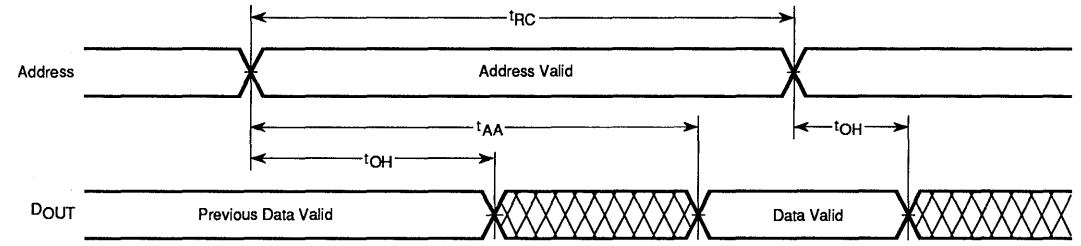


Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}



Timing Waveforms

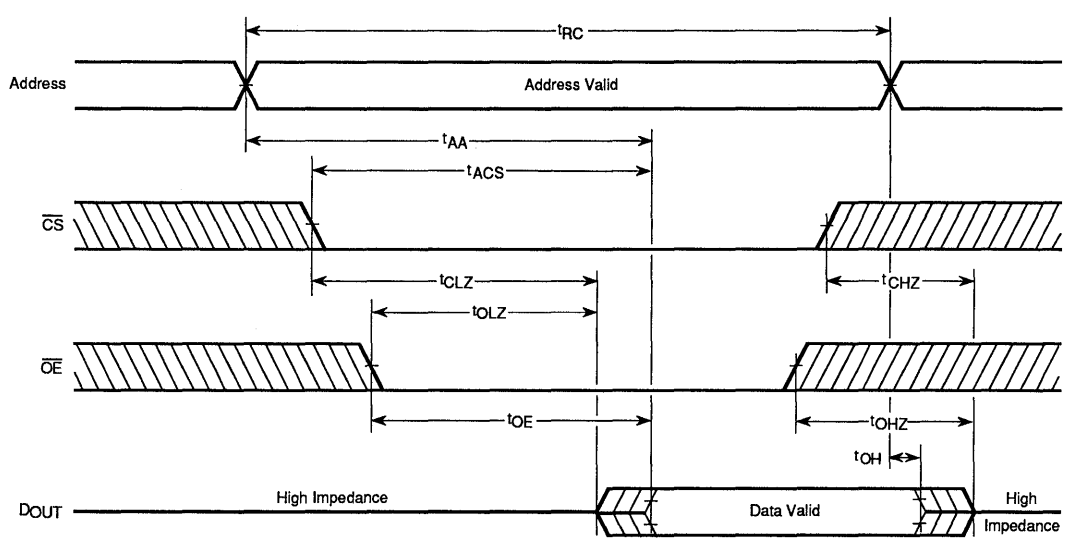
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6436B

Chip Select Access Cycle



Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

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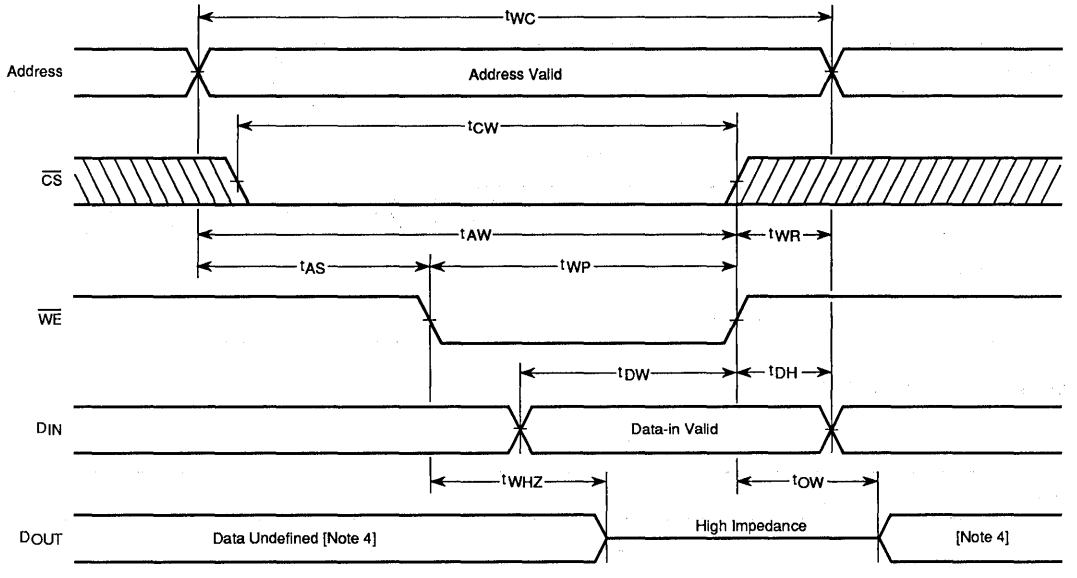
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

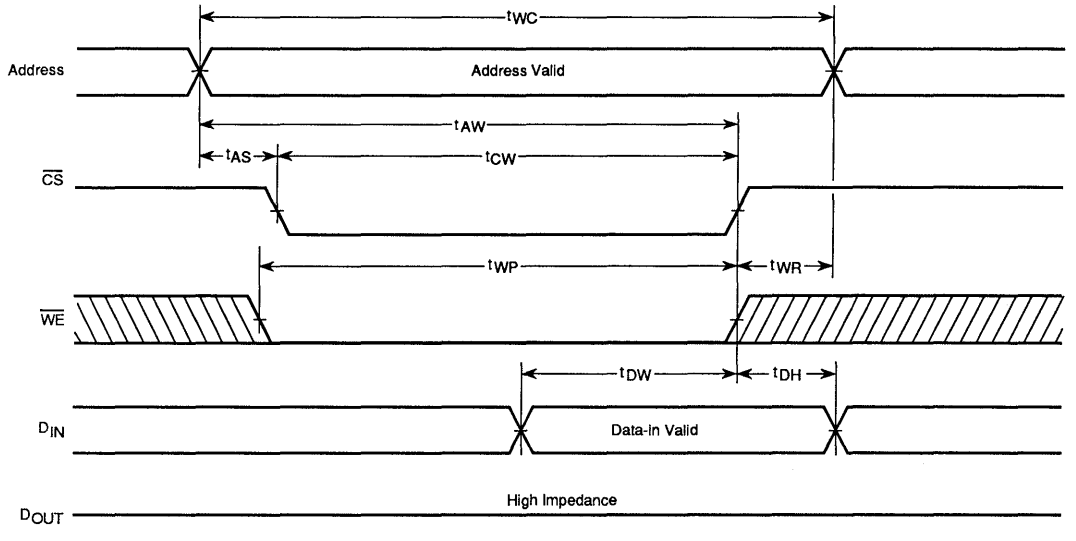
[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

[4] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

83IH-6438B

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

83IH-6439B

μPD43256B
32,768 x 8-Bit
Static CMOS RAM

Description

The μPD43256B is a 32,768-word by 8-bit static RAM fabricated with advanced silicon-gate technology. Its unique design uses CMOS peripheral circuits and N-channel memory cells with polysilicon resistors to make the μPD43256B a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when $\overline{CS}$ is high, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 V. The μPD43256B is available in standard 28-pin plastic DIP and 28-pin plastic miniflat.

Features

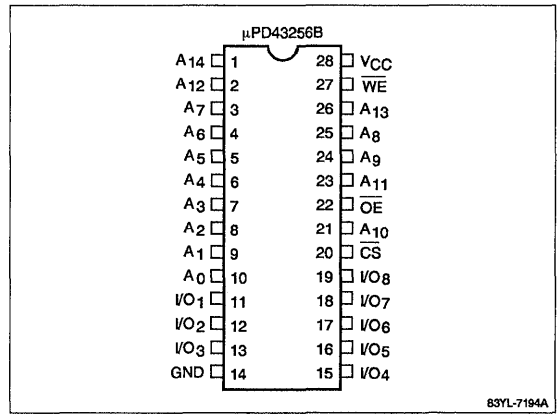
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- Data retention of 2 V minimum
- Standard 28-pin plastic DIP and miniflat packaging
- Fast access time of 55 ns

Ordering Information

Part Number	Access Time (max)	Package
μPD43256BCZ-55L	55 ns	28-pin plastic DIP
CZ-70L	70 ns	
CZ-85L	85 ns	
μPD43256BCZ-55LL	55 ns	
CZ-70LL	70 ns	
CZ-85LL	85 ns	
μPD43256BGU-55L	55 ns	28-pin plastic miniflat
GU-70L	70 ns	
GU-85L	85 ns	
μPD43256BGU-55LL	55 ns	
GU-70LL	70 ns	
GU-85LL	85 ns	

Pin Configuration

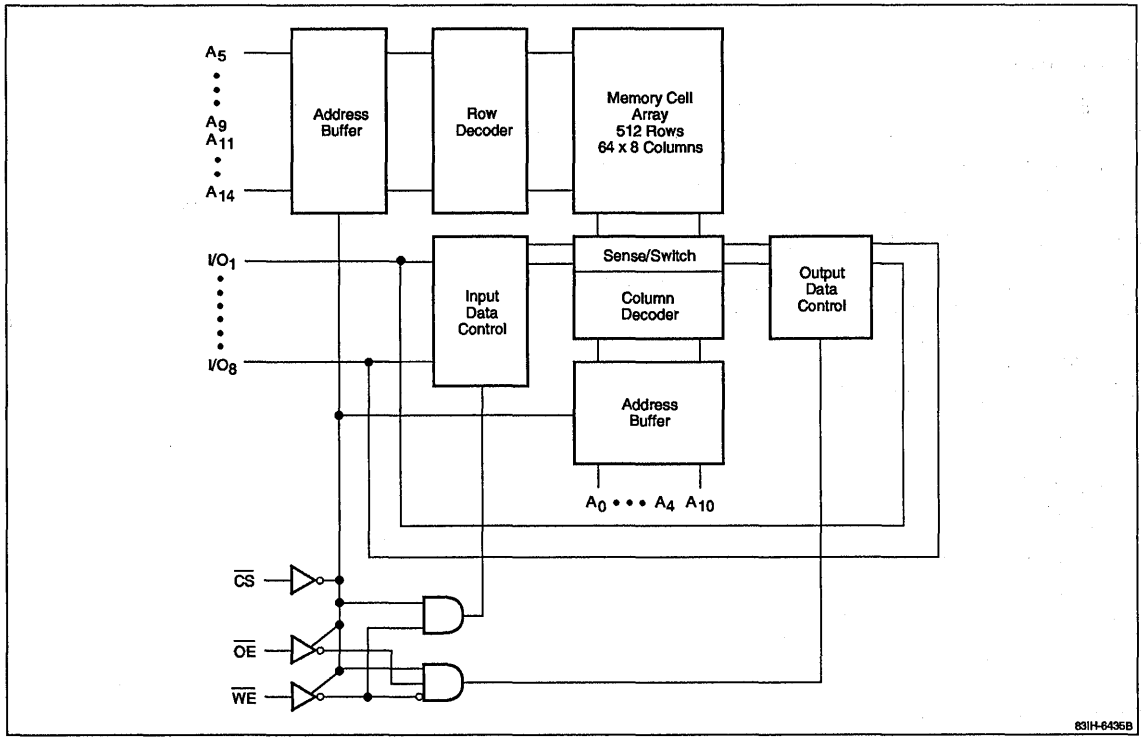
28-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_1 - I/O_8	Data inputs and outputs
$\overline{CS}$	Chip select
Pin Identification	
Symbol	Function
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		5	pF
Input/output capacitance	$C_{I/O}$		8	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Function	I/O	I_{CC}
H	X	X	Not selected	High-Z	Standby
L	H	H	Outputs disabled	High-Z	Active
L	L	H	Read	D_{OUT}	Active
L	X	L	Write	D_{IN}	Active

Notes:

(1) X = don't care.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low (Note 1)	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−1		1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−1		1	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS} \geq V_{IH}$ or $\overline{OE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$
Operating supply current	I_{CCA1}			50	mA	$\overline{CS} \leq V_{IL}$ (min cycle); $I_{I/O}$ = 0 V (Note 1)
	I_{CCA2}			10	mA	$\overline{CS} = V_{IL}$; $I_{I/O}$ = 0 V
	I_{CCA3}			10	mA	$\overline{CS} \leq 0.2$ V; f = 1 MHz; $I_{I/O}$ = 0 V; $V_{IL} \leq 0.2$ V; $V_{IH} \geq V_{CC} - 0.2$ V
Standby supply current	I_{SB}			3	mA	$\overline{CS} \geq V_{IH}$
	I_{SB1}		0.002	0.1	μA	$\overline{CS} \geq V_{CC} - 0.2$ V (Note 2)
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC} − 0.5			V	I_{OH} = −0.1 mA

Notes:

(1) -70 and -85 = 45 mA (max).

(2) -LL = 0.001 (typ) and 0.05 (max).

AC Characteristics

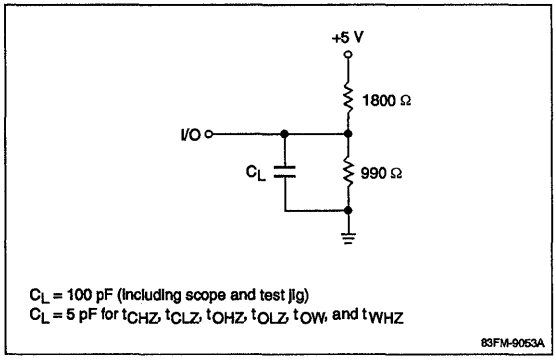
T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	μPD43256B-55		μPD43256B-70		μPD43256B-85		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Read Operation									
Read cycle time	t_{RC}	55		70		85		ns	
Address access time	t_{AA}		55		70		85	ns	
Chip select access time	t_{ACS}		55		70		85	ns	
Output enable to output valid	t_{OE}		30		35		40	ns	
Output hold from address change	t_{OH}	10		10		10		ns	
Chip select to output in low-Z	t_{CLZ}	10		10		10		ns	
Output enable to output in low-Z	t_{OLZ}	5		5		5		ns	
Chip select to output in high-Z	t_{CHZ}		30		30		30	ns	
Output enable to output in high-Z	t_{OHZ}		30		30		30	ns	
Write Operation									
Write cycle time	t_{WC}	55		70		85		ns	
Chip select to end of write	t_{CW}	50		60		70		ns	
Address valid to end of write	t_{AW}	50		60		70		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	45		55		65		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	30		30		35		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		30		30		30	ns	
Output active from end of write	t_{OW}	10		10		10		ns	

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) Output loads:



C_L = 100 pF (including scope and test jig)
C_L = 5 pF for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{OW}, and t_{WHZ}

83FM-9053A

Low V_{CC} Data Retention Characteristics

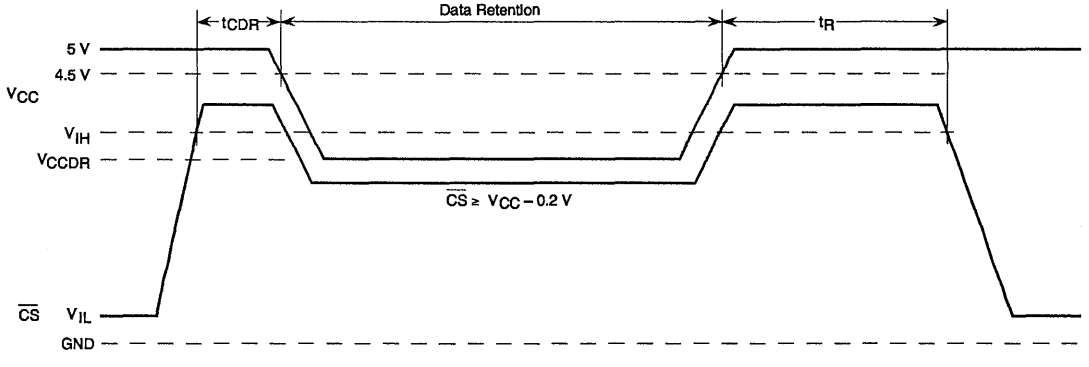
T_A = 0 to 70°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	V_{CC} = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2$ V (Note 1)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) At 0 to 40°C, the maximum for I_{CCDR} is 15 μA for the -L version and 3μ A for the -LL version.

Data Retention Timing

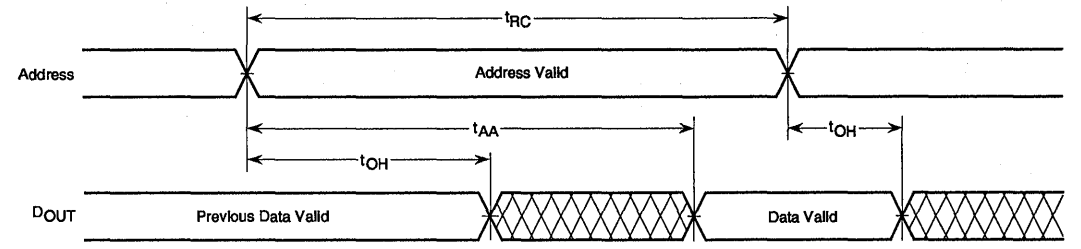


Note:
[1] The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in a state of high impedance.

83IH-6440B

Timing Waveforms

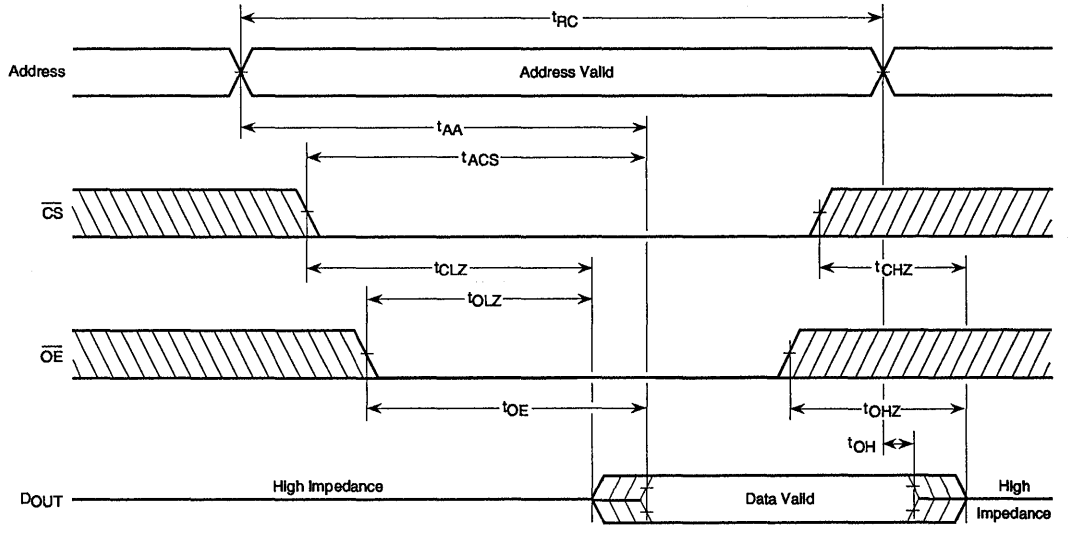
Address Access Cycle



Notes:
[1] $\overline{WE}$ is held high for a read cycle.
[2] The device is continually selected, where $\overline{CS} = \overline{OE} = V_{IL}$.

83IH-6436B

Chip Select Access Cycle

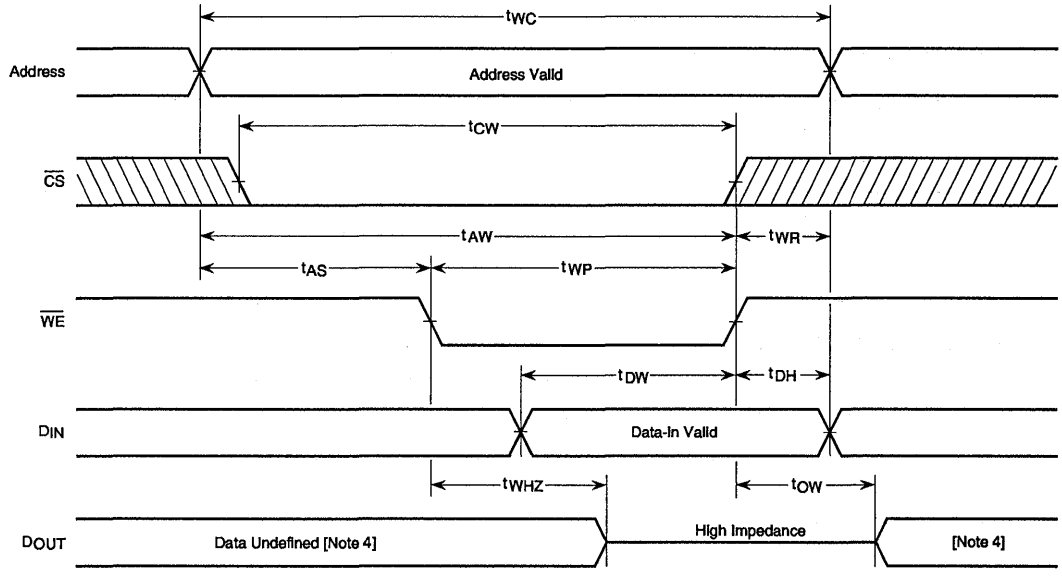


Notes:
[1] $\overline{WE}$ is high for a read cycle.
[2] Address valid prior to or coincident with the low transition of $\overline{CS}$.

83IH-6437B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

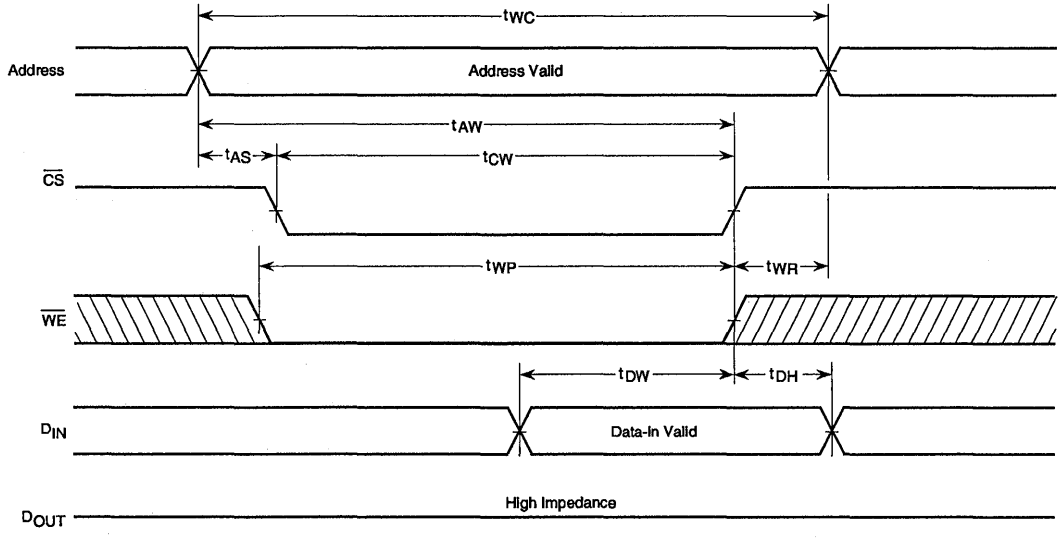
[4] During this period, the I/O pins may be in the output state. Therefore, input signals of opposite phase must not be applied.

83IH-6438B

24b

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in a state of high impedance.

83IH-6439B

μPD431000A
131,072 x 8-Bit
Static CMOS RAM

Description

The μPD431000A is a 131,072-word by 8-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with polysilicon resistors make the μPD431000A a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when CE_2 is low, independent of the other inputs' levels. Data retention is guaranteed at a power supply voltage as low as 2 volts. The μPD431000A is available in standard 32-pin plastic DIP, 32-pin plastic miniflat, and 32-pin plastic TSOP packaging.

Features

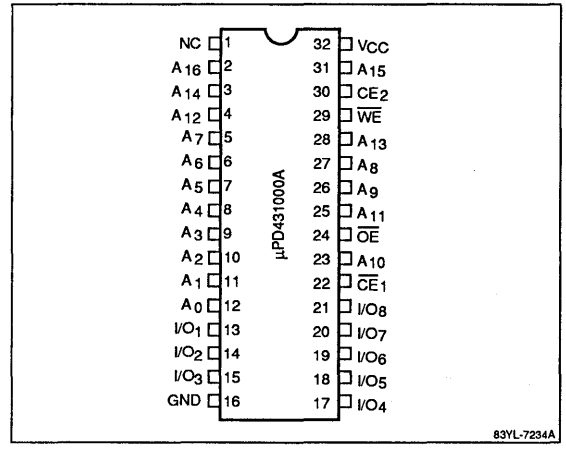
- 131,072-word by 8-bit organization
- Single + 5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- Two CE pins and one $\overline{OE}$ pin for easy application
- Data retention current of 0.5 μA typical
- Data retention voltage of 2 V minimum
- Standard 32-pin plastic DIP, miniflat, and TSOP packaging

Pin Identification

Symbol	Function
A_0 - A_{16}	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}_1$ and CE_2	Chip enables 1 and 2
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

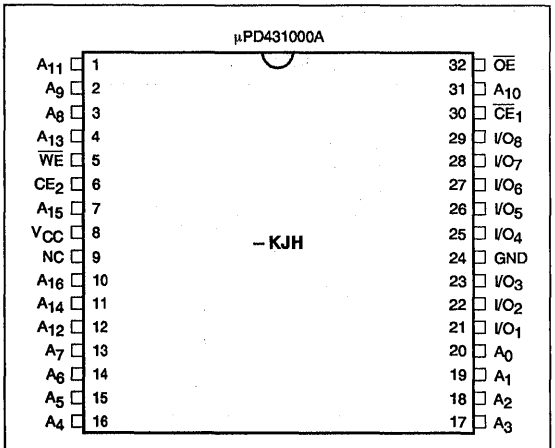
Pin Configurations

32-Pin Plastic DIP or Miniflat



Pin Configurations (cont)

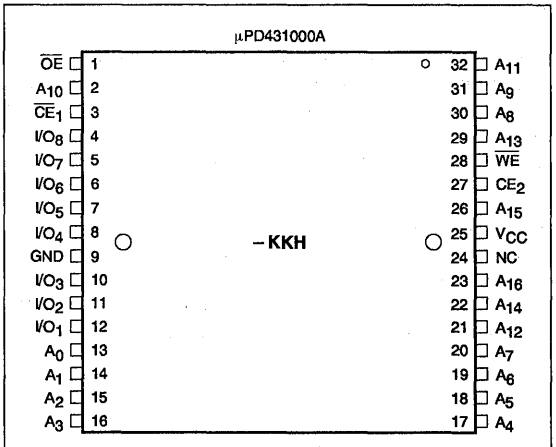
32-Pin Plastic TSOP (Normal Pinouts)



Suffix –KJH in the package identifier denotes normal pinout sequence.

83FM-9107A

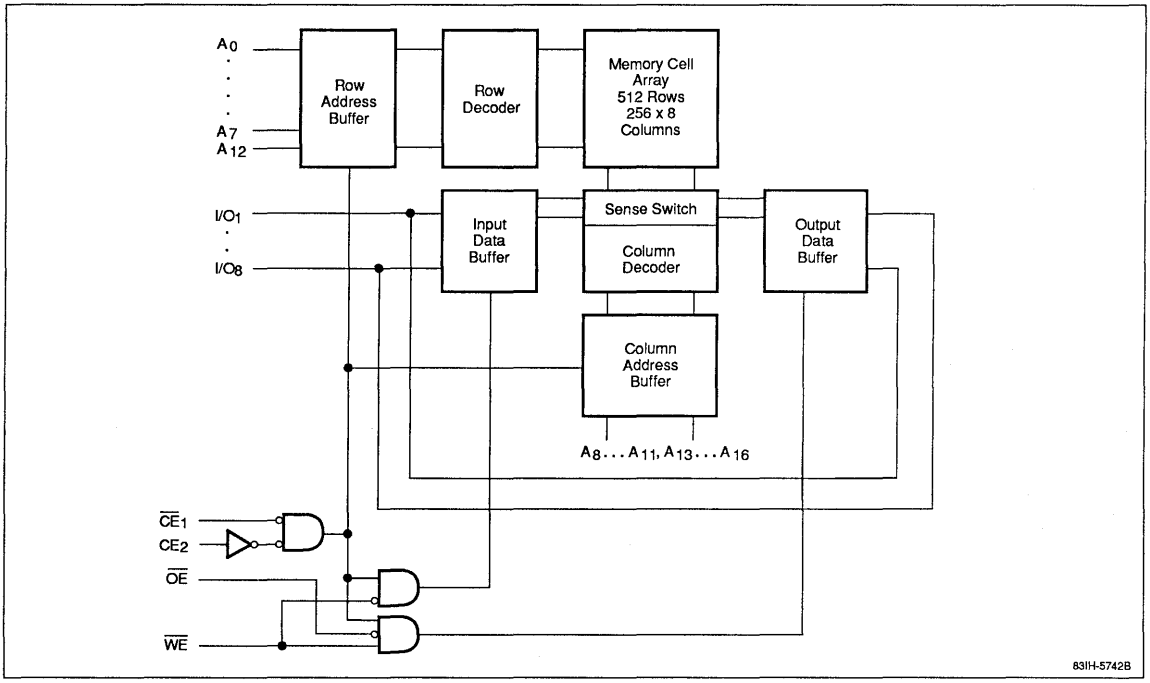
32-Pin Plastic TSOP (Reverse Pinouts)



Suffix –KKH in the package identifier denotes reverse pinout sequence.

83FM-9108A

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Input/output capacitance	$C_{I/O}$			10	pF

Notes:

(1) This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Notes:

(1) −3.0 V minimum (pulse width = 50 ns).

Truth Table

Function	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	X	High-Z	Standby
Not selected	X	L	X	X	High-Z	Standby
Selected	L	H	H	H	High-Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

Notes:

(1) X = don't care.

Ordering Information

Catalog Part Number	Access Time (max)	I_{SB1} (max)	Package
μPD431000ACZ-70L	70 ns	0.1 mA	32-pin plastic DIP
CZ-85L	85 ns		
CZ-10L	100 ns		
μPD431000ACZ-70LL	70 ns	0.05 mA	
CZ-85LL	85 ns		
CZ-10LL	100 ns		
μPD431000AGW-70L	70 ns	0.1 mA	32-pin plastic miniflat
GW-85L	85 ns		
GW-10L	100 ns		
μPD431000AGW-70LL	70 ns	0.05 mA	
GW-85LL	85 ns		
GW-10LL	100 ns		
μPD431000AGZ-70L	70 ns	0.1 mA	32-pin plastic TSOP (normal pinouts)
GZ-85L	85 ns		
GZ-10L	100 ns		
μPD431000AGZ-70LL	70 ns	0.05 mA	
GZ-85LL	85 ns		
GZ-10LL	100 ns		
μPD431000AGZM-70L	70 ns	0.1 mA	32-pin plastic TSOP (reverse pinouts)
GZM-85L	85 ns		
GZM-10L	100 ns		
μPD431000AGZM-70LL	70 ns	0.05 mA	
GZM-85LL	85 ns		
GZM-10LL	100 ns		

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		-L Version			-LL Version				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input leakage current	I_{LI}	−1		1	-1		1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−1		1	-1		1	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CE}_1$ = V_{IH}, or CE_2 = V_{IL}, or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}
Operating supply current	I_{CCA1}		40	70		40	70	mA	$\overline{CE}_1$ = V_{IL}; CE_2 = V_{IH}; t_{RC} = t_{RC} (min); $I_{I/O}$ = 0 mA
	I_{CCA2}			15			15	mA	$\overline{CE}_1$ = V_{IL}; CE_2 = V_{IH}; $I_{I/O}$ = 0 mA
	I_{CCA3}			10			10	mA	$V_{CE1} \leq 0.2$ V; $V_{CE2} \geq V_{CC} - 0.2$ V; t_{RC} or t_{WC} = 1 MHz; $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V
Standby supply current	I_{SB}			3			3	mA	$\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} (Note 1)
	I_{SB1}		0.002	0.1		0.001	0.05	mA	$\overline{CE}_1$ and $CE_2 \geq V_{CC} - 0.2$ V (Note 2)
	I_{SB2}		0.002	0.1		0.001	0.05	mA	$CE_2 \leq 0.2$ V (Note 2)
Output voltage, low	V_{OL}			0.4			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH}	2.4			2.4			V	I_{OH} = −1.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	μPD431000A-70 Min	μPD431000A-70 Max	μPD431000A-85 Min	μPD431000A-85 Max	μPD431000A-10 Min	μPD431000A-10 Max	Unit	Test Conditions
Read Operation									
Read cycle time	t_{RC}	70		85		100		ns	
Address access time	t_{AA}		70		85		100	ns	(Note 2)
$\overline{CE}_1$ access time	t_{CO1}		70		85		100	ns	(Note 2)
CE_2 access time	t_{CO2}		70		85		100	ns	(Note 2)
Output enable to output valid	t_{OE}		35		45		50	ns	(Note 2)
Output hold from address change	t_{OH}	10		10		10		ns	
$\overline{CE}_1$ to output in low-Z	t_{LZ1}	10		10		10		ns	(Note 3)
CE_2 to output in low-Z	t_{LZ2}	10		10		10		ns	(Note 3)
Output enable to output in low-Z	t_{OLZ}	5		5		5		ns	(Note 3)
$\overline{CE}_1$ to output in high-Z	t_{HZ1}		25		30		35	ns	(Note 3)
CE_2 to output in high-Z	t_{HZ2}		25		30		35	ns	(Note 3)
Output enable to output in high-Z	t_{OHZ}		25		30		35	ns	(Note 3)
Write Operation									
Write cycle time	t_{WC}	70		85		100		ns	
$\overline{CE}_1$ to end of write	t_{CW1}	55		70		85		ns	
CE_2 to end of write	t_{CW2}	55		70		85		ns	
Address valid to end of write	t_{AW}	55		70		85		ns	
Address setup time	t_{AS}	0		0		0		ns	
Write pulse width	t_{WP}	50		60		70		ns	
Write recovery time	t_{WR}	5		5		5		ns	
Data valid to end of write	t_{DW}	35		35		40		ns	
Data hold time	t_{DH}	0		0		0		ns	
Write enable to output in high-Z	t_{WHZ}		25		30		35	ns	(Note 3)
Output active from end of write	t_{OW}	5		5		5		ns	(Note 3)

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output loading.

(3) See figure 2 for output loading.

Figure 1. Output Loading

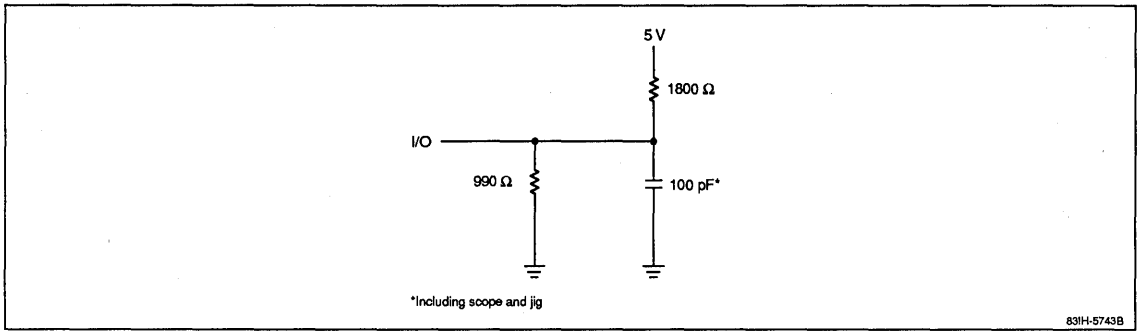
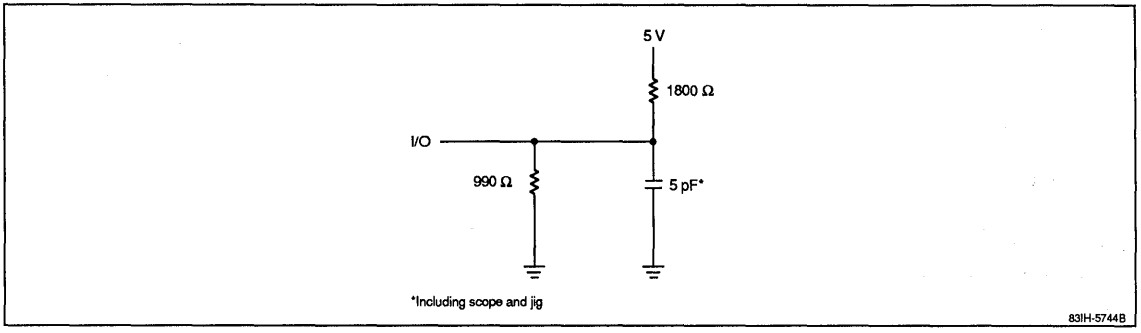


Figure 2. Output Loading for t_{HZ1}, t_{HZ2}, t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{OHZ}, t_{OW}, and t_{WHZ}



Low V_{CC} Data Retention Characteristics

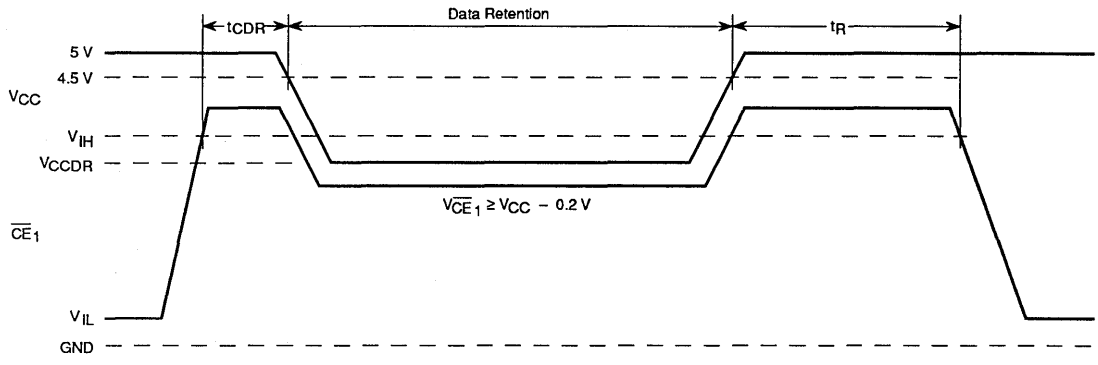
T_A = 0 to +70°C

Parameter	Symbol	-L Version Min	-L Version Typ	-L Version Max	-LL Version Min	-LL Version Typ	-LL Version Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR1}	2		5.5	2		5.5	V	$\overline{CE_1} \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V
	V_{CCDR2}	2		5.5	2		5.5	V	$CE_2 \leq 0.2$ V
Data retention supply current	I_{CCDR1}		1	50		0.5	20	μA	$V_{CC} = 3.0$ V; $\overline{CE_1} \geq V_{CC} - 0.2$ V; $CE_2 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V (Note 1)
	I_{CCDR2}		1	50		0.5	20	μA	$V_{CC} = 3.0$ V; $CE_2 \leq 0.2$ V (Note 1)
Chip deselection to data retention	t_{CDR}	0			0			ns	
Operation recovery time	t_R	5			5			ms	

Notes:

(1) At 0 to 40°C, the maximum for I_{CCDR1} and I_{CCDR2} is 15 μA for the -L version and 3 μA for the -LL version.

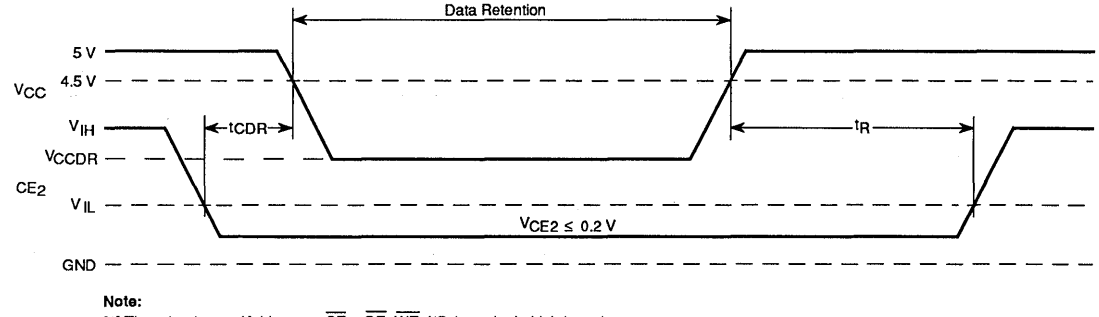
Figure 3. $\overline{CE_1}$-Controlled Data Retention Timing



Note:
[1] CE_2 must be equal to or higher than V_{CC} − 0.2 V, or equal to or lower than 0.2 V.
The other inputs (Addresses, $\overline{OE}$, $\overline{WE}$, I/Os) can be in high impedance.

83IH-5749B

Figure 4. CE_2-Controlled Data Retention Timing



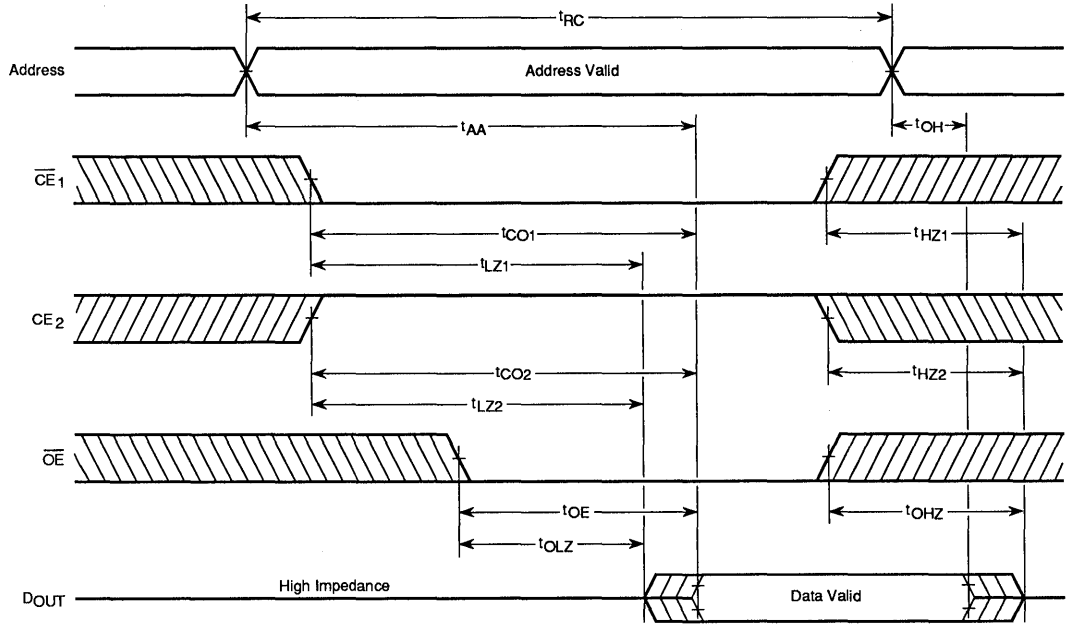
Note:
[1] The other inputs (Addresses, $\overline{CE_1}$, $\overline{OE}$, $\overline{WE}$, I/Os) can be in high impedance.

83IH-5750B

24c

Timing Waveforms

Read Cycle



Notes:

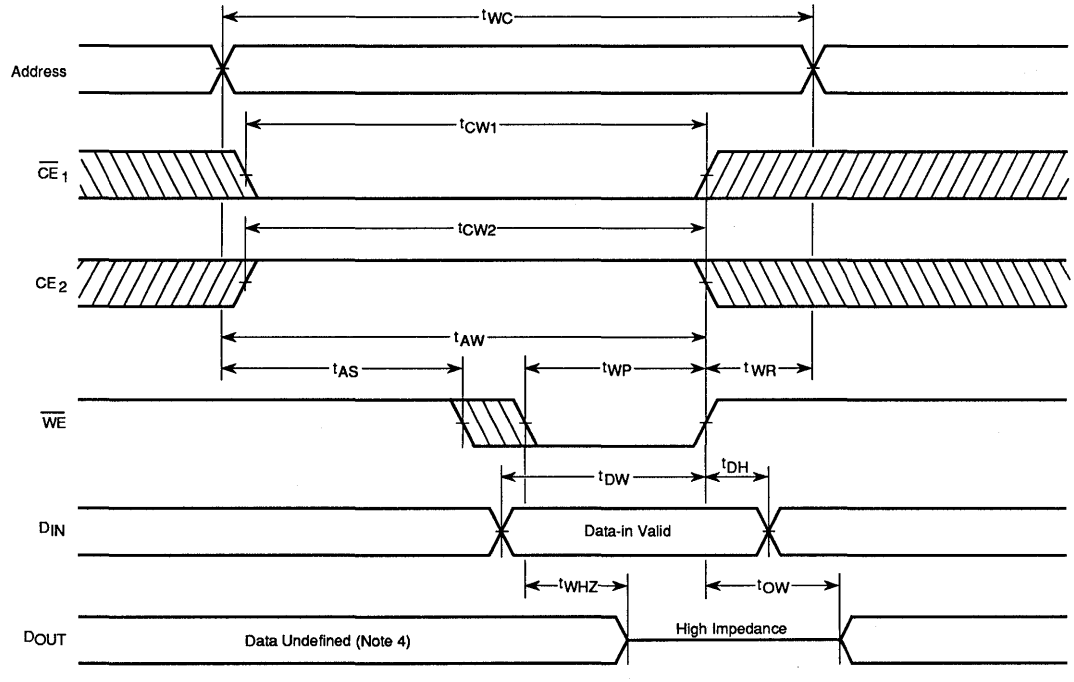
[1] $\overline{WE}$ is high for a read cycle.

[2] Address valid prior to or coincident with the latter of the low transition of $\overline{CE}_1$ or the high transition of CE_2.

83IH-5745B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

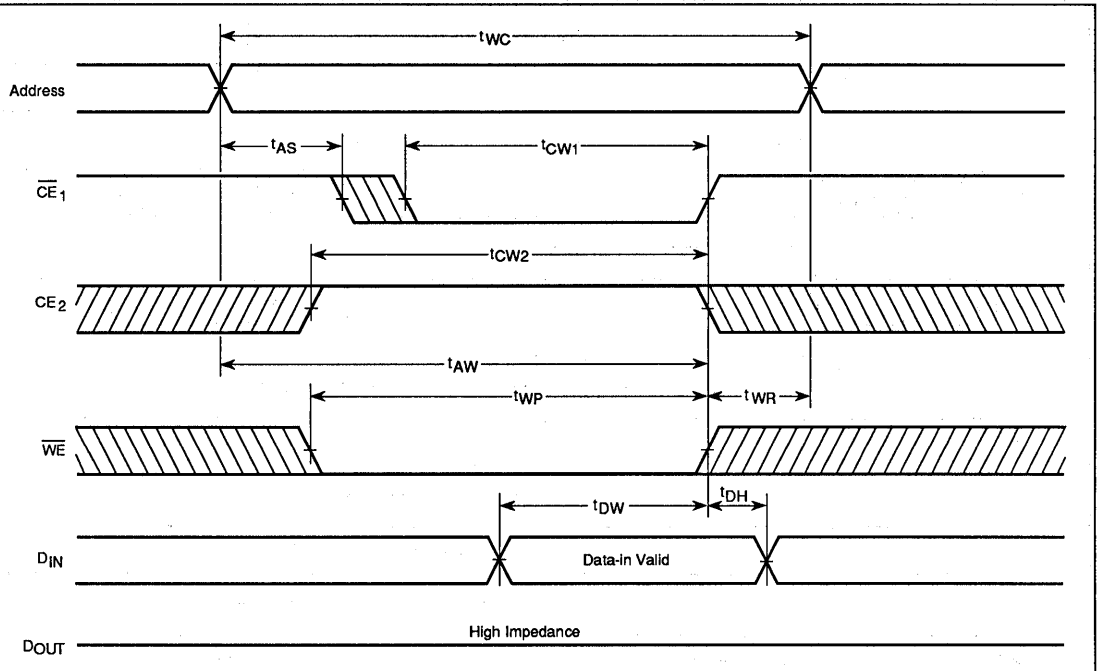
[4] During this period, the I/O pins may be in the output state; therefore, input signals of opposite phase to the output must not be applied.

83IH-5746B

24c

Timing Waveforms (cont)

$\overline{CE_1}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE_1}$ and $\overline{WE}$ and a high CE_2.

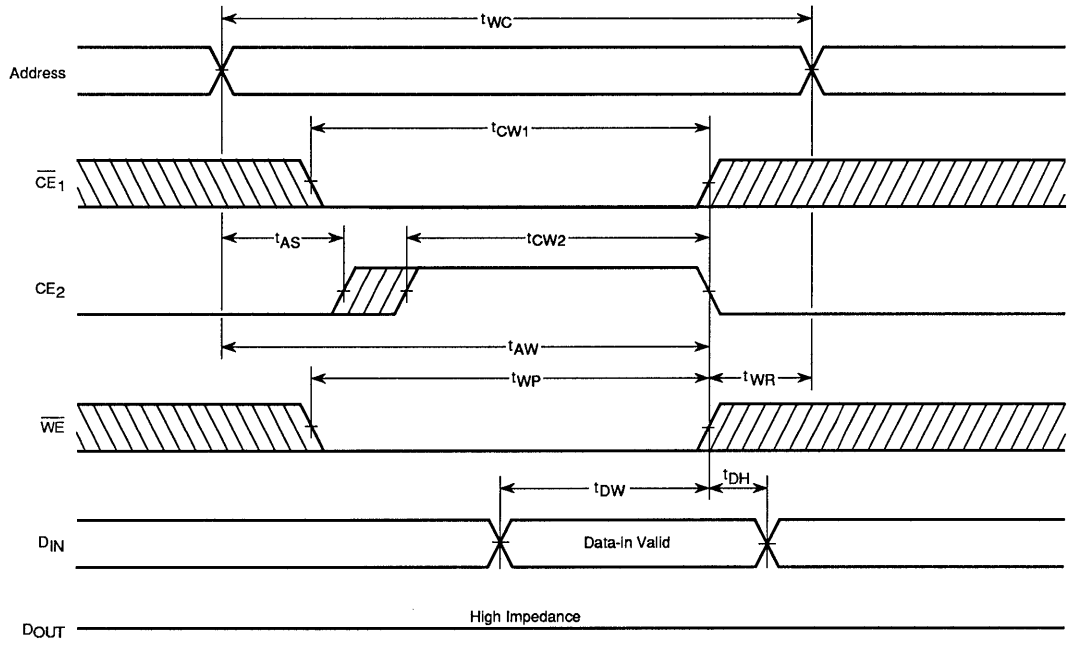
[2] $\overline{CE_1}$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

83IH-5747B

Timing Waveforms (cont)

CE_2-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CE}_1$ and $\overline{WE}$ and a high CE_2.

[2] $\overline{CE}_1$ or $\overline{WE}$ must be high or CE_2 must be low during address transition.

[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

83IH-5748B

μPD434000
524,288 x 8-Bit
Static CMOS RAM

Description

The μPD434000 is a 524,288-word by 8-bit static RAM fabricated with advanced silicon-gate technology. CMOS peripheral circuits and N-channel memory cells with thin-film transistor (TFT) loads make the μPD434000 a high-speed device that requires very low power and no clock or refreshing.

Minimum standby power is drawn when $\overline{CS}$ is high, independent of $\overline{OE}$ and $\overline{WE}$. Data retention is guaranteed at a power supply voltage as low as 2 volts.

The μPD434000 is available in standard 32-pin DIP, SOP, and TSOP plastic packaging.

Features

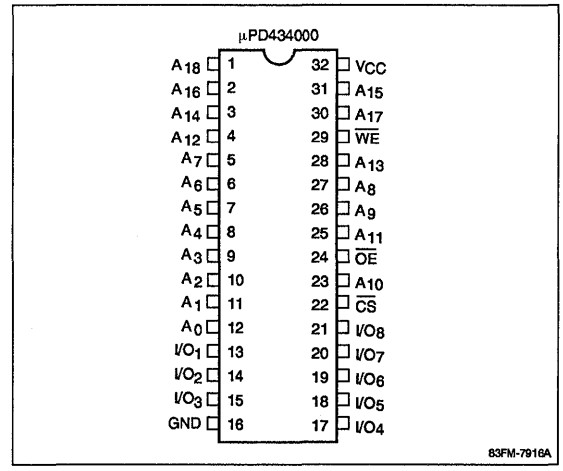
- 524,288-word by 8-bit organization
- Single +5-volt power supply
- Fully static operation—no clock or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- Chip select ($\overline{CS}$) and output enable ($\overline{OE}$) inputs for easy application
- Data retention current of 0.5 μA typical
- Data retention voltage of 2 V minimum
- Packages: 32-pin plastic DIP, SOP, and TSOP

Pin Identification

Symbol	Function
A_0 - A_{18}	Address inputs
I/O_1 - I/O_8	Data inputs/outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

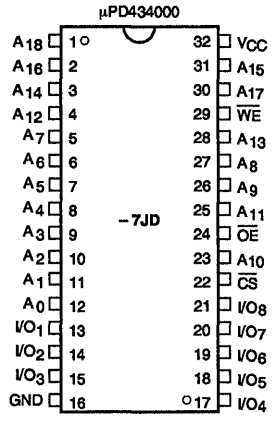
Pin Configurations

32-Pin Plastic DIP or SOP



Pin Configurations (cont)

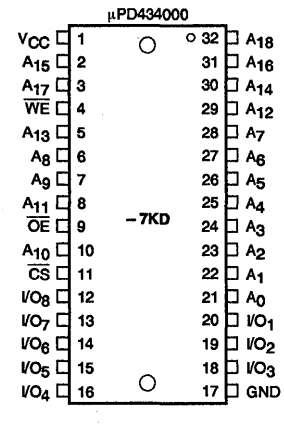
32-Pin Plastic TSOP (Normal Pinouts)



Suffix –7JD in the package identifier denotes normal pinout sequence.

83FM-8618A

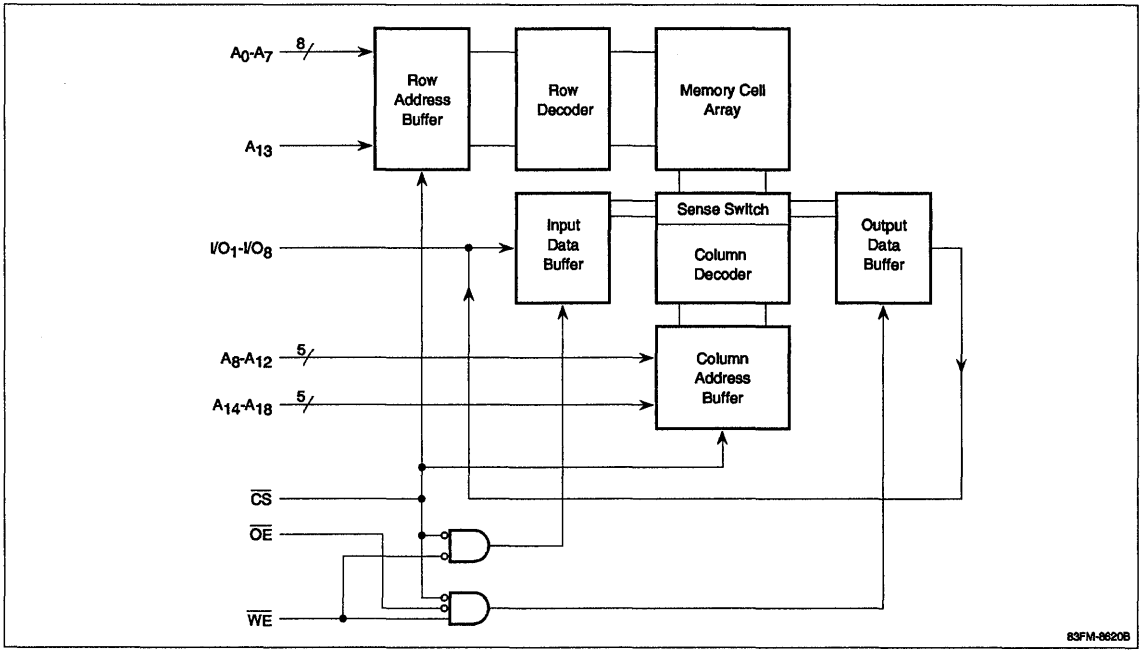
32-Pin Plastic TSOP (Reverse Pinouts)



Suffix –7KD in the package identifier denotes normal pinout sequence.

83FM-8619A

Block Diagram



83FM-8620B

Ordering Information

Part Number	Access Time (max)	Standby Supply Current	Package
μPD434000CZ-55	55 ns	2 mA	32-pin plastic DIP
CZ-70	70 ns		
CZ-85	85 ns		
CZ-10	100 ns		
μPD434000CZ-55L	55 ns	0.1 mA	
CZ-70L	70 ns		
CZ-85L	85 ns		
CZ-10L	100 ns		
μPD434000CZ-55LL	55 ns	0.05 mA	
CZ-70LL	70 ns		
CZ-85LL	85 ns		
CZ-10LL	100 ns		
μPD434000GW-55	55 ns	2 mA	32-pin plastic SOP
GW-70	70 ns		
GW-85	85 ns		
GW-10	100 ns		
μPD434000GW-55L	55 ns	0.1 mA	
GW-70L	70 ns		
GW-85L	85 ns		
GW-10L	100 ns		
μPD434000GW-55LL	55 ns	0.05 mA	
GW-70LL	70 ns		
GW-85LL	85 ns		
GW-10LL	100 ns		

Ordering Information (cont)

Part Number	Access Time (max)	Standby Supply Current	Package
μPD434000G5-55	55 ns	2 mA	32-pin plastic TSOP (normal pinouts)
G5-70	70 ns		
G5-85	85 ns		
G5-10	100 ns		
μPD434000G5-55L	55 ns	0.1 mA	
G5-70L	70 ns		
G5-85L	85 ns		
G5-10L	100 ns		
μPD434000G5-55LL	55 ns	0.05 mA	
G5-70LL	70 ns		
G5-85LL	85 ns		
G5-10LL	100 ns		
μPD434000G5M-55	55 ns	2 mA	32-pin plastic TSOP (reverse pinouts)
G5M-70	70 ns		
G5M-85	85 ns		
G5M-10	100 ns		
μPD434000G5M-55L	55 ns		
G5M-70L	70 ns	0.1 mA	
G5M-85L	85 ns		
G5M-10L	100 ns		
μPD434000G5M-55LL	55 ns		
G5M-70LL	70 ns	0.05 mA	
G5M-85LL	85 ns		
G5M-10LL	100 ns		

Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) −3.0 V minimum (pulse width = 30 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter †	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			6	pF
Input/output capacitance	$C_{I/O}$			10	pF

† Parameter is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Note:

(1) −3.0 V minimum (pulse width = 30 ns).

Truth Table

Function	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	High-Z	Standby
D_{OUT} disabled	L	H	H	High-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active

X = don't care.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		μPD434000			μPD434000-L			μPD434000-LL				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}	−1		1	−1		1	−1		1	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}	−1		1	−1		1	−1		1	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{CS}$ = V_{IH}
Operating supply current	I_{CCA2}			15			15			15	mA	$I_{I/O}$ = 0 mA; $\overline{CS}$ = V_{IL}
	I_{CCA3}			15			15			15	mA	$\overline{CS}$ ≤ 0.2 V; t_{RC} = 1 μs; V_{IL} ≤ 0.2 V; V_{IH} ≥ V_{CC} − 0.2 V; $I_{I/O}$ = 0 mA
Standby supply current	I_{SB}			5			3			3	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}		0.02	2		0.002	0.1		0.001	0.05	mA	$\overline{CS}$ ≥ V_{CC} − 0.2 V
Output voltage, low	V_{OL}			0.4			0.4			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH1}	2.4			2.4			2.4			V	I_{OH} = −1.0 mA
	V_{OH2}	V_{CC} − 0.5			V_{CC} − 0.5			V_{CC} − 0.5			V	I_{OH} = −0.1 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; see figure 1 for ac test conditions.

		-55		-70		-85		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Operating supply current	I_{CCA1}		70		65		60		55	mA	$\overline{CS}$ = V_{IL}; t_{RC} = t_{RC} (min); $I_{I/O}$ = 0 mA
Address access time	t_{AA}		55		70		85		100	ns	
$\overline{CS}$ access time	t_{ACS}		55		70		85		100	ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address valid to end of write	t_{AW}	50		60		70		80		ns	
$\overline{CS}$ to output in high-Z	t_{CHZ}		25		30		30		35	ns	
$\overline{CS}$ to output in low-Z	t_{CLZ}	10		10		10		10		ns	
$\overline{CS}$ to end of write	t_{CW}	50		60		70		80		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Data valid to end of write	t_{DW}	30		35		35		40		ns	
Output enable to output valid	t_{OE}		30		35		45		50	ns	
Output hold from address change	t_{OH}	10		10		10		10		ns	
Output enable to output in high-Z	t_{OHZ}		25		30		30		35	ns	
Output enable to output in low-Z	t_{OLZ}	5		5		5		5		ns	
Output active from end of write	t_{OW}	5		5		5		5		ns	
Read cycle time	t_{RC}	55		70		85		100		ns	
Write cycle time	t_{WC}	55		70		85		100		ns	
Write enable to output in high-Z	t_{WHZ}		25		30		30		35	ns	
Write pulse width	t_{WP}	45		55		65		70		ns	
Write recovery time	t_{WR}	5		5		5		5		ns	

Low V_{CC} Data Retention Characteristics

T_A = 0 to +70°C; see figure 2 for timing diagram.

		-L Version			-LL Version				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Data retention supply voltage	V_{CCDR1}	2		5.5	2		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	† I_{CCDR1}		1	50		0.5	20	μA	V_{CC} = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2$ V
Chip deselection to data retention	t_{CDR}	0			0			ns	
Operation recovery time	t_R	5			5			ms	

† At 0 to 40°C, the maximum for I_{CCDR1} is 15 μA for the -L version and 3 μA for the -LL version.

Figure 1. AC Test Conditions

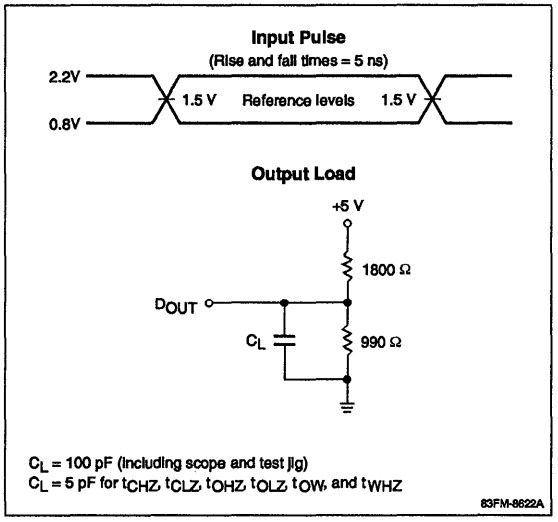
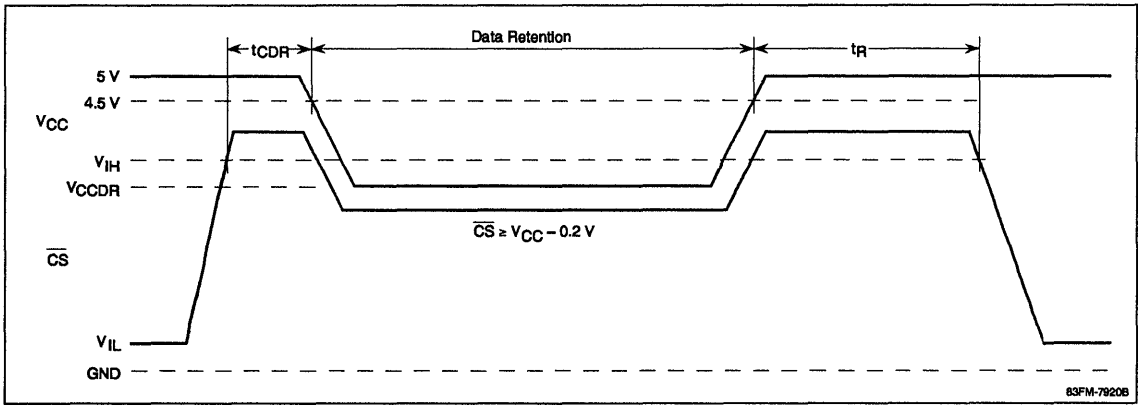
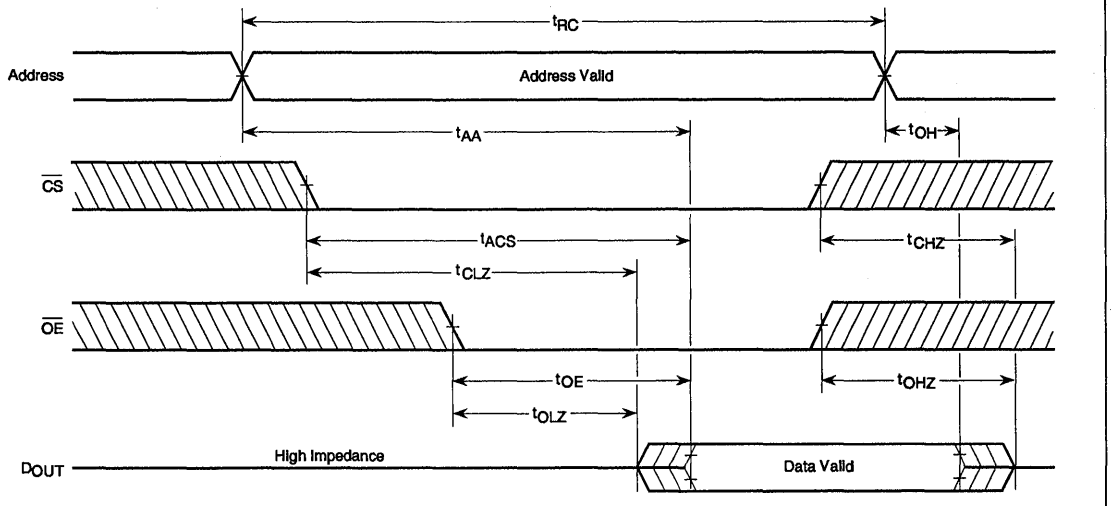


Figure 2. Data Retention Timing



Timing Waveforms

Read Cycle



Notes:
[1] $\overline{WE}$ is high for a read cycle.

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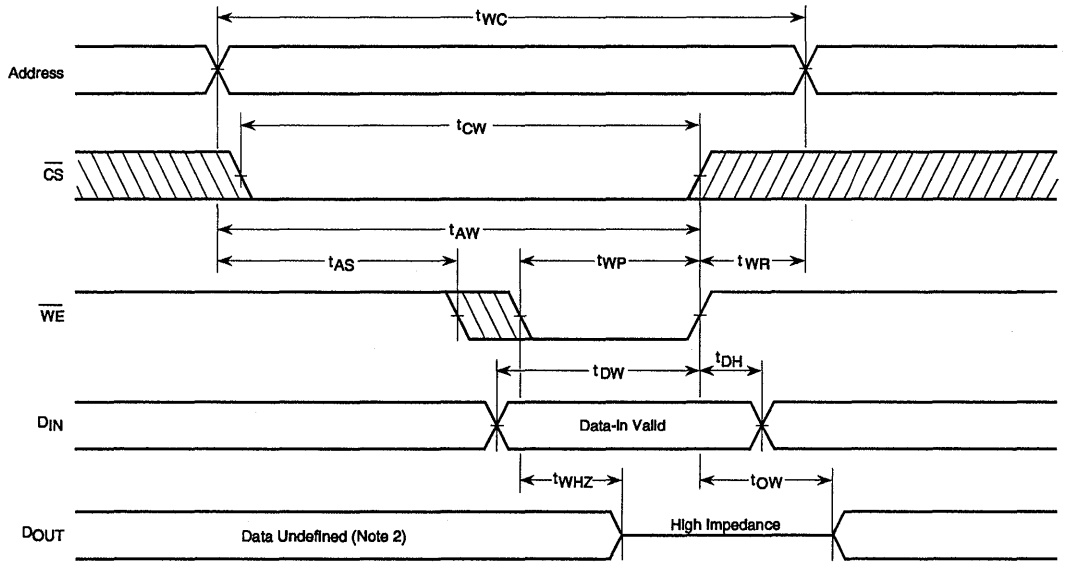
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[2] During this period, the I/O pins may be in the output state; therefore, input signals of opposite phase to the output must not be applied.

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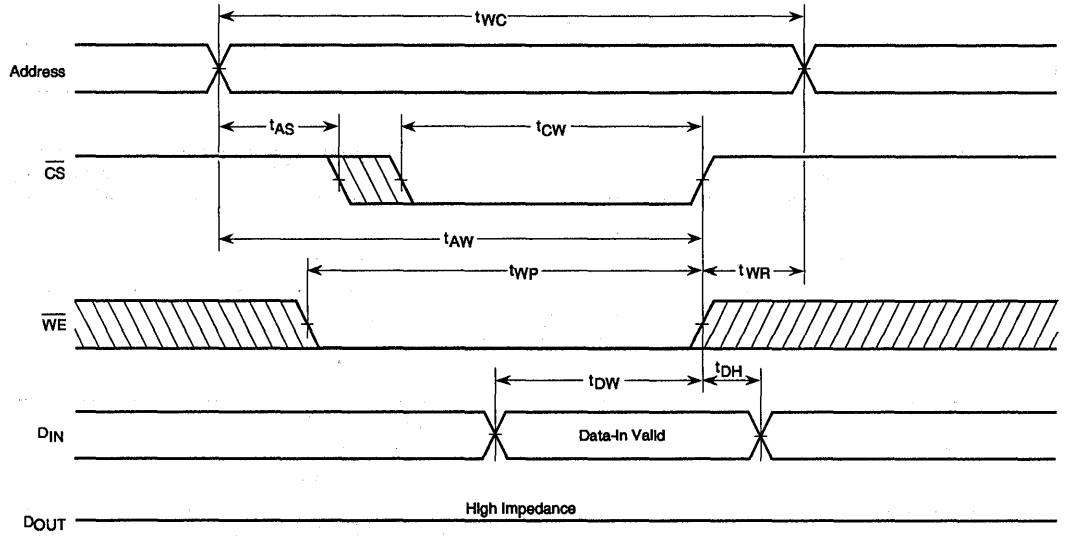
Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

83FM-7923B

NEC Electronics Inc.

MC-434000
524,288 x 8-Bit
Static CMOS RAM Module

Advance Information

Description

The MC-434000 is a high-density 4M static RAM module with four 128K x 8-bit SRAMs and one decoder circuit. The module is compatible with the future 4M monolithic SRAM—with TTL-compatible inputs and outputs and fully asynchronous circuitry that requires no clocks or refreshing and provides equal access and cycle times for ease of use.

The MC-434000 operates from a +5-volt power supply and is available in a standard 600-mil, 32-pin ceramic DIP or a JEDEC-type 32-pin plastic (FR-4) DIP.

Features

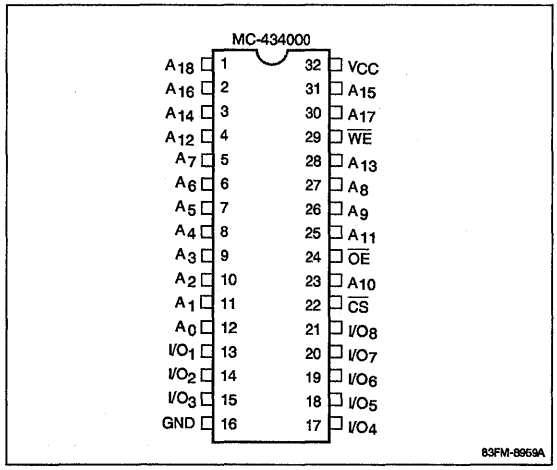
- 524,288-word by 8-bit organization
- Single +5-volt power supply
- Fully static operation—no clocks or refreshing
- TTL-compatible inputs and outputs
- Common I/O using three-state outputs
- One $\overline{CS}$ pin and one $\overline{OE}$ pin for easy application
- 32-pin ceramic and plastic (FR-4) DIP packaging

Pin Identification

Symbol	Function
A_0 - A_{18}	Address inputs
I/O_1 - I/O_8	Data inputs/outputs
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

Pin Configuration

32-Pin Ceramic or Plastic (FR-4) DIP

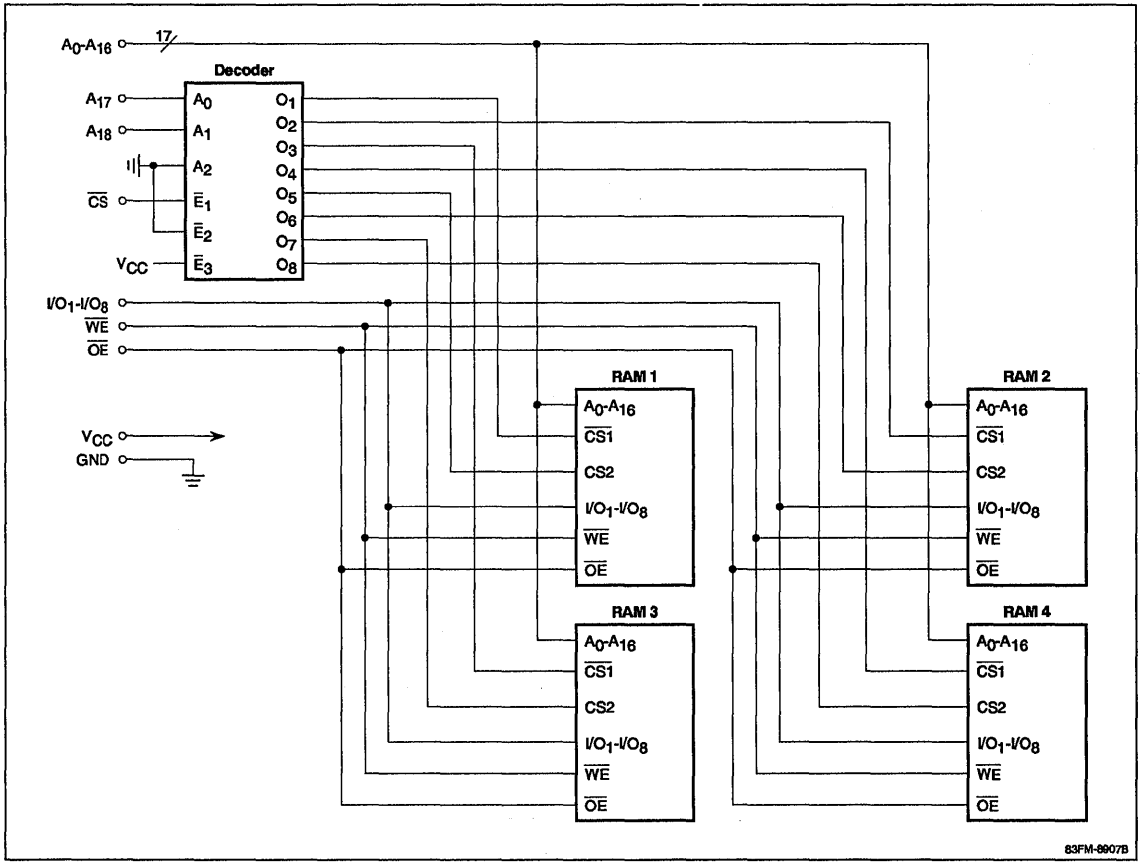


Ordering Information

Catalog Part Number	Access Time (max)	Package
MC-434000D-85	85 ns	32-pin ceramic DIP
D-10	100 ns	
MC-434000E-85	85 ns	32-pin plastic (FR-4) DIP
E-10	100 ns	

24e

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC} (Note 1)	−0.5 to +7.0 V
Input voltage, V_{IN} (Note 1)	−0.5 to V_{CC} + 0.5 V
Output voltage, $V_{I/O}$ (Note 1)	−0.5 to V_{CC} + 0.5 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Note:

(1) −3.0 V minimum (pulse width = 30 ns).

Capacitance

T_A = +25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Max	Unit	Pins
Input capacitance	C_{IN}	45	pF	A_0 - A_{18}, $\overline{WE}$, $\overline{OE}$, $\overline{CS}$
Input/output capacitance	$C_{I/O}$	50	pF	I/O_1 - I/O_8

Note: Capacitance is sampled and not 100% tested.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Input voltage, high	V_{IH}	2.2		V_{CC} + 0.5	V
Ambient temperature	T_A	0		70	°C

Note: −3.0 V minimum (pulse width = 30 ns).

Truth Table

Function	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Not selected	H	X	X	High-Z	Standby
Selected	L	H	H	High-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active

X = don't care.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI}			2	μA	V_{IN} = 0 V to V_{CC}
I/O leakage current	I_{LO}			2	μA	$V_{I/O}$ = 0 V to V_{CC}; $\overline{CS1}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}
Operating supply current	I_{CCA1}		48	89	mA	$\overline{CS1}$ = V_{IL}; t_{RC} = t_{RC} (min); $I_{I/O}$ = 0 mA
	I_{CCA2}		19	46	mA	$\overline{CS1}$ = V_{IL}; $I_{I/O}$ = 0 mA
	I_{CCA3}			36	mA	$\overline{CS}$ ≤ 0.2 V; t_{RC} or t_{WC} = 1 MHz; V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} − 0.2 V
Standby supply current	I_{SB}		4	12	mA	$\overline{CS1}$ = V_{IH} (Note 1)
	I_{SB1}		8	400	μA	$\overline{CS}$ ≥ V_{CC} − 0.2 V (Note 2)
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output voltage, high	V_{OH}	2.4			V	I_{OH} = −1.0 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

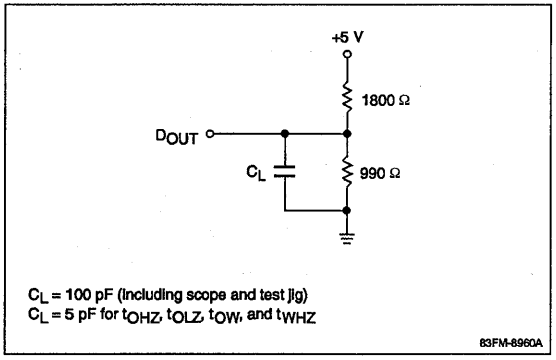
Parameter	Symbol	MC-434000-85 Min	MC-434000-85 Max	MC-434000-10 Min	MC-434000-10 Max	Unit
Read Operation						
Read cycle time	t_{RC}	85		100		ns
Address access time	t_{AA}		85		100	ns
$\overline{CS}$ access time	t_{CO}		85		100	ns
Output enable to output valid	t_{OE}		35		45	ns
Output hold from address change	t_{OH}	10		10		ns
$\overline{CS}$ to output in low-Z	t_{LZ}	10		10		ns
Output enable to output in low-Z	t_{OLZ}	5		5		ns
$\overline{CS}$ to output in high-Z	t_{HZ}		25		30	ns
Output enable to output in high-Z	t_{OHZ}		20		30	ns
Write Operation						
Write cycle time	t_{WC}	85		100		ns
$\overline{CS}$ to end of write	t_{CW}	75		90		ns
Address valid to end of write	t_{AW}	75		90		ns
Address setup time	t_{AS}	0		0		ns
Write pulse width	t_{WP}	65		75		ns
Write recovery time	t_{WR}	5		5		ns
Data valid to end of write	t_{DW}	35		40		ns
Data hold time	t_{DH}	0		0		ns
Write enable to output in high-Z	t_{WHZ}		30		35	ns
Output active from end of write	t_{OW}	5		5		ns

Notes:

(1) Input pulse levels = 0.8 to 2.2 V; input rise and fall times = 5 ns; timing reference levels = 1.5 V.

(2) See figure 1 for output load.

Figure 1. Output Load

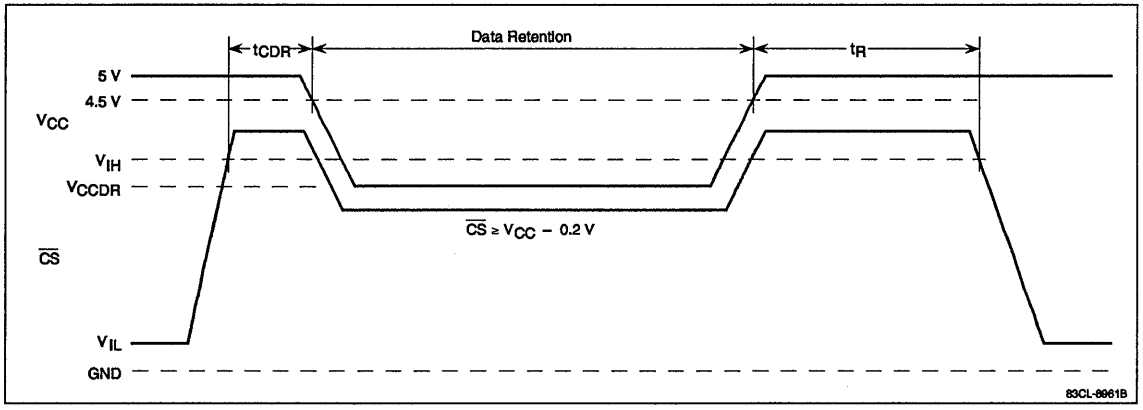


Low-V_{CC} Data Retention Characteristics

T_A = 0 to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2		5.5	V	$\overline{CS1} \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		4	200	μA	V_{CC} = 3.0 V; $\overline{CS} \geq V_{CC} - 0.2$ V
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	5			ms	

Figure 2. $\overline{CS}$-Controlled Data Retention Timing



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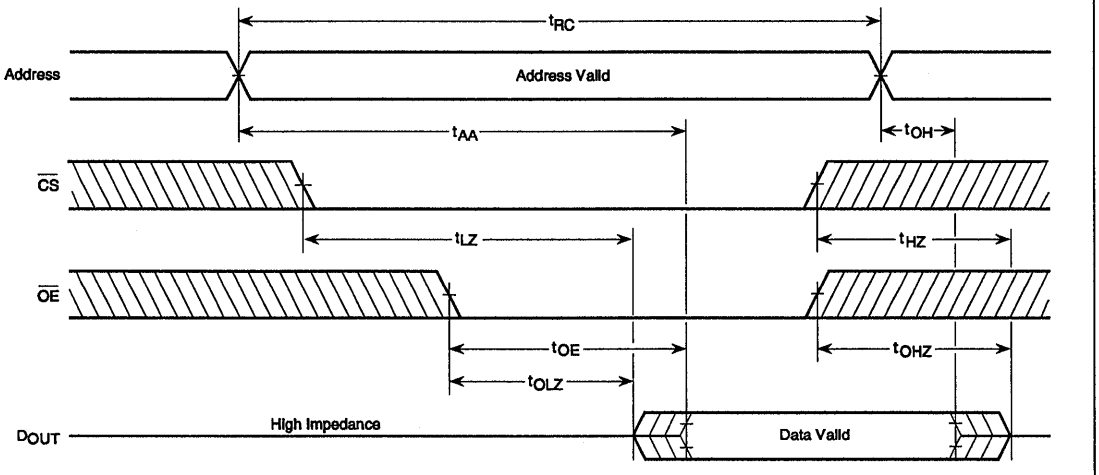
Timing Waveforms

Read Cycle



Notes:

[1] $\overline{WE}$ is high for a read cycle.

[2] Address valid prior to or coincident with the latter of the low transition of $\overline{CS}$.

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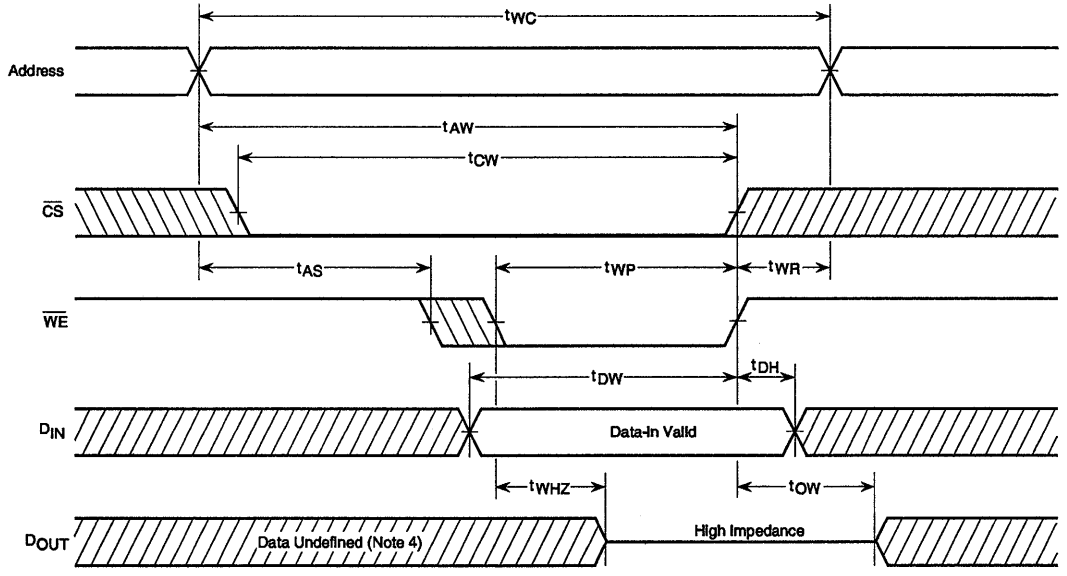
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] A write occurs during the overlap of low $\overline{CS}$ and low $\overline{WE}$.

[2] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

[3] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

[4] During this period, I/O pins are in the output state; therefore, input signals of opposite phase to the output must not be applied.

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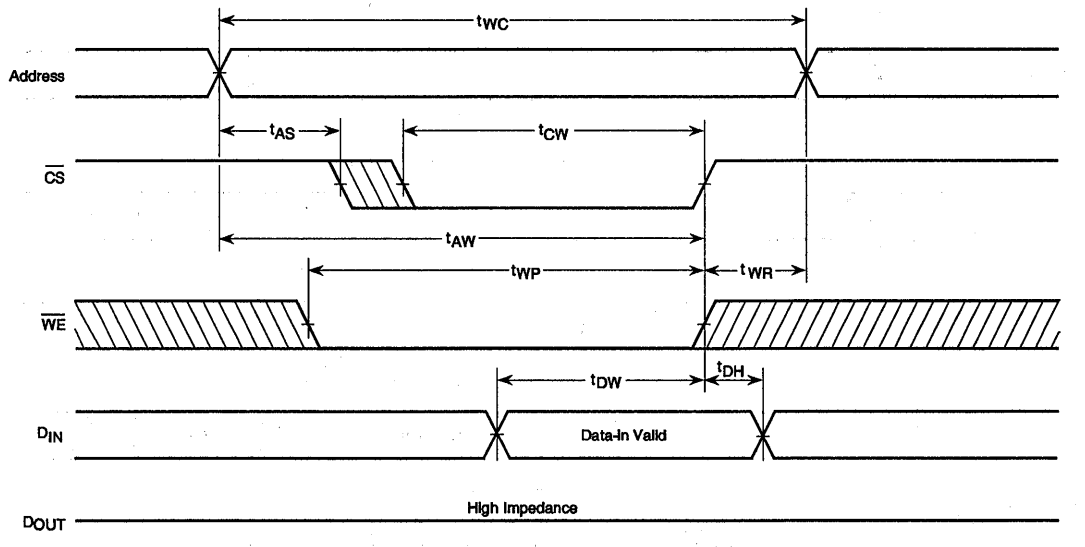
24e

Timing Waveforms (cont)

$\overline{CS}$-Controlled Write Cycle



Notes:

[1] A write cycle occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$.

[2] $\overline{CS}$ or $\overline{WE}$ must be high during address transition.

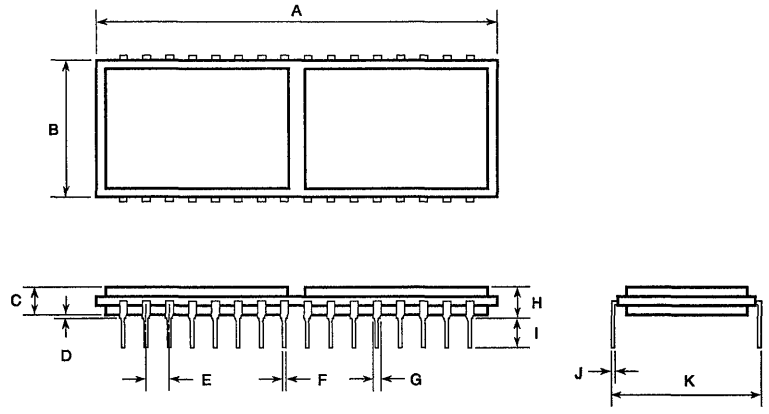
[3] If $\overline{OE}$ is high, the I/O pins remain in high impedance.

83CL-8994B

Package Drawings

32-Pin Ceramic DIP

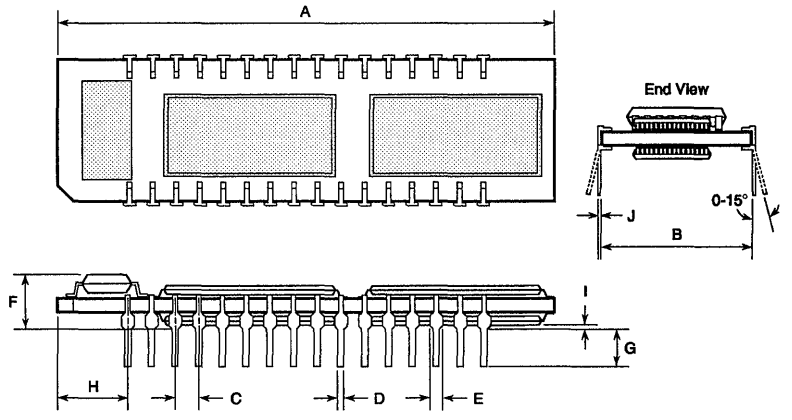
Item	Millimeters	Inches
A	43.053 ± .127	1.7 ± 0.01
B	14.99 ± .254	.59 ± 0.10
C	9.78 max	.385 max
D	0.254 ± .127	.010 ± .005
E	2.54 [TP]	.100 [TP]
F	0.508 ± .127	.02 ± .005
G	1.27 ± .381	.05 ± .015
H	10.287 max	.405 max
I	3.81 ± .635	.15 ± .025
J	0.254 ± .076	.01 ± .003
K	15.37 ± .381	.605 ± .015



83FM-8966B (8/92)

32-Pin Plastic (FR-4) DIP

Item	Millimeters	Inches
A	53.47 ± 0.13	2.105 ± .005
B	15.24	.600
C	2.54 [TP]	.100 [TP]
D	0.47 ± 0.12	.019 ± .005
E	1.02	.040
F	5.84 max	.230 max
G	2.54 min	.100 min
H	7.62	.300
I	0.38 min	.015 min
J	0.28 ± 0.08	.011 ± .003



83FM-8966B (8/92)

24e

NEC

Section 25
ECL RAMs (10K Interface)

μPB	Organization	Features	
10422	256 x 4	7-ns	25a
10470	4K x 1	10-ns	25b
10474	1K x 4	8-ns	25c
10474A	1K x 4	5-ns	25d
10474E	1K x 4	3-ns	25e
10476LL	1K x 4	6-ns	25f
10480	16K x 1	10-ns	25g
10484	4K x 4	10-ns	25h
10484A	4K x 4	5-ns	25i
10A484	4K x 4	5-ns	25j
μPD10500	256K x 1	15-ns; BiCMOS	25k

Upcoming Products

Description	Device Number	Comments
16K x 4	μPD10494	T_{AA} = 6, 7 ns; 28-pin PDIP/PFP
16K x 4	μPD10494LL	Tcycle = 10, 12 ns; 32-pin PDIP/PFP
32K x 9	μPD10509	Tcycle = 6, TDQ= 3; registered I/O, scannable; 52-pin PLCC
64K x 4	μPD10504	T_{AA} = 8, 10 ns; 32-pin PDIP/PFP

μPB10422
256 x 4-Bit
10K ECL RAM

Description

The μPB10422 is a very high-speed 10K interface ECL RAM organized as 256 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 7 and 10 ns maximum are available in 24-pin ceramic DIP packaging.

Features

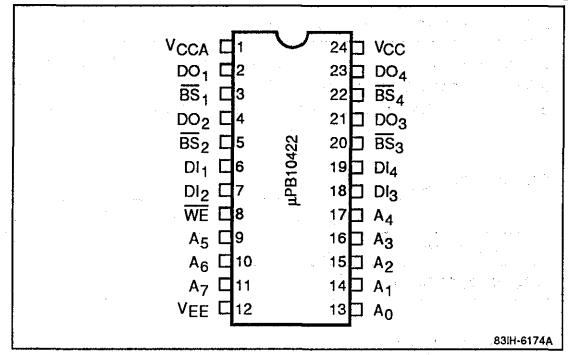
- 256-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 24-pin ceramic DIP packaging

Ordering Information

Part Number	Access Time (max)	Supply Current (min)	Package
μPB10422D-7	7 ns	−220 mA	24-pin ceramic DIP
D-10	10 ns		

Pin Configurations

24-Pin Ceramic DIP



Pin Identification

Symbol	Function
A_0 - A_7	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{BS}_1$ - $\overline{BS}_4$	Block select inputs
$\overline{WE}$	Write enable
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

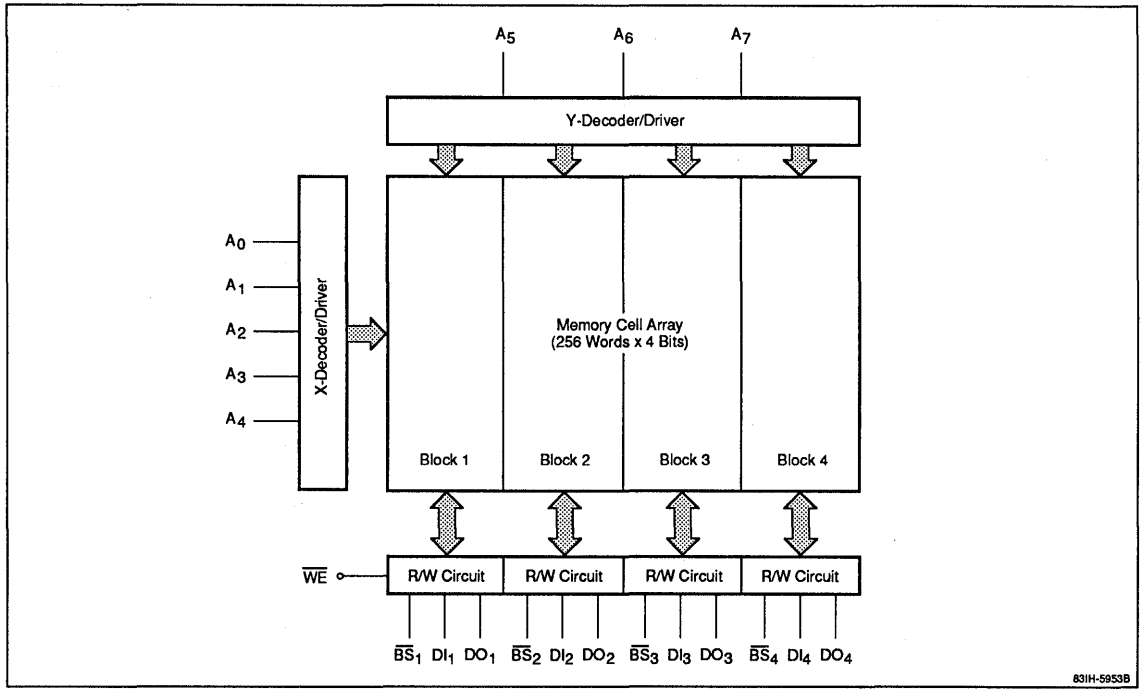
Truth Table

$\overline{BS}$	$\overline{WE}$	DI	DO	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	Data Valid	Read

Notes:

(1) The Block Select input for each of the four memory blocks is used independently as shown in the block diagram.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000	−840	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 0°C
		−960	−810	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 25°C
		−900	−720	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870	−1665	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 0°C
		−1850	−1650	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 25°C
		−1830	−1625	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020		mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 0°C
		−980		mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 25°C
		−920		mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}		−1645	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 0°C
			−1630	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 25°C
			−1605	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145	−840	mV	For all inputs: T_A = 0°C
		−1105	−810	mV	For all inputs: T_A = 25°C
		−1045	−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870	−1490	mV	For all inputs: T_A = 0°C
		−1850	−1475	mV	For all inputs: T_A = 25°C
		−1830	−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}		220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5	170	μA	$\overline{BS_1}$ - $\overline{BS_4}$; $V_{IN} = V_{IL}$ min
		−50		μA	For all others: $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−220		mA	For all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V

		μPB10422-7			μPB10422-10				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Block select access time	t_{ABS}			5			5	ns	
Block select recovery time	t_{RBS}			5			5	ns	
Address access time	t_{AA}			7			10	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			2			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	1			2			ns	
Address hold time	t_{WHA}	1			2			ns	
Block select setup time	t_{WSBS}	1			2			ns	
Block select hold time	t_{WHBS}	1			2			ns	
Write disable time	t_{WS}			5			5	ns	
Write recovery time	t_{WR}			6			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) All timing measurements are referenced to 50% input levels.

(3) See figures 1 and 2.

Figure 1. Loading Conditions Test Circuit

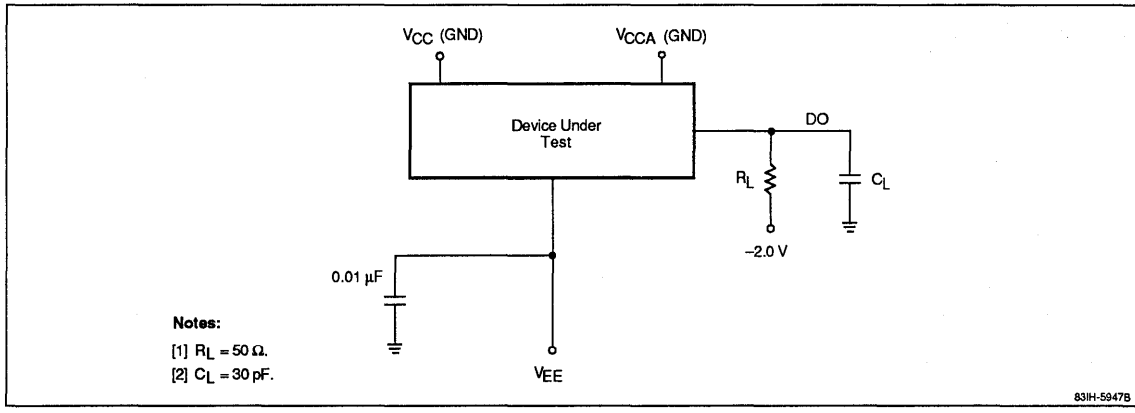
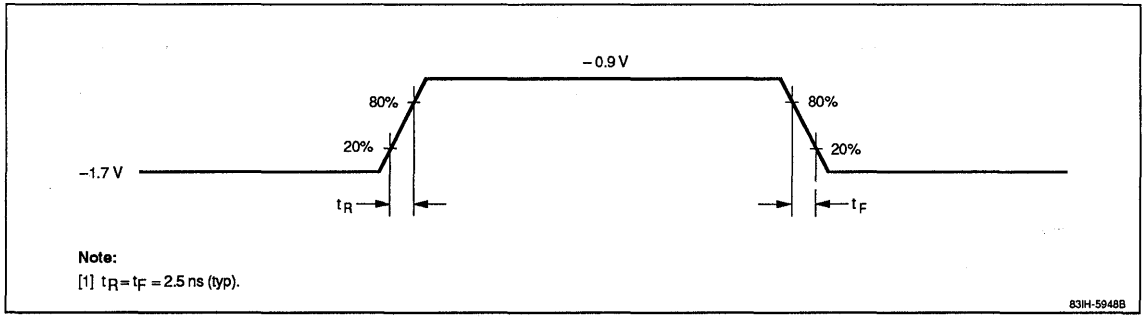
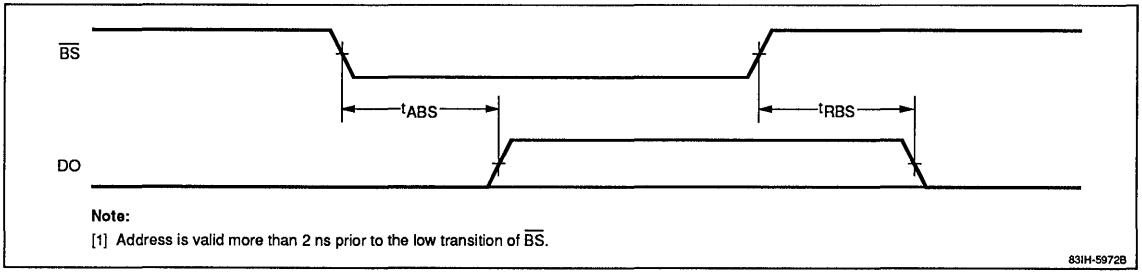


Figure 2. Input Pulse



Timing Waveforms

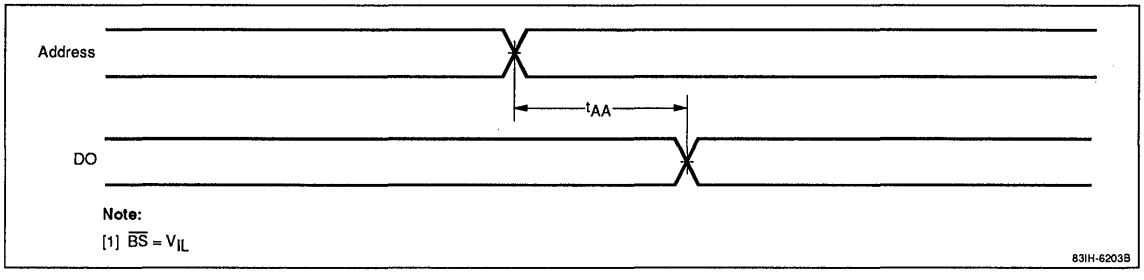
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{BS}$.

83IH-5972B

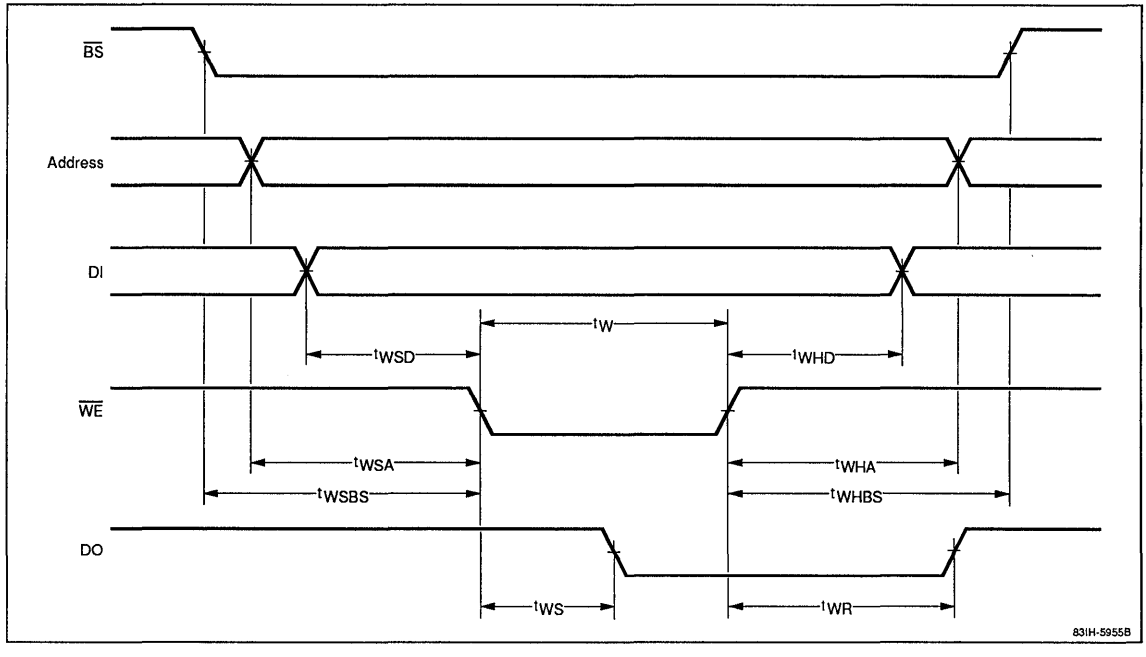
Address Access Cycle



Note:
[1] $\overline{BS} = V_{IL}$

83IH-6203B

Write Cycle



83IH-5955B

μPB10470
4,096 x 1-BIT
10K ECL RAM

Description

The μPB10470 is a very high-speed 10K interface ECL RAM organized as 4K words by 1 bit and designed with an open emitter output (noninverted) for low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB10470 is available in a hermetic, 300-mil, 18-pin cerdip.

Features

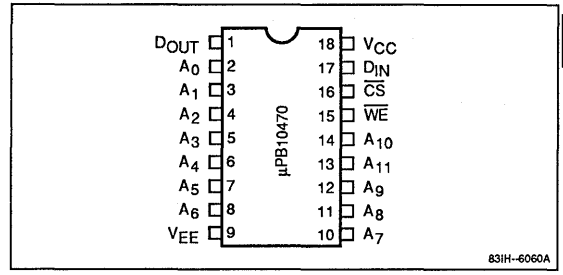
- 4096-word x 1-bit organization
- 10K ECL interface
- Open emitter output (noninverted)
- Fast access times
- Low power consumption
- 300-mil, 18-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10470D-10	10 ns	18-pin cerdip
D-15	15 ns	

Pin Configuration

18-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	–5.2-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

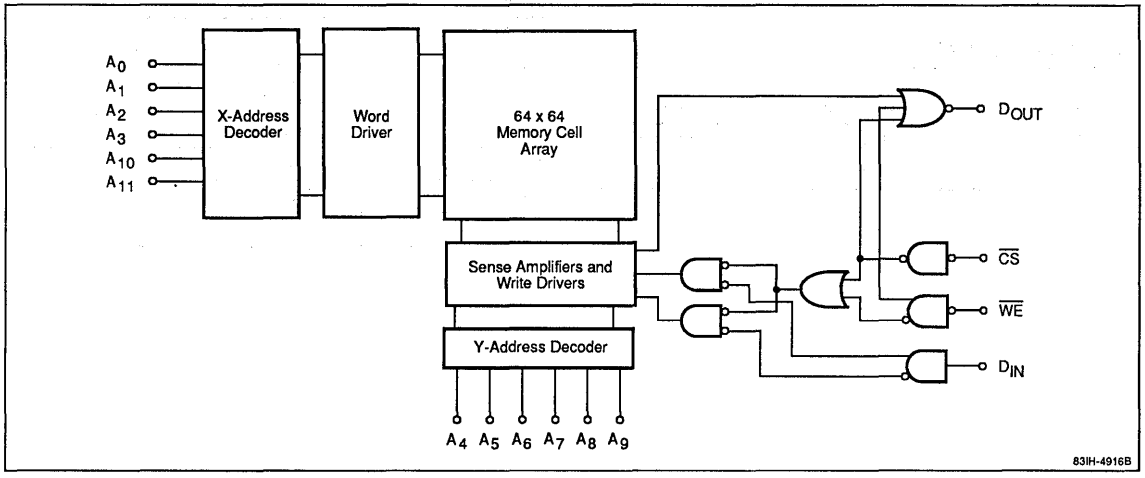
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Function	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	T_A (°C)	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	0	−1000	−840	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
		+25	−960	−810	mV	
		+75	−900	−720	mV	
Output voltage, low	V_{OL}	0	−1870	−1665	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
		+25	−1850	−1650	mV	
		+75	−1830	−1625	mV	
Output threshold voltage, high	V_{OHC}	0	−1020		mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
		+25	−980		mV	
		+75	−920		mV	
Output threshold voltage, low	V_{OLC}	0		−1645	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
		+25		−1630	mV	
		+75		−1605	mV	
Input voltage, high	V_{IH}	0	−1145	−840	mV	Guaranteed input voltage high for all inputs
		+25	−1105	−810	mV	
		+75	−1045	−720	mV	
Input voltage, low	V_{IL}	0	−1870	−1490	mV	Guaranteed input voltage low for all inputs
		+25	−1850	−1475	mV	
		+75	−1830	−1450	mV	
Input current, high	I_{IH}	0 to +75		220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0 to +75	0.5	170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		0 to +75	−50		μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	0 to +75	−220		mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

25b

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%

Parameter	Symbol	μPB10470-10			μPB10470-15			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select access time	t_{ACS}			6			8	ns	
Chip select recovery time	t_{RCS}			6			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	3			3			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			6			8	ns	
Write recovery time	t_{WR}			10			10	ns	
Output Rise and Fall Times									
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Figure 1. Loading Conditions Test Circuit

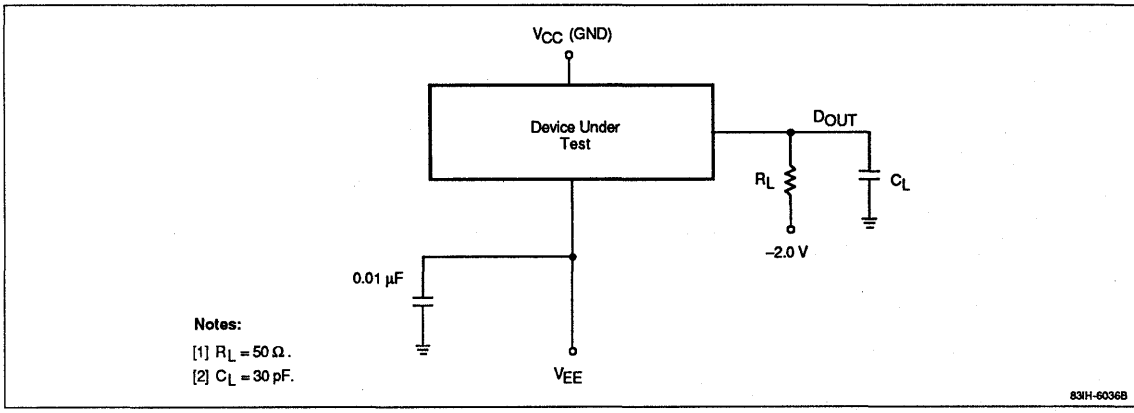
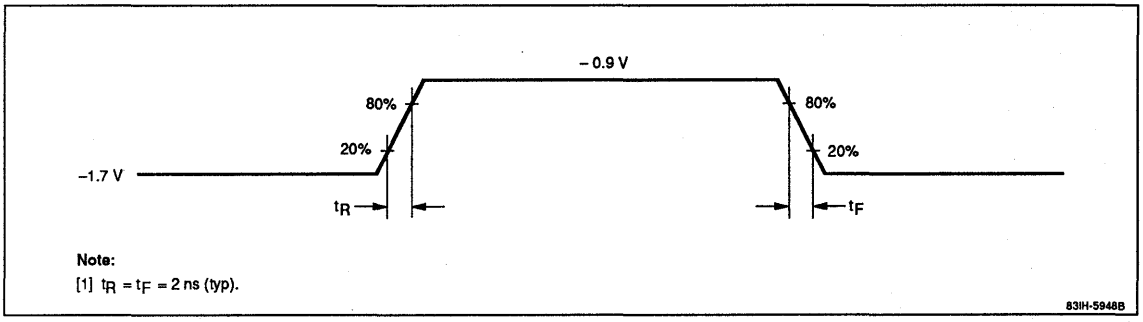
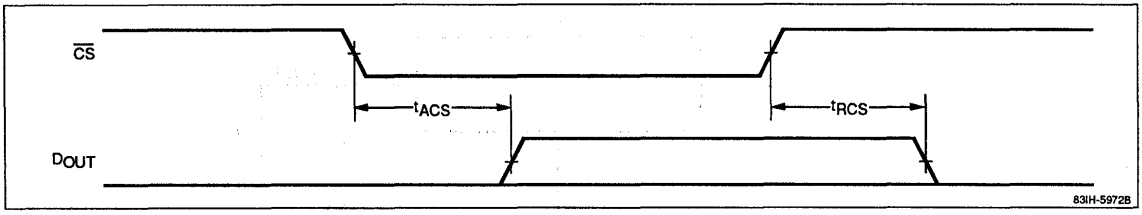


Figure 2. Input Pulse

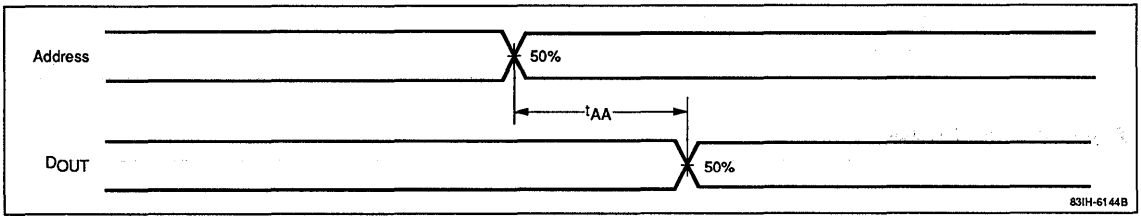


Timing Waveforms

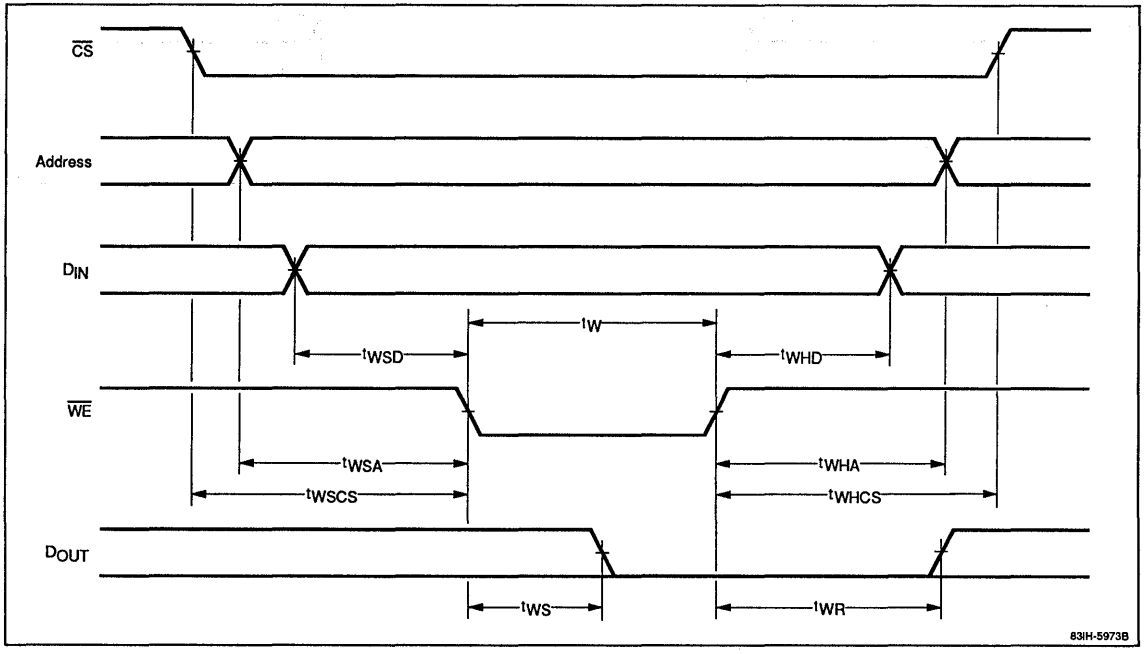
Chip Select Access Cycle



Address Access Cycle



Write Cycle



μPB10474
1,024 x 4-Bit
10K ECL RAM

Description

The μPB10474 is a very high-speed 10K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Three versions with access times of 8 ns, 10 ns and 15 ns maximum are available in hermetic, 400-mil, 24-pin cerdip packaging.

Features

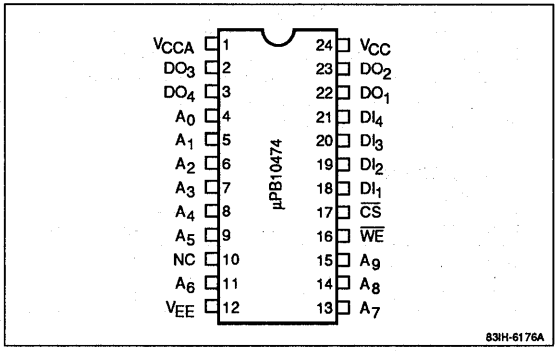
- 1,024-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10474D-8	8 ns	24-pin cerdip
D-10	10 ns	
D-15	15 ns	

Pin Configuration

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply
NC	No connection

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

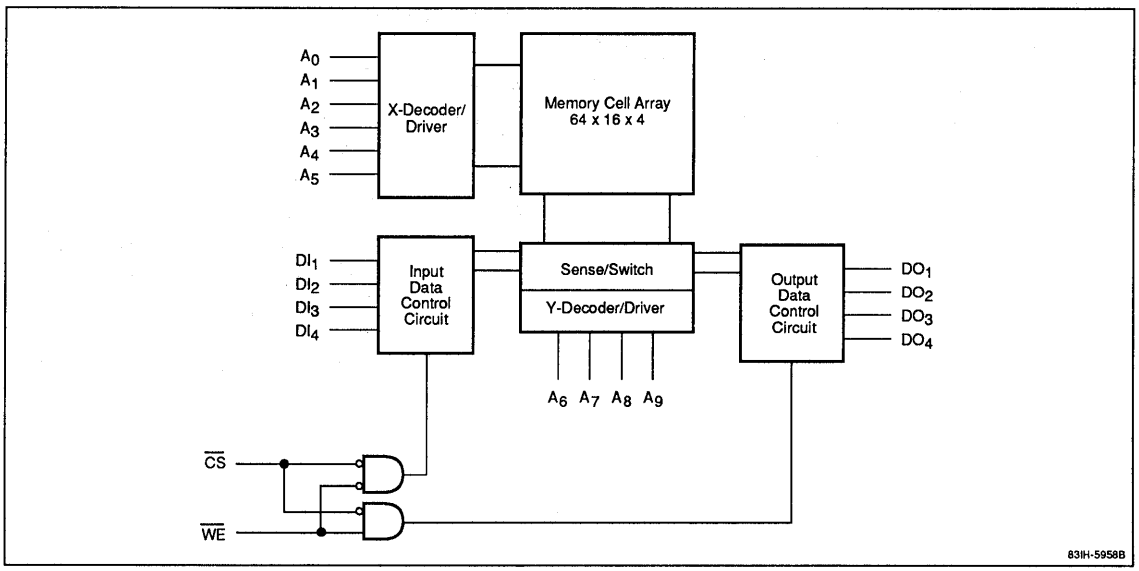
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V

		μPB10474-8			μPB10474-10			μPB10474-15				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation												
Chip select access time	t_{ACS}			5			6			8	ns	
Chip select recovery time	t_{RCS}			5			6			8	ns	
Address access time	t_{AA}			8			10			15	ns	
Write Operation												
Write pulse width	t_W	6			10			15			ns	
Data setup time	t_{WSD}	1			2			2			ns	
Data hold time	t_{WHD}	1			2			2			ns	
Address setup time	t_{WSA}	1			3			3			ns	
Address hold time	t_{WHA}	1			2			2			ns	
Chip select setup time	t_{WSCS}	1			2			2			ns	
Chip select hold time	t_{WHCS}	1			2			2			ns	
Write disable time	t_{WS}			5			6			8	ns	
Write recovery time	t_{WR}			8			10			10	ns	
Output Rise and Fall Times												
Output rise time	t_R		2			2			2		ns	
Output fall time	t_F		2			2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

25c

Figure 1. Loading Conditions Test Circuit

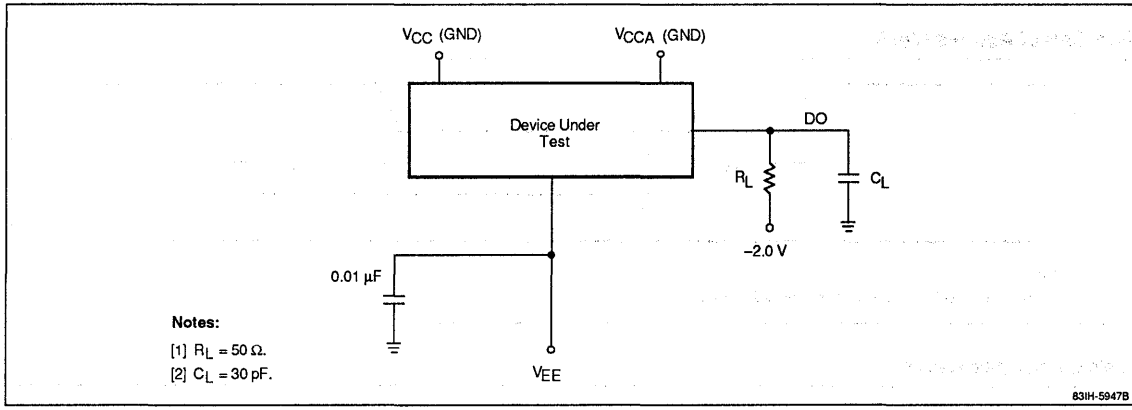
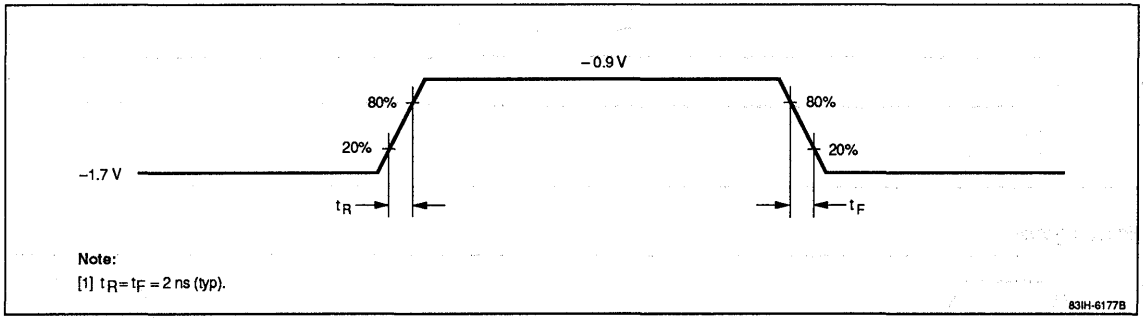
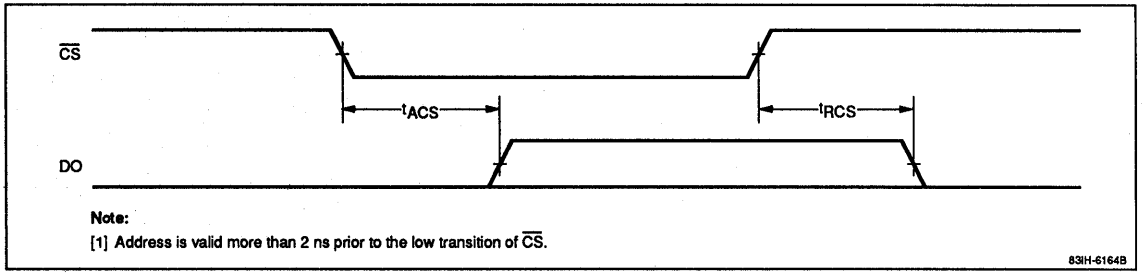


Figure 2. Input Pulse



Timing Waveforms

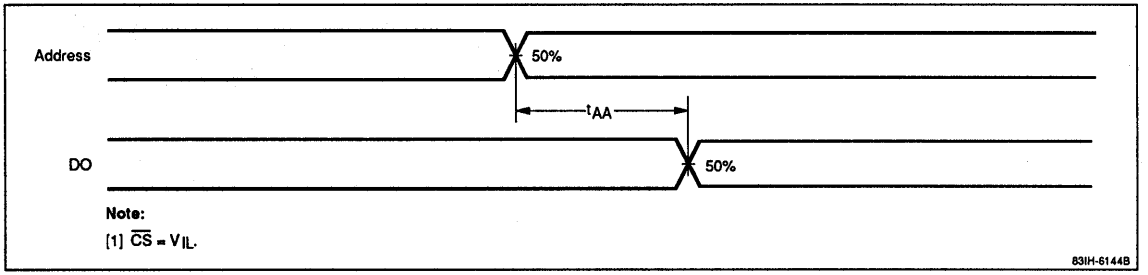
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

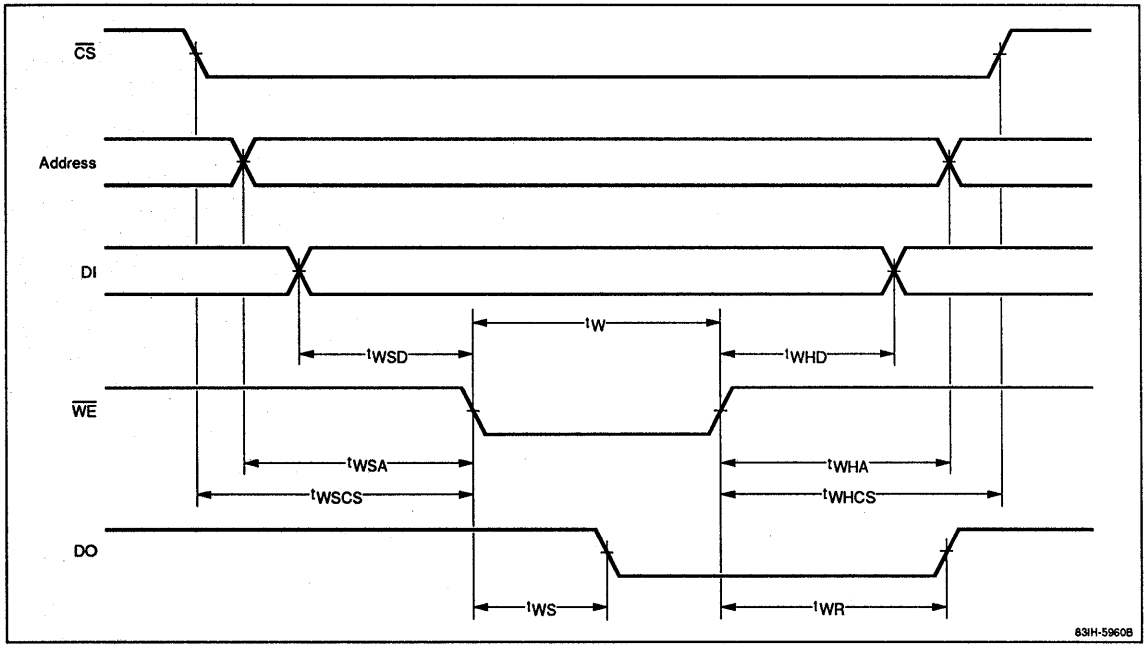
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5960B

μPB10474A
1,024 x 4-Bit
10K ECL RAM

Description

The μPB10474A is a very high-speed 10K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with access times of 5 and 6 ns maximum are available in hermetic, 400-mil, 24-pin cerdip packaging.

Features

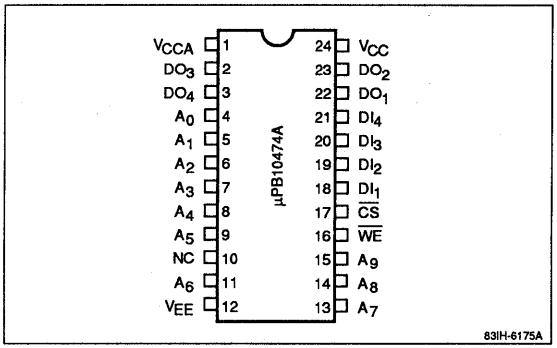
- 1,024-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB10474AD-5	5 ns	24-pin cerdip
D-6	6 ns	

Pin Configurations

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–5.2-volt power supply
NC	No connection

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0\,V$

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

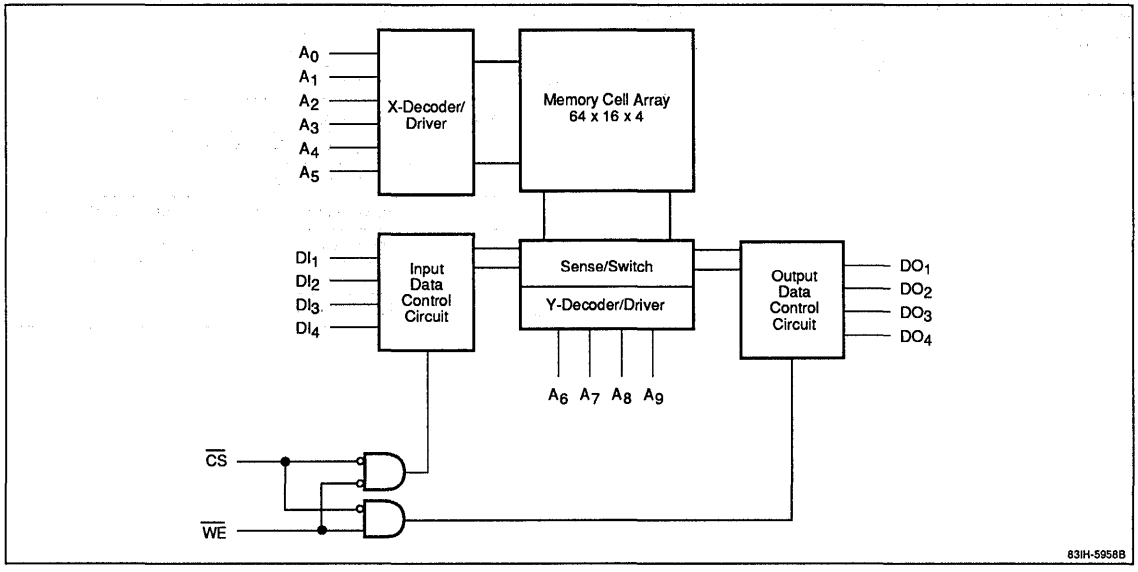
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−250			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

25d

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB10474A-5			μPB10474A-6				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			5			6	ns	
Chip select recovery time	t_{RCS}			3			4	ns	
Chip select access time	t_{ACS}			3			4	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	1			1			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	1			1			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	1			1			ns	
Write disable time	t_{WS}			3			4	ns	
Write recovery time	t_{WR}			6			7	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

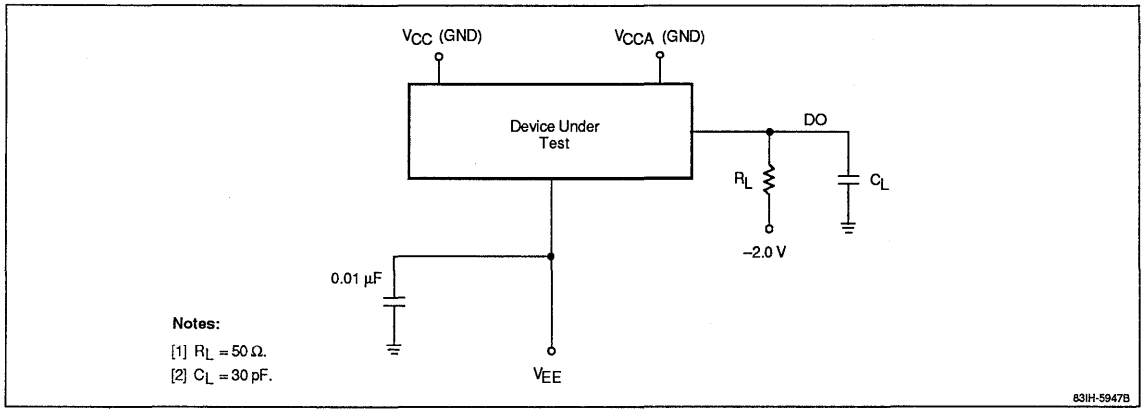
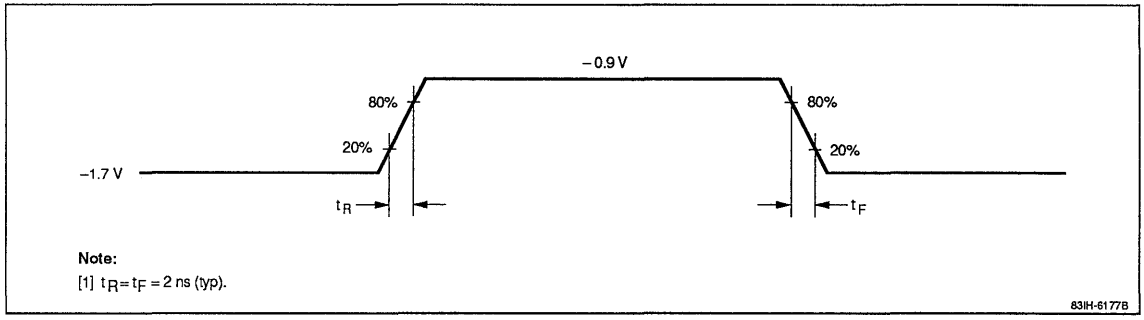
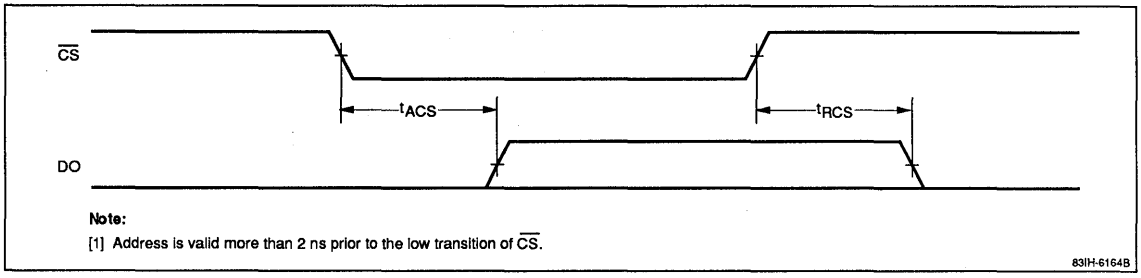


Figure 2. Input Pulse



Timing Waveforms

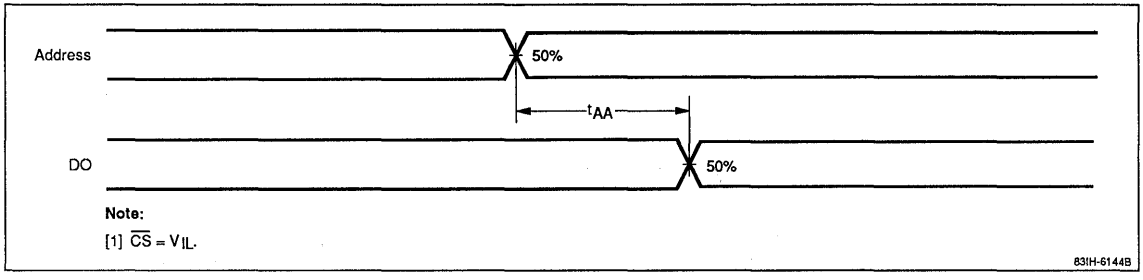
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

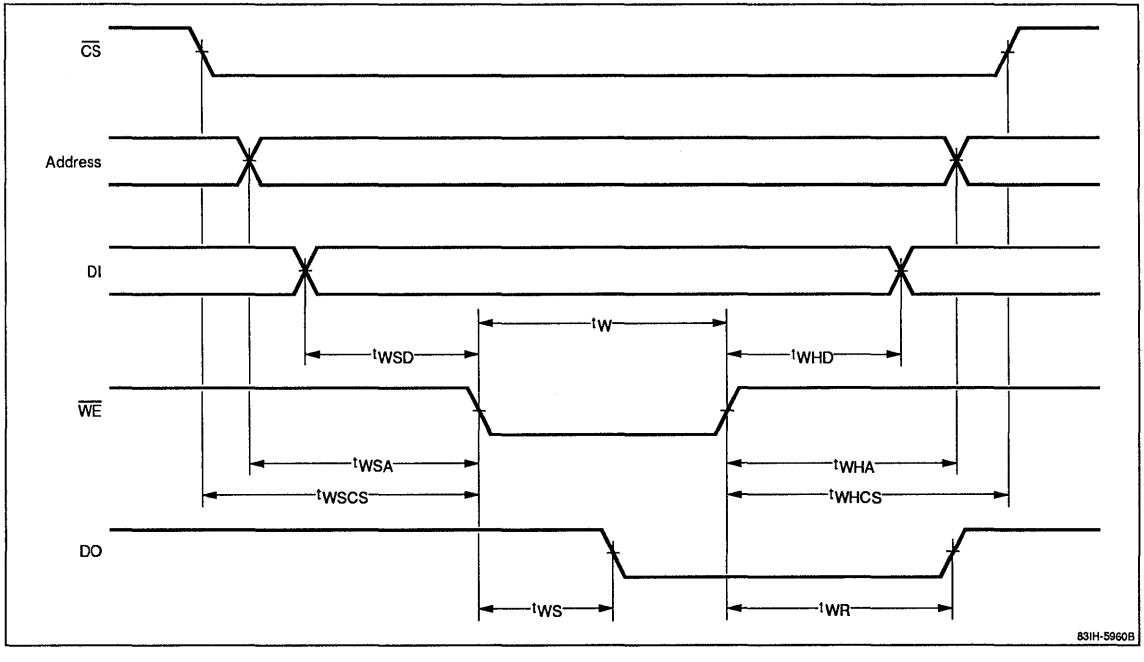
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5960B

μPB10474E
1024 x 4-Bit
10K ECL RAM

Description

The μPB10474E is a very-high-speed 10K interface ECL RAM organized as 1024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption.

Features

- 1024-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption: 1.6 W max
- 24-pin ceramic package, DIP or flatpack

Ordering Information

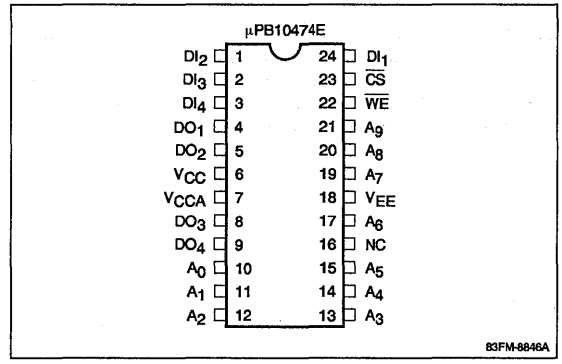
Part Number	Access Time (max)	Package
μPB10474EDH-3	3 ns	24-pin cerdip
DH-4	4 ns	
μPB10474EBH-3	3 ns	24-pin ceramic flatpack
BH-4	4 ns	

Pin Identification

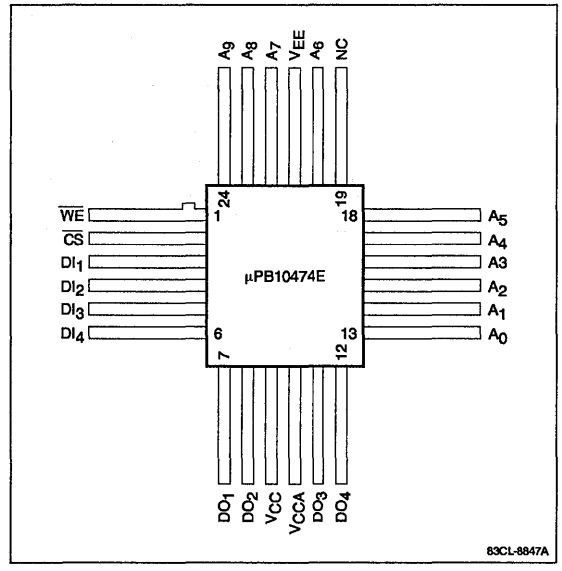
Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable input
$\overline{CS}$	Chip select input
V_{CC}	Power supply ground (current switches and bias driver)
V_{CCA}	Power supply ground (output devices)
V_{EE}	Power supply (–5.2 volts)
NC	No connection

Pin Configurations

24-Pin Cerdip



24-Pin Ceramic Flatpack



Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

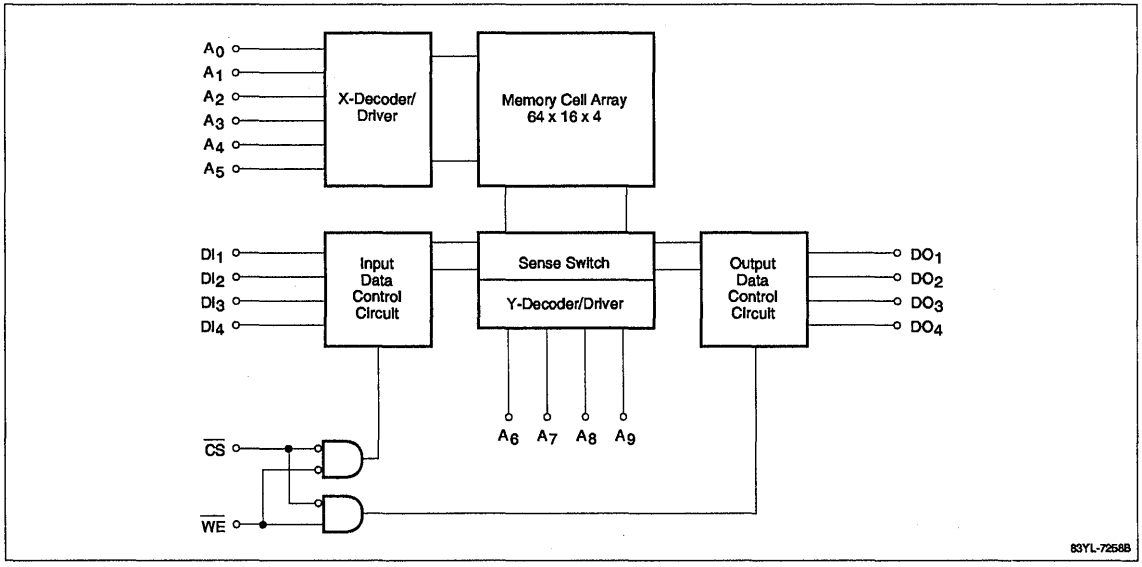
Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 0°C
		−960		−810	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 25°C
		−900		−720	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	$V_{IN} = V_{IH}$ max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 0°C
		−980			mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 25°C
		−920			mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 0°C
				−1630	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 25°C
				−1605	mV	$V_{IN} = V_{IH}$ min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	$V_{IN} = V_{IH}$ max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: $V_{IN} = V_{IL}$ min
		−50			μA	For all others: $V_{IN} = V_{IL}$ min
Supply current	I_{EE}	−330			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V

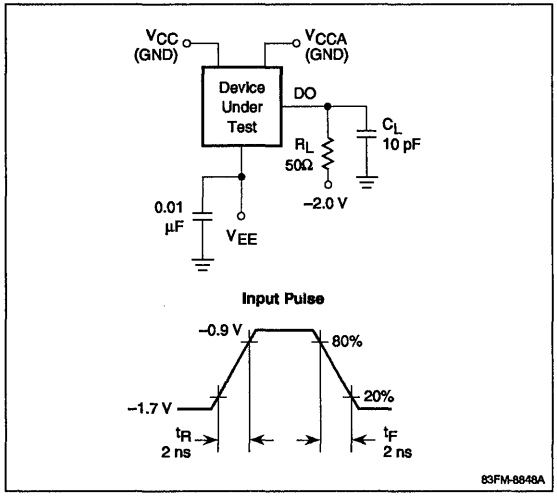
Parameter	Symbol	μPB10474E-3 Min	μPB10474E-3 Typ	μPB10474E-3 Max	μPB10474E-4 Min	μPB10474E-4 Typ	μPB10474E-4 Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			3			4	ns	
Chip select access time	t_{ACS}			2			3	ns	
Chip select recovery time	t_{RCS}			2			3	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Address hold time	t_{WHA}	0.5			0.5			ns	
Chip select hold time	t_{WHCS}	0.5			0.5			ns	
Data hold time	t_{WHD}	0.5			0.5			ns	
Write recovery time	t_{WR}			4			5	ns	
Write disable time	t_{WS}			2			3	ns	
Address setup time	t_{WSA}	0.5			0.5			ns	
Chip select setup time	t_{WSCS}	0.5			0.5			ns	
Data setup time	t_{WSD}	0.5			0.5			ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figure 1 for loading conditions and input pulse shape.

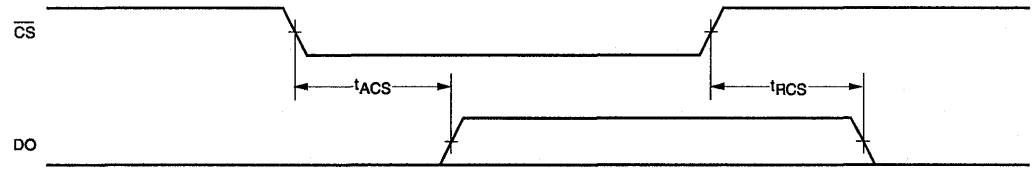
Figure 1. Test Circuit



25e

Timing Waveforms

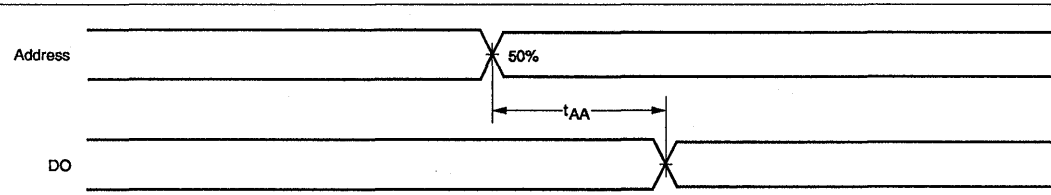
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.
[2] $\overline{WE} = V_{IH}$.

83IH-6164B

Address Access Cycle

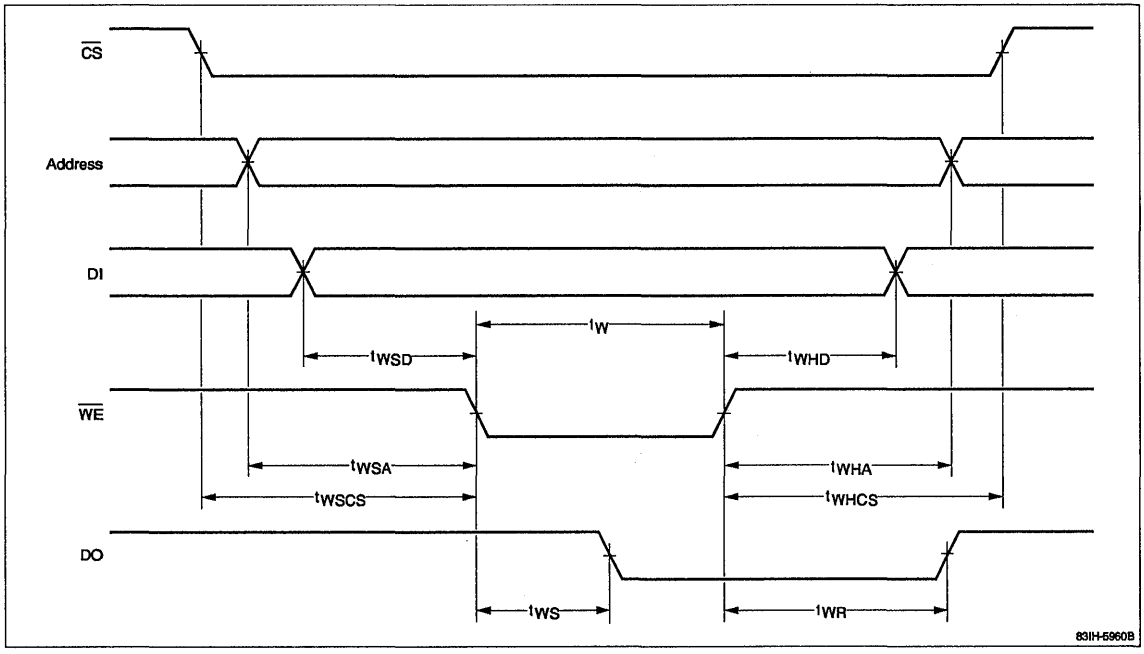


Note:
[1] $\overline{CS} = V_{IL}$.
[2] $\overline{WE} = V_{IH}$.

83IH-6144B

Timing Waveforms (cont)

Write Cycle



NEC Electronics Inc.

μPB10476LL
1024 x 4-Bit
10K ECL Synchronous RAM

Preliminary Information

Description

The μPB10476LL is a very-high-speed 10K interface ECL RAM organized as 1024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption.

The device integrates input latches, high-speed ECL RAM, output latches, and a write pulse generator. The synchronous design allows precise cycle control by use of an internal clock.

Features

- 1024-word x 4-bit organization
- 10K ECL interface
- High-speed clock cycle: 6 ns
- Latched I/O
- Self-timed write
- 28-pin ceramic package, DIP or flatpack

Ordering Information

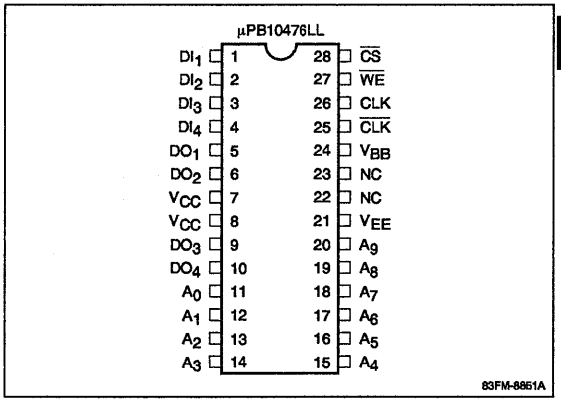
Part Number	Access Time (max)	Package
μPB10476LLDH-6	6 ns	28-pin cerdip
BH-6	6 ns	28-pin ceramic flatpack

Pin Identification

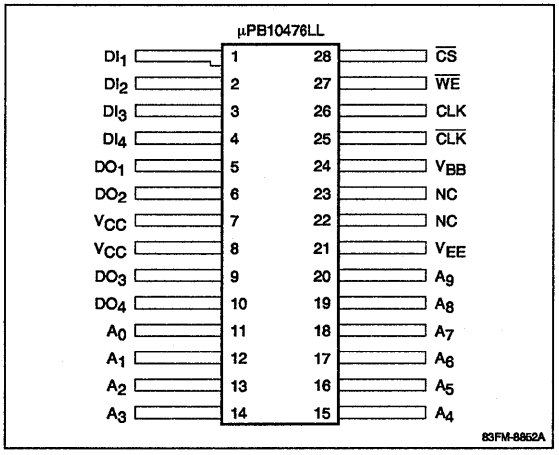
Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
CLK, $\overline{CLK}$	Clock inputs
$\overline{CS}$	Chip select input
$\overline{WE}$	Write enable input
V_{BB}	Reference voltage output
V_{CC}	Power supply ground (current switches and bias driver)
V_{CCA}	Power supply ground (output devices)
V_{EE}	Power supply (–5.2 volts)
NC	No connection

Pin Configuration

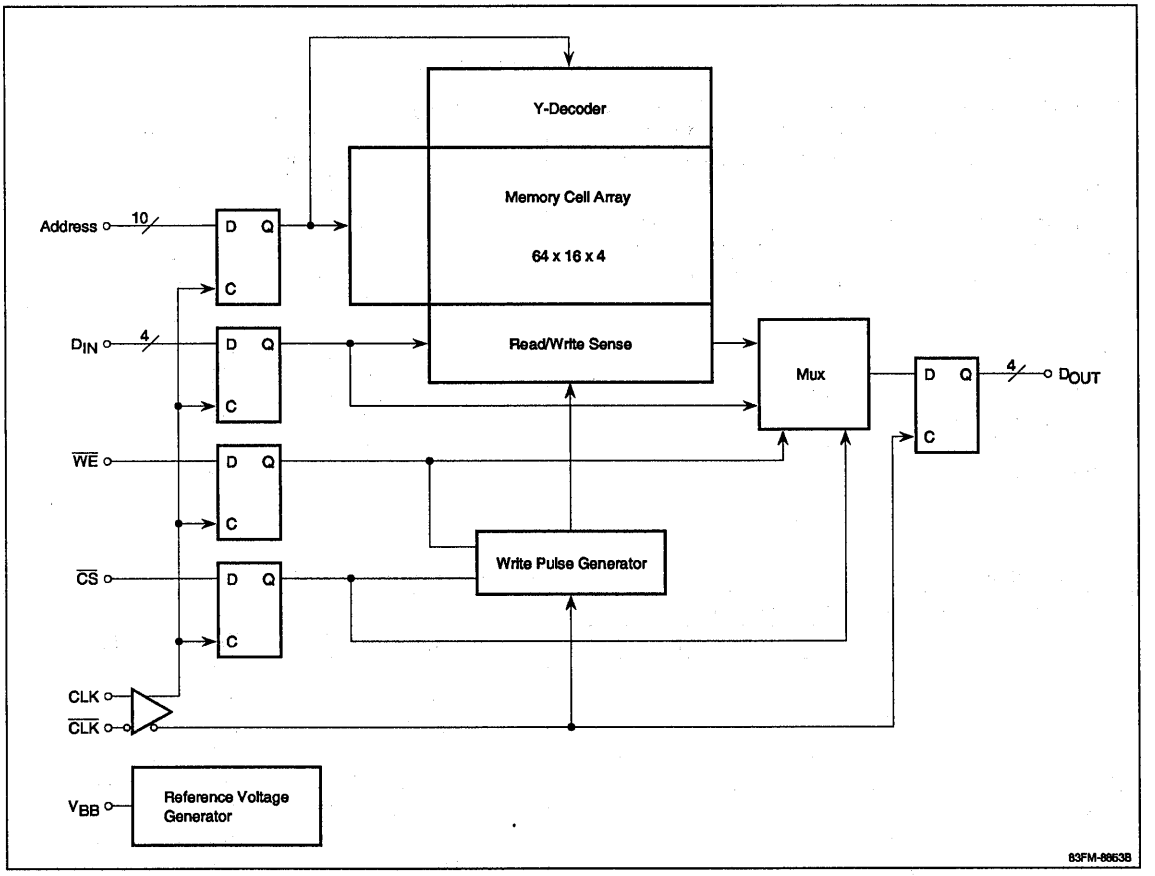
28-Pin Cerdip



28-Pin Ceramic Flatpack



Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	H	Write 1
L	H	X	D_{OUT}	Read

X = don't care.

DC Characteristics

T_A = 0 to +75°C; V_{CC} = V_{CCA} = 0 V; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−350			mA	All inputs and outputs open
Reference voltage	V_{BB}	−1820		−1250	mV	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V

		μPB10476LL-6				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Address access time	$t_{A(Add)}$			2.5	ns	t_{SA} = 0.5 ns
Clock access time	$t_{A(Clk)}$			3.3	ns	$t_{WL(Clk)}$ = 1.5 ns
$\overline{CS}$ access time	$t_{A(CS)}$			2.3	ns	t_{SC} = 0.5 ns
Data access time	$t_{A(DI)}$			2.3	ns	t_{SD} = 0.5 ns
Write access time	$t_{A(W)}$			2.3	ns	t_{SW} = 0.5 ns
Clock cycle time	t_{CYC}	6			ns	
Data release time	t_{DR}	0.3		1.8	ns	$t_{WL(Clk)} > t_{A(Clk)}$ max, $t_{SA} > t_{A(Add)}$ max, $t_{SC} > t_{A(CS)}$ max, $t_{SD} > t_{A(DI)}$ max
Address hold time	t_{HA}	1			ns	
$\overline{CS}$ hold time	t_{HC}	1			ns	
Data hold time	t_{HD}	1			ns	
$\overline{WE}$ hold time	t_{HW}	1			ns	
Address setup time	t_{SA}	0.5			ns	
$\overline{CS}$ setup time	t_{SC}	0.5			ns	
Data setup time	t_{SD}	0.5			ns	
$\overline{WE}$ setup time	t_{SW}	0.5			ns	
Clock high-pulse width	$t_{WH(Clk)}$	4.5			ns	
Clock low-pulse width	$t_{WL(Clk)}$	1.5			ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figure 1 for loading conditions and input pulse shape.

Figure 1. Test Circuit

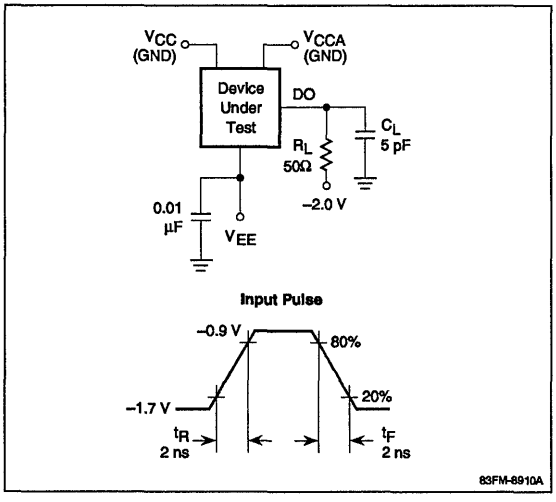
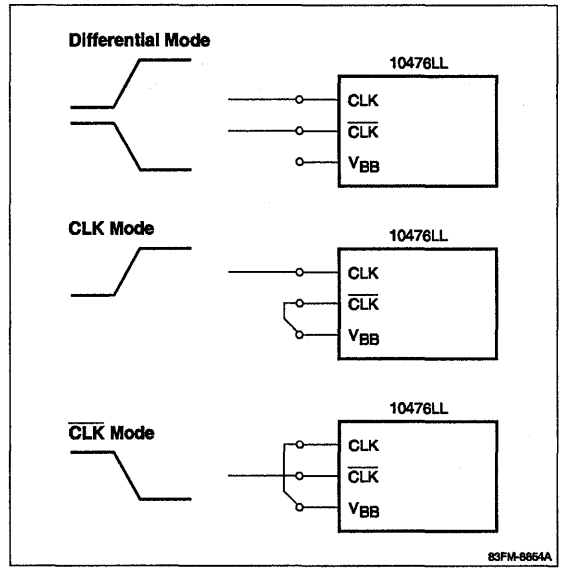


Figure 2. Clock Input Modes



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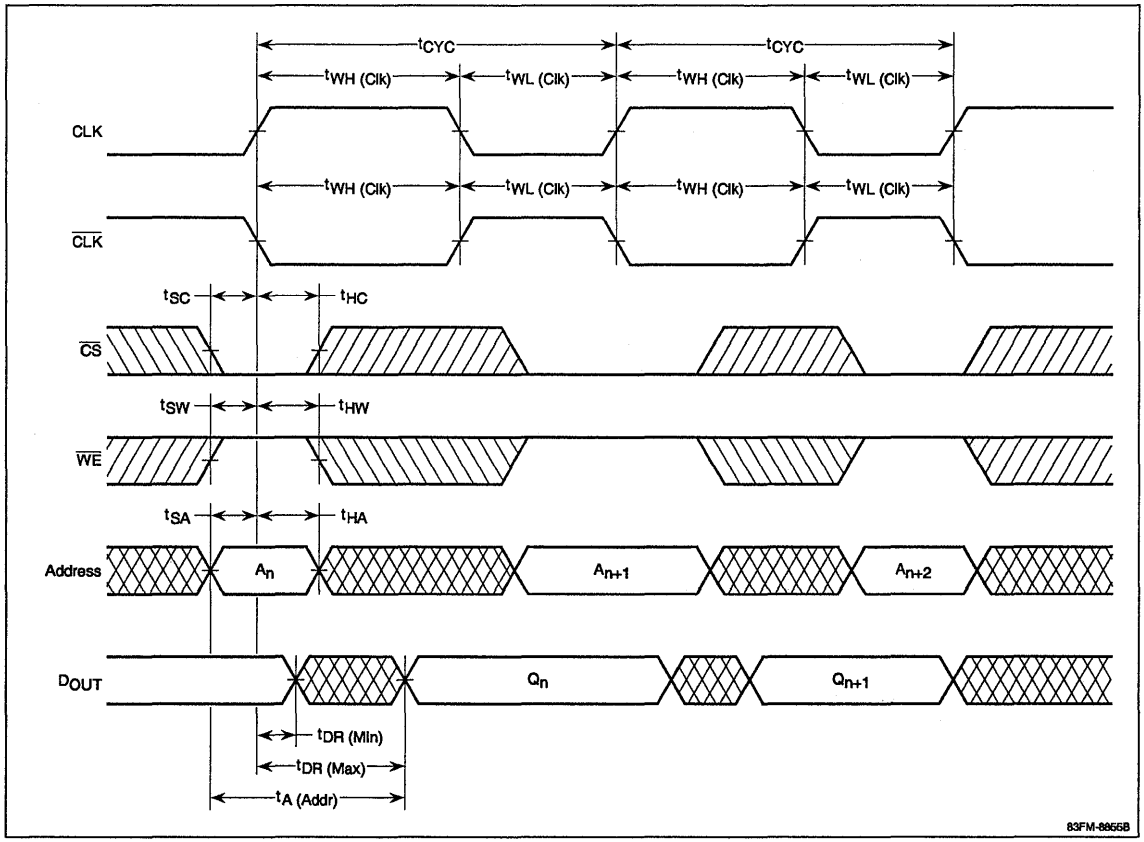
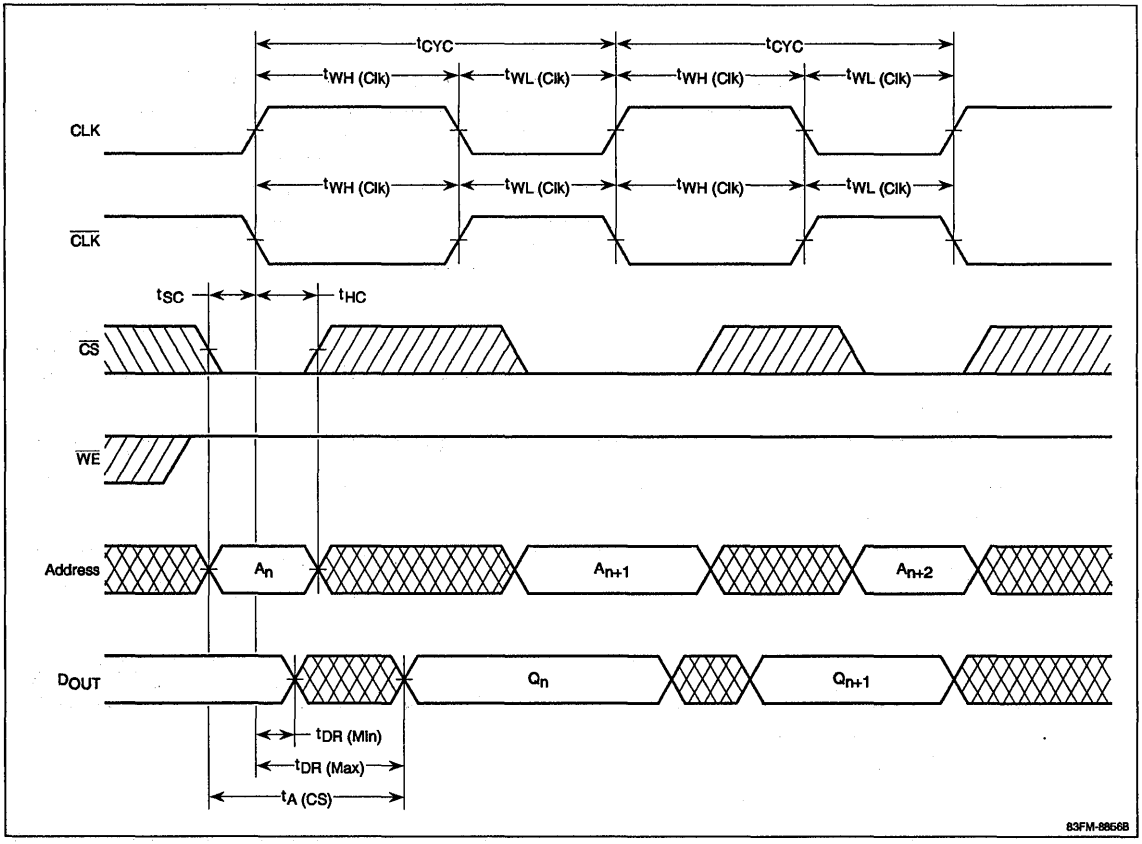
Timing Waveforms

Address Access, Read Mode



Timing Waveforms (cont)

Chip Select Access, Read Mode



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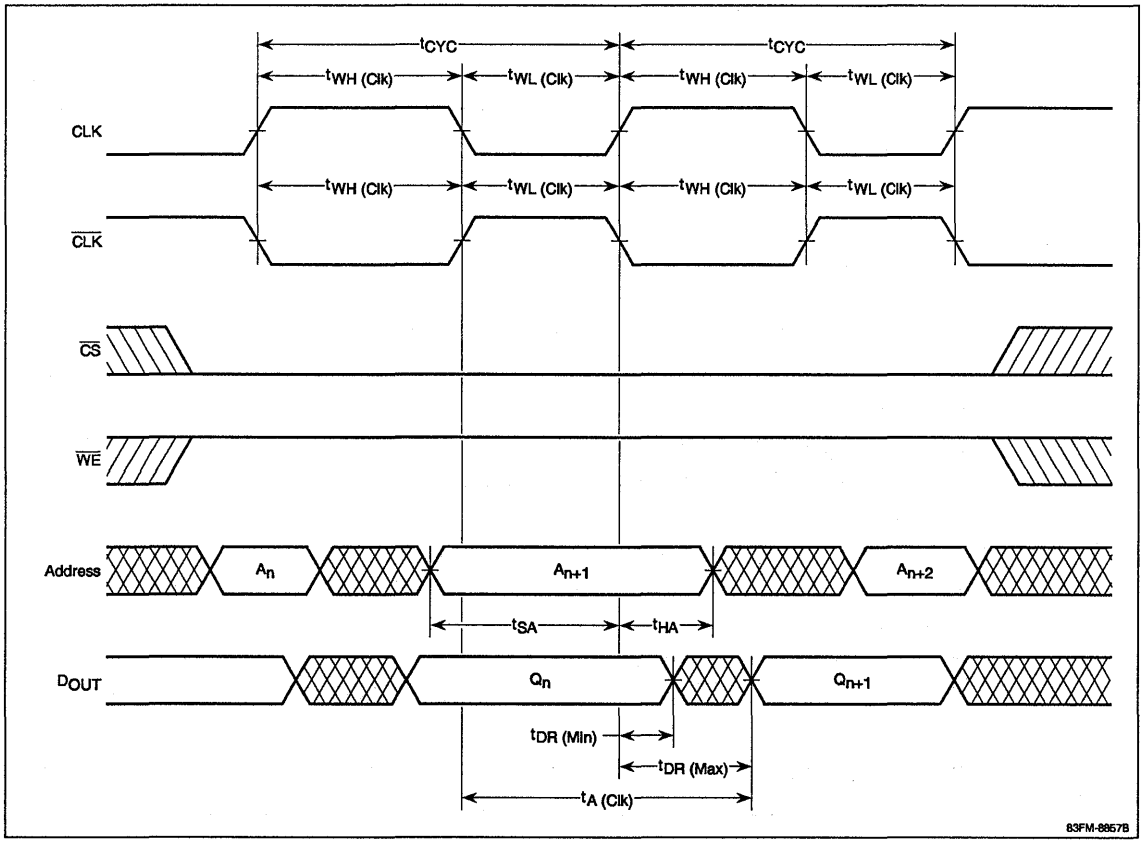
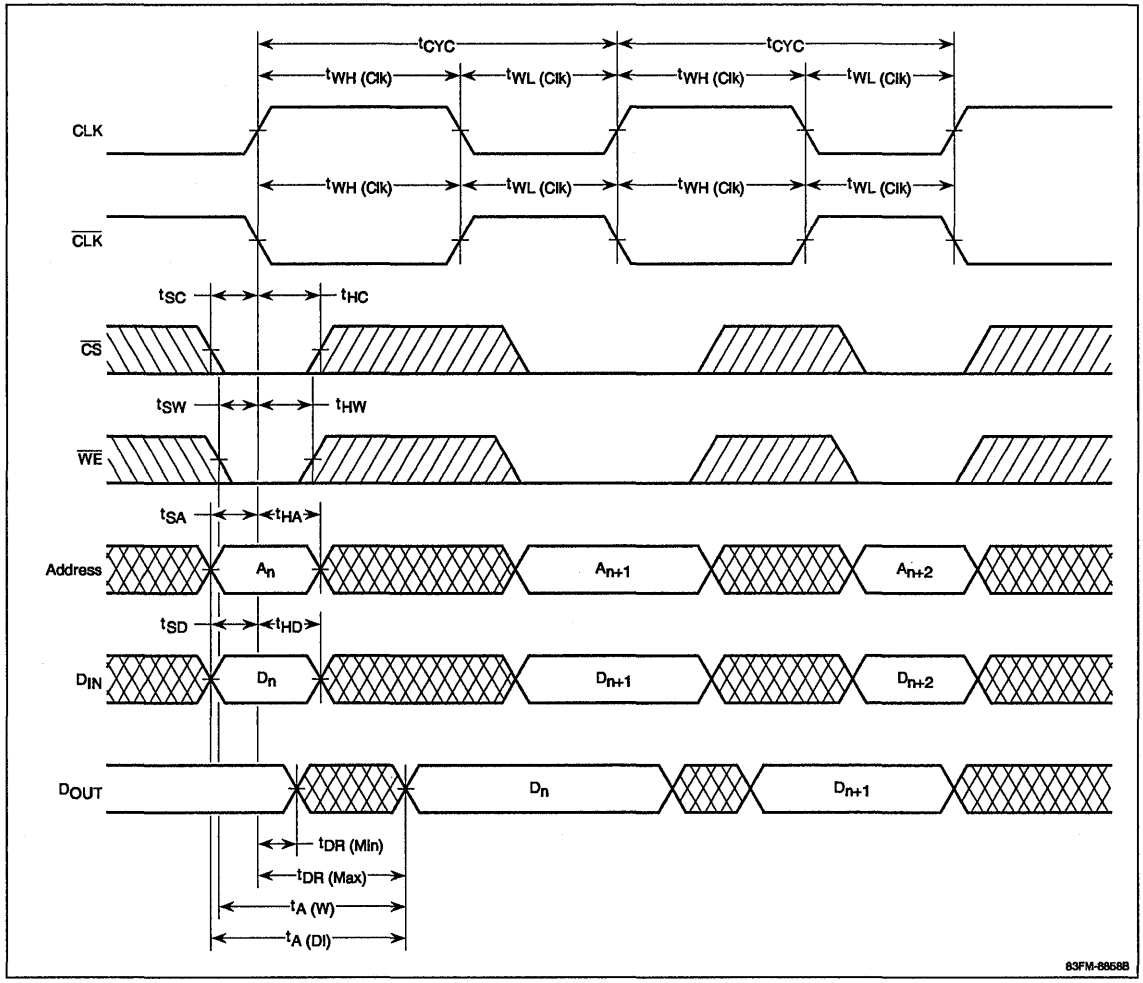
Timing Waveforms (cont)

Clock Access, Read Mode



Timing Waveforms (cont)

Write Mode



μPB10480
16,384 x 1-Bit
10K ECL RAM

Description

The μPB10480 is a very high-speed 10K interface ECL RAM organized as 16,384 words by 1 bit and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 10 ns and 15 ns maximum are available in hermetic, 300-mil, 20-pin cerdip or 20-pin ceramic flatpack packaging.

Features

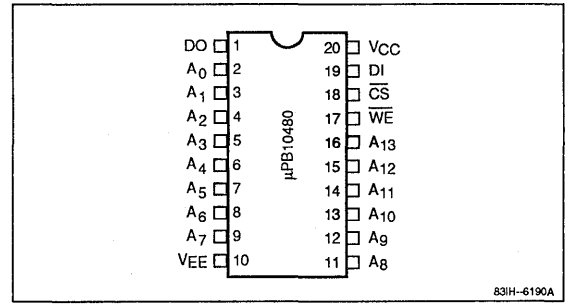
- 16,384-word x 1-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 300-mil, 20-pin cerdip or 20-pin ceramic flatpack packaging

Ordering Information

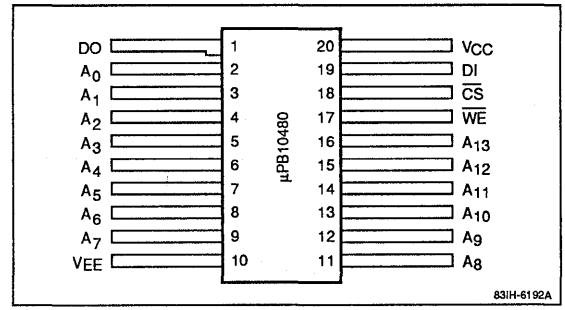
Part Number	Access Time (max)	Power Consumption (max)	Package
μPB10480D-10	10 ns	1.4 W	20-pin cerdip
D-15	15 ns	1.3 W	
μPB10480B-10	10 ns	1.4 W	20-pin ceramic flatpack
B-15	15 ns	1.3 W	

Pin Configurations

20-Pin Cerdip



20-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_{13}	Address inputs
DI	Data input
DO	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	–5.2-volt power supply

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

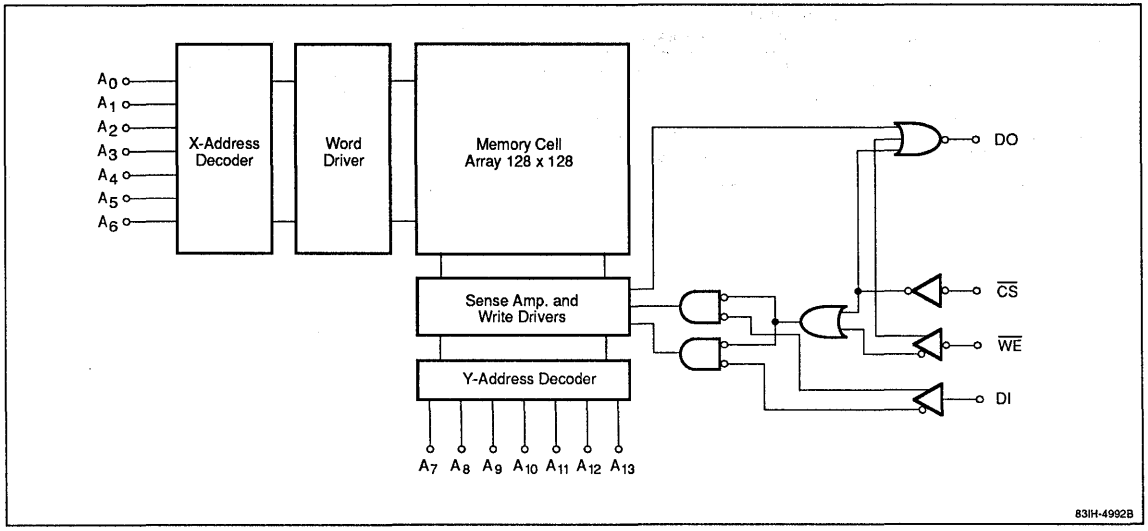
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB10480-10: all inputs and outputs open
		−240			mA	For μPB10480-15: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ±5%

Parameter	Symbol	μPB10480-10			μPB10480-15			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select recovery time	t_{RCS}			5			8	ns	
Chip select access time	t_{ACS}			5			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	2			3			ns	
Address hold time	t_{WHA}	1			2			ns	
Chip select setup time	t_{WSCS}	2			3			ns	
Chip select hold time	t_{WHCS}	1			2			ns	
Write disable time	t_{WS}			5			8	ns	
Write recovery time	t_{WR}			11			17	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% to 20%) = 2.5 ns; input and output timing reference level = 50%.

25g

Figure 1. Loading Conditions Test Circuit

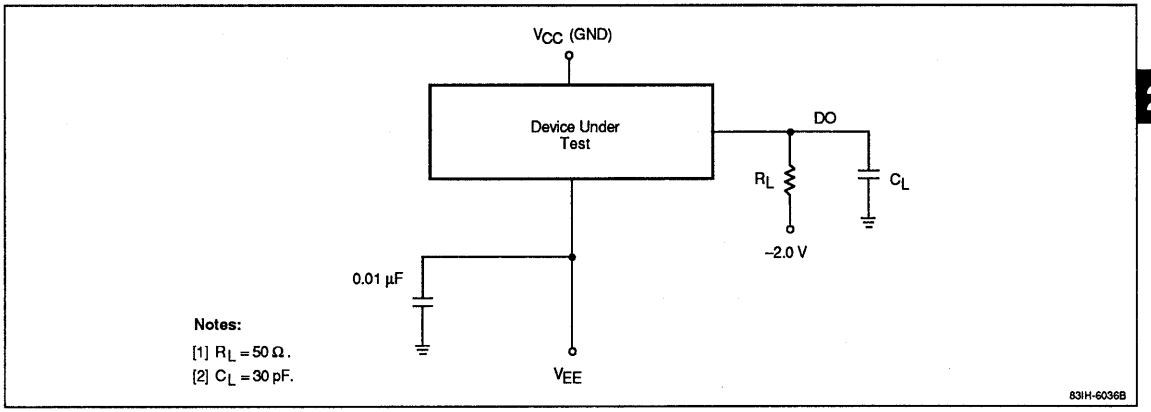
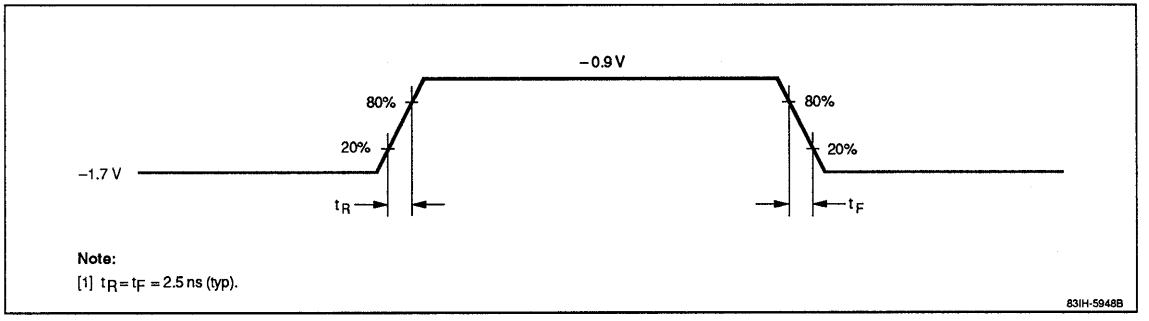
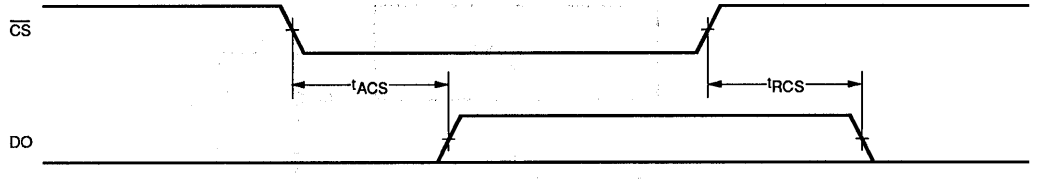


Figure 2. Input Pulse



Timing Waveforms

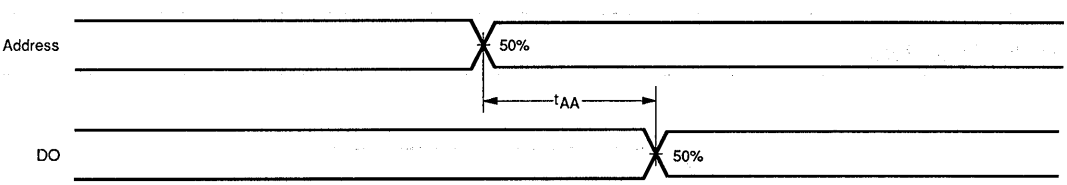
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

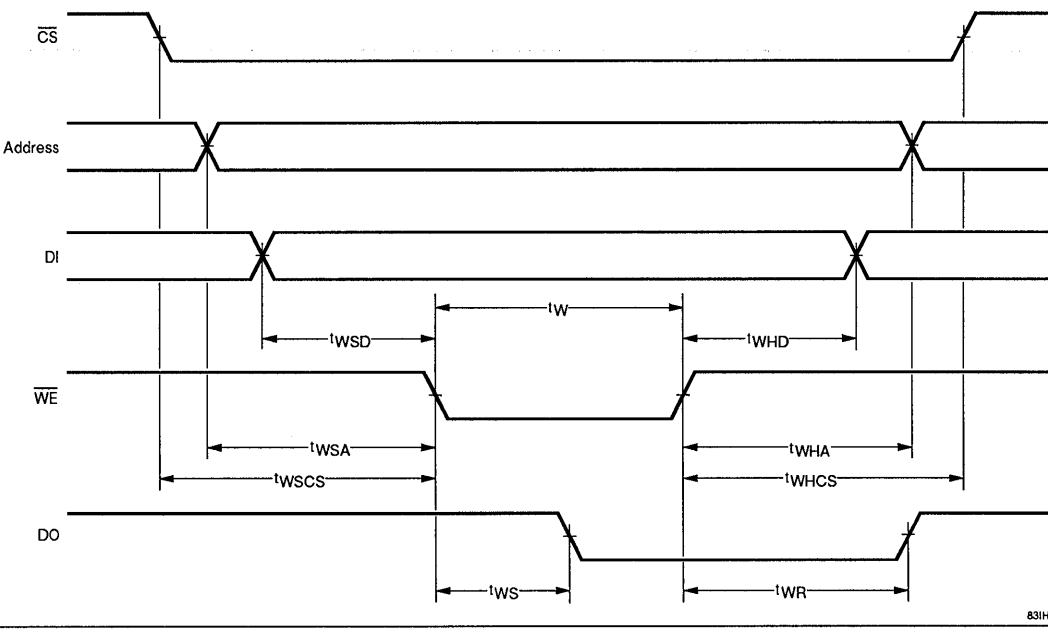
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5950B

NEC Electronics Inc.

μPB10484
4,096 x 4-Bit
10K ECL RAM

25h

Description

The μPB10484 is a very high-speed 10K interface ECL RAM organized as 4,096 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with access times of 10 and 15 ns maximum are available. The μPB10484 is packaged in a hermetic, 400-mil, 28-pin cerdip or 28-pin ceramic flatpack.

Features

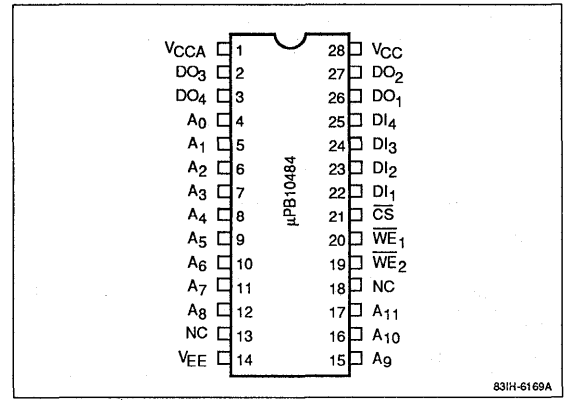
- 4,096-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Low power consumption of 1.4 W maximum
- Fast access times of 10 and 15 ns maximum
- 400-mil, 28-pin cerdip or 28-pin ceramic flatpack packaging

Ordering Information

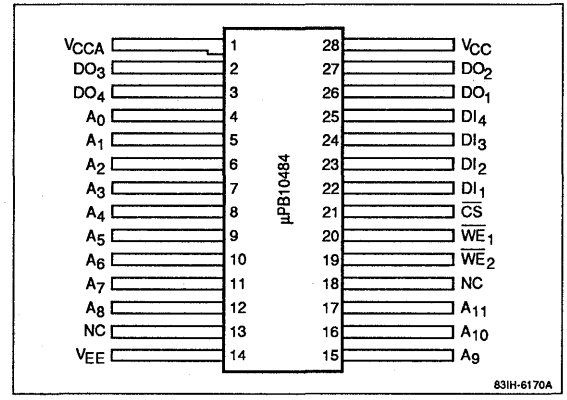
Part Number	Access Time (max)	Package
μPB10484D-10	10 ns	28-pin cerdip
D-15	15 ns	
μPB10484B-10	10 ns	28-pin ceramic flatpack
B-15	15 ns	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–5.2-volt power supply
NC	No connection

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

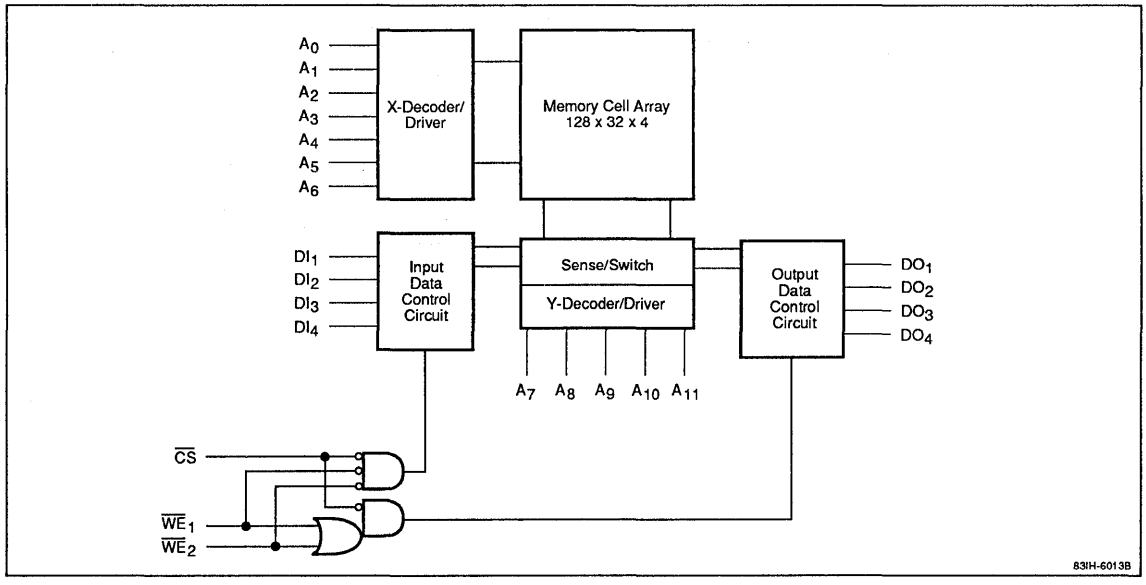
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE}_1$ and $\overline{WE}_2$ must be low to initiate write operation. For read operation, either $\overline{WE}_1$ or $\overline{WE}_2$ or both must be high.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB10484-10: all inputs and outputs open
		−240			mA	For μPB10484-15: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

25h

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB10484-10			μPB10484-15				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select recovery time	t_{RCS}			5			8	ns	
Chip select access time	t_{ACS}			5			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	2			3			ns	
Address hold time	t_{WHA}	1			2			ns	
Chip select setup time	t_{WSCS}	2			3			ns	
Chip select hold time	t_{WHCS}	1			2			ns	
Write disable time	t_{WS}			5			8	ns	
Write recovery time	t_{WR}			11			17	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% to 20%) = 2.5 ns; input and output timing reference level = 50%.

Figure 1. Loading Conditions Test Circuit

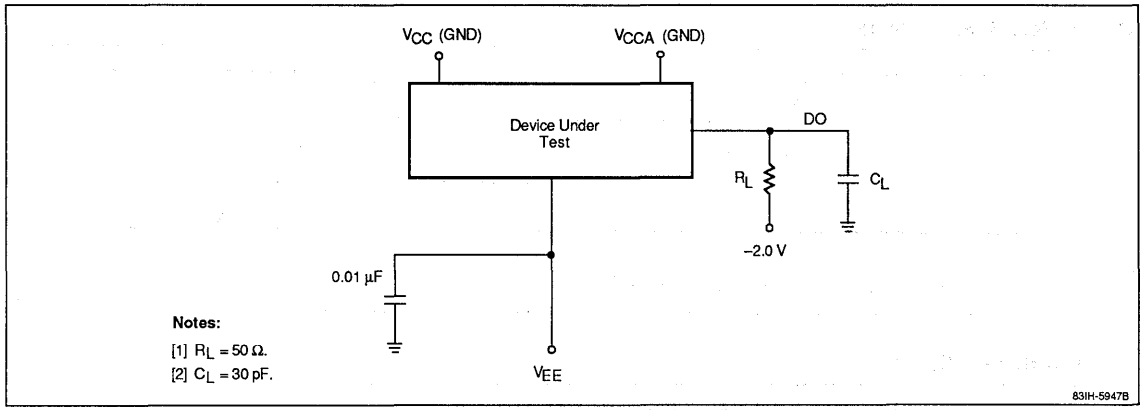
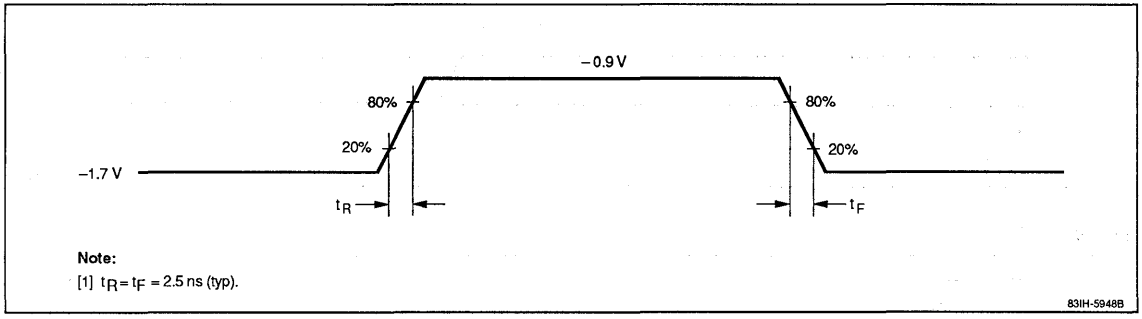
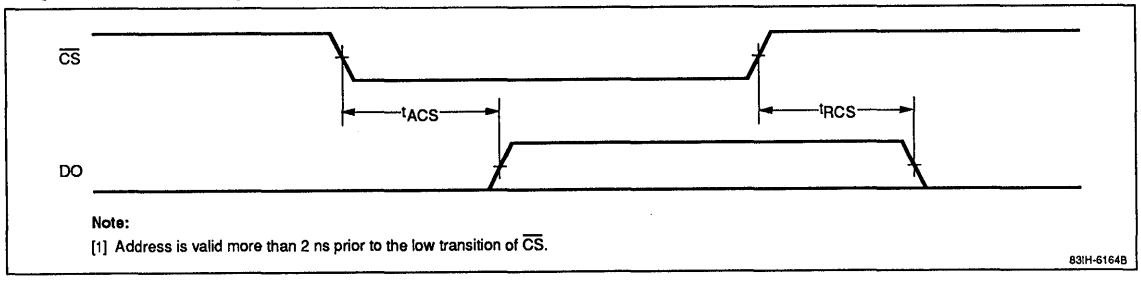


Figure 2. Input Pulse



Timing Waveforms

Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

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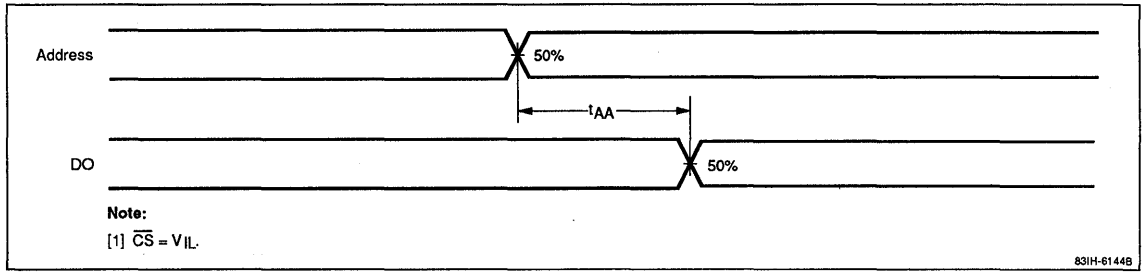
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

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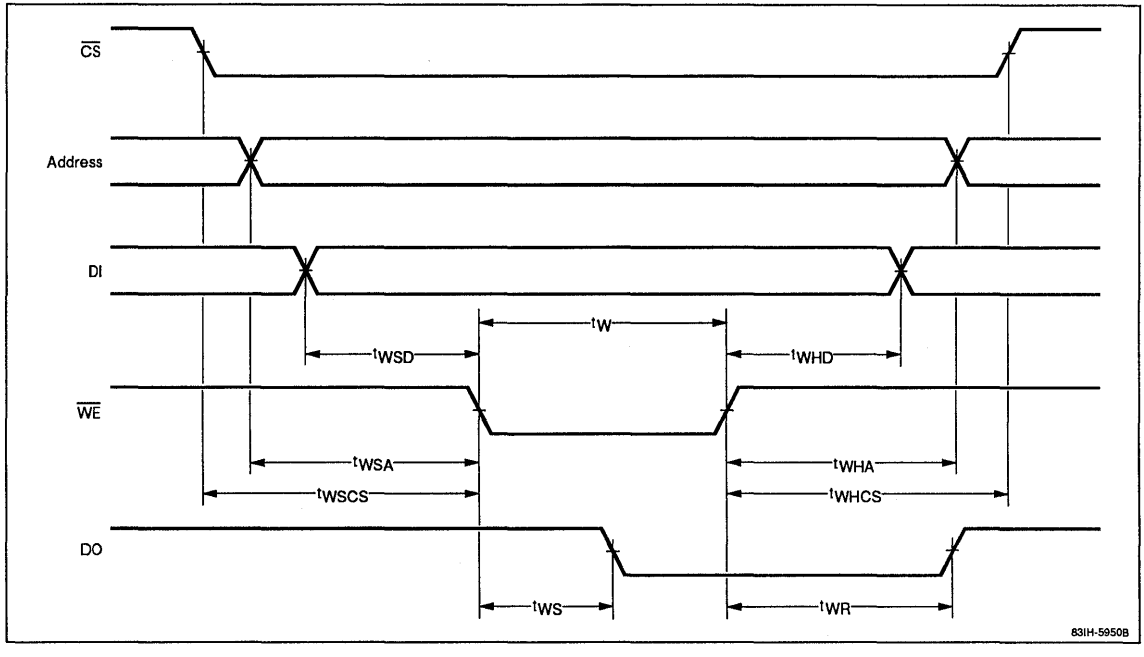
Write Cycle



83IH-5950B

Description

The μPB10484A is a very high-speed 10K interface ECL RAM. It is organized as 4,096 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with access times of 5 or 7 ns maximum are available. The μPB10484A is packaged in a hermetic, 400-mil, 28-pin cerdip or 28-pin ceramic flatpack.

Features

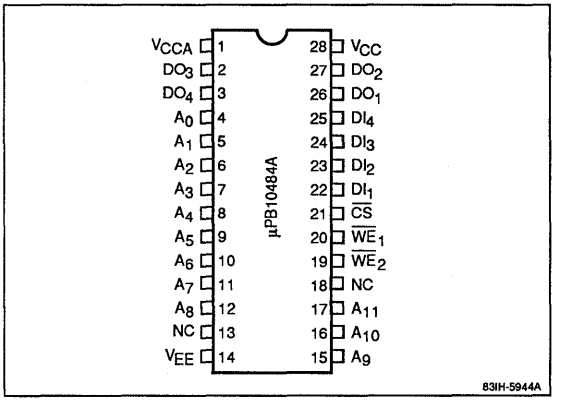
- 4,096-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times of 5 and 7 ns maximum
- Low power consumption of 1.4 W maximum
- 400-mil, 28-pin cerdip or ceramic flatpack packaging

Ordering Information

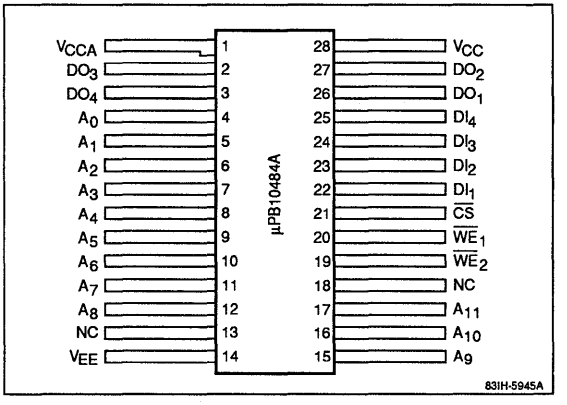
Part Number	Access Time (max)	Package
μPB10484AD-5	5 ns	28-pin cerdip
D-7	7 ns	
μPB10484AB-5	5 ns	28-pin ceramic flatpack
B-7	7 ns	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–5.2-volt power supply
NC	No connection

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150 °C
Storage temperature under bias, T_{STG} (bias)	–55 to +125 °C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

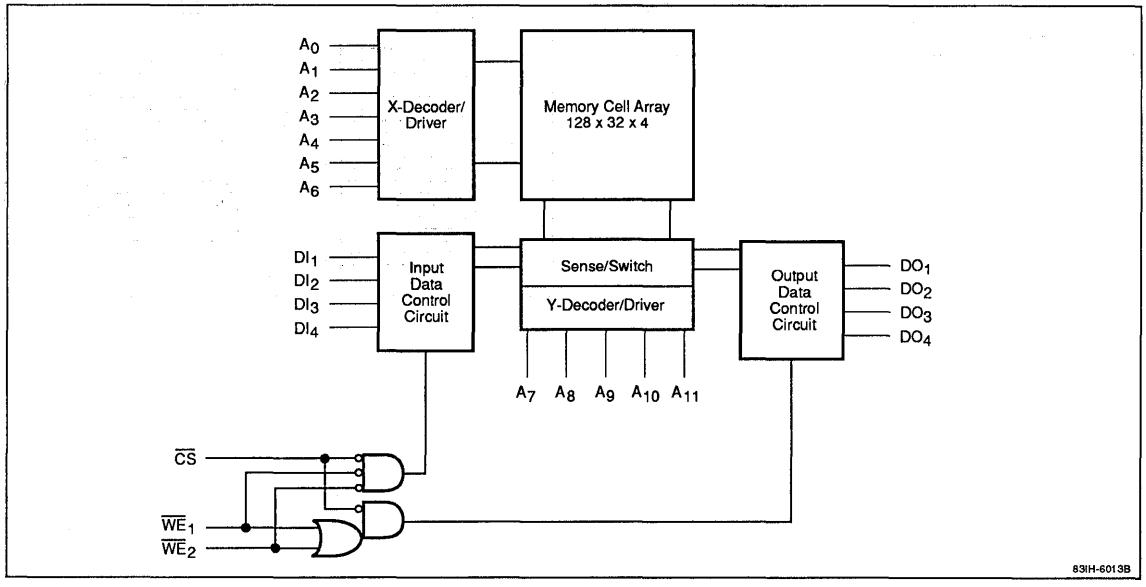
$\overline{CS}$	$\overline{WE}$	DI	Output	Function
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE}_1$ and $\overline{WE}_2$ must be low to initiate write operation. For read operation, either $\overline{WE}_1$ or $\overline{WE}_2$ or both must be high.

Block Diagram



DC Characteristics

T_A = 0 to +75 °C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0 °C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25 °C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75 °C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0 °C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25 °C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75 °C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0 °C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25 °C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75 °C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0 °C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25 °C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75 °C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0 °C
		−1105		−810	mV	For all inputs: T_A = 25 °C
		−1045		−720	mV	For all inputs: T_A = 75 °C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0 °C
		−1850		−1475	mV	For all inputs: T_A = 25 °C
		−1830		−1450	mV	For all inputs: T_A = 75 °C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB10484A-5: all inputs and outputs open
		−240			mA	For μPB10484A-7: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75 °C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB10484A-5			μPB10484A-7				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			5			7	ns	
Chip select recovery time	t_{RCS}			3.5			4	ns	
Chip select access time	t_{ACS}			3.5			4	ns	
Write Operation									
Write pulse width	t_W	6			8			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			3.5			5	ns	
Write recovery time	t_{WR}			7			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.5 ns; input and output timing reference level = 50%.

Figure 1. Loading Conditions Test Circuit

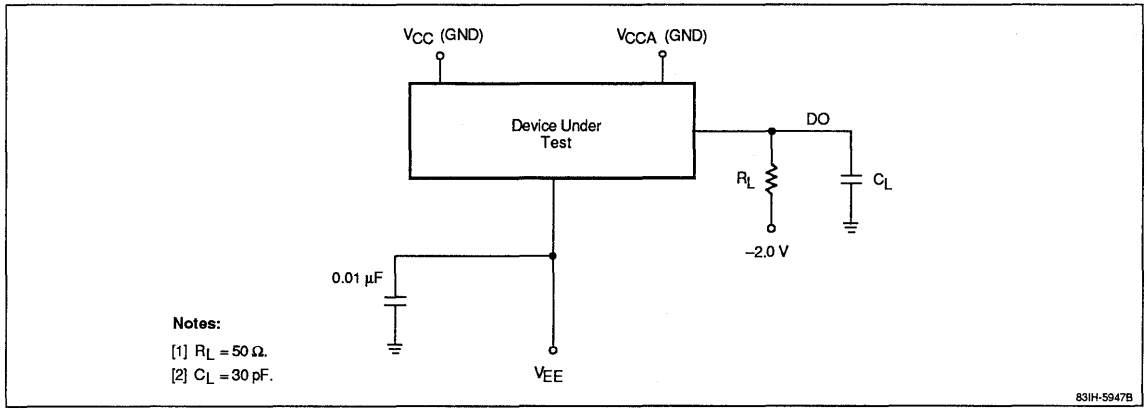
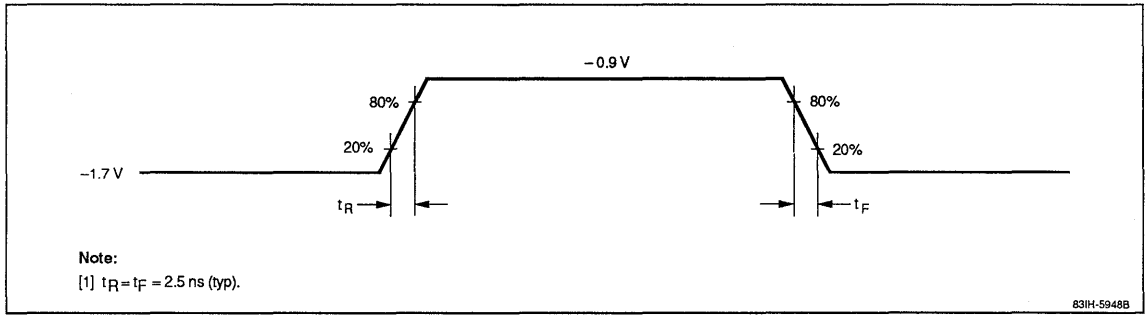
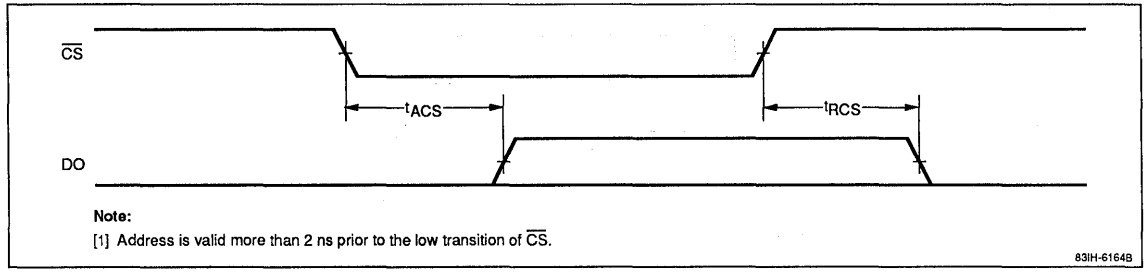


Figure 2. Input Pulse



Timing Waveforms

Chip Select Access Cycle



Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

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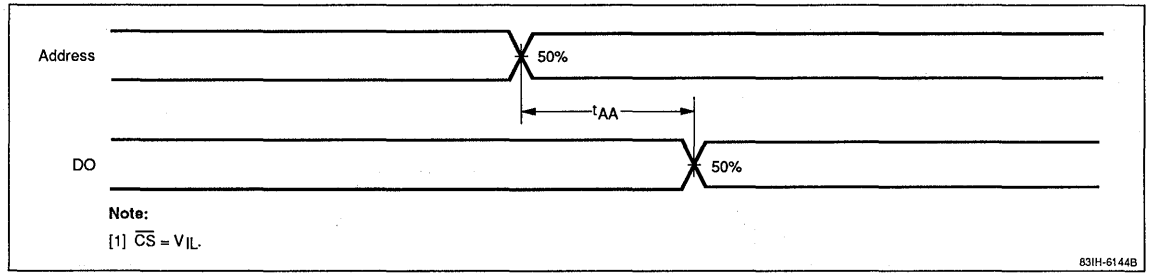
Address Access Cycle



Note:

[1] $\overline{CS} = V_{IL}$.

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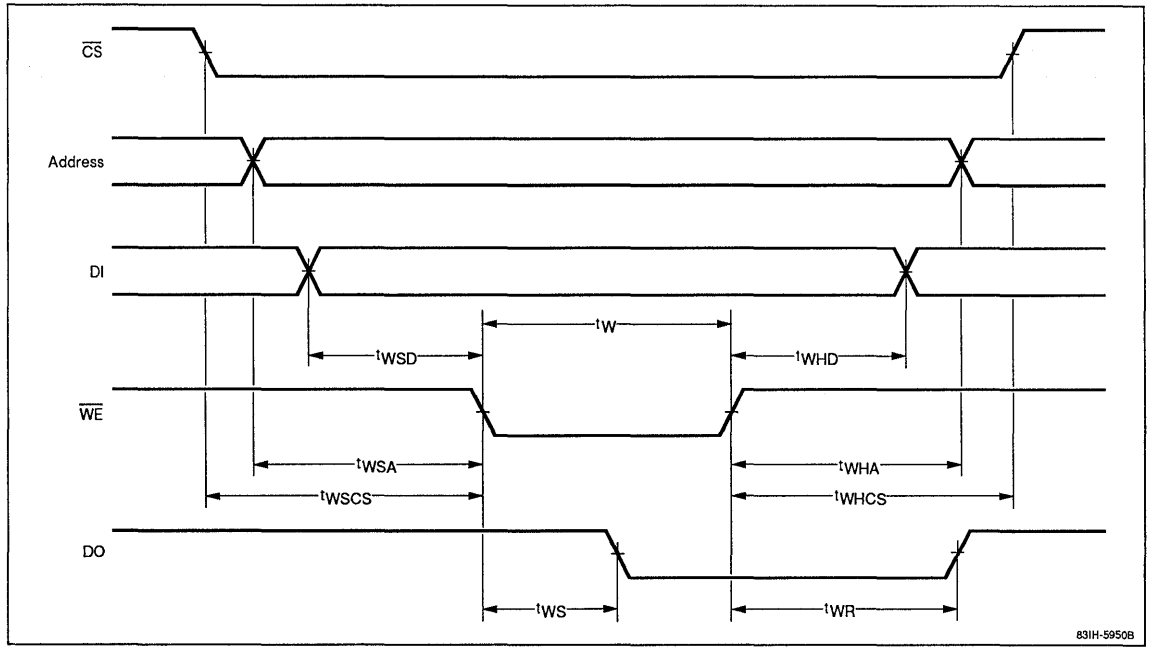
Write Cycle



83IH-5950B

μPB10A484
4,096 x 4-Bit
10K ECL RAM

Description

The μPB10A484 is a very high-speed 10K interface ECL RAM organized as 4,096 words by 4 bits with noninverted, open-emitter outputs. Two versions with access times of 5 ns and 7 ns maximum are available. The μPB10A484 is packaged in a hermetic, 400-mil, 28-pin cerdip or 28-pin ceramic flatpack.

Features

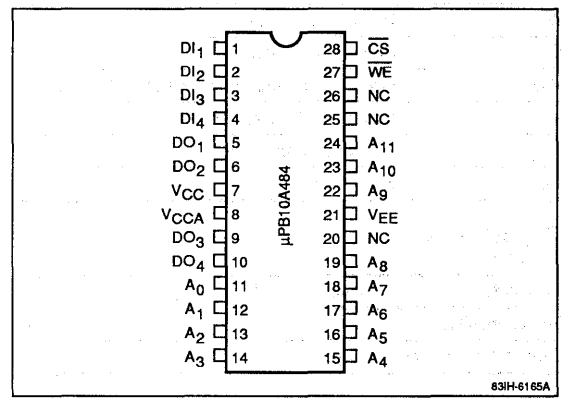
- 4,096-word x 4-bit organization
- 10K ECL interface
- Noninverted, open-emitter outputs
- Fast access times of 5 and 7 ns maximum
- 400-mil, 28-pin cerdip or ceramic flatpack packaging
- Center power pins

Ordering Information

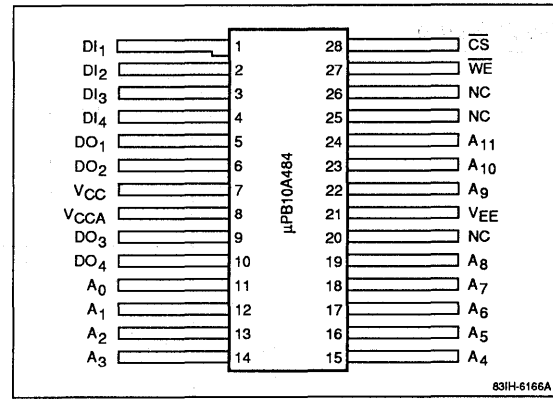
Part Number	Access Time (max)	Package
μPB10A484D-5	5 ns	28-pin cerdip
D-7	7 ns	
μPB10A484BH-5	5 ns	28-pin ceramic flatpack
BH-7	7 ns	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	-5.2-volt power supply
NC	No connection

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	-7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	-30 to +0.1 mA
Storage temperature, T_{STG}	-65 to +150°C
Storage temperature under bias, T_{STG} (bias)	-55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

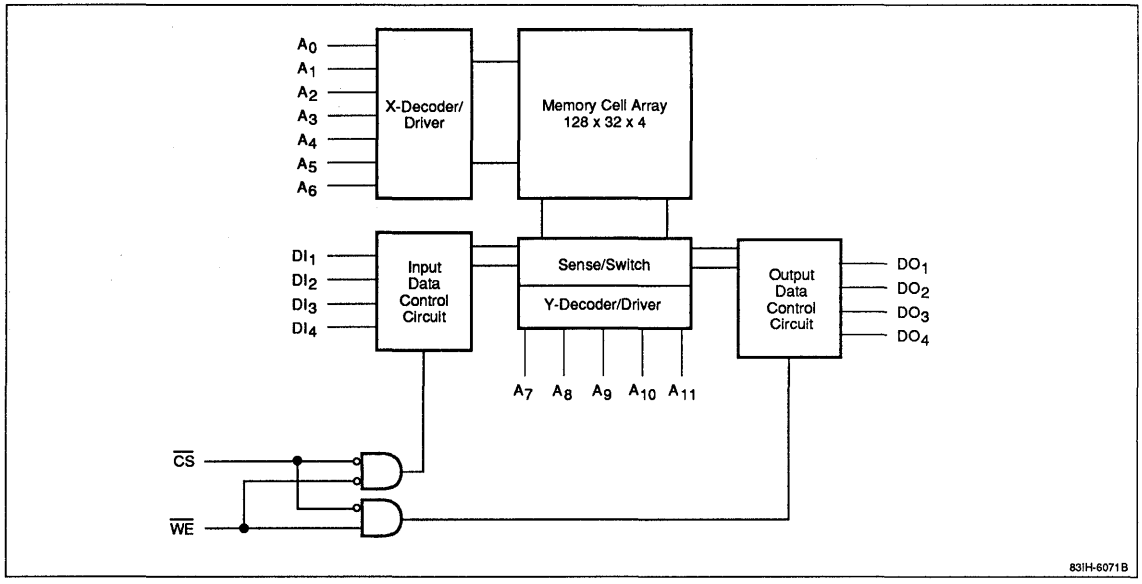
Truth Table

Function	$\overline{CS}$	$\overline{WE}$	D_{IN}	Output
Not selected	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	320			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ± 5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB10A484-5			μPB10A484-7				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			5			7	ns	
Chip select recovery time	t_{RCS}			3.5			4	ns	
Chip select access time	t_{ACS}			3.5			4	ns	
Write Operation									
Write pulse width	t_W	6			8			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			3.5			5	ns	
Write recovery time	t_{WR}			7			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

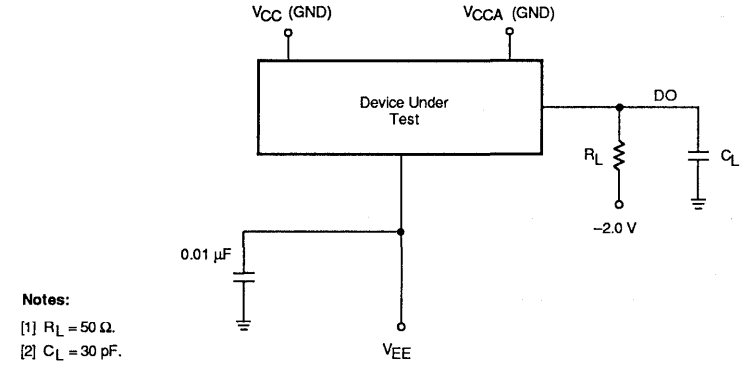
Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.5 ns; input and output timing reference level = 50%.

25j

Figure 1. Loading Conditions Test Circuit



Notes:

[1] $R_L = 50\ \Omega$.

[2] $C_L = 30$ pF.

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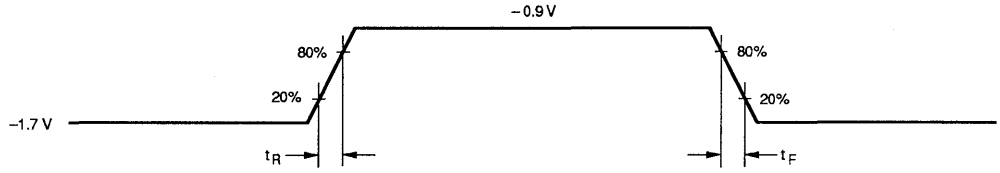
Figure 2. Input Pulse



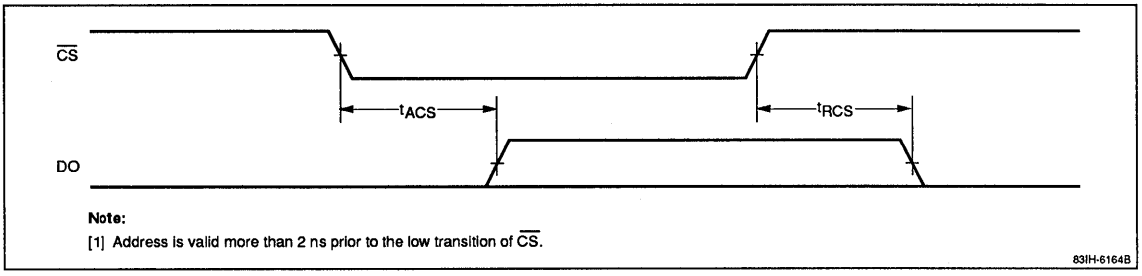
Note:

[1] $t_R = t_F = 2.5$ ns (typ).

83IH-5948B

Timing Waveforms

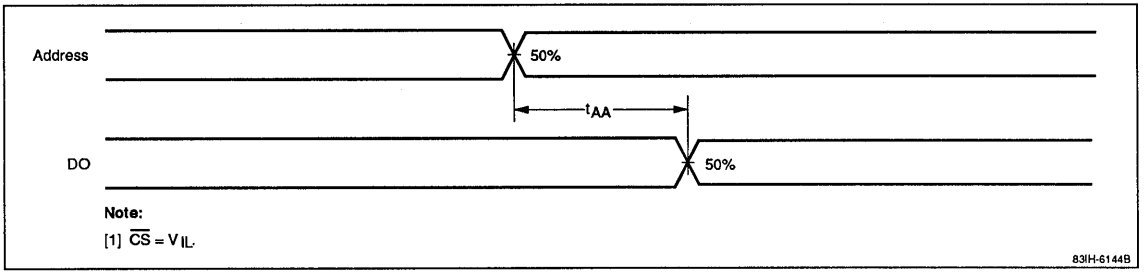
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

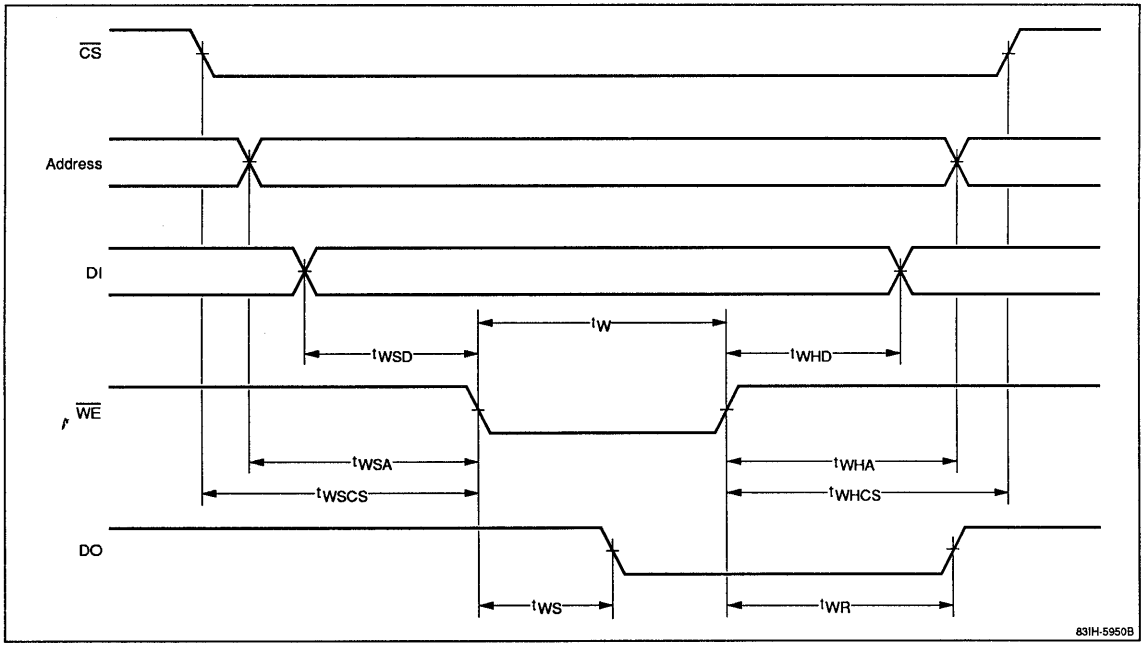
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5950B

μPD10500
262,144 x 1-Bit
10K BiCMOS ECL RAM

Description

The μPD10500 is a very high-speed BiCMOS RAM with a 10K ECL interface. Its unique design uses blended CMOS and bipolar peripheral circuits and N-channel MOS memory cells. The device is organized as 262,144 words by 1 bit and is designed with an open-emitter output (noninverted) and low power consumption. Two versions with fast access times of 15 and 20 ns maximum are available in hermetic, 300-mil, 24-pin cerdip packaging.

Features

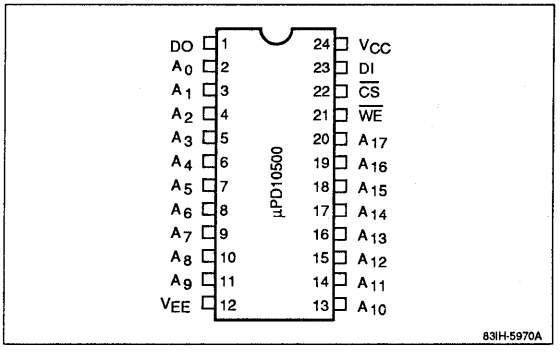
- BiCMOS technology
- 262,144-word x 1-bit organization
- 10K ECL interface
- Open-emitter output (noninverted)
- Fast access times
- Low power consumption
- 300-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Power Consumption (max)	Package
μPD10500D-15	15 ns	832 mW	24-pin cerdip
D-20	20ns		

Pin Configuration

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
DI	Data input
DO	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}, V_{CCA}	Ground
V_{EE}	–5.2-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

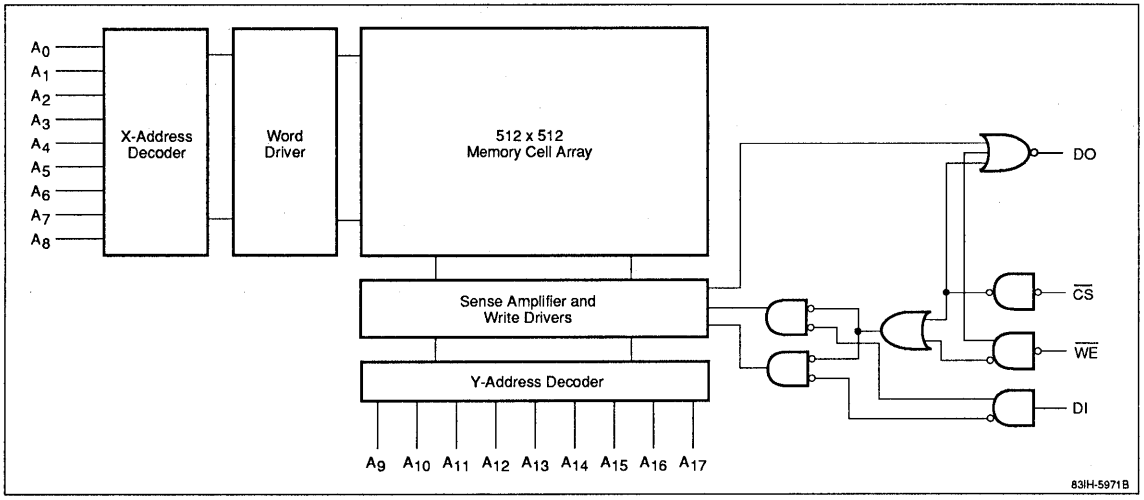
Truth Table

$\overline{CS}$	$\overline{WE}$	DI	Function	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +75°C; V_{EE} = −5.2 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1000		−840	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−960		−810	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−900		−720	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output voltage, low	V_{OL}	−1870		−1665	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 0°C
		−1850		−1650	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 25°C
		−1830		−1625	mV	V_{IN} = V_{IH} max or V_{IL} min; T_A = 75°C
Output threshold voltage, high	V_{OHC}	−1020			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
		−980			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
		−920			mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Output threshold voltage, low	V_{OLC}			−1645	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 0°C
				−1630	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 25°C
				−1605	mV	V_{IN} = V_{IH} min or V_{IL} max; T_A = 75°C
Input voltage, high	V_{IH}	−1145		−840	mV	For all inputs: T_A = 0°C
		−1105		−810	mV	For all inputs: T_A = 25°C
		−1045		−720	mV	For all inputs: T_A = 75°C
Input voltage, low	V_{IL}	−1870		−1490	mV	For all inputs: T_A = 0°C
		−1850		−1475	mV	For all inputs: T_A = 25°C
		−1830		−1450	mV	For all inputs: T_A = 75°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−160			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +75 °C; V_{EE} = −5.2 V ± 5%

Parameter	Symbol	μPD10500-15			μPD10500-20			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Read Operation									
Address access time	t_{AA}			15			20	ns	
Chip select access time	t_{ACS}			10			15	ns	
Chip select recovery time	t_{RCS}			10			15	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	3			3			ns	
Address setup time	t_{WSA}	2			2			ns	
Address hold time	t_{WHA}	3			3			ns	
Chip select setup time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	3			3			ns	
Write disable time	t_{WS}			10			15	ns	
Write recovery time	t_{WR}			18			23	ns	
Output Rise and Fall Times									
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.5 ns; input and output timing reference levels = 50%.

25k

Figure 1. Loading Conditions Test Circuit

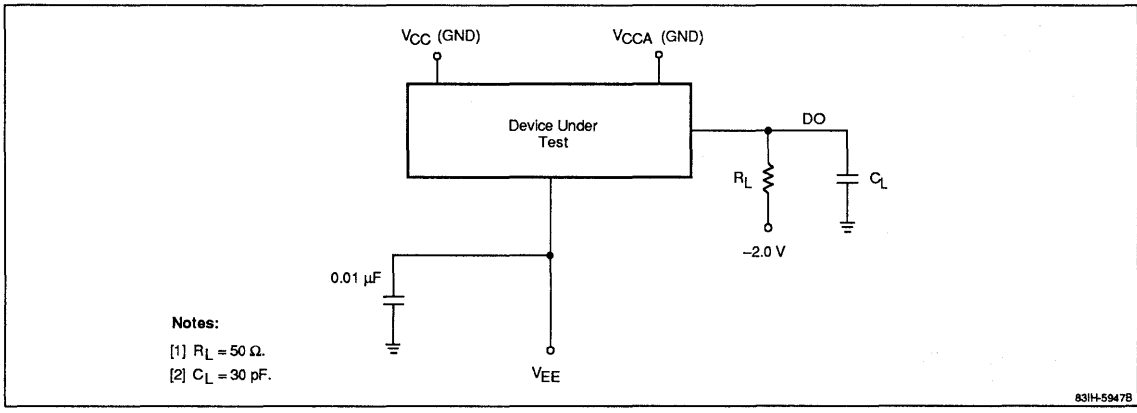
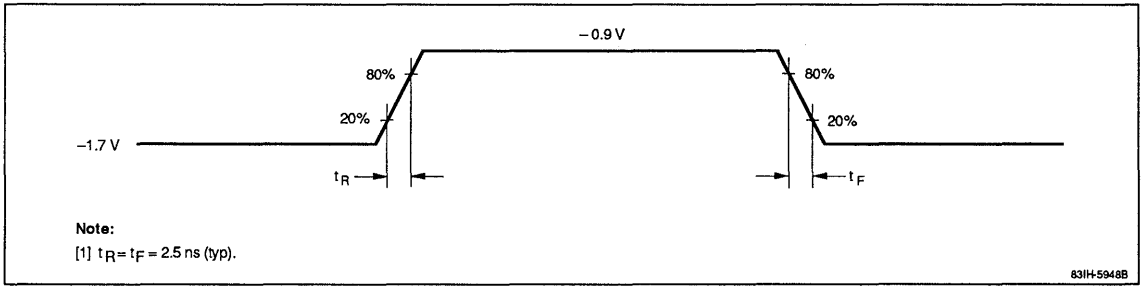
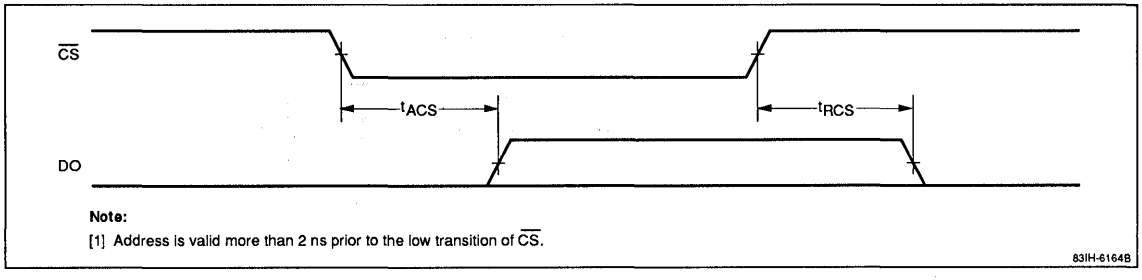


Figure 2. Input Pulse



Timing Waveforms

Chip Select Access Cycle

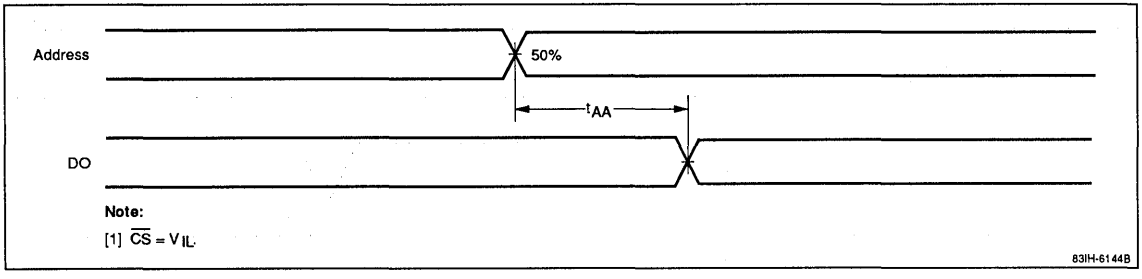


Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

Address Access Cycle

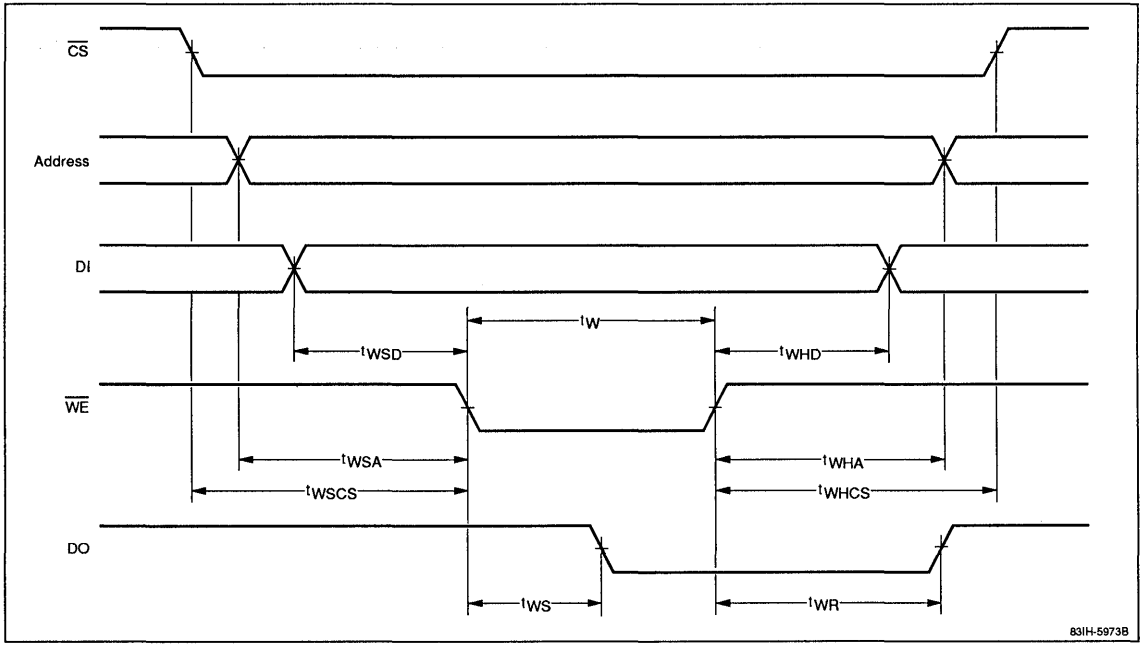


Note:

[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5973B

NEC

Section 26
ECL RAMs (100K Interface)

μPB	Organization	Features	
100422	256 x 4	7-ns	26a
100470	4K x 1	10-ns	26b
100474	1K x 4	4.5-ns	26c
100474A	1K x 4	5-ns	26d
100474E	1K x 4	3-ns	26e
100476LL	1K x 4	6-ns	26f
100480	16K x 1	10-ns	26g
100484	4K x 4	10-ns	26h
100484A	4K x 4	5-ns	26i
100A484	4K x 4	5-ns	26j
μPD100500	256K x 1	15-ns; BiCMOS	26k

Upcoming Products (101/100K Interface)

Description	Device Number	Comments
16K x 4	μPD101/100494	T_{AA} = 6, 7 ns; 28-pin PDIP/PFP
16K x 4	μPD101/100494LL	Tcycle = 10, 12 ns; 32-pin PDIP/PFP
32K x 9	μPD101/100509	Tcycle = 6, TDQ= 3; registered I/O, scannable; 52-pin PLCC
64K x 4	μPD101/100504	T_{AA} = 8, 10 ns; 32-pin PDIP/PFP

μPB100422
256 x 4-Bit
100K ECL RAM

Description

The μPB100422 is a very high-speed 100K interface ECL RAM organized as 256 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 7 or 10 ns maximum are available in 24-pin ceramic DIP or ceramic flatpack packaging.

Features

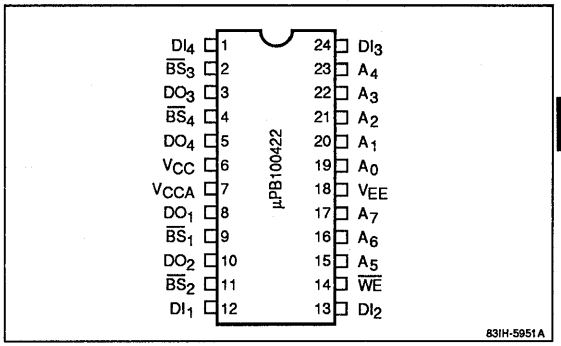
- 256-word x 4-bit organization
- 100K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Low power consumption
- 400-mil, 24-pin ceramic DIP or 24-pin ceramic flatpack packaging

Ordering Information

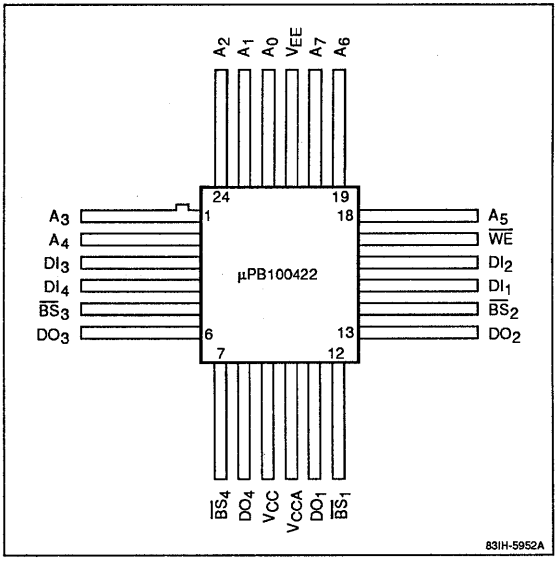
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100422D-7	7 ns	−220 mA	24-pin ceramic DIP
D-10	10 ns		
μPB100422B-7	7 ns	−220 mA	24-pin ceramic flatpack
B-10	10 ns		

Pin Configurations

24-Pin Ceramic DIP



24-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_7	Addresses
$\overline{BS}_1$ - $\overline{BS}_4$	Block select inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature, under bias, $T_{STG\ (bias)}$	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

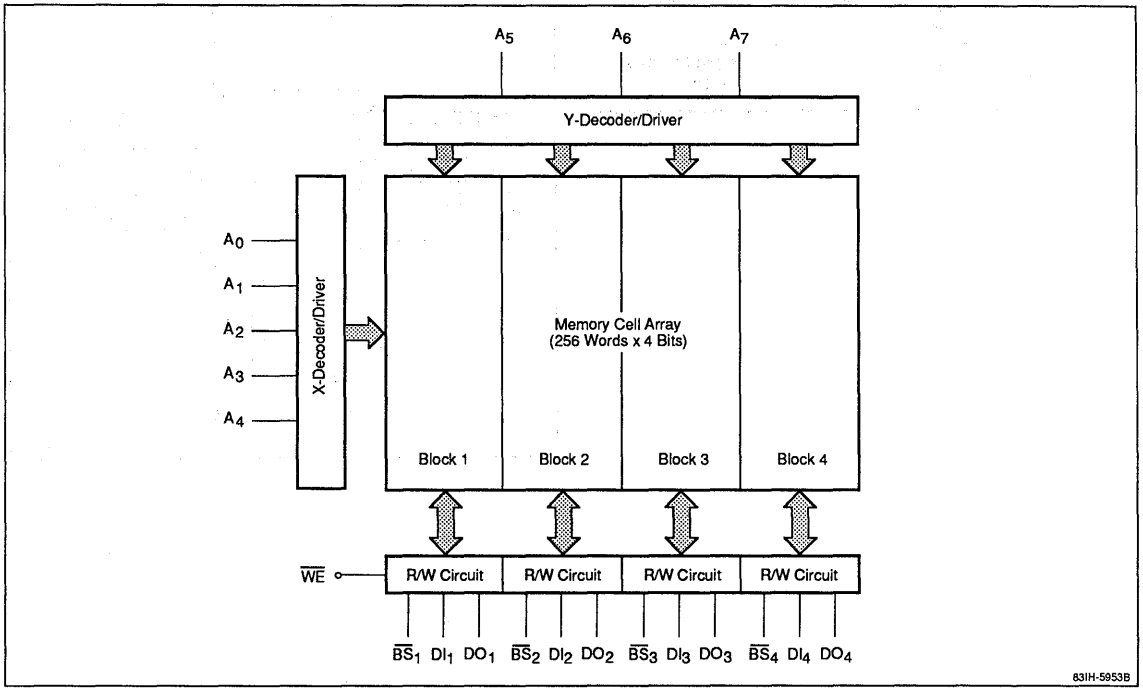
Truth Table

$\overline{BS}$	$\overline{WE}$	DI	DO	Function
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data Valid	Read

Notes:

(1) The Block Select input for each of the four memory blocks is used independently as shown in the block diagram.

Block Diagram



DC Characteristics

T_A = 0 to +85 °C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	For all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	For all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{BS_1}$-$\overline{BS_4}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220			mA	All inputs and outputs open

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85 °C; V_{EE} = −4.5 V ± 5%

		μPB100422-7			μPB100422-10				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Block select access time	t_{ABS}			5			5	ns	
Block select recovery time	t_{RBS}			5			5	ns	
Address access time	t_{AA}			7			10	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			2			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	1			2			ns	
Address hold time	t_{WHA}	1			2			ns	
Block select setup time	t_{WSBS}	1			2			ns	
Block select hold time	t_{WHBS}	1			2			ns	
Write disable time	t_{WS}			5			5	ns	
Write recovery time	t_{WR}			6			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) Device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) All timing measurements are referenced to 50% input levels.

(3) The output load is shown in figure 1.

(4) Input transition times are shown in figure 2.

26a

Figure 1. Loading Conditions Test Circuit

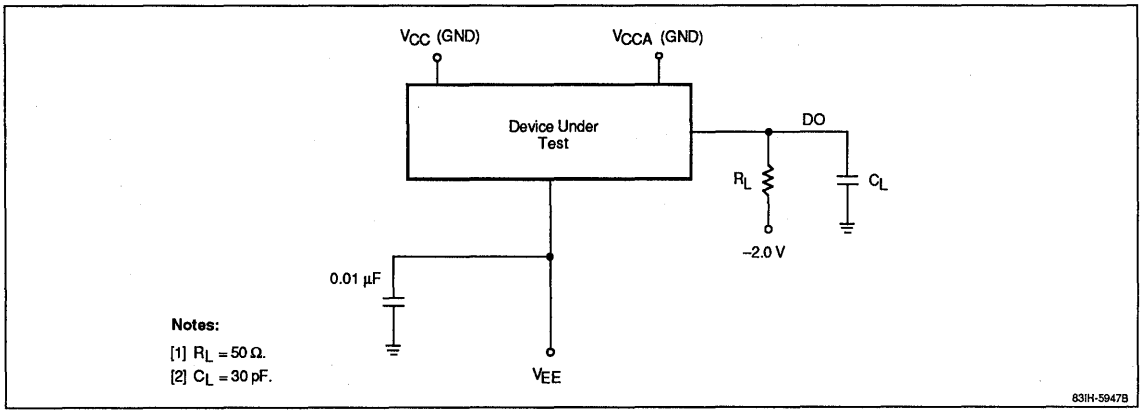
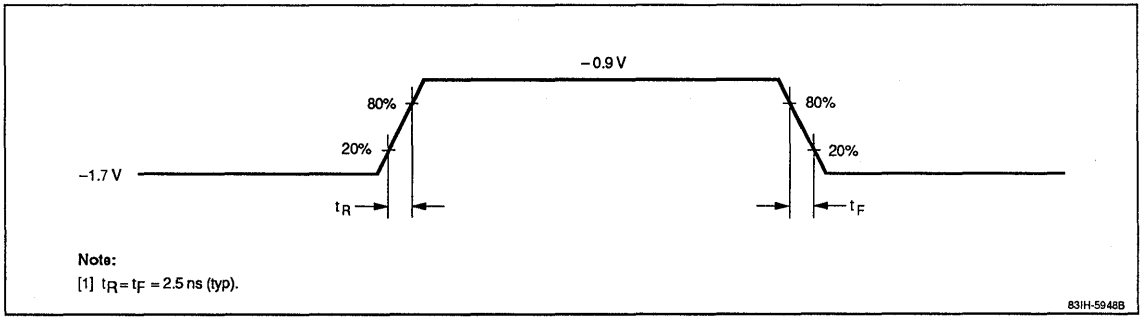
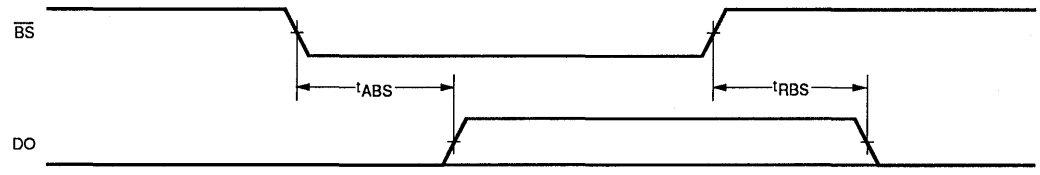


Figure 2. Input Pulse



Timing Waveforms

Chip Select Access

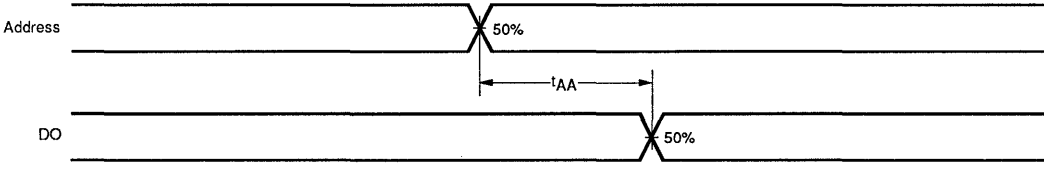


Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{BS}$.

83IH-5972B

Address Access Cycle

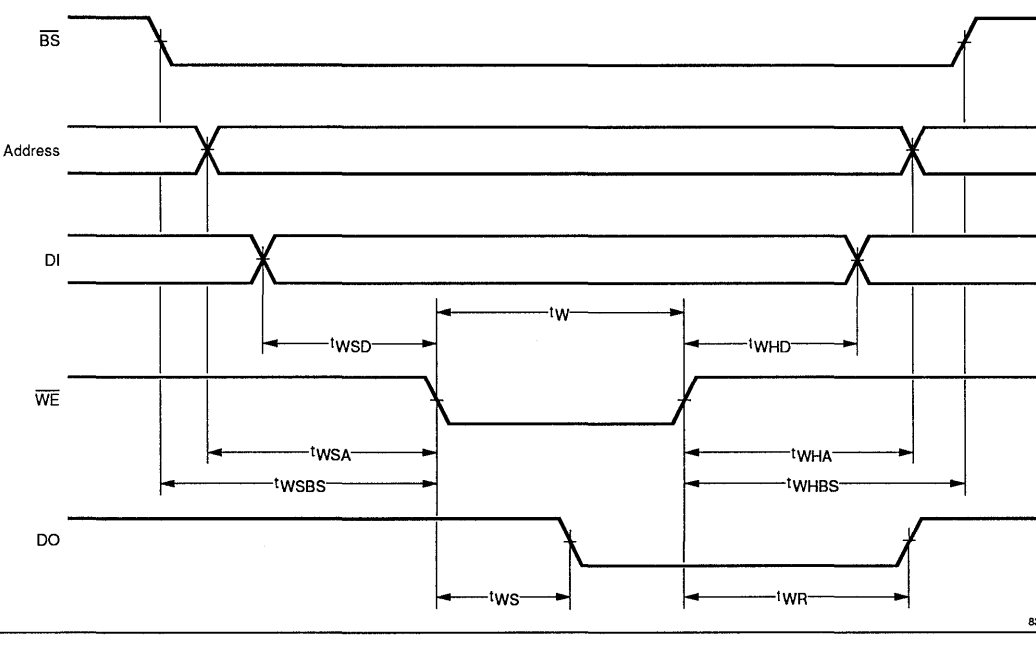


Note:

[1] $\overline{BS} = V_{IL}$

83IH-6203B

Write Cycle



83IH-5955B

μPB100470
4,096 x 1-BIT
100K ECL RAM

Description

The μPB100470 is a very high-speed 100K interface ECL RAM with full voltage and temperature compensation. The device is organized as 4K words by 1 bit, and is designed with an open emitter output (noninverted) for low power consumption. Two fast access time versions are available: 10 ns maximum and 15 ns maximum. The μPB100470 is available in a hermetic, 300-mil, 18-pin cerdip.

Features

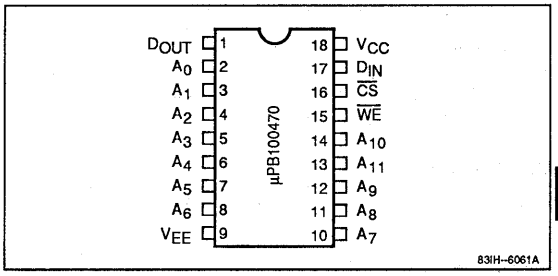
- 4,096-word x 1-bit organization
- 100K ECL interface with full voltage and temperature compensation
- Open emitter output (noninverted)
- Fast access times
- Low power consumption
- 300-mil, 18-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Package
μPB100470D-10	10 ns	18-pin cerdip
D-15	15 ns	

Pin Configuration

18-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	−4.5-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

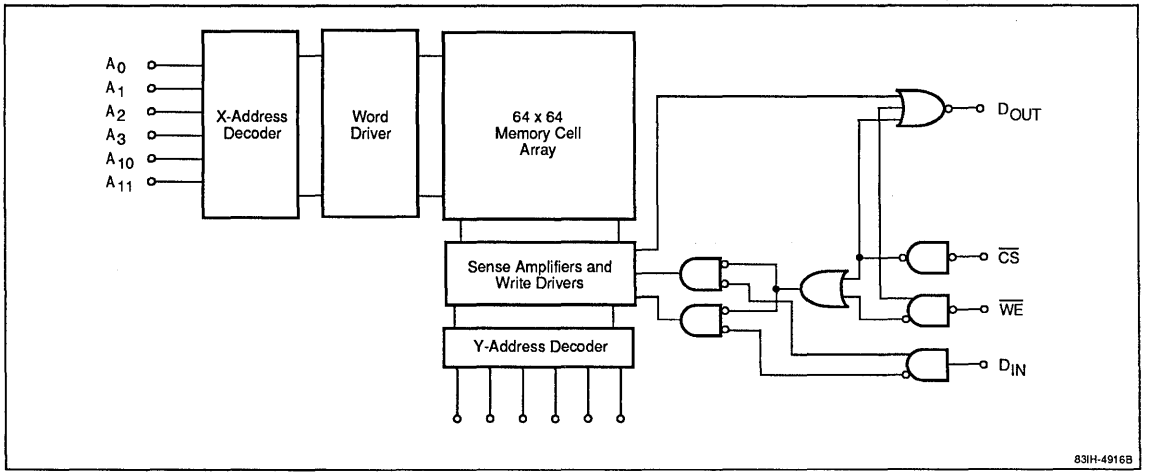
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Function	Output
H	X	X	Not selected	L
L	L	L	Write 0	L
L	L	H	Write 1	L
L	H	X	Read	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025	−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810	−1620	mV	
Output threshold voltage, high	V_{OHC}	−1035		mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}		−1610	mV	
Input voltage, high	V_{IH}	−1165	−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810	−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5	170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50		μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	−220		mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%

		μPB100470-10			μPB100470-15				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select access time	t_{ACS}			6			8	ns	
Chip select recovery time	t_{RCS}			6			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			2			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	3			3			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			6			8	ns	
Write recovery time	t_{WR}			10			10	ns	
Output Rise and Fall Times									
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Figure 1. Loading Conditions Test Circuit

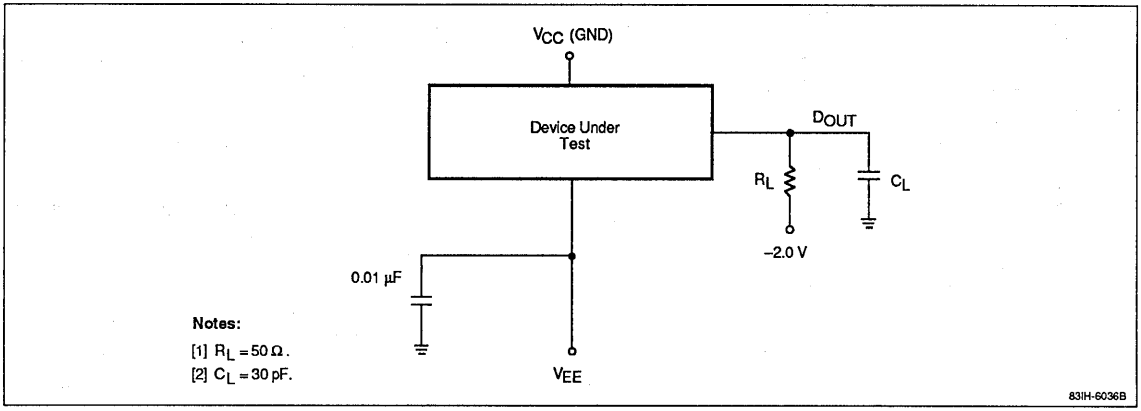
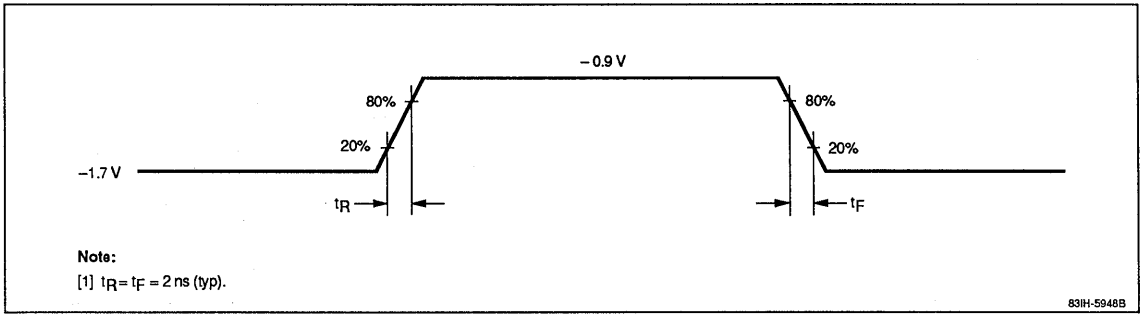
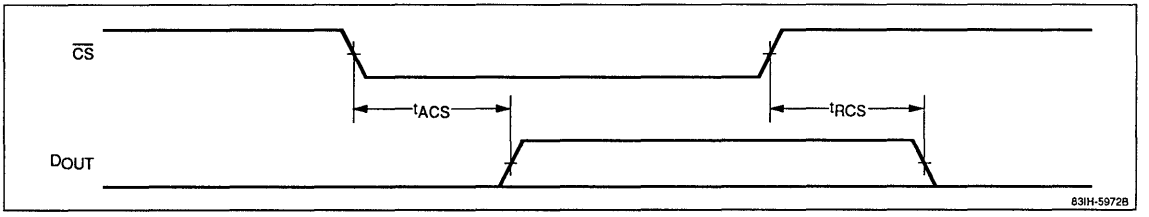


Figure 2. Input Pulse

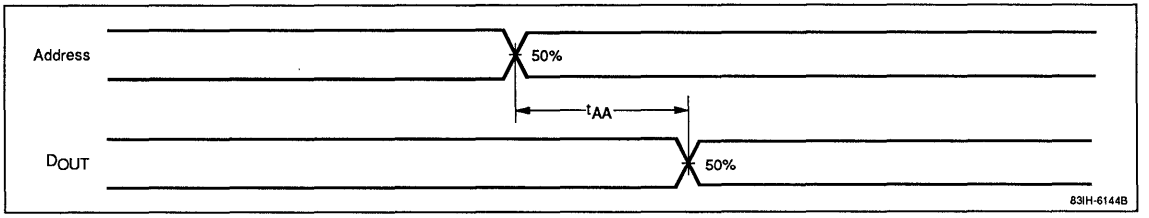


Timing Waveforms

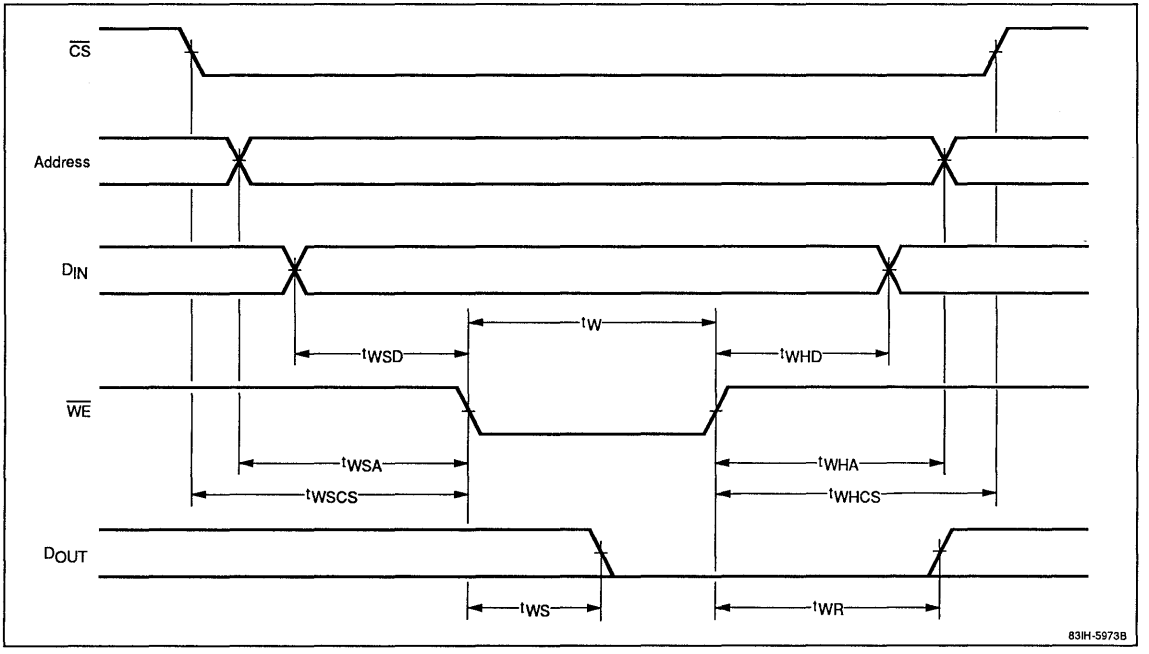
Chip Select Access Cycle



Address Access Cycle



Write Cycle



μPB100474
1,024 x 4-Bit
100K ECL RAM

Description

NEC's μPB100474 is a very high-speed 100K interface ECL RAM organized as 1,024 words by 4 bits and designed with open-emitter, noninverted outputs. It is available in a 24-pin cerdip, 24-pin ceramic LCC, or 24-pin ceramic flatpack package.

Features

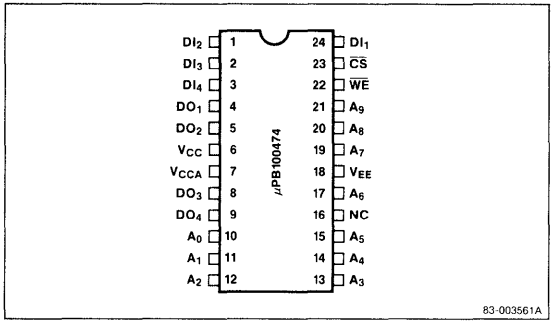
- 1024-word by 4-bit organization
- 100K interface ECL
- Full voltage and temperature compensation
- Noninverted, open emitter outputs
- Fast access times
- 24-pin cerdip, ceramic LCC, and ceramic flatpack packaging

Ordering Information

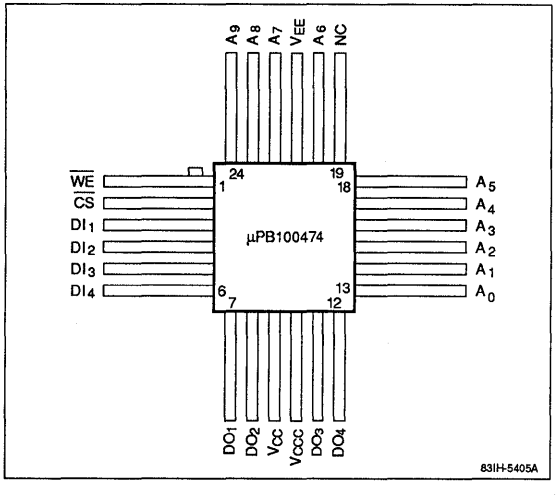
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100474B-6	6 ns	−450 mA	24-pin ceramic flatpack
B-8	8 ns	−220 mA	
B-10	10 ns		
B-15	15 ns		
μPB100474D-8	8 ns	−220 mA	24-pin cerdip
D-10	10 ns		
D-15	15 ns		
μPB100474K-4.5	4.5 ns	−450 mA	24-pin ceramic LCC
K-6	6 ns		

Pin Configurations

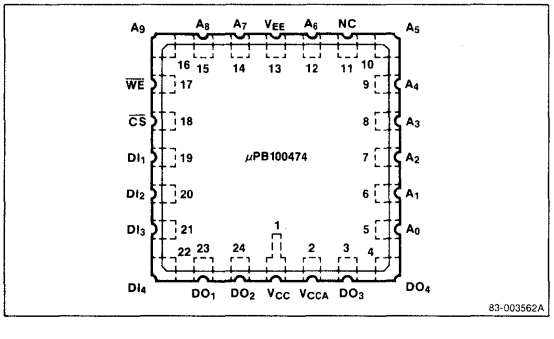
24-Pin Cerdip



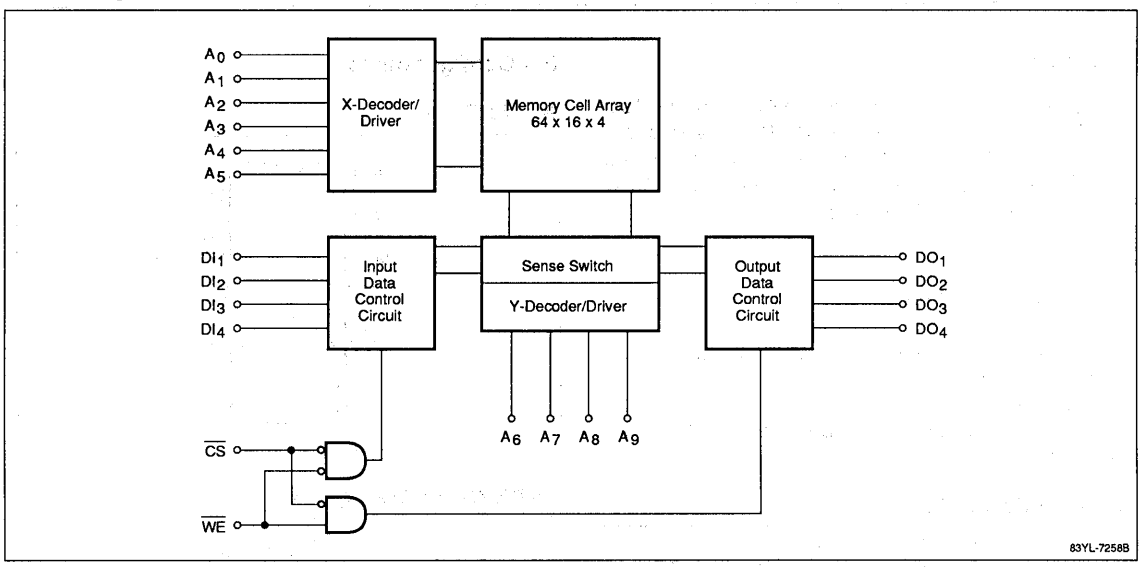
24-Pin Ceramic Flatpack



24-Pin Ceramic LCC



Block Diagram



Pin Identification

Symbol	Function
A_0 - A_9	Addresses
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	Power supply
NC	No connection

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 V to +0.5
Input voltage, V_{IN}	+0.5 V to V_{EE}
Output current, I_{OUT}	−30 mA to +0.1
Storage temperature, T_{STG}	−65 to +150 °C
Storage temperature under bias, T_{STG} (Bias)	−55 to +125 °C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−220			mA	t_{AA} = 8/10/15 ns; all inputs and outputs open
		−450			mA	t_{AA} = 4.5/6 ns; all inputs and outputs open (Note 2)

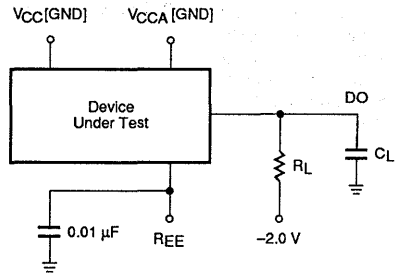
Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 ms.

(2) For the μPB100474-4.5/-6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90 °C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10°C/W.

26c

Figure 1. Loading Conditions Test Circuit



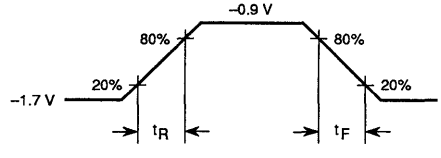
Note:

R_L = 50 Ω

C_L = 30 pF

83YL-7305B

Figure 2. Input Pulse



Note:

t_R = t_F = 2.0 ns

83YL-7306B

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%

Parameter	Symbol	μPB100474-4.5		μPB100474-6		μPB100474-8		μPB100474-10		μPB100474-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Operation												
Chip select access time	t_{ACS}		4		4		5		6		8	ns
Chip select recovery time	t_{RCS}		4		4		5		6		8	ns
Address access time	t_{AA}		4.5		6		8		10		15	ns
Write Operation												
Write pulse width	t_W	4.5		6		6		10		15		ns
Data setup time	t_{WSD}	1		1		1		2		2		ns
Data hold time	t_{WHD}	1		1		1		2		2		ns
Address setup time	t_{WSA}	1		1		1		3		3		ns
Address hold time	t_{WHA}	2		2		1		2		2		ns
Chip select setup time	t_{WSCS}	1		1		1		2		2		ns
Chip select hold time	t_{WHCS}	1		1		1		2		2		ns
Write disable time	t_{WS}		4		4		5		6		8	ns
Write recovery time	t_{WR}		4.5		6		8		10		10	ns

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

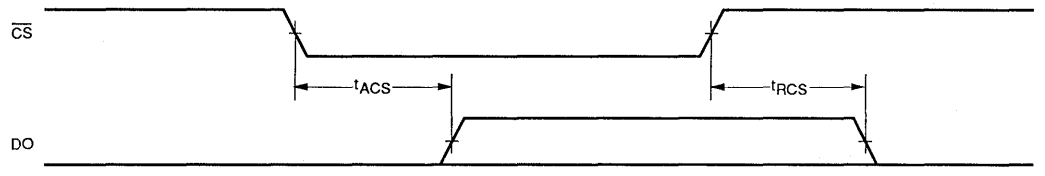
(2) For the μPB100474-4.5/-6, take measures to reduce the thermal resistance and to keep the junction temperature less than 90°C. Forced air and appropriate fins on the substrate on which the package is mounted, or on the package itself, are recommended. The thermal resistance of the junction to the case (bottom side) of an LCC or flatpack package is less than 10°C/W.

(3) See figures 1 and 2 for loading conditions and input pulse timing. For the μPB100474-4.5/-6, C_L = 5 pF. For the μPB100474-8/10/15, C_L = 30 pF.

(4) Output rise and fall times = 2 ns (typ).

Timing Waveforms

Chip Select Access Cycle



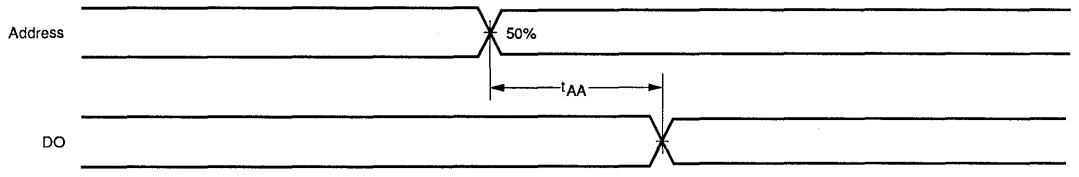
Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

[2] $\overline{WE} = V_{IH}$.

83IH-6164B

Address Access Cycle



Note:

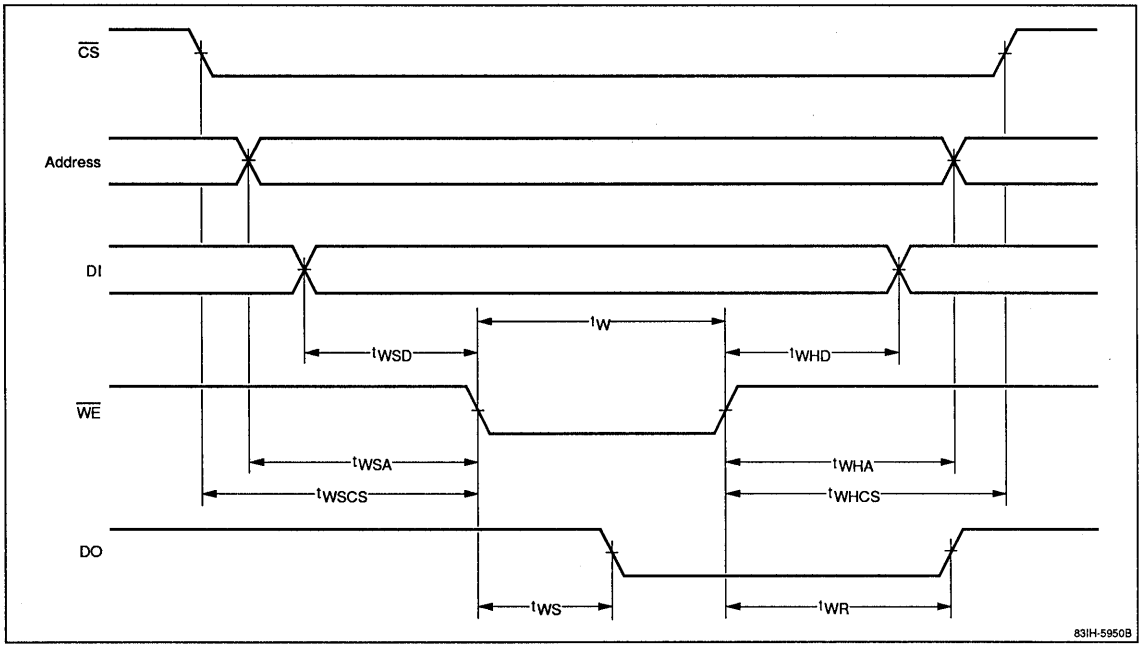
[1] $\overline{CS} = V_{IL}$.

[2] $\overline{WE} = V_{IH}$.

83IH-6144B

Timing Waveforms (cont)

Write Cycle



μPB100474A
1,024 x 4-Bit
100K ECL RAM

Description

The μPB100474A is a very high-speed 100K interface ECL RAM organized as 1,024 words by 4 bits and designed with noninverted, open emitter outputs and full voltage and temperature compensation. The device is packaged in a 24-pin cerdip or ceramic flatpack.

Features

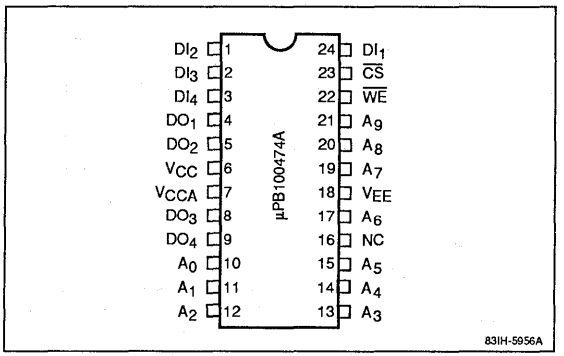
- 1,024 word by 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Open emitter outputs (noninverted)
- Fast access times
- 24-pin cerdip and flatpack packaging

Ordering Information

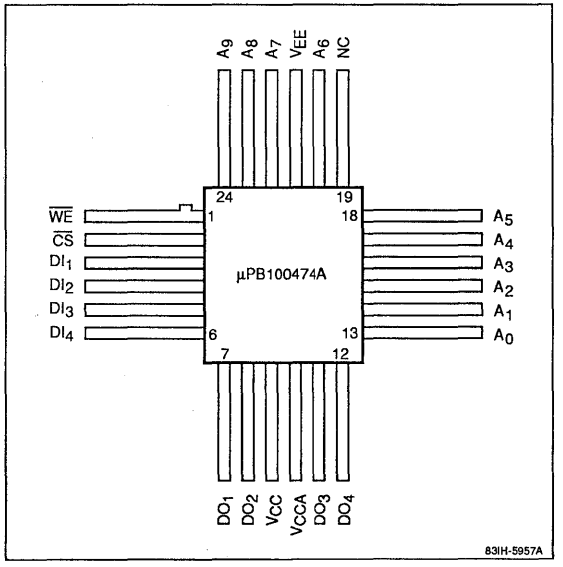
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100474AD-5	5 ns	−250 mA	24-pin cerdip
AD-6	6 ns		
μPB100474ABH-5	5 ns	−250 mA	24-pin ceramic flatpack
ABH-6	6 ns		

Pin Configurations

24-Pin Cerdip



24-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	–4.5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		4		pF
Output capacitance	C_O		6		pF

Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	–7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	–30 to +0.1 mA
Storage temperature, T_{STG}	–65 to +150°C
Storage temperature under bias, T_{STG} (Bias)	–55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

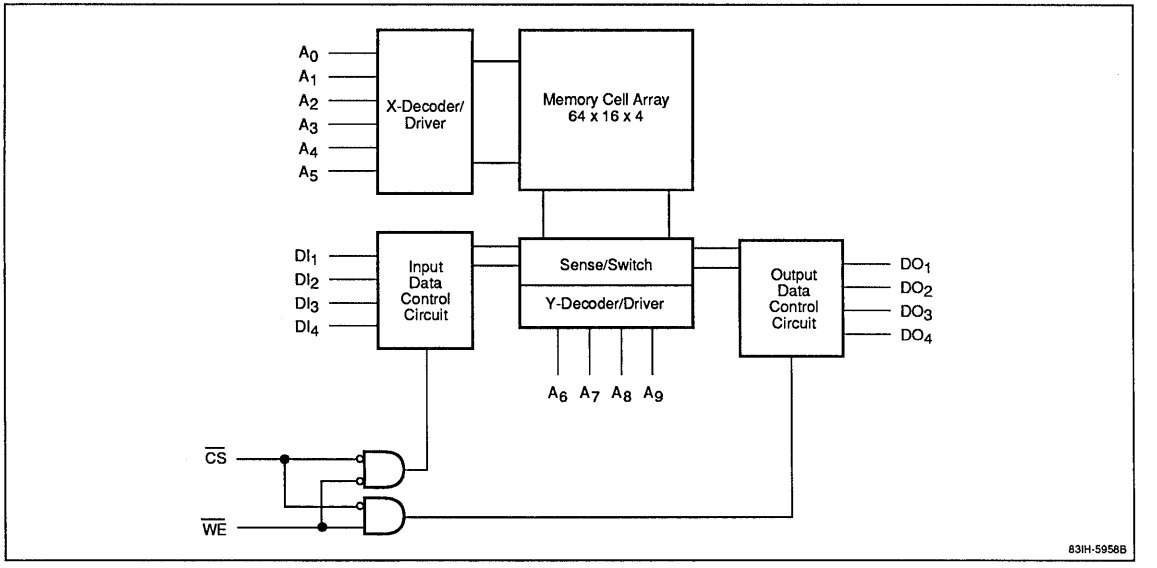
Truth Table

Function	$\overline{CS}$	$\overline{WE}$	D_{IN}	Output
Not selected	H	X	X	L
Write 0	L	L	L	L
Write 1	L	L	H	L
Read	L	H	X	D_{OUT}

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50			μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	−250			mA	All inputs and outputs open

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB100474A-5			μPB100474A-6				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			5			6	ns	
Chip select access time	t_{ACS}			3			4	ns	
Chip select recovery time	t_{RCS}			3			4	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	1			1			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	1			1			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	1			1			ns	
Write disable time	t_{WS}			3			4	ns	
Write recovery time	t_{WR}			6			7	ns	
Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test (DUT) is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

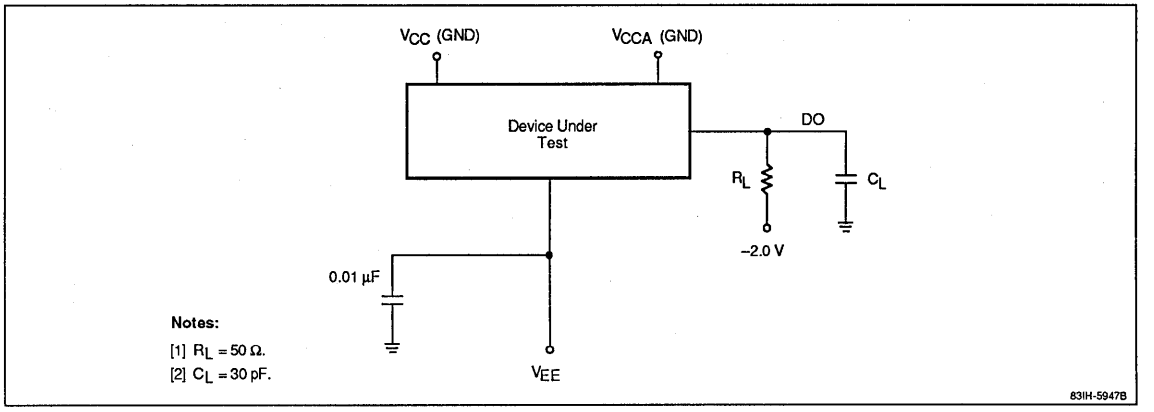
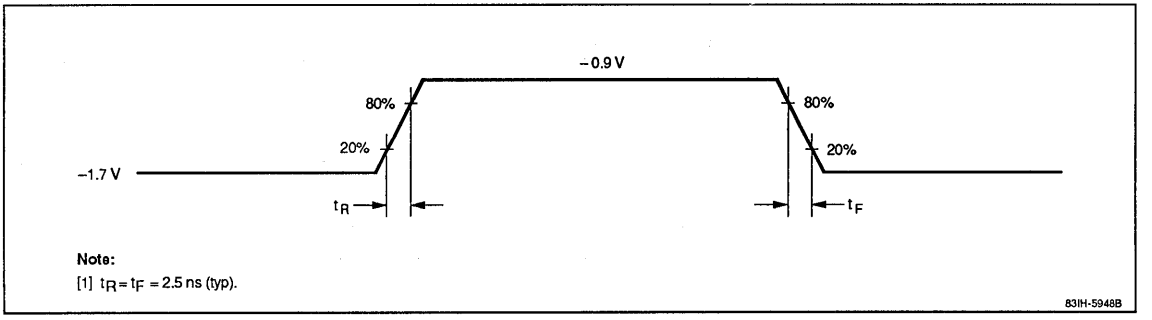
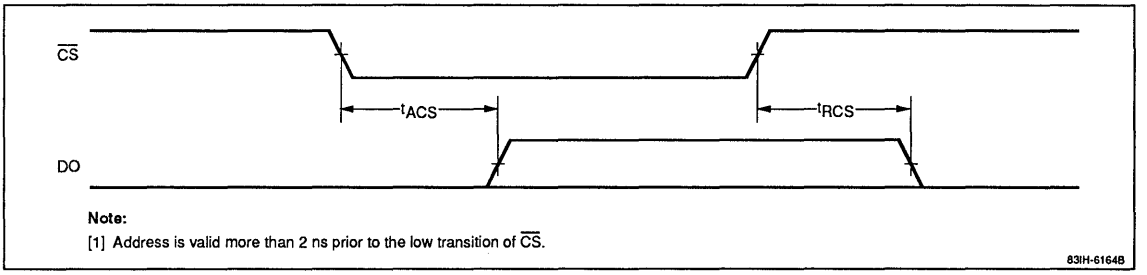


Figure 2. Input Pulse



Timing Waveforms

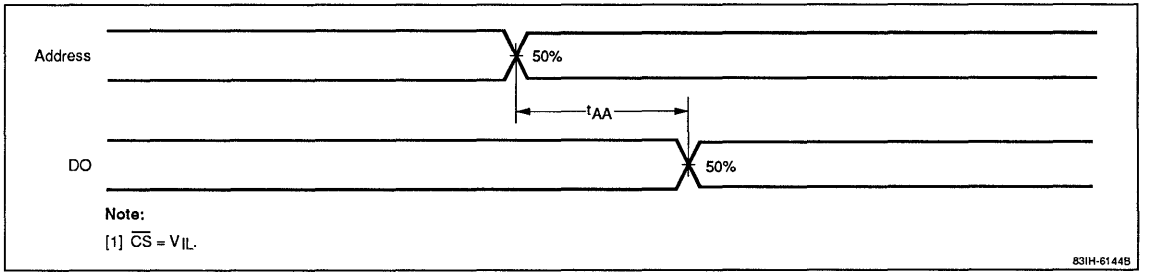
Chip Select Access Cycle



Note:
[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

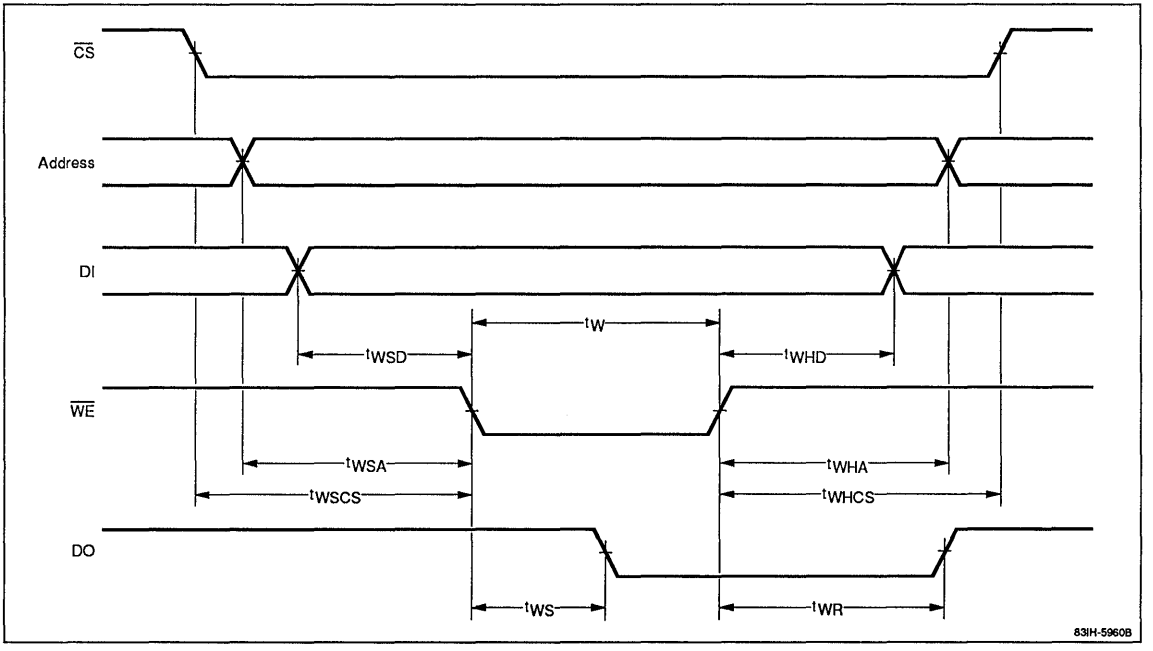
Address Access Cycle



Note:
[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5960B

μPB100474E
1024 x 4-Bit
100K ECL RAM

Description

The μPB100474E is a very-high-speed 100K interface ECL RAM organized as 1024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption.

Features

- 1024-word x 4-bit organization
- 100K ECL interface
- Noninverted, open-emitter outputs
- Fast access times
- Full voltage and temperature compensation
- 24-pin ceramic package, DIP or flatpack

Ordering Information

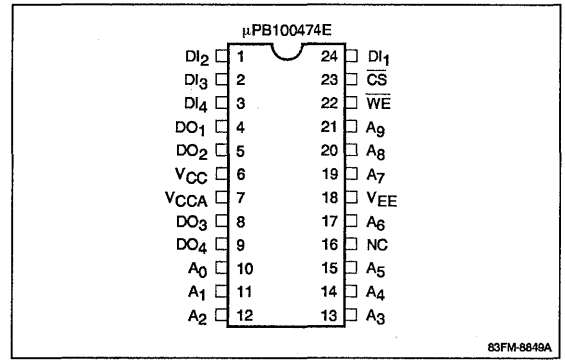
Part Number	Access Time (max)	Package
μPB100474EDH-3	3 ns	24-pin cerdip
DH-4	4 ns	
μPB100474EBH-3	3 ns	24-pin ceramic flatpack
BH-4	4 ns	

Pin Identification

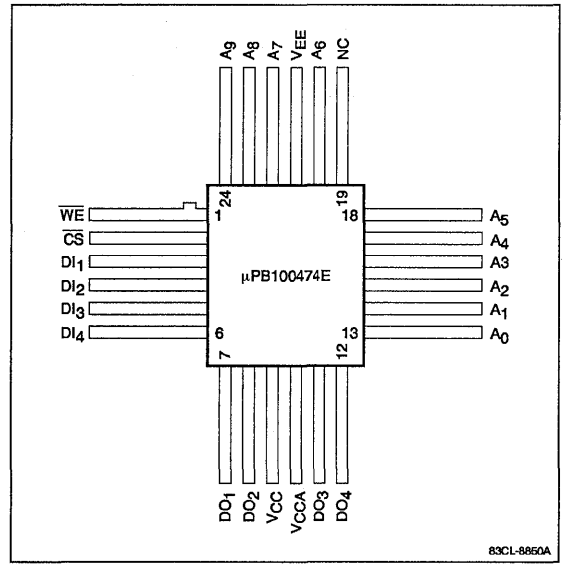
Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable input
$\overline{CS}$	Chip select input
V_{CC}	Power supply ground (current switches and bias driver)
V_{CCA}	Power supply ground (output devices)
V_{EE}	Power supply (–5.2 volts)
NC	No connection

Pin Configurations

24-Pin Cerdip



24-Pin Ceramic Flatpack



Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

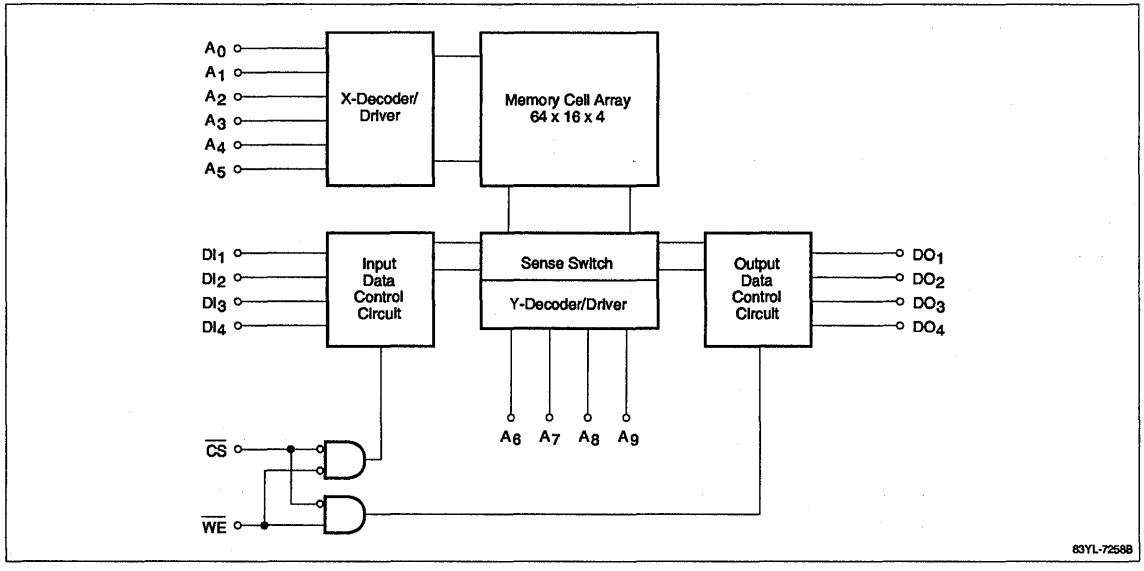
Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{CC} = V_{CCA} = 0 V; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min;
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min;
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max;
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max;
Input voltage, high	V_{IH}	−1165		−880	mV	For all inputs: T_A = 0°C
Input voltage, low	V_{IL}	−1810		−1475	mV	For all inputs: T_A = 0°C
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−330			mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%; output load = 50 Ω to −2.0 V

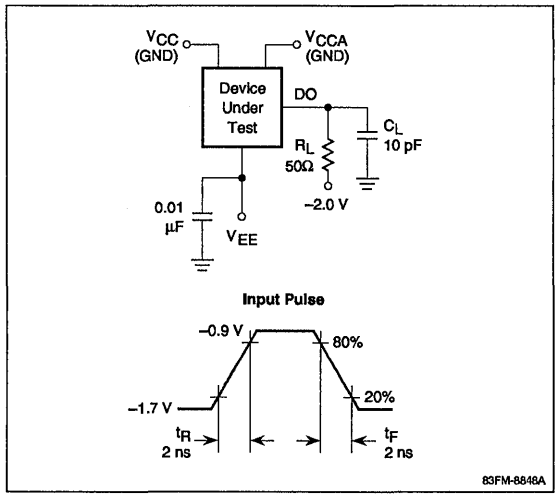
		μPB100474E-3			μPB100474E-4				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			3			4	ns	
Chip select access time	t_{ACS}			2			3	ns	
Chip select recovery time	t_{RCS}			2			3	ns	
Write Operation									
Write pulse width	t_W	5			6			ns	
Address hold time	t_{WHA}	0.5			0.5			ns	
Chip select hold time	t_{WHCS}	0.5			0.5			ns	
Data hold time	t_{WHD}	0.5			0.5			ns	
Write recovery time	t_{WR}			4			5	ns	
Write disable time	t_{WS}			2			3	ns	
Address setup time	t_{WSA}	0.5			0.5			ns	
Chip select setup time	t_{WSCS}	0.5			0.5			ns	
Data setup time	t_{WSD}	0.5			0.5			ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

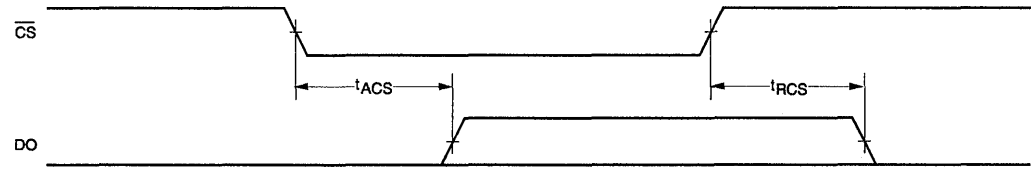
(2) See figure 1 for loading conditions and input pulse shape.

Figure 1. Test Circuit



Timing Waveforms

Chip Select Access Cycle



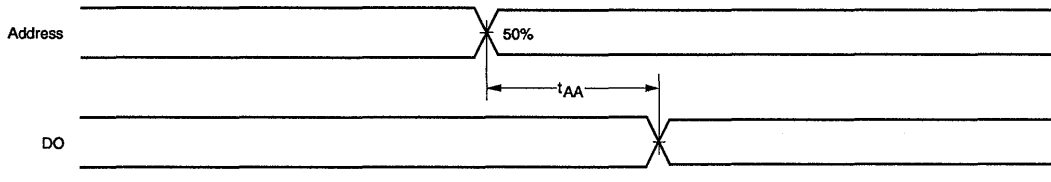
Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

[2] $\overline{WE} = V_{IH}$.

83IH-6164B

Address Access Cycle



Note:

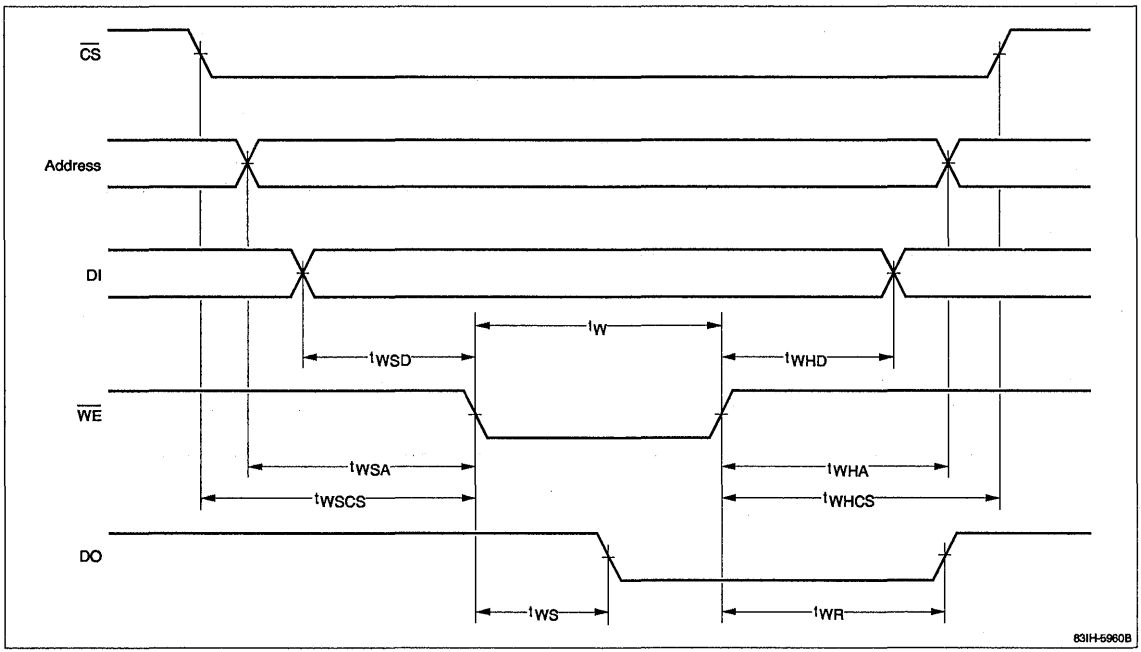
[1] $\overline{CS} = V_{IL}$.

[2] $\overline{WE} = V_{IH}$.

83IH-6144B

Timing Waveforms (cont)

Write Cycle



μPB100476LL
1024 x 4-Bit
100K ECL Synchronous RAM

Preliminary Information

Description

The μPB100476LL is a very-high-speed 100K interface ECL RAM organized as 1024 words by 4 bits and designed with noninverted, open-emitter outputs and low power consumption.

The device integrates input latches, high-speed ECL RAM, output latches, and a write pulse generator. The synchronous design allows precise cycle control by use of an internal clock.

Features

- 1024-word x 4-bit organization
- 100K ECL interface
- High-speed clock cycle: 6 ns
- Latched I/O
- Self-timed write
- 28-pin ceramic package, DIP or flatpack

Ordering Information

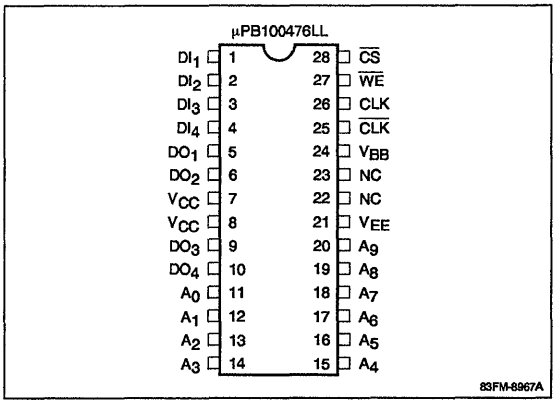
Part Number	Access Time (max)	Package
μPB100476LLDH-6	6 ns	28-pin cerdip
BH-6	6 ns	28-pin ceramic flatpack

Pin Identification

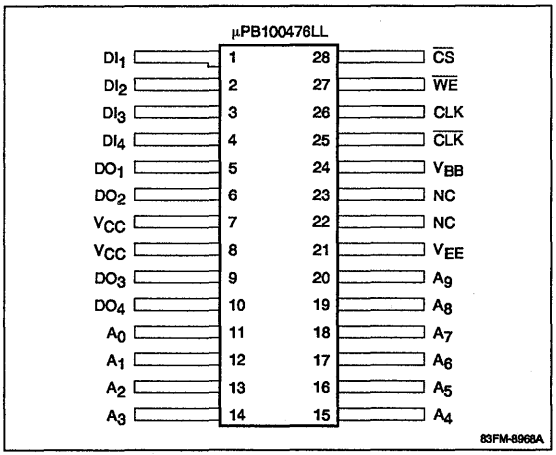
Symbol	Function
A_0 - A_9	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
CLK, $\overline{CLK}$	Clock inputs
$\overline{CS}$	Chip select input
$\overline{WE}$	Write enable input
V_{BB}	Reference voltage output
V_{CC}	Power supply ground (current switches and bias driver)
V_{CCA}	Power supply ground (output devices)
V_{EE}	Power supply (–5.2 volts)
NC	No connection

Pin Configurations

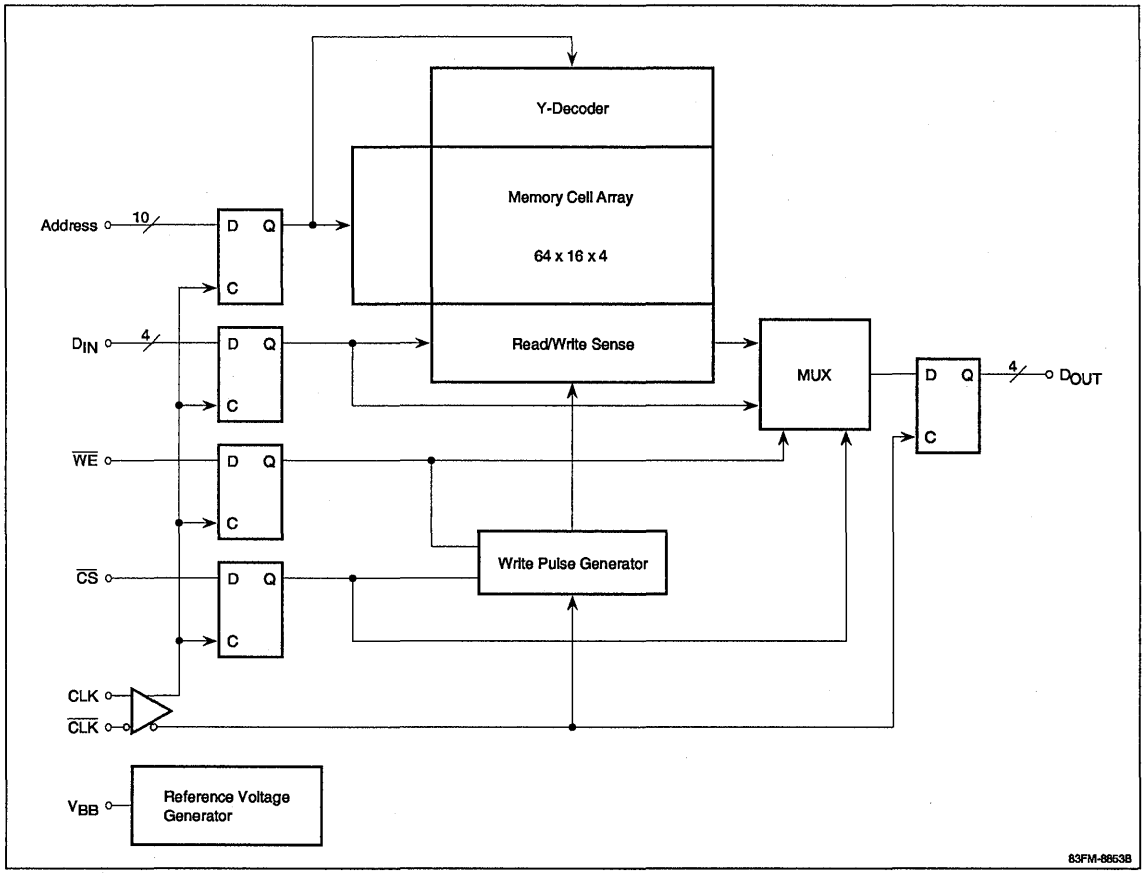
28-Pin Cerdip



28-Pin Ceramic Flatpack



Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{EE} to V_{CC}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		5		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

X = don't care.

DC Characteristics

T_A = 0 to +85°C; V_{CC} = V_{CCA} = 0 V; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−350			mA	All inputs and outputs open
Reference voltage	V_{BB}	−1390		−1250	mV	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V

		μPB100476LL-6				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Address access time	$t_{A(Add)}$			2.5	ns	t_{SA} = 0.5 ns
Clock access time	$t_{A(Clk)}$			3.3	ns	$t_{WL(Clk)}$ = 1.5 ns
$\overline{CS}$ access time	$t_{A(CS)}$			2.3	ns	t_{SC} = 0.5 ns
Data access time	$t_{A(DI)}$			2.3	ns	t_{SD} = 0.5 ns
Write access time	$t_{A(W)}$			2.3	ns	t_{SW} = 0.5 ns
Clock cycle time	t_{CYC}	6			ns	
Data release time	t_{DR}	0.3		1.8	ns	$t_{WL(Clk)} > t_{A(Clk)}$ max, $t_{SA} > t_{A(Add)}$ max, $t_{SC} > t_{A(CS)}$ max, $t_{SD} > t_{A(DI)}$ max
Address hold time	t_{HA}	1			ns	
$\overline{CS}$ hold time	t_{HC}	1			ns	
Data hold time	t_{HD}	1			ns	
$\overline{WE}$ hold time	t_{HW}	1			ns	
Address setup time	t_{SA}	0.5			ns	
$\overline{CS}$ setup time	t_{SC}	0.5			ns	
Data setup time	t_{SD}	0.5			ns	
$\overline{WE}$ setup time	t_{SW}	0.5			ns	
Clock high-pulse width	$t_{WH(Clk)}$	4.5			ns	
Clock low-pulse width	$t_{WL(Clk)}$	1.5			ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figure 1 for loading conditions and input pulse shape.

Figure 1. Test Circuit

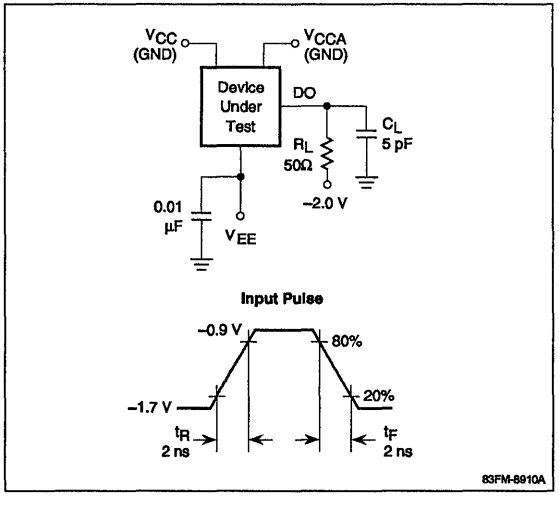
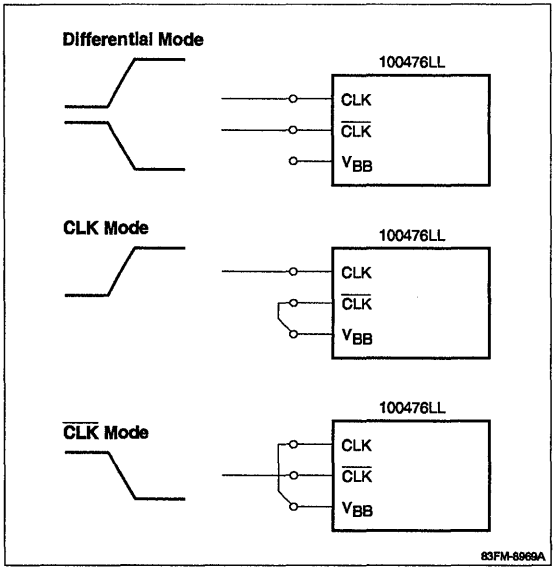
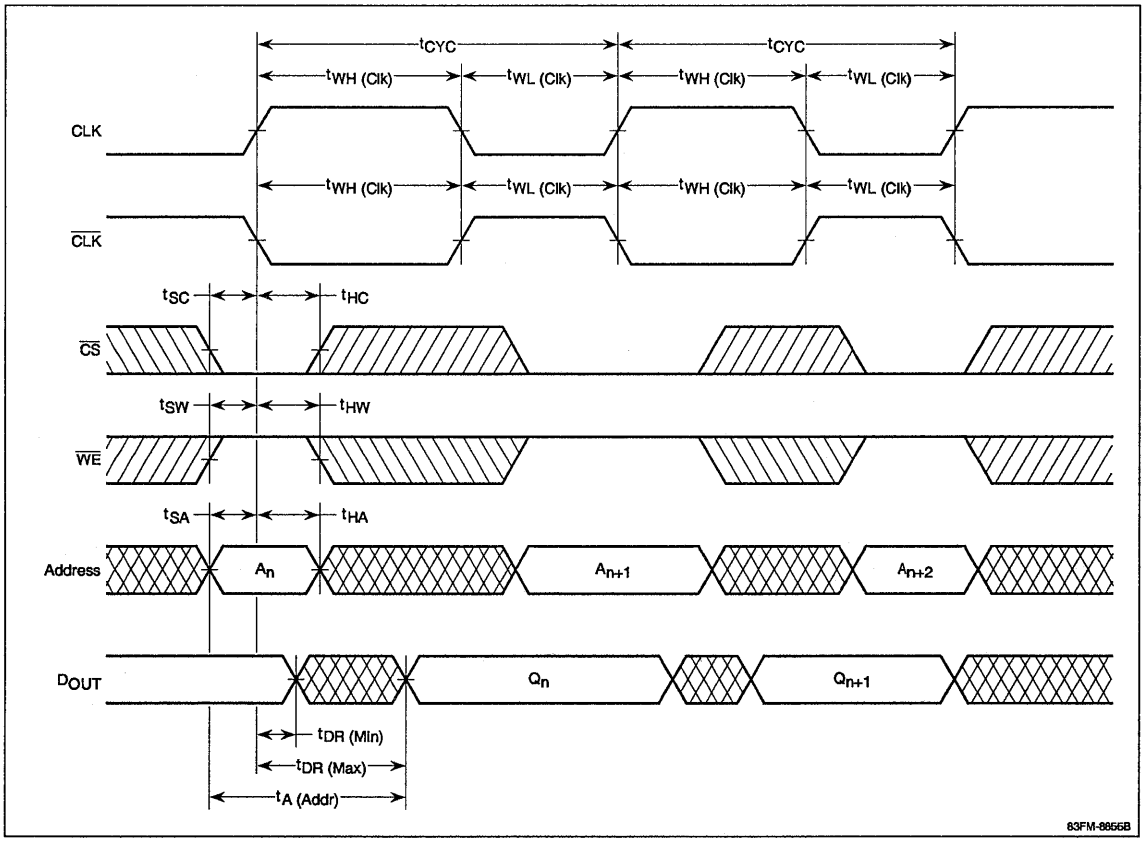


Figure 2. Clock Input Modes



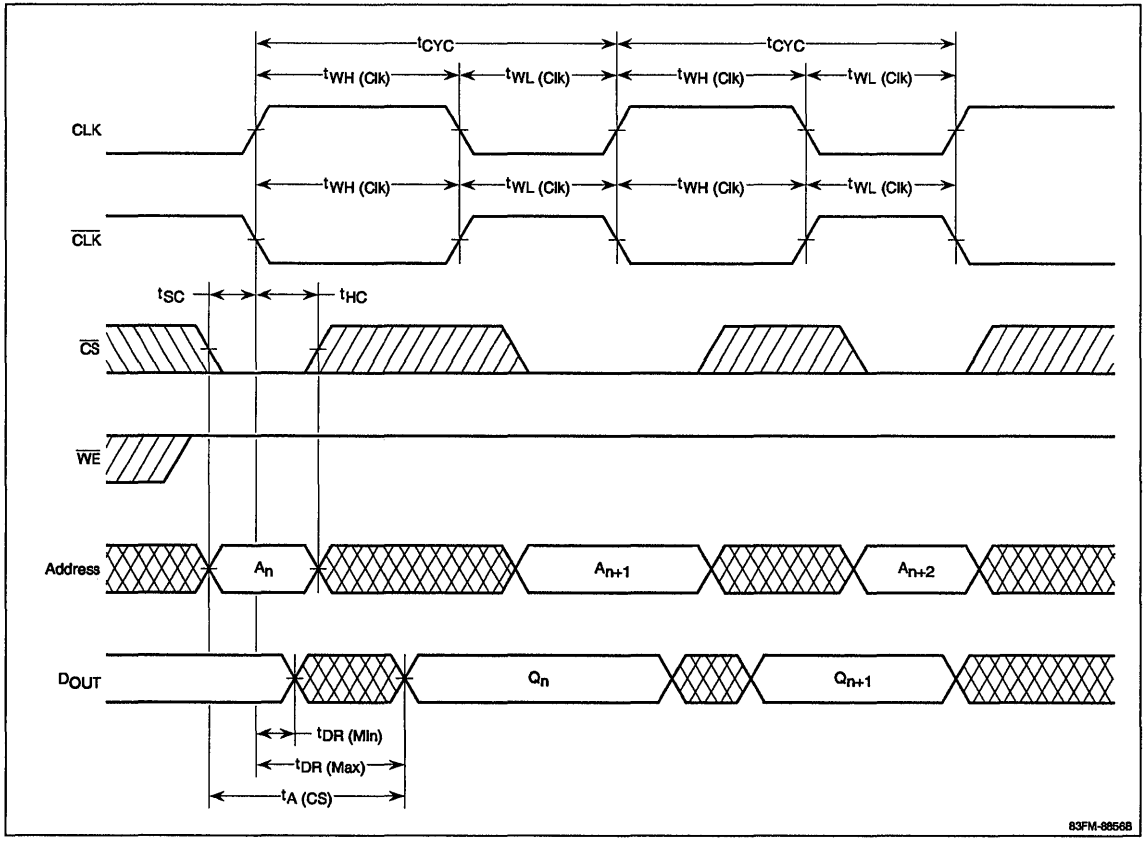
Timing Waveforms

Address Access, Read Mode



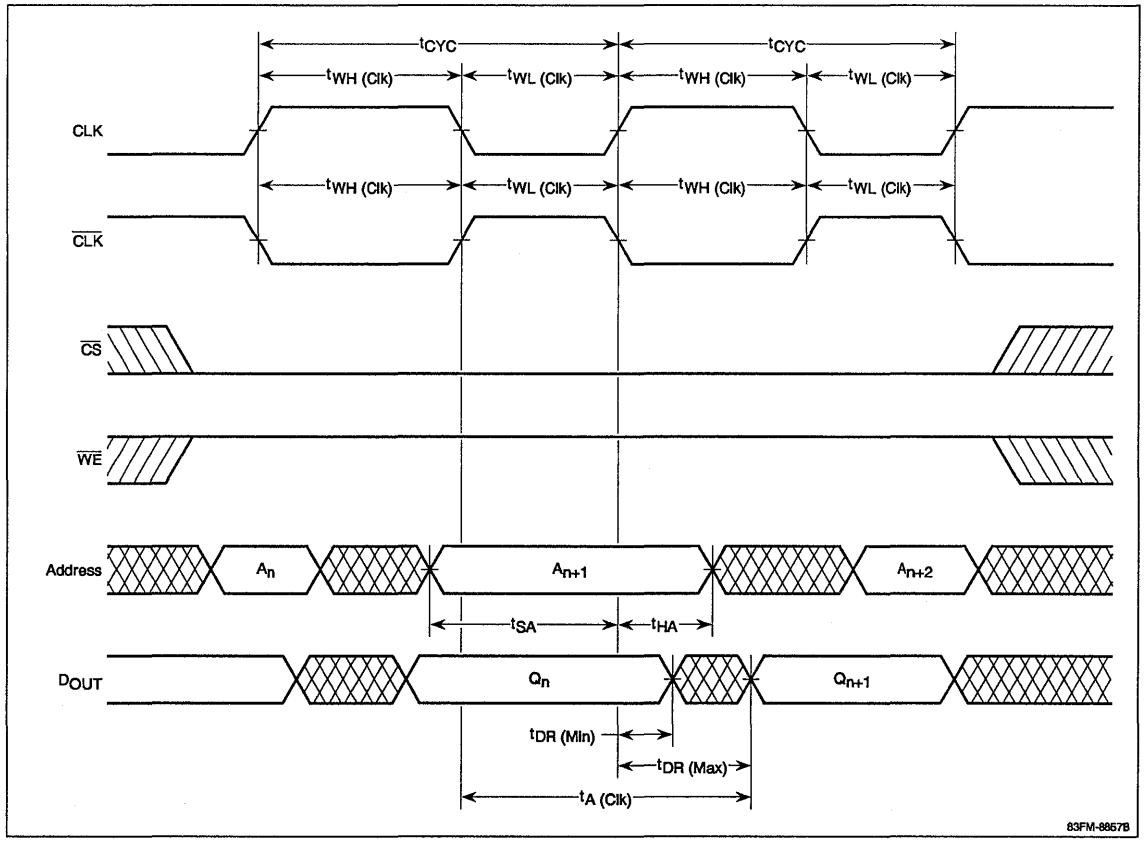
Timing Waveforms (cont)

Chip Select Access, Read Mode



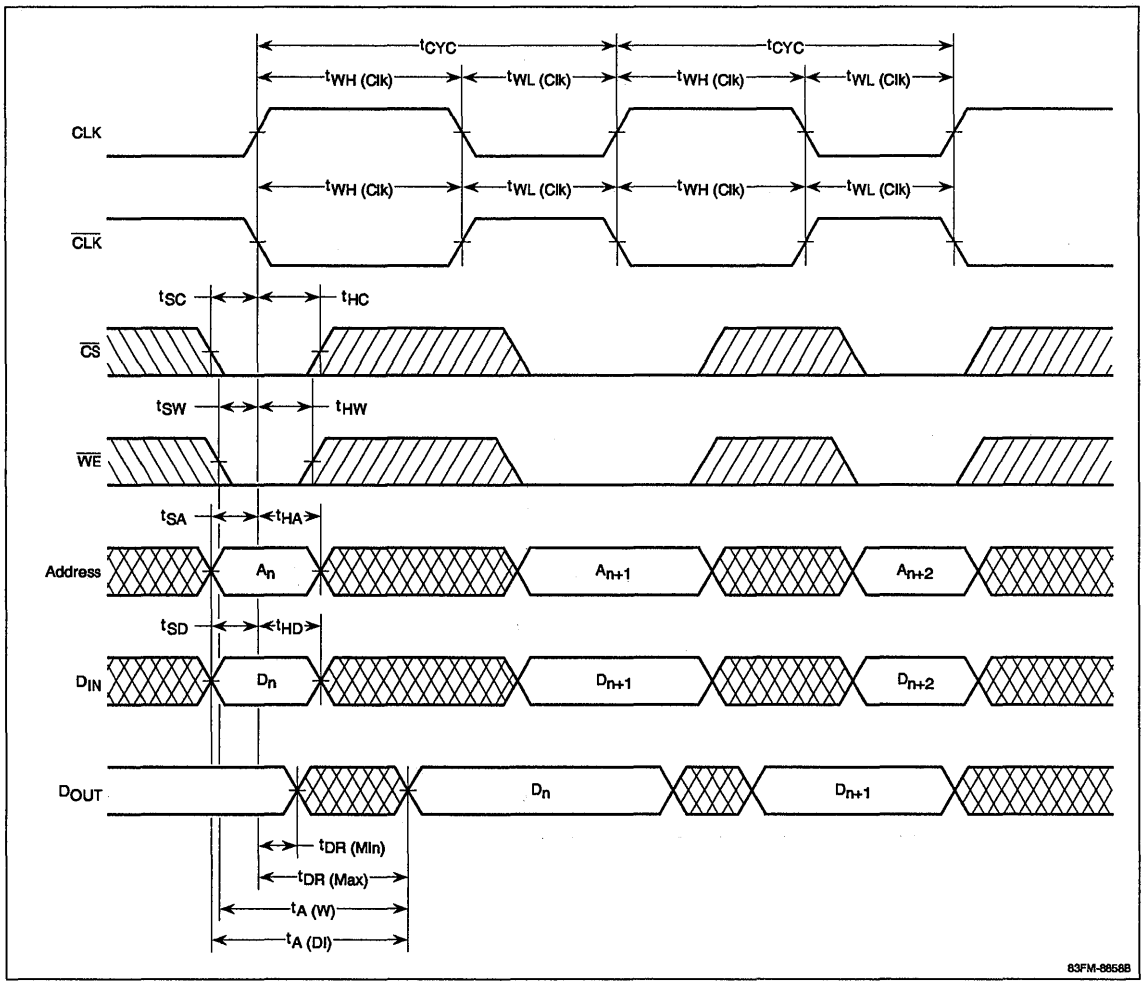
Timing Waveforms (cont)

Clock Access, Read Mode



Timing Waveforms (cont)

Write Mode



μPB100480
16,384 x 1-Bit
100K ECL RAM

Description

The μPB100480 is a very high-speed 100K interface ECL RAM with full voltage and temperature compensation. The device is organized as 16,384 words by 1 bit and designed with noninverted, open-emitter outputs and low power consumption. Two versions with fast access times of 10 ns and 15 ns maximum are available. The μPB100480 is packaged in a hermetic, 300-mil, 20-pin cerdip or 20-pin ceramic flatpack.

Features

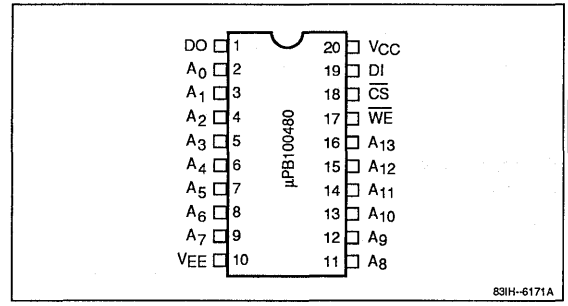
- 16,384-word x 1-bit organization
- 100K ECL interface with full voltage and temperature compensation
- Noninverted, open-emitter outputs
- Fast access times of 10 and 15 ns maximum
- Low power consumption
- 300-mil, 20-pin cerdip or 20-pin ceramic flatpack packaging

Ordering Information

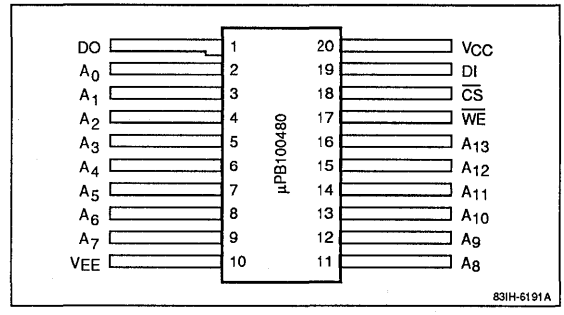
Part Number	Access Time (max)	Power Consumption (max)	Package
μPB100480D-10	10 ns	1.2 W	20-pin cerdip
D-15	15 ns	1.1 W	
μPB100480B-10	10 ns	1.2 W	20-pin ceramic flatpack
B-15	15 ns	1.1 W	

Pin Configurations

20-Pin Cerdip



20-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_{13}	Address inputs
DI	Data input
DO	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	−4.5-volt power supply

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

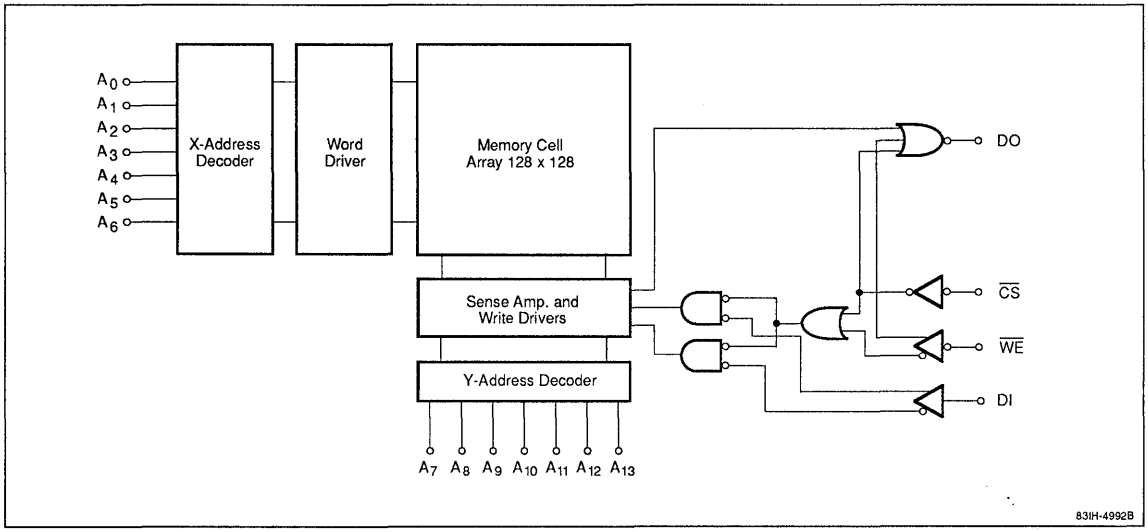
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810		−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB100480-10: all inputs and outputs open
		−240			mA	For μPB100480-15: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

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AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%

		μPB100480-10			μPB100480-15				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select recovery time	t_{RCS}			5			8	ns	
Chip select access time	t_{ACS}			5			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	2			3			ns	
Address hold time	t_{WHA}	1			2			ns	
Chip select setup time	t_{WSCS}	2			3			ns	
Chip select hold time	t_{WHCS}	1			2			ns	
Write disable time	t_{WS}			5			8	ns	
Write recovery time	t_{WR}			11			17	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% to 20%) = 2.5 ns; input and output timing reference level = 50%.

Figure 1. Loading Conditions Test Circuit

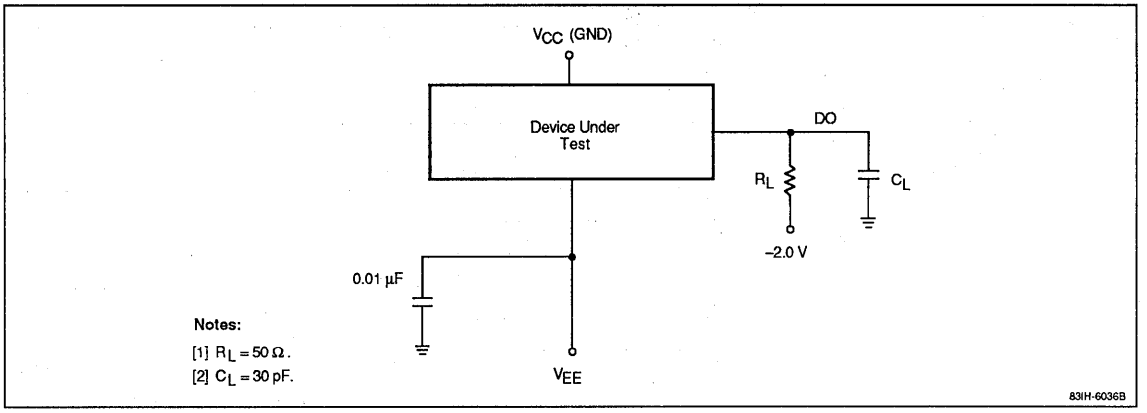
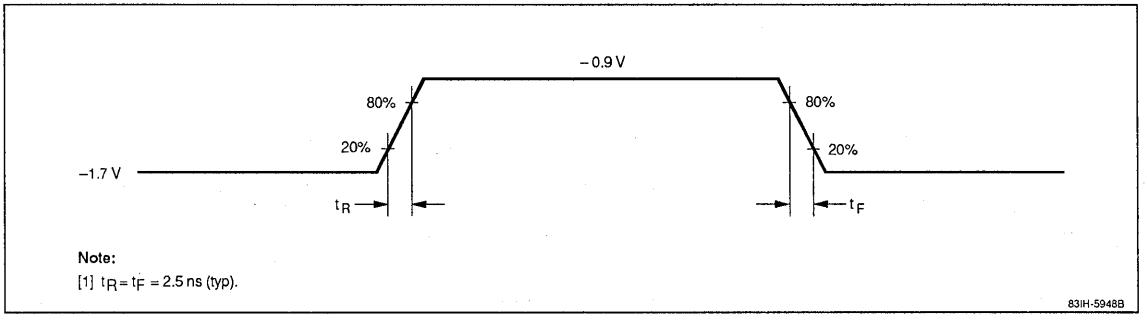
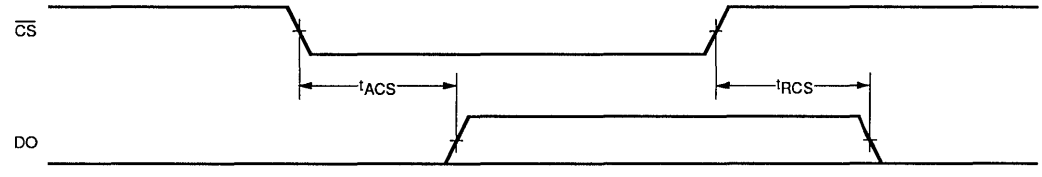


Figure 2. Input Pulse



Timing Waveforms

Chip Select Access Cycle

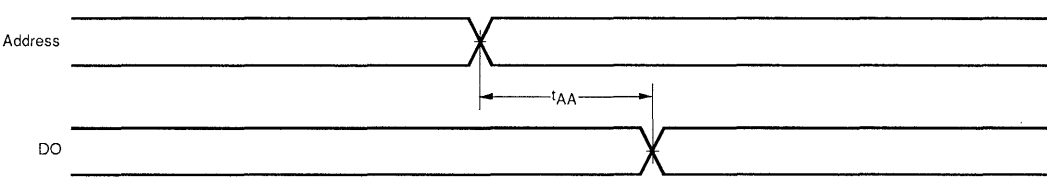


Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

Address Access Cycle

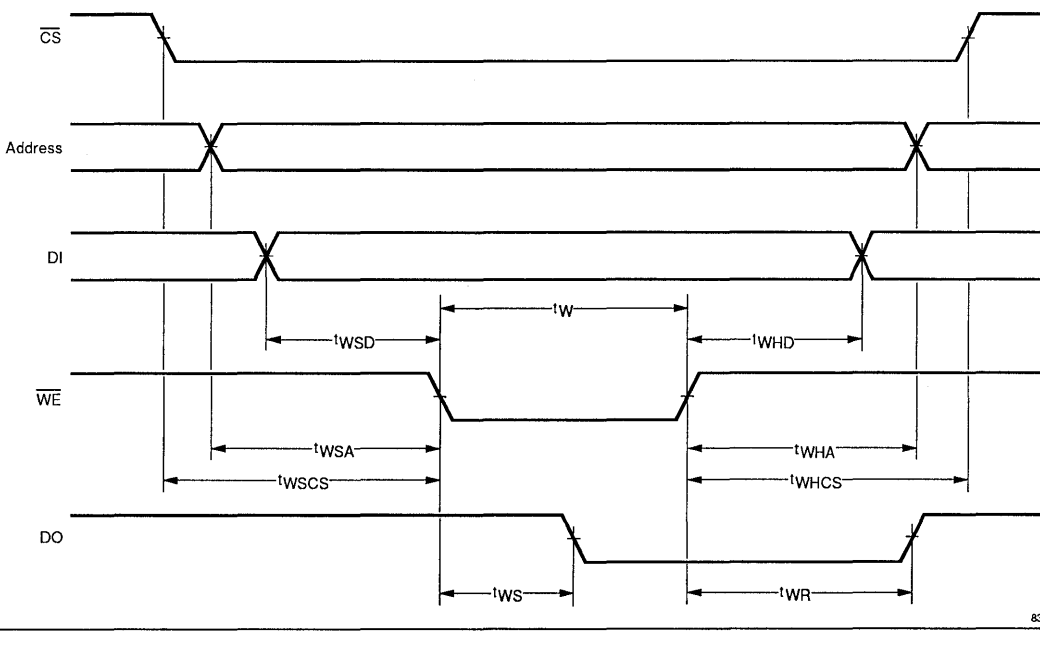


Note:

[1] $\overline{CS} = V_{IL}$

83IH-5954B

Write Cycle



83IH-5950B

μPB100484
4,096 x 4-Bit
100K ECL RAM

Description

The μPB100484 is a very high-speed 100K interface ECL RAM organized as 4,096 words by 4 bits with open-emitter outputs (noninverted). It is available in 28-pin cerdip or flatpack packages.

Features

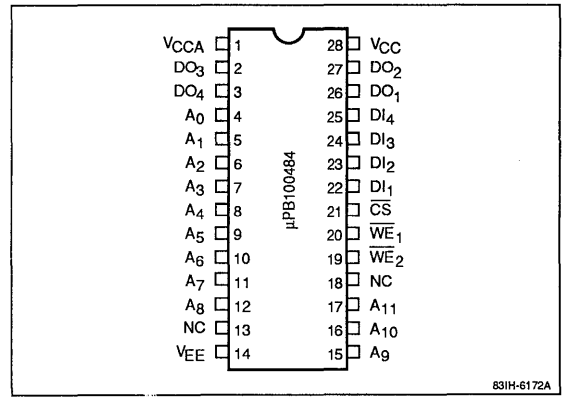
- 4,096-word x 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Open-emitter outputs (noninverted)
- Fast access times and low power consumption
- 28-pin cerdip and 28-pin flatpack packaging

Ordering Information

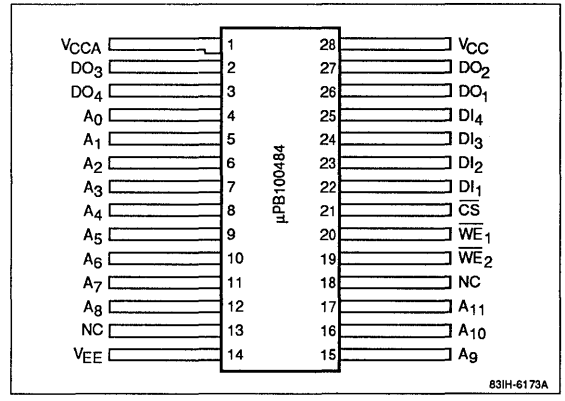
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100484D-10	10 ns	−260 mA	28-pin cerdip
D-15	15 ns	−240 mA	
μPB100484B-10	10 ns	−260 mA	28-pin ceramic flatpack
B-15	15 ns	−240 mA	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	−4.5-volt power supply
NC	No connection

Capacitance

f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Truth Table

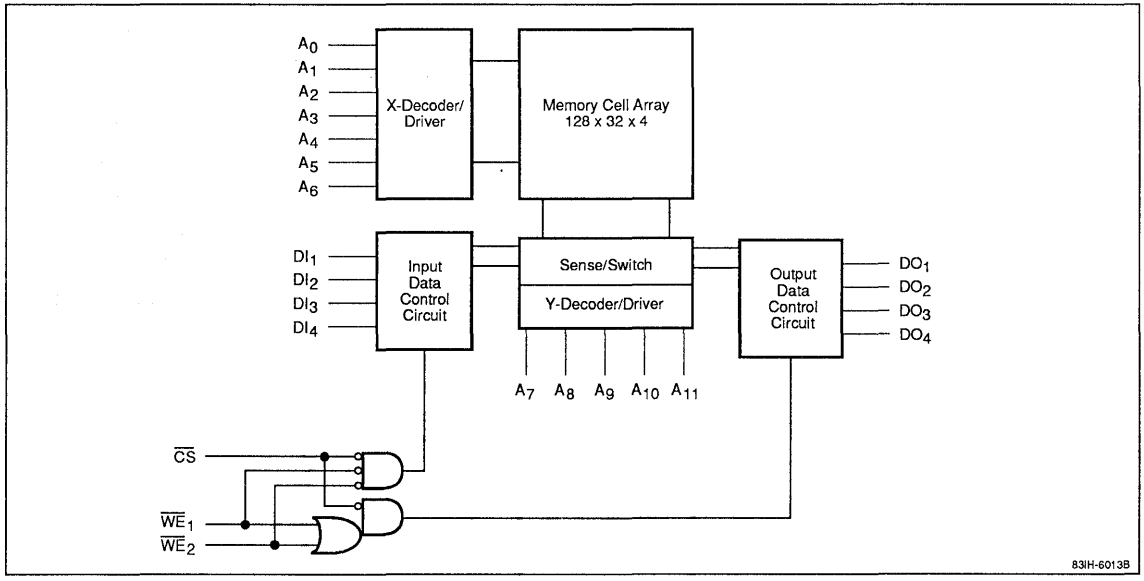
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE}_1$ and $\overline{WE}_2$ must be low to initiate write operation. For read operation, either $\overline{WE}_1$ or $\overline{WE}_2$ or both must be high.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB100484-10: all inputs and outputs open
		−240			mA	For μPB100484-15: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB100484-10			μPB100484-15				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			10			15	ns	
Chip select recovery time	t_{RCS}			5			8	ns	
Chip select access time	t_{ACS}			5			8	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	1			2			ns	
Address setup time	t_{WSA}	2			3			ns	
Address hold time	t_{WHA}	1			2			ns	
Chip select setup time	t_{WSCS}	2			3			ns	
Chip select hold time	t_{WHCS}	1			2			ns	
Write disable time	t_{WS}			5			8	ns	
Write recovery time	t_{WR}			11			17	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figure 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times = 2.5 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

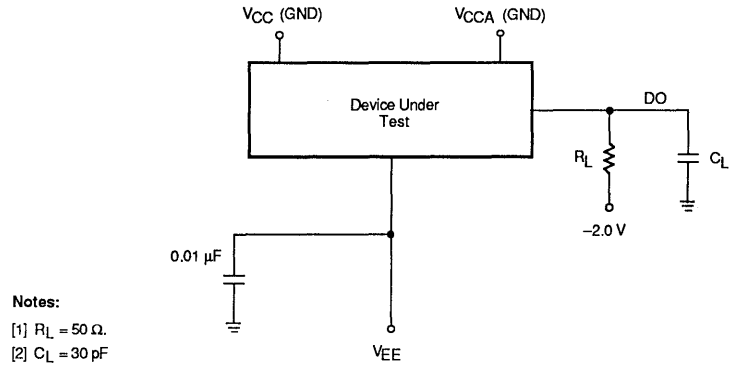
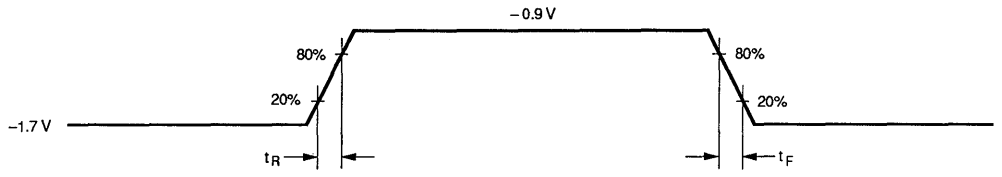


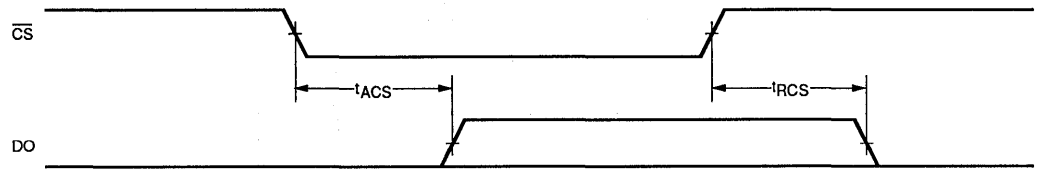
Figure 2. Input Pulse



26h

Timing Waveforms

Chip Select Access Cycle

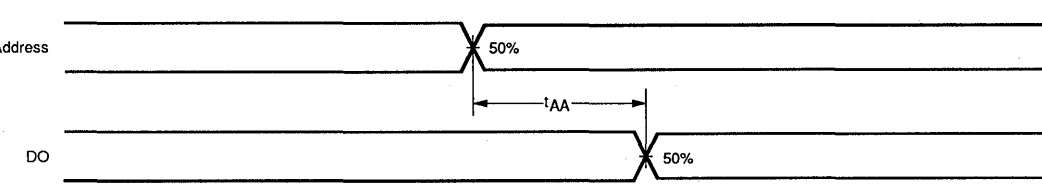


Note:

[1] Address is valid more than 2 ns prior to the low transition of $\overline{CS}$.

83IH-6164B

Address Access Cycle

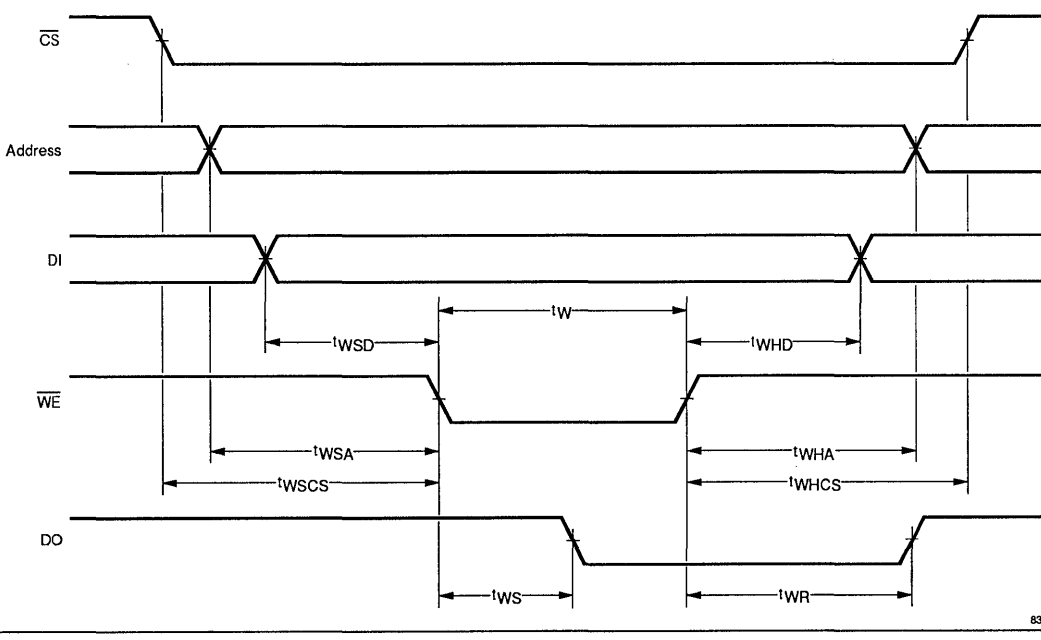


Note:

[1] $\overline{CS} = V_{IL}$.

83IH-6144B

Write Cycle



83IH-5950B

Description

The μPB100484A is a very high-speed 100K interface ECL RAM. It is organized as 4,096 words by 4 bits with noninverted, open-emitter outputs and low power consumption. Two access time versions are available: 5 ns and 7 ns maximum. The μPB100484A is available in a hermetic, 400-mil, 28-pin cerdip or 28-pin ceramic flatpack.

Features

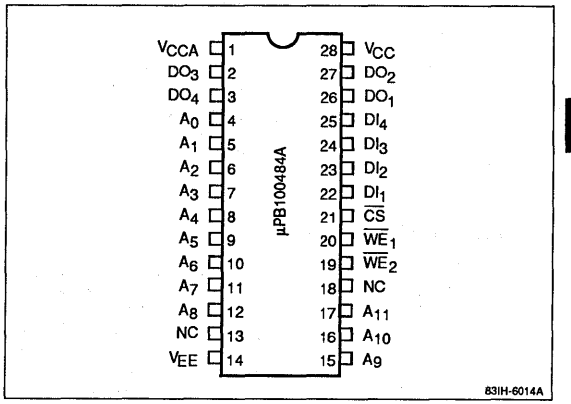
- 4,096-word x 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Noninverted, open-emitter outputs
- Fast access times: 5 and 7 ns maximum
- Low power consumption
- 400-mil, 28-pin cerdip or 28-pin ceramic flatpack packaging

Ordering Information

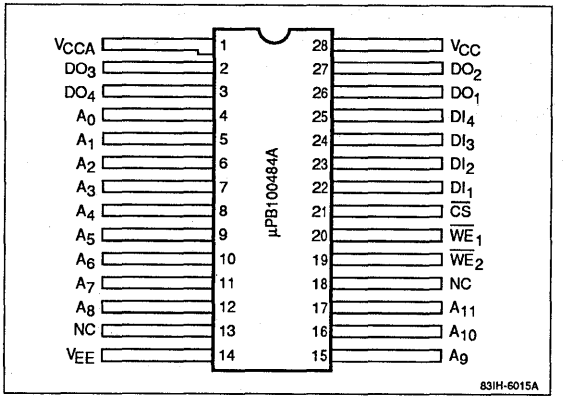
Part Number	Access Time (max)	Supply current (min)	Package
μPB100484AB-5	5 ns	−260 mA	28-pin ceramic flatpack
B-7	7 ns	−240 mA	
μPB100484AD-5	5 ns	−260 mA	28-pin cerdip
D-7	7 ns	−240 mA	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write enable (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	– 4.5-volt power supply
NC	No connection

Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	– 7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	– 30 to +0.1 mA
Storage temperature, T_{STG}	– 65 to +150 °C
Under bias, T_{STG} (bias)	– 55 to +125 °C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}		4		pF	
Output capacitance	C_{OUT}		6		pF	

Truth Table

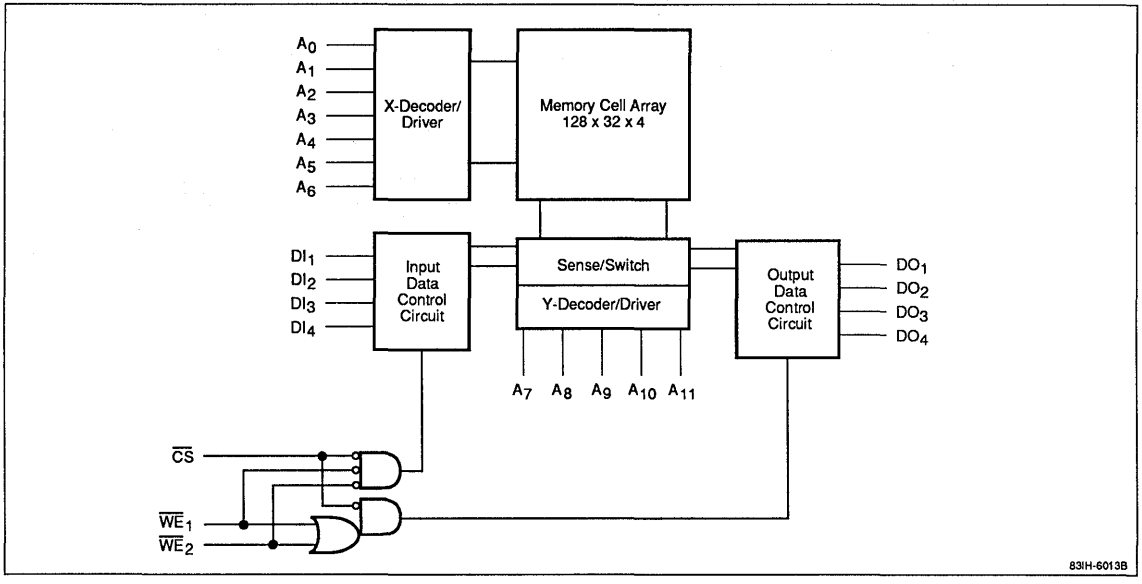
$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L (Note 2)	L	L	Write 0
L	L (Note 2)	H	L	Write 1
L	H (Note 2)	X	D_{OUT}	Read

Notes:

(1) X = don't care.

(2) Both $\overline{WE}_1$ and $\overline{WE}_2$ must be low to initiate write operation. For read operation, either $\overline{WE}_1$ or $\overline{WE}_2$ or both must be high.

Block Diagram



DC Characteristics

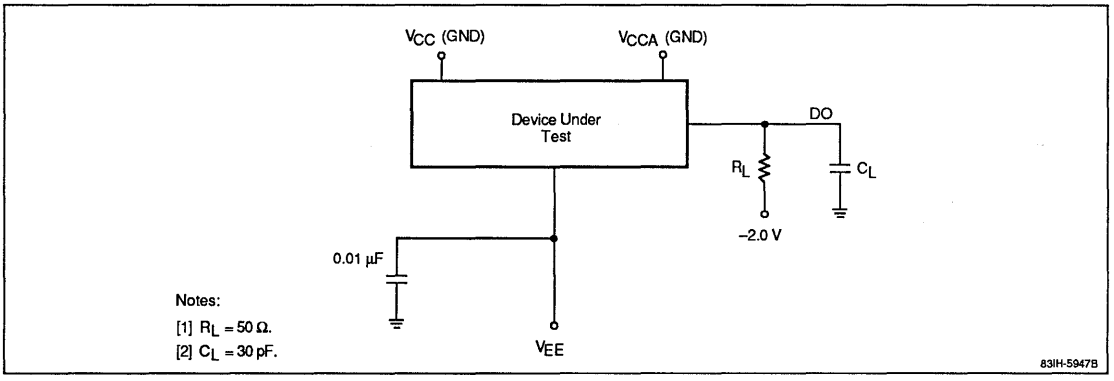
T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50			μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−260			mA	For μPB100484A-5: All inputs and outputs open
		−240			mA	For μPB100484A-7: All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

Figure 1. Loading Conditions Test Circuit



AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ± 5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

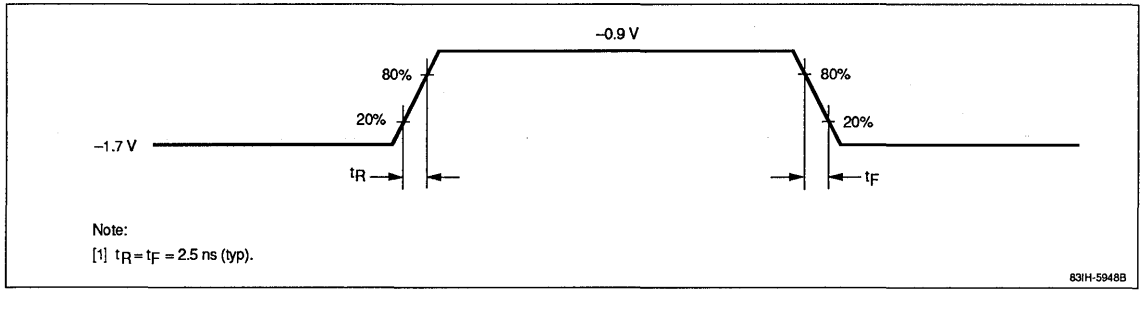
		μPB100484A-5			μPB100484A-7				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Read Operation									
Address access time	t_{AA}			5			7	ns	
Chip select recovery time	t_{RCS}			3.5			4	ns	
Chip select access time	t_{ACS}			3.5			4	ns	
Write Operation									
Write pulse width	t_W	6			8			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			3.5			5	ns	
Write recovery time	t_{WR}			7			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times = 2.5 ns; input and output timing reference levels = 50%.

Figure 2. Input Pulse

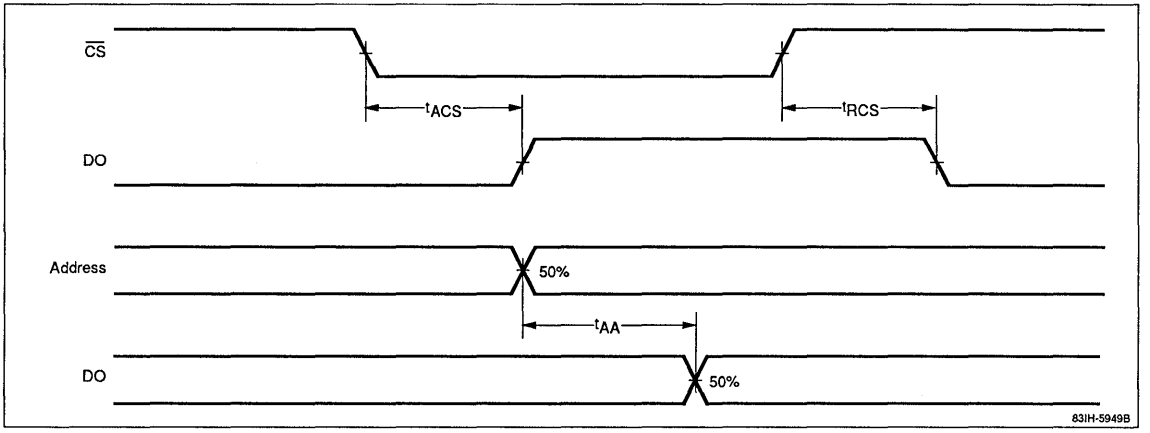


Note:
[1] $t_R = t_F$ = 2.5 ns (typ).

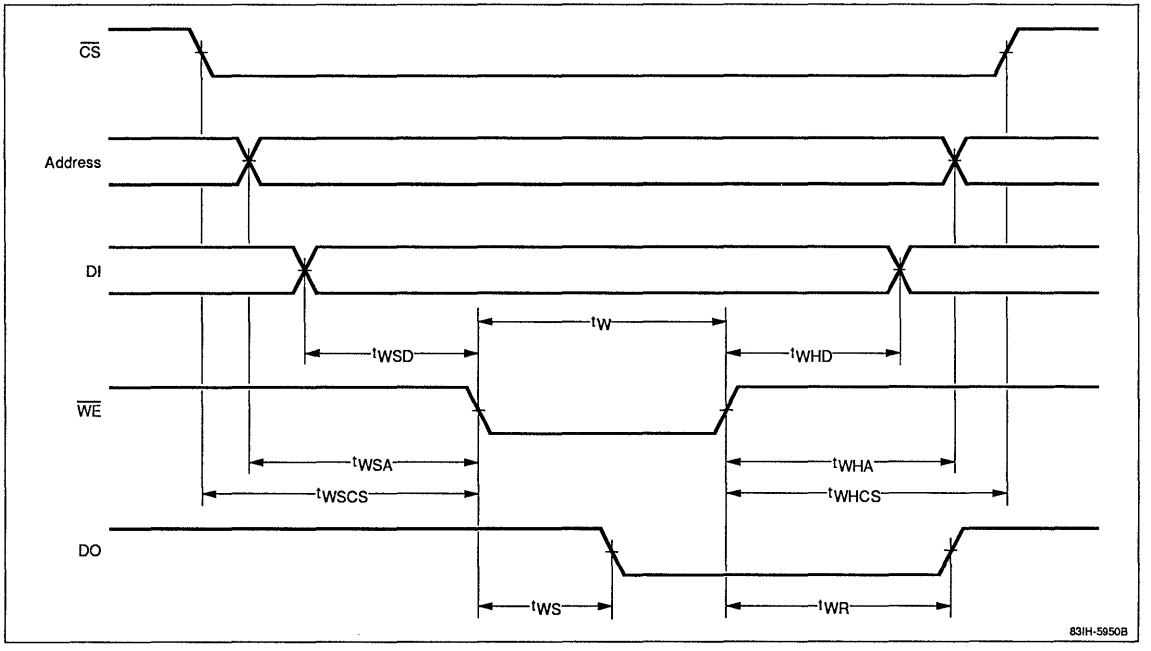
83IH-5948B

Timing Waveforms

Read Cycle



Write Cycle



μPB100A484
4,096 x 4-Bit
100K ECL RAM

Description

The μPB100A484 is a very high-speed 100K interface ECL RAM organized as 4K words by 4 bits and designed with open emitter outputs (noninverted). It is available in 28-pin cerdip or flatpack packages.

Features

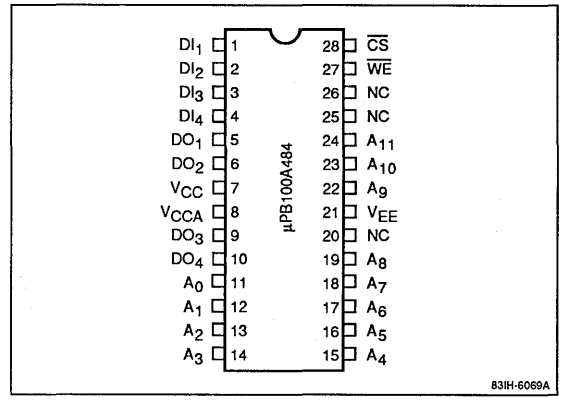
- 4096 word x 4-bit organization
- 100K ECL interface
- Full voltage and temperature compensation
- Open emitter outputs (noninverted)
- Fast access times and low power consumption
- 28-pin cerdip and flatpack packaging
- Center power pins

Ordering Information

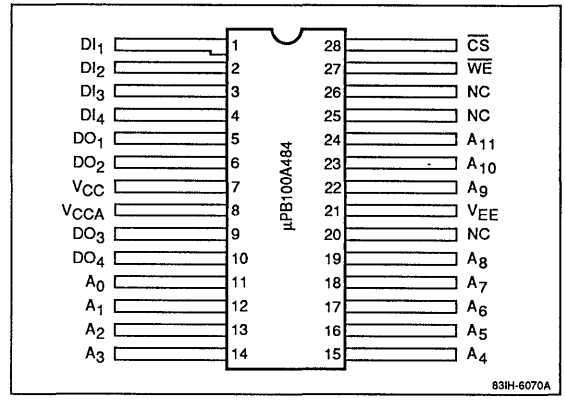
Part Number	Access Time (max)	Supply Current (min)	Package
μPB100A484B-5	5 ns	TBD	28-pin ceramic flatpack
B-7	7 ns	TBD	
μPB100A484D-5	5 ns	TBD	28-pin cerdip
D-7	7 ns	TBD	

Pin Configurations

28-Pin Cerdip



28-Pin Ceramic Flatpack



Pin Identification

Symbol	Function
A_0 - A_{11}	Address inputs
DI_1 - DI_4	Data inputs
DO_1 - DO_4	Data outputs
$\overline{WE}$	Write enable input (active low)
$\overline{CS}$	Chip select (active low)
V_{CC}	Power supply (current switches and bias driver)
V_{CCA}	Power supply (output devices)
V_{EE}	−4.5-volt power supply
NC	No connection

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Function
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

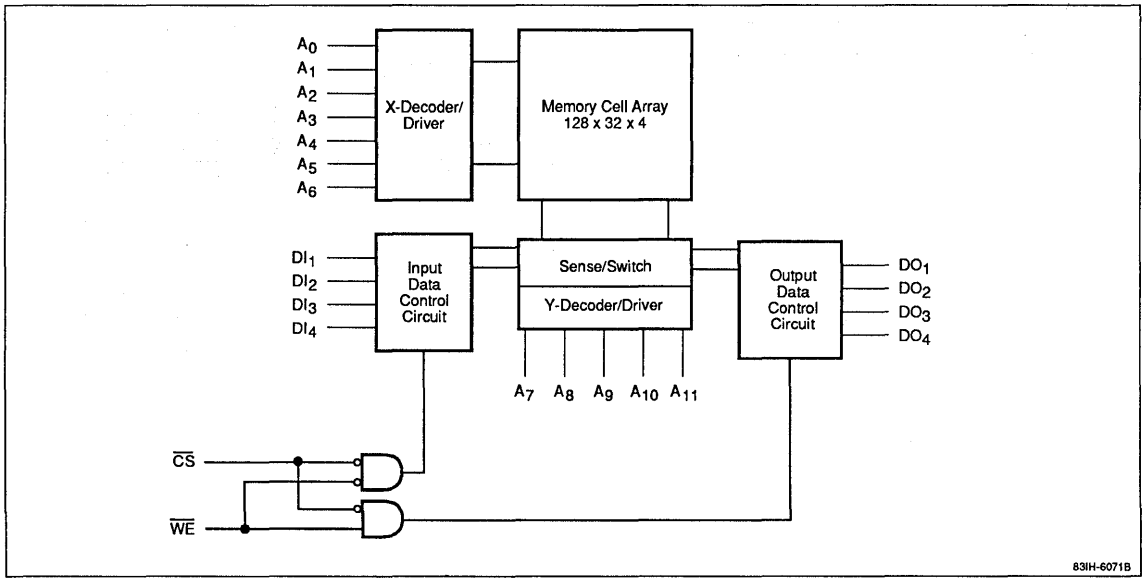
Absolute Maximum Ratings

$V_{CC} = V_{CCA} = 0$ V

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (Bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025		−880	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output voltage, low	V_{OL}	−1810		−1620	mV	V_{IN} = V_{IH} (max) or V_{IL} (min)
Output threshold voltage, high	V_{OHC}	−1035			mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Output threshold voltage, low	V_{OLC}			−1610	mV	V_{IN} = V_{IH} (min) or V_{IL} (max)
Input voltage, high	V_{IH}	−1165		−880	mV	
Input voltage, low	V_{IL}	−1810		−1475	mV	
Input current, high	I_{IH}			220	μA	V_{IN} = V_{IH} (max)
Input current, low	I_{IL}	0.5		170	μA	For $\overline{CS}$: V_{IN} = V_{IL} (min)
		−50			μA	For all others: V_{IN} = V_{IL} (min)
Supply current	I_{EE}	TBD			mA	μPB100A484-5: all inputs and outputs open
		TBD			mA	μPB100A484-7: all inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/sec.

26j

AC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V ±5%; output load = 50 Ω to −2.0 V; V_{CC} = V_{CCA} = 0 V

		μPB100A484-5			μPB100A484-7				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			5			7	ns	
Chip select recovery time	t_{RCS}			3.5			4	ns	
Chip select access time	t_{ACS}			3.5			4	ns	
Write Operation									
Write pulse width	t_W	6			8			ns	
Data setup time	t_{WSD}	1			1			ns	
Data hold time	t_{WHD}	2			2			ns	
Address setup time	t_{WSA}	1			1			ns	
Address hold time	t_{WHA}	2			2			ns	
Chip select setup time	t_{WSCS}	1			1			ns	
Chip select hold time	t_{WHCS}	2			2			ns	
Write disable time	t_{WS}			3.5			5	ns	
Write recovery time	t_{WR}			7			9	ns	
Output Rise and Fall Times									
Output rise time	t_R		2			2		ns	
Output fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) See figures 1 and 2 for loading conditions and input pulse timing. Input pulse levels = −1.7 to −0.9 V; input rise and fall times = 2.5 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

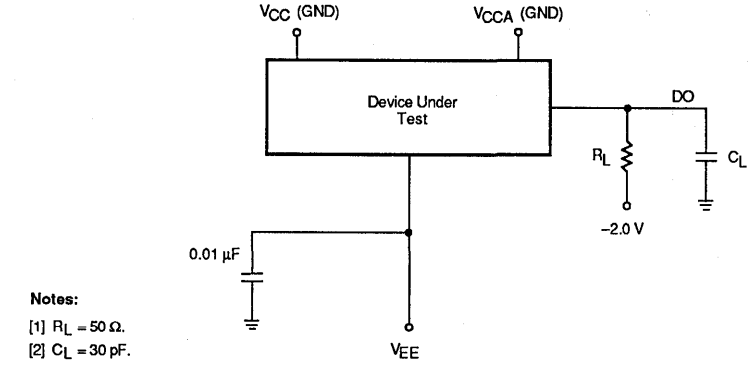
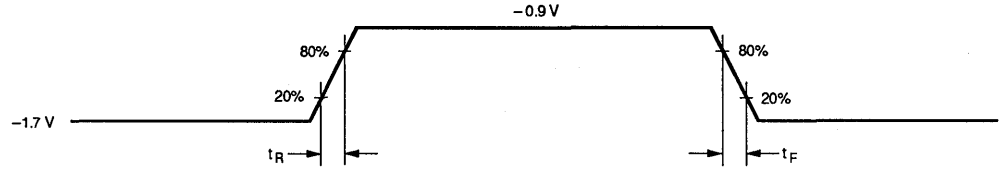
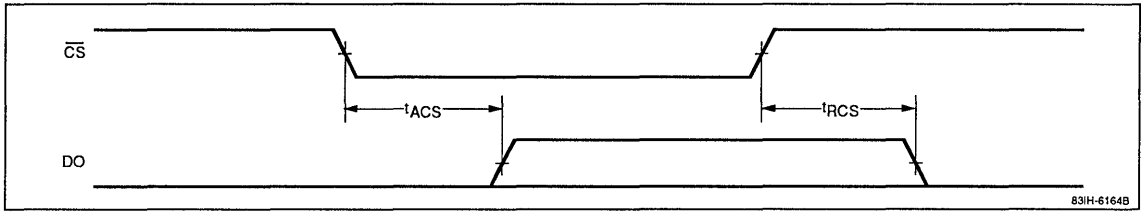


Figure 2. Input Pulse

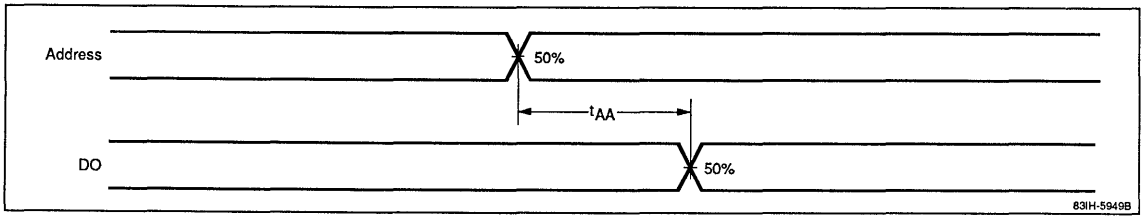


Timing Waveforms

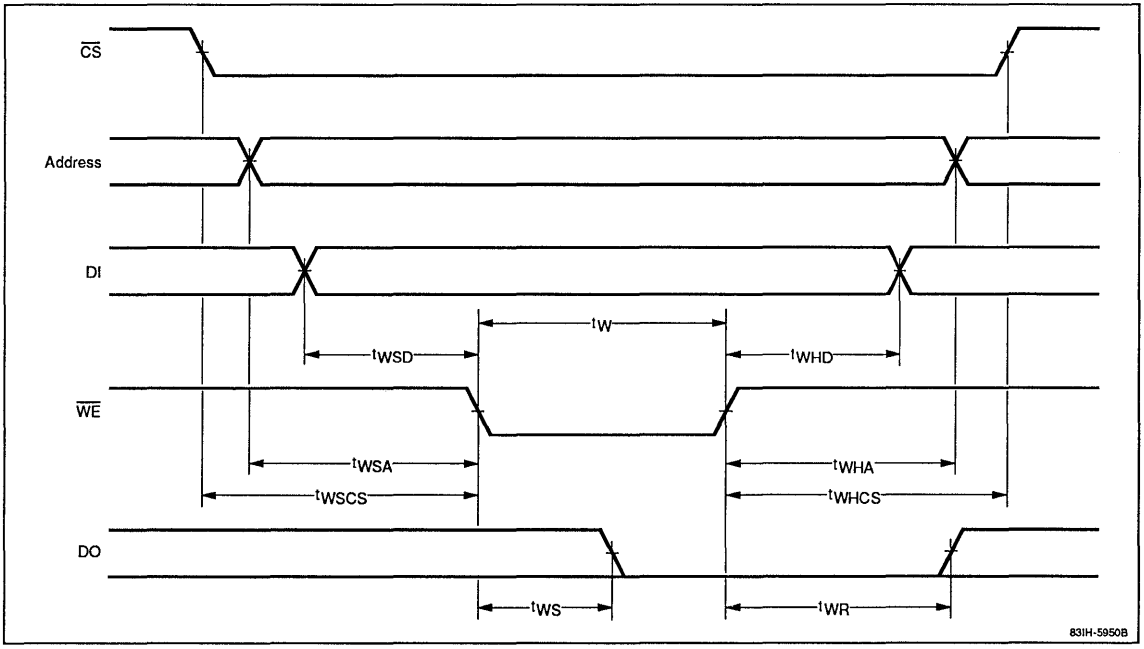
Chip Select Access Cycle



Address Access Cycle



Write Cycle



μPD100500
262,144 x 1-Bit
100K BiCMOS ECL RAM

Description

The μPD100500 is a very high-speed BiCMOS RAM with full voltage and temperature compensation for a 100K ECL interface. Its unique design uses blended CMOS and bipolar peripheral circuits and N-channel MOS memory cells. The device is organized as 262,144 words by 1 bit and designed with an open-emitter output (noninverted) for low power consumption. Two versions with fast access times of 15 and 20 ns maximum are available in hermetic, 300-mil, 24-pin cerdip packaging.

Features

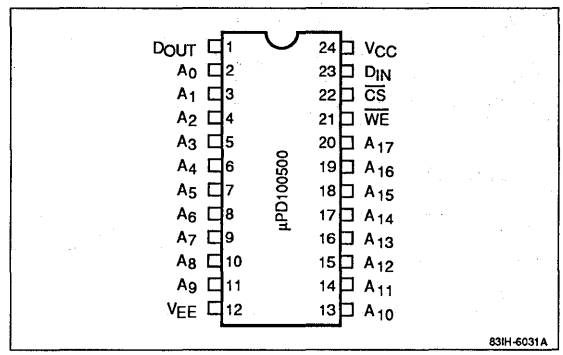
- BiCMOS technology
- 262,144-word x 1-bit organization
- 100K interface ECL with full voltage and temperature compensation
- Noninverted, open-emitter output
- Fast access times of 15 and 20 ns maximum
- Low power consumption
- 300-mil, 24-pin cerdip packaging

Ordering Information

Part Number	Access Time (max)	Power Consumption (max)	Package
μPD100500D-15	15 ns	720 mW	24-pin cerdip
D-20	20 ns		

Pin Configuration

24-Pin Cerdip



Pin Identification

Symbol	Function
A_0 - A_{17}	Address inputs
D_{IN}	Data input
D_{OUT}	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
V_{CC}	Ground
V_{EE}	−4.5-volt power supply

Absolute Maximum Ratings

Supply voltage, V_{EE}	−7.0 to +0.5 V
Input voltage, V_{IN}	V_{EE} to +0.5 V
Output current, I_{OUT}	−30 to +0.1 mA
Storage temperature, T_{STG}	−65 to +150°C
Storage temperature under bias, T_{STG} (bias)	−55 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_{IN}		4		pF
Output capacitance	C_{OUT}		6		pF

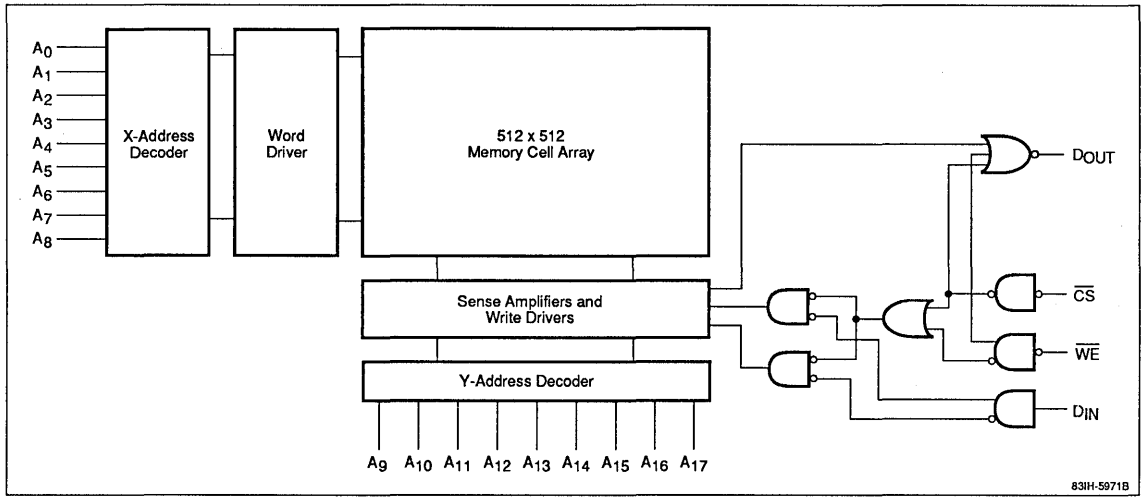
Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	Output	Mode
H	X	X	L	Not selected
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

Notes:

(1) X = don't care.

Block Diagram



DC Characteristics

T_A = 0 to +85°C; V_{EE} = −4.5 V; output load = 50 Ω to −2.0 V; V_{CC} = 0 V

Parameter	Symbol	Min	Max	Unit	Test Conditions
Output voltage, high	V_{OH}	−1025	−880	mV	V_{IN} = V_{IH} max or V_{IL} min
Output voltage, low	V_{OL}	−1810	−1620	mV	V_{IN} = V_{IH} max or V_{IL} min
Output threshold voltage, high	V_{OHC}	−1035		mV	V_{IN} = V_{IH} min or V_{IL} max
Output threshold voltage, low	V_{OLC}		−1610	mV	V_{IN} = V_{IH} min or V_{IL} max
Input voltage, high	V_{IH}	−1165	−880	mV	Guaranteed input voltage high for all inputs
Input voltage, low	V_{IL}	−1810	−1475	mV	Guaranteed input voltage low for all inputs
Input current, high	I_{IH}		220	μA	V_{IN} = V_{IH} max
Input current, low	I_{IL}	0.5	170	μA	For $\overline{CS}$: V_{IN} = V_{IL} min
		−50		μA	For all others: V_{IN} = V_{IL} min
Supply current	I_{EE}	−160		mA	All inputs and outputs open

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

26k

AC Characteristics

T_A = 0 to +85 °C; V_{EE} = −4.5 V ± 5%

		μPD100500-15			μPD100500-20				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Read Operation									
Address access time	t_{AA}			15			20	ns	
Chip select access time	t_{ACS}			10			15	ns	
Chip select recovery time	t_{RCS}			10			15	ns	
Write Operation									
Write pulse width	t_W	10			15			ns	
Data setup time	t_{WSD}	2			3			ns	
Data hold time	t_{WHD}	3			3			ns	
Address setup time	t_{WSA}	2			2			ns	
Address hold time	t_{WHA}	3			3			ns	
Chip select setup time	t_{WSCS}	2			2			ns	
Chip select hold time	t_{WHCS}	3			3			ns	
Write disable time	t_{WS}			10			15	ns	
Write recovery time	t_{WR}			18			23	ns	
Output Rise and Fall Times									
Rise time	t_R		2			2		ns	
Fall time	t_F		2			2		ns	

Notes:

(1) The device under test is mounted in a test socket and is measured at a thermal equilibrium established with a transverse air flow maintained at greater than 2.0 m/s.

(2) Input pulse levels = −1.7 to −0.9 V; input rise and fall times (measured between 20% and 80% or 80% and 20%) = 2.5 ns; input and output timing reference levels = 50%.

Figure 1. Loading Conditions Test Circuit

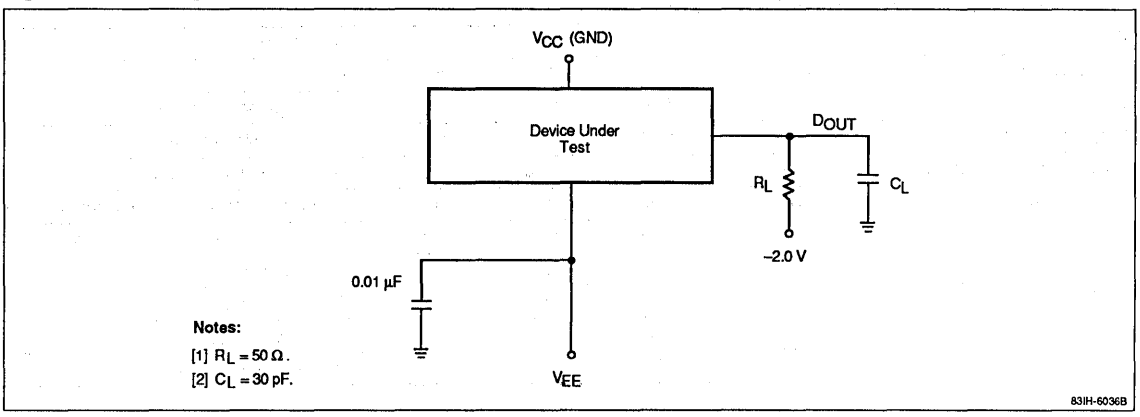
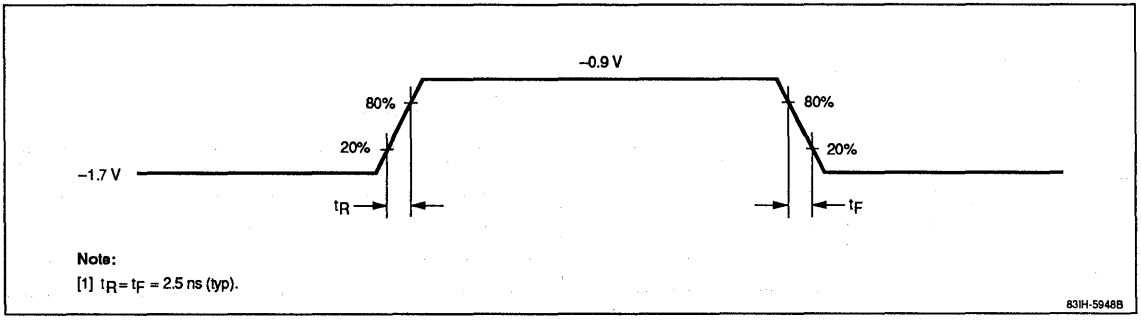
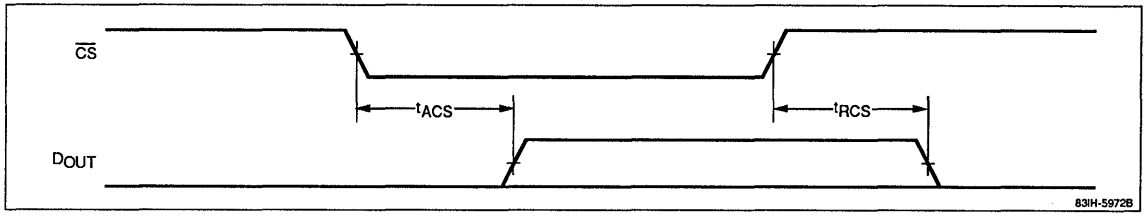


Figure 2. Input Pulse

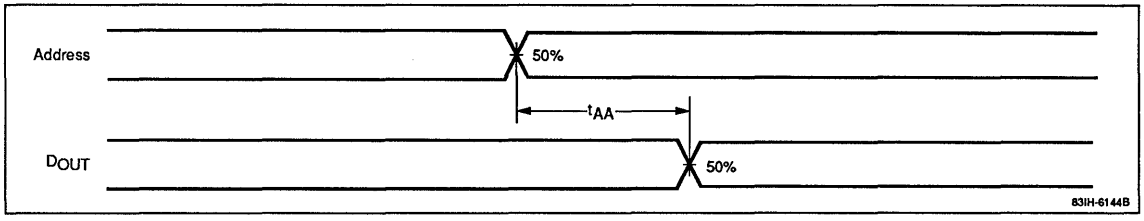


Timing Waveforms

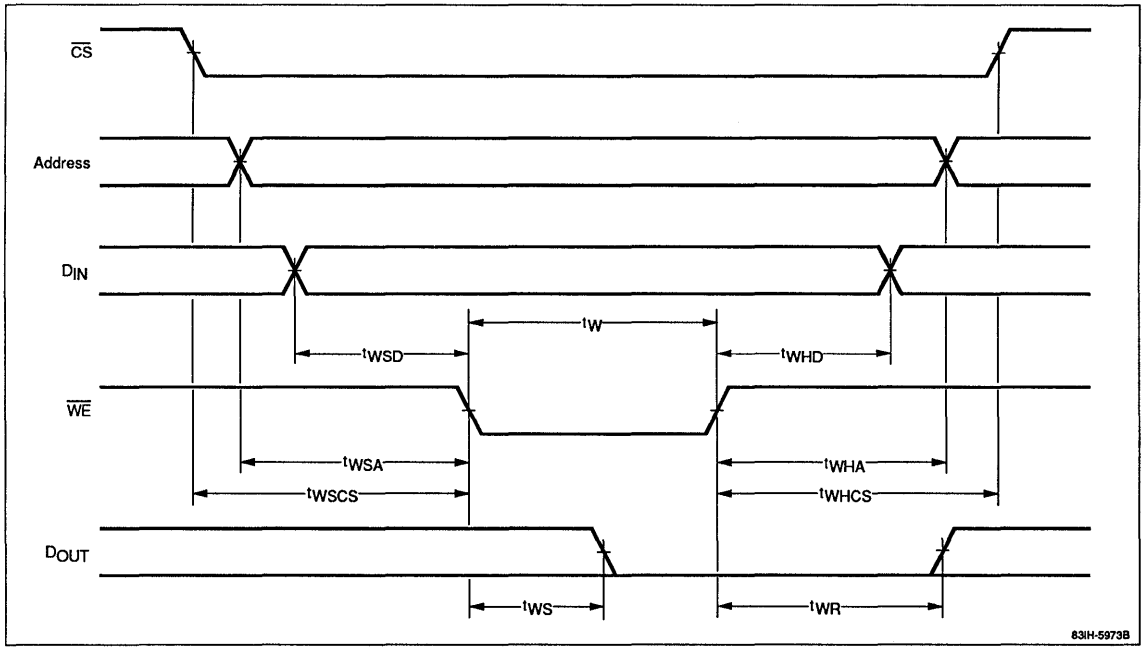
Chip Select Access Cycle



Address Access Cycle



Write Cycle



NEC

Section 27
EEPROMs

μPD	Organization	
28C04	512 x 8	27a
28C05	512 x 8	27b
28C64	8K x 8	27c
28C256	32K x 8	27d

μPD28C04
512 x 8-Bit
CMOS EEPROM

Description

The μPD28C04 is a 4,096-bit electrically erasable and programmable read-only memory (EEPROM) organized as 512 x 8 bits and fabricated with an advanced CMOS process for high performance and low power consumption.

The device operates from a single + 5-volt power supply and provides a $\overline{\text{DATA}}$ polling function to indicate the precise end of write cycles. Additional features include chip erase, auto erase and programming cycles. The μPD28C04 is available in standard 24-pin plastic DIP or miniflat packaging.

Features

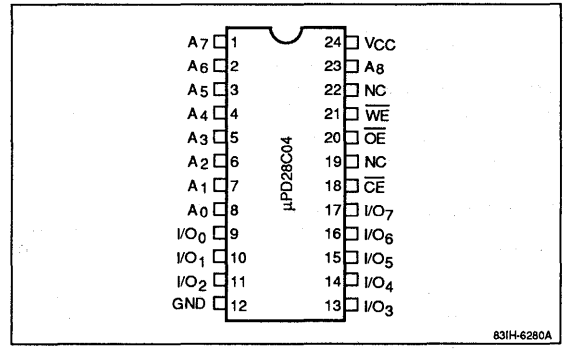
- Fast access times of 200 and 250 ns maximum
- Single + 5-volt power supply
- Chip erase feature
- Auto erase and programming at 10 ms maximum
- $\overline{\text{DATA}}$ polling verification
- Low power dissipation
  - 50 mA max (active)
  - 100 μA max (standby)
- Endurance: 100,000 erase/write cycles per byte
- TTL-compatible inputs and outputs
- Three-state outputs
- Advanced CMOS technology
- 24-pin plastic DIP or miniflat packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C04C-20	200 ns	24-pin plastic DIP
C-25	250 ns	
μPD28C04G-20	200 ns	24-pin plastic miniflat
G-25	250 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
I/O_0 - I/O_7	Data inputs/outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+ 5-volt power supply
NC	No connection

27a

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{I1}	−0.6 to +7.0 V
Input voltage, V_{I3} ($\overline{OE}$)	−0.6 to +16.5 V
Output voltage, V_O	−0.6 to +7.0 V
Operating temperature, T_{OPT}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I		7	12	pF
Output capacitance	C_O			10	pF

Truth Table

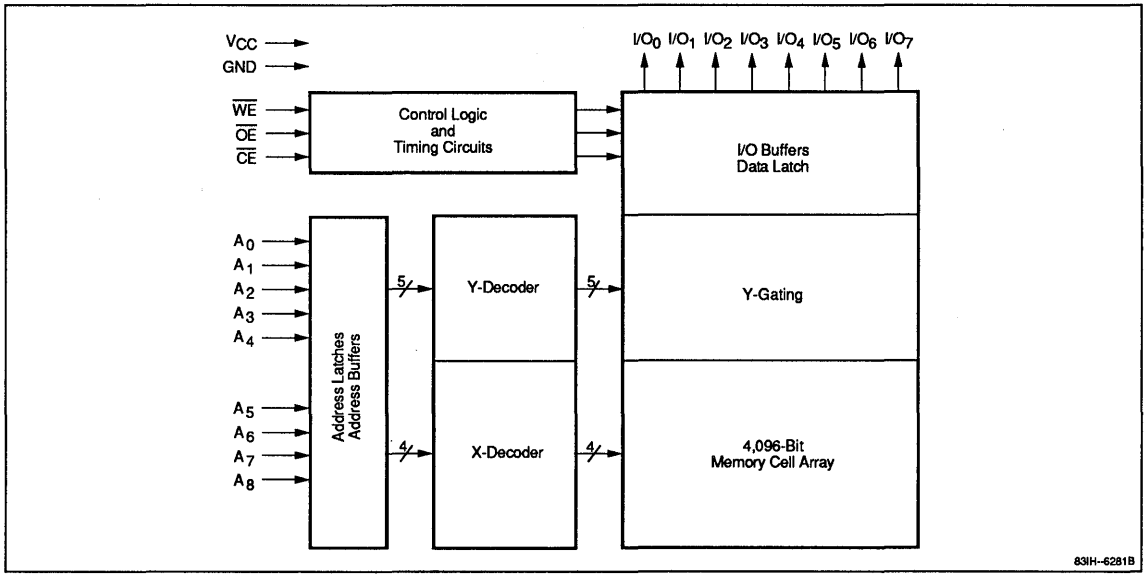
Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	$D_{IN} = V_{IH}$	Active
Write inhibit	X	V_{IL}	X	—	—
	X	X	V_{IH}		

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 ±0.5 V.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}			10	μA	V_{OUT} = 0 to V_{CC}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 to V_{CC}
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

27a

		μPD28C04-20		μPD28C04-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{CE}$ high to output float	t_{DFC}	0	60	0	80	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float	t_{DFO}	0	60	0	80	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
Output hold time from address change	t_{OHA}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{CE}$	t_{OHC}	0		0		ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{OE}$	t_{OHO}	0		0		ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{WE}$ hold time from rising edge of $\overline{OE}$	t_{WHO}	10		10		ns	$\overline{OE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{CE}$	t_{WSC}	10		10		ns	$\overline{CE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{OE}$	t_{WSO}	10		10		ns	$\overline{OE}$ = V_{IH}
Write Operation							
Address hold time	t_{AH}	200		200		ns	
Address setup time	t_{AS}	10		10		ns	
$\overline{CE}$ high after $\overline{CE}$-controlled write cycle	t_{CEH}	9.9		9.9		ms	
Write hold time	t_{CH}	0		0		ns	
Write setup time	t_{CS}	0		0		ns	

AC Characteristics (cont)

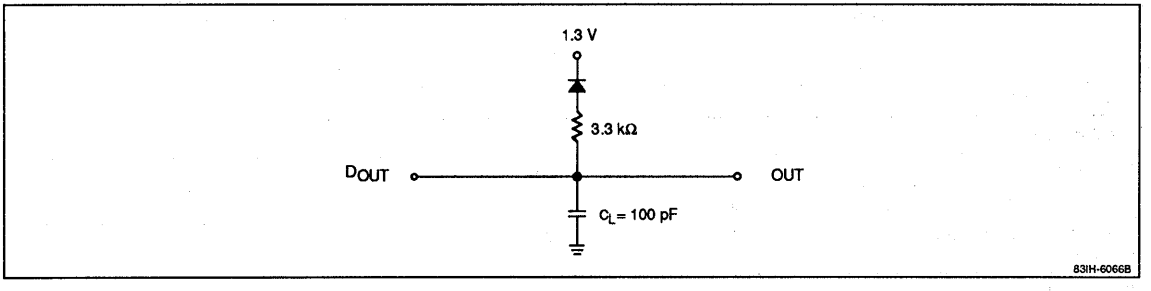
Parameter	Symbol	μPD28C04-20 Min	μPD28C04-20 Max	μPD28C04-25 Min	μPD28C04-25 Max	Unit	Test Conditions
Write Operation (cont)							
$\overline{CE}$ pulse width	t_{CW}	150		150		ns	
Data hold time	t_{DH}	20		20		ns	
Data setup time	t_{DS}	100		100		ns	
Data valid time	t_{DV}		300		300	ns	
$\overline{OE}$ high hold time	t_{OEH}	10		10		ns	
$\overline{OE}$ high setup time	t_{OES}	10		10		ns	
Write cycle time	t_{WC}	10		10		ms	
$\overline{WE}$ high after $\overline{WE}$-controlled write cycle	t_{WEH}	9.9		9.9		ms	
$\overline{WE}$ pulse width	t_{WP}	150		150		ns	
$\overline{WE}$ high hold time	t_{WPH}	50		50		ns	
Chip Erase Operation							
$\overline{CE}$ hold time	t_{ECH}	5		5		μs	
$\overline{CE}$ setup time	t_{ECS}	500		500		ns	
Data hold time	t_{EDH}	100		100		ns	
Data setup time	t_{EDS}	500		500		ns	
$\overline{OE}$ hold time	t_{EOEH}	t_{ECH} + 3		t_{ECH} + 3		μs	
$\overline{OE}$ setup time	t_{EOES}	500		500		ns	
$\overline{WE}$ pulse width	t_{EWP}	10		10		ms	

Notes:

(1) See figure 1 for the output load. Input rise and fall time ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs.

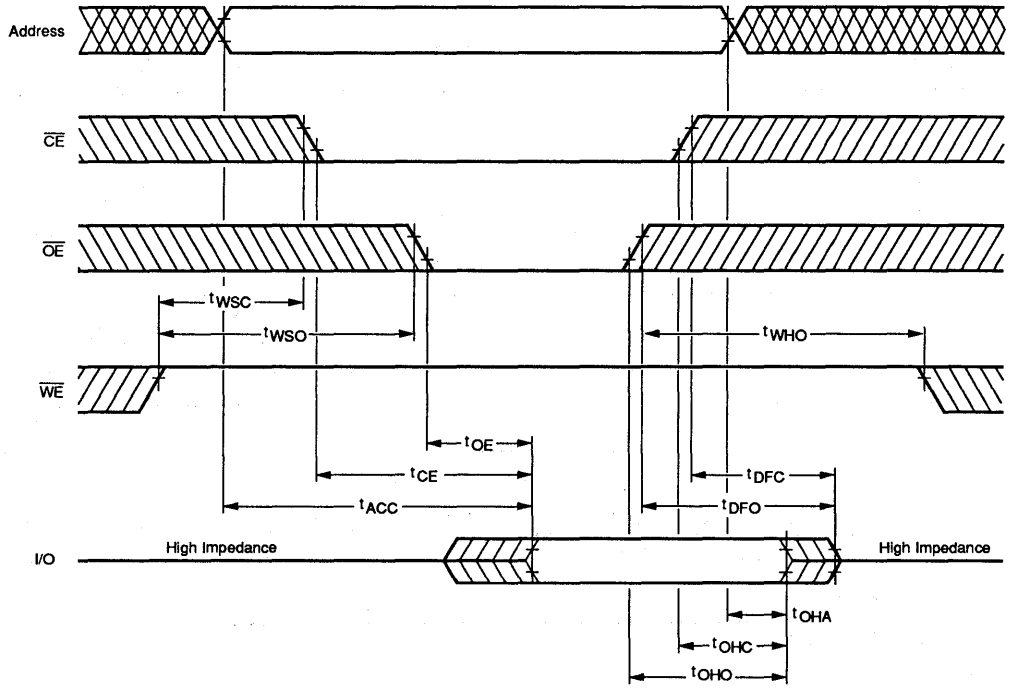
(2) Output hold time is specified from address, $\overline{OE}$ or $\overline{CE}$, whichever goes invalid first.

Figure 1. Output Load



Timing Waveforms

Read Cycle



Notes:

[1] Use t_{DFC} if $\overline{CE}$ transitions to V_{IH} before $\overline{OE}$ transitions to V_{IH}.

[2] Use t_{DFO} if $\overline{OE}$ transitions to V_{IH} before $\overline{CE}$ transitions to V_{IH}.

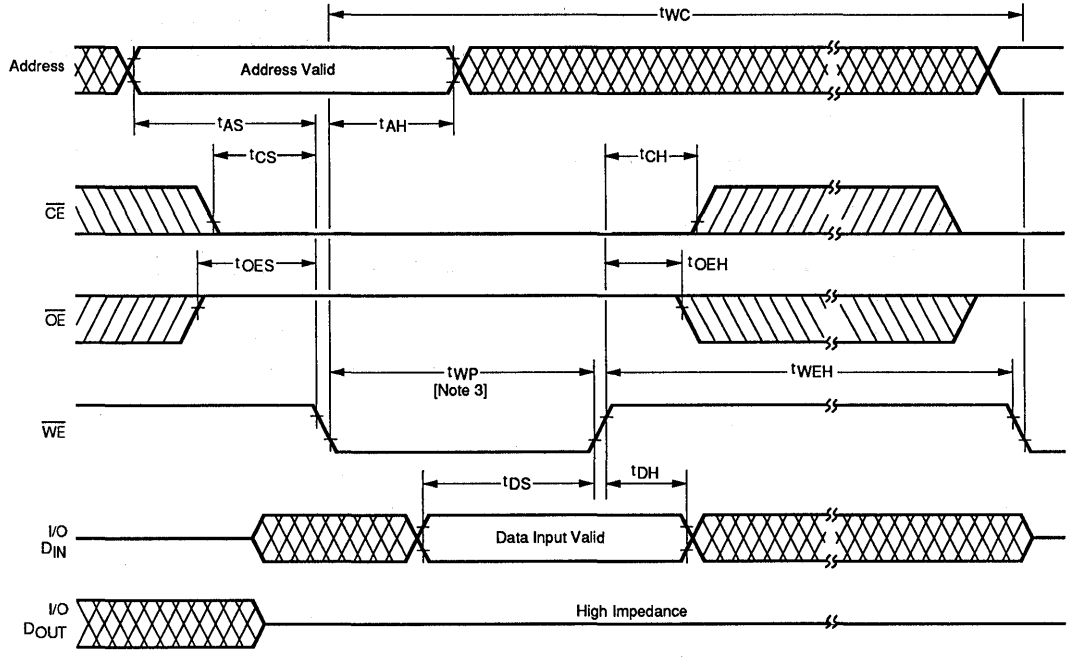
[3] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

83IH-6306B

27a

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

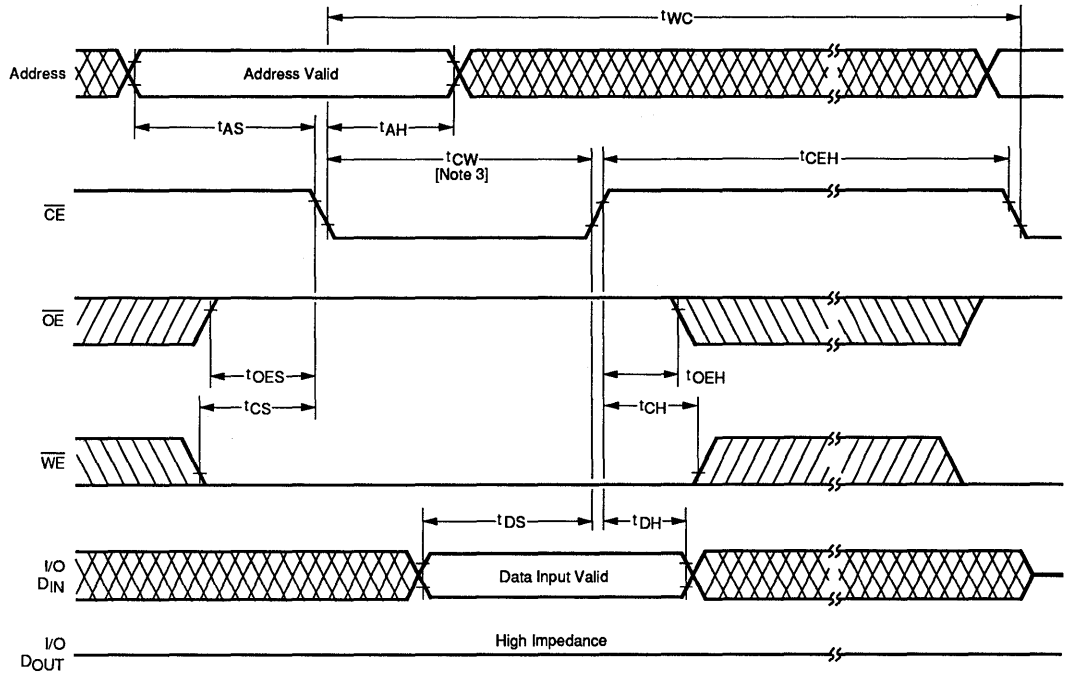
[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{WP} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

83IH-6223B

Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{CW} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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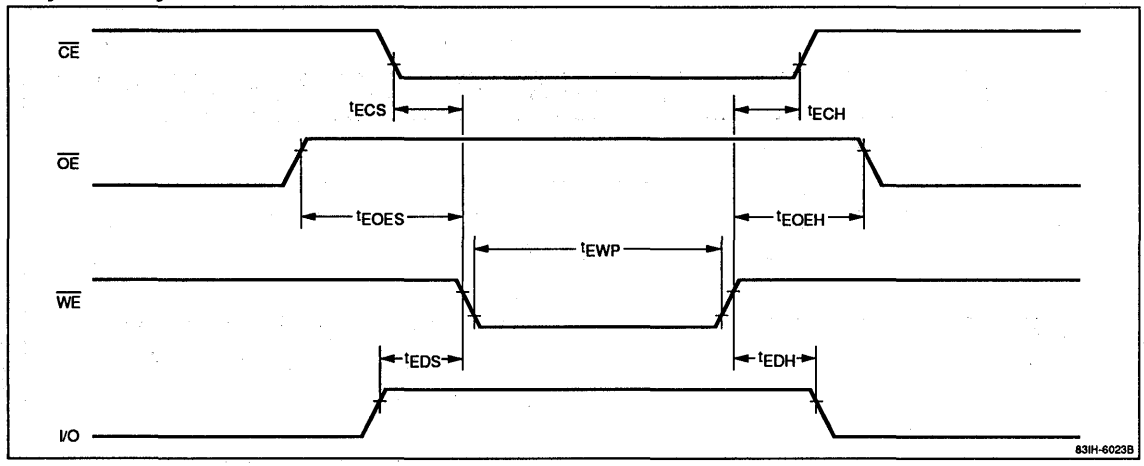
Timing Waveforms (cont)

Chip Erase Cycle



Read Cycle

Both $\overline{CE}$ and $\overline{OE}$ must be at V_{IL} in order to read stored data. While the device is executing read cycles, bringing either of these inputs to V_{IH} will place the outputs in a state of high impedance. This two-line output control allows bus contention to be eliminated in the system application.

Byte Write Cycle

Low levels on $\overline{CE}$ and $\overline{WE}$ and a high level on $\overline{OE}$ place the μPD28C04 in write operation. The write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write cycles begin executing, internal circuits assume all timing control and the byte being addressed is automatically erased and then programmed. The operation is completed within a write cycle time (t_{WC}) of 10 ms.

Chip Erase Cycle

All bytes of the μPD28C04 can be erased simultaneously by making $\overline{CE}$ and $\overline{WE}$ fall to V_{IL} after $\overline{OE}$ has been increased to V_{IHH} (15±0.5 V). The address inputs are "don't care," but the data inputs must all be driven to V_{IH} before the chip erase cycle begins.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write cycles. $\overline{DATA}$ polling can be used to reduce the total programming time of the μPD28C04 to a minimum value, which varies with the system environment.

While internal automatic write cycles are in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7 (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write cycle is complete, a read cycle will result in true data being output on I/O_7.

Write Protection Features

The μPD28C04 provides three features to prevent invalid write cycles:

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- Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less.
- Supply voltage-level detection, where write operation is inhibited when V_{CC} is 2.5 volts or less.
- Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power-on or -off of the V_{CC} supply voltage.

μPD28C05
512 x 8-BIT
CMOS EEPROM

Description

The μPD28C05 is an electrically erasable and programmable read-only memory (EEPROM) organized as 512 words by 8 bits. The device operates from a +5-volt power supply and is fabricated with an advanced CMOS process for high performance and low power consumption.

The device offers an $\overline{ALE}$ pin to control the latching of addresses and a $\overline{DATA}$ polling function to indicate the precise end of write cycles. Additional features include chip erase, auto erase and programming. The μPD28C05 is available in standard 24-pin plastic DIP or miniflat packaging.

Features

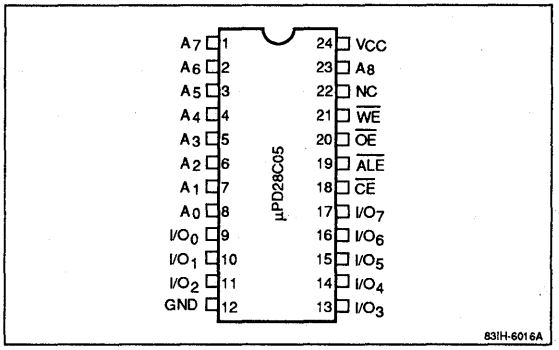
- 512-word by 8-bit organization
- Single +5-volt power supply
- Fast access times of 200 and 250 ns maximum
- Chip erase feature
- Auto erase and programming: 10 ms maximum
- $\overline{DATA}$ polling feature
- Address latching by means of $\overline{ALE}$ pin
- Low power dissipation
  - 50 mA max (active)
  - 100 μA max (standby)
- Endurance: 100,000 erase/write cycles per byte
- TTL-compatible inputs and outputs
- Three-state outputs
- Advanced CMOS technology
- 24-pin plastic DIP or miniflat packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C05C-20	200 ns	24-pin plastic DIP
C-25	250 ns	
μPD28C05G-20	200 ns	24-pin plastic miniflat
G-25	250 ns	

Pin Configuration

24-Pin Plastic DIP or Miniflat



Pin Identification

Symbol	Function
A_0 - A_8	Address inputs
I/O_0 - I/O_7	Data inputs and outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$\overline{ALE}$	Address latch enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{I1}	−0.6 to +7.0 V
Input voltage, V_{I2} ($\overline{OE}$)	−0.6 to +16.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPT}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance	C_I		12	pF
Output capacitance	C_O		10	pF

Truth Table

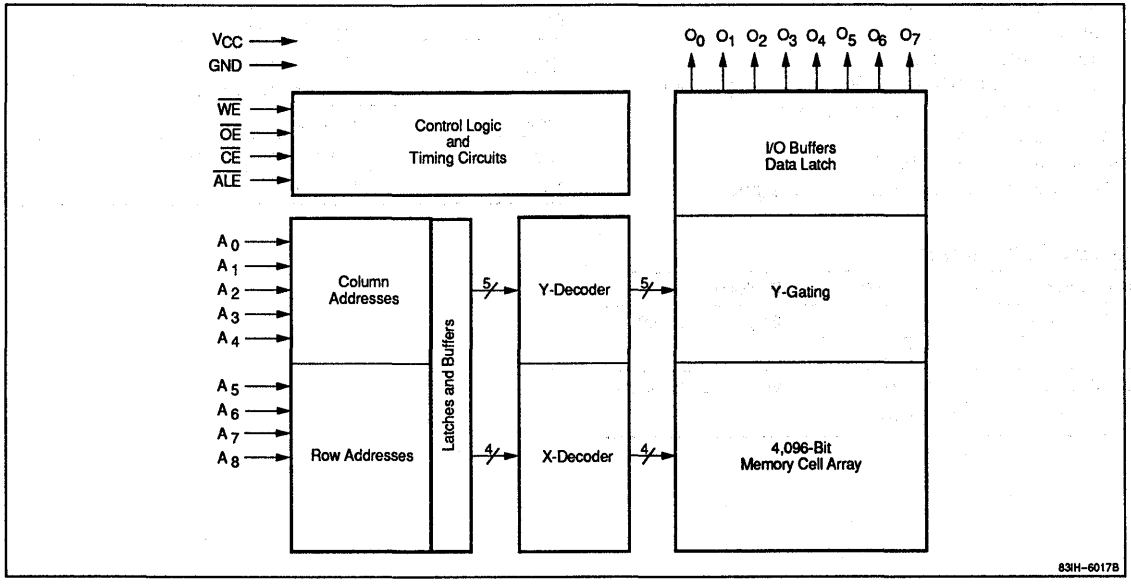
Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{ALE}$	I/O	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	V_{IH}	$D_{IN} = V_{IH}$	Active
Write inhibit	X	V_{IL}	X	X	—	—
	X	X	V_{IH}	X	—	—

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 ±0.5 V.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}			10	μA	V_{OUT} = 0 V to V_{CC} (max)
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC} (max)
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD28C05-20		μPD28C05-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Cycle							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{ALE}$ = $\overline{WE}$ = V_{IH}
Address hold time from $\overline{ALE}$	t_{AHL}	20		30		ns	$\overline{WE}$ = V_{IH}
$\overline{ALE}$ to output delay	t_{ALE}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
Address setup time to $\overline{ALE}$	t_{ASL}	15		20		ns	$\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{CE}$ setup time to $\overline{ALE}$	t_{CSL}	20		20		ns	$\overline{WE}$ = V_{IH}
$\overline{CE}$ high to output float	t_{DFC}	0	60	0	80	ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{OE}$ high to output float	t_{DFO}	0	60	0	80	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{ALE}$ high-level pulse width	t_{LL}	40		40		ns	$\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
Output hold time from address change	t_{OHA}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{ALE}$ = $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{CE}$	t_{OHC}	0		0		ns	$\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{ALE}$	t_{OHL}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; $\overline{WE}$ = V_{IH} (Note 2)
Output hold time from rising edge of $\overline{OE}$	t_{OHO}	0		0		ns	$\overline{CE}$ = V_{IL}; $\overline{WE}$ = V_{IH}
$\overline{WE}$ hold time from rising edge of $\overline{OE}$	t_{WHO}	10		10		ns	$\overline{OE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{CE}$	t_{WSC}	10		10		ns	$\overline{CE}$ = V_{IH}
$\overline{WE}$ setup time to $\overline{OE}$	t_{WSO}	10		10		ns	$\overline{OE}$ = V_{IH}

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AC Characteristics (cont)

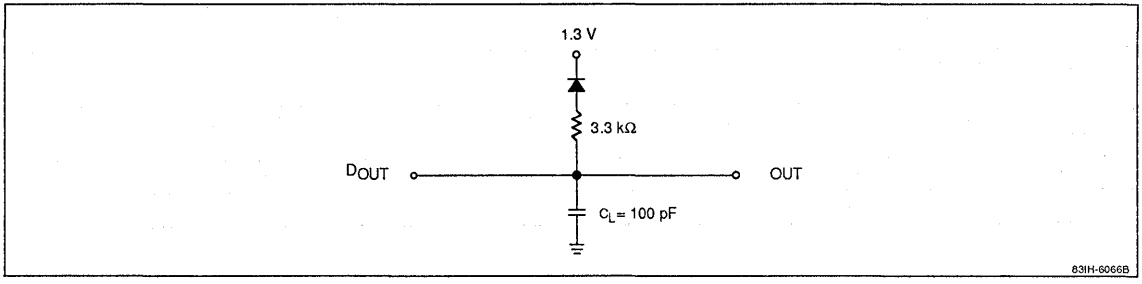
Parameter	Symbol	μPD28C05-20 Min	μPD28C05-20 Max	μPD28C05-25 Min	μPD28C05-25 Max	Unit	Test Conditions
Write Cycle							
Address hold time from $\overline{WE}$	t_{AH}	200		200		ns	
Address setup time to $\overline{WE}$	t_{AS}	10		10		ns	
$\overline{CE}$ high after $\overline{CE}$-controlled write cycle	t_{CEH}	9.9		9.9		ms	
$\overline{CE}$ hold time from $\overline{WE}$ high	t_{CH}	0		0		ns	
$\overline{CE}$ setup time to $\overline{WE}$	t_{CS}	0		0		ns	
$\overline{CE}$ pulse width	t_{CW}	150		150		ns	
Data hold time	t_{DH}	20		20		ns	
Data setup time	t_{DS}	100		100		ns	
$\overline{OE}$ high hold time	t_{OEH}	10		10		ns	
$\overline{OE}$ high setup time	t_{OES}	10		10		ns	
Write cycle time	t_{WC}	10		10		ms	
$\overline{WE}$ high after $\overline{WE}$-controlled write cycle	t_{WEH}	9.9		9.9		ms	
$\overline{WE}$ pulse width	t_{WP}	150		150		ns	
Chip Erase Cycle							
$\overline{CE}$ hold time	t_{ECH}	5		5		μs	
$\overline{CE}$ setup time	t_{ECS}	500		500		ns	
Data hold time	t_{EDH}	100		100		ns	
Data setup time	t_{EDS}	500		500		ns	
$\overline{OE}$ hold time	t_{EOEH}	t_{ECH} + 3		t_{ECH} + 3		μs	
$\overline{OE}$ setup time	t_{EOES}	500		500		ns	
$\overline{WE}$ pulse width	t_{EWP}	10		10		ms	

Notes:

(1) Input rise and fall time ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs. See figure 1 for output load.

(2) Output hold time is specified either from the address, or from the $\overline{ALE}$, $\overline{OE}$ or $\overline{CE}$ pins, whichever goes invalid first.

Figure 1. Output Load



Read Cycles

$\overline{CE}$ and $\overline{OE}$ must both be at V_{IL} for read cycles to be executed. If either of these inputs rise to V_{IH} while the device is reading stored data, the outputs will be placed in a state of high impedance. This two-line output control eliminates bus contention in the system application.

Byte Write Cycles

Low logic levels on $\overline{CE}$ and $\overline{WE}$ and high logic levels on $\overline{OE}$ and $\overline{ALE}$ place the μPD28C05 in write operation. The write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write operation has begun, the internal circuitry assumes all timing control and the byte being addressed in automatically erased and then programmed. The operation completes within the write cycle time (t_{WC}) of 10 ms.

Chip Erase Cycles

All bytes of the μPD28C05 can be erased simultaneously by making $\overline{CE}$ and $\overline{WE}$ fall to V_{IL} and $\overline{ALE}$ rise to V_{IH} after $\overline{OE}$ has been increased to V_{IHH} (+15 ± 0.5 V). The address inputs are "don't care," but the data inputs must all be driven to V_{IH} before the chip erase cycle begins.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write cycles and can be used to reduce the total programming time of the μPD28C05 to a minimum value, which varies with the system environment.

While internal automatic write cycles are being executed, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7. For example, if write data = 1xxx xxxx, then read data = 0xxx xxxx. Once write cycles have finished executing, the execution of a subsequent read cycle will result in true data being output on I/O_7.

Write Protection Features

Three features protect against invalid write cycles:

— Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less;

— Supply voltage-level detection, where write operation is inhibited when V_{CC} is 2.5 volts or less; and

— Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power-on or off of the V_{CC} supply voltage.

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Truth Table

Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{ALE}$	I/O_0 - I/O_7	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	V_{IH}	$D_{IN} = V_{IH}$	Active
Write inhibit	X	V_{IL}	X	X	—	—
	X	X	V_{IH}	X		

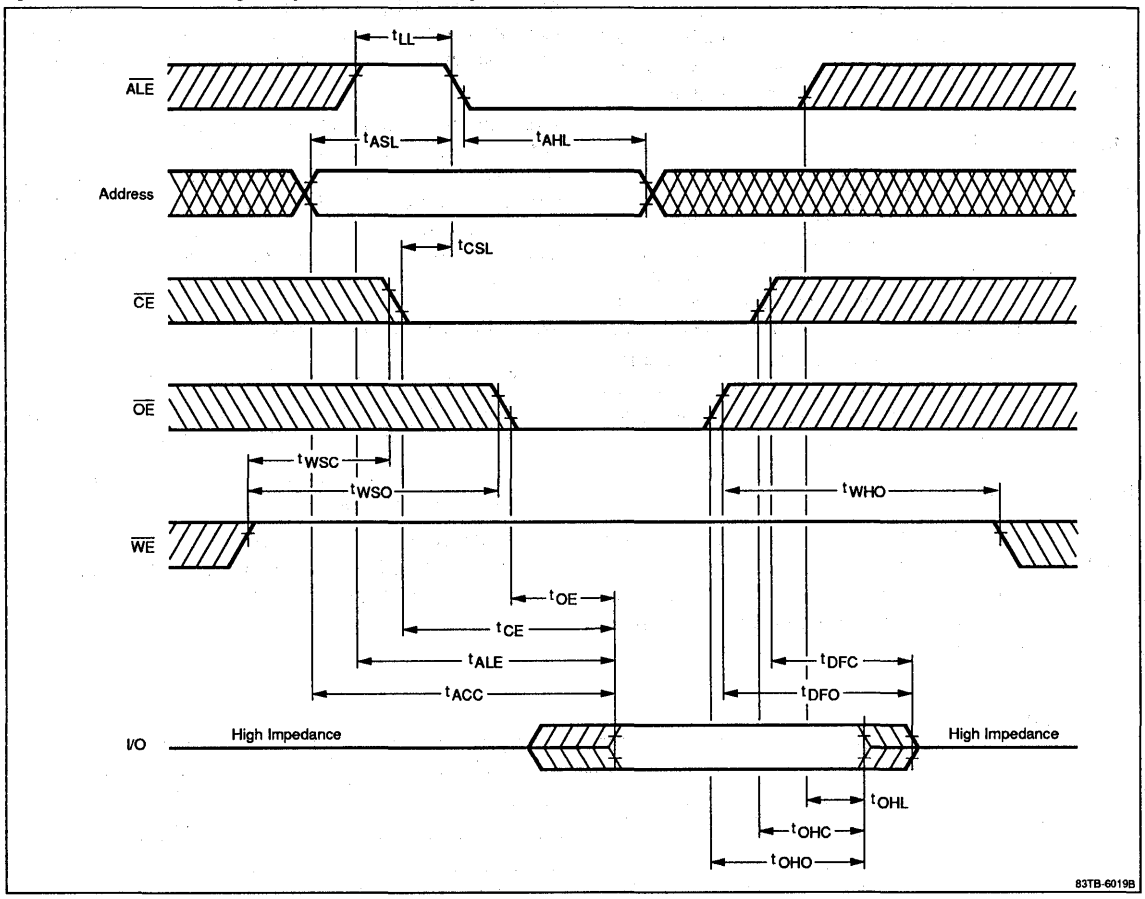
Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 ± 0.5 V.

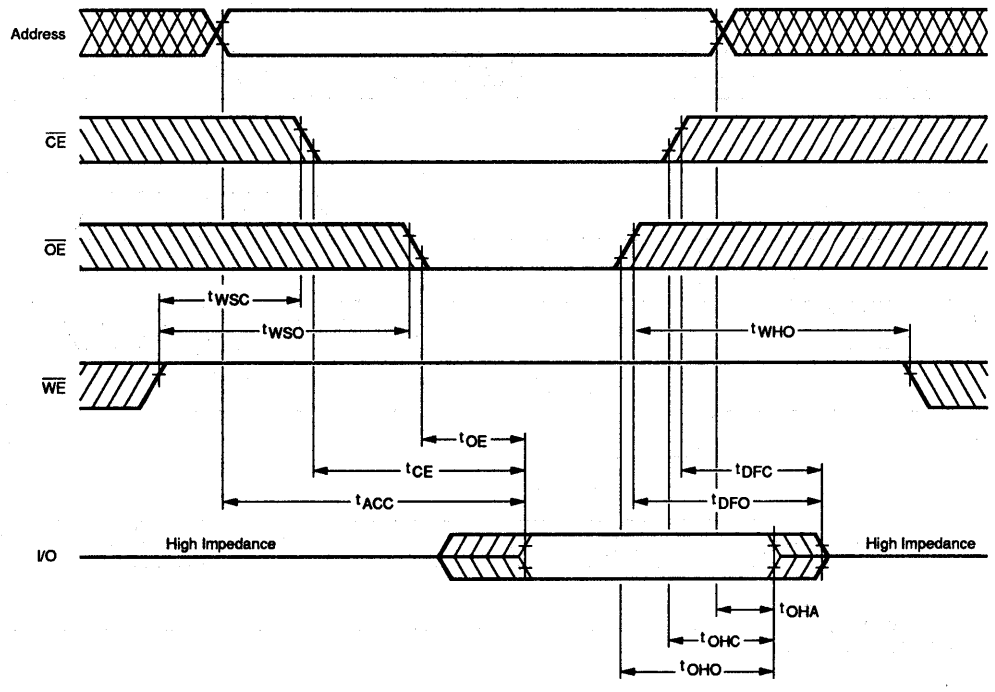
Timing Waveforms

Synchronous Read Cycle ($\overline{ALE}$-Controlled)



Timing Waveforms (cont)

Asynchronous Read Cycle



Note:

[1] $\overline{ALE} = V_{IH}$.

[2] Use t_{DFC} if $\overline{CE}$ transitions to V_{IH} before $\overline{OE}$ transitions to V_{IH}.

[3] Use t_{DFO} if $\overline{OE}$ transitions to V_{IH} before $\overline{CE}$ transitions to V_{IH}.

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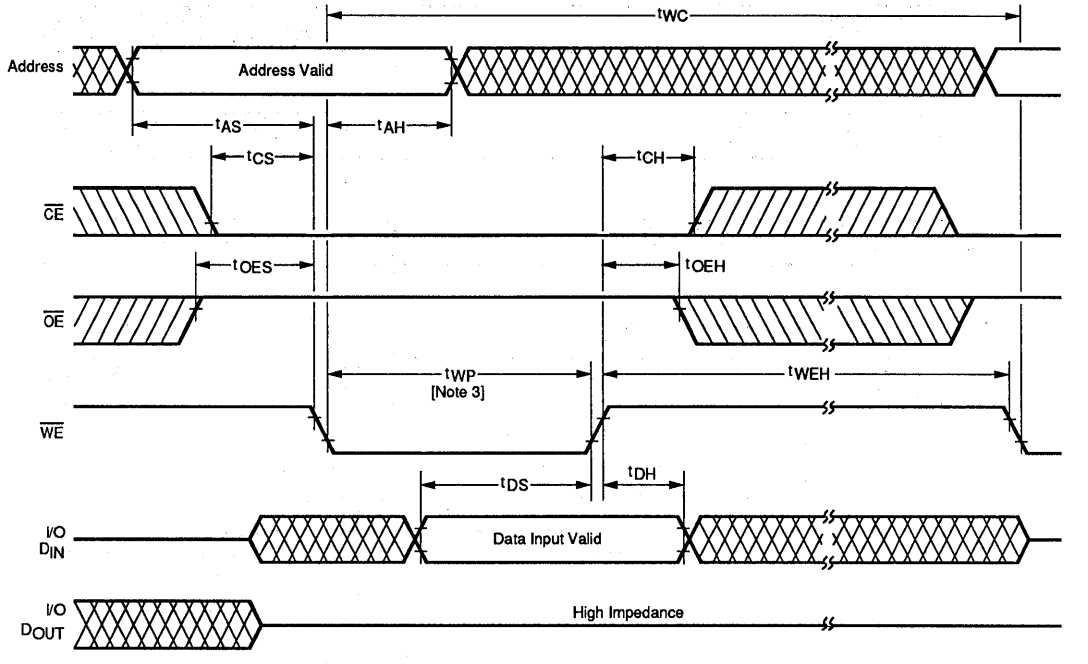
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{WP} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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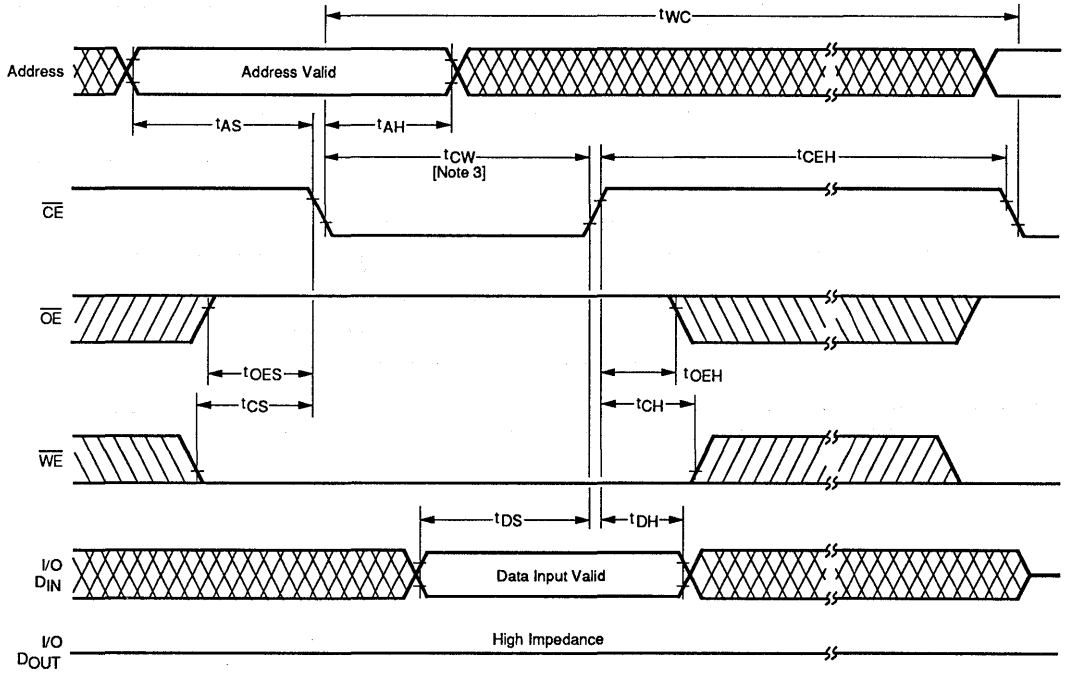
Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameter t_{CW} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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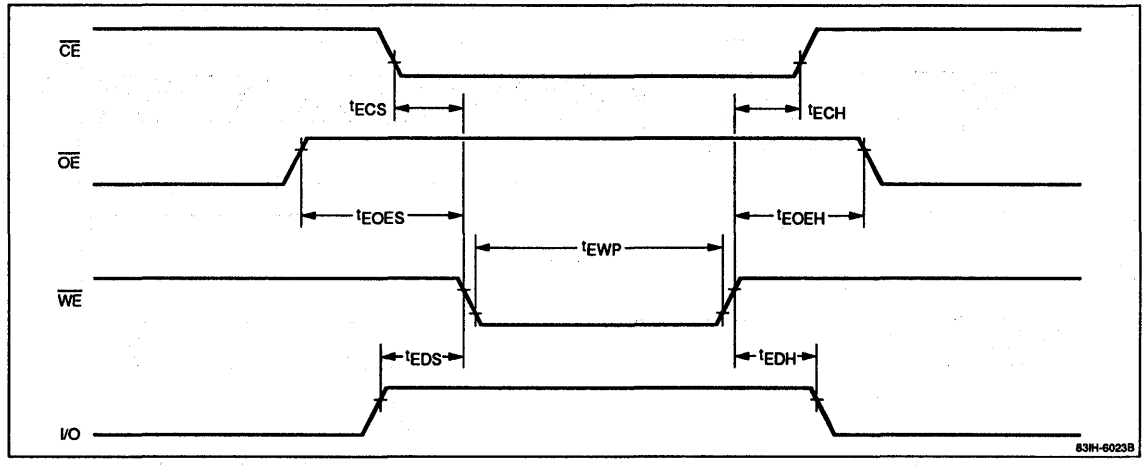
Timing Waveforms (cont)

Chip Erase Cycle



μPD28C64
8192 x 8-Bit
CMOS EEPROM

Description

The μPD28C64 is a 65,536-bit electrically erasable and programmable read-only memory (EEPROM) organized as 8,192 x 8 bits and fabricated with an advanced CMOS process for high performance and low power consumption.

Operating from a single +5-volt power supply, the μPD28C64 provides $\overline{\text{DATA}}$ polling function to indicate the precise end of write cycles. Additional features include chip erase, auto erase and programming, and 32-byte page write cycles.

The μPD28C64 is available in standard 28-pin plastic DIP.

Features

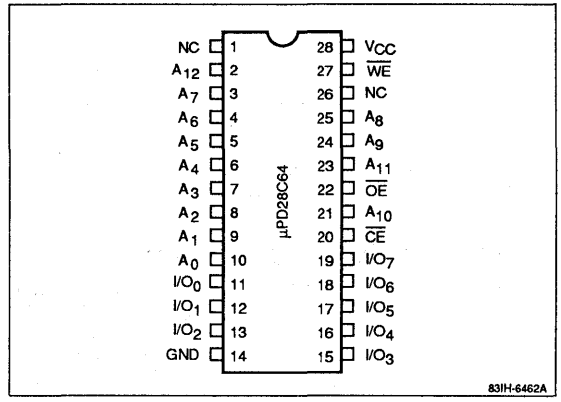
- 8,192 x 8-bit organization
- Single +5-volt power supply
- Chip erase cycles
- Auto erase and programming at 10 ms max
- 32-byte page programming cycles
- $\overline{\text{DATA}}$ polling verification
- Low power dissipation
  - 50 mA max (active)
  - 100 μA max (standby)
- Endurance: 100,000 erase/write cycles per byte
- Silicon signature
- TTL-compatible inputs and outputs
- Three-state outputs
- Advanced CMOS technology
- 28-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C64C-20	200 ns	28-pin plastic DIP
C-25	250 ns	

Pin Configuration

28-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{12}	Address inputs
I/O_0 - I/O_7	Data inputs and outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to +7.0 V
Input voltage, A_9	−0.6 to +13.5 V
$\overline{OE}$	−0.6 to +16.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			12	pF
Output capacitance	C_O			10	pF

Truth Table

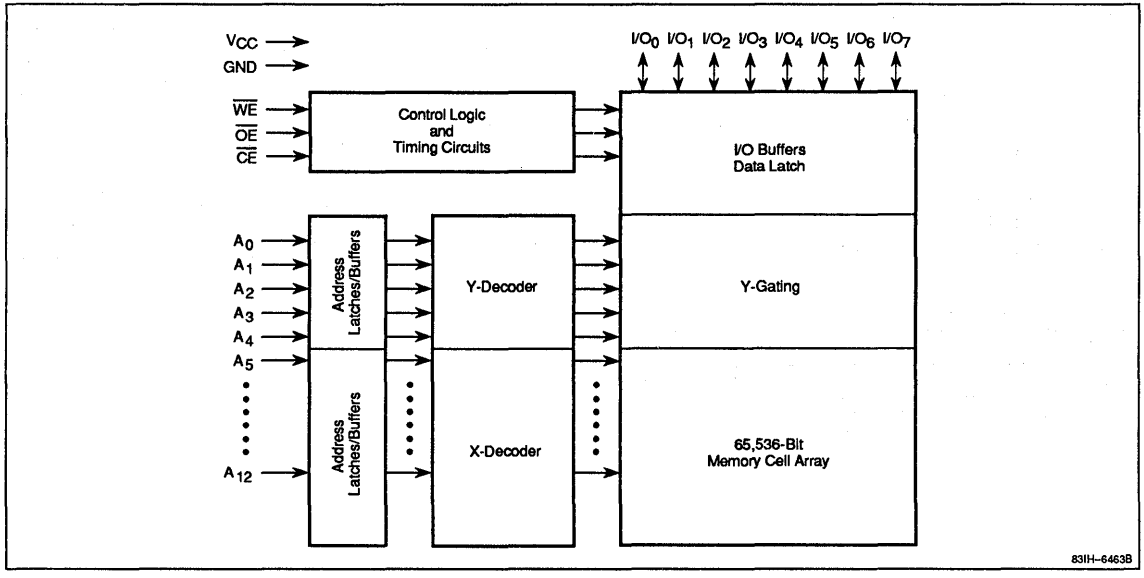
Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active
Chip erase	V_{IL}	V_{IHH}	V_{IL}	$D_{IN} = V_{IH}$	Active
Write Inhibit	X	V_{IL}	X	—	—
	X	X	V_{IH}		

Notes:

(1) X can be either V_{IL} or V_{IH}.

(2) V_{IHH} = +15 V ±0.5.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}			10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CE}$ or $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 V to V_{CC}
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

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AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

		μPD28C64-20		μPD28C64-25			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Read Operation							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}	0	60	0	80	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}
Output hold from address, $\overline{OE}$ or $\overline{CE}$, whichever transition occurs first	t_{OH}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Write Operation						
Address hold time	t_{AH}	200			ns	
Address setup time	t_{AS}	10			ns	
Write hold time	t_{CH}	0			ns	
Write setup time	t_{CS}	0			ns	
$\overline{CE}$ pulse width	t_{CW}	150			ns	
$\overline{OE}$ high hold time	t_{OEH}	10			ns	
$\overline{OE}$ high setup time	t_{OES}	10			ns	
Write cycle time	t_{WC}	10			ms	
$\overline{WE}$ pulse width	t_{WP}	150			ns	
$\overline{WE}$ high hold time	t_{WPH}	50			ns	

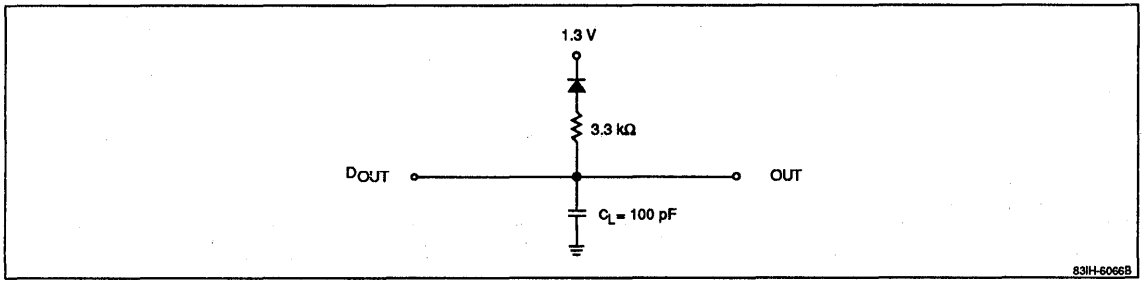
AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Write Operation						
Byte load cycle time	t_{BLC}	3		100	μs	
Data hold time	t_{DH}	20			ns	
Data setup time	t_{DS}	100			ns	
Data valid time	t_{DV}			300	ns	
Chip Erase Operation						
$\overline{OE}$ hold time	t_{CEH}	t_{CH} + 3			μs	
$\overline{CE}$ hold time	t_{CH}	5			μs	
$\overline{CE}$ setup time	t_{CS}	500			ns	
Data hold time	t_{DH}	100			ns	
Data setup time	t_{DS}	500			ns	
$\overline{OE}$ setup time	t_{OES}	500			ns	
$\overline{WE}$ pulse width	t_{WP}	10			ms	

Notes:

(1) See figure 1 for the output load. Input rise and fall times ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs.

Figure 1. Output Load



Read Cycles

Both $\overline{CE}$ and $\overline{OE}$ must both be at V_{IL} in order to read stored data. While the device is executing read cycles, bringing either of these inputs to V_{IH} will place the outputs in a state of high impedance. This two-line output control allows bus contention to be eliminated in the system application.

Byte Write Cycles

Low levels on $\overline{CE}$ and $\overline{WE}$ and a high level on $\overline{OE}$ place the μPD28C64 in write operation. Write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. The data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write operation has begun, the internal circuits assume all timing control. The byte being addressed is automatically erased and then programmed. The operation completes within the write cycle time (t_{WC}) of 10 ms.

Page Write Cycle

This option allows the μPD28C64 to be completely programmed in a much shorter time than is required using byte write cycles. The loading of up to 32 bytes of data before internal write cycles program all of these bytes simultaneously allows the μPD28C64 to be completely written in a maximum of 2.6 seconds. The page address is specified by the inputs A_5 through A_{12}; once set, this address cannot be changed during a page write cycle. Within the page, address inputs A_0 through A_4 can be used sequentially or in random order to specify individual bytes.

The beginning of a page write cycle is the same as a $\overline{WE}$-controlled byte write cycle. If the next falling edge of $\overline{WE}$ occurs within a byte load cycle time of 100 μs, the internal byte load register will be loaded with another byte of input data. This cycle can be repeated to load a maximum of 32 bytes of data. At any point in the sequence, if $\overline{WE}$ does not have a new falling edge within the byte load cycle time of 100 μs, byte load operation will terminate and automatic erasing and programming operations will begin.

Chip Erase Cycles

All bytes of the μPD28C64 can be erased simultaneously by making $\overline{CE}$ and $\overline{WE}$ fall to V_{IL} after $\overline{OE}$ has been increased to V_{IHH} (15 V ±0.5). The address inputs are "don't care," but the data inputs must all be driven to V_{IH} before the chip erase cycle begins.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write and page write cycles. $\overline{DATA}$ polling can be used to reduce total programming time of the μPD28C64 to a minimum value, which varies with the system environment.

While internal automatic write operation is in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7 (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write cycle is complete, a read cycle will result in true data being output on I/O_7.

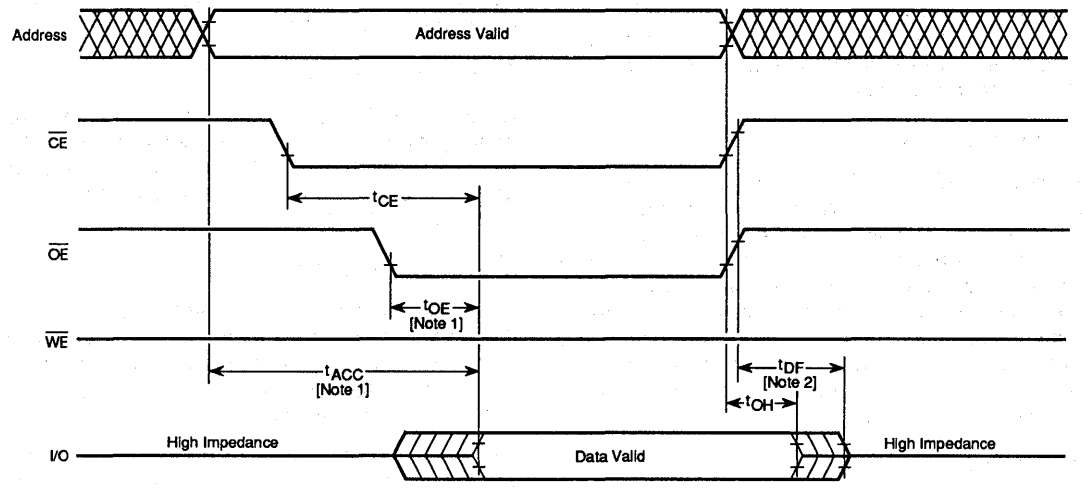
Write Protection Features

The μPD28C64 provides three features to prevent invalid write cycles.

- Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less.
- Supply voltage level detection, where write operation is inhibited when V_{CC} is 2.5 V or less.
- Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power on or off of the V_{CC} supply voltage.

Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$, after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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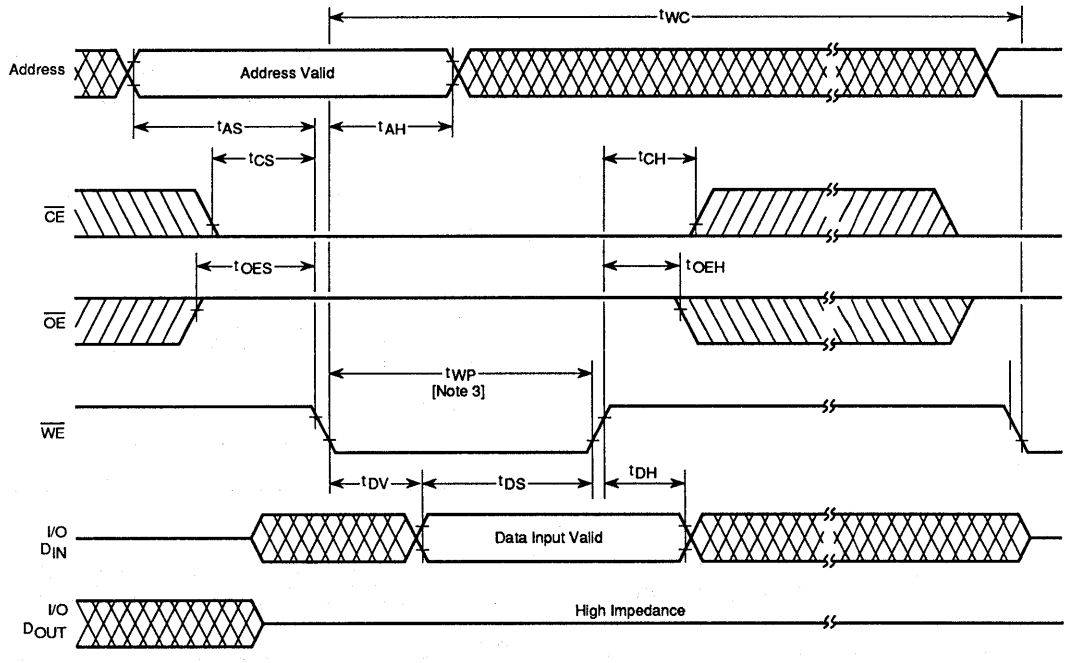
Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

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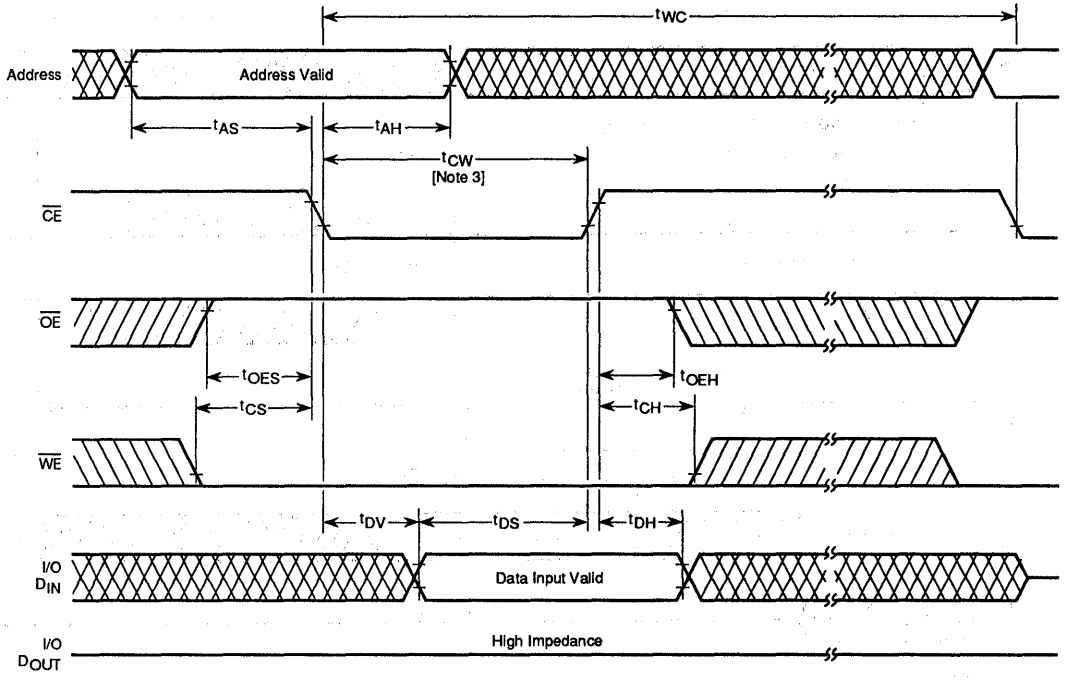
Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} is defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

[4] $\overline{OE}$ may be delayed up to ($t_{ACC} - t_{OE}$) without impacting t_{ACC}.

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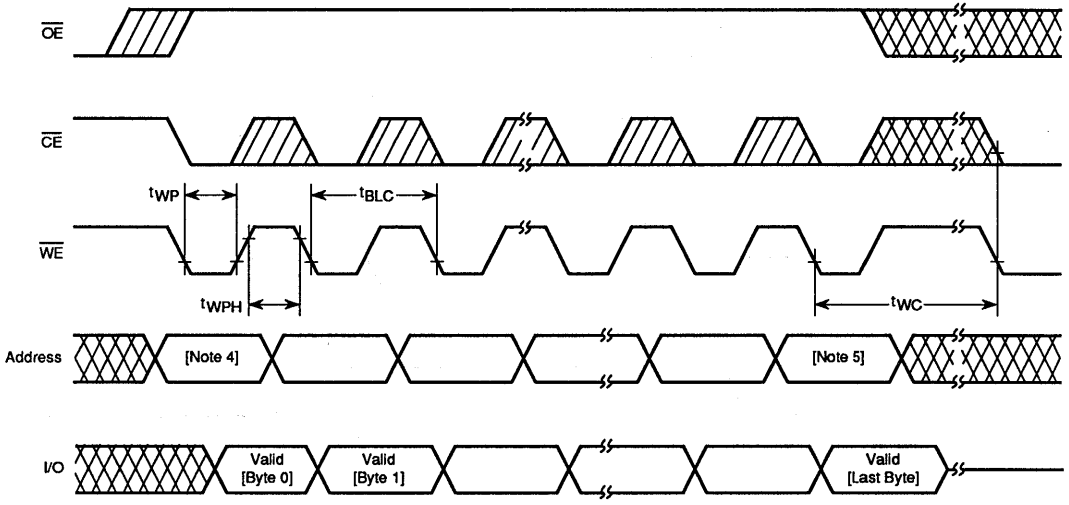
Timing Waveforms (cont)

Page Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

[4] The page cannot be changed in the middle of a page write cycle. Address inputs $A_5 - A_{12}$ must be supplied for every byte load cycle and must remain the same throughout the page write cycle to prevent writing to an unknown address location. Address inputs $A_0 - A_4$ are altered for each byte load cycle and determine the individual byte to be written within the page.

[5] A maximum of 32 bytes may be loaded in a single page write cycle.

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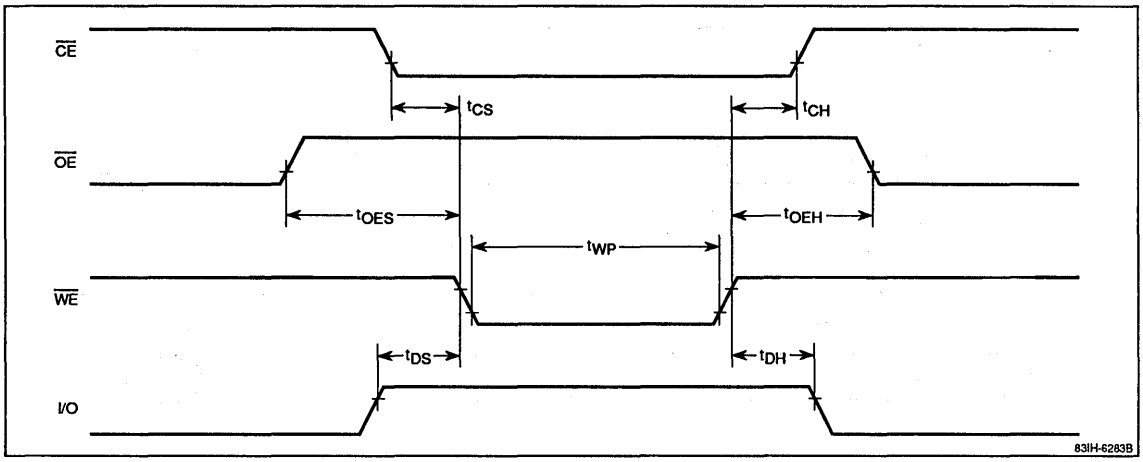
Timing Waveforms (cont)

Chip Erase Cycle



μPD28C256
32,768 x 8-Bit
CMOS EEPROM

Description

The μPD28C256 is a 262,144-bit electrically erasable and programmable read-only memory (EEPROM) organized as 32,768 x 8 bits and fabricated with an advanced CMOS process for high performance and low power consumption.

Operating from a single +5-volt power supply, the μPD28C256 provides $\overline{\text{DATA}}$ polling and toggle bit functions to indicate the precise end of write cycles. Additional features include software data protection, software chip erase, auto erase and programming, and 64-byte page write operation using automatic write timing and internal address and data latches.

The μPD28C256 is available in standard 28-pin plastic DIP packaging.

Features

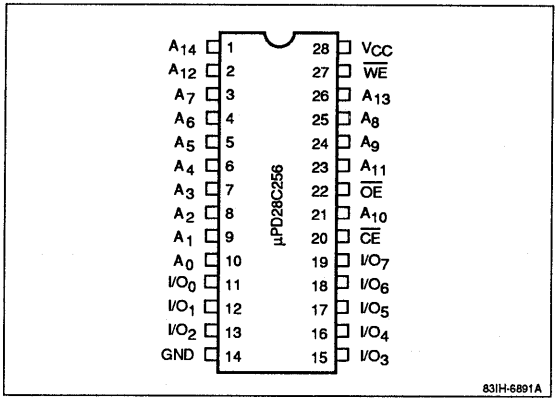
- Single + 5-volt power supply
- Fast access time of 200 ns (max)
- Software chip erase cycles
- Auto erase and programming at 10 ms (max)
- 64-byte page programming cycles
- End of write detection
  - — $\overline{\text{DATA}}$ polling
  - — Toggle bit
- Software data protection
- Low power dissipation
  - — 50 mA max (active)
  - — 100 μA max (standby)
- 10,000 erase/write cycles per byte
- Silicon signature included
- Advanced CMOS technology
- 28-pin plastic DIP packaging

Ordering Information

Part Number	Access Time (max)	Package
μPD28C256CZ-20	200 ns	28-pin plastic DIP
CZ-25	250 ns	

Pin Configuration

28-Pin Plastic DIP



Pin Identification

Symbol	Function
A_0 - A_{14}	Address inputs
I/O_0 - I/O_7	Data inputs and outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply

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Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.6 to +7.0 V
Input voltage, V_{IN}	−0.6 to V_{CC} + 0.3 V
Input voltage (A_9)	−0.6 to +13.5 V
Output voltage, V_{OUT}	−0.6 to +7.0 V
Operating temperature, T_{OPR}	−10 to +85°C
Storage temperature, T_{STG}	−65 to +125°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.0		V_{CC} + 0.3	V
Input voltage, low	V_{IL}	−0.3		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz; V_{IN} and V_{OUT} = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			12	pF
Output capacitance	C_O			10	pF

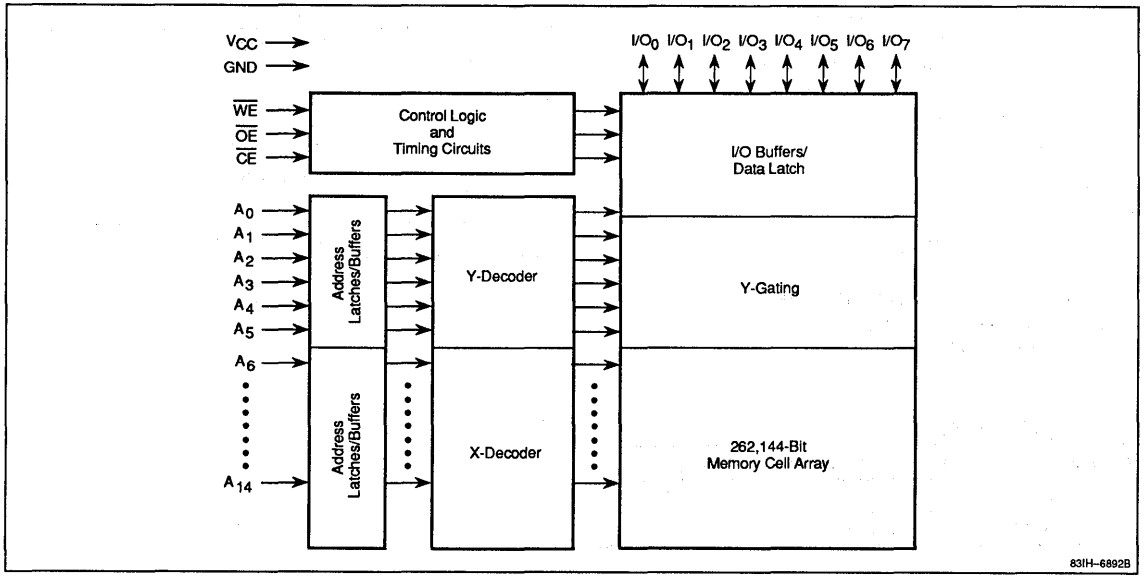
Truth Table

Function	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Input/Output	I_{CC}
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Standby and write inhibit	V_{IH}	X	X	High-Z	Standby
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	Active
Write Inhibit	X	V_{IL}	X	—	—
	X	X	V_{IH}		

Notes:

(1) X can be either V_{IL} or V_{IH}.

Block Diagram



DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Output voltage, high	V_{OH1}	2.4			V	I_{OH} = −400 μA
	V_{OH2}	V_{CC} − 0.7			V	I_{OH} = −100 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 2.1 mA
Output leakage current	I_{LO}	−10		10	μA	V_{OUT} = 0 V to V_{CC}; $\overline{CE}$ or $\overline{OE}$ = V_{IH}
Input leakage current	I_{LI}	−10		10	μA	V_{IN} = 0 V to V_{CC}
V_{CC} current (active)	I_{CCA1}			20	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
	I_{CCA2}			50	mA	f = 5 MHz; I_{OUT} = 0 mA
V_{CC} current (standby)	I_{CCS1}			1	mA	$\overline{CE}$ = V_{IH}
	I_{CCS2}			100	μA	$\overline{CE}$ = V_{CC}; V_{IN} = 0 V to V_{CC}

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ± 10%

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Parameter	Symbol	μPD28C256-20 Min	μPD28C256-20 Max	μPD28C256-25 Min	μPD28C256-25 Max	Unit	Test Conditions
Read Operation							
Address to output delay	t_{ACC}		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to output delay	t_{CE}		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to output delay	t_{OE}	10	75	10	100	ns	$\overline{CE}$ = V_{IL}
$\overline{OE}$ or $\overline{CE}$ high to output float	t_{DF}	0	60	0	80	ns	$\overline{CE}$ = V_{IL} or $\overline{OE}$ = V_{IL}
Output hold from address, $\overline{OE}$ or $\overline{CE}$, whichever transition occurs first	t_{OH}	0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
Write Operation							
Write cycle time	t_{WC}	10		10		ms	
Address setup time	t_{AS}	10		10		ns	
Address hold time	t_{AH}	200		200		ns	
Write setup time	t_{CS}	0		0		ns	
Write hold time	t_{CH}	0		0		ns	
$\overline{CE}$ pulse width	t_{CW}	150		150		ns	
$\overline{OE}$ high setup time	t_{OES}	10		10		ns	
$\overline{OE}$ high hold time	t_{OEH}	50		50		ns	
$\overline{WE}$ pulse width	t_{WP}	150		150		ns	
$\overline{WE}$ high pulse width	t_{WPH}	2		2		μs	
$\overline{WE}$ high hold time	t_{WEH}	9.9		9.9		ms	
$\overline{CE}$ high hold time	t_{CEH}	9.9		9.9		ms	
Data setup time	t_{DS}	100		100		ns	
Data hold time	t_{DH}	50		50		ns	
Byte load cycle time	t_{BLC}	3	100	3	100	μs	

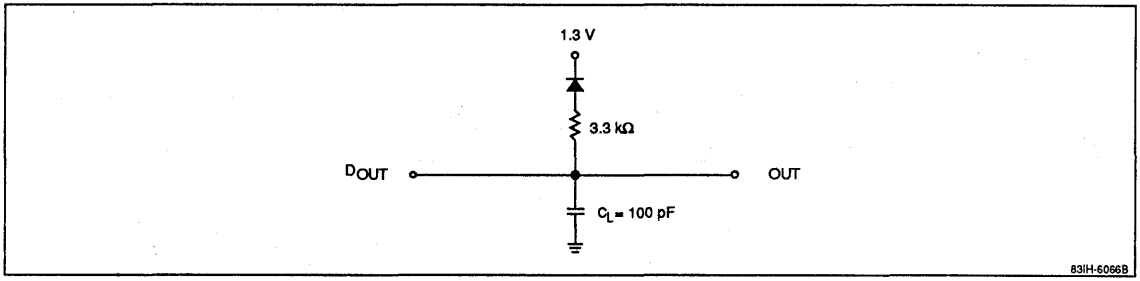
AC Characteristics (cont)

Parameter	Symbol	μPD28C256-20 Min	μPD28C256-20 Max	μPD28C256-25 Min	μPD28C256-25 Max	Unit	Test Conditions
Software Chip Erase Operation							
$\overline{CE}$ setup time	t_{ECS}	500		500		ns	
$\overline{WE}$ pulse width	t_{EWP}	10		10		ms	
$\overline{CE}$ hold time	t_{ECH}	20		20		μs	

Notes:

(1) See figure 1 for the output load. Input rise and fall times ≤ 20 ns; input pulse levels = 0.45 and 2.4 V; timing measurement reference levels = 0.8 and 2.0 V for both inputs and outputs.

Figure 1. Output Load



Read Cycles

Both $\overline{CE}$ and $\overline{OE}$ must be at V_{IL} to enable stored data to be read. While the device is executing read cycles, bringing either of these inputs to V_{IH} will place the outputs in high impedance. This two-line output control allows bus contention to be eliminated in the system application.

Byte Write Cycles

Low levels on $\overline{CE}$ and $\overline{WE}$ and a high level on $\overline{OE}$ place the μPD28C256 in write operation. Write address inputs are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs later. Data inputs are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier. Once byte write operation has begun, the internal circuits assume all timing control and the byte being addressed is automatically erased and then programmed within the write cycle time (t_{WC}) of 10 ms.

Page Write Cycles

This option allows the μPD28C256 to be completely programmed in a much shorter time than is required by byte write cycles. Page write cycles can program up to 64 bytes simultaneously, enabling the μPD28C256 to be completely written within a maximum of 5.2 seconds. The page address is specified by the inputs A_6 through A_{14}; once set, this address cannot be changed. Within the page, address inputs A_0 through A_5 can be used sequentially or in random order to specify individual bytes.

The beginning of a page write cycle is the same as a $\overline{WE}$-controlled byte write cycle. If the next falling edge of $\overline{WE}$ occurs within a byte load cycle time of 100 μs, the internal byte register will be loaded with another byte of input data. This cycle can be repeated to load a maximum of 64 bytes of data. At any point in the sequence, if $\overline{WE}$ does not have a new falling edge within the cycle time of 100 μs, byte loading will terminate and automatic erasing and programming operations will begin.

$\overline{DATA}$ Polling Feature

This feature supports system software by indicating the precise end of byte write and page write cycles. $\overline{DATA}$ polling can be used to reduce total programming time of the μPD28C256 to a minimum value, which varies with the system environment.

While internal automatic write operation is in progress, any attempt to read data at the last externally supplied address location will result in inverted data on pin I/O_7 (for example, if write data = 1xxx xxxx, then read data = 0xxx xxxx). Once the write cycle is complete, a read cycle will result in true data being output on I/O_7.

Toggle Bit Feature

The feature provides another method for indicating the end of write cycles. During the internal automatic write operation, I/O_6 will toggle from 0 to 1 and back on successive attempts to read data. When the write cycle is complete, the toggling stops; a read cycle results in true data being output on I/O_6 (figure 2).

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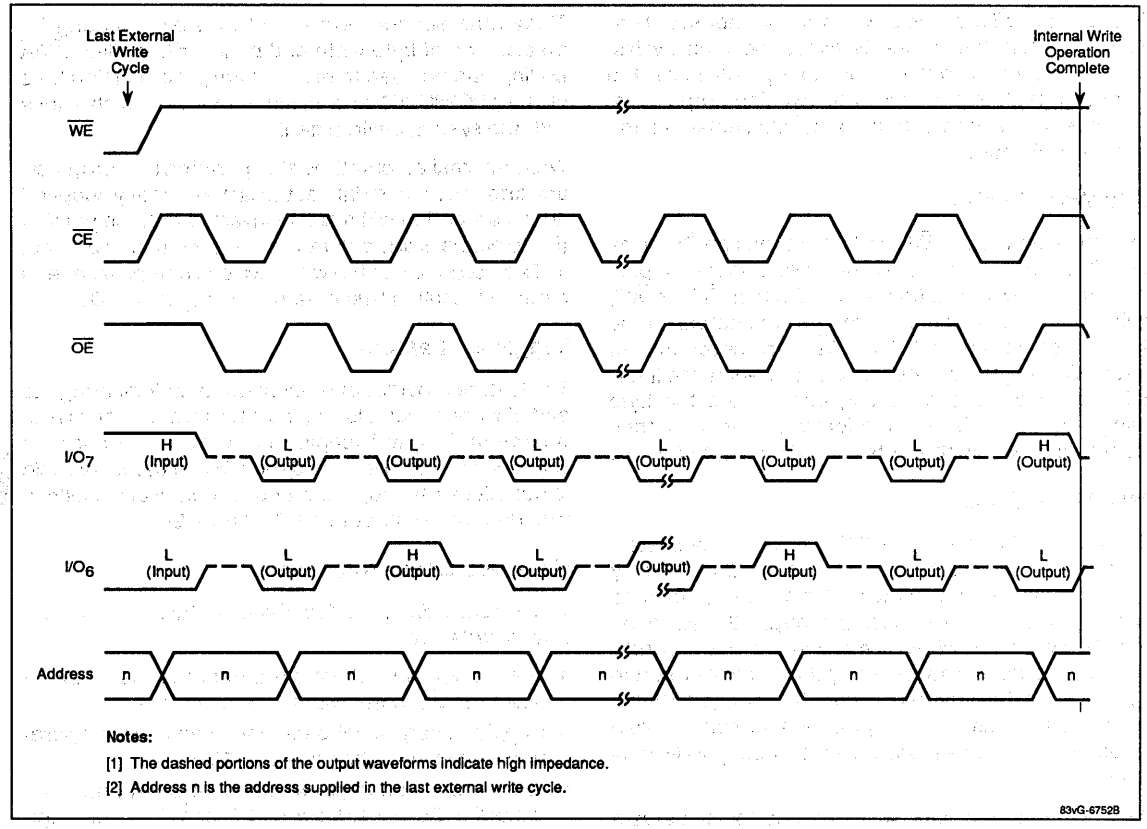
Hardware Data Protection

The μPD28C256 provides three features to prevent invalid write cycles:

- Noise immunity, where write operation is inhibited when the $\overline{WE}$ pulse width is 20 ns or less.
- Supply voltage level detection, where write operation is inhibited when V_{CC} is 2.5 V or less.
- Write protection logic, where write operation is inhibited if $\overline{OE}$ is held low or $\overline{CE}$ or $\overline{WE}$ is held high during power on or off of the V_{CC} supply voltage.

Figure 2. Data Polling and Toggle Bit Operation



Notes:

[1] The dashed portions of the output waveforms indicate high impedance.

[2] Address n is the address supplied in the last external write cycle.

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Software Data Protection

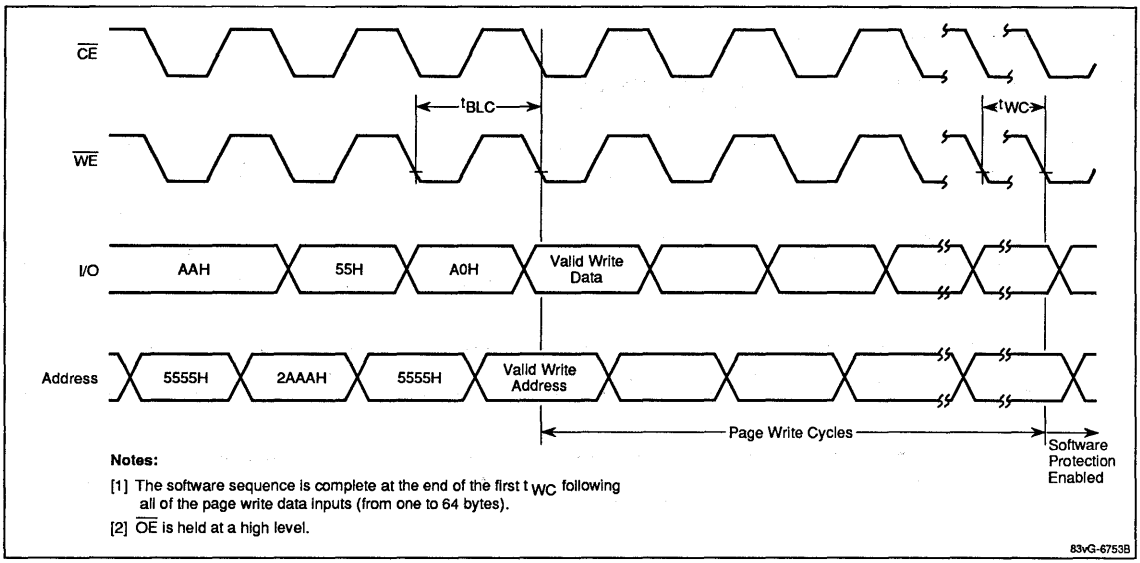
Additional protection of data is available using software control. Standard, unprotected write cycles are illustrated in the timing waveforms. Additional software-controlled protection is enabled or reset with two special sequences of write cycles. To enable software data protection, or to execute additional write cycles after the μPD28C256 is in a protected state, use the address and data sequence shown in table 1. All three byte write cycles must be issued in sequence and must meet the timing illustrated in figure 3.

Table 1. Sequence to Enable Software Data Protection

Address Input (Hex)	Write Data (Hex)
5555H	AAH
2AAAH	55H
5555H	A0H

Under software protection, no write cycles will be executed unless preceded by the above sequence. The protection circuit is nonvolatile and continues to protect the data during power-down and power-up.

Figure 3. Sequence to Initiate or Continue Software Data Protection



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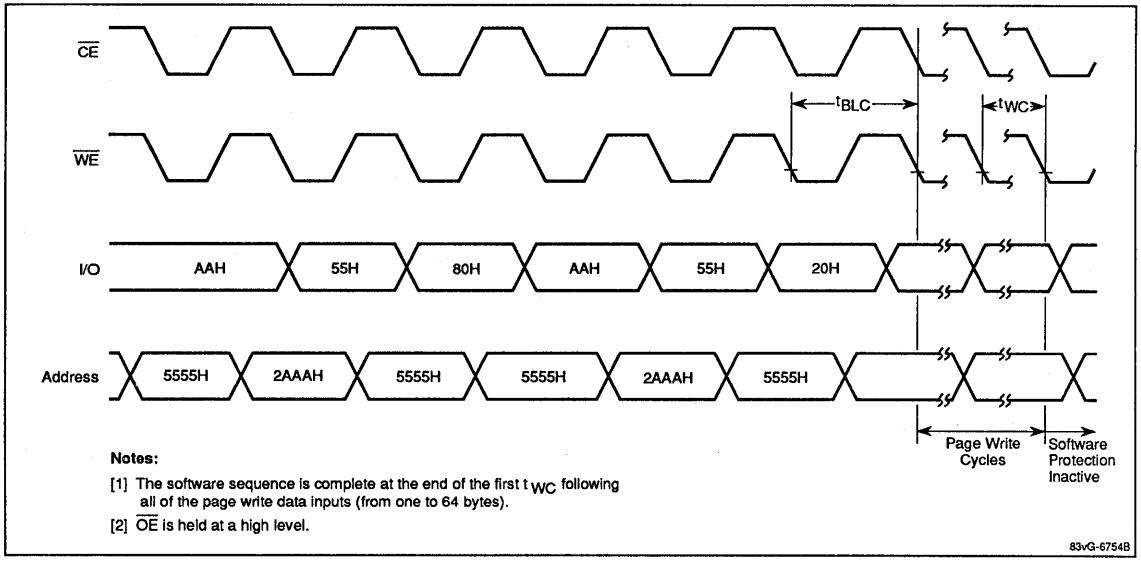
To disable software protection for ease in testing or reprogramming of the μPD28C256, the byte reset sequence shown in table 2 must be issued. The timing is illustrated in figure 4.

Table 2. Sequence to Disable Software Data Protection

Address Input (Hex)	Write Data (Hex)
5555H	AAH
2AAAH	55H
5555H	80H
5555H	AAH
2AAAH	55H
5555H	20H

At the end of this sequence, and after a minimum delay of t_{WC} to reset the nonvolatile protection circuit, the μPD28C256 is in an unprotected state. Any standard write cycle can be executed as desired. In this state, the hardware features provide all data protection.

Figure 4. Reset Sequence for Software Data Protection



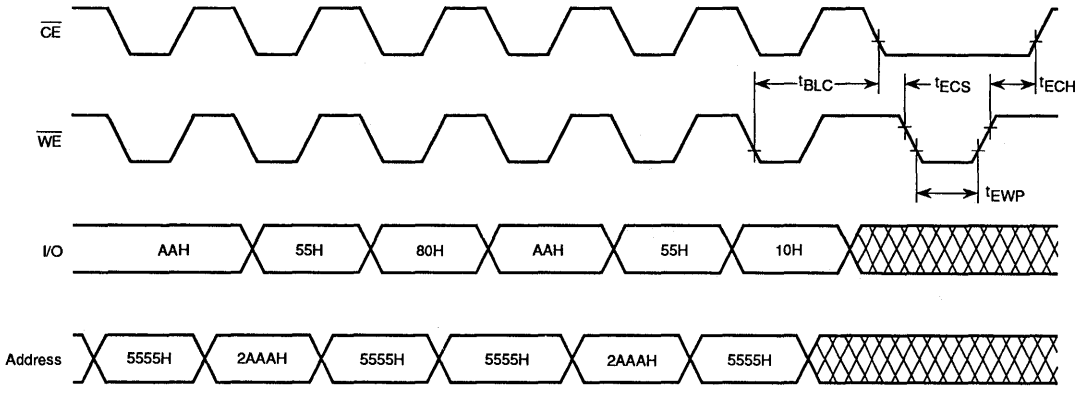
Software Chip Erase Feature

All bytes of the μPD28C256 can be erased simultaneously by making $\overline{CE}$ and then $\overline{WE}$ fall to V_{IL} using the address and data sequence shown in table 3. The required timing is illustrated in figure 5.

Table 3. Sequence to Set Up Software Chip Erase

Address Input (Hex)	Write Data (Hex)
5 5 5 5 H	AAH
2 A A A H	55H
5 5 5 5 H	80H
5 5 5 5 H	AAH
2 A A A H	55H
5 5 5 5 H	10H

Figure 5. Sequence for Software Chip Erase



Notes:

[1] The software sequence is complete at the end of t_{ECH} following the special address and data sequence and the erase pulse on $\overline{WE}$.

[2] $\overline{OE}$ must be held at a high level.

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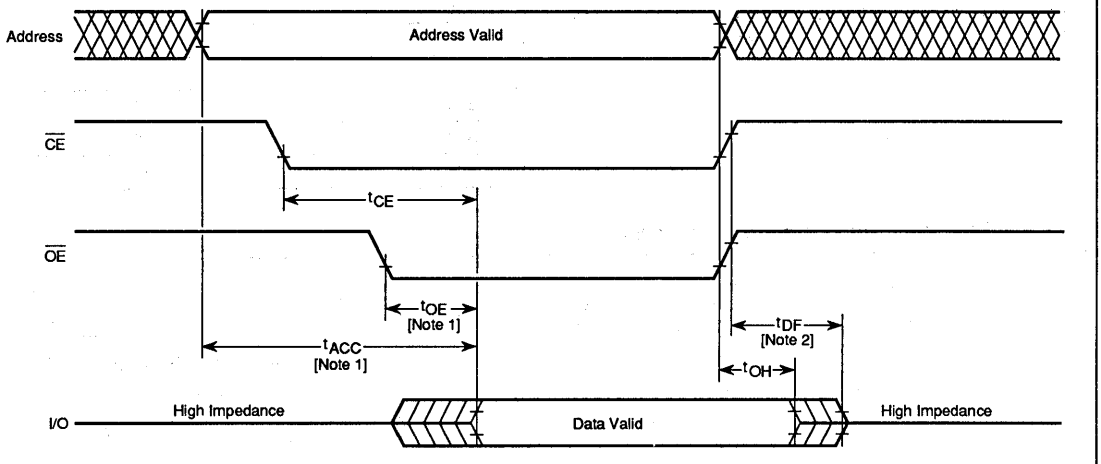
Timing Waveforms

Read Cycle



Notes:

[1] $\overline{OE}$ may be delayed for read operation up to $t_{ACC} - t_{OE}$, after the falling edge of $\overline{CE}$, without impact on t_{ACC}.

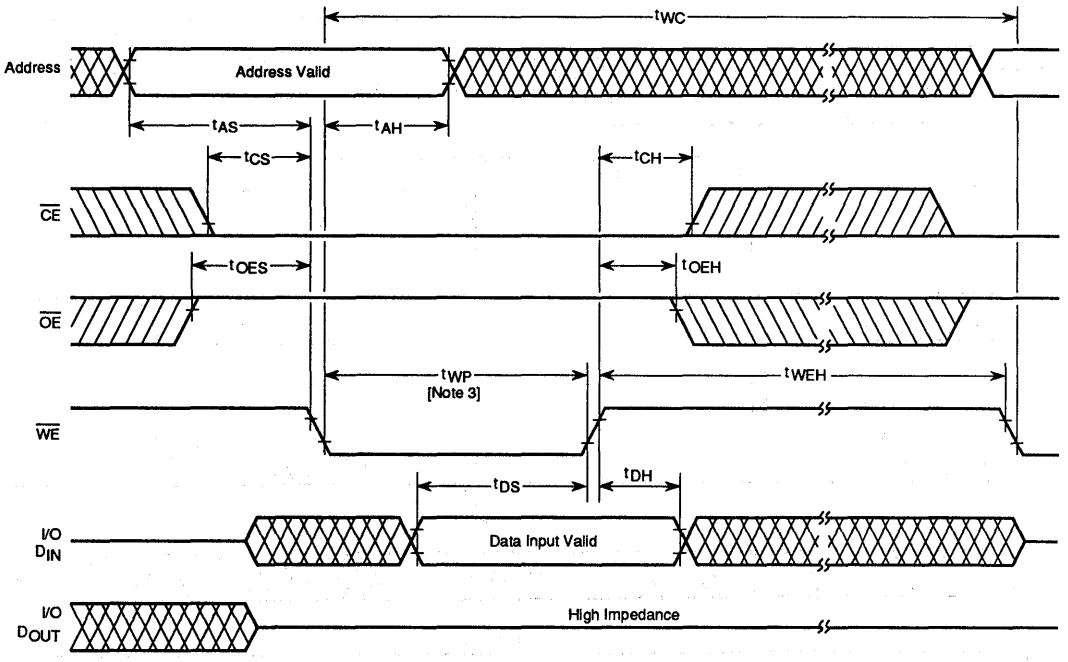
[2] t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

[3] $\overline{WE} = V_{IH}$.

83IH-6464B

Timing Waveforms (cont)

$\overline{WE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

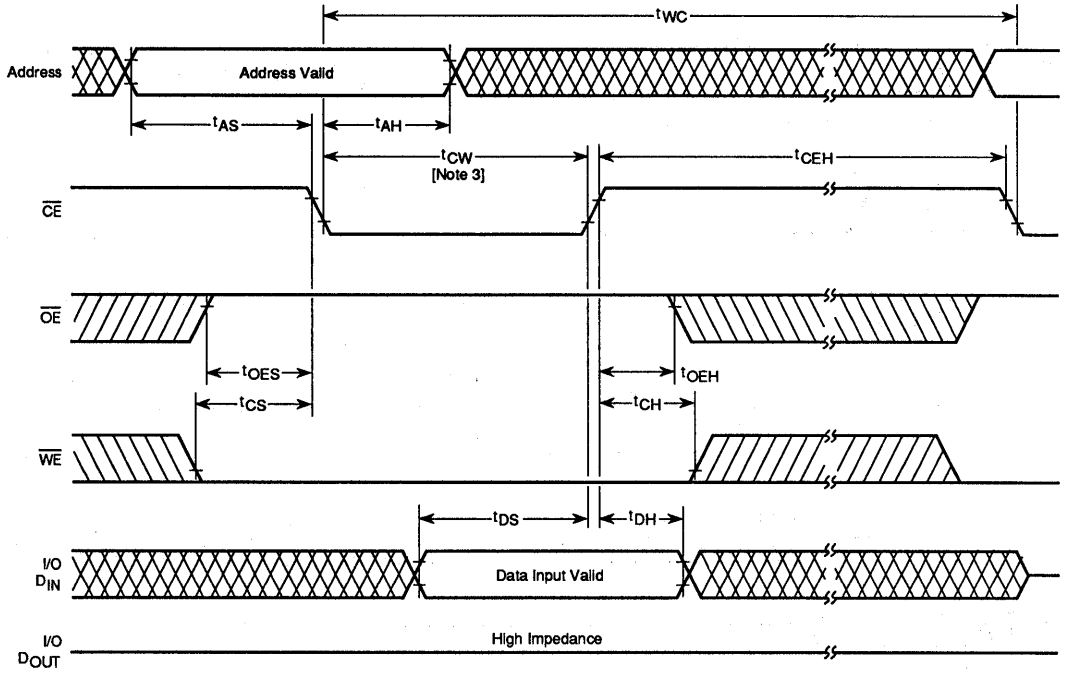
[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

83IH-6893B

27d

Timing Waveforms (cont)

$\overline{CE}$-Controlled Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

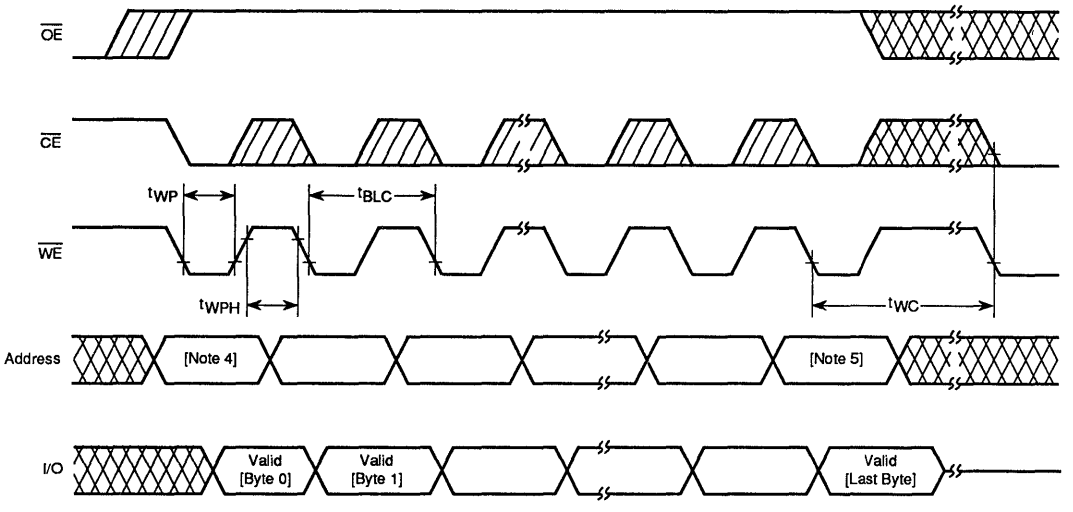
[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

831H-6894B

Timing Waveforms (cont)

Page Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

[4] The page cannot be changed in the middle of a page write cycle. Address inputs $A_6 - A_{14}$ must be supplied for every byte load cycle and must remain the same throughout the page write cycle to prevent writing to an unknown address location. Address inputs $A_0 - A_5$ are altered for each byte load cycle and determine the individual byte to be written within the page.

[5] A maximum of 64 bytes may be loaded in a single page write cycle.

83IH-6895B

27d

NEC

Section 28
Application Notes

Introduction

The objective of a memory system is to match the operating speed of a processor with the rate of information transfer. A CPU is usually about a thousand times faster than the average access time of a memory system, and the high cost of implementing a system with enough speed to accommodate this performance gap would be out of reach. To be able to meet cost and performance goals, a multilevel or hierarchical system encompassing a mix of memory devices must be implemented.

In most of these systems, the top level will have the highest performance and lowest level the slowest. Alternatively, the highest level is usually the most expensive and has the smallest density and the lowest level is the least expensive and has the highest density. Hierarchies are typically structured so that devices at level i are higher than those at level $i + 1$. If C_i, T_i, and S_i, respectively, are the cost per byte, the average access time, and the total memory size at level i, then the following relationships normally would hold between level i and $i + 1$:

$C_i > C_i + 1$, $T_i < T_i + 1$, and $S_i < S_i + 1$ for $i \geq 1$

Memory hierarchy can be classified into primary and secondary devices, depending on access times. In a typical hierarchy, the top level may consist of fast static RAMs with access times of less than 35 ns. These devices have been produced in x1, x4 and x8 organizations, and in some cases need a very low current to retain data during power failures. The next level is classified as main memory and consists of dynamic RAMs with access times between 80 and 120 ns. Secondary memory may consist of several levels of rotating drum or fixed-head magnetic disks with average times taken from the sum of rotational latency and transfer time, most likely a few milliseconds for blocks or sectors of between 1 and 4 Kbytes. Their capacity is in the Mbyte range and reflect a price equaling a few hundredths of a cent per bit. These devices are usually connected to the primary memory on a shared bus. Finally, the lowest level consists of removable magnetic tape for offline storage in a data archive.

A performance gap traditionally has existed between primary and secondary memories. The magnetic bubbles and charge-coupled devices developed to fill this gap did not find wide acceptance in most memory system applications, and contemporary designs are now using low-power, solid-state devices such as NEC's μPD42601 silicon file.

The goal of a system designer is to optimize the memory hierarchy so that system performance approaches that of the highest level of memory and cost approaches the cost of the cheapest memory. Performance depends on a number of interrelated factors, including program behavior with respect to memory references, access time and memory size of each level, granularity of information transfer (size of the data field or block), and management policies. One other important factor is the design of the processor-memory interconnection network.

Hierarchical performance can be measured by *effective access time* from the processor to the lowest level of the hierarchy, i.e., the sum of individual average access times of each of the memory levels. Effective access time generally includes the wait time caused by memory conflicts at a particular level, as well as delays in the switching network between one level and the next. The degree of conflict is usually a function of the number of processors, the number of memory modules, and the interconnection network between the processors and memory modules.

Connections between hierarchical levels are characterized by their transfer rates, or bandwidth, i.e., the number of bits per second that can be accessed. For example, if a memory system has a cycle time of 500 ns and is able to access 32 bits (4 bytes) per cycle, its bandwidth is 64 Mbits (8 Mbytes). To increase bandwidth, a designer might choose to reduce the cycle time, increase word size of the memory, or access the memory modules in parallel. Each would have a different impact on system architecture and cost.

Although the best possible design depends on workload and the available technology, there is no one formula for creating an optimal generic design. When considering a traditional von Neumann architecture, a single memory module of conventional design can access no more than one word during each clock cycle. With this fundamental constraint, the designer must rely on technological advances to be able to improve computer system performance.

HIERARCHICAL CLASSIFICATIONS

High-Speed Static RAMs at Level 1

Although the highest hierarchical level contains memory capable of matching the cycle time of the CPU, capacity of these devices typically will be determined by the cost and performance goals of the system. Static RAM traditionally has been used in this level because of its performance capabilities and ease of use. An SRAM is basically a stable dc flip-flop requiring no clocks or refreshing, which means its storage element retains data as power is applied. Fast access times, a parallel address structure, and the absence of strict timing requirements have made these devices very attractive in cache and small system designs.

SRAMs have been developed with technologies such as Bipolar, CMOS and BiCMOS, resulting in a number of products with different access times and organizations. Some of the most common configurations are 32K x 8, 64K x 4 and 256K x 1, 1M x 1 and 256K x 4, as reflected in NEC's μPD43256A, μPD43254, μPD46251, μPD431001 and μPD431004 devices, respectively. In the small system market, where low cost rather than high performance is the primary objective, byte-wide SRAMs with access times similar to DRAMs or EPROMs are required. Alternatively, cache memory design requires very fast access time, high density, and x1 or x4 organizations with high performance and advanced SRAM technology.

Some SRAMs have the ability to retain data when system power has failed or is shut down. In this case, the SRAM is usually designated as a low-power device (-LL version) whose data retention current can be as low as 10 μA and whose backup power is supplied by a battery backup circuit. This feature is attractive in small laptop systems and in instrumentation applications where low power is a primary concern.

The byte-wide SRAM such as NEC's 32K x 8-bit μPD43256A has access times in the range of 85 to 150 ns, 28-pin DIP packaging (600 mil wide), and access time compatibility with EPROMs (figure 1). However, a 600-mil device requires a substantial amount of board space (figure 1), and thus the part is also offered in a 28-pin plastic miniflat package for higher density, surface-mounted printed circuit board applications (figure 2).

A x1 SRAM is often used for large, high-speed memory circuits where fast access time and high-density chip layouts are required. Having only one data bit per SRAM chip reduces the pin count and allows use of an

Figure 1. 28-Pin Plastic DIP (600 mil)

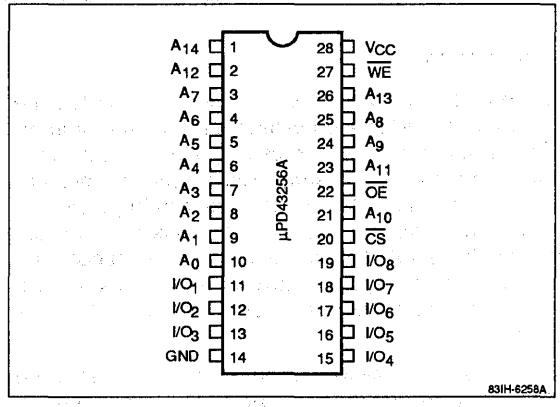
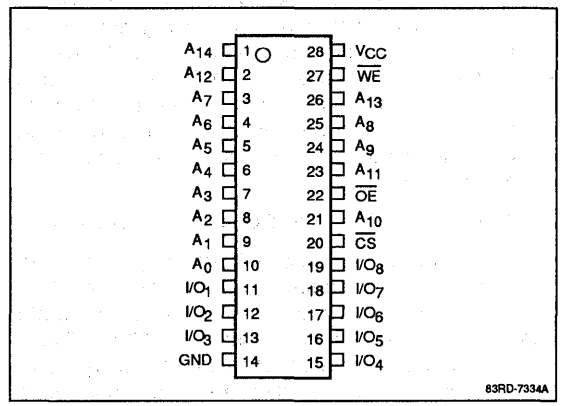


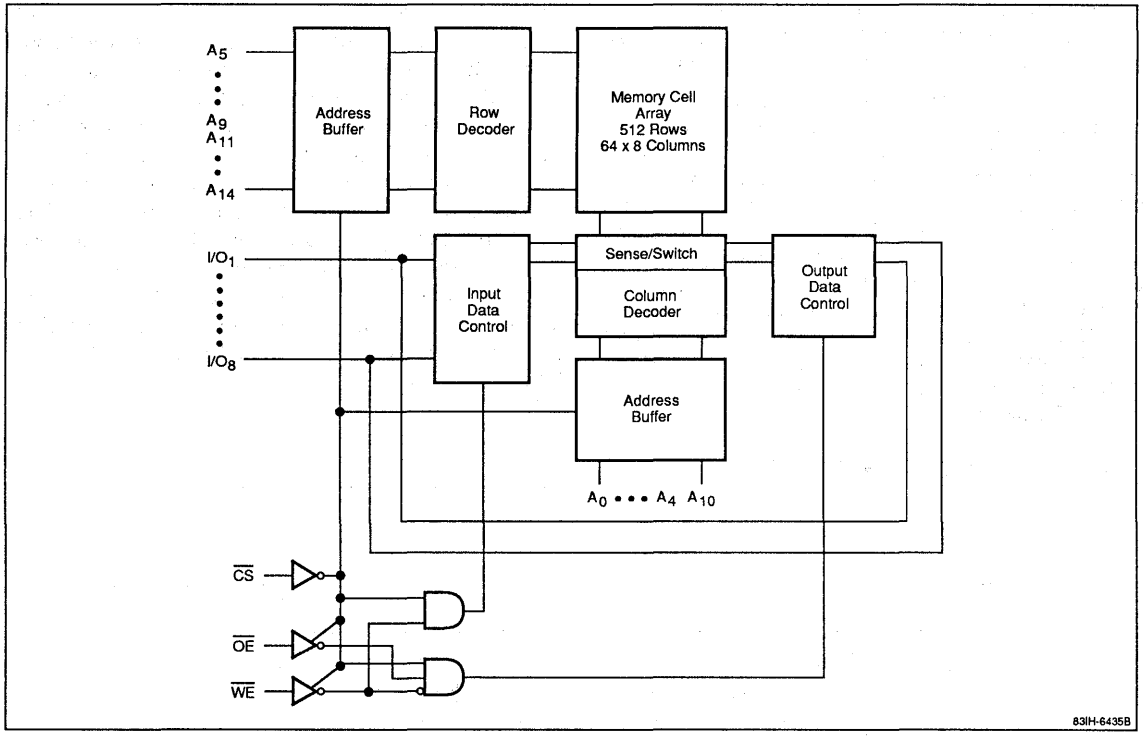
Figure 2. 28-Pin Plastic Miniflat (450 mil)



18- or 22-pin package that significantly reduces board space. High-speed static RAMs are available in x1, x4, and x8 configurations with access times ranging from 15 to 80 ns. A typical application for these devices is as data and address tag memories in cache subsystems whose access times must equal processor access times.

One advantage of using an SRAM is its ability to interface to a memory bus. The μPD43256A, for example, has 15 address lines, 8 common input/output signals, an output enable ($\overline{OE}$) pin, a write enable ($\overline{WE}$) pin, and power and ground pins (figure 3). A chip select ($\overline{CS}$) pin controls operation of the device. When $\overline{CS}$ is high, the device is in standby and power consumption is greatly reduced. A designer can minimize total power supply current by enabling only the accessed devices in standby.

Figure 3. Block Diagram of μPD43256A



The $\overline{OE}$ pin controls the three-state output drivers during a read cycle and can only be active when $\overline{CS}$ is asserted. Write cycles are controlled by $\overline{WE}$. When $\overline{CS}$ and $\overline{WE}$ are asserted low, data on the common I/O pins is written into the memory cells and the output data drivers are disabled to prevent a possible bus fight.

The separation of the chip select function into two components, $\overline{OE}$ and $\overline{CE}$, has several timing implications. The access times from chip select (t_{ACS}) and address valid (t_{AA}) are the same in the μPD43256A, 85 ns, but typically an SRAM design requires that the address be decoded before the chip can be selected. This decoding function requires an additional delay, making the effective address time the sum of the worst case propagation delay of the address decoder (74LS138) and the chip select address access time (t_{ACS}). Alternatively, since the output enable time (t_{OE}) of 40 ns is less than the access time, the effective access time can be optimized by concurrently accessing the SRAM with a valid address and controlling the $\overline{OE}$ pin with a read signal and the output of the address decoder. The disadvantage of this scheme is that the $\overline{CS}$ pin is always asserted, causing the SRAM to always be active. For circuits with only a few SRAM devices, the power considerations are not important. In cases where a lot of SRAMs are being used, power requirements may necessitate that $\overline{CS}$ be asserted to control the active and standby current.

Dynamic RAMs at Level 2

Data in an SRAM cell will remain valid as long as power is applied to the chip, because data is stored as a 1 or 0 in a flip-flop circuit consisting of four or six transistors. This approach allows for simplified operation, although the relatively large memory cell requires a large die. A dynamic RAM, on the other hand, stores data in the charge on a capacitor rather than in a flip-flop, thereby reducing the area required for each cell. And since die size has a direct bearing on the cost of a chip, a denser DRAM circuit will have a lower cost per bit.

Using a capacitor to store memory data means that more complex circuitry is required, as well as sophisticated techniques to sense the charge on the storage capacitor. Because of leakage current, a method of periodically refreshing the charge on the capacitor is

also required. Since DRAMs are traditionally used in large systems where tens or hundreds of memory chips are needed, the more complex interface circuitry can be absorbed into the cost of the memory circuit.

In a hierarchy, DRAMs are used in the larger, slower main level. It is this level that degrades effective access time and system performance. When the smaller cache does not have the data requested by the processor, the cache executes a replacement cycle to read the data from main memory and fetch it for the processor. Because the access time of main memory is in the range of 80 to 120 ns, the CPU must go into a wait state while the data is being read. In fact, high performance 20 to 33 MHz microprocessors require at least one wait state to access a DRAM circuit, requiring in the top level of the hierarchy a high performance cache able to match CPU cycle time.

DRAM performance can be enhanced with a number of circuit design techniques, as well as with a number of on-chip operating features that help to optimize bandwidth. Most contemporary 1M DRAMs are manufactured with extended features such as fast-page cycles that allow several locations within a row of memory to be accessed without repeating the row address, thereby reducing cycle time (figure 4). DRAMs designed with a nibble mode are able to read four successive bits by simply pulsing the $\overline{CAS}$ control signal, because column addresses are incremented internally (figure 5). Static-column DRAMs use static circuitry to decode the column addresses, reducing cycle time by allowing column accesses to be executed the same as in static RAMs (figure 6).

Figure 4. Fast-Page Early Write Cycle

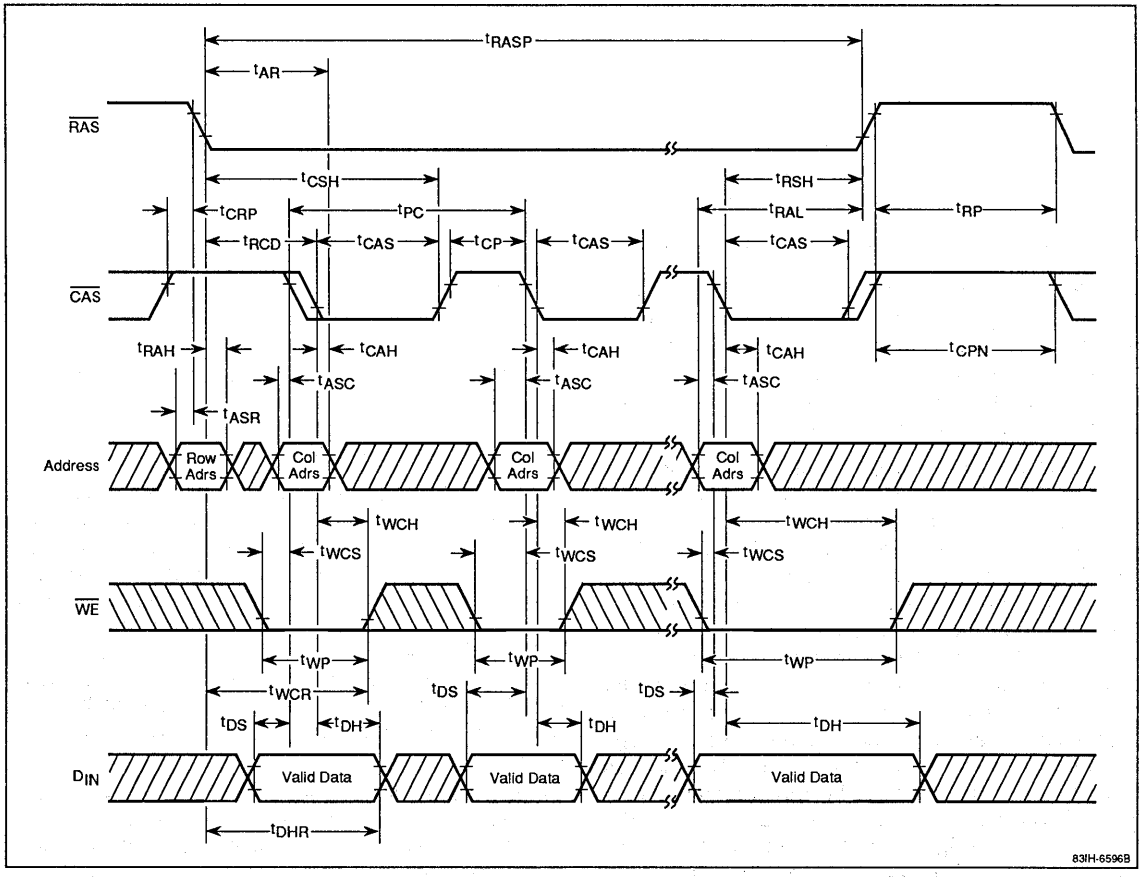


Figure 5. Nibble Mode Read Cycle

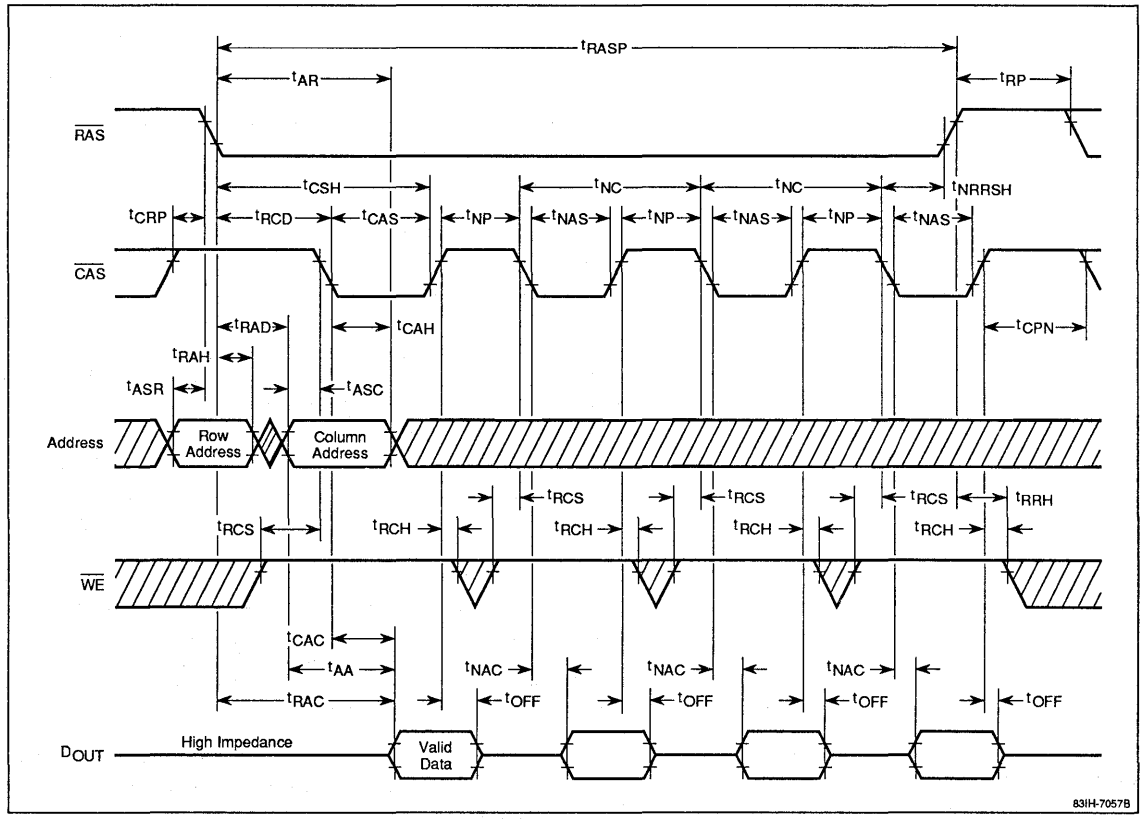


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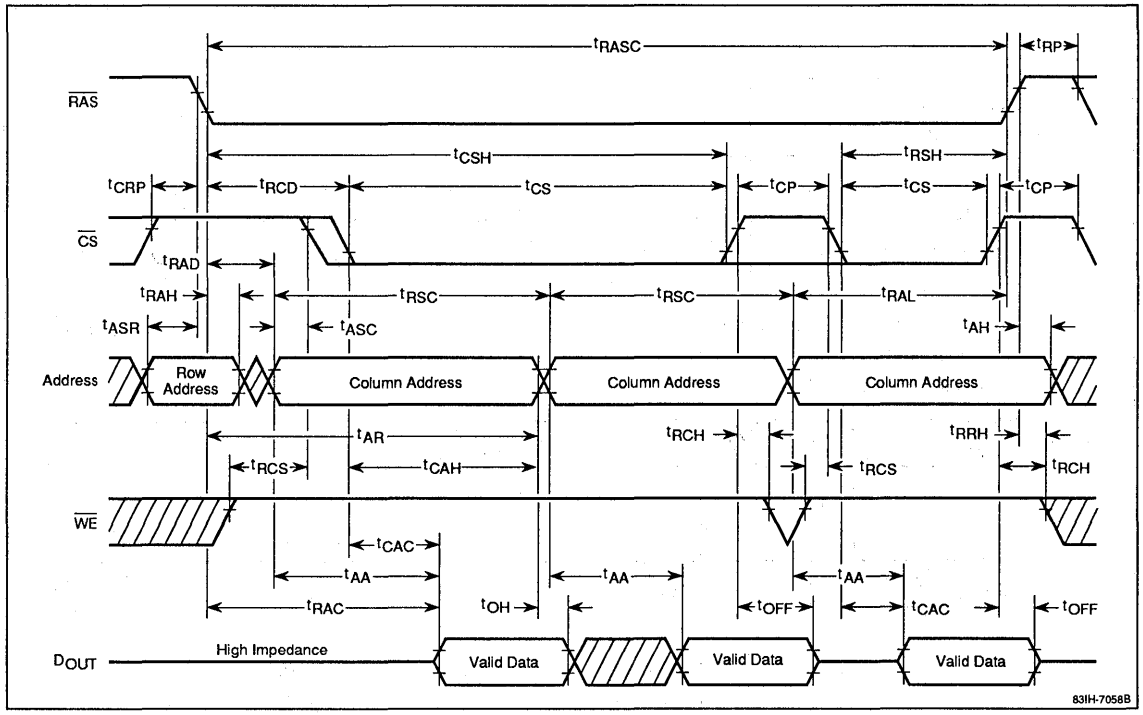
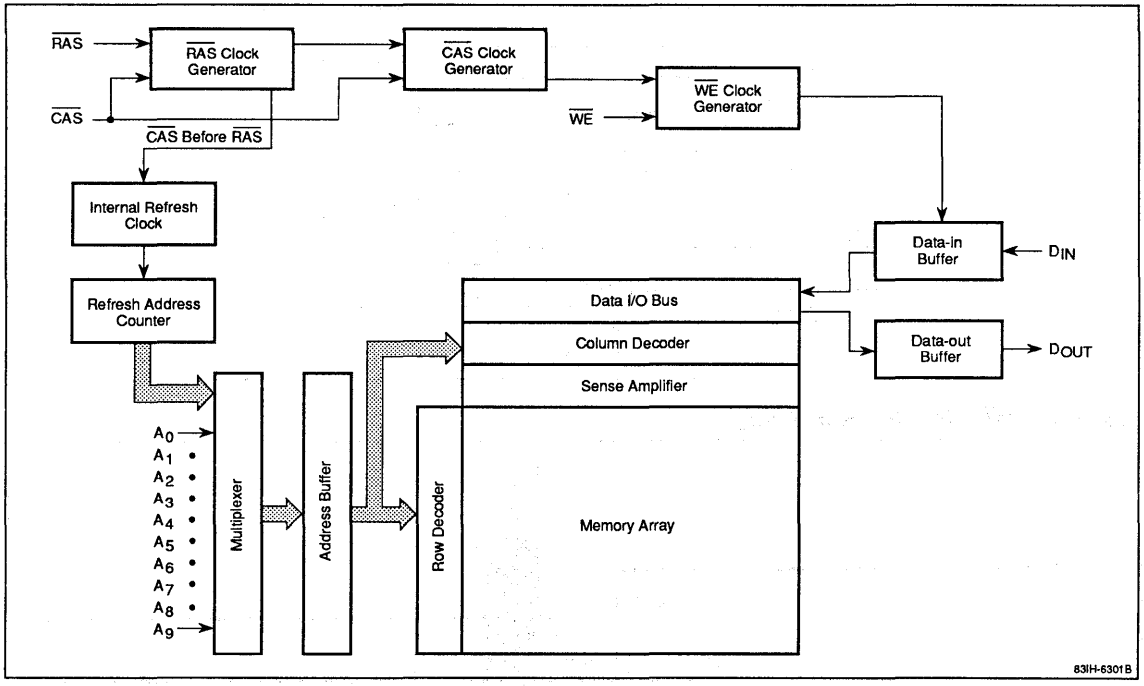
Figure 6. Static-Column Read Cycle



The architecture of the interface between the CPU and main memory is another important factor in determining system performance. Pipelined and interleaved architectures that can access the device in parallel operations can also enhance bandwidth, but require another level of complexity and cost in the CPU-memory interface.

In main memory design, the most efficient DRAM configuration is the x1 DRAM because its organization minimizes the number of pins on the chip (figure 7). Main memory circuits may have hundreds of memory chips on a printed circuit board, and since the address, data and control signals are connected to every chip, the memory section of the board is layed out in a very dense array. In fact, one of the most important parts of the DRAM design is the printed circuit layout. This array requires a memory chip with minimal pins and package size, making the x1 the most efficient. Also, with the high number of memory chips for each circuit, the cost of the circuit is high compared to other system boards and requires a higher system reliability standard.

Figure 7. Block Diagram of 1 Meg DRAM



An error correction and detection technique is typically used to enhance reliability. Most ERCC algorithms can detect two-bit errors and correct single-bit errors, allowing a single memory chip to fail without causing the system to malfunction. If the circuit uses a x4 organization and a single chip failure occurred, the ERCC circuit could not correct the multibit failure, reducing system reliability. Also, a x4 DRAM has more pins, a larger package size, and higher costs, increasing the size and cost of the memory array.

The wider organization does have one advantage for systems that require the number of memory chips to be limited because of layout area or cost. One x4 chip can replace four x1 devices in applications where density is not a factor. A typical application for the x4 organization is in computer graphics where memory size is constrained by screen resolution and the 4:1 increase in bandwidth is required to refresh the screen.

Some disadvantages of using DRAMs involve their complex interface circuitry and dynamic nature. DRAMs are arranged in a rectangular array, in which the cells are connected in a matrix of rows and columns. To be able to reduce the number of address pins, the address field is multiplexed into a row address field and a column address field (figure 8). A row address is first presented to the memory and the row address strobe ($\overline{RAS}$) control signal is asserted, beginning the memory cycle and latching the row address. The row address decoding circuit selects the appropriate row of cells (512 cells in the case of a 1M DRAM) and the column address is multiplexed onto the address pins.

Figure 8. $\overline{RAS}$ /$\overline{CAS}$ Address Multiplexer Circuit

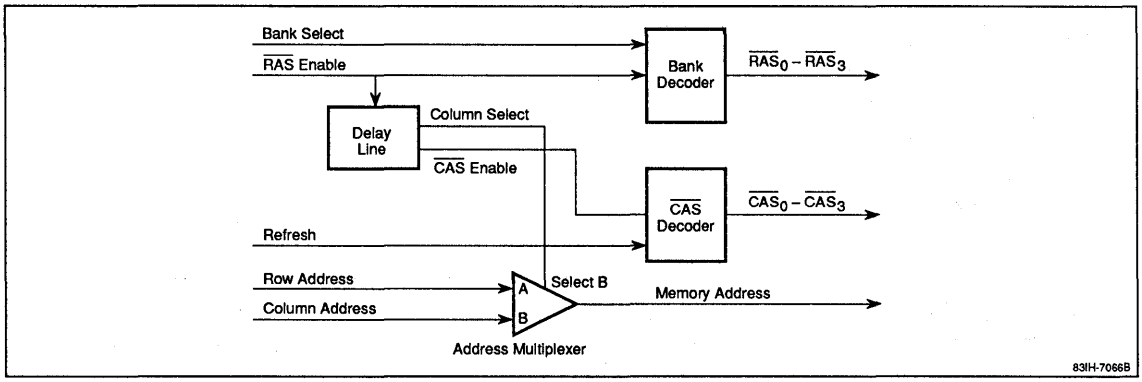
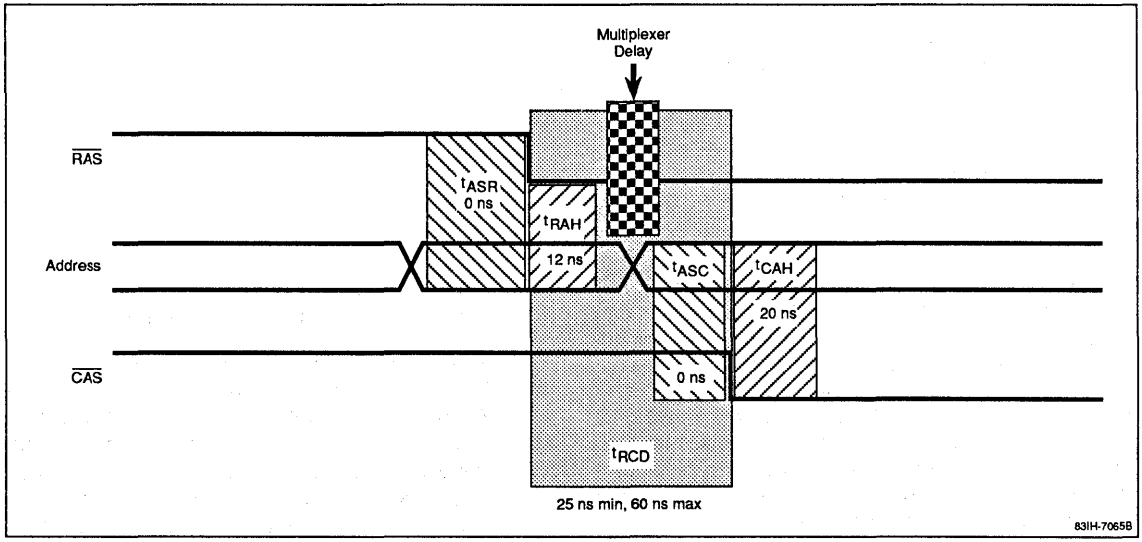


Figure 9. $\overline{RAS}$ /$\overline{CAS}$ Address Timing



The column address strobe ($\overline{CAS}$) is then asserted to latch the column address and enable the output drivers. The column address decoder selects one of the memory cells in the selected row and the data is read and sent to the output circuits. Once the data has been accessed, the $\overline{RAS}$ and $\overline{CAS}$ signals are de-asserted and remain inactive for a specified precharge time so that the circuits can recover from the previous access. Thus, the increase in cycle time over access time equals the precharge time.

DRAMs with an access time of 80 ns typically have a cycle time of 160 ns. Although multiplexing provides some substantial system benefits in terms of minimizing the number of pins and reducing package size, the address timing is complicated and requires more interface circuitry (figure 9). Row and column addresses are both multiplexed, presenting a rather tight window during which the individual events must occur. Row and column addresses both have setup and hold times with respect to $\overline{RAS}$ and $\overline{CAS}$, and if these specifications aren't met, the read or write cycle could fail. Therefore, the designer must consider the complex requirements very carefully, eliminating any timing skews, control or address line noise, and power supply noise.The dynamic nature of a DRAM means that data is stored in the charge of a capacitor, causing the charge to leak over time and the data to be lost. To prevent data loss, the DRAM must be periodically accessed to guarantee

that the charge will remain in memory. This operation is called a refresh cycle and for a 1M DRAM, all 512 rows have to be refreshed every 8 ms. This requires the DRAM interface circuit to access each row in the memory by means of either a read, write, or refresh cycle every 15.6 μs. Failure to execute a refresh cycle in the specified interval will cause the cell to leak off the charge, resulting in data errors. A refresh cycle consists of using a row address to access the appropriate row and executing a $\overline{RAS}$ cycle to refresh all the cells in that row. No $\overline{CAS}$ or column address is required.

DRAMs specify several refresh cycles: $\overline{RAS}$-only refreshing in which an external counter drives the address on the address pins; $\overline{CAS}$ before $\overline{RAS}$ refreshing in which an internal address counter is used; and hidden refreshing which is executed during a normal refresh cycle. For all refresh cycles, an external timer is required to signal the control circuit to initiate the cycle. Memory control circuitry must also have to arbitrate between an active refresh request and active memory cycle, ensuring that the refresh interval is not exceeded.

An important system design consideration is the standardization of pinouts and package size so that the circuit can be upgraded with the next generation of higher density chips (figures 10, 11, 12, 13). It is also advantageous to design a circuit with options that allow the density of the memory board to be upgraded, saving the expense of developing a new board with each new generation. For example, in the past, a memory board could be designed to easily accommodate both 64K x 1 and 256K x 1 DRAMs, both of which were packaged in a 16-pin plastic DIP. The only difference was that most 64K memory chips had one pin designated as a *no connection*. To accommodate the 256K x 1 device, the extra address line A_8 was added to the circuit to allow operation with both devices.

Figure 10. Typical 256K x 1 DRAM Pin Configuration

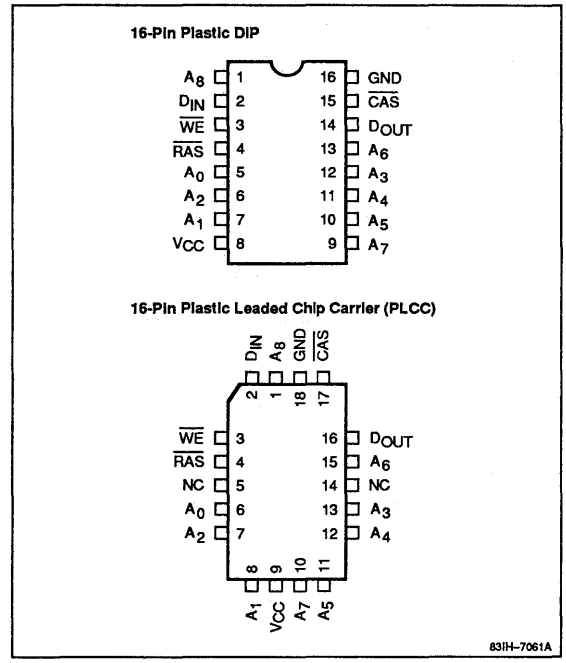


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Figure 11. Typical 64K x 4 DRAM Pin Configuration

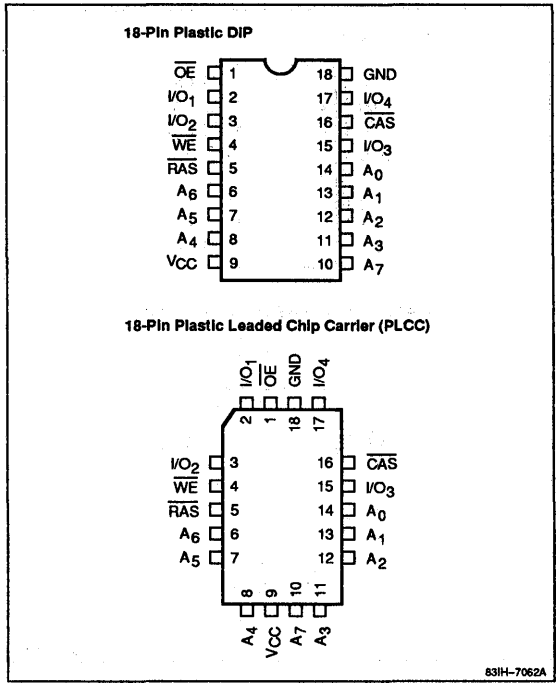


Figure 12. Typical 1 Meg x 1 DRAM Pin Configuration

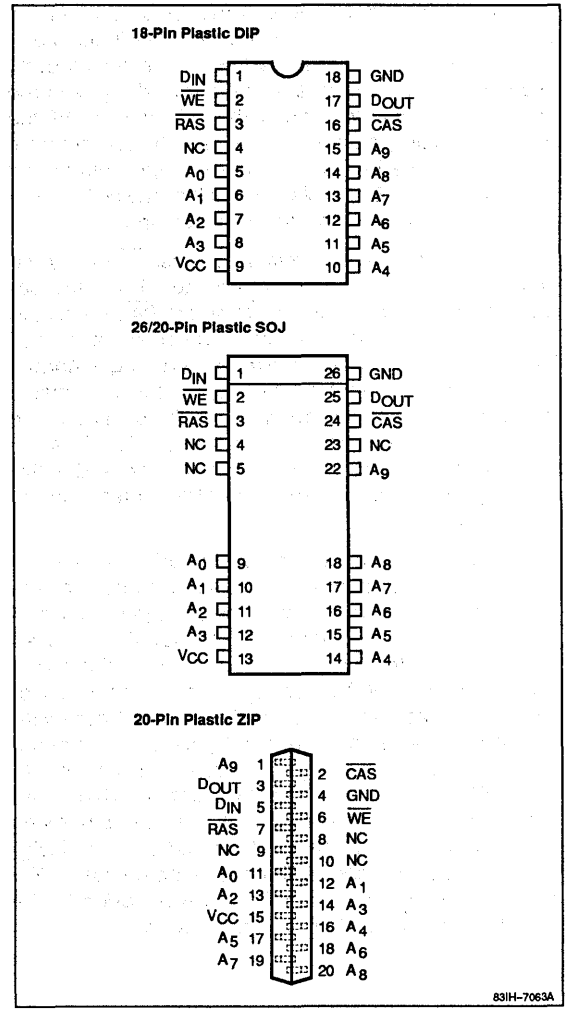
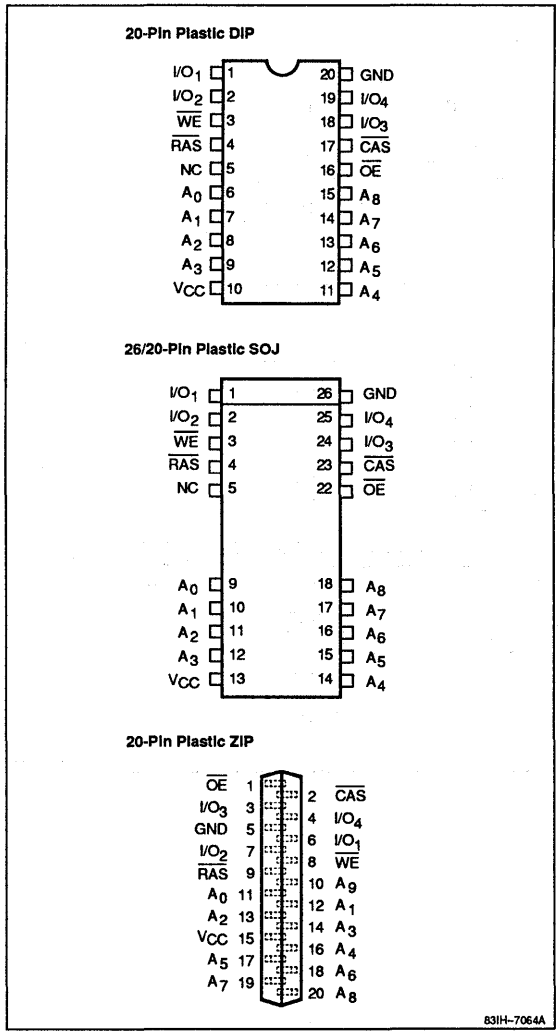


Figure 13. Typical 256K x 4 DRAM Pin Configuration



Designing the system to use either memory size also affects the multiplexing and address decoding logic. Compatibility between 256K and 1M DRAMs is more difficult because the number of pins increases from 16 to 18 pins to accommodate the additional A_9 address. The current 1M and future 4M DRAMs have the same number of pins, with the additional A_{10} address line designated for pin 4 on the DIP package, pin 5 on the SOJ, and pin 10 on the ZIP. The trend in DRAM packaging is evolving from predominantly DIP packages in the 256K era to surface-mounted SOJs and high-density ZIPs in the 1M and 4M eras.

The size of the package is another concern the designer must address when choosing 1M and 4M DRAMs. The transition from 256K to 1M DRAMs saw a change from the 16-pin packages to 18-pin packages. The 1M to 4M evolution represents a crossover generation in SOJ package width—from 300 to 350 mils. NEC's SOJ-packaged 1M μPD421000 has a specified width of 300 mils, but because of the larger die needed to implement the 4M DRAM, a width with an additional 50 mils is required for the initial 4M SOJ package. The 1M and 4M ZIP packages remain the same size, while the 4M DIP is 100 mils larger than the 300-mil DIP for the 1M DRAM. Because the surface-mounted SOJ package is projected to be the dominant package type in the future, some manufacturers may market compatible 300-mil packages for the 1M and 4M devices, but the trend will be toward even larger package sizes. For example, packages for the 16M DRAMs are likely to be 400-mil SOJs and 475-mil ZIPs, while the DIP package eventually will be phased out.

The typical development cycle of a DRAM includes a second generation of 4M DRAMs, scaled in size to optimize access time and die size. This scaled or shrink version will allow the die of a 4M DRAM to be mounted in a 300-mil SOJ package that is compatible with the SOJ package of a 1M DRAM. Also, the shrink version of the 4M DRAM will provide a very fast access time of 60 ns.

The trend in DRAM technology has seen a quadrupling in capacity about every two to four years, a result of fewer features and estimates that the 64M DRAM could use 0.35 μm technology. One major concern with very high density memory chips is test time. The widely used GALPAT standard has a test complexity of $4n^2 + 4n$ for an n-bit RAM and needs about 162 days to test a 4M RAM chip with a cycle time of 200 ns, which is unacceptable in today's manufacturing environment.

To reduce this test time, NEC has built into its μPD421000 1M DRAM a test function that reorganizes the 1M x 1-bit part into a 256K x 4-bit configuration (figure 14). The 1M test mode is enabled by applying a super voltage (V_{CC} + 3 volts) to pin 4 on the 1M DIP package (figure 15). While this super voltage is being applied, the internal configuration is changed to a 4-bit width intended to be used in a testing environment rather than in a circuit environment. Pin 4 should be regarded as a no connection, and as long as standard TTL voltage levels are connected to this pin, the 1M DRAM will remain in its normal operating state.

Figure 14. Internal Test Circuit Block Diagram

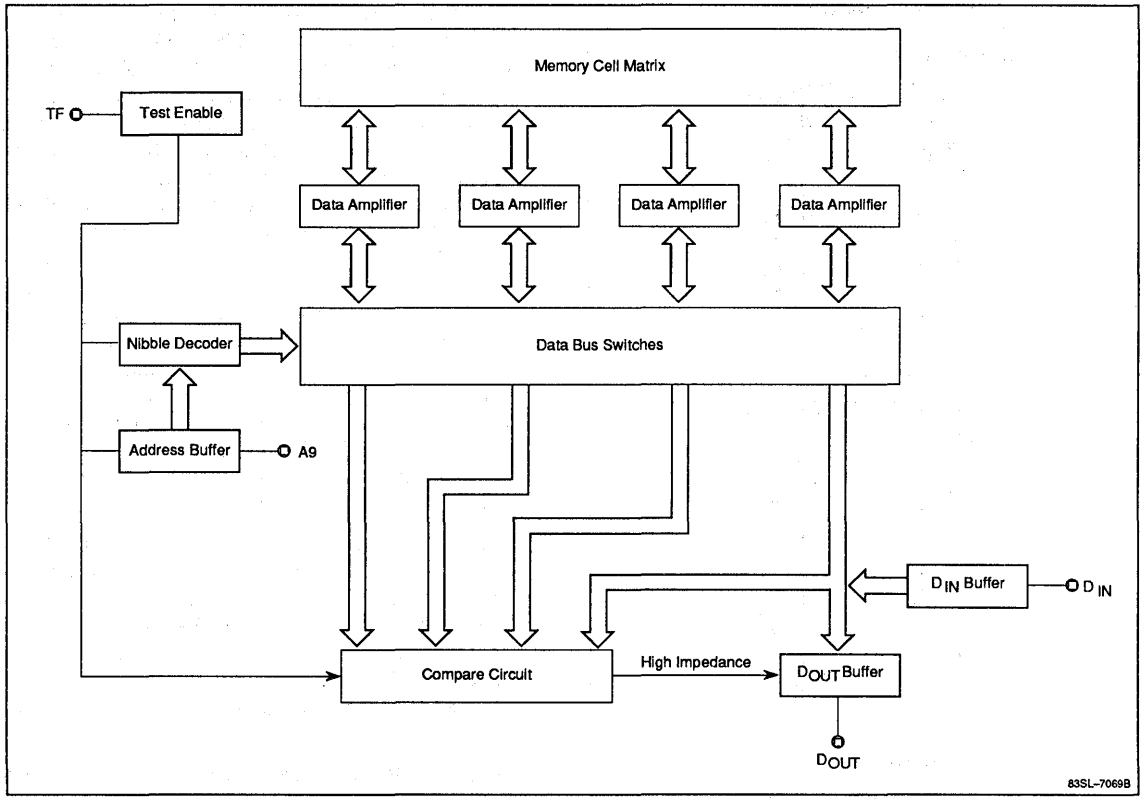
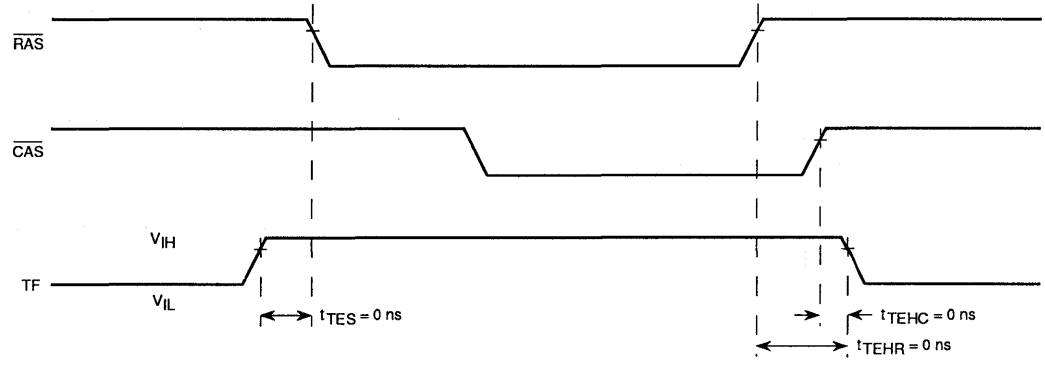


Figure 15. Timing of 1 Meg DRAM Internal Test Circuit



Notes:

[1] $V_{IH} = 9.5\ V + V_{CC}/2$.

[2] $V_{IL} = 1\ V$ min and 7 V max.

[3] Maximum voltage = 12.5 V.

[4] When a test cycle is executed, access times, device power, and the level of V_{CC} are higher than normal. Therefore, a test cycle should only be executed for verifying functional operation of the device.

[5] Data output is high impedance during a write cycle in read-modify-write test operation.

[6] Data output is high impedance after $\overline{RAS}$ goes high in a hidden refresh cycle.

[7] Four bits in a test cycle are treated the same as four bits in nibble mode.

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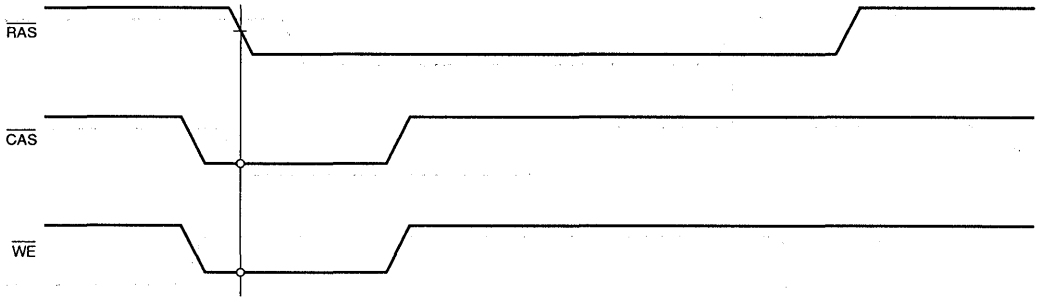
The same test strategy is implemented for the 4M DRAM, except that pin 4 on the DIP package becomes the new A_{10} address line and the test mode is initialized with logic functions rather than a super voltage. The 4M test mode will be initialized when the $\overline{WE}$ and $\overline{CAS}$ signals are active before the $\overline{RAS}$ signal is asserted, similar to a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, except that $\overline{WE}$ is asserted at the same time as the $\overline{CAS}$ signal (figure 16). The memory designer must ensure that the memory control logic does not execute $\overline{WE}$ and the $\overline{CAS}$ before $\overline{RAS}$ cycle during normal operation, which would cause the device to be configured into a 4-bit organization and errors to occur. The test issue is a major concern for future DRAM products. The 16M DRAM may have a built-in test circuit that can execute simple test programs and detect on-chip failure, but at this time no standard 16M test procedure has been defined.

Pseudostatic RAMs

The advantage of using a static RAM is its simple interface circuit and its static nature, which means it doesn't have to be periodically refreshed to retain data. Alternatively, a dynamic RAM provides greater density and a lower cost per bit. One approach that tries to provide the best attributes of both devices is the *pseudostatic RAM*, a chip that uses dynamic storage cells but contains all refresh logic on-chip so that it is able to function similarly to a static RAM. NEC's μPD428128 is a 128K x 8-bit pseudostatic RAM that offers a system designer a byte-wide RAM with the density and simple interface of a 1M DRAM (figure 17).

Figure 16. Timing of 4 Meg DRAM Internal Test Circuit



Notes:

[1] $\overline{RAS}$-only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh may be executed to transistion from a test cycle.

[2] For x 1 parts D_{OUT} is high if all 8 bits are equal, and low if all 8 bits are not equal.

[3] For x 4 parts, all I/O pins are enabled and D_{OUT} is high if all 2 bits are equal, and low if all 2 bits are not equal.

[4] Address compression control bits are defined below.

Data Bus Width (bits)	Control Address Bits (Don't care address)
8	A10R, A10C, A0C (for x 1 bit)
2	A0C (for x 4 bit)

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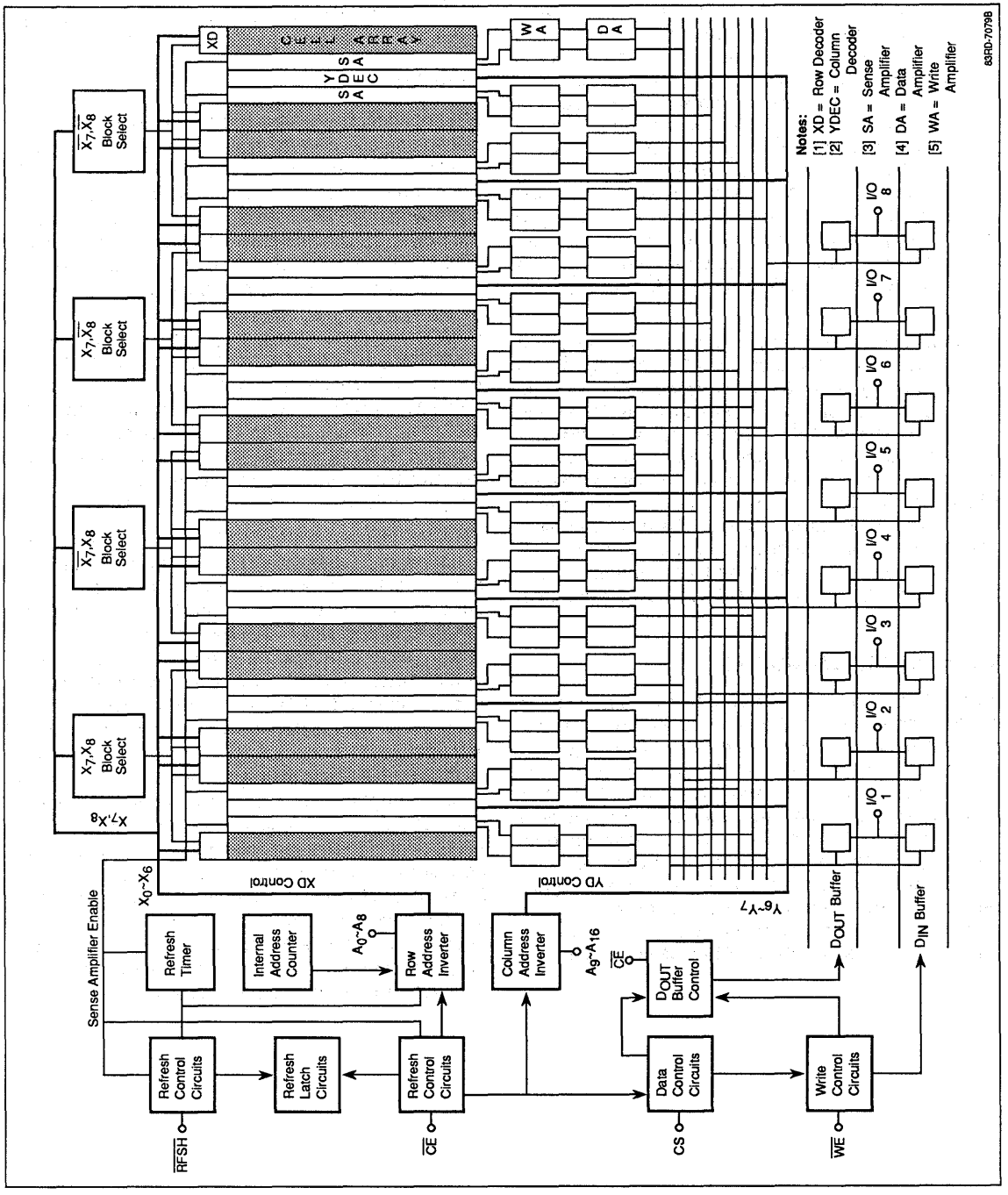
Figure 17. Block Diagram of Pseudostatic RAM



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Pseudostatic RAM are nearly, but not quite, as easy to use as fully static RAMs. Because pseudostatic RAMs must execute internal refresh cycles periodically, there is a potential for a conflict between an external access request and an internal cycle. The μPD428128 uses two types of refresh cycles, pulse and self-refresh, each of which requires an extra $\overline{RFSH}$ function pin. In pulse refresh operation, the $\overline{RFSH}$ signal is asserted during a read or write cycle, allowing refreshing to occur during a valid memory cycle. NEC's other pseudostatic RAM, the 32K x 8-bit μPD42832 (now obsolete), was packaged in a 28-pin plastic DIP and did not have a separate $\overline{RFSH}$ pin. As a result, external pulse and self-refresh operations were controlled by the $\overline{CE}$ and $\overline{OE}/\overline{RFSH}$ signals.

The μPD428128, on the other hand, is packaged in a 32-pin package and has separate $\overline{RFSH}$ (pin 1), $\overline{CE}$ (pin 22), $\overline{OE}$ (pin 24), and $\overline{CS}$ (pin 30) signals. Similar to its counterpart in the 32K x 8-bit μPD42832, the $\overline{CE}$ pin can control external or $\overline{CE}$-controlled refresh cycles, but only the separate $\overline{RFSH}$ signal can control pulse refreshing. Also, self-refresh cycles are generated by the $\overline{RFSH}$ signal and feature a very low 200 μA self-refresh current. Therefore, the pseudostatic RAM, with its lower cost per bit, simplified interface circuit, and low self-refresh current fills a cost and performance niche between the higher priced SRAM and the more complex DRAM.

NONVOLATILE MEMORIES

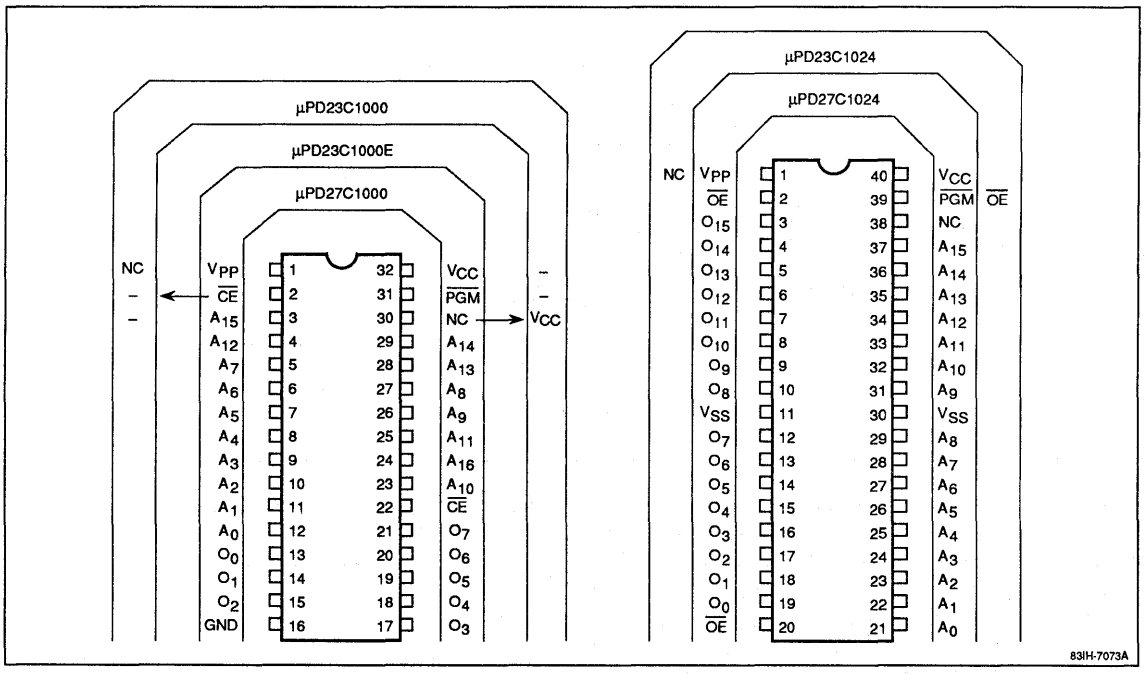
Unlike SRAMs and DRAMs, which lose data as soon as power is removed from the device, nonvolatile memories have the capability to store data indefinitely, even when power has been removed. Although these devices have slower access times and are not usually part of the high performance memory hierarchy, they are able to store data for functions involving communications, CRTs, keyboards, and other peripheral circuits. In today's system development environment, the designer can choose from erasable programmable read-only memories or one-time programmable EPROMs, electrically programmable ROMs (EEPROMs), and mask-programmable ROMs, each of which has a different effect on product development and manufacturing in terms of functionality, compatibility and cost.

EPROMs

EPROMs offer the system designer a nonvolatile memory source and also the ability to erase and program. EPROMs are programmed by an instrument called a PROM programmer and then inserted into an applications system. EPROMs retain their data for years without power, and can be erased by shining an ultraviolet light into the window in the top of the IC package. The EPROM can then be reprogrammed any number of times. Programming requires a special programming voltage (V_{PP}) which is typically 12 to 25 volts, depending on the type of device. The programmer interfaces to the EPROM, supplying the control signals, address, data and V_{PP} for each address and follows an algorithm that programs and verifies the data being written into the device. Early EPROM designs required a 25 volt programming voltage, which was reduced in succeeding generations to 21 volts and then to 12.5 volts.

EPROMs are used to storing a local program for system initiation, baud rate and data formats for CRT terminals and character translation for keyboards. Such applications require the EPROM to interface directly to the CPU's local bus, which may be 8, 16 or 32 bits. For this reason, most EPROMs are configured as a byte-wide (8-bit) device, requiring a relatively large, 600-mil package and pinout. EPROMs are primarily intended to be used in the circuit development phase and replaced with less costly one-time programmable devices such as OTP EPROMs and mask-programmable ROMs in the production phase. This requires compatible package sizes and pin assignments across the family of nonvolatile devices. To accommodate this compatibility issue, nonvolatile devices use a standard byte-wide format for package size and pin assignments (figure 18). If the designer designs a circuit to upgrade from an EPROM of one size to an EPROM of the next size, the required jumper options need to be implemented to reconfigure the circuit to the next highest density.

Figure 18. EPROM/ROM Pinout Compatibility



EEPROMs

One disadvantage of the EPROM is that it cannot be programmed while it is in a circuit. The EEPROM solves that problem by providing a write function that can be used while the EEPROM is still in the circuit. The microprocessor can write to the EEPROM just as if it were a RAM and continue with other operations during the long write cycle time. NEC's 8K x 8-bit μPD28C64 EEPROM includes a feature called $\overline{\text{DATA}}$ polling to indicate when a write cycle is complete (figure 19). If the EEPROM is read while an internal write cycle is in progress, the EEPROM returns the complement of the last data written. Thus, the system software can determine when the write cycle is complete by reading the location last written and comparing it to the data being written. The EEPROM can accomplish this because it includes on-chip latches and an automatic "erase before write" function.

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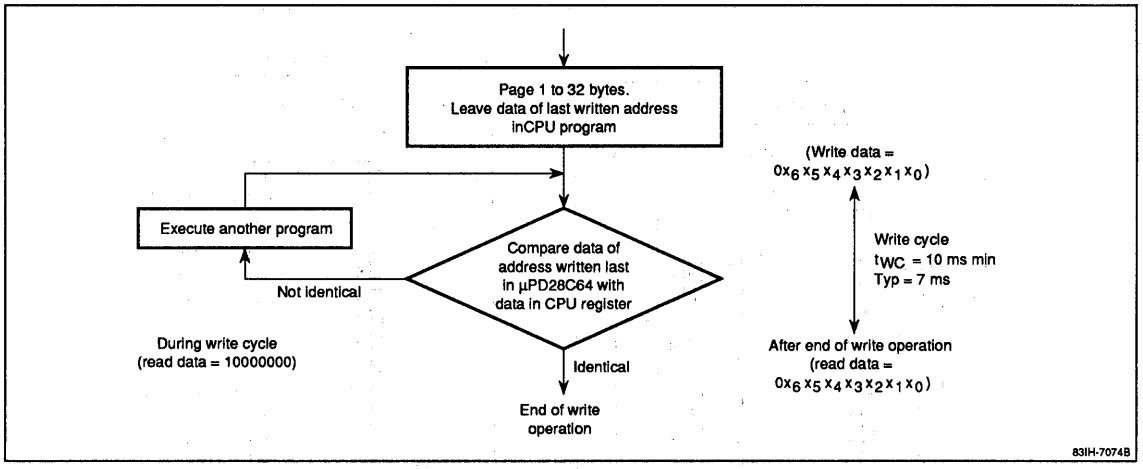
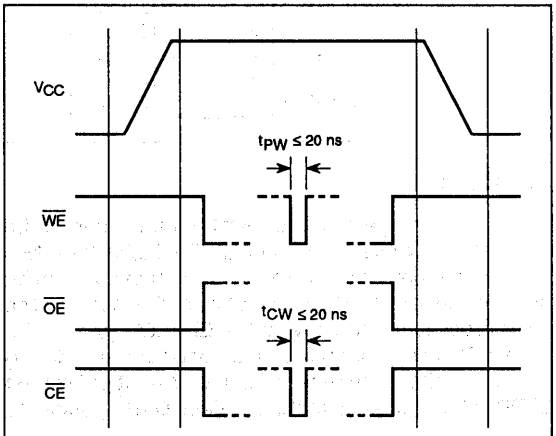
Figure 19. DATA Polling Flow Chart



The microprocessor can execute other instructions and periodically poll the EEPROM to determine if the write cycle is complete. The μD28C64 also includes protection against accidental write cycles at power down (figure 20). For a write cycle to occur, $\overline{WE}$ and $\overline{CE}$ must be asserted low and $\overline{OE}$ must be high. It is unlikely that this combination would occur during power transitions. Additional write protection is provided by a noise immunity filter that inhibits write operation when the $\overline{WE}$ pulse is 20 ns or less, and when the power supply voltage level is detected to be 2.5 volts or less.

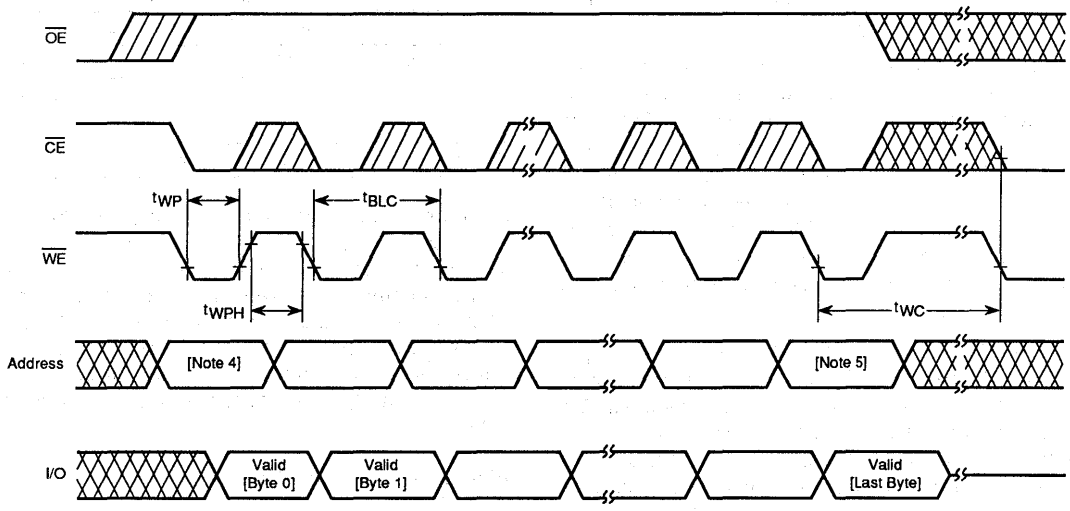
The μPD28C64 optimizes the write cycle with a feature that speeds effective access time when writing a series of 32 bytes simultaneously (figure 20). The 8K x 8-bit device is compatible with the byte-wide pin assignment standard and is pin-compatible with the 8K x 8-bit EPROM and SRAM. While the 8K x 8-bit device is targeted at the larger capacity EEPROM applications, several small devices provide a low-cost solution for low-end systems. The μPD28C04 is such a device and is orgnanized as 256 x 8 bits and provides the same write and protection features as the μPD28C64.

Figure 20. Error Write Protection



Control Terminal			
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	
V_{IH} or V_{IL}	V_{IH} or V_{IL}	V_{IH}	$\overline{WE}$ Write Inhibit
V_{IH} or V_{IL}	V_{IH} or V_{IL}	≤ 20 ns	
V_{IH} or V_{IL}	V_{IL}	V_{IH} or V_{IL}	$\overline{OE}$ Write Inhibit
V_{IH}	V_{IH} or V_{IL}	V_{IH} or V_{IL}	$\overline{CE}$ Write Inhibit
≤ 20 ns	V_{IH} or V_{IL}	V_{IH} or V_{IL}	

Figure 21. μPD28C64 Page Write Cycle



Notes:

[1] The address inputs are latched at the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs later.

[2] The data inputs are latched at the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs earlier.

[3] Write operation requires both $\overline{CE}$ and $\overline{WE}$ to be at V_{IL}. Parameters t_{WP} and t_{CW} are defined only for the period when both $\overline{CE}$ and $\overline{WE}$ are at V_{IL}.

[4] The page cannot be changed in the middle of a page write cycle. Address inputs $A_5 - A_{12}$ must be supplied for every byte load cycle and must remain the same throughout the page write cycle to prevent writing to an unknown address location. Address inputs $A_0 - A_4$ are altered for each byte load cycle and determine the individual byte to be written within the page.

[5] A maximum of 32 bytes may be loaded in a single page write cycle.

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Mask-Programmable ROMs

The ability to erase an EPROM is an important feature, especially during the product development phase when the EPROM code is frequently changed. When the product enters its manufacturing stage and the program code becomes fixed, the extra cost due to the special package with a transparent lid is difficult to justify. Mask-programmable ROMs, which are programmed during the manufacture of the chip itself, are less expensive. NEC produces mask-programmable ROMs and will also manufacture the custom mask required for the device. There is a charge and lead time required for producing the mask, but for high-volume applications, the mask can be amortized with a cost savings compared to the standard EPROM. Typically, the mask-programmable ROM is compatible with the byte-wide standard used in EPROM devices for feature and package compatibility.

One of the disadvantages of the mask-programmable ROM is that if a bug is found in the code, the mask has to be replaced at a large cost. A one-time programmable (OTP) EPROM fills the gap between the standard EPROM in cost and functionality because this product can be programmed like a standard EPROM, but cannot be erased. Since it doesn't have the special EPROM package with transparent lid, the cost is less than an EPROM but higher than a mask-programmable ROM. The mask charge and lead time is eliminated and the parts can be inventoried in their unprogrammed state and programmed just prior to final assembly. Waste caused by program changes is thus minimized, and only one part type is purchased for any number of different programs.

Silicon File

In the past, there has existed a technology gap between the faster primary and the slower secondary memories (figure 22). Average access time of secondary devices, most often magnetic disks and drums, is 1000 to 10,000 times slower than that of primary devices. Electronic disks such as charge-coupled devices and magnetic

bubble memories have not proved cost-effective in closing the technology gap and thus have had little impact on system design.

Standard semiconductor memory in the secondary level is able to bridge this gap, and of the various alternatives, battery backed-up static RAM and EPROM/EEPROM technologies historically have been used in solid-state nonvolatile systems. Typically they have been restricted to low-capacity applications, since the high cost of static RAMs prohibits using them either as replacements for magnetic media or in applications where the operating environment makes rotating media too unreliable.

NEC's μPD42601 silicon file, a device with higher performance, higher capacity, and lower power requirements is also able to bridge this performance gap. The silicon file is based on DRAM technology and provides the capacity and reliability of a standard DRAM, but also features a way to retain data by means of batteries when power is shut off. Although reliability and ruggedness are important attributes of solid-state memories, the silicon file also offers advantages such as lighter weight, higher I/O bandwidth, and simpler interfacing.

The silicon file is an economical mass storage device specifically designed to replace magnetic media in silicon disk, solid-state recording, and system backup applications. It is based on the trench cell technology of NEC's 1M DRAMs and implements the same read and write cycles (figure 23), but optimizes system bandwidth with a page cycle that repeatedly pulses $\overline{CAS}$ while maintaining $\overline{RAS}$ low (figure 24). The silicon file must also periodically execute standard $\overline{RAS}$-only and $\overline{CAS}$ before $\overline{RAS}$ refresh cycles to refresh its cells within a specified interval of 32 ms, which is four times slower than a 1M DRAM.

An important feature of the silicon file is its ability to retain data while being powered by a backup battery. This is accomplished by means of a self-refresh cycle that can be used in applications requiring a low data retention or self-refresh current. The $\overline{RFSH}$ control signal goes low while the $\overline{RAS}$ signal is clocked at a relatively slow rate (t_{RCF}). Since data loss is caused by leakage, and leakage current is a function of temperature, t_{RCF} is specified at three temperature ratings: 50° C, 60°C, and 70°C. Each rating has a corresponding refresh current (directly proportional to the refresh rate) which is required to maintain data (table 2).

Table 2. Self-Refresh Current Versus Clock Frequency and Temperature

Type	Temperature	$\overline{RAS}$ Clock	Maximum Current
μPD42601-60L	0 to 50°C	50 KHz	30 μA
	0 to 60°C	100 KHz	60 μA
	0 to 70°C	200 KHz	120 μA
μPD42601-60	0 to 70°C	200 KHz	120 μA

Self-refresh cycles are intended to be used when power to the silicon file's memory array is shut down for an extended amount of time. In this case, the system backup circuit is required to provide to the memory array a backup supply voltage between 4.5 and 5.5 volts while pulsing $\overline{RAS}$ at the given t_{RCF} frequency and driving $\overline{RFSH}$ low. As long as the circuit can maintain these operating conditions, the silicon file will retain data.

Figure 22. Memory Hierarchy

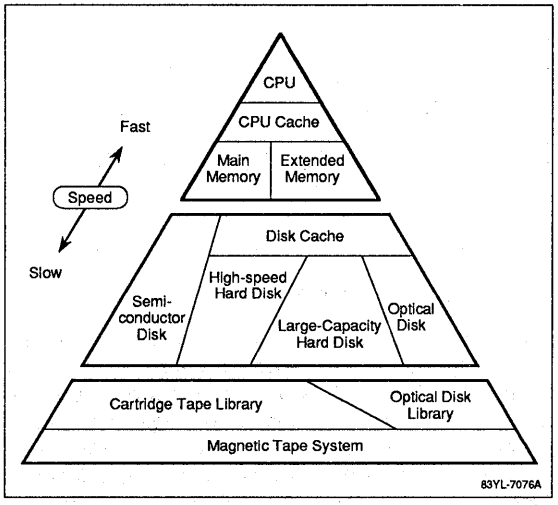

Figure 23. Silicon File Read Cycle

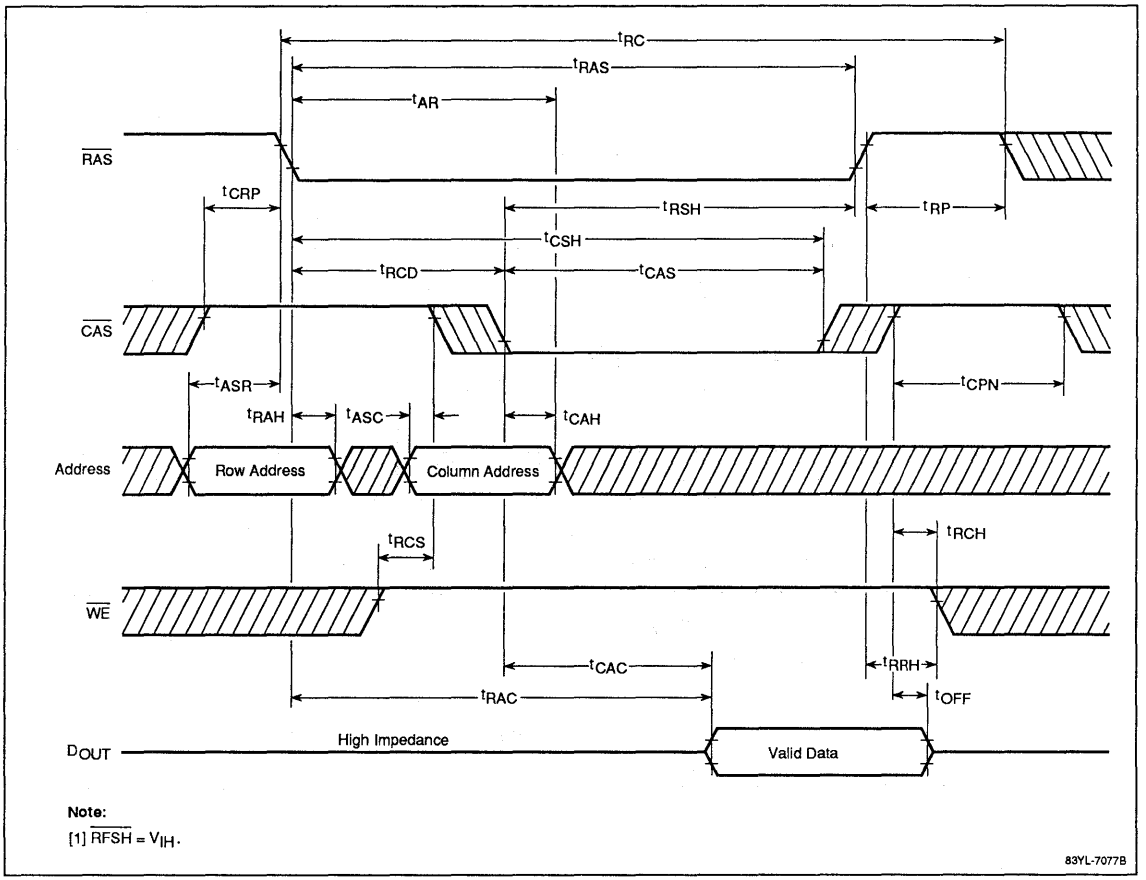

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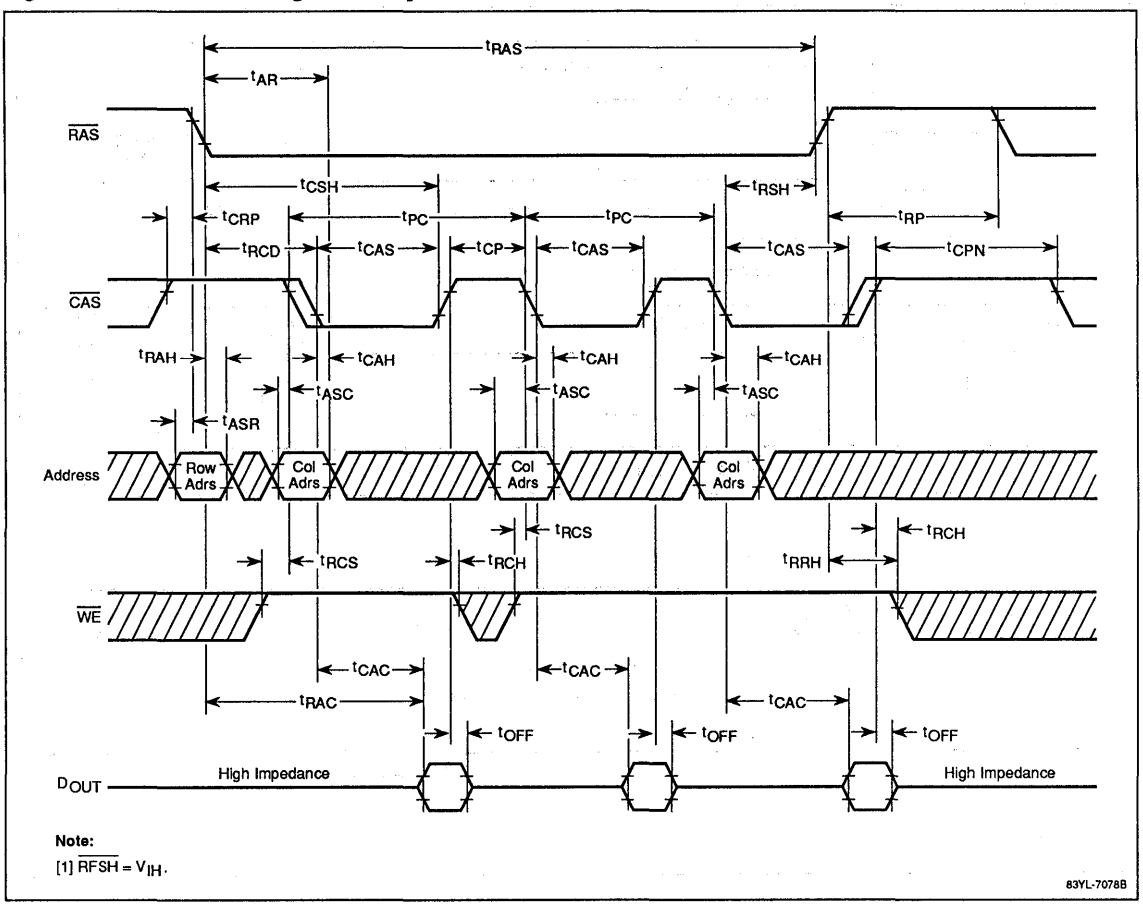
Figure 24. Silicon File Page Read Cycle



Application Note 54
μPD42505 Line Buffer For Communications Systems

Introduction

The current trend in storage devices is toward larger, faster, better-performing products. There is a complementary trend toward the development of storage devices designed for specific purposes. The video buffer is an example of a dedicated device. Line buffers, field (frame) buffers for TV and broadcast equipment, and graphics buffers for computers are examples of video storage devices. Table 1 shows some of NEC's dedicated video buffers.

Table 1. Video Buffers

Function	Product	Storage Configuration	Serial Cycle Time	Application in Video/Optical Systems
Line buffers	μPD42505	5048 x 8	50 or 75 ns	Line storage in facsimile machines, copiers, and scanners
	μPD41101/μPD42101	910 x 8	34 or 69 ns	Double-speed scan conversion for NTSC TV, luma/chroma separation
	μPD41102/μPD42102	1135 x 8	28 or 56 ns	Double-speed scan conversion for PAL TV, luma/chroma separation
Field buffer	μPD42270	263 x 910 x 4	60 ns	Image field storage
Dual-port graphics buffers	μPD41264	64K x 4/256 x 4	40 or 60 ns	High-speed drawing device
	μPD42274/μPD42273	256K x 4/512 x 4	30 or 40 ns	
Triple-port graphics buffer	μPD42232	32K x 8/256K x 1/128 x 8	40 or 60 ns	High-speed drawing/image processing device
Bidirectional data buffer	μPD42532	32K x 8	100 ns	Data transfer rate conversion

This application note introduces the μPD42505, a high-speed serial access device with the same general interface specifications as those of the μPD41101. The μPD42505 was developed specifically for office automation equipment that handles a large amount of data in each horizontal line, equipment such as G3 and G4 digital facsimile machines, high-performance copiers, and image scanners.

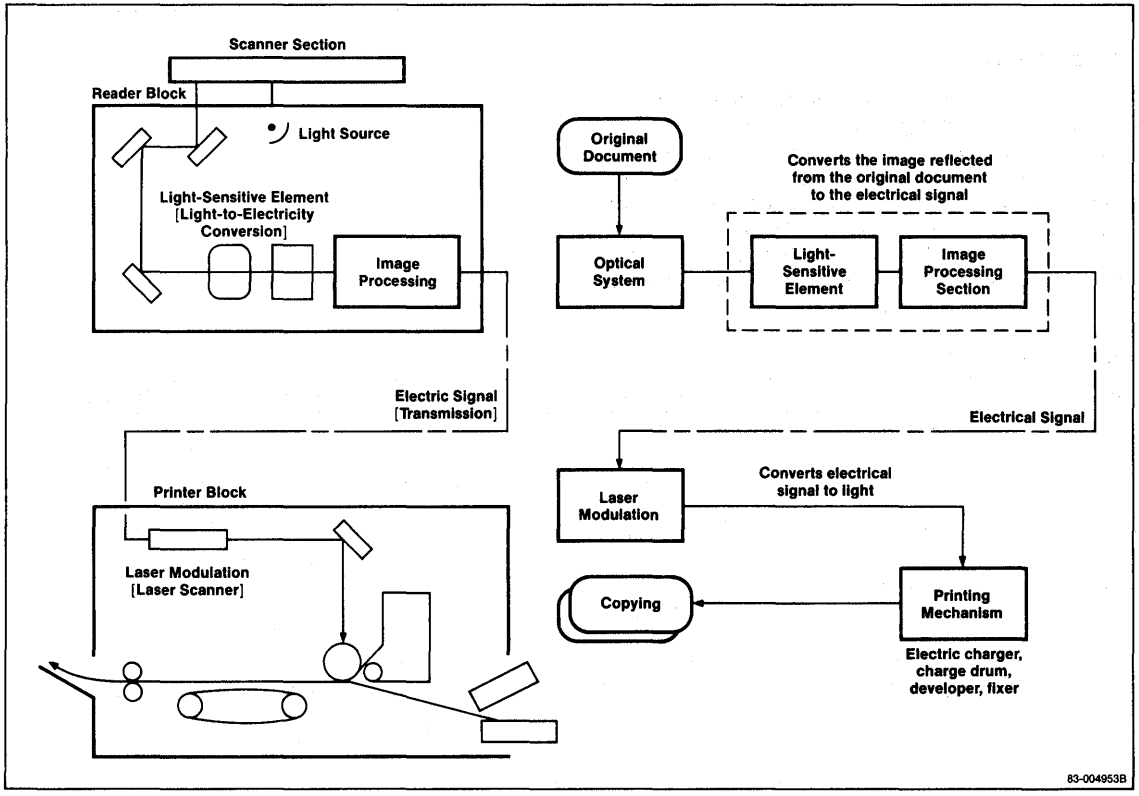
There has been a great deal of technical progress toward higher quality and performance in the development of this image-processing equipment. For example, there are already advances in image quality using two-dimensional filtering, image contraction and expansion, and high-speed video signal transfer. The μPD42505 achieves optimal processing with a storage array of 5048 x 8 bits, and by use of an internal algorithm to read out data in the order in which it was input. The fast cycle time of 50 ns allows the μPD42505 to perform various types of image processing.

Figure 1 shows a typical application for the μPD42505 using a digital copier as an example.

A digital copier mainly consists of a reader and a printer section. The image reflected from the original document placed in the scanner section is input to an image sensor (e.g., a CCD or contact-type image sensor) and photoelectrically converted to a digital signal. The digital signal is then input to the image processing section for image quality improvement and processing. The electronic image signal processed in the reader block is sent to the printer block, converted to light in the laser modulation section, developed, fixed, and printed out. If a communication facility is added to this copier, it can function as a facsimile machine.

Digital copiers and facsimile machines configured in this way can use dedicated video buffers in the image processing or transmission section.

Figure 1. Configuration and Data Flow in a Digital Copier

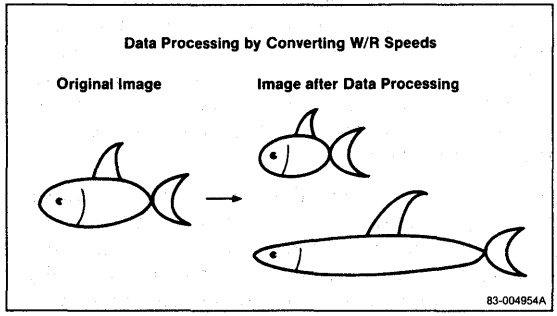


Uses for the μPD42505

The following discussion describes the types of applications for which the μPD42505 was developed: frequency (speed) conversion, a data delay line for one horizontal scanning line, and buffering for data transfer operations in a simple configuration with simple control.

Consider the need for a device that asynchronously converts the read and write speed for frequency conversion, e.g., a serial access device used for image contraction or expansion, with a word length of one to two horizontal lines. The buffer must be written to and read from asynchronously and at different rates. High speed is also a requirement. Figure 2 illustrates a frequency conversion application.

Figure 2. Frequency Conversion



Another application might require a data delay line with a delay length of one to two lines. This type of buffer could be used for image quality improvement in two-dimensional filtering, especially for filtering in the vertical direction, because it could be written to and read from simultaneously in synchronization with a single clock signal. Figure 3 illustrates two-dimensional filtering.

A third application is a buffer for data transfer operations. This application requires a device large enough to store the amount of data handled, with the capability to read and write asynchronously, simultaneously, and at different speeds. An output such as a flag to indicate the amount of data in the storage array might also be required. Figure 4 illustrates buffering for data transfer.

Figure 3. Two-Dimensional Filtering

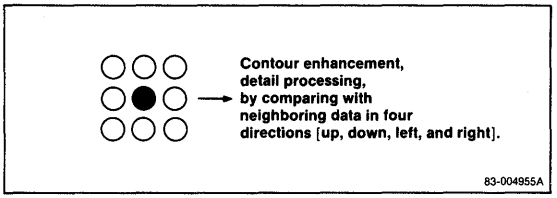
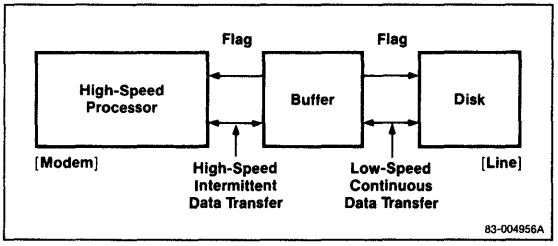


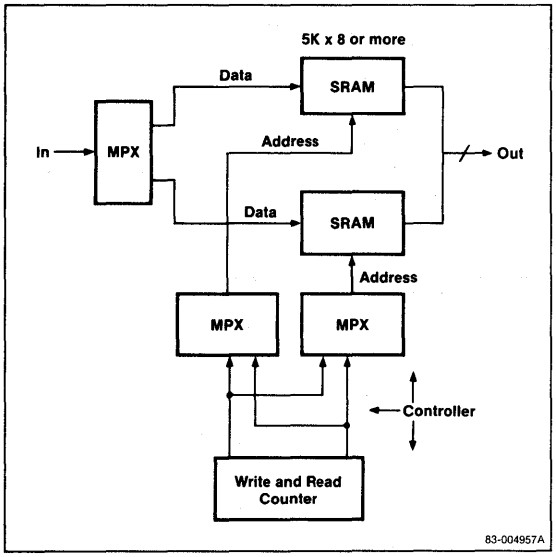
Figure 4. Data Transfer Buffering



These applications typically require a double-buffer configuration using high-speed SRAMs for data storage in bits, as shown in figure 5.

In the first phase, data is written to the first SRAM while data in the second SRAM is read simultaneously, alternating operations between the two SRAMs. However, this operation requires components such as read and write address counters, a multiplexer to switch address signals according to the read and write state of each device, a multiplexer to switch write data input and read data output, and a sophisticated controller to control the SRAMs and the other components. The μPD42505, by performing some of these functions itself, considerably simplifies these applications.

Figure 5. Typical System Using High-Speed SRAMs



Features of the μPD42505

The μPD42505 is a 5048-word x 8-bit high-speed serial access device that uses 1.5-μm CMOS processing and dual-port storage cell circuits allowing simultaneous, asynchronous read and write cycles at different speeds. An internal algorithm makes an external address signal unnecessary.

Read and write operations are fully and independently controlled by their own set of control signals. The storage array length of 5048 words meets the size required to sample one line of JIS A3-size paper on the shorter side (297 mm) with a sampling rate of 16 dots/mm (400 dots/in). On the longer side (418 mm), the sampling rate is 12 dots/mm (300 dots/in). The μPD42505 can easily process document data for each line. The configuration of 8 bits to 1 word corresponds to the number of bits for one sampling point, which allows the device to process natural-looking images.

The μPD42505 can be used in video applications that require high-speed processing because of its minimum simultaneous write/read cycle time of 50 ns and maximum access time of 40 ns. For example, the cycle time of 50 ns is fast enough to digitally process an NTSC or PAL composite video signal at a sampling rate of four times the color subcarrier frequency ($4f_{SC}$).

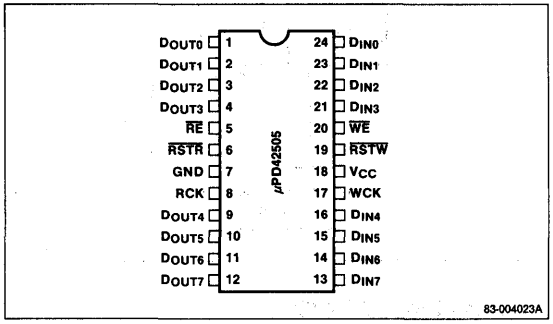
The μPD42505 is particularly suitable for use as a digital delay line with a delay length of up to 5048 cycles in one-cycle steps. The device is mounted in a 300-mil, 24-pin plastic slim DIP. The 300-mil width allows high-density mounting.

μPD42505 Pinout

Pins 1 through 12 control read operation (D_{OUT0}-D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK) and the GND pin. Pins 13 through 24 control write operation (D_{IN0}-D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK) and the power supply (V_{CC}).

$\overline{RSTW}$ and $\overline{RSTR}$ are control signal inputs that reset the internal read and write address pointers to starting address 0. These pins are useful for initializing the chip after power-on or for returning the address to 0.

Figure 6. μPD42505 Pin Configuration



$\overline{WE}$ and $\overline{RE}$ are control signals that enable (low) or disable (high) write and read operation. When $\overline{WE}$ is high, write operation is disabled and the write address stops at the current value. When $\overline{RE}$ is high, read operation is disabled, the read address stops at the current value, and the output goes to high impedance. $\overline{WE}$ and $\overline{RE}$ may be input at any time, but they are latched in each cycle at the rising edge of WCK or RCK, respectively.

WCK and RCK are the write and read system clock inputs. One write or read cycle is executed in synchronization with each WCK or RCK input when $\overline{WE}$ or $\overline{RE}$ is low. The write or read address is incremented internally in single steps and wraps around automatically from 5047 to 0.

D_{IN0}-D_{IN7} are the write data input pins. Write data is clocked into the chip at the rising edge at the end of the WCK cycle. D_{OUT0}-D_{OUT7} are the read data output pins. Read data is output when the access time has elapsed from the rising edge at the beginning of the RCK cycle.

Read and Write Timing

Input a low-level signal to $\overline{RSTW}$ (for writing) or $\overline{RSTR}$ (for reading) to satisfy the setup and hold times measured from the rising edge at the beginning of the WCK or RCK cycle. This returns the cycle to starting address 0. Figure 7 shows read and write timing for the μPD42505.

As the figure shows, the $\overline{RSTW}$ or $\overline{RSTR}$ signal can end in one write or read cycle or can be repeated for successive write or read cycles. Repeating the reset cycle holds the address at 0. The address is incremented to address 1 only in a cycle when $\overline{RSTW}$ or $\overline{RSTR}$ is set high at the rising edge of the WCK (RCK) cycle. For write reset, the write data clocked in the last reset cycle is written to address 0. For read reset, the data in address 0 is output continuously. After the reset, write or read operation continues as the address is incremented by 1 for each cycle in synchronization with its appropriate clock. When the internal address reaches 5,047 (i.e., when write or read cycles are executed 5,048 times), the address returns to address 0 and the write or read operation starts over at that point.

Speed Conversion. Independently controlling the read and write operations of the μPD42505 allows you to perform speed conversion. For example, when the read and write addresses are initialized by $\overline{RSTW}$ and $\overline{RSTR}$, data is written in synchronization with WCK and the write data is written to the chip from device address 0. Data written can be read out from address 0. In this case, the reset signal input timing and the clock signal speed (cycle time) can be independently controlled for read and write operation. The μPD42505 can be used for speed (frequency or time axis) conversion by outputting the data previously input with an arbitrary drive frequency and time at a different drive frequency and time.

Digital Delay Line. To use the μPD42505 as a digital delay line, input the same clock to WCK and RCK and reset the read and write cycles in parallel. Written data is read out after 5,048 cycles to provide a 5,048-cycle digital delay line.

There are three ways to control the delay length:

- By controlling the $\overline{WE}$ and $\overline{RE}$ signals
- By inputting $\overline{RSTW}$ and $\overline{RSTR}$ at different times (the delay length is determined by the offset between the signals)
- By changing the reset signal interval when $\overline{RSTW}$ and $\overline{RSTR}$ are concurrently controlled (the delay length is determined by the reset signal input interval)

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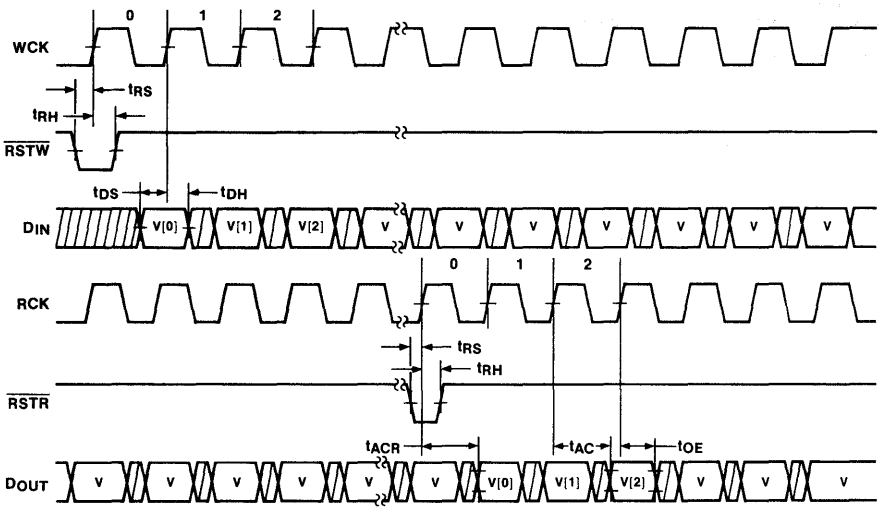
Figure 7. Read and Write Timing



Notes:
[1] $\overline{WE} = \overline{RE} = V_{IL}$.
[2] V = Valid data.

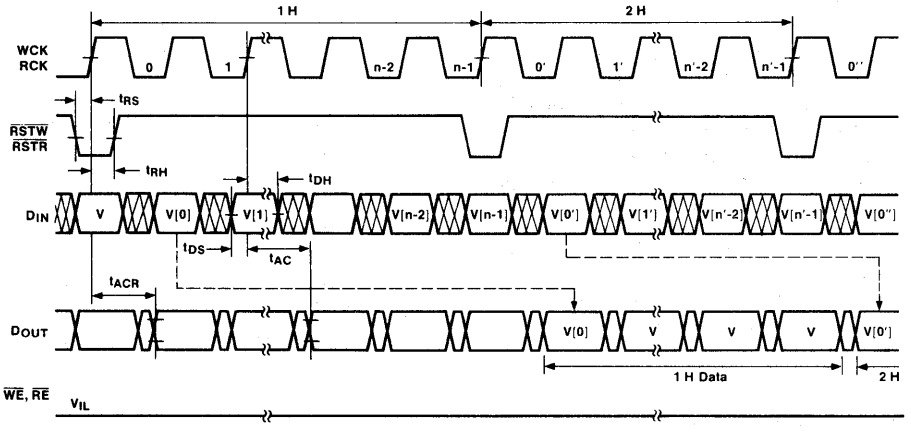
83-004958B

The delay length can be changed in one-cycle steps by controlling $\overline{WE}$ and $\overline{RE}$. When $\overline{WE}$ and $\overline{RE}$ are high, write and read operation is disabled. The write and read addresses remain where they were when the operations were disabled, regardless of WCK and RCK.

When $\overline{RSTW}$ and $\overline{RSTR}$ are used to control the delay length, the data written at address 0 when $\overline{RSTW}$ is input is read out from address 0 when $\overline{RSTR}$ is next input. The offset between $\overline{RSTW}$ and $\overline{RSTR}$ determines the delay length.

In the third method, changing the reset signal input interval, the same signal is used for WCK and RCK so that $\overline{RSTW}$ and $\overline{RSTR}$ are controlled together. The data, written after a reset signal, is read out after the next reset signal in the order it was written. This interval determines the delay length. For example, if the reset signal is input every 4,800 cycles, the delay length is 4,800 cycles. Figure 8 shows the timing for this method.

Figure 8. Controlling Delay Length with the Reset Interval



Note:
[1] V = Valid Data.
[2] 1H = the first group of n bits. 2H = the second group of n'bits.

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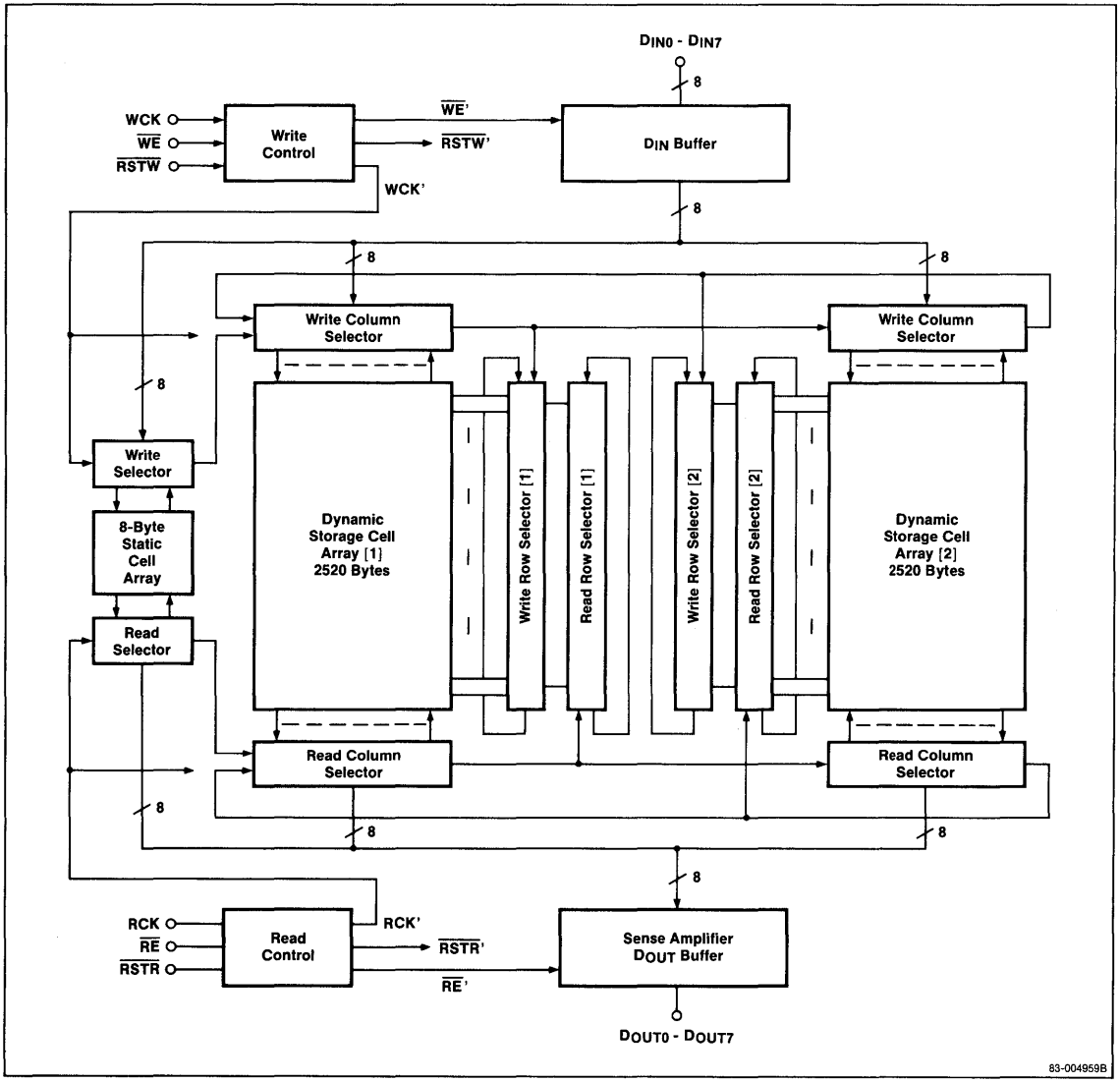
Functional Blocks

The write data input from pins D_{IN0}-D_{IN7} goes through the D_{IN} buffer and is serially written to either a static cell in an 8-byte configuration, or a dynamic cell in a 5,040-byte configuration, one byte (8 bits) at a time, in synchronization with WCK. The data read out from these cells is serially output from the D_{OUT} pins through the sense amplifier and the D_{OUT} buffer, one byte at a time, in synchronization with RCK. The read and write control circuits control these operations.

Figure 9. μPD42505 Block Diagram



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Storage Cells

The μPD42505 uses dual-port storage cells to allow read and write cycles to be executed asynchronously and at different speeds. Figure 10 shows a circuit diagram of a static dual-port storage cell, and figure 11 shows a dynamic dual-port storage cell.

In the static cell, read and write data are input as a differential signal so that it can operate at a higher speed. The circuit size is larger because it requires more components.

Figure 10. Static Dual-Port Storage Cell

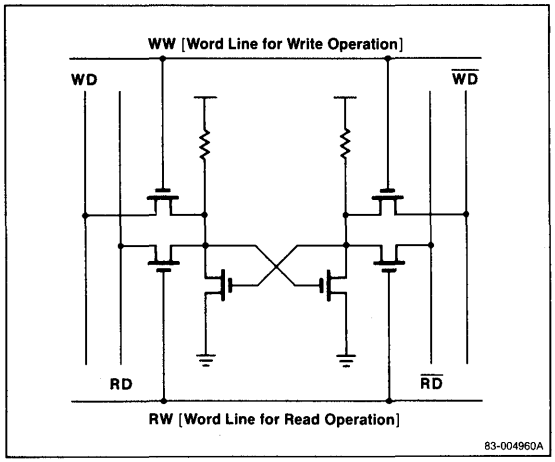
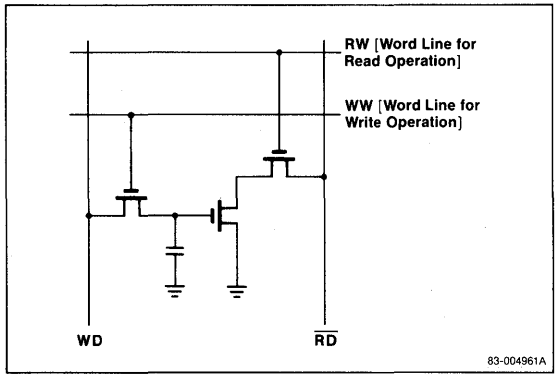


Figure 11. Dynamic Dual-Port Storage Cell



The dynamic cell has only one bit line for read operation and one for write operation. It requires a longer data sense phase, reducing the speed. However, it can be configured with fewer components.

Both types of cells are used in the μPD42505 to exploit the advantages of each. Other than initializing the internal address pointer to the starting address with the reset signal, the μPD42505 is configured so that the internal address is incremented one bit at a time and data is serially accessed. After a reset operation (immediately changing the addressing sequence), a static dual-port storage cell that can operate at higher speed is accessed. Simultaneously or subsequently, a dynamic cell is used as a pipeline, allowing both types of cells to be accessed at high speed.

Pipeline operation refers to an instance where the word line (row) to be selected next is set to the selected level in advance, so that it can be written or read at high speed in the time required to select a column in dynamic static-column mode.

Shift registers are used as read and write column and row selectors to enable the sequential selection of write or read addresses in pipeline processing.

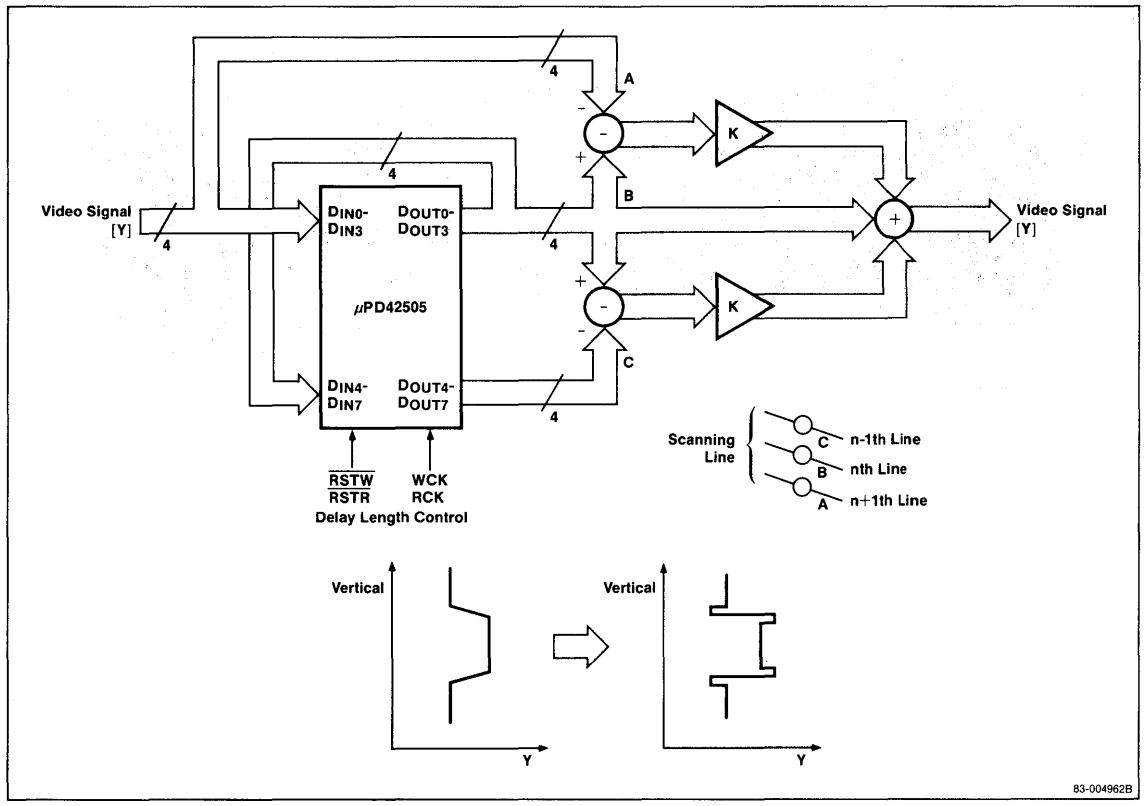
Applications

Signal processing technology aims toward higher quality in the development of digital copiers and facsimile machines. As examples, consider image quality improvement processing such as the adaptive bilevel control technique, which produces a stable and accurate binarization regardless of the original document type, and the two-dimensional equalizing filter, which corrects fading in photoelectric signal conversion. The μPD42505 fits easily into these processes. It can also reduce system size and cost.

Two-Dimensional Filter

In handling an image with half-tones, e.g., a photograph, there is some deterioration in the image quality, such as thin lines and small characters fading out; fading is usually caused by the lens or photoelectric signal conversion system in a CCD sensor. A two-dimensional filter is very effective in enhancing contours where contrast changes sharply and in reducing the fading problems. Figure 12 shows a contour enhancement circuit.

Figure 12. Contour Enhancement Circuit



In this example, the video input is handled as a 4-bit signal so that a circuit with a delay length equal to two scanning lines can be configured with a single μPD42505. Adding adders or subtractors and multipliers to the μPD42505 completes the contour enhancement configuration.

The video signal of the n+1th line (delayed by one scanning line) is input to D_{IN0}-D_{IN3} and output from D_{OUT0}-D_{OUT3} as the nth line. Applying this output directly to D_{IN4}-D_{IN7} delays the video signal another scanning line before it is output from D_{OUT4}-D_{OUT7} as the n−1th line. There is a delay of one scanning line between the signal input to D_{IN0}-D_{IN3} and the signal output from D_{OUT0}-D_{OUT3}, and a delay of another scanning line between the signal input to D_{IN4}-D_{IN7} and the signal output from D_{OUT4}-D_{OUT7}. Processing these signals in the adders and multipliers provides contour enhancement in the vertical direction. You can control the delay length by controlling the reset signals ($\overline{RSTW}$ and $\overline{RSTR}$) and the clock signals (WCK and RCK) in common, and by controlling the reset signal input interval.

The delay length of one scanning line is used in various applications for two-dimensional data processing. The μPD42505 can also be used in applications such as VTR jitter compensation (time axis variation) caused by the variance in head drum rotation rate or the expansion or shrinkage of the tape, applications requiring variable-length delay lines to contract or expand a video image in the horizontal direction, applications involving the synchronization of two or more digital signal inputs, and as a line buffer in data transfer operations between devices using different data transfer rates.

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Figure 13. μPD42505 5048 x 8 Line Buffer

Introduction

The μPD41101 and μPD41102 are high-speed serial access line buffers organized as 910 words x 8 bits and as 1135 words x 8 bits, respectively. An algorithm that enables data to be read out in the order in which it was input makes these devices suitable for use as data delay lines or for converting data transfer rates, e.g., as buffer storage used for data transfer between devices with different data processing rates.

The μPD41101 can process an NTSC composite video signal (the TV system used in Japan and North America) that has been previously digitized. The fast access times of the device allow a sampling frequency of four times the color signal subcarrier frequency (where f_{SC} = 3.58 MHz and $4f_{SC}$ = 14.32 MHz) for each scanning line to be used. This means that 910 addresses are required for each scanning line when sampling at $4f_{SC}$.

The μPD41102 can process a PAL composite video signal (the TV system used in European countries other than France) that has been previously digitized. This device also uses a sampling frequency of four times the color signal subcarrier frequency (where f_{SC} = 4.43 MHz and $4f_{SC}$ = 17.72 MHz) for each scanning line, which means that 1135 addresses are required for each scanning line when sampling at $4f_{SC}$.

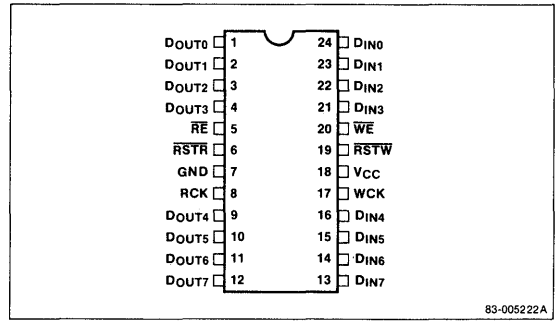
Figure 1 shows the pin configuration for these devices. The D_{IN0}-D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK pins control write operation, while D_{OUT0}-D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK control read operation. The pins are organized to operate asynchronously and at different speeds simultaneously. A built-in serial address generator automatically generates read and write addresses so that an address need not be supplied externally.

High-Speed Operation

Write and Read Operation

Write and read cycles are executed identically. One address of data (8 bits) is written or read in one cycle in synchronization with WCK or RCK when $\overline{WE}$ or $\overline{RE}$ is low. The write or read address is incremented by 1 at the falling edge of each write or read clock. Write data must satisfy setup and hold times as measured from the rising edge of WCK.

Figure 1. Pin Configuration



The $\overline{RSTW}$ and $\overline{RSTR}$ reset signals initialize the write and read address pointers to 0. A reset signal must be input to satisfy the setup and hold times as measured from the rising edge of WCK or RCK. Once the address is initialized, a write or read cycle is executed in synchronization with its respective clock and the pointer is incremented by 1. In the μPD41101, the pointer returns to 0 after address 909. In the μPD41102, the pointer returns to 0 after address 1134.

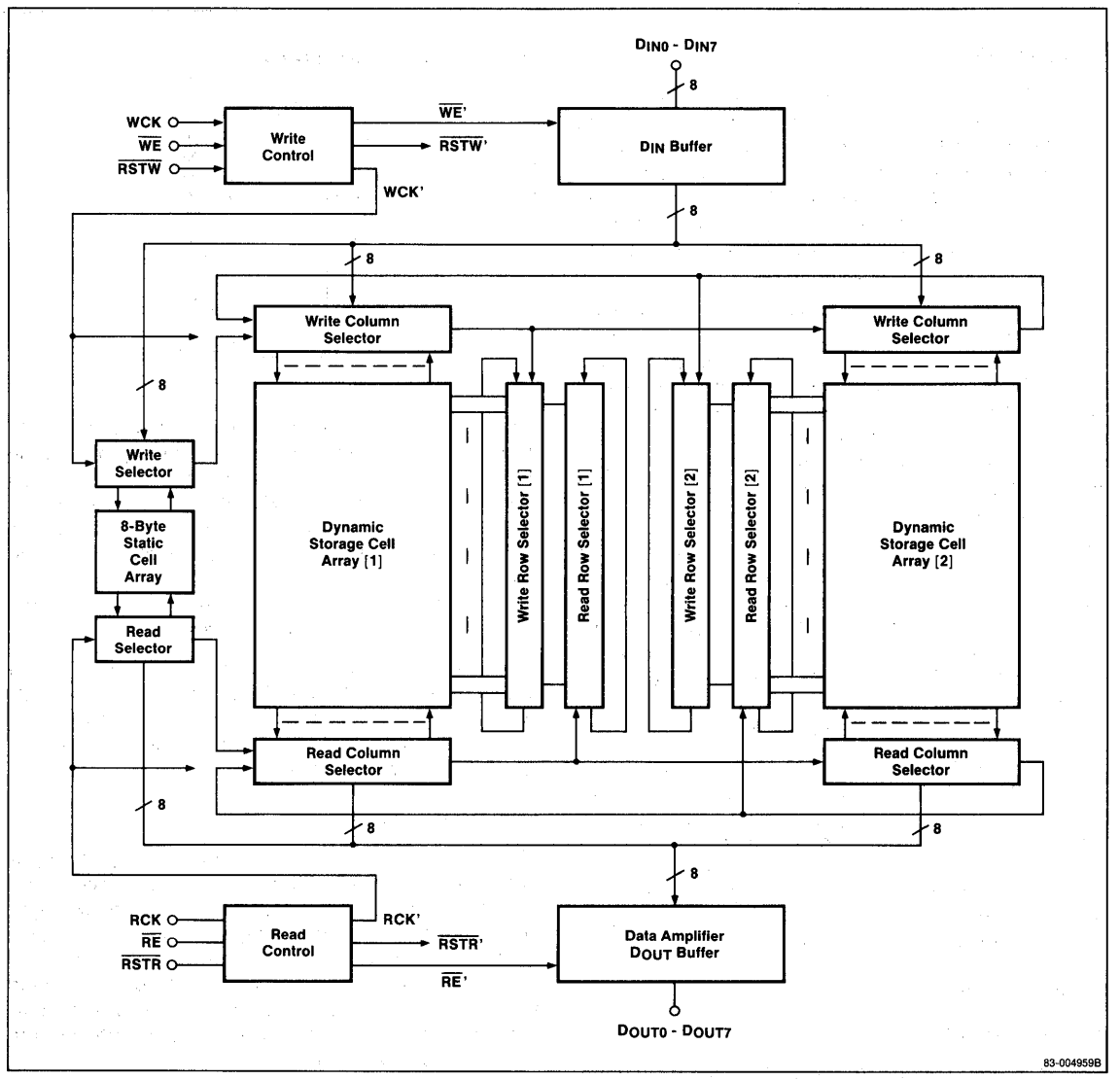
When $\overline{WE}$ is high, write operation is disabled and the line address is held regardless of the status of WCK. When $\overline{RE}$ is high, read operation is disabled, the output goes to high impedance, and the line address is held regardless of the status of RCK.

Functional Blocks

The write data from D_{IN0}-D_{IN7} goes through an input buffer and is serially written to either a static cell in an 8-byte configuration, or a dynamic cell in an 1136-byte configuration, one byte (8 bits) at a time, in synchronization with WCK. The data read from these cells is serially output from the D_{OUT} pins through a sense amplifier and the output buffer, one byte at a time, in synchronization with RCK. The read and write circuits control these operations.

WCK, $\overline{WE}$, and $\overline{RSTW}$ are input to the write control circuit. RCK, $\overline{RE}$, and $\overline{RSTR}$ are input to the read control circuit. These segments are composed of simple gate circuits (figure 2).

Figure 2. Block Diagram of the μPD41101 and μPD41102



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Storage Cells

The μPD41101 and μPD41102 use dual-port storage cells to execute read and write cycles asynchronously and at different speeds (figures 3 and 4).

Static Cell Organization. In the static cell, two pairs of transfer gates (one pair each for read and write operation) are connected to the flip-flop in the middle. The other end is connected to a pair of bit lines for read operation (RD, $\overline{RD}$), and another pair for write operation (WD, $\overline{WD}$). One word line each for RW and WW are connected to the transfer gate pins.

When the word line for a write cycle (WW) goes to the selected level, and write data is applied to the pair of bit lines (WD, $\overline{WD}$) of the selected column, a write cycle is executed on the cell where the row (word line) and column (bit line) intersect.

A read cycle is executed independently. When the word line goes to the selected level (RW), data is transferred to the bit line pair (RD, $\overline{RD}$) through a transfer gate. Data is selected by the column signal and read externally. Data in the storage cell at the intersection of the selected row and column is also read.

Read and write data are input as a differential signal so that the static dual-port cell can operate at a higher speed. The circuit size is larger because it requires more components.

Dynamic Cell Organization. Each dynamic array in the μPD41101 and μPD41102 consists of two subarrays with 71 rows apiece. Each row of the subarray consists of 8 (number of bits) x 8 addresses (bytes). Each row of each subarray therefore has 8 subword lines. Figure 5 shows the organization of a dynamic array.

Figure 3. Dual-Port Static Storage Cell

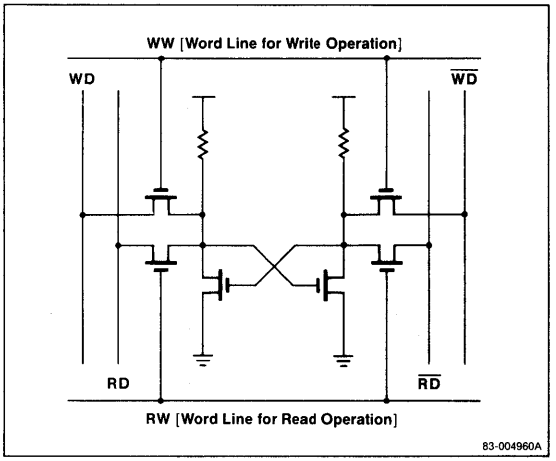
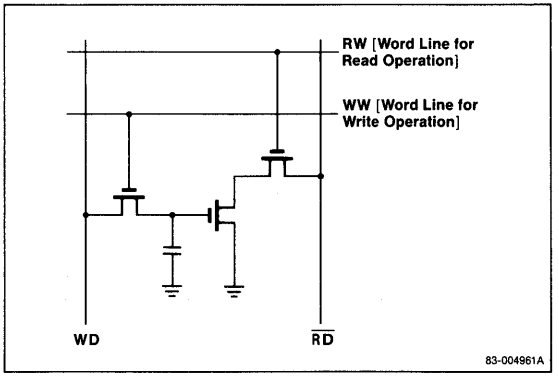
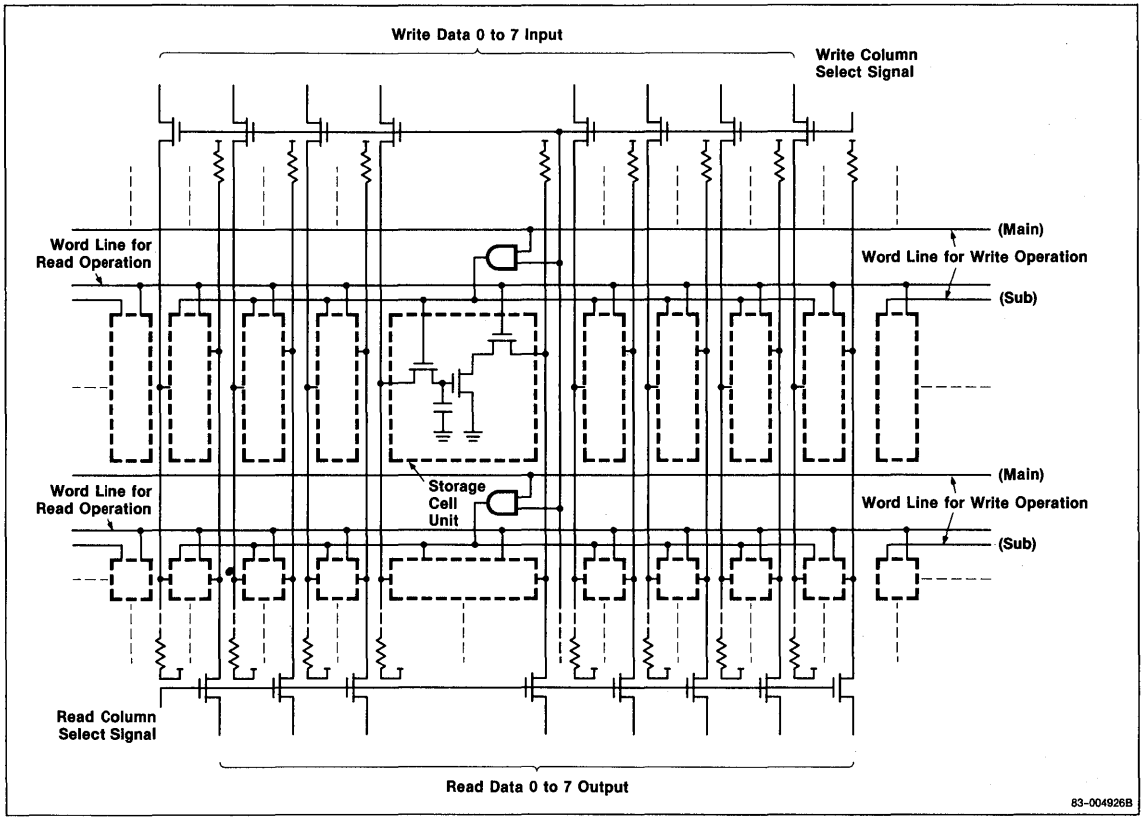


Figure 4. Dual-Port Dynamic Storage Cell



28c

Figure 5. Organization of Dynamic Storage Array



The dynamic cell has only one bit line for each read ($\overline{RD}$) and write (WD) operation, one word line for each read (RW) and write (WW) operation, three transistors, and one capacitor. Although the longer data sense phase reduces its speed, a dynamic cell can be configured with fewer components and used for high-density integration.

In a write cycle, write data input through the bit line (WD) is guided through a transfer gate made conductive by the word line (WW). The gate charges or discharges the storage capacitor.

In a read cycle, the transistor with the gate connected to one end of the storage capacitor is turned on or off depending on whether or not the capacitor is charged. Data is transferred to the bit line ($\overline{RD}$) through the transfer gate, made conductive by the word line (RW), and then read externally. Word and bit lines for each operation are independent of each other so that read and write cycles can be executed asynchronously.

Data Transfer

The μPD41101 and μPD41102 are configured so that the internal address is incremented one bit at a time and data is accessed serially. After a reset signal initializes the device, a static cell that can operate at higher speed is accessed. Simultaneously or later, a dynamic cell is used as a pipeline, allowing access to both types of cells at high speed.

Stored information is defined by the state of the storage capacitor. When the word line for the write cycle goes to a selected level, the write transfer gate of each storage cell connected to the word line becomes conductive, and the data (electrical level) given to the bit line is rewritten to the capacitor connected to the end of the transfer gate. The precharge level of the write bit line (typically a high level) is rewritten to the storage cells on the selected word line, other than the one to which the column signal applies data, thereby destroying data stored there.

The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

The μPD41101 and μPD41102 prevent this destruction of data by using a main word line and a subword line. The subword line is driven by the ANDed signals of the main word line and the write column. The transfer gate of each cell corresponding to each address is connected to a subword line. Therefore, the write word line of the storage cells at the selected row and column address is the only one which goes to a high level, preventing the destruction of data in other cells on the same write line.

Address Selection

A dynamic storage array consists of subarrays 1 and 2, each of which is 568 (71 x 8) bytes. A column selector and a row selector circuit are provided for independent read and write operation for each subarray.

The first step of address selection involves the accessing of an 8-byte static cell immediately after a reset cycle. The address selector moves to the first row of the subarray, and subarray 1 is accessed from left to right, one byte at a time. When 8 bytes of subarray 1 have been accessed, the address selector moves to the first row of subarray 2, also accessed from left to right, one byte at a time. When 8 bytes of subarray 2 have been accessed, the address selector alternately selects 8 bytes from addresses in both subarrays, so that rows are selected from the higher row to the lower row.

When the number of access cycles to the static cell array (8 addresses) and the dynamic cell array reaches 910 (for the μPD41101) or 1135 (for the μPD41102), the pointer moves to address 0 of the static array.

This method of sequential address selection increases the access speed of the dynamic cell by selecting row addresses in the pipeline method. Pipeline operation occurs when the word line (row) to be selected next is set to the selected level in advance so that it can be written or read at high speed, i.e., in the time required to select one column in static-column mode.

After a reset cycle, when 8 bytes of the static cell are being accessed, the first row of subarray 1, which is accessed next, is set to the selected level in advance. When the selected address moves to the first row of subarray 1 (after 8 bytes of static storage are accessed), a read or write cycle can be executed at high speed for that row. The first row of subarray 1 can be accessed at high speed even after the static array is selected. This process continues with the first row of subarray 2, the second row of subarray 1, and so on.

While the static cell is being accessed immediately after a reset cycle, the address on the dynamic cell is held on the first column and row of subarray 1. The dynamic array is not accessed at this time. Pipeline operation is performed independently for write and read cycles by the row and column selectors for each subarray.

Shift registers are used as read and write column and row selectors for the sequential selection of write or read addresses and pipeline processing. Shift registers are provided for each column and row, and each node level is set in advance so that when reset, each shift register outputs a high signal for the first column or row and a low signal for other columns or rows.

The column selector (shift register) is driven by WCK or RCK and the address is incremented by 1 for each clock cycle, i.e., the node that outputs a high signal changes in synchronization with the clock, and the column selector changes with it.

The row selector (shift register) is related to pipeline control and is driven by the pulse generated when the column address selector moves from subarray 1 to subarray 2 or vice versa. The row selector is incremented by one row address after the change from one subarray to another.

Each shift register used as a column or row selector is configured as a ring counter so that when the last column or row is reached, it automatically returns to the first column or row.

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Applications

For the most part, the applications described below pertain to noninterlaced digital TV. The descriptions apply to NTSC systems, unless otherwise specified.

Comb Filter

A composite TV signal (output of a TV tuner) is the sum of the luminance (Y) and chrominance (R-Y, B-Y) color signals. The Y, R-Y, and B-Y signals must be separated, and the R, G, and B signals input to the picture tube generated from them.

A comb filter with line buffers derives the color or luminance signal by cancelling it from the composite signal, using the correlation between neighboring lines. This filtering fully separates the color and luminance signals, especially when there is a strong correlation between lines, to produce a clear picture.

If the signals are not well separated, the color signal may interfere with the luminance signal and cause dot crawl. The luminance signal may also interfere with the color signal and cause cross-color. This interference degrades the picture quality, especially where color or luminance changes sharply. Figure 6 shows a typical comb filter using line correlation.

This example compares target line B with neighboring lines A and C. Two μPD41101s are used as 910-bit delay lines. The color signal (C = R-Y, B-Y) is separated by subtracting the data of the upper and lower lines (A + C) from the target line data (B) and filtering the separated signal through the 3.58-MHz bandpass filter. The luminance signal is the result of subtracting the separate color signal from the original data (B). See the description of the "Variable-Length Delay Line" application for information on controlling a delay line of 910 bits or less.

Double-Speed Scan Conversion

The current NTSC and PAL TV systems use interlaced scanning to eliminate the flickering caused by field transition. Scanning is performed every two lines, reducing the pixel density and doubling the field frequency (number of fields-per-second), as illustrated in figure 7.

In interlaced scanning in the NTSC system, a complete frame consists of two fields of 262.5 scanning lines each. The field frequency is 60 Hz, i.e., the sum of 30 first fields-per-second and 30 second fields-per-second. In the PAL system, a complete frame is comprised of two fields of 312.5 scanning lines each. The field frequency is 50 Hz, the sum of 25 first fields-per-second and 25 second fields-per-second. In both cases, interlaced scanning reduces the flicker in motion scenes caused by field transition. The pixel density in the vertical direction is also reduced, diminishing the level of detail.

Figure 6. Interline Y/C Separation with a Comb Filter

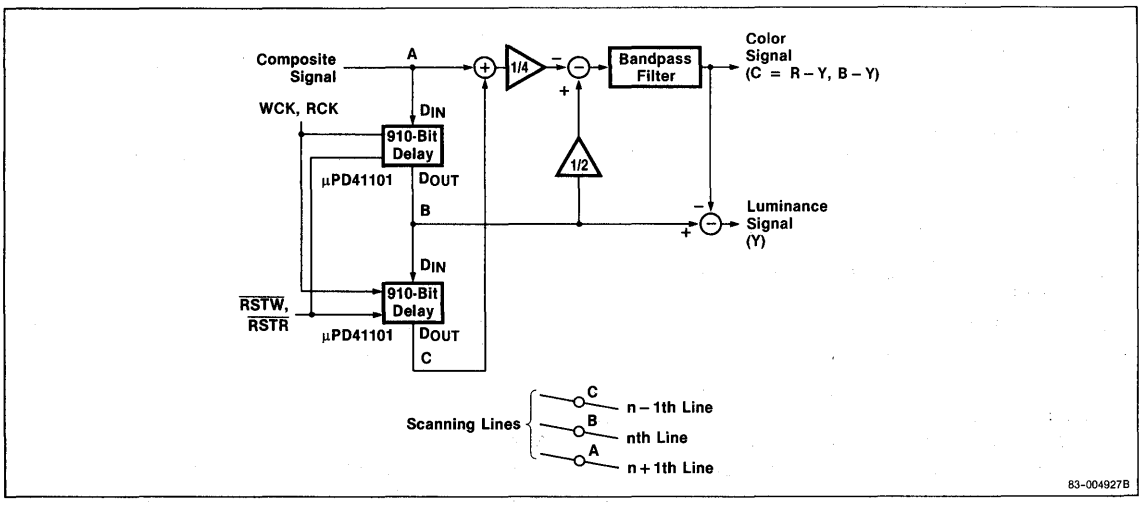
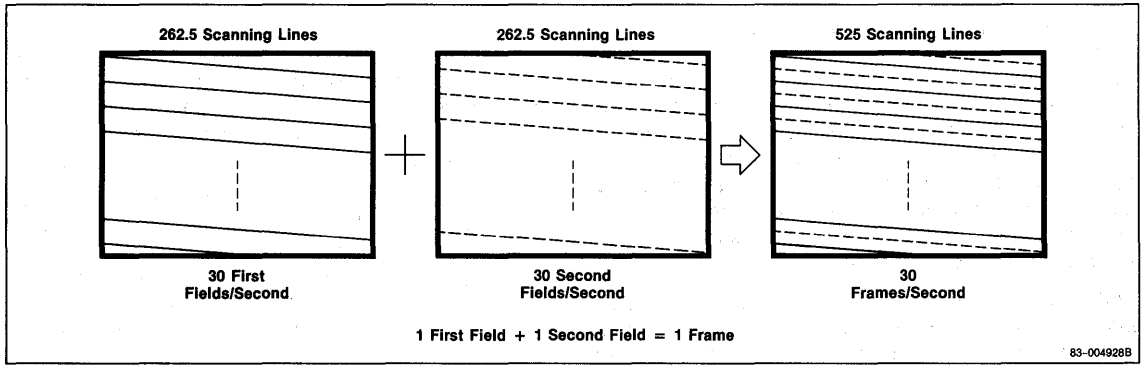


Figure 7. Relationship of Field to Frame in NTSC Systems



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

The μPD41101 or μPD41102 can be used to convert interlaced scanning to noninterlaced scanning. Doubling the pixel density (number of scanning lines) in the vertical direction without changing the field frequency produces clear and precise images (figure 8). In interlaced scanning, the first field of solid lines and the second field of broken lines are scanned alternately at 30 fields-per-second (25 fields-per-second in PAL). In noninterlaced scanning, the number of scanning lines per field is doubled, and 60 fields-per-second are scanned (50 fields-per-second in PAL).

In noninterlaced scanning, the data of the skipped line is created using the buffer. It is read at twice the sampling frequency of interlaced scanning (8 f_{SC} if the interlaced sampling rate is 4 f_{SC}). Noninterlaced scanning scans two lines in the time that one line is scanned in interlaced scanning. The horizontal frequency of the CRT must also be doubled for noninterlaced scanning.

The data of the skipped line can be created

- Using the data of the previous line (reading out the same data twice)
- Using the average value of the lines before and after the skipped line
- Using data that is one-field-old (the data for 262 lines before for NTSC, or 312 lines before for PAL)

In the first option, one μPD41101 (or one μPD41102 for PAL) is used for one input signal. The data is written at 4 f_{SC} and read out at 8 f_{SC}. Reading starts when data is written to half of the line (455 bytes). The same data is read twice (910 bytes x 2) at 8 f_{SC}. Data read in the latter half is used as interpolated data (figure 9).

In the second method, one μPD41101 delays the data of one line, and two μPD41101s convert the current data and the interpolated data for double-speed scanning.

Figure 8. Interlaced and Noninterlaced Scanning

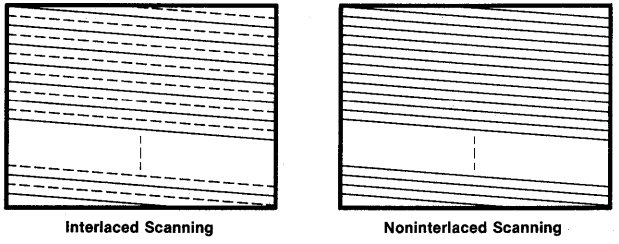


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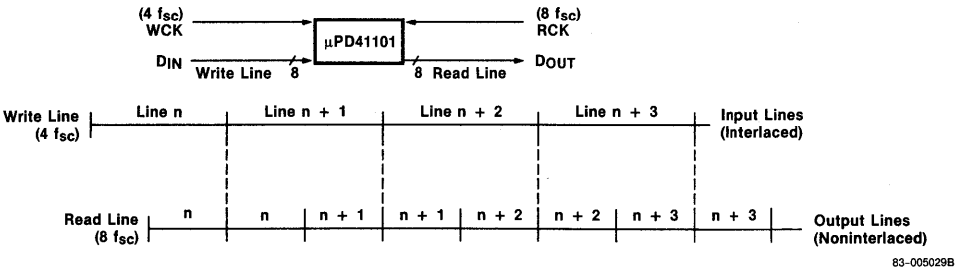
Figure 9. Using the Previous Line as Interpolated Data



The two μPD41101s used for scan conversion are written at 4 f_{SC} and read at 8 f_{SC}. The $\overline{RE}$ signal is controlled to first read the μPD41101 to which the current line data is written, and then read the μPD41101 to which the interpolated data is written (figure 10).

In the last option, as in the previous one, one buffer delays the data for one field and two other μPD41101s perform scan conversion. The control sequence is the same as described in the second method. Using data from a line of the previous field produces a clear image, especially in a still scene (figure 11).

Figure 10. Using the Average of the Previous and Following Lines

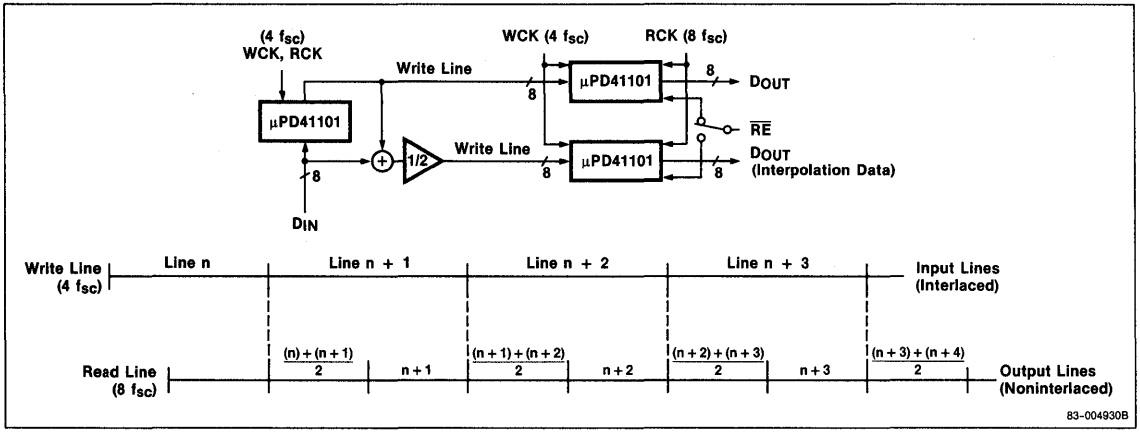
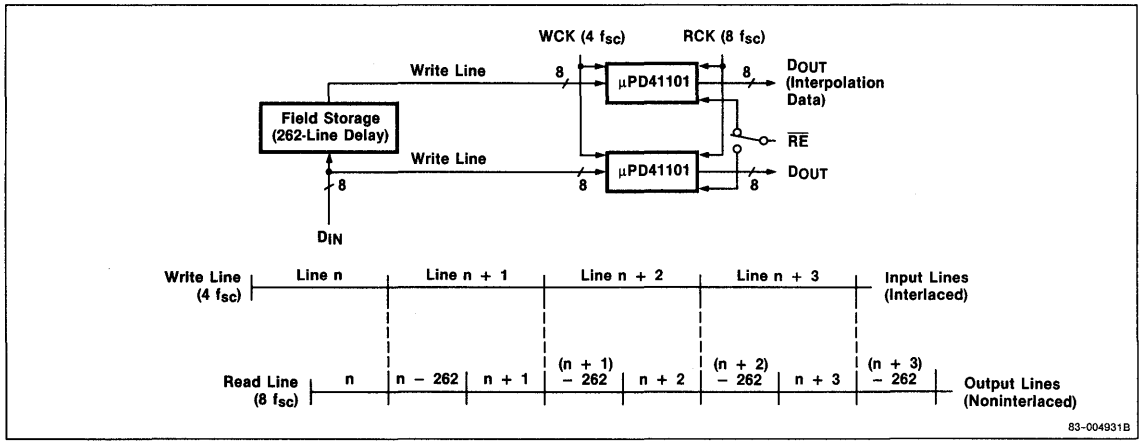


Figure 11. Using a Line from the Previous Field

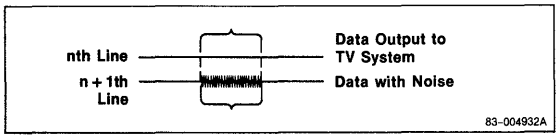


The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Dropout Compensation

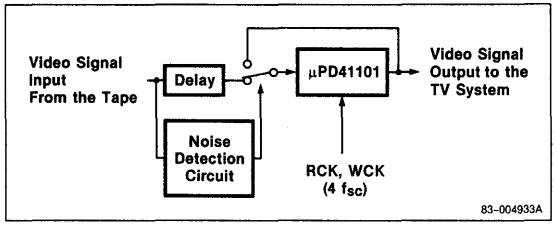
Dropout compensation cancels the noise in a VTR picture reproduction. If a line contains noise, the portion of the previous line in the same position as the noise is reproduced instead, eliminating the noise from the reproduced image (figure 12).

Figure 12. Example of Dropout Compensation



Video data from a tape normally is written to the μPD41101, delayed for one scanning line (910 bits), and then used as image data to a TV system. The noise-detection circuit senses noise in the video signal. When data containing noise is input to the μPD41101, the input is switched to the data already in the buffer so that the previous data line is written again. Data containing the noise is not output to the TV system (figure 13).

Figure 13. Dropout Compensation Circuit

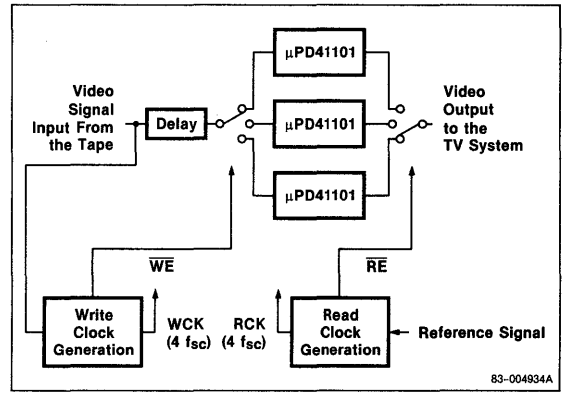


The μPD41101 can also be used as a 910-bit (one scanning line) delay. If the write data fed back by switching is delayed, the delay length must be reduced to compensate for it. For example, if switching causes two bits of delay, the delay length must be adjusted to 908 bits.

Jitter Compensation [Time Base Correction]

In a VTR, variation in head drum rotation speed or tape contraction or expansion can cause jitter in the reproduced image. The image can be reproduced clearly when jitter is adjusted and the image is reproduced with accurate clocks (figure 14).

Figure 14. Basic Jitter Compensation Circuit



The video signal input from the tape is written to the μPD41101 with a clock that can be accurately slaved to the time axis variation of the input video signal. Video data with the same time axis is reproduced by reading data using the synchronized read clock as a reference. If a jitter compensation circuit is configured so that the device to which the data is written, or from which it is read, is selected from among two or more devices by the $\overline{RE}$ or $\overline{WE}$ signal, the circuit can have a delay length of two or more lines.

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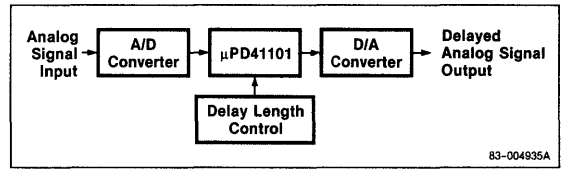
Variable-Length Delay Line

The μPD41101, driven at 8 f_{SC}, can be used as a variable-length delay line with a delay length of 10 to 910 bits (12 to 1135 bits for the μPD41102). Driven at 4 f_{SC}, it can produce a delay of 5 to 910 bits (6 to 1135 bits for the μPD41102). If an analog-to-digital (A/D) and a digital-to-analog (D/A) converter are connected to the input and output sides, respectively, it can also be used as an analog signal delay line (figure 15).

Figure 15. Analog Signal Delay Line



When reading data at a certain address, the μPD41101 requires 300 ns + 0.5 write cycles (maximum) to read data once the write cycle is complete. For example, when the μPD41101 operates on a 34-ns clock, the minimum delay length is (300 + 34/2)/34 = 9.3, or 10 cycles. When the μPD41102 operates on a 28-ns clock, the minimum delay length is (300 + 28/2)/28 = 11.2, or 12 cycles. The maximum delay length of the μPD41101 is 910 cycles and 1135 cycles for the μPD41102.

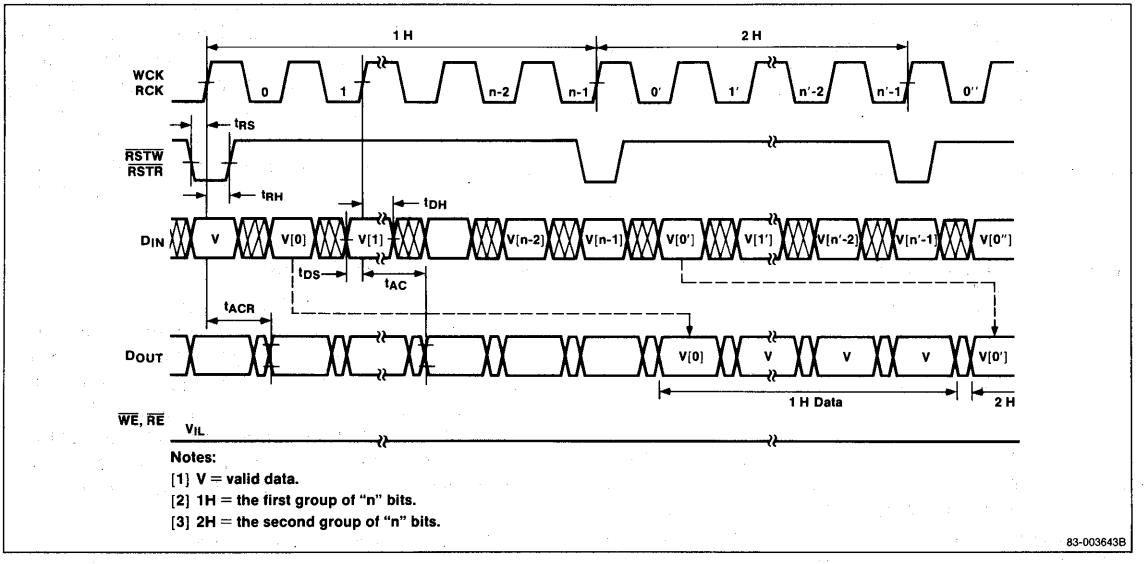
Delay length can be controlled by

- Controlling the reset input interval
- Inputting the write and read reset signals at different times (the delay length is determined by the offset between the inputs)
- Controlling the $\overline{WE}$ and $\overline{RE}$ signals

In the first method, the same signal is used for WCK and RCK. $\overline{RSTW}$ and $\overline{RSTR}$ are controlled together. Data written after a reset signal is read after the next reset interval. If the reset signal is input every 900 cycles, the delay length is 900 bits. This option produces a delay length determined by the reset interval to control the delay length (figure 16).

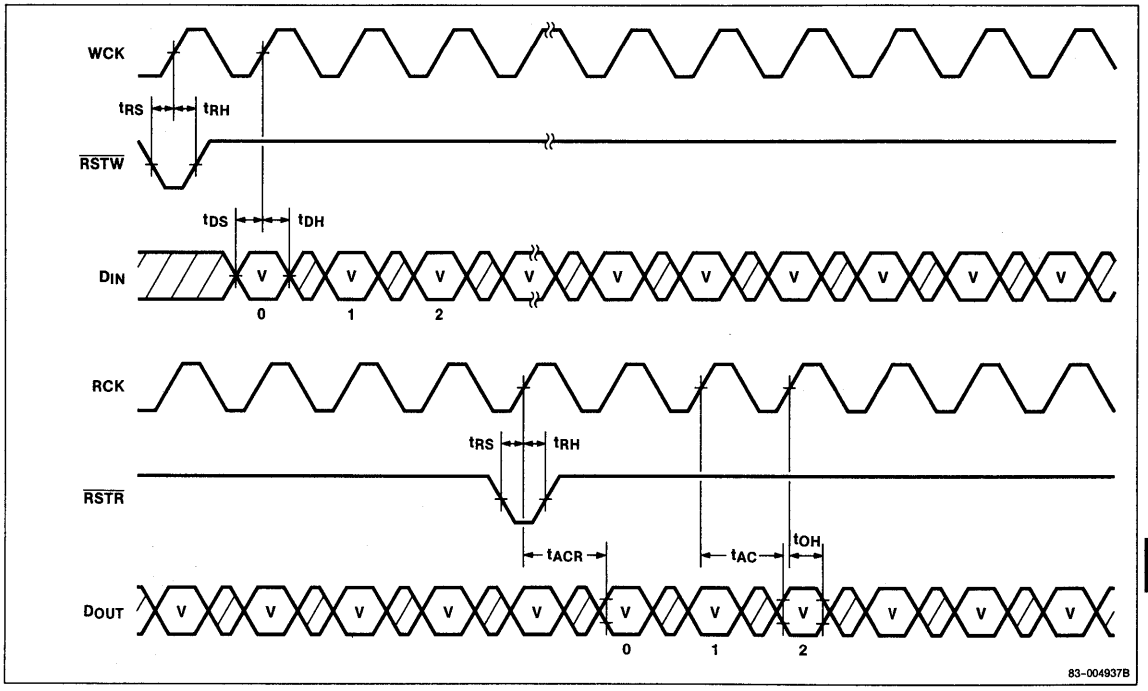
In the second method, using the write and read reset signals, data written from address 0 by the $\overline{RSTW}$ signal is read out from address 0 when the next $\overline{RSTR}$ signal is input. The delay length is determined by the offset between the write reset signal and the next read reset signal input (figure 17).

Figure 16. Controlling Delay Length with the Reset Interval



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 17. Controlling Delay Length with $\overline{RSTW}$ and $\overline{RSTR}$



In the third method, using the $\overline{WE}$ and $\overline{RE}$ signals, write or read operation is disabled when $\overline{WE}$ or $\overline{RE}$ is high; the interval pointer remains at the address where operation is disabled, regardless of the status of WCK or RCK. The delay length can be controlled in one-cycle units by controlling $\overline{WE}$ and $\overline{RE}$. After the reset interval, read data is delayed by 910 cycles (1135 cycles for the μPD41102) from the write data (figure 18).

Time Axis Conversion

You can use the μPD41101 for time axis conversion by changing the write clock frequency (WCK) and the read clock frequency (RCK). One application for time axis conversion involves image contraction or expansion in the horizontal direction. The image contracts if the read clock frequency is higher than the write clock frequency, and it expands if WCK is higher than RCK (figure 19).

Figure 18. Controlling Delay Length with $\overline{WE}$ and $\overline{RE}$ in the μPD41101

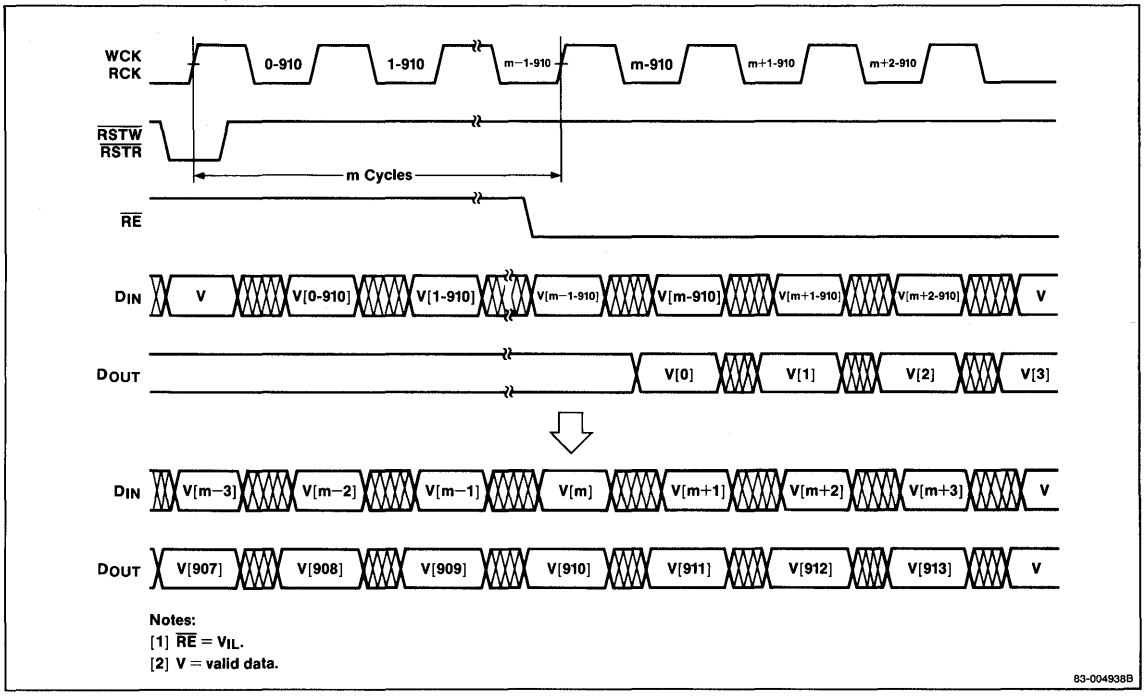
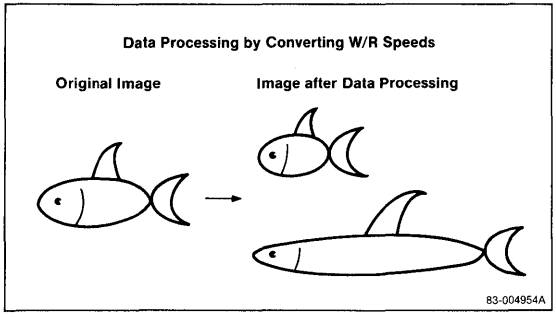


Figure 19. Time Access Conversion Application



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Digital Signal Input Synchronization

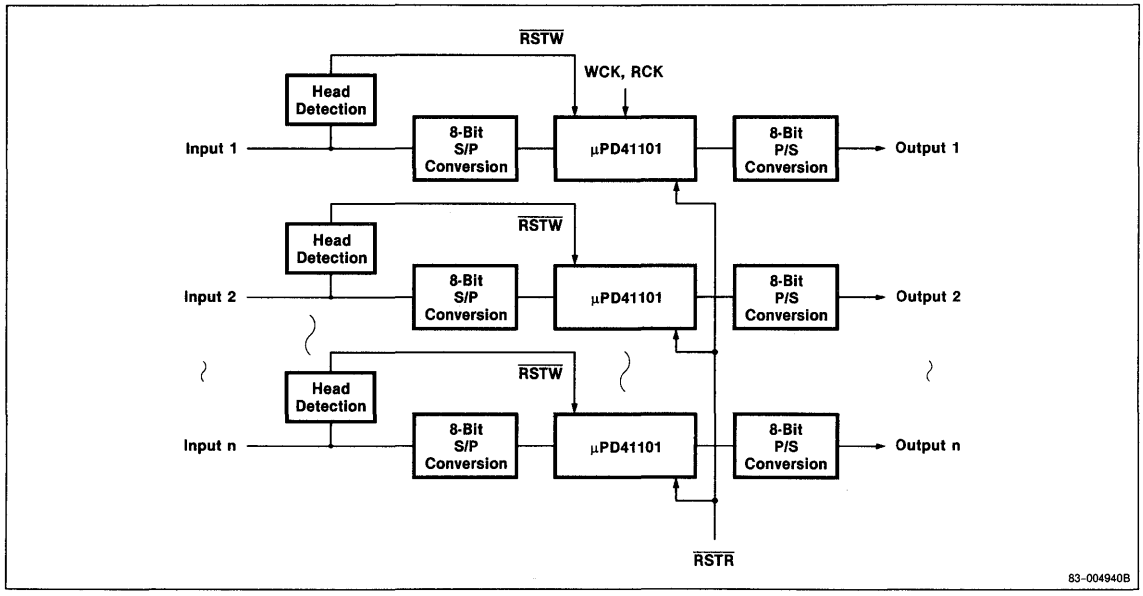
When performing timeshared data processing in an electronic telephone exchanger or in a star-configured local area network, the phase between input streams may be offset because of differences between the terminal and the central line exchange module. The μPD41101 can be used to correct the phase offset (figure 20).

Inputs 1 to n are serial data input streams. However, the frame heads (flags indicating the beginning of the data) of each input stream are not synchronized.

The solution requires controlling write operation for each stream. When a frame head is detected, the write address is reset to 0. A clock extracted from each input can be used as the clock for that write cycle. When data is written to all μPD41101s, the read address is reset to 0 by inputting $\overline{\text{RSTR}}$ with appropriate timing. All data streams then can be read out in the same phase by reading all μPD41101s simultaneously, even if the input streams are not synchronized.

The serial-to-parallel and parallel-to-serial conversion circuits shown in figure 20 may be used only when serial data is handled at each input and output.

Figure 20. Digital Signal Input Synchronization



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General Application

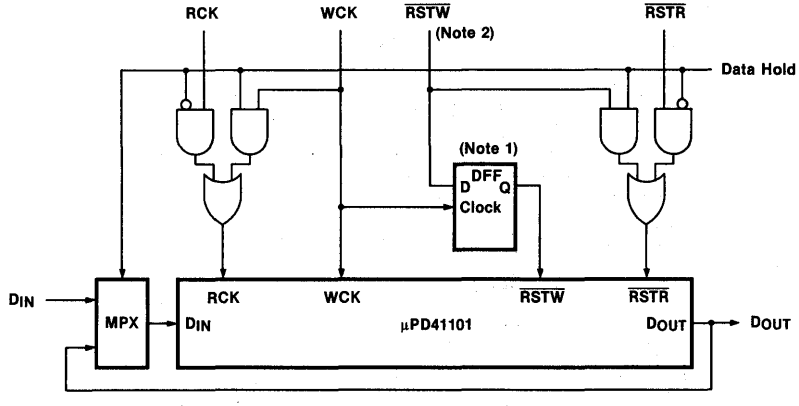
The μPD41101 and μPD41102 are suitable for use as buffer storage in data transfer operations between devices of different speeds. Because they use dynamic circuits, the maximum hold time for storage cell data is 1 ms. To hold data longer than 1 ms, you must rewrite it to the same address within 1 ms (figure 21).

The read and write addresses must coincide when rewriting data. If the feedback data is not delayed by a multiplexer, input the $\overline{RSTW}$ and $\overline{RSTR}$ signals simultaneously so that the output data of address n is fed back to the input as it is, and then written again to address n.

If the feedback data is delayed, adjust the input timing of $\overline{RSTW}$ and $\overline{RSTR}$, depending on the delay (number of cycles) of the feedback data. $\overline{RSTR}$ must be advanced according to the feedback data delay.

In either case, WCK and RCK must be the same. To read the data written to an address after the write cycle for that address is complete, 300 ns + one-half write cycle is required.

Figure 21. Static Hold Circuit for Storage Cell Data



Notes:

[1] A D-type flip-flop must be provided when the data is delayed.

[2] $\overline{RSTW}$ must be input at least once while Data Hold is at a true (high) logic level.

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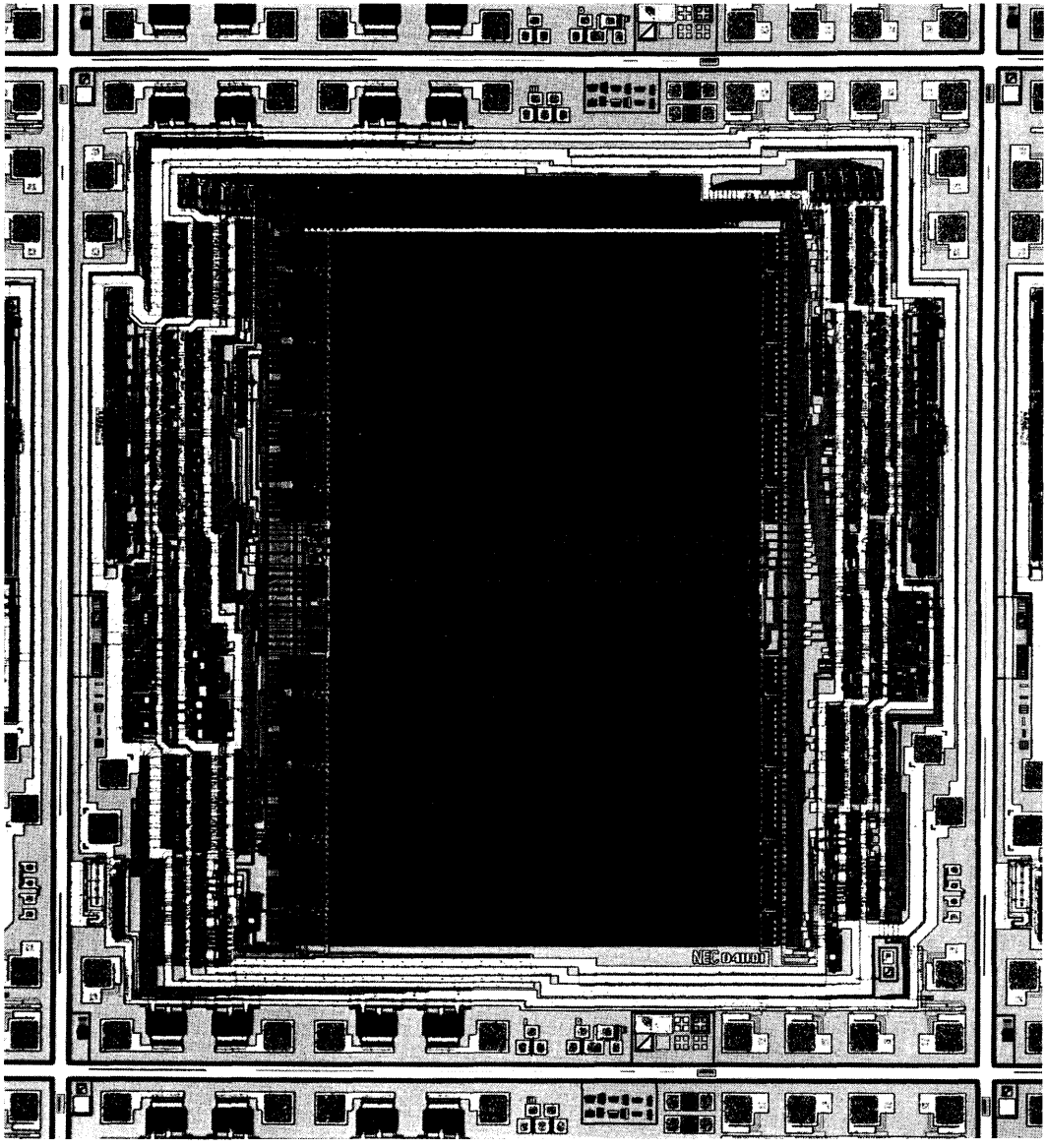
The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 22. μPD41101/μPD41102 High-Speed Line Buffer



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Application Note 57
μPD42101/42102/42505
High-Speed Line Buffers

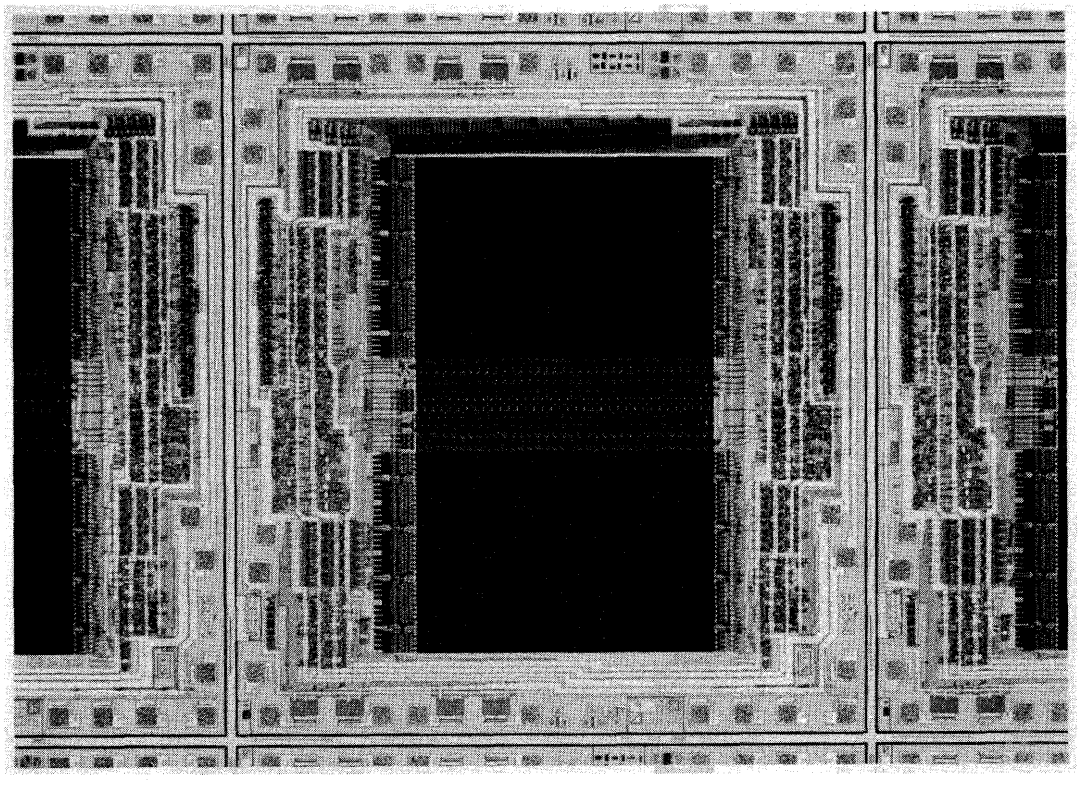
Introduction

The need for storage devices to provide delay and speed conversion in a variety of computer, telecommunication, and consumer applications has led to NEC's development of several new high-speed line buffers. The synchronous or asynchronous operation of these devices allows them to be used as elastic storage to synchronize data flow between two asynchronous parts of a system, e.g., between communication and microcomputer chips.

In graphics systems, line storage devices can act as high-speed source and destination registers during raster operations. In television and VCR products, the 1K x 8 buffers provide the raster line storage required for luminance and chrominance separation and non-interlaced scan conversion. The larger 5K x 8 devices are perfectly suited for facsimile and printer applications because they can store a line of information or a page of text at high speed.

This application note describes NEC's μPD41101, μPD41102 and μPD42505, three functionally equivalent buffers with different capacities and speeds. Each device has independent, 1-byte write and read ports with separate write and read clocks. High-speed performance is achieved by means of unique circuitry rather than a submicron process. Fast access times

Figure 1. Die Photograph of the μPD41101 and μPD41102



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

and low cost are possible because of specialized dynamic circuit designs using the best of MOS technology (figures 1 and 2).

Features

The μPD41101, μPD41102, and μPD42505 are identical except in organization and cycle times (table 1). The following discussion applies to the three devices collectively, unless noted otherwise.

Serial Addressing. Addresses are generated automatically by an internal address counter and need not be supplied externally. The clocks provided by the WCK and RCK signals increment the respective write and read address counters, enabling data to be read out in the order in which it was input.

Wraparound Addresses. The internal address pointers are implemented as ring counters; they return to address 0 after the last byte in a line has been accessed.

Asynchronous Operation. Separate write and read clocks, coupled with their respective enable inputs, allow for independent write and read operation.

Reset Function. The $\overline{\text{RSTW}}$ and $\overline{\text{RSTR}}$ pins reset the internal pointers to address 0. Resetting of the read pointer can be initiated after "n" write cycles to provide an adjustable delay line of "n" cycles.

High-Speed Address Selection. By interleaving the internal storage arrays and using a novel pipelining technique for high-speed address selection, the devices achieve very fast access times. The μPD41102-3, for example, has a specified minimum cycle time of 28 ns.

Large Capacity. All devices are 1-byte wide. Their line lengths vary as shown in table 1. The μPD42505 is configured as 5048 by 8 bits to store a page of information.

Table 1. Configurations and Cycle Times

Part Number	Organization	Cycle Times
μPD41101	910 x 8 bits	34 or 69 ns
μPD41102	1135 x 8 bits	28, 34, or 56 ns
μPD42505	5048 x 8 bits	50 or 75 ns

Functional Description

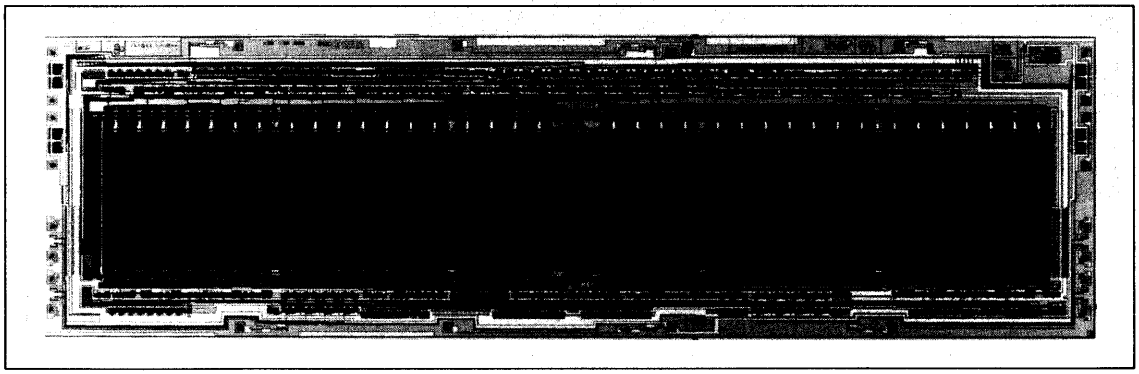
Historically, line buffers were designed with shift registers that suffered from fall-through delay as data tumbled down the stack. With NEC's new generation of buffers, which provide independent write and read clocks for asynchronous writing and reading, the write data requires a delay of at least 10 or 11 cycles before appearing at the output. The minimum line delay (specified in the individual data sheets for each device) is not a problem in most applications because the required delay is usually longer than the specified minimum delay.

In synchronous operation, where write and read cycles are controlled together (and write and read addresses coincide), the internal logic causes a write cycle to be delayed by one-half cycle from the read cycle. Read data is output from the previous line, while new input data is written just one-half cycle later.

Storage Arrays

Unlike other devices based solely on static cells, NEC's line buffers have two types of storage elements: a static cell for high-speed operation and a dynamic cell for achieving large capacity in a small die area. To operate at high speed, the fast static cell is used as a prefetch buffer. While the first 8 bytes of data are being accessed from the static cell, the first row of the dynamic cell is preselected for subsequent access (see **Addressing**).

Figure 2. Die Photograph of the μPD42505



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 3. Dual-Port Static Storage Cell Array

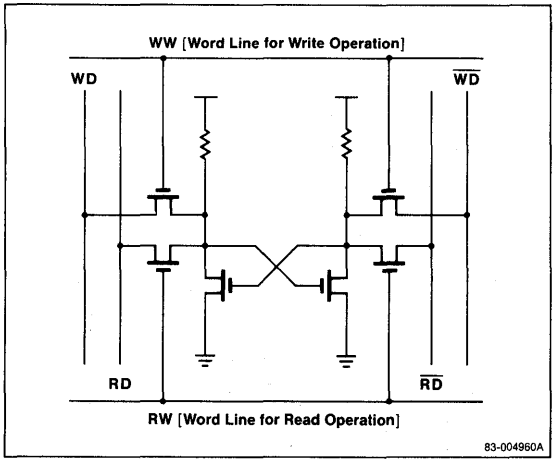
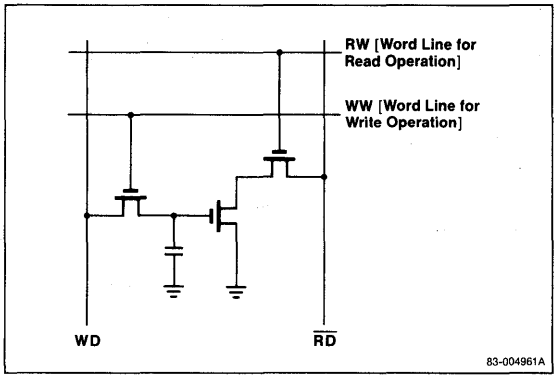


Figure 4. Dual-Port Dynamic Storage Cell Array



The static storage cell has separate word lines for write and read cycles (RW and WW), as well as differential data inputs (RD/$\overline{RD}$ and WD/$\overline{WD}$) for high-speed operation (figure 3). The three-transistor, one-capacitor dynamic storage cell contains separate write and read data and word lines, two access transistors, and a third transistor for cell signal pre-amplification (figure 4). Pre-amplification is required since there are only eight data amplifiers, one each for the eight input/output ports.

Unlike the static cell, the dynamic cell uses only one write and read data line and cannot take advantage of differential sensing. Although the speed is slower, its fewer components make this cell more suitable for compact layout and high device integration. The success of these high-speed buffers lies in the matching of the static and dynamic cells to achieve high performance at a low cost (figure 5).

Addressing

On a cold start, initial writing and reading to the device requires fast access times from the six-transistor static cell. While the first eight bytes are being accessed from the static cell, the first row of the dynamic cell is preselected. To achieve relatively fast dynamic access, the dynamic array is split into two segments and storage interleaving is employed.

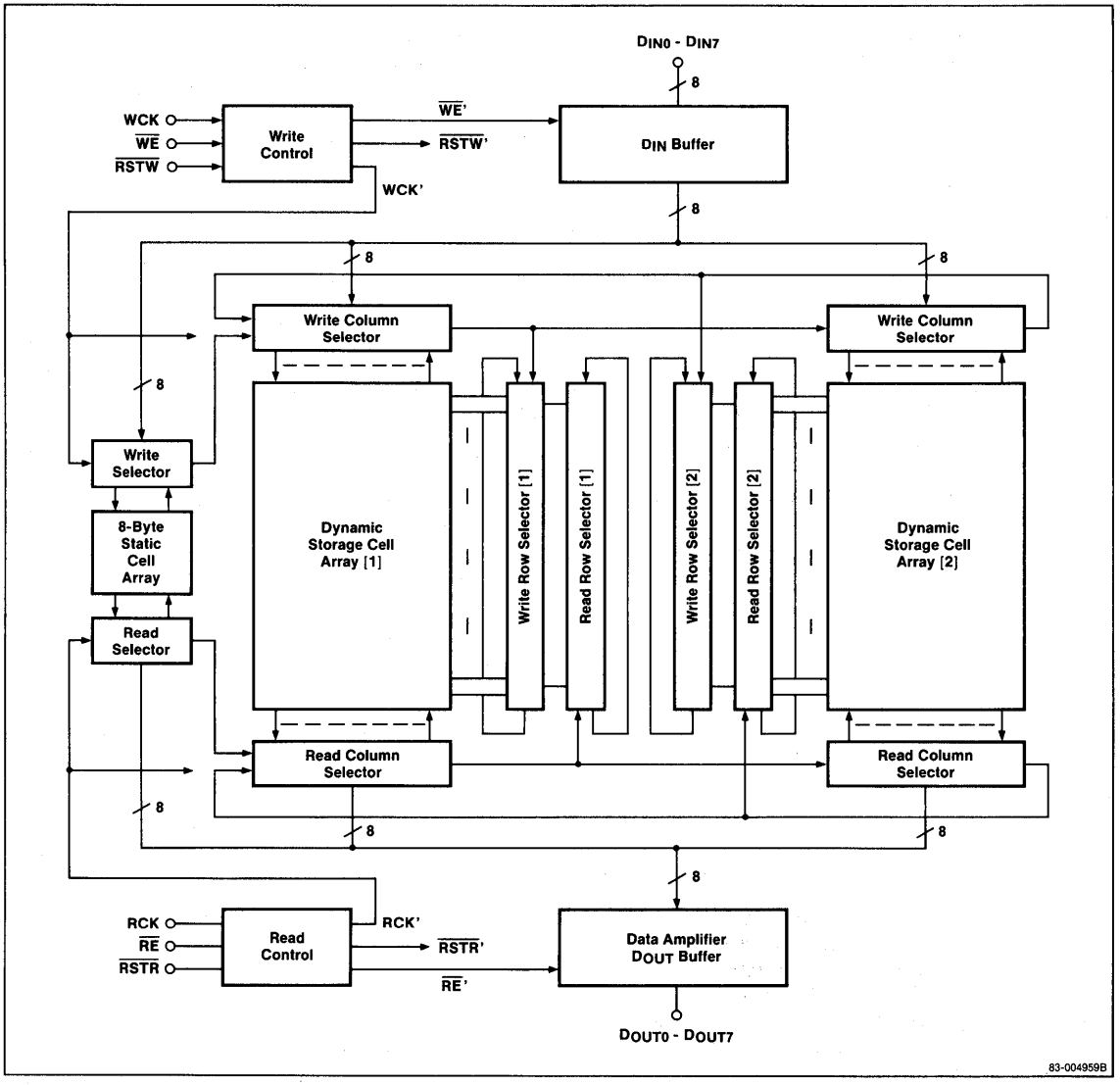
From a functional point of view, the line buffer is a long, eight-bit-wide shift register. Its layout is compacted to produce a small die size. The chip has two arrays, each representing one-half of the line length. For the 1135 x 8 device, each subarray is organized as 568 bytes (71 x 8 bytes).

The serial addresses are generated automatically using column and row selectors for both write and read operation. The following steps summarize the interleaving sequence.

- In a reset cycle, data is read from the 8-byte static cell, and the first row of subarray 2 is preselected.
- Row 1 of dynamic subarray 2 is accessed, and the address pointer moves to subarray 1 for preselection.
- Row 1 of subarray 1 is read, and row 2 of subarray 2 is preselected.
- Interleaving continues between the subarrays until the last address is accessed, at which time the internal pointer automatically resets to address 0.

The address pointers are shift registers wired as ring counters and clocked in a wraparound fashion to control writing and reading of data at specific locations. The shift registers are incremented by one address for each WCK or RCK clock. Separate write and read address pointers are required to execute write and read cycles independently and at different speeds.

Figure 5. Block Diagram



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Write and Read Timing

The μPD41101, μPD41102, and μPD42505 are equipped with the following pins: D_{IN0} through D_{IN7}, $\overline{RSTW}$, $\overline{WE}$, and WCK for write operation and D_{OUT0} through D_{OUT7}, $\overline{RSTR}$, $\overline{RE}$, and RCK for read operation (figures 6 and 7). Serial addresses are automatically generated by an internal address counter. When $\overline{WE}$ is low, one byte is written to each address in synchronization with the WCK write clock (refer to the individual data sheets for timing diagrams); the internal write address pointer increments by 1 with each falling edge of WCK. Write data must meet the specified setup and hold times as measured from the rising edge of WCK.

Figure 6. Configuration of 24-Pin Plastic DIP (and Miniflat for μPD41101, μPD41102 only)

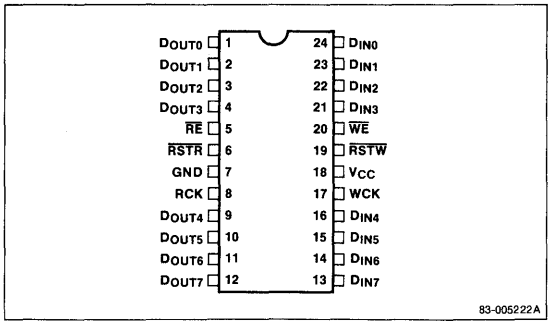
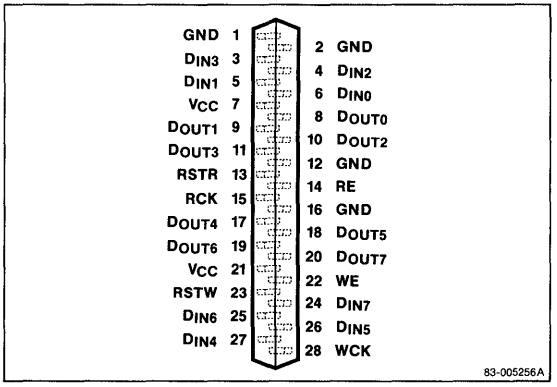


Figure 7. Configuration of 28-Pin Plastic ZIP (μPD42505 only)



The signal on $\overline{RSTW}$, which is used to reset the write address pointer to 0, also has setup and hold requirements with respect to the write clock.

When the signal on the read enable ($\overline{RE}$) pin is low, one byte of data is read out of the device for each RCK clock cycle, and the read address pointer increments by 1. The read address pointer is totally independent of the write address pointer.

The control functions of $\overline{WE}$ and $\overline{RE}$ are shown in figure 8. Bringing these two signals high (inactive) stops the internal address pointers; activating them again causes the internal pointers to increment to the next sequential address.

Synchronous Operation

Figure 8 shows the internal timing sequences, including those for address transitions and write cycles, during synchronous operation of these devices. With a common write and read clock, the internal write period is delayed from the write address. This delay, required when the write and read addresses are identical, allows a read cycle and then a write cycle to be executed to the same cell location. Read data is taken from the previously written line.

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Designing with NEC's Line Buffers

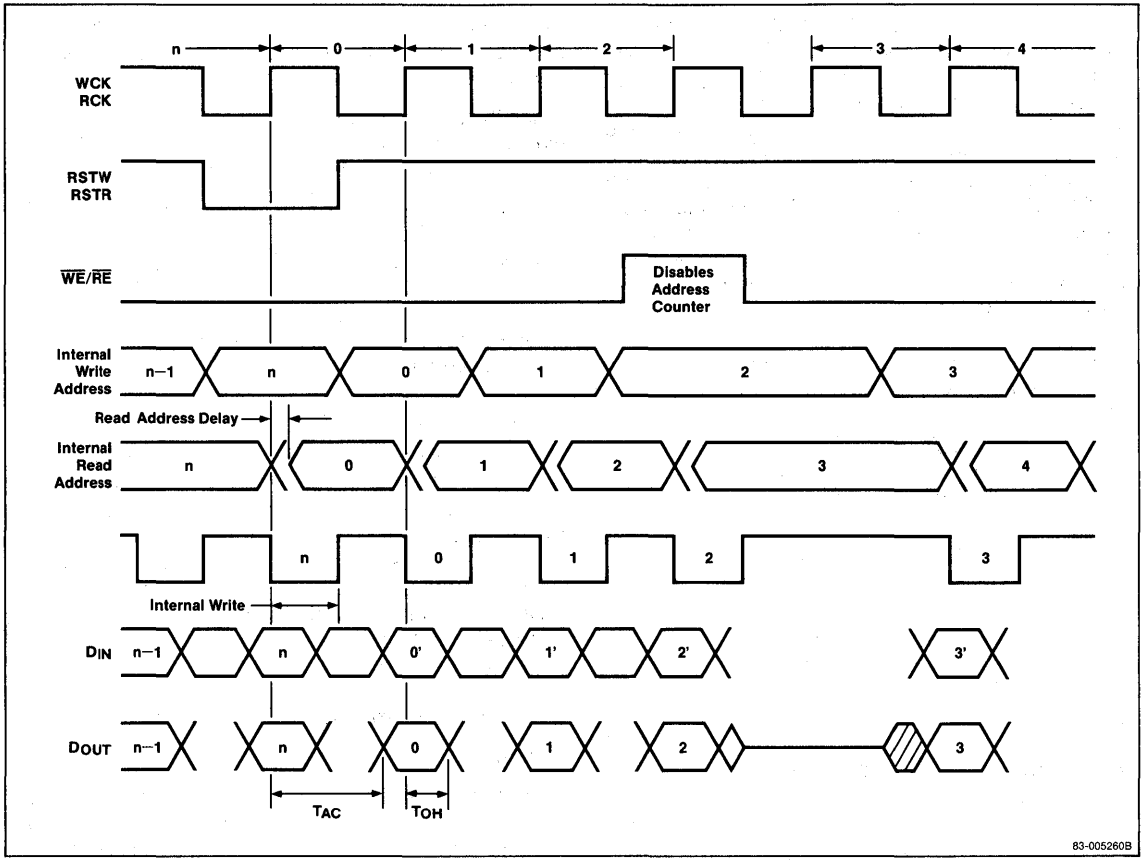
Initialization

After power has been applied, the write and read address pointers are undefined and therefore need to be set to address 0. Proper timing for a $\overline{RSTR}$ or $\overline{RSTW}$ reset cycle is described in the individual data sheet for each device.

Refreshing

Refreshing of the dynamic storage cells must be performed at regular intervals. Data remains valid for 1 or 5 ms, depending on the line length of the device (1 ms for the μPD41101 or μPD41102 and 5 ms for the μPD42505). Since NEC's line buffers contain only data amplifiers and no sense amplifiers, a standard read cycle does not refresh the storage cell. If longer hold times are required, the original data must be rewritten to the same address.

Figure 8. Internal Timing for Synchronous Operation



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Minimum Delay Length

Unlike register-based line buffers, which use a data flow-through cycle, NEC's line storage elements are not capable of reading data immediately after it has been written. Each device requires a minimum delay, as calculated by the equations shown in table 2.

Table 2. Calculating Minimum Delay

Part Number	Equation
μPD41101	1/2 write cycle + 300 ns (34 ns/2 + 300 ns)/34 = 9.3 or 10 cycles
μPD41102	1/2 write cycle + 300 ns (28 ns/2 + 300 ns)/28 = 11.2 or 12 cycles
μPD42505	1/2 write cycle + 500 ns (50 ns/2 + 500 ns)/50 = 10.5 or 11 cycles

Delay length, as measured by the number of cycles, is dependent on the speed of the clock, i.e., at 14.3 MHz, the minimum delay for the μPD41101 would be 5 cycles.

Storage Contention

In asynchronous operation, when write and read cycles contend for the same line, the last "n" bytes (where "n" may be 5-12 bytes) of line output are taken from the previous line. This type of contention occurs most frequently when executing continuous write and read cycles at different rates, such as when converting video images from interlaced to noninterlaced scanning. In this case, the read clock operates at twice the speed of the write clock. Near the end of the line, the read cycle catches up and contends with the write cycle.

Setting Delay Length

Varying the Reset Interval in Synchronous Operation. Depending on the application, some schemes for implementing delay length suit system timing better than others (see individual data sheets for timing). In synchronous operation, the delay is set simply by varying the interval between the reset pulses. In this case, the reset clocks are tied together. Since write and read clocks are common, line delay is determined by the offset between resets.

Varying the Reset Interval in Asynchronous Operation. In asynchronous operation, the reset interval can be varied using independent clocks and reset signals. Delay length is calculated as the timing difference between the write and read reset pulses.

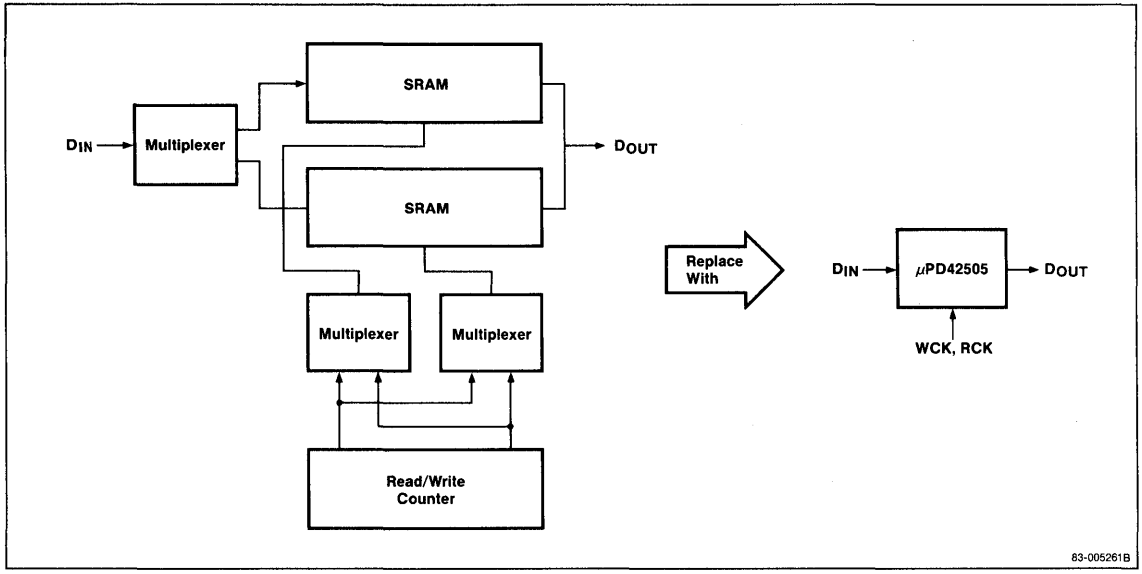
Controlling the $\overline{RE}$ Pin. In the third option, the read enable pin ($\overline{RE}$) can be used to control read operation and the read address counter. When $\overline{RE}$ is high (disabled), the read address counter does not increment and no data is output. After the desired delay, $\overline{RE}$ can be brought low to begin executing read cycles. For delays exceeding one line length, care must be taken to ensure that new data is not written into an address before the old data is read.

μPD42505 Large-Capacity Line Buffer

The μPD42505 was designed for applications where a large amount of data is handled per line, e.g., in high-performance digital copiers and G3 or G4 facsimile machines requiring buffer storage for image compression, expansion, data transmission, and in some cases, image enhancement using filtering techniques for digital signal processing. The 5K x 8 line length has also been used in some designs to hold the data tokens in digital filtering arrays.

Although line buffering can be achieved using fast static RAMs as shown in figure 9, the need for two devices and other complicated peripheral circuits necessarily increases the cost of a system and makes it more difficult to implement. The μPD42505 eliminates the complexity and high cost by providing the same functions and more advantages in one package.

Figure 9. System Design Using Static RAMs Versus High-Speed Line Buffer



The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

Figure 10. Line Buffering in Local Area Networks

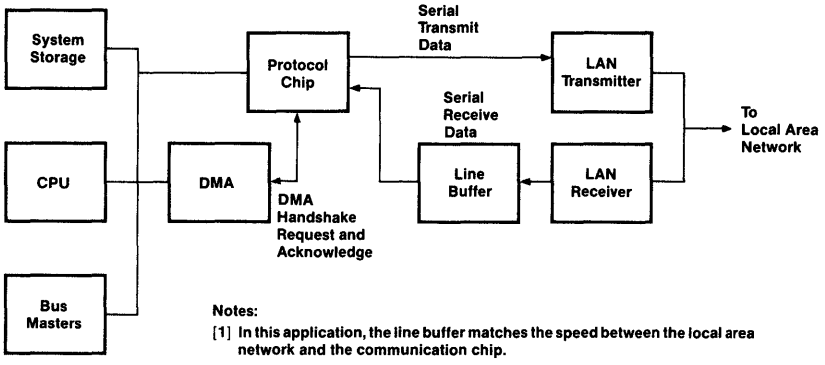


Figure 11. Elastic Storage for Digital Signal Processing Applications

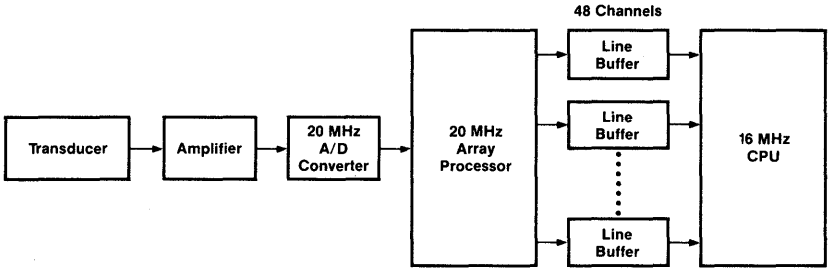


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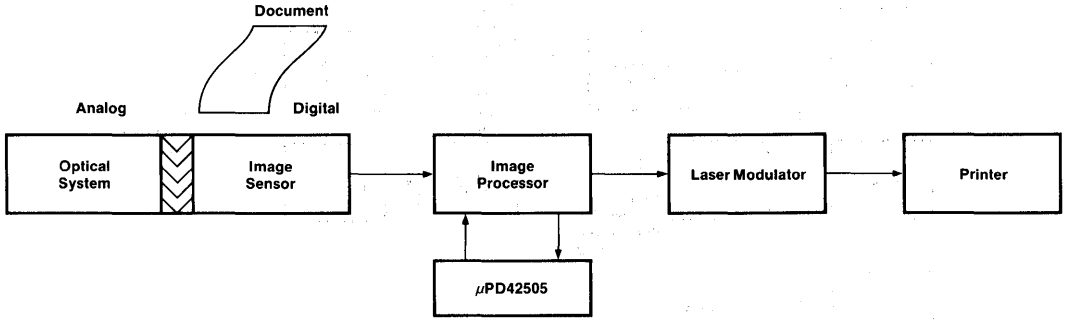
Figure 12. Image Enhancement Techniques in High-Performance Digital Copiers



Notes:
[1] In this application, a large-capacity line buffer is used to hold token data for digital signal processing.

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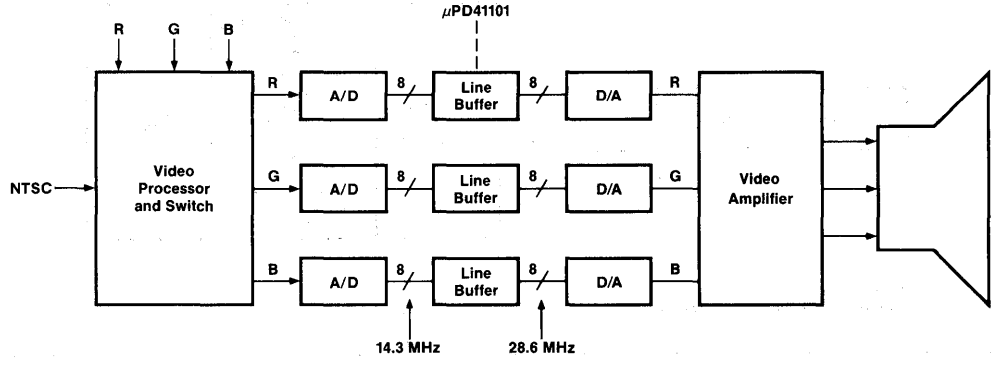
Figure 13. Doubling the Line Rate in Scan Conversion



Notes:
[1] In high-definition TV applications, the line buffer is used to double the scan rate by reading at twice the write frequency.

83-005265B

The μPD42101 and μPD42102 exactly replace the μPD41101 and μPD41102.

NEC Electronics Inc.

Application Note 58
Interlaced To Noninterlaced Video Scanning Using The μPD42101 High-Speed Line Buffer

Introduction

Interlaced scanning is used in television, videotape, and videocassette recording applications to reduce bandwidth and maintain an acceptable amount of screen flicker in video signals. The procedure involves lowering the vertical resolution and doubling the number of fields so that one complete frame is formed from the first and second fields. When a video signal subsequently is decoded and ready for display on a monitor or TV, bandwidth generally is no longer a problem and the higher vertical resolution of a noninterlaced signal may be used to produce a sharper image on the screen.

In NTSC TV systems, there are 262.5 scan lines per field, 2 fields per frame, and 30 frames per second (figure 1). With the resolution per field in the vertical direction lowered by interlaced scanning, the lines become rougher and the gap between scanned lines more visible. This drawback becomes all the more conspicuous in larger-screen TVs.

Vertical resolution problems caused by interlaced scanning can be resolved by first repeating the signal of each scan line. The number of scan lines per field then can be doubled by doubling the horizontal frequency and keeping the vertical frequency intact. Subsequently, an interlaced signal can be converted to a noninterlaced signal to increase the resolution of the picture in the vertical direction (figure 2).

The conversion from interlaced to noninterlaced scanning can be achieved by temporarily storing each line in a buffer and then displaying it twice to double the number of lines per field (figure 3).

Figure 1. Relationship of Field to Frame in Interlaced Scanning

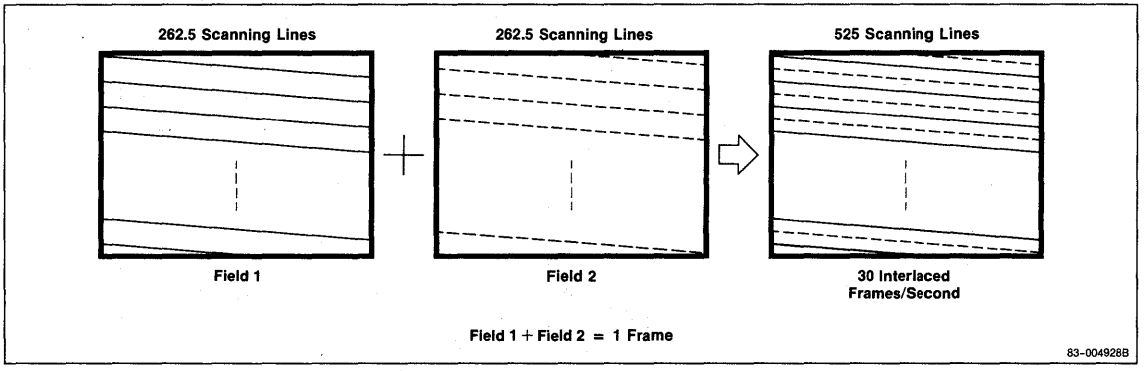
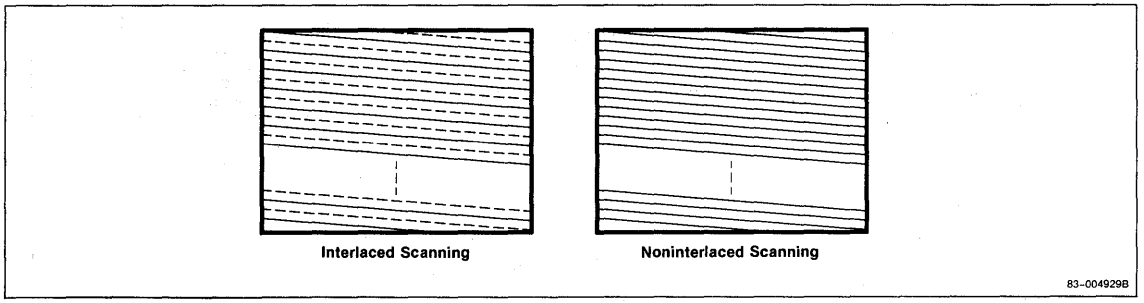


Figure 2. Difference Between Interlaced and Noninterlaced Scanning



The μPD42101 exactly replaces the μPD41101.

Figure 3. Doubling the Line Rate

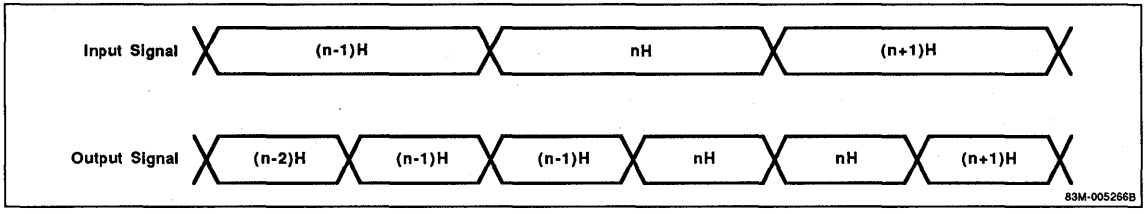
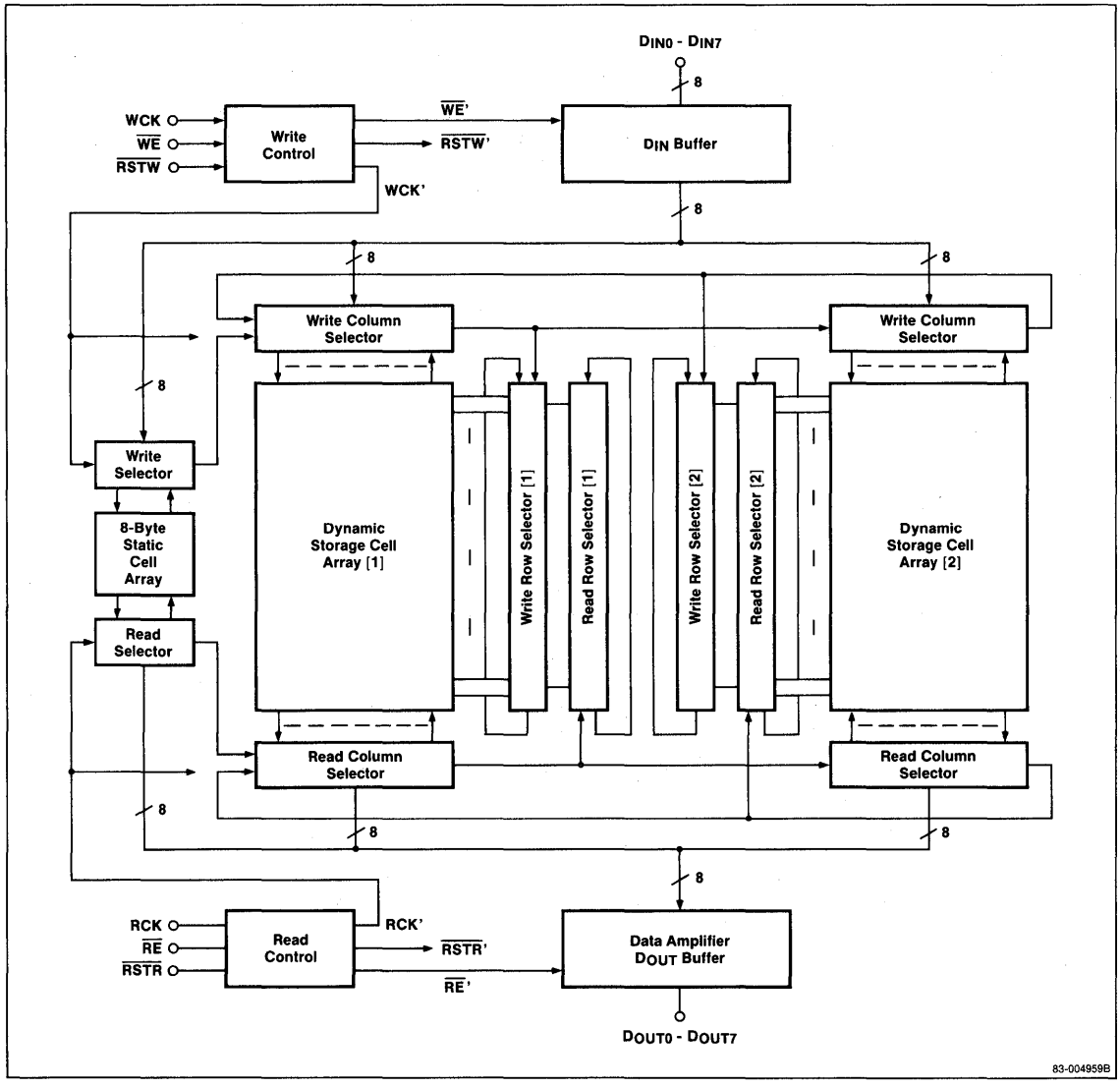


Figure 4. Block Diagram



The μPD42101 exactly replaces the μPD41101.

The μPD41101 High-Speed Line Buffer

The type of scan conversion described in this application note requires buffer storage for each line. Required storage is calculated by dividing the scanning period per line by the sampling period to determine the number of samples per line. Required storage for NTSC systems is computed as shown in the following sequence.

(1) Scanning period per line:

$$\frac{1}{\frac{(525 \text{ lines}}{\text{frame}} \times \frac{30 \text{ frames})}{\text{second}}} = 63.5\ \mu s$$

(2) Minimum sampling frequency:

$$3.58 \text{ MHz} \times 4 = 14.32 \text{ MHz} = 69.83 \text{ ns}$$

(3) Samples per line:

$$63.5\ \mu s / 69.8 \text{ ns} = 909.7 \text{ samples}$$

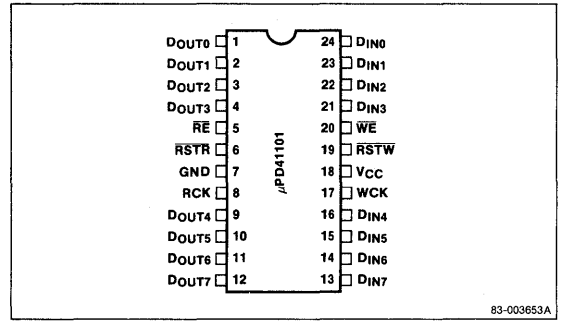
This application requires the storing of 910 words, exactly one horizontal scanning line of data. NEC's μPD41101 high-speed line buffer, configured as 910 words by 8 bits, is ideally suited for the digital processing of video signals because one-line delays and time axis conversions can be executed easily.

The μPD41101 differs from general-purpose static devices in that it doesn't require a double-buffer configuration (figure 4). Writing and reading can be executed independently and asynchronously. Since an internal address pointer eliminates the need for external address generation, the only external controls required are those for the WCK and RCK write and read clocks and the $\overline{RSTW}$ and $\overline{RSTR}$ write and read reset signals (see figure 5 for pin assignments). As shown in table 1, three versions of the μPD41101 are available.

Table 1. Access and Cycle Times of the μPD41101

Part Number	Access Time (max)	Write Cycle Time (min)	Read Cycle Time (min)
μPD41101-3	27 ns	34 ns	34 ns
μPD41101-2	27 ns	69 ns	34 ns
μPD41101-1	49 ns	69 ns	69 ns

Figure 5. μPD41101 Pin Configuration



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Operation

Write and Read Reset Cycles. After power is applied to the μPD41101, its internal address pointers are undefined and must be initialized to address 0. As shown in figure 6, the inputs on $\overline{RSTW}$ and $\overline{RSTR}$ have required setup and hold times as measured from the rising edges of WCK and RCK, respectively.

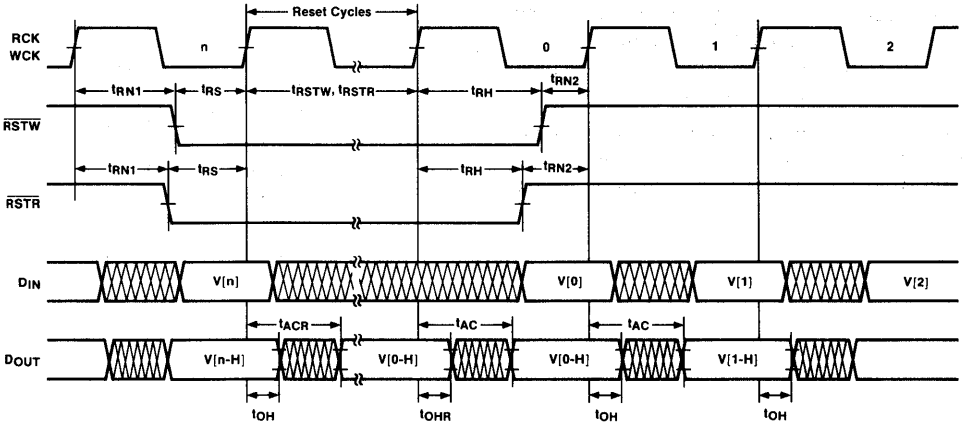
Write Cycles. Write cycles are executed in synchronization with the WCK clock (figure 7). When $\overline{WE}$ is low, 8 bits of data are sampled from D_{IN0}-D_{IN7} at the rising edge of WCK and the internal write pointer increments to the next sequential address. When the pointer reaches the last address, it wraps around to address 0 again. When high, $\overline{WE}$ disables write operation and inhibits the write address pointer. Write data must satisfy required setup and hold times as specified from the rising edge of WCK.

Read Cycles. When $\overline{RE}$ is low, read cycles are executed in synchronization with the RCK clock (figure 7). Read data is output from D_{OUT0}-D_{OUT7} after a specified access time as measured from the rising edge of RCK. The internal read pointer functions identically to the write pointer, except that the read address increments sequentially with each RCK clock.

Example of System Configuration

The block diagram in figure 8 shows a hardware system designed to convert a standard NTSC interlaced video signal to a noninterlaced signal. In this configuration, described on the following pages, the input signals derive either from an NTSC composite signal (video input), from a TV/VTR/VCR, or from the R-G-B signal output of a personal computer.

Figure 6. Write or Read Reset Cycle



Note:

[1] $\overline{WE} = \overline{RE} = V_{IL}$.

[2] V = Valid Data.

[3] Read operations commence from the rising edge of RCK at the beginning of a cycle. For the first cycle in a group of reset cycles, the read access time is defined as t_{ACR}. In all other cycles, t_{AC} defines the read access time.

[4] H = 910 cycles.

[5] Write data is strobed into the device on the rising edge of WCK at the end of a cycle.

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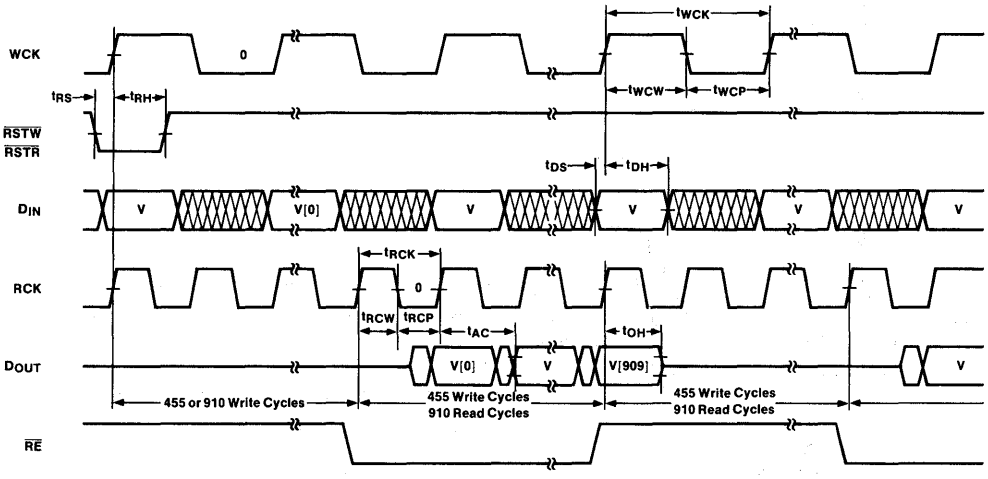
Figure 7. Write or Read Cycle



Note:

[1] $\overline{WE} = V_{IL}$.

[2] V = Valid Data.

[3] For compatibility with NTSC standards the WCK frequency is approximately 14.3 MHz. RCK cycles at twice this frequency, 28.6 MHz.

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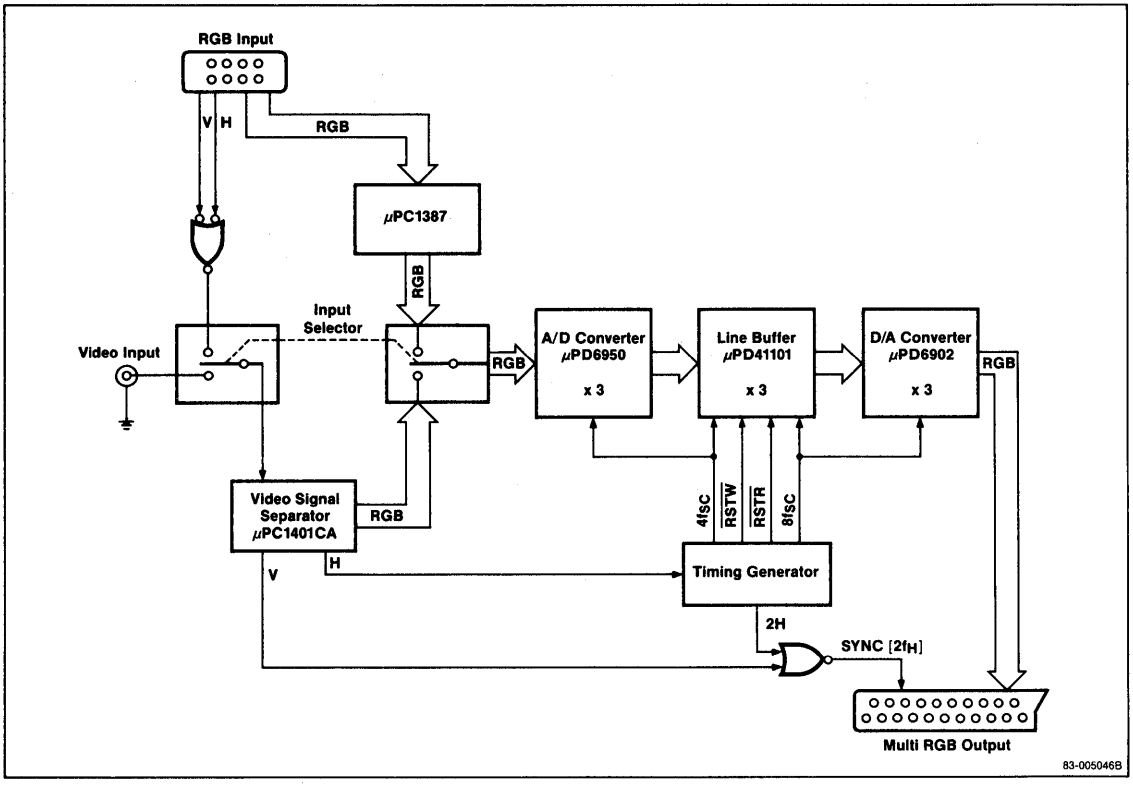
Figure 8. Scan Converter Block Diagram



The μPD42101 exactly replaces the μPD41101.

Video Signal Processor

The video signal is decoded from the R-G-B inputs by NEC's μPC1401, a device specifically designed to process the color, video, and synchronizing signals used in NTSC color TV systems (figures 9 and 10). By separating the signals, the μPC1401 can independently control them and thereby reduce the number of peripheral devices usually required in this phase.

Figure 9. μPD1401 Block Diagram

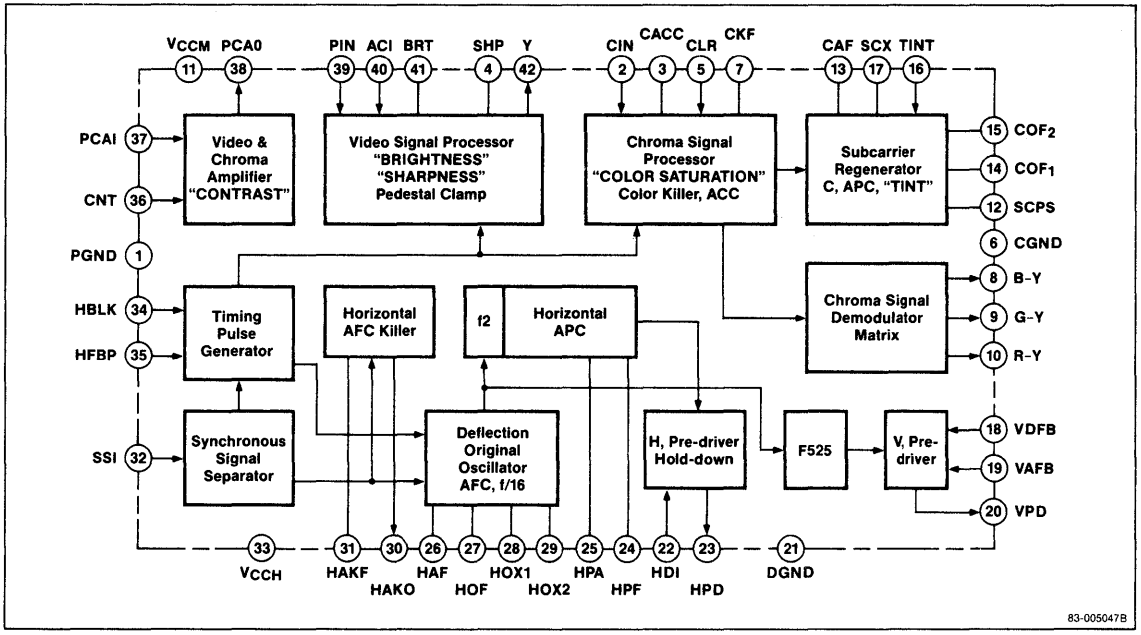
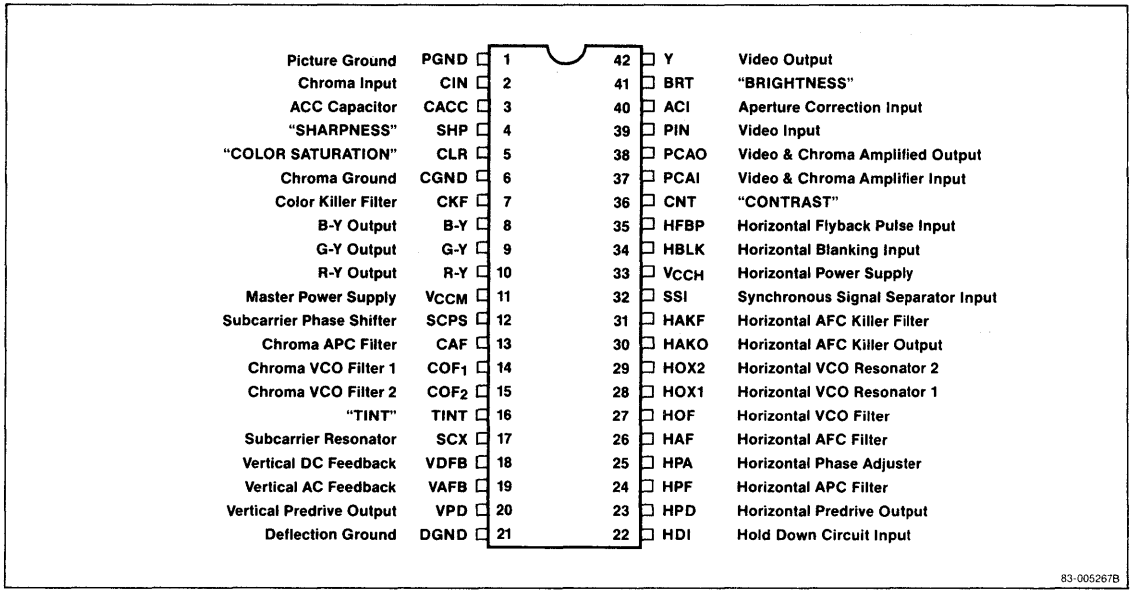


Figure 10. μPD1401 Pin Configuration



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R-G-B Signal Processor

The level of the R-G-B output signals from the personal computer are adjusted by a μPC1387 (figures 11 and 12). An interface between the digital R-G-B signals and the TV color signal output, the μPC1387 provides high-speed switching by means of a built-in R-G-B signal converter and sophisticated circuitry that blanks the signal levels. The horizontal (H) and vertical (V) synchronizing signals from the personal computer are combined into a composite synchronizing signal. When the selector switches to the R-G-B input position, the composite signal is applied to the μPC1401 in place of a TV signal.

Figure 12. μPD1387 Pin Configuration

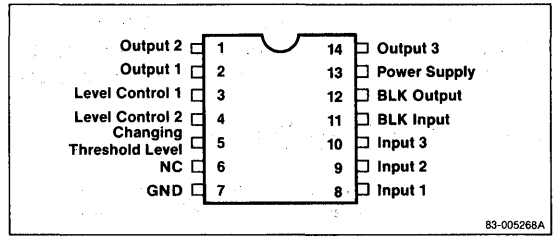
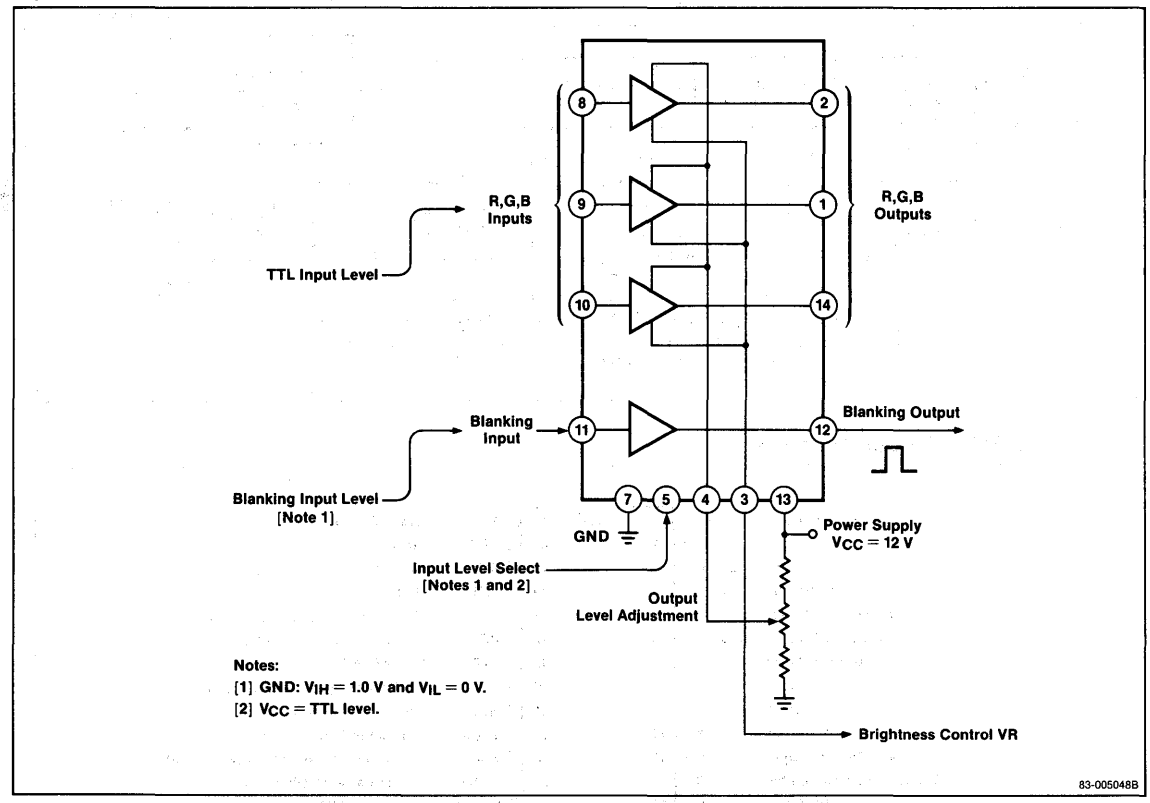


Figure 11. μPD1387 Block Diagram



The μPD42101 exactly replaces the μPD41101.

Analog-to-Digital Converter

The input selector chooses one of the two R-G-B signals from the μPC1401 and μPC1387 and passes it to the μPD6950, where it first is sampled at a clock frequency equal to $4f_{SC}$ (14.3 MHz) and then written to the μPD41101 line buffer. The CMOS-fabricated μPD6950 is an analog-to-digital (A/D) converter whose high speed and low power consumption are particularly suited to video applications (figures 13 and 14).

Figure 13. μPD6950 Pin Configuration

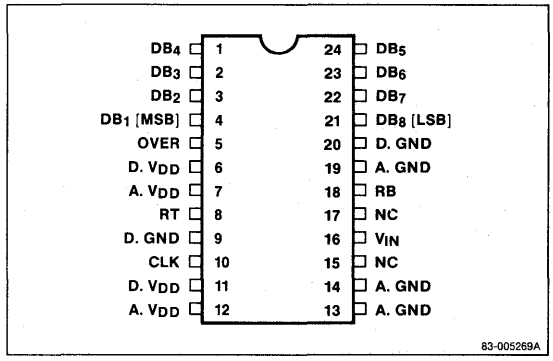
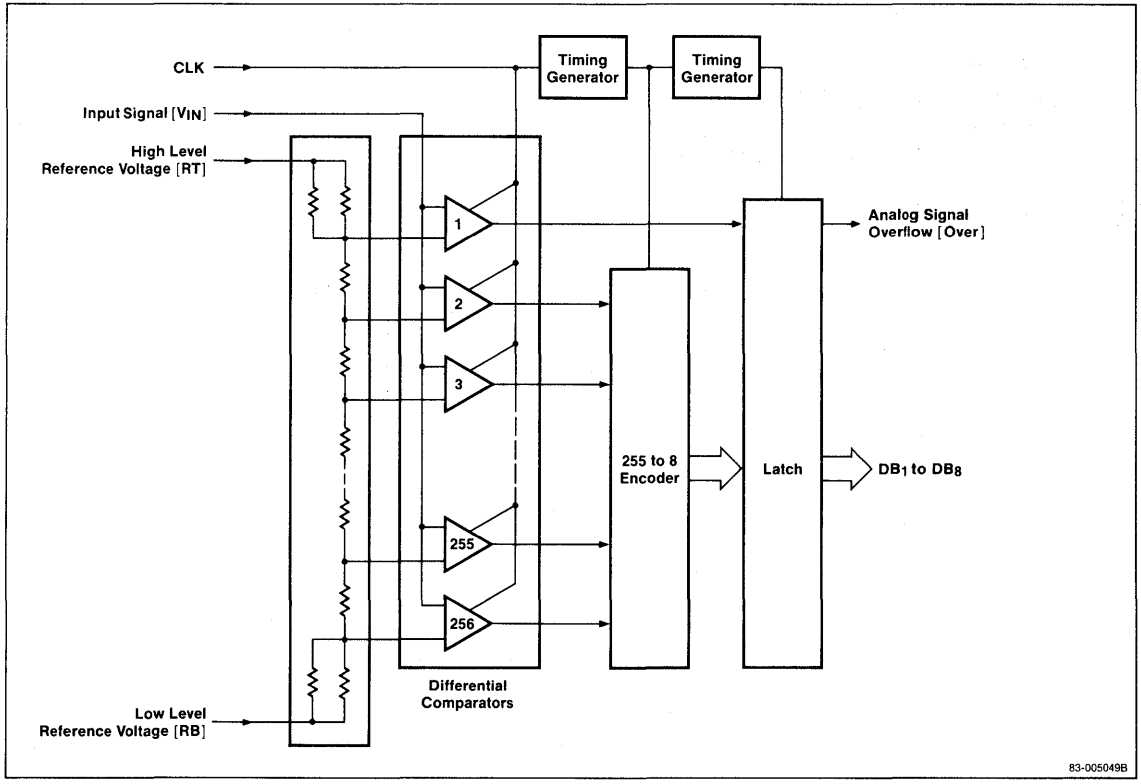


Figure 14. μPD6950 Block Diagram



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Line Buffer

This configuration uses a total of three μPD41101 line buffers, one each for the R-G-B inputs. Independent control of write and read operation by the μPD41101 allows the inputs to be written at a $4f_{SC}$ sampling rate and subsequently read at twice that frequency ($8f_{SC}$). Reading the scanned image twice doubles the number of lines sent to the TV monitor, fills the gaps between lines of an interlaced signal, and increases the vertical resolution.

Digital-to-Analog Converter

After being read at a frequency of $8f_{SC}$ (28.6 MHz), the digital signal from the μPD41101 is converted to an analog signal by the μPC6902 (figures 15 and 16). The CMOS-fabricated μPC6902 D/A converter is designed to handle 50 million samples per second.

Timing Generator

The $8f_{SC}$ and $4f_{SC}$ clocks and $\overline{RSTW}$ and $\overline{RSTR}$ signals are output by the timing generator. The horizontal (H) signal from the μPC1401 passes to a phase-locked loop circuit, where it is compared and locked with a horizontal signal obtained by dividing the $8f_{SC}$ clock. After the horizontal frequency has been multiplied by 2 (2H), this signal is combined with the vertical drive signal (V) from the μPC1401 for use as the composite synchronizing signal in noninterlaced scanning. Together with the R-G-B output signals, it is then passed to the TV monitor.

Figure 15. μPD6902 Pin Configuration

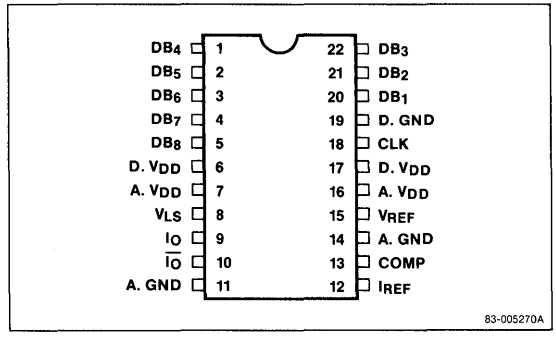
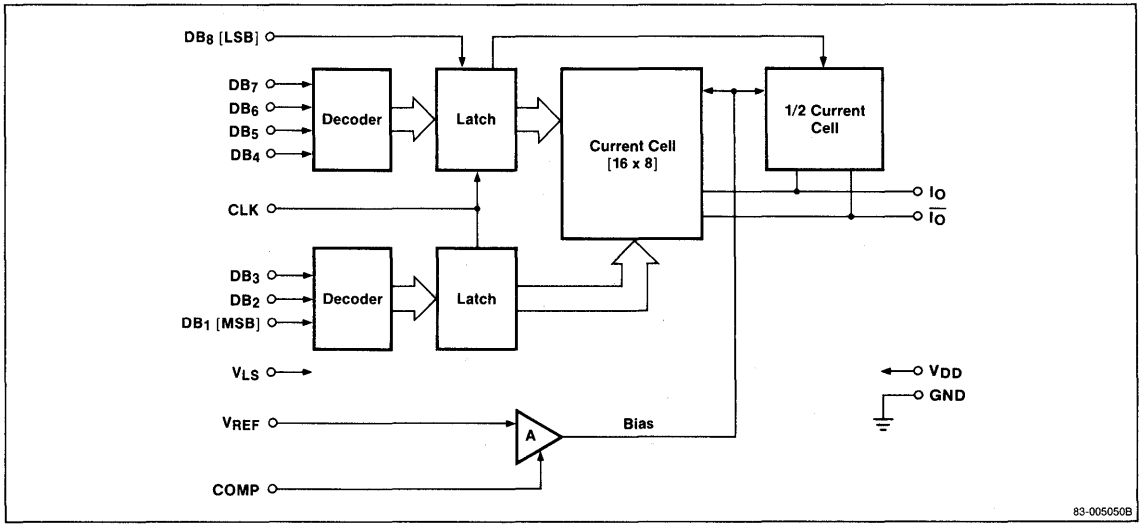


Figure 16. μPD6902 Block Diagram



The μPD42101 exactly replaces the μPD41101.

Operation

A circuit diagram for the scan converter is shown in figure 17. The operation in each block is described below.

Video Signal Input Stage

Switch SW_1 selects the NTSC video signal and applies it to the μPC1401, which decodes the composite signal and outputs R-G-B horizontal and vertical synchronizing signals. The μPC1401 integrated circuit separates color types (Y, R-Y, B-Y, G-Y) to form a matrix using three external transistors (Tr_3-Tr_5) to produce the R-G-B signal.

A 4528BC one-shot multivibrator sets the horizontal synchronizing signal to a suitable pulse width. One of the pulse signals is applied to pins 34 and 35 of the μPC1401 as the burst gate and blanking pulses; the other signal is applied to the MC4044 phase comparator for clock generation comparison purposes.

R-G-B Signal Input Stage

The R-G-B input signal passes to a 74LS08 two-input positive AND gate and then to the μPC1387 which, together with Tr_6 and the 74LS08, ensures that no signal is applied during the horizontal retracing period.

The R-G-B signal applied to the μPC1387 is adjusted to a suitable level prior to being output from that device. Conversely, the vertical and horizontal synchronizing signals are combined in the 74LS08 to form the composite synchronizing signal passed to the μPC1401 by selection switch SW_1.

A/D Conversion Stage

The R-G-B signal selected by SW_1 is passed to the μPC6950 through a 7-MHz low-pass filter to cut frequencies in excess of one-half the sampling frequency of 14.3 MHz (figure 18). This analog signal is converted by the 14.3-MHz clock and then passed to the μPC1401 as an 8-bit digital signal.

Line Buffer Stage

The 8-bit digital input is written at 14.3 MHz before being passed to the μPC6902 for D/A conversion at 28.6 MHz. The WCK, RCK, $\overline{\text{RSTW}}$, and $\overline{\text{RSTR}}$ controls for the line buffer are supplied from the timing generator (figure 19).

D/A Conversion Stage

The digital input from the μPD41101 is converted to an analog signal by the 28.6-MHz clock to reproduce an R-G-B signal of twice the horizontal line frequency.

Timing Generation Stage

An LC oscillator circuit uses a 74F04 inverter to generate the 28.6-MHz signals required for driving the line buffer and D/A converter clocks, as well as the 14.3-MHz signals required for driving the line buffer and A/D converter clocks.

The horizontal signal from the μPC1401 is passed to the MC4044 phase frequency detector for phase comparison with the horizontal signal obtained by dividing the clock from the clock generator. The resultant signal is then transferred through a low-pass filter to the 1SV164 varactor diode of a voltage-controlled oscillator to adjust the oscillating frequency (figure 20).

Three 74LS163 synchronous 4-bit counters divide the 14.3-MHz clock by a factor of 455. The resultant 31.5-kHz clock ($2f_H$) is timed by the 28.6-MHz clock and passed to the line buffer as the $\overline{\text{RSTR}}$ signal.

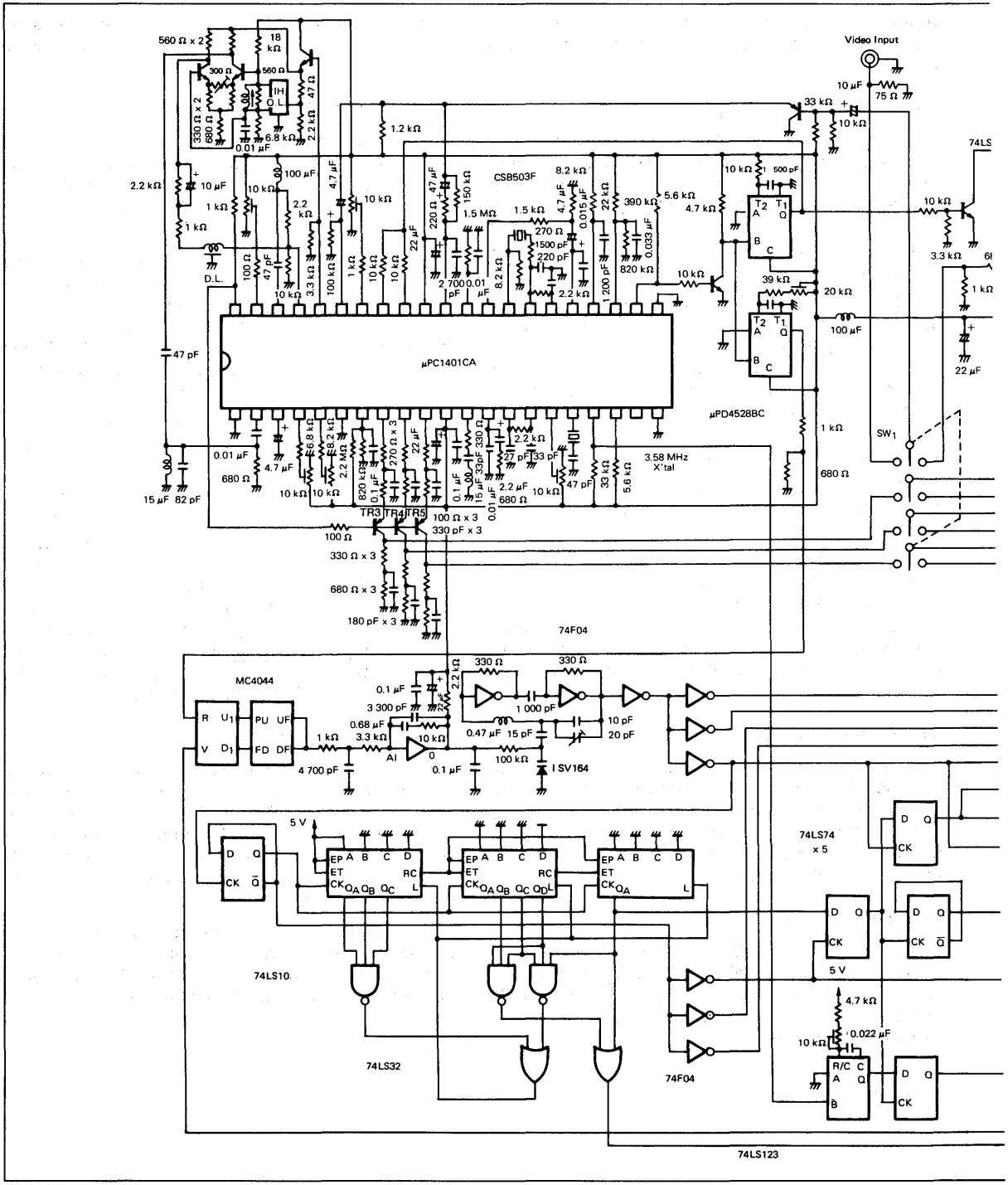
The vertical synchronizing signal from the μPC1401 is adjusted to a suitable pulse width by a 74LS123 retriggerable monostable multivibrator. The signal timed by this $2f_H$ clock is then combined with the $2f_H$ clock to obtain the composite synchronizing signal for noninterlaced scanning purposes. The $2f_H$ clock is subsequently divided in half and timed by the 14.3-MHz clock to become the $\overline{\text{RSTW}}$ signal passed to the line buffer and MC4044 (figures 21 and 22).

R-G-B Output Stage

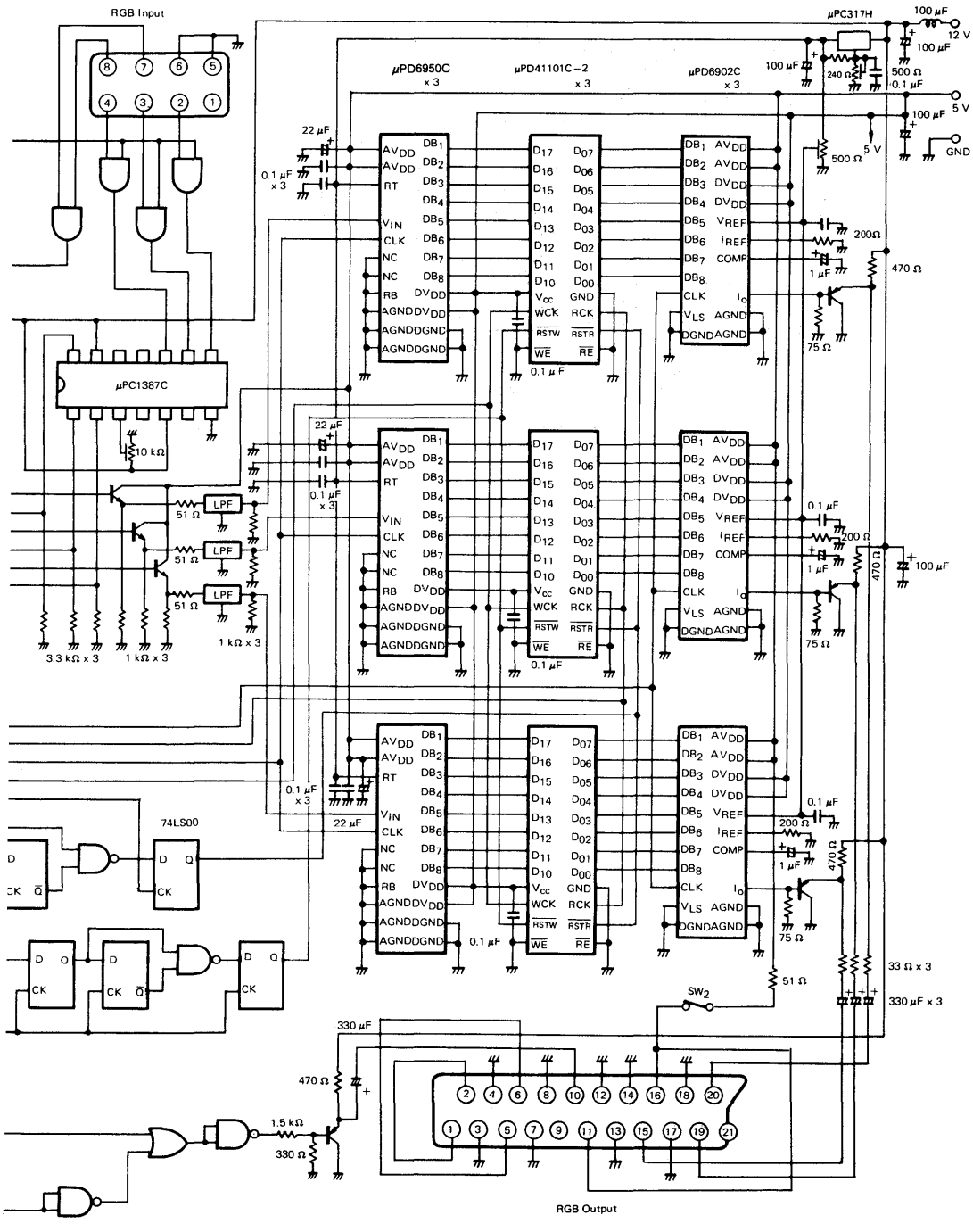
The noninterlaced R-G-B signal and the composite synchronizing signal output to the TV monitor are adjusted to levels of 0.7 and 0.3 V_{PP}, respectively, by a 75-ohm terminating resistor. Switch SW_2 is used to select external or internal display. When on, the switch allows a noninterlaced picture to be displayed externally on a TV monitor.

In this application, the TV monitor must be capable of operating at a horizontal scanning frequency of 31.5 kHz. Suitable monitors include the PC-TV451 and PC-TV471 from NEC Home Electronics.

Figure 17. μPD41101 Composite Schematic

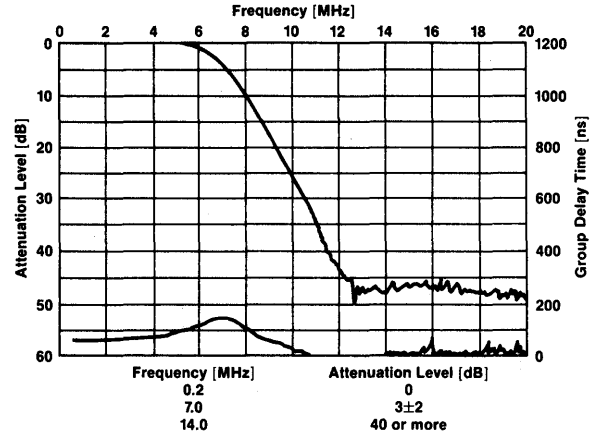


The μPD42101 exactly replaces the μPD41101.


RGB Input
μPD6950C
x 3
μPD41101C-2
x 3
μPD6902C
x 3
μPC317H
μPC1387C
74LS00
LPF
RGB Output
83-005274B

28e

Figure 18. Characteristics of LT15LP7.0M01-32 Low-Pass Filter



The μPD42101 exactly replaces the μPD41101.

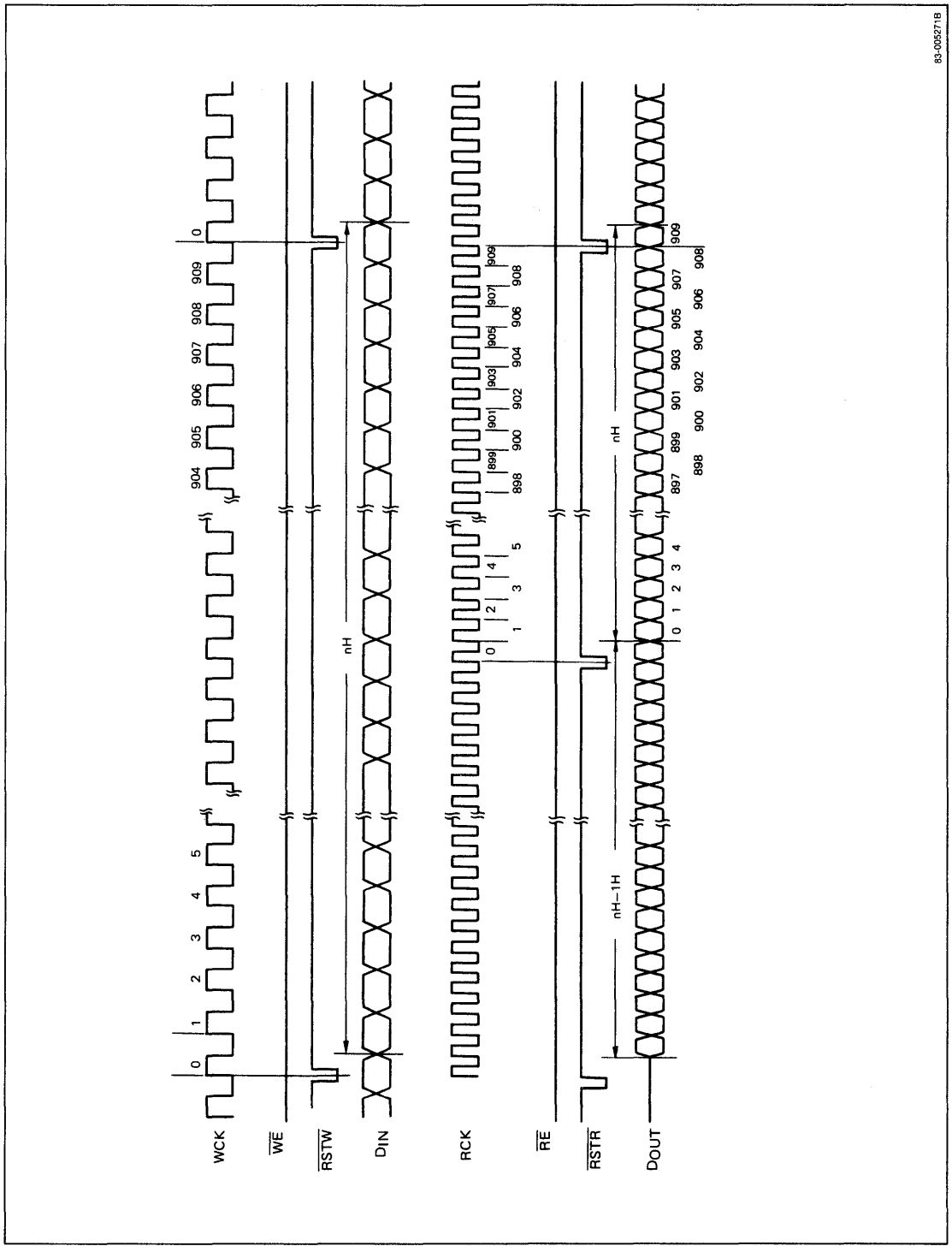


Figure 19. Scan Conversion Timing

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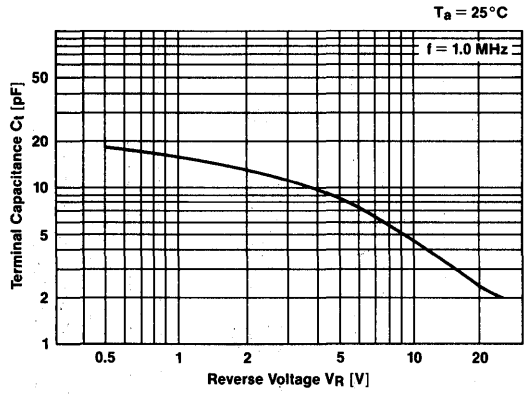
Figure 20. Characteristic Curve of 1SV164



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The μPD42101 exactly replaces the μPD41101.

Figure 21. Counter Stage of Timing Generator

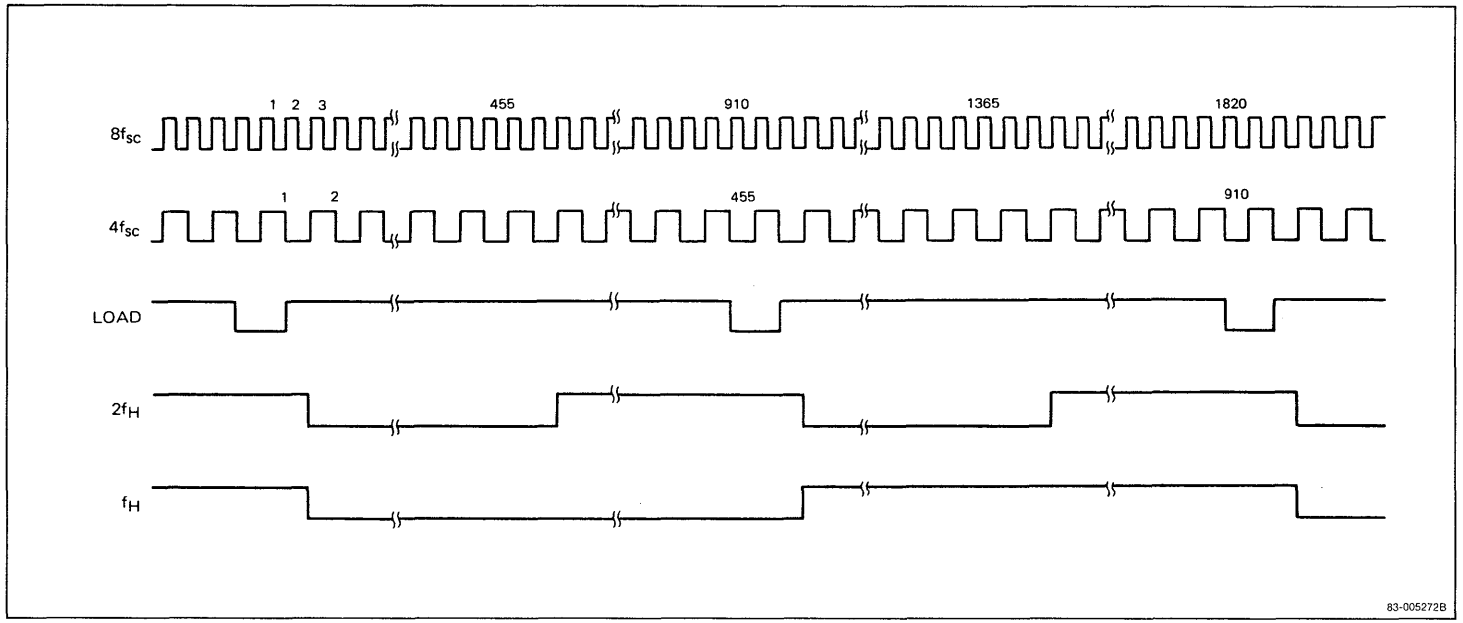
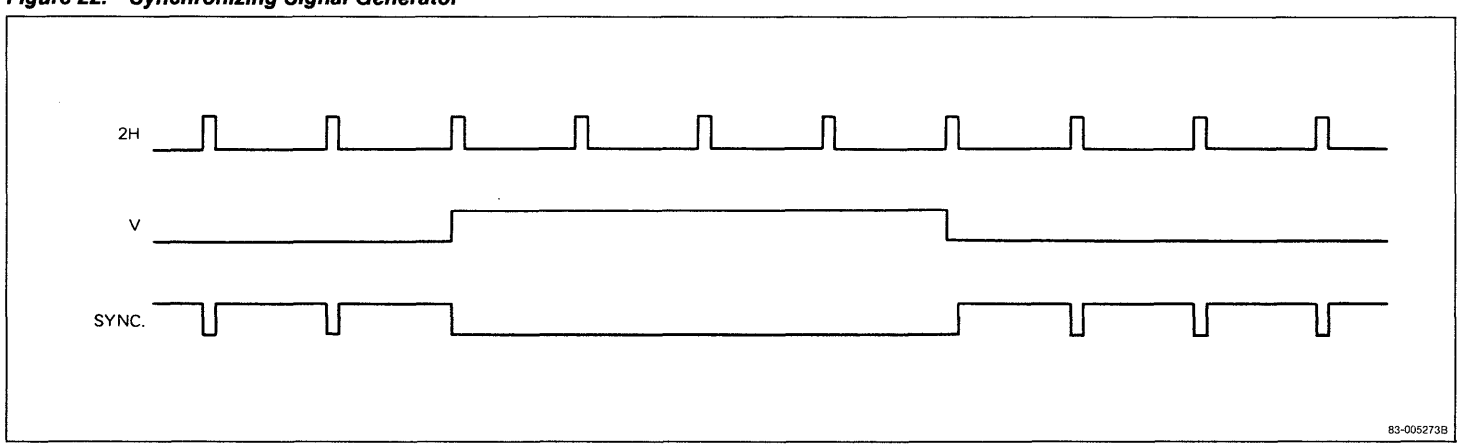


Figure 22. Synchronizing Signal Generator



Introduction

In the field of computer-aided design and manufacturing (CAD/CAM), running software with many utility programs results in time-consuming disk accesses. Workstations operating in a local area network (LAN) also are performance-limited by the heavy burden on magnetic disks serving multiple users. These systems receive a performance boost when the magnetic disk is replaced with a solid-state disk.

NEC developed the μPD42601 silicon file, a 1,048,576 x 1-bit semiconductor disk, precisely for such applications. The CMOS-fabricated μPD42601 operates much faster than hard disks, with simplified circuitry and fewer sense amplifiers than standard DRAMs. Although access times from $\overline{RAS}$ (t_{RAC}) and $\overline{CAS}$ (t_{CAC}) of 600 ns and 100 ns, respectively, make this device slower than standard DRAMs such as NEC's μPD421000, the use of word-width system architecture and page-cycle accesses achieves very high data transfer rates and can therefore improve system efficiency.

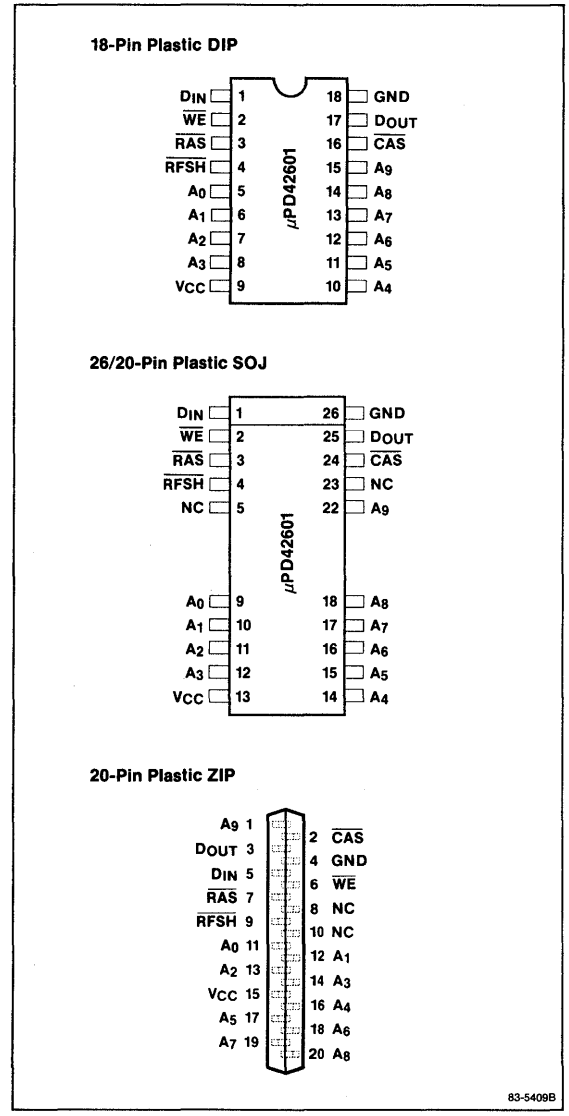
Applications

Because the device's high capacity, battery-supportable nonvolatility, and environmental hazard resistance are expected to challenge the niche previously defined by bubble devices, the μPD42601 should find its major market in large solid-state disk applications. However, as shown in table 1, other potential markets exist. For example, the μPD42601's very low data retention current, which reduces heat buildup and simplifies thermal design, means that a cool die operating in a 300-mil SOJ offers greater flexibility in packaging and stimulates new ideas for other product applications (see figure 1 for packaging options and pin assignments of the μPD42601).

Table 1. Potential Markets for μPD42601 Silicon File

Market	Requirements	Applications
Solid-state disks	High capacity Reliability Battery backup	High-end engineering workstation (100 Mbytes to 1 Gbyte)
Portable handheld products	Light weight Low power Small size	Personal computers Retail point-of-sale terminals
Industrial	Immunity to a hazardous environment: vapors, dust, vibration	Process control Robotics

Figure 1. Pin Configurations



Power and Speed Enhancements

All access cycles and timing specifications for the μPD42601 are similar to those of generic DRAMs. However, the μPD42601 requires only 25% of the operating power and 5% of the standby power of a standard DRAM, and therefore provides a better silicon solution for the aforementioned applications. The silicon file has a specified access time from $\overline{RAS}$ (t_{RAC}) of 600 ns. A quick page access time from $\overline{CAS}$ (t_{CAC}) of 100 ns is also available. Heavy system use of page cycles makes the best choice for two reasons: the first is speed enhancement over standard $\overline{RAS}/\overline{CAS}$ cycles and the second is disk sector size, which closely matches the number of bits accessible in page cycles.

In target applications for the μPD42601, low power is required. Both operating and standby power are important: low operating power results in cooler device temperatures and higher reliability, while standby currents in the microampere range allow for battery backup and small packaging options.

Self-Refreshing

The μPD42601 has a self-refresh feature similar to the one found in pseudostatic DRAMs. Bringing the $\overline{RFSH}$ pin low and clocking $\overline{RAS}$ permits the silicon file to retain data while using only 30 μA of power. In large solid-state systems, the solid-state disk would use byte-wide or word-wide banks of silicon file storage, with only one bank of devices active at a time, and all others in a state of self-refreshing. In this low-power operation, total power consumption of the system would be very low, making battery backup possible with compact batteries.

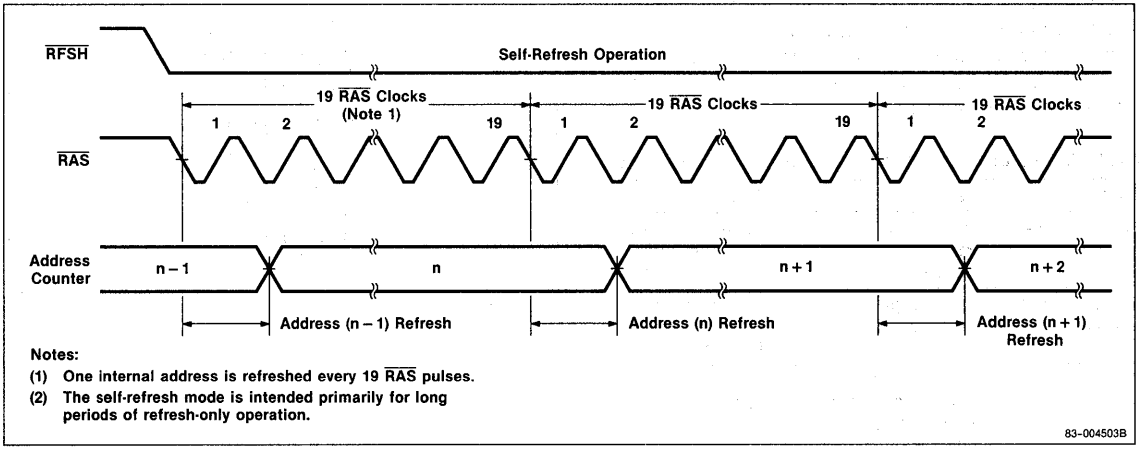
During self-refresh cycles, a relatively slow $\overline{RAS}$ clock can be applied and data integrity still be maintained. To enter this power-down quiescent state, the user can pull $\overline{RFSH}$ low and start the $\overline{RAS}$ clock at a slow cycle time (t_{RCF}). Since data loss is caused by leakage, and leakage current increases with temperature, NEC has specified the t_{RCF} rating at 50 °C, 60 °C and 70 °C. Each temperature rating has a corresponding refresh current (directly proportional to the refresh rate) which is required to maintain data, with faster rates required for higher temperatures (table 2).

Table 2. Self-Refresh Conditions

T_A	t_{RCF} (max)	Self-Refresh Current (max)
50 °C	20 μs	30 μA
60 °C	10 μs	60 μA
70 °C	5 μs	120 μA

It is important to make a distinction between self-refresh cycles and the more familiar $\overline{CAS}$ before $\overline{RAS}$ refresh cycles. When low, the $\overline{RFSH}$ pin enables self-refreshing and disables most of the internal circuits. Only those circuits required for self-refresh operation are active. Because of the rate of t_{RCF} required for substrate bias generation, nineteen $\overline{RAS}$ clocks are used in the μPD42601 to refresh one row (figure 2).

Figure 2. Internal Address Generation in Self-Refresh Operation



Notes:
(1) One internal address is refreshed every 19 $\overline{RAS}$ pulses.
(2) The self-refresh mode is intended primarily for long periods of refresh-only operation.

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Figure 3 shows a simplified block diagram of the μPD42601 during self-refresh operation. The low level of $\overline{RFSH}$ disables the ring oscillator and initializes the $\overline{RAS}$ buffer and 19-bit counter. The external $\overline{RAS}$ clock is reduced in frequency by the 19-bit counter. The outputs of the counter and the timing generator are then used to generate the slow-speed timing, decoding, and sensing operations, while the substrate bias generator functions at a reduced frequency to keep the substrate stabilized but minimize power consumption.

Figure 4 shows the transition and delay times for I_{DD1}, I_{DD2}, I_{DD3}, and I_{DD5}. When $\overline{RFSH}$ goes low, a 2.5-ms delay occurs before the device enters true self-refreshing. The timing shown in figure 4 depends on internal temperature-compensated delay circuits and is required to allow the die to stabilize at a lower temperature. During this 2.5-ms period, the standby current is specified as I_{DD3}, or 500 μA. After the die cools, the substrate bias generator operates at a lower frequency and power consumption is composed of five components: the $\overline{RAS}$ buffer, the 19-bit counter, the decoder, the substrate bias generator, and the sense amplifiers. All other peripheral circuits are disabled.

Figure 4. Transition and Delay Timing in Self-Refresh Operation

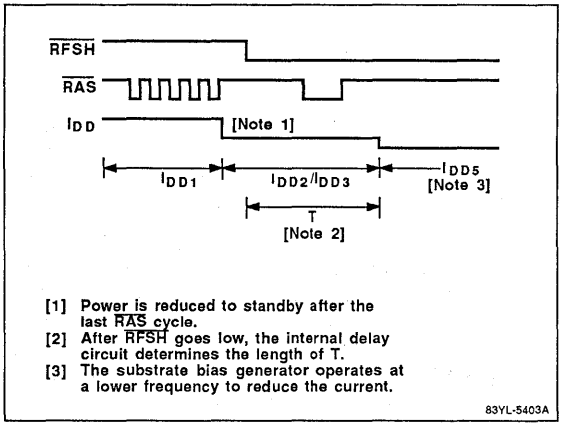
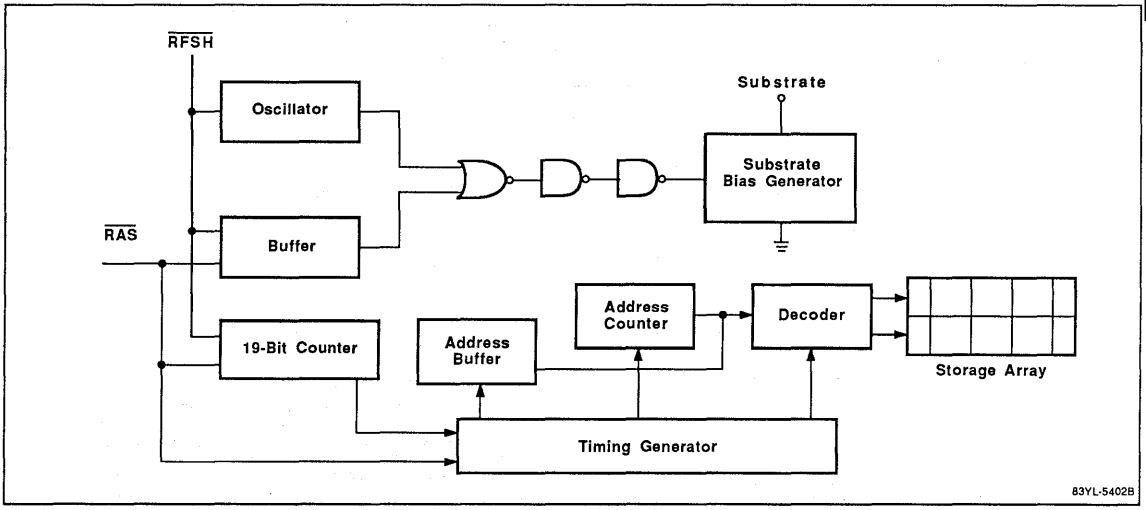


Figure 3. Circuit Operation in Self-Refresh Operation



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$\overline{CAS}$ Before $\overline{RAS}$ Refreshing

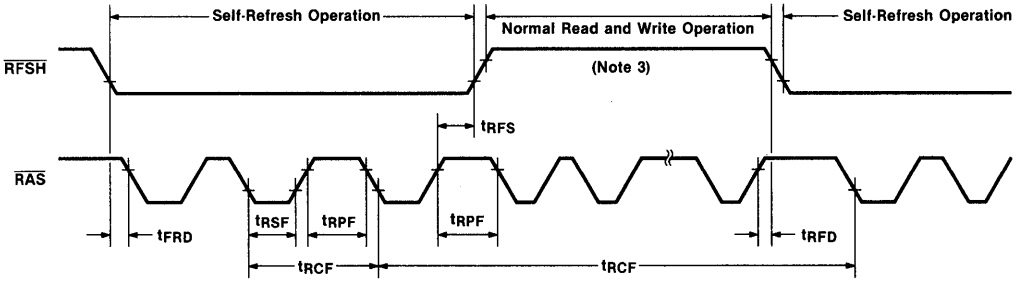
The μPD42601 does not incorporate its own automatic refresh circuits on-chip, but requires pulsing $\overline{RAS}$ in the self-refresh state to hold data. Another more descriptive term for this function is "pulse refreshing." In most pulse-refreshed devices, the method of entering and exiting self-refresh operation is crucial; however, the 1M x 1 silicon file makes transitioning between operating and self-refresh modes simpler than previous-generation pseudostatic devices.

In the case shown in figure 5, no $\overline{CAS}$ before $\overline{RAS}$ cycles are executed during a period of normal write and read cycles. Re-entering self-refresh operation after short write/read bursts limits the number of bits that could have been accessed in the relatively short time specified for t_{RCF} (i.e., the maximum cycle time for $\overline{RAS}$ in self-refresh operation).

If system timing remains in normal write or read operation longer than t_{RCF} (max), then refresh logic is needed to control $\overline{CAS}$ before $\overline{RAS}$ refreshing. Every 32 ms, 512 refresh cycles are needed to refresh the 512 row addresses, an average rate of one every 62 μs. Because of the reduced operating current and the resultant lower die temperature, the refresh period can be extended to four times the 8-ms value specified for most 1M x 1 DRAMs.

In $\overline{CAS}$ before $\overline{RAS}$ cycles, addresses need not be supplied because an internal counter supplies them to the decoders. Since the clocks for both $\overline{CAS}$ before $\overline{RAS}$ refresh cycles and self-refresh cycles increment the same internal address counter, there are orderly and sequential transitions from self-refreshing to $\overline{CAS}$ before $\overline{RAS}$ refreshing and back to self-refreshing. Ensuring that the row addresses are refreshed in a timely fashion is the function of the refresh counter, which is clocked by $\overline{CAS}$ before $\overline{RAS}$ during normal cycles and at the rate of $1/(19 \times t_{RCF})$ during self-refresh cycles. The μPD42601 runs cooler than other self-refreshing devices and does not require a burst of extra $\overline{CAS}$ before $\overline{RAS}$ cycles before self-refreshing to ensure data integrity.

Figure 5. Special Requirements for t_{RCF} Near Periods of Limited Standard Refresh Cycles



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50 °C	20 μs	5 μs
60 °C	10 μs	5 μs
70 °C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] In this period of normal read/write operation, there are no CBR refresh cycles or less than 512 $\overline{RAS}$-only refresh cycles.

[4] The time delay between the last self-refresh pulse in one self-refresh cycle, and the first self-refresh pulse in the next cycle, is defined by t_{RCF} [max] when the intervening period of read and write operation meets the conditions in Note 3.

[5] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

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As discussed earlier, a lower die temperature permits both a relaxed refresh rate and simplified transition timing between self-refresh and normal write and read cycles. The die temperature is a function of the ambient temperature, operating power, and the junction-to-ambient thermal resistance (θ_{JA}). The calculations showing the increase of junction temperature (T_J) over ambient temperature (T_A) at maximum power consumption (P_D max) are shown in the sequence below.

(1) $T_J = (\theta_{JA} \times P_D) + T_A$

(2) $T_J = [95\,°C/W \times (5.5\ V \times 12\ mA)] + 55\,°C$

(3) $T_J = 61.27\,°C$

In a solid-state disk system where the air temperature stabilizes at 55 °C, the silicon file chip temperature would not exceed 61.27 °C, comparing favorably with the die temperature of 81 °C or more for a standard DRAM encapsulated in a plastic SOJ and operating in similar conditions.

Figure 6 shows the maximum specification for t_{RCF}, the critical parameter when transitioning between $\overline{CAS}$ before $\overline{RAS}$ and self-refresh cycles. When exiting self-refresh operation, t_{RCF} (max) is measured between the falling edges of $\overline{RAS}$, from the last self-refresh cycle to the first $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. After transitioning from self-refresh operation to a period of normal write or read cycles, writing and reading can proceed for only 5 μs (at 70 °C) before a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is required. When transitioning from write and read operation to self-refresh operation, the process is simply reversed, with t_{RCF} (max) referenced between the last $\overline{CAS}$ before $\overline{RAS}$ refresh cycle and the first self-refresh cycle.

$\overline{RAS}$-only refreshing does not increment the refresh counter, complicating the procedure for moving between refresh modes. In refresh methods other than $\overline{CAS}$ before $\overline{RAS}$, a burst of 512 refresh cycles is required before entering and also after exiting self-refresh operation. Complete refreshing of all rows is needed since, in refresh modes other than $\overline{CAS}$ before $\overline{RAS}$, the status of the refresh counter is unknown and the maximum specification for t_{RCF} may be exceeded. When the self-refresh capability is used, then $\overline{CAS}$ before $\overline{RAS}$ refreshing is recommended.

Soft Error Performance

Like the 1M x 1 DRAM, the μPD42601 uses the trench cell for a small die size and excellent immunity to alpha particles. Accelerated soft error results are less than 1000 FITs (Failures In Time, or errors in 10^9 device-hours) . With low manufacturing cost as an objective, the device includes no error correction circuit (ECC), parity, or data checking functions on-chip. Most customers prefer to implement these functions off-chip.

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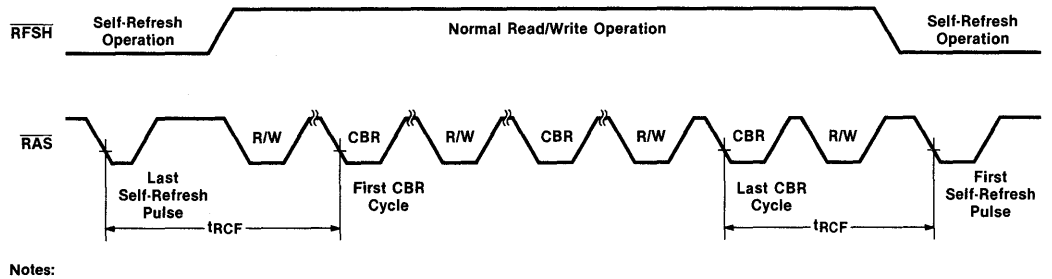
Figure 6. Timing Restrictions Entering and Exiting Self-Refresh Operation



Notes:

[1] The value for t_{RCF} [min] is specified in AC Characteristics. The value for t_{RCF} [max] is dependent upon temperature and shown in the table below.

	t_{RCF} [max]	
T_A	μPD42601-L	μPD42601
50 °C	20 μs	5 μs
60 °C	10 μs	5 μs
70 °C	5 μs	5 μs

[2] When exiting self-refresh to a period of read and write operation which includes CBR refresh cycles, t_{RCF} is the delay between the last self-refresh pulse and the first CBR cycle. When entering self-refresh operation, t_{RCF} is the delay between the last CBR cycle and the first self-refresh pulse.

[3] The built-in counter generates the refresh address in self-refresh and CBR refresh cycles. Since this address increments sequentially from the last cycle in either self-refresh or CBR operation to the first cycle in the alternate refresh mode, CBR refreshing should be used during normal read and write operation to refresh one address location every 62 μs or less. If some other means of refreshing is used, it is necessary to do a burst refresh of all storage cells just before changing to and just after exiting self-refresh operation.

83-004501

Silicon File-Based Solid-State Disk System

To assist our customers in the design-in of the μPD42601, NEC undertook a 20-Mbyte solid-state disk hardware project, a block diagram of which appears in figure 7 and a photograph in figure 8 (the hardware enclosure was designed for expansion to 40 Mbytes). Contained within the same package form factor as a 5.25-inch Winchester, the solid-state disk system includes batteries, a power supply, and the necessary power fail logic to provide complete nonvolatility for up to one month. The error correction device is a gate array developed at NEC and is not commercially available. A specification summary of this application project is shown in table 3.

Table 3. Specification Summary

Parameter	Specification
Capacity	20 Mbytes
Interface	SCSI (host)
Data transfer rate	1.5 Mbytes/sec (max)
Access time	0.1 ms (max)
Error correction	1-bit correction and 2-bit detection
Sector size	256 or 512 bytes
Power supply	5 volts, 2 amps
Package size	5.25-inch disk
Battery voltage	4.8 volts
Battery backup	One month
Operating temperature	5 to 50°C

Description of the Block Diagram

For the purpose of explanation, the block diagram in figure 7 and the following system description are detailed according to the format shown in table 4.

Table 4.

Major Functional Blocks	Major Components
Power source/switch	Battery, power control circuits
Silicon file and ECC	μPD42601LA, ECC gate array
Timing generator circuits	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ logic
Data/address control	V40™, WD33C93™, RAM, ROM

Power Supply and Power Fail Circuits

The upper left corner of the block diagram consists of the battery, power switch, voltage detector, and power fail circuits. Included in the power switch is a 5-volt switching regulator and the power conversion circuits. When the detector senses the falling power supply voltage, the power switch supplies the battery voltage to the components shown within the shaded block (battery backup). At the same time, the power fail logic sends a nonmaskable interrupt (NMI) to the V40, which initiates an internal subroutine and places the microprocessor in the low-current HALT mode.

When system power is restored, the rising voltage is detected. After a delay, the power switch disconnects the battery source and allows the 5-volt supply to power the system. Once the V40 receives the second NMI and resets the processor, $\overline{RFSH}$ goes inactive and normal timing resumes.

To ensure nonvolatility and reduced battery current drain, the silicon file devices must be placed in self-refresh operation when system power fails. In figure 7, the power fail logic has two outputs: one called self-refresh, which pulls $\overline{RFSH}$ low on all the storage chips, and a second output connected to the control pins of the V40 and the timing generator block. This output is actually two lines: one for the V40 NMI input initializing HALT mode and the second for initializing the timing generator circuits. When this output signal is active, the power fail logic switches the timing for $\overline{RAS}$ from normal read/write/refresh timing to the self-refresh oscillator. For this application, the self-refresh frequency is set at 50 kHz because this system is specified to operate at 50°C (maximum).

Storage Organization with ECC

The solid-state disk is organized as five banks of 39 devices, a 32-bit internal data word and an additional 7 bits for the ECC check bits. The ECC device is capable of 2-bit detection and 1-bit correction.

A 32-bit data bus is acceptable for the ECC chip, but the V40 and the SCSI interface controller require a byte-wide bus. The lower right corner of figure 7 shows a four-section register to accomplish this 32- to 8-bit conversion. This register is composed of eight octal bus transceivers with eight enable lines generated in the timing generator block. Four of these transceivers are used for the input side and four are used for the output side. The four octal bus transceivers (4 x 8 bits) comprise the 32-bit-wide data bus. The enable signals select one of the four transceivers receiving and sending each byte to or from the 8-bit data bus.

V40 is a trademark of NEC Corporation.
WD33C93 is a trademark of Western Digital.

Figure 7. Block Diagram of Silicon File Disk

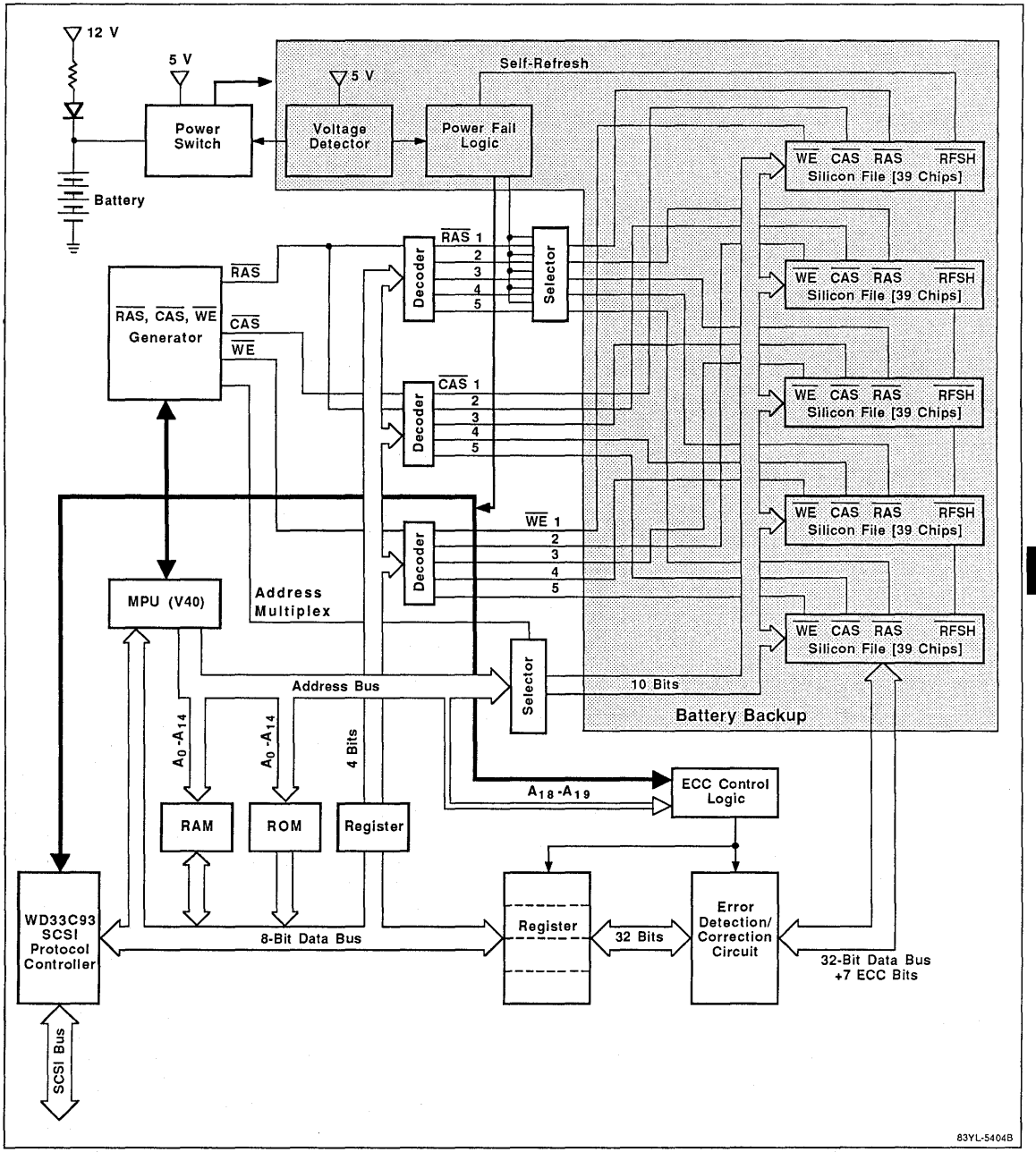


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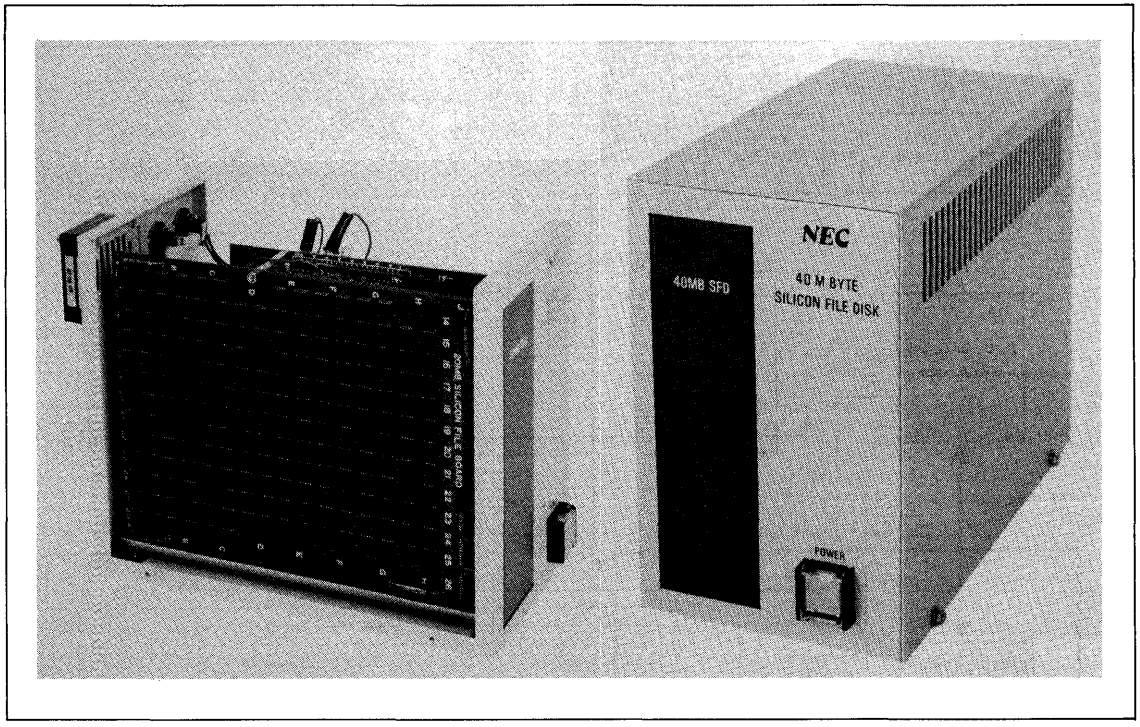
Figure 8. Photograph of Silicon File Disk



Timing Generation and Decoding

The timing generator block consists of a delay line, several PALs®, and glue logic. Its purpose is to control write and read operation and $\overline{CAS}$ before $\overline{RAS}$ timing. One of the PALs is used for decoding the eight enable signals used in the 32- to 8-bit multiplexing and demultiplexing operation discussed in the preceding section. Selecting one of five of the storage banks is accomplished by decoding $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$. This function, together with the selection of the self-refresh oscillator, is contained in the logic blocks shown to the left of the storage array. The self-refresh oscillator is contained in the power fail logic block.

Data Transfer Control [V40 and SCSI Controller]

In this system, the SCSI controller is the target and the host computer connected to the SCSI controller is the initiator. Although a solid-state device is not a disk in that it has no cylinders, heads, or sectors, the V40 has been designed to handle all the control, data transfer, and address translation functions. Used as a microcontroller, the V40 makes the silicon disk look like a magnetic disk to the WD33C93.

Read Operation

Upon receiving the input/output command from the host system, the host adapter arbitrates and wins bus control. The target, the SCSI controller in this case, is selected and receives the read instruction and starting address from the host adapter. This information is stored as part of the command data block in the SCSI controller's internal register. At this point, the host disconnects. The V40 first recognizes the read command and the address and then sets the proper bits in the WD33C93 address register. Under V40 control, data is accessed from the correct logical address in the silicon file and moved to the μPD43256A buffer RAM.

Once the silicon file has started filling the RAM, the SCSI adapter can reconnect to the host. During this phase, the target arbitrates for the bus and wins control of it. The host is selected and the target sends the message that it is reconnecting. Under control of the V40, data is moved from the RAM to the SCSI controller and is received by the host adapter completing the operation. With this fast semiconductor disk, the data transfer rate depends more on arbitration time than on device access time.

PAL is a registered trademark of Advanced Micro Devices, Inc.

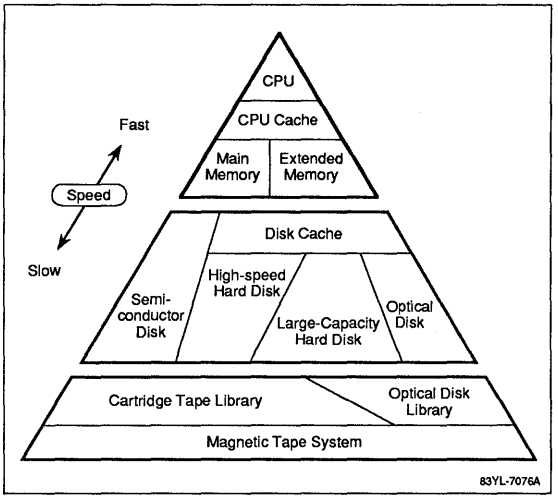
Application Note 90-06
Silicon File System Architecture

Introduction

The objective in designing a hierarchical memory system is to match the processor's speed either with the rate of information transfer or with the bandwidth of the memory at the lowest level, at a reasonable cost. No one type of device meets all criteria, i.e., inexpensive, reliable, fast and nonvolatile. In fact, the hierarchy in most computers is often organized so that the highest level has the fastest speed and the lowest level has the lowest speed, e.g., a cache typically resides in the highest level and contains the fastest and most expensive memory, the next level contains random access devices that are 5 to 10 times slower than the cache, and the lowest level has the slowest and cheapest devices.

In the past, there has existed a technology gap between the faster primary and the slower secondary memories (figure 1). Average access time of secondary devices, most often magnetic disks and drums, is 1000 to 10,000 times slower than that of primary devices. Electronic disks such as charge-coupled devices and magnetic bubble memories have not proved cost-effective in closing the gap and thus have had little impact on system design.

Figure 1. Memory Hierarchy



Standard semiconductor memory in the secondary level is able to bridge this gap, and of the various alternatives, battery backed-up static RAM and EPROM/EEPROM technologies historically have been used in solid-state nonvolatile systems. Typically they have been restricted to low-capacity applications, since the high cost of static RAMs prohibits using them in place of magnetic media or in applications where the operating environment makes rotating media unreliable.

NEC's μPD42601 silicon file, a device with higher performance, higher capacity, and lower power requirements is also able to bridge this performance gap. Based on DRAM technology, the μPD42601 provides the capacity and reliability of a standard DRAM, but also features a way to retain data by means of batteries when power is shut off. It also offers the reliability and ruggedness of solid-state memories, as well as lighter weight, higher I/O bandwidth, and simpler interfacing.

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Functional Overview

Standard Operation. The silicon file is specifically designed to replace magnetic media in silicon disk, solid-state recording, and system backup applications. It is based on the trench cell technology of NEC's 1M DRAMs and implements the same read and write cycles (figure 2), but optimizes system bandwidth with a page cycle that repeatedly pulses $\overline{CAS}$ while maintaining $\overline{RAS}$ low (figure 3). The silicon file also periodically executes standard $\overline{RAS}$-only and $\overline{CAS}$ before $\overline{RAS}$ refresh cycles to refresh its cells within a specified interval of 32 ms, which is four times slower than a 1M DRAM.

Low-Power Operation. An important feature of the silicon file is its ability to retain data while being powered by a backup battery. This is accomplished by means of a self-refresh cycle that can be used in applications requiring a low data retention or self-refresh current. The $\overline{RFSH}$ control signal goes low while the $\overline{RAS}$ signal is clocked at a relatively slow rate (t_{RCF}). Since data loss is caused by leakage, and leakage current is a function of temperature, t_{RCF} is specified at three temperature ratings: 50°C, 60°C, and 70°C. Each rating has a corresponding refresh current (directly proportional to the refresh rate) which is required to maintain data (table 1).

Figure 2. Read Cycle

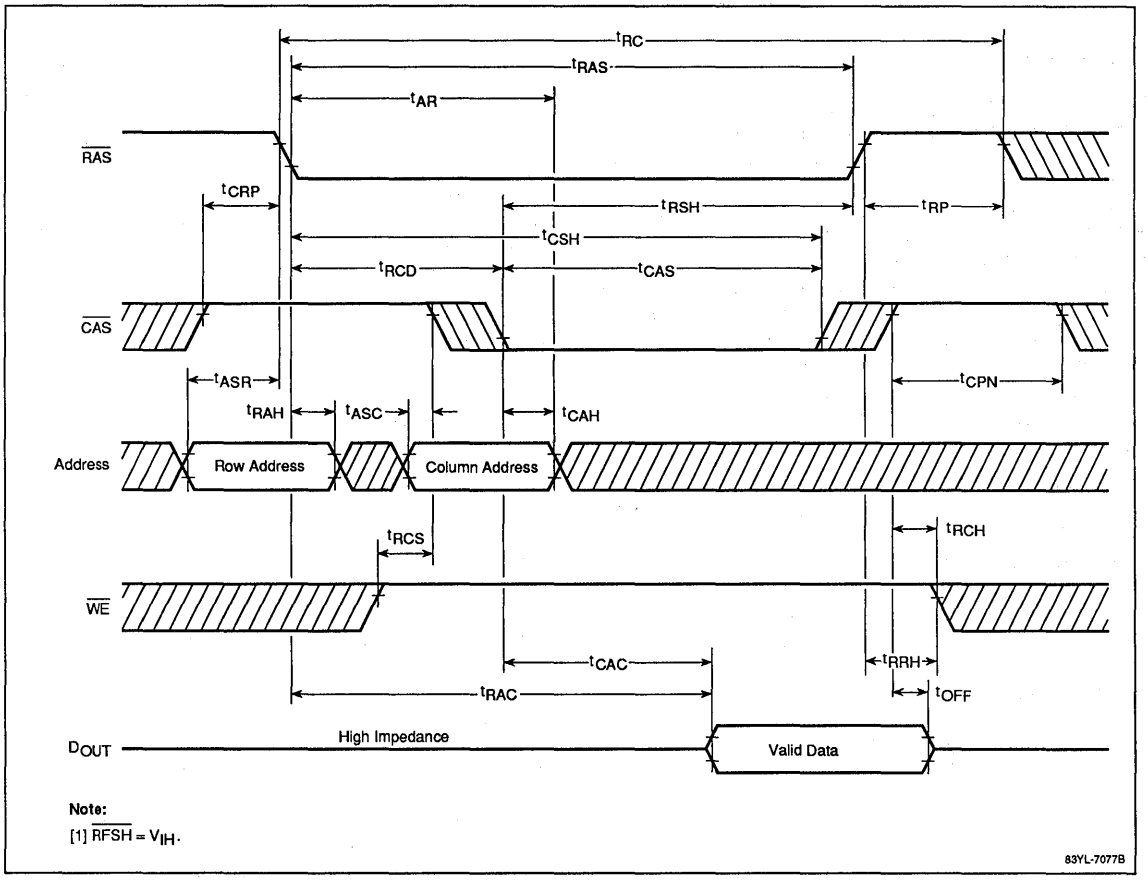

Table 1. Self-Refresh Current Versus Clock Frequency and Temperature

Type	Temperature	RAS Clock	Maximum Current
μPD42601-60L	0 to 50°C	50 KHz	30 μA
	0 to 60°C	100 KHz	60 μA
	0 to 70°C	200 KHz	120 μA
μPD42601-60	0 to 70°C	200 KHz	120 μA

Self-refresh cycles are intended to be used when power to the silicon file's memory array is shut down for an extended amount of time. In this case, the system backup circuit is required to provide to the memory array a backup supply voltage of between 4.5 and 5.5 volts while pulsing RAS at the given t_{RCF} frequency and driving RFSH low. As long as the circuit can maintain these operating conditions, the silicon file will retain data (figure 4).

Special consideration must be given to the requirements for t_{RCF} near periods of limited standard refresh cycles, and to the time restriction when entering and exiting self-refresh operation (refer to the data sheet for the μPD42601 as well as *Application Note 56*).

Comparison with 1M DRAMs

Table 2 compares the functions of the μPD421000 DRAM with the μPD42601 silicon file. Both have a similar 1M x 1 organization and interface circuit, and both are available in the same high-density 26/20-pin plastic SOJ and 20-pin plastic ZIP packages.

Figure 3. Page Read Cycle

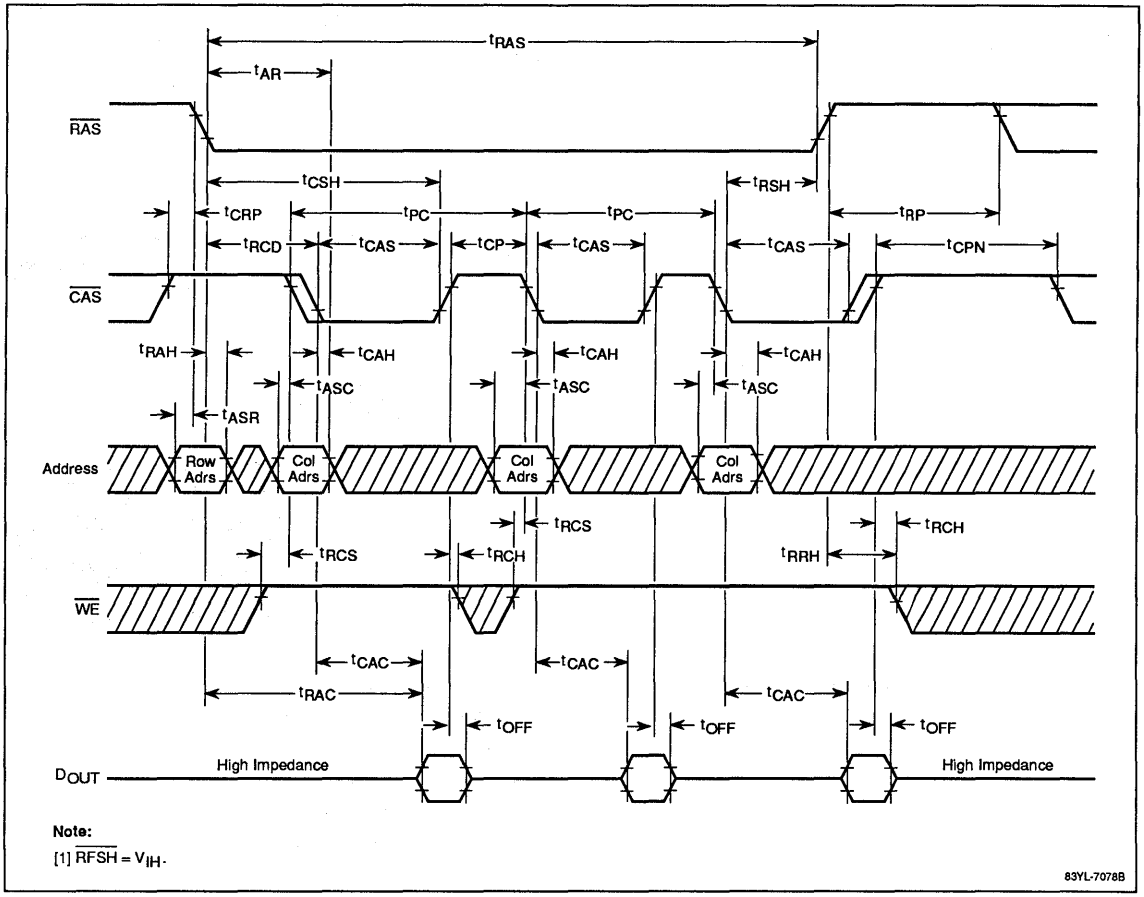

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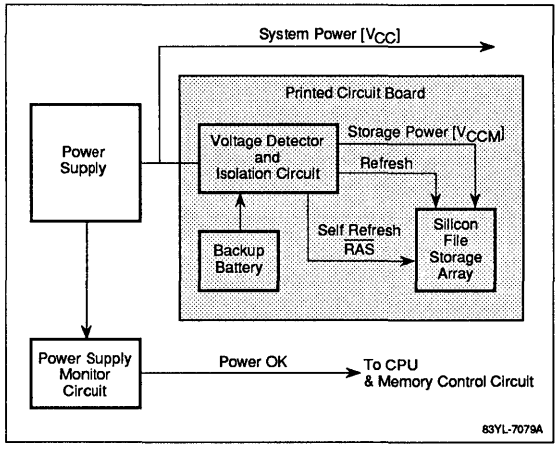
Table 2. Comparison of Silicon File to Standard DRAM

Part Number	Organization	Pinout	Package	Access Times	Active Power	Refresh Operation
μPD421000	1M x 1	Standard	26-pin plastic SOJ 20-pin plastic ZIP 18-pin plastic DIP	***Fast-Page*** t_{RAC} = 120 ns t_{CAC} = 30 ns t_{PC} = 70 ns ***Standard*** t_{RAC} = 600 ns t_{CAC} = 100 ns t_{PC} = 200 ns	40 mA max 14.8 max	$\overline{CAS}$ before $\overline{RAS}$ refreshing $\overline{RAS}$-only refreshing Refresh current = 50 mA max Standby refresh current $\overline{RAS}$ cycle at 64 KHz = 1.7 mA
μPD42601	1M x 1	Standard plus $\overline{RFSH}$ pin	26-pin plastic SOJ 20-pin plastic ZIP	***Page*** t_{RAC} = 600 ns t_{CAC} = 100 ns t_{PC} = 200 ns	12 mA max	$\overline{CAS}$ before $\overline{RAS}$ refreshing $\overline{RAS}$-only refreshing Refresh current = 10 mA max Self-refresh current ($\overline{RAS}$ cycle) 50 KHz = 30 μA 100 KHz = 60 μA 200 KHz = 120 μA

Figure 4. Block Diagram of Backup Circuit for Self-Refreshing



Access Time and Power Comparison

The 1M DRAM is designed for high performance at low cost. Its optimized technology, also used in the silicon file and based on NEC's CMOS process and trench memory cell, is proven to provide high reliability, excellent immunity to alpha particles, and accelerated soft error rates of less than 1000 FITs (Failures in Time or errors in device-hours).

Figure 5 shows a comparison of the die layouts for the silicon file and 1M DRAM. The 1M DRAM is segmented into 16 memory cell arrays with appropriate column decoders and sense amplifiers separating each pair of arrays. This highly segmented approach is used to reduce the length of the bit line, which in turn reduces bit line capacitance and results in a faster access time.

Conversely, the eight memory cell segments and eight sense amplifiers in the simplified layout of the silicon file optimize power consumption rather than access time. The silicon file has a slower access time and lower active current, and although active current can be reduced in any DRAM if cycle time is also reduced, active current in the silicon file is still much lower than active current in a DRAM when both are operating at a 1 μs cycle rate.

When a standard DRAM and the silicon file are not being accessed by the system, they operate in standby and dissipate a current much lower than their active current. Standby is used by both devices to reduce system power requirements during normal system operation. The silicon file also has a unique self-refresh

cycle that isn't implemented on a standard DRAM and can operate at very low currents, as low as 30 μA, and still retain data via a battery powered backup system. Furthermore, the silicon file uses an additional $\overline{RFSH}$ pin (pin 4 on the 20/26-pin SOJ and pin 9 on the 20-pin plastic ZIP).

System Design

When considering a system design using the silicon file, the system designer will recognize a number of similarities with the 1M DRAM. Both devices use the same x1 organization, as well as $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and A_0 through A_9, and both are available in the same SOJ and ZIP package types. Typically, a silicon file system design will be functionally similar to a standard DRAM system, making it very easy for the designer to use traditional DRAM system design techniques.

Figure 6 shows an interface between the silicon file and a host interface. It is very similar to a DRAM system, except for the power monitor and backup circuit used to implement self-refreshing. The interface circuit is application-dependent, and can be an interface to a variety of standard I/O or memory interfaces.

Figure 5. Die Comparison of 1M DRAM and Silicon File

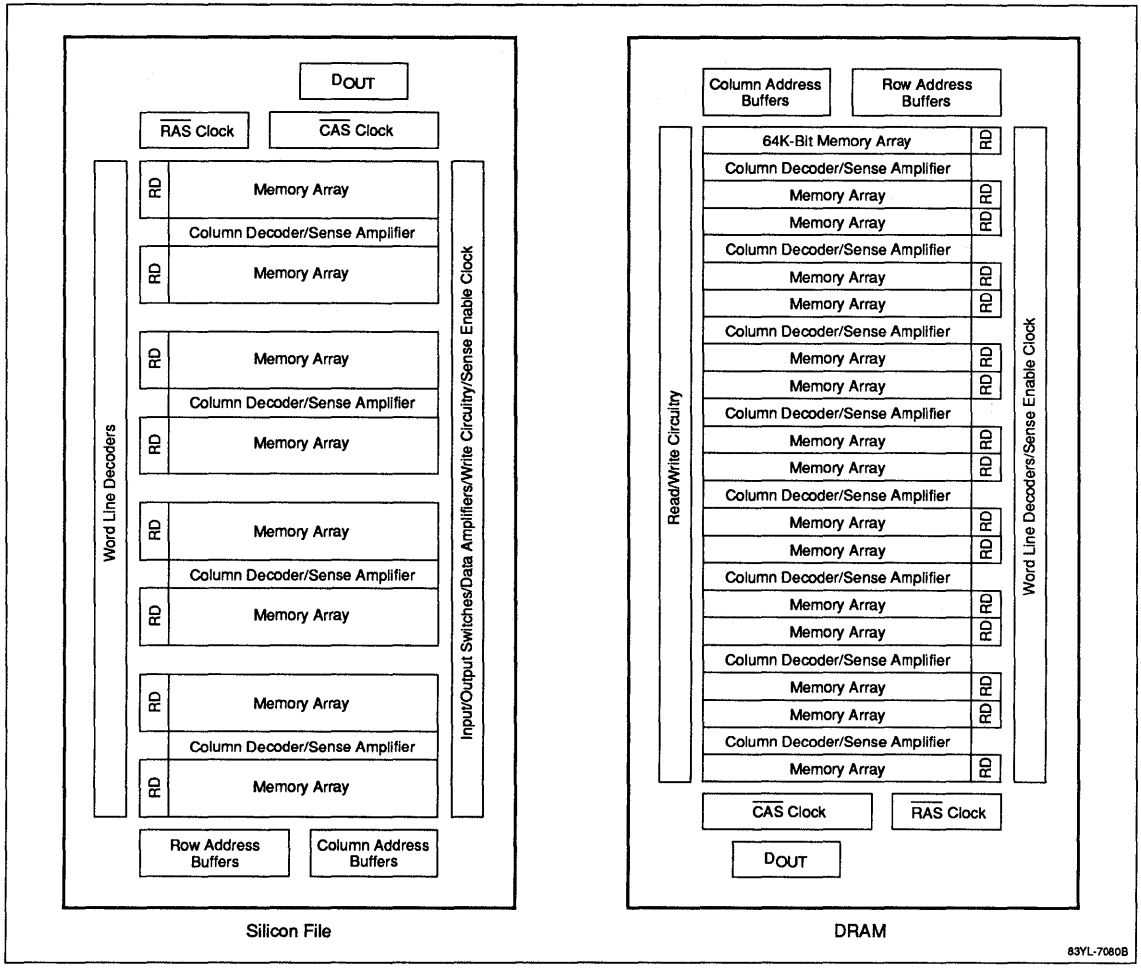


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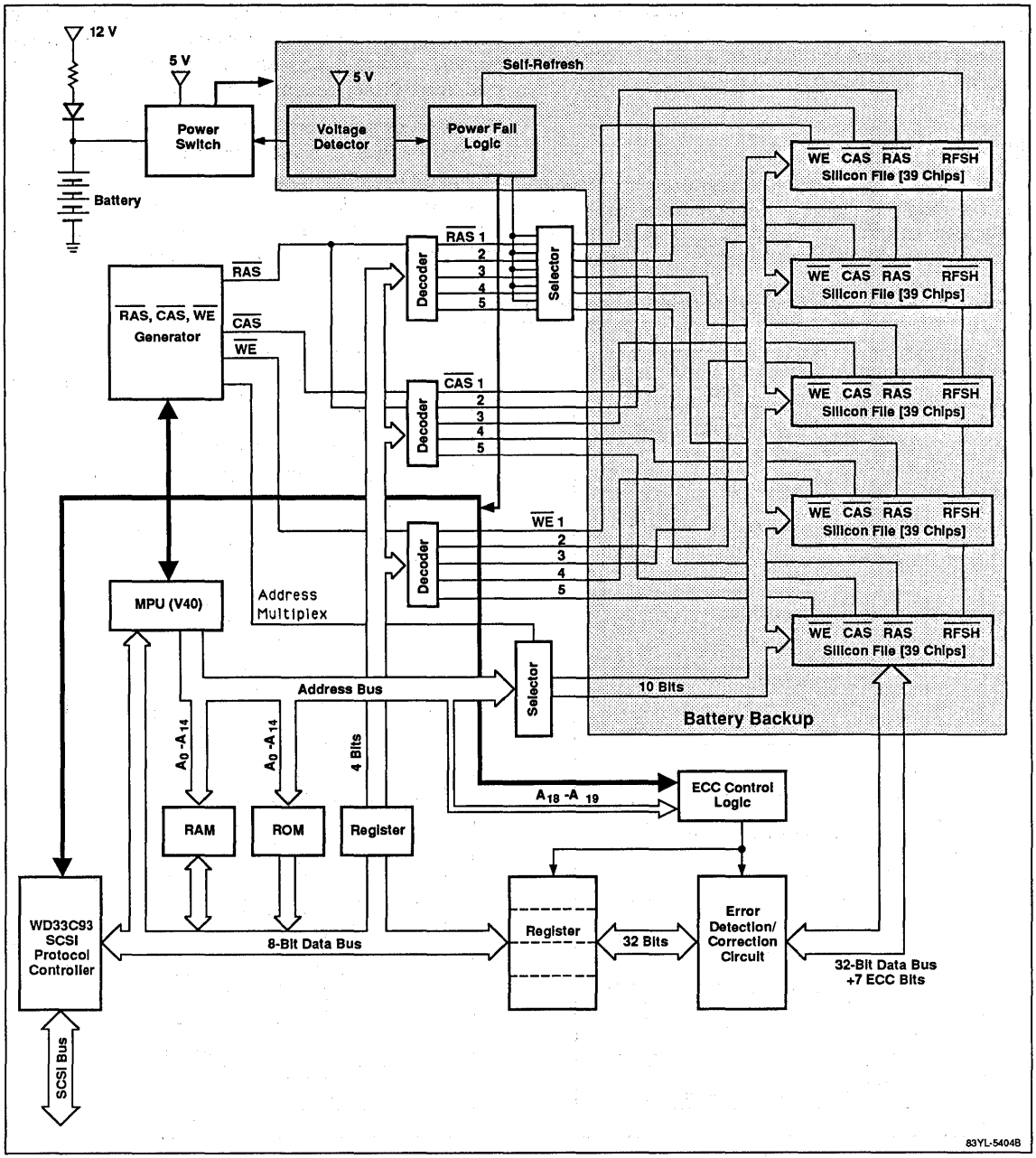
Figure 6. Block Diagram of 20 Mbyte Solid-State Disk System



The control circuit supervises interaction between the host interface and the storage array of the silicon file, translating signals from the host interface into silicon file access cycles and controlling the transfer of data on the host interface bus. The power monitor and backup circuit track power supply voltage for power failures or shutdowns, and maintain memory data by generating control signals for self-refresh cycles and battery backup voltage. To increase system reliability, an error correction and detection circuit, such as a parity bit or ERCC, may be implemented. One common design characteristic is that the silicon file control and memory array circuits will remain application-independent, while the system interface circuit will be application-dependent.

Control Circuitry

This section focuses on the circuitry of a silicon file system, and in particular on the application-independent control circuits and various system interfaces.

The similarity between the silicon file and a 1M DRAM extends to the organization of their memory cells in a matrix of rows and columns, with each individual cell accessed by first addressing a row and then a column (figure 7). The external address is presented to the silicon file in two parts, as shown in the waveform in figure 2. The row address first is driven on the address input pins and $\overline{RAS}$ goes low to clock the row address into an internal row address latch. The row address must be stable for the specified setup time of t_{ASR} before $\overline{RAS}$ is asserted, and also for the specified hold time of t_{RAH} after $\overline{RAS}$ is asserted.

The address inputs are then changed to column addresses and $\overline{CAS}$ is asserted. $\overline{CAS}$ also serves as the output enable signal, in that the three-state driver is enabled whenever $\overline{CAS}$ is asserted. The time when $\overline{CAS}$ can be asserted is determined by the minimum requirements for a $\overline{RAS}$ to $\overline{CAS}$ delay, as specified by t_{RCD}. Additionally, setup and hold times for $\overline{CAS}$ must be met. Presenting the address in two parts has the advantage of reducing by 50% the number of address pins and the package size. The silicon file is typically used in large memory systems where chip size is an important consideration.

Data is available after the access times from both $\overline{RAS}$ (t_{RAC}) and $\overline{CAS}$ (t_{CAC}) have been satisfied. The limit of performance is determined by the access time from $\overline{RAS}$. If the assertion of $\overline{CAS}$ is delayed longer than required, then maximum performance will not be obtained and access time from $\overline{CAS}$ will determine the overall access time.

Another specification of importance is the t_{RP} precharge time for $\overline{RAS}$, which is required for the memory circuit to recover from the previous access. Because a read cycle destroys the data in an addressed memory cell, a precharge cycle must be executed to restore the data and equalize signal levels on the bit lines. Thus, the cycle time for a silicon file is greater than the access time. The difference between access time and cycle time is equal to the precharge time, e.g., a silicon file with an access time of 600 ns will have a cycle time of 1 μs.

Figure 8 shows the timing for an early write cycle. The addressing sequence is the same; the only difference is that $\overline{WE}$ is asserted, and data is supplied by the CPU on the D_{IN} pin. There are two types of write cycles, depending upon the timing relationship between $\overline{WE}$ and $\overline{CAS}$. Figure 8 shows the $\overline{WE}$ signal being asserted before $\overline{CAS}$. In this case, setup and hold times are referenced to the falling edge of $\overline{CAS}$. In a late write cycle, $\overline{WE}$ is asserted after $\overline{CAS}$.

Figure 7. Silicon File Block Diagram

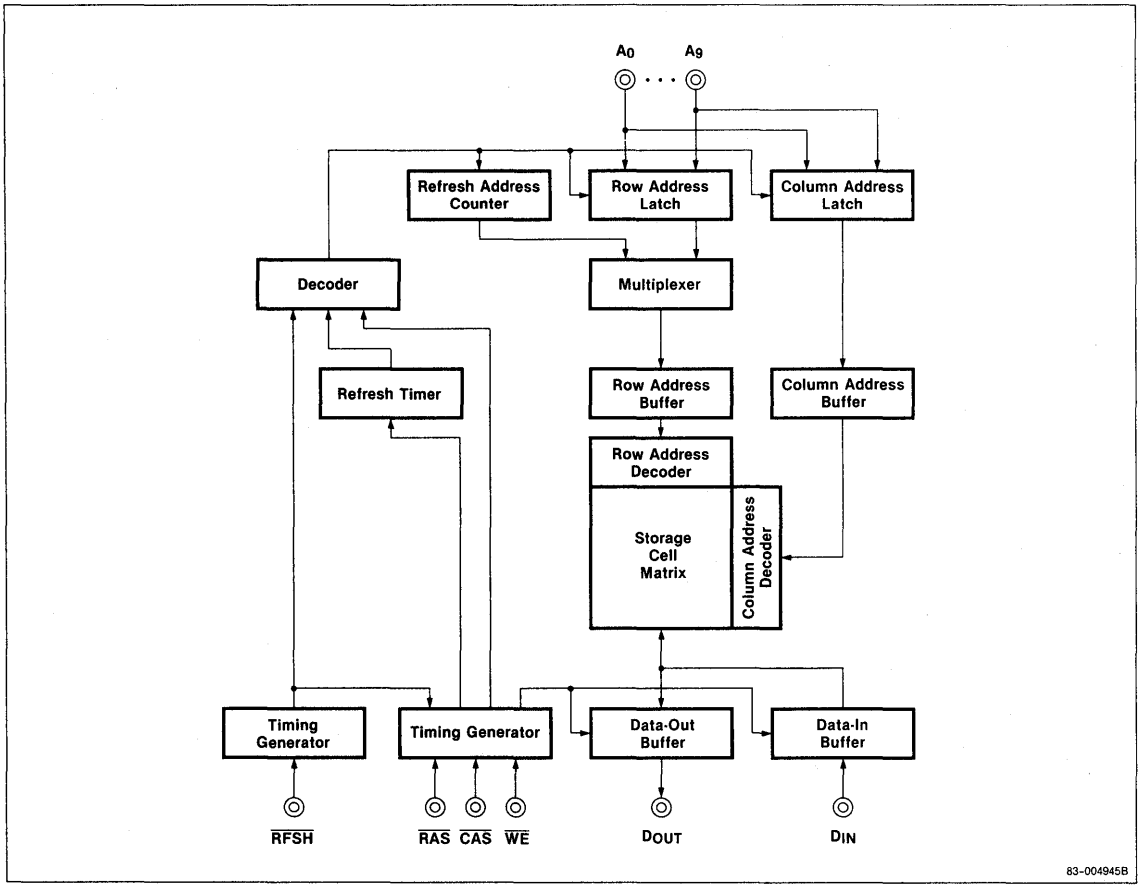
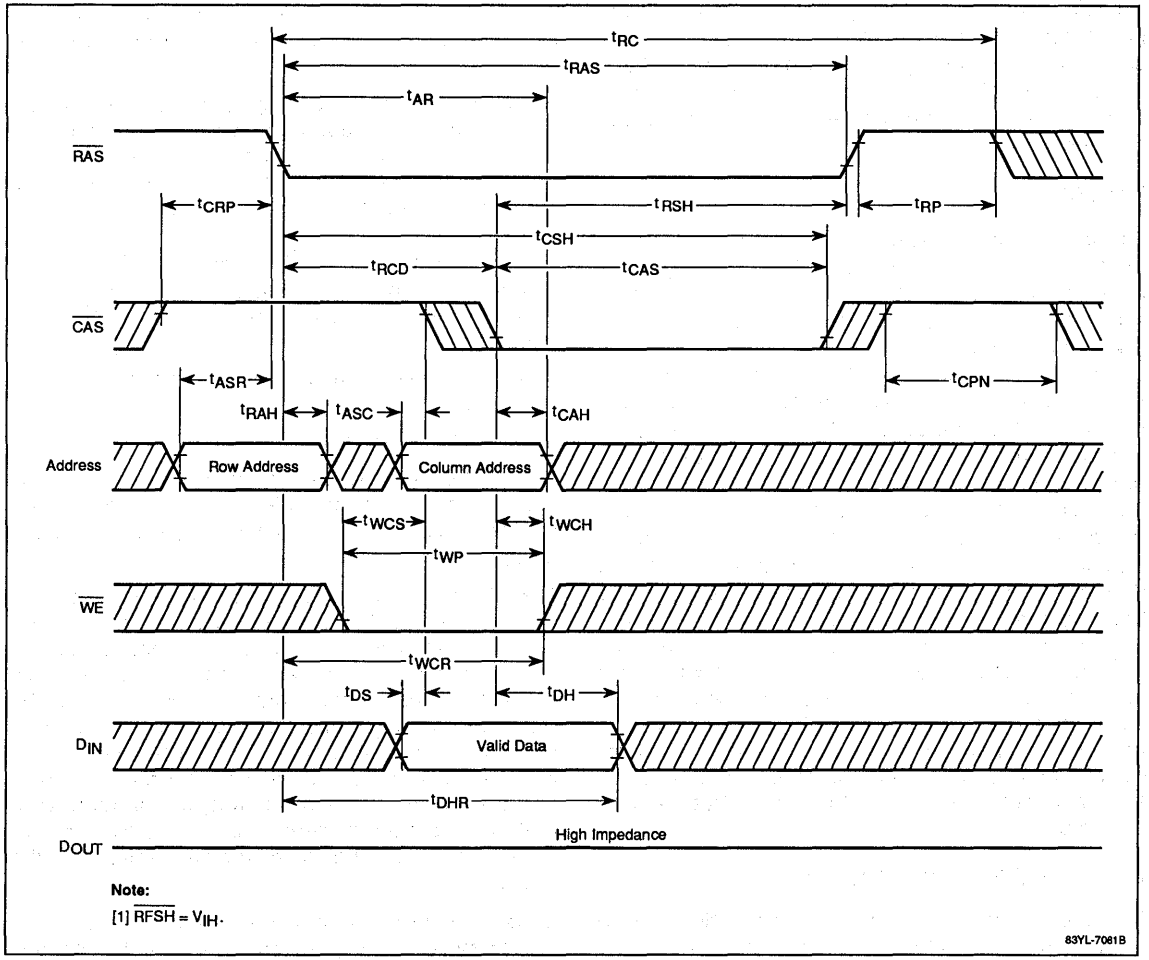


Figure 8. Early Write Cycle



Refreshing of Dynamic Cells

The silicon file, as well as all DRAMs, uses a memory cell structure that stores a dynamic charge on a capacitor, which means that the charge can decrease in time because of leakage. As a result, all devices using DRAM cell technology must be periodically restored or refreshed. Whenever a row is selected in a silicon file, all the cells in that row are accessed and the charge in that cell refreshed. The maximum interval in which a row address must be refreshed is called the refresh period (t_{REF}) and is specified as 32 ms for the silicon file. If each row address is not accessed every 32 ms, data in that row cannot be guaranteed.

Two refresh cycles can be used to refresh a silicon file. $\overline{RAS}$-only refresh cycles are executed when the refresh address is driven onto the address pins by an external circuit when $\overline{RAS}$ is low. $\overline{CAS}$ is left inactive during this cycle since no data is being read or written.

To simplify the circuitry needed to initiate refresh cycles, the silicon file has an on-chip counter that generates every refresh address and is activated by asserting $\overline{CAS}$ before the $\overline{RAS}$ signal. Internal control logic detects this state and uses the address generated by the internal refresh address counter to execute a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, which is standard in most DRAMs. Its advantage is that no external counter is required and the refresh address sequence is main-

tained when switching between $\overline{CAS}$ before $\overline{RAS}$ and self-refresh operation during operation of the silicon file. In fact, the use of $\overline{RAS}$-only refresh cycles with the silicon file is discouraged because of the difficulty in synchronizing $\overline{RAS}$-only operation (external refresh counter) with self-refresh operation (internal refresh counter).

Page Mode

The silicon file provides a page mode to increase effective bandwidth of the memory hierarchy. Page mode takes advantage of the matrix organization of the silicon file by continuously accessing data in a single row in the memory array. The silicon file is organized with 512 columns per each of the 512 rows, allowing a page cycle to access a maximum of 512 bits of information. The first word is accessed in the same manner as in a standard read and write operation, with row addresses latched onto the chip by $\overline{RAS}$ and column addresses latched by $\overline{CAS}$. Subsequent column addresses are accessed for each $\overline{CAS}$ cycle, repeated for a period equal to the maximum specification for the $\overline{RAS}$ pulse width. System performance is enhanced because the 100 ns page cycle access time (t_{PC}) is much faster than the 600 ns standard access time from $\overline{RAS}$. In solid-state disk applications, a 512-byte sector can use a page cycle to reduce read or write access times for the sector. However, the logic required to implement a page cycle is more complex than for conventional read or write operation, requiring extra system control logic or a controller chip that supports page mode.

Control and Interface Circuit Design

A silicon file requires a number of functions to be performed to execute a read or write operation. A control circuit must determine that a valid silicon file cycle is being executed and translate the read and write control signals from the host CPU into $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ signals compatible with silicon file timing. The address must be latched and multiplexed into the row and column address, conforming to the timing specifications. Finally, the silicon file must be refreshed periodically to guarantee data retention.

The first task requires the control circuit to monitor the system interface and determine if a valid silicon file cycle is being executed by the host. When a valid access cycle is active, the control circuit must interface with the host through asynchronous or asynchronous acknowledgement signals that determine when silicon file data will be valid on the system bus. The control circuit must also generate control and timing signals to the silicon file memory array that executes a read or write cycle. Once the cycle is complete, the control circuit releases the system interface for the next operation.

A control circuit can be implemented with discrete logic or integrated controller circuits that include a number of on-chip interface functions. The discrete design requires a PAL-based, status machine control circuit to perform the following functions:

- Determine valid silicon file access cycles
- Input and translate the system interface control signals into silicon file control signals, i.e., $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
- Acknowledge to the host when valid data is available
- Execute refresh cycles

The controller must also determine when a refresh cycle is required and provide the circuitry for controlling the silicon file data and address path control and timing circuits.

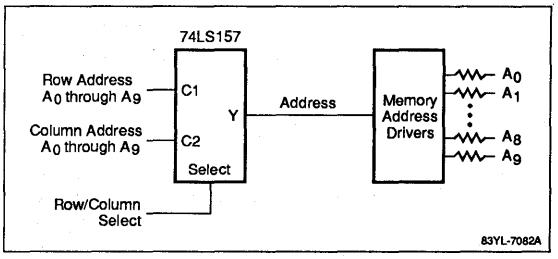
The PAL-based controller must provide internal synchronous feedback of system access information and synchronize timing of the silicon file access cycle with timing of the host's access cycle. The valid signal indicates to the control circuit that an access to the silicon file is being requested by the host. The control circuit must determine if the system access is a read or write cycle, determine whether a refresh cycle is also being requested at the same time, signal the host to wait for valid data, generate the $\overline{RAS}$ enable signal to initiate the control and addressing timing circuits of the silicon file.

Once the control circuit has determined that a valid access cycle is being executed and arbitrated any refresh and access cycle conflicts, it must generate the $\overline{RAS}$ enable signal to initiate the control and address timing circuit. This circuit generates the $\overline{RAS}$ and $\overline{CAS}$ signals and controls the address multiplexer that multiplexes the row and column addresses. Since most silicon file devices are organized into banks of data, the control circuit must also determine what bank is being accessed. The bank decoder circuit decodes the appropriate address bits and selects the $\overline{RAS}$ signal for the selected bank allowing the read or write cycle to start.

The address multiplexer, a two-input device controlled by the select signal *(mux_select)* generated by the control circuit, selects either the lower or upper address bits to generate the row and column address (figure 9). In applications using $\overline{RAS}$-only refresh cy-

cles, the refresh address must also be multiplexed onto the address lines during a refresh cycle. This can be done with an additional multiplexer or by using three-state drivers to drive the address onto one of the multiplexer inputs. Since the silicon file uses the internal $\overline{CAS}$ before $\overline{RAS}$ address counter for self-refresh operation, it is recommended that the $\overline{CAS}$ before $\overline{RAS}$ refresh method be used to eliminate the need for synchronization of the external $\overline{RAS}$-only refresh with the internal self-refresh address. An additional signal from the PAL-based control circuit is required to enable the $\overline{CAS}$ signal before the $\overline{RAS}$ signal.

Figure 9. Address Multiplexer and Driver Circuits



μPD42601 read or write cycles follow this sequence:

- The address multiplexer is selected for the row address bits and the row address is driven onto the address pins for a specified setup time.
- The control circuit generates $\overline{RAS}$, and the bank select decoder selects the $\overline{RAS}$ signal corresponding to the selected bank.
- The row address is maintained for a specified hold time.
- The multiplexer is switched to select a column address.
- The column address is maintained for a specified setup time and for the minimum specification for a $\overline{RAS}$ to $\overline{CAS}$ delay.
- The $\overline{CAS}$ signal is asserted.

The timing for this cycle must be precise to be able to maintain the address setup and hold times and $\overline{RAS}$ to $\overline{CAS}$ delay specifications. This timing is usually implemented in DRAM applications with a delay line of ±1 or 2 ns (figure 10), but since the silicon file's specification are not as critical as a DRAM's, the timing can be derived from a high-speed clock using synchronous flip-flop circuits (although consideration for timing skews between different devices should be considered and minimized by using flip-flops circuits from the same package). A gate array controller could also easily generate the address timing signals for a silicon file application.

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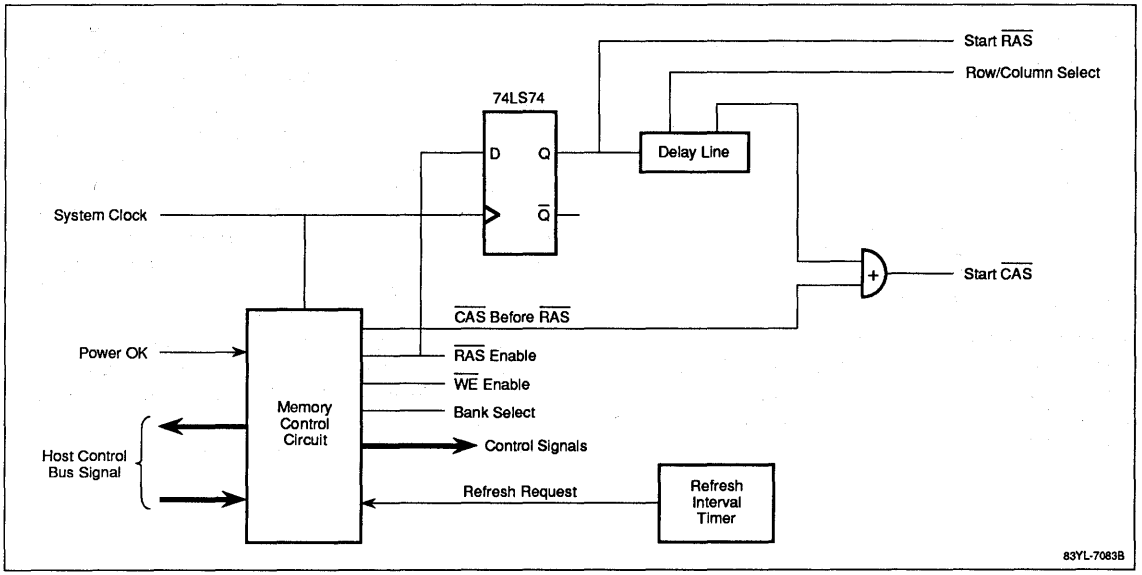
Figure 10. Memory Control Circuit and $\overline{RAS}$/$\overline{CAS}$ Timing Circuit



Since the silicon file cannot be read or written while a refresh cycle is executing, the host cannot always have access to memory. The simplest way to override this is to halt the host every 32 ms and execute a burst of 512 refresh cycles, also known as *burst refreshing*. It must be pointed out that burst refresh cycles can degrade the performance of the system. The percentage of time that the microprocessor is halted for refreshing isn't large, but the length of the burst refresh period increases the system's latency time in responding to an asynchronous event.

Another approach is called *distributed refreshing*, in which a single refresh cycle is executed every 62.5 μs. In this method, if a refresh cycle and an access cycle are active at the same time, the silicon file control circuit must arbitrate control between the two cycles, i.e., the control circuit must delay the host until the refresh cycle is completed by causing the host to execute a wait state. The refresh cycle must take precedent over the active access cycle to ensure that the maximum refresh period is not exceeded. Both refresh methods require a refresh interval counter to signal the control circuit when a refresh cycle is to be executed. This circuit consists of synchronous counters, clocked by the system clock and reset after each refresh cycle.

Data Input

Data to be written into a selected cell is latched by an on-chip register with the combination of the $\overline{WE}$ and $\overline{CAS}$ signals while $\overline{RAS}$ is active. There are two types of write cycles, both of which depend on when the write data is available. If write data is valid before $\overline{CAS}$ goes low, an early write cycle can be executed. In an early write cycle, $\overline{WE}$ signal is asserted before $\overline{CAS}$, and setup and hold times for the write pulse and the data are referenced to the falling edge of $\overline{CAS}$. The other type is called a late write, and is executed when $\overline{WE}$ and $\overline{CAS}$ are both low. Since $\overline{CAS}$ controls the output drivers, the output buffer is briefly enabled from the time $\overline{CAS}$ is active until the assertion of the $\overline{WE}$ signal. In a late write cycle, setup and hold times are referenced from the falling edge of $\overline{WE}$.

The timing specification for the host's write data will determine which write cycle is to be implemented in each design. If data is valid before the assertion of $\overline{CAS}$, the control circuit must assert a write pulse before $\overline{CAS}$ while maintaining the specified t_{WCS} write command setup, t_{WCH} hold, and t_{WP} pulse width times. Since the $\overline{WE}$ signal is connected in parallel to all of the silicon file chips, propagation delays caused by capacitive loading should also be taken into account.

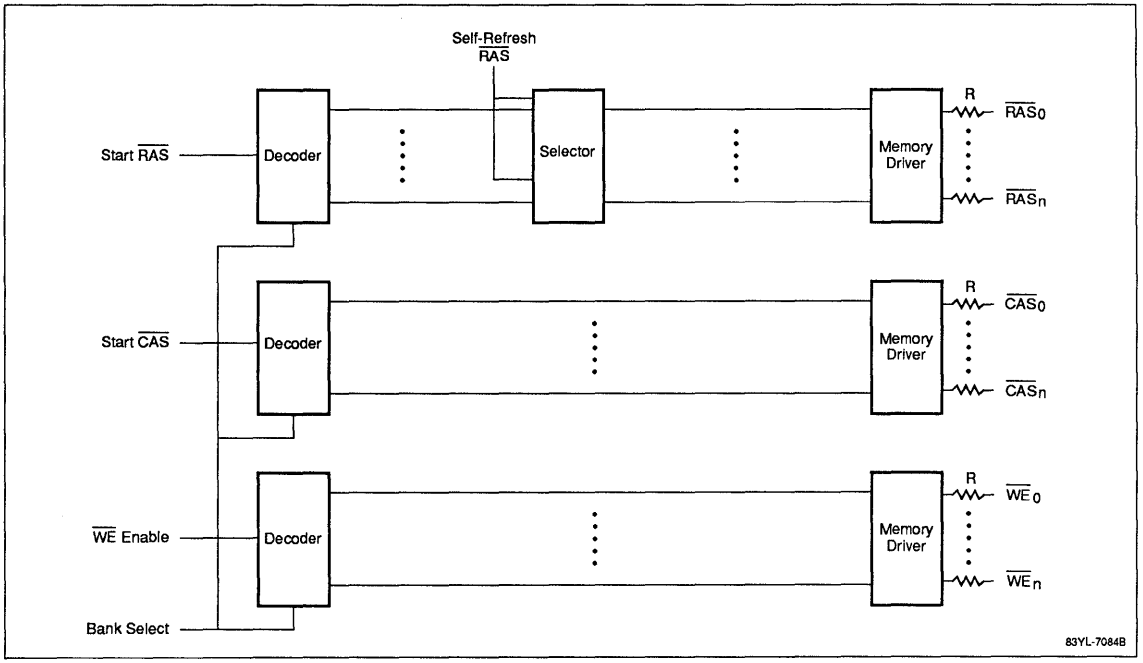
The circuit may also require write data to be latched in a transparent latch if the host isn't capable of maintaining write data long enough to meet the setup and hold times, or if a refresh arbitration cycle has to remain active during a number of wait cycles. A write data latch is controlled by a data strobe from the host that is connected to the latch enable input of the latch. The strobe should be high while write data is valid. The host system bus and the falling edge of the data strobe latch the write data at the end of the host's data cycle. The need for a write data latch is dependent upon the host's requirement for write data timing and should be considered when designing a silicon file circuit.

Memory Design Considerations

The silicon file memory array is organized into banks of chips, and the size of each bank is determined by the size of the system bus, as well as by the additional chips required for parity or error detection and correction (ERCC). For example, a 20 MByte solid-state disk with ERCC will have 5 banks of silicon file chips, each bank consisting of 32 devices to store the memory word and 7 devices to store the ERCC syndrome bits. The bank organization allows active system power to be minimized because only a part of the total array is accessed during each cycle.

The bank organization requires that the address and control lines be wired in parallel, which presents a large capacitive load to the driver circuits. The compact design presents inductive and capacitive loads to the address and control line drivers, which can cause ringing and large under- and overshoots during signal transitions, subsequent violation of address setup and hold times, or glitching on the control lines that will result in memory failures. The undershoot and ringing can be minimized with proper printed circuit board design techniques that reduce not only the length of the etch run between the driver and input pin but also the impedance of the signal etch. This is accomplished by means of damping resistors between the address and control line drivers and the silicon file inputs (figure 11). The value of these damping resistors is typically 15 to 33 ohms and should be empirically chosen.

Figure 11. Bank Decoding and Memory Driver Circuits



Because of the large input capacitance of the memory array, the transitions of address and control signals are slowed by the need to charge and discharge this capacitance. Drivers designed for use with memory arrays can drive large capacitive loads, but the designer must account for the added propagation delay due to the loading effects. If driver circuits are required to drive the address and control lines of each memory bank, the bank must divided into separate groups, and the total capacitance load must not exceed the driver's capabilities. For this purpose, some manufacturers produce memory drivers, but an integrated memory controller will provide such drivers internally.

A typical memory driver can drive a 250 pF capacitive load with the silicon file address and control line inputs specified at 5 pF for address lines and 8 pF for control lines. For a bank of 39 chips, one driver is required to drive each address line (A_0 through A_9) and two drivers to drive each control line ($\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$). This requires 16 drivers for all address and control lines. Because the driver circuits are quad packages, an additional four packages are required to drive each bank.

Power Distribution and Decoupling

As in all high-speed memory designs, controlling large current transients and protecting high frequency components from fast switching speeds is an important consideration. In order to control these current transients and prevent them from generating voltage spikes that can cause loss of data and *soft errors*, every effort must be made to minimize impedance in the decoupling path of the device.

The decoupling path is the trace distance from a power pin through a decoupling capacitor and to package ground. The impedance of this path is determined by the line inductance and series impedance of the decoupling capacitor. The line inductance can be minimized either by providing a power plane or by girding the power. To increase the effectiveness of the girded power, decoupling capacitors should be placed between the power and ground pins of every chip. The decoupling capacitors used for a typical silicon file design would be a high frequency (100 MHz) 0.2 μF ceramic capacitor. Since most memory designs have some low frequency DC currents, large bulk electrolyte 27 μF capacitors should be located judiciously around the periphery of the printed circuit board.

Application Note 90-02
High-Performance Memory Systems

Introduction

Today's RISC microprocessor architectures offer a promise of high performance systems able to execute an instruction in one system clock cycle, which means the challenge for a system designer is to design a memory system that can support high CPU throughput requirements. Common elements of these VLSI designs include on-chip subsystems such as floating point units and/or cache memory.

Although the size of an on-chip cache is typically small (4 to 8 Kb) to minimize chip size and optimize cost, the system may also require an external, second-level cache that is much larger (256 Kb to 1 Mb) and can interface to a high performance system bus. If the CPU executes an instruction that isn't stored in the cache, the cache must access main memory and fetch an instruction for the processor. Even though a cache is designed to sustain a high hit rate, a percentage of the CPU's read cycles and all writes cycles must access main memory, making it essential that data transfer cycles be executed so that latency of the system bus is minimized. System bus latency may increase dramatically in a multiprocessor system and can be the critical issue in determining system performance.

This application note will discuss quantitative measures of memory performance, as well as a number of design techniques for optimizing performance in today's system environment.

Hierarchical Systems

Bottlenecks in most Von Neumann architectures have traditionally occurred because a processor could only read a single word from memory during each access cycle, and to be able to match processor cycle time, a system would have to use very high-speed devices that in most cases could not be justified in terms of cost. The classical solution has been to configure a hierarchical or multilevel structure containing several types of memory devices with various cost and performance characteristics.

Performance can be affected by such interrelated factors as program behavior with respect to memory references, access times and sizes of each level, granularity of information transfer, memory management policies, and the processor-to-memory interconnection network. One measure of performance is called *effective access time*, which is the sum of average access times at each level of the hierarchy. Another quantitative measure is *bandwidth*, which refers to the number of bits that can be accessed per second. To increase bandwidth, a system designer may choose to reduce cycle time, increase word size by accessing more bits per cycle, or replicate the memory banks and access two or more concurrently.

Properties of Program Locality

The majority of computer systems developed today are based on properties of program locality that reveal a strong tendency for accesses to be clustered in small regions of memory during any short period of time. Program locality has two aspects, temporal and spatial. The first, locality of time, means that information that will be in use in the near future is likely to be in use already. This type of behavior can be expected from program loops in which both the data and instructions are reused. The second property, locality of space, means that portions of the address space which are in use generally consist of a fairly small number of individual contiguous segments of that address space. Locality of space means that the program's loci of reference in the near future are likely to be near the current loci of reference. This theory is based on common patterns of behavior: related data items (e.g., variable arrays) are usually stored together and instructions are mostly executed sequentially.

The characteristics of temporal locality have shown a strong tendency for program references to be grouped in time, and in fact were responsible for the invention of virtual memory and the subsequent design of high-speed caches, both of which exploit the properties of locality by storing a copy of the program in a temporary segment of memory. Virtual memory increases the size of the system by segmenting the program into pages that are individually loaded from magnetic secondary memory into main memory. A cache optimizes CPU throughput by also storing a segment of the program in a buffer that matches the speed of the processor.

Optimizing the Hierarchy

Once program behavior is understood, main memory can be structured to optimize processor performance. As discussed earlier, effective access time is the sum of the average access time in each of the levels of the hierarchy, defined as

$$t_{EFF} = \Sigma\, t_K$$

where t_{EFF} is effective access time from the processor to the *ith* level of the hierarchy, and t_K is the individual average access time at each level, where $K = 1$ *to* i. Generally, t_K includes not only the wait time caused by memory conflicts at level K, but also the delay in the switching network between levels $K - 1$ and K. The degree of conflicts is usually a function of the number of processors, the number of memory modules, and the interconnection network between the processors and modules.

In modeling the performance of a hierarchy, it is often assumed that the probability of finding requested information in the memory of a given level is characterized by a success function or hit ratio h. In general, h depends on the granularity of information transfer, the capacity of memory at that level, the management strategy, and other factors. However, for some class of management policies, it has been found that h is most sensitive to memory size. Because copies of information at the highest hierarchical level are assumed to exist in levels below that level, the probability of finding the data at the higher levels is $f = 1 - h$, where f is the miss ratio. Therefore in a two-level system, effective access time would be equal to

$$t_{EFF} = h\,t_{K1} + (1 - h)\,t_{K2}$$

where $t_{K1} = t_{ACC}$ at level 1 and $t_{K2} = t_{ACC}$ at level 2. If the hierarchy consists of one level of infinite size (an expensive option for most applications), the probability of accessing this data at level one is 100% (hit ratio = 1). Memory size greatly impacts the probability of finding data at a given level, which is why the probabilities at each level are expressed in terms of hit and miss ratios. For example, effective access time for a two-level hierarchy would be expressed as follows:

$$t_{EFF} = h\,t_{K1} + (1 - h)\,t_{K2}$$

If the hit ratio at level one is 0.99, then the probability of finding the data at level two, or the miss ratio at level two, would be $1 - 0.99 = 0.01$. Effective access time then would be

$$t_{EFF} = (0.99)\,t_{K1} + (0.01)\,t_{K2}$$

Hit ratio is crucial to system performance. For example, if the memory at level two is ten times slower than the memory at level one, the hit ratio decreases from 0.99 to 0.98 (roughly 1% fewer hits) and results in an increase in t_{EFF} of roughly 10%. Small changes in hit ratio affect effective cycle time of the overall system, making t_{EFF} very sensitive to hit ratio. A decrease of 10% in hit ratio (from 0.99 to 0.89) almost doubles the effective cycle time and divides net performance in half when the cycle time ratio is 10. If the cycle time ratio is 20, that same 10% decrease increases effective cycle time by almost a factor of 4. Hit ratio should be as high as possible; in many cases, techniques resulting in marginal 1% to 2% improvements may yield substantial performance improvements.

A very large structure in only one level is too expensive for most systems, and a multilevel structure is the only configuration that makes sense in terms of cost and performance objectives. Therefore, the goal is to structure the hierarchy so that the highest performance is available for the least cost. Because hit ratio is a function of the memory size at each level, the implication is that the larger the memory at a given level, the higher the hit rate at that level.

Optimizing the Cache

The other variable in the t_{EFF} equation is average access time (t_K) at each level. The hierarchical level closest to the processor should have access times equal to the processor's cycle time, as well as capacity large enough to maintain a high hit rate. The classical solution has been to design this level as a cache, which is a high-speed buffer typically located between the processor and main memory that provides data to the processor without any wait intervals. Success of the cache is attributed to the properties of program locality and is measured by cache hit ratio, as well as by placement algorithm (degree of associativity), block size, ability to perform during a miss, write cycles, and data consistency in multiprocessor or multicache systems.

A cache operation starts when the processor executes a read cycle and outputs a physical address to the memory system. The physical address is separated into two fields, the address tag field and the set select field. The cache latches the address, and the set field in the physical address selects a set in the cache directory or address tag memory. The address tag from the cache directory is compared to the physical address tag from the CPU. If they're the same, a hit occurs and the data is read from the selected block. If the address tags are not the same, a miss occurs and the data has to be fetched from main memory, which means the CPU must wait until the data is read. New data with a new address tag is stored in the cache.

Cache performance is determined by hit ratio, a function of the design that includes the size of the cache, the degree of associativity used to search the cache directory (placement algorithm), the size of its data block, and the replacement algorithm used in a miss cycle.

Although a larger cache can be effective in sustaining a high hit rate, its benefits are diminished by higher costs.

The same relationship regarding effective access for a two-level hierarchy is valid for a two-level system with a cache in the first level. The cache's hit rate can be optimized not only by increasing the size of the cache, but also by optimizing its placement algorithm, block size, and replacement algorithm. With an optimized architecture, the hit rate should be above 90%.

Effective access time in a two-level hierarchy, with the cache in the first level and main memory in the second level, is calculated as the sum of the hit rate and cache access time in the first level and the miss rate multiplied by the access time of main memory in the second level. For a cache with a read cycle time of 60 ns and a hit ratio of 95%, and a main memory read cycle time of 250 ns and a miss rate of 5%, effective access would be determined as followed:

$t_{EFF} = (h_{CACHE})\ (t_{CACHE}) + (1 - h_{CACHE})\ (t_{MAIN\ MEMORY})$

$t_{EFF} = (0.95)\ (60) + (0.05)\ (250) = 59 + 12.5 = 71.5$ ns

Effective access time must also include the effect of a write cycle on system performance. To determine this effect, the ratio of read and write cycles must be determined by analyzing the program address characteristics. The ratio between read and write cycles is typically 85% to 15% in general-purpose computer environments, but it may change to 50%-50% in scientific and other computation-based environments. The equation would have to be expanded as follows:

$t_{EFF} = R\ [(h_{CACHE})\ (t_{CACHE}) + (1 - h_{CACHE})\ (t_{MAIN\ MEMORY})] + W\ (t_{WCYC})$

where R is the fraction of cycles that are read cycles, W is the fraction of cycles that are write cycles, and t_{WCYC} equals write cycle time. If R = 0.85, W = 0.15, and t_{WCYC} = 250 ns, total effective access time would be equal to

$t_{EFF} = 0.85\ [(0.95)\ (60) + (0.05)\ (250)] + 0.15\ (250) =$ 96.57 ns

The span of a write cycle does not reflect hit rate. A larger percentage of write cycles will increase t_{EFF}. For example, if R and W were equal at 50%, then t_{EFF} would increase as follows:

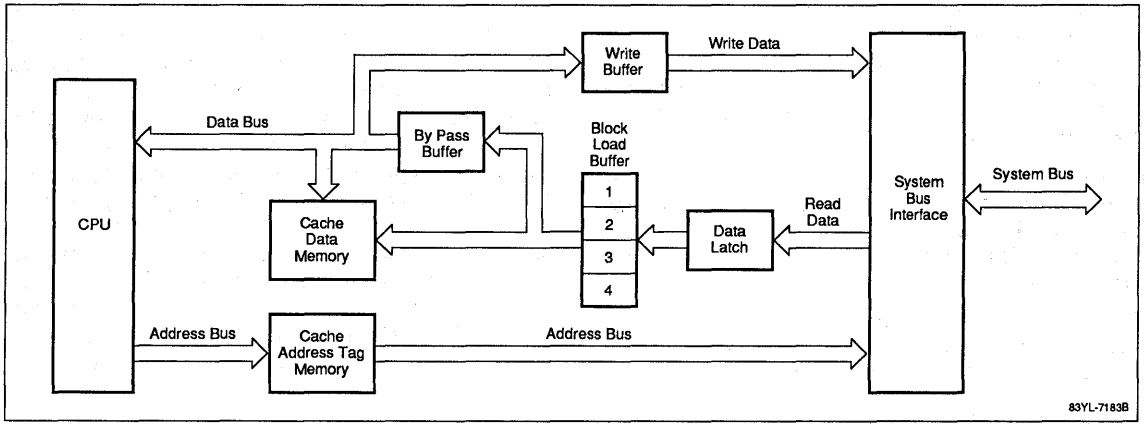
$t_{EFF} = 0.50\ [(0.95)\ (60) + (0.05)\ (250)] + 0.50\ (250) =$ 159.75 ns

Most program workloads generally have a higher ratio of read cycles to write cycles, allowing the cache to optimize read operation as well as system performance. The main concern with write cycles is that the CPU has to wait for the entire transfer cycle between cache and main memory (> 250 ns) before proceeding to the next instruction. If the cache were able to buffer write data, write cycle time could be reduced to the write access time and the processor wouldn't have to wait for access into main memory and could proceed to the next instruction. Meanwhile the cache could concurrently execute a write cycle into main memory (figure 1). In this case, t_{WCYC} would equal the 60 ns access time of the cache and not the 250 ns access time of main memory. The equation for t_{EFF} in a buffered write cycle is calculated as follows:

$t_{EFF} = 0.85\ [(0.95)\ (60)] + 0.15\ (60) = 57.45$ ns

28h

Figure 1. Write, Fetch Bypass, and Wraparound Load Buffers



The disadvantage of a buffered write cycle is that the circuitry required to control the concurrent CPU and main memory write cycles would have to be more complex.

Optimizing the Miss Cycle

The block size of a cache is the parameter, together with the overall size of the cache itself, that most strongly affects cache performance and also overall system performance. When the data the processor is addressing is not in the cache, the cache executes a miss cycle to access main memory and fetch the missed data to the cache and the CPU. Enlarging block size can decrease the miss ratio and thereby increase the storage delay component of an average instruction, but the longer transfer time required may cause problems in multiprocessor systems because of higher levels of traffic.

A number of design tradeoffs influence block size. For example, architecture of the bus between a cache and main memory plays an important role. A bus protocol that requires an address with each data transfer may force the block size to be one word, because multiple word transfers would be very inefficient. Conversely, if one address can fetch several words of data, then a larger block size would be advantageous. Devices with the ability to transfer bursts of data are becoming popular in a number of microprocessor systems and, together with nibble mode DRAMs, can be implemented to increase memory bus bandwidth. Increasing the width of the bus is another technique that can increase system bandwidth.

In large mainframe systems, block size can reflect the wider bus size and also take advantage of the degree of memory interleaving. Interleaving increases memory bandwidth by enabling data to be accessed from a number of memory banks concurrently, eliminating the delay required while individual banks are accessed separately. In multiprocessor systems, a large block size will increase the cache miss data transfer time, increasing the system bus I/O latency and decreasing the system bus bandwidth.

A larger block size generally increases cache performance, but doesn't necessarily improve system performance. Cache features such as burst data transfers, prefetching, fetch bypass and wraparound load cycles can be added as necessary.

During a miss cycle, the cache accesses main memory and reads the missed block. If the missed word is loaded directly into the cache before the CPU can fetch the data, access time of the miss cycle will equal the sum of the access time from main memory and the delay required for the missed word to be written and read from the cache. The fetch bypass and wraparound load functions minimize this time by initially bypassing the cache and allowing the CPU to directly fetch the missed word from the fetch bypass buffer, which is loaded with the missed word as soon as it is fetched from main memory (figure 1). The CPU can fetch and execute the missed word from the fetch bypass buffer and then proceed to the next address without having to wait for the cache to be updated. The missed data block is concurrently loaded into the wraparound load buffer; after the entire block is fetched from main memory, the cache is updated. If the CPU attempts to fetch the next word in the block before the block is loaded into memory, the CPU may be required to wait for the memory to be updated or, if an additional function exists in the block load buffer, to directly access the next word from the block load buffer.

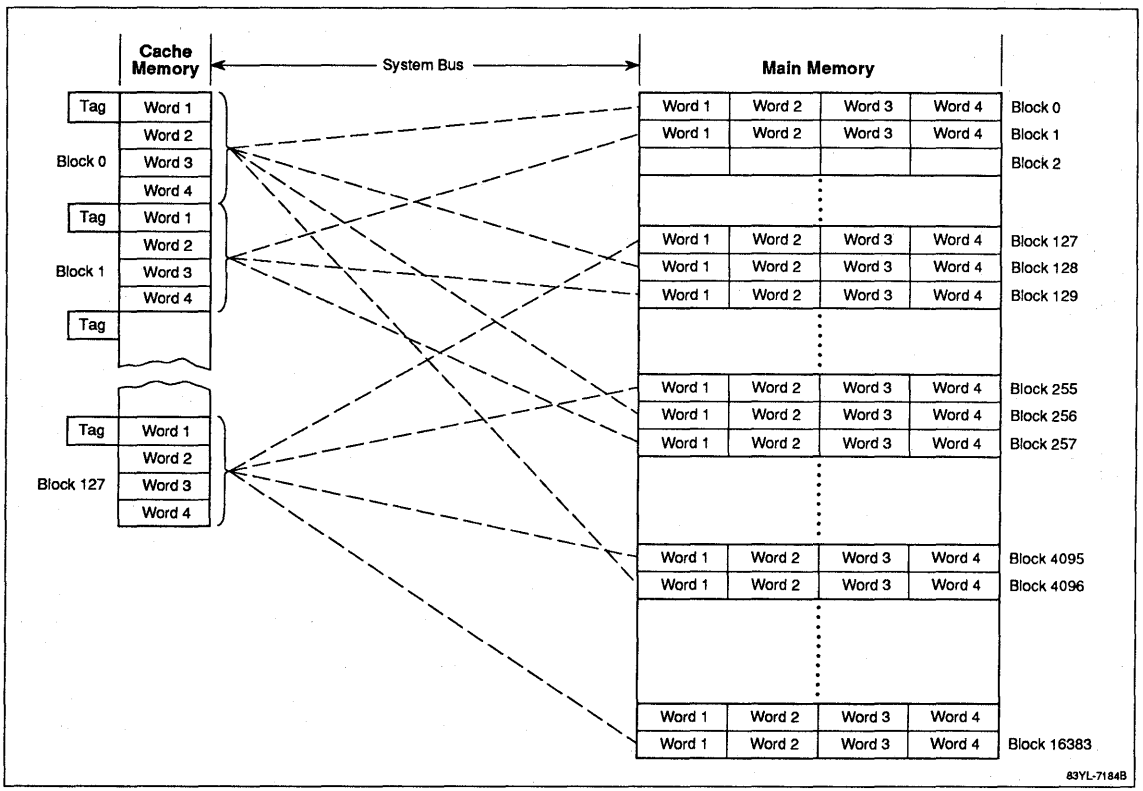
The effective access time of the miss cycle can be minimized by reducing the amount of data required to execute a cache miss cycle. This can be accomplished by employing a data transfer mode, called *burst data transfer*, that requires a single address for each 16 bytes of data rather than separate addresses for each 4 bytes of data. Burst data transfers are implemented in high performance microprocessors such as Intel's 80486, Motorola's 68040, and NEC's V80™. Burst mode allows a 16-byte cache block to be transferred during a cache miss, minimizing the cache miss data transfer time and increasing system bus bandwidth.

Optimizing the Transfer Cycle

As discussed above, during a miss cycle, the missed data is fetched from main memory. The cache block is the data element used to transfer the data between main memory and the cache. The size of the cache data block can be one word, but typically it is more than one word (figure 2). It has been determined that the cache hit rate increases as a function of cache block size and is generally dependent on the properties of program locality, which are enhanced by fetching a large number of consecutive instructions. However, a very large block size increases the time required to transfer the data over the system bus, decreasing the system bus bandwidth and increasing bus latency. Therefore, the choice of block size is a tradeoff between maintaining the cache hit rate and maximizing the system bus bandwidth.

V80 is a trademark of NEC Corporation

Figure 2. Block Transfers for a Direct Mapped Cache



Burst Mode. A 16-byte block size has been implemented in a number of RISC/CISC architectures. This block size is a good compromise between maintaining a high hit rate and minimizing the bus latency during a cache miss cycle. This 16-byte block transfer is called burst mode data transfer and it requires only one address for each 16-byte data transfer. By allowing four consecutive words to be accessed with one address, this feature decreases data transfer time and maximizes system bandwidth.

Although its primary advantage is being able to minimize bus latency and sustain a high hit rate, burst mode would be useless if it could not easily be supported by the interface circuit for main memory. Fortunately, burst mode is designed to be used with DRAMs offering a nibble mode, whereby four consecutive bits can be accessed in a single cycle. In a standard DRAM read cycle, each cycle requires a address that must satisfy the specifications for $\overline{RAS}$ access (t_{RAS}) and precharging (t_{RP}), calculated as follows:

TOTAL CYCLE TIME = $(t_{RAS1} + t_{RP1}) + (t_{RAS2} + t_{RP2}) + (t_{RAS3} + t_{RP3}) + (t_{RAS4} + t_{RP4})$

The separate address and precharge time represents a significant amount of overhead to complete the memory access.

Nibble mode DRAMs provide additional on-chip circuitry that minimizes total cycle time by eliminating the requirement for precharge between consecutive memory accesses. The nibble mode cycle time is given as follows:

TOTAL NIBBLE MODE CYCLE TIME = $t_{RAS1} + t_{RAS2} + t_{RAS3} + t_{RAS4} + t_{RPN}$

28h

Four consecutive data bits are accessed by a single address and loaded into an on-chip shift register that is clocked by $\overline{CAS}$. The precharge cycle is delayed until after the bits are valid to prevent the timing skew that usually occurs between each memory cycle (figure 3).

Burst mode data transfers are intended to be implemented with nibble mode DRAMs in main memory. Although nibble mode DRAMs provide the simplest interface for burst mode data transfers, other DRAM operating modes such as fast-page and static-column modes can be used. These DRAM operating modes also reduce DRAM effective access time and require additional external circuitry for implementation.

Fast-page and static-column DRAMs differ from nibble mode DRAMs in that they require a new column address and can access a total of 512 data bits in a single cycle. Most often they are required in computer graphics applications or in direct memory access (DMA) I/O cycles.

Future Enhancements. Among the features proposed for future generations of DRAMs is a feature called *gated* $\overline{RAS}$ *precharge*, which minimizes DRAM access time by eliminating one of the $\overline{RAS}$ transition times. In a standard DRAM cycle, cycle time is defined as follows:

$$t_{RC} = t_{T1} + t_{RAS} + t_{T2} + t_{RP}$$

where t_{T1} and t_{T2} are $\overline{RAS}$ transition times, t_{RAS} is $\overline{RAS}$ cycle time, and t_{RP} is $\overline{RAS}$ precharge time. Minimum cycle time cannot be achieved in a system because of a mininum and maximum skew in the logic generating the edges of the $\overline{RAS}$ signal (figure 4). The gated $\overline{RAS}$ precharge feature removes both t_{T2} and the timing skew from the minimum cycle time, as follows:

$$t_{RC} = t_{T1} + t_{RAS} + t_{RP}$$

Unlike a standard DRAM, this feature allows $\overline{RAS}$ to go inactive anytime after $\overline{CAS}$ is asserted. For a minimum cycle, $\overline{RAS}$ can go inactive prior to the minimum time for t_{RAS}, allowing internal timing to place the device into precharge.

Another proposed DRAM enhancement is *extended fast-page data output*, which would permit system-level page cycle times to approach those permitted by the specification for memory data. Currently, data output is sampled after a specified access time and after an additional lapse caused by a skew in the system logic has expired. $\overline{CAS}$ is not permitted to go inactive until after the setup and hold times of the devices are satisfied. Using an extended data output feature, data output would remain valid after $\overline{CAS}$ goes inactive if $\overline{RAS}$ is also active. Data output can then be sampled by the same signal used to turn off $\overline{CAS}$. When $\overline{CAS}$ goes inactive again, the data output changes from the previous data to that of the currently accessed location. If the previous and current data are the same, there will be no discharging or precharging of the memory bus. The outputs will be three-state when both $\overline{RAS}$ and $\overline{CAS}$ are inactive (figure 5). The elimination of the additional timing skew will improve effective cycle time and simplify the complexity of the control logic.Both of these proposed enhancements offer solutions that minimize the effective memory cycle by eliminating timing skews inherent to standard DRAM designs. Unfortunately, the precharge time remains an inherent disadvantage, because consecutive accesses to the memory module will always have a timing skew (t_{RP}).

Figure 3. Types of Data Transfer Cycles

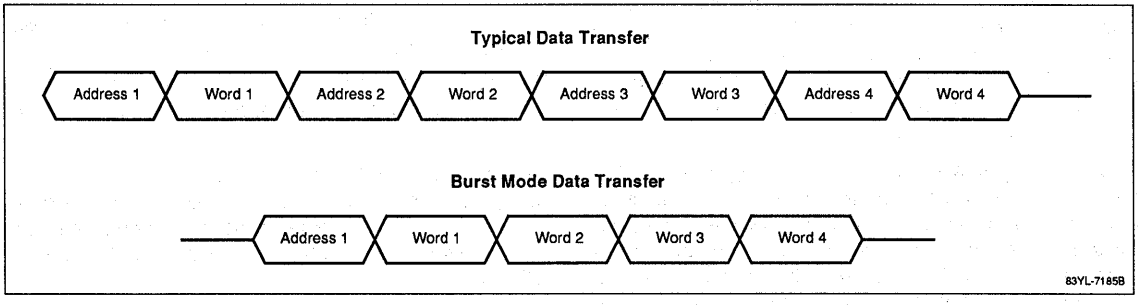
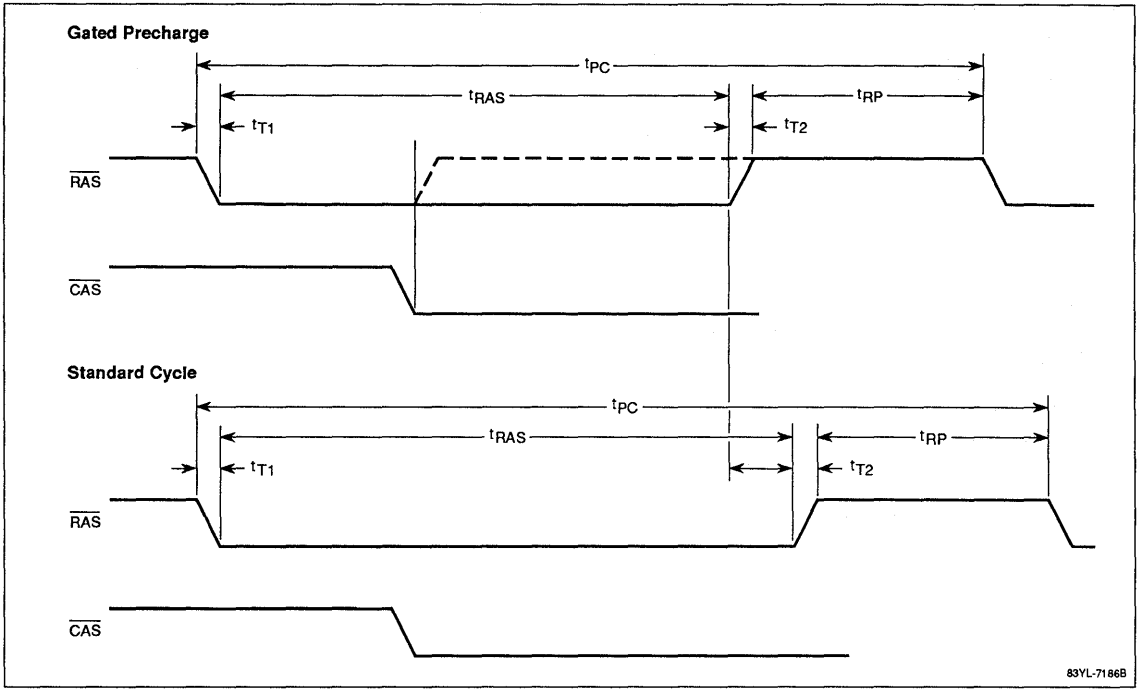


Figure 4. Gated Precharge



Interleaving

In a two-level hierarchy, memory bandwidth in the first level can be optimized by means of a cache that matches the CPU's read cycle time. For cache misses and write cycles, the cache-to-main memory bandwidth can be maximized by means of burst mode data transfers and standard DRAMs with special operating modes.

Interleaving optimizes effective access when more than one row of data needs to be accessed at the same time. Fast-page cycles are a means of reducing access time for bits located in the same row of the memory array, but they are inefficient for handling the consecutive access of data residing in different row addresses. To fetch diagonal elements in the matrix, the system needs to concurrently access row 1 and column 1, row 2 and column 2, etc. Page cycles can't be used in this scheme because a new row must be accessed for each data element.

A memory system organized to distribute the address to several banks simultaneously is said to be interleaved. The interleaving of addresses among *M* modules is called *M*-way interleaving and allows consecutive access to *M* memory banks. In high-order interleaving, the addresses are distributed so that the memory modules contain consecutive addresses. High-order bits are used to select the module while the low-order bits are used to select the address within the module. A second method, called low-order interleaving, distributes the address so that consecutive addresses are located within consecutive modules. The low-order bits of the address select the module, while the remaining bits select the address within the module.

In a low-order interleaved system, the memory is organized into banks with each bank providing data bits equal to the width of the CPU memory bus. An address is latched by the memory circuit and the low-order bits are decoded to determine the number of banks to be accessed (figure 6). If four banks are accessed, they are said to be four-way interleaved.

A memory controller circuit initially generates the control signals for the accessing of bank 1. The data for access 1 will be valid after the specified time for t_{RAS} has elapsed, after which the accessed bank will be precharged. Control signals are simultaneously being generated for bank 2, and they may be skewed by a system clock to accommodate data access for the second fetch from the CPU. Data from bank 2 becomes

valid immediately after the data from bank 1 becomes valid, and no timing skew exists for precharging in the data stream. A precharge cycle for bank 2 is executed while the access to bank 3 is initiated. Data is read from bank 3 immediately after the data from bank 2 is read. Bank 3 executes the precharge while bank 4 accesses data for the cycle immediately following the bank 3 access. Finally, bank 4 executes the precharge cycle to end the interleaving. This scheme eliminates the precharge timing skew and maximizes memory bus bandwidth, but at the cost of a more complex control circuit.

Another scheme uses low-order interleaving and applies the high-order bits of the address to all memory modules simultaneously in one access (figure 7). The single access returns *M* consecutive words of information from the *M* memory modules and accesses information from a particular module using the low-order bits. A data latch is associated with each module, the information from each module is gated into a latch in a fetch cycle, whereupon a multiplexer can be used to direct the desired data to the data bus. Figure 7 illustrates timing for a multiword read access using this method, which is ideal for accessing a vector of data elements or for prefetching sequential instructions in a pipeline processor. It can also be used to access a block of information for a pipeline processor with a cache.

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Figure 5. Extended Data Output

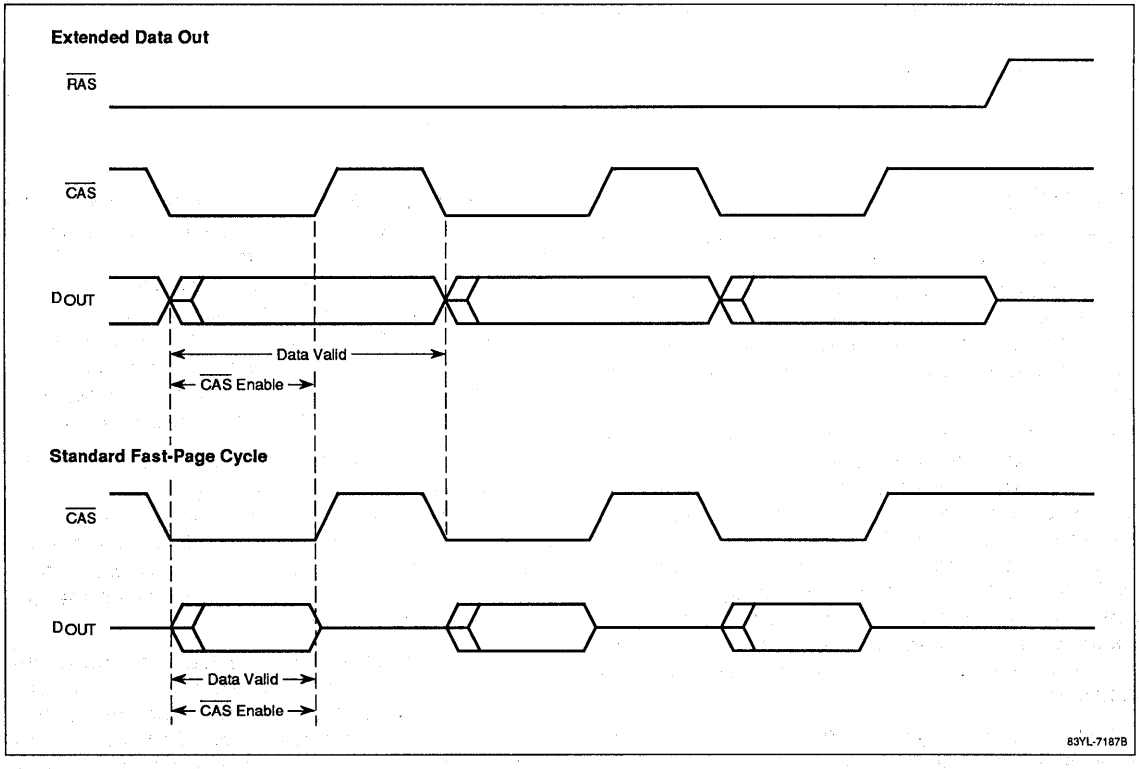


Figure 6. Low-Order Interleaving with Concurrent Access

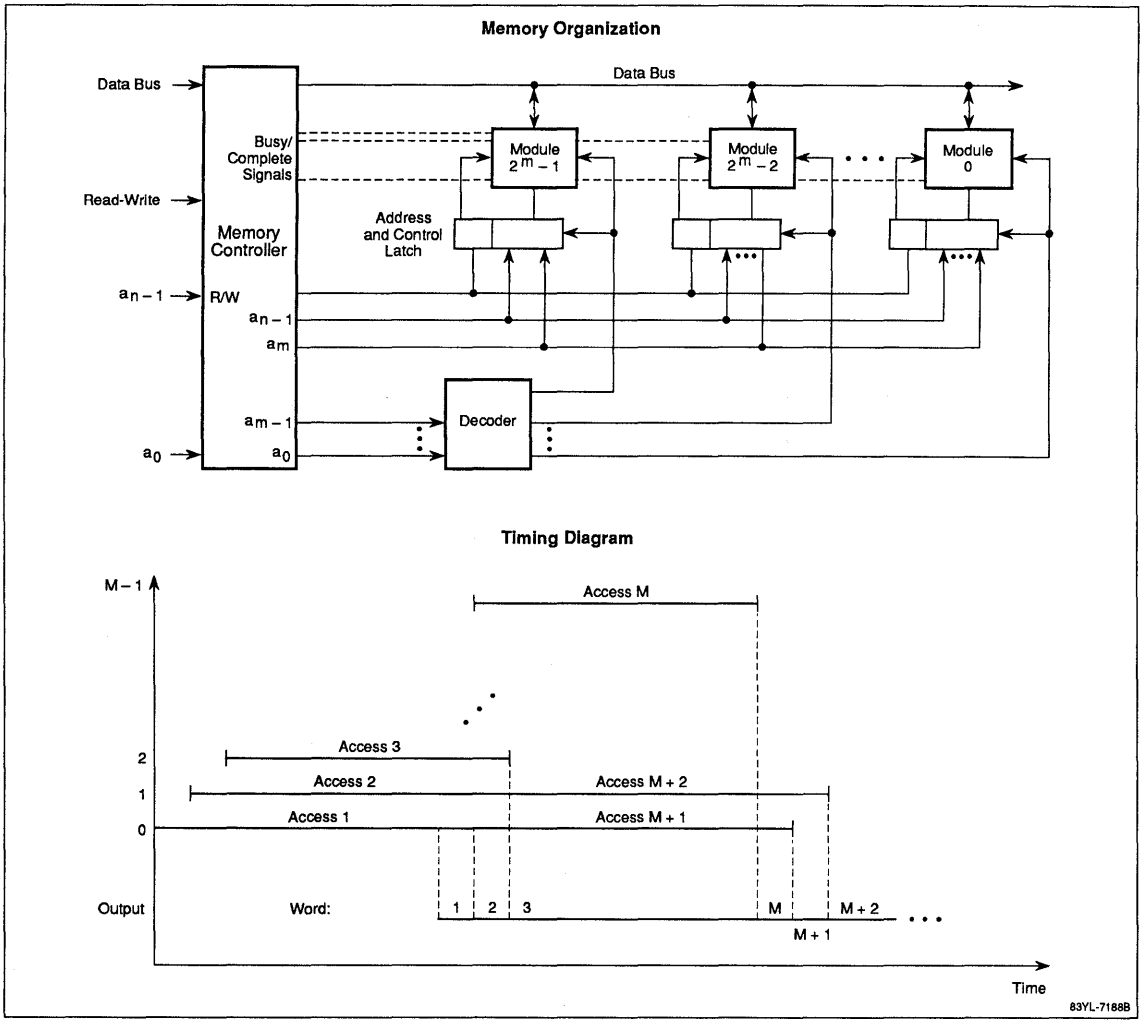
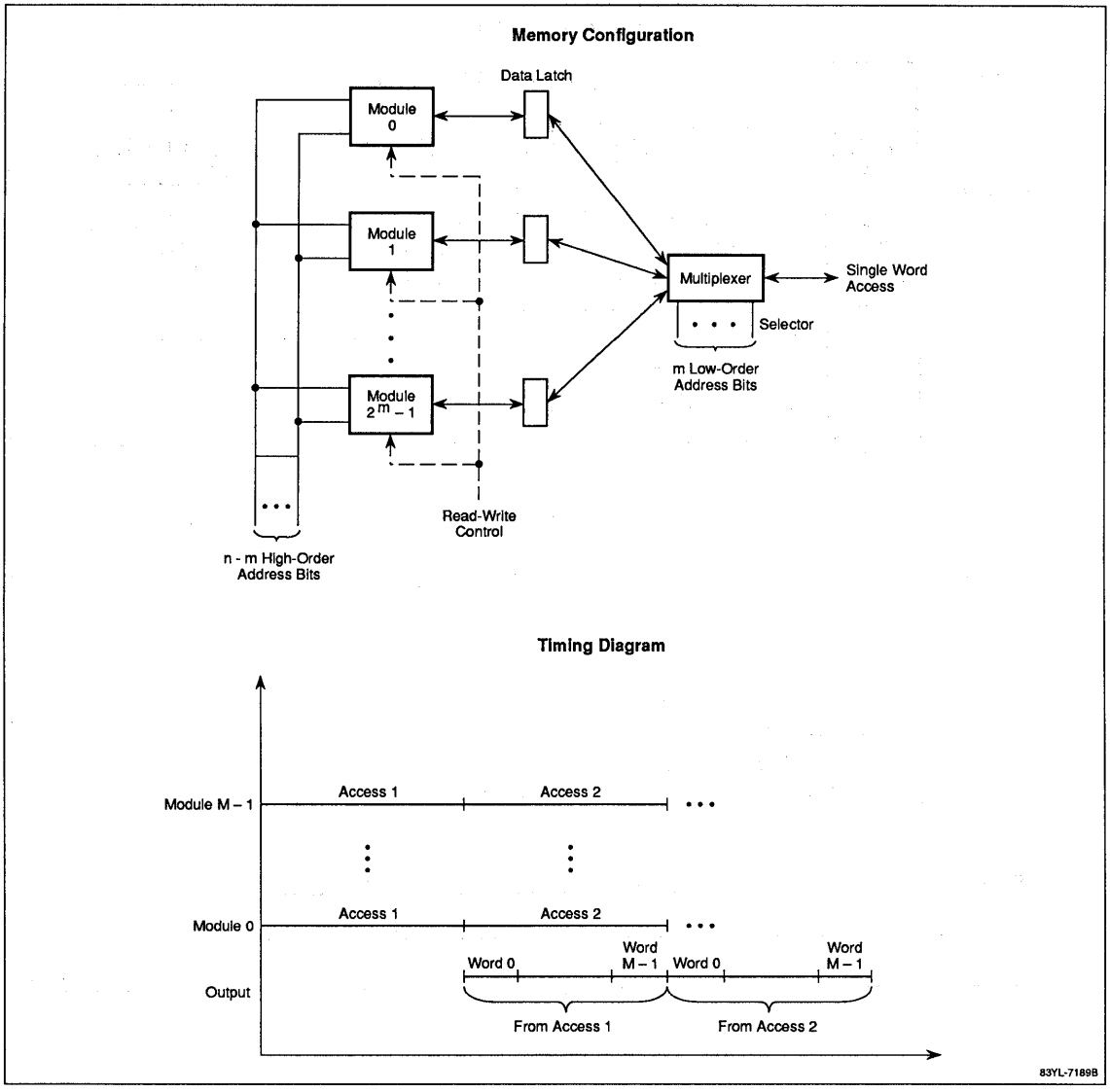


Figure 7. Low-Order Interleaving with Simultaneous Access



Introduction

The evolution of low-power, high-capacity, high-speed memory technologies has led the system designer to novel and highly portable computer designs. As technology has advanced to low-power devices, it has become possible to make an entire system nonvolatile for the life of the product.

To provide this nonvolatile function, secondary power sources are mounted on a printed circuit board controlled by a backup circuit that switches from the primary power to secondary power during power failures. The backup issue is considered as part of the overall system design, and the choice of a secondary power source and backup circuit are based on the unique characteristics of each application.

This application note deals with the issues of providing a nonvolatile memory system. A review of the evolution of static RAMs (SRAMs) with regard to state-of-the-art, low-power SRAM technology is followed by an example of secondary power sources, as well as several sample backup circuit designs.

SRAM Technology

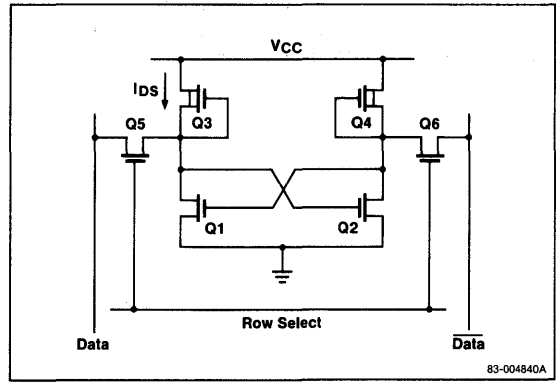
The SRAM historically has been used by system designers to provide a high-speed, low-power data storage function for a variety of computer architectures. The higher cost-per-bit compared to dynamic memories is offset by a simpler circuit design that features a nonmultiplexed address structure, simple timing signals, and no refresh requirement.

Six-Transistor Cell

The development of the SRAM memory cell has followed the trail of bipolar, NMOS, and CMOS technologies in that large-capacity memory devices require minimal cell size, not only to reduce power requirements, but also to be able to fit the die into the package.

The static memory cell is basically a cross-coupled flip-flop circuit requiring no clocks or refreshing. Early six-transistor NMOS static memory cell designs employed the use of enhancement or depletion mode FETs as load devices. Figure 1 shows an example using depletion loads. Q3 and Q4 are depletion-type devices fabricated such that they are always conductive when their respective gate and source nodes are shorted together. If the gate of enhancement device Q2 is written to a low level using Q5 and the data line, Q2 turns off. This allows load device Q4 to pull its source node high and turn on Q1; the write operation using Q6 also helps this action. The cell is designed so that Q1 has much lower "on" resistance than its load Q3. After the write operation ends, and Q5 and Q6 are off, Q1 keeps its drain node at a low level to maintain Q2 in the off state, while the drain node of Q2 is maintained high by Q4. The stored voltages are stable.

Figure 1. Six-Transistor Cell—Depletion



Four-Transistor Cell

As NMOS technology evolved, the active device for the load was replaced with polysilicon resistors (see figure 2). With the polysilicon load resistor, current levels of less than 1 nA are achievable. Because of these low-current levels, the cell can be used in advanced SRAMs with very high memory density and low standby current. NEC uses this technology in its low-power family of SRAMs to facilitate their use in battery backup applications. This type of core cell is used in both NMOS and CMOS SRAMs from NEC.

CMOS Cell

CMOS technology, with its high-speed, low-power characteristics, makes an attractive choice for memory backup systems.

In figure 3, Q1-Q3 and Q2-Q4 form two CMOS inverters that are cross-coupled to form the conventional flip-flop of the SRAM cell. Unlike the enhancement or polysilicon resistor cells, the CMOS cell does not have a dc current path (other than leakage) in either of its quiescent logic states. While the potentially lower-leakage and wider-voltage operating range makes the six-transistor CMOS cell very desirable for battery backup operation, the large die area required makes it less competitive in cost and memory density.

Figure 2. Four-Transistor Cell—Polysilicon Resistor

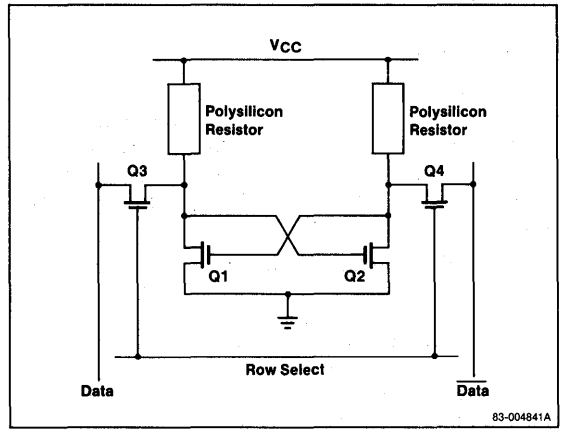
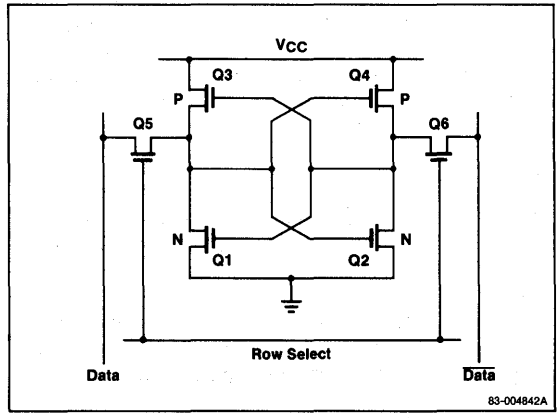


Figure 3. CMOS Cell



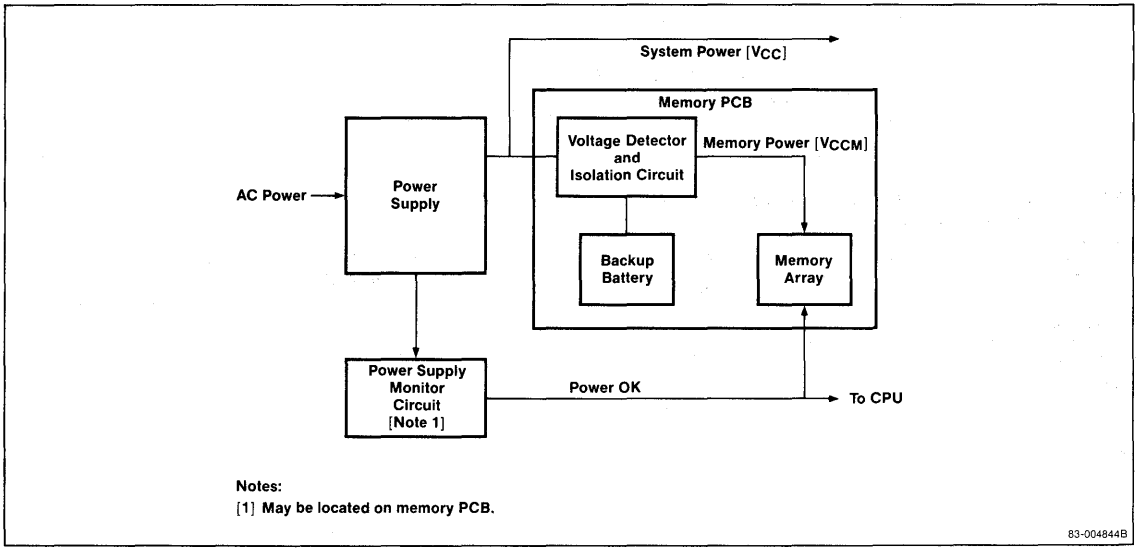
Battery Backup Concept

The goal of a memory backup system design is to guarantee memory data retention for days, months, or years. In the past, these memory backup circuits were implemented as part of the computer's power supply circuit. Today, the memory backup function is designed as part of the individual memory circuit, where each provides a constant secondary (backup) power source and the necessary circuitry to detect power failures and isolate the main power supply from the backup power source (battery). The battery backup circuit must be an integral part of printed circuit board layout. Furthermore, SRAM technology must be able to guarantee the requirements of the memory battery backup function. The following sections discuss in detail the aspects of memory battery backup circuit design using NEC's low-power SRAM technology.

A typical functional block diagram for a memory battery backup system is illustrated in figure 4. The power supply converts ac voltage into a regulated dc voltage, which powers all of the system components (V_{CC}). The power supply monitor circuit detects a power failure and generates an interrupt to the CPU. This circuit also signals the memory circuit to deselect the memory array, thus protecting the memory from false CPU commands. The power supply monitor circuit may be centralized to the power supply or decentralized to each memory circuit.

On the memory circuit, power failure is sensed by a voltage-detector circuit, which isolates the system power from the memory power, allowing the backup battery to become active.

Figure 4. Battery Backup System Block Diagram



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Backup Battery Selection

Battery Type

Nickel-cadmium batteries and lithium batteries were compared for use in a memory battery backup application. Although nickel-cadmium batteries have been a popular choice for this application, recent years have seen the development of lithium batteries. Some characteristics of these two types of batteries are contrasted in table 1. For additional comparison, the characteristics of current drain versus operating time for nickel-cadmium and lithium batteries are shown in figures 5 and 6, respectively.

Since lithium batteries provide a constant current for up to 10 years in this type of low-power application, they were chosen over nickel-cadmium for this design example. A single 3-volt lithium battery is adequate for most CMOS SRAM applications. If higher voltage is required, batteries may be connected in series.

Physical characteristics of a battery are determined by the manufacturer according to common system requirements. The designer must select a battery of the proper size and shape to meet the requirements of printed circuit board technology. Such requirements may include terminal connections and solderability.

Table 1. Lithium Versus Nickel-Cadmium Battery Characteristics

Characteristic	Lithium	Nickel-Cadmium
Shelf life	10 years	6 months
Rechargeable	no	yes
Energy density	5000 mAh*	4000 mAh*
Cost	moderate	moderate
PCB-compatible	yes	yes

*milliampere hours

Figure 5. Current Drain Versus Operating Time— Nickel Cadmium Battery

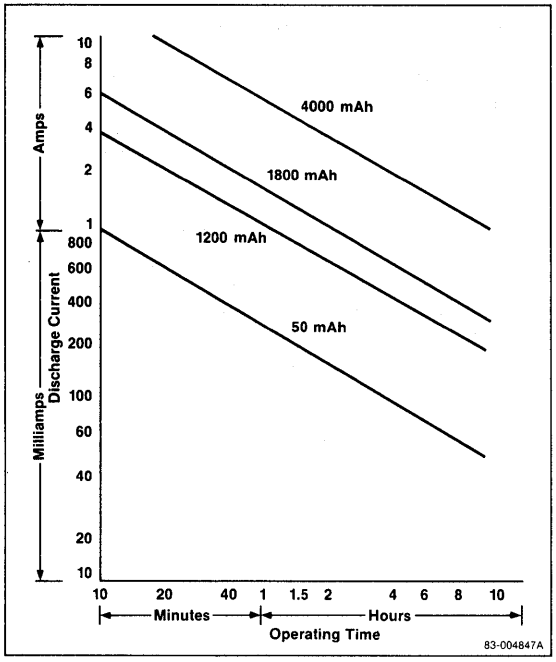
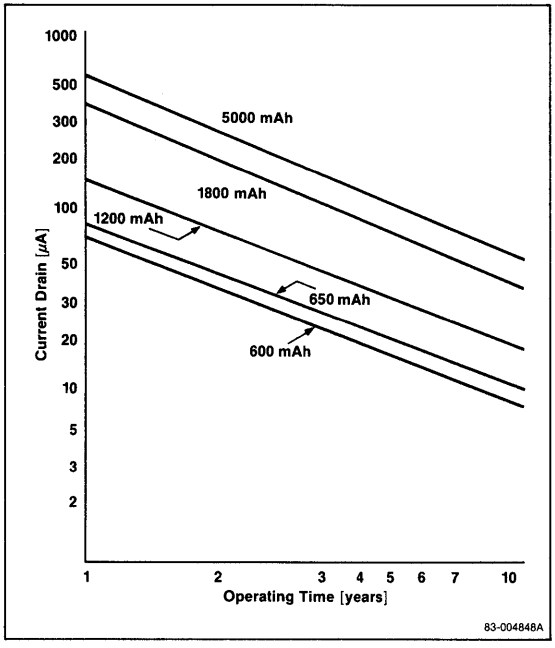


Figure 6. Current Drain Versus Operating Time— Lithium Battery



Battery Capacity

Battery capacity defines the current drive of the battery over a period of time, measured in milliampere hours (mAh). Required capacity of the battery selected for the memory backup circuit can be determined from the following formula:

Current required (mA) x time in backup mode (hours/day) x 365 days/year x number of years

Battery capacity is affected by temperature, humidity, and load conditions. The designer must ensure that these conditions do not degrade the operating life (discharge characteristics) of the battery. Figures 7 and 8 show the effects of temperature and load current variations on lithium battery discharge characteristics.

Figure 7. Lithium Discharge Characteristics— ≃ 20 μA Load

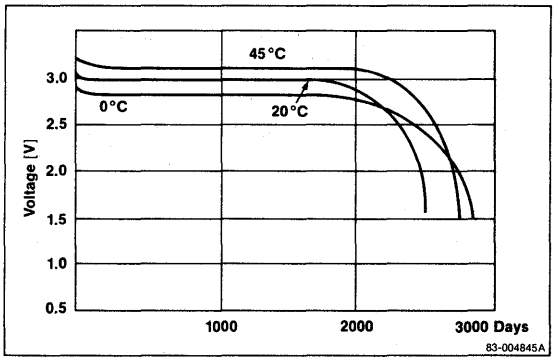
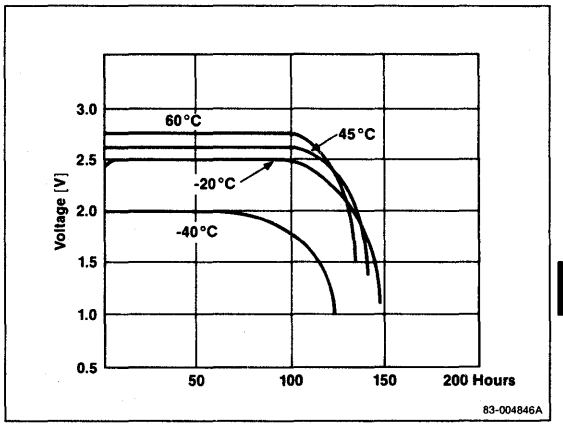


Figure 8. Lithium Discharge Characteristics— ≃ 8.5 mA Load



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Design Example

This section presents and documents a detailed battery backup design example. The discussion encompasses SRAM memory array design, current and voltage requirements, voltage-detector and isolation circuitry, and memory protection design considerations.

SRAM Memory Array

For the battery backup design example, NEC's μPD43256A-15LL (a CMOS-fabricated, 150-ns SRAM memory device) is used to implement the memory array, configured as 32K by 32 bits using four 32K x 8-bit memory devices (figure 9). The memory array's interface of common address lines, common I/O lines, and control signals are asserted by control logic common to all devices. However, the power supply connection to the memory array requires special consideration. The power plane of the memory array must be isolated from the system power supply to ensure that the backup battery drives only the memory array (see "Voltage-Level Detector and Isolation Circuit Design").

Current and Voltage Requirements

The first task for the designer is to define the required battery capacity. Table 2 shows data retention characteristics for the μPD43256A SRAM. The maximum data retention current for this device is 20 μA at 0 to 70 °C. For a circuit with four memory devices, total memory array current is 4 x 20 μA = 80 μA.

The battery's operating period is assumed to be 10 years at 12 hours-per-day. Using the formula shown under "Battery Capacity," the required capacity of the battery can be derived from this calculation.

80 μA x 12 hours/day x 365 days/year x 10 years = 3504 mAh

Requirements for the data retention voltage of the μPD43256A SRAM are defined in table 2, while figure 10 shows timing requirements for data retention with respect to the $\overline{CS}$ chip select signal.

Table 2. μPD43256A SRAM Data Retention Characteristics

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{CCDR}	2.0		5.5	V	$\overline{CS} \geq V_{CC} - 0.2$ V
Data retention supply current	I_{CCDR}		1	50	μA	$V_{CC} = 3.0$ V; $\overline{CS} \geq V_{CC} - 0.2$ V (Notes 1, 2)
Chip deselection to data retention	t_{CDR}	0			ns	
Operation recovery time	t_R	t_{RC}			ns	

Notes:

(1) μPD43256A-LL: I_{CCDR} = 20 μA (max) for T_A = 0 to 70 °C and 3 μA (max) for T_A = 0 to 40 °C.

(2) μPD43256A-L: I_{CCDR} = 15 μA (max) for T_A = 0 to 40 °C.

Figure 9. SRAM Memory Array

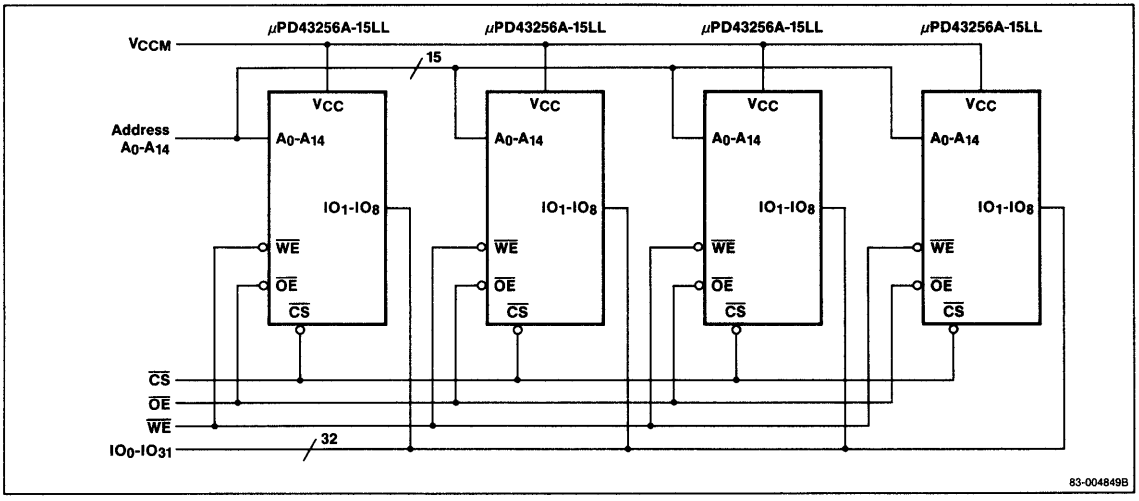
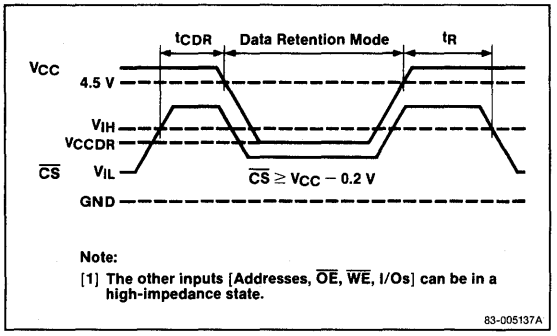


Figure 10. Data Retention Timing Waveforms



Battery Protection. Figure 11 shows the battery portion of the memory battery backup circuit. This portion of the circuit must be designed to provide the required data retention voltage and energy capacity for the memory backup function, yet protect the battery from reverse (charging) current. The diode and resistor shown in figure 11 were selected to protect the battery according to UL standards.

Since lithium batteries are not rechargeable, current-limiting protection must be provided to control the amount of current from the main power supply. For this purpose, the designer must select a diode that protects against charging current, yet provides sufficient voltage for memory battery backup.

The UL-allowable charging current for a lithium battery is specified as 1% of the battery capacity, calculated as follows:

1% x capacity of battery (mAh) ÷ (amount of time charging may occur (hours/day) x 365 days/year x number of years)

In this design example, a minimum capacity of 3504 mAh is required. The closest standard-size lithium battery has a capacity of 5000 mAh. The allowed charging current of this battery for a 10-year period is calculated in this way:

1% x 5000 mAh ÷ (12 hours/day x 365 days/year x 10 years) = 1.1 μA

Therefore, the diode selected to protect the battery must have a maximum reverse leakage current rating of 1.1 μA. To maintain the required data retention voltage at the memory device, a diode with a small forward-voltage drop must be selected. A Schottky diode, with a forward-voltage drop of 0.2 volt, provides a 2.7-volt battery backup voltage and also meets the reverse leakage current specification for this circuit.

According to UL standards, the battery must also be protected against charging current in case the protection diode is damaged. The designer must select a current-limiting resistor for this purpose. Resistor value is determined according to this formula:

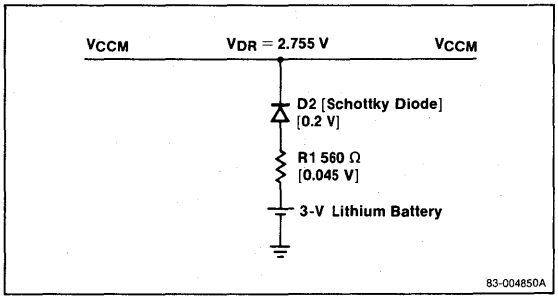
(V_{CC} − $V_{Battery}$) ÷ maximum charging current

UL standards specify a maximum charging current of 5 mA. Therefore, for the circuit in this design example, the minimum resistor value is specified as follows:

(5.5 − 3 V) ÷ 5 mA = 500 Ω

Selecting the aforementioned Schottky diode and a standard 10% resistor value of 560 Ω would guarantee minimum data retention voltage for the battery backup circuit. Total voltage drop across the protection diode and current-limiting resistor is equal to 0.245 volt, which provides a memory backup voltage of 2.755 volts—well above the minimum data retention voltage of 2 volts.

Figure 11. Backup Energy Source Circuit



Voltage-Level Detector and Isolation Circuit Design

The designer must also determine the best method for detecting power failures and isolating the main power supply from the backup battery. The circuit designed for these functions must fulfill two requirements: 1) sustain maximum operating current for the memory array, and 2) provide isolation protection during battery backup operation. Several design alternatives for voltage-level detector and isolation circuits are discussed in this section. The standards of comparison between these circuits are relative simplicity of design and voltage drop of the isolation element.

Note: In applications that are subjected to brownouts or extreme temperatures, these voltage-level detector and isolation circuits will minimize unnecessary cycling of the backup battery. However, considerations must be made to protect the memory devices from unstable circuit conditions, especially during power failure. For a discussion of memory protection under these circumstances, refer to "System Power Failure Design Considerations," following this section.

The designer must first determine maximum operating current of the memory array. Since maximum operating current for the μPD43256A SRAM is specified as 35 mA, total operating current is calculated as 4 x 35 mA = 140 mA for the memory array in this design example.

Diode Isolation Circuit. The diode isolation circuit in figure 12 provides a simple approach to memory battery backup. The isolation diode (D1) must be able to sustain the maximum memory operating current, yet minimize voltage skew between V_{CC} and V_{CCM} by limiting forward-voltage drop. A large voltage skew could cause illegal conditions to occur in normal system operations. A typical silicon diode with a forward-voltage drop of 0.7 V at a 140-mA load current would provide a large voltage skew between V_{CC} and V_{CCM}. Since SRAM V_{CC} is 0.7 V less than the level of a logic signal from a device not in the backup system, V_{CC} would have to be adjusted to a nonstandard level of 5.7 V to maintain V_{CC} at 5 V.

In contrast, a Schottky diode typically provides a forward-voltage drop of 0.2 V at a 3-A load current. This low voltage drop minimizes voltage skew and maintains logic input levels to within 0.2 V of V_{CC}, which makes the Schottky diode an ideal choice for the diode isolation circuit.

Voltage-Level Detector Circuit. The diode isolation circuit provides a simple means of battery backup, but some applications may require a circuit that minimizes voltage skew and has a more defined threshold level. The voltage-level detector circuit shown in figure 13 would allow the designer to fulfill these system requirements.

The voltage-level detector circuit isolates the supply voltage from the memory voltage when the voltage level falls below V_{CC} minimum. Threshold voltage is specified by using a zener diode in the voltage-divider circuit of figure 13. Care must be taken to ensure that marginal V_{CC} levels do not cause unnecessary cycling of the backup battery.

Figure 12. Diode Isolation Circuit

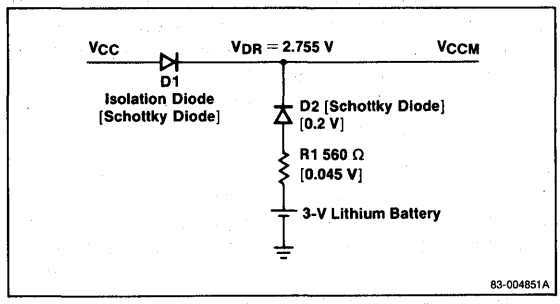
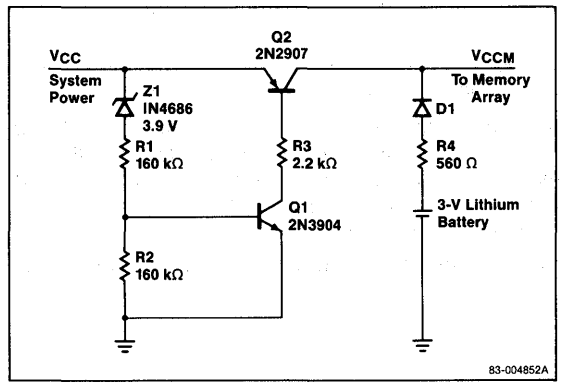


Figure 13. Voltage-Level Detector Circuit



The voltage-level detector circuit consists of zener diode Z1, switching transistor Q1, and the R1 and R2 voltage-divider network. The collector of Q1 is connected to the base of PNP isolation transistor Q2, isolating V_{CC} from V_{CCM} when the V_{CC} voltage level falls below threshold. Threshold voltage (V_{TH}) is determined by $V_{TH} = V_Z + V_{BE1}$, where V_Z is zener voltage and V_{BE1} is the base-to-emitter voltage drop of Q1. The threshold voltage in figure 13 is 3.9 + 0.6 V = 4.5 V, which is the specification for minimum V_{CC}. When V_{CC} drops below minimum specification, the zener diode operates in its forward-voltage region, and no base current flows into Q1. Q1 is then forced into cutoff. With Q1 in cutoff, no base current flows into Q2, consequently forcing Q2 into cutoff and isolating V_{CC} from V_{CCM}.

Isolation transistor Q2 must be capable of supplying a maximum memory operating current of 140 mA and also must provide a minimum V_{SAT} to reduce voltage skew. The PNP 2N2907 medium-power transistor chosen for this application can drive up to 150 mA with a dc gain range of 100 to 300. The maximum base current needed to turn on Q2 is calculated as follows:

$I_{BQ2} = I_{CQ2} \div h_{fe} = 140\ mA \div 100 = 1.4\ mA$

Since the base of Q2 is connected to the collector of Q1, and $I_{BQ2} = I_{CQ1}$, Q1 must be capable of driving a collector current of 1.4 mA or greater. The choice for Q1 is an NPN 2N3904, a general-purpose transistor with an I_C maximum of 10 mA and an h_{fe} of 100. The base current needed to turn on Q1 is calculated at 3 mA ÷ 100 = 30 μA, which is much less than the maximum I_{BQ1} provided by the R1-R2 network. The voltage divider R1-R2 must also forward-bias the base-emitter junction of Q1 to allow the transistor to operate in its active region. The voltage at the Q1 base node is 4.1 volts, which keeps Q1 turned on until threshold voltage is reached.

The circuit in figure 13 was characterized, and the relationship between the input and output voltage for two output loads is shown in figure 14. At an input voltage level of 4.5 V, the output voltage maintains a voltage level higher than the minimum data retention voltage of 2 V.

Schmitt Trigger Voltage-Level Detector. The voltage-level detector circuit is an improvement over the diode isolation circuit. However, the threshold point is sensitive to variations in Q1 gain, and could cause oscillations around the trigger point, draining the backup battery. The circuit shown in figure 15 reduces threshold sensitivity by adding an operational amplifier, thereby improving threshold margin by introducing hysteresis into the threshold region. This comparator circuit is commonly referred to as a Schmitt trigger.

Figure 14. Voltage-Level Detector/Transfer Function

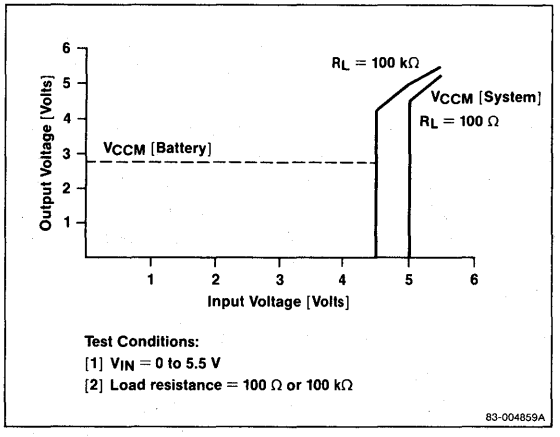


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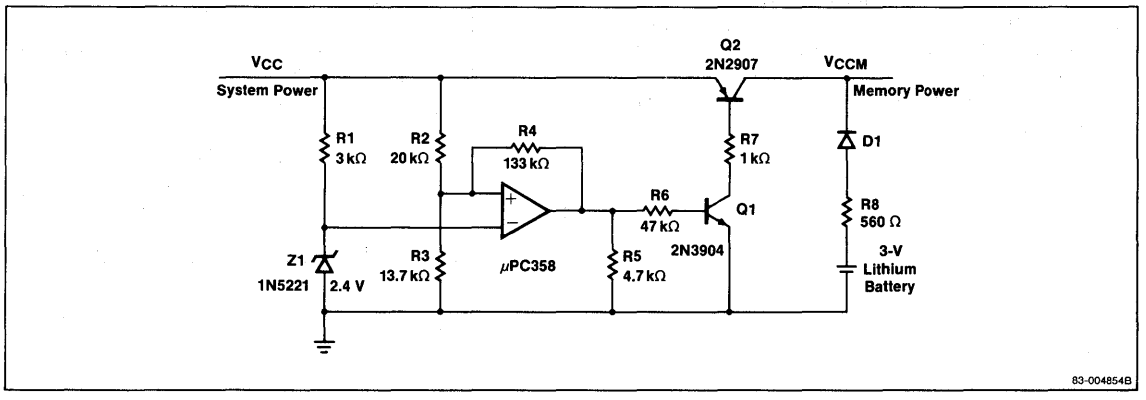
Figure 15. Schmitt Trigger Voltage-Level Detector Circuit



The noninverting input of the μPC358 is connected to a reference-voltage network consisting of R4 and R5. This reference voltage, when compared to the input voltage on the inverting input, determines when the output of the operational amplifier will transition. If a loop gain in excess of unity is chosen, the output waveform continues to be virtually discontinuous at the comparison voltage. However, at this point, the circuit would exhibit a phenomenom called hysteresis. Hysteresis voltage is determined by the resistor network of R4 and R5.

Figure 16 illustrates the response of the Schmitt trigger voltage-level detector circuit to the input signals connected to the noninverting input of the μPC358. When the input voltage reaches the value V1, the output goes high, and when the input is at V2, the output transitions to the low state. The difference between the input signals (V1 − V2) is called the hysteresis voltage (V_H). Therefore, the threshold voltage is dependent upon two input values, increasing the threshold sensitivity by the difference between the two voltages. For the circuit in figure 15, V_H is equal to 0.34 V. This circuit provides the best response of the three backup circuits, but at a cost of increased device count.

The circuit in figure 15 was characterized, and the relationship between input voltage and output voltage for a 100-kΩ output load is shown in figure 17. When the input voltage reaches 4.5 V (V1), the output voltage is set at a level higher than the minimum data retention voltage. Output voltage does not change until input voltage reaches a value of 4.1 V (V2).

System Power Failure Design Considerations

As shown in figure 18, V_{CC} decays slowly after power failure, providing time for an orderly system shutdown. Even during an orderly shutdown, the system may generate spurious memory commands, causing viable data to be overwritten. The designer can use the status signal generated by the system's power supply monitor circuit to protect the memory from false CPU commands after power failure. (The power supply monitor circuit is shown as part of the memory battery backup system in figure 4.)

Figure 16. Response of the Schmitt Trigger to an Arbitrary Signal

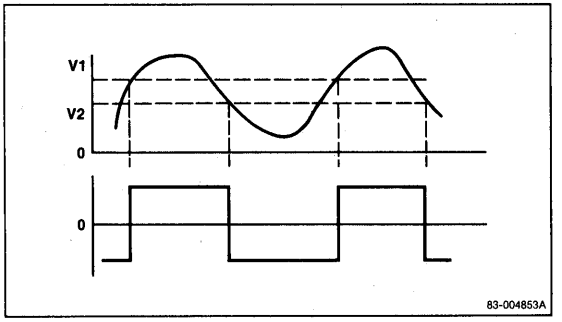


Figure 17. Schmitt Trigger Detector/Transfer Function

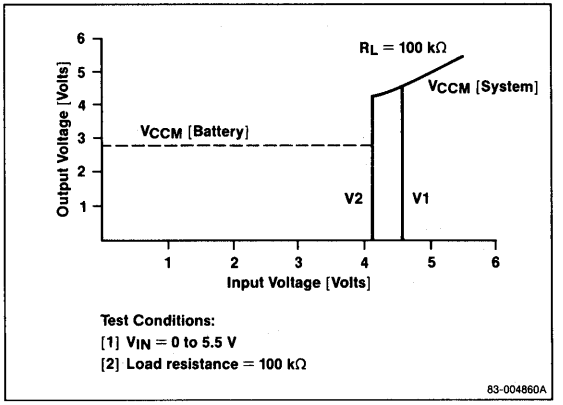
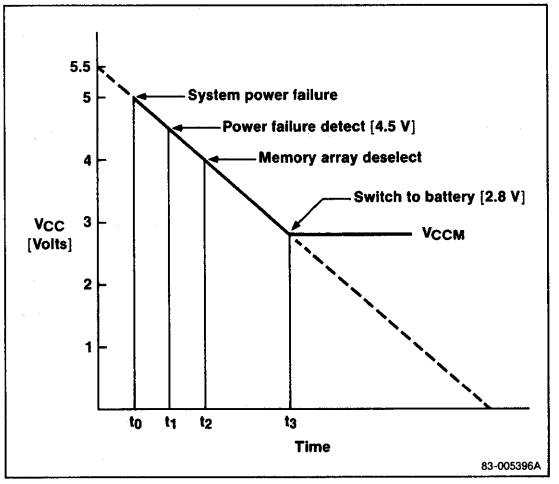


Figure 18. Power Failure V_{CC} Profile



The power supply status signal (Power OK) remains inactive during the entire time V_{CC} is off to force the output of the NAND gate to remain inactive (high). This status signal also is sent to the NAND gate of the memory circuit ("Power OK" in figure 19). The memory circuit "ands" this status signal with the other control signals and deselects the memory array before any false commands are generated.

Once the backup circuit has taken over and the memory array has been deselected, $\overline{CS}$ must be maintained at $V_{CC} - 0.2$ V. The 10-kΩ resistor ensures that the requirement for $\overline{CS} \geq V_{CCM} - 0.2$ V is met.

If a power supply monitor circuit is not provided, the designer may design one. The circuit shown in figure 20 uses a voltage-level detector design to detect when V_{CC} falls below 4.5 V. This circuit is similar to the voltage-level detector circuit used in the battery backup design example. Rather than control an isolation transistor, this power supply monitor circuit generates a power supply status signal (Power OK) to the memory select logic.

The circuit shown in figure 20 is subject to oscillations due to variations in Q1 gain and limited threshold margins. The addition of a Schmitt trigger to the power supply monitor circuit (figure 21) increases threshold margins by introducing hysteresis into the threshold region. The amount of hysteresis is determined by the values of R4 and R5. When input voltage falls below 4.5 V, the circuit generates a low signal (Power OK) to the memory select logic, and the memory array is deselected. Power OK remains low because R5 pulls it down as long as V_{CC} is off.

Figure 19. Memory Array Deselect Circuit

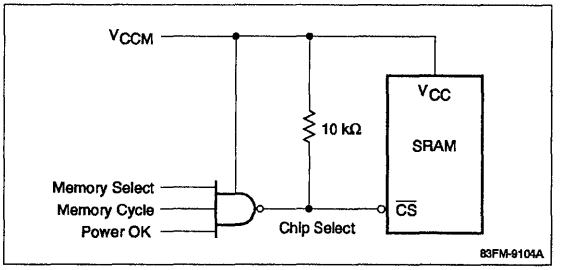


Figure 20. Power Supply Monitor Circuit

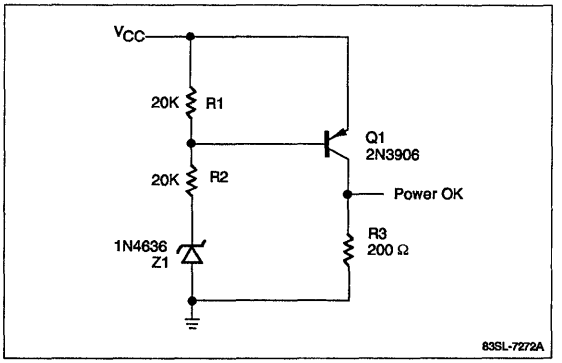
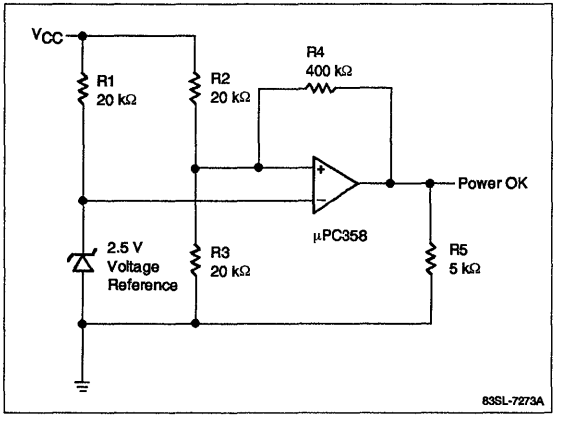


Figure 21. Power Supply Monitor Circuit With Schmitt Trigger



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NEC Electronics Inc.

Application Note 90-04
Battery Backup Using NEC's Supercaps™

Introduction

Supercaps are an innovative type of capacitor providing a volumetric efficiency (i.e., capacitance per unit volume for a given voltage) of 10 to 50 times that of conventional aluminum electrolytic capacitors. High capacitance (2.2 million μF) and low leakage current make the supercap an efficient, reliable and cost-effective energy storage device.

In 1879, the theory of electric double-layer capacitance was introduced by Helmholtz, but the first electric double-layer capacitor using solid electrolyte wasn't developed until 90 years later, a gap caused in part by a lack of proper materials. In 1979, NEC introduced its electric double-layer supercapacitor, nicknamed *supercap*, and with it a new manufacturing technology and newly developed construction materials.

Today NEC manufactures an extensive line of supercaps to meet a variety of demands. For example, large current backup is provided by our FA- and FE-series, small current backup by our FY-series, moderate current backup by the FS-series, and wide operating margins by the FR-series.

Theory of Operation

At each interface (figure 1), an array of charged particles and induced charges is thought to exist. This array is known as an electric double layer. The large capacitance of an electric double-layer capacitor arises from the charge stored at the interface as the electric field changes across two available phases. In a supercap, one phase consists of activated carbon particles and the other of sulfuric acid solution as an ionically conducting electrolyte. In general, the relationship of the charge per unit area (η) and the double-layer potential (ϕ) is reflected by the following equation:

$$\eta = [d / (4\pi\delta)] \times \phi$$

where d is the dielectric constant of the interface media and δ is the mean distance between the solid surface (polarizable electrode) and the ionic center. The value of δ is a few angstroms. In the Helmholtz model, the potential gradient exists only in the area of the electric double layer. As a result, the potential curve is as shown in figure 1.

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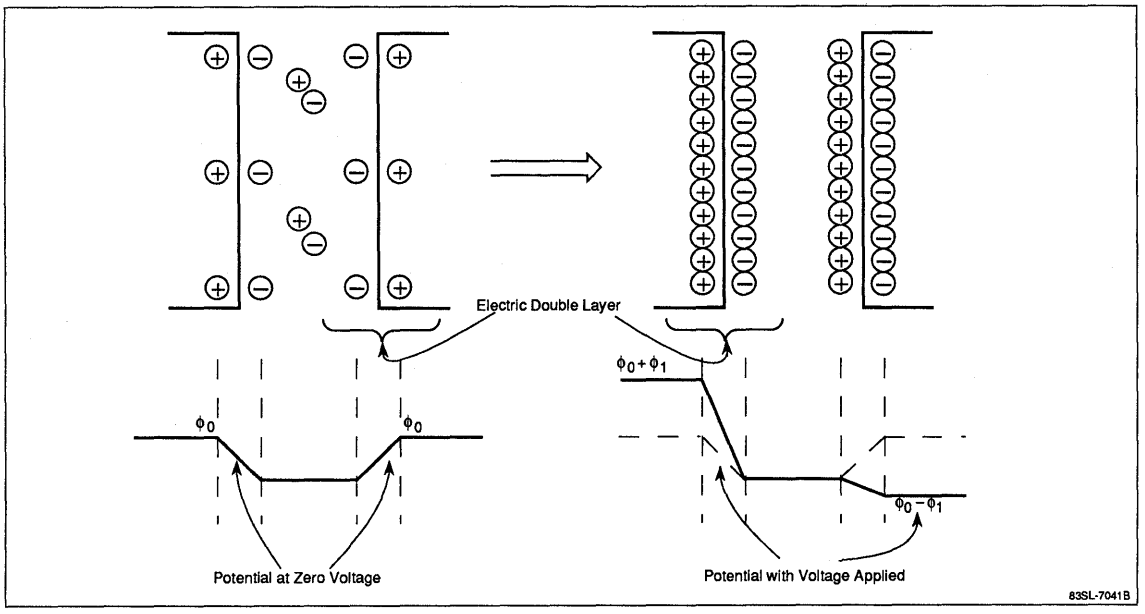
Figure 1. Basic Model of a Supercap



Supercap is a trademark of NEC Corporation.

If ϕ_0 represents ϕ when no external bias is applied, then the calculation is expressed this way:

$$\eta_0 = [d / (4\pi\delta)] \times \phi_0$$

Conversely, some charges are accumulated at the interface if an external electric field is applied to the system shown in figure 1. In this case, the potential rises to ϕ_1 and the charge of η_1 can be accumulated as shown by this equation:

$$\eta_1 = [d / (4\pi\delta)] \times (2\phi_1 - \phi_0)$$

The charge equivalent to η_1 can be accumulated by changing the external electric field, as follows:

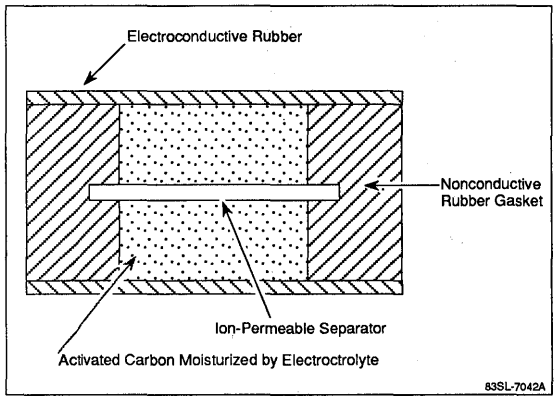
$$\eta_1 \cong 2\eta_0 (\phi_1 / \phi_0), \text{ where } (\phi_1 \gg \phi_0)$$

The experimental result, using mercury as a polarizable electrode, shows a 20 to 40 $\mu F/cm^2$ value. Therefore, if the activated carbon behavior is the same as that of mercury, the capacitance for a capacitor consisting of activated carbon with a 1,000 m^2/g surface area is calculated to be 200 to 400 F/g, a very large value. In this way, a device with large capacitance and small size can be easily manufactured.

Structure

The cross section of a unit cell is shown in figure 2. The activated carbon particles moisturized (semi-liquid state) by diluted sulfuric acid electrolyte are segregated by a porous, ion-permeable separator. The unit cell is sealed by the electroconductive polymer and a nonconductive rubber gasket, which are vulcanized simultaneously. No adhesive glue is used for the seal.

Figure 2. Unit Cell



The breakdown voltage of the unit cell can be as low as 1.2 volts (thermodynamically), which is the decomposition voltage of aqueous electrolyte solution. Therefore, several unit cells are stacked in series to get the required rated voltage (figure 3).

Performance

Supercaps have no standard specifications from groups such as the EIA and, accordingly, are specified by individual manufacturers. For example, NEC has specifications to cover the following:

- Operating temperature
- Maximum working voltage
- Capacitance
- Capacitance tolerance
- Equivalent series resistance[1] (ESR)
- Charging (leakage) current at 30 minutes
- Voltage holding characteristics
- Temperature characteristics
- Lead terminal strength
- Vibration
- Solderability
- Resistance to soldering heat
- Temperature cycling
- Humidity
- Load life

Detailed information can be found in the data sheets for each series.

Note:

[1] Due to relatively high ESR, supercaps may be unsuitable for filtering applications. ESR involves different resistance factors in the electrolyte, the activated carbon particles, the carbon to electroconductive polymer contacts, and the contacts between cell units, among others.

Calculating Required Supercap Size

When the required backup current is on the order of miliamps or more, size is determined as shown in figure 4. When backup current is on the order of microamps or less, figure 5 applies. Keep in mind that the curves in figure 5 are approximations and actual backup time may vary.

Figure 3. Cross Section

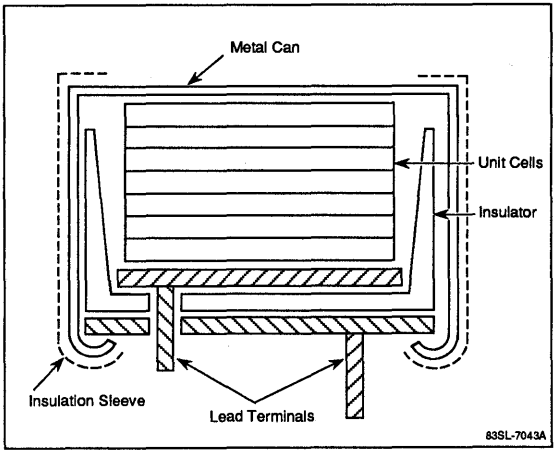


Figure 4. Relationship Between Voltage and Time While the Supercap is Charging and Discharging

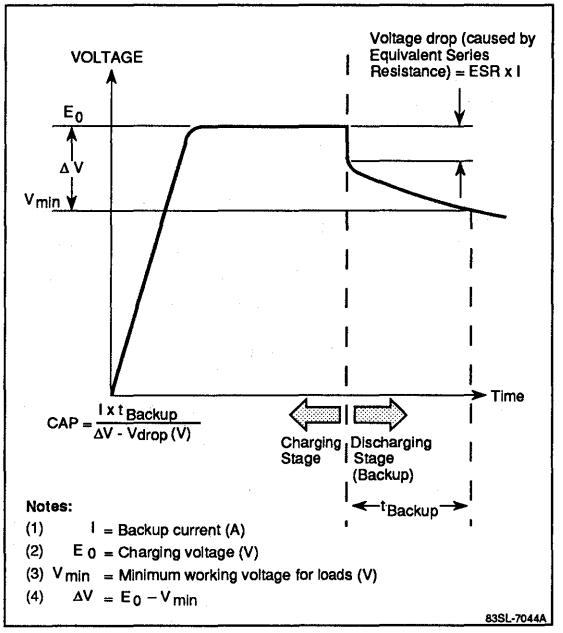


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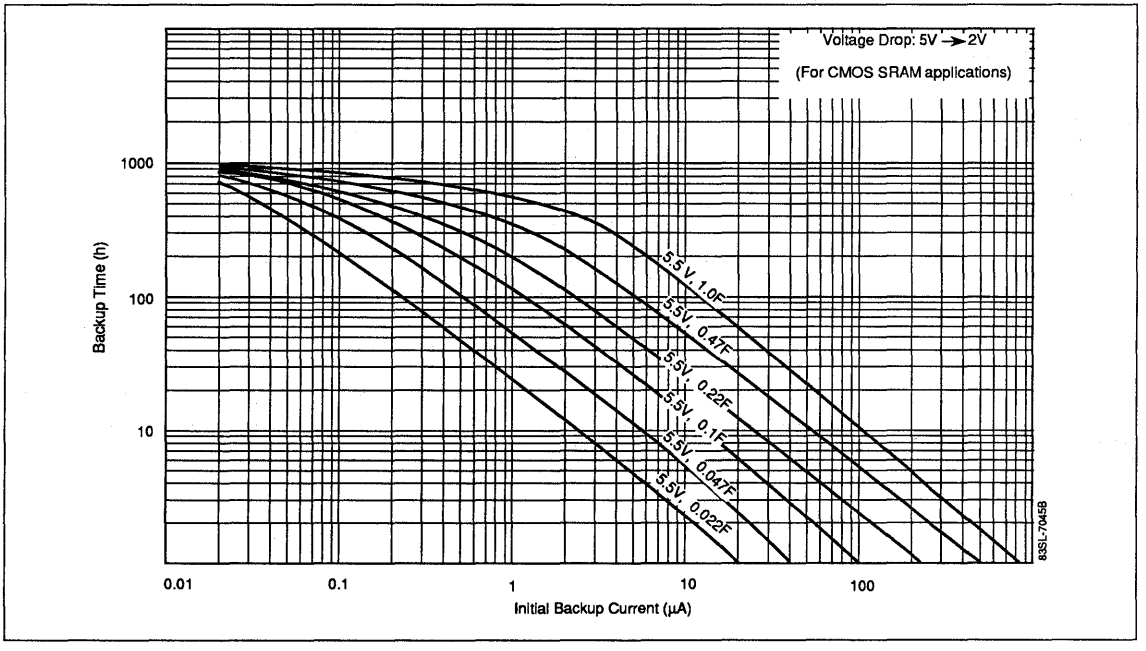
Figure 5. Minimum Backup for CMOS RAMs



Applications

Supercaps typically are used as

- Backup power during primary outages
- Backup power during voltage drops caused by heavy loads
- Backup sources to primary batteries

As battery backup sources for the microcomputer and memory devices found in VCRs, AM-FM tuners, cameras and hand-held computers, their primary function is to prevent errors in operation during power outages (figure 6). Until recently, batteries or electrolytic capacitors have been used, but because batteries have to be replaced or recharged and aluminum capacitors are too large, supercaps are an excellent alternative to traditional backup technologies.

Figure 6. Basic Backup Circuit Using a Supercap

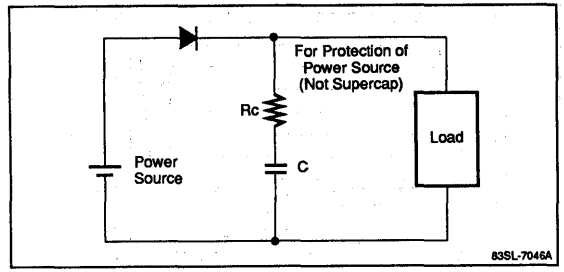


Table 1. Comparison of Features

Features	Supercaps	Ni-Cd Batteries	Lithium Batteries	Aluminum Electrolytic Capacitors
Operating temperature	−40 to 85°C	−20 to 65°C	−20 to 60°C	−40 to 85°C
Working voltage	5.5 V and 11 V	1.2 V	3 V	Over 6.3 V
Capacitance	1	210	360	0.01
Charging time	Several seconds	Several hours	—	Several seconds
Charging current limitations	None	Limited	—	None
Charge/discharge cycles	Infinite (more than 10^5 times)	300 to 500 times	—	Infinite (more than 10^5 times)
Reflow soldering	Applicable	Not applicable	Not applicable	Applicable
Materials safety	No noxious materials	Cadmium	No noxious materials	No noxious materials

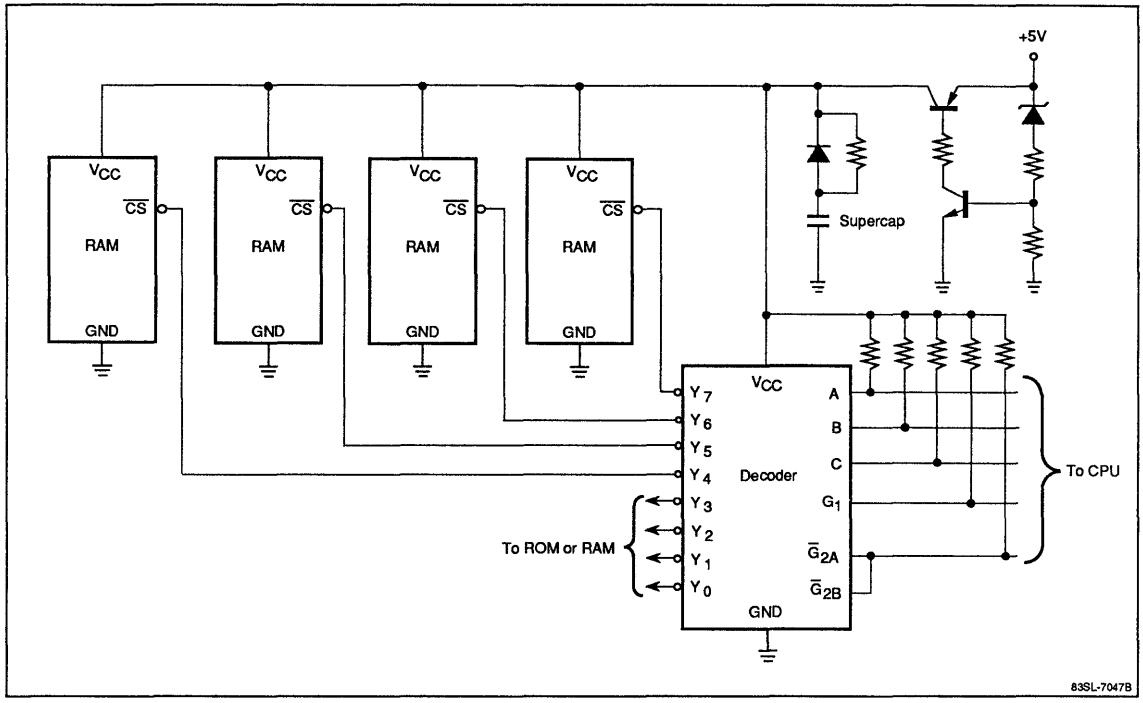
Notes:

(1) Capacitance is shown as a ratio to the supercap's electric charge per unit volume.

Table 2. Advantages and Disadvantages of Alternate Sources to Supercaps

Backup Source	Advantages	Disadvantages
Ni-Cd Battery	Rechargeable	Noxious materials
	Large capacity	Must be replaced every 6 months to 2 years because of limited charge/discharge cycles
		Needs protection against rapid charging
		May be broken by shorting terminals after charging
Lithium Battery	Large capacity	Unsuitable for high current applications
		No reflow soldering
		Not rechargeable
Aluminum Electrolytic Capacitor	Easy to use	Small capacitance

Figure 7. Memory Backup Circuit Block Diagram



Section 29
Package Drawings

Device/Package Cross-Reference

Part Number	Ordering Designation	Package	Page
MC-434000	D	32-Pin Ceramic DIP (600-mil)	43
	E	32-Pin Plastic (FR-4) DIP (600-mil)	44
μPB100422	B	24-Pin Ceramic Flatpack	29
	D	24-Pin Ceramic DIP (400-mil)	25
μPB100470	D	18-Pin Cerdip (300-mil)	17
μPB100474	B	24-Pin Ceramic Flatpack	29
	D	24-Pin Ceramic DIP (400-mil)	25
	K	24-Pin Ceramic LCC	28
μPB100474A	BH	24-Pin Ceramic Flatpack	29
	D	24-Pin Cerdip (400-mil) #2	25
μPB100474E	DH	24-Pin Cerdip (400-mil) #1	24
	BH	24-Pin Ceramic Flatpack	29
μPB100476LL	DH	28-Pin Cerdip (400-mil) #2	36
	BH	28-Pin Ceramic Flatpack	37
μPB100480	B	20-Pin Ceramic Flatpack	20
	D	20-Pin Cerdip (300-mil)	19
μPB100484	B	28-Pin Ceramic Flatpack	37
	D	28-Pin Cerdip (400-mil) #1	35
μPB100484A	B	28-Pin Ceramic Flatpack	37
	D	28-Pin Cerdip (400-mil) #1	35
μPB100A484	B	28-Pin Ceramic Flatpack	37
	D	28-Pin Cerdip (400-mil) #1	35
μPB10422	D	24-Pin Ceramic DIP (400-mil)	25
μPB10470	D	18-Pin Cerdip (300-mil)	17
μPB10474	D	24-Pin Cerdip (400-mil) #2	25
μPB10474A	D	24-Pin Cerdip (400-mil) #2	25
μPB10474E	DH	24-Pin Cerdip (400-mil) #1	24
	BH	24-Pin Ceramic Flatpack	29
μPB10476LL	DH	28-Pin Cerdip (400-mil) #2	36
	BH	28-Pin Ceramic Flatpack	37
μPB10480	B	20-Pin Ceramic Flatpack	20
	D	20-Pin Cerdip (300-mil)	19
μPB10484	B	28-Pin Ceramic Flatpack	37
	D	28-Pin Cerdip (400-mil) #1	35
μPB10484A	B	28-Pin Ceramic Flatpack	37
	D	28-Pin Cerdip (400-mil) #1	35
μPB10A484	BH	28-Pin Ceramic Flatpack	37
	D	28-Pin Cerdip (400-mil) #1	35
μPD100500	D	24-Pin Cerdip (300-mil)	24
μPD10500	D	24-Pin Cerdip (300-mil)	24

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD28C04	C	24-Pin Plastic DIP (600-mil)	23
	G	24-Pin Plastic SOP (Miniflat) (450-mil)	27
μPD28C05	C	24-Pin Plastic DIP (600-mil)	23
	G	24-Pin Plastic SOP (Miniflat) (450-mil)	27
μPD28C256	CZ	28-Pin Plastic DIP (600-mil)	34
μPD28C64	C	28-Pin Plastic DIP (600-mil)	34
μPD41256	C	16-Pin Plastic DIP (300-mil)	16
	L	18-Pin Plastic Leaded Chip Carrier	18
μPD41264	C	24-Pin Plastic DIP (400-mil)	22
	V	24-Pin Plastic ZIP (350-mil)	27
μPD41464	C	18-Pin Plastic DIP (300-mil) #1	16
	L	18-Pin Plastic Leaded Chip Carrier	18
μPD421000	C	18-Pin Plastic DIP (300-mil) #2	17
	GX	24/20-Pin Plastic TSOP I	26
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
μPD42101	C	24-Pin Plastic DIP (300-mil) #2	21
	G	24-Pin Plastic SOP (Miniflat) (450-mil)	27
μPD42102	C	24-Pin Plastic DIP (300-mil) #2	21
	G	24-Pin Plastic SOP (Miniflat) (450-mil)	27
μPD42116162		50-Pin Plastic TSOP II (400-mil)	55
μPD42116182		50-Pin Plastic TSOP II (400-mil)	55
μPD42116420		44-Pin Plastic TSOP II (400-mil) #2	54
μPD42116820		44-Pin Plastic TSOP II (400-mil) #2	54
μPD42116920		44-Pin Plastic TSOP II (400-mil) #2	54
μPD4216100	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	V	24-Pin Plastic ZIP (425-mil)	28
μPD4216101	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	V	24-Pin Plastic ZIP (425-mil)	28
μPD4216102	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD4216160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD4216160L	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4216180	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4216180L	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD4216400	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	V	24-Pin Plastic ZIP (425-mil)	28
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
μPD4216402	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	V	24-Pin Plastic ZIP (425-mil)	28
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
μPD4216410	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	V	24-Pin Plastic ZIP (425-mil)	28
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
μPD4216412	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	V	24-Pin Plastic ZIP (425-mil)	28
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
μPD4216800	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
μPD4216800L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD4216802	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD4216802L	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD4216900	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD4216900L	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD4216902	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD4216902L	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD4217100	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217101	G5	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217102	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4217160L	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4217180	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4217180L	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4217400	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD4217402	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217410	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217412	V	24-Pin Plastic ZIP (425-mil)	28
	G5M	28/24-Pin Plastic TSOP II (400-mil)	39
	LE	28/24-Pin Plastic SOJ (400-mil)	38
	G5	28/24-Pin Plastic TSOP II (400-mil)	39
μPD4217800	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD4217800L	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD4217802	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD4217802L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD4217900	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD4217900L	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD4217902	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD4217902L	G5M	32-Pin Plastic TSOP II (400-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD4218160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD4218160L	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4218180	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD4218180L	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42264	C	24-Pin Plastic DIP (400-mil)	22
	V	24-Pin Plastic ZIP (350-mil)	27
	LA	24-pin Plastic SOJ (300-mil)	26
μPD42270	C	28-Pin Plastic DIP (400-mil)	33
μPD42271	GF	64-Pin Plastic QFP	58
μPD42272	GF	64-Pin Plastic QFP	58
μPD42273	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42274	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42274-80	V	28-Pin Plastic ZIP (350-mil)	41
	LE	28-Pin Plastic SOJ (400-mil)	38
μPD42275	LE	40-Pin Plastic SOJ (400-mil)	49
μPD42280	GU	28-Pin Plastic SOP (Miniflat) (450-mil) #1	40
	V	28-Pin Plastic ZIP (350-mil)	41
μPD424100	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
μPD424100A	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
μPD424100L	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
μPD424101	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD424102	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424170A	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424170L	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424190A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424190L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400- il)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424256	C	20-Pin Plastic DIP (300-mil)	18
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GX	24/20-Pin Plastic TSOP I	26
μPD424260A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424260L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424263A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424263L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD424280A	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424280L	V	40-Pin Plastic ZIP (400-mil)	50
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
μPD424400	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424400A	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
μPD424400L	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
μPD424402	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424410	V	20-Pin Plastic ZIP (350-mil)	19
	LB	26/20-Pin Plastic SOJ (350-mil)	30
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424412	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD424440	LE	26/24-Pin Plastic SOJ (350-mil)	31
μPD424440L	LE	26/24-Pin Plastic SOJ (350-mil)	31
μPD424800A	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD424800L	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5M	28-Pin Plastic TSOP II (400-mil)	39

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD424810A	LE	28-Pin Plastic SOJ (400-mil)	38
	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	V	28-Pin Plastic ZIP (350-mil)	41
μPD424810L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	V	28-Pin Plastic ZIP (350-mil)	41
μPD424900A	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD424900L	G5	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD42505	C	24-Pin Plastic DIP (300-mil) #2	21
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42532	C	40-Pin Plastic DIP (600-mil)	49
μPD42601	V	20-Pin Plastic ZIP (350-mil)	19
	LA	26/20-Pin Plastic SOJ (300-mil)	30
μPD42641	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42644	LA	26/20-Pin Plastic SOJ (300-mil)	30
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42S16160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S16160L	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S16180	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S16180L	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD42S16800	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
μPD42S16800L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD42S16802	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
μPD42S16802L	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
μPD42S16900	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
μPD42S16900L	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD42S16902	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD42S16902L	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD42S17160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S17160L	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S17180	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S17180L	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S17800	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD42S17800L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD42S17802	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD42S17802L	LE	28-Pin Plastic SOJ (400-mil)	38
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	G5	28-Pin Plastic TSOP II (400-mil)	39
μPD42S17900	G5	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD42S17900L	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD42S17902	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5M	32-Pin Plastic TSOP II (400-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD42S17902L	G5M	32-Pin Plastic TSOP II (400-mil)	47
	LE	32-Pin Plastic SOJ (400-mil) #2	45
	G5	32-Pin Plastic TSOP II (400-mil)	47
μPD42S18160	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S18160L	LE	42-Pin Plastic SOJ (400-mil)	51
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S18180	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	LE	42-Pin Plastic SOJ (400-mil)	51
μPD42S18180L	LE	42-Pin Plastic SOJ (400-mil)	51
	G5	50/44-Pin Plastic TSOP II (400-mil)	56
	G5M	50/44-Pin Plastic TSOP II (400-mil)	56
μPD42S4100A	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42S4100L	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
	GSM	26/20-Pin Plastic TSOP II (300-mil)	32

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD42S4170A	V	40-Pin Plastic ZIP (400-mil)	50
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD42S4170L	V	40-Pin Plastic ZIP (400-mil)	50
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD42S4190A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4190L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4260A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4260L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4263A	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4263L	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
	V	40-Pin Plastic ZIP (400-mil)	50
μPD42S4280A	V	40-Pin Plastic ZIP (400-mil)	50
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD42S4280L	V	40-Pin Plastic ZIP (400-mil)	50
	G5	44/40-Pin Plastic TSOP II (300-mil)	52
	G5M	44/40-Pin Plastic TSOP II (300-mil)	52
	LE	40-Pin Plastic SOJ (400-mil)	49

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD42S4400A	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	LA	26/20-Pin Plastic SOJ (300-mil)	30
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42S4400L	GSM	26/20-Pin Plastic TSOP II (300-mil)	32
	LA	26/20-Pin Plastic SOJ (300-mil)	30-
	V	20-Pin Plastic ZIP (350-mil)	19
	GS	26/20-Pin Plastic TSOP II (300-mil)	32
μPD42S4440	LE	26/24-Pin Plastic SOJ (350-mil)	31
μPD42S4440L	LE	26/24-Pin Plastic SOJ (350-mil)	31
μPD42S4800A	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42S4800L	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42S4810A	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD42S4810L	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
μPD42S4900A	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD42S4900L	G5	28-Pin Plastic TSOP II (400-mil)	39
	G5M	28-Pin Plastic TSOP II (400-mil)	39
	LE	28-Pin Plastic SOJ (400-mil)	38
	V	28-Pin Plastic ZIP (350-mil)	41
μPD431000A	GZM	32-Pin Plastic TSOP I #1	46
	CZ	32-Pin Plastic DIP (600-mil)	43
	GW	32-Pin Plastic SOP (Miniflat) (525-mil)	47
	GZ	32-Pin Plastic TSOP I #1	46
μPD431001	LE	28-Pin Plastic SOJ (400-mil)	38
μPD431004	LE	28-Pin Plastic SOJ (400-mil)	38
μPD431008	LE	32-Pin Plastic SOJ (400-mil) #1	45

Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD431009	LE	36-Pin Plastic SOJ (400-mil)	48
μPD431016	LE	44-Pin Plastic SOJ (400-mil)	51
	G5	44-Pin Plastic TSOP II (400-mil) #3	55
μPD431018	G5	44-Pin Plastic TSOP II (400-mil) #3	55
	LE	44-Pin Plastic SOJ (400-mil)	51
μPD43251B	LA	24-Pin Plastic SOJ (300-mil)	26
	CR	24-Pin Plastic DIP (300-mil) #1	21
μPD43253B	LA	28-Pin Plastic SOJ (300-mil)	37
	CR	28-Pin Plastic DIP (300-mil) #2	33
μPD43254B	LA	24-Pin Plastic SOJ (300-mil)	26
	CR	24-Pin Plastic DIP (300-mil) #1	21
μPD43256A	GU	28-Pin Plastic SOP (Miniflat) (450-mil) #2	40
	C	28-Pin Plastic DIP (600-mil)	34
	GXM	32-Pin Plastic TSOP I #2	46
	GX	32-Pin Plastic TSOP I #2	46
μPD43256B	GU	28-Pin Plastic SOP (Miniflat) (450-mil) #2	40
	CZ	28-Pin Plastic DIP (600-mil)	34
μPD43258A	LA	28-Pin Plastic SOJ (300-mil)	37
	CR	28-Pin Plastic DIP (300-mil) #2	33
μPD43259A	CR	32-Pin Plastic DIP (300-mil)	42
	LA	32-Pin Plastic SOJ (300-mil)	44
μPD434000	CZ	32-Pin Plastic DIP (600-mil)	43
	GW	32-Pin Plastic SOP (Miniflat) (525-mil)	47
	G5	32-Pin Plastic TSOP II (400-mil)	47
	G5M	32-Pin Plastic TSOP II (400-mil)	47
μPD434001	LE	32-Pin Plastic SOJ (400-mil) #1	45
μPD434004	LE	32-Pin Plastic SOJ (400-mil) #1	45
μPD434008	LE	36-Pin Plastic SOJ (400-mil)	48
μPD4361B	CR	22-Pin Plastic DIP (300-mil)	20
	LA	24-Pin Plastic SOJ (300-mil)	26
μPD4362B	LA	24-Pin Plastic SOJ (300-mil)	26
	CR	22-Pin Plastic DIP (300-mil)	20
μPD4363B	CR	24-Pin Plastic DIP (300-mil) #1	21
	LA	24-Pin Plastic SOJ (300-mil)	26
μPD4368	CR	28-Pin Plastic DIP (300-mil) #2	33
	LA	28-Pin Plastic SOJ (300-mil)	37
μPD4369	CR	28-Pin Plastic DIP (300-mil) #1	32
	LA	28-Pin Plastic SOJ (300-mil)	37
μPD46710A	LN	52-Pin Plastic LCC	57
μPD46741A	LP	68-Pin Plastic LCC	59
μPD481440	LE	40-Pin Plastic SOJ (400-mil)	49

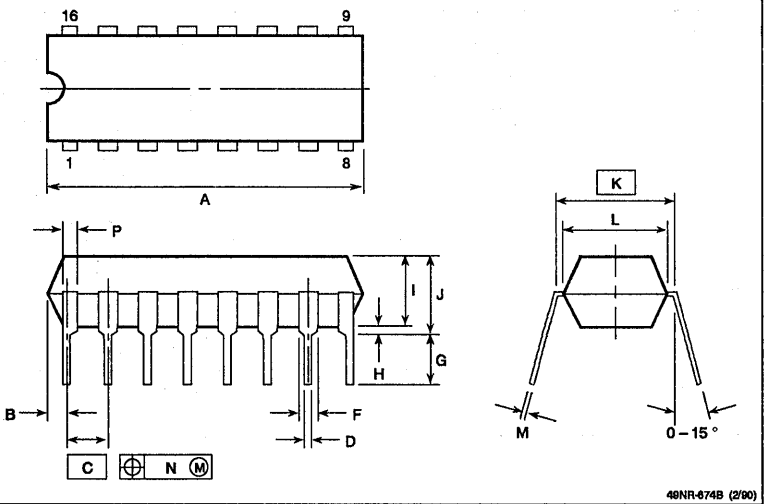
Device/Package Cross-Reference (cont)

Part Number	Ordering Designation	Package	Page
μPD482234	G5M	44-Pin Plastic TSOP II (400-mil) #1	53
	VF	40-Pin Plastic Shrink ZIP (450-mil)	50
	G5	44-Pin Plastic TSOP II (400-mil) #1	53
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD482235	G5M	44-Pin Plastic TSOP II (400-mil) #1	53
	VF	40-Pin Plastic Shrink ZIP (450-mil)	50
	G5	44-Pin Plastic TSOP II (400-mil) #1	53
	LE	40-Pin Plastic SOJ (400-mil)	49
μPD485505	GU	24-Pin Plastic SOP (Miniflat) (450-mil)	27-
	V	24-Pin Plastic ZIP (350-mil)	27
μPD485506	G5	44-Pin Plastic TSOP II (400-mil) #1	53
μPD488130		32-Pin Surface Vertical Package (SVP)	48
μPD488170		32-Pin Surface Vertical Package (SVP)	48

16-Pin Plastic DIP (300-mil)

Item	Millimeters	Inches
A	20.32 max	.800 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



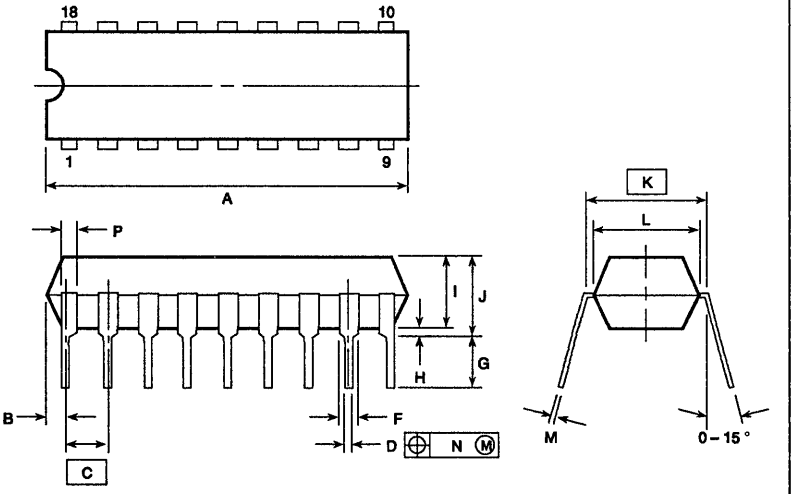
P16C-100-300SA

49NR-674B (2/90)

18-Pin Plastic DIP (300-mil) #1

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



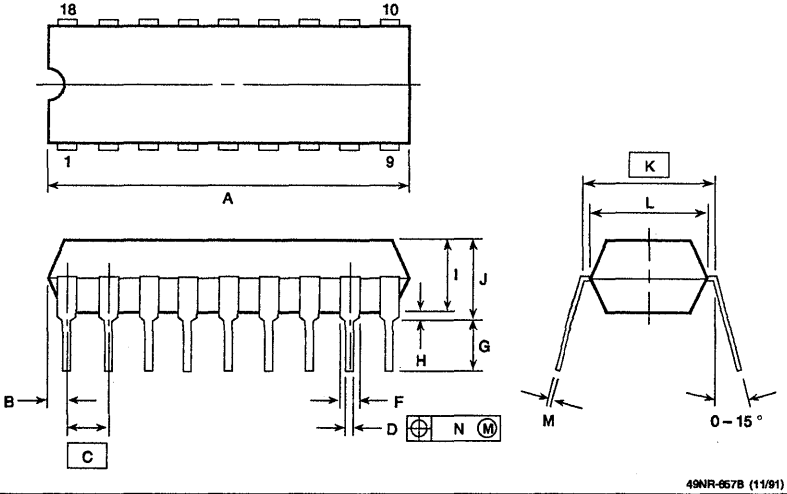
P18C-100-300SA

49NR-607B (2/92)

18-Pin Plastic DIP (300-mil) #2

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K *	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.

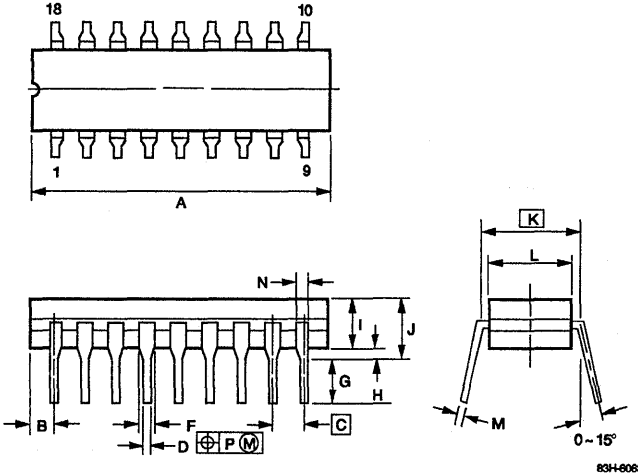


P18C-100-300WA

49NR-657B (11/91)

18-Pin Cerdip (300-mil)

Item	Millimeters	Inches
A	22.86 max	.900 max
B	1.27 max	.050 max
C	2.54 [TP]	.100[TP]
D	0.46 ± .05	.018 $^{+.003}_{-.002}$
F	1.42 min	.055 min
G	3.50 ±.30	.138 ±.012
H	0.51 min	.020 min
I	3.95	.156
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.60	.260
M	0.25 ±.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010



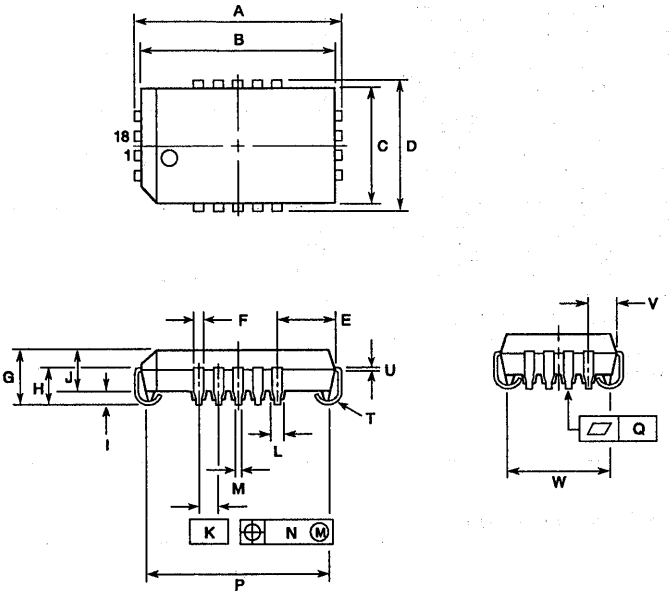
P18DH-100-300A

83H-8063B (6/89)

29

18-Pin Plastic Leaded Chip Carrier

Item	Millimeters	Inches
A	13.4 ± 0.2	.528 $^{+.008}_{-.009}$
B	12.5	.492
C	7.4	.291
D	8.3 ± 0.2	.327 $^{+.008}_{-.009}$
E	3.71 ± 0.15	.146 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ± 0.2	.138 $^{+.008}_{-.009}$
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
L	0.7	.028
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P	11.68 ± 0.20	.460 $^{+.008}_{-.009}$
Q	0.15	.006
T	0.8 rad	.031 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$
V	1.80 ± 0.15	.071 $^{+.006}_{-.007}$
W	6.60 ± 0.20	.260 $^{+.008}_{-.009}$



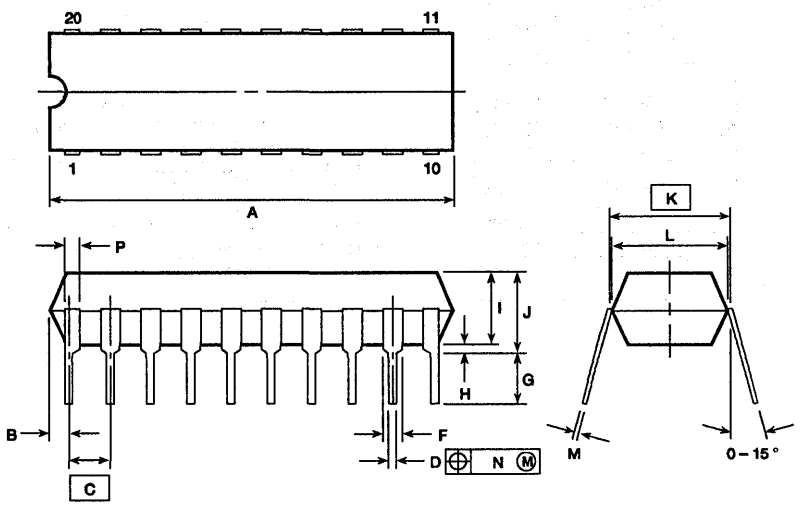
P18L-50A

49NR-675B (2/90)

20-Pin Plastic DIP (300-mil)

Item	Millimeters	Inches
A	25.4 max	1.000 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.

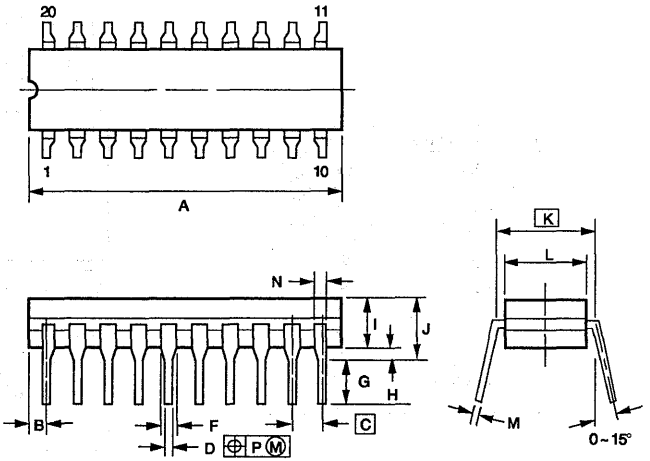


P20C-100-300WA

49NR-611B (11/91)

20-Pin Cerdip (300-mil)

Item	Millimeters	Inches
A	25.4 max	1.00 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ± .002
F	1.42 min	.055 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	3.95	.156
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.32	.288
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010

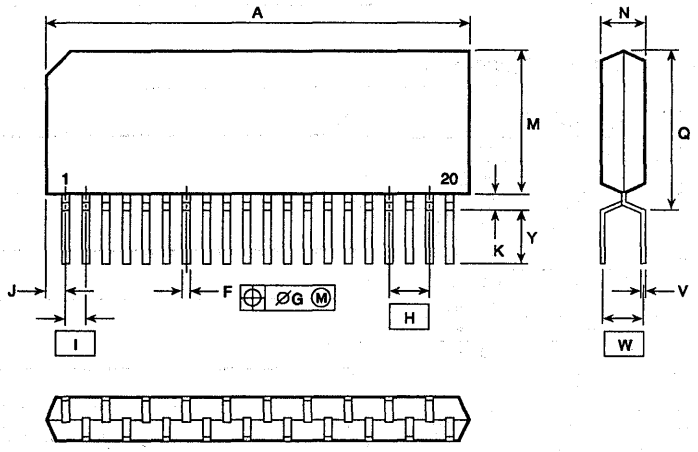


P20DH-100-300A

83IH-6194B

20-Pin Plastic ZIP (350-mil)

Item	Millimeters	Inches
A	26.67 max	1.050 max
F	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
G	∅0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ± 0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020



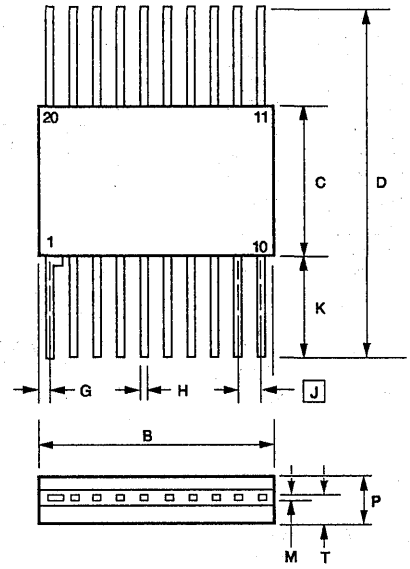
P20V-254-400A-1

49NR-620B (9/91)

29

20-Pin Ceramic Flatpack

Item	Millimeters	Inches
B	12.6 $^{+0.4}_{-0.1}$	.496 $^{+.016}_{-.004}$
C	9.8 $^{+0.4}_{-0.1}$	.388 $^{+.016}_{-.005}$
D	29.0	1.142
G	0.6	.024
H	0.43	.169
J	1.27	.050
K	9.6	.378
M	0.13	.005
P	2.18 max	.086 max
T	1.14 max	.045 max



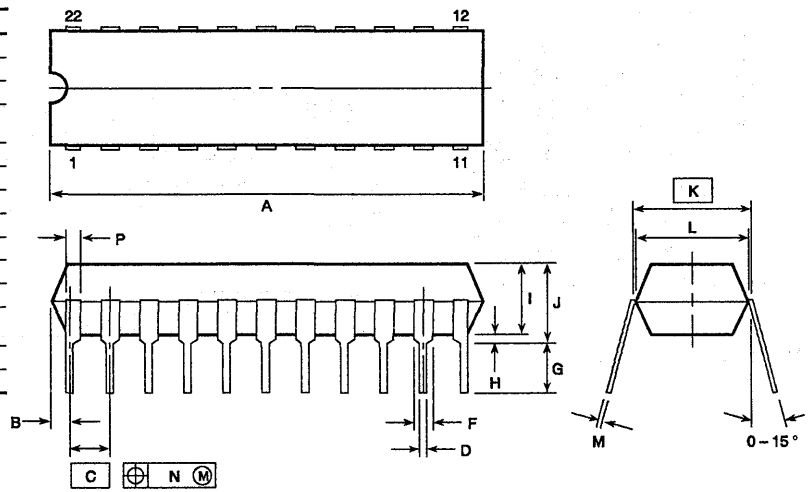
X20B-100A

83IH-5014B (7/89)

22-Pin Plastic DIP (300-mil)

Item	Millimeters	Inches
A	27.94 max	1.100 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.9 min	.035 min

* Item K to center of leads when formed parallel.



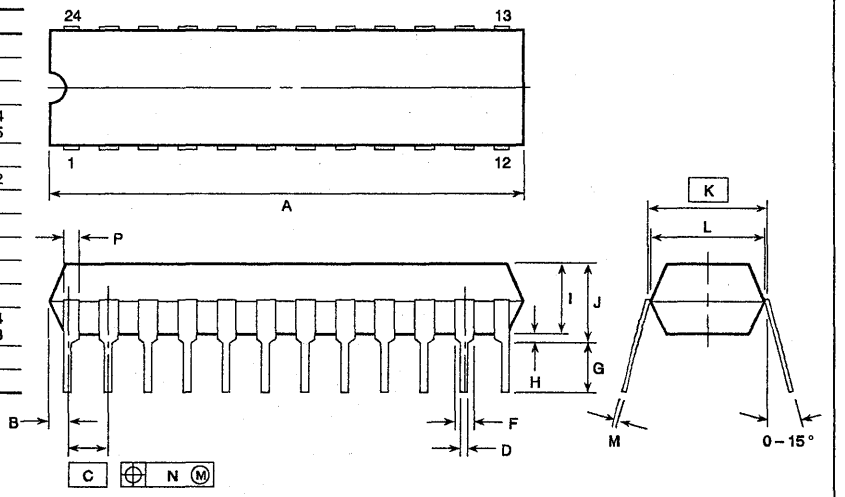
P22C-100-300WA

49NR-614B (10/89)

24-Pin Plastic DIP (300-mil) #1

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.35	.289
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.9 min	.035 min

* Item K to center of leads when formed parallel.



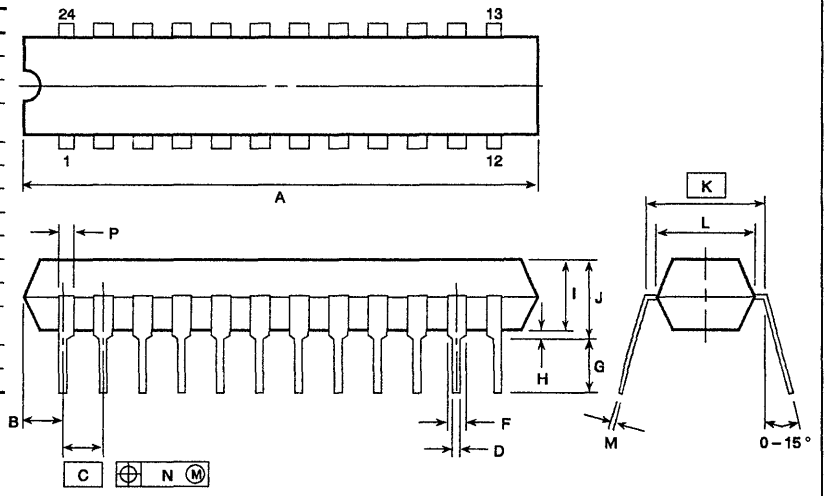
P24C-100-300WA

49NR-590B (6/89)

24-Pin Plastic DIP (300-mil) #2

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.4	.252
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



P24C-100-300A

49NR-619B (11/89)

29

NEC

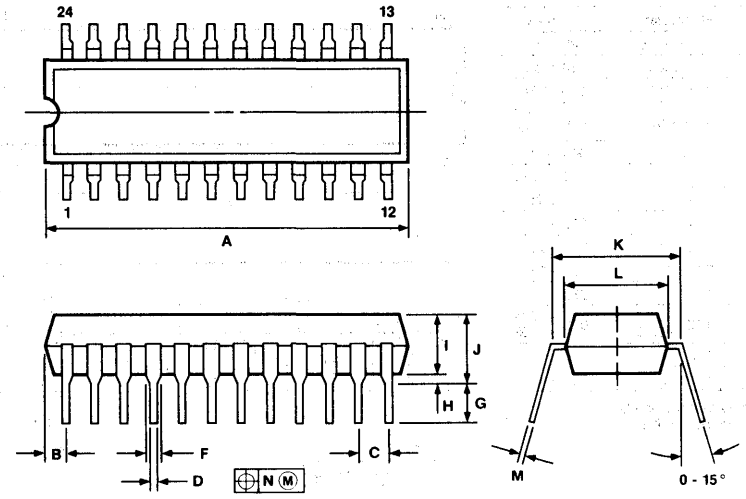
24-Pin Plastic DIP (400-mil)

Item	Millimeters	Inches
A	30.48 max	1.200 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	$.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.003}$
N	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



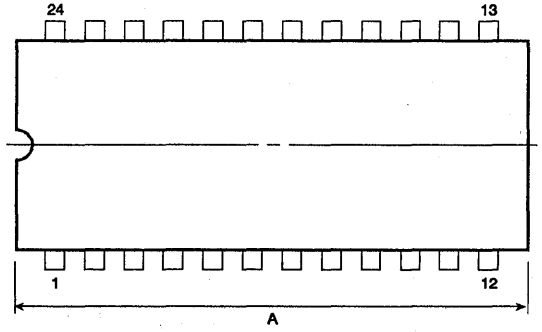
P24C-100-400A1

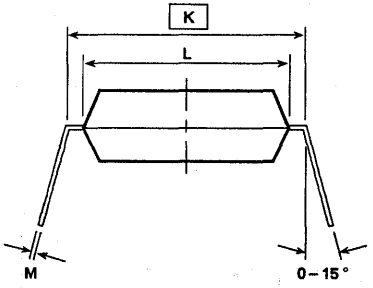
83-003627B

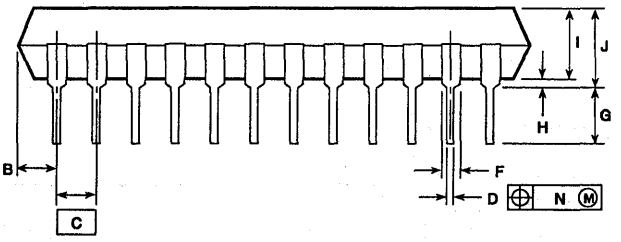
24-Pin Plastic DIP (600-mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K*	15.24 (TP)	.600 (TP)
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.







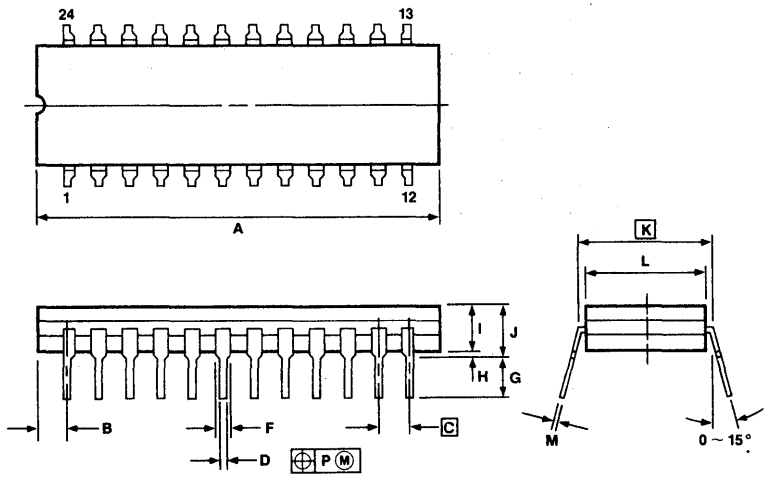
P24C-100-600

49NR-592B (6/91)

29

24-Pin Cerdip (300-mil)

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ±.002
F	1.42 min	.055 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	7.32	.288
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
P	0.25	.010



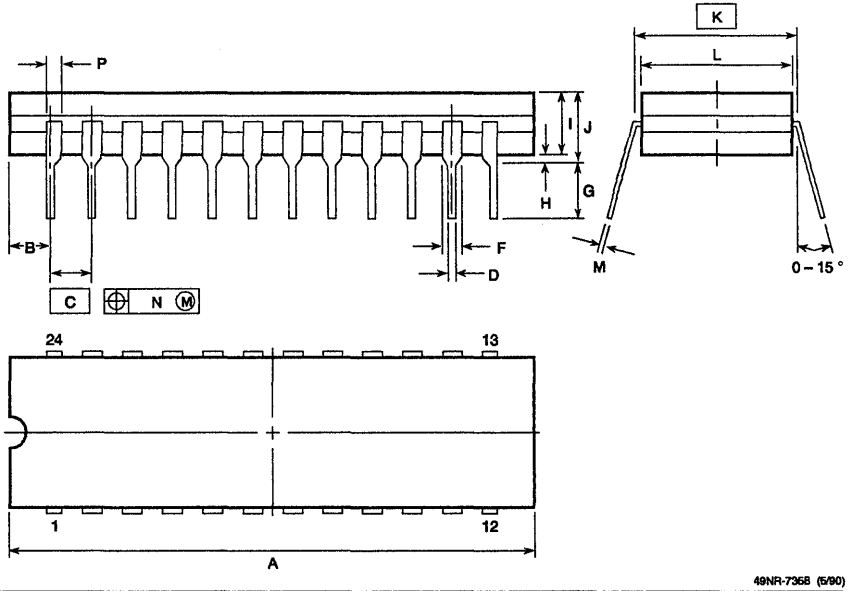
P24DH-100-300A

83-006012B

24-Pin Cerdip (400-mil) #1

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.20 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K*	10.16 (TP)	.400 (TP)
L	9.70	.382
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
P	0.89 min	.035 min

* Item K to center of leads when formed parallel.



P24DH-100-400A

49NR-7368 (5/90)

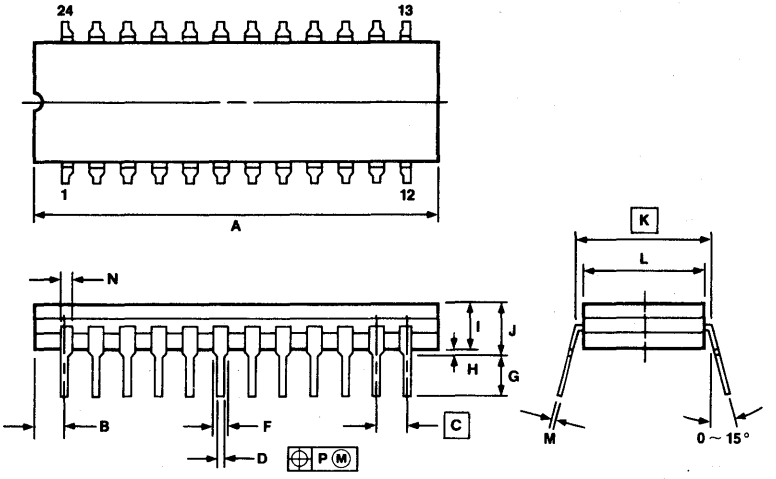
24-Pin Cerdip (400-mil) #2

Item	Millimeters	Inches
A	33.02 max	1.300 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	9.70	.382
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.89 min	.035 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



P24DH-100-400A

83-005012B

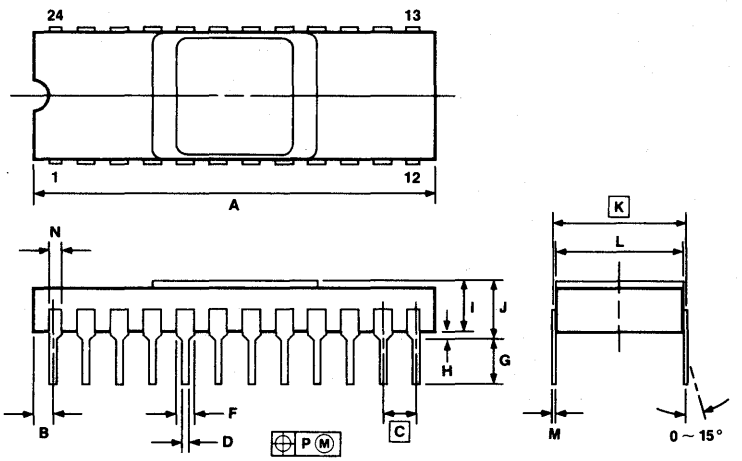
24-Pin Ceramic DIP (400-mil)

Item	Millimeters	Inches
A	33.02 max	1.30 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.46 ± 0.05	.018 ± .002
F	1.25 min	.049 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	2.74	.108
J	4.57 max	.180 max
K	10.16 [TP]	.400 [TP]
L	10.0	.394
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	1.00 min	.039 min
P	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

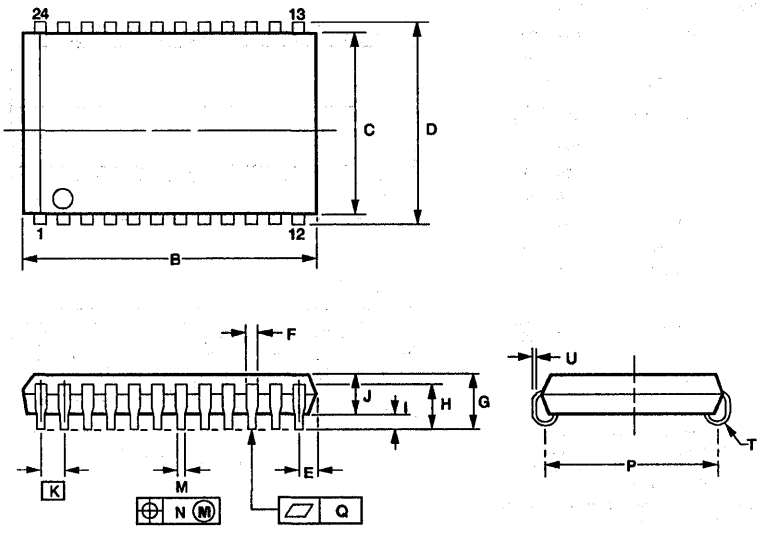


83-003579B

29

24-Pin Plastic SOJ (300-mil)

Item	Millimeters	Inches
B	$16.13^{+0.20}_{-0.35}$	$.635^{+.008}_{-.013}$
C	7.57	.298
D	8.47 ± 0.20	$.333^{+.009}_{-.008}$
E	1.08 ± 0.15	$.043^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ± 0.20	.138 ± .008
H	2.4 ± 0.20	$.094^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 [TP]	.050 [TP]
M	0.40 ± 0.10	$.016^{+.004}_{-.005}$
N	0.12	.005
P	6.73 ± 0.20	.265 ± .008
Q	0.15	.006
T	R 0.85	R .033
U	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$

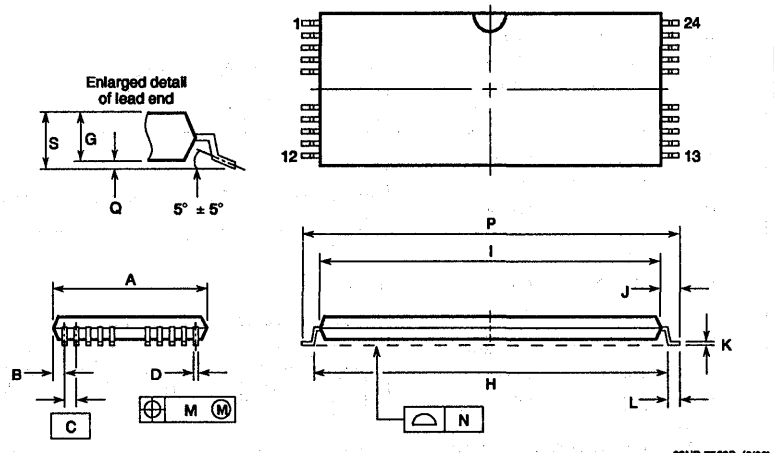


P24LA-50A

83IH-6851B

24/20-Pin Plastic TSOP I

Item	Millimeters	Inches
A	6.0 ± 0.2	.236 ± .008
B	0.45 max	.018 max
C	0.5 (TP)	.020 (TP)
D	0.20 ± 0.10	.008 ± .004
G	1.02 max	.041 max
H	15.0 ± 0.2	$.591^{+.008}_{-.009}$
I	14.4 ± 0.2	.567 ± .008
J	0.8 ± 0.2	$.031^{+.009}_{-.008}$
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$
M	0.08	.003
N	0.10	.004
P	16.0 ± 0.2	.630 ± .008
Q	0.05 ± 0.05	.002 ± .002
S	1.1 max	.044 max

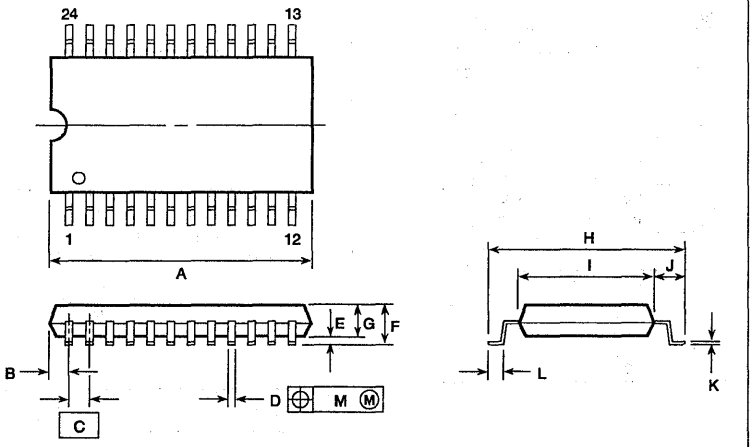


S24GX-50-JJH

83NR-7566B (8/92)

24-Pin Plastic SOP (Miniflat) (450-mil)

Item	Millimeters	Inches
A	16.51 max	.650 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.1 $^{+0.2}_{-0.1}$	.004 $^{+.008}_{-.004}$
F	2.5 max	.099 max
G	2.00	.079
H	12.2 ± 0.3	.480 $^{+.013}_{-.012}$
I	8.4	.331
J	1.9	.075
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.9 ± 0.2	.035 $^{+.009}_{-.008}$
M	0.12	.005

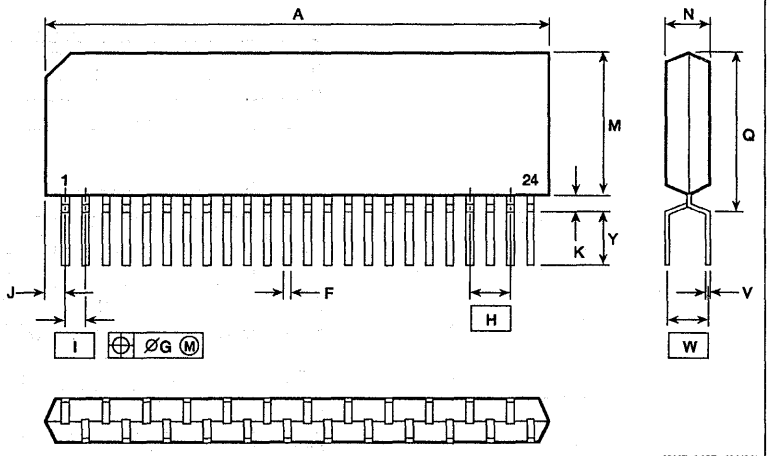


P24GM-50-450A

49NR-513B (6/91)

24-Pin Plastic ZIP (350-mil)

Item	Millimeters	Inches
A	31.75 max	1.250 max
F	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ± 0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020

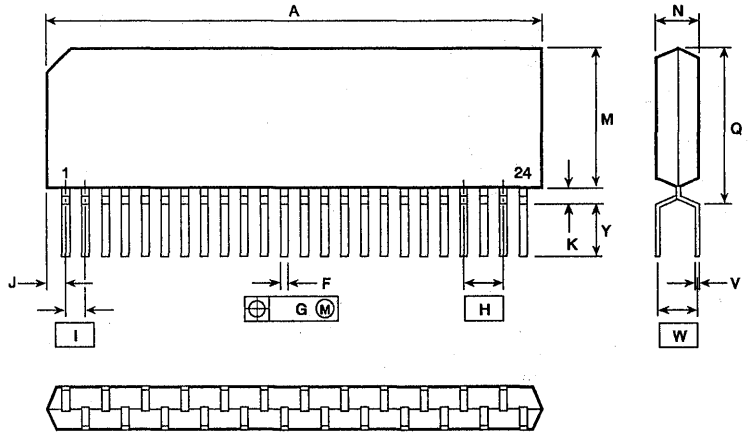


P24V-254-400A

49NR-642B (11/89)

24-Pin Plastic ZIP (425-mil)

Item	Millimeters	Inches
A	31.75 max	1.250 max
F	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	Ø.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	10.8 max	.425 max
N	2.8 ± 0.2	.110 $^{+.009}_{-.008}$
Q	12.07 max	.475 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020

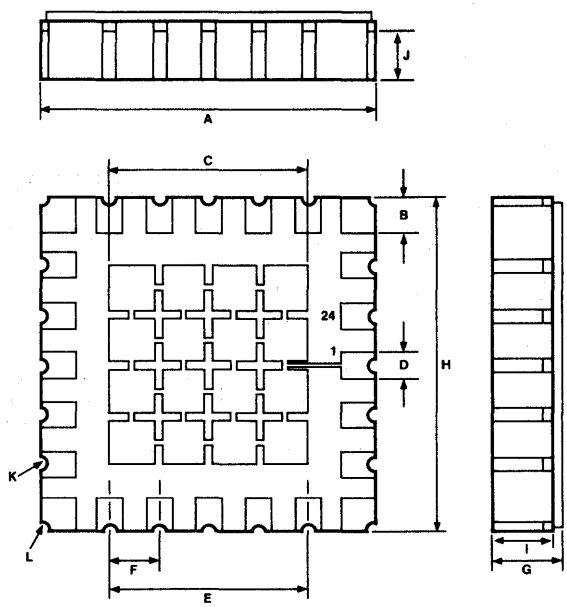


P24V-100-475A

63NR-8160B (10/91)

24-Pin Ceramic LCC

Item	Millimeters	Inches
A	8.51 ±0.4	.335 ±.016
B	.89 ±0.2	.035 ±.008
C	5.14	.202
D	.64 ±0.1	.025 $^{+.005}_{-.004}$
E	5.08	.200
F	1.27	.050
G	2.0 max	.079 max
H	8.51 ±0.4	.335 ±.016
I	1.4	.055
J	1.02	.040
K	0.2R	.008R
L	0.3R	.012R



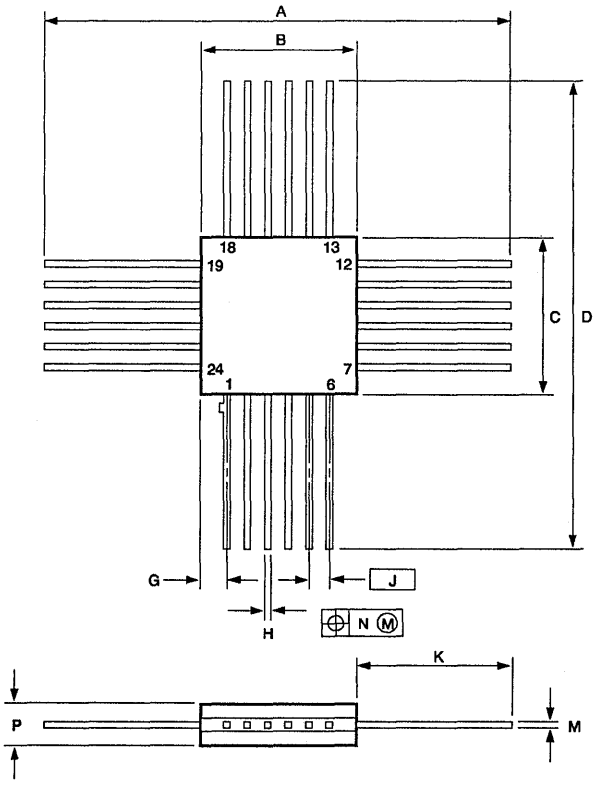
83-003582B

24-Pin Ceramic Flatpack

Item	Millimeters	Inches
A	28.5 ± 1.0	1.122 ± .040
B	9.6	.378
C	9.6	.378
D	28.5 ± 1.0	1.122 ± .040
G	1.62	.064
H	0.4 ± 0.1	$.016^{+.004}_{-.005}$
J	1.27 (TP)	.050 (TP)
K	9.45 ± 1.0	.372 ± .040
M	$0.15^{+0.10}_{-0.05}$	$.006^{+.004}_{-.002}$
N	0.25	.010
P	2.6 max	.103 max

Note:

(1) Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (TP) at maximum material condition.



X24B-127A1

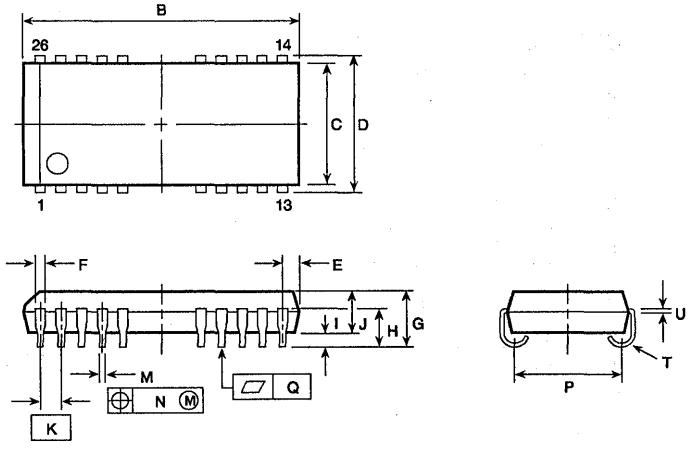
83YL-5407B

29

26/20-Pin Plastic SOJ (300-mil)

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	7.57	.298
D	8.47 ± 0.2	.333 $^{+.009}_{-.008}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	6.73 ± 0.20	.265 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



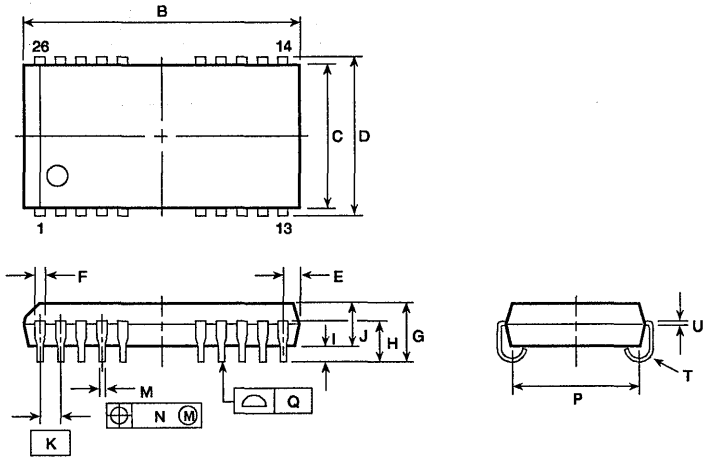
P26LA-50A

49NR-661B (9/91)

26/20-Pin Plastic SOJ (350-mil)

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	8.89	.350
D	9.78 ± 0.2	.385 ± .008
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.6 ± 0.2	.142 $^{+.008}_{-.007}$
H	2.45 ± 0.2	.096 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.7	.106
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	8.06 ± 0.20	.317 $^{+.008}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



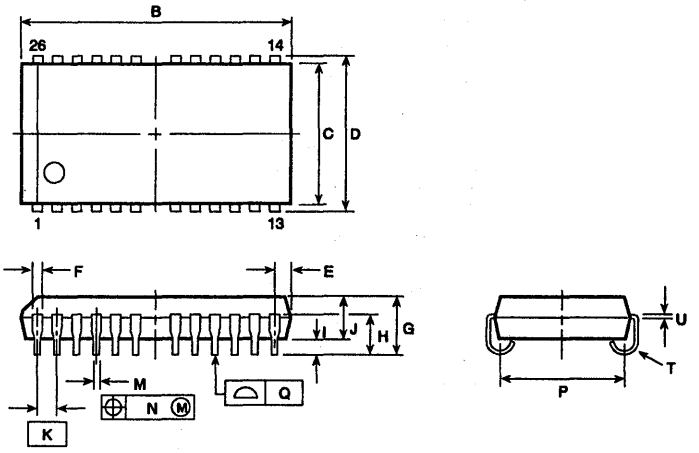
P26LB-350A

49NR-673B (9/91)

26/24-Pin Plastic SOJ (350-mil)

Item	Millimeters	Inches
B	17.4 $^{+0.2}_{-0.35}$	.685 $^{+.008}_{-.013}$
C	8.89	.350
D	9.78 ± 0.2	.385 ± .008
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.6 ± 0.2	.142 $^{+.008}_{-.007}$
H	2.45 ± 0.2	.096 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.7	.106
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	8.06 ± 0.20	.317 $^{+.008}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

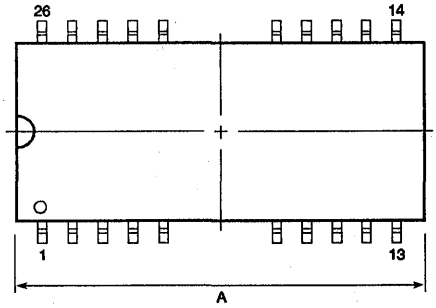


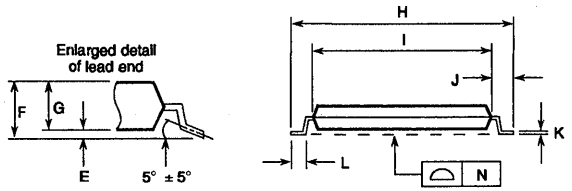
83CL-9096B (10/92)

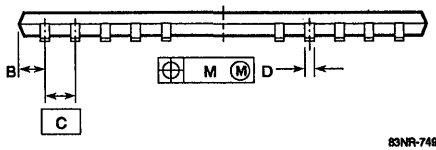
29

26/20-Pin Plastic TSOP II (300-mil)

Item	Millimeters	Inches
A	17.54 max	.691 max
B	1.18 max	.047 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.05 ± 0.05	.002 ± .002
F	1.13 max	.045 max
G	1.0	.039
H	9.22 ± 0.2	.363 ± .008
I	7.62 ± 0.1	.300 ± .004
J	0.8 ± 0.2	.031 $^{+.009}_{-.008}$
K	0.14 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
L	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
M	0.21	.009
N	0.10	.004







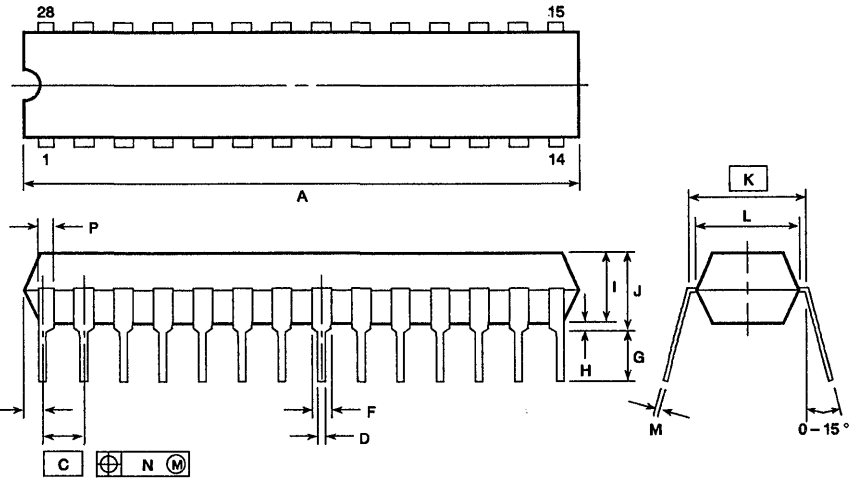
S26GS-50-9JD

83NR-7495B (9/91)

28-Pin Plastic DIP (300-mil) #1

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	6.7	.264
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



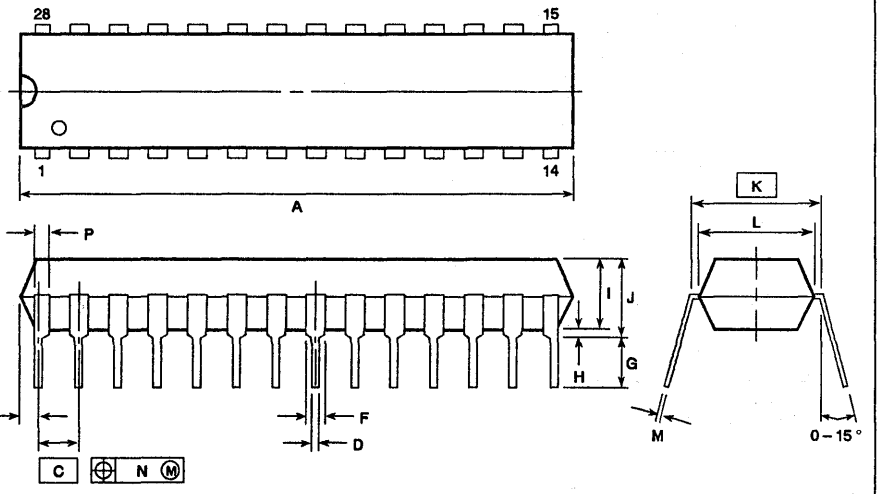
P28C-100-300SA

49NR-621B (11/86)

28-Pin Plastic DIP (300-mil) #2

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.25	.286
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.



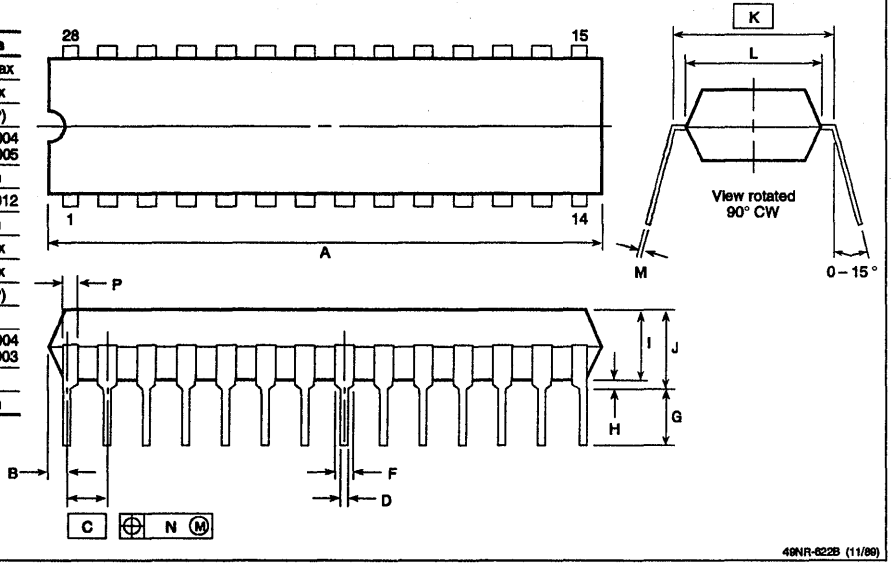
P28C-100-300WA

83NR-7521B (12/90)

28-Pin Plastic DIP (400-mil)

Item	Millimeters	Inches
A	35.56 max	1.400 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K*	10.16 (TP)	.400 (TP)
L	8.6	.339
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010
P	0.9 min	.035 min

* Item K to center of leads when formed parallel.



P28C-100-400

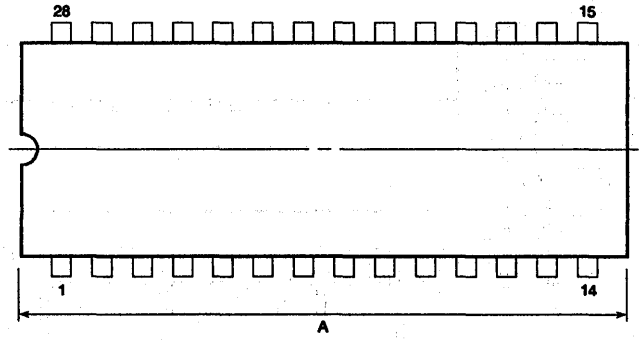
49NR-622B (11/89)

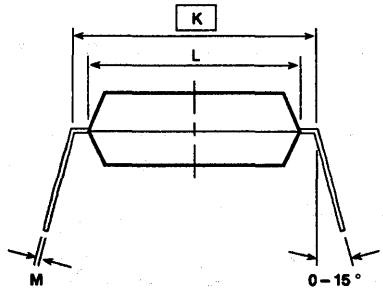
29

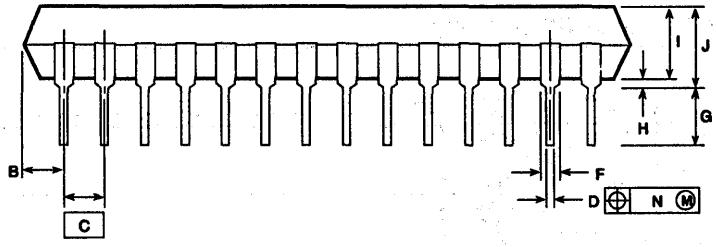
28-Pin Plastic DIP (600-mil)

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.6 ± 0.3	.142 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K*	15.24 (TP)	.600 (TP)
L	13.2	.520
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.010

* Item K to center of leads when formed parallel.







P28C-100-600A1

49NR-614B (6/91)

28-Pin Cerdip (400-mil) #1

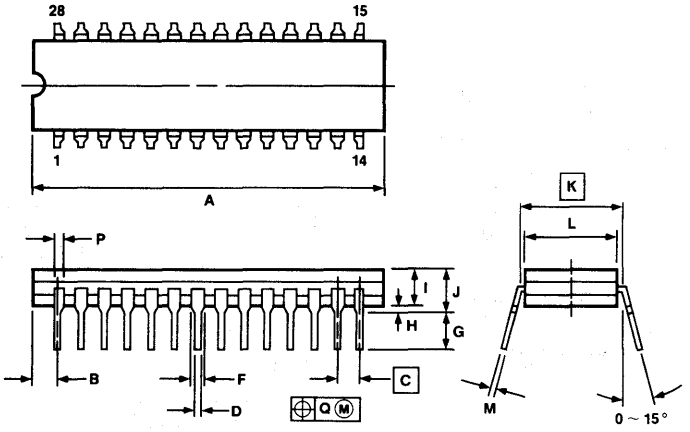
Item	Millimeters	Inches
A	38.10 max	1.50 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020^{+.004}_{-.005}$
F	1.20 min	.047 min
G	3.50 ± 0.30	.138 ± .012
H	0.51 min	.020 min
I	4.00	.157
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	9.65	.380
M	0.25 ± 0.05	$.010^{+.002}_{-.003}$
P	0.89 min	.035 min
Q	0.25	.010

Notes:

[1] Each lead centerline is located within 0.25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.

P28DH-100-400A

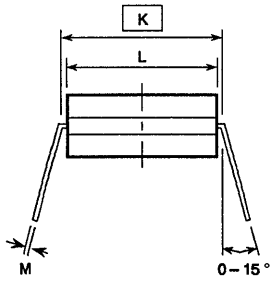


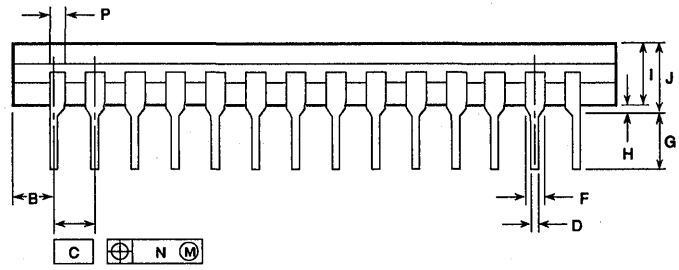
83-005015B

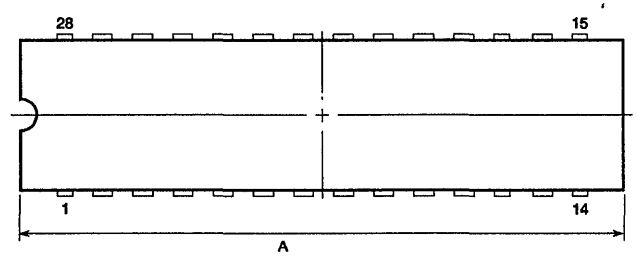
28-Pin Cerdip (400-mil) #2

Item	Millimeters	Inches
A	38.10 max	1.500 max
B	2.54 max	.100 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.20 min	.047 min
G	3.5 ± 0.3	.138 ± .012
H	0.51 min	.020 min
I	4.00	.157
J	5.08 max	.200 max
K*	10.16 (TP)	.400 (TP)
L	9.65	.380
M	0.25 ± 0.05	.010 $^{+.002}_{-.003}$
N	0.25	.010
P	0.89 min	.035 min

* Item K to center of leads when formed parallel.





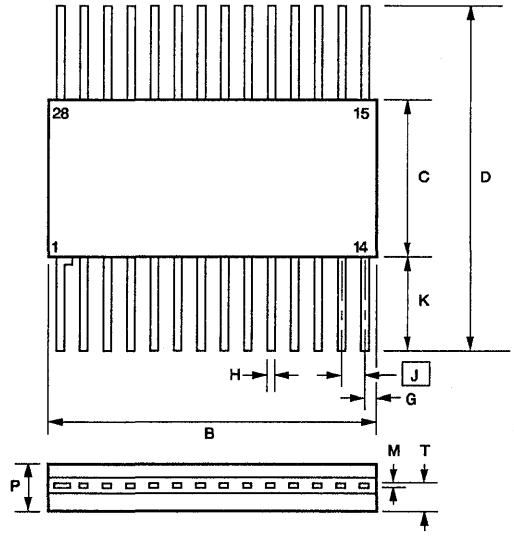


P28DH-100-400A

83CL-6863B (7/92)

28-Pin Ceramic Flatpack

Item	Millimeters	Inches
B	17.5	.689
C	9.84	.387
D	29.0	1.142
G	0.50	.020
H	0.43	.017
J	1.27 [TP]	.050 [TP]
K	9.58	.377
M	0.15	.006
P	2.18 max	.086 max
T	1.14 max	.045 max



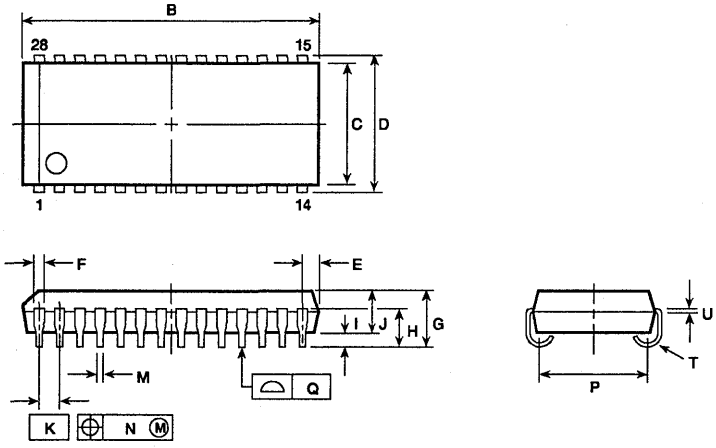
X28B-100A

83IH-4610B (5/89)

28-Pin Plastic SOJ (300-mil)

Item	Millimeters	Inches
B	18.67 $^{+0.2}_{-0.35}$	.735 $^{+.008}_{-.014}$
C	7.57	.298
D	8.47 ± 0.2	.333 $^{+.009}_{-.008}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.74	.029
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.55	.100
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	6.73 ± 0.20	.265 ± .008
Q	0.1	.004
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



P28LA-300A

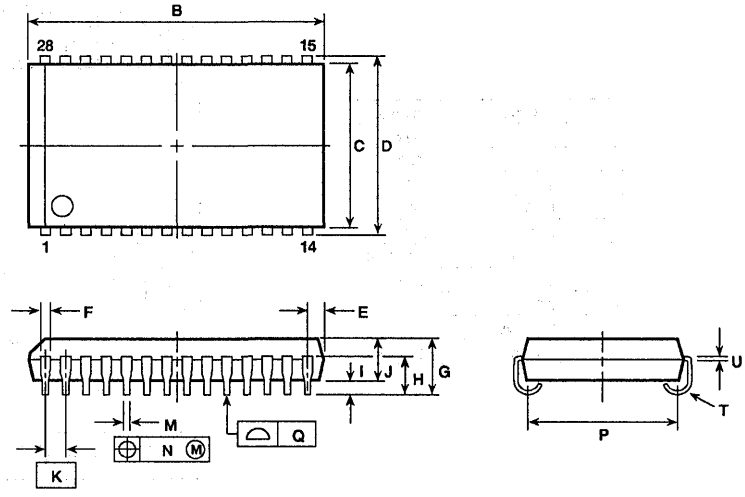
83NR-7520B (12/90)

29

28-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	18.67 $^{+0.20}_{-0.35}$	.735 $^{+.008}_{-.013}$
C	10.16	.400
D	11.18 ± 0.20	.440 $^{+.006}_{-.007}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.6	.024
G	3.5 ± 0.2	.138 $^{+.006}_{-.007}$
H	2.4 ± 0.2	.094 $^{+.006}_{-.007}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	9.40 ± 0.20	.370 $^{+.006}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



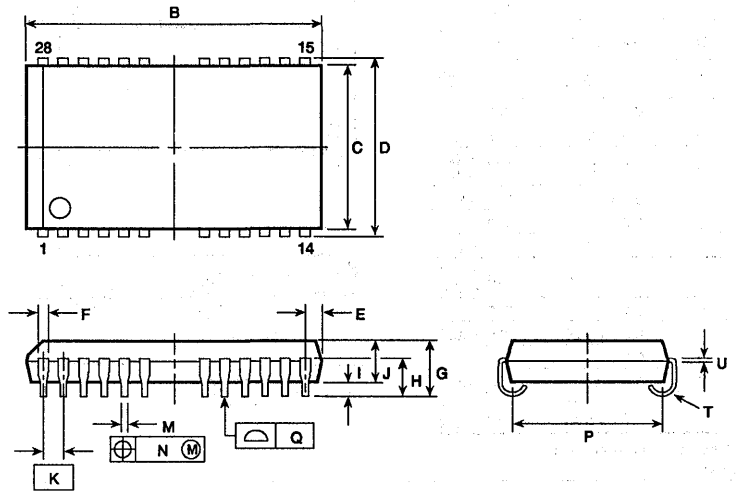
P28LA-400A-1

49NR-690B (1/92)

28/24-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	18.67 $^{+0.20}_{-0.35}$	.735 $^{+.008}_{-.013}$
C	10.16	.400
D	11.18 ± 0.20	.440 $^{+.006}_{-.007}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.7	.028
G	3.5 ± 0.2	.138 $^{+.006}_{-.007}$
H	2.4 ± 0.2	.094 $^{+.006}_{-.007}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	9.40 ± 0.20	.370 $^{+.006}_{-.007}$
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

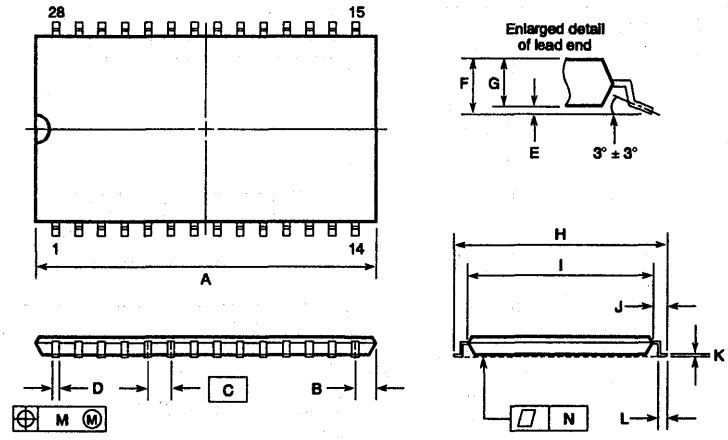


P28LB-400A1

83NR-8159B (4/92)

28-Pin Plastic TSOP II (400-mil)

Item	Millimeters	Inches
A	18.81 max	.741 max
B	1.15 max	.046 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.044 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.14^{+0.10}_{-0.05}$	$.006^{+.004}_{-.003}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$
M	0.21	.009
N	0.10	.004

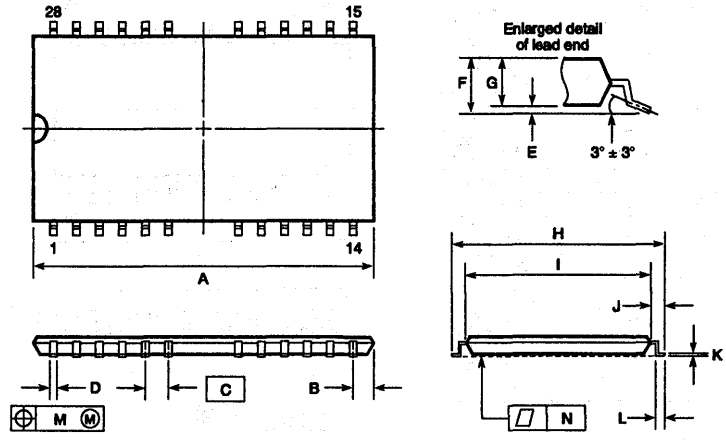


S28G5-50-7JD

83RD-8340B (1/92)

28/24-Pin Plastic TSOP II (400-mil)

Item	Millimeters	Inches
A	18.81 max	.741 max
B	1.15 max	.045 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.2	.400 ± .008
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	.020 ± .004
M	0.21	.008
N	0.10	.004

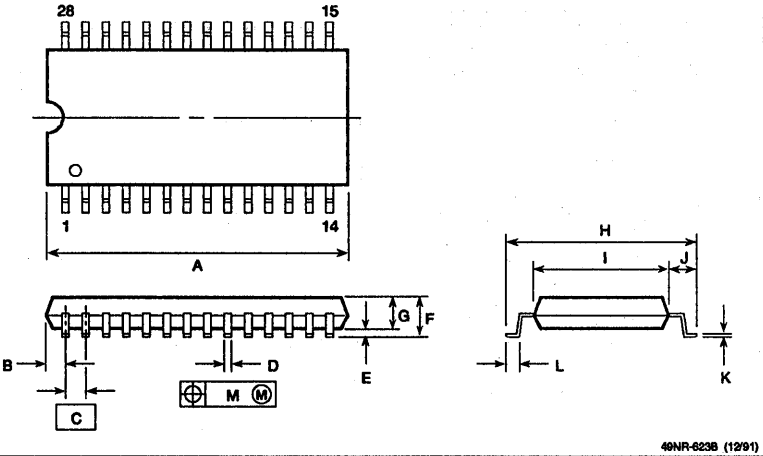


S28G5-50-7JD1

83RD-8157B (10/91)

28-Pin Plastic SOP (Miniflat) (450-mil) #1

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.1 $^{+0.2}_{-0.1}$	.004 $^{+.008}_{-.004}$
F	2.5 max	.099 max
G	2.00	.079
H	11.8 ± 0.3	.465 $^{+.012}_{-.013}$
I	8.4	.331
J	1.7	.067
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.7 ± 0.2	.028 $^{+.008}_{-.009}$
M	0.12	.005

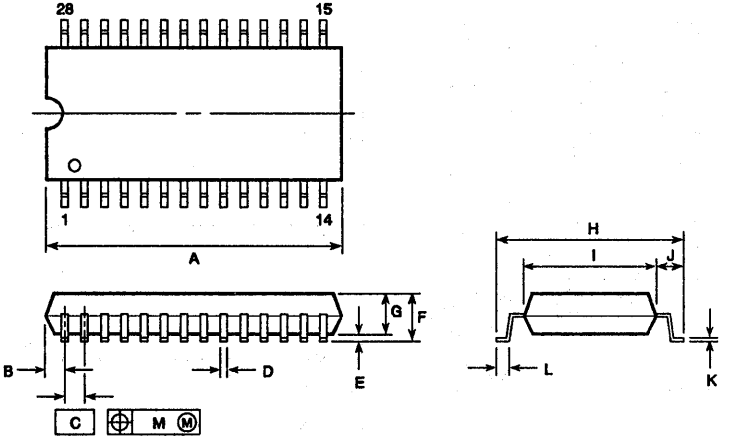


P28GM-50-450A1

49NR-623B (12/91)

28-Pin Plastic SOP (Miniflat) (450-mil) #2

Item	Millimeters	Inches
A	19.05 max	.750 max
B	1.27 max	.050 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
E	0.1 ± 0.1	.004 $^{+.005}_{-.004}$
F	3.0 max	.119 max
G	2.55	.100
H	11.8 ± 0.3	.465 $^{+.012}_{-.013}$
I	8.4	.331
J	1.7	.067
K	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.002}$
L	0.7 ± 0.2	.028 $^{+.008}_{-.009}$
M	0.12	.005

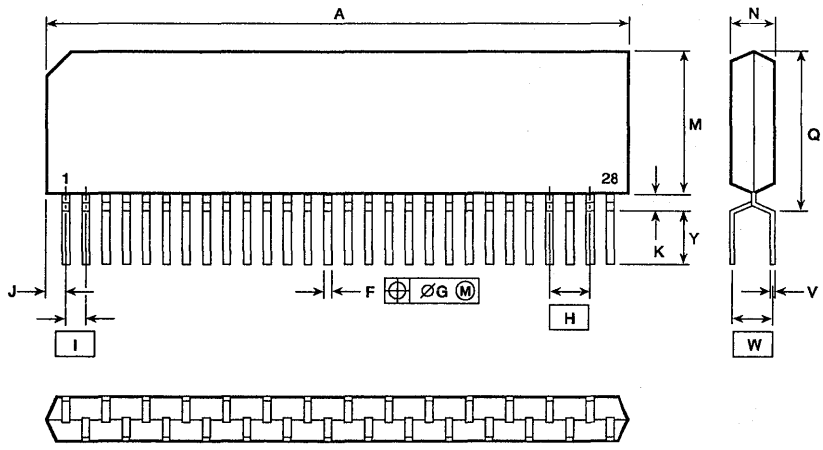


P28GM-50-450A2

49NR-635B (11/89)

28-Pin Plastic ZIP (350-mil)

Item	Millimeters	Inches
A	36.83 max	1.450 max
F	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
G	Ø0.25	.010
H	2.54	.100
I	1.27	.050
J	1.27 max	.050 max
K	1.0 min	.039 min
M	8.9 max	.350 max
N	2.8 ± 0.2	.110 $^{+.009}_{-.008}$
Q	10.16 max	.400 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
W	2.54	.100
Y	3.3 ± 0.5	.130 ± .020



P28V-254-400A

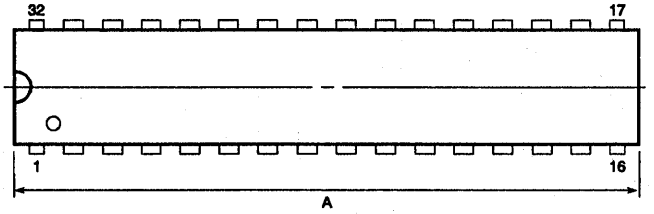
49NR-702B (4/92)

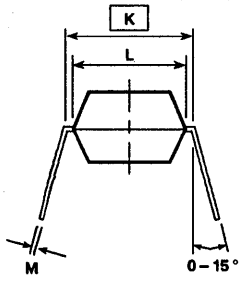
29

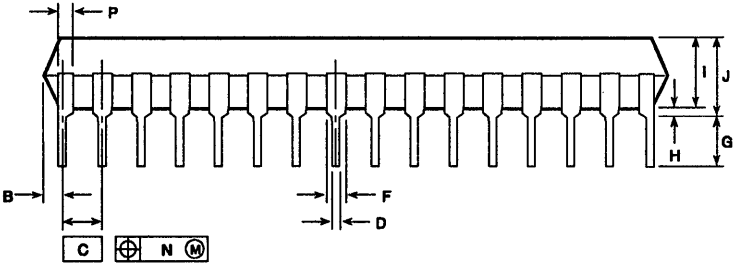
32-Pin Plastic DIP (300-mil)

Item	Millimeters	Inches
A	40.64 max	1.600 max
B	1.27 max	.050 max
C	2.54 (TP)	.100 (TP)
D	0.50 ± 0.10	.020 $^{+.004}_{-.005}$
F	1.2 min	.047 min
G	3.2 ± 0.3	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K*	7.62 (TP)	.300 (TP)
L	7.25	.285
M	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.003}$
N	0.25	.01
P	1.0 min	.039 min

* Item K to center of leads when formed parallel.





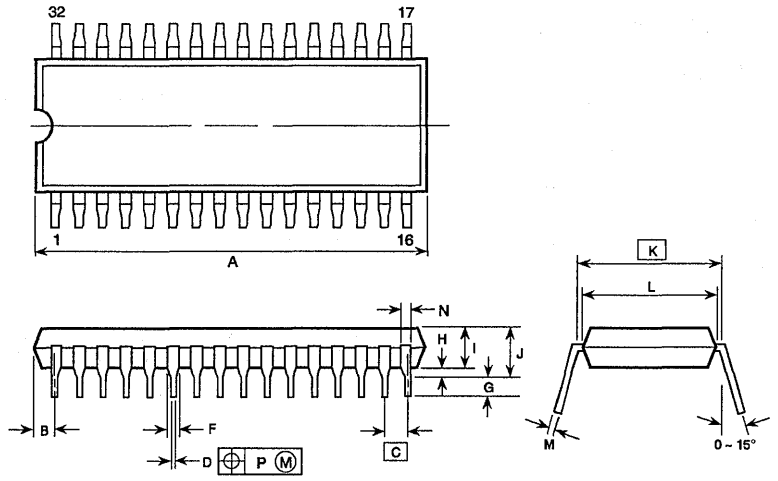


P32C-100-300WA

83NR-7543B (1/91)

32-Pin Plastic DIP (600-mil)

Item	Millimeters	Inches
A	40.64 max	1.60 max
B	1.27 max	.050 max
C	2.54 [TP]	.100 [TP]
D	0.50 ± 0.10	$.020^{+.004}_{-.005}$
F	1.1 min	.043 min
G	3.2 ± 0.30	.126 ± .012
H	0.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	$0.25^{+0.10}_{-0.05}$	$.010^{+.004}_{-.003}$
N	0.9 min	.035 min
P	0.25	.010

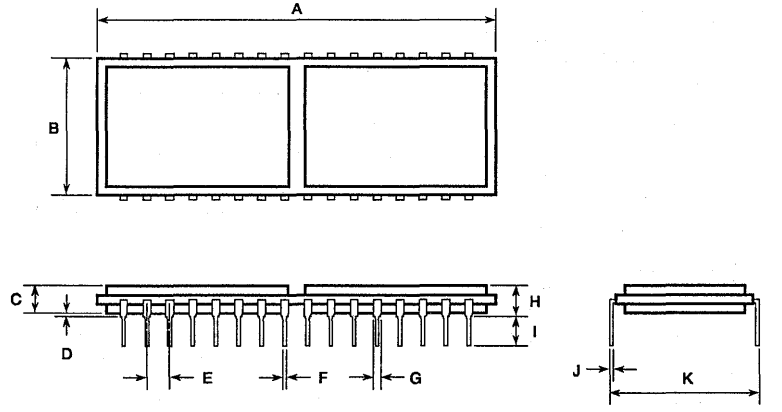


P32C-100-600A

83IH-5818B (9/89)

32-Pin Ceramic DIP (600-mil)

Item	Millimeters	Inches
A	43.053 ± .127	1.7 ± 0.01
B	14.99 ± .254	.59 ± 0.10
C	9.78 max	.385 max
D	0.254 ± .127	.010 ± .005
E	2.54 [TP]	.100 [TP]
F	0.508 ± .127	.02 ± .005
G	1.27 ± .381	.05 ± .015
H	10.287 max	.405 max
I	3.81 ± .635	.15 ± .025
J	0.254 ± .076	.01 ± .003
K	15.37 ± .381	.605 ± .015

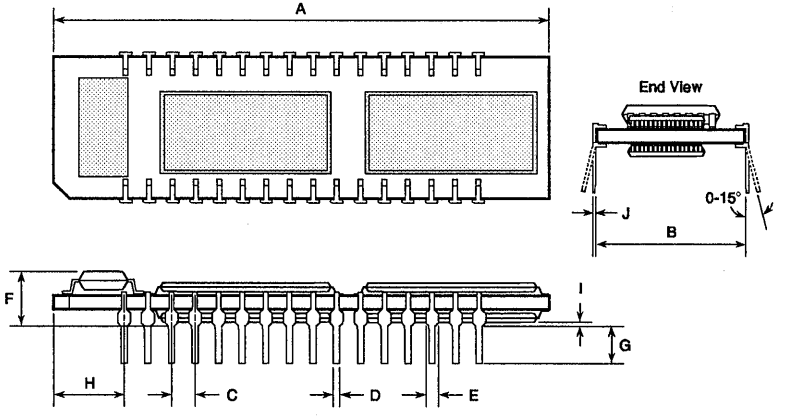


83FM-8966B (8/92)

29

32-Pin Plastic (FR-4) DIP (600-mil)

Item	Millimeters	Inches
A	53.47 ± 0.13	2.105 ± .005
B	15.24	.600
C	2.54 [TP]	.100 [TP]
D	0.47 ± 0.12	.019 ± .005
E	1.02	.040
F	5.84 max	.230 max
G	2.54 min	.100 min
H	7.62	.300
I	0.38 min	.015 min
J	0.28 ± 0.08	.011 ± .003

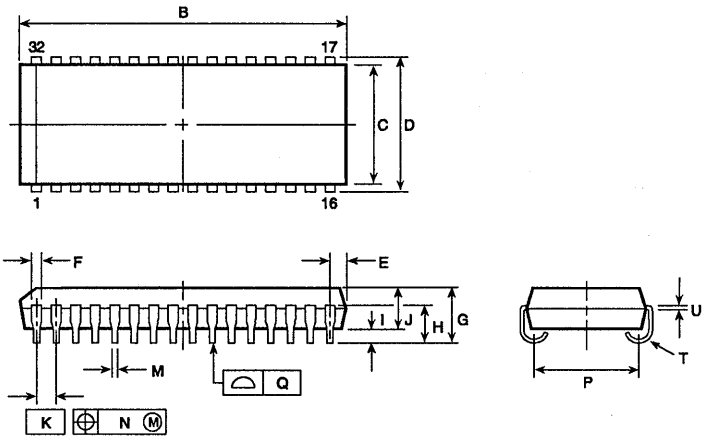


83FM-8966B (8/92)

32-Pin Plastic SOJ (300-mil)

Item	Millimeters	Inches
B	21.21 $^{+0.3}_{-0.35}$	.835 $^{+.009}_{-.014}$
C	7.57	.298
D	8.47 ± 0.2	.333 $^{+.009}_{-.008}$
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.74	.029
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.009}_{-.008}$
I	0.8 min	.031 min
J	2.55	.100
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P *	6.73 ± 0.20	.265 ± .008
Q	0.1	.004
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



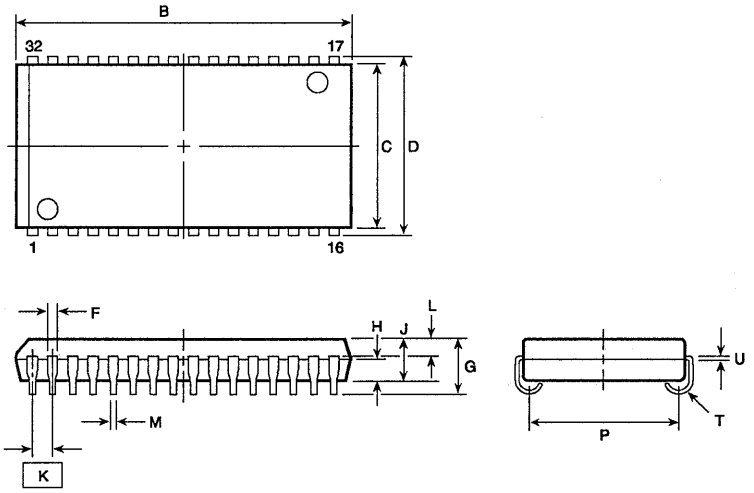
P32LA-300A

83NR-7544B (1/91)

32-Pin Plastic SOJ (400-mil) #1

Item	Millimeters	Inches
B	21.01 ± 0.15	.827 ± .006
C	10.16 ± 0.05	.400 ± .002
D	11.18 ± 0.10	.440 ± .004
F	0.74 ± 0.10	.029 ± .004
G	3.5 ± 0.10	.138 ± .004
H	1.445 ± 0.025	.057 ± .001
J	2.6	.102
K	1.27 (TP)	.050 (TP)
L	0.955 ± 0.025	.038 ± .001
M	0.40 ± 0.05	.016 ± .002
P*	9.40 ± 0.15	.370 ± .006
T	0.85 ± 0.10 rad	.033 ± .004 rad
U	0.22 ± 0.05	.009 ± .002

* Item P to center of leads.

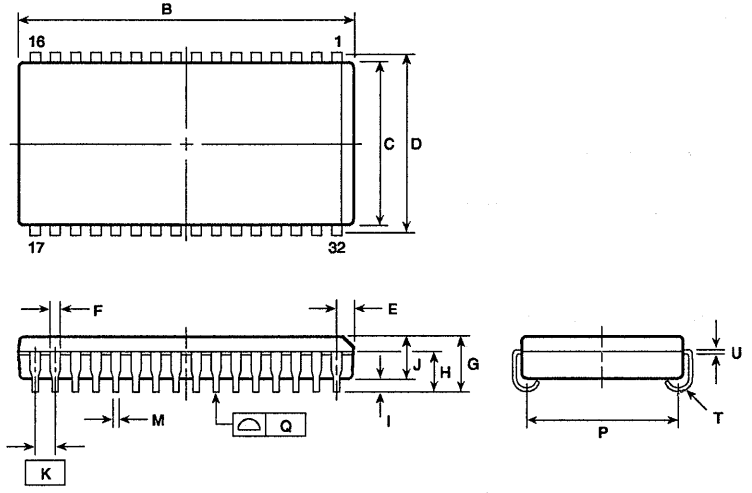


83YL-8647B (6/92)

32-Pin Plastic SOJ (400-mil) #2

Item	Millimeters	Inches
B	21.21 $^{+0.20}_{-0.35}$	.835 $^{+.008}_{-.014}$
C	10.16	.400
D	11.18 ± 0.20	.440 ± .008
E	1.08 ± 0.15	.043 ± .006
F	0.6	.024
G	3.5	.138
H	2.545 ± 0.2	.100 ± .008
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 ± .004
P*	9.40 ± 0.20	.370 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

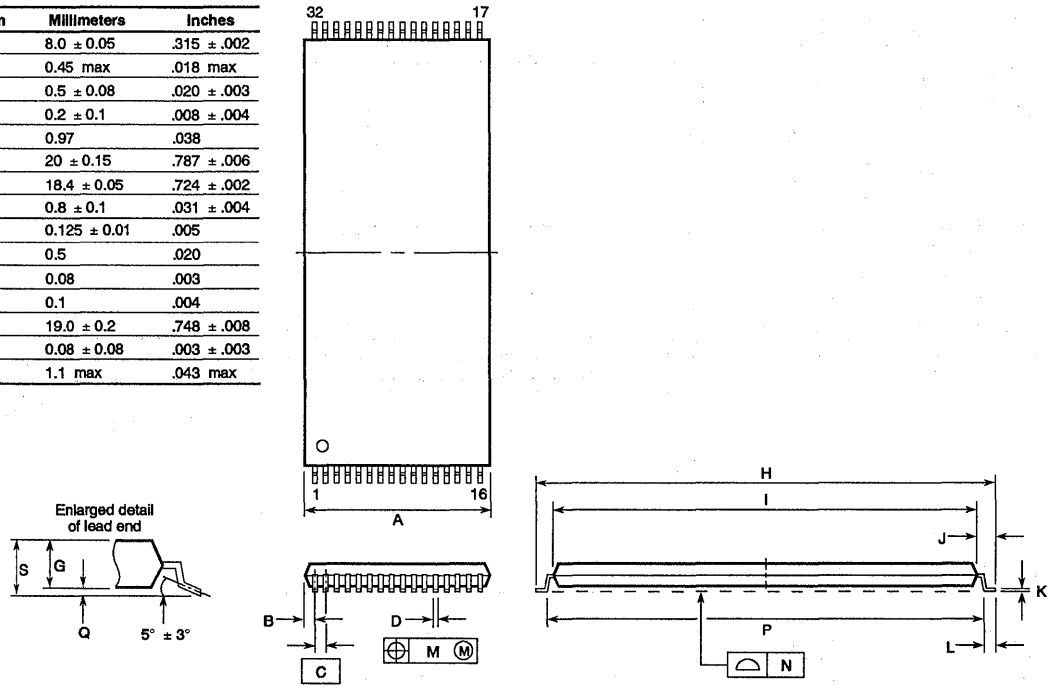


83YL-9023B (9/92)

29

32-Pin Plastic TSOP I #1

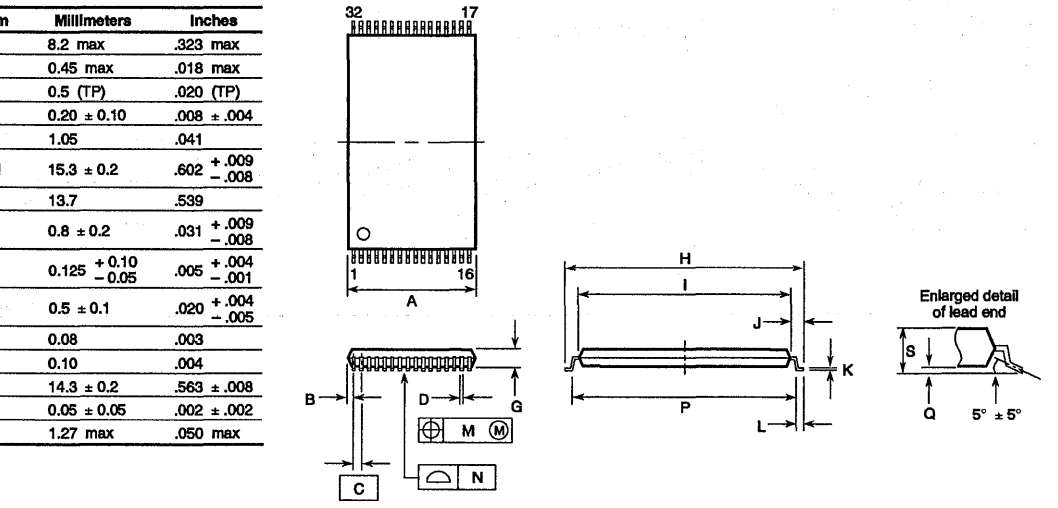
Item	Millimeters	Inches
A	8.0 ± 0.05	.315 ± .002
B	0.45 max	.018 max
C	0.5 ± 0.08	.020 ± .003
D	0.2 ± 0.1	.008 ± .004
G	0.97	.038
H	20 ± 0.15	.787 ± .006
I	18.4 ± 0.05	.724 ± .002
J	0.8 ± 0.1	.031 ± .004
K	0.125 ± 0.01	.005
L	0.5	.020
M	0.08	.003
N	0.1	.004
P	19.0 ± 0.2	.748 ± .008
Q	0.08 ± 0.08	.003 ± .003
S	1.1 max	.043 max



49NR-737B (11/91)

32-pin Plastic TSOP I #2

Item	Millimeters	Inches
A	8.2 max	.323 max
B	0.45 max	.018 max
C	0.5 (TP)	.020 (TP)
D	0.20 ± 0.10	.008 ± .004
G	1.05	.041
H	15.3 ± 0.2	.602 $^{+.009}_{-.008}$
I	13.7	.539
J	0.8 ± 0.2	.031 $^{+.009}_{-.008}$
K	0.125 $^{+0.10}_{-0.05}$	.005 $^{+.004}_{-.001}$
L	0.5 ± 0.1	.020 $^{+.004}_{-.005}$
M	0.08	.003
N	0.10	.004
P	14.3 ± 0.2	.563 ± .008
Q	0.05 ± 0.05	.002 ± .002
S	1.27 max	.050 max

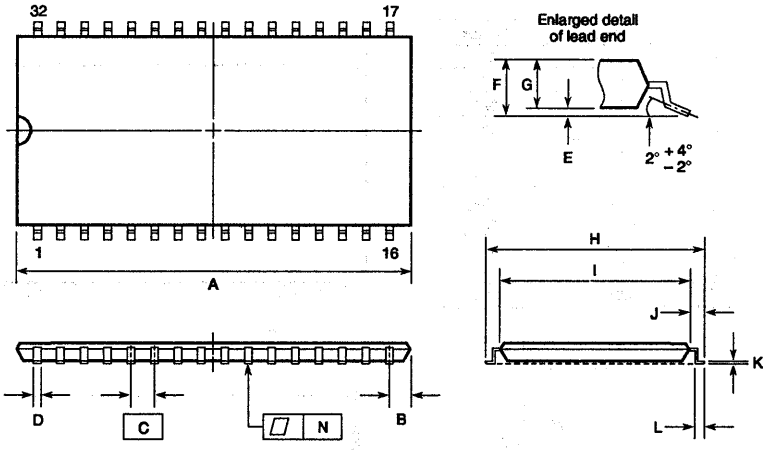


S32GX-50-EJA

49NR-601B (11/91)

32-Pin Plastic TSOP II (400-mil)

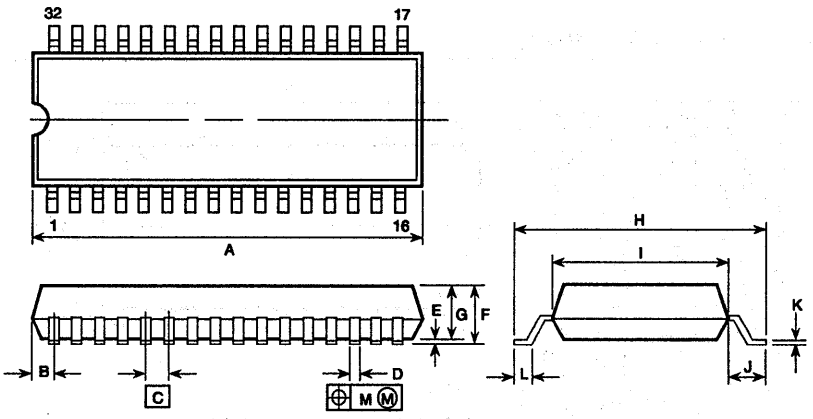
Item	Millimeters	Inches
A	21.16 max	.833 max
B	1.06 max	.042 max
C	1.27 (TP)	.050 (TP)
D	0.40 ± 0.10	.016 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$
N	0.10	.004



83YL-9026B (9/92)

32-Pin Plastic SOP (Miniflat) (525-mil)

Item	Millimeters	Inches
A	20.61 max	.812 max
B	0.78 max	.031 max
C	1.27 [TP]	.050 [TP]
D	$0.40^{+0.10}_{-0.05}$	$.016^{+.004}_{-.003}$
E	0.05 ±0.05	.002 ±.002
F	2.85 max	.113 max
G	2.7	.106
H	14.1 ±0.3	.555 ±.012
I	11.3	.445
J	1.4	.055
K	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$
L	0.8 ±0.2	$.031^{+.009}_{-.008}$
M	0.12	.005



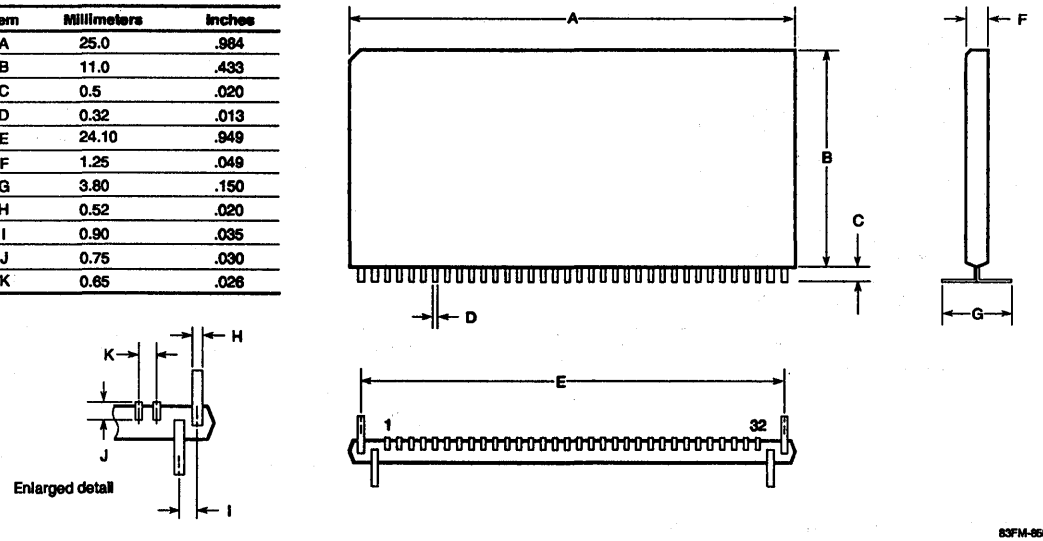
S32GM-50-525A-1

83IH-6227B (10/90)

29

32-Pin Surface Vertical Package (SVP)

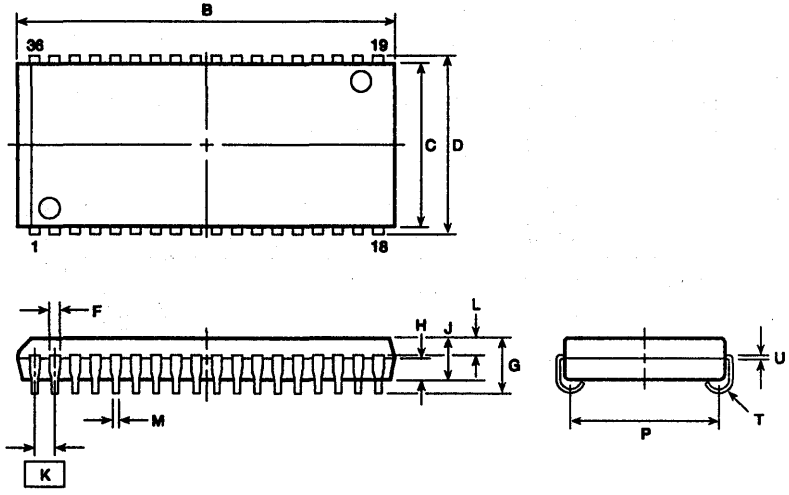
Item	Millimeters	Inches
A	25.0	.984
B	11.0	.433
C	0.5	.020
D	0.32	.013
E	24.10	.949
F	1.25	.049
G	3.80	.150
H	0.52	.020
I	0.90	.035
J	0.75	.030
K	0.65	.026



36-Pin Plastic SOJ (400-mil)

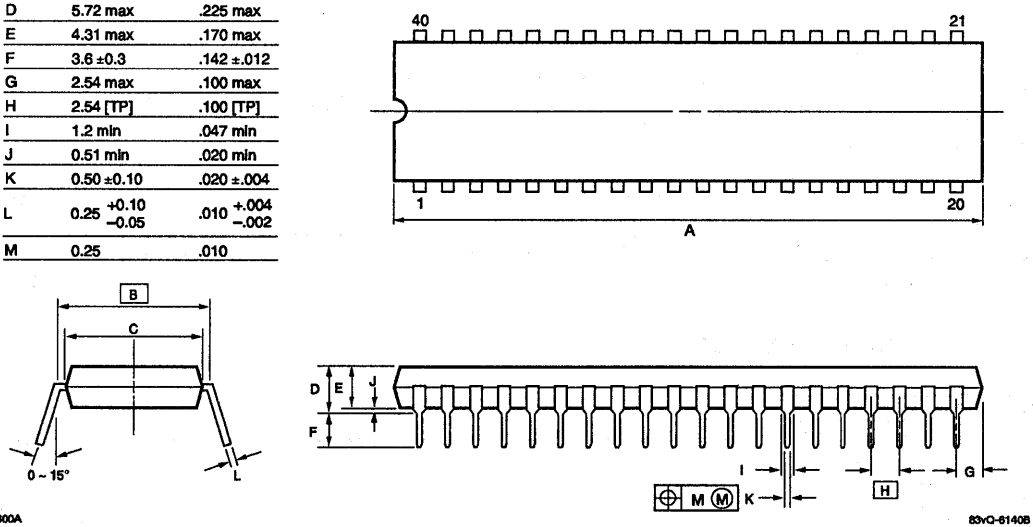
Item	Millimeters	Inches
B	23.55 ± 0.15	.927 ± .006
C	10.16 ± 0.05	.400 ± .002
D	11.18 ± 0.10	.440 ± .004
F	0.74 ± 0.10	.029 ± .004
G	3.5 ± 0.10	.138 ± .004
H	1.445 ± 0.025	.057 ± .001
J	2.6	.102
K	1.27 (TP)	.05 (TP)
L	0.955 ± 0.025	.0376 ± .001
M	0.40 ± 0.05	.0157 ± .002
P*	9.40 ± 0.15	.37 ± .006
T	0.85 ± 0.10 rad	.033 ± .004 rad
U	0.22 ± 0.05	.009 ± .002

* Item P to center of leads.



40-Pin Plastic DIP (600-mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	15.24 [TP]	.600 [TP]
C	13.2	.520
D	5.72 max	.225 max
E	4.31 max	.170 max
F	3.6 ±0.3	.142 ±.012
G	2.54 max	.100 max
H	2.54 [TP]	.100 [TP]
I	1.2 min	.047 min
J	0.51 min	.020 min
K	0.50 ±0.10	.020 ±.004
L	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.002}$
M	0.25	.010



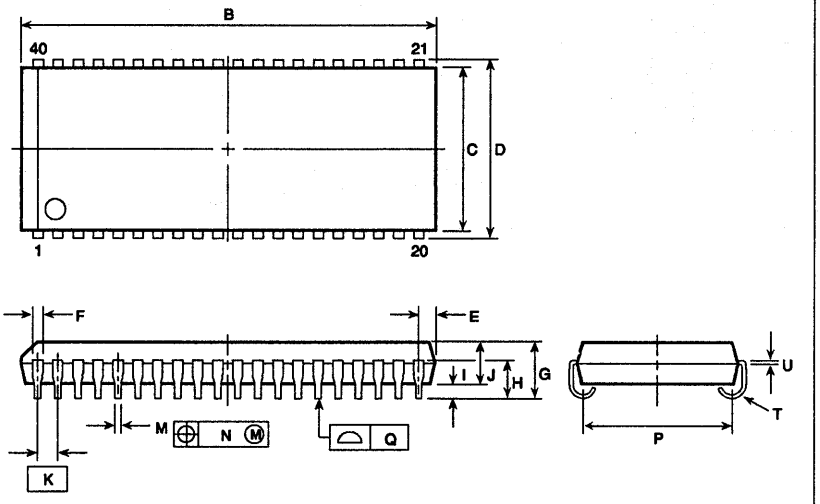
P40C-100-600A

83vQ-6140B (6/89)

40-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	26.29 $^{+.02}_{-.035}$	1.035 $^{+.008}_{-.014}$
C	10.16	.400
D	11.18 ± 0.2	.440 ± .008
E	1.08 ± 0.15	.043 $^{+.006}_{-.007}$
F	0.7	.028
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 $^{+.007}_{-.008}$
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
N	0.12	.005
P*	9.40 ± 0.20	.370 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.



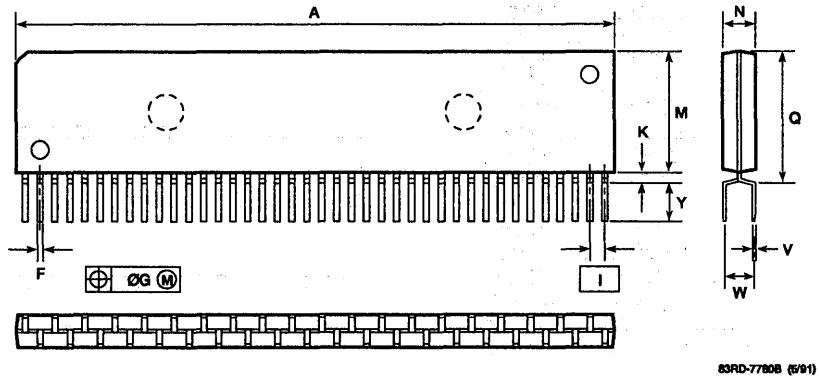
P40LE-400A

49NR-700B (7/91)

29

40-Pin Plastic ZIP (400-mil)

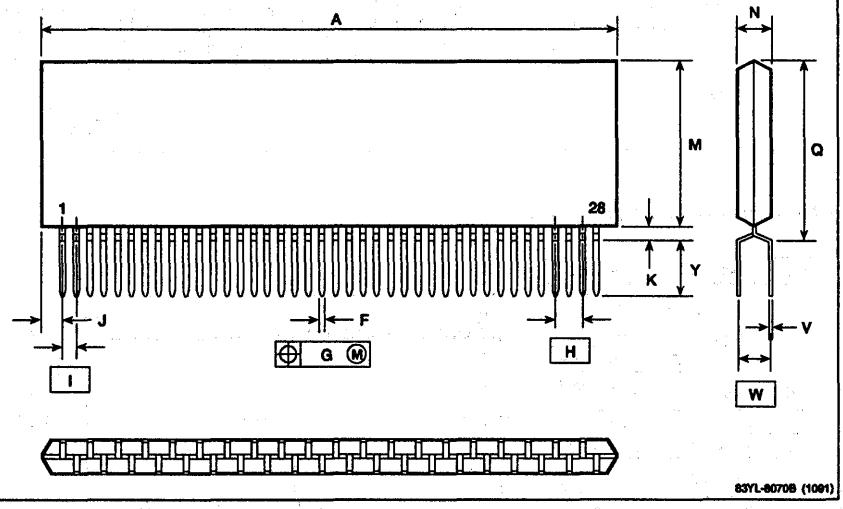
Item	Millimeters	Inches
A	50.98 $^{+0.05}_{-0.35}$	2.007 $^{+0.002}_{-0.014}$
F	14.0 ± 0.2	0.20 ± 0.002
G	Ø0.25	Ø0.010
I	1.27 ± 0.1	0.050 ± 0.004
K	0.9 min	0.035 min
M	10.29 ± 0.05	0.405 ± 0.002
N	2.8 ± 0.05	0.110 ± 0.002
Q	11.5 ± 0.15	0.453 ± 0.006
V	.25 $^{+0.1}_{-0.05}$	0.010 $^{+0.004}_{-0.002}$
W	2.50 ± 0.1	0.098 ± .004
Y	3.25 ± 0.15	0.128 ± .006



83RD-7780B (5/91)

40-Pin Plastic Shrink ZIP (450-mil)

Item	Millimeters	Inches
A	36.83 max	1.450 max
F	0.4 ± 0.1	.016 ± .004
G	0.2	.008
H	1.778	.070
I	0.889	.035
J	1.016	.040
K	1.0 min	.039 min
M	10.50 max	.413 max
N	2.2 ± 0.2	.087 ± .008
Q	11.70 max	.461 max
V	0.25 $^{+0.10}_{-0.05}$	.010 $^{+.004}_{-.002}$
W	1.778	.070
Y	3.108	.122

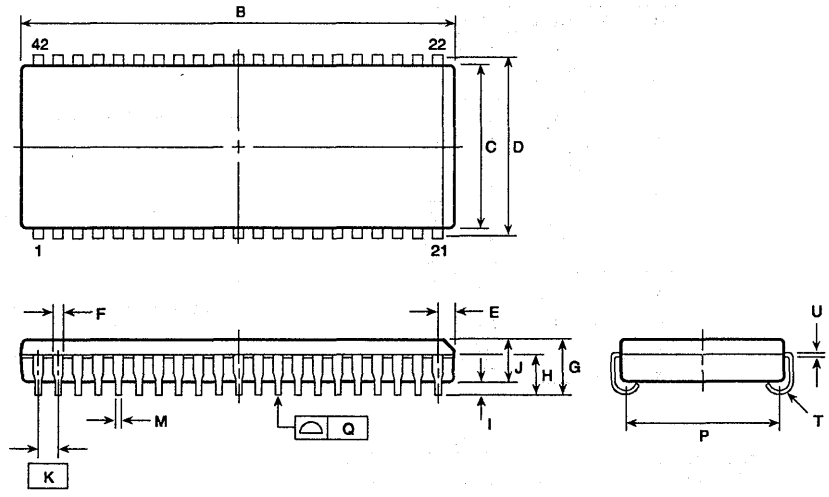


83YL-8070B (1091)

42-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	27.41 $^{+0.20}_{-0.35}$	1.08 $^{+.008}_{-.014}$
C	10.16	.400
D	11.18 ± 0.20	.440 ± .008
E	1.08 ± 0.15	.043 ± .006
F	0.6	.024
G	3.5 ± 0.20	.138 ± .008
H	2.545 ± 0.2	.100 ± .008
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 ± .004
P*	9.40 ± 0.20	.370 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

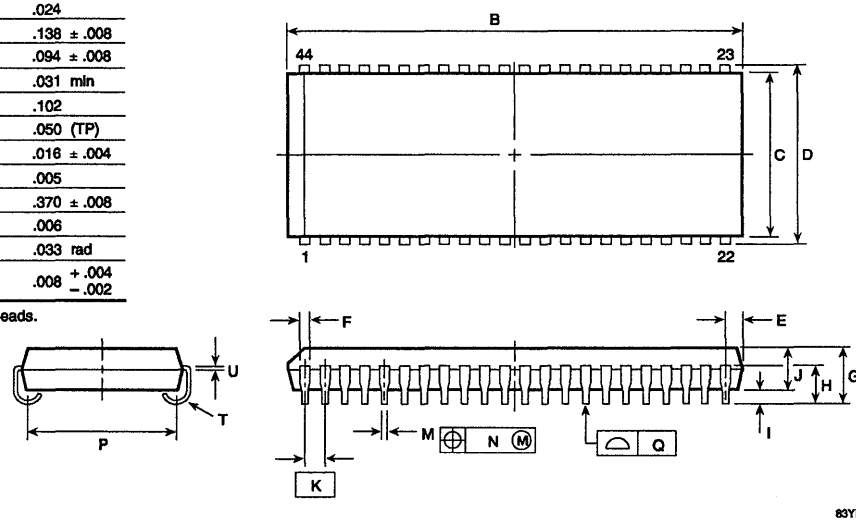


83YL-9024B (9/92)

44-Pin Plastic SOJ (400-mil)

Item	Millimeters	Inches
B	28.83 $^{+0.20}_{-0.35}$	1.135 $^{+.008}_{-.014}$
C	10.16	.400
D	11.18 ± 0.2	.440 ± .008
E	1.08 ± 0.15	.043 ± .006
F	0.6	.024
G	3.5 ± 0.2	.138 ± .008
H	2.4 ± 0.2	.094 ± .008
I	0.8 min	.031 min
J	2.6	.102
K	1.27 (TP)	.050 (TP)
M	0.40 ± 0.10	.016 ± .004
N	0.12	.005
P*	9.40 ± 0.20	.370 ± .008
Q	0.15	.006
T	0.85 rad	.033 rad
U	0.20 $^{+0.10}_{-0.05}$	.008 $^{+.004}_{-.002}$

* Item P to center of leads.

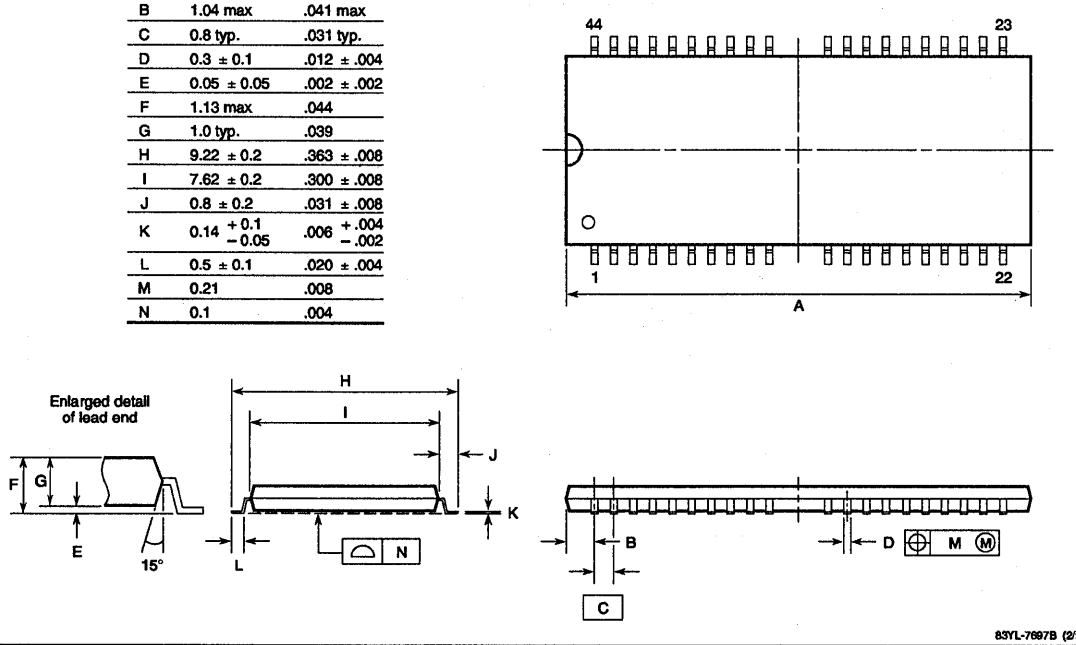


83YL-8649B (5/92)

29

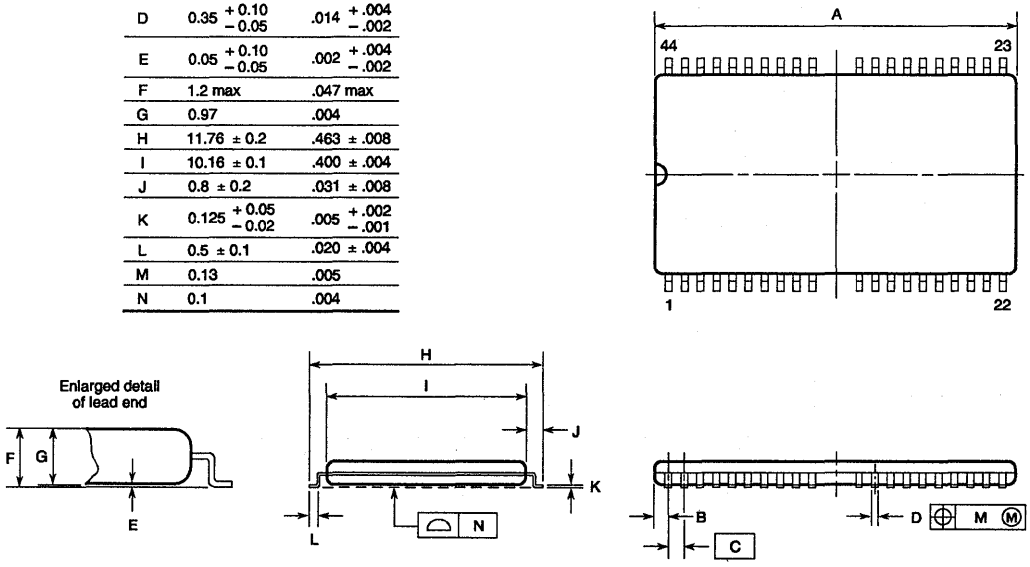
44/40-Pin Plastic TSOP II (300-mil)

Item	Millimeters	Inches
A	18.81 max	.741 max
B	1.04 max	.041 max
C	0.8 typ.	.031 typ.
D	0.3 ± 0.1	.012 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.13 max	.044
G	1.0 typ.	.039
H	9.22 ± 0.2	.363 ± .008
I	7.62 ± 0.2	.300 ± .008
J	0.8 ± 0.2	.031 ± .008
K	$0.14^{+0.1}_{-0.05}$	$.006^{+.004}_{-.002}$
L	0.5 ± 0.1	.020 ± .004
M	0.21	.008
N	0.1	.004



44-Pin Plastic TSOP II (400-mil) #1

Item	Millimeters	Inches
A	18.41 ± 0.1	.725 ± .004
B	1.0 max	.039 max
C	0.8 ± 0.1	.031 ± .004
D	$0.35^{+0.10}_{-0.05}$	$.014^{+.004}_{-.002}$
E	$0.05^{+0.10}_{-0.05}$	$.002^{+.004}_{-.002}$
F	1.2 max	.047 max
G	0.97	.004
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.05}_{-0.02}$	$.005^{+.002}_{-.001}$
L	0.5 ± 0.1	.020 ± .004
M	0.13	.005
N	0.1	.004

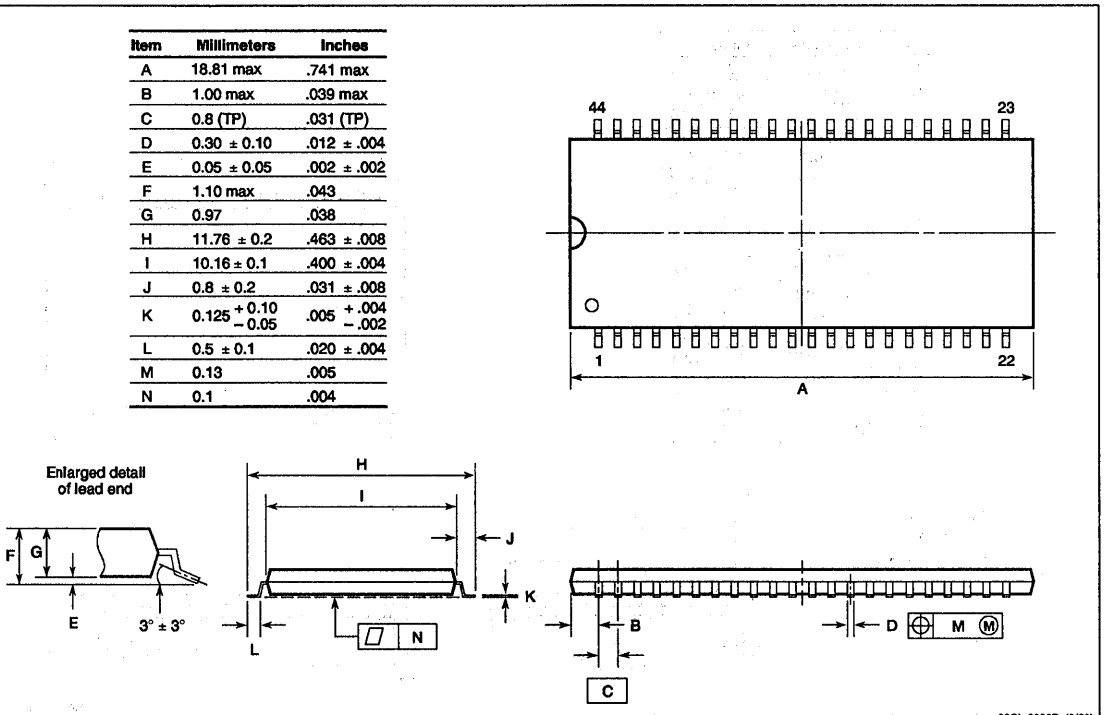


83YL-8069B (10/91)

29

44-Pin Plastic TSOP II (400-mil) #2

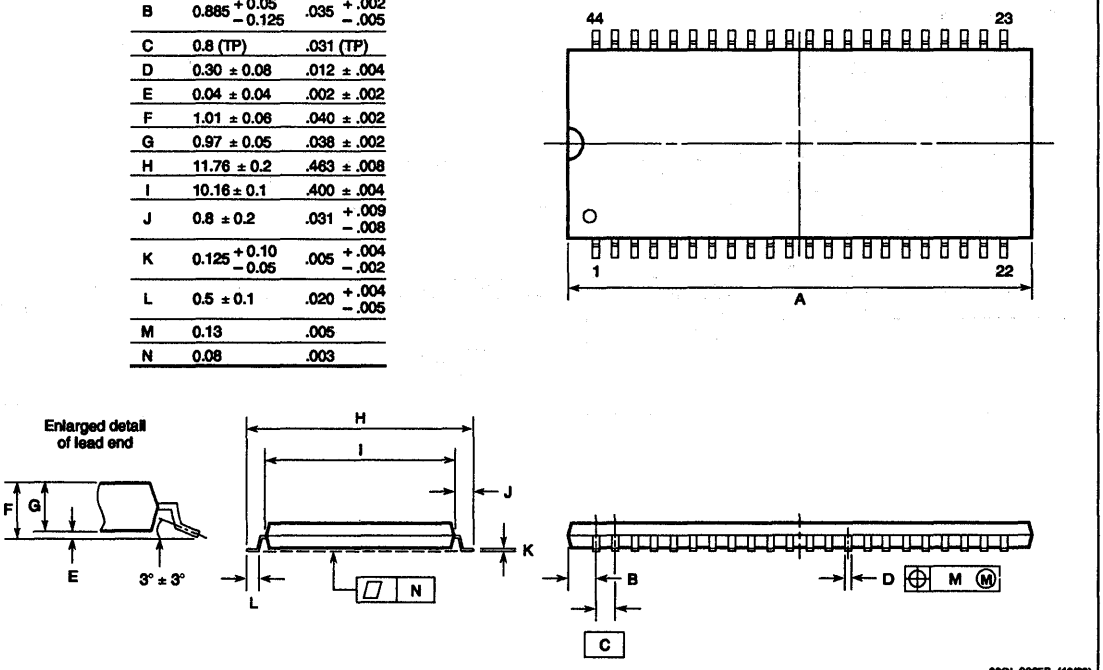
Item	Millimeters	Inches
A	18.81 max	.741 max
B	1.00 max	.039 max
C	0.8 (TP)	.031 (TP)
D	0.30 ± 0.10	.012 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	.020 ± .004
M	0.13	.005
N	0.1	.004



83CL-9080B (9/92)

44-Pin Plastic TSOP II (400-mil) #3

Item	Millimeters	Inches
A	18.37 ± 0.05	.723 ± .002
B	$0.885^{+0.05}_{-0.125}$	$.035^{+.002}_{-.005}$
C	0.8 (TP)	.031 (TP)
D	0.30 ± 0.08	.012 ± .004
E	0.04 ± 0.04	.002 ± .002
F	1.01 ± 0.06	.040 ± .002
G	0.97 ± 0.05	.038 ± .002
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	$.031^{+.009}_{-.008}$
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$
M	0.13	.005
N	0.08	.003

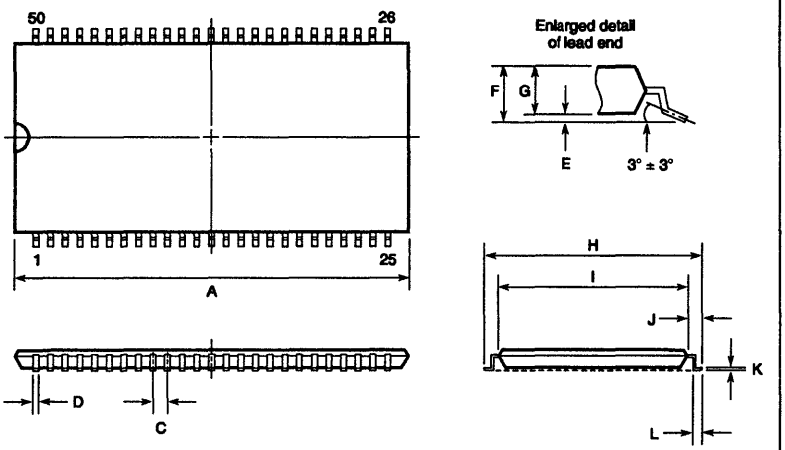


83CL-9065B (10/92)

29

50-Pin Plastic TSOP II (400-mil)

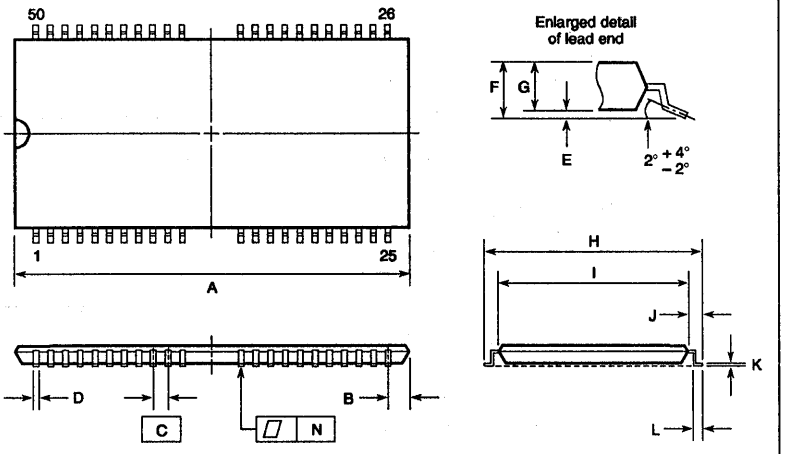
Item	Millimeters	Inches
A	21.11 ± .05	.831 ± .002
C	0.8 ± 0.05	.031 ± .002
D	0.3 ± 0.08	.012 ± .003
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$



83CL-9061B (9/92)

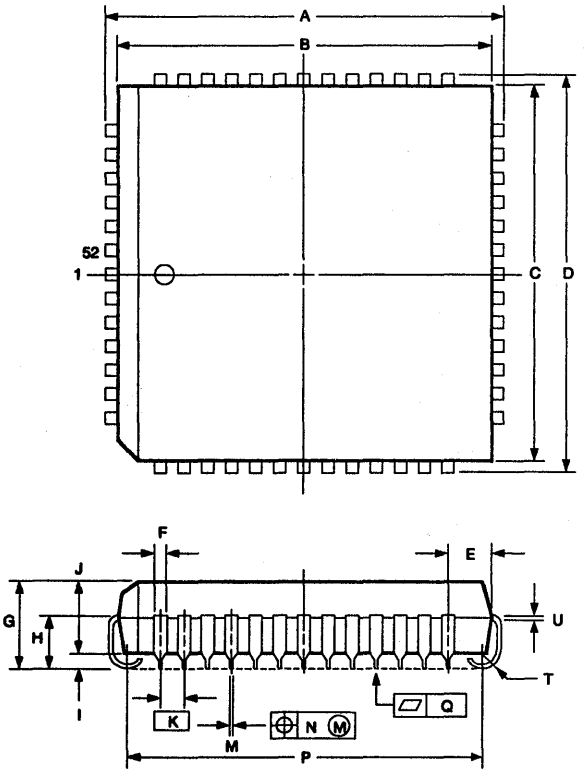
50/44-Pin Plastic TSOP II (400-mil)

Item	Millimeters	Inches
A	21.45 max	.844 max
B	1.06 max	.042 max
C	0.8 (TP)	.031 (TP)
D	0.30 ± 0.10	.012 ± .004
E	0.05 ± 0.05	.002 ± .002
F	1.10 max	.043 max
G	0.97	.038
H	11.76 ± 0.2	.463 ± .008
I	10.16 ± 0.1	.400 ± .004
J	0.8 ± 0.2	.031 ± .008
K	$0.125^{+0.10}_{-0.05}$	$.005^{+.004}_{-.002}$
L	0.5 ± 0.1	$.020^{+.004}_{-.005}$
N	0.10	.004



52-Pin Plastic LCC

Item	Millimeters	Inches
A	20.1 ±0.2	.791 ±.008
B	19.12	.753
C	19.12	.753
D	20.1 ±0.2	.791 ±.008
E	1.94 ±0.15	.076 ±.006
F	0.6	.024
G	4.4 ±0.2	.173 ±.008
H	2.8 ±0.2	.110 ±.008
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	.016 ±.004
N	0.12	.005
P	18.04 ±0.20	.710 ±.008
Q	0.15	.006
T	0.8 radius	.031 radius
U	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$



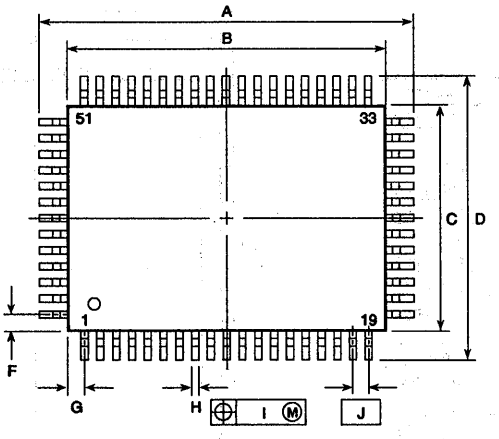
P52L-50A1

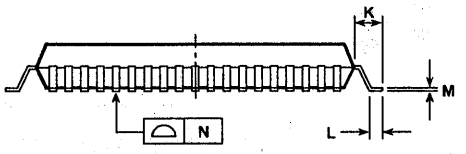
83YL-5805B

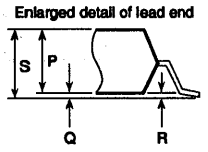
29

64-Pin Plastic QFP

Item	Millimeters	Inches
A	23.6 ± 0.4	.929 ± .016
B	20.0 ± 0.2	.795 $^{+.009}_{-.008}$
C	14.0 ± 0.2	.551 $^{+.009}_{-.008}$
D	17.6 ± 0.4	.693 ± .016
F	1.0	.039
G	1.0	.039
H	0.40 ± 0.10	.016 $^{+.004}_{-.005}$
I	0.20	.008
J	1.0 (TP)	.039 (TP)
K	1.8 ± 0.2	.071 $^{+.008}_{-.009}$
L	0.8 ± 0.2	.031 $^{+.009}_{-.008}$
M	0.15 $^{+0.10}_{-0.05}$	.006 $^{+.004}_{-.003}$
N	0.15	.006
P	2.7	.106
Q	0.1 ± 0.1	.004 ± .004
R	0.1 ± 0.1	.004 ± .004
S	3.0 max	.119 max





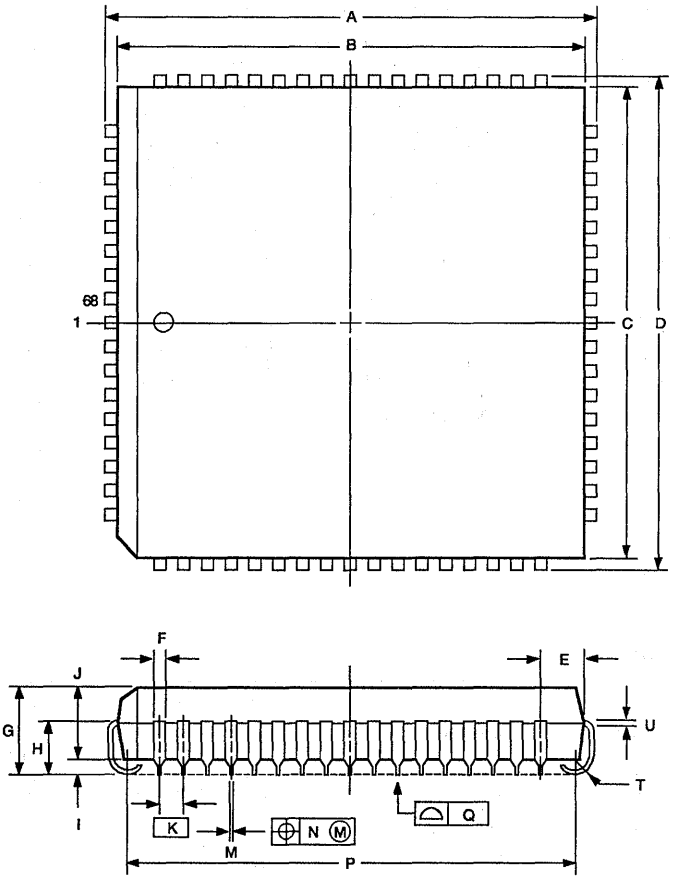


P64GF-100-3B8, 3BE-1

49NR-599B (6/91)

68-Pin Plastic LCC

Item	Millimeters	Inches
A	25.2 ±0.2	.992 ±.008
B	24.20	.953
C	24.20	.953
D	25.2 ±0.2	.992 ±.008
E	1.94 ±0.15	$.076^{+.007}_{-.006}$
F	0.6	.024
G	4.4 ±0.2	$.173^{+.009}_{-.008}$
H	2.8 ±0.2	$.110^{+.009}_{-.008}$
I	0.9 min	.035 min
J	3.4	.134
K	1.27 (TP)	.050 (TP)
M	0.40 ±0.10	$.016^{+.004}_{-.005}$
N	0.12	.005
P	23.12 ±0.20	$.910^{+.009}_{-.008}$
Q	0.15	.006
T	0.8 radius	.031 radius
U	$0.20^{+0.10}_{-0.05}$	$.008^{+.004}_{-.002}$



P68L-60A1-1

(2/90)

83YL-5561B

29

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