NEC Electronics Inc.

NEC

VOL 1 OF 2

MICROCOMPUTER PRODUCTS

1987 DATA BOOK

SINGLE-CHIP PRODUCTS

1987
MICROCOMPUTER
DATA BOOK

SINGLE-CHIP PRODUCTS
VOL 1 OF 2

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FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

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V25 is a trademark of NEC Corporation.

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GENERAL INFORMATION 1

Section 1 — General Information

Introduction

The NEC microcomputer data book is issued in two volumes.

- Volume 1: Single-Chip Products
- Volume 2: Microprocessors, Peripherals, and DSP Products

NEC offers a wide variety of single-chip microcomputer products for you to choose from. Volume 1 covers 4-bit, 8-bit, and 16-bit microcomputers plus LCD peripheral products, both NMOS and CMOS, in an assortment of packages. This extraordinary selection provides greater design alternatives with products that truly fit your needs in data processing, communications, instrumentation, industrial, and consumer applications.

Volume 1 is divided into the following sections.

1. General Information. This section includes ordering information, product selection guides, and ROM Code submission procedures.

2. Quality and Reliability. The NEC concepts of designed-in quality and total quality control as a company-wide activity are discussed here.

3. Four-Bit Single-Chip Microcomputers. This section covers the 7500 Series, the 75000 Series, and the cost-effective, low-end mini-microcomputers known as 755x/756x.

4. Eight-Bit Single-Chip Microcomputers. The 8-bit products include the popular 80xx/87xx and 80Cxx Series together with the high-end 7800 and 78000 Series.

5. Sixteen-Bit Single-Chip Microcomputers. The 16-bit microcomputers are CMOS products, type 70320/70322.

6. LCD Peripherals. Peripherals include LCD controller-driver products for alphanumeric, dot-addressable, and large-area displays.

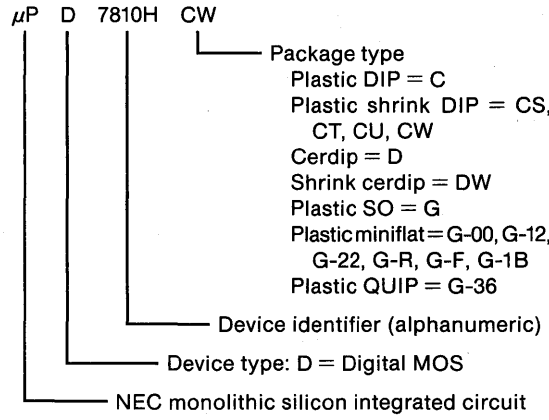
7. Development Tools. A comprehensive line of development hardware and software products support NEC's single-chip microcomputer families.

8. Packaging. This section provides dimensioned package drawings and a cross-reference from package type to device numbers.

Ordering Information

Part numbers for ordering microcomputer products are listed on the first page of each data sheet. NEC's part numbers consist of four elements as shown in the example that follows.

Part Numbering System



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4-Bit, Single-Chip CMOS Microcomputer Selection Guide

Device	Description	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X4)	I/O	Package	Pins
μPD7500HG-36	Microcomputer	0.7	4.5 to 5.5	External	256	46	Plastic QUIP	64
μPD7500H-EG-36	Microcomputer	0.2	4.5 to 5.5	External	256	46	Plastic QUIP	64
μPD7501G-12	Microcomputer with LCD Controller/Driver	0.4	2.5 to 6.0	1K	96	24	Plastic Miniflat	64
μPD7502G-12	Microcomputer with LCD Controller/Driver	0.4	2.7 to 6.0	2K	128	23	Plastic Miniflat	64
μPD7503G-12	Microcomputer with LCD Controller/Driver	0.4	2.7 to 6.0	4K	224	23	Plastic Miniflat	64
μPD7506C	Microcomputer	0.4	2.5 to 6.0	1K	64	22	Plastic DIP	28
μPD7506CT	Microcomputer	0.4	2.5 to 6.0	1K	64	22	Plastic Shrink DIP	28
μPD7506G-00	Microcomputer	0.4	2.5 to 6.0	1K	64	22	Plastic Miniflat	52
μPD7507C	Microcomputer	0.4	2.5 to 6.0	2K	128	32	Plastic DIP	40
μPD7507CU	Microcomputer	0.4	2.5 to 6.0	2K	128	32	Plastic Shrink DIP	40
μPD7507G-00	Microcomputer	0.4	2.5 to 6.0	2K	128	32	Plastic Miniflat	52
μPD7507HC	Microcomputer	4.19	2.7 to 6.0	2K	128	32	Plastic DIP	40
μPD7507HCU	Microcomputer	4.19	2.7 to 6.0	2K	128	32	Plastic Shrink DIP	40
μPD7507HG-22	Microcomputer	4.19	2.7 to 6.0	2K	128	32	Plastic Miniflat	44
μPD7507SC	Microcomputer	0.4	2.2 to 6.0	2K	128	20	Plastic DIP	28
μPD7507SCT	Microcomputer	0.4	2.2 to 6.0	2K	128	20	Plastic Shrink DIP	28
μPD7508C	Microcomputer	0.4	2.5 to 6.0	4K	224	32	Plastic DIP	40
μPD7508CU	Microcomputer	0.4	2.5 to 6.0	4K	224	32	Ptatic Shrink DIP	40
μPD7508G-00	Microcomputer	0.4	2.5 to 6.0	4K	224	32	Plastic Miniflat	52
μPD75CG08E	Piggyback EPROM Microcomputer	0.4	4.5 to 5.5	4K	224	32	Ceramic DIP	40
μPD7508HC	Microcomputer	4.19	2.7 to 6.0	4K	224	32	Plastic DIP	40
μPD7508HCU	Microcomputer	4.19	2.7 to 6.0	4K	224	32	Plastic Shrink DIP	40
μPD7508HG-22	Microcomputer	4.19	2.7 to 6.0	4K	224	32	Plastic Miniflat	44
μPD75CG08HE	Piggyback EPROM Microcomputer	4.19	4.5 to 5.5	4K	224	32	Ceramic DIP	40
μPD7508AC	Microcomputer with FIP Driver	0.4	2.7 to 5.5	4K	208	32	Plastic DIP	40
μPD7514G-12	Microcomputer with LCD Controllier/Driver	0.5	2.7 to 6.0	4K	256	31	Plastic Miniflat	80
μPD7516HG-12	Microcomputer with FIP Controller/Driver	6.55	2.5 to 6.0	6K	256	53	Plastic Miniflat	64
μPD7516HG-36	Microcomputer with FIP Controller/Driver	6.55	2.5 to 6.0	6K	256	53	Plastic QUIP	64
μPD7516HCW	Microcomputer with FIP Controller/Driver	6.55	2.5 to 6.0	6K	256	53	Plastic Shrink DIP	64
μPD75CG16HE	Piggyback EPROM Microcomputer with FIP Controller/Driver	6.55	4.5 to 5.5	6K	256	53	Ceramic QUIP	64

4-Bit, Single-Chip CMOS Microcomputer Selection Guide (cont)

Device	Description	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X4)	I/O	Package	Pins
μPD7519G-12	Microcomputer with FIP Controller/Driver	4.19	2.5 to 6.0	4K	256	53	Plastic Miniflat	64
μPD7519G-36	Microcomputer with FIP Controller/Driver	4.19	2.5 to 6.0	4K	256	53	Plastic QUIP	64
μPD7519CW	Microcomputer with FIP Controller/Driver	4.19	2.5 to 6.0	4K	256	53	Plastic Shrink DIP	64
μPD75CG19E	Piggyback EPROM Microcomputer with FIP Controller/Driver	4.19	4.5 to 5.5	4K	256	53	Ceramic DIP	64
μPD7519HG-12	Microcomputer with FIP Controller/Driver	6.55	2.5 to 6.0	4K	256	53	Plasti Miniflat	64
μPD7519HG-36	Microcomputer with FIP Controller/Driver	6.55	2.5 to 6.0	4K	256	53	Plastic QUIP	64
μPD7519HCW	Microcomputer with FIP Controller/Driver	6.55	2.5 to 6.0	4K	256	53	Plastic Shrink DIP	64
μPD75CG19HE	Piggyback EPROM Microcomputer with FIP Controller/Driver	6.55	4.5 to 5.5	4K	256	53	Ceramic DIP	64
μPD7527AC	Microcomputer with FIP Display	0.6	2.7 to 6.0	2K	128	35	Plastic DIP	42
μPD7527ACU	Microcomputer with FIP Display	0.6	2.7 to 6.0	2K	128	35	Plastic Shrink DIP	42
μPD7528AC	Microcomputer with FIP Display	0.6	2.7 to 6.0	4K	160	35	Plastic DIP	42
μPD7528ACU	Microcomputer with FIP Display	0.6	2.7 to 6.0	4K	160	35	Plastic Shrink DIP	42
μPD75CG28E	Piggyback EPROM Microcomputer with FIP Display	0.5	4.5 to 5.5	4K	160	35	Ceramic DIP	42
μPD7533C	Microcomputer with A/D Converter	0.5	2.7 to 6.0	4K	160	34	Plastic DIP	42
μPD7533CU	Microcomputer with A/D Converter	0.5	2.7 to 6.0	4K	160	34	Plastic Shrink DIP	42
μPD7533G-22	Microcomputer with A/D Converter	0.5	2.7 to 6.0	4K	160	34	Plastic Minflat	44
μPD75CG33E	Piggyback EPROM Microcomputer with A/D Converter	0.5	4.5 to 5.5	4K	160	34	Ceramic DIP	42
μPD7537AC	Microcomputer with FIP Driver	0.6	2.7 to 6.0	2K	128	35	Plastic DIP	42
μPD7537ACU	Microcomputer with FIP Driver	0.6	2.7 to 6.0	2K	128	35	Plastic Shrink DIP	42
μPD7538AC	Microcomputer with FIP Driver	0.6	2.7 to 6.0	4K	160	35	Plastic DIP	42
μPD7538ACU	Microcomputer with FIP Driver	0.6	2.7 to 6.0	4K	160	35	Plastic Shrink DIP	42

4-Bit, Single-Chip CMOS Microcomputer Selection Guide (cont)

Device	Description	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X4)	I/O	Package	Pins
μPD75CG38E	Piggyback EPROM Microcomputer with FIP Driver	0.5	4.5 to 5.5	4K	160	35	Ceramic DIP	42
μPD7554CS	Microcomputer with Serial I/O	0.7	2.5 to 6.0	1K	64	16	Plastic Shrink DIP	20
μPD7554G	Microcomputer with Serial I/O	0.7	2.5 to 6.0	1K	64	16	Plastic SO	20
μPD7556CS	Microcomputer with Comparator	0.7	2.5 to 6.0	1K	64	20	Plastic Shrink DIP	24
μPD7556G	Microcomputer with Comparator	0.7	2.5 to 6.0	1K	64	20	Plastic SO	24
μPD7564CS	Microcomputer with Serial I/O	0.7	2.7 to 6.0	1K	64	15	Plastic Shrink DIP	20
μPD7564G	Microcomputer with Serial I/O	0.7	2.7 to 6.0	1K	64	15	Plastic SO	20
μPD7566CS	Microcomputer with Comparator	0.7	2.7 to 6.0	1K	64	19	Plastic Shrink DIP	24
μPD7566G	Microcomputer with Comparator	0.7	2.7 to 6.0	1K	64	19	Plastic SO	24
μPD75104CW	Microcomputer	4.19	2.5 to 6.0	4K	320	58	Platic Shrink DIP	64
μPD75104G-1B	Microcomputer	4.19	2.5 to 6.0	4K	320	58	Plastic Miniflat	64
μPD75106CW	Microcomputer	4.19	2.5 to 6.0	(6016)	320	58	Plastic Shrink DIP	64
μPD75106G-1B	Microcomputer	4.19	2.5 to 6.0	(6016)	320	58	Plastic Miniflat	64
μPD75108CW	Microcomputer	4.19	2.5 to 6.0	8K	512	58	Plastic Shrink DIP	64
μPD75108G-1B	Microcomputer	4.19	2.5 to 6.0	8K	512	58	Plastic Miniflat	64
μPD75P108CW	Microcomputer with On-Chip OTPROM	4.19	2.5 to 6.0	8K	512	58	Plastic Shrink DIP	64
μPD75P108DW	Microcomputer with On-Chip EPROM	4.19	2.5 to 6.0	8K	512	58	Plastic Shrink DIP	64
μPD75P108G-1B	Microcomputer with On-Chip OTPROM	4.19	2.5 to 6.0	8K	512	58	Plastic Miniflat	64

8-Bit, Single-Chip Microcomputer Selection Guide

Device	Description	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	Package	Pins
μPD78C05AG-36	CMOS Microcomputer	6.25	2.6 to 6.0	External	128	46	Plastic QUIP	64
μPD78C06AG-12	CMOS Microcomputer	6.25	2.5 to 6.0	4K	128	46	Plastic Miniflat	64
μPD7807CW	NMOS Microcomputer with Comparator	12	4.5 to 5.5	External	256	28	Plastic Shrink DIP	64
μPD7807G-36	NMOS Microcomputer with Comparator	12	4.5 to 5.5	External	256	28	Plastic QUIP	64
μPD7808CW	NMOS Microcomputer with Comparator	12	4.5 to 5.5	4K	256	40	Plastic Shrink DIP	64
μPD7808G-36	NMOS Microcomputer with Comparator	12	4.5 to 5.5	4K	256	40	Plastic QUIP	64
μPD7809CW	NMOS Microcomputer with Comparator	12	4.5 to 5.5	8K	256	40	Plastic Shrink DIP	64
μPD7809G-36	NMOS Microcomputer with Comparator	12	4.5 to 5.5	8K	256	40	Plastic QUIP	64
μPD78P09R	NMOS Microcomputer with Comparator	12	4.5 to 5.5	EPROM 8K	256	40	Ceramic QUIP with Window	64
μPD7810CW	NMOS Microcomputer with A/D Converter	12	4.5 to 5.5	External	256	32	Plastic Shrink DIP	64
μPD7810G-36	NMOS Microcomputer with A/D Converter	12	4.5 to 5.5	External	256	32	Plastic QUIP	64
μPD78C10CW	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	External	256	32	Plastic Shrink DIP	64
μPD78C10G-1B	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	External	256	32	Plastic Miniflat	64
μPD78C10G-36	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	External	256	32	Plastic QUIP	64
μPD78C10L	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	External	256	32	PLCC	68
μPD7810HCW	NMOS Microcomputer with A/D Converter	15	4.5 to 5.5	External	256	32	Plastic Shrink DIP	64
μPD7810HG-36	NMOS Microcomputer with A/D Converter	15	4.5 to 5.5	External	256	32	Plastic QUIP	64
μPFD7811CW	NMOS Microcomputer with A/D Converter	12	4.5 to 5.5	4K	256	44	Plastic Shrink DIP	64
μPD7811G-36	NMOS Microcomputer with A/D Converter	12	4.5 to 5.5	4K	256	44	Plastic QUIP	64
μPD78C11CW	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	4K	256	44	Plastic Shrink DIP	64
μPD78C11G-1B	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	4K	256	44	Plastic Miniflat	64
μPD78C11G-36	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	4K	256	44	Plastic QUIP	64
μPD78C11L	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	4K	256	44	PLCC	68

8-Bit, Single-Chip Microcomputer Selection Guide (cont)

Device	Description	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	Package	Pins
μPD7811HG-36	NMOS Microcomputer with A/D Converter	15	4.5 to 5.5	4K	256	44	Plastic QUIP	64
μPD78PG11E	Piggy Back EPROM NMOS Microcomputer with A/D Converter	12	4.5 to 5.5	4K	256	44	Ceramic QUIP	64
μPD78C14CW	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	16K	256	44	Plastic Shrink DIP	64
μPD78C14G-1B	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	External	256	44	Plastic Miniflat	64
μPD78C14G-36	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	External	256	44	Plastic QUIP	64
μPD78C14L	CMOS Microcomputer with A/D Converter	12	4.5 to 5.5	External	256	44	PLCC	68
μPD78310CW	CMOS Microcomputer	12	4.5 to 5.5	External	256	28	Plastic Shrink DIP	64
μPD78310G-1B	CMOS Microcomputer	12	4.5 to 5.5	External	256	28	Plastic Miniflat	64
μPD78310G-36	CMOS Microcomputer	12	4.5 to 5.5	External	256	28	Plastic QUIP	64
μPD78310L	CMOS Microcomputer	12	4.5 to 5.5	External	256	28	PLCC	68
μPD78312CW	CMOS Microcomputer	12	4.5 to 5.5	8K	256	40	Plastic Shrink DIP	64
μPD78312G-1B	CMOS Microcomputer	12	4.5 to 5.5	8K	256	40	Plastic Miniflat	64
μPD78312G-36	CMOS Microcomputer	12	4.5 to 5.5	8K	256	40	Plastic QUIP	64
μPD78312L	CMOS Microcomputer	12	4.5 to 5.5	8K	256	40	PLCC	68
μPD78P312G-36	EPROM Microcomputer	12	4.5 to 5.5	8K	256	40	Plastic QUIP	64
μPD8035HLC	HMOS Microcomputer	6	4.5 to 5.5	External	64	27	Plastic DIP	40
μPD80C35C	CMOS Microcomputer	6	4.5 to 5.5	External	64	27	Plastic DIP	40
μPD8039HLC	HMOS Microcomputer	11	4.5 to 5.5	External	128	27	Plastic DIP	40
μPD80C39HC	CMOS Microcomputer	12	2.5 to 6	External	128	27	Plastic DIP	40
μPD80C40HC	CMOS Microcomputer	12	2.5 to 6	External	256	27	Plastic DIP	40
μPD8041AHC	NMOS Microcomputer with Universal PPI	11	4.5 to 5.5	1K	64	18	Plastic DIP	40
μPD80C42C	CMOS Microcomputer with Universal PPI	12	4.5 to 5.5	2K	128	18	Plastic DIP	40
μPD80C42G-22	CMOS Microcomputer with Universal PPI	12	4.5 to 5.5	2K	128	18	Plastic Miniflat	44
μPD8048HC	HMOS Microcomputer	6	4.5 to 5.5	1K	64	27	Plastic DIP	40
μPD80C48C	CMOS Microcomputer	6	2.5 to 6.0	1K	64	27	Plastic DIP	40
μPD80C48G-00	CMOS Microcomputer	6	2.5 to 6.0	1K	64	27	Plastic Miniflat	52
μPD48G-22	CMOS Microcomputer	6	2.5 to 6.0	1K	64	27	Plastic Miniflat	44
μPD8049HC	HMOS Microcomputer	11	4.5 to 5.5	2K	128	27	Plastic DIP	40
μPD80C49HC	CMOS Microcomputer	12	2.5 to 6.0	2K	128	27	Plastic DIP	40
μPD80C49G-00	CMOS Microcomputer	12	2.5 to 6.0	2K	128	27	Plastic Miniflat	52
μPD49HG-22	CMOS Microcomputer	12	2.5 to 6.0	2K	128	27	Plastic Miniflat	44

8-Bit, Single-Chip Microcomputer Selection Guide (cont)

Device	Description	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	Package	Pins
μPD80C50HC	CMOS Microcomputer	12	2.5 to 6.0	4K	256	27	Plastic DIP	40
μPD50HG-22	CMOS Microcomputer	12	2.5 to 6.0	4K	256	27	Plastic Miniflat	44
μPD8741AD	NMOS Microcomputer with Universal PPI	6	4.5 to 5.5	1K	64	18	Cerdip with Window	40
μPD8748HC	NMOS Microcomputer with UV EPROM	11	4.5 to 5.5	1K	64	27	Plastic DIP	40
μPD8748HD	NMOS Microcomputer with UV EPROM	11	4.5 to 5.5	1K	64	27	Cerdip with Window	40
μPD8749HC	HMOS Microcomputer	11	4.5 to 5.5	2K	128	27	Plastic DIP	40
μPD8749HD	HMOS Microcomputer	11	4.5 to 5.5	2K	128	27	Cerdip with Window	40

16-Bit, Single-Chip Microcomputer Selection Guide

Device	Description	Clock (MHz)	Supply Voltage (V)	ROM (X8)	RAM (X8)	I/O	Package	Pins
μPD70320G-12	CMOS Microcomputer	10	4.5 to 5.5 V	16K	256	32	Plastic Miniflat	80
μPD70320L	CMOS Microcomputer	10	4.5 to 5.5 V	16K	256	32	PLCC	84
μPD70322G-12	CMOS Microcomputer	10	4.5 to 5.5 V	16K	256	32	Plastic Miniflat	80
μPD70322L	CMOS Microcomputer	10	4.5 to 5.5 V	16K	256	32	PLCC	84

CMOS LCD Peripheral Selection Guide

Device	Description	No. of Rows	No. of Column	Clock (MHz)	Supply Voltage (V)	Power Dissipation		Package	Pins
						Active (mA)	Standby (mA)		
μPD6307G-F	LCD Row Driver	32	—	2.5	4.5 to 5.5	1	—	Plastic Miniflat	54
μPD6307G-R	LCD Row Driver	32	—	2.5	4.5 to 5.5	1	—	Plastic Miniflat Reverse leads	54
μPD6308G-F	LCD Column Driver	—	40	2	4.5 to 5.5	1.2	—	Plastic Miniflat	54
μPD6308G-R	LCD Column Driver	—	40	2	4.5 to 5.5	1.2	—	Plastic Miniflat Reverse leads	54
μPD7225G-00	LCD Controller/Driver	4	32	0.2	2.7 to 5.5	0.1	—	Plastic Miniflat	52
μPD7227G-12	LCD Controller/Driver	8	40	1	+5	0.2	—	Plastic Miniflat	64
μPD7228G-12	LCD Controller/Driver	8/16	42/50	1.1	+5	0.2	0.02	Plastic Miniflat	80
μPD72030G-12	LCD Display Controller	—	—	6	+5	5	0.001	Plastic Miniflat	64

μPD7500 Series Hardware Development Tool Selection Guide

Part Number	Emulator	Add-On Board (Required)	System Evaluation Board	EPROM Device
μPD7501	EVAKIT-7500B	EV7514	SE-7514A	—
μPD7502	EVAKIT-7500B	EV7514	SE-7514A	—
μPD7503	EVAKIT-7500B	EV7514	SE-7514A	—
μPD7506	EVAKIT-7500B	—	SE-7508	—
μPD7507	EVAKIT-7500B	—	—	μPD75CG08E
μPD7507H	EVAKIT-7500B	EV7508H	—	μPD75CG08HE
μPD7507S	EVAKIT-7500B	—	SE-7508	—
μPD7508	EVAKIT-7500B	—	—	μPD75CG08E
μPD7508A	EVAKIT-7500B	—	SE-7508	—
μPD7508H	EVAKIT-7500B	EV7508H	—	μPD75CG08HE
μPD7514	EVAKIT-7500B	EV7514	SE-7514A	—
μμPD7516H	EVAKIT-7500B	EV7500FIP	—	μPD75CG16HE
μPD7519	EVAKIT-7500B	EV7500FIP	—	μPD75CG19E
μPD7519H	EVAKIT-7500B	EV7500FIP	—	μPD75CG19HE
μPD7527	EVAKIT-7500B	EV7528	—	μPD75CG28E
μPD7528	EVAKIT-7500B	EV7528	—	μPD75CG28E
μPD7533	EVAKIT-7500B	EV7533	—	μPD75CG33E
μPD7537	EVAKIT-7500B	EV7528	—	μPD75CG38E
μPD7538	EVAKIT-7500B	EV7528	—	μPD75CG38E
μPD7554	EVAKIT-7500B	EV7554A	SE-7554A	—
μPD7556	EVAKIT-7500B	EV7554A	SE-7554A	—
μPD7564	EVAKIT-7500B	EV7554A	SE-7554A	—
μPD7566	EVAKIT-7500B	EV7554A	SE-7554A	—

μPD75000 Series Hardware Development Tool Selection Guide

Device	Description
EV75108	Add-on board
EV75208	Add-on board

μPD7800 Series Hardware Development Tool Selection Guide

Part Number	Emulator	Real-time Trace Board	Add-on Board	System Evaluation Board	EPROM Device
μPD78C05A	EVAKIT-87LC [Note 1]	EV87LCRTT	EV78C06A	SE-78C06	—
μPD78C06A	EVAKIT-87LC	EV87LCRTT	EV78C06A	SE-78C06	—
μPD7807	IE-7809-M	—	—	—	μPD78P09R
μPD7808	IE-7809-M	—	—	—	μPD78P09R
μPD7809	IE-7809-M	—	—	—	μPD78P09R
μPD7810	EVAKIT-87AD [Note 1] IE-87AD-M	EV87ADRTT —	— —	— —	— —
μPD7810H	IE-7811H	—	—	—	—
μPD78C10	IE-78C11-M	—	—	—	—
μPD7811	EVAKIT-87AD [Note 1] IE-87AD-M	EV87ADRTT —	— —	— —	μPD78PG11E μPD78PG11E
μPD7811H	IE-7811H	—	—	—	μPD78PG11E [Note 2]
μPD78C11	IE-78C11-M	—	—	—	—
μPD78C14	IE-78C11-M	—	—	—	—

Notes:

(1) Addresses 0-0FFFH access memory on the Evakit only.

(2) Special selected parts.

μPD78000 Series Hardware Development Tool Selection Guide

Device	Description
IE-310-R	Stand-alone in-circuit emulator

μPD70320/322 Hardware Development Tool Selection Guide

Device	Description
IE-70322	Portable stand-alone in-circuit emulator

μPD8048 Series Hardware Development Tool Selection Guide

Part Number	Emulator	System Evaluation Board	EPROM Device
μPD8035H	EVAKIT-84C-1	—	—
μPD8048H	EVAKIT-84C-1	—	μPD8748H*
μPD8039H	EVAKIT-84C-1	—	—
μPD8049H	EVAKIT-84C-1	—	μPD8749H*
μPD80C39H	EVAKIT-84C-1	—	—
μPD80C48	EVAKIT-84C-1	SE-80C50H	—
μPD80C35	EVAKIT-84C-1	—	—
μPD80C49H	EVAKIT-84C-1	SE-80C50H	—
μPD80C40H	EVAKIT-84C-1	—	—
μPD80C50H	EVAKIT-84C-1	SE-80C50H	—
μPD80C42	EVAKIT-80C42	—	μPD8741A

*μPD8748H and μPD8749H are both available in erasable windowed packages or in the economical one time programmable plastic package.

Conversion Board	Function
EV-9001-64	64-pin QUIP to 64-pin shrink DIP
EV-9002-42	42-pin standard DIP to 42-pin shrink DIP
EV-9002-40	40-pin standard DIP to 40-pin shrink DIP
EV-9002-28	28-pin standard DIP to 28-pin shrink DIP

MD-086 Series Microcomputer Development System Selection Guide

Device	Description
MD-086FD-10	MD-086 series, floppy-disk based system
MD-086HD-10	MD-086 series, floppy-hard-disk based system
MD-086DK	Hard-disk upgrade for MD-086FD-10
MD-910TM	Character display terminal

MD-910TM Character Display Terminal Development System Selection Guide

Device	Description
MD-910TM	Character display terminal

PG1000 PROM Programmer Selection Guide

Device	Description
PG1003	Plug-in personality module
PG1005	Plug-in personality module

Ordering Procedure for ROM-Based Microcomputer Products

The devices listed below are ROM-based microcomputer products.

μPD70322	μPD7533	μPD78C11
μPD7501	μPD7537A	μPD78C14
μPD7502	μPD7538A	μPD78312
μPD7503	μPD7554	μPD8041AH
μPD7506	μPD7556	μPD80C42
μPD7507	μPD7564	μPD8048H
μPD7507H	μPD7566	μPD80C48
μPD7507S	μPD75104	μPD8049H
μPD7508	μPD75106	μPD80C49H
μPD7508H	μPD75108	μPD80C50H
μPD7514	μPD75206	μPD8355
μPD7516H	μPD75208	
μPD7519	μPD78C06A	
μPD7519H	μPD7809	
μPD7527A	μPD7811	
μPD7528A	μPD7811H	

Please use the following ordering guidelines. Contact your local sales representative for assistance and to obtain the necessary forms.

A complete order must include:

- ☐ Two copies of ROM code information contained in either the equivalent memory EPROMs or EPROM-based microcomputers.
- ☐ ROM code submission form (provided by your local sales representative); see next three pages.
- ☐ Your engineering specifications, if applicable. Please ignore this item if NEC has already reviewed your specification.
- ☐ Mask charge payment.
- ☐ Liability agreement for ROM-based work-in-progress. The NEC form, "ROM-Based Microprocessors Agreement," can be obtained from your local sales representative.
- ☐ Your purchase order.

NEC Electronics Inc. will return the ROM code patterns in the EPROM media together with a code listing and a ROM-code verification form to you. Please return the verification form to verify the code in the EPROM provided by NEC. NEC guarantees that the final product will contain the same code you verified.

Summary:

Step 1 ☐ Customer submits a complete order, including the items listed above.

Step 2 ☐ NEC returns ROM pattern to customer together with a ROM-code verification form and a code listing.

Step 3 ☐ Customer verifies code received from NEC and returns verification form.

Step 4 ☐ NEC acknowledges customer order and begins production.

NEC
NEC Electronics Inc.

ROM CODE SUBMISSION

To: NEC Electronics Inc.
Corporate Headquarters
401 Ellis Street, P.O. Box 7241
Mountain View, CA 94039

Date _____

Attn: ROM Code Administrator

We are ready to place a purchase order for our _____ (Customer Part Number), your _____ (NEC Part Number), and are submitting **two** copies of the ROM code on the following medium/media. (Please check all applicable boxes.)

- ☐ μPD2764
- ☐ μPD27128
- ☐ μPD70P322
- ☐ μPD75P108
- ☐ μPD77P20
- ☐ μPD78P09
- ☐ μPD78P312
- ☐ μPD8741A
- ☐ μPD8748H
- ☐ μPD8749H
- ☐ μPD8755A

This device should be manufactured as follows: (Please check all applicable boxes.)

- ☐ To our engineering specification # _____
- ☐ With special marking: _____
- ☐ With the I/O port loading options (available only on the devices listed on this form).
- ☐ Lead type (if applicable) Bent _____ Straight _____
- ☐ Application _____

NEC Electronics Inc.
Please return the processed ROM code to the following individual for our verification.

Name _____

Company _____

Division _____

Shipping Address (not a P.O. Box, please) _____

City _____ State _____ ZIP _____

Telephone Number _____

Customer
Please send this form and the items listed below in a package clearly marked "ROM CODE Enclosed" to the address above.

- Two copies of ROM code
- Engineering specification, if applicable. Not required if NEC has already reviewed the specification.
- Mask charge payment.
- Signed "ROM-Based Microprocessors Agreement"
- Purchase order

Form No. NEC-0000071 Rev. B 7/86

NEC

μPD7519, μPD7519H, μPD7516H

Pin	I/O Port Loading Option	
	Open drain	Pull-down resistor to V_{LOAD}
S_0	□	□
S_1	□	□
S_2	□	□
S_3	□	□
S_4	□	□
S_5	□	□
S_6	□	□
S_7	□	□
T_8/S_8	□	□
T_9/S_9	□	□
T_{10}/S_{10}	□	□
T_{11}/S_{11}	□	□
T_{12}/S_{12}	□	□
T_{13}/S_{13}	□	□
T_{14}/S_{14}	□	□
T_{15}/S_{15}	□	□
T_0	□	□
T_1	□	□
T_2	□	□
T_3	□	□
T_4	□	□
T_5	□	□
T_6	□	□
T_7	□	□

μPD7527A, μPD7528A, μPD7537A, μPD7538A

Pin	I/O Port Loading Option	
$P0_0$/INT0	□ Direct connection (no zero-crossing detector)	□ Zero-crossing detector
	Open drain	Pull-down resistor to V_{LOAD}
$P2_3$-$P2_1$	□	□
$P3_3$-$P3_0$	□	□
$P4_3$-$P4_0$	□	□
$P5_3$-$P5_0$	□	□
$P8_0$	□	□
$P8_1$	□	□
$P8_2$	□	□
$P8_3$	□	□
$P9_0$	□	□
$P9_1$	□	□
$P9_2$	□	□
$P9_3$	□	□
$P10_0$	□	□
$P10_1$	□	□
$P10_2$	□	□
$P10_3$	□	□
$P11_0$	□	□
$P11_1$	□	□
$P11_2$	□	□
$P11_3$	□	□

μPD7554, μPD7564

Pin	I/O Port Loading Option		
	Pull-up resistor	Pull-down resistor	No internal resistor
$P0_0$	□	□	□
$P0_1$	□	□	□
$P0_2$	□	□	□
$P0_3$	□	□	□
	N-channel, open drain	CMOS, push-pull output	
$P8_0$	□	□	
$P8_1$	□	□	
$P8_2$	□	□	N-channel, open-drain, and pull-up
$P8_3$*	□	□	
$P10_0$	□	□	□
$P10_1$	□	□	□
$P10_2$	□	□	□
$P10_3$	□		□
$P11_0$	□	□	□
$P11_1$	□	□	□
$P11_2$	□	□	□
$P11_3$	□	□	□
Oscillator	□ R-oscillator		□ External clock (7554 only)
RESET	□ No internal resistor		□ Pull-down resistor

* If $P8_3$ is used for CL2, the N-channel open-drain option should be selected. In this case, $P8_3$ cannot function as a port.

NEC

μPD7556, μPD7566

Pin	I/O Port Loading Option			
	Pull-up resistor	Pull-down resistor	No internal resistor	
$P0_0$	☐	☐	☐	V_{REF} ☐
$P0_1$	☐	☐	☐	
$P0_2$	☐	☐	☐	Comparator input
$P0_3$	☐	☐	☐	
$P1_0$	☐	☐	☐	☐
$P1_1$	☐	☐	☐	☐
$P1_2$	☐	☐	☐	☐
$P1_3$	☐	☐	☐	☐
	N-channel, open-drain	CMOS, push-pull output		
$P8_0$	☐	☐		
$P8_1$	☐	☐		
$P8_2$	☐	☐		
$P8_3$*	☐	☐		
$P9_0$	☐	☐	N-channel, open-drain, and pull-up	
$P9_1$	☐	☐		
$P10_0$	☐	☐	☐	
$P10_1$	☐	☐	☐	
$P10_2$	☐	☐	☐	
$P10_3$	☐	☐	☐	
$P11_0$	☐	☐	☐	
$P11_1$	☐	☐	☐	
$P11_2$	☐	☐	☐	
$P11_3$	☐	☐	☐	
Oscillator	☐ R-oscillator		☐ External clock (7556 only)	
RESET	☐ No internal resistor		☐ Pull-down resistor	
V_{REF}	☐ No internal bias		☐ Internal bias	

* If $P8_3$ is used for CL2, the N-channel open-drain option should be selected. In this case, $P8_3$ cannot function as a port.

μPD75104, μPD75106

Pin	I/O Port Loading Option	
	Open drain	Pull-up resistor
$P12_0$	☐	☐
$P12_1$	☐	☐
$P12_2$	☐	☐
$P12_3$	☐	☐
$P13_0$	☐	☐
$P13_1$	☐	☐
$P13_2$	☐	☐
$P13_3$	☐	☐
$P14_0$	☐	☐
$P14_1$	☐	☐
$P14_2$	☐	☐
$P14_3$	☐	☐
Power-on reset flag	☐ Yes	☐ No
Power-on reset generator	☐ Yes*	☐ No

* If power-on reset generator is selected, power-on reset flag must be selected also.

μPD80C48

Pin	I/O Port Loading Option	
	CMOS (−5 μA)	TTL-compatible (−50 μA)
$P1_0$-$P1_7$	☐	☐
$P2_0$-$P2_3$	☐	☐
$P2_4$-$P2_7$	☐	☐

μPD80C49H, μPD80C50H

Pin	I/O Port Loading Option		
	CMOS (−5 μA)	No pull-up resistor	TTL-compatible (−50 μA)
$P0_0$-$P0_7$	☐	☐	☐
$P1_0$-$P1_7$	☐	☐	☐
$P2_4$-$P2_7$	☐	☐	☐

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QUALITY AND RELIABILITY

Section 2 — Quality and Reliability

Introduction

As large-scale integration reaches a higher level of density, reliability of devices imposes a profound impact on system reliability. And as device reliability becomes a major factor, test methods to assure acceptable reliability become more complicated. Simply performing a reliability test according to a conventional method cannot satisfy the demanding requirements for higher reliability. At these new, higher levels of LSI density, it is increasingly difficult to activate all the elements in the internal circuits. A different philosophy and methodology is needed for reliability assurance. Moreover, as integration density increases, the degradation of internal elements in an LSI device is seldom detected by measuring characteristics across external terminals.

In order to improve and guarantee a certain level of reliability for large-scale integrated circuits, it is essential to build quality and reliability into the product. Then, the conventional reliability tests are followed to ensure that the product demonstrates an acceptable level of reliability.

NEC has introduced the concept of total quality control (TQC) across its entire semiconductor product line. By adopting TQC, NEC can build quality into the product and thus assure higher reliability. The concept and methodology of total quality control are company-wide activities involving workers, engineers, quality control staffs, and all levels of management.

NEC has also introduced a prescreening method into the production line that helps eliminate potentially defective units. The combination of building quality in and screening projected early failures out has resulted in superior quality and excellent reliability.

Technology Description

Most large-scale integrated circuits utilize high-density, MOS technology. State-of-the-art high performance has been achieved by introducing fine-line generation techniques. By reducing physical parameters, circuit density and performance increase while active circuit power dissipation decreases. The data presented here shows that this advanced technology yields products as reliable as those from previous technologies.

Reliability Testing

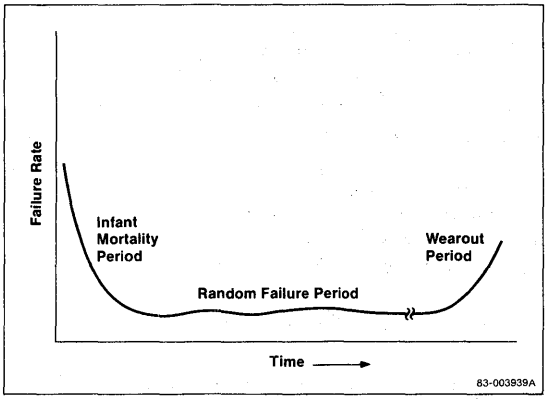
Reliability is defined as the characteristics of an item expressed by the probability that it will perform a required function under stated conditions for a stated period of time. This involves the concept of probability, definition of required function(s), and the critical time used in defining the reliability.

Definition of a required function, by implication, treats the definition of a failure. Failure is defined as the termination of the ability of a device to perform its required function. Furthermore, a device is said to have failed if it shows inability to perform within quaranteed parameters as given in an electrical specification.

Discussion of reliability and failure can be approached in two ways: with respect to systems or to individual devices. The accumulation of normal device failure rates constitutes the expected failure rate of the system hardware. Important considerations here are the constant failure period, the early failure (infant mortality) period, and overall reliability level. With regard to individual devices, areas of prime interest include specific failure mechanisms, failures in accelerated tests, and screening tests.

Some of these failure considerations pertain to both systems and devices. The probability of no failures in a system is the product of the probability of no failure in each of its components. The failure rate of system hardware is then the sum of the failure rates of the components used to construct the system.

Figure 1. Reliability Life (Bathtub) Curve



Life Distribution

The fundamental principles of reliability engineering predict that the failure rate of a group of devices will follow the well-known bathtub curve in figure 1. The curve is divided into three regions: infant mortality, random failures, and wearout failures.

Infant mortality, as the name implies, represents the early-life failures of devices. These failures are usually associated with one or more manufacturing defects.

After some period of time, the failure rate reaches a low value. This is the random failure portion of the curve, representing the useful portion of the life of a device. During this random failure period, there is a decline in the failure rate due to the depletion of potential random failures from the general population.

The wearout failures occur at the end of the device's useful life. They are characterized by a rapidly rising failure rate over time as devices wear out both physically and electrically.

Thus, for devices that have very-long life expectancies compared to those of systems, the areas of concern will be the infant mortality and the random failure portions of the population.

The system failure rates are related to the collective device failure rates. In a given system, after elimination of the early failures, the system will be left to the failure rate of its components. In order to make proper projections of the failure rate in the operating environment, time-to-failure must be accelerated in tests in a predictable way.

Failure Distribution at NEC

Integrated circuits returned to NEC from the field underwent extensive failure analysis at NEC's Integrated Circuit Division.

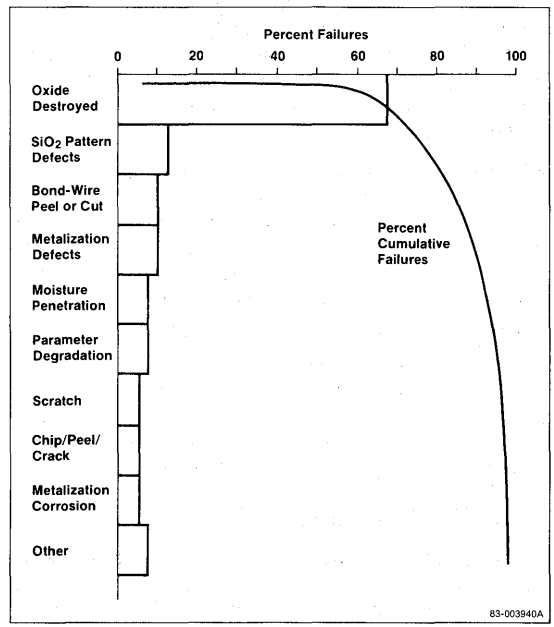
First, approximately 50 percent of the field returns were found to be damaged either from improper handling or misuse of the devices. These units were eliminated from the analysis. The remaining failed units were classified by their failure mechanisms as depicted in figure 2. These failures were then related to the major integrated circuit failure mechanisms and to their origins in a particular manufacturing step.

As shown in figure 2, the first four failure mechanisms accounted for more than 90 percent of total failures. As a result, NEC improved processes and material to reduce these failures. Additionally, NEC introduced screening procedures to detect and eliminate defective devices.

Temperature, humidity, and bias tests are used for testing the moisture resistance of plastic encapsulated integrated circuits. NEC developed a special process to improve the plastic encapsulation material. As a result, moisture-related—thus packaging-related—failures have been drastically reduced.

As a preventive measure, NEC has introduced a special screening procedure embedded in the production line. A burn-in at an elevated temperature is performed for 100 percent of the lots. This burn-in effectively removes the potentially defective units. In addition, improvement of the plastic encapsulation material has lowered the failures in a high-temperature and high-humidity environment.

Figure 2. Failure Distribution of MOS Integrated Circuits



Accelerated Reliability Testing

As an example, assume that an electronic system contains 1000 integrated circuits and can tolerate 1 percent system failures per month. The failure rate per component is:

$$\frac{0.01 \text{ Failures}}{720\text{K Device Hours}} = 13.888 \times 10^{-9} \text{ Failures/Hour or } 13.8888 \text{ FITs}$$

where FIT = Failure units per 10^9 device hours

To demonstrate this failure rate, note that 13.8888 FITs corresponds to one failure in about 7000 devices during an operating test of 10,000 hours. It is quickly apparent that a test condition is required to accelerate the time-to-failure in a predictable and understandable way. The implicit requirement for the accelerated stress test is that the relationship between the accelerated stress testing condition and the condition of actual use be known.

A most common time-to-failure relationship involves the effect of temperature, which accelerates many physiochemical reactions leading to device failure. Other environmental conditions are voltage, current, humidity, vibration, or some combination of these. Table 1 lists the reliability assurance tests performed at NEC for integrated circuits.

Table 1. Monthly NEC Reliability Tests

Test	MIL-STD-883 Method	Test Conditions
Life Test		
High-temperature, operating	1005A, D	T_A = 100 to 125°C for 1000 hours
High-temperature, storage	1008C	T_A = 150°C for 1000 hours
High-temperature, high-humidity test	—	T_A = 85°C at 85% RH for 1000 hours
Pressure cooker test	—	T_A = 125°C at 2.3 atm for 168 hours
Environmental Test		
Soldering heat test	2031 (MIL-STD-750)	T = 260°C for 10 s without flux
Temperature cycle	1010C	T = −65 to +150°C for 10 cycles
Thermal shock	1011A	T = 0 to 100°C for 15 cycles
Lead fatigue	2004B2	at 250 gm: 3 leads, 3 bends
Solderability	2003	T = 230°C for 5 s with flux

Temperature Effect. The effect of temperature that concerns us is that which responds to the Arrhenius relationship. This relates the reaction rate to temperature.

$$R = R_o \exp(-E_a/kT)$$

where R_o = Constant
E_a = Activation energy in eV
k = Boltzmann's constant
= 8.617×10^{-5} eV/K
T = Absolute temperature in kelvin (K)

The significance of this relationship is that the failure mechanisms of semiconductor devices are directly applicable to it. A linear relationship between failure mechanism and time is assumed.

Activation Energy. Associated with each failure mechanism is an activation energy value. Table 2 lists some of the more common failure mechanisms and the associated activation energy of each.

Table 2. Activation Energy and Detection of Failure Mechanisms

Failure Mechanism	Activation Energy	Detection
Oxide defect	0.3 eV	High-temperature operating life test
Silicon defect	0.3 eV	
Ionic contamination	1.0-1.35 eV	
Electromigration	0.4-0.8 eV	
Charge injection	1.3 eV	
Gold-aluminum interface	0.8 eV	
Metal corrosion	0.7 eV	High-humidity operating life test

High-Temperature Operating Life Test. This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature of 125°C. The data obtained is translated to a lower temperature by using the Arrhenius relationship.

High-Temperature and High-Humidity Test. Semiconductor integrated circuits are highly sensitive to the general accelerating effect of humidity in causing electrolytic corrosion between biased lines. The high-temperature and high-humidity test is performed to detect failure mechanisms that are accelerated by these conditions. This test is effective in accelerating leakage-related failures and drifts in device parameters due to process instability.

High-Temperature Storage Test. Another common test is the high-temperature storage test in which devices are subjected to elevated temperatures with no applied bias. This test is used to detect mechanical problems and process instability.

Environmental Test. Other environmental tests are performed to detect problems related to the package, material, susceptibility to extremes in environment, and problems related to usage of the devices.

Failure Rate Calculation and Prediction

Analysis of integrated circuit failure rates can serve many useful purposes. For example, the early-life failure rate helps establish a warranty period, while the mature-life failure rate aids in estimating repair costs, spare parts stock requirements, or product downtime. Accurate prediction of failure rates can also be used for process control.

The following sections describe the failure rate calculation and prediction methods used by NEC's Integrated Circuit Division.

The Arrhenius Model

Most integrated circuit failure mechanisms depend to some degree on temperature. This relationship can be represented by the Arrhenius model, which includes the effects of temperature and activation energy of the failure mechanisms.

As applied to accelerated life testing of integrated circuits, the Arrhenius model assumes that degradation of a performance parameter is linear with time. Temperature dependence is taken to be the exponential function that defines the probability of occurrence. The relationship of failure rate to temperature is expressed as:

$$F_1 = F_2 \exp[(E_a/k) \times (1/T_1 - 1/T_2)]$$

Where: F_2 = Failure rate at T_2
F_1 = Failure rate at T_1
E_a = Activation energy in eV
k = Boltzmann's constant
T = Operating junction temperature in kelvin (K)

The equation explains the thermal dependence of integrated circuit failure rates and is used for derating the resulting failure rate to a more realistic temperature.

Acceleration Factor

The acceleration factor is the factor by which the failure rate can be accelerated by increased temperature. This factor is derived from the Arrhenius failure rate expression, resulting in the following form.

$$A = F_1/F_2 = \exp[(E_a/k) \times (1/T_1 - 1/T_2)]$$

where A = Acceleration factor
F_2 = Failure rate at T_2
F_1 = Failure rate at T_1

In calculating the field reliability of an integrated circuit, it is necessary to calculate the junction temperature. In general, the junction temperature will depend on the ambient temperature, cooling, package type, operating cycle time, and power dissipation of the circuit itself. In these terms, the junction temperature (T_J) is expressed as:

$$T_J = T_A + P_d A_f \theta_{JA}$$

where T_J = Junction temperature
T_A = Ambient temperature
P_d = Power dissipation
A_f = Air flow factor
θ_{JA} = Package thermal resistance

Table 3 lists derating factors of various failure mechanisms. This table is generated assuming that an accelerated test is performed at a junction temperature of 125°C. The result is then derated to 55°C junction temperature. The acceleration factor may then be obtained by taking the inverse of the derating factor.

Table 3. Derating Factors of Failure Mechanisms

Failure Mechanisms	Activation Energy, eV	Derating Factor
Oxide defect	0.3	0.1546
Silicon defect	0.3	0.1546
Ionic contamination	1.0	0.001984
Electromigration	0.4	0.08307
Charge injection	1.3	0.0003067
Metal corrosion	0.7	0.01315
Gold-aluminum interface	0.8	0.006886

The acceleration of failure mechanisms in a high-humidity and high-temperature environment must be expressed as a function not only of temperature but also of humidity.

According to the reliability test statistics, the acceleration factor in such an environment can best be approximated with Peck's model as follows.

$$A = \exp[(E_a/k) \times (1/T_1 - 1/T_2)] \times (H_2/H_1)^{4.5}$$

where E_a = Activation energy
k = Boltzmann's constant
T = Junction temperature
H = Relative humidity

For example, the acceleration factor for high-humidity and high-temperature or pressure cooker tests ranges from 100 to 1000 times that of the normal operating environment.

Failure Rate Calculation

As an example, suppose that product samples are submitted to a 1000-hour life test at 125 °C junction temperature and two failures are encountered: one oxide and one metalization defect. The sample size is 885 units.

Thus, the oxide failure rate is 0.11 percent per 1000 hours and the metalization failure rate is 0.11 percent per 1000 hours. Therefore, the total failure rate at 125 °C sums to 0.22 percent per 1000 hours at 1K hours.

Failure Rate Prediction

To derate these failure rates to a normal operating environment, use the derating factors listed in table 3.

Oxide failures = 0.11 x 0.1546 = 0.01701% per 1K hrs
Metal failures = 0.11 x 0.01315 = 0.00145% per 1K hrs
Total failures = 0.01846% per 1K hrs

Note that the example above is a snapshot of the high-temperature life test performed on a particular lot. It is not accumulated data that can be used to represent overall reliability. This conservative illustration, however, shows that the failure rate in a normal operating environment is approximately one-twelfth the failure rate in a higher-temperature environment.

The failure rate prediction takes different activation energies into account whenever the causes of failures are known through performing failure analysis. In some cases, however, an activation energy is assumed in order to accomplish a quick first-order approximation. To yield a conservative estimate of failure rates, NEC assumes an average activation energy of 0.7 eV whenever the exact failure mechanism is not known.

Reliability Test Results

Before introducing new technologies or products, NEC's internal reliability goals must be attained. Several categories of testing are used in the internal qualification program to assure that product reliability meets NEC's reliability goals. Once the product is qualified, its reliability level is regularly monitored in a monthly reliability test.

NEC's Goals on Failure Rates

NEC's approach to achieving high reliability is to build quality into the product, as opposed to merely screening out defective units. The use of distributed control methods embedded in the production line, in conjunction with conventional screening methods, results in the highest reliability at the lowest cost.

NEC's maximum failure rate goals for infant mortality and long-term device operation are listed in table 4.

Table 4. Infant Mortality and Long-Term Failure Rates

Type	Failure Rate Percent/1000 Hours
Infant mortality	0.10 max
Long-term	
1.2M device hours average	0.02 max
3.0M device hours average	0.01 max

Infant Mortality Failure Rate

The infant mortality goal for each product group is set at 0.10 percent maximum. When a failure rate exceeds this level, there is prompt remedial action.

Long-Term Failure Rate

The long-term failure rate goal is based on the following conditions:

- A minimum of 1.2 million device hours at 125 °C is accumulated to resolve 0.02 percent per 1000 hours at 55 °C with a 60-percent confidence level.
- A minimum of 3 million device hours at 125 °C is accumulated to resolve 0.01 percent per 1000 hours at 55 °C with a 60-percent confidence level.

Infant Mortality Failure Screening

It is logical to assume the integrated circuit that fails at one temperature would also fail at another temperature, except it would fail sooner at a higher temperature. As can be expected, the failure rate is a function of activation energy. Establishing infant mortality screening, therefore, requires knowledge of the likely failure mechanisms and their associated activation energy.

The most likely mechanisms associated with infant mortality failures are generally manufacturing defects and process anomalies. These generally consist of contamination, cracked chips, wire bond shorts, or bad wire bonds. Since these describe a number of possible mechanisms, any one of which might predominate at a given time, the activation energy for infant mortality might be expected to vary considerably.

The effectiveness of a screening condition, preferably at some stress level in order to shorten the time, varies greatly with the failure mechanism being screened for. Another factor is the economics of the screening process introduced into the production line. Optimal conditions and duration of a screening process will be a compromise of these two factors.

For example, failures due to ionic contamination have an activation energy of approximately 1.0 eV. Therefore, a 15-hour stress at 125°C junction temperature would be the equivalent of approximately 90 days of operation at a junction temperature of 55°C. On the other hand, failures due to oxide defects have an activation energy of approximately 0.3 eV, and a 15-hour stress at 125°C junction temperature would be the equivalent of approximately one week's operation at 55°C junction temperature. As indicated by this, the condition and duration of infant mortality screening would be a strong function of the allowable component failures, hence the system failure, in the field.

Empirical data, gathered over more than a year at NEC, indicates that early failure does occur after less than 4 hours of stress at 125°C ambient temperature. This fact is supported by the life test of the same lot, where the failure rate shows random distribution, as opposed to a decreasing failure rate that then runs into the random failure region.

NEC has adopted the initial infant mortality burn-in at 125°C as a standard production screening procedure. As a result, the field reliability of NEC devices is an order of magnitude higher than the goals set for NEC's integrated circuit products.

Life Tests

The most significant difference between NEC's products and those of other integrated circuit manufacturers is that NEC's have been prescreened for their infant mortality defects. The products delivered to customers are operating at the beginning of the random failure region of the life curve. The life test data also reflects this fact, as will be shown.

The failure mechanism distribution from field failures, as previously shown in figure 2, also contains a very low percentage due to infant mortality. The majority of failures are long-term life failures, and these can be eliminated by stringent process control. Usually, these failure mechanisms have low activation energy associated with them.

Another significant improvement devised by NEC is plastic encapsulation and passivation. As a result, NEC products show excellent reliability in both high-humidity and high-temperature environments. Following is life test data accumulated over more than a year for large-scale integrated circuits.

High-Temperature Operating Life Test

This test is used to accelerate failure mechanisms by operating the devices at an elevated temperature. For large-scale integrated circuits, the failure rate is 0.242 percent per 1000 hours at 125°C. This is equivalent to 0.0071 percent per 1000 hours in an operating environment of 55°C (table 5).

Table 5. High-Temperature Operating Life Test

Number of Samples	Number of Failures at				
	48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
3317	0	0	1	4	3
Total number of failures at 1K hrs	= 8				
Failure rate at 1K hrs at 125°C	= 0.242% per 1K hrs				
Projected failure rate at 1K hrs at 55°C	= 0.007% per 1K hrs				

High-Temperature and High-Humidity Life Test

This test is used to accelerate failure mechanisms by operating the devices at high temperature and high humidity. Leakage-related failures and device parameter drift are accelerated by this test. For these large-scale integrated circuits, the failure rate is 0.091 percent per 1000 hours. This is equivalent to 0.0027 percent per 1000 hours in an operating environment of 55°C. The test conditions are $T_A = 85°C$ and relative humidity (RH) = 80% (table 6).

Table 6. High-Temperature and High-Humidity Life Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
2190	0	0	0	0	2
Total number of failures at 1K hrs	= 2				
Failure rate at 1K hrs at 85°C/80% RH	= 0.091% per 1K hrs				
Projected failure rate at 1K hrs at 55°C/60% RH	= 0.003% per 1K hrs				

High-Temperature Storage Life Test

This test is effective in accelerating the failure mechanisms related to mechanical reliability problems and process instability. For these LSI devices, the failure rate is 0.207 percent per 1000 hours at 125°C. This is equivalent to 0.0061 percent per 1000 hours in an operating environment of 55°C (table 7).

Table 7. High-Temperature Storage Life Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
2410	0	0	0	1	4
Total number of failures at 1K hrs	= 5				
Failure rate at 1K hrs at 125°C	= 0.207% per 1K hrs				
Projected failure rate at 1K hrs at 55°C	= 0.006% per 1K hrs				

Pressure Cooker Test

This test is effective in accelerating failure mechanisms related to metalization corrosion due to moisture. The failure rate is 0.52 percent per 1000 hours at T_A = 125°C and 2.3 atm at 100 percent humidity. This is equivalent to 0.0013 percent per 1000 hours at 55°C and an environment of 60 percent humidity (table 8).

Table 8. Pressure Cooker Test

Number of Samples	Number of Failures at 48 hrs	96 hrs	168 hrs	500 hrs	1K hrs
1718	0	4	5	No test performed	
Total number of failures at 168 hrs	= 9				
Failure rate at 125°C	= 0.54% per 1K hrs				
Projected failure rate at 55°C	= 0.001% per 1K hrs				

Life Test Data Summary

Table 9 summarizes the life test results and projected failure rates in the normal operating environment. The failure rate shows random distribution as opposed to a decreasing failure rate. This is a result of infant mortality screening.

Table 9. Life Test Data

Test Time	Number of Samples	Number of Failures at 96 hrs	168 hrs	500 hrs	1K hrs	Total Number of Failures
High-temperature life test	3317	0	1	4	3	8
High-humidity life test	2190	0	0	0	2	2
High-temperature storage life test	2410	0	0	1	4	5
Pressure cooker test	1718	4	5	No test performed		9
Total	9635	4	6	5	9	24

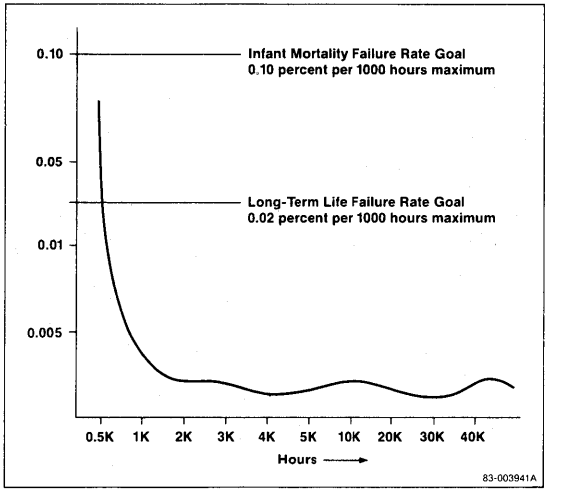
The projected failure rate in the normal operating environment is calculated assuming that the average activation energy is 0.7 eV.

Figure 3 shows the life distribution of NEC integrated circuits as a form of the bathtub curve.

This life test data shows improvements of approximately an order of magnitude better than NEC's goal. The hours of operation are equivalent to the normal operating environment. Wear-out failures, which had been the main target for reliability improvement, have also been significantly reduced. This result comes mainly from process improvements and stringent manufacturing process control.

NEC's main goal has been to improve reliability with respect to infant mortality and long-term life failures. This can be achieved by introducing an effective screening method for infant mortality and building quality into the product.

Figure 3. Plot of Life Test Results



Thermal Stress Tests

Temperature cycling and thermal shock test the thermal compatibility of material and metal used to make integrated circuits. Table 10 lists the reliability test results of thermal stress tests.

Table 10. Thermal Stress Tests

Test Item	Number of Samples	Number of Failures
Soldering heat test $T_A = 260°C$ for 10 seconds	1891	0
Temperature cycle $T_A = -65$ to $+150°C$, 10 cycles	1891	0
Thermal shock test $T_A = 0$ to $+100°C$, 15 cycles	1891	0

Mechanical Stress Tests

In addition to the device life test, NEC performs mechanical stress tests to detect reliability problems related to the package, material, and device susceptibility to an extreme environment. Table 11 lists mechanical stress test results.

Table 11. Mechanical Stress Tests

Test Item	Number of Samples	Number of Failures
Mechanical shock test at 15 kg, 3 axis	315	0
Vibration test at 100 Hz to 2 kHz, 20 g	315	0
Constant acceleration at 20 kg, 3 axis	315	0
Lead fatigue test at 240 grams	538	0
Solderability test at 230°C for 5 seconds	638	0

Built-In Quality and Reliability

As large-scale integration reaches even higher levels of density, simple quality inspections cannot assure adequate levels of product quality and reliability. In order to ensure the reliability of state-of-the-art VLSI, NEC has adopted another approach. Highest reliability and superior quality of a device can only be achieved by building these characteristics into the product at each process step. NEC, therefore, has introduced the notion of total quality control (TQC) into its entire semiconductor production line. Quality control is distributed into each process step and then summed to form a consolidated system.

Approaches to Total Quality Control

First, the quality control function is embedded into each process. This method enables early detection of possible causes of failure and immediate feedback.

Second, the reliability and quality assurance policy is an integral part of the entire organization. This enables a companywide quality control activity. At NEC, everyone in the company is involved with the concept and methodology of total quality control.

Third, there is an ongoing research and development effort to set even higher standards of device quality and reliability.

Fourth, extensive failure analysis is performed periodically and corrective actions are taken as preventive measures. Process control is based on statistical data gathered from this analysis.

The goal is to maintain the superior product quality and reliability that has become synonymous with the NEC name. The new standard is continuously upgraded and the iterative process continues.

Implementation of Distributed Quality Control

Building quality into a product requires early detection of possible causes of failure at each process step. Then, immediate feedback to remove the causes is a must. A fixed station quality inspection is often lacking in immediate feedback. It is, therefore, necessary to distribute quality control functions to each process step, including the conceptual stage. NEC has implemented a distributed quality control function at each step of the process. Following is a breakdown of the significant steps:

- Product development phase
- Wafer processing
- Chip mounting and packaging
- Electrical testing and thermal aging
- Incoming material inspection

Product Development Phase. The product development phase includes conception of a product, review of the device proposal, organization and physical element design, engineering evaluation, and finally, transfer of the product to manufacturing. Quality and reliability are considered at every step. More significantly, at the design review stage and prior to product transfer, the quality and reliability requirements have to be examined and determined to be satisfactory. This often adds 2 to 3 months to the product development cycle. Building in high reliability, however, cannot be sacrificed.

Wafer Processing Stage Inspection. The in-process quality inspections that occur at the wafer fabrication stage are listed in table 12.

Table 12. Wafer Processing Inspection

Process	Inspection Item
Wafer	Resistivity, dimension, and appearance, (lot sampling inspection)
Mask	
Photolithography	Alignment and etching (100% inspection)
Cleaning	
Diffusion and oxidation	Oxide thickness, sheet resistivity (lot sampling inspection)
Metalization and passivation	Thickness, V_{th}, C-V characteristics (lot sampling)
Wafer sort and scribe	Dc parameters (100% inspection)
Die sort	100% visual inspection

Chip Mounting and Packaging. The in-process quality inspections done at the chip mounting and packaging stage are listed in table 13.

Table 13. Chip Mounting and Packaging Inspection

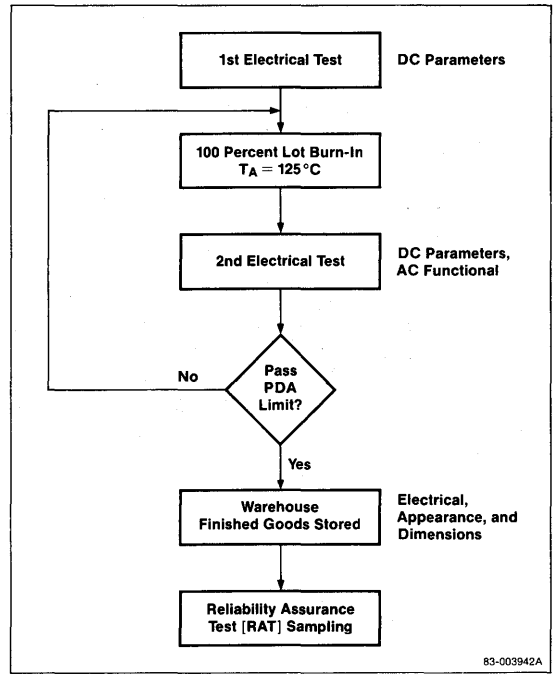
Process	Inspection Item
Die	Incoming material Inspection
Die attach	Appearance (lot sampling inspection)
Wire bonding	Bond strength, appearance (lot sampling)
Packaging	100% appearance inspection
Fine leak*	Lot sampling
Gross leak*	100% inspection

*For ceramic package devices only.

Electrical Testing and Screening. Electrical testing and infant mortality screening are performed at this stage. A flowchart of the process is depicted in figure 4.

At the first electrical test, dc parameters are tested according to the electrical specifications on 100% of each lot. This is a prescreening prior to the infant mortality test. At the second electrical test, ac functional tests as well as dc parameter tests are performed on 100% of the subjected lot. If the percentage of defective units exceeds the limit, the lot is subjected to an additional burn-in. During this time, the defective units are undergoing a failure analysis, the results of which are then fed back into the process for corrective action.

Figure 4. Electrical Testing and Screening



Incoming Material Inspection. Prior to warehouse storage, lots are subjected to an incoming inspection according to the following sampling plan.

- Electrical test: Dc parameters LTPD 3%
  Functional test LTPD 3%
- Appearance LTPD 3%

Reliability Assurance Test

Samples are continually taken from the warehouse and subjected to monthly reliability tests as discussed previously. They are taken from similar process groups so that it can be assumed that any device is representative of the reliability of the group.

In-Process Screening

Perhaps the most significant preventive measure that NEC has implemented is the introduction of 100% burn-in as an integral part of the standard production process. Most of the potential infant failures are effectively screened from every lot, thereby improving reliability. Assuming average activation energy of 0.7 eV, burn-in at $T_A = 125\,°C$ for 4 hours is equivalent to a week's operation in a normal operating environment. This appears to be ample time for accelerating the time-to-failure mechanisms for early failures.

Process automation, as previously mentioned, has also contributed a great deal toward improving reliability. Since its introduction, assembly related failure mechanisms have been substantially reduced. And, in combination with in-process screening and materials improvement, it has helped establish quality and reliability above NEC's initial goals.

Summary and Conclusion

As has been discussed, building quality and reliability into products is the most efficient way to ensure product reliability. NEC's approach of distributing quality control functions to process steps, then forming a consolidated quality control system, has produced superior quality and excellent reliability.

Prescreening, introduced as an integral part of large-scale integrated circuit protection, has been a major factor in improving reliability. The most recent year's production clearly demonstrates continuation of NEC's high reliability and the effectiveness of this method.

Reliability assurance tests (RATs), performed monthly, have ensured high outgoing quality levels. The combination of building quality into products, effective prescreening of potential failures, and the reliability assurance test has established a singularly high standard of quality and reliability for NEC's large-scale integrated circuits.

With a companywide quality control program, NEC is committed to building superior quality and highest reliability into all its products. Through continuous research and development activities, extensive failure analysis, and process improvements, a higher standard of quality and reliability will continuously be set and maintained.

NEC

4-BIT, SINGLE-CHIP MICROCOMPUTERS

3

Section 3 — 4-Bit, Single-Chip Microcomputers

FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

Description

The μPD7500 series of 4-bit, single-chip CMOS microcomputers is a broad product line of devices designed for a variety of applications; for example, electronic games, home electronic products such as the VCR, and electronic automotive devices. To this end, more than 25 products based on the μPD7500 evaluation chip have been designed with various combinations of memory size, number of I/O ports, output drive capability, type of display driver/ controller (LCD or FIP®), oscillators, package type (DIP, shrink DIP for ease of handling, flat for high-density installations, QUIP), and more. Because the μPD7500 series products have hardware and software in common, systems are easily upgraded.

The μPD7500 series uses a low-power CMOS design. As an example, the current consumption of the μPD7508C operating at 5 V is typically 300 μA (at 10 μs, 200 kHz). In standby mode at 3 V, current consumption is reduced to 0.3 μA (typ). This feature is most suitable for systems requiring battery backup or for battery-powered devices that must operate for long periods.

The wide operating voltage range of the series allows systems to be configured with normal operation at 5 V ±10% and battery backup operation at 3 V. In particular, the μPD7507S can run at 2.2 V, and systems using this device need only a single lithium battery, thus reducing the overall system cost.

Although the normal operating temperature range is −10 to +70°C, products in the μPD7500 series can operate from −40 to +85°C and −40 to +110°C in accordance with the user's request. This is useful in automotive and outdoor applications.

Table 1 lists the μPD7500 series products and features, and figure 1 shows the different development directions of the series. Within each of these directions, the memory sizes have been serialized. For example, in the product group with built-in LCD controllers, the μPD7501 has a 1K-byte ROM, the μPD7502 has a 2K-byte ROM, and the μPD7503 has a 4K-byte ROM. (Note also that the μPD7502 and μPD7503 are pin compatible; software developed on the μPD7502 can be used without modification on the μPD7503. Except LAMT instruction for μPD7502 only and LAMTL instruction for μPD7503 only.)

The many kinds of peripheral hardware (such as display controllers/drivers) that are built into the members of the series can significantly reduce the cost of a system. One common hardware feature is an 8-bit timer, which easily provides a clock function. With the exception of the μPD7506/7556/7566, all products of the series incorporate an 8-bit serial I/O, so that developing multiprocessor systems or connecting peripheral devices is easier. The μPD7533 offers a 4-channel, 8-bit A/D converter.

Piggyback products, such as the μPD75CG08, are available and can be used as a final check of functions during system development, preproduction, and small volume production.

The same support tools can be used for the entire series, thus helping to reduce system development cost.

Table 2 lists the package types applicable to each chip in the μPD7500 series.

FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

Table 1. μPD7500 Series Product List

Product (μPD)	Features	Clock Osc	ROM (x8)	RAM (x4)	I/O	Power Supply
7500H	EVACHIP, high speed (2.86 μs)	RC	8K (External)	256	46	5 V ±10%
7500H-E	EVACHIP	RC	8K (External)	256	46	5 V ±10%
7501	LCD controller/driver, 24-segment	RC	1K	96	24	2.5 to 6.0 V
7502	LCD controller/driver, 24-segment	RC	2K	128	23	2.5 to 6.0 V
7503	LCD controller/driver, 24-segment	RC	4K	224	23	2.5 to 6.0 V
7514	LCD controller/driver, 32-segment	RC	4K	256	31	2.7 to 6.0 V
7507S	General purpose, low voltage	RC	2K	128	20	2.2 to 6.0 V
7507	General purpose	RC	2K	128	32	2.5 to 6.0 V
7508	General purpose	RC	4K	224	32	2.5 to 6.0 V
7507H	General purpose, high speed (2.86 μs)	Xtal/Cer	2K	128	32	2.7 to 6.0 V
7508H	General purpose, high speed (2.86 μs)	Xtal/Cer	4K	224	32	2.7 to 6.0 V
7506	General purpose	R	1K	64	22	2.5 to 6.0 V
7554	LED direct drive, mask option ports, serial I/O	R	1K	64	16	2.5 to 6.0 V
7564	LED direct drive, mask option ports, serial I/O	Ceramic	1K	64	15	2.5 to 6.0 V
7556	LED direct drive, mask option ports, 4-channel comparator	R	1K	64	20	2.5 to 6.0 V
7566	LED direct drive, mask option ports, 4-channel comparator	Ceramic	1K	64	19	2.5 to 6.0 V
7527A	P-ch, high-voltage output ports for FIP driver; high speed (3.3 μs)	RC	2K	128	35	2.7 to 6.0 V
7537A	P-ch, high-voltage output ports for FIP driver; high speed (3.3 μs)	Ceramic	2K	128	35	2.7 to 6.0 V
7528A	P-ch, high-voltage output ports for FIP driver; high speed (3.3 μs)	RC	4K	160	35	2.7 to 6.0 V
7538A	P-ch, high-voltage output ports for FIP driver; high speed (3.3 μs)	Ceramic	4K	160	35	2.7 to 6.0 V
7508A	P-ch, high-voltage output ports for FIP driver	RC	4K	208	32	2.7 to 5.5 V
7519	FIP controller/driver	Xtal	4K	256	53	2.5 to 6.0 V
7519H	FIP controller/driver; high speed (2.44 μs)	Xtal	4K	256	53	2.5 to 6.0 V
7516H	FIP controller/driver; high speed (2.44 μs)	Xtal	6K	256	53	2.5 to 6.0 V
7533	LED driver; 4-channel A/D converter	Ceramic	4K	160	30	3.0 to 6.0 V
75CG08	Piggyback; for 7507/08	RC	4K	224	32	5 V ±10%
75CG08H	Piggyback; for 7507H/08H	Xtal/Cer	4K	224	32	5 V ±10%
75CG19	Piggyback; for 7519	Xtal	4K	256	53	5 V ±10%
75CG19H	Piggyback; for 7519H	Xtal	4K	256	53	5 V ±10%
75CG16H	Piggyback; for 7516H	Xtal	6K	256	53	5 V ±10%
75CG28	Piggyback; for 7527A/28A	RC	4K	160	35	5 V ±10%
75CG38	Piggyback; for 7537A/38A	Ceramic	4K	160	35	5 V ±10%
75CG33	Piggyback; for 7533	Ceramic	4K	160	30	5 V ±10%

Figure 1. μPD7500 Series Product Classification

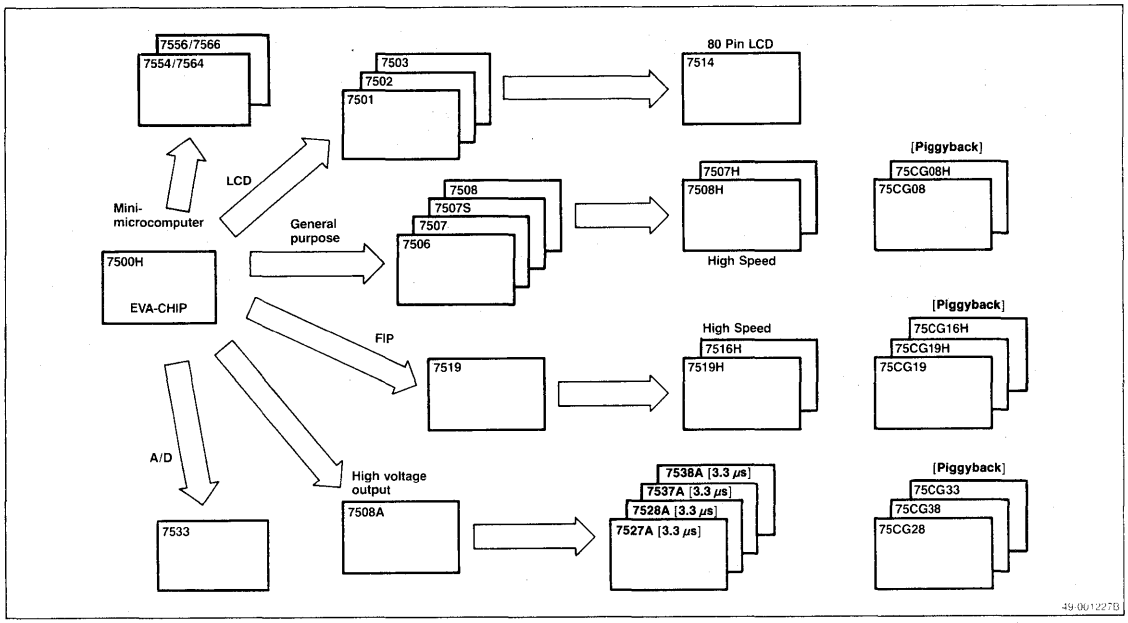


Table 2. Applicability of Packages

Product (μPD)	Package
7500H, 7500H-E	64 QUIP
7501	64 miniflat
7502, 7503	64 miniflat
7506	28 DIP or SDIP; 52 miniflat
7507, 7508	40 DIP or SDIP; 52 miniflat
75CG08	40 ceramic piggyback DIP
7507H, 7508H	40 DIP or SDIP; 44 miniflat
75CG08H	40 ceramic piggyback DIP
7507S	28 DIP or SDIP
7508A	40 DIP
7514	80 miniflat
7516H	64 miniflat, QUIP, or SDIP
75CG16H	64 ceramic piggyback QUIP
7519, 7519H	64 miniflat, QUIP, or SDIP
75CG19, 75CG19H	64 ceramic piggyback QUIP

Product (μPD)	Package
7527A, 7528A	42 DIP or SDIP
75CG28	42 ceramic piggyback DIP
7533	42 DIP, SDIP, or 44 miniflat
75CG33	42 ceramic piggyback DIP
7537A, 7538A	42 DIP or SDIP
75CG38	42 ceramic piggyback DIP
7554, 7564	20 SDIP or SO package
7556, 7566	24 SDIP or SO package

Note:

(1) For ordering information, including package codes, refer to the applicable data sheet.

(2) Packages are plastic unless otherwise specified.

3

Applications

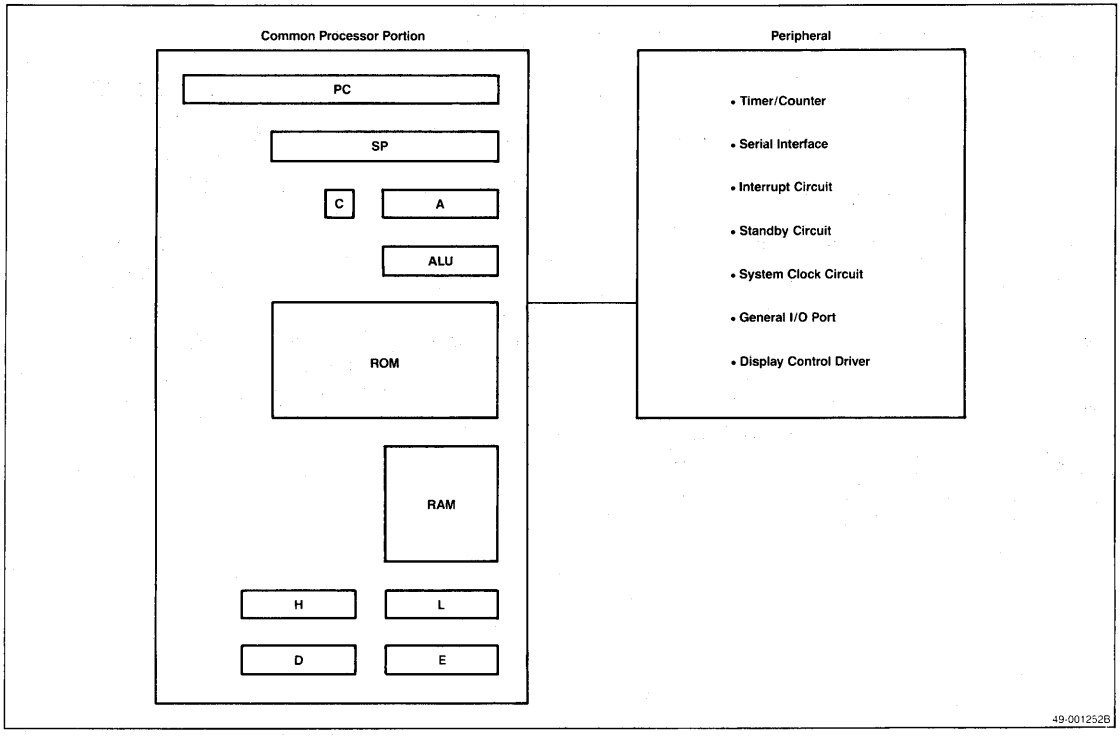
7500 series products with a built-in LCD controller:
- Electronic game
- Automotive device (dashboard display)
- Phone
- VCR (timer)
- Camera
- Calculator
- Electronic musical instrument
- Measuring equipment
- Medical device (blood pressure gauge)
- Water, gas, or electric meter
- Pager
- PPC
- Data terminal

7500 series general-purpose products:
- VCR
- Phone
- Automobile
- ECR
- Record player
- Transceiver
- PPC
- Cassette

7500 series products with built-in high-voltage outputs:
- VCR
- ECR
- Microwave oven
- Electronic game
- Scanner
- Trip computer

7500 series products with a built-in LED controller/driver:
- Electronic game
- Deck controller
- Refrigerator
- Cooking appliance
- Washing machine

Block Diagram



Functional Description

A μPD7500 series microcomputer consists of the following:

- Program counter (PC)
- Accumulator (A)
- Program status word (PSW)
- Arithmetic logic unit (ALU)
- General-purpose registers (H, L, D, E)
- Program memory (ROM)
- Data memory (RAM)

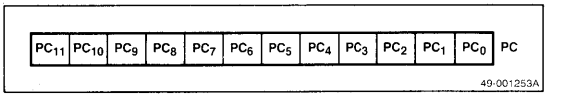
The peripheral hardware includes the following:

- Timer/counter
- Serial interface
- Interrupt circuit
- Standby circuit
- System clock oscillation circuit
- General-purpose I/O
- Display controller/driver

Program Counter [PC]

The program counter (figure 2) is a binary counter that generates a 12-bit address. The bit length of the PC will vary depending on the ROM size for the particular device. The μPD7516H and μPD7500H/H-E, which contain more than 4K-bytes of memory, access upper memory by setting bit 1 of the program status word (BNK flag) to 1.

Figure 2. Program Counter Structure



When an instruction executes, the PC increments by the number of bytes in the instruction.

When a jump instruction (JMP, JCP, JAM) executes, either immediate data or the contents of the accumulator and data memory, which show a jump destination, are loaded into some or all bits of the PC.

While a call instruction is executing (CALL, CALT) or at an interrupt occurrence, the contents of the PC (the return address already incremented to designate the next instruction) are stored in stack memory. A proper address is then loaded into the PC.

While a return instruction is executing (RT, RTS, RTPSW), the contents of stack memory are loaded into the PC.

The RESET instruction clears the PC to 0.

3

Stack Pointer [SP]

The stack area for the μPD7500 series resides in data memory. The stack depth can be as large as the maximum size of RAM, since the stack pointer is user programmable.

The stack pointer is an 8-bit register (SP_7-SP_0) that stores the stack's top address for the area in data memory used as an LIFO stack. The SP decrements when a call (CALL, CALT) or push (PSHDE, PSHHL) instruction executes and at an interrupt generation. It increments when a return (RT, RTS, RTPSW) or pop (POPDE, POPHL) instruction executes.

To determine the stack area, the SP must be initialized by the TAMSP instruction. However, when TAMSP executes, 0 (zero) is unconditionally loaded into SP_0. Because the SP decrements before a stack instruction executes, the top of the stack will always begin at an odd memory location. Thus the initial value of the SP should be set to the top of the stack (odd) plus one (set to an even value). To set the most significant address of the stack area to FFH, the initial value of the SP should be 00H.

Although TSPAM may read the SP at any time, it cannot read the contents of SP_0; 0 is unconditionally stored in bit 0 of data memory. See figure 2 and table 3.

Figure 3. Data Movement at Execution of TAMSP and TSPAM

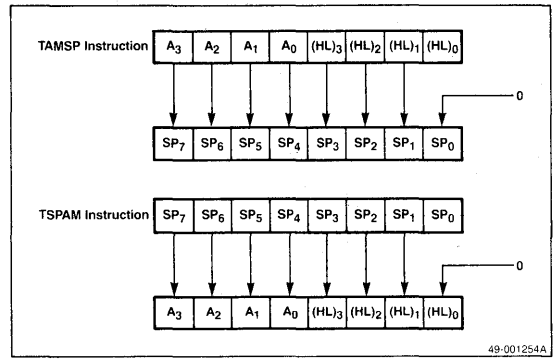


Table 3. Stack Memory Push/Pop Operation

Process Order	CALL, CALT Interrupt	RT, RTS	RTPSW	PSHDE, PSHHL	POPDE, POPHL
1	(SP − 1) ← PCM	PCH ← (SP)	PCH ← (SP)	(SP − 1) ← D/H	E/L ← (SP)
2	(SP − 2) ← PCL	PCL ← (SP + 2)	PSW ← (SP + 1)	(SP − 2) ← E/L	D/H ← (SP + 1)
3	(SP − 3) ← PSW	PCM ← (SP + 3)	PCL ← (SP + 2)	SP ← SP − 2	SP ← SP + 2
4	(SP − 4) ← PCH	SP ← SP + 4	PCM ← (SP + 3)		
5	SP ← SP − 4		SP ← SP + 4		

Note:

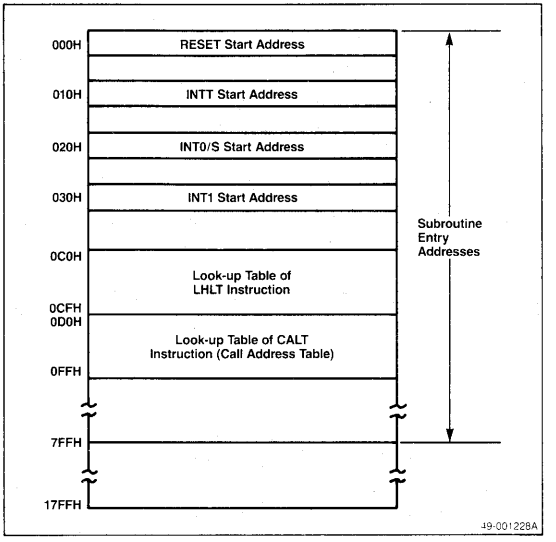
(1) PCH = PC_{11}-PC_8
PCM = PC_7-PC_4
PCL = PC_3-PC_0

Program Memory [ROM]

Program memory is a mask-programmable ROM of 6144 words x 8 bits (maximum). It stores programs and table data, and is addressed by the PC. (See figure 4.) ROM address locations are from 000H to 17FFH.

Specific fixed address locations are allocated to RESET and interrupt start addresses and the table areas of the LHLT and CALT instructions. Consideration of these locations in program memory should be taken in preparing a program.

Figure 4. Program Memory Map



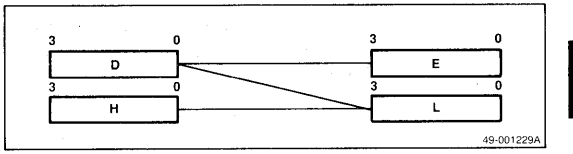
General-Purpose Registers

The four 4-bit general-purpose registers D, E, H, and L either operate in units of 4 bits, or can form the 8-bit pair registers DE, DL, and HL (D or H is the upper-order 4 bits, and E or L is the lower-order 4 bits) to be used as data pointers.

When pair register HL operates as a data pointer, it can perform automatic increment and decrement for the L register only. (See figure 5.) The L register is also used to specify I/O ports and mode registers when the I/O instruction (OPL, IPL) is executed.

The μPD7501/06/27/28/33/37/38/54/64/56/66 do not contain DE registers.

Figure 5. General-Purpose Register Configurations



3

Data Memory [RAM]

Data memory is a static RAM of 256 words x 4 bits (maximum). It is used to store processing data and display data. It also operates with the accumulator to process data in 8-bit units.

There are three types of data memory addressing:

- Direct, performed by the second byte of the instruction
- Register indirect, performed indirectly by the contents of the pair register designated by an instruction
- Stack indirect, performed by the contents of the SP

Locations 00 to 3FH are used for display memory devices μPD7516H/19H, so these locations cannot be used for stack area. Locations 00 to 17H (1FH for the μPD7514) are used for display memory devices μPD7501/02/03/14, so these locations cannot be used for stack area. See figure 6.

Valid stack area is used during execution of the instructions CALL, CALT, RT, RTS, RTPSW, PSHDE, PSHHL, POPDE, and POPHL. At the execution of a call instruction or an interrupt occurrence, the contents of the PC and PSW are stored in the stack area. At the execution of a push instruction, the contents of DE or HL are stored in the stack. See figure 7.

Figure 6. Data Memory Map

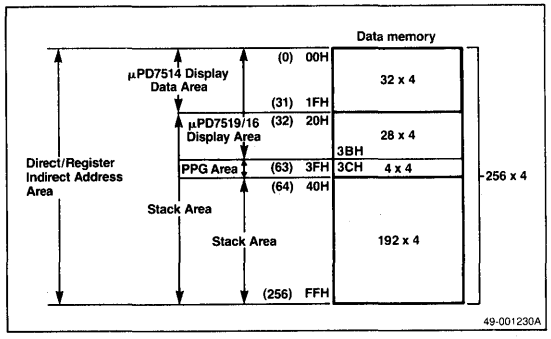
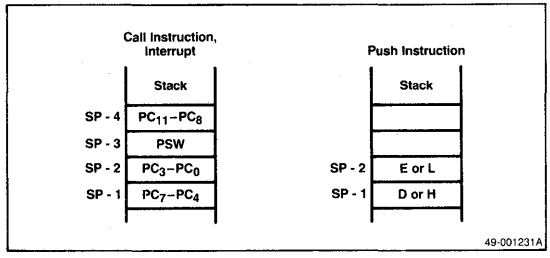


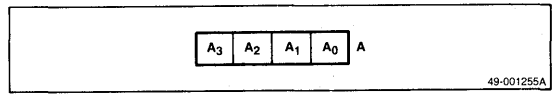
Figure 7. Stack Contents After Call, Interrupt, or Push



Accumulator [A]

The accumulator is a 4-bit register that performs various arithmetic/logical operations. Operating with data memory addressed by pair register HL, data processing may be done in 8-bit units (higher-order bits in the accumulator and lower-order bits in data memory). See figure 8.

Figure 8. Accumulator Configuration



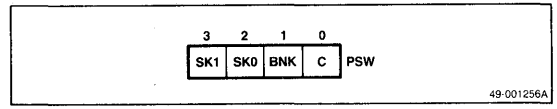
Arithmetic Logic Unit [ALU]

The ALU is a 4-bit arithmetic logic circuit that performs such processes as binary addition, arithmetic/logical operation, comparison, and rotation.

Program Status Word [PSW]

The 4-bit PSW consists of two skip flags (SK1, SK0) and a carry flag (C), as shown in figure 9.

Figure 9. Structure of Program Status Word



The contents of the PSW are automatically stored in the stack area at an execution of a call instruction (CALL, CALT) or at an interrupt occurrence, and are restored by an RTPSW instruction. The BNK flag is used in the μPD7500H/H-E and 7516H to access high memory.

At RESET, SK1 and SK0 are cleared to 0, and C is undefined.

Skip Flags [SK1, SK0]. The skip flag is used to hold the following skip states:

- String effect of an LAI instruction
- String effect of an LHLI or LHLT instruction
- Skip condition accomplished by instructions other than string effect

The skip flag is automatically set and reset when an instruction is executed.

Carry Flag [C]. This flag can be generated only by the addition instruction (ACSC). If a carry is generated from bit 3 of the ALU, the carry flag is set to 1. If a carry is not generated, the carry flag is reset to 0.

The carry flag is set to 1 by the SC instruction and reset to 0 by the RC instruction. Its contents are tested by the SKC instruction. The carry bit is rotated into the high bit of the accumulator by the rotation instruction (RAR).

System Clock Generator

The system clock (CL) is generated by one of the five types of oscillators listed in table 4. The CPU clock (ϕ) is derived from CL by frequency division.

Table 4. μPD7500 Series System Clock (CL) and CPU Clock (ϕ)

Product (μPD)	ϕ/CL Frequency Ratio	Oscillator Type	Stop Mode Released by
7500H, 7500H-E 7501 7502 7503 7514 7507, 7507S 7508, 7508A 7527A 7528A	1/2	RC	Interrupt or RESET
7506 7554 7564 7556 7566	1/2	R	Interrupt or RESET
7507H 7508H	1/12	Crystal/ceramic 1.0 to 4.2 MHz	RESET (Note 1)
7519 7519H 7516H	1/32 or 1/64 1/16 or 1/64 1/16 or 1/64	Crystal 4.19 to 6.55 MHz (7519 4.19 MHz max)	RESET
7537A 7538A 7533	1/2	Ceramic	RESET

Note:

(1) RESET pulse width provides time for oscillation stabilization.

3

RC Oscillator

The system clock generator (figure 10) consists of an RC oscillator and a half-frequency divider. The RC oscillator is controlled by an external resistor (R) and capacitor (C) connected to CL1 and CL2.

An external clock can be input to the CL1 pin without using an RC circuit. Pin CL2 should be left open. In this case, the RC oscillator merely operates as an inverting buffer.

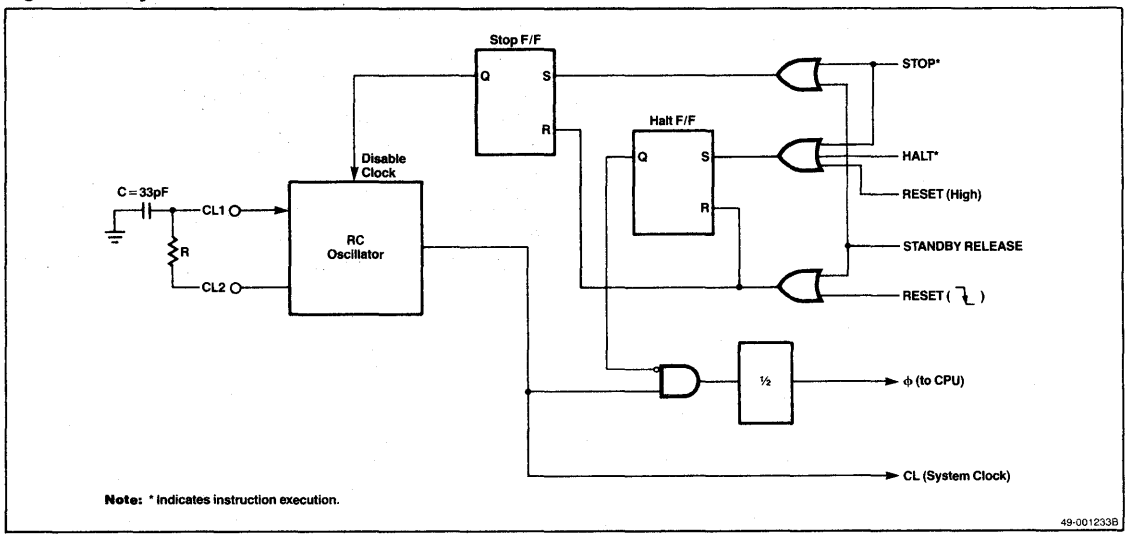
The frequency of CL is the RC oscillation frequency of the CL1 input clock frequency. The RC oscillator output is frequency divided by 2 to become the CPU clock (ϕ), which is sent to the CPU and the serial interface.

Using the standby circuit, the RC oscillator and the half-frequency divider are stopped in the stop mode, thereby stopping the output of CL and ϕ. In halt mode, only the half-frequency divider is stopped, so that ϕ stops but CL continues to be supplied.

Not shown in figure 10, the RC oscillator output (CL) is sent to a clock control circuit, and then frequency divided to become a count pulse (CP) for the timer/event counter.

If an external clock is used, the CL1 input clock becomes CL via an inverting buffer, so the supply of CL does not stop even in stop mode. Thus, both stop mode and halt mode stop only the half-frequency divider. In both modes, only the output of ϕ is stopped.

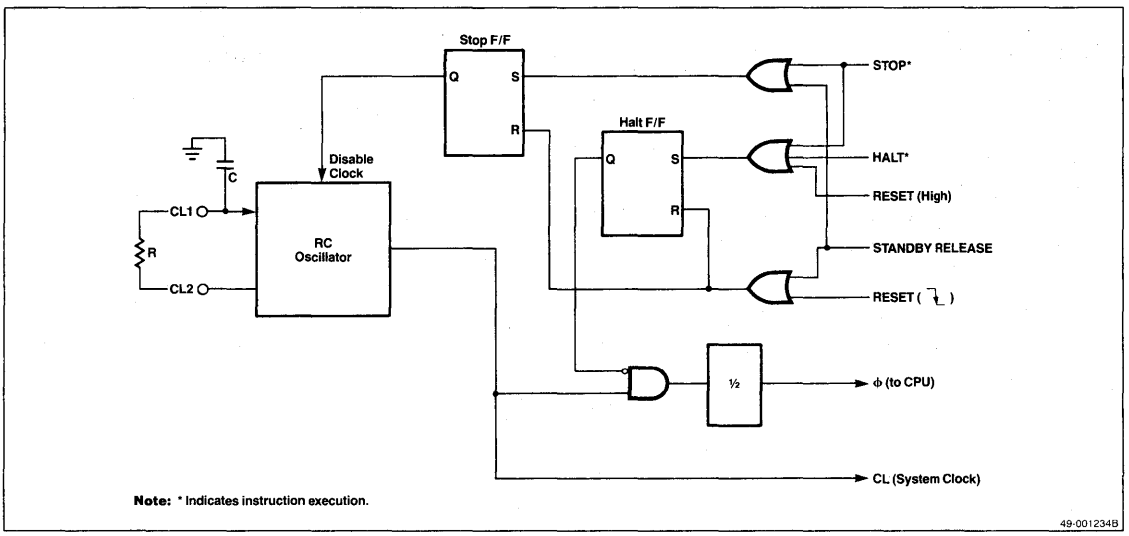
Figure 10. System Clock Generator; RC Oscillator



R Oscillator

In this circuit, the resistor is external and the capacitor is internal. See figure 11.

Figure 11. System Clock Generator; R Oscillator



Crystal/Ceramic Oscillator

This clock generator provides stable high-speed operation. The circuit (figure 12) consists mainly of a crystal oscillator circuit, several frequency dividers, and a control circuit for standby (halt/stop) modes.

The crystal oscillator operates at the fundamental crystal frequency, typically 4.19 MHz. Or, a ceramic resonator (typically 4.0 MHz) may be connected between the CL1 and CL2 pins. Or, an external clock may be input at CL1, in which case the crystal oscillator operates as an inverting buffer.

The frequency divider generates several kinds of clocks by dividing the crystal/ceramic oscillation frequency (f_{CC}) or the external clock frequency (f_C), where f_{CC} or f_C = 4.19 MHz, as follows:

- System clock (CL): $f_{CC}/6$ or $f_C/6$ (698 kHz)
- CPU clock (ϕ) and output clock (ϕ_{OUT}): $f_{CC}/12$ or $f_C/12$ (349 kHz):
- Timer/event counter clock: $f_{CC}/8$ or $f_C/8$ (524 kHz)

System clock CL is supplied to the timer/event counter, the clock synchronizing the gate of the INT1 interrupt input, etc.

The standby mode control circuit is mainly composed of a stop flip-flop and a halt flip-flop. See figures 12 and 13.

The STOP instruction sets the stop flip-flop to the stop mode, in which crystal oscillation and all clock supplies are stopped. A high input to RESET resets the stop flip-flop, and crystal oscillation starts again. When RESET goes low, the supply for each clock restarts.

Figure 13. Stop Mode Timing

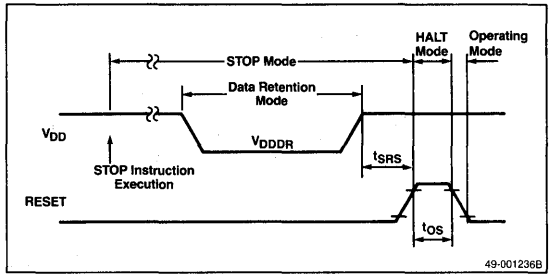
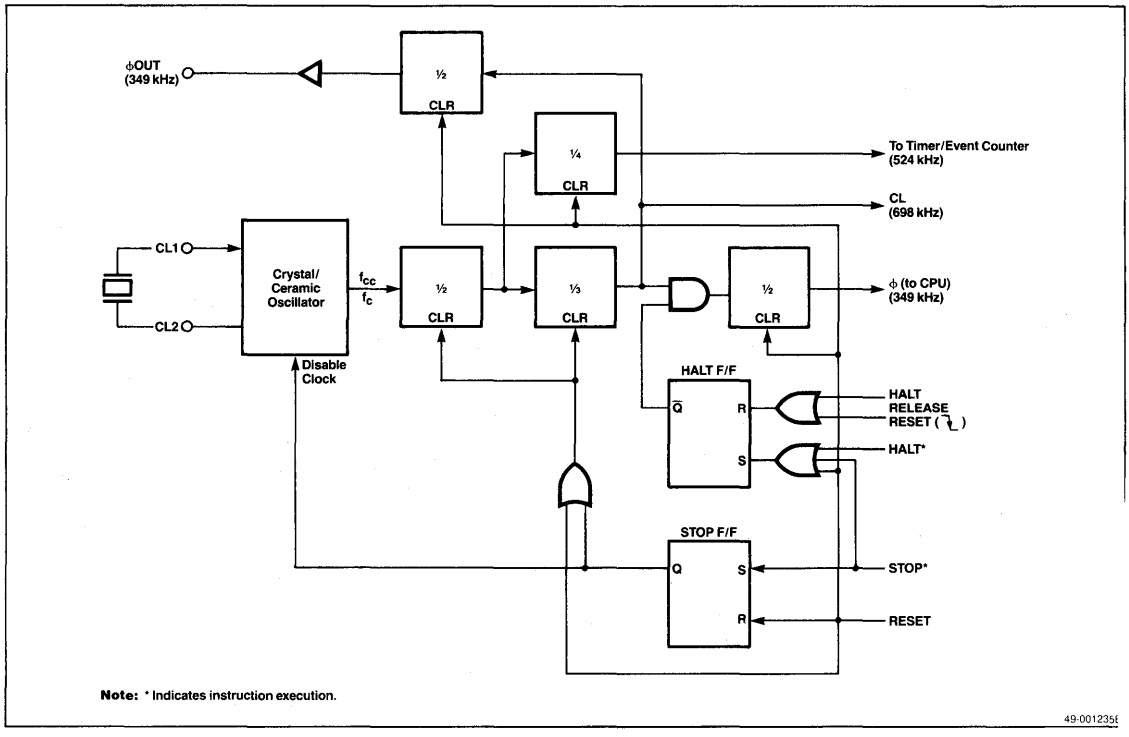


Figure 12. System Clock Generator; Crystal/Ceramic Oscillator



The HALT instruction sets the halt flip-flop to halt mode. In this mode, input from the half-frequency divider that generates the CPU clock is inhibited and the CPU clock is stopped. The halt flip-flop is reset either by the RELEASE signal, which becomes active when the interrupt request flag is set, or at the falling edge of the RESET signal. The supply to the CPU clock restarts.

Crystal Oscillator

This clock generator (figure 14), applicable to 7516H, 7519, and 7519H, consists of a crystal oscillator, a frequency divider, and a standby (halt/stop) mode control circuit. The crystal (for example, 6.55 MHz is 4.19 MHz) is connected to pins X1, X2. (The μPD7519 is 4.19 MHz only).

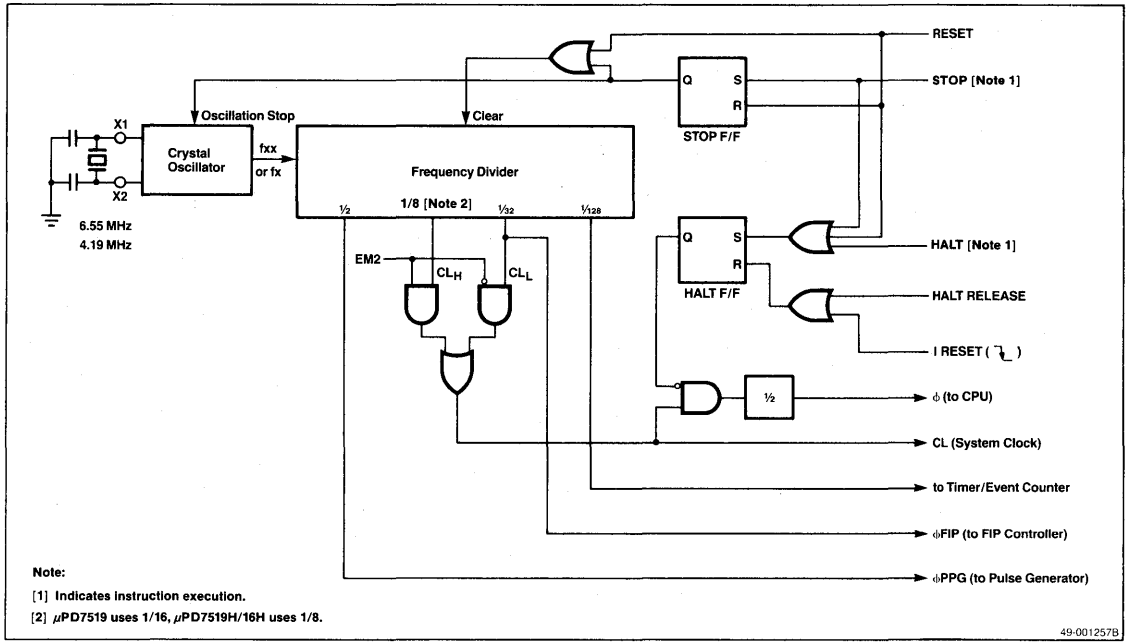
It is also possible to operate with an external clock input at X1. In this case, the crystal oscillator acts merely as an inverting buffer.

The frequency divider divides the output of the crystal oscillator (f_{XX} for crystal oscillation, and f_X for the external clock) to the following values:

- 1/2 for pulse generator clock ϕ_{PPG}
- 1/8 for system clock CLH (μPD7519H/16H)
- 1/16 for system clock CLH (μPD7519)
- 1/32 for system clock CLL and FIP controller clock ϕ_{FIP}
- 1/128 for the timer/event counter clock.

3

Figure 14. System Clock Generator; Crystal Oscillator



The 1/8 and 1/32 frequency-divided outputs are available as system clock sources. If expansion mode register bit 2 (EM_2) is 1, 1/8 is selected; if it is 0, 1/32 is selected. (Note: For μPD7519, the divisor is 1/16 instead of 1/8.) In systems where high-speed processing is not required, or in part of a program that does not require high-speed processing, power consumption can be held to a minimum with the 1/32 frequency-divided low-speed clock. It is necessary to use the low-speed clock when using a supply voltage that is too low to allow operation with a high-speed clock.

System clock selection via EM2 does not apply to ϕ_{FIP} (FIP controller clock) or ϕ_{PPG} (pulse generator clock).

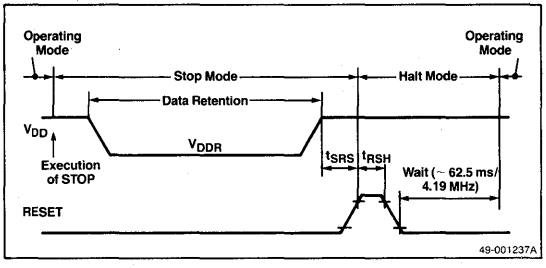
The ϕ_{FIP} clock is always 1/32 times the input frequency; the ϕ_{PPG} clock is always half the input frequency.

The system clock is half-frequency divided to be a CPU clock, ϕ. Also, the system clock becomes an input of the clock control circuit, which generates a count pulse (CP) of the timer/event counter.

The standby mode control circuit consists mainly of the stop and halt flip-flops. The STOP instruction sets the stop flip-flop, which stops crystal oscillation and clears the frequency divider circuit. All output from the frequency divider circuit stops; the system is in stop mode. A RESET input clears the stop flip-flop and starts crystal oscillation and the frequency dividing operation.

The HALT instruction sets the halt flip-flop. This inhibits the input of the half-frequency divider from generating a CPU clock ϕ, thereby causing the CPU clock to be halted (halt mode). The halt flip-flop is also set when the STOP instruction executes and when RESET is input, so that the flip-flop performs the same operation as that in halt mode. The flip-flop is reset at the falling edge of either the RELEASE signal (which becomes active when any one interrupt flag is set) or the internal reset (IRESET) signal (which is released after a certain waiting time following the release of the RESET input), thereby starting the supply of ϕ. See figure 15.

Figure 15. Release of Stop Mode



Ceramic Oscillator

This circuitry (figure 16) consists of a ceramic oscillator, half-frequency divider, control circuit for standby (halt) mode, etc. The oscillator frequency is set by a ceramic resonator connected to pins CL1 and CL2. Or, an external clock may be input at CL1. In this case, the oscillator operates as an inverting buffer. Output from the oscillator is used as the system clock (CL), which is divided into a CPU clock ϕ (1/2 CL).

The standby mode control circuit consists mainly of the halt flip-flop. When this flip-flop is set, input of the half-frequency divider is inhibited from generating the CPU clock ϕ, thereby causing the CPU clock to be halted (halt mode). This flip-flop is reset either by the RELEASE signal, which becomes active when one interrupt request flag is set, or by the falling edge of the RESET input. The supply of the ϕ clock then begins.

The halt flip-flop is also set when the RESET input is active. At power-on reset, RESET goes high and then the ceramic oscillator is driven. After a short time, the oscillation output becomes stable. So that an unstable clock does not cause the CPU to misoperate, the halt flip-flop inhibits the CPU clock as long as RESET is high level. Thus, the high-level pulse width for the RESET input should be wide enough to cover the required time for oscillator stabilization.

Count Clock Generator Circuit

This crystal oscillator (figure 17) is fed either by the crystal connected to pins X1 and X2, or by an external clock connected to X1 (in which case it operates as an inverting buffer). The output X is sent to the clock control circuit, either directly or after being frequency divided, in order to become a count pulse (CP) for the timer/event counter. The frequency of X is equivalent to the crystal oscillation frequency or the X1 external clock frequency. This circuit is not affected by standby (halt/stop) mode.

The count clock oscillator generates frequencies between 25 and 50 kHz. Figures 18 and 19 illustrate the frequency error (ppm) vs. temperature and capacitance.

Figure 16. System Clock Generator; Ceramic Oscillator

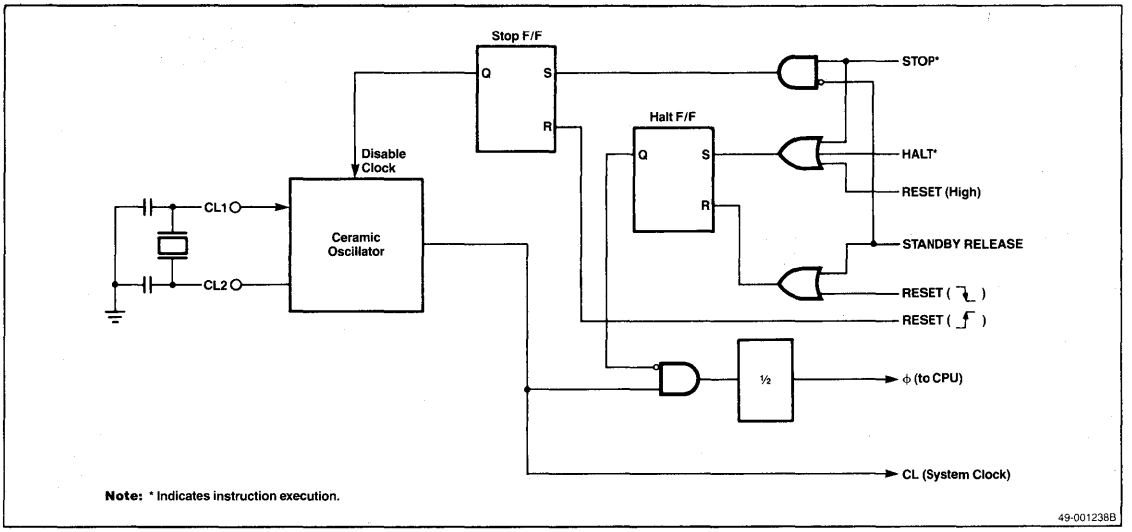


Figure 17. Count Clock Generator

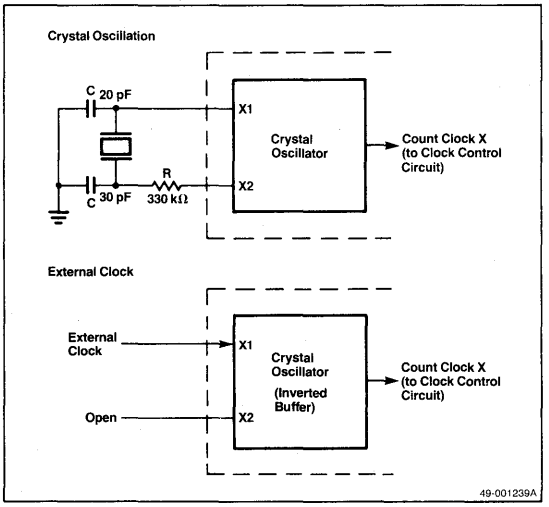


Figure 18. Temperature Dependence of Count Clock Frequency

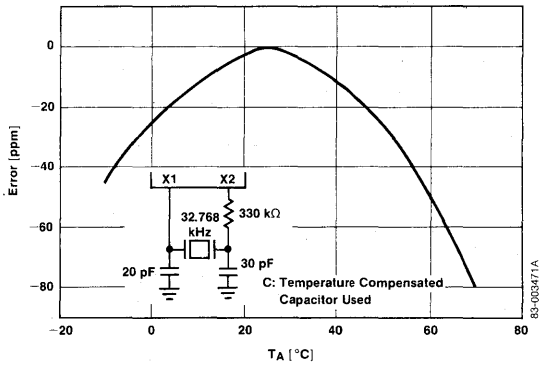
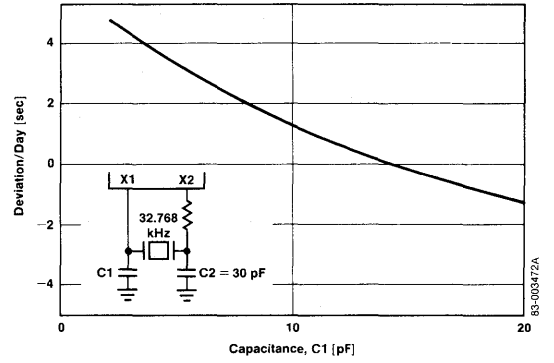


Figure 19. Capacitance (C1) Dependence of Count Clock Frequency



3

I/O Ports

Input and output buffers (figure 20) are classified as types A through I. Table 5 shows the applicability of each type to the 7500 series. For example, on the μPD7506, port $P0_0$ is a type B input buffer and $P0_3$ is a type A input buffer; $P0_1$ and $P0_2$ are not used. (Part numbers in table 5 are abbreviated; thus, μPD7506 becomes "06".)

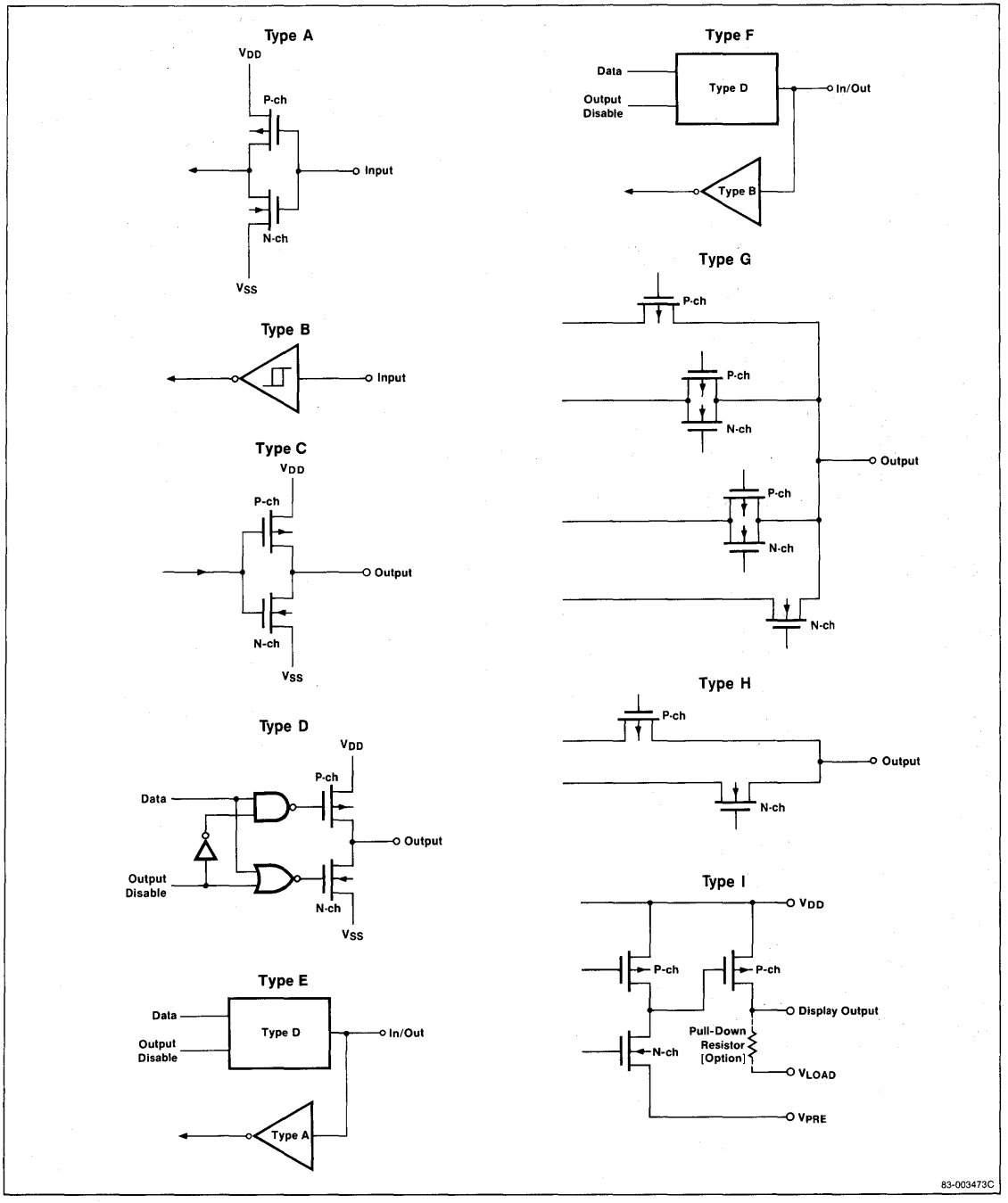
Table 5. μPD7500 Series I/O Buffer Configurations

Port	00H/00HE	06	02/03	07/07S/07H/08/08H/01/14/19/19H/16H
$P0_0$	A	B	—	B
$P0_1$	F	—	F	F
$P0_2$	E	—	E	E
$P0_3$	B	A	B	B
Port	**01**	**02/03**		**00H/00HE/06/07/07H/08/08H/14/19/19H/16H**
$P1_0$	B	B		E
$P1_1$	A	A		E
$P1_2$	A	A		E
$P1_3$	A	A		E
Port				**00H/00HE/06/07/07S/07H/08/08H/14/19/19H/16H**
$P2_0$-$P2_3$				D
Port				**00H/00HE/01/02/03/07/07S/07H/08/08H/14/19/19H/16H**
$P3_0$-P_3				D
Port				**00H/00HE/01/02/03/06/07/07S/07H/08/08H/14/19/19H/16H**
$P4_0$-$P4_3$				E
Port				**00H/00HE/01/02/03/06/07/07S/08/08H/14/19/19H/16H**
$P5_0$-P_3				E

Table 5. μPD7500 Series I/O Buffer Configurations (cont)

Port			00H/00HE/01/02/03/06/07/07H/08/08H/14/19/19H/16H
$P6_0$-$P6_3$			E
Port			**00H/00HE/07/07H/08/08H/14**
$P7_0$-$P7_3$			E
Port	**00H/00HE**	**06**	**01/02/03/07/07S/07H/08/08H/14/19/19H/16H**
INT0	B	B	B
INT1	B	—	B
INT2	B	—	—
RESET	B	B	B
Port	**07H/08**		**19/19H/16H**
EVENT	B		B
ϕOUT	C		—
Port			**19/19H/16H**
PPO			D
Port			**01/02/03/14**
COM_0-COM_3			G
S_0-S_{23}			H
Port			**14**
S_{24}-S_{31}			H
Port			**19/19H/16H**
S_0-S_7			I
T_8/S_8-T_{15}/S_{15}			I
T_0-T_7			I
Port			**00H/00HE**
BUS_8, BUS_9			C
BUS_0-BUS_7			E
BUS_{10}-BUS_{13}			E
$\overline{DOUT}$			C
ALE			C
$\overline{PSEN}$			C
LCDCL			C
$\overline{CSOUT}$			C
$\overline{STB}$			C
$\overline{TEST}$			A

Figure 20. Interface at Input/Output Ports



System Development

The μPD7500H/H-E evaluation chip has all the functionality of the entire μPD7500 series, and must be used with the EVAKIT-7500 to emulate the target product. During development, pay careful attention to the two precautions below to prevent fatal errors in mask ROM products.

Setting the Stack Pointer

The μPD7500 series microcomputers are without stack registers; a stack pointer specifies the stack area in memory. The value of the stack pointer becomes undefined when RESET is input, so it is necessary to specify an initial value at the start of the program. If a value is not specified or specified incorrectly, there is a danger the stack pointer could point to a location where data memory does not exist. In that case, unpredictable operation will result. Since evaluation chip μPD7500H/H-E has the largest RAM size in the series, there is a possibility it will operate properly even though the stack pointer setting is incorrect and the error is not detected. For these reasons, take care in setting the stack pointer. See table 6.

Table 6. Setting the Stack Pointer

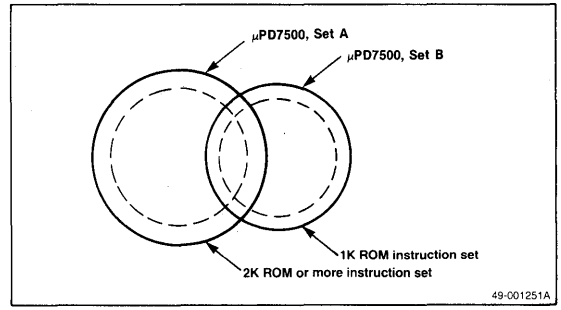
Product (μPD)	Stack Area	SP Max Value
7501	18H to 5FH	60H
7502	18H to 7FH	80H
7503	18H to DFH	E0H
7514	20H to FFH	00H
7506	00H to 3FH	40H
7507/07S/07H	00H to 7FH	80H
7508/08H	00H to DFH	E0H
7508A	00H to CFH	D0H
7527A/37A	00H to 7FH	80H
7528A/38A	00H to 9FH	A0H
7519/19H	40H to FFH	00H
7516H	40H to FFH	00H
7533	00H to 9FH	A0H
7554/64	00H to 3FH	40H
7556/66	00H to 3FH	40H

Instruction Set Selection

The instructions for the μPD7500 series have been divided into set A and set B according to the size of the mask ROM product to be implemented. As shown in figure 21, set B is adopted for products with a 1K-byte ROM and set A is for products with a ROM size of 2K-bytes or more. The actual instruction sets employed in the mask ROM products are subsets of set A and set B.

During system development, make sure the instructions being used actually exist in the product for which development is being performed. Also, if your program includes a jump to an address outside the current bank (address above 4K-bytes), either the set A or the set B assembler can be used effectively. When making the ordering tape for the mask ROM, however, be sure to assemble with the dedicated assembler for the product and confirm that the program fits in the mask ROM.

Figure 21. Instruction Sets A and B vs ROM size



The Instruction Set

The instruction set of each product is a subset of the μPD7500 instruction set A or B. In the columns at the right side of the instruction set table, "X" identifies the members of the seven subsets: A1 through A4 and B1 through B3.

Table 7 shows the applicability of subsets to the 7500 series products. Evaluation chips μPD7500H/H-E can execute all instructions in set A (subset A1) and set B (subset B1). The same assembler can be used for all products in the series.

Table 8 gives the meanings of symbols used in the Operand column. Operands are defined in detail by the assembler specification.

Symbols in the Operation column of the instruction set table are explained in table 9. The table 8 symbols also appear in this column.

Several of the parallel I/O instructions (IPL and IP, OPL and OP, ANP and ORP) select a port or register by immediate data or by data in the L register. Tables 10, 11, and 12 provide the required data.

Instructions SPBL and RPBL, respectively, set and reset one bit of a port defined by the contents of the L register. Table 13 provides the four bits to be loaded into the L register, by an LLI instruction for example.

Machine codes are not included in the instruction set table but they are in the User's Manuals.

Table 7. Applicability of Instruction Subsets

Subset	Products that Execute the Subset
A1	7500H, 7500H-E (Instruction set A)
A2	7516H, 7519, 7519H
A3	7502, 7503, 7507, 7507H, 7507S, 7508, 7508A, 7508H, 7514
A4	7527A, 7528A, 7537A, 7538A, 7533
B1	7500H, 7500H-E (Instruction set B)
B2	7501, 7506
B3	7554, 7556, 7564, 7566

Table 8. Symbols in the Operand Column of the Instruction Set

Symbol	Meaning
addr	13-bit immediate data or label
addr1	12-bit immediate data or label
addr2	11-bit immediate data or label
addr3	10-bit immediate data or label
addr4	1 to FH immediate data or label
addr5	0, 1, or 4 to BH immediate data or label
addr6	2 to BH immediate data or label
addr7	4-bit immediate data or label
cadr	11-bit immediate data or label
caddr1	0100H to 0107H, 0140H to 0147H, 0180H to 0187H, 01C0H to 01C7H immediate data or label
taddr	00C0 to 00CFH immediate data or label
taddr1	00D0 to 00FFH immediate data or label
mem	8-bit immediate data or label
byte	8-bit immediate data or label
n5	5-bit immediate data or label
n4	4-bit immediate data or label
n3	3-bit immediate data or label
bit	2-bit immediate data or label
pr	DL, DE, HL−, HL+, HL
pr1	HL−, HL+, HL

Table 9. Other Symbols in the Instruction Set

Symbol	Meaning
A	Accumulator
D	D register
E	E register
H	H register
L	L register
DE	Pair register (DE)
DL	Pair register (DL)
HL	Pair register (HL)
pr	Pair register (DL, DE, HL−, HL+, HL)
SP	Stack pointer
PC	Program counter
CT	Count register
BNK	Bank flag
C	Carry flag
PSW	Program status word
SIO	Shift register
MOD	Modulo register
IE	Interrupt enable register
IME	Interrupt master enable FF
In	byte, n5, n4, n3 type immediate data
Pn	addr, addr1, addr2, addr3, addr7, caddr, taddr, taddr1 type immediate data
Dn	addr4, addr5, addr6, mem type immediate data
Bn	bit type immediate data
R	pr, pr1 type immediate data
(xx)	Contents of memory addressed by xx
xxH	Hexadecimal data
←	Transfer direction, result
∧	Logical product (logical AND)
V	Logical sum (logical OR)
∀	Exclusive OR
—	Complement (overbar)

Table 10. Port or Register Selection; Instructions IPL and IP

L or addr5	Port or Register
0	Port 0
1	Port 1
4	Port 4
5	Port 5
6	Port 6
7	Port 7
8	7500, 7516H, 7519/19H: Expansion port (8243 port 4) 7533: SA register lower 4 bits
9	7500, 7516H, 7519/19H: Expansion port (8243 port 5) 7533: SA register higher 4 bits
AH	7500, 7516H, 7519/19H: Expansion port (8243 port 6) 7533: EOC flag bit 2
BH	7500, 7516H, 7519/19H: Expansion port (8243 port 7)

Table 11. Port or Register Selection; Instructions OPL and OP

L or addr4	Port or Register
1	Port 1
2	Port 2
3	Port 3
4	Port 4
5	Port 5
6	Port 6
7	Port 7
8	7500, 7516H, 7519/19H: Expansion port (8243 port 4)
9	7500, 7516H, 7519/19H: Expansion port (8243 port 5)
AH	7500, 7516H, 7519/19H: Expansion port (8243 port 6) 7533: ADM register
BH	7500, 7516H, 7519/19H: Expansion port (8243 port 7)
CH	Clock mode register
DH	Interrupt mode register
EH	Port 6 mode register
FH	Shift mode register

Table 12. Port Selection; Instructions ANP and ORP

addr6	Port
2	Port 2
3	Port 3
4	Port 4
5	Port 5
6	Port 6
7	Port 7
8	7500, 7516H, 7519/19H: Expansion port (8243 port 4)
9	7500, 7516H, 7519/19H: Expansion port (8243 port 5)
AH	7500, 7516H, 7519/19H: Expansion port (8243 port 6)
BH	7500, 7516H, 7519/19H: Expansion port (8243 port 7)

Table 13. Port and Bit Selection; Instructions RPBL and SPBL

Product (μPD)	Port Select (L_3, L_2)	Bit Select L_1, L_0 00	01	10	11
7500H/H-E, 7516H, 7519, 7519H (Note 1)	00	$P4_0$	$P4_1$	$P4_2$	$P4_3$
	01	$P5_0$	$P5_1$	$P5_2$	$P5_3$
	10	$P6_0$	$P6_1$	$P6_2$	$P6_3$
	11	$P7_0$	$P7_1$	$P7_2$	$P7_3$
7527A/28A, 7537A/38A	00	$P8_0$	$P8_1$	$P8_2$	$P8_3$
	01	$P9_0$	$P9_1$	$P9_2$	$P9_3$
	10	$P10_0$	$P10_1$	$P10_2$	$P10_3$
	11	$P11_0$	$P11_1$	$P11_2$	$P11_3$
7554/64	00	$P8_0$	$P8_1$	$P8_2$	$P8_3$
	01	Use inhibited			
	10	$P10_0$	$P10_1$	$P10_2$	$P10_3$
	11	$P11_0$	$P11_1$	$P11_2$	$P11_3$
7556/66	00	$P8_0$	$P8_1$	$P8_2$	$P8_3$
	01	$P9_0$	$P9_1$	Use inhibited	
	10	$P10_0$	$P10_1$	$P10_2$	$P10_3$
	11	$P11_0$	$P11_1$	$P11_2$	$P11_3$

Note:

(1) Ports P4, P5, P6 and P7 are on μPD8243.

Instruction Set

Mnemonic	Operand	Operation	Skip Condition	μPD7500 Series Instruction Subset (Note 1)						
				A1	A2	A3	A4	B1	B2	B3
• Load Instructions										
LAI	n4	A ← n4	String effect LAI	X	X	X	X	X	X	X
LDI	n4	D ← n4		X	X	X				
LEI	n4	E ← n4		X	X	X				
LHI	n4	H ← n4		X	X	X				
LHI	n3	H ← $0I_2I_1I_0$						X	X (2)	X (2)
LLI	n4	L ← n4		X	X	X				
LAM	pr	A ← (pr) pr = DL, DE, HL−, HL+, HL	L = 0 (HL+) L = FH (HL−)	X	X	X	X			
LAM	pr1	A ← (pr1) pr1 = HL−, HL+, HL	L = 0 (HL+) L = FH (HL−)					X	X	X
LADR	mem	A ← (mem)		X	X	X	X	X	X	
LDEI	byte	DE ← byte		X	X	X				
LHLI	byte	HL ← byte	String effect LHLI, LHLT	X	X	X	X			
LHLI	n5	HL ← 000 $I_4I_3I_2I_1I_0$	String effect LHLI					X	X	X
LHLT	taddr	H ← TABLE $(000001100P_3P_2P_1P_0)_H$ L ← TABLE $(000001100P_3P_2P_1P_0)_L$	String effect LHLT, LHLI	X	X	X	X			
LAMT (3)		A ← TABLE (BNK, PC_{11}-PC_6, 0, C, A_3-$A_0)_H$ (HL) ← TABLE (BNK, PC_{11}-PC_6, 0, C, A_3-$A_0)_L$		X		X (4)		X	X	
LAMTL (3)		A ← TABLE (BNK, PC_{11}-PC_8, A_3-A_0, $(HL)_3$-$(HL)_0)_H$ (HL) ← TABLE (BNK, PC_{11}-PC_8, A_3-A_0, $(HL)_3$-$(HL)_0)_L$		X	X	X (4)	X	X		
• Store Instructions										
ST		(HL) ← A	X	X	X	X	X	X	X	X
STII	n4	(HL) ← $I_3I_2I_1I_0$ L ← L + 1						X	X	X

Note:

(1) X means the instruction is part of the subset.

(2) μPD7506/54/64/56/66 operation is H ← $00I_1I_0$.

(3) BNK is used only for the μPD7516 and Set A (A1). PC_{10}, PC_{11} use varies depending on ROM capacity.

(4) LAMT is used only in μPD7502. LAMTL is not used in the μPD7502 but is used by other devices in the A3 group.

Instruction Set (cont)

Mnemonic	Operand	Operation	Skip Condition	μPD7500 Series Instruction Subset (Note 1) A1	A2	A3	A4	B1	B2	B3
• Transfer Instructions										
TAD		D ← A		X	X	X				
TAE		E ← A		X	X	X				
TAH		H ← A		X	X	X				
TAL		L ← A		X	X	X				
TDA		A ← D		X	X	X				
TEA		A ← E		X	X	X				
THA		A ← H		X	X	X				
TLA		A ← L		X	X	X				
• Exchange Instructions										
XAD		A ⟷ D		X	X	X				
XAE		A ⟷ E		X	X	X				
XAH		A ⟷ H		X	X	X	X	X	X	
XAL		A ⟷ L		X	X	X	X	X	X	X
XAM	pr	A ⟷ (pr) pr = DL, DE, HL−, HL+, HL	L = 0 (HL+), L = FH (HL−)	X	X	X	X			
XAM	pr1	A ⟷ (pr1) pr1 = HL−, HL+, HL	L = 0 (HL+), L = FH (HL−)					X	X	X
XADR	mem	A ⟷ (mem)		X	X	X	X	X	X	
XHDR	mem	H ⟷ (mem)		X	X	X	X	X	X	
XLDR	mem	L ⟷ (mem)		X	X	X	X	X	X	
• Arithmetic Instructions										
AISC	n4	A ← A + n4	carry	X	X	X	X	X	X	X
ASC		A ← A + (HL)	carry	X	X	X	X	X	X	X
ACSC		A, C ← A + (HL) + C	carry	X	X	X	X	X	X	X
ADSC		A ← A + D	carry	X	X					
AESC		A ← A + E	carry	X	X					
AHSC		A ← A + H	carry	X	X					
ALSC		A ← A + L	carry	X	X					
SDSB		A ← A − D	borrow	X	X					
SESB		A ← A − E	borrow	X	X					
SHSB		A ← A − H	borrow	X	X					
SLSB		A ← A − L	borrow	X	X					
• Logical Instructions										
EXL		A ← A ⊻ (HL)		X	X	X	X	X	X	X
ANL		A ← A ∧ (HL)		X	X	X	X	X	X	
ORL		A ← A ∨ (HL)		X	X	X	X	X	X	

Instruction Set (cont)

Mnemonic	Operand	Operation	Skip Condition	μPD7500 Series Instruction Subset (Note 1)						
				A1	A2	A3	A4	B1	B2	B3
• Accumulator Instructions										
CMA		A ← A		X	X	X	X	X	X	X
RAR		C ← A_0; A_3 ← C; A_n ← A_{n+1}		X	X	X	X	X	X	
RAL		C ← A_3; A_0 ← C; A_n ← A_{n-1}		X	X			X		
• Program Status Word Instructions										
RC		C ← 0		X	X	X	X	X	X	X
SC		C ← 1		X	X	X	X	X	X	X
• Increment and Decrement Instructions										
IES		E ← E + 1	E = 0	X	X	X	X			
ILS		L ← L + 1	L = 0	X	X	X	X	X	X	X
IDE		DE ← DE + 1		X	X					
IHL		HL ← HL + 1		X	X					
IDRS	mem	(mem) ← (mem) + 1	(mem) = 0	X	X	X	X	X	X	X
DES		E ← E − 1	E = FH	X	X	X	X			
DLS		L ← L − 1	L = FH	X	X	X	X	X	X	X
DDE		DE ← DE − 1		X	X					
DHL		HL ← HL − 1		X	X					
DDRS	mem	(mem) ← (mem) − 1	(mem) = FH	X	X	X	X	X	X	X
• Bit Manipulation Instructions										
RMB		(HL) bit ← 0		X	X	X	X	X	X	X
SMB		(HL) bit ← 1		X	X	X	X	X	X	X
• Branch Instructions										
JMP	addr1	PC_{11}-PC_0 ← P_{11}-P_0		X	X	X (5)	X (6)		X (10)	X (10)
JMP	addr2	PC_{11}-PC_0 ← P_{10}-P_0				X (7)	X (8)	X		
JMPL	addr	BNK ← P_{13}; PC_{11}-PC_0 ← P_{11}-P_0		X	X (9)			X		
JCP	addr1	PC_5-PC_0 ← P_5-P_0		X	X	X	X	X	X	X
JAM	addr7	PC_{11}-PC_8 ← P_3-P_0; PC_7-PC_4 ← A_3-A_0; PC_3-PC_0 ← (HL)		X	X	X	X	X	X	

Note:

(5) Only for μPD7503/08/08A/08H.

(6) Only for μPD7528A/38A.

(7) Only for μPD7502/07/07S/07H.

(8) Only for μPD7527A/37A.

(9) Only for μPD7516H.

(10) Operation: PC_9-PC_0 ← P_9-P_0

Instruction Set (cont)

Mnemonic	Operand	Operation	Skip Condition	μPD7500 Series Instruction Subset (Note 1)						
				A1	A2	A3	A4	B1	B2	B3
• Conditional Skip Instructions										
SKC		Skip if C = 1	C = 1	X	X	X	X	X	X	X
SKABT	bit	Skip if A bit = 1	A bit = 1	X	X	X	X	X	X	X
SKMBT	bit	Skip if (HL) bit = 1	(HL) bit = 1	X	X	X	X	X	X	X
SKMBF	bit	Skip if (HL) bit = 0	(HL) bit = 0	X	X	X	X	X	X	X
SKAEM		Skip if A = (HL)	A = (HL)	X	X	X	X	X	X	X
SKAEI	n4	Skip if A = n4	A = n4	X	X	X	X	X	X	X
SKDEI	n4	Skip if D = n4	D = n4	X	X	X				
SKEEI	n4	Skip if E = n4	E = n4	X	X	X				
SKHEI	n4	Skip if H = n4	H = n4	X	X	X				
SKLEI	n4	Skip if L = n4	L = n4	X	X	X	X	X	X	
SKMEI	n4	Skip if (HL) = n4	(HL) = n4	X	X		X	X		
• Serial Interface Instructions										
TAMSIO		$SIO_H \leftarrow A$; $SIO_L \leftarrow (HL)$		X	X	X	X	X	X (12)	X (13)
TSIOAM		$A \leftarrow SIO_H$; $(HL) \leftarrow SIO_L$		X	X	X	X	X	X (12)	X (13)
SIO		Start SIO		X	X	X	X	X	X (12)	X (13)
• Timer/Event Counter Instructions										
TAMMOD		$MOD_H \leftarrow A$; $MOD_L \leftarrow (HL)$		X	X	X	X	X	X	
TIMER		CT_7-$CT_0 \leftarrow 0$		X	X	X	X	X	X	X
TCNTAM		$A \leftarrow CT_7$-CT_4; $(HL) \leftarrow CT_3$-CT_0		X	X	X	X	X	X	X
• Interrupt Control Instructions										
EI	n4	Enable interrupt		X	X	X	X			
DI	n4	Disable interrupt		X	X	X	X			
SKI	n4	Skip if interrupt		X	X	X	X	X	X	X

Note:

(12) SIO is not used in the μPD7506.

(13) SIO is not used in the μPD7556/66.

Instruction Set (cont)

Mnemonic	Operand	Operation	Skip Condition	μPD7500 Series Instruction Subset (Note 1)						
				A1	A2	A3	A4	B1	B2	B3
• Stack Instructions										
CALL (11)	caddr	(SP − 1) (SP − 2) (SP − 4) ← PC_{11}-PC_0; X (SP − 3) ← PSW; SP ← SP − 4; BNK ← 0; PC_{11}-PC_0 ← 0, P_{10}-P_0		X	X	X	X	X	X	X
CAL (11)	caddr1	(SP − 1) (SP − 2) (SP − 4) ← PC_{11}-PC_0; (SP − 3) ← PSW; SP ← SP − 4; BNK ← 0; PC_{11}-PC_0 ← 0001$P_4P_3$000$P_2P_1P_0$						X	X	X
CALT (11)	taddr1	(SP − 1) (SP − 2) (SP − 4) ← PC_{11}-PC_0; (SP − 3) ← PSW; SP ← SP − 4; BNK ← 0, PC_{11}, PC_{10}, PC_6, PC_5 ← 0: PC_9-PC_7, PC_4-PC_0 ← TABLE (0000011$P_5P_4P_3P_2P_1P_0$)		X	X	X	X			
RT (11)		PC_{11}-PC_0 ← (SP) (SP + 2) (SP + 3); BNK ← $(SP + 1)_1$; SP ← SP + 4		X	X	X	X	X	X	X
RTS (11)		PC_{11}-PC_0 ← (SP) (SP + 2) (SP + 3); BNK ← $(SP + 1)_1$; SP ← SP + 4, then skip unconditionally		X	X	X	X	X	X	X
RTPSW (11)		PC_{11}-PC_0 ← (SP) (SP + 2) (SP + 3); PSW ← (SP + 1); SP ← SP + 4		X	X	X	X			
PSHDE		(SP − 1) ← H; (SP − 2) ← E; SP ← SP − 2		X	X	X				
PSHHL		(SP − 1) ← H; (SP − 2) ← L; SP ← SP − 2		X	X	X				
POPDE		D ← (SP + 1); E ← (SP); SP ← SP + 2		X	X	X				
POPHL		H ← (SP + 1); L ← (SP); SP ← SP+ 2		X	X	X				
TAMSP		SP_7-SP_4 ← A; SP_3-SP_1 ← $(HL)_3$-$(HL)_1$; SP_0 ← 0		X	X	X	X	X	X	X
TSPAM		A ← SP_7-SP_4; $(HL)_3$-$(HL)_1$, ← SP_3-SP_1; $(HL)_0$ ← 0		X	X	X	X	X		

Note:

(11) BNK is used only for μPD7516H and Set A. The use of PC_{10} and PC_{11} varies depending on the ROM capacity.

Instruction Set (cont)

Mnemonic	Operand	Operation	Skip Condition	μPD7500 Series Instruction Subset (Note 1)						
				A1	A2	A3	A4	B1	B2	B3
• Parallel I/O Instructions										
IPL		A ← PORT (L)		X	X	X	X	X	X	X
IP	addr5	A ← PORT (addr5)		X	X	X	X	X	X	
IP1		A ← PORT1		X	X	X (14)		X	X	X (15)
IP54		A ← PORT5; (HL) ← PORT4		X	X	X	X	X	X	
OPL		PORT/MODE REG (L) ← A		X	X	X	X	X	X	X
OP	addr4	PORT/MODE REG (addr4) ← A		X	X	X	X	X	X	
OP3		PORT3 ← A		X	X	X	X	X	X (16)	
OP54		PORT5 ← A; PORT4 ← (HL)		X	X	X	X	X	X	
ANP	addr6, n4	PORT (addr6) ← PORT (addr6) ∧ n4		X	X	X	X (17)			
ORP	addr6, n4	PORT (addr6) ← PORT (addr6) ∨ n4		X	X	X	X (17)			
RPBL		Port bit (L) ← 0		X			X (18)	X		X
SPBL		Port bit (L) ← 1		X			X (18)	X		X
HALT		Set Halt mode		X	X	X	X	X	X	X
STOP		Set Stop mode		X	X	X	X	X	X	X
NOP		No operation		X	X	X	X	X	X	X

Note:

(14) IP1 is not used in the μPD7507S.

(15) IP1 is not used in the μPD7554/64.

(16) OP3 is not used in the μPD7506.

(17) ANP and ORP are used only in the μPD7533.

(18) SPBL and RPBL are not used in the μPD7533.

μPD7500H/H-E 4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS FOR μPD7500-SERIES EVALUATION

Description

The μPD7500H and μPD7500H-E are single-chip microcomputers created as ROM-less evaluation chips for 4-bit single-chip microcomputers in the μPD7500 series. They are used with the appropriate Evakit development tool to emulate device operation of the μPD7500 series. The μPD7500H and μPD7500H-E incorporate a 4-bit parallel ALU, a data memory (RAM), a bus interface, I/O ports, an 8-bit serial interface, an 8-bit programmable timer/event counter, and vectored interrupt functions integrated into a single-chip design.

External memory may be a 2764 or any other type that interfaces an 8085-type bus.

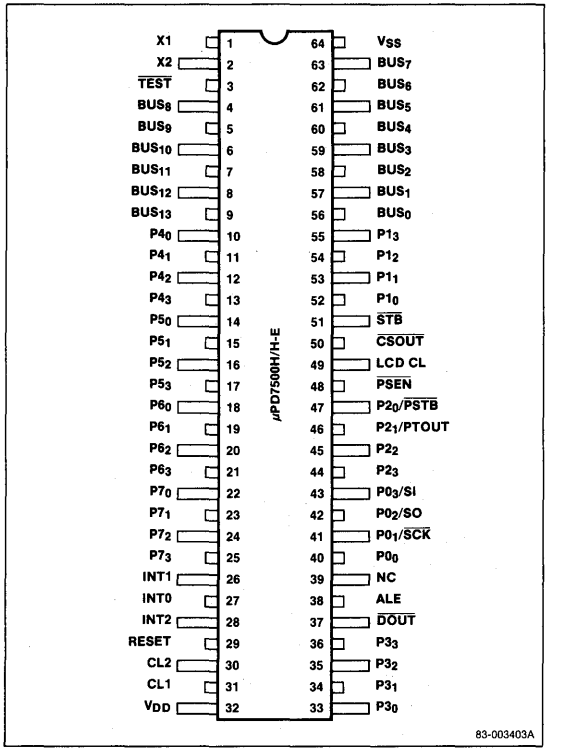
Features

- ☐ μPD7500 series evaluation chip
- ☐ 4-bit microcomputer
- ☐ Two instruction sets:
  - — Set A: 110 instructions
  - — Set B: 70 instructions
- ☐ Instruction cycles:
  - — μPD7500H: RC oscillator = 5 μs/400 kHz
    External clock = 2.86 μs/700 kHz
  - — μPD7500H-E: RC oscillator = 10 μs/200 kHz
    External clock = 10 μs/200 kHz
- ☐ External program memory: 8192 words x 8 bits
- ☐ Internal data memory (RAM): 256 words x 4 bits
- ☐ Three vectored interrupts (INT0, INT1, INT2)
- ☐ Two internal interrupts (INTS, INTT)
- ☐ 8-bit interval timer/event counter
- ☐ 8-bit serial interface
- ☐ Three types of serial clocks
- ☐ 8243 I/O expander interface
- ☐ Power-down functions using standby (STOP/HALT) mode
- ☐ Built-in RC oscillator for system clock (external drive also possible)
- ☐ Built-in crystal oscillator for count clock (external drive also possible)
- ☐ LCD regulating clock output (LCD CL)
- ☐ Low power consumption CMOS
- ☐ Single +5 V ±10% power supply

Ordering Information

Part Number	Package Type	Maximum Frequency of Operation
μPD7500HG-36	64-pin plastic QUIP	700 kHz
μPD7500H-EG-36	64-pin plastic QUIP	410 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 2	X2, X1	Crystal clock/external event input port n
3	$\overline{TEST}$	Factory test pin (connect to V_{SS})
4-9, 56-63	BUS_0-BUS_{13}	External data bus connected to external program memory
10-13	$P4_0$-$P4_3$	4-bit input/latched three-state output port 4
14-17	$P5_0$-$P5_3$	4-bit input/latched three-state output port 5
18-21	$P6_0$-$P6_3$	4-bit input/latched three-state output port 6
22-25	$P7_0$-$P7_3$	4-bit input/latched three-state output port 7
26	INT1	External interrupt INT1
27	INT0	External interrupt INT0
28	INT2	External interrupt INT2
29	RESET	RESET input
30, 31	CL1, CL2	System clock input
32	V_{DD}	Positive power supply
33-36	$P3_0$-$P3_3$	4-bit input/latched three-state output port 3
37	$\overline{DOUT}$	Data output
38	ALE	Address latch enable
39	NC	No connection
40-43	$P0_0$ $P0_1/\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input port 0, serial I/O interface
44-47	$P2_0/\overline{PSTB}$ $P2_1$/PTOUT $P2_2$, $P2_3$	4-bit latched three-state output port 2
48	$\overline{PSEN}$	Program store enable
49	LCD CL	Display timing pulse
50	$\overline{CSOUT}$	Chip select output
51	$\overline{STB}$	Strobe output
52-55	$P1_0$-$P1_3$	4-bit input/three-state output port 1
64	V_{SS}	Ground

Pin Functions

BUS_0-BUS_{13} [Data Bus]

External data bus connected to external program memory.

$P0_0$, $P0_1/\overline{SCK}$, $P0_2$/SO, $P0_3$/SI [Port 0/Serial Interface]

4-bit input port 0/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface, under control of the serial mode select register. The serial input SI , serial output SO , and the serial clock $\overline{SCK}$ (synchronizes data transfer) make up the 8-bit serial I/O interface.

$P1_0$-$P1_3$ [Port 1]

4-bit input/three-state output port 1. Data output from port 1 is strobed in synchronization with a $P2_0/\overline{PSTB}$ pulse.

$P2_0/\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2]

4-bit latched three-state output port 2 . Line $P2_0$ is shared with $\overline{PSTB}$, the port 1 output strobe pulse. Line $P2_1$ is shared with PTOUT, the timer-out F/F signal .

$P3_0$-$P3_3$ [Port 3]

4-bit input/latched three-state output port 3.

$P4_0$-$P4_3$ [Port 4]

4-bit input/latched three-state output port 4. Also performs 8-bit parallel I/O with port 5.

$P5_0$-$P5_3$ [Port 5]

4-bit input/latched three-state output port 5. Also performs 8-bit parallel I/O with port 4.

$P6_0$-$P6_3$ [Port 6]

4-bit input/latched three-state output port 6. Individual lines can be configured as inputs or outputs under control of the port 6 mode select register.

$P7_0$-$P7_3$ [Port 7]

4-bit input/latched three-state output port 7.

INT0 [Interrupt 0]

External interrupt INT0 . This is a rising edge-triggered interrupt.

INT1 [Interrupt 1]

External interrupt INT1. This is a rising edge-triggered interrupt.

INT2 [Interrupt 2]

External interrupt INT2. This is a rising edge-triggered interrupt.

CL1, CL2 [Clock Inputs]

System clock input. Connect 62-kΩ resistor across CL1 and CL2, and connect 33-pF capacitor from CL1 to V_{SS}. Alternatively, you may connect an external clock source to CL1 and leave CL2 open.

X2, X1 [Crystal Inputs]

Crystal clock/external event input port n. A crystal oscillator circuit is connected to input X1 and output X2 for crystal clock operation. Alternatively, external event pulses are connected to input X1 and output X2 is left open.

$\overline{DOUT}$ [Data Output]

Data output.

ALE [Address Latch Enable]

Address latch enable.

$\overline{PSEN}$ [Program Store Enable]

Program store enable.

LCD CL [Display Timing]

Display timing pulse.

$\overline{CSOUT}$ [Chip Select Output]

Chip select output. Connected to μPD82C43.

$\overline{STB}$ [Strobe Output]

Strobe output. Connected to μPD82C43.

$\overline{TEST}$ [Test Pin]

Factory test pin (connect to V_{SS}).

RESET [Reset]

RESET input. RC circuit or pulse initializes μPD7500H after power up.

NC [No Connection]

No connection.

V_{DD} [Power Supply]

Positive power supply. Apply single voltage in the range 4.5 to 6.0 V for proper operation.

V_{SS} [Ground]

Ground.

Evaluation Chip Selection for Emulation

Table 1 lists which evaluation chip should be used with the Evakits to emulate the appropriate speed of each device in the μPD7500 series.

Table 1. Evaluation Chip Selection

μPD7500H	μPD7500H-E
μPD7507H	μPD7501
μPD7508H	μPD7502
μPD7514	μPD7503
μPD7516H (Note 1)	μPD7506
μPD7519H (Note 1)	μPD7507
μPD7527A	μPD7507S
μPD7528A	μPD7508
μPD7533	μPD7508A
μPD7537A	μPD7519
μPD7538A	
μPD7554	
μPD7556	
μPD7564	
μPD7566	

Note:

(1) Up to 5.5 MHz during emulation.

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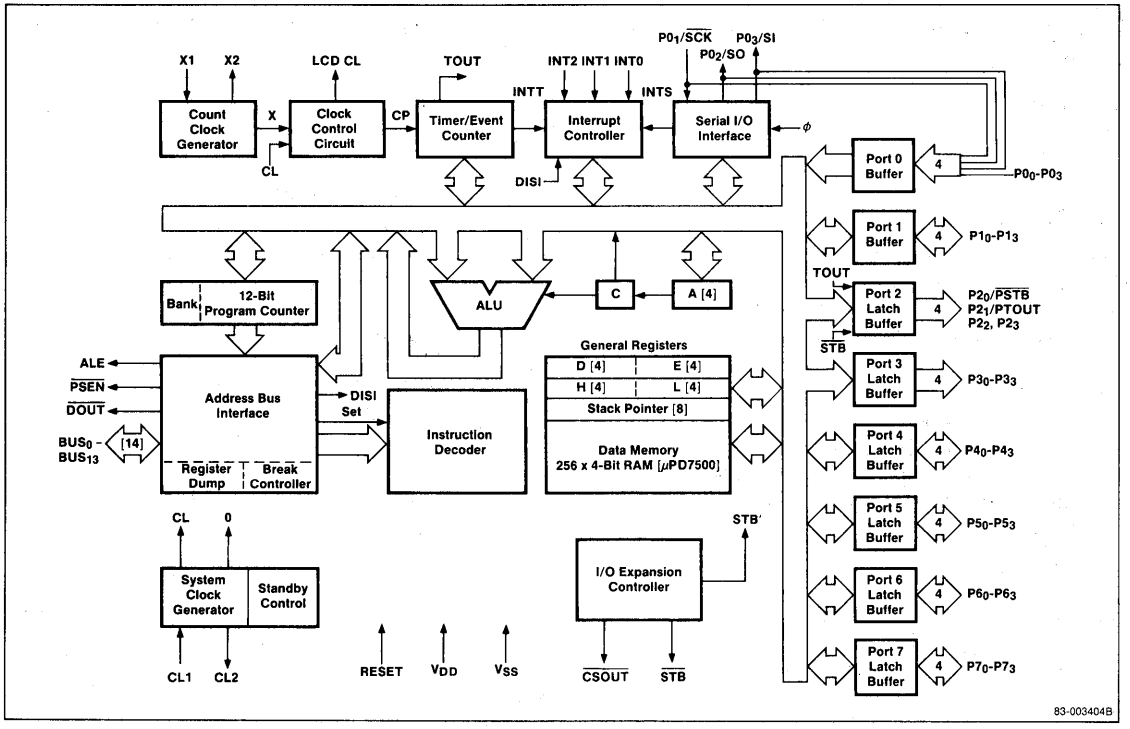
Block Diagram



See figures 1 through 7 for additional block diagram details.

Figure	Title
1	Data Memory Map
2	Program Memory Map
3	Timer/Event Counter
4	Serial Interface
5	Interrupt Control
6	Clock Control
7	Interface at Input/Output Ports

Figure 1. Data Memory Map

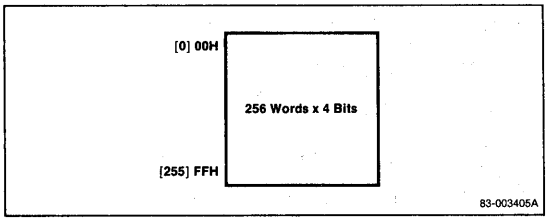


Figure 2. Program Memory Map

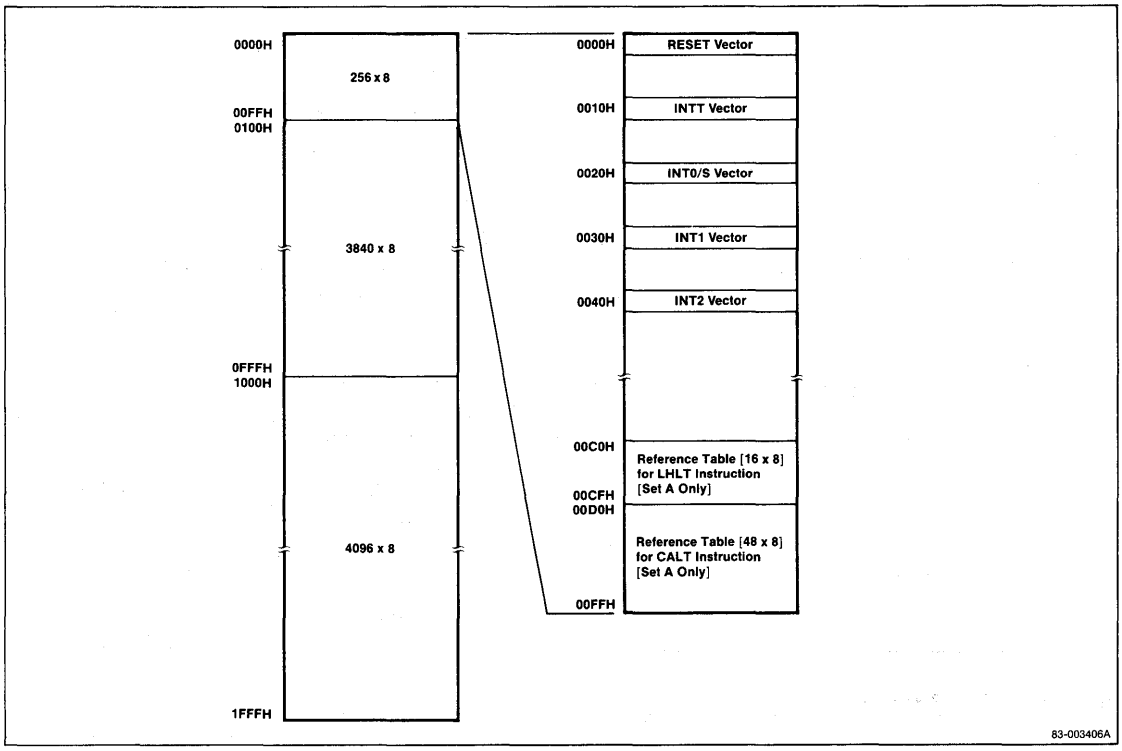


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Figure 3. Timer/Event Counter

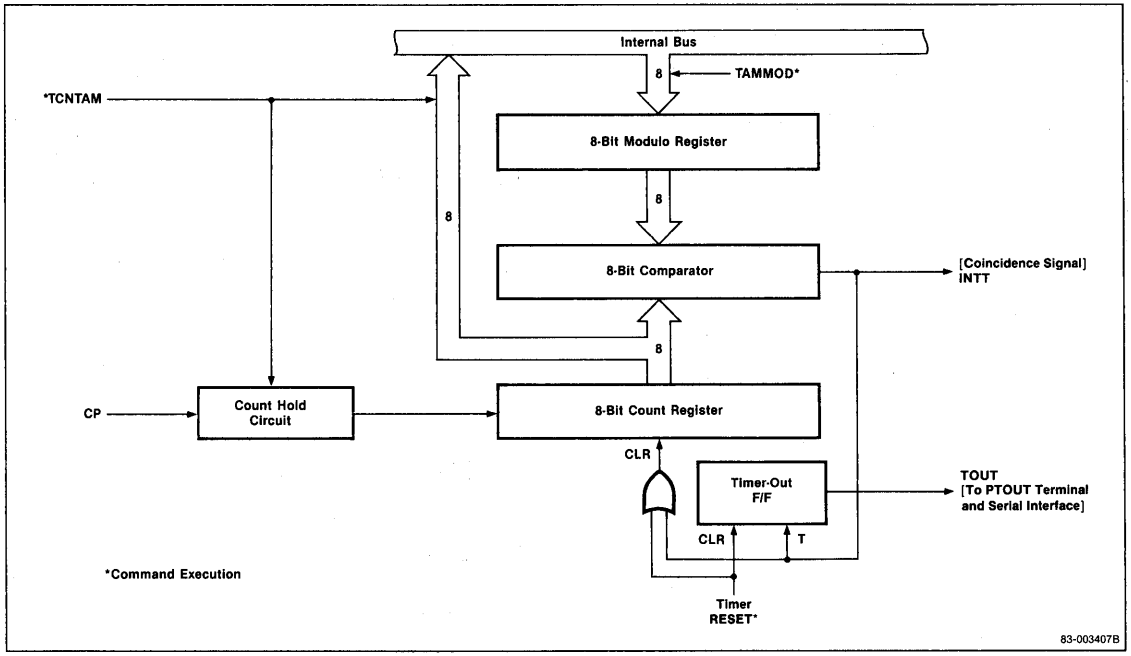


Figure 4. Serial Interface

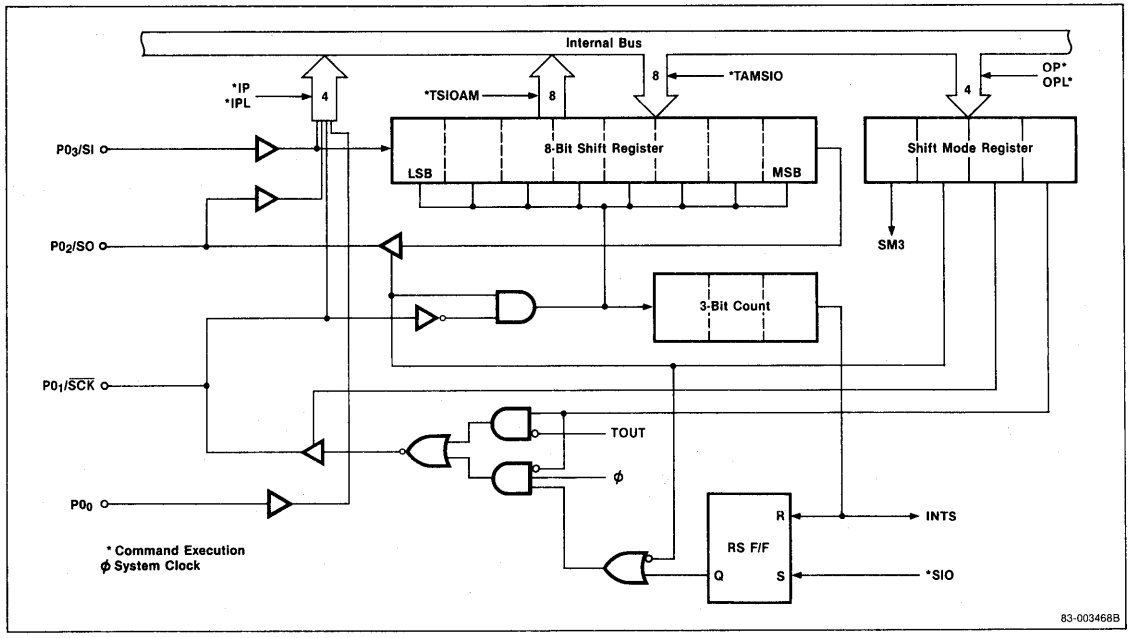


Figure 5. Interrupt Control

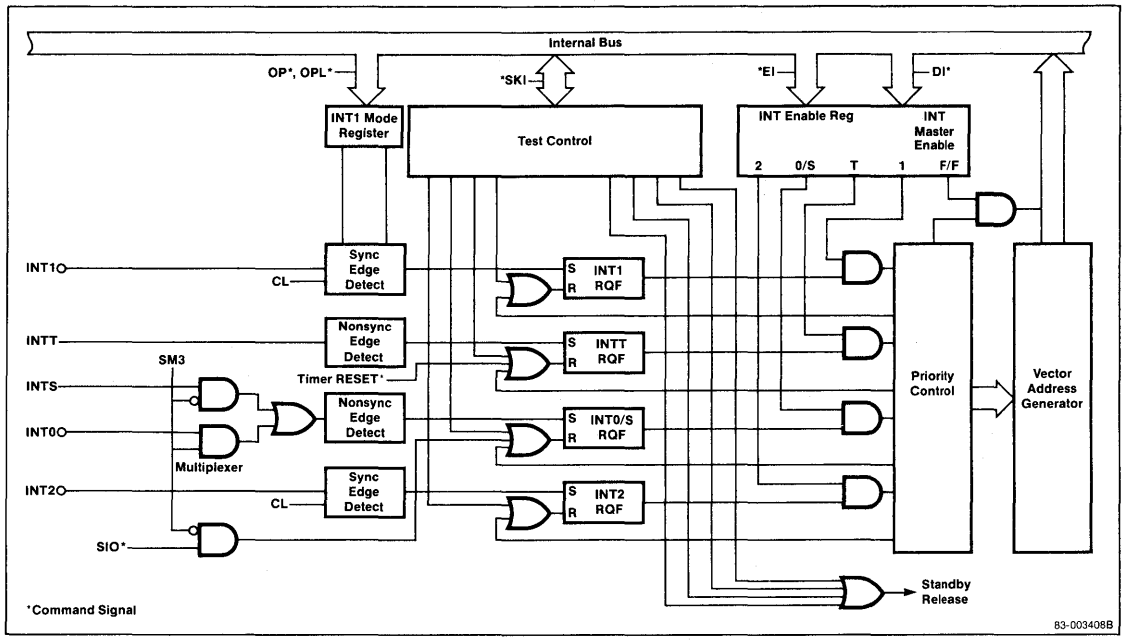


Figure 6. Clock Control

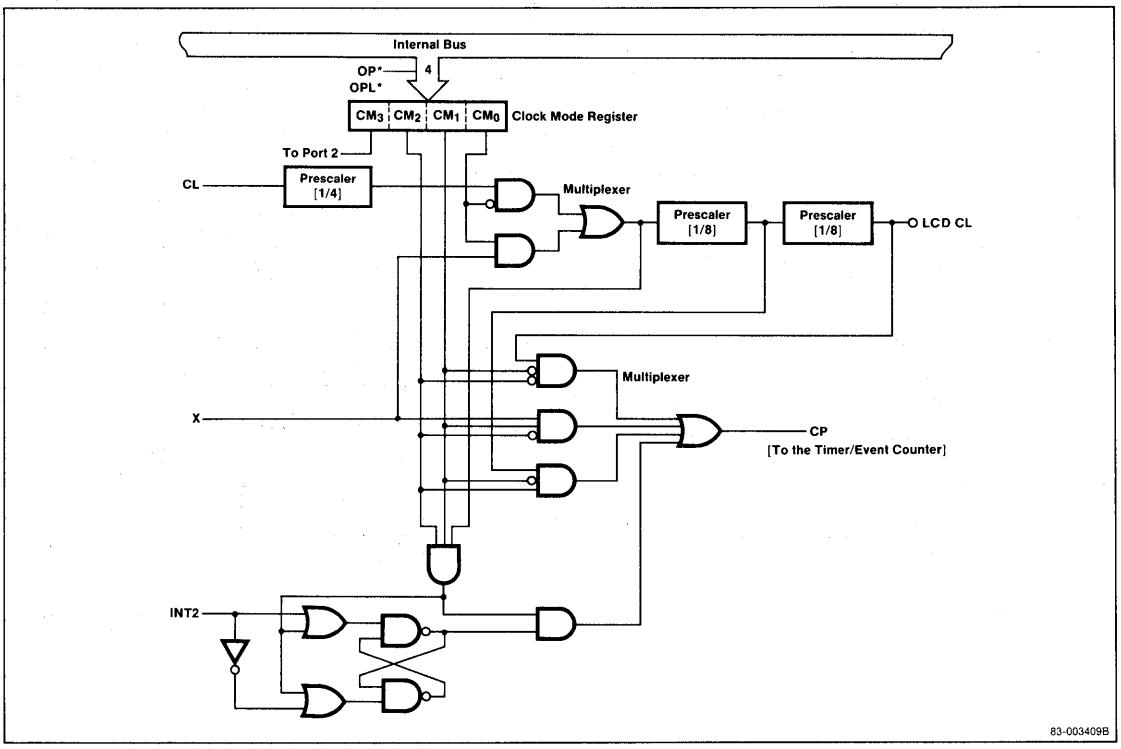
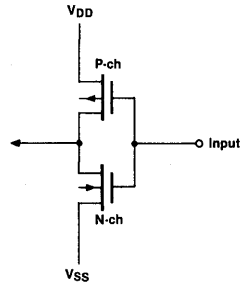
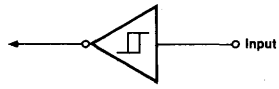


Figure 7. Interface at Input/Output Ports

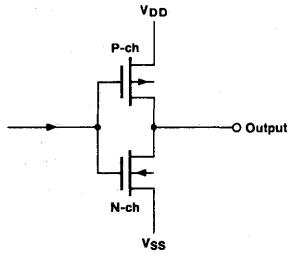
Type A
TEST, $P0_0$



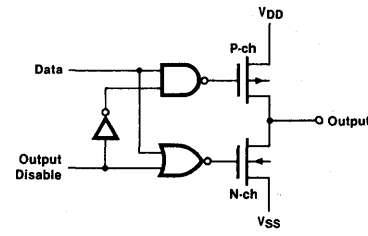
Type B
INT0, INT1, INT2, RESET, $P0_3$/SI



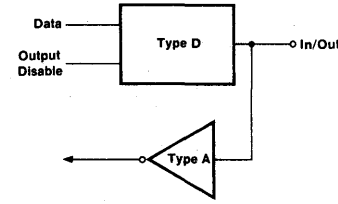
Type C
BUS_8, BUS_9 $\overline{DOUT}$, ALE, $\overline{PSEN}$, LCD CL, $\overline{CSOUT}$, $\overline{STB}$



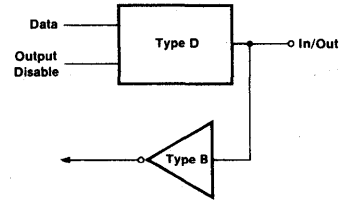
Type D
$P3_0$-$P3_3$, $P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$



Type E
BUS_0-BUS_7, BUS_{10}-BUS_{13}, $P4_0$-$P4_3$, $P5_0$-$P5_3$, $P6_0$-$P6_3$, $P7_0$-$P7_3$, $P0_2$/SO, $P1_0$-$P1_3$



Type F
$P0_1$/$\overline{SCK}$



83-003410C

Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	
μPD7500H	0 to +40°C
μPD7500H-E	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 to V_{DD} + 0.3 V
Output current (total, all output ports)	
I_{OH}	−20 mA
I_{OL}	50 mA

Comment: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

μPD7500H: $T_A = 0$ to +40°C, $V_{DD} = 5\ V \pm 5\%$
μPD7500H-E: $T_A = -10$ to +70°C, $V_{DD} = 5\ V \pm 10\%$

		Limits							
		μPD7500H			μPD7500H-E				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH1}	0.7 V_{DD}		V_{DD}	0.7 V_{DD}		V_{DD}	V	All inputs other than CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
Input low voltage	V_{IL1}	0		0.3 V_{DD}	0		0.3 V_{DD}	V	All inputs other than CL1, X1
	V_{IL2}	0		0.5	0		0.5	V	CL1, X1
Input leakage current, high	I_{LIH1}			3			3	μA	All inputs other than CL1, X1
	I_{LIH2}			10			10	μA	CL1, X1
Input leakage current, low	I_{LIL1}			−3			−3	μA	All inputs other than CL1, X1
	I_{LIL2}			−10			−10	μA	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V_{DD} − 1.0			V	$I_{OH} = 1.0$ mA
Output voltage, low	V_{OL}			0.4			0.4	V	$I_{OL} = 1.6$ mA
Output leakage current, high	I_{LOH}		3			3		μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}		−3			−3		μA	$V_O = 0$ V
Supply current	I_{DD1}		4			3		mA	Normal operation, all output pins open, no BUS conflicts
	I_{DD2}	2	20		2	20		μA	Stop mode, X1 = 0 V

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V, f = 1 MHz

		Limits							
		μPD7500H			μPD7500H-E				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15			15	pF	Unmeasured pins returned to V_{SS}
Output capacitance	C_O			15			15	pF	
I/O capacitance	C_{IO}			15			15	pF	

AC Characteristics

μPD7500H: $T_A = 0$ to 40°C, $V_{DD} = 5\ V \pm 5\%$
μPD7500H-E: $T_A = -10$ to +70°C, $V_{DD} = 5\ V \pm 10\%$

		Limits							
		μPD7500H			μPD7500H-E				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Clock Operation									
System clock oscillation frequency	f_ϕ	300	400	500	160	200	250	kHz	C = 33 pF ±5%; μPD7500H: R = 33 kΩ ±2%; μPD7500H-E: R = 62 kΩ ±2%
		10		700	10		410	kHz	CL1 = external clock
CL1 input rise time	t_{CR}			0.2			0.2	μs	
CL1 input fall time	t_{CF}			0.2			0.2	μs	
CL1 input clock width (high)	t_{CH}	0.7			1.2			μs	
CL1 input clock width (low)	t_{CL}	0.7			1.2			μs	
Count clock oscillation frequency (X1, X2)	f_{XX}	25	32	50	25	32	50	kHz	Crystal oscillation
Count clock input frequency (X1)	f_X	0		700	0		410	kHz	
X1 input rise time	f_{XR}			0.2			0.2	μs	
X1 input fall time	f_{XF}			0.2			0.2	μs	
X1 input clock width (high)	t_{XH}	0.7			1.2			μs	
X1 input clock width (low)	t_{XL}	0.7			1.2			μs	
Bus I/O Operation									
ALE pulse width (high)	t_{LH}	400			600			ns	
Address setup time to ALE ↓	t_{AL}	100			200			ns	
Address hold time to ALE ↓	t_{LA}	80			80			ns	
Output data setup time to $\overline{DOUT}$ ↑	t_{DDO}	200			200			ns	
Output data hold time after $\overline{DOUT}$ ↑	t_{DOD}	80			80			ns	
$\overline{DOUT}$ pulse width (low)	t_{DOL}	400			600			ns	
ALE → data input valid time	t_{LDV}			600			700	ns	
Address → data input valid time	t_{ADV}			700			900	ns	
$\overline{PSEN}$ pulse width (low)	t_{PSL}	700			1000			ns	
$\overline{PSEN}$ → data input valid time	t_{PSDV}			300			600	ns	
$\overline{PSEN}$ → data float	t_{PSDF}	0			0			ns	

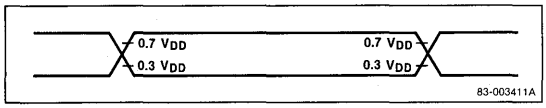
3

AC Characteristics (cont)

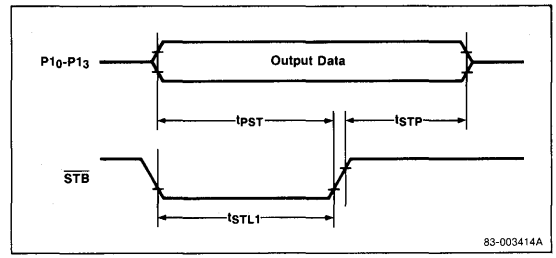
Parameter	Symbol	Limits μPD7500H Min	Typ	Max	Limits μPD7500H-E Min	Typ	Max	Unit	Test Conditions
Port I/O Operation									
Port 1 output setup time to $\overline{STB}\uparrow$	t_{PST}	200			200			ns	Port output mode
Port 1 output hold time after $\overline{STB}\uparrow$	t_{STP}	80			80			ns	
$\overline{STB}$ pulse width (low)	t_{STL1}	400			600			ns	
Output data setup time to $\overline{STB}\uparrow$	t_{DST}	300			300			ns	I/O expander mode
Output data hold time after $\overline{STB}\uparrow$	t_{STD}	80			80			ns	
$\overline{STB}\downarrow\rightarrow$ input data valid time	t_{STDV}			850			850	ns	
$\overline{STB}\downarrow\rightarrow$ input data float time	t_{STDF}	0			0			ns	
Control setup time to $\overline{STB}\downarrow$	t_{CST}	200			200			ns	
Control hold time after $\overline{STB}\downarrow$	t_{STC}	80			80			ns	
$\overline{STB}$ pulse width (low)	t_{STL2}	700			1000			ns	
$\overline{CSOUT}$ setup time to $\overline{STB}\downarrow$	t_{CSST}	200			200			ns	
$\overline{CSOUT}$ hold time after $\overline{STB}\downarrow$	t_{STCS}	80			80			ns	
Serial Interface Operation									
$\overline{SCK}$ cycle time	t_{KCY}	2.5			3.0			μs	Input
		2.86			4.9			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	1.1			1.3			μs	Input
		1.3			2.2			μs	Output
$\overline{SCK}$ pulse width, low	t_{KL}	1.1			1.3			μs	Input
		1.3			2.2			μs	Output
SI setup time to $\overline{SCK}\uparrow$	t_{SIK}	300			300			ns	
SI hold time after $\overline{SCK}\uparrow$	t_{KSI}	450			450			ns	
SO output delay after $\overline{SCK}\uparrow$	t_{SKO}			500			850	ns	
Other Operations									
INT0 pulse width, high	t_{I0H}	10			10			μs	
INT0 pulse width, low	t_{I0L}	10			10			μs	
INT1 pulse width, high	t_{I1H}	$2/f_\phi$			$2/f_\phi$			μs	
INT1 pulse width, low	t_{I1L}	$2/f_\phi$			$2/f_\phi$			μs	
INT2 pulse width, high	t_{I2H}	$2/f_\phi$			$2/f_\phi$			μs	
INT2 pulse width, low	t_{I2L}	$2/f_\phi$			$2/f_\phi$			μs	
RESET pulse width, high	t_{RSH}	10			10			μs	
RESET pulse width, low	t_{RSL}	10			10			μs	

Timing Waveforms

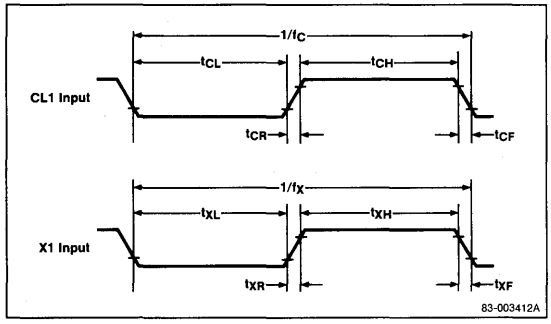
AC Test Input



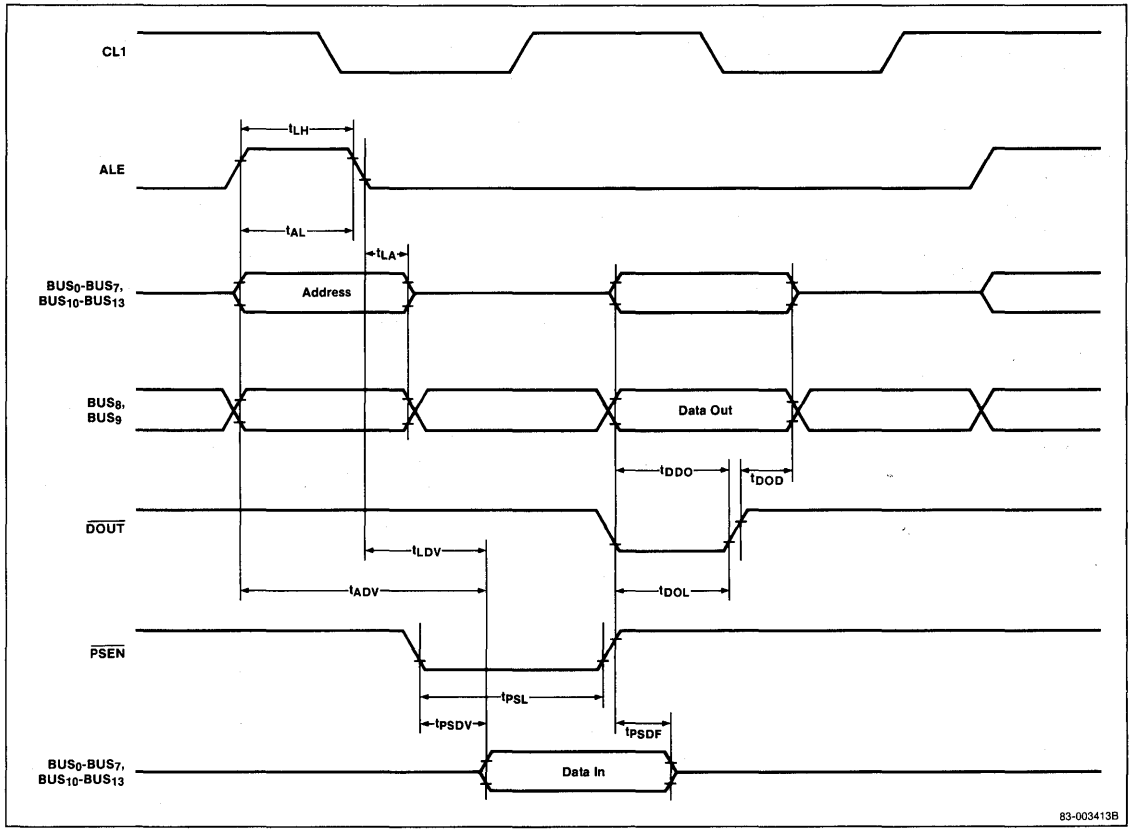
Strobe Output Timing



Clock Timing



Bus I/O Timing



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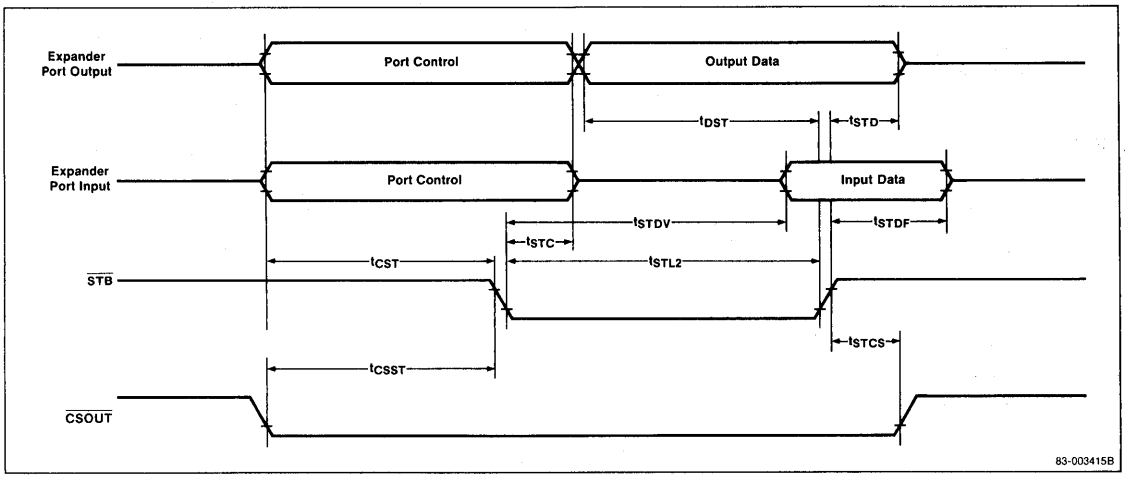
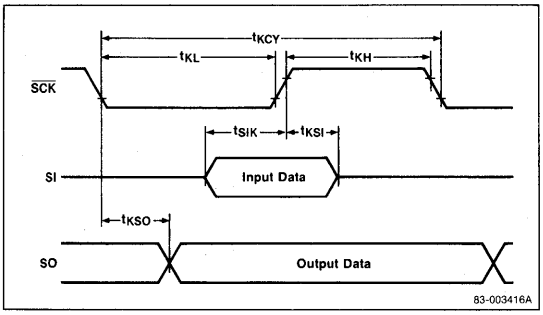
Timing Waveforms (cont)

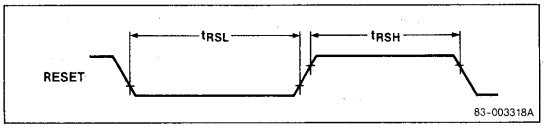
Port 1 I/O Expander Port Timing



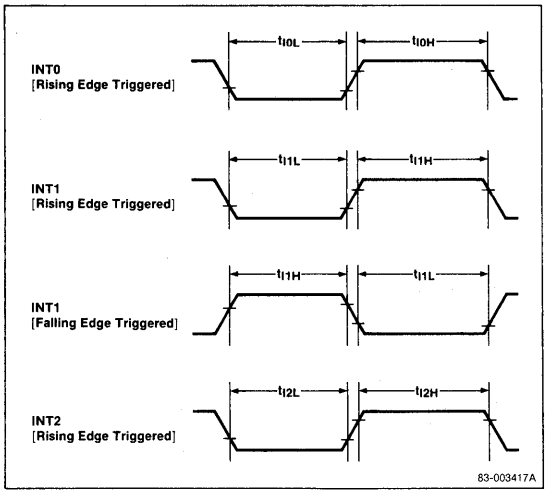
Serial Interface Timing



RESET Input Timing



Interrupt Input Timing



NEC Electronics Inc.

μPD7501
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH LCD CONTROLLER/DRIVER

Description

The μPD7501 4-bit, single-chip CMOS microcomputer has advanced fourth-generation architecture with the functional blocks necessary for a single-chip controller, including an 8-bit timer/event counter, an 8-bit serial I/O, and an LCD display controller/driver.

The μPD7501 contains two 4-bit general-purpose registers outside of RAM. The μPD7501 executes a subset of the μPD7500 series B instruction set with a 10-μs instruction cycle time.

Maximum power consumption is 900 μA at 5 V and 300 μA at 3 V. The HALT and STOP instructions further reduce power consumption.

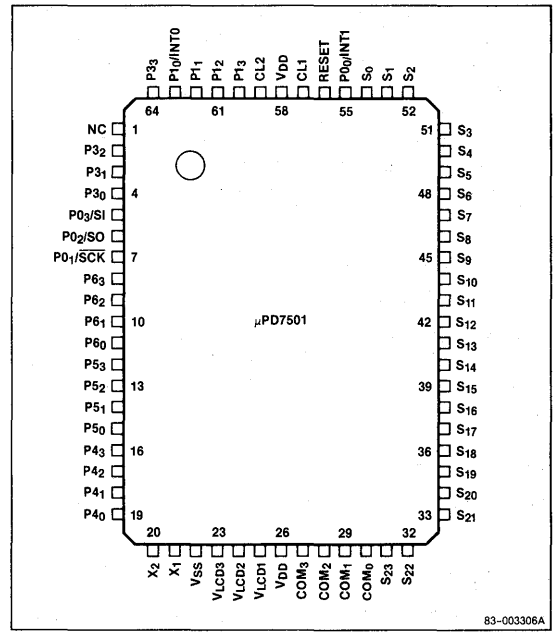
Features

- ☐ 1024 x 8-bit program ROM
- ☐ 96 x 4-bit data RAM
- ☐ Interrupts
  - —External: INT0, INT1
  - —Internal: INTT (timer/event counter), INTS (serial interface)
- ☐ 8-bit timer/event counter
  - —Based on crystal oscillation
  - —External event counter (prescale option by 64)
- ☐ Serial interface
- ☐ LCD controller/driver
  - —Programmable multiplexing mode: triplex or quadruplex
  - —4 common lines (COM_0-COM_3)
  - —24 segment lines (S_0-S_{23})
- ☐ Standby modes: stop, halt
- ☐ Data retention mode
- ☐ I/O ports
  - —3 input ports
  - —1 output port
  - —3 I/O ports
- ☐ RC oscillation clock
- ☐ Crystal oscillation clock
- ☐ 2.5 to 6.0 V operating voltages
- ☐ CMOS technology

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7501G-12	64-pin plastic miniflat	410 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	NC	No connection
2-4, 64	$P3_3$-$P3_0$	Output port 3
5-7, 55	$P0_3$/SI $P0_2$/SO $P0_1$/SCK $P0_0$/INT1	Input port 0, serial I/O interface, external interrupt
8-11	$P6_3$-$P6_0$	I/O port 6
12-15	$P5_3$-$P5_0$	I/O port 5
16-19	$P4_3$-$P4_0$	I/O port 4
20, 21	X2, X1	Crystal clock/external event input
22	V_{SS}	Ground
23-25	V_{LCD3}-V_{LCD1}	LCD bias voltage inputs
26, 58	V_{DD}	Positive power supply
27-30	COM_0-COM_3	LCD backplane driver outputs
31-54	S_{23}-S_0	LCD segment driver outputs
56	RESET	Reset input
57, 59	CL1, CL2	System clock input
60-63	$P1_3$-$P1_1$ $P1_0$/INT0	Input port 1, external interrupt

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Pin Functions

$P0_3$-$P0_0$ [Input Port 0]; SI, SO, $\overline{SCK}$ [Serial I/O Interface]; and INT1 [External Interrupt]

This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO, and the serial clock $\overline{SCK}$ (active low) used for synchronizing data transfer make up the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT1. If $P0_0$/INT1 is unused, it should be connected to V_{SS}. If $P0_1/\overline{SCK}$, $P0_2$/SO, or $P0_3$/SI are unused, connect them to V_{SS} or V_{DD}.

$P1_3$-$P1_0$ [Input Port 1] and INT0 [External Interrupt]

Four-bit input port. Line $P1_0$ is shared with external interrupt INT0, a rising edge-triggered interrupt. If $P1_0$/INT0 is unused, connect it to V_{SS}. If $P1_3$-$P1_1$ are unused, connect them to V_{SS} or V_{DD}.

$P3_3$-$P3_0$ [Output Port 3]

Four-bit latched three-state output port 3. Leave unused pins open.

$P4_3$-$P4_0$ [I/O Port 4]

Four-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 5. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [I/O Port 5]

Four-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [I/O Port 6]

Four-bit input/latched three-state output port. The port 6 mode select register configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

COM_3-COM_0 [LCD Backplane Driver Outputs]

Leave unused pins open.

S_{23}-S_0 [LCD Segment Driver Outputs]

Leave unused pins open.

V_{LCD3}-V_{LCD1} [LCD Bias Voltage Inputs]

LCD bias voltage supply to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}. Leave unused pins open.

X2, X1 [Crystal Clock/External Event Input]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, input event pulses to X1 and leave X2 open. If X1 is not used, leave it open. If X2 is not used, connect it to V_{SS}.

CL1, CL2 [System Clock Input]

Connect an 82-kΩ resistor across CL1 and CL2, and connect a 33-pF capacitor from CL1 to V_{SS}. Alternatively, connect an external clock source to CL1 and leave CL2 open.

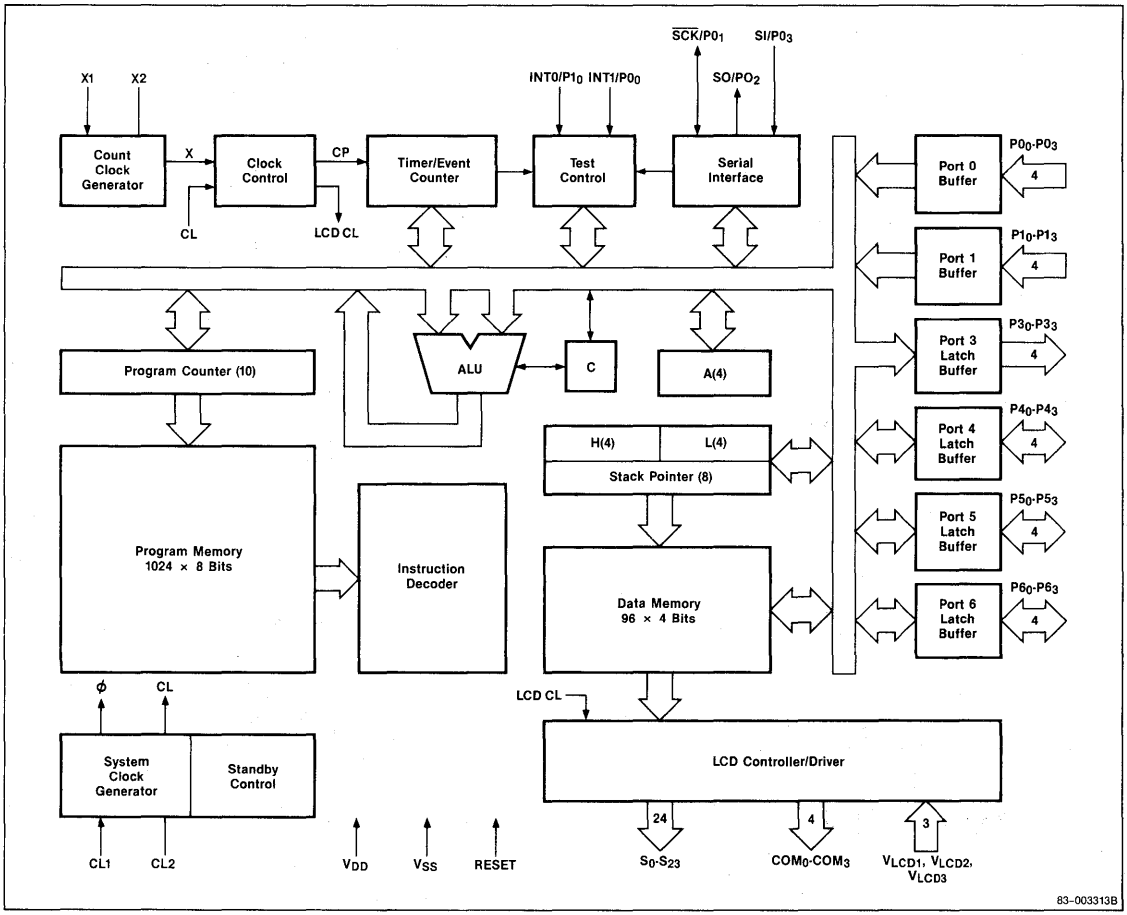
RESET [Reset Input]

A high-level input to the RESET pin initializes the μPD7501 after power-up.

V_{DD} [Positive Power Supply]

Apply a single voltage in the range +2.7 to +6.0 volts for proper operation.

Block Diagram



Details of some blocks on the diagram are illustrated in figures 1 through 6 as listed below.

Figure	Title
1	Interface at Input/Output Ports
2	Clock Control
3	Timer/Event Counter
4	Test Control
5	Serial Interface
6	LCD Controller/Driver

Figure 1. Interface at Input/Output Ports

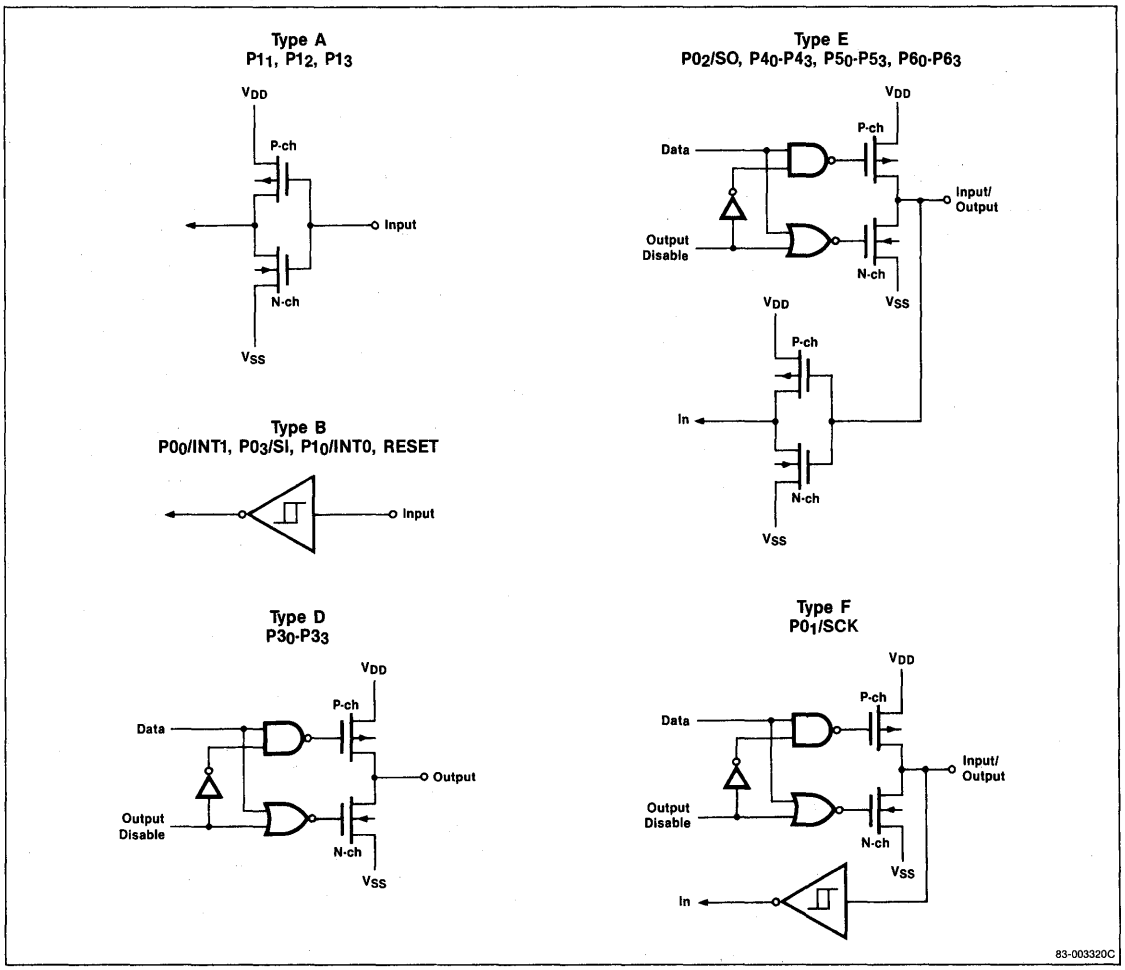
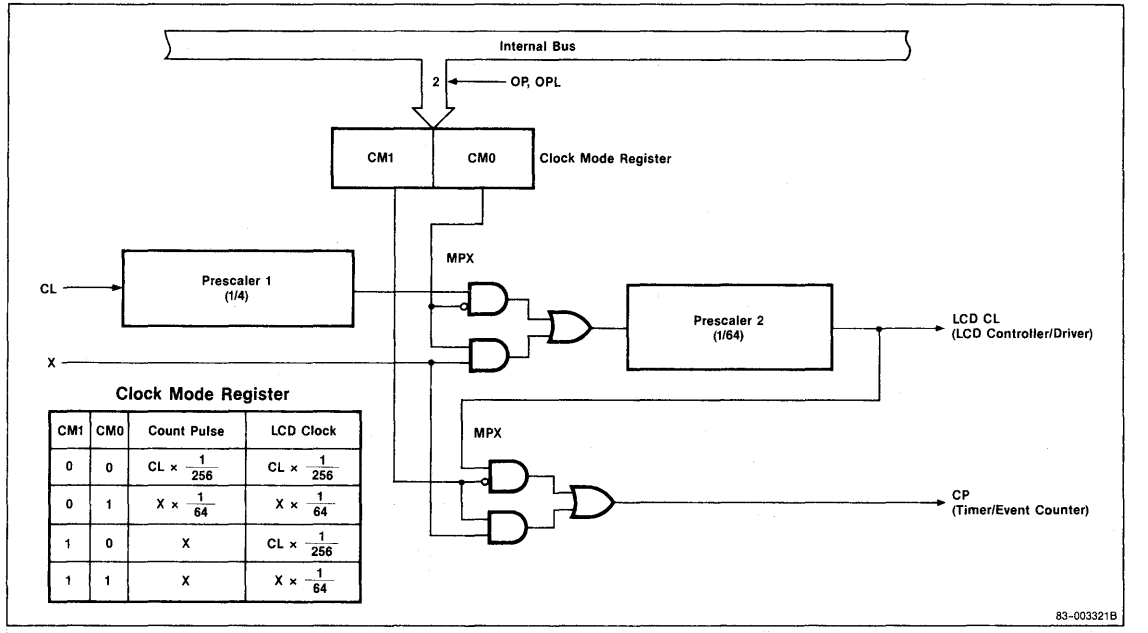


Figure 2. Clock Control



Clock Mode Register

CM1	CM0	Count Pulse	LCD Clock
0	0	CL × $\frac{1}{256}$	CL × $\frac{1}{256}$
0	1	X × $\frac{1}{64}$	X × $\frac{1}{64}$
1	0	X	CL × $\frac{1}{256}$
1	1	X	X × $\frac{1}{64}$

Figure 3. Timer/Event Counter

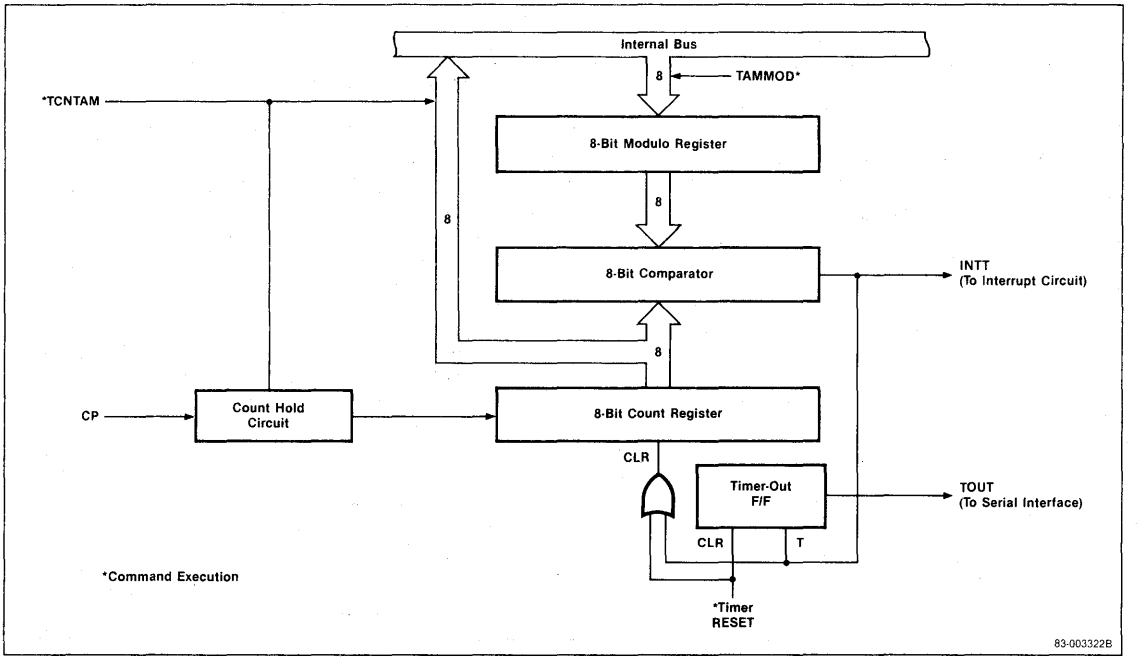


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Figure 4. Test Control

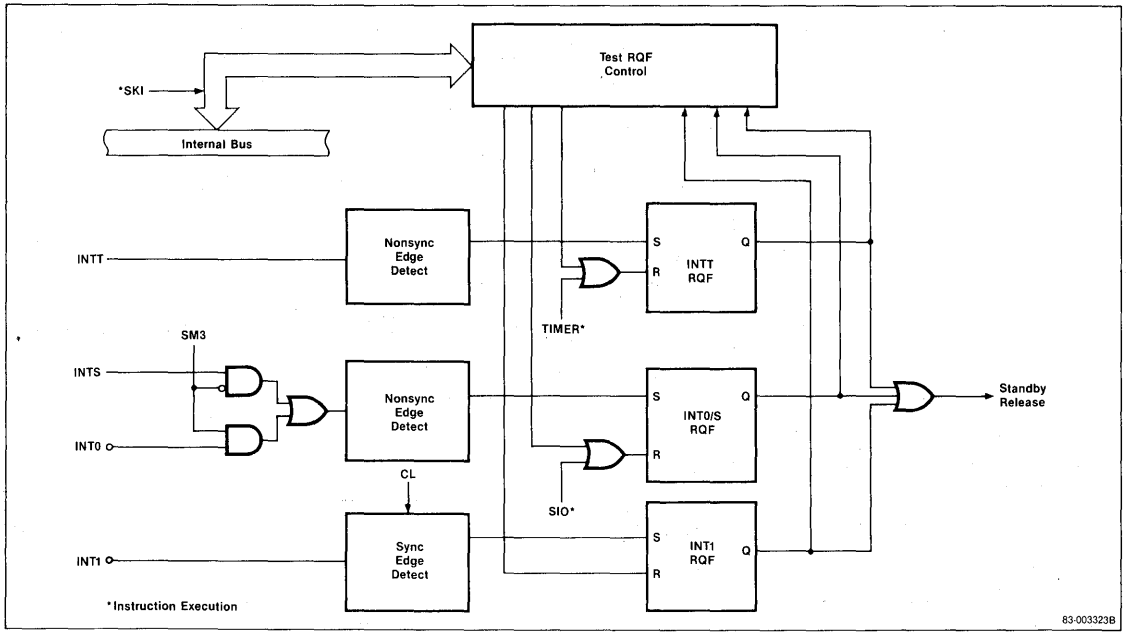


Figure 5. Serial Interface

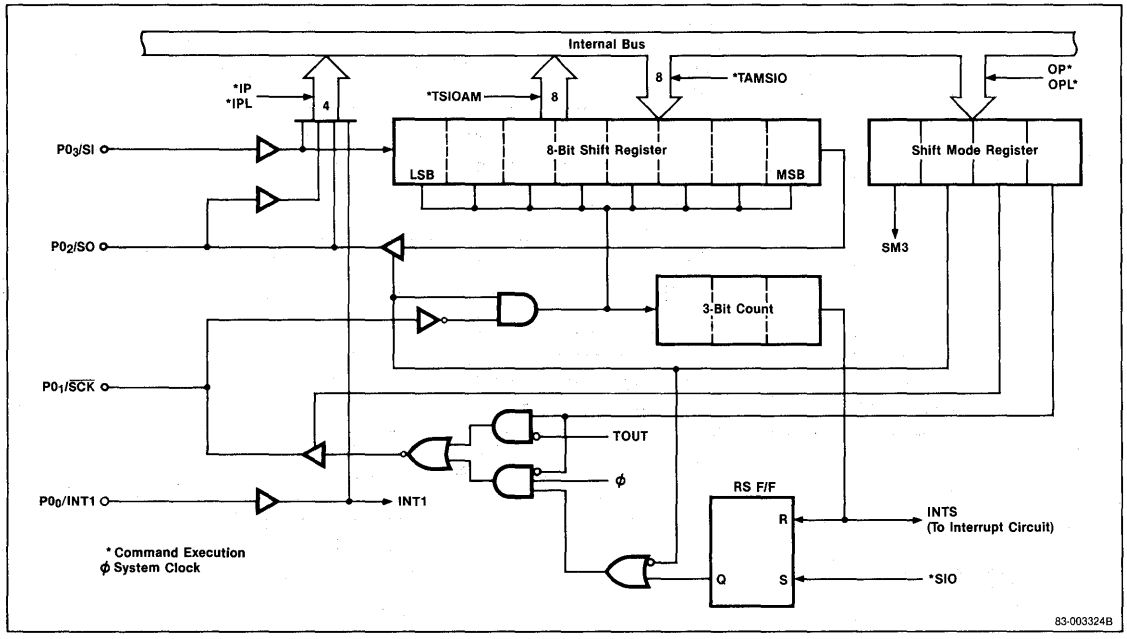
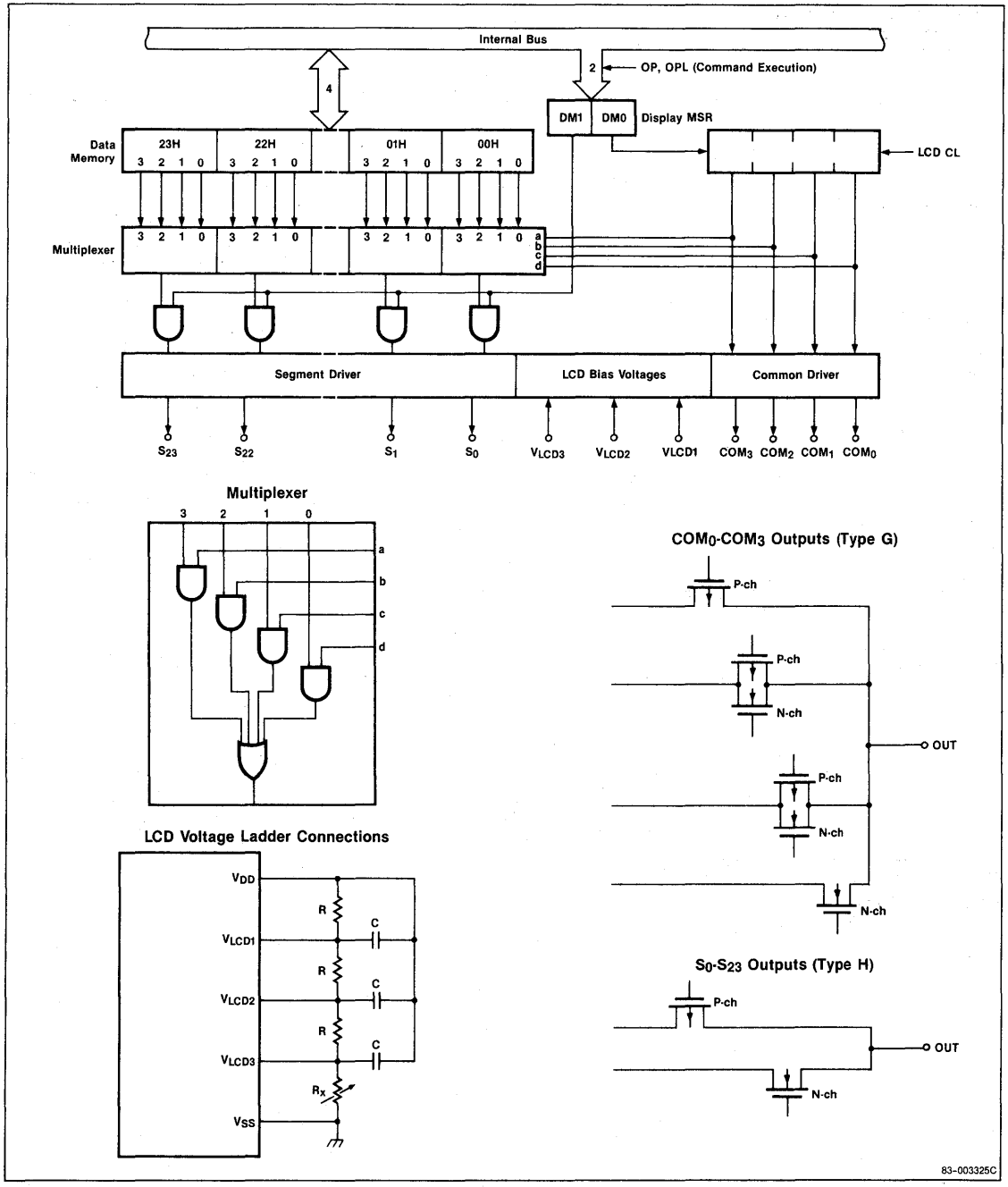


Figure 6. LCD Controller/Driver



DC Characteristics

For V_{DD} = 2.7 to 6.0 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.5	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA; V_{DD} = 4.5 to 6.0 V
		V_{DD} − 0.5			V	I_{OL} = −100 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 1.6 mA; V_{DD} = 4.5 to 6.0 V
				0.5	V	I_{OL} = 400 μA
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	I_{LIL2}			−10	μA	CL1, X1; V_I = 0 V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Output impedance (Note 1)	R_{COM}		3	5	kΩ	COM_0-COM_3; V_{DD} = 4.5 to 6.0 V
			5	15	kΩ	COM_0-COM_3
	R_S		15	20	kΩ	S_0-S_{23}; V_{DD} = 4.5 to 6.0 V
			20	60	kΩ	S_0-S_{23}
Supply voltage	V_{DDDR}	2.0		6.0	V	Data retention mode
Supply current	I_{DD1}		300	900	μA	Normal operation, V_{DD} = 5 V ±10%; R = 82 kΩ ±2%, C = 33 pF ±5%
			70	300	μA	Normal operation, V_{DD} = 3 V ±10%; R = 160 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		1.0	20	μA	Stop mode, X1 = 0 V; V_{DD} = 5 V ±10%
			0.3	10	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%
	I_{DDDR}		0.2	10	μA	Data retention mode, V_{DDDR} = 2.0 V

Note:

(1) V_{LCD} = 2.7 V to V_{DD}
$V_{LCD1} = V_{DD} - (1/3)\ V_{LCD}$
$V_{LCD2} = V_{DD} - (2/3)\ V_{LCD}$
$V_{LCD3} = V_{DD} - V_{LCD}$

DC Characteristics (cont)

For V_{DD} = 2.5 to 3.3 Volts

$T_A = -10$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	$0.8\ V_{DD}$		V_{DD}	V	Except CL1, X1
	V_{IH2}	$V_{DD} - 0.3$		V_{DD}	V	CL1, X1
	V_{IHDR}	$0.9\ V_{DDDR}$		$V_{DDDR} + 0.2$	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		$0.2\ V_{DD}$	V	Except CL1, X1
	V_{IL2}	0		0.3	V	CL1, X1
Output voltage, high	V_{OH}	$V_{DD} - 0.5$			V	$I_{OH} = -80\ \mu A$
Output voltage, low	V_{OL}			0.5	V	$I_{OL} = 350\ \mu A$
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	$V_O = 0$ V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		50	250	μA	Normal operation, $V_{DD} = 3$ V ±10%; R = 240 kΩ ±2%, C = 33 pF ±5%
			35	230	μA	Normal operation, $V_{DD} = 2.5$ V; R = 240 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		0.3	10	μA	Stop mode, X1 = 0 V; $V_{DD} = 3$ V ±10%
			0.2	10	μA	Stop mode, X1 = 0 V; $V_{DD} = 2.5$ V
	I_{DDDR}		0.2	10	μA	Data retention mode, $V_{DDDR} = 2.0$ V

3

Absolute Maximum Ratings

Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 V to V_{DD} + 0.3 V
Output current high, I_{OH}	
Per pin	−17 mA
Total, output ports	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Total, output ports	55 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

Parameter	Symbol	Limits Typ	Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	f = 1 MHz; unmeasured pins returned to V_{SS}
Output capacitance	C_O		15	pF	
I/O capacitance	C_{IO}		15	pF	

AC Characteristics

For V_{DD} = 2.7 to 6.0 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	V_{DD} = 5 V ±10%; R = 82 kΩ ±2% (Note 1)
		75	100	120	kHz	V_{DD} = 3 V ±10%; R = 160 kΩ ±2% (Note 1)
		75		135	kHz	R = 160 kΩ ±2% (Note 1)
	f_C	10		410	kHz	CL1, external clock, 50% duty; V_{DD} = 4.5 to 6.0 V
		10		125	kHz	CL1, external clock, 50% duty; V_{DD} = 2.7 V
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.2		50	μs	CL1, external clock; V_{DD} = 4.5 to 6.0 V
		4.0		50	μs	CL1, external clock; V_{DD} = 2.7 V
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input, 50% duty; V_{DD} = 4.5 to 6.0 V
		0		125	kHz	X1, external pulse input, 50% duty; V_{DD} = 2.7 V
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.2			μs	X1, external pulse input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	X1, external pulse input; V_{DD} = 2.7 V
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		8.0			μs	$\overline{SCK}$ as input
		4.9			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		16.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	$\overline{SCK}$ as input
		2.2			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		8.0			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	300			ns	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	450			ns	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			850	ns	V_{DD} = 4.5 V to 6.0 V
				1200	ns	
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	$2/f_\phi$			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leqq 60$ ppm.

AC Characteristics (cont)

For V_{DD} = 2.5 to 3.3 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	50		80	kHz	V_{DD} = 5 V ±10%; R = 240 kΩ ±2% (Note 1)
		50	64	77	kHz	V_{DD} = 2.5 V; R = 240 kΩ ±2% (Note 1)
	f_C	10		80	kHz	CL1, external clock, 50% duty
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	6.25		50	μs	CL1, external clock
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	6.25			μs	X1, external pulse input
$\overline{SCK}$ cycle time	t_{KCY}	12.5			μs	$\overline{SCK}$ as input
		25.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	6.25			μs	$\overline{SCK}$ as input
		11.5			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	1			μs	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			2	μs	
INT0 pulse width	t_{I0H}, t_{I0L}	30			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	$2/f_\phi$			μs	
RESET pulse width	t_{RSH}, t_{RSL}	30			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq$ 60 ppm.

Recommended R and C Values for System Clock Oscillation Circuit

T_A = −10 to +70°C

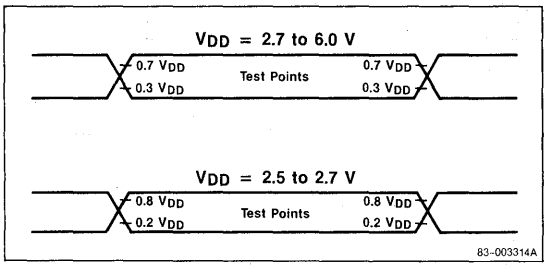
Supply Voltage Range	Recommended Values (Note 1)	Frequency Range
4.5 to 6.0 V	R = 82 kΩ ±2%	150 to 240 kHz, 200 kHz typical
2.7 to 3.3 V	R =160 kΩ ±2%	75 to 120 kHz, 100 kHz typical
2.7 to 6.0 V	R =160 kΩ ± 2%	75 to 135 kHz
2.5 to 3.3 V	R = 240 kΩ ±2%	50 to 80 kHz
2.5 V	R = 240 kΩ ±2 %	50 to 77 kHz

Note:

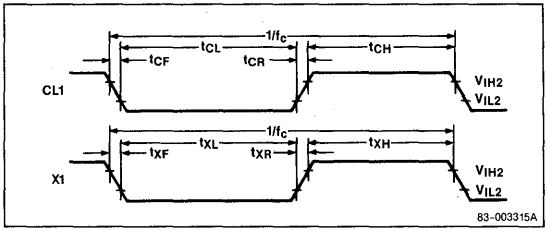
(1) C = 33 pF ±5%, $|\Delta C/°C| \leq$ 60 ppm.

Timing Waveforms

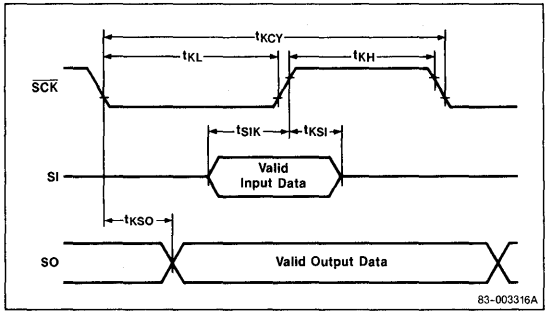
AC Test Points



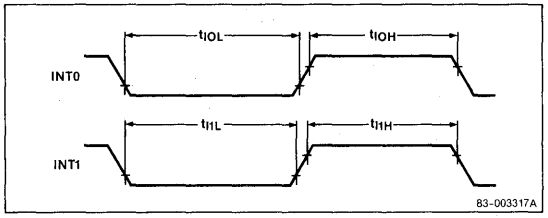
Clocks



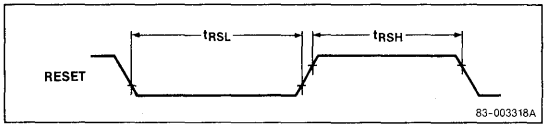
Serial Interface



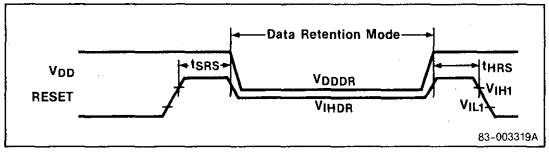
External Interrupts



Reset

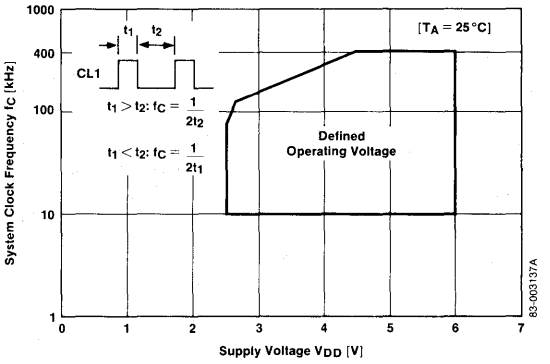


Data Retention

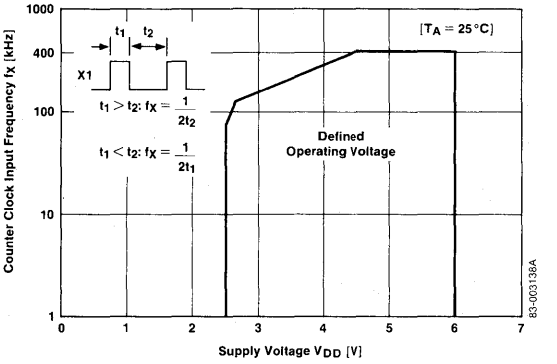


Operating Characteristics

f_C vs V_{DD}



f_X vs V_{DD}



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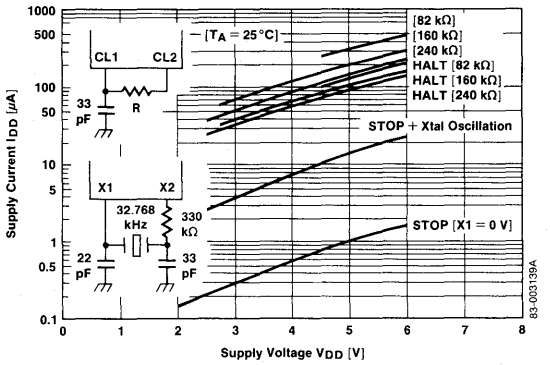
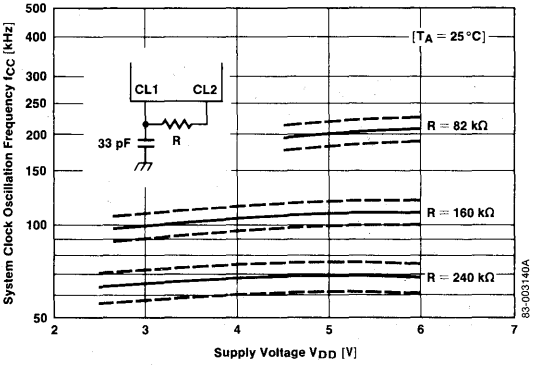
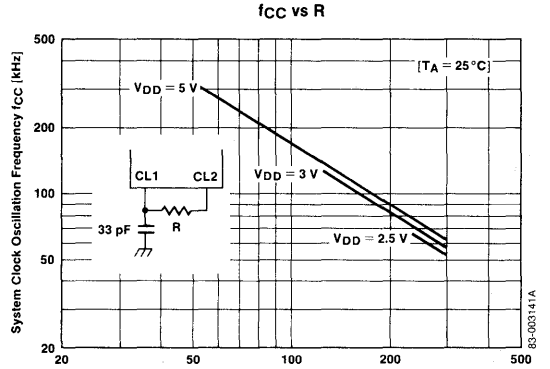
I_{DD} vs V_{DD}



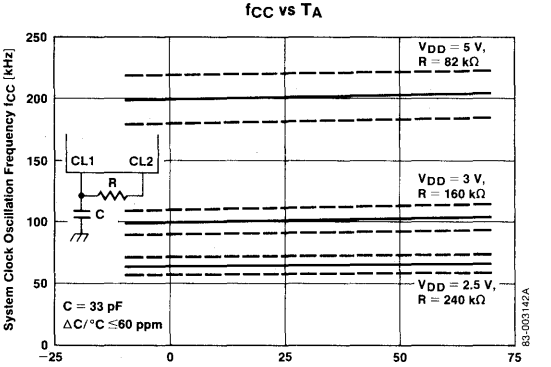
f_{CC} vs V_{DD}



f_{CC} vs R

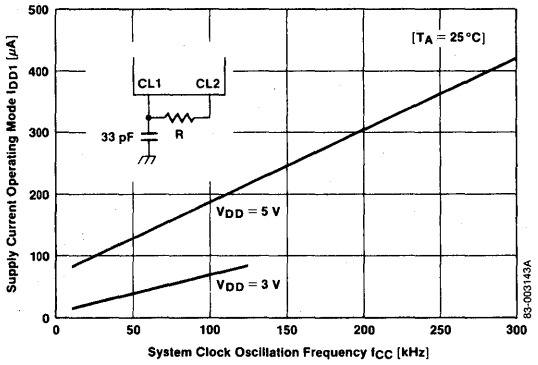


f_{CC} vs T_A

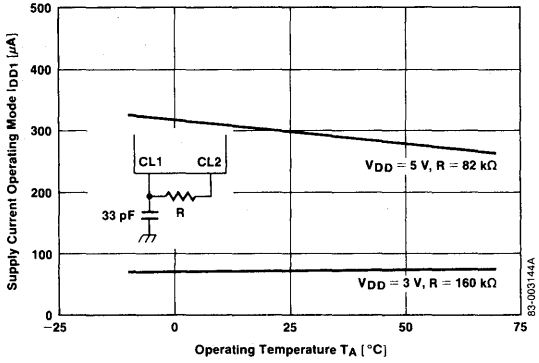


Operating Characteristics (cont)

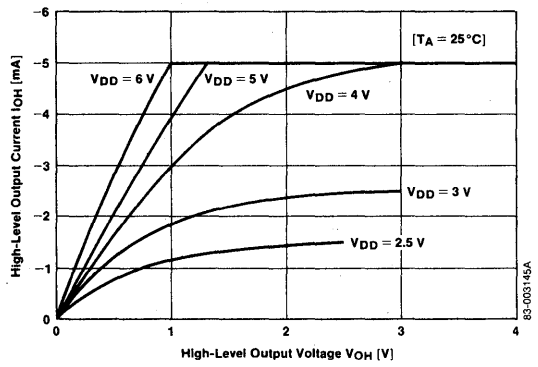
I_{DD1} vs f_{CC}



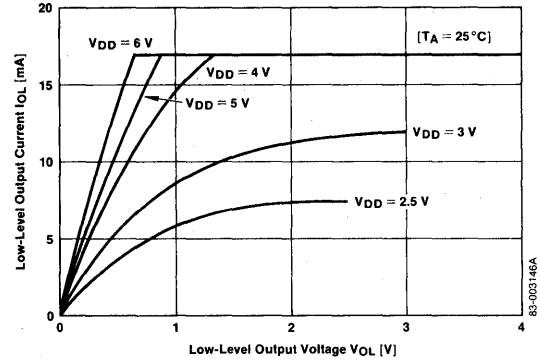
I_{DD1} vs T_A



I_{OH} vs V_{OH}



I_{OL} vs V_{OL}



μPD7502/03
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS WITH LCD CONTROLLER/DRIVER

Description

The μPD7502 and μPD7503 4-bit, single-chip CMOS microcomputers have advanced fourth-generation architecture with the functional blocks necessary for a single-chip controller, including an 8-bit timer/event counter, an 8-bit serial I/O, and an LCD controller/driver.

The instruction set includes the following types of instructions: addressing, table look-up, bit manipulation, vectored dump, auto increment or decrement data pointer, and conditional skip. These instructions maximize use of fixed program memory space.

Both devices are manufactured with the CMOS process and have a maximum power consumption of 900 μA at 5 V and 300 μA at 3 V. Halt and stop modes further reduce power consumption.

These devices are ideal for a wide range of solar- and battery-powered applications.

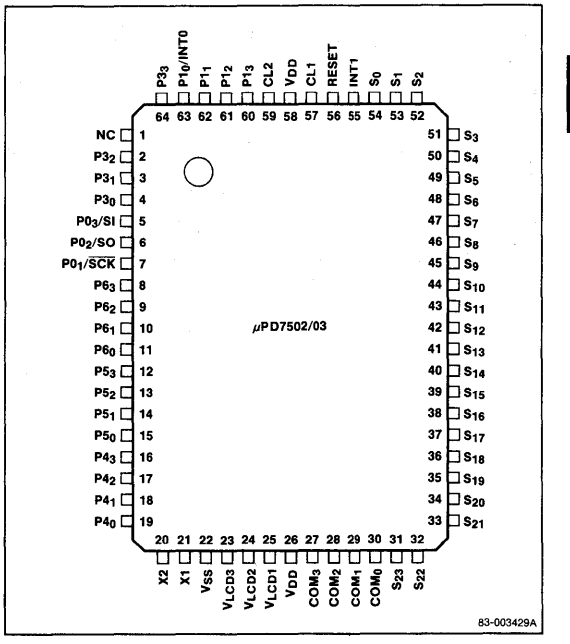
Features

- ☐ 92 powerful instructions
- ☐ Program ROM
  - — μPD7502: 2048 x 8-bit
  - — μPD7503: 4096 x 8-bit
- ☐ Data RAM
  - — μPD7502: 128 x 4-bit
  - — μPD5703: 224 x 4-bit
- ☐ Interrupts
  - — External: INT0, INT1
  - — Internal: INTT (timer/event counter)
    INTS (serial interface)
- ☐ 8-bit timer/event counter
  - — Based on crystal oscillation
  - — External event counter (prescale option by 64)
- ☐ Serial interface
- ☐ LCD controller/driver
  - — Programmable multiplexing mode: triplex or quadruplex
  - — 4 common lines (COM_0-COM_3)
  - — 24 segment lines (S_0-S_{23})
- ☐ Standby modes: stop, halt
- ☐ Data retention mode
- ☐ I/O ports
  - — 3-bit input port
  - — 4-bit input port
  - — 4-bit output port
  - — Two 4-bit I/O ports with 8-bit capability
  - — 4-bit I/O port with each bit configurable as an input or output
- ☐ RC oscillation clock
- ☐ Crystal oscillation clock
- ☐ 2.7 to 6.0 V operating voltage
- ☐ CMOS technology

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7502G-12	64-pin plastic miniflat	410 kHz
μPD7503G-12	64-pin plastic miniflat	410 kHz

Pin Configuration



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Pin Identification

No.	Symbol	Function
1	NC	No connection
2-4, 64	$P3_3$-$P3_0$	4-bit output port 3
5-7	$P0_3$/SI $P0_2$/$\overline{SO}$ $P0_1$/$\overline{SCK}$	3-bit input port 0, or serial I/O interface
8-11	$P6_3$-$P6_0$	4-bit I/O port 6
12-15	$P5_3$-$P5_0$	4-bit I/O port 5
16-19	$P4_3$-$P4_0$	4-bit I/O port 4
20, 21	X2, X1	Crystal clock/external event input port X
22	V_{SS}	Ground
23-25	V_{LCD3}-V_{LCD1}	LCD bias supply inputs
26, 58	V_{DD}	Positive power supply
27-30	COM_3-COM_0	LCD backplane driver outputs
31-54	S_{23}-S_0	LCD segment driver outputs
55	INT1	External interrupt
56	RESET	RESET input
57, 59	CL1, CL2	System clock input
60-63	$P1_3$-$P1_1$, $P1_0$/INT0	4-bit input port 1, or external interrupt INT0

Status of Unused Pins

Name	Pin Connection
CL2	Open
X1	V_{SS}
X2	Open
$P0_1$/$\overline{SCK}$ $P0_2$/SO $P0_3$/SI	V_{SS} or V_{DD}
$P1_0$/INT0	V_{SS}
$P1_1$-$P1_3$	V_{SS} or V_{DD}
$P3_0$-$P3_3$	Open
$P4_0$-$P4_3$ $P5_0$-$P5_3$ $P6_0$-$P6_3$	Input mode: V_{SS} or V_{DD} Output mode: Open
INT1	V_{SS}
S_0-S_{23} COM_0-COM_3 V_{LCD1}-V_{LCD3}	Open

Pin Functions

$P0_3$/SI, $P0_2$/SO, $P0_1$/$\overline{SCK}$ [Port 0 or Serial Interface]

This port can be configured as a 4-bit parallel input port 0 or as the 8-bit serial I/O interface under control of the serial mode select register. The serial interface consists of the serial input (SI), the serial output (SO), and the serial clock ($\overline{SCK}$), which synchronizes data transfer.

$P1_3$-$P1_1$, $P1_0$/INT0 [Port 1 or Interrupt]

4-bit input port 1. Line $P1_0$ is shared with external interrupt INT0, which is a rising edge-triggered interrupt.

$P3_3$-$P3_0$ [Port 3]

4-bit, latched three-state output port 3.

$P4_3$-$P4_0$ [Port 4]

4-bit input or latched three-state output port 4. Can perform 8-bit I/O in conjunction with port 5.

$P5_3$-$P5_0$ [Port 5]

4-bit input or latched three-state output port 5. Can perform 8-bit I/O in conjunction with port 4.

$P6_3$-$P6_0$ [Port 6]

4-bit input or latched three-state output port 6. The port 6 mode select register configures individual lines as inputs or outputs.

COM_3-COM_0 [LCD Backplane Driver Outputs]

LCD backplane driver outputs.

S_{23}-S_0 [LCD Segment Driver Outputs]

LCD segment driver outputs.

INT1 [Interrupt]

This external interrupt is a rising edge-triggered interrupt.

RESET

A high-level input to this pin initializes the μPD7502/7503.

X2, X1 [Crystal Clock/External Event Input Port X]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, input external event pulses to X1 and leave X2 open.

CL1, CL2 [System Clock Input]

Connect an 82-kΩ resistor across CL1 and CL2, and a 33-pF capacitor from CL1 to V_{SS}. Or, connect an external clock source to CL1 and leave CL2 open.

V_{LCD3}-V_{LCD1} [LCD Bias Voltage Inputs]

LCD bias voltage supply inputs to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.

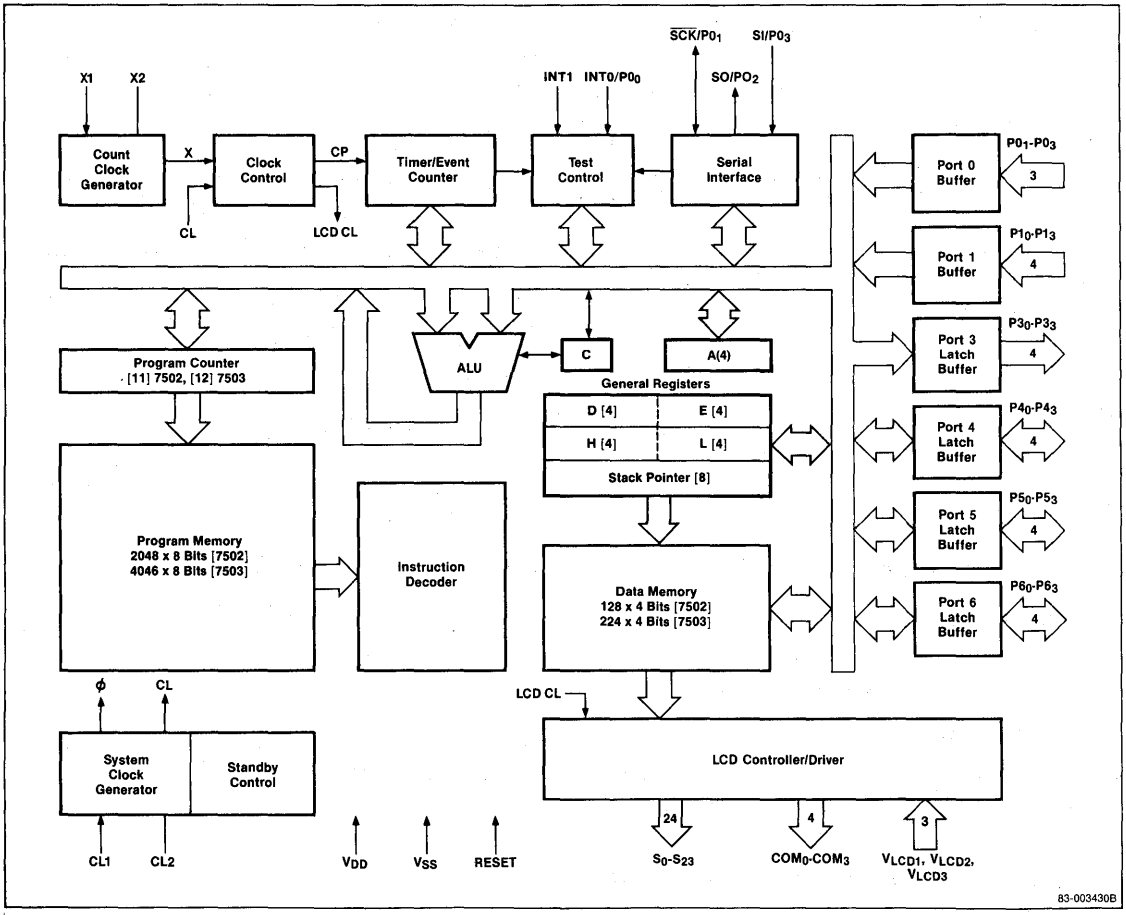
V_{DD}

Positive power supply. For proper operation, apply a single voltage from 2.7 to 6.0 V.

V_{SS}

Ground.

Block Diagram



See figures 1 through 8 for additional block diagram details.

Figure	Title
1	Data Memory Map
2	Program Memory Map
3	Interface at Input/Output Ports
4	Clock Control
5	Timer/Event Counter
6	Interrupt Control
7	Serial Interface
8	LCD Controller/Driver

Figure 1. Data Memory Map

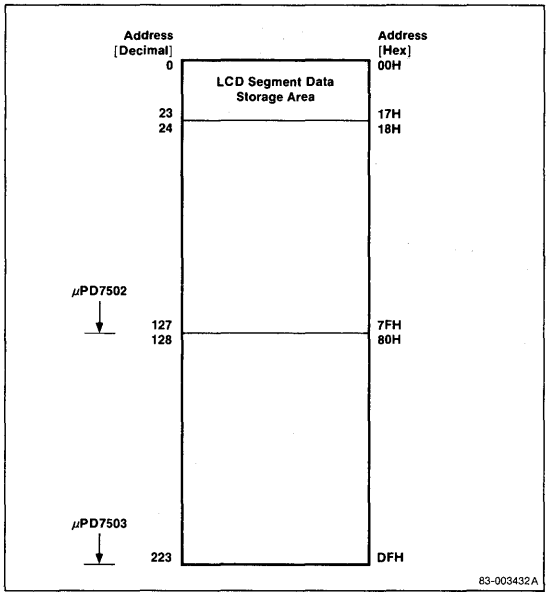


Figure 2. Program Memory Map

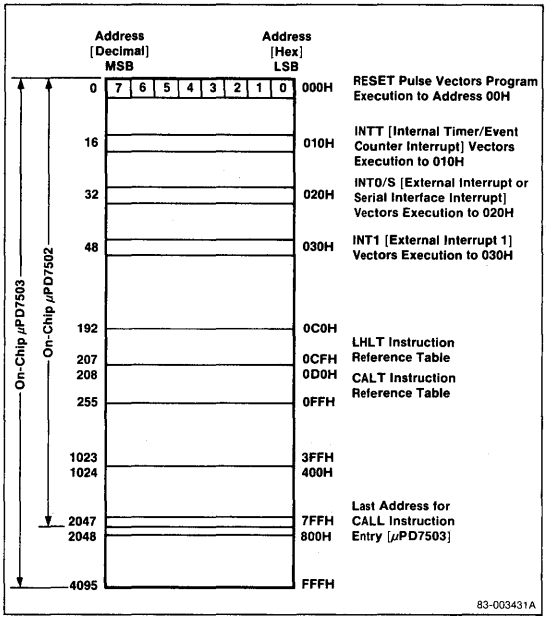


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Figure 3. Interface at Input/Output Ports

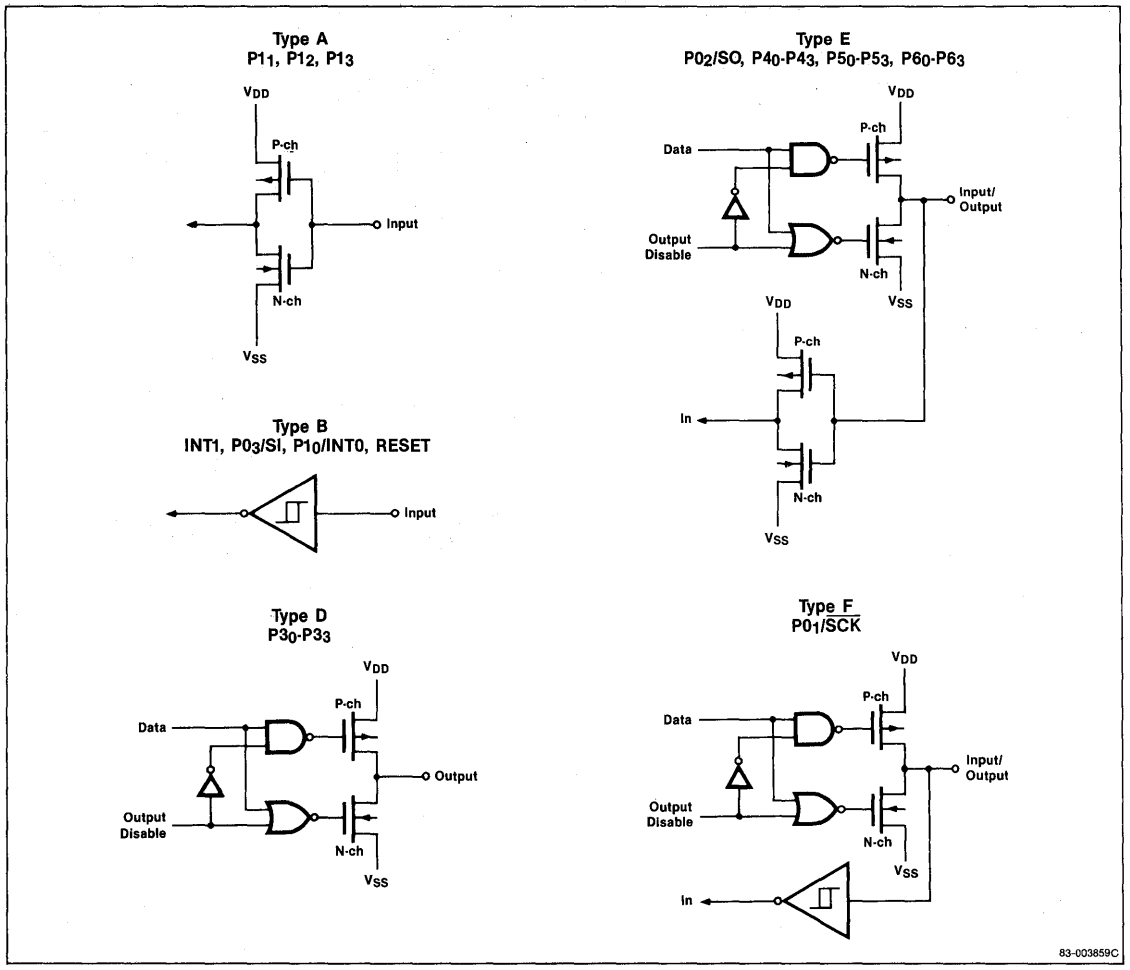
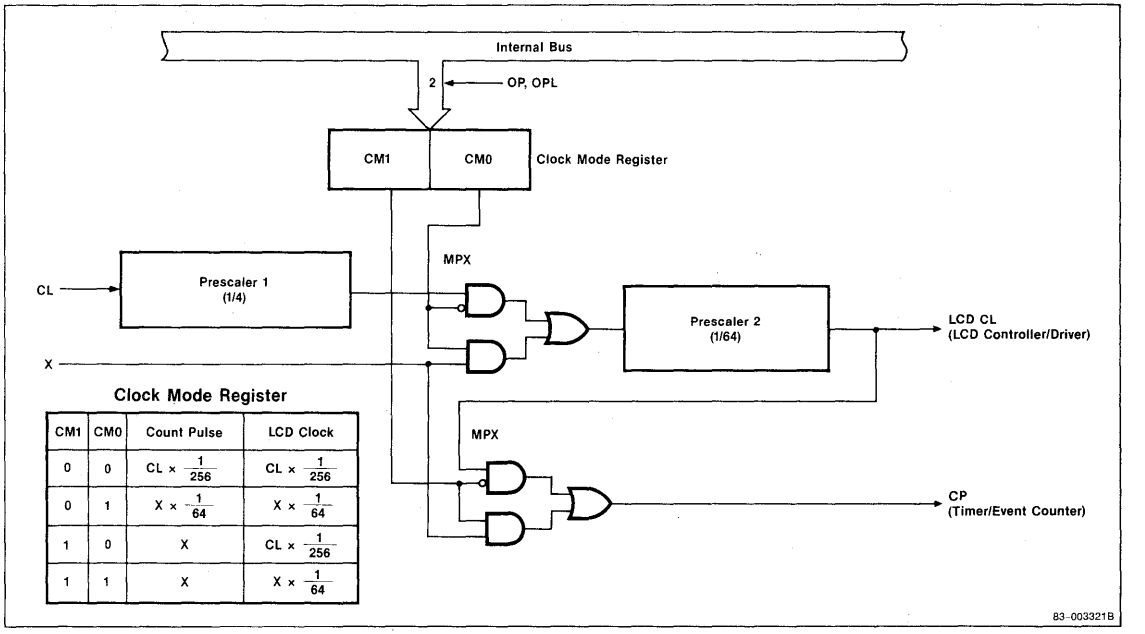


Figure 4. Clock Control



Clock Mode Register

CM1	CM0	Count Pulse	LCD Clock
0	0	CL × $\frac{1}{256}$	CL × $\frac{1}{256}$
0	1	X × $\frac{1}{64}$	X × $\frac{1}{64}$
1	0	X	CL × $\frac{1}{256}$
1	1	X	X × $\frac{1}{64}$

Figure 5. Timer/Event Counter

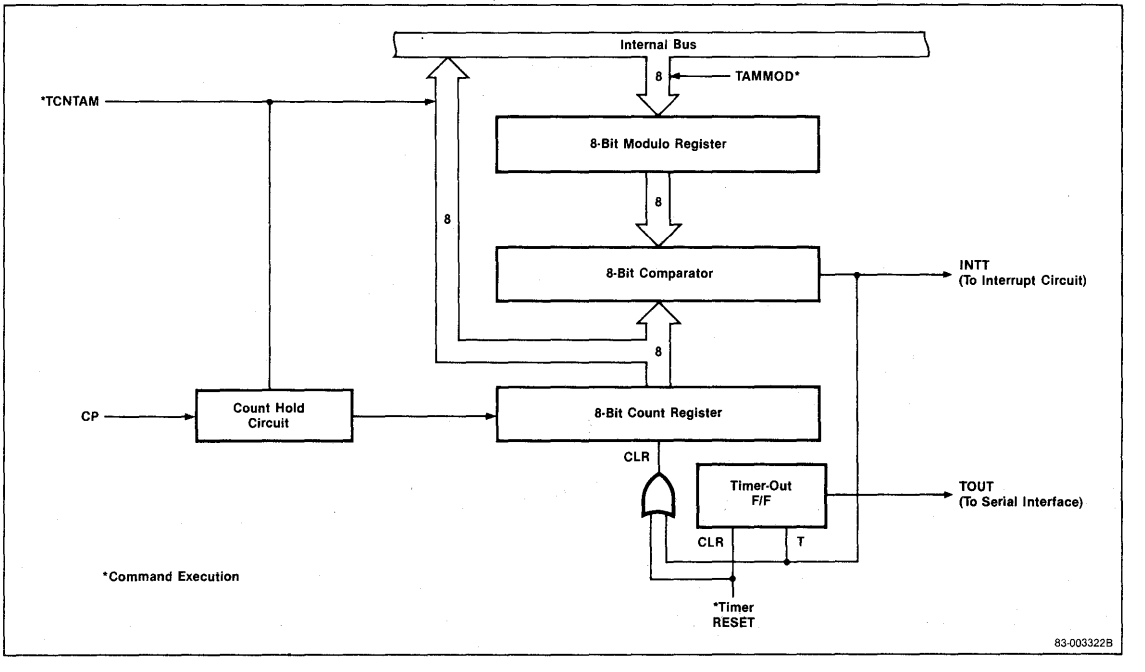


Figure 6. Interrupt Control

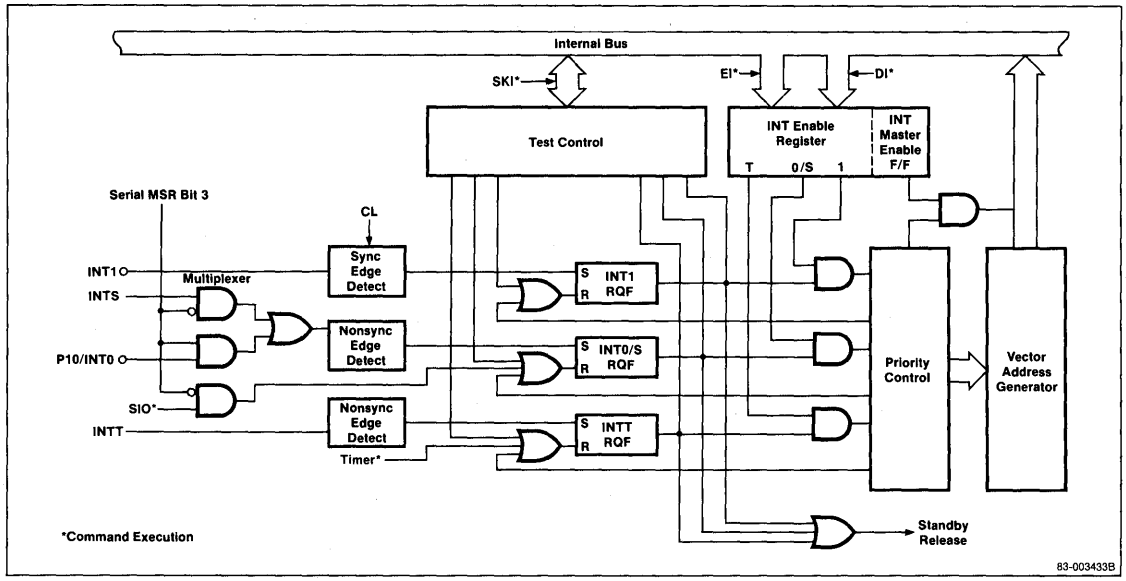


Figure 7. Serial Interface

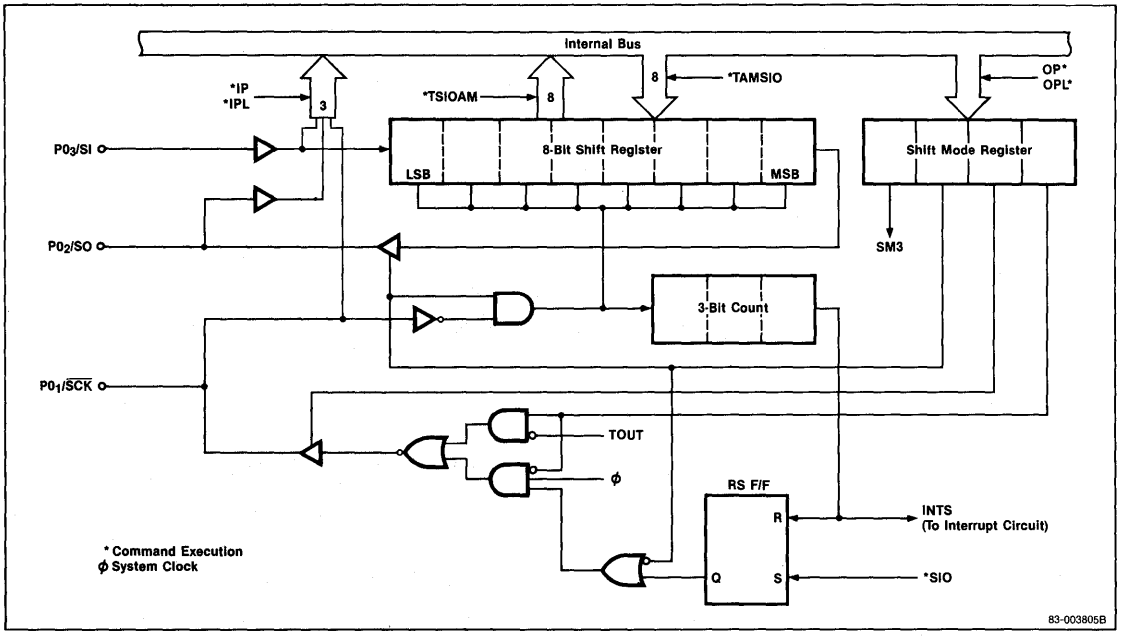
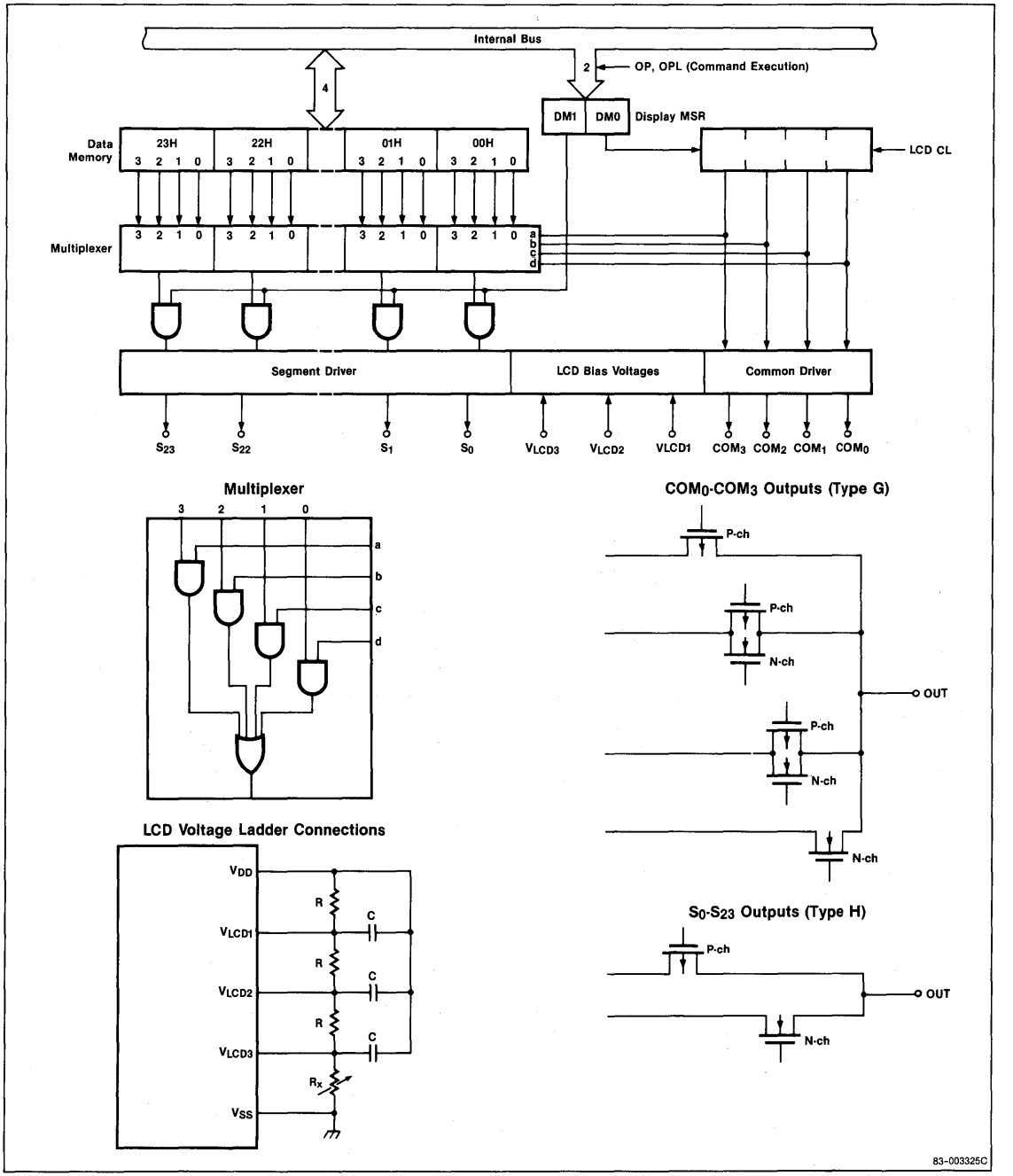


Figure 8. LCD Controller/Driver



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 V to V_{DD} + 0.3 V
Output current high, I_{OH}	
Per pin	−17 mA
Total, output ports	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Total, output ports	55 mA
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$; $V_{DD} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	$f_C = 1$ MHz Unmeasured pins returned to V_{SS}
Output capacitance	C_O			15	pF	
I/O capacitance	C_{IO}			15	pF	

DC Characteristics

For V_{DD} = 2.5 to 3.3 Volts

$T_A = -10$ to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.8 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.3		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.2 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.3	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 0.5			V	$I_{OH} = -80\ \mu A$
Output voltage, low	V_{OL}			0.5	V	$I_{OL} = 350\ \mu A$
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_{IN} = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_{IN} = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; $V_{IN} = 0$ V
	I_{LIL2}			−10	μA	CL1, X1; $V_{IN} = 0$ V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	$V_O = 0$ V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		50	250	μA	Normal operation, $V_{DD} = 3$ V ± 10%; R = 240 kΩ ±2%, C = 33 pF ±5%
			35	230	μA	Normal operation, $V_{DD} = 2.5$ V; R = 240 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		0.3	10	μA	Stop mode, X1 = 0 V; $V_{DD} = 3$ V ±10%
			0.2	10	μA	Stop mode, X1 = 0 V; $V_{DD} = 2.5$ V
	I_{DDDR}		0.2	10	μA	Data retention mode, $V_{DDDR} = 2.0$ V

DC Characteristics (cont)

For V_{DD} == 2.7 to 6.0 Volts

$T_A = -10$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	$V_{DD} - 0.5$		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		$V_{DDDR} + 0.2$		RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.5	V	CL1, X1
Output voltage, high	V_{OH}	$V_{DD} - 1.0$			V	$I_{OH} = -1.0$ mA, $V_{DD} = 4.5$ to 6.0 V
		$V_{DD} - 0.5$			V	$I_{OL} = -100\ \mu A$
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 1.6$ mA, $V_{DD} = 4.5$ to 6.0 V
				0.5	V	$I_{OL} = 400\ \mu A$
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; $V_I = 0$ V
	I_{LIL2}			−10	μA	CL1, X1
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	$V_O = 0$ V
Output impedance (1)	R_{COM}		3	5	kΩ	COM_0-COM_3; $V_{DD} = 4.5$ to 6.0 V
			5	15	kΩ	COM_0-COM_3
	R_S		15	20	kΩ	S_0-S_{23}; $V_{DD} = 4.5$ to 6.0 V
			20	60	kΩ	S_0-S_{23}
Supply voltage	V_{DDDR}	2.0		6.0	V	Data retention mode
Supply current	I_{DD1}		300	900	μA	Normal operation, $V_{DD} = 5$ V ± 10%; R = 82 kΩ ± 2%, C = 33 pF ± 5%
			70	300	μA	Normal operation, $V_{DD} = 3$ V ± 10%; R = 160 kΩ ± 2%, C = 33 pF ± 5%
	I_{DD2}		1.0	20	μA	Stop mode, X1 = 0 V; $V_{DD} = 5$ V ± 10%
			0.3	10	μA	Stop mode, X1 = 0 V; $V_{DD} = 3$ V ± 10%
	I_{DDDR}		0.2	10	μA	Data retention mode, $V_{DDDR} = 2.0$ V

Note:

(1) $V_{LCD} = 2.7$ V to V_{DD}
$V_{LCD1} = V_{DD} - (1/3)\ V_{LCD}$
$V_{LCD2} = V_{DD} - (2/3)\ V_{LCD}$
$V_{LCD3} = V_{DD} - V_{LCD}$

3

AC Characteristics

For V_{DD} = 2.7 to 6.0 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	V_{DD} = 5 V ±10%; R = 82 kΩ ±2% (Note 1)
		75	100	120	kHz	V_{DD} = 3 V ±10%; R = 160 kΩ ±2% (Note 1)
		75		135	kHz	R = 160 kΩ ±2% (Note 1)
	f_C	10		410	kHz	CL1, external clock, 50% duty; V_{DD} = 4.5 to 6.0 V
		10		125	kHz	CL1, external clock, 50% duty; V_{DD} = 2.7 V
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.2		50	μs	CL1, external clock; V_{DD} = 4.5 to 6.0 V
		4.0		50	μs	CL1, external clock; V_{DD} = 2.7 V
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input, 50% duty; V_{DD} = 4.5 to 6.0 V
		0		125	kHz	X1, external pulse input, 50% duty; V_{DD} = 2.7 V
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.2			μs	X1, external pulse input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	X1, external pulse input; V_{DD} = 2.7 V
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		8.0			μs	$\overline{SCK}$ as input
		4.9			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		16.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	$\overline{SCK}$ as input
		2.2			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		8.0			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	300			ns	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	450			ns	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			850	ns	V_{DD} = 4.5 V to 6.0 V
				1200	ns	
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	$2/f_\phi$			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leqq$ 60 ppm.

AC Characteristics (cont)

For V_{DD} = 2.7 to 5.5 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	50		80	kHz	V_{DD} = 5 V ±10%; R = 240 kΩ ±2% (Note 1)
		50	64	77	kHz	V_{DD} = 2.5 V; R = 240 kΩ ±2% (Note 1)
	f_C	10		80	kHz	CL1, external clock, 50% duty
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	6.25		50	μs	CL1, external clock
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	6.25			μs	X1, external pulse input
$\overline{SCK}$ cycle time	t_{KCY}	12.5			μs	$\overline{SCK}$ as input
		25			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	6.25			μs	$\overline{SCK}$ as input
		11.5			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	1			μs	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			2	μs	
INT0 pulse width	t_{I0H}, t_{I0L}	30			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	$2/f_\phi$			μs	
RESET pulse width	t_{RSH}, t_{RSL}	30			μs	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq$ 60 ppm.

Recommended R and C Values for System Clock Oscillation Circuit

T_A = −10 to +70°C

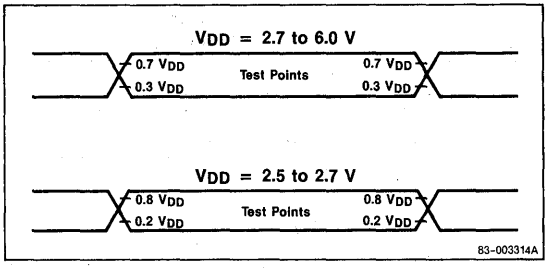
Supply Voltage Range	Recommended Values (Note 1)	Frequency Range
4.5 to 6.0 V	R = 82 kΩ ±2%	150 to 250 kHz, 200 kHz typical
2.7 to 3.3 V	R =160 kΩ ±2%	75 to 120 kHz, 100 kHz typical
2.7 to 6.0 V	R =160 kΩ± 2%	75 to 135 kHz
2.5 to 3.3 V	R = 240 kΩ ±2%	50 to 80 kHz
2.5 to 6.0 V	R = 240 kΩ ±2 %	50 to 85 kHz

Note:

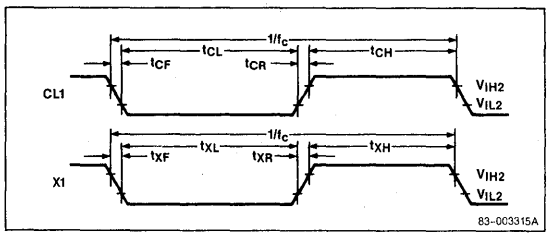
(1) C = 33 pF ±5%, $|\Delta C/°C| \leq$ 60 ppm.

Timing Waveforms

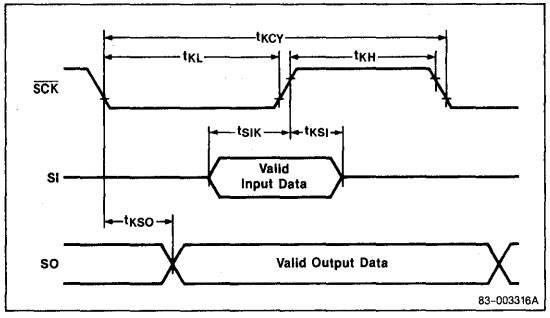
Timing Measurement Points



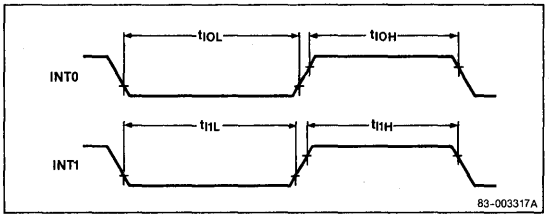
Clocks



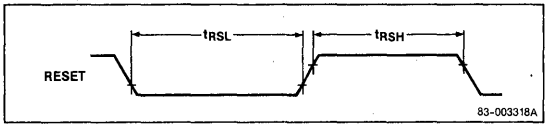
Serial Interface



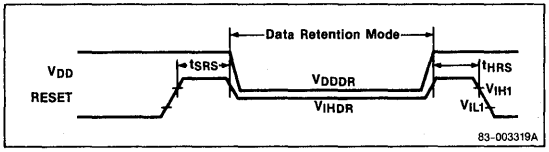
External Interrupts



Reset



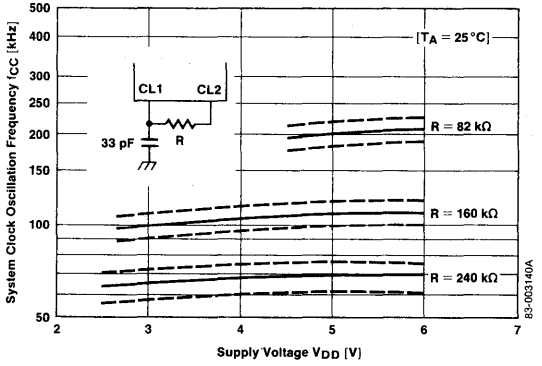
Data Retention Mode



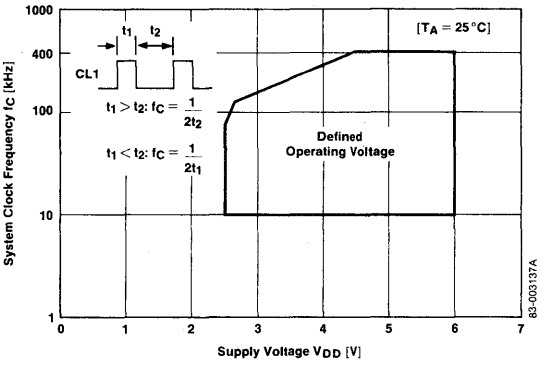
Operating Characteristics

$T_A = 25°C$

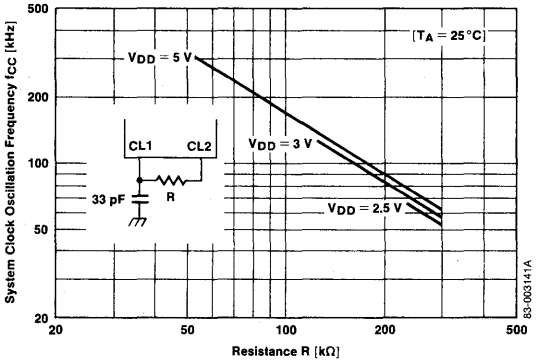
f_{CC} vs V_{DD}



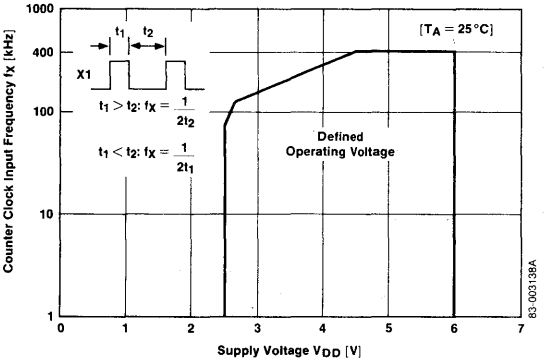
f_C vs V_{DD}



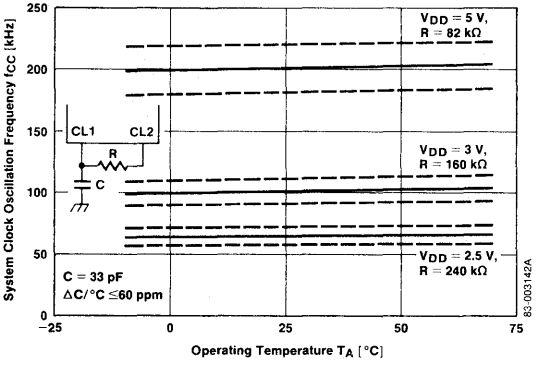
f_{CC} vs R



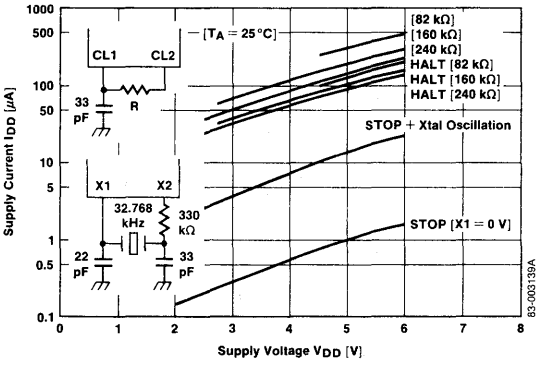
f_X vs V_{DD}



f_{CC} vs T_A



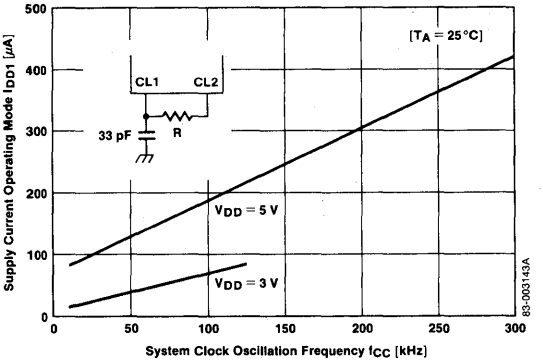
I_{DD} vs V_{DD}



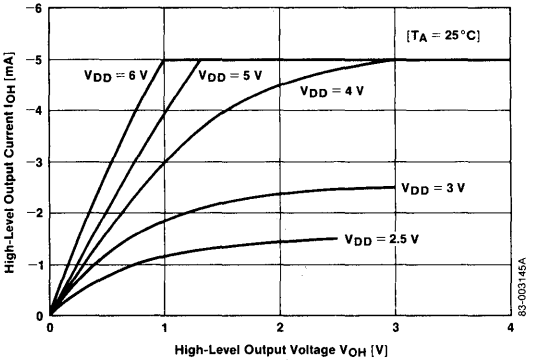
3

Operating Characteristics (cont)

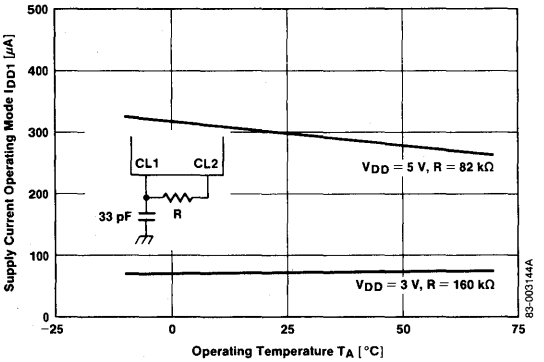
I_{DD1} vs f_{CC}



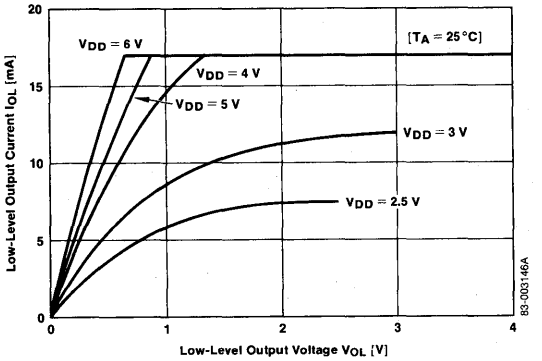
I_{OH} vs V_{OH}



I_{DD1} vs T_A



I_{OL} vs V_{OL}



μPD7506
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER

Description

The μPD7506 CMOS 4-bit single chip microcomputer has the μPD7500 series architecture. Twenty-two I/O lines are organized into the 2-bit input port 0, the 4-bit output port 2, and the 4-bit I/O ports 1, 4, 5, and 6. The device executes 58 of the μPD7500 Set B instructions, and has a 5-μs instruction cycle time. The subroutine stack is implemented in RAM for greater nesting depth and flexibility.

Due to the CMOS process, the device has a maximum power consumption of 600 μA at 5 V, and this is further reduced in halt and stop modes.

Features

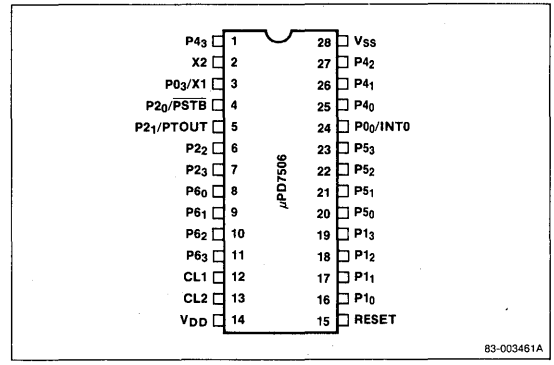
- ☐ 1024 x 8-bit program ROM
- ☐ 64 x 4-bit data RAM
- ☐ 8-bit timer/event counter
- ☐ Two 4-bit general-purpose registers
- ☐ Two testable interrupts
- ☐ 5-μs instruction cycle/400 kHz external clock
- ☐ 600 μA max current consumption
- ☐ 2 standby modes
- ☐ 22 I/O lines

Ordering Information

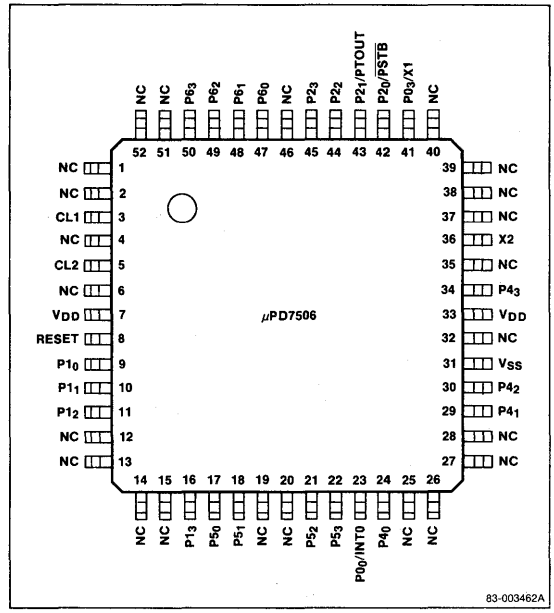
Part No.	Package Type	Max Frequency of Operation
μPD7506C	28-pin plastic DIP	410 kHz
μPD7506CT	28-pin plastic shrink DIP	410 kHz
μPD7506G-00	52-pin plastic miniflat	410 kHz

Pin Configurations

28-Pin Plastic DIPs



52-Pin Plastic Miniflat



Pin Identification

28-Pin Plastic DIPs

No.	Symbol	Function
1, 25-27	$P4_3$-$P4_0$	4-bit I/O port 4
2	X2	External event input
3	$P0_3$/X1	Input port 0/Clock input
4	$P2_0$/$\overline{PSTB}$	Output port 2/Output strobe
5	$P2_1$/PTOUT	Output port 2/Timer out F/F signal
6-7	$P2_2$-$P2_3$	Output port 2
8-11	$P6_0$-$P6_3$	4-bit I/O port 6
12, 13	CL1, CL2	System clock input
14	V_{DD}	Positive power supply
15	RESET	RESET input
16-19	$P1_0$-$P1_4$	4-bit I/O port 1
20-23	$P5_0$-$P5_3$	4-bit I/O port 5
24	$P0_0$/INT0	Input port 0/External Interrupt
28	V_{SS}	Ground

52-Pin Plastic Miniflat

No.	Symbol	Function
3, 5	CL1, CL2	System clock input
7, 33	V_{DD}	Positive power supply
8	RESET	RESET input
9-11, 16	$P1_0$-$P1_4$	4-bit I/O port 1
16-18, 21	$P5_0$-$P5_3$	4-bit I/O port 5
23	$P0_0$/INT0	Input port 0/External interrupt
24, 29, 30, 34	$P4_0$-$P4_3$	4-bit I/O port 4
31	V_{SS}	Ground
36	X2	External event input
41	$P0_3$/X1	Input port 0/Clock input
42	$P2_0$/$\overline{PSTB}$	Output port 2/Output strobe
43	$P2_1$/PTOUT	Output port 2/Timer out F/F signal
44, 45	$P2_2$-$P2_3$	Output port 2
47-50	$P6_0$-$P6_3$	4-bit I/O port 6
1, 2, 4, 6, 12-15, 19, 20, 25-28, 32, 35, 37-40, 46, 51, 52	NC	No connection

Pin Functions

$P0_0$/INT0, $P0_3$/X1 [Port 0]

2-bit input port 0. Line $P0_0$ is shared with external interrupt INT0. Line $P0_3$ is shared with crystal clock/external event input X1. Ground any unused pins.

$P1_0$-$P1_3$ [Port 1]

4-bit input port or three-state output port. Output is strobed in synchronization with the $\overline{PSTB}$ pulse. Connect unused pins to V_{SS} or V_{DD}.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2, Strobe, Timer F/F Output]

4-bit latched, three-state output port. Line $P2_0$ is shared with the port 1 output strobe pulse $\overline{PSTB}$. Line $P2_1$ is shared with the timer out flip flop signal PTOUT. Leave unused pins open.

$P4_3$-$P4_0$ [Port 4]

4-bit input or latched three-state output port. Can perform 8-bit parallel I/O in conjunction with port 5. In input mode, connect unused pins to V_{DD} or V_{SS}. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [Port 5]

4-bit input or latched three-state output port. Can perform 8-bit parallel I/O in conjunction with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [Port 6]

4-bit input or latched three-state output port. The port 6 mode select register (MSR) configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

CL1, CL2 [System Clock Input]

Connect a 120-kΩ resistor across CL1 and CL2, and a 33-pF capacitor from CL1 to V_{SS}. Or, connect an external clock source to CL1 and leave CL2 open.

X2, X1 [Crystal Clock/External Event Input]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, connect external event pulses to input X1 and leave X2 open. If X1 is not used, connect it to V_{SS}. If X2 is not used, leave it open.

RESET

A high level input to this pin initializes the μPD7506.

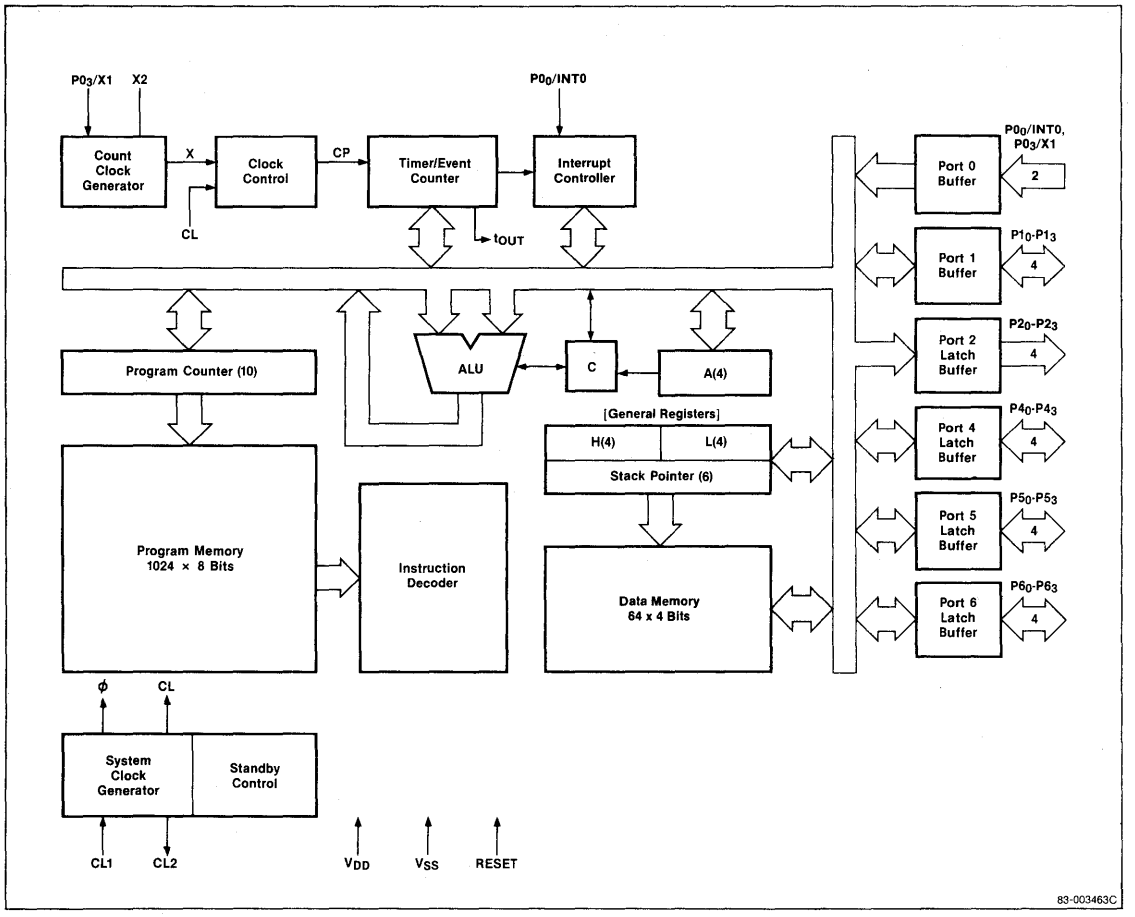
V_{DD}

Positive power supply. For proper operation, apply a single voltage from 2.7 to 6.0 V.

V_{SS}

Ground.

Block Diagram



Clock Control Circuit

This circuit consists of a 4-bit clock mode register (CMR), prescalers 1 and 2, and a multiplexer, as shown in figure 1. The circuit selects the clock source, accepts output from the system clock oscillator (CL) and count clock generator circuit (X), divides the signal according to the setting in the CMR, and outputs the count pulse (CP) to the timer/event counter.

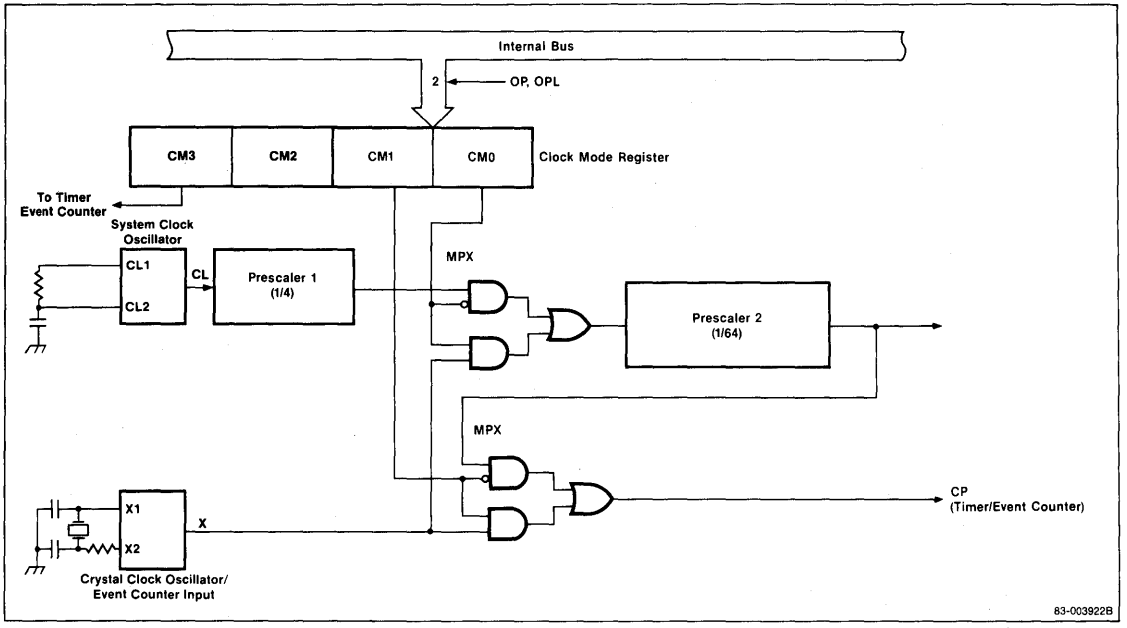
The OP or OPL instruction sets the CMR as defined by table 1. Before loading the CMR, it is necessary to clear bit 2 of the accumulator (A2) to zero.

Table 1. Selecting the Count Pulse Frequency

CM_1	CM_0	Frequency Selected
0	0	CL/256
0	1	X/64
1	0	X
1	1	X

CM_3	TOUT Signal
0	Disabled
1	Enabled

Figure 1. Clock Control Circuit



Timer/Event Counter

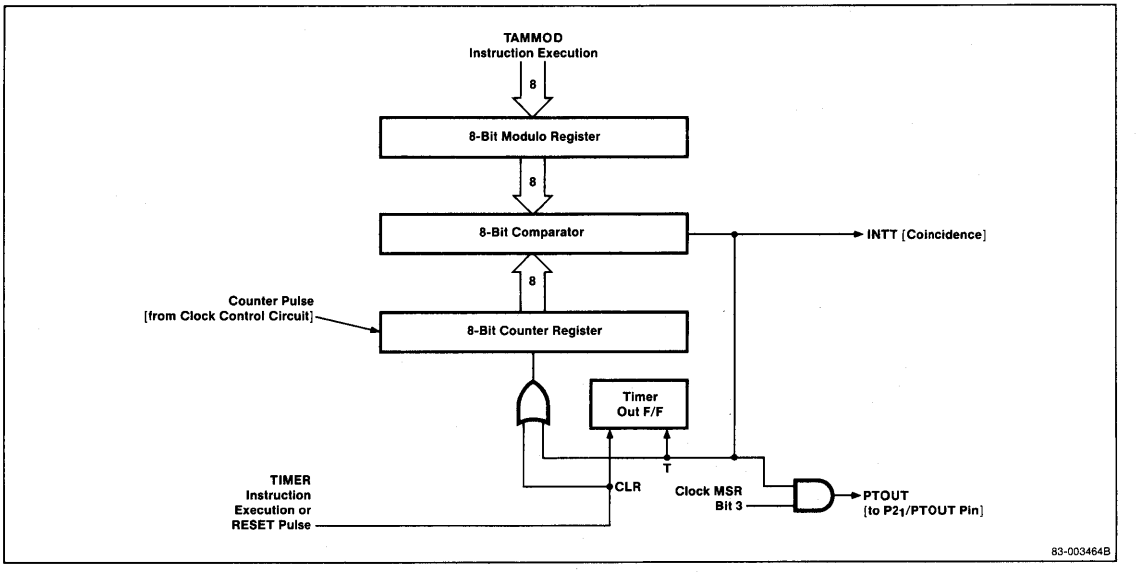
The timer/event counter consists of an 8-bit count register, an 8-bit modulo register, an 8-bit comparator, and a timer out flip flop, as shown in figure 2.

The count register is a binary up-counter that increments each time a count pulse is input. The TIMER instruction, a RESET signal, or an INTT coincidence signal clears it to 00H. When an overflow occurs, the counter is reset from FFH to 00H.

The modulo register determines the number in the count register. The TAMMOD instruction sets the contents of the modulo register. On reset, its contents are FFH.

The comparator compares the contents of the count register and the modulo register; when equal, the comparator outputs INTT.

Figure 2. Timer/Event Counter



Interrupts

The μPD7506 has two interrupts, INTT and INT0. INTT is internally generated by the timer/event counter. INT0 is externally generated. See figure 3.

System Clock and Timing Circuitry

Timing for the μPD7506 is internally generated except for a frequency reference, which can be an RC circuit or an external clock source. Connect the frequency reference to the on-chip oscillator for the feedback phase-shift required for oscillation. Figure 4 shows the connection for an RC circuit. Figure 5 shows the connection for an external clock source.

Table 2 compares stop and halt modes. The main difference is that stop mode stops the system clock; halt does not.

Table 2. Stop and Halt Modes

Mode	CL	ϕ	X	CPU	Timer
Stop	x	x	0	x	Δ
Halt	0	x	0	x	0

o: operates
x: stops
Δ: external clock source: operates
internal clock source: stops

Figure 3. μPD7506 Interrupts

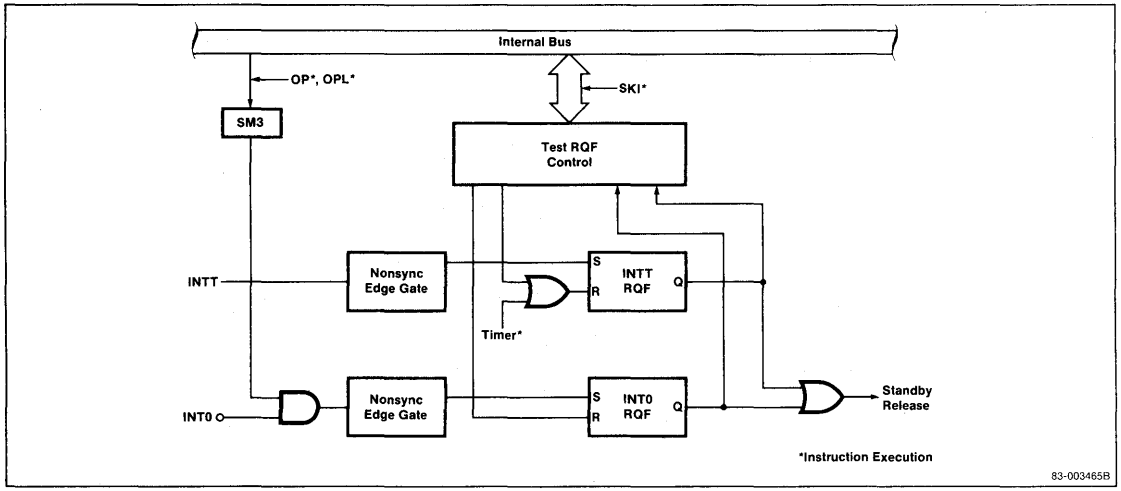


Figure 4. RC Circuit Connection

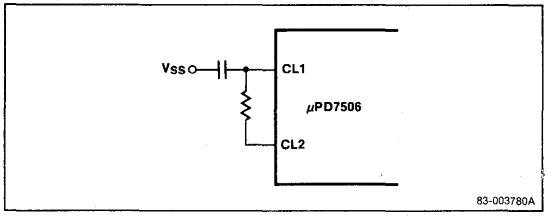
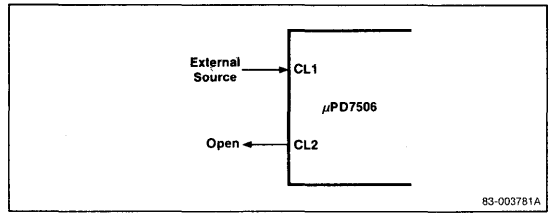


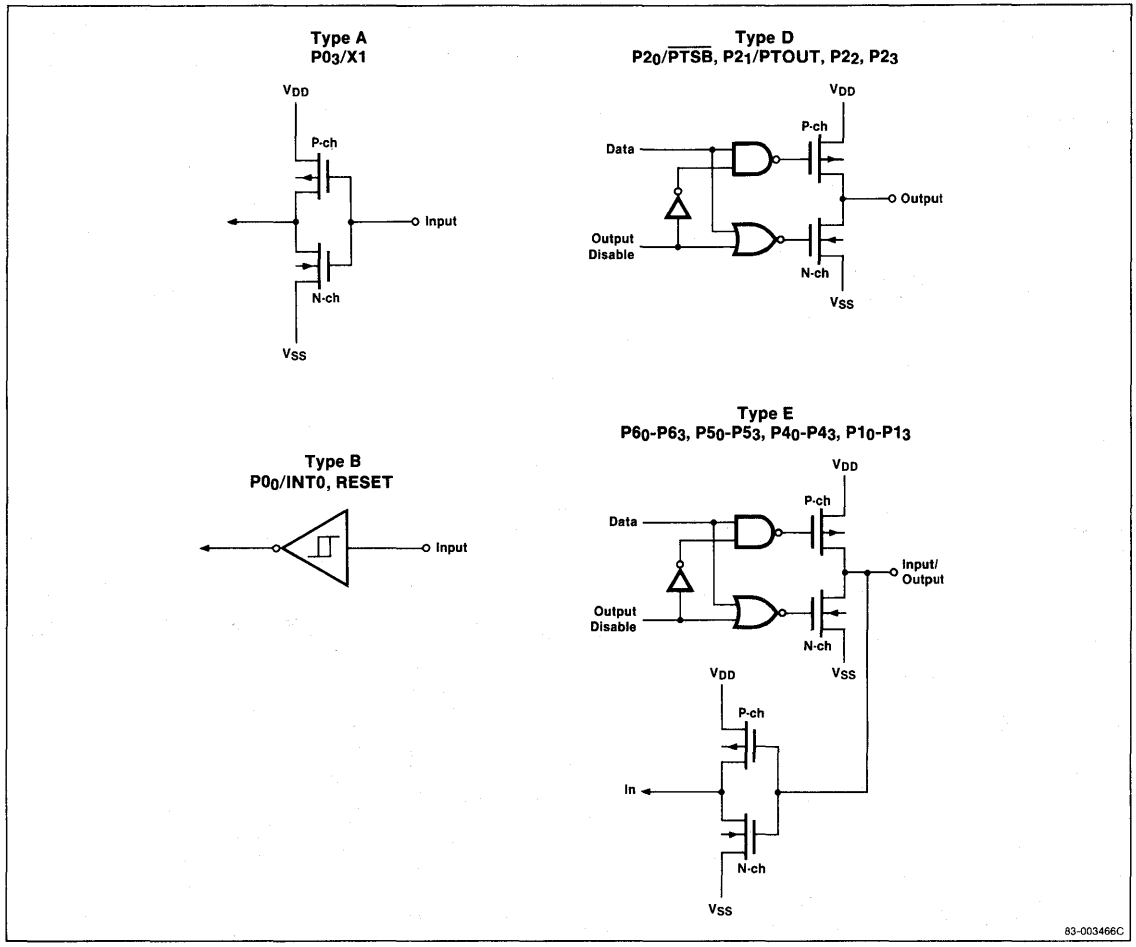
Figure 5. External Clock Source Connection



I/O Pin Configurations

Figure 6 shows the different input and output configurations.

Figure 6. Interface at Input/Output Ports



Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	−10 to 70°C
Storage temperature, T_{STG}	−65 to 150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
Total, input and output voltages	0.3 to V_{DD} + 0.3 V
Output current high, I_{OH}	
Per pin	−17 mA
Ports 2, 6	−17 mA
Ports 1, 4, 5	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Ports 2, 6; $P4_3$	25 mA
Ports 1, 5; $P4_0$-$P4_2$	25 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$; $V_{DD} = 0$ V

Parameter	Symbol	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	$f_c = 1$ MHz Unmeasured pins returned to V_{SS}
Output capacitance	C_O		15	pF	
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

For V_{DD} = 2.7 to 6.0 V

$T_A = -10$ to $+70°C$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.5	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	$I_{OH} = -1.0$ mA; $V_{DD} = 4.5$ to 6.0 V
		V_{DD} − 0.5			V	$I_{OL} = -100$ μA
Output voltage, low	V_{OL}			0.4	V	$I_{OL} = 1.6$ mA; $V_{DD} = 4.5$ to 6.0 V
				0.5	V	$I_{OL} = 400$ μA
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; $V_I = 10$ V
	I_{LIL2}			−10	μA	CL1, X1; $V_I = 10$ V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	$V_O = 0$ V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		200	600	μA	Normal operation, $V_{DD} = 5$ V ±10%; R = 120 kΩ ±2%, C = 33 pF ±5%
			50	180	μA	Normal operation, $V_{DD} = 3$ V ±10%; R = 240 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		1.0	10	μA	Stop mode, X1 = 0 V; $V_{DD} = 5$ V ±10%
			0.3	5	μA	Stop mode, X1 = 0 V; $V_{DD} = 3$ V ±10%
	I_{DDDR}		0.2	5	μA	Data retention mode, $V_{DDDR} = 2.0$ V

DC Characteristics (cont)

For V_{DD} = 2.5 to 3.3 V

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.8 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.3		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.2 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.3	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 0.5			V	I_{OH} = −80 μA
Output voltage, low	V_{OL}			0.5	V	I_{OL} = 350 μA
Input leakage current, high	V_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	V_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
Input leakage current, low	V_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	V_{LIL2}			−10	μA	CL1, X1; V_I = 0 V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		35	150	μA	Normal operation, V_{DD} = 3 V ±10%; R = 390 kΩ ±2%, C = 33 pF ±5%
			25	130	μA	Normal operation, V_{DD} = 2.5 V; R = 390 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		0.3	5	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%
			0.2	5	μA	Stop mode, X1 = 0 V; V_{DD} = 2.5 V
	I_{DDDR}		0.2	5	μA	Data retention mode, V_{DDDR} = 2.0 V

3

AC Characteristics

For V_{DD} = 2.7 to 6.0 V

$T_A = -10$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	V_{DD} = 5 V ±10%; R = 120 kΩ ±2% (Note 1)
		75	100	120	kHz	V_{DD} = 3 V ±10%; R = 240 kΩ ±2% (Note 1)
		75		135	kHz	R = 240 kΩ ±2% (Note 1)
	f_C	10		410	kHz	CL1, external clock, 50% duty; V_{DD} = 4.5 to 6.0 V
		10		125	kHz	CL1, external clock, 50% duty; V_{DD} = 2.7 V
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.2		50	μs	CL1, external clock; V_{DD} = 4.5 to 6.0 V
		4.0		50	μs	CL1, external clock; V_{DD} = 2.7 V
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input, 50% duty; V_{DD} = 4.5 to 6.0 V
		0		125	kHz	X1, external pulse input, 50% duty; V_{DD} = 2.7 V
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.2			μs	X1, external pulse input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	X1, external pulse input; V_{DD} = 2.7 V
Port 1 output set-up time to $\overline{PSTB}$ ↑	t_{PST}	$1/(2f_\phi - 800)$			ns	V_{DD} = 4.5 to 6.0 V
		$1/(2f_{CC} - 2.0)$			ns	
Port 1 output hold time after $\overline{PSTB}$ ↑	t_{STP}	100			ns	V_{DD} = 4.5 to 6.0 V
		100			ns	
$\overline{PSTB}$ pulse width	t_{SWL}	$1/(2f_\phi - 800)$			ns	V_{DD} = 4.5 to 6.0 V
		$1/(2f_{CC} - 2.0)$			ns	
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq 60$ ppm.

AC Characteristics (cont)

For V_{DD} = 2.7 to 3.3 V

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	50		80	kHz	R = 310 kΩ ±2% (Note 1)
		50	64	77	kHz	V_{DD} = 2.5 V; R = 310 kΩ ±2% (Note 1)
	f_C	10		80	kHz	CL1, external clock
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	6.25		50	μs	CL1, external clock
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	6.25			μs	X1, external pulse input
Port 1 output set-up time to PSTB ↑	t_{PST}	$1/(2f_{CC} - 2)$			ns	
Port 1 output hold time after PSTB ↑	t_{STP}	100			ns	
$\overline{PSTB}$ pulse width	t_{SWL}	$1/(2f_{CC} - 2)$			ns	
INT0 pulse width	t_{I0H}, t_{I0L}	30			μs	
RESET pulse width	t_{RSH}, t_{RSL}	30			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq 60$ ppm.

Recommended R and C Values for System Clock Oscillation Circuit

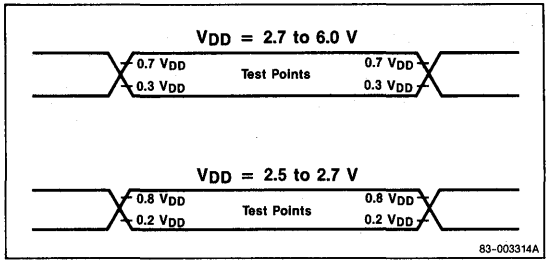
T_A = −10 to +70°C

Supply Voltage Range	Recommended Values	Frequency Range
4.5 to 6.0 V	R = 120 kΩ ±2%	150 to 250 kHz, 200 kHz typical
2.7 to 3.3 V	R = 240 kΩ ±2%	75 to 120 kHz, 100 kHz typical
2.7 to 6.0 V	R = 240 kΩ± 2%	75 to 135 kHz
2.5 to 3.3 V	R = 390 kΩ ±2%	50 to 80 kHz
2.5 to 6.0 V	R = 390 kΩ ±2 %	50 to 85 kHz

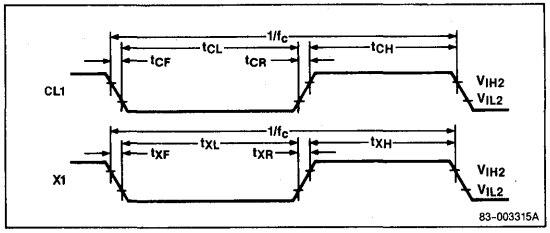
3

Timing Waveforms

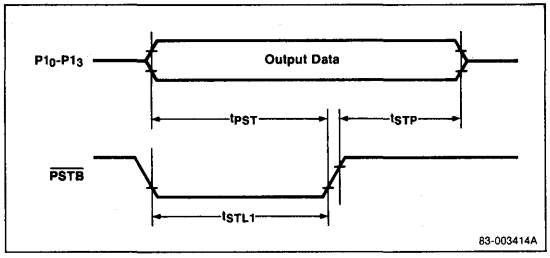
Timing Test Points



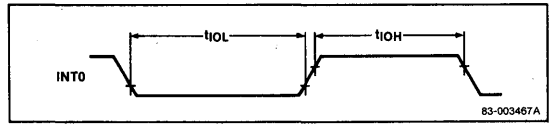
Clocks



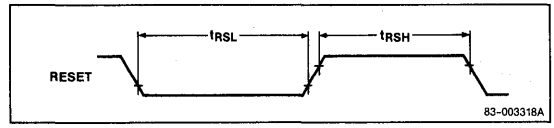
Output Strobe



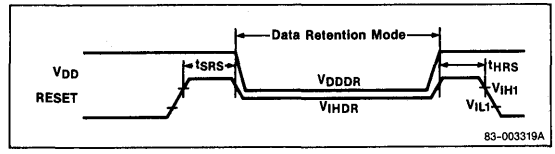
External Interrupt



Reset



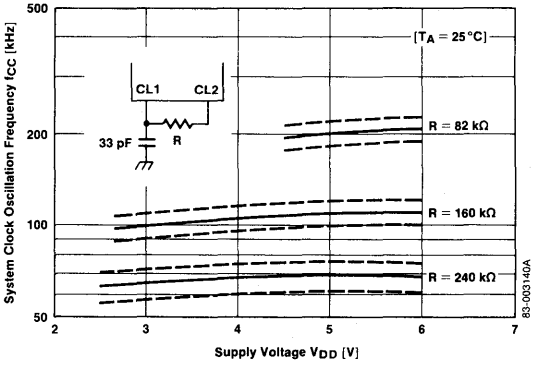
Data Retention Mode



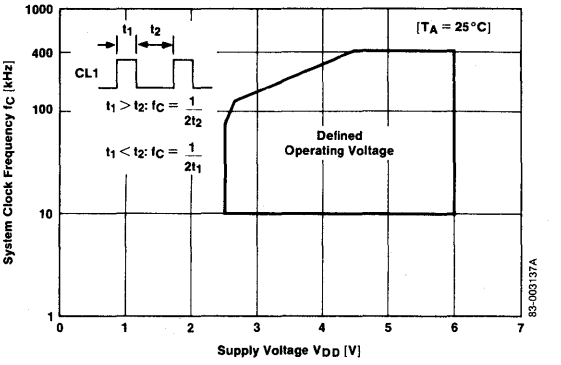
Operating Characteristics

$T_A = 25°C$

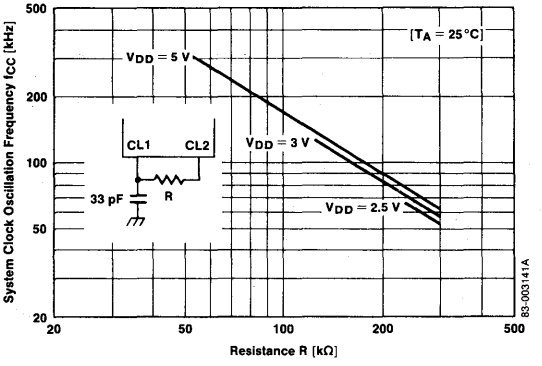
f_{CC} vs V_{DD}



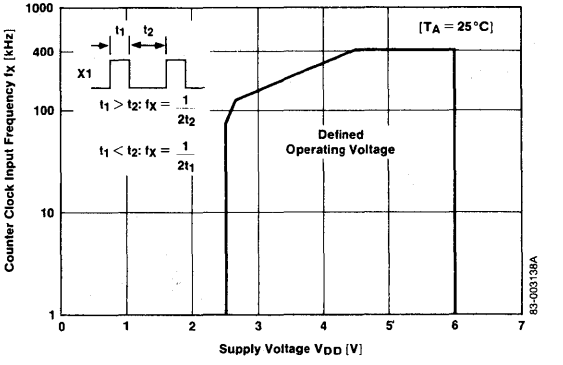
f_C vs V_{DD}



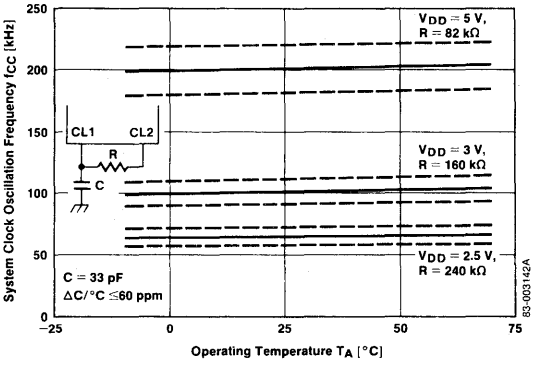
f_{CC} vs R



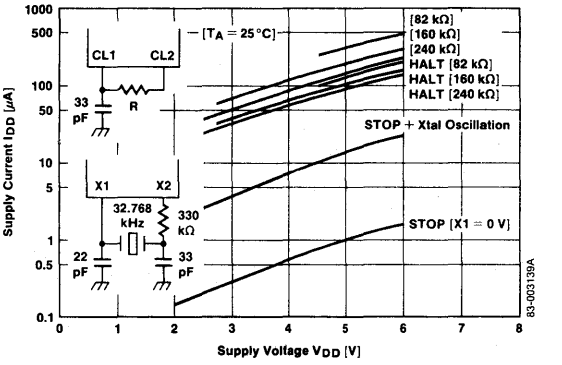
f_X vs V_{DD}



f_{CC} vs T_A

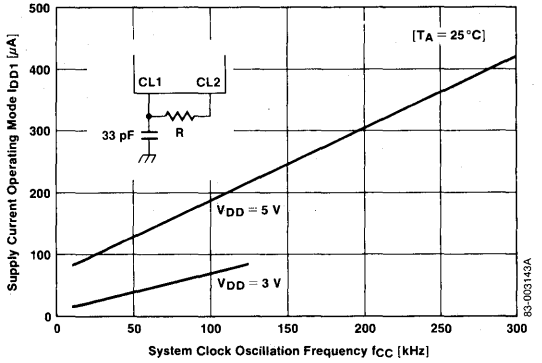


I_{DD} vs V_{DD}

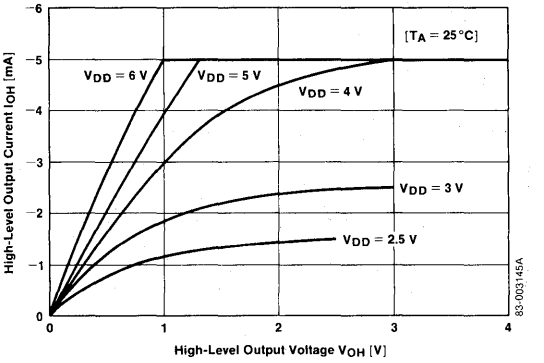


Operating Characteristics (cont)

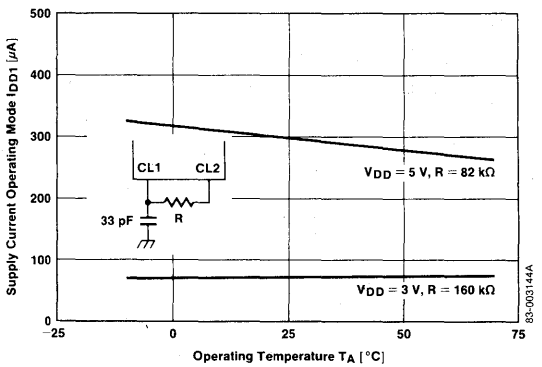
I_{DD1} vs f_{CC}



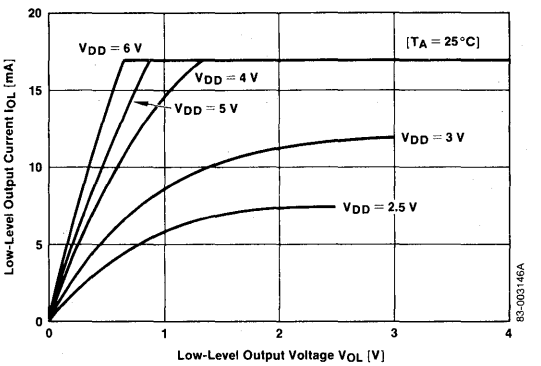
I_{OH} vs V_{OH}



I_{DD1} vs T_A



I_{OL} vs V_{OL}



μPD7507/08
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

Description

The μPD7507 and μPD7508 4-bit, single-chip CMOS microcomputers have the μPD7500 series architecture. The subroutine stack is implemented in RAM for greater nesting depth and flexibility.

Thirty-two I/O lines are organized into eight 4-bit ports: input port/serial interface port 0, output ports 2 and 3, and I/O ports 1, 4, 5, 6, and 7.

The μPD7507 and μPD7508 execute 92 instructions of the μPD7500 series A instruction set with a 5-μs instruction cycle time.

Maximum power consumption is 900 μA at 5 V, less in the HALT and STOP low-power modes.

The μPD75CG08 is a piggyback EPROM prototyping chip that is pin-compatible with μPD7507 and μPD7508. A 2716 inserted into the top of the μPD75CG08 emulates the μPD7507's ROM. A 2732 emulates the μPD7508's ROM. When emulating the μPD7507, the user must take care to use only the first 128 RAM locations. Although the μPD7507 and μPD7508 can operate over a range of 2.5 to 5.5 V, μPD75CG08 operation is limited to 5 V ±10%.

Table 1 summarizes the differences among μPD7507, μPD7508 and μPD75CG08.

Table 1. Features Comparison

	μPD75CG08	μPD7507/7508
Program memory	2K x 8 EPROM (2716) 4K x 8 EPROM (2732)	2K x 8 masked ROM (7507) 4K x 8 masked ROM (7508)
Data memory	224 x 4	128 x 4 (7507) 224 x 4 (7508)
Data retention mode	No	Yes
Power supply	5 V ±10%	2.7 to 6.0 V
Package types	40-pin ceramic piggyback DIP	40-pin plastic DIP 40-pin plastic shrink DIP 52-pin plastic miniflat

Features

- ☐ Single chip microcomputer
- ☐ Program ROM
  - — μPD7507: 2048 x 8-bit
  - — μPD7508: 4096 x 8-bit
  - — μPD75CG08: piggyback EPROM
- ☐ Data RAM
  - — μPD7507: 128 x 4-bit
  - — μPD7508: 224 x 4-bit
  - — μPD75CG08: 224 x 4-bit
- ☐ 8-bit timer/event counter
- ☐ Four 4-bit general purpose registers
- ☐ Four vectored, prioritized interrupts
- ☐ Executes 92 instructions of μPD7500 series A instruction set
- ☐ 5 μs instruction cycle/400 kHz external clock
- ☐ Two standby modes
- ☐ 32 I/O lines
- ☐ Low-power HALT and STOP modes

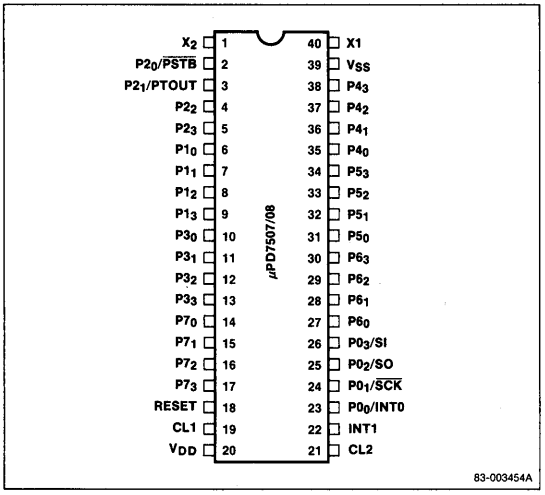
Ordering Information

*Part Number	Package Type	Max Frequency of Operation
μPD7507C	40-pin plastic DIP	410 kHz
μPD7507CU	40-pin plastic shrink DIP	410 kHz
μPD7507G-00	52-pin plastic miniflat	410 kHz
μPD7508C	40-pin plastic DIP	410 kHz
μPD7508CU	40-pin plastic shrink DIP	410 kHz
μPD7508G-00	52-pin plastic miniflat	410 kHz
μPD75CG08E	40-pin ceramic piggyback DIP	410 kHz

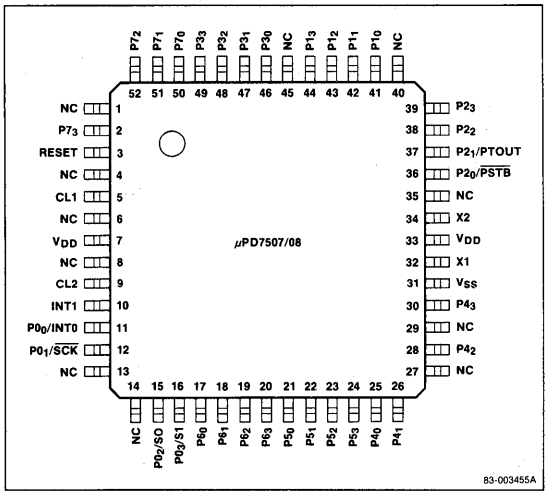
* A 3-digit mask identification code is added to the part number by NEC at the time of code verification.

Pin Configurations

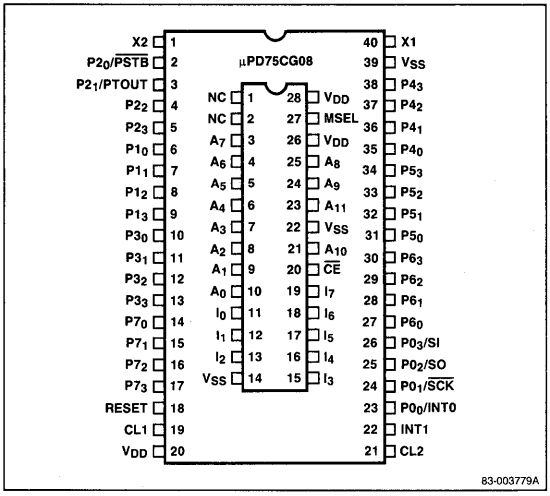
40-Pin Plastic DIP and Plastic Shrink DIP



52-Pin Plastic Miniflat



40-Pin Ceramic Piggyback DIP



Pin Identification

40-Pin DIP, Shrink DIP and Piggyback DIP

No.	Symbol	Function
1, 40	X2, X1	Crystal clock/external event input port
2-5	$P2_0/\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$	Output port 2/output strobe pulse, timer out F/F signal
6-9	$P1_0$-$P1_3$	I/O port 1
10-13	$P3_0$-$P3_3$	Output port 3
14-17	$P7_0$-$P7_3$	I/O port 7
18	RESET	RESET input
19, 21	CL1, CL2	System clock inputs
20	V_{DD}	Positive power supply
22	INT1	External interrupt
23-26	$P0_0$/INT0, $P0_1/\overline{SCK}$, $P0_2$/SO, $P0_3$/SI	Input port 0/external interrupt, serial I/O interface
27-30	$P6_0$-$P6_3$	I/O port 6
31-34	$P5_0$-$P5_3$	I/O port 5
35-38	$P4_3$-$P4_0$	I/O port 4
39	V_{SS}	Ground

Pin Identification (cont)

28-Pin EPROM Socket on Piggyback DIP

No.	Symbol	Function
1, 2	NC	Not connected
3-10	A_7-A_0	Address bits 7-0
11-13	I_0-I_2	Data bits 0-2
14, 22	V_{SS}	Ground
15-19	I_3-I_7	Data bits 3-7
20	$\overline{CE}$	Chip Enable
21, 23	A_{10}-A_{11}	Address bits 10, 11
24, 25	A_9, A_8	Address bits 9, 8
26, 28	V_{DD}	Positive power supply
27	MSEL	Memory select

52-Pin Miniflat

No.	Symbol	Function
1, 4, 6, 13, 14, 27, 29, 35, 40, 45	NC	Not connected
2, 50-52	$P7_0$-$P7_3$	I/O port 7
3	RESET	RESET input
5, 9	CL1, CL2	System clock inputs
7	V_{DD}	Positive power supply
10	INT1	External interrupt
11, 12, 15, 16	$P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI	Input port 0/external interrupt, serial I/O interface
17-20	$P6_0$-$P6_3$	I/O port 6
21-24	$P5_0$-$P5_3$	I/O port 5
25, 26 28, 30	$P4_3$-$P4_0$	I/O port 4
31	V_{SS}	Ground
32, 34	X1, X2	Crystal clock/external event input
33	V_{DD}	Positive power supply
36-39	$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$	4-bit output port 2/output strobe pulse, timer out F/F signal
41-44	$P1_0$-$P1_3$	I/O port 1
46-49	$P3_0$-$P3_3$	Output port 3

Pin Functions

$P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI [Port 0/ External Interrupt, Serial Interface]

4-bit input port/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO (active low), and the serial clock $\overline{SCK}$ (active low), used for synchronizing data transfer, make up the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT0, a rising edge-triggered interrupt. If $P0_0$/INT0 is unused, it should be connected to V_{SS}. If $P0_1$/$\overline{SCK}$, $P0_2$/SO, or $P0_3$/SI are unused, connect them to V_{SS} or V_{DD}.

$P1_0$-$P1_3$ [Port 1]

4-bit input/three-state output port. Data output to port 1 is strobed in synchronization with a $P2_0$/$\overline{PSTB}$ pulse. Connect unused pins to V_{SS} or V_{DD}.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2]

4-bit latched three-state output port. Line $P2_0$ is shared with $\overline{PSTB}$, the port 1 output strobe pulse. Line $P2_1$ is shared with PTOUT, the timer out F/F signal. Leave unused pins open.

$P3_0$-$P3_3$ [Port 3]

4-bit latched three-state output port. Leave unused pins open.

$P4_0$-$P4_3$ [Port 4]

4-bit latched three-state output port. Can also perform 8-bit parallel I/O with port 5. In input mode, connect unused pins to V_{DD} or GND. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [Port 5]

4-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [Port 6]

4-bit input/latched three-state output port. The port 6 mode select register configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P7_0$-$P7_3$ [Port 7]

4-bit input/latched three state output port. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

X2, X1 [Crystal Clock/External Event Input]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, input external event pulses to input X1 while leaving output X2 open. If X1 is not used, leave it open. If X2 is not used, connect it to ground.

CL1, CL2 [System Clock Input]

Connect a 120 kΩ resistor across CL1 and CL2, and connect a 33 pF capacitor from CL1 to V_{SS}. Alternatively, connect an external clock source to CL1 and leave CL2 open. If CL1 is unused, connect it to V_{SS}.

RESET [Reset]

A high level input to this pin initializes the μPD7507/08 after power up.

INT1 [Interrupt 1]

External rising edge-triggered interrupt. Connect to V_{SS} if unused.

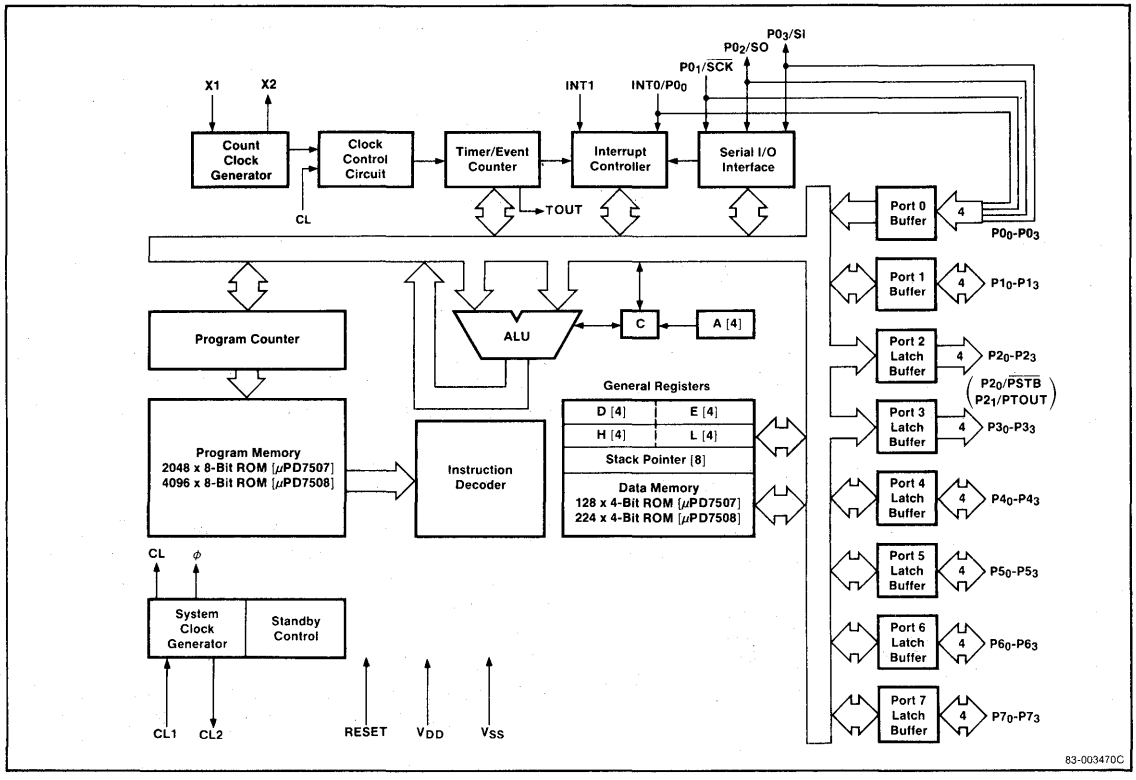
V_{DD} [Power Supply]

Positive power supply. Apply a single voltage in the range 2.7 to 6.0 V for proper operation.

V_{SS} [Ground]

Ground.

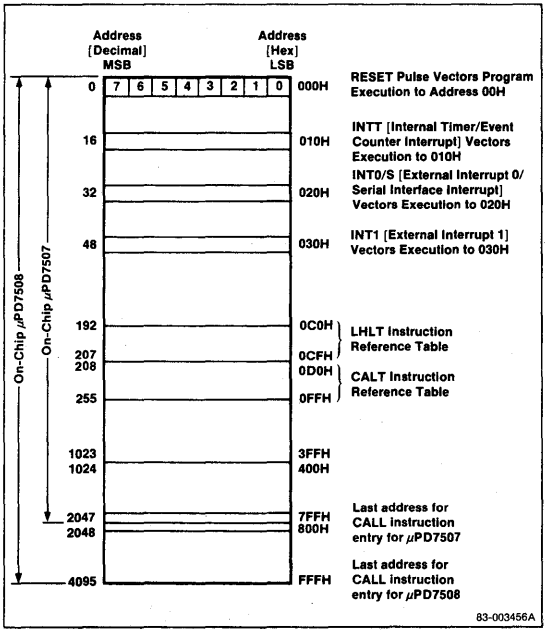
Block Diagram



Memory Map

Figure 1 shows the ROM memory map of the μPD7507/08.

Figure 1. ROM Map



Clock Control Circuit

The clock control circuit consists of a 4-bit clock mode register (bits CM_1 and CM_2), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and count clock generator circuit (I). It also selects the clock source and divides the signal according to the setting in the clock mode register. It outputs the count pulse (CP) to the timer/event counter. Figure 2 shows the clock control circuit.

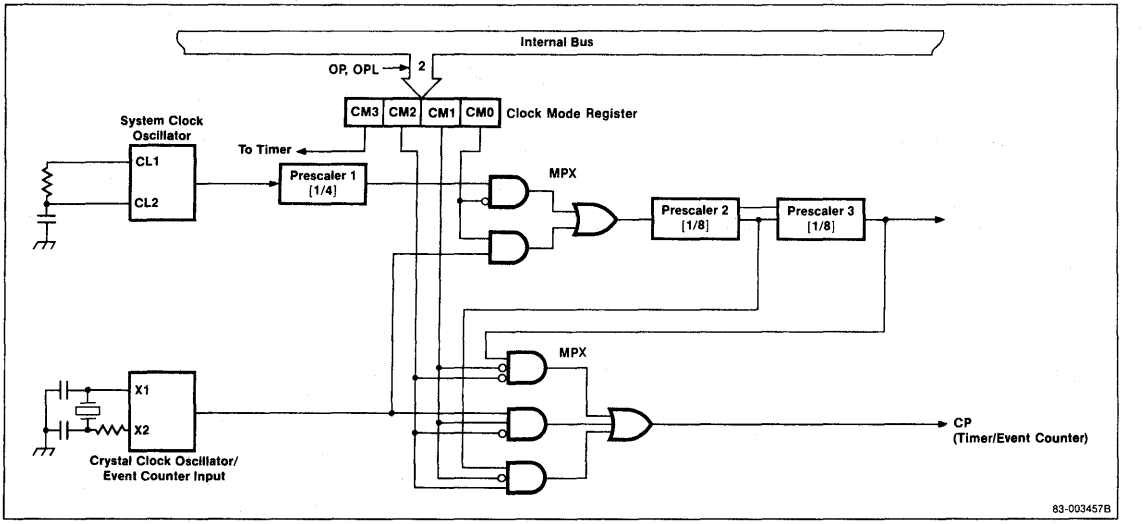
Table 2 lists the codes set in the clock mode register by the OP or OPL instruction to specify the count pulse frequency. Be sure to clear the high-order bits of the accumulator (A_3, A_2) to zero before loading the clock mode register.

Table 2. Selecting the Count Pulse Frequency

CM_2	CM_1	CM_0	Frequency Selected
0	0	0	CL/256
0	0	1	X/64
0	1	0	X
0	1	1	X
1	0	0	CL/32
1	0	1	X/8
1	1	0	Not used
1	1	1	Not used

CM3	TOUT Signal
0	Disabled
1	Enabled

Figure 2. Clock Control Circuit



Timer/Event Counter

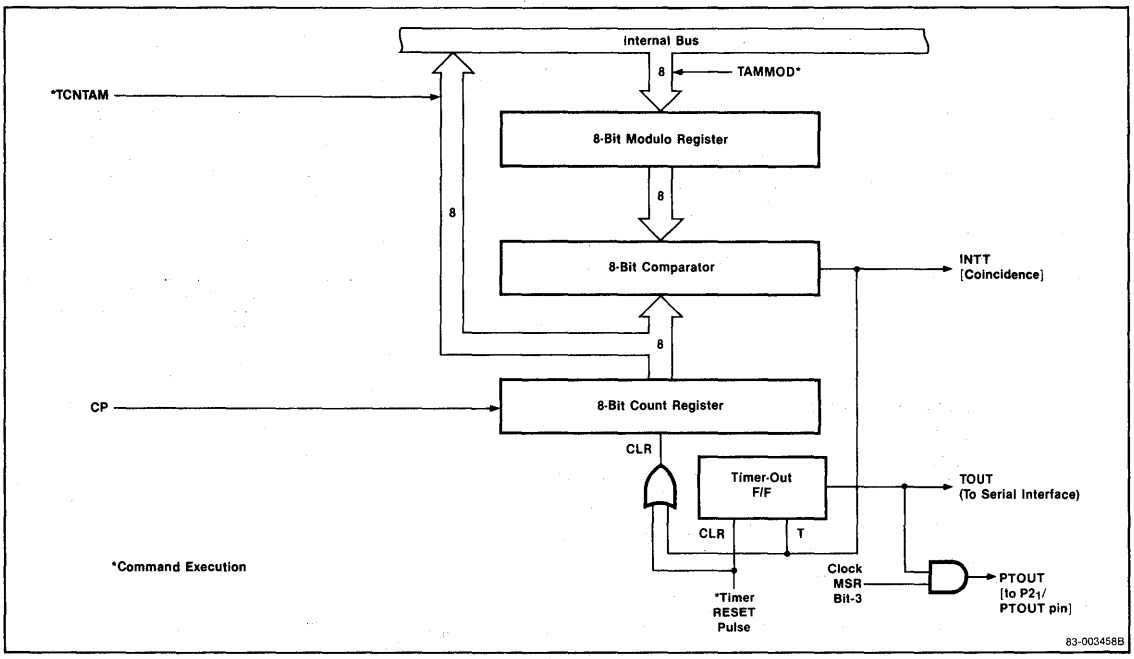
The timer/event counter consists of an 8-bit counter, an 8-bit modulo register, an 8-bit comparator, and a timer out flip-flop as shown in figure 3.

The 8-bit count register is a binary 8-bit up-counter which is incremented each time a count pulse is input. The TIMER instruction, a RESET signal, or an INTT coincidence signal clears it to 00H.

The 8-bit modulo register determines the number of counts the count register holds. The TAMMOD instruction loads the contents of the modulo register. RESET sets the modulo register to FFH.

The 8-bit comparator compares the contents of the count register and the modulo register and outputs an INTT when they are equal.

Figure 3. Timer/Event Counter

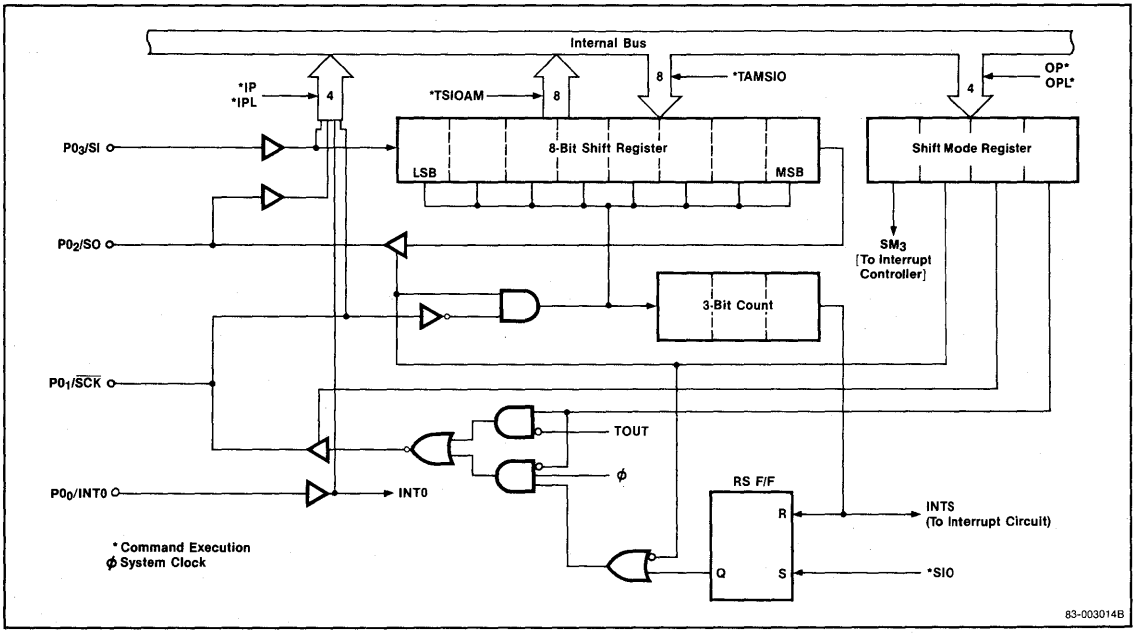


Serial Interface

The 8-bit serial interface allows the μPD7507/08 to communicate with peripheral devices such as the μPD7001 A/D converter, the μPD7227 dot matrix LCD controller/driver, and other microprocessors or microcomputers. Figure 4 shows the serial interface.

The serial interface consists of an 8-bit shift register, a 3-bit $\overline{SCK}$ pulse counter, the SI input port, the SO output port, the $\overline{SCK}$ serial clock I/O port, and a 4-bit serial mode select register (MSR). The MSR selects serial I/O or port 0 operation.

Figure 4. Serial Interface



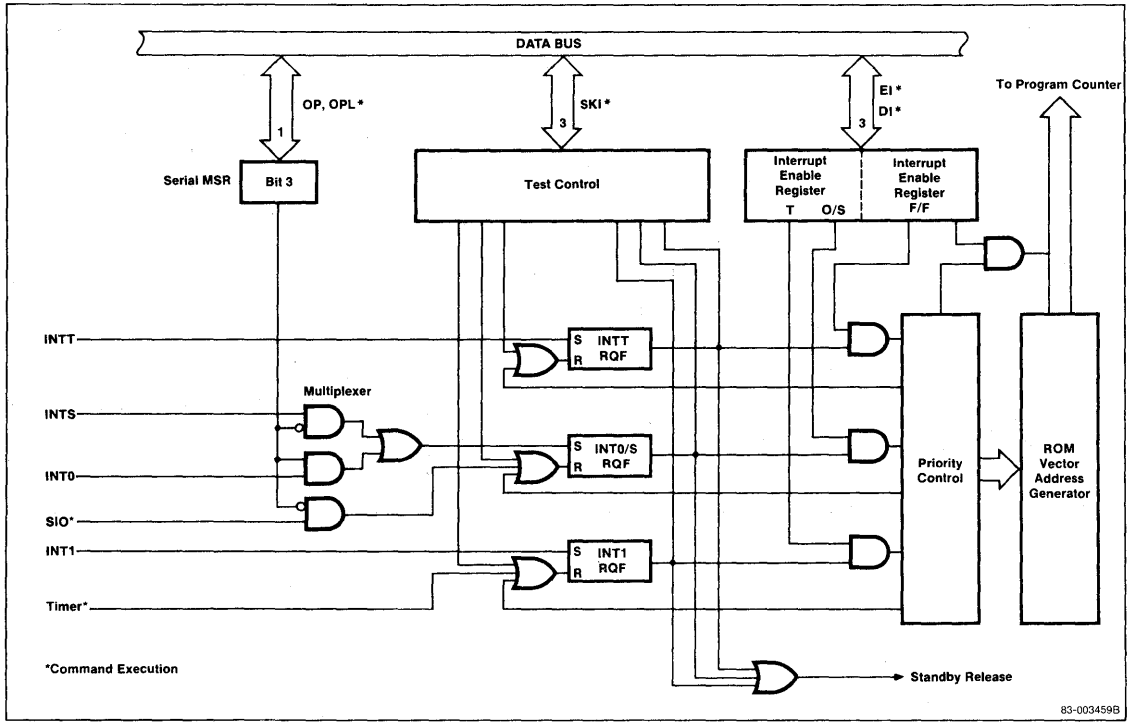
Interrupts

The μPD7507/08 has four vectored, prioritized interrupts. Two of these interrupts, INTT and INTS, are internally generated from the timer/event counter and serial interface, respectively. INT0 and INT1 are externally generated. Table 3 is a summary of the four interrupts. Figure 5 is the block diagram.

Table 3. μPD7507/08 Interrupts

Source	Function	Location	Priority	ROM Vector Address
INTT	Coincidence in timer/event counter	Internal	1	10H
INTS	Transfer complete signal from serial interface	Internal	2	20H
INT0	INT0 pin	External	2	20H
INT1	INT1 pin	External	3	30H

Figure 5. Interrupt Block Diagram



System Clock and Timing Circuitry

Timing for the μPD7507/08 is internally generated except for a frequency reference, which can be an RC circuit or an external clock source. Connect the frequency reference to the on-chip oscillator for the feedback phase shift required for oscillation. Figure 6 shows the connection for an RC circuit. Figure 7 shows the connection for an external clock source.

The internal oscillator generates a frequency in the range 60 kHz to 300 kHz depending on the frequency reference. For example, at $V_{DD} = 5$ V, an 83-kΩ resistor and a 33-pF capacitor generate a frequency of 200 kHz. The oscillation frequency is fed to the clock control circuit. It is divided by two and the resulting signal is fed to the CPU and serial interface as shown in figure 8.

Table 4 shows the operating status of the various logic blocks under the three power down-modes.

Figure 6. RC Circuit Connection

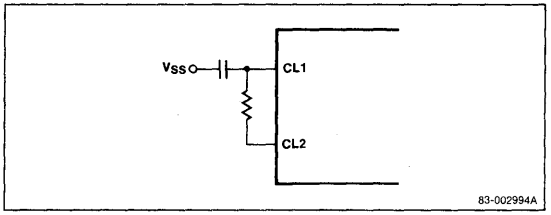


Figure 7. External Clock Source Connection

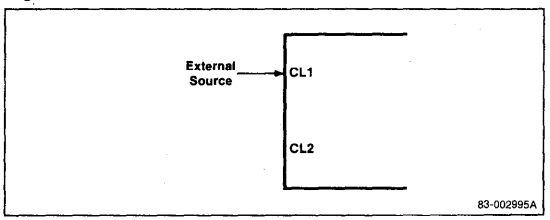


Figure 8. System Clock Circuitry

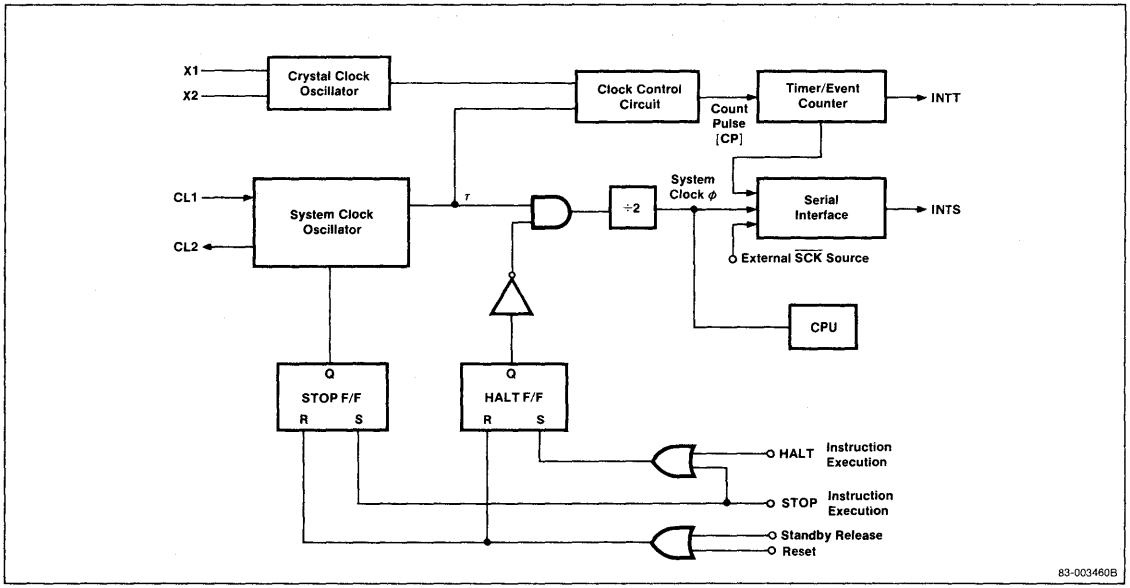


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Table 4. Power-Down Operating Status

	Power-Down Mode		
Logic Block	**HALT**	**STOP**	**Data Retention Mode**
System clock	(Note 1)	Disabled	Disabled
X2	Normal	Normal	Disabled
CPU	Disabled	Disabled	Disabled
RAM	Data retained	Data retained	Data retained
Internal registers	Data retained	Data retained	Data retained
Timer/event counter	Normal	(Note 3)	Disabled
Serial interface	(Note 2)	(Note 2)	Disabled
INT0	Normal	Normal	Disabled
INT1	Normal	Disabled	Disabled
RESET	Normal	Normal	(Note 4)

Note:

(1) Supplied to timer/event counter but not to CPU or serial interface.

(2) Can function normally if the serial MSR is set to get the $\overline{SCK}$ signal externally or from the TOUT signal.

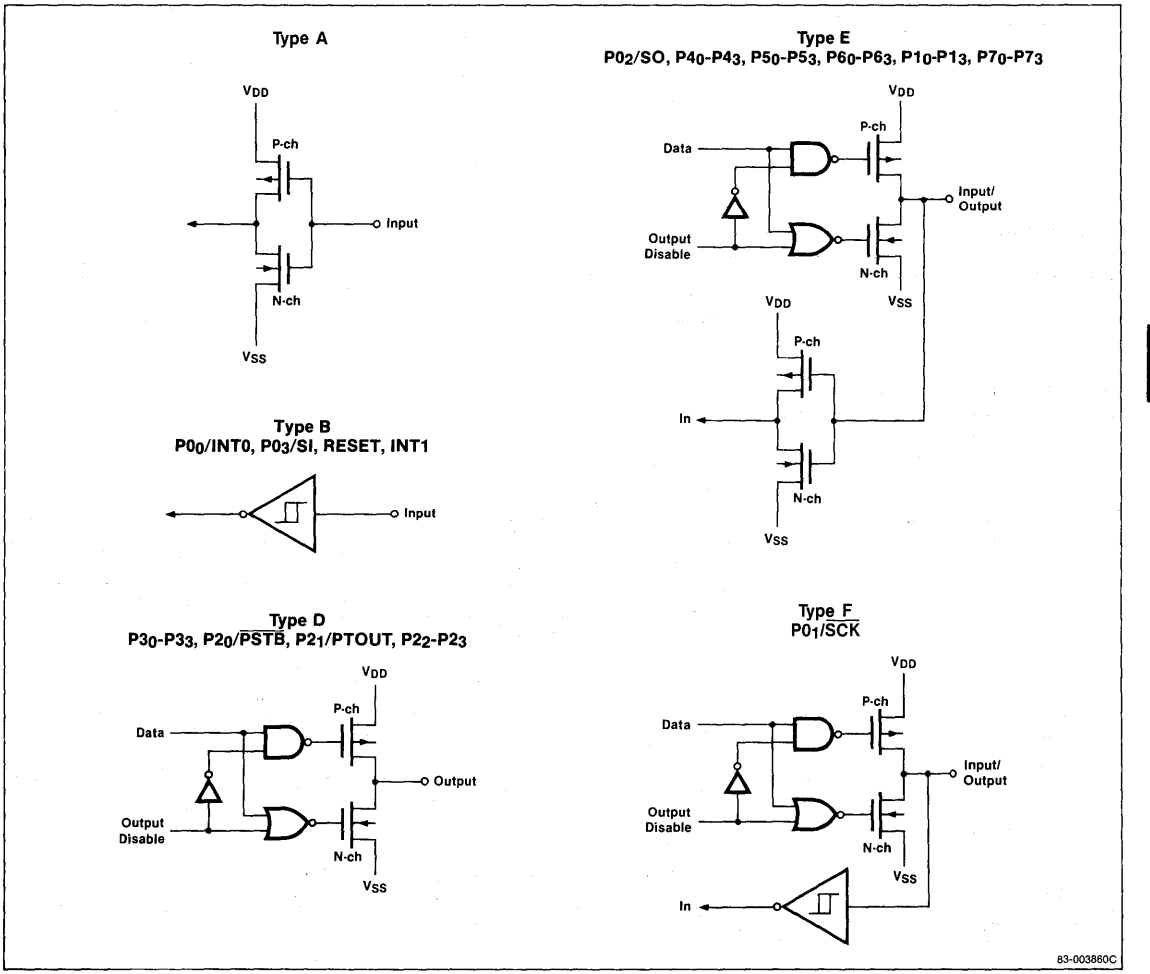
(3) Can function normally if the clock MSR is set to use X1 as the source for the count pulse.

(4) To enter the data retention mode, raise RESET while V_{DD} is lowered. To end the data retention mode, raise RESET when V_{DD} is raised, then lower it. INTT, INT0, INTS or RESET releases the STOP mode. RESET or any interrupt releases the HALT mode.

I/O Port Interfaces

Figure 9 shows the internal circuit configurations at the I/O ports.

Figure 9. Interface at Input/Output Ports



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Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 to V_{DD} + 0.3 V
Output current high, I_{OH}	
One pin	−17 mA
All pins, total	−30 mA
Output current low, I_{OL}	
One pin	17 mA
Ports 1, 2, 3, 7	25 mA
Ports 4, 5, 6	25 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

Parameter	Symbol	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	f = 1 MHz; unmeasured pins returned to V_{SS}
Output capacitance	C_O		15	pF	
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

For V_{DD} = 2.5 to 3.3 V (7507, 7508 only)

$T_A = -10$ to +70°C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.8 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.3		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.2 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.3	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 0.5			V	$I_{OH} = -80\ \mu A$
Output voltage, low	V_{OL}			0.5	V	$I_{OL} = 350\ \mu A$
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	V_{LIH2}			10	μA	CL1, X1
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; $V_I = 0$ V
	V_{LIL2}			−10	μA	CL1, X1
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	$V_O = 0$ V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		50	250	μA	Normal operation, V_{DD} = 3 V ±10%; R = 240 kΩ ±2%, C = 33 pF ±5%
			35	230	μA	Normal operation, V_{DD} = 2.5 V; R = 240 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		0.3	10	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%
			0.2	10	μA	Stop mode, X1 = 0 V; V_{DD} = 2.5 V
	I_{DDDR}		0.2	10	μA	Data retention mode, V_{DDDR} = 2.0 V

DC Characteristics (cont)

For V_{DD} = 2.7 to 6.0 V (75CGO8, 5 V ±10%)

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.5	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA; V_{DD} = 4.5 to 6.0 V, 7507/08 only
		V_{DD} − 0.5			V	I_{OH} = −100 μA, 7507/08 only
	V_{OH1}	V_{DD} − 1.0			V	I_{OH} = −1.0 mA, 75CG08 only
	V_{OH2}	V_{DD} − 0.75			V	I_{OH} = −5.0 mA, 75CG08 only
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 1.6 mA; V_{DD} = 4.5 to 6.0 V, 7507/08 only
				0.5	V	I_{OL} = 400 μA, 7507/08 only
				0.4	V	I_{OL} = 1.6 mA, 75CG08 only
Input current, high	I_{IH}			300	μA	75CG08 only, $V_I = V_{DD}$, MSEL
Input current, low	I_{IL}			−200	μA	75CG08 only, V_I = 0 V, I_0-I_7
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	I_{LIL2}			−10	μA	CL1, X1
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode, 7507/08 only
Supply current	I_{DD1}		300	900	μA	Normal operation, V_{DD} = 5 V ±10%; R = 82 kΩ ±2%, C = 33 pF ±5%
			70	300	μA	Normal operation, V_{DD} = 3 V ±10%; R = 160 kΩ ±2%, C = 33 pF ±5%, 7507/08 only
	I_{DD2}		1.0	20	μA	Stop mode, X1 = 0 V; V_{DD} = 5 V ±10%
			0.3	10	μA	Stop mode, X1 = 0 V; V_{DD} = 3 V ±10%, 7507/08 only
			2	20	μA	Stop mode, X1 = 0 V; V_{DD} = 5 V ±10%, 75CG08 only
	I_{DDDR}		0.2	10	μA	Data retention mode V_{DDDR} = 2.0 V, 7507/08 only

3

AC Characteristics

For V_{DD} = 2.7 to 6.0 V (75CG08, 5 V ±10%)

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	V_{DD} = 5.0 V ±10%; R = 82 kΩ ±2% (Note 1)
		75	100	120	kHz	V_{DD} = 3.0 ±10%; R = 160 kΩ ±2% (Note 1), 7507/08 only
		75		135	kHz	V_{DD} = 3.0 ±10%; R = 160 kΩ ±2% (Note 1), 7507/08 only
	f_C	10		410	kHz	CL1, external clock, 50% duty; V_{DD} = 4.5 to 6.0 V, 7507/08 only, V_{DD} = 5 V ±5%, 75CG08 only
		10		125	kHz	CL1, external clock, 50% duty; V_{DD} = 2.7 V, 7507/08 only
		10		300	kHz	CL1, external clock, 50% duty; 75CG08 only
System clock rise and fall times	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.2		50	μs	CL1, external clock; V_{DD} = 4.5 to 6.0 V, 7507/08 only
		4.0		50	μs	CL1, external clock; V_{DD} = 2.7 V, 7507/08 only
		1.5		50	μs	CL1, external clock, 75CG08 only
		1.2		50	μs	CL1, external clock; V_{DD} = 5 V ±5%, 75CG08 only
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input; 50% duty; V_{DD} = 4.5 to 6.0 V, 7507/08 only
		0		125	kHz	X1, external pulse input, 50% duty; V_{DD} = 2.7 V, 7507/08 only
		0		300	kHz	X1, external pulse input; 50% duty, 75CG08 only
		0		410	kHz	X1, external pulse input; 50% duty; V_{DD} = 5 V, 75CG08 only
Counter clock rise and fall times	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.2			μs	X1, external pulse input; V_{DD} = 4.5 to 6.0 V, 7507/08 only
		4.0			μs	X1, external pulse input; V_{DD} = 2.7 V, 7507/08 only
		1.5			μs	X1, external pulse input, 75CG08 only
		1.2			μs	X1, external pulse input; V_{DD} = 5 V ±5%, 75CG08 only
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V, 7507/08 only 5 V ±5%, 75CG08 only
		8.0			μs	$\overline{SCK}$ as input, 7507/08 only
		4.9			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V, 7507/08 only 5V ±5%, 75CG08 only
		16.0			μs	$\overline{SCK}$ as output, 7507/08 only
		4.0			μs	$\overline{SCK}$ as input, 75CG08 only
		6.7			μs	$\overline{SCK}$ as output, 75CG08 only
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V, 7507/08 only 5V ±5%, 75CG08 only
		4.0			μs	$\overline{SCK}$ as input

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq$ 60 ppm.

AC Characteristics (cont)

For V_{DD} = 2.7 to 6.0 V (75CG08, 5 V ±10%)

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	2.2			μs	$\overline{SCK}$ as output, V_{DD} = 4.5 to 6.0 V, 7507/08 only 5 V ±10% 75CG08 only
		8.0			μs	$\overline{SCK}$ as output, 7507/08 only
		3.0			μs	$\overline{SCK}$ as output, 75CG08 only
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	300			ns	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	450			ns	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			850	ns	V_{DD} = 4.5 to 6.0 V, 7507/08 only 5 V ±10% 75CG08 only
				1200	ns	7507/08 only
Port 1 output setup time to $\overline{PSTB}$ ↑	t_{PST}	$1/(2f_{CC} - 800)$			ns	V_{DD} = 4.5 to 6.0 V, 7507/08 only 5 V ±10% 75CG08 only
		$1/(2f_{CC} - 2.0)$			ns	7507/08 only
Port 1 output setup time to $\overline{PSTB}$ ↑	t_{STP}	100			ns	V_{DD} = 4.5 to 6.0 V, 7507/08 only 5 V ±10% 75CG08 only
		100			ns	7507/08 only
$\overline{PSTB}$ pulse width	t_{STL}	$1/(2f_{CC} - 800)$			ns	V_{DD} = 4.5 to 6.0 V, 7507/08 only 5 V ±10% 75CG08 only
		$1/(2f_{CC} - 2.0)$			ns	7507/08 only
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	$2/f_{CC}$			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

3

AC Characteristics (cont)

For V_{DD} = 2.5 to 3.3 V (7507, 7508 only)

$T_A = -10$ to $+70°C$

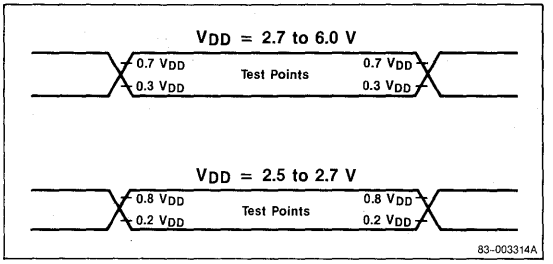
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	50		80	kHz	R = 240 kΩ ±2% (Note 1)
		50	64	77	kHz	V_{DD} = 2.5 V; R = 240 kΩ ±2% (Note 1)
	f_C	10		80	kHz	CL1, external clock, 50% duty
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	6.25		50	μs	CL1, external clock
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	6.25			μs	X1, external pulse input
$\overline{SCK}$ cycle time	t_{KCY}	12.5			μs	$\overline{SCK}$ as input
		25.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	6.25			μs	$\overline{SCK}$ as input
		11.5			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	1			μs	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			2	μs	
Port 1 output setup time to $\overline{PSTB}$ ↑	t_{PST}	$1/(2f_{CC} - 2.0)$			ns	
Port 1 output hold time after $\overline{PSTB}$ ↑	t_{STP}	100			ns	
$\overline{PSTB}$ pulse width	t_{STL}	$1/(2f_{CC} - 2.0)$			ns	
INT0 pulse width	t_{I0H}, t_{I0L}	30			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	$2/f_{CC}$			μs	
RESET pulse width	t_{RSH}, t_{RSL}	30			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

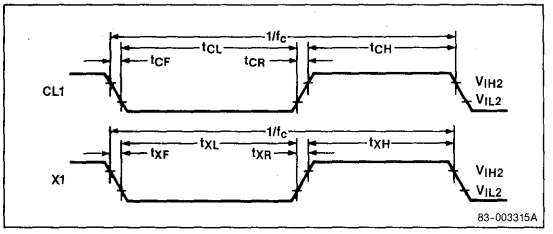
(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq 60$ ppm.

Timing Waveforms

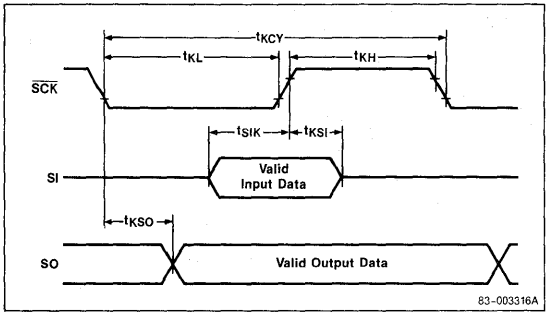
Timing Measurement Points



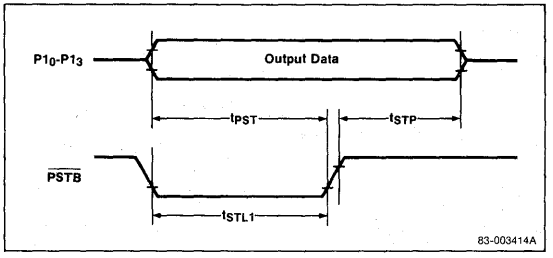
Clocks



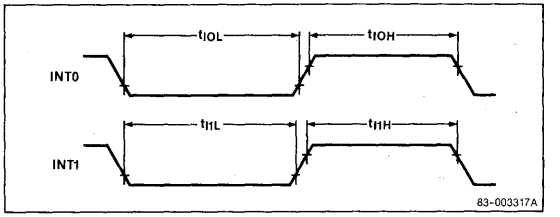
Serial Interface



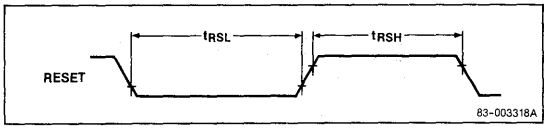
Output Strobe



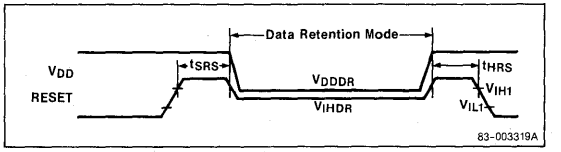
External Interrupts



RESET



Data Retention Mode

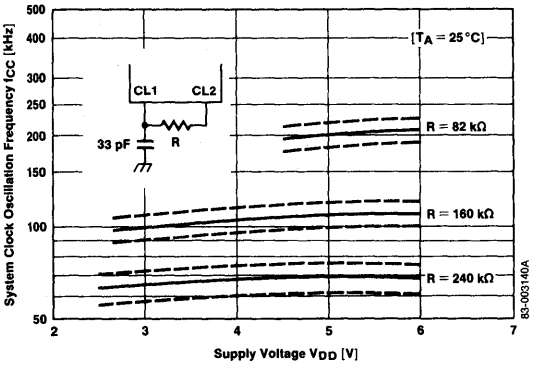


3

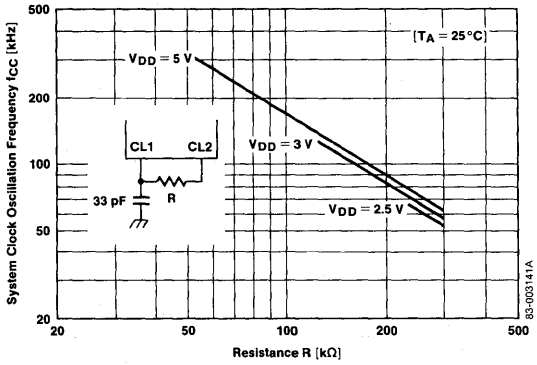
Operating Characteristics

$T_A = 25°C$

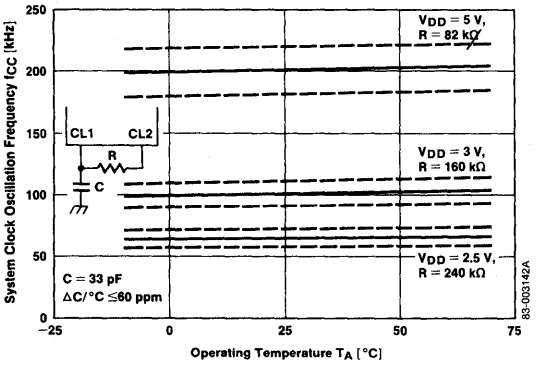
f_{CC} vs V_{DD}



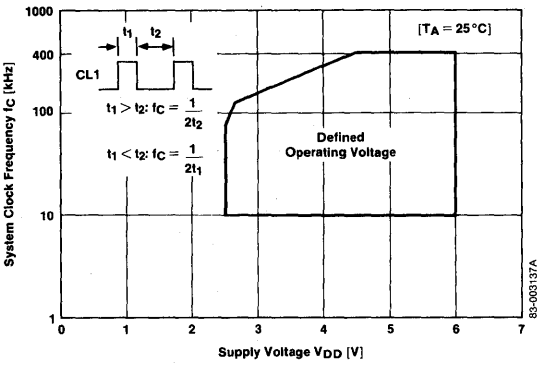
f_{CC} vs R



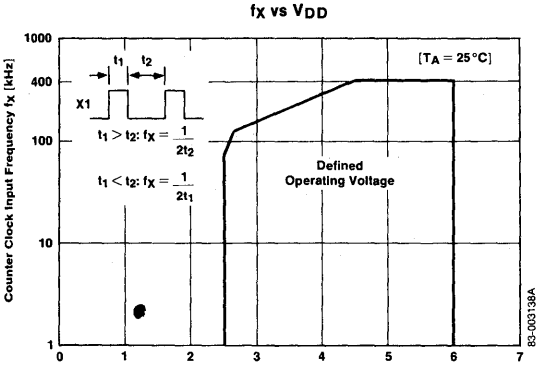
f_{CC} vs T_A



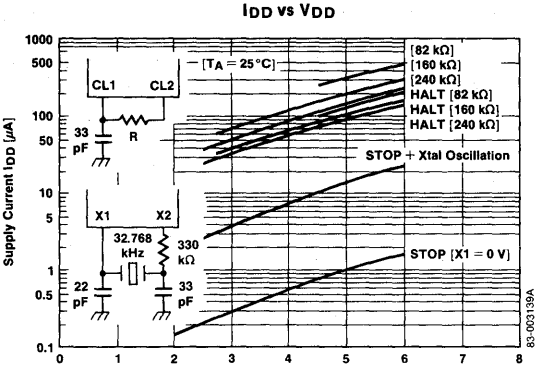
f_C vs V_{DD}



f_X vs V_{DD}



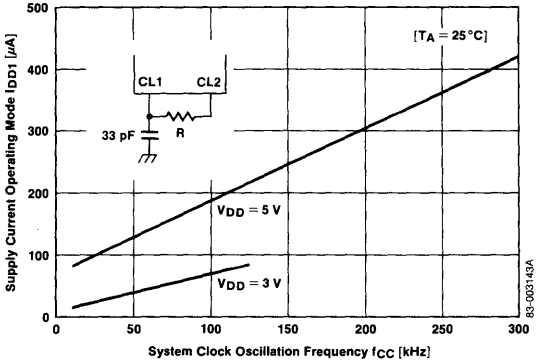
I_{DD} vs V_{DD}



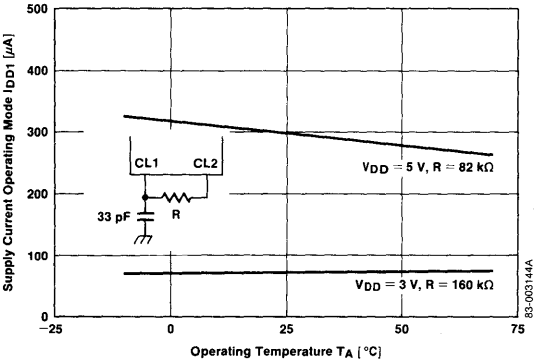
Operating Characteristics (cont)

T_A = 25°C

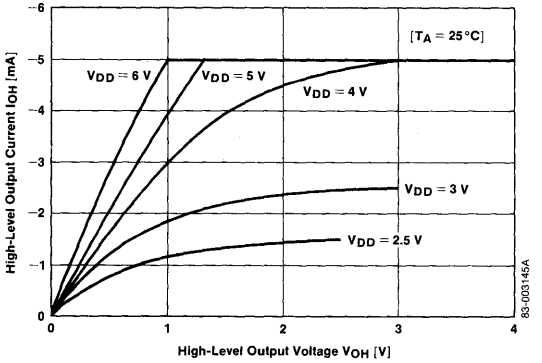
I_{DD1} vs f_{CC}



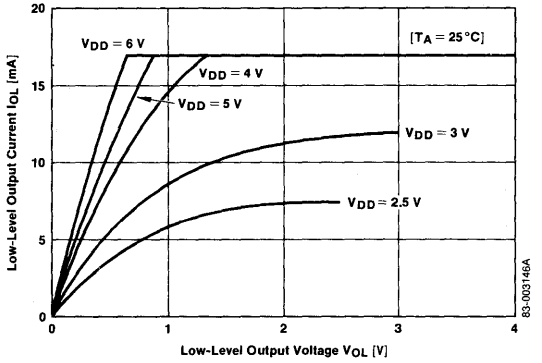
I_{DD1} vs T_A



I_{OH} vs V_{OH}



I_{OL} vs V_{OL}



3

μPD7507H/08H
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

Description

The μPD7507H and μPD7508H are pin-compatible, high-speed (4.19 MHz), 4-bit, single-chip CMOS microcomputers with the μPD7500 series architecture. The subroutine stack is implemented in RAM for greater nesting depth and flexibility.

Thirty-two I/O lines are organized into eight 4-bit ports: input port/serial interface port 0, output ports 2 and 3, and I/O ports 1, 4, 5, 6, and 7.

The μPD7507H and μPD7508H execute 92 instructions of the μPD7500 series A instruction set with a 2.86-μs instruction cycle time.

Maximum power consumption is 800 μA at 5 V and less in the HALT and STOP low-power modes.

The 75CG08H is a piggyback EPROM prototyping chip that is pin-compatible with 7507H and 7508H. A 2716 plugged into the top of the 75CG08H emulates the ROM of a 7507H. A 2732 emulates the ROM of 7508H. When emulating the 7507H, the user must take care to use only the first 128 RAM locations. Although 7507H and 7508H can operate over a range of 2.5 to 6.0 V, 75CG08H is limited to 5 V ±10%. Table 1 summarizes the differences among 7507H, 7508H, and 75CG08H

Features

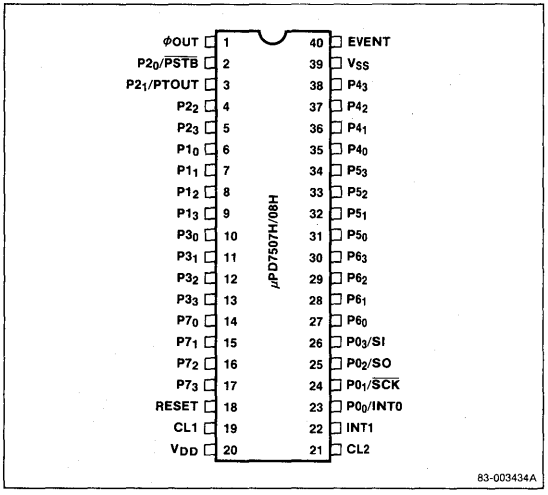
- ☐ Single-chip microcomputer
- ☐ Program ROM
  - — μPD7507H: 2048 x 8-bit
  - — μPD7508H: 4096 x 8-bit
  - — μPD75CG08H: piggyback EPROM
- ☐ Data RAM
  - — μPD7507H: 128 x 4-bit
  - — μPD7508H: 224 x 4-bit
  - — μPD75CG08H: 224 x 4-bit
- ☐ 8-bit timer/event counter
- ☐ Four 4-bit general purpose registers
- ☐ Four vectored, prioritized interrupts
- ☐ Executes 92 instructions of 7500 series A instruction set
- ☐ 2.86-μs instruction cycle/4.19-MHz external clock
- ☐ Two standby modes
- ☐ 32 I/O lines
- ☐ LED direct drive (ports 2-5; 16 lines)
- ☐ Low power HALT and STOP modes

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7507HC	40-pin plastic DIP	4.19 MHz
μPD7507HCU	40-pin plastic shrink DIP	4.19 MHz
μPD7507HG-22	44-pin plastic miniflat	4.19 MHz
μPD7508HC	40-pin plastic DIP	4.19 MHz
μPD7508HCU	40-pin plastic shrink DIP	4.19 MHz
μPD7508HG-22	44-pin plastic miniflat	4.19 MHz
μPD75CG08HE	40-pin ceramic piggyback DIP	4.19 MHz

Pin Configurations

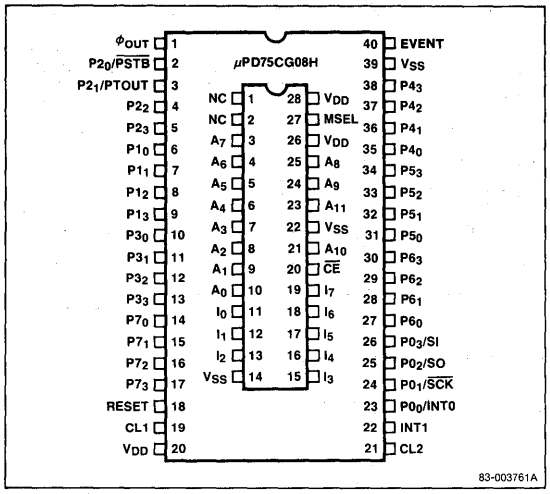
40-Pin Plastic DIP and Plastic Shrink DIP



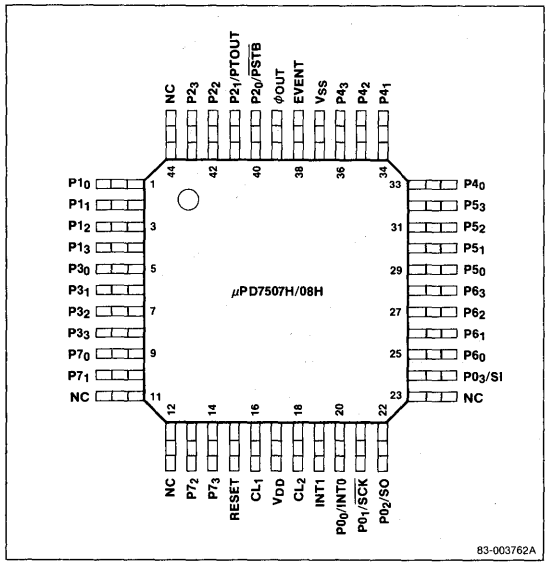
3

Pin Configurations (cont)

40-Pin Ceramic Piggyback DIP



44-Pin Plastic Miniflat



Pin Identification

40-Pin DIP, Shrink DIP, and Piggyback DIP

No.	Symbol	Function
1	ϕOUT	f_{CC}/12 square wave
2-5	$P2_0$/PSTB $P2_1$/PTOUT, $P2_2$, $P2_3$	Output port 2/output strobe pulse, timer out F/F signal
6-9	$P1_0$-$P1_3$	I/O port 1
10-13	$P3_0$-$P3_3$	Output port 3
14-17	$P7_0$-$P7_3$	I/O port 7
18	RESET	RESET input
19, 21	CL1, CL2	System clock inputs
20	V_{DD}	Positive power supply
22	INT1	External interrupt
23-26	$P0_0$/INT0, $P0_1$/SCK, $P0_2$/SO $P0_3$/SI	Input port 0/external interrupt, serial I/O interface
27-30	$P6_0$-$P6_3$	I/O port 6
31-34	$P5_0$-$P5_3$	I/O port 5
35-38	$P4_0$-$P4_3$	I/O port 4
39	V_{SS}	Ground
40	EVENT	External event input port

44-Pin Miniflat

No.	Symbol	Function
1, 4	$P1_0$-$P1_3$	I/O port 1
5-8	$P3_0$-$P3_3$	Port 3 output
9, 10, 13, 14	$P7_0$-$P7_3$	I/O port 7
11-12	NC	Not connected
15	RESET	RESET input
16, 18	CL1, CL2	System clock inputs
17	V_{DD}	Positive power supply
19	INT1	External interrupt 1
20	$P0_0$/INT0	Port 0 input/Interrupt 0
21	$P0_1$/SCK	Port 0 input/Serial clock I/O
22	$P0_2$/SO	Port 0 input/Serial output
23	NC	Not connected
24	$P0_3$/SI	Port 0 input/Serial output
25-28	$P6_0$-$P6_3$	I/O port 6
29-32	$P5_0$-$P5_3$	I/O port 5
33-36	$P4_0$-$P4_3$	I/O port 4

Pin Identification (cont)

44-Pin Miniflat (cont)

No.	Symbol	Function
37	V_{SS}	Ground
38	EVENT	External event input
39	ϕOUT	$f_{CC}/12$ square wave
40	$P2_0/\overline{PSTB}$	Port 2 output/Output strobe pulse
41	$P2_1$/PTOUT	Port 2 output/Timer out F/F signal
42, 43	$P2_2$, $P2_3$	Port 2 output
44	NC	Not connected

28-Pin EPROM Socket on Piggyback DIP

No.	Symbol	Function
1, 2	NC	Not connected
3-10	A_7-A_0	Address bits 7-0
11-13	I_0-I_2	Data bits 0-2
14, 22	V_{SS}	Ground
15-19	I_3-I_7	Data bits 3-7
20	$\overline{CE}$	Chip enable
21, 23	A10, A11	Address bits 10, 11
24, 25	A9, A8	Address bits 9, 8
26, 28	V_{DD}	Positive power supply
27	MSEL	Memory select

Pin Functions

$P0_0$/INT0, $P0_1/\overline{SCK}$, [Port 0/External Interrupt, Serial Interface] $P0_2$/SO, $P0_3$/SI

4-bit input port/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO, and the serial clock $\overline{SCK}$ (active low) used for synchronizing data transfer make up the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT0, a rising edge-triggered interrupt. If $P0_0$/INT0 is unused, it should be connected to V_{SS}. If $P0_1/\overline{SCK}$, $P0_2$/SO, or $P0_2$/SI are unused, connect them to V_{SS} or V_{DD}.

$P1_0$-$P1_3$ [Port 1]

4-bit input/three-state output port. Data output to port 1 is strobed in synchronization with a $P2_0/\overline{PSTB}$ pulse. Connect unused pins to V_{SS} or V_{DD}.

$P2_0/\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2]

4-bit latched three-state output port. Line $P2_0$ is shared with $\overline{PSTB}$, the port 1 output strobe pulse. Line $P2_1$ is shared with PTOUT, the timer out F/F signal. Leave unused pins open.

$P3_0$-$P3_3$ [Port 3]

4-bit latched three-state output port. Leave unused pins open.

$P4_0$-$P4_3$ [Port 4]

4-bit latched three-state output port. Can also perform 8-bit parallel I/O with port 5. In input mode, connect unused pins to V_{DD} or GND. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [Port 5]

4-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [Port 6]

4-bit input/latched three-state output port. The port 6 mode select register configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P7_0$-$P7_3$ [Port 7]

4-bit input/latched three-state output port. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

ϕOUT [Clock Out]

Outputs a square wave with frequency $f_{CC}/12$.

EVENT [External Event Input]

Pulses on this line are counted by the timer/event counter and an interrupt is generated when a predetermined count is reached.

CL1, CL2 [System Clock Input]

The system clock can be generated by connecting a crystal or a ceramic resonator across CL1 and CL2 and capacitors from each side of the crystal to ground. Alternatively a clock signal can be input to CL1 and its invert to CL2. See figure 1.

RESET [Reset]

A high level input to this pin initializes the μPD7507H/08H after power up.

INT1 [Interrupt 1]

External rising edge-triggered interrupt. Connect to V_{SS} if unused.

V_{DD} [Power Supply]

Positive power supply. Apply a single voltage in the range 2.7 to 6.0 V for proper operation.

V_{SS} [Ground]

Ground.

Table 1. Features Comparison

	μPD75CG08H	μPD7507H/7508H
Program memory	2K x 8 EPROM (2716) 4K x 8 EPROM (2732)	2K x 8 masked ROM (7507H) 4K x 8 masked ROM (7508H)
Data memory	224 x 4	128 x 4 (7507H) 224 x 4 (7508H)
Data retention mode	Use more current than 7507H, 7508H	Yes
Power supply	5 V ±10%	2.7 to 6.0 V
Package types	40-pin ceramic piggyback DIP	40-pin plastic DIP 40-pin plastic shrink DIP 44-pin plastic miniflat

Block Diagram

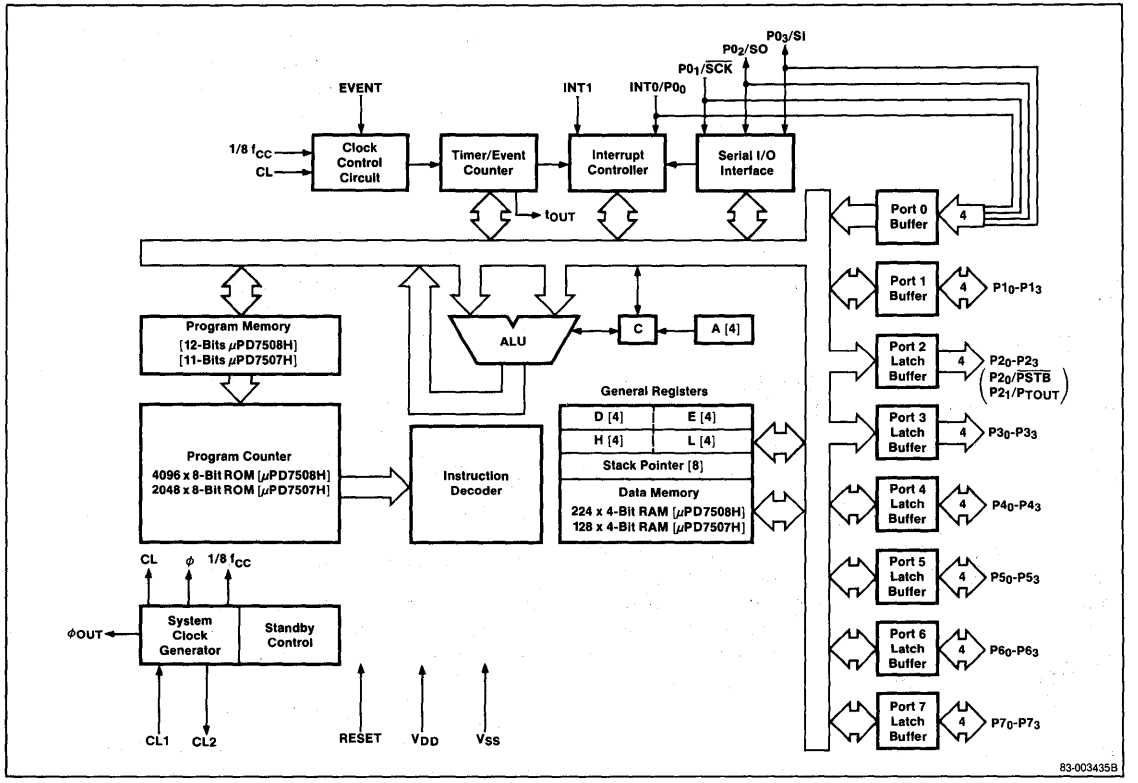
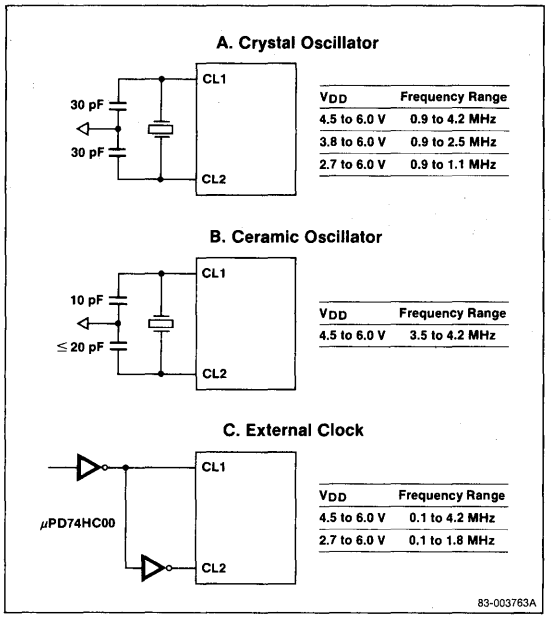


Figure 1. System Clock Options



Memory Map

Figure 2 shows the ROM program map of the 7507H/7508H.

Clock Control Circuit

The clock control circuit consists of a 4-bit clock mode register (bits CM_0-CM_3), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and external EVENT input. It also selects the clock source and divides the signal according to the setting in the clock mode register. It outputs the count pulse (CP) to the timer/event counter. Figure 3 shows the clock control circuit.

Table 2 lists the codes set in the clock mode register by the OP or OPL instruction to specify the count pulse frequency. Bit CM_3 controls the timer out F/F; it is disabled when the bit is 0 and output when the bit is 1.

Table 2. Selecting the Count Pulse Frequency

CM_2	CM_1	CM_0	Frequency Selected
0	0	0	f_{CC}/1536 (CL/256)
0	0	1	f_{CC}/512 (f_{CC}/8 x 1/64)
0	1	0	EVENT input
0	1	1	Not used
1	0	0	f_{CC}/192 (CL/32)
1	0	1	f_{CC}/64 (f_{CC}/8 x 1/8)
1	1	0	Not used
1	1	1	Not used

Figure 2. ROM Map

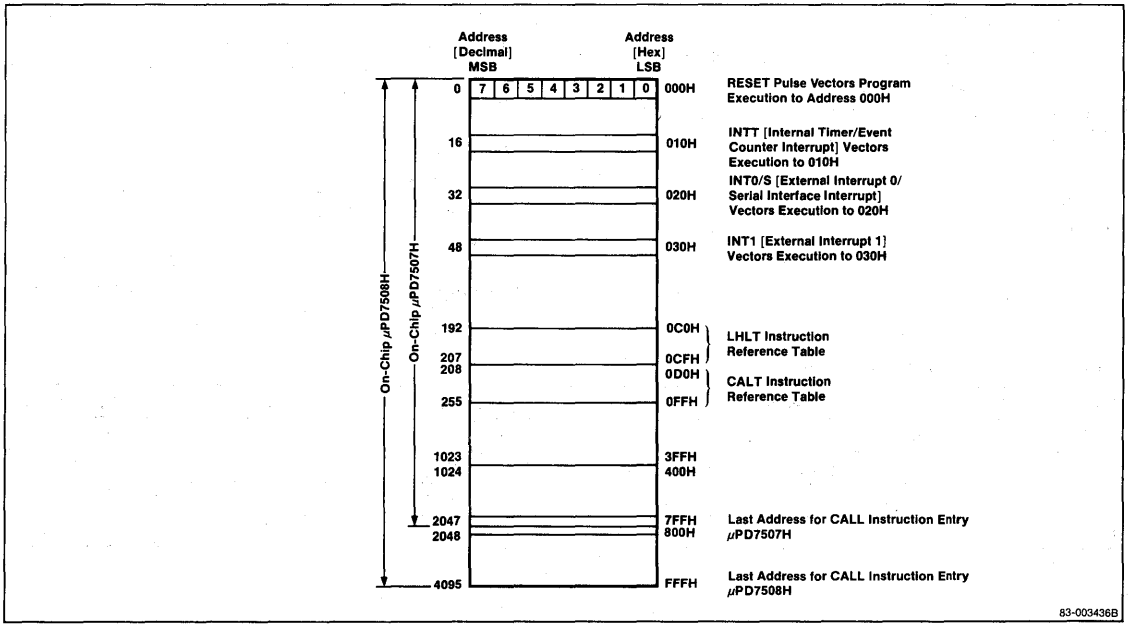
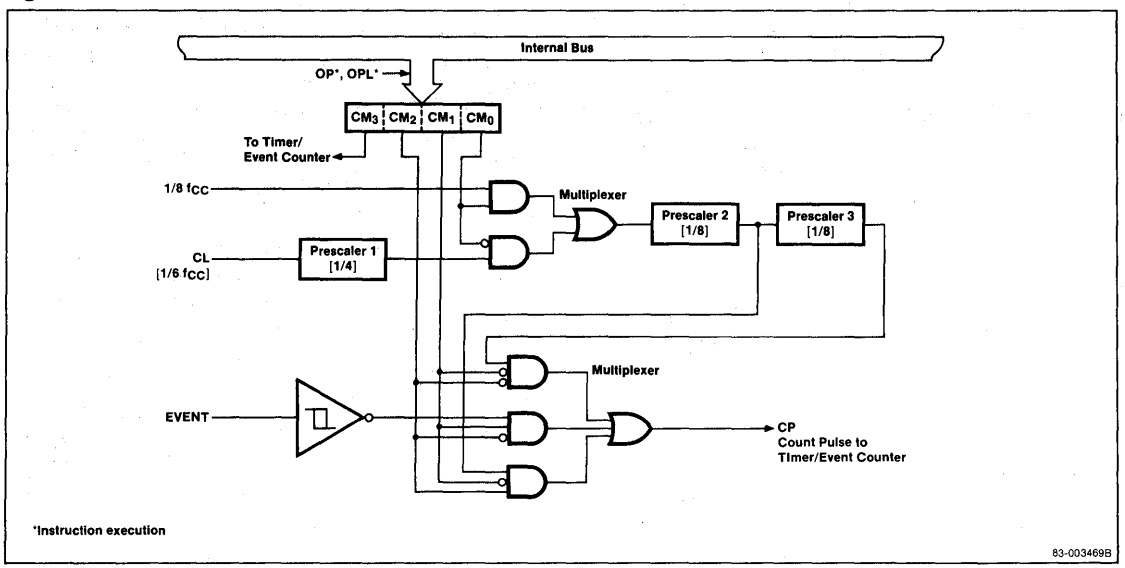


Figure 3. Clock Control Circuit



Timer/Event Counter

The timer/event counter consists of an 8-bit counter, an 8-bit modulo register, an 8-bit comparator, and a timer out flip flop as shown in figure 4.

The 8-bit count register is a binary 8-bit up counter, which is incremented each time a count pulse is input. The TIMER instruction, a RESET signal, or an INTT coincidence signal clears it to 00H.

The 8-bit modulo register determines the number of counts the count register holds. The TAMMOD instruction loads the contents of the modulo register. RESET sets the modulo register to FFH.

The 8-bit comparator compares the contents of the count register and the modulo register and outputs an INTT one clock pulse after they are equal.

Serial Interface

The 8-bit serial interface allows the μPD7507H/08H to communicate with peripheral devices such as the μPD7001 A/D converter, the μPD7227 dot matrix LCD controller/driver, and other microprocessors or microcomputers.

The serial interface consists of an 8-bit shift register, a 3-bit $\overline{SCK}$ pulse counter, the SI input port, the SO output port, the $\overline{SCK}$ serial clock I/O port, and a 4-bit serial mode select register (MSR). The MSR selects serial I/O or port 0 operation.

Interrupts

The μPD7507H/08H has four vectored, prioritized interrupts. Two of these interrupts, INTT and INTS, are internally generated from the timer/event counter and serial interface, respectively. INT0 and INT1 are externally generated. Table 3 is a summary of the four interrupts.

Table 3. μPD7507H/08H Interrupts

Source	Function	Location	Priority	ROM Vector Address
INTT	Coincidence in timer/event counter	Internal	1	10H
INTS	Transfer complete signal from serial interface	Internal	2	20H
INT0	INT0 pin	External	2	20H
INT1	INT1 pin	External	3	30H

Figure 4. Timer/Event Counter

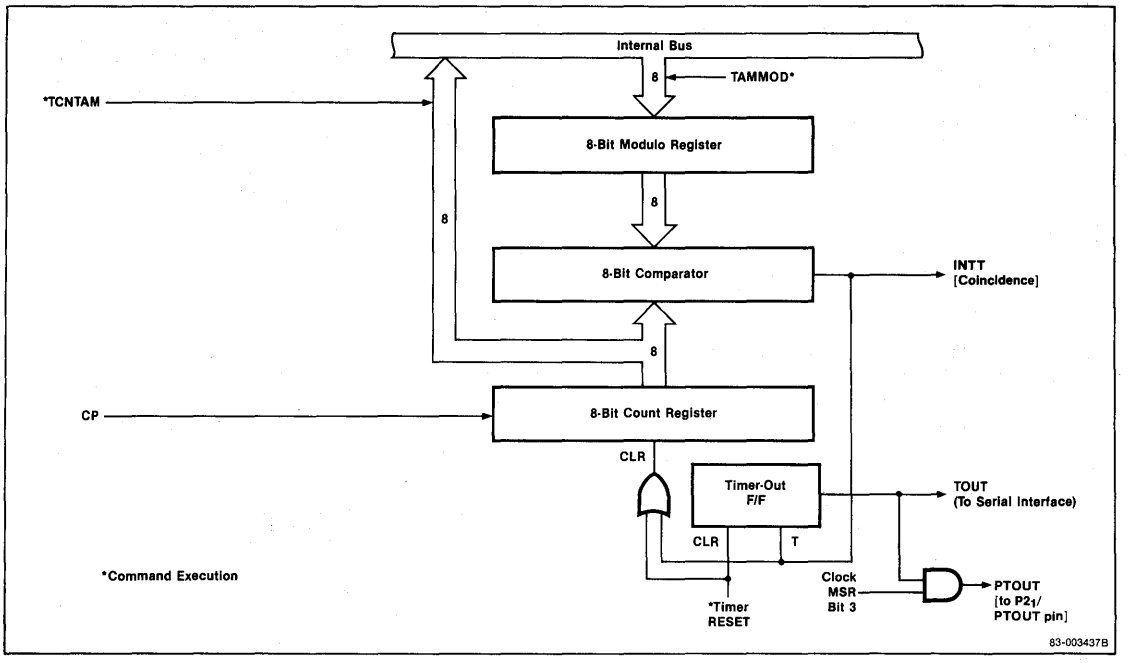
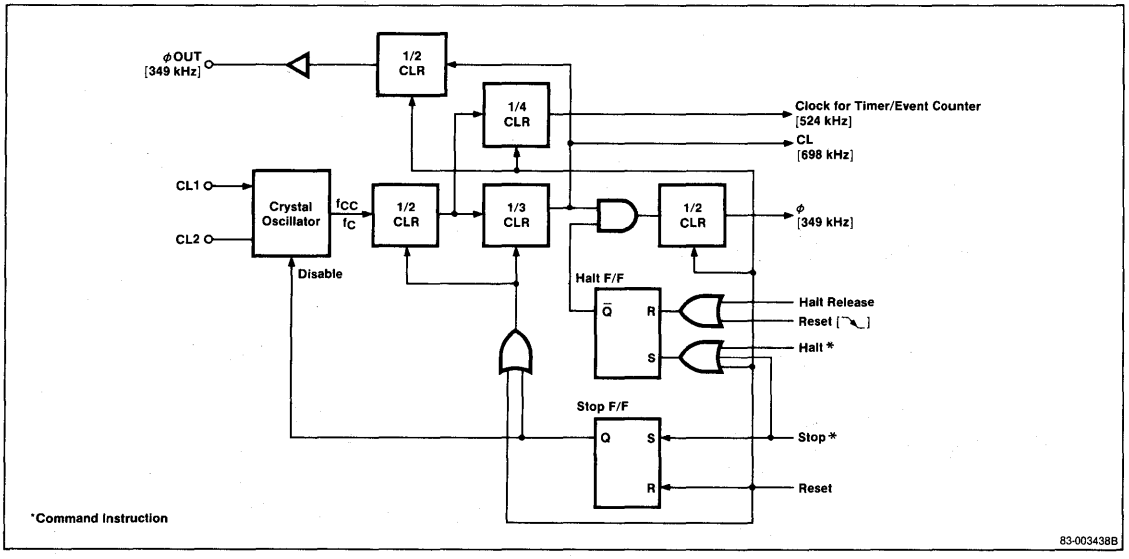


Figure 5. System Clock Circuitry



System Clock and Timing Circuitry

There are four time bases available for the μPD7507H/08H. Table 4 shows these bases and the frequencies generated.

The CPU clock is used by the CPU and serial interface. The system clock is used by the timer/event counter and the INT1 signal.

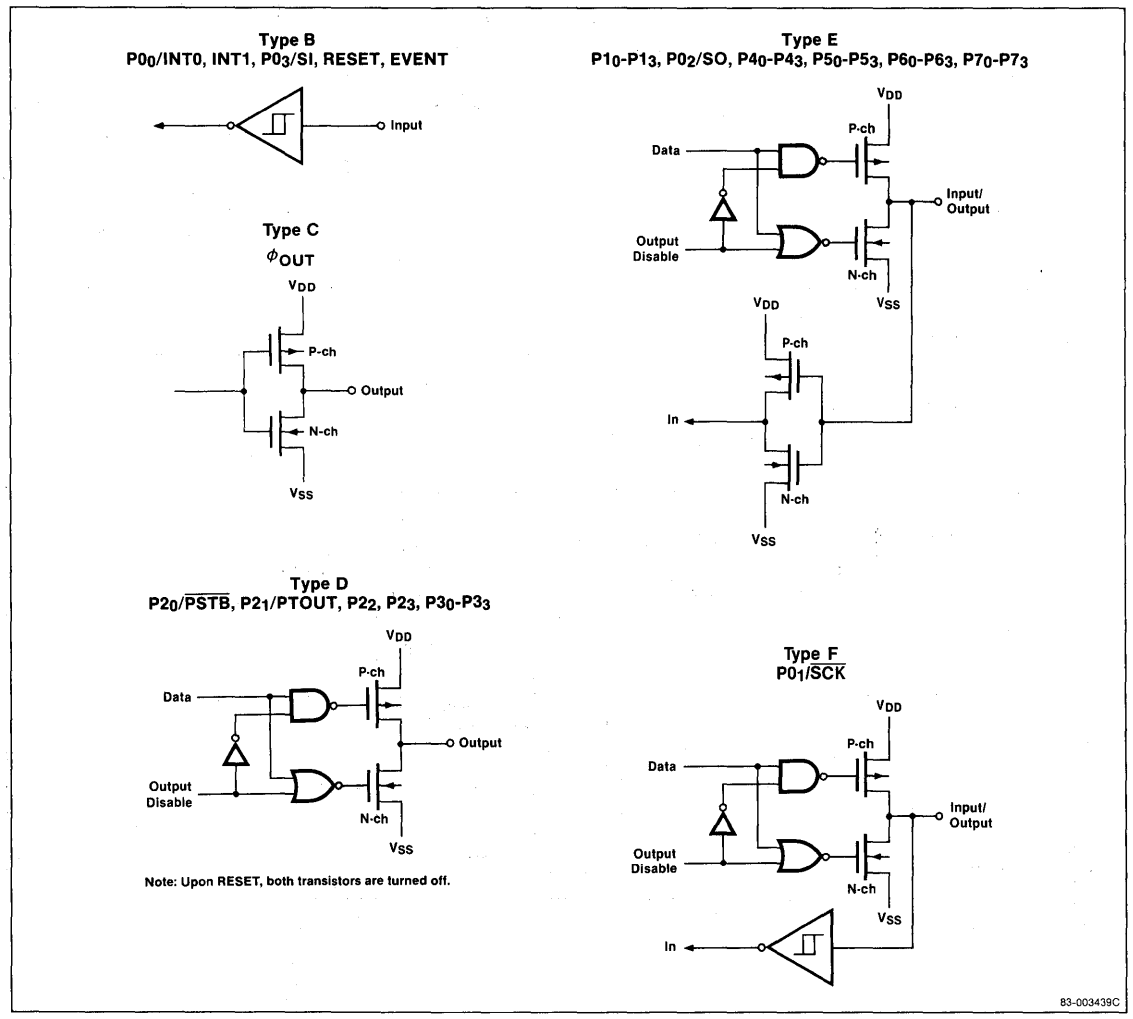
Table 4. μPD7507H/08H Time Bases

Base	Symbol	Frequency
System clock	CL	1/6 f_{CC} (698 kHz/4.19 MHz)
CPU clock		1/12 f_{CC} (349 kHz/4.19 MHz)
External clock	ϕ_{OUT}	1/12 f_{CC} (349 kHz/4.19 MHz)
Timer/event counter clock	—	1/8 f_{CC} (524 kHz/4.19 MHz)

I/O Port Interfaces

Figure 6 shows the internal circuit configurations at the I/O ports.

Figure 6. Interface at Input/Output Ports



Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	−10 to 70°C
Storage temperature, T_{STG}	−65 to 150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
All input and output voltages	−0.3 to V_{DD} + 0.3 V
Output current, high, I_{OH}	
One pin	−5 mA
All pins, total	−20 mA
Output current, low, I_{OL}	
One pin	17 mA
Ports 6, 7	20 mA
Total ports	200 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

		Limits			
Parameter	Symbol	Typ	Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	f = 1 MHz; unmeasured pins returned to V_{SS}
Output capacitance	C_O		15	pF	
I/O capacitance	C_{IO}		15	pF	

3

DC Characteristics

$T_A = -10$ to $+70°C$; $V_{DD} = 2.7$ to 6.0 V (5 V ±10% for 75CG08H)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, CL2
	V_{IH2}	$V_{DD} - 0.5$		V_{DD}	V	CL1, CL2
	V_{IHDR}	0.9 V_{DDDR}		$V_{DDDR} + 0.2$	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, CL2
	V_{IL2}	0		0.5	V	CL1, CL2
Output voltage, high	V_{OH}	$V_{DD} - 1.0$			V	$I_{OH} = -1.0$ mA; $V_{DD} = 4.5$ to 6.0 V; except A_{11}/V_{PP}
		$V_{DD} - 0.5$			V	$I_{OL} = -100\ \mu A$
		$V_{DD} - 0.75$			V	A_{11}/V_{PP}; $I_{OH} = -5$ mA (μPD75CG08H only)
Output voltage, low	V_{OL}		0.5	1.5	V	$I_{OL} = 12$ mA; $V_{DD} = 4.5$ to 6.0 V; Ports 2-5
				0.4	V	$I_{OL} = 1.6$ mA; $V_{DD} = 4.5$ to 6.0 V; Ports 6-7
				0.5	V	$I_{OL} = 400\ \mu A$
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, CL2; $V_I = V_{DD}$
	I_{LIH2}			20	μA	CL1, CL2; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, CL2; $V_I = 0$ V
	I_{LIL2}			−20	μA	CL1, CL2; $V_I = 0$ V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	$V_O = 0$ V
Supply voltage	V_{DDDR}	2.0		6.0	V	Data retention mode
Supply current	I_{DD1}		900 (1) 1000 (2)	3000 (1) 3000 (2)	μA μA	Normal operation, $V_{DD} = 4.5$ to 6.0 V; f = 4.19 MHz
			150 (2)	700 (2)	μA	Normal operation, $V_{DD} = 2.7$ to 3.3 V; f = 1 MHz
	I_{DD2}		350 (1) 500 (2)	800 (1) 1100 (2)	μA μA	HALT mode, X1 = 0 V; $V_{DD} = 4.5$ to 6.0 V; f = 4.19 MHz
			70 (2)	180 (2)	μA	HALT mode, X1 = 0 V; $V_{DD} = 2.7$ to 3.3 V; f = 1 MHz
	I_{DD3}		0.1	10	μA	STOP mode

Note:

(1) Crystal oscillation; C1 = C2 = 10 pF.

(2) Ceramic oscillation; C1 = C2 = 30 pF.

AC Characteristics

$T_A = -10$ to $+70°C$; $V_{DD} = 2.7$ to 6.0 V (5 V ±10% for 75CG08H)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CY}	2.86		120	kHz	$V_{DD} = 4.5$ to 5.5 V
		6.7		120	kHz	
EVENT input frequency	f_E	0		700	kHz	$V_{DD} = 4.5$ to 6.0 V
		0		250	kHz	
EVENT input high	t_{EH}	0.7			μs	$V_{DD} = 4.5$ to 6.0 V
EVENT input low	t_{EL}	3.3			μs	
$\overline{SCK}$ cycle time	t_{KCY}	2.5			μs	$\overline{SCK}$ as input; $V_{DD} = 4.5$ to 6.0 V
		10			μs	$\overline{SCK}$ as input
		2.86			μs	$\overline{SCK}$ as output; $V_{DD} = 4.5$ to 6.0 V
		11			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.1			μs	$\overline{SCK}$ as input; $V_{DD} = 4.5$ to 6.0 V
		4.5			μs	$\overline{SCK}$ as input
		1.3			μs	$\overline{SCK}$ as output; $V_{DD} = 4.5$ to 6.0 V
		5.0			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	300			ns	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	450			ns	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			850	ns	$V_{DD} = 4.5$ to 6.0 V
				1200	ns	
Port 1 output setup time to $\overline{PSTB}$ ↑	t_{PST}	(Note 1)			ns	$V_{DD} = 4.5$ to 6.0 V
		(Note 2)			ns	
Port 1 output hold time after $\overline{PSTB}$ ↑	t_{STP}	80			ns	
$\overline{PSTB}$ pulse width	t_{SWL}	(Note 1)			ns	$V_{DD} = 4.5$ to 6.0 V
		(Note 2)			ns	
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width	t_{I1WH}, t_{I1WL}	(Note 3)			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	
Clock stabilization time	t_{OS}	25			ms	$V_{DD} = 4.5$ V

Note:

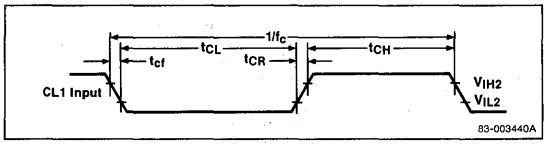
(1) $(3 \div f_{CC}$ or $f_C) - 350$.

(2) $(3 \div f_{CC}$ or $f_C) - 1000$.

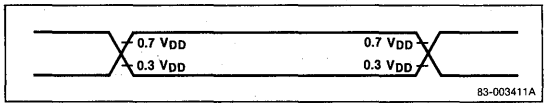
(3) $t_{CY} = 12 \div f_{CC}$ or f_C.

Timing Waveforms

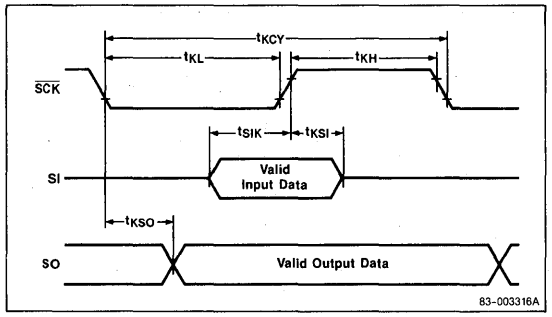
Clocks



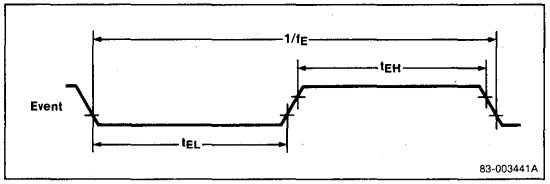
Timing Measurement Points



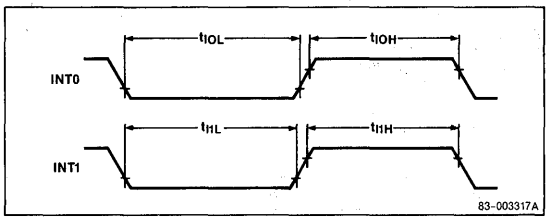
Serial Interface



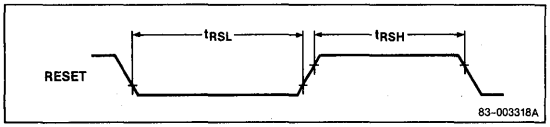
EVENT Input



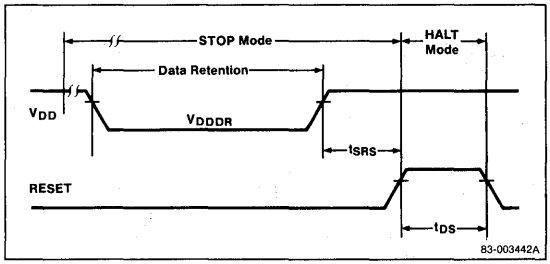
External Interrupts



Reset



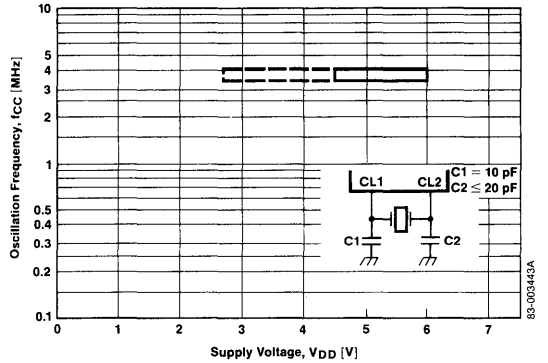
STOP Mode



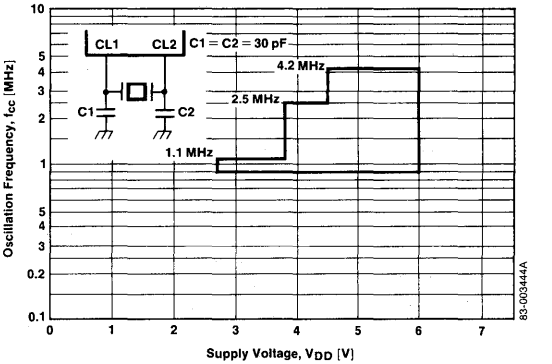
Operating Characteristics (cont)

$T_A = 25°C$

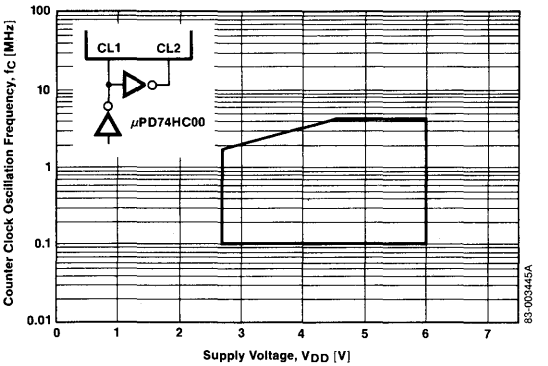
Oscillator Frequency vs Supply Voltage



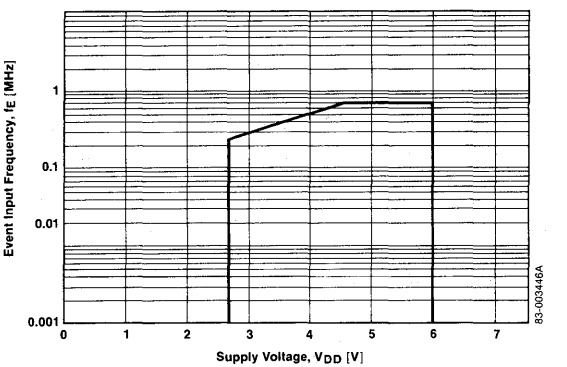
Oscillator Frequency vs Supply Voltage



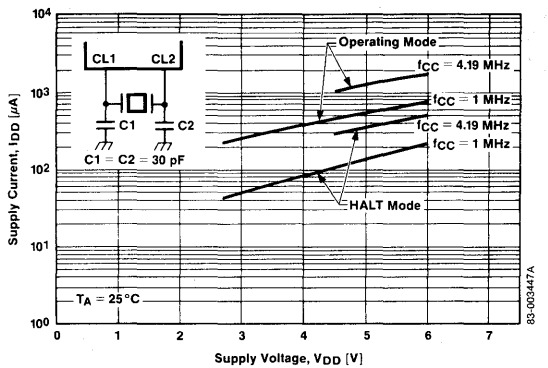
Clock Frequency vs Supply Voltage



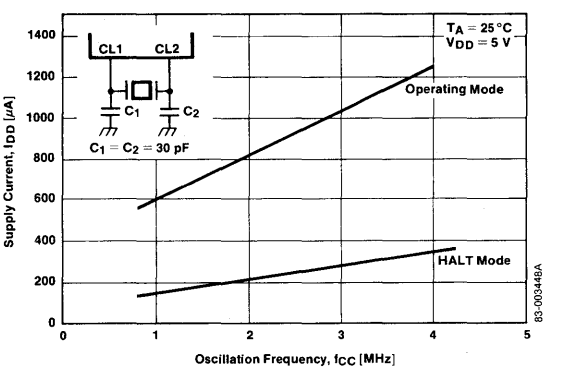
Event Frequency vs Supply Voltage



Supply Current vs Supply Voltage



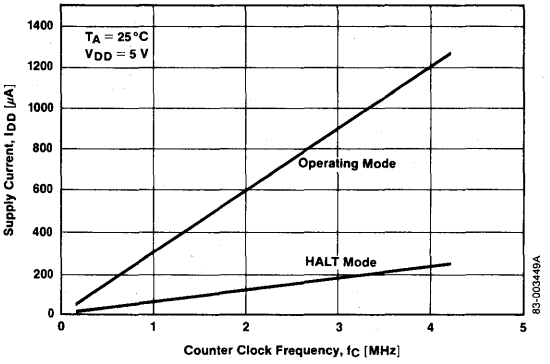
Oscillator Frequency vs Supply Voltage



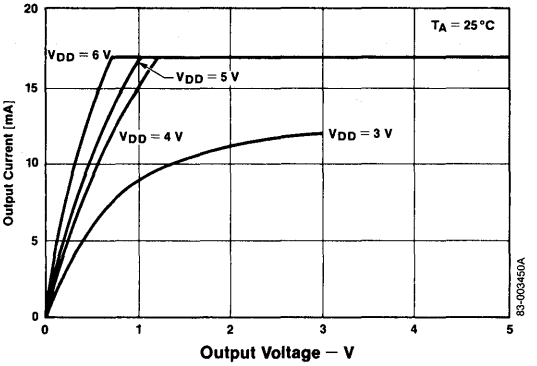
Operating Characteristics (cont)

$T_A = 25°C$

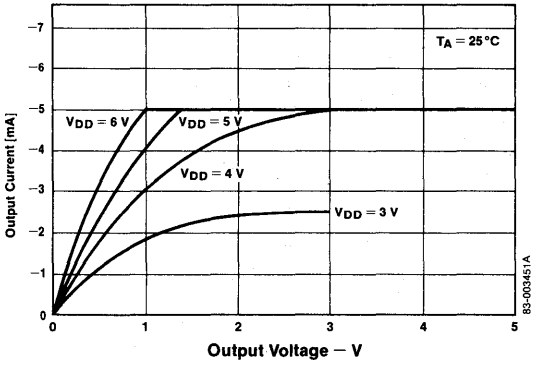
Clock Frequency vs Supply Voltage



V_{OL} vs. I_{OL} [Ports 2-7]



V_{OH} vs. I_{OH}



μPD7507S
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER

Description

The μPD7507S 4-bit, single-chip CMOS microcomputer has advanced fourth-generation architecture. It is a reduced version of the μPD7507, with fewer I/O lines. The device can be operated as low as V_{DD} = 2.2 V to minimize power consumption.

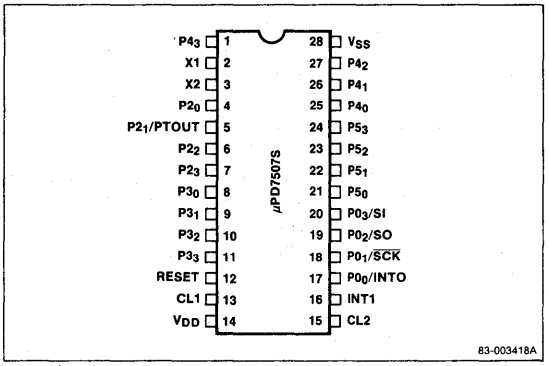
Features

- ☐ Single-chip microcomputer
- ☐ Can operate on a single lithium battery
- ☐ Executes 91 instructions of μPD7500 instruction set A
- ☐ 2048 x 8-bit program ROM
- ☐ 128 x 4-bit data RAM
- ☐ Interrupt capabilities
  - — Two external interrupts: INT0, INT1
  - — Two internal interrupts: INTT, INTS
- ☐ 8-bit timer/event counter
- ☐ 8-bit serial interface
- ☐ Two standby modes
- ☐ Data retention mode
- ☐ 20 I/O lines
- ☐ Internal RC oscillation circuitry
- ☐ Crystal oscillation circuitry for count clock
- ☐ Low power consumption
- ☐ Single 2.2 to 6.0 V operating voltage
- ☐ CMOS technology

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7507SC	28-pin plastic DIP	410 kHz
μPD7507SCT	28-pin plastic shrink DIP	410 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 25-27	$P4_0$-$P4_3$	I/O port 4
2, 3	X2, X1	Crystal clock/external event input
4-7	$P2_0$, $P2_1$/PTOUT, $P2_2$, $P2_3$	Output port 2/timer out F/F signal
8-11	$P3_3$-$P3_0$	Output port 3
12	RESET	RESET input
13, 15	CL1, CL2	System clock input
14	V_{DD}	Positive power supply
16	INT1	External interrupt
17-20	$P0_0$/INT0 $P0_1$/SCK $P0_2$/SO $P0_3$/SI	Input port 0/external interrupt, serial I/O interface
21-24	$P5_3$-$P5_0$	I/O port 5
28	V_{SS}	Ground

3

Pin Functions

$P0_0$/INT0, $P0_1$/$\overline{SCK}$, [Port 0/External Interrupt, Serial Interface] $P0_2$/SO, $P0_3$/SI

4-bit input port/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO, and the serial clock $\overline{SCK}$ (active low) used for synchronizing data transfer make up the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT0, a rising-edge triggered interrupt. If $P0_0$/INT0 is unused, it should be connected to ground. If $P0_1$/$\overline{SCK}$, $P0_2$/SO, or $P0_3$/SI are unused, connect them to ground or V_{DD}.

$P2_0$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2]

4-bit latched three-state output port. Line $P2_1$ is shared with PTOUT, the timer out F/F signal. If any pins are unused, leave them open.

$P3_3$-$P3_0$ [Port 3]

4-bit latched three-state output port. Leave unused pins open.

$P4_3$-$P4_0$ [Port 4]

4-bit input/latched three-state output port. This port, with port 5, also performs 8-bit parallel I/O. In input mode, connect unused pins to ground or V_{DD}. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [Port 5]

4-bit input/latched three-state output port. This port, with port 4, also performs 8-bit parallel I/O. In input mode, connect unused pins to ground or V_{DD}. In output mode, leave unused pins open.

X2, X1 [Crystal Clock/External Event Input]

Connect a crystal oscillator circuit to input X1 and output X2 for crystal clock operation. Alternatively, connect external event pulses to input X1 and leave output X2 open for external event counting. If X1 is not used, connect it to ground. If X2 is not used, leave it open.

CL1, CL2 [System Clock Input]

Connect an 82-kΩ resistor across CL1 and CL2 and connect a 33-pF capacitor from CL1 to GND (200 kHz). Alternatively, connect an external clock source to CL1 and leave CL2 open.

INT1 [External Interrupt]

This is a rising edge-triggered interrupt.

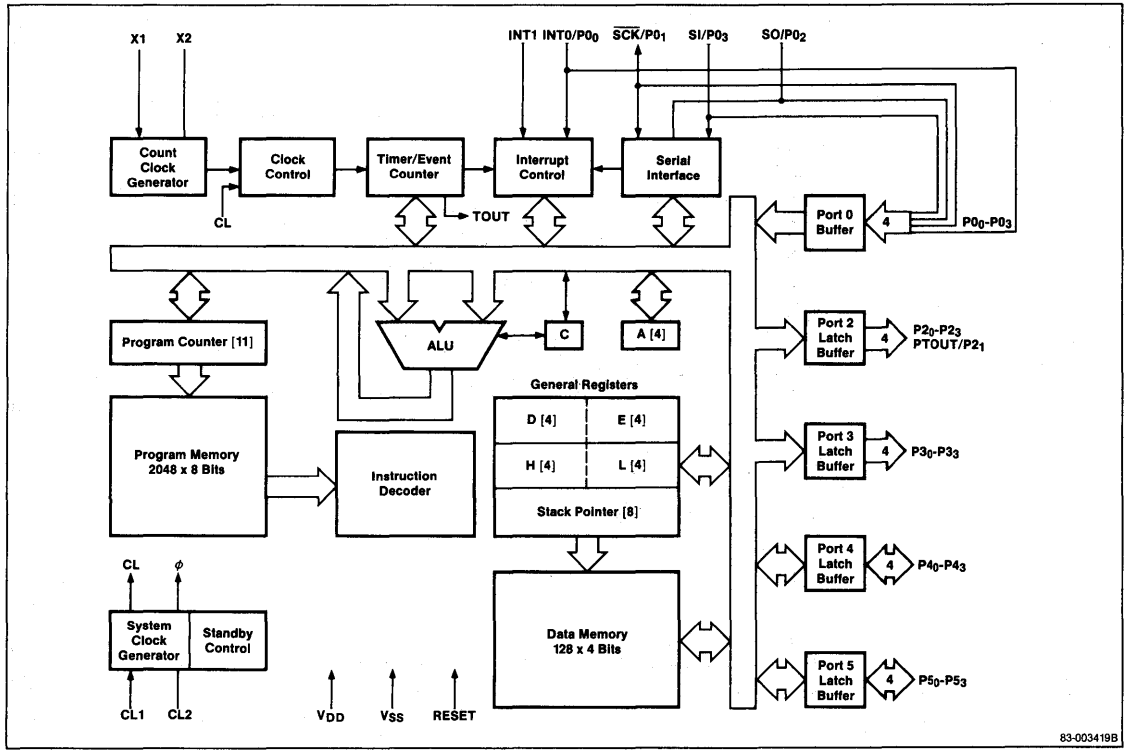
V_{DD} [Power Supply]

Positive power supply. Apply a single voltage in the range 2.2 to 6.0 V for proper operation.

V_{SS} [Ground]

Ground.

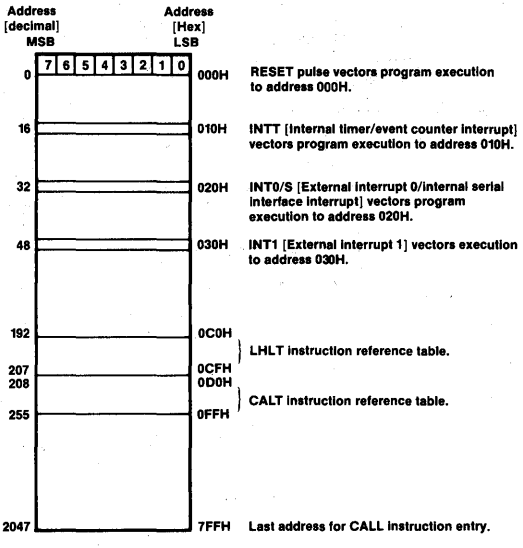
Block Diagram



Memory Map

Figure 1 shows the program memory map of the μPD7507S.

Figure 1. Program Memory Map



83-003421B

Clock Control Circuit

The clock control circuit consists of a 4-bit clock mode register (bits CM_0-CM_3), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and the count clock generator circuit (I). It also selects the clock source and divides the signal according to the setting in the clock mode register. It supplies the timer/event counter with the count pulse. Figure 2 shows the clock control circuit.

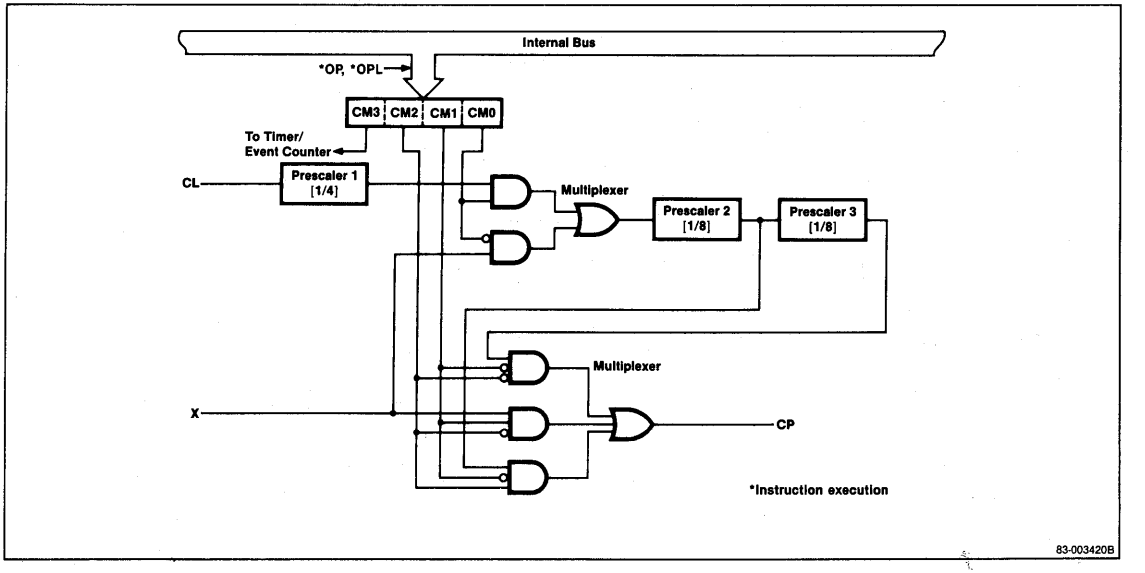
Table 1 lists the codes set in the clock mode register by the OP 12 and OPL instruction to specify the count pulse frequency. CM_3 controls the timer out flip flop. When CM_3 is 0, the timer out F/F is disabled; when CM_3 is 1, it is output. When you set the clock mode register with the OPL instruction, clear the high-order two bits of the accumulator.

Table 1. Selecting the Count Pulse Frequency

CM_2	CM_1	CM_0	Frequency Selected
0	0	0	CL/256
0	0	1	X/64
0	1	0	X
0	1	1	X
1	0	0	CL/32
1	0	1	X/8
1	1	0	Not used
1	1	1	Not used

CM_3	Timer F/F Output
0	Disabled
1	Output

Figure 2. Clock Control Circuit



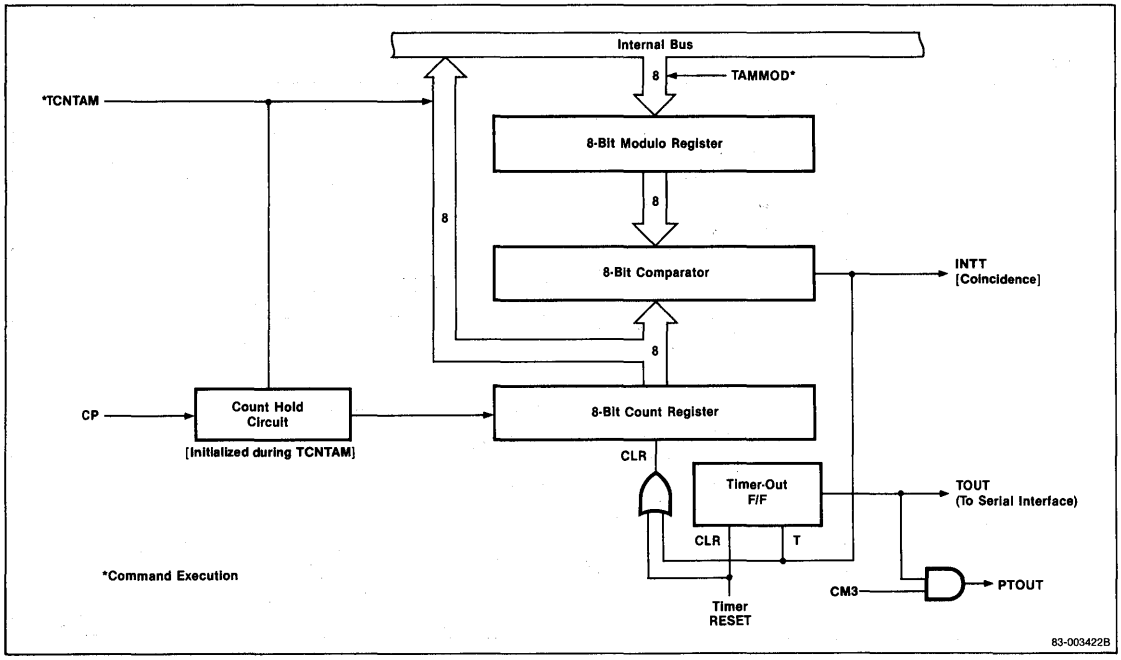
Timer/Event Counter

The timer/event counter consists of an 8-bit counter, an 8-bit modulo register, an 8-bit comparator, and a timer-out flip-flop as shown in figure 3.

The 8-bit counter is a binary up-counter which is incremented each time a count pulse is input. The TIMER instruction, an INTT coincidence signal, or a RESET signal clears it to 00H. The 8-bit modulo register determines the number of counts the count register holds. The TAMMOD instruction loads the modulo register. RESET sets the modulo register to FFH.

The 8-bit comparator compares the contents of the count register to the modulo register and outputs a coincidence signal when these are equal.

Figure 3. Timer/Event Counter

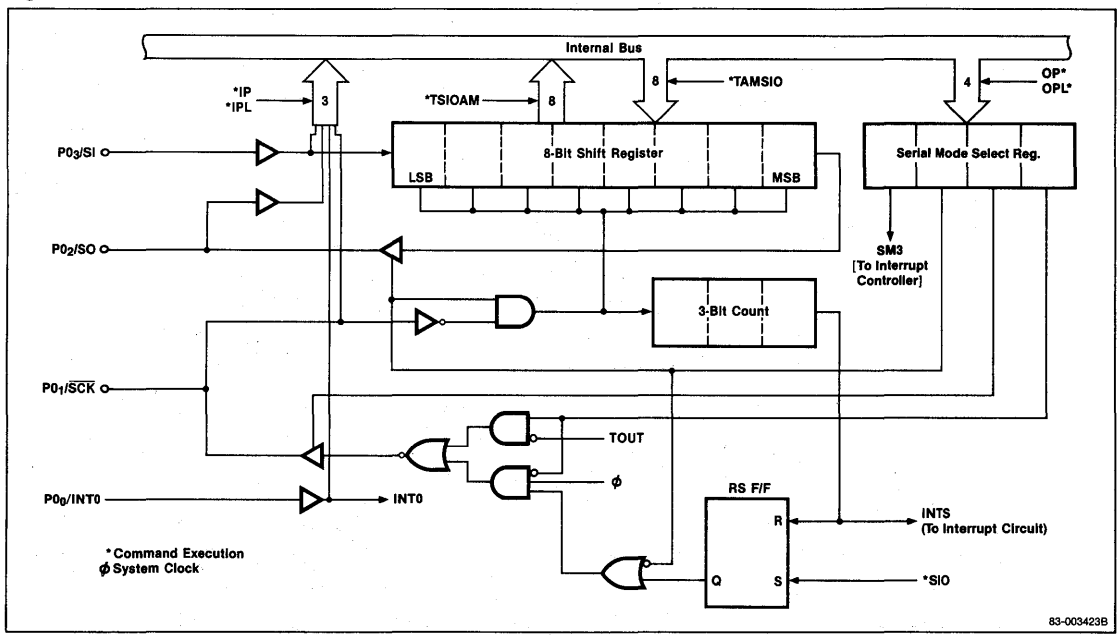


Serial Interface

The 8-bit serial interface allows the μPD7507S to communicate with peripheral devices such as the μPD7001 A/D convertor, the μPD7227 dot matrix LCD controller/driver, and other microprocessors or microcomputers. Figure 4 shows the serial interface.

The serial interface consists of an 8-bit shift register, a 3-bit $\overline{SCK}$ pulse counter, the SI input port, the SO output port, the $\overline{SCK}$ serial clock I/O port, and a 4-bit serial mode select register (MSR). The MSR selects serial I/O or port 0 operation.

Figure 4. Serial Interface



Interrupts

The μPD7507S has four vectored, prioritized interrupts. Two of these interrupts, INTT and INTS, are internally generated from the timer/event counter and serial interface, respectively. INT0 and INT1 are externally generated. Table 2 is a summary of the four interrupts. Figure 5 is the block diagram.

System Clock and Timing Circuitry

Timing generation for the μPD7507S is internally generated except for a frequency reference, which can be an RC circuit or an external clock source. Connect the frequency reference to the on-chip oscillator for the feedback and phase shift required for oscillation. Figures 6 to 9 show the connections for count clocks and system clocks.

Table 3 shows the operating status of the various logic blocks under the three power-down modes.

Table 2. μPD7507S Interrupts

Source	Function	Location	Priority	ROM Vector Address
INTT	Coincidence in timer/event counter	Internal	1	10H
INTS	Transfer complete signal from serial interface	Internal	2	20H
INT0	INT0 pin	External	2	20H
INT1	INT1 pin	External	3	30H

Figure 5. Interrupt Block Diagram

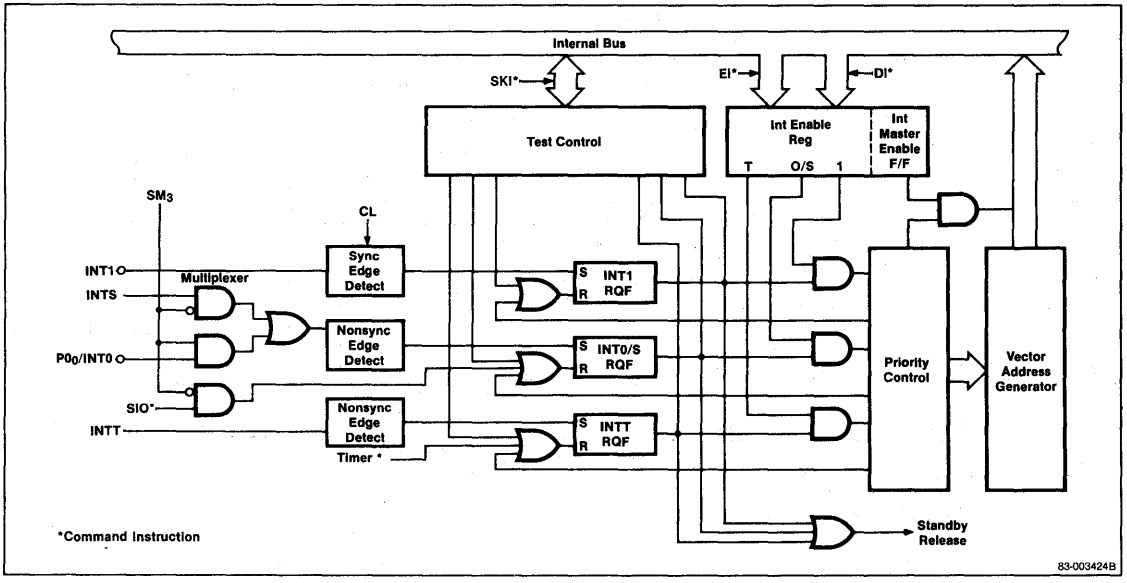


Figure 6. Count Clock, Crystal Oscillator

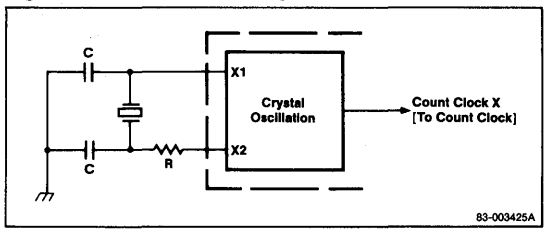


Figure 7. Count Clock, External Source

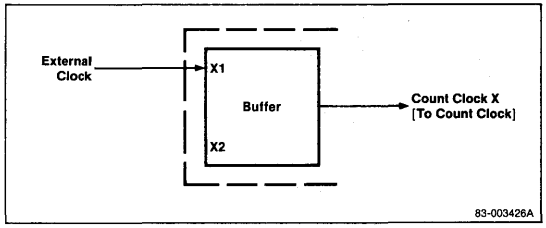


Figure 8. System Clock, RC Oscillation

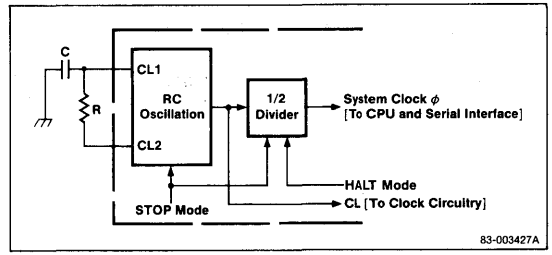


Figure 9. System Clock, External Source

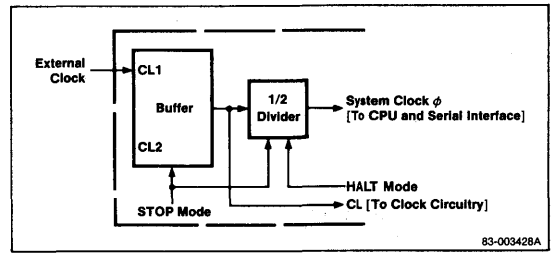


Table 3. Power-Down Operating Status

	Power Down Mode		
Logic Block	**HALT**	**STOP**	**Data Retention**
System clock	(1)	Disabled	Disabled
X2	Normal	Normal	Disabled
CPU	Disabled	Disabled	Disabled
RAM	Data retained	Data retained	Data retained
Internal registers	Data retained	Data retained	Data retained
Timer/event counter	Normal	(3)	Disabled
Serial interface	(2)	(2)	Disabled
INT0	Normal	Normal	Disabled
INT1	Normal	Disabled	Disabled
RESET	Normal	Normal	(4)

Note:

(1) Supplied to timer/event counter but not to CPU or serial interface.

(2) Can function normally if the MSR is set to get the $\overline{SCK}$ signal externally or from the TOUT signal.

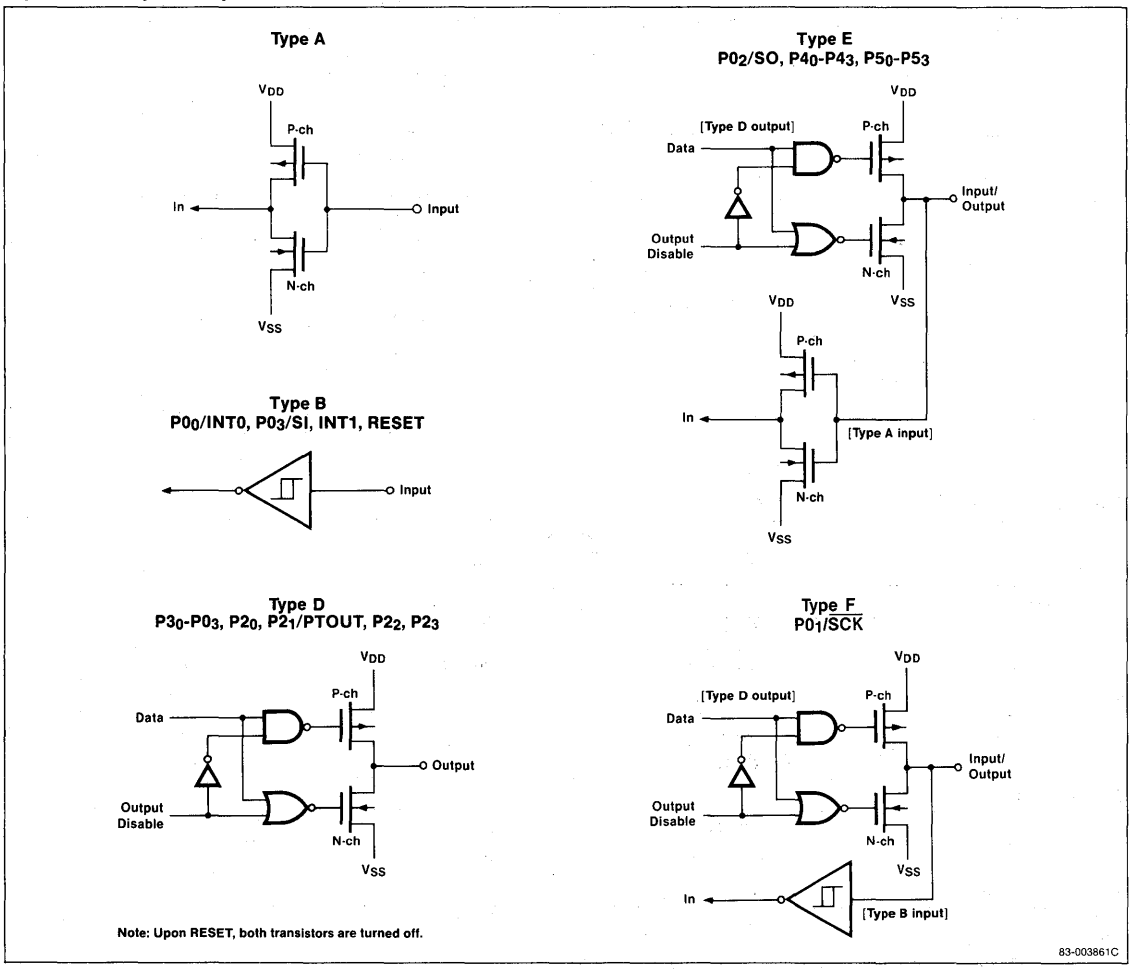
(3) Can function normally if the clock MSR is set to use X1 as the source for the count pulse.

(4) To enter the data retention mode, raise RESET while V_{DD} is lowered. To end the data retention mode, raise RESET when V_{DD} is raised, then lower it. INTT, INT0, INTS or RESET releases the STOP mode. RESET or any interrupt releases the HALT mode.

I/O Port Interfaces

Figure 10 shows the configurations at the I/O ports.

Figure 10. Input/Output Port Interfaces



Absolute Maximum Ratings

Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−6.5 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 to V_{DD} + 0.3 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
Output current high, I_{OH}	
One pin	−17 mA
Total, all pins	−34 mA
Output current low, I_{OL}	
One pin	17 mA
Total, all pins	
Ports P2, P3, and $P4_3$	25 mA
Ports P5 and $P4_0$-$P4_2$	25 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

Parameter	Symbol	Limits Typ	Limits Max	Unit	Test Conditions
Input capacitance	C_I		15	pF	f = 1 MHz; unmeasured pins returned to V_{SS}
Output capacitance	C_O		15	pF	
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

For V_{DD} = 2.7 to 6.0 V

$T_A = -10$ to +70°C

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.5	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	I_{OH} = 1.0 mA; V_{DD} = 4.5 to 6.0 V
		V_{DD} − 0.5			V	I_{OL} = −100 μA
Output voltage, low	V_{OL}			0.4	V	I_{OL} = 1.6 mA; V_{DD} = 4.5 to 6.0 V
				0.5	V	I_{OL} = 400 μA
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	I_{LIL2}			−10	μA	CL1, X1; V_I = 0 V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		300	900	μA	Normal operation, V_{DD} = 5 V ±10%; R = 82 kΩ ±2%, C = 33 pF ±5%
			70	300	μA	Normal operation, V_{DD} = 3 V ±10%; R = 160 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		1	20	μA	Stop mode, X1 = 0 V; V_{DD} = 5 V ±10%
			0.3	10	μA	Stop mode, X1 = 0 V
	I_{DDDR}		0.2	10	μA	Data retention mode V_{DDDR} = 2.0 V

3

DC Characteristics (cont)

V_{DD} = 2.2 to 3.3 V

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1
	V_{IH2}	V_{DD} − 0.1		V_{DD}	V	CL1, X1
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.2 V_{DD}	V	Except CL1, X1
	V_{IL2}	0		0.2	V	CL1, X1
Output voltage, high	V_{OH}	V_{DD} − 0.5			V	I_{OH} = −80 μA
Output voltage, low	V_{OL}			0.5	V	I_{OL} = 350 μA
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1; V_I = 0 V
	I_{LIL2}			−10	μA	CL1, X1; V_I = 0 V
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	V_O = 0 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		50	200	μA	Normal operation, R = 270 kΩ ±2%, C = 33 pF ±5%
			30	100	μA	Normal operation, V_{DD} = 2.2 V; R = 270 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		0.3	10	μA	Stop mode, X1 = 0 V
			0.2	10	μA	Stop mode, X1 = 0 V; V_{DD} = 2.2 V
	I_{DDDR}		0.2	10	μA	Data retention mode, V_{DDDR} = 2.0 V

AC Characteristics

For V_{DD} = 2.7 to 6.0 Volts

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	V_{DD} = 5 V ±10%; R = 82 kΩ ±2% (Note 1)
		75	100	120	kHz	V_{DD} = 3 V ±10%; R = 160 kΩ ±2% (Note 1)
		75		135	kHz	R = 160 kΩ ±2% (Note 1)
	f_C	10		410	kHz	CL1, external clock, 50% duty; V_{DD} = 4.5 to 6.0 V
		10		125	kHz	CL1, external clock, 50% duty; V_{DD} = 2.7 V
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.2		50	μs	CL1, external clock; V_{DD} = 4.5 to 6.0 V
		4.0		50	μs	CL1, external clock; V_{DD} = 2.7 V
Counter clock frequency	f_{XX}	20	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input, 50% duty; V_{DD} = 4.5 to 6.0 V
		0		125	kHz	X1, external pulse input, 50% duty; V_{DD} = 2.7 V
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.2			μs	X1, external pulse input; V_{DD} = 4.5 to 6.0 V
		4.0			μs	X1, external pulse input; V_{DD} = 2.7 V
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		4.9			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		8.0			μs	$\overline{SCK}$ as input
		16.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ as input; V_{DD} = 4.5 to 6.0 V
		2.2			μs	$\overline{SCK}$ as output; V_{DD} = 4.5 to 6.0 V
		4.0			μs	$\overline{SCK}$ as input
		8.0			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	300			ns	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	450			ns	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			850	ns	V_{DD} = 4.5 V to 6.0 V
				1200	ns	
INT0 pulse width	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	2/f			μs	
RESET pulse width	t_{RSH}, t_{RSL}	10			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leqq$ 60 ppm.

AC Characteristics (cont)

For V_{DD} = 2.2 to 3.3 V

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	40	60	70	kHz	R = 240 kΩ ±2% (Note 1)
		43	55	65	kHz	V_{DD} = 2.2 V; R = 240 kΩ ±2% (Note 1)
	f_C	10		80	kHz	CL1, external clock, 50% duty
System clock rise and fall time	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	6.1		50	μs	CL1, external clock
Counter clock frequency	f_{XX}	20	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		80	kHz	X1, external pulse input, 50% duty
Counter clock rise and fall time	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	6.1			μs	X1, external pulse input
$\overline{SCK}$ cycle time	t_{KCY}	12.5			μs	$\overline{SCK}$ as input
		25			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	6.5			μs	$\overline{SCK}$ as input
		11.5			μs	$\overline{SCK}$ as output
SI setup time to $\overline{SCK}$ ↑	t_{SIK}	1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{KSI}	1			μs	
SO delay time after $\overline{SCK}$ ↓	t_{KSO}			2	μs	
INT0 pulse width	t_{I0H}, t_{I0L}	30			μs	
INT1 pulse width	t_{I1H}, t_{I1L}	2/f			μs	
RESET pulse width	t_{RSH}, t_{RSL}	30			μs	
RESET setup time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Note:

(1) RC network at CL1 and CL2; C = 33 pF ±5%, $|\Delta C/°C| \leq 60$ ppm.

Recommended R and C Values for System Clock Oscillation Circuit

T_A = −10 to +70°C

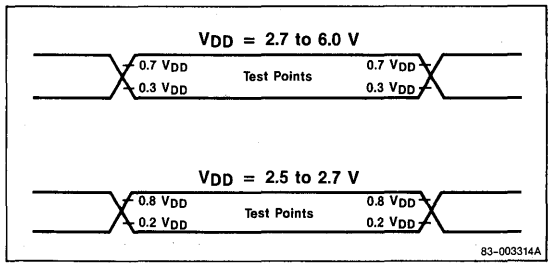
Supply Voltage Range	Recommended Values (Note 1)	Frequency Range
4.5 to 6.0 V	R = 82 kΩ ±2%	150 to 250 kHz, 200 kHz typical
2.7 to 3.3 V	R = 160 kΩ ±2%	75 to 120 kHz, 100 kHz typical
2.7 to 6.0 V	R = 160 kΩ± 2%	75 to 135 kHz
2.2 to 3.3 V	R = 270 kΩ ±2%	40 to 70 kHz
2.2V	R = 270 kΩ ±2 %	43 to 65 kHz

Note:

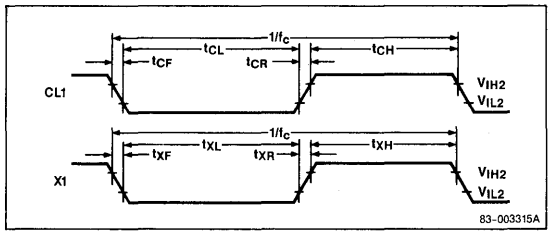
(1) C = 33 pF ±5%, $|\Delta C/°C| \leq 60$ ppm.

Timing Waveforms

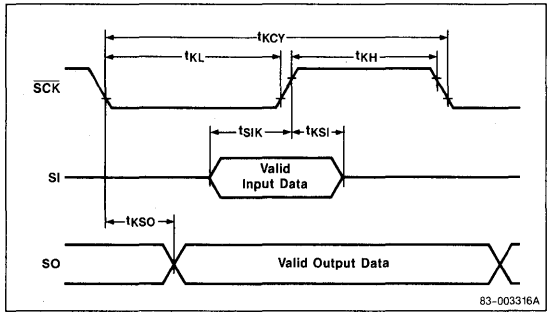
Timing Test Points



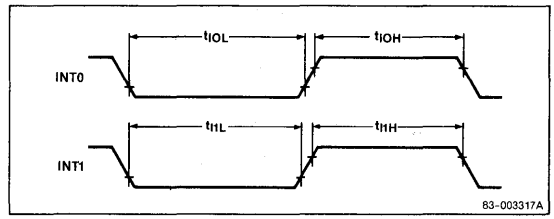
Clocks



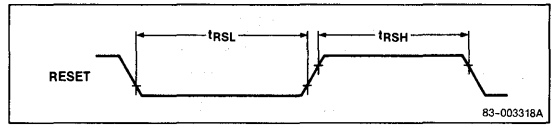
Serial Interface



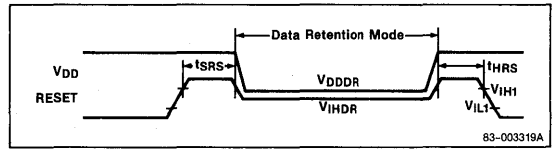
External Interrupts



RESET



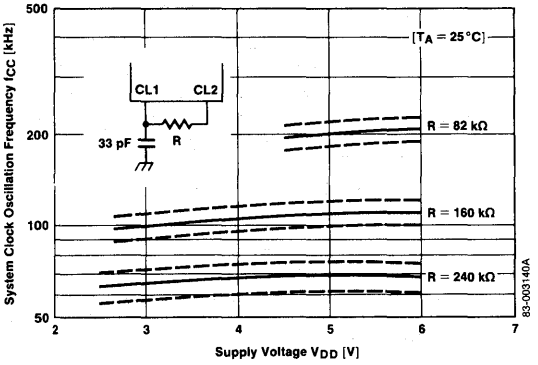
Data Retention Mode



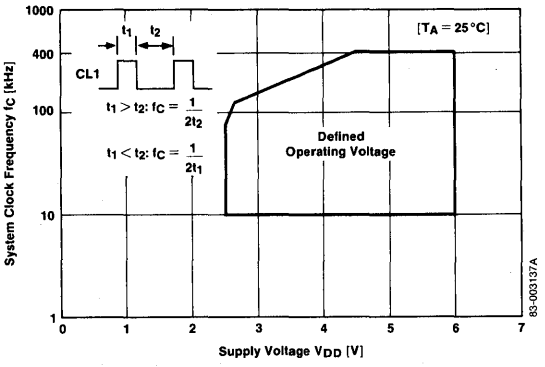
Operating Characteristics

T_A = 25°C

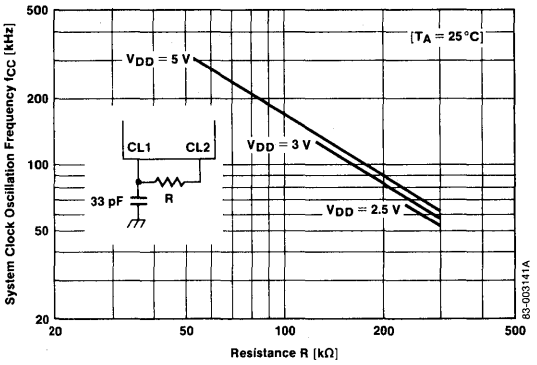
f_{CC} vs V_{DD}



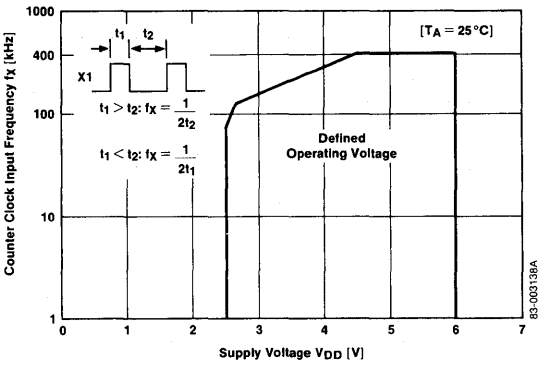
f_C vs V_{DD}



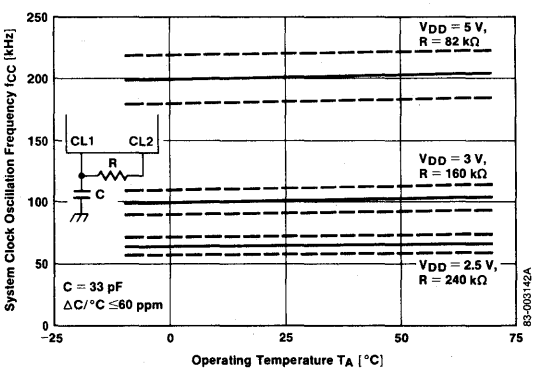
f_{CC} vs R



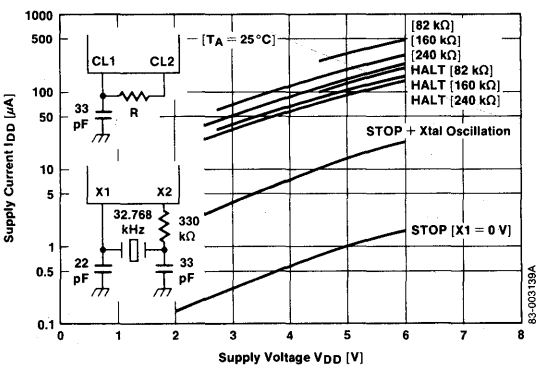
f_X vs V_{DD}



f_{CC} vs T_A



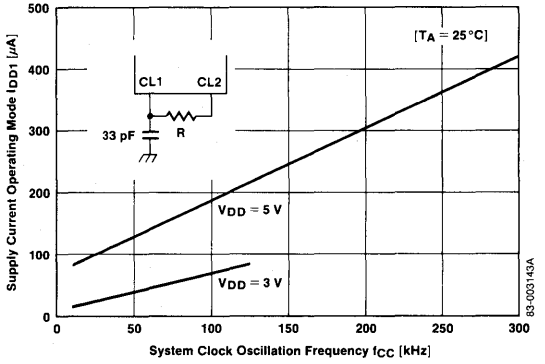
I_{DD} vs V_{DD}



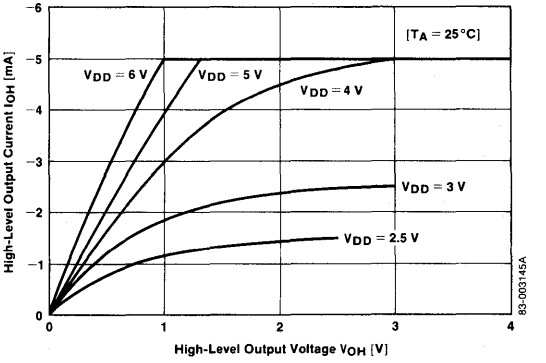
Operating Characteristics (cont)

T_A = 25°C

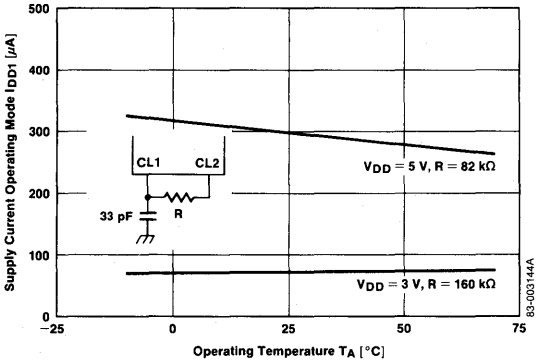
I_{DD1} vs f_{CC}



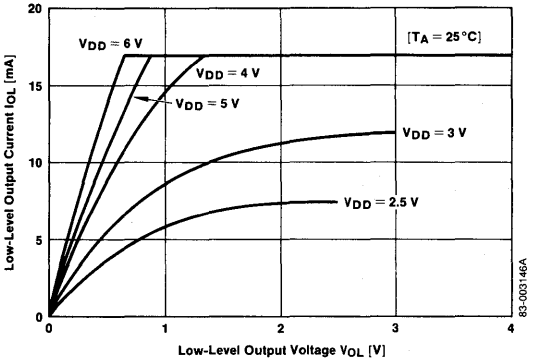
I_{OH} vs V_{OH}



I_{DD1} vs T_A



I_{OL} vs V_{OL}



3

μPD7508A
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH FIP® DRIVER

Description

The μPD7508A 4-bit, single-chip CMOS microcomputer has advanced fourth-generation architecture. It is identical to the μPD7508 except for a smaller RAM and 16 lines of vacuum fluorescent display FIP drive capability. It contains a 4096 x 8-bit ROM and a 208 x 4-bit RAM.

The μPD7508A contains four 4-bit general purpose registers outside RAM. The subroutine stack is implemented in RAM for greater nesting depth and flexibility. The μPD7508A executes 92 instructions of the μPD7500 series instruction set A with a 10-μs cycle time.

The μPD7508A has two external and two internal edge-triggered hardware vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to reduce software requirements. Ports 3-6 can be pulled to −35 V to drive vacuum fluorescent displays. CMOS technology allows the use of a single 2.7 V to 6.0 V power supply with a maximum current consumption of 900 μA. This is even lower in the HALT and STOP standby modes.

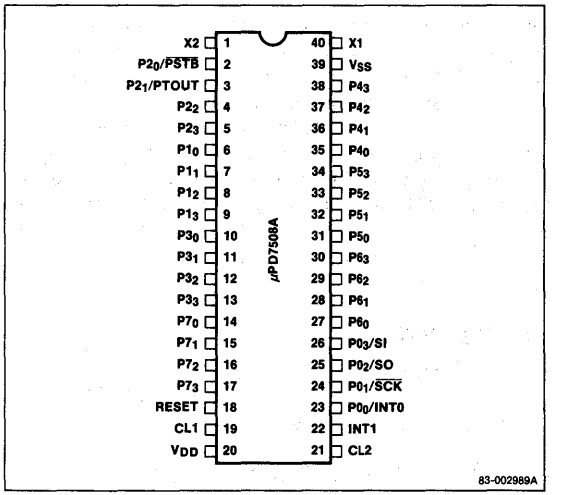
Features

- ☐ Single-chip microcomputer
- ☐ Executes 92 instructions of μPD7500 instruction set A
- ☐ Instruction cycle:
  - — 10 μs/200 kHz (5 V internal)
  - — 5 μs/400 kHz (5 V external)
- ☐ 4096 x 8-bit program ROM
- ☐ 208 x 4-bit data RAM
- ☐ Interrupt capabilities
  - — Two external interrupts: INT0, INT1
  - — Two internal interrupts: INTT, INTS
- ☐ 8-bit timer/event counter
- ☐ 8-bit serial interface
- ☐ Two standby modes
- ☐ Data retention mode
- ☐ 32 I/O lines
- ☐ Four high-voltage (40 V) ports
- ☐ Two high-current (8 mA) ports
- ☐ Internal RC oscillation circuitry
- ☐ Crystal oscillation circuitry for count clock
- ☐ Low power consumption
- ☐ Single 2.7 to 6.0 V operating voltage
- ☐ CMOS technology

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7508AC	40-pin plastic DIP	400 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 40	X2, X1	Crystal clock/external event input port
2-5	$P2_0/\overline{PSTB}$ $P2_1$/PTOUT, $P2_2$, $P2_3$	Output port 2/output strobe pulse, timer out F/F signal
6-9	$P1_0$-$P1_3$	I/O port 1
10-13	$P3_0$-$P3_3$	Output port 3
14-17	$P7_0$-$P7_3$	I/O port 7
18	RESET	RESET input
19, 21	CL1, CL2	System clock inputs
20	V_{DD}	Positive power supply
22	INT1	External interrupt
23-26	$P0_0/\overline{INT0}$, $P0_1/\overline{SCK}$, $P0_2$/SO $P0_3$/SI	Input port 0/ external interrupt, serial I/O interface
27-30	$P6_0$-$P6_3$	I/O port 6
31-34	$P5_0$-$P5_3$	I/O port 5
35-38	$P4_3$-$P4_0$	I/O port 4
39	V_{SS}	Ground

FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

Pin Functions

$P0_0$/INT0, $P0_1$/$\overline{SCK}$, [Port 0/External Interrupt, Serial Interface] $P0_2$/SO, $P0_3$/SI

4-bit input port/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface under control of the serial-mode select register. The serial input SI, serial output SO (active low), and the serial clock $\overline{SCK}$ (active low) used for synchronizing data transfer make up the 8-bit serial I/O interface. Line $P0_0$ is always shared with external interrupt INT0, a rising edge-triggered interrupt. If $P0_0$/INT0 is unused, it should be connected to V_{SS}. If $P0_1$/$\overline{SCK}$, $P0_2$/SO, or $P0_3$/SI are unused, connect them to V_{SS} or V_{DD}.

$P1_0$-$P1_3$ [Port 1]

4-bit input/three-state output port. Data output to port 1 is strobed in synchronization with a $P2_0$/$\overline{PSTB}$ pulse. Connect unused pins to V_{SS} or V_{DD}.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$, $P2_3$ [Port 2]

4-bit latched three-state output port. Line $P2_0$ is shared with $\overline{PSTB}$, the port 1 output strobe pulse. Line $P2_1$ is shared with PTOUT, the timer out F/F signal. Leave unused pins open.

$P3_0$-$P3_3$ [Port 3]

4-bit latched three-state output port. Leave unused pins open.

$P4_0$-$P4_3$ [Port 4]

4-bit latched three-state output port. Can also perform 8-bit parallel I/O with port 5. In input mode, connect unused pins to V_{DD} or GND. In output mode, leave unused pins open.

$P5_3$-$P5_0$ [Port 5]

4-bit input/latched three-state output port. This port also performs 8-bit parallel I/O with port 4. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P6_3$-$P6_0$ [Port 6]

4-bit input/latched three-state output port. The port 6 mode select register configures individual lines as inputs or outputs. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

$P7_0$-$P7_3$ [Port 7]

4-bit input/latched three-state output port. In input mode, connect unused pins to V_{SS} or V_{DD}. In output mode, leave unused pins open.

X2, X1 [Crystal Clock/External Event Input]

For crystal clock operation, connect a crystal oscillator circuit to input X1 and output X2. For external event counting, input external event pulses to input X1 while leaving output X2 open. If X1 is not used, leave it open. If X2 is not used, connect it to ground.

CL1, CL2 [System Clock Input]

Connect an 82 kΩ resistor across CL1 and CL2, and connect a 33 pF capacitor from CL1 to V_{SS} (200 kHz). Alternatively, connect an external clock source to CL1 and leave CL2 open. If CL1 is not used, connect it to V_{SS}.

RESET [Reset]

A high level input to this pin initializes the μPD7508A after power up.

INT1 [Interrupt 1]

External rising edge-triggered interrupt. Connect to V_{SS} if unused.

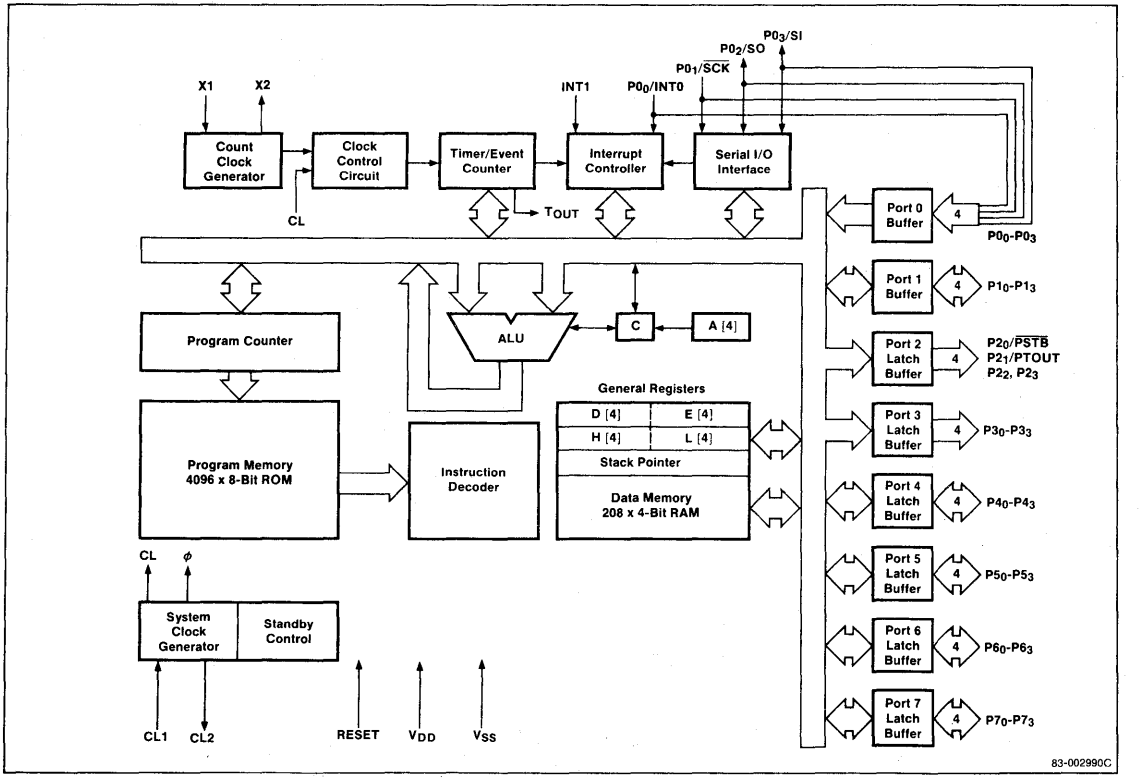
V_{DD} [Power Supply]

Positive power supply. Apply a single voltage in the range 2.7 to 6.0 V for proper operation.

V_{SS} [Ground]

Ground.

Block Diagram

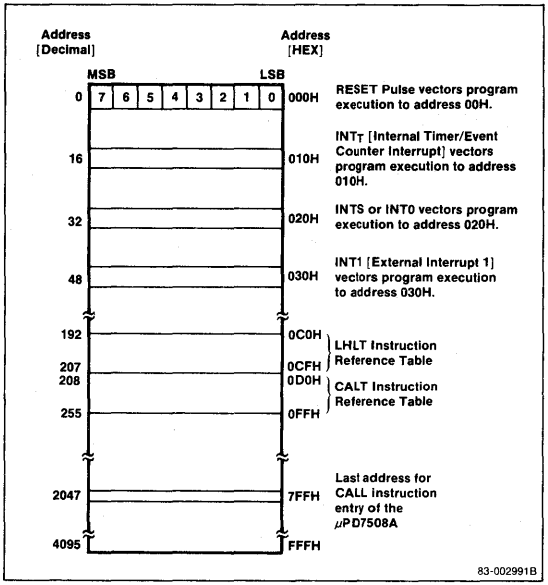


Functional Description

Program Memory

Figure 1 is a map of the 4096 x 8-bit program ROM.

Figure 1. Program Memory Map



Clock Control Circuit

The clock control circuit (figure 2) consists of a 4-bit clock mode register (bits CM_1 and CM_2), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and count clock generator circuit (I). It also selects the clock source and divides the signal according to the setting in the clock mode register. It outputs the count pulse (CP) to the timer/event counter.

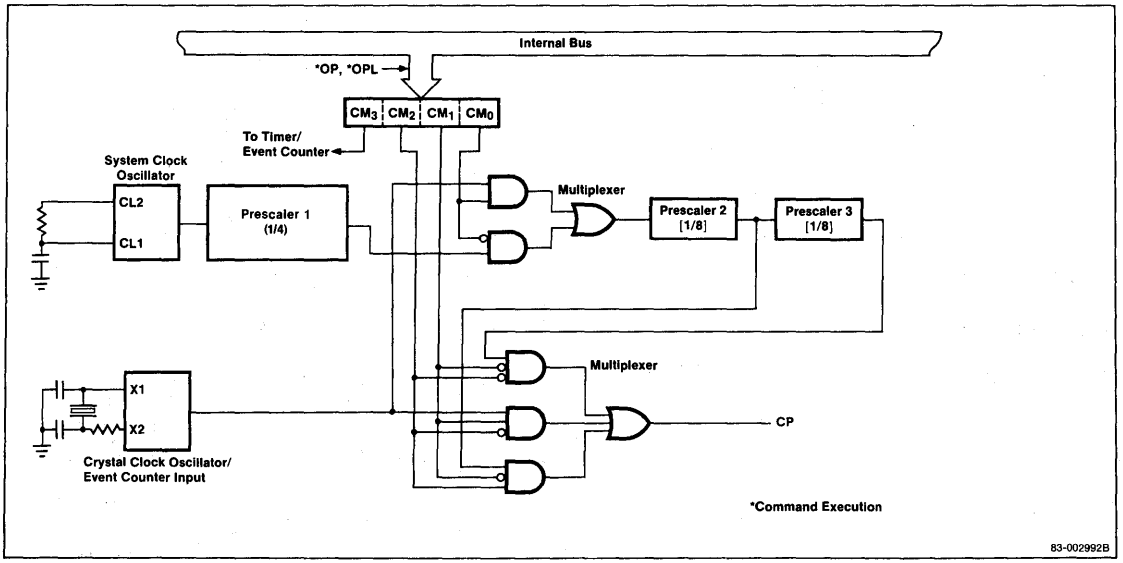
Table 1 lists the codes set in the clock mode register by the OP or OPL instruction to specify the count pulse frequency. Bit CM3 controls the timer out F/F; it is disabled when the bit is 0 and output when the bit is 1. When you set the clock mode register with the OP or OPL instruction, clear the high-order two bits of the accumulator.

Table 1. Selecting the Count Pulse Frequency

CM_2	CM_1	CM_0	Frequency Selected
0	0	0	CL/256
0	0	1	X/64
0	1	0	X
0	1	1	X
1	0	0	CL/32
1	0	1	X/8
1	1	0	Not used
1	1	1	Not used

CM_3	Timer F/F Signal
0	Enabled
1	Disabled

Figure 2. Clock Control Circuit



Timer/Event Counter

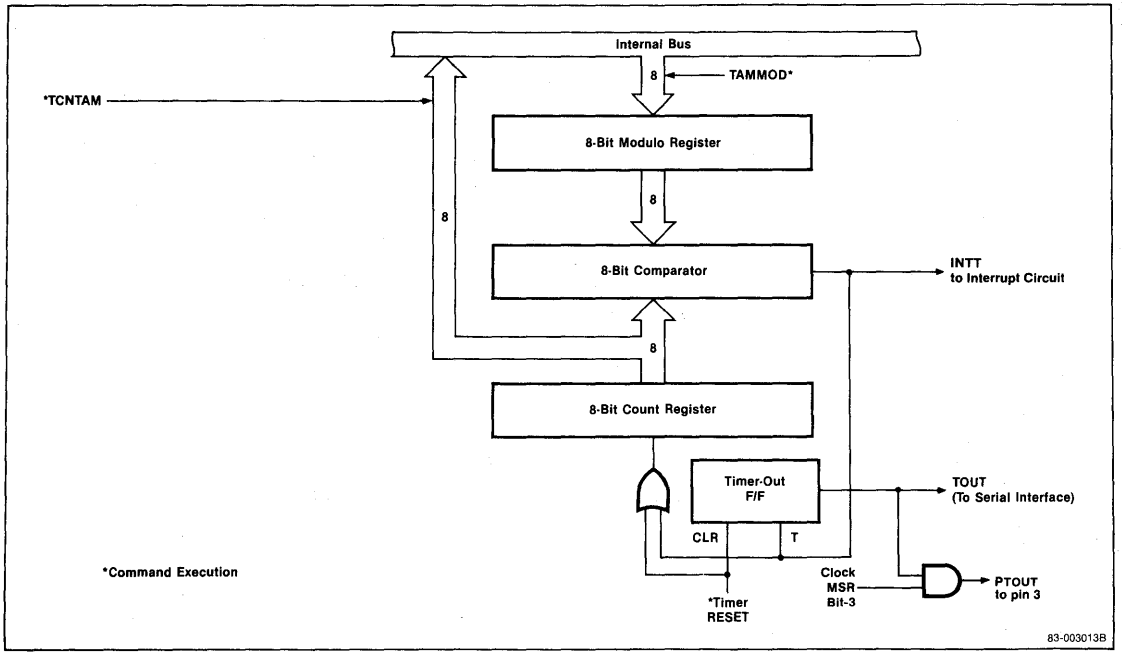
The timer/event counter consists of an 8-bit counter, an 8-bit modulo register, an 8-bit comparator, and a timer out flip flop, as shown in figure 3.

The 8-bit count register is a binary 8-bit up counter which is incremented each time a count pulse is input. The TIMER instruction, a RESET signal, or an INTT coincidence signal clears it to 00H.

The 8-bit modulo register determines the number of counts the count register holds. The TAMMOD instruction loads the contents of the modulo register. RESET sets the modulo register to FFH.

The 8-bit comparator compares the contents of the count register and those of the modulo register and outputs an INTT when they are equal.

Figure 3. Timer/Event Counter

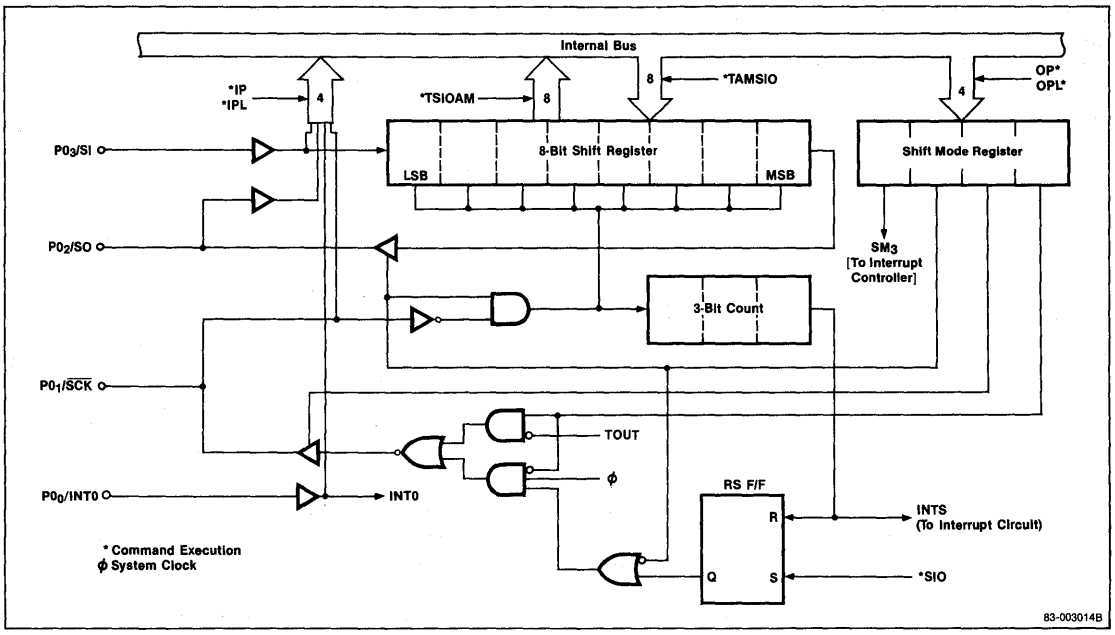


Serial Interface

The 8-bit serial interface allows the μPD7508A to communicate with peripheral devices such as the μPD7001 A/D converter, the μPD7227 dot matrix LCD controller/driver, and other microprocessors or microcomputers. Figure 4 shows the serial interface.

The serial interface consists of an 8-bit shift register, a 3-bit $\overline{SCK}$ pulse counter, the SI input port, the SO output port, the $\overline{SCK}$ serial clock I/O port, and a 4-bit serial mode select register (MSR). The MSR selects serial I/O or port 0 operation.

Figure 4. Serial Interface



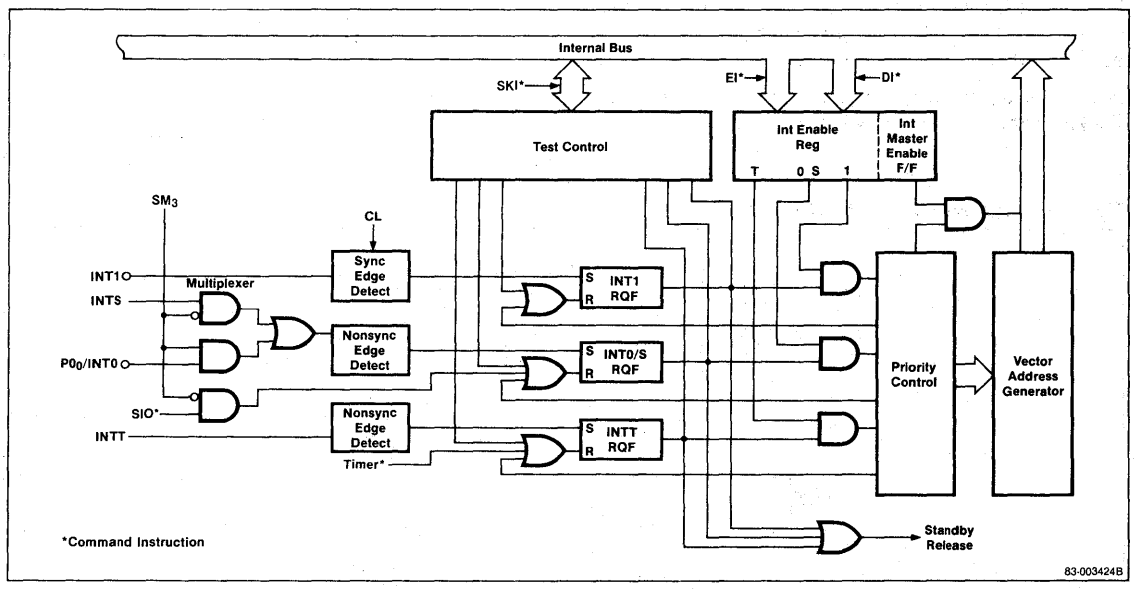
Interrupts

The μPD7508A has four vectored, prioritized interrupts. Two of these interrupts, INTT and INTS, are internally generated from the timer/event counter and serial interface, respectively. INT0 and INT1 are externally generated. Table 2 is a summary of the four interrupts. Figure 5 is a block diagram of the interrupts.

Table 2. μPD7508A Interrupts

Source	Function	Location	Priority	ROM Vector Address
INTT	Coincidence in timer/event counter	Internal	1	10H
INTS	Transfer complete signal from serial interface	Internal	2	20H
INT0	INT0 pin	External	2	20H
INT1	INT1 pin	External	3	30H

Figure 5. Interrupt Block Diagram



System Clock and Timing Circuitry

Timing for the μPD7508A is internally generated except for a frequency reference, which can be an RC circuit or an external clock source. Connect the frequency reference to the on-chip oscillator for the feedback phase shift required for oscillation. Figure 6 shows the connection for an RC circuit. Figures 6 and 7 show the connection for the frequency reference.

The internal oscillator generates a frequency in the range 60 kHz to 300 kHz depending on the frequency reference. For example, at $V_{DD} = 5$ V, an 83 kΩ resistor and a 33 pF capacitor generate a frequency of 200 kHz. The oscillation frequency is fed to the clock control circuit. It is divided by two and the resulting signal is fed to the CPU and serial interface as shown in figure 8.

Table 3 shows the operating status of the various logic blocks under the three power down modes.

Figure 6. RC Circuit Frequency Reference

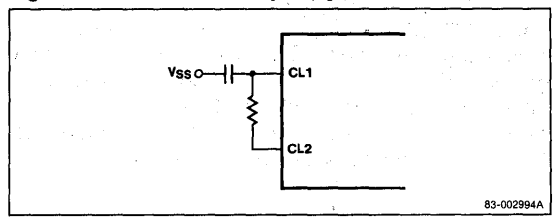


Figure 7. External Clock Frequency Reference

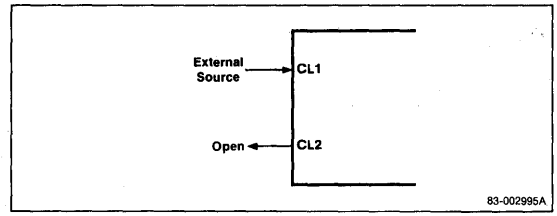


Figure 8. System Clock Circuitry

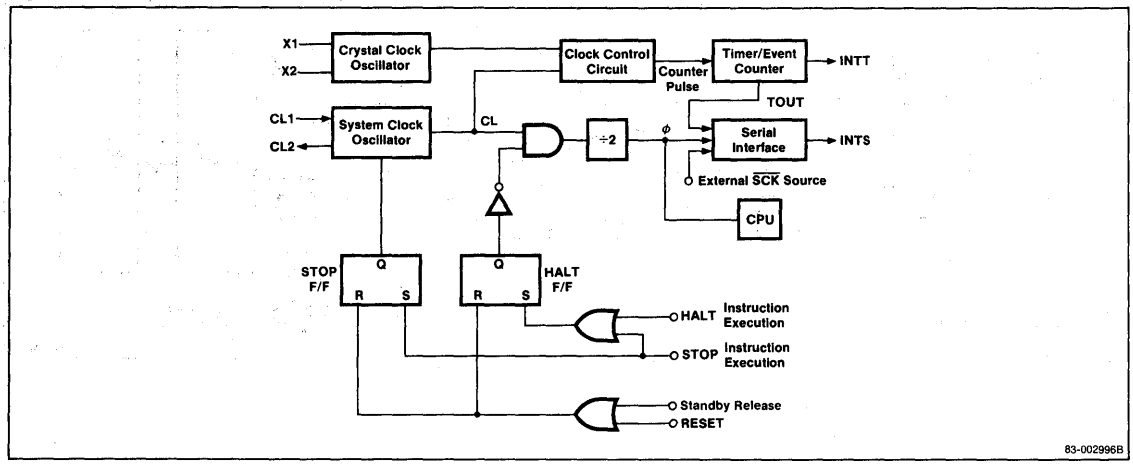


Table 3. Power Down Operating Status

Power Down Mode Logic Block	HALT	STOP	Data Retention
System clock	(1)	Disabled	Disabled
X2	Normal	Normal	Disabled
CPU	Disabled	Disabled	Disabled
RAM	Data retained	Data retained	Data retained
Internal registers	Data retained	Data retained	Data retained
Timer/event counter	Normal	(3)	Disabled
Serial interface	(2)	(2)	Disabled
INT0	Normal	Normal	Disabled
INT1	Normal	Disabled	Disabled
RESET	Normal	Normal	(4)

Note:

(1) Supplied to timer/event counter but not to CPU or serial interface.

(2) Can function normally if the serial MSR is set to get the $\overline{SCK}$ signal externally or from the TOUT signal.

(3) Can function normally if the clock MSR is set to use X1 as the source for the count pulse.

(4) You must raise RESET while V_{DD} is lowered to enter data retention mode. Raise RESET when V_{DD} is raised, then lower it to end the data retention mode. INTT, INT0, INTS or RESET releases STOP mode. RESET or any interrupt releases HALT mode.

Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	−10 to 70°C
Storage temperature, T_{STG}	−65 to 150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	
Except ports 4-6	−0.3 to V_{DD} + 0.3 V
Ports 4-6	V_{DD} − 40 to V_{DD} + 0.3 V
Output voltage, V_O	
Except ports 3-6	−0.3 to V_{DD} + 0.3 V
Ports 3-6	V_{DD} − 40 to V_{DD} + 0.3 V
Output current, high, I_{OH}	
Single port, one pin except ports 3-6	−17 mA
Single port, one pin ports 3-6	−30 mA
All port pins	−150 mA
Output current, low, I_{OL}	
One pin	17 mA
All port pins	50 mA

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_I			15	pF	
Output capacitance	C_O			15	pF	Except port 3
	C_O			35	pF	Port 3
I/O capacitance	C_{IO}			15	pF	Except ports 4-6
	C_{IO}			35	pF	Ports 4-6

3

DC Characteristics

T_A = −10 to +70°C, V_{DD} = 2.7 to 5.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CL1, X1, ports 4-6
	V_{IH2}	V_{DD} − 0.5		V_{DD}	V	CL1, X1
	V_{IH3}	0.7 V_{DD}		V_{DD}	V	Ports 4-6; V_{DD} = 4.5 to 5.5 V
	V_{IH3}	V_{DD} − 0.5		V_{DD}	V	Ports 4-6; V_{DD} = 3 to 4.5 V
	V_{IH3}	2.5		V_{DD}	V	Ports 4-6; V_{DD} = 2.7 to 3 V
	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} + 0.2	V	RESET, data retention mode
Input voltage, low	V_{IL1}	0		0.3 V_{DD}	V	Except CL1, X1, ports 4-6
	V_{IL2}	0		0.5	V	CL1, X1
	V_{IL3}	V_{DD} − 35		0.3 V_{DD}	V	Ports 4-6
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	Except ports 3,6; I_{OH} = 1.0 mA, V_{DD} = 4.5 to 5.5 V
	V_{OH}	V_{DD} − 2.0			V	Ports 3, 6; I_{OH} = −8.0 mA; V_{DD} = 4.5 to 5.5 V
	V_{OH}	V_{DD} − 0.5			V	I_{OH} = −100 μA; V_{DD} = 2.7 to 5.5 V
Output voltage, low	V_{OL}			0.4	V	Except ports 3, 6; I_{OL} = 1.6 mA, V_{DD} = 4.5 to 5.5 V
	V_{OL}			0.5	V	Except ports 3, 6; I_{OL} = 400 μA; V_{DD} = 2.7 to 5.5 V
Input leakage current, high	I_{LIH1}			3	μA	Except CL1, X1, ports 4-6; $V_I = V_{DD}$
	I_{LIH2}			10	μA	CL1, X1; $V_I = V_{DD}$
	I_{LIH3}			60	μA	Ports 4-6; $V_I = V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	Except CL1, X1, ports 4-6; V_I = 0 V
	I_{LIL2}			−10	μA	CL1, X1; V_I = 0V
	I_{LIL3}			−30	μA	Ports 4-6; $V_I = V_{DD}$ − 35 V
Output leakage current, high	I_{LOH1}			3	μA	V_O == V_{DD} Except ports 4-6
	I_{LOH2}			30	μA	Ports 4-6; $V_O = V_{DD}$
Output leakage current, low	I_{LOL1}			−3	μA	V_O = 0 V
	I_{LOL2}			−30	μA	Ports 3-6; $V_O = V_{DD}$ − 35 V
Supply voltage	V_{DDDR}	2.0			V	Data retention mode
Supply current	I_{DD1}		300	900	μA	Normal operation, V_{DD} = 5 V ±10%; R = 82 kΩ ±2%, C = 33 pF ±5%
	I_{DD1}		70	300	μA	Normal operation, V_{DD} = 3 V ±10%; R = 160 kΩ ±2%, C = 33 pF ±5%
	I_{DD2}		1	20	μA	Stop mode, V_{DD} = 5 V ±10% (1)
	I_{DD2}		0.3	10	μA	Stop mode, V_{DD} = 3 V ±10% (1)
	I_{DDDR}		0.3	10	μA	Data retention mode V_{DDDR} = 2.0 V

Note:

(1) X1 = 0 V; ports 4-6 output disabled or low level input.

AC Characteristics

$T_A = -10$ to 70°C, $V_{DD} = 2.7$ to 5.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock frequency	f_{CC}	150	200	240	kHz	CL1, CL2, RC clock, R = 82 kΩ ±2%; C = 33 pF ±5% V_{DD} = 5 V ±10%, $\lvert \Delta C/°C \rvert \leq$ 60 ppm
	f_{CC}	75	100	120	kHz	CL1, CL2, RC clock, R = 160 kΩ ±2%; C = 33 pF ± 5% V_{DD} = 3 V ±10%, $\lvert \Delta C/°C \rvert \leq$ 60 ppm
	f_{CC}	75		135	kHz	CL1, CL2, RC clock, R = 160 kΩ ±2%; C = 33 pF ±5% $\lvert \Delta C/°C \rvert \leq$ 60 ppm
	f_C	10		410	kHz	CL1, external clock, 50% duty, V_{DD} = 4.5 to 5.5 V
	f_C	10		125	kHz	CL1, external clock, 50% duty, V_{DD} = 2.7 V
System clock rise and fall times	t_{CR}, t_{CF}			0.2	μs	CL1, external clock
System clock pulse width	t_{CH}, t_{CL}	1.1		50	μs	CL1, external clock, V_{DD} = 4.5 to 5.5 V
	t_{CH}, t_{CL}	3.5		50	μs	CL1, external clock, V_{DD} = 2.7 V
Counter clock frequency	f_{XX}	25	32	50	kHz	X1, X2, crystal oscillator
	f_X	0		410	kHz	X1, external pulse input 50% duty, V_{DD} = 4.5 to 6.0 V
	f_X	0		135	kHz	X1, external pulse input 50% duty, V_{DD} = 2.7 V
Counter clock rise and fall times	t_{XR}, t_{XF}			0.2	μs	X1, external pulse input
Counter clock pulse width	t_{XH}, t_{XL}	1.1			μs	X1, external pulse input, V_{DD} = 4.5 to 5.5 V
	t_{XH}, t_{XL}	3.5			μs	X1, external pulse input, V_{DD} = 2.7 V
Port 1 output setup time to $\overline{PSTB}$ ↑	t_{PST}	(1)			μs	V_{DD} = 4.5 to 5.5 V
	t_{PST}	(2)			μs	
Port 1 output hold time from $\overline{PSTB}$ high	t_{STP}	0.1			μs	V_{DD} = 4.5 to 5.5 V
	t_{STP}	0.1			μs	
$\overline{PSTB}$ low pulse width	t_{STL}	(1)			μs	V_{DD} = 4.5 to 5.5 V
	t_{STL}	(2)			μs	
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	$\overline{SCK}$ as input, V_{DD} = 4.5 to 5.5 V
	t_{KCY}	5.0			μs	$\overline{SCK}$ as output, V_{DD} = 4.5 to 5.5 V
	t_{KCY}	7.0			μs	$\overline{SCK}$ as input
	t_{KCY}	14.0			μs	$\overline{SCK}$ as output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	1.3			μs	$\overline{SCK}$ as input, V_{DD} = 4.5 to 5.5 V
	t_{KH}, t_{KL}	2.2			μs	$\overline{SCK}$ as output, V_{DD} = 4.5 to 5.5 V
	t_{KH}, t_{KL}	3.3			μs	$\overline{SCK}$ as input
	t_{KH}, t_{KL}	6.5			μs	$\overline{SCK}$ as output

AC Characteristics (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
SI setup time to $\overline{SCK}$ high	t_{SIK}	0.3			μs	
SI hold time after $\overline{SCK}$ high	t_{KSI}	0.45			μs	
SO delay time after $\overline{SCK}$ low	t_{SKO}			0.85	μs	V_{DD} = 4.5 to 6.0 V
	t_{SKO}			1.2	μs	
INT0 pulse width	t_{I0H}	10			μs	
	t_{I0L}	10			μs	
INT1 pulse width	t_{I1H}	(3)			μs	
	t_{I1L}	(3)			μs	
RESET pulse width	t_{RSH}	10			μs	
	t_{RSL}	10			μs	
RESET high set up time	t_{SRS}	0			ns	
RESET high hold time	t_{HRS}	0			ns	

Note:

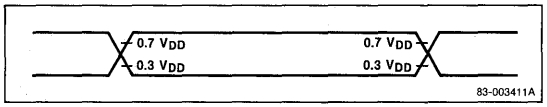
(1) $f_{CC}/2 - 0.8$ or $f_C/2 - 0.8$

(2) $f_{CC}/2 - 0.3$ or $f_C/2 - 0.2$

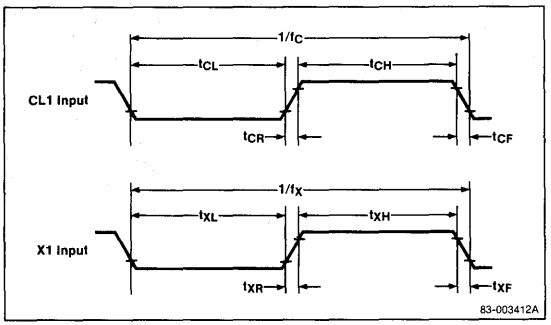
(3) $2/f_{CC}$ or $2/f_C$

Timing Waveforms

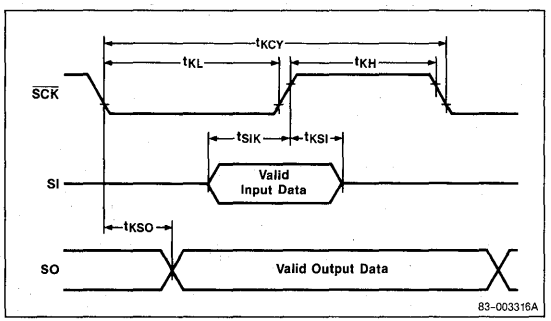
Timing Test Points



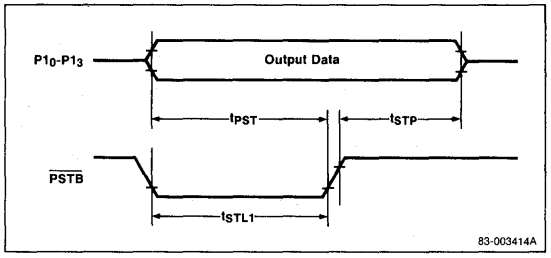
Clocks



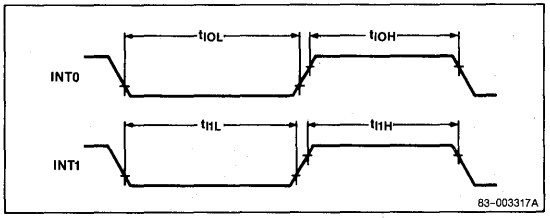
Serial Interface



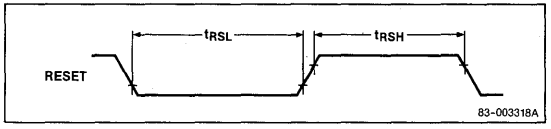
Output Strobe



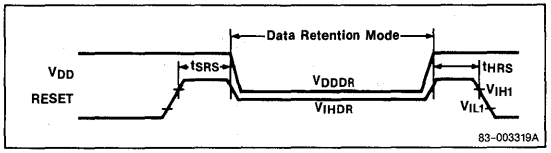
External Interrupts



RESET



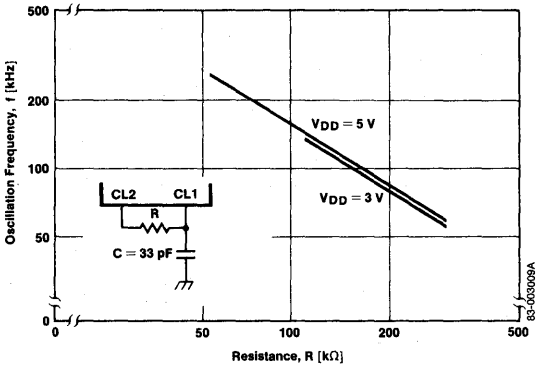
Data Retention Mode



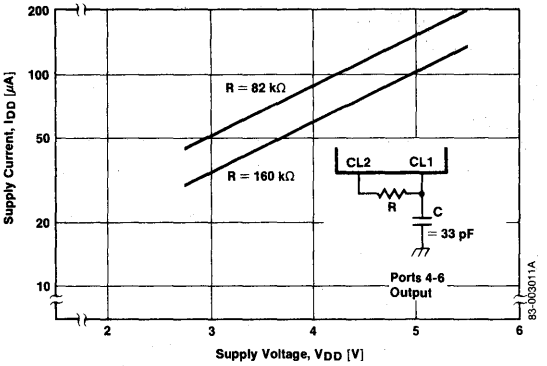
3

Operating Characteristics

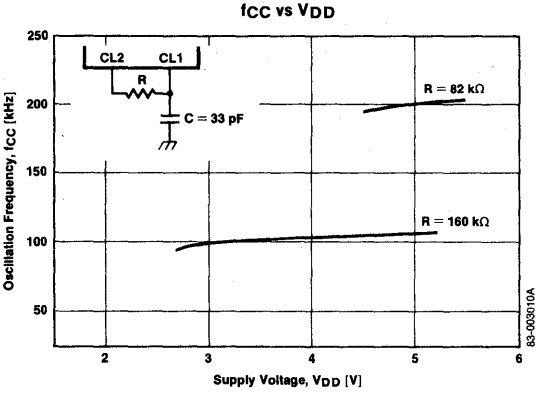
f vs R



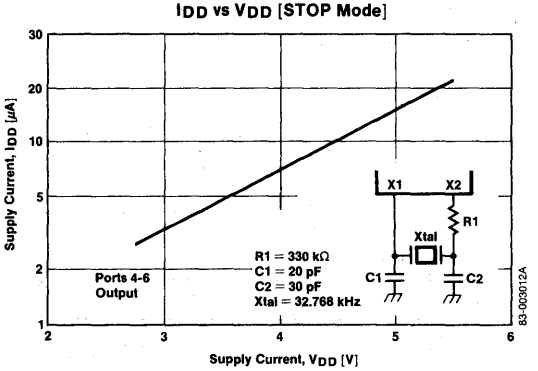
IDD vs VDD [HALT Mode]



fCC vs VDD



IDD vs VDD [STOP Mode]



NEC
NEC Electronics Inc.

μPD7514
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH LCD CONTROLLER/DRIVER

Description

The μPD7514 is a 4-bit single-chip microcomputer with a 4-bit ALU, a 4K × 8-bit program memory (ROM), a 256 × 4-bit data memory (RAM), an 8-bit serial interface, a programmable 8-bit timer/event counter, an LCD controller/driver, and 31 general purpose I/O lines.

The LCD controller/driver supervises all of the timing required by 32 segment drivers and 4 common drivers, for biplexed/triplexed LCD (1/2 bias method) or triplexed/quadriplexed LCD (1/3 bias method).

The instruction set includes transfer and increment/decrement instructions to directly address memory, memory bit manipulation instructions, test instructions for bit test and data comparison, memory reference instructions with automatic register increment/decrement functions, table look-up instructions, load instructions with a string effect, and multi-branch instructions.

The μPD7514 allows the organization of any system with the least additional circuitry. It is suited for the following applications:

- Telephones
- Personal radio equipment
- Automobile equipment (electric)
- High-grade electronic calculators
- Electronic games
- VCRs

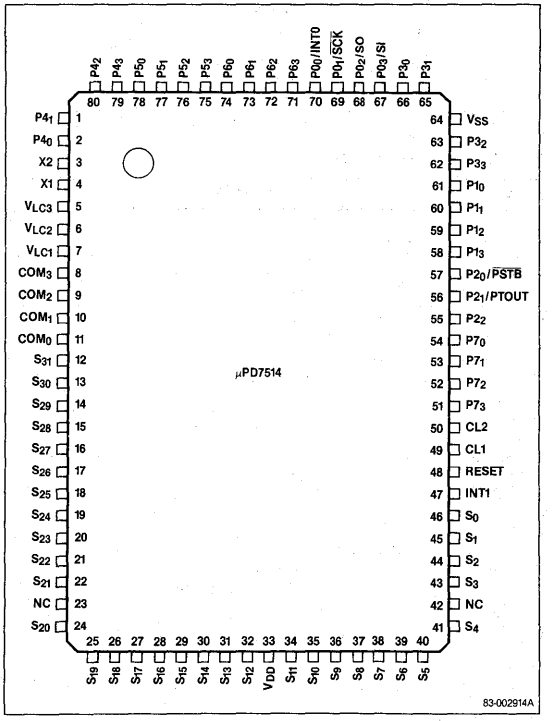
Features

- ☐ 92 powerful instructions
- ☐ Instruction cycle 5 μs at 400 kHz, 5 V
- ☐ Interrupts
  - 2 external: INT0, INT1
  - 2 internal: INTT (timer/event counter)
    INTS (serial interface)
- ☐ Programmable 8-bit timer/event counter
  - Time base count operation
  - External event count operation
- ☐ 8-bit serial interface (three serial clocks)
- ☐ LCD controller/driver
  - Static method
  - Biplexed/triplexed LCD (1/2 bias method)
  - Triplexed/quadriplexed LCD (1/3 bias method)
  - Common outputs (strobe): 4 lines (COM_0–COM_3)
  - Segment outputs (data): 32 lines (S_0–S_{31})
- ☐ Standby operation
  - Stop and halt modes
- ☐ I/O ports
  - 4-bit input port ($P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI)
  - Strobed 4-bit I/O port ($P1_0$–$P1_3$)
  - 3-bit output port ($P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$)
  - 4-bit output port ($P3_0$–$P3_3$)
  - 4-bit I/O ports ($P4_0$–$P4_3$, $P5_0$–$P5_3$, $P6_0$–$P6_3$, $P7_0$–$P7_3$)
- ☐ On-chip RC oscillator for system clock
- ☐ Crystal oscillator input pins
- ☐ CMOS technology
- ☐ Low power consumption
- ☐ Single power supply (2.7 V to 6.0 V)

Ordering Information

Part No.	Package Type	Max Frequency of Operation
μPD7514G-12	80-pin plastic miniflat	500 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 2, 79, 80	$P4_0$-$P4_3$	I/O port 4
3, 4	X1, X2	Crystal clock
5-7	V_{LC1}-V_{LC3}	LCD bias voltage input
8-11	COM_0-COM_3	LCD common output
12-22, 24-32, 34-41, 43-46	S_0-S_{31}	LCD segment output
33	V_{DD}	Power supply positive
47	INT1	External interrupt input
48	RESET	Reset input
49, 50	CL1, CL2	System clock
51-54	$P7_0$-$P7_3$	I/O port 7
55 56 57	$P2_2$ $P2_1$/PTOUT $P2_0$/$\overline{PSTB}$	3-bit output port 2. PTOUT is the timer F/F output. $\overline{PSTB}$ is the strobe output.
58-61	$P1_0$-$P1_3$	I/O port 1
62, 63, 65, 66	$P3_0$-$P3_3$	I/O port 3
64	VSS	Ground
67 68 69 70	$P0_3$/SI $P0_2$/$\overline{SO}$ $P0_1$/$\overline{SCK}$ $P0_0$/INT0	4-bit input port 0. Serial input. Serial output. Serial clock I/O. Interrupt request input.
71-74	$P6_0$-$P6_3$	I/O port 6
75-78	$P5_0$-$P5_3$	I/O port 5

Status of Unused Pins

Name	Pin Connection
CL2	Open
X1	V_{SS}
X2	Open
INT1 $P0_0$/INT0	V_{SS}
$P0_1$/$\overline{SCK}$ $P0_2$/SO $P0_3$/SI $P1_0$-$P1_3$	V_{SS} or V_{DD}
$P2_0$/$\overline{PSTB}$ $P2_1$/PTOUT $P2_2$ $P3_0$-$P3_3$	Open
$P4_0$-$P4_3$ $P5_0$-$P5_3$ $P6_0$-$P6_3$ $P7_0$-$P7_3$	Input mode: V_{SS} or V_{DD} Output mode: Open
S_0-S_{31} COM_0-COM_3 V_{LC1}-V_{LC3}	Open

Pin Functions

$P0_0$-$P0_3$ (Port 0)

This is the 4-bit input port 0. The pins also operate as the interrupt input (INT0/$P0_0$), serial clock I/O ($\overline{SCK}$/$P0_1$), and serial data output (SO/$P0_2$) and input (SI/$P0_3$).

$P1_0$-$P1_3$ (Port 1)

This is the 4-bit I/O port 1. Data on these lines is loaded into the accumulator by execution of a port input instruction (IP, IP1, IPL). The contents of the accumulator are output by the execution of a port output instruction (OP, OPL). Port 1 does not have an output latch. When a port output instruction is executed, the strobe signal, which is used for latching output data externally, is automatically output from $\overline{PSTB}$. The $\overline{PSTB}$ signal is suitable for data output to memory or peripheral circuits requiring write strobe signals. Port 1 is usually held high impedance, and is driven for output with a port output instruction.

$P2_0$-$P2_2$ (Port 2)

This is the three-state 3-bit latched output port 2. Following RESET, these pins become high impedance.

When port 1 is outputting data, $P2_0$ operates as the write strobe output ($P2_0$/$\overline{PSTB}$). $P2_1$ is the output ($P2_1$/PTOUT) for the timer flip-flop signal (TOUT).

$P3_0$-$P3_3$ (Port 3)

This is the 4-bit latched output port 3. On RESET, the contents of the output latches become undefined and the output goes high impedance.

$P4_0$-$P4_3$ (Port 4), $P5_0$-$P5_3$ (Port 5)

Ports 4 and 5 are both 4-bit latched I/O ports. Ports 5 and 4 can be treated as a pair, and can input or output 8-bit data (by an IP54 or OP54 instruction) between the accumulator and memory (addressed by the HL register).

A RESET or input instruction will place these ports in input mode (high impedance). On RESET, the output latch contents become undefined.

If data is input to an I/O port just after changing it from output to input mode, data on the line at the execution of the first input instruction may be unstable. Accordingly, the first input data just after the modification should be ignored. Executing the input instruction again will insure the data is stable.

$P6_0$-$P6_3$ (Port 6)

This is the 4-bit latched I/O port 6. Each line can be set as an input or output using the port 6 mode register (PM_3-PM_0). Port 6 performs data I/O to and from the accumulator in 4-bit units. An output instruction will cause the output latches to latch the contents of the accumulator. Then the contents of the output latch at the bit position that the PMR designates as being in the output mode are output from the pins via the output buffers. The other pins are high impedance (input).

$P7_0$-$P7_3$ (Port 7)

This is the 4-bit latched I/O port 7. An input instruction reads port data into the accumulator. An output instruction latches and outputs the accumulator contents. A RESET or input instruction will place port 7 in input mode (high impedance).

INT0 (Interrupt 0)

This input is the rising-edge-triggered external interrupt. It has a Schmidt-trigger input in order to decrease noise. Setting bit 3 of the shift mode register (SM_3) low level selects INTS; setting it high selects INT0. INT0 can be used in both stop and halt modes.

INT1 (Interrupt 1)

INT1 is the rising-edge-triggered external interrupt input.

X1, X2 (Crystal Clock)

X1 and X2 are the crystal connection pins for the count clock generator. An external clock may be input to X1 directly, in which case X2 must be open.

CL1, CL2 (System Clock)

CL1 and CL2 are the resistor and capacitor connection pins for the system clock generator. An external clock may be input to CL1 directly, in which case CL2 must be open.

S_0-S_{31} (Segment)

These segment signal outputs directly drive the LCD segment lines. They are used for biplexed/triplexed LCD (1/2 bias method) and triplexed/quadriplexed LCD (1/3 bias method).

COM_0-COM_3 (Common)

These outputs directly drive common (backplane) LCD lines via the following strobe signals:

- 1/2 bias method: biplexed (COM_0, COM_1), triplexed (COM_0-COM_2)
- 1/3 bias method: triplexed (COM_0-COM_2), quadriplexed (COM_0-COM_3)

V_{LC1}, V_{LC2}, V_{LC3} (LCD Power Supply)

These pins are the LCD bias voltage supply. Based on applied voltages to these pins, the on-chip LCD controller/driver generates segment and common signals to the LCD. The bias voltage configuration for the 1/2 bias method is different from that for the 1/3 bias method.

RESET

A high level input to this pin resets the μPD7514.

VDD

Positive power supply.

VSS

Ground.

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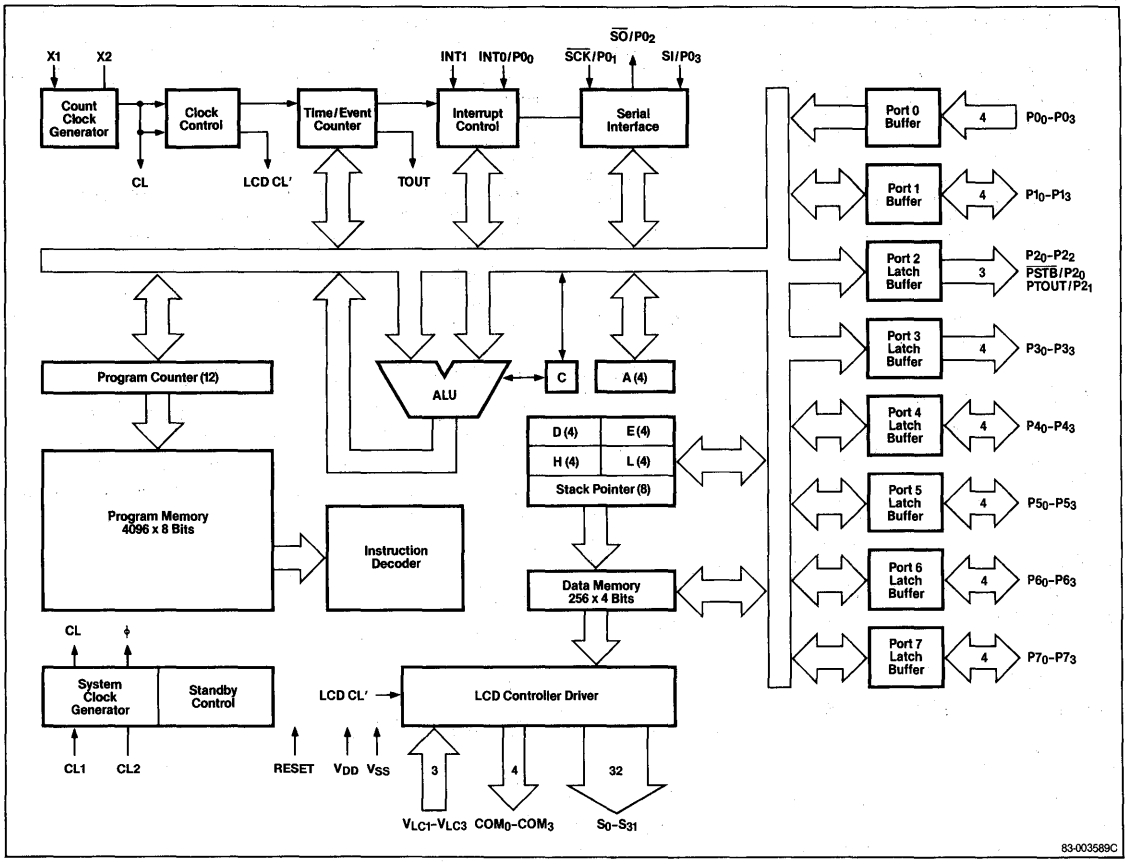
Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	−0.3 V to V_{DD} +0.3 V
Output current high, I_{OH}	
Per pin	−5 mA
Total, all output ports	−50 mA
Output current low, I_{OL}	
Per pin	15 mA
Total, Ports 0, 4, 5, 6, $P3_0$, $P3_1$	40 mA
Total, Ports 1, 2, 7, $P3_2$, $P3_3$	40 mA
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = -10°C$ to +70°C, $V_{DD} = 2.7$ V to 6 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except X1, CL1, RES, INT0, INT1, SI, $\overline{SCK}$
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	RES, INT0, INT1, SI, $\overline{SCK}$
	V_{IH3}	$V_{DD}-0.5$		V_{DD}	V	X1, CL1
Input voltage low	V_{IL1}	0		0.3 V_{DD}	V	Except X1, CL1, RES, INT0, INT1, SI, $\overline{SCK}$
	V_{IL2}	0		0.2 V_{DD}	V	RES, INT0, INT1, SI, $\overline{SCK}$
	V_{IL3}	0		0.5	V	X1, CL1
Output voltage high	V_{OH}	$V_{DD}-1.0$			V	V_{DD} = 4.5 to 6.0 V; $I_{OH} = -1.0$ mA
		$V_{DD}-0.5$			V	$I_{OH} = -100$ μA
Output voltage low	V_{OL}			0.4	V	V_{DD} = 4.5 to 6.0 V; I_{OL} = 1.6 mA
				0.5	V	I_{OL} = 400 μA
Input leakage current high	I_{LIH1}			3	μA	$V_I = V_{DD}$ except X1, CL1
	I_{LIH2}			10	μA	$V_I = V_{DD}$; X1, CL1
Input leakage current low	I_{LIL1}			−3	μA	V_I = 0 V except X1, CL1
	I_{LIL2}			−10	μA	X1, CL1
Output leakage current high / low	I_{LOH}			3	μA	$V_O = V_{DD}$
	I_{LOL}			−3	μA	V_O = 0 V

DC Characteristics (cont)

$T_A = -10°C$ to +70°C, $V_{DD} = 2.7$ V to 6 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Common output impedance	R_{COM}		3	5	kΩ	V_{DD} = 4.5 to 6.0 V
			5	15	kΩ	
Segment output impedance	R_S		15	20	kΩ	V_{DD} = 4.5 to 6.0 V
			20	60	kΩ	
Supply current	I_{DD1}		600	1800	μA	Operating mode V_{DD} = 5 V ±10%; R = 39 kΩ ±2%; C = 33 pF ±5%
			70	210	μA	Operating mode V_{DD} = 3 V ±10%; R = 160 kΩ ±2%; C = 33 pF ±5%
	I_{DD2}		300	900	μA	Halt mode X1 = 0 V; V_{DD} = 5 V ±10%; R = 39 kΩ ±2%; C = 33 pF ±5%
			35	100	μA	Halt mode X1 = 0 V; V_{DD} = 3 V ±10%; R = 160 kΩ ±2%; C = 33 pF ±5%
	I_{DD3}		1.0	20	μA	Stop mode X1 = 0 V; V_{DD} = 5 V ±10%
			0.3	10	μA	Stop mode X1 = 0 V; V_{DD} = 3 V ±10%

Capacitance

$T_A = 25°C$; $V_{DD} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	(Note 1)
Output capacitance	C_O			15	pF	(Note 1)
I/O capacitance	C_{IO}			15	pF	(Note 1)

Note:
(1) f_C = 1 MHz. Return unmeasured pins to 0 V.

3

AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = 3\,V$ to $6\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation (CL1, CL2)	f_{cc}	300	400	500	kHz	C = 33 pF ±5%, |ΔC/°C| ≤ 60 ppm R = 39 kΩ ±2%, V_{DD} = 5 V ±10%
		75	100	120	kHz	C = 33 pF ±5%, |ΔC/°C| ≤ 60 ppm R = 160 kΩ ±2%, V_{DD} = 3 V ±10%
System clock input frequency (CL1)	f_c	10		510	kHz	V_{DD} = 4.5 V to 6.0 V, Duty = 50%
		10		150	kHz	Duty = 50%
CL1 input rise time	t_{CR}			0.2	μs	
CL1 input fall time	t_{CF}			0.2	μs	
CL1 input pulse width high	t_{CH}	0.9		50	μs	V_{DD} = 4.5 V to 6.0 V
		3.2		50	μs	
CL1 input pulse width low	t_{CL}	0.9		50	μs	V_{DD} = 4.5 V to 6.0 V
		3.2		50	μs	
Count clock oscillation frequency (X1, X2)	f_{xx}	25	32	50	kHz	C1 = 20 pF C2 = 30 pF R = 220 kΩ (Note 1)
Count clock input frequency (X1)	f_x	0		500	kHz	V_{DD} = 4.5 to 6.0 V, Duty = 50%
		0		150	kHz	
X1 input rise time	t_{XR}			0.2	μs	
X1 input fall time	t_{XF}			0.2	μs	
X1 input pulse width high	t_{XH}	0.9			μs	V_{DD} = 4.5 V to 6.0 V
		3.2			μs	V_{DD} = 2.7 V
X1 input pulse width low	t_{XL}	0.9			μs	V_{DD} = 4.5 V to 6.0 V
		3.2			μs	V_{DD} = 2.7 V
Port 1 output set-up time to $\overline{PSTB}$↑	t_{PST}	(2)			μs	V_{DD} = 4.5 V to 6.0 V
		(3)			μs	
Port 1 output hold after $\overline{PSTB}$↑	t_{STP}	0.1			μs	V_{DD} = 4.5 V to 6.0 V
		0.1			μs	

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{PSTB}$ pulse width low	t_{STL}	(2)			ns	V_{DD} = 4.5 V to 6.0 V
		(3)			μs	
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	Input V_{DD} = 4.5 V to 6.0 V
		4.0			μs	Output
		8.0			μs	Input
		13.0			μs	Output
$\overline{SCK}$ pulse width high	t_{KH}	1.3			μs	Input V_{DD} = 4.5 V to 6.0 V
		1.8			μs	Output
		3.8			μs	Input
		6.3			μs	Output
$\overline{SCK}$ pulse width low	t_{KL}	1.3			μs	Input V_{DD} = 4.5 V to 6.0 V
		1.8			μs	Output
		3.8			μs	Input
		6.3			μs	Output
SI set-up time (to SCK↑)	t_{SIK}	300			ns	
SI hold time (after SCK↑)	t_{KSI}	450			ns	
SO output delay time (after SCK↓)	t_{KSO}			850	ns	V_{DD} = 4.5 V to 6.0 V
				1200	ns	
INT0 pulse width high	t_{I0H}	10			μs	
INT0 pulse width low	t_{I0L}	10			μs	
INT1 pulse width high	t_{I1H}	(4)			μs	
INT1 pulse width low	t_{I1L}	(4)			μs	
RESET pulse width high	t_{RSH}	10			μs	
RESET pulse width low	t_{RSL}	10			μs	

Note:

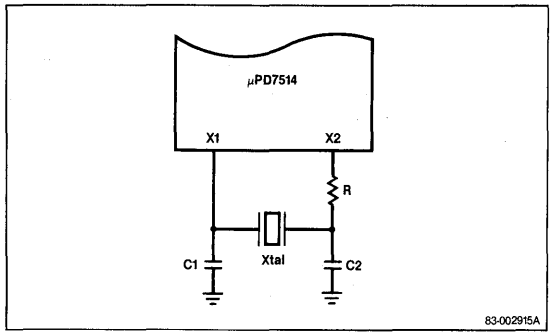
(1) See recommended clock circuit on next page.

(2) $1/2\,f_{cc} - 0.8$ or $1/2\,f_c - 0.8$

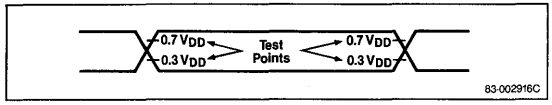
(3) $1/2\,f_{cc} - 2.0$ or $1/2\,f_c - 2.0$

(4) $2/f_{cc}$ or $2/f_c$

Recommended Clock Circuit



AC Timing Test Points



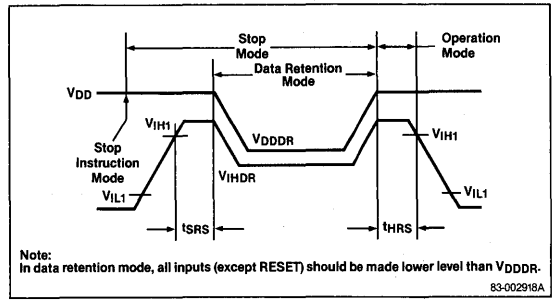
Data Retention Characteristics

$T_A = -10°C$ to $+70°C$

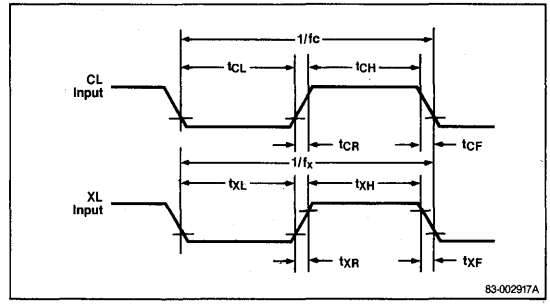
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0			V	
Data retention supply current	I_{DDDR}		0.3	10	μA	$V_{DDDR} = 2V$
Data retention RESET input voltage high	V_{IHDR}	0.9 × V_{DDDR}		V_{DDDR} +0.2	V	
RESET set-up time	t_{SRS}	0			ns	
RESET hold time	t_{HRS}	0			ns	

Timing Waveforms

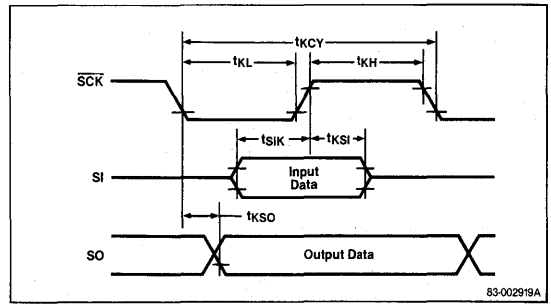
Data Retention Mode Timing



Clock Timing



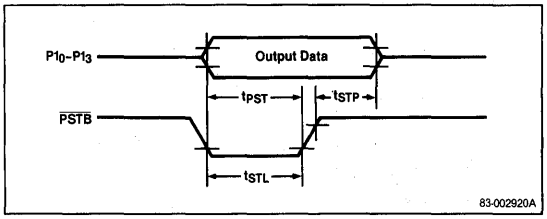
Serial Transfer Timing



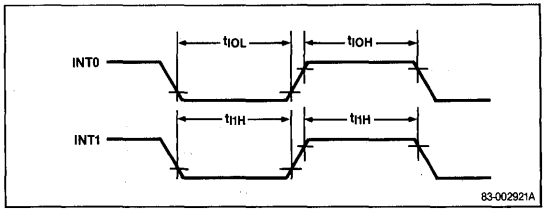
3

Timing Waveforms (cont)

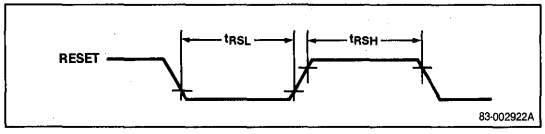
Strobe OutputTiming



Interrupt Input Timing



RESET Input Timing

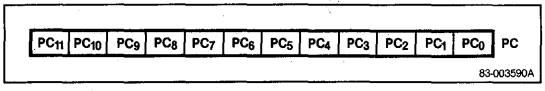


Functional Description

Program Counter (PC)

This 12-bit binary counter, shown in figure 1, holds the address of the current instruction in program memory. When an instruction executes, the PC increments by the number of bytes in the instruction. RESET clears the PC to 0.

Figure 1. Program Counter Structure



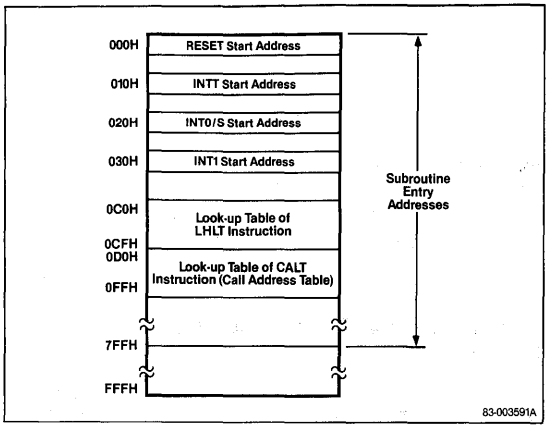
Stack Pointer (SP)

This 8-bit register (SP_7-SP_0) stores the top address of the data memory area used as a LIFO stack. The SP decrements when a call (CALL, CALT) or a push (PSHDE, PSHHL) instruction executes, and at an interrupt generation. It increments when a return (RT, RTS, RTPSW) or POP (POPDE, POPHL) instruction executes.

Program Memory (ROM)

This 4,096-word × 8-bit mask-programmable ROM stores programs and table data and is addressed by the PC. ROM address locations are from 000H to FFFH. Fixed locations are allocated to the RESET and interrupt start addresses, and table areas of the LHLT and CALT instructions. See figure 2.

Figure 2. Program Memory Map

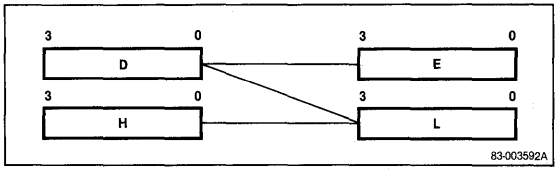


General Purpose Registers

Registers D, E, H, and L operate in units of 4 bits, or they form the 8-bit pair registers DE, DL, and HL for use as a data pointer (D or H is the upper-order 4 bits). See figure 3.

Pair register HL can perform the functions of automatic increment (+1) and automatic decrement (−1) for the L register only. The L register is also used to specify I/O ports and mode registers when the I/O instruction (OPL, IPL) is executed.

Figure 3. General-Purpose Register Configuration



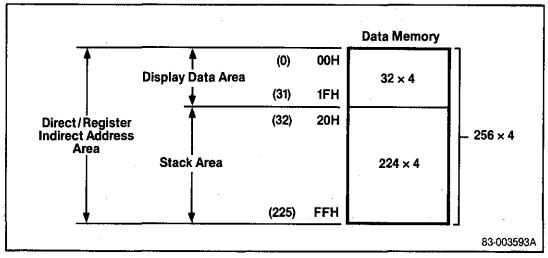
Data Memory (RAM)

This 256-word × 4-bit static RAM stores processing data and display data. It also operates with the accumulator to process data in 8-bit units. There are three types of data memory addressing:

- Direct addressing is made by the second byte of the instruction.
- Register indirect addressing is made indirectly by the contents of the register pair designated by an instruction.
- Stack indirect addressing is made by the contents of the SP.

RAM resides at addresses 00H-FFH. Thirty-two of these locations (00H-1FH) are allocated for the LCD display data area. When display data is written to 00H-1FH, the LCD controller/driver reads it and generates an LCD drive signal. Address locations 00H-1FH cannot be used as stack area. See figure 4.

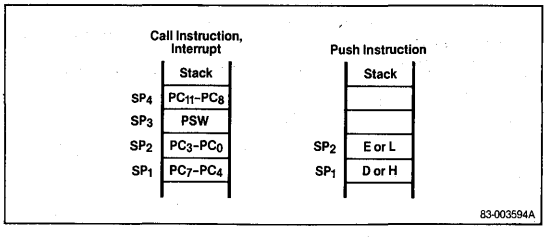
Figure 4. Data Memory Map



Addresses 20H-FFH in data memory can be used as a stack area at execution of a call or return instruction (CALL, CALT, RT, RTS, RTPSW), a push/pop instruction (PSHDE, PSHHL, POPDE, POPHL), or at an interrupt occurrence.

At the execution of a call instruction or an interrupt occurrence, the contents of the PC and PSW are stored in the stack. At the execution of a push instruction, the contents of DE or HL are stored in the stack. The data is stored in the stack as shown in figure 5.

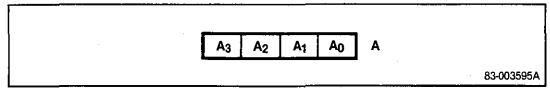
Figure 5. Stack Contents after Call, Interrupt, or Push



Accumulator (A)

The accumulator is a 4-bit register. (See figure 6.) Various arithmetic/logical operations are done mainly by the accumulator. Operating with the data memory addressed by the pair register HL, data processing may be done in 8-bit units (higher-order bits in the accumulator and lower-order bits in the data memory).

Figure 6. Accumulator Configuration



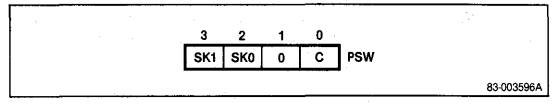
Arithmetic Logic Unit (ALU)

The ALU is a 4-bit arithmetic logic circuit that performs such processes as binary addition, arithmetic/logical operation, comparison, and rotation.

Program Status Word (PSW)

The program status word consists of two skip flags (SK_1, SK_0) and a carry flag (C). (See figure 7.) These are stored in the stack area upon execution of a call instruction (CALL, CALT) or at an interrupt occurrence; they are restored by an RTPSW instruction. At RESET, SK_1 and SK_0 are cleared to 0, and C is undefined.

Figure 7. Structure of Program Status Word



System Clock Generator Circuit

This circuit consists of an RC oscillator circuit and a half-frequency divider circuit, as shown in figure 8. The RC oscillator circuit is controlled by an external resistor (R) and capacitor (C) connected to CL1 and CL2.

An external clock can be input to CL1 without using an RC circuit. CL2 should be left open, in which case the RC oscillator circuit merely operates as an inverted buffer.

In stop mode, the RC oscillator circuit and the half-frequency divider circuit stop, thereby stopping the output of CL and ϕ, respectively. In halt mode, the half-frequency divider circuit stops (ϕ), but CL continues to be supplied.

With an external clock, when the device is in standby mode, the CL1 input clock becomes CL via an inverted buffer; CL continues to be supplied. In this case, both standby modes stop only the half-frequency divider (ϕ).

Figure 8. System Clock Generator Circuits

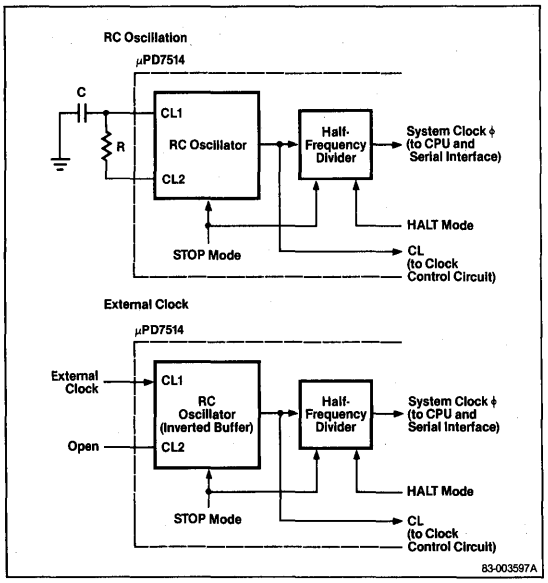
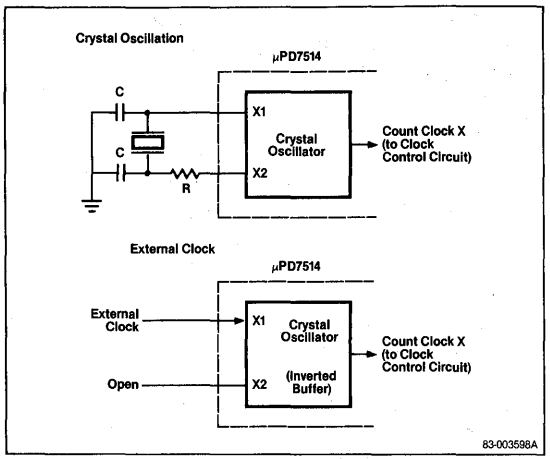


Figure 9. Count Clock Generator Circuits



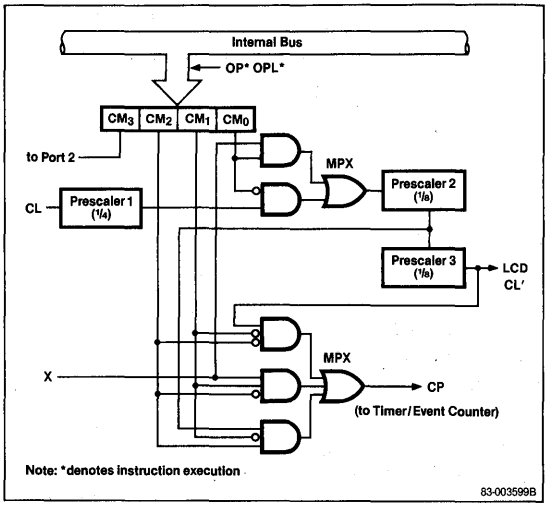
Count Clock Generator Circuit

This crystal oscillator circuit is fed either by the crystal connected to X1 and X2 or by an external clock from X1, in which case it operates as an inverted buffer. Output from this circuit (X) is sent to the clock control circuit to become a count pulse (CP) for the timer/event counter either directly, or after being frequency-divided. The frequency of X equals the crystal oscillation frequency of the X1 external clock. This circuit is unaffected by standby mode. See figure 9.

Clock Control Circuit

The clock control circuit consists of a 4-bit clock mode register (CM_3–CM_0), prescalers 1, 2, 3, and multiplexers. (See figure 10.) The circuit accepts both the system clock generator circuit output (CL) and the count clock generator circuit output (X). The clock mode register selects a clock source and prescaler designation. By so doing, the clock control circuit supplies a count pulse (CP) to the timer/event counter, and the LCD clock source (LCD CL') to the LCD controller/driver.

Figure 10. Clock Control Circuit



A code is sent to the clock mode register by transferring the contents of the accumulator with an OP or OPL instruction.

Bits CM_2–CM_0 specify a clock source and frequency of the timer-out signal. When CM_3 is high, TOUT is output via PTOUT. CM_0 selects a clock source of LCD CL' and a frequency. See table 1.

Table 1. Clock Mode Register

CM_2	CM_1	CM_0	Count Pulse Selection
0	0	0	CL × 1/256
0	0	1	X × 1/64
0	1	0	X
0	1	1	X
1	0	0	CL × 1/32
1	0	1	X × 1/8
1	1	0	Prohibited
1	1	1	Prohibited

CM_3	Output Control of TOUT
0	Output Prohibited
1	TOUT→$P2_1$ / PTOUT

CM_0	LCD CL'
0	CL × 1/256
1	X × 1/64

Timer/Event Counter

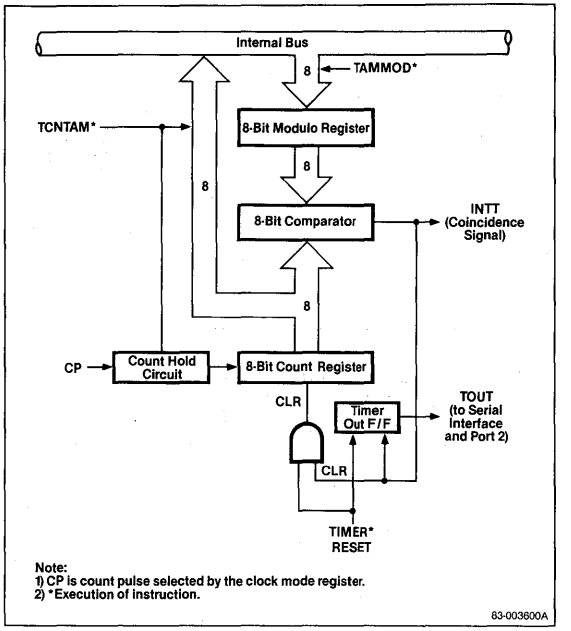
This counter consists of an 8-bit count register, an 8-bit modulo register, an 8-bit comparator, and a timer flip flop (F/F), as shown in figure 12.

The 8-bit register, a binary upcounter that increments at every input of the counter pulse (CP), is cleared to 0 by the execution of a TIMER instruction, RESET input, or a coincidence signal from the comparator.

The 8-bit modulo register determines the count register's maximum count. Its contents are set by the TAMMOD instruction. It is initialized to FFH by RESET.

The 8-bit comparator compares the contents of the count and modulo registers; it outputs the timer interrupt signal (INTT) one CP after they are found to be coincident.

Figure 11. Timer/Event Counter Configuration



Note:
1) CP is count pulse selected by the clock mode register.
2) *Execution of instruction.

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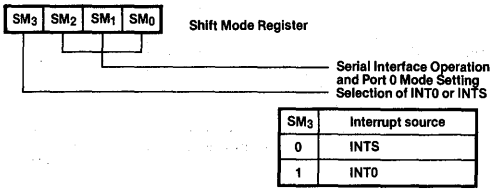
Serial Interface

The serial interface consists of an 8-bit shift register, a 4-bit shift mode register (figure 12) and a 3-bit octal counter, as shown in figure 13. This interface performs serial data I/O, which is controlled by the serial clock ($\overline{SCK}$). At the falling edge of $\overline{SCK}$, the MSB of the shift register (bit 7) is output via the SO line. At the next rising edge of $\overline{SCK}$, the register's contents shift one bit and the data on SI is loaded into the LSB. The 3-bit counter counts each $\overline{SCK}$, generates an internal interrupt (INTS) at every count of 8 clocks (at the end of a 1-byte serial data transfer), and sets the interrupt request flag (INT0/S RQF).

Figure 12. Format of Shift Mode Register



SM_3	Interrupt source
0	INTS
1	INT0

SM_2	SM_1	SM_0	$P0_3$/SI	$P0_2$/SO	$P0_1$/SCK	Serial Operation
0	0	0	Port input	Port input	Port input	Stop
0	1	0	Port input	Port input	To output 0	Stop
0	1	1	Port input	Port input	To output TOUT	Stop
1	0	0	SI input	SO input	$\overline{SCK}$ input	To operate with external clock
1	1	0	SI Input	SO input	$\overline{SCK}$ output (0×8)	To operate with 0
1	1	1	SI input	SO input	$\overline{SCK}$ output (TOUT)	To operate with TOUT

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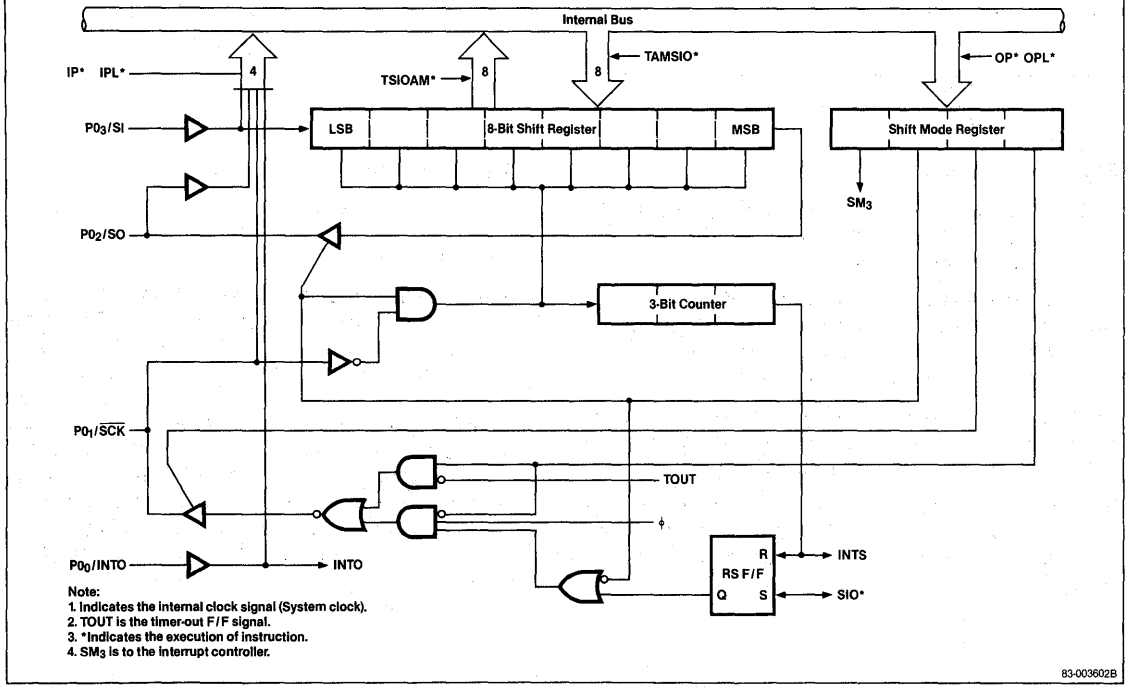
Figure 13. Serial Interface Block Diagram



Note:
1. Indicates the internal clock signal (System clock).
2. TOUT is the timer-out F/F signal.
3. *Indicates the execution of instruction.
4. SM_3 is to the interrupt controller.

83-003602B

LCD Controller/Driver

This controller/driver directly drives an LCD with static, 1/2 bias voltage (biplexed, triplexed) and 1/3 bias voltage (triplexed, quadriplexed) configurations. Thirty-two segment lines (S_0–S_{31}) and 4 common lines (COM_0–COM_3) serve as the LCD driver outputs. See tables 2 and 3, and figure 14.

To supply the proper voltage to the segment and common lines, supply the voltages listed in table 4 to pins V_{LC1}, V_{LC2}, and V_{LC3}. See also figure 15.

Table 2. Maximum Segment Number

Bias	Multiplexing	COM Lines	Maximum Segment Number
1/2	biplexed	COM0, 1	64 (32 Segments × 2 Commons)
1/2	triplexed	COM0, 1, 2	96 (32 Segments × 3 Commons)
1/3	triplexed	COM0, 1, 2	96 (32 Segments × 3 Commons)
1/3	quadriplexed	COM0, 1, 2, 3	128 (32 Segments × 4 Commons)

Note:
In the following cases, LCD driving waveform stops operation and DC potential is applied between LCD electrodes. This will considerably reduce the life span of the LCD.

LCD Clock Source	Primary Causes
CL Channel 0 (System Clock)	1. STOP instruction is executed. 2. External clock is stopped.
X Channel (Count Clock)	1. External clock is stopped.

Table 3. Display Mode Register

					CMO = 0		MCO = 1	
DM_3	DM_2	DM_0	Multiplexing	Bias Voltage	LCD CL	Frame Frequency	LCD CL	Frame Frequency
0	0	0	Quadriplexed	1/3	CL/256	CL/1024	X/164	X256
		1	Triplexed			CL/768		X192
	1	0	Biplexed	1/2	CL/512	CL/1024	X/128	X256
		1	Triplexed			CL/1536		X384
0	0	0	Quadriplexed	1/3	CL/512	CL/2048	X/128	X512
		1	Triplexed			CL/1536		X584
	1	0	Biplexed	1/2	CL/1024	CL/2048	X/256	X1512
		1	Triplexed			CL/3072		X768

DM_1	Display output control	DM_1	Display output control
0	T0 deselect all segments signal	1	To enable display outs

Table 4. LCD Supply Voltage

Pin Name	1/2 Bias	1/3 Bias
V_{LC1}	V_{DD}–(1/2) V_{LCD}	V_{DD}–(1/3) V_{LCD}
V_{LC2}	V_{DD}–(1/2) V_{LCD}	V_{DD}–(2/3) V_{LCD}
V_{LC3}	V_{DD}–V_{LCD}	V_{DD}–V_{LCD}

3

Figure 14. LCD Controller/DriverBlock Diagram

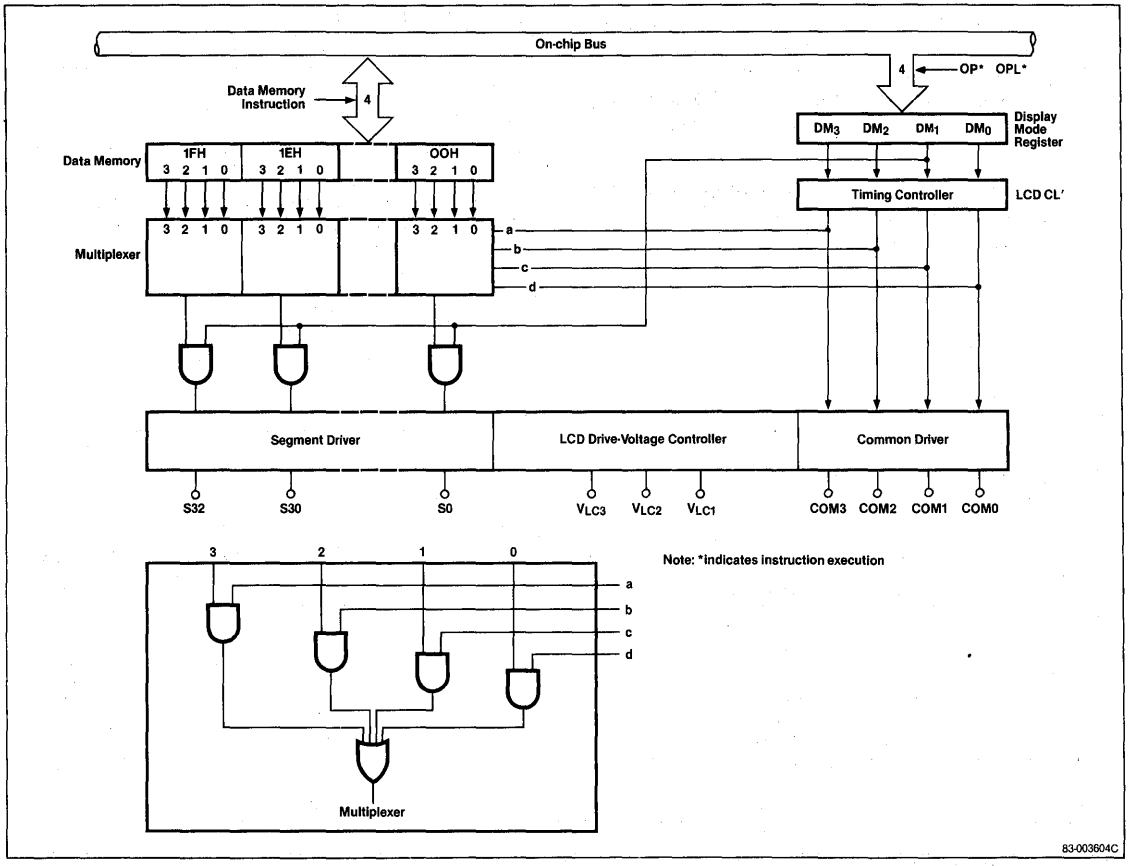
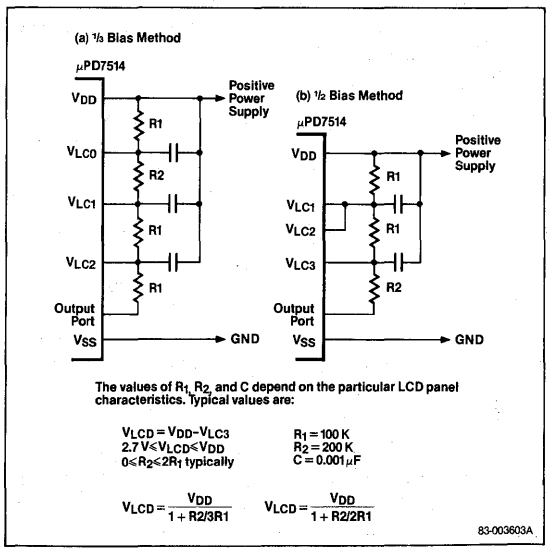


Figure 15. Configuration of LCD Power Supply by Voltage Dividing Method



Interrupt Function

There are two external (INT0, INT1) and two internal (INTT, INTS) interrupts. Interrupt INT0 and pin $P0_0$ share one line; figure 12 shows how to select between these. When INT0 is selected, either INT0 or INTS may be specified. The interrupt process (interrupt address and priority) for INT0 and INTS is the same. See table 5 and figure 16.

Interrupt Enable Register (IE_2-IE_0). This register permits or inhibits individual interrupt requests of INTT, INT0/S and INT1; it allows the interrupt if the respective bit of each interrupt is set to 1, and inhibits the interrupt if 0. See figure 17.

Figure 16. Interrupt Controller Block Diagram

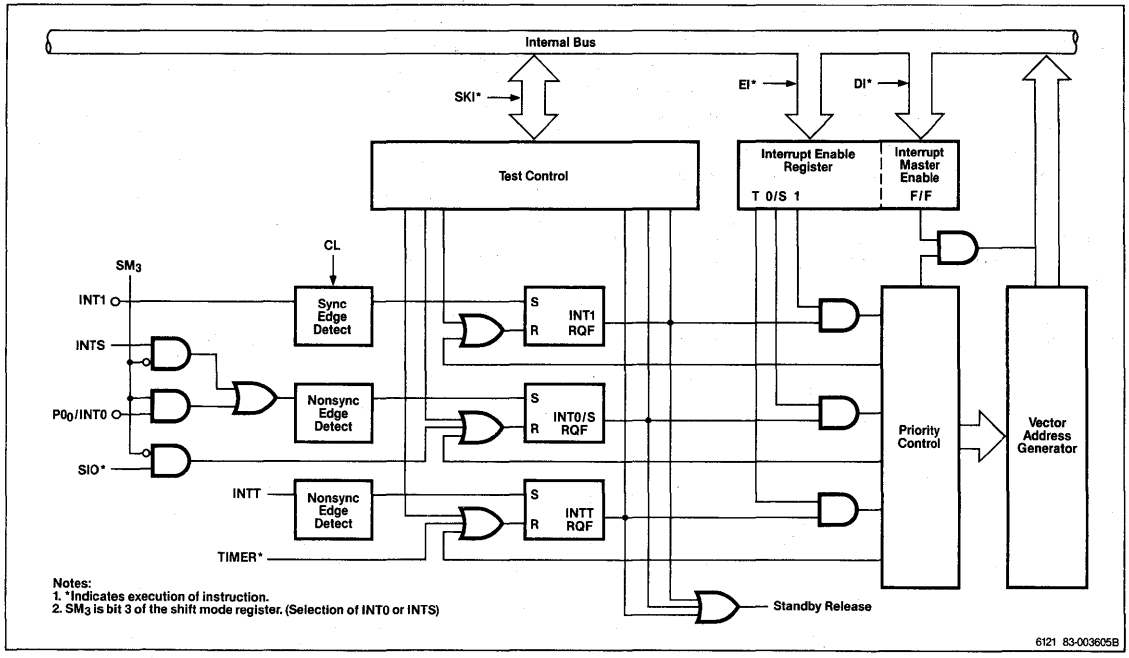
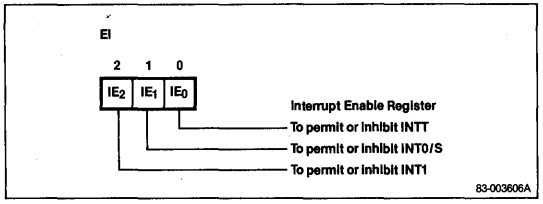


Table 5. Source of Interrupts

Interrupt	Int/Ext	Priority	Interrupt Address
INTT (coincidence signal from timer / event counter)	Int	1	10H (16)
INT0 (interrupt signal from $P0_0$ pin)	Ext	2	20H (32)
INTS (transfer end signal from serial interface)	Int	2	20H (32)
INT1 (interrupt signal from INT1 pin)	Ext	3	30H (48)

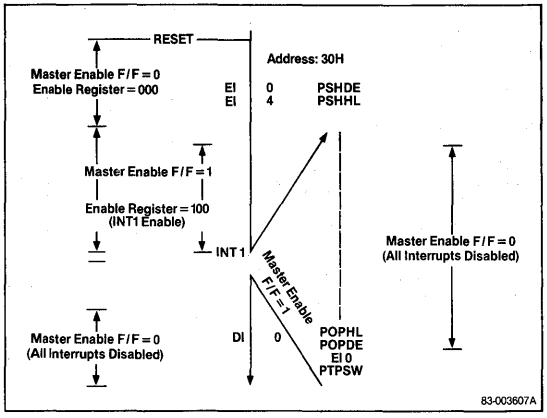
Figure 17. Format of Interrupt Enable Register



Interrupt Master Enable F/F (IME). This F/F permits or inhibits the acceptance of all interrupts (INTT, INT0, INTS, and INT1); after accepting an interrupt, it is reset to inhibit subsequent interrupts. The F/F is set by the EI 0 instruction to permit all interrupts not individually disabled, or it is reset by the DI 0 instruction to inhibit all interrupts. In either case, the interrupt enable register is unaffected.

Typical Interrupts. Figure 18 is an example of the interrupt process for the INT1 interrupt.

Figure 18. Typical Interrupt Process Flow



Standby Function

Two standby modes, stop and halt, are provided to reduce power consumption during a program standby state. The STOP and HALT instructions select these modes.

In standby mode, program execution ceases and the contents of data memory and all internal registers are held. The shift register and timer/event counter still operate.

A RESET or interrupt generation releases standby mode; if an interrupt request flag is set, stop/halt mode cannot be set in spite of the STOP/HALT instruction execution. Consequently, when setting standby mode when there is a possibility of a request flag being set, it is necessary to have the interrupt request flag reset either by processing the interrupt in advance or by executing a SKI instruction.

Differences between stop and halt modes are shown in table 6. The main difference lies in that RC oscillation output (CL) either stops (stop mode), or does not stop (halt mode), when the system clock is being supplied by RC oscillation.

Table 6. Comparing Stop and Halt Modes

Mode	Instruction	CL	0	X	CPU	SIO	CNT	Interrupt used for release
Stop	STOP	X	X	0	X	*	*	INTT, INT0/S
Halt	HALT	0	X	0	X	*	0	INTT, INT0/S, INT1

Note:
0 Operation possible
* Operation possible with a mode selected
X Operation disabled

Reset Function

A high level RESET input initializes the μPD7514. The sequence of events is as follows:

(1) The PC is cleared to 0.

(2) PSW flags SK_1 and SK_0 are cleared to 0.

(3) The timer/event counter as reset as follows:
Count register = 00H
Modulo register = FFH
Timer out F/F = 0

(4) The clock control circuit is reset as follows:
Clock mode register (CM_3–CM_0) is cleared to 0
CP = LCD CL' = CL × 1/256
TOUT is disabled.
Prescalers 1, 2, 3 = 0

(5) Shift mode register (SM_3–SM_0) is cleared to 0.
Serial interface shift operation stops.
Port 0 is placed in input mode (high impedance).
INTS is selected for the interrupt source of INT0/S.

(6) Display mode register (DM_3–DM_0) is cleared to 0.
1/3 bias, quadriplexed
Frame frequency = CL/1024, LCD drive deselected

(7) Interrupt control circuit becomes as follows:
Interrupt request flags = 0
Interrupt master enable F/F = 0
Interrupt enable register = 0
All pending interrupts cancelled.
All interrupts disabled.

(8) Port 6 mode register (PM_3–PM_0) is cleared to 0.

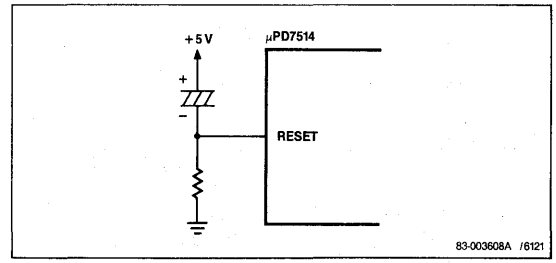
(9) All output buffers of ports 0–7 are turned off, and become high impedance, I/O ports are set to input mode.

(10) The contents of data memory and the following registers are undefined:
Stack pointer (SP)
Accumulator (A)
Carry flag (C)
General-purpose registers (D, E, H, L)
Output latch of each port
Shift register

After RESET, program execution starts from address 00H. The contents of each register must be initialized as needed.

Power-On-Reset Circuit. The simplest example is shown in figure 19.

Figure 19. Power-On-Reset Circuit



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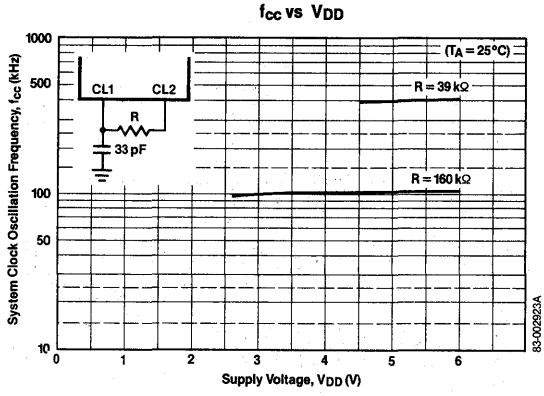
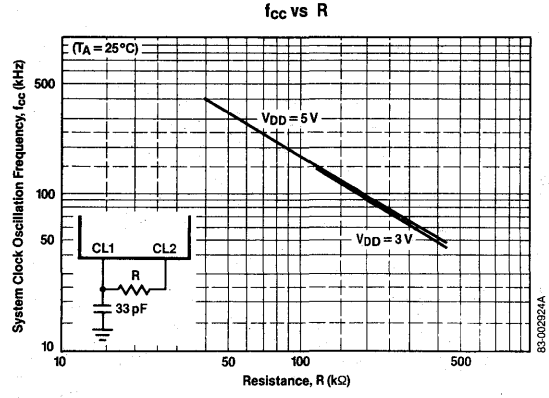
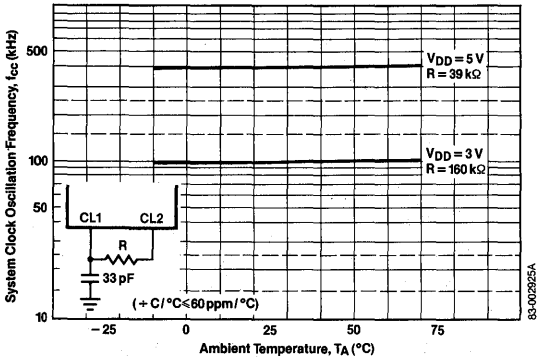
Operating Characteristics



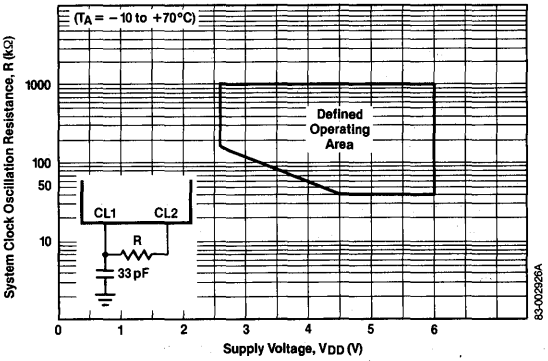


Operating Characteristics (cont)

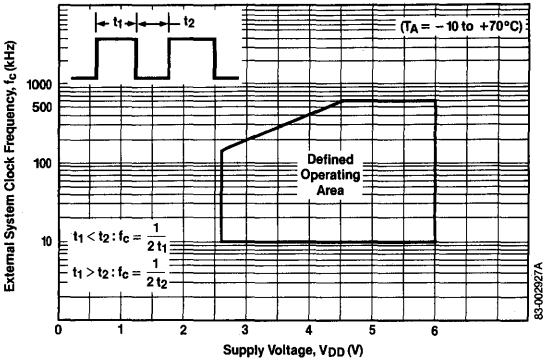
f_{CC} vs T_A



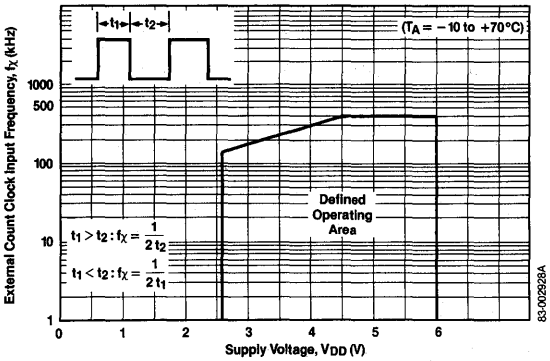
R vs V_{DD}



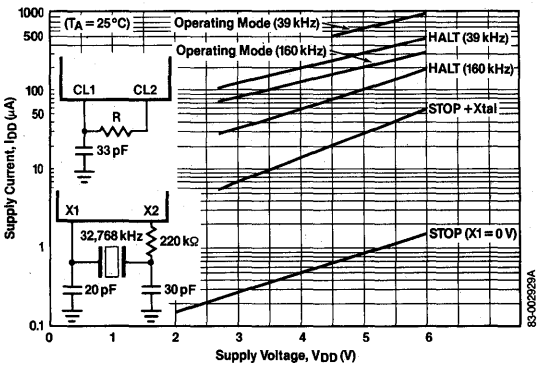
f_C vs V_{DD}



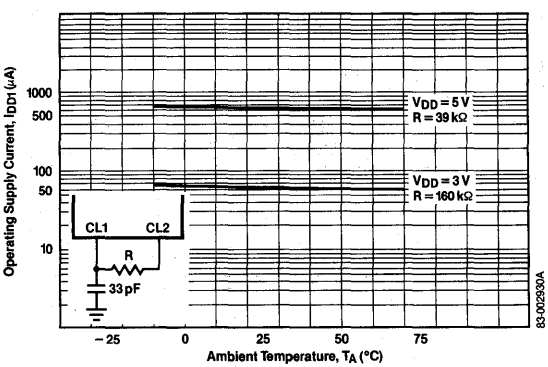
f_X vs V_{DD}



I_{DD} vs V_{DD}

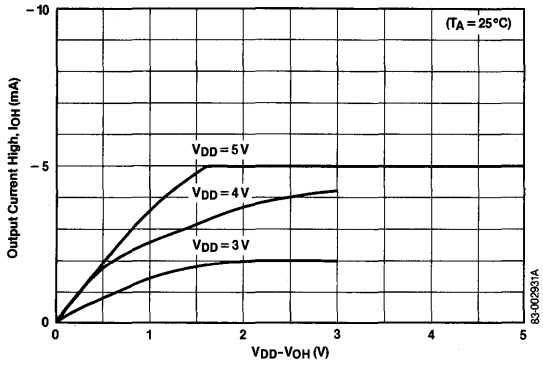


I_{DD1} vs T_A

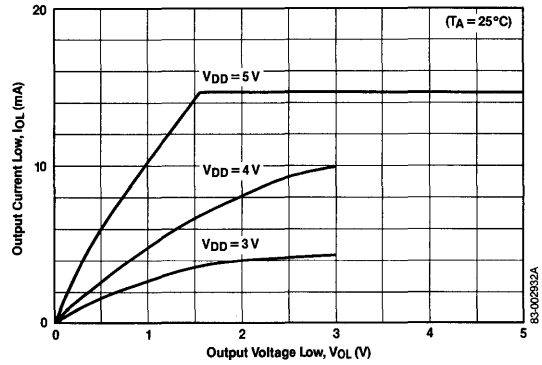


Operating Characteristics (cont)

V_{OH} vs I_{OH}



V_{OL} vs I_{OL}



Differences Between the μPD7514, μPD7508, and μPD7503

The μPD7514 integrates the features of the μPD7508 and the strengthened LCD controller/driver of the μPD7503. Differences are shown in table 7.

Table 7. Difference Between μPD7514, μPD7508, and μPD7503

	μPD7514	μPD7508C/G	μPD7503G
On-chip RAM	256×4	226×4	224×4
Input ports	Port 0 (PO_0–PO_3)	Port 0 (PO_1–PO_3) Port 1 ($P1_1$–$P1_3$)	Port 0 (PO_1–PO_3) Port 1 ($P1_1$–$P1_3$)
Output ports	Port 2 ($P2_0$–$P2_2$)	Port 2 ($P2_0$–$P2_3$)	—
I/O ports	Port 1 ($P1_0$–$P1_3$) Port 7 ($P7_0$–$P7_3$)	Port 1 ($P1_0$–$P1_3$) Port 7 ($P7_0$–$P7_3$)	—
Number of ports	31	32	23
LCD controller/driver Multiplexing	Biplexed Triplexed Quadriplexed	—	Triplexed Quadriplexed
LCD controller/driver Segments	32		24
Package	80-pin flat	40-pin DIP/ 52-pin flat	64-pin flat

NEC

NEC Electronics Inc.

μPD7516H
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH FIP® CONTROLLER/DRIVER

Description

The μPD7516H and 75CG16H are 4-bit, single-chip CMOS microcomputers with the μPD7500 series architecture and a FIP controller/driver. On-board peripheral functions include an 8-bit timer/event counter, an 8-bit serial interface, a 14-bit programmable pulse generator, and a display controller/driver that supervises all of the timing requirements by the 24-port S segment drivers either for a 16-character, 7-segment FIP, or an 8-character, 14-segment FIP. The μPD7516H is functionally equivalent to the μPD7519H except for ROM size.

Twenty-eight I/O lines are organized into seven 4-bit ports: the input/serial interface port 0, output ports 2 and 3, and I/O ports 1, 4, 5, and 6.

The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values.

The μPD7516H/75CG16H has a 2.44 μs instruction cycle time at f_{XX} = 6.55 MHz.

For the μPD7516H, current consumption is less than 6 mA for normal operation (V_{DD} = 5 V ±10%, f_{XX} = 6.55 MHz, high speed mode).

The μPD75CG16H, a piggyback EPROM version, is available for prototyping and program development. It is pin-compatible and functionally equivalent to the masked version.

Features

- ☐ 6144 × 8-bit program memory (ROM)
- ☐ 256 × 4-bit data memory (RAM)
- ☐ 28 I/O lines
- ☐ Programmable FIP controller/driver
  - — 24 high-voltage output lines
- ☐ 8-bit serial interface
- ☐ 8-bit timer/event counter
- ☐ Programmable pulse generator (PPG)
  - — Variable duty port (D/A converter)
  - — Signal generator port
  - — 1-bit output port
- ☐ Vectored, prioritized interrupts
  - — Two external: INT0, INT1
  - — Two internal: timer (INTT) and serial (INTS)
- ☐ Four 4-bit general purpose registers
- ☐ 107 instructions; subset of μPD7500 series instruction set A
  - — Look-up-table capability
  - — Indirect indexed addressing
- ☐ Instruction cycle
  - — μPD7516H low speed mode: 15.26 μs/4.19 MHz
  - — μPD7516H low speed mode: 9.77 μs/6.55 MHz
  - — μPD7516H high speed mode: 3.81 μs/4.19 MHz
  - — μPD7516H high speed mode: 2.44 μs/6.55 MHz
- ☐ Two power-down modes
- ☐ Single power supply (2.5 V to 6 V)

® FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

Applications

The μPD7516H has a variety of flexible powerful functions and is best suited for the following applications:

- Video tape recorders
- Plain paper copiers
- Electronic cash registers
- Telephone sets
- Electronic scales
- Automobiles

Figures 1-4 show how to apply the device to a digital tuning system, a telephone, an ECR, and automotive equipment.

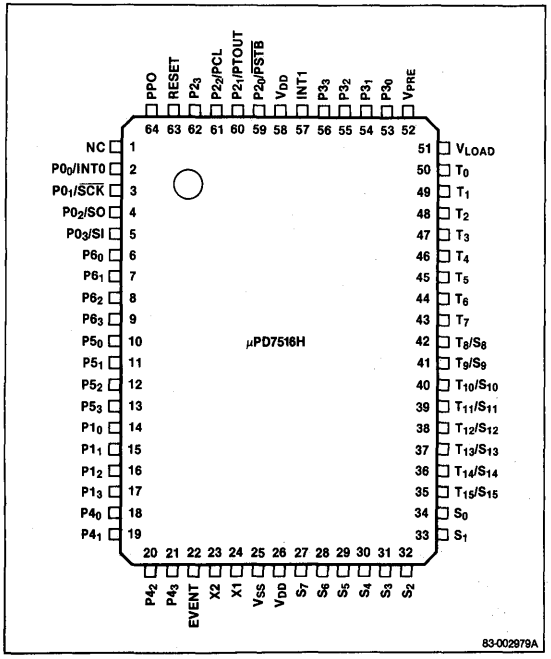
Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7516HG-12	64-pin plastic miniflat	6.55 MHz
μPD7516HG-36	64-pin plastic QUIP	6.55 MHz
μPD7516HCW	64-pin plastic shrink DIP	6.55 MHz
μPD75CG16HE	64-pin ceramic piggyback QUIP	6.55 MHz

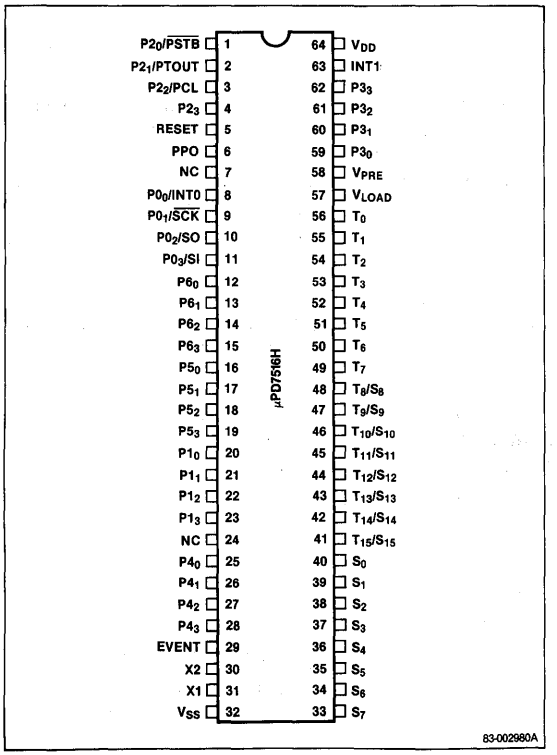
3

Pin Configurations

64-Pin Plastic Miniflat



64-Pin Plastic QUIP and Shrink DIP



Pin Identification

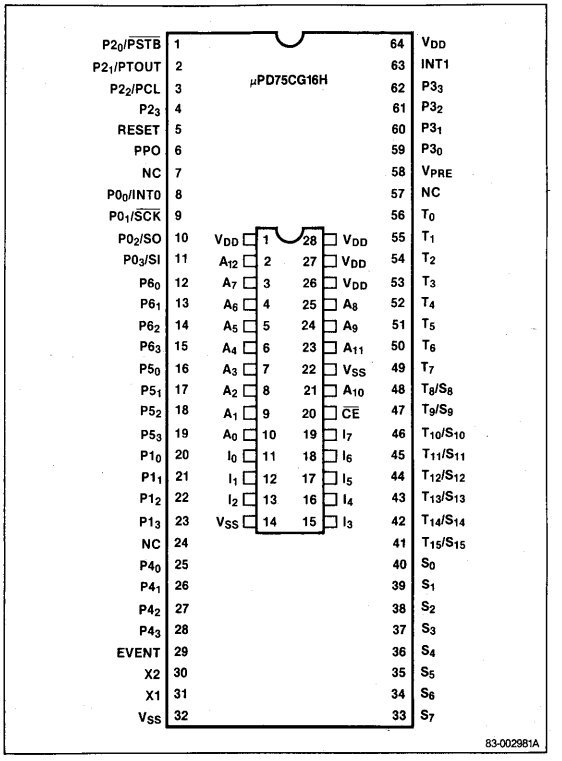
Plastic Miniflat, QUIP, and Shrink DIP

Flat	QUIP(1)	Symbol	Function
1	7, 24	NC	No connection
2	8	$P0_0$ / INT0	Port 0, or external interrupt INT0 and the serial I / O interface
3	9	$P0_1$ / $\overline{SCK}$	
4	10	$P0_2$ / SO	
5	11	$P0_3$ / SI	
6–9	12–15	$P6_0$–$P6_3$	Port 6
10–13	16–19	$P5_0$–$P5_3$	Port 5
14–17	20–23	$P1_0$–$P1_3$	Port 1
18–21	25–28	$P4_0$–$P4_3$	Port 4
22	29	EVENT	Timer / event counter input
23, 24	30, 31	X2, X1	Crystal clock input
25	32	V_{SS}	Ground
26, 58	64	V_{DD}	Power supply positive
27–34	33–40	S_0–S_7	Segment outputs
35–42	41–48	T_8 / S_8–T_{15} / S_{15}	Timing / segment outputs
43–50	49–56	T_0–T_7	Timing outputs
51	57	V_{LOAD}	High voltage option resistor supply negative. This pin is not used (NC) in the μPD75CG16H.
52	58	V_{PRE}	High voltage predriver supply negative
53–56	59–62	$P3_0$–$P3_3$	Port 3
57	63	INT1	External interrupt
59	1	$P2_0$ / $\overline{PSTB}$	Port 2, or port 1 STB signal, timer F / F output, internal CL output, and general purpose output
60	2	$P2_1$ / PTOUT	
61	3	$P2_2$ / PCL	
62	4	$P2_3$	
63	5	RESET	RESET input
64	6	PPO	PPG output

Note:
(1) This QUIP pin identification is also true for the shrink DIP and piggyback packages.

Pin Configurations (cont)

64-Pin Ceramic Piggyback QUIP



Pin Identification (cont)

μPD75CG16H, Piggyback EPROM

No.	Symbol	Function
1	V_{DD}	Unused
2–10, 21, 23–25	A_0–A_{12}	Program counter output
11–13, 15–19	I_0–I_7	Data input from the 2764
14	V_{SS}	Same as bottom pin 32; connected to 2764 GND pin
20	$\overline{CE}$	Chip enable output
22	V_{SS}	Same as bottom pin 32; supplies OE signal to the 2764
26	V_{DD}	Same as bottom pin 64; supplies V_{CC} to the 2764
27, 28	V_{DD}	Unused

Pin Functions

(Except EPROM)

$P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI (Port 0)

This port can be configured as the 4-bit, parallel input port 0, or as the 8-bit serial I/O interface under control of the serial mode select register. The 8-bit serial I/O interface consists of the serial input (SI), the serial output (SO), and a serial clock ($\overline{SCK}$) used for synchronizing data transfer. Line $P0_0$ is shared with external interrupt INT0, which is a rising edge-triggered interrupt.

$P1_0$–$P1_3$ (Port 1)

Individual lines can be configured as a 4-bit input or as a latched, three-state output under control of the port 1 mode select register.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$/PCL, $P2_3$

$P2_0$–$P2_3$ are the 4-bit latched output port 2. $\overline{PSTB}$ is the port 1 output strobe pulse. PTOUT is the timer-out F/F signal. PCL is the internal system clock output. $P2_3$ is a general purpose output.

$P3_0$–$P3_3$ (Port 3)

4-bit, latched three-state output port 3.

$P4_0$–$P4_3$ (Port 4)

4-bit latched three-state I/O port. Can perform 8-bit parallel I/O in conjunction with port 5.

$P5_0$–$P5_3$ (Port 5)

4-bit latched three-state I/O port. Can perform 8-bit parallel I/O in conjunction with port 4.

$P6_0$–$P6_3$ (Port 6)

Individual lines can be configured as a 4-bit input or as a latched, three-state output under control of the port 6 mode select register.

EVENT

1-bit external event input for the timer/event counter.

S_0–S_7, T_8/S_8–T_{15}/S_{15}, T_0–T_7

High voltage outputs. S_0–S_7 are segment driver outputs, and T_0–T_7 are digit driver outputs. T_8/S_8–T_{15}/S_{15} can be configured as either segment or digit driver outputs under control of the display mode select register.

INT1

External, rising edge triggered interrupt.

PPO

1-bit programmable pulse generator output. PPO can operate as the pulse width modulation output, signal generator port, or 1-bit output port, as dictated by the PPG mode select register.

RESET

RESET input. R/C circuit or pulse initializes μPD7516H and also releases stop or halt mode.

X1, X2

Crystal clock connection. A crystal oscillator circuit is connected to X1 and X2 for system clock operation, or an external clock may be connected to X1 and an inverted clock to X2.

V_{PRE}

High voltage predriver supply. Apply single voltage from V_{DD} – 12 V to V_{DD} for proper display operation.

V_{LOAD}

High voltage option resistor supply negative. Apply single voltage from V_{DD} – 40 V to V_{DD} for proper display operation. This pin is not used (NC) in the μPD75CG16H.

V_{DD}

Power supply positive. Apply single voltage ranging from 2.5 V to 6.0 V for proper operation.

V_{SS}

Ground.

EPROM Pin Functions

Piggyback EPROM

A_0–A_{12} (Address)

Output the 13 bits of the program counter (PC_0–PC_{11}), which are the address signals of EPROM 2764.

I_0–I_7 (Data Input)

Input data from the 2764.

$\overline{CE}$ (Chip Enable)

Outputs the chip enable signal to the 2764.

V_{DD} (Pin 1)

Electrically equivalent to V_{DD} of the bottom pins. Provided for future devices. Use in the open condition.

V_{DD} (Pin 26)

Electrically equivalent to V_{DD} of the bottom pins. Supplies V_{CC} to 2764.

V_{DD} (Pins 27, 28)

Electrically equivalent to V_{DD} of the bottom pins. Do not use these pins.

V_{SS} (Pin 22)

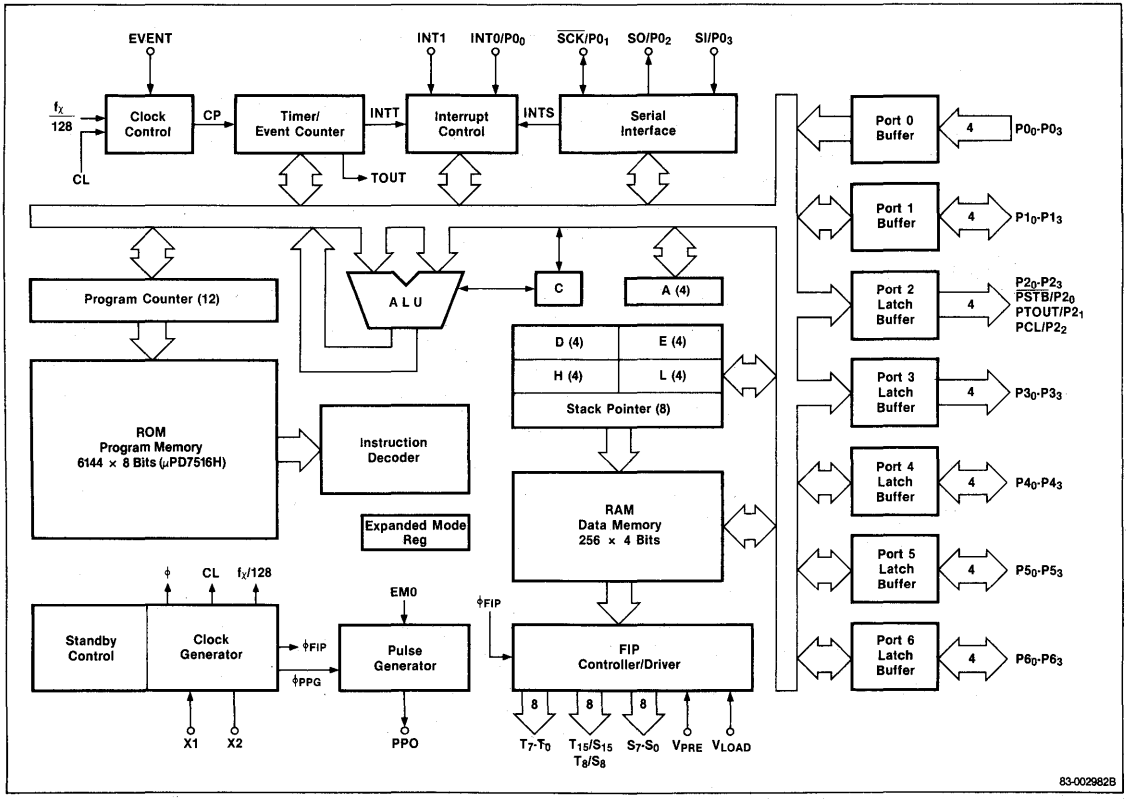
Electrically equivalent to VSS of the bottom pins. Supplies $\overline{OE}$ signal to the 2764.

V_{SS} (Pin 14)

Electrically equivalent to V_{SS} of the bottom pins. Connected to 2764 GND pin.

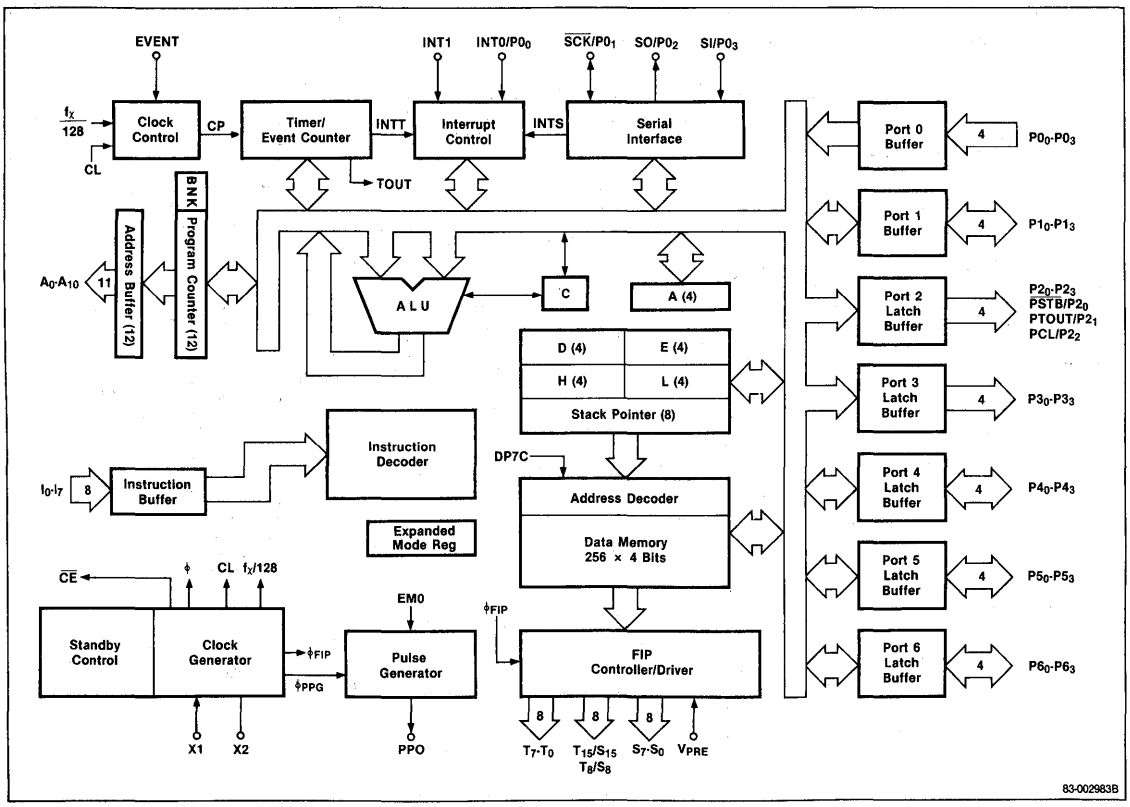
Block Diagrams

μPD7516H



Block Diagrams (cont)

μPD75CG16H



Absolute Maximum Ratings

$T_A = 25°C$

Supply voltages	
V_{DD}	−0.3 V to +7 V
V_{LOAD} (μPD7516H)	V_{DD} −40 V to +V_{DD} +0.3 V
V_{PRE}	V_{DD} −12 V to +V_{DD} +0.3 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	
Display outputs, V_O	V_{DD} −40 V to V_{DD} +0.3 V
Other outputs, V_{OD}	−0.3 V to V_{DD} +0.3 V
Output current high, I_{OH}	
Per pin, other than display outputs	−15 mA
Per pin, S_0–S_7	−15 mA
Per pin, T_0–T_7, T_8/S_8–T_{15}/S_{15}	−30 mA
Total, display outputs, μPD7516H	−120 mA
display outputs, μPD75CG16H	−90 mA
Total, other than display outputs	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Total, all output ports	60 mA
Total power consumption (Note 1), PT	
Plastic flat package (μPD7516H)	400 mW
Plastic QUIP, (μPD7516H)	600 mW
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

(1) Calculation of PT: there are three kinds of power consumption, the total of which should be less than the total power consumption (PT) in this specification. Use of less than 80% of PT is recommended. The three different power consumptions are as follows:
1. CPU power consumption. V_{DD}(max) × I_{DD1}(max)
2. Power consumption of output pins. This includes both normal output and display output. Calculate the total consumption of each output pin to which the maximum current flows.
3. Power consumption of on-chip pull-down resistors (mask option).

Example

Configuration:
9 segments × 11 digits, 4 LED outputs
V_{DD} = 5 V ±10%, 4.19 MHz oscillation
Segment pin = 5 mA (max)
Timing pin = 15 mA (max)
LED output pin = 10 mA (max)
Vacuum fluorescent display (V_{LOAD}) = −30 V

Consumption:
(1) CPU
5.5 V × 2.0 mA = 11 mW

(2) Output pins
Segment pins: (5/7 × 2 V) × 5 mA × 9 = 64 mW
Timing pins: 2 V × 15 mA = 30 mW
LED output pins: (10/15 × 2 V) × 10 mA × 4 = 53 mW

(3) Pull-down resistors
$(30 + 5.5\,V)^2/80\,k\Omega \times 10 = 158$ mW

Therefore, PT = (1) + (2) + (3) = 316 mW

DC Characteristics

μPD7516H: T_A = −10°C to +70°C, V_{DD} = 2.5 V to 6 V
μPD75CG16H: T_A = −10°C to +70°C, V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than X1, X2
	V_{IH2}	V_{DD}−0.4		V_{DD}	V	X1, X2 (Note 1)
Input voltage low	V_{IL1}	0		0.3 V_{DD}	V	Other than X1, X2
	V_{IL2}	0		0.4	V	X1, X2 (Note 1)
Output voltage high	V_{OH}	V_{DD}−1.0			V	V_{DD} = 5 V ±10%, I_{OH} = −1 mA
		V_{DD}−0.5			V	μPD7516H only, I_{OH} = −100 μA
Output voltage low	V_{OL}			0.4	V	V_{DD} = 5 V ±10%, I_{OL} = 1.6 mA
				0.5	V	μPD7516H only, I_{OL} = 400 μA
Input leakage current high	I_{LIH1}			3	μA	$V_I = V_{DD}$; other than X1, X2
	I_{LIH2}			20	μA	$V_I = V_{DD}$; X1, X2
Input leakage current low	I_{LIL1}			−3	μA	V_I = 0 V; other than X1, X2
	I_{LIL2}			−20	μA	V_I = 0 V; X1, X2
Input leakage current	I_{IL}			−200	μA	μPD75CG16H only; V_I = 0 V, I_0–I_7
Output leakage current high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current low	I_{LOL1}			−3	μA	V_O = 0 V; other than display outputs
	I_{LOL2}			−10	μA	$V_O = V_{LOAD} = V_{DD}$−35 V; display outputs

3

DC Characteristics (cont)

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 2.5\,V$ to $6\,V$
μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Display output current	I_{OD}	−7			mA	S_0–S_7; (Notes 2 & 3)
		−4			mA	μPD75CG16H; (Notes 2 & 3)
		−15			mA	T_0–T_{15} (Notes 2 & 3)
		−10			mA	μPD75CG16H; (Notes 2 & 3)
		−3			mA	S_0–S_7; (Note 4)
		−2			mA	μPD75CG16H; (Note 4)
		−7			mA	T_0–T_{15} (Note 4)
		−5			mA	μPD75CG16H; (Note 4)
On-chip pull-down resistance	R_L	40	70	120	kΩ	$V_{OD} - V_{LOAD} = 35\,V$
Supply current, μPD7516H	I_{DD1}		3.0	9.0	mA	High speed $V_{DD} = 5\,V \pm 10\%$; (Note 5)
	I_{DD2}		0.6	1.9	mA	Low speed halt mode $V_{DD} = 5\,V \pm 10\%$; (Note 5)
	I_{DD1}		2.0	6.0	mA	High speed $V_{DD} = 5\,V \pm 10\%$; (Note 6)
			400	1200	μA	$V_{DD} = 3\,V \pm 10\%$; (Note 6)
	I_{DD2}		450	1500	μA	Halt mode $V_{DD} = 5\,V \pm 10\%$; (Note 6)
			150	400	μA	Halt mode $V_{DD} = 3\,V \pm 10\%$; (Note 6)
	I_{DD3}		0.1	20	μA	Stop mode $V_{DD} = 5\,V \pm 10\%$; (Note 6)
			0.1	10	μA	Stop mode $V_{DD} = 3\,V \pm 10\%$; (Note 6)
Supply current, μPD75CG16H	I_{DD1}		1.2	3.6	mA	High speed $V_{DD} = 4.75\,V$ to $5.5\,V$; (Note 5)
			1.0	3.0	mA	High speed; (Note 6)
	I_{DD2}		350	1000	μA	Halt mode $V_{DD} = 5\,V \pm 10\%$; (Note 6)
	I_{DD3}			20	μA	Stop mode; (Note 6)

Note:
(1) The circuits in figures 19 and 20 are recommended.
(2) The external circuit in figure 21 is recommended.
(3) $V_{PRE} = V_{DD} - 9\,V \pm 1\,V$, $V_{DD} = 4\,V$ to $6\,V$, $V_{OD} = V_{DD} - 2\,V$
(4) $V_{PRE} = 0\,V$, $V_{OD} = V_{DD} - 2\,V$
(5) 6.55 MHz crystal, C1 = C2 = 10 pF
(6) 4.19 MHz crystal, C1 = C2 = 10 pF

Capacitance

$T_A = 25°C$; $V_{DD} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	(Note 1)
Output capacitance, Display outputs	C_O			35	pF	(Note 1)
Other outputs				15	pF	(Note 1)
I/O capacitance	C_{IO}			15	pF	(Note 1)

Note:
(1) $f_c = 1\,MHz$, Unmeasured pins are connected to 0 V.

AC Characteristics

Clock Operation

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 2.5\,V$ to $6\,V$

μPD75GC16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation	f_{XX}	3.5	4.19	4.2	MHz	(Notes 1, 2 & 3)
		4.2	6.55	6.6	MHz	$V_{DD} = 4.5\,V$ to $6.0\,V$; (Notes 1, 2 & 3)
System clock input frequency	f_X	0.1		4.2	MHz	(Notes 1 & 4)
		4.2		6.6	MHz	$V_{DD} = 4.5\,V$ to $6.0\,V$; (Notes 1 & 4)
X1, X2 input pulse width high, low	t_{XH}	100			ns	(Notes 1 & 4)
	t_{XL}	75				$V_{DD} = 4.5\,V$ to $6.0\,V$; (Notes 1 & 4)
EVENT input frequency	f_E			410	kHz	$V_{DD} = 4.0\,V$ to $6.0\,V$
				80	kHz	μPD7516H only
EVENT input pulse width high, low	t_{EL}	1.2			μs	$V_{DD} = 4.0\,V$ to $6.0\,V$
	t_{EH}	6.25			μs	μPD7516H only

Note:

(1) The circuits in figures 19 and 20 are recommended.

(2) Refer to the Operating Supply Voltage table.

(3) Crystal oscillation.

(4) External clock.

Port 1 I/O Operation

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 2.5\,V$ to $6\,V$

μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 5\,V \pm 10\%$

$0.1\,MHz \leq f_X, f_{XX} \leq 4.2\,MHz$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port 1 output set-up time (to $\overline{PSTB}$ ↑)	t_{PST}	250			ns	(Note 1)
Port 1 output hold time (after $\overline{PSTB}$ ↑)	t_{STP}	100			ns	(Note 1)
$\overline{PSTB}$ pulse width low	t_{STL1}	450			ns	(Note 1)
Output data set-up time (to $\overline{PSTB}$ ↑)	t_{DST}	200			ns	(Note 2)
Output data hold time (after $\overline{PSTB}$ ↑)	t_{STD}	100			ns	(Note 2)

Port 1 I/O Operation (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input data valid time (after $\overline{PSTB}$ ↓)	t_{STDV}			700	ns	(Note 2)
Input data floating time (after $\overline{PSTB}$ ↑)	t_{STDF}	0			ns	(Note 2)
Control set-up time (to $\overline{PSTB}$ ↓)	t_{CST}	100			ns	(Note 2)
Control hold time Output command	t_{STC}	100			ns	(Note 2)
Input command		0		80	ns	(Note 2)
$\overline{PSTB}$ pulse width low	t_{STL2}	750			ns	(Note 2)

Note:

(1) Port output mode.

(2) I/O expander mode $V_{DD} = 4\,V$ to $6\,V$.

Port 1 I/O Operation

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.5\,V$ to $6.0\,V$

μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.75\,V$ to $5.5\,V$

$4.2\,MHz \leq f_X, f_{XX} \leq 6.6\,MHz$

Low Speed Mode(1) ($EM_2 = 0$)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port 1 output set-up time (to $\overline{PSTB}$ ↑)	t_{PST}	400			ns	(Note 2)
Port 1 output hold time (after $\overline{PSTB}$ ↑)	t_{STP}	100			ns	(Note 2)
$\overline{PSTB}$ pulse width low	t_{STL1}	600			ns	(Note 2)
Output data set-up time (to $\overline{PSTB}$ ↑)	t_{DST}	400			ns	(Note 3)
Output data hold time (after $\overline{PSTB}$ ↑)	t_{STD}	100			ns	(Note 3)
Input data valid time (after $\overline{PSTB}$ ↓)	t_{STDV}			850	ns	(Note 3)
Input data floating time (after $\overline{PSTB}$ ↑)	t_{STDF}	0			ns	(Note 3)
Control set-up time (to $\overline{PSTB}$ ↓)	t_{CST}	400			ns	(Note 3)

3

AC Characteristics (cont)

Port 1 I/O Operation (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Control hold time Output command	t_{STC}	100			ns	(Note 3)
Input command		0		80	ns	(Note 3)
$\overline{PSTB}$ pulse width low	t_{STL2}	1200			ns	(Note 3)

Note:
(1) The μPD82C43/8243H, etc, cannot interface with the μPD7516H in high speed mode ($EM_2 = 1$).
(2) Port output mode.
(3) I/O expander mode $V_{DD} = 4$ V to 6 V.

Serial Interface Operation

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 2.5$ V to 6 V
μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 5$ V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{KCY}	2.1			μs	$V_{DD} = 4$ V to 6 V; Input
		12.5			μs	μPD7516H only; Input
		(1)			μs	$V_{DD} = 4$ V to 6 V; Output
		(2)			μs	μPD7516H only; Output
$\overline{SCK}$ pulse width high, low	t_{KH}	0.7			μs	$V_{DD} = 4$ V to 6 V; Input
	t_{KL}	6.5			μs	μPD7516H only; Input
		(3)			μs	$V_{DD} = 4$ V to 6 V; Output
		(4)			μs	μPD7516H only; Output
SI set-up time (to $\overline{SCK}$ ↑)	t_{SIK}	300			ns	$V_{DD} = 4$ V to 6 V
		1000			ns	μPD7516H only
SI hold time (after $\overline{SCK}$ ↑)	t_{KSI}	450			ns	$V_{DD} = 4$ V to 6 V
		1000			ns	μPD7516H only
SO output delay time (after $\overline{SCK}$ ↓)	t_{KSO}			500	ns	$V_{DD} = 4$ V to 6 V for 7516H
				2000	ns	μPD7516H only

Note:
(1) High speed mode: $16/f_x$ or $16/f_{xx}$
Low speed mode: $64/f_x$ or $64/f_{xx}$
(2) $64/f_{xx}$ or $64/f_{xx}$
(3) High speed mode: $8/f_x$ or $8/f_{xx}$
Low speed mode: $32/f_x$ or $32/f_{xx}$
(4) $32/f_{xx} - 2.0$ μs, or $32/f_{xx} - 2.0$ μs

Other Operations

μPD7516H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.5$ V to 6.0 V
μPD75CG16H: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.75$ V to 5.5 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
INT0 pulse width high, low	t_{I0H}, t_{I0L}	10			μs	
INT1 pulse width high, low	t_{I1H}, t_{I1L}	(1)			μs	
RESET pulse width high, low	t_{RSH}, t_{RSL}	10			μs	

Note:
(1) $26/f_x$ or $26/f_{xx}$

μPD75CG16H EPROM Characteristics

$T_A = -10°C$ to $+70°C$; $V_{DD} = 5$ V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Access time	t_{ACC}			700	ns	
$\overline{CE}$ low set-up time to data valid	t_{CE}			700	ns	
Data valid hold time to $\overline{CE}$ rising edge	t_{IH}	0			ns	

Operating Supply Voltages

$T_A = -10°C$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CPU (Note 1)		4.5		6.0	V	f_x, $f_{xx} = 4.2$ MHz to 6.6 MHz, (Note 3)
		4.0		6.0	V	$f_x = 0.1$ MHz to 4.2 MHz, $f_{xx} = 3.5$ MHz to 4.2 MHz, (Note 3)
		4.5		6.0	V	f_x, $f_{xx} = 4.2$ MHz to 6.6 MHz, (Note 4)
		2.5		6.0	V	$f_x = 0.1$ MHz to 4.2 MHz, $f_{xx} = 3.5$ MHz to 4.2 MHz, (Note 4)

AC Characteristics (cont)

Operating Supply Voltages (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Crystal oscillation circuit (Note 2)		4.5		6.0	V	f_{XX} = 4.2 MHz to 6.6 MHz, C1 = 10 pF, C2 ≤ 10 pF, (Note 5)
		2.7		6.0	V	C1 = 10 pF, C2 ≤ 10 pF, f_{XX} = 3.5 MHz to 4.2 MHz, (Note 5)
		2.85		6.0	V	C1 = 10 pF, C2 ≤ 22 pF, f_{XX} = 3.5 MHz to 4.2 MHz, (Note 5)
		2.5		6.0	V	External clock
Display controller		4.0		6.0	V	
PPG		4.0		6.0	V	
Port 1		2.5		6.0	V	Port output mode
		4.0		6.0	V	I/O expander mode

Note:

(1) Except the crystal oscillation circuit, display controller, PPG, and port 1.

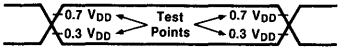
(2) The circuits in figure 19 and 20 are recommended.

(3) High speed mode, $EM_2 = 1$.

(4) Low speed mode, $EM_2 = 0$.

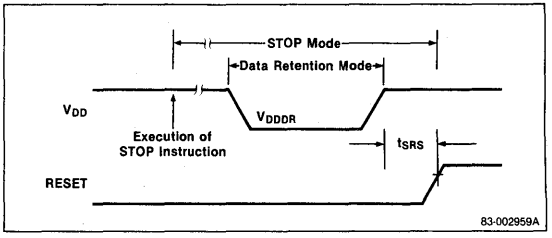
(5) Crystal Oscillator.

AC Waveform Measurement Points (Except X1, X2)

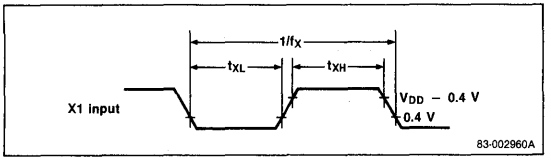


Timing Waveforms

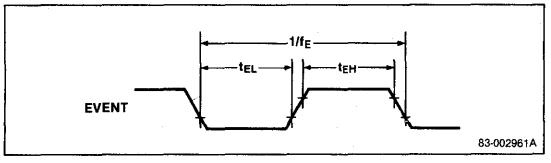
Data Retention Timing



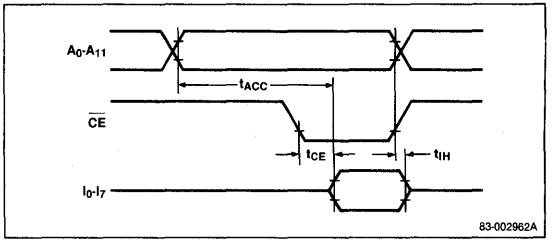
Clock Timing



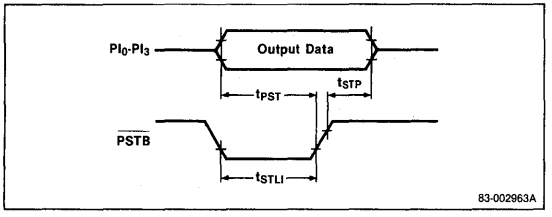
EVENT Timing



EPROM Timing

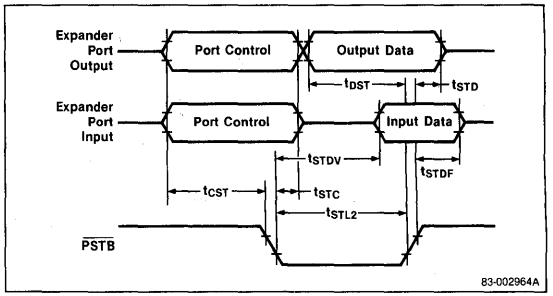


Strobe Output Timing

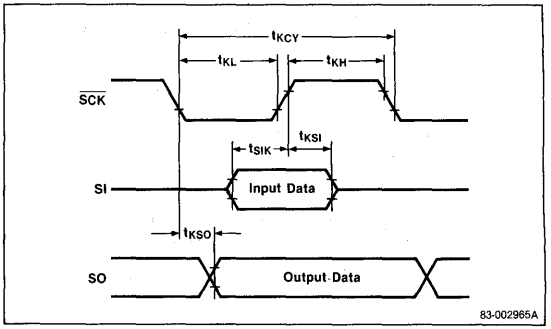


Timing Waveforms (cont)

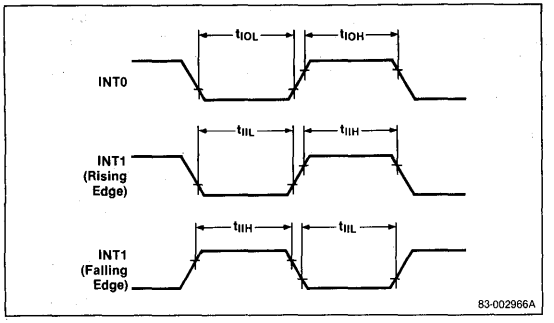
Port I/O Expander I/O Timing



Serial Transfer Timing



Interrupt Input Timing



RESET Input Timing

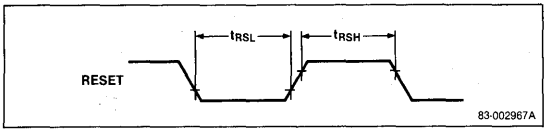


Figure 1. Digital Tuning System Application

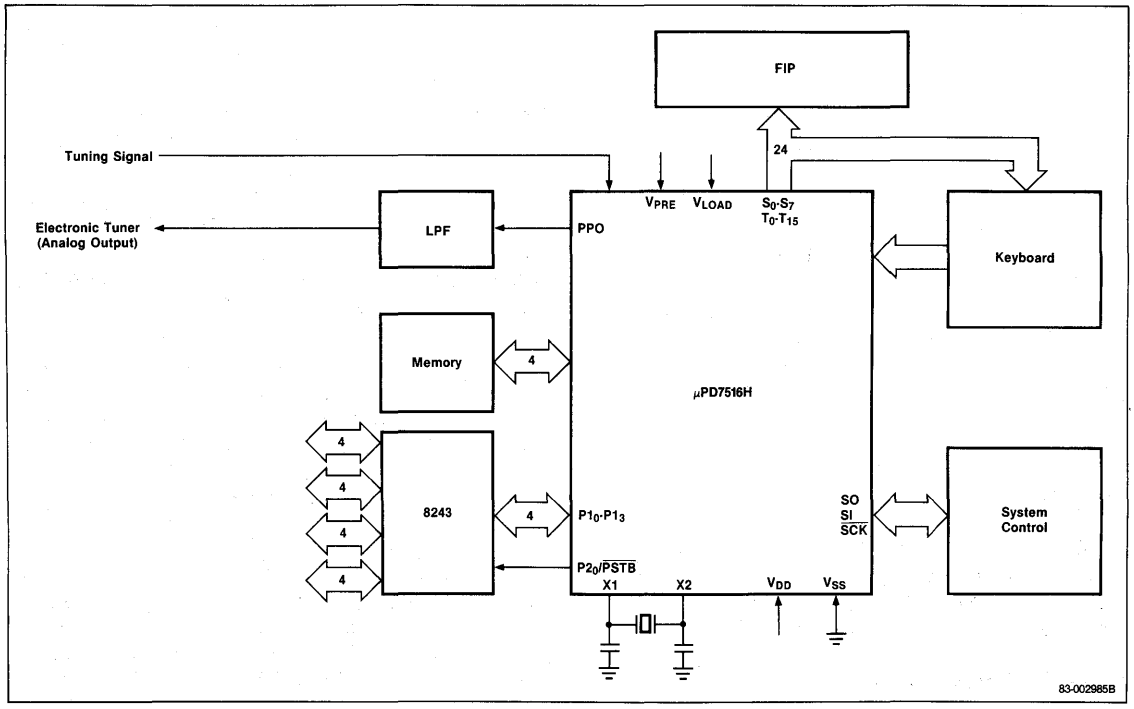


Figure 2. Telephone Application

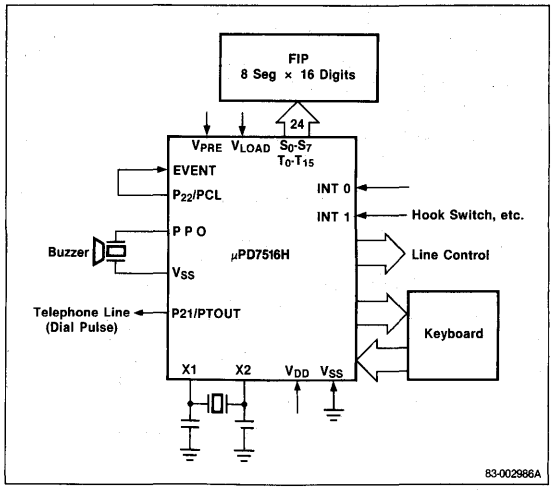


Figure 3. ECR Application

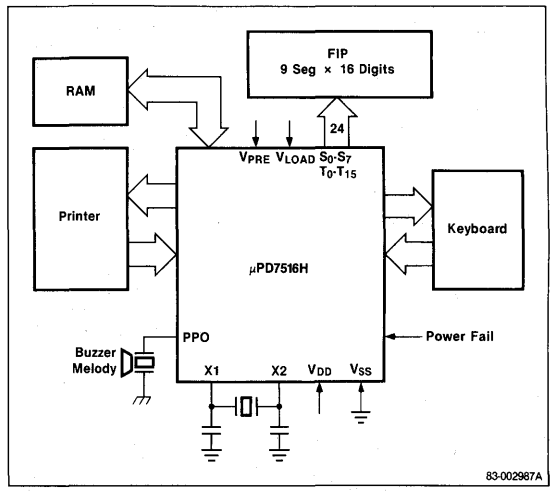


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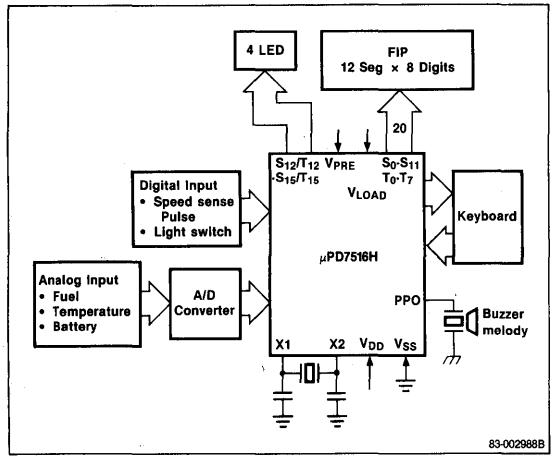
Figure 4. Automotive Equipment Application

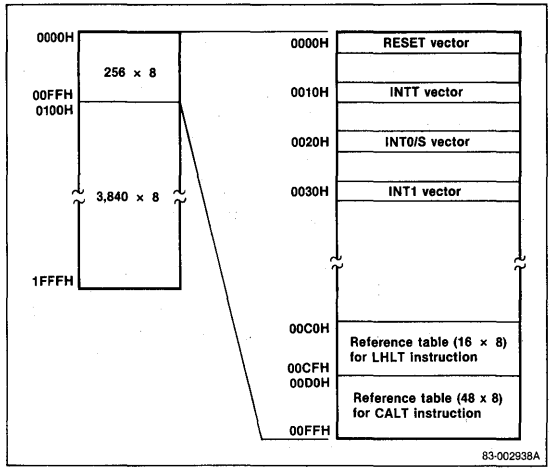


Functional Description

Program Memory (ROM), 6144 Words × 8 Bits

This mask-programmable memory is addressed by the bank flag (BNK) and the program counter (PC), and is used to store programs and table data. See figure 5.

Figure 5. Program Memory Map



General Purpose Registers

Four 4-bit general purpose registers (D, E, H, L) may be paired as follows for 8-bit operations: DE, HL, and DL. These 8-bit register pairs are commonly used as pointers to memory locations. When using the HL register pair as a data pointer, auto-increment and auto-decrement of the L register may be specified.

Data Memory (RAM), 256 Words × 4 Bits

This static RAM used to store display and operation data. It may also function with the accumulator (A) for 8-bit data processing.

There are three types of data memory addressing:

- Direct. Address designation is made on the second byte of the instruction.
- Register indirect. Address designation is made by the contents of a register pair designated by the instruction.
- Stack. Indirect address designation is made by the contents of the stack pointer (SP).

Data memory addresses are from 00H to 0FFH. The first 64 locations are pre-assigned as display data for the FIP display (00H to 03BH) and the programmable pulse generator (PPG) modulo section (03CH to 03FH). When display data is written in 00H-03BH, the FIP controller/driver automatically reads it and generates drive signals for the FIP. See figure 6.

Addresses 00H-03FH cannot be accessed by stack operations. RAM locations 40H-0FFH can be used as a stack area addressed by the SP. This data memory area is used when executing call or return instructions (CALL, CALT, RT, RTS, RTSPW), push/pop instructions (PSHDE, PSHHL, POPDE, POPHL), and when answering an interrupt.

When executing a call instruction or interrupt occurence with interrupts enabled, the contents of the PC and program status word (PSW) are stored in the stack area. A push instruction stores the contents of DE or HL in the stack area. See figure 7.

Figure 6. Data Memory Map

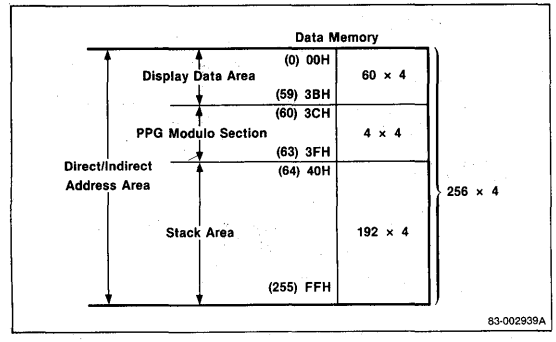
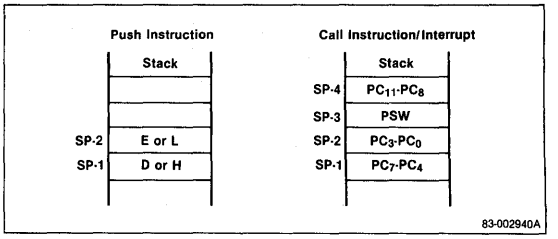


Figure 7. Push, Call, Interrupt



Clock Generator

The system clock generator consists of a crystal oscillator, a frequency divider, and a standby (stop/halt) mode control circuit, as shown in figure 8. When an external crystal is connected to X1 and X2, the crystal oscillator generates the f_{XX}. (The notation 'f_{XX}' is used when referring to crystal oscillation; 'f_X' is used when an external clock is input.) It is also possible to obtain a clock by inputting an external clock into X1 and an inverted clock to X2.

The frequency divider divides the output of the crystal oscillator into four frequencies, as follows:

- 1/2 (pulse generator clock, PPG)
- 1/8 (system clock, CLH)
- 1/32 (system clock, CLL; and FOP controller clock, FIP)
- 1/128 (timer/event counter clock)

The system clock (CL) may be 1/8 or 1/32 frequency-divided, depending on the state of expansion mode register bit 2 (EM_2). $EM_2 = 1$ selects 1/8, and $EM_2 = 0$ selects 1/32. CL is supplied to all circuits except the FIP controller and PPG, which use the $f_{XX} \times 1/32$ and $f_{XX} \times 1/2$, respectively. CL is 1/2 frequency divided to supply the CPU (ϕ) clock. CL is an input to the clock control circuitry used to generate the count pulse (CP) used by the timer/event counter.

The standby mode control circuit consists mainly of the stop and halt flip-flops. The stop flip-flop, when set, stops the crystal oscillator. There is no input to the frequency divider, so no clocks are output to the μPD7516H circuitry. The STOP instruction sets the stop flip-flop; RESET clears it. The halt flip-flop, when set, inhibits the input to the 1/2 frequency divider that generates ϕ, thereby stopping ϕ. A HALT or STOP sets this flip-flop; it is reset by the RELEASE signal (generated when an interrupt flag is set) or at the falling edge of the internal reset (IRESET) signal. (IRESET is released after a waiting time following the release of the external RESET input.)

Figure 8. Clock Generator Circuit

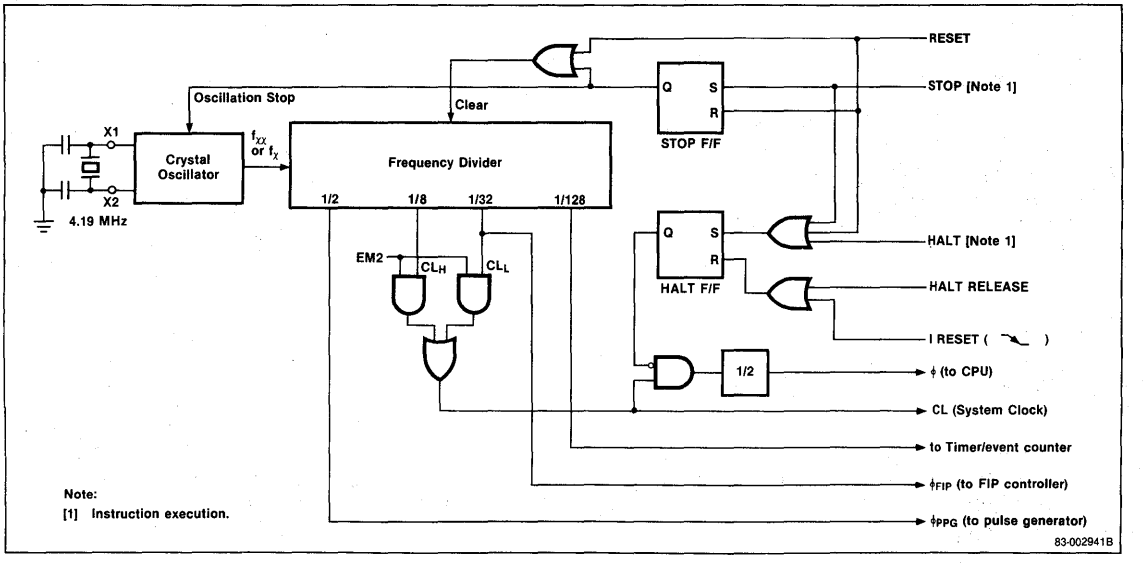
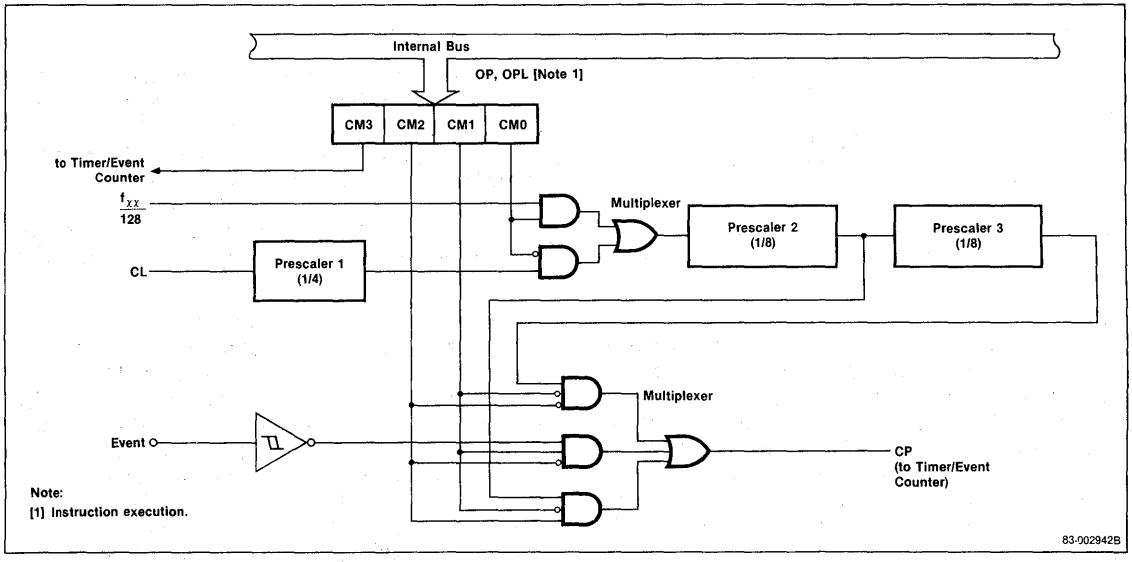


Figure 9. Clock Control Circuit



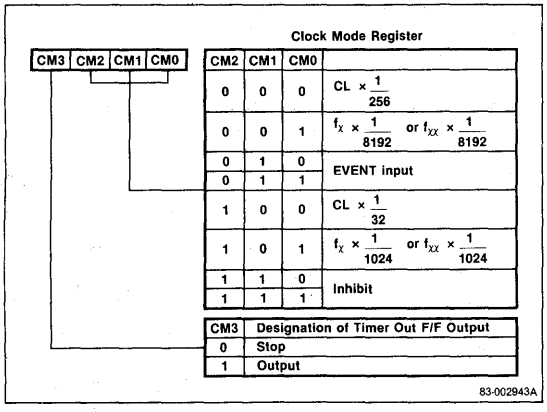
Clock Control Circuit

This circuit consists of a 4-bit clock mode register (CM_0–CM_3), three prescalers, and a multiplexer, as shown in figure 9. The circuit generates the clock pulse (CP) input to the timer/event counter from the following inputs:

- System clock (CL)
- $1/128$ divided clock from the crystal oscillator ($f_{XX}/128$)
- External EVENT pulse

Bit CM_0–CM_2 determine the clock input selection and divide ratio. CM_3 gates the output of a timer out signal from the PTOUT ($P2_1$) pin. When $CM_3 = 1$, output from the timer out flop-flop (TOUT) is output to $P2_1$. Executing an OP or OPL instruction loads the clock mode register. The format of the clock mode register is shown in figure 10.

Figure 10. Clock Mode Register



Timer/Event Counter

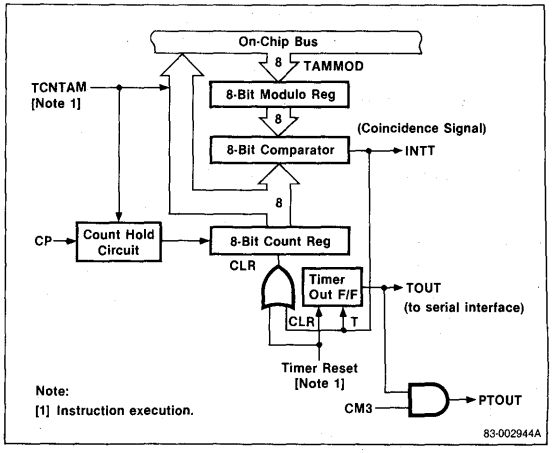
This counter consists of an 8-bit counter register, an 8-bit modulo register, an 8-bit comparator, and a timer-out flip-flop, as shown in figure 11.

The 8-bit count increments at every rising edge of the clock pulse (CP). It is cleared to 0 when executing the TIMER instruction, a RESET input, or a coincidence signal from the comparator.

The modulo register determines the INTT signal interval. The contents of this register are set via the TAMMOD instruction. RESET sets the contents to 0FFH.

The timer-out flip-flop inverts with every INTT signal output from the comparator. Its output, TOUT, can by sent to the PTOUT pin when bit 3 (CM_3) of the clock mode register is set. TOUT may also be used as a serial clock source to the serial interface.

Figure 11. Structure of the Timer/Event Counter



Serial Interface

The serial interface is used for serial data I/O. It consists of an 8-bit shift register, a 4-bit shift mode register, and a 3-bit counter, as shown in figure 12. Figure 13 shows the serial shift timing.

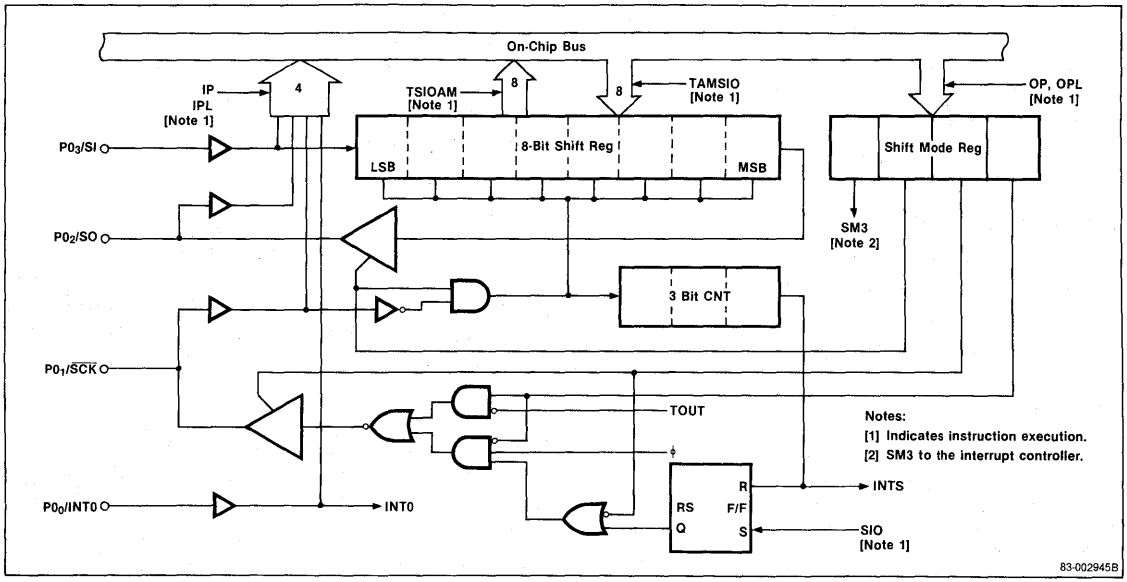
The serial clock ($\overline{SCK}$) controls the serial data communication rate. An 8-bit byte clocks into the serial input (SI) port or out of the serial output (SO) port starting with the MSB. Data transmission occurs synchronously with the falling edge of $\overline{SCK}$. Data reception occurs synchronously with the rising edge of $\overline{SCK}$.

The 3-bit counter counts the number of serial clock pulses. When a byte of serial data is transferred, an internal interrupt signal (INTS) is generated. Selecting INTS (setting SM_3 of the shift mode register to 0) sets the interrupt request flag, INT0/S RQF.

The end of transfer of each byte can also be verified by testing INTS RQF with the SKI instruction instead of interrupt processing.

3

Figure 12. Serial Interface Block Diagram



CPU Clock (ϕ)

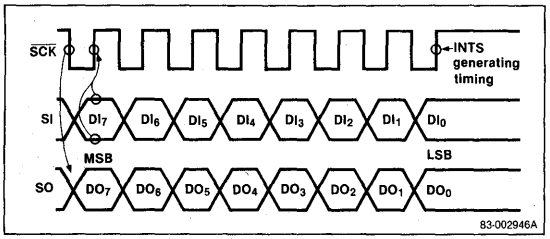
When the SIO instruction executes, eight CPU clock pulses (ϕ) are supplied to the serial interface for the serial clock and output from $\overline{SCK}$. After the eighth clock, $\overline{SCK}$ is fixed high level, automatically stopping serial data I/O after one byte has transferred.

$\overline{SCK}$ does not have to be software controlled. Its transfer rate is determined by the frequency of ϕ. See table 1.

Table 1. $\overline{SCK}$ Frequencies

f_{XX}	Low Speed Mode	High Speed Mode
6.55 MHz	102.4 kHz	409.6 kHz
4.19 MHz	65.5 kHz	262 kHz

Figure 13. Serial Shift Timing



Interrupt Function

There are two external and two internal interrupts, with the specifications listed in table 2. The external interrupt INT0 uses the $P0_0$ port pin as the interrupt signal input, and has the same interrupt process as the internal serial interrupt INTS. Selection of the interrupt is programmable and depends on the application.

Table 2. Interrupt Specifications

Source	Int/ Ext	Priority	Vector Address
INTT (coincidence signal from timer / event counter)	int	1	10H(16)
INT0 (interrupt signal from $P0_0$ terminal)	ext	2	20H(32)
INTS (end of transfer signal from serial interface)	int	2	20H(32)
INT1 (interrupt signal from INT1 terminal)	ext	3	30H(48)

Interrupt Sequence

When an interrupt goes active, the following occur:

- A corresponding interrupt request flag is set.
- The interrupt master enable flip-flop is reset.
- The contents of the PC and PSW are saved in the stack.
- An interrupt start address is generated and jumped to.
- The interrupt request flag set by the interrupt is reset.

Two machine cycles are required for interrupt execution, one for saving the return address and one for jumping to the interrupt start address. If several interrupts occur simultaneously, all respective request flags are set, and the interrupt with the highest priority is processed. The remaining interrupts are pending until serviced by reenabling the master interrupt flip-flop or until their interrupt request flags are reset by executing a SKI instruction.

Figure 14 is a block diagram of the interrupt control circuit.

FIP Controller/Driver

The FIP controller/driver consists of 60 4-bit nibbles of display memory (000-03BH of data RAM), a 4-bit display mode register (DM_3-DM_0), a 4-bit timing mode register (TM_3-TM_0), a 4-bit blanking mode register (BM_3-BM_0), an output selector, and a high voltage output driver. See figure 15.

The FIP controller/driver has 24 outputs for directly driving a high voltage vacuum fluorescent display:

- 8 segment signal outputs (S_0-S_7)
- 8 timing signal (grid) outputs (T_0-T_7)
- 8 timing or segment outputs (T_8/S_8-T_{15}/S_{15})

The contents of the display mode register determines which of the five display modes is available to the user. The modes are as follows:

- Static mode
  - 24 static output
- Dynamic mode
  - 8 segment mode
  - 12 segment mode I
  - 12 segment mode II
  - 16 segment mode

The contents of the timing mode register determine the number of display digits (1-16) and control the number of timing signals (T_0-T_{15}) output. Timing signals drive the grids of vacuum fluorescent display tubes. The voltage on the grid will determine the brightness of a digit (made up of one or more segments) or if the digit will be turned on or off.

The width of the timing signal pulse can be adjusted at eight independent steps by the value loaded into the blanking mode register. This function is useful for dimming control and for preventing display cross-talk of adjacent digits.

The active level of the timing signal can be designated high or low by bit DM_3.

Figure 14. Interrupt Control Circuit Block Diagram

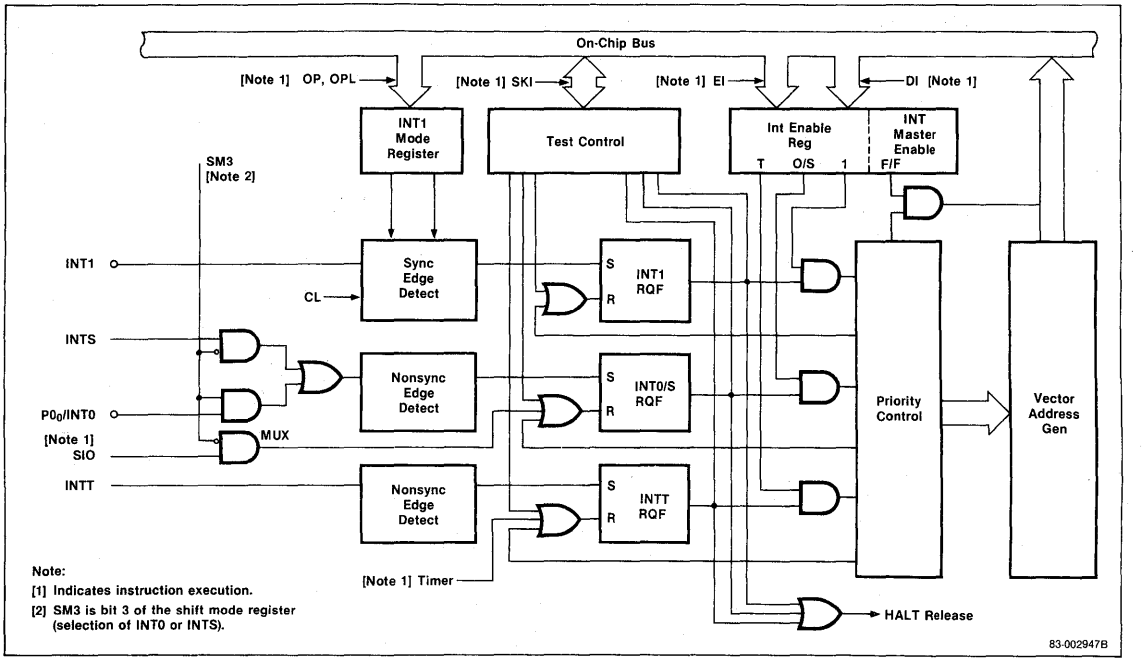
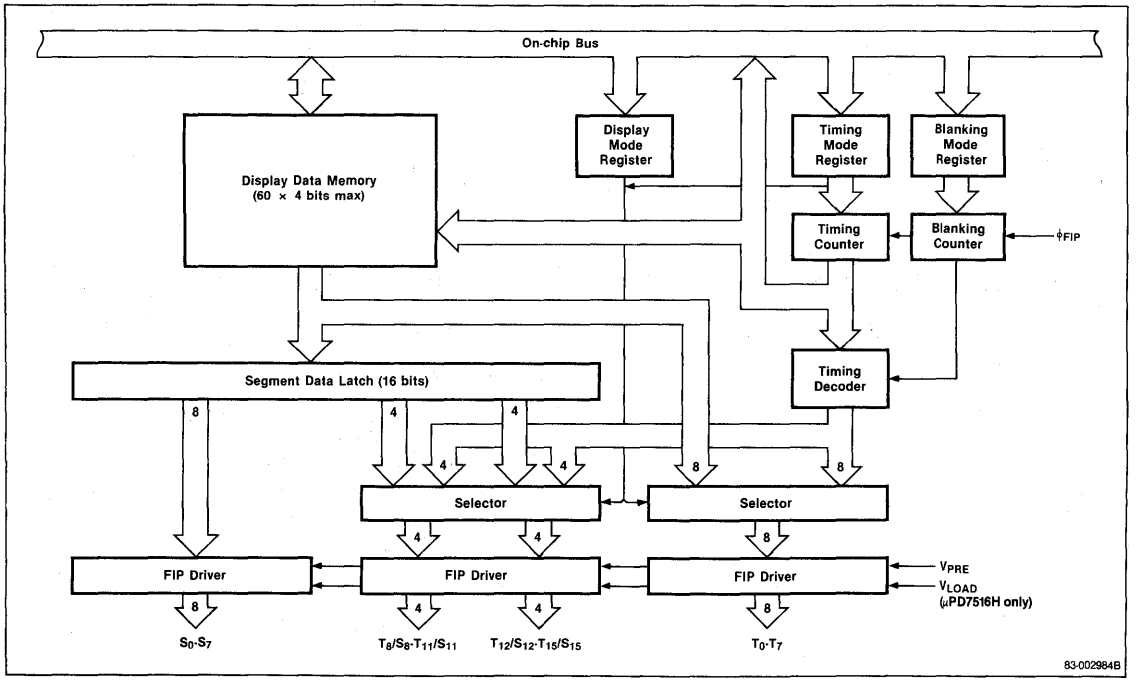


Figure 15. FIP Controller/Driver Block Diagram



Display Mode Register (DM)

This 4-bit write-only register (DM_3–DM_0) determines the display mode (dynamic, static, and off) of the FIP controller/driver. It also determines the active level of the display timing signals. This is shown in figure 16.

The DM register has an output address of 0BH and is accessed by the output instructions OP and OPL when bit EM3 of the expansion mode register is set. The DM register is cleared by a RESET.

Figure 17 showns a display example in 12-segment mode I.

Figure 16. Display Mode Register Format

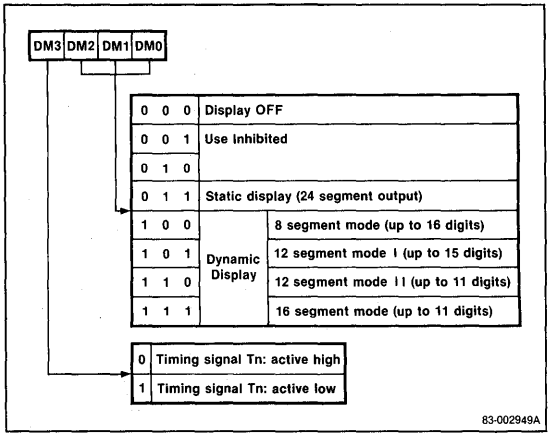
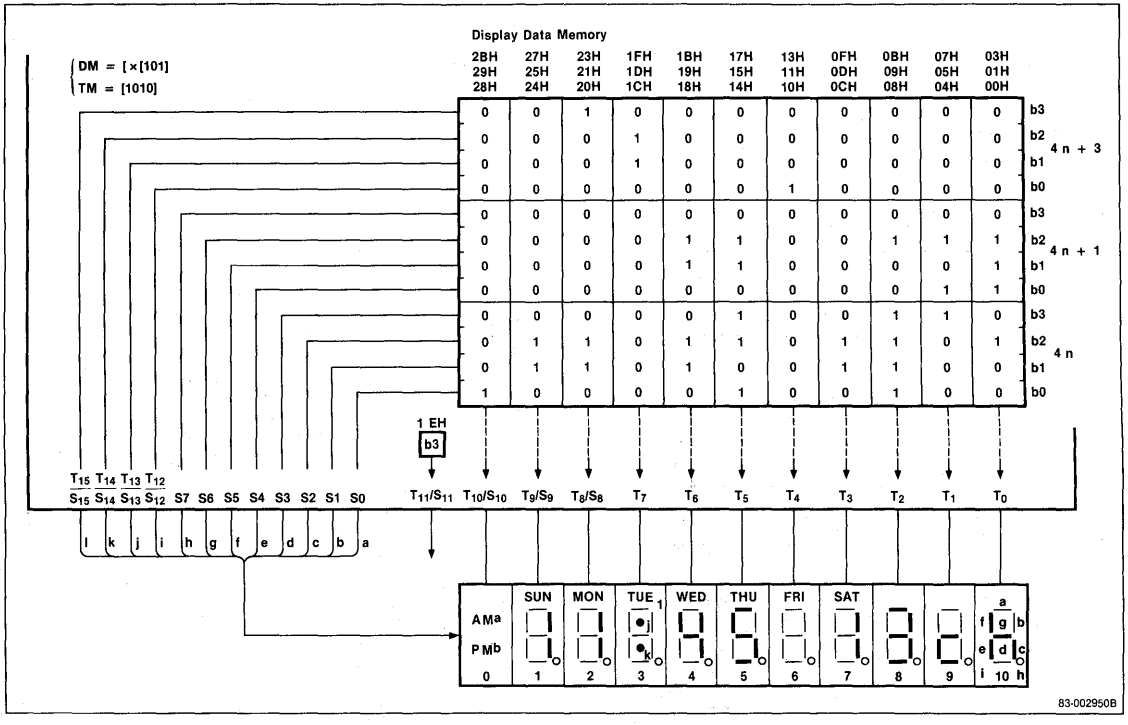


Figure 17. Display Example in 12-Segment Mode I



Standby Function

Two standby modes, stop and halt, hold device power consumption to a minimum. Stop mode is entered via the STOP instruction, and halt mode is entered via the HALT instruction. In stop mode, all clocks are stopped. In halt mode, only the CPU clock (ϕ) is stopped.

Stop mode can only be released by a RESET. Halt mode may be released either by a RESET or by the setting of an interrupt request flag.

Stop Mode

In stop mode, the contents of memory are retained, and all other functions are stopped. RESET releases stop mode.

In stop mode, the X1 input is internally shorted to V_{SS} in order to hold the crystal oscillator leakage to a minimum. A system using stop mode cannot use an external clock.

Halt Mode

When no interrupt flags are set, the HALT instruction causes the device to enter halt mode. In this mode, only ϕ stops; all other clocks continue to operate. The following functions continue to operate:

- Clock oscillation
- Frequency division and output of clocks other than ϕ
- Event input
- Timer/event counter
- Serial interface (except when ϕ is used as SCK)
- FIP controller/driver
- PPG
- Interrupts (INT0, INTS, INTT, INT1)
- RESET

Since a set interrupt flag releases the device from halt mode, this mode cannot be entered if an interrupt request flag is set. It is therefore necessary to reset the request flag(s) either by answering the interrupt(s) (setting the interrupt master enable F/F and process interrupt) or by executing the SKI instruction.

In halt mode, CPU power consumption is eliminated. To hold power consumption to a minimum, all unnecessary circuits should be inactive and the steps below should be taken:

- Set the system clock (CL) to low speed
- Set the FIP controller/driver to the off mode
- Set the PPG for static operation
- Stop $\overline{SCK}$ input

Low Supply Voltage Data Retention (μPD7516H only)

Data retention is possible with V_{DD} as low as 2 V. V_{DD} should be lowered after the device is put in stop mode and while RESET is inactive. Stop mode cannot be released in low voltage data retention mode; V_{DD} should first be raised to normal operation.

Release of Stop Mode

RESET releases stop mode. On RESET's rising edge, the device mode changes to halt mode, starting clock oscillation. At the falling edge of RESET, a waiting time (about 62.5 ms/4.19 MHz, 40 ms/6.55 MHz) elapses, allowing for stabilization of crystal operation; following this the halt mode is released. After normal RESET operation, the CPU begins program execution from address 0000H.

In the release operation, the contents of data memory are retained while the contents of other registers become undefined.

Power-on Reset Circuit

An example of the simplest power-on reset circuit using a resistor and capacitor is shown in figure 18.

Figure 18. Power-on Reset Circuit

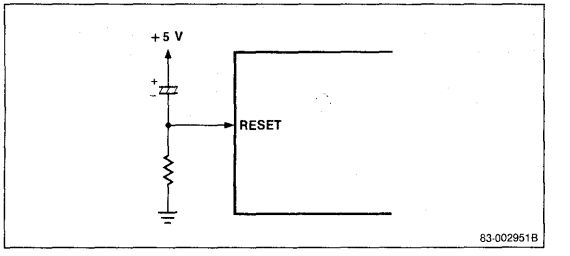


Figure 19. Crystal

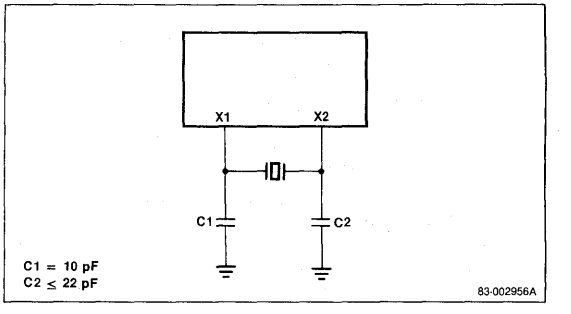


Figure 20. External Clock

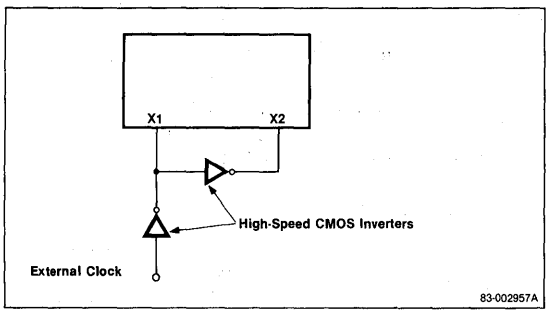
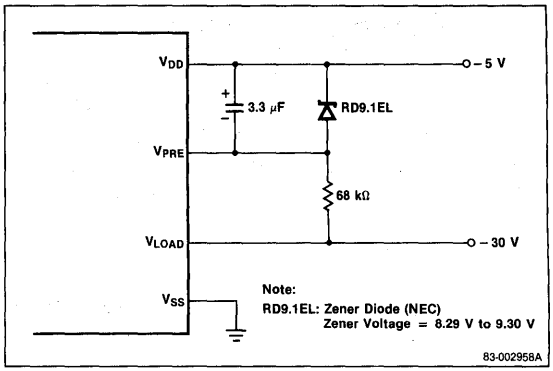
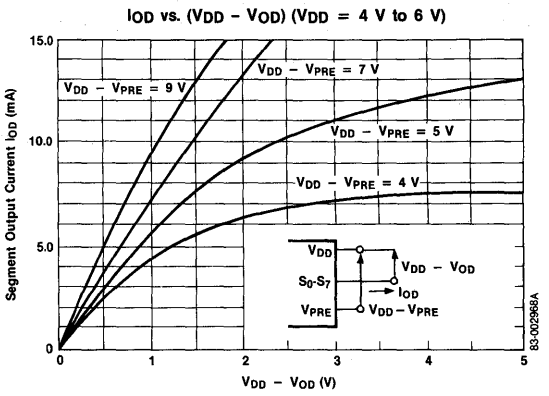


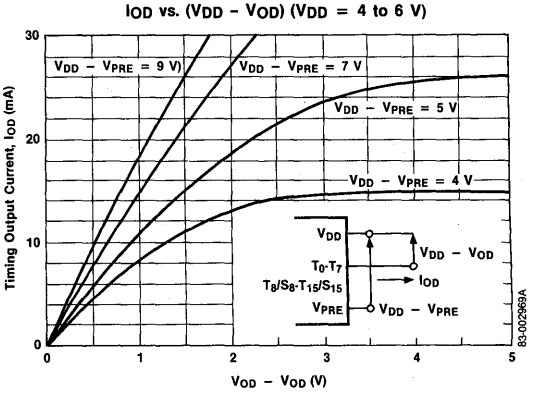
Figure 21. External Circuit

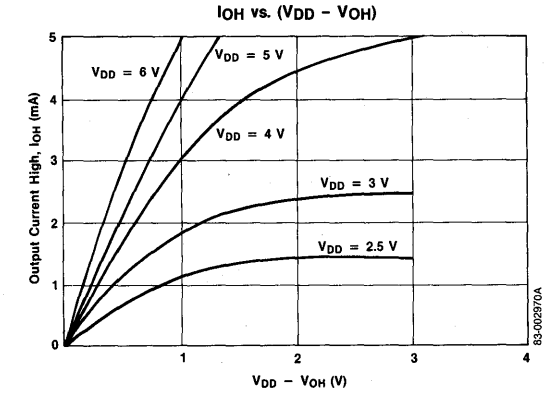


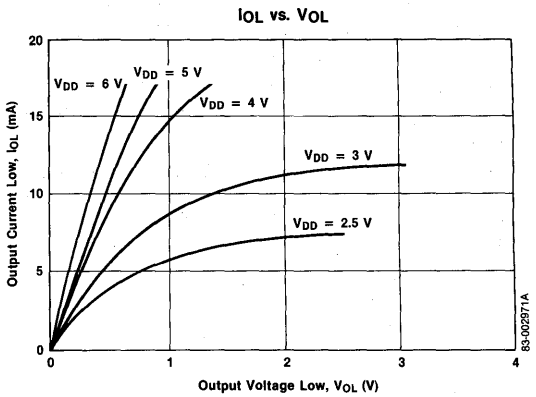
Operating Characteristics

$T_A = 25°C$



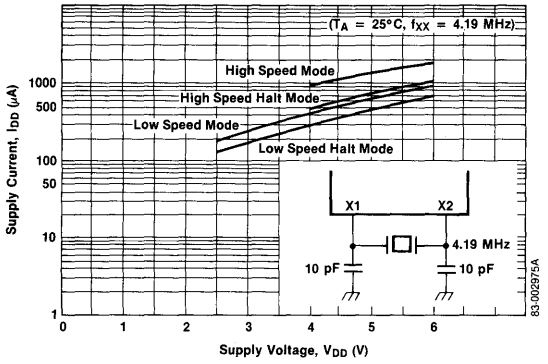




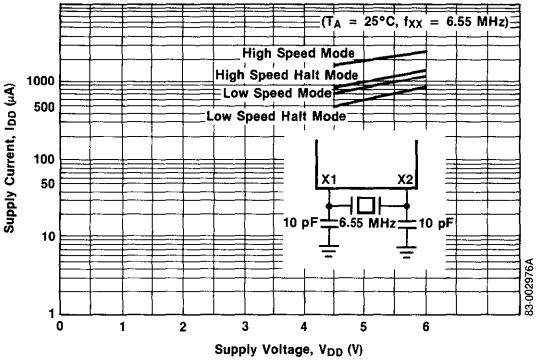


Operating Characteristics (cont)

I_{DD} vs. V_{DD}

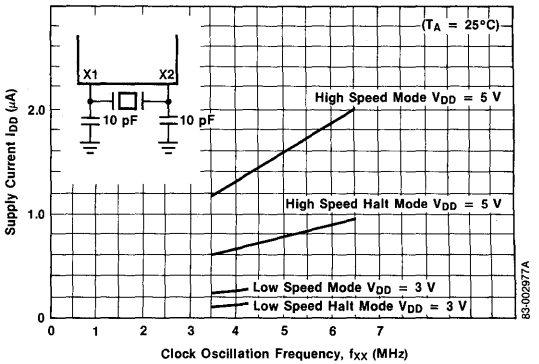


I_{DD} vs. V_{DD}

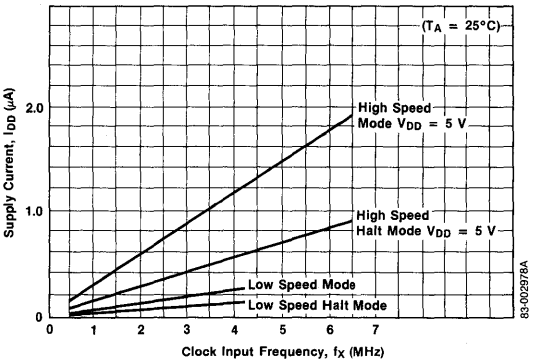


3

I_{DD} vs. f_{XX}



I_{DD} vs. f_X



NEC Electronics Inc.

μPD7519/19H 4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS WITH FIP® CONTROLLER/DRIVER

Description

The μPD7519, 7519H, 75CG19, and 75CG19H are CMOS 4-bit, single-chip microcomputers with the μPD7500 series architecture and a FIP controller/driver. On-board peripheral functions include and 8-bit timer/event counter, an 8-bit serial interface, a 14-bit programmable pulse generator, and a display controller/driver that supervises all of the timing requirements of the 24 port S segment drivers either for a 16-character, 7-segment FIP, or an 8-character, 14-segment FIP.

Twenty-eight I/O lines are organized into seven 4-bit ports: the input serial interface port 0, output ports 2 and 3, and I/O ports 1, 4, 5, and 6.

The subroutine stack is implemented in RAM for greater nesting depth and flexibility, providing such operations as the pushing and popping of register values.

The μPD7519 has a 7.63 μs instruction cycle time at f_{XX} = 4.19 MHz. The μPD7519H/75CG19H has a 2.44 μs instruction cycle time at f_{XX} = 6.55 MHz.

Current consumption for the μPD7519 is less than 2 mA in normal operation (V_{DD} = 5 V ± 10%, f_{XX} = 4.19 MHz, high speed mode) and is further reduced in the halt and stop power-down modes. For the μPD7519H, current consumption is less than 6 mA for normal operation (V_{DD} = 5 V ± 10%, f_{XX} = 6.55 MHz, high speed mode).

The μPD75CG19/75CG19H piggyback EPROM version, is available for prototyping and program development. It is pin-compatible and functionally equivalent to the masked version.

Note: FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

Features

- ☐ 4096 × 8-bit program memory (ROM)
- ☐ 256 × 4-bit data memory (RAM)
- ☐ 28 I/O lines
- ☐ Programmable FIP controller/driver
  - — 24 high-voltage output lines
- ☐ 8-bit serial interface
- ☐ 8-bit timer/event counter
- ☐ Programmable pulse generator (PPG)
  - — Variable duty port (D/A converter)
  - — Signal generator port
  - — 1-bit output port
- ☐ Vectored, prioritized interrupts
  - — Two external: INT0, INT1
  - — Two internal: timer (INTT) and serial (INTS)
- ☐ Four 4-bit general purpose registers
- ☐ 106 instructions; subset of μPD7500 series instructions set A
  - — Look-up-table capability
  - — Indirect indexed addressing
- ☐ Instruction cycle
  - — μPD7519 low speed mode: 15.26 μs/4.19 MHz
  - — μPD7519 high speed mode: 7.63 μs/4.19 MHz
  - — μPD7519H low speed mode: 15.26 μs/4.19 MHz
  - — μPD7519H low speed mode: 9.77 μs/6.55 MHz
  - — μPD7519H high speed mode: 3.81 μs/4.19 MHz
  - — μPD7519H high speed mode: 2.44 μs/6.55 MHz
- ☐ Two power-down modes
- ☐ Single power supply (2.5 V to 6.0 V)

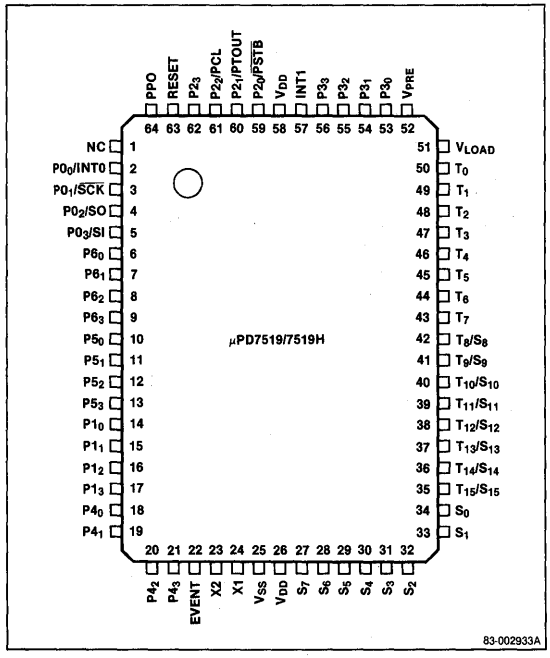
Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7519G-12	64-pin plastic miniflat	4.19 MHz
μPD7519G-36	64-pin plastic QUIP	4.19 MHz
μPD7519CW	64-pin plastic shrink DIP	4.19 MHz
μPD75CG19E	64-pin ceramic piggyback QUIP	4.19 MHz
μPD7519HG-12	64-pin plastic miniflat	6.55 MHz
μPD7519HG-36	64-pin plastic QUIP	6.55 MHz
μPD7519HCW	64-pin plastic shrink DIP	6.55 MHz
μPD75CG19HE	64-pin ceramic piggyback QUIP	6.55 MHz

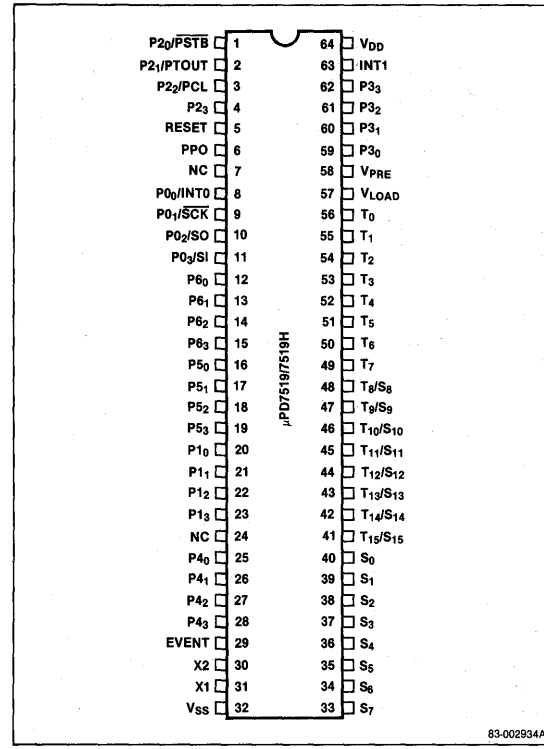
3

Pin Configurations

64-Pin Plastic Miniflat

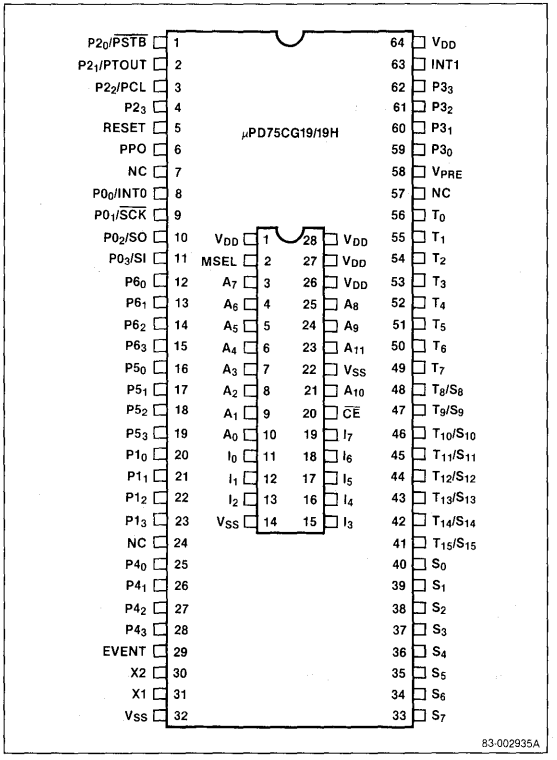


64-Pin Plastic QUIP and Shrink DIP



Pin Configurations (cont)

64-Pin Ceramic Piggyback QUIP



83-002935A

Pin Identification

Flatpack, Shrink DIP, and QUIP Packages

Flat	QUIP(1)	Name	Function
1	7, 24	NC	No connection
2	8	$P0_0$/INT0	Port 0 or external interrupt INT0 and the serial I/O interface
3	9	$P0_1$/$\overline{SCK}$	
4	10	$P0_2$/SO	
5	11	$P0_3$/SI	
6-9	12-15	$P6_0$-$P6_3$	Port 6
10-13	16-19	$P5_0$-$P5_3$	Port 5
14-17	20-23	$P1_0$-$P1_3$	Port 1
18-21	25-28	$P4_0$-$P4_3$	Port 4
22	29	EVENT	Timer/event counter input
23-24	30-31	X2, X1	Crystal clock input
25	32	V_{SS}	Ground
26, 58	64	V_{DD}	Power supply positive
27-34	33-40	S_0-S_7	Segment outputs
35-42	41-48	T_8/S_8-T_{15}/S_{15}	Timing/segment outputs
43-50	49-56	T_0-T_7	Timing outputs
51	57	V_{LOAD}	High voltage option resistor supply negative. This pin is not used (NC) in the μPD75CG19/75CG19H.
52	58	V_{PRE}	High voltage predriver supply negative
53-56	59-62	$P3_0$-$P3_3$	Port 3
57	63	INT1	External interrupt
59	1	$P2_0$/$\overline{PSTB}$	Port 2, or port 1 STB signal, timer F/F output, internal CL output, and general purpose output
60	2	$P2_1$/PTOUT	
61	3	$P2_2$/PCL	
62	4	$P2_3$	
63	5	RESET	RESET input
64	6	PPO	PPG output

Note:

(1) This QUIP pin identification is also true for the shrink DIP and piggyback packages.

3

Pin Identification (cont)

EPROM Socket on Piggyback QUIP

No.	Symbol	Function
1	V_{DD}	Unused
2	MSEL	Unused
3-10, 21, 23-25	A_0-A_{11}	Program counter output
11-13, 15-19	I_0-I_7	Data input from the 2732
14	V_{SS}	Same as bottom pin 32; connected to 2732 GND pin
20	$\overline{CE}$	Chip enable output
22	V_{SS}	Same as bottom pin 32; supplies $\overline{OE}$ signal to the 2732
26	V_{DD}	Same as bottom pin 64; supplies V_{CC} to the 2732
27, 28	V_{DD}	Unused

Pin Functions

$P0_0$/INT0, $P0_1$/$\overline{SCK}$, $P0_2$/SO, $P0_3$/SI (Port 0)

This port can be configured as the 4-bit, parallel input port 0, or as the 8-bit serial I/O interface under control of the serial mode select register. The serial interface consists of the serial input (SI), serial output (SO), and serial clock ($\overline{SCK}$) used for synchronizing data transfer. Line $P0_0$ is shared with external interrupt INT0, which is a rising edge-triggered interrupt.

$P1_0$-$P1_3$ (Port 1)

Individual lines can be configured as a 4-bit input or as a latched, three-state output under control of the port 1 mode select register.

$P2_0$/$\overline{PSTB}$, $P2_1$/PTOUT, $P2_2$/PCL, $P2_3$ (Port 2)

$P2_0$-$P2_3$ are the 4-bit latched output port 2. $\overline{PSTB}$ is the port 1 output strobe pulse. PTOUT is the timer-out F/F signal. PCL is the internal system clock output. $P2_3$ is a general purpose output.

$P3_0$-$P3_3$ (Port 3)

4-bit, latched three-state output port 3.

$P4_0$-$P4_3$ (Port 4)

4-bit latched three-state I/O port. Can perform 8-bit parallel I/O in conjunction with port 5.

$P5_0$-$P5_3$ (Port 5)

4-bit latched three-state I/O port. Can perform 8-bit parallel I/O in conjunction with port 4.

$P6_0$-$P6_3$ (Port 6)

Individual lines can be configured as a 4-bit input or as a latched, three-state output under control of the port 6 mode select register.

EVENT

1-bit external event input for the timer/event counter.

S_0-S_7, T_8/S_8-T_{15}/S_{15}, T_0-T_7

High voltage outputs. S_0-S_7 are segment driver outputs, and T_0-T_7 are digit driver outputs. T_8/S_8-T_{15}/S_{15} can be configured as either segment or digit driver outputs under control of the display mode select register.

INT1

External, rising edge triggered interrupt.

PPO

1-bit programmable pulse generator output. PPO can operate as the pulse width modulation output, the signal generator port, or as a 1-bit output port, as dictated by the PPG mode select register.

RESET

RESET input. R/C circuit or pulse initializes μPD7519/7519H and also releases stop or halt mode.

X2, X1

Crystal clock connection. A crystal oscillator circuit is connected to X1 and X2 for system clock operation. Or, an external clock may be connected to X1 and an inverted clock to X2.

V_{PRE}

High voltage predriver supply. Apply single voltage from V_{DD}–12 V to V_{DD} for proper display operation.

V_{LOAD}

High voltage option resistor supply negative. Apply single voltage from V_{DD}–40 V to V_{DD} for proper display operation. This pin is not used (NC) in the μPD75CG19/75CG19H.

V_{DD}

Power supply positive. Apply single voltage ranging from 2.5 V to 6.0 V for proper operation.

V_{SS}

Ground.

Pin Functions, EPROM Socket

A_0-A_{11} (Address)

Output the 12 bits of the program counter (PC_0-PC_{11}), which are the address signals of EPROM 2732.

I_0-I_7 (Data Input)

Input data from the 2732.

$\overline{CE}$ (Chip Enable)

Outputs the chip enable signal to the 2732.

V_{DD} (Pin 1)

Electrically equivalent to V_{DD} of the bottom pins. Provided for future devices. Use in the open condition.

V_{DD} (Pin 26)

Electrically equivalent to V_{DD} of the bottom pins. Supplies V_{CC} to the 2732.

V_{DD} (Pins 27, 28)

Electrically equivalent to V_{DD} of the bottom pins. Do not use these pins.

V_{SS} (Pin 22)

Electrically equivalent to V_{SS} of the bottom pins. Supplies $\overline{OE}$ signal to the 2732.

V_{SS} (Pin 14)

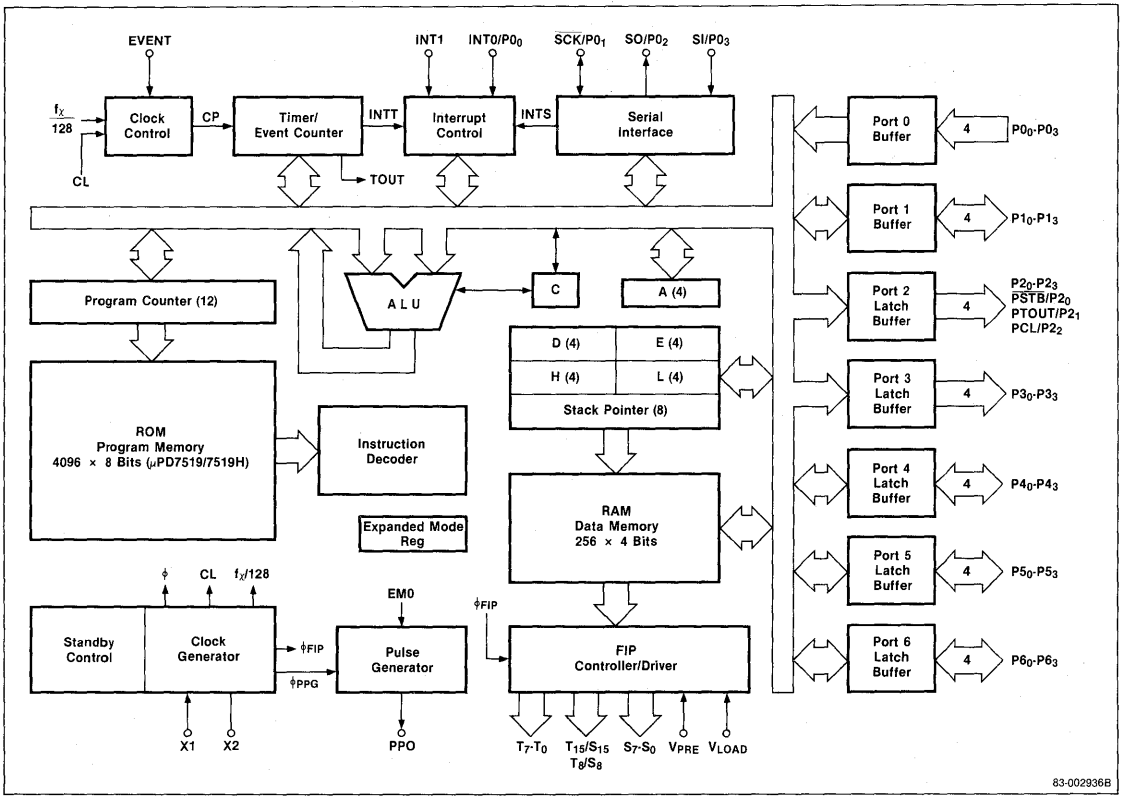
Electrically equivalent to V_{SS} of the bottom pins. Connected to 2732 GND pin.

MSEL

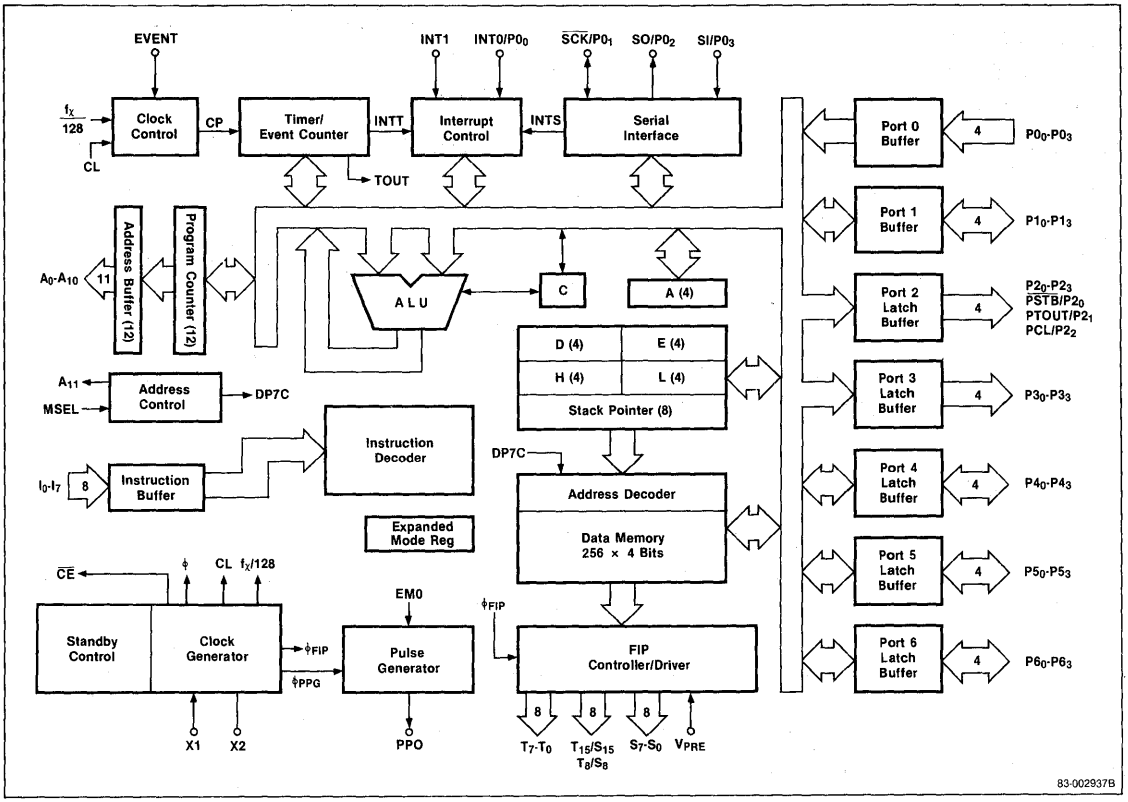
Provided for future devices. Use in the open condition.

3

Block Diagram, μPD7519/7519H



Block Diagram, μPD75CG19/75CG19H



Functional Description

Program Memory (ROM), 4096 Words × 8 Bits

This mask programmable memory is addressed by the program counter (PC), and is used to store programs and table data. See figure 1.

General Purpose Registers

Four 4-bit general purpose registers (D, E, H, L) may be paired as follows for 8-bit operations: DE, HL, and DL. These 8-bit register pairs are commonly used as pointers to memory locations. When using the HL register pair as a data pointer, auto-increment and -decrement of the L register may be specified.

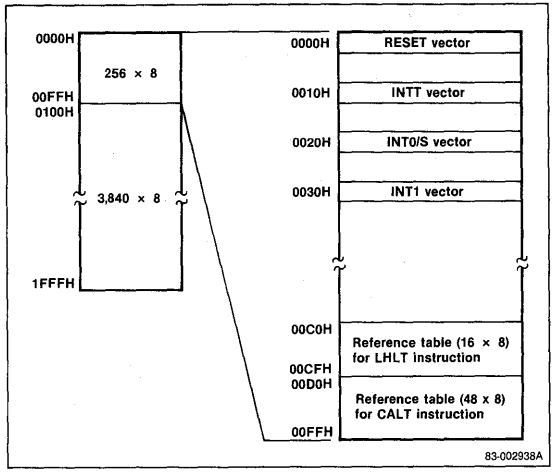
Data Memory (RAM), 256 Words × 4 Bits

This static RAM is used to store display and operation data. It may also function with the accumulator (A) for 8-bit data processing.

There are three types of data memory addressing:

- Direct. Address designation is made on the second byte of the instruction.
- Register indirect. Address designation is made by the contents of a register pair designated by the instruction.
- Stack. Indirect address designation is made by the contents of the stack pointer (SP).

Figure 1. Program Memory Map



Data memory addresses are from 00H to 0FFH. The first 64 locations are pre-assigned as display data for the FIP display (00H to 03BH) and the programmable pulse generator (PPG) modulo section (03CH to 03FH). When display data is written in 00H-03BH, the FIP controller/driver automatically reads it and generates drive signals for the FIP. See figure 2.

Addresses 00H-03FH cannot be accessed by stack operations. RAM locations 40H-0FFH can be used as a stack area addressed by the SP. This data memory area is used when executing call or return instructions (CALL, CALT, RT, RTS, RTSPW), push/pop instructions (PSHDE, PSHHL, POPDE, POPHL), and when answering an interrupt.

When executing a call instruction or interrupt occurrence with interrupts enabled, the contents of the PC and program status word (PSW) are stored in the stack area. A push instruction stores the contents of DE or HL in the stack area. See figure 3.

Figure 2. Data Memory Map

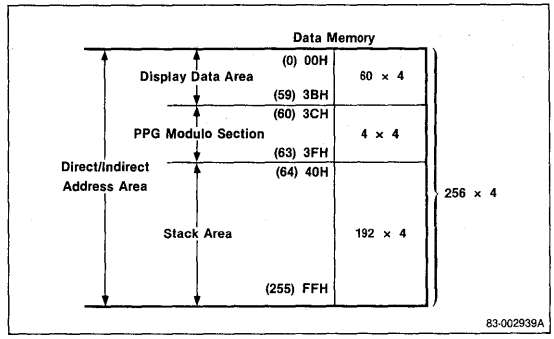
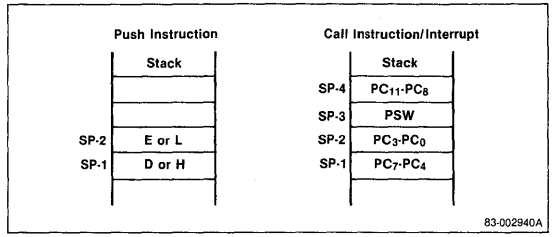


Figure 3. Push, Call, Interrupt



3

Clock Generator

The system clock generator consists of a crystal oscillator, a frequency divider, and a standby (stop/halt) mode control circuit, as shown in figure 4. When an external crystal is connected to X1 and X2, the crystal oscillator generates the f_{XX}. (The notation 'f_{XX}' is used when referring to crystal oscillation; 'f_X' is used when an external clock is input.) It is also possible to obtain a clock by inputting an external clock into X1 and an inverted clock to X2.

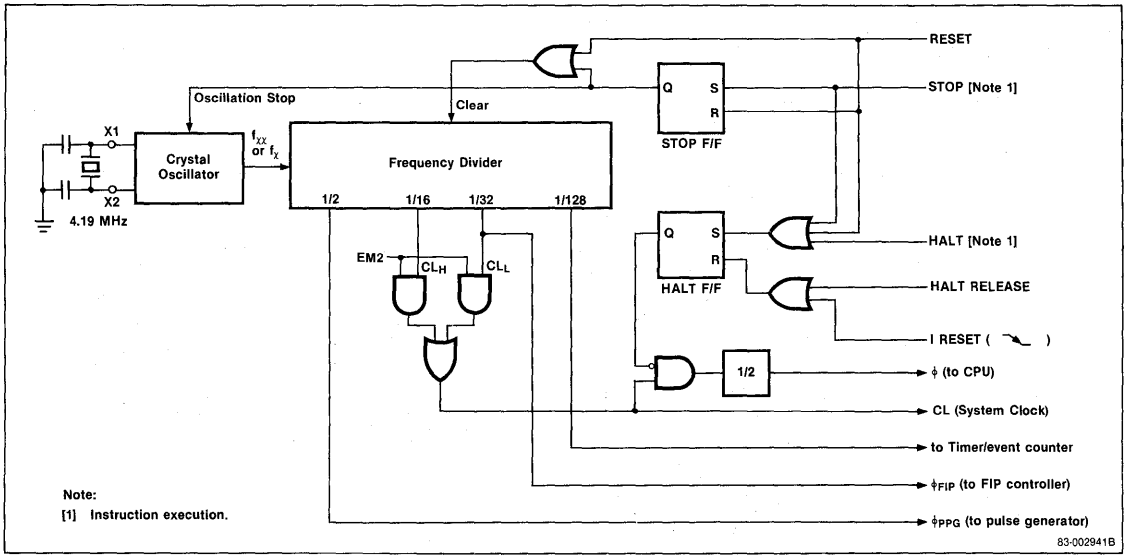
The frequency divider divides the output of the crystal oscillator into four frequencies, as follows:

- 1/2 (pulse generator clock, PPG)
- 1/8 (system clock, CLH) μPD7519H only
- 1/16 (system clock, CLH) μPD7519 only
- 1/32 (system clock, CLL; and FIP controller clock, FIP)
- 1/128 (timer/event counter clock)

The system clock (CL) may be 1/8 (μPD7519H), 1/16 (μPD7519) or 1/32 frequency-divided, depending on the state of expansion mode register bit 2 (EM_2). EM_2 = 1 selects 1/8 (μPD7519H) and 1/16 (μPD7519), and EM_2 = 0 selects 1/32. CL is supplied to all circuits except the FIP controller and PPG, which use the $f_{XX} \times 1/32$ and $f_{XX} \times 1/2$, respectively. CL is 1/2 frequency divided to supply the CPU (ϕ) clock. CL is an input to the clock control circuitry used to generate the clock pulse (CP) used by the timer/event counter.

The standby mode control circuit consists mainly of the stop and halt flip-flops. The stop flip-flop, when set, stops the crystal oscillator. There is no input to the frequency divider, so no clocks are output to the μPD7519/7519H circuitry. The STOP instruction sets the stop flip-flop, and RESET clears it. The halt flip-flop, when set, inhibits the input to the 1/2 frequency divider that generates ϕ, thereby stopping ϕ, A HALT or STOP sets this flip-flop; it is reset by the RELEASE signal (generated when an interrupt flag is set) or at the falling edge of the internal reset (IRESET) signal. (IRESET is released after a waiting time following the release of the external RESET input.)

Figure 4. Clock Generator Circuit



Clock Control Circuit

This circuit consists of a 4-bit clock mode register (CM_0-CM_3), three prescalers, and a multiplexer, as shown in figure 5. The circuit generates the clock pulse (CP) input to the timer/event counter from the following inputs:

- System clock (CL)
- 1/128 divided clock from the crystal oscillator ($f_{XX}/128$)
- External EVENT pulse

Bits CM_0-CM_2 determine the clock input selection and divide ratio. CM_3 gates the output of a timer out signal from the PTOUT ($P2_1$) pin. When $CM_3 = 1$, output from the timer out flip-flop (TOUT) is output to $P2_1$. Executing an OP or OPL instruction loads the clock mode register.

The format of the clock mode register is shown in figure 6.

Figure 6. Clock Mode Register

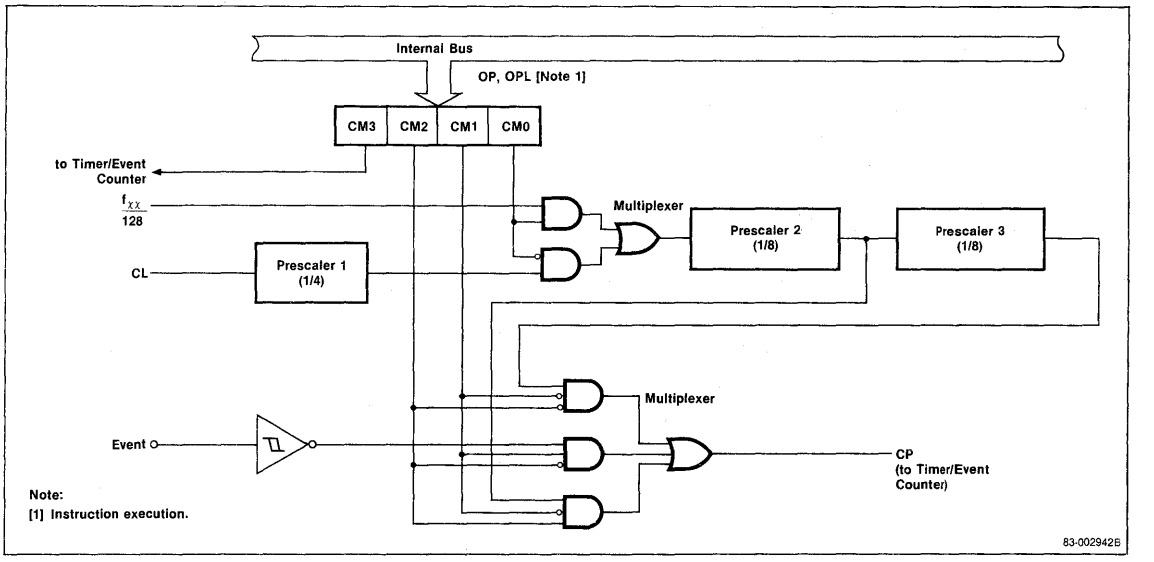
Clock Mode Register

CM3	CM2	CM1	CM0	
	0	0	0	CL × 1/256
	0	0	1	$f_X \times \frac{1}{8192}$ or $f_{XX} \times \frac{1}{8192}$
	0	1	0	EVENT input
	0	1	1	
	1	0	0	CL × 1/32
	1	0	1	$f_X \times \frac{1}{1024}$ or $f_{XX} \times \frac{1}{1024}$
	1	1	0	Inhibit
	1	1	1	

CM3	Designation of Timer Out F/F Output
0	Stop
1	Output

83-002943A

Figure 5. Clock Control Circuit



Timer/Event Counter

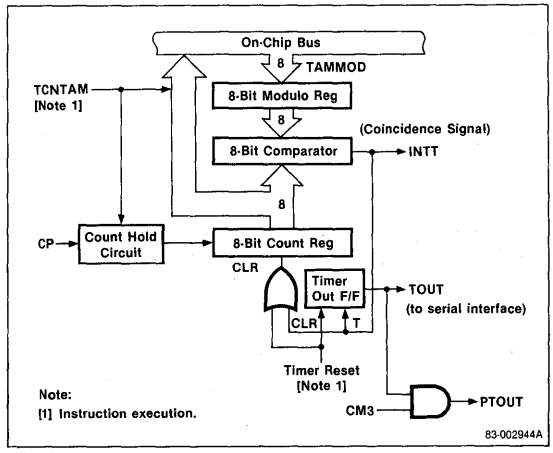
This counter consists of an 8-bit count register, an 8-bit modulo register, an 8-bit comparator, and a timer-out flip-flop, as shown in figure 7.

The 8-bit count increments at every rising edge of the clock pulse (CP). Executing the TIMER instruction, a RESET input, or a coincidence signal from the comparator clears it to 0.

The modulo register determines the INTT signal interval. The contents of this register are set via the TAMMOD instruction. RESET sets the contents to OFFH.

The timer-out flip-flop inverts with every INTT signal output from the comparator. Its output, TOUT, can be sent to the PTOUT pin when bit 3 (CM_3) of the clock mode register is set. TOUT may also be used as a serial clock source to the serial interface.

Figure 7. Structure of the Timer/Event Counter



Serial Interface

The serial interface, used for serial data I/O, consists of an 8-bit shift register, a 4-bit shift mode register, and a 3-bit counter, as shown in figure 8. Figure 9 shows the serial shift timing.

The serial clock ($\overline{SCK}$) controls the serial data communication rate. An 8-bit byte clocks into the serial input (SI) port or out of the serial output (SO) port starting with the MSB. Data transmission occurs synchronously with the falling edge of $\overline{SCK}$. Data reception occurs synchronously with the rising edge of $\overline{SCK}$.

The 3-bit counter counts the number of serial clock pulses. When a byte of serial data is transferred, an internal interrupt signal (INTS) is generated. Selecting INTS (setting SM_3 of the shift mode register to 0) sets the interrupt request flag, INT0/S RQF.

The end of transfer of each byte can also be verified by testing INTS RQF with the SKI instruction instead of interrupt processing.

Figure 8. Serial Interface Block Diagram

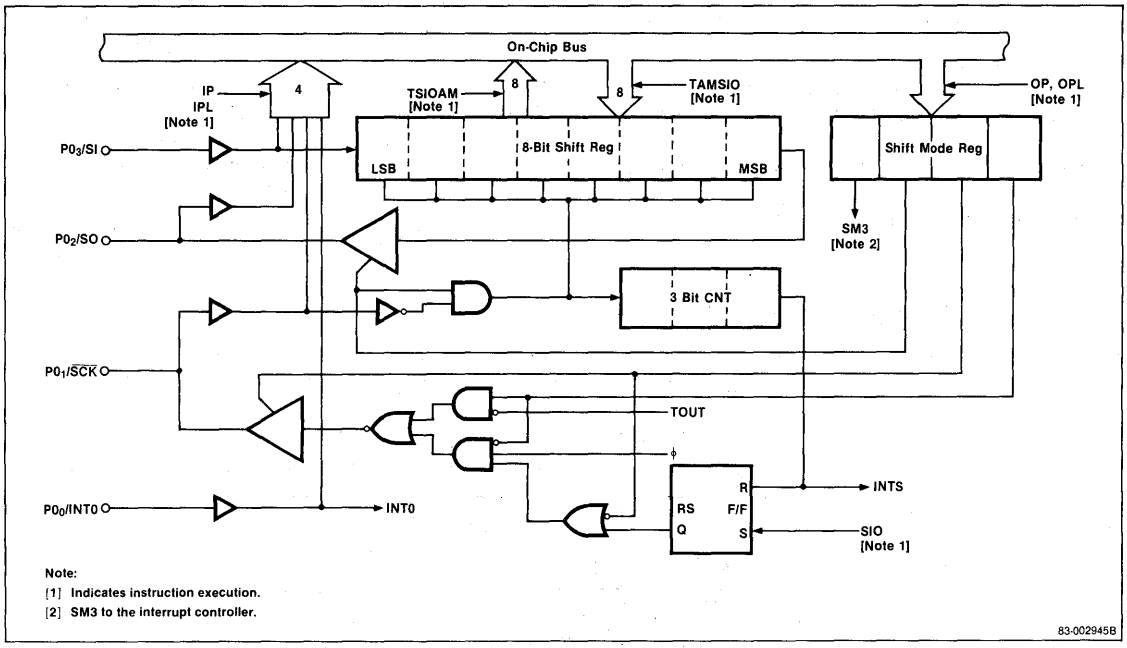
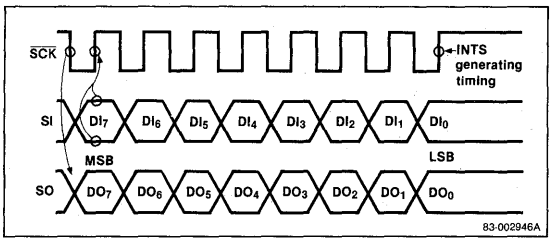


Figure 9. Serial Shift Timing



CPU Clock (ϕ)

When the SIO instruction executes, eight CPU clock pulses (ϕ) are supplied to the serial interface for the serial clock and output from $\overline{SCK}$. After the eighth clock, $\overline{SCK}$ is fixed high level, automatically stopping serial data I/O after one byte has transferred.

$\overline{SCK}$ does not have to be software controlled. Its transfer rate is determined by the frequency of ϕ. See table 1.

Interrupt Function

There are two external and two internal interrupts, with the specifications listed in table 2. The external interrupt INT0 uses the $P0_0$ port pin as the interrupt signal input, and has the same interrupt process as the internal serial interrupt INTS. Selection of the interrupt is programmable and depends on the application.

Table 1. SCK Frequencies

f_{XX}	Low Speed Mode	High Speed Mode
6.55 MHz	102.4 kHz	409.6 kHz (μPD7519H)
4.19 MHz	65.5 kHz	262 kHz (μPD7519H)
4.19 MHz	65.6 kHz	131 kHz (μPD7519)

Table 2. Interrupt Specifications

Source	Int/Ext	Priority	Vector Address
INTT (coincidence signal from timer/event counter)	int	1	10H(16)
INT0 (interrupt signal from $P0_0$ terminal)	ext	2	20H(32)
INTS (end of transfer signal from serial interface)	int	2	20H(32)
INT1 (interrupt signal from INT1 terminal)	ext	3	30H(48)

Interrupt Sequence

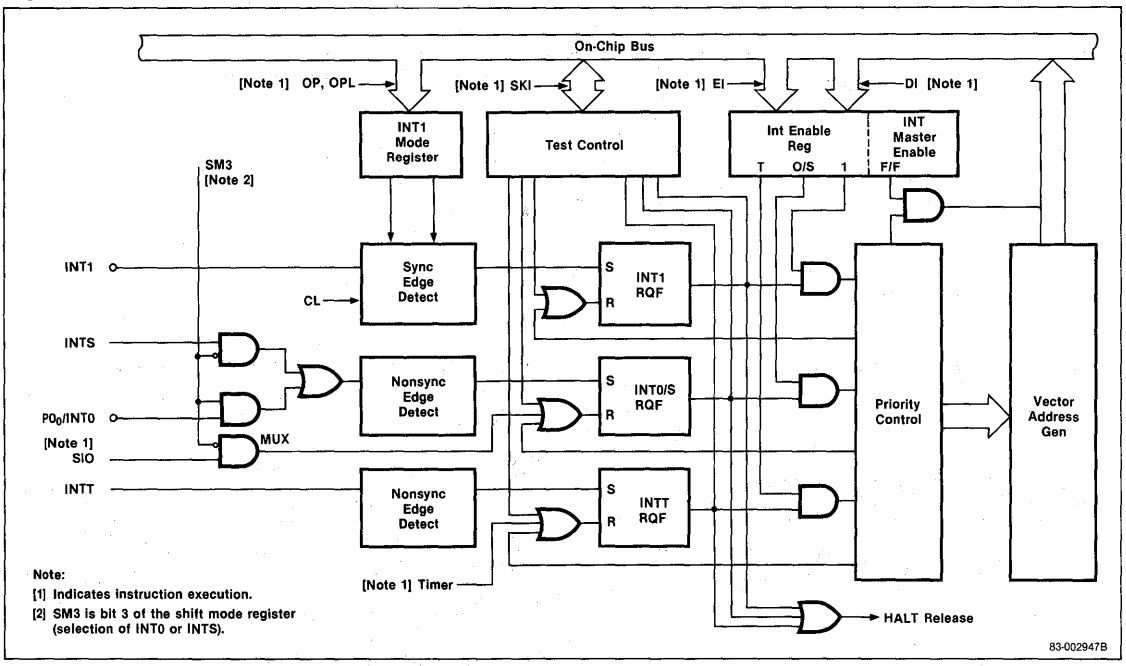
When an interrupt goes active, the following occur:

- A corresponding interrupt request flag is set.
- The interrupt master enable flip-flop is reset.
- The contents of the PC and PSW are saved in the stack.
- An interrupt start address is generated and jumped to.
- The interrupt request flag set by the interrupt is reset.

Two machine cycles are required for interrupt execution, one for saving the return address and one for jumping to the interrupt start address. If several interrupts occur simultaneously, all respective request flags are set, and the interrupt with the highest priority is processed. The remaining interrupts are pending until serviced by reenabling the master interrupt flip-flop or until their interrupt request flags are reset by executing a SKI instruction.

Figure 10 is a block diagram of the interrupt control circuit.

Figure 10. Interrupt Control Circuit Block Diagram



FIP Controller/Driver

The FIP controller/driver consists of 60 4-bit nibbles of display memory (000-03BH of data RAM), a 4-bit display mode register (DM_3-DM_0), a 4-bit timing mode register (TM_3-TM_0), a 4-bit blanking mode register (BM_3-BM_0), an output selector, and a high voltage output driver. See figure 11.

The FIP controller/driver has 24 outputs for directly driving a high voltage vacuum fluorescent display:

- 8 segment signal outputs (S_0-S_7)
- 8 timing signal (grid) outputs (T_0-T_7)
- 8 timing or segment outputs (T_8/S_8-T_{15}/S_{15}

The content of the display mode register determines which of five display modes is available to the user. The modes are as follows:

- Static mode
  - — 24 static output
- Dynamic mode
  - — 8 segment mode
  - — 12 segment mode I
  - — 12 segment mode II
  - — 16 segment mode

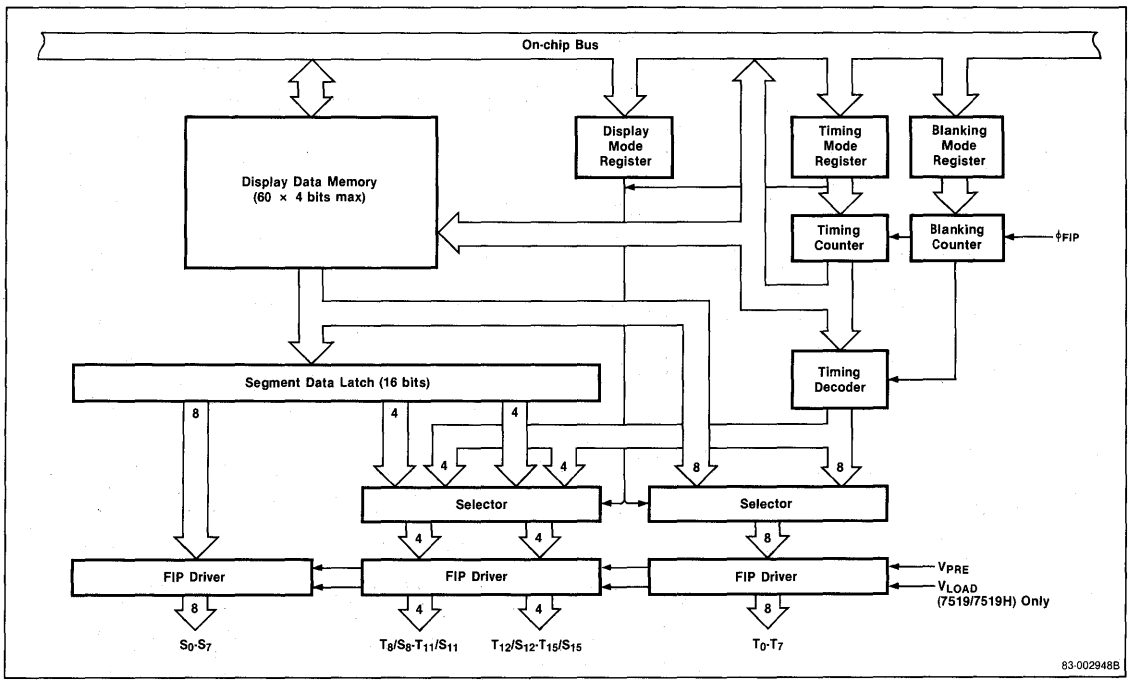
The content of the timing mode register determines the number of display digits (1-16), and controls the number of timing signals (T_0-T_{15}) output. Timing signals drive the grids of vacuum fluorescent display tubes. The voltage on the grid will determine the brightness of a digit (made up of one or more segments) or if the digit will be turned on or off.

The width of the timing signal pulse can be adjusted at eight independent steps by the value loaded into the blanking mode register. This function is useful for dimming control and for preventing display cross-talk of adjacent digits.

The active level of the timing signal can be designated high or low by bit DM_3.

3

Figure 11. FIP Controller/Driver Block Diagram



Display Mode Register (DM)

This 4-bit write-only register (DM_3-DM_0) determines the display mode (dynamic, static, and off) of the FIP controller/driver. It also determines the active level of the display timing signals. This is shown in figure 12.

The DM register has an output address of 0BH and is accessed by the output instructions OP and OPL when bit EM_3 of the expansion mode register is set. The DM register is cleared by a RESET.

Figure 13 shows a display example in 12 segment mode I.

Figure 12. Display Mode Register Format

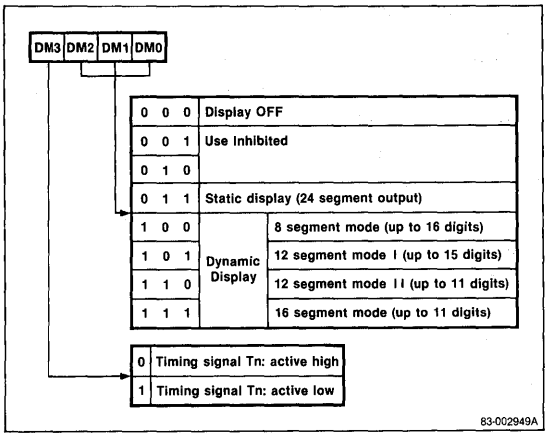
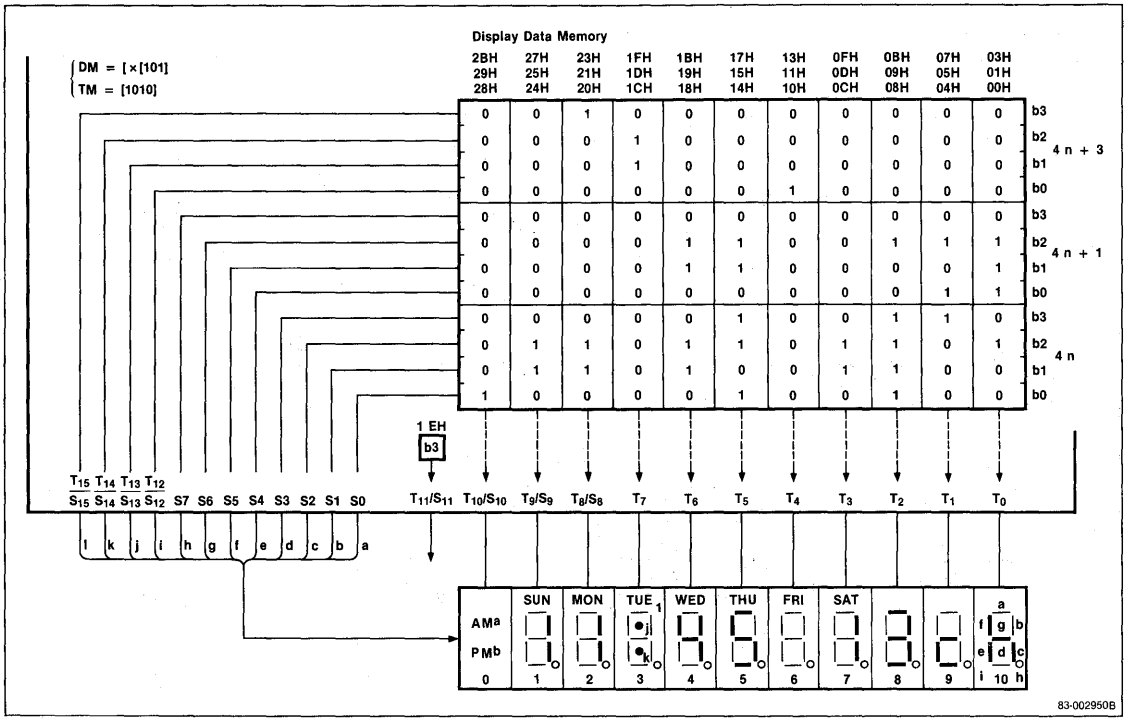


Figure 13. Display Example in 12 Segment Mode I



Standby Function

Two standby modes, stop and halt, hold device power consumption to a minimum. Stop mode is entered via the STOP instruction, and halt mode is entered via the HALT instruction. In stop mode, all clocks are stopped. In halt mode, only the CPU clock (ϕ) is stopped.

Stop mode can only be released by a RESET. Halt mode may be released either by a RESET or by the setting of an interrupt request flag.

Stop Mode

In stop mode, the contents of memory are retained, and all other functions are stopped. RESET releases stop mode.

In stop mode, the X1 input is internally shorted to V_{SS} in order to hold the crystal oscillator leakage to a minimum. A system using stop mode cannot use an external clock.

Halt Mode

When no interrupt flags are set, the HALT instruction causes the device to enter halt mode. In this mode, only ϕ stops; all other clocks continue to operate. The following functions continue to operate:

- Clock oscillation
- Frequency division and output of clocks other than ϕ
- Event input
- Timer/event counter
- Serial interface (except when ϕ is used as SCK)
- FIP controller/driver
- PPG
- Interrupts (INT0, INTS, INTT, INT1)
- RESET

Since a set interrupt flag releases the device from halt mode, this mode cannot be entered if an interrupt request flag is set. It is therefore necessary to reset the request flag(s) either by answering the interrupt(s) (setting the interrupt master enable F/F and process interrupt) or by executing the SKI instruction.

In halt mode, CPU power consumption is eliminated. To hold power consumption to a minimum, all unnecessary circuits should be inactive and the steps below should be taken:

- Set the system clock (CL) to low speed
- Set the FIP controller/driver to the off mode
- Set the PPG for static operation
- Stop $\overline{SCK}$ input

Low Supply Voltage Data Retention (μPD7519/7519H only)

Data retention is possible with V_{DD} as low as 2 V. V_{DD} should be lowered after the device is put in stop mode, and while RESET is inactive. Stop mode cannot be released in low voltage data retention mode; V_{DD} should first be raised to normal operation.

Release of Stop Mode

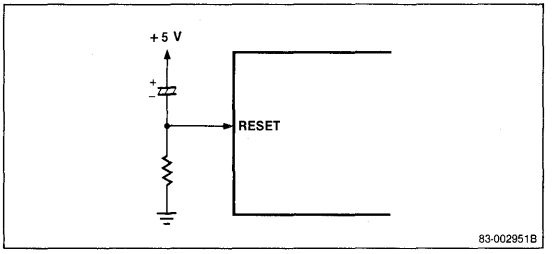
RESET releases stop mode. On RESET's rising edge, the device mode changes to halt mode, starting clock oscillation. At the falling edge of RESET, a waiting time (about 62.5 ms/4.19 MHz, 40 ms/6.55 MHz) elapses, allowing for stabilization of crystal operation, following which halt mode is released. After normal RESET operation, the CPU begins program execution from address 0000H.

In the release operation, the contents of data memory are retained while the contents of other registers become undefined.

Power-on Reset Circuit

An example of the simplest power-on reset circuit using a resistor and capacitor is show in figure 14.

Figure 14. Power-on Reset Circuit



Application

The μPD7519/7519H has a variety of flexible powerful functions and is best suited for the following applications:

- Video tape recorders
- Plain paper copiers
- Electronic cash registers
- Telephone sets
- Electronic scales
- Automobiles

Figures 15-18 show how to apply the device to a digital tuning system, a telephone, an ECR, and automotive equipment.

Figure 15. Digital Tuning System Application

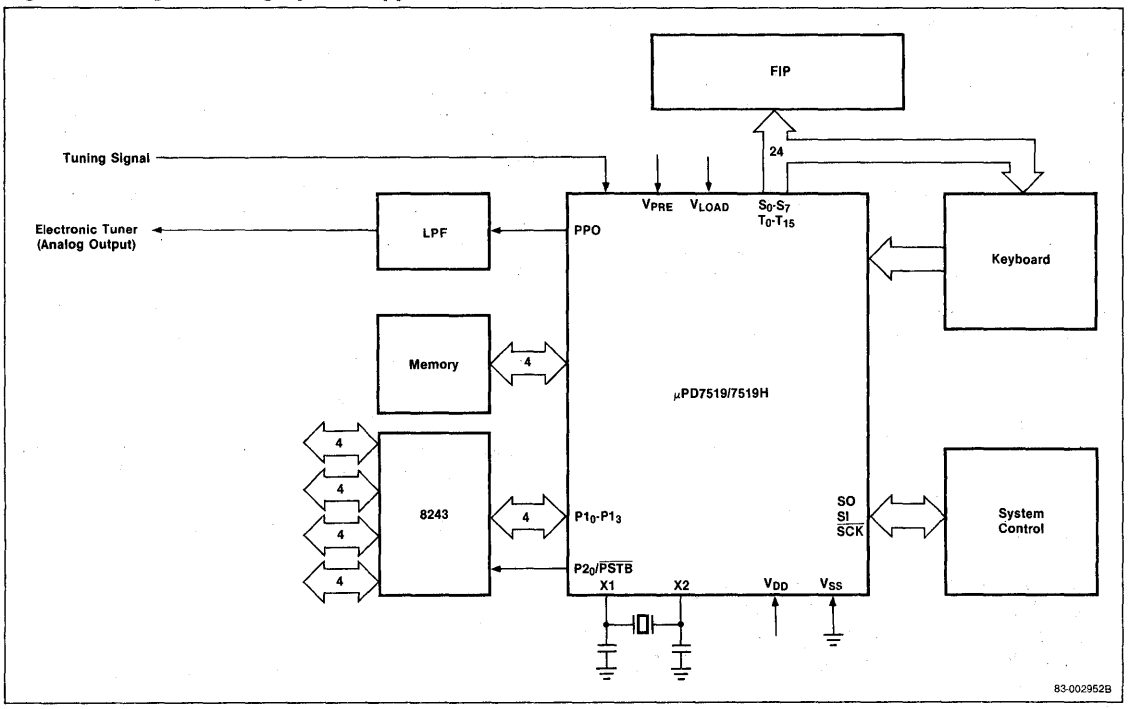


Figure 16. Telephone Application

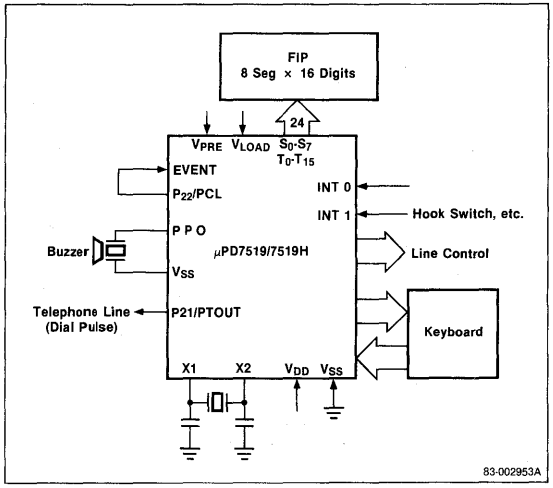


Figure 17. ECR Application

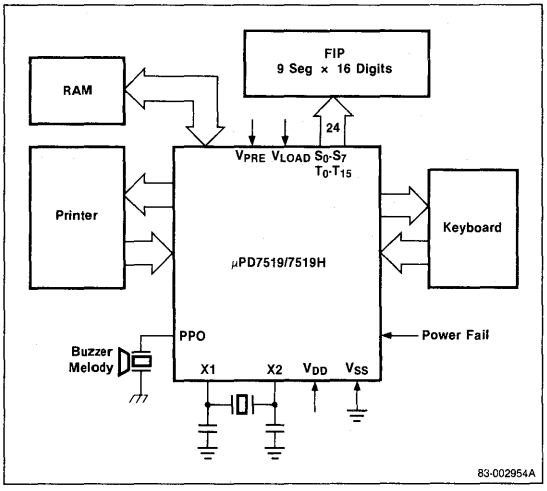
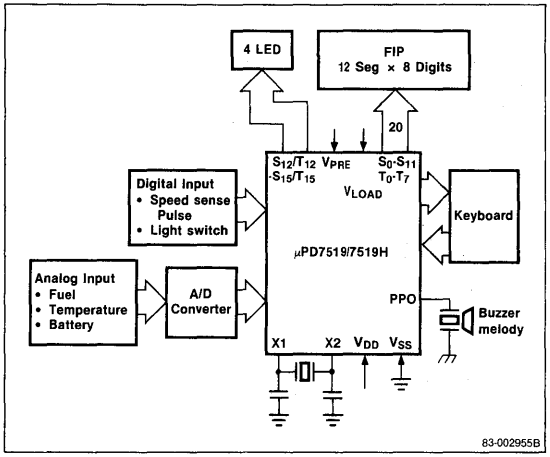


Figure 18. Automotive Equipment Application



3

Absolute Maximum Ratings

T_A = 25°C

Supply voltages, V_{DD}	−0.3 V to +7 V
V_{LOAD} (μPD7519/7519H)	(V_{DD} − 40) to (V_{DD} + 0.3)
V_{PRE}	(V_{DD} − 12) to (V_{DD} + 0.3)
Input voltage, V_I	−0.3 V to (V_{DD} + 0.3)
Output voltage, Display outputs, V_O	(V_{DD} − 40) to (V_{DD} + 0.3)
Other outputs, V_{OD}	−0.3 V to (V_{DD} + 0.3)
Output current high, I_{OH}	
Per pin, other than display outputs	−15 mA
Per pin, S_0-S_7	−15 mA
Per pin, T_0-T_7, T_8/S_8-T_{15}/S_{15}	−30 mA
Total, display outputs, μPD7519/7519H	−120 mA
Display outputs, μPD75CG19/75CG19H	−90 mA
Total, other than display outputs	−20 mA
Output current low, I_{OL}	
Per pin	17 mA
Total, all output ports	60 mA
Total power consumption (1), PT Plastic flat package (μPD7519/7519H)	400 mW
Plastic QUIP, (μPD7519/7519H)	600 mW
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:

(1) Calculation of PT: There are three kinds of power consumption, the total of which should be less than the total power consumption (PT) in this specification. Use of less than 80% of PT is recommended. The three different power consumptions are as follows:

1. CPU power consumption. V_{DD}(max) × I_{DD1}(max)
2. Power consumption of output pins. This includes both normal output and display output. Calculate the total consumption of each output pin to which the maximum current flows.
3. Power consumption of on-chip pull-down resistors (mask option).

Example

Configuration:

9 segments × 11 digits, 4 LED outputs
V_{DD} = 5 V ± 10%, 4.19 MHz oscillation
Segment pin = 5 mA (max)
Timing pin = 15 mA (max)
LED output pin = 10 mA (max)
Vacuum fluorescent display (V_{LOAD}) = −30 V

Consumption:

(1) CPU
5.5 V × 2.0 mA = 11 mW
(2) Output pins
Segment pins: (5/7 × 2 V) × 5 mA × 9 = 64 mW
Timing pins: 2 V × 15 mA = 30 mW
LED output pins: (10/15 × 2 V) × 10 mA × 4 = 53 mW
(3) Pull-down resistors
$(30 + 5.5\ V)^2/80\ k\Omega \times 10 = 158$ mW

Therefore, PT = (1) + (2) + (3) = 316 mW

Capacitance

T_A = 25°C; V_{DD} = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	f_C = 1 MHz Unmeasured pins are connected to 0 V
Output capacitance, Display outputs	C_O			35	pF	
Other outputs				15	pf	
I/O capacitance	C_{IO}			15	pF	

Operating Supply Voltages

T_A = −10°C to +70°C

Parameter	Limits Min	Max	Unit	Test Conditions	
CPU (1) μPD7519/ 75CG19	4.0	6.0	V	f_X = 0.4 MHz to 4.2 MHz	High speed mode, EM2 = 1
	2.5	6.0	V	f_{XX} = 3.5 MHz to 4.2 MHz	
					Low speed mode, EM2 = 0
CPU (1) μPD7519H/ 75CG19H	4.5	6.0	V	f_X, f_{XX} = 4.2 MHz to 6.6 MHz	High speed mode, EM2 = 1
	4.0	6.0	V	f_X = 0.1 MHz to 4.2 MHz f_{XX} = 3.5 MHz to 4.2 MHz	
	4.5	6.0	V	f_X, f_{XX} = 4.2 MHz to 6.6 MHz	Low speed mode, EM2 = 0
	2.5	6.0	V	f_X = 0.1 MHz to 4.2 MHz f_{XX} = 3.5 MHz to 4.2 MHz	
Crystal oscillation circuit (2) μPD7519/ 75CG19	2.7	6.0	V	C_1 = 10 pF $C_2 \leq$ 10 pF	Crystal Oscillator
	2.85	6.0	V	C_1 = 10 pF $C_2 \leq$ 22 pF	
	2.5	6.0	V		External clock
Crystal oscillation circuit (2) μPD7519H/ 75CG19H	4.5	6.0	V	f_{XX} = 4.2 MHz to 6.6 MHz C_1 = 10 pF, $C_2 \leq$ 10 pF	Crystal Oscillator
	2.7	6.0	V	C_1 = 10 pF, $C_2 \leq$ 10 pF f_{XX} = 3.5 MHz to 4.2 MHz	
	2.85	6.0	V	C_1 = 10 pF, $C_2 \leq$ 22 pF f_{XX} = 3.5 MHz to 4.2 MHz	
	2.6	6.0	V		External clock
Display controller	4.0	6.0	V		
PPG	4.0	6.0	V		
Port 1	2.5	6.0	V	Port output mode	
	4.0	6.0	V	I/O expander mode	

Note:

(1) Except the crystal oscillation circuit, display controller, PPG, and port 1.

(2) The circuits in figures 19 and 20 are recommended.

3

DC Characteristics

$T_A = -10°C$ to $+70°C$
μPD7519/7519H: V_{DD} = 2.5 V to 6 V; μPD75CG19/75CG19H: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Other than X1, X2
	V_{IH2}	V_{DD} −0.4		V_{DD}	V	X1, X2 (1)
Input voltage low	V_{IL1}	0		0.3 V_{DD}	V	Other than X1, X2
	V_{IL2}	0		0.4	V	X1, X2 (1)
Output voltage high	V_{OH}	V_{DD} −1.0			V	V_{DD} = 5 V ± 10%, I_{OH} = −1 mA
		V_{DD} −0.5			V	μPD7519/19H only, I_{OH} = −100 μA
Output voltage low	V_{OL}			0.4	V	V_{DD} = 5 V ± 10%, I_{OL} = 1.6 mA;
				0.5	V	μPD7519/19H only, I_{OL} = 400 μA
Input leakage current high	I_{LIH1}			3	μA	$V_I = V_{DD}$; other than X1, X2
	I_{LIH2}			20	μA	$V_I = V_{DD}$; X1, X2
Input leakage current low	I_{LIL1}			−3	μA	V_I = 0 V; other than X1, X2
	I_{LIL2}			−20	μA	V_I = 0 V; X1, X2
Input leakage current	I_{IL}			−200	μA	μPD75CG19H only V_I = 0 V, $I_0 - I_7$
Output leakage current high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current low	I_{LOL1}			−3	μA	V_O = 0 V; other than display outputs
	I_{LOL2}			−10	μA	$V_O = V_{LOAD} = V_{DD}$−35 V; display outputs
Display output current	I_{OD}	−7			mA	S_0-S_7 $V_{PRE} = V_{DD}$−9 V ± 1 V(2)
		−4			mA	μPD75CG19/75CG19H $V_{OD} = V_{DD}$−2 V, V_{DD} = 4 V to 6 V
		−15			mA	T_0-T_{15}
		−10			mA	μPD75CG19/75CG19H
		−3			mA	S_0-S_7 V_{PRE} = 0 V
		−2			mA	μPD75CG19/75CG19H $V_{OD} = V_{DD}$ −2 V, V_{DD} = 4 V to 6 V
		−7			mA	T_0-T_{15}
		−5			mA	μPD75CG19/75CG19H
On-chip pull-down resistance, μPD7519	R_L	80	140	220	kΩ	$V_{OD} - V_{LOAD}$ = 35 V
On-chip pull-down resistance, μPD7519H	R_L	40	70	120	kΩ	$V_{OD} - V_{LOAD}$ = 35 V

DC Characteristics (cont)

T_A = −10°C to +70°C
μPD7519/7519H: V_{DD} = 2.5 V to 6 V; μPD75CG19/75CG19H: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply current, μPD7519 (3)	I_{DD1}		600	2000	μA	High speed V_{DD} = 5 V ± 10% 4.19 MHz crystal C1 = C2 = 10 pF
			200	700	μA	Low speed V_{DD} = 3 V ± 10%
	I_{DD2}		260	800	μA	Low speed halt mode V_{DD} = 5 V ± 10%
			120	400	μA	Low speed halt mode V_{DD} = 3 V ± 10%
	I_{DD3}		0.1	10	μA	Stop mode
Supply current, μPD75CG19 (3)	I_{DD1}		700	2000	μA	High speed 4.19 MHz crystal C1 = C2 = 10 pF
	I_{DD2}		350	800	μA	Low speed halt mode V_{DD} = 5 V ± 10%
Supply current, μPD7519H (3)	I_{DD1}		2.0	6.0	mA	High speed 6.55 MHz crystal
	I_{DD2}		0.6	1.9	mA	Halt mode C1 = C2 = 10 pF V_{DD} = 5 V ± 10
	I_{DD1}		1.3	4.0	mA	High speed 4.19 MHz crystal V_{DD} = 5 V ± 10% C1 = C2 = 10 pF
			250	800	μA	Low speed V_{DD} = 3 V ± 10%
	I_{DD2}		450	1500	μA	Low speed halt mode V_{DD} = 5 V ± 10%
			150	400	μA	Low speed halt mode V_{DD} = 3 V ± 10%
	I_{DD3}		0.1	20	μA	V_{DD} = 5 V ± 10% Stop mode
			0.1	10	μA	V_{DD} = 3 V ± 10%
Supply current, μPD75CG19H (3)	I_{DD1}		1.2	3.6	mA	High speed V_{DD} = 5 V ± 10% 6.55 MHz crystal C1 = C2 = 10 pF
			1.0	3.0	mA	High speed halt mode V_{DD} = 4.75 to 5.5 V 4.19 MHz crystal C1 = C2 = 10 pF
	I_{DD2}		350	1000	μA	Low speed halt mode V_{DD} = 5 V ± 10% 4.19 MHz crystal C1 = C2 = 10 pF
	I_{DD3}			20	μA	V_{DD} = 5 V ± 10% Stop mode

Note:

(1) The circuits in figures 19 and 20 are recommended.

(2) The external circuit in figure 21 is recommended.

(3) The display controller and PPG are not operated.

3

Figure 19. Crystal

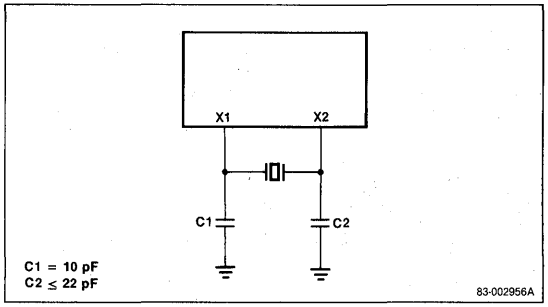


Figure 20. External Clock

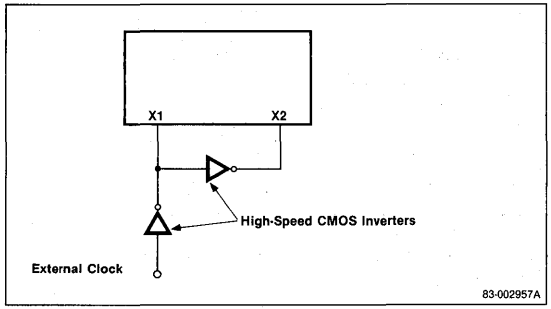
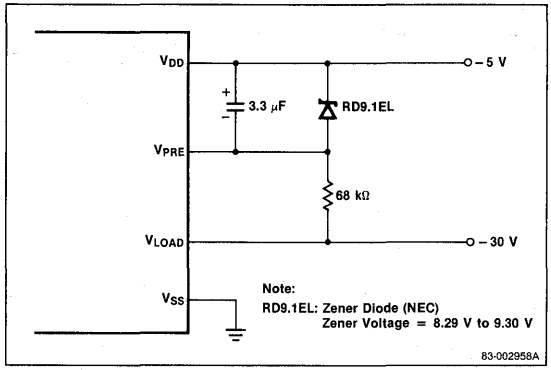


Figure 21. External Circuit



AC Characteristics

T_A = −10°C to +70°C

Clock Operation, μPD7519/75CG19

μPD7519: V_{DD} = 2.5 V to 6 V
μPD75CG19: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency	f_{XX}	3.5	4.19	4.2	MHz	Crystal oscillation (1), (2)
System clock input frequency	f_X	0.1		5	MHz	External clock (1)
X1, X2 input pulse width high and low	t_{XH}	100			ns	External clock (1)
	t_{XL}	100			ns	
EVENT input frequency	f_E			410	kHz	V_{DD} = 4.0 V to 6.0 V
				80	kHz	μPD7519 only
EVENT input pulse width high, low	t_{EL}	1.2			μs	V_{DD} = 4.0 V to 6.0 V
	t_{EH}	6.25			μs	μPD7519 only

Note:

(1) The circuits in figures 19 and 20 are recommended.

(2) Refer to the Operating Supply Voltages tables.

Clock Operation, μPD7519H/75CG19H

μPD7519H: V_{DD} = 2.5 V to 6 V
μPD75CG19H: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency	f_{XX}	3.5	4.19	4.2	MHz	Crystal oscillation (1), (2)
		4.2	6.55	6.6	MHz	V_{DD} = 4.5 V to 6.0 V
System clock input frequency	f_X	0.1		4.2	MHz	External clock (1)
		4.2		6.6	MHz	V_{DD} = 4.5 V to 6.0 V
X1, X2 input pulse width high, low	t_{XH}	100			ns	External clock (1)
	t_{XL}	75			ns	V_{DD} = 4.5 V to 6.0 V
EVENT input frequency	f_E			410	kHz	V_{DD} = 4.0 V to 6.0 V
				80	kHz	μPD7519H only
EVENT Input pulse width high, low	t_{EL}	6.25			μs	V_{DD} = 4.0 V to 6.0 V
						μPD7519H only

Note:

(1) The circuits in figures 19 and 20 are recommended.

(2) Refer to the Operating Supply Voltages table.

AC Characteristics (cont)

T_A = −10°C to +70°C

Port 1 I/O Operation, μPD7519/75CG19

μPD7519: V_{DD} = 2.5 V to 6 V
μPD75CG19: V_{DD} = 5 V ± 10%
0.1 MHz ≤ f_x, f_{xx} ≤ 4.2 MHz

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Port 1 output setup time (to $\overline{PSTB}$↑)	t_{PST}	400		ns	Port output mode
Port 1 output hold time (after $\overline{PSTB}$↑)	t_{STP}	100		ns	
$\overline{PSTB}$ pulse width low	t_{STL1}	600		ns	
Output data set-up time (to $\overline{PSTB}$↑)	t_{DST}	400		ns	I/O expander mode V_{DD} = 4 V to 6 V
Output data hold time (after $\overline{PSTB}$↑)	t_{STD}	100		ns	
Input data valid time (after $\overline{PSTB}$↓)	t_{STDV}		850	ns	
Input data floating time (after $\overline{PSTB}$↑)	t_{STDF}	0		ns	
Control set-up time (to $\overline{PSTB}$↓)	t_{CST}	400		ns	
Control hold time	t_{STC}				
Output command		100		ns	
Input command		0	80	ns	
$\overline{PSTB}$ pulse width low	t_{STL2}	1200		ns	

Port 1 I/O Operation, μPD7519H/75CG19H

μPD7519H: V_{DD} = 2.5 V to 6 V
μPD75CG19H: V_{DD} = 5 V ± 10%
0.1 MHz ≤ f_x, f_{xx} ≤ 4.2 MHz

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Port 1 output setup time (to $\overline{PSTB}$↑)	t_{PST}	250		ns	Port output mode
Port 1 output hold time (after $\overline{PSTB}$↑)	t_{STP}	100		ns	
$\overline{PSTB}$ pulse width low	t_{STL1}	450		ns	
Output data set-up time (to $\overline{PSTB}$↑)	t_{DST}	200		ns	I/O expander mode V_{DD} = 4 V to 6 V
Output data hold time (after $\overline{PSTB}$↑)	t_{STD}	100		ns	
Input data valid time (after $\overline{PSTB}$↓)	t_{STDV}		700	ns	
Input data floating time (after $\overline{PSTB}$↑)	t_{STDF}	0		ns	
Control set-up time (to $\overline{PSTB}$↓)	t_{CST}	100		ns	
Control hold time	t_{STC}				
Output command		100		ns	
Input command		0	80	ns	
$\overline{PSTB}$ pulse width low	t_{STL2}	750		ns	

AC Characteristics (cont)

T_A = −10°C to +70°C

Port 1 I/O Operation, μPD7519H/75CG19H

μPD7519H: V_{DD} = 4.5 V to 6 V
μPD75CG19H: V_{DD} = 4.75 V to 5.5 V
4.2 MHz ≤ f_x, f_{xx} ≤ 6.6 MHz, Low Speed Mode(1) (EM_2 = 0)

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Port 1 output setup time (to $\overline{PSTB}$↑)	t_{PST}	400		ns	Port output mode
Port 1 output hold time (after $\overline{PSTB}$↑)	t_{STP}	100		ns	
$\overline{PSTB}$ pulse width low	t_{STL1}	600		ns	
Output data set-up time (to $\overline{PSTB}$↑)	t_{DST}	400		ns	I/O expander mode V_{DD} = 4 V to 6 V
Output data hold time (after $\overline{PSTB}$↑)	t_{STD}	100		ns	
Input data valid time (after $\overline{PSTB}$↓)	t_{STDV}		850	ns	
Input data floating time (after $\overline{PSTB}$↑)	t_{STDF}	0		ns	
Control set-up time (to $\overline{PSTB}$↓)	t_{CST}	400		ns	
Control hold time	t_{STC}				
Output command		100		ns	
Input command		0	80	ns	
$\overline{PSTB}$ pulse width low	t_{STL2}	1200		ns	

Note:

(1) The μPD82C43/8243H, etc, cannot interface with the μPD7519H in high speed mode (EM_2 = 1).

AC Characteristics (cont)

T_A = −10°C to +70°C

Serial Interface Operation, μPD7519/75CG19

μPD7519: V_{DD} = 2.5 V to 6 V
μPD75CG19: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{KCY}	3.0		μs	Input V_{DD} = 4 V to 6 V
		12.5		μs	μPD7519 only
		4.9		μs	Output V_{DD} = 4 V to 6 V
		10		μs	μPD7519 only
$\overline{SCK}$ pulse width high, low	t_{KH}	1.3		μs	Input V_{DD} = 4 V to 6 V
	t_{KL}	65		μs	μPD7519 only
		2.2		μs	Output V_{DD} = 4 V to 6 V
		4.5		μs	μPD7519 only
SI set-up time (to $\overline{SCK}$↑)	t_{SIK}	300		ns	V_{DD} = 4 V to 6 V
		1000		ns	μPD7519 only
SI hold time (after $\overline{SCK}$↑)	t_{KSI}	450		ns	V_{DD} = 4 V to 6 V
		1000		ns	μPD7519 only
SO output delay time (after $\overline{SCK}$↓)	t_{KSO}		850	ns	V_{DD} = 4 V to 6 V
			2000	ns	μPD7519 only

AC Characteristics (cont)

T_A = −10°C to +70°C

Serial Interface Operation, μPD7519H/75CG19H

μPD7519: V_{DD} = 2.5 V to 6 V
μPD75CG19: V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{KCY}	2.1		μs	Input V_{DD} = 4 V to 6 V
		12.5		μs	μPD7519H only
		(1)		μs	Output V_{DD} = 4 V to 6 V
		(2)		μ	μPD7519H only
$\overline{SCK}$ pulse width high, low	t_{KH}	0.7		μs	Input V_{DD} = 4 V to 6 V
	t_{KL}	6.5		μs	μPD7519H only
		(3)		μs	Output V_{DD} = 4 V to 6 V
		(4)		μs	μPD7519H only
SI set-up time (to $\overline{SCK}$↑)	t_{SIK}	300		ns	V_{DD} = 4 V to 6 V
		1000		ns	μPD7519H only
SI hold time (after $\overline{SCK}$↑)	t_{KSI}	450		ns	V_{DD} = 4 V to 6 V
		1000		ns	μPD7519H only
SO output delay time (after $\overline{SCK}$↓)	t_{KSO}		500	ns	V_{DD} = 4 V to 6 V
			2000	ns	μPD7519H only

Note:

(1) High speed mode: $16/f_X$ or $16/f_{XX}$
Low speed mode: $64/f_X$ or $64/f_{XX}$

(2) $64/f_X$ or $64/f_{XX}$

(3) High speed mode: $8/f_X$ − 0.8 μs, or $8/f_{XX}$ − 0.8 μs
Low speed mode: $32/f_X$ − 0.8 μs, or $32/f_{XX}$ − 0.8 μs

(4) $32/f_X$ − 2.0 μs, or $32/f_{XX}$ − 2.0 μs

AC Characteristics (cont)

T_A = −10°C to +70°C

Other Operations

μPD7519/7519H: V_{DD} = 4.5 V to 6.0 V
μPD75CG19/75CG19H: V_{DD} = 4.75 V to 5.5 V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
INT0 pulse width high, low	t_{I0H}, t_{I0L}	10		μs	
INT1 pulse width high, low	t_{I1H}, t_{I1L}	(1)		μs	
RESET pulse width high, low	t_{RSH}, t_{RSL}	10		μs	

Note:

(1) $26/f_X$ or $26/f_{XX}$

μPD75CG19/75CG19H EPROM Characteristics

T_A = −10°C to +70°C; V_{DD} = 5 V ± 10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Access time	t_{ACC}			700	ns	
$\overline{CE}$ low set-up time to data valid	t_{CE}			700	ns	
Data valid hold time to $\overline{CE}$ rising edge	t_{IH}	0			ns	

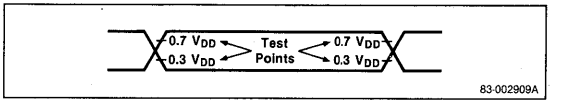
Stop Mode Low Voltage Data Retention Characteristics, μPD7519/7519H

T_A = −10°C to +70°C

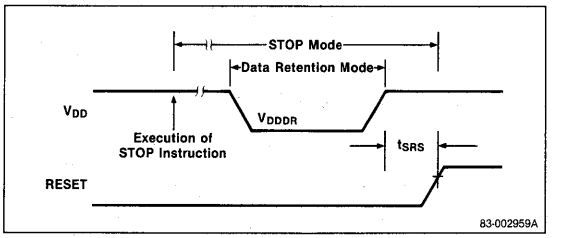
Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		6.0	V	
Data retention supply current	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2 V
RESET set-up time	t_{SRS}	0			μs	

Timing Waveforms

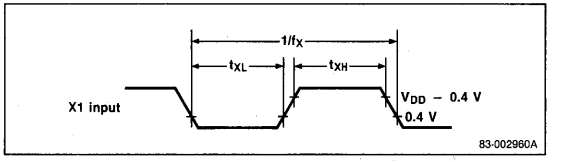
AC Waveform Measurement Points (Except X1, X2)



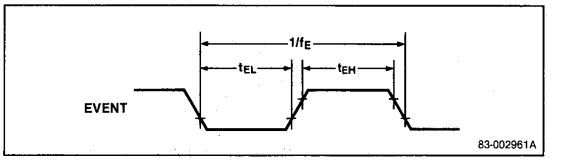
Data Retention Timing



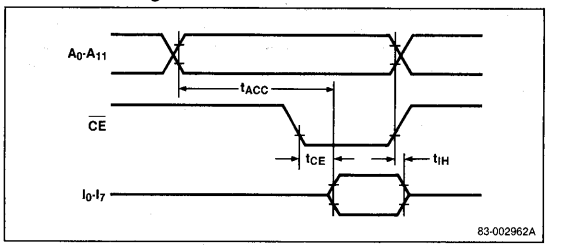
Clock Timing



EVENT Timing

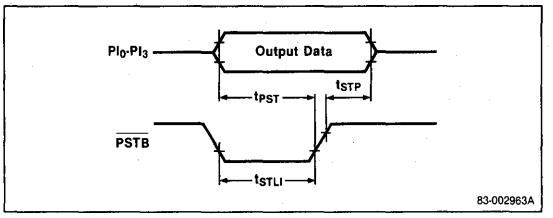


EPROM Timing

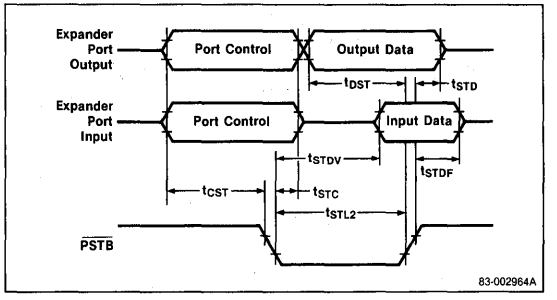


Timing Waveforms (cont)

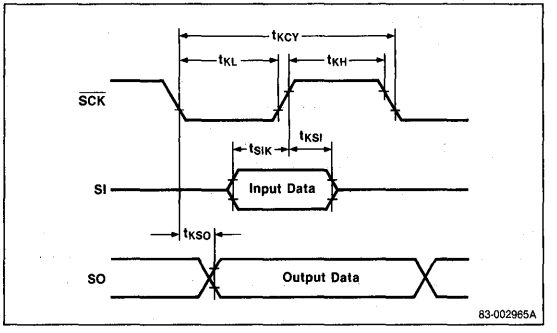
Strobe Output Timing



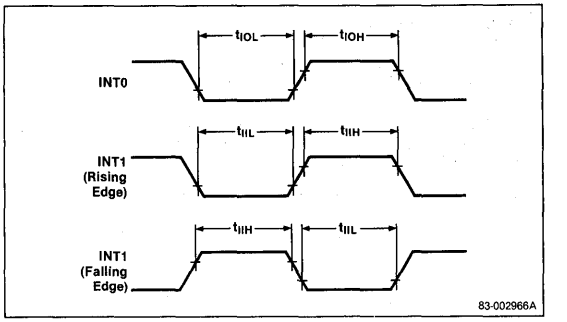
Port 1 I/O Expander I/O Timing



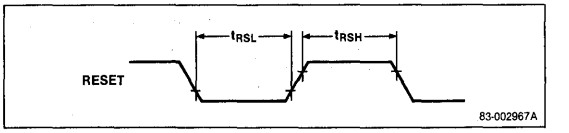
Serial Transfer Timing



Interrupt Input Timing



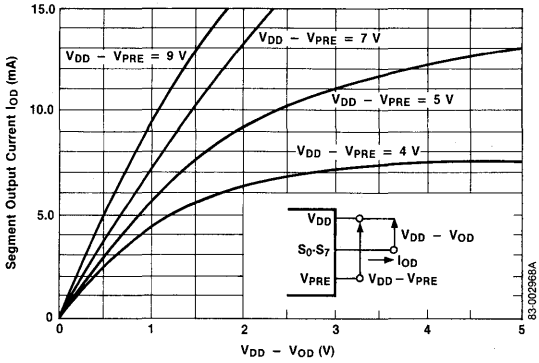
RESET Input Timing



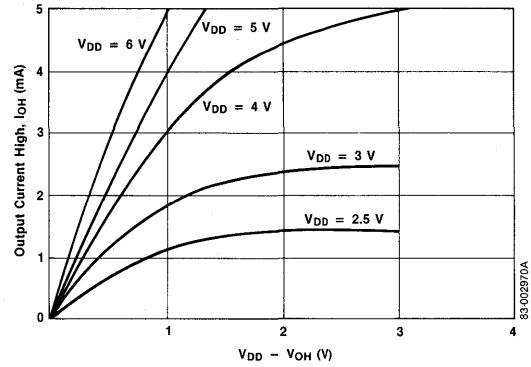
Operating Characteristics, μPD7519/7519H

T_A = 25°C

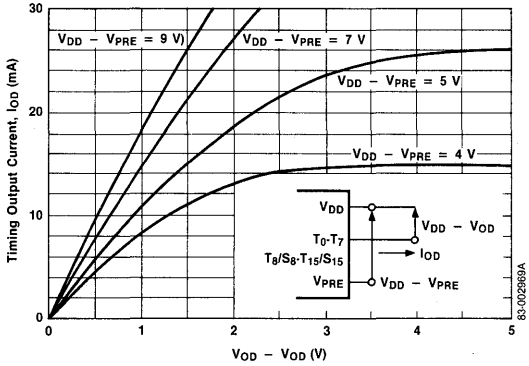
I_{OD} vs (V_{DD} – V_{OD}) (V_{DD} = 4 V to 6 V)



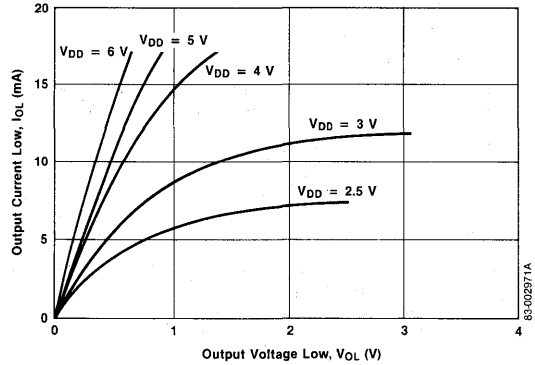
I_{OH} vs (V_{DD} – V_{OH})



I_{OD} vs (V_{DD} – V_{OD}) (V_{DD} = 4 to 6 V)



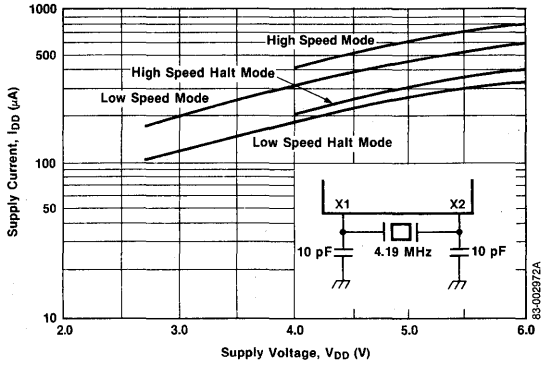
I_{OL} vs V_{OL}



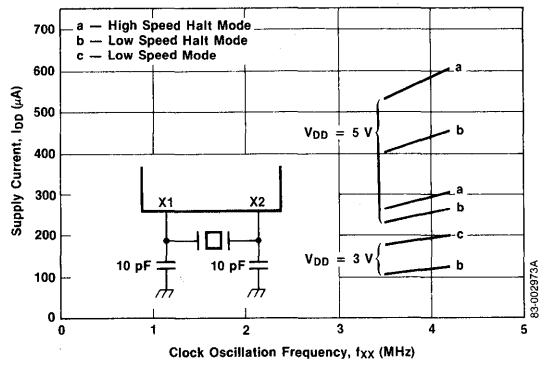
Operating Characteristics, μPD7519H only

T_A = 25°C

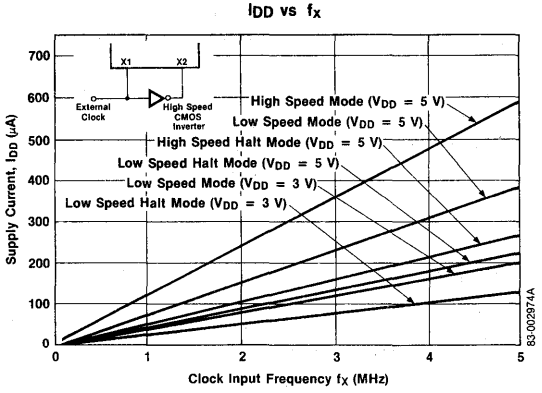
I_{DD} vs V_{DD} (f_{XX} = 4.19 MHz)



I_{DD} vs f_{XX}



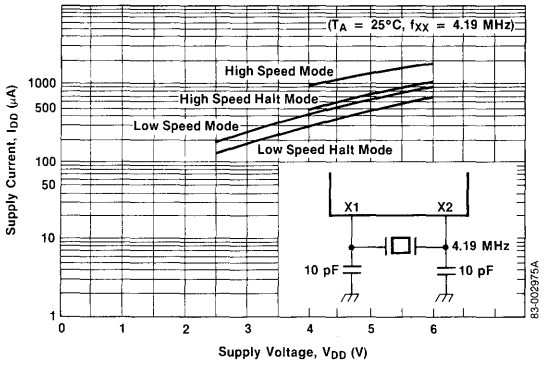
I_{DD} vs f_X



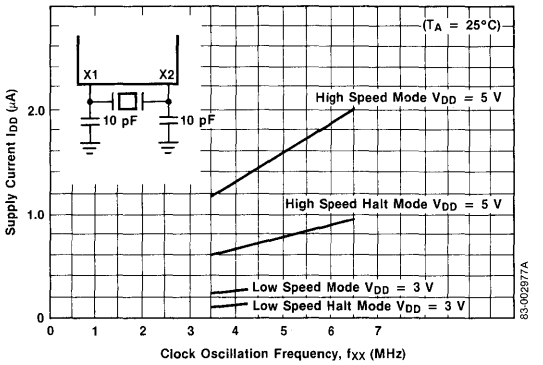
Operating Characteristics, μPD7519 only

T_A = 25°C

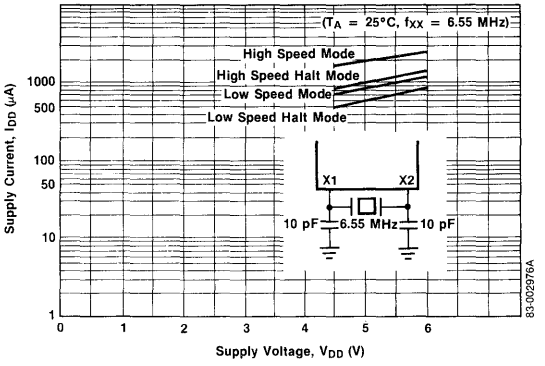
I_{DD} vs V_{DD}



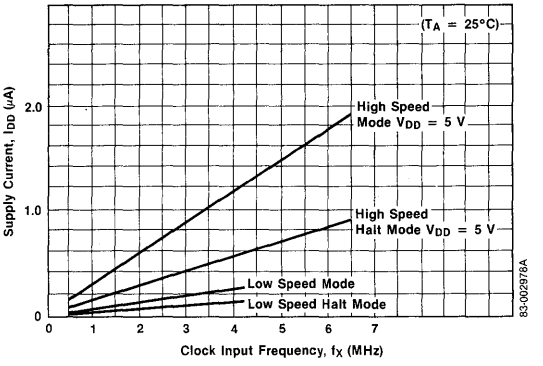
I_{DD} vs f_{XX}



I_{DD} vs V_{DD}



I_{DD} vs f_X



3

μPD7527A/28A
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS WITH FIP® DRIVER

Description

The μPD7527A, μPD7528A, and μPD75CG28 are 4-bit, single-chip CMOS microcomputers with the μPD7500 architecture and FIP direct-drive capability.

Note: This data sheet pertains to μPD7527A, μPD7528A, and μPD75CG28. For simplification, the revision letter (A) usually is omitted from the part numbers within the data sheet.

The μPD7527 contains a 2048 × 8-bit ROM and a 128 × 4-bit RAM. The μPD7528 contains a 4096 × 8-bit ROM and a 160 × 4-bit RAM.

The μPD7527/28 contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater depth and flexibility. The μPD7527/28 typically executes 67 instructions with a 5 μs instruction cycle time.

The μPD7527/28 has one external and two internal edge-triggered hardware-vectored interrupts. It also contains an 8-bit timer/event counter and an 8-bit serial interface to help reduce software requirements.

Thirty-one high-voltage lines are organized into the 3-bit output port 2, the 4-bit output ports 3, 8, and 9, and the 4-bit I/O ports 4, 5, 10, and 11.

The low power consumption CMOS process allows the use of a power supply between 2.7 and 6.0 V. Current consumption is less than 3.0 mA maximum, and can be further reduced in the halt and stop power-down modes.

The μPD75CG28 is a piggyback EPROM version of the μPD7527/28. Pin-compatible and function-compatible with the final, masked versions of the μPD7527/28, the μPD75CG28 is used for prototyping and for aiding in program development.

Features

- ☐ 67 instructions
- ☐ Instruction cycle:
  - — Internal clock: 5 μs/400 kHz, 5 V
  - — External clock: 4 μs/500 kHz, 5 V
- ☐ Upwardly compatible with the μPD7500 series product family
- ☐ 4,096 × 8-bit ROM (μPD7528/75CG28)
  2,048 × 8-bit ROM (μPD7527)
- ☐ 160 × 4-bit RAM (μPD7528/75CG28)
  128 × 4-bit RAM (μPD7527)
- ☐ 35 I/O lines
- ☐ 31 high-voltage output lines that can directly drive a vacuum fluorescent display (FIP)
- ☐ Can select either a pull-down resistor or open-drain output per 31 high-voltage outputs (mask optional)
- ☐ Vectored interrupts: one external, two internal
- ☐ 8-bit timer/event counter
- ☐ 8-bit serial interface
- ☐ Standby function (HALT, STOP)
- ☐ Data retention mode
- ☐ Zero-cross detector on $P0_0$/INT0 input (mask optional)
- ☐ System clock (μPD7527/7528/75CG28): on-chip RC oscillator
- ☐ CMOS technology
- ☐ Low power consumption
- ☐ Single power supply
  - — μPD7527/7528: 2.7 to 6.0 V
  - — μPD75CG28: 5.0 V

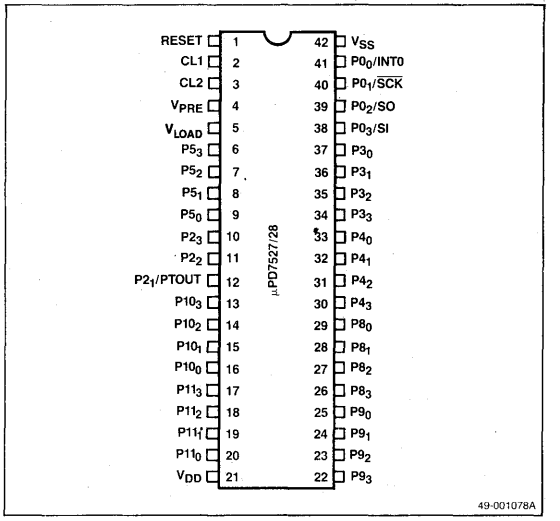
FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7527AC / 28AC	42-pin plastic DIP	610 kHz
μPD7527ACU / 28ACU	42-pin plastic shrink DIP	610 kHz
μPD75CG28E	42-pin ceramic piggyback DIP	500 kHz

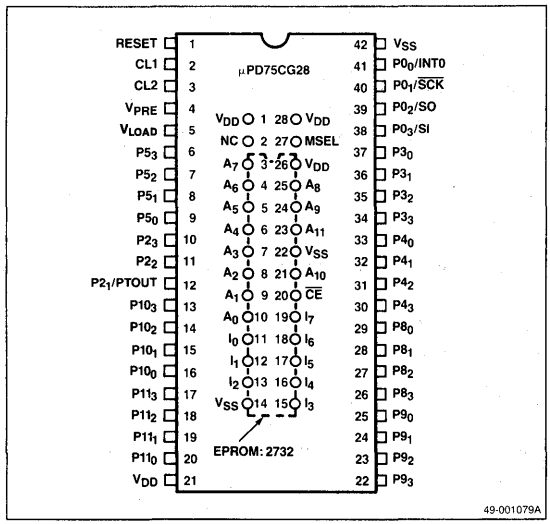
Pin Configurations

μPD7527/28, 42-Pin Plastic DIP or Shrink DIP



Pin Configurations (cont)

μPD75CG28, 42-Pin Ceramic Piggyback DIP



Pin Identification

μPD7527/28 and μPD75CG28

No.	Symbol	Function
1	RESET	Reset input
2, 3	CL1, CL2	Clock pins
4	V_{PRE}	High-voltage predriver supply
5	V_{LOAD}	High-voltage option resistor supply
6–9	$P5_0$–$P5_3$	High-voltage I/O port 5
10, 12	$P2_3$, $P2_2$ $P2_1$/PTOUT	High-voltage output port 2, and output port from timer/event counter (PTOUT)
13–16	$P10_0$–$P10_3$	High-current, high-voltage I/O port 10
17–20	$P11_0$–$P11_3$	High-voltage, high-current I/O port 11
21	V_{DD}	Positive power supply
22–25	$P9_0$–$P9_3$	High-voltage, high-current output port 9
26–29	$P8_0$–$P8_3$	High-voltage, high-current output port 8
30–33	$P4_0$–$P4_3$	High-voltage I/O port 4
34–37	$P3_0$–$P3_3$	High-voltage output port 3
38 39 40 41	$P0_3$/SI $P0_2$/SO $P0_1$/$\overline{SCK}$ $P0_0$/INT0	4-bit input of port 0; or serial data input (SI), serial data output (SO), serial clock I/O ($\overline{SCK}$), and external interrupt input (INT0) or zero-cross detect input ($P0_0$).
42	V_{SS}	Ground

μPD75CG28 EPROM

No.	Symbol	Function
1	V_{DD}	Connection to pin 21 of μPD75CG28
2	NC	No connection
3–10, 21, 24, 25	A_0–A_{10}	EPROM address output
11–13, 15–19	I_0–I_7	Data read input from the EPROM
14	V_{SS}	Connection to EPROM GND pin
20	$\overline{CE}$	Chip enable output
22	V_{SS}	Supplies EPROM $\overline{OE}$ signal
23	A_{11}	Program counter MSB output
26	V_{DD}	Supplies V_{CC} to the EPROM
27	MSEL	Mode select input
28	V_{DD}	Supplies high-level signal to MSEL

Note:

(1) Output drivers on ports 2–5 and 8–11 are mask-optional. Accordingly, either an open-drain output or a pull-down resistor can be selected. V_{LOAD} is suitable for an output driver with a pull-down resistor.

(2) Ports 2–5 are suitable as FIP segment signal outputs, and ports 8–11 are suitable for FIP digit signal outputs.

(3) Ports 8–11 have high-current drive capability and can drive an LED directly.

Pin Functions, μPD7527/28 and μPD75CG28

RESET

System reset (input).

CL1, CL2

Connection to the RC oscillator. CL1 is the external clock input.

V_{PRE}

Negative power supply for high-voltage output predrivers (for ports 2–5, 8–11).

V_{LOAD}

Negative power supply for optional load resistors (pull-down resistors) of high-voltage output drivers (for ports 2–5, 8–11). This pin is only on the μPD7527/28.

$P5_3$–$P5_0$

4-bit, high-voltage I/O port 5.

$P2_1$–$P2_3$

3-bit, high-voltage output port 2.

PTOUT

Output port from the timer/event counter.

$P10_3$-$P10_0$

4-bit, high-voltage, high-current I/O port 10. Capable of bit set/reset by SPBL/RPBL instructions.

$P11_3$-$P11_0$

4-bit, high-voltage, high-current I/O port 11. Capable of bit set/reset by SPBL/RPBL instructions.

V_{DD}

Positive power supply.

$P9_3$-$P9_0$

4-bit, high-voltage, high-current output port 9. Capable of bit set/reset by SPBL/RPBL instructions.

$P8_3$-$P8_0$

4-bit, high-voltage, high-current output port 8. Capable of bit set/reset by SPBL/RPBL instructions.

$P4_3$-$P4_0$

4-bit, high-voltage I/O port 4.

$P3_3$-$P3_0$

4-bit, high-voltage output port 3.

$P0_0$-$P0_3$

4-bit input port 0. $P0_0$ is also used as the zero-cross detection input.

SI

Serial data input.

SO

Serial data output.

$\overline{SCK}$

I/O serial clock.

INT0

External interrupt input.

V_{SS}

Ground.

Pin Functions, μPD75CG28 EPROM

MSEL

Changes the addressing area of the external EPROM and the on-chip RAM (with a pull-down resistor). Connecting a jumper between socket pins 27 (MSEL) and 28 (V_{DD}) selects μPD7527 mode (2-Kbyte EPROM, 128 × 4-bit RAM). Leaving MSEL open selects μPD7528 mode (4-Kbyte EPROM, 160 × 4-bit RAM).

A_0-A_{10}

Output the low-order 11 bits of the program counter (PC_0-PC_{10}). Used as EPROM address signals.

A_{11}

When MSEL is high level, A_{11} outputs high-level signals. When MSEL is open, A_{11} outputs the MSB of the PC, which is used as the most significant address signal of the 4-Kbyte EPROM 2732.

I_0-I_7

Input data read from the EPROM.

$\overline{CE}$

Outputs the chip enable signal to the EPROM.

V_{DD}

Pin 26 is electrically equivalent to the bottom V_{DD} pin and is used to supply V_{CC} to the EPROM. Pin 28 is electrically equivalent to the bottom V_{DD} pin and is used to supply the high level signal to MSEL. Pin 1 connects to pin 21 of μPD75CG28.

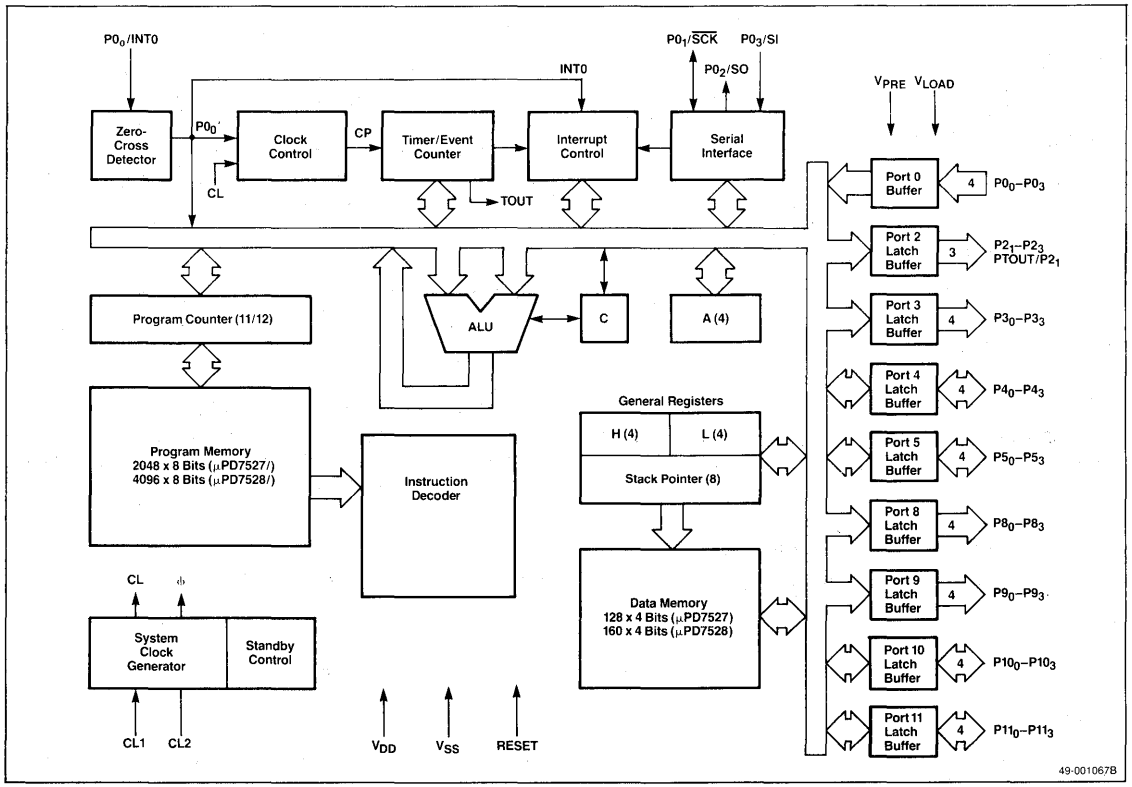
V_{SS}

Pin 14 is electrically equivalent to the bottom V_{SS} pin in voltage, and is connected to the EPROM GND pin. Pin 22 is electrically equivalent to the bottom V_{SS} pin and is used to supply the $\overline{OE}$ signal to the EPROM.

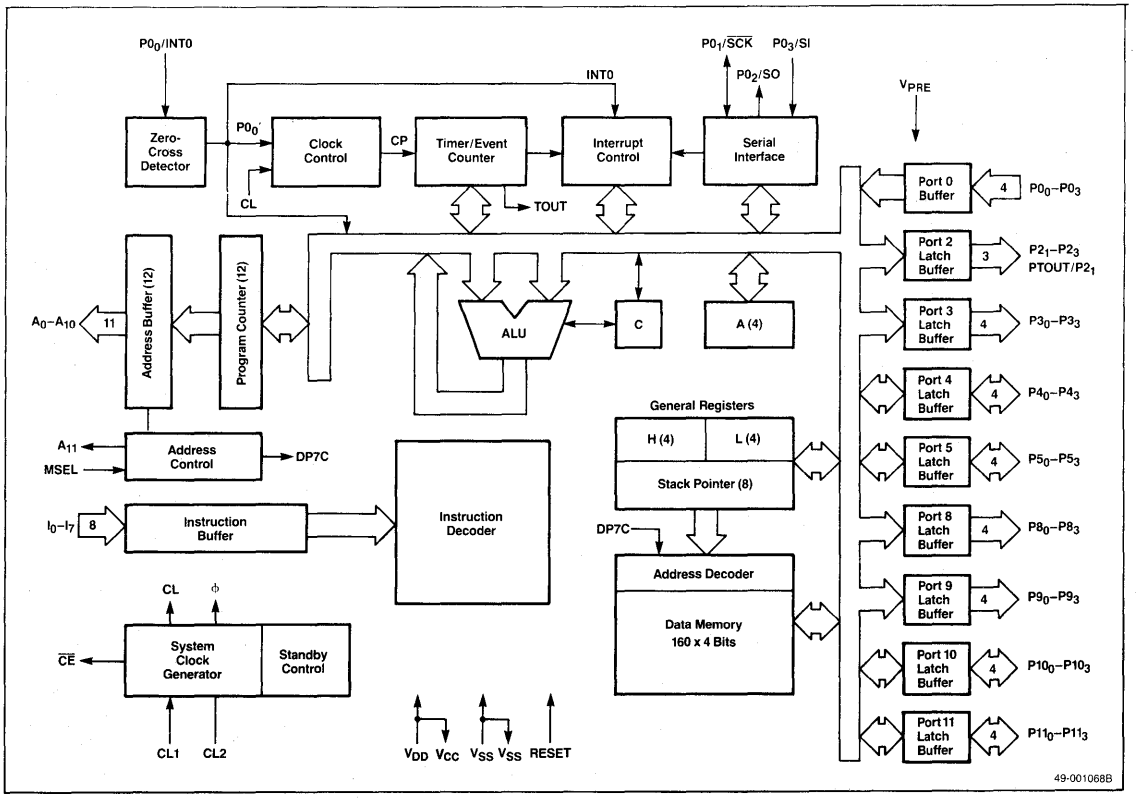
Instruction Set

Refer to the User's Manual. The instruction set appears also as subset A4 in the data sheet for the μPD7500 series of single-chip microcomputers.

Block Diagram, μPD7527/28



Block Diagram, μPD75CG28



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 to +7 V
Power supply voltage, V_{LOAD} (μPD7527 / 28)	V_{DD} −40 V to V_{DD} +0.3 V
Power supply voltage, V_{PRE}	V_{DD} −12 V to V_{DD} +0.3 V
Input voltage, except ports 4, 5, 10, 11, V_{IN}	−0.3 V to V_{DD} +0.3 V
Input voltage, ports 4, 5, 10, 11, V_{IN}	V_{DD} −40 V to V_{DD} +0.3 V
Output voltage, except ports 2–5, 8–11, V_O	−0.3 V to V_{DD} +0.3 V
Output voltage, ports 2–5, 8–11, V_O	V_{DD} −40 V to V_{DD} +0.3 V
Output current high, per pin: $P0_1$, $P0_2$; I_{OH}	−15 mA
Output current high, per pin: ports 2–5, 8–11; I_{OH}	−30 mA
Output current high, ports 3, 4, 8, 9 total, I_{OH}	−55 mA
Output current high, ports 2, 5, 10, 11 total, I_{OH}	−55 mA
Output current low, per pin, I_{OL}	15 mA
Output current low, all ports total, I_{OL}	15 mA
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

μPD7527/28

$T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, low	V_{IL1}	0		$0.3V_{DD}$	V	Port 0, RESET
	V_{IL2}	0		0.5	V	CL1
	V_{IL3}	$V_{DD}-35$		$0.3V_{DD}$	V	Ports 4, 5, 10, 11
Input voltage, high	V_{IH1}	$0.7V_{DD}$		V_{DD}	V	Port 0, RESET
	V_{IH2}	$V_{DD}-0.5$		V_{DD}	V	CL1
	V_{IH3}	$0.7V_{DD}$		V_{DD}	V	Ports 4, 5, 10, 11; $4.5V \leqslant V_{DD} \leqslant 6.0V$
		$V_{DD}-0.5$		V_{DD}	V	Ports 4, 5, 10, 11; $2.7V \leqslant V_{DD} \leqslant 4.5V$
Output voltage, low	V_{OL}			0.4	V	PO_1, PO_2; $4.5V \leqslant V_{DD} \leqslant 6.0V$; $I_{OL}=1.6$ mA
				0.5	V	PO_1, PO_2; $I_{OL}=400\,\mu A$
Output voltage, high	V_{OH}	$V_{DD}-2.0$			V	Ports 2–5, $I_{OH}=-4$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH}=-10$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 2–5, $I_{OH}=-2$ mA (Note 2)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH}=-5$ mA (Note 2)
		$V_{DD}-1.0$			V	PO_1, PO_2; $I_{OH}=-1$ mA (Note 3)
		$V_{DD}-0.5$			V	PO_1, PO_2; $I_{OH}=-100\,\mu A$
Input leakage current, low	I_{LIL1}			-3	μA	$V_{IN}=0$ V; PO_0–PO_3
	I_{LIL2}			-40	μA	$V_{IN}=0$ V; PO_0 (Note 5)
	I_{LIL3}			-10	μA	$V_{IN}=0$ V; CL1
	I_{LIL4}			-10	μA	$V_{IN}=V_{DD}-35$ V; ports 4, 5, 10, 11
Input leakage current, high	I_{LIH1}			3	μA	$V_{IN}=V_{DD}$; PO_0–PO_3 (Note 4)
	I_{LIH2}			40	μA	$V_{IN}=V_{DD}$; PO_0 (Note 5)
	I_{LIH3}			10	μA	$V_{IN}=V_{DD}$; CL1
	I_{LIH4}			80	μA	$V_{IN}=V_{DD}$; ports 4, 5, 10, 11

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output leakage current, low	I_{LOL1}			-3	μA	$V_O=0$ V; PO_1, PO_2
	I_{LOL2}			-10	μA	$V_O=V_{DD}-35$ V; ports 2–5, 8–11
Output leakage current, high	I_{LOH1}			3	μA	$V_O=V_{DD}$; except ports 4, 5, 10, 11
	I_{LOH2}			80	μA	$V_O=V_{DD}$; ports 4, 5, 10, 11
Supply current, normal operation	I_{DD1}		1.0	3.0	mA	$V_{DD}=5\,V\pm10\%$, $R=39\,k\Omega$
			0.4	1.0	mA	$V_{DD}=3$ V, $R=82\,k\Omega$
Supply current, HALT mode (Note 6)	I_{DD2}		200	600	μA	$V_{DD}=5\,V\pm10\%$, $R=39\,k\Omega$ (Note 4)
			60	200	μA	$V_{DD}=3$ V, $R=82\,k\Omega$ (Note 4)
			210	640	μA	$V_{DD}=5\,V\pm10\%$, $R=39\,k\Omega$ (Note 5)
			67	230	μA	$V_{DD}=3$ V, $R=82\,k\Omega$ (Note 5)
Supply current, STOP mode (Note 6)	I_{DD3}		0.1	10	μA	$V_{DD}=3$ V (Note 4)
			10	40	μA	$V_{DD}=5\,V\pm10\%$ (Note 5)
			7	30	μA	$V_{DD}=3$ V (Note 5)
On-chip pull-down resistance	R_L	80	140	220	kΩ	$V_{DD}-V_{LOAD}=35$ V

Note:

(1) $V_{PRE}=V_{DD}-9\,V+1\,V$. The circuit in figure 5 is recommended.

(2) $V_{PRE}=0$ V. $V_{DD}=4.5$ V to 6.0 V.

(3) $V_{DD}=4.5$ V to 6.0 V.

(4) Without zero-cross detector.

(5) With zero-cross detector.

(6) Ports 4, 5, 10, 11 are low level output or low level input.

DC Characteristics (cont)

μPD75CG28

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, low	V_{IL1}	0		$0.3V_{DD}$	V	Port 0, RESET
	V_{IL2}	0		0.5	V	CL1
	V_{IL3}	$V_{DD}-35$		$0.3V_{DD}$	V	Ports 4, 5, 10, 11
Input voltage, high	V_{IH1}	$0.7V_{DD}$		V_{DD}	V	Port 0, RESET
	V_{IH2}	$V_{DD}-0.5$		V_{DD}	V	CL1
	V_{IH3}	$0.7V_{DD}$		V_{DD}	V	Ports 4, 5, 10, 11
Output voltage, low	V_{OL}			0.4	V	PO_1, PO_2; $I_{OL}=1.6$ mA
				0.5	V	PO_1, PO_2; $I_{OL}=400\mu A$
Output voltage, high	V_{OH}	$V_{DD}-2.0$			V	Ports 2–5, $I_{OH}=-4$ mA (1)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH}=-10$ mA(1)
		$V_{DD}-2.0$			V	Ports 2–5, $I_{OH}=-2$ mA(2)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH}=-5$ mA(2)
		$V_{DD}-1.0$			V	PO_1, PO_2; $I_{OH}=-1$ mA
Input current, low (I_0–I_7)	I_{IL}			−200	μA	$V_{IN}=0V$
Input current, high (MSEL)	I_{IH}			300	μA	$V_{IN}=V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	$V_{IN}=0V$; $P0_0$–$P0_3$
	I_{LIL2}			−40	μA	$V_{IN}=0V$; $P0_0$
	I_{LIL3}			−10	μA	$V_{IN}=0V$; CL1
	I_{LIL4}			−10	μA	$V_{IN}=V_{DD}-35V$; ports 4, 5, 10, 11
Input leakage current, high	I_{LIH1}			3	μA	$V_{IN}=V_{DD}$; $P0_0$–$P0_3$
	I_{LIH2}			40	μA	$V_{IN}=V_{DD}$; $P0_0$
	I_{LIH3}			10	μA	$V_{IN}=V_{DD}$; CL1
	I_{LIH4}			80	μA	$V_{IN}=V_{DD}$; ports 4, 5, 10, 11
Output leakage current, low	I_{LOL1}			−3	μA	$V_O=0V$; PO_1, PO_2
	I_{LOL2}			−10	μA	$V_O=V_{DD}-35V$; ports 2–5, 8–11
Output leakage current, high	I_{LOH1}			3	μA	$V_O=V_{DD}$; except ports 4, 5, 10, 11
	I_{LOH2}			80	μA	$V_O=V_{DD}$; ports 4, 5, 10, 11
Supply current, normal operation	I_{DD1}		1.0	3.0	mA	R=39 kΩ
Supply current, HALT mode(3)	I_{DD2}		210	630	μA	R=39 kΩ
Supply current, STOP mode(3)	I_{DD3}		10	50	μA	

Note:

(1) $V_{PRE} = V_{DD} - 9V + 1V$. The circuit in figure 6 is recommended.

(2) $V_{PRE} = 0V$

(3) Ports 4, 5, 10, 11 are output off or low input.

Figure 1. Recommended Circuit, μPD7527/7528

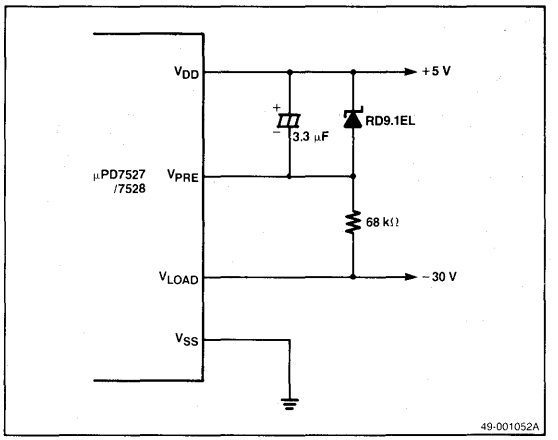
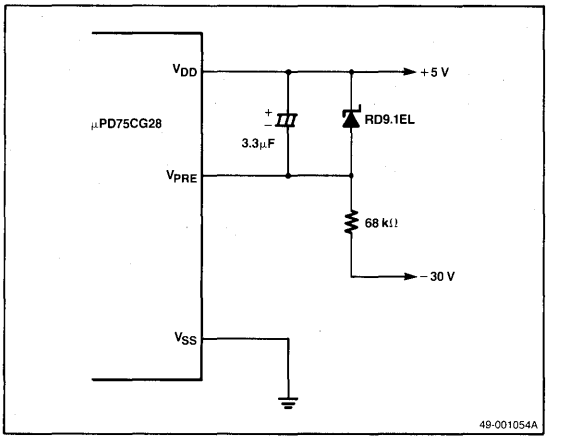


Figure 2. Recommended Circuit, μPD75CG28

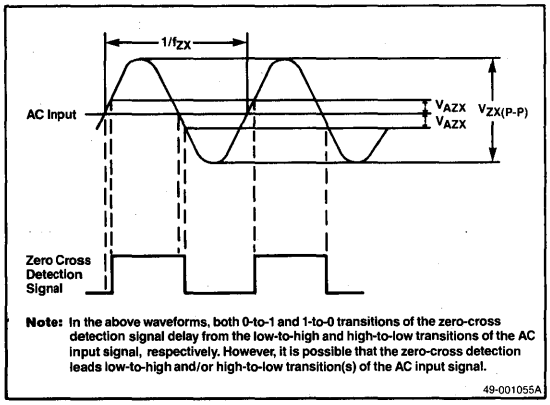


Zero-Cross Detection Characteristics

μPD7527/28: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.5$ V to 6.0 V
μPD75CG28: $T_A = -10°C$ to $+70°C$, $V_{DD} = +5$ V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Zero-cross detection input voltage	V_{ZX}(P-P)	1		3	V_{P-P}	AC coupled, C = 0.1 μF
Zero-cross accuracy	V_{AZX}			±100	mV	50 Hz to 60 Hz sine wave
Zero-cross detection input frequency	f_{ZX}	45		1000	Hz	

Zero-Cross Detection Waveform



Note: In the above waveforms, both 0-to-1 and 1-to-0 transitions of the zero-cross detection signal delay from the low-to-high and high-to-low transitions of the AC input signal, respectively. However, it is possible that the zero-cross detection leads low-to-high and/or high-to-low transition(s) of the AC input signal.

49-001055A

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V, f = 1.0 MHz, Unmeasured pins returned to GND

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	$P0_0$, $P0_3$
Output capacitance	C_O			15	pF	Port 2
				35	pF	Ports 3, 8, 9
I/O capacitance	C_{IO}			15	pF	$P0_1$, $P0_2$
				35	pF	Ports 4, 5, 10, 11

AC Characteristics

μPD7527/28

$T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Cycle time (Note 1)	t_{CY}	3.3		200	μs	V_{DD} = 4.5 V to 6.0 V
		6.9		200	μs	
$P0_0$ event input frequency	f_{P0}	0		610	kHz	V_{DD} = 4.5 V to 6.0 V
		0		290	kHz	
$P0_0$ input rise time	t_{P0R}			0.1	μs	
$P0_0$ input fall time	t_{P0F}			0.1	μs	
$P0_0$ input pulse width, low	t_{P0L}	1.63			μs	
$P0_0$ input pulse width, high	t_{P0H}	0.72			μs	V_{DD} = 4.5 V to 6.0 V
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	Input; V_{DD} = 4.5 V to 6.0 V
		3.3			μs	Output; V_{DD} = 4.5 V to 6.0 V
		8.0			μs	Input
		6.9			μs	Output
$\overline{SCK}$ pulse width, low	t_{KL}	3.9			μs	Input
		3.35			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	1.4			μs	Input; V_{DD} = 4.5 V to 6.0 V
		1.55			μs	Output; V_{DD} = 4.5 V to 6.0 V
SI set-up time (to rising-edge of $\overline{SCK}$)	t_{SIK}	300			ns	
SI hold time (after rising-edge of $\overline{SCK}$)	t_{KSI}	450			ns	
SO output delay time (after falling-edge of $\overline{SCK}$)	t_{KSO}			850	ns	V_{DD} = 4.5 V to 6.0 V
				1200	ns	
INT0 pulse width, high, low	t_{IOH}, t_{IOL}	10			μs	
RESET pulse width, high, low	t_{RSH}, t_{RSL}	10			μs	

AC Characteristics (cont)

μPD75CG28

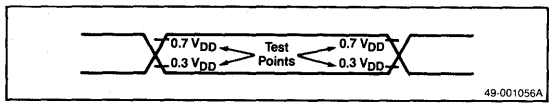
$T_A = -10°C$ to $+70°C$, $V_{DD} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Cycle time (Note 1)	t_{CY}	4.0		200	μs	
$P0_0$ event input frequency	f_{P0}	0		500	kHz	
$P0_0$ input rise time	t_{P0R}			0.2	μs	
$P0_0$ input fall time	t_{P0F}			0.2	μs	
$P0_0$ input pulse width, high, low	t_{P0H}, t_{P0L}	0.8			μs	
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	Input
		4.0			μs	Output
$\overline{SCK}$ pulse width, low	t_{KL}	1.8			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	1.3			μs	Input
SI set-up time (to rising-edge of $\overline{SCK}$)	t_{SIK}	300			ns	
SI hold time (after rising-edge of $\overline{SCK}$)	t_{KSI}	450			ns	
SO output delay time (after falling-edge of $\overline{SCK}$)	t_{KSO}			850	ns	
INT0 pulse width, high, low	t_{I0H}, t_{I0L}	10			μs	
RESET pulse width, high, low	t_{RSH}, t_{RSL}	10			μs	
Data input delay time from address	t_{ACC}			700	ns	
Data input delay time from $\overline{CE}$	t_{CE}			700	ns	
Input hold time after address	t_{IH}	0			ns	

Note:

(1) $t_{CY} = 2/f_{CC}$ or $2/f_C$

AC Waveform Measurement Points (Except CL1)



Oscillation Characteristics

μPD7527/28

$T_A = -10°C$ to $+70°C$, $V_{DD} = 2.7\,V$ to $6.0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency (Note 1)	f_{CC}	300	400	500	kHz	$R = 39\,k\Omega \pm 2\%$; $V_{DD} = 4.5\,V$ to $6.0\,V$
		110	150	190	kHz	$R = 110\,k\Omega \pm 2\%$
System clock CL1 input frequency (Note 2)	f_C	10		500	kHz	$V_{DD} = 4.5\,V$ to $6.0\,V$
		10		210	kHz	
CL1 input rise time (Note 2)	t_{CR}			0.2	μs	
CL1 input fall time (Note 2)	t_{CF}			0.2	μs	
CL1 input pulse width, low (Note 2)	t_{CL}	2.0		50	μs	
CL1 input pulse width, high (Note 2)	t_{CH}	0.8		50	μs	$V_{DD} = 4.5\,V$ to $6.0\,V$

μPD75CG28

$T_A = -10°C$ to $+70°C$, $V_{DD} = 5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency (Note 1)	f_{CC}	300	400	500	kHz	$R = 39\,k\Omega \pm 2\%$
		110	150	190	kHz	$R = 110\,k\Omega \pm 2\%$
System clock CL1 input frequency (Note 2)	f_C	10		500	kHz	
CL1 input rise time (Note 2)	t_{CR}			0.2	μs	
CL1 input fall time (Note 2)	t_{CF}			0.2	μs	
CL1 input pulse width, high, low	t_{CH}, t_{CL}	0.8		50	μs	

Note:

(1) R, C (see figure 3)

(2) External clock (see figure 4)

3

Figure 3. Recommended RC Oscillator Circuit

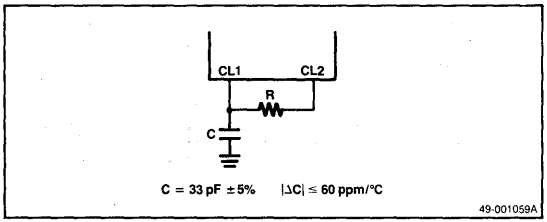
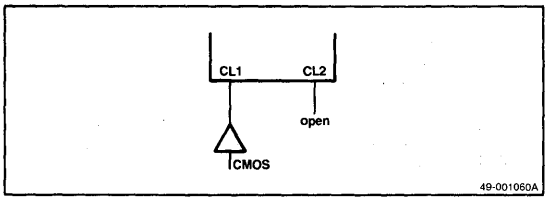


Figure 4. Recommended External Clock Circuit



Stop Mode Low Voltage Data Retention Characteristics

μPD7527/28

$T_A = -10°C$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		6.0	V	
Data retention supply current	I_{DDDR}		0.3	10	μA	V_{DDDR} = 2 V (Note 1)
			7	30	μA	V_{DDDR} = 2 V (Note 2)
Data retention RESET input voltage high	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} +0.2	V	
RESET set-up time	t_{SRS}	0			μs	
RESET hold time	t_{HRS}	0			μs	

μPD75CG28

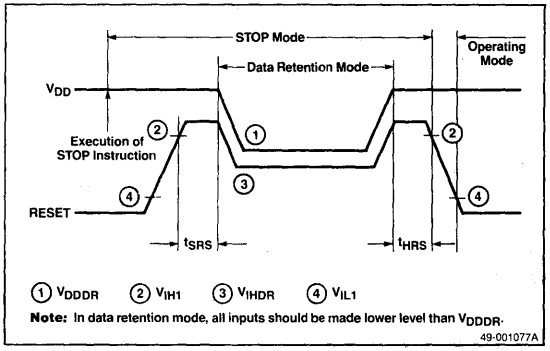
$T_A = -10°C$ to $+70°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		5.5	V	
Data retention supply current	I_{DDDR}		7	30	μA	V_{DDDR} = 2 V
Data retention RESET input voltage high	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} +0.2	V	
RESET set-up time	t_{SRS}	0			μs	
RESET hold time	t_{HRS}	0			μs	

Note:
(1) Without zero-cross detector

(2) With zero-cross detector

Data Retention Mode Timing



μPD75CG28 EPROM Interface

A 4-Kbyte EPROM (2732) plugs into socket pins on top of the μPD75CG28. A high input to MSEL selects μPD7527 mode and fixes the A_{11} output high level in order to access the upper 2-Kbytes of the 4-Kbyte EPROM. When MSEL is open, μPD7528 mode is selected. All EPROM addresses can be accessed because A_{11} functions as the MSB of the address. Figure 5 shows the address control unit. Figures 6 and 7 show the μPD75CG28 connected with the 2732.

Figure 8 shows the EPROM read timing. Data is read into the instruction buffer at the end of the T4 state. The chip enable ($\overline{CE}$) signal is made active during 2 states (T3, T4) in order to decrease the power consumption of the EPROM.

Figure 5. Address Control Unit

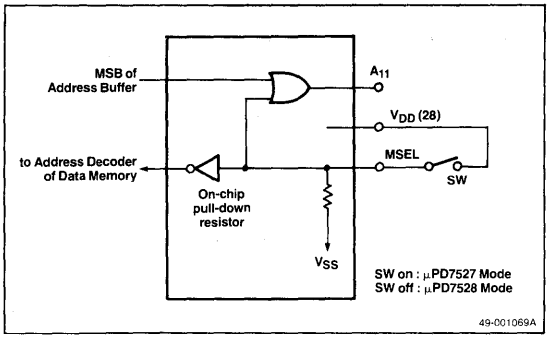


Figure 6. Connection with the 2732 (μPD7527 Mode)

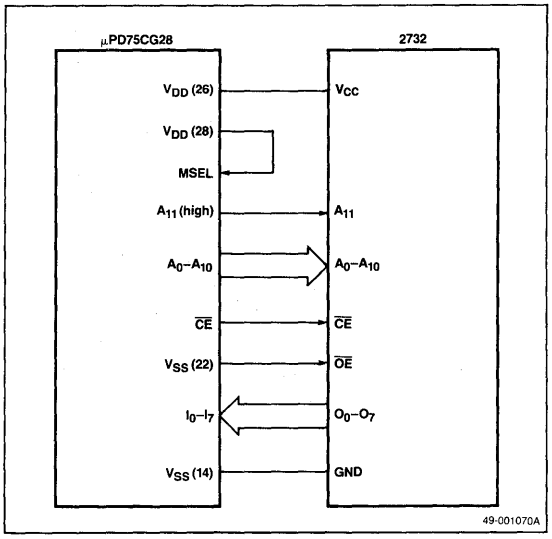


Figure 7. Connection with the 2732 (μPD7528 Mode)

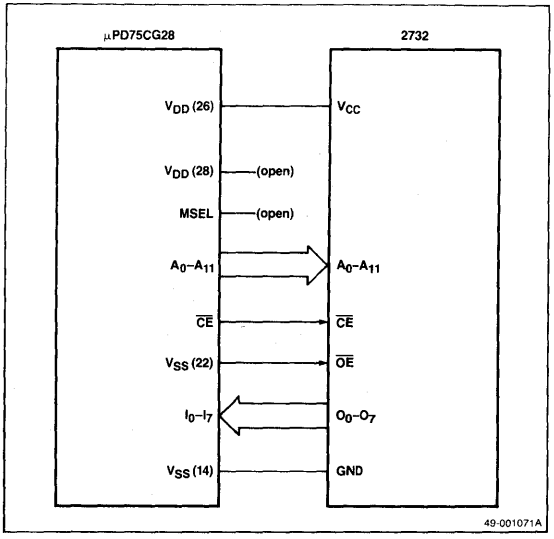
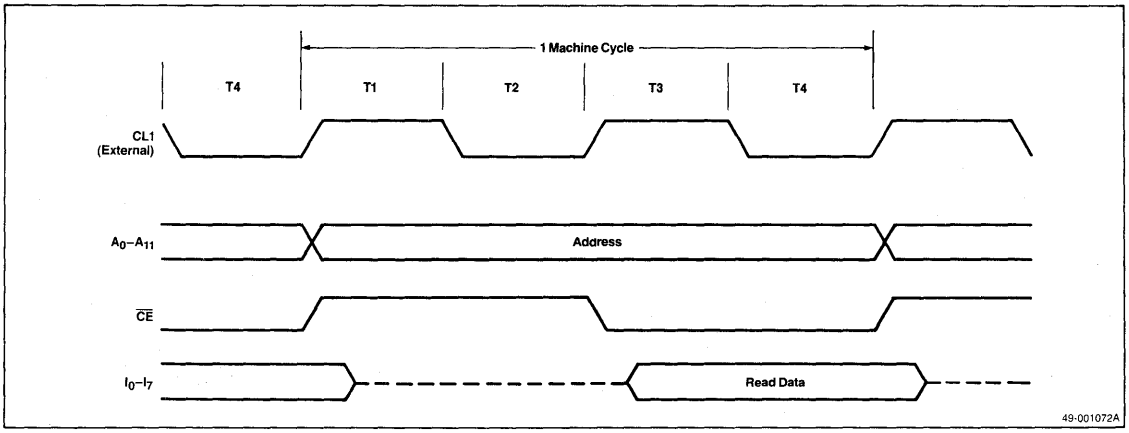
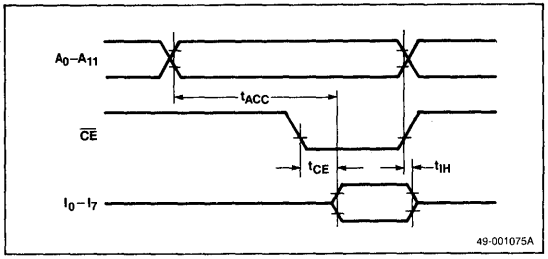


Figure 8. EPROM Read Timing

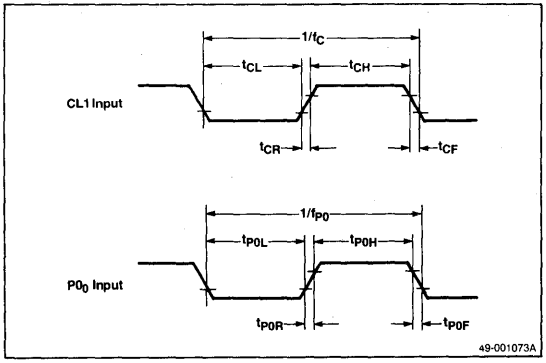


Timing Waveforms

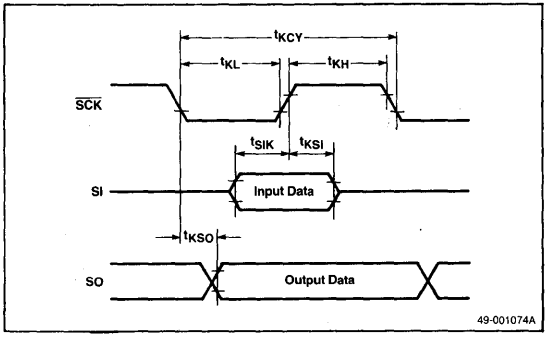
EPROM (μPD75CG28 only)



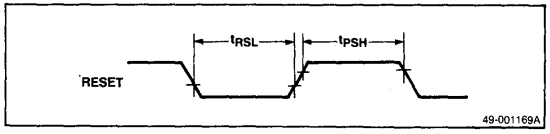
Clock



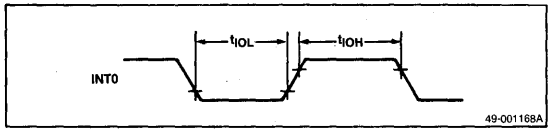
Serial Interface



Interrupt Input

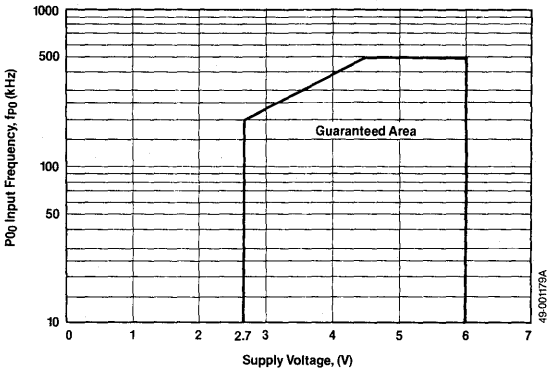


Reset Input

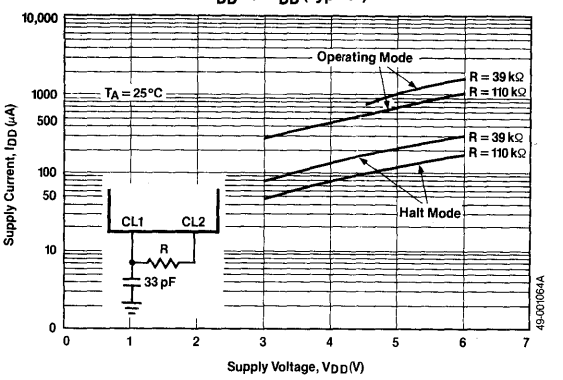


Operating Characteristics

f_{P0} vs V_{DD}

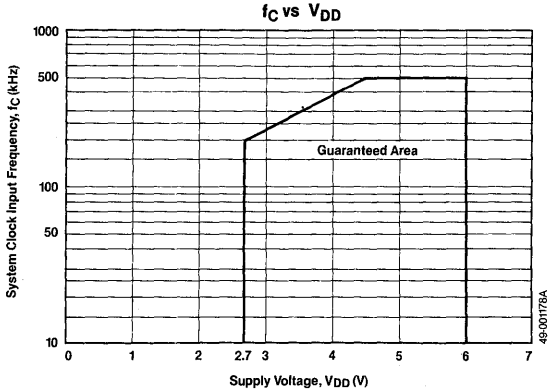


I_{DD} vs V_{DD} (Typical)

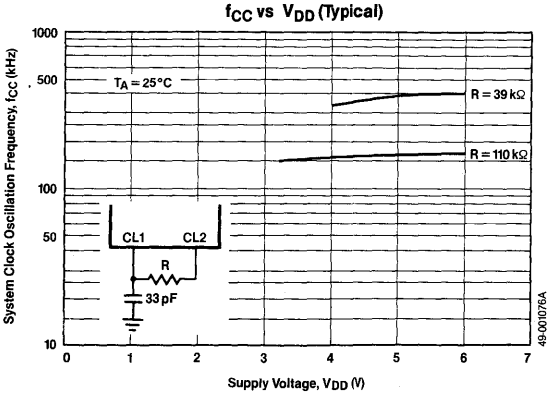


3

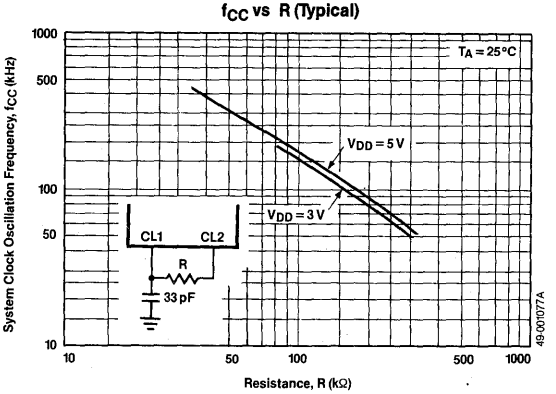
f_C vs V_{DD}



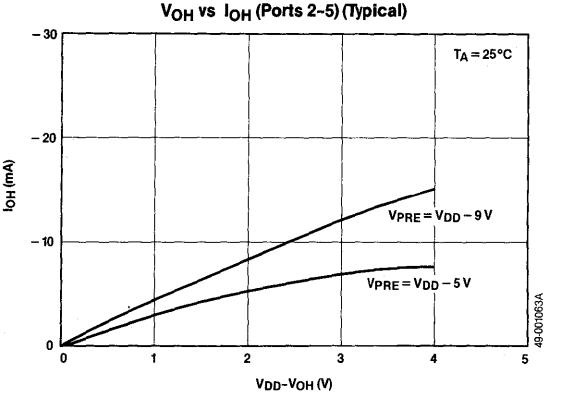
f_{CC} vs V_{DD} (Typical)



f_{CC} vs R (Typical)

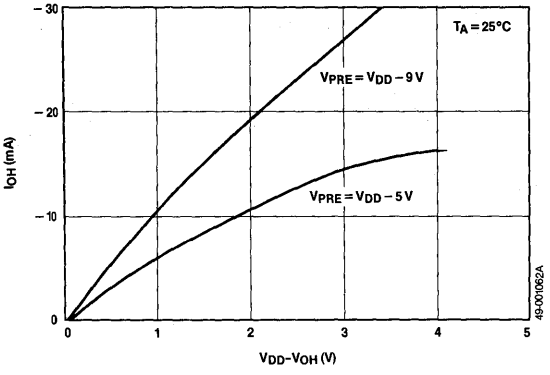


V_{OH} vs I_{OH} (Ports 2-5) (Typical)



Operating Characteristics (cont)

V_{OH} vs I_{OH} (Ports 8–11) (Typical)



Differences Among the μPD7527/28/CQ28

	μPD75CQ28	μPD7527	μPD7528
Program memory	4 Kbyte EPROM (2732) connectable on top	On-chip 2 Kbyte ROM	On-chip 4 Kbyte ROM
Data memory (RAM)	160×4	128×4	160×4
High-voltage output lines	All open-drain outputs	On-chip load capacitor or open drain output (bit by bit, mask optional)	
V_{LOAD} pin	No		
Zero-cross detection	Yes	Mask optional	
Package	42-pin ceramic piggyback DIP bottom pin compatible with μPD7527 / 28	42-pin plastic DIP 42-pin plastic shrink DIP	
Power supply	5 V	2.7 V to 6.0 V	

NEC

NEC Electronics Inc.

μPD7533
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH A/D CONVERTER

PRELIMINARY INFORMATION

Description

The μPD7533 is a 4-bit, single-chip CMOS microcomputer with a 4-channel, 8-bit A/D converter, 8-bit timer/event counter, and an 8-bit serial interface. The μPD7533 has 30 I/O lines, 8 of which can be used to directly drive LEDs. The μPD7533 executes 67 instructions of the μPD7500 series "A" instruction set.

The A/D converter has various temperature monitoring applications that can be used with household electrical appliances, such as air conditioners and electric ovens. Other applications include health monitoring equipment and cameras.

The μPD75CG33 consists of a 28-pin socket "piggy-backed" on the lower 42-pin ceramic DIP. This socket is configured to hold either a 2732A or 2764 EPROM. For engineering purposes, programs can be tried and debugged before ROM code submission.

Features

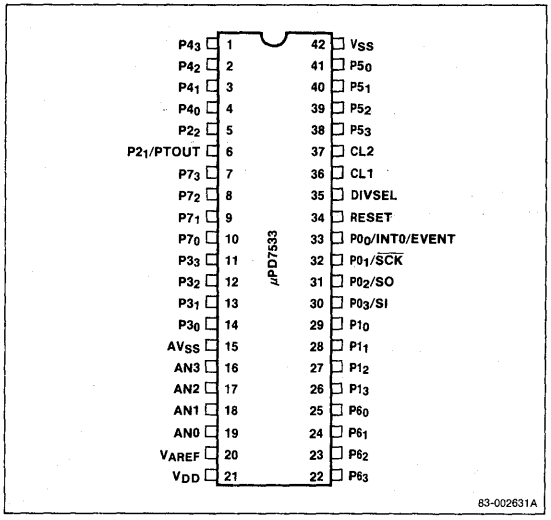
- ☐ 4-bit single chip microcomputer
- ☐ 67 instructions (subset of μPD7500 series set A)
- ☐ Instruction cycle
  - — 5 μs at 5 V, 400-kHz clock at ceramic oscillation, DIVSEL = high
  - — 10 μs at 5 V, 400-kHz clock at ceramic oscillation, DIVSEL = low
- ☐ Program memory (ROM): 4096 words x 8 bits
  - — External in the μPD75CG33
- ☐ Data memory (RAM): 160 words x 4 bits
- ☐ 8 high current output lines for LED direct drive
- ☐ Input/output ports
  - — Two 4-bit input ports
  - — One 2-bit output port
  - — One 4-bit output port
  - — Three 4-bit input/output ports (two of which can function in 8-bit units)
  - — One 4-bit input/output port usable at bit level
- ☐ Interrupts: two internal and one external
- ☐ 8-bit serial interface
- ☐ Standby operation
  - — STOP mode
  - — HALT mode
- ☐ On-chip system clock oscillator
  - — Ceramic resonator
  - — Full or 1/2 oscillation frequency
- ☐ CMOS technology
- ☐ Low power consumption
- ☐ Single power supply

Ordering Information

Part Number	Package Type	Maximum Frequency of Operation
μPD7533C	42-pin plastic DIP	500 kHz
μPD7533CU	42-pin plastic shrink DIP	500 kHz
μPD7533G-22	44-pin plastic miniflat	500 kHz
μPD75CG33E	42-pin ceramic piggyback DIP	500 kHz

Pin Configurations

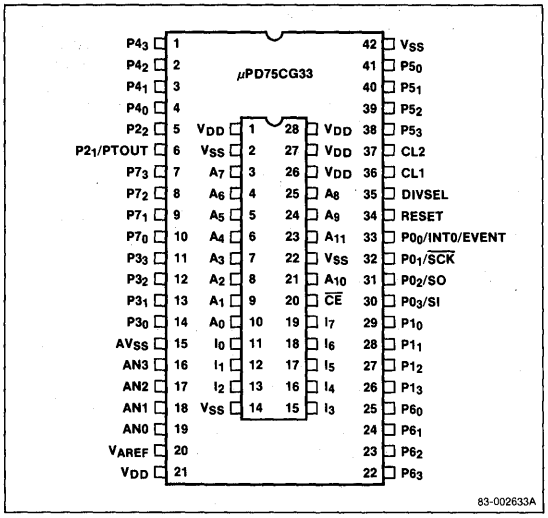
42-Pin Plastic DIP or Plastic Shrink DIP



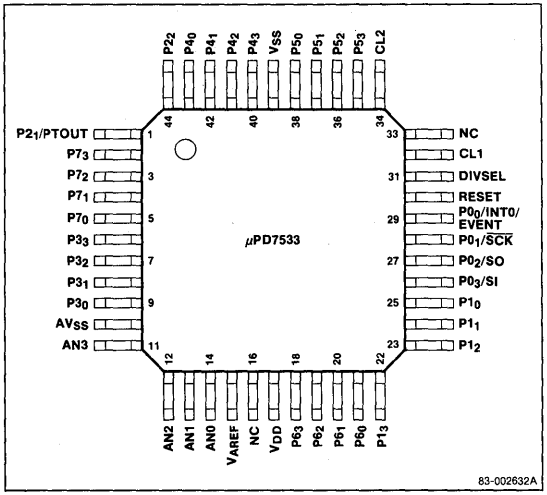
3

Pin Configurations (cont)

42-Pin Ceramic Piggyback DIP



44-Pin Plastic Miniflat



Pin Identification

42-Pin DIP, Shrink DIP, and Piggyback DIP

No.	Symbol	Function
1-4	$P4_3$-$P4_0$	I/O port 4
5, 6	$P2_2$, $P2_1$/PTOUT	Port 2 output
7-10	$P7_3$-$P7_0$	I/O port 7
11-14	$P3_3$-$P3_0$	Port 3 output
15	A_{VSS}	A/D converter ground
16-19	AN3-AN0	Analog input
20	V_{AREF}	A/D reference voltage input
21	V_{DD}	Positive power supply
22-25	$P6_3$-$P6_0$	I/O port 6
26-29	$P1_3$-$P1_0$	Port 1 input
30	$P0_3$/SI	Port 0 input/Serial input
31	$P0_2$/SO	Port 0 input/Serial output
32	$P0_1$/$\overline{SCK}$	Port 0 input/(I/O) Serial clock
33	$P0_0$/INT0/EVENT	Port 0 input/Interrupt 0/Event input
34	RESET	RESET input
35	DIVSEL	System clock selection input
36, 37	CL1, CL2	External clock input/System clock terminal
38-41	$P5_3$-$P5_0$	I/O port 5
42	V_{SS}	Ground

Pin Identification (cont)

44-Pin Miniflat

No.	Symbol	Function
1, 44	$P2_1$/PTOUT, $P2_2$	Port 2 output
2-5	$P7_3$-$P7_0$	I/O port 7
6-9	$P3_3$-$P3_0$	Port 3 output
10	A_{VSS}	A/D converter ground
11-14	AN3-AN0	Analog input
15	V_{AREF}	A/D reference voltage input
17	V_{DD}	Positive power supply
18-21	$P6_3$-$P6_0$	I/O port 6
21-25	$P1_3$-$P1_0$	Port 1 input
26	$P0_3$/SI	Port 0 input/Serial input
27	$P0_2$/SO	Port 0 input/Serial output
28	$P0_1$/$\overline{SCK}$	Port 0 input/(I/O) Serial clock
29	$P0_0$/INT0/EVENT	Port 0 input/Interrupt 0/Event input
30	RESET	RESET input
31	DIVSEL	System clock selection input
32, 34	CL1, CL2	External clock input/System clock
35-38	$P5_3$-$P5_0$	I/O port 5
39	V_{SS}	Ground
40-43	$P4_3$-$P4_0$	I/O port 4

28-Pin EPROM Socket on 42-pin Piggyback DIP

No.	Symbol	Function
1, 26-28	V_{DD}	Positive power supply
2, 14, 22	V_{SS}	Ground
20	$\overline{CE}$	Chip enable output
3-10, 21, 23-25	A_0-A_{11}	Address bus
11-13, 15-19	I_0-I_7	Data bus

Pin Functions

$P0_0$-$P0_3$ [Port 0]

$P0_0$-$P0_3$ function as port 0. $P0_0$ also functions as a count pulse input pin for the timer/event counter (EVENT) or as interrupt 0 (INT0). $P0_1$ also functions as a serial clock input/output pin ($\overline{SCK}$) for the serial interface. $P0_2$ functions as a serial data output pin (SO) and pins $P0_3$ as a serial data input pin (SI). The $P0_1$/$\overline{SCK}$ and $P0_2$/SO pins are three-state input/output.

The shift mode register (SM_0-SM_3) determines the operation mode of the port 0 input/output pins; however, the data on $P0_0$-$P0_3$ can be loaded into the accumulator at any time by executing a port input instruction (IP/IPL). This is possible even when $P0_1$-$P0_3$ are functioning as the serial interface.

After a RESET, $P0_0$-$P0_3$ become input ports (high impedance).

$P1_0$-$P1_3$ [Port 1]

$P1_0$-$P1_3$ function as port 1. Execution of an IP or IPL instruction reads data present on $P1_0$-$P1_3$ into the accumulator. Tie any unused lines of $P1_0$-$P1_3$ to V_{DD} or V_{SS}.

$P2_1$-$P2_2$ [Port 2]

$P2_1$-$P2_2$ function as port 2 with an output latch. When an output instruction (OP/OPL) to port 2 is executed, the middle 2 bits (A_1 and A_2) of the accumulator are latched by the output latch and, at the same time, output to $P2_1$-$P2_2$.

After being written once, the output latch contents remain until they are rewritten by an output instruction or a reset. The status of the corresponding output signal also remains. After a reset, the output latch contents become undefined, all output signals are disabled, and the output drivers are turned off.

$P2_1$ is also used as an output pin (PTOUT) for the timer-out F/F signal (PTOUT). Bit 3 (CM_3) of the clock mode register controls the PTOUT output. When CM_3 is 1, TOUT is ORed with the $P2_1$ output latch contents and sent to the output driver. Therefore, to output the $P2_1$ output latch contents, reset CM_3 to 0 to inhibit the TOUT signal.

Note that soon after the RESET signal is asserted, CM_3 is reset and TOUT is inhibited. However, since the output latch contents are undefined after a reset, to output the TOUT signal, first write 0 in the $P2_1$ output latch and then set CM_3 to 1 to output TOUT.

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$P3_0$-$P3_3$ [Port 3]

$P3_0$-$P3_3$ function as port 3 with an output latch. When an output instruction to port 3 is executed, the accumulator contents are latched and output.

Once data is written in the output latch, the data is held until the next output instruction to port 3 is executed or RESET is asserted. After a reset, the output latch contents become undefined and the output driver is turned off.

$P4_0$-$P4_3$ [Port 4]
$P5_0$-$P5_3$ [Port 5]

$P4_0$-$P4_3$ function as port 4 and $P5_0$-$P5_3$ function as port 5. When an input instruction is executed, the data on these pins is read into the accumulator. When an output instruction is executed, the accumulator contents are latched and output. After the data is written into the latch, it is held until the next output instruction to ports 4 or 5 is executed, or RESET is asserted.

Ports 4 and 5 can work as a pair enabling data (input with the IP54 instruction and output with the OP54 instruction) in 8-bit units. The high four bits of data are from the accumulator and the low four bits are from memory (addressed by HL).

Ports 4 and 5 automatically set in the input mode (high impedance output) after a reset or when the input instructions to these ports are executed. After a reset, the output latch contents become undefined. Both ports 4 and 5 can drive LEDs directly.

Note that after the port changes from output mode to input mode, the data on the line is unstable when the input instruction that changes the mode is first executed. It is strongly recommended that you re-execute the input instruction considering the input/output mode switching time. This will insure reading stable data.

The bit manipulation instruction affects the specified bit only. So when the output latch contents are undefined, (immediately after a reset), initialize the output latch contents with an output instruction before the bit manipulation instruction is executed.

$P6_0$-$P6_3$ [Port 6]

$P6_0$-$P6_3$ function as the 4-bit input latched, three-state output port. The individual lines can be programmed as either inputs or outputs.

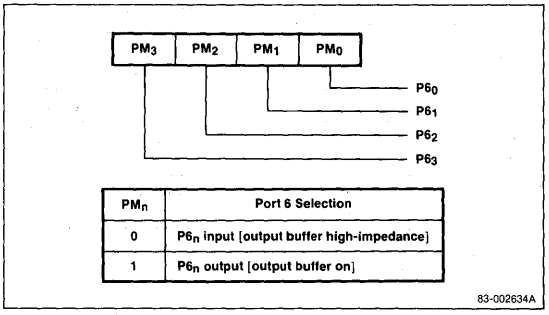
In input mode, data present at this port is read into the accumulator by the execution of an IP or IPL instruction. Accumulator data written to this port by the execution of an OP, OPL, ANP, or ORP instruction is statically latched, and remains unchanged until rewritten. This data, however, is not output since the output buffer is disabled and placed in the high impedance state.

In output mode, accumulator data written to the specified port line by the execution of the OP, OPL, ANP, or ORP instruction is statically latched and output to the $P6_n$ pin. Data present at $P6_n$ is read into the accumulator by the execution of the IP or IPL instruction, making it possible to read the contents of the $P6_n$ output latch.

All lines of port 6 are initialized to the high impedance state at Reset. Leave any unused lines open (if outputs) or tied to V_{DD} or V_{SS} (if inputs).

The port 6 mode select register (MSR) controls the function of the individual port 6 lines. The execution of the OP or OPL instruction loads the port 6 MSR with the accumulator contents. The 4-bit immediate data operand or the contents of the L register must be set to 0EH. Figure 1 shows the format of the port 6 MSR.

Figure 1. Port 6 MSR Format



PM_n	Port 6 Selection
0	$P6_n$ input [output buffer high-impedance]
1	$P6_n$ output [output buffer on]

83-002634A

$P7_0$-$P7_3$ [Port 7]

Port 7 is a 4-bit input or latched three-state output port. The execution of an IP or IPL instruction execution reads data present at this port into the accumulator. Accumulator data written to this port by the execution of an OP, OPL, ANP, or ORP instruction is statically latched and remains unchanged until rewritten.

Upon reset, all lines are initialized to the high-impedance state. Leave any unused lines open (if outputs) or tied to V_{DD} or V_{SS} (if inputs).

AN0-AN3 [A/D Input Terminal]

AN0-AN3 are the 4-channel A/D converter input terminals. The A/D converter uses a successive approximation method.

V_{AREF} [A/D Converter Positive Reference]

The voltage on V_{AREF} determines the full scale analog voltage.

A_{VSS} [A/D Converter Ground]

A_{VSS} is the ground for the A/D circuit.

CL1, CL2 [Clock]

CL1 and CL2 connect external oscillator elements to the system clock. Connect a ceramic resonator to these pins. If an external clock is used, place a buffer between the clock source and the CL1 and CL2 pins.

When connecting the oscillation parts to the CL1 and CL2 pins, use the shortest wiring possible. Ground the capacitor as close to the V_{SS} pin as possible.

DIVSEL [System Clock Divider Selection Input]

DIVSEL selects whether the system clock runs at ceramic oscillation frequency, or at one-half the ceramic oscillation frequency. If a logic 0 (V_{SS}) is connected to DIVSEL, the system clock is one-fourth the ceramic oscillation. If DIVSEL is high, then the system clock will be one-half of the ceramic oscillation.

RESET [Reset]

A high on RESET activates this input.

V_{DD} [Power Supply]

V_{DD} is the positive power supply pin.

V_{SS} [Ground]

V_{SS} is the ground pin.

Pin Functions, μPD75CG33 EPROM

A_0-A_{11} [EPROM Address]

A_0-A_{11} output the contents of the EPROM program address counter. A reset leaves A_0-A_{11} undefined.

I_0-I_7 [Data Bus]

I_0-I_7 input the contents of the EPROM data bus.

$\overline{CE}$ [Chip Enable]

$\overline{CE}$ outputs the EPROM chip enable signal. (Active low.)

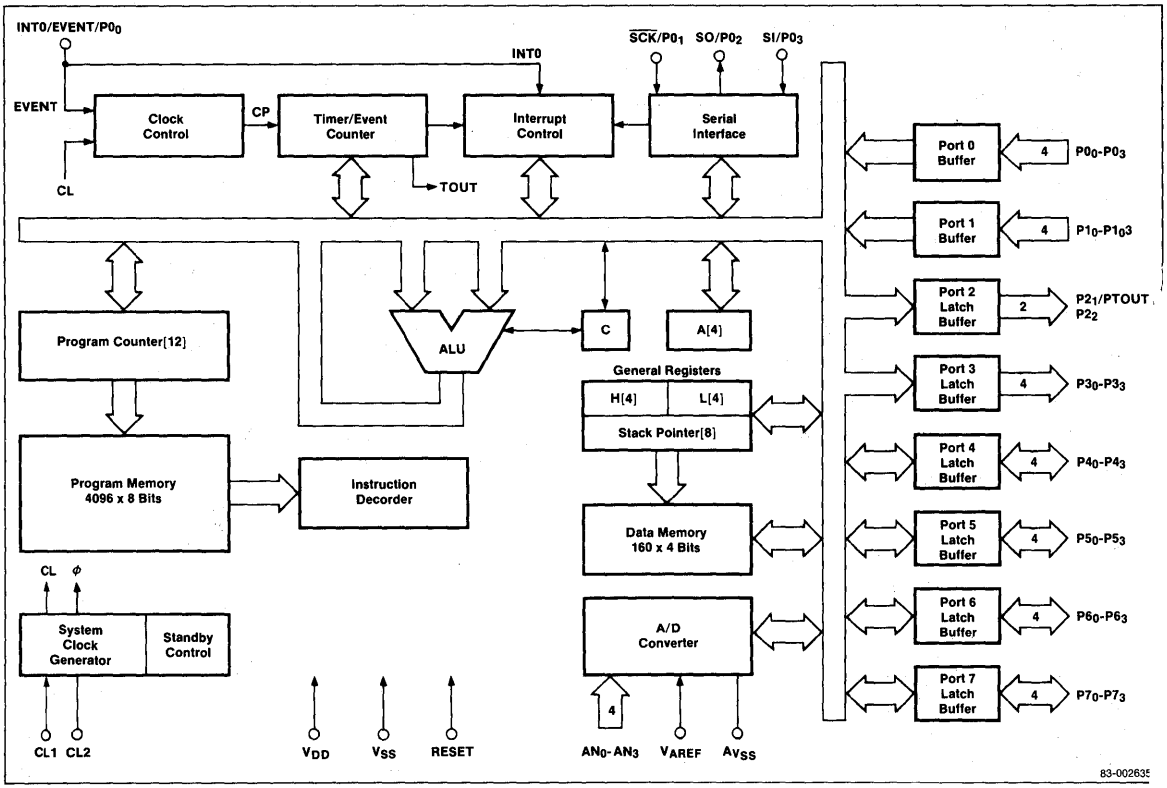
V_{DD} [Power Supply], V_{SS} [Ground]

V_{DD} is the positive power supply pin with the same voltage as the lower portion pin 21. V_{SS} is the ground pin with the same voltage as the lower portion pin 42. The following voltages are supplied to the 2764 or 2732A pins from V_{DD} or V_{SS}.

Pin Number			
2764	2732A	Symbol	Voltage
1	20	V_{PP}	V_{DD} pin 21 = +5 V
28	24	V_{CC}	V_{DD} pin 21 = +5 V
22	20	$\overline{OE}$	V_{SS} pin 42 = 0 V
2	—	A_{12}	V_{DD} pin 21 = +5 V
14	12	V_{SS}	V_{SS} pin 42 = 0 V

3

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{DD} + 0.3 V
Output voltage, V_O	−0.3 V to V_{DD} + 0.3 V
High level output current, I_{OH}	−10 mA (1 pin)
	−20 mA (all output ports)
Low level output current, I_{OL}	10 mA (1 pin)
	45 mA ports 2,3,4,7 (total pins)
	45 mA ports 0,5,6
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +150°C
A/D V_{SS}, A_{VSS}	−0.3 to +0.3 V
A/D reference, V_{AREF}	−0.3 V to V_{DD}

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input capacitance	C_{IN}		15	pF	f = 1 MHz Unmeasured pins are 0 V
Output capacitance	C_{OUT}		15	pF	
I/O capacitance	C_{IO}		15	pF	

DC Characteristics

$T_A = -10$ to $+70°C$, $V_{DD} = 3.0$ to 6.0 V, DIVSEL = 1

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
High level input voltage (other than CL1, CL2)	V_{IH1}	0.7 V_{DD}	V_{DD}	V	Conditions specified by oscillation characteristics
High level input voltage (CL1, CL2)	V_{IH2}	$V_{DD} - 0.5$	V_{DD}	V	
Low level input voltage (other than CL1, CL2)	V_{IL1}	0	0.3 V_{DD}	V	
Low level input voltage (CL1, CL2)	V_{IL2}	0	0.5	V	
High level output voltage	V_{OH}	$V_{DD} - 1.0$		V	$V_{DD} = 4.5–6.0$ V, $I_{OH} = -1$ mA
		$V_{DD} - 0.5$		V	$I_{OH} = -100$ μA
Low level output voltage	V_{OL}	0.5 (typ)	2.0	V	$V_{DD} = 4.5–6.0$ V, $I_{OL} = 10$ mA
			0.4	V	$I_{OL} = 1.6$ mA
			0.5	V	$I_{OL} = 400$ μA
High level input leakage current (other than CL1, CL2)	I_{LIH1}		3	μA	$V_{IN} = V_{DD}$
High level input leakage current (CL1, CL2)	I_{LIH2}		20	μA	$V_{IN} = V_{DD}$
Low level input leakage current (other than CL1, CL2)	I_{LIL1}		–3	μA	$V_{IN} = 0$ V
Low level input leakage current (CL1, CL2)	I_{LIL2}		–20	μA	
High level output leakage current	I_{LOH}		3	μA	$V_{OUT} = V_{DD}$
Low level output leakage current	I_{LOL}		–3	μA	$V_{OUT} = 0$ V
Supply current	I_{DD1}	1.0 (typ)	3.0	mA	Operating mode: $V_{DD} = 4.5–6.0$ V; $f_{CC} = 400$ Hz
	I_{DD2}	450 (typ)	1200	μA	HALT mode: $V_{DD} = 4.5–6.0$ V; $f_{CC} = 400$ HZ
	I_{DD3}	0.1 (typ)	10	μA	STOP mode

AC Characteristics

$T_A = -10$ to $+70°C$, $V_{DD} = 3.0$ to 6.0 V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Cycle time	t_{CY}	4.0	200	μs	$V_{DD} = 4.5–6.0$ V
		9.5	200	μs	
EVENT input frequency	f_E	0	500	kHz	$V_{DD} = 4.5–6.0$ V
		0	210	kHz	
EVENT input high duration	t_{EH}	0.8		μs	$V_{DD} = 4.5–6.0$V
EVENT input low duration	t_{EL}	2.3		μs	
$\overline{SCK}$ cycle time	t_{KCY}	3.0		μs	Input $V_{DD} = 4.5–6.0$ V
		4.0		μs	Output
		8.0		μs	Input
		9.5		μs	Output
$\overline{SCK}$ high, low level duration	t_{KH}, t_{KL}	1.3		μs	Input $V_{DD} = 4.5–6.0$ V
		1.8		μs	Output
		4.0		μs	Input
		4.7		μs	Output
SI setup time ($\overline{SCK}$ high)	t_{SIK}	300		ns	
SI hold time ($\overline{SCK}$ high)	t_{KSI}	450		ns	
$\overline{SCK}$ low to SO output delay time	t_{KSO}		850	ns	$V_{DD} = 4.5–6.0$ V
			1200		
INT0 high, low level duration	t_{I0H}, t_{I0L}	10		μs	
RESET high, low level duration	t_{RSH}, t_{RSL}	10		μs	

3

Data Memory, STOP Mode Data Retention Characteristics

T_A = −10 to +70°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		6.0	V	
Data retention supply current	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V
RESET setup time	t_{SRS}	0			μs	
Oscillation stabilizing time	t_{OS}	20			ms	Ceramic resonator: when V_{DD} greater than 4.5 V
		25			ms	Crystal: when V_{DD} greater than 4.5 V

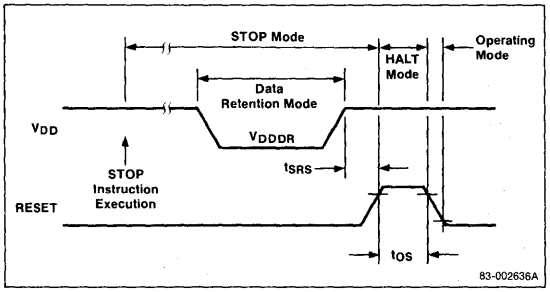
A/D Converter Characteristics

T_A = −10 to +70°C, V_{DD} = +5.0 V ±5%, $V_{SS} = A_{VSS}$ = 0 V, $V_{AREF} = V_{DD}$ − 0.5 V to V_{DD}

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Resolution		8			Bits	
Absolute accuracy				0.6 ±1/2	LSB	
Conversion time	t_{CONV}		9		t_{CYC}*	
Sampling time	t_{SAMP}		1		t_{CYC}*	
Analog input voltage	V_{IAM}	0		V_{AREF}	V	
Analog input impedance	R_{AN}		1000		MΩ	
V_{AREF} current	I_{AREF}	0.4	1	2	mA	

* $t_{CYC} = \frac{2}{f_{CC}}$ (DIVSEL = 1)

Data Retention Timing



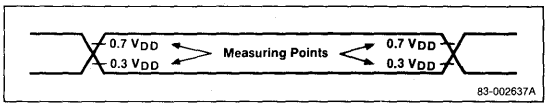
Oscillator Characteristics

T_A = −10 to +70°C, V_{DD} = 3.0 to 6.0 V, DIVSEL = 1

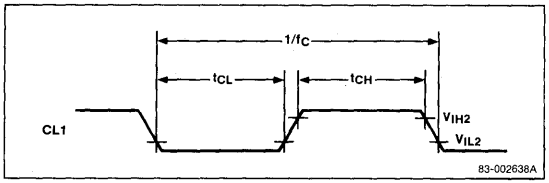
Oscillation	Configuration	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
Ceramic	See figure 3	Oscillation frequency (f_{CC})	390	400	410	kHz	V_{DD} = 4.5 to 6.0 V
		Stabilization time	20			ms	V_{DD} greater than 4.5 V
External clock	See figure 3	CL1 input frequency	10		410	kHz	V_{DD} = 4.5 to 6.0 V
			10		210	kHz	
		CL1 input high, low level duration (t_{CH},t_{CL})	1.0		50	μs	V_{DD} = 4.5 to 6.0 V
			2.0		50	μs	

Timing Waveforms

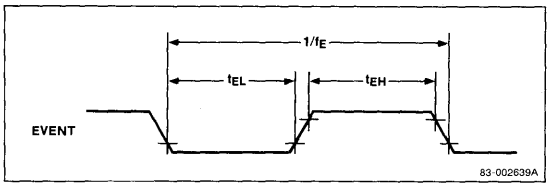
AC Timing Measuring Points (Except CL1)



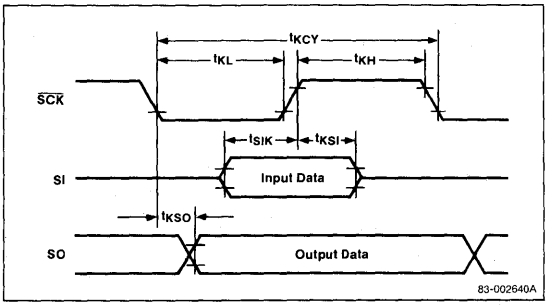
Clock Timing



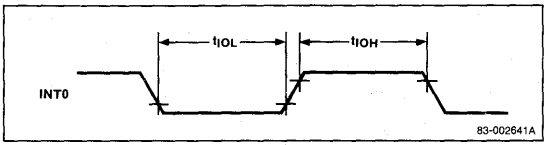
EVENT Timing



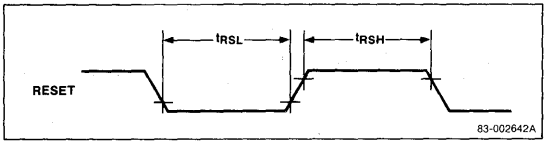
Serial Transfer Timing



Interrupt Input Timing



RESET Input Timing



3

Functional Description

System Clock Generator

The ceramic oscillator circuit generates the system clock for the μPD7533. Figure 2 shows that the oscillator circuit for the μPD7533 includes a ceramic oscillator, two divide-by-two circuits, the DIVSEL input, and control circuitry for the standby modes, HALT and STOP.

Figure 3 shows that the ceramic oscillator requires that a ceramic resonator be connected to the CL1 and CL2 pins. An external clock can also be input at CL1. In this case, the oscillator operates as an inverted buffer.

Figure 2 shows that the output frequency from the ceramic oscillator connects either directly to the clock selector or via a divide-by-two circuit. The selector is controlled by the DIVSEL line. If DIVSEL is low, the divide-by-two frequency is selected. This option is used during a low power operating mode. If DIVSEL is high, then the direct frequency is chosen. The output of the selector is used as system clock (CL), and is also divided by two to supply the CPU clock (ϕ).

Table 1 shows how DIVSEL selects the system and CPU clocks, and machine cycle timing.

Table 1. Clock Selection

DIVSEL	System Clock (CL)	CPU Clock (ϕ)	Machine Cycle
Low	200 kHz	100 kHz	10 μs
High	400 kHz	200 kHz	5 μs

Standby Control

The HALT F/F and the STOP F/F comprise the control circuitry for standby mode (figure 2). The STOP F/F is set by the STOP instruction. When the STOP F/F is set, the ceramic oscillator stops. The rising edge of the RESET input resets the STOP F/F.

The HALT instruction sets the HALT F/F and inhibits the input of the half-frequency divider which generates the CPU clock. As a result, only the CPU clock is stopped in HALT mode. The RELEASE signal resets the HALT F/F. RELEASE becomes active when any interrupt request flag is set, or at the falling edge of the RESET input.

While RESET is active, the HALT F/F is set, and the chip goes into the HALT mode. At a power-on Reset, the ceramic oscillation is driven when the RESET input signal becomes high.

Figure 3. Clock Driver Configuration

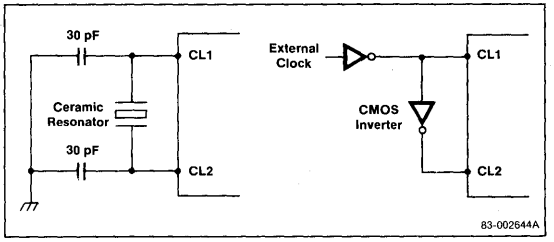
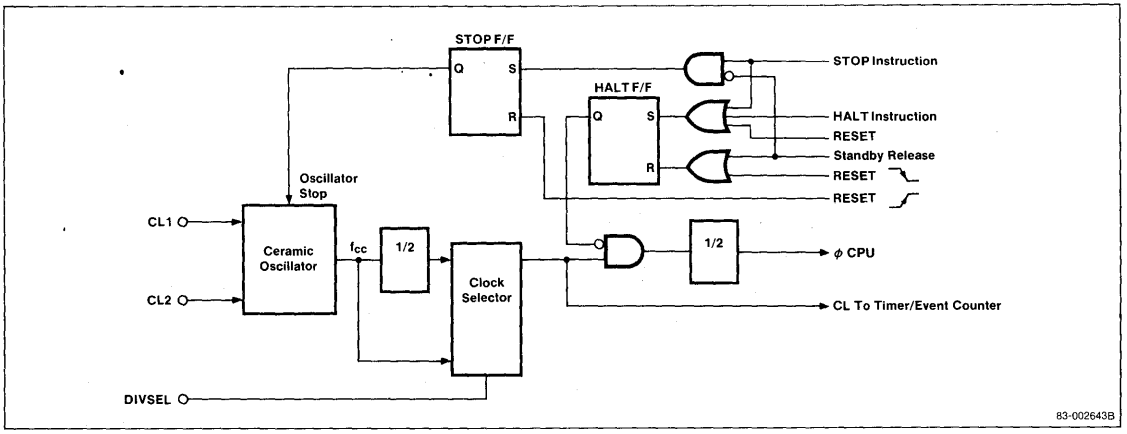


Figure 2. System Clock Generator



It takes a short period of time for the oscillator output to become stable. To prevent errors due to an unstable clock, the HALT F/F is set to inhibit the CPU clock while the RESET input is high. Therefore, the high-level pulse width for the RESET input should be wide enough to cover the required time for the ceramic resonator oscillation to stabilize.

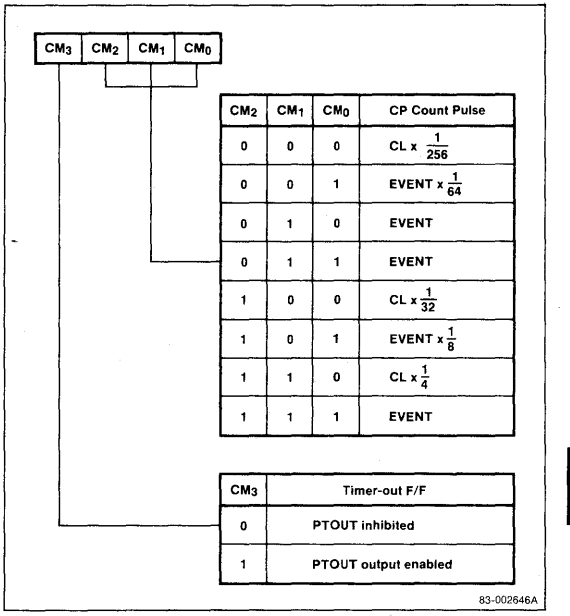
Clock Control

Figure 4 shows that the clock controller contains a 4-bit clock mode register (CM0-CM3), prescalers 1-3, and multiplexers. The clock controller selects the clock sources and prescalers, and supplies the count pulses (CP) to the timer/event counter. The clock sources are the system clock generator output (CL) or the EVENT pulse.

The OP 12 or OPL (L = 12) instruction sets codes in the clock mode register. CM3 designates the output of the timer-out signals. If CM3 = 1, the output of the timer-out F/F (TOUT) is available at the PTOUT (P21) pin.

Figure 5 shows the format of the clock mode register.

Figure 5. Format of Clock Mode Register

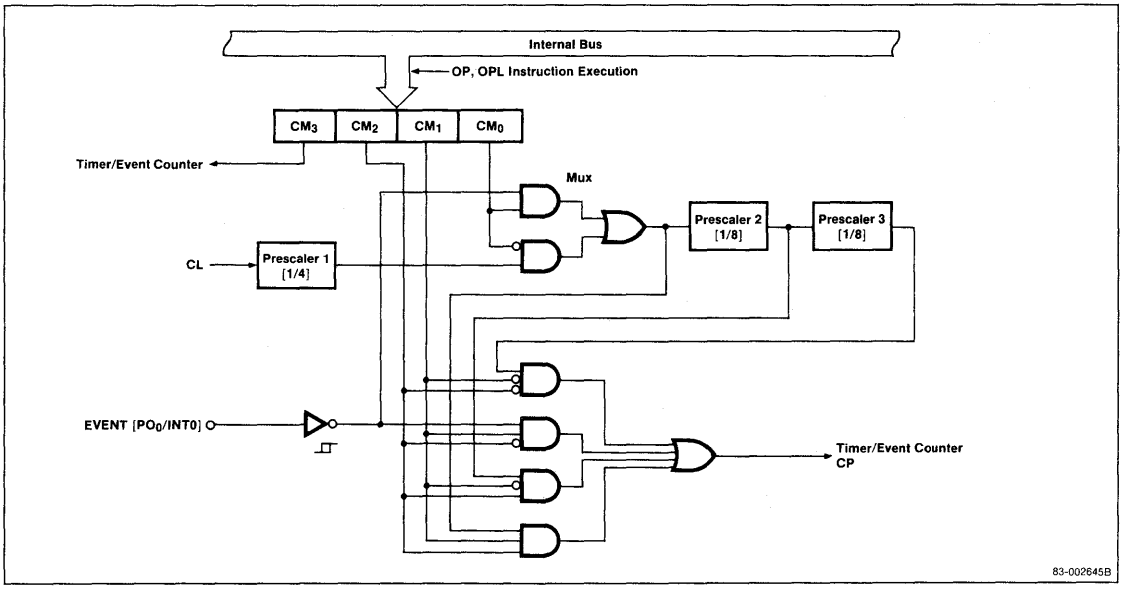


CM_2	CM_1	CM_0	CP Count Pulse
0	0	0	CL x $\frac{1}{256}$
0	0	1	EVENT x $\frac{1}{64}$
0	1	0	EVENT
0	1	1	EVENT
1	0	0	CL x $\frac{1}{32}$
1	0	1	EVENT x $\frac{1}{8}$
1	1	0	CL x $\frac{1}{4}$
1	1	1	EVENT

CM_3	Timer-out F/F
0	PTOUT inhibited
1	PTOUT output enabled

83-002646A

Figure 4. Clock Controller Block Diagram



Timer/Event Counter

Figure 6 shows the timer/event counter has an 8-bit count register, 8-bit modulo register, an 8-bit comparator, and a timer-out flip flop.

Timer Operation

After the TAMMOD instruction sets a count value in the modulo register and the TIMER instruction clears the contents of the count register, the timer starts counting count pulses (CP). If an external clock is used, the count pulses are synchronized with the rising edge of CL1 or the $P0_0$ input.

When the value of the modulo register equals the value of the count register, the comparator generates a coincidence signal (INTT) to set an interrupt request flag. Then it clears the count register to repeat the counting. In this manner, the timer functions as an interval timer whose interval is set by the modulo register.

Regardless of any instructions, the count pulses are always input into the count register, updating the count value. If the contents of the count register are equal to those of the modulo register, the INTT request flag is then set. For this reason, inhibit INTT interrupts when not using the timer.

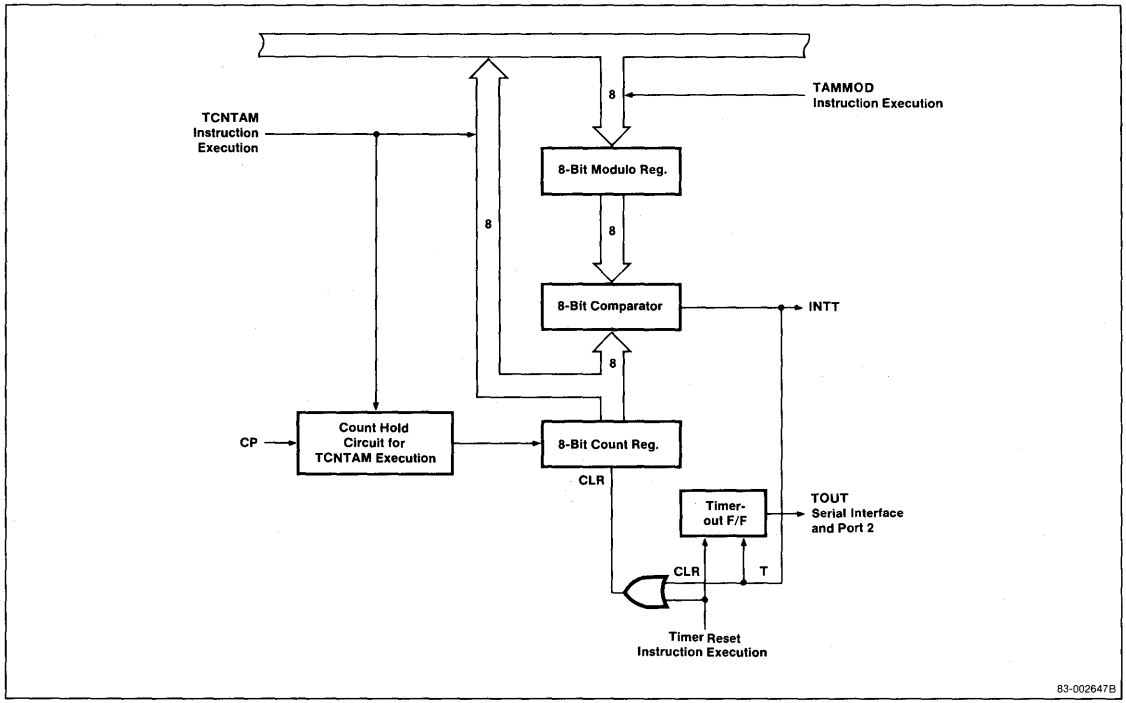
Event Counter Operation

To use the timer/event counter as an event counter, input the external event pulse into the $P0_0$ pin, and select $P0_0'$ as the count pulse (CP) for the clock controller. The count register counts the external event pulses input at the $P0_0$ pin, either as they are, or frequency divided.

As a result, the timer/event counter operates as an event counter that generates interrupts after observing the number of counts (events) specified by the modulo register. The TCNTAM instruction can read the current count at any time.

Set the modulo register with the number of count pulses minus one. If set to 0, no counting will occur because the counter register is held at 0 (both the detection of coincidence and zero-clearing are simultaneously made).

Figure 6. Block Diagram of Timer/Event Counter



Serial Interface

As figure 7 shows, the serial interface includes an 8-bit shift register, a 4-bit shift mode register, and a 3-bit counter.

The serial clock controls serial data I/O. At the falling edge of the serial clock ($\overline{SCK}$), the SO line outputs the most significant bit (7) of the shift register. The contents of the shift register are shifted by one bit at the rising edge of the next serial clock (n ←0 n+1). At the same time, the data on the SI line is loaded into the least significant bit (0) of the shift register.

The 3-bit counter (octal counter) counts up the serial clocks and generates an internal interrupt signal INTS at every count of 8 clocks (at the end of a 1-byte serial data transfer). It then sets the interrupt request flag (INTO/S RQF). The TAMSIO instruction sets data in the shift register during the transmission of serial data, then starts transmission. At the end of the transmission of each byte (8 bits) an internal interrupt (INTS) is generated.

The SIO instruction also starts the reception of serial data. The received data is taken from the shift register by executing the TSIOAM instruction after an interrupt (INTS) is generated by the reception of one byte of data.

The end of a 1-byte transfer can be confirmed by testing the INTS RQF with the SKI instruction instead of interrupt processing.

The following three types of serial clock sources are available: system clock ϕ, external clock ($\overline{SCK}$ input), and timer-out F/F output signal (TOUT). Bits SM_2-SM_0 of the shift mode register select the clock source.

If the system clock ϕ is chosen, execute the SIO instruction to supply the clock to the serial interface, controlling the input/output of serial data while ϕ is output from the $\overline{SCK}$ pin.

After eight ϕ pulses, the clock is automatically discontinued by holding the $\overline{SCK}$ output at a high level. Therefore, the input/output of serial data automatically stops after each byte has been transferred. Consequently, the software does not need to control the serial clock and the transfer rate is determined by the system clock frequency.

In this mode, after six machine cycles from the execution of the SIO, the TSIOAM instruction can read out the received data from the shift register or can write in the next transmit data.

Figure 8 shows the shift mode register format.

3

Figure 7. Serial Interface Block Diagram

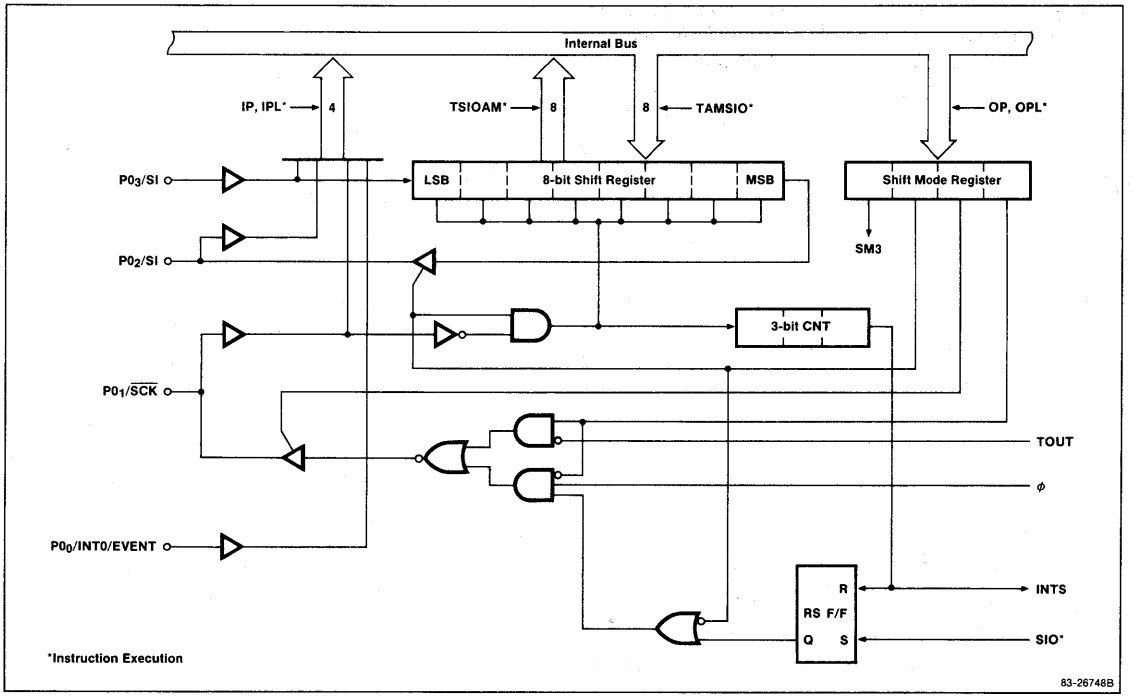


Figure 8. Format of Shift Mode Register

SM_2	SM_1	SM_0	PO_3/SI	PO_2/SO	$PO_1/\overline{SCK}$	Serial Operation
0	0	0	Port input	Port input	Port input	Stops
0	1	0			Outputs ϕ continuously	
0	1	1			Outputs TOUT continuously	
1	0	0	SI input	SO output	$\overline{SCK}$ input	Operates with external clock
1	1	0			$\overline{SCK}$ output (ϕ x 8)	Operates with ϕ
1	1	1			$\overline{SCK}$ output (TOUT)	Operates with TOUT

Bit SM_3 selects the interrupt source in the following manner:

SM_3	Interrupt Source
0	INTS
1	INT0

If the external clock ($\overline{SCK}$ input) is selected, the serial clocks are input from $\overline{SCK}$. When the eighth external serial clock is input, an internal interrupt (INTS) is generated, signalling the end of a 1-byte data transfer.

Since the serial clocks are not internally inhibited, the external clock must hold the signal high after eight clocks. The external serial clock determines the transfer rate. The serial interface can be operated from DC to the maximum rate in the electrical specifications.

If TOUT is selected, the half-frequency divided coincidence signal of the timer/event counter is the serial clock. This serial clock controls the input/output of the serial data and is output from the $\overline{SCK}$ pin.

The count pulse supplied to the timer/event counter and the value set in the modulo register determine the transfer rate. The end of a 1-byte data transfer is signalled by INTS. TOUT is not inhibited automatically, therefore the program should stop TOUT at intervals of 16.

To use the external clock or the TOUT signal, execute the SIO, TAMSIO or TSIOAM instructions while the serial clock ($\overline{SCK}$) is held high. Operation cannot be guaranteed if these intructions are executed over the rising or falling edge of $\overline{SCK}$, or at the low level.

In a system that does not require serial data transfer, the 8-bit shift register can be ued as a register with the serial operation stopped. The TSIOAM or TAMSIO instruction can read or write data.

Analog to Digital Converter

The μPD7533 integrates a 4-channel 8-bit A/D converter with separate positive reference and ground from the device power supply. Figure 9 shows that the A/D converter includes an A/D converter mode register, successive approximation (SA) register, and end of conversion (EOC) control circuitry.

A/D Converter Mode Register

The A/D converter mode register is a 4-bit internal port that controls the A/D circuitry. The lower two bits, ANI0 and ANI1, select which analog signal (AN0-AN3) is input to the A/D converter. The most significant bit, ADS, initiates the A/D conversion. If ADS is set to a logic 1, the analog signal selected by ANI1 and ANI0 is converted to 8-bit digital data. Upon completion of the data conversion, ADS is cleared to 0.

Figure 10 shows the format for the A/D conversion mode register.

Figure 10. A/D Conversion Mode Register Format

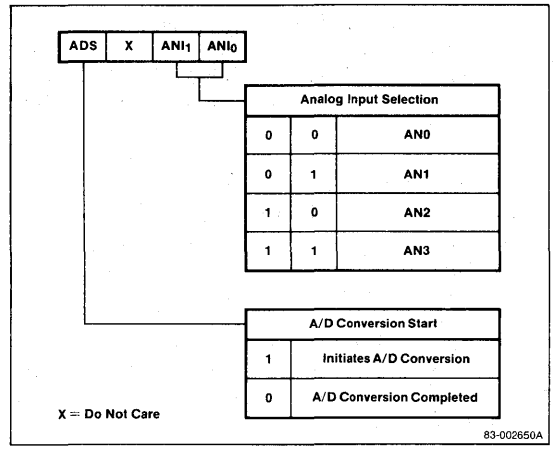
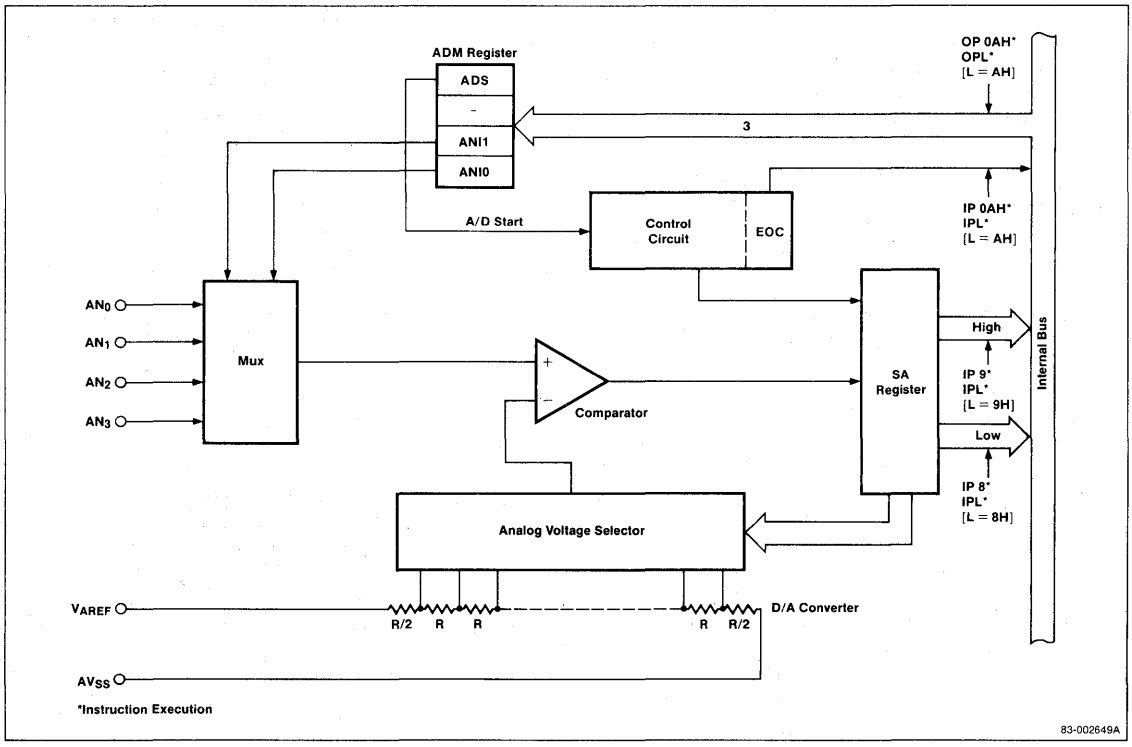


Figure 9. A/D Converter Block Diagram



Successive Approximation [SA]

The 8-bit data converted from the analog signal using the successive approximation method is stored in the SA register. When ADS is set to a logic 1, the contents of the SA register are undetermined. The SA register is set to 7FH after a reset.

End of Conversion [EOC] Flag

The EOC flag specifies the completion of an A/D conversion. When ADS is set to 1, the EOC flag is set to a logic 0 and an A/D conversion starts. When the 8-bit A/D conversion is complete, the EOC flag is set to a logic 1. The EOC flag resides in bit 2 of internal Port A. The IP 0AH or IPL instruction can read the contents of Port A when the L register is set to 0AH. The contents of Port A (other than bit 2) will be read as a logic 0. The EOC flag is set to 1 after a reset.

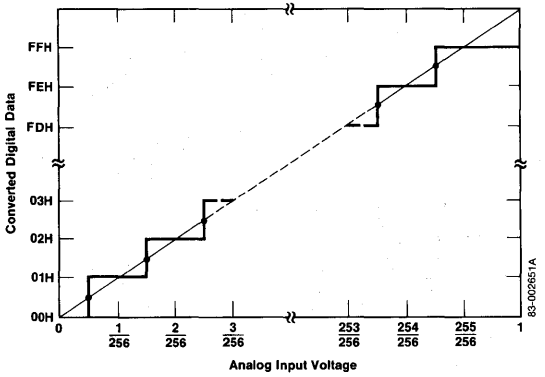
A/D Converter Operation

An OP 0AH or OPL instruction selects one of four analog signals and starts a conversion when the L register is set to 0AH. The lower two bits of the accumulator specify which analog signal will be converted. Bit 3 of the accumulator sets to 1 to initiate the A/D conversion. The A/D conversion requires 9 machine cycles for completion. When the conversion is complete, the EOC flag is set.

In order to assure an accurate data conversion, do not execute an output instruction when EOC is a logic 0.

Figure 11 shows how the analog input voltage corresponds to the converted digital data.

Figure 11. A/D Conversion Graph



Reading Converted Data

Internal port 9 specifies the upper four bits of the SA register. Therefore, execute an IP 9 or IPL (L = 9) instruction to read the data in the accumulator.

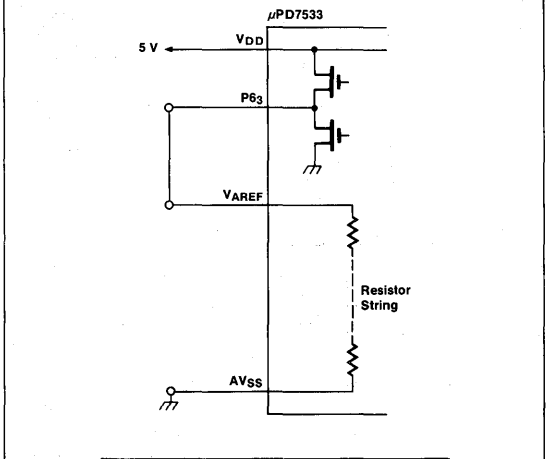
Internal port 8 specifies the lower four bits of the SA register. Therefore, execute an IP 8 or IPL (L = 8) instruction to read the data in the accumulator. Do not read the SA register until EOC is set to 1.

Figure 12 shows the configuration for the A/D converter reference voltage during standby mode.

Interrupt Function

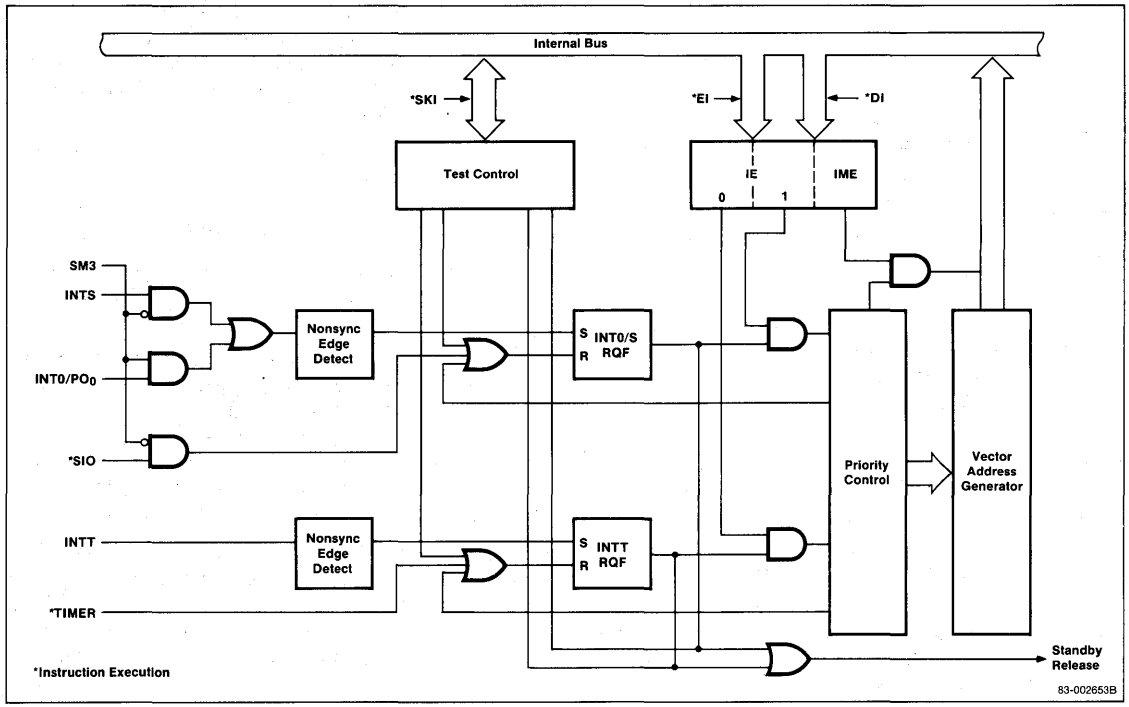
The μPD7533 provides one external interrupt and two types of internal interrupts. The $P0_0$ pin is used as the input pin for external interrupt INT0. INT0 shares priority and vectored addresses with internal interrupt INTS. Figure 13 shows the interrupt controller block diagram.

Figure 12. Configuration of V_{AREF} for Standby Mode Operation



$P6_3$ Output	V_{AREF}
High Level	V_{AREF} approximately = V_{DD}
Low Level or High Impedance	V_{AREF} approximately = 0 V

Figure 13. Interrupt Controller Block Diagram



Standby Function

The μPD7533 has two types of standby modes (STOP and HALT) to minimize power consumption during a program standby state. STOP mode is set by the STOP instruction and HALT mode by the HALT instruction.

When standby mode is set, program execution is stopped, and the contents of all internal registers and data memory are held. However, it is possible to operate the shift register and the timer/event counter. An interrupt or reset releases standby mode. Since an interrupt releases standby mode, neither STOP nor HALT modes can be set if an interrupt request flag is set. Therefore, when setting standby mode when there is a possibility of a request flag being set, first reset the interrupt request flag by processing the interrupt in advance or by executing the SKI instruction.

The major difference in the two modes is that crystal oscillation (CL) stops in STOP mode but does not stop in HALT mode.

In STOP mode, it is possible to go into data retention mode by lowering the power supply voltage. During data retention mode, all operation stops and only the data RAM stays intact.

Table 2 shows the differences between STOP and HALT modes.

Table 2. Differences Between STOP and HALT Modes

	Mode	
Operation	**STOP Mode**	**HALT Mode**
Ceramic Oscillation	X (1)	0 (2)
1/2 Ceramic Oscillation	X	X
CPU	X	X
Serial I/O	(3)	
Timer/Event Counter	X	0
A/D Converter	X	0
Release of Standby Mode	RESET	INT0/S RQF NTT RQF RESET Input

Note:

(1) Not possible
(2) Possible
(3) Possible depending on clock source selected

STOP Mode

In STOP mode, ceramic oscillation and the half-frequency divider stop. The CPU stops and the operations requiring the system clock (CL, 0) stop.

Release from STOP mode is with the RESET input only. All other functions cease to operate.

In order to minimize power consumption, the current flowing through the resistor ladder of the A/D converter must be minimized. To minimize power consumption, turn off the power to the V_{AREF} pin.

Note that ceramic oscillation stops and disables the system clock during STOP mode by bringing CL2 to ground. Therefore, if the external clock is connected to CL1 and a STOP instruction is executed, the CPU will enter HALT mode instead.

HALT Mode

In HALT mode, only the half-frequency divider circuit stops in the clock generator circuit (CL operates, ϕ stops). Therefore, the CPU and the operation of the serial interface (when using ϕ as a serial clock) stop.

However, since the clock control circuit is still in operation, it can select the CL signal from the clock generator or the EVENT input and supply the count pulse (CP) to the timer/event counter.

Consequently, the timer/event counter can be operated in HALT mode. The serial interface operates if a serial clock other than ϕ (such as the external clock, TOUT signal) is selected. The HALT mode is released by the RESET input or an interrupt, even if the interrupt is disabled.

Release from Standby Mode by Interrupt

The standby mode is released when the interrupt request flag is set by an interrupt source, whether interrupts are disabled or enabled. However, the operations after release differ in each case.

If the interrupt master enable F/F is enabled, and if the interrupt is enabled, the corresponding interrupt routine is initiated after execution of one instruction after the STOP/HALT instruction. Then, the result flag is reset. If the corresponding bit of the interrupt enable register has been reset, execution of instructions starts after the STOP/HALT instruction, and the interrupt routine is not initiated. In this case, the request flag for release remains set. If necessary, reset the request flag with the SKI instruction.

If the interrupt master enable F/F is disabled, the instruction following the STOP/HALT instruction is executed regardless of the state of the interrupt enable register (interrupt routine is not initiated). In this case, the interrupt request flag is left set. If necessary, it can be reset by the SKI instruction.

After any release, operation resumes with the same register contents as before standby mode.

Release From Standby Mode with RESET

Both STOP and HALT modes are released unconditionally by the RESET input. Figure 14 shows the release timing.

If the device is reset during STOP mode, the low to high transition of the RESET pin will take the processor from STOP mode to HALT mode. When RESET goes high to low, the HALT mode is abandoned, and after a normal reset operation, the PC is initialized to 0. Only the data memory will stay intact during the HALT mode, but all registers become undefined.

If the device is reset during HALT mode, the high to low transition of RESET will release the device from standby mode. After a normal reset operation, the PC is initialized to 0. Only the data memory will stay intact during the STOP mode, but all registers become undefined.

Figure 15 shows the release from HALT mode by RESET.

Figure 14. Release from STOP mode by RESET

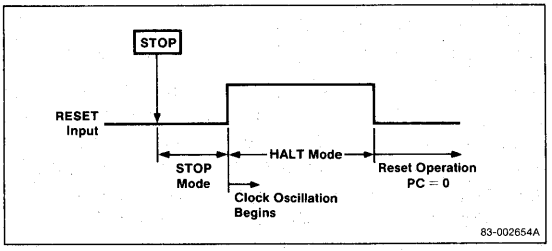
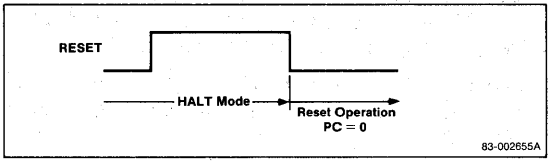


Figure 15. Release from HALT Mode by RESET



Reset Function

The μPD7533 is reset and initialized by the input of the RESET signal (active high).

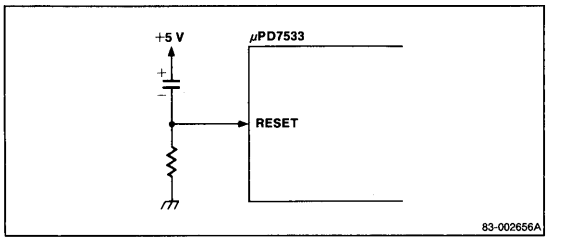
A RESET causes the CPU to initialize in the following manner:

- Program counter (PC) is cleared to 0
- Skip flags (SK1, SK0) and program status word (PSW) are reset to 0
- Timer/event counter:
  - — Count register = 00H
  - — Modulo register = FFH
  - — Timer-out F/F = 0
- Clock control circuitry:
  - — Clock mode register (CM_3-CM_0) = 0
  - — CP $= \frac{CL}{256}$
  - — Timer-out FF signal not output to PTOUT
  - — Prescalers 1-3 = 0
- Shift Mode Register (SM_3-SM_0) is cleared to 0.
  - — Shift operation stops
  - — Port 0 is in input mode (high impedance)
  - — INTS is selected interrupt source of INT0/S
- A/D converter circuit:
  - — ADM register is set to 0
  - — AN0 is selected
  - — SA register is set to 7FH
  - — EOC flag is set to logic 1
- Interrupt control circuit:
  - — Interrupt request flags = 0
  - — Interrupt master enable F/F = 0
  - — Interrupt enable register = 0
  - — All pending interrupts are cancelled
  - — All interrupts are disabled
- All Port 2-7 output buffers are turned off
- Contents of data memory and the following registers are undefined:
  - — Stack pointer (SP)
  - — Accumulator (A)
  - — Carry flag (C)
  - — General purpose registers (H,L)
  - — All port output latches
  - — Shift register

Power-on Reset Circuit

Figure 16 shows an example of the simplest power-on reset circuit using a resistor and a capacitor.

Figure 16. Power-on Reset Circuit



3

NEC
NEC Electronics Inc.

μPD7537A/38A 4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS WITH FIP® DRIVER

Description

The μPD7537A, μPD7538A, and μPD75CG38 are 4-bit, single-chip CMOS microcomputers with the μPD7500 architecture and FIP direct-drive capability.

Note: This data sheet pertains to μPD7537A, μPD7538A, and μPD75CG38. For simplification, the revision letter (A) usually is omitted from the part numbers within the data sheet.

The μPD7537 contains a 2048 × 8-bit ROM and a 128 × 4-bit RAM. The μPD7538 contains a 4096 × 8-bit ROM and a 160 × 4-bit RAM.

The μPD7537/38 contains two 4-bit general purpose registers located outside RAM. The subroutine stack is implemented in RAM for greater depth and flexibility. The μPD7537/38 typically executes 67 instructions with a 5 μs instruction cycle time.

The μPD7537/38 has one external and two internal edge-triggered hardware-vectored interrupts. An 8-bit timer/event counter and an 8-bit serial interface help to reduce software requirements.

Thirty-one high-voltage lines are organized into the 3-bit output port 2, the 4-bit output ports 3, 8, and 9, and the 4-bit I/O ports 4, 5, 10, and 11.

The low power consumption CMOS process allows the use of a power supply between 2.7 V and 6.0 V. Current consumption is less than 3.0 mA maximum, and can be further reduced in the halt and stop power-down modes.

The μPD75CG38 is a piggyback EPROM version of the μPD7537/38. Pin-compatible and function-compatible with the final, masked versions of the μPD7537/38, the μPD75CG38 is used for prototyping and for aiding in program development.

Features

- ☐ 67 instructions
- ☐ Instruction cycle:
  - — Internal clock: 5 μs/400 kHz, 5 V
  - — External clock: 4 μs/500 kHz, 5 V
- ☐ Upwardly compatible with the μPD7500 series product family
- ☐ 4,096 × 8-bit ROM (μPD7538/75CG38)
  2,048 × 8-bit ROM (μPD7537)
- ☐ 160 × 4-bit RAM (μPD7538/75CG38)
  128 × 4-bit RAM (μPD7537)
- ☐ 35 I/O lines
- ☐ 31 high-voltage output lines that can directly drive a vacuum fluorescent diplay (FIP)

FIP is the registered trademark for NEC's fluorescent indicator panel (vacuum fluorescent display).

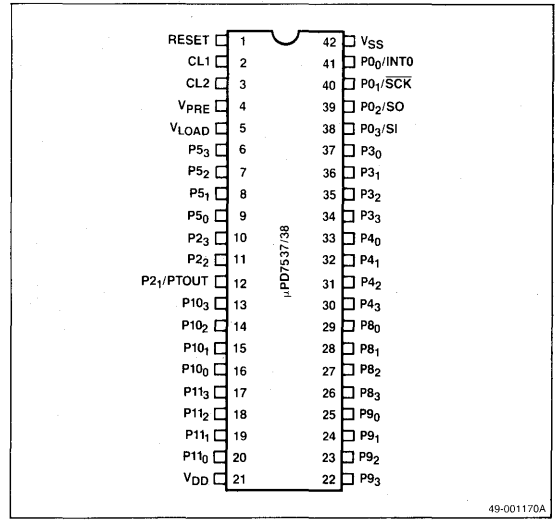
- ☐ Can select either a pull-down resistor or open-drain output per 31 high-voltage outputs (mask optional)
- ☐ Vectored interrupts: one external, two internal
- ☐ 8-bit timer/event counter
- ☐ 8-bit serial interface
- ☐ Standby function (HALT, STOP)
- ☐ Data retention mode
- ☐ Zero-cross detector on $P0_0$/INT0 input (mask optional)
- ☐ System clock (μPD7537/7538/75CG38): on-chip ceramic oscillator
- ☐ CMOS technology
- ☐ Low power consumption
- ☐ Single power supply
  - — μPD7537/7538: 2.7 V to 6.0 V
  - — μPD75CG38: 5.0 V ± 10%

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7537AC / 38AC	42-pin plastic DIP	610 kHz
μPD7537ACU / 38ACU	42-pin plastic shrink DIP	610 kHz
μPD75CG38E	42-pin ceramic piggyback DIP	500 kHz

Pin Configurations

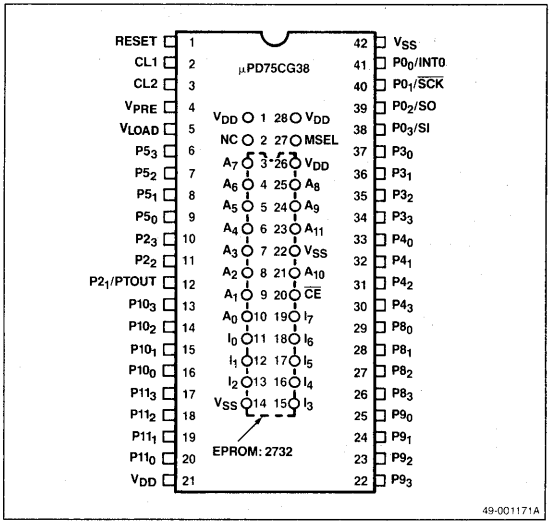
μPD7537/38 42-Pin Plastic DIP or Shrink DIP



3

Pin Configurations (cont)

μPD75G38 42-Pin Ceramic Piggyback DIP



Pin Identification

μPD7537/38 and μPD75CG38

No.	Symbol	Function
1	RESET	Reset input
2, 3	CL1, CL2	Clock pins
4	V_{PRE}	High-voltage output predriver supply
5	V_{LOAD}	High-voltage output option resistor supply
6–9	$P5_0$–$P5_3$	High-voltage I/O port 5
10, 12	$P2_3$, $P2_2$ $P2_1$/PTOUT	High-voltage output port 2, and output port from timer/event counter (PTOUT)
13–16	$P10_0$–$P10_3$	High-current, high-voltage I/O port 10
17–20	$P11_0$–$P11_3$	High-voltage, high-current I/O port 11
21	V_{DD}	Positive power supply
22–25	$P9_0$–$P9_3$	High-voltage, high-current output port 9
26–29	$P8_0$–$P8_3$	High-voltage, high-current output port 8
30–33	$P4_0$–$P4_3$	High-voltage I/O port 4
34–37	$P3_0$–$P3_3$	High-voltage output port 3
38 39 40 41	$P0_3$/SI $P0_2$/SO $P0_1$/SCK $P0_0$/INT0	4-bit input of port 0; or serial data input (SI), serial data output (SO), serial clock I/O (SCK), and external interrupt input (INT0) or zero-cross detect input ($P0_0$).
42	V_{SS}	Ground

μPD75CG38 EPROM

No.	Symbol	Function
1	V_{DD}	Connection to pin 21 of μPD75CG38
2	NC	No connection
3–10, 21, 24, 25	A_0–A_{10}	EPROM address output
11–13, 15–19	I_0–I_7	Data read input from the EPROM
14	V_{SS}	Connection to EPROM GND pin
20	CE	Chip enable output
22	V_{SS}	Supplies EPROM OE signal
23	A_{11}	Program counter MSB output
26	V_{DD}	Supplies V_{CC} to the EPROM
27	MSEL	Mode select input
28	V_{DD}	Supplies high-level signal to MSEL

Note:

(1) Output drivers on ports 2–5 and 8–11 are mask-optional. Accordingly, either an open-drain output or a pull-down resistor can be selected. V_{LOAD} is suitable for an output driver with a pull-down resistor.

(2) Ports 2–5 are suitable as FIP segment signal outputs, and ports 8–11 are suitable for FIP digit signal outputs.

(3) Ports 8–11 have high-current drive capability and can drive an LED directly.

Pin Functions, μPD7537/38 and μPD75CG38

RESET

System reset (input).

CL1, CL2

Connection to the ceramic oscillator. CL1 is the external clock input.

V_{PRE}

Negative power supply for high-voltage output predrivers (for ports 2–5, 8–11).

V_{LOAD}

Negative power supply for optional load resistors (pull-down resistors) of high-voltage output drivers (for ports 2–5, 8–11). This pin is only on the μPD7537/38.

$P5_3$–$P5_0$

4-bit, high-voltage I/O port 5.

$P2_1$–$P2_3$

3-bit, high-voltage output port 2.

PTOUT

Output port for the timer/event counter.

$P10_3$-$P10_0$

4-bit, high-voltage, high-current I/O port 10. Capable of bit set/reset by SPBL/RPBL instructions.

$P11_3$-$P11_0$

4-bit, high-voltage, high-current I/O port 11. Capable of bit set/reset by SPBL/RPBL instructions.

V_{DD}

Positive power supply.

$P9_3$-$P9_0$

4-bit, high-voltage, high-current output port 9. Capable of bit set/reset by SPBL/RPBL instructions.

$P8_3$-$P8_0$

4-bit, high-voltage, high-current output port 8. Capable of bit set/reset by SPBL/RPBL instructions.

$P4_3$-$P4_0$

4-bit, high-voltage I/O port 4.

$P3_3$-$P3_0$

4-bit, high-voltage output port 3.

$P0_0$-$P0_3$

4-bit input port 0. $P0_0$ is also used as the zero-cross detection input.

SI

Serial data input.

SO

Serial data output.

$\overline{SCK}$

Serial I/O clock.

INT0

External interrupt input.

V_{SS}

Ground.

Pin Functions, μPD75CG38 EPROM

MSEL

Changes the addressing area of the external EPROM and the on-chip RAM (with a pull-down resistor). Connecting a jumper between socket pins 27 (MSEL) and 28 (V_{DD}) selects μPD7537 mode (2-Kbyte EPROM, 128 × 4-bit RAM). Leaving MSEL open selects μPD7538 mode (4-Kbyte EPROM, 160 × 4-bit RAM).

A_0-A_{10}

Output the low-order 11 bits of the program counter (PC_0-PC_{10}). Used as EPROM address signals.

A_{11}

When MSEL is high level, A_{11} outputs high-level signals. When MSEL is open, A_{11} outputs the MSB of the PC, which is used as the most significant address signal of the 4-Kbyte EPROM 2732.

I_0-I_7

Input data read from the EPROM.

$\overline{CE}$

Outputs the chip enable signal to the EPROM.

V_{DD}

Pin 26 is electrically equivalent to the bottom V_{DD} pin and is used to supply V_{CC} to the EPROM. Pin 28 is electrically equivalent to the bottom V_{DD} pin and is used to supply the high level signal to MSEL. Pin 1 connects to pin 21 of μPD75CG38.

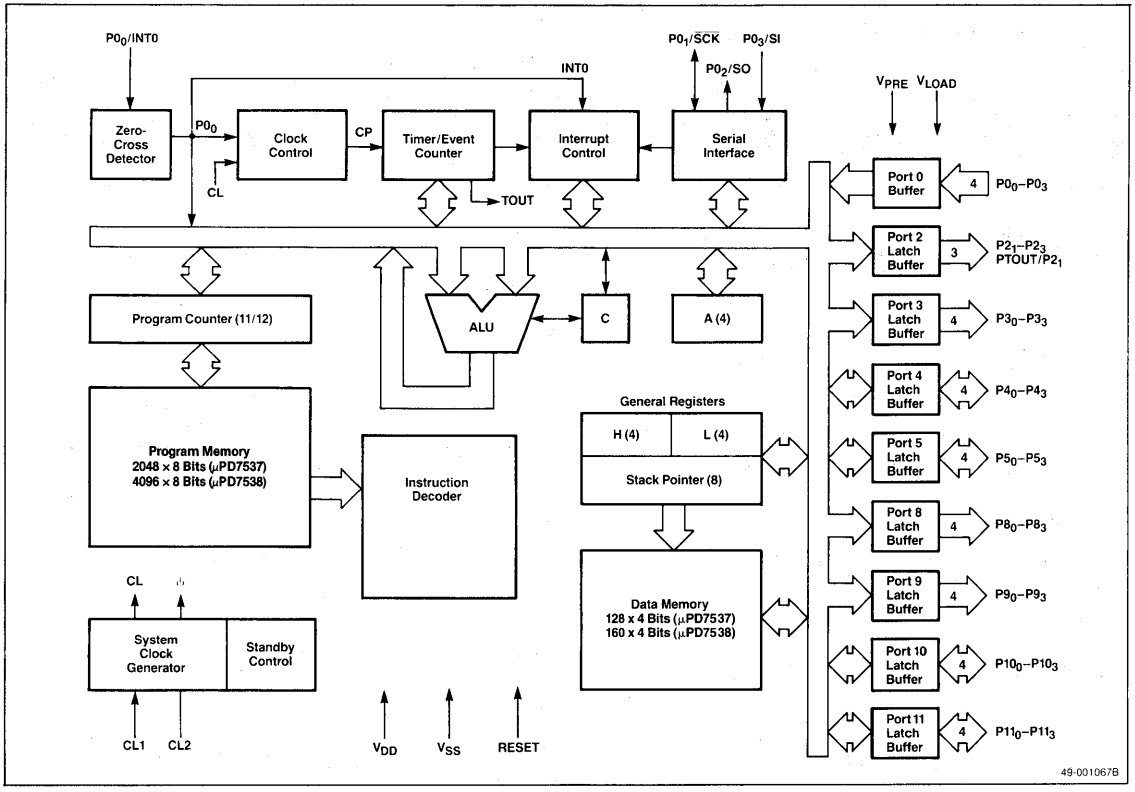
V_{SS}

Pin 14 is electrically equivalent to the bottom V_{SS} pin in voltage, and is connected to the EPROM GND pin. Pin 22 is electrically equivalent to the bottom V_{SS} pin and is used to supply the OE signal to the EPROM.

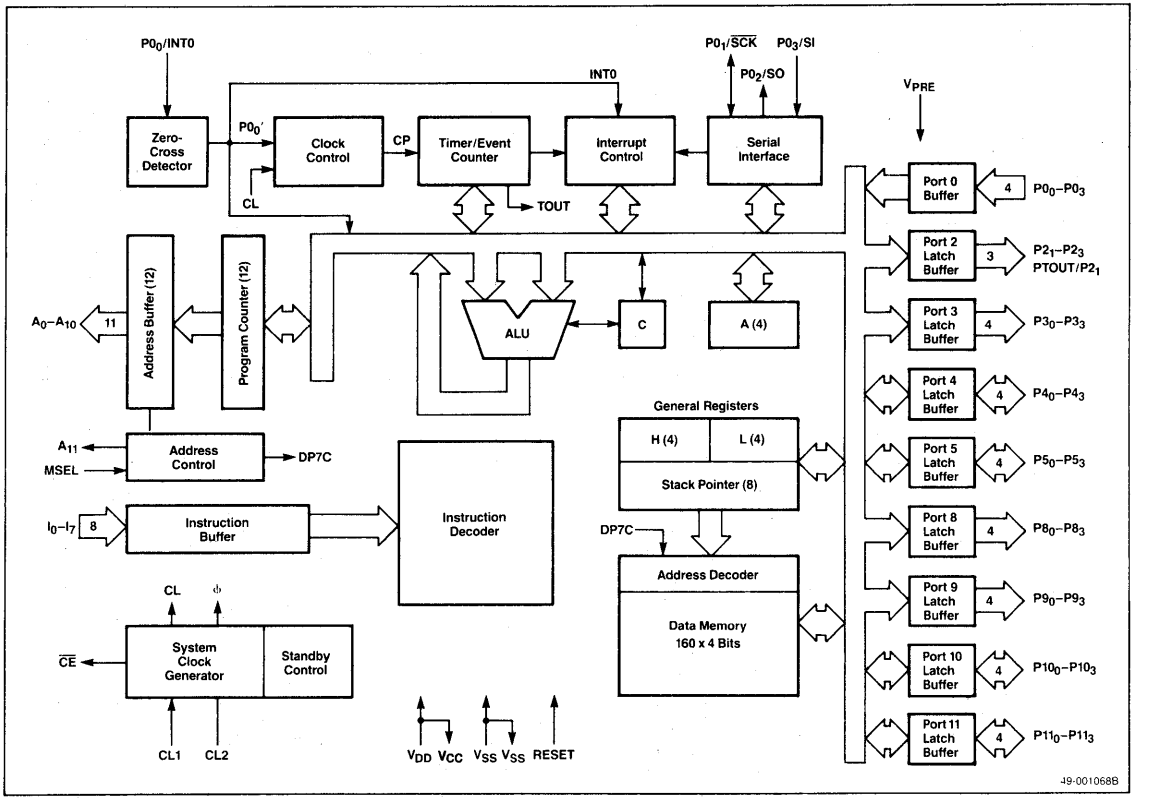
Instruction Set

Refer to the User's Manual. The instruction set appears also as subset A4 in the data sheet for the μPD7500 series of single-chip microcomputers.

Block Diagram, μPD7537/38



Block Diagram, μPD75CG38



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 V to +7 V
Power supply voltage, V_{LOAD}(μPD7537 / 38)	V_{DD} − 40 V to V_{DD} +0.3 V
Power supply voltage, V_{PRE}	V_{DD} − 12 V to V_{DD} +0.3 V
Input voltage, except ports 4, 5, 10, 11, V_{IN}	−0.3 V to V_{DD} +0.3 V
Input voltage, ports 4, 5, 10, 11, V_{IN}	V_{DD} − 40 V to V_{DD} +0.3 V
Output voltage, except ports 2–5, 8–11, V_O	−0.3 V to V_{DD} +0.3 V
Output voltage, ports 2–5, 8–11, V_O	V_{DD} − 40 V to V_{DD} +0.3 V
Output current high, per pin: $P0_1$, $P0_2$; I_{OH}	−15 mA
Output current high, per pin: ports 2–5, 8–11; I_{OH}	−30 mA
Output current high, ports 3, 4, 8, 9 total, I_{OH}	−55 mA
Output current high, ports 2, 5, 10, 11 total, I_{OH}	−55 mA
Output current low, per pin, I_{OL}	15 mA
Output current low, all ports total, I_{OL}	15 mA
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = 0$ V, f = 1.0 MHz, Unmeasured pins returned to GND

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	$P0_0$–$P0_3$
Output capacitance	C_O			15	pF	Port 2
				35	pF	Ports 3, 8, 9
I/O capacitance	C_{IO}			15	pF	$P0_1$, $P0_2$
				35	pF	Ports 4, 5, 10, 11

DC Characteristics

μPD7537/38

$T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, low	V_{IL1}	0		$0.3V_{DD}$	V	Port 0, RESET
	V_{IL2}	0		0.5	V	CL1
	V_{IL3}	$V_{DD}-35$		$0.3V_{DD}$	V	Ports 4, 5, 10, 11
Input voltage, high	V_{IH1}	$0.7V_{DD}$		V_{DD}	V	Port 0, RESET
	V_{IH2}	$V_{DD}-0.5$		V_{DD}	V	CL1
	V_{IH3}	$0.7V_{DD}$		V_{DD}	V	Ports 4, 5, 10, 11; $4.5\,V \leq V_{DD} \leq 6.0\,V$
		$V_{DD}-0.5$		V_{DD}	V	Ports 4, 5, 10, 11; $2.7\,V \leq V_{DD} < 4.5\,V$
Output voltage, low	V_{OL}			0.4	V	PO_1, PO_2; $4.5\,V \leq V_{DD} \leq 6.0\,V$; $I_{OL} = 1.6$ mA
				0.5	V	PO_1, PO_2; $I_{OL} = 400\,\mu A$
Output voltage, high	V_{OH}	$V_{DD}-2.0$			V	Ports 2–5, $I_{OH} = -4$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH} = -10$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 2–5, $I_{OH} = -2$ mA (Note 2)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH} = -5$ mA (Note 2)
		$V_{DD}-1.0$			V	PO_1, PO_2; $I_{OH} = -1$ mA (Note 3)
		$V_{DD}-0.5$			V	PO_1, PO_2; $I_{OH} = -100\,\mu A$
Input leakage current, low	I_{LIL1}			−3	μA	$V_{IN} = 0$ V; $P0_0$ (Note 4)–$P0_3$
	I_{LIL2}			−40	μA	$V_{IN} = 0$ V; $P0_0$ (Note 5)
	I_{LIL3}			−20	μA	$V_{IN} = 0$ V; CL1
	I_{LIL4}			−10	μA	$V_{IN} = V_{DD} - 35$ V; ports 4, 5, 10, 11
Input leakage current, high	I_{LIH1}			3	μA	$V_{IN} = V_{DD}$; $P0_0$ (Note 4)–$P0_3$
	I_{LIH2}			40	μA	$V_{IN} = V_{DD}$; $P0_0$ (Note 5)
	I_{LIH3}			20	μA	$V_{IN} = V_{DD}$; CL1
	I_{LIH4}			80	μA	$V_{IN} = V_{DD}$; ports 4, 5, 10, 11
Output leakage current, low	I_{LOL1}			−3	μA	$V_O = 0$ V; PO_1, PO_2
	I_{LOL2}			−10	μA	$V_O = V_{DD} - 35$ V; ports 2–5, 8–11

μPD7537/38

$T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output leakage current, high	I_{LOH1}			3	μA	$V_O = V_{DD}$; except ports 4, 5, 10, 11
	I_{LOH2}			80	μA	$V_O = V_{DD}$; ports 4, 5, 10, 11
Supply current, normal operation	I_{DD1}		1.5	4.0	mA	$V_{DD} = 5\,V \pm 10\%$, $f_{CC} = 600$ kHz
Supply current, HALT mode (Note 6)	I_{DD2}		700	1800	μA	$V_{DD} = 5\,V \pm 10\%$, $f_{CC} = 600$ kHz (Note 4)
			230	700	μA	$V_{DD} = 3\,V \pm 10\%$, $f_{CC} = 600$ kHz (Note 4)
			710	1840	μA	$V_{DD} = 5\,V \pm 10\%$, $f_{CC} = 600$ kHz (Note 5)
			237	730	μA	$V_{DD} = 3\,V \pm 10\%$, $f_{CC} = 600$ kHz (Note 5)
Supply current, STOP mode (Note 6)	I_{DD3}		0.1	10	μA	(Notes 4, 6)
			10	40	μA	$V_{DD} = 5\,V \pm 10\%$ (Note 5)
			7	30	μA	$V_{DD} = 3$ V (Note 5)

Note:

(1) $V_{PRE} = V_{DD} - 9\,V \pm 1\,V$. The circuit in figure 5 is recommended.

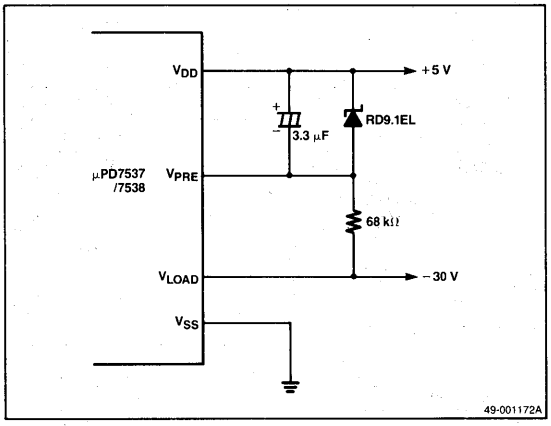
(2) $V_{PRE} = 0$ V. $V_{DD} = 4.5$ V to 6.0 V.

(3) $V_{DD} = 4.5$ V to 6.0 V.

(4) Without zero-cross detector.

(5) With zero-cross detector.

Figure 1. Recommended Circuit, μPD7537/7538



DC Characteristics (cont)

μPD75CG38

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage, low	V_{IL1}	0		$0.3V_{DD}$	V	Port 0, RESET
	V_{IL2}	0		0.5	V	CL1
	V_{IL3}	$V_{DD}-35$		$0.3V_{DD}$	V	Ports 4, 5, 10, 11
Input voltage, high	V_{IH1}	$0.7V_{DD}$		V_{DD}	V	Port 0, RESET
	V_{IH2}	$V_{DD}-0.5$		V_{DD}	V	CL1
	V_{IH3}	$0.7V_{DD}$		V_{DD}	V	Ports 4, 5, 10, 11
Output voltage, low	V_{OL}			0.4	V	PO_1, PO_2; $I_{OL}=1.6$ mA
				0.5	V	PO_1, PO_2; $I_{OL}=400\mu A$
Output voltage, high	V_{OH}	$V_{DD}-2.0$			V	Ports 2–5, $I_{OH}=-4$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH}=-10$ mA (Note 1)
		$V_{DD}-2.0$			V	Ports 2–5, $I_{OH}=-2$ mA (Note 2)
		$V_{DD}-2.0$			V	Ports 8–11, $I_{OH}=-5$ mA (Note 2)
		$V_{DD}-1.0$			V	PO_1, PO_2; $I_{OH}=-1$ mA (Note 2)
Input current, low (I_0–I_7)	I_{IL}			−200	μA	$V_{IN}=0$ V
Input current, high (MSEL)	I_{IH}			300	μA	$V_{IN}=V_{DD}$
Input leakage current, low	I_{LIL1}			−3	μA	$V_{IN}=0$ V; PO_1–PO_3
	I_{LIL2}			−40	μA	$V_{IN}=0$ V; PO_0
	I_{LIL3}			−20	μA	$V_{IN}=0$ V; CL1
	I_{LIL4}			−10	μA	$V_{IN}=V_{DD}-35$ V; ports 4, 5, 10, 11
Input leakage current, high	I_{LIH1}			3	μA	$V_{IN}=V_{DD}$; PO_1–PO_3
	I_{LIH2}			40	μA	$V_{IN}=V_{DD}$; PO_0
	I_{LIH3}			20	μA	$V_{IN}=V_{DD}$; CL1
	I_{LIH4}			80	μA	$V_{IN}=V_{DD}$; ports 4, 5, 10, 11
Output leakage current, low	I_{LOL1}			−3	μA	$V_O=0$ V; PO_1, PO_2
	I_{LOL2}			−10	μA	$V_O=V_{DD}-35$ V; ports 2–5, 8–11

μPD75CG38

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output leakage current, high	I_{LOH1}			3	μA	$V_O=V_{DD}$; except ports 4, 5, 10, 11
	I_{LOH2}			80	μA	$V_O=V_{DD}$; ports 4, 5, 10, 11
Supply current, normal operation	I_{DD1}		1.0	3.0	mA	$f_{CC}=400$ kHz
Supply current, HALT mode (Note 3)	I_{DD2}		460	1230	μA	$f_{CC}=400$ kHz
Supply current, STOP mode (Note 3)	I_{DD3}		10	40	μA	

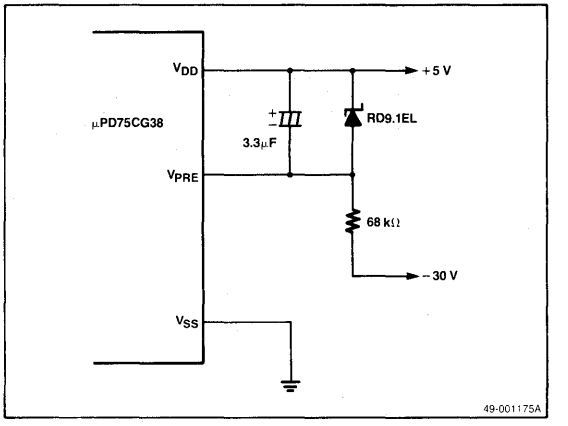
Note:

(1) $V_{PRE} = V_{DD} - 9V \pm 1V$. The circuit in figure 6 is recommended.

(2) $V_{PRE} = 0V$

(3) Ports 4, 5, 10, 11 are output off or low input.

Figure 2. Recommended Circuit, μPD75CG38

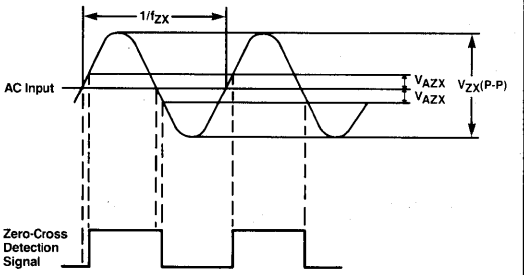


Zero-Cross Detection Characteristics

μPD7537/38: $T_A = -10°C$ to $+70°C$, $V_{DD} = 4.5$ V to 6.0 V
μPD75CG38: $T_A = -10°C$ to $+70°C$, $V_{DD} = +5$ V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Zero-cross detection input voltage	V_{ZX}(P-P)	1.0		3.0	V_{P-P}	AC coupled, C = 0.1 μF
Zero-cross accuracy	V_{AZX}			±100	mV	50 Hz to 60 Hz sine wave
Zero-cross detection input frequency	f_{ZX}	45		1000	Hz	

Zero-Cross Detection Waveform



Note: In the above waveforms, both 0-to-1 and 1-to-0 transitions of the zero-cross detection signal delay from the low-to-high and high-to-low transitions of the AC input signal, respectively. However, it is possible that the zero-cross detection leads low-to-high and/or high-to-low transition(s) of the AC input signal.

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AC Characteristics

μPD7537/38

$T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Cycle time (Note 1)	t_{CY}	3.3		200	μs	V_{DD} = 4.5 V to 6.0 V
		9.5		200	μs	
$P0_0$ event input frequency	f_{P0}	0		610	kHz	V_{DD} = 4.5 V to 6.0 V
		0		210	kHz	
$P0_0$ input rise time	t_{P0R}			0.2	μs	
$P0_0$ input fall time	t_{P0F}			0.2	μs	
$P0_0$ input pulse width, low	t_{P0L}	2.3			μs	
$P0_0$ input pulse width, high	t_{P0H}	0.62			μs	V_{DD} = 4.5 V to 6.0 V
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	Input; V_{DD} = 4.5 V to 6.0 V
		3.3			μs	Output; V_{DD} = 4.5 V to 6.0 V
		8.0			μs	Input
		9.5			μs	Output
$\overline{SCK}$ pulse width, low	t_{KL}	4.0			μs	Input
		4.7			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	1.3			μs	Input; V_{DD} = 4.5 V to 6.0 V
		1.45			μs	Output; V_{DD} = 4.5 V to 6.0 V
SI set-up time (to rising-edge of $\overline{SCK}$)	t_{SIK}	300			ns	
SI hold time (after rising-edge of $\overline{SCK}$)	t_{KSI}	450			ns	
SO output delay time (after falling-edge of $\overline{SCK}$)	t_{KSO}			850	ns	V_{DD} = 4.5 V to 6.0 V
				1200	ns	
INT0 pulse width, high, low	t_{I0H}, t_{I0L}	10			μs	
RESET pulse width, high, low	t_{RSH}, t_{RSL}	10			μs	

Note:
(1) $t_{CY} = 2/f_{CC}$ or $2/f_C$

AC Characteristics (cont)

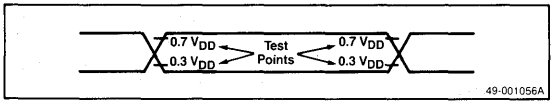
μPD75CG38

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Cycle time (Note 1)	t_{CY}	4.0		200	μs	
$P0_0$ event input frequency	f_{P0}	0		500	kHz	
$P0_0$ input rise time	t_{P0R}			0.2	μs	
$P0_0$ input fall time	t_{P0F}			0.2	μs	
$P0_0$ input pulse width, high, low	t_{P0H}, t_{P0L}	0.8			μs	
$\overline{SCK}$ cycle time	t_{KCY}	3.0			μs	Input
		4.0			μs	Output
$\overline{SCK}$ pulse width, low	t_{KL}	1.8			μs	Output
$\overline{SCK}$ pulse width, high	t_{KH}	1.3			μs	Input
SI set-up time (to rising-edge of $\overline{SCK}$)	t_{SIK}	300			ns	
SI hold time (after rising-edge of $\overline{SCK}$)	t_{KSI}	450			ns	
SO output delay time (after falling-edge of $\overline{SCK}$)	t_{KSO}			850	ns	
INT0 pulse width, high, low	t_{I0H}, t_{I0L}	10			μs	
RESET pulse width, high, low	t_{RSH}, t_{RSL}	10			μs	
Data input delay time from address	t_{ACC}			700	ns	
Data input delay time from $\overline{CE}$	t_{CE}			700	ns	
Input hold time after address	t_{IH}	0			ns	

Note:
(1) $t_{CY} = 2/f_{CC}$ or $2/f_C$

AC Waveform Measurement Points (Except CL1)



Oscillation Characteristics

μPD7537/38

$T_A = -10°C$ to $+70°C$, $V_{DD} = 2.7V$ to $6.0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency (Note 1)	f_{CC}	390	400	410	kHz	(Note 2) $V_{DD} = 4.5$ to $6.0V$
Oscillation stable time (Note 1)	t_{OS}	20			ms	(Note 3)
System clock CL1 input frequency (Note 4)	f_C	10		500	kHz	$V_{DD} = 4.5V$ to $6.0V$
		10		210	kHz	
CL1 input rise time	t_{CR}			0.2	μs	
CL1 input fall time	t_{CF}			0.2	μs	
CL1 input pulse width, low	t_{CL}	2.0		50	μs	
CL1 input pulse width, high	t_{CH}	0.8		50	μs	$V_{DD} = 4.5V$ to $6.0V$

Note:
(1) Ceramic resonator: CSB400P (MURATA) or KBR-400B (KYO-CERA) is recommended (see figure 3).

(2) Oscillation is only guaranteed at $3V \leqslant V_{DD} \leqslant 4.5V$.

(3) After V_{DD} reaches 4.5 V.

(4) External clock (see figure 4).

μPD75CG38

$T_A = -10°C$ to $+70°C$, $V_{DD} = 5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
System clock oscillation frequency (Note 1)	f_{CC}	390	400	410	kHz	
Oscillation stable time (Note 1)	t_{OS}	20			ms	After V_{DD} reaches 4.5 V
System clock CL1 input frequency (Note 2)	f_C	10		500	kHz	
CL1 input rise time	t_{CR}			0.2	μs	
CL1 input fall time	t_{CF}			0.2	μs	
CL1 input pulse width high, low	t_{CH}, t_{CL}	0.8		50	μs	

Note:
(1) Ceramic resonator: CSB400P (MURATA) is recommended; C = 300 pF (see figure 3).

(2) External clock (see figure 4).

Figure 3. Recommended Circuit, μPD7537/7538

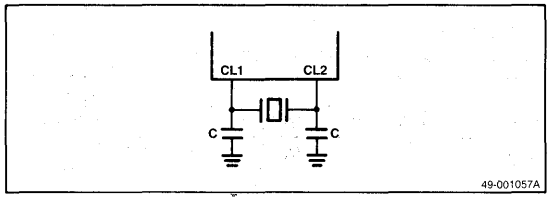
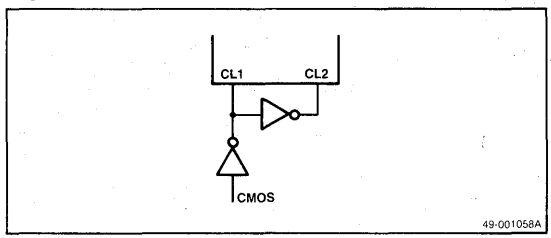


Figure 4. Recommended Circuit, μPD75CG38



Stop Mode Low Voltage Data Retention Characteristics

μPD7537/38

$T_A = -10°C$ to $+70°C$, $V_{DD} = 2.7\,V$ to $6.0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		6.0	V	
Data retention supply current	I_{DDDR}		0.1	10	μA	$V_{DDDR} = 2\,V$ (Note 1)
			7	30	μA	$V_{DDDR} = 2\,V$ (Note 2)
RESET set-up time	t_{SRS}	0			μs	
Oscillation stable time	t_{OS}	20			ms	After V_{DD} reaches 4.5 V

μPD75CG38

$T_A = -10°C$ to $+70°C$, $V_{DD} = 5\,V \pm 10\%$

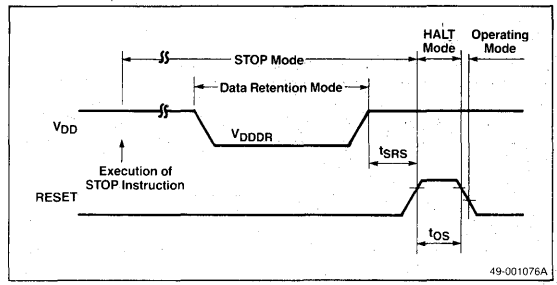
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		5.5	V	
Data retention supply current	I_{DDDR}		7	30	μA	$V_{DDDR} = 2\,V$
RESET set-up time	t_{SRS}	0			μs	
Oscillation stable time	t_{OS}	20			ms	After V_{DD} reaches 4.5 V

Note:

(1) Without zero-cross detector.

(2) With zero-cross detector.

Data Retention Mode Timing



μPD75CG38 EPROM Interface

A 4-Kbyte EPROM (2732) plugs into socket pins on top of the μPD75CG38. A high input to MSEL selects the μPD7537 mode and fixes the A_{11} output high level in order to access the upper 2-Kbytes of the 4-Kbyte EPROM. When MSEL is open, μPD7538 mode is selected. All EPROM addresses can be accessed because A_{11} functions as the MSB of the address. Figure 5 shows the address control unit. Figures 6 and 7 show the μPD75CG38 connected with the 2732.

Figure 8 shows the EPROM read timing. Data is read into the instruction buffer at the end of the T4 state. The chip enable ($\overline{CE}$) signal is made active during 2 states (T3, T4) in order to decrease the power consumption of the EPROM.

Figure 5. Address Control Unit

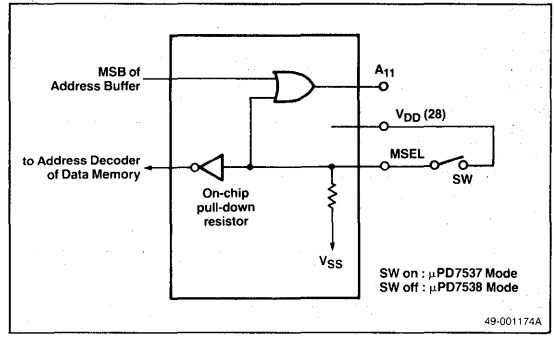


Figure 6. Connection with the 2732 (μPD7537 Mode)

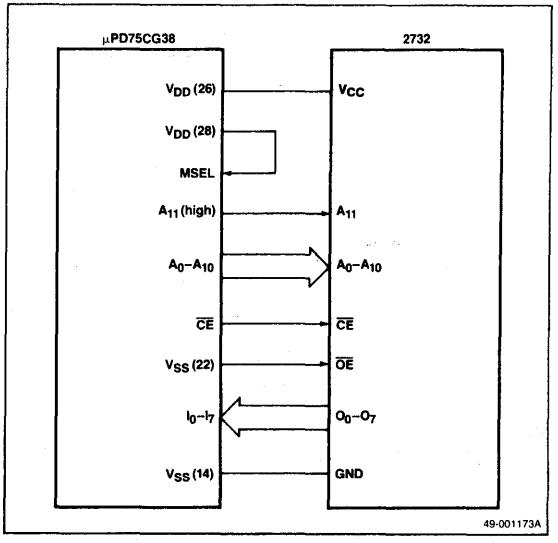


Figure 7. Connection with the 2732 (μPD7538 Mode)

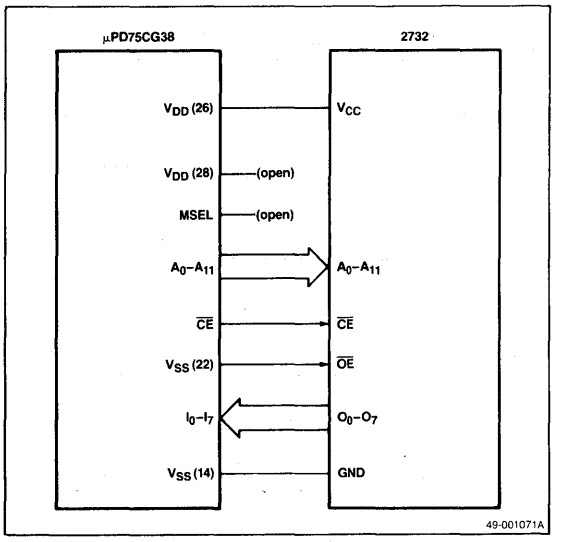
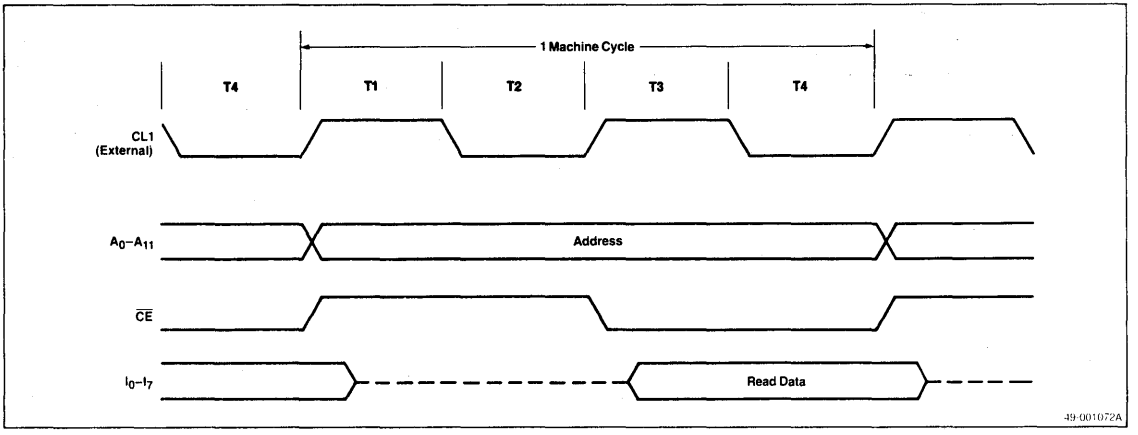
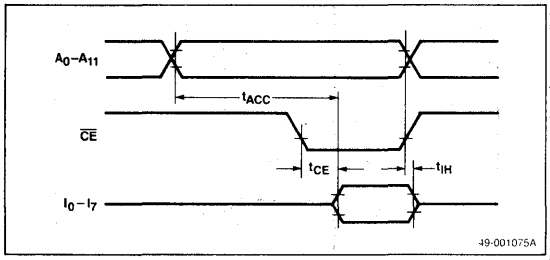


Figure 8. EPROM Read Timing

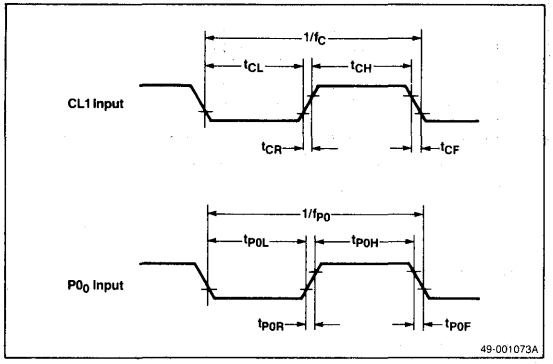


Timing Waveforms

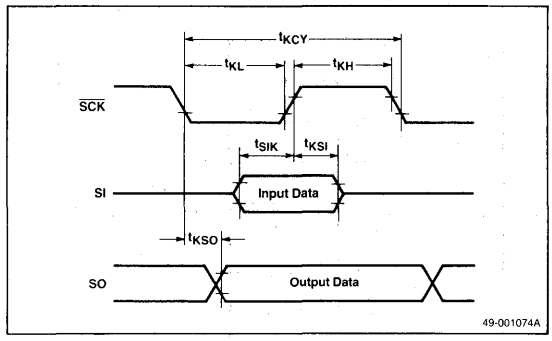
EPROM (μPD75CG38 only)



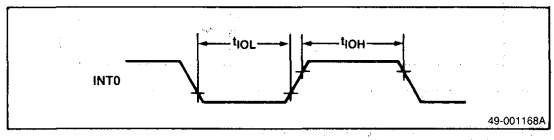
Clock



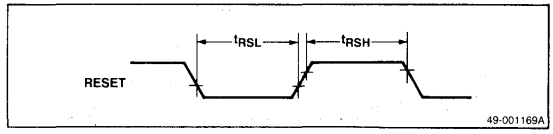
Serial Interface



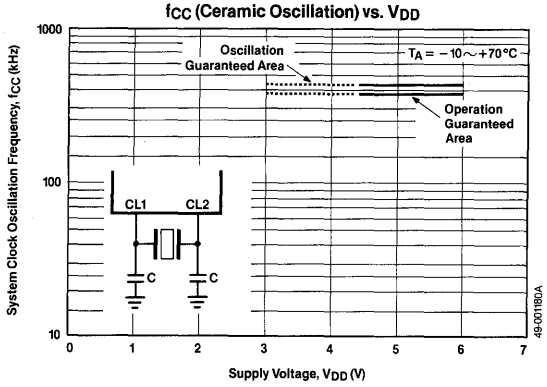
Interrupt Input

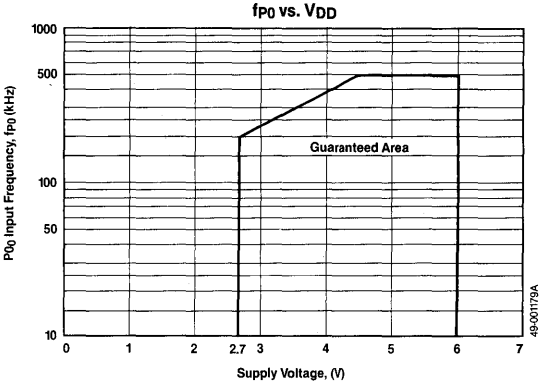


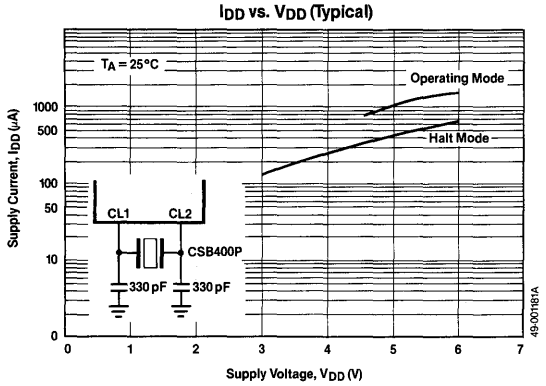
Reset Input

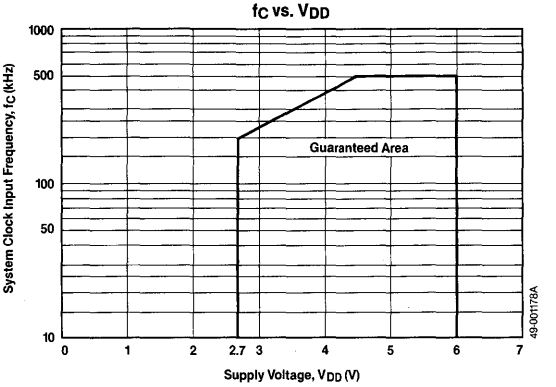


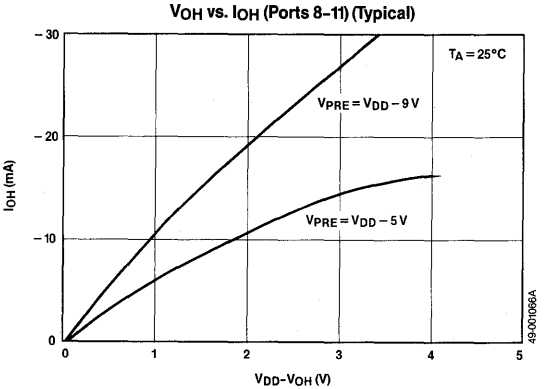
Operating Characteristics

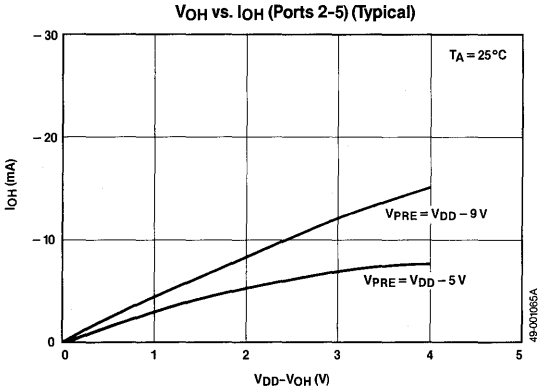












Differences Among the μPD7537/38/CG38

	μPD75CG38	μPD7537	μPD7538
Program memory	4 Kbyte EPROM (2732) connectable on top	On-chip 2 Kbyte ROM	On-chip 4 Kbyte ROM
Data memory (RAM)	160×4	128×4	160×4
High-voltage output lines	All open-drain outputs	On-chip load capacitor or open drain output (bit by bit, mask optional)	
V_{LOAD} pin	No	Yes	
Zero-cross detection	Yes	Mask optional	
Package	42-pin ceramic piggyback DIP bottom pin compatible with μPD7537/38	42-pin plastic DIP 42-pin plastic shrink DIP	
Power supply	5 V	2.7 V to 6.0 V	

NEC

NEC Electronics Inc.

μPD7554/64
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTES WITH SERIAL I/O

PRELIMINARY INFORMATION

Description

The μPD7554 and μPD7564 are low-end versions of μPD7500 series products. These microcomputers incorporate a serial interface and are useful as slave CPUs to high-end μPD7500 series or 8-bit μCOM-87 series products.

The μPD7554/7564 has output ports that can directly drive triacs and LEDs. Also, various mask-optional I/O circuits can be configured for a wide selection of outputs allowing a reduction of external circuitry in your design.

The μPD7554 and μPD7564 differ only in their clock circuitry. The μPD7554 uses an external resistor with an internal capacitor for an RC oscillator clock, where the μPD7564 uses an external ceramic oscillator as a clock. These microcomputers are ideally suited to control devices such as plain paper copiers (PPCs), printers, VCRs, and audio equipment.

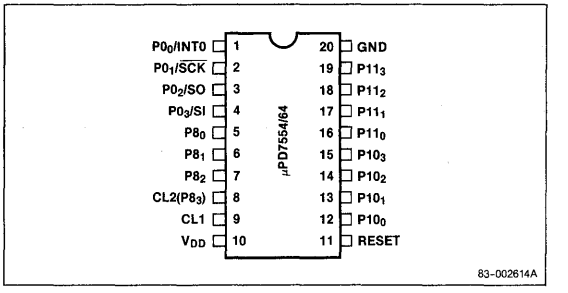
Features

- ☐ 47 instructions (subset of μPD7500 set B)
- ☐ Instruction cycle:
  - External clock: 2.86 μs/700 kHz, 5 V
  - RC oscillator (μPD7554): 4 μs/500 kHz, 5 V
  - Ceramic oscillator (μPD7564): 3 μs/660 kHz, 5 V
- ☐ Program memory (ROM) of 1024 x 8-bits
- ☐ Data memory (RAM) of 64 x 4-bits
- ☐ 8-bit timer/event counter
- ☐ 8-bit serial interface
- ☐ 16 I/O lines
- ☐ Data memory retention at low supply voltage
- ☐ CMOS technology
- ☐ Low power consumption
- ☐ Single power supply (2.5 V to 6.0 V) μPD7554
  (2.7 V to 6.0 V) μPD7564

Ordering Information

Part Number	Package Type
μPD7554CS	20-pin plastic shrink DIP
μPD7564CS	20-pin plastic shrink DIP
μPD7554G	20-pin plastic SO
μPD7564G	20-pin plastic SO

Pin Configuration



Pin Identification

No.	Symbol	Function
1-4	$P0_0$/INT0 $P0_1$/$\overline{SCK}$ $P0_2$/SO $P0_3$/SI	4-bit input port 0/count clock input/serial interface
5-8	$P8_0$-$P8_2$ $P8_3$/CL_2	4-bit output port 8 Connection for ceramic resonator or RC.
9	CL1	Connection for ceramic resonator or RC
10	V_{DD}	+5 V power supply
11	RESET	Reset input pin
12-15	$P10_1$-$P10_3$	4-bit I/O port 10
16-19	$P11_0$-$P11_3$	4-bit I/O port 11
20	GND	Ground

Pin Functions

$P0_0$/INT0, $P0_1$/$\overline{SCK}$
$P0_2$/SO, $P0_3$/SI
(Port 0/count clock input/serial interface)

4-bit input port 0/count clock input/serial I/O interface. This port can be configured as a 4-bit parallel input port or as the 8-bit serial I/O interface, under control of the serial mode select register. The serial input SI (active high), serial output SO (active low), and the serial clock $\overline{SCK}$ (active low—synchronizes data transfer) comprise the 8-bit serial I/O interface. If $P0_0$/INT0 is unused, connect it to ground. If any of $P0_1$-$P0_3$ are unused, connect them to ground or V_{DD}. The port is in the input state at reset.

3

$P8_0$-$P8_2$ $P8_3$/CL2 (Port 8/clock input 2)

4-bit output port 8. This port can sink 15 mA and interface 12 V. On the μPD7554, the port function of $P8_3$/CL2 is specified by mask option. $P8_3$ is a normal output port on the μPD7564. On the μPD7554, CL2 is one of the pins to which a resistor for RC oscillation is connected. On the μPD7564, CL2 is one of the pins to which a ceramic resonator is connected. If any of $P8_0$-$P8_2$ pins are unused, leave them open. The port is in the high impedance state at reset.

CL1 (Clock input 1)

On the μPD7554, CL1 is one of the two pins to which a resistor for RC oscillation is connected. On the μPD7564, CL1 is one of the two pins to which a ceramic resonator is connected.

V_{DD} (Power supply)

Positive power supply.

RESET (Reset)

System reset input pin (active high). This pin can be internally connected to a pull-down resistor if specified by mask option.

$P10_0$-$P10_3$ (Port 10)

4-bit I/O port. This port can sink 10 mA and interface 12 V. If any of these pins are unused, connect them to ground or V_{DD} in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset.

$P11_0$-$P11_3$ (Port 11)

4-bit I/O port. This port can sink 10 mA and interface 12 V. If any of these pins are unused, connect them to ground or V_{DD} in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset.

GND (Ground)

Ground.

Pin Mask Options

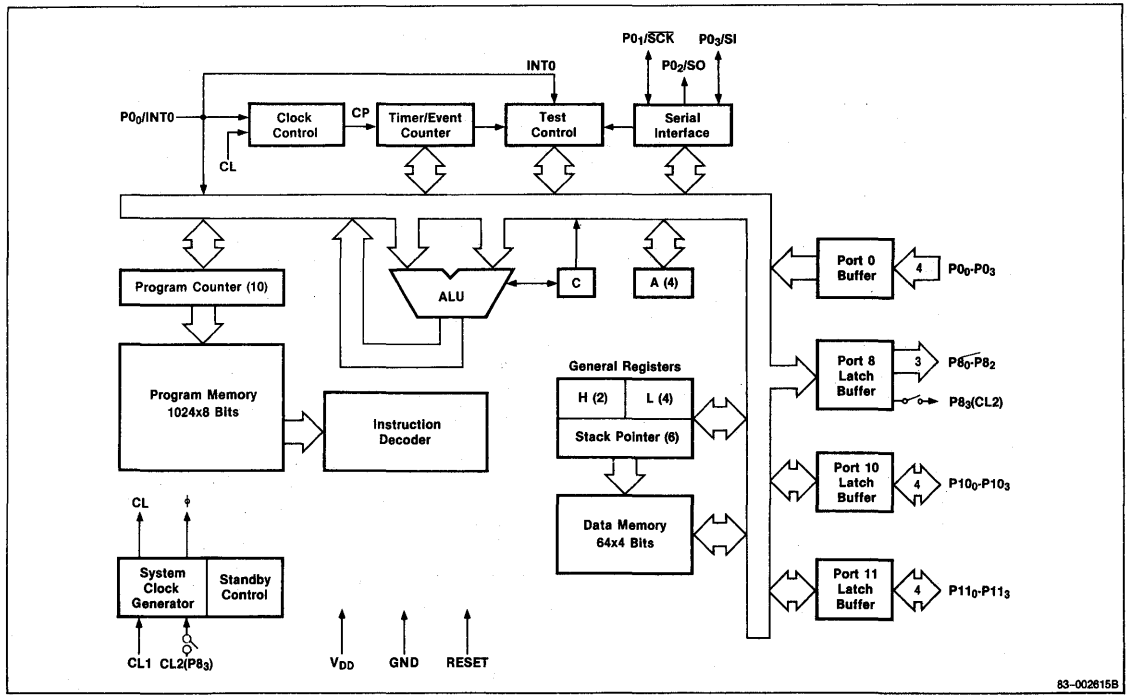
Table 1 shows the mask options for all the port pins and the RESET pin. You may select these options in bit units.

Table 1. Pin Mask Options

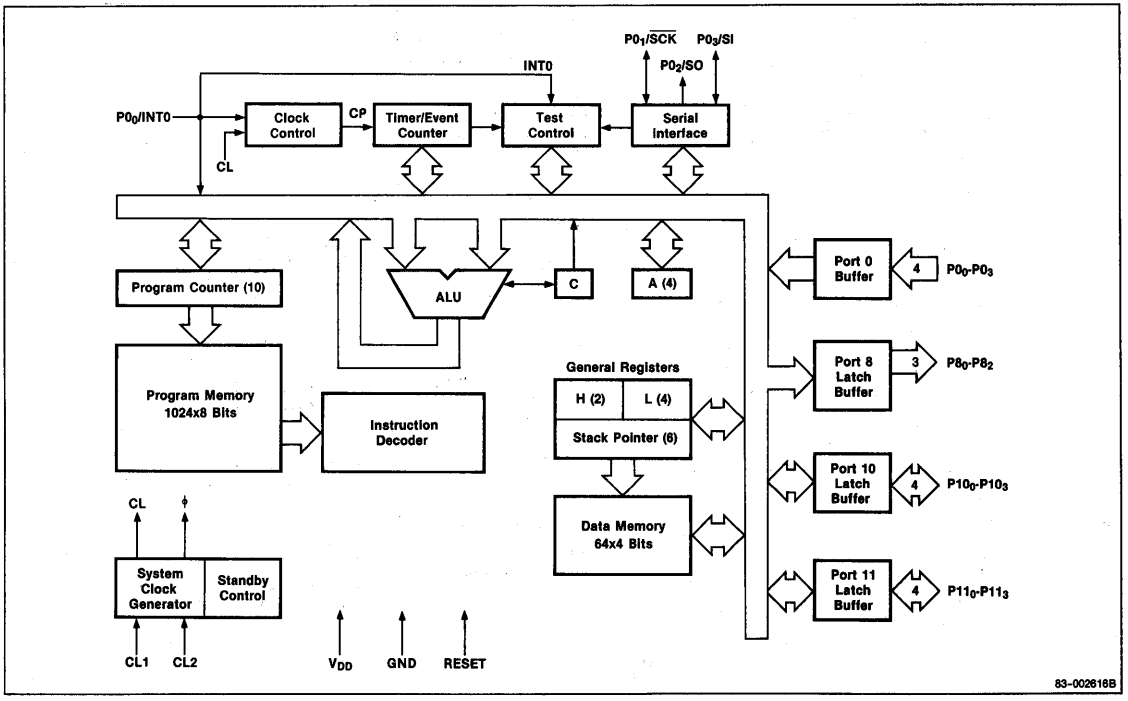
Pin	Options	
$P0_0$-$P0_3$	1 No connection to internal resistor 2 Connected to internal pull-up resistor 3 Connected to internal pull-down resistor	
$P8_0$-$P8_2$	1 CMOS (push-pull) output 2 N-channel open-drain output	
$P8_3$/CL2*	1 Use as $P8_3$ 2 Use as CL2	
	1 CMOS (push-pull) output 2 N-channel open-drain output	Used as $P8_3$
$P10_0$-$P10_3$ $P11_0$-$P11_3$	1 N-channel open-drain input/output 2 CMOS (push-pull) input/output 3 N-channel open-drain input/output with internal pull-up resistor.	
RESET	1 Connected to internal pull-down resistor 2 Not connected to internal pull-down resistor	

*: μPD7554 only

μPD7554 Block Diagram



μPD7564 Block Diagram



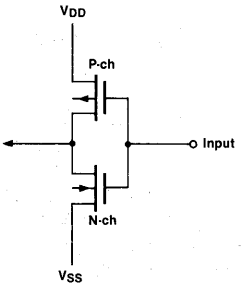
Functional Description

I/O Ports

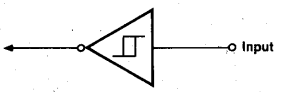
Figure 1 shows the internal circuits at I/O ports P0, P8, PI0, and P11

Figure 1. Interface at I/O Ports

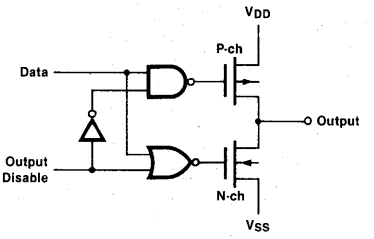
Type A. CMOS Input Cell
(Part of Type E)



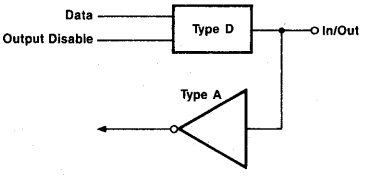
Type B. Schmitt-Triggered Input
P0$_0$/INT0, P0$_3$/SI



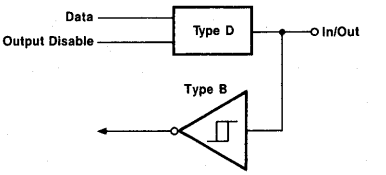
Type D. Push-Pull Output (part of types E and F)
High impedance on RESET (output disabled); both P- and N-channel transistors are turned off.



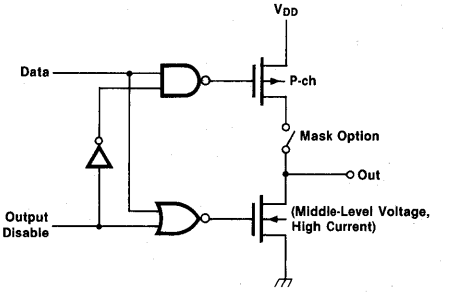
Type E. Type D Output with Type A Input Buffer
P0$_2$/SO



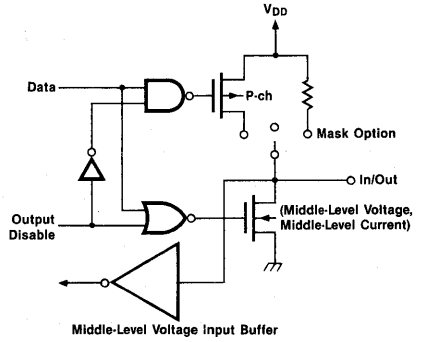
Type F. Type D Output with Type B Schmitt-Triggered input
P0$_1$/SCK



Type O. Mid-Level Voltage, High-Current
P8$_0$/P8$_2$, P8$_3$/CL$_2$



Type P. Mid-level Voltage Input Buffer
P10$_0$-P10$_3$, P11$_0$-P11$_3$



83-003557C

Program Memory

The μPD7554/7564 has a mask-programmable ROM with a capacity of 1024 words by 8 bits for program storage. It is addressed by the program counter. The reset start address is 000H. Figure 2 shows the program memory map.

General Purpose Registers

Two registers, H (2-bit) and L (4-bit) are provided as general purpose registers. Each register can be individually manipulated. The two registers also form pair register HL; H being the high register and L being the low one. The HL register is a data pointer to address data memory. Figure 3 shows the configuration of the general purpose registers.

The L register also specifies an I/O port or mode register when an I/O instruction (IPL or OPL) is executed. It also specifies the bits of a port when the SPBL or RPBL instruction is executed.

Figure 2. Program Memory Map

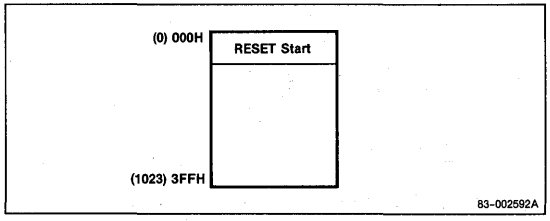
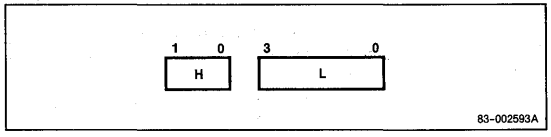


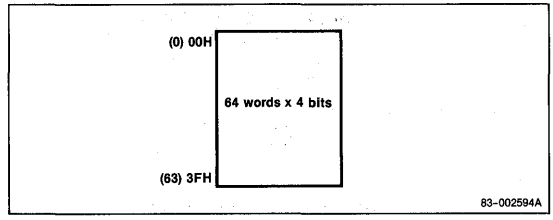
Figure 3. Configuration of General Purpose Registers



Data Memory

The data memory is static RAM with a capacity of 64 words by 4 bits. Part of this memory is used as the stack area. The data memory is also used in 8-bit data processing when paired with the accumulator. Figure 4 shows the data memory map.

Figure 4. Data Memory Map

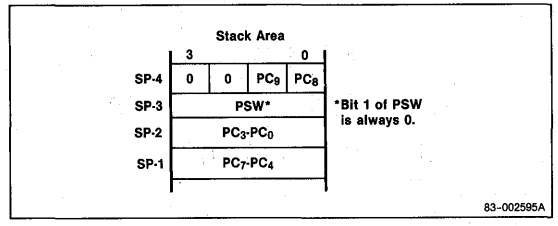


Data memory can be addressed directly, with the immediate data from an instruction; indirectly, with the contents of HL (including autoincrement and autodecrement); and indirectly by the contents of the stack pointer.

You may use any area of the data memory as the stack. The boundary of the stack is determined by how the TAMSP instruction initializes the stack pointer. Once the boundary is set, a call or return instruction automatically accesses the stack.

When a call instruction is executed, the contents of the program counter and the program status word (PSW) are stored to the stack in the sequence shown in figure 5.

Figure 5. Call Instruction Storage to Stack

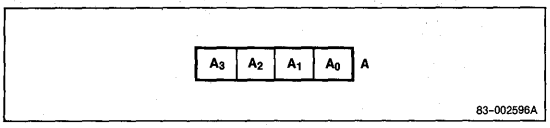


When a return instruction is executed, the contents of the program counter are automatically restored, but the PSW is not. The contents of data memory can be retained with a low supply voltage during STOP mode.

Accumulator

The accumulator is a 4-bit register used in arithmetic operations. The accumulator can process 8-bit data with paired data addressed by HL. Figure 6 shows the configuration of the accumulator.

Figure 6. Configuration of the Accumulator



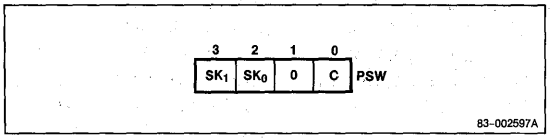
Arithmetic Logic Unit

The arithmetic logic unit (ALU) is a 4-bit arithmetic circuit that performs operations such as binary addition, logical operation, increment, decrement, comparison, and bit processing.

Program Status Word

The program status word (PSW) consists of two skip flags (SK0 and SK1), a carry flag (C), and bit 1, which is always zero. Figure 7 shows the configuration of the PSW.

Figure 7. Configuration of the Program Status Word



The contents of the PSW are stored to the stack when a call instruction is executed, but are not restored from the stack by the return instruction.

The skip flags retain the following skip conditions: string effect by LAI or LHLI instruction, and skip condition satisfied by an instruction other than a string-effect instruction. The skip flag is set or reset in accordance with the instruction executed.

The carry flag is set to 1 if an addition instruction (ACSC) generates a carry from bit 3 of the ALU. If no carry is generated, the flag is reset to zero. The SC instruction sets the carry flag and the RC instruction resets it.

When a RESET is input, the SK1 and SK0 flags are cleared to zero and the contents of the carry flag are undefined.

System Clock Generator

The system clock generator consists of a ceramic oscillator, a 1/2 frequency divider, standby modes (STOP/HALT), and control circuit. Figure 8 is a circuit diagram of the system clock generator.

In the μPD7554, the RC oscillator operates with a single external resistor connected across CL1 and CL2 (the capacitor C is incorporated). When the RC oscillator is not used, external clock pulses can be input via the CL1 pin. In this case, the RC oscillator functions as an inverting buffer. The output from the RC oscillator serves as the system clock (CL) which is then divided by two and used as the CPU clock (ϕ).

The standby mode control circuit is made up of a STOP flip-flop and a HALT flip-flop. The STOP instruction sets the STOP flip-flop and stops the system clock supply. This flip-flop also stops the RC oscillator. The STOP flip-flop is reset by the standby release signal that becomes active when one of the test requests flags is set or at the falling edge of the RESET signal. When the STOP flip-flop is reset, the RC oscillator resumes operation and supplies the system clock.

The HALT & STOP instruction & RESET HIGH sets the HALT flip-flop which disables signals from going to the 1/2 frequency divider that generates the CPU clock. Only the CPU clock stops in HALT mode. The HALT flip-flop is reset by the same conditions as the STOP flip-flop.

Figure 9 shows the system clock generator circuit for the μPD7564.

Figure 8. System Clock Generator for μPD7554

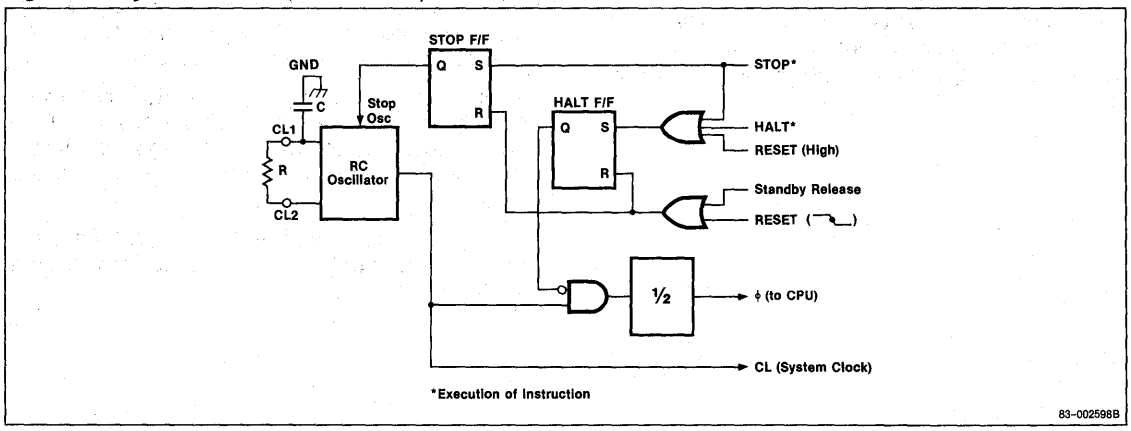
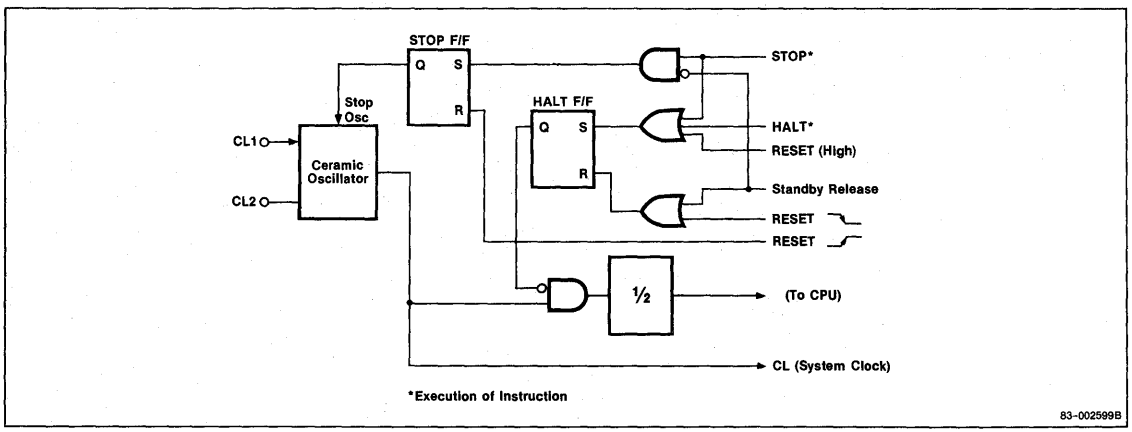


Figure 9. System Clock Generator for μPD7564



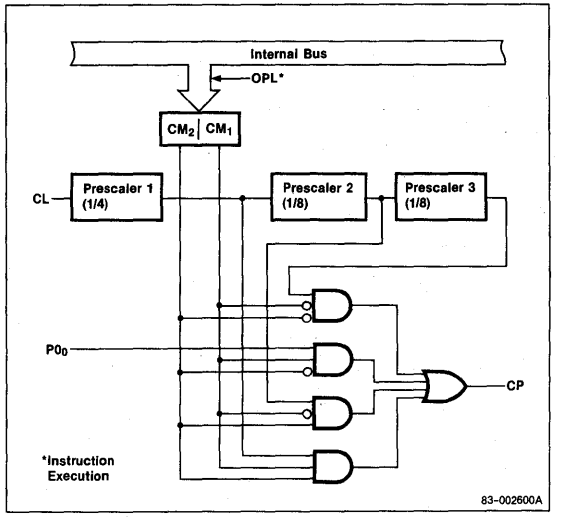
On the μPD7564, the ceramic oscillator operates with a ceramic resonator connected across CL1 and CL2. The output from the ceramic oscillator is used as the system clock (CL); it is divided by two to produce the CPU clock (ϕ).

The standby mode control circuit is made up of a STOP flip-flop and a HALT flip-flop. The STOP instruction sets the STOP flip-flop and stops the ceramic oscillation, thus stopping the supply for all clocks. The STOP flip-flop is reset by the RESET signal (high level) and restarts ceramic oscillation. The supply of each clock resumes when RESET goes low.

The HALT instruction sets the HALT flip-flop which disables signals from going to the 1/2 frequency divider that generates the CPU clock. Only the CPU clock stops in HALT mode. The HALT flip-flop is reset by the HALT RELEASE signal (activated by setting at least one test request flag) or the falling edge of RESET, resuming supply of the CPU clock.

The HALT flip-flop is also set when RESET is active (high level). At power on reset operation, the rising edge of RESET starts ceramic oscillation; however, some time is required to achieve stable oscillation. To prevent the unstable clock from operating the CPU, the HALT flip-flop is set and the CPU clock is stopped while RESET is high. Accordingly, the high-level width of RESET must be more than the required stable time for the ceramic resonator.

Figure 10. Clock Control Circuit



Clock Control Circuit

The clock control circuit consists of a 2-bit clock mode register (bits CM1 and CM2), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and event pulses ($P0_0$). It also selects the clock source and prescaler according to the setting in the clock mode register and supplies the timer/event counter with count pulses. Figure 10 shows the clock control circuit.

Table 2 lists the codes set in the clock mode register by the OPL instruction to specify the count pulse frequency.

When you set the clock mode register with the OPL instruction, clear bit 0 of the accumulator (corresponding to bit CM0 of the EVAKIT-7500 or μPD7500H during emulation).

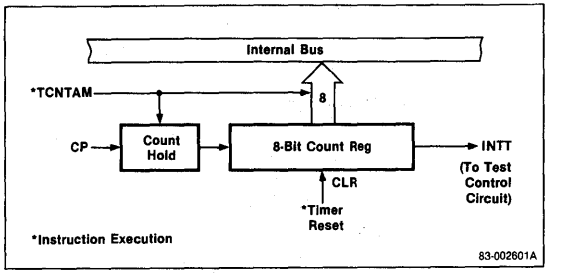
Timer/Event Counter

The timer/event counter is a binary 8-bit up-counter which is incremented each time a count pulse is input. The TIMER instruction or a RESET signal clears it to 00H. When an overflow occurs, the counter is reset from FFH to 00H. Figure 11 shows the inputs and outputs of the counter.

Table 2. Selecting the Count Pulse Frequency

CM2	CM1	Frequency Selected
0	0	CL/256
0	1	$P0_0$
1	0	CL/32
1	1	CL/4

Figure 11. Timer/Event Counter



Serial Interface

The serial interface consists of an 8-bit shift register, a 3-bit shift mode register, and a 3-bit counter. This interface inputs and outputs serial data. Figure 12 is a block diagram of the interface.

Test Control Circuit

The μPD7564 has three test sources, as shown in table 3.

The test control circuit consists of two test request flags (INT T RQF and INT0/S RQF) set by the three test sources, and a test request flag control circuit that checks the contents of each test request flag by executing an SKI instruction and resetting the flags.

Test sources INT0 and INTS share the request flag INT0/S RQF. Bit 3 of the shift mode register (SM_3) determines which source is selected. A zero in SM_3 selects INTS and a one selects INT0.

Table 3. μPD7564 Test Sources

Source	Function	Location	Request Flag
INTT	Overflow in timer/event counter	internal	INTT RQF
INT0	Test request signal from $P0_0$ pin	external	INT0/S RQF
INTS	Transfer complete signal from serial interface	internal	INT0/S RQF

The request flag INTT RQF is set when a timer overflow occurs in the timer event counter. The SKI or TIMER instruction resets it.

When SM_3 is zero, request flag INT0/S RQF is set when the INTS signal is generated, indicating the end of an 8-bit serial data transfer. The SKI or SIO instruction resets the flag.

When SM_3 is one, request flag INT0/S RQF is set at the rising edge of the signal input to the $P0_0$/INT0 pin. The SKI instruction resets the flag.

The logical sum of the outputs from the test request flags releases standby mode (STOP* or HALT mode). The mode is released when one or both flags are set. Both flags and SM_3 are reset when the RESET signal is input. After reset, source INTS is selected and signal input to the INT0 pin is inhibited as the initial condition.

Figure 13 is a block diagram of the test control circuit.

*only μPD7554

Figure 12. Serial Interface Block Diagram

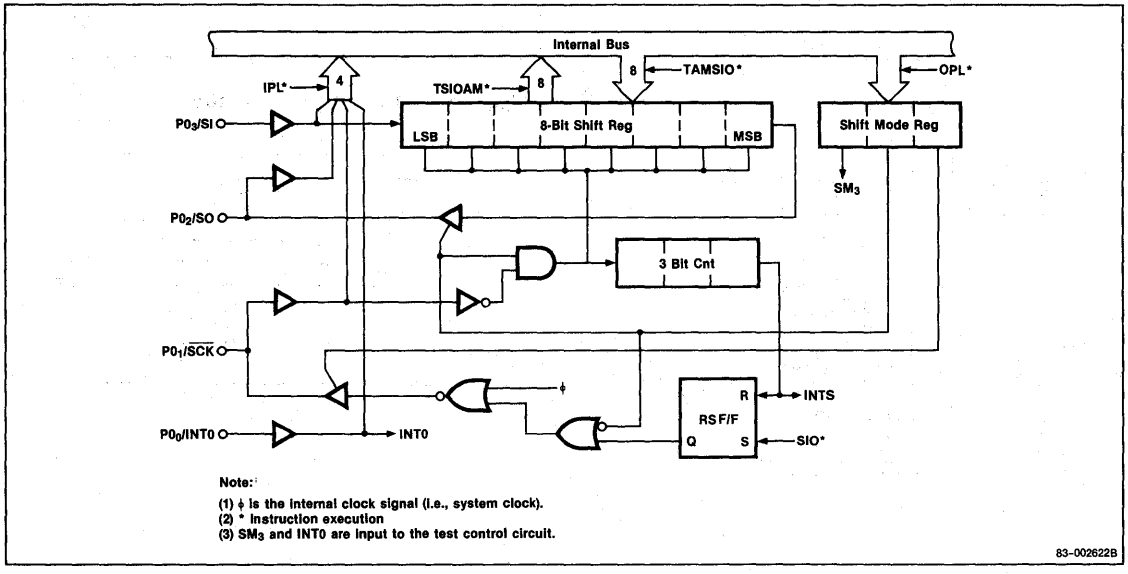
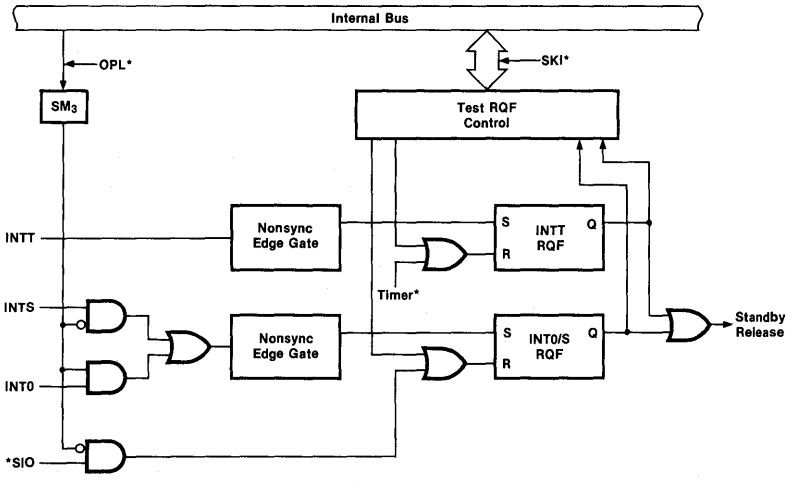


Figure 13. Test Control Circuit Block Diagram



Standby Modes

The μPD7554/64 has two standby modes to reduce power consumption while the program is in the wait state. The STOP and HALT instructions set these modes.

When the program enters a standby mode, program execution stops and the contents of all registers and data memory immediately before the program entered standby mode are retained. The timer and serial interface can operate.

The RESET signal and STANDBY Release Signal *1 releases STOP mode. HALT mode is released when one or both of the test request flags are set, or when the RESET signal is input. The program cannot enter a standby mode when a test request is being set, even if the STOP or HALT command is executed.

If there is some uncertainty as to the state of the test request flags, execute the SKI instruction to reset them so the program can enter standby mode.

Table 4 compares STOP and HALT modes. The main difference is that STOP mode stops the system clock and HALT does not. Ceramic oscillation stops during STOP mode. The power consumed by the ceramic oscillator is the difference between the two modes. In STOP mode, data memory can be retained with a lower supply voltage.

*1 standby release signal only for μPD7554

Table 4. STOP and HALT Modes

Mode	CL	φ	PO_0	CPU	Timer	Released by
STOP	x	x	0	x	△	RESET input
HALT	0	x	0	x	0	INTT RQF INT0/S RQF RESET input

Note:

(1) o: operates x: stops △: will operate depending on clock source

μPD7554, if external clock is used STOP instruction will not STOP CL. In this case STOP mode acts as HALT mode.

Power-on Reset Circuit

Figure 14 shows a circuit example of the power-on reset circuit using a resistor and a capacitor. This is the simplest reset control circuit. Figure 21 shows the circuit with a pull-down resistor internally connected to RESET as a mask option.

μPD7554/7564 Applications

Figures 16 and 17 show examples of application circuits for the μPD7554/7564.

Table 5 compares the features of products in this part of the 7500 series devices.

Figure 14. Power-on Reset Circuit

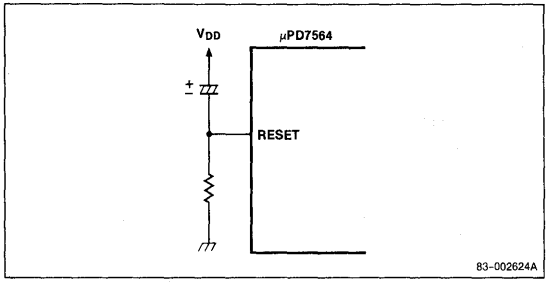


Figure 15. Power-on Reset Circuit with Pull-down Resistor

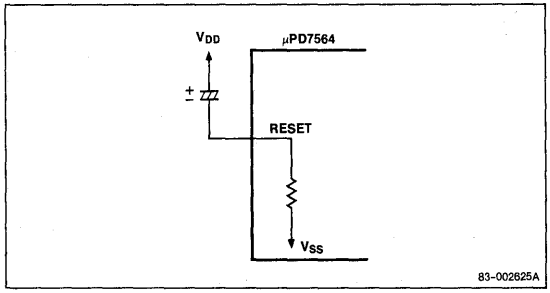


Table 5. Product Comparison

Item		μPD7554	μPD7564	μPD7556	μPD7566
Instruction cycle/system clock (5 V)	RC	4 μs/ 500 kHz		4 μs/ 500 kHz	
	External	2.86 μs/ 700 kHz		2.86 μs/ 700 kHz	
	Ceramic		3 μs/ 660 kHz		3 μs/ 660 kHz
Instruction set		47	47	45	45
ROM		1024x8	1024x8	1024x8	1024x8
RAM		64x4	64x4	64x4	64x4
I/O port total		16 (max)	15	20 (max)	19
Port 0		$P0_0$-$P0_3$	$P0_0$-$P0_3$	$P0_0$-$P0_1$	$P0_0$-$P0_1$
Port 1				$P1_0$-$P1_3$	$P0_1$-$P0_3$
Port 8		$P8_0$-$P8_2$ $P8_2$/CL2	$P8_0$-$P8_2$	$P8_0$-$P8_2$ $P8_3$/CL2	$P8_0$-$P8_2$
Port 9				$P9_0$-$P9_1$	$P9_0$-$P9_1$
Port 10		$P10_0$- $P10_3$	$P10_0$- $P10_3$	$P10_0$- $P10_3$	$P10_0$- $P10_3$
Port 11		$P11_0$- $P11_3$	$P11_0$- $P11_3$	$P11_0$- $P11_3$	$P11_0$- $P11_3$
Timer/Event counter		8-bit	8-bit	8-bit	8-bit
Serial interface		8-bit	8-bit		
Comparator				4-channel	4-channel
Process		CMOS	CMOS	CMOS	CMOS
Package		20-pin plastic shrink DIP	20-pin plastic shrink DIP	24-pin plastic shrink DIP	24-pin plastic shrink DIP

Figure 16. Tape Counter Circuit

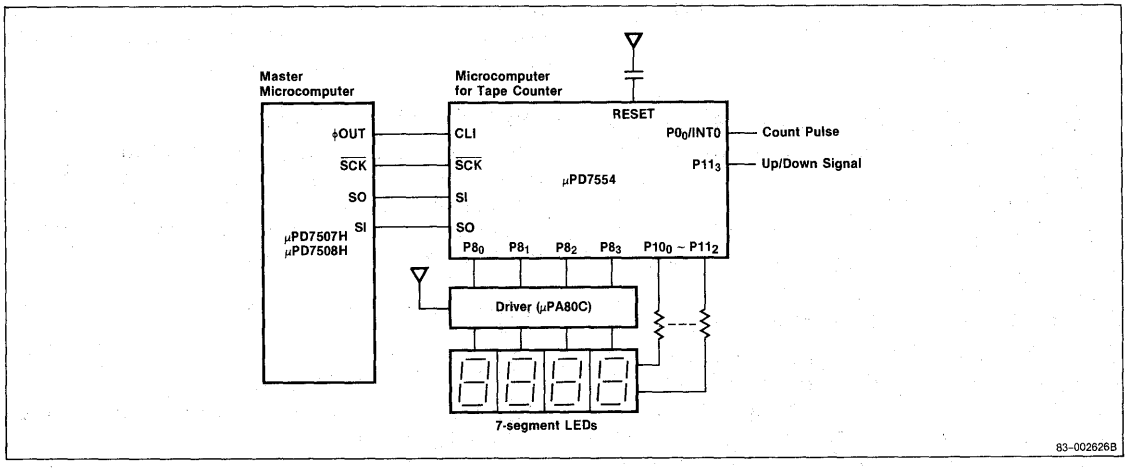
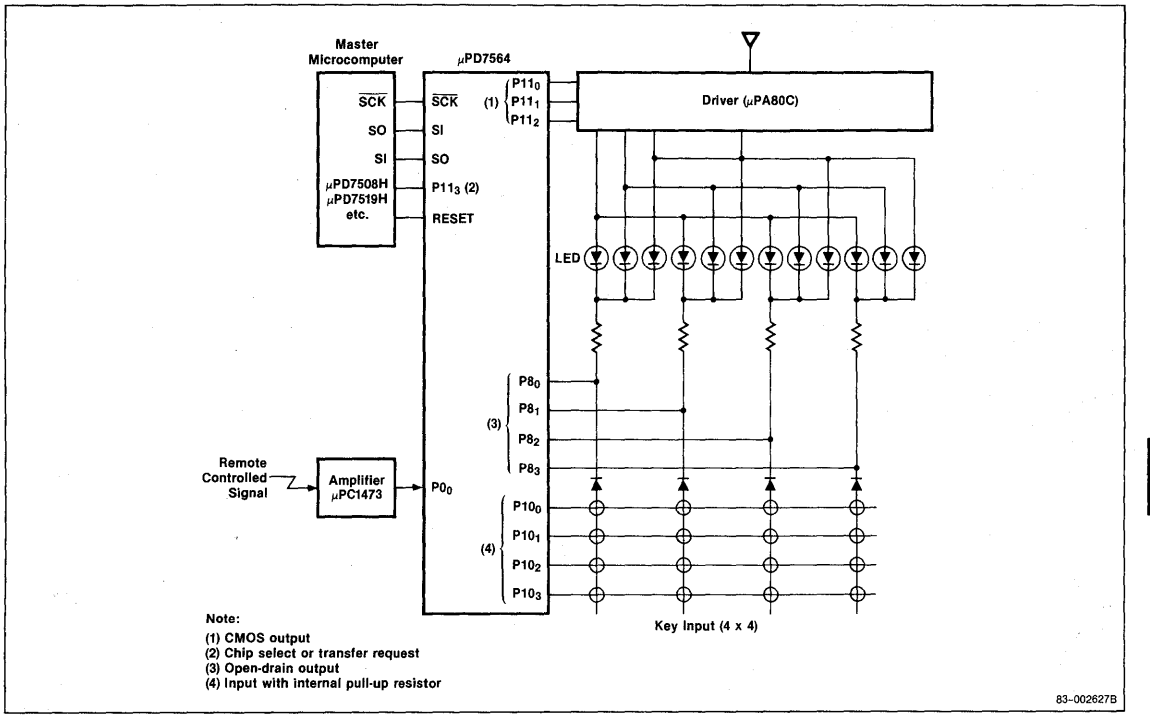


Figure 17. Remote-controlled Data Reception, Key Input and LED Display.



Absolute Maximum Ratings

T_A = 25°C

Operating temperature, T_{OPT}			−10°C to +70°C
Storage temperature, T_{STG}			−65°C to +150°C
Power supply voltage, V_{DD}			−0.3 V to +7.0 V
Input Voltage VI	Except Port 10 & 11		−0.3 V to V_{DD} + 0.3 V
	Port 10 & 11	(1)	−0.3 to V_{DD} + 0.3 V
		(2)	−0.3 to + 13 V
Output Voltage V_O	Except Port 8, 10 & 11		−0.3 to V_{DD} + 0.3 V
	Ports 8, 10, 11	(1)	−0.3 to V_{DD} + 0.3 V
		(2)	− 0.3 to +13 V
Output current high, one port I_{OH}			−5 mA
all output ports, total I_{OH}			−15 mA
Output current low $P0_1$, $P0_2$	I_{OL}		5 mA
Ports 9, 10, 11	I_{OL}		15 mA
Ports 8,	I_{OL}		30 mA
All ports, total			100 mA
Power dissipation, P_D			480 mW (T_A = 70°C)

Comment: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) CMOS I/O or N-channel open drain + internal pull up resistor

(2) N-channel open drain I/O

Capacitance

T_A = 25°C, V_{DD} = GND = 0 V; f = 1 MHz,
Unmeasured pins returned to GND

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	$P0_0$, $P0_3$
Output capacitance	C_O			35	pF	Port 8
I/O capacitance	C_{IO}			35	pF	Ports 10, 11,
I/O capacitance	C_{IO}			15	pF	$P0_1$, $P0_2$

DC Characteristics

μPD7554 only: T_A = −10°C to +70°C, V_{DD} = 2.5 V to 3.3 V, GND = 0 V
μPD7554/64: T_A = −10°C to +70°C, V_{DD} = 2.7 V to 6.0 V, GND = 0 V

Parameter	Symbol	(V_{DD} = 2.5–3.3) 7554 only Limits			(V_{DD} = 2.7 to 6.0 V) 7554/64 Limits			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Input high voltage except CL1	V_{IH1}	0.8 V_{DD}		V_{DD}	0.7 V_{DD}		V_{DD}	V	
Input high voltage CL1 (2)	V_{IH2}	V_{DD}-0.3		V_{DD}	V_{DD}-0.5		V_{DD}	V	
Input high voltage ports 10, 11	V_{IH3}	0.8 V_{DD}		12 (1)	0.7 V_{DD}		12 (1)	V	
Input high voltage RESET	V_{IHDR}	0.9 V_{DDDR}		V_{DDDR} +0.2	0.9 V_{DDDR}		V_{DDDR} +0.2	V	Data retention mode
Input low voltage except CL1	V_{IL1}	0		0.2 V_{DD}	0		0.3 V_{DD}	V	Includes CLI for 7564
Input low voltage CL1 (2)	V_{IL2}	0		0.3	0		0.5	V	
Input leakage current except CL1 Input leakage current CL1	I_{LI1} I_{LI1}	−3		3	−3		3	μA	0 V ≤ V_I ≤ V_{DD} Includes CLI for 7564
Input leakage current CL1 (2)	I_{LI2}	−10		10	−10		10	μA	0 V ≤ V_I ≤ V_{DD}
Input leakage current ports 10, 11	I_{LI3}			10 (1)			10 (1)	μA	V_I = 12 V
Output voltage high PO_1, PO_2, ports 8–11	V_{OH}	V_{DD}-1.0						V	I_{OH} = −80 μA
Output voltage high PO_1, PO_2, ports 8–11	V_{OH}				V_{DD}-2.0			V	V_{DD} = 4.5 V to 6.0 V, I_{OH} = 1 mA
Output voltage high PO_1, PO_2, ports 8–11	V_{OH}				V_{DD}-1.0			V	V_{DD} = 2.7 V I_{OH} = −100 μA
Output voltage low PO_1, PO_2, ports 10, 11	V_{OL}			0.5				V	I_{OL} = 350 μA
Output voltage low PO_1, PO_2	V_{OL}						0.4	V	V_{DD} = 4.5 V to 6.0 V, I_{OL} = 1.6 mA
Output voltage low PO_1, PO_2	V_{OL}						0.5	V	I_{OL} = 400 μA
Output voltage low ports 10, 11	V_{OL}						0.4	V	V_{DD} = 4.5 V to 6.0 V, I_{OL} = 1.6 mA
Output voltage low ports 10, 11	V_{OL}						2.0	V	V_{DD} = 4.5 V to 6.0 V, I_{OL} = 10 mA
Output voltage low ports 10, 11	V_{OL}						0.5	V	V_{DD} = 2.7 V, I_{OL} = 400 μA
Output voltage low port 8	V_{OL}			0.5				V	I_{OL} = 500 μA
Output voltage low port 8	V_{OL}						2.0	V	V_{DD} = 4.5 V to 6.0 V, I_{OL} = 15 mA
Output voltage low port 8	V_{OL}						0.5	V	V_{DD} = 2.7 V I_{OL} = 600 μA
Output leakage current	I_{LO1}	−3		3	−3		3	μA	0 V ≤ V0 ≤ V_{DD}
Output leakage current ports 8–11	I_{LO2}			10 (1)			10 (1)	μA	V_O = 12 V
Supply voltage, data retention mode	V_{DDDR}	2.0			2.0			V	
Supply current, normal operation	I_{DD1}		55	180				μA	V_{DD} = 3 V ± 0.3 V R = 150 kΩ ± 2%
R oscillation	I_{DD1}		40	150				μA	V_{DD} = 2.5 V R = 150 kΩ ± 2%
Supply current, normal operation, ceramic oscillation	I_{DD1}					650	2200	μA	V_{DD} = 5 V + 0.5 V f_{CC} = 700 kHz
Supply current, normal operation, ceramic oscillation	I_{DD1}					120	360	μA	V_{DD} = 3 V ± 10% f_{CC} = 300 kHz

DC Characteristics (cont)

μPD7554 only: T_A = −10°C to +70°C, V_{DD} = 2.5 V to 3.3 V, GND = 0 V
μPD7554/64: T_A = −10°C to +70°C, V_{DD} = 2.7 V to 6.0 V, GND = 0 V

		(V_{DD} = 2.5–3.3) 7554 only Limits			(V_{DD} = 2.7 to 6.0 V) 7554/64 Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Supply current, normal operation, R oscillation	I_{DD1}					270	900	μA	V_{DD} = 5 V ± 0.5 V R = 56 kΩ = 2%
Supply current, normal operation, R oscillation	I_{DD1}					80	240	μA	V_{DD} = 3 V ± 10% R = 100 kΩ ± 2%
Supply current, HALT mode, R osc.	I_{DD2}		25	180				μA	V_{DD} = 3 V ± 0.3 V R = 150 kΩ ± 2%
	I_{DD2}		18	60				μA	V_{DD} = 2.5 V R = 150 kΩ ± 2%
Supply current, HALT mode, ceramic osc.	I_{DD2}					450	1500	μA	V_{DD} = 5 V ± 0.5 V f_{CC} = 700 kHz
Supply current, HALT mode, ceramic osc.	I_{DD2}					65	200	μA	V_{DD} = 3.0 V ± 10% f_{CC} = 300 kHz
Supply current, HALT mode, R osc.	I_{DD2}					120	400	μA	V_{DD} = 5 V ± 0.5 V R = 56 kΩ ± 2%
Supply current, HALT mode, R osc.	I_{DD2}					35	110	μA	V_{DD} = 3 V ± 10% R = 100 kΩ ± 2%
Supply current, STOP mode	I_{DD3}		0.1	5				μA	
Supply current, STOP mode	I_{DD3}					0.1	10	μA	V_{DD} = 5 V ± 0.5 V
Supply current, STOP mode	I_{DD3}					0.1	5	μA	V_{DD} = 3 V ± 10%
Supply current, data retention mode	I_{DDDR}		0.1	5		0.1	5	μA	V_{DDDR} = 2.0 V
Pull-up/down resistance, Port 0, RESET	RP1	23.5	47	70.5	23.5	47	70.5	kΩ	
Pull-up resistance Ports 8–11	RP2	7.5	15	22.5	7.5	15	22.5	kΩ	

Note:

(1) N-channel open drain I/O ports.
(2) μPD7554 only

AC Characteristics

μPD7554 only: T_A = −10°C to +70°C, V_{DD} = 2.5 V to 3.3 V, GND = 0 V
μPD7554/64: T_A = −10°C to +70°C, V_{DD} = 2.7 V to 6.0 V, GND = 0 V

		(V_{DD} = 2.5–3.3) 7554 only Limits			(V_{DD} = 2.7 to 6.0 V) 7554/64 Limits				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
System clock osc. frequency (1)	f_{CC}	140	180	220				kHz	R = 150 kΩ ± 2%
System clock osc. frequency (1)	f_{CC}				400	500	600	kHz	V_{DD} = 4.5 V to 6.0 V; R = 56 kΩ ± 2%
System clock osc. frequency (1)	f_{CC}				200	350	300	kHz	V_{DD} = 3 V ± 10%; R = 100 kΩ ± 2%
System clock osc. frequency, CL1, CL2	f_{CC}	140	175	240				kHz	V_{DD} = 2.5 V R = 150 kΩ ± 2%; 50% duty
External clock frequency, CL1	f_C	10		250				kHz	
External clock frequency, CL1	f_C				10		710	kHz	V_{DD} = 4.5 V to 6.0 V; 50% duty
External clock frequency, CL1	f_C				10		350	kHz	V_{DD} = 2.7 V; 50% duty

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AC Characteristics (cont)

μPD7554 only: T_A = −10°C to +70°C, V_{DD} = 2.5 V to 3.3 V, GND = 0 V
μPD7554/64: T_A = −10°C to +70°C, V_{DD} = 2.7 V to 6.0 V, GND = 0 V

Parameter	Symbol	(V_{DD} = 2.5–3.3) 7554 only Limits			(V_{DD} = 2.7 to 6.0 V) 7554/64 Limits			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
System clock osc. frequency (2)	f_{CC}	290	700	710				kHz	V_{DD} = 4.5 to 6.0 V
		290	500	510				kHz	V_{DD} = 4.0 to 6.0 V
		290	400	410				kHz	V_{DD} = 3.5 to 6.0 V
		290	300	310				kHz	V_{DD} = 2.7 to 6.0 V
Oscillation stabilization time (2)	t_{OS}	20						μs	V_{DD} = 2.7 to 6.0 V
System clock rise time, CL1	t_{CR}			200			200	ns	
System clock fall time, CL1	t_{CF}			200			200	ns	
System clock pulse width	t_{CH}	2		50				μs	
System clock pulse width	t_{CH}				0.7		50	μs	
System clock pulse width	t_{CL}	2		50					
System clock pulse width, CL1	t_{CL}				1.45		50	μs	V_{DD} = 2.7 V
External clock frequency ($P0_0$)	f_{P00}	0		250				kHz	50% duty
External clock frequency ($P0_0$)	f_{P00}				0		710	kHz	V_{DD} = 4.5 V to 6.0 V; 50% duty
External clock frequency ($P0_0$)	f_{P00}				0		350	kHz	V_{DD} = 2.7 V 50% duty
$P0_0$ rise time	t_{CRP00}			200			200	ns	
$P0_0$ fall time	t_{CFP0}			200			200	ns	
$P0_0$ pulse width	t_{P00H}	2						μs	
$P0_0$ pulse width	t_{P00H}				0.7			μs	V_{DD} = 4.5 V to 6.0 V
$P0_0$ pulse width	t_{P00L}	2						μs	
$P0_0$ pulse width	t_{P00L}				1.45			μs	V_{DD} = 2.7 V
INT0 high time	t_{IOH}	30			10			μs	
INT0 low time	t_{IOL}	30			10			μs	
RESET high time	t_{RSH}	30			10			μs	
RESET low time	t_{RSL}	30			10			μs	
RESET setup time	t_{SRS}	0			0			μs	
RESET hold time	t_{HRS}	0			0			μs	
$\overline{SCK}$ cycle time	t_{KCY}	8.0						μs	Input
$\overline{SCK}$ cycle time	t_{KCY}	10.0						μs	Output
$\overline{SCK}$ cycle time	t_{KCY}				2.0			μs	Input; V_{DD} = 4.5 V to 6.0 V
$\overline{SCK}$ cycle time	t_{KCY}				2.5			μs	Output; V_{DD} = 4.5 V to 6.0 V
$\overline{SCK}$ cycle time	t_{KCY}				5.0			μs	Input; V_{DD} = 2.7 V
$\overline{SCK}$ cycle time	t_{KCY}				5.7			μs	Output; V_{DD} = 2.7 V
$\overline{SCK}$ pulse width	t_{KH}	4.0						μs	Input
$\overline{SCK}$ pulse width	t_{KH}				1.0			μs	Input; V_{DD} = 4.5 V to 6.0 V
$\overline{SCK}$ pulse width	t_{KH}				1.25			μs	Output; V_{DD} = 4.5 V to 6.0 V
$\overline{SCK}$ pulse width	t_{KL}	5.0						μs	Output
$\overline{SCK}$ pulse width	t_{KL}				2.5			μs	Input; V_{DD} = 2.7 V

AC Characteristics (cont)

μPD7554 only: T_A = −10°C to +70°C, V_{DD} = 2.5 V to 3.3 V, GND = 0 V
μPD7554/64: T_A = −10°C to +70°C, V_{DD} = 2.7 V to 6.0 V, GND = 0 V

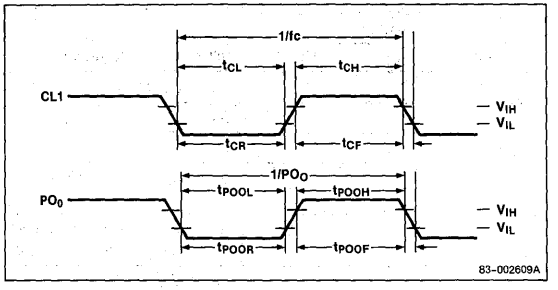
Parameter	Symbol	(V_{DD} = 2.5–3.3) 7554 only Limits			(V_{DD} = 2.7 to 6.0 V) 7554/64 Limits			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
$\overline{SCK}$ pulse width	t_{KL}				2.85			μs	Output; V_{DD} = 2.7 V
SI setup time to $\overline{SCK}$↑	t_{SIK}	0.3			0.1			μs	
SI hold time after $\overline{SCK}$↑	t_{KSI}	0.3			0.1			μs	
SO output delay time after $\overline{SCK}$↑	t_{KSO}			2.0				μs	C_{OUT} = 100 pF max.
SO output delay time after $\overline{SCK}$↑	t_{KSO}						0.85	μs	V_{DD} = 4.5 V to 6.0 V; C_{OUT} = 100 pF max.
SO output delay time after $\overline{SCK}$↑	t_{KSO}						1.2	μs	V_{DD} = 2.7 V; C_{OUT} = 100 pF max.

(1) μPD7554 only
(2) μPD7564 only

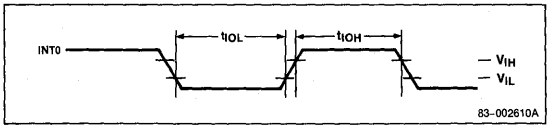
3

Timing Waveforms

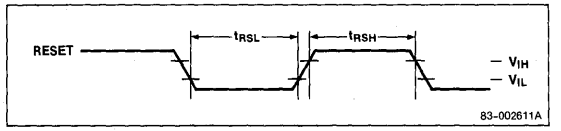
Clocks



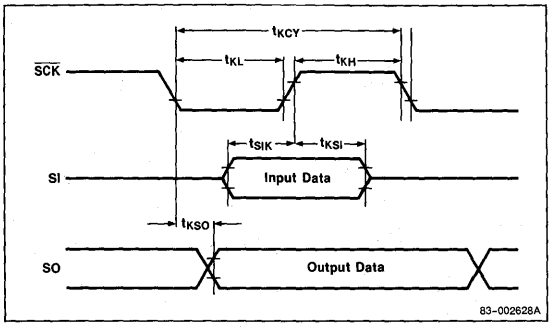
External Interrupt



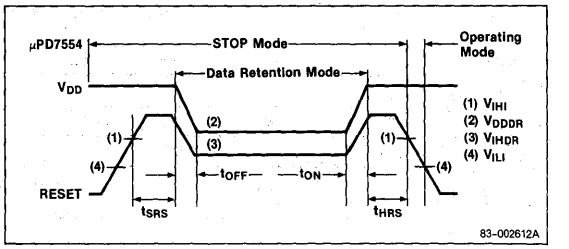
Reset



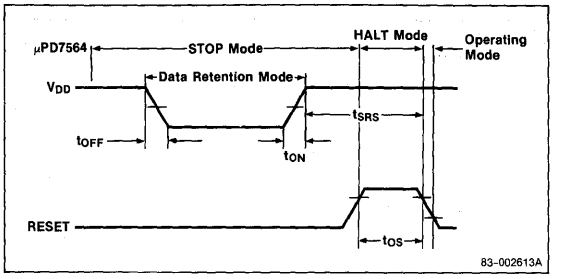
Serial Interface



Data Retention Mode μPD7554



Data Retention Mode μPD7564



NEC
NEC Electronics Inc.

μPD7556/66
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS WITH COMPARATOR

Description

The μPD7556 and μPD7566 are low-end versions of μPD7500 series products. These microcomputers incorporate a 4-bit comparator input and are useful as slave CPUs to high-end μPD7500 series or 8-bit μCOM-87 series products.

The μPD7556/66 has output ports that can directly drive triacs and LEDs. Also, various mask-optional I/O circuits can be configured for a wide selection of outputs allowing a reduction of external circuitry in your design. There are two testable interrupts.

The μPD7556 and μPD7566 differ only in their clock circuitry. The μPD7556 uses an external resistor with an internal capacitor for an RC oscillator clock, where the μPD7566 uses a ceramic oscillator as a clock. These microcomputers are ideally suited to control devices such as air conditioners, microwave ovens, refrigerators, rice cookers, and audio equipment.

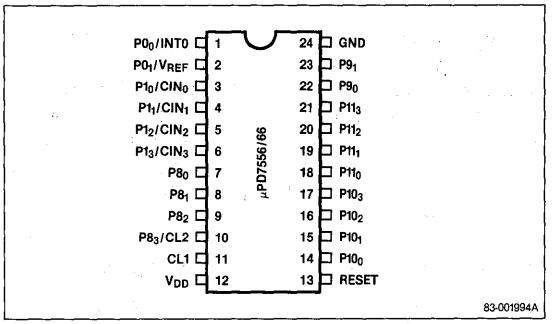
Features

- ☐ 45 instructions (subset of μPD7500 set B)
- ☐ Instruction cycle:
  - — External clock: 2.86 μs/700 kHz, 5 V
  - — RC oscillator (μPD7556): 4 μs/500 kHz, 5 V
  - — Ceramic oscillator (μPD7566): 3 μs/660 kHz, 5 V
- ☐ Program memory (ROM) of 1024 × 8 bits
- ☐ Data memory (RAM) of 64 × 4 bits
- ☐ 8-bit timer/event counter
- ☐ I/O lines:
  - — μPD7556: 20
  - — μPD7566: 19
- ☐ Data memory retention at low supply voltage
- ☐ Standby (STOP/HALT) functions
- ☐ CMOS technology
- ☐ Low power consumption
- ☐ Single power supply (2.5 V to 6.0 V μPD7556)
  (2.7 V to 6.0 V μPD7566)

Ordering Information

Part Number	Package Type
μPD7556CS	24-pin plastic shrink DIP
μPD7566CS	24-pin plastic shrink DIP
μPD7556G	24-pin plastic SO
μPD7566G	24-pin plastic SO

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 2	$P0_0$ / INT_0 $P0_1$ / V_{REF}	2-bit input port 0 / testable input pin / comparator reference voltage input pin
3–6	$P1_0$ / CIN_0 $P1_1$ / CIN_1 $P1_2$ / CIN_2 $P1_3$ / CIN_3	4-bit input port 1 / 4-bit comparator inputs
7–9, 10	$P8_0$–$P8_2$, $P8_3$ / CL2	3-bit output port 8 (7566), 3- (4-) bit output port 8 / connection for RC oscillator (7556) / Ceramic resonator (7566)
11	CL1	Connection for ceramic resonator / RC oscillator
12	V_{DD}	+5 V power supply
13	RESET	Reset input pin
14–17	$P10_1$–$P10_3$	4-bit I / O port 10
18–21	$P11_0$–$P11_3$	4-bit I / O port 11
22–23	$P9_0$–$P9_1$	2-bit output port 9
24	GND	Ground

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Pin Functions

$P0_0$/INT0, $P0_1$/V_{REF} (Port 0/count clock input/comparator reference voltage input)

2-bit input port 0/count clock input/comparator reference voltage input. INT0 is an edge-sensitive testable input pin that detects a signal at the rising edge. V_{REF} is the comparator reference voltage input pin. A mask option specifies whether this pin is used as $P0_1$ or V_{REF}. $P0_0$/INT0 is unused; connect it to ground. If $P0_1$/V_{REF} is unused, connect it to ground or V_{DD}. The port is in the input state at reset.

$P1_0$/CIN_0-$P1_3$/CIN_3 (Port 1/comparator inputs)

4-bit input port 1/comparator inputs. A mask option specifies whether these pins are used as digital inputs (Port 1) or as comparator inputs (CIN_0-CIN_3). If any of $P1_0$-$P1_3$ pins are unused, connect them to ground or V_{DD}. The port is in the input state at reset.

$P8_0$-$P8_2$, $P8_3$/CL2 (Port 8/clock input 2)

4-bit output port 8. This port sinks 15 mA and can interface to 12 V. On the μPD7556, the port function of $P8_3$/CL2 is specified by mask option. $P8_3$ is a normal output port on the μPD7556. On the μPD7556, CL2 is one of the pins to which a resistor for RC oscillation is connected. On the μPD7566, CL2 is one of the pins to which a ceramic resonator is connected. If any of $P8_0$-$P8_2$ pins are unused, leave them open. The port is in the high impedance state at reset.

CL1 (Clock input 1)

On the μPD7556, CL1 is one of the two pins to which a resistor for RC oscillation is connected. On the μPD7566, CL1 is one of the two pins to which a ceramic resonator is connected.

V_{DD} (Power supply)

Positive power supply.

RESET (Reset)

System reset input pin (active high). This pin can be internally connected to a pull-down resistor if specified by mask option.

$P10_0$-$P10_3$ (Port 10)

4-bit I/O port. This port sinks 10 mA and can interface to 12 V. If any of these pins are unused, connect them to ground or V_{DD} in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset.

$P11_0$-$P11_3$ (Port 11)

4-bit I/O port. This port sinks 10 mA and can interface to 12 V. If any of these pins are unused, connect them to ground or V_{DD} in the input state, or leave open in the output state. The port is in the high impedance or high-level output state at reset.

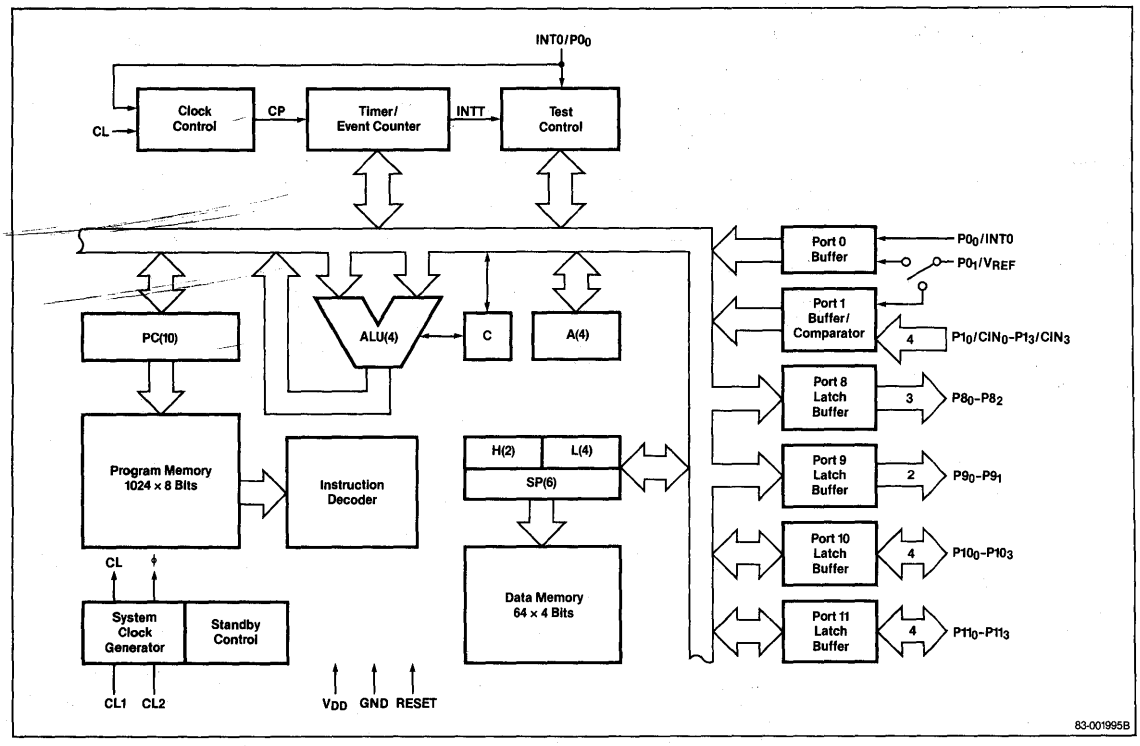
$P9_0$-$P9_1$ (Port 9)

2-bit output port. This port sinks 15 mA and can interface to 12 V. If either of these pins is unused, leave it open. The port is in the high impedance state at reset.

GND (Ground)

Ground.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, ports other than 10 & 11, V_I	−0.3 V to V_{DD} +0.3 V
Input voltage, ports 10, 11, V_I (1)	−0.3 V to V_{DD} +0.3 V
Input voltage, ports 10, 11, V_I (2)	−0.3 V to V_{DD} +13 V
Output voltage, ports other than 8, 10 & 11, V_O	−0.3 V to V_{DD} +0.3 V
Output voltage, ports 8, 10, 11, V_O (1)	−0.3 V to V_{DD} +0.3 V
Output voltage, ports 8, 10, 11, V_O (2)	−0.3 V to V_{DD} +13 V
Output current high, one pin, I_{OH}	−5 mA
Output current high, all output ports total, I_{OH}	−15 mA
Output current low, ports 10, 11, I_{OL}	15 mA
Output current low, ports 8, 9, I_{OL}	30 mA
Output current low, all ports total, I_{OL}	100 mA
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Power dissipation, P_D	480 mW (T_A = 70°C)

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
(1) CMOS push pull or N-channel open drain + pull up resistor I/O
(2) N-channel open drain I/O

Capacitance

$T_A = 25°C$, $V_{DD} = GND = 0$ V, f = 1.0 MHz, Unmeasured pins returned to GND

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}			15	pF	$P0_0$–$P0_1$; $P1_0$–$P1_3$, CIN_0–CIN_3
Output capacitance	C_{OUT}			35	pF	Ports 8, 9
I/O capacitance	$C_{I/O}$			35	pF	Ports 10, 11

3

DC Characteristics

μPD7556: $T_A = -10°C$ to $+70°C$, $V_{DD} = +2.5$ V to 3.3 V, GND = 0 V
μPD7556/μPD7566: $T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V, GND = 0 V

		Limits							
		$T_A = 10°C$ to $+70°C$, $V_{DD} = +2.5$ V to 3.3 V μPD7556			$T_A = 10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V μPD7566/μPD7556				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Input voltage low	V_{IL1}	0		$0.2V_{DD}$	0		$0.3V_{DD}$	V	Except CL1
	V_{IL2}	0		0.3	0		0.5	V	CL1
Input voltage, high	V_{IH1}	$0.8V_{DD}$		V_{DD}	$0.7V_{DD}$		V_{DD}	V	Except CL1
	V_{IH2}	$V_{DD}-0.3$		V_{DD}	$V_{DD}-0.5$		V_{DD}	V	CL1
	V_{IH3}	$0.5V_{DD}$		12(1)	$0.7V_{DD}$		12(1)	V	Ports 10, 11
	V_{IHDR}	$0.7V_{DDDR}$		$V_{DDDR}+0.2$	$0.9V_{DDDR}$		$V_{DDDR}+0.2$	V	RESET; data retention
Output voltage low	V_{OL}			0.5				V	Ports 10, 11; $I_{OL} = 350\,\mu A$
							0.4	V	Ports 10, 11; $V_{DD} = 4.5$ V to 6.0 V, $I_{OL} = 1.6$ mA
							2.0	V	Ports 10, 11; $V_{DD} = 4.5$ V to 6.0 V, $I_{OL} = 10$ mA
							0.5	V	Ports 10, 11; $V_{DD} = 2.7$ V, $I_{OL} = 400\,\mu A$
				0.5				V	Ports 8, 9; $I_{OL} = 500\,\mu A$
							2.0	V	Ports 8, 9; $V_{DD} = 4.5$ V to 6.0 V, $I_{OL} = 15$ mA
							0.5	V	Ports 8, 9; $V_{DD} = 2.7$ V, $I_{OL} = 600\,\mu A$
Output voltage high	V_{OH}	$V_{DD}-1.0$						V	Ports 8–11; $I_{OH} = -80\,\mu A$
					$V_{DD}-2.0$			V	Ports 8–11; $V_{DD} = 4.5$ V to 6.0 V, $I_{OH} = 1$ mA
					$V_{DD}-1.0$			V	Ports 8–11; $V_{DD} = 2.7$ V, $I_{OH} = 100\,\mu A$
Supply voltage, data retention mode	V_{DDDR}	2.0			2.0			V	
Input leakage current	I_{LI1}	−3		3	−3		3	μA	Except CL1; $0 V \leq V_I \leq V_{DD}$
	I_{LI2}	−10		10	−10		10	μA	CL1; $0 V \leq V_I \leq V_{DD}$
	I_{LI3}			10(1)			10(1)	μA	Ports 10, 11; $V_O = 12$ V
Output leakage current	I_{LO1}	−3		3	−3		3	μA	$0 V \leq V_O \leq V_{DD}$
	I_{LO2}			10(1)			10(1)	μA	Ports 8–11; $V_O = 12$ V

DC Characteristics (cont)

μPD7556: $T_A = -10°C$ to $+70°C$, $V_{DD} = +2.5$ V to 3.3 V, GND = 0 V
μPD7556/μPD7566: $T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V, GND = 0 V

		Limits							
		$T_A = 10°C$ to $+70°C$, $V_{DD} = +2.5$ V to 3.3 V μPD7556			$T_A = 10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V μPD7566/μPD7556				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Supply current, normal operation	I_{DD1}		55	180				μA	R oscillation; $V_{DD} = 3$ V ± 0.3 V, R = 150 kΩ ± 2%
			40	150				μA	R oscillation; $V_{DD} = 2.5$ V, R = 150 kΩ ± 2%
						650	2200	μA	Ceramic oscillation; $V_{DD} = 5$ V ± 0.5 V, $f_{CC} = 700$ kHz
						120	360	μA	Ceramic oscillation; $V_{DD} = 3$ V ± 10%, $f_{CC} = 300$ kHz
						270	900	μA	R oscillation; $V_{DD} = 5$ V ± 0.5 V, R = 56 kΩ ± 2%
						80	240	μA	R oscillation; $V_{DD} = 3$ V ± 10%, R = 100 kΩ ± 2%
Supply current, HALT mode	I_{DD2}		25	80				μA	R oscillation; $V_{DD} = 3$ V ± 0.3 V, R = 150 kΩ ± 2%
			18	60				μA	R oscillation; $V_{DD} = 2.5$ V, R = 150 kΩ ± 2%
						450	1500	μA	Ceramic oscillation; $V_{DD} = 5$ V ± 0.5 V, $f_{CC} = 700$ kHz
						65	200	μA	Ceramic oscillation; $V_{DD} = 3$ V ± 10%, $f_{CC} = 300$ kHz
						120	400	μA	R oscillation; $V_{DD} = 5$ V ± 0.5 V, R = 56 kΩ ± 2%
						35	110	μA	R oscillation; $V_{DD} = 3$ V ± 10%, R = 100 kΩ ± 2%
Supply current, STOP mode	I_{DD3}		0.1	5				μA	
						0.1	10	μA	$V_{DD} = 5$ V ± 0.5 V
						0.1	5	μA	$V_{DD} = 3$ V ± 10%
Supply current, data retention mode	I_{DDDR}		0.1	5		0.1	5	μA	$V_{DDDR} = 2.0$ V
Pull-up / down resistance	RP1	23.5	47	70.5	23.5	47	70.5	kΩ	Port 0, RESET, Port 1
Pull-up resistance	RP2	7.5	15	22.5	7.5	15	22.5	kΩ	Ports 8–11

Note:
(1) N-channel open-drain I/O ports.

3

Comparator

$T_A = -10°C$ to $+70°C$, $V_{DD} = 3.0$ V to 6.0 V, GND = 0 V

Parameter	Symbol	Limits μPD7556 Min	Typ	Max	Limits μPD7566 Min	Typ	Max	Unit	Test Conditions
Input voltage range	V_{CIN} / V_{REF}	0		V_{DD}	0		V_{DD}	V	All comparators
Response time	T_{COMP}	2		4	2		4	MC(1)	All comparators
Input voltage resolution	ΔV_{CIN}			100			100	mV	All comparators
			10	50		10	50	mV	All comparators; $V_{DD} = 5\text{ V} \pm 0.5\text{ V}$
Input leakage current	I_{CIN} / I_{REF}	−3		3	−3		3	μA	All comparators
V_{REF} bias resistance (R1, R2)	BIAS		100			100		kΩ	(R1 = R2) typically
Comparator circuit current	I_{DDCMP}		50			50		μA	Comparator; $V_{DD} = 5\text{ V} \pm 0.5\text{ V}$

Note:
(1) Machine cycle.

AC Characteristics

μPD7556: $T_A = -10°C$ to $+70°C$, $V_{DD} = +2.5$ V to 3.3 V, GND = 0 V
μPD7556/μPD7566: $T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V, GND = 0 V

Parameter	Symbol	Limits: $T_A = 10°C$ to $+70°C$, $V_{DD} = +2.5$ V to 3.3 V, μPD7556 Min	Typ	Max	Limits: $T_A = 10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V, μPD7566/μPD7556 Min	Typ	Max	Unit	Test Conditions
System clock oscillator frequency	f_{CC}	140	180	220				kHz	R = 150 kΩ ± 2%
					400	500	600	kHz	$V_{DD} = 4.5$ V to 6.0 V; R = 56 kΩ ± 2%
					200	250	300	kHz	$V_{DD} = 3\text{ V} \pm 10\%$, R = 100 kΩ ± 2%
		140	175	210				kHz	CL1, CL2; $V_{DD} = 2.5$ V; R = 150 kΩ ± 2%
External clock frequency	f_C	10		250				kHz	CL1; 50% duty
					10		710	kHz	CL1; $V_{DD} = 4.5$ V to 6.0 V; 50% duty
					10		350	kHz	CL1; $V_{DD} = 2.7$ V; 50% duty
System clock rise time	t_{CR}			200			200	ns	CL1
System clock fall time	t_{CF}			200			200	ns	CL1
System clock pulse width, low	t_{CL}	2		50				μs	
					1.45		50	μs	CL1; $V_{DD} = 2.7$ V
System clock pulse width, high	t_{CH}	2		50				μs	
					0.7		50	μs	CL1; $V_{DD} = 4.5$ V to 6.0 V
	f_{CC}	290	700	710				kHz	$V_{DD} = 4.5$ to 6.0 V
		290	500	510				kHz	$V_{DD} = 4.0$ to 6.0 V
		290	400	410				kHz	$V_{DD} = 3.5$ to 6.0 V
		290	300	310				kHz	$V_{DD} = 2.7$ to 6.0 V

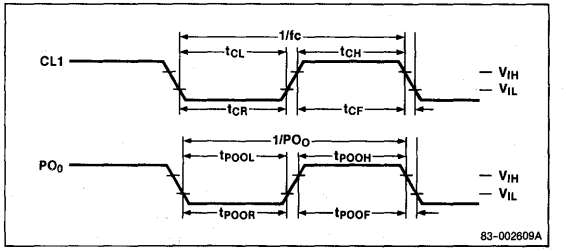
AC Characteristics (cont)

μPD7556: $T_A = -10°C$ to $+70°C$, $V_{DD} = +2.5$ V to 3.3 V, GND = 0 V
μPD7556/μPD7566: $T_A = -10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V, GND = 0 V

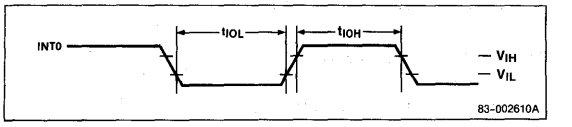
		Limits							
		$T_A = 10°C$ to $+70°C$, $V_{DD} = +2.5$ V to 3.3 V μPD7556			$T_A = 10°C$ to $+70°C$, $V_{DD} = +2.7$ V to 6.0 V μPD7566/μPD7556				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Oscillator setup	t_{OS}	20						μs	Oscillator stabilization time after $V_{DD} = 4.5$ V
External clock frequency (PO_0)	f_{POO}	0		250				kHz	50% duty
					0		710	kHz	$V_{DD} = 4.5$ V to 6.0 V; 50% duty
					0		350	kHz	$V_{DD} = 2.7$ V; 50% duty
PO_0 rise time	t_{CRPO}			200			200	ns	
PO_0 fall time	t_{CFPO}			200			200	ns	
PO_0 pulse width, low	t_{POOL}	2						μs	
					1.45			μs	$V_{DD} = 2.7$ V
PO_0 pulse width, high	t_{POOH}	2						μs	
					0.7			μs	$V_{DD} = 4.5$ V to 6.0 V
INT0 low time	t_{IOL}	30			10			μs	
INT0 high time	t_{IOH}	30			10			μs	
RESET low time	t_{RSL}	30			10			μs	
RESET high time	t_{RSH}	30			10			μs	
RESET setup time	t_{SRS}	0			0			μs	
RESET hold time	t_{HRS}	0			0			μs	

Timing Waveforms

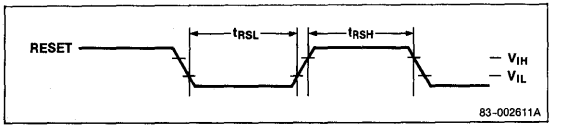
Clocks



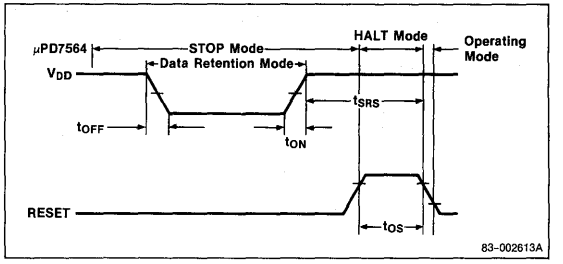
External Interrupt



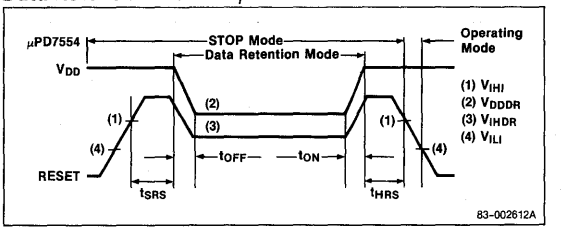
Reset



Data Retention Mode — μPD7566



Data Retention Mode — μPD7556



Pin Mask Options

Table 1 shows the mask options for all the port pins and the RESET pin. You may select these options in bit units.

Table 1. Pin Mask Options

Pin	Options	
$P0_0$	1	No connection to internal resistor
	2	Connected to internal pull-up resistor
	3	Connected to internal pull-down resistor
$P0_1$ / V_{REF}	1	No connection to internal resistor
	2	Connected to internal pull-up resistor
	3	Connected to internal pull-down resistor
	4	Used as V_{REF} pin
	1	A bias of V_{DD} / 2 internally applied to V_{REF} pin
	2	Bias not applied
$P1_0$ / CIN_0– $P1_3$ / CIN_3	1	No connection to internal resistor
	2	Connected to internal pull-up resistor
	3	Connected to internal pull-down resistor
	4	Used as comparator input pins
$P8_0$–$P8_2$	1	CMOS (push-pull) output
$P9_0$–$P9_1$	2	N-channel open-drain output
$P8_3$–CL_2 (7556) option one	1	Used as P83
	2	Used as CL2
$P8_3$–CL_2 (7556) option two	1	CMOS push-pull
	2	N-channel open-drain
$P10_0$–$P10_3$ $P11_0$–$P11_3$	1	N-channel open-drain input / output
	2	CMOS (push-pull) input / output
	3	N-channel open-drain input / output with internal pull-up resistor
RESET	1	Connected to internal pull-down resistor
	2	Not connected to internal pull-down resistor

I/O Pin Configurations

Figure 1. Type 1 Input Cell (part of Type 2)

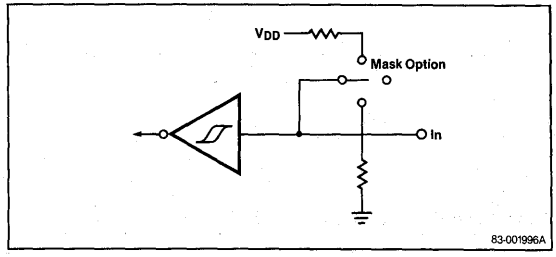


Figure 2. Type 2 Schmitt-triggered Input: $P1_0$–$P1_3$/CIN_0–CIN_3

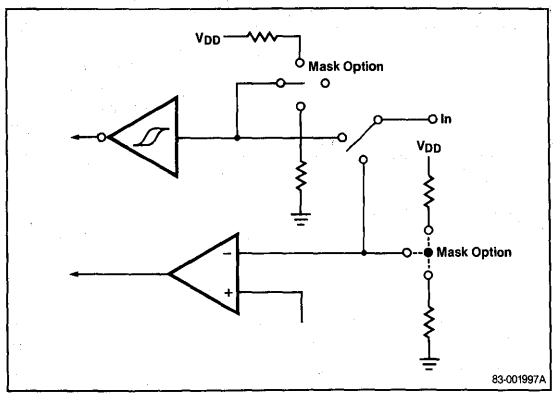


Figure 3. Type 3 Input Cell: $P0_1$/V_{REF}

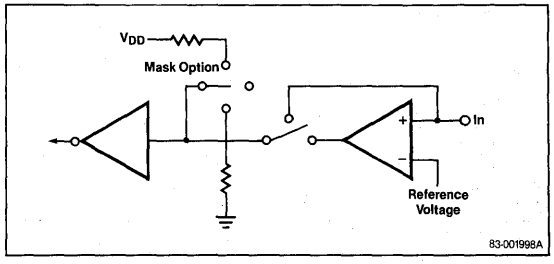


Figure 4. Type 4 Output Cell: $P8_0$–$P8_3$, $P9_0$–$P9_1$

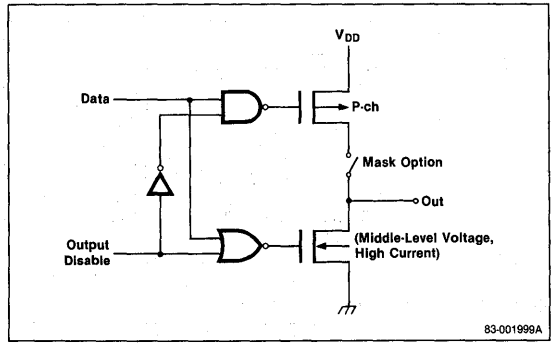


Figure 5. Type 5 I/O Cell: $P10_0$-$P10_3$, $P11_0$-$P11_3$

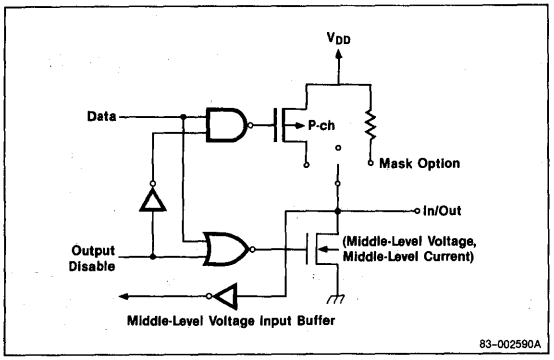
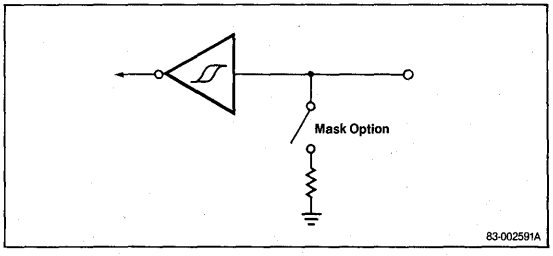


Figure 6. Type 6 Schmitt-triggered Input: $P0_0$/INT0



Program Memory

The μPD7556/66 has a mask-programmable ROM with a capacity of 1024 words by 8 bits for program storage or table data. It is addressed by the program counter. The reset start address is 000H. Figure 7 shows the program memory map.

General Purpose Registers

Two registers, H (2-bit) and L (4-bit), are provided as general purpose registers. Each register can be individually manipulated. The two registers also form pair register HL; H being the high register and L being the low one. The HL register is a data pointer to address data memory. Figure 8 shows the configuration of the general purpose registers.

The L register also specifies an I/O port or mode register when an I/O instruction (IPL or OPL) is executed. It also specifies the bits of a port when the SPBL or RPBL instruction is executed.

Figure 7. Program Memory Map

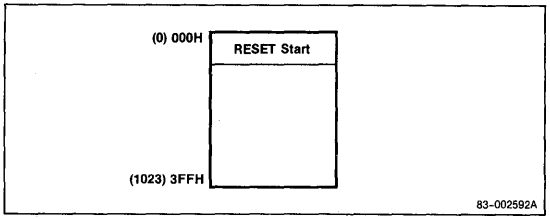
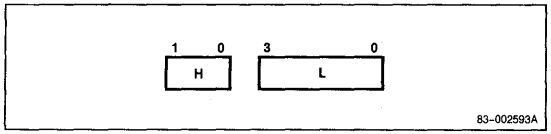


Figure 8. Configuration of General Purpose Registers



Data Memory

The data memory is static RAM with a capacity of 64 words by 4 bits. Part of this memory is used as the stack area. The data memory is also used in 8-bit data processing when paired with the accumulator. Figure 9 shows the data memory map.

Data memory can be addressed directly, with the immediate data from an instruction; indirectly, with the contents of HL (including autoincrement and autodecrement); and indirectly by the contents of the stack pointer.

You may use any area of the data memory as the stack. The boundary of the stack is determined by how the TAMSP instruction initializes the stack pointer. Once the boundary is set, a call or return instruction automatically accesses the stack.

When a call instruction is executed, the contents of the program counter and the program status word (PSW) are stored to the stack in the sequence shown in figure 10.

When a return instruction is executed, the contents of the program counter are automatically restored, but the PSW is not. The contents of data memory can be retained with a low supply voltage during STOP mode.

Accumulator

The accumulator is a 4-bit register used in arithmetic operations. The accumulator can process 8-bit data when paired with the data memory addressed by HL. Figure 11 shows the configuration of the accumulator.

Figure 9. Data Memory Map

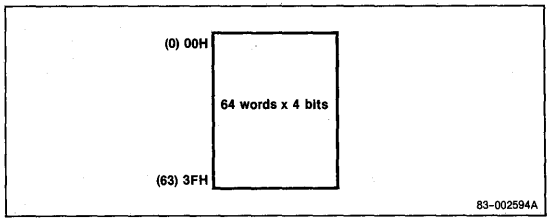


Figure 10. Call Instruction Storage to Stack

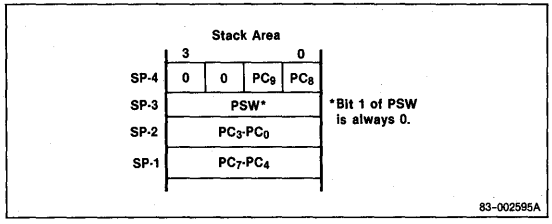
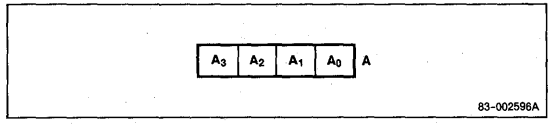


Figure 11. Configuration of the Accumulator



Arithmetic Logic Unit

The arithmetic logic unit (ALU) is a 4-bit arithmetic circuit that performs operations such as binary addition, logical operation, increment, decrement, comparison, and bit processing.

Program Status Word

The program status word (PSW) consists of two skip flags (SK0 and SK1), a carry flag (C), and bit 1, which is always zero. Figure 12 shows the configuration of the PSW.

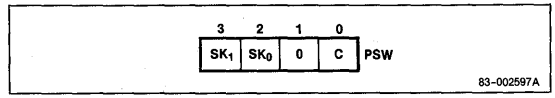
The contents of the PSW are stored to the stack when a call instruction is executed, but are not restored from the stack by the return instruction.

The skip flags retain the following skip conditions: string effect by LAI or LHLI instruction, and skip condition satisfied by an instruction other than a string-effect instruction. The skip flag is set or reset in accordance with the instruction executed.

The carry flag is set to 1 if an addition instruction (ACSC) generates a carry from bit 3 of the ALU. If no carry is generated, the flag is reset to zero. The SC instruction sets the carry flag and the RC instruction resets it.

When a RESET is input, the SK1 and SK0 flags are cleared to zero and the contents of the carry flag are undefined.

Figure 12. Configuration of the Program Status Word



System Clock Generator

The system clock generator consists of a RC oscillator (7556) a ceramic resonator (7566), a 1/2 frequency divider, standby modes (STOP/HALT), and control circuit. Figure 13 is a circuit diagram of the system clock generator for the μPD7556.

In the μPD7556, the RC oscillator operates with a single external resistor connected across CL1 and CL2 (the capacitor C is incorporated). When the RC oscillator is not used, external clock pulses can be input via the CL1 pin. In this case, the RC oscillator functions as an inverting buffer. The output from the RC oscillator serves as the system clock (CL) which is then divided by two and used as the CPU clock (ϕ).

The standby mode control circuit is made up of a STOP flip-flop and a HALT flip-flop. The STOP instruction sets the STOP flip-flop and stops the system clock supply. This flip-flop also stops the RC oscillator. The STOP flip-flop is reset by the standby release signal that becomes active when one of the test request flags is set or at the falling edge of the RESET signal. When the STOP flip-flop is reset, the RC oscillator resumes operation and supplies the system clock.

The HALT instruction sets the HALT flip-flop which disables signals from going to the 1/2 frequency divider that generates the CPU clock. Only the CPU clock stops in HALT mode. The HALT flip-flop is set or reset by the same conditions as the STOP flip-flop.

Figure 14 shows the system clock generator circuit for the μPD7566.

On the μPD7566, the ceramic oscillator operates with a ceramic resonator connected across CL1 and CL2. The output from the ceramic oscillator is used as the system clock (CL); it is divided by two to produce the CPU clock (ϕ).

The standby mode control circuit is made up of a STOP flip-flop and a HALT flip-flop. The STOP instruction sets the STOP flip-flop and stops the ceramic oscillation, thus stopping the supply for all clocks. The STOP flip-flop is reset by the RESET signal (high level) and restarts ceramic oscillation. The supply of each clock resumes when RESET goes low.

Figure 13. System Clock Generator for μPD7556

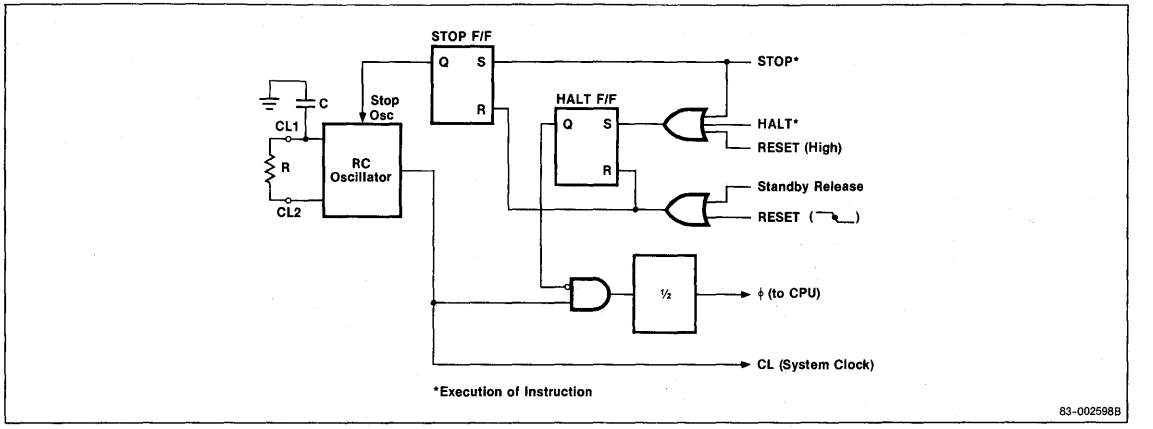
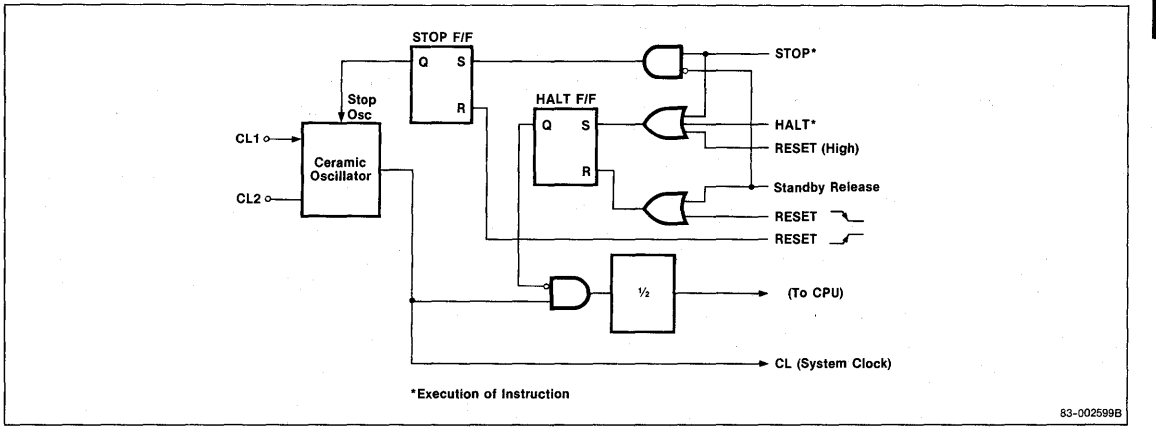


Figure 14. System Clock Generator for μPD7566



The HALT instruction sets the HALT flip-flop which disables signals from going to the ½ frequency divider that generates the CPU clock. Only the CPU clock stops in HALT mode. The HALT flip-flop is reset by the HALT RELEASE signal (activated by setting at least one test request flag) or the falling edge of RESET, resuming supply of the CPU clock.

The HALT flip-flop is also set when RESET is active (high level). At power-on reset operation, the rising edge of RESET starts ceramic oscillation; however, some time is required to achieve stable oscillation. To prevent the unstable clock from operating the CPU, the HALT flip-flop is set and the CPU clock is stopped while RESET is high. Accordingly, the high-level width of RESET must be more than the required stable time for the ceramic resonator.

Clock Control Circuit

The clock control circuit consists of a 2-bit clock mode register (bits CM1 and CM2), prescalers 1, 2, and 3, and a multiplexer. It takes the output of the system clock generator (CL) and event pulses ($P0_0$). It also selects the clock source and prescaler according to the setting in the clock mode register and supplies the timer/event counter with count pulses. Figure 15 shows the clock control circuit.

Table 2 lists the codes set in the clock mode register by the OPL instruction to specify the count pulse frequency.

Figure 15. Clock Control Circuit

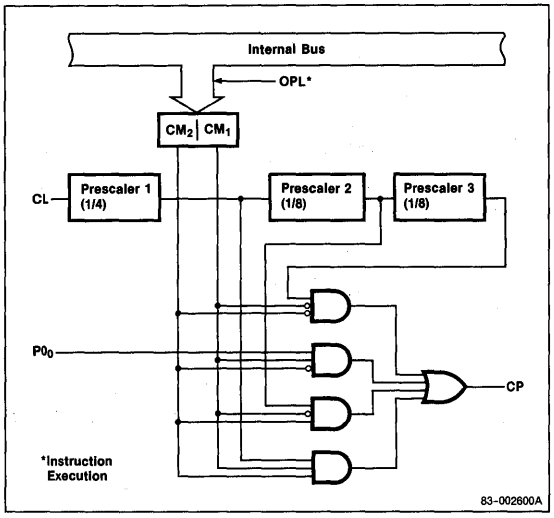


Table 2. Selecting the Count Pulse Frequency

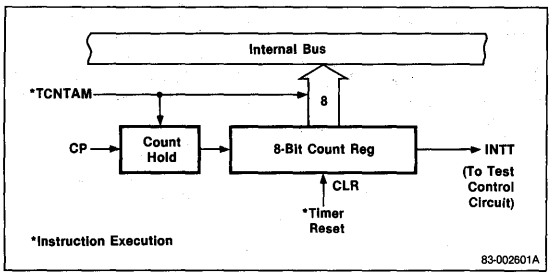
CM2	CM1	Frequency Selected
0	0	CL/256
0	1	$P0_0$
1	0	CL/32
1	1	CL/4

When you set the clock mode register with the OPL instruction, clear bit 0 of the accumulator (corresponding to bit CM0 of the EVAKIT-7500 or μPD7500H during emulation).

Timer/Event Counter

The timer/event counter is a binary 8-bit up-counter which is incremented each time a count pulse is input. The TIMER instruction or a RESET signal clears it to 00H. When an overflow occurs, the counter is reset from FFH to 00H. Figure 16 shows the inputs and outputs of the counter.

Figure 16. Timer/Event Counter



Test Control Circuit

The μPD7556/66 has two test sources, as shown in table 3.

Table 3. μPD7556/66 Test Sources

Source	Function	Location	Request Flag
INTT	Overflow in timer / event counter	Internal	INTT RQF
INT0	Test request signal from $P0_0$ pin	External	INT0 RQF

The test control circuit consists of two test request flags (INTT RQF and INT0 RQF) set by the two test sources, the SM3 flag which determines whether INT0 is enabled, and a test request flag control circuit that checks the contents of each test request flag by executing an SKI instruction and resetting the flags.

The OPL instruction (L = FH, corresponding to A3) sets the SM3 flag. INT0 is enabled when SM3 = 1.

The request flag INTT RQF is set when a timer overflow occurs in the timer event counter. The SKI or TIMER instruction resets it.

Request flag INT0 RQF is set at the rising edge of the signal input to the INT0/$P0_0$ pin and the SKI instruction resets it.

The logical sum of the outputs from the test request flags release HALT mode. The mode is released when one or both flags are set. Both flags and SM3 are reset when the RESET signal is input. After reset, signal input to the INT0 pin is inhibited as the initial condition.

Figure 17 is a block diagram of the test control circuit.

Standby Modes

The μPD7556/66 has two standby modes to reduce power consumption while the program is in the wait state. The STOP and HALT instructions set these modes.

When the program enters a standby mode, program execution stops and the contents of all registers and data memory immediately before the program entered standby mode are retained. The timer can operate even in HALT mode.

The RESET signal or standby release signal (7556 only) releases STOP mode. HALT mode is released when one or both of the test request flags are set, or when the RESET signal is input. The program cannot enter a standby mode when a test request is being set, even if the STOP or HALT command is executed.

If there is some uncertainty as to the state of the test request flags, execute the SKI instruction to reset them so the program can enter standby mode.

Figure 17. Test Control Circuit Block Diagram

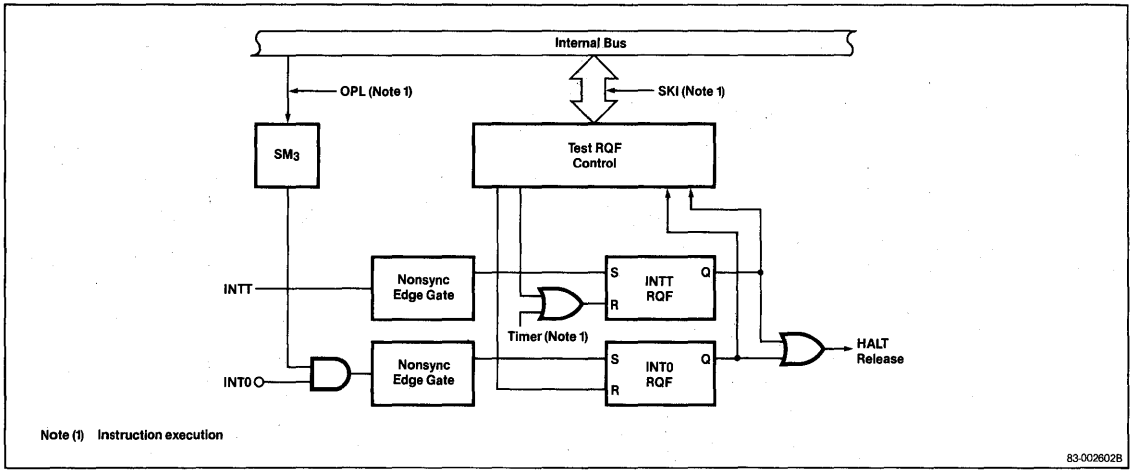


Table 4 compares STOP and HALT modes. The main difference is that STOP mode stops the system clock and HALT does not. Oscillation stops during STOP mode. The power consumed by the oscillator is the difference between the two modes. In STOP mode, data memory can be retained with a lower supply voltage.

Table 4. STOP and HALT Modes

Mode	CL	ϕ	PO_0	CPU	Timer	Released by
STOP	x	x	o	x	Δ	RESET input INTT RQF, INT0 RQF (7556 only)
HALT	o	x	o	x	o	INTT RQF INT0 RQF RESET input

Note:
o = operates
x = stops
Δ = operational depending on clock source

Power-on Reset Circuit

Figure 18 shows a circuit example of the power-on reset circuit using a resistor and a capacitor. This is the simplest reset control circuit. Figure 19 shows the circuit with a pull-down resistor internally connected to RESET as a mask option.

Figures 20 to 23 show examples of application circuits for the μPD7556/66.

Figure 18. Power-on Reset Circuit

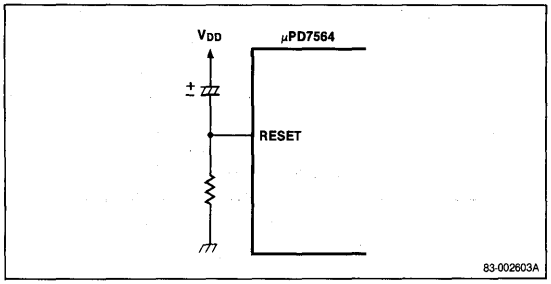


Figure 19. Power-on Reset Circuit with Pull-down Resistor

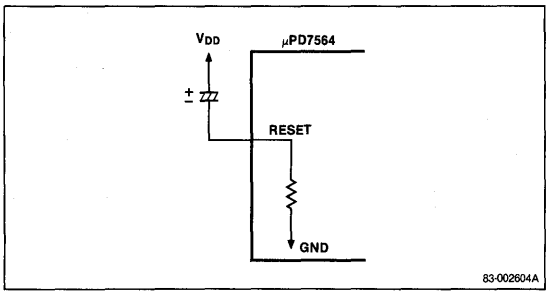


Figure 20. Refrigerator or Air Conditioner Circuitry

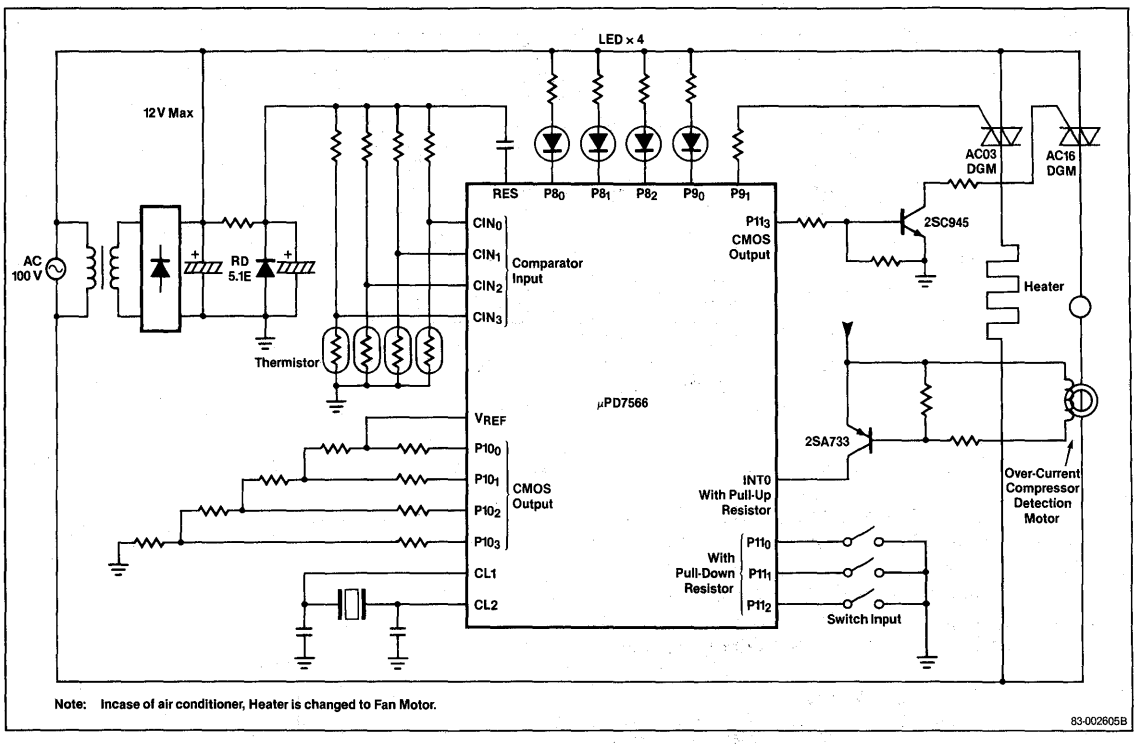


Figure 21. Rice Cooker Circuitry

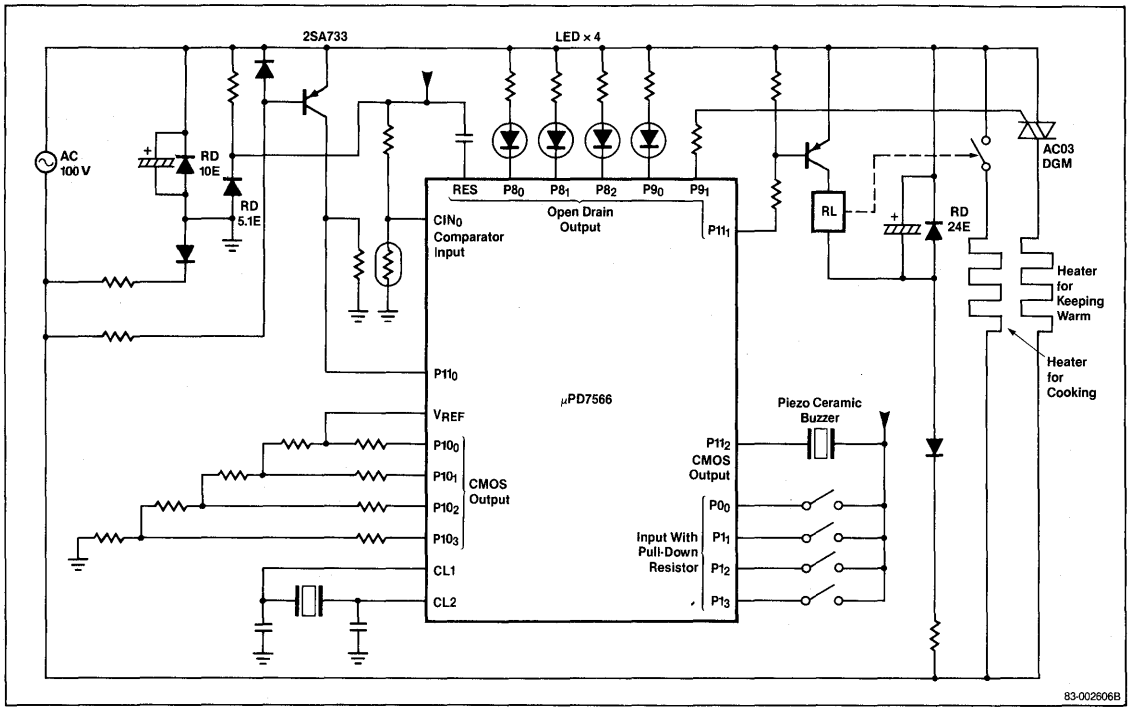


Figure 22. Washing Machine Circuitry

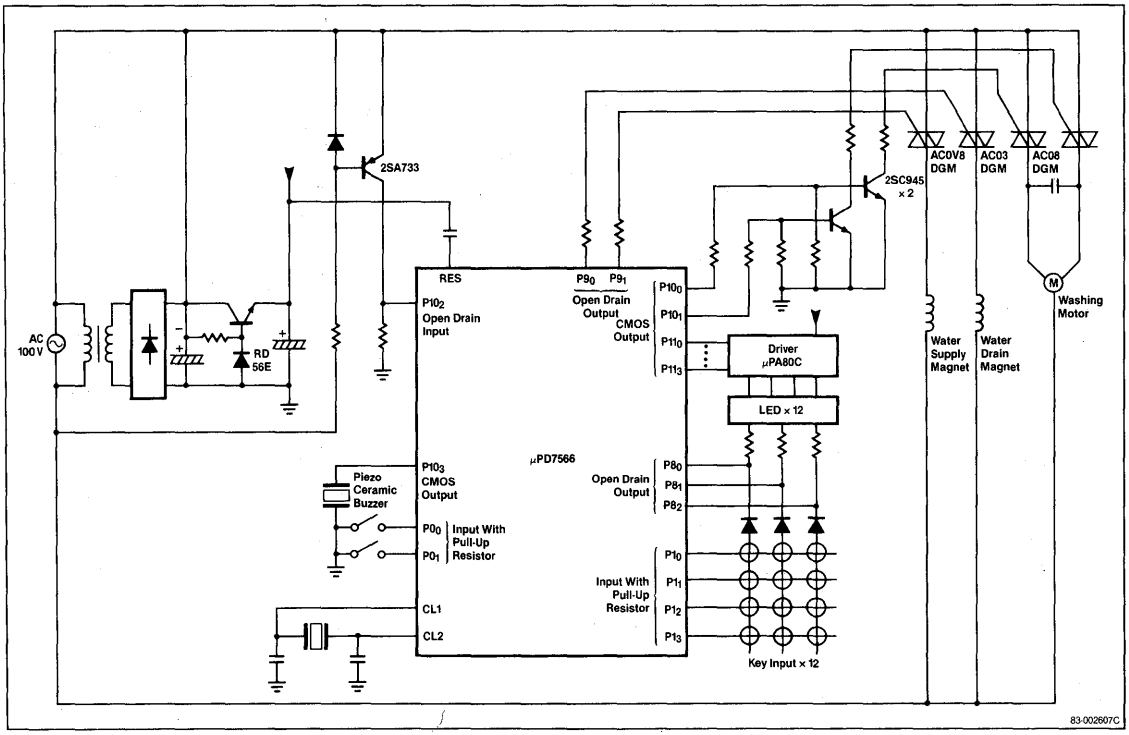


Figure 23. Tape Deck Controller Circuitry

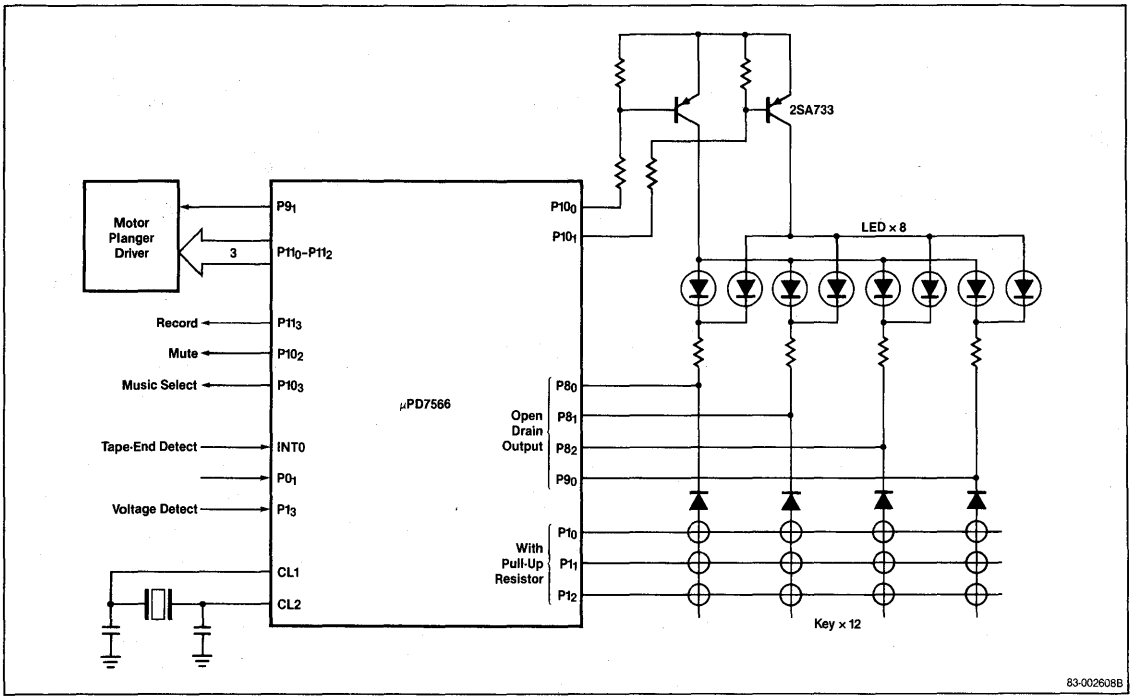


Table 5 compares the features of products in this part of the 7500 series devices.

Table 5. Product Comparison

Item		μPD7554	μPD7564	μPD7556	μPD7566
Instruction cycle / system clock (5 V)	RC	4 μs / 500 kHz		4 μs / 500 kHz	
	External	2.86 μs / 700 kHz		2.86 μs / 700 kHz	
	Ceramic		3 μs / 660 kHz		3 μs / 660 kHz
Instruction set		47	47	45	45
ROM		1024 × 8	1024 × 8	1024 × 8	1024 × 8
RAM		64 × 4	64 × 4	64 × 4	64 × 4
I / O port total		16 (max)	15	20 (max)	19
Port 0		$P0_0$–$P0_3$	$P0_0$–$P0_3$	$P0_0$–$P0_1$	$P0_0$–$P0_1$
Port 1				$P1_0$–$P1_3$	$P1_0$–$P1_3$
Port 8		$P8_0$–$P8_2$ $P8_2$ / CL2	$P8_0$–$P8_2$	$P8_0$–$P8_2$ $P8_3$ / CL2	$P8_0$–$P8_2$
Port 9				$P9_0$–$P9_1$	$P9_0$–$P9_1$
Port 10		$P10_0$–$P10_3$	$P10_0$–$P10_3$	$P10_0$–$P10_3$	$P10_0$–$P10_3$
Port 11		$P11_0$–$P11_3$	$P11_0$–$P11_3$	$P11_0$–$P11_3$	$P11_0$–$P11_3$
Timer / event counter		8-bit	8-bit	8-bit	8-bit
Serial interface		8-bit	8-bit		
Comparator				4-channel	4-channel
Process		CMOS	CMOS	CMOS	CMOS
Package		20-pin plastic shrink DIP	20-pin plastic shrink DIP	24-pin plastic shrink DIP	24-pin plastic shrink DIP

μPD75104/106/108
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

Description

The μPD75104, μPD75106, and μPD75108 are high-performance single-chip CMOS microcomputers that incorporate a CPU, ROM, RAM, I/O ports, vector interrupt functions, serial interface, and timer/event counters.

The devices can manipulate data in 1-, 4-, or 8-bit units. A variety of bit manipulation instructions enhance I/O data control. The devices are especially suitable for controlling VCRs, audio sets, touch-tone telephones, and printers.

Features

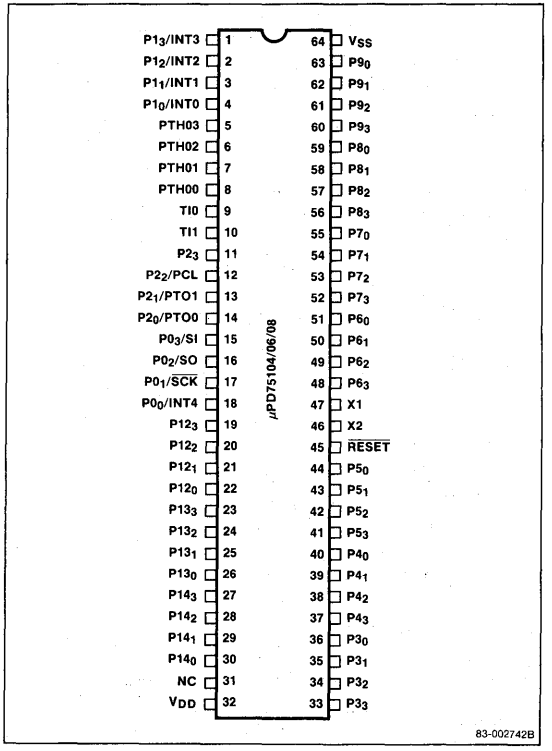
- ☐ 46 instructions
  - — Bit manipulation instructions
  - — 8-bit data transfer, comparison, and increment/decrement instructions
  - — 1-byte relative branch instructions
  - — GETI instruction that realizes 2- or 3-byte instructions in 1-byte units
- ☐ Instruction cycles
  - — High-speed cycle: 0.95 μs/4.19 MHz, V_{DD} = 5 V
  - — Low-voltage cycle: 1.91 μs/4.19 MHz, 15.3 μs/4.19 MHz
- ☐ Program memory (ROM)
  - — μPD75104: 4096 x 8 bits
  - — μPD75106: 6016 x 8 bits
  - — μPD75108: 8064 x 8 bits
- ☐ Data memory (RAM)
  - — μPD75104: 320 x 4 bits
  - — μPD75106: 320 x 4 bits
  - — μPD75108: 512 x 4 bits
- ☐ Bit manipulation memory (bit-sequential buffer): 16 bits
- ☐ Four banks of 8 x 4-bit general purpose registers
- ☐ Accumulators
  - — Bit accumulator (CY)
  - — 4-bit accumulator (A)
  - — 8-bit accumulator (XA)
- ☐ 58 I/O lines
  - — High-current output ports that can directly drive LEDs (total of 200 mA for 32 pins)
  - — 12 N-channel, open-drain outputs with 12 V maximum
  - — Four programmable threshold comparator inputs
  - — Two external event inputs
- ☐ Vectored interrupt function capable of multiple interrupts
  - — Three external vectored interrupts
  - — Two external test inputs
  - — Four internal vectored interrupts
- ☐ Two 8-bit timer/event counters
- ☐ 8-bit serial interface
  - — Data transfer can start with LSB or MSB
  - — Two transfer modes (transmit/receive and receive-only)
  - — Mask option power-on reset circuit
  - — Crystal or ceramic oscillator
  - — Standby modes (STOP/HALT)
  - — CMOS technology
  - — Low power consumption

Ordering Information

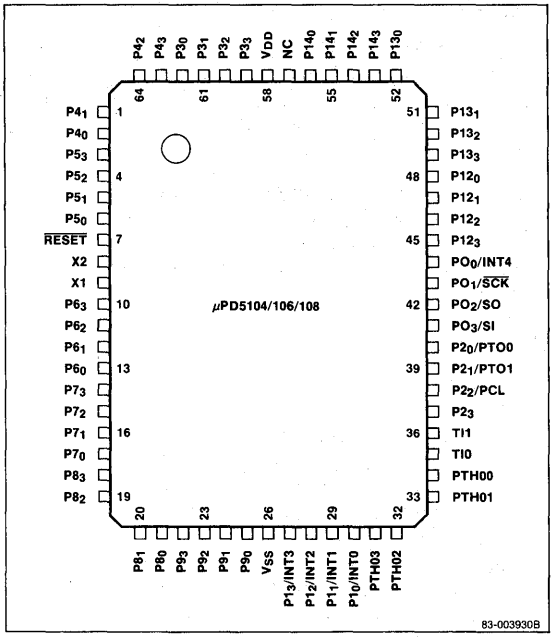
Part Number	ROM (Bytes)	Package Type
μPD75104CW	4096	64-pin plastic shrink DIP
μPD75106CW	6016	64-pin plastic shrink DIP
μPD75108CW	8064	64-pin plastic shrink DIP
μPD75104G-1B	4096	64-pin plastic miniflat
μPD75106G-1B	6016	64-pin plastic miniflat
μPD75108G-1B	8064	64-pin plastic miniflat

Pin Configurations

64-Pin Shrink DIP



64-Pin Miniflat



Pin Identification

Symbol	Function
$P1_3$/INT3 $P1_2$/INT2 $P1_1$/INT1 $P1_0$/INT0	4-bit input port 1/Edge-triggered vectored interrupts
PTH03- PTH00	Programmable threshold comparator analog input port
TI0, TI1	External event input for timer/event counter
$P2_3$, $P2_2$/PCL $P2_1$/PTO1, $P2_0$/PTO0	4-bit I/O port 2/Clock output terminal/Timer/ event counter output pins
$P0_3$/SI $P0_2$/SO $P0_1$/SCK $P0_0$/INT4	4-bit input port 0/Serial interface/Edge-triggered vectored interrupt
$P12_3$-$P12_0$	4-bit I/O port 12
$P13_3$-$P13_0$	4-bit I/O port 13

Symbol	Function
$P14_3$-$P14_0$	4-bit I/O port 14
NC	No connection
V_{DD}	Positive power supply
$P3_3$-$P3_0$	Programmable 4-bit I/O port 3
$P4_3$-$P4_0$	4-bit I/O port 4
$P5_3$-$P5_0$	4-bit I/O port 5
RESET	Reset input
X2, X1	Ceramic or crystal system clock oscillator
$P6_3$-$P6_0$	Programmable 4-bit I/O port 6
$P7_3$-$P7_0$	4-bit I/O port 7
$P8_3$-$P8_0$	4-bit I/O port 8
$P9_3$-$P9_0$	4-bit I/O port 9
V_{SS}	Ground

Pin Functions

$P0_3$/SI, $P0_2$/SO, $P0_1$/$\overline{SCK}$, $P0_0$/INT4 [Port 0, Serial I/O, Interrupt 4]

Port 0 can be configured as a 4-bit parallel input port or as the serial I/O interface under control of the serial mode select register. The serial input SI (active high), serial output SO (active low), and the serial clock $\overline{SCK}$ (active low synchronizes data transfer) make-up the serial I/O interface. INT4 is an edge-triggered vectored interrupt triggered by a rising or falling edge. The port is in the input state at reset.

$P1_3$-$P1_0$/INT3-INT0 [Port 1, Interrupts 3-0]

Port 1 is a 4-bit input port. INT0 and INT1 are edge-triggered vectored interrupts selected by a rising or falling edge. INT2 and INT3 are triggered by a rising edge only. The port and the interrupts are in the input state at reset.

$P2_3$, $P2_2$/PCL, $P2_1$/PTO1, $P2_0$/PTO0 [Port 2, Clock Output, Timer/Event Counter Output]

Port 2 is a 4-bit I/O port for directly driving LEDs. PTO1 and PTO0 are the timer/event counter output pins. PCL is the clock output pin. These pins are in the input state at reset.

$P3_3$-$P3_0$ [Port 3]

Programmable 4-bit I/O port for directly driving LEDs with bit-level I/O selection. The port is in the input state at reset.

$P4_3$-$P4_0$ [Port 4]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 5.

$P5_3$-$P5_0$ [Port 5]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 4.

$P6_3$-$P6_0$ [Port 6]

Programmable 4-bit I/O port for directly driving LEDs with bit-level I/O selection. The port is in the input state at reset and has 8-bit I/O capability when paired with port 7.

$P7_3$-$P7_0$ [Port 7]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 6.

$P8_3$-$P8_0$ [Port 8]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 9.

$P9_3$-$P9_0$ [Port 9]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 8.

$P12_3$-$P12_0$ [Port 12]

4-bit I/O port, N-channel open-drain, 12 V max. An internal pull-up resistor is a mask option. The port is in the high-impedance state at reset when open-drain is selected or in the high-level state when a pull-up resistor is selected. Port 12 has 8-bit I/O capability when paired with port 13.

$P13_3$-$P13_0$ [Port 13]

4-bit I/O port, N-channel open-drain, 12 V max. An internal pull-up resistor is a mask option. The port is in the high-impedance state at reset when open-drain is selected or in the high-level state when a pull-up resistor is selected. Port 13 has 8-bit I/O capability when paired with port 12.

$P14_3$-$P14_0$ [Port 14]

4-bit I/O port, N-channel open-drain 12 V max. An internal pull-up resistor is a mask option. The port is in the high-impedance state at reset when open-drain is selected or in the high-level state when a pull-up resistor is selected.

PTH03-PTH00 [Threshold Detector Analog Input Port]

Threshold detector analog input port.

TI0, TI1 [Timer/Event Counter Input]

External event input for the timer/event counter. These two pins are also an edge-triggered vectored interrupt and a 1-bit input port.

$\overline{RESET}$ [Reset]

System reset input pin (active low).

X2, X1 [System Clock I/O]

These pins are the system clock I/O. The clock may be from an external source or from an internal oscillator controlled by a crystal or ceramic resonator connected to pins X2 and X1. See figure 1.

V_{DD} [Power Supply]

Positive power supply.

V_{SS} [Ground]

System ground.

μPD7500 Series

Table 1 compares the features of similar products in the μPD75000 series.

I/O Port Interfaces

Figure 2 shows the internal circuit configurations at the I/O ports.

Figure 1. System Clock Configurations

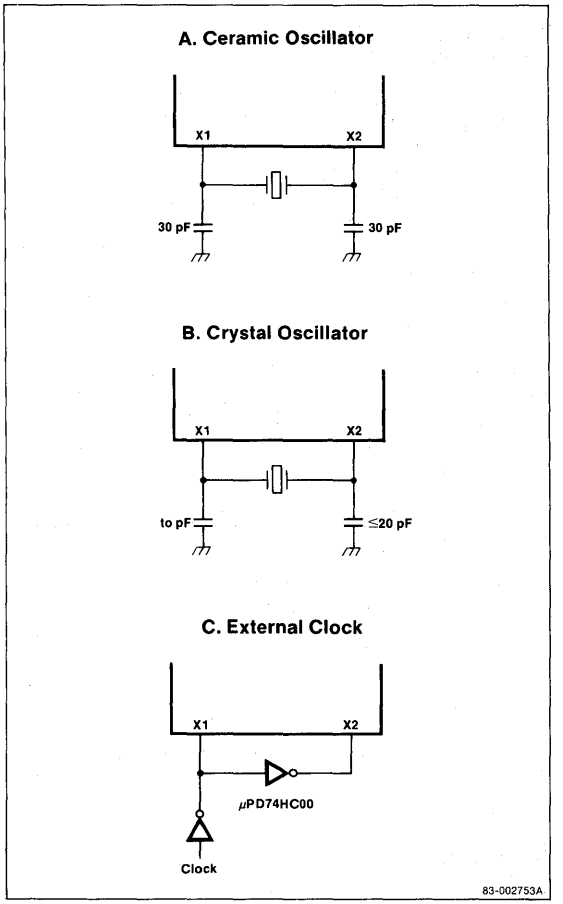
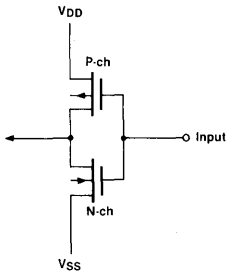


Table 1. Product Comparison

Item	μPD75P108	μPD75104	μPD75106	μPD75108
Program memory	EPROM 0000-1FFFH	Mask ROM 0000-0FFFH	Mask ROM 0000-177FH	Mask ROM 0000-1FFFH
Data memory	512 x 4-bit Bank 0: 256 Bank 1: 256	320 x 4-bit Bank 0: 256 Bank 1: 64	320 x 4-bit Bank 0: 256 Bank 1: 64	512 x 4-bit Bank 0: 256 Bank 1: 256
Instruction set	Set P108	Set P108 minus BR!addr (3-byte instr.)	Set P108	Set P108
Ports 12-14 pull-up resistor	Not offered	Mask option	Mask option	Mask option
Power-on reset	Integrated	Mask option	Mask option	Mask option
Power-on flag	Integrated	Mask option	Mask option	Mask option
Operating voltage	5 V ±10%	2.5 to 6.0 V	2.5 to 6.0 V	2.5 to 6.0 V
Pin 31	V_{PP}	NC	NC	NC
Packaging	64-pin ceramic shrink DIP	64-pin plastic miniflat or shrink DIP	64-pin plastic miniflat or shrink DIP	64-pin plastic miniflat or shrink DIP

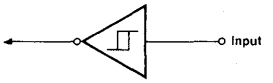
Figure 2. Interface at Input/Output Ports

Type A

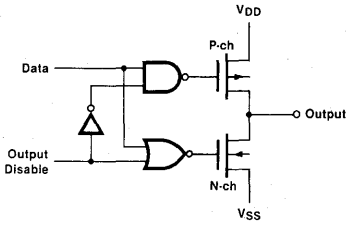


Type B

P13-P10/INT3-INT0, TI0, TI1, P00/INT4, P03/SI, RESET

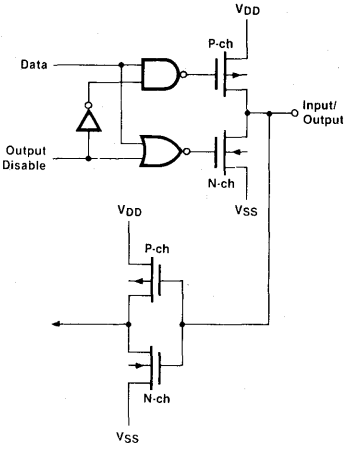


Type D



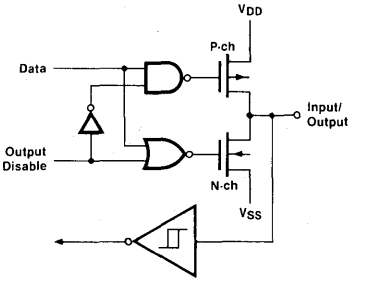
Type E

P23, P22/PCL, P21/PT01, P20/PTO0. P02/SO, P33-P30, P43-P40, P53-P50, P60, P73-P70, P83-P80, P93-P90



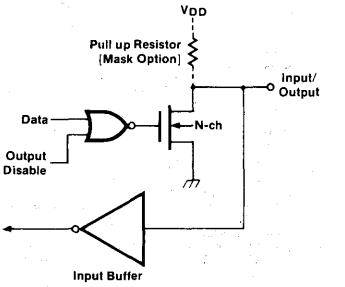
Type F

P01/SCK



Type M

P123-P120, P133-P130, P143-P140



Type N

PTH03-PTH09

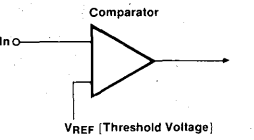
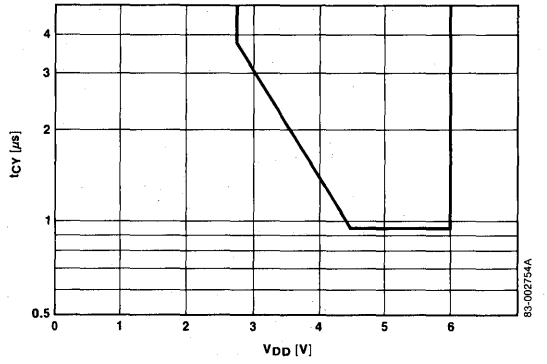
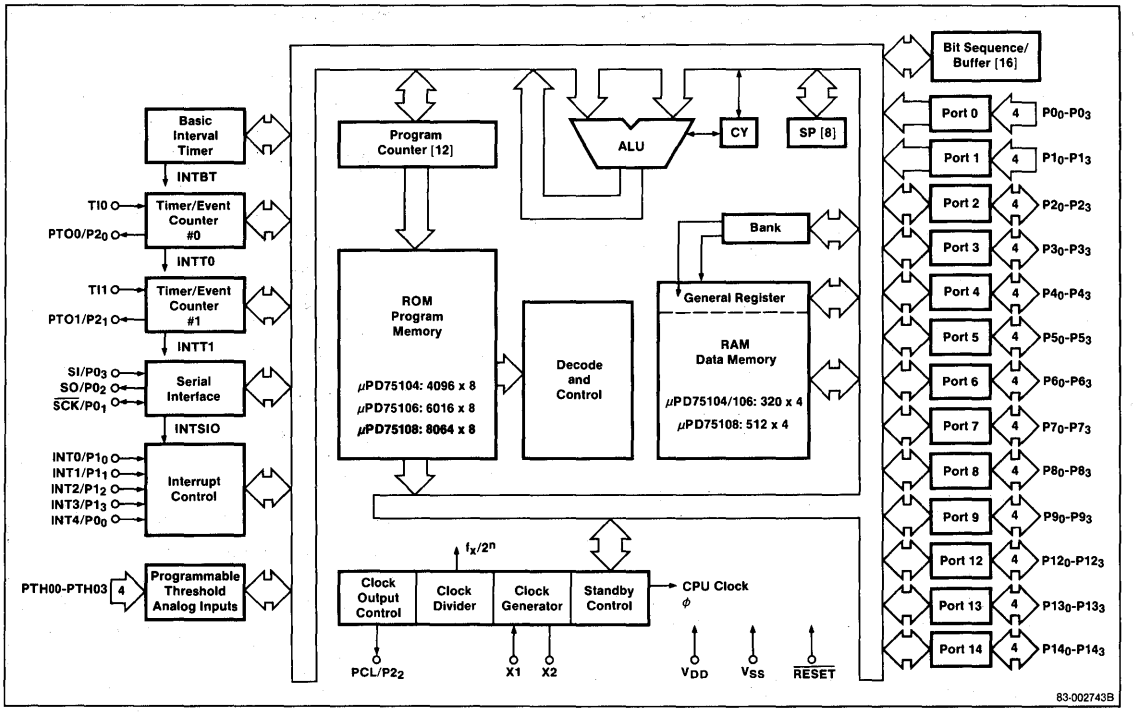


Figure 3. Cycle Time vs Supply Voltage



Block Diagram



Absolute Maximum Ratings

(Preliminary Specifications)

$T_A = 25°C$

Operating temperature, T_{OPT}	−40 to +85°C
Storage temperature, T_{STG}	−65 to +150°C
Power supply voltage, V_{DD}	−0.3 to +7.0 V
Input voltage	
Ports 12, 13, 14 (1), V_{I2}	−0.3 to +13 V
Other ports V_{I1}	−0.3 to V_{DD} + 0.3 V
Output voltage, V_O	−0.3 to V_{DD} + 0.3 V
Output current, high	
One pin	−15 mA
All output pins, total	−30 mA
Output current, low	
Single pin (peak value)	30 mA
	(2) 15 mA
Ports 0, 2-4, 12-14, total (peak value)	100 mA
	(2) 60 mA
Ports 5-9, total (peak value)	100 mA
	(2) 60 mA
Power dissipation, P_D ($T_A = 70°C$)	480 mW

Note:

(1) No internal pull-up resistor (mask option). If internal pull up resistor is used, then voltages are same as V_{I1}.

(2) The calculation method is: value = peak value x duty.

Comment: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$, $V_{DD} = GND = 0$ V, f = 1 MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			15	pF	Unmeasured pins returned to GND
Output capacitance	C_O			15	pF	
I/O capacitance	C_{IO}			15	pF	

3

DC Characteristics

$T_A = -40$ to $+85$°C, $V_{DD} = 2.7$ to 6.0 V, GND = 0 V

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input high voltage except X1, X2, TI0, TI1, ports 0, 1, 12-14, and RESET	V_{IH1}	0.7 V_{DD}		V_{DD}	V	
Input high voltage, ports 0, 1, TI0, TI1, and RESET	V_{IH2}	0.8 V_{DD}		V_{DD}	V	
Input high voltage, ports 12-14	V_{IH3}	0.7 V_{DD}		12	V	(Note 1)
Input high voltage X1, X2	V_{IH4}	$V_{DD} - 0.5$		V_{DD}	V	
Input low voltage except X1, X2, TI0, TI1, ports 0, 1, and RESET	V_{IL1}	0		0.3 V_{DD}	V	
Input low voltage ports 0, 1, TI0, TI1, and RESET	V_{IL2}	0		0.2	V	
Input low voltage X1, X2	V_{IL3}	0		0.4	V	
Input leakage current high, except X1, X2	I_{LIH1}			3	μA	$V_I = V_{DD}$
Input leakage current high, X1, X2	I_{LIH2}			20	μA	$V_I = V_{DD}$
Input leakage current low, except X1, X2	I_{LIL1}			−3	μA	$V_I = 0$ V
Input leakage current low, X1, X2	I_{LIL2}			−20	μA	$V_I = 0$ V
Output voltage, high	V_{OH}	$V_{DD} - 1.0$			V	$V_{DD} = 4.5$ to 6.0 V; $I_{OH} = -1$ mA
		$V_{DD} - 0.5$			V	$I_{OH} = -100$ μA
Output voltage, low Ports 0, 2-9 Ports 12-14	V_{OL}			2.0	V	$V_{DD} = 4.5$ to 6.0 V $I_{OL} = 15$ mA $I_{OL} = 10$ mA
Output voltage, low	V_{OL}			0.4	V	$V_{DD} = 4.5$ to 6.0 V; $I_{OL} = -1.6$ mA
				0.5	V	$I_{OH} = 400$ μA
Output leakage current, high	I_{LOH}			3	μA	$V_O = V_{DD}$
Output leakage current, low	I_{LOL}			−3	μA	$V_O = 0$ V
Supply current	I_{DD1}		3.5		mA	$V_{DD} = 5$ V + 10% (Note 2, 3, 4)
			0.9		mA	$V_{DD} = 3$ V + 10% (Note 2, 3, 5)
Supply current HALT mode	I_{DD2}		600		μA	$V_{DD} = 5$ V + 10% (Note 2, 3, 5)
			150		μA	$V_{DD} = 3$ V + 10% (Note 2, 3, 5)
Supply current, STOP mode	I_{DD3}		0.1	10	μA	(Note 2)
Pull-up resistance, ports 12-14	R_L	15	35	55	kΩ	

Notes:

(1) No internal pull-up resistor. If an internal pull-up resistor is used, then same as V_{I1}. If an input voltage greater than 10 V is supplied to port 12, 13, or 14, the pull-up resistor must be > 50 kΩ.

(2) Does not account for current drawn through the mask option pull-up resistor, the mask option power-on reset circuit, or the comparator circuit.

(3) 4.19-MHz crystal oscillation; C1 = C2 = 10 pF.

(4) Set PCC to 0011B for high-speed operation.

(5) Set PCC to 0000B for low-speed operation.

Crystal Characteristics

$T_A = -40$ to $+85°C$; $V_{DD} = 2.7$ to 6.0 V

Type	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
Ceramic oscillator	Frequency (fXX)	2.0		5.0	MHz	
	Oscillation			4	ms	$V_{DD} = 4.5$ to 6.0 V
	Stabilization (1)			20	ms	
Crystal oscillator	Frequency (fXX)	2.0	4.19	5.0	MHz	
	Oscillation			5	ms	$V_{DD} = 4.5$ to 6.0 V
	Stabilization (1)			25	ms	
External clock	Input frequency	2.0		5.0	MHz	
	High/low level duration (txH, txL)	100		250	ns	

Note:

(1) Time required for oscillator to stabilize after power-on or release of STOP mode.

AC Characteristics

$T_A = -40$ to $+85°C$, $V_{DD} = 2.7$ to 6.0 V, GND = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Cycle time (Note 1)	t_{CY}	0.95		32	μs	$V_{DD} = 4.5$ to 6.0 V
		3.85		32	μs	
TI input frequency	f_{TI}	0		1	MHz	$V_{DD} = 4.5$ to 6.0 V
		0		550	kHz	
TI high time	t_{TIH}	0.48			μs	$V_{DD} = 4.5$ to 6.0 V
TI low time	t_{TIL}	1.8			μs	
$\overline{SCK}$ cycle time	t_{KCY}	0.8			μs	Input; $V_{DD} = 4.5$ to 6.0 V
		0.95			μs	Output; $V_{DD} = 4.5$ to 6.0 V
		3.2			μs	Input
		3.8			μs	Output
$\overline{SCK}$ pulse width	t_{KH}, t_{KL}	0.4			μs	Input; $V_{DD} = 4.5$ to 6.0 V
		$(t_{KCY}/2) - 50$			ns	Output; $V_{DD} = 4.5$ to 6.0 V
		1.6			μs	Input
		$(t_{KCY}/2) - 50$			ns	Output
$\overline{SI}$ setup time to $\overline{SCK}$ high	t_{SIK}	100			ns	
$\overline{SI}$ hold time from $\overline{SCK}$ high	t_{KSL}	500			ns	
$\overline{SCK}$ low to SO valid delay time	t_{KSO}			300	ns	$V_{DD} = 4.5$ to 6.0 V
				1000	ns	
INT0 pulse width	t_{INTH}, t_{INTL}	5			μs	
$\overline{RESET}$ pulse width	t_{RSL}	5			μs	

Note:

(1) Cycle time depends on the supply voltage as shown in figure 3.

Power-On Reset Characteristics (Mask Option)

T_A = −40 to +85 °C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Power-on reset circuit operation voltage				0.5	V	
Power-on reset circuit operation voltage rise time		10			μs	
Power-on reset circuit consumption current			30	100	μA	

Comparator Characteristics

T_A = −40 to +85 °C, V_{DD} = 4.5 to 6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Comparision accuracy	V_{ACOMP}			±100	mV	
Threshold voltage	V_{TH}	0		V_{DD}	V	
PTH input voltage	V_{IPTH}	0		V_{DD}	V	
Comparator consumption current			1		mA	Set PTHM7 to 1

Table 2. Oscillation Stable Wait Times

BTM3	BTM2	BTM1	BTM0	Wait Time (f_{XX} = 4.19 MHz)
-	0	0	0	$2^{20}/f_{XX}$ (approx 250 ms)
-	0	1	1	$2^{17}/f_{XX}$ (approx 31.3 ms)
-	1	0	1	$2^{15}/f_{XX}$ (approx 7.82 ms)
-	1	1	1	$2^{13}/f_{XX}$ (approx 1.95 ms)

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

T_A = −40 to +85 °C

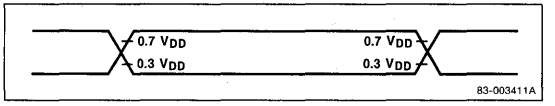
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention supply voltage	V_{DDDR}	2.0		6.0	V	
Data retention supply current	I_{DDDR}		0.1	10	μA	V_{DDDR} = 2.0 V
Release signal set time	t_{SREL}	0			μs	
Oscillation stable wait time	t_{WAIT}		$2^{17}/f_X$		ms	When released by $\overline{\text{RESET}}$ (Note 1)
			See table 2.		ms	When released by interrupt request

Note:

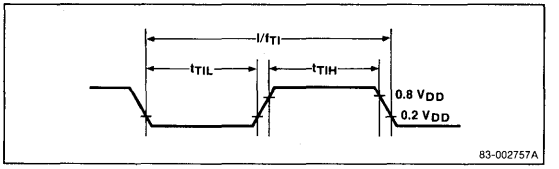
(1) During oscillation stable wait time, CPU operation must be stopped to avoid unstable operation upon oscillation start.

Timing Waveforms

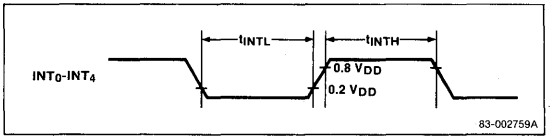
Timing Measurement Points (Except Ports 0, 1, TI1, X1, X2, $\overline{RESET}$)



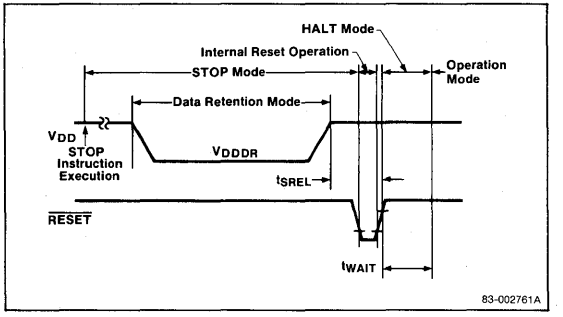
TI Timing



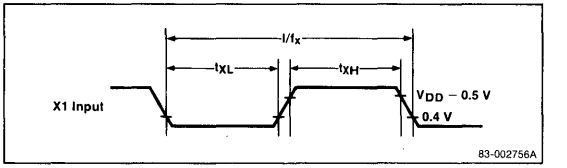
Interrupt Input Timing



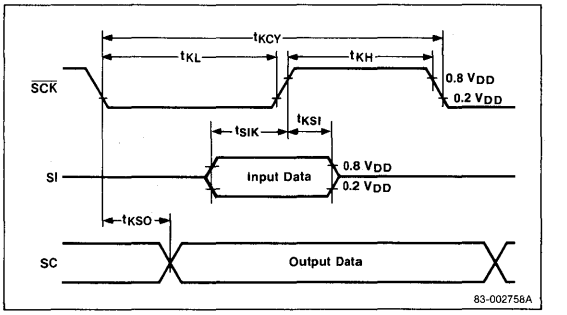
Data Retention Timing (STOP Mode is Released by $\overline{RESET}$)



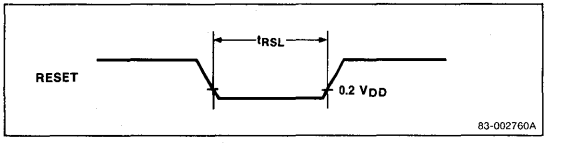
Clock Timing



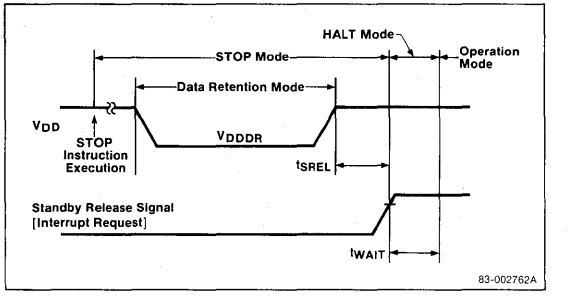
Serial Interface Timing



Reset Input Timing



Data Retention Timing (STOP Mode is Released by Interrupt Request)



NEC

NEC Electronics Inc.

μPD75P108
4-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH ON-CHIP EPROM

PRELIMINARY INFORMATION

Description

The μPD75P108 is a high-performance, single-chip CMOS microcomputer that incorporates a CPU, ROM, RAM, I/O ports, vector interrupt functions, serial interface, and timer/event counters.

The device is functionally equivalent and pin-compatible with the μPD75104/μPD75106/μPD75108. The EPROM in the μPD75P108 allows you to evaluate your program before placing the mask order. An OTP ROM version is available for small production runs.

Features

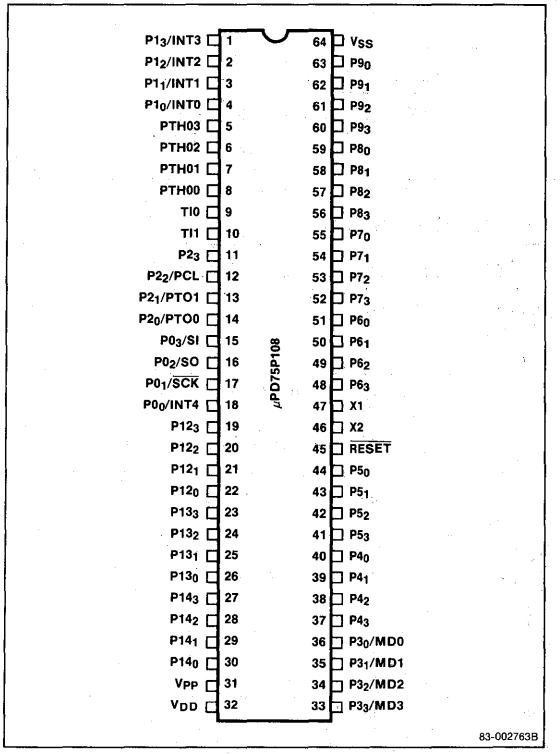
- ☐ 46 instructions
  - — Bit manipulation instructions
  - — 8-bit data transfer, comparison, and increment/decrement instructions
  - — 1-byte relative branch instructions
  - — GETI instruction that realizes 2-or 3-byte instructions in 1-byte units
- ☐ Instruction cycles
  - — High-speed cycle: 0.95 μs/4.19 MHz, $V_{DD} = 5$ V
  - — Low-voltage cycle: 1.91 μs/4.19 MHz, 15.3 μs/4.19 MHz
- ☐ Program memory (EPROM): 8192 x 8 bits
- ☐ Data memory (RAM): 512 x 4 bits
- ☐ Bit manipulation memory (bit-sequential buffer): 16 bits
- ☐ Four banks of 8 x 4-bit general-purpose registers
- ☐ Accumulators
  - — Bit accumulator (CY)
  - — 4-Bit accumulator (A)
  - — 8-Bit accumulator (XA)
- ☐ 58 I/O lines
  - — High-current output ports that can directly drive LEDs (total of 200 mA for 32 pins)
  - — 12 N-channel open-drain outputs with 12 V maximum
  - — Four programmable comparator threshold inputs
  - — Two external event inputs
- ☐ Vectored interrupt function capable of multiple interrupts
  - — Three external vectored interrupts
  - — Two external test inputs
  - — Four internal vectored interrupts
- ☐ Two 8-bit timer/event counters
- ☐ 8-bit serial interface
  - — Data transfer can start with LSB or MSB
  - — Two transfer modes (transmit/receive and receive-only)
- ☐ Power-on reset circuit
- ☐ Crystal or ceramic oscillator
- ☐ Standby modes (STOP/HALT)
- ☐ CMOS technology
- ☐ Low power consumption

Ordering Information

Part Number	Package Type	ROM (8K x 8)
μPD75P108DW	64-pin shrink cerdip with window	EPROM
μPD75P108CW	64-pin plastic shrink DIP	OTP ROM
μPD75P108G-1B	64-pin plastic miniflat	OTP ROM

Pin Configurations

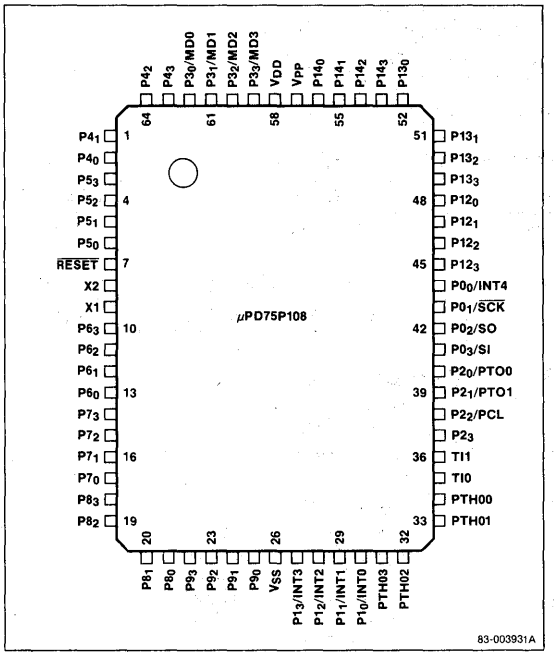
64-Pin Ceramic Shrink DIP or Shrink Cerdip with Window



3

Pin Configurations (cont)

64-Pin Plastic Miniflat



Pin Identification

Symbol	Function
$P1_3$/INT3 $P1_2$/INT2 $P1_1$/INT1 $P1_0$/INT0	4-bit input port 1/Edge-triggered vectored interrupts
PTH03-PTH00	Programmable threshold comparator analog input port
TI0, TI1	External event input for timer/event counter
$P2_3$, $P2_2$/PCL $P2_1$/PTO1 $P2_0$/PTO0	4-bit I/O port 2/Clock output terminal/Timer/event counter output pins
$P0_3$/SI $P0_2$/SO $P0_1$/SCK $P0_0$/INT4	4-bit input port 0/Serial interface/Edge-triggered vectored interrupt
$P12_3$-$P12_0$	4-bit I/O port 12
$P13_3$-$P13_0$	4-bit I/O port 13
$P14_3$-$P14_0$	4-bit I/O port 14
V_{PP}	EPROM programming power supply
V_{DD}	Positive power supply
$P3_3$/MD3 $P3_2$/MD2 $P3_1$/MD1 $P3_0$/MD0	Programmable 4-bit I/O port 3/EPROM function mode selection inputs

Symbol	Function
$P4_3$-$P4_0$	4-bit I/O port 4
$P5_3$-$P5_0$	4-bit I/O port 5
RESET	Reset input
X2, X1	Ceramic or crystal system clock oscillator
$P6_3$-$P6_0$	Programmable 4-bit I/O port 6
$P7_3$-$P7_0$	4-bit I/O port 7
$P8_3$-$P8_0$	4-bit I/O port 8
$P9_3$-$P9_0$	4-bit I/O port 9
V_{SS}	Ground

Pin Functions

$P0_0$/INT4, $P0_1$/SCK, $P0_2$/SO, $P0_3$/SI [Port 0, Interrupt, Serial Clock, Serial Interface]

This port can be configured as a 4-bit parallel input port or as the serial I/O interface under control of the serial mode select register. The serial input SI, serial output SO, and the serial clock SCK make up the serial I/O interface. INT4 is an edge-triggered vectored interrupt triggered by a rising or falling edge. The port is in the input state at reset.

$P1_3$/INT3, $P1_2$/INT2, $P1_1$/INT1, $P1_0$/INT0 [Port 1, Edge-Triggered Interrupts]

4-bit input port 1/interrupts. INT0 and INT1 are edge-triggered vectored interrupts selected by a rising or falling edge. INT2 and INT3 are triggered by a rising edge only. The port and the interrupts are in the input state at reset.

$P2_3$, $P2_2$/PCL, $P2_1$/PTO1, $P2_0$/PTO0 [Port 2, Clock Output, Timer/Event Counter Output]

Port 2 is a 4-bit I/O port for directly driving LEDs. PTO1 and PTO0 are the timer/event counter output pins. PCL is the clock output pin. These pins are in the input state at reset.

$P3_3$/MD3, $P3_2$/MD2, $P3_1$/MD1, $P3_0$/MD0 [Port 3, EPROM Function Mode Inputs]

Programmable 4-bit I/O port for directly driving LEDs with bit-level I/O selection. MD0-MD3 select the EPROM operating mode. The port is in the input state at reset.

$P4_3$-$P4_0$ [Port 4]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 5.

Pin Functions (cont)

$P5_3$-$P5_0$ [Port 5]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 4.

$P6_3$-$P6_0$ [Port 6]

Programmable 4-bit I/O port for directly driving LEDs with bit-level I/O selection. The port is in the input state at reset and has 8-bit I/O capability when paired with port 7.

$P7_3$-$P7_0$ [Port 7]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 6.

$P8_3$-$P8_0$ [Port 8]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 9.

$P9_3$-$P9_0$ [Port 9]

4-bit I/O port for directly driving LEDs. The port is in the input state at reset and has 8-bit I/O capability when paired with port 8.

$P12_3$-$P12_0$ [Port 12]

4-bit I/O port, N-channel, open-drain (12 V max). The port is in the high-impedance state at reset and has 8-bit I/O capability when paired with port 13.

$P13_3$-$P13_0$ [Port 13]

4-bit I/O port, N-channel, open-drain (12 V max). The port is in the high-impedance state at reset and has 8-bit I/O capability when paired with port 12.

$P14_3$-$P14_0$ [Port 14]

4-bit I/O port, N-channel, open-drain (12 V max). The port is in the high-impedance state at reset.

PTH03-PTH00 [Threshold Detector Analog Input Port]

Threshold detector analog input port.

TI0, TI1 [Timer/Event Counter Input]

External event input for the timer/event counter. These two pins are also an edge-triggered vectored interrupt and a 1-bit input port.

$\overline{RESET}$ [Reset]

System reset input pin (active low).

X2, X1 [System Clock I/O]

These pins are the system clock I/O. The clock may be ceramic or crystal.

V_{DD} [Power Supply]

Positive power supply.

V_{PP} [EPROM Programming Power Supply]

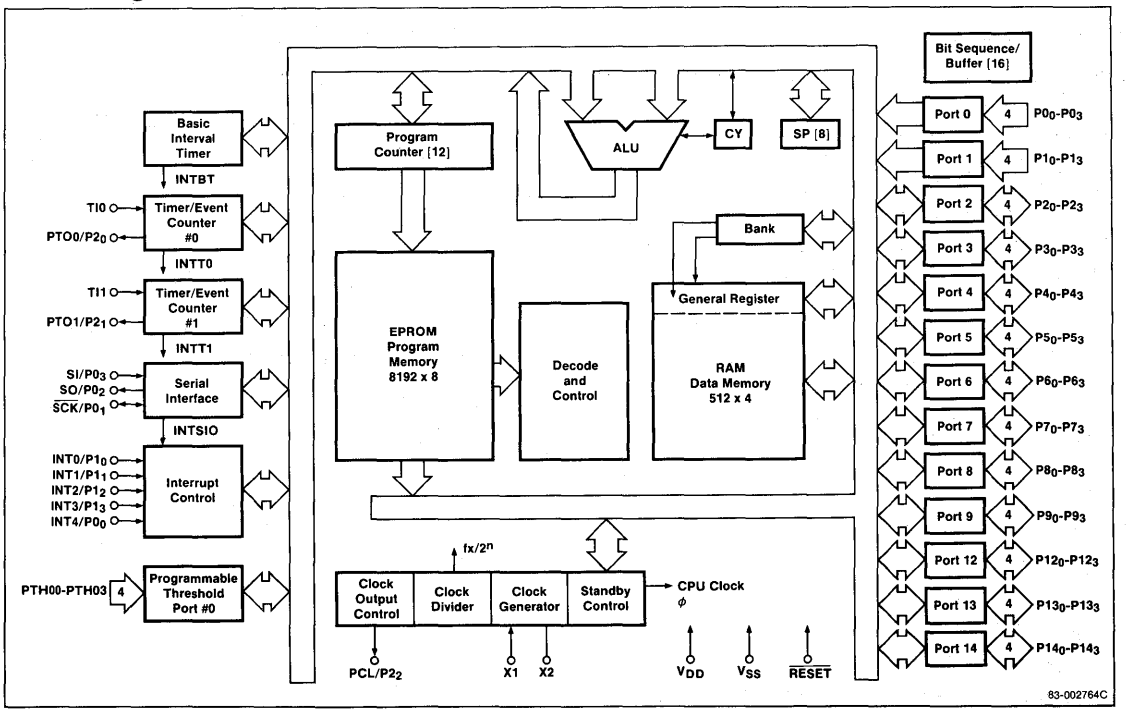
During normal operation, connect to V_{DD}. Connect to +21 V for EPROM programming.

V_{SS} [Ground]

System ground.

3

Block Diagram



μPD75000 Series

Table 1 compares the features of similar products in the μPD75000 series.

Table 1. Product Comparison

Item	μPD75P108	μPD75104	μPD75106	μPD75108
Program memory	EPROM 0000-1FFFH	Mask ROM 0000-0FFFH	Mask ROM 0000-177FH	Mask ROM 0000-1FFFH
Data memory	512 x 4-bit Bank 0: 256 Bank 1: 256	320 x 4-bit Bank 0: 256 Bank 1: 64	320 x 4-bit Bank 0: 256 Bank 1: 64	512 x 4-bit Bank 0: 256 Bank 1: 256
Instruction set	Set P108	Set P108 minus BR!addr (3-byte instr.)	Set P108	Set P108
Ports 12-14 pull-up resistor	Not offered	Mask option	Mask option	Mask option
Power-on reset	Integrated	Mask option	Mask option	Mask option
Power-on flag	Integrated	Mask option	Mask option	Mask option
Operating voltage	5 V ±10%	2.5 to 6.0 V	2.5 to 6.0 V	2.5 to 6.0 V
Pin 31	V_{PP}	NC	NC	NC
Packaging	64-pin ceramic shrink DIP or plastic miniflat	64-pin plastic miniflat or shrink DIP	64-pin plastic miniflat or shrink DIP	64-pin plastic miniflat or shrink DIP

EPROM Programming

The internal 8K-byte EPROM is programmed via the pins and functions listed in table 2. Refer to the flowchart, figure 1.

The V_{PP} and V_{DD} pins must be held at 5 V for at least 10 μs upon power-up and before the programming voltages of 21 V to V_{PP} and 6 V to V_{DD} are applied.

Mode pins MD_0-MD_3 control the programming steps as shown in table 3. Address inputs are not used during programming. The program memory address is first cleared via the mode pins, then incremented by applying four clock pulses to the X1 input.

Table 2. EPROM Access

Pin	Function
V_{PP}	Programming voltage. Connect to 21 V when programming EPROM.
X1, X2	Address increment clock input. X2 inputs the inverse of X1.
MD_0-MD_3	Mode selection
$P4_0$-$P4_3$	8-bit data bus connection, low
$P5_0$-$P5_3$	8-bit data bus connection, high
V_{DD}	Connect to 6 V during programming.

Table 3. EPROM Mode Selection

V_{PP} = 21 V, V_{DD} = 6.0 V

MD0	MD1	MD2	MD3	Operating Mode
H	L	H	L	Program memory address clear
L	H	H	H	Program memory write
L	L	H	H	Program verify
H	X	H	H	Program inhibit

I/O Port Interfaces

Figure 2 shows the internal circuit configurations at the I/O ports.

Figure 1. EPROM Programming Flowchart

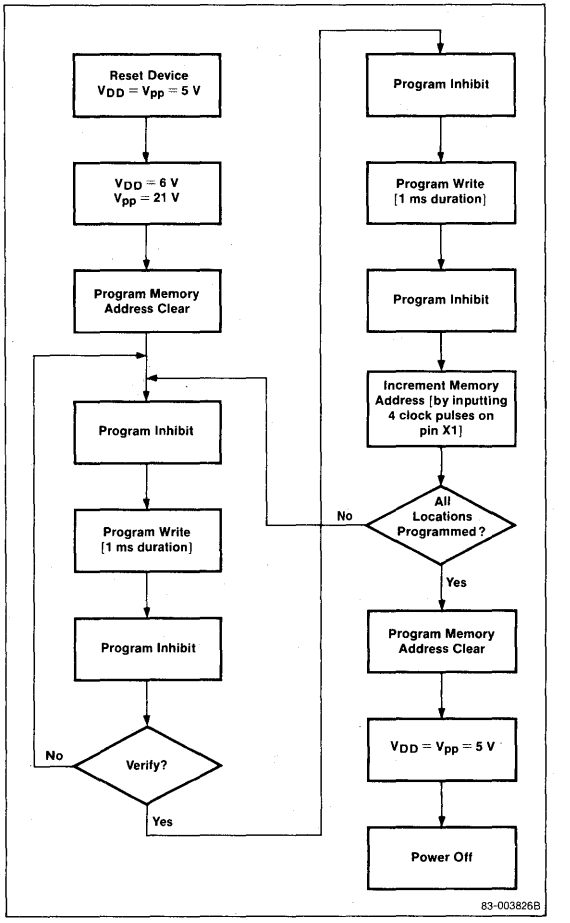
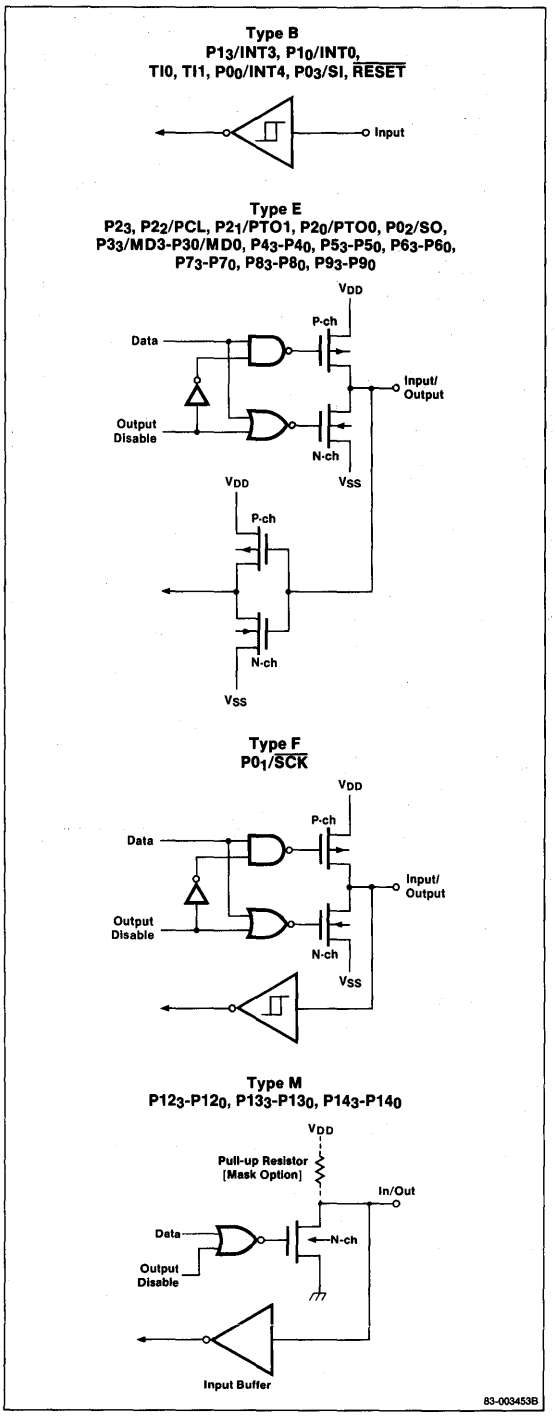


Figure 2. Interface at Input/Output Ports



8-BIT, SINGLE-CHIP MICROCOMPUTERS

Section 4 — 8-Bit, Single-Chip Microcomputers

μPD78C05A/06A
HIGH-END, 8-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

Description

The μPD78C05A and μPD78C06A are advanced CMOS 8-bit general purpose, single-chip microcomputers intended for applications requiring 8-bit microprocessor control and extremely low power consumption. They are ideally suited for portable, battery-powered/backed-up products. Subsets of the μPD7801, the μPD78C05A/06A integrate an 8-bit ALU, 4K-byte ROM, 128-byte RAM, 46 I/O lines, an 8-bit timer, and a serial I/O port on a single die. Expanded system operation can easily be implemented using industry standard peripheral and memory components. Total memory space can be increased to 64K bytes.

The μPD78C05A/06A lend themselves well to low-power, portable applications by featuring two power-down modes to further conserve power when the processor is not active. The μPD78C06A is packaged in a 64-pin plastic miniflat package. The μPD78C05A is a ROM-less version, packaged in a 64-pin QUIP, and designed for prototype development and small volume production.

Features

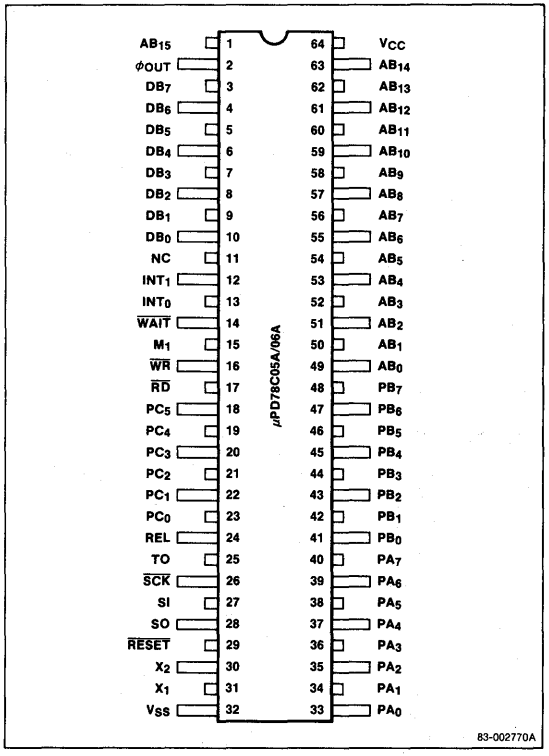
- ☐ CMOS silicon gate technology; +5 V supply
- ☐ Complete single-chip microcomputer
  - —8-bit ALU
  - —4K-byte ROM
  - —128-byte RAM
- ☐ 6.25 MHz
- ☐ Low power consumption
- ☐ 46 I/O lines
- ☐ Expansion capabilities
  - —60K-byte external memory address range
  - —8080A bus compatible
- ☐ Serial I/O port
- ☐ 101 instructions with multiple address modes
- ☐ Power-down modes
  - —Halt mode
  - —Stop mode
- ☐ 8-bit timer
- ☐ Prioritized interrupt structure
  - —Two external
  - —One internal
- ☐ On-chip clock generator
- ☐ ROM-less version available (78C05A)

Ordering Information

Part Number	Package Type
μPD78C05AG-36	64-pin plastic QUIP
μPD78C06AG-12	64-pin plastic miniflat

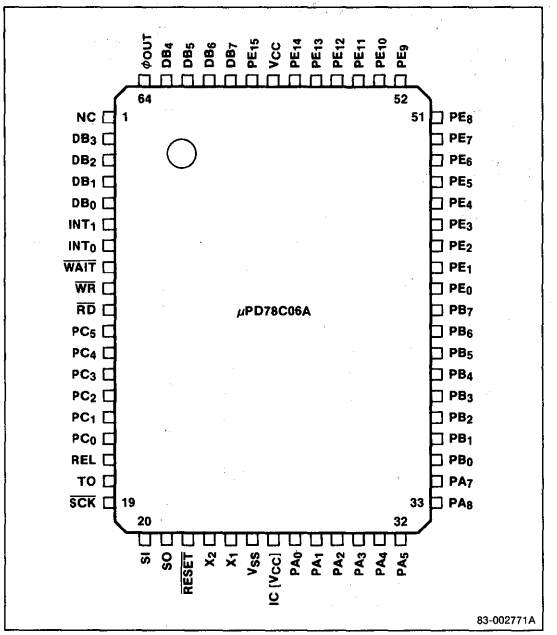
Pin Configurations

64-Pin Plastic QUIP



Pin Configurations (cont)

64-Pin Plastic Miniflat



Pin Identification

Plastic QUIP

No.	Symbol	Function
1	PE_{15} (78C06A) AB_{15}(78C05A)	Address bus/output port E, bit 15 Address bus, bit 15
2	ϕ_{OUT}	Clock output
3-10	DB_7-DB_0	Bidirectional data bus
11	NC	Not connected
12, 13	INT_1, INT_0	Interrupt inputs 1 and 0
14	$\overline{WAIT}$	Wait request input
15	M_1	Machine cycle 1 output
16	$\overline{WR}$	Write strobe output
17	$\overline{RD}$	Read strobe output
18-23	PC_5-PC_0	Input port C
24	REL	STOP release input
25	TO	Timer output
26	$\overline{SCK}$	Serial clock input/output

Plastic QUIP (cont.)

No.	Symbol	Function
27	SI	Serial data input
28	SO	Serial data output
29	$\overline{RESET}$	Reset input
30, 31	X_2, X_1	Crystal connections
32	V_{SS}	Ground potential
33-40	PA_0-PA_7	I/O port A, bits 0-7
41-48	PB_0-PB_7	I/O port B, bits 0-7
49-63	PE_0-PE_{14} (78C06A) AB_0-AB_{14} (78C05A)	Address bus/output port E, bits 0-14 Address bus, bits 0-14
64	V_{CC}	Power supply

Plastic Miniflat

No.	Symbol	Function
1	NC	Not connected
2-5	DB_3-DB_0	Bidirectional data bus, bits 3-0
6, 7	INT_1, INT_0	Interrupt inputs 1 and 0
8	$\overline{WAIT}$	Wait request input
9	$\overline{WR}$	Write strobe output
10	$\overline{RD}$	Read strobe output
11-16	PC_5-PC_0	Input port C
17	REL	STOP release input
18	TO	Timer output
19	$\overline{SCK}$	Serial clock input/output
20	SI	Serial data input
21	SO	Serial data output
22	$\overline{RESET}$	Reset input
23, 24	X_2, X_1	Crystal connections
25	V_{SS}	Ground potential
26	IC (V_{CC})	Internally conected to V_{CC}
27-34	PA_0-PA_7	I/O port A, bits 0-7
35-42	PB_0-PB_7	I/O port B, bits 0-7
43-57	PE_0-PE_{14}	Address bus/output port E, bits 0-14
58	V_{CC}	Power supply
59	PE_{15}	Address bus/output port E, bit 15
60-63	DB_7-DB_4	Bidirectional data bus, bits 7-4
64	ϕ_{OUT}	Clock output

Pin Functions

DB_0-DB_7 [Data Bus]

The 8-bit bidirectional data bus transfers data between the accumulator and external memory or memory-mapped I/O.

INT_0, INT_1 [Interrupts 0 and 1]

INT_0 is a rising-edge-triggered external interrupt input. INT_1 is an active-high external interrupt input. Both inputs must be held high for a least 2 μs to be recognized as valid.

$\overline{WAIT}$ [Wait Request]

The $\overline{WAIT}$ input is used to interface with slow memories or peripherals. $\overline{WAIT}$ is sampled at the end of machine cycle T_2. If it is low, then the processor goes into a wait state until $\overline{WAIT}$ returns high.

M_1 [Machine Cycle 1]

(78C05A only) The M_1 output is high during machine cycles T_1 through T_3 of the first opcode fetch of an instruction.

$\overline{WR}$ [Write Strobe]

When the $\overline{WR}$ output is low, valid output data is available on the data bus.

$\overline{RD}$ [Read Strobe]

The processor loads data from the data bus into the accumulator on the rising edge of the $\overline{RD}$ output.

PC_0-PC_5 [Port C]

The 6-bit input port has internal pull-up resistors. When contents of the port buffer are transferred to the accumulator, they fill the least significant six bits.

REL [STOP Release]

The STOP release input has an internal pull-down resistor. High level on REL releases the processor from stop mode, allowing the clock generator to restart.

TO [Timer Output]

Frequency of square wave output at TO is determined by the timer register contents. TO outputs a low level after reset.

$\overline{SCK}$ [Serial Clock]

The control clock for the serial data port is user-programmable as an input or output.

SI [Serial Data Input]

The SI input loads into the serial register on the rising edge of SCK.

SO [Serial Data Output]

On the falling edge of SCK, the serial register outputs data to SO, most significant bit first.

$\overline{RESET}$ [Reset]

A low level on $\overline{RESET}$ input of more than 8 μs resets the processor.

X_1, X_2 [Crystal Connections]

These pins connect to the internal clock generator circuit. If an external clock generator is used, then it is connected to X_1.

V_{SS} [Ground]

This is the power supply ground potential input.

IC [V_{CC}]

(78C06A only) This is the internal connection to V_{CC} through a high impedance. It should be left open.

PA_0-PA_7 [Port A]

Port A is an 8-bit latched output port. Data can be readily transferred between the accumulator and the output latch buffers. The contents of the output latches can be modified using arithmetic and logic instructions. Data remains latched at port A unless it is acted on by another port A instruction or a RESET is issued.

PB_0-PB_7 [Port B]

Port B is an 8-bit I/O port. Data is latched at port B in both the input and output modes. Each bit of port B can be independently set to either input or output mode. The mode B register programs the individual lines of port B to be either an input (mode $B_n = 1$) or an output (mode $B_n = 0$).

PE_0-PE_{15} [Port E]

(78C06A only) Port E is a 16-bit address bus/output port. It can be set to one of two operating modes using the PER or PEX instruction.

- 16-bit address bus: the PER instruction sets this mode for use with external I/O or memory expansion (up to 60K bytes, externally).
- 16-bit output port: the PEX instruction sets port E to a 16-bit output port. The contents of B and C registers appear on PE_8-PE_{15} and PE_0-PE_7, respectively.

AB_0-AB_{15} [Address Bus]

These lines are the 16-bit address bus to the main memory. The 78C05A, having no internal ROM, must address the area from 0 to 4096 as external ROM.

The 78C05A AB lines are unlike the 78C06A PE lines in that they have no internal latches. When the Port E output instruction PEX is executed in a 78C05A, the register pair BC is output to the AB lines for only one clock cycle during the third machine cycle. This is provided to allow external hardware to emulate the Port E operation of the 78C06A.

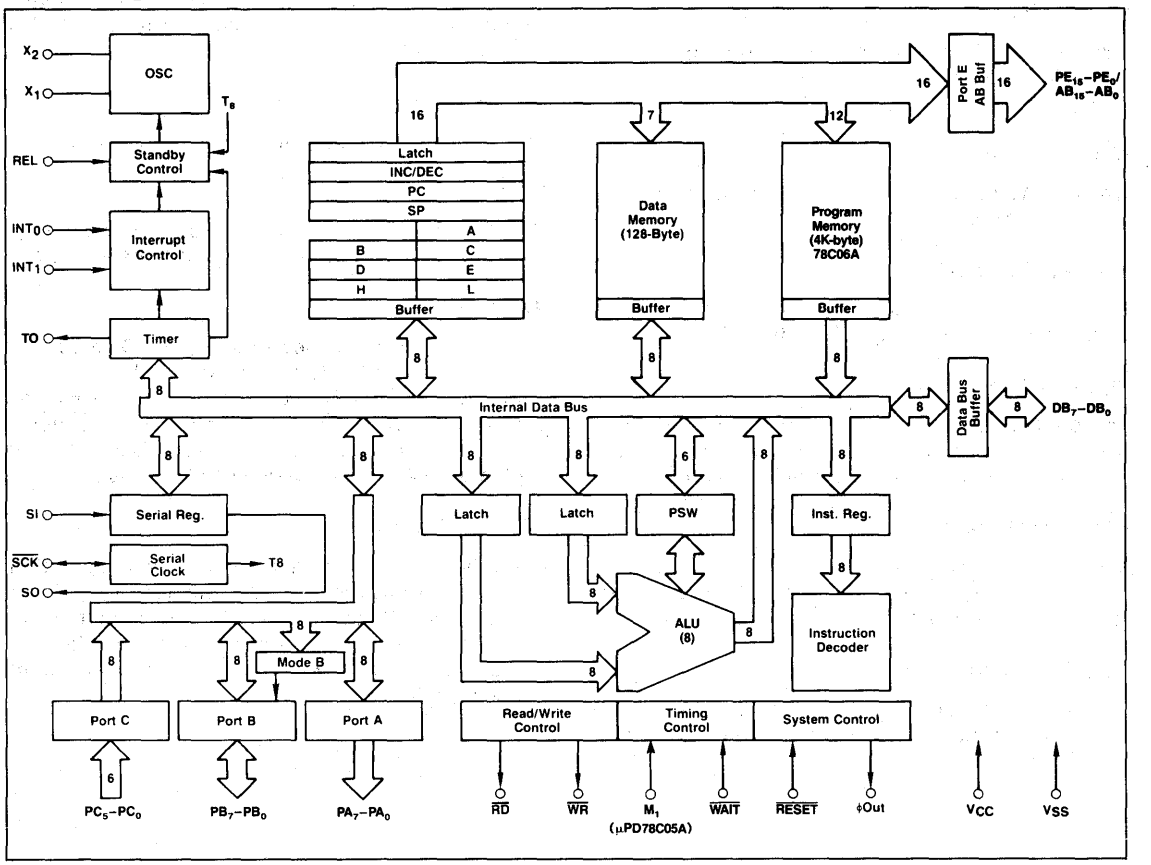
V_{CC} [Power Supply]

This pin is the power supply input, 3.5 to 6.0 V during normal operation.

ϕ OUT [Clock Output]

The system clock frequency, which is 1/4 or 1/8 of the crystal frequency, is output on this pin. ϕ OUT is active in halt mode but is held high in stop mode.

Block Diagram



Absolute Maximum Ratings

Supply voltage, V_{CC}	−0.3 to +7.0 V
Input voltage, V_I	−0.3 V to V_{CC} + 0.3 V
Output voltage, V_O	−0.3 V to V_{CC} + 0.3 V
Output high current, I_{OH} (device total)	−5 mA
Output low current, I_{OL} (device total)	43.5 mA
Operating temperature, T_{OPR}	−40 to +85 °C
Storage temperature, T_{STG}	−65 to +150 °C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = +25 °C; V_{CC} = GND = 0 V

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input capacitance	C_I			15	pF	f_c = 1 MHz; unmeasured pins returned to 0 V
Output capacitance	C_O			15	pF	
I/O capacitance	$C_{I/O}$			15	pF	

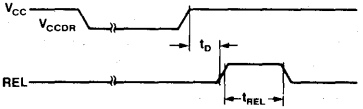
Low-Power Data Memory Retention in Stop Mode

T_A = −40 to + 85 °C

		Limits				Test
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Data retention voltage	V_{CCDR}	2.0			V	
Data retention supply current	I_{CCDR}		0.8	20	μA	V_{CCDR} = 2.0 V, (X_1 = 0 V, X_2 = open)
Data retention input low RESET voltage	V_{ILDR}	0		0.2 V_{CCDR}		
Data retention input high RESET voltage	V_{IHDR}	0.8 V_{CCDR}		V_{CCDR}	V	
REL input delay time	t_D	500			μs	
REL Input high time	t_{REL}	10			μs	

Note:

(1) In data retention mode, input voltages to $\overline{WAIT}$ and PC_0-PC_5 pins (with pull-up resistors) should be maintained the same as V_{CCDR} level; other input voltages should be kept less than V_{CCDR} level.



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DC Characteristics

$T_A = -40$ to $+85°C$; $V_{CC} = +5\ V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input high voltage	V_{IH1}	0.7 V_{CC}		V_{CC}	V	$\overline{INT_0}$, $\overline{INT_1}$, $\overline{WAIT}$, PB_0-PB_7, PC_0-PC_5
	V_{IH2}	0.75 V_{CC}			V	$\overline{RESET}$, $\overline{SCK}$, REL, SI
	V_{IH3}	$V_{CC} - 2.0$		V_{CC}	V	DB_0-DB_7
	V_{IH4}	$V_{CC} - 0.5$		V_{CC}	V	X_1
Input low voltage	V_{IL1}	0		0.3 V_{CC}	V	$\overline{INT_0}$-$\overline{INT_1}$, $\overline{WAIT}$, PB_0-PB_7, PC_0-PC_5
	V_{IL2}	0		0.25 V_{CC}	V	$\overline{RESET}$, $\overline{SCK}$, REL, SI
	V_{IL3}	0		0.8	V	DB_0-DB_7
	$V_{IL}4$	0		0.5	V	X_1
Output high voltage	V_{OH1}	2.4			V	$I_{OH} = -100\ \mu A$
	V_{OH2}	$V_{CC}- 0.5$			V	$I_{OH} = -50\ \mu A$
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 1.8$ mA
Input high current	I_{IH1}	7		100	μA	$V_{IN} = V_{CC}$ (REL)
	I_{IH2}			45	μA	$V_{IN} = V_{CC}$ (X_1)
Input low current	I_{IL1}	−7		−100	μA	$V_{IN} = 0$ V (WAIT, PC_0-PC_5)
	I_{IL2}			−45	μA	$V_{IN} = 0$ V (X_1)
Input high leakage current	I_{LIH}			3.2	μA	$V_{IN} = V_{CC}$ (except REL, X_1)
Input low leakage current	I_{LIL1}			−3.2	μA	$V_{IN} = 0$ V (except WAIT, PC_0-PC_5, X_1)
	I_{LIL2}			−3.2	μA	$V_{IN} = 0$ V (Stop mode, X_1)
Output high leakage current	I_{LOH}			3.2	μA	$V_{OUT} = V_{CC}$
Output low leakage current	I_{LOL}			−3.2	μA	$V_{OUT} = 0$ V
V_{CC} supply current	I_{CC1}		4	7.5	mA	Operation mode
	I_{CC2}		1.2	2.7	mA	Halt mode
	I_{CC3}		1	20	μA	Stop mode ($X_1 = 0$ V, X_2 = Open)

AC Characteristics

Read/Write Operation

78C05A, $t_{CY\phi} = 660$ ns; 78C06A, $t_{CY\phi} = 1320$ ns

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{RD}$ low time	t_{RR}	1070 + 660			ns	
$\overline{RD}$ LE to $\overline{WAIT}$ LE	t_{RWT}			460	ns	
Address (PE_0-PE_{15}) to $\overline{WAIT}$ LE	t_{AWTI}			790	ns	
$\overline{WAIT}$ set-up time to ϕ_{OUT} LE	t_{WTS}	370			ns	
$\overline{WAIT}$ hold time after ϕ_{OUT} LE	t_{WTH}	0			ns	
M_1 to $\overline{RD}$ LE (1)	t_{MR}	108			ns	
$\overline{RD}$ TE to M_1 (1)	t_{RM}	130			ns	
ϕ_{OUT} LE to $\overline{WR}$ LE	$t_{\phi W}$			175	ns	
Address (PE_0-PE_{15}) to ϕ_{OUT} TE	$t_{A\phi}$	420			ns	
Address (PE_0-PE_{15}) to ϕ_{OUT} TE (1)	$t_{A\phi}$-	90			ns	
Address (PE_0-PE_{15}) to data output	t_{AD2}	510			ns	
Data output to $\overline{WR}$ TE	t_{DW}	740 + 660N			ns	
$\overline{WR}$ TE to data stable time	t_{WD}	130			ns	
Address (PE_0-PE_{15}) to $\overline{WR}$ LE	t_{AW}	460			ns	
$\overline{WR}$ TE to address stable time	t_{WA}	180			ns	
$\overline{WR}$ low time	t_{WW}	690 + 900N			ns	
$\overline{WR}$ LE to $\overline{WAIT}$ LE	t_{WWT}			110	ns	

Note:

(1) Applies only to 78C05A.

(2) N is number of WAIT states (T_{WAIT}).
In the 78C06A, two WAIT states are automatically inserted when accessing internal ROM.

(3) LE is leading edge and TE is trailing edge.

AC Characteristics (cont)

Bus Timing Depending on $t_{CY\phi}$

$T_A = -40$ to $+85°C$

Symbol	Formula	Min/Max	Unit
$t_{R\phi}$	$(1/2)T - 150$	Min	ns
t_{AD1}	$(3/2 + N)T - 200$	Max	ns
$t_{RA}(T3)$	$(1/2)T - 150$	Min	ns
$t_{RA}(T4)$	$(3/2)T - 150$	Min	ns
t_{RD}	$(1 + N)T - 200$	Max	ns
t_{RR}	$(2 + N)T - 250$	Min	ns
t_{RWT}	$T - 200$	Max	ns
t_{AWTI}	$(3/2)T - 200$	Max	ns
t_{WTS}	$(1/3)T + 150$	Min	ns
t_{MR} (1)	$(3/8)T - 140$	Min	ns
t_{RM} (1)	$(1/2)T - 200$	Min	ns
$t_{A\phi}$ (1)	$(1/2)T - 240$	Min	ns
$t_{A\phi}$	$T - 240$	Min	ns
t_{AD2}	$T - 150$	Min	ns
t_{DW}	$(3/2 + N)T - 250$	Min	ns
t_{WD}	$(1/2)T - 200$	Min	ns
t_{AW}	$T - 200$	Min	ns
t_{WA}	$(1/2)T - 150$	Min	ns
t_{WW}	$(3/2 + N)T - 300$	Min	ns
t_{WWT}	$(1/2)T - 220$	Max	ns
t_{CYK}	$2T$	Min	ns
t_{KKL}	$T - 120$	Min	ns
t_{KKH}	$T - 120$	Min	ns

Note:

(1) For 78C05A only

(2) N = Number of T_{WAIT} states
In the 78C06A, two wait states are automatically inserted when accessing internal ROM.
$T = t_{CY\phi}$ for 78005A
$T = 2t_{CY\phi}$ for 78C06A
t_{CY} assumes 50% duty cycle on X_1.

Serial Operation

78C05A, $t_{CY\phi} = 660$ ns; 78C06A, $t_{CY\phi} = 1320$ ns

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{CYK}	1270 1280		80,000	ns ns	$\overline{SCK}$ input $\overline{SCK}$ output
$\overline{SCK}$ low time	t_{KKL}	515 520			ns ns	$\overline{SCK}$ input $\overline{SCK}$ output
$\overline{SCK}$ high time	t_{KKH}	515 520			ns ns	$\overline{SCK}$ input $\overline{SCK}$ output
SI set-up time to $\overline{SCK}$ TE	t_{SIS}	200			ns	
SI hold time after $\overline{SCK}$ TE	t_{SIH}	250			ns	
$\overline{SCK}$ LE to SO delay time	t_{KO}			300	ns	

Note:

(1) Input timings are measured at V_{IH} min and V_{IL} max.

(2) Output timings are measured at $V_{OH} = 2.4$ V, $V_{OL} = 0.45$ V, and load = one TTL + 200 pF.

(3) LE is leading edge and TE is trailing edge.

Clock Timing

$T_A = -40$ to $+85°C$ $V_{DD} = +5$ V $\pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
X_1 input cycle time	t_{CYX}	160		10,000	ns	
X_1 input low time	t_{XXL}	75			ns	
X_1 input high time	t_{XXH}	75			ns	
ϕ_{OUT} cycle time (2)	$t_{CY\phi}$	1,280		80,000	ns	
ϕ_{OUT} low time (2)	$t_{\phi\phi L}$	515			ns	
ϕ_{OUT} high time (2)	$t_{\phi\phi H}$	515			ns	
ϕ_{OUT} cycle time (1)	$t_{CY\phi}$	640		40,000	ns	
ϕ_{OUT} Low time (1)	$t_{\phi\phi L}$	195			ns	
ϕ_{OUT} high time (1)	$t_{\phi\phi H}$	195			ns	
ϕ_{OUT} rise/ fall time	t_R, t_F			120	ns	

Note:

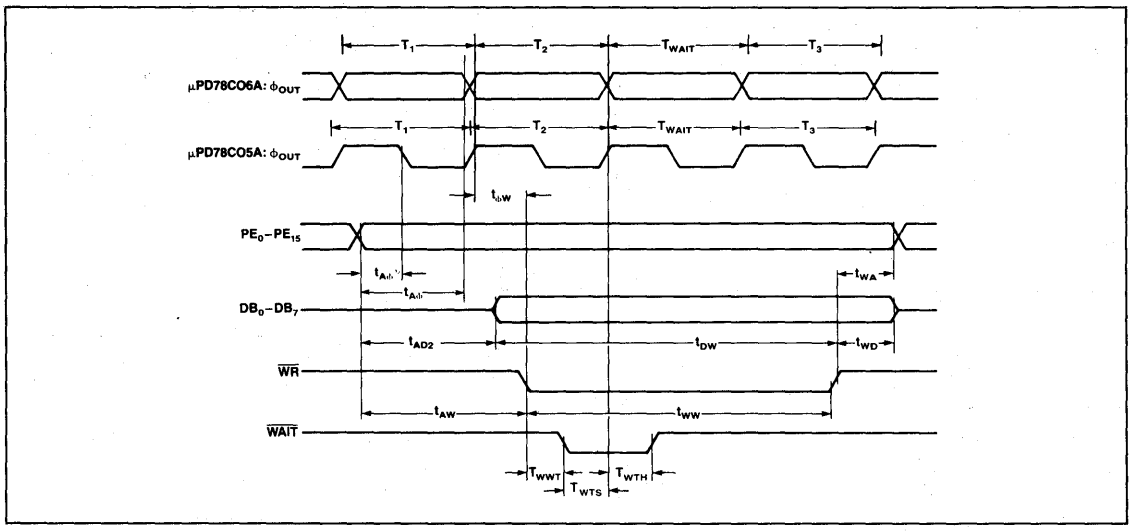
(1) Applies only to 78C05A. ($t_{CY\phi} = 4/f_{OSC}$)

(2) Applies only to 78C06A. ($t_{CY\phi} = 8/f_{OSC}$)

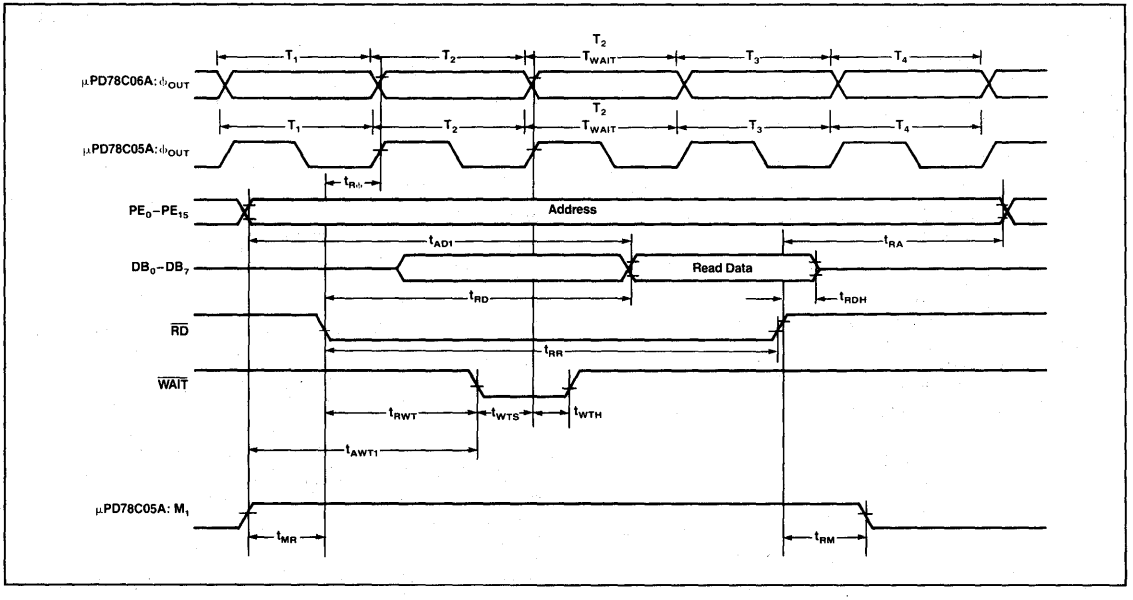
4

Timing Waveforms

Write Operation

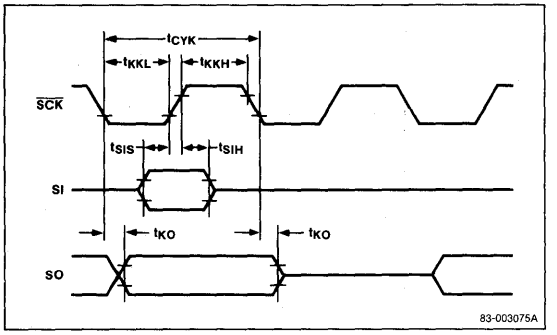


Read Operation

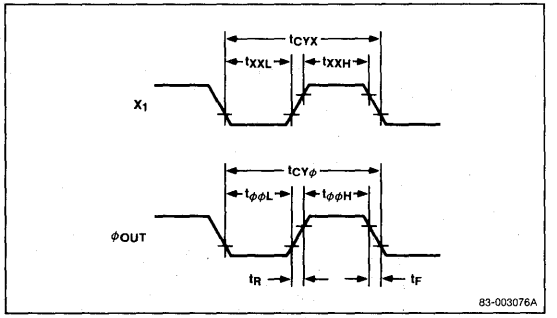


Timing Waveforms (cont)

Serial Operation



Clock Timing



Functional Description

Memory Map

The μPD78C06A can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4,095) and RAM (65,408-65,535), any memory location can be used as either ROM or RAM. Figure 1 defines the 0-64K-byte memory space for the μPD78C06A showing that the reset start address, interrupt start address, call tables, etc, are located in the internal ROM area.

Timer Operation

A programmable 8-bit timer (figure 2) is provided on-chip for measuring time intervals, generating pulses, and general time-related control functions. It is capable of measuring time intervals from 5 μs to 21 ms in duration. The timer consists of a prescaler that decrements an 8-bit counter at a fixed 5-μs or 82-μs rate.

Countup operation is initiated upon execution of the STM instruction. When the contents of the upcounter are incremented and a coincidence with the Timer Reg. occurs, an internal interrupt (INT_T) is generated. The duration of the time-out may be altered by loading new contents into the timer register.

The timer flip-flop is set by the STM instruction and reset on a countup operation. Its output (TO) is available externally and may be used for general external synchronization.

Serial Port Operation

The on-chip serial port (figure 3) provides basic synchronous serial communication functions allowing the μPD78C05A/06A to serially interface with external devices.

Serial transfers are synchronized with either the internal clock or an external clock input ($\overline{SCK}$). The transfer rate is fixed at $f_{OSC}/8$ if the internal clock is used or is variable between dc and $f_{OSC}/8$ when an external clock is used. The clock source select is determined by the serial mode register. Data on the SI (serial input) line is latched into the serial register on each rising edge of the serial clock ($\overline{SCK}$). Concurrently, data is transferred out of the serial register onto the SO (serial output) line with each falling edge of $\overline{SCK}$. At this time, receive and transmit operations through the SI/SO port are enabled. Receive and transmit operations are performed MSB first.

Interrupt Structure

The μPD78C05A/06A provide a maskable interrupt structure capable of handling vectored prioritized interrupts. Interrupts can be generated from three different sources: two external interrupts and a timer interrupt. When activated, each interrupt branches to a designated memory vector location for that interrupt. See table 1.

Table 1. Interrupt Structure

INT	Vectored Memory Location	Priority	Type
INT_T	8	2	Internal, timer overflow
INT_0	4	1	External, level sensitive
INT_1	16	3	External, rising-edge sensitive

4

Figure 1. Memory Map

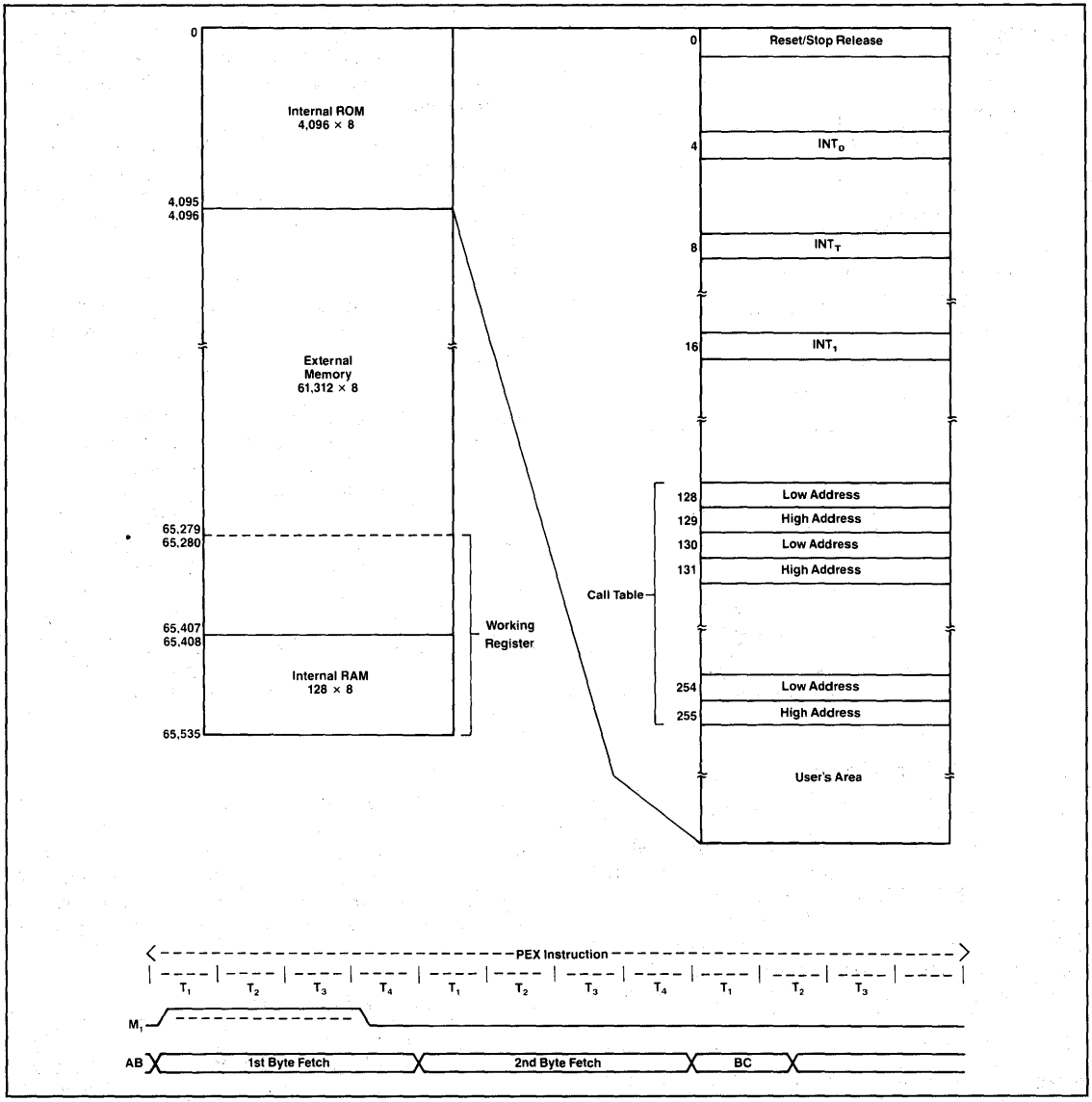


Figure 2. Timer Block Diagram

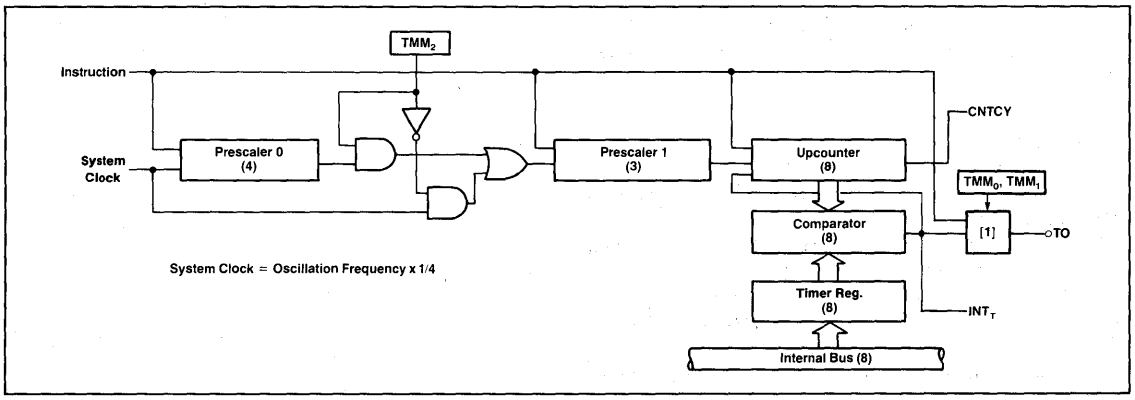
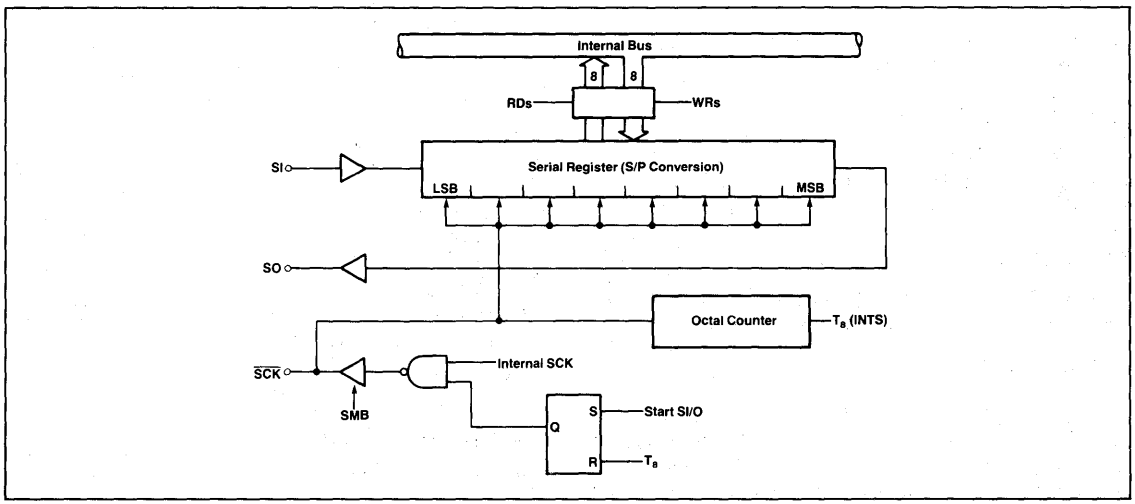


Figure 3. Serial Port Diagram



4

Reset

An active-low signal on the $\overline{RESET}$ input for more than 4 μs forces the μPD78C05A/06A into a reset condition, which affects the following internal functions:

- The interrupt enable flags are reset, and interrupts are inhibited.
- The interrupt request flag is reset.
- The halt flip-flop is reset, and the halt state is released.
- The contents of the mode B register are set to FFH, and port B becomes an input port.
- All flags are reset to 0.
- The internal count register for timer operation is set to FFH and the timer F/F is reset.
- The contents of the program counter are set to 0000H.
- Data bus (DB_0-DB_7), $\overline{RD}$, and $\overline{WR}$ go to a high-impedance state.

Once the $\overline{RESET}$ input goes high, the program is started at location 0000H.

Stop and Halt Modes

The μPD78C05A/06A have a stop and a halt mode. The effects of stop and halt on various functions are shown in table 2.

Registers

The μPD78C05A/06A contain seven 8-bit registers and two 16-bit registers. See figure 4.

General Purpose Registers

The general purpose registers B, C, D, E, H, L can function as auxiliary registers to the accumulator or in pairs as data pointers (BC, DE, HL). Automatic increment and decrement addressing mode capabilities extend the uses for the DE and HL register pairs.

Figure 4. Registers

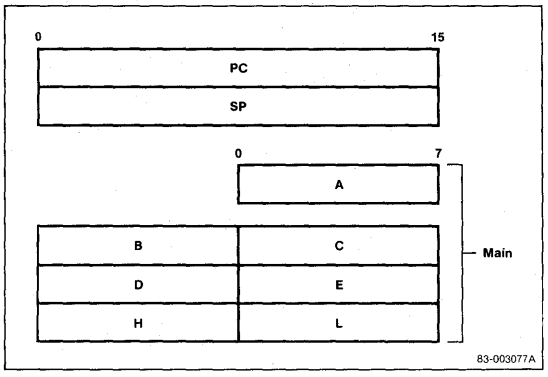


Table 2. Halt and Stop Modes

Function	Halt Mode	Stop Mode
Oscillator	Run	Stop
Internal system clock	Stop	
Timer	Run	
Timer register	Hold	Set
Upcounter, prescaler 0, 1	Run	Cleared
Serial interface	Run	Run (1)
Serial clock	Hold	Hold
Interrupt control circuit	Run	Stop
Interrupt enable flag	Hold	Reset
INT_0, INT_1 input	Active	Inactive
INT_T		—
T_8 (INTFS)		—
Mask register	Hold	Set
Pending interrupts (INTFX)		Reset
REL input	Inactive	Active
RESET input	Active	
On-chip RAM	Hold	Hold
Output latch in ports A, B, E		
Program counter (PC)		Cleared
Stack pointer (SP)		Unknown
General registers (A, B, C, D, E, F, L)		
Program status word (PSW)		Reset
Mode B register		Hold
Standby control register (SC_0-SC_3)		
Standby control register (SC_4)		Set
Timer mode register (TMM_0-TMM_1)		Hold
Timer mode register (TMM_1)		Set
Serial mode register (SM)		Hold
Data bus (DB_0-DB_7)	High-Z	High-Z
RD, WR output	High	High

Note:

(1) Serial clock counter is running and T_8 is generated; however, there are no effects from it.

Accumulator [A]

All data transfers between the μPD78C05A/ 06A and external memory or I/O are done through the accumulator.

Program Counter [PC]

The PC is a 16-bit register containing the address of the next instruction to be fetched. Under normal program flow, the PC is automatically incremented. However, in the case of a branch instruction, the PC contents are from another register or an instruction's immediate data. A reset sets the PC to 0000H.

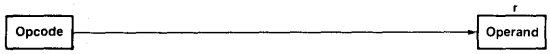
Stack Pointer [SP]

The stack pointer is a 16-bit register used to maintain the top of the stack area (last-in/first-out). The contents of the SP are decremented during a Call or Push instruction or if an interrupt occurs. The SP is incremented during a Return or POP instruction.

Address Modes

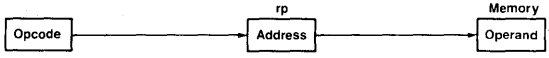
Register Addressing

The instruction opcode specifies a register that contains the operand.



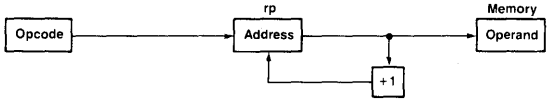
Register Indirect Addressing

The instruction opcode specifies a register pair that contains the memory address of the operand. Mnemonics with an X suffix indicate this address mode.

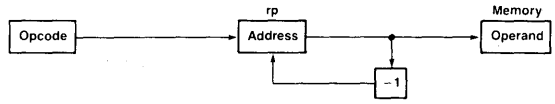


Automatic Increment Addressing

The opcode specifies a register pair that contains the memory address of the operand. The contents of the register pair are automatically incremented to point to a new operand. This mode provides automatic sequential stepping when working with a table of operands.

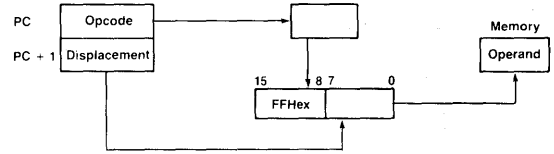


Automatic Decrement Addressing



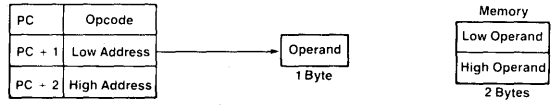
Working-Register Addressing

The contents of the register are linked with the byte following the opcode to form a memory address that contains the operand. The V register is used to indicate the memory page. This address mode is useful as a short-offset address mode when working with operands in a common memory page where only one additional byte is required for the address. Mnemonics with a W suffix indicate this address mode. In the μPD78C05A/ 06A, the V register is always FFH.



Direct Addressing

The two bytes following the opcode specify an address of a location containing the operand.

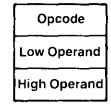


Immediate Addressing

PC
PC + 1

Immediate Extended Addressing

PC
PC + 1
PC + 2



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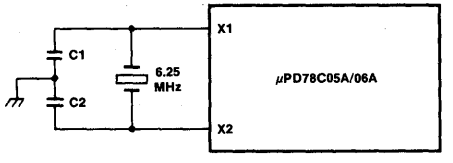
Clock Driver Circuit

The 6.25-MHz master timing signal is from an external oscillator connected to pin X1 or from an internal oscillator controlled by an external 6.25-MHz crystal connected to pins X1 and X2 (figure 5). Dividing f_{OSC} by four creates the internal CPU clock (f_ϕ = 1.5625 MHz).

A system clock is available for external use at the ϕ_{OUT} pin. Its frequency is 1.5625 MHz (6.25/4) or 0.78125 MHz (6.25/8) for 78C05A and 78C06A, respectively.

Figure 5. External 6.25-MHz Crystal



Crystal specifications
AT cut
f_{OSC} = 6.25 MHz
R = 50 Ω
C_L = 16 ±0.2 pF
P = 1.0 ±0.2 mW

Capacitor specifications
C1, C2 = 5 to 20 pF [including stray capacitance]
|C1 − C2| ≤ 10 pF

83-002772A

Instructions

Instruction Set Definitions

Operand	Description
r	A, B, C, D, E, H, L
r1	B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, MK, MB, TM_0, TM_1, S, SM, SC
sr1	PA, PB, PC, MK, S, TM_0, TM_1, SC
sr2	PA, PB, PC, MK
rp	SP, B, D, H
rp1	B, D, H
rpa	B, D, H, D^+, H^+, D^-, H^-
wa	8-bit immediate data used to access working register area
word	16-bit immediate data
byte	8-bit immediate data
bit	1-bit immediate data
if	F0, F1, FT, FS
F	CY, Z
fa	10-bit immediate data used to access fixed area in locations 0-2047
ta	5-bit immediate data used to access table in locations 128-191
n	Number of bytes in an instruction

Note:

(1) When special register operands sr, sr1, sr2 are used, PA = port A, PB = port B, PC = port C, MK = mask register, MB = mode B register, SM = serial mode register, SC = standby control register, TM_0 = timer register 0, TM_1 = timer register 1, S = serial register.

(2) When register pair operands rp, rp1 are used, SP = stack pointer, B = BC, D = DE, H = HL.

(3) Operands rpa, rp1, wa are used in indirect addressing and auto-increment/auto-decrement addressing modes. B = (BC), D = (DE), H = (HL), D^+ = $(DE)^+$, H^+ = $(HL)^+$, D^- = $(DE)^-$, and H^- = $(HL)^-$.

(4) When the interrupt operand "if" is used, F0 = INTF0, F1 = INTF1, FT = INTFT, FS = INTFS.

(5) When the operand F is used, CY = Carry and Z = Zero.

(6) The V register is always FFH.

Instruction Set

Mnemonic	Operand	Bytes	*Clocks	Operation	Skip Condition	Flags CY	Flags Z
8-Bit Data Transfer							
MOV	r1,A	1	4/6	(r1) ← (A)			
MOV	A,r1	1	4/6	(A) ← (r1)			
MOV	sr,A	2	10/14	(sr) ← (A)			
MOV	A,sr1	2	10/14	(A) ← (sr1)			
MOV	r,word	4	17/25	(r) ← (word)			
MOV	word,r	4	17/25	(word) ← (r)			
MV1	r,byte	2	7/11	(r) ← (byte)			
STAW	wa	2	10/14	(FFH,wa) ← (A)			
LDAW	wa	2	10/14	(A) ← (FFH,wa)			
STAX	rpa	1	7/9	((rpa)) ← (A)			
LDAX	rpa	1	7/9	(A) ← ((rpa))			
16-Bit Data Transfer							
SBCD	word	4	20/28	(word) ← (C), (word + 1) ← (B)			
SDED	word	4	20/28	(word) ← (E), (word + 1) ← (D)			
SHLD	word	4	20/28	(word) ← (L), (word + 1) ← (H)			
SSPD	word	4	20/28	(word) ← (SP_L), ((word) + 1) ← (SP_H)			
LBCD	word	4	20/28	(C) ← (word), (B) ← (word + 1)			
LDED	word	4	20/28	(E) ← (word), (D) ← (word + 1)			
LHLD	word	4	20/28	(L) ← (word), (H) ← (word + 1)			
LSPD	word	4	20/28	(SP_1) ← (word)			
POP	rp1	2	14/18	($rp1_L$) ← ((SP)) ($rp1_H$) ← ((SP) + 1), (SP) ← (SP) + 2			
LXI	rp,word	3	10/16	(rp) ← word			
Arithmetic							
ADD	A,r	2	8/12	(A) ← (A) + (r)		↕	↕
ADDX	rpa	2	11/15	(A) ← (A) + ((rpa))		↕	↕
ADC	A,r	2	8/12	(A) ← (A) + (r) + (CY)		↕	↕
ADCX	rpa	2	11/15	(A) ← (A) + ((rpa)) + (CY)		↕	↕
SUB	A,r	2	8/12	(A) ← (A) − (r)		↕	↕
SUBX	rpa	2	11/15	(A) ← (A) − ((rpa))		↕	↕
SBB	A,r	2	8/12	(A) ← (A) − (r) − (CY)		↕	↕
SBBX	rpa	2	11/15	(A) ← (A) − ((rpa)) − (CY)		↕	↕
ADDNC	A,r	2	8/12	(A) ← (A) − (r)	No carry	↕	↕
ADDNCX	rpa	2	11/15	(A) ← (A) − ((rpa))	No carry	↕	↕
SUBNB	A,r	2	8/12	(A) ← (A) − (r)	No borrow	↕	↕
SUBNBX	rpa	2	11/15	(A) ← (A) − (rpa)	No borrow	↕	↕

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Instruction Set (cont)

Mnemonic	Operand	Bytes	*Clocks	Operation	Skip Condition	Flags CY	Flags Z
Logical							
ANA	A,r	2	8/12	(A) ← (A) ∧ (r)			‡
ANAX	rpa	2	11/15	(A) ← (A) ∧ ((rpa))			‡
ORA	A,r	2	8/12	(A) ← (A) ∨ (r)			‡
ORAX	rpa	2	11/15	(A) ← (A) ∨ ((rpa))			‡
XRA	A,r	2	8/12	(A) ← (A) ∨ (r)			‡
XRAX	rpa	2	12/15	(A) ← (A) ∨ ((rpa))			‡
GTA	A,r	2	8/12	(A) − (r) − 1	No borrow	‡	‡
GTAX	rpa	2	11/15	(A) − ((rpa)) − 1	No borrow	‡	‡
LTA	A,r	2	8/12	(A) − (r)	Borrow	‡	‡
LTAX	rpa	2	11/15	(A) − ((rpa))	Borrow	‡	‡
ONAX	rpa	2	8/12	(A) ∧ ((rpa))	No zero	‡	‡
OFFAX	rpa	2	11/15	(A) ∧ ((rpa))	Zero	‡	‡
NEA	A,r	2	8/12	(A) − (r)	No zero	‡	‡
NEAX	rpa	2	11/15	(A) − ((rpa))	No zero	‡	‡
EQA	A,r	2	8/12	(A) − (r)	Zero	‡	‡
EQAX	rpa	2	11/15	(A) − ((rpa))	Zero	‡	‡
Immediate Data Transfer (Accumulator)							
XRI	A,byte	2	7/11	(A) ← (A) ∨ byte			‡
ADINC	A,byte	2	7/11	(A) ← (A) − byte	No carry	‡	‡
SUINB	A,byte	2	7/11	(A) ← (A) − byte	No borrow	‡	‡
ADI	A,byte	2	7/11	(A) ← (A) + byte		‡	‡
ACI	A,byte	2	7/11	(A) ← (A) + byte + (CY)		‡	‡
SUI	A,byte	2	7/11	(A) ← (A) − byte		‡	‡
SBI	A,byte	2	7/11	(A) ← (A) − byte −(CY)		‡	‡
ANI	A,byte	2	7/11	(A) ← (A) ∧ byte			‡
ORI	A,byte	2	7/11	(A) ← (A) ∨ byte			‡
GTI	A,byte	2	7/11	(A) − byte − 1	No borrow	‡	‡
LTI	A,byte	2	7/11	(A) − byte	Borrow	‡	‡
ONI	A,byte	2	7/11	(A) ∧ byte	No zero	‡	‡
OFFI	A,byte	2	7/11	(A) ∧ byte	Zero		‡
NEI	A,byte	2	7/11	(A) − byte	No zero	‡	‡
EQI	A,byte	2	7/11	(A) − byte	Zero	‡	‡
Immediate Data Transfer (Special Register)							
ANI	sr2,byte	3	17/23	(sr2) ← (sr2) ∧ byte			‡
ORI	sr2,byte	3	17/23	(sr2) ← (sr2) ∨ byte			‡
OFFI	sr2,byte	3	14/20	(sr2) ∧ byte	Zero		‡
ONI	sr2,byte	3	14/20	(sr2) ∧ byte	No zero		‡

Instruction Set (cont)

Mnemonic	Operand	Bytes	*Clocks	Operation	Skip Condition	Flags CY	Flags Z
Working Register							
ANIW	wa,byte	3	16/22	(FFH, wa) ← (FFH, wa) ∧ byte			↕
ORIW	wa,byte	3	16/22	(FFH, wa) ← (FFH, wa) V byte			↕
GTIW	wa,byte	3	13/19	(FFH, wa) − byte − 1	No borrow	↕	↕
LTIW	wa,byte	3	13/19	(FFH, wa) − byte	Borrow	↕	↕
ONIW	wa,byte	3	13/19	(FFH, wa) ∧ byte	No zero		↕
OFFIW	wa,byte	3	13/19	(FFH, wa) ∧ byte	Zero		↕
NEIW	wa,byte	3	13/19	(FFH, wa) − byte	No zero	↕	↕
EQIW	wa,byte	3	13/19	(FFH, wa) − byte	Zero	↕	↕
Increment/Decrement							
INR	r2	1	4/6	(r2) ← (r2) + 1	Carry		↕
INRW	wa	2	13/17	(FFH, wa) ← (FFH, wa) + 1	Carry		↕
DCR	r2	1	4/6	(r2) ← (r2) − 1	Borrow		↕
DCRW	wa	2	13/17	(FFH, wa) ← (FFH, wa) − 1	Borrow		↕
INX	rp	1	7/9	(rp)←(rp) + 1			
DCX	rp	1	7/9	(rp)←(rp) − 1			
Miscellaneous							
DAA		1	4/6	Decimal adjust accumulator		↕	↕
STC		2	8/12	(CY) ← 1		1	
CLC		2	8/12	(CY) ← 0		0	
Rotate and Shift							
RLD		2	17/21	Rotate left digit			
RRD		2	17/21	Rotate right digit			
RAL		2	8/12	$(A_{m+1}) \leftarrow (A_m)$, $(A_0) \leftarrow (CY)$, $(CY) \leftarrow (A_7)$		↕	
RAR		2	8/12	$(A_{m-1}) \leftarrow (A_m)$, $(A_7) \leftarrow (CY)$, $(CY) \leftarrow (A_0)$		↕	
Jump							
JMP	word	3	10/16	(PC) ← word			
JB		1	4/6	$(PC_H) \leftarrow (B)$, $(PC_L) \leftarrow (C)$			
JR	word	1	10/12	(PC) ← (PC) + 1 + jdisp1			
JRE	word	2	13/17	(PC) ← (PC) + 2 + jdisp			

Instruction Set

Mnemonic	Operand	Bytes	*Clocks	Operation	Skip Condition	Flags CY	Flags Z
Call							
CALL	word	3	16/22	$((SP)-1) \leftarrow ((PC)+3)_H$, $((SP)-2) \leftarrow ((PC)+3)_L$, $(PC) \leftarrow$ word			
CALF	word	2	13/17	$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_{15}\text{-}PC_{11}) \leftarrow 00001$, $(PC_{10}\text{-}PC_0) \leftarrow$fa			
CALT	word	1	19/21	$((SP)-1) \leftarrow ((PC)+1)_H$, $((SP)-2) \leftarrow ((PC)+1)_L$, $(PC_L) \leftarrow (128+2ta)$, $(PC_H) \leftarrow (129+2ta)$			
Return							
RET		1	10/12	$(PC_L) \leftarrow ((SP))$, $(PC_H) \leftarrow ((SP)+1)$, $(SP) \leftarrow (SP)+2$			
RETS		1	10+n/12+n	$(PC_L) \leftarrow ((SP))$, $(PC_H) \leftarrow ((SP)+1)$, $(SP) \leftarrow (SP)+2$, $(PC) \leftarrow (PC)+n$			
RETI		1	13/15	$(PC_L) \leftarrow ((SP))$, $(PC_H) \leftarrow ((SP)+1)$, $(PSW) \leftarrow ((SP)+2)$, $(SP) \leftarrow (SP)+3$			
Skip							
SKNC		2	8/12	Skip if no carry	CY = 0		
SKNZ		2	8/12	Skip if co zero	Z = 0		
SKNIT	f	2	8/12	Skip if no INT X otherwise reset INT X	f = 0		
CPU Control							
NOP		1	4/6	No operation			
EI		2	8/12	Enable interrupt			
DI		2	8/12	Disable interrupt			
Serial Port Control							
SIO		1	4/6	Start (trigger) serial I/O			
STM		1	4/6	start timer			
Port E Control							
PEX		2	11/15	$(PE_{15}\text{-}PE_8) \leftarrow$ (B), $(PE_7\text{-}PE_0) \leftarrow$ (C)			
PER		2	8/12	Port E AB mode			

Program Status Word (PSW) Operation

Operation					D_6	D_5	D_4	D_3	D_2	D_0
Reg. Memory		**Immediate**		**Skip**	**Z**	**SK**	**HC**	**L1**	**L0**	**CY**
ADD ADC SUB SBB	ADDX ADCX SUBX SBBX	ADI ACI SUI SBI			↕	0	↕	0	0	↕
ANA ORA XRA	ANAX ORAX XRAX	ANI ORI XRI	ANIW ORIW		↕	0	•	0	0	•
ADDNC SUBNB GTA LTA	ADDNCX SUBNBX GTAX LTAX	ADINC SUINB GTI LTI	 GTIW LTIW		↕	↕	↕	0	0	↕
	ONAX OFFAX	ONI OFFI	ONIW OFFIW		↕	↕	•	0	0	•
NEA EQA	NEAX EQAX	NEI EQI	NEIW EQIW		↕	↕	↕	0	0	↕
INR DCR	INRW DCRW				↕	↕	↕	0	0	•
DAA					↕	0	↕	0	0	↕
RLL, RLR					•	0	•	0	0	↕
RLD-RRD					•	0	•	0	0	•
STC					•	0	•	0	0	↕
CLC					•	0	•	0	0	0
		MVI A, byte			•	0	•	1	0	•
		MVI L, byte LXI H, word			•	0	•	0	1	•
				SKNC SKNZ SKNIT	•	↕	•	0	0	•
				RETS	•	1	•	0	0	•
All other instructions					•	0	•	0	0	•

Flag Symbols:

↕ Flag affected according to result of operation.
1 Flag set
0 Flag reset
• Flag not affected.

4

NEC

NEC Electronics Inc.

μPD7807/08/09
HIGH-END, 8-BIT, SINGLE-CHIP NMOS MICROCOMPUTERS WITH COMPARATOR AND 8K ROM

PRELIMINARY INFORMATION

Description

The μPD7807/μPD7808/μPD7809 single chip microcomputer augments the high-end NEC family of 8-bit microcomputers with on-chip peripheral functions. Like the μPD7811, the device has a fast internal 16-bit ALU and data paths, 256 bytes of RAM, a multifunctional 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs.

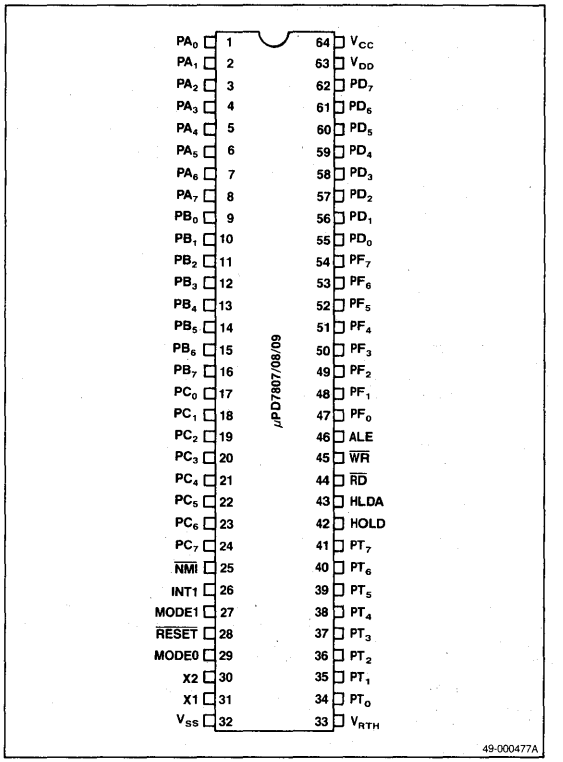
Other features are 8K ROM (4K ROM for the μPD7808), a programmable threshold comparator (8 inputs), a programmable WAIT function, a watchdog timer, hold and hold acknowledge for DMA interfaces, and bit test/write instructions for both RAM and I/O.

The μPD7809 and μPD7808 are mask-ROM versions with your program on chip. The μPD7807 is the ROM-less version for prototyping and small volume applications.

Features

- ☐ NMOS silicon gate technology requiring +5 V power supply
- ☐ Complete single-chip microcomputer
  - —16-bit ALU
  - —8K ROM (4K ROM for the μPD7808)
  - —256-byte RAM
- ☐ Large I/O capability
  - —40 I/O port lines (μPD7809 and μPD7808)
  - —28 I/O port lines (μPD7807)
  - —8 input lines
- ☐ Two zero-cross detect inputs
- ☐ Expansion capabilities (64K memory access total)
  - —8085A bus compatible
  - —56K-byte external memory address range (60K for the μPD7808)
- ☐ Programmable threshold comparator
  - —8 inputs, 1 of 16 software selectable levels
- ☐ Full duplex USART
  - —Synchronous and asynchronous
- ☐ 165 instructions
  - —16-bit arithmetic, multiply and divide
- ☐ 1 μs instruction cycle time
- ☐ Prioritized interrupt structure
  - —3 external
  - —8 internal
- ☐ Hold, hold acknowledge for DMA interface
- ☐ Programmable WAIT function
- ☐ Watchdog timer
- ☐ Standby function
- ☐ On-chip clock generator
- ☐ 64-pin plastic straight or bent lead QUIP or plastic shrink DIP

Pin Configuration



Ordering Information

Part Number	Package Type	Max Freq. of Operation
μPD7807G-36 μPD7808G-36 μPD7809G-36	64-Pin plastic QUIP	12 MHz
μPD7807CW μPD7808CW μPD7809CW	64-Pin plastic shrink DIP	12 MHz

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Pin Identification

No.	Symbol	Function
1-8	PA_0-PA_7	Port A I/O
9-16	PB_0-PB_7	Port B I/O
17	PC_0/TxD	Port C I/O line 0/Transmit data output
18	PC_1/RxD	Port C I/O line 1/Receive data input
19	PC_2/$\overline{SCK}$	Port C I/O line 2/Serial clock I/O
20	PC_3/TI/ $\overline{INT2}$	Port C I/O line 3/Timer input/Interrupt request 2 input
21	PC_4/TO	Port C I/O line 4/Timer output
22	PC_5/CI	Port C I/O line 5/Counter input
23,24	PC_6, PC_7/ CO_0, CO_1	Port C I/O lines 6, 7/Counter outputs 0, 1
25	$\overline{NMI}$	Nonmaskable interrupt input
26	INT1	Interrupt request 1 input
27	MODE1/$\overline{M1}$	Mode 1 input/memory cycle 1 output
28	$\overline{RESET}$	Reset input
29	MODE0/ $\overline{IO}$/M	Mode 0 input/I/O/memory output
30,31	X2, X1	Crystal connections 1, 2
32	V_{SS}	Ground
33	V_{RTH}	Port T threshold voltage input
34-41	PT_0-PT_7	Port T variable threshold input port
42	HOLD	Hold request input
43	HLDA	Hold acknowledge output
44	$\overline{RD}$	Read strobe output
45	$\overline{WR}$	Write strobe output
46	ALE	Address latch enable output
47-54	PF_0-PF_7	Port F I/O
55-62	PD_0-PD_7	Port D I/O
63	V_{DD}	RAM backup power supply
64	V_{CC}	5 V power supply

Pin Functions

PA_0-PA_7 [Port A]

Port A is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port A inputs.

PB_0-PB_7 [Port B]

Port B is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port B inputs.

PC_0-PC_7 [Port C]

Port C is an 8-bit three-state port. Each bit is independently programmable as either input or output. Alternatively, the lines of port C can be used as control lines for the USART and timer. Reset puts all lines of port C in port mode, input.

TxD [Transmit Data]. Serial data output terminal.

RxD [Receive Data]. Serial data input terminal.

$\overline{SCK}$ [Serial Clock]. Output for the serial clock when internal clock is used. Input for serial clock when external clock is used.

TI [Timer Input]. Timer input terminal.

$\overline{INT2}$ [Interrupt Request 2]. Falling-edge-triggered, maskable interrupt input terminal and AC-input, zero-cross detection terminal.

TO [Timer Output]. The output of TO is a square wave with a frequency determined by the timer.

CI [Counter Input]. External pulse input to timer/event counter.

CO_0, CO_1 [Counter Outputs 0, 1]. Programmable rectangular wave outputs based on timer/event counter.

PD_0-PD_7 [Port D]

Port D is an 8-bit three-state port. It can be programmed as either 8 bits of input or 8 bits of output. When external expansion memory is used, port D acts as the multiplexed address/data bus.

PF_0-PF_7 [Port F]

Port F is an 8-bit three-state port. Each bit is independently programmable as an input or output. When external expansion memory is used, port F outputs the high-order address bits.

PT_0-PT_7 [Port T]

Port T is made up of 8 variable threshold inputs. The input of each line is compared to a threshold voltage.

V_{RTH} [Variable Threshold Reference Voltage]

V_{RTH} is the reference voltage that the port T threshold voltage is derived from.

$\overline{NMI}$ [Nonmaskable Interrupt]

Falling-edge-triggered nonmaskable interrupt input.

INT1 [Interrupt Request 1]

INT1 is a rising-edge-triggered, maskable interrupt input. It is also an AC-input, zero-cross detection terminal.

$\overline{\text{RESET}}$ [Reset]

When the $\overline{\text{RESET}}$ input is brought low, it initializes the PD7807/08/09.

MODE1, MODE0 [Mode 1, 0]

The MODE1 and MODE0 inputs select the memory expansion mode. MODE1 also outputs the $\overline{\text{M1}}$ signal during each opcode fetch. MODE0 outputs the $\overline{\text{IO}}$/M signal.

HOLD [Hold Request]

When the HOLD input is high, the CPU is put in a hold state until HOLD is brought low.

HLDA [Hold Acknowledge]

The CPU brings the HLDA output high when it is in the hold state, and low when the hold is released.

$\overline{\text{RD}}$ [Read Strobe]

The $\overline{\text{RD}}$ output goes low to gate data from external devices onto the data bus. $\overline{\text{RD}}$ goes high during reset. Three-state.

$\overline{\text{WR}}$ [Write Strobe]

The $\overline{\text{WR}}$ output goes low to indicate that the data bus holds valid data. It is a strobe signal for external memory or I/O write operations. $\overline{\text{WR}}$ goes high during reset. Three-state.

ALE [Address Latch Enable]

The ALE output latches the address signal to the output of PD_0-PD_7.

X1, X2 [Crystal Connections 1, 2]

X1 and X2 are the system clock crystal oscillator terminals. X1 is the input for an external clock.

V_{SS} [Ground]

Ground potential.

V_{DD} [Backup Power]

Backup power for on-chip RAM.

V_{CC} [Power Supply]

+5 V power supply.

Input/Output

The μPD7807/08/09 has 8 comparator input lines (port T) and 40 digital I/O lines; five 8-bit ports (port A, port B, port C, port D, port F).

Comparator Input Lines. PT_0-PT_7 are configured as variable threshold comparator input lines.

Port A, Port B, Port C, Port F. Each line of these ports can be individually programmed as an input or output. When used as I/O ports, all have latched outputs and high-impedance inputs.

Port D. Port D can be programmed as a byte input or a byte output.

Control Lines. Under software control, each line of port C can be configured individually to provide control lines for the serial interface, timer, and timer/counter.

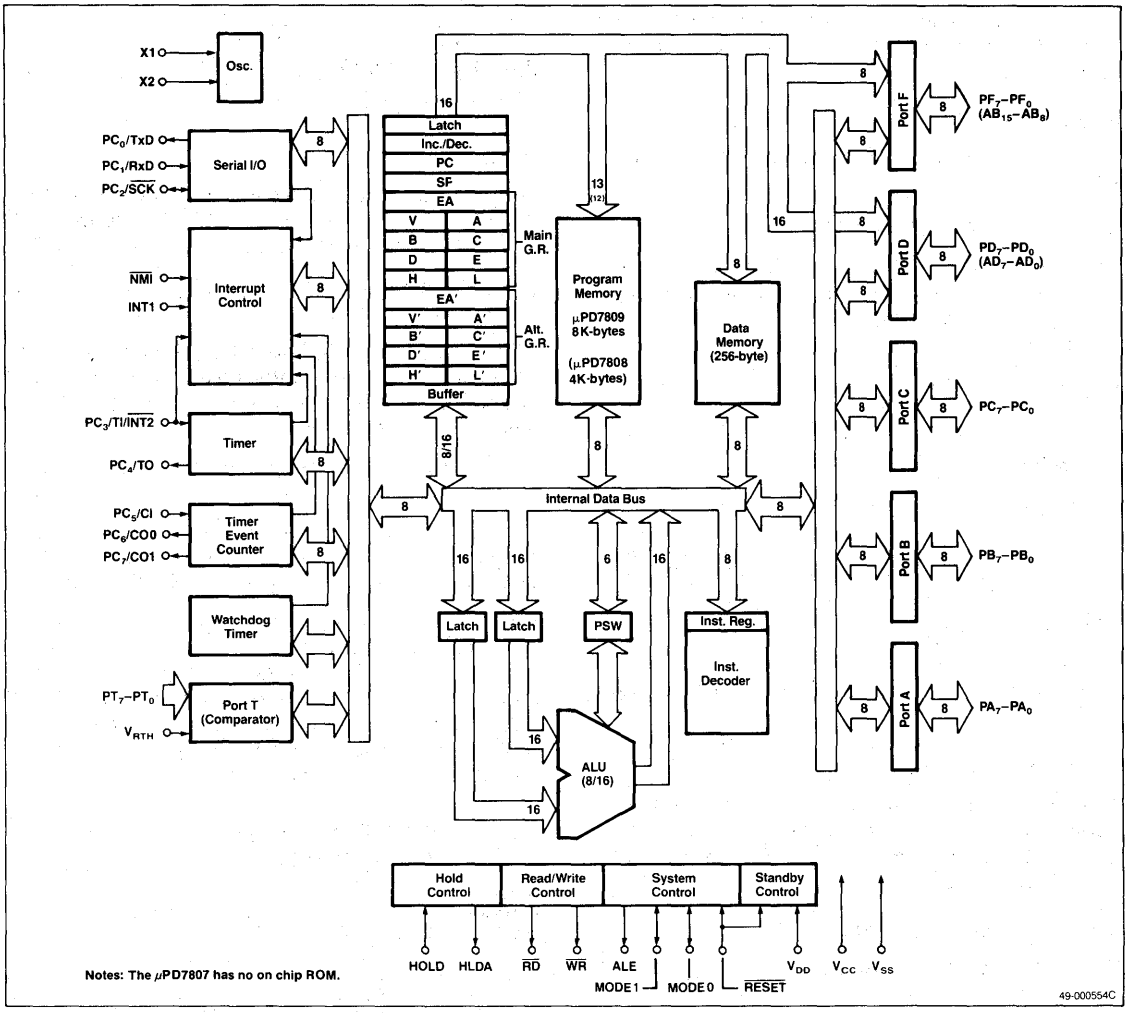
Memory Expansion. In addition to the single-chip operation mode, the μPD7809 has four memory expansion modes. Under software control, port D can provide a multiplexed low-order address and data bus; port F can provide a high-order address bus. Table 1 shows the relation between memory expansion modes and the pin configurations of port D and port F.

Table 1. Memory Expansion Modes and Port Configurations

Memory Expansion	Port Configuration	
None	Port D	I/O port
	Port F	I/O port
256 Bytes	Port D	Multiplexed address/data bus
	Port F	I/O port
4K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_3	Address bus
	Port F_4-F_7	I/O port
16K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_5	Address bus
	Port F_6-F_7	I/O port
56K Bytes	Port D	Multiplexed address/data bus
	Port F	Address bus

4

Block Diagram



Timers

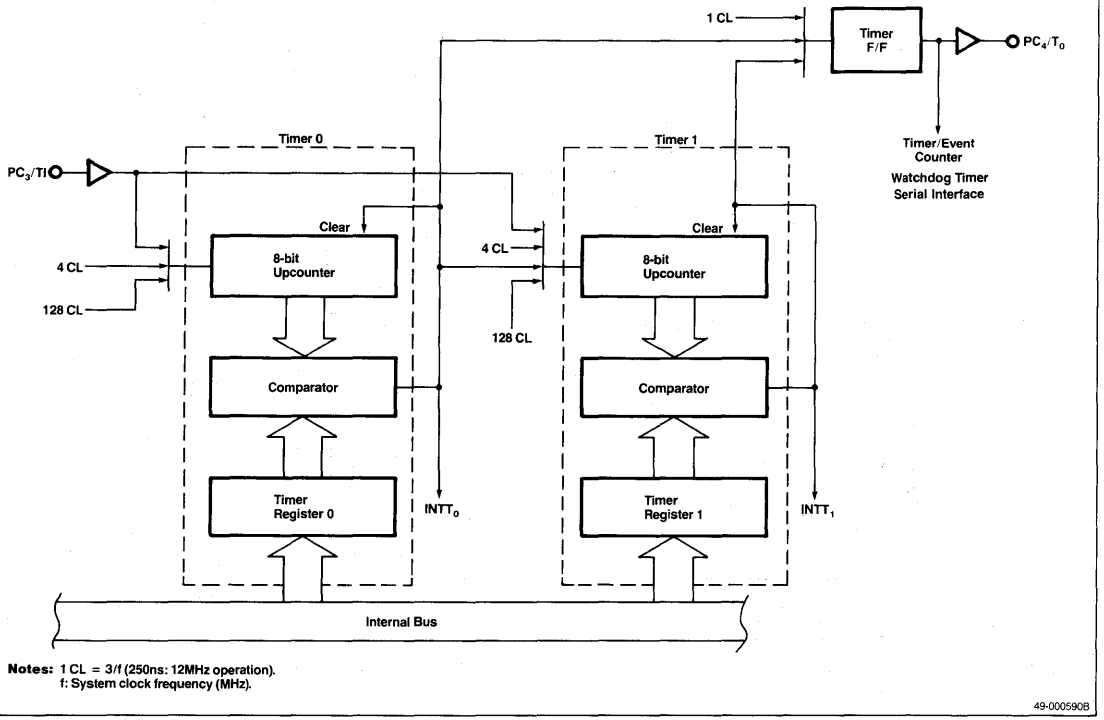
The timers consist of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be software set to increment at intervals of four machine cycles (1 μs at 12 MHz operation) or 128 machine cycles (32 μs at 12 MHz), or to increment on receipt of a pulse at TI. Figure 1 shows the block diagram for the timer.

Timer/Event Counter

The 16-bit multifunctional timer/event counter (figure 2) can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output

Figure 1. Timer Block Diagram



Interrupt Structure

There are 11 interrupt sources. Three are external interrupts and eight are internal. The following, table 2, shows 11 interrupt sources divided into six priority levels. See figure 3.

Standby Function

The standby function saves the top 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On power up, you can check the standby flag to determine whether recovery was made from standby mode or from a cold start.

Table 2. Interrupt Sources

Interrupt Request	Interrupt Address	Type of Interrupt	Internal/ External
IRQ0	4	$\overline{NMI}$ (Nonmaskable interrupt)	Ext
		INTWD (Watchdog timer)	Int
IRQ1	8	INTT0 (Coincidence signal from timer 0)	Int
		INTT1 (Coincidence signal from timer 1)	
IRQ2	16	$\overline{INT1}$ (Maskable interrupt)	Ext
		INT2 (Maskable interrupt)	
IRQ3	24	INTE0 (Coincidence signal from timer/event counter)	Int
		INTE1 (Coincidence signal from timer/event counter)	
IRQ4	32	INTEIN (Falling signal of CI and TO counter)	Int/Ext
IRQ5	40	INTSR (Serial receive interrupt)	Int
		INST (Serial send interrupt)	

4

Figure 2. Timer/Event Counter Block Diagram

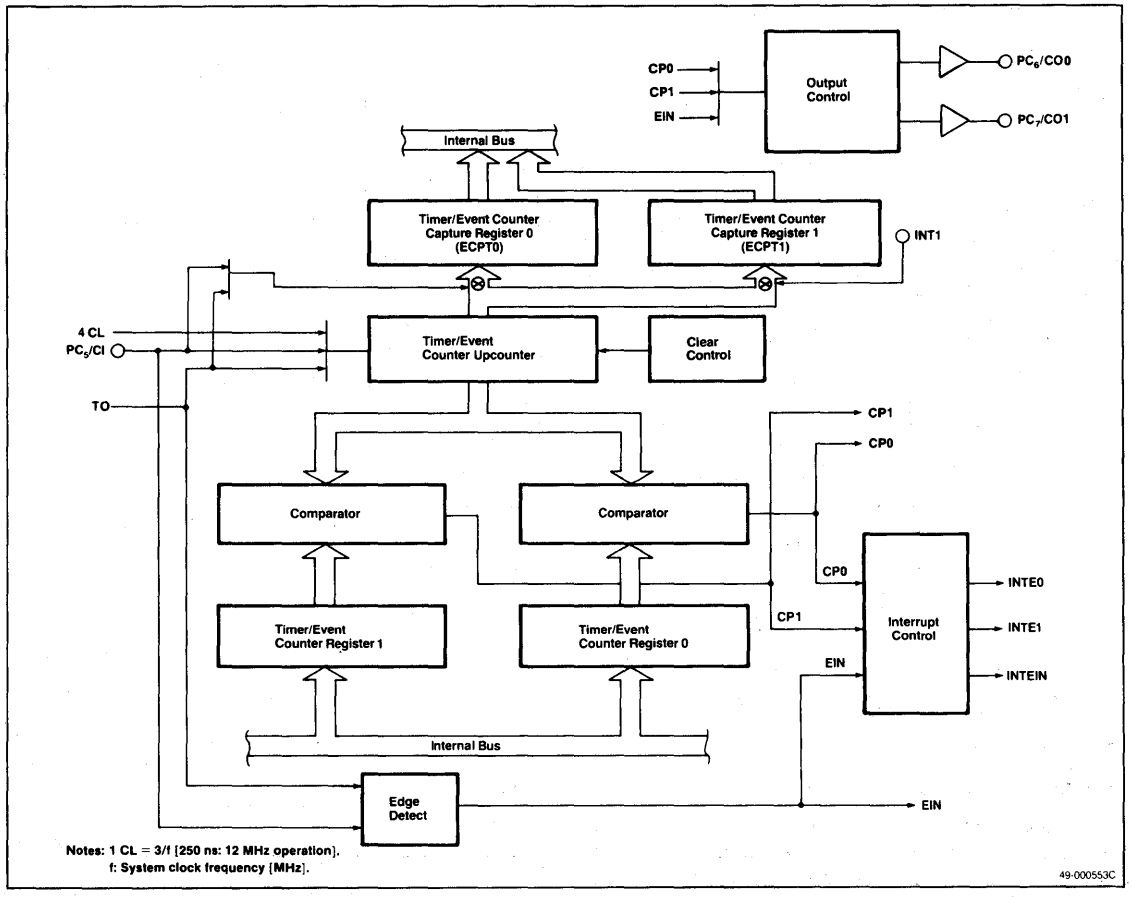


Figure 3. Interrupt Structure Block Diagram

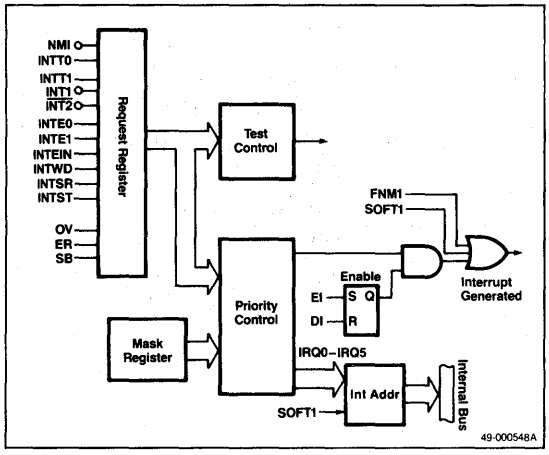
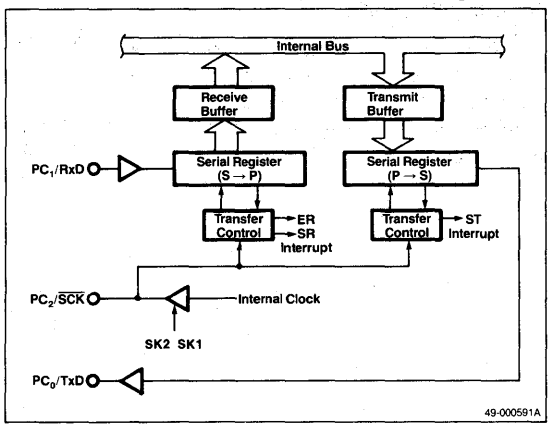


Figure 4. Universal Serial Interface Block Diagram



Universal Serial Interface

The serial interface can operate in one of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first, for easy interfacing to certain NEC peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception: search and nonsearch. In the search mode, data is transferred one bit at a time from the serial register to the receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from the serial register to the transmit buffer occurs eight bits at a time. In asynchronous mode, the serial interface can act as a full-duplex USART with data transfer rates up to 125K bps. Figure 4 shows the universal serial interface block diagram.

Zero-Crossing Detector

The INT1 and $\overline{INT2}$ terminals (used common to TI and PC_3) can detect the zero-crossing point of low-frequency AC signals. When driven directly, these pins respond as a normal digital input. Figure 5 shows the zero-crossing detection circuitry.

The zero-crossing detection capability allows you to make the 50-60 Hz power signal the basis for system timing and to control voltage phase sensitive devices.

To use the zero-cross detection mode, an AC signal of approximately 1-3 V AC (peak-to-peak) and a maximum frequency of 1 kHz is coupled through an external capacitor to the INT1 and $\overline{INT2}$ pins.

For the INT1 pin, the internal digital state is sensed as a 0 until the rising edge crosses the average DC level, when it becomes a 1 and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a 1 until the falling edge crosses the average DC level, when it becomes a 0 and $\overline{INT2}$ interrupt is generated.

Variable Threshold Input Port [Port T]

Port T has the following features:

- 8 input lines
- 16 threshold levels from 1/16 to 16/16 of reference voltage (V_{RTH})
- Level selected by writing to mode T register (figure 7)
- Output of comparator reads 0 until voltage at pin exceeds selected level
- Comparison execution time: 12 μs

Figure 6 shows the block diagram for the threshold variable input port. Figure 7 shows the mode T register format.

Figure 5. Zero-Crossing Detection Circuitry

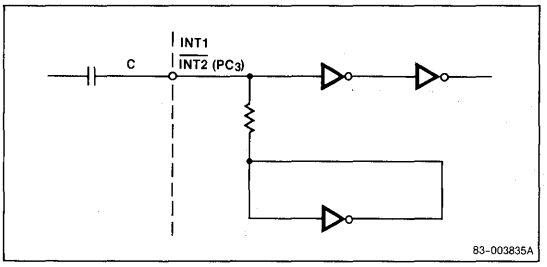


Figure 6. Threshold Variable Input Port

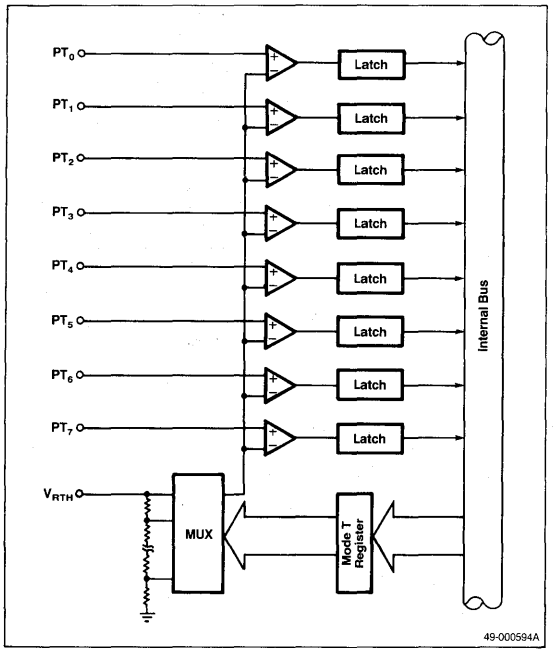
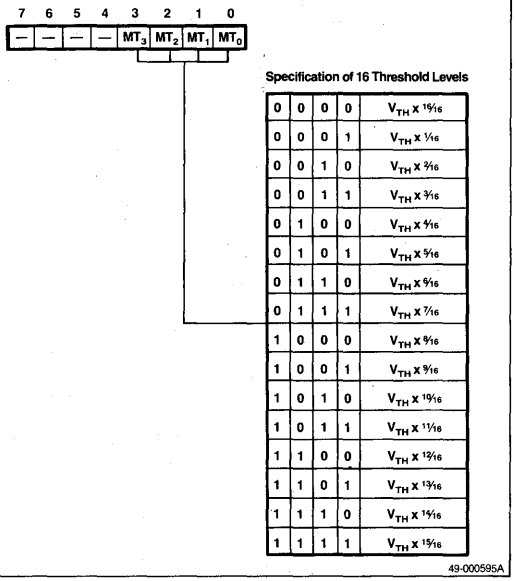


Figure 7. Mode T Register Format



Watchdog Timer

Use the watchdog timer for software or overall performance safety checks. If the watchdog is enabled, it must be cleared at regular intervals in program execution to avoid watchdog interrupts. Intervals are software selectable via the WDM register. Figure 8 shows the block diagram for the watchdog timer.

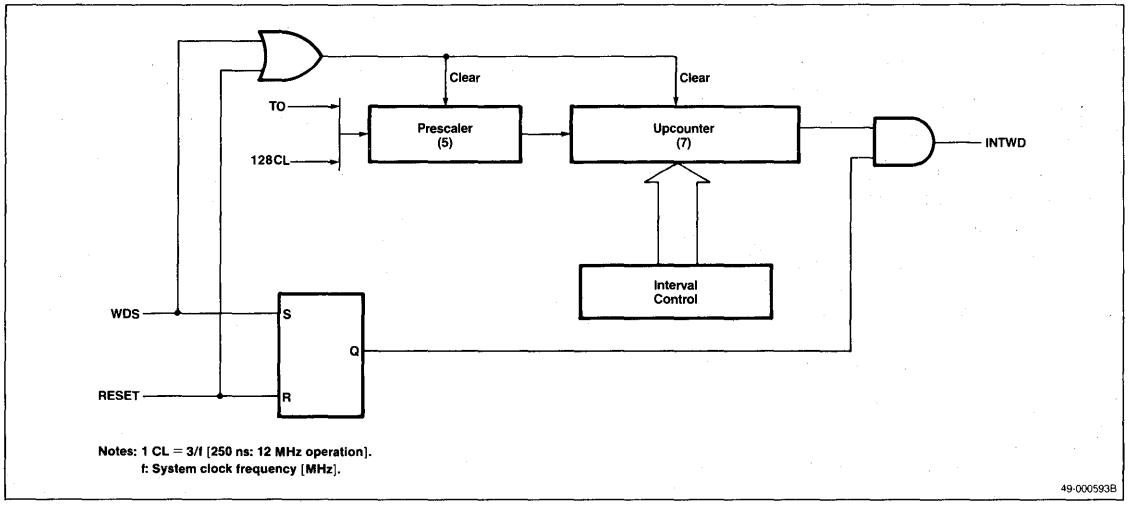
Bit Address Instructions

The following bits may be addressed directly with certain instructions:

- Any bit in the first 16 bytes of memory addressed by the V register
- Any bit in the five 8-bit I/O ports (A, B, C, D, F)
- Any bit in the comparator port
- Any bit in the following special registers: interrupt mask, serial mode high, timer mode, timer/event counter output control.

An addressed bit may be tested, set, cleared, or complemented. It also may be moved to or from the carry flag. An addressed bit may be ANDed, ORed, and XORed with the carry flag.

Figure 8. Watchdog Timer Block Diagram



Absolute Maximum Ratings

Power supply voltages,	V_{CC}	−0.5 V to +7.0 V
	V_{DD}	−0.5 V to +7.0 V
	AV_{CC}	−0.5 V to +7.0 V
Input voltage, V_I		−0.5 V to +7.0 V
Output voltage, V_O		−0.5 V to +7.0 V
Reference input threshold voltage, V_{RTH}		−0.5 V to V_{CC} +0.1V
Operating temperature, T_{OPR} 10 MHz ≤ f_{XTAL} ≤ 12 MHz		−10°C to +70°C
f_{XTAL} ≤ 10 MHz (μPD7807/09)		−10°C to +70°C
f_{XTAL} ≤ 10 MHz (μPD7808 only)		−40°C to +85°C
Storage temperature, T_{STG} (μPD7807/09)		−40°C to +125°C
Storage temperature, (μPD7808 only)		−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

Oscillating Frequency	T_A	V_{CC}, AV_{CC}
10 MHz ≤ f_{XTAL} ≤ 12 MHz	−10°C to +70°C	+5.0 V ± 5%
f_{XTAL} ≤ 10 MHz (μPD7807/09)	−10°C to +70°C	+5.0 V ± 10%
f_{XTAL} ≤ 10 MHz (μPD7808)	−40°C to −85°C	+5.0 V ± 10%

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Capacitance	C_I			10	pF	Af_c = 1 MHz.
Output capacitance	C_O			20	pF	Unmeasured pin returned to 0 V.
I/O capacitance	C_{IO}			20	pF	

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5.0 V ±10%; V_{SS} = 0 V; V_{CC} −0.8 V ≤ V_{DD} ≤ V_{CC}; T_A = −40°C to +85°C (μPD7808)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	0		0.8	V	
Input high voltage	V_{IH1}	2.0		V_{CC}	V	All except $\overline{SCK}$, $\overline{RESET}$, and X1
	V_{IH2}	0.8 V_{CC}		V_{CC}	V	$\overline{SCK}$, X1
	V_{IH3}	0.8 V_{DD}		V_{CC}	V	$\overline{RESET}$
Output low voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	2.4			V	I_{OH} = −200 μA
Input current	I_I			±200	μA	INT1, TI(PC_3); + 0.45 V ≤ V_{IN} ≤ V_{CC}
Input leakage current	I_{LI}			±10	μA	All except INT1, TI(PC_3) 0 V ≤ V_{IN} ≤ V_{CC}
Output leakage current	I_{LO}			±10	μA	+0.45 V ≤ V_O ≤ V_{CC}
V_{RTH} input current	I_{RTH}		0.2(1)	0.6	mA	V_{RTH} = V_{CC}
V_{DD} supply current	I_{DD}		1.5(1)	3.5	mA	
V_{CC} supply current	I_{CC}		150(1)	220	mA	

Note:

(1) T_A = 25°C: V_{CC} = V_{DD} = +5.0 V

Hold Operation

T_A = −10°C to +70°C; V_{CC} = +5.0 V ±10%; V_{SS} = 0 V; V_{CC} −0.8 V ≤ V_{DD} ≤ V_{CC}; T_A = −40°C to +85°C (μPD7808)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
HOLD ↑ setup time to ALE ↑	t_{SHDL}	2T + 150			ns	
ALE ↑ to HLDA ↑ delay	t_{DLHA}			T + 150	ns	
HLDA ↑ to bus floating	t_{FBHA}	0			ns	
HOLD ↓ to HLDA ↓ delay	t_{HDDA}	T − 50		4T + 150	ns	
HLDA ↓ to bus enable time	t_{EHAB}	0			ns	
Bus setup time to ALE	t_{BL}	2T − 100			ns	

Comparator Characterisctics

$T_A = -10°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$; $V_{SS} = 0\ V$; $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$; $T_A = -40°C$ to $+85°C$ (μPD7808)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Comparison accuracy	V_{ACOMP}			±100	mV	
Threshold voltage	V_{TH}	0		V_{CC}	V	
Comparison time	t_{COMP}	144		145	t_{CYC}	
PT input voltage	V_{IPT}	0		V_{CC}	V	

External Clock

$T_A = -10°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$; $V_{SS} = 0\ V$; $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$; $T_A = -40°C$ to $+85°C$ (μPD7808)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
High level width	$t_{\Phi H}$	30		250	ns	
Low level width	$t_{\Phi L}$	30		250	ns	
Rising time	t_r	0		30	ns	
Falling time	t_f	0		30	ns	

Data Retention Characteristics

$T_A = -10°C$ to $+70°C$; $V_{CC} = 0\ V$, $V_{DD} = V_{DDDR}$; $T_A = -40°C$ to $+85°C$ (μPD7808)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention voltage	V_{DDDR}	3.2		5.5	V	RESET = V_{IL}
Data retention supply current	I_{DDDR}		1.3	3.0	mA	RESET = V_{IL} $V_{DDDR} = 3.2\ V$

AC Characteristics

$V_{SS} = 0\ V$, $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$; See Operating Conditions table

Parameter	Symbol	Limits $f_{XTAL} = 10$ MHz Min	Max	$f_{XTAL} = 12$ MHz Min	Max	Unit	Test Conditions (1)
Read/Write Operation							
$\overline{RESET}$ pulse width	t_{RP}	6.0		5.0		μs	
Interrupt pulse width	t_{IP}	3.6		3.0		μs	
Counter input pulse width	t_{CI}	600		500		ns	Event counter mode
	t_{CI}	4.8		4.0		μs	Pulse width measurement mode
Timer input pulse width	t_{TI}	600		500		ns	
X1 Input cycle time	t_{CYC}	100	250	83	250	ns	
Address set-up to ALE ↓	t_{AL}	100		65		ns	
Address hold after ALE ↓	t_{LA}	70		50		ns	
Address to $\overline{RD}$ ↓ delay time	t_{AR}	200		150		ns	
$\overline{RD}$ ↓ to address floating	t_{AFR}		20		20	ns	
Address to data input	t_{AD}		480		360	ns	

Note:

(1) Load capacitance: $C_L = 150$ pF.

AC Characteristics (cont)

V_{SS} = 0 V, V_{CC} −0.8 V ≤ V_{DD} ≤ V_{CC}; See Operating Conditions table

Parameter	Symbol	Limits f_{XTAL} = 10 MHz Min	Limits f_{XTAL} = 10 MHz Max	Limits f_{XTAL} = 12 MHz Min	Limits f_{XTAL} = 12 MHz Max	Unit	Test Conditions (1)
Read/Write Operation							
ALE ↓ to data input	t_{LDR}		300		215	ns	
$\overline{RD}$ ↓ to data input	t_{RD}		250		180	ns	
ALE ↓ to $\overline{RD}$ ↓ delay time	t_{LR}	50		35		ns	
Data hold time to $\overline{RD}$ ↑	t_{RDH}	0		0		ns	
$\overline{RD}$ ↑ to ALE ↑ delay time	t_{RL}	150		115		ns	
$\overline{RD}$ width low	t_{RR}	350		280		ns	Data read
		650		530		ns	Opcode fetch
ALE width high	t_{LL}	160		125		ns	
$\overline{M1}$ setup time to ALE ↓	t_{ML}	100		65		ns	
$\overline{M1}$ hold time from ALE ↓	t_{LM}	70		50		ns	
$\overline{IO}$/M setup time to ALE ↓	t_{IL}	100		65		ns	
$\overline{IO}$/M hold time from ALE ↓	t_{LI}	70		50		ns	
Address to $\overline{WR}$ ↓ delay	t_{AW}	200		150		ns	
ALE ↓ to data output	t_{LDW}		210		195	ns	
$\overline{WR}$ ↓ to data output	t_{WD}		100		100	ns	
ALE ↓ to $\overline{WR}$ ↓ delay	t_{LW}	50		35		ns	
Data set-up time to $\overline{WR}$ ↑	t_{DW}	300		230		ns	
Data hold time to $\overline{WR}$ ↑	t_{WDH}	130		95		ns	
$\overline{WR}$ ↑ to ALE ↑ delay time	t_{WL}	150		115		ns	
$\overline{WR}$ width low	t_{WW}	350		280		ns	

Note:

(1) Load capacitance: C_L = 150 pF.

4

Serial Operation

See Operating Conditions table

Parameter	Symbol	Limits f_{XTAL} = 10 MHz Min	Limits f_{XTAL} = 10 MHz Max	Limits f_{XTAL} = 12 MHz Min	Limits f_{XTAL} = 12 MHz Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{CYK}	1.2		1		μs	$\overline{SCK}$ input (4)
		500		500		ns	$\overline{SCK}$ input (5)
		2.4		2		μs	$\overline{SCK}$ output
$\overline{SCK}$ width low	t_{KKL}	500(6)		400(7)		ns	$\overline{SCK}$ input(4)
		200		200		ns	$\overline{SCK}$ input (5)
		1100		900		ns	$\overline{SCK}$ output
$\overline{SCK}$ width high	t_{KKH}	500(6)		400(7)		ns	$\overline{SCK}$ input (4)
		200		200		ns	$\overline{SCK}$ input (5)
		1100		900		ns	$\overline{SCK}$ output
RxD set-up time to $\overline{SCK}$ ↑	t_{RXK}	80		80		ns	(4)
RxD hold time after $\overline{SCK}$ ↑	t_{KRX}	80		80		ns	(4)
$\overline{SCK}$ ↓ TxD delay time	t_{KTX}		210		210	ns	(4)

Note:

(4) 1x Baud rate in Asynchronous, Synchronous, or I/O Interface mode.

(5) 16x Baud rate or 64x Baud rate in Asynchronous mode.

(6) 505 ns min for μPD7808 only.

(7) 420 ns min for μPD7808 only.

Zero-Cross Characteristics

Parameter	Limits Symbol	Min	Typ	Max	Unit	Test Conditions
Zero-cross detection input	V_{ZX}	1		3(8)	VAC_{P-P}	AC coupled
Zero-cross accuracy	A_{ZX}			±135	mV	60 Hz sine wave
Zero-cross detection input frequency	f_{ZX}	0.05		1	kHz	

Note:

(8) 1.8 VAC_{p-p} max for μPD7808 only.

Bus Timing Depending on t_{CYC}

Symbol	Calculating Expression	Min/Max
t_{RP}	60T	Min
t_{TI}	6T	Min
t_{CI}(2)	6T	Min
t_{CI}(3)	48T	Min
t_{IP}	36T	Min
t_{AL}	2T − 100	Min
t_{LA}	T − 30	Min
t_{AR}	3T − 100	Min
t_{AD}	7T − 220(4)	Max
t_{LDR}	5T − 200(4)	Max
t_{RD}	4T − 150(4)	Max
t_{LR}	T − 50	Min
t_{RL}	2T − 50	Min
t_{RR}	4T − 50 (Data Read)(4)	Min
	7T − 50 (Opcode Fetch)(4)	
t_{LL}	2T − 40	Min
t_{ML}	2T − 100	Min
t_{LM}	T − 30	Min
t_{IL}	2T − 100	Min
t_{LI}	T − 30	Min

Bus Timing Depending on t_{CYC} (cont)

Symbol	Calculating Expression	Min/Max
t_{AW}	3T −100	Min
t_{LDW}	T + 110	Max
t_{LW}	T − 50	Min
t_{DW}	4T − 100(4)	Min
t_{WDH}	2T − 70	Min
t_{WL}	2T − 50	Min
t_{WW}	4T − 50(4)	Min
t_{CYK}	12T (SCK input)(1)	Min
	24T (SCK output)	
t_{KKL}	6T − 100 (SCK input)(1)(5)	Min
	12T − 100 (SCK output)	
t_{KKH}	6T − 100 (SCK input)(1)(5)	Min
	12T − 100 (SCK output)	

Note:

(1) 1x Baud rate in asynchronous, synchronous, or I/O interface mode.

$$T = t_{CYC} = \frac{1}{f_{XTAL}}$$

The items not included in this list are independent of oscillator frequency (f_{XTAL}).

(2) Event counter mode.

(3) Pulse width measurement mode.

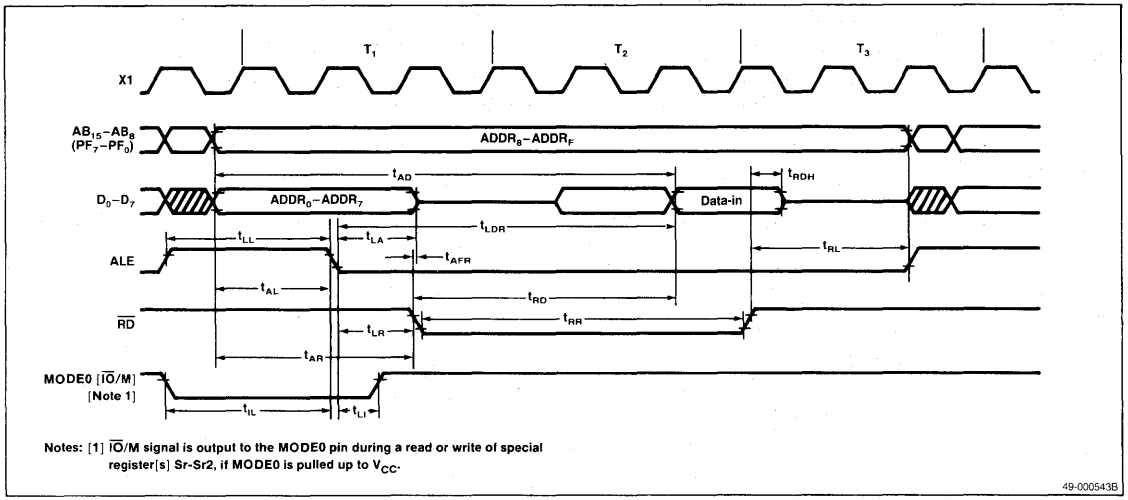
(4) Add 3T when using external program memory with programmable WAIT function.

(5) 5T+5 (SCK input)(1) min for μPD7808 only.

4

Timing Waveforms

Read Operation

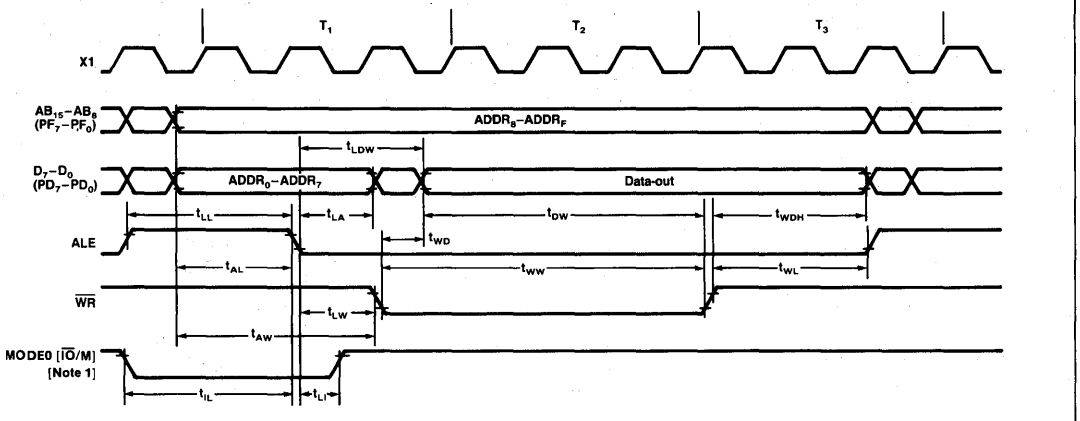


Notes: [1] IO/M signal is output to the MODE0 pin during a read or write of special register[s] Sr-Sr2, if MODE0 is pulled up to V_{CC}.

49-000543B

Timing Waveforms (cont)

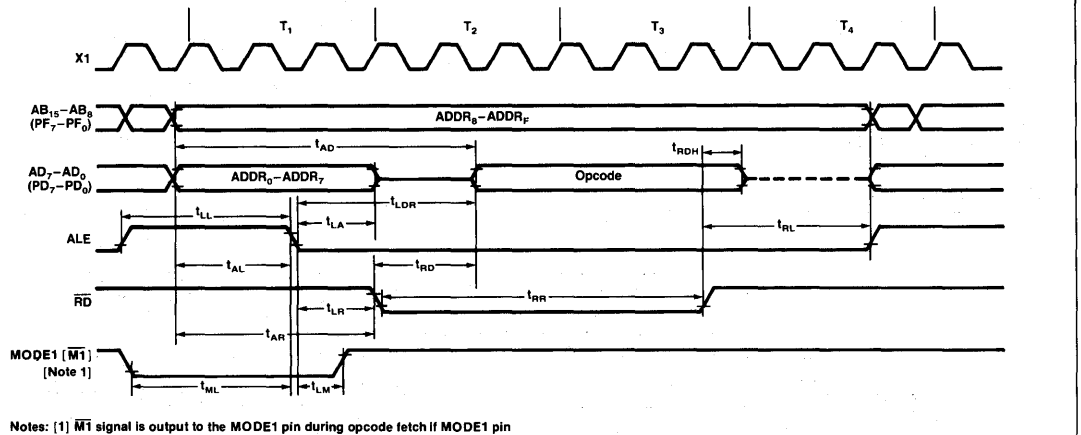
Write Operation



Notes: [1] $\overline{IO}$/M signal is output to the MODE0 pin during a read or write of special register[s] Sr-Sr2, if MODE0 is pulled up to V_{CC}.

49-000544B

Opcode Fetch Operation

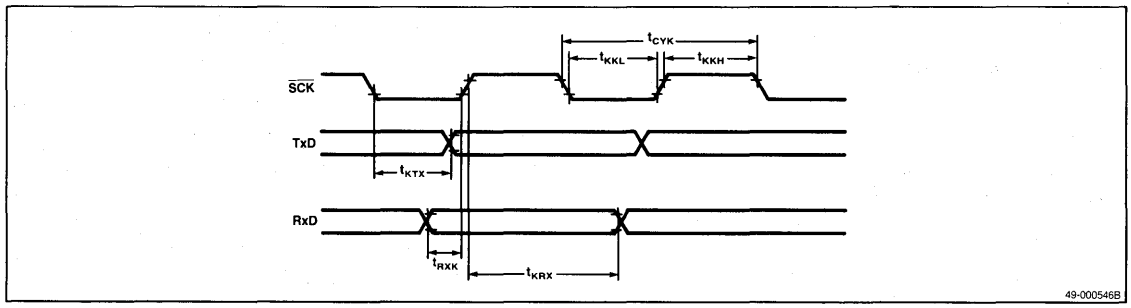


Notes: [1] $\overline{M1}$ signal is output to the MODE1 pin during opcode fetch if MODE1 pin is pulled up to V_{CC}.

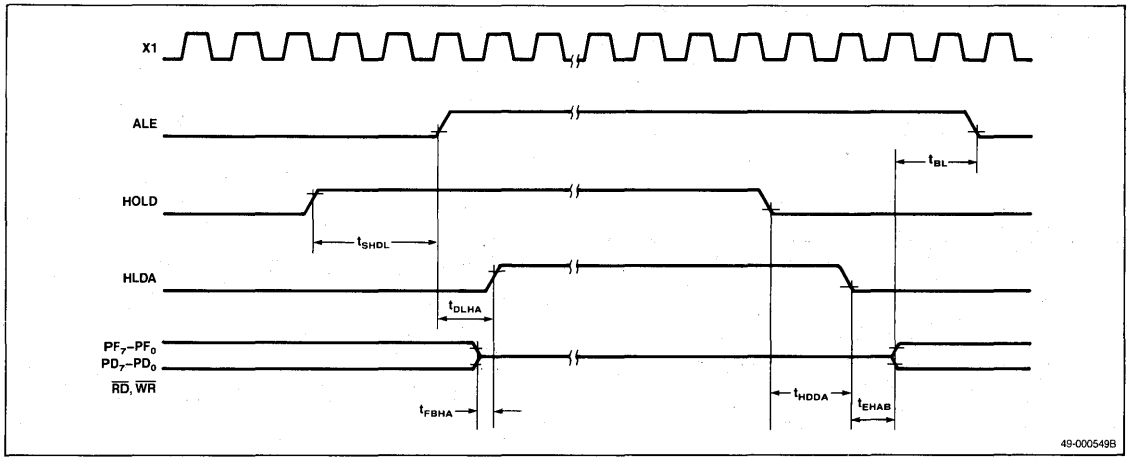
49-000545B

Timing Waveforms (cont)

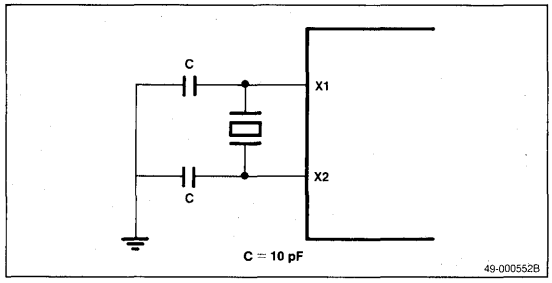
Serial Operation Transmit/Recieve Timing



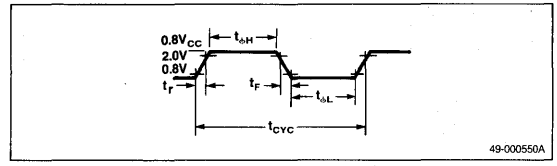
Hold Operation



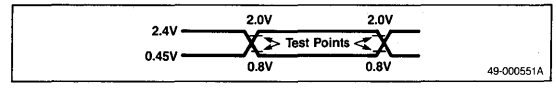
XTAL Oscillation Circuit



External Clock Timing



AC Timing Test Points



Instruction Set

In addition to the basic 7800 family instruction set, the μPD7807/08/09 executes the following types of instructions:

- ☐ 16-bit data transfers between memory, registers, and extended accumulator
- ☐ 16-bit addition and subtraction
- ☐ 16-bit comparison and skip
- ☐ 16-bit AND, OR, XOR operation
- ☐ 16-bit data shift and rotation
- ☐ Multiply; 8-bit by 8-bit, 16-bit product (less than 8 μs execution)
- ☐ Divide; 16-bit by 8-bit, 16-bit quotient, 8-bit remainder (less than 15 μs execution)
- ☐ Working register instruction for efficient RAM addressing, testing, and manipulating
- ☐ Direct bit addressing for code-efficient addressing, testing, and manipulating bits in RAM, port lines, and mode registers.

Operand Format/Description

Format	Description
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TxB, TM_0, TM_1, WDM, MT
sr1	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, RxB, PT, WDM
sr2	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM
sr3	ETM_0, ETM_1
sr4	ECNT, ECPT0, ECPT1
sr5	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, PT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D−, H−, D + byte, H + A, H + B, H + EA, H + byte
rpa3	D, H, D++, H++, D + byte, H + A, H + B, H + EA, H + byte
wa	8-Bit immediate data
word	16-Bit immediate data
byte	8-Bit immediate data
bit	8-Bit address of bit location
f	CY, HC, Z
irf	NMI, FT0, FT1, F1, F2, FE0, FE1, FEIN, FSR, FST, ER, OV, IFE2, SB

Instruction Set Symbol Definitions

Symbol	Description
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
∨̲	Exclusive OR
—	Complement
•	Concatenation

Remarks

1. sr-sr5 (special register)

PA = Port A	ECNT = Timer/Event Counter Upcounter
PB = Port B	ECPT0 = Timer/Event Counter Capture 0
PC = Port C	ECPT1 = Timer/Event Counter Capture 1
PD = Port D	ETMM = Timer/Event Counter Mode
PF = Port F	EOM = Timer/Event Counter Output Mode
PT = Port T	WDM = Watchdog Timer Mode
MA = Mode A	TxB = Tx Buffer
MB = Mode B	RxB = Rx Buffer
MC = Mode C	SMH = Serial Mode High
MCC = Mode Control C	SML = Serial Mode Low
MF = Mode F	MKH = Mask High
MT = Mode T	MKL = Mask Low
MM = Memory Mapping	
TM_0 = Timer Register 0	
TM_1 = Timer Register 1	
TMM = Timer Mode	
ETM_0 = Timer/Event Counter Register 0	
ETM_1 = Timer/Event Counter Register 1	

2. rp-rp3 (register pair)

SP = Stack Pointer	H = HL
B = BC	V = VA
D = DE	EA = Extended Accumulator

3. rpa-rpa3 (rp addressing)

B = (BC)	D++ = (DE) + 2
D = (DE)	H++ = (HL) + 2
H = (HL)	D + byte = (DE) + byte
D+ = (DE) + 1	H + A = (HL) + (A)
H− = (HL) + (B)	H + B = (HL) + (B)
D− = (DE) − 1	H + EA = (HL) + (EA)
H− = (HL) − 1	H + byte = (HL) + byte

4. f (flag)

CY = Carry	HC = Half Carry	Z = Zero

5. irf (interrupt flag)

NMI = NMI input	FEIN = INTFEIN
FT0 = INTFT0	FSR = INTFSR
FT1 = INTFT1	FST = INTFST
F1 = INTF1	ER = Error
F2 = INTF2	OV = Overflow
FE0 = INTFE0	IE2 = Interrupt Enable F/F2
FE1 = INTFE1	SB = Standby

Instruction Set

Mnemonic	Operand	Operation	Operation Code: 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Data Transfer													
MOV	r1,A	(r1) ← (A)	0	0	0	1	1	T_2	T_1	T_0	4	1	
	A, r1	(A) ← (r1)	0	0	0	0	1	T_2	T_1	T_0	4	1	
	*sr,A	(sr) ← (A)	0	1	0	0	1	1	0	1	10	2	
	*A,sr1	(A) ← (sr1)	0	1	0	0	1	1	0	0	10	2	
	r,word	(r) ← (word)	0	1	1	1	0	0	0	0	17	4	
			Low addr								High addr		
	word,r	(word) ← (r)	0	1	1	1	0	0	0	0	17	4	
			Low addr								High addr		
MVI	*r,byte	(r) ← byte set L1 if r = A set L0 if r = L	0	1	1	0	1	R_2	R_1	R_0	Data	7	2	L1 = 1 and r = A L0 = 1 and r = L
	sr2,byte	(sr2) ← byte	0	1	1	0	0	1	0	0	S_3 0 0 0 0 S_2 S_1 S_0	14	3	
			Data										
MVIW	*wa, byte	((V)•(wa)) ← byte	0	1	1	1	0	0	0	1	Offset	13	3	
			Data										
MVIX	*rpa1,byte	(rpa1) ← byte	0	1	0	0	1	0	A_1	A_0	Data	10	2	
STAW	*wa	((V)•(wa)) ← A	0	1	1	0	0	0	1	1	Offset	10	2	
LDAW	*wa	(A) ← ((V)•(wa))	0	0	0	0	0	0	0	1	Offset	10	2	
STAX	*rpa2	(rpa2) ← (A)	A_3	0	1	1	1	A_2	A_1	A_0	Data (2)	7/13(3)	2	
LDAX	rpa2	(A) ← ((rpa2))	A_3	0	1	0	1	A_2	A_1	A_0	Data (2)	7/13(3)	2	
EXX		(B) ↔ (B'),(C) ↔ (C'),(D) ↔ (D') (E) ↔ (E'),(H) ↔ (H'),(L) ↔ (L')	0	1	0	0	1	0	0	0	1 0 1 0 1 1 1 1	8	2	
EXA		(V) ↔ (V'),(A) ↔ (A'),(EA) ↔ (EA')	0	1	0	0	1	0	0	0	1 0 1 0 1 1 0 0	8	2	
EXH		(H) ↔ (H'),(L) ↔ (L')	0	1	0	0	1	0	0	0	1 0 1 0 1 1 1 0	8	2	
EXR		(V) ↔ (V'),(A) ↔ (A'),(B) ↔ (B'); (C) ↔ (C') (D) ↔ (D') (E) ↔ (E'),(H) ↔ (H'),(L) ↔ (L'),(EA) ↔ (EA')	0	1	0	0	1	0	0	0	1 0 1 0 1 1 0 1	8	2	
16-Bit Data Transfer													
BLOCK	D+	((DE)) ← ((HL)),(DE) ← (DE) + 1, (HL) ← (HL) + 1, (C) ← (C) − 1 End if borrow	0	0	0	1	0	0	0	0	13 x (C + 1)	1	
	D−	((DE)) ← (HL)),(DE) ← (DE) − 1, (HL) ← (HL) − 1, (C) ← (C) − 1 End if borrow	0	0	0	1	0	0	0	1	13 x (C + 1)	1	
DMOV	rp3, EA	($rp3_L$) ← (EAL),($rp3_H$) ← (EAH)	1	0	1	1	0	1	P_1	P_0	4	1	
	EA,rp3	(EAL) ← ($rp3_L$),(EAH) ← ($rp3_H$)	1	0	1	0	0	1	P_1	P_0	4	1	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	Operation Code B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
16-Bit Data Transfer (cont)																					
DMOV	sr3, EA	(sr3) ← (EA)	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1	U_0	14	2	
	EA,sr4	(EA) ← (sr4)	0	1	0	0	1	0	0	0	1	1	0	0	0	0	V_1	V_0	14	2	
SBCD	word	(word) ← (C), (word + 1) ← (B)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	20	4	
			Low addr								High addr										
SDED	word	(word) ← (E), (word + 1) ← (D)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	0	20	4	
			Low addr								High addr										
SHLD	word	(word) ← (L), (word + 1) ← (H)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	20	4	
			Low addr								High addr										
SSPD	word	(word) ← (SP_L),(word + 1) ← (SP_H)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	20	4	
			Low addr								High addr										
STEAX	rpa3	((rpa3)) ← (EAL),((rpa3)) + 1 ← (EAH)	0	1	0	0	1	0	0	0	1	0	0	1	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
LBCD	word	(C) ← (word),(B) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	20	4	
			Low addr								High addr										
LDED	word	(E) ← (word),(D) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	20	4	
			Low addr								High addr										
LHLD	word	(L) ← (word),(H) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	20	4	
			Low addr								High addr										
LSPD	word	(SP_L) ← (word),(SP_H) ← ((word) + 1)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	20	4	
			Low addr								High addr										
LDEAX	rpa3	(EAL) ← ((rpa3)),(EAH) ← ((rpa3) + 1)	0	1	0	0	1	0	0	0	1	0	0	0	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
PUSH	rp1	((SP) − 1) ← ($rp1_H$) ((SP) − 2) ← ($rp1_L$) (SP) ← (SP) − 2	1	0	1	1	0	Q_2	Q_1	Q_0									13	1	
POP	rp1	($rp1_L$) ← ((SP)),($rp1_H$) ← ((SP) + 1) (SP) ← (SP) + 2	1	0	1	0	0	Q_2	Q_1	Q_0									10	1	
LXI	*rp2,word	(rp2) ← (word) set L0 if rp2 = H	0	P_2	P_1	P_0	0	1	0	0	Low byte								10	3	L0 = 1 and rp2 = H
			High byte																		
TABLE		(C) ← ((PC)+3+(A)),B ← ((PC)+3+(A)+ 1)	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	0	17	2	
8-Bit Arithmetic [Register]																					
ADD	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	1	0	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	1	0	0	0	R_2	R_1	R_0	8	2	
ADC	A,r	(A) ← (A) + (r) + (CY)	0	1	1	0	0	0	0	0	1	1	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A) + (CY)	0	1	1	0	0	0	0	0	0	1	0	1	0	R_2	R_1	R_0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 7	6	5	B3 4	3	2	1	0	B2 7	6	5	B4 4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Arithmetic [Register] (cont)																					
ADDNC	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	0	1	0	0	R_2	R_1	R_0	8	2	No carry
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	0	1	0	0	R_2	R_1	R_0	8	2	No carry
SUB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	0	R_2	R_1	R_0	8	2	
SBB	A,r	(A) ← (A) − (r) − (CY)	0	1	1	0	0	0	0	0	1	1	1	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A) − (CY)	0	1	1	0	0	0	0	0	0	1	1	1	0	R_2	R_1	R_0	8	2	
SUBNB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
ANA	A,r	(A) ← (A) ∧ (r)	0	1	1	0	0	0	0	0	1	0	0	0	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∧ (A)	0	1	1	0	0	0	0	0	0	0	0	0	1	R_2	R_1	R_0	8	2	
ORA	A,r	(A) ← (A) ∨ (r)	0	1	1	0	0	0	0	0	1	0	0	1	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∨ (A)	0	1	1	0	0	0	0	0	0	0	0	1	1	R_2	R_1	R_0	8	2	
XRA	A,r	(A) ← (A) ∀ (r)	0	1	1	0	0	0	0	0	1	0	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∀ (A)	0	1	1	0	0	0	0	0	0	0	0	1	0	R_2	R_1	R_0	8	2	
GTA	A,r	(A) − (r) − 1	0	1	1	0	0	0	0	0	1	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) − (A) − 1	0	1	1	0	0	0	0	0	0	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
LTA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
NEA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	1	R_2	R_1	R_0	8	2	No zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	8	2	No zero
EQA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	1	1	R_2	R_1	R_0	8	2	Zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	8	2	Zero
ONA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	0	1	R_2	R_1	R_0	8	2	No zero
OFFA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	1	1	R_2	R_1	R_0	8	2	Zero
8-Bit Arithmetic (Memory)																					
ADDX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	0	A_2	A_1	A_0	11	2	
ADCX	rpa	(A) ← (A) + ((rpa)) + (CY)	0	1	1	1	0	0	0	0	1	1	0	1	0	A_2	A_1	A_0	11	2	
ADDNCX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	0	1	0	0	A_2	A_1	A_0	11	2	No carry
SUBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	0	A_2	A_1	A_0	11	2	
SBBX	rpa	(A) ← (A) − ((rpa)) − (CY)	0	1	1	1	0	0	0	0	1	1	1	1	0	A_2	A_1	A_0	11	2	
SUBNBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	0	A_2	A_1	A_0	11	2	No borrow
ANAX	rpa	(A) ← (A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	0	1	A_2	A_1	A_0	11	2	
ORAX	rpa	(A) ← (A) ∨ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	1	A_2	A_1	A_0	11	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 B3 7	6	5	4	3	2	1	0	B2 B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Arithmetic (Memory) (cont)																					
XRAX	rpa	(A) ← (A) ∀ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	0	A_2	A_1	A_0	11	2	
GTAX	rpa	(A) – ((rpa)) – 1	0	1	1	1	0	0	0	0	1	0	1	0	1	A_2	A_1	A_0	11	2	No borrow
LTAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	1	A_2	A_1	A_0	11	2	Borrow
NEAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	1	A_2	A_1	A_0	11	2	No zero
EQAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	1	1	A_2	A_1	A_0	11	2	Zero
ONAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	1	A_2	A_1	A_0	11	2	No zero
OFFAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	1	1	A_2	A_1	A_0	11	2	Zero
Immediate Data																					
ADI	*A,byte	(A) ← (A) + byte	0	1	0	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	1	0	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2, byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	1	0	0	0	S_2	S_1	S_0	20	3	
			Data																		
ACI	*A,byte	(A) ← (A) + byte + (CY)	0	1	0	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte + (CY)	0	1	1	1	0	1	0	0	0	1	0	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte + (CY)	0	1	1	0	0	1	0	0	S_3	1	0	1	0	S_2	S_1	S_0	20	3	
			Data																		
ADINC	*A,byte	(A) ← (A) + byte	0	0	1	0	0	1	1	0	Data								7	2	No carry
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	0	1	0	0	R_2	R_1	R_0	11	3	No carry
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	0	1	0	0	S_2	S_1	S_0	20	3	No carry
			Data																		
SUI	*A,byte	(A) ← (A) – byte	0	1	1	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte	0	1	1	1	0	1	0	0	0	1	1	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte	0	1	1	0	0	1	0	0	S_3	1	1	0	0	S_2	S_1	S_0	20	3	
			Data																		
SBI	*A,byte	(A) ← (A) – byte – (CY)	0	1	1	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte – (CY)	0	1	1	1	0	1	0	0	0	1	1	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte – (CY)	0	1	1	0	0	1	0	0	S_3	1	1	1	0	S_2	S_1	S_0	20	3	
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 7	6	5	4	B3 3	2	1	0	B2 7	6	5	B4 4	3	2	1	0	State(1)	Bytes	Skip Condition
Immediate Data (cont)																					
SUINB	*A,byte	(A) ← (A) − byte	0	0	1	1	0	1	1	0				Data					7	2	No borrow
	r,byte	(r) ← (r) − byte	0	1	1	1	0	1	0	0	0	0	1	1	0	R_2	R_1	R_0	11	3	No borrow
			Data																		
	sr2,byte	(sr2) ← (sr2) − byte	0	1	1	0	0	1	0	0	S_3	0	1	1	0	S_2	S_1	S_0	20	3	No borrow
			Data																		
ANI	*A,byte	(A) ← (A) ∧ byte	0	0	0	0	0	1	1	1				Data					7	2	
	r,byte	(r) ← (r) ∧ byte	0	1	1	1	0	1	0	0	0	0	0	0	1	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) ∧ byte	0	1	1	0	0	1	0	0	S_3	0	0	0	1	S_2	S_1	S_0	20	3	
			Data																		
ORI	*A,byte	(A) ← (A) V byte	0	0	0	1	0	1	1	1				Data					7	2	
	r,byte	(r) ← (r) V byte	0	1	1	1	0	1	0	0	0	0	0	1	1	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) V byte	0	1	1	0	0	1	0	0	S_3	0	0	1	1	S_2	S_1	S_0	20	3	
			Data																		
XRI	*A,byte	(A) ← (A) ∀ byte	0	0	0	1	0	1	1	0				Data					7	2	
	r,byte	(r) ← (r) ∀ byte	0	1	1	1	0	1	0	0	0	0	0	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) ∀ byte	0	1	1	0	0	1	0	0	S_3	0	0	1	0	S_2	S_1	S_0	20	3	
			Data																		
GTI	*A,byte	(A) − byte − 1	0	0	1	0	0	1	1	1				Data					7	2	No borrow
	r,byte	(r) − byte − 1	0	1	1	1	0	1	0	0	0	0	1	0	1	R_2	R_1	R_0	11	3	No borrow
			Data																		
	sr5,byte	(sr5) − byte − 1	0	1	1	0	0	1	0	0	S_3	0	1	0	1	S_2	S_1	S_0	14	3	No borrow
			Data																		
LTI	*A,byte	(A) − byte	0	0	1	1	0	1	1	1				Data					7	2	Borrow
	r,byte	(r) − byte	0	1	1	1	0	1	0	0	0	0	1	1	1	R_2	R_1	R_0	11	3	Borrow
			Data																		
	sr5,byte	(sr5) − byte	0	1	1	0	0	1	0	0	S_3	0	1	1	1	S_2	S_1	S_0	14	3	Borrow
			Data																		
NEI	*A,byte	(A) − byte	0	1	1	0	0	1	1	1				Data					7	2	No zero
	r,byte	(r) − byte	0	1	1	1	0	1	0	0	0	1	1	0	1	R_2	R_1	R_0	11	3	No zero
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
Immediate Data (cont)																					
NEI	sr5,byte	(sr5) – byte	0	1	1	0	0	1	0	0	S_3	1	1	0	1	S_2	S_1	S_0	14	3	No zero
			Data																		
EQI	*A,byte	(A) – byte	0	1	1	1	0	1	1	1	Data								7	2	Zero
	r,byte	(r) – byte	0	1	1	1	0	1	0	0	0	1	1	1	1	R_2	R_1	R_0	11	3	Zero
			Data																		
	sr5,byte	(sr5) – byte	0	1	1	0	0	1	0	0	S_3	1	1	1	1	S_2	S_1	S_0	14	3	Zero
			Data																		
ONI	*A,byte	(A) ∧ byte	0	1	0	0	0	1	1	1	Data								7	2	No zero
	r,byte	(r) ∧ byte	0	1	1	1	0	1	0	0	0	1	0	0	1	R_2	R_1	R_0	11	3	No zero
			Data																		
	sr5,byte	(sr5) ∧ byte	0	1	1	0	0	1	0	0	S_3	1	0	0	1	S_2	S_1	S_0	14	3	No zero
			Data																		
OFFI	*A,byte	(A) ∧ byte	0	1	0	1	0	1	1	1	Data								7	2	Zero
	r,byte	(r) ∧ byte	0	1	1	1	0	1	0	0	0	1	0	1	1	R_2	R_1	R_0	11	3	Zero
			Data																		
	sr5,byte	(sr5) ∧ byte	0	1	1	0	0	1	0	0	S_3	1	0	1	1	S_2	S_1	S_0	14	3	Zero
			Data																		
Working Register																					
ADDW	wa	(A) ← (A) + ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	0	0	0	0	0	14	3	
			Offset																		
ADCW	wa	(A) ← (A) + ((V)•(wa)) + (CY)	0	1	1	1	0	1	0	0	1	1	0	1	0	0	0	0	14	3	
			Offset																		
ADDNCW	wa	(A) ← (A) + ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	14	3	No carry
			Offset																		
SUBW	wa	(A) ← (A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	0	0	0	0	0	14	3	
			Offset																		
SBBW	wa	(A) ← (A) – ((V)•(wa)) – (CY)	0	1	1	1	0	1	0	0	1	1	1	1	0	0	0	0	14	3	
			Offset																		
SUBNBW	wa	(A) ← (A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	1	0	0	0	0	14	3	No borrow
			Offset																		
ANAW	wa	(A) ← (A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	0	1	0	0	0	14	3	
			Offset																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7 6 5 4 3 2 1 0	Operation Code B2/B4 7 6 5 4 3 2 1 0	State(1)	Bytes	Skip Condition
Working Register (cont)							
ORAW	wa	(A) ← (A) V ((V)•(wa))	0 1 1 1 0 1 0 0	1 0 0 1 0 0 0 0	14	3	
			Offset				
XRAW	wa	(A) ← (A) V ((V)•(wa))	0 1 1 1 0 1 0 0	1 0 0 1 0 0 0 0	14	3	
			Offset				
GTAW	wa	(A) – ((V)•(wa)) – 1	0 1 1 1 0 1 0 0	1 0 1 0 1 0 0 0	14	3	No borrow
			Offset				
LTAW	wa	(A) – ((V)•(wa))	0 1 1 1 0 1 0 0	1 0 1 1 0 0 0 0	14	3	Borrow
			Offset				
NEAW	wa	(A) – ((V)•(wa))	0 1 1 1 0 1 0 0	1 1 1 0 0 0 0 0	14	3	No zero
			Offset				
EQAW	wa	(A) – ((V)•(wa))	0 1 1 1 0 1 0 0	1 1 1 1 0 0 0 0	14	3	Zero
			Offset				
ONAW	wa	(A) ∧ ((V)•(wa))	0 1 1 1 0 1 0 0	1 1 0 0 0 0 0 0	14	3	No zero
			Offset				
OFFAW	wa	(A) ∧ ((V)•(wa))	0 1 1 1 0 1 0 0	1 1 0 1 0 0 0 0	14	3	Zero
			Offset				
ANIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) ∧ byte	0 0 0 0 0 1 0 1	Offset	19	3	
			Data				
ORIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) V byte	0 0 0 1 0 1 0 1	Offset	19	3	
			Data				
GTIW	*wa,byte	((V)•(wa)) – byte – 1	0 0 1 0 0 1 0 1	Offset	13	3	No borrow
			Data				
LTIW	*wa,byte	((V)•(wa)) – byte	0 0 1 1 0 1 0 1	Offset	13	3	Borrow
			Data				
NEIW	*wa,byte	((V)•(wa)) – byte	0 1 1 0 0 1 0 1	Offset	13	3	No zero
			Data				
EQIW	*wa,byte	((V)•(wa)) – byte	0 1 1 1 0 1 0 1	Offset	13	3	Zero
			Data				
ONIW	*wa,byte	((V)•(wa)) ∧ byte	0 1 0 0 0 1 0 1	Offset	13	3	No zero
			Data				
OFFIW	*wa,byte	((V)•(wa)) ∧ byte	0 1 0 1 0 1 0 1	Offset	13	3	Zero
			Data				

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code																State(1)	Bytes	Skip Condition
			7	6	5	4	B1 B3	2	1	0	7	6	5	B2 B4	3	2	1	0			
16-Bit Arithmetic																					
EADD	EA,r2	(EA) ← (EA) + (r2)	0	1	1	1	0	0	0	0	0	1	0	0	0	0	R_1	R_0	11	2	
DADD	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	0	1	P_1	P_0	11	2	
DADC	EA,rp3	(EA) ← (EA) + (rp3) + (CY)	0	1	1	1	0	1	0	0	1	1	0	1	0	1	P_1	P_0	11	2	
DADDNC	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	0	1	0	0	1	P_1	P_0	11	2	No carry
ESUB	EA,r2	(EA) ← (EA) − (r2)	0	1	1	1	0	0	0	0	0	1	1	0	0	0	R_1	R_0	11	2	
DSUB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	0	1	P_1	P_0	11	2	
DSBB	EA,rp3	(EA) ← (EA) − (rp3) − (CY)	0	1	1	1	0	1	0	0	1	1	1	1	0	1	P_1	P_0	11	2	
DSUBNB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	0	1	P_1	P_0	11	2	No borrow
DAN	EA,rp3	(EA) ← (EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	0	0	0	1	1	P_1	P_0	11	2	
DOR	EA,rp3	(EA) ← (EA) ∨ (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	1	1	P_1	P_0	11	2	
DXR	EA,rp3	(EA) ← (EA) ⊻ (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	0	1	P_1	P_0	11	2	
DGT	EA,rp3	(EA) − (rp3) − 1	0	1	1	1	0	1	0	0	1	0	1	0	1	1	P_1	P_0	11	2	No borrow
DLT	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	1	1	P_1	P_0	11	2	Borrow
DNE	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	1	1	P_1	P_0	11	2	No zero
DEQ	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	1	1	1	P_1	P_0	11	2	Zero
DON	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	1	1	P_1	P_0	11	2	No zero
DOFF	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	1	1	1	P_1	P_0	11	2	Zero
Multiply/Divide																					
MUL	r2	(EA) ← (A) x (r2)	0	1	0	0	1	0	0	0	0	0	1	0	1	1	R_1	R_0	32	2	
DIV	r2	(EA) ← (EA) ÷ (r2), (r2) ← Remainder	0	1	0	0	1	0	0	0	0	0	1	1	1	1	R_1	R_0	59	2	
Increment/Decrement																					
INR	r2	(r2) ← (r2) + 1	0	1	0	0	0	0	R_1	R_0									4	1	Carry
INRW	*wa	((V)•(wa)) ← ((V)•(wa)) + 1	0	0	1	0	0	0	0	0				Offset					16	2	Carry
INX	rp	(rp) ← (rp) + 1	0	0	P_1	P_0	0	0	1	0									7	1	
	EA	(EA) ← (EA) + 1	1	0	1	0	1	0	0	0									7	1	
DCR	r2	(r2) ← (r2) − 1	0	1	0	1	0	0	R_1	R_0									4	1	Borrow
DCRW	wa	((V)•(wa)) ← ((V)•(wa)) − 1	0	0	1	1	0	0	0	0				Offset					16	2	Borrow
DCX	rp	(rp) ← (rp) − 1	0	0	P_1	P_0	0	0	1	1									7	1	
	EA	(EA) ← (EA) − 1	1	0	1	0	1	0	0	1									7	1	
Others																					
DAA		Decimal Adjust Accumulator	0	1	1	0	0	0	0	1									4	1	
STC		(CY) ← 1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	8	2	
CLC		(CY) ← 0	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	0	8	2	
CMC		(CY) ← $\overline{(CY)}$	0	1	0	0	1	0	0	0	1	0	1	0	1	0	1	0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Others (cont)																					
NEGA		(A) ← (A) + 1	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	0	8	2	
Rotate and Shift																					
RLD		Rotate left digit	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	17	2	
RRD		Rotate right digit	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	1	17	2	
RLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow (CY)$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	1	1	0	1	R_1	R_0	8	2	
RLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$, $(r2_7) \leftarrow (CY)$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	1	1	0	0	R_1	R_0	8	2	
SLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	1	0	0	1	R_1	R_0	8	2	
SLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$, $(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	1	0	0	0	R_1	R_0	8	2	
SLLC	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	0	0	0	1	R_1	R_0	8	2	Carry
SLRC	r2	$(r2_{m-1}) \leftarrow (r2_m)$, $(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	R_1	R_0	8	2	Carry
DRLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$, $(EA_0) \leftarrow (CY)$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	1	0	1	1	0	1	0	0	8	2	
DRLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$, $(EA_{15}) \leftarrow (CY)$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	1	0	1	1	0	0	0	0	8	2	
DSLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$, $(EA_0) \leftarrow 0$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	8	2	
DSLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$, $(EA_{15}) \leftarrow 0$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	8	2	
Jump																					
JMP	*word	(PC) ← word	0	1	0	1	0	1	0	0	Low addr								10	3	
			High addr																		
JB		$(PC_H) \leftarrow (B)$, $(PC_L) \leftarrow (C)$	0	0	1	0	0	0	0	1									4	1	
JR	word	(PC) ← (PC) + 1 + jdisp 1	1	1	← jdisp1 →														10	1	
JRE	*word	(PC) ← (PC) + 2 + jdisp	0	1	0	0	1	1	1	← jdisp →									10	2	
JEA		(PC) ← (EA)	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	0	8	2	
Call																					
CALL	*word	$((SP)-1) \leftarrow ((PC)+3)_H$, $((SP)-2) \leftarrow ((PC)+3)_L$, (PC) ← word, (SP) ← (SP) − 2	0	1	0	0	0	0	0	0	Low addr								16	3	
			High addr																		
CALB		$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_H) \leftarrow (B)$ $(PC_L) \leftarrow (C)$, (SP) ← (SP) − 2	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	1	17	2	
CALF	*word	$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_{15\text{-}11}) \leftarrow 00001$, $(PC_{10\text{-}0}) \leftarrow fa$, (SP) ← (SP) − 2	0	1	1	1	1	← fa →											13	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code 7	6	5	B1/B3 4	3	2	1	0	B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Call (cont)																					
CALT	word	$((SP)-1) \leftarrow ((PC)+1)_H$, $((SP)-2) \leftarrow ((PC)+1)_L$ $(PC_L) \leftarrow (128+2ta)$,$(PC_H) \leftarrow$ $(129+2ta)$,$(SP) \leftarrow (SP)-2$	1	0	0	←	ta			→									16	1	
SOFTI		$((SP)-1) \leftarrow (PSW)$,$((SP)-2) \leftarrow$ $((PC)+1)_H$,$((SP)-3) \leftarrow ((PC)+1)_L$, $(PC) \leftarrow 0060H$,$(SP) \leftarrow (SP)-3$	0	1	1	1	0	0	1	0									16	1	
Return																					
RET		$(PC_L) \leftarrow ((SP))$,$(PC_H) \leftarrow ((SP)+1)$ $(SP) \leftarrow (SP)+2$	1	0	1	1	1	0	0	0									10	1	
RETS		$(PC_L) \leftarrow ((SP))$,$(PC_H) \leftarrow ((SP)+1)$ $(SP) \leftarrow (SP)+2$,$(PC) \leftarrow (PC)+n$	1	0	1	1	1	0	0	1									10	1	Unconditional Skip
RETI		$(PC_L) \leftarrow ((SP))$,$(PC_H) \leftarrow ((SP)+1)$ $(PSW) \leftarrow ((SP)+2)$, $(SP) \leftarrow (SP)+3$	0	1	1	0	0	0	1	0									13	1	
Bit Manipulation																					
MOV	*CY, bit	$(CY) \leftarrow (bit)$	0	1	0	1	1	1	1	1				Bit Addr					10	2	
	*bit CY	$(bit) \leftarrow (CY)$	0	1	0	1	1	0	1	0				Bit Addr					13	2	
AND	*CY,bit	$(CY) \leftarrow (CY) \wedge (bit)$	0	0	1	1	0	0	0	1				Bit Addr					10	2	
OR	*CY, bit	$(CY) \leftarrow (CY) \vee bit$	0	1	0	1	1	1	0	0				Bit Addr					10	2	
XOR	*CY, bit	$(CY) \leftarrow (CY) \veebar (bit)$	0	1	0	1	1	1	1	0				Bit Addr					10	2	
SETB	*bit	$(bit) \leftarrow 1$	0	1	0	1	1	0	0	0				Bit Addr					13	2	
CLR	*bit	$(bit) \leftarrow 0$	0	1	0	1	1	0	1	1				Bit Addr					13	2	
NOT	*bit	$(bit) \leftarrow \overline{(bit)}$	0	1	0	1	1	0	0	1				Bit Addr					13	2	
SK	*bit	Skip if (bit) = 1	0	1	0	1	1	1	0	1				Bit Addr					10	2	(bit) = 1
SKN	*bit	Skip if (bit) = 0	0	1	0	1	0	0	0	0				Bit Addr					10	2	(bit) = 0

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
CPU Control																					
SK	f	Skip if f = 1	0	1	0	0	1	0	0	0	0	0	0	0	1	F_2	F_1	F_0	8	2	f = 1
SKN	f	Skip if f = 0	0	1	0	0	1	0	0	0	0	0	0	1	1	F_2	F_1	F_0	8	2	f = 0
SKIT	irf	Skip if irf = 1, then reset irf	0	1	0	0	1	0	0	0	0	1	0	I_4	I_3	I_2	I_1	I_0	8	2	irf = 1
SKNIT	irf	Skip if irf = 0 Reset irf if irf = 1	0	1	0	0	1	0	0	0	0	1	1	I_4	I_3	I_2	I_1	I_0	8	2	irf = 0
NOP		No operation	0	0	0	0	0	0	0	0									4	1	
EI		Enable interrupt	1	0	1	0	1	0	1	0									4	1	
DI		Disable interrupt	1	0	1	1	1	0	1	0									4	1	
HLT		Halt	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	1	11	2	

Notes:

(1) In the case of skip condition, the idle states are as follows:

1-byte instruction: 4 states	2-byte instruction (with *): 7 states
2-byte instruction: 8 states	3-byte instruction (with *): 10 states
3-byte instruction: 11 states	4-byte instruction: 14 states

(2) B2 (Data): rpa2 = D + byte, H + byte

(3) Right side of slash (/) in states indicates case rpa2, rpa3 = D + byte, H + A, H + B, H + EA, H + byte

(4) B3 (Data): rpa3 = D + byte, H + byte

NEC
NEC Electronics Inc.

μPD78P09
HIGH-END, 8-BIT, SINGLE-CHIP NMOS MICROCOMPUTER WITH COMPARATOR AND 8K EPROM

Description

The μPD78P09 single-chip microcomputer augments the high-end NEC family of 8-bit microcomputers with on-chip peripheral functions. Like the μPD7809, the device has a fast internal 16-bit ALU and data paths, 256 bytes of RAM, a multifunctional 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs.

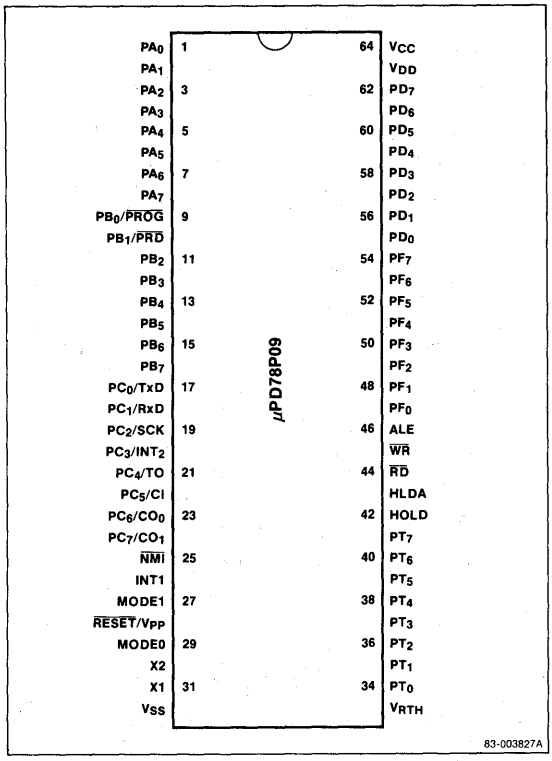
Other features are 8K EPROM, a programmable threshold comparator (8 inputs), a programmable WAIT function, a watchdog timer, hold and hold acknowledge for DMA interfaces, and bit test/write instructions for both RAM and I/O.

The μPD78P09 is a monolithic EPROM version of the μPD7809. It can be used for prototyping μPD7809 and μPD7808 applications.

Features

- ☐ NMOS silicon gate technology requiring +5 V power supply
- ☐ Complete single-chip microcomputer
  - — 16-bit ALU
  - — 8K EPROM
  - — 256-byte RAM
- ☐ Large I/O capability
  - — 40 I/O port lines
- ☐ Two zero-cross detect inputs
- ☐ Expansion capabilities (64K memory access total)
  - — 8085A bus-compatible
  - — 56K-byte external memory address range
  - — (60K for the μPD7808)
- ☐ Programmable threshold comparator
  - — Eight inputs, 16 software-selectable reference levels
- ☐ Full duplex USART
  - — Synchronous and asynchronous
- ☐ 165 instructions
  - — 16-bit arithmetic, multiply and divide
- ☐ 1 μs instruction cycle time
- ☐ Prioritized interrupt structure
  - — Three external
  - — Eight internal
- ☐ Hold, hold acknowledge for DMA interface
- ☐ Programmable WAIT function
- ☐ Watchdog timer
- ☐ Standby function
- ☐ On-chip clock generator
- ☐ 64-pin ceramic QUIP

Pin Configuration



Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD78P09R	64-pin ceramic QUIP with quartz window	12 MHz

Pin Identification

No.	Symbol	Function
1-8	PA_0-PA_7	Port A I/O
9-16	PB_0-PB_7/ $\overline{PROG}$/$\overline{PRD}$	Port B I/O
17	PC_0/TxD	Port C I/O line 0/Transmit data output
18	PC_1/RxD	Port C I/O line 1/Receive data input
19	PC_2/$\overline{SCK}$	Port C I/O line 2/Serial clock I/O
20	PC_3/TI/ $\overline{INT2}$	Port C I/O line 3/Timer input/Interrupt request 2 input
21	PC_4/TO	Port C I/O line 4/Timer output
22	PC_5/CI	Port C I/O line 5/Counter input
23, 24	PC_6, PC_7/ CO_0, CO_1	Port C I/O lines 6, 7/Counter outputs 0, 1
25	$\overline{NMI}$	Nonmaskable interrupt input
26	INT1	Interrupt request 1 input
27	MODE1	Mode 1 input/memory cycle 1 output
28	$\overline{RESET}$/V_{PP}	Reset input/V_{PP} input
29	MODE0	Mode 0 input/I/O/memory output
30, 31	X2, X1	Crystal connections 1, 2
32	V_{SS}	Ground
33	V_{RTH}	Port T threshold voltage input
34-41	PT_0-PT_7	Port T variable threshold input port
42	HOLD	Hold request input
43	HLDA	Hold acknowledge output
44	$\overline{RD}$	Read strobe output
45	$\overline{WR}$	Write strobe output
46	ALE	Address latch enable output
47-54	PF_0-PF_7	Port F I/O
55-62	PD_0-PD_7	Port D I/O
63	V_{DD}	RAM backup power supply
64	V_{CC}	5 V power supply

Pin Functions

PA_0-PA_7 [Port A]

Port A is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port A inputs. Port A inputs the low 8 bits of the address during EPROM programming/reading.

PB_0-PB_7 [Port B]

Port B is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port B inputs. PB_0 inputs the $\overline{PROG}$ signal during EPROM programming; PB_1 inputs $\overline{PRD}$ when the EPROM is programmed or read.

PC_0-PC_7 [Port C]

Port C is an 8-bit three-state port. Each bit is independently programmable as either input or output. Alternatively, the lines of port C can be used as control lines for the USART and timer. Reset puts all lines of port C in port mode as input lines.

TxD [Transmit Data]. Serial data output terminal.

RxD [Receive Data]. Serial data input terminal.

$\overline{SCK}$ [Serial Clock]. Output for the serial clock when internal clock is used. Input for serial clock when external clock is used.

TI [Timer Input]. Timer input terminal.

$\overline{INT2}$ [Interrupt Request 2]. Falling-edge-triggered, maskable interrupt input terminal and AC-input, zero-cross detection terminal.

TO [Timer Output]. The output of TO is a square wave with a frequency determined by the timer.

CI [Counter Input]. External pulse input to timer/event counter.

CO_0, CO_1 [Counter Outputs 0, 1]. Programmable rectangular-wave outputs based on timer/event counter.

PD_0-PD_7 [Port D]

Port D is an 8-bit three-state port. It can be programmed as either 8 bits of input or 8 bits of output. When external expansion memory is used, port D acts as the multiplexed address/data bus.

PF_0-PF_7 [Port F]

Port F is an 8-bit three-state port. Each bit is independently programmable as an input or output. When external expansion memory is used, port F outputs the high-order address bits; it inputs the high-order address bits during EPROM programming.

PT_0-PT_7 [Port T]

Port T is made up of eight variable threshold inputs. The input of each line is compared to a threshold voltage.

V_{RTH} [Variable Threshold Reference Voltage]

V_{RTH} is the reference voltage that the port T threshold voltage is derived from.

$\overline{NMI}$ [Nonmaskable Interrupt]

Falling-edge-triggered nonmaskable interrupt input.

INT1 [Interrupt Request 1]

INT1 is a rising-edge-triggered, maskable interrupt input. It is also an AC-input, zero-cross detection terminal. It can also latch contents of the 16-bit timer/event counter into the ECPT1 capture register.

$\overline{RESET}$ [Reset]

When the $\overline{RESET}$ input is brought low, it initializes the μPD78P09.

MODE1, MODE0 [Mode 1, 0]

The MODE1 and MODE0 inputs set the operating mode to either program read EPROM or normal operation (see table 1.)

Table 1. Operating Mode Selection

Mode 1	Mode 0	Operation
0	0	EPROM program/read
0	1	Reserved
1	0	Normal operation
1	1	Outputs control signals synchronized with ALE

HOLD [Hold Request]

When the HOLD input is high, the CPU is put in a hold state until HOLD is brought low.

HLDA [Hold Acknowledge]

The CPU brings the HLDA output high when it is in the hold state, and low when the hold is released.

$\overline{RD}$ [Read Strobe]

The $\overline{RD}$ output goes low to gate data from external devices onto the data bus. $\overline{RD}$ goes high during reset. Three-state.

$\overline{WR}$ [Write Strobe]

The $\overline{WR}$ output goes low to indicate that the data bus holds valid data. It is a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during reset. Three-state.

ALE [Address Latch Enable]

The ALE output latches the address signal to the output of PD_0-PD_7.

X1, X2 [Crystal Connections 1, 2]

X1 and X2 are the system clock crystal oscillator terminals. X1 is the input for an external clock.

V_{SS} [Ground]

Ground potential.

V_{DD} [Backup Power]

Backup power for on-chip RAM. The μPD78P09 will not function without power applied to V_{DD}.

V_{CC} [Power Supply]

+5 V power supply.

V_{PP}

Programming voltage input when in programming mode.

Functional Description

Input/Output

The μPD78P09 has eight comparator input lines (port T) and 40 digital I/O lines; five 8-bit ports (port A, port B, port C, port D, port F).

Comparator Input Lines. PT_0-PT_7 are configured as variable-threshold comparator input lines.

Port A, Port B, Port C, Port F. Each line of these ports can be individually programmed as an input or output. When used as I/O ports, all have latched outputs and high-impedance inputs.

Port D. Port D can be programmed as a byte input or a byte output.

Control Lines. Under software control, each line of port C can be configured individually to provide control lines for the serial interface, timer, and timer/counter.

Memory Expansion. In addition to the single-chip operation mode, the μPD78P09 has four memory expansion modes. Under software control, port D can provide a multiplexed low-order address and data bus; port F can provide a high-order address bus. Table 2 shows the relation between memory expansion modes and the pin configurations of port D and port F.

Block Diagram

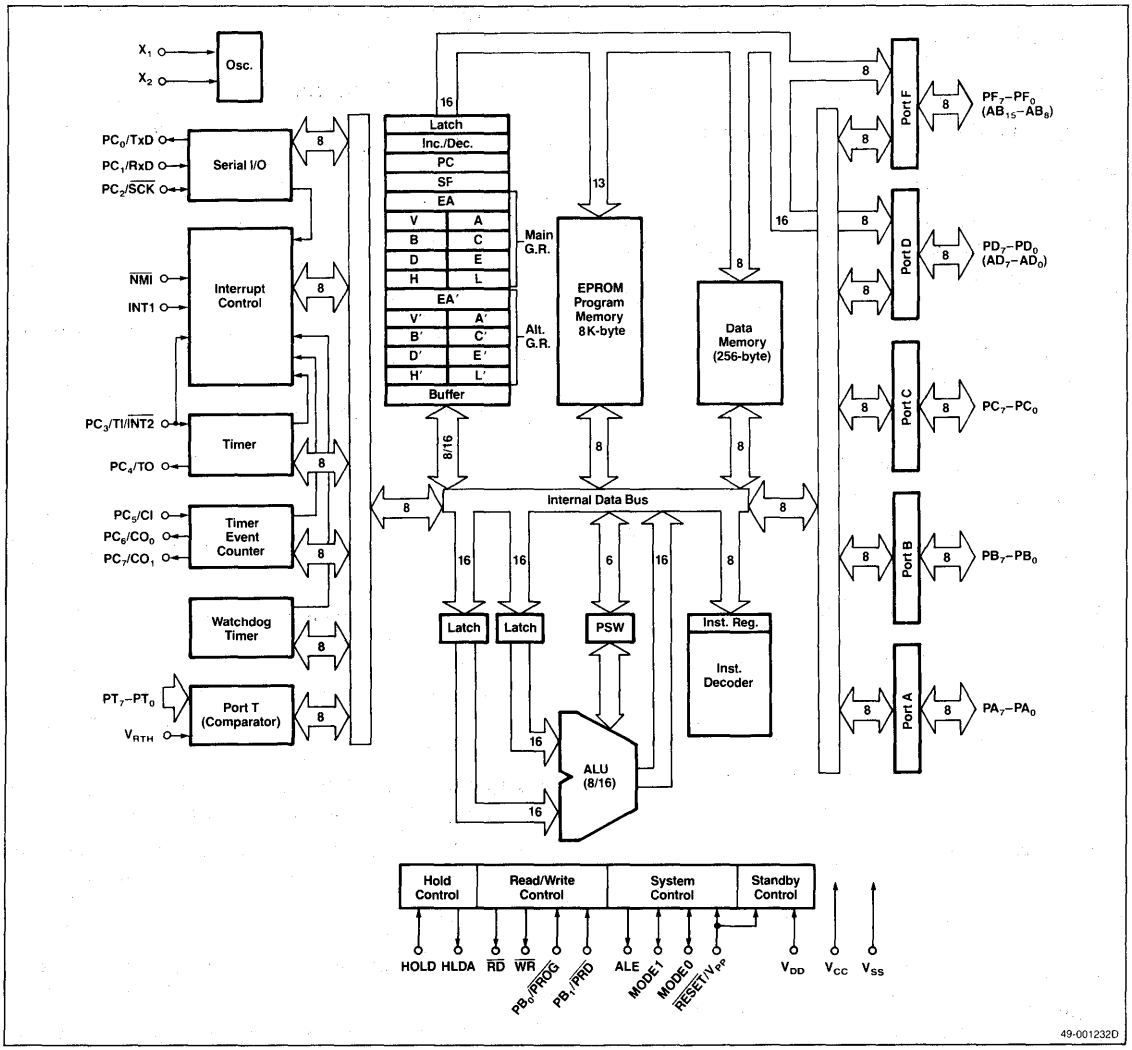


Table 2. Memory Expansion Modes and Port Configurations

Memory Expansion	Port Configuration	
None	Port D	I/O port
	Port F	I/O port
256 Bytes	Port D	Multiplexed address/data bus
	Port F	I/O port
4K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_3	Address bus
	Port F_4-F_7	I/O port
16K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_5	Address bus
	Port F_6-F_7	I/O port
56K Bytes	Port D	Multiplexed address/data bus
	Port F	Address bus

Timers

The timers consist of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be software set to increment at intervals of four machine cycles (1 μs at 12 MHz operation) or 128 machine cycles (32 μs at 12 MHz), or to increment on receipt of a pulse at TI. Figure 1 is the block diagram for the timer.

Timer/Event Counter

The 16-bit multifunctional timer/event counter (figure 2) can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output

Figure 1. Timer Block Diagram

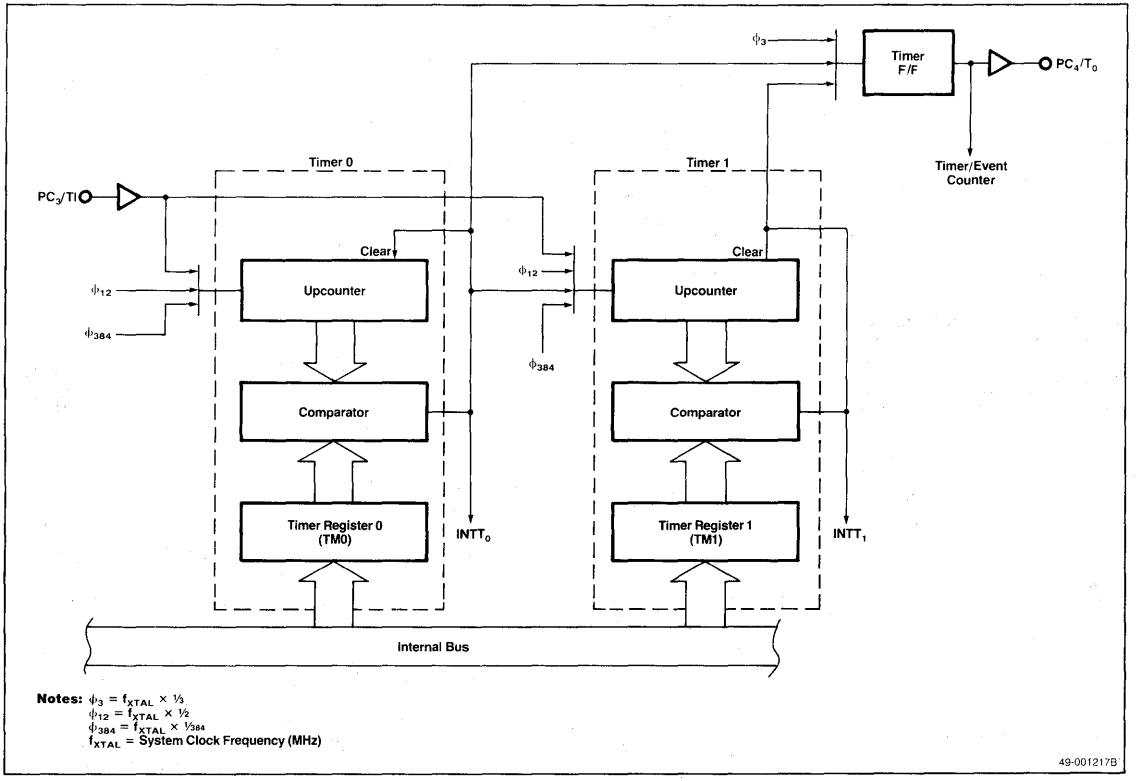


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Figure 2. Timer/Event Counter Block Diagram

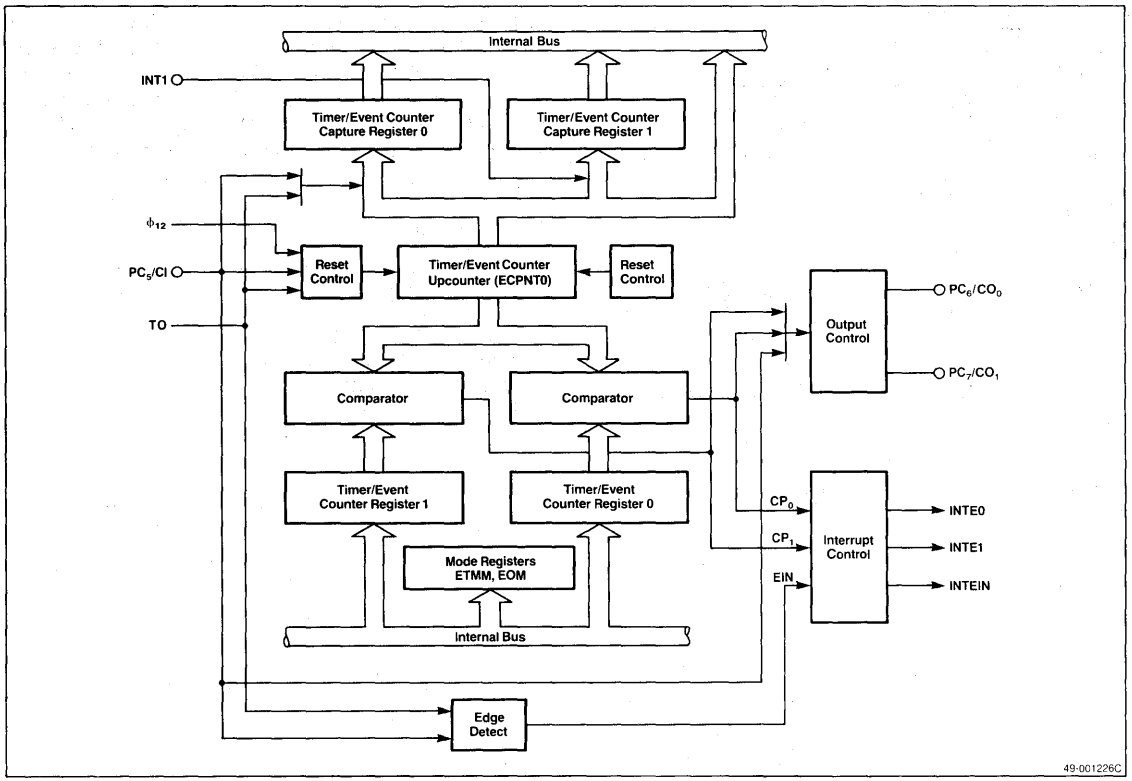


Table 3. Interrupt Sources

Interrupt Request	Interrupt Address	Type of Interrupt	Internal/ External
IRQ0	4	$\overline{NMI}$ (Nonmaskable interrupt)	Ext
		INTWD (Watchdog timer)	Int
IRQ1	8	INTT0 (Coincidence signal from timer 0)	Int
		INTT1 (Coincidence signal from timer 1)	
IRQ2	16	INT1 (Maskable interrupt)	Ext
		$\overline{INT2}$ (Maskable interrupt)	
IRQ3	24	INTE0 (Coincidence signal from timer/event counter)	Int
		INTE1 (Coincidence signal from timer/event counter)	
IRQ4	32	INTEIN (Falling signal of CI and TO counter)	Int/Ext
IRQ5	40	INTSR (Serial receive interrupt)	Int
		INST (Serial send interrupt)	

Interrupt Structure

There are 11 interrupt sources. Three are external interrupts and eight are internal. Table 3 shows 11 interrupt sources divided into six priority levels. See figure 3.

Standby Function

The standby function saves the top 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On power up, you can check the standby flag to determine whether recovery was made from standby mode or from a cold start.

Universal Serial Interface

The serial interface can operate in one of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first, for easy interfacing to certain NEC peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception: search and nonsearch. In the search mode, data is transferred one bit at a time from the

serial register to the receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from the serial register to the transmit buffer occurs eight bits at a time. In asynchronous mode, the serial interface can act as a full-duplex USART with data transfer rates up to 125 kb/s. Figure 4 shows the universal serial interface block diagram.

Zero-Crossing Detector

The INT1 and $\overline{INT2}$ terminals (used common to TI and PC_3) can detect the zero-crossing point of low-frequency AC signals. When driven directly, these pins respond as a normal digital input. Figure 5 shows the zero-crossing detection circuitry.

The zero-crossing detection capability allows you to make the 50-60 Hz power signal the basis for system timing and to control voltage phase sensitive devices.

To use the zero-cross detection mode, an AC signal of approximately 1-3 V AC (peak-to-peak) and a maximum frequency of 1 kHz is coupled through an external capacitor to the INT1 and $\overline{INT2}$ pins.

For the INT1 pin, the internal digital state is sensed as a 0 until the rising edge crosses the average DC level, when it becomes a 1 and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a 1 until the falling edge crosses the average DC level, when it becomes a 0 and $\overline{INT2}$ interrupt is generated.

Variable Threshold Input Port [Port T]

Port T has the following features:

- 8 input lines
- 16 threshold levels from 1/16 to 16/16 of reference voltage (V_{RTH})
- Level selected by writing to mode T register (figure 7)
- Output of comparator port bit reads 0 until voltage at pin exceeds selected level
- Comparison execution time: 12 μs

Figure 6 shows the block diagram for the threshold variable input port. Figure 7 shows the mode T register format.

Watchdog Timer

Use the watchdog timer for software or overall performance safety checks. If the watchdog is enabled, it must be cleared at regular intervals in program execution to avoid watchdog interrupts. Intervals are software selectable via the WDM register. Figure 8 shows the block diagram for the watchdog timer.

Figure 3. Interrupt

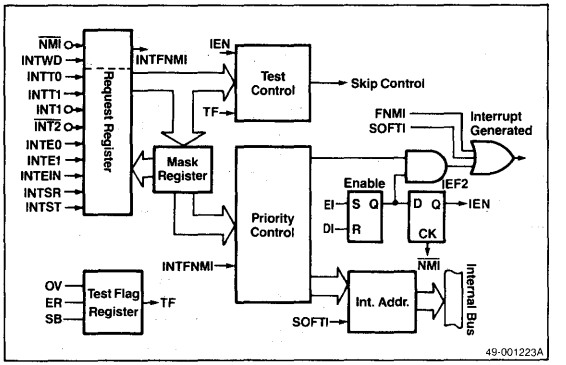


Figure 4. Universal Serial Interface Block Diagram

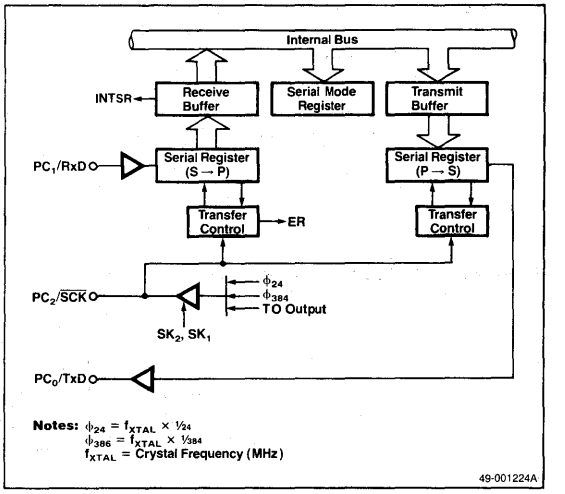


Figure 5. Zero-Crossing Detection Circuitry

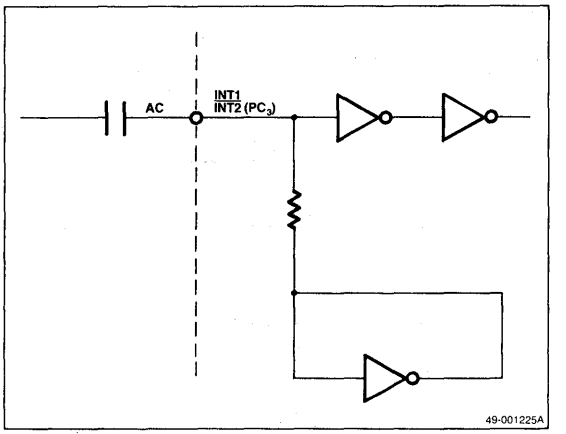


Figure 6. Threshold Variable Input Port

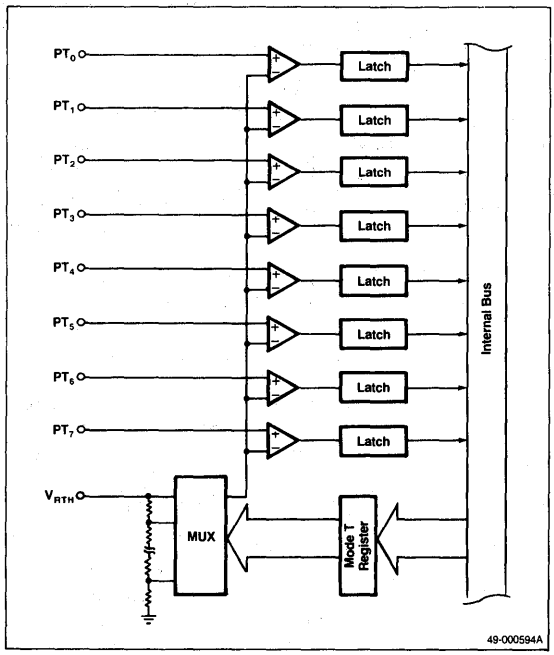


Figure 7. Mode T Register Format

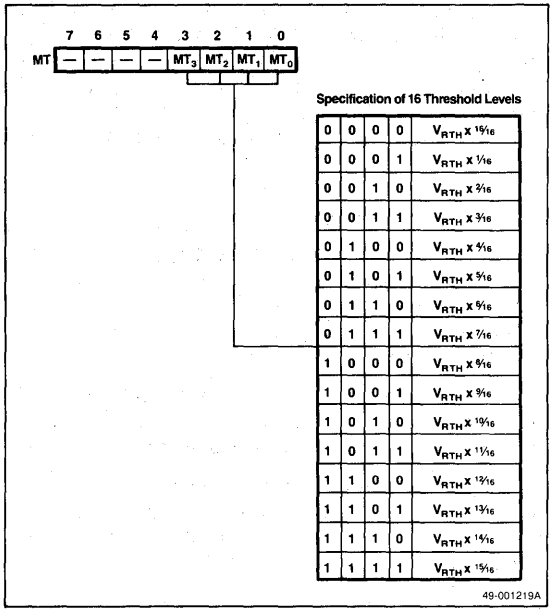
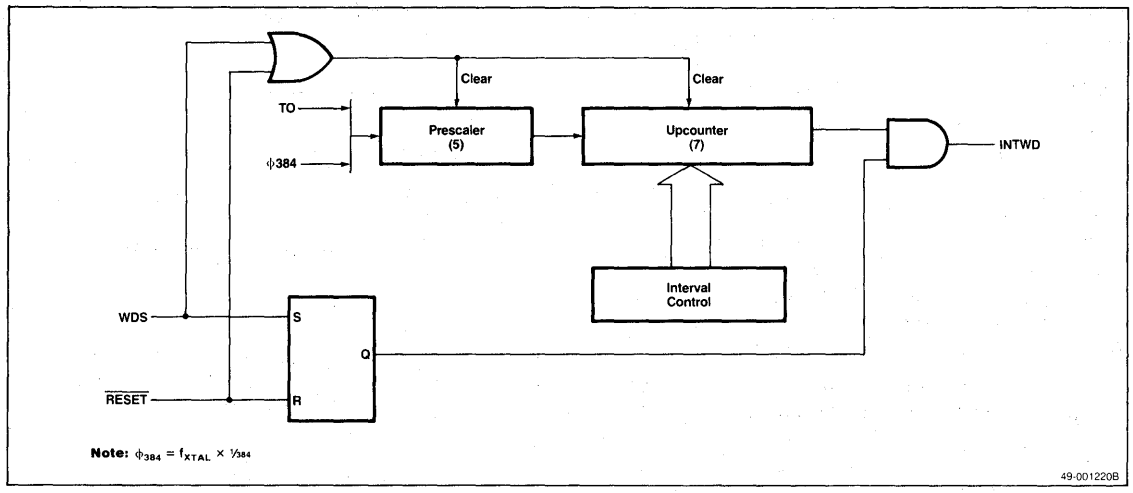


Figure 8. Watchdog Timer Block Diagram



Bit Address Instructions

The following bits may be addressed directly with certain instructions:

- Any bit in the first 16 bytes of memory addressed by the V register
- Any bit in the five 8-bit I/O ports (A, B, C, D, F)
- Any bit in the comparator port
- Any bit in the following special registers: interrupt mask, serial mode high, timer mode, timer/event counter output control.

An addressed bit may be tested, set, cleared, or complemented. It also may be moved to or from the carry flag. An addressed bit may be ANDed, ORed, and XORed with the carry flag.

Absolute Maximum Ratings

Power supply voltages, V_{CC}	−0.5 to +7.0 V
V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to +7.0 V
Output voltage, V_O	−0.5 to +7.0 V
Output current low, I_{OL}	
Each output pin	4.0 mA
Total, all output pins	100 mA
Output current high, I_{OH}	
Each output pin	−0.5 mA
Total, all output pins	−20 mA
Operating temperature, T_{OPR}	−10 to +50 °C
Storage temperature, T_{STG} (μPD7807/09)	−65 to +150 °C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			10	pF	f_c = 1 MHz. Unmeasured pins returned to 0 V.
Output capacitance	C_O			20	pF	
I/O capacitance	C_{IO}			20	pF	

DC Characteristics

T_A = −10 to +50 °C; V_{CC} = +5.0 V ±5%; V_{SS} = 0 V; V_{CC} − 0.8 V ≤ V_{DD} ≤ V_{CC}

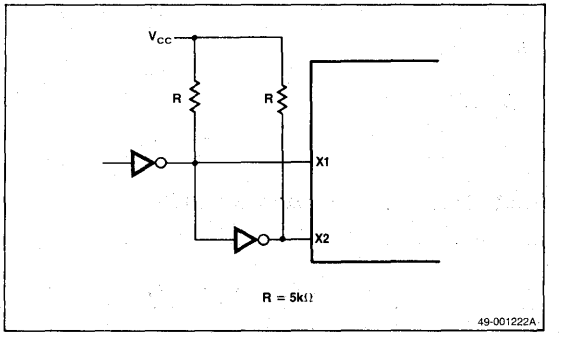
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	0		0.8	V	
Input high voltage	V_{IH1}	2.0		V_{CC}	V	All except $\overline{SCK}$, $\overline{RESET}$, X1, X2 (Note 2)
	V_{IH2}	0.8 V_{CC}		V_{CC}	V	$\overline{SCK}$, X1, X2
	V_{IH3}	0.8 V_{DD}		V_{CC}	V	$\overline{RESET}$
Output low voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output high voltage	V_{OH}	2.4			V	I_{OH} = −200 μA
Input current	I_I			±200	μA	INT1, TI(PC_3); + 0.45 V ≤ V_I ≤ V_{CC}
Input leakage current	I_{LI}			±10	μA	All except INT1, TI(PC_3) 0 V ≤ V_I ≤ V_{CC}
Output leakage current	I_{LO}			±10	μA	+0.45 V ≤ V_O ≤ V_{CC}
V_{RTH} input current	I_{RTH}		0.2(1)	0.5	mA	V_{RTH} = V_{CC}
V_{DD} supply current	I_{DD}		1.5(1)	3.2	mA	
V_{CC} supply current	I_{CC}		240(1)	320	mA	

Note:

(1) T_A = 25 °C: V_{CC} = V_{DD} = +5.0 V

(2) External clock drive circuit, see figure 9.

Figure 9. External Clock Input



Hold Operation

$T_A = -10$ to $+50°C$; $V_{CC} = +5.0\ V \pm 5\%$; $V_{SS} = 0\ V$; $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
HOLD ↑ setup time to ALE ↑	t_{SHDL}	2T + 150			ns	
ALE ↑ to HLDA ↑ delay	t_{DLHA}			T + 150	ns	
HLDA ↑ to bus floating	t_{FBHA}	0			ns	
HOLD ↓ to HLDA ↓ delay	t_{HDDA}	T − 50		4T + 150	ns	
HLDA ↓ to bus enable time	t_{EHAB}	0			ns	
Bus setup time to ALE	t_{BL}	2T − 100			ns	

Comparator Characteristics

$T_A = +10$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$; $V_{SS} = 0\ V$; $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Comparison accuracy	V_{ACOMP}			±100	mV	
Threshold voltage	V_{TH}	0		V_{CC} + 0.1	V	
Comparison time	t_{COMP}	144		145	t_{CYC}	
PT input voltage	V_{IPT}	0		V_{CC}	V	

External Clock

$T_A = -10$ to $+50°C$; $V_{CC} = +5.0\ V \pm 5\%$; $V_{SS} = 0\ V$; $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
High level width	$t_{\Phi H}$	30	250	ns	
Low level width	$t_{\Phi L}$	30	250	ns	
Rising time	t_r	0	30	ns	
Falling time	t_f	0	30	ns	

Data Retention Characteristics

$T_A = -10$ to $+50°C$; $V_{CC} = 0\ V$, $V_{DD} = V_{DDDR}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Data retention voltage	V_{DDDR}	3.2		5.5	V	$\overline{RESET} = V_{IL}$
Data retention supply current	I_{DDDR}		1.3	3.0	mA	$\overline{RESET} = V_{IL}$, $V_{DDDR} = 3.2\ V$

AC Characteristics

Read/Write Operation

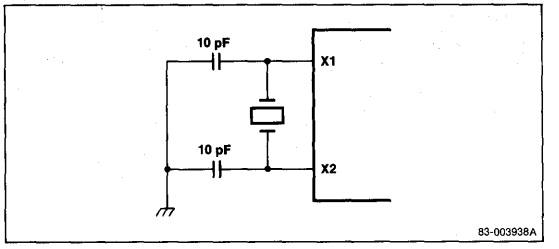
$T_A = -10$ to $+50°C$, $V_{CC} = +5.0\ V \pm 5\%$, $V_{SS} = 0\ V$, $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions (1)
X1 Input cycle time	t_{CYC}	83	250	ns	
Address set-up to ALE ↓	t_{AL}	65		ns	
Address hold after ALE ↓	t_{LA}	50		ns	
Address to $\overline{RD}$ ↓ delay time	t_{AR}	150		ns	
$\overline{RD}$ ↓ to address floating	t_{AFR}		20	ns	
Address to data input	t_{AD}		360	ns	
ALE ↓ to data input	t_{LDR}		215	ns	
$\overline{RD}$ ↓ to data input	t_{RD}		180	ns	
ALE ↓ to $\overline{RD}$ ↓ delay time	t_{LR}	35		ns	
Data hold time to $\overline{RD}$ ↑	t_{RDH}	0		ns	
$\overline{RD}$ ↑ to ALE ↑ delay time	t_{RL}	115		ns	
$\overline{RD}$ width low	t_{RR}	280		ns	Data read
		530		ns	Opcode fetch
ALE width high	t_{LL}	125		ns	
M1 setup time to ALE ↓	t_{ML}	65		ns	
M1 hold time from ALE ↓	t_{LM}	50		ns	
IO/M setup time to ALE ↓	t_{IL}	65		ns	
IO/M hold time from ALE ↓	t_{LI}	50		ns	
Address to $\overline{WR}$ ↓ delay	t_{AW}	150		ns	
ALE ↓ to data output	t_{LDW}		195	ns	
$\overline{WR}$ ↓ to data output	t_{WD}		100	ns	
ALE ↓ to $\overline{WR}$ ↓ delay	t_{LW}	35		ns	
Data set-up time to $\overline{WR}$ ↑	t_{DW}	230		ns	
Data hold time to $\overline{WR}$ ↑	t_{WDH}	95		ns	
$\overline{WR}$ ↑ to ALE ↑ delay time	t_{WL}	115		ns	
$\overline{WR}$ width low	t_{WW}	280		ns	

Note:

(1) Load capacitance: $C_L = 150$ pF; $f_{XTAL} = 12$ MHz (figure 10).

Figure 10. External Crystal Connections



DC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 5\ V \pm 10\%$, $V_{PP} = 21\ V \pm 0.5\ V$, $V_{SS} = 0\ V$, $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	0		0.8	V	
Input voltage high	V_{IH1}	2.0		V_{CC}	V	All except $\overline{SCK}$, $\overline{RESET}$ and X1
	V_{IH2}	0.8 V_{CC}		V_{CC}	V	$\overline{SCK}$, X1
Input leakage current all except INT1, TI (PC3)	I_{LI}			±10	μA	$0\ V \leqq V_I < V_{CC}$
Output voltage low	V_{OL}			0.45	V	$I_{OL} = 2.0\ mA$
Output voltage high	V_{OH}	2.4			V	$I_{OH} = -200\ \mu A$
V_{CC} supply current	I_{CC}		200	300	mA	
V_{PP} supply current	I_{PP}			30	mA	PGM = V_{IL}

AC Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 5\ V \pm 10\%$, $V_{PP} = 21\ V \pm 0.5\ V$, $V_{SS} = 0\ V$, $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address set-up time to $\overline{PROG}\downarrow$	t_{AP}	2			μs	
Address hold time from $\overline{PROG}\uparrow$	t_{PA}	2			μs	
Address set-up time to PREAD↓	t_{APR}	2			μs	
Address hold time from PREAD↑	t_{PRA}	0			μs	
Data set-up time to $\overline{PROG}\downarrow$	t_{DP}	2			μs	
Data hold time from $\overline{PROG}\uparrow$	t_{PD}	2			μs	
$\overline{PROG}$ pulse width low	t_{PP}	45	50	55	ms	
V_{PP} rise time	t_{RVP}	50			ns	
V_{PP} set-up time to $\overline{PROG}\downarrow$	t_{VPP}	2			μs	
V_{PP} hold time from $\overline{PROG}\uparrow$	t_{PVP}	2			μs	
$V_{PP}\downarrow$ to PREAD↓	t_{VPPR}	2			μs	
Data delay from PREAD↓	t_{PRD}			1	μs	
Data float delay from PREAD↑	t_{PRDF}	0		130	ns	
Input rise, fall time	t_{IR}, t_{IF}			20	μs	

Serial Operation

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{CYK}	1.66		μs	$\overline{SCK}$ input (1)
		500		ns	$\overline{SCK}$ input (2)
		2		μs	$\overline{SCK}$ output
$\overline{SCK}$ width low	t_{KKL}	750		ns	$\overline{SCK}$ input (1)
		200		ns	$\overline{SCK}$ input (2)
		900		ns	$\overline{SCK}$ output
$\overline{SCK}$ width high	t_{KKH}	750		ns	$\overline{SCK}$ input (1)
		200		ns	$\overline{SCK}$ input (2)
		900		ns	$\overline{SCK}$ output
RxD set-up time to $\overline{SCK}\uparrow$	t_{RXK}	80		ns	(1)
RxD hold time after $\overline{SCK}\uparrow$	t_{KRX}	80		ns	(1)
$\overline{SCK}\downarrow$ TxD delay time	t_{KTX}		210	ns	(1)

Note:

(1) 1x baud rate in asynchronous, synchronous, or I/O interface mode.

(2) 16x baud rate or 64x baud rate in asynchronous mode.

Zero-Cross Characteristics

$T_A = -10$ to $+50°C$, $V_{CC} = +5.0\ V + 5\%$, $V_{SS} = 0\ V$, $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Zero-cross detection input	V_{ZX}	1	1.8	V ac, p-p	Ac coupled
Zero-cross accuracy	A_{ZX}		±135	mV	60-Hz sine wave
Zero-cross detection input frequency	f_{ZX}	0.05	1	kHz	

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Bus Timing Depending on t_{CYC}

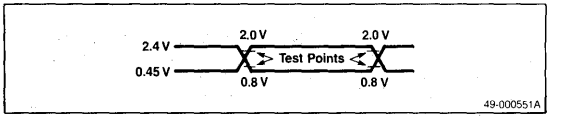
Symbol	Calculating Expression	Min/Max
t_{RP}	60T	Min
t_{TI}	6T	Min
t_{CI} (2)	6T	Min
t_{CI} (3)	48T	Min
t_{IP}	36T	Min
t_{AL}	2T − 100	Min
t_{LA}	T − 30	Min
t_{AR}	3T − 100	Min
t_{AD}	7T − 220 (4)	Max
t_{LDR}	5T − 200 (4)	Max
t_{RD}	4T − 150 (4)	Max
t_{LR}	T − 50	Min
t_{RL}	2T − 50	Min
t_{RR}	4T − 50 (Data Read) (4)	Min
	7T − 50 (Opcode Fetch) (4)	
t_{LL}	2T − 40	Min
t_{ML}	2T − 100	Min
t_{LM}	T − 30	Min
t_{IL}	2T − 100	Min
t_{LI}	T − 30	Min
t_{AW}	3T −100	Min
t_{LDW}	T + 110	Max
t_{LW}	T − 50	Min
t_{DW}	4T − 100 (4)	Min
t_{WDH}	2T − 70	Min
t_{WL}	2T − 50	Min
t_{WW}	4T − 50 (4)	Min
t_{CYK}	20T ($\overline{SCK}$ input) (1)	Min
	24T ($\overline{SCK}$ output)	
t_{KKL}	10T − 80 ($\overline{SCK}$ input) (1)	Min
	12T − 100 ($\overline{SCK}$ output)	
t_{KKH}	10T − 80 ($\overline{SCK}$ input) (1)	Min
	12T − 100 ($\overline{SCK}$ output)	

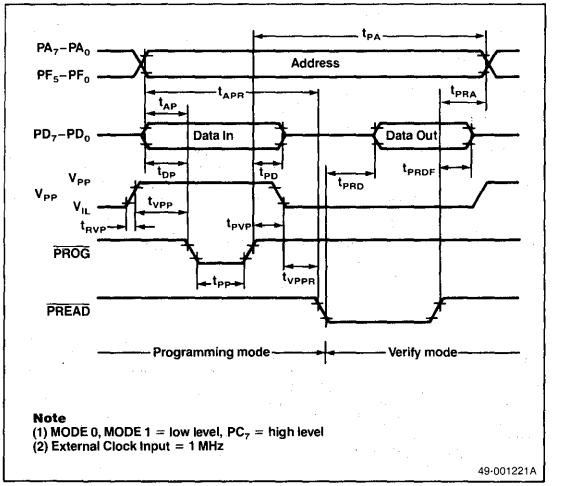
Note:

(1) 1x baud rate in asynchronous, synchronous, or I/O interface mode.
$T = t_{CYC} = 1\ f_{XTAL}$.
The items not included in this list are independent of oscillator frequency (f_{XTAL}).
(2) Event counter mode.
(3) Pulse width measurement mode.
(4) Add 3T when using external program memory with programmable WAIT function.

Timing Waveforms

AC Timing Test Points





Note
(1) MODE 0, MODE 1 = low level, PC_7 = high level
(2) External Clock Input = 1 MHz

Instruction Set

In addition to the basic 7800 family instruction set, the μPD78P09 executes the following types of instructions:

- 16-bit data transfers between memory, registers, and extended accumulator
- 16-bit addition and subtraction
- 16-bit comparison and skip
- 16-bit AND, OR, XOR operation
- 16-bit data shift and rotation
- Multiply; 8-bit by 8-bit, 16-bit product (less than 8 μs execution)
- Divide; 16-bit by 8-bit, 16-bit quotient, 8-bit remainder (less than 15 μs execution)
- Working register instruction for efficient RAM addressing, testing, and manipulating
- Direct bit addressing for code-efficient addressing, testing, and manipulating bits in RAM, port lines, and mode registers.

Operand Format/Description

Format	Description
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TxB, TM_0, TM_1, WDM, MT
sr1	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, RxB, PT, WDM
sr2	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM
sr3	ETM_0, ETM_1
sr4	ECNT, ECPT0, ECPT1
sr5	PA, PB, PC, PD, PF, MKH, MKL, SMH, EOM, TMM, PT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D−, H−, D + byte, H + A, H + B, H + EA, H + byte
rpa3	D, H, D++, H++, D + byte, H + A, H + B, H + EA, H + byte
wa	8-Bit immediate data
word	16-Bit immediate data
byte	8-Bit immediate data
bit	8-Bit address of bit location
f	CY, HC, Z
irf	NMI, FT0, FT1, F1, F2, FE0, FE1, FEIN, FSR, FST, ER, OV, IFE2, SB

Instruction Set Symbol Definitions

Symbol	Description
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
∨̄	Exclusive OR
—	Complement
•	Concatenation

Remarks

1. sr-sr5 (special register)

PA = Port A	ECNT = Timer/Event Counter Upcounter
PB = Port B	ECPT0 = Timer/Event Counter Capture 0
PC = Port C	ECPT1 = Timer/Event Counter Capture 1
PD = Port D	ETMM = Timer/Event Counter Mode
PF = Port F	EOM = Timer/Event Counter Output Mode
PT = Port T	WDM = Watchdog Timer Mode
MA = Mode A	TxB = Tx Buffer
MB = Mode B	RxB = Rx Buffer
MC = Mode C	SMH = Serial Mode High
MCC = Mode Control C	SML = Serial Mode Low
MF = Mode F	MKH = Mask High
MT = Mode T	MKL = Mask Low
MM = Memory Mapping	
TM_0 = Timer Register 0	
TM_1 = Timer Register 1	
TMM = Timer Mode	
ETM_0 = Timer/Event Counter Register 0	
ETM_1 = Timer/Event Counter Register 1	

2. rp-rp3 (register pair)

SP = Stack Pointer	H = HL
B = BC	V = VA
D = DE	EA = Extended Accumulator

3. rpa-rpa3 (rp addressing)

B = (BC)	D++ = (DE) + 2
D = (DE)	H++ = (HL) + 2
H = (HL)	D + byte = (DE) + byte
D+ = (DE) + 1	H + A = (HL) + (A)
H+ = (HL) + 1	H + B = (HL) + (B)
D− = (DE) − 1	H + EA = (HL) + (EA)
H− = (HL) − 1	H + byte = (HL) + byte

4. f (flag)

CY = Carry HC = Half Carry Z = Zero

5. irf (interrupt flag)

NMI = NMI input	FEIN = INTFEIN
FT0 = INTFT0	FSR = INTFSR
FT1 = INTFT1	FST = INTFST
F1 = INTF1	ER = Error
F2 = INTF2	OV = Overflow
FE0 = INTFE0	IE2 = Interrupt Enable F/F2
FE1 = INTFE1	SB = Standby

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Instruction Set

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	Operation Code B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Data Transfer																					
MOV	r1,A	(r1) ← (A)	0	0	0	1	1	T_2	T_1	T_0									4	1	
	A, r1	(A) ← (r1)	0	0	0	0	1	T_2	T_1	T_0									4	1	
	*sr,A	(sr) ← (A)	0	1	0	0	1	1	0	1	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	*A,sr1	(A) ← (sr1)	0	1	0	0	1	1	0	0	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	r,word	(r) ← (word)	0	1	1	1	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
	word,r	(word) ← (r)	0	1	1	1	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
MVI	*r,byte	(r) ← byte set L1 if r = A set L0 if r = L	0	1	1	0	1	R_2	R_1	R_0	Data								7	2	L1 = 1 and r = A L0 = 1 and r = L
	sr2,byte	(sr2) ← byte	0	1	1	0	0	1	0	0	S_3	0	0	0	0	S_2	S_1	S_0	14	3	
											Data										
MVIW	*wa, byte	((V)•(wa)) ← byte	0	1	1	1	0	0	0	1	Offset								13	3	
			Data																		
MVIX	*rpa1,byte	(rpa1) ← byte	0	1	0	0	1	0	A_1	A_0	Data								10	2	
STAW	*wa	((V)•(wa)) ← A	0	1	1	0	0	0	1	1	Offset								10	2	
LDAW	*wa	(A) ← ((V)•(wa))	0	0	0	0	0	0	0	1	Offset								10	2	
STAX	*rpa2	(rpa2) ← (A)	A_3	0	1	1	1	A_2	A_1	A_0	Data (2)								7/13(3)	2	
LDAX	rpa2	(A) ← ((rpa2))	A_3	0	1	0	1	A_2	A_1	A_0	Data (2)								7/13(3)	2	
EXX		(B) ↔ (B'),(C) ↔ (C'),(D) ↔ (D') (E) ↔ (E'),(H) ↔ (H'),(L) ↔ (L')	0	1	0	0	1	0	0	0	1	0	1	0	1	1	1	1	8	2	
EXA		(V) ↔ (V'),(A) ↔ (A'),(EA) ↔ (EA')	0	1	0	0	1	0	0	0	1	0	1	0	1	1	0	0	8	2	
EXH		(H) ↔ (H'),(L) ↔ (L')	0	1	0	0	1	0	0	0	1	0	1	0	1	1	1	0	8	2	
EXR		(V) ↔ (V'),(A) ↔ (A'),(B) ↔ (B'); (C) ↔ (C') (D) ↔ (D') (E) ↔ (E'),(H) ↔ (H'),(L) ↔ (L'),(EA) ↔ (EA')	0	1	0	0	1	0	0	0	1	0	1	0	1	1	0	1	8	2	
16-Bit Data Transfer																					
BLOCK	D+	((DE)) ← ((HL)),(DE) ← (DE) + 1, (HL) ← (HL) + 1, (C) ← (C) − 1 End if borrow	0	0	0	1	0	0	0	0									13 x (C + 1)	1	
	D−	((DE)) ← ((HL)),(DE) ← (DE) + 1, (HL) ← (HL) − 1, (C) ← (C) − 1 End if borrow	0	0	0	1	0	0	0	1									13 x (C + 1)	1	
DMOV	rp3, EA	($rp3_L$) ← (EAL),($rp3_H$) ← (EAH)	1	0	1	1	0	1	P_1	P_0									4	1	
	EA,rp3	(EAL) ← ($rp3_L$),(EAH) ← ($rp3_H$)	1	0	1	0	0	1	P_1	P_0									4	1	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
16-Bit Data Transfer (cont)																					
DMOV	sr3, EA	(sr3) ← (EA)	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1	U_0	14	2	
	EA,sr4	(EA) ← (sr4)	0	1	0	0	1	0	0	0	1	1	0	0	0	0	V_1	V_0	14	2	
SBCD	word	(word) ← (C), (word + 1) ← (B)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	20	4	
			Low addr								High addr										
SDED	word	(word) ← (E), (word + 1) ← (D)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	0	20	4	
			Low addr								High addr										
SHLD	word	(word) ← (L), (word + 1) ← (H)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	20	4	
			Low addr								High addr										
SSPD	word	(word) ← (SP_L),(word + 1) ← (SP_H)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	20	4	
			Low addr								High addr										
STEAX	rpa3	((rpa3)) ← (EAL),((rpa3)) + 1 ← (EAH)	0	1	0	0	1	0	0	0	1	0	0	1	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
LBCD	word	(C) ← (word),(B) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	20	4	
			Low addr								High addr										
LDED	word	(E) ← (word),(D) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	20	4	
			Low addr								High addr										
LHLD	word	(L) ← (word),(H) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	20	4	
			Low addr								High addr										
LSPD	word	(SP_L) ← (word),(SP_H) ← ((word) + 1)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	20	4	
			Low addr								High addr										
LDEAX	rpa3	(EAL) ← ((rpa3)),(EAH) ← ((rpa3) + 1)	0	1	0	0	1	0	0	0	1	0	0	0	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
PUSH	rp1	((SP) − 1) ← ($rp1_H$) ((SP) − 2) ← ($rp1_L$) (SP) ← (SP) − 2	1	0	1	1	0	Q_2	Q_1	Q_0									13	1	
POP	rp1	($rp1_L$) ← ((SP)),($rp1_H$) ← ((SP) + 1) (SP) ← (SP) + 2	1	0	1	0	0	Q_2	Q_1	Q_0									10	1	
LXI	*rp2,word	(rp2) ← (word) set L0 if rp2 = H	0	P_2	P_1	P_0	0	1	0	0	Low byte								10	3	L0 = 1 and rp2 = H
			High byte																		
TABLE		(C) ← ((PC)+3+(A)),B ← ((PC)+3+(A)+ 1)	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	0	17	2	
8-Bit Arithmetic [Register]																					
ADD	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	1	0	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	1	0	0	0	R_2	R_1	R_0	8	2	
ADC	A,r	(A) ← (A) + (r) + (CY)	0	1	1	0	0	0	0	0	1	1	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A) + (CY)	0	1	1	0	0	0	0	0	0	1	0	1	0	R_2	R_1	R_0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code																State(1)	Bytes	Skip Condition
			7	6	5	4 (B1)	3 (B3)	2	1	0	7	6	5	4 (B2)	3 (B4)	2	1	0			
8-Bit Arithmetic [Register] (cont)																					
ADDNC	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	0	1	0	0	R_2	R_1	R_0	8	2	No carry
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	0	1	0	0	R_2	R_1	R_0	8	2	No carry
SUB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	0	R_2	R_1	R_0	8	2	
SBB	A,r	(A) ← (A) − (r) − (CY)	0	1	1	0	0	0	0	0	1	1	1	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A) − (CY)	0	1	1	0	0	0	0	0	0	1	1	1	0	R_2	R_1	R_0	8	2	
SUBNB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
ANA	A,r	(A) ← (A) ∧ (r)	0	1	1	0	0	0	0	0	1	0	0	0	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∧ (A)	0	1	1	0	0	0	0	0	0	0	0	0	1	R_2	R_1	R_0	8	2	
ORA	A,r	(A) ← (A) ∨ (r)	0	1	1	0	0	0	0	0	1	0	0	1	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∨ (A)	0	1	1	0	0	0	0	0	0	0	0	1	1	R_2	R_1	R_0	8	2	
XRA	A,r	(A) ← (A) ∨̄ (r)	0	1	1	0	0	0	0	0	1	0	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∨̄ (A)	0	1	1	0	0	0	0	0	0	0	0	1	0	R_2	R_1	R_0	8	2	
GTA	A,r	(A) − (r) − 1	0	1	1	0	0	0	0	0	1	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) − (A) − 1	0	1	1	0	0	0	0	0	0	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
LTA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
NEA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	1	R_2	R_1	R_0	8	2	No zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	8	2	No zero
EQA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	1	1	R_2	R_1	R_0	8	2	Zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	8	2	Zero
ONA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	0	1	R_2	R_1	R_0	8	2	No zero
OFFA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	1	1	R_2	R_1	R_0	8	2	Zero
8-Bit Arithmetic (Memory)																					
ADDX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	0	A_2	A_1	A_0	11	2	
ADCX	rpa	(A) ← (A) + ((rpa)) + (CY)	0	1	1	1	0	0	0	0	1	1	0	1	0	A_2	A_1	A_0	11	2	
ADDNCX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	0	1	0	0	A_2	A_1	A_0	11	2	No carry
SUBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	0	A_2	A_1	A_0	11	2	
SBBX	rpa	(A) ← (A) − ((rpa)) − (CY)	0	1	1	1	0	0	0	0	1	1	1	1	0	A_2	A_1	A_0	11	2	
SUBNBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	0	A_2	A_1	A_0	11	2	No borrow
ANAX	rpa	(A) ← (A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	0	1	A_2	A_1	A_0	11	2	
ORAX	rpa	(A) ← (A) ∨ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	1	A_2	A_1	A_0	11	2	

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Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 B3 7	6	5	4	3	2	1	0	B2 B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Arithmetic (Memory) (cont)																					
XRAX	rpa	(A) ← (A) ∀ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	0	A_2	A_1	A_0	11	2	
GTAX	rpa	(A) – ((rpa)) – 1	0	1	1	1	0	0	0	0	1	0	1	0	1	A_2	A_1	A_0	11	2	No borrow
LTAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	1	A_2	A_1	A_0	11	2	Borrow
NEAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	1	A_2	A_1	A_0	11	2	No zero
EQAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	1	1	A_2	A_1	A_0	11	2	Zero
ONAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	1	A_2	A_1	A_0	11	2	No zero
OFFAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	1	1	A_2	A_1	A_0	11	2	Zero
Immediate Data																					
ADI	*A,byte	(A) ← (A) + byte	0	1	0	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	1	0	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2, byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	1	0	0	0	S_2	S_1	S_0	20	3	
			Data																		
ACI	*A,byte	(A) ← (A) + byte + (CY)	0	1	0	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte + (CY)	0	1	1	1	0	1	0	0	0	1	0	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte + (CY)	0	1	1	0	0	1	0	0	S_3	1	0	1	0	S_2	S_1	S_0	20	3	
			Data																		
ADINC	*A,byte	(A) ← (A) + byte	0	0	1	0	0	1	1	0	Data								7	2	No carry
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	0	1	0	0	R_2	R_1	R_0	11	3	No carry
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	0	1	0	0	S_2	S_1	S_0	20	3	No carry
			Data																		
SUI	*A,byte	(A) ← (A) – byte	0	1	1	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte	0	1	1	1	0	1	0	0	0	1	1	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte	0	1	1	0	0	1	0	0	S_3	1	1	0	0	S_2	S_1	S_0	20	3	
			Data																		
SBI	*A,byte	(A) ← (A) – byte – (CY)	0	1	1	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte – (CY)	0	1	1	1	0	1	0	0	0	1	1	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte – (CY)	0	1	1	0	0	1	0	0	S_3	1	1	1	0	S_2	S_1	S_0	20	3	
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7 6 5 4 3 2 1 0	Operation Code B2/B4 7 6 5 4 3 2 1 0	State(1)	Bytes	Skip Condition
Immediate Data (cont)							
SUINB	*A,byte	(A) ← (A) – byte	0 0 1 1 0 1 1 0	Data	7	2	No borrow
	r,byte	(r) ← (r) – byte	0 1 1 1 0 1 0 0	0 0 1 1 0 R_2 R_1 R_0	11	3	No borrow
			Data				
	sr2,byte	(sr2) ← (sr2) – byte	0 1 1 0 0 1 0 0	S_3 0 1 1 0 S_2 S_1 S_0	20	3	No borrow
			Data				
ANI	*A,byte	(A) ← (A) ∧ byte	0 0 0 0 0 1 1 1	Data	7	2	
	r,byte	(r) ← (r) ∧ byte	0 1 1 1 0 1 0 0	0 0 0 0 1 R_2 R_1 R_0	11	3	
			Data				
	sr2,byte	(sr2) ← (sr2) ∧ byte	0 1 1 0 0 1 0 0	S_3 0 0 0 1 S_2 S_1 S_0	20	3	
			Data				
ORI	*A,byte	(A) ← (A) V byte	0 0 0 1 0 1 1 1	Data	7	2	
	r,byte	(r) ← (r) V byte	0 1 1 1 0 1 0 0	0 0 0 1 1 R_2 R_1 R_0	11	3	
			Data				
	sr2,byte	(sr2) ← (sr2) V byte	0 1 1 0 0 1 0 0	S_3 0 0 1 1 S_2 S_1 S_0	20	3	
			Data				
XRI	*A,byte	(A) ← (A) ∀ byte	0 0 0 1 0 1 1 0	Data	7	2	
	r,byte	(r) ← (r) ∀ byte	0 1 1 1 0 1 0 0	0 0 0 1 0 R_2 R_1 R_0	11	3	
			Data				
	sr2,byte	(sr2) ← (sr2) ∀ byte	0 1 1 0 0 1 0 0	S_3 0 0 1 0 S_2 S_1 S_0	20	3	
			Data				
GTI	*A,byte	(A) – byte – 1	0 0 1 0 0 1 1 1	Data	7	2	No borrow
	r,byte	(r) – byte – 1	0 1 1 1 0 1 0 0	0 0 1 0 1 R_2 R_1 R_0	11	3	No borrow
			Data				
	sr5,byte	(sr5) – byte – 1	0 1 1 0 0 1 0 0	S_3 0 1 0 1 S_2 S_1 S_0	14	3	No borrow
			Data				
LTI	*A,byte	(A) – byte	0 0 1 1 0 1 1 1	Data	7	2	Borrow
	r,byte	(r) – byte	0 1 1 1 0 1 0 0	0 0 1 1 1 R_2 R_1 R_0	11	3	Borrow
			Data				
	sr5,byte	(sr5) – byte	0 1 1 0 0 1 0 0	S_3 0 1 1 1 S_2 S_1 S_0	14	3	Borrow
			Data				
NEI	*A,byte	(A) – byte	0 1 1 0 0 1 1 1	Data	7	2	No zero
	r,byte	(r) – byte	0 1 1 1 0 1 0 0	0 1 1 0 1 R_2 R_1 R_0	11	3	No zero
			Data				

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Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3 7	6	5	4	3	2	1	0	B2 / B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Immediate Data (cont)																					
NEI	sr5,byte	(sr5) – byte	0	1	1	0	0	1	0	0	S_3	1	1	0	1	S_2	S_1	S_0	14	3	No zero
			Data																		
EQI	*A,byte	(A) – byte	0	1	1	1	0	1	1	1	Data								7	2	Zero
	r,byte	(r) – byte	0	1	1	1	0	1	0	0	0	1	1	1	1	R_2	R_1	R_0	11	3	Zero
			Data																		
	sr5,byte	(sr5) – byte	0	1	1	0	0	1	0	0	S_3	1	1	1	1	S_2	S_1	S_0	14	3	Zero
			Data																		
ONI	*A,byte	(A) ∧ byte	0	1	0	0	0	1	1	1	Data								7	2	No zero
	r,byte	(r) ∧ byte	0	1	1	1	0	1	0	0	0	1	0	0	1	R_2	R_1	R_0	11	3	No zero
			Data																		
	sr5,byte	(sr5) ∧ byte	0	1	1	0	0	1	0	0	S_3	1	0	0	1	S_2	S_1	S_0	14	3	No zero
			Data																		
OFFI	*A,byte	(A) ∧ byte	0	1	0	1	0	1	1	1	Data								7	2	Zero
	r,byte	(r) ∧ byte	0	1	1	1	0	1	0	0	0	1	0	1	1	R_2	R_1	R_0	11	3	Zero
			Data																		
	sr5,byte	(sr5) ∧ byte	0	1	1	0	0	1	0	0	S_3	1	0	1	1	S_2	S_1	S_0	14	3	Zero
			Data																		
Working Register																					
ADDW	wa	(A) ← (A) + ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	0	0	0	0	0	14	3	
			Offset																		
ADCW	wa	(A) ← (A) + ((V)•(wa)) + (CY)	0	1	1	1	0	1	0	0	1	1	0	1	0	0	0	0	14	3	
			Offset																		
ADDNCW	wa	(A) ← (A) + ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	0	0	0	0	0	14	3	No carry
			Offset																		
SUBW	wa	(A) ← (A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	0	0	0	0	0	14	3	
			Offset																		
SBBW	wa	(A) ← (A) – ((V)•(wa)) – (CY)	0	1	1	1	0	1	0	0	1	1	1	1	0	0	0	0	14	3	
			Offset																		
SUBNBW	wa	(A) ← (A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	1	0	0	0	0	14	3	No borrow
			Offset																		
ANAW	wa	(A) ← (A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	0	1	0	0	0	14	3	
			Offset																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Working Register (cont)																					
ORAW	wa	(A) ← (A) V ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0	14	3	
			Offset																		
XRAW	wa	(A) ← (A)⊻((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0	14	3	
			Offset																		
GTAW	wa	(A) – ((V)•(wa)) – 1	0	1	1	1	0	1	0	0	1	0	1	0	1	0	0	0	14	3	No borrow
			Offset																		
LTAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	1	0	0	0	0	14	3	Borrow
			Offset																		
NEAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	0	0	0	0	0	14	3	No zero
			Offset																		
EQAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	1	0	0	0	0	14	3	Zero
			Offset																		
ONAW	wa	(A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	0	0	0	0	0	14	3	No zero
			Offset																		
OFFAW	wa	(A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	1	0	0	0	0	14	3	Zero
			Offset																		
ANIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) ∧ byte	0	0	0	0	0	1	0	1	Offset								19	3	
			Data																		
ORIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) V byte	0	0	0	1	0	1	0	1	Offset								19	3	
			Data																		
GTIW	*wa,byte	((V)•(wa)) – byte – 1	0	0	1	0	0	1	0	1	Offset								13	3	No borrow
			Data																		
LTIW	*wa,byte	((V)•(wa)) – byte	0	0	1	1	0	1	0	1	Offset								13	3	Borrow
			Data																		
NEIW	*wa,byte	((V)•(wa)) – byte	0	1	1	0	0	1	0	1	Offset								13	3	No zero
			Data																		
EQIW	*wa,byte	((V)•(wa)) – byte	0	1	1	1	0	1	0	1	Offset								13	3	Zero
			Data																		
ONIW	*wa,byte	((V)•(wa)) ∧ byte	0	1	0	0	0	1	0	1	Offset								13	3	No zero
			Data																		
OFFIW	*wa,byte	((V)•(wa)) ∧ byte	0	1	0	1	0	1	0	1	Offset								13	3	Zero
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 B3 7	6	5	4	3	2	1	0	B2 B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
16-Bit Arithmetic																					
EADD	EA,r2	(EA) ← (EA) + (r2)	0	1	1	1	0	0	0	0	0	1	0	0	0	0	R_1	R_0	11	2	
DADD	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	0	1	P_1	P_0	11	2	
DADC	EA,rp3	(EA) ← (EA) + (rp3) + (CY)	0	1	1	1	0	1	0	0	1	1	0	1	0	1	P_1	P_0	11	2	
DADDNC	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	0	1	0	0	1	P_1	P_0	11	2	No carry
ESUB	EA,r2	(EA) ← (EA) − (r2)	0	1	1	1	0	0	0	0	0	1	1	0	0	0	R_1	R_0	11	2	
DSUB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	0	1	P_1	P_0	11	2	
DSBB	EA,rp3	(EA) ← (EA) − (rp3) − (CY)	0	1	1	1	0	1	0	0	1	1	1	1	0	1	P_1	P_0	11	2	
DSUBNB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	0	1	P_1	P_0	11	2	No borrow
DAN	EA,rp3	(EA) ← (EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	0	0	0	1	1	P_1	P_0	11	2	
DOR	EA,rp3	(EA) ← (EA) ∨ (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	1	1	P_1	P_0	11	2	
DXR	EA,rp3	(EA) ← (EA) ∨ (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	0	1	P_1	P_0	11	2	
DGT	EA,rp3	(EA) − (rp3) − 1	0	1	1	1	0	1	0	0	1	0	1	0	1	1	P_1	P_0	11	2	No borrow
DLT	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	1	1	P_1	P_0	11	2	Borrow
DNE	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	1	1	P_1	P_0	11	2	No zero
DEQ	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	1	1	1	P_1	P_0	11	2	Zero
DON	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	1	1	P_1	P_0	11	2	No zero
DOFF	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	1	1	1	P_1	P_0	11	2	Zero
Multiply/Divide																					
MUL	r2	(EA) ← (A) x (r2)	0	1	0	0	1	0	0	0	0	0	1	0	1	1	R_1	R_0	32	2	
DIV	r2	(EA) ← (EA) ÷ (r2), (r2) ← Remainder	0	1	0	0	1	0	0	0	0	0	1	1	1	1	R_1	R_0	59	2	
Increment/Decrement																					
INR	r2	(r2) ← (r2) + 1	0	1	0	0	0	0	R_1	R_0									4	1	Carry
INRW	*wa	((V)•(wa)) ← ((V)•(wa)) + 1	0	0	1	0	0	0	0	0				Offset					16	2	Carry
INX	rp	(rp) ← (rp) + 1	0	0	P_1	P_0	0	0	1	0									7	1	
	EA	(EA) ← (EA) + 1	1	0	1	0	1	0	0	0									7	1	
DCR	r2	(r2) ← (r2) − 1	0	1	0	1	0	0	R_1	R_0									4	1	Borrow
DCRW	wa	((V)•(wa)) ← ((V)•(wa)) − 1	0	0	1	1	0	0	0	0				Offset					16	2	Borrow
DCX	rp	(rp) ← (rp) − 1	0	0	P_1	P_0	0	0	1	1									7	1	
	EA	(EA) ← (EA) − 1	1	0	1	0	1	0	0	1									7	1	
Others																					
DAA		Decimal Adjust Accumulator	0	1	1	0	0	0	0	1									4	1	
STC		(CY) ← 1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	8	2	
CLC		(CY) ← 0	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	0	8	2	
CMC		(CY) ← (CY)	0	1	0	0	1	0	0	0	1	0	1	0	1	0	1	0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code																State(1)	Bytes	Skip Condition
						B1	B3						B2	B4							
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
Others (cont)																					
NEGA		(A) ← (A) + 1	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	0	8	2	
Rotate and Shift																					
RLD		Rotate left digit	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	17	2	
RRD		Rotate right digit	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	1	17	2	
RLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow (CY)$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	1	1	0	1	R_1	R_0	8	2	
RLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$, $(r2_7) \leftarrow (CY)$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	1	1	0	0	R_1	R_0	8	2	
SLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	1	0	0	1	R_1	R_0	8	2	
SLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$, $(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	1	0	0	0	R_1	R_0	8	2	
SLLC	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	0	0	0	1	R_1	R_0	8	2	Carry
SLRC	r2	$(r2_{m-1}) \leftarrow (r2_m)$, $(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	R_1	R_0	8	2	Carry
DRLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$, $(EA_0) \leftarrow (CY)$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	1	0	1	1	0	1	0	0	8	2	
DRLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$, $(EA_{15}) \leftarrow (CY)$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	1	0	1	1	0	0	0	0	8	2	
DSLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$, $(EA_0) \leftarrow 0$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	8	2	
DSLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$, $(EA_{15}) \leftarrow 0$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	8	2	
Jump																					
JMP	*word	(PC) ← word	0	1	0	1	0	1	0	0	Low addr								10	3	
			High addr																		
JB		$(PC_H) \leftarrow (B)$, $(PC_L) \leftarrow (C)$	0	0	1	0	0	0	0	1									4	1	
JR	word	(PC) ← (PC) + 1 + jdisp 1	1	1	←		jdisp1		→										10	1	
JRE	*word	(PC) ← (PC) + 2 + jdisp	0	1	0	0	1	1	1	←	jdisp							→	10	2	
JEA		(PC) ← (EA)	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	0	8	2	
Call																					
CALL	*word	$((SP)-1) \leftarrow ((PC)+3)_H$, $((SP)-2) \leftarrow ((PC)+3)_L$, (PC) ← word, (SP) ← (SP) − 2	0	1	0	0	0	0	0	0	Low addr								16	3	
			High addr																		
CALB		$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_H) \leftarrow (B)$, $(PC_L) \leftarrow (C)$, (SP) ← (SP) − 2	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	1	17	2	
CALF	*word	$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_{15\text{-}11}) \leftarrow 00001$, $(PC_{10\text{-}0}) \leftarrow$ fa, (SP) ← (SP) − 2	0	1	1	1	1	←			fa							→	13	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
						B1	B3							B2	B4						
Call (cont)																					
CALT	word	$((SP)-1) \leftarrow ((PC)+1)_H$, $((SP)-2) \leftarrow ((PC)+1)_L$ $(PC_L) \leftarrow (128+2ta), (PC_H) \leftarrow (129+2ta), (SP) \leftarrow (SP)-2$	1	0	0	←		ta		→									16	1	
SOFTI		$((SP)-1) \leftarrow (PSW), ((SP)-2) \leftarrow ((PC)+1)_H, ((SP)-3) \leftarrow ((PC)+1)_L$, $(PC) \leftarrow 0060H, (SP) \leftarrow (SP)-3$	0	1	1	1	0	0	1	0									16	1	
Return																					
RET		$(PC_L) \leftarrow ((SP)), (PC_H) \leftarrow ((SP)+1)$ $(SP) \leftarrow (SP)+2$	1	0	1	1	1	0	0	0									10	1	
RETS		$(PC_L) \leftarrow ((SP)), (PC_H) \leftarrow ((SP)+1)$ $(SP) \leftarrow (SP)+2, (PC) \leftarrow (PC)+n$	1	0	1	1	1	0	0	1									10	1	Unconditional Skip
RETI		$(PC_L) \leftarrow ((SP)), (PC_H) \leftarrow ((SP)+1)$ $(PSW) \leftarrow ((SP)+2), (SP) \leftarrow (SP)+3$	0	1	1	0	0	0	1	0									13	1	
Bit Manipulation																					
MOV	*CY, bit	(CY) ← (bit)	0	1	0	1	1	1	1	1				Bit Addr					10	2	
	*bit CY	(bit) ← (CY)	0	1	0	1	1	0	1	0				Bit Addr					13	2	
AND	*CY,bit	(CY) ← (CY) ∧ (bit)	0	0	1	1	0	0	0	1				Bit Addr					10	2	
OR	*CY, bit	(CY) ← (CY) V bit	0	1	0	1	1	1	0	0				Bit Addr					10	2	
XOR	*CY, bit	(CY) ← (CY) ∀ (bit)	0	1	0	1	1	1	1	0				Bit Addr					10	2	
SETB	*bit	(bit) ← 1	0	1	0	1	1	0	0	0				Bit Addr					13	2	
CLR	*bit	(bit) ← 0	0	1	0	1	1	0	1	1				Bit Addr					13	2	
NOT	*bit	(bit) ← (bit)	0	1	0	1	1	0	0	1				Bit Addr					13	2	
SK	*bit	Skip if (bit) = 1	0	1	0	1	1	1	0	1				Bit Addr					10	2	(bit) = 1
SKN	*bit	Skip if (bit) = 0	0	1	0	1	0	0	0	0				Bit Addr					10	2	(bit) = 0

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
CPU Control																					
SK	f	Skip if f = 1	0	1	0	0	1	0	0	0	0	0	0	0	1	F_2	F_1	F_0	8	2	f = 1
SKN	f	Skip if f = 0	0	1	0	0	1	0	0	0	0	0	0	1	1	F_2	F_1	F_0	8	2	f = 0
SKIT	irf	Skip if irf = 1, then reset irf	0	1	0	0	1	0	0	0	0	1	0	I_4	I_3	I_2	I_1	I_0	8	2	irf = 1
SKNIT	irf	Skip if irf = 0 Reset irf if irf = 1	0	1	0	0	1	0	0	0	0	1	1	I_4	I_3	I_2	I_1	I_0	8	2	irf = 0
NOP		No operation	0	0	0	0	0	0	0	0									4	1	
EI		Enable interrupt	1	0	1	0	1	0	1	0									4	1	
DI		Disable interrupt	1	0	1	1	1	0	1	0									4	1	
HLT		Halt	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	1	11	2	

Note:

(1) In the case of skip condition, the idle states are as follows:
- 1-byte instruction: 4 states
- 2-byte instruction: 8 states
- 3-byte instruction: 11 states
- 2-byte instruction (with *): 7 states
- 3-byte instruction (with *): 10 states
- 4-byte instruction: 14 states

(2) B2 (Data): rpa2 = D + byte, H + byte.

(3) Right side of slash (/) in states indicates case rpa2, rpa3 = D + byte, H + A, H + B, H + EA, H + byte.

(4) B3 (Data): rpa3 = D + byte, H + byte

μPD7810/11
8-BIT, SINGLE-CHIP NMOS MICROCOMPUTERS WITH A/D CONVERTER

Description

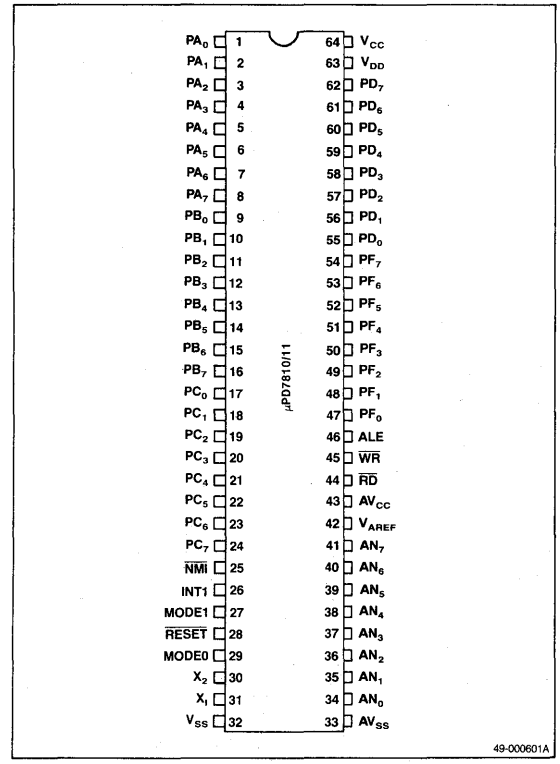
The μPD7810 and μPD7811 single-chip microcomputers integrate sophisticated on-chip peripheral functionality normally provided by external components. The device's internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make the μPD7810/11 appropriate in data processing as well as control applications. The devices integrate a 16-bit ALU, 4K-ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs on a single die, allowing their use in fast, high end processing applications. This involves analog signal interface and processing.

The μPD7811 is the mask-ROM high volume production device embedded with custom customer program. The μPD7810 is a ROM-less version for prototyping and small volume production. The μPD78PG11E is a piggy-back EPROM version for design development.

Features

- ☐ NMOS silicon gate technology requiring +5 V power supply
- ☐ Complete single-chip microcomputer
  - — 16-bit ALU
  - — 4K x 8 ROM
  - — 256-byte RAM
- ☐ 44 I/O lines
- ☐ Two zero-cross detect inputs
- ☐ Two 8-bit timers
- ☐ Expansion capabilities
  - — 8085A bus-compatible
  - — 60K-byte external memory address range
- ☐ 8-channel, 8-bit A/D converter
  - — Autoscan mode
  - — Channel select mode
- ☐ Full duplex USART
  - — Synchronous and asynchronous
- ☐ 153 instructions
  - — 16-bit arithmetic, multiply and divide
- ☐ 1 μs instruction cycle time (12 MHz operation)
- ☐ Prioritized interrupt structure
  - — 3 external
  - — 8 internal
- ☐ Standby function
- ☐ On-chip clock generator
- ☐ 64-pin plastic QUIP or shrink DIP

Pin Configuration



Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7810G-36 μPD7811G-36	64-pin plastic QUIP	12 MHz
μPD7810CW μPD7811CW	64-pin plastic shrink DIP	12 MHz

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Pin Identification

No.	Symbol	Function
1-8	PA_0-PA_7	Port A I/O
9-16	PB_0-PB_7	Port B I/O
17	PC_0/TxD	Port C I/O line 0/Transmit data output
18	PC_1/RxD	Port C I/O line 1/Receive data input
19	PC_2/$\overline{SCK}$	Port C I/O line 2/Serial clock I/O
20	PC_3/TI/$\overline{INT2}$	Port C I/O line 3/Timer input/Interrupt request 2 input
21	PC_4/TO	Port C I/O line 4/Timer output
22	PC_5/CI	Port C I/O line 5/Counter input
23, 24	PC_6, PC_7/CO_0, CO_1	Port C I/O lines 6, 7/Counter outputs 0, 1
25	$\overline{NMI}$	Nonmaskable interrupt input
26	INT1	Interrupt request 1 input
27	MODE1/$\overline{M1}$	Mode 1 input/Memory cycle 1 output
28	RESET	Reset input
29	MODE0/$\overline{IO}$/M	Mode 0 input/I/O/Memory output
30, 31	X2, X1	Crystal connections 1, 2
32	V_{SS}	Ground
33	AV_{SS}	Port T threshold voltage input
34-41	AN_0-AN_7	A/D converter analog inputs 0-7
42	V_{AREF}	A/D converter reference voltage
43	AV_{CC}	A/D converter power supply
44	$\overline{RD}$	Read strobe output
45	$\overline{WR}$	Write strobe output
46	ALE	Address latch enable output
47-54	PF_0-PF_7	Port F I/O/Expansiom memory address bus (bits 8-15)
55-62	PD_0-PD_7	Port D I/O/Expansion memory address/data bus
63	V_{DD}	RAM backup power supply
64	V_{CC}	5 V power supply

Pin Functions

PA_0-PA_7 [Port A]

Port A is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port A inputs.

PB_0-PB_7 [Port B]

Port B is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port B inputs.

PC_0-PC_7 [Port C]

Port C is an 8-bit three-state port. Each bit is independently programmable as either input or output. Alternatively, the lines of port C can be used as control lines for the USART and timer. Reset puts all lines of port C in port mode, input.

TxD [Transmit Data]. Serial data output terminal.

RxD [Receive Data]. Serial data input terminal.

$\overline{SCK}$ [Serial Clock]. Output for the serial clock when internal clock is used. Input for serial clock when external clock is used.

TI [Timer Input]. Timer input terminal.

$\overline{INT2}$ [Interrupt Request 2]. Falling-edge-triggered, maskable interrupt input terminal and AC-input, zero-cross detection terminal.

TO [Timer Output]. The output of TO is a square wave with a frequency determined by the timer/counter.

CI [Counter Input]. External pulse input to timer/event counter.

CO_0, CO_1 [Counter Outputs 0, 1]. Programmable rectangular wave outputs based on timer/event counter.

PD_0-PD_7 [Port D]

Port D is an 8-bit three-state port. It can be programmed as either 8 bits of input or 8 bits of output. When external expansion memory is used, port D acts as the multiplexed address/data bus.

PF_0-PF_7 [Port F]

Port F is an 8-bit three-state port. Each bit is independently programmable as an input or output. When external expansion memory is used, port F outputs the high-order address bits.

AN_0-AN_7

These are the eight analog inputs to the A/D converter. AN_4-AN_7 can also be used as a digital input for falling edge detection.

AV_{SS} [A/D Converter Power Ground]

AV_{SS} is the ground potential for the A/D converter power supply.

$\overline{NMI}$ [Nonmaskable Interrupt]

Falling-edge-triggered nonmaskable interrupt input.

INT1 [Interrupt Request 1]

INT1 is a rising-edge-triggered, maskable interrupt input. It is also an AC-input, zero-cross detection terminal.

$\overline{\text{RESET}}$ [Reset]

When the $\overline{\text{RESET}}$ input is brought low, it initializes the μPD7810/11.

MODE1, MODE0 [Mode 1, 0]

The MODE1 and MODE0 inputs select the memory expansion mode. MODE1 also outputs the M1 signal during each opcode fetch. MODE0 outputs the $\overline{\text{IO}}$/M signal.

V_{AREF} [A/D Converter Reference]

V_{AREF} set the upper limit for the A/D converter's conversion range.

AV_{CC} [A/D Converter Power]

This is the power supply voltage for the A/D converter.

$\overline{\text{RD}}$ [Read Strobe]

The $\overline{\text{RD}}$ output goes low to gate data from external devices onto the data bus. $\overline{\text{RD}}$ goes high during reset.

$\overline{\text{WR}}$ [Write Strobe]

The $\overline{\text{WR}}$ output goes low to indicate that the data bus holds valid data. It is a strobe signal for external memory or I/O write operations. $\overline{\text{WR}}$ goes high during reset.

ALE [Address Latch Enable]

The ALE output latches the address signal to the output of PD_0-PD_7.

X1, X2 [Crystal Connections 1, 2]

X1 and X2 are the system clock crystal oscillator terminals. X1 is the input for an external clock.

V_{SS} [Ground]

Ground potential.

V_{DD} [Backup Power]

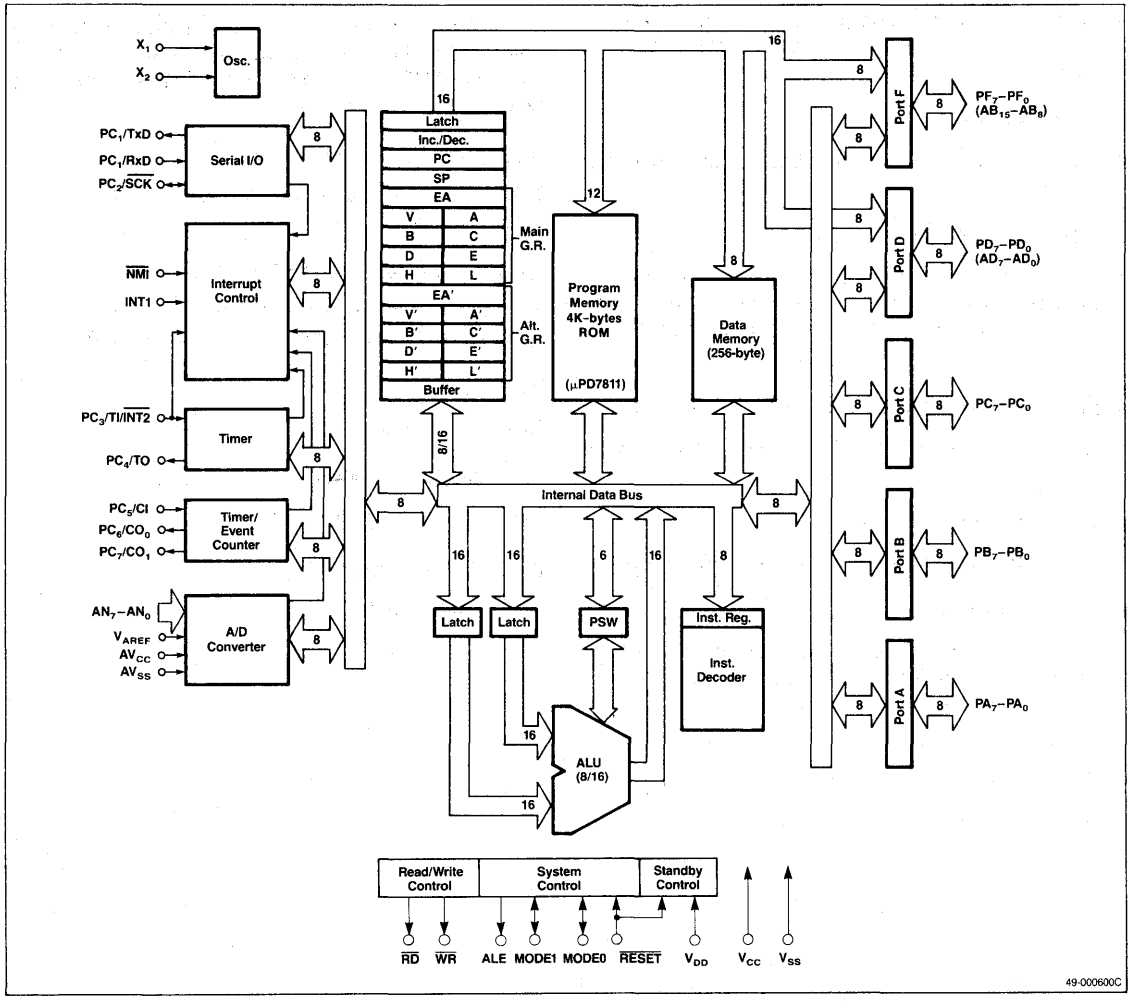
Backup power for on-chip RAM.

V_{CC} [Power Supply]

+5 V power supply.

4

Block Diagram



Functional Description

Memory Map

The μPD7811 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65280-65535), any memory location can be used as ROM or RAM. The memory map, figure 1, defines the 0 to 64K byte memory space for the μPD7811.

Input/Output

The μPD7810/11 has 8 analog input lines (AN_0-AN_7), 44 digital I/O lines, five 8-bit ports (port A, port B, port C, port D, port F), and 4 input lines (AN_4-AN_7).

Analog Input Lines. AN_0-AN_7 are configured as analog input lines for on-chip A/D converter.

Port A, Port B, Port C, Port F. Each line of these ports can be individually programmed as an input or output. When used as I/O ports, all have latched outputs and high-impedance inputs.

Port D. Port D can be programmed as a byte input or a byte output.

AN_4-AN_7. The high order analog input lines, AN_4-AN_7, can be used as digital input lines for falling edge detection.

Control Lines. Under software control, each line of port C can be configured individually to provide control lines for the serial interface, timer, and timer/counter.

Memory Expansion. In addition to the single-chip operation mode, the μPD7811 has four memory expansion modes. Under software control, port D can provide a multiplexed low-order address and data bus; port F can provide a high-order address bus. Table 1 shows the relation between memory expansion modes and the pin configurations of port D and port F.

Table 1. Memory Expansion Modes and Port Configurations

Memory Expansion	Port Configuration	
None	Port D	I/O port
	Port F	I/O port
256 Bytes	Port D	Multiplexed address/data bus
	Port F	I/O port
4K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_3	Address bus
	Port F_4-F_7	I/O port
16K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_5	Address bus
	Port F_6-F_7	I/O port
60K Bytes	Port D	Multiplexed address/data bus
	Port F	Address bus

Timers

There are two 8-bit timers. The timers may be programmed independently or may be cascaded and used as an 8-bit timer with 8-bit prescaler. The timer can be software set to increment at intervals of four machine cycles (1 μs at 12 MHz operation) or 128 machine cycles (32 μs at 12 MHz), or to increment on receipt of a pulse at TI. Figure 2 shows the block diagram for the timer.

Timer/Event Counter

The 16-bit multifunctional timer/event counter (figure 3) can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output

Figure 1. Memory Map

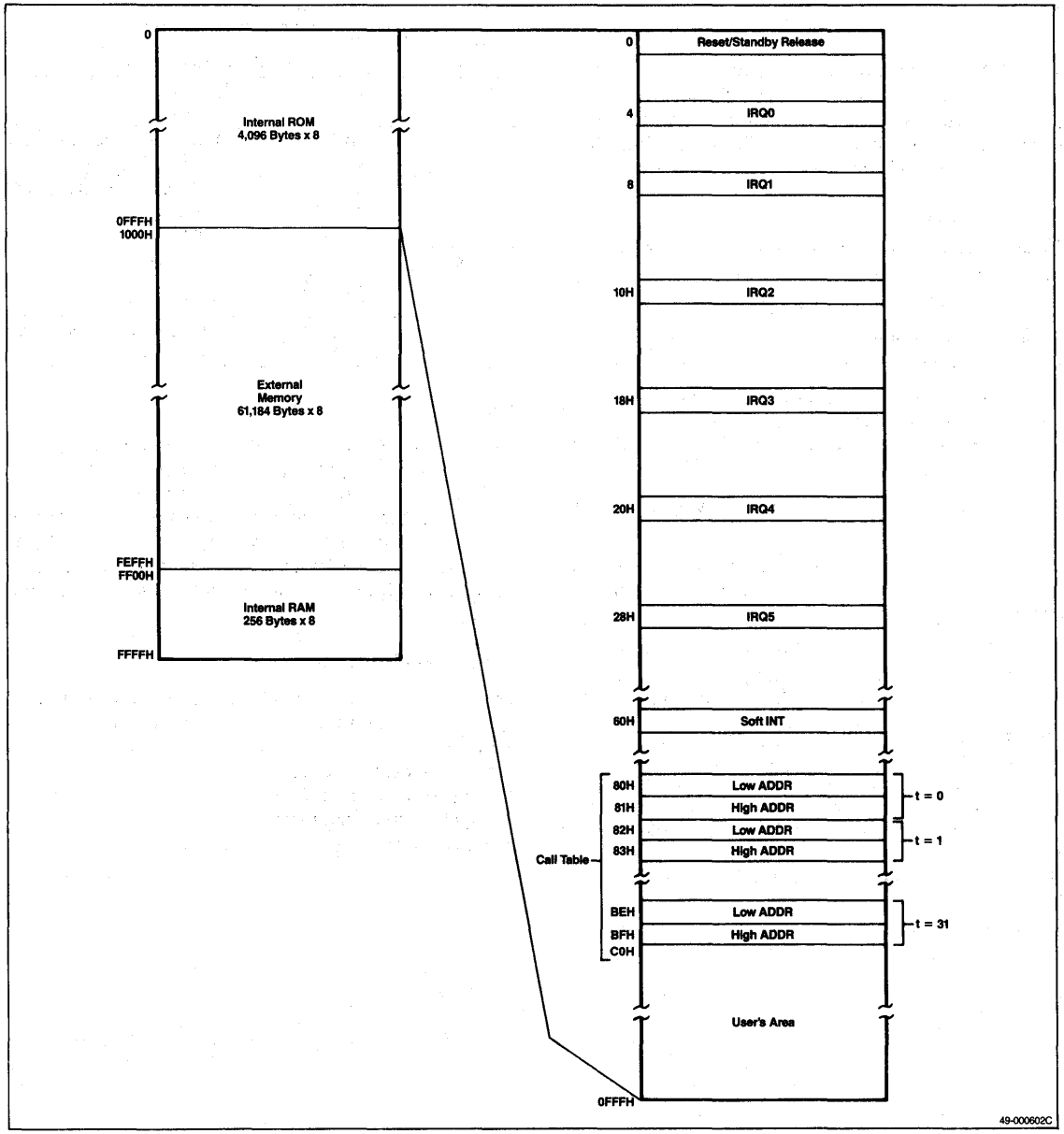
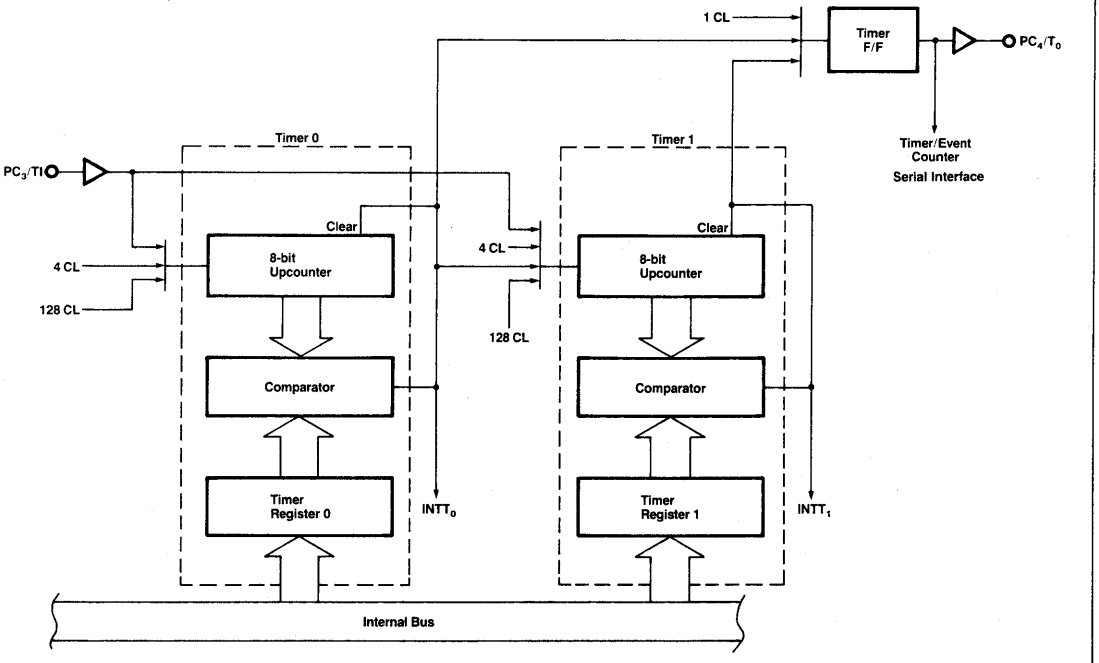


Figure 2. Timer Block Diagram

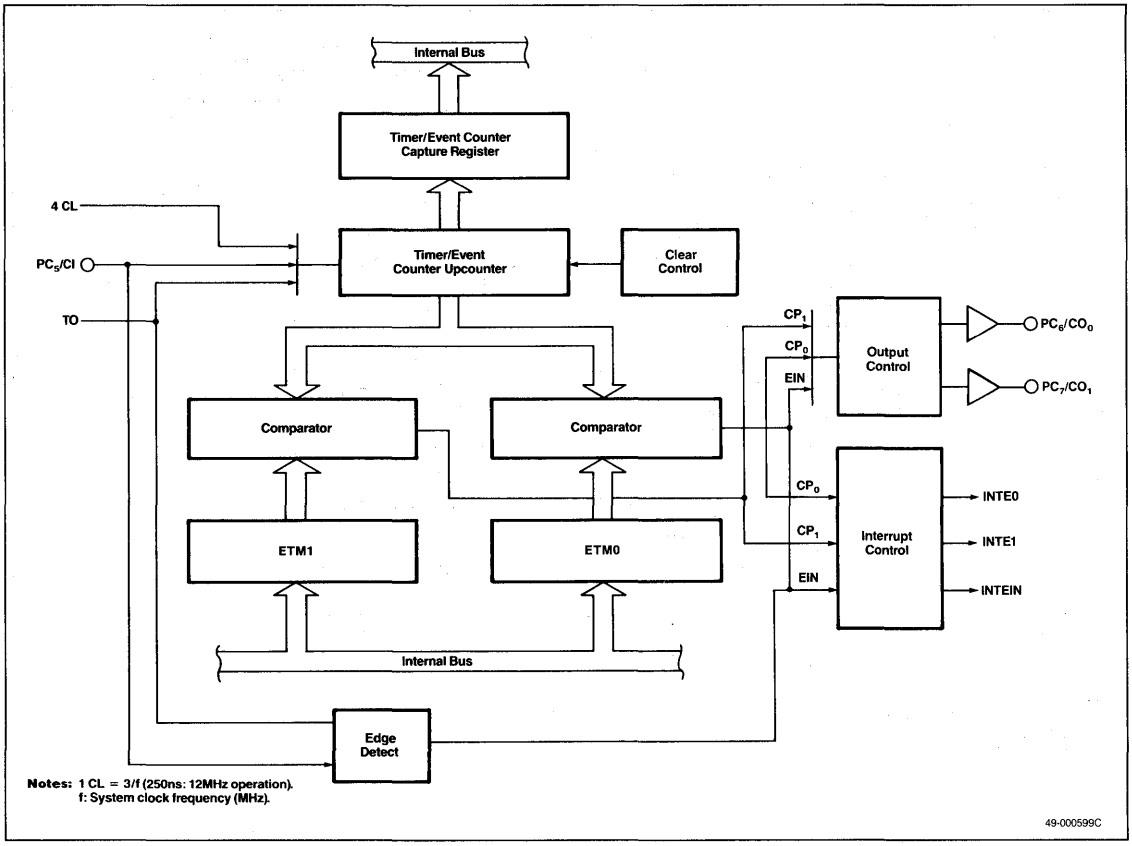


Notes: 1 CL = 3/f (250ns: 12MHz operation).
f: System clock frequency (MHz).

49-000590B

4

Figure 3. Block Diagram for Timer/Event Counter



8-Bit A/D Converter

- 8 input channels
- 4 conversion result registers
- 2 powerful operation modes
  - — Autoscan mode
  - — Channel select mode
- Successive approximation technique
- Absolute accuracy: ±1.5 LSB (±0.6%)
- Conversion range: 0 to 5 V
- Conversion time: 48 μs
- Interrupt generation

Analog/Digital Converter

The μPD7810/11 features an 8-bit, high speed, high accuracy A/D converter. The A/D converter is made up of a 256-resistor ladder and a successive approximation register (SAR). There are four conversion result registers (CR_0-CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0-CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers. Figure 4 shows the block diagram for the A/D converter.

Interrupt Structure

There are 11 interrupt sources. Three are external interrupts and eight are internal. The following, table 2, shows 11 interrupt sources divided into six priority levels. See figure 5.

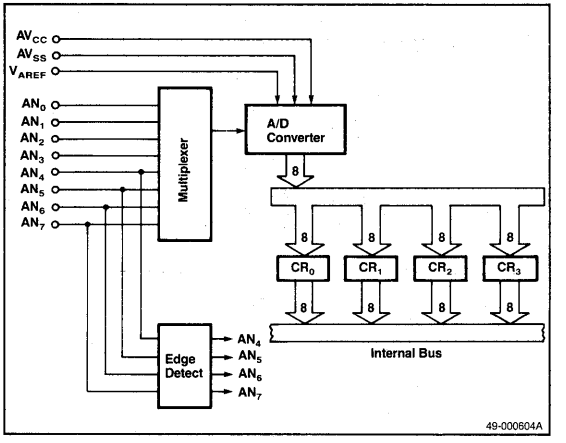
Standby Function

The standby function saves the top 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On power-up, you can check the standby flag (SB) to determine whether recovery was made from standby mode or from a cold start.

Table 2. Interrupt Sources

Interrupt Request	Interrupt Address	Type of Interrupt	Internal/ External
IRQ0	4	$\overline{NMI}$ (Nonmaskable interrupt)	Ext
IRQ1	8	INTT0 (Coincidence signal from timer 0)	Int
		INTT1 (Coincidence signal from timer 1)	
IRQ2	16	INT1 (Maskable interrupt)	Ext
		$\overline{INT2}$ (Maskable interrupt)	
IRQ3	24	INTE0 (Coincidence signal from timer/event counter)	Int
		INTE1 (Coincidence signal from timer/event counter)	
IRQ4	32	INTEIN (Falling signal of CI and TO counter)	Int/Ext
		INTAD (A/D converter interrupt)	
IRQ5	40	INTSR (Serial receive interrupt)	Int
		INST (Serial send interrupt)	

Figure 4. A/D Converter Block Diagram



Universal Serial Interface

The serial interface can operate in one of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first, for easy interfacing to certain NEC peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception: search and nonsearch. In the search mode, data is transferred one bit at a time from the serial register to the receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from the serial register to the transmit buffer occurs eight bits at a time. Figure 6 shows the universal serial interface block diagram.

Figure 5. Interrupt Structure Block Diagram

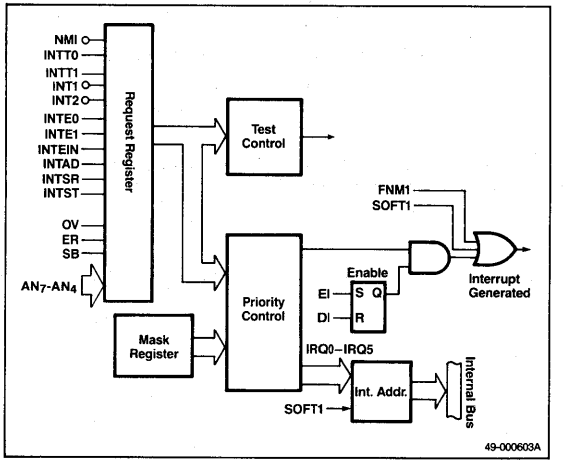
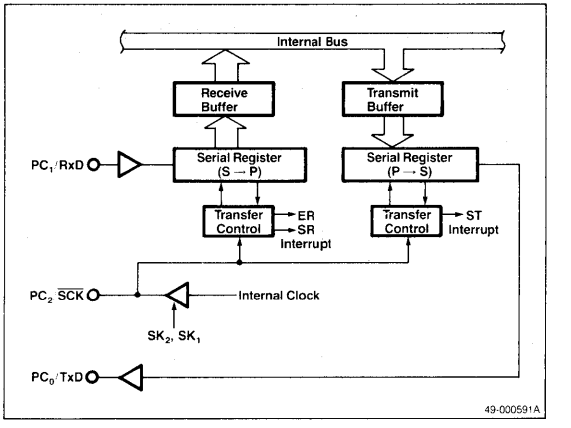


Figure 6. Universal Signal Interface Block Diagram



Zero-Crossing Detector

The INT1 and $\overline{INT2}$ terminals (used common to TI and PC_3) can detect the zero-crossing point of low-frequency AC signals. When driven directly, these pins respond as a normal digital input. Figure 7 shows the zero-crossing detection circuitry.

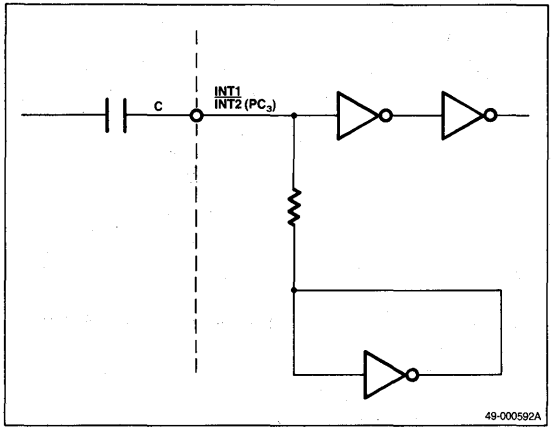
The zero-crossing detection capability allows you to make the 50-60 Hz power signal the basis for system timing and to control voltage phase-sensitive devices.

To use the zero-cross detection mode, an AC signal of approximately 1-3 V AC (peak-to-peak) and a maximum frequency of 1 kHz is coupled through an external capacitor to the INT1 and $\overline{INT2}$ pins.

For the INT1 pin, the internal digital state is sensed as a 0 until the rising edge crosses the average DC level, when it becomes a 1 and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a 1 until the falling edge crosses the average DC level, when it becomes a 0 and $\overline{INT2}$ interrupt is generated.

Figure 7. Zero-Crossing Detection Circuit



Absolute Maximum Ratings

Power supply voltages,	V_{CC}	−0.5 V to +7.0 V
	V_{DD}	−0.5 V to +7.0 V
	AV_{CC}	−0.5 V to +7.0 V
	AV_{SS}	−0.5 V to +0.5 V
Input voltage, V_I		−0.5 V to +7.0 V
Output voltage, V_O		−0.5 V to +7.0 V
Reference input voltage, V_{AREF}		−0.5 V to V_{CC}
Operating temperature, T_{OPR} 10 MHz ≤ f_{XTAL} ≤ 12 MHz		−10°C to +70°C
f_{XTAL} ≤ 10 MHz		−40°C to −85°C
Storage temperature, T_{STG}		−65°C to +150°C

Comment: Exposing the device to stresses above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

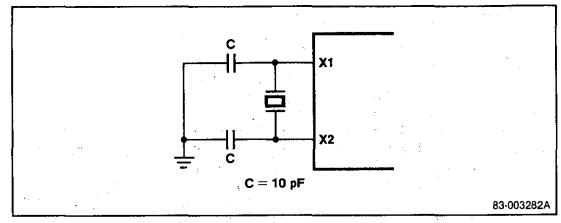
Oscillating Frequency	T_A	V_{CC}, AV_{CC}
f_{XTAL} ≤ 10 MHz	−40°C to +85°C	+5.0 V ±10%
10 MHz ≤ f_{XTAL} ≤ 12 MHz	−10°C to +70°C	+5.0 V ±5%

Capacitance

T_A = 25°C; V_{CC} = V_{DD} = V_{SS} = 0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Capacitance	C_I			10	pF	Af_c = 1 MHz. Unmeasured pins returned to 0 V.
Output capacitance	C_O			20	pF	
I/O capacitance	C_{IO}			20	pF	

Recommended XTAL Oscillation Circuit



DC Characteristics

$T_A = -10°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 5\%$; $V_{SS} = 0\ V$; $V_{DD} = V_{CC} - 0.8\ V$ to V_{CC}

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	0		0.8	V	
Input high voltage	V_{IH1}	2.0		V_{CC}	V	All except $\overline{SCK}$, RESET, X1 and X2
	V_{IH2}	0.8 V_{CC}		V_{CC}	V	$\overline{SCK}$, X1, X2
	V_{IH3}	0.8 V_{DD}		V_{CC}	V	RESET
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 2.0\ mA$
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -200\ \mu A$
Data retention voltage	V_{DDDR}	3.2			V	$V_{CC} = 0\ V$; $\overline{RESET} = V_{IL}$
Input current	I_I			±200	μA	INT1, TI(PC_3); $+0.45\ V \le V_I < V_{CC}$
Input leakage current	I_{LI}			±10	μA	All except INT, TI(PC_3) $0\ V \le V_I \le V_{CC}$
Output leakage current	I_{LO}			±10	μA	$+0.45\ V \le V_O \le V_{CC}$
AV_{CC} supply current	AI_{CC}		6	12	mA	
V_{DD} supply current	I_{DD}		1.5	3.5	mA	$T_A = -40$ to $+85°C$
				3.2	mA	$V_{CC} = V_{DD} = 5\ V$ $T_A = -10$ to $+70°C$
V_{CC} supply current	I_{CC}		150	220	mA	$T_A = -40$ to $+85°C$; $V_{CC} = V_{DD} = 5\ V$

Serial Operation

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{CYK}	1		μs	$\overline{SCK}$ input (1)
		500		ns	(2)
		2		μs	$\overline{SCK}$ output
$\overline{SCK}$ width low	t_{KKL}	750		ns	$\overline{SCK}$ input(1)
		200		ns	$\overline{SCK}$ input (2)
		900		ns	$\overline{SCK}$ output
$\overline{SCK}$ width high	t_{KKH}	750		ns	$\overline{SCK}$ input (1)
		200		ns	$\overline{SCK}$ input (2)
		900		ns	$\overline{SCK}$ output
RxD set-up time to SCK ↑	t_{RXK}	80		ns	(1)
RxD hold time after $\overline{SCK}$ ↑	t_{KRX}		80	ns	(1)
$\overline{SCK}$ ↓ TxD delay time	t_{KTX}		210	ns	(1)

Note:

(1) 1x baud rate in asynchronous, synchronous, or I/O interface mode.

(2) 16x baud rate or 64x baud rate in asynchronous mode.

Zero-Cross Characteristics

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Zero-cross detection input	V_{ZX}	1	3	V ac, p-p	Ac coupled
Zero-cross accuracy	A_{ZX}		±135	mV	60-Hz sine wave
Zero-cross detection input frequency	f_{ZX}	0.05	1	kHz	

AC Characteristics

Read/Write Operation

$V_{SS} = 0\ V$, $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits $f_{XTAL} = 10$ MHz Min	Limits $f_{XTAL} = 10$ MHz Max	Limits $f_{XTAL} = 12$ MHz Min	Limits $f_{XTAL} = 12$ MHz Max	Unit	Test Conditions (1)
$\overline{RESET}$ pulse width	t_{RP}	6.0		5.0		μs	
Interrupt pulse width	t_{IP}	3.6		3.0		μs	
Counter input pulse width	t_{CI}	600		500		ns	Event counter mode
	t_{CI}	4.8		4.0		μs	Pulse width measurement mode
Timer input pulse width	t_{TI}	600		500		ns	
X1 Input cycle time	t_{CYC}	100	250	83	250	ns	
Address set-up to ALE ↓	t_{AL}	100		65		ns	
Address hold after ALE ↓	t_{LA}	70		50		ns	
Address to RD ↓ delay time	t_{AR}	200		150		ns	
$\overline{RD}$ ↓ to address floating	t_{AFR}		20		20	ns	
Address to data input	t_{AD}		480		360	ns	
ALE ↓ to data input	t_{LDR}		300		215	ns	
$\overline{RD}$ ↓ to data input	t_{RD}		250		180	ns	
ALE ↓ to RD ↓ delay time	t_{LR}	50		35		ns	
Data hold time to $\overline{RD}$ ↑	t_{RDH}	0		0		ns	
$\overline{RD}$ ↑ to ALE ↑ delay time	t_{RL}	150		115		ns	
$\overline{RD}$ width low	t_{RR}	350		280		ns	Data read
		650		530		ns	Opcode fetch
ALE width high	t_{LL}	160		125		ns	
$\overline{M1}$ setup time to ALE ↓	t_{ML}	100		65		ns	
$\overline{M1}$ hold time after ALE ↓	t_{LM}	70		50		ns	
$\overline{IO}$/M setup time to ALE ↓	t_{IL}	100		65		ns	
$\overline{IO}$/M hold time after ALE ↓	t_{LI}	70		50		ns	
Address to $\overline{WR}$ ↓ delay	t_{AW}	200		150		ns	
ALE ↓ to data output	t_{LDW}		210		195	ns	
$\overline{WR}$ ↓ to data output	t_{WD}		100		100	ns	
ALE ↓ to $\overline{WR}$ ↓ delay	t_{LW}	50		35		ns	
Data set-up time to $\overline{WR}$ ↑	t_{DW}	300		230		ns	
Data hold time to $\overline{WR}$ ↑	t_{WDH}	130		95		ns	
$\overline{WR}$ ↑ to ALE ↑ delay time	t_{WL}	150		115		ns	
$\overline{WR}$ width low	t_{WW}	350		280		ns	

Note:

(1) Load capacitance: $C_L = 150$ pF.

A/D Converter Characteristics

$T_A = -10°C$ to $+70°C$; $V_{CC} = AV_{CC} = 5.0\ V \pm 5\%$; $V_{SS} = AV_{SS} = 0\ V$; $V_{AREF} = AV_{CC} - 0.5\ V$ to AV_{CC}.

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Resolution		8			Bits	
Absolute accuracy				0.4% ± 1/2	LSB	$T_A = -10°C$ to $+50°C$
				0.6% ±1/2	LSB	$T_A = -10°C$ to $+70°C$ (Note 1)
Conversion time	t_{CONV}	576			t_{CYC}	83 ns ≤ t_{CYC} ≤ 110 ns
		432			t_{CYC}	110 ns ≤ t_{CYC} ≤ 170 ns
Sampling time	t_{SAMP}	96			t_{CYC}	83 ns ≤ t_{CYC} ≤ 110 ns
		72			t_{CYC}	110 ns ≤ t_{CYC} ≤ 170 ns
Analog input voltage	V_{IA}	0		V_{AREF}	V	
Analog resistance	R_{AN}		1000		MΩ	
Analog reference current	I_{AREF}	0.2	0.5	1.5	mA	

Note:

(1) In case of $f_{XTAL} \leq 10$ MHz, $T_A = -40°C$ to $+85°C$.

Bus Timing Depending on t_{CYC}

Symbol	Calculating Expression	Min/Max
t_{RP}	60T	Min
t_{TI}	6T	Min
t_{CI}(2)	6T	Min
t_{CI}(3)	48T	Min
t_{IP}	36T	Min
t_{AL}	2T − 100	Min
t_{LA}	T − 30	Min
t_{AR}	3T − 100	Min
t_{AD}	7T − 220	Max
t_{LDR}	5T − 200	Max
t_{RD}	4T − 150	Max
t_{LR}	T − 50	Min
t_{RL}	2T − 50	Min
t_{RR}	4T − 50 (Data Read) 7T − 50 (Opcode Fetch)	Min
t_{LL}	2T − 40	Min
t_{AW}	3T −100	Min
t_{LDW}	T + 110	Max
t_{LW}	T − 50	Min
t_{DW}	4T − 100	Min
t_{WDH}	2T − 70	Min
t_{WL}	2T − 50	Min
t_{WW}	4T − 50	Min
t_{CYK}	20T ($\overline{SCK}$ input)(1) 24T ($\overline{SCK}$ output)	Min
t_{KKL}	10T − 80 ($\overline{SCK}$ input)(1) 12T − 100 ($\overline{SCK}$ output)	Min
t_{KKH}	10T − 80 ($\overline{SCK}$ input)(1) 12T − 100 ($\overline{SCK}$ output)	Min

Note:

(1) 1x Baud rate in asynchronous, synchronous, or I/O interface mode.
$T = t_{CYC} = 1/f_{XTAL}$.
The items not included in this list are independent of oscillator frequency (f_{XTAL}).

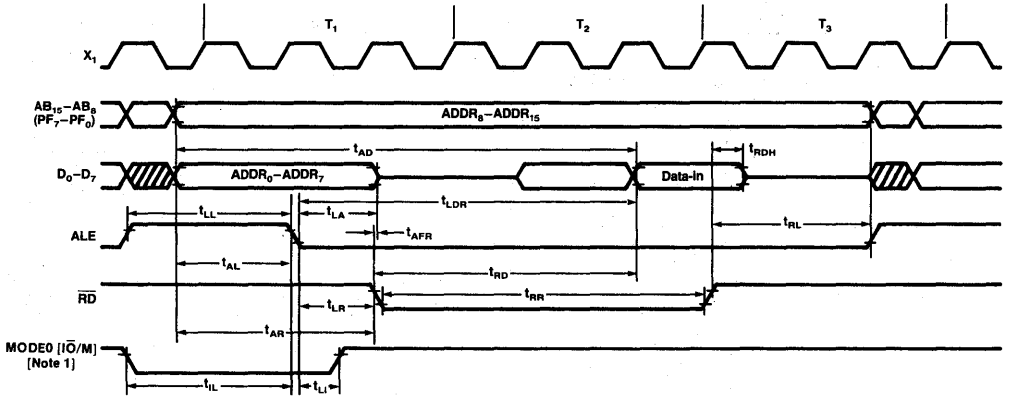
(2) Event counter mode.

(3) Pulse width measurement mode.

4

Timing Waveforms

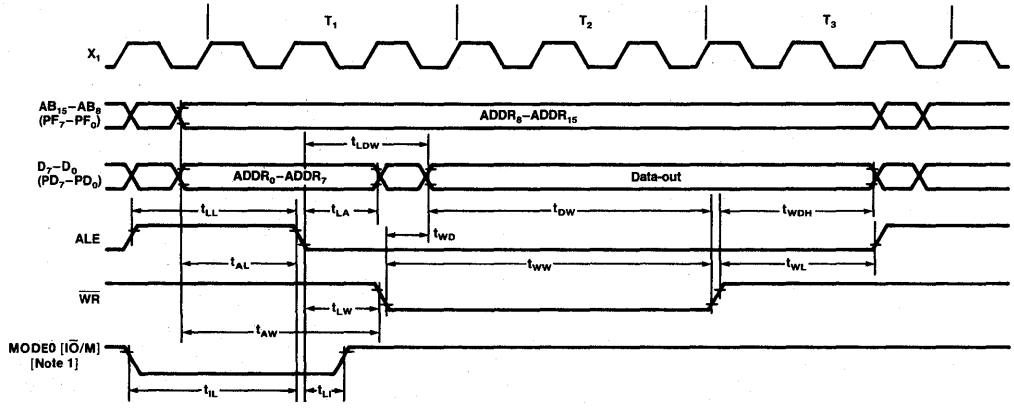
Read Operation



Note: [1] IO/M signal is output to the MODE0 pin during a read or write of special register[s] Sr-Sr2, if MODE0 is pulled up to V_{CC}.

49-000543B

Write Operation

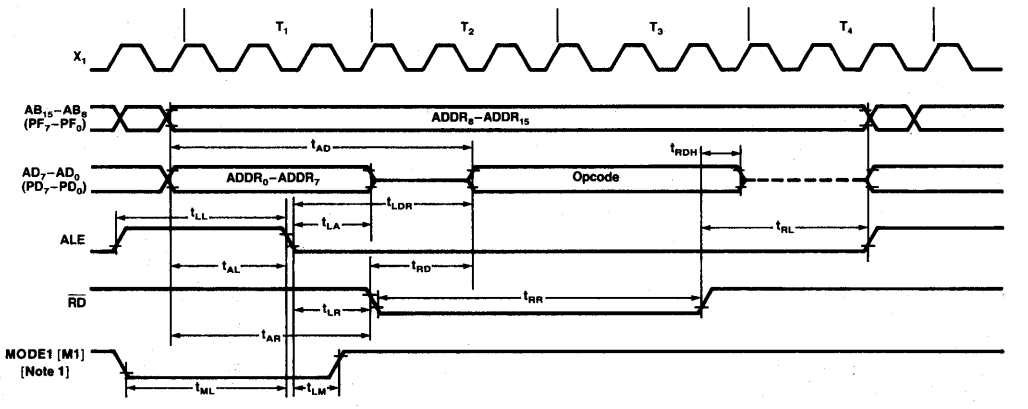


Note: [1] IO/M signal is output to the MODE0 pin during a read or write of special register[s] Sr-Sr2, if MODE0 is pulled up to V_{CC}.

49-000639B

Timing Waveforms (cont)

Opcode Fetch Operation

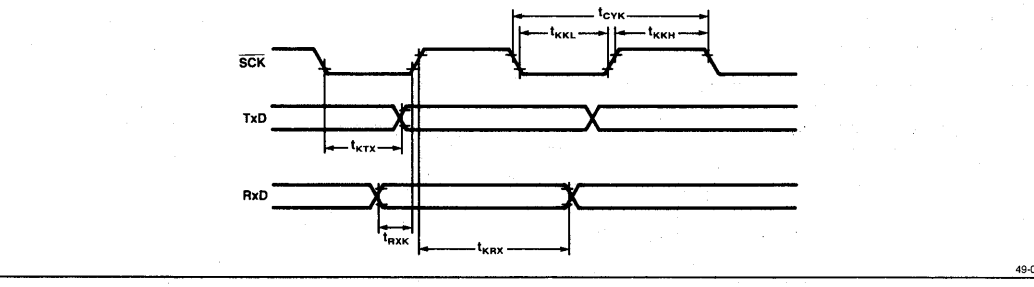


Note:

[1] M1 signal is output to the MODE1 pin during Opcode Fetch if MODE1 pin is pulled up to V_{CC}.

49-000545B

Serial Operation Transmit/Receive Timing



49-000546B

Operand Format/Description

Format	Description
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TxB, TM_0, TM_1
sr1	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3
sr2	PA, PB, PC, PD, PF, MKH, ANM, MKL, SMH, EOM, TMM
sr3	ETM_0, ETM_1
sr4	ECNT, ECPT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D−, H−, D + byte, H + A, H + B, H + EA, H + byte
rpa3	D, H, D++, H++, D + byte, H + A, H + B, H + EA, H + byte
wa	8-Bit immediate data
word	16-Bit immediate data
byte	8-Bit immediate data
bit	3-Bit immediate data
f	CY, HC, Z
irf	FNMI, FT0, FT1, F1, F2, FE0, FE1, FEIN, FAD, FSR, FST, ER, 0V, AN_4, AN_5, AN_6, AN_7, SB

Instruction Set Symbol Definitions

Symbol	Description
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
∀	Exclusive OR
—	Complement
•	Concatenation

Remarks

1. sr-sr4 (special register)

PA = Port A
PB = Port B
PC = Port C
PD = Port D
PF = Port F
MA = Mode A
MB = Mode B
MC = Mode C
MCC = Mode Control C
MF = Mode F

MM = Memory Mapping
TM_0 = Timer Register 0
TM_1 = Timer Register 1
TMM = Timer Mode
ETM_0 = Timer/Event Counter Register 0
ETM_1 = Timer/Event Counter Register 1

ECNT = Timer/Event Counter Upcounter
ECPT = Timer/Event Counter Capture

ETMM = Timer/Event Counter Mode
EOM = Timer/Event Counter Output Mode

TxB = TX Buffer
RxB = RX Buffer
SMH = Serial Mode High
SML = Serial Mode Low
MKH = Mask High
MKL = Mask Low
ANM = A/D Channel Mode
CR_0 = A/D Conversion Result 0-3 to CR_3

2. rp-rp3 (register pair)

SP = Stack Pointer
B = BC
D = DE
H = HL
V = VA
EA = Extended Accumulator

3. rpa-rpa3 (rp addressing)

B = (BC)
D = (DE)
H = (HL)
D+ = (DE) +
H− = (HL) +
D− = (DE) −
H− = (HL) −
D++ = (DE) ++
H++ = (HL) ++
D + byte = (DE) + byte
H + A = (HL) + (A)
H + B = (HL) + (B)
H + EA = (HL) + (EA)
H + byte = (HL) + byte

4. f (flag)

CY = Carry HC = Half Carry Z = Zero

5. irf (interrupt flag)

NMI = NMI* Input
FT0 = INTFT0
FT1 = INTFT1
F1 = INTF1
F2 = INTF2
FE0 = INTFE0
FE1 = INTFE1

FEIN = INTFEIN
FAD = INTFAD
FSR = INTFSR
FST = INTFST
ER = Error
0V = Overflow
AN_4 to AN_7 = Analog Input 4-7
SB = Standby

Instruction Set

Mnemonic	Operand	Operation	Operation Code B1 7	6	5	4	3	2	1	0	B2 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Data Transfer																					
MOV	r1,A	(r1) ← (A)	0	0	0	1	1	T_2	T_1	T_0									4	1	
	A, r1	(A) ← (r1)	0	0	0	0	1	T_2	T_1	T_0									4	1	
	*sr,A	(sr) ← (A)	0	1	0	0	1	1	0	1	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	*A,sr1	(A) ← (sr1)	0	1	0	0	1	1	0	0	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	r,word	(r) ← (word)	0	1	1	1	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
	word,r	(word) ← (r)	0	1	1	1	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
MVI	*r,byte	(r) ← byte set L1 if r = A set L0 if r = L	0	1	1	0	1	R_2	R_1	R_0	Data								7	2	L1 = 1 and r = A L0 = 1 and r = L
	sr2,byte	(sr2) ← byte	0	1	1	0	0	1	0	0	S_3	0	0	0	0	S_2	S_1	S_0	14	3	
			Data																		
MVIW	*wa, byte	((V)•(wa)) ← byte	0	1	1	1	0	0	0	1	Offset								13	3	
			Data																		
MVIX	*rpa1,byte	(rpa1) ← byte	0	1	0	0	1	0	A_1	A_0	Data								10	2	
STAW	*wa	((V)•(wa)) ← A	0	1	1	0	0	0	1	1	Offset								10	2	
LDAW	*wa	(A) ← ((V)•(wa))	0	0	0	0	0	0	0	1	Offset								10	2	
STAX	*rpa2	(rpa2) ← (A)	A_3	0	1	1	1	A_2	A_1	A_0	Data (2)								7/13(3)	2	
LDAX	*rpa2	(A) ← ((rpa2))	A_3	0	1	0	1	A_2	A_1	A_0	Data (2)								7/13(3)	2	
EXX		(B) ↔ (B'),(C) ↔ (C'),(D) ↔ (D') (E) ↔ (E'),(H) ↔ (H'),(L) ↔ (L')	0	0	0	1	0	0	0	1									4	1	
EXA		(V) ↔ (V'),(A) ↔ (A'),(EA) ↔ (EA')	0	0	0	1	0	0	0	0									4	1	
EXH		(H) ↔ (H'),(L) ↔ (L')	0	1	0	1	0	0	0	0									4	1	
16-Bit Data Transfer																					
BLOCK	D	((DE)) ← ((HL)),(DE) ← (DE + 1), (HL) ← (HL) + 1, (C) ← (C) − 1 End if borrow	0	0	1	1	0	0	0	1									13 x (C + 1)	1	
DMOV	rp3, EA	($rp3_L$) ← (EAL),($rp3_H$) ← (EAH)	1	0	1	1	0	1	P_1	P_0									4	1	
	EA,rp3	(EAL) ← ($rp3_L$),(EAH) ← ($rp3_H$)	1	0	1	0	0	1	P_1	P_0									4	1	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
			B1			B3					B2			B4							
16-Bit Data Transfer (cont)																					
DMOV	sr3, EA	(sr3) ← (EA)	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1	U_0	14	2	
	EA,sr4	(EA) ← (sr4)	0	1	0	0	1	0	0	0	1	1	0	0	0	0	V_1	V_0	14	2	
SBCD	word	(word) ← (C), (word + 1) ← (B)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	20	4	
			Low addr								High addr										
SDED	word	(word) ← (E), (word + 1) ← (D)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	0	20	4	
			Low addr								High addr										
SHLD	word	(word) ← (L), (word + 1) ← (H)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	20	4	
			Low addr								High addr										
SSPD	word	(word) ← (SP_L),(word + 1) ← (SP_H)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	20	4	
			Low addr								High addr										
STEAX	rpa3	((rpa3)) ← (EAL),((rpa3) + 1 ← (EAH)	0	1	0	0	1	0	0	0	1	0	0	1	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
LBCD	word	(C) ← (word),(B) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	20	4	
			Low addr								High addr										
LDED	word	(E) ← (word),(D) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	20	4	
			Low addr								High addr										
LHLD	word	(L) ← (word),(H) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	20	4	
			Low addr								High addr										
LSPD	word	(SP_L) ← (word),(SP_H) ← ((word) + 1)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	20	4	
			Low addr								High addr										
LDEAX	rpa3	(EAL) ← ((rpa3)),(EAH) ← ((rpa3) + 1)	0	1	0	0	1	0	0	0	1	0	0	0	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
PUSH	rp1	((SP) − 1) ← ($rp1_H$) ((SP) − 2) ← ($rp1_L$) (SP) ← (SP) − 2	1	0	1	1	0	Q_2	Q_1	Q_0									13	1	
POP	rp1	($rp1_L$) ← ((SP)),($rp1_H$) ← ((SP) + 1) (SP) ← (SP) + 2	1	0	1	0	0	Q_2	Q_1	Q_0									10	1	
LXI	*rp2,word	(rp2) ← (word) set L0 if rp2 = H	0	P_2	P_1	P_0	0	1	0	0	Low byte								10	3	L0 = 1 and rp2 = H
			High byte																		
TABLE		(C) ← ((PC)+3+(A)),B ← ((PC)+3+(A)+ 1)	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	0	17	2	
8-Bit Arithmetic (Register)																					
ADD	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	1	0	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	1	0	0	0	R_2	R_1	R_0	8	2	
ADC	A,r	(A) ← (A) + (r) + (CY)	0	1	1	0	0	0	0	0	1	1	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A) + (CY)	0	1	1	0	0	0	0	0	0	1	0	1	0	R_2	R_1	R_0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Arithmetic [Register] (cont)																					
ADDNC	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	0	1	0	0	R_2	R_1	R_0	8	2	No carry
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	0	1	0	0	R_2	R_1	R_0	8	2	No carry
SUB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	0	R_2	R_1	R_0	8	2	
SBB	A,r	(A) ← (A) − (r) − (CY)	0	1	1	0	0	0	0	0	1	1	1	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A) − (CY)	0	1	1	0	0	0	0	0	0	1	1	1	0	R_2	R_1	R_0	8	2	
SUBNB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
ANA	A,r	(A) ← (A) ∧ (r)	0	1	1	0	0	0	0	0	1	0	0	0	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∧ (A)	0	1	1	0	0	0	0	0	0	0	0	0	1	R_2	R_1	R_0	8	2	
ORA	A,r	(A) ← (A) ∨ (r)	0	1	1	0	0	0	0	0	1	0	0	1	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∨ (A)	0	1	1	0	0	0	0	0	0	0	0	1	1	R_2	R_1	R_0	8	2	
XRA	A,r	(A) ← (A) ∀ (r)	0	1	1	0	0	0	0	0	1	0	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∀ (A)	0	1	1	0	0	0	0	0	0	0	0	1	0	R_2	R_1	R_0	8	2	
GTA	A,r	(A) − (r) − 1	0	1	1	0	0	0	0	0	1	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) − (A) − 1	0	1	1	0	0	0	0	0	0	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
LTA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
NEA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	1	R_2	R_1	R_0	8	2	No zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	8	2	No zero
EQA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	1	1	R_2	R_1	R_0	8	2	Zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	8	2	Zero
ONA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	0	1	R_2	R_1	R_0	8	2	No zero
OFFA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	1	1	R_2	R_1	R_0	8	2	Zero
8-Bit Arithmetic (Memory)																					
ADDX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	0	A_2	A_1	A_0	11	2	
ADCX	rpa	(A) ← (A) + ((rpa)) + (CY)	0	1	1	1	0	0	0	0	1	1	0	1	0	A_2	A_1	A_0	11	2	
ADDNCX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	0	1	0	0	A_2	A_1	A_0	11	2	No carry
SUBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	0	A_2	A_1	A_0	11	2	
SBBX	rpa	(A) ← (A) − ((rpa)) − (CY)	0	1	1	1	0	0	0	0	1	1	1	1	0	A_2	A_1	A_0	11	2	
SUBNBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	0	A_2	A_1	A_0	11	2	No borrow
ANAX	rpa	(A) ← (A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	0	1	A_2	A_1	A_0	11	2	
ORAX	rpa	(A) ← (A) ∨ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	1	A_2	A_1	A_0	11	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
8-Bit Arithmetic (Memory) (cont)																					
XRAX	rpa	(A) ← (A) ∀ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	0	A_2	A_1	A_0	11	2	
GTAX	rpa	(A) – ((rpa)) – 1	0	1	1	1	0	0	0	0	1	0	1	0	1	A_2	A_1	A_0	11	2	No borrow
LTAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	1	A_2	A_1	A_0	11	2	Borrow
NEAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	1	A_2	A_1	A_0	11	2	No zero
EQAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	1	1	A_2	A_1	A_0	11	2	Zero
ONAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	1	A_2	A_1	A_0	11	2	No zero
OFFAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	1	1	A_2	A_1	A_0	11	2	Zero
Immediate Data																					
ADI	*A,byte	(A) ← (A) + byte	0	1	0	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	1	0	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2, byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	1	0	0	0	S_2	S_1	S_0	20	3	
			Data																		
ACI	*A,byte	(A) ← (A) + byte + (CY)	0	1	0	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte + (CY)	0	1	1	1	0	1	0	0	0	1	0	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte + (CY)	0	1	1	0	0	1	0	0	S_3	1	0	1	0	S_2	S_1	S_0	20	3	
			Data																		
ADINC	*A,byte	(A) ← (A) + byte	0	0	1	0	0	1	1	0	Data								7	2	No carry
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	0	1	0	0	R_2	R_1	R_0	11	3	No carry
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	0	1	0	0	S_2	S_1	S_0	20	3	No carry
			Data																		
SUI	*A,byte	(A) ← (A) – byte	0	1	1	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte	0	1	1	1	0	1	0	0	0	1	1	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte	0	1	1	0	0	1	0	0	S_3	1	1	0	0	S_2	S_1	S_0	20	3	
			Data																		
SBI	*A,byte	(A) ← (A) – byte – (CY)	0	1	1	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte – (CY)	0	1	1	1	0	1	0	0	0	1	1	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte – (CY)	0	1	1	0	0	1	0	0	S_3	1	1	1	0	S_2	S_1	S_0	20	3	
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
Immediate Data (cont)																					
SUINB	*A,byte	(A) ← (A) − byte	0	0	1	1	0	1	1	0					Data				7	2	No borrow
	r,byte	(r) ← (r) − byte	0	1	1	1	0	1	0	0	0	0	1	1	0	R_2	R_1	R_0	11	3	No borrow
							Data														
	sr2,byte	(sr2) ← (sr2) − byte	0	1	1	0	0	1	0	0	S_3	0	1	1	0	S_2	S_1	S_0	20	3	No borrow
							Data														
ANI	*A,byte	(A) ← (A) ∧ byte	0	0	0	0	0	1	1	1					Data				7	2	
	r,byte	(r) ← (r) ∧ byte	0	1	1	1	0	1	0	0	0	0	0	0	1	R_2	R_1	R_0	11	3	
							Data														
	sr2,byte	(sr2) ← (sr2) ∧ byte	0	1	1	0	0	1	0	0	S_3	0	0	0	1	S_2	S_1	S_0	20	3	
							Data														
ORI	*A,byte	(A) ← (A) ∨ byte	0	0	0	1	0	1	1	1					Data				7	2	
	r,byte	(r) ← (r) ∨ byte	0	1	1	1	0	1	0	0	0	0	0	1	1	R_2	R_1	R_0	11	3	
							Data														
	sr2,byte	(sr2) ← (sr2) ∨ byte	0	1	1	0	0	1	0	0	S_3	0	0	1	1	S_2	S_1	S_0	20	3	
							Data														
XRI	*A,byte	(A) ← (A) ∀ byte	0	0	0	1	0	1	1	0					Data				7	2	
	r,byte	(r) ← (r) ∀ byte	0	1	1	1	0	1	0	0	0	0	0	1	0	R_2	R_1	R_0	11	3	
							Data														
	sr2,byte	(sr2) ← (sr2) ∨ byte	0	1	1	0	0	1	0	0	S_3	0	0	1	0	S_2	S_1	S_0	20	3	
							Data														
GTI	*A,byte	(A) − byte − 1	0	0	1	0	0	1	1	1					Data				7	2	No borrow
	r,byte	(r) − byte − 1	0	1	1	1	0	1	0	0	0	0	1	0	1	R_2	R_1	R_0	11	3	No borrow
							Data														
	sr2,byte	(sr2) − byte − 1	0	1	1	0	0	1	0	0	S_3	0	1	0	1	S_2	S_1	S_0	14	3	No borrow
							Data														
LTI	*A,byte	(A) − byte	0	0	1	1	0	1	1	1					Data				7	2	Borrow
	r,byte	(r) − byte	0	1	1	1	0	1	0	0	0	0	1	1	1	R_2	R_1	R_0	11	3	Borrow
							Data														
	sr2,byte	(sr2) − byte	0	1	1	0	0	1	0	0	S_3	0	1	1	1	S_2	S_1	S_0	14	3	Borrow
							Data														
NEI	*A,byte	(A) − byte	0	1	1	0	0	1	1	1					Data				7	2	No zero
	r,byte	(r) − byte	0	1	1	1	0	1	0	0	0	1	1	0	1	R_2	R_1	R_0	11	3	No zero
							Data														

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3 7 6 5 4 3 2 1 0	Operation Code B2 / B4 7 6 5 4 3 2 1 0	State(1)	Bytes	Skip Condition
Immediate Data (cont)							
NEI	sr2,byte	(sr2) – byte	0 1 1 0 0 1 0 0 Data	S_3 1 1 0 1 S_2 S_1 S_0	14	3	No zero
EQI	*A,byte	(A) – byte	0 1 1 1 0 1 1 1 Data		7	2	Zero
	r,byte	(r) – byte	0 1 1 1 0 1 0 0 Data	0 1 1 1 1 R_2 R_1 R_0	11	3	Zero
	sr2,byte	(sr2) – byte	0 1 1 0 0 1 0 0 Data	S_3 1 1 1 1 S_2 S_1 S_0	14	3	Zero
ONI	*A,byte	(A) ∧ byte	0 1 0 0 0 1 1 1 Data		7	2	No zero
	r,byte	(r) ∧ byte	0 1 1 1 0 1 0 0 Data	0 1 0 0 1 R_2 R_1 R_0	11	3	No zero
	sr2,byte	(sr2) ∧ byte	0 1 1 0 0 1 0 0 Data	S_3 1 0 0 1 S_2 S_1 S_0	14	3	No zero
OFFI	*A,byte	(A) ∧ byte	0 1 0 1 0 1 1 1 Data		7	2	Zero
	r,byte	(r) ∧ byte	0 1 1 1 0 1 0 0 Data	0 1 0 1 1 R_2 R_1 R_0	11	3	Zero
	sr2,byte	(sr2) ∧ byte	0 1 1 0 0 1 0 0 Data	S_3 1 0 1 1 S_2 S_1 S_0	14	3	Zero
Working Register							
ADDW	wa	(A) ← (A) + ((V)•(wa))	0 1 1 1 0 1 0 0 Offset	1 1 0 0 0 0 0 0	14	3	
ADCW	wa	(A) ← (A) + ((V)•(wa)) + (CY)	0 1 1 1 0 1 0 0 Offset	1 1 0 1 0 0 0 0	14	3	
ADDNCW	wa	(A) ← (A) + ((V)•(wa))	0 1 1 1 0 1 0 0 Offset	1 0 1 0 0 0 0 0	14	3	No carry
SUBW	wa	(A) ← (A) – ((V)•(wa))	0 1 1 1 0 1 0 0 Offset	1 1 1 0 0 0 0 0	14	3	
SBBW	wa	(A) ← (A) – ((V)•(wa)) – (CY)	0 1 1 1 0 1 0 0 Offset	1 1 1 1 0 0 0 0	14	3	
SUBNBW	wa	(A) ← (A) – ((V)•(wa))	0 1 1 1 0 1 0 0 Offset	1 0 1 1 0 0 0 0	14	3	No borrow
ANAW	wa	(A) ← (A) ∧ ((V)•(wa))	0 1 1 1 0 1 0 0 Offset	1 0 0 0 1 0 0 0	14	3	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3 7	6	5	4	3	2	1	0	Operation Code B2 / B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Working Register (cont)																					
ORAW	wa	(A) ← (A) V ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0	14	3	
			Offset																		
XRAW	wa	(A) ← (A) ⊻ ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0	14	3	
			Offset																		
GTAW	wa	(A) – ((V)•(wa)) – 1	0	1	1	1	0	1	0	0	1	0	1	0	1	0	0	0	14	3	No borrow
			Offset																		
LTAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	1	1	0	0	0	14	3	Borrow
			Offset																		
NEAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	0	1	0	0	0	14	3	No zero
			Offset																		
EQAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	1	1	0	0	0	14	3	Zero
			Offset																		
ONAW	wa	(A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	0	1	0	0	0	14	3	No zero
			Offset																		
OFFAW	wa	(A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	1	0	0	0	0	14	3	Zero
			Offset																		
ANIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) ∧ byte	0	0	0	0	0	1	0	1	Offset								19	3	
			Data																		
ORIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) V byte	0	0	0	1	0	1	0	1	Offset								19	3	
			Data																		
GTIW	*wa,byte	((V)•(wa)) – byte – 1	0	0	1	0	0	1	0	1	Offset								13	3	No borrow
			Data																		
LTIW	*wa,byte	((V)•(wa)) – byte	0	0	1	1	0	1	0	1	Offset								13	3	Borrow
			Data																		
NEIW	*wa,byte	((V)•(wa)) – byte	0	1	1	0	0	1	0	1	Offset								13	3	No zero
			Data																		
EQIW	*wa,byte	((V)•(wa)) – byte	0	1	1	1	0	1	0	1	Offset								13	3	Zero
			Data																		
ONIW	*wa,byte	((V)•(wa)) ∧ byte	0	1	0	0	0	1	0	1	Offset								13	3	No zero
			Data																		
OFFIW	*wa,byte	((V)•(wa)) ∧ byte	0	1	0	1	0	1	0	1	Offset								13	3	Zero
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 B3								Operation Code B2 B4								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
16-Bit Arithmetic																					
EADD	EA,r2	(EA) ← (EA) + (r2)	0	1	1	1	0	0	0	0	0	1	0	0	0	0	R_1	R_0	11	2	
DADD	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	0	1	P_1	P_0	11	2	
DADC	EA,rp3	(EA) ← (EA) + (rp3) + (CY)	0	1	1	1	0	1	0	0	1	1	0	1	0	1	P_1	P_0	11	2	
DADDNC	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	0	1	0	0	1	P_1	P_0	11	2	No carry
ESUB	EA,r2	(EA) ← (EA) − (r2)	0	1	1	1	0	0	0	0	0	1	1	0	0	0	R_1	R_0	11	2	
DSUB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	0	1	P_1	P_0	11	2	
DSBB	EA,rp3	(EA) ← (EA) − (rp3) − (CY)	0	1	1	1	0	1	0	0	1	1	1	1	0	1	P_1	P_0	11	2	
DSUBNB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	0	1	P_1	P_0	11	2	No borrow
DAN	EA,rp3	(EA) ← (EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	0	0	0	1	1	P_1	P_0	11	2	
DOR	EA,rp3	(EA) ← (EA) ∨ (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	1	1	P_1	P_0	11	2	
DXR	EA,rp3	(EA) ← (EA) ⊻ (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	0	1	P_1	P_0	11	2	
DGT	EA,rp3	(EA) − (rp3) − 1	0	1	1	1	0	1	0	0	1	0	1	0	1	1	P_1	P_0	11	2	No borrow
DLT	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	1	1	P_1	P_0	11	2	Borrow
DNE	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	1	1	P_1	P_0	11	2	No zero
DEQ	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	1	1	1	P_1	P_0	11	2	Zero
DON	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	1	1	P_1	P_0	11	2	No zero
DOFF	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	1	1	1	P_1	P_0	11	2	Zero
Multiply/Divide																					
MUL	r2	(EA) ← (A) x (r2)	0	1	0	0	1	0	0	0	0	0	1	0	1	1	R_1	R_0	32	2	
DIV	r2	(EA) ← (EA) + (r2), (r2) ← Remainder	0	1	0	0	1	0	0	0	0	0	1	1	1	1	R_1	R_0	59	2	
Increment/Decrement																					
INR	r2	(r2) ← (r2) + 1	0	1	0	0	0	0	R_1	R_0									4	1	Carry
INRW	*wa	((V)•(wa)) ← ((V)•(wa)) + 1	0	0	1	0	0	0	0	0				Offset					16	2	Carry
INX	rp	(rp) ← (rp) + 1	0	0	P_1	P_0	0	0	1	0									7	1	
	EA	(EA) ← (EA) + 1	1	0	1	0	1	0	0	0									7	1	
DCR	r2	(r2) ← (r2) − 1	0	1	0	1	0	0	R_1	R_0									4	1	Borrow
DCRW	*wa	((V)•(wa)) ← ((V)•(wa)) − 1	0	0	1	1	0	0	0	0				Offset					16	2	Borrow
DCX	rp	(rp) ← (rp) − 1	0	0	P_1	P_0	0	0	1	1									7	1	
	EA	(EA) ← (EA) − 1	1	0	1	0	1	0	0	1									7	1	
Others																					
DAA		Decimal Adjust Accumulator	0	1	1	0	0	0	0	1									4	1	
STC		(CY) ← 1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	8	2	
CLC		(CY) ← 0	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	Operation Code B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Others (cont)																					
NEGA		(A) ← $(\overline{A})+1$	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	0	8	2	
Rotate and Shift																					
RLD		Rotate left digit	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	17	2	
RRD		Rotate right digit	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	1	17	2	
RLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow (CY)$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	1	1	0	1	R_1	R_0	8	2	
RLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$,$(r2_7) \leftarrow (CY)$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	1	1	0	0	R_1	R_0	8	2	
SLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$,$(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	1	0	0	1	R_1	R_0	8	2	
SLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$,$(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	1	0	0	0	R_1	R_0	8	2	
SLLC	r2	$(r2_{m+1}) \leftarrow (r2_m)$,$(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	0	0	0	1	R_1	R_0	8	2	Carry
SLRC	r2	$(r2_{m-1}) \leftarrow (r2_m)$,$(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	R_1	R_0	8	2	Carry
DRLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$,$(EA_0) \leftarrow (CY)$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	1	0	1	1	0	1	0	0	8	2	
DRLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$,$(EA_{15}) \leftarrow (CY)$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	1	0	1	1	0	0	0	0	8	2	
DSLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$,$(EA_0) \leftarrow 0$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	8	2	
DSLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$,$(EA_{15}) \leftarrow 0$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	8	2	
Jump																					
JMP	*word	(PC) ← word	0	1	0	1	0	1	0	0	Low addr								10	3	
			High addr																		
JB		$(PC_H) \leftarrow (B)$,$(PC_L) \leftarrow (C)$	0	0	1	0	0	0	0	1									4	1	
JR	word	(PC) ← (PC) + 1 + jdisp 1	1	1	←		jdisp1			→									10	1	
JRE	*word	(PC) ← (PC) + 2 + jdisp	0	1	0	0	1	1	1	←	jdisp							→	10	2	
JEA		(PC) ← (EA)	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	0	8	2	
Call																					
CALL	*word	$((SP)-1) \leftarrow ((PC)+3)_H$, $((SP)-2) \leftarrow ((PC)+3)_L$, (PC) ← word, (SP) ← (SP) − 2	0	1	0	0	0	0	0	0	Low addr								16	3	
			High addr																		
CALB		$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_H) \leftarrow (B)$, $(PC_L) \leftarrow (C)$, (SP) ← (SP) − 2	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	1	17	2	
CALF	*word	$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_{15\text{-}11}) \leftarrow 00001$, $(PC_{10\text{-}0}) \leftarrow$ fa, (SP) ← (SP) − 2	0	1	1	1	1	←			fa							→	13	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
			B1			B3					B2			B4							
Call (cont)																					
CALT	word	$((SP)-1) \leftarrow ((PC)+1)_H$, $((SP)-2) \leftarrow ((PC)+1)_L$, $(PC_L) \leftarrow (128+2ta)$, $(PC_H) \leftarrow (129+2ta)$, $(SP) \leftarrow (SP)-2$	1	0	0	←		ta		→									16	1	
SOFTI		$((SP)-1) \leftarrow (PSW)$, $((SP)-2) \leftarrow ((PC)+1)_H$, $((SP)-3) \leftarrow ((PC)+1)_L$, $(PC) \leftarrow 0060H$, $(SP) \leftarrow (SP)-3$	0	1	1	1	0	0	1	0									16	1	
Return																					
RET		$(PC_L) \leftarrow ((SP))$, $(PC_H) \leftarrow ((SP)+1)$ $(SP) \leftarrow (SP)+2$	1	0	1	1	1	0	0	0									10	1	
RETS		$(PC_L) \leftarrow ((SP))$, $(PC_H) \leftarrow ((SP)+1)$ $(SP) \leftarrow (SP)+2$, $(PC) \leftarrow (PC)+n$	1	0	1	1	1	0	0	1									10	1	Unconditional Skip
RETI		$(PC_L) \leftarrow ((SP))$, $(PC_H) \leftarrow ((SP)+1)$ $(PSW) \leftarrow ((SP)+2)$, $(SP) \leftarrow (SP)+3$	0	1	1	0	0	0	1	0									13	1	
Skip																					
Bit		bit, wa	0	1	0	1	1	B_2	B_1	B_0	Offset								10	2	Bit Test
CPU Control																					
SK	f	Skip if f = 1	0	1	0	0	1	0	0	0	0	0	0	0	1	F_2	F_1	F_0	8	2	f = 1
SKN	f	Skip if f = 0	0	1	0	0	1	0	0	0	0	0	0	1	1	F_2	F_1	F_0	8	2	f = 0
SKIT	irf	Skip if irf = 1, then reset irf	0	1	0	0	1	0	0	0	0	1	0	I_4	I_3	I_2	I_1	I_0	8	2	irf = 1
SKNIT	irf	Skip if irf = 0 Reset irf if irf = 1	0	1	0	0	1	0	0	0	0	1	1	I_4	I_3	I_2	I_1	I_0	8	2	irf = 0
NOP		No operation	0	0	0	0	0	0	0	0									4	1	
EI		Enable interrupt	1	0	1	0	1	0	1	0									4	1	
DI		Disable interrupt	1	0	1	1	1	0	1	0									4	1	
HLT		Halt	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	1	11	2	

Notes:

(1) In the case of skip condition, the idle states are as follows:
- 1-byte instruction: 4 states
- 2-byte instruction: 8 states
- 3-byte instruction: 11 states
- 2-byte instruction (with *): 7 states
- 3-byte instruction (with *): 10 states
- 4-byte instruction: 14 states

(2) B2 (Data): rpa2 = D + byte, H + byte.

(3) Right side of slash (/) in states indicates case rpa2, rpa3 = D + byte, H + A, H + B, H + EA, H + byte.

(4) B3 (Data): rpa3 = D + byte, H + byte

NEC

μPD78C10/C11/C14 8-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS WITH A/D CONVERTER

Description

The μPD78C10, μPD78C11, and μPD78C14 single-chip microcomputers integrate sophisticated on-chip peripheral functionality normally provided by external components. The devices' internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make them appropriate in data processing as well as control applications. The devices integrate a 16-bit ALU, 4K-byte ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs on a single die, allowing their use in fast, high end processing applications. This involves analog signal interface and processing.

The μPD78C11 is a 4K-byte mask ROM high-volume production device embedded with custom customer program. The μPD78C14 is a 16K-byte mask ROM device. The μPD78C10 is a ROM-less version for prototyping and small volume production.

Features

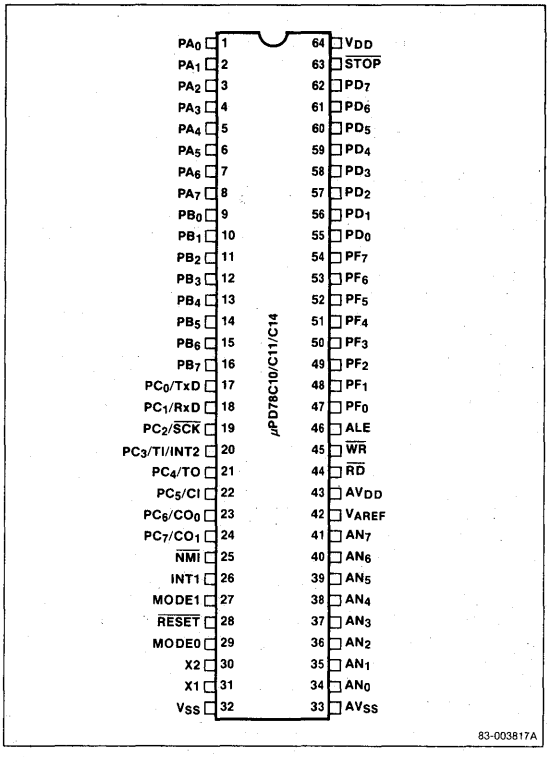
- ☐ CMOS technology
  - — 2.5 to 6.0 V operating range
  - — 30 mA operating current
- ☐ Complete single-chip microcomputer
  - — 16-bit ALU
  - — 4K x 8 ROM (78C11)
  - — 16K x 8 ROM (78C14)
  - — 256-byte RAM
- ☐ 44 I/O lines
- ☐ Two zero-cross detect inputs
- ☐ Two 8-bit timers
- ☐ Expansion capabilities
  - — 8085A bus-compatible
  - — 60K-byte external memory address range
- ☐ 8-channel, 8-bit A/D converter
  - — Autoscan mode
  - — Channel select mode
- ☐ Full duplex USART
  - — Synchronous and asynchronous
- ☐ 154 instructions
  - — 16-bit arithmetic, multiply and divide
  - — HALT and STOP instructions
- ☐ 1 μs instruction cycle time (12 MHz operation)
- ☐ Prioritized interrupt structure
  - — 3 external
  - — 8 internal
- ☐ Standby function
- ☐ On-chip clock generator
- ☐ 64-pin plastic QUIP, shrink DIP, or flatpack

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD78C10G-36 μPD78C11G-36 μPD78C14G-36	64-pin plastic QUIP	12 MHz
μPD78C10CW μPD78C11CW μPD78C14CW	64-pin plastic shrink DIP	12 MHz
μPD78C10G-1B μPD78C11G-1B μPD78C14G-1B	64-pin plastic miniflat	12 MHz
μPD78C10L μPD78C11L μPD78C14L	68-pin PLCC (available 3Q86)	12 MHz

Pin Configurations

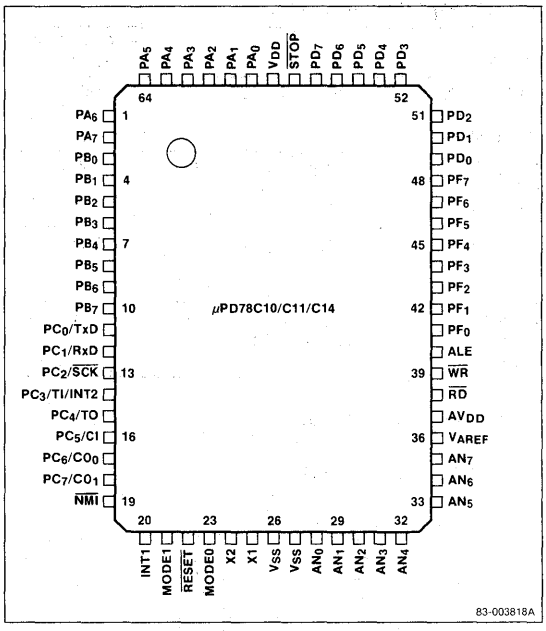
64-Pin QUIP or Shrink DIP



4

Pin Configurations (cont)

64-Pin Miniflat



Pin Identification

Symbol	Function
PA_0-PA_7	Port A I/O
PB_0-PB_7	Port B I/O
PC_0/TxD	Port C I/O line 0/Transmit data output
PC_1/RxD	Port C I/O line 1/Receive data input
PC_2/$\overline{SCK}$	Port C I/O line 2/Serial clock I/O
PC_3/TI/INT2	Port C I/O line 3/Timer input/Interrupt request 2 input
PC_4/TO	Port C I/O line 4/Timer output
PC_5/CI	Port C I/O line 5/Counter input
PC_6, PC_7/CO_0, CO_1	Port C I/O lines 6, 7/Counter outputs 0, 1
$\overline{NMI}$	Nonmaskable interrupt input
INT1	Interrupt request 1 input
MODE1	Mode 1 input/Memory cycle 1 output
$\overline{RESET}$	Reset input
MODE0	Mode 0 input/I/O/Memory output
X1, X2	Crystal connections 1, 2

Pin Identification (cont)

Symbol	Function
V_{SS}	Ground
AV_{SS}	A/D converter power supply ground
AN_0-AN_7	A/D converter analog inputs 0-7
V_{AREF}	A/D converter reference voltage
AV_{DD}	A/D converter power supply voltage
$\overline{RD}$	Read strobe output
$\overline{WR}$	Write strobe output
ALE	Address latch enable output
PF_0-PF_7	Port F I/O/Expansion memory address bus (bits 8-15)
PD_0-PD_7	Port D I/O/Expansion memory address/data bus
$\overline{STOP}$	Stop mode control input
V_{DD}	5 V power supply

Pin Functions

PA_0-PA_7 [Port A]

Port A is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port A inputs.

PB_0-PB_7 [Port B]

Port B is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port B inputs.

PC_0-PC_7 [Port C]

Port C is an 8-bit three-state port. Each bit is independently programmable as either input or output. Alternatively, the lines of port C can be used as control lines for the USART and timer. Reset puts all lines of port C in port mode, input.

TxD [Transmit Data]. Serial data output terminal.

RxD [Receive Data]. Serial data input terminal.

$\overline{SCK}$ [Serial Clock]. Output for the serial clock when internal clock is used. Input for serial clock when external clock is used.

TI [Timer Input]. Timer input terminal.

$\overline{INT2}$ [Interrupt Request 2]. Falling-edge-triggered, maskable interrupt input terminal and AC-input, zero-cross detection terminal.

TO [Timer Output]. The output of TO is a square wave with a frequency determined by the timer/counter.

CI [Counter Input]. External pulse input to timer/event counter.

CO_0, CO_1 [Counter Outputs 0, 1]. Programmable rectangular wave outputs based on timer/event counter.

PD_0-PD_7 [Port D]

Port D is an 8-bit three-state port. It can be programmed as either 8 bits of input or 8 bits of output. When external expansion memory is used, port D acts as the multiplexed address/data bus.

PF_0-PF_7 [Port F]

Port F is an 8-bit three-state port. Each bit is independently programmable as an input or output. When external expansion memory is used, port F outputs the high-order address bits.

AN_0-AN_7

These are the eight analog inputs to the A/D converter. AN_4-AN_7 can also be used as a digital input for falling edge detection.

AV_{SS} [A/D Converter Power Ground]

AV_{SS} is the ground potential for the A/D converter power supply.

$\overline{NMI}$ [Nonmaskable Interrupt]

Falling-edge-triggered nonmaskable interrupt input.

INT1 [Interrupt Request 1]

INT1 is a rising-edge-triggered, maskable interrupt input. It is also an AC-input, zero-cross detection terminal.

$\overline{RESET}$ [Reset]

When the $\overline{RESET}$ input is brought low, it initializes the device.

MODE1, MODE0 [Mode 1, 0]

The MODE1 and MODE0 inputs select the memory expansion mode. MODE1 also outputs the M1 signal during each opcode fetch. MODE0 outputs the $\overline{IO}$/M signal.

V_{AREF} [A/D Converter Reference]

V_{AREF} sets the upper limit for the A/D conversion range.

AV_{DD} [A/D Converter Power]

This is the power supply voltage for the A/D converter.

$\overline{RD}$ [Read Strobe]

The $\overline{RD}$ output goes low to gate data from external devices onto the data bus. $\overline{RD}$ goes high during reset. Three-state.

$\overline{WR}$ [Write Strobe]

The $\overline{WR}$ output goes low to indicate that the data bus holds valid data. It is a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during reset. Three-state.

ALE [Address Latch Enable]

The ALE output latches the address signal to the output of PD_0-PD_7.

X1, X2 [Crystal Connections 1, 2]

X1 and X2 are the system clock crystal oscillator terminals. X1 is the input for an external clock.

V_{SS} [Ground]

Ground potential.

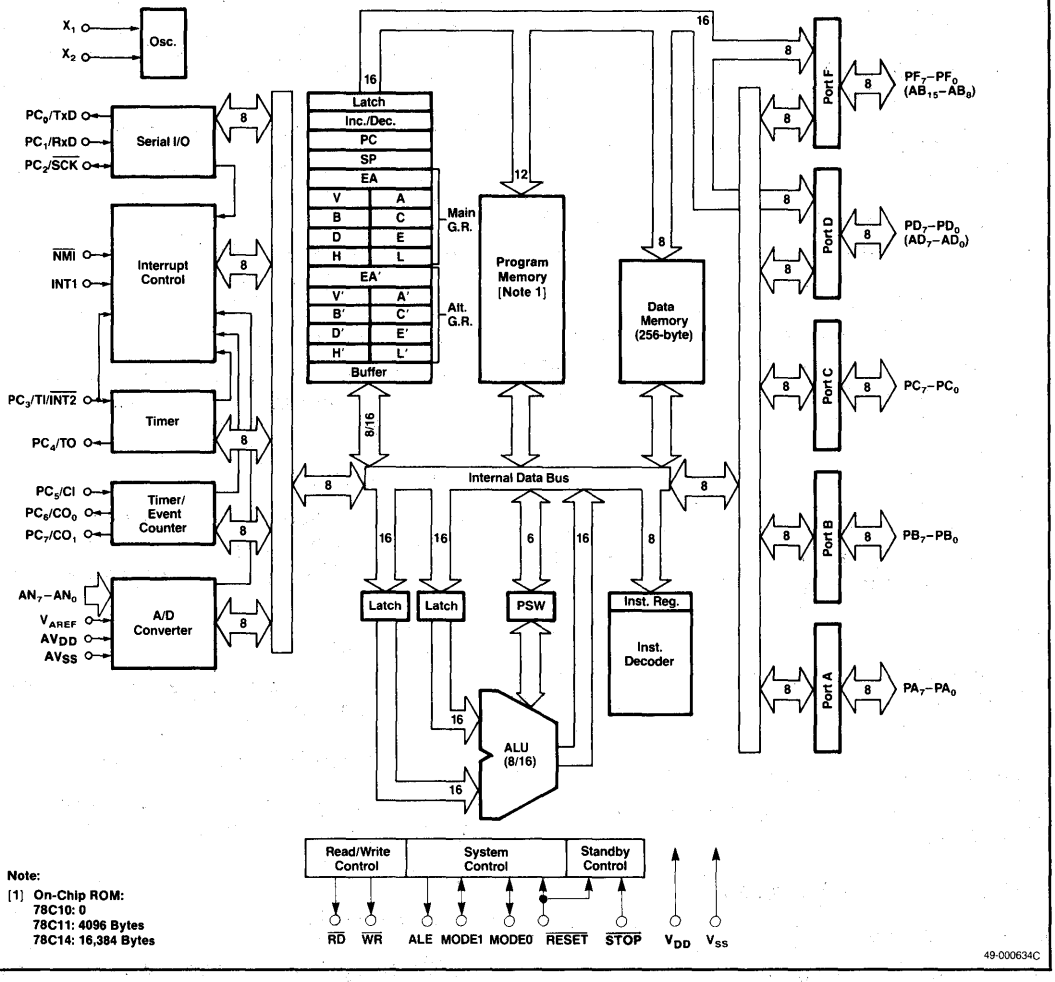
$\overline{STOP}$ [Stop Mode Control Input]

A low-level input on $\overline{STOP}$ stops the system clock oscillator.

V_{DD} [Power Supply]

+5 V power supply.

Block Diagram



Note:
[1] On-Chip ROM:
78C10: 0
78C11: 4096 Bytes
78C14: 16,384 Bytes

Functional Description

Memory Map

The μPD78C11 can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65,280-65,335), any memory location can be used as ROM or RAM. The memory map, figure 1, defines the 0 to 64K byte memory space for the μPD78C11. On-chip ROM is located from 0-16,383 in the μPD78C14.

Input/Output

The μPD78C10/C11/C14 has 8 analog input lines (AN_0-AN_7), 44 digital I/O lines, five 8-bit ports (port A, port B, port C, port D, port F), and 4 input lines (AN_4-AN_7).

Analog Input Lines. AN_0-AN_7 are configured as analog input lines for on-chip A/D converter.

Port A, Port B, Port C, Port F. Each line of these ports can be individually programmed as an input or output. When used as I/O ports, all have latched outputs and high-impedance inputs.

Port D. Port D can be programmed as a byte input or a byte output.

AN_4-AN_7. The high-order analog input lines, AN_4-AN_7, can be used as digital input lines for falling-edge detection.

Control Lines. Under software control, each line of port C can be configured individually to provide control lines for the serial interface, timer, and timer/counter.

Memory Expansion. In addition to the single-chip operation mode, the μPD78C11 has four memory expansion modes. Under software control, port D can provide a multiplexed low-order address and data bus; port F can provide a high-order address bus. Table 1 shows the relation between memory expansion modes and the pin configurations of port D and port F.

Table 1. Memory Expansion Modes and Port Configurations

Memory Expansion	Port Configuration	
None	Port D	I/O port
	Port F	I/O port
256 Bytes	Port D	Multiplexed address/data bus
	Port F	I/O port
4K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_3	Address bus
	Port F_4-F_7	I/O port
16K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_5	Address bus
	Port F_6-F_7	I/O port
60K Bytes	Port D	Multiplexed address/data bus
	Port F	Address bus

Timers

There are two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be software set to increment at intervals of four machine cycles (1 μs at 12 MHz operation) or 128 machine cycles (32 μs at 12 MHz), or to increment on receipt of a pulse at TI. Figure 2 is the block diagram for the timer.

Timer/Event Counter

The 16-bit multifunctional timer/event counter (figure 3) can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output

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Figure 1. Memory Map

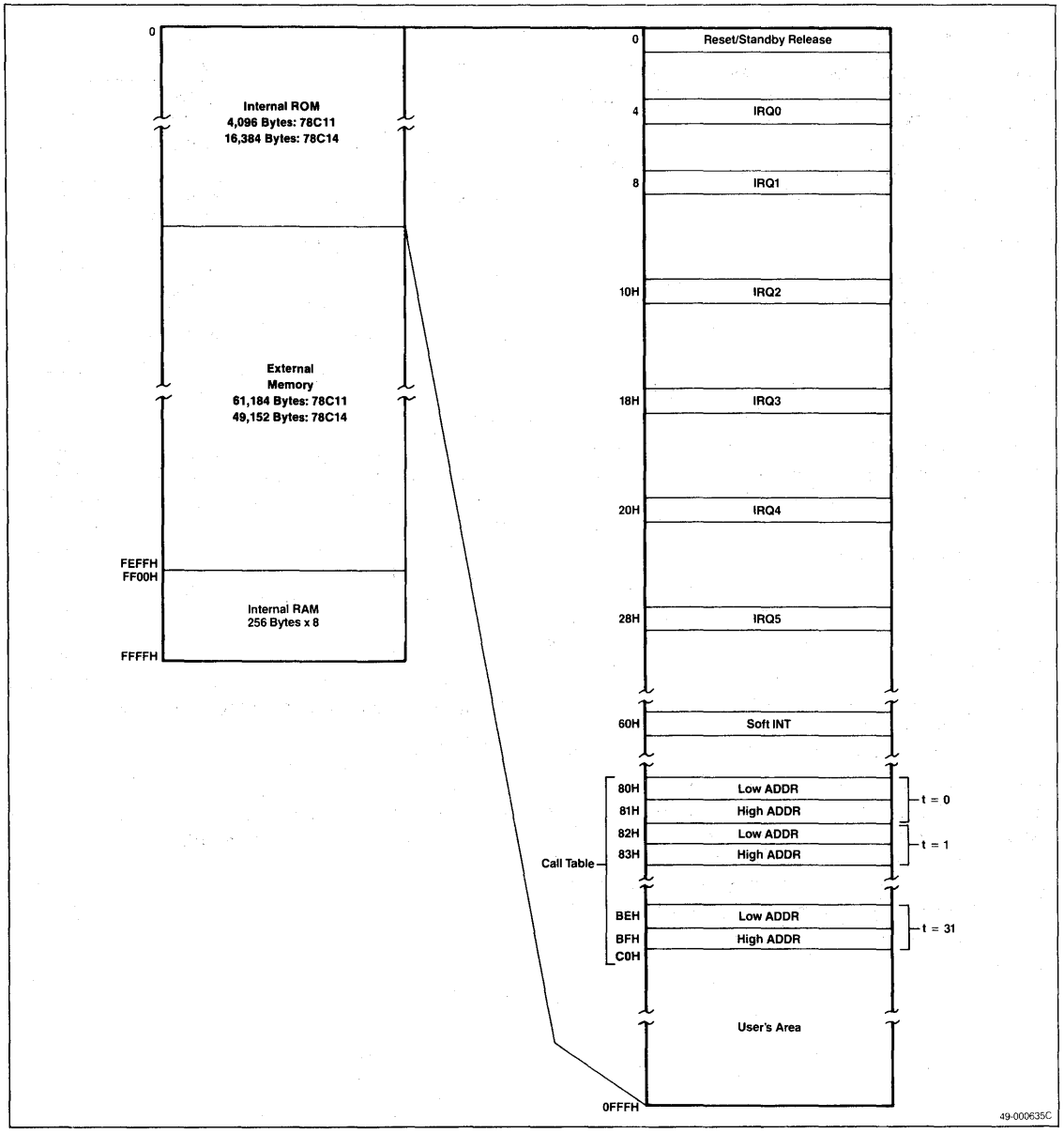
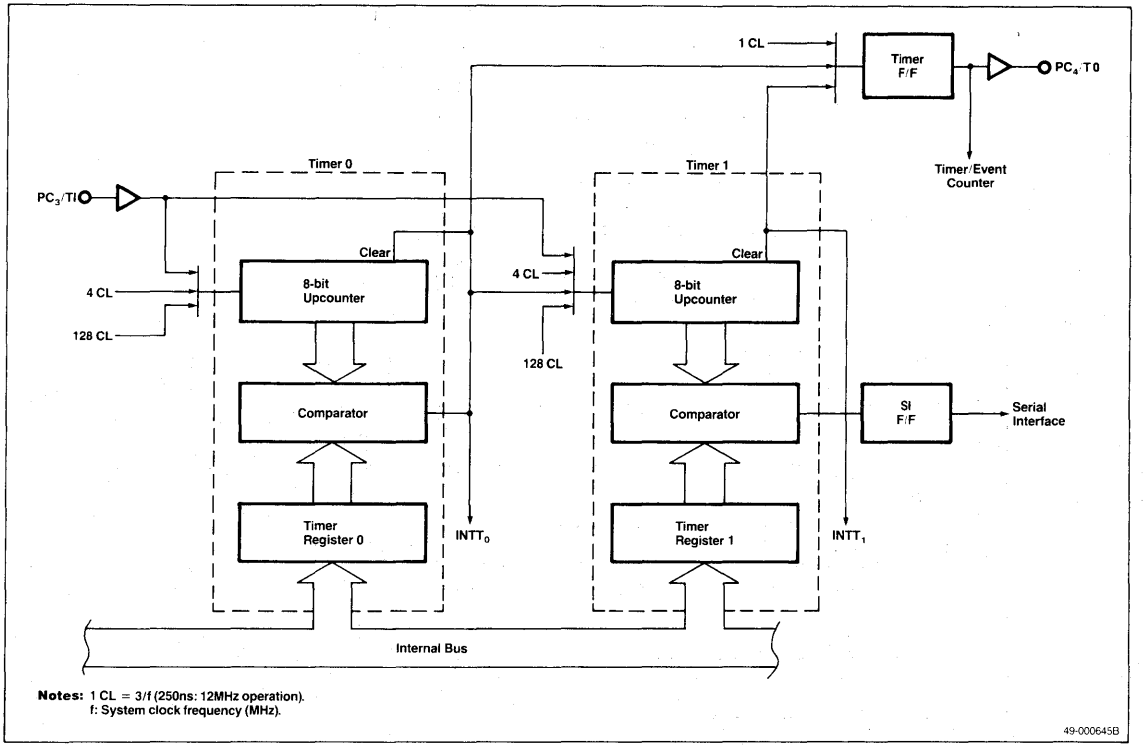


Figure 2. Timer Block Diagram



Notes: 1 CL = 3/f (250ns: 12MHz operation).
f: System clock frequency (MHz).

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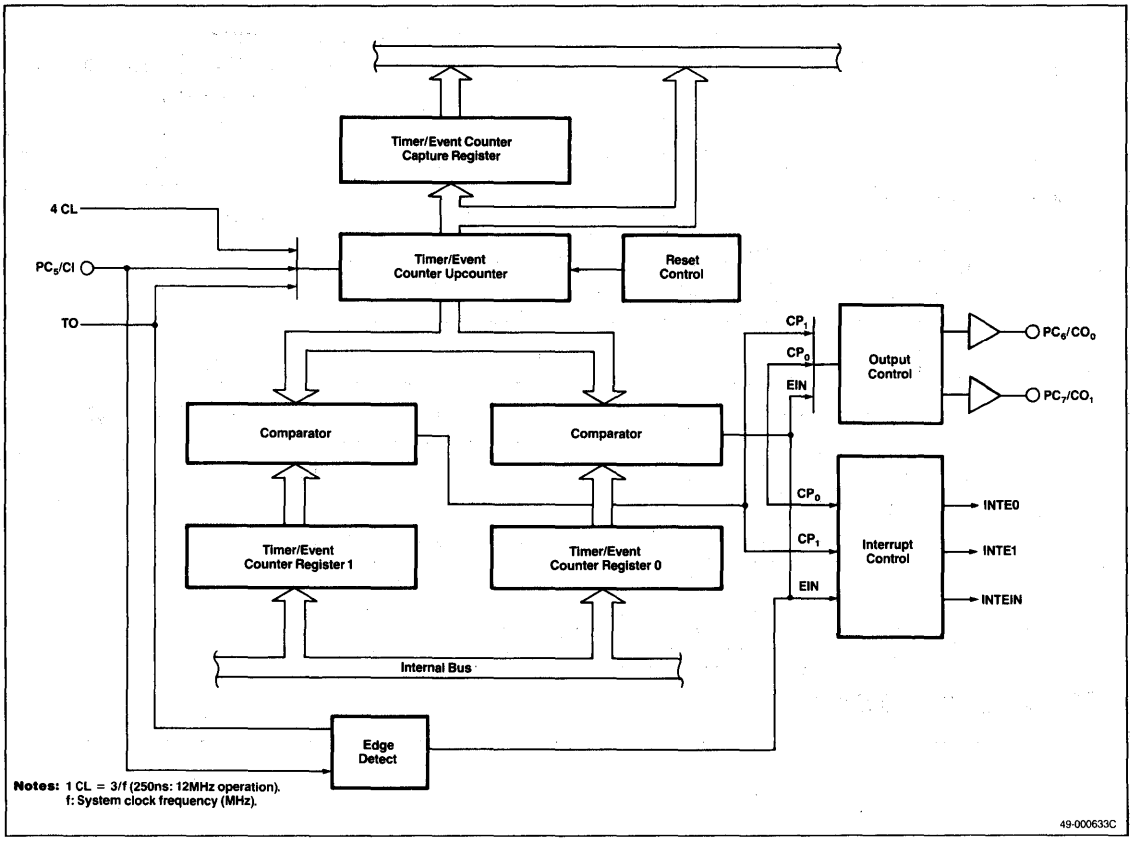
Figure 3. Block Diagram for Timer/Event Counter



8-Bit A/D Converter

- 8 input channels
- 4 conversion result registers
- 2 powerful operation modes
  - — Autoscan mode
  - — Channel select mode
- Successive approximation technique
- Absolute accuracy: 0.6% ±1/2 LSB
- Conversion range: 0 to 5 V
- Conversion time: 42 μs
- Interrupt generation

Analog/Digital Converter

The μPD78C10/C11/C14 features an 8-bit, high-speed, high-accuracy A/D converter. The A/D converter is made up of a 256-resistor ladder and a successive approximation register (SAR). There are four conversion result registers (CR_0-CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0-CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers. Figure 4 shows the block diagram for the A/D converter. To prevent operation of the A/D converter and thus reduce power consumption, set $V_{AREF} = 0$ V.

Interrupt Structure

There are 11 interrupt sources. Three are external interrupts and eight are internal. Table 2 shows 11 interrupt sources divided into six priority levels. See figure 5.

Standby Function

The μPD78C10/C11/C14 has two standby modes: HALT and STOP. The HALT mode reduces power consumption to less than 50% of normal operating requirements, while maintaining the contents of on-chip registers, RAM, and control status. The system clock and on-board peripherals continue to operate, but the CPU stops executing instructions. The HALT mode is initiated by executing the HLT instruction. The HALT mode can be released by any nonmasked interrupt or by $\overline{\text{RESET}}$.

The STOP mode reduces power consumption to less than 0.1% of normal operating requirements. There are two STOP modes: type A and type B.

Type A is initiated by executing a STOP instruction. If V_{CC} is maintained within the operating range (2.5 to 6.0 V), on-board RAM and CPU register contents are saved. If V_{CC} is held above 2.0 V (but less than 2.5 V), only on-board RAM is saved. The oscillator is stopped. The STOP mode can be released by an input on $\overline{\text{NMI}}$ or $\overline{\text{RESET}}$. The user can program oscillator stabilization time via timer 1. By checking the standby flag (SB), the user can determine whether the processor has been in the standby mode.

Table 2. Interrupt Sources

Interrupt Request	Interrupt Address	Type of Interrupt	Internal/ External
IRQ0	4	$\overline{\text{NMI}}$ (Nonmaskable interrupt)	Ext
IRQ1	8	INTT0 (Coincidence signal from timer 0)	Int
		INTT1 (Coincidence signal from timer 1)	
IRQ2	16	INT1 (Maskable interrupt)	Ext
		$\overline{\text{INT2}}$ (Maskable interrupt)	
IRQ3	24	INTE0 (Coincidence signal from timer/event counter)	Int
		INTE1 (Coincidence signal from timer/event counter)	
IRQ4	32	INTEIN (Falling signal of CI and TO counter)	Int/Ext
		INTAD (A/D converter interrupt)	
IRQ5	40	INTSR (Serial receive interrupt)	Int
		INST (Serial send interrupt)	

Type B is initiated by inputting a low level on the STOP input. Only RAM contents are saved, not the CPU register contents. The oscillator is stopped. The STOP mode is released by raising STOP to a high level. The oscillator stabilization time is fixed at 65 ms; 65 ms after STOP is raised, instruction execution will begin at location 0. You can increase the stabilization time by holding RESET low for the required time period.

Figure 4. A/D Converter Block Diagram

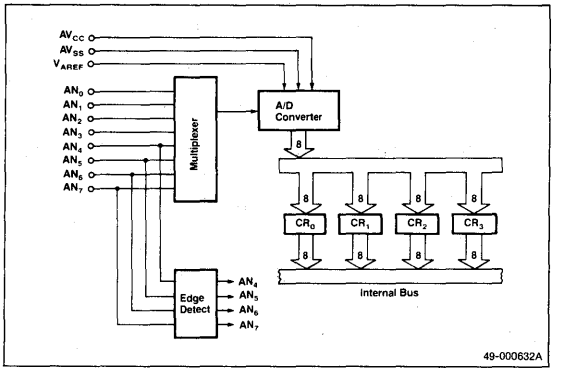
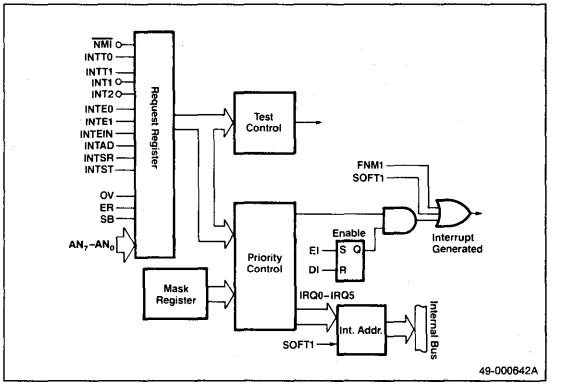


Figure 5. Interrupt Structure Block Diagram



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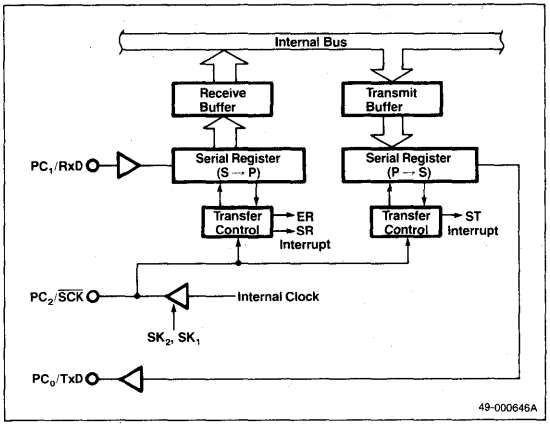
Universal Serial Interface

The serial interface can operate in one of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first, for easy interfacing to certain NEC peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception: search and nonsearch. In the search mode, data is transferred one bit at a time from the serial register to the receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from the serial register to the transmit buffer occurs eight bits at a time. Figure 6 shows the universal serial interface block diagram.

Figure 6. Universal Serial Interface Block Diagram



Zero-Crossing Detector

The INT1 and $\overline{INT2}$ terminals (used common to TI and PC_3) can detect the zero-crossing point of low-frequency AC signals. When driven directly, these pins respond as a normal digital input. Figure 7 shows the zero-crossing detection circuitry.

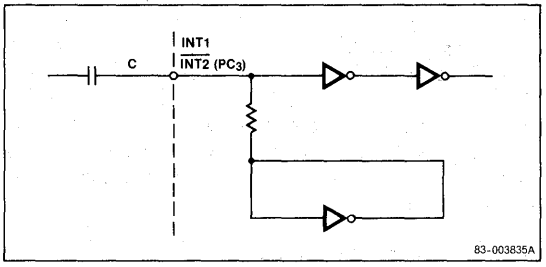
The zero-crossing detection capability allows you to make the 50-60 Hz power signal the basis for system timing and to control voltage phase-sensitive devices.

To use the zero-cross detection mode, an AC signal of approximately 1-3 V AC (peak-to-peak) and a maximum frequency of 1 kHz is coupled through an external capacitor to the INT1 and $\overline{INT2}$ pins.

For the INT1 pin, the internal digital state is sensed as a 0 until the rising edge crosses the average DC level, when it becomes a 1 and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a 1 until the falling edge crosses the average DC level, when it becomes a 0 and $\overline{INT2}$ interrupt is generated.

Figure 7. Zero-Crossing Detection Circuit



Absolute Maximum Ratings

Power supply voltages, V_{DD}		−0.5 V to +7.0 V
	AV_{DD}	AV_{SS} to V_{DD} + 0.5 V
	AV_{SS}	−0.5 V to +0.5 V
Input voltage, V_I		−0.5 V to +7.0 V
Output voltage, V_O		−0.5 V to V_{DD}+ 0.5 V
Output current low, I_{OL}		4.0 mA
Output current low, total for all pins		100 mA
Output current high, I_{OH}		−2.0 mA
Output current high, total for all pins		−50 mA
Reference input voltage, V_{AREF}		−0.5 V to AV_{DD} + 0.3 V
Operating temperature, T_{OPR} $f_{XTAL} \leq 12$ MHz		−40°C to +85°C
Storage temperature, T_{STG}		−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

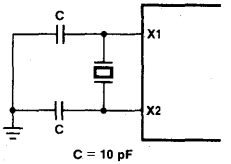
Oscillating Frequency	T_A	V_{DD}, AV_{DD}
$f_{XTAL} \leq 12$ MHz	−40°C to +85°C	+5.0 V ±10%

Capacitance

T_A = 25°C; $V_{DD} = V_{SS} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			10	pF	$Af_C = 1$ MHz. Unmeasured pins returned to 0 V.
Output capacitance	C_O			20	pF	
I/O capacitance	C_{IO}			20	pF	

Recommended XTAL Oscillation Circuit



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DC Characteristics

$T_A = -10°C$ to $+70°C$; $V_{DD} = +5.0\ V \pm 5\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL1}	0		0.8	V	All except Note 1 inputs.
	V_{IL2}	0		0.2 V_{DD}	V	Note 1 inputs.
Input high voltage	V_{IH1}	2.2		V_{DD}	V	All except X1, X2, and Note 1 inputs.
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	X1, X2, and Note 1 inputs.
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 2.0\ mA$
Output high voltage	V_{OH}	$V_{DD} - 1.0$			V	$I_{OH} = -1.0\ mA$
		$V_{DD} - 0.5$			V	$I_{OH} = -100\ \mu A$
Data retention voltage	V_{DDDR}	2.5			V	$\overline{STOP}$ mode
Input current	I_I			±200	μA	INT1, TI(PC_3); $0\ V \le V_I \le V_{DD}$
Input leakage current	I_{LI}			±10	μA	All except INT, TI(PC_3) $0\ V \le V_I \le V_{DD}$
Output leakage current	I_{LO}			±10	μA	$0\ V \le V_O \le V_{DD}$
AV_{DD} supply current	AI_{DD}		0.3	1.0	mA	
V_{DD} supply current	I_{DD1}		15	30	mA	Operation mode f = 12 MHz
	I_{DD2}		10	20	mA	HALT mode f = 12 MHz
Data retention current	I_{DDDR}		1	15	μA	$V_{DDDR} = 2.5\ V$
			10	50	μA	$V_{DDDR} = 5\ V \pm 10\%$

Note:

(1) Inputs $\overline{RESET}$, $\overline{STOP}$, $\overline{NMI}$, $\overline{SCK}$, INT1, TI, and AN_4-AN_7.

Serial Operation

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
$\overline{SCK}$ cycle time	t_{CYK}	1		μs	$\overline{SCK}$ input (1)
		500		ns	(2)
		2		μs	$\overline{SCK}$ output
$\overline{SCK}$ width low	t_{KKL}	420		ns	$\overline{SCK}$ input (1)
		200		ns	$\overline{SCK}$ input (2)
		900		ns	$\overline{SCK}$ output
$\overline{SCK}$ width high	t_{KKH}	420		ns	$\overline{SCK}$ input (1)
		200		ns	$\overline{SCK}$ input (2)
		900		ns	$\overline{SCK}$ output
RxD set-up time to $\overline{SCK}\uparrow$	t_{RXK}	80		ns	(1)
RxD hold time after $\overline{SCK}\uparrow$	t_{KRX}	80		ns	(1)
$\overline{SCK}\downarrow$ TxD delay time	t_{KTX}		210	ns	(1)

Note:

(1) 1x baud rate in asynchronous, synchronous, or I/O interface mode.

(2) 16x baud rate or 64x baud rate in asynchronous mode.

Zero-Cross Characteristics

Parameter	Symbol	Limits Min	Max	Unit	Test Conditions
Zero-cross detection input	V_{ZX}	1	1.8	VAC_{p-p}	Ac coupled 60-Hz sine wave
Zero-cross accuracy	A_{ZX}		±135	mV	
Zero-cross detection input frequency	f_{ZX}	0.05	1	kHz	

AC Characteristics

Read/Write Operation

$T_A = -40°C$ to $+85°C$; $V_{DD} = +5.0\ V \pm 10\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limits $f_{XTAL} = 12$ MHz Min	Limits $f_{XTAL} = 12$ MHz Max	Unit	Test Conditions (1)
$\overline{RESET}$ pulse width	t_{RP}	10		μs	
Interrupt pulse width (INT1, INT2)	t_{IP}	3.0		μs	
$\overline{NMI}$ pulse width		10		μs	
Counter input pulse width	t_{CI}	500		ns	Event counter mode
		4.0		μs	Pulse width measurement mode
Timer input pulse width	t_{TI}	500		ns	
X1 Input cycle time	t_{CYC}	83	250	ns	
Address set-up to ALE ↓	t_{AL}	65		ns	
Address hold after ALE ↓	t_{LA}	50		ns	
Address to $\overline{RD}$ ↓ delay time	t_{AR}	150		ns	
$\overline{RD}$ ↓ to address floating	t_{AFR}		20	ns	
Address to data input	t_{AD}		360	ns	
ALE ↓ to data input	t_{LDR}		215	ns	
$\overline{RD}$ ↓ to data input	t_{RD}		180	ns	
ALE ↓ to $\overline{RD}$ ↓ delay time	t_{LR}	35		ns	
Data hold time to $\overline{RD}$ ↑	t_{RDH}	0		ns	
$\overline{RD}$ ↑ to ALE ↑ delay time	t_{RL}	115		ns	
$\overline{RD}$ width low	t_{RR}	280		ns	Data read
		530		ns	Opcode fetch
ALE width high	t_{LL}	125		ns	
$\overline{M1}$ Setup time to ALE ↓	t_{ML}	65		ns	
$\overline{M1}$ Hold time after ALE ↓	t_{LM}	50		ns	
$\overline{IO}$/M Setup time to ALE ↓	t_{IL}	65		ns	
$\overline{IO}$/M Hold time after ALE ↓	t_{LI}	50		ns	
Address to $\overline{WR}$ ↓ Delay	t_{AW}	150		ns	
ALE ↓ to data output	t_{LDW}		195	ns	
$\overline{WR}$ ↓ to data output	t_{WD}		100	ns	
ALE ↓ to $\overline{WR}$ ↓ delay	t_{LW}	35		ns	
Data set-up time to $\overline{WR}$ ↑	t_{DW}	230		ns	
Data hold time to $\overline{WR}$ ↑	t_{WDH}	95		ns	
$\overline{WR}$ ↑ to ALE ↑ delay time	t_{WL}	115		ns	
$\overline{WR}$ width low	t_{WW}	280		ns	

Note:

(1) Load capacitance: $C_L = 150$ pF.

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A/D Converter Characteristics

$T_A = -40°C$ to $+85°C$; $V_{SS} = AV_{SS} = 0$ V; $AV_{DD} - 0.5$ V $\leq V_{AREF} \leq AV_{DD}$; $V_{DD} - 0.5 \leq AV_{DD}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Resolution		8			Bits	
Absolute accuracy				0.4% ± 1/2	LSB	$T_A = -10°C$ to $+50°C$
				0.6% ± 1/2	LSB	
Conversion time	t_{CONV}	567			t_{CYC}	83 ns $\leq t_{CYC} \leq$ 110 ns
		432			t_{CYC}	110 ns $\leq t_{CYC} \leq$ 170 ns
Sampling time	t_{SAMP}	96			t_{CYC}	83 ns $\leq t_{CYC} \leq$ 110 ns
		72			t_{CYC}	110 ns $\leq t_{CYC} \leq$ 170 ns
Analog input voltage	V_{IA}	0		V_{AREF}	V	
Analog input impedance	R_{AN}		1000		MΩ	
V_{AREF} current	I_{AREF}		1.5	3.0	mA	

Bus Timing Depending on t_{CYC}

Symbol	Calculating Expression	Min/Max
t_{RP}	60T	Min
t_{TI}	6T	Min
t_{CI} (2)	6T	Min
t_{CI} (3)	48T	Min
t_{IP}	36T	Min
t_{AL}	2T − 100	Min
t_{LA}	T − 30	Min
t_{AR}	3T − 100	Min
t_{AD}	7T − 220	Max
t_{LDR}	5T − 200	Max
t_{RD}	4T − 150	Max
t_{LR}	T − 50	Min
t_{RL}	2T − 50	Min
t_{RR}	4T − 50 (Data Read)	Min
	7T − 50 (Opcode Fetch)	
t_{LL}	2T − 40	Min
t_{ML}	2T − 100	Min
t_{LM}	T − 30	Min
t_{IL}	2T − 100	Min
t_{LI}	T − 30	Min
t_{AW}	3T −100	Min
t_{LDW}	T + 110	Max
t_{LW}	T − 50	Min
t_{DW}	4T − 100	Min
t_{WDH}	2T − 70	Min
t_{WL}	2T − 50	Min
t_{WW}	4T − 50	Min
t_{CYK}	12T ($\overline{SCK}$ input) (1)	Min
	24T ($\overline{SCK}$ output)	
t_{KKL}	5T + 5 ($\overline{SCK}$ input) (1)	Min
	12T − 100 ($\overline{SCK}$ output)	
t_{KKH}	5T + 5 ($\overline{SCK}$ input) (1)	Min
	12T − 100 ($\overline{SCK}$ output)	

Note:

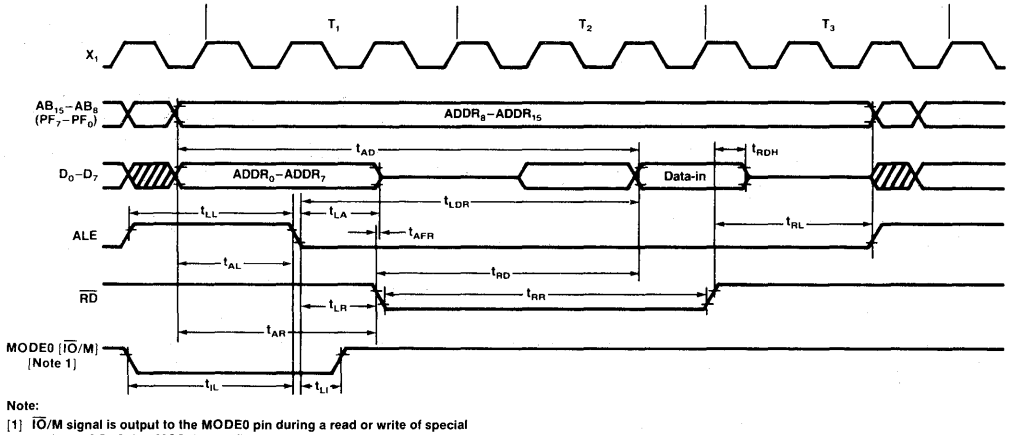
(1) 1x baud rate in asynchronous, synchronous, or I/O interface mode.
$T = t_{CYC} = 1/f_{XTAL}$.
The items not included in this list are independent of oscillator frequency (f_{XTAL}).

(2) Event counter mode.

(3) Pulse width measurement mode.

Timing Waveforms

Read Operation



Note:

[1] IO/M signal is output to the MODE0 pin during a read or write of special register[s] Sr-Sr2, if MODE0 is pulled up to V_{DD}.

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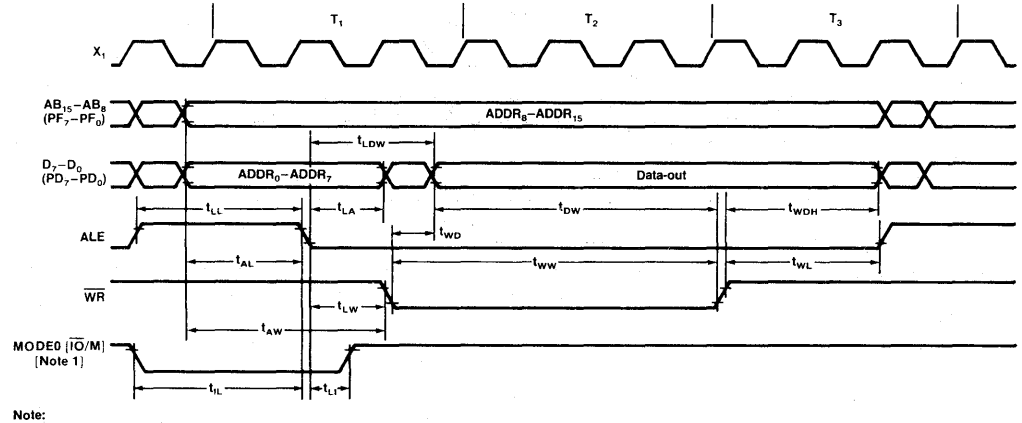
Write Operation



Note:

[1] IO/M signal is output to the MODE0 pin during a read or write of special register[s] Sr-Sr2, if MODE0 is pulled up to V_{DD}.

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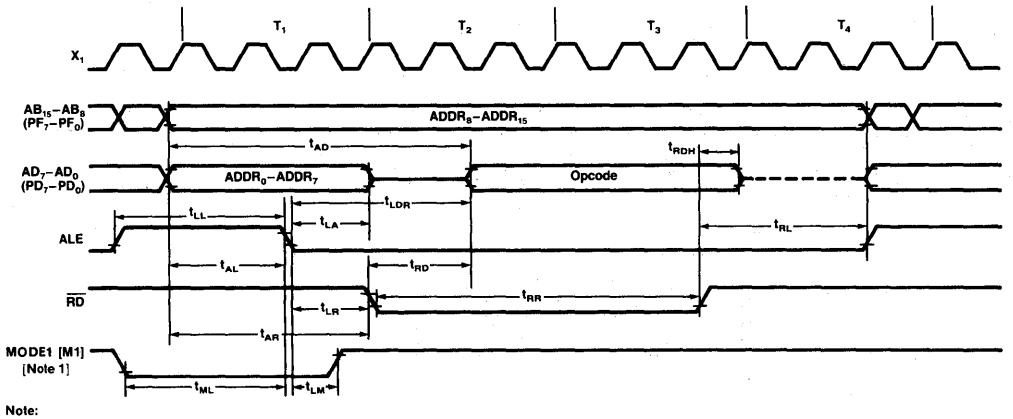
Timing Waveforms (cont)

Opcode Fetch Operation



Note:

[1] M1 signal is output to the MODE1 pin during Opcode Fetch if MODE1 pin is pulled up to V_{DD}.

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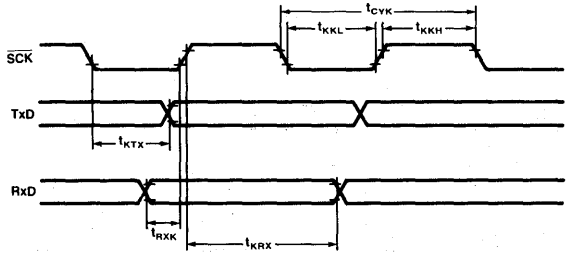
Serial Operation Transmit/Receive Timing



49-000546B

Operand Format/Description

Format	Description
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TxB, TM_0, TM_1, ZCM
sr1	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RxB, CR0, CR1, CR2, CR3
sr2	PA, PB, PC, PD, PF, MKH, ANM, MKL, SMH, EOM, TMM
sr3	ETM_0, ETM_1
sr4	ECNT, ECPT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+ , H + , D −, H −
rpa1	B, D, H
rpa2	B, D, H, D +, H + , D −, H −, D + byte, H + A, H + B, H + EA, H + byte
rpa3	D, H, D + +, H + +, D + byte, H + A, H + B, H + EA, H + byte
wa	8-Bit immediate data
word	16-Bit immediate data
byte	8-Bit immediate data
bit	3-Bit immediate data
f	CY, HC, Z
irf	FNMI, FT0, FT1, F1, F2, FE0, FE1, FEIN, FAD, FSR, FST, ER, OV, AN_4, AN_5, AN_6, AN_7, SB

Instruction Set Symbol Definitions

Symbol	Description
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
∀	Exclusive OR
—	Complement
•	Concatenation

Remarks

1. sr-sr4 (special register)

PA = Port A
PB = Port B
PC = Port C
PD = Port D
PF = Port F
MA = Mode A
MB = Mode B
MC = Mode C
MCC = Mode Control C
MF = Mode F

MM = Memory Mapping
TM_0 = Timer Register 0
TM_1 = Timer Register 1
TMM = Timer Mode
ETM_0 = Timer/Event Counter Register 0
ETM_1 = Timer/Event Counter Register 1
ZCM = Zero-Cross Mode Control Register

ECNT = Timer/Event Counter Upcounter
ECPT = Timer/Event Counter Capture

ETMM = Timer/Event Counter Mode
EOM = Timer/Event Counter Output Mode

TxB = Tx Buffer
RxB = Rx Buffer
SMH = Serial Mode High
SML = Serial Mode Low
MKH = Mask High
MKL = Mask Low
ANM = A/D Channel Mode
CR_0 = A/D Conversion Result 0-3 to CR_3
TxB = Tx Buffer
RxB = Rx Buffer
SMH = Serial Mode High
SML = Serial Mode Low
MKH = Mask High High
MKL = Mask Low

2. rp-rp3 (register pair)

SP = Stack Pointer
B = BC
D = DE
H = HL
V = VA
EA = Extended Accumulator

3. rpa-rpa3 (rp addressing)

B = (BC)
D = (DE)
H = (HL)
D + = (DE) +
H − = (HL) +
D − = (DE) −
H − = (HL) −
D + + = (DE) ++
H + + = (HL) ++
D + byte = (DE) + byte
H + A = (HL) + (A)
H + B = (HL) + (B)
H + EA = (HL) + (EA)
H + byte = (HL) + byte

4. f (flag)

CY = Carry HC = Half Carry Z = Zero

5. irf (interrupt flag)

NMI = NMI* Input

FT0 = INTFT0
FT1 = INTFT1
F1 = INTF1
F2 = INTF2
FE0 = INTFE0
FE1 = INTFE1

FEIN = INTFEIN
FAD = INTFAD
FSR = INTFSR
FST = INTFST
ER = Error
OV = Overflow
AN_4 to AN_7 = Analog Input 4-7
SB = Standby

Instruction Set

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
8-Bit Data Transfer																					
MOV	r1,A	(r1) ← (A)	0	0	0	1	1	T_2	T_1	T_0									4	1	
	A, r1	(A) ← (r1)	0	0	0	0	1	T_2	T_1	T_0									4	1	
	*sr,A	(sr) ← (A)	0	1	0	0	1	1	0	1	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	*A,sr1	(A) ← (sr1)	0	1	0	0	1	1	0	0	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	r,word	(r) ← (word)	0	1	1	1	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
	word,r	(word) ← (r)	0	1	1	1	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
MVI	*r,byte	(r) ← byte set L1 if r = A set L0 if r = L	0	1	1	0	1	R_2	R_1	R_0	Data								7	2	L1 = 1 and r = A L0 = 1 and r = L
	sr2,byte	(sr2) ← byte	0	1	1	0	0	1	0	0	S_3	0	0	0	0	S_2	S_1	S_0	14	3	
			Data																		
MVIW	*wa, byte	((V)•(wa)) ← byte	0	1	1	1	0	0	0	1	Offset								13	3	
			Data																		
MVIX	*rpa1,byte	(rpa1) ← byte	0	1	0	0	1	0	A_1	A_0	Data								10	2	
STAW	*wa	((V)•(wa)) ← A	0	1	1	0	0	0	1	1	Offset								10	2	
LDAW	*wa	(A) ← ((V)•(wa))	0	0	0	0	0	0	0	1	Offset								10	2	
STAX	*rpa2	(rpa2) ← (A)	A_3	0	1	1	1	A_2	A_1	A_0	Data (2)								7/13(3)	2	
LDAX	*rpa2	(A) ← ((rpa2))	A_3	0	1	0	1	A_2	A_1	A_0	Data (2)								7/13(3)	2	
EXX		(B) ↔ (B'),(C) ↔ (C'),(D) ↔ (D') (E) ↔ (E'),(H) ↔ (H'),(L) ↔ (L')	0	0	0	1	0	0	0	1									4	1	
EXA		(V) ↔ (V'),(A) ↔ (A'),(EA) ↔ (EA')	0	0	0	1	0	0	0	0									4	1	
EXH		(H) ↔ (H'),(L) ↔ (L')	0	1	0	1	0	0	0	0									4	1	
16-Bit Data Transfer																					
BLOCK	D	((DE)) ← ((HL)),(DE) ← (DE + 1), (HL) ← (HL) + 1, (C) ← (C) − 1 End if borrow	0	0	1	1	0	0	0	1									13 x (C + 1)	1	
DMOV	rp3, EA	($rp3_L$) ← (EAL),($rp3_H$) ← (EAH)	1	0	1	1	0	1	P_1	P_0									4	1	
	EA,rp3	(EAL) ← ($rp3_L$),(EAH) ← ($rp3_H$)	1	0	1	0	0	1	P_1	P_0									4	1	

NEC

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 7	6	5	4	3	2	1	0	B2 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
16-Bit Data Transfer (cont)																					
DMOV	sr3, EA	(sr3) ← (EA)	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1	U_0	14	2	
	EA,sr4	(EA) ← (sr4)	0	1	0	0	1	0	0	0	1	1	0	0	0	0	V_1	V_0	14	2	
SBCD	word	(word) ← (C), (word + 1) ← (B)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	20	4	
			Low addr								High addr										
SDED	word	(word) ← (E), (word + 1) ← (D)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	0	20	4	
			Low addr								High addr										
SHLD	word	(word) ← (L), (word + 1) ← (H)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	20	4	
			Low addr								High addr										
SSPD	word	(word) ← (SP_L),(word + 1) ← (SP_H)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	20	4	
			Low addr								High addr										
STEAX	rpa3	((rpa3)) ← (EAL),((rpa3) + 1 ← (EAH)	0	1	0	0	1	0	0	0	1	0	0	1	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
LBCD	word	(C) ← (word),(B) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	20	4	
			Low addr								High addr										
LDED	word	(E) ← (word),(D) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	20	4	
			Low addr								High addr										
LHLD	word	(L) ← (word),(H) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	20	4	
			Low addr								High addr										
LSPD	word	(SP_L) ← (word),(SP_H) ← ((word) + 1)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	20	4	
			Low addr								High addr										
LDEAX	rpa3	(EAL) ← ((rpa3)),(EAH) ← ((rpa3) + 1)	0	1	0	0	1	0	0	0	1	0	0	0	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
PUSH	rp1	((SP) − 1) ← ($rp1_H$) ((SP) − 2) ← ($rp1_L$) (SP) ← (SP) − 2	1	0	1	1	0	Q_2	Q_1	Q_0									13	1	
POP	rp1	($rp1_L$) ← ((SP)),($rp1_H$) ← ((SP) + 1) (SP) ← (SP) + 2	1	0	1	0	0	Q_2	Q_1	Q_0									10	1	
LXI	*rp2,word	(rp2) ← (word) set L0 if rp2 = H	0	P_2	P_1	P_0	0	1	0	0	Low byte								10	3	L0 = 1 and rp2 = H
			High byte																		
TABLE		(C) ← ((PC)+3+(A)),B ← ((PC)+3+(A)+ 1)	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	0	17	2	
8-Bit Arithmetic (Register)																					
ADD	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	1	0	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	1	0	0	0	R_2	R_1	R_0	8	2	
ADC	A,r	(A) ← (A) + (r) + (CY)	0	1	1	0	0	0	0	0	1	1	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A) + (CY)	0	1	1	0	0	0	0	0	0	1	0	1	0	R_2	R_1	R_0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code 7	6	5	4	B1 3	2	1	0	7	6	5	B2 4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Arithmetic (Register) (cont)																					
ADDNC	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	0	1	0	0	R_2	R_1	R_0	8	2	No carry
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	0	1	0	0	R_2	R_1	R_0	8	2	No carry
SUB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	0	R_2	R_1	R_0	8	2	
SBB	A,r	(A) ← (A) − (r) − (CY)	0	1	1	0	0	0	0	0	1	1	1	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A) − (CY)	0	1	1	0	0	0	0	0	0	1	1	1	0	R_2	R_1	R_0	8	2	
SUBNB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
ANA	A,r	(A) ← (A) ∧ (r)	0	1	1	0	0	0	0	0	1	0	0	0	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∧ (A)	0	1	1	0	0	0	0	0	0	0	0	0	1	R_2	R_1	R_0	8	2	
ORA	A,r	(A) ← (A) V (r)	0	1	1	0	0	0	0	0	1	0	0	1	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) V (A)	0	1	1	0	0	0	0	0	0	0	0	1	1	R_2	R_1	R_0	8	2	
XRA	A,r	(A) ← (A) V (r)	0	1	1	0	0	0	0	0	1	0	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) V (A)	0	1	1	0	0	0	0	0	0	0	0	1	0	R_2	R_1	R_0	8	2	
GTA	A,r	(A) − (r) − 1	0	1	1	0	0	0	0	0	1	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) − (A) − 1	0	1	1	0	0	0	0	0	0	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
LTA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
NEA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	1	R_2	R_1	R_0	8	2	No zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	8	2	No zero
EQA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	1	1	R_2	R_1	R_0	8	2	Zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	8	2	Zero
ONA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	0	1	R_2	R_1	R_0	8	2	No zero
OFFA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	1	1	R_2	R_1	R_0	8	2	Zero
8-Bit Arithmetic (Memory)																					
ADDX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	0	A_2	A_1	A_0	11	2	
ADCX	rpa	(A) ← (A) + ((rpa)) + (CY)	0	1	1	1	0	0	0	0	1	1	0	1	0	A_2	A_1	A_0	11	2	
ADDNCX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	0	1	0	0	A_2	A_1	A_0	11	2	No carry
SUBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	0	A_2	A_1	A_0	11	2	
SBBX	rpa	(A) ← (A) − ((rpa)) − (CY)	0	1	1	1	0	0	0	0	1	1	1	1	0	A_2	A_1	A_0	11	2	
SUBNBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	0	A_2	A_1	A_0	11	2	No borrow
ANAX	rpa	(A) ← (A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	0	1	A_2	A_1	A_0	11	2	
ORAX	rpa	(A) ← (A) V ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	1	A_2	A_1	A_0	11	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 7	6	5	4	B3 3	2	1	0	B2 7	6	5	B4 4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Arithmetic (Memory) (cont)																					
XRAX	rpa	(A) ← (A) V ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	0	A_2	A_1	A_0	11	2	
GTAX	rpa	(A) – ((rpa)) – 1	0	1	1	1	0	0	0	0	1	0	1	0	1	A_2	A_1	A_0	11	2	No borrow
LTAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	1	A_2	A_1	A_0	11	2	Borrow
NEAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	1	A_2	A_1	A_0	11	2	No zero
EQAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	1	1	A_2	A_1	A_0	11	2	Zero
ONAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	1	A_2	A_1	A_0	11	2	No zero
OFFAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	1	1	A_2	A_1	A_0	11	2	Zero
Immediate Data																					
ADI	*A,byte	(A) ← (A) + byte	0	1	0	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	1	0	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2, byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	1	0	0	0	S_2	S_1	S_0	20	3	
			Data																		
ACI	*A,byte	(A) ← (A) + byte + (CY)	0	1	0	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte + (CY)	0	1	1	1	0	1	0	0	0	1	0	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte + (CY)	0	1	1	0	0	1	0	0	S_3	1	0	1	0	S_2	S_1	S_0	20	3	
			Data																		
ADINC	*A,byte	(A) ← (A) + byte	0	0	1	0	0	1	1	0	Data								7	2	No carry
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	0	1	0	0	R_2	R_1	R_0	11	3	No carry
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	0	1	0	0	S_2	S_1	S_0	20	3	No carry
			Data																		
SUI	*A,byte	(A) ← (A) – byte	0	1	1	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte	0	1	1	1	0	1	0	0	0	1	1	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte	0	1	1	0	0	1	0	0	S_3	1	1	0	0	S_2	S_1	S_0	20	3	
			Data																		
SBI	*A,byte	(A) ← (A) – byte – (CY)	0	1	1	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte – (CY)	0	1	1	1	0	1	0	0	0	1	1	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte – (CY)	0	1	1	0	0	1	0	0	S_3	1	1	1	0	S_2	S_1	S_0	20	3	
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	Operation Code B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Immediate Data (cont)																					
SUINB	*A,byte	(A) ← (A) − byte	0	0	1	1	0	1	1	0					Data				7	2	No borrow
	r,byte	(r) ← (r) − byte	0	1	1	1	0	1	0	0	0	0	1	1	0	R_2	R_1	R_0	11	3	No borrow
							Data														
	sr2,byte	(sr2) ← (sr2) − byte	0	1	1	0	0	1	0	0	S_3	0	1	1	0	S_2	S_1	S_0	20	3	No borrow
							Data														
ANI	*A,byte	(A) ← (A) ∧ byte	0	0	0	0	0	1	1	1					Data				7	2	
	r,byte	(r) ← (r) ∧ byte	0	1	1	1	0	1	0	0	0	0	0	0	1	R_2	R_1	R_0	11	3	
							Data														
	sr2,byte	(sr2) ← (sr2) ∧ byte	0	1	1	0	0	1	0	0	S_3	0	0	0	1	S_2	S_1	S_0	20	3	
							Data														
ORI	*A,byte	(A) ← (A) V byte	0	0	0	1	0	1	1	1					Data				7	2	
	r,byte	(r) ← (r) V byte	0	1	1	1	0	1	0	0	0	0	0	1	1	R_2	R_1	R_0	11	3	
							Data														
	sr2,byte	(sr2) ← (sr2) V byte	0	1	1	0	0	1	0	0	S_3	0	0	1	1	S_2	S_1	S_0	20	3	
							Data														
XRI	*A,byte	(A) ← (A) V byte	0	0	0	1	0	1	1	0					Data				7	2	
	r,byte	(r) ← (r) V byte	0	1	1	1	0	1	0	0	0	0	0	1	0	R_2	R_1	R_0	11	3	
							Data														
	sr2,byte	(sr2) ← (sr2) V byte	0	1	1	0	0	1	0	0	S_3	0	0	1	0	S_2	S_1	S_0	20	3	
							Data														
GTI	*A,byte	(A) − byte − 1	0	0	1	0	0	1	1	1					Data				7	2	No borrow
	r,byte	(r) − byte − 1	0	1	1	1	0	1	0	0	0	0	1	0	1	R_2	R_1	R_0	11	3	No borrow
							Data														
	sr2,byte	(sr2) − byte − 1	0	1	1	0	0	1	0	0	S_3	0	1	0	1	S_2	S_1	S_0	14	3	No borrow
							Data														
LTI	*A,byte	(A) − byte	0	0	1	1	0	1	1	1					Data				7	2	Borrow
	r,byte	(r) − byte	0	1	1	1	0	1	0	0	0	0	1	1	1	R_2	R_1	R_0	11	3	Borrow
							Data														
	sr2,byte	(sr2) − byte	0	1	1	0	0	1	0	0	S_3	0	1	1	1	S_2	S_1	S_0	14	3	Borrow
							Data														
NEI	*A,byte	(A) − byte	0	1	1	0	0	1	1	1					Data				7	2	No zero
	r,byte	(r) − byte	0	1	1	1	0	1	0	0	0	1	1	0	1	R_2	R_1	R_0	11	3	No zero
							Data														

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1	B2	B3	B4	State(1)	Bytes	Skip Condition
Immediate Data (cont)									
NEI	sr2,byte	(sr2) – byte	0 1 1 0 0 1 0 0	S_3 1 1 0 1 S_2 S_1 S_0	Data		14	3	No zero
EQI	*A,byte	(A) – byte	0 1 1 1 0 1 1 1	Data			7	2	Zero
	r,byte	(r) – byte	0 1 1 1 0 1 0 0	0 1 1 1 1 R_2 R_1 R_0	Data		11	3	Zero
	sr2,byte	(sr2) – byte	0 1 1 0 0 1 0 0	S_3 1 1 1 1 S_2 S_1 S_0	Data		14	3	Zero
ONI	*A,byte	(A) ∧ byte	0 1 0 0 0 1 1 1	Data			7	2	No zero
	r,byte	(r) ∧ byte	0 1 1 1 0 1 0 0	0 1 0 0 1 R_2 R_1 R_0	Data		11	3	No zero
	sr2,byte	(sr2) ∧ byte	0 1 1 0 0 1 0 0	S_3 1 0 0 1 S_2 S_1 S_0	Data		14	3	No zero
OFFI	*A,byte	(A) ∧ byte	0 1 0 1 0 1 1 1	Data			7	2	Zero
	r,byte	(r) ∧ byte	0 1 1 1 0 1 0 0	0 1 0 1 1 R_2 R_1 R_0	Data		11	3	Zero
	sr2,byte	(sr2) ∧ byte	0 1 1 0 0 1 0 0	S_3 1 0 1 1 S_2 S_1 S_0	Data		14	3	Zero
Working Register									
ADDW	wa	(A) ← (A) + ((V)•(wa))	0 1 1 1 0 1 0 0	1 1 0 0 0 0 0 0	Offset		14	3	
ADCW	wa	(A) ← (A) + ((V)•(wa)) + (CY)	0 1 1 1 0 1 0 0	1 1 0 1 0 0 0 0	Offset		14	3	
ADDNCW	wa	(A) ← (A) + ((V)•(wa))	0 1 1 1 0 1 0 0	1 0 1 0 0 0 0 0	Offset		14	3	No carry
SUBW	wa	(A) ← (A) – ((V)•(wa))	0 1 1 1 0 1 0 0	1 1 1 0 0 0 0 0	Offset		14	3	
SBBW	wa	(A) ← (A) – ((V)•(wa)) – (CY)	0 1 1 1 0 1 0 0	1 1 1 1 0 0 0 0	Offset		14	3	
SUBNBW	wa	(A) ← (A) – ((V)•(wa))	0 1 1 1 0 1 0 0	1 0 1 1 0 0 0 0	Offset		14	3	No borrow
ANAW	wa	(A) ← (A) ∧ ((V)•(wa))	0 1 1 1 0 1 0 0	1 0 0 0 1 0 0 0	Offset		14	3	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 B3 7	6	5	4	3	2	1	0	B2 B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Working Register (cont)																					
ORAW	wa	(A) ← (A) V ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0	14	3	
			Offset																		
XRAW	wa	(A) ← (A) V ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0	14	3	
			Offset																		
GTAW	wa	(A) – ((V)•(wa)) – 1	0	1	1	1	0	1	0	0	1	0	1	0	1	0	0	0	14	3	No borrow
			Offset																		
LTAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	1	1	0	0	0	14	3	Borrow
			Offset																		
NEAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	0	1	0	0	0	14	3	No zero
			Offset																		
EQAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	0	1	0	0	0	14	3	Zero
			Offset																		
ONAW	wa	(A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	0	1	0	0	0	14	3	No zero
			Offset																		
OFFAW	wa	(A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	1	0	0	0	0	14	3	Zero
			Offset																		
ANIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) ∧ byte	0	0	0	0	0	1	0	1	Offset								19	3	
			Data																		
ORIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) V byte	0	0	0	1	0	1	0	1	Offset								19	3	
			Data																		
GTIW	*wa,byte	((V)•(wa)) – byte – 1	0	0	1	0	0	1	0	1	Offset								13	3	No borrow
			Data																		
LTIW	*wa,byte	((V)•(wa)) – byte	0	0	1	1	0	1	0	1	Offset								13	3	Borrow
			Data																		
NEIW	*wa,byte	((V)•(wa)) – byte	0	1	1	0	0	1	0	1	Offset								13	3	No zero
			Data																		
EQIW	*wa,byte	((V)•(wa)) – byte	0	1	1	1	0	1	0	1	Offset								13	3	Zero
			Data																		
ONIW	*wa,byte	((V)•(wa)) ∧ byte	0	1	0	0	0	1	0	1	Offset								13	3	No zero
			Data																		
OFFIW	*wa,byte	((V)•(wa)) ∧ byte	0	1	0	1	0	1	0	1	Offset								13	3	Zero
			Data																		

NEC

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 B3 7	6	5	4	3	2	1	0	Operation Code B2 B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
16-Bit Arithmetic																					
EADD	EA,r2	(EA) ← (EA) + (r2)	0	1	1	1	0	0	0	0	0	1	0	0	0	0	R_1	R_0	11	2	
DADD	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	0	1	P_1	P_0	11	2	
DADC	EA,rp3	(EA) ← (EA) + (rp3) + (CY)	0	1	1	1	0	1	0	0	1	1	0	1	0	1	P_1	P_0	11	2	
DADDNC	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	0	1	0	0	1	P_1	P_0	11	2	No carry
ESUB	EA,r2	(EA) ← (EA) − (r2)	0	1	1	1	0	0	0	0	0	1	1	0	0	0	R_1	R_0	11	2	
DSUB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	0	1	P_1	P_0	11	2	
DSBB	EA,rp3	(EA) ← (EA) − (rp3) − (CY)	0	1	1	1	0	1	0	0	1	1	1	1	0	1	P_1	P_0	11	2	
DSUBNB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	0	1	P_1	P_0	11	2	No borrow
DAN	EA,rp3	(EA) ← (EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	0	0	0	1	1	P_1	P_0	11	2	
DOR	EA,rp3	(EA) ← (EA) V (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	1	1	P_1	P_0	11	2	
DXR	EA,rp3	(EA) ← (EA) V (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	0	1	P_1	P_0	11	2	
DGT	EA,rp3	(EA) − (rp3) − 1	0	1	1	1	0	1	0	0	1	0	1	0	1	1	P_1	P_0	11	2	No borrow
DLT	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	1	1	P_1	P_0	11	2	Borrow
DNE	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	1	1	P_1	P_0	11	2	No zero
DEQ	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	1	1	1	P_1	P_0	11	2	Zero
DON	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	1	1	P_1	P_0	11	2	No zero
DOFF	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	1	1	1	P_1	P_0	11	2	Zero
Multiply/Divide																					
MUL	r2	(EA) ← (A) x (r2)	0	1	0	0	1	0	0	0	0	0	1	0	1	1	R_1	R_0	32	2	
DIV	r2	(EA) ← (EA) + (r2), (r2) ← Remainder	0	1	0	0	1	0	0	0	0	0	1	1	1	1	R_1	R_0	59	2	
Increment/Decrement																					
INR	r2	(r2) ← (r2) + 1	0	1	0	0	0	0	R_1	R_0									4	1	Carry
INRW	*wa	((V)•(wa)) ← ((V)•(wa)) + 1	0	0	1	0	0	0	0	0				Offset					16	2	Carry
INX	rp	(rp) ← (rp) + 1	0	0	P_1	P_0	0	0	1	0									7	1	
	EA	(EA) ← (EA) + 1	1	0	1	0	1	0	0	0									7	1	
DCR	r2	(r2) ← (r2) − 1	0	1	0	1	0	0	R_1	R_0									4	1	Borrow
DCRW	*wa	((V)•(wa)) ← ((V)•(wa)) − 1	0	0	1	1	0	0	0	0				Offset					16	2	Borrow
DCX	rp	(rp) ← (rp) − 1	0	0	P_1	P_0	0	0	1	1									7	1	
	EA	(EA) ← (EA) − 1	1	0	1	0	1	0	0	1									7	1	
Others																					
DAA		Decimal Adjust Accumulator	0	1	1	0	0	0	0	1									4	1	
STC		(CY) ← 1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	8	2	
CLC		(CY) ← 0	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0			
Others (cont)													
NEGA		(A) ← (A) + 1	0	1	0	0	1	0	0	0	8	2	
Rotate and Shift													
RLD		Rotate left digit	0	1	0	0	1	0	0	0	17	2	
RRD		Rotate right digit	0	1	0	0	1	0	0	0	17	2	
RLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow (CY)$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	8	2	
RLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$, $(r2_7) \leftarrow (CY)$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	8	2	
SLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	8	2	
SLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$, $(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	8	2	
SLLC	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	8	2	Carry
SLRC	r2	$(r2_{m-1}) \leftarrow (r2_m)$, $(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	8	2	Carry
DRLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$, $(EA_0) \leftarrow (CY)$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	8	2	
DRLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$, $(EA_{15}) \leftarrow (CY)$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	8	2	
DSLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$, $(EA_0) \leftarrow 0$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	8	2	
DSLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$, $(EA_{15}) \leftarrow 0$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	8	2	
Jump													
JMP	*word	(PC) ← word	0	1	0	1	0	1	0	0	10	3	
			High addr								Low addr		
JB		$(PC_H) \leftarrow (B)$, $(PC_L) \leftarrow (C)$	0	0	1	0	0	0	0	1	4	1	
JR	word	(PC) ← (PC) + 1 + jdisp 1	1	1	←		jdisp1			→	10	1	
JRE	*word	(PC) ← (PC) + 2 + jdisp	0	1	0	0	1	1	1	←	jdisp	→	10	2	
JEA		(PC) ← (EA)	0	1	0	0	1	0	0	0	8	2	
Call													
CALL	*word	$((SP) - 1) \leftarrow ((PC) + 3)_H$, $((SP) - 2) \leftarrow ((PC) + 3)_L$, (PC) ← word, (SP) ← (SP) − 2	0	1	0	0	0	0	0	0	16	3	
			High addr								Low addr		
CALB		$((SP) - 1) \leftarrow ((PC) + 2)_H$, $((SP) - 2) \leftarrow ((PC) + 2)_L$, $(PC_H) \leftarrow (B)$, $(PC_L) \leftarrow (C)$, (SP) ← (SP) − 2	0	1	0	0	1	0	0	0	17	2	
CALF	*word	$((SP) - 1) \leftarrow ((PC) + 2)_H$, $((SP) - 2) \leftarrow ((PC) + 2)_L$, $(PC_{15\text{-}11}) \leftarrow 00001$, $(PC_{10\text{-}0}) \leftarrow$ fa, (SP) ← (SP) − 2	0	1	1	1	1	←			13	2	
			fa							→			

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Call (cont)																					
CALT	word	$((SP)-1) \leftarrow ((PC)+1)_H$, $((SP)-2) \leftarrow ((PC)+1)_L$ $(PC_L) \leftarrow (128+2ta)$,$(PC_H) \leftarrow$ $(129+2ta)$,$(SP) \leftarrow (SP)-2$	1	0	0	←		ta		→									16	1	
SOFTI		$((SP)-1) \leftarrow (PSW)$,$((SP)-2) \leftarrow$ $((PC)+1)_H$,$((SP)-3) \leftarrow ((PC)+1)_L$, $(PC) \leftarrow 0060H$,$(SP) \leftarrow (SP)-3$	0	1	1	1	0	0	1	0									16	1	
Return																					
RET		$(PC_L) \leftarrow ((SP))$,$(PC_H) \leftarrow ((SP)+1)$ $(SP) \leftarrow (SP)+2$	1	0	1	1	1	0	0	0									10	1	
RETS		$(PC_L) \leftarrow ((SP))$,$(PC_H) \leftarrow ((SP)+1)$ $(SP) \leftarrow (SP)+2$,$(PC) \leftarrow (PC)+n$	1	0	1	1	1	0	0	1									10	1	Unconditional Skip
RETI		$(PC_L) \leftarrow ((SP))$,$(PC_H) \leftarrow ((SP)+1)$ $(PSW) \leftarrow ((SP)+2)$, $(SP) \leftarrow (SP)+3$	0	1	1	0	0	0	1	0									13	1	
Skip																					
Bit		bit, wa	0	1	0	1	1	B_2	B_1	B_0	Offset								10	2	Bit Test
CPU Control																					
SK	f	Skip if f = 1	0	1	0	0	1	0	0	0	0	0	0	0	1	F_2	F_1	F_0	8	2	f = 1
SKN	f	Skip if f = 0	0	1	0	0	1	0	0	0	0	0	0	1	1	F_2	F_1	F_0	8	2	f = 0
SKIT	irf	Skip if irf = 1, then reset irf	0	1	0	0	1	0	0	0	0	1	0	I_4	I_3	I_2	I_1	I_0	8	2	irf = 1
SKNIT	irf	Skip if irf = 0 Reset irf if irf = 1	0	1	0	0	1	0	0	0	0	1	1	I_4	I_3	I_2	I_1	I_0	8	2	irf = 0
NOP		No operation	0	0	0	0	0	0	0	0									4	1	
EI		Enable interrupt	1	0	1	0	1	0	1	0									4	1	
DI		Disable interrupt	1	0	1	1	1	0	1	0									4	1	
HLT		Halt CPU operation	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	1	12	2	
STOP		Stop system clock	0	1	0	0	1	0	0	0	1	0	1	1	1	0	1	1	12	2	

Notes:

(1) In the case of skip condition, the idle states are as follows:

1-byte instruction: 4 states	2-byte instruction (with *): 7 states
2-byte instruction: 8 states	3-byte instruction (with *): 10 states
3-byte instruction: 11 states	4-byte instruction: 14 states

(2) B2 (Data): rpa2 = D + byte, H + byte.

(3) Right side of slash (/) in states indicates case rpa2, rpa3 = D + byte, H + A, H + B, H + EA, H + byte.

(4) B3 (Data): rpa3 = D + byte, H + byte

μPD7810H/11H 8-BIT, SINGLE-CHIP NMOS MICROCOMPUTERS WITH A/D CONVERTER

Description

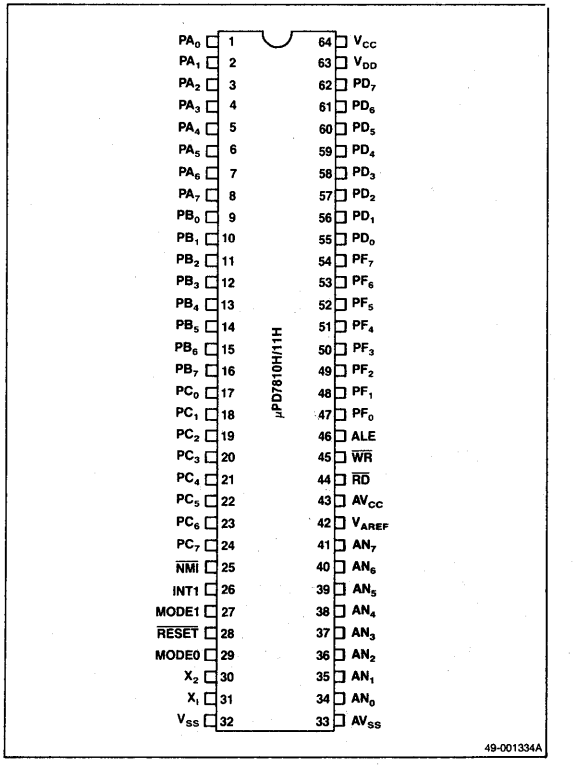
The μPD7810H and μPD7811H single-chip microcomputers integrate sophisticated on-chip peripheral functionality normally provided by external components. The devices' internal 16-bit ALU and data paths, combined with a powerful instruction set and addressing, make the μPD7810H/11H appropriate in data processing as well as control applications. The devices integrate a 16-bit ALU, 4K-ROM, 256-byte RAM with an 8-channel A/D converter, a multifunction 16-bit timer/event counter, two 8-bit timers, a USART, and two zero-cross detect inputs on a single die, allowing their use in fast, high-end processing applications. This involves analog signal interface and processing.

The μPD7810H/11H are high-speed versions of the μPD7810/11. The μPD7811H is the mask-ROM high volume production device embedded with custom customer program. The μPD7810H is a ROM-less version for prototyping and small volume production.

Features

- ☐ NMOS silicon gate technology requiring +5 V power supply
- ☐ Complete single-chip microcomputer
  - —16-bit ALU
  - —4K x 8 ROM
  - —256-byte RAM
- ☐ 44 I/O lines
- ☐ Two zero-cross detect inputs
- ☐ Two 8-bit timers
- ☐ Expansion capabilities
  - —8085A bus compatible
  - —60K-byte external memory address range
- ☐ 8-channel, 8-bit A/D converter
  - —Autoscan mode
  - —Channel select mode
- ☐ Full duplex USART
  - —Synchronous and asynchronous
- ☐ 153 instructions
  - —16-bit arithmetic, multiply and divide
- ☐ 1 μs instruction cycle time
- ☐ Prioritized interrupt structure
  - —3 external
  - —8 internal
- ☐ Standby function
- ☐ On-chip clock generator
- ☐ 64-pin plastic QUIP, shrink DIP

Pin Configuration



Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7810HG-36 μPD7811HG-36	64-pin plastic QUIP	15 MHz
μPD7810HCW μPD7811HCW	64-pin plastic shrink DIP	15 MHz

Pin Identification

No.	Symbol	Function
1-8	PA_0-PA_7	Port A I/O
9-16	PB_0-PB_7	Port B I/O
17	PC_0/TxD	Port C I/O line 0/Transmit data output
18	PC_1/RxD	Port C I/O line 1/Receive data input
19	PC_2/$\overline{SCK}$	Port C I/O line 2/Serial clock I/O
20	PC_3/TI/ $\overline{INT2}$	Port C I/O line 3/Timer input/Interrupt request 2 input
21	PC_4/TO	Port C I/O line 4/Timer output
22	PC_5/CI	Port C I/O line 5/Counter input
23, 24	PC_6, PC_7/ CO_0, CO_1	Port C I/O lines 6, 7/Counter outputs 0, 1
25	$\overline{NMI}$	Nonmaskable interrupt input
26	INT1	Interrupt request 1 input
27	MODE1/M1	Mode 1 input/Memory cycle 1 output
28	$\overline{RESET}$	Reset input
29	MODE0/ $\overline{IO}$/M	Mode 0 input/I/O/Memory output
30, 31	X2, X1	Crystal connections 1, 2
32	V_{SS}	Ground
33	AV_{SS}	Port T threshold voltage input
34-41	AN_0-AN_7	A/D converter analog inputs 0-7
42	V_{AREF}	A/D converter reference voltage
43	AV_{CC}	A/D converter power supply
44	$\overline{RD}$	Read strobe output
45	$\overline{WR}$	Write strobe output
46	ALE	Address latch enable output
47-54	PF_0-PF_7	Port F I/O/Expansion memory address bus bits 8-15
55-62	PD_0-PD_7	Port D I/O/Expansion memory address/ data bus
63	V_{DD}	RAM backup power supply
64	V_{CC}	5 V power supply

Pin Functions

PA_0-PA_7 [Port A]

Port A is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port A inputs.

PB_0-PB_7 [Port B]

Port B is an 8-bit three-state port. Each bit is independently programmable as either input or output. Reset makes all lines of port B inputs.

PC_0-PC_7 [Port C]

Port C is an 8-bit three-state port. Each bit is independently programmable as either input or output. Alternatively, the lines of port C can be used as control lines for the USART and timer. Reset puts all lines of port C in port mode, input.

TxD [Transmit Data]. Serial data output terminal.

RxD [Receive Data]. Serial data input terminal.

$\overline{SCK}$ [Serial Clock]. Output for the serial clock when internal clock is used. Input for serial clock when external clock is used.

TI [Timer Input]. Timer input terminal.

$\overline{INT2}$ [Interrupt Request 2]. Falling-edge-triggered, maskable interrupt input terminal and AC-input, zero-cross detection terminal.

TO [Timer Output]. The output of TO is a square wave with a frequency determined by the timer/counter.

CI [Counter Input]. External pulse input to timer/event counter.

CO_0, CO_1 [Counter Outputs 0, 1]. Programmable rectangular wave outputs based on timer/event counter.

PD_0-PD_7 [Port D]

Port D is an 8-bit three-state port. It can be programmed as either 8 bits of input or 8 bits of output. When external expansion memory is used, port D acts as the multiplexed address/data bus.

PF_0-PF_7 [Port F]

Port F is an 8-bit three-state port. Each bit is independently programmable as an input or output. When external expansion memory is used, port F outputs the high-order address bits.

AN_0-AN_7

These are the eight analog inputs to the A/D converter. AN_4-AN_7 can also be used as a digital input for falling edge detection.

AV_{SS} [A/D Converter Power Ground]

AV_{SS} is the ground potential for the A/D converter power supply.

$\overline{NMI}$ [Nonmaskable Interrupt]

Falling-edge-triggered nonmaskable interrupt input.

INT1 [Interrupt Request 1]

INT1 is a rising-edge-triggered, maskable interrupt input. It is also an AC-input, zero-cross detection terminal.

$\overline{\text{RESET}}$ [Reset]

When the $\overline{\text{RESET}}$ input is brought low, it initializes the μPD7810H/11H.

MODE1, MODE0 [Mode 1, 0]

The MODE1 and MODE0 inputs select the memory expansion mode. MODE1 also outputs the M1 signal during each opcode fetch. MODE0 outputs the IO/M signal.

V_{AREF} [A/D Converter Reference]

V_{AREF} set the upper limit for the A/D converter's conversion range.

AV_{CC} [A/D Converter Power]

This is the power supply voltage for the A/D converter.

$\overline{\text{RD}}$ [Read Strobe]

The $\overline{\text{RD}}$ output goes low to gate data from external devices onto the data bus. $\overline{\text{RD}}$ goes high during reset.

$\overline{\text{WR}}$ [Write Strobe]

The $\overline{\text{WR}}$ output goes low to indicate that the data bus holds valid data. It is a strobe signal for external memory or I/O write operations. $\overline{\text{WR}}$ goes high during reset.

ALE [Address Latch Enable]

The ALE output latches the address signal to the output of PD_0-PD_7.

X1, X2 [Crystal Connections 1, 2]

X1 and X2 are the system clock crystal oscillator terminals. X1 is the input for an external clock.

V_{SS} [Ground]

Ground potential.

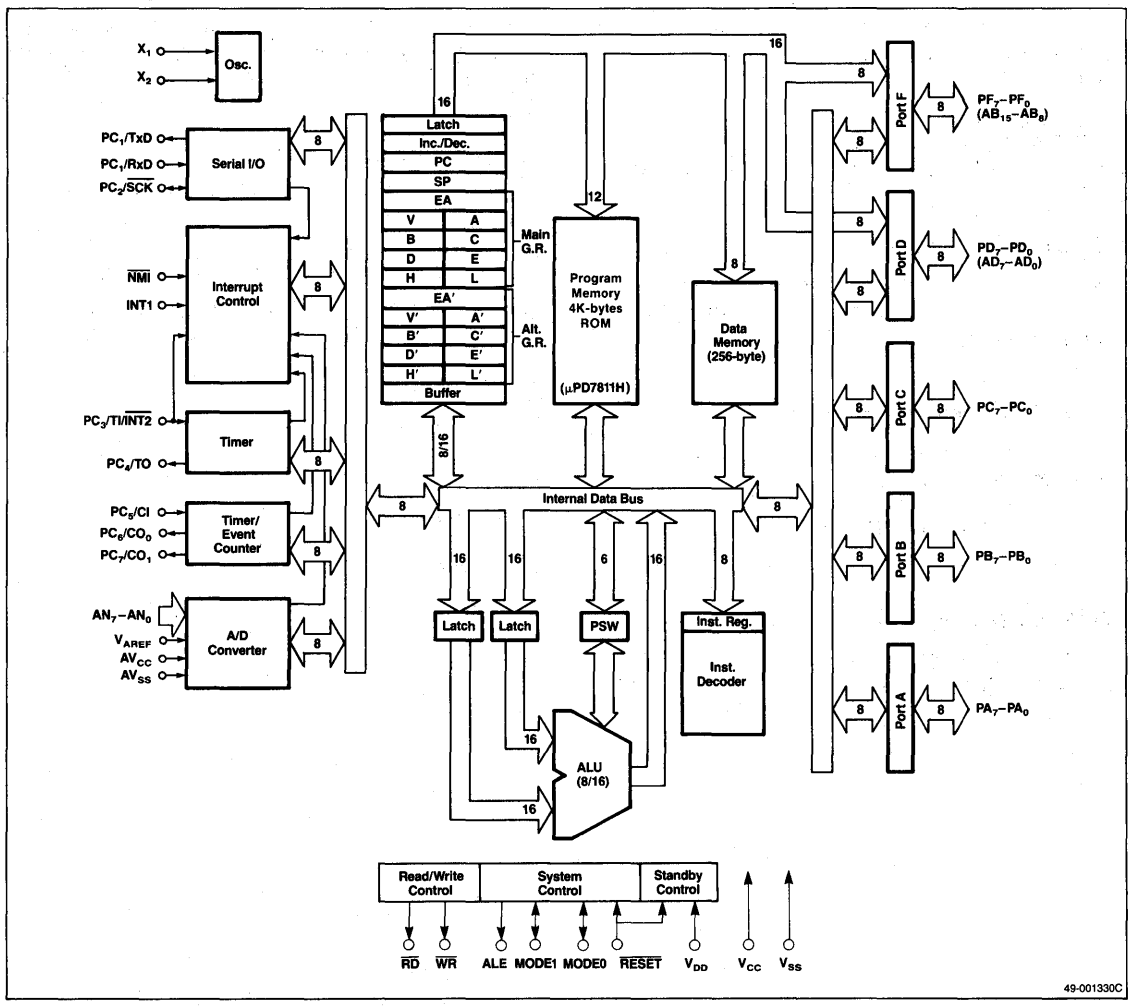
V_{DD} [Backup Power]

Backup power for on-chip RAM.

V_{CC} [Power Supply]

+5 V power supply.

Block Diagram



Functional Description

Memory Map

The μPD7811H can directly address up to 64K bytes of memory. Except for the on-chip ROM (0-4095) and RAM (65280-65535), any memory location can be used as ROM or RAM. The memory map, figure 1, defines the 0-to 64K-byte memory space for the μPD7811H.

Input/Output

The μPD7810H/11H has 8 analog input lines (AN_0-AN_7), 44 digital I/O lines, five 8-bit ports (port A, port B, port C, port D, port F), and 4 input lines (AN_4-AN_7).

Analog Input Lines. AN_0-AN_7 are configured as analog input lines for on-chip A/D converter.

Port A, Port B, Port C, Port F. Each line of these ports can be individually programmed as an input or output. When used as I/O ports, all have latched outputs and high-impedance inputs.

Port D. Port D can be programmed as a byte input or a byte output.

AN_4-AN_7. The high order analog input lines, AN_4-AN_7, can be used as digital input lines for falling edge detection.

Control Lines. Under software control, each line of port C can be configured individually to provide control lines for the serial interface, timer, and timer/counter.

Memory Expansion. In addition to the single-chip operation mode, the μPD7811H has four memory expansion modes. Under software control, port D can provide a multiplexed low-order address and data bus; port F can provide a high-order address bus. Table 1 shows the relation between memory expansion modes and the pin configurations of port D and port F.

Table 1. Memory Expansion Modes and Port Configurations

Memory Expansion	Port Configuration	
None	Port D	I/O port
	Port F	I/O port
256 Bytes	Port D	Multiplexed address/data bus
	Port F	I/O port
4K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_3	Address bus
	Port F_4-F_7	I/O port
16K Bytes	Port D	Multiplexed address/data bus
	Port F_0-F_5	Address bus
	Port F_6-F_7	I/O port
60K Bytes	Port D	Multiplexed address/data bus
	Port F	Address bus

Timers

There are two 8-bit timers. The timers may be programmed independently or may be cascaded and used as an 8-bit timer with 8-bit prescaler. The timer can be software set to increment at intervals of four machine cycles (1 μs at 12 MHz operation) or 128 machine cycles (32 μs at 12 MHz), or to increment on receipt of a pulse at TI. Figure 2 shows the block diagram for the timer.

Timer/Event Counter

The 16-bit multifunctional timer/event counter (figure 3) can be used for the following operations:

- Interval timer
- External event counter
- Frequency measurement
- Pulse width measurement
- Programmable square-wave output

Figure 1. Memory Map

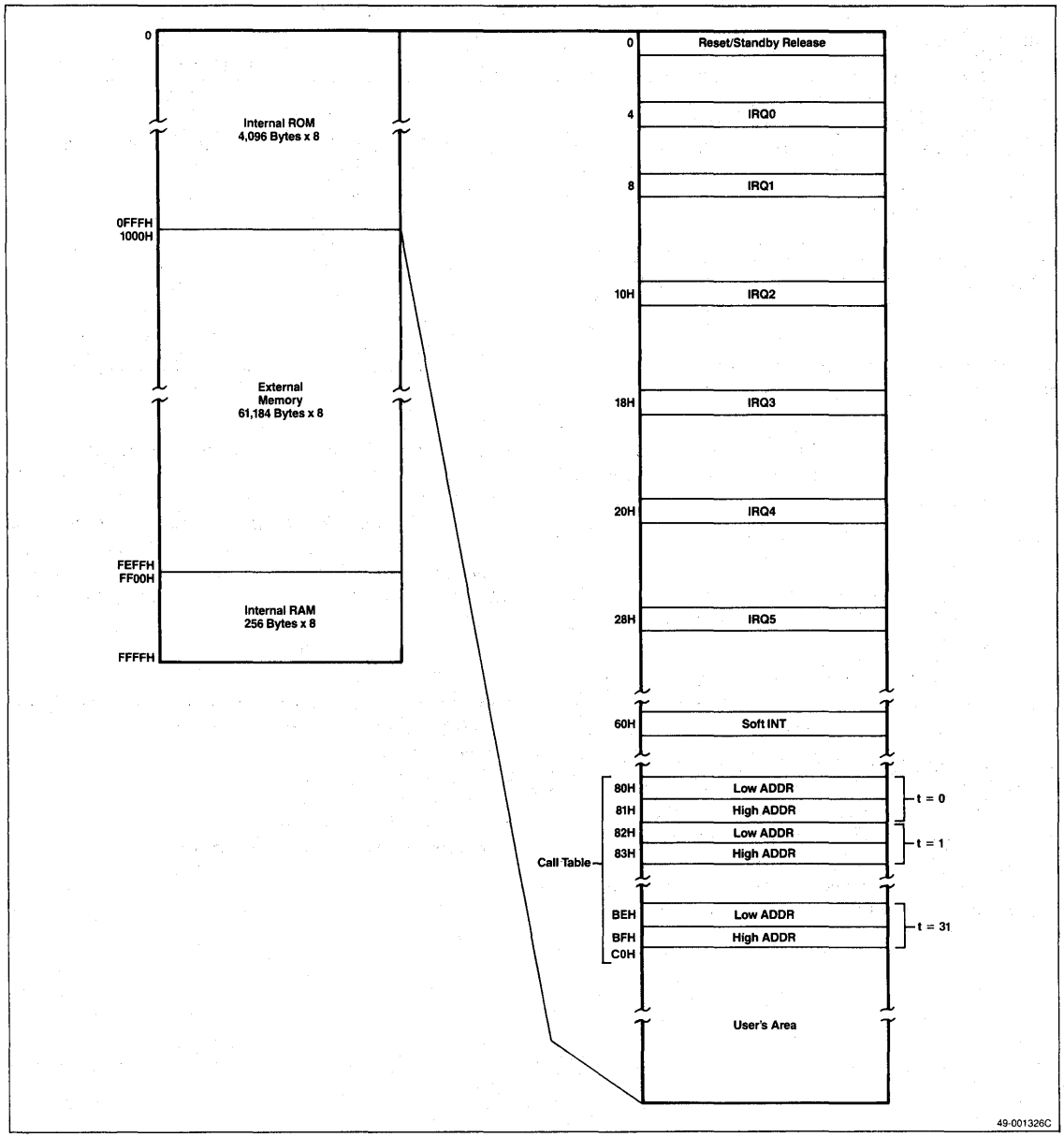
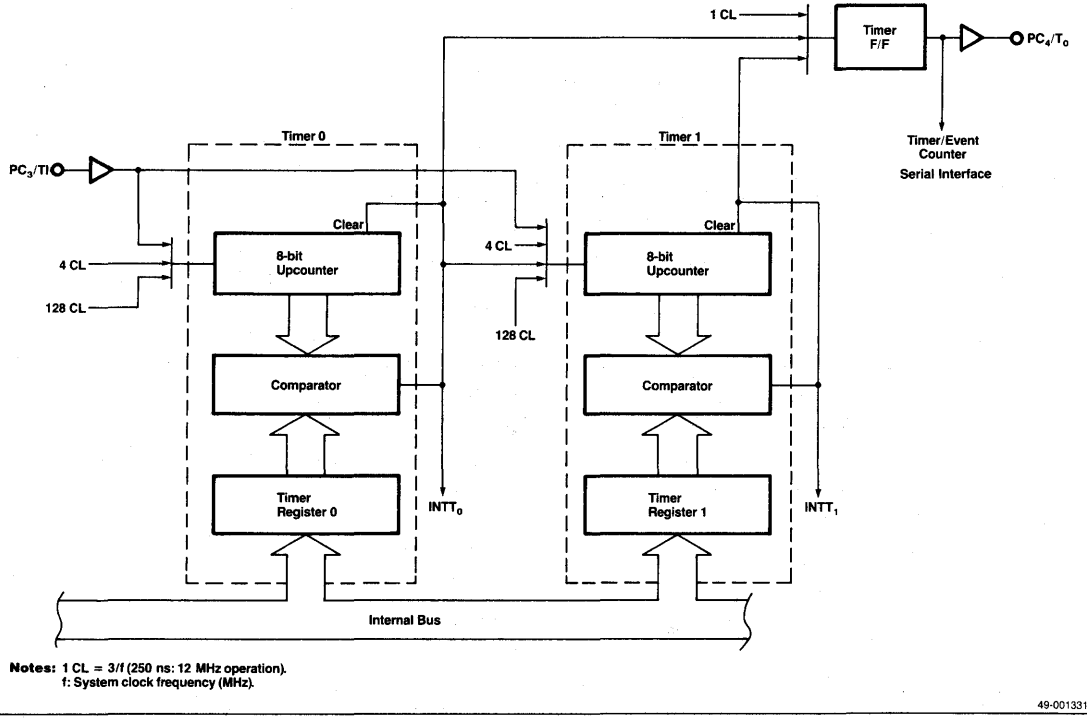


Figure 2. Timer Block Diagram



Notes: 1 CL = 3/f (250 ns: 12 MHz operation).
f: System clock frequency (MHz).

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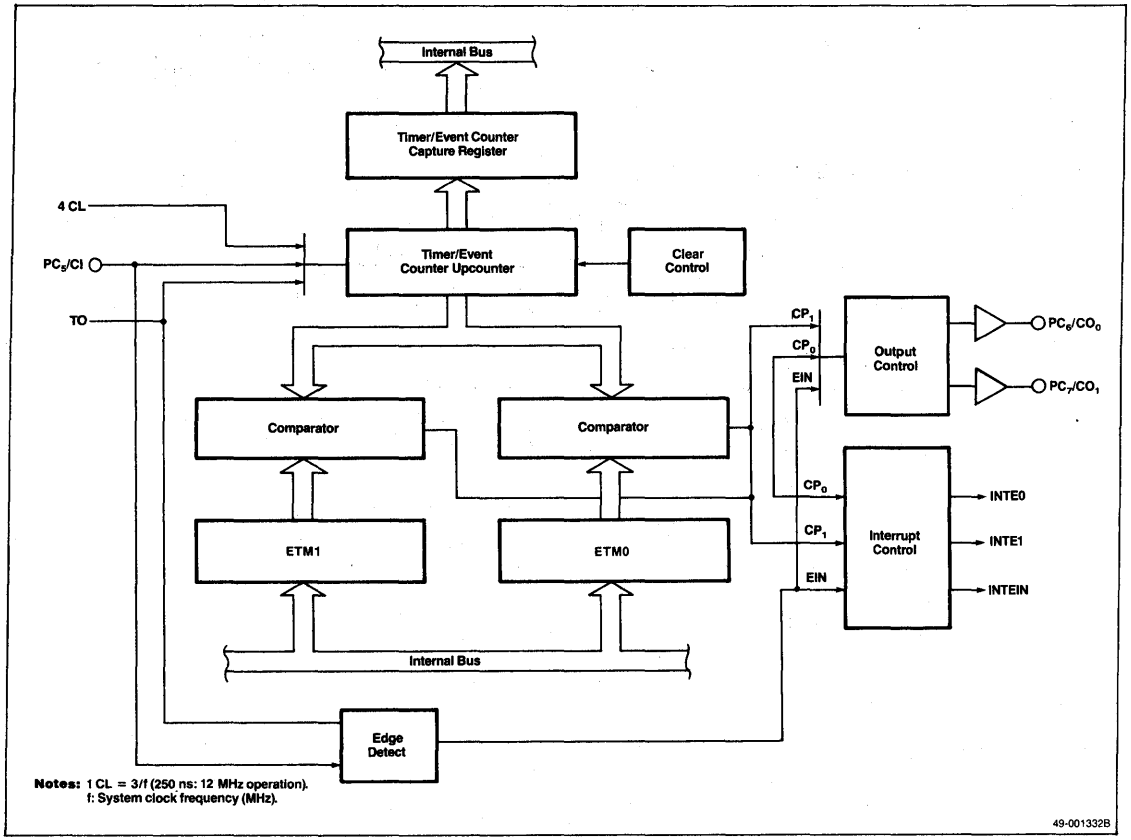
Figure 3. Block Diagram for Timer/Event Counter



8-Bit A/D Converter

- 8 input channels
- 4 conversion result registers
- 2 powerful operation modes
  —Autoscan mode
  —Channel select mode
- Successive approximation technique
- Absolute accuracy: ±1.5 LSB (±0.6%)
- Conversion range: 0 to 5 V
- Conversion time: 40 μs
- Interrupt generation

Analog/Digital Converter

The μPD7810H/11H features an 8-bit, high speed, high accuracy A/D converter. The A/D converter is made up of a 256-resistor ladder and a successive approximation register (SAR). There are four conversion result registers (CR_0-CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0-CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers. Figure 4 shows the block diagram for the A/D converter

Interrupt Structure

There are 11 interrupt sources. Three are external interrupts and eight are internal. The following, table 2, shows 11 interrupt sources divided into six priority levels. See figure 5.

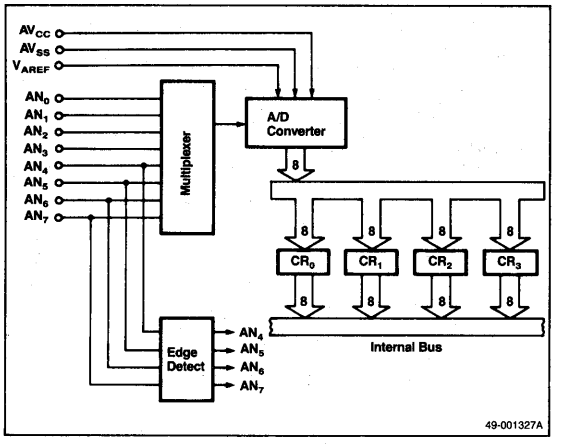
Standby Function

The standby function saves the top 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On power up you can check the standby flag (SB) to determine whether recovery was made from standby mode or from a cold start.

Table 2. Interrupt Sources

Interrupt Request	Interrupt Address	Type of Interrupt	Internal/ External
IRQ0	4	$\overline{NMI}$ (Nonmaskable interrupt)	Ext
IRQ1	8	INTT0 (Coincidence signal from timer 0)	Int
		INTT1 (Coincidence signal from timer 1)	
IRQ2	16	INT1 (Maskable interrupt)	Ext
		$\overline{INT2}$ (Maskable interrupt)	
IRQ3	24	INTE0 (Coincidence signal from timer/event counter)	Int
		INTE1 (Coincidence signal from timer/event counter)	
IRQ4	32	INTEIN (Falling signal of CI and $\overline{TO}$ counter)	Int/Ext
		$\overline{INTAD}$ (A/D converter interrupt)	
IRQ5	40	INTSR (Serial receive interrupt)	Int
		INST (Serial send interrupt)	

Figure 4. A/D Converter Block Diagram



Universal Serial Interface

The serial interface can operate in one of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first, for easy interfacing to certain NEC peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception: search and nonsearch. In the search mode, data is transferred one bit at a time from the serial register to the receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from the serial register to the transmit buffer occurs eight bits at a time. Figure 6 shows the universal serial interface block diagram.

Figure 5. Interrupt Structure Block Diagram

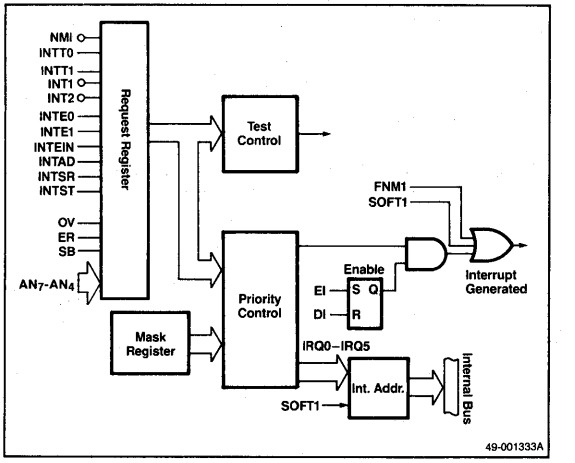
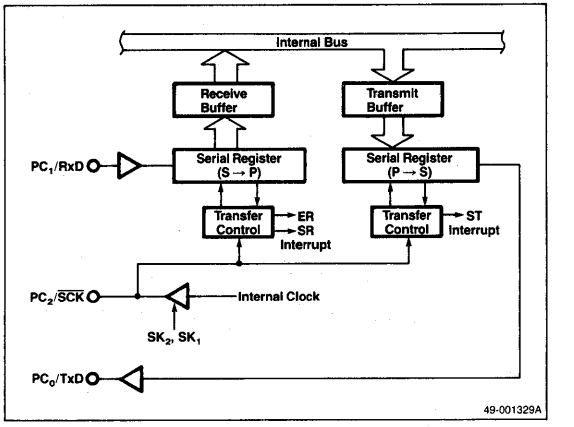


Figure 6. Universal Signal Interface Block Diagram



Zero-Crossing Detector

The INT1 and $\overline{INT2}$ terminals (used common to TI and PC_3) can detect the zero-crossing point of low-frequency AC signals. When driven directly, these pins respond as a normal digital input. Figure 7 shows the zero-crossing detection circuitry.

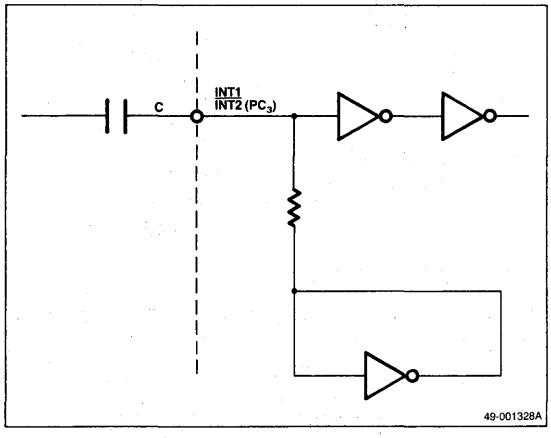
The zero-crossing detection capability allows you to make the 50-60 Hz power signal the basis for system timing and to control voltage phase sensitive devices.

To use the zero-cross detection mode, an AC signal of approximately 1-3 V AC (peak-to-peak) and a maximum frequency of 1 kHz is coupled through an external capacitor to the INT1 and $\overline{INT2}$ pins.

For the INT1 pin, the internal digital state is sensed as a 0 until the rising edge crosses the average DC level, when it becomes a 1 and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a 1 until the falling edge crosses the average DC level, when it becomes a 0 and $\overline{INT2}$ interrupt is generated.

Figure 7. Zero-Crossing Detection Circuit



Absolute Maximum Ratings

Power supply voltages,	V_{CC}	−0.5 V to +7.0 V
	V_{DD}	−0.5 V to +7.0 V
	AV_{CC}	−0.5 V to +7.0 V
	AV_{SS}	−0.5 V to +0.5 V
Input voltage, V_I		−0.5 V to +7.0 V
Output voltage, V_O		−0.5 V to +7.0 V
Reference input voltage, V_{AREF}		−0.5 V to V_{CC} V
Output current low, I_{OL}		
All outputs		4.0 mA
Total, all outputs		100 mA
Output current high, I_{OH}		
All outputs		−0.5 mA
Total, all outputs		−20 mA
Operating temperature, T_{OPR} $f_{XTAL} \leq 15$ MHz		−10°C to +70°C
Storage temperature, T_{STG}		−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

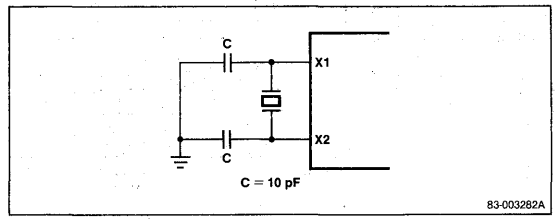
Oscillating Frequency	T_A	V_{CC}, AV_{CC}
$f_{XTAL} \leq 15$ MHz	−10°C to +70°C	+5.0 V ± 10%

Capacitance

T_A =25°C; $V_{CC} = V_{DD} = V_{SS} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Capacitance	C_I			10	pF	f_c = 1 MHz. Unmeasured pins returned to 0 V.
Output capacitance	C_O			20	pF	
I/O capacitance	C_{IO}			20	pF	

Recommended XTAL Oscillation Circuit



DC Characteristics

$T_A = -10°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$; $V_{SS} = 0\ V$; $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage	V_{IL}	0		0.8	V	
Input high voltage	V_{IH1}	2.0		V_{CC}	V	All except $\overline{SCK}$, $\overline{RESET}$, and X1
	V_{IH2}	0.8 V_{CC}		V_{CC}	V	$\overline{SCK}$, X1(1)
	V_{IH3}	0.8 V_{DD}		V_{CC}	V	$\overline{RESET}$
Output low voltage	V_{OL}			0.45	V	$I_{OL} = 2.0\ mA$
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -200\ \mu A$
Data retention voltage	V_{DDD}	3.2			V	$V_{CC} = 0\ V$; $\overline{RESET} = V_{IL}$
Input current	I_I			±200	μA	INT1, TI(PC_3); $+0.45\ V \leq V_I < V_{CC}$
Input leakage current	I_{LI}			±10	μA	All except INT1, TI(PC_3) $0\ V \leq V_I \leq V_{CC}$
Output leakage current	I_{LO}			±10	μA	$+0.45\ V \leq V_O \leq V_{CC}$
AV_{CC} supply current	AI_{CC}		6	12	mA	
V_{DD} supply current	I_{DD}		1.5	3.2	mA	$T_A = +25°C$; $V_{CC} = V_{DD} = 5\ V$
V_{CC} supply current	I_{CC}		150	200	mA	$T_A = +25°C$; $V_{CC} = V_{DD} = 5\ V$

Note:

(1) For XTAL oscillation, see the recommended circuit.

External Clock Timing

$T_A = -10°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 10\%$; $V_{SS} = 0\ V$; $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
X1 input width high	$t_{\Phi H}$	20		250	ns	
X1 input width low	$t_{\Phi L}$	20		250	ns	
X1 input rise time	t_r	0		20	ns	
X1 input fall time	t_f	0		20	ns	

AC Characteristics

Read/Write Operation

$T_A = -10°C$ to $+70°C$, $V_{CC} = +5.0\ V \pm 10\%$, $V_{SS} = -0\ V$, $V_{CC} - 0.8\ V \leqq V_{DD} \leqq V_{CC}$

Parameter	Symbol	Limits Min	Max	Unit	Conditions
X1 input cycle time	t_{CYC}	66	250	ns	
$\overline{RD}\downarrow$ to address floating	t_{AFR}		20	ns	Load capacitance: $C_L = 150\ pF$
Data hold after $\overline{RD}\uparrow$	t_{RDH}	0		ns	
$\overline{WR}\downarrow$ to data output	t_{WD}		100	ns	
Address setup to ALE↓	t_{AL}	30		ns	$f_{XTAL} = 15\ MHz$
Address hold after ALE↓	t_{LA}	35		ns	
Address to $\overline{RD}\downarrow$ delay time	t_{AR}	100		ns	
Address to data input	t_{AD}		250	ns	
ALE↓ to data input	t_{LDR}		135	ns	
$\overline{RD}\downarrow$ to data input	t_{RD}		120	ns	
ALE to $\overline{RD}\downarrow$ delay time	t_{LR}	15		ns	
ALE to $\overline{WR}\downarrow$ delay time	t_{LW}	15		ns	
Data setup time to $\overline{WR}\uparrow$	t_{DW}	165		ns	
Data hold time after $\overline{WR}\uparrow$	t_{WDH}	60		ns	
$\overline{WR}\uparrow$ to ALE↑ delay time	t_{WL}	80		ns	
$\overline{WR}$ width low	t_{WW}	215		ns	
$\overline{RD}\uparrow$ to ALE↑ delay time	t_{RL}	80		ns	
RD width low	t_{RR}	215		ns	Data read, $f_{XTAL} = 15\ MHz$; $C_L = 150\ pF$
		415		ns	OP code fetch, $f_{XTAL} = 15\ MHz$; $C_L = 150\ pF$
ALE width high	t_{LL}	90		ns	$f_{XTAL} = 15\ MHz$ Load capacitance = 150 pF
Address to $\overline{WR}\downarrow$ delay	t_{AW}	100		ns	
ALE↓ to data output	t_{LDW}		180	ns	
$\overline{M1}$ setup time to ALE↓	t_{ML}	30		ns	
$\overline{M1}$ hold time after ALE↓	t_{LM}	35		ns	
$\overline{IO}/M$ setup time to ALE↓	t_{IL}	30		ns	
$\overline{IO}/M$ hold time after ALE↓	t_{LI}	35		ns	

4

Serial Operation

Parameter	Symbol	Limits Min	Limits Max	Unit	Conditions
$\overline{SCK}$ cycle time	t_{CYK}	800		ns	$\overline{SCK}$ input (1)
		500		ns	$\overline{SCK}$ input (2)
		1.6		μs	$\overline{SCK}$ output
$\overline{SCK}$ width low	t_{KKL}	335		ns	$\overline{SCK}$ input (1)
		200		ns	$\overline{SCK}$ input (2)
		700		ns	$\overline{SCK}$ output
$\overline{SCK}$ width high	t_{KKH}	335		ns	$\overline{SCK}$ input (1)
		200		ns	$\overline{SCK}$ input (2)
		700		ns	$\overline{SCK}$ output
RxD set-up time to $\overline{SCK}$ ↑	t_{RXK}	80		ns	(1)
RxD hold time after $\overline{SCK}$ ↑	t_{KRX}	80		ns	(1)
$\overline{SCK}$ ↓ TxD delay time	t_{KTX}		210	ns	(1)

Note:

(1) 1x clock rate in asynchronous, synchronous, or I/O interface mode.

(2) 16x, 64x clock rate in asynchronous mode.

A/D Converter Characteristics

$T_A = 0$ to $+70°C$; $V_{CC} = AV_{CC} = +5.0\ V \pm 10\%$; $V_{SS} = AV_{SS} = 0\ V$; $AV_{CC} - 0.5\ V \leq V_{AREF} \leq AV_{CC}$

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Conditions
Resolution		8			bits	
Absolute accuracy				0.8% ± 1/2	LSB	$T_A = -10$ to $+150°C$, 66 ns ≤ t_{CYC} ≤ 170 ns
Conversion time	t_{CONV}	576			t_{CYC}	66 ns ≤ t_{CYC} ≤ 110 ns
		432			t_{CYC}	110 ns ≤ t_{CYC} ≤ 170 ns
Sampling time	t_{SAMP}	96			t_{CYC}	66 ns ≤ t_{CYC} ≤ 110 ns
		72			t_{CYC}	110 ns ≤ t_{CYC} ≤ 170 ns
Analog input voltage	V_{IA}	0		V_{AREF}	V	
Analog resistance	R_{AN}		1000		MΩ	
Analog reference current	I_{AREF}	0.2	0.5	1.5	mA	

Zero-Cross Characteristics

$T_A = -10$ to $+70°C$, $V_{CC} = +5.0\ V \pm 10\%$, $V_{SS} = 0\ V$, $V_{CC} - 8\ V \leq V_{DD} \leq V_{CC}$

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Zero-cross detection input	V_{ZX}	1	1.8	VAC_{P-P}	AC coupled
Zero-cross accuracy	A_{ZX}		±135	mV	60 Hz sine wave
Zero-cross detection input frequency	f_{ZX}	0.05	1	kHz	

Bus Timing Depending on t_{CYC}

Symbol	Calculating Expression	Min/Max
t_{AL}	2T − 100	Min
t_{LA}	T − 30	Min
t_{AR}	3T − 100	Min
t_{AD}	7T − 220	Max
t_{LDR}	5T − 200	Max
t_{RD}	4T − 150	Max
t_{LR}	T − 50	Min
t_{RL}	2T − 50	Min
t_{RR}	4T − 50 (Data Read)	Min
	7T − 50 (Opcode Fetch)	
t_{LL}	2T − 40	Min
t_{ML}	2T − 100	Min
t_{LM}	T − 30	Min
t_{IL}	2T − 100	Min
t_{LI}	T − 30	Min
t_{AW}	3T −100	Min
t_{LDW}	T + 110	Max
t_{LW}	T − 50	Min
t_{DW}	4T − 100	Min
t_{WDH}	2T − 70	Min
t_{WL}	2T − 50	Min
t_{WW}	4T − 50	Min
t_{CYK}	12T ($\overline{SCK}$ input)(1)	Min
	24T ($\overline{SCK}$ output)	
t_{KKL}	5T + 5 ($\overline{SCK}$ input)(1)	Min
	12T − 100 ($\overline{SCK}$ output)	
t_{KKH}	5T + 5 ($\overline{SCK}$ input)(1)	Min
	12T − 100 ($\overline{SCK}$ output)	

Note:

(1) 1x clock rate in asynchronous, synchronous, or I/O interface mode.

(2) $T = t_{CYC} = 1/f_{XTAL}$.

(3) The items not included in this list are independent of oscillator frequency (f_{XTAL}).

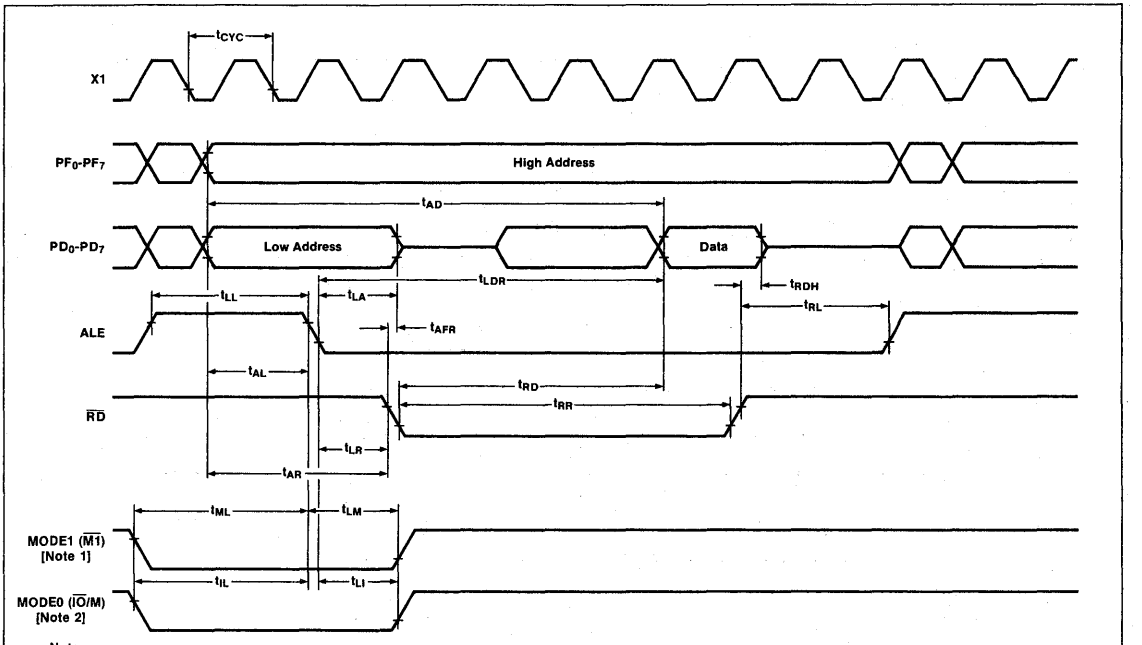
Other Operations

$T_A = -10$ to $+70$ °C, $V_{CC} = +5.0$ V ± 10%, $V_{SS} = 0$ V, $V_{CC} - 0.8$ V ≦ V_{DD} ≦ V_{CC}

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
TI width high, low	t_{TIH}, t_{TIL}	6		t_{CYC}	
	t_{CI1H}, t_{CI1L}	6		t_{CYC}	Event count mode
CI width high, low	t_{CI2H}, t_{CI2L}	48		t_{CYC}	Pulse width measurement mode
$\overline{NMI}$ width high, low	t_{NIH}, t_{NIL}	36		t_{CYC}	
INT1 width high, low	t_{I1H}, t_{I1L}	36		t_{CYC}	
$\overline{INT2}$ width high, low	t_{I2H}, t_{I2L}	36		t_{CYC}	
$\overline{RESET}$ width high, low	t_{RSH}, t_{RSL}	60		t_{CYC}	

Timing Waveforms

Read Operation



Note:

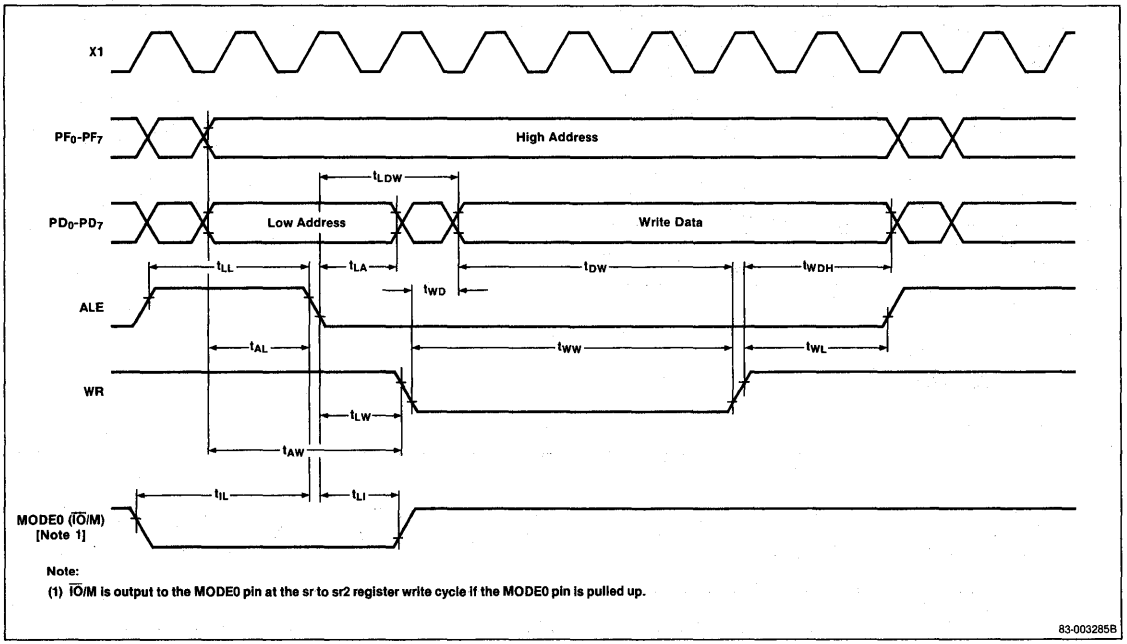
[1] M1 is output to the MODE1 pin at the first opcode fetch cycle if the MODE 1 pin is pulled up.

[2] IO/M is output to the MODE0 pin at the sr to sr2 register read cycle if the MODE0 pin is pulled up.

83-003284B

Timing Waveforms (cont)

Write Operation



Note:

(1) $\overline{IO}/M$ is output to the MODE0 pin at the sr to sr2 register write cycle if the MODE0 pin is pulled up.

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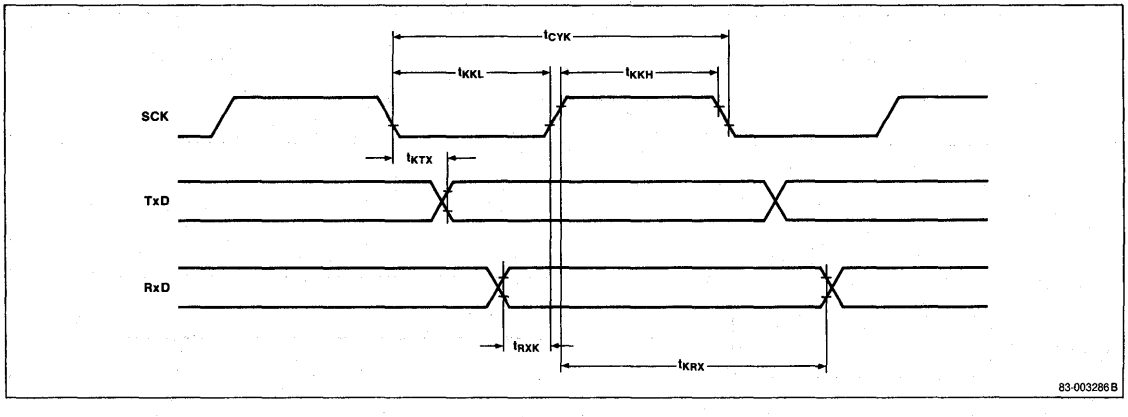
Serial Operation



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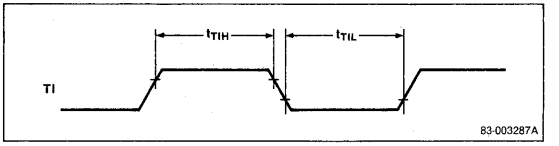
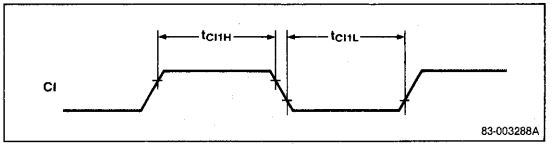
Timing Waveforms (cont)

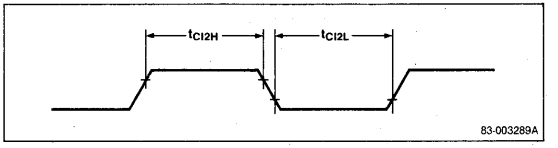
Timer Input Timing



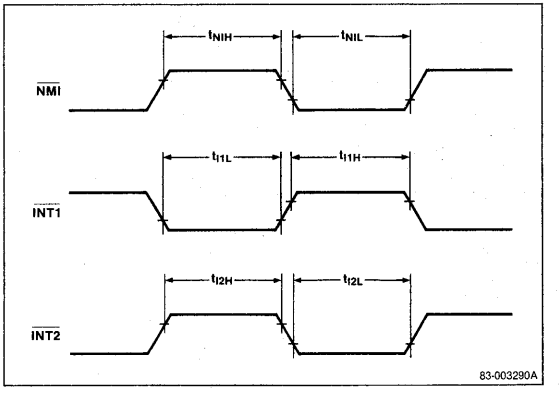
Timer/Event Counter Input Timing: Event Counter Mode



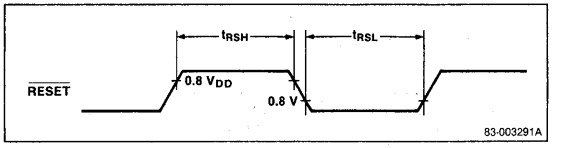
Timer/Event Counter Input Timing: Pulse Width Measurement Mode



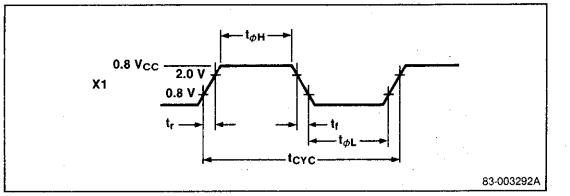
Interrupt Input Timing



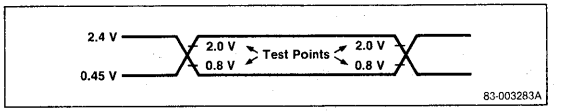
RESET Input Timing



External Clock Timing



AC Timing Test Points



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Instruction Set

Operand Format/Description

Format	Description
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC, MF, TxB, TM_0, TM_1
sr1	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RXB, CR0, CR1, CR2, CR3
sr2	PA, PB, PC, PD, PF, MKH, ANM, MKL, SMH, EOM, TMM
sr3	ETM_0, ETM_1
sr4	ECNT, ECPT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D−, H−
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D−, H−, D + byte, H + A, H + B, H + EA, H + byte
rpa3	D, H, D++, H++, D + byte, H + A, H + B, H + EA, H + byte
wa	8-Bit immediate data
word	16-Bit immediate data
byte	8-Bit immediate data
bit	3-Bit immediate data
f	CY, HC, Z
irf	FNMI, FT0, FT1, F1, F2, FE0, FE1, FEIN, FAD, FSR, FST, ER, 0V, AN_4, AN_5, AN_6, AN_7, SB

Instruction Set Symbol Definitions

Symbol	Description
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
∀	Exclusive OR
—	Complement
•	Concatenation

Remarks

1. sr-sr4 (special register)

PA = Port A
PB = Port B
PC = Port C
PD = Port D
PF = Port F
MA = Mode A
MB = Mode B
MC = Mode C
MCC = Mode Control C
MF = Mode F

MM = Memory Mapping
TM_0 = Timer Register 0
TM_1 = Timer Register 1
TMM = Timer Mode
ETM_0 = Timer/Event Counter Register 0
ETM_1 = Timer/Event Counter Register 1

ECNT = Timer/Event Counter Upcounter
ECPT = Timer/Event Counter Capture

ETMM = Timer/Event Counter Mode
EOM = Timer/Event Counter Output Mode

TxB = TX Buffer
RxB = RX Buffer
SMH = Serial Mode High
SML = Serial Mode Low
MKH = Mask High
MKL = Mask Low
ANM = A/D Channel Mode
CR_0 = A/D Conversion Result 0-3 to CR_3

2. rp-rp3 (register pair)

SP = Stack Pointer
B = BC
D = DE
H = HL
V = VA
EA = Extended Accumulator

3. rpa-rpa3 (rp addressing)

B = (BC)
D = (DE)
H = (HL)
D+ = (DE) +
H− = (HL) +
D− = (DE) −
H− = (HL) −
D++ = (DE) ++
H++ = (HL) ++
D + byte = (DE) + byte
H + A = (HL) + (A)
H + B = (HL) + (B)
H + EA = (HL) + (EA)
H + byte = (HL) + byte

4. f (flag)

CY = Carry
HC = Half Carry
Z = Zero

5. irf (interrupt flag)

NMI = NMI* Input
FT0 = INTFT0
FT1 = INTFT1
F1 = INTF1
F2 = INTF2
FE0 = INTFE0
FE1 = INTFE1
FEIN = INTFEIN
FAD = INTFAD
FSR = INTFSR
FST = INTFST
ER = Error
0V = Overflow
AN_4 to AN_7 = Analog Input 4-7
SB = Standby

Instruction Set

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
8-Bit Data Transfer																					
MOV	r1,A	(r1) ← (A)	0	0	0	1	1	T_2	T_1	T_0									4	1	
	A, r1	(A) ← (r1)	0	0	0	0	1	T_2	T_1	T_0									4	1	
	*sr,A	(sr) ← (A)	0	1	0	0	1	1	0	1	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	*A,sr1	(A) ← (sr1)	0	1	0	0	1	1	0	0	1	1	S_5	S_4	S_3	S_2	S_1	S_0	10	2	
	r,word	(r) ← (word)	0	1	1	1	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
	word,r	(word) ← (r)	0	1	1	1	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	17	4	
			Low addr								High addr										
MVI	*r,byte	(r) ← byte set L1 if r = A set L0 if r = L	0	1	1	0	1	R_2	R_1	R_0	Data								7	2	L1 = 1 and r = A L0 = 1 and r = L
	sr2,byte	(sr2) ← byte	0	1	1	0	0	1	0	0	S_3	0	0	0	0	S_2	S_1	S_0	14	3	
			Data																		
MVIW	*wa, byte	((V)•(wa)) ← byte	0	1	1	1	0	0	0	1	Offset								13	3	
			Data																		
MVIX	*rpa1,byte	(rpa1) ← byte	0	1	0	0	1	0	A_1	A_0	Data								10	2	
STAW	*wa	((V)•(wa)) ← A	0	1	1	0	0	0	1	1	Offset								10	2	
LDAW	*wa	(A) ← ((V)•(wa))	0	0	0	0	0	0	0	1	Offset								10	2	
STAX	*rpa2	(rpa2) ← (A)	A_3	0	1	1	1	A_2	A_1	A_0	Data (2)								7/13(3)	2	
LDAX	*rpa2	(A) ← ((rpa2))	A_3	0	1	0	1	A_2	A_1	A_0	Data (2)								7/13(3)	2	
EXX		(B) ↔ (B'),(C) ↔ (C'),(D) ↔ (D') (E) ↔ (E'),(H) ↔ (H'),(L) ↔ (L')	0	0	0	1	0	0	0	1									4	1	
EXA		(V) ↔ (V'),(A) ↔ (A'),(EA) ↔ (EA')	0	0	0	1	0	0	0	0									4	1	
EXH		(H) ↔ (H'),(L) ↔ (L')	0	1	0	1	0	0	0	0									4	1	
16-Bit Data Transfer																					
BLOCK	D	((DE)) ← ((HL)),(DE) ← (DE + 1), (HL) ← (HL) + 1, (C) ← (C) − 1 End if borrow	0	0	1	1	0	0	0	1									13 x (C + 1)	1	
DMOV	rp3, EA	($rp3_L$) ← (EAL),($rp3_H$) ← (EAH)	1	0	1	1	0	1	P_1	P_0									4	1	
	EA,rp3	(EAL) ← ($rp3_L$),(EAH) ← ($rp3_H$)	1	0	1	0	0	1	P_1	P_0									4	1	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code																State(1)	Bytes	Skip Condition
			B1 / B3								B2 / B4										
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
16-Bit Data Transfer (cont)																					
DMOV	sr3, EA	(sr3) ← (EA)	0	1	0	0	1	0	0	0	1	1	0	1	0	0	1	U_0	14	2	
	EA,sr4	(EA) ← (sr4)	0	1	0	0	1	0	0	0	1	1	0	0	0	0	V_1	V_0	14	2	
SBCD	word	(word) ← (C), (word + 1) ← (B)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	0	20	4	
			Low addr								High addr										
SDED	word	(word) ← (E), (word + 1) ← (D)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	0	20	4	
			Low addr								High addr										
SHLD	word	(word) ← (L), (word + 1) ← (H)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	20	4	
			Low addr								High addr										
SSPD	word	(word) ← (SP_L),(word + 1) ← (SP_H)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	20	4	
			Low addr								High addr										
STEAX	rpa3	((rpa3)) ← (EAL),((rpa3) + 1 ← (EAH)	0	1	0	0	1	0	0	0	1	0	0	1	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
LBCD	word	(C) ← (word),(B) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	0	1	1	1	1	1	20	4	
			Low addr								High addr										
LDED	word	(E) ← (word),(D) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1	1	20	4	
			Low addr								High addr										
LHLD	word	(L) ← (word),(H) ← (word + 1)	0	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	20	4	
			Low addr								High addr										
LSPD	word	(SP_L) ← (word),(SP_H) ← ((word) + 1)	0	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	20	4	
			Low addr								High addr										
LDEAX	rpa3	(EAL) ← ((rpa3)),(EAH) ← ((rpa3) + 1)	0	1	0	0	1	0	0	0	1	0	0	0	C_3	C_2	C_1	C_0	14/20(3)	3	
			Data(4)																		
PUSH	rp1	((SP) − 1) ← ($rp1_H$) ((SP) − 2) ← ($rp1_L$) (SP) ← (SP) − 2	1	0	1	1	0	Q_2	Q_1	Q_0									13	1	
POP	rp1	($rp1_L$) ← ((SP)),($rp1_H$) ← ((SP) + 1) (SP) ← (SP) + 2	1	0	1	0	0	Q_2	Q_1	Q_0									10	1	
LXI	*rp2,word	(rp2) ← (word) set L0 if rp2 = H	0	P_2	P_1	P_0	0	1	0	0	Low byte								10	3	L0 = 1 and rp2 = H
			High byte																		
TABLE		(C) ← ((PC)+3+(A)),B ← ((PC)+3+(A)+ 1)	0	1	0	0	1	0	0	0	1	0	1	0	1	0	0	0	17	2	
8-Bit Arithmetic [Register]																					
ADD	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	1	0	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	1	0	0	0	R_2	R_1	R_0	8	2	
ADC	A,r	(A) ← (A) + (r) + (CY)	0	1	1	0	0	0	0	0	1	1	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) + (A) + (CY)	0	1	1	0	0	0	0	0	0	1	0	1	0	R_2	R_1	R_0	8	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1/B3 7	6	5	4	3	2	1	0	B2/B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
8-Bit Arithmetic [Register] (cont)																					
ADDNC	A,r	(A) ← (A) + (r)	0	1	1	0	0	0	0	0	1	0	1	0	0	R_2	R_1	R_0	8	2	No carry
	r,A	(r) ← (r) + (A)	0	1	1	0	0	0	0	0	0	0	1	0	0	R_2	R_1	R_0	8	2	No carry
SUB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	0	R_2	R_1	R_0	8	2	
SBB	A,r	(A) ← (A) − (r) − (CY)	0	1	1	0	0	0	0	0	1	1	1	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) − (A) − (CY)	0	1	1	0	0	0	0	0	0	1	1	1	0	R_2	R_1	R_0	8	2	
SUBNB	A,r	(A) ← (A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) ← (r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	0	R_2	R_1	R_0	8	2	No borrow
ANA	A,r	(A) ← (A) ∧ (r)	0	1	1	0	0	0	0	0	1	0	0	0	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) ∧ (A)	0	1	1	0	0	0	0	0	0	0	0	0	1	R_2	R_1	R_0	8	2	
ORA	A,r	(A) ← (A) V (r)	0	1	1	0	0	0	0	0	1	0	0	1	1	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) V (A)	0	1	1	0	0	0	0	0	0	0	0	1	1	R_2	R_1	R_0	8	2	
XRA	A,r	(A) ← (A) V (r)	0	1	1	0	0	0	0	0	1	0	0	1	0	R_2	R_1	R_0	8	2	
	r,A	(r) ← (r) V (A)	0	1	1	0	0	0	0	0	0	0	0	1	0	R_2	R_1	R_0	8	2	
GTA	A,r	(A) − (r) − 1	0	1	1	0	0	0	0	0	1	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
	r,A	(r) − (A) − 1	0	1	1	0	0	0	0	0	0	0	1	0	1	R_2	R_1	R_0	8	2	No borrow
LTA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	0	1	1	1	R_2	R_1	R_0	8	2	Borrow
NEA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	0	1	R_2	R_1	R_0	8	2	No zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	0	1	R_2	R_1	R_0	8	2	No zero
EQA	A,r	(A) − (r)	0	1	1	0	0	0	0	0	1	1	1	1	1	R_2	R_1	R_0	8	2	Zero
	r,A	(r) − (A)	0	1	1	0	0	0	0	0	0	1	1	1	1	R_2	R_1	R_0	8	2	Zero
ONA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	0	1	R_2	R_1	R_0	8	2	No zero
OFFA	A,r	(A) ∧ (r)	0	1	1	0	0	0	0	0	1	1	0	1	1	R_2	R_1	R_0	8	2	Zero
8-Bit Arithmetic (Memory)																					
ADDX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	0	A_2	A_1	A_0	11	2	
ADCX	rpa	(A) ← (A) + ((rpa)) + (CY)	0	1	1	1	0	0	0	0	1	1	0	1	0	A_2	A_1	A_0	11	2	
ADDNCX	rpa	(A) ← (A) + ((rpa))	0	1	1	1	0	0	0	0	1	0	1	0	0	A_2	A_1	A_0	11	2	No carry
SUBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	0	A_2	A_1	A_0	11	2	
SBBX	rpa	(A) ← (A) − ((rpa)) − (CY)	0	1	1	1	0	0	0	0	1	1	1	1	0	A_2	A_1	A_0	11	2	
SUBNBX	rpa	(A) ← (A) − ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	0	A_2	A_1	A_0	11	2	No borrow
ANAX	rpa	(A) ← (A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	0	0	0	1	A_2	A_1	A_0	11	2	
ORAX	rpa	(A) ← (A) V ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	1	A_2	A_1	A_0	11	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 / B3								Operation Code B2 / B4								State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
8-Bit Arithmetic (Memory) (cont)																					
XRAX	rpa	(A) ← (A) V ((rpa))	0	1	1	1	0	0	0	0	1	0	0	1	0	A_2	A_1	A_0	11	2	
GTAX	rpa	(A) – ((rpa)) – 1	0	1	1	1	0	0	0	0	1	0	1	0	1	A_2	A_1	A_0	11	2	No borrow
LTAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	0	1	1	1	A_2	A_1	A_0	11	2	Borrow
NEAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	0	1	A_2	A_1	A_0	11	2	No zero
EQAX	rpa	(A) – ((rpa))	0	1	1	1	0	0	0	0	1	1	1	1	1	A_2	A_1	A_0	11	2	Zero
ONAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	0	1	A_2	A_1	A_0	11	2	No zero
OFFAX	rpa	(A) ∧ ((rpa))	0	1	1	1	0	0	0	0	1	1	0	1	1	A_2	A_1	A_0	11	2	Zero
Immediate Data																					
ADI	*A,byte	(A) ← (A) + byte	0	1	0	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	1	0	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2, byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	1	0	0	0	S_2	S_1	S_0	20	3	
			Data																		
ACI	*A,byte	(A) ← (A) + byte + (CY)	0	1	0	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) + byte + (CY)	0	1	1	1	0	1	0	0	0	1	0	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte + (CY)	0	1	1	0	0	1	0	0	S_3	1	0	1	0	S_2	S_1	S_0	20	3	
			Data																		
ADINC	*A,byte	(A) ← (A) + byte	0	0	1	0	0	1	1	0	Data								7	2	No carry
	r,byte	(r) ← (r) + byte	0	1	1	1	0	1	0	0	0	0	1	0	0	R_2	R_1	R_0	11	3	No carry
			Data																		
	sr2,byte	(sr2) ← (sr2) + byte	0	1	1	0	0	1	0	0	S_3	0	1	0	0	S_2	S_1	S_0	20	3	No carry
			Data																		
SUI	*A,byte	(A) ← (A) – byte	0	1	1	0	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte	0	1	1	1	0	1	0	0	0	1	1	0	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte	0	1	1	0	0	1	0	0	S_3	1	1	0	0	S_2	S_1	S_0	20	3	
			Data																		
SBI	*A,byte	(A) ← (A) – byte – (CY)	0	1	1	1	0	1	1	0	Data								7	2	
	r,byte	(r) ← (r) – byte – (CY)	0	1	1	1	0	1	0	0	0	1	1	1	0	R_2	R_1	R_0	11	3	
			Data																		
	sr2,byte	(sr2) ← (sr2) – byte – (CY)	0	1	1	0	0	1	0	0	S_3	1	1	1	0	S_2	S_1	S_0	20	3	
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1				B3				B2				B4				State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
Immediate Data (cont)																					
SUINB	*A,byte	(A) ← (A) − byte	0	0	1	1	0	1	1	0					Data				7	2	No borrow
	r,byte	(r) ← (r) − byte	0	1	1	1	0	1	0	0	0	0	1	1	0	R_2	R_1	R_0	11	3	No borrow
							Data														
	sr2,byte	(sr2) ← (sr2) − byte	0	1	1	0	0	1	0	0	S_3	0	1	1	0	S_2	S_1	S_0	20	3	No borrow
							Data														
ANI	*A,byte	(A) ← (A) ∧ byte	0	0	0	0	0	1	1	1					Data				7	2	
	r,byte	(r) ← (r) ∧ byte	0	1	1	1	0	1	0	0	0	0	0	0	1	R_2	R_1	R_0	11	3	
							Data														
	sr2,byte	(sr2) ← (sr2) ∧ byte	0	1	1	0	0	1	0	0	S_3	0	0	0	1	S_2	S_1	S_0	20	3	
							Data														
ORI	*A,byte	(A) ← (A) V byte	0	0	0	1	0	1	1	1					Data				7	2	
	r,byte	(r) ← (r) V byte	0	1	1	1	0	1	0	0	0	0	0	1	1	R_2	R_1	R_0	11	3	
							Data														
	sr2,byte	(sr2) ← (sr2) V byte	0	1	1	0	0	1	0	0	S_3	0	0	1	1	S_2	S_1	S_0	20	3	
							Data														
XRI	*A,byte	(A) ← (A) V byte	0	0	0	1	0	1	1	0					Data				7	2	
	r,byte	(r) ← (r) V byte	0	1	1	1	0	1	0	0	0	0	0	1	0	R_2	R_1	R_0	11	3	
							Data														
	sr2,byte	(sr2) ← (sr2) V byte	0	1	1	0	0	1	0	0	S_3	0	0	1	0	S_2	S_1	S_0	20	3	
							Data														
GTI	*A,byte	(A) − byte − 1	0	0	1	0	0	1	1	1					Data				7	2	No borrow
	r,byte	(r) − byte − 1	0	1	1	1	0	1	0	0	0	0	1	0	1	R_2	R_1	R_0	11	3	No borrow
							Data														
	sr2,byte	(sr2) − byte − 1	0	1	1	0	0	1	0	0	S_3	0	1	0	1	S_2	S_1	S_0	14	3	No borrow
							Data														
LTI	*A,byte	(A) − byte	0	0	1	1	0	1	1	1					Data				7	2	Borrow
	r,byte	(r) − byte	0	1	1	1	0	1	0	0	0	0	1	1	1	R_2	R_1	R_0	11	3	Borrow
							Data														
	sr2,byte	(sr2) − byte	0	1	1	0	0	1	0	0	S_3	0	1	1	1	S_2	S_1	S_0	14	3	Borrow
							Data														
NEI	*A,byte	(A) − byte	0	1	1	0	0	1	1	1					Data				7	2	No zero
	r,byte	(r) − byte	0	1	1	1	0	1	0	0	0	1	1	0	1	R_2	R_1	R_0	11	3	No zero
							Data														

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 B3	7	6	5	4	3	2	1	0	B2 B4	7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Immediate Data (cont)																							
NEI	sr2,byte	(sr2) – byte		0	1	1	0	0	1	0	0		S_3	1	1	0	1	S_2	S_1	S_0	14	3	No zero
			Data																				
EQI	*A,byte	(A) – byte		0	1	1	1	0	1	1	1						Data				7	2	Zero
	r,byte	(r) – byte		0	1	1	1	0	1	0	0		0	1	1	1	1	R_2	R_1	R_0	11	3	Zero
			Data																				
	sr2,byte	(sr2) – byte		0	1	1	0	0	1	0	0		S_3	1	1	1	1	S_2	S_1	S_0	14	3	Zero
			Data																				
ONI	*A,byte	(A) ∧ byte		0	1	0	0	0	1	1	1						Data				7	2	No zero
	r,byte	(r) ∧ byte		0	1	1	1	0	1	0	0		0	1	0	0	1	R_2	R_1	R_0	11	3	No zero
			Data																				
	sr2,byte	(sr2) ∧ byte		0	1	1	0	0	1	0	0		S_3	1	0	0	1	S_2	S_1	S_0	14	3	No zero
			Data																				
OFFI	*A,byte	(A) ∧ byte		0	1	0	1	0	1	1	1						Data				7	2	Zero
	r,byte	(r) ∧ byte		0	1	1	1	0	1	0	0		0	1	0	1	1	R_2	R_1	R_0	11	3	Zero
			Data																				
	sr2,byte	(sr2) ∧ byte		0	1	1	0	0	1	0	0		S_3	1	0	1	1	S_2	S_1	S_0	14	3	Zero
			Data																				
Working Register																							
ADDW	wa	(A) ← (A) + ((V)•(wa))		0	1	1	1	0	1	0	0		1	1	0	0	0	0	0	0	14	3	
			Offset																				
ADCW	wa	(A) ← (A) + ((V)•(wa)) + (CY)		0	1	1	1	0	1	0	0		1	1	0	1	0	0	0	0	14	3	
			Offset																				
ADDNCW	wa	(A) ← (A) + ((V)•(wa))		0	1	1	1	0	1	0	0		1	0	1	0	0	0	0	0	14	3	No carry
			Offset																				
SUBW	wa	(A) ← (A) – ((V)•(wa))		0	1	1	1	0	1	0	0		1	1	1	0	0	0	0	0	14	3	
			Offset																				
SBBW	wa	(A) ← (A) – ((V)•(wa)) – (CY)		0	1	1	1	0	1	0	0		1	1	1	1	0	0	0	0	14	3	
			Offset																				
SUBNBW	wa	(A) ← (A) – ((V)•(wa))		0	1	1	1	0	1	0	0		1	0	1	1	0	0	0	0	14	3	No borrow
			Offset																				
ANAW	wa	(A) ← (A) ∧ ((V)•(wa))		0	1	1	1	0	1	0	0		1	0	0	0	1	0	0	0	14	3	
			Offset																				

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 B3 7	6	5	4	3	2	1	0	Operation Code B2 B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Working Register (cont)																					
ORAW	wa	(A) ← (A) V ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0	14	3	
			Offset																		
XRAW	wa	(A) ← (A) V ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	0	1	0	0	0	0	14	3	
			Offset																		
GTAW	wa	(A) – ((V)•(wa)) – 1	0	1	1	1	0	1	0	0	1	0	1	0	1	0	0	0	14	3	No borrow
			Offset																		
LTAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	0	1	1	1	0	0	0	14	3	Borrow
			Offset																		
NEAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	0	1	0	0	0	14	3	No zero
			Offset																		
EQAW	wa	(A) – ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	1	1	1	0	0	0	14	3	Zero
			Offset																		
ONAW	wa	(A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	0	1	0	0	0	14	3	No zero
			Offset																		
OFFAW	wa	(A) ∧ ((V)•(wa))	0	1	1	1	0	1	0	0	1	1	0	1	0	0	0	0	14	3	Zero
			Offset																		
ANIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) ∧ byte	0	0	0	0	0	1	0	1					Offset				19	3	
			Data																		
ORIW	*wa,byte	((V)•(wa)) ← ((V)•(wa)) V byte	0	0	0	1	0	1	0	1					Offset				19	3	
			Data																		
GTIW	*wa,byte	((V)•(wa)) – byte – 1	0	0	1	0	0	1	0	1					Offset				13	3	No borrow
			Data																		
LTIW	*wa,byte	((V)•(wa)) – byte	0	0	1	1	0	1	0	1					Offset				13	3	Borrow
			Data																		
NEIW	*wa,byte	((V)•(wa)) – byte	0	1	1	0	0	1	0	1					Offset				13	3	No zero
			Data																		
EQIW	*wa,byte	((V)•(wa)) – byte	0	1	1	1	0	1	0	1					Offset				13	3	Zero
			Data																		
ONIW	*wa,byte	((V)•(wa)) ∧ byte	0	1	0	0	0	1	0	1					Offset				13	3	No zero
			Data																		
OFFIW	*wa,byte	((V)•(wa)) ∧ byte	0	1	0	1	0	1	0	1					Offset				13	3	Zero
			Data																		

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code 7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
						B1	B3							B2	B4						
16-Bit Arithmetic																					
EADD	EA,r2	(EA) ← (EA) + (r2)	0	1	1	1	0	0	0	0	0	1	0	0	0	0	R_1	R_0	11	2	
DADD	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	0	1	P_1	P_0	11	2	
DADC	EA,rp3	(EA) ← (EA) + (rp3) + (CY)	0	1	1	1	0	1	0	0	1	1	0	1	0	1	P_1	P_0	11	2	
DADDNC	EA,rp3	(EA) ← (EA) + (rp3)	0	1	1	1	0	1	0	0	1	0	1	0	0	1	P_1	P_0	11	2	No carry
ESUB	EA,r2	(EA) ← (EA) − (r2)	0	1	1	1	0	0	0	0	0	1	1	0	0	0	R_1	R_0	11	2	
DSUB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	0	1	P_1	P_0	11	2	
DSBB	EA,rp3	(EA) ← (EA) − (rp3) − (CY)	0	1	1	1	0	1	0	0	1	1	1	1	0	1	P_1	P_0	11	2	
DSUBNB	EA,rp3	(EA) ← (EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	0	1	P_1	P_0	11	2	No borrow
DAN	EA,rp3	(EA) ← (EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	0	0	0	1	1	P_1	P_0	11	2	
DOR	EA,rp3	(EA) ← (EA) V (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	1	1	P_1	P_0	11	2	
DXR	EA,rp3	(EA) ← (EA) V (rp3)	0	1	1	1	0	1	0	0	1	0	0	1	0	1	P_1	P_0	11	2	
DGT	EA,rp3	(EA) − (rp3) − 1	0	1	1	1	0	1	0	0	1	0	1	0	1	1	P_1	P_0	11	2	No borrow
DLT	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	0	1	1	1	1	P_1	P_0	11	2	Borrow
DNE	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	0	1	1	P_1	P_0	11	2	No zero
DEQ	EA,rp3	(EA) − (rp3)	0	1	1	1	0	1	0	0	1	1	1	1	1	1	P_1	P_0	11	2	Zero
DON	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	0	1	1	P_1	P_0	11	2	No zero
DOFF	EA,rp3	(EA) ∧ (rp3)	0	1	1	1	0	1	0	0	1	1	0	1	1	1	P_1	P_0	11	2	Zero
Multiply/Divide																					
MUL	r2	(EA) ← (A) x (r2)	0	1	0	0	1	0	0	0	0	0	1	0	1	1	R_1	R_0	32	2	
DIV	r2	(EA) ← (EA) + (r2), (r2) ← Remainder	0	1	0	0	1	0	0	0	0	0	1	1	1	1	R_1	R_0	59	2	
Increment/Decrement																					
INR	r2	(r2) ← (r2) + 1	0	1	0	0	0	0	R_1	R_0									4	1	Carry
INRW	*wa	((V)•(wa)) ← ((V)•(wa)) + 1	0	0	1	0	0	0	0	0					Offset				16	2	Carry
INX	rp	(rp) ← (rp) + 1	0	0	P_1	P_0	0	0	1	0									7	1	
	EA	(EA) ← (EA) + 1	1	0	1	0	1	0	0	0									7	1	
DCR	r2	(r2) ← (r2) − 1	0	1	0	1	0	0	R_1	R_0									4	1	Borrow
DCRW	*wa	((V)•(wa)) ← ((V)•(wa)) − 1	0	0	1	1	0	0	0	0					Offset				16	2	Borrow
DCX	rp	(rp) ← (rp) − 1	0	0	P_1	P_0	0	0	1	1									7	1	
	EA	(EA) ← (EA) − 1	1	0	1	0	1	0	0	1									7	1	
Others																					
DAA		Decimal Adjust Accumulator	0	1	1	0	0	0	0	1									4	1	
STC		(CY) ← 1	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	1	8	2	
CLC		(CY) ← 0	0	1	0	0	1	0	0	0	0	0	1	0	1	0	1	0	8	2	

NEC

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code B1 B3 7	6	5	4	3	2	1	0	B2 B4 7	6	5	4	3	2	1	0	State(1)	Bytes	Skip Condition
Others (cont)																					
NEGA		(A) ← (A) + 1	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	0	8	2	
Rotate and Shift																					
RLD		Rotate left digit	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	0	17	2	
RRD		Rotate right digit	0	1	0	0	1	0	0	0	0	0	1	1	1	0	0	1	17	2	
RLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$, $(r2_0) \leftarrow (CY)$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	1	1	0	1	R_1	R_0	8	2	
RLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$,$(r2_7) \leftarrow (CY)$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	1	1	0	0	R_1	R_0	8	2	
SLL	r2	$(r2_{m+1}) \leftarrow (r2_m)$,$(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	1	0	0	1	R_1	R_0	8	2	
SLR	r2	$(r2_{m-1}) \leftarrow (r2_m)$,$(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	1	0	0	0	R_1	R_0	8	2	
SLLC	r2	$(r2_{m+1}) \leftarrow (r2_m)$,$(r2_0) \leftarrow 0$, $(CY) \leftarrow (r2_7)$	0	1	0	0	1	0	0	0	0	0	0	0	0	1	R_1	R_0	8	2	Carry
SLRC	r2	$(r2_{m-1}) \leftarrow (r2_m)$,$(r2_7) \leftarrow 0$, $(CY) \leftarrow (r2_0)$	0	1	0	0	1	0	0	0	0	0	0	0	0	0	R_1	R_0	8	2	Carry
DRLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$,$(EA_0) \leftarrow (CY)$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	1	0	1	1	0	1	0	0	8	2	
DRLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$,$(EA_{15}) \leftarrow (CY)$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	1	0	1	1	0	0	0	0	8	2	
DSLL	EA	$(EA_{n+1}) \leftarrow (EA_n)$,$(EA_0) \leftarrow 0$, $(CY) \leftarrow (EA_{15})$	0	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0	8	2	
DSLR	EA	$(EA_{n-1}) \leftarrow (EA_n)$,$(EA_{15}) \leftarrow 0$, $(CY) \leftarrow (EA_0)$	0	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	8	2	
Jump																					
JMP	*word	(PC) ← word	0	1	0	1	0	1	0	0	Low addr								10	3	
			High addr																		
JB		$(PC_H) \leftarrow (B)$,$(PC_L) \leftarrow (C)$	0	0	1	0	0	0	0	1									4	1	
JR	word	(PC) ← (PC) + 1 + jdisp 1	1	1	←		jdisp1			→									10	1	
JRE	*word	(PC) ← (PC) + 2 + jdisp	0	1	0	0	1	1	1	←	jdisp							→	10	2	
JEA		(PC) ← (EA)	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	0	8	2	
Call																					
CALL	*word	$((SP)-1) \leftarrow ((PC)+3)_H$, $((SP)-2) \leftarrow ((PC)+3)_L$, (PC) ← word, (SP) ← (SP) − 2	0	1	0	0	0	0	0	0	Low addr								16	3	
			High addr																		
CALB		$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_H) \leftarrow (B)$, $(PC_L) \leftarrow (C)$, (SP) ← (SP) − 2	0	1	0	0	1	0	0	0	0	0	1	0	1	0	0	1	17	2	
CALF	*word	$((SP)-1) \leftarrow ((PC)+2)_H$, $((SP)-2) \leftarrow ((PC)+2)_L$, $(PC_{15\text{-}11}) \leftarrow 00001$, $(PC_{10\text{-}0}) \leftarrow$ fa, (SP) ← (SP) − 2	0	1	1	1	1	←			fa							→	13	2	

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code																State(1)	Bytes	Skip Condition
			7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
						B1	B3							B2	B4						
Call (cont)																					
CALT	word	((SP) − 1) ← ((PC) + 1)$_H$, ((SP) − 2) ← ((PC) + 1)$_L$ (PC$_L$) ← (128 + 2ta),(PC$_H$) ← (129 + 2ta),(SP) ← (SP) − 2	1	0	0	←		ta		→									16	1	
SOFTI		((SP) − 1) ← (PSW),((SP) − 2) ← ((PC) + 1)$_H$,((SP) − 3) ← ((PC) + 1)$_L$, (PC) ← 0060H,(SP) ← (SP) − 3	0	1	1	1	0	0	1	0									16	1	
Return																					
RET		(PC$_L$) ← ((SP)),(PC$_H$) ← ((SP) + 1) (SP) ← (SP) + 2	1	0	1	1	1	0	0	0									10	1	
RETS		(PC$_L$) ← ((SP)),(PC$_H$) ← ((SP) + 1) (SP) ← (SP) + 2,(PC) ← (PC) + n	1	0	1	1	1	0	0	1									10	1	Unconditional Skip
RETI		(PC$_L$) ← ((SP)),(PC$_H$) ← ((SP) + 1) (PSW) ← ((SP) + 2), (SP) ← (SP) + 3	0	1	1	0	0	0	1	0									13	1	
Skip																					
Bit		bit, wa	0	1	0	1	1	B_2	B_1	B_0	Offset								10	2	Bit Test
CPU Control																					
SK	f	Skip if f = 1	0	1	0	0	1	0	0	0	0	0	0	0	1	F_2	F_1	F_0	8	2	f = 1
SKN	f	Skip if f = 0	0	1	0	0	1	0	0	0	0	0	0	1	1	F_2	F_1	F_0	8	2	f = 0
SKIT	irf	Skip if irf = 1, then reset irf	0	1	0	0	1	0	0	0	0	1	0	I_4	I_3	I_2	I_1	I_0	8	2	irf = 1
SKNIT	irf	Skip if irf = 0 Reset irf if irf = 1	0	1	0	0	1	0	0	0	0	1	1	I_4	I_3	I_2	I_1	I_0	8	2	irf = 0
NOP		No operation	0	0	0	0	0	0	0	0									4	1	
EI		Enable interrupt	1	0	1	0	1	0	1	0									4	1	
DI		Disable interrupt	1	0	1	1	1	0	1	0									4	1	
HLT		Halt	0	1	0	0	1	0	0	0	0	0	1	1	1	0	1	1	11	2	

Notes:

(1) In the case of skip condition, the idle states are as follows:
- 1-byte instruction: 4 states
- 2-byte instruction: 8 states
- 3-byte instruction: 11 states
- 2-byte instruction (with *): 7 states
- 3-byte instruction (with *): 10 states
- 4-byte instruction: 14 states

(2) B2 (Data): rpa2 = D + byte, H + byte.

(3) Right side of slash (/) in states indicates case rpa2, rpa3 = D + byte, H + A, H + B, H + EA, H + byte.

(4) B3 (Data): rpa3 = D + byte, H + byte

NEC Electronics Inc.

μPD78PG11
HIGH-END, 8-BIT, SINGLE-CHIP NMOS MICROCOMPUTER WITH PIGGYBACK EPROM

Description

The NEC μPD78PG11 is a prototyping device used to emulate the masked-ROM μPD7811. The user can insert a standard EPROM (2732A or 2764) into the terminals on top of the μPD78PG11. The program will be executed from the EPROM just as it would be executed from the masked-ROM on the μPD7811.

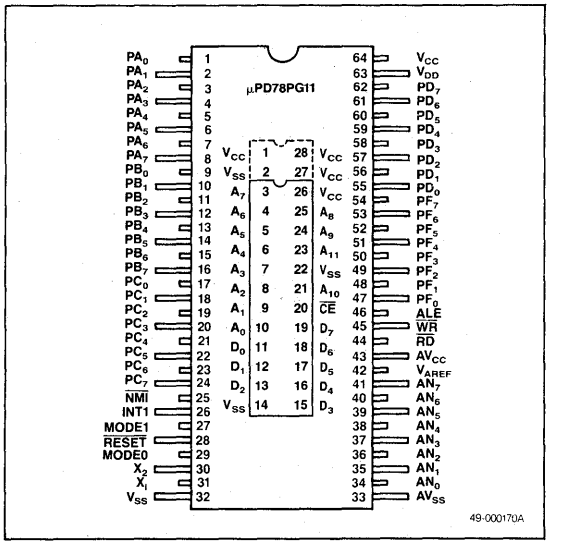
Features

- NMOS silicon gate technology requiring +5V power supply
- Complete single-chip microcomputer
  - 16-bit ALU
  - 4K-EPROM (via piggyback socket)
  - 256-byte RAM
- 44 I/O lines
- Two zero-cross detect inputs
- Two 8-bit timers
- Multifunction 16-bit timer/event counter
- Expansion capabilities
  - 8085A bus-compatible
  - 60K-byte external memory address range
- 8-channel, 8-bit A/D converter
  - Autoscan mode
  - Channel select mode
- Full duplex USART
  - Synchronous and asynchronous
- 153 instruction set
  - 16-bit arithmetic, multiply, and divide
- 1μs instruction cycle time (12MHz operation)
- Prioritized interrupt structure
  - 2 external
  - 9 internal
- Standby function
- On-chip clock generator

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD78PG11E	64-pin ceramic piggyback QUIP	12MHz

Pin Configuration



Terminal Identification (Note 1)

Pin No.	Symbol	Function
1	V_{CC}	Provides V_{PP} pin of μPD2764 with 5V.
2	V_{SS}	Maintains 0V on A_{12} address pin of μPD2764 forcing all instruction fetches from lower 4K of EPROM.
3 — 10, 21 23 — 25	A_0 — A_{11}	Address Bus. Outputs lower order 12 bits of the program counter which will be used as an EPROM address signal.
11 — 13, 15 — 19	D_0 — D_7	Data Bus. Inputs data read from EPROM.
14	V_{SS}	Connects to the GND terminal of EPROM.
20	$\overline{CE}$	Chip Enable. Outputs an EPROM chip enable signal.
22	V_{SS}	Ties EPROM $\overline{OE}$ signal to V_{SS}.
26	V_{CC}	Provides μPD2732A with +5V V_{CC} power supply.
27	V_{CC}	Maintains +5V on $\overline{PGM}$ pin of μPD2764.
28	V_{CC}	Provides μPD2764 with +5V V_{CC} power supply.

Note:

(1) Connections from μPD78PG11 to EPROM.

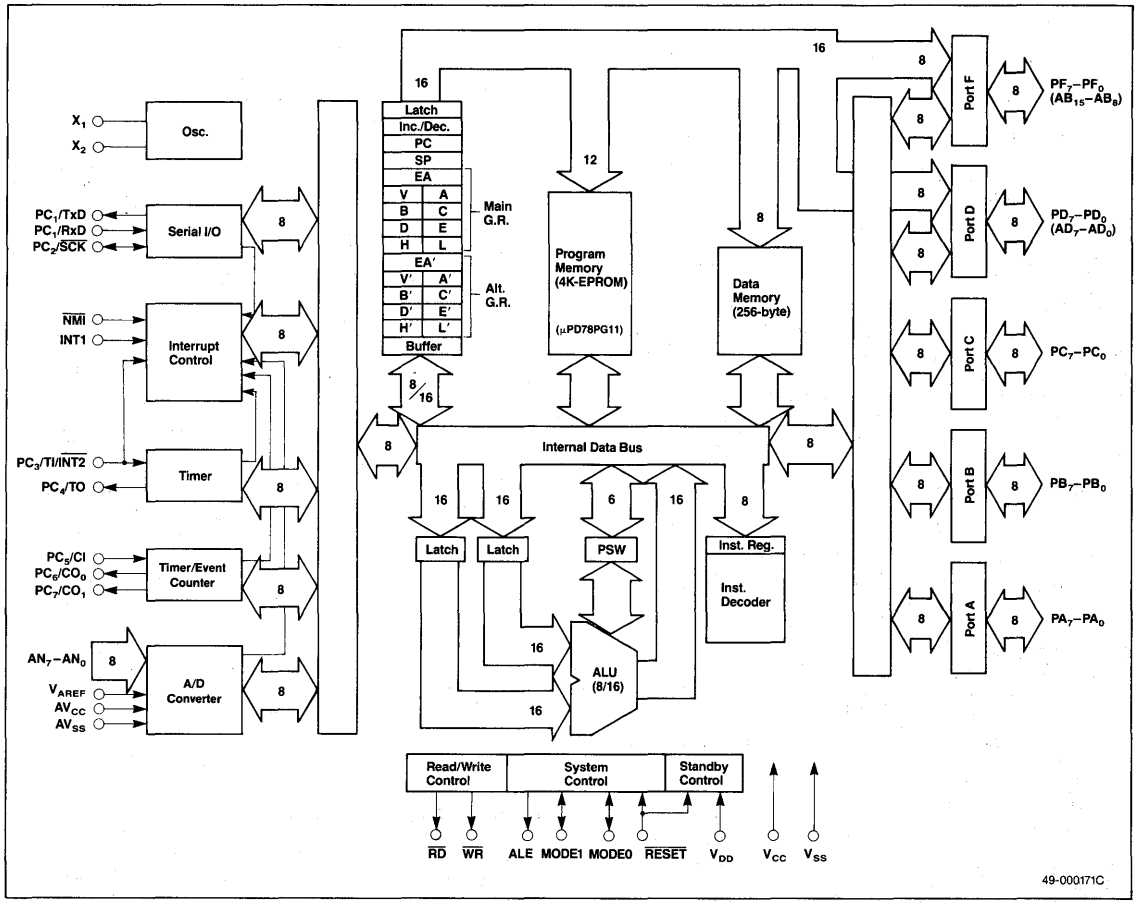
4

Pin Identification

Pin No.	Pin Symbol	Function
1—8	PA_0—PA_7	Port A: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port A in input mode.
9—16	PB_0—PB_7	Port B: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Reset places all lines of Port B in input mode.
17—24	PC_0—PC_7	Port C: (Three-state input/output) 8-bit programmable I/O port. Each line independently programmable as an input or output. Alternatively, Port C may be used as control lines for USART and timer. Reset puts Port C in port mode and all lines in input mode.
17	PC_0	Transmit Data (T x D): Serial data output terminal.
18	PC_1	Receive Data (R x D): Serial data input terminal.
19	PC_2	Serial Clock ($\overline{SCK}$): Serial clock input/output terminal. When internal clock is used, the output can be selected: when an external clock is used, the input can be selected.
20	PC_3	Timer Input (TI)/interrupt request input ($\overline{INT2}$): Timer clock input terminal; can also be used as falling edge, maskable-interrupt input terminal and AC input zero-cross detection terminal.
21	PC_4	Timer Output (TO): This output signal is a square wave whose frequency is determined by the timer/counter.
22	PC_5	Counter Input (CI): External pulse input terminal to the timer/event counter.
23, 24	PC_6, PC_7	Counter Outputs 0, 1 (CO_0—CO_1): Programmable rectangular wave output terminal based on timer/event counter.
25	$\overline{NMI}$	Falling-edge, nonmaskable interrupt ($\overline{NMI}$) input.
26	INT1	A rising-edge, maskable interrupt input. Alternatively, can be used for a zero-cross detection AC input.
27	MODE1	Used as input in conjunction with MODE0 to select appropriate memory expansion mode. Also outputs M1 signal during each opcode fetch.
28	$\overline{RESET}$	(Input, active low). $\overline{RESET}$ initializes the μPD78PG11.
29	MODE0	Used as input in conjunction with MODE1 to select appropriate memory expansion mode. Also used to output IO/M.
30—31	X_2, X_1 (crystal)	A crystal connection terminal for system clock osciliation. When an external clock is supplied X_1 is the input.
32	V_{SS}	Power supply ground potential.
33	AV_{SS}	A/D converter power supply ground potential. Sets conversion range lower limit.
34—41	AN_0—AN_7	Eight analog inputs to the A/D converter. AN_7—AN_4 can also be used as a digital input port for falling edge detection.
42	V_{AREF}	Reference voltage for A/D converter. Sets conversion range upper limit.
43	AV_{CC}	Power supply voltage for A/D converter.
44	$\overline{RD}$	(Three-state output, active low) $\overline{RD}$ is used as a strobe to gate data from external devices onto the data bus. $\overline{RD}$ goes high during Reset.
45	$\overline{WR}$	(Three-state output, active low) $\overline{WR}$, when active, indicates that the data bus holds valid data. Used as a strobe signal for external memory or I/O write operations. $\overline{WR}$ goes high during Reset.
46	ALE	The strobe signal is for latching the address signal to the output from PD_7—PD_0 when accessing external expansion memory.
47—54	PF_0—PF_7	Port F: (Three-state input/output) 8-bit programmable I/O port. Each line configurable independently as an input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
55—62	PD_0—PD_7	Port D: 8-bit programmable I/O port. This byte can be designated as either input or output. Address Bus: When external expansion memory is used, multiplexed address/data bus can be selected.
63	V_{DD}	Backup power terminal for on-chip RAM.
64	V_{CC}	+5V power supply.

Notes: 1 clock cycle = 1 CL = 3/f.
1 machine cycle = 3 or 4 clock cycles.
1 instruction cycle = 1 to 19 machine cycles.
f: System clock frequency (MHz).

Block Diagram



Absolute Maximum Ratings

T_A = 25°C

Power Supply Voltage V_{CC}, V_{DD}, AV_{CC}	-0.5V to +7.0V
Input Voltage, V_I	-0.5V to +7.0V
Output Voltage, V_O	-0.5V to +7.0V
Reference Input Voltage, V_{AREF}	-0.5V to +V_{CC}
Operating Temperature, T_{ORP}	
10MHz<f_{XTAL}≤12MHz	-10°C to +70°C
f_{XTAL}≤10MHz	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

Oscillator Frequency	T_A	V_{CC}, AV_{CC}
10MHz<f_{XTAL}≤12MHz	-10°C to +70°C	+5.0V ±5%
f_{XTAL}≤10MHz	-40°C to +85°C	±5.0V +10%

Capacitance

T_A = 25°C; V_{CC} = V_{DD} = V_{SS} = 0V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Capacitance	C_I			10	pF	All f_C = 1MHz Unmeasured pin returned to 0V.
Output Capacitance	C_O			20	pF	
I/O Capacitance	C_{IO}			20	pF	

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = −5.0 V ±5%; V_{SS} = 0 V; V_{CC} −0.8 V ≤ V_{DD} ≤ V_{CC}

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	0		0.8	V	
Input High Voltage	V_{IH1}	2.0		V_{CC}	V	All except $\overline{SCK}$, $\overline{RESET}$ and X_1
	V_{IH2}	0.8V_{CC}		V_{CC}	V	$\overline{SCK}$, X_1
	V_{IH3}	0.8V_{DD}		V_{CC}	V	$\overline{RESET}$
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −200μA
Input Current	I_I			±200	μA	INT1, TI (PC_3): +0.45V ≤ V_{IN} < V_{CC}
Input Leakage Current	I_{LI}			±10	μA	All except INT1, TI(PC_3) 0V ≤ V_{IN} ≤ V_{CC}
Output Leakage Current	I_{LO}			±10	μA	+0.45V ≤ V_O ≤ V_{CC}
V_{DD} Supply Current	I_{DD}		1.5	3.5	mA	T_A = −40°C to +85°C
V_{CC} Supply Current	I_{CC}		140[1]	250	mA	T_A = −40°C to +85°C

Note: 1. T_A = 25°C; V_{CC} = V_{DD} = +5.0 V

Zero-cross Characteristics

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero-cross Detection Input	V_{ZX}	1		3	VAC_{P-P}	AC Coupled
Zero-cross Accuracy	A_{ZX}			±135	mV	60Hz Sine Wave
Zero-cross Detection Input Frequency	f_{ZX}	0.06		1	kHz	

Serial Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ Cycle Time	t_{CYK}	1			μs	$\overline{SCK}$ Input 1, 2
		500			ns	
		2			μs	$\overline{SCK}$ Output
$\overline{SCK}$ Width Low	t_{KKL}	400			ns	$\overline{SCK}$ Input 1, 2
		200			ns	
		900			ns	$\overline{SCK}$ Output
$\overline{SCK}$ Width High	t_{KKH}	400			ns	$\overline{SCK}$ Input 1, 2
		200			ns	
		900			ns	$\overline{SCK}$ Output
RxD Set-up Time to $\overline{SCK}$ ↑	t_{RXK}	80			ns	Note 1
RxD Hold Time After $\overline{SCK}$ ↑	t_{KRS}	80			ns	Note 1
$\overline{SCK}$ ↓ TxD Delay Time	t_{KTX}			210	ns	Note 1

Notes: 1. 1x Baud rate in Asynchronous, Synchronous, or I/O interface mode.
2. 16x Baud rate or 64x Baud rate in Asynchronous mode.

A/D Converter Characteristics

$T_A = -10°C$ to $+70°C$; $V_{CC} = AV_{CC} = +5.0\,V \pm 5\%$; $V_{SS} = AV_{SS} = 0\,V$; $AV_{CC} - 0.5\,V \leq V_{AREF} \leq AV_{CC}$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Resolution		8			Bits	
Absolute Accuracy			0.4% ± ½		LSB	$T_A = -10°C$ to $+50°C$
			0.6% ± ½		LSB	$T_A = -10°C$ to $+70°C$ Note 1
Conversion Time	t_{CONV}	576			t_{CYC}	$83ns \leq t_{CYC} \leq 110ns$
		432			t_{CYC}	$110ns \leq t_{CYC} \leq 170ns$
Sampling Time	t_{SAMP}	96			t_{CYC}	$83ns \leq t_{CYC} \leq 110ns$
		72			t_{CYC}	$110ns \leq t_{CYC} \leq 170ns$
Analog Input Voltage	V_{IA}	0		V_{AREF}	V	

Note: 1. In case of $f_{XTAL} \leq 10$ MHz, $T_A = -40°C$ to $+85°C$.

Bus Timing Depending on t_{CYC}

Symbol	Calculating Expression	Min/Max
t_{RP}	6OT	Min
t_T	6T	Min
t_{CI}2	6T	Min
t_{CI}3	48T	Min
t_{IP}	36T	Min
t_{AL}	2T - 100	Min
t_{LA}	T - 30	Min
t_{AR}	3T - 100	Min
t_{AD}	7T - 220	Max
t_{LDR}	5T - 200	Max
t_{RD}	4T - 150	Max
t_{LR}	T - 50	Min
t_{RL}	2T - 50	Min
t_{RR}	4T - 50 (Data Read) 7T - 50 (Opcode Fetch)	Min
t_{LL}	2T - 40	Min
t_{AW}	3T - 100	Min
t_{LDW}	T + 110	Max
t_{LW}	T - 50	Min
t_{DW}	4T - 100	Min
t_{WDH}	2T - 70	Min
t_{WL}	2T - 50	Min
t_{WW}	4T - 50	Min
t_{CYK}	12T ($\overline{SCK}$ Input) 1 24T ($\overline{SCK}$ Output)	Min
t_{KKL}	6T - 100 ($\overline{SCK}$ Input) 1 12T - 100 ($\overline{SCK}$ Output)	Min
t_{KKH}	6T - 100 ($\overline{SCK}$ Input) 1 12T - 100 ($\overline{SCK}$ Output)	Min

Notes: 1. 1x Baud rate in Asynchronous, Synchronous, or I/O interface mode. $T = t_{CYC} = 1\,f_{XTAL}$. The items not included in this list are independent of oscillator frequency (f_{XTAL}).
2. Event Counter mode.
3. Pulse Width Measurement mode.

4

AC Characteristics

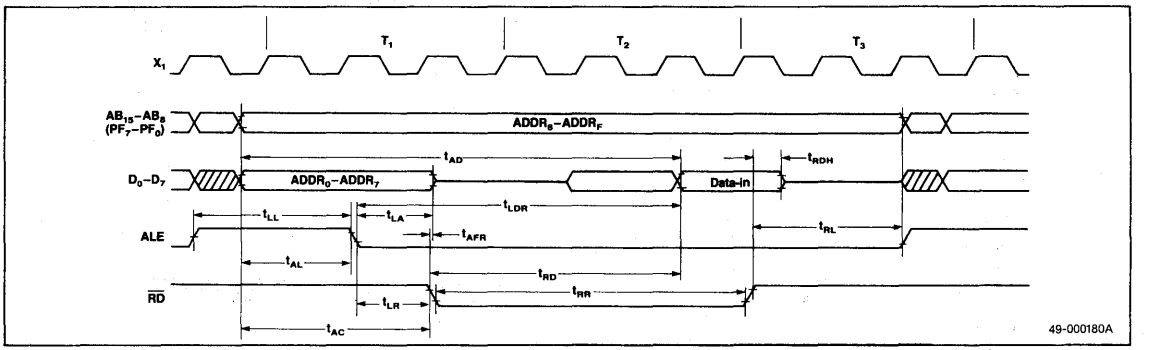
$T_A = 10°C$ to $+70°C$; $V_{CC} = +5.0\ V \pm 5\%$; $V_{SS} = 0\ V$; $V_{CC} - 0.8\ V \leq V_{DD} \leq V_{CC}$

Read/Write Operation		Limits					Test Conditions
		f_{XTAL} = 10 MHz		f_{XTAL} = 12 MHz			
Parameter	Symbol	Min	Max	Min	Max	Unit	1
$\overline{\text{Reset}}$ Pulse Width	t_{RP}	6.0		5.0		μs	
Interrupt Pulse Width	t_{IP}	3.6		3.0		μs	
Counter Input Pulse Width	t_{CI}2	600		500		ns	
	t_{CI}3	4.8		4.0		μs	
Timer Input Pulse Width	t_{TI}	600		500		ns	
X_1 Input Cycle Time	t_{CYC}	100		83		ns	
Address Set-Up to ALE ↓	t_{AL}	100		65		ns	
Address Hold after ALE ↓	t_{LA}	70		50		ns	
Address to $\overline{\text{RD}}$ ↓ Delay Time	t_{AR}	200		150		ns	
$\overline{\text{RD}}$ ↓ to Address Floating	t_{AFR}		20		20	ns	
Address to Data Input	t_{AD}		480		360	ns	
ALE ↓ to Data Input	t_{LDR}		300		215	ns	
$\overline{\text{RD}}$ ↓ to Data Input	t_{RD}		250		180	ns	
ALE ↓ to $\overline{\text{RD}}$ ↓ Delay Time	t_{LR}	50		35		ns	
Data Hold Time to $\overline{\text{RD}}$ ↑	t_{RDH}	0		0		ns	
$\overline{\text{RD}}$ ↑ to ALE ↑ Delay Time	t_{RL}	150		115		ns	
$\overline{\text{RD}}$ Width Low	t_{RR}	350		280		ns	Data Read
		650		530		ns	Opcode Fetch
ALE Width High	t_{LL}	160		125		ns	
Address to $\overline{\text{WR}}$ ↓ Delay	t_{AW}	200		150		ns	
ALE ↓ to Data Output	t_{LDW}		210		195	ns	
$\overline{\text{WR}}$ ↓ to Data Output	t_{WD}	130		100		ns	
ALE ↓ to $\overline{\text{WR}}$ ↓ Delay	t_{LW}	50		35		ns	
Data Set-up Time to $\overline{\text{WR}}$ ↑	t_{DW}	300		230		ns	
Data Hold Time to $\overline{\text{WR}}$ ↑	t_{WDH}	130		95		ns	
$\overline{\text{WR}}$ ↑ to ALE ↑ Delay Time	t_{WL}	150		115		ns	
$\overline{\text{WR}}$ Width Low	t_{WW}	350		280		ns	

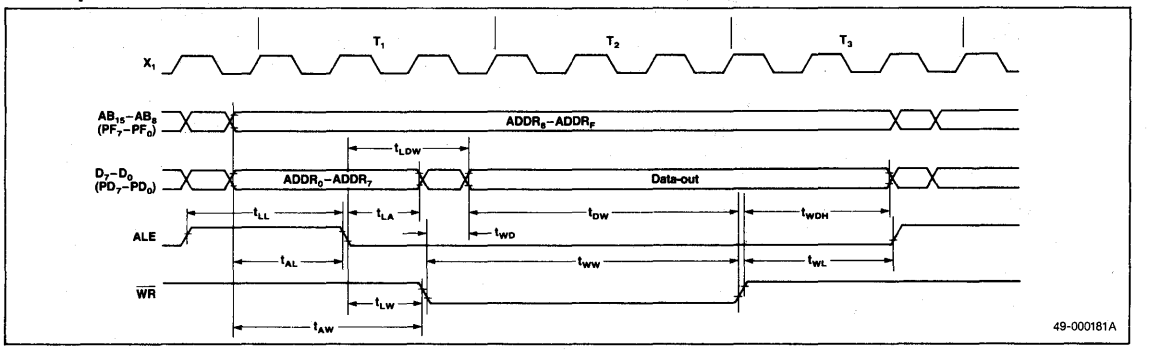
Notes: 1. Load Capacitance: $C_L = 150$ pF. 2. Event counter mode. 3. Pulse width measurement mode.

Timing Waveforms

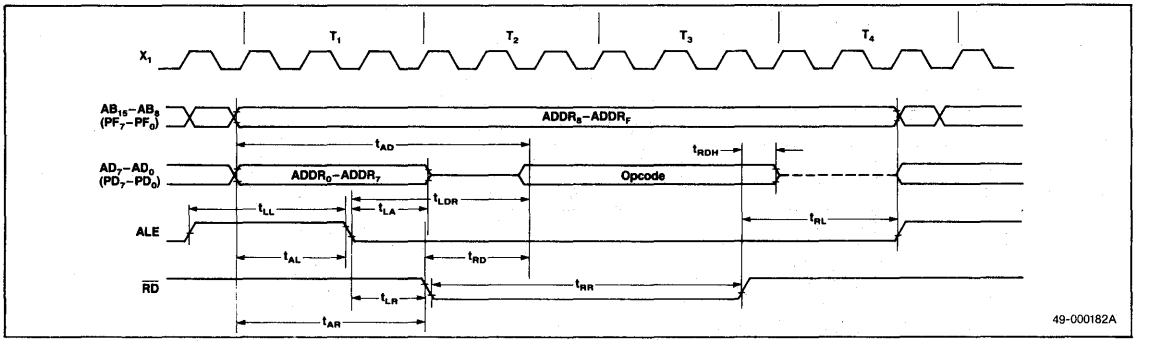
Read Operation



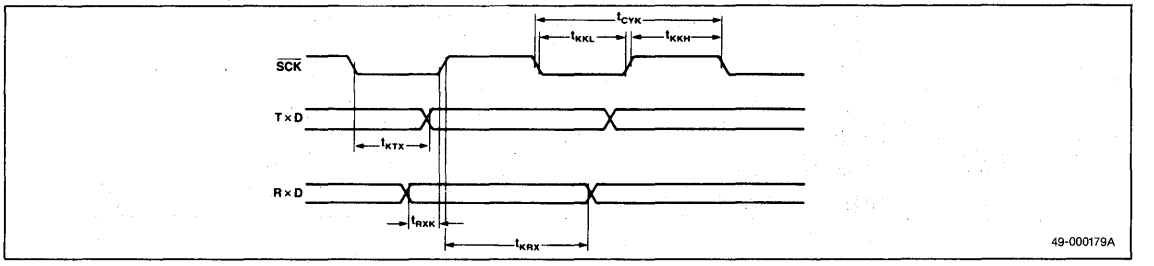
Write Operation



Opcode Fetch Operation



Transmit/Receive Timing



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Remarks

1. sr—sr4 (special register)

PA	= Port A	ECNT	= Timer/Event Counter Upcounter
PB	= Port B	ECPT	= Timer/Event Counter Capture
PC	= Port C	ETMM	= Timer/Event Counter Mode
PD	= Port D	EOM	= Timer/Event Counter Output Mode
PF	= Port F	ANM	= A/D Channel Mode
MA	= Mode A		
MB	= Mode B	CR_0 to CR_3	= A/D Conversion Results 0—3
MC	= Mode C	TxB	= TxBuffer
MCC	= Mode Control C	RxB	= RxBuffer
MF	= Mode F	SMH	= Serial Mode High
MM	= Memory Mapping	SML	= Serial Mode Low
TM_0	= Timer Register 0	MKH	= Mask High
TM_1	= Timer Register 1	MKL	= Mask Low
TMM	= Timer Mode		
ETM_0	= Timer Event Counter Register 0		
ETM_1	= Timer Event Counter Register 1		

2. rp—rp3 (register pair)

SP	= Stack Pointer	H	= HL
B	= BC	V	= VA
D	= DE	EA	= Extended Accumulator

3. rpa—rpa3 (rp addressing)

B	= (BC)	D++	= (DE)++
D	= (DE)	H++	= (HL)++
H	= (HL)	D+byte	= (DE+byte)
D+	= (DE)+	H+A	= (HL+A)
H+	= (HL)+	H+B	= (HL+B)
D-	= (DE)-	H+EA	= (HL+EA)
H-	= (HL)-	H+byte	= (HL+byte)

4. (flag)

CY = Carry	HC = Half Carry	Z = Zero

5. irf (interrupt flag)

FNMI	= INTFNMI	FSR	= INTFSR
FT0	= INTFT0	FST	= INTFST
FT1	= INTFT1	ER	= Error
F1	= INTF1	OV	= Overflow
F2	= INTF2	AN_4 to AN_4	= Analog Input 4—7
FE0	= INTFE0	SB	= Standby
FE1	= INTFE1		
FEIN	= INTFEIN		
FAD	= INTFAD		

Instruction Set Symbol Definitions

Symbol	Description
←	Transfer direction, result
∧	Logical product (logical AND)
∨	Logical sum (logical OR)
∀	Exclusive OR
—	Complement
•	Concatenation

Instruction Groups

8-bit Data Transfer

Mnemonic		Operand	Opcode B1	B2	B3	B4	State[1]	Operation	Skip Condition
MOV		r1, A	$00011T_2T_1T_0$				4	(r1)←(A)	
		A, r1	$00001T_2T_1T_0$				4	(A)←(r1)	
	*	sr, A	01001101	$110S_4S_3S_2S_1S_0$			10	(sr)←(A)	
	*	A, sr1	01001100	$11S_5S_4S_3S_2S_1S_0$			10	(A)←(sr1)	
		r, word	01110000	$01101R_2R_1R_0$	Low Addr	High Addr	17	(r)←(word)	
		word, r	01110000	$01111R_2R_1R_0$	Low Addr	High Addr	17	(word)←(r)	
MVI	*	r, byte	$01101R_2R_1R_0$	Data			7	(r)←byte String skip, when r = A or L	
		sr2, byte	01100100	$S_300000S_2S_1S_0$	Data		14	(sr2)←byte	
MVIW	*	wa, byte	01110001	Offset	Data		13	((V), (wa))←byte	
MVIX	*	rpa1, byte	$01001 0A_1A_0$	Data			10	(rpa1)←byte	
STAW	*	wa	01100011	Offset			10	((V)(wa))←A	

Instruction Groups (cont)

8-Bit Data Transfer (cont)

Mnemonic		Operand	Opcode B1	B2	B3	B4	State [1]	Operation	Skip Condition
LDAW	*	wa	00000001	Offset			10	(A)←((V), (wa))	
STAX	*	rpa2	$A_3$0111$A_2A_1A_0$	Data [2]			7/13 [3]	(rpa2)←(A)	
LDAX	*	rpa2	$A_3$0101$A_2A_1A_0$	Data [2]			7/13 [3]	(A)←((rpa2))	
EXX			00010001				8	(B)↔(B'), (C)↔(C'), (D)↔(D') (E)↔(E'), (H)↔(H'), (L)↔(L')	
EXA			00010000				8	(V)↔(V'), (A)↔(A'), (EA)↔(EA')	
EXH			01010000				8	(H)↔(H'), (L)↔(L')	

16-bit Data Transfer

Mnemonic		Operand	Opcode B1	B2	B3	B4	State [1]	Operation	Skip Condition
BLOCK			00110001				13 (C + 1)	((DE))←((HL)), (DE)←(DE) + 1, (HL)←(HL) + 1, (C)←(C) - 1 End if borrow	
DMOV		rp3, EA	101101P_1P_0				4	($rp3_L$)←(EAL), ($rp3_H$)←(EAH)	
		EA, rp3	101001P_1P_0				4	(EAL)←($rp3_L$), (EAH)←($rp3_H$)	
		sr3, EA	01001000	1101001U_0			14	(sr3)←(EA)	
		EA, sr4	↓	110000V_1V_0			14	(EA)←(sr4)	
SBCD		word	01110000	00011110	Low Addr	High Addr	20	(word)←(C), ((word) + 1) ←(B)	
SDED		word	↓	00101110	↓	↓	20	(word)←(E), ((word) + 1) ←(D)	
SHLD		word		00111110			20	(word)←(L), ((word) + 1) ←(H)	
SSPD		word		00001110			20	(word)←(SP_L), ((word + 1) ←(SP_H)	
STEAX		rpa3	01001000	1001$C_3C_2C_1C_0$	Data [4]		14/20 [3]	((rpa3))←(EAL), ((rpa3) + 1)←(EAH)	
LBCD		word	01110000	00011111	Low Addr	High Addr	20	(C)←(word), (B)←((word) + 1)	
LBCD		word	↓	00101111	↓	↓	20	(E)←(word), (D)←((word) + 1)	
LHLD		word		00111111			20	(L)←(word), (H)←((word) + 1)	
LSPD		word		00001111			20	(SP_L)←(word), (SP_H)←((word) + 1)	
LDEAX		rpa3	01001000	1000$C_3C_2C_1C_0$	Data [4]		14/20 [3]	(EAL)←((rpa3)), (EAH)←((rpa3) + 1)	
PUSH		rp1	10110$Q_2Q_1Q_0$				13	((SP) - 1)←($rp1_H$)((SP) - 2) ← ($rp1_L$)(SP)←(SP) - 2	
POP		rp1	10100$Q_2Q_1Q_0$				10	($rp1_L$)←((SP)), ($rp1_H$)←((SP) + 1) (SP)←(SP) + 2)	
LXI	*	rp2, word	0$P_2P_1P_0$0100		Low Byte	High Byte	10	(rp2)←(word) String skip when rp2 = H	

8-bit Aritmetic (Register)

Mnemonic		Operand	Opcode B1	B2	B3	B4	State [1]	Operation	Skip Condition
TABLE			01001000	10101000			17	(C)←((PC) + 3 + (A)) B←((PC) + 3 + (A) + 1)	
ADD		A, r	01100000	11000$R_2R_1R_0$			8	(A)←(A) + (r)	
		r, A	↓	01000$R_2R_1R_0$			8	(r)←(r) + (A)	
ADC		A, r		11010$R_2R_1R_0$			8	(A)←(A) + (r) + (CY)	
		r, A		01010$R_2R_1R_0$			8	(r)←(r) + (A) + (CY)	

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Instruction Groups (cont)

Mnemonic	Operand	Opcode B1	Opcode B2	Opcode B3	Opcode B4	State [1]	Operation	Skip Condition
8-Bit Arithmetic (Register) (cont)								
ADDNC	A, r	01100000	10100$R_2R_1R_0$			8	(A)←(A) + (r)	No Carry
	r, A		00100$R_2R_1R_0$			8	(r)←(r) + (A)	No Carry
SUB	A, r		11100$R_2R_1R_0$			8	(A)←(A) - (r)	
	r, A		01100$R_2R_1R_0$			8	(r)←(r) - (A)	
SBB	A, r		11110$R_2R_1R_0$			8	(A)←(A) - (r) - (CY)	
	r, A		01110$R_2R_1R_0$			8	(r)←(r) - (A) - (CY)	
SUBNB	A, r		10110$R_2R_1R_0$			8	(A)←(A) - (r)	No Borrow
	r, A		00110$R_2R_1R_0$			8	(r)←(r) - (A)	No Borrow
ANA	A, r		10001$R_2R_1R_0$			8	(A)←(A) ∧ (r)	
	r, A		00001$R_2R_1R_0$			8	(r)←(r) ∧ (A)	
ORA	A, r	01100000	10011$R_2R_1R_0$			8	(A)←(A)∨(r)	
	r, A		00011$R_2R_1R_0$			8	(r)←(r)∨(A)	
XRA	A, r		10010$R_2R_1R_0$			8	(A)←(A)∀(r)	
	r, A		00010$R_2R_1R_0$			8	(r)←(r)∀(A)	
GTA	A, r		10101$R_2R_1R_0$			8	(A) - (r) - 1	No Borrow
	r, A		00101$R_2R_1R_0$			8	(r) - (A) - 1	No Borrow
LTA	A, r		10111$R_2R_1R_0$			8	(A) - (r)	Borrow
	r, A		00111$R_2R_1R_0$			8	(r) - (A)	Borrow
NEA	A, r		11101$R_2R_1R_0$			8	(A) - (r)	No Zero
	r, A		01101$R_2R_1R_0$			8	(r) - (A)	No Zero
EQA	A, r		11111$R_2R_1R_0$			8	(A) - (r)	Zero
	r, A		01111$R_2R_1R_0$			8	(r) - (A)	Zero
ONA	A, r		11001$R_2R_1R_0$			8	(A)∧(r)	No Zero
OFFA	A, r	01100000	11011$R_2R_1R_0$			8	(A)∧(r)	Zero
8-bit Arithmetic (Memory)								
ADDX	rpa	01110000	11000$A_2A_1A_0$			11	(A)←(A) + ((rpa))	
ADCX	rpa		11010$A_2A_1A_0$			11	(A)←(A) + ((rpa)) + (CY)	
ADDNCX	rpa		10100$A_2A_1A_0$			11	(A)←(A) + ((rpa))	No Carry
SUBX	rpa		11100$A_2A_1A_0$			11	(A)←(A) - ((rpa))	
SBBX	rpa		11110$A_2A_1A_0$			11	(A)←(A) - ((rpa)) - (CY)	
SUBNBX	rpa		10110$A_2A_1A_0$			11	(A)←(A) - ((rpa))	No Borrow
ANAX	rpa		10001$A_2A_1A_0$			11	(A)←(A) - ((rpa))	
ORAX	rpa		10011$A_2A_1A_0$			11	(A)←(A)∨((rpa))	
XRAX	rpa		10010$A_2A_1A_0$			11	(A)←(A)∀((rpa))	
GTAX	rpa		10101$A_2A_1A_0$			11	(A) - ((rpa)) - 1	No Borrow
LTAX	rpa		10111$A_2A_1A_0$			11	(A) - ((rpa))	Borrow
NEAX	rpa		11101$A_2A_1A_0$			11	(A) - ((rpa))	No Zero
EQAX	rpa		11111$A_2A_1A_0$			11	(A) - ((rpa))	Zero
ONAX	rpa		11001$A_2A_1A_0$			11	(A)←((rpa))	No Zero
OFFAX	rpa		11011$A_2A_1A_0$			11	(A)←((rpa))	Zero

Instruction Groups (cont)

Immediate Data

Mnemonic		Operand	Opcode B1	Opcode B2	Opcode B3	Opcode B4	State [1]	Operation	Skip Condition
ADI	*	A, byte	01000110	←Data→			7	(A)←(A) + byte	
		r, byte	01110100	$01000R_2R_1R_0$	Data		11	(r)←(r) + byte	
		sr2, byte	0110 ↓	$S_31000S_2S_1S_0$	↓		20	(sr2)←(sr2) + byte	
ACI	*	A, byte	01010110	←Data→			7	(A)←(A) + byte + (CY)	
		r, byte	01110100	$01010R_2R_1R_0$	Data		11	(r)←(r) + byte + (CY)	
		sr2, byte	0110 ↓	$S_31010S_2S_1S_0$	↓		20	(sr2)←(sr2) + byte + (CY)	
ADINC	*	A, byte	00100110	←Data→			7	(A)←(A) + byte	No Carry
		r, byte	01110100	$00100R_2R_1R_0$	Data		11	(r)←(r) + byte	No Carry
		sr2, byte	0110 ↓	$S_30100S_2S_1S_0$	↓		20	(sr2)←(sr2) + byte	No Carry
SUI	*	A, byte	01100110	←Data→			7	(A)←(A) - byte	
		r, byte	01110100	$01100R_2R_1R_0$	Data		11	(r)←(r) - byte	
		sr2, byte	0110 ↓	$S_31100S_2S_1S_0$	↓		20	(sr2)←(sr2) - byte	
SBI	*	A, byte	01110110	←Data→			7	(A)←(A) - byte - (CY)	
		r, byte	01110100	$01110R_2R_1R_0$	Data		11	(r)←(r) - byte - (CY)	
		sr2, byte	0110 ↓	$S_31110S_2S_1S_0$	↓		20	(sr2)←(sr2) - byte - (CY)	
SUINB	*	A, byte	00110110	←Data→			7	(A)←(A) - byte	No Borrow
		r, byte	01110100	$00110R_2R_1R_0$	Data		11	(r)←(r) - byte	No Borrow
		sr2, byte	0110 ↓	$S_30110S_2S_1S_0$	↓		20	(sr2)←(sr2) - byte	No Borrow
ANI	*	A, byte	00000111	←Data→			7	(A)←(A)∧byte	
		r, byte	01110100	$00001R_2R_1R_0$	Data		11	(r)←(r)∧byte	
		sr2, byte	01100100	$S_30001S_2S_1S_0$	↓		20	(sr2)←(sr2)∧byte	
ORI	*	A, byte	00010111	←Data→			7	(A)←(A)∨byte	
		r, byte	01110100	$00011R_2R_1R_0$	Data		11	(r)←(r)∨byte	
		sr2, byte	0110 ↓	$S_30011S_2S_1S_0$	↓		20	(sr2)←(sr2)∨byte	
XRI	*	A, byte	00010110	←Data→			7	(A)←(A)¥byte	
		r, byte	01110100	$00010R_2R_1R_0$	Data		11	(r)←(r)¥byte	
		sr2, byte	0110 ↓	$S_30010S_2S_1S_0$	↓		20	(sr2)←(sr2)¥byte	
GTI	*	A, byte	00100111	←Data→			7	(A) - byte - 1	No Borrow
		r, byte	01110100	$00101R_2R_1R_0$	Data		11	(r) - byte - 1	No Borrow
		sr2, byte	0110 ↓	$S_30101S_2S_1S_0$	↓		14	(sr5) - byte - 1	No Borrow
LTI	*	A, byte	00110111	←Data→			7	(A) - byte	Borrow
		r, byte	01110100	$00111R_2R_1R_0$	Data		11	(r) - byte	Borrow
		sr2, byte	0110 ↓	$S_30111S_2S_1S_0$	↓		14	(sr5) - byte	Borrow
NEI	*	A, byte	01100111	←Data→			7	(A) - byte	No Zero
		r, byte	01110100	$01101R_2R_1R_0$	Data		11	(r) - byte	No Zero
		sr2, byte	0110 ↓	$S_31101S_2S_1S_0$	↓		14	(sr5) - byte	No Zero
EQI	*	A, byte	01110111	←Data→			7	(A) - byte	Zero
		r, byte	01110100	$01111R_2R_1R_0$	Data		11	(r) - byte	Zero
		sr2, byte	0110 ↓	$S_31111S_2S_1S_0$	↓		14	(sr5) - byte	Zero

Instruction Groups (cont)

Mnemonic		Operand	Opcode B1	B2	B3	B4	State [1]	Operation	Skip Condition
Immediate Data (cont)									
ONI	*	A, byte	01000111	←Data→			7	(A).∧byte	No Zero
		r, byte	01110100	01001$R_2R_1R_0$	Data		11	(r).∧byte	No Zero
		sr2, byte	0110 ↓	$S_3$1001$S_2S_1S_0$	↓		14	(sr5).∧byte	No Zero
OFFI	*	A, byte	01010111	←Data→			7	(A).∧byte	Zero
		r, byte	01110100	01011$R_2R_1R_0$	Data		11	(r).∧byte	Zero
		sr2, byte	0110 ↓	$S_3$1011$S_2S_1S_0$	↓		14	(sr5).∧byte	Zero
Working Register									
ADDW		wa	01110100	11000000	Offset		14	(A)←(A) + ((V)•(wa))	
ADCW		wa		1101			14	(A)←(A) + ((V)•(wa)) + (CY)	
ADDNCW		wa		1010			14	(A)←(A) + ((V)•(wa))	No Carry
SUBW		wa		1110			14	(A)←(A) - ((V)•(wa))	
SBBW		wa		1111			14	(A)←(A) - ((V)•(wa)) - (CY)	
SUBNBW		wa		1011			14	(A)←(A) - ((V)•(wa))	No Borrow
ANAW		wa		10001000			14	(A)←(A).∧((V)•(wa))	
ORAW		wa		1001 ↓			14	(A)←(A)V((V)•(wa))	
XRAW		wa	01110100	10010000	Offset		14	(A)←(A)⊻((V)•(wa))	
GTAW		wa		10101000			14	(A) - ((V)•(wa)) - 1	No Borrow
LTAW		wa		1011			14	(A) - ((V)•(wa))	Borrow
NEAW		wa		1110			14	(A) - ((V)•(wa))	No Zero
EQAW		wa		1111			14	(A) - ((V)•(wa))	Zero
ONAW		wa		1100			14	(A).∧((V)•(wa))	No Zero
OFFAW		wa		1101			14	(A).∧((V)•(wa))	Zero
ANIW	*	wa, byte	00000101	←Offset→	Data		19	((V)•(wa))←((V)•(wa)).∧byte	
ORIW	*	wa, byte	0001				19	((V)•(wa))←((V)•(wa))Vbyte	
GTIW	*	wa, byte	0010				13	((V)•(wa)) - byte - 1	No Borrow
LTIW	*	wa, byte	0011				13	((V)•(wa)) - byte	Borrow
NEIW	*	wa, byte	0110				13	((V)•(wa)) - byte	No Zero
EQIW	*	wa, byte	0111				13	((V)•(wa)) - byte	Zero
ONIW	*	wa, byte	0100				13	((V)•(wa)).∧byte	No Zero
OFFIW	*	wa, byte	0101				13	((V)•(wa)).∧byte	Zero
16-bit Arithmetic									
EADD		EA, r2	01110000	010000R_1R_0			11	(EA)←(EA) + (r2)	
DADD		EA, rp3	0100	110001P_1P_0			11	(EA)←(EA) + (rp3)	
DADC		EA, rp3		1101			11	(EA)←(EA) + (rp3) + (CY)	
DADDNC		EA, rp3		1010			11	(EA)←(EA) + (rp3)	No Carry
ESUB		EA, r2	0000	011000R_1R_0			11	(EA)←(EA) - (r2)	
DSUB		EA, rp3	01110100	111001P_1P_0			11	(EA)←(EA) - (rp3)	
DSBB		EA, rp3		1111			11	(EA)←(EA) - (rp3) - (CY)	
DSUBNB		EA, rp3		1011			11	(EA)←(EA) - (rp3)	No Borrow
DAN		EA, rp3		100011P_1P_0			11	(EA)←(EA) - (rp3)	

Instruction Groups (cont)

Mnemonic		Operand	Opcode B1	Opcode B2	Opcode B3	Opcode B4	State [1]	Operation	Skip Condition
16-Bit Arithmetic (cont)									
DOR		EA, rp3	01110100	$100111P_1P_0$			11	(EA)←(EA)∨(rp3)	
DXR		EA, rp3		$100101P_1P_0$			11	(EA)←(EA)∀(rp3)	
DGT		EA, rp3		$101011P_1P_0$			11	(EA) - (rp3) - 1	No Borrow
DLT		EA, rp3		1011			11	(EA) - (rp3)	Borrow
DNE		EA, rp3		1110			11	(EA) - (rp3)	No Zero
DEQ		EA, rp3		1111			11	(EA) - (rp3)	Zero
DON		EA, rp3		1100			11	(EA).∧(rp3)	No Zero
DOFF		EA, rp3		1101			11	(EA).∧(rp3)	Zero
Multiply/Divide									
MUL		r2	01001000	$001011R_1R_0$			32	(EA)←(A) × (r2)	
DIV		r2	↓	0011 ↓			59	(EA)←(EA) + (r2), (r2)←Remainder	
Increment/Decrement									
INR		r2	$010000R_1R_0$				4	(r2) - (r2) + 1	Carry
INRW	*	wa	00100000	←Offset→			16	((V), (wa))←((V), (wa)) + 1	Carry
INX		rp	$00P_1P_00010$				7	(rp)←(rp) + 1	
		EA	10101000				7	(EA)←(EA) + 1	
DCR		r2	$010100R_1R_0$				4	(r2)←(r2) - 1	Borrow
DCRW	*	wa	00110000	←Offset→			16	((V), (wa))←((V), (wa)) - 1	Borrow
DCX		rp	$00P_1P_00011$				7	(rp)←(rp) - 1	
		EA	10101001				7	(EA)←(EA) - 1	
Others									
DAA			01100001				4	Decimal Adjust Accumulator	
STC			01001000	00101011			8	(CY)←1	
CLC			↓	00101010			8	(CY)←0	
NEGA			↓	00111010			8	(A)←(A) + 1	
Rotate and Shift									
RLD			01001000	00111000			17	Rotate Left Digit	
RRD				↓ 1001			17	Rotate Right Digit	
RLL		r2	01001000	$001101R_1R_0$			8	$(r2_{M+1})$←$(r2_M)$, $(r2_0)$←(CY), (CY)←$(r2_7)$	
RLR		r2		↓ $00R_1R_0$			8	$(r2_{M+1})$←$(r2_M)$, $(r2_7)$←(CY), (CY)←$(r2_0)$	
SLL		r2		$001001R_1R_0$			8	$(r2_{M+1})$←$(r2_M)$, $(r2_0)$←0, (CY)←$(r2_7)$	
SLR		r2		↓ $00R_1R_0$			8	$(r2_{M-1})$←$(r2_M)$, $(r2_7)$←0, (CY)←$(r2_0)$	
SLLC		r2		$000001R_1R_0$			8	$(r2_{M+1})$←$(r2_M)$, $(r2_0)$←0, (CY)←$(r2_7)$	Carry
SLRC		r2		↓ $00R_1R_0$			8	$(r2_{M-1})$←$(r2_M)$, $(r2_7)$←0, (CY)←$(r2_0)$	Carry

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Instruction Groups (cont)

Mnemonic		Operand	Opcode B1	B2	B3	B4	State [1]	Operation	Skip Condition
Rotate and Shift (cont)									
DRLL		EA	01001000	10110100			8	$(EA_{N+1})\leftarrow(EA_N)$, $(EA_0)\leftarrow(CY)$, $(CY)\leftarrow(EA_{15})$	
DRLR		EA	↓	↓ 0000			8	$(EA_{N-1})\leftarrow(EA_N)$, $(EA_{15})\leftarrow(CY)$, $(CY)\leftarrow(EA_0)$	
DSLL		EA		10100100			8	$(EA_{N+1})\leftarrow(EA_N)$, $(EA_0)\leftarrow 0$, $(CY)\leftarrow(EA_{15})$	
DSLR		EA	↓	↓ 0000			8	$(EA_{N-1})\leftarrow(EA_N)$, $(EA_{15})\leftarrow 0$	
Jump									
JMP	*	word	01010100	←Low Addr→	High Addr		10	(PC)←word	
JB			00100001				4	$(PC_H)\leftarrow(B)$, $(PC_L)\leftarrow(C)$	
JR		word	11←jdisp 1→				10	(PC)←(PC) + 1 + jdisp 1	
JRE	*	word	0100111←	jdisp→			10	(PC)←(PC) + 2 + jdisp	
JEA			01001000	00101000			8	(PC)←EA	
Call									
CALL	*	word	01000000	←Low Addr→	High Addr		16	$((SP)-1)\leftarrow((PC)+3)_H$, $((SP)-2)\leftarrow((PC)+3)_L$, (PC)←word, (SP)←(SP) - 2	
CALB			01001000	00101001			17	$((SP)-1)\leftarrow((PC)+2)_H$, $((SP)-2)\leftarrow((PC)+2)_L$, $(PC_H)\leftarrow(B)$, (SP)←(SP) - 2	
CALF	*	word	01111←	fa→			13	$((SP)-1)\leftarrow((PC)+2)_H$, $((SP)-2)\leftarrow((PC)+2)_L$, $(PC_{15\text{-}11})\leftarrow$00001, $(PC_{10\text{-}0})\leftarrow$fa, (SP)←(SP) - 2	
CALT		word	100←ta→				16	$((SP)-1)\leftarrow((PC)+1)_H$, $((SP)-2)\leftarrow((PC)+1)_L$ $(PC_L)\leftarrow(128+2ta)$, $(PC_H)\leftarrow(129+2ta)$, (SP)←(SP) - 2	
SOFTI			01110010				16	$((SP)-1)\leftarrow$(PSW), $((SP)-2)\leftarrow((PC)+1)_H$, $((SP)-3)\leftarrow((PC)+1)_L$, (PC)←0060H, (SP)←(SP) - 3	
Return									
RET			10111000				10	$(PC)\leftarrow((SP))$, $(PC_H)\leftarrow((SP)+1)$ (SP)←(SP) + 2	
RETS			↓ 1001				10	$(PC_L)\leftarrow((SP))$, $(PC_H)\leftarrow((SP)+1)$ (SP)←(SP) + 2, (PC)←(PC) + n	
RETI			01100010				13	$(PC_L)\leftarrow((SP))$, $(PC_H)\leftarrow((SP)+1)$ (PSW)←((SP) + 2), (SP)←(SP) + 3	Unconditional Skip
Skip									
BIT		bit, wa	$01011B_2B_1B_0$	←Offset→			10	Bit Test	((V), (wa)) bit = 1
CPU Control									
SK		f	01001000	$0001F_2F_1F_0$			8	Skip if f = 1	f = 1
SKN		f	↓	0001 ↓			8	Skip if f = 0	f = 0
SKIT		irf		$0101I_4I_3I_2I_1I_0$			8	Skip if irf = 1, then reset irf	irf = 1

Instruction Groups (cont)

CPU Control (cont)

Mnemonic	Operand	Opcode B1	Opcode B2	Opcode B3	Opcode B4	State [1]	Operation	Skip Condition
SKNIT	irf	01001000	$0111_4I_3I_2I_1I_0$			8	Skip if irf = 0 Reset irf, if irf = 1	irf = 1
NOP		00000000				4	No Operation	
EI		10101010				4	Enable Interrupt	
DI		10111010				4	Disable Interrupt	
HLT		01001000	00111011			11	Halt	

Notes: * 1 :In the case of skip condition, the idle states are as follows:
1-byte instruction: 4 states 2-byte instruction (with *): 7 states
2-byte instruction: 8 states 3-byte instruction (with *): 10 states
3-byte instruction: 11 states 4-byte instruction (with *): 14 states
* 2 : B2 (Data):rpa2 = D + byte. H + byte.
* 3 : Right side of slash (/) in states indicate case rpa2, rpa3 = D + byte, H + A, H + B, H + EA, H + byte.
* 4 : B3 (Data): rpa3 = D + byte, H + byte.

Emulating the μPD7811

To emulate the μPD7811: tie MODE0 to ground and pull up MODE1 through a 10-kΩ resistor; insert a 2732A or 2764 into the upper terminals of the μPD78PG11. If a 2732 is used it should be inserted so that pin 1 of the 2732A goes into terminal 3 (see pin configuration). If a 2764 is used, address line A_{12} will be held low so that only memory locations 0-OFFFH (the lower 4K bytes) of the 2764 will be accessed. This simulates accessing 4K bytes of masked-ROM in the μPD7811. In other respects μPD78PG11 is functionally equivalent to μPD7811.

Input/Output

8 Analog Input Lines
44 Digital I/O Lines: five 8-bit ports (Port A, Port B, Port C, Port D, Port F) and 4 input lines (AN_4-AN_7)

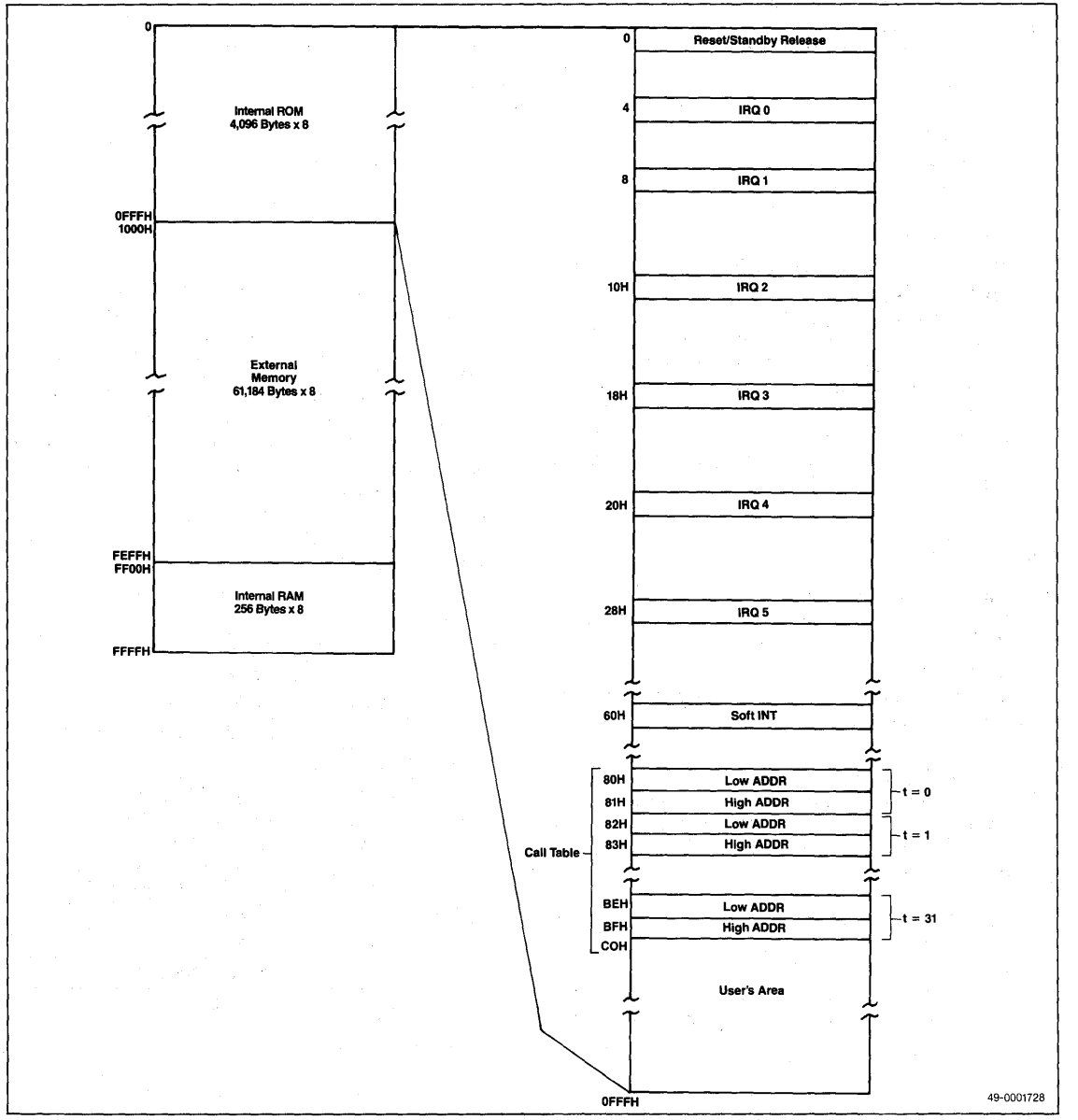
1. Analog Input Lines
   AN_0-AN_7 are configured as analog input lines for on-chip A/D converter.
2. Port Operation
   —Port A, Port B, Port C, Port F
   Each line of these ports can be individually programmed as an input or as an output. When used as I/O ports, all have latched outputs, high-impedance inputs.
   —Port D
   Port D can be programmed as a byte input or a byte output.
   —AN_4-AN_7
   The high-order analog input lines, AN_4-AN_7 can be used as digital input lines for falling edge detection.
3. Control Lines
   Under software control, each line of Port C can be configured individually to provide control lines for serial interface, timer, and timer/event counter.
4. Memory Expansion
   In addition to the single-chip operation mode, μPD78PG11 has 4 memory expansion modes. Under software control, Port D can provide multiplexed low-order address and data bus and Port F can provide high-order address bus. The relation between memory expansion modes and the pin configurations of Port D and Port F is shown in the table that follows.

Memory Expansion	Port Configuration	
None	Port D	I/O Port
	Port F	I/O Port
256 Bytes	Port D	Multiplexed Address/Data Bus
	Port F	I/O Port
4K Bytes	Port D	Multiplexed Address/Data Bus
	Port F_0 — F_3	Address Bus
	Port F_4 — F_7	I/O Port
16K Bytes	Port D	Multiplexed Address/Data Bus
	Port F_0 — F_5	Address Bus
	Port F_6 — F_7	I/O Port
60K Bytes	Port D	Multiplexed Address/Data Bus
	Port F	Address Bus

Memory Map

The μPD78PG11 can directly address up to 64K bytes of memory. Except for the EPROM (0-4,095) and RAM (65,280-65,535), any memory location can be used as ROM or RAM. The following memory map defines the 0-64K-byte memory space for the μPD78PG11.

Memory Map



Timers

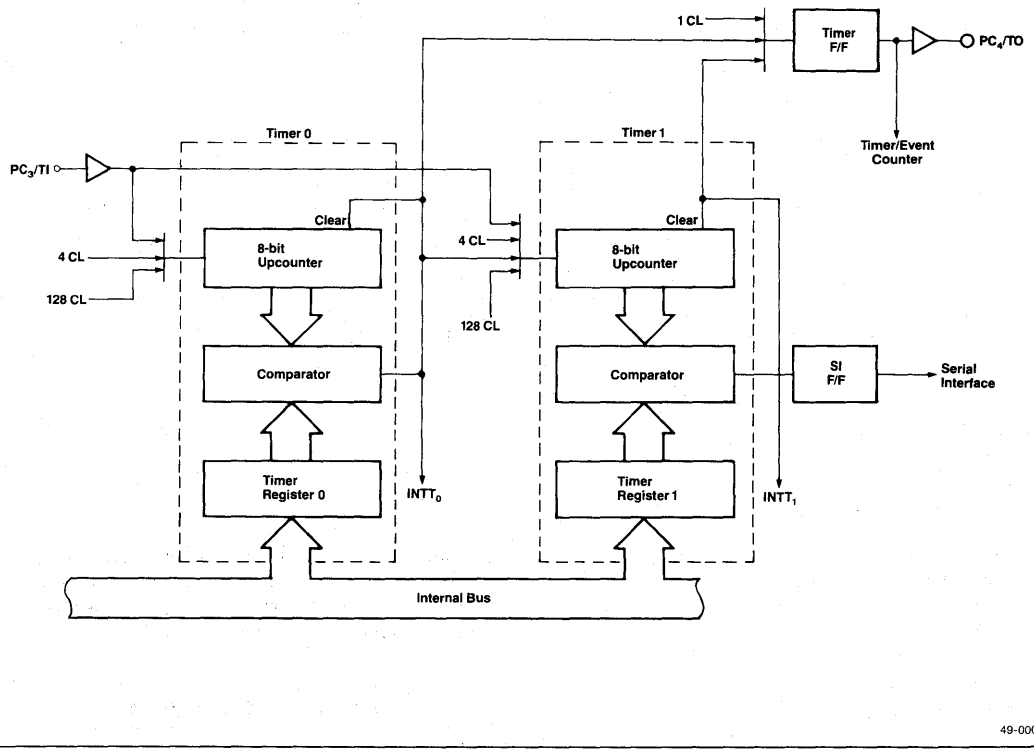
The timer/event counter consists of two 8-bit timers. The timers may be programmed independently or may be cascaded and used as a 16-bit timer. The timer can be set in software to increment at intervals of 4 machine cycles (1μs at 12MHz operation) or 128 machine cycles (32μs at 12MHz), or to increment on receipt of a pulse at T1.

Timer/Event Counter

The 16-bit multifunctional timer/event counter can be used for the following operations:

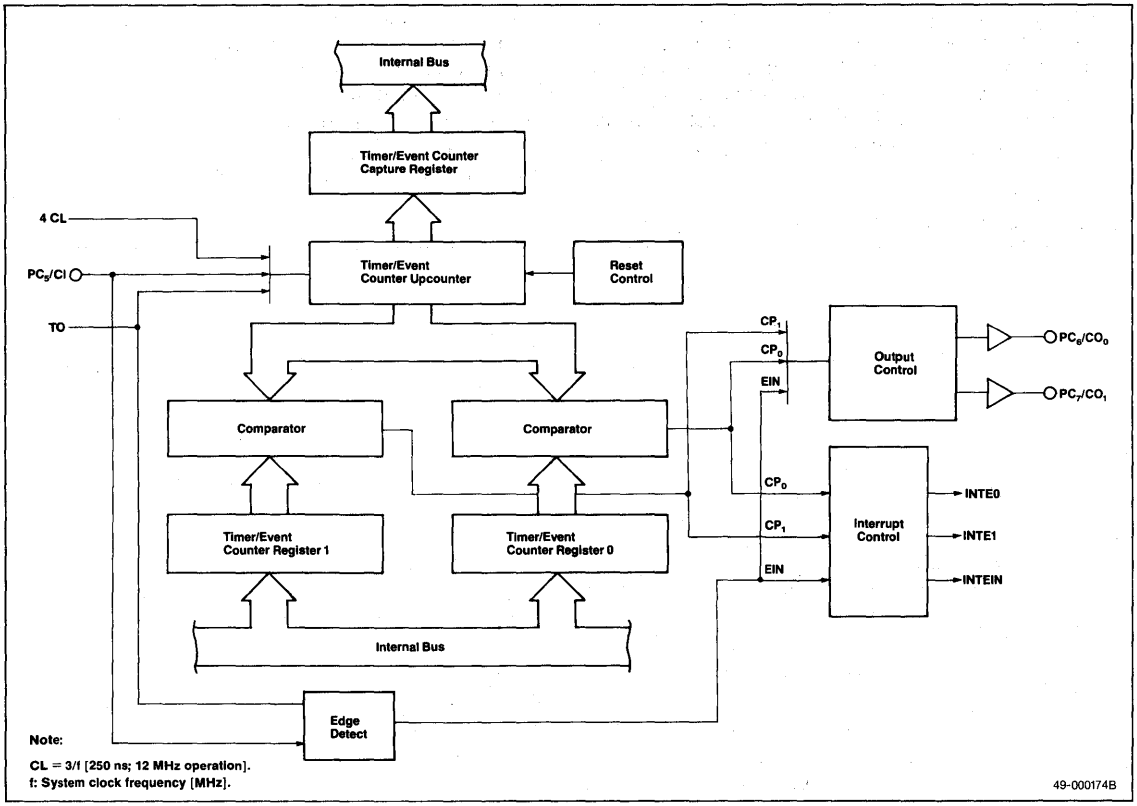
- ☐ Interval timer
- ☐ External event timer
- ☐ Frequency measurement
- ☐ Pulse width measurement
- ☐ Programmable square-wave output

Timer Block Diagram



4

Block Diagram for Timer/Event Counter



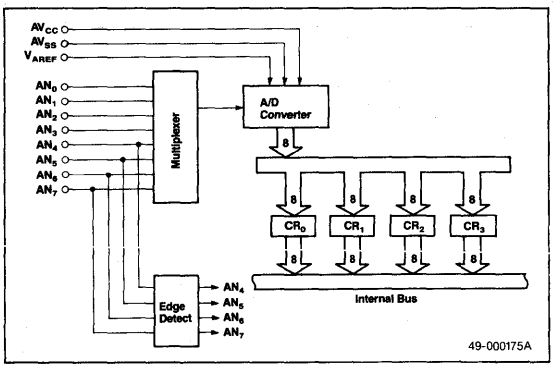
8-Bit A/D Converter

- 8 input channels
- 4 conversion result registers
- 2 powerful operation modes
  - —Autoscan mode
  - —Channel select mode
- Successive approximation technique
- Absolute accuracy: ±1.5 LSB (±0.6%)
- Conversion range: 0V to 5V
- Conversion time: 50μs
- Interrupt generation

Analog/Digital Converter

The μPD78PG11 features an 8-bit, high-speed, high-accuracy A/D converter. The A/D converter consists of a 256-resistor ladder and a successive approximation register (SAR). There are four conversion result registers (CR_0-CR_3). The 8-channel analog input may be operated in either of two modes. In the select mode, the conversion value of one analog input is sequentially stored in CR_0-CR_3. In the scan mode, the upper four channels or the lower four channels may be specified. Then those four channels will be consecutively selected and the conversion results stored sequentially in the four conversion result registers.

A/D Converter Block Diagram

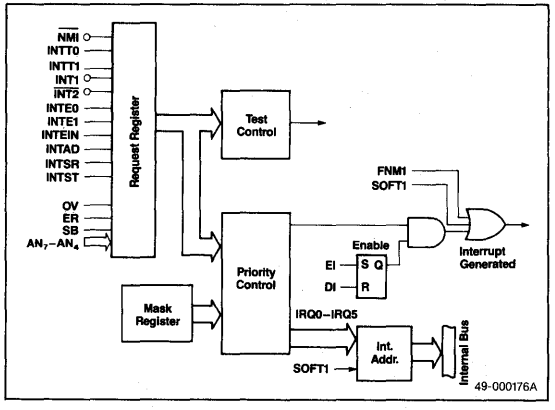


Interrupt Structure

There are 11 interrupt sources. Three are external interrupts and 8 are internal. These 11 interrupt sources are divided into 6 priority levels as shown in the table below.

Interrupt Request	Interrupt	Type of Interrupt		In/Ext
IRQ0	4	$\overline{NMI}$	(Nonmaskable interrupt)	External
IRQ1	8	INTT0	(Coincidence signal from timer 0)	Internal
		INTT1	(Coincidence signal from timer 1)	
IRQ2	16	INT1	(Maskable interrupt)	External
		$\overline{INT2}$	(Maskable interrupt)	
IRQ3	24	INTE0	(Coincidence signal from timer/event counter)	Internal
		INTE1	(Coincidence signal from timer/event counter)	
IRQ4	32	INTEIN	(Falling signal of C1 and T0 counter)	In/External
		INTAD	(A/D converter interrupt)	
IRQ5	40	INTSR	(Serial receive interrupt)	Internal
		INST	(Serial send interrupt)	

Interrupt Structure Block Diagram



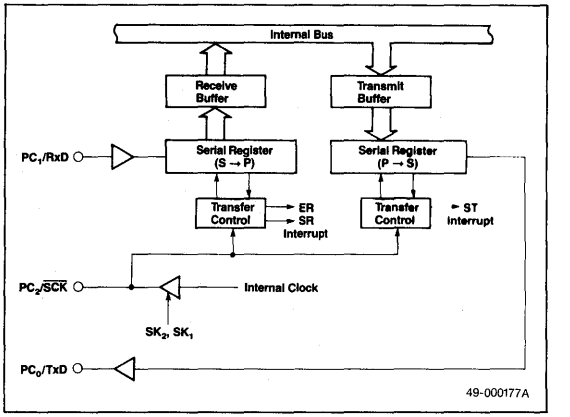
Standby Function

The μPD78PG11 offers a standby function that allows the user to save up to 32 bytes of RAM with backup power (V_{DD}) if the main power (V_{CC}) fails. On powerup the μPD78PG11 checks whether recovery was made from standby mode or from cold start.

Universal Serial Interface

The serial interface can operate in any of three modes: synchronous, asynchronous, and I/O interface. The I/O interface mode transfers data MSB first for ease of communication with certain peripheral devices. Synchronous and asynchronous modes transfer data LSB first. Synchronous operation offers two modes of data reception. In the search mode, data is transferred one bit at a time from serial register to receive buffer. This allows a software search for a sync character. In the nonsearch mode, data transfer from serial register to transmit buffer occurs 8 bits at a time.

Universal Serial Interface Block Diagram



Zero-crossing Detector

The INT1 and $\overline{INT2}$ terminals (used common to TI and PC_3) can be used to detect the zero-crossing point of slow moving AC signals. When driven directly, these pins respond as a normal digital input.

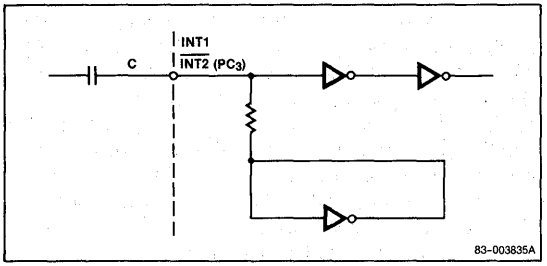
To utilize the zero-cross detection mode, an AC signal of approximately 1—3V AC peak-to-peak magnitude and a maximum frequency of 1kHz is coupled through an external capacitor to these pins.

For the INT1 pin, the internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one and INT1 interrupt is generated.

For the $\overline{INT2}$ pin, the state is sensed as a one until the falling edge crosses the DC average level, when it becomes a zero and $\overline{INT2}$ interrupt is generated.

The zero-cross detection capability allows the user to make the 50-60Hz power signal the basis for system timing and to control voltage phase sensitive devices.

Zero-Crossing Detection Circuit



Operand Format/Description

Format	Description
r	V, A, B, C, D, E, H, L
r1	EAH, EAL, B, C, D, E, H, L
r2	A, B, C
sr	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, SML, EOM, ETMM, TMM, MM, MCC, MA, MB, MC MF, TxB, TM_0, TM_1
sr1	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM, RxB, CR_0, CR_1, CR_2, CR_3
sr2	PA, PB, PC, PD, PF, MKH, MKL, ANM, SMH, EOM, TMM
sr3	ETM_0, ETM_1
sr4	ECNT, ECPT
rp	SP, B, D, H
rp1	V, B, D, H, EA
rp2	SP, B, D, H, EA
rp3	B, D, H
rpa	B, D, H, D+, H+, D-, H-
rpa1	B, D, H
rpa2	B, D, H, D+, H+, D-, H-, D+byte, H+A , H+B, H+EA, H+byte
rpa3	D, H, D+, H++, D+byte, H+A, H+B, H+EA, H+byte
wa	8-bit immediate data
word	16-bit immediate data
byte	8-bit immediate data
bit	3-bit immediate data
f	CY, HC, Z
irf	FNMI, FTO, FT1, F1, F2, FEO, FE1, FEIN, FAD, FSR, FST, ER, OV, AN_4, AN_5, AN_6, AN_7, SB

μPD78310/312
8-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS, REAL-TIME CONTROL ORIENTED

Description

The μPD78310 and μPD78312 microcomputers are designed for use in process control. They perform all the usual process control functions and are particularly well-suited for driving dc motors in servo loops and stepping motors. The processor includes on-chip memory, timers, input/output registers, and a powerful interrupt handling facility. The μPD78310/312 is constructed of high-speed CMOS circuitry and operates from a +5 V power supply.

The input frequency (maximum 12 MHz) is derived from an external crystal or an external oscillator. The internal processor clock is two-phase, and thus machine states are executed at a rate of 6 MHz. The shortest instructions require three states, making the minimum time 500 ns. The CPU contains a three-byte instruction prefetch queue which allows a subsequent instruction to be fetched during execution of an instruction that does not reference memory.

Program memory is 8K bytes of mask-programmable ROM (μPD78312 only), and data memory is 256 bytes of static RAM. The μPD78310 is the ROM-less version.

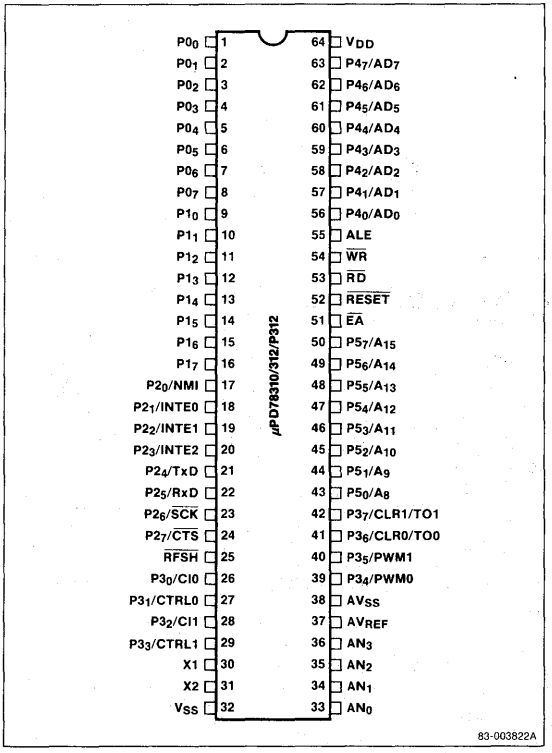
Note: μPD78P312, available in 3Q86, is a prototyping chip for μPD78312. It has an on-chip 8K EPROM instead of a mask ROM.

Features

- ☐ Complete single-chip microcomputer
  - — 16-bit ALU
  - — 8K ROM (μPD78312 only)
  - — 256 bytes RAM
  - — 1-bit and 8-bit logic
- ☐ Instruction prefetch queue
- ☐ 16-bit unsigned multiply and divide
- ☐ String instructions
- ☐ Memory expansion
- ☐ — 8085A bus-compatible
  - — Total 64K address space
- ☐ Large I/O capacity
  - — Up to 32 I/O port lines
- ☐ Extensive timer/counter system
  - — Two 16-bit up/down counters
  - — Two 16-bit timers
  - — Free running counter with two 16-bit capture registers
  - — Pulse-width modulated outputs
  - — Timebase counter
- ☐ Four-channel 8-bit A/D converter
- ☐ Two 4-bit real-time output ports
- ☐ Two nonmaskable interrupts
- ☐ Eight hardware priority interrupt levels
- ☐ Macro service facility for interrupts
  - — Gives the effect of 8 DMA channels
- ☐ Bidirectional serial port
  - — Either UART or interface mode
  - — Dedicated baud rate generator
- ☐ Watchdog timer
- ☐ Refresh output for pseudostatic RAM
- ☐ Programmable HALT and STOP modes
- ☐ One-byte call instruction
- ☐ On-chip clock generator
- ☐ CMOS silicon gate technology
- ☐ +5 V power supply

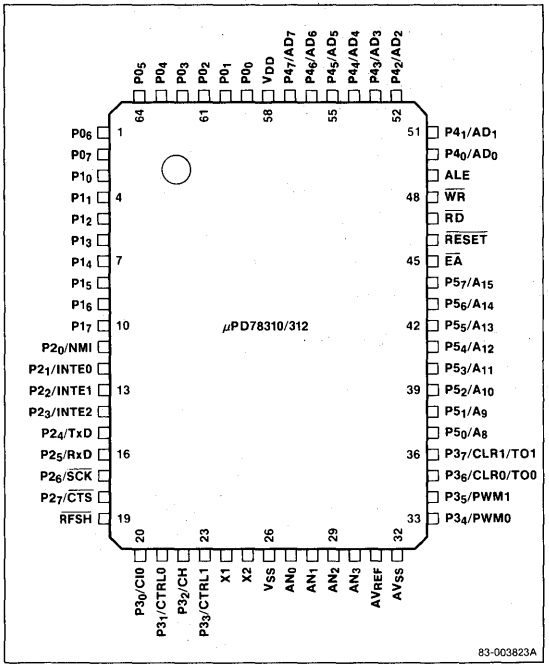
Pin Configurations

64-Pin DIP and QUIP



Pin Configurations (cont)

64-Pin Miniflat



Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD78310CW μPD78312CW	64-pin plastic shrink DIP	12 MHz
μPD78310G-36 μPD78312G-36 μPD78P312G-36	64-pin plastic QUIP	12 MHz
μPD78310G-1B μPD78312G-1B	64-pin plastic miniflat	12 MHz
μPD78310L μPD78312L	68-pin PLCC	12 MHz

Pin Identification

Symbol	Function
$P0_0$-$P0_7$	I/O port 0
$P1_0$-$P1_7$	I/O port 1
$P2_0$/NMI	Nonmaskable interrupt input
$P2_1$-$P2_3$/INTE0-INTE2	Maskable interrupt inputs
$P2_4$/TxD	I/O port 2/Serial transmit output
$P2_5$/RxD	I/O port 2/Serial transmit output
$P2_6$/$\overline{SCK}$	I/O port 2/Serial clock output

Pin Identification (cont)

Symbol	Function
$P2_7$/$\overline{CTS}$	I/O port 2/Clear to send input
$\overline{RFSH}$	Refresh output
$P3_0$/CI0	Up/down counter 0 input
$P3_1$/CTRL0	Up/down counter 0 control input
$P3_2$/CI1	Up/down counter 1 input
$P3_3$/CTRL1	Up/down counter 1 control input
X1	External crystal/External clock input
X2	External crystal
V_{SS}	Power return
AN_0-AN_3	A/D converter inputs
AV_{REF}	A/D reference voltage
AV_{SS}	Analog ground
$P3_4$/PWM0	I/O port 3/Pulse width modulated output 0
$P3_5$/PWM1	I/O port 3/Pulse width modulated output 1
$P3_6$/CLR0/T00	I/O port 3/Counter 0 clear input/Timer 0 output
$P3_7$/CLR1/T01	I/O port 3/Counter 1 clear input/Timer 1 output
$P5_0$-$P5_7$/A_8-A_{15}	I/O port 5/High address byte output
$\overline{EA}$	External access control input
$\overline{RESET}$	External reset input
$\overline{RD}$	Read strobe output
$\overline{WR}$	Write strobe output
ALE	Address latch enable output
$P4_0$-$P4_7$/AD_0-AD_7	I/O port 4/External address/Data bus
V_{DD}	Power supply

Pin Functions

$P0_0$-$P0_7$ [Port 0]

Port 0 consists of 8 bits, individually programmable for input/output or two 4-bit real-time (timer controlled) output ports.

$P1_0$-$P1_7$ [Port 1]

Port 1 consists of 8 bits, individually programmable for input/output.

$P2_0$/NMI

Port $P2_0$ is dedicated to NMI, the nonmaskable external interrupt request.

$P2_1$-$P2_3$/INTE0-INTE2

Ports $P2_1$-$P2_3$ are dedicated to INTE0, INTE1, and INTE2, the maskable external interrupt requests.

$P2_4$/TxD

$P2_4$ is an I/O port bit or the transmitted serial data output.

$P2_5$/RxD

$P2_5$ is an I/O port bit or the received serial data input.

$P2_6$/$\overline{SCK}$

$P2_6$ is an I/O port bit or the serial shift clock output.

$P2_7$/$\overline{CTS}$

$P2_7$ is an I/O port bit or clear-to-send input (external serial transmission control) in the asynchronous communication mode. In the serial I/O interface mode, it becomes the serial receive clock I/O pin.

$\overline{RFSH}$

$\overline{RFSH}$ is the refresh pulse output to be used for external pseudostatic DRAM.

$P3_0$/CI0

Port $P3_0$ is dedicated to CI0, the external count input for up/down counter 0.

$P3_1$/CTRL0

Port $P3_1$ is dedicated to CTRL0, the external control input for up/down counter 0.

$P3_2$/CI1

Port $P3_2$ is dedicated to CI1, the external count input for up/down counter 1.

$P3_3$/CTRL1

Port $P3_3$ is dedicated to CTRL1, the external control input for up/down counter 1.

X1

X1 is the external oscillator input or one of the connections for an external crystal. It is used to generate the system clock. The system clock frequency is half the input frequency.

X2

X2 is the second connection for an external crystal.

V_{SS}

V_{SS} is the power supply return, normally ground.

AN_0-AN_3

AN_0-AN_3 are the four program selectable input channels for the A/D converter.

AV_{REF}

AV_{REF} is the reference voltage input for the A/D converter.

AV_{SS}

AV_{SS} is the analog ground pin.

$P3_4$/PWM0

$P3_4$ is an I/O port bit or the pulse-width modulated output 0.

$P3_5$/PWM1

$P3_5$ is an I/O port bit or the pulse-width modulated output 1.

$P3_6$/CLR0/TO0

$P3_6$ is an I/O port bit, or the clear input for up/down counter 0, or the timer 0 flip-flop output.

$P3_7$/CLR1/TO1

$P3_7$ is an I/O port bit, or the clear input for up/down counter 1, or the timer 1 flip-flop output.

$P5_0$-$P5_7$/A_8-A_{15} [Port 5]

Port 5 consists of 8 bits, individually programmable for input or output, or the high-order address bits for external memory. Under control of the memory mask register, bits $P5_0$-$P5_3$ are used for 4K memory expansion, bits $P5_0$-$P5_5$ are used for 16K memory expansion, or bits $P5_0$-$P5_7$ are used for 56K memory expansion.

$\overline{EA}$ [External Access]

On μPD78312, a low on $\overline{EA}$ enables use of external memory in place of on-chip ROM. The $\overline{EA}$ pin must be low on μPD78310.

$\overline{RESET}$

This pin is used for the external reset input. A low level sets all registers to their specified reset values.

$\overline{RD}$

$\overline{RD}$ is the read strobe output. It is to be used by external memory (or data registers) to place data on the I/O bus during a read operation.

$\overline{WR}$

$\overline{WR}$ is the write strobe output. It is to be used by external memory (or data registers) to latch data from the I/O bus during a write operation.

ALE

ALE is the address latch enable. It is to be used by external circuitry to latch the low-order 8 address bits during the first part of a read or write cycle.

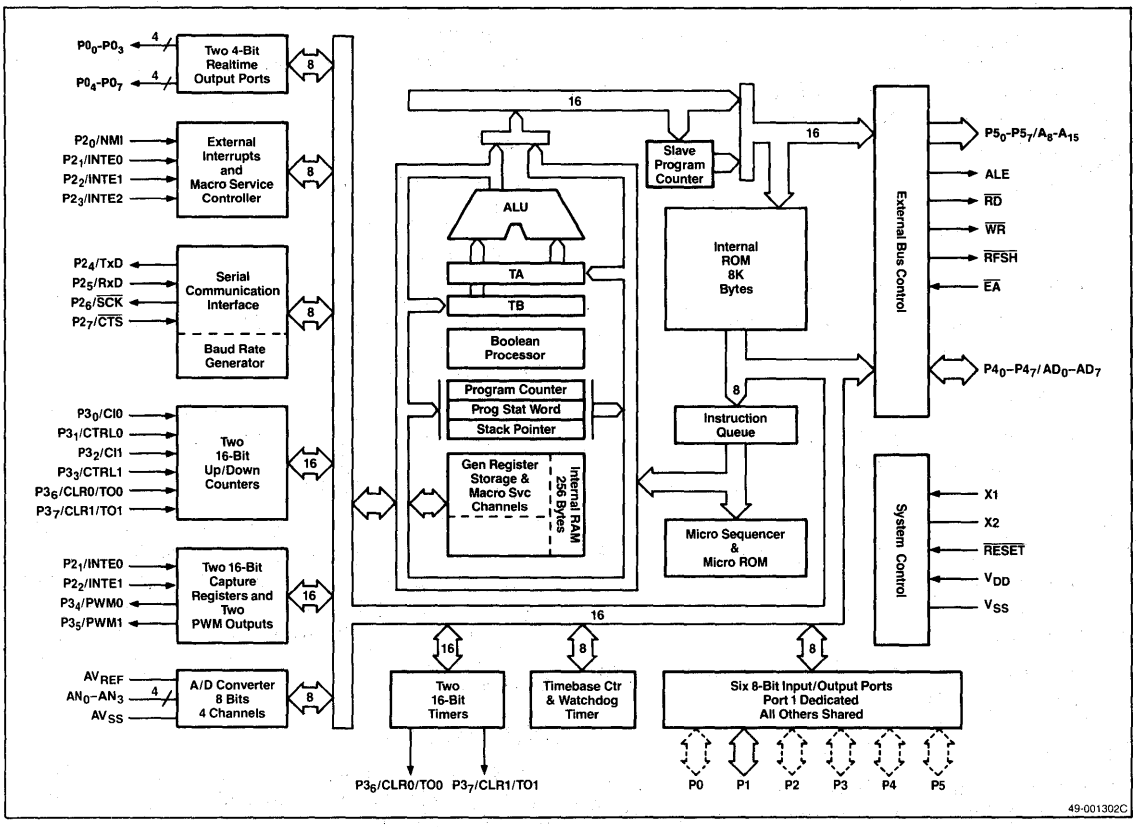
$P4_0$-$P4_7$/AD_0-AD_7 [Port 4]

Port 4 consists of 8 bits, programmable as a unit for input or output, or as the multiplexed address/data bus if external memory or external interface circuitry is used. The port is controlled by the memory mapping register.

V_{DD}

V_{DD} is the positive power supply input.

Block Diagram



Functional Description

On-chip features designed to facilitate process control include two 16-bit timers, two 16-bit up/down counters, two pulse-width modulated outputs, a free-running counter with two capture registers, two 4-bit real-time (timer controlled) output ports, an 8-bit A/D converter with 4 input channels, a timebase counter to generate widely spaced interrupts, and a watchdog timer to guard against infinite program loops.

In addition there is a serial I/O port which can be used in either an interface mode or an asynchronous communication mode. HALT and STOP modes are provided to conserve power at times when the action of the CPU is not required.

All I/O, timer, and control registers are defined as special function registers and assigned addresses in the top 256 bytes of memory. The special function registers may be operated on directly by many of the arithmetic, logic, and move instructions of the CPU. Table 2 at the end of the Functional Description describes the registers.

Addressing

The μPD78310/312 features 1-byte addressing of the special function registers and 1-byte addressing of the internal RAM. There are nine modes of addressing main memory, including autoincrement, autodecrement, indexing, and double indexing. There are 8- and 16-bit immediate operands.

External Memory

External memory (figure 1) is supported by I/O port 4, an 8-bit multiplexed address/data bus. The memory mapping register controls the size of external memory as well as the number of additional wait states. High-order address bits are taken from I/O port 5 as required. No bits are required for 256 bytes of external memory; bits $P5_0$-$P5_3$ are used for 4K bytes, $P5_0$-$P5_5$ for 16K bytes, and $P5_0$-$P5_7$ for 56K bytes. Any remaining port 5 bits are available for I/O.

Refresh

The μPD78310/312 has a refresh signal for use with the pseudostatic RAM. The refresh cycle can be set to one of four intervals ranging from 2.67 to 21.3 μs. The refresh is timed to follow a read or write operation so that the CPU does not have to wait.

General Registers

The CPU has 16 8-bit registers (figure 2) that can also be used in pairs to function as 16-bit registers. A complete set of 16 general registers is mapped into each of 8 program-selectable register banks, stored in RAM. Three bits in the PSW specify which of the register banks is active at any given time. Each register bank has two program-selectable accumulators.

Figure 1. Memory Map

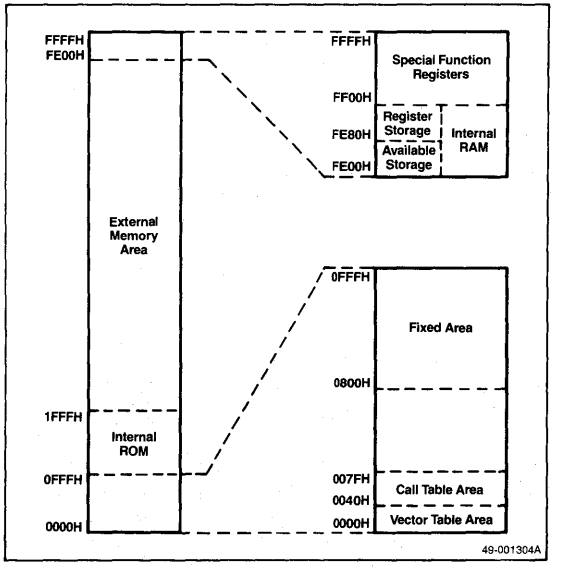
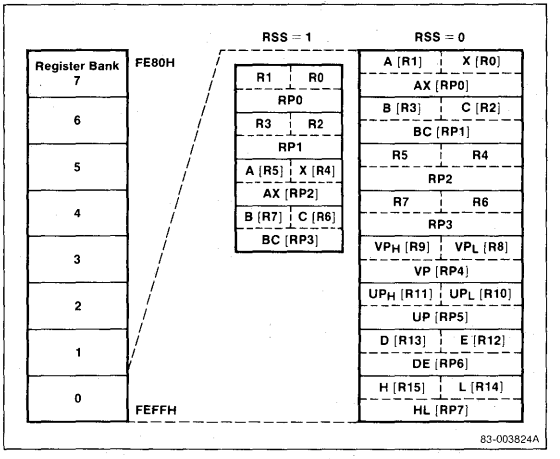


Figure 2. Register Designation and Storage



Program Status Word

Following is the program status word format.

15							8
0	RB_2	RB_1	RB_0	0	0	IE	0

7							0
S	Z	RSS	AC	UF	P/V	SUB	CY

RB_2-RB_0	Active register bank number
IE	Interrupt enable
S	Sign (1 if last result was negative)
Z	Zero (1 if last result was zero)
RSS	Register set select
AC	Auxiliary carry (carry out of 3 bit)
UF	User flag
P/V	Parity or arithmetic overflow
SUB	Subtract (1 if last operation was subtract)
CY	Carry

Input/Output

All ports may be used for either latched output or high-impedance input. All ports except port 4 are bit-programmable for input or output. Port 0 is used for real-time or normal I/O. Port 1 is used for normal I/O. The low nibble of ports 2 and 3 is always used for control and the high nibble for control or normal I/O. Port 4 is used for the external address/data bus or byte-programmable I/O. Port 5 is used for the high bits of the external address or for normal I/O.

Real-Time Output Port

The real-time output port shares pins with I/O port 0. The high and low nibbles are treated separately or together. Data is transferred from a buffer to the port latches on either a timer or software command.

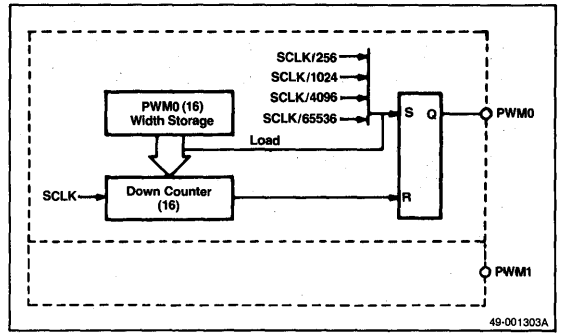
Serial Port

The serial port can operate in UART or interface mode with the baud rate and byte format under program control. The serial port also includes a dedicated baud rate generator.

Pulse-Width Modulated Outputs

The two independent pulse-width modulated outputs are controlled by two 16-bit modulus registers and counters. There are four programmable repetition rates ranging from 91.6 Hz to 23.4 kHz. Figure 3 shows one of these outputs.

Figure 3. Pulse-Width Modulated Output



Timers

The μPD78310/312 has two 16-bit timers. The inputs to these timers may be the internal clock divided by 6 or by 128. Each timer has an associated modulus register to store the timer count. The timer counts down to zero, sets a flag, reloads from the modulus register, and then counts down again. The timer flags can be used under program control to generate interrupt requests and/or a square-wave output. TM0 also functions optionally as two one-shot timers.

Figure 4 is a diagram of the interval timers.

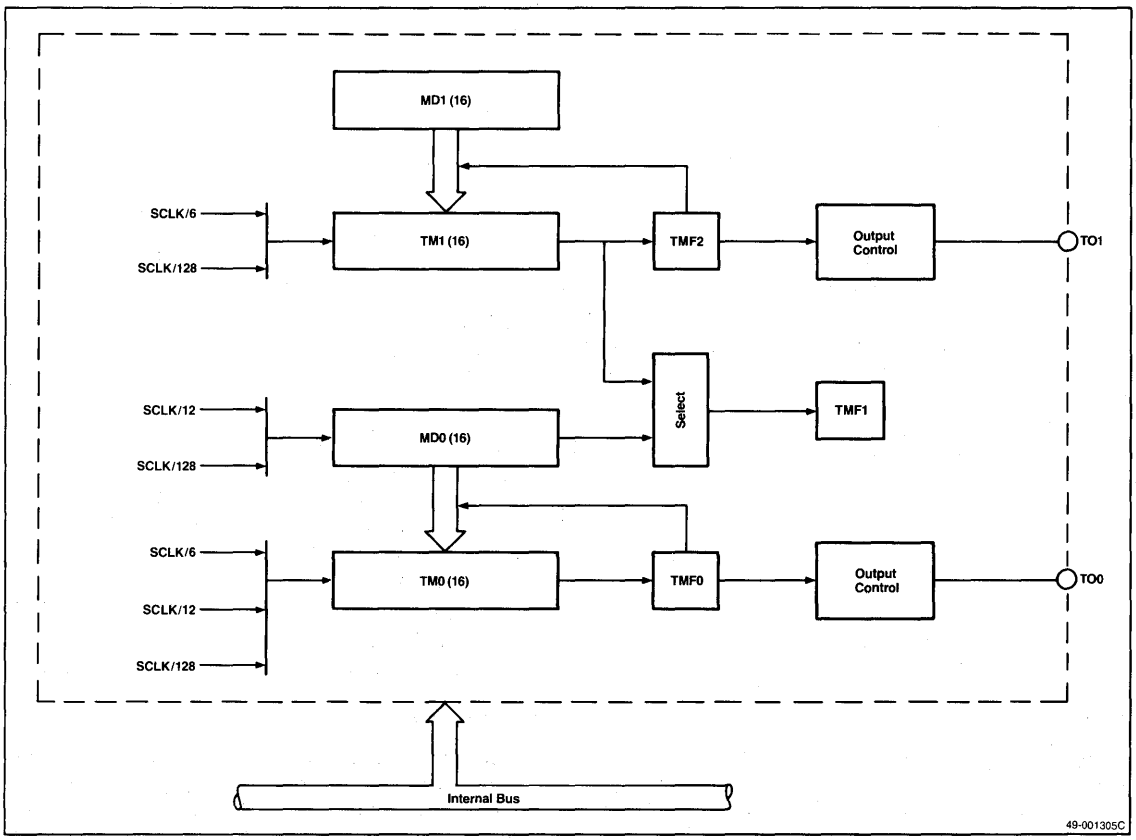
There is a free-running counter that counts the internal clock divided by 4 or by 16. The counter has two 16-bit capture registers. Capture is triggerd by an external interrupt request or by the up/down counter clock.

The timebase counter generates a signal at one of four intervals ranging from 170 μs to 175 ms. The signal can be used to generate an interrupt request and/or an up/down counter capture.

Up/Down Counters

The μPD78310/312 has two 16-bit up/down counters, each of which has two capture/compare registers. There are three modes of operation: compare and interrupt, capture on external command, and capture on timebase counter command. There are five sources of counts: the internal clock divided by 3, the external clock, external independent up and down inputs, external clock with direction control, and external clock with automatic up/down discrimination. Figure 5 shows an up/down counter.

Figure 4. Timer Block Diagram



Standby Modes

HALT and STOP modes conserve power when CPU action is not required. In HALT mode, the CPU stops and the clock continues to run. Maskable interrupts can restart the CPU.

In STOP mode, the CPU and clock are both stopped. A $\overline{\text{RESET}}$ pulse or the nonmaskable external interrupt is required to restart them.

There is also the option of slowing the system clock by a factor of four. The standby control register controls the standby modes and is a protected location written to only by a special instruction.

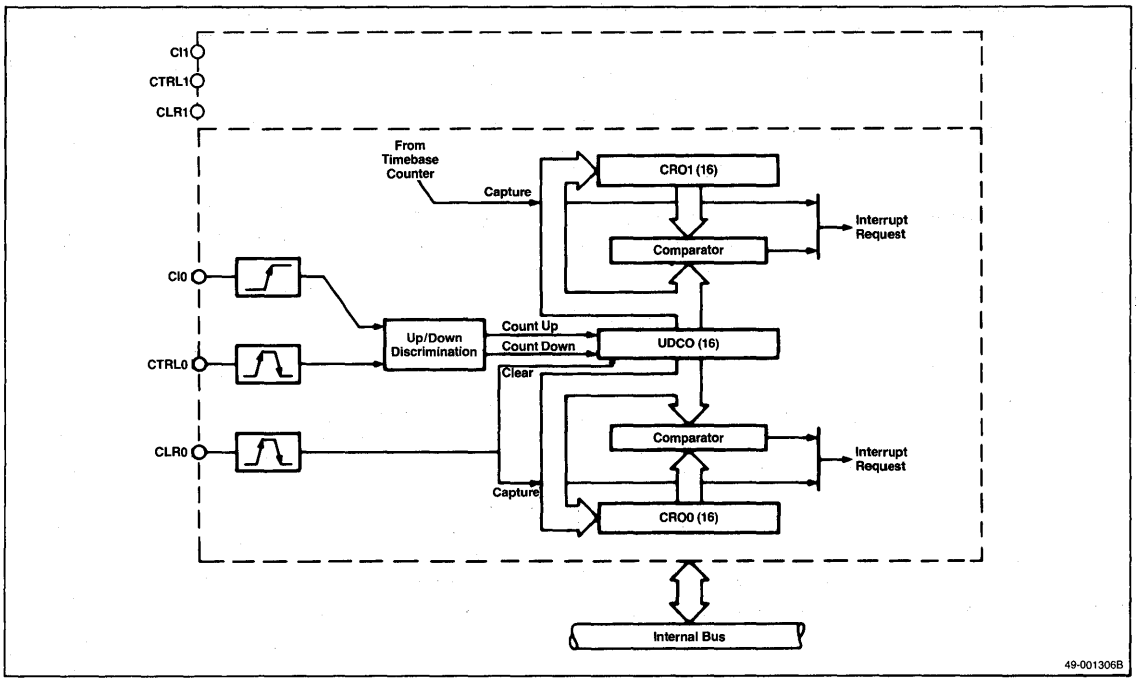
Watchdog Timer

The watchdog timer protects agains inadvertent program loops. A nonmaskable interrupt occurs if the timer is not reset before a timeout occurs. There are four program-selectable intervals ranging from −5.5 ms to 349.3 ms. The watchdog timer can be disabled by software. The watchdog timer mode register controls the watchdog timer and is a protected location written to by a special instruction.

A/D Converter

The A/D converter has four input channels and can operate in either scan or select mode. The A/D converter performs 8-bit successive approximation conversions, has a 30-μs conversion time, and is triggered either internally or externally. The A/D converter includes an on-chip sample and hold amplifier.

Figure 5. Up/Down Counter Block Diagram



Interrupts

There are two nonmaskable interrupt sources: the external nonmaskable interrupt and the watchdog timer. Their relative priorities are software selectable.

There are eight hardware priority interrupt levels, level 0 having the highest priority and level 7 the lowest. The fifteen maskable interrupt sources (table 1) are divided into five groups, and each group can, under program control, be assigned to any one of the priority levels.

Interrupts may be serviced by routines entered either by vectoring or by context switching. Context switching automatically saves all the general registers, the program status word, and the program counter. Figure 6 illustrates the mechanism of context switching.

Finally, there is an optional macro service function that transfers data between any one special function register and memory without program intervention.

Macro Service

The macro service controller can be programmed to perform word or byte transfers. It can transfer data from a special function register to memory or from memory to a special function register. Transfer events are triggered by interrupt requests and take place without software intervention.

There are eight macro service channels; channel control information is stored in RAM. This information (figure 7) consists of a 16-bit memory address (optionally incremented at each transfer), an 8-bit special function register designator, and an 8-bit transfer counter (decremented at each transfer.) When the count equals 0, a context switch or vectored interrupt occurs.

Table 1. Interrupt Sources and Vector Addresses

	Default Priority	Source	Interrupt Service	Macro Service	Vector
Nonmaskable interrupts	—	BRK	Break instruction	No	003EH
	—	NMI	External nonmaskable interrupt	No	0002H
	—	WDT	Watchdog timer	No	000AH
Maskable interrupts	0	CRF00	Up/down counter	Yes	001AH
	1	CRF01	Up/down counter	No	001CH
	2	CRF10	Up/down counter	Yes	001EH
	3	CRF11	Up/down counter	No	0020H
	4	EXIF0	External interrupt 0	Yes	0004H
	5	EXIF1	External interrupt 1	Yes	0006H
	6	EXIF2	External interrupt 2	Yes	0008H
	7	TIMF0	Timer flag 0	Yes	000EH
	8	TIMF1	Timer flag 1	Yes	0010H
	9	TIMF2	Timer flag 2	Yes	0012H
	10	SEF	Serial port error	No	0022H
	11	SRF	Serial port receive buffer	Yes	0024H
	12	STF	Serial port transmit buffer	Yes	0026H
	13	ADF	A/D converter done flag	Yes	0028H
	14	TBF	Timebase counter flag	No	000CH
	—	RESET	External reset line	—	0000H

Figure 6. Hardware Context Switching

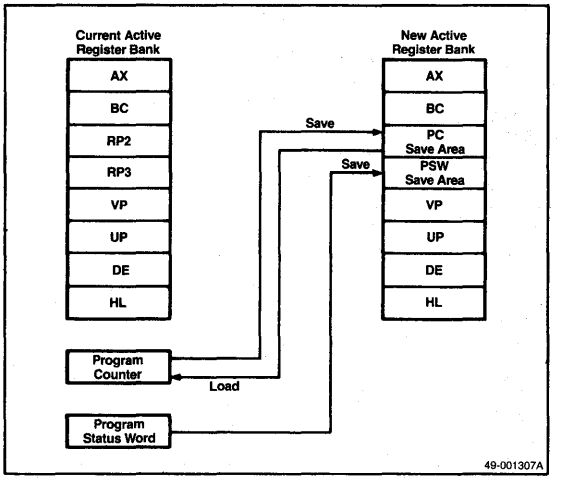


Figure 7. μPD78312 Macro Service Pointer Addresses

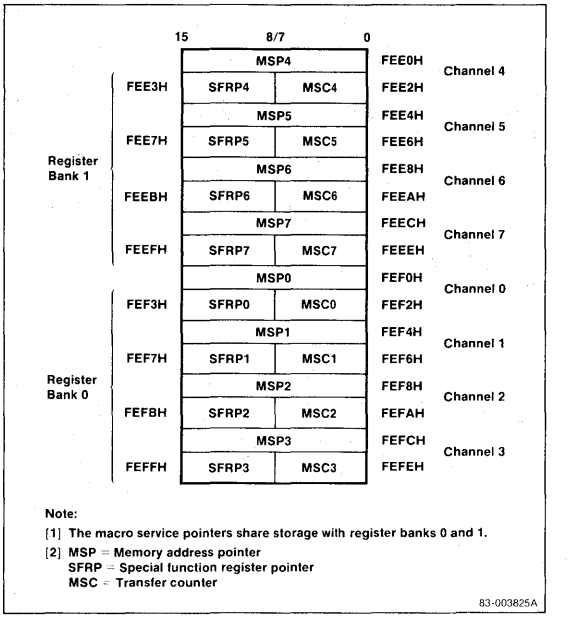


Table 2. Special Function Registers

Address	Function	Mnemonic	Read/ Write	16-Bit Transfer	Reset State
FF00H	I/O port 0	P0	R/W	No	Undefined
FF01H	I/O port 1	P1	R/W	No	Undefined
FF02H	I/O port 2	P2	R/W	No (Note 1)	Undefined
FF03H	I/O port 3	P3	R/W	No (Note 1)	Undefined
FF04H	I/O port 4	P4	R/W	No	Undefined
FF05H	I/O port 5	P5	R/W	No	Undefined
FF08H FF09H	Capture/compare register 00	CR00L CR00H	R/W	Yes	Undefined
FF0AH FF0BH	Capture/compare register 01	CR01L CR01H	R/W	Yes	Undefined
FF0CH FF0DH	Capture/compare register 10	CR10L CR10H	R/W	Yes	Undefined
FF0EH FF0FH	Capture/compare register 11	CR11L CR11H	R/W	Yes	Undefined
FF10H FF11H	Capture register 0 (from FRC)	CPT0L CPT0H	R/W	Yes	Undefined
FF12H FF13H	Capture register 1 (from FRC)	CPT1L CPT1H	R/W	Yes	Undefined
FF14H FF15H	PWM register 0 (duration)	PWM0L PWM0H	R/W	Yes	Undefined
FF16H FF17H	PWM register 1 (duration)	PWM1L PWM1H	R/W	Yes	Undefined
FF1CH FF1DH	Presettable up/down counter 0	UDC0L UDC0H	R/W	Yes	Undefined
FF1EH FF1FH	Presettable up/down counter 1	UDC1L UDC1H	R/W	Yes	Undefined
FF20H	Port 0 mode register	PM0	R/W	No	FFH
FF21H	Port 1 mode register	PM1	R/W	No	FFH
FF22H	Port 2 mode register	PM2	R/W	No	FFH
FF23H	Port 3 mode register	PM3	R/W	No	FFH
FF25H	Port 5 mode register	PM5	R/W	No	FFH
FF32H	Port 2 mode control register	PMC2	R/W	No	0FH
FF33H	Port 3 mode control register	PMC3	R/W	No	0FH
FF38H	Real-time output port control register	RTPC	R/W	No	08H

Table 2. Special Function Registers (cont)

Address	Function	Mnemonic	Read/ Write	16-Bit Transfer	Reset State
FF3AH FF3BH	Port 0 buffer register (Note 2)	P0L P0H	R/W R/W	No No	Undefined Undefined
FF40H	Memory mapping register	MM	R/W	No	30H
FF41H	Refresh mode register	RFM	R/W	No	10H
FF42H	Watchdog timer mode register	WDM	R/W	No	00H
FF44H	Standby control register	STBC	R/W	No	2nH (Note 3)
FF46H	Timebase mode register	TMB	R/W	No	00H
FF48H	Interrupt mode register	INTM	R/W	No	00H
FF4AH	In-service priority register	ISPR	R/W	No	00H
FF4EH	CPU control word	CCW	R/W	No	00H
FF50H	Serial communication mode register	SCM	R/W	No	00H
FF52H	Serial communication control register	SCC	R/W	No	00H
FF53H	Baud rate generator	BRG	R/W	No	00H
FF56H	Serial communication receive buffer	RXB	R	No	Undefined
FF57H	Serial communication transmit buffer	TXB	W	No	Undefined
FF60H	Free-running counter control register	FRCC	R/W	No	00H
FF64H	Capture mode register	CPTM	R/W	No	00H
FF66H	PWM mode register	PWMM	R/W	No	00H
FF68H	A/D converter mode register	ADM	R/W	No	00H
FF6AH	A/D converter result register	ADCR	R	No	Undefined
FF70H	Count unit input mode register	CUIM	R/W	No	00H
FF72H	Up/down counter control register 0	UDCC0	R/W	No	00H
FF74H	Capture/compare control register	CRC	R/W	No	00H
FF80H	Timer 0 control register	TMC0	R/W	No	00H
FF82H	Timer 1 control register	TMC1	R/W	No	00H
FF88H FF89H	Timer 0	TM0L TM0H	R/W	Yes	Undefined
FF8AH FF8BH	Modulus/timer register 0	MD0L MD0H	R/W	Yes	Undefined
FF8CH FF8DH	Timer 1	TM1L TM1H	R/W	Yes	Undefined
FF8EH FF8FH	Modulus register 1	MD1L MD1H	R/W	Yes	Undefined
FFB0H- FFBFH	External area (Note 4)				

Table 2. Special Function Registers (cont)

Address	Function		Mnemonic	Read/ Write	16-Bit Transfer	Reset State
FFC0H	Interrupt control 00	Up/down counter	CRIC00	R/W	No	47H
FFC1H	Macro service control 00	Up/down counter	CRMS00	R/W	No	Undefined
FFC2H	Interrupt control 01	Up/down counter	CRIC01	R/W	No	47H
FFC4H	Interrupt control 10	Up/down counter	CRIC10	R/W	No	47H
FFC5H	Macro service control 10	Up/down counter	CRMS10	R/W	No	Undefined
FFC6H	Interrupt control 11	Up/down counter	CRIC11	R/W	No	47H
FFC8H	EXIF0 interrupt control	External interrupt	EXIC0	R/W	No	47H
FFC9H	EXIF0 macro service control	External interrupt	EXMS0	R/W	No	Undefined
FFCAH	EXIF1 interrupt control	External interrupt	EXIC1	R/W	No	47H
FFCBH	EXIF1 macro service control	External interrupt	EXMS1	R/W	No	Undefined
FFCCH	EXIF2 interrupt control	External interrupt	EXIC2	R/W	No	47H
FFCDH	EXIF2 macro service control	External interrupt	EXMS2	R/W	No	Undefined
FFCEH	TMF0 interrupt control	Timer flag	TMIC0	R/W	No	47H
FFCFH	TMF0 macro service control	Timer flag	TMMS0	R/W	No	Undefined
FFD0H	TMF1 interrupt control	Timer flag	TMIC1	R/W	No	47H
FFD1H	TMF1 macro service control	Timer flag	TMMS1	R/W	No	Undefined
FFD2H	TMF2 interrupt control	Timer flag	TMIC2	R/W	No	47H
FFD3H	TMF2 macro service control	Timer flag	TMMS2	R/W	No	Undefined
FFDAH	Error interrupt control	Serial port	SEIC	R/W	No	47H
FFDCH	Receive interrupt control	Serial port	SRIC	R/W	No	47H
FFDDH	Receive macro service control	Serial port	SRMS	R/W	No	Undefined
FFDEH	Transmit interrupt control	Serial port	STIC	R/W	No	47H
FFDFH	Transmit macro service control	Serial port	STMS	R/W	No	Undefined
FFE0H	A/D converter interrupt control		ADIC	R/W	No	47H
FFE1H	A/D converter macro service control		ADMS	R/W	No	Undefined
FFE2H	Timebase counter interrupt control		TBIC	R/W	No	47H
FFFCH FFFDH	Stack pointer (Note 5)		SPL SPH	R/W	Yes	Undefined
FFFEH FFFFH	Program status word (Note 5)		PSWL PSWH	R/W	Yes	00H

Note:

(1) Bits 0-3 of port 2 and port 3 are read-only.

(2) P0H and P0L are 4-bit buffer registers used to store data to be loaded into the high and low nibbles of the real-time output (P0).

(3) Bit 3 of the STBC is not affected by RESET (n = 0 or 8).

(4) External registers interfaced with these addresses can be accessed by special function register addressing.

(5) SP and PSW do not have real SFR addresses and can be accessed only by special instructions.

Instruction Set

The instruction set for the μPD78310/312 has 8- and 16-bit arithmetic instructions including a 16 x 16-bit unsigned multiply with a 32-bit product and a 32 by 16-bit unsigned divide with a 32-bit quotient and a 16-bit remainder. The instruction set also excutes an 8-bit and a 16-bit shift and rotate by count, 1- and 8-bit logic, and 1-, 2-, and 3-byte call instructions. String manipulation instructions are also included.

There are four addressing modes for unconditional branching. Branch instructions exist to test single bits in the program status word, the 16-bit accumulator, the special function registers, and internal RAM. The instruction set also includes multiple register PUSH and POP instructions.

Following are several tables explaining symbols, designations, and codes in the Instruction Set. Machine codes are omitted from the instructions but they are in the User's Manual.

Symbols in the Operand and Operation Columns

Symbol	Meaning
r	R0-R15
r1	R0-R7
r2	C,B
rp	RP0-RP7*
rp1	RP0-RP7*
rp2	DE, HL, VP, UP
sfr	Special function register, 8 bits
sfrp	Special function register, 16 bits
post	RP0, RP1, RP2, RP3, RP4, RP5/PSW, RP6, RP7 Bits set to 1 indicate register pairs to be pushed/popped to/from the stack RP5 pushed/popped by PUSH/POP: SP is stack pointer PSW pushed/popped by PUSHU/POPU: RP5 is stack pointer
mem	(DE), (HL), (DE+), (HL+), (DE−), (HL−), (VP), (UP); register indirect (DE + A), (HL + A), (DE + B), (HL + B), (VP + DE), (VP + HL); base/index mode (DE + byte), (HL + byte), (VP + byte), (UP + byte), (SP + byte); base mode Word (A), word (B), word (DE), word (HL); index mode
saddr	FF20H-FF1FH: immediate byte addresses one byte in RAM, or label
saddrp	FE20H-FF1FH: immediate byte (bit 0 = 0) addresses one word in RAM
word	16 bits of immediate data
byte	8 bits of immediate data
jdisp	8-bit two's complement displacement (immediate data)
bit	3 bits of immediate data (bit position in byte), or label
n	3 bits of immediate data
addr16	0000H-FEFFH: 16-bit immediate address (up to FFFFH in MOV instruction)
!addr16	0000H-FEFFH: 16-bit absolute branch address (immediate data)
$addr16	Relative branch address ((PC)+jdisp))
addr11	0800H-0FFFH: 0800H+ (11-bit immediate address), or label
addr5	0040H-007EH: 0040H + 2 x (5-bit immediate address), or label

Symbols in the Operand and Operation Columns (cont)

Symbol	Meaning
A	A register (8-bit accumulator)
X	X register
B	B register
C	C register
D	D register
E	E register
H	H register
L	L register
R0-R15	Register 0-15
AX	Register pair AX (16-bit accumulator)
BC	Register pair BC
DE	Register pair DE
HL	Register pair HL
RP0-RP7	Register pair 0-7
PC	Program counter
SP	Stack pointer
UP	User stack pointer (RP5)
PSW	Program status word
CY	Carry flag
AC	Auxiliary carry flag
Z	Zero flag
P/V	Parity/overflow flag
S	Sign flag
SUB	Subtract flag
TPF	Table position flag
RBS	Register bank select flag
RSS	Register set select flag
IE	Interrupt enable flag
EOS	End of software interrupt flag
STBC	Standby control register
WDM	Watchdog timer mode register
( )	Contents of the location whose address is within ( ); (+) and (−) indicate that the address is incremented after or decremented before it is used.
(( ))	Contents of the memory location defined by the contents of the location defined by the quantity within the (( )).
XXH	Hexadecimal number
XH, XL	High-order 8 bits and low-order 8 bits of X

* rp and rp1 describe the same registers, but generate different machine code.

Flag Indicators

Symbol	Meaning
(blank)	No change
0	Cleared to 0
1	Set to 1
X	Set or cleared according to result
P	Parity of result
V	Arithmetic overflow
U	Undefined
R	Restored from saved PSW

Execution Times of Memory Reference Instructions: Number of Processor States

Instruction		Memory Reference Mode: Register Indirect	Base Index	Base	Index
MOV	A, mem	5	6	6	6
	mem, A				
XCH	A, mem	7	8	8	8
	mem, A				
ADD, ADDC, SUB, SUBC, AND, OR, XOR	A, mem	6	7	7	7
	mem, A	7	8	8	8
CMP	A, mem	6	7	7	7
	mem, A				

Memory Addressing Modes

	mod	1 0110	1 0111	0 0110	0 1010
mem		Register Indirect	Base Index	Base	Index
0 0 0		(DE+)*	(DE + A)	(DE + byte)	word (DE)
0 0 1		(HL+)*	(HL + A)	(SP + byte)	word (A)
0 1 0		(DE−)*	(DE + B)	(HL + byte)	word (HL)
0 1 1		(HL−)*	(HL + B)	(UP + byte)	word (B)
1 0 0		(DE)*	(VP + DE)	(VP + byte)	—
1 0 1		(HL)*	(VP + HL)	—	—
1 1 0		(VP)	—	—	—
1 1 1		(UP)	—	—	—

*1-byte instructions: defined by special opcode and mem only.

General Register Designations

r, r1

R3	R2	R1	R0	reg	
0	0	0	0	R0	r1
0	0	0	1	R1	
0	0	1	0	R2	
0	0	1	1	R3	
0	1	0	0	R4	
0	1	0	1	R5	
0	1	1	0	R6	
0	1	1	1	R7	
1	0	0	0	R8	r
1	0	0	1	R9	
1	0	1	0	R10	
1	0	1	1	R11	
1	1	0	0	R12	
1	1	0	1	R13	
1	1	1	0	R14	
1	1	1	1	R15	

r2

C	reg
0	C
1	B

rp

P2	P1	P0	reg-pair
0	0	0	RP0
0	0	1	RP1
0	1	0	RP2
0	1	1	RP3
1	0	0	RP4
1	0	1	RP5
1	1	0	RP6
1	1	1	RP7

rp1

Q2	Q1	Q0	reg-pair
0	0	0	RP0
0	0	1	RP4
0	1	0	RP1
0	1	1	RP5
1	0	0	RP2
1	0	1	RP6
1	1	0	RP3
1	1	1	RP7

rp2

S1	S0	reg-pair
0	0	VP
0	1	UP
1	0	DE
1	1	HL

Instruction Set

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
MOV	r1, #byte	r1 ← byte	3	2						
	saddr, #byte	(saddr) ← byte	3	3						
	sfr**, #byte	sfr ← byte	3	3						
	r, r1	r ← r1	3	2						
	A, r1	A ← r1	3	1						
	A, saddr	A ← (saddr)	3	2						
	saddr, A	(saddr) ← A	3	2						
	saddr, saddr	(saddr) ← (saddr)	4	3						
	A, sfr	A ← sfr	3	2						
	sfr, A	sfr ← A	3	2						
	A, mem*	A ← (mem)	5	1						
	A, mem	A ← (mem)	5-6	2-4						
	mem, A*	(mem) ← A	5	1						
	mem, A	(mem) ← A	5-6	2-4						
	A, (saddrp)	A ← ((saddrp))	5	2						
	(saddrp), A	((saddrp)) ← A	4	2						
	A, addr16	A ← (addr16)	4	4						
	addr16, A	(addr16) ← A	3	4						
	PSWL, #byte	PSW_L ← byte	3	3	X	X	X	X	X	X
	PSWH, #byte	PSW_H ← byte	3	3						
	PSWL, A	PSW_L ← A	3	2	X	X	X	X	X	X
	PSWH, A	PSW_H ← A	3	2						
	A, PSWL	A ← PSW_L	3	2						
	A, PSWH	A ← PSW_H	3	2						
XCH	A, r1	A ⟷ r1	4	1						
	r, r1	r ⟷ r1	4	2						
	A, mem	A ⟷ (mem)	7-8	2-4						
	A, saddr	A ⟷ (saddr)	4	2						
	A, sfr	A ⟷ sfr	7	3						
	A, (saddrp)	A ⟷ ((saddrp))	6	2						
	saddr, saddr	(saddr) ⟷ (saddr)	8	3						

** A special instruction is used to write to STBC and WDM (see below).

* One-byte move instruction.

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
MOVW	rp1, #word	rp1 ← word	3	3						
	saddrp, #word	(saddrp) ← word	4	4						
	sfrp, #word	sfrp ← word	3	4						
	rp, rp1	rp ← rp1	3	2						
	AX, saddrp	AX ← (saddrp)	3	2						
	saddrp, AX	(saddrp) ← AX	3	2						
	saddrp, saddrp	(saddrp) ← (saddrp)	4	3						
	AX, sfrp	AX ← sfrp	3	2						
	sfrp, AX	sfrp ← AX	3	2						
XCHW	AX, saddrp	AX ⟷ (saddrp)	4	2						
	AX, sfrp	AX ⟷ sfrp	7	3						
	saddrp, saddrp	(saddrp) ⟷ (saddrp)	8	3						
	rp rp1	rp ⟷ rp1	5	2						
ADD	A, #byte	A, CY ← A + byte	3	2	X	X	X	V	0	X
	saddr, #byte	(saddr), CY ← (saddr) + byte	4	3	X	X	X	V	0	X
	sfr, #byte	sfr, CY ← sfr + byte	7	4	X	X	X	V	0	X
	r, r1	r, CY ← r + r1	3	2	X	X	X	V	0	X
	A, saddr	A, CY ← A + (saddr)	3	2	X	X	X	V	0	X
	A, sfr	A, CY ← A + sfr	6	3	X	X	X	V	0	X
	saddr, saddr	(saddr), CY ← (saddr) + (saddr)	6	3	X	X	X	V	0	X
	A, mem	A, CY ← A + (mem)	6-7	2-4	X	X	X	V	0	X
	mem, A	(mem), CY ← (mem) + A	7-8	2-4	X	X	X	V	0	X
ADDC	A, #byte	A, CY ← A + byte + CY	3	2	X	X	X	V	0	X
	saddr, #byte	(saddr), CY ← (saddr) + byte + CY	4	3	X	X	X	V	0	X
	sfr, #byte	sfr, CY ← sfr + byte + CY	7	4	X	X	X	V	0	X
	r, r1	r, CY ← r + r1 + CY	3	2	X	X	X	V	0	X
	A, saddr	A, CY ← A + (saddr) + CY	3	2	X	X	X	V	0	X
	A, sfr	A, CY ← A + sfr + CY	6	3	X	X	X	V	0	X
	saddr, saddr	(saddr), CY ← (saddr) + (saddr) + CY	6	3	X	X	X	V	0	X
	A, mem	A, CY ← A + (mem) + CY	6-7	2-4	X	X	X	V	0	X
	mem, A	(mem), CY ← (mem) + A + CY	7-8	2-4	X	X	X	V	0	X

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
SUB	A, #byte	A, CY ← A − byte	3	2	X	X	X	V	1	X
	saddr, #byte	(saddr), CY ← (saddr) − byte	4	3	X	X	X	V	1	X
	sfr, #byte	sfr, CY ← sfr − byte	7	4	X	X	X	V	1	X
	r, r1	r, CY ← r − r1	3	2	X	X	X	V	1	X
	A, saddr	A, CY ← A − (saddr)	3	2	X	X	X	V	1	X
	A, sfr	A, CY ← A − sfr	6	3	X	X	X	V	1	X
	saddr, saddr	(saddr), CY ← (saddr) − (saddr)	6	3	X	X	X	V	1	X
	A, mem	A, CY ← A − (mem)	6-7	2-4	X	X	X	V	1	X
	mem, A	(mem), CY ← (mem) − A	7-8	2-4	X	X	X	V	1	X
SUBC	A, #byte	A, CY ← A − byte − CY	3	2	X	X	X	V	1	X
	saddr, #byte	(saddr), CY ← (saddr) − byte − CY	4	3	X	X	X	V	1	X
	sfr, #byte	sfr, CY ← sfr − byte − CY	7	4	X	X	X	V	1	X
	r, r1	r, CY ← r − r1 − CY	3	2	X	X	X	V	1	X
	A, saddr	A, CY ← A − (saddr) − CY	3	2	X	X	X	V	1	X
	A, sfr	A, CY ← A − sfr − CY	6	3	X	X	X	V	1	X
	saddr, saddr	(saddr), CY ← (saddr) − (saddr) − CY	6	3	X	X	X	V	1	X
	A, mem	A, CY ← A − (mem) − CY	6-7	2-4	X	X	X	V	1	X
	mem, A	(mem), CY ← (mem) − A − CY	7-8	2-4	X	X	X	V	1	X
AND	A, #byte	A ← A ∧ byte	3	2	X	X	U	P	0	0
	saddr, #byte	(saddr) ← (saddr) ∧ byte	4	3	X	X	U	P	0	0
	sfr, #byte	sfr ← sfr ∧ byte	7	4	X	X	U	P	0	0
	r, r1	r ← r ∧ r1	3	2	X	X	U	P	0	0
	A, saddr	A ← A ∧ (saddr)	3	2	X	X	U	P	0	0
	A, sfr	A → A ∧ sfr	6	3	X	X	U	P	0	0
	saddr, saddr	(saddr) ← (saddr) ∧ (saddr)	6	3	X	X	U	P	0	0
	A, mem	A ← A ∧ (mem)	6-7	2-4	X	X	U	P	0	0
	mem, A	(mem) ← (mem) ∧ A	7-8	2-4	X	X	U	P	0	0
OR	A, #byte	A ← A V byte	3	2	X	X	U	P	0	0
	saddr, #byte	(saddr) ← (saddr) V byte	4	3	X	X	U	P	0	0
	sfr, #byte	sfr ← sfr V byte	7	4	X	X	U	P	0	0
	r, r1	r ← r V r1	3	2	X	X	U	P	0	0
	A, saddr	A ← A V (saddr)	3	2	X	X	U	P	0	0
	A, sfr	A ← A V sfr	6	3	X	X	U	P	0	0
	saddr, saddr	(saddr) ← (saddr) V (saddr)	6	3	X	X	U	P	0	0
	A, mem	A ← A V (mem)	6-7	2-4	X	X	U	P	0	0
	mem, A	(mem) ← (mem) V A	7-8	2-4	X	X	U	P	0	0

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
XOR	A, #byte	A ← A ∨ byte	3	2	X	X	U	P	0	0
	saddr, #byte	(saddr) ← (saddr) ∨ byte	4	3	X	X	U	P	0	0
	sfr, #byte	sfr ← sfr ∨ byte	7	4	X	X	U	P	0	0
	r, r1	r ← r ∨ r1	3	2	X	X	U	P	0	0
	A, saddr	A ← A ∨ (saddr)	3	2	X	X	U	P	0	0
	A, sfr	A ← A ∨ sfr	6	3	X	X	U	P	0	0
	saddr, saddr	(saddr) ← (saddr) ∨ (saddr)	6	3	X	X	U	P	0	0
	A, mem	A ← A ∨ (mem)	6-7	2-4	X	X	U	P	0	0
	mem, A	(mem) ← (mem) ∨ A	7-8	2-4	X	X	U	P	0	0
CMP	A, #byte	A − byte	3	2	X	X	X	V	1	X
	saddr, #byte	(saddr) − byte	4	3	X	X	X	V	1	X
	sfr, #byte	sfr − byte	7	4	X	X	X	V	1	X
	r, r1	r − r1	3	2	X	X	X	V	1	X
	A, saddr	A − (saddr)	3	2	X	X	X	V	1	X
	A, sfr	A − sfr	6	3	X	X	X	V	1	X
	saddr, saddr	(saddr) − (saddr)	6	3	X	X	X	V	1	X
	A, mem	A − (mem)	6-7	2-4	X	X	X	V	1	X
	mem, A	(mem) − A	6-7	2-4	X	X	X	V	1	X
ADDW	AX, #word	AX, CY ← AX + word	4	3	X	X	U	V	0	X
	saddrp, #word	(saddrp), CY ← (saddrp) + word	5	4	X	X	U	V	0	X
	sfrp, #word	sfrp, CY ← sfrp + word	8	5	X	X	U	V	0	X
	rp, rp1	rp, CY ← rp + rp1	4	2	X	X	U	V	0	X
	AX, saddrp	AX, CY ← AX + (saddrp)	4	2	X	X	U	V	0	X
	AX, sfrp	AX, CY ← AX + sfrp	7	3	X	X	U	V	0	X
	saddrp, saddrp	(saddrp), CY ← (saddrp) + (saddrp)	6	3	X	X	U	V	0	X
SUBW	AX, #word	AX, CY ← AX − word	4	3	X	X	U	V	1	X
	saddrp, #word	(saddrp), CY ← (saddrp) − word	5	4	X	X	U	V	1	X
	sfrp, #word	sfrp, CY ← sfrp − word	8	5	X	X	U	V	1	X
	rp, rp1	rp, CY ← rp − rp1	4	2	X	X	U	V	1	X
	AX, saddrp	AX, CY ← AX − (saddrp)	4	2	X	X	U	V	1	X
	AX, sfrp	AX, CY ← AX − sfrp	7	3	X	X	U	V	1	X
	saddrp, saddrp	(saddrp), CY ← (saddrp) − (saddrp)	6	3	X	X	U	V	1	X
CMPW	AX, #word	AX − word	4	3	X	X	U	V	1	X
	saddrp, #word	(saddrp) − word	5	4	X	X	U	V	1	X
	sfrp, #word	sfrp − word	8	5	X	X	U	V	1	X
	rp, rp1	rp − rp1	4	2	X	X	U	V	1	X
	AX, saddrp	AX − (saddrp)	4	2	X	X	U	V	1	X
	AX, sfrp	AX − sfrp	7	3	X	X	U	V	1	X
	saddrp, saddrp	(saddrp) − (saddrp)	6	3	X	X	U	V	1	X

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
MULU	r1	AX ← A x r1	18	2						
DIVU	r1	AX (Quotient), r1 (Remainder) ← AX ÷ r1	18	2						
MULUW	rp1	AX (High Order 16 Bits), rp1 (Low Order 16 Bits), ← AX x rp1	27	2						
DIVUX	rp1	AXDE (Quotient), rp1 (Remainder) ← AXDE ÷ rp1	50	2						
INC	r1	r1 ← r1 + 1	3	1	X	X	X	V	0	
	saddr	(saddr) ← (saddr) + 1	4	2	X	X	X	V	0	
DEC	r1	r1 ← r1 − 1	3	1	X	X	X	V	1	
	saddr	(saddr) ← (saddr) − 1	4	2	X	X	X	V	1	
INCW	rp2	rp2 ← rp2 + 1	3	1						
	saddrp	(saddrp) ← (saddrp) + 1	6	3						
DECW	rp2	rp2 ← rp2 − 1	3	1						
	saddrp	(saddrp) ← (saddrp) − 1	6	3						
ROR	r1, n	(CY, $r1_7$ ← $r1_0$; $r1_{m-1}$ ← $r1_m$) x n	4 + 3n	2	X	X	0	P	0	X
ROL	r1, n	(CY, $r1_0$ ← $r1_7$; $r1_{m+1}$ ← $r1_m$) x n	4 + 3n	2	X	X	0	P	0	X
RORC	r1, n	(CY ← $r1_0$; $r1_7$ ← CY; $r1_{m-1}$ ← $r1_m$) x n	4 + 3n	2	X	X	0	P	0	X
ROLC	r1, n	(CY ← $r1_7$; $r1_0$ ← CY; $r1_{m+1}$ ← $r1_m$) x n	4 + 3n	2	X	X	0	P	0	X
SHR	r1, n	(CY ← $r1_0$; $r1_7$ ← 0; $r1_{m-1}$ ← $r1_m$) x n	4 + 3n	2	X	X	0	P	0	X
SHL	r1, n	(CY ← $r1_7$; $r1_0$ ← 0; $r1_{m+1}$ ← $r1_m$) x n	4 + 3n	2	X	X	0	P	0	X
SHRW	rp1, n	(CY ← rp_0; rp_{15} ← 0; rp_{m-1} ← rp_m) x n	4 + 3n	2	X	X	0	P	0	X
SHLW	rp1, n	(CY ← rp_{15}; rp_0 ← 0; rp_{m+1} ← rp_m) x n	4 + 3n	2	X	X	0	P	0	X
ROR4	(rp1)	A_{3-0} ← $(rp1)_{3-0}$; $(rp1)_{7-4}$ ← A_{3-0}; $(rp1)_{3-0}$ ← $(rp1)_{7-4}$	8	2	X	X	0	P	0	
ROL4	(rp1)	A_{3-0} ← $(rp1)_{7-4}$; $(rp1)_{3-0}$ ← A_{3-0}; $(rp1)_{7-4}$ ← $(rp1)_{3-0}$	8	2	X	X	0	P	0	
ADJ4		Decimal Adjust Accumulator	3	1	X	X	X	V	0	X

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
MOV1	CY, saddr.bit	CY ← (saddr.bit)	6	3						X
	CY, sfr.bit	CY ← sfr.bit	6	3						X
	CY, A.bit	CY ← A.bit	6	2						X
	CY, X.bit	CY ← X.bit	6	2						X
	CY, PSWH, bit	CY ← PSW_H.bit	6	2						X
	CY, PSWL, bit	CY ← PSW_L.bit	6	2						X
	saddr.bit, CY	(saddr.bit) ← CY	7	3						
	sfr.bit, CY	sfr.bit ← CY	7	3						
	A.bit, CY	A.bit ← CY	8	2						
	X.bit, CY	X.bit ← CY	8	2						
	PSWH.bit, CY	PSW_H.bit ← CY	8	2						
	PSWL.bit, CY	PSW_L.bit ← CY	8	2						
AND1	CY, saddr.bit	CY ← CY ∧ (saddr.bit)	6	3						X
	CY,/saddr.bit	CY ← CY ∧ $\overline{(saddr.bit)}$	6	3						X
	CY, sfr.bit	CY ← CY ∧ sfr.bit	6	3						X
	CY,/sfr.bit	CY ← CY ∧ $\overline{sfr.bit}$	6	3						X
	CY, A.bit	CY ← CY ∧ A.bit	6	2						X
	CY,/A.bit	CY ← CY ∧ $\overline{A.bit}$	6	2						X
	CY, X.bit	CY ← CY ∧ X.bit	6	2						X
	CY,/X.bit	CY ← CY ∧ $\overline{X.bit}$	6	2						X
	CY, PSWH.bit	CY ← CY ∧ PSW_H.bit	6	2						X
	CY,/PSWH.bit	CY ← CY ∧ $\overline{PSW_H.bit}$	6	2						X
	CY, PSWL.bit	CY ← CY ∧ PSW_L.bit	6	2						X
	CY,/PSWL.bit	CY ← CY ∧ $\overline{PSW_L.bit}$	6	2						X
OR1	CY, saddr.bit	CY ← CY V (saddr.bit)	6	3						X
	CY,/saddr.bit	CY ← CY V $\overline{(saddr.bit)}$	6	3						X
	CY, sfr.bit	CY ← CY V sfr.bit	6	3						X
	CY,/sfr.bit	CY ← CY V $\overline{sfr.bit}$	6	3						X
	CY, A.bit	CY ← CY V A.bit	6	2						X
	CY,/A.bit	CY ← CY V $\overline{A.bit}$	6	2						X
	CY, X.bit	CY ← CY V X.bit	6	2						X
	CY,/X.bit	CY ← CY V $\overline{X.bit}$	6	2						X
	CY, PSWH.bit	CY ← CY V PSW_H.bit	6	2						X
	CY,/PSWH.bit	CY ← CY V $\overline{PSW_H.bit}$	6	2						X
	CY, PSWL.bit	CY ← CY V PSW_L.bit	6	2						X
	CY,/PSWL.bit	CY ← CY V $\overline{PSW_L.bit}$	6	2						X

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
XOR1	CY, saddr.bit	CY ← CY ∀ (saddr.bit)	6	3						X
	CY, sfr.bit	CY ← CY ∀ sfr.bit	6	3						X
	CY, A.bit	CY ← CY ∀ A.bit	6	2						X
	CY, X.bit	CY ← CY ∀ X.bit	6	2						X
	CY, PSWH.bit	CY ← CY ∀ PSW_H.bit	6	2						X
	CY, PSWL.bit	CY ← CY ∀ PSW_L.bit	6	2						X
SET1	saddr.bit	(saddr.bit) ← 1	5	2						
	sfr.bit	sfr.bit ← 1	6	3						
	A.bit	A.bit ← 1	7	2						
	X.bit	X.bit ← 1	7	2						
	PSWH.bit	PSW_H.bit ← 1	7	2						
	PSWL.bit	PSW_L.bit ← 1	7	2						
CLR1	saddr.bit	(saddr.bit) ← 0	5	2						
	sfr.bit	sfr.bit ← 0	6	3						
	A.bit	A.bit ← 0	7	2						
	X.bit	X.bit ← 0	7	2						
	PSWH.bit	PSW_H.bit ← 0	7	2						
	PSWL.bit	PSW_L.bit ← 0	7	2						
NOT1	saddr.bit	(saddr.bit) ← $\overline{\text{(saddr.bit)}}$	6	3						
	sfr.bit	sfr.bit ← $\overline{\text{sfr.bit}}$	6	3						
	A.bit	A.bit ← $\overline{\text{A.bit}}$	7	2						
	X.bit	X.bit ← $\overline{\text{X.bit}}$	7	2						
	PSWH.bit	PSW_H.bit ← $\overline{PSW_H.bit}$	7	2						
	PSWL.bit	PSW_L.bit ← $\overline{PSW_L.bit}$	7	2						
SET1	CY	CY ← 1	3	1						1
CLR1	CY	CY ← 0	3	1						0
NOT1	CY	CY ← $\overline{CY}$	3	1						X
CALL	!addr16	$(SP-1) \leftarrow (PC+3)_H$; $(SP-2) \leftarrow (PC+3)_L$; PC ← addr16; SP ← SP − 2	8	3						
CALLF	!addr11	$(SP-1) \leftarrow (PC+2)_H$; $(SP-2) \leftarrow (PC+2)_L$; PC ← addr11; SP ← SP − 2	8	2						
CALLT	(addr5)	$(SP-1) \leftarrow (PC+1)_H$; $(SP-2) \leftarrow (PC+1)_L$; $PC_H \leftarrow$ (TPFX8000H + addr5 + 1); $PC_H \leftarrow$ (TPFX8000H + addr5); SP ← SP − 2	10	1						

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
CALL	rp1	$(SP-1) \leftarrow (PC+2)_H$; $(SP-2) \leftarrow (PC+2)_L$; $PC_H \leftarrow rp1_H$; $PC_L \leftarrow rp1_L$; $SP \leftarrow SP-2$	13	2						
	(rp1)	$(SP-1) \leftarrow (PC+2)_H$; $(SP-2) \leftarrow (PC+2)_L$; $PC_H \leftarrow (rp1)_H$; $PC_L \leftarrow (rp1)_L$; $SP \leftarrow SP-2$	11	2						
BRK		$(SP-1) \leftarrow PSW_H$; $(SP-2) \leftarrow PSW_L$; $(SP-3) \leftarrow (PC+1)_H$; $(SP-4) \leftarrow (PC+1)_L$; $PC_L \leftarrow (003EH)$; $PC_H \leftarrow (003FH)$; $SP \leftarrow SP-4$	16	1						
RET		$PC_L \leftarrow (SP)$; $PC_H \leftarrow (SP+1)$; $SP \leftarrow SP+2$	8	1						
RETI		$PC_L \leftarrow (SP)$; $PC_H \leftarrow (SP+1)$; $PSW_L \leftarrow (SP+2)$; $PSW_H \leftarrow (SP+3)$; $SP \leftarrow SP+4$; $EOS \leftarrow 0$	14	1	R	R	R	R	R	R
PUSH	post	$((SP-1) \leftarrow post_H$; $(SP-2) \leftarrow post_L$; $SP \leftarrow SP-2) \times n$.	$7+8n$	2						
	PSW	$(SP-1) \leftarrow PSW_H$; $(SP-2) \leftarrow PSW_L$; $SP \leftarrow SP-2$	5	1						
PUSHU	post	$((UP-1) \leftarrow post_H$; $(UP-2) \leftarrow post_L$; $UP \leftarrow UP-2) \times n$.	$8+8n$	2						
POP	post	$(post_L \leftarrow (SP)$; $(post_H \leftarrow (SP+1)$; $SP \leftarrow SP+2) \times n$.	$7+8n$	2						
	PSW	$PSW_L \leftarrow (SP)$; $PSW_H \leftarrow (SP+1)$; $SP \leftarrow SP+2$	5	1	R	R	R	R	R	R
POPU	post	$(post_L \leftarrow (UP)$; $post_H \leftarrow (UP+1)$; $UP \leftarrow UP+2) \times n$.	$8+8n$	2						
MOVW	SP, #word	$SP \leftarrow word$	3	4						
	SP, AX	$SP \leftarrow AX$	3	2						
	AX, SP	$AX \leftarrow SP$	3	2						
INCW	SP	$SP \leftarrow SP+1$	6	2						
DECW	SP	$SP \leftarrow SP-1$	6	2						

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
BR	!addr16	PC ← addr16	4	3						
	rp1	$PC_H \leftarrow rp1_H$; $PC_L \leftarrow rp1_L$;	6	2						
	(rp1)	$PC_H \leftarrow (rp1)_H$; $PC_L \leftarrow (rp1)_L$;	9	2						
	$addr16	PC ← addr16	7	2						
BC BL	$addr16	PC ← addr16 if CY = 1	7(3)	2						
BNC BNL	$addr16	PC ← addr16 if CY = 0	7(3)	2						
BZ BE	$addr16	PC ← addr16 if Z = 1	7(3)	2						
BNZ BNE	$addr16	PC ← addr16 if Z = 0	7(3)	2						
BV BPE	$addr16	PC ← addr16 if P/V = 1	7(3)	2						
BNV BPO	$addr16	PC ← addr16 if P/V = 0	7(3)	2						
BN	$addr16	PC ← addr16 if S = 1	7(3)	2						
BP	$addr16	PC ← addr16 if S = 0	7(3)	2						
BGT	$addr16	PC ← addr16 if (P/V ⊻ S) V Z = 0	9(5)	3						
BGE	$addr16	PC ← addr16 if P/V ⊻ S = 0	9(5)	3						
BLT	$addr16	PC ← addr16 if P/V ⊻ S = 1	9(5)	3						
BLE	$addr16	PC ← addr16 if (P/V ⊻ S) V Z = 1	9(5)	3						
BH	$addr16	PC ← addr16 if Z + CY = 0	9(5)	3						
BNH	$addr16	PC ← addr16 if Z + CY = 1	9(5)	3						
BT	saddr.bit, $addr16	PC ← addr16 if (saddr.bit) = 1	9(7)	3						
	sfr.bit, $addr16	PC ← addr16 if (sfr.bit) = 1	10(7)	4						
	A.bit, $addr16	PC ← addr16 if A.bit = 1	10(7)	3						
	X.bit, $addr16	PC ← addr16 if X.bit = 1	10(7)	3						
	PSWH.bit, $addr16	PC ← addr16 if PSW_H.bit = 1	10(7)	3						
	PSWL.bit, $addr16	PC ← addr16 if PSW_L.bit = 1	10(7)	3						
BF	saddr.bit, $addr16	PC ← addr16 if (saddr.bit) = 0	10(7)	4						
	sfr.bit, $addr16	PC ← addr16 if (sfr.bit) = 0	10(7)	4						
	A.bit, $addr16	PC ← addr16 if A.bit = 0	10(7)	3						
	X.bit, $addr16	PC ← addr16 if X.bit = 0	10(7)	3						
	PSWH.bit, $addr16	PC ← addr16 if PSW_H.bit = 0	10(7)	3						
	PSWL.bit, $addr16	PC ← addr16 if PSW_L.bit = 0	10(7)	3						
BTCLR	saddr.bit, $addr16	PC ← addr16 if (saddr.bit) = 1 then reset (saddr.bit)	12(7)	4						
	sfr.bit, $addr16	PC ← addr16 if (sfr.bit) = 1 then reset (sfr.bit)	12(7)	4						
	A.bit, $addr16	PC ← addr16 if A.bit = 1 then reset A.bit	11(7)	3						

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
BTCLR (cont)	X.bit, $addr16	PC ← addr16 if X.bit = 1 then reset X.bit	11(7)	3						
	PSWH.bit, $addr16	PC ← addr16 if PSW_H.bit = 1 then reset PSW_H.bit	12(7)	3						
	PSWL.bit, $addr16	PC ← addr16 if PSW_L.bit = 1 then reset PSW_L.bit	12(7)	3						
BFSET	saddr.bit, $addr16	PC ← addr16 if (saddr.bit) = 0 then set (saddr.bit)	12(7)	4						
	sfr.bit, $addr16	PC ← addr16 if (sfr.bit) = 0 then set (sfr.bit)	12(7)	4						
	A.bit, $addr16	PC ← addr16 if A.bit = 0 then set A.bit	11(7)	4						
	X.bit, $addr16	PC ← addr16 if X.bit = 0 then set X.bit	11(7)	3						
	PSWH.bit, $addr16	PC ← addr16 if PSW_H.bit = 0 then set PSW_H.bit	12(7)	3						
	PSWL.bit, $addr16	PC ← addr16 if PSW_L.bit = 0 then set PSW_L.bit	12(7)	3						
DBNZ	r2, $addr16	r2 ← r2 − 1; then PC ← addr16 if r2 ≠ 0	8(5)	2						
	saddr, $addr 16	(saddr) ← (saddr) − 1; then PC ← addr16 if saddr ≠ 0	7(6)	3						
BRKCS	RBn	PC_H ⟷ R5; PC_L ⟷ R4; R7 ⟷ PSW_H; R6 ⟷ PSW_L; RBS2-0 ← n; RSS ← 0; IE ← 0	13	2						
RETCS	!addr16	PC_H ← R5; PC_L ← R4; R4, R5 ← (addr16); PSW_H ← R7; PSW_L ← R6; EOS ← 0	6	3						
MOVM	(DE+), A	(DE+) ← A; C ← C − 1, End if C = 0	2 + 7n	2						
	(DE−), A	(DE−) ← A; C ← C − 1, End if C = 0	2 + 7n	2						
MOVBK	(DE+), (HL+)	(DE+) ← (HL+); C ← C − 1, End if C = 0	2 + 10n	2						
	(DE−), (HL−)	(DE−) ← (HL−); C ← C − 1, End if C = 0	2 + 10n	2						
XCHM	(DE+), A	(DE+) ⟷ A; C ← C − 1, End if C = 0	2 + 12n	2						
	(DE−), A	(DE−) ⟷ A; C ← C − 1, End if C = 0	2 + 12n	2						

Instruction Set (cont)

Mnemonic	Operand	Operation	States	Bytes	Flags S	Z	AC	P/V	SUB	CY
XCHBK	(DE+), (HL+)	(DE+) ⟷ (HL+); C ← C − 1, End if C = 0	2 + 15n	2						
	(DE−), (HL−)	(DE−) ⟷ (HL−); C ← C − 1, End if C = 0	2 + 15n	2						
CMPME	(DE+), A	(DE+) − A; C ← C − 1, End if C = 0 or Z = 0	2 + 8n	2	X	X	X	V	1	X
	(DE−), A	(DE−) − A; C ← C − 1, End if C = 0 or Z = 0	2 + 8n	2	X	X	X	V	1	X
CMPBKE	(DE+), (HL+)	(DE+) − (HL+); C ← C − 1, End if C = 0 or Z = 0	2 + 11n	2	X	X	X	V	1	X
	(DE−), (HL−)	(DE−) − (HL−); C ← C − 1, End if C = 0 or Z = 0	2 + 11n	2	X	X	X	V	1	X
CMPMNE	(DE+), A	(DE+) − A; C ← C − 1, End if C = 0 or Z = 1	2 + 8n	2	X	X	X	V	1	X
	(DE−), A	(DE−) − A; C ← C − 1, End if C = 0 or Z = 1	2 + 8n	2	X	X	X	V	1	X
CMPBKNE	(DE+), (HL+)	(DE+) − (HL+); C ← C − 1, End if C = 0 or Z = 1	2 + 11n	2	X	X	X	V	1	X
	(DE−), (HL−)	(DE−) − (HL−); C ← C − 1, End if C = 0 or Z = 1	2 + 11n	2	X	X	X	V	1	X
CMPMC	(DE+), A	(DE+) − A; C ← C − 1, End if C = 0 or CY = 0	2 + 8n	2	X	X	X	V	1	X
	(DE−), A	(DE−) − A; C ← C − 1, End if C = 0 or CY = 0	2 + 8n	2	X	X	X	V	1	X
CMPBKC	(DE+), (HL+)	(DE+) − (HL+); C ← C − 1, End if C = 0 or CY = 0	2 + 11n	2	X	X	X	V	1	X
	(DE−), (HL−)	(DE−) − (HL−); C ← C − 1, End if C = 0 or CY = 0	2 + 11n	2	X	X	X	V	1	X
CMPMNC	(DE+), A	(DE+) − A; C ← C − 1, End if C = 0 or CY = 1	2 + 8n	2	X	X	X	V	1	X
	(DE−), A	(DE−) − A; C ← C − 1, End if C = 0 or CY = 1	2 + 8n	2	X	X	X	V	1	X
CMPBKNC	(DE+), (HL+)	(DE+) − (HL+); C ← C − 1, End if C = 0 or CY = 1	2 + 11n	2	X	X	X	V	1	X
	(DE−), (HL−)	(DE−) − (HL−); C ← C − 1, End if C = 0 or CY = 1	2 + 11n	2	X	X	X	V	1	X
MOV	STBC, #byte	STBC ← byte	5	4						
	WDM, #byte	WDM ← byte	5	4						
SWRS		RSS ← $\overline{\text{RSS}}$	3	1						
SEL	RBn	RSS ← 0; RBS2-0 ← n	3	2						
	RBn, ALT	RSS ← 1; RBS2-0 ← n	3	2						
NOP		No Operation	3	1						
EI		IE ← 1 (Enable Interrupt)	3	1						
DI		IE ← 0 (Disable Interrupt	3	1						

NEC
NEC Electronics Inc.

μPD8035HL/48H
HIGH-SPEED, 8-BIT, SINGLE-CHIP HMOS MICROCOMPUTERS

Description

The μPD8035HL and the μPD8048H make up the μPD8048H family of single-chip 8-bit microcomputers. The processors in this family differ only in their internal program memory options: the μPD8048H with 1K×8 bytes of mask ROM and the μPD8035HL with external memory.

The NEC μPD8035HL and μPD8048H are single component, 8-bit, parallel microprocessors using n-channel silicon gate MOS technology. The μPD8048H family of components functions efficiently in control as well as in arithmetic applications. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8035HL/48H instruction set comprises 1 and 2 byte instructions with over 70% of them single-byte. Execution requires only 1 or 2 cycles per instruction and over 50% are single-cycle instructions.

The functions of the μPD8048H series of microprocessors can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8048H contains the following functions usually found in external peripheral devices: 1024×8 bits of ROM program memory; 64×8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The μPD8035HL is intended for applications using external program memory only. It contains all the features of the μPD8048H except the 1024×8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

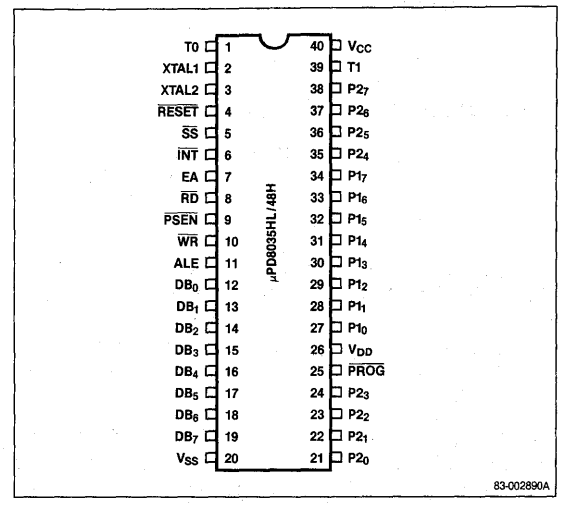
Features

- ☐ Fully compatible with industry standard 8048/8748/8035
- ☐ 2.5 μs cycle time: all instructions 1 or 2 bytes
- ☐ Interval timer/event counter
- ☐ 64×8-byte RAM data memory
- ☐ External and timer interrupts
- ☐ 96 instructions: 70% single byte
- ☐ 27 I/O lines
- ☐ Internal clock generator
- ☐ 8 level stack
- ☐ Compatible with 8080A/8085A peripherals
- ☐ HMOS silicon gate technology
- ☐ Single +5 V power supply

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8035HLC	40-pin plastic DIP	6 MHz
μPD8048HC	40-pin plastic DIP	6 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	T0	Test 0 input/output
2	XTAL1	Crystal 1 input
3	XTAL2	Crystal 2 input
4	$\overline{RESET}$	Reset input
5	$\overline{SS}$	Single step input
6	$\overline{INT}$	Interrupt input
7	EA	External access input
8	$\overline{RD}$	Read output
9	$\overline{PSEN}$	Program store enable output
10	$\overline{WR}$	Write output
11	ALE	Address latch enable output
12-19	DB_0-DB_7	Bidirectional data bus
20	V_{SS}	Ground
21-24, 35-38	$P2_0$-$P2_7$	Quasi-bidirectional Port 2
25	$\overline{PROG}$	Program output

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Pin Identification (cont)

No.	Symbol	Function
26	V_{DD}	RAM power supply
27-34	$P1_0$-$P1_7$	Quasi-bidirectional Port 1
39	T1	Test 1 input
40	V_{CC}	Primary power supply

Pin Functions

XTAL 1 (Crystal 1)

XTAL1 is one side of the crystal, LC, or external frequency source (non-TTL-compatible V_{IH}).

XTAL 2 (Crystal 2)

XTAL2 is the other side of the crystal or frequency source.

T0 (Test 0)

T0 is the testable input using conditional transfer functions JT0 and JNT0. The internal state clock (CLK) is available to T0 using the ENT0 CLK instruction. T0 can also be used during programming as a testable flag.

T1 (Test 1)

T1 is the testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.

$\overline{\text{RESET}}$ (Reset)

An active low on $\overline{\text{RESET}}$ initializes the processor. $\overline{\text{RESET}}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).

$\overline{\text{SS}}$ (Single Step)

An active low on $\overline{\text{SS}}$, together with ALE, causes the processor to execute the program one step at a time.

$\overline{\text{INT}}$ (Interrupt)

An active low on $\overline{\text{INT}}$ starts an interrupt if interrupts are enabled. A reset disables an interrupt. $\overline{\text{INT}}$ can be tested with the JNI instruction and, depending on the results, a jump to the specified address can occur.

EA (External Access)

An active high on EA disables internal program memory and fetches and accesses external program memory. EA is used for system testing and debugging.

$\overline{\text{RD}}$ (Read)

$\overline{\text{RD}}$ will pulse low when the processor performs a bus read. An active low on $\overline{\text{RD}}$ enables data onto the processor bus from a peripheral device and functions as a read strobe for external data memory.

$\overline{\text{WR}}$ (Write)

$\overline{\text{WR}}$ will pulse low when the processor performs a bus write. $\overline{\text{WR}}$ can also function as a write strobe for external data memory.

$\overline{\text{PSEN}}$ (Program Store Enable)

$\overline{\text{PSEN}}$ becomes active only during an external memory fetch. (Active low).

ALE (Address Latch Enable)

ALE occurs at each cycle. ALE can also be used as a clock output. The falling edge of ALE addresses external data memory or external program memory.

DB_0-DB_7 (Data Bus)

DB_0-DB_7 is a bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes. The contents of the DB_0-DB_7 bus can be latched in a static mode.

During an external memory fetch, DB_0-DB_7 output the low-order eight bits of the memory address. $\overline{\text{PSEN}}$ fetches the instruction. DB_0-DB_7 also output the address of an external data memory fetch. The addressed data is controlled by ALE, $\overline{\text{RD}}$, and $\overline{\text{WR}}$.

$P1_0$-$P1_7$ (Port 1)

$P1_0$-$P1_7$ is an 8-bit quasi-bidirectional port.

$P2_0$-$P2_7$ (Port 2)

$P2_0$-$P2_7$ is an 8-bit quasi-bidirectional port. $P2_0$-$P2_3$ output the high-order four bits of the address during an external program memory fetch. $P2_0$-$P2_3$ also function as a 4-bit I/O bus for the μPD82C43 I/O port expander.

$\overline{\text{PROG}}$ (Program Pulse)

$\overline{\text{PROG}}$ is used as an output pulse during a fetch when interfacing with the μPD82C43 I/O port expander.

V_{CC} (Primary Power Supply)

V_{CC} is the primary power supply. V_{CC} is +5V during normal operation.

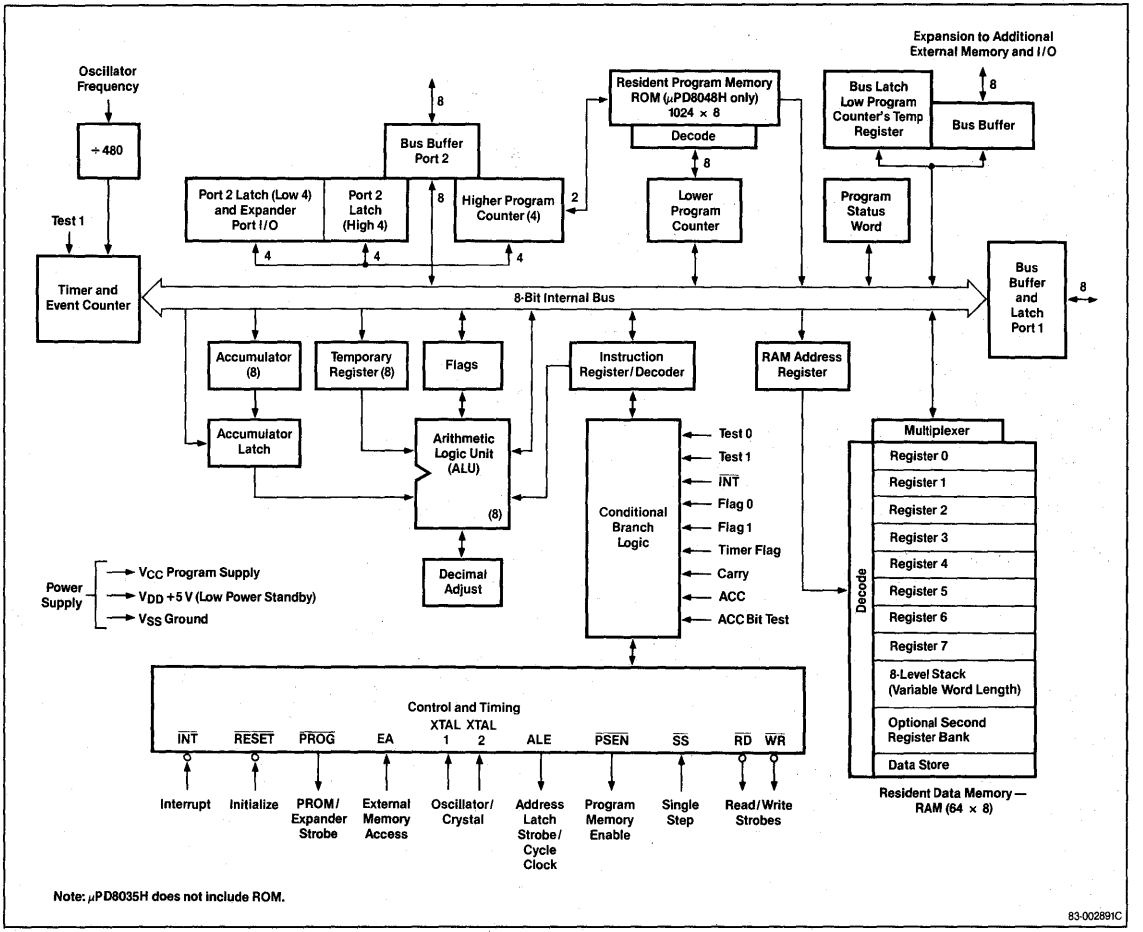
V_{DD} (RAM Power Supply)

V_{DD} must be set to +5 V for normal operation. V_{DD} supplies power to the internal RAM during standby mode.

V_{SS} (Ground)

V_{SS} is ground potential.

Block Diagram



Note: μPD8035H does not include ROM.

83-002891C

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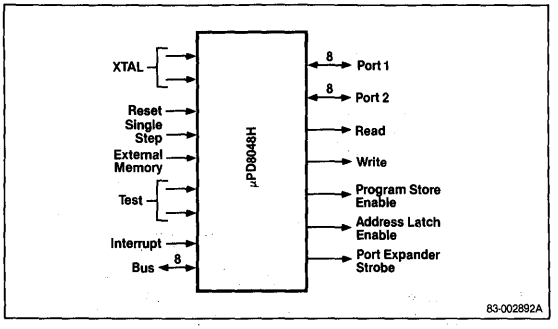
Logic Symbol



Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin, $V_{I/O}$	−0.5 V to +7 V (Note 1)
Power dissipation, P_D	1.5 W

Note:
(1) With respect to ground.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0°C$ to +70°C, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage (All except XTAL1, XTAL2)	V_{IL}	−0.5		0.8	V	
Input low voltage ($\overline{RESET}$, X1, X2)	V_{IL1}	−0.5		0.8	V	
Input high voltage (All except XTAL1, XTAL2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input high voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IH1}	3.8		V_{CC}	V	
Output low voltage (bus)	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output low voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL1}			0.45	V	$I_{OL} = 2.0$ mA
Output low voltage ($\overline{PROG}$)	V_{OL2}			0.45	V	$I_{OL} = 2.0$ mA

DC Characteristics (cont)

$T_A = 0°C$ to +70°C, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output low voltage (all other outputs)	V_{OL3}			0.45	V	$I_{OL} = 2.0$ mA
Output high voltage (bus)	V_{OH}	2.4			V	$I_{OH} = -400\,\mu A$
Output high voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, $\overline{ALE}$)	V_{OH1}	2.4			V	$I_{OH} = -400\,\mu A$
Output high voltage (all other outputs)	V_{OH2}	2.4			V	$I_{OH} = -40\,\mu A$
Input leakage current (T1, $\overline{INT}$)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, $\overline{SS}$)	I_{IL1}			−500	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45$ V
Output leakage current (bus, T0, high impedance state)	I_{OL}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45$ V
Power down supply current	I_{DD}		4	8	mA	$T_A = 25°C$
Total supply current	$I_{DD} + I_{CC}$		50	80	mA	$T_A = 25°C$
RAM standby voltage	V_{DD}	2.2		5.5	V	Standby mode. Reset ≤ 0.6 V

AC Characteristics

$T_A = 0°C$ to +70°C, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
ALE pulse width	t_{LL}	410			ns	(Note 1)
Address setup to ALE	t_{AL}	220			ns	(Note 1)
Address hold from ALE	t_{LA}	120			ns	(Note 1)
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	1050			ns	(Note 1)
Control pulse width ($\overline{PSEN}$)	t_{CC2}	800			ns	(Note 1)
Data setup $\overline{WR}$	t_{DW}	880			ns	(Note 1)
Data hold after $\overline{WR}$	t_{WD}	110			ns	(Note 2)
Data hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	0		220	ns	(Note 1)
$\overline{RD}$ to data in	t_{RD1}			800	ns	(Note 1)
$\overline{PSEN}$ to data in	t_{RD2}			550	ns	(Note 1)

AC Characteristics (cont)

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address setup to $\overline{WR}$	t_{AW}	680			ns	(Note 1)
Address setup to data ($\overline{RD}$)	t_{AD1}			1570	ns	(Note 1)
Address setup to data ($\overline{PSEN}$)	t_{AD2}			1090	ns	(Note 1)
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	290			ns	(Note 1)
Address float to $\overline{PSEN}$	t_{AFC2}	40			ns	(Note 1)
ALE to control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	420			ns	(Note 1)
ALE to control ($\overline{PSEN}$)	t_{LAFC2}	170			ns	(Note 1)
Control to ALE ($\overline{RD}$, $\overline{WR}$, $\overline{PROG}$)	t_{CA1}	120			ns	(Note 1)
Control to ALE ($\overline{PSEN}$)	t_{CA2}	620			ns	(Note 1)
Port control setup to $\overline{PROG}$	t_{CP}	210			ns	(Note 1)
Port control hold to $\overline{PROG}$	t_{PC}	460			ns	(Note 1)
$\overline{PROG}$ to P2 input valid	t_{PR}			1300	ns	(Note 1)
Input data hold from $\overline{PROG}$	t_{PF}			250	ns	(Note 1)
Output data setup	t_{DP}	850			ns	(Note 1)
Output data hold	t_{PD}	200			ns	(Note 1)
$\overline{PROG}$ pulse width	t_{PP}	1500			ns	(Note 1)
Port 2 I/O data setup to ALE	t_{PL}	460			ns	(Note 1)
Port 2 I/O data hold to ALE	t_{LP}	150			ns	(Note 1)
Port output from ALE	t_{PV}			850	ns	(Note 1)
Cycle time	t_{CY}	2.5		15	μs	(Note 1)
T0 rep rate	t_{0PRR}	500			ns	(Note 1)

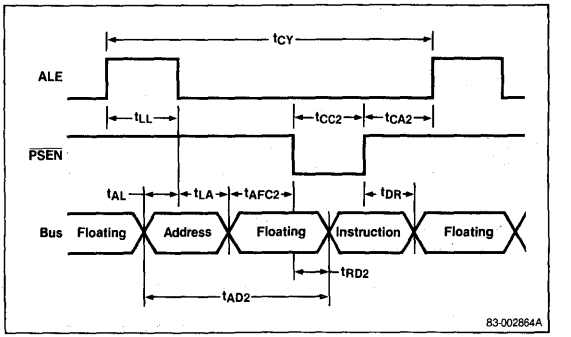
Note:

(1) Control outputs: $C_L = 80$ pF, bus outputs: $C_L = 150$ pF

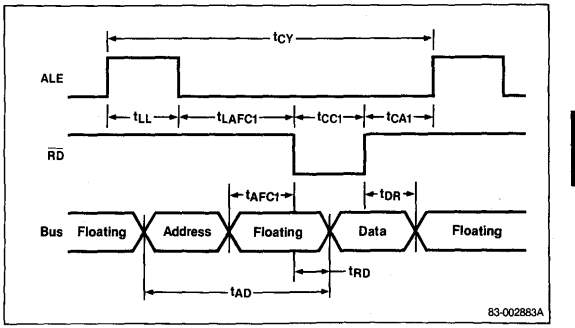
(2) Bus high impedance, load = 20 pF

Timing Waveforms

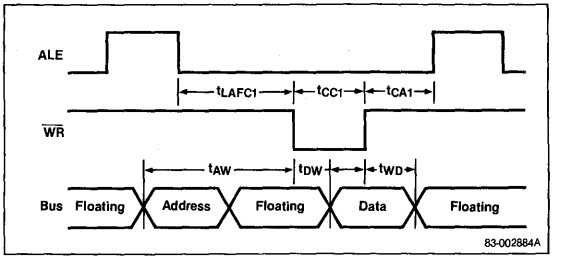
Instruction Fetch from External Memory



Read from External Data Memory



Write to External Memory



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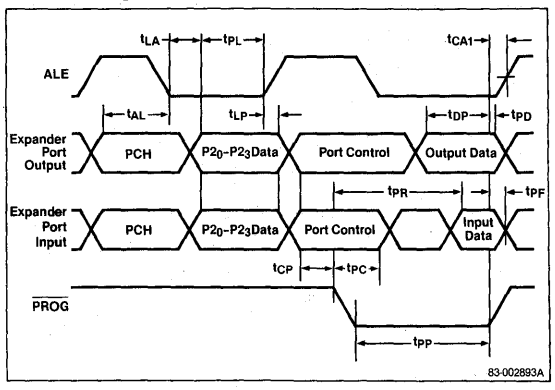
Timing Waveforms (cont)

Port 2 Timing



Bus Timing Requirements

Symbol	Timing Formula	Min/Max	Unit
t_{LL}	$(7/30)\,t_{CY}-170$	Min	ns
t_{AL}	$(2/15)\,t_{CY}-110$	Min	ns
t_{LA}	$(1/15)\,t_{CY}-40$	Min	ns
t_{CC1}	$(1/2)\,t_{CY}-200$	Min	ns
t_{CC2}	$(2/5)\,t_{CY}-200$	Min	ns
t_{DW}	$(13/30)\,t_{CY}-200$	Min	ns
t_{WD}	$(1/15)\,t_{CY}-50$	Min	ns
t_{DR}	$(1/10)\,t_{CY}-30$	Max	ns
t_{RD1}	$(2/5)\,t_{CY}-200$	Max	ns
t_{RD2}	$(3/10)\,t_{CY}-200$	Max	ns
t_{AW}	$(1/3)\,t_{CY}-150$	Min	ns
t_{AD1}	$(11/15)\,t_{CY}-250$	Max	ns
t_{AD2}	$(8/15)\,t_{CY}-250$	Max	ns
t_{AFC1}	$(2/15)\,t_{CY}-40$	Min	ns
t_{AFC2}	$(1/30)\,t_{CY}-40$	Min	ns
t_{LAFC1}	$(1/5)\,t_{CY}-75$	Min	ns
t_{LAFC2}	$(1/10)\,t_{CY}-75$	Min	ns
t_{CA1}	$(1/15)\,t_{CY}-40$	Min	ns
t_{CA2}	$(4/15)\,t_{CY}-40$	Min	ns
t_{CP}	$(1/10)\,t_{CY}-40$	Min	ns
t_{PC}	$(4/15)\,t_{CY}-200$	Min	ns
t_{PR}	$(17/30)\,t_{CY}-120$	Max	ns
t_{PF}	$(1/10)\,t_{CY}$	Max	ns
t_{DP}	$(2/5)\,t_{CY}-150$	Min	ns
t_{PD}	$(1/10)\,t_{CY}-50$	Min	ns
t_{PP}	$(7/10)\,t_{CY}-250$	Min	ns
t_{PL}	$(4/15)\,t_{CY}-200$	Min	ns
t_{LP}	$(1/10)\,t_{CY}-100$	Min	ns
t_{PV}	$(3/10)\,t_{CY}-100$	Max	ns
t_{OPRR}	$(3/15)\,t_{CY}$	Min	ns
t_{CY}	6 MHz		μs

Instruction Set

Mnemonic	Function	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator																
ADD A, # data	(A) ← (A) + data	Add immediate the specified data to the accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) r = 0–7	Add contents of designated register to the accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) r = 0–1	Add indirect the contents of the data memory location to the accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0–7	Add with carry the contents of the designated register to the accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0–1	Add indirect with carry the contents of data memory location to the accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # data	(A) ← (A) AND data	Logical AND specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) r = 0–7	Logical AND contents of designated register with accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) r = 0–1	Logical AND indirect the contents of data memory with accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	Clear the contents of the accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		Decimal adjust the contents of the accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) – 1	Decrement by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0–7	Logical OR contents of designated register with accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0–1	Logical OR indirect the contents of data memory location with accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (A_7)	Rotate accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (C) (C) ← (A_7)	Rotate accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (A_0)	Rotate accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1				

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator (cont)																
RRC A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (C) (C) ← (A_0)	Rotate accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_4–A_7) ← (A_0–A_3)	Swap the two 4-bit nibbles in the accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0–7	Logical XOR contents of designated register with accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0–1	Logical XOR indirect the contents of data memory location with accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0–7 If (Rr) = 0; (PC_0–PC_7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC_0–PC_7) ← addr if B_b = 1 (PC) ← (PC) + 2 if B_b = 0	Jump to specified address if accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC_0–PC_7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC_0–PC_7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC_0–PC_7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Direct jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC_0–PC_7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC_0–PC_7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC_0–PC_7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT0 addr	(PC_0–PC_7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC_0–PC_7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC_0–PC_7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 1	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC_0–PC_7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if timer flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Branch (cont)																
JT0 addr	$(PC_0$–$PC_7) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jump to specified address if test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	$(PC_0$–$PC_7) \leftarrow$ addr if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jump to specified address if test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	$(PC_0$–$PC_7) \leftarrow$ addr if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jump to specified address if accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the external interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the external interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the clock output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select bank 0 (locations 0–2047) of program memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select bank 1 (locations 2048–4095) of program memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select bank 0 (locations 0–7) of data memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select bank 1 (locations 24–31) of data memory.	1	1	0	1	0	1	0	1	1	1				
Data Moves																
MOV A, # data	(A) ← data	Move immediate the specified data into the accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0–7	Move the contents of the designated registers into the accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0–1	Move indirect the contents of data memory location into the accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the program status word into the accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0–7	Move immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0–7	Move accumulator contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0–1	Move indirect accumulator contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0–1	Move immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	1 d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	$(PC_0$–$PC_7) \leftarrow$ (A) (A) ← ((PC))	Move data in the current page into the accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	$(PC_0$–$PC_7) \leftarrow$ (A) $(PC_8$–$PC_{10}) \leftarrow$ 011 (A) ← ((PC))	Move program data in page 3 into the accumulator.	1	1	1	0	0	0	1	1	2	1				

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Data Moves (cont)																
MOVX A, @ R	(A) ← ((Rr)); r = 0–1	Move indirect the contents of external data memory into the accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0–1	Move indirect the contents of the accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ↔ (Rr); r = 0–7	Exchange the accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ↔ ((Rr)); r = 0–1	Exchange indirect contents of accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	$(A_0–A_3) \leftrightarrow ((Rr))_0–((Rr))_3$; r = 0–1	Exchange indirect 4-bit contents of accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement contents of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement contents of flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement contents of flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear contents of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear contents of flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear contents of flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•
Input / Output																
ANL BUS, # data	(bus) ← (bus) AND data	Logical AND immediate specified data with contents of bus.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1–2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND $(A_0–A_3)$; p = 4–7	Logical AND contents of accumulator with designated port (4–7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1–2	Input data from designated port (1–2) into accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (bus)	Input strobed bus data into accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	$(A_0–A_3)$ ← (Pp); p = 4–7 $(A_4–A_7)$ ← 0	Move contents of designated port (4–7) into accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← $(A_0–A_3)$; p = 4–7	Move contents of accumulator to designated port (4–7).	0	0	1	1	1	1	p	p	2	1				
ORL BUS, # data	(bus) ← (bus) OR data	Logical OR immediate specified data with contents of bus.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR $(A_0–A_3)$; p = 4–7	Logical OR contents of accumulator with designated port (4–7).	1	0	0	0	1	1	p	p	2	1				
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1–2	Logical OR immediate specified data with designated port (1–2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(bus) ← (A)	Output contents of accumulator onto bus.	0	0	0	0	0	0	1	0	2	1				
OUTL Pp,A	(Pp) ← (A); p = 1–2	Output contents of accumulator to designated port (1–2).	0	0	1	1	1	0	p	p	2	1				

NEC

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Subroutine																
Registers																
DEC Rr (Rr)	(Rr) ← (Rr) − 1; r = 0–7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0–7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0–1	Increment indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
CALL addr	((SP)) ← (PC), (PSW$_4$–PSW$_7$), (SP) ← (SP) + 1 (PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Call designated subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) = 1 (PC) ← ((SP))	Return from subroutine without restoring program status word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) = 1 (PC) ← ((SP)) (PSW$_4$–PSW$_7$) ← ((SP))	Return from subroutine restoring program status word.	1	0	0	1	0	0	1	1	2	1				
Timer / Counter																
EN TCNTI		Enable internal interrupt flag for timer / counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable internal interrupt flag for timer / counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of timer / counter into accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of accumulator into timer / counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop count for event counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start count for event counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start count for timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No operation performed.	0	0	0	0	0	0	0	0	1	1				

Note:

(1) Operation code designations r and p form the binary representation of the registers and ports involved.

(2) The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

(3) References to the address and data are specified in bytes 2 and/or 1 of the instruction.

(4) Numerical subscripts appearing in the function column reference the specific bits affected.

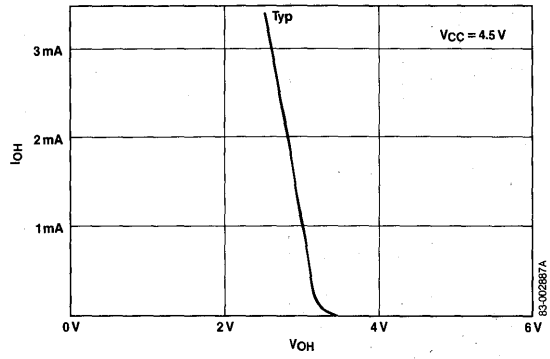
(5) When the bus is written to, with an OUTL instruction, the bus remains an output port until either device is reset or a MOVX instruction is excecuted.

Instruction Set Symbol Definitions

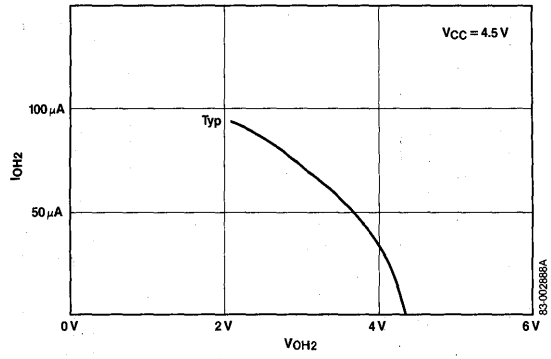
Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program memory address (12 bits)
B_b	Bit designator (b = 0–7)
BS	Bank switch
BUS	Bus port
C	Carry flag
CLK	Clock signal
CNT	Event counter
D	Nibble designator (4 bits)
data	Number of expression (8 bits)
DBF	Memory bank flip-flop
F0, F1	Flags 0, 1
I	Interrupt
P	"In-page" operation designator
Pp	Port designator (p = 1, 2 or 4–7)
PSW	Program status word
Rr	Register designator (r = 0, 1 or 0–7)
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Testable flags 0, 1
X	External RAM
#	Prefix for immediate data
@	Prefix for indirect address
$	Program counter's current value
(x)	Contents of external RAM location
((x))	Contents of memory location addressed by the contents of external RAM location
←	Replaced by
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
XOR	Exclusive-OR

Operating Characteristics

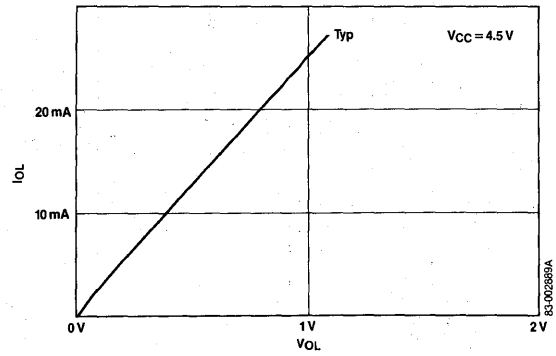
Bus Output High Voltage vs. Source Current



Port P1 & P2 Output High Voltage vs. Source Current



Bus Output Low Voltage vs. Sink Current



μPD80C35/C48, μPD48
8-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

Description

The μPD80C35, μPD80C48, and μPD48 are true stand-alone 8-bit microcomputers fabricated using CMOS technology. All of the functional blocks necessary for an integrated microcomputer are incorporated, including a 1K-byte ROM (μPD80C48 only), a 64-byte RAM, 27 I/O lines, an 8-bit timer/event counter, and a clock generator. This integrated capability permits use in stand-alone applications. For designs requiring extra capability, the μPD80C35/μPD80C48 can be expanded using peripherals and is memory compatible with industry-standard 8080A/8085A processors.

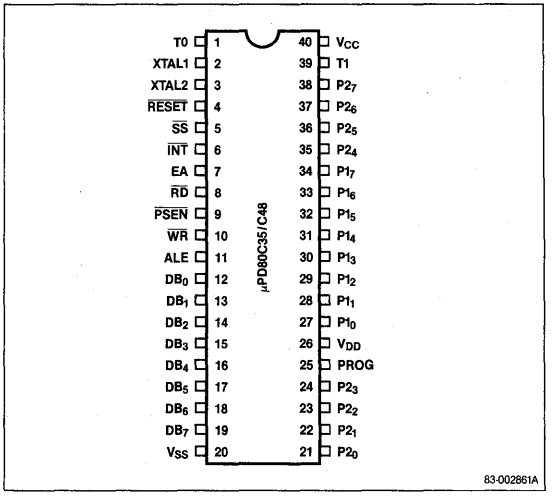
Providing compatibility with industry-standard 8048, 8748, and 8035 processors, the μPD80C35/μPD80C48 features significant savings in power consumption. In addition to the power savings gained through CMOS technology, the μPD80C35/μPD80C48 offers two standby modes (Halt and Stop modes) to further minimize power drain.

Features

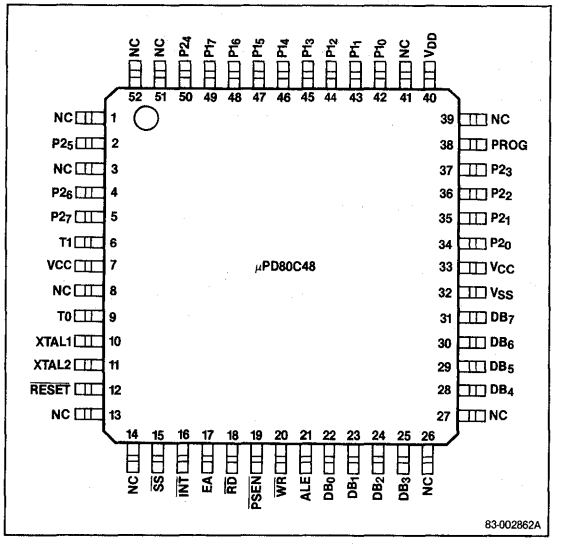
- ☐ 8-Bit CPU with memory and I/O on a single-chip
- ☐ Hardware/software-compatible with industry-standard 8048, 8748, and 8035 processors
- ☐ 1K x 8 ROM (μPD80C48 only)
- ☐ 64 x 8 RAM
- ☐ 27 I/O lines
- ☐ 2.5-μs cycle time (6-MHz crystal)
- ☐ All instructions executable in 1 or 2 cycles
- ☐ 97 instructions: 70 percent are single-byte instructions
- ☐ Internal timer/event counter
- ☐ Two interrupts (external and timer)
- ☐ Easily expandable memory and I/O
- ☐ Bus compatible with 8080A/8085A peripherals
- ☐ Power-efficient CMOS technology requiring a single +2.5 to +6.0 V power supply
- ☐ Halt mode
- ☐ Stop mode

Pin Configurations

40-Pin Plastic DIP

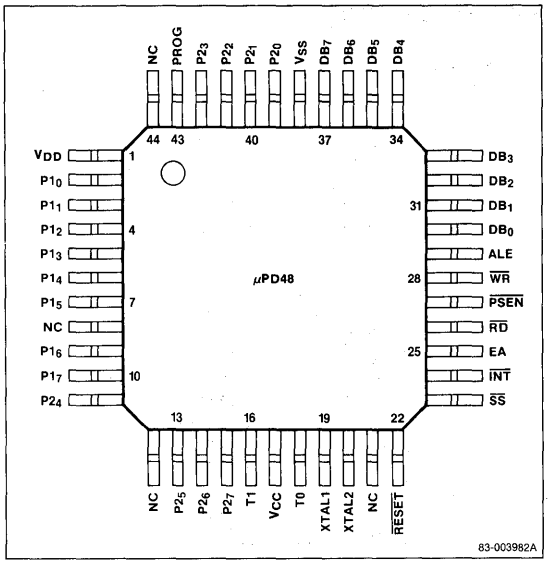


52-Pin Plastic Miniflat



Pin Configurations (cont)

44-Pin Plastic Miniflat



Ordering Information

Part Number	Package Type	Max Frequency of Operation	ROM
μPD80C35C	40-pin plastic DIP	6 MHz	None
μPD80C48C	40-pin plastic DIP	6 MHz	1K x 8
μPD80C48G-00	52-pin plastic miniflat	6 MHz	1K x 8
μPD48G-22	44-pin plastic miniflat	6 MHz	1K x 8

Note:

μPD80C48C, μPD80C48G-00, and μPD48G-22 have two optional port types: type 0, $I_{OH} = -5\,\mu A$; type 1, $I_{OH} = -50\,\mu A$. Type 0 or 1 can be selected independently for $P1_0$-$P1_7$, $P2_0$-$P2_3$, and $P2_4$-$P2_7$.

Pin Identification

Symbol	Function
T0	Test 0 input/clock output
XTAL1	Crystal 1 input
XTAL2	Crystal 2 input
$\overline{RESET}$	Reset input
$\overline{SS}$	Software stop input
$\overline{INT}$	Interrupt input
EA	External access input
$\overline{RD}$	Read output
$\overline{PSEN}$	Program store enable output
$\overline{WR}$	Write output
ALE	Address latch enable output
DB_0-DB_7	Bidirectional data bus
V_{SS}	Ground
$P2_0$-$P2_7$	Quasi-bidirectional port 2
PROG	Program output
V_{DD}	Oscillator control voltage
$P1_0$-$P1_7$	Quasi-bidirectional port 1
T1	Test 1 input
V_{CC}	Primary power supply
NC	No connection

Pin Functions

XTAL1, XTAL2 [Crystals 1, 2]

XTAL1 and XTAL2 are the crystal inputs for the internal clock oscillator. XTAL1 is also used as an input for external clock signals.

T0 [Test 0]

The JT0 and JNT0 instructions test the level of T0 and, if it is high, the program address jumps to the specified address. T0 becomes a clock output when the ENT0 CLK instruction is executed.

T1 [Test 1]

The JT1 and JNT1 instructions test the level of T1 and, if it is high, the program address jumps to the specified address. T1 becomes an internal counter input when the STRT CNT instruction is executed.

$\overline{RESET}$ [Reset]

$\overline{RESET}$ initializes the processor and is also used to verify the internal ROM. $\overline{RESET}$ determines the oscillation stabilizing time during the release of STOP mode. The $\overline{RESET}$ pulse width requires at least 5 machine cycles when the supply voltage is within specifications and the oscillation frequency is stable.

$\overline{SS}$ [Single Step]

$\overline{SS}$ causes the processor to execute the program one step at a time.

$\overline{INT}$ [Interrupt]

$\overline{INT}$ starts an interrupt if interrupts are enabled. A reset disables an interrupt. INT can be tested with the JNI instruction and, depending on the results, a jump to the specified address can occur.

EA [External Access]

EA disables internal program memory and fetches and accesses external program memory. EA is used for system testing and debugging.

$\overline{RD}$ [Read]

$\overline{RD}$ enables a data read from external memory.

$\overline{WR}$ [Write]

$\overline{WR}$ enables a data write to external memory.

$\overline{PSEN}$ [Program Store Enable]

$\overline{PSEN}$ fetches instructions only from external program memory.

ALE [Address Latch Enable]

ALE occurs at each cycle. The falling edge of ALE addresses external data memory or external program memory. ALE can also be used as a clock output.

DB_0-DB_7 [Data Bus]

DB_0-DB_7 is a bidirectional port, which reads and writes data using $\overline{RD}$ and $\overline{WR}$ for latching. During an external program memory fetch, DB_0-DB_7 output the low-order eight bits of the memory address. $\overline{PSEN}$ fetches the instruction. DB_0-DB_7 also output the address of an external data memory fetch. The addressed data is read and written by $\overline{RD}$ and $\overline{WR}$.

$P1_0$-$P1_7$ [Port 1]

$P1_0$-$P1_7$ is an 8-bit quasi-bidirectional port.

$P2_0$-$P2_7$ [Port 2]

$P2_0$-$P2_7$ is an 8-bit quasi-bidirectional port. $P2_0$-$P2_3$ output the high-order four bits of the address during an external program memory fetch. $P2_0$-$P2_3$ also function as a 4-bit I/O bus for the μPD82C43 I/O port expander.

PROG [Program Pulse]

PROG is used as an output pulse during a fetch when interfacing with the μPD82C43 I/O port expander.

V_{DD} [Oscillator Control Voltage]

V_{DD} stops and starts the oscillator in STOP mode. STOP mode is enabled by forcing V_{DD} low during a rest.

V_{CC} [Primary Power Supply]

V_{CC} is the primary power supply. V_{CC} must be between +2.5 V and +6.0 V for normal operation. In STOP mode, V_{CC} must be at least +2.0 V to ensure data retention.

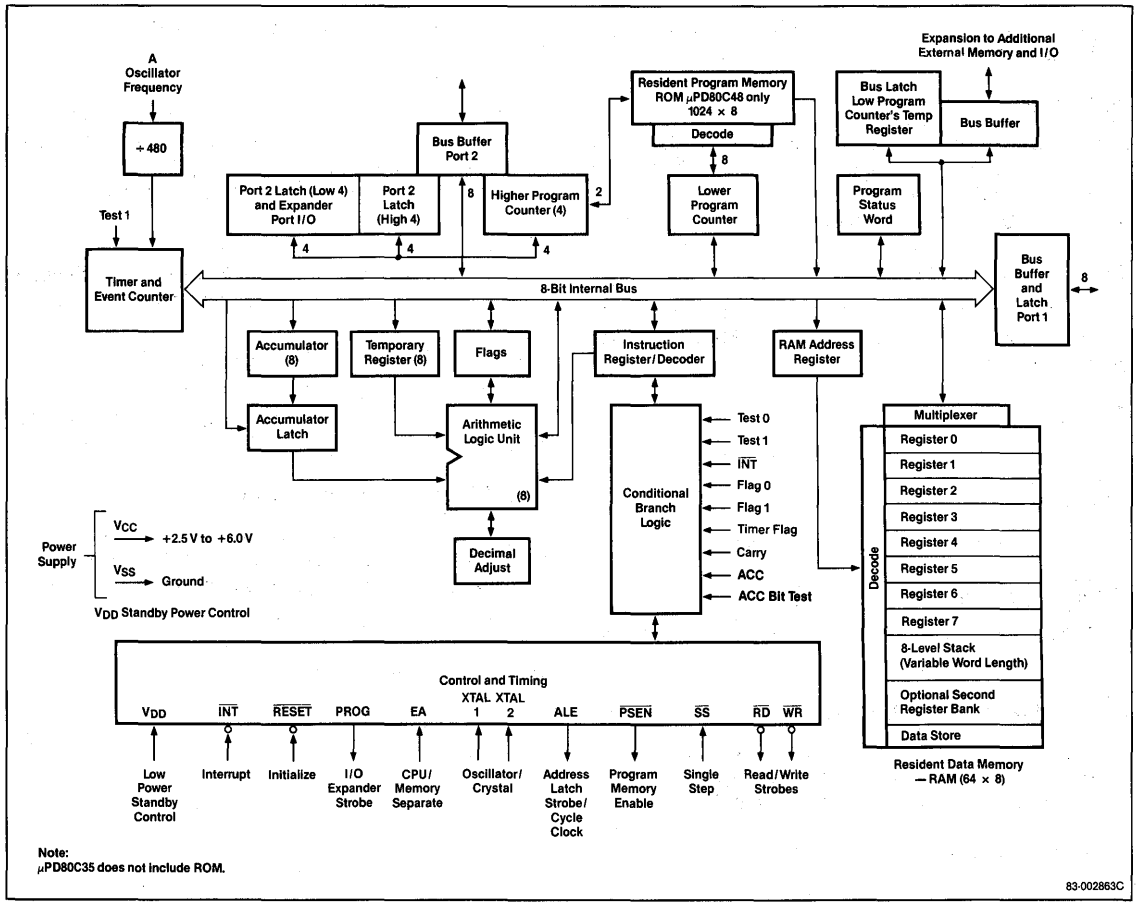
V_{SS} [Ground]

V_{SS} is ground potential.

NC [No Connection]

NC is no connection.

Block Diagram



Note:
μPD80C35 does not include ROM.

83-002863C

Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{CC}	V_{SS} −0.3 to +10 V
Input voltage, V_{IN}	V_{SS} −0.3 to V_{CC} +0.3 V
Output voltage, V_O	V_{SS} −0.3 to V_{CC} +0.3 V
Operating temperature, T_{OPT}	−40°C to +85°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Standard Voltage Range

$T_A = -40°C$ to $+85°C$, $V_{CC} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		+0.8	V	
Input voltage high	V_{IH}	$V_{CC}-2$		V_{CC}	V	Except XTAL1, XTAL2, $\overline{RESET}$
	V_{IH1}	$V_{CC}-1$		V_{CC}	V	$\overline{RESET}$, XTAL1, XTAL2
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 2.0$ mA
Output voltage high	V_{OH}	2.4			V	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; $I_{OH} = -100\,\mu A$
	V_{OH1}(1)	2.4			V	$I_{OH} = -5\,\mu A$ (type 0) port 1, port 2
		2.4			V	$I_{OH} = -50\,\mu A$ (type 1) port 1, port 2
	V_{OH2}	$V_{CC}-0.5$			V	All outputs, $I_{OH} = -0.2\,\mu A$
Input current	I_{ILP}(1)		−15	−40	μA	Port 1, port 2; $V_{IN} \leq V_{IL}$ (type 0)
				−500	μA	Port 1, port 2; $V_{IN} \leq V_{IL}$ (type 1)
	I_{ILC}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \leq V_{IL}$
Input leakage current	I_{LI1}			±1	μA	T1, $\overline{INT}$, V_{CC}; $V_{SS} \leq V_{IN} \leq V_{CC}$
	I_{LI2}			±3	μA	EA; $V_{SS} \leq V_{IN} \leq V_{CC}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} \leq V_O \leq V_{CC}$ High impedance, bus, T0
Standby current	I_{CC1}		0.4	0.8	mA	Halt mode $t_{CY} = 2.5\,\mu s$
	I_{CC2}		1	20	μA	Stop mode (Note 2)
Supply current	I_{CC}		4	8	mA	$t_{CY} = 2.5\,\mu s$
Data retention voltage	V_{CCDR}	2.0			V	Stop mode (V_{DD}, $\overline{RESET} \geq 0.4\,V$)

Extended Voltage Range

$T_A = -40°C$ to $+85°C$, $V_{CC} = +2.5\,V$ to $+6.0\,V$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		$+0.18V_{CC}$	V	
Input voltage high	V_{IH}	$0.7V_{CC}$		V_{CC}	V	Except XTAL1, XTAL2
	V_{IH1}	$0.8V_{CC}$		V_{CC}	V	XTAL1, XTAL2
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 1.0$ mA
Output voltage high	V_{OH}	$0.75V_{CC}$			V	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; $I_{OH} = -100\,\mu A$
	V_{OH1}	$0.7V_{CC}$			V	All other outputs; $I_{OH} = -1\,\mu A$ (type 0) port 1, port 2
		$0.7V_{CC}$			V	All other outputs; $I_{OH} = -10\,\mu A$ (type 1) port 1, port 2
Input current	I_{ILP}		−15	−40	μA	Port 1, port 2; $V_{IN} \leq V_{IL}$ (type 0)
				−500	μA	Port 1, port 2; $V_{IN} \leq V_{IL}$ (type 1)
Input leakage current	I_{IL}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_{IN} \leq V_{IL}$
	I_{LI1}			±1	μA	T1, $\overline{INT}$, $V_{SS} < V_{IN} < V_{CC}$
	I_{LI2}			±5	μA	EA; $V_{SS} < V_{IN} < V_{CC}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} < V_O < V_{CC}$, Bus, T0 — high impedance state
Supply current	I_{CC}		0.8	1.6	mA	$V_{CC} = 3\,V$, $t_{CY} = 10\,\mu s$
			6	12	μA	$V_{CC} = 6\,V$, $t_{CY} = 25\,\mu s$
Standby current	I_{CC1}		100	200	μA	Halt mode; $V_{CC} = 3\,V$, $t_{CY} = 10\,\mu s$
			0.6	1.2	mA	$V_{CC} = 6\,V$, $t_{CY} = 2.5\,\mu s$
	I_{CC2}		1	20	μA	Stop mode, $V_{CC} = 3\,V$
			1	50	μA	$V_{CC} = 6\,V$

Note:

(1) Types 0, 1 for μPD80C48 only.
Type 0 for μPD80C35 only.

(2) Input pin voltage is $V_{IN} \leq V_{IL}$, or $V_{IN} \geq V_{IH}$.

4

AC Characteristics

Read, Write and Instruction Fetch: External Data and Program Memory

$T_A = -40°C$ to $+85°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$

		Limits					
		V_{CC} = +5V ±10%		V_{CC} = 2.5V to 6.0V			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
ALE pulse width	t_{LL}	400		2160		ns	
Address setup before ALE	t_{AL}	120		1620		ns	
Address hold from ALE	t_{LA}	80		330		ns	(Note 1)
Control pulse width ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$)	t_{CC}	700		3700		ns	
Data setup before $\overline{WR}$	t_{DW}	500		3500		ns	
Data hold after $\overline{WR}$	t_{WD}	120		370		ns	(Note 2)
Cycle time	t_{CY}	2.5	150	10	150	μs	6 MHz XTAL
Data hold	t_{DR}	0	200	0	950	ns	
$\overline{PSEN}$, $\overline{RD}$ to data in	t_{RD}		500		2750	ns	
Address setup before $\overline{WR}$	t_{AW}	230		3230		ns	(Note 1)
Address setup before data in	t_{AD}		950		5450		
Address float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0		500		ns	
Control pulse to ALE	t_{CA}	10		10		ns	

Port 2 Timing

$T_A = -40°C$ to $+85°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$; $V_{SS} = 0V$

		Limits					
		V_{CC} = +5V ±10%		V_{CC} = 2.5V to 6.0V			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test Conditions
Port control setup before falling edge of $\overline{PROG}$	t_{CP}	110		860		ns	
Port control hold after falling edge of PROG	t_{PC}	0	80	0	200	ns	(Note 4)
PROG to time P2 input must be valid	t_{PR}		810		5310	ns	
Output data setup time	t_{DP}	250		3250		ns	(Note 3)
Output data hold time	t_{PD}	65		820		ns	
Input data hold time	t_{PF}	0	150	0	900	ns	
PROG pulse width	t_{PP}	1200		6450		ns	
Port 2 I/O data setup time	t_{PL}	350		2100		ns	
Port 2 I/O data hold time	t_{LP}	150		1400		ns	

Note:

(1) Control outputs: $C_L = 80$ pF, bus outputs: $C_L = 150$ pF

(2) $C_L = 20$ pF

(3) Control outputs: $C_L = 80$ pF

(4) Refer to the operating characteristics curves for supply voltage and port control hold.

Bus Timing Requirements (Note 1)

Symbol	Timing Formula	Min/Max	Unit
t_{LL}	(7/30) t_{CY} − 170	Min	ns
t_{AL}	(1/5) t_{CY} − 380	Min	ns
t_{LA}	(1/30) t_{CY}	Min	ns
t_{CC}	(2/5) t_{CY} − 300	Min	ns
t_{DW}	(2/5) t_{CY} − 500	Min	ns
t_{WD}	(1/30) t_{CY} + 40	Min	ns
t_{DR}	(1/10) t_{CY} − 50	Max	ns
t_{RD}	(3/10) t_{CY} − 250	Max	ns
t_{AW}	(2/5) t_{CY} − 770	Min	ns
t_{AD}	(3/5) t_{CY} − 550	Max	ns
t_{AFC}	(1/15) t_{CY} − 165	Min	ns

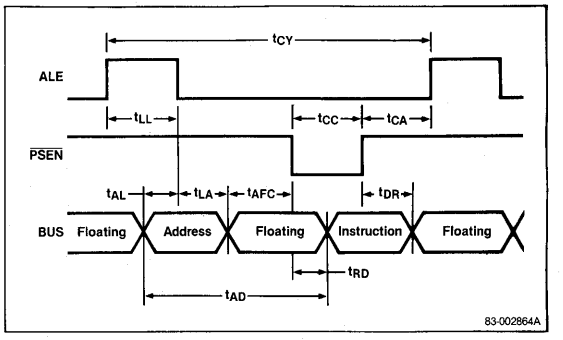
Symbol	Timing Formula	Min/Max	Unit
t_{CP}	(1/10) t_{CY} − 140	Min	ns
t_{PC2}	(4/15) t_{CY} − 200	Min	ns
t_{PR}	(3/5) t_{CY} − 690	Max	ns
t_{PF}	(1/10) t_{CY} − 100	Max	ns
t_{DP}	(2/5) t_{CY} − 750	Min	ns
t_{PD}	(1/10) t_{CY} − 180	Min	ns
t_{PP}	(7/10) t_{CY} − 550	Min	ns
t_{PL}	(7/30) t_{CY} − 230	Min	ns
t_{LP}	(1/6) t_{CY} − 265	Min	ns

Note:

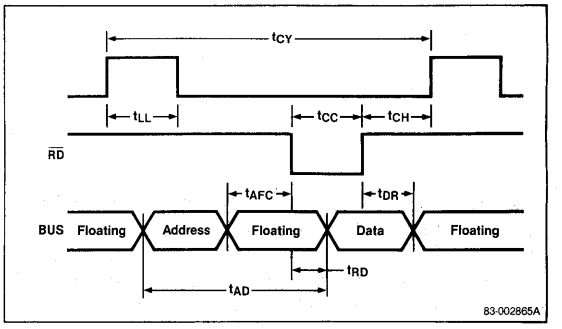
(1) Unlisted parameters are not affected by cycle time.

Timing Waveforms

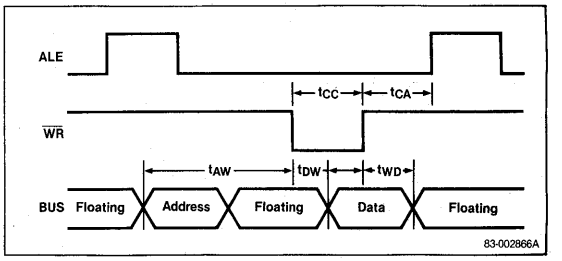
Instruction Fetch From External Memory



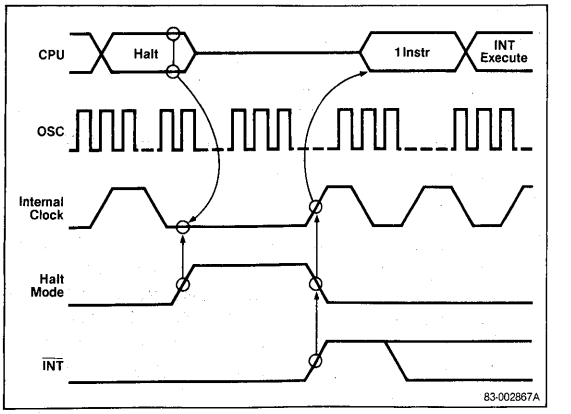
Read From External Data Memory



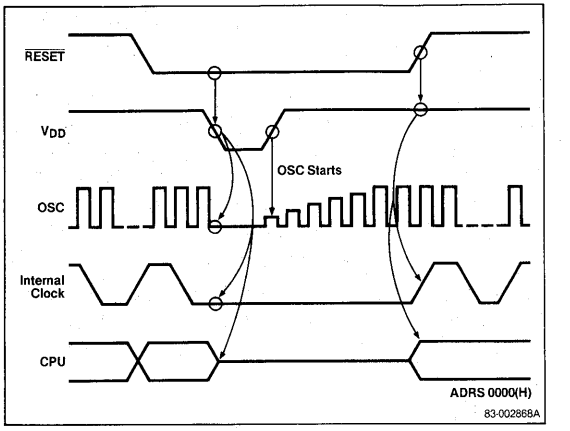
Write to External Memory



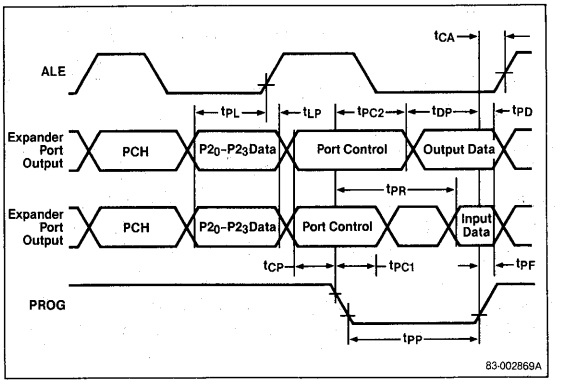
Low Power Standby Operation
1) Halt Mode (When EI)



2) Stop Mode



Port 2 Timing



4

Functional Description

Standby Function

Halt Mode

In Halt mode, the oscillator continues to operate, but the internal clock is disabled. The status of all internal logic just prior to execution of the HALT instruction is maintained by the CPU. In Halt mode, power consumption is less than 10 percent of normal μPD80C48 operation and less than 1 percent of normal 8048 operation.

The Halt mode is initiated by execution of the HALT instruction, and is released by either $\overline{INT}$ or $\overline{RESET}$ input.

INT Input. When the $\overline{INT}$ pin receives a low-level input, if interrupts are enabled, the internal clock is restarted and the interrupt is executed after the first or second instruction following the HALT instruction. However, if interrupts are disabled, program operation is resumed from the next address following the HALT instruction. The first instruction following a HALT instruction should be a NOP instruction to ensure proper program execution.

If the Halt mode is released when interrupts are enabled, the interrupt service routine is usually executed after the first or second instruction following the release of Halt mode. However, if either a timer or external interrupt is accepted within one machine cycle prior to a HALT instruction, the corresponding timer or external interrupt service routine is executed immediately following the release of Halt mode. It is important to note this sequence of execution when considering interrupt service routine execution following a HALT instruction.

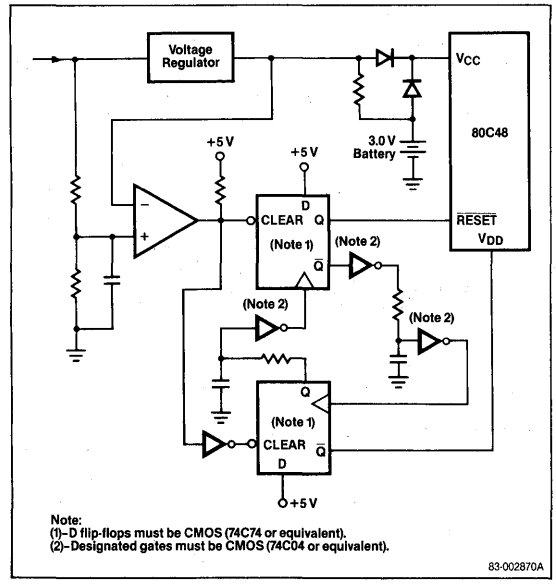
$\overline{RESET}$ Input. When a low-level input is received by the $\overline{RESET}$ pin, Halt mode is released and the normal reset operation is activated, restarting program operation from address 0.

Stop Mode

In Stop mode, the oscillator is deactivated and only the contents of RAM are maintained. The operation status of the μPD80C35/μPD80C48 resembles that of a reset condition. Because only the contents of RAM are maintained, Stop mode provides even lower power consumption than Halt mode, only requiring a minimum V_{CC} as low as +2 V.

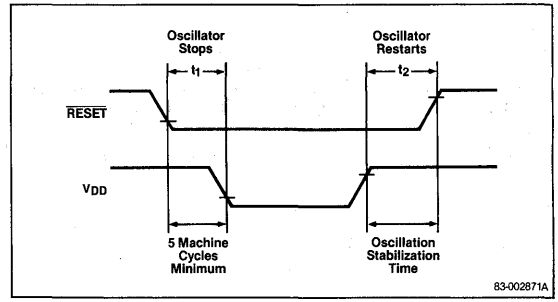
Stop mode is initiated by setting V_{DD} to low when $\overline{RESET}$ is low, to protect the contents of RAM. Stop mode is released by first raising the supply voltage at the V_{CC} pin from standby level to correct operating level and setting V_{DD} to high when $\overline{RESET}$ is low. After the oscillator has been restarted and the oscillation has stabilized, $\overline{RESET}$ must be set to high, whereby program operation is started from address 0. Figure 1 shows the Stop mode circuit.

Figure 1. Stop Mode Circuit



Stop Mode Circuit. Since V_{DD} controls the restarting of the oscillator, it is important that V_{DD} be protected from noise interference. The time required to reset the CPU is represented by t_1 (see figure 2), which is a minimum of 5 machine cycles. The reset operation will not be completed in less than 5 machine cycles. In Stop mode, it is important to note that if V_{DD} goes low before 5 machine cycles have elapsed, the CPU will be deactivated and the output of ALE, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, and PROG will not have been stabilized.

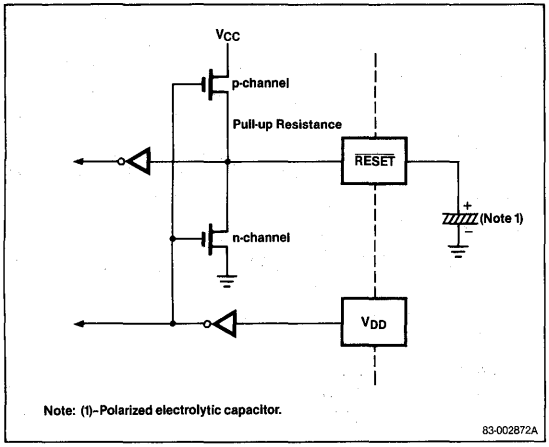
Figure 2. Stop Mode Timing



Oscillation stabilization time is represented by t_2 (see figure 2). When V_{DD} goes high, oscillator operation is reactivated, but it takes time before oscillation can be stabilized. In particular, such high Q resonators as crystals require longer periods to stabilize. Because there is a delay between restarting of the oscillator and oscillator stabilization, t_2 should be long enough to ensure that the oscillator has been fully stabilized.

To facilitate Stop mode control, an external capacitor can be connected to the $\overline{\text{RESET}}$ pin (see figure 3), affecting only t_2, allowing control of the oscillator stabilization time. When V_{DD} is asserted in Stop mode, the capacitor begins charging, pulling up $\overline{\text{RESET}}$. When $\overline{\text{RESET}}$ reaches a threshold level equivalent to a logic 1, Stop mode is released. The time it takes $\overline{\text{RESET}}$ to reach the threshold level of logic 1 determines the oscillator stabilization time, which is a function of the capacitance and pull-up resistance values.

Figure 3. Stop Mode Control Circuit

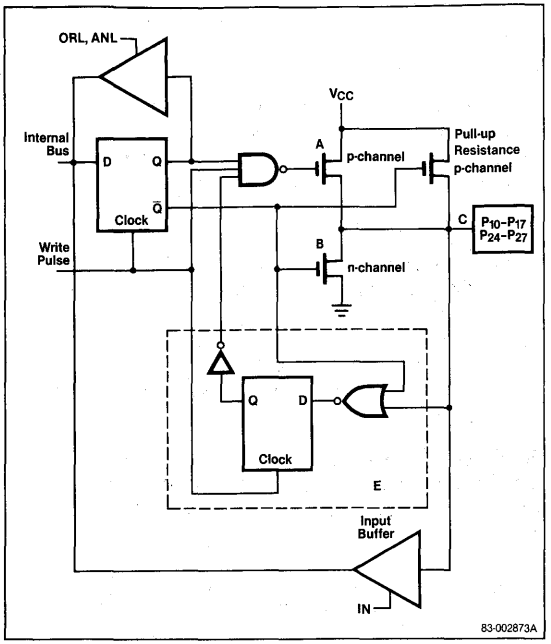


Port Operation

A port-loading option is offered at the time of ordering the mask. Individual source current requirements for Port 1 and the upper and lower halves of Port 2 may be factory set at either $-5\,\mu A$ or $-50\,\mu A$ (see Port-Loading Options table). The $-50\,\mu A$ option is required for interfacing with TTL/NMOS devices. The $-5\,\mu A$ option is recommended for interfacing to other CMOS devices. The CMOS option results in lower power consumption and greater noise immunity.

Port lines $P1_0$-$P1_7$ and $P2_4$-$P2_7$ include a protective circuit "E" to prevent a signal conflict at the port. The circuit prevents a logic 1 from being written to a line that is being pulled down externally (see figure 4, Port Protection Circuit E diagram). When a logic 0 is detected at the port line and a logic 1 is written from the bus, the NOR gate sends a logic 1 to the D input of the flip-flop. The output is inverted, forcing the NAND gate to send a high-level output. This turns off transistor A, preventing the output of a logic 1 from the port.

Figure 4. Port Protection Circuit E



Port-Loading Options

I_{OH} (min) $V_{CC} = V_{DD} = 5\,V \pm 10\%$; $V_{OH} = 2.4\,V$ (min)

Option Selected	$P1_0$-$P1_7$	$P2_0$-$P2_3$	$P2_4$-$P2_7$	Unit
A	−5	−5	−5	μA
B	−50	−5	−5	μA
C	−5	−50	−5	μA
D	−50	−50	−5	μA
E	−5	−5	−50	μA
F	−50	−5	−50	μA
G	−5	−50	−50	μA
H	−50	−50	−50	μA

Note:

(1) The selection of $I_{OH} = -5\,\mu A$ will result in a port source current of $I_{ILP} = -40\,\mu A$ max when used as input port.

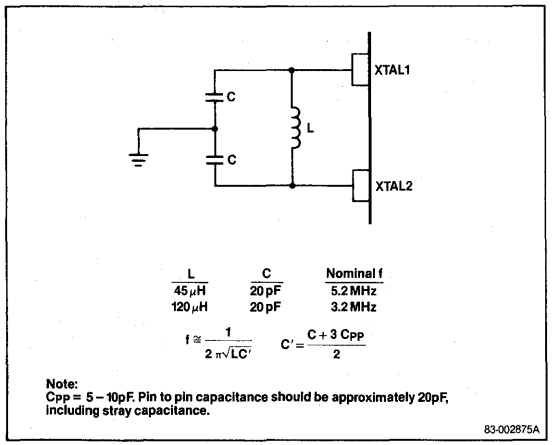
(2) The selection of $I_{OH} = -50\,\mu A$ will result in a port source current of $I_{ILP} = -500\,\mu A$ max when used as input port.

Oscillator Operation

The oscillator maintains an internal frequency for clock generation and controls all system timing cycles. The oscillation is initiated by either a self-generating external resonator or external clock input. The oscillator acts as a high-gain amplifier which produces square-wave pulses at the frequency determined by the resonator or clock source to which it is connected.

To obtain the oscillation frequency, an external LC network (figure 5) may be connected to the oscillator, or, a ceramic or crystal external resonator (figure 6) may be connected.

Figure 5. LC Frequency Reference Circuit



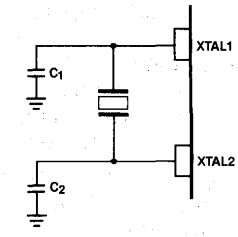
L	C	Nominal f
45 μH	20 pF	5.2 MHz
120 μH	20 pF	3.2 MHz

$$f \cong \frac{1}{2\pi\sqrt{LC'}} \qquad C' = \frac{C + 3\,C_{PP}}{2}$$

Note:
C_{PP} = 5 – 10pF. Pin to pin capacitance should be approximately 20pF, including stray capacitance.

83-002875A

Figure 6. Crystal Frequency Reference Circuit



Notes:
(1) Crystal oscillator constants of
$f_{OSC} = 6\,MHz$
$R_{max} = 50\,\Omega$
$C_L = 16 \pm 0.2\,pF$
$P = 1 \pm 0.2\,mW$

(2) Operating frequency less than 4 MHz
$0 < C_1 \leq 20\,pF$
$0 < C_2 \leq 20\,pF$
$|C_2 - C_1| \leq 10\,pF$

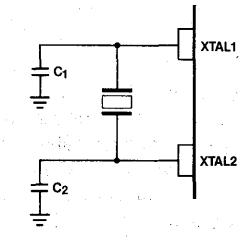
(3) Operating frequency more than 4 MHz
$0 < C_1 \leq 10\,pF$
$0 < C_2 \leq 10\,pF$
$|C_2 - C_1| \leq 5\,pF$

83-002874A

As the crystal frequency is lowered, there is an equivalent reduction in series resistance (R). As the temperature of the crystal is lowered, R is increased. Due to this relationship, it becomes difficult to stabilize oscillation when there is low power supply voltage. When V_{CC} is less than 2.7 V and the oscillator frequency is 3 MHz or less, T_A (ambient temperature) should not be less than −10°C.

Figures 7 and 8 show the ceramic resonator and external clock frequency reference circuits. Figure 9 shows the μPD80C35/μPD80C48 major I/O signals.

Figure 7. Ceramic Resonator Frequency Reference Circuit



Note:
$C_1 > C_2$
$|C_1 - C_2| \cong 20\,pF$
For example, $C_1 = 30\,pF$, and $C_2 = 10\,pF$.
Values of C_1 and C_2 do not include stray capacitance.

83-002876A

Figure 8. External Clock Frequency Reference Circuit

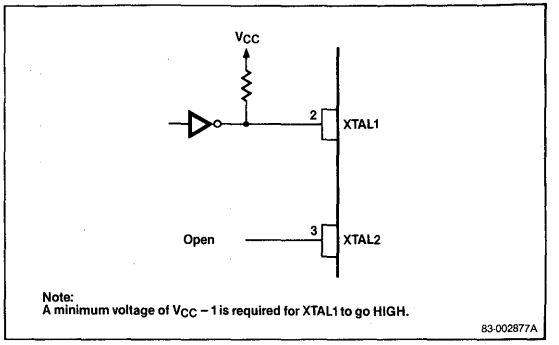
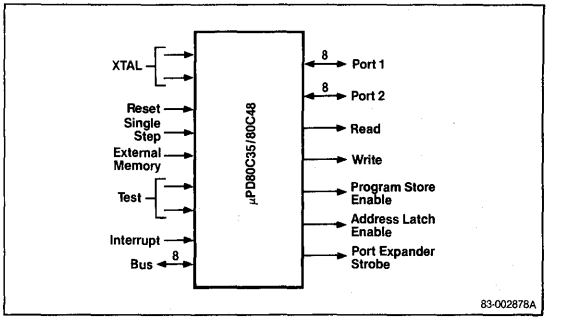


Figure 9. Major Input and Output Signals



Instruction Set

Instruction Set Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program or data memory address (a_0–a_7) or (a_0–a_{10})
b	Accumulator bit (b = 0–7)
BS	Bank switch
BUS	Bus
C	Carry flag
CLK	Clock
CNT	Counter
data	8-bit binary data (d_0–d_7)
DBF	Memory bank flip-flop
F0, F1	Flag 0, flag 1
INT	Interrupt pin
n	Indicates the hex number of the specified register or port
PC	Program counter
Pp	Port 1, port 2, or ports 4–7 (p = 1, 2 or 4–7)
PSW	Program status word
Rr	Register (r = 0–7)

Symbol	Description
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Test 0, test 1 pin
#	Prefix for immediate data
@	Prefix for indirect address
x	Indicates the hex number corresponding to the accumulator bit or page number specified in the operand
(x)	Contents of RAM
((x))	Contents of memory location addressed by (x)
←	Transfer direction, result
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
EXOR	Exclusive-OR
———	Complement

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Accumulator													
ADD A, # data	(A) ← (A) + data	Adds immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags. (Note 2)	03	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, Rr	(A) ← (A) + (Rr) r = 0–7	Adds the contents of register Rr to the accumulator. Sets or clears both carry flags. (Note 2)	6n(4)	0	1	1	0	1	r	r	r	1	1
ADD A, @ Rr	(A) ← (A) + ((Rr)) r = 0–1	Adds the contents of the internal data memory location specified by bits 0–5 of register Rr to the accumulator. Sets or clears both carry flags. (Note 2)	6n(4)	0	1	1	0	0	0	0	r	1	1
ADDC A, # data	(A) ← (A) + (C) + data	Adds, with carry, immediate data d_0–d_7 to the accumulator. Sets or clears both carry flags. (Note 2)	13	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, Rr	(A) ← (A) + (C) + (Rr) r = 0–7	Adds, with carry, the contents of register Rr to the accumulator. Sets or clears both carry flags. (Note 2)	7n(4)	0	1	1	1	1	r	r	r	1	1
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) r = 0–1	Adds, with carry, the contents of the internal data memory location specified by bits 0–5 of register Rr, to the accumulator. Sets or clears both carry flags. (Note 2)	7n(4)	0	1	1	1	0	0	0	r	1	1
ANL A, # data	(A) ← (A) AND data	Takes the logical product (logical AND) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	53	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, Rr	(A) ← (A) AND (Rr) r = 0–7	Takes the logical product (logical AND) of the contents of register Rr and the accumulator, and stores the result in the accumulator.	5n(4)	0	1	0	1	1	r	r	r	1	1
ANL A, @ Rr	(A) ← (A) AND ((Rr)) r = 0–1	Takes the logical product (logical AND) of the contents of the internal data memory location specified by bits 0–5 of register Rr, and the accumulator, and stores the result in the accumulator.	5n(4)	0	1	0	1	0	0	0	r	1	1
CPL A	(A) ← ($\overline{A}$)	Takes the complement of the contents of the accumulator.	37	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clears the contents of the accumulator.	27	0	0	1	0	0	1	1	1	1	1
DA A		Converts the contents of the accumulator to BCD. Sets or clears the carry flags. When the lower 4 bits (A_0–A_3) are greater than 9, or if the auxiliary carry flag has been set, adds 6 to (A_0–A_3). When the upper 4 bits (A_4–A_7) are greater than 9 or if the carry flag (C) has been set, adds 6 to (A_4–A_7). If an overflow occurs at this point, C is set. (Note 2)	57	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) – 1	Decrements the contents of the accumulator by 1.	07	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increments the contents of the accumulator by 1.	17	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A) OR data	Takes the logical sum (logical OR) of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	43	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, Rr	(A) ← (A) OR (Rr) r = 0–7	Takes the logical sum (logical OR) of register Rr and the contents of the accumulator, and stores the result in the accumulator.	4n(4)	0	1	0	0	1	r	r	r	1	1

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Accumulator (cont)													
ORL A, @ Rr	(A) ← (A) OR ((Rr)) r = 0–1	Takes the logical sum (logical OR) of the contents of the internal data memory location specified by bits 0–5 in register Rr, and the contents of the accumulator, and stores the result in the accumulator.	4n(4)	0	1	0	0	0	0	0	r	1	1
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) N = 0–6	Rotates the contents of the accumulator one bit to the left. The MSB is rotated into the LSB.	E7	1	1	1	0	0	1	1	1	1	1
RLC A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (C) (C) ← (A_7)	Rotates the contents of the accumulator one bit to the left through carry.	F7	1	1	1	1	0	1	1	1	1	1
RR A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (A_0)	Rotates the contents of the accumulator one bit to the right. The LSB is rotated into the MSB.	77	0	1	1	1	0	1	1	1	1	1
RRC A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (C) (C) ← (A_0)	Rotates the contents of the accumulator one bit to the right through carry.	67	0	1	1	0	0	1	1	1	1	1
SWAP A	(A_4–A_7) ↔ (A_0–A_3)	Exchanges the contents of the lower 4 bits of the accumulator with the upper 4 bits of the accumulator.	47	0	1	0	0	0	1	1	1	1	1
XRL A, # data	(A) ← (A) XOR data	Takes the exclusive OR of immediate data d_0–d_7 and the contents of the accumulator, and stores the result in the accumulator.	D3	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, Rr	(A) ← (A) XOR (Rr) r = 0–7	Takes the exclusive OR of the contents of register Rr and the accumulator, and stores the result in the accumulator.	Dn(4)	1	1	0	1	1	r	r	r	1	1
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) r = 0–1	Takes the exclusive OR of the contents of the location in data memory specified by bits 0–5 in register Rr, and the accumulator, and stores the result in the accumulator.	Dn(4)	1	1	0	1	0	0	0	r	1	1
Branch													
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0–7 If (Rr) ≠ 0; (PC_0–PC_7) ← addr	Decrements the contents of register Rr by 1, and if the result is not equal to 0, jumps to the address indicated by a_0–a_7.	En	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2
JBb addr	(PC_0–PC_7) ← addr if b = 1 (PC) = (PC) + 2 if b = 0	Jumps to the address specified by a_0–a_7 if the bit in the accumulator specified by b_0–b_2 is set.	x2(6)	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Branch (cont)													
JC addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if C = 1 $(PC) \leftarrow (PC) + 2$ if C = 0	Jumps to the address specified by $a_0\text{-}a_7$ if the carry flag is set.	F6	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if F0 = 1 $(PC) \leftarrow (PC) + 2$ if F0 = 0	Jumps to the address specified by $a_0\text{-}a_7$ if F0 is set.	B6	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if F1 = 1 $(PC) \leftarrow (PC) + 2$ if F1 = 0	Jumps to the address specified by $a_0\text{-}a_7$ if F1 is set.	76	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_8\text{-}PC_{10}) \leftarrow (addr_8\text{-}addr_{10})$ $(PC_0\text{-}PC_7) \leftarrow (addr_0\text{-}addr_7)$ $(PC_{11}) \leftarrow$ DBF	Jumps directly to the address specified by $a_0\text{-}a_{10}$ and the DBF.	x4(6)	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP @ A	$(PC_0\text{-}PC_7) \leftarrow ((A))$	Replaces the lower 8 bits of the program counter with the contents of program memory specified by the contents of the accumulator, producing a jump to the specified address within the current page.	B3	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if C = 0 $(PC) \leftarrow (PC) + 2$ if C = 1	Jumps to the address specified by $a_0\text{-}a_7$ if the carry flag is not set.	E6	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNI addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if I = 0 $(PC) \leftarrow (PC) + 2$ if I = 1	Jumps to the address specified by $a_0\text{-}a_7$ if the interrupt flag is not set.	86	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T0 = 0 $(PC) \leftarrow (PC) + 2$ if T0 = 1	Jumps to the address specified by $a_0\text{-}a_7$ if test 0 is low.	26	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T1 = 0 $(PC) \leftarrow (PC) + 2$ if T1 = 1	Jumps to the address specified by $a_0\text{-}a_7$ if test 1 is low.	46	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if A ≠ 0 $(PC) \leftarrow (PC) + 2$ if A = 0	Jumps to the address specified by $a_0\text{-}a_7$ if the contents of the accumulator are not equal to 0.	96	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JTF addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if TF = 1 $(PC) \leftarrow (PC) + 2$ if TF = 0	Jumps to the address specified by $a_0\text{-}a_7$ if the timer flag is set. The timer flag is cleared after the instruction is executed.	16	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jumps to the address specified by $a_0\text{-}a_7$ if test 0 is high.	36	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jumps to the address specified by $a_0\text{-}a_7$ if test 1 is high.	56	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ	$(PC_0\text{-}PC_7) \leftarrow$ addr if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jump to the address specified by $a_0\text{-}a_7$ if the contents of the accumulator are equal to 0.	C6	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Control													
EN I		Enables external interrupts. When external interrupts are enabled, a low-level input to the INT pin causes the processor to vector to the interrupt service routine.	05	0	0	0	0	0	1	0	1	1	1
DIS I		Disables external interrupts. When external interrupts are disabled, low-level inputs to the INT pin have no effect on program execution.	15	0	0	0	1	0	1	0	1	1	1
ENT0 CLK		Enables clock output to pin T0.	75	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF) ← 0	Clears the memory bank flip-flop, selecting program memory bank 0 (program memory addresses $0–2047_{(10)}$). Clears PC_{11} after the next JMP or CALL instruction.	E5	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF) ← 1	Sets the memory bank flip-flop, selecting program memory bank 1 (program memory addresses $2048–4095_{(10)}$). Sets PC_{11} after the next JMP or CALL instruction.	F5	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS) ← 0	Selects data memory bank 0 by clearing bit 4 (bank switch) of the PSW. Specifies data memory addresses $0–7_{(10)}$ as registers 0–7 of data memory bank 0.	C5	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS) ← 1	Selects data memory bank 1 by setting bit 4 (bank switch) of the PSW. Specifies data memory $24–31_{(10)}$ as registers 0–7 of data memory bank 1.	D5	1	1	0	1	0	1	0	1	1	1
HALT		Initiates halt mode.	01	0	0	0	0	0	0	0	1	1	1
Data Moves													
MOV A, # data	(A) ← data	Moves immediate data $d_0–d_7$ into the accumulator.	23	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, Rr	(A) ← (Rr); r = 0–7	Moves the contents of register Rr into the accumulator.	Fn(4)	1	1	1	1	1	r	r	r	1	1
MOV A, @ Rr	(A) ← ((Rr)); r = 0–1	Moves the contents of internal data memory specified by bits 0–5 in register Rr, into the accumulator.	Fn(4)	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) ← (PSW)	Moves the contents of the program status word into the accumulator.	C7	1	1	0	0	0	1	1	1	1	1
MOV Rr, # data	(Rr) ← data; r = 0–7	Moves immediate data $d_0–d_7$ into register Rr.	Bn(4)	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2
MOV Rr, A	(Rr) ← (A); r = 0–7	Moves the contents of the accumulator into register Rr.	An(4)	1	0	1	0	1	r	r	r	1	1
MOV @ Rr, A	((Rr)) ← (A); r = 0–1	Moves the contents of the accumulator into the data memory location specified by bits 0–5 in register Rr.	An(4)	1	0	1	0	0	0	0	r	1	1
MOV @ Rr, # data	((Rr)) ← data; r = 0–1	Moves immediate data $d_0–d_7$ into the data memory location specified by bits 0–5 in register Rr.	Bn(4)	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Data Moves (cont)													
MOV PSW, A	(PSW) ← (A)	Moves the contents of the accumulator into the program status word.	D7	1	1	0	1	0	1	1	1	1	1
MOVP A, @ A	(PC_0–PC_7) ← (A) (A) ← ((PC))	Moves the contents of the program memory location specified by PC_8–PC_{11} concatenated with the contents of the accumulator, into the accumulator.	A3	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	(PC_0–PC_7) ← (A) (PC_8–PC_{11}) ← 001 (A) ← ((PC))	Moves the contents of the program memory location specified by 0011 (PC_8–PC_{11}, page 3 of program memory bank 0) and the contents of the accumulator, into the accumulator.	E3	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	(A) ← ((Rr)); r = 0–1	Moves the contents of the external data memory location specified by register Rr, into the accumulator.	8n(4)	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	((Rr)) ← (A); r = 0–1	Moves the contents of the accumulator into the external data memory location specified by register Rr.	9n(4)	1	0	0	1	0	0	0	r	2	1
XCH A, Rr	(A) ↔ (Rr); r = 0–7	Exchanges the contents of the accumulator and register Rr.	2n(4)	0	0	1	0	1	r	r	r	1	1
XCH A, @ Rr	(A) ↔ ((Rr)); r = 0–1	Exchanges the contents of the accumulator and the contents of the data memory location specified by bits 0–5 in register Rr.	2n(4)	0	0	1	0	0	0	0	r	1	1
XCHD A, @ Rr	(A_0–A_3) ↔ $((Rr))_0$–$((Rr))_3$; r = 0–1	Exchanges the contents of the lower 4 bits of the accumulator with the contents of the lower 4 bits of the internal data memory location specified by bits 0–5 in register Rr.	3n(4)	0	0	1	1	0	0	0	r	1	1
Flags													
CPL C	(C) ← ($\overline{C}$)	Takes the complement of the carry bit.	A7	1	0	1	0	0	1	1	1	1	1
CPL F0	(F0) ← ($\overline{F0}$)	Takes the complement of flag 0.	95	1	0	0	1	0	1	0	1	1	1
CPL F1	(F1) ← ($\overline{F1}$)	Takes the complement of flag 1.	B5	1	0	1	1	0	1	0	1	1	1
CLR C	(C) ← 0	Clears the carry bit.	97	1	0	0	1	0	1	1	1	1	1
CLR F0	(F0) ← 0	Clears flag 0.	85	1	0	0	0	0	1	0	1	1	1
CLR F1	(F1) ← 0	Clears flag 1.	A5	1	0	1	0	0	1	0	1	1	1

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Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Input / Output													
ANL BUS, # data	(bus) ← (bus) AND data	Takes the logical AND of the contents of the bus and immediate data d_0–d_7, and sends the result to the bus.	98	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ANL Pp, # data	(Pp) ← (Pp) AND data; p = 1–2	Takes the logical AND of the contents of designated port Pp and immediate data d_0–d_7, and sends the result to port Pp for output.	9n(5)	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
ANLD Pp, A	(Pp) ← (Pp) AND (A_0–A_3); p = 4–7	Takes the logical AND of the contents of designated port Pp and the lower 4 bits of the accumulator, and sends the result to port Pp for output.	9n(5)	1	0	0	1	1	1	p	p	2	1
IN A, Pp	(A) ← (Pp); p = 1–2	Loads the accumulator with the contents of designated port Pp.	0n(5)	0	0	0	0	1	0	p	p	2	1
INS A, BUS	(A) ← (bus)	Loads the contents of the bus into the accumulator on the rising edge of $\overline{RD}$.	08	0	0	0	0	1	0	0	0	2	1
MOVD A, Pp	(A_0–A_3) ← (Pp); p = 4–7 (A_4–A_7) ← 0	Moves the contents of designated port Pp to the lower 4 bits of the accumulator, and clears the upper 4 bits.	0n(5)	0	0	0	0	1	1	p	p	2	1
MOVD Pp, A	(Pp) ← (A_0–A_3); p = 4–7	Moves the lower 4 bits of the accumulator to designated port Pp. The upper 4 bits of the accumulator are not changed.	3n(5)	0	0	1	1	1	1	p	p	2	1
ORL BUS, # data	(bus) ← (bus) OR data	Takes the logical OR of the contents of the bus and immediate data d_0–d_7, and sends the result to the bus.	88	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ORLD Pp, A	(Pp) ← (Pp) OR (A_0–A_3); p = 4–7	Takes the logical OR of the contents of designated port Pp and the lower 4 bits of the accumulator, and sends the result to port Pp for output.	8n(5)	1	0	0	0	1	1	p	p	2	1
ORL Pp, # data	(Pp) ← (Pp) OR data; p = 1–2	Takes the logical OR of the contents of designated port Pp and immediate data d_0–d_7, and sends the result to port Pp for output.	9n(5)	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
OUTL BUS, A	(bus) ← (A)	Latches the contents of the accumulator onto the bus on the rising edge of $\overline{WR}$. Note: Never use the OUTL BUS instruction when using external program memory, as this will permanently latch the bus.	02	0	0	0	0	0	0	1	0	2	1
OUTL Pp,A	(Pp) ← (A); p = 1–2	Latches the contents of the accumulator into designated port Pp for output.	3n(5)	0	0	1	1	1	0	p	p	2	1
Registers													
DEC Rr	(Rr) ← (Rr) – 1; r = 0–7	Decrements the contents of register Rr by 1.	Cn(4)	1	1	0	0	1	r	r	r	1	1
INC Rr	(Rr) ← (Rr) + 1; r = 0–7	Increments the contents of register Rr by 1.	1n(4)	0	0	0	1	1	r	r	r	1	1
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0–1	Increments by 1 the contents of the data memory location specified by bits 0–5 in register Rr.	1n(4)	0	0	0	1	0	0	0	r	1	1

Instruction Set (cont)

Mnemonic	Function	Description	Hex Code	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Subroutine													
CALL addr	((SP)) ← (PC), (PSW_4–PSW_7) (SP) ← (SP) + 1 (PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Stores the contents of the program counter and the upper 4 bits of the PSW in the address indicated by the stack pointer, and increments the contents of the stack pointer, calling the subroutine specified by address a_0–a_{10} and the DBF.	x4(6)	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Decrements the contents of the stack pointer by 1 and stores, in the program counter, the contents of the location specified by the stack pointer, executing a return from subroutine without restoring the PSW.	83	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW_4–PSW_7) ← ((SP))	Decrements the contents of the stack pointer by 1 and stores, in the program counter, the contents of the upper 4 bits of the PSW and the contents of the location specified by the stack pointer, executing a return from subroutine with restoration of the PSW.	93	1	0	0	1	0	0	1	1	2	1
Timer / Counter													
EN TCNTI		Enables internal interrupt of timer / event counter. If an overflow condition occurs, then an interrupt will be generated.	25	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disables internal interrupt of timer / event counter.	35	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Moves the contents of the timer / counter into the accumulator.	42	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Moves the contents of the accumulator into the timer / counter.	62	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stops the operation of the timer / event counter.	65	0	1	1	0	0	1	0	1	1	1
STRT CNT		Starts the event counter operation of the timer / counter when T1 changes from a low-level input to a high-level input.	45	0	1	0	0	0	1	0	1	1	1
STRT T		Starts the timer operation of the timer / counter. The timer is incremented every 32 machine cycles.	55	0	1	0	1	0	1	0	1	1	1
Miscellaneous													
NOP		Uses one machine cycle without performing any operation.	00	0	0	0	0	0	0	0	0	1	1

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Instruction Set (cont)

Note:

(1) Binary operation code designations r and p represent encoded values or the lowest-order bit value of specified registers and ports, respectively.

(2) Execution of the ADD, ADDC, and DA instructions affect the carry flags, which are not shown in the respective function equations. These instructions set the carry flags when there is an overflow in the accumulator (the auxiliary carry flag is set when there is an overflow of bit 3 of the accumulator) and clear the carry flags when there is no overflow. Flags that are specifically addressed by flag instructions are shown in the function equations for those instructions.

(3) References to addresses and data are specified in byte 1 and/or 2 in the opcode of the corresponding instruction.

(4) The hex value of n for specific registers is as follows:

a) Direct addressing

R0: n = 8	R2: n = A	R4: n = C	R6: n = E
R1: n = 9	R3: n = B	R5: n = D	R7: n = F

b) Indirect addressing

@ R0: n = 0 @ R1: n = 1

(5) The hex value of n for specific ports is as follows:

P1: n = 9	P4: n = C	P6: n = E
P2: n = A	P5: n = D	P7: n = F

(6) The hex value of x for specific accumulator or address bits is as follows:

a) JBb instruction

B_0: x = 1	B_2: x = 5	B_4: x = 9	B_6: x = D
B_1: x = 3	B_3: x = 7	B_5: x = B	B_7: x = F

b) JMP instruction

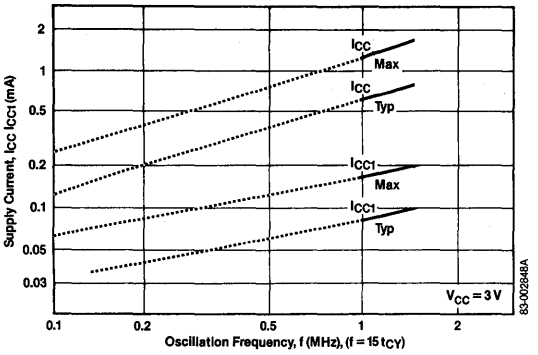
Page 0: x = 0	Page 2: x = 4	Page 4: x = 8	Page 6: x = C
Page 1: x = 2	Page 3: x = 6	Page 5: x = A	Page 7: x = E

c) CALL instruction

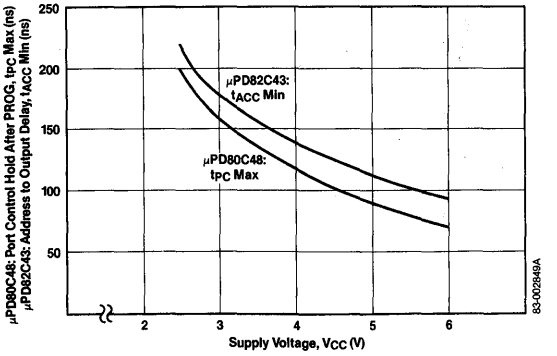
Page 0: x = 1	Page 2: x = 5	Page 4: x = 9	Page 6: x = D
Page 1: x = 3	Page 3: x = 7	Page 5: x = B	Page 7: x = F

Operating Characteristics

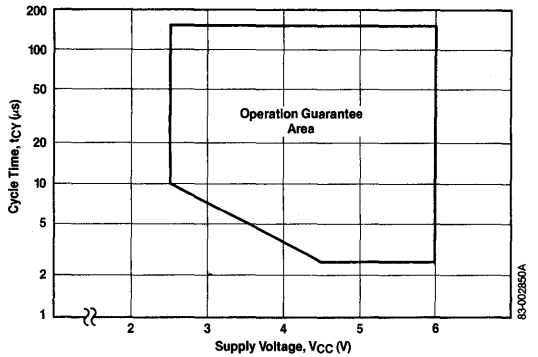
Supply Current vs. Oscillation Frequency



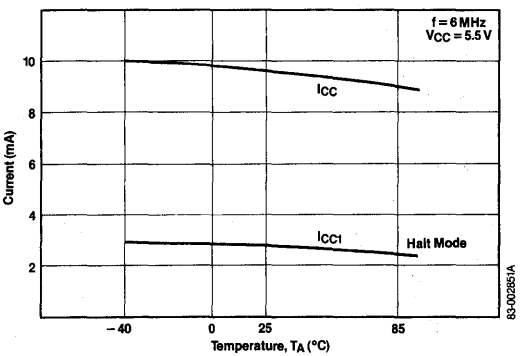
Port Control Hold After PROG, t_{PC} Max (μPD80C48), and Address to Output Delay, t_{ACC} Min (μPD82C43), vs. Supply Voltage



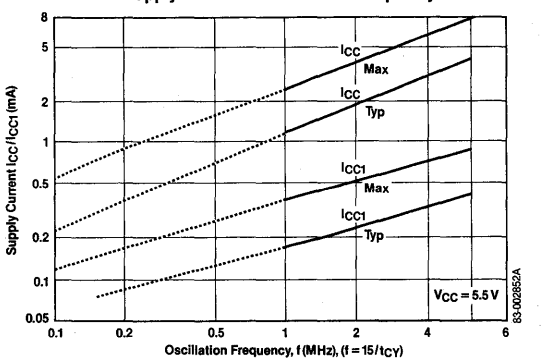
Cycle Time vs. Supply Voltage



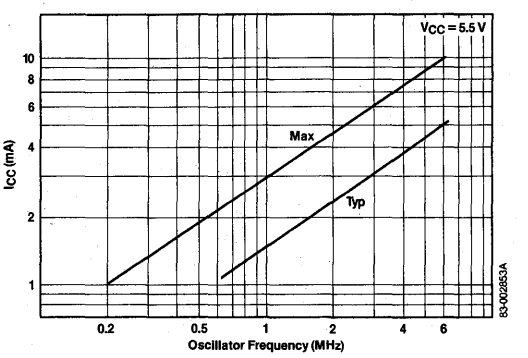
Current Consumption as a Function of Temperature — Normal Operating Mode



Supply Current vs. Oscillation Frequency



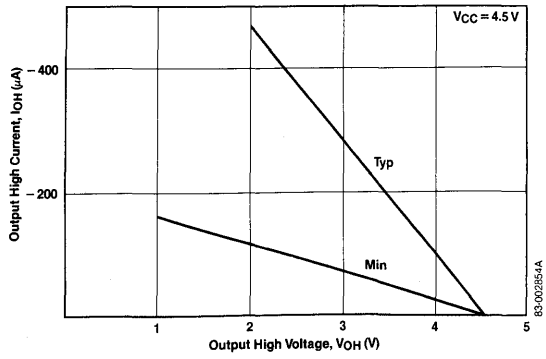
Current Consumption as a Function of Operating Frequency — Normal Operating Mode



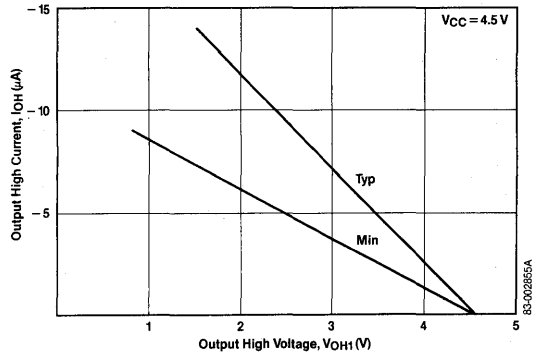
Note: External oscillation is for frequency less than 1 MHz. Internal oscillation requires more power.

Operating Characteristics (cont)

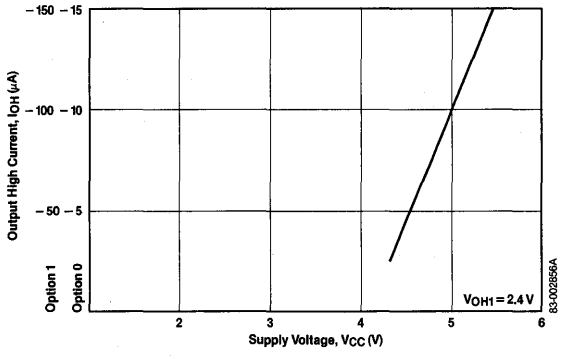
Output High Current vs. Output High Voltage



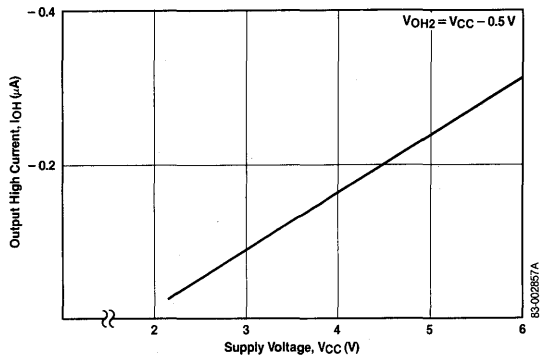
Output High Current vs. Output High Voltage



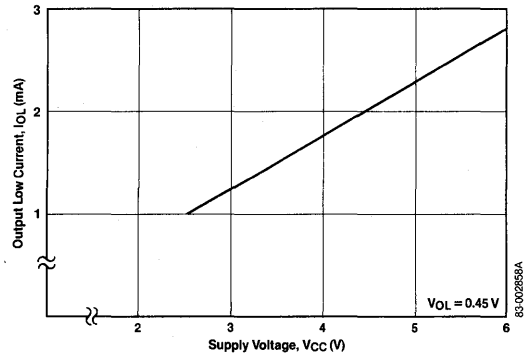
Output High Current vs. Supply Voltage



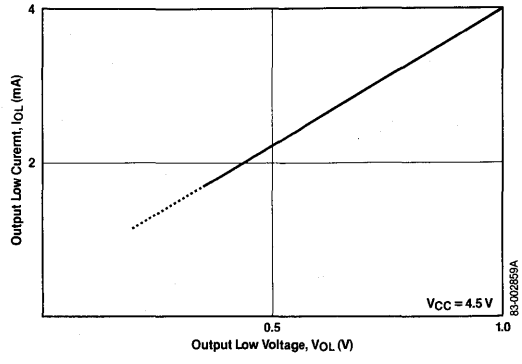
Output High Current vs. Supply Voltage



Output Low Current vs. Supply Voltage

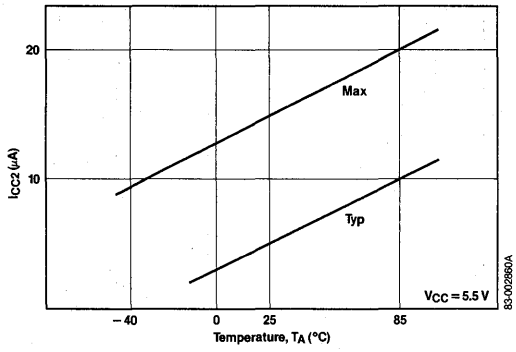


Output Low Current vs. Output Low Voltage



Operating Characteristics (cont)

Current Consumption as a Function of Temperature — Stop Mode



NEC
NEC Electronics Inc.

μPD8039HL/49H, μPD8749H
HIGH-SPEED, 8-BIT, SINGLE-CHIP HMOS MICROCOMPUTERS

Description

The NEC μPD8039HL, μPD8049H and the μPD8749H are high performance, single component, 8-bit parallel microcomputers using n-channel silicon gate MOS technology. The processors differ only in their internal program memory options: the μPD8049H has 2K × 8 bytes of mask ROM, the μPD8749H has 2K × 8 of UV erasable EPROM and the μPD8039HL has external program memory.

The μPD8049H family functions efficiently in control as well as arithmetic applications. The powerful instruction set eases bit handling applications and provides facilities for binary and BCD arithmetic. Standard logic functions implementation is facilitated by the large variety of branch and table look-up instructions. The instruction set is comprised of 1 and 2 byte instructions, most of which are single-byte. The instruction set requires only 1 or 2 cycles per instruction with over 50 percent of the instructions single-cycle.

The μPD8049H family of microprocessors will function as stand-alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories. The μPD8039HL is intended for applications using external program memory only. It contains all the features of the μPD8049H except for the internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products. The μPD8049H contains the following functions usually found in external peripheral devices: 2048 × 8 bits of mask ROM program memory; 128 × 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; and oscillator and clock circuitry. The μPD8749H differs from the μPD8049H in its 2048 × 8-bit UV erasable EPROM program memory instead of the mask ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

Features

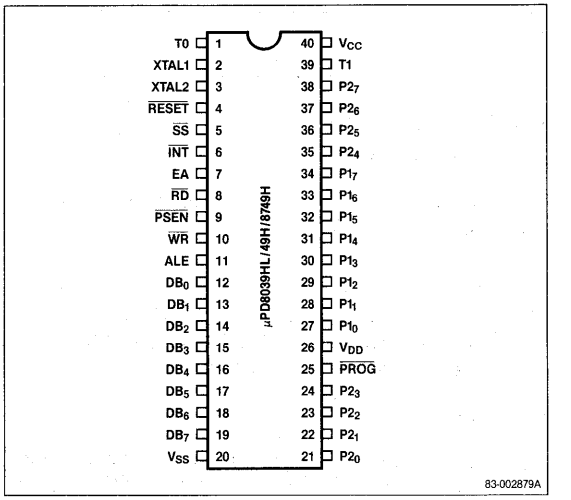
- ☐ High performance 11 MHz operation
- ☐ Fully compatible with industry standard 8039/8049/8749
- ☐ Pin compatible with the μPD8048/8748
- ☐ 1.36 μs cycle time. All instructions 1 or 2 bytes
- ☐ Programmable interval timer/event counter
- ☐ 2K × 8 bytes of ROM, 128 × 8 bytes of RAM
- ☐ External and internal interrupts
- ☐ 96 instructions: 70 percent single byte
- ☐ 27 I/O lines
- ☐ Internal clock generator
- ☐ Expandable with 8080A/8085A peripherals
- ☐ HMOS silicon gate technology
- ☐ Single +5 V ± 10 percent power supply

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8039HLC	40-pin plastic DIP	11 MHz
μPD8049HC	40-pin plastic DIP	11 MHz
μPD8749HC	40-pin plastic DIP	11 MHz
μPD8749HD	40-pin cerdip (Note 1)	11 MHz

Note:
(1) With quartz window.

Pin Configuration



Pin Identification

No.	Symbol	Function
1	T0	Test 0 input / output
2	XTAL1	Crystal 1 input
3	XTAL2	Crystal 2 input
4	$\overline{RESET}$	Reset input
5	$\overline{SS}$	Single step input
6	$\overline{INT}$	Interrupt input
7	EA	External access input
8	$\overline{RD}$	Read output
9	$\overline{PSEN}$	Program store enable output
10	$\overline{WR}$	Write output
11	ALE	Address latch enable output
12-19	DB_0-DB_7	Bidirectional data bus
20	V_{SS}	Ground
21-24	$P2_0$-$P2_7$	Quasi-bidirectional Port 2
25, 35-38	PROG	Program output
26	V_{DD}	RAM power supply
27-34	$P1_0$-$P1_7$	Quasi-bidirectional Port 1
39	T1	Test 1 input
40	V_{CC}	Primary power supply

Pin Functions

XTAL 1 (Crystal 1)

XTAL1 is one side of the crystal, LC, or external frequency source (non-TTL-compatible V_{IH}).

XTAL 2 (Crystal 2)

XTAL2 is the other side of the crystal or frequency source. For external sources, XTAL2 must be driven with the logical complement of the XTAL1 input.

T0 (Test 0)

T0 is the testable input using conditional transfer functions JT0 and JNT0. The internal state clock (CLK) is available to T0 using the ENT0 CLK instruction. T0 can also be used during programming as a testable flag.

T1 (Test 1)

T1 is the testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.

$\overline{RESET}$ (Reset)

An active low on $\overline{RESET}$ initializes the processor. $\overline{RESET}$ is also used for PROM programming verification and power-down (non-TTL compatible V_{IH}).

$\overline{SS}$ (Single Step)

An active low on $\overline{SS}$, together with ALE, causes the processor to execute the program one step at a time.

$\overline{INT}$ (Interrupt)

An active low on $\overline{INT}$ starts an interrupt if interrupts are enabled. A reset disables an interrupt. $\overline{INT}$ can be tested with the JNI instruction and, depending on the results, a jump to the specified address can occur.

EA (External Access)

An active high on EA disables internal program memory and fetches and accesses external program memory. EA is used for system testing and debugging.

$\overline{RD}$ (Read)

$\overline{RD}$ will pulse low when the processor performs a bus read. An active low on $\overline{RD}$ enables data onto the processor bus from a peripheral device and functions as a read strobe for external data memory.

$\overline{WR}$ (Write)

$\overline{WR}$ will pulse low when the processor performs a bus write. $\overline{WR}$ can also function as a write strobe for external data memory.

$\overline{PSEN}$ (Program Store Enable)

$\overline{PSEN}$ becomes active only during an external memory fetch. (Active low).

ALE (Address Latch Enable)

ALE occurs at each cycle. ALE can also be used as a clock output. The falling edge of ALE addresses external data memory or external program memory.

DB_0-DB_7 (Data Bus)

DB_0-DB_7 is a bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the DB_0-DB_7 bus can be latched in a static mode.

During an external memory fetch, DB_0-DB_7 output the low order eight bits of the memory address. $\overline{PSEN}$ fetches the instruction. DB_0-DB_7 also output the address of an external data memory fetch. The addressed data is controlled by ALE, $\overline{RD}$, and $\overline{WR}$.

$P1_0$-$P1_7$ (Port 1)

$P1_0$-$P1_7$ is an 8-bit quasi-bidirectional port.

$P2_0$-$P2_7$ (Port 2)

$P2_0$-$P2_7$ is an 8-bit quasi-bidirectional port. $P2_0$-$P2_3$ output the high order four bits of the address during an external program memory fetch. $P2_0$-$P2_3$ also function as a 4-bit I/O bus for the μPD82C43 I/O port expander.

PROG (Program Pulse)

PROG is used as an output pulse during a fetch when interfacing with the μPD82C43 I/O port expander. When the μPD8049H is used in a stand-alone mode, PROG can be allowed to float.

V_{CC} (Primary Power Supply)

V_{CC} is the primary power supply. V_{CC} is +5V during normal operation.

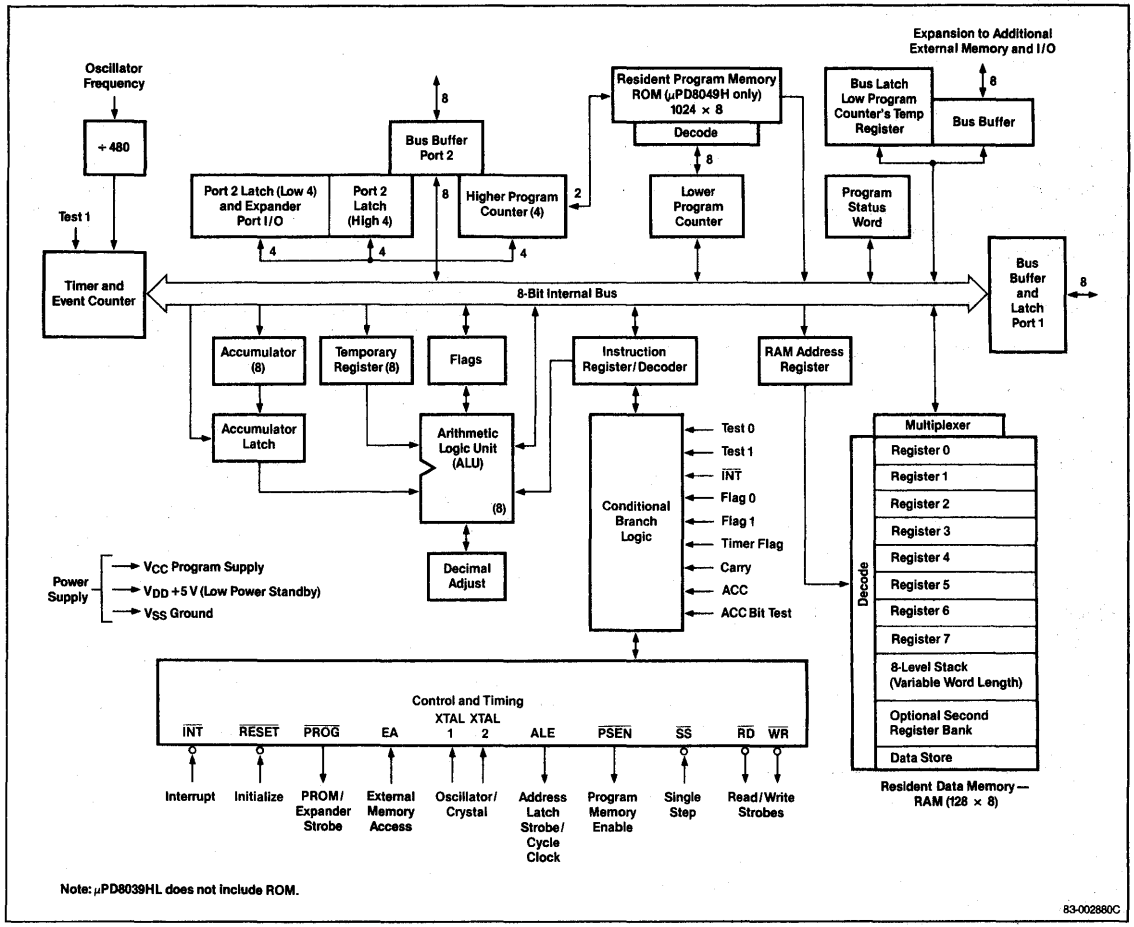
V_{DD} (RAM Power Supply)

V_{DD} provides +5 V to the 128 x 8-bit RAM section. During normal operation, V_{CC} must also be +5 V to provide power to the other functions in the device. During standby operation, V_{DD} must remain at +5 V while V_{CC} is at ground potential.

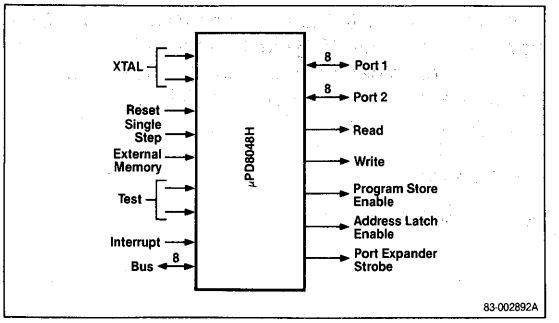
V_{SS} (Ground)

V_{SS} is ground potential.

Block Diagram



Logic Symbol



Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C
Voltage on any pin	−0.5 V to +7.0 V (Note 1)
Power dissipation, P_D	1.5 W

Note:
(1) With respect to ground.

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage (All except XTAL1, XTAL2)	V_{IL}	−0.5		0.8	V	
Input high voltage (All except XTAL1, XTAL2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input high voltage (XTAL1, XTAL2, $\overline{RESET}$)	V_{IH1}	3.8		V_{CC}	V	
Output low voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output low voltage (All others except PROG)	V_{OL1}			0.45	V	$I_{OL} = 2.0$ mA
Output low voltage (PROG)	V_{OL2}			0.45	V	$I_{OL} = 2.0$ mA
Output high voltage (•••)	V_{OH}	2.4			V	$I_{OH} = -400\,\mu A$
Output high voltage (RD, WR, PSEN, ALE)	V_{OH1}	2.4			V	$I_{OH} = -400\,\mu A$
Output high voltage (all other outputs)	V_{OH2}	2.4			V	$I_{OH} = -40\,\mu A$
Input leakage current (T1, EA, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, SS)	I_{IL1}			−500	μA	$V_{SS} + 0.45\,V \leq V_{IN} \leq V_{CC}$
Output leakage current (BUS, T0, high impedance state)	I_{LO}			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45\,V$
Power down supply current	I_{DD}		5	10	mA	$T_A = 25°C$
			2	5		8749H only
Total supply current	$I_{DD} + I_{CC}$		80	110	mA	$T_A = 25°C$
			85	110		8749H only

DC Programming Characteristics

$T_A = 25°C \pm 5°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +21V \pm 0.5V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
V_{DD} program voltage high level	V_{DDH}	20.5		21.5	V	
V_{DD} program voltage low level	V_{DDL}	4.75		5.25	V	
PROG program voltage high level	V_{PH}	17.5		18.5	V	
PROG voltage low level	V_{PL}	4.0		V_{CC}	V	
EA program / verify voltage high level	V_{EAH}	17.5		18.5	V	
V_{DD} high voltage supply current	I_{DD}			20.0	mA	
PROG high voltage supply current	I_{PROG}			1.0	mA	
EA high voltage supply current	I_{EA}			1.0	mA	

AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
ALE pulse width	t_{LL}	150			ns	
Address setup to ALE	t_{AL}	70			ns	
Address hold from ALE	t_{LA}	50			ns	
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	480			ns	
Control pulse width ($\overline{PSEN}$)	t_{CC2}	350			ns	
Data setup before $\overline{WR}$	t_{DW}	390			ns	
Data hold after $\overline{WR}$	t_{WD}	40			ns	(Note 2)
Data hold ($\overline{RD}$, $\overline{PSEN}$)	t_{DR}	0		110	ns	
$\overline{RD}$ to data in	t_{RD1}			350	ns	
$\overline{PSEN}$ to data in	t_{RD2}			210	ns	
Address setup to $\overline{WR}$	t_{AW}	300			ns	
Address setup to data ($\overline{RD}$)	t_{AD1}			750	ns	
Address setup to data ($\overline{PSEN}$)	t_{AD2}			480	ns	
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	140			ns	
Address float to $\overline{PSEN}$	t_{AFC2}	10			ns	
ALE to control ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	200			ns	
ALE to control ($\overline{PSEN}$)	t_{LAFC2}	60			ns	
Control to ALE ($\overline{RD}$, $\overline{WR}$, PROG)	t_{CA1}	50			ns	
Control to ALE ($\overline{PSEN}$)	t_{CA2}	320			ns	
Port control setup to $\overline{PROG}$	t_{CP}	100			ns	
Port control hold to $\overline{PROG}$	t_{PC}	160			ns	
$\overline{PROG}$ to P2 input valid	t_{PR}			650	ns	
Input data hold from $\overline{PROG}$	t_{PF}	0		140	ns	
Output data setup	t_{DP}	400			ns	
Output data hold	t_{PD}	90			ns	
$\overline{PROG}$ pulse width	t_{PP}	700			ns	
Port 2 I/O data setup to ALE	t_{PL}	160			ns	
Port 2 I/O data hold to ALE	t_{LP}	40			ns	
Port output from ALE	t_{PV}			510	ns	
Cycle time	t_{CY}	1.36		15	μs	
I/O rep rate	t_{OPRR}	270			ns	

Note:

(1) Control outputs: $C_L = 60pF$, bus outputs: $C_L = 150pF$

(2) Bus high impedance, load = 20 pF

(3) Calculated values will be equal to or better than published 8049 values.

AC Programming Characteristics

$T_A = 25°C \pm 5°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +21V \pm 0.5V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address setup time to $\overline{RESET}\uparrow$	t_{AW}	$4t_{CY}$				
Address hold time after $\overline{RESET}\uparrow$	t_{WA}	$4t_{CY}$				
Data in setup time to PROG↑	t_{DW}	$4t_{CY}$				
Data in hold time after PROG↓	t_{WD}	$4t_{CY}$				
$\overline{RESET}$ hold time to verify	t_{PH}	$4t_{CY}$				
V_{DD}	t_{VDDW}	0		1.0	ms	
V_{DD} hold time after PROG↓	t_{VDDH}	0		1.0	ms	
PROG pulse width	t_{PW}	50		60	ms	
TEST0 setup time for program mode	t_{TW}	$4t_{CY}$				
TEST0 hold time after program mode	t_{WT}	$4t_{CY}$				
TEST0 to data out delay(1)	t_{DO}			$4t_{CY}$		
$\overline{RESET}$ pulse width to latch address	t_{WW}	$4t_{CY}$				
V_{DD} and PROG rise and fall times	t_r, t_f	0.5		100	μs	

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AC Programming Characteristics (cont)

$T_A = 25°C \pm 5°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +21V \pm 0.5V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
CPU operation cycle time	t_{CY}	4.0		15	μs	
RESET setup time before EA↑	t_{RE}	$4t_{CY}$				

Note:

(1) Control outputs: $C_L = 60$ pF, bus outputs: $C_L = 150$ pF

(2) Bus high impedance, load = 20 pF

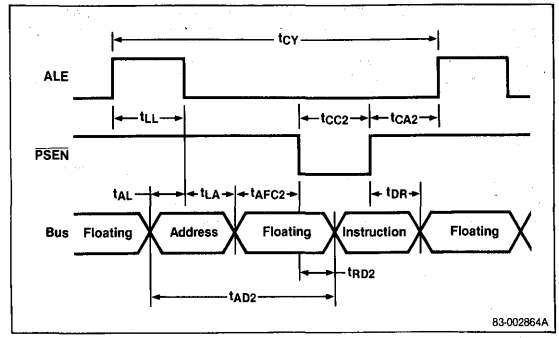
(3) Calculated values will be equal to or better than published 8049 values.

Bus Timing Requirements

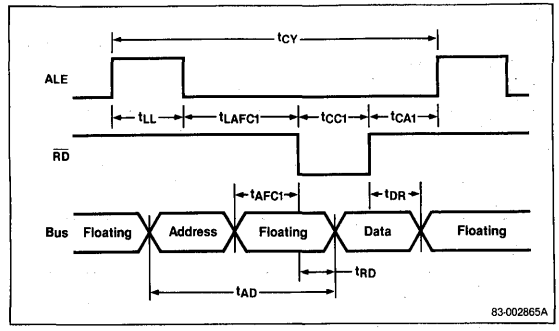
Symbol	Timing Formula	Min/Max	Unit
t_{LL}	$(7/30)\,t_{CY} - 170$	Min	ns
t_{AL}	$(2/15)\,t_{CY} - 110$	Min	ns
t_{LA}	$(1/15)\,t_{CY} - 40$	Min	ns
t_{CC1}	$(1/2)\,t_{CY} - 200$	Min	ns
t_{CC2}	$(2/5)\,t_{CY} - 200$	Min	ns
t_{DW}	$(13/30)\,t_{CY} - 200$	Min	ns
t_{WD}	$(1/15)\,t_{CY} - 50$	Min	ns
t_{DR}	$(1/10)\,t_{CY} - 30$	Max	ns
t_{RD1}	$(2/5)\,t_{CY} - 200$	Max	ns
t_{RD2}	$(3/10)\,t_{CY} - 200$	Max	ns
t_{AW}	$(1/3)\,t_{CY} - 150$	Min	ns
t_{AD1}	$(11/15)\,t_{CY} - 250$	Max	ns
t_{AD2}	$(8/15)\,t_{CY} - 250$	Max	ns
t_{AFC1}	$(2/15)\,t_{CY} - 40$	Min	ns
t_{AFC2}	$(1/30)\,t_{CY} - 40$	Min	ns
t_{LAFC1}	$(1/5)\,t_{CY} - 75$	Min	ns
t_{LAFC2}	$(1/10)\,t_{CY} - 75$	Min	ns
t_{CA1}	$(1/15)\,t_{CY} - 40$	Min	ns
t_{CA2}	$(4/15)\,t_{CY} - 40$	Min	ns
t_{CP}	$(2/15)\,t_{CY} - 80$	Min	ns
t_{PC}	$(4/15)\,t_{CY} - 200$	Min	ns
t_{PR}	$(17/30)\,t_{CY} - 120$	Max	ns
t_{PF}	$(1/10)\,t_{CY}$	Max	ns
t_{DP}	$(2/5)\,t_{CY} - 150$	Min	ns
t_{PD}	$(1/10)\,t_{CY} - 50$	Min	ns
t_{PP}	$(7/10)\,t_{CY} - 250$	Min	ns
t_{PL}	$(4/15)\,t_{CY} - 200$	Min	ns
t_{LP}	$(1/10)\,t_{CY} - 100$	Min	ns
t_{PV}	$(3/10)\,t_{CY} - 100$	Max	ns
t_{OPRR}	$(3/15)\,t_{CY}$	Min	ns
t_{CY}	11 MHz		μs

Timing Waveforms

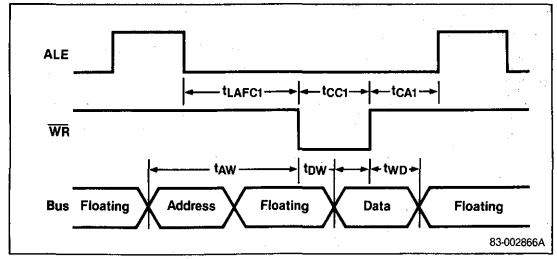
Instruction Fetch from External Memory



Read from External Data Memory

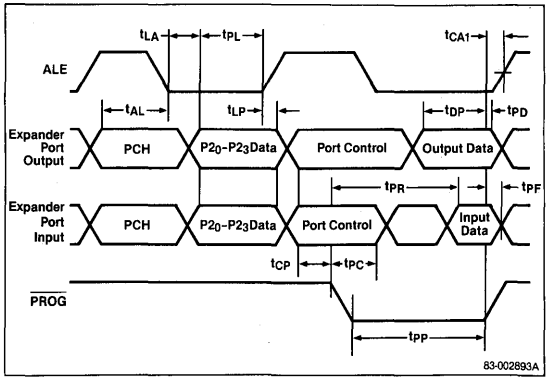


Write to External Memory

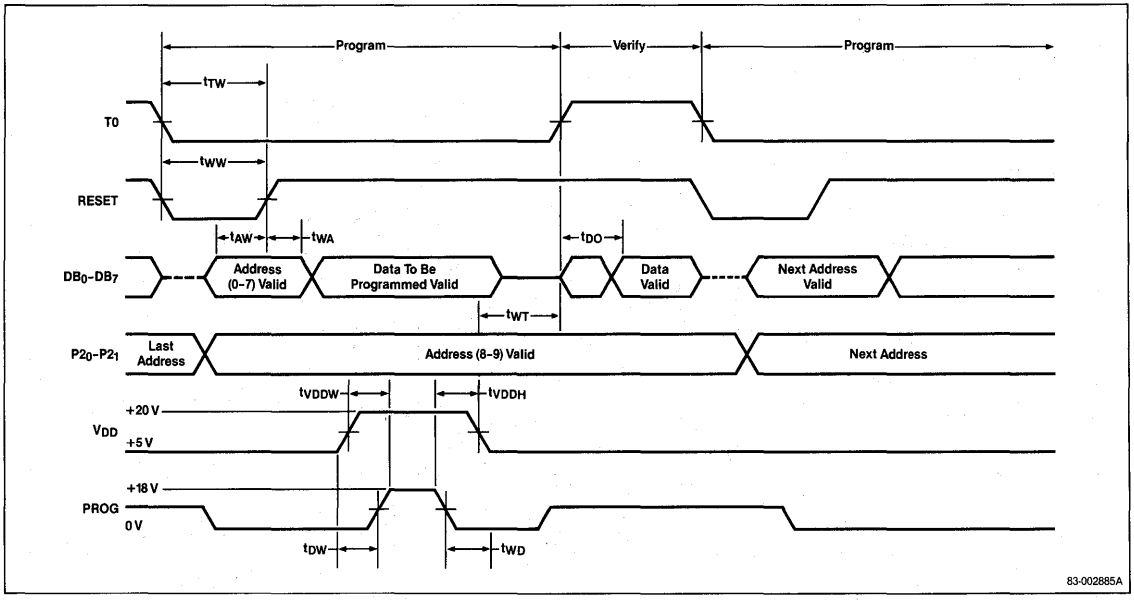


Timing Waveforms (cont)

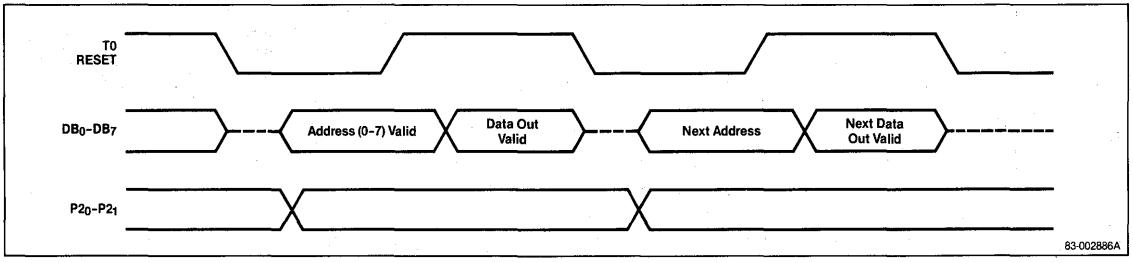
Port 2 Timing



Waveforms for Programming the μPD8749H



Program/Verify Timing (ROM/EPROM)



Instruction Set

Mnemonic	Funciton	Description	Operation Code								Cycles	Bytes	Flags			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
Accumulator																
ADD A, # data	(A) ← (A) + data	Add immediate the specified data to the accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) r = 0–7	Add contents of designated register to the accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) r = 0–1	Add indirect the contents of the data memory location to the accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) r = 0–7	Add with carry the contents of the designated register to the accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) r = 0–1	Add indirect with carry the contents of data memory location to the accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # data	(A) ← (A) AND data	Logical AND specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) r = 0–7	Logical AND contents of designated register with accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) r = 0–1	Logical AND indirect the contents of data memory with accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	Clear the contents of the accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		Decimal adjust the contents of the accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) – 1	Decrement by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) r = 0–7	Logical OR contents of designated register with accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) r = 0–1	Logical OR indirect the contents of data memory location with accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (A_7)	Rotate accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (C) (C) ← (A_7)	Rotate accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (A_0)	Rotate accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1				

NEC

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Accumulator (cont)																
RRC A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (C) (C) ← (A_0)	Rotate accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_4–A_7) ← (A_0–A_3)	Swap the 2 4-bit nibbles in the accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) r = 0–7	Logical XOR contents of designated register with accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) r = 0–1	Logical XOR indirect the contents of data memory location with accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) − 1; r = 0–7 If (Rr) ≠ 0; (PC_0–PC_7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC_0–PC_7) ← addr if B_b = 1 (PC) ← (PC) + 2 if B_b = 0	Jump to specified address if accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC_0–PC_7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC_0–PC_7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC_0–PC_7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Direct jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC_0–PC_7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC_0–PC_7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC_0–PC_7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT0 addr	(PC_0–PC_7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC_0–PC_7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC_0–PC_7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 1	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC_0–PC_7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if timer flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Branch (cont)																
JT0 addr	(PC_0–PC_7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC_0–PC_7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC_0–PC_7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 1	Jump to specified address if accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the external interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the external interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the clock output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select bank 0 (locations 0–2047) of program memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select bank 1 (locations 2048–4095) of program memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select bank 0 (locations 0–7) of data memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select bank 1 (locations 24–31) of data memory.	1	1	0	1	0	1	0	1	1	1				
Data Moves																
MOV A, # data	(A) ← data	Move immediate the specified data into the accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0–7	Move the contents of the designated registers into the accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0–1	Move indirect the contents of data memory location into the accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the program status word into the accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0–7	Move immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0–7	Move accumulator contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0–1	Move indirect accumulator contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0–1	Move immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	1 d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC_0–PC_7) ← (A) (A) ← ((PC))	Move data in the current page into the accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC_0–PC_7) ← (A) (PC_8–PC_{10}) ← 011 (A) ← ((PC))	Move program data in page 3 into the accumulator.	1	1	1	0	0	0	1	1	2	1				

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Instruction Set (cont)

Mnemonic	Function	Description	Operation Code								Cycles	Bytes	Flags			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
Data Moves (cont)																
MOVX A, @ R	(A) ← ((Rr)); r = 0–1	Move indirect the contents of external data memory into the accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0–1	Move indirect the contents of the accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ↔ (Rr); r = 0–7	Exchange the accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ↔ ((Rr)); r = 0–1	Exchange indirect contents of accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	$(A_0–A_3)$ ↔ $((Rr))_0–((Rr))_3$; r = 0–1	Exchange indirect 4-bit contents of accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement contents of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement contents of flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement contents of flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear contents of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear contents of flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear contents of flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•
Input / Output																
ANL BUS, # data	(bus) ← (bus) AND data	Logical AND immediate specified data with contents of bus.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1–2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND $(A_0–A_3)$; p = 4–7	Logical AND contents of accumulator with designated port (4–7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1–2	Input data from designated port (1–2) into accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (bus)	Input strobed bus data into accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	$(A_0–A_3)$ ← (Pp); p = 4–7 $(A_4–A_7)$ ← 0	Move contents of designated port (4–7) into accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← $(A_0–A_3)$; p = 4–7	Move contents of accumulator to designated port (4–7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, # data	(bus) ← (bus) OR data	Logical OR immediate specified data with contents of bus.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR $(A_0–A_3)$; p = 4–7	Logical OR contents of accumulator with designated port (4–7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1–2	Logical OR immediate specified data with designated port (1–2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(bus) ← (A)	Output contents of accumulator onto bus.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1–2	Output contents of accumulator to designated port (1–2).	0	0	1	1	1	0	p	p	1	1				

Instruction Set (cont)

Mnemonic	Function	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Registers																
DEC Rr (Rr)	(Rr) ← (Rr) − 1; r = 0–7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) + 1; r = 0–7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0–1	Increment indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
Subroutine																
CALL addr	((SP)) ← (PC), (PSW_4–PSW_7), (SP) ← (SP) + 1 (PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Call designated subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) − 1 (PC) ← ((SP))	Return from subroutine without restoring program status word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) − 1 (PC) ← ((SP)) (PSW_4–PSW_7) ← ((SP))	Return from subroutine restoring program status word.	1	0	0	1	0	0	1	1	2	1				
Timer / Counter																
EN TCNTI		Enable internal interrupt flag for timer / counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable internal interrupt flag for timer / counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of timer / counter into accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of accumulator into timer / counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop count for event counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start count for event counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start count for timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No operation performed.	0	0	0	0	0	0	0	0	1	1				

Note:

(1) Operation code designations r and p form the binary representation of the registers and ports involved.

(2) The dot under the appropriate flag bit indicates that its contents are subject to change by the instruction it appears in.

(3) References to the address and data are specified in bytes 2 and/or 1 of the instruction.

(4) Numerical subscripts appearing in the function column reference the specific bits affected.

(5) When the bus is written to with an OUTL instruction, the bus remains an output port until either the device is reset or a MOVX instruction is executed.

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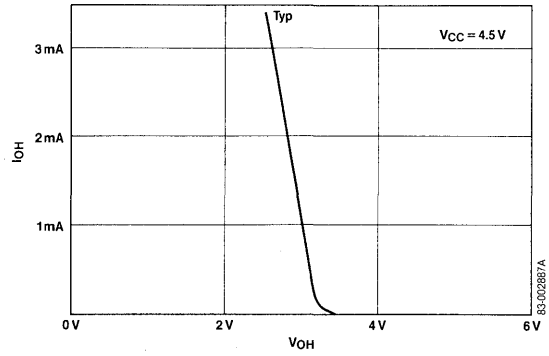
Instruction Set Symbol Definitions

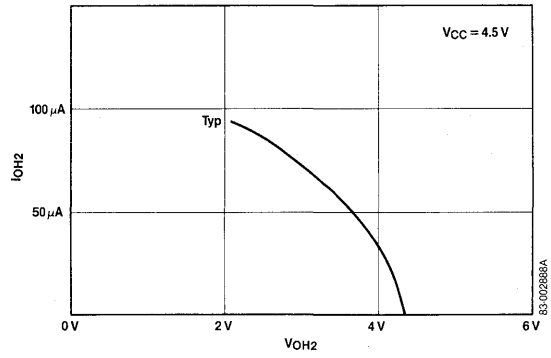
Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program memory address (12 bits)
B_b	Bit designator (b = 0–7)
BS	Bank switch
BUS	Bus port
C	Carry flag
CLK	Clock signal
CNT	Event counter
D	Nibble designator (4 bits)
data	Number of expression (8 bits)
DBF	Memory bank flip-flop
F0, F1	Flags 0, 1
I	Interrupt
P	"In-page" operation designator
Pp	Port designator (p = 1, 2 or 4–7)
PSW	Program status word
Rr	Register designator (r = 0, 1 or 0–7)
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Testable flags 0, 1
X	External RAM
#	Prefix for immediate data
@	Prefix for indirect address
$	Program counter's current value
(x)	Contents of external RAM location
((x))	Contents of memory location addressed by the contents of external RAM location
←	Replaced by
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
EXOR	Exclusive-OR

Operating Characteristics

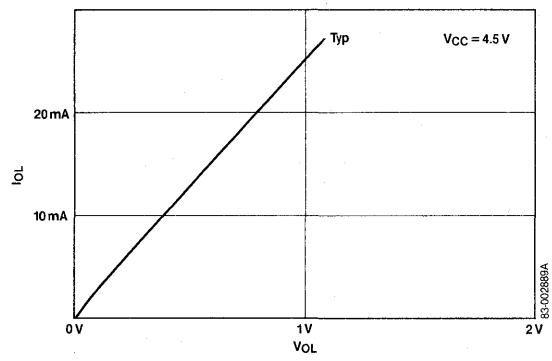
Bus Output High Voltage vs. Source Current



Port P1 & P2 Output High Voltage vs. Source Current



Bus Output Low Voltage vs. Sink Current



4

μPD80C39H/49H, μPD49H
HIGH-SPEED, 8-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

Description

The μPD80C39H, μPD80C49H, and μPD49H are single-chip, 8-bit microcomputers containing an 8-bit CPU, ROM (80C49H and 49H), RAM, I/O ports, and control circuitry. Through CMOS technology, the devices can retain data with low power consumption. In addition, the processor uses two standby modes (HALT and STOP) to further minimize power drain.

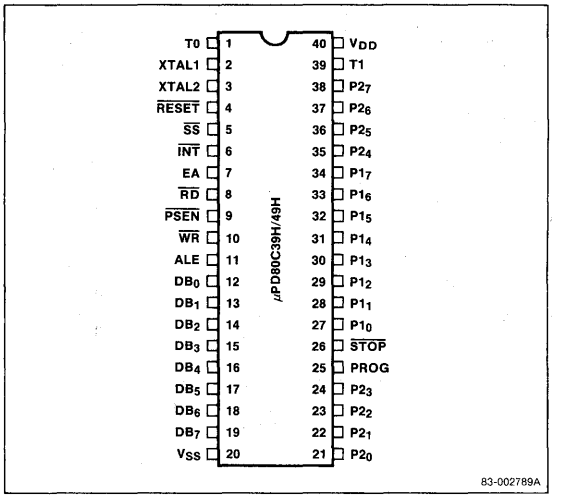
Features

- ☐ 98 instructions
- ☐ 1.25 μs instruction cycle time (12 MHz crystal)
- ☐ Addition, logic, and decimal adjust functions
- ☐ 2K × 8-bit ROM (μPD80C49H and μPD49H)
- ☐ 256 × 8-bit RAM
- ☐ Standby function
- ☐ 8-level stack
- ☐ Two sets of working registers
- ☐ Interrupt capability
- ☐ Two test inputs
- ☐ Internal timer/event counter
- ☐ Input/output ports (8 bits × 2)
  - — Data bus alternative to I/O ports (8 bits × 1)
- ☐ Expandable memory and I/O ports
- ☐ Single-step function
- ☐ Internal clock generator
- ☐ CMOS technology
- ☐ Single power supply of +2.5 to +6.0 V
- ☐ Intel 8049H, 8039H pin compatible

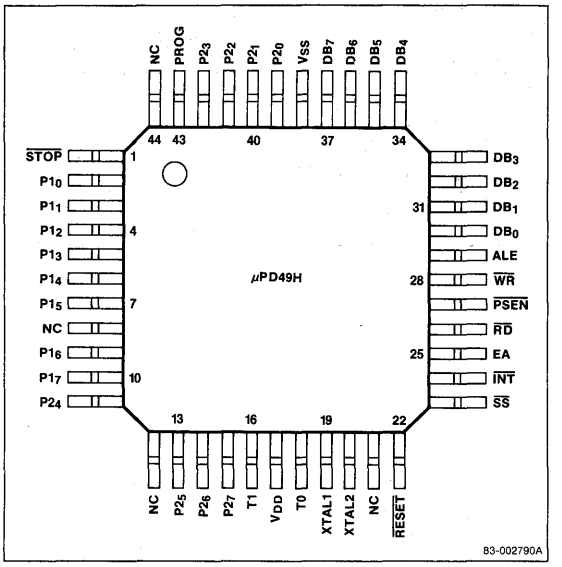
Item	μPD80C49H	μPD80C49
Instructions	98 (STOP instruction added)	97
Instruction Cycle	1.25 μs (12 MHz crystal)	1.875 μs (8 MHz crystal)
Standby Modes	3 (HALT, hardware $\overline{\text{STOP}}$, software STOP)	2 (STOP and HALT)
Standby Functions	All standby modes stop at the same timing. The control signal (ALE) stops in the inactive state whether or not internal or external ROM is accessed.	HALT and STOP modes stop at different timing.
Port Options	Type 0: $I_{OH} = -5\ \mu A$; $V_{DD} = 5\ V \pm 10\%$ Type 1: $I_{OH} = -50\ \mu A$; $V_{DD} = 5\ V \pm 10\%$ Type 2: no pullup resistor	Type 0: $I_{OH} = -5\ \mu A$; $V_{DD} = 5\ V \pm 10\%$ Type 1: $I_{OH} = -50\ \mu A$; $V_{DD} = 5\ V \pm 10\%$

Pin Configurations

40-Pin Plastic DIP



44-Pin Plastic Miniflat



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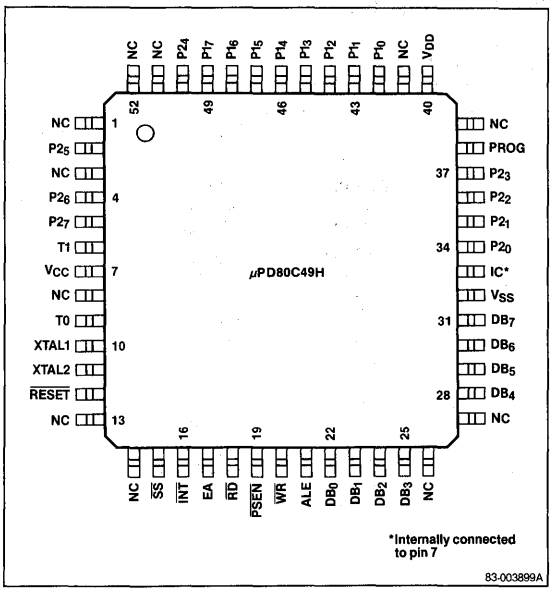
Pin Configurations (cont)

52-Pin Plastic Miniflat



Ordering Information

Part Number	Package Type	Max Frequency of Operation	ROM
μPD80C39HC	40-pin plastic DIP	12 MHz	None
μPD80C49HG-00	52-pin plastic miniflat	12 MHz	2K × 8 bits
μPD80C49HC	40-pin plastic DIP	12 MHz	2K × 8 bits
μPD49HG-22	44-pin plastic miniflat	12 MHz	2K × 8 bits

Pin Identification

Symbol	Function
T0	Test 0 input / clock output
XTAL1	Crystal 1 input
XTAL2	Crystal 2 input
$\overline{RESET}$	Reset input
$\overline{SS}$	Single step input
$\overline{INT}$	Interrupt input
EA	External access input
$\overline{RD}$	Read output
$\overline{PSEN}$	Program store enable output
$\overline{WR}$	Write output
ALE	Address latch enable output
DB_0–DB_7	Bidirectional data bus
V_{SS}	Ground
$P2_0$–$P2_7$	Quasi-bidirectional port 2
PROG	Program output
$\overline{STOP}$	Stop input
$P1_0$–$P1_7$	Quasi-bidirectional port 1
T1	Test 1 input
V_{DD}	Power supply
NC	Not connected
IC	Internal connection

Pin Functions

XTAL1, XTAL2 (Crystals 1, 2)

XTAL1 and XTAL2 are the crystal inputs for the internal clock oscillator. XTAL1 is also used as an input for external clock signals.

T0 (Test 0)

The JT0 and JNT0 instructions test the level of T0 and, if it is high, the program address jumps to the specified address. T0 becomes a clock output when the ENT0 CLK instruction is executed.

T1 (Test 1)

The JT1 and JNT1 instructions test the level of T1 and, if it is high, the program address jumps to the specified address. T1 becomes an internal counter input when the STRT CNT instruction is executed.

$\overline{\text{RESET}}$ (Reset)

$\overline{\text{RESET}}$ initializes the processor and is also used to verify the internal ROM. $\overline{\text{RESET}}$ determines the oscillation stabilizing time during the release of STOP mode. The $\overline{\text{RESET}}$ pulse width requires at least 5 machine cycles when the supply voltage is within specifications and the oscillation frequency is stable. (Active low).

$\overline{\text{SS}}$ (Single Step)

$\overline{\text{SS}}$ causes the processor to execute the program one step at a time. $\overline{\text{SS}}$ also determines the oscillation stabilizing time during the release of the software STOP mode.

$\overline{\text{INT}}$ (Interrupt)

$\overline{\text{INT}}$ starts an interrupt if interrupts are enabled. A reset disables an interrupt. $\overline{\text{INT}}$ can be tested with the JNI instruction and, depending on the results, a jump to the specified address can occur.

EA (External Access)

EA disables internal program memory and fetches and accesses external program memory. EA is used for system testing and debugging. (Active high).

$\overline{\text{RD}}$ (Read)

$\overline{\text{RD}}$ enables a data read from external memory. (Active low).

$\overline{\text{WR}}$ (Write)

$\overline{\text{WR}}$ enables a data write to external memory.

$\overline{\text{PSEN}}$ (Program Store Enable)

$\overline{\text{PSEN}}$ fetches instructions only from external program memory. (Active low).

ALE (Address Latch Enable)

ALE occurs at each cycle. The falling edge of ALE addresses external data memory or external program memory. ALE can also be used as a clock output.

DB_0-DB_7 (Data Bus)

DB_0-DB_7 is a bidirectional port. DB_0-DB_7 reads and writes data using $\overline{\text{RD}}$ and $\overline{\text{WR}}$ for latching. During an external program memory fetch, DB_0-DB_7 output the low-order eight bits of the memory address. $\overline{\text{PSEN}}$ fetches the instruction. DB_0-DB_7 also output the address of an external data memory fetch. The addressed data is read and written by $\overline{\text{RD}}$ and $\overline{\text{WR}}$.

$P1_0$-$P1_7$ (Port 1)

$P1_0$-$P1_7$ is an 8-bit quasi-bidirectional port.

$P2_0$-$P2_7$ (Port 2)

$P2_0$-$P2_7$ is an 8-bit quasi-bidirectional port. $P2_0$-$P2_3$ output the high-order four bits of the address during an external program memory fetch. $P2_0$-$P2_3$ also function as a 4-bit I/O bus for the μPD82C43 I/O port expander.

PROG (Program Pulse)

PROG is used as an output pulse during a fetch when interfacing with the μPD82C43 I/O port expander.

$\overline{\text{STOP}}$ (Stop)

$\overline{\text{STOP}}$ controls the hardware STOP mode. $\overline{\text{STOP}}$ stops the oscillator when active low.

V_{DD} (Power Supply)

V_{DD} is the positive power supply (+2.5 V to +6.0 V).

V_{SS} (Ground)

V_{SS} is ground potential.

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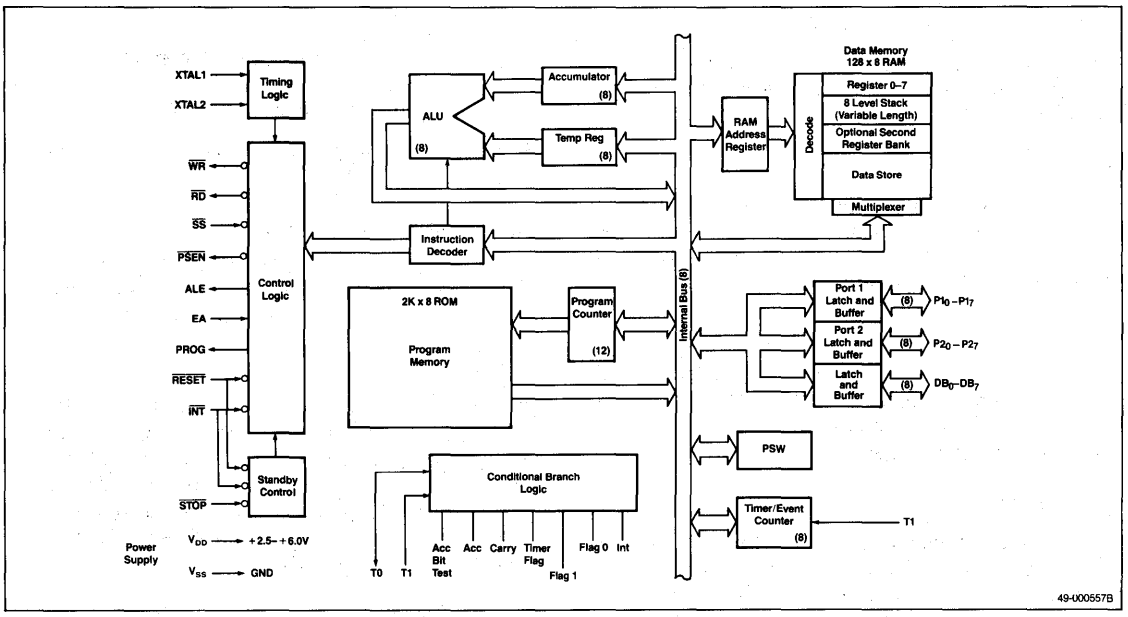
Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	$V_{SS} - 0.3$ V to +7 V
Input voltage, V_I	$V_{SS} - 0.3$ V to V_{DD} +0.3 V
Output voltage, V_O	$V_{SS} - 0.3$ V to V_{DD} +0.3 V
Operating temperature, T_{OPT}	−40°C to +85°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Standard Voltage Range

$T_A = -40°C$ to +85°C, $V_{DD} = +5$ V ± 10%, $V_{SS} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		+0.8	V	
Input voltage high	V_{IH}	$V_{DD}-2$		V_{DD}	V	Except XTAL1, XTAL2, RESET, SS
	V_{IH1}	$V_{DD}-1$		V_{DD}	V	RESET, XTAL1, XTAL2, SS
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 2.0$ mA
Output voltage high	V_{OH}	2.4			V	Bus, RD, WR, PSEN, ALE, PROG, T0; $I_{OH} = -400\,\mu$A
	V_{OH1}(1)	2.4			V	$I_{OH} = -5\,\mu$A (type 0) port 1, port 2
		2.4			V	$I_{OH} = -50\,\mu$A (type 1) port 1, port 2
	V_{OH2}	$V_{DD}-0.5$			V	All outputs, $I_{OH} = -0.2\,\mu$A
Input current	I_{ILP}(1)		−15	−40	μA	Port 1, port 2; $V_I \leq V_{IL}$ (type 0)
				−500	μA	Port 1, port 2; $V_I \leq V_{IL}$ (type 1)
	I_{ILC}			−40	μA	SS, RESET; $V_I \leq V_{IL}$

DC Characteristics (cont)

Standard Voltage Range (cont)

$T_A = -40°C$ to $+85°C$, $V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI1}			±1	μA	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leq V_I \leq V_{DD}$
	I_{LI2}			±3	μA	EA; $V_{SS} \leq V_I \leq V_{DD}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} \leq V_O \leq V_{DD}$ High impedance, bus, T0(3)
Standby current	I_{DD1}(4)		1.5	3.0	mA	$t_{CY} = 1.25$ μs
	I_{DD2}(5)		1	20	μA	(2)
Supply current (total)	I_{DD}		6	18	mA	$t_{CY} = 1.25$ μs
Data retention voltage	V_{DDDR}	2.0			V	At hardware STOP mode ($\overline{STOP}$, $\overline{RESET} \leq 0.4$ V) or $\overline{RESET}$ ($\overline{RESET} \leq 0.4$ V)

Extended Voltage Range

$T_A = -40°C$ to $+85°C$, $V_{DD} = +2.5V$ to $+6.0V$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		+0.18V_{DD}	V	
Input voltage high	V_{IH}	0.7V_{DD}		V_{DD}	V	Except XTAL1, $\overline{RESET}$, $\overline{SS}$
	V_{IH1}	0.8V_{DD}		V_{DD}	V	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 1.0$ mA
Output voltage high	V_{OH}	0.75V_{DD}			V	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; $I_{OH} = -100$ μA
	V_{OH1}(1)	0.7V_{DD}			V	$I_{OH} = -1$ μA (type 0) port 1, port 2
		0.7V_{DD}			V	$I_{OH} = -10$ μA (type 1) port 1, port 2
Input current	I_{ILP}(1)		−15	−40	μA	Port 1, port 2; $V_I \leq V_{IL}$ (type 0)
				−500	μA	Port 1, port 2; $V_I \leq V_{IL}$ (type 1)
	I_{ILC}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$
Input leakage current	I_{LI1}			±1	μA	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leq V_I \leq V_{DD}$
	I_{LI2}			±5	μA	EA; $V_{SS} \leq V_I \leq V_{DD}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} \leq V_O \leq V_{DD}$ High impedance, bus, T0 (3)

Extended Voltage Range (cont)

$T_A = -40°C$ to $+85°C$, $V_{DD} = +2.5V$ to $+6.0V$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Standby current	I_{DD1}(4)		0.3	0.6	mA	$V_{DD} = 3V$; $t_{CY} = 5$ μs
			2.0	4.0	mA	$V_{DD} = 6V$ $t_{CY} = 1.25$ μs
	I_{DD2}(5)		1	20	μA	(2) ; $V_{DD} = 3V$
			1	50	μA	$V_{DD} = 6V$
Supply current	I_{DD}		2.0	4.0	mA	$V_{DD} = 3V$; $t_{CY} = 5$ μs
			10	20	mA	$V_{DD} = 6V$; $t_{CY} = 1.25$ μs

Note:

(1) Types 0, 1, and 2 options can be specified for μPD80C49H. Type 0 for μPD80C39H only.

(2) Input pin voltage is $V_I \leq V_{IL}$ or $V_I \geq V_{IH}$.

(3) Includes port 1 and port 2 pins optionally specified with type 2.

(4) HALT mode.

(5) STOP mode.

AC Characteristics

$T_A = -40°C$ to $+85°C$, $V_{SS} = 0V$

Parameter	Symbol	Limits V_{DD} = +5V ±10% Min	Max	V_{DD} = 2.5V to 6.0V Min	Max	Unit	Test Conditions
Cycle time	t_{CY}	1.25	150	5	150	μs	
ALE pulse width	t_{LL}	125		995		ns	(1)
Address setup before ALE	t_{AL}	140		890		ns	(1)
Address hold from ALE	t_{LA}	45		295		ns	(1)
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	425		2300		ns	(1)
Control pulse width ($\overline{PSEN}$)	t_{CC2}	300		1400		ns	(1)
Data setup before $\overline{WR}$	t_{DW}	340		1965		ns	(1)
Data hold after $\overline{WR}$	t_{WD}	45		295		ns	(2)
Data hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}	0	95	0	470	ns	(1)
$\overline{RD}$ to data in	t_{RD1}		300		1800	ns	(1)
$\overline{PSEN}$ to data in	t_{RD2}		175		1300	ns	(1)
Address setup before $\overline{WR}$	t_{AW}	350		1850		ns	(1)
Address setup before data in ($\overline{RD}$)	t_{AD1}		700		3585		(1)

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AC Characteristics (cont)

$T_A = -40°C$ to $+85°C$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits V_{DD} = +5 V ±10% Min	Max	Limits V_{DD} = 2.5 V to 6.0 V Min	Max	Unit	Test Conditions
Address setup before data in ($\overline{PSEN}$)	t_{AD2}		500		2750	ns	(1)
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	105		600		ns	(1)
Address float to $\overline{PSEN}$	t_{AFC2}	5		125		ns	(1)
ALE to control signal ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	175		925		ns	(1)
ALE to control signal ($\overline{PSEN}$)	t_{LAFC2}	50		425		ns	(1)
Control signal ($\overline{RD}$, $\overline{WR}$, PROG) to ALE	t_{CA1}	35		285		ns	(1)
Control signal ($\overline{PSEN}$) to ALE	t_{CA2}	280		1285		ns	(1)
Port control setup before falling edge of PROG	t_{CP}	85		460		ns	(3)
Port control hold	t_{PC1}	0	80	0	200	ns	(3, 4)
Port control hold after falling edge of PROG	t_{PC2}	135		1135		ns	(3, 5)
PROG to time P2 input must be valid	t_{PR}		585		2715	ns	(3)
Input data hold time	t_{PF}	0	125	0	500	ns	(3)
Output data setup time	t_{DP}	350		1850		ns	(3)
Output data hold time	t_{PD}	75		450		ns	(3)
PROG pulse width	t_{PP}	625		3250		ns	(3)
Port 2 I/O data setup time	t_{PL}	135		1135		ns	(3)
Port 2 I/O data hold time	t_{LP}	5		125		ns	(3)
ALE to port output	t_{PV}		475		1600	ns	(3)
T0 clock period	t_{OPRR}	250		1000		ns	(3)

Note:

(1) Control output: $C_L = 80\,pF$, bus output: $C_L = 150\,pF$

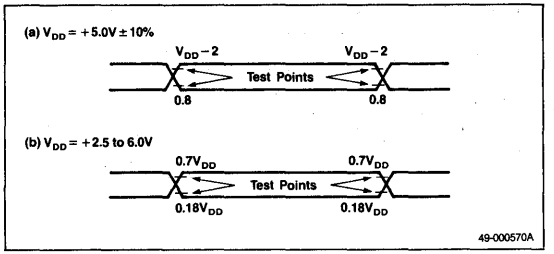
(2) $C_L = 20\,pF$

(3) Control output: $C_L = 80\,pF$

(4) At execution of MOVD A, Pp instruction

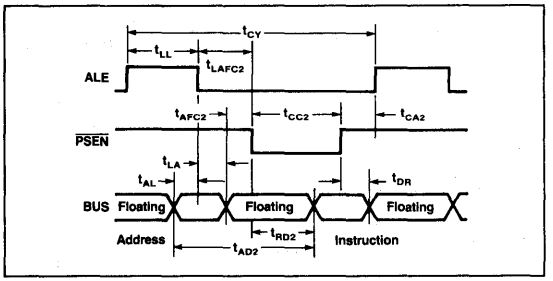
(5) At execution of MOVD Pp, A; ANLD Pp, A; ORLD Pp, A instructions

AC Timing Test Points (Except RESET, XTAL1, XTAL2, SS)

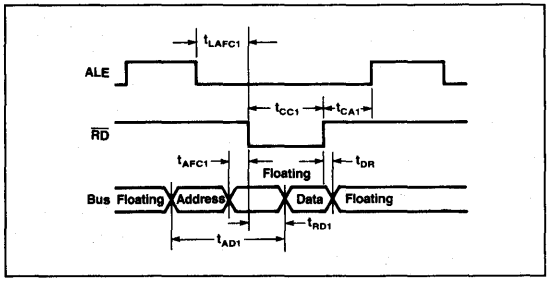


Timing Waveforms

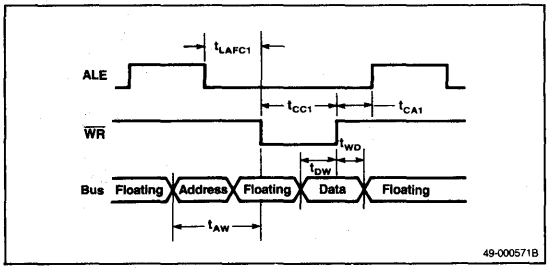
Instruction Fetch (External Program Memory)



Read (External Data Memory)

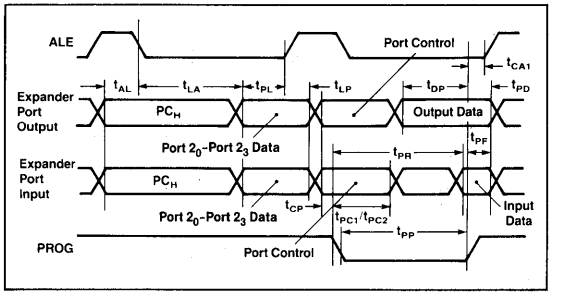


Write (External Data Memory)

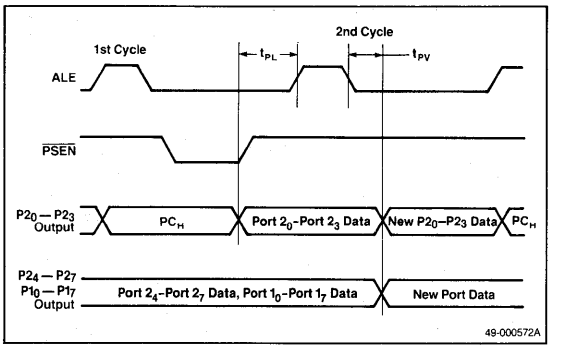


Timing Waveforms (cont)

Port 2 Expansion Timing



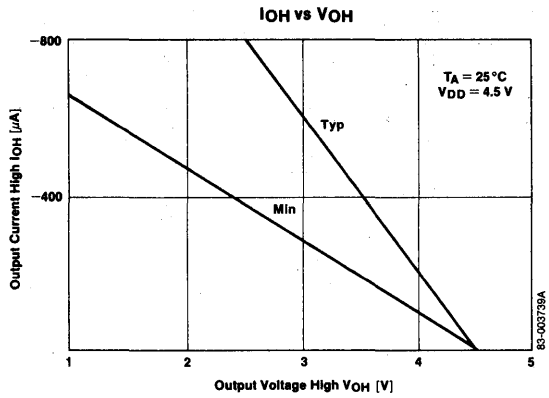
I/O Port Timing

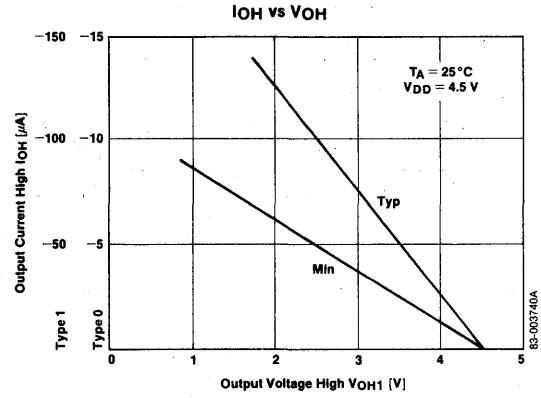


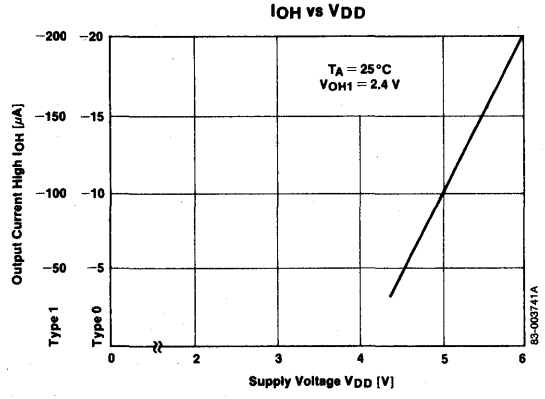
Bus Timing Requirements

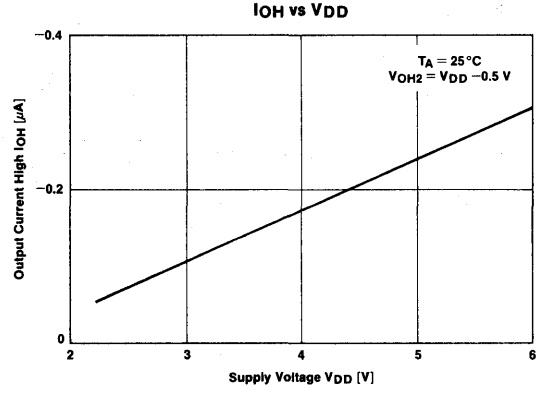
Symbol	Timing Formula	Min/Max	Unit
t_{LL}	$(7/30)\,t_{CY}-170$	Min	ns
t_{AL}	$(1/5)\,t_{CY}-110$	Min	ns
t_{LA}	$(1/15)\,t_{CY}-40$	Min	ns
t_{CC1}	$(1/2)\,t_{CY}-200$	Min	ns
t_{CC2}	$(2/5)\,t_{CY}-200$	Min	ns
t_{DW}	$(13/30)\,t_{CY}-200$	Min	ns
t_{WD}	$(1/15)\,t_{CY}-40$	Min	ns
t_{DR}	$(1/10)\,t_{CY}-30$	Max	ns
t_{RD1}	$(2/5)\,t_{CY}-200$	Max	ns
t_{RD2}	$(3/10)\,t_{CY}-200$	Max	ns
t_{AW}	$(2/5)\,t_{CY}-150$	Min	ns
t_{AD1}	$(23/30)\,t_{CY}-250$	Max	ns
t_{AD2}	$(3/5)\,t_{CY}-250$	Max	ns
t_{AFC1}	$(2/15)\,t_{CY}-65$	Min	ns
t_{AFC2}	$(1/30)\,t_{CY}-40$	Min	ns
t_{LAFC1}	$(1/5)\,t_{CY}-75$	Min	ns
t_{LAFC2}	$(1/10)\,t_{CY}-75$	Min	ns
t_{CA1}	$(1/15)\,t_{CY}-50$	Min	ns
t_{CA2}	$(4/15)\,t_{CY}-50$	Min	ns
t_{CP}	$(1/10)\,t_{CY}-40$	Min	ns
t_{PC2}	$(4/15)\,t_{CY}-200$	Min	ns
t_{PR}	$(17/30)\,t_{CY}-120$	Max	ns
t_{PF}	$(1/10)\,t_{CY}$	Max	ns
t_{DP}	$(2/5)\,t_{CY}-150$	Min	ns
t_{PD}	$(1/10)\,t_{CY}-50$	Min	ns
t_{PP}	$(7/10)\,t_{CY}-250$	Min	ns
t_{PL}	$(4/15)\,t_{CY}-200$	Min	ns
t_{LP}	$(1/30)\,t_{CY}-40$	Min	ns
t_{PV}	$(3/10)\,t_{CY}+100$	Max	ns
t_{OPRR}	$(1/5)\,t_{CY}$	Min	ns
t_{CY}	$(1/f_{XTAL})\times 15$		μs

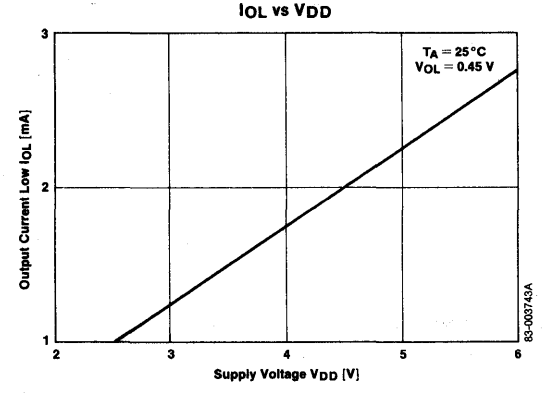
Operating Characteristics

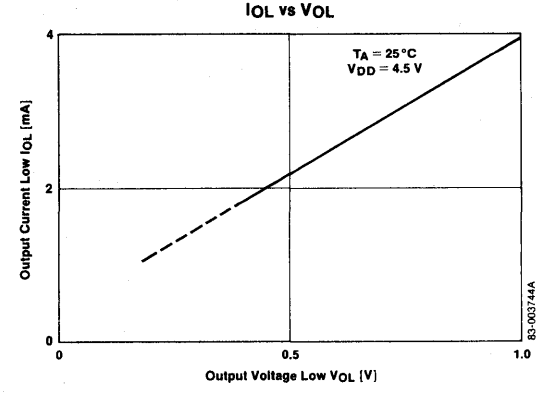






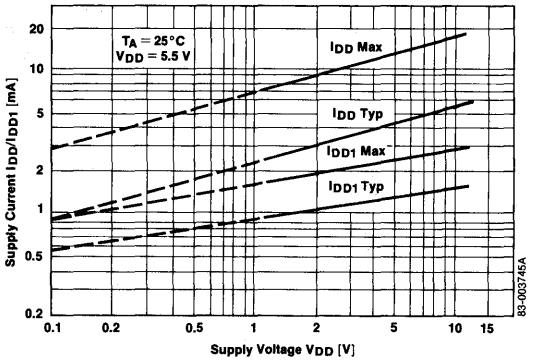






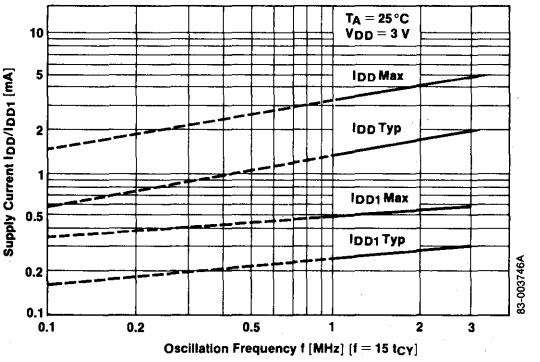
Operating Characteristics (cont)

I_{DD}/I_{DD1} vs f



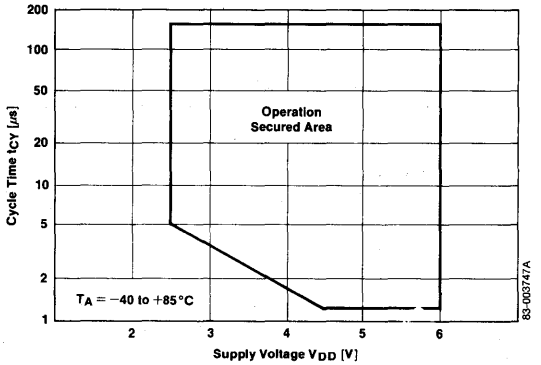
Curves below 1 MHz show characteristics for external oscillation

I_{DD}/I_{DD1} vs f

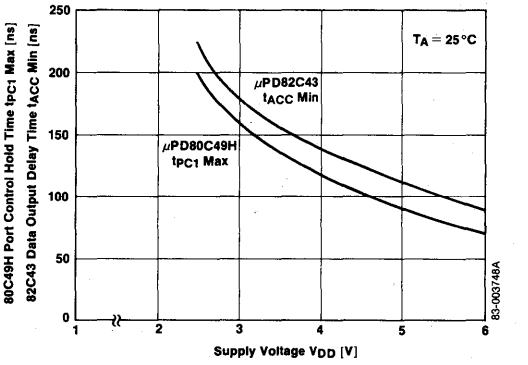


Curves below 1 MHz show characteristics for external oscillation.

t_{CY} vs V_{DD}



t_{PC1} Max [80C49H] and t_{ACC} Min [82C43] vs V_{DD}



Note: Curves without "operation secured area" show reference data.

4

Functional Description

The μPD80C39H/μPD80C49H has the following functional blocks:

Instruction Decoder

The instruction decoder stores the operation code of each instruction and converts it into outputs that control the functions of each block. These outputs control the functions executed by the ALU, data source, and specified registers.

Arithmetic Logic Unit (ALU)

The ALU receives 8-bit data from the accumulator or temporary register and computes an 8-bit result under control of the instruction decoder.

The ALU executes the following functions:
- Add with carry or add without carry
- Logical AND, OR, XOR
- Increment and decrement
- Bit complement
- Rotate left and right
- Swap nibbles
- BCD decimal correction

When a carry results from ALU overflows, the carry bit of the program word is set.

Accumulator

The accumulator is an 8-bit register that stores ALU input data and arithmetic results. It can also be used for transferring data between I/O ports and memory.

Temporary Register

The temporary register is an 8-bit register used for the internal processing necessary with arithmetic operations. The contents of the temporary register are input to the ALU.

Program Counter

The program counter is a 12-bit register that addresses on-chip program memory. The program counter specifies the address of the next instruction to be executed.

Program Memory

The μPD80C49H contains a mask-programmable ROM of 2048 × 8 bits that can be addressed by a program counter. The μPD80C39H has no internal ROM, so it uses external program memory. You can expand internal program memory to 4096 bytes by connecting external program memory. When the contents of the program counter exceed the built-in ROM area, the external program memory will be automatically accessed by DB_0-DB_7, $P2_0$-$P2_3$, and $\overline{PSEN}$.

Data Memory

The μPD80C39H/μPD80C49H has 128 words × 8 bits of data memory that can be externally expanded 256 words maximum when needed.

RAM Address Register

The RAM address register specifies the next address to be accessed in data memory.

Program Status Word

The PSW (figure 1) is an 8-bit status word containing the information shown in table 1.

Figure 1. Program Status Word

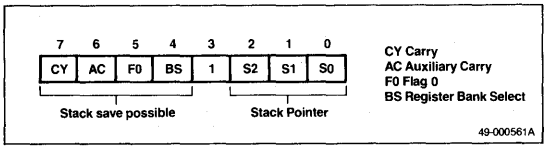


Table 1. PSW Bit Functions

Bits 0-2	Stack pointer bits (S0-S2) A $\overline{RESET}$ clears the stack pointer to 0.
Bit 3	Not used (1).
Bit 4	Working register bank switch bit (BS) 0 = Bank 0 1 = Bank 1
Bit 5	Flag bit (F0). User-controlled bit that can be complemented, cleared, or tested by conditional jump instruction JF0.
Bit 6	Auxiliary Carry (AC) Generated by an auxiliary carry, ADD instruction. Can by used by decimal adjust instruction DA A.
Bit 7	Carry flag (CY) Indicates that an accumulator overflow has taken place with the previously executed instruction.

Conditional Branch Logic

The conditional branch logic is used to test processor conditions. Use a conditional jump instruction to test the conditions shown in table 2.

Control Logic

The control logic generates or receives the signals that control various functions including memory reads and writes, interrupts, software STOP mode, resets, and external memory fetches.

Table 2. Branching Conditions

Test Device	Conditional Jump	
Accumulator	All 0	Not all 0
Accumulator bit	—	1
Carry flag	0	1
User flags (F0, F1)	—	1
Timer overflow flag	—	1
Test inputs (T0, T1)	0	1
Interrupt input (INT)	0	—

Reset Functions

A reset performs the following functions:

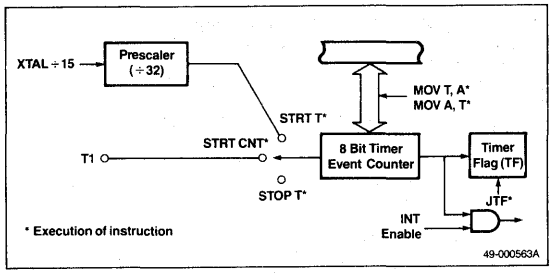
- Clears the program counter and the stack pointer to 0
- Selects register bank and memory bank 0
- Sets the data bus in a high impedance state (except when EA is high)
- Sets ports 1, 2 in input mode
- Disables interrupts (timer and external)
- Stops the timer
- Clears the timer flag, F0, and F1
- Disables the clock output from T0
- Releases HALT and STOP modes

Timer/Event Counter

The timer/event counter can count external events in order to generate a precise time delay. The counter operation is the same in both modes, the only difference is the input source.

The counter is an 8-bit binary up counter (figure 2) that can be reset. It is possible to transfer the contents of the timer to the accumulator and vice-versa by using the MOV A, T and MOV T, A instructions, respectively. The contents of the counter can be independently initialized by the MOV T, A instruction. Use the STRT T instruction to use the counter as a timer and the STRT CNT instruction to use the counter as an event counter.

Figure 2. Timer/Event Counter



Once the counter starts, it continues counting until the program executes a STOP TCNT instruction or $\overline{\text{RESET}}$ becomes active. The counter is incremented up to the maximum count (FFH) and overflows when the count goes from FFH to 00H.

Event Counter. When the T1 pin and counter input are connected by the execution of a STRT CNT instruction, the counter starts counting as an event counter. A change in T1 from high to low causes a count signal which increments the counter by +1. The maximum speed of a count increment is one count per 3 machine cycles. When a 12 MHz crystal is used, the maximum speed is 1 count per 3.75 μs. There is no mimimum speed. After a count signal the T1 input must be held low at least 250 ns (at 12 MHz).

Timer. When an internal clock is connected with the counter input by the execution of the STRT T instruction, the counter starts counting as a timer. When used as a machine cycle clock, ALE is passed through a prescaler which generates an internal clock that increments the timer every 32 machine cycles. The prescaler is reset during the execution of a STRT T instruction. With a 12 MHz crystal, the counter is incremented by +1 at each 25 kHz clock every 40 μs.

You can obtain a delay from 40 μs to 10 ms (256 counts) by presetting the counter and detecting the overflow. To obtain time, through software control, in excess of 10 ms, count overflows in a separate register. To count in steps of 40 μs or less, an external clock can be supplied to the T1 input which causes the counter to operate in the event counter mode. Use the ALE frequency divided by 3 or more for the external clock. Use a software delay loop for fine adjustment of an extremely small or large delay.

Ports 1 and 2 Latch and Buffer

Ports 1 and 2 are 8-bit input/output ports. The data written to the port by an output instruction is latched and output and the data is maintained unless a new output instruction is executed. Input data is not latched, so it is necessary to stabilize input data when reading data by an input instruction.

Several port-loading options are available. At the time you order a mask ROM, (μPD80C49H), you can designate the pullup resistors for port lines $P1_0$-$P1_7$, $P2_0$-$P2_3$, and $P2_4$-$P2_7$.

Three types of pullup resistors are available:

Type 0	($I_{OH} = -5\,\mu A$: $V_{DD} = +5\,V\ +10\%$)
Type 1	($I_{OH} = -50\,\mu A$: $V_{DD} = +5\,V\ +10\%$)
Type 2	No pullup resistor

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Only type 0 pullup resistors are available with the μPD80C39H.

Timing Logic

The oscillator generates a clock signal that controls all system timing operations. Oscillation is generated by either an external self-oscillating element or external clock input. The oscillator acts as an internal high-gain amplifier for serial resonance. To obtain the oscillation frequency, an external LC network or a crystal or ceramic external resonator may be connected.

As the crystal frequency is lowered, there is an equivalent reduction in series resistance (R). As the temperature of the crystal is lowered, R is increased. Due to this relationship, it becomes difficult to stabilize oscillation where there is low power supply voltage. When V_{CC} is less than 2.7 V and the oscillator frequency is 3 MHz or less, T_A (ambient temperature) should not be less than −10°C.

Standby Control

The standby control circuitry allows low power consumption operation. The standby function operates in 2 modes: HALT and STOP.

HALT Mode

In HALT mode, the oscillation circuit continues to operate but the internal clock stops. The CPU holds all the status of the internal circuits just prior to execution of the HALT instruction. In HALT mode, power consumption is much less than normal.

Setting HALT Mode. HALT mode is set by execution of the HALT instruction and released by either $\overline{INT}$ or $\overline{RESET}$. If interrupts are disabled and $\overline{INT}$ becomes low at a machine cycle right before the HALT instruction and remains low during 2 machine cycles, the HALT instruction byte will be fetched and decoded, but the HALT mode will not be set. Program operation resumes from the instruction following the HALT instruction.

If interrupts are enabled under the same conditions as above, the HALT instruction byte will be fetched and decoded but the HALT mode will not be set and the program will jump to the interrupt start address. After returning from the interrupt routine, the program will continue from the instruction following the HALT instruction.

Releasing HALT Mode. Release HALT mode by activating $\overline{INT}$ or $\overline{RESET}$. When using $\overline{INT}$ to release HALT mode, a low level is present at the $\overline{INT}$ pin and the internal clock is restarted. If interrupts are enabled, the interrupt is executed after the first instruction following the HALT instruction.

In the interrupt enable state, hold the $\overline{INT}$ pin low until the interrupt procedure is started to ensure the interrupt.

When using $\overline{RESET}$ to release HALT mode, a low level is present at the $\overline{RESET}$ pin and the HALT mode is reset and a normal reset operation is executed. When $\overline{RESET}$ goes to a high level, the program starts from address 0.

STOP Mode

In STOP mode, the oscillator stops and only the contents of RAM are maintained. Power consumption is lower than that of the HALT mode. You can set the STOP mode with hardware, by controlling the $\overline{RESET}$ and $\overline{STOP}$ pins; and by software, by executing the corresponding instruction.

Hardware STOP Mode

In hardware STOP mode, the contents of RAM can be held at a voltage as low as +2.0 V.

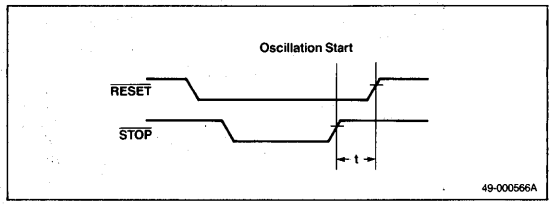
To set hardware STOP mode, set the $\overline{RESET}$ pin to a low level to protect the contents of RAM. Set the $\overline{STOP}$ pin to a low level to stop operation of the oscillation circuit.

To release hardware STOP mode, apply the normal operating level (+2.5 V to +6.0 V) to the power supply at the V_{DD} pin. As figure 3 shows, set the $\overline{STOP}$ pin to a high level while holding the $\overline{RESET}$ pin at a low level. This will restart the oscillation circuit. When $\overline{RESET}$ is set high after oscillation circuit operation is stabilized, the program is started from address 000H. Because the $\overline{STOP}$ pin controls oscillator operation, be careful to protect the $\overline{STOP}$ pin from noise.

When power is turned on, or when STOP mode is released, the oscillation circuit restarts. Because the crystal or ceramic resonator utilizes mechanical vibration, a certain time is required for the oscillation to stabilize. The "t" represents the oscillation stabilizing wait time in the timing waveform.

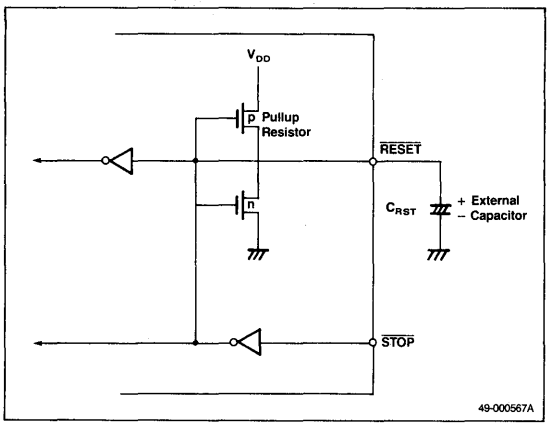
During this wait time, it is necessary to stop instruction execution in order to prevent CPU errors, Therefore, "t" must be longer than the oscillator's stabilizing time.

Figure 3. Oscillator Stop and Start



Oscillation stabilizing time differs somewhat by the type of oscillator used. With a 6 MHz oscillation frequency, a crystal resonator needs several milliseconds to stabilize, while a ceramic resonator needs several hundred microseconds. Figure 4 shows how to easily control the hardware STOP mode by externally connecting a capacitor to the RESET pin. This allows control of the oscillation stabilizing time.

Figure 4. Hardware STOP Mode Control Circuit



Software STOP Mode

In software STOP mode, the oscillation circuits stop, but the CPU maintains all status of internal circuits and data existing just before the STOP instruction. Software STOP mode is the same as when the oscillation circuit stops in HALT mode.

In software STOP mode, if a capacitor (C_{SS}) is connected to the SS pin as shown in figure 5, you can obtain the oscillation stabilizing wait time when releasing STOP mode.

Setting Software STOP Mode. To set software STOP mode, execute the STOP instruction. This sets the internal software STOP mode flip-flop which stops the oscillator and turns transistors A and B off and on, respectively. Capacitor C_{SS} discharges through transistor B causing the SS pin to go low.

Releasing Software STOP Mode. To release software STOP mode, apply an INT or RESET input.

When using the INT input (figure 6), a low at the INT pin resets the software STOP flip-flop and turns transistors A and B on and off, respectively. Then the oscillator restarts, but since SS is still low, program execution remains stopped. With transistor A on, C_{SS} charges and causes SS to go to a high level. Then, program execution restarts. The time it takes for SS to reach the threshold of a logic 1 determines the oscillation stabilizing wait time.

After software STOP mode is released, if interrupts are disabled as in the HALT mode, program execution is resumed from the instruction following the STOP instruction. If interrupts are enabled, the interrupt procedure is initiated (address 003H) after the execution of 1 instruction following the STOP instruction. To assure the interrupt, hold INT at a low level until the interrupt procedure is initiated. Even with short low level timing, the interrupt procedure will be assured if you place a 1-machine cycle instruction after the STOP instruction. However, it is recommended that you hold INT low for at least 2 machine cycles.

When using the RESET input, a low level at the RESET pin resets the software STOP flip-flop. The oscillator starts and the SS pin goes to a high level as C_{SS} is charged. The program starts from address 000H when RESET goes high. Also, since the oscillation stabilizing wait time is generated when SS is low, the RESET pin should be held low longer than the SS pin. When the oscillation stabilizing wait time is obtained by the externally connected capacitor, the value of the capacitor (C_{RST}) connected to the RESET pin (figure 4) should be set at least 3 times larger than that of capacitor C_{SS} connected to the SS pin. For example, if C_{SS} is set to 0.33 μF, C_{RST} should be 1 μF.

When no capacitor is connected to the SS pin, the low level time of the RESET pin should be set to a value larger than the oscillation stabilizing time and SS should be open or pulled up with a 1 k or more resistor.

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Figure 5. Software STOP Mode Control Circuit

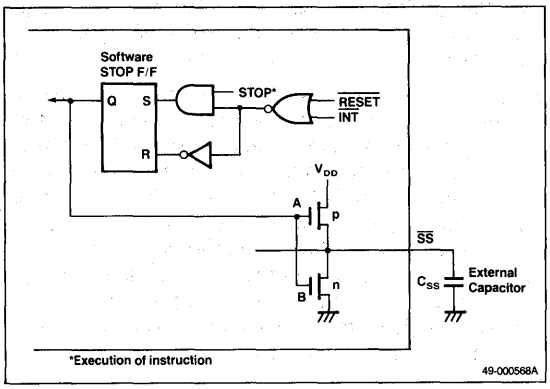
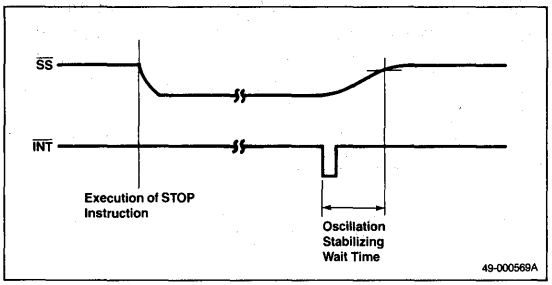


Figure 6. Software STOP Mode Timing



Instruction Set

Mnemonic	Operation	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Accumulator													
ADD A, # data	(A) ← (A) + data	Add immediate the specified data to the accumulator.(2)	03	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, Rr	(A) ← (A) + (Rr) for r = 0–7	Add contents of designated register to the accumulator.(2)	6n(4)	0	1	1	0	1	r	r	r	1	1
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0–1	Add indirect the contents the data memory location to the accumulator.(2)	6n(4)	0	1	1	0	0	0	0	r	1	1
ADDC A, # data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the accumulator.(2)	13	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0–7	Add with carry the contents of the designated register to the accumulator.(2)	7n(4)	0	1	1	1	1	r	r	r	1	1
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0–1	Add indirect with carry the contents of data memory location to the accumulator.(2)	7n(4)	0	1	1	1	0	0	0	r	1	1
ANL A, # data	(A) ← (A) AND data	Logical AND specified immediate data with accumulator.	53	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0–7	Logical AND contents of designated register with accumulator.	5n(4)	0	1	0	1	1	r	r	r	1	1
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0–1	Logical AND indirect the contents of data memory with accumulator.	5n(4)	0	1	0	1	0	0	0	r	1	1
CPL A	(A) ← NOT (A)	Complement the contents of the accumulator.	37	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clear the contents of the accumulator.	27	0	0	1	0	0	1	1	1	1	1
DA A		Decimal adjust the contents of the accumulator.(2)	57	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) – 1	Decrement by 1 the accumulator's contents.	07	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	17	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with accumulator.	43	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0–7	Logical OR contents of designated register with accumulator.	4n(4)	0	1	0	0	1	r	r	r	1	1
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0–1	Logical OR indirect the contents of data memory location with accumulator.	4n(4)	0	1	0	0	0	0	0	r	1	1
RL A	$(A_{N+1}) \leftarrow (A_N)$ $(A_0) \leftarrow (A_7)$ for N = 0–6	Rotate accumulator left by 1 bit without carry.	E7	1	1	1	0	0	1	1	1	1	1
RLC A	$(A_{N+1}) \leftarrow (A_N)$; N = 0–6 $(A_0) \leftarrow (C)$ $(C) \leftarrow (A_7)$	Rotate accumulator left by 1 bit through carry.	F7	1	1	1	1	0	1	1	1	1	1
RR A	$(A_N) \leftarrow (A_{N+1})$; N = 0–6 $(A_7) \leftarrow (A_0)$	Rotate accumulator right by 1 bit without carry.	77	0	1	1	1	0	1	1	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Accumulator (cont)													
RRC A	$(A_N) \leftarrow (A_{N+1})$; N = 0–6 $(A_7) \leftarrow (C)$ $(C) \leftarrow (A_0)$	Rotate accumulator right by 1 bit through carry.	67	0	1	1	0	0	1	1	1	1	1
SWAP A	$(A_4\text{–}A_7) \longleftrightarrow (A_0\text{–}A_3)$	Swap the 2 4-bit nibbles in the accumulator.	47	0	1	0	0	0	1	1	1	1	1
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with accumulator.	D3	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0–7	Logical XOR contents of designated register with accumulator.	Dn(4)	1	1	0	1	1	r	r	r	1	1
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0–1	Logical XOR indirect the contents of data memory location with accumulator.	Dn(4)	1	1	0	1	0	0	0	r	1	1
Branch													
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0–7 If (Rr) ≠ 0; $(PC_0\text{–}PC_7) \leftarrow$ addr	Decrement the specified register and test contents.	En	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2
JBb addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if accumulator bit is set.	x2(6)	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2
JC addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	F6	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if flag F0 is set.	B6	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if flag F1 is set.	76	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_8\text{–}PC_{10}) \leftarrow (addr_8\text{–}addr_{10})$ $(PC_0\text{–}PC_7) \leftarrow (addr_0\text{–}addr_7)$ $(PC_{11}) \leftarrow$ DBF	Direct jump to specified address within the 2K address block.	x4(6)	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP @ A	$(PC_0\text{–}PC_7) \leftarrow ((A))$	Jump indirect to specified address with address page.	B3	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	E6	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNI addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	86	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if test 0 is low.	26	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if test 1 is low.	46	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	96	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2

NEC

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Branch (cont)													
JTF addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if TF = 1 $(PC) \leftarrow (PC) + 2$ if TF = 0	Jump to specified address if timer flag is set to 1.	16	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jump to specified address if test 0 is a 1.	36	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jump to specified address if test 1 is a 1.	56	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ addr	$(PC_0\text{-}PC_7) \leftarrow$ addr if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jump to specified address if accumulator is 0.	C6	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
Control													
EN I		Enable the external interrput input.	05	0	0	0	0	0	1	0	1	1	1
DIS I		Disable the external interrupt input.	15	0	0	0	1	0	1	0	1	1	1
ENT0 CLK		Enable the clock output pin T0.	75	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF) $\leftarrow$ 0	Select bank 0 (locations 0–2047) of program memory.	E5	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF) $\leftarrow$ 1	Select bank 1 (locations 2048–4095) of program memory.	F5	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS) $\leftarrow$ 0	Select bank 0 (locations 0–7) of data memory.	C5	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS) $\leftarrow$ 1	Select bank 1 (locations 24–31) of data memory.	D5	1	1	0	1	0	1	0	1	1	1
HALT		Initiates halt mode.	01	0	0	0	0	0	0	0	1	1	1
STOP		Sets CPU to software stop mode.	82	1	0	0	0	0	0	1	0	1	1
Data Moves													
MOV A, # data	(A) $\leftarrow$ data	Move immediate the specified data into the accumulator.	23	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, Rr	(A) $\leftarrow$ (Rr); r = 0–7	Move the contents of the designated registers into the accumulator.	Fn(4)	1	1	1	1	1	r	r	r	1	1
MOV A, @ Rr	(A) $\leftarrow$ ((Rr)); r = 0–1	Move indirect the contents of data memory location into the accumulator.	Fn(4)	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) $\leftarrow$ (PSW)	Move contents of the program status word into the accumulator.	C7	1	1	0	0	0	1	1	1	1	1
MOV Rr, # data	(Rr) $\leftarrow$ data; r = 0–7	Move immediate the specified data into the designated register.	Bn(4)	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2
MOV Rr, A	(Rr) $\leftarrow$ (A); r = 0–7	Move accumulator contents into the designated register.	An(4)	1	0	1	0	1	r	r	r	1	1
MOV @ Rr, A	((Rr)) $\leftarrow$ (A); r = 0–1	Move indirect accumulator contents into data memory location.	An(4)	1	0	1	0	0	0	0	r	1	1
MOV @ Rr, # data	((Rr)) $\leftarrow$ data; r = 0–1	Move immediate the specified data into data memory.	Bn(4)	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2
MOV PSW, A	(PSW) $\leftarrow$ (A)	Move contents of accumulator into the program status word.	D7	1	1	0	1	0	1	1	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Data Moves (cont)													
MOVP A, @ A	$(PC_0–PC_7) \leftarrow (A)$ $(A) \leftarrow ((PC))$	Move data in the current page into the accumulator.	A3	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	$(PC_0–PC_7) \leftarrow (A)$ $(PC_8–PC_{11}) \leftarrow 0011$ $(A) \leftarrow ((PC))$	Move program data in page 3 into the accumulator.	E3	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	$(A) \leftarrow ((Rr))$; r = 0–1	Move indirect the contents of external data memory into the accumulator.	8n(4)	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	$((Rr)) \leftarrow (A)$; r = 0–1	Move indirect the contents of the accumulator into external data memory.	9n(4)	1	0	0	1	0	0	0	r	2	1
XCH A, Rr	$(A) \longleftrightarrow (Rr)$; r = 0–7	Exchange the accumulator and designated register's contents.	2n(4)	0	0	1	0	1	r	r	r	1	1
XCH A, @ Rr	$(A) \longleftrightarrow ((Rr))$; r = 0–1	Exchange indirect contents of accumulator and location in data memory.	2n(4)	0	0	1	0	0	0	0	r	1	1
XCHD A, @ Rr	$(A_0–A_3) \longleftrightarrow ((Rr))_0–((Rr))_3$; r = 0–1	Exchange indirect 4-bit contents of accumulator and data memory.	3n(4)	0	0	1	1	0	0	0	r	1	1
Flags													
CPL C	$(C) \leftarrow$ NOT (C)	Complement contents of carry bit.	A7	1	0	1	0	0	1	1	1	1	1
CPL F0	$(F0) \leftarrow$ NOT (F0)	Complement contents of flag F0.	95	1	0	0	1	0	1	0	1	1	1
CPL F1	$(F1) \leftarrow$ NOT (F1)	Complement contents of flag F1.	B5	1	0	1	1	0	1	0	1	1	1
CLR C	$(C) \leftarrow 0$	Clear contents of carry bit to 0.	97	1	0	0	1	0	1	1	1	1	1
CLR F0	$(F0) \leftarrow 0$	Clear contents of flag 0 to 0.	85	1	0	0	0	0	1	0	1	1	1
CLR F1	$(F1) \leftarrow 0$	Clear contents of flag 1 to 0.	A5	1	0	1	0	0	1	0	1	1	1
Input / Output													
ANL BUS, # data	(bus) ← (bus) AND data	Logical AND immediate specified data with contents of bus.	98	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1–2	Logical AND immediate specified data with designated port (1 or 2).	9n(5)	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
ANLD Pp, A	(Pp) ← (Pp) AND $(A_0–A_3)$; p = 4–7	Logical AND contents of accumulator with designated port (4–7).	9n(5)	1	0	0	1	1	1	p	p	2	1
IN A, Pp	$(A) \leftarrow (Pp)$; p = 1–2	Input data from designated port (1–2) into accumulator.	0n(5)	0	0	0	0	1	0	p	p	2	1
INS A, BUS	$(A) \leftarrow$ (bus)	Input strobed bus data into accumulator.	08	0	0	0	0	1	0	0	0	2	1
MOVD A, Pp	$(A_0–A_3) \leftarrow (Pp)$; p = 4–7 $(A_4–A_7) \leftarrow 0$	Move contents of designated port (4–7) into accumulator.	0n(5)	0	0	0	0	1	1	p	p	2	1

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Input / Output (cont)													
MOVD Pp, A	(Pp) ← (A_0–A_3); p = 4–7	Move contents of accumulator to designated port (4–7).	3n(5)	0	0	1	1	1	1	p	p	2	1
ORL BUS, # data	(bus) ← (bus) OR data	Logical OR immediate specified data with contents of bus.	88	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ORLD Pp, A	(Pp) ← (Pp) OR (A_0–A_3); p = 4–7	Logical OR contents of accumulator with designated port (4–7).	8n(5)	1	0	0	0	1	1	p	p	2	1
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1–2	Logical OR immediate specified data with designated port (1–2).	9n(5)	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
OUTL BUS, A	(bus) ← (A)	Output contents of accumulator onto bus.	02	0	0	0	0	0	0	1	0	2	1
OUTL Pp,A	(Pp) ← (A); p = 1–2	Output contents of accumulator to designated port (1–2).	3n(5)	0	0	1	1	1	0	p	p	2	1
Registers													
DEC Rr	(Rr) ← (Rr) – 1; r = 0–7	Decrement by 1 contents of designated register.	Cn(4)	1	1	0	0	1	r	r	r	1	1
INC Rr	(Rr) ← (Rr) + 1; r = 0–7	Increment by 1 contents of designated register.	1n(4)	0	0	0	1	1	r	r	r	1	1
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0–1	Increment indirect by 1 the contents of data memory location.	1n(4)	0	0	0	1	0	0	0	r	1	1
Subroutine													
CALL addr	((SP)) ← (PC), (PSW_4–PSW_7) (SP) ← (SP) + 1 (PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Call designated subroutine.	x4(6)	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from subroutine without restoring program status word.	83	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW_4–PSW_7) ← ((SP))	Return from subroutine restoring program status word.	93	1	0	0	1	0	0	1	1	2	1
Timer / Counter													
EN TCNTI		Enable internal interrupt flag for timer / counter output.	25	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disable internal interrupt flag for timer / counter output.	35	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Move contents of timer / counter into accumulator.	42	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Move contents of accumulator into timer / counter.	62	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stop count for event counter.	65	0	1	1	0	0	1	0	1	1	1
STRT CNT		Start count for event counter.	45	0	1	0	0	0	1	0	1	1	1
STRT T		Start count for timer.	55	0	1	0	1	0	1	0	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Miscellaneous													
NOP		No operation performed.	00	0	0	0	0	0	0	0	0	1	1

Note:

(1) Binary instruction code designations r and p represent encoded values or the lowest-order bit value of specified registers and ports, respectively.

(2) Execution of the ADD, ADDC, and DA instructions affect the carry flags, which are not shown in the respective function equations. These instructions set the carry flags when there is an overflow in the accumulator (the auxiliary carry flag is set when there is an overflow of bit 3 of the accumulator) and clear the carry flags when there is no overflow. Flags that are specifically addressed by flag instructions are shown in the function equations for those instructions.

(3) References to addresses and data are specified in byte 1 and/or 2 in the opcode of the corresponding instruction.

(4) The hex value of n for specific registers is as follows:
a) Direct addressing
R0: n = 8 R2: n = A R4: n = C R6: n = E
R1: n = 9 R3: n = B R5: n = D R7: n = F
b) Indirect addressing
@ R0: n = 0 @ R1: n = 1

(5) The hex value of n for specific ports is as follows:
P1: n = 9 P4: n = C P6: n = E
P2: n = A P5: n = D P7: n = E

(6) The hex value of x for specific accumulator or address bits is as follows:
a) JBb instruction
B_0: x = 1 B_2: x = 5 B_4: x = 9 B_6: x = D
B_1: x = 3 B_3: x = 7 B_5: x = B B_7: x = F
b) JMP instruction
Page 0: x = 0 Page 2: x = 4 Page 4: x = 8 Page 6: x = C
Page 1: x = 2 Page 3: x = 6 Page 5: x = A Page 7: x = E
c) CALL instruction
Page 0: x = 1 Page 2: x = 5 Page 4: x = 9 Page 6: x = D
Page 1: x = 3 Page 3: x = 7 Page 5: x = B Page 7: x = F

Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program memory address (a_0–a_7) or (a_0–a_{10})
b	Accumulator bit (b = 0–7)
BS	Bank switch
BUS	Bus port
C	Carry flag
CLK	Clock signal
CNT	Event counter
data	Number or expression (8 bits)
DBF	Memory bank flip-flop
F0, F1	Flags 0, 1
$\overline{INT}$	Interrupt
n	Indicates the hex number of the specified register or port
PC	Program counter
Pp	Port designator (p = 1, 2 or 4–7)
PSW	Program status word
Rr	Register designator (r = 0–7)

Symbol	Description
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Testable flags 0, 1
#	Prefix for immediate data
@	Prefix for indirect address
x	Indicates the hex number corresponding to the accumulator bit or page number specified in the operand
(x)	Contents of external RAM location
((x))	Contents of memory location addressed by the contents of external RAM location
←	Replaced by
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
XOR	Exclusive-OR
———	Complement

4

μPD80C40H/50H, μPD50H
HIGH-SPEED, 8-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

Description

The μPD80C40H, μPD80C50H, and μPD50H are single-chip, CMOS 8-bit microcomputers containing an 8-bit CPU, ROM (μPD80C50H only), RAM, I/O ports, and control circuitry. Through CMOS technology, the devices can retain data with low power consumption. In addition, the processor uses two standby modes (HALT and STOP) to further minimize power drain.

Features

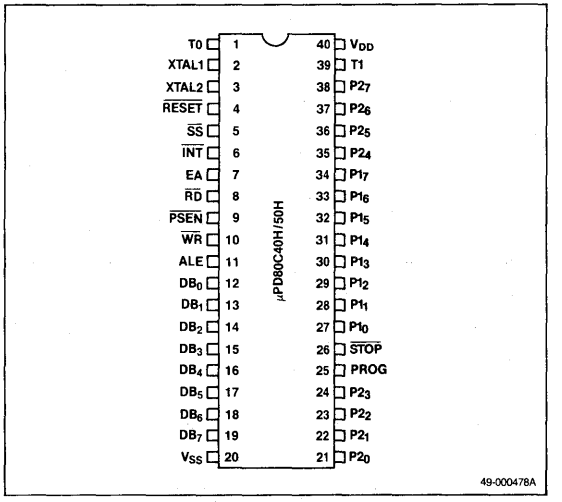
- ☐ 98 instructions
- ☐ 1.25 μs instruction cycle time (12 MHz crystal)
- ☐ Addition, logic, and decimal adjust functions
- ☐ 2K × 8-bit ROM (μPD80C50H)
- ☐ 256 × 8-bit RAM
- ☐ Standby function
- ☐ 8-level stack
- ☐ Two sets of working registers
- ☐ Interrupt capability
- ☐ Two test inputs
- ☐ Internal timer/event counter
- ☐ Input/output ports (8 bits × 2)
  - — Data bus alternative to I/O ports (8 bits × 1)
- ☐ Expandable memory and I/O ports
- ☐ Single-step function
- ☐ Internal clock generator
- ☐ CMOS technology
- ☐ Single power supply of +2.5 V to +6.0 V
- ☐ Intel 8050H, 8040H pin compatible

Ordering Information

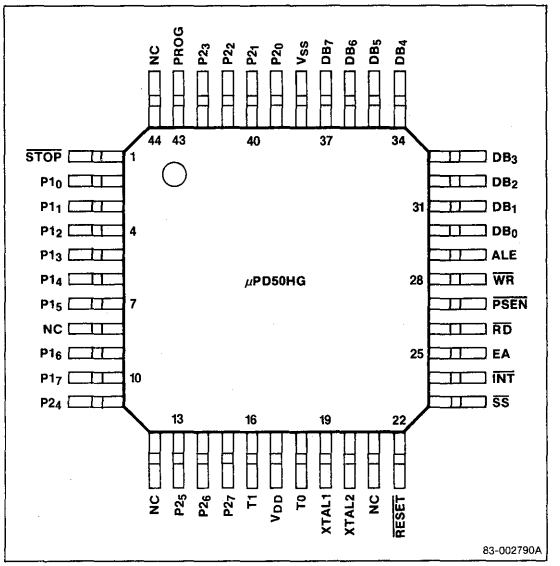
Part Number	Package Type	Max Frequency of Operation	ROM
μPD80C40HC	40-pin plastic DIP	12 MHz	None
μPD80C50HC	40-pin plastic DIP	12 MHz	2K x 8 bits
μPD50HG-22	44-pin plastic miniflat	12 MHz	2K x 8 bits

Pin Configurations

40-Pin Plastic DIP



44-Pin Plastic Miniflat



Pin Identification

Symbol	Function
T0	Test 0 input / clock output
XTAL1	Crystal 1 input
XTAL2	Crystal 2 input
$\overline{RESET}$	Reset input
$\overline{SS}$	Single step input
$\overline{INT}$	Interrupt input
EA	External access input
$\overline{RD}$	Read output
$\overline{PSEN}$	Program store enable output
$\overline{WR}$	Write output
ALE	Address latch enable output
DB_0–DB_7	Bidirectional data bus
V_{SS}	Ground
$P2_0$–$P2_7$	Quasi-bidirectional port 2
PROG	Program output
$\overline{STOP}$	Stop input
$P1_0$–$P1_7$	Quasi-bidirectional port 1
T1	Test 1 input
V_{DD}	Power supply

Pin Functions

XTAL1, XTAL2 (Crystals 1, 2)

XTAL1 and XTAL2 are the crystal inputs for the internal clock oscillator. XTAL1 is also used as an input for external clock signals.

T0 (Test 0)

The JT0 and JNT0 instructions test the level of T0 and, as a result, the program address jumps to the specified address. T0 becomes a clock output when the ENT0 CLK instruction is executed.

T1 (Test 1)

The JT1 and JNT1 instructions test the level of T1 and, as a result, the program address jumps to the specified address. T1 becomes an internal counter input when the STRT CNT instruction is executed.

$\overline{RESET}$ (Reset)

$\overline{RESET}$ initializes the processor and is also used to verify the internal ROM. $\overline{RESET}$ determines the oscillation stabilizing time during the release of STOP mode. The $\overline{RESET}$ pulse width requires at least 5 machine cycles when the supply voltage is within specifications and the oscillation frequency is stable. (Active low).

$\overline{SS}$ (Single Step)

SS causes the processor to execute the program one step at a time. $\overline{SS}$ also determines the oscillation stabilizing time during the release of the software STOP mode.

$\overline{INT}$ (Interrupt)

$\overline{INT}$ starts an interrupt if interrupts are enabled. A reset disables an interrupt. $\overline{INT}$ can be tested with the JNI instruction and, depending on the results, a jump to the specified address can occur.

EA (External Access)

EA disables internal program memory and fetches and accesses external program memory. EA is used for system testing and debugging. (Active high).

$\overline{RD}$ (Read)

$\overline{RD}$ enables a data read from external memory. (Active low).

$\overline{WR}$ (Write)

$\overline{WR}$ enables a data write to external memory.

$\overline{PSEN}$ (Program Store Enable)

$\overline{PSEN}$ fetches instructions only from external program memory. (Active low).

ALE (Address Latch Enable)

ALE occurs at each cycle. The falling edge of ALE addresses external data memory or external program memory. ALE can also be used as a clock output.

DB_0-DB_7 (Data Bus)

DB_0-DB_7 is a bidirectional port. DB_0-DB_7 reads and writes data using $\overline{RD}$ and $\overline{WR}$ for latching. During an external program memory fetch, DB_0-DB_7 output the low-order eight bits of the memory address. $\overline{PSEN}$ fetches the instruction. DB_0-DB_7 also output the address of an external data memory fetch. The addressed data is read and written by $\overline{RD}$ and $\overline{WR}$.

$P1_0$-$P1_7$ (Port 1)

$P1_0$-$P1_7$ is an 8-bit quasi-bidirectional port.

$P2_0$-$P2_7$ (Port 2)

$P2_0$-$P2_7$ is an 8-bit quasi-bidirectional port. $P2_0$-$P2_3$ output the high-order four bits of the address during an external program memory fetch. $P2_0$-$P2_3$ also function as a 4-bit I/O bus for the μPD82C43 I/O port expander.

PROG (Program Pulse)

PROG is used as an output pulse during a fetch when interfacing with the μPD82C43 I/O port expander.

$\overline{STOP}$ (Stop)

$\overline{STOP}$ controls the hardware STOP mode. $\overline{STOP}$ stops the oscillator when active low.

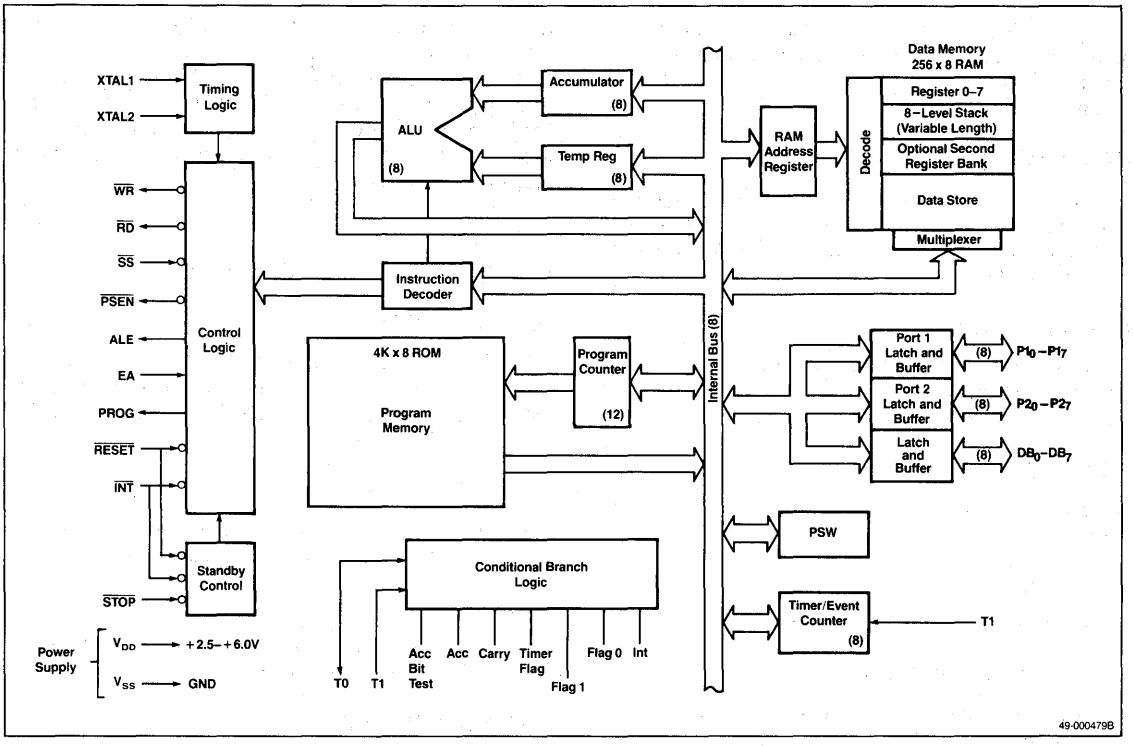
V_{DD} (Power Supply)

V_{DD} is the positive power supply (+2.5 V to +6.0 V).

V_{SS} (Ground)

V_{SS} is ground potential.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	V_{SS} −0.3 V to +7 V
Input voltage, V_I	V_{SS} −0.3 V to V_{DD} +0.3 V
Output voltage, V_O	V_{SS} −0.3 V to V_{DD} +0.3 V
Operating temperature, T_{OPT}	−40°C to +85°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Standard Voltage Range

$T_A = -40°C$ to $+85°C$, $V_{DD} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		+0.8	V	
Input voltage high	V_{IH}	$V_{DD}-2$		V_{DD}	V	Except XTAL1, XTAL2, RESET, SS
	V_{IH1}	$V_{DD}-1$		V_{DD}	V	RESET, XTAL1, XTAL2, SS
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 2.0$ mA
Output voltage high	V_{OH}	2.4			V	Bus, RD, WR, PSEN, ALE, PROG, T0; $I_{OH} = -400\,\mu A$
	V_{OH1}(1)	2.4			V	$I_{OH} = -5\,\mu A$ (type 0) port 1, port 2
		2.4			V	$I_{OH} = -50\,\mu A$ (type 1) port 1, port 2

DC Characteristics (cont)

Standard Voltage Range (cont)

$T_A = -40°C$ to $+85°C$, $V_{DD} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input current	I_{ILP}(1)		−15	−40	μA	Port 1, port 2; $V_I \leq V_{IL}$ (type 0)
				−500	μA	Port 1, port 2; $V_I \leq V_{IL}$ (type 1)
	I_{ILC}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$
Input leakage current	I_{LI1}			±1	μA	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leq V_I \leq V_{DD}$
	I_{LI2}			±3	μA	EA; $V_{SS} \leq V_I \leq V_{DD}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} \leq V_O \leq V_{DD}$ High impedance, bus, T0(3)
Standby current	I_{DD1}(4)		1.5	3.0	mA	$t_{CY} = 1.25\,\mu s$
	I_{DD2}(5)		1	20	μA	(2)
Supply current (total)	I_{DD}		6	18	mA	$t_{CY} = 1.25\,\mu s$
Data retention voltage	V_{DDDR}	2.0			V	At hardware STOP mode ($\overline{STOP}$, $\overline{RESET} \leq 0.4\,V$) or $\overline{RESET}$ ($\overline{RESET} \leq 0.4\,V$)

Extended Voltage Range

$T_A = -40°C$ to $+85°C$, $V_{DD} = +2.5\,V$ to $+6.0\,V$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		+0.18V_{DD}	V	
Input voltage high	V_{IH}	0.7V_{DD}		V_{DD}	V	Except XTAL1, XTAL2, $\overline{RESET}$, $\overline{SS}$
	V_{IH1}	0.8V_{DD}		V_{DD}	V	$\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 1.0\,mA$
Output voltage high	V_{OH}	0.75V_{DD}			V	Bus, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE, PROG, T0; $I_{OH} = -100\,\mu A$
	V_{OH1}(1)	0.7V_{DD}			V	$I_{OH} = -1\,\mu A$ (type 0) port 1, port 2
		0.7V_{DD}			V	$I_{OH} = -10\,\mu A$ (type 1) port 1, port 2
Input current	I_{ILP}(1)		−15	−40	μA	Port 1, port 2; $V_I \leq V_{IL}$ (type 0)
				−500	μA	Port 1, port 2; $V_I \leq V_{IL}$ (type 1)
	I_{ILC}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$

Extended Voltage Range (cont)

$T_A = -40°C$ to $+85°C$, $V_{DD} = +2.5\,V$ to $+6.0\,V$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input leakage current	I_{LI1}			±1	μA	T1, $\overline{INT}$, $\overline{STOP}$; $V_{SS} \leq V_I \leq V_{DD}$
	I_{LI2}			±5	μA	EA; $V_{SS} \leq V_I \leq V_{DD}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} \leq V_O \leq V_{DD}$ High impedance, bus, T0 (3)
Standby current	I_{DD1}(4)		0.3	0.6	mA	$V_{DD} = 3\,V$; $t_{CY} = 5\,\mu s$
			2.0	4.0	mA	$V_{DD} = 6\,V$ $t_{CY} = 1.25\,\mu s$
	I_{DD2}(5)		1	20	μA	(2) ; $V_{DD} = 3\,V$
			1	50	μA	$V_{DD} = 6\,V$
Supply current	I_{DD}		2.0	5.0	mA	$V_{DD} = 3\,V$; $t_{CY} = 5\,\mu s$
			10	20	mA	$V_{DD} = 6\,V$; $t_{CY} = 1.25\,\mu s$

Note:

(1) Types 0, 1, and 2 options can be specified for μPD80C50H. Type 0 for μPD80C40H only.

(2) Input pin voltage is $V_I \leq V_{IL}$ or $V_I \geq V_{IH}$.

(3) Includes port 1 and port 2 pins optionally specified with type 2.

(4) HALT mode.

(5) STOP mode.

AC Characteristics

$T_A = -40°C$ to $+85°C$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits V_{DD} = +5 V ±10% Min	Max	V_{DD} = 2.5 V to 6.0 V Min	Max	Unit	Test Conditions
Cycle time	t_{CY}	1.25	150	5	150	μs	
ALE pulse width	t_{LL}	125		995		μs	(1)
Address setup before ALE	t_{AL}	140		890		ns	(1)
Address hold from ALE	t_{LA}	45		295		ns	(1)
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	425		2300		ns	(1)
Control pulse width ($\overline{PSEN}$)	t_{CC2}	300		1800		ns	(1)
Data setup before $\overline{WR}$	t_{DW}	340		1965		ns	(1)
Data hold after $\overline{WR}$	t_{WD}	45		295		ns	(2)
Data hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}	0	95	0	470	ns	(1)
$\overline{RD}$ to data in	t_{RD1}		300		1800	ns	(1)

AC Characteristics (cont)

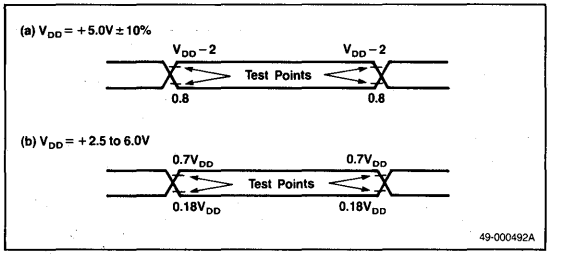
$T_A = -40°C$ to $+85°C$, $V_{SS} = 0$ V

Parameter	Symbol	Limits V_{DD} = +5 V ± 10% Min	Max	Limits V_{DD} = 2.5 V to 6.0 V Min	Max	Unit	Test Conditions
$\overline{PSEN}$ to data in	t_{RD2}		175		1300	ns	(1)
Address setup before $\overline{WR}$	t_{AW}	350		1850		ns	(1)
Address setup before data in ($\overline{RD}$)	t_{AD1}		700		3585		(1)
Address setup before data in ($\overline{PSEN}$)	t_{AD2}		500		2750	ns	(1)
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	105		600		ns	(1)
Address float to $\overline{PSEN}$	t_{AFC2}	5		125		ns	(1)
ALE to control signal ($\overline{RD}$, $\overline{WR}$)	t_{LAFC1}	175		925		ns	(1)
ALE to control signal ($\overline{PSEN}$)	t_{LAFC2}	50		425		ns	(1)
Control signal ($\overline{RD}$, $\overline{WR}$, PROG) to ALE	t_{CA1}	35		285		ns	(1)
Control signal ($\overline{PSEN}$) to ALE	t_{CA2}	280		1285		ns	(1)
Port control setup before falling edge of PROG	t_{CP}	85		460		ns	(3)
Port control hold	t_{PC1}	0	80	0	200	ns	(3, 4)
Port control hold after falling edge of PROG	t_{PC2}	135		1135		ns	(3, 5)
PROG to time P2 input must be valid	t_{PR}		585		2715	ns	(3)
Input data hold time	t_{PF}	0	125	0	500	ns	(3)
Output data setup time	t_{DP}	350		1850		ns	(3)
Output data hold time	t_{PD}	75		450		ns	(3)
PROG pulse width	t_{PP}	625		3250		ns	(3)
Port 2 I/O data setup time	t_{PL}	135		1135		ns	(3)
Port 2 I/O data hold time	t_{LP}	5		125		ns	(3)
ALE to port output	t_{PV}		475		1600	ns	(3)
T0 clock period	t_{OPRR}	250		1000		ns	(3)

Note:

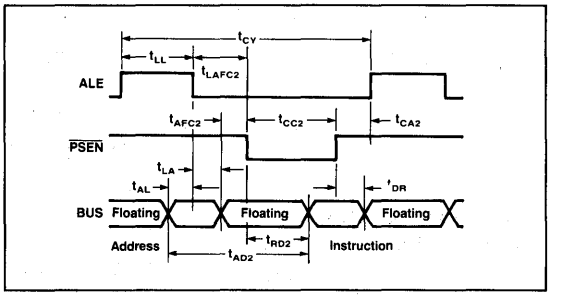
(1) Control output: $C_L = 80$ pF, bus output: $C_L = 150$ pF
(2) $C_L = 20$ pF
(3) Control output: $C_L = 80$ pF
(4) At execution of MOVD A, Pp instruction
(5) At execution of MOVD Pp, A; ANLD Pp, A; ORLD Pp, A instructions

AC Timing Test Points (Except $\overline{RESET}$, XTAL1, XTAL2, $\overline{SS}$)

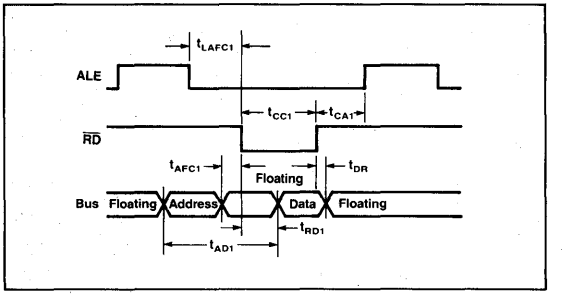


Timing Waveforms

Instruction Fetch (External Program Memory)

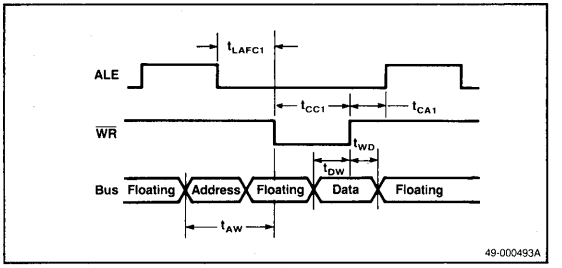


Read (External Data Memory)

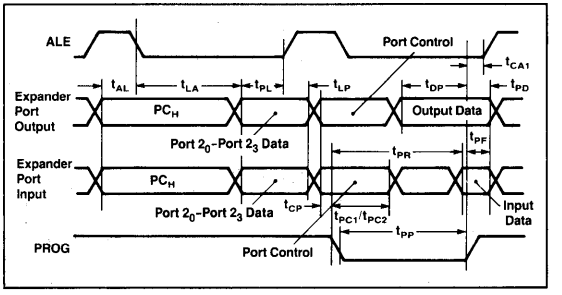


Timing Waveforms (cont)

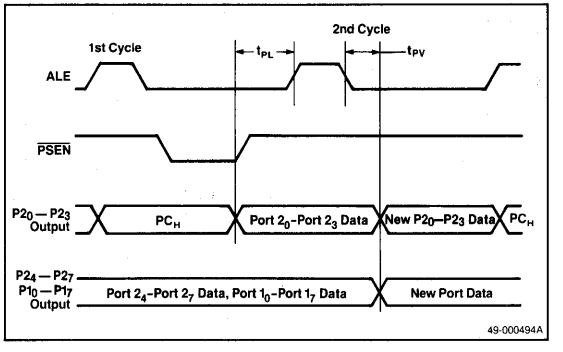
Write (External Data Memory)



Port 2 Expansion Timing



I/O Port Timing

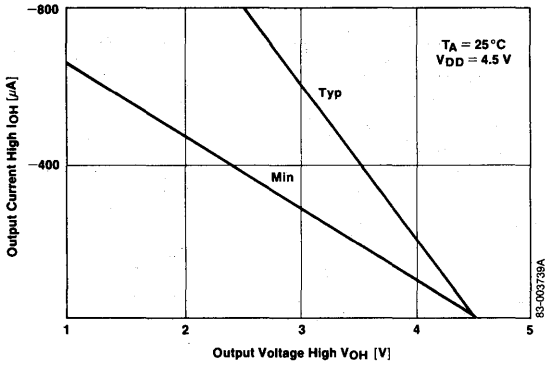


Bus Timing Requirements

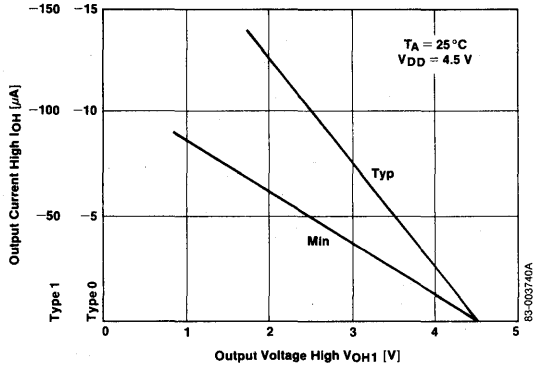
Symbol	Timing Formula	Min/Max	Unit
t_{LL}	$(7/30)\,t_{CY}-170$	Min	ns
t_{AL}	$(1/5)\,t_{CY}-110$	Min	ns
t_{LA}	$(1/15)\,t_{CY}-40$	Min	ns
t_{CC1}	$(1/2)\,t_{CY}-200$	Min	ns
t_{CC2}	$(2/5)\,t_{CY}-200$	Min	ns
t_{DW}	$(13/30)\,t_{CY}-200$	Min	ns
t_{WD}	$(1/15)\,t_{CY}-40$	Min	ns
t_{DR}	$(1/10)\,t_{CY}-30$	Max	ns
t_{RD1}	$(2/5)\,t_{CY}-200$	Max	ns
t_{RD2}	$(3/10)\,t_{CY}-200$	Max	ns
t_{AW}	$(2/5)\,t_{CY}-150$	Min	ns
t_{AD1}	$(23/30)\,t_{CY}-250$	Max	ns
t_{AD2}	$(3/5)\,t_{CY}-250$	Max	ns
t_{AFC1}	$(2/15)\,t_{CY}-65$	Min	ns
t_{AFC2}	$(1/30)\,t_{CY}-40$	Min	ns
t_{LAFC1}	$(1/5)\,t_{CY}-75$	Min	ns
t_{LAFC2}	$(1/10)\,t_{CY}-75$	Min	ns
t_{CA1}	$(1/15)\,t_{CY}-50$	Min	ns
t_{CA2}	$(4/15)\,t_{CY}-50$	Min	ns
t_{CP}	$(1/10)\,t_{CY}-40$	Min	ns
t_{PC2}	$(4/15)\,t_{CY}-200$	Min	ns
t_{PR}	$(17/30)\,t_{CY}-120$	Max	ns
t_{PF}	$(1/10)\,t_{CY}$	Max	ns
t_{DP}	$(2/5)\,t_{CY}-150$	Min	ns
t_{PD}	$(1/10)\,t_{CY}-50$	Min	ns
t_{PP}	$(7/10)\,t_{CY}-250$	Min	ns
t_{PL}	$(4/15)\,t_{CY}-200$	Min	ns
t_{LP}	$(1/30)\,t_{CY}-40$	Min	ns
t_{PV}	$(3/10)\,t_{CY}+100$	Max	ns
t_{OPRR}	$(1/5)\,t_{CY}$	Min	ns
t_{CY}	$(1/f_{XTAL})\times 15$		μs

Operating Characteristics

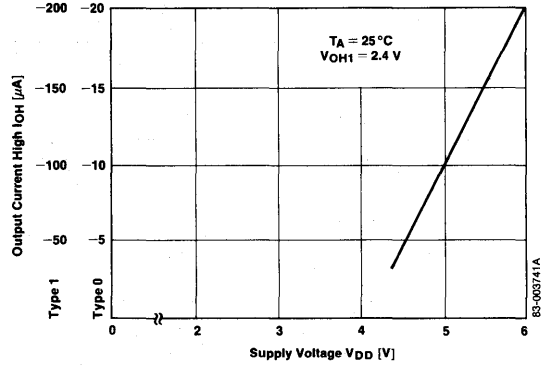
I_{OH} vs V_{OH}



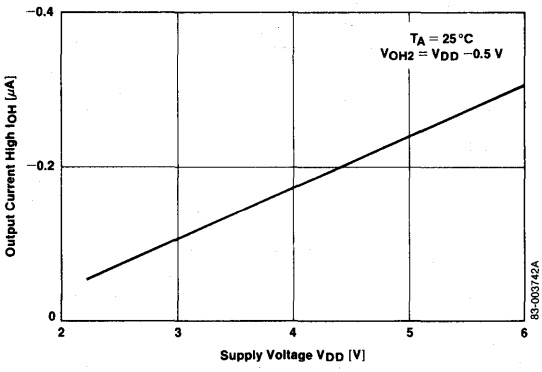
I_{OH} vs V_{OH}



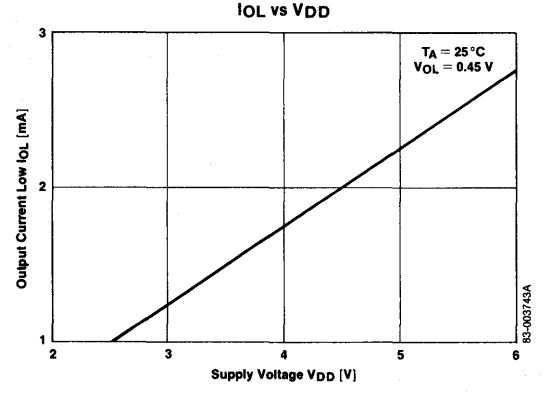
I_{OH} vs V_{DD}



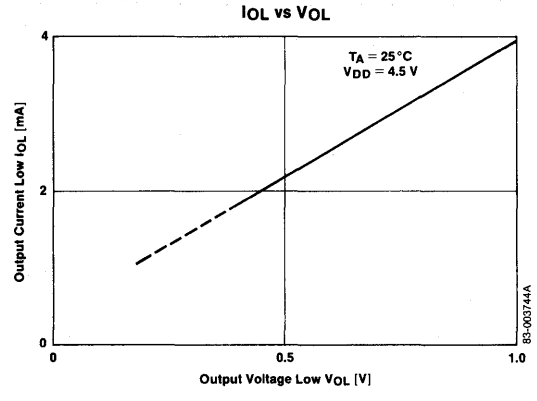
I_{OH} vs V_{DD}



I_{OL} vs V_{DD}

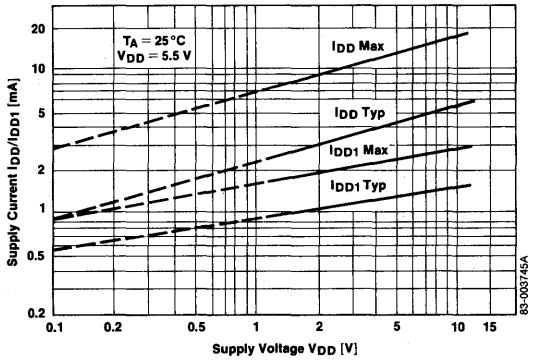


I_{OL} vs V_{OL}



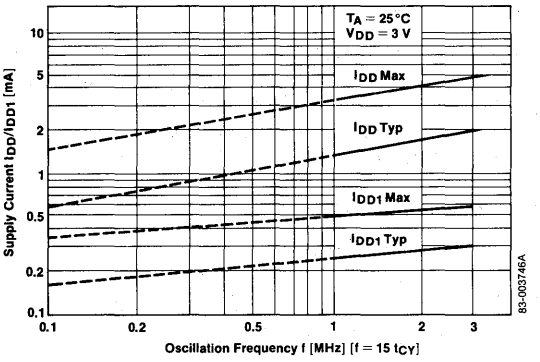
Operating Characteristics (cont)

I_{DD}/I_{DD1} vs f



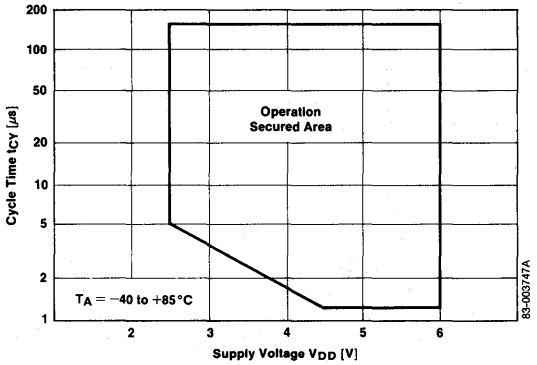
Curves below 1 MHz show characteristics for external oscillation

I_{DD}/I_{DD1} vs f

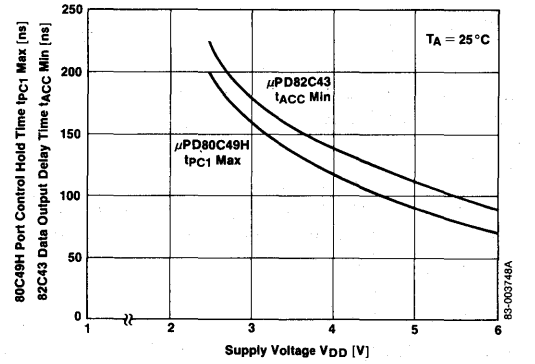


Curves below 1 MHz show characteristics for external oscillation.

t_{CY} vs V_{DD}



t_{PC1} Max [80C49H] and t_{ACC} Min [82C43] vs V_{DD}



Note: Curves without "operation secured area" show reference data.

Functional Description

The μPD80C40H/μPD80C50H has the following functional blocks:

Instruction Decoder

The instruction decoder stores the operation code of each instruction and converts it into outputs that control the functions of each block. These outputs control the functions executed by the ALU, data source, and specified registers.

Arithmetic Logic Unit (ALU)

The ALU receives 8-bit data from the accumulator or temporary register and computes an 8-bit result under control of the instruction decoder.

The ALU executes the following functions:

- Add with carry or add without carry
- Logical AND, OR, XOR
- Increment and decrement
- Bit complement
- Rotate left and right
- Swap nibbles
- BCD decimal correction

When a carry results from ALU overflows, the carry bit of the program word is set.

Accumulator

The accumulator is an 8-bit register that stores ALU input data and arithmetic results. It can also be used for transferring data between I/O ports and memory.

Temporary Register

The temporary register is an 8-bit register used for the internal processing necessary with operations such as multiply or divide. The contents of the temporary register are input to the ALU.

Program Counter

The program counter is a 12-bit register that addresses on-chip program memory by specifying the address of the next instruction to be executed.

Program Memory

The μPD80C50H contains a mask-programmable ROM of 4096 × 8 bits. Program memory can be addressed by a program counter. The μPD80C40H has no internal ROM, so it uses external program memory. External program memory is accessed by DB_0-DB_7, $P2_0$-$P2_3$, and $\overline{PSEN}$.

Data Memory

The μPD80C40H/μPD80C50H has 256 words × 8 bits of internal RAM for data memory. Data memory can be externally expanded 256 words maximum when needed.

RAM Address Register

The RAM address register specifies the next address to be accessed in data memory.

Program Status Word

The PSW (figure 1) is an 8-bit status word containing the information shown in table 1.

Figure 1. Program Status Word

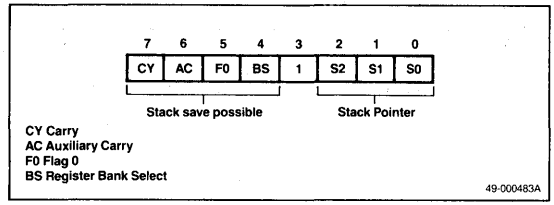


Table 1. PSW Bit Functions

Bits 0-2	Stack pointer bits (S0-S2) A $\overline{RESET}$ clears the stack pointer to 0.
Bit 3	Not used (1).
Bit 4	Working register bank switch bit (BS) 0 = Bank 0 1 = Bank 1
Bit 5	Flag bit (F0). User-controlled bit that can be complemented, cleared, or tested by conditional jump instruction JF0.
Bit 6	Auxiliary Carry (AC) Generated by an auxiliary carry, ADD instruction. Can by used by decimal adjust instruction DA A.
Bit 7	Carry flag (CY) Indicates that an accumulator overflow has taken place with the previously executed instruction.

Conditional Branch Logic

The conditional branch logic is used to test processor conditions. Use a conditional jump instruction to test the conditions shown in table 2.

Table 2. Branching Conditions

Test Device	Conditional Jump	
Accumulator	All 0	Not all 0
Accumulator bit	—	1
Carry flag	0	1
User flags (F0, F1)	—	1
Timer overflow flag	—	1
Test inputs (T0, T1)	0	1
Interrupt input (INT)	0	—

Control Logic

The control logic generates or receives the signals that control various functions including memory reads and writes, interrupts, software STOP mode, resets, and external memory fetches.

Reset Functions

A reset performs the following functions:

- Clears the program counter and the stack pointer to 0
- Selects register bank and memory bank 0
- Sets the data bus in a high impedance state (except when EA is high)
- Sets ports 1, 2 in input mode
- Disables interrupts (timer and external)
- Stops the timer
- Clears the timer flag, F0, and F1
- Disables the clock output from T0
- Releases HALT and STOP modes

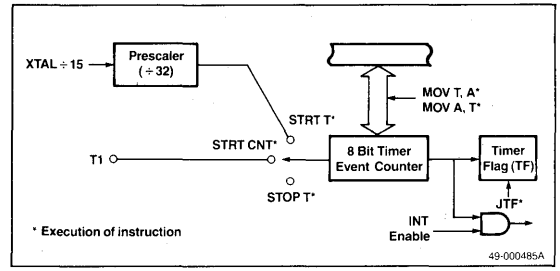
Timer/Event Counter

The timer/event counter can count external events in order to generate a precise time delay. The counter operation is the same in both modes, the only difference is the input source.

The counter is an 8-bit binary up counter (figure 2) that can be reset. It is possible to transfer the contents of the timer to the accumulator and vice-versa by using the MOV A, T and MOV T, A instructions, respectively. The contents of the counter can be independently initialized by the MOV T, A instruction. Use the STRT T instruction to use the counter as a timer and the STRT CNT instruction to use the counter as an event counter.

Once the counter starts, it continues counting until the program executes a STOP TCNT instruction or $\overline{\text{RESET}}$ becomes active. The counter is incremented up to the maximum count (FFH) and overflows when the count goes from FFH to 00H.

Figure 2. Timer/Event Counter



Event Counter. When the T1 pin and counter input are connected by the execution of a STRT CNT instruction, the counter starts counting as an event counter. A change in T1 from high to low causes a count signal which increments the counter by +1. The maximum speed of a count increment is one count per 3 machine cycles. When a 12 MHz crystal is used, the maximum speed is 1 count per 3.75 μs. There is no mimimum speed. After a count signal the T1 input must be held low at least 250 ns (at 12 MHz).

Timer. When an internal clock is connected with the counter input by the execution of the STRT T instruction, the counter starts counting as a timer. When used as a machine cycle clock, ALE is passed through a prescaler which generates an internal clock that increments the timer every 32 machine cycles. The prescaler is reset during the execution of a STRT T instruction. With a 12 MHz crystal, the counter is incremented by +1 at each 25 kHz clock every 40 μs.

You can obtain a delay from 40 μs to 10 ms (256 counts) by presetting the counter and detecting the overflow. To obtain time, through software control, in excess of 10 ms, count overflows in a separate register. To count in steps of 40 μs or less, an external clock can be supplied to the T1 input which causes the counter to operate in the event counter mode. Use the ALE frequency divided by 3 or more for the external clock. Use a software delay loop for fine adjustment of an extremely small or large delay.

Ports 1 and 2 Latch and Buffer

Ports 1 and 2 are 8-bit input/output ports. The data written to the port by an output instruction is latched and output and the data is maintained unless a new output instruction is executed. Input data is not latched, so it is necessary to stabilize input data when reading data by an input instruction.

Several port-loading options are available. At the time you order a mask ROM, (μPD80C50H), you can designate the pullup resistors for port lines $P1_0$-$P1_7$, $P2_0$-$P2_3$, and $P2_4$-$P2_7$.

Three types of pullup resistors are available:

Type 0	(I_{OH} = −5 μA: V_{DD} = +5 V ±10%)
Type 1	(I_{OH} = −50 μA: V_{DD} = +5 V ±10%)
Type 2	No pullup resistor

Only type 0 pullup resistors are available with the μPD80C40H.

Timing Logic

The oscillator generates a clock signal that controls all system timing operations. Oscillation is generated by either an external self-oscillating element or external clock input. The oscillator acts as an internal high-gain amplifier for serial resonance. To obtain the oscillation frequency, an external LC network or a crystal or ceramic external resonator may be connected.

As the crystal frequency is lowered, there is an equivalent reduction in series resistance (R). As the temperature of the crystal is lowered, R is increased. Due to this relationship, it becomes difficult to stabilize oscillation where there is low power supply voltage. When V_{CC} is less than 2.7 V and the oscillator frequency is 3 MHz or less, T_A (ambient temperature) should not be less than −10°C.

Standby Control

The standby control circuitry allows low power consumption operation. The standby function operates in 2 modes: HALT and STOP.

HALT Mode

In HALT mode, the oscillation circuit continues to operate but the internal clock stops. The CPU holds all the status of the internal circuits just prior to execution of the HALT instruction. In HALT mode, power consumption is much less than normal.

Setting HALT Mode. HALT mode is set by execution of the HALT instruction and released by either $\overline{INT}$ or $\overline{RESET}$. If interrupts are disabled and $\overline{INT}$ becomes low at a machine cycle right before the HALT instruction and remains low during 2 machine cycles, the HALT instruction byte will be fetched and decoded, but the HALT mode will not be set. Program operation resumes from the instruction following the HALT instruction.

If interrupts are enabled under the same conditions as above, the HALT instruction byte will be fetched and decoded but the HALT mode will not be set and the program will jump to the interrupt start address. After returning from the interrupt routine, the program will continue from the instruction following the HALT instruction.

Releasing HALT Mode. Release HALT mode by activating $\overline{INT}$ or $\overline{RESET}$. When using $\overline{INT}$ to release HALT mode, a low level is present at the $\overline{INT}$ pin and the internal clock is restarted. If interrupts are enabled, the interrupt is executed after the first instruction following the HALT instruction.

In the interrupt enable state, hold the $\overline{INT}$ pin low until the interrupt procedure is started to ensure the interrupt.

When using $\overline{RESET}$ to release HALT mode, a low level is present at the $\overline{RESET}$ pin and the HALT mode is reset and a normal reset operation is executed. When $\overline{RESET}$ goes to a high level, the program starts from address 0.

STOP Mode

In STOP mode, the oscillator stops and only the contents of RAM are maintained. Power consumption is lower than that of the HALT mode. You can set the STOP mode with hardware, by controlling the $\overline{RESET}$ and $\overline{STOP}$ pins; and by software, by executing the corresponding instruction.

Hardware STOP Mode

In hardware STOP mode, the contents of RAM can be held at a voltage as low as +2.0 V.

To set hardware STOP mode, set the $\overline{RESET}$ pin to a low level to protect the contents of RAM. Set the $\overline{STOP}$ pin to a low level to stop operation of the oscillation circuit.

To release hardware STOP mode, apply the normal operating level (+2.5 V to +6.0 V) to the power supply at the V_{DD} pin. As figure 3 shows, set the $\overline{STOP}$ pin to a high level while holding the $\overline{RESET}$ pin at a low level. This will restart the oscillation circuit. When $\overline{RESET}$ is set high after oscillation circuit operation is stabilized, the program is started from address 000H. Because the $\overline{STOP}$ pin controls oscillator operation, be careful to protect the $\overline{STOP}$ pin from noise.

When power is turned on, or when STOP mode is released, the oscillation circuit restarts. Because the crystal or ceramic resonator utilizes mechanical vibration, a certain time is required for the oscillation to stabilize. The "t" represents the oscillation stabilizing wait time in the timing waveform.

During this wait time, it is necessary to stop instruction execution in order to prevent CPU errors, Therefore, "t" must be longer than the oscillator's stabilizing time.

Oscillation stabilizing time differs somewhat by the type of oscillator used. With a 6 MHz oscillation frequency, a crystal resonator needs several milliseconds to stabilize, while a ceramic resonator needs several hundred microseconds. Figure 4 shows how to easily

Figure 3. Oscillator Stop and Start

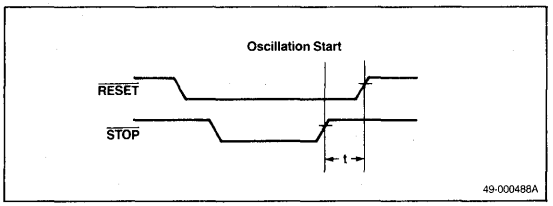
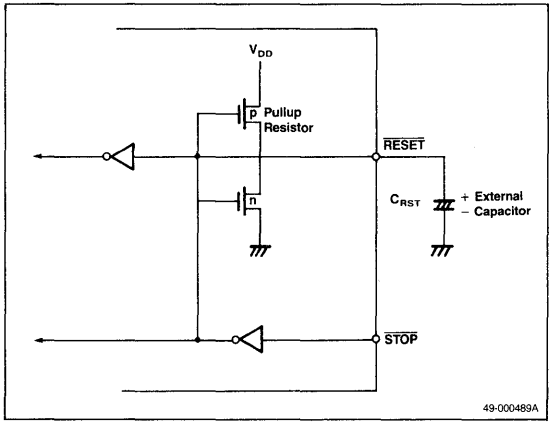


Figure 4. Hardware STOP Mode Control Circuit



control the hardware STOP mode by externally connecting a capacitor to the $\overline{\text{RESET}}$ pin. This allows control of the oscillation stabilizing time.

Software STOP Mode

In software STOP mode, the oscillation circuits stop, but the CPU maintains all status of internal circuits and data existing just before the STOP instruction. Software STOP mode is the same as when the oscillation circuit stops in HALT mode.

In software STOP mode, if a capacitor (C_{SS}) is connected to the $\overline{\text{SS}}$ pin as shown in figure 5, you can obtain the oscillation stabilizing wait time when releasing STOP mode.

Setting Software STOP Mode. To set software STOP mode, execute the STOP instruction. This sets the internal software STOP mode flip-flop which stops the oscillator and turns transistors A and B off and on, respectively. Capacitor C_{SS} discharges through transistor B causing the $\overline{\text{SS}}$ pin to go low.

Releasing Software STOP Mode. To release software STOP mode, apply an $\overline{\text{INT}}$ or $\overline{\text{RESET}}$ input.

When using the $\overline{\text{INT}}$ input (figure 6), a low at the $\overline{\text{INT}}$ pin resets the software STOP flip-flop and turns transistors A and B on and off, respectively. Then the oscillator restarts, but since $\overline{\text{SS}}$ is still low, program execution remains stopped. With transistor A on, C_{SS} charges and causes $\overline{\text{SS}}$ to go to a high level. Then, program execution restarts. The time it takes for $\overline{\text{SS}}$ to reach the threshold of a logic 1 determines the oscillation stabilizing wait time.

After software STOP mode is released, if interrupts are disabled as in the HALT mode, program execution is resumed from the instruction following the STOP instruction. If interrupts are enabled, the interrupt procedure is initiated (address 003H) after the execution of 1 instruction following the STOP instruction. To assure the interrupt, hold $\overline{\text{INT}}$ at a low level until the interrupt procedure is initiated. Even with short low level timing, the interrupt procedure will be assured if you place a 1-machine cycle instruction after the STOP instruction. However, it is recommended that you hold $\overline{\text{INT}}$ low for at least 2 machine cycles.

When using the $\overline{\text{RESET}}$ input, a low level at the $\overline{\text{RESET}}$ pin resets the software STOP flip-flop. The oscillator starts and the $\overline{\text{SS}}$ pin goes to a high level as C_{SS} is charged. The program starts from address 000H when $\overline{\text{RESET}}$ goes high. Also, since the oscillation stabilizing wait time is generated when $\overline{\text{SS}}$ is low, the $\overline{\text{RESET}}$ pin should be held low longer than the $\overline{\text{SS}}$ pin. When the oscillation stabilizing wait time is obtained by the externally connected capacitor, the value of the capacitor (C_{RST}) connected to the $\overline{\text{RESET}}$ pin (figure 4) should be set at least 3 times larger than that of capacitor C_{SS} connected to the $\overline{\text{SS}}$ pin. For example, if C_{SS} is set to 0.33 μF, C_{RST} should be 1 μF.

Figure 5. Software STOP Mode Control Circuit

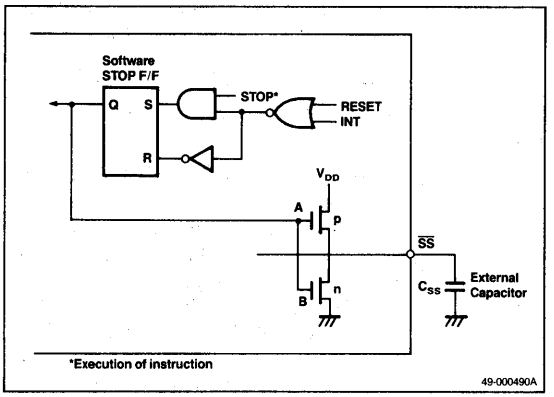
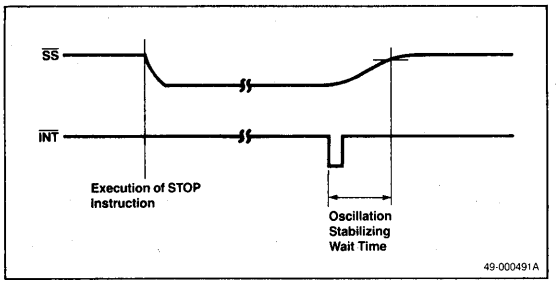


Figure 6. Software STOP Mode Timing



Instruction Set

Mnemonic	Operation	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Accumulator													
ADD A, # data	(A) ← (A) + data	Add immediate the specified data to the accumulator.(2)	03	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, Rr	(A) ← (A) + (Rr) for r = 0–7	Add contents of designated register to the accumulator.(2)	6n(4)	0	1	1	0	1	r	r	r	1	1
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0–1	Add indirect the contents the data memory location to the accumulator.(2)	6n(4)	0	1	1	0	0	0	0	r	1	1
ADDC A, # data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the accumulator.(2)	13	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0–7	Add with carry the contents of the designated register to the accumulator.(2)	7n(4)	0	1	1	1	1	r	r	r	1	1
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0–1	Add indirect with carry the contents of data memory location to the accumulator.(2)	7n(4)	0	1	1	1	0	0	0	r	1	1
ANL A, # data	(A) ← (A) AND data	Logical AND specified immediate data with accumulator.	53	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0–7	Logical AND contents of designated register with accumulator.	5n(4)	0	1	0	1	1	r	r	r	1	1
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0–1	Logical AND indirect the contents of data memory with accumulator.	5n(4)	0	1	0	1	0	0	0	r	1	1
CPL A	(A) ← NOT (A)	Complement the contents of the accumulator.	37	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clear the contents of the accumulator.	27	0	0	1	0	0	1	1	1	1	1
DA A		Decimal adjust the contents of the accumulator.(2)	57	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) – 1	Decrement by 1 the accumulator's contents.	07	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	17	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with accumulator.	43	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0–7	Logical OR contents of designated register with accumulator.	4n(4)	0	1	0	0	1	r	r	r	1	1
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0–1	Logical OR indirect the contents of data memory location with accumulator.	4n(4)	0	1	0	0	0	0	0	r	1	1
RL A	$(A_{N+1}) \leftarrow (A_N)$ $(A_0) \leftarrow (A_7)$ for N = 0–6	Rotate accumulator left by 1 bit without carry.	E7	1	1	1	0	0	1	1	1	1	1
RLC A	$(A_{N+1}) \leftarrow (A_N)$; N = 0–6 $(A_0) \leftarrow (C)$ $(C) \leftarrow (A_7)$	Rotate accumulator left by 1 bit through carry.	F7	1	1	1	1	0	1	1	1	1	1
RR A	$(A_N) \leftarrow (A_{N+1})$; N = 0–6 $(A_7) \leftarrow (A_0)$	Rotate accumulator right by 1 bit without carry.	77	0	1	1	1	0	1	1	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Accumulator (cont)													
RRC A	$(A_N) \leftarrow (A_{N+1})$; N = 0–6 $(A_7) \leftarrow (C)$ $(C) \leftarrow (A_0)$	Rotate accumulator right by 1 bit through carry.	67	0	1	1	0	0	1	1	1	1	1
SWAP A	$(A_4\text{–}A_7) \leftrightarrow (A_0\text{–}A_3)$	Swap the 2 4-bit nibbles in the accumulator.	47	0	1	0	0	0	1	1	1	1	1
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with accumulator.	D3	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0–7	Logical XOR contents of designated register with accumulator.	Dn(4)	1	1	0	1	1	r	r	r	1	1
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0–1	Logical XOR indirect the contents of data memory location with accumulator.	Dn(4)	1	1	0	1	0	0	0	r	1	1
Branch													
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0–7 If (Rr) ≠ 0; $(PC_0\text{–}PC_7) \leftarrow$ addr	Decrement the specified register and test contents.	En	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2
JBb addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if accumulator bit is set.	x2(6)	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2
JC addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	F6	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if flag F0 is set.	B6	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if flag F1 is set.	76	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_8\text{–}PC_{10}) \leftarrow (addr_8\text{–}addr_{10})$ $(PC_0\text{–}PC_7) \leftarrow (addr_0\text{–}addr_7)$ $(PC_{11}) \leftarrow$ DBF	Direct jump to specified address within the 2K address block.	x4(6)	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP @ A	$(PC_0\text{–}PC_7) \leftarrow ((A))$	Jump indirect to specified address with address page.	B3	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	E6	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNI addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	86	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if test 0 is low.	26	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if test 1 is low.	46	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_0\text{–}PC_7) \leftarrow$ addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	96	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code								Cycles	Bytes
				D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
Branch (cont)													
JTF addr	$(PC_0$–$PC_7) \leftarrow$ addr if TF = 1 $(PC) \leftarrow (PC) + 2$ if TF = 0	Jump to specified address if timer flag is set to 1.	16	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_0$–$PC_7) \leftarrow$ addr if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jump to specified address if test 0 is a 1.	36	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_0$–$PC_7) \leftarrow$ addr if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jump to specified address if test 1 is a 1.	56	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ addr	$(PC_0$–$PC_7) \leftarrow$ addr if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jump to specified address if accumulator is 0.	C6	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
Control													
EN I		Enable the external interrput input.	05	0	0	0	0	0	1	0	1	1	1
DIS I		Disable the external interrupt input.	15	0	0	0	1	0	1	0	1	1	1
ENT0 CLK		Enable the clock output pin T0.	75	0	1	1	1	0	1	0	1	1	1
SEL MB0	(DBF) ← 0	Select bank 0 (locations 0–2047) of program memory.	E5	1	1	1	0	0	1	0	1	1	1
SEL MB1	(DBF) ← 1	Select bank 1 (locations 2048–4095) of program memory.	F5	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS) ← 0	Select bank 0 (locations 0–7) of data memory.	C5	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS) ← 1	Select bank 1 (locations 24–31) of data memory.	D5	1	1	0	1	0	1	0	1	1	1
HALT		Initiates halt mode.	01	0	0	0	0	0	0	0	1	1	1
STOP		Sets CPU to software stop mode.	82	1	0	0	0	0	0	1	0	1	1
Data Moves													
MOV A, # data	(A) ← data	Move immediate the specified data into the accumulator.	23	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, Rr	(A) ← (Rr); r = 0–7	Move the contents of the designated registers into the accumulator.	Fn(4)	1	1	1	1	1	r	r	r	1	1
MOV A, @ Rr	(A) ← ((Rr)); r = 0–1	Move indirect the contents of data memory location into the accumulator.	Fn(4)	1	1	1	1	0	0	0	r	1	1
MOV A, PSW	(A) ← (PSW)	Move contents of the program status word into the accumulator.	C7	1	1	0	0	0	1	1	1	1	1
MOV Rr, # data	(Rr) ← data; r = 0–7	Move immediate the specified data into the designated register.	Bn(4)	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2
MOV Rr, A	(Rr) ← (A); r = 0–7	Move accumulator contents into the designated register.	An(4)	1	0	1	0	1	r	r	r	1	1
MOV @ Rr, A	((Rr)) ← (A); r = 0–1	Move indirect accumulator contents into data memory location.	An(4)	1	0	1	0	0	0	0	r	1	1
MOV @ Rr, # data	((Rr)) ← data; r = 0–1	Move immediate the specified data into data memory.	Bn(4)	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2
MOV PSW, A	(PSW) ← (A)	Move contents of accumulator into the program status word.	D7	1	1	0	1	0	1	1	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Data Moves (cont)													
MOVP A, @ A	$(PC_0–PC_7) \leftarrow (A)$ $(A) \leftarrow ((PC))$	Move data in the current page into the accumulator.	A3	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	$(PC_0–PC_7) \leftarrow (A)$ $(PC_8–PC_{11}) \leftarrow 0011$ $(A) \leftarrow ((PC))$	Move program data in page 3 into the accumulator.	E3	1	1	1	0	0	0	1	1	2	1
MOVX A, @ R	$(A) \leftarrow ((Rr))$; r = 0–1	Move indirect the contents of external data memory into the accumulator.	8n(4)	1	0	0	0	0	0	0	r	2	1
MOVX @ R, A	$((Rr)) \leftarrow (A)$; r = 0–1	Move indirect the contents of the accumulator into external data memory.	9n(4)	1	0	0	1	0	0	0	r	2	1
XCH A, Rr	$(A) \longleftrightarrow (Rr)$; r = 0–7	Exchange the accumulator and designated register's contents.	2n(4)	0	0	1	0	1	r	r	r	1	1
XCH A, @ Rr	$(A) \longleftrightarrow ((Rr))$; r = 0–1	Exchange indirect contents of accumulator and location in data memory.	2n(4)	0	0	1	0	0	0	0	r	1	1
XCHD A, @ Rr	$(A_0–A_3) \longleftrightarrow ((Rr))_0–((Rr))_3$; r = 0–1	Exchange indirect 4-bit contents of accumulator and data memory.	3n(4)	0	0	1	1	0	0	0	r	1	1
Flags													
CPL C	$(C) \leftarrow$ NOT (C)	Complement contents of carry bit.	A7	1	0	1	0	0	1	1	1	1	1
CPL F0	$(F0) \leftarrow$ NOT (F0)	Complement contents of flag F0.	95	1	0	0	1	0	1	0	1	1	1
CPL F1	$(F1) \leftarrow$ NOT (F1)	Complement contents of flag F1.	B5	1	0	1	1	0	1	0	1	1	1
CLR C	$(C) \leftarrow 0$	Clear contents of carry bit to 0.	97	1	0	0	1	0	1	1	1	1	1
CLR F0	$(F0) \leftarrow 0$	Clear contents of flag 0 to 0.	85	1	0	0	0	0	1	0	1	1	1
CLR F1	$(F1) \leftarrow 0$	Clear contents of flag 1 to 0.	A5	1	0	1	0	0	1	0	1	1	1
Input / Output													
ANL BUS, # data	(bus) ← (bus) AND data	Logical AND immediate specified data with contents of bus.	98	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1–2	Logical AND immediate specified data with designated port (1 or 2).	9n(5)	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
ANLD Pp, A	(Pp) ← (Pp) AND $(A_0–A_3)$; p = 4–7	Logical AND contents of accumulator with designated port (4–7).	9n(5)	1	0	0	1	1	1	p	p	2	1
IN A, Pp	(A) ← (Pp); p = 1–2	Input data from designated port (1–2) into accumulator.	0n(5)	0	0	0	0	1	0	p	p	2	1
INS A, BUS	(A) ← (bus)	Input strobed bus data into accumulator.	08	0	0	0	0	1	0	0	0	2	1
MOVD A, Pp	$(A_0–A_3) \leftarrow$ (Pp); p = 4–7 $(A_4–A_7) \leftarrow 0$	Move contents of designated port (4–7) into accumulator.	0n(5)	0	0	0	0	1	1	p	p	2	1

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Input / Output (cont)													
MOVD Pp, A	(Pp) ← (A_0–A_3); p = 4–7	Move contents of accumulator to designated port (4–7).	3n(5)	0	0	1	1	1	1	p	p	2	1
ORL BUS, # data	(bus) ← (bus) OR data	Logical OR immediate specified data with contents of bus.	88	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2
ORLD Pp, A	(Pp) ← (Pp) OR (A_0–A_3); p = 4–7	Logical OR contents of accumulator with designated port (4–7).	8n(5)	1	0	0	0	1	1	p	p	2	1
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1–2	Logical OR immediate specified data with designated port (1–2).	9n(5)	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2
OUTL BUS, A	(bus) ← (A)	Output contents of accumulator onto bus.	02	0	0	0	0	0	0	1	0	2	1
OUTL Pp,A	(Pp) ← (A); p = 1–2	Output contents of accumulator to designated port (1–2).	3n(5)	0	0	1	1	1	0	p	p	2	1
Registers													
DEC Rr	(Rr) ← (Rr) – 1; r = 0–7	Decrement by 1 contents of designated register.	Cn(4)	1	1	0	0	1	r	r	r	1	1
INC Rr	(Rr) ← (Rr) + 1; r = 0–7	Increment by 1 contents of designated register.	1n(4)	0	0	0	1	1	r	r	r	1	1
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0–1	Increment indirect by 1 the contents of data memory location.	1n(4)	0	0	0	1	0	0	0	r	1	1
Subroutine													
CALL addr	((SP)) ← (PC), (PSW_4–PSW_7) (SP) ← (SP) + 1 (PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Call designated subroutine.	x4(6)	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from subroutine without restoring program status word.	83	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW_4–PSW_7) ← ((SP))	Return from subroutine restoring program status word.	93	1	0	0	1	0	0	1	1	2	1
Timer / Counter													
EN TCNTI		Enable internal interrupt flag for timer / counter output.	25	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disable internal interrupt flag for timer / counter output.	35	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Move contents of timer / counter into accumulator.	42	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Move contents of accumulator into timer / counter.	62	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stop count for event counter.	65	0	1	1	0	0	1	0	1	1	1
STRT CNT		Start count for event counter.	45	0	1	0	0	0	1	0	1	1	1
STRT T		Start count for timer.	55	0	1	0	1	0	1	0	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Hex Code	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Miscellaneous													
NOP		No operation performed.	00	0	0	0	0	0	0	0	0	1	1

Note:

(1) Binary instruction code designations r and p represent encoded values or the lowest-order bit value of specified registers and ports, respectively.

(2) Execution of the ADD, ADDC, and DA instructions affect the carry flags, which are not shown in the respective function equations. These instructions set the carry flags when there is an overflow in the accumulator (the auxiliary carry flag is set when there is an overflow of bit 3 of the accumulator) and clear the carry flags when there is no overflow. Flags that are specifically addressed by flag instructions are shown in the function equations for those instructions.

(3) References to addresses and data are specified in byte 1 and/or 2 in the opcode of the corresponding instruction.

(4) The hex value of n for specific registers is as follows:
a) Direct addressing
R0: n = 8 R2: n = A R4: n = C R6: n = E
R1: n = 9 R3: n = B R5: n = D R7: n = F
b) Indirect addressing
@ R0: n = 0 @ R1: n = 1

(5) The hex value of n for specific ports is as follows:
P1: n = 9 P4: n = C P6: n = E
P2: n = A P5: n = D P7: n = E

(6) The hex value of x for specific accumulator or address bits is as follows:
a) JBb instruction
B_0: x = 1 B_2: x = 5 B_4: x = 9 B_6: x = D
B_1: x = 3 B_3: x = 7 B_5: x = B B_7: x = F
b) JMP instruction
Page 0: x = 0 Page 2: x = 4 Page 4: x = 8 Page 6: x = C
Page 1: x = 2 Page 3: x = 6 Page 5: x = A Page 7: x = E
c) CALL instruction
Page 0: x = 1 Page 2: x = 5 Page 4: x = 9 Page 6: x = D
Page 1: x = 3 Page 3: x = 7 Page 5: x = B Page 7: x = F

Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program memory address (a_0–a_7) or (a_0–a_{10})
b	Accumulator bit (b = 0–7)
BS	Bank switch
BUS	Bus port
C	Carry flag
CLK	Clock signal
CNT	Event counter
data	Number or expression (8 bits)
DBF	Memory bank flip-flop
F0, F1	Flags 0, 1
I	Interrupt
n	Indicates the hex number of the specified register or port
PC	Program counter
Pp	Port designator (p = 1, 2 or 4–7)
PSW	Program status word
Rr	Register designator (r = 0–7)

Symbol	Description
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Testable flags 0, 1
#	Prefix for immediate data
@	Prefix for indirect address
x	Indicates the hex number corresponding to the accumulator bit or page number specified in the operand
(x)	Contents of external RAM location
((x))	Contents of memory location addressed by the contents of external RAM location
←	Replaced by
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
EXOR	Exclusive-OR
———	Complement

μPD8041AH, μPD8741A
8-BIT, SINGLE-CHIP NMOS MICROCOMPUTERS WITH UNIVERSAL PPI

Description

The μPD8041AH and μPD8741A are programmable peripheral interface controllers intended for use in master/slave configurations with 8048, 8080A, 8085A, 8086, and other 8- and 16-bit microprocessors. The μPD8041AH/8741A functions as a totally self-sufficient controller with its own program and data memory to effectively unburden the master CPU from I/O handling and peripheral control functions.

The bus structure and data and status registers of the μPD8041AH/8741A allow easy interface to the master processor bus. This enables the processor to perform control tasks which offload main system processing and more efficiently distribute processing functions.

The μPD8041AH/8741A contains an 8-bit CPU, 1K × 8 program memory, 64 × 8 data memory, 18 I/O lines, a counter/timer, and a clock generator. The program memory for the μPD8041AH is factory mask-programmed, while program memory for the μPD8741A is UV EPROM for more flexibility.

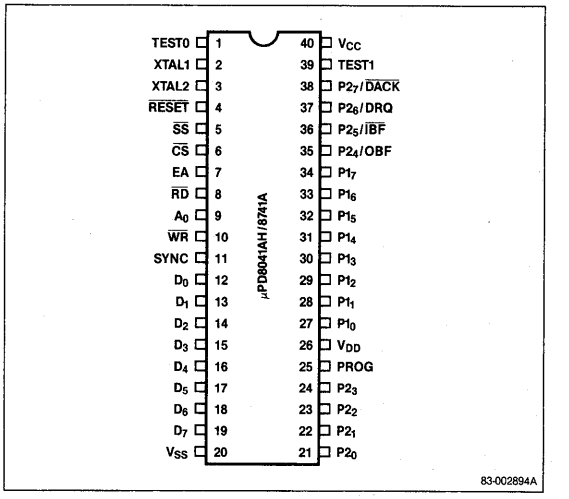
Features

- ☐ Complete single chip microcomputer
  - 8-bit CPU
  - 1K × 8 ROM
  - 64 × 8 RAM
  - 8-bit timer/counter
  - 18 I/O lines
- ☐ 8048-, 8080A-, 8085A-, 8086-compatible bus structure
- ☐ Asynchronous slave-to-master interface
  - 8-bit status register
  - Two data registers
- ☐ Interrupt, DMA, or polled operation
- ☐ Expandable I/O
- ☐ Single +5 V power supply

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD8041AHC	40-pin plastic DIP	11 MHz
μPD8741AD	40-pin cerdip with quartz window	6 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	T0	Testable input 0
2	XTAL1	Crystal input 1
3	XTAL2	Crystal input 2
4	$\overline{RESET}$	Reset input
5	$\overline{SS}$	Single step input
6	$\overline{CS}$	Chip select input
7	EA	External access input
8	$\overline{RD}$	Read strobe input
9	A_0	Address input 0
10	$\overline{WR}$	Write strobe output
11	SYNC	SYNC output
12-19	D_0-D_7	Bidirectional data bus
20	V_{SS}	Ground potential
21-24, 35-38	$P2_0$-$P2_7$	Quasi-bidirectional Port 2
25	PROG	Program pulse output
26	V_{DD}	Programming supply voltage
27-34	$P1_0$-$P1_7$	Quasi-bidirectional Port 1
39	T1	Testable input 1
40	V_{CC}	Primary power supply

Pin Functions

XTAL1 (Crystal 1)

XTAL1 is one side of the crystal or external oscillator or external frequency source.

XTAL2 (Crystal 2)

XTAL2 is the other side of the crystal or frequency source.

T0 (Test 0)

T0 is the testable input using conditional transfer functions JT0, and JNT0. T0 can also be used during programming as a testable flag.

T1 (Test 1)

T1 is the testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.

$\overline{\text{RESET}}$ (Reset)

An active low on $\overline{\text{RESET}}$ initializes the processor. $\overline{\text{RESET}}$ is also used for PROM programming, verification, and power-down.

$\overline{\text{SS}}$ (Single Step)

An active low on $\overline{\text{SS}}$, together with the SYNC output, allows the processor to single step through each instruction in program memory.

EA (External Access)

An active high on EA disables internal program memory and fetches and accesses external program memory.

$\overline{\text{RD}}$ (Read)

$\overline{\text{RD}}$ will pulse low when the processor reads data and status words from the data bus buffer or status register.

$\overline{\text{WR}}$ (Write)

$\overline{\text{WR}}$ will pulse low when the processor writes data or status words to the data bus buffer or status register.

D_0-D_7 (Data Bus)

D_0-D_7 is a three-state, bidirectional data bus. D_0-D_7 interfaces the μPD8041AH/8741A to the 8-bit master system's data bus.

$P1_0$-$P1_7$ (Port 1)

$P1_0$-$P1_7$ is an 8-bit quasi-bidirectional port.

$P2_0$-$P2_7$ (Port 2)

$P2_0$-$P2_7$ is an 8-bit quasi-bidirectional port. $P2_0$-$P2_3$ output the high-order four bits of the address during an external program memory fetch. $P2_0$-$P2_3$ also function as a 4-bit I/O bus for the μPD82C43 I/O port expander. $P2_4$-$P2_7$ can be used as port lines or interrupt requests ($\overline{\text{IBF}}$ and OBF) and DMA handshake signals (DRQ and $\overline{\text{DACK}}$).

PROG (Program Pulse)

PROG is used in programming the μPD8041AH/8741A. PROG is also used as an output pulse during a fetch when interfacing with the μPD82C43 I/O port expander.

V_{CC} (Primary Power Supply)

V_{CC} is the primary power supply. V_{CC} must be +5 V during programming and operation of the μPD8041AH.

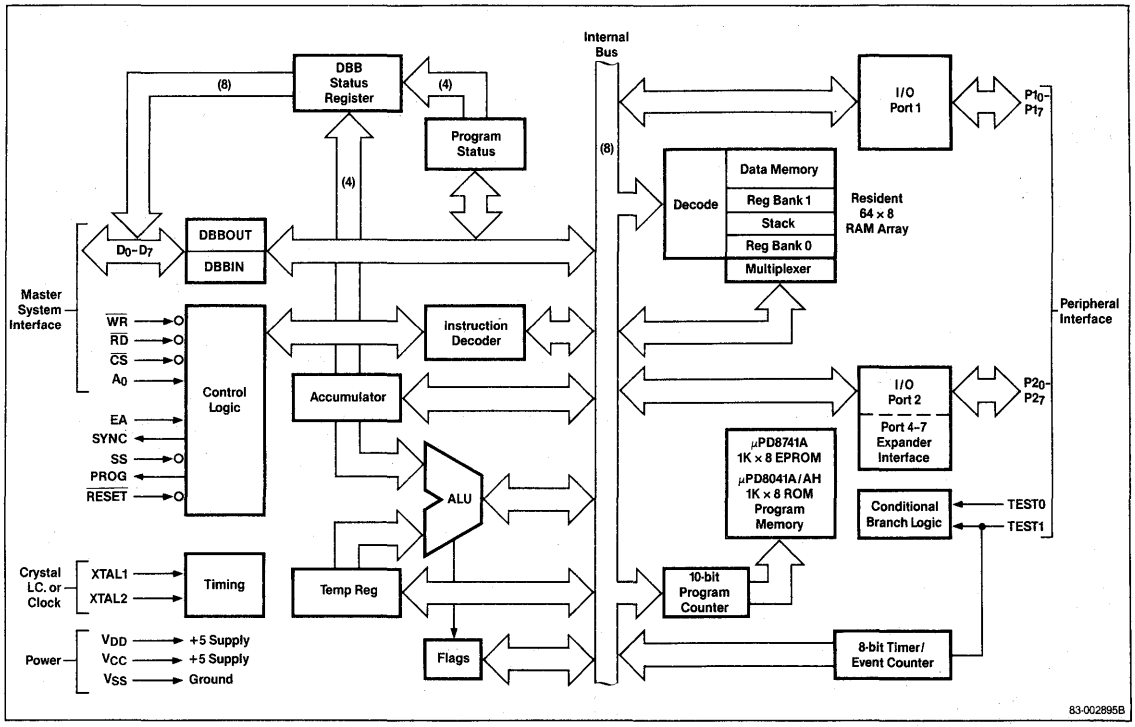
V_{DD} (Programming Supply Voltage)

V_{DD} is the programming supply voltage for programming the μPD8741AH. It is +5 V for normal operation of the μPD8041AH/8741A. V_{DD} is also the low power standby input for the ROM version.

V_{SS} (Ground)

V_{SS} is ground potential.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{CC}	−0.5 V to +7.0 V
Power supply voltage, V_{DD}	−0.5 V to +7.0 V
Input voltage, V_{IN}	−0.5 V to +7.0 V
Output voltage, V_O	−0.5 V to +7.0 V
Operating temperature, T_{OPT}	0°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			10	pF	
Output capacitance	C_{IO}			20	pF	

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DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5\,V \pm 10\%$; μPD8041AH: $V_{DD} = +5\,V \pm 5\%$; μPD8741A: $V_{SS} = 0\,V$

Parameter	Symbol	Limits μPD8741A Min	Limits μPD8741A Max	Limits μPD8041AH Min	Limits μPD8041AH Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.5	0.8	−0.5	0.8	V	All except X1, X2, and $\overline{RESET}$
	V_{IL1}	−0.5	0.6	−0.5	0.6	V	X1, X2, $\overline{RESET}$
Input voltage high	V_{IH}	2.0	V_{CC}	2.0	V_{CC}	V	Except X1, X2, and $\overline{RESET}$
	V_{IH1}	3.8	V_{CC}	3.8	V_{CC}	V	X1, X2, $\overline{RESET}$
Output voltage low	V_{OL}		0.45		0.45	V	D_0–D_7, SYNC, $I_{OL} = 2.0\,mA$
	V_{OL1}		0.45		0.45	V	Except PROG, $I_{OL} = 1.0\,mA$
	V_{OL2}		0.45		0.45	V	PROG, $I_{OL} = 1.0\,mA$
Output voltage high	V_{OH}	2.4		2.4		V	D_0–D_7, $I_{OH} = -400\,\mu A$
	V_{OH1}	2.4		2.4		V	All other outputs: $I_{OH} = -50\,\mu A$
Input current low	I_{LI}		0.5		0.5	mA	$P1_0$–$P1_7$, $P2_0$–$P2_7$: $V_{IL} = 0.8\,V$
	I_{LI1}		0.2		0.2	mA	$\overline{SS}$, $\overline{RESET}$, $V_{IL} = 0.8\,V$
Input leakage current	I_{IL}		±10		±10	μA	T0, T1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, EA, A_0, $V_{SS} \leq V_{IN} \leq V_{CC}$
Output leakage current	I_{OL}		±10		±10	μA	D_0–D_7, High Z state, $V_{SS} + 0.45\,V \leq V_{IN} \leq V_{CC}$
Supply current (total)	I_{DD}		15		15	mA	V_{DD}
	$I_{DD} + I_{CC}$		135		125	mA	

AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5\,V \pm 10\%$ $V_{SS} = 0\,V$

DBB Read

Parameter	Symbol	Limits μPD8741A Min	Limits μPD8741A Max	Limits μPD8041AH Min	Limits μPD8041AH Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{RD}$ ↓	t_{AR}	300		0		ns	
$\overline{CS}$, A_0 hold after $\overline{RD}$ ↑	t_{RA}	30		0		ns	
$\overline{RD}$ pulse width	t_{RR}	300		160		ns	
$\overline{CS}$, A_0, to data out delay	t_{AD}		370		130	ns	μPD8041A / 8741A: $C_L = 150\,pF$ μPD8041AH: $C_L = 100\,pF$
$\overline{RD}$ ↓ to data out delay	t_{RD}		200		130	ns	μPD8041A / 8741A: $C_L = 150\,pF$ μPD8041AH: $C_L = 100\,pF$
$\overline{RD}$ ↑ to data float delay	t_{DF}		140		85		
Cycle time	t_{CY}	2.5	15	1.36	15	ns	

AC Characteristics (cont)

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5\,V \pm 10\%$ $V_{SS} = 0\,V$

DBB Write

Parameter	Symbol	Limits μPD8741A Min	Limits μPD8741A Max	Limits μPD8041AH Min	Limits μPD8041AH Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{WR}$ ↓	t_{AW}	0		0		ns	
$\overline{CS}$, A_0 hold after $\overline{WR}$ ↑	t_{WA}	0		0		ns	
$\overline{WR}$ pulse width	t_{WW}	250		160		ns	μPD8041A / 8741A: $t_{CY} = 2.5\,\mu s$
Data setup to $\overline{WR}$ ↑	t_{DW}	150		130		ns	
Data hold after $\overline{WR}$ ↑	t_{WD}	0		0		ns	

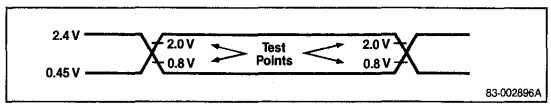
Port 2

Parameter	Symbol	Limits μPD8741A Min	Limits μPD8741A Max	Limits μPD8041AH Min	Limits μPD8041AH Max	Unit	Test Conditions
Port control setup to PROG ↓	t_{CP}	110		100		ns	μPD8041AH: $C_L = 80$ pF
Port control hold after PROG ↓	t_{PC}	100		60		ns	μPD8041AH: $C_L = 20$ pF
Input data setup to PROG ↓	t_{PR}		810		650	ns	μPD8041AH: $C_L = 80$ pF
Input data hold time	t_{PF}	0	150	0	150	ns	μPD8041AH: $C_L = 20$ pF
Output data setup time	t_{DP}	250		200		ns	μPD8041AH: $C_L = 80$ pF
Output data hold time	t_{PD}	65		65		ns	μPD8041AH: $C_L = 20$ pF
PROG pulse width	t_{PP}	1200		700		ns	

DMA

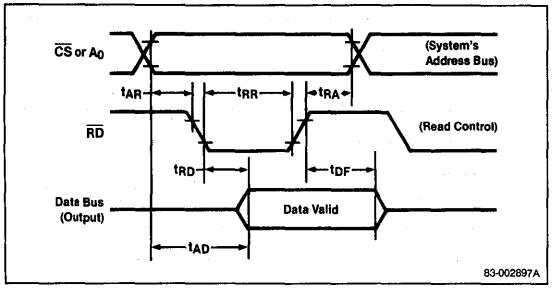
Parameter	Symbol	Limits μPD8741A Min	Limits μPD8741A Max	Limits μPD8041AH Min	Limits μPD8041AH Max	Unit	Test Conditions
$\overline{DACK}$ setup time to $\overline{RD}$, $\overline{WR}$	t_{ACC}	0		0		ns	
$\overline{DACK}$ hold time after $\overline{RD}$, $\overline{WR}$	t_{CAC}	0		0		ns	
Data output delay after $\overline{DACK}$	t_{ACD}		225		130	ns	μPD8041A / 8741A: $C_L = 150$ pF
DRQ clear delay time after $\overline{RD}$, $\overline{WR}$	t_{CRQ}		200		130	ns	μPD8041AH: $C_L = 100$ pF

AC Timing Test Points

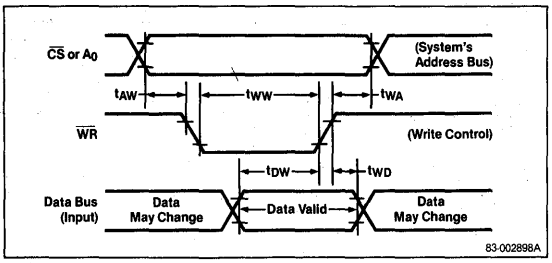


Timing Waveforms

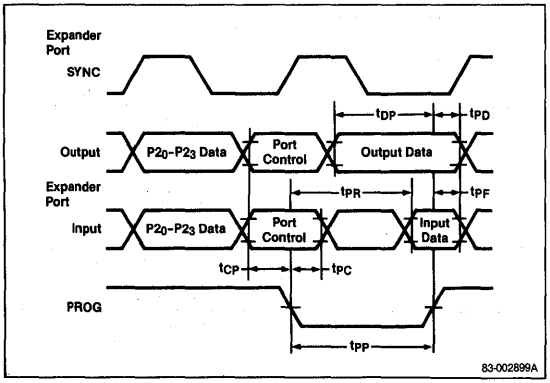
Read Operation (DBBOUT Register)



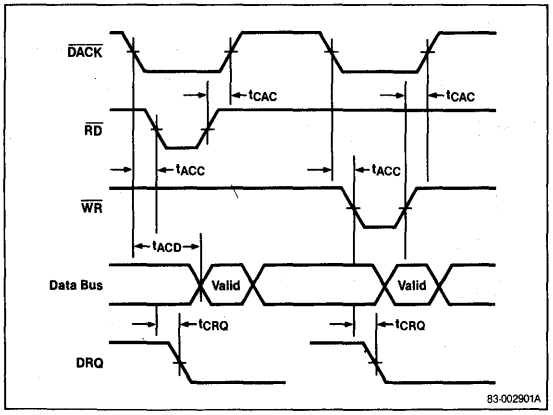
Write Operation (DBBIN Register)



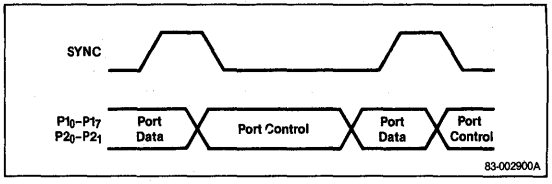
PORT 2



DMA



PORT (EA = 1)



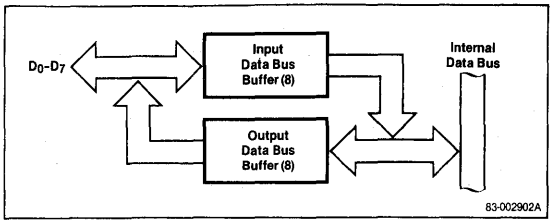
Functional Description

Two data bus buffers, an 8-bit status register, the $\overline{RD}$ and $\overline{WR}$ inputs, and expandable I/O lines enhance the μPD8041AH/8741A. These features enable easier master/slave interface and increased functionality.

Data Bus Buffers

Figure 1 shows how the input and output data bus buffers enable a smooth data flow to and from the master processors.

Figure 1. Data Bus Buffers



Status Register

The 8-bit status register includes four user-definable bits, ST_4-ST_7. Use the MOV STS, A instruction (90H) to define bits ST_4-ST_7 by moving accumulator bits 4-7 to bits 4-7 of the status register. Bits ST_0-ST_3 are not affected.

Figure 2 shows the format of the status register.

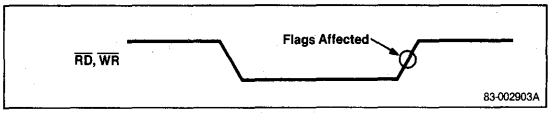
Figure 2. Status Register Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
ST_7	ST_6	ST_5	ST_4	F1	F0	IBF	OBF

$\overline{RD}$ and $\overline{WR}$

The $\overline{RD}$ and $\overline{WR}$ inputs are edge-sensitive. Figure 3 shows that status bits $\overline{IBF}$, OBF, F1, and F0 are affected on the trailing edge at $\overline{RD}$ or $\overline{WR}$.

Figure 3. $\overline{RD}$ and $\overline{WR}$ Inputs



Port 2_4-Port 2_7

$P2_4$ and $P2_5$ can be used as either port lines or buffer status flag lines. This allows you to make OBF and $\overline{IBF}$ status available externally to interrupt the master processor. Upon execution of the EN FLAGS instruction (F5H), $P2_4$ becomes the OBF pin. When a 1 is written to $P2_4$, the OBF pin is enabled and the status of OBF is output. A_0 to $P2_4$ disables the OBF pin AND the pin remains low. This pin indicates valid data is available from the μPD8041AH/8741A.

An EN FLAGS instruction execution also enables $P2_5$ to indicate that the μPD8041AH/8741A is ready to accept data. A_1 written to $P2_5$ enables the $\overline{IBF}$ pin and the status of $\overline{IBF}$ is available on $P2_5$. A_0 written to $P2_5$ disables the $\overline{IBF}$ pin. If OBF is not true, the data at the data bus is invalid.

$P2_6$ and $P2_7$ can be used as either port lines or DMA handshake lines to allow DMA interface. The EN DMA instruction (E5H) enables $P2_6$ and $P2_7$ to be used as DRQ (DMA request) and $\overline{DACK}$ (DMA acknowledge), respectively.

When a 1 is written to $P2_6$, DRQ is activated and a DMA request is issued. The EN DMA instruction deactivates DRQ. You can also deactivate DRQ by adding $\overline{DACK}$ with $\overline{RD}$ or $\overline{WR}$. Execution of the EN DMA instruction enables $P2_7$ ($\overline{DACK}$) to function as a chip select input for the data bus buffer registers during DMA transfers.

4

Instruction Set

Mnemonic	Operand	Operation	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1	$\overline{IBF}$	OBF	ST_4-ST_7
Accumulator																			
ADD	A, # data	(A) ← (A) + data	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•						
ADD	A, Rr	(A) ← (A) + (Rr) r = 0–7	0	1	1	0	1	r	r	r	1	1	•						
ADD	A, @ Rr	(A) ← (A) + ((Rr)) r = 0–1	0	1	1	0	0	0	0	r	1	1	•						
ADDC	A, # data	(A) ← (A) + (C) + data	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•						
ADDC	A, Rr	(A) ← (A) + (C) + (Rr) r = 0–7	0	1	1	1	1	r	r	r	1	1	•						
ADDC	A, @ Rr	(A) ← (A) + (C) + ((Rr)) r = 0–1	0	1	1	1	0	0	0	r	1	1	•						
ANL	A, # data	(A) ← (A) AND data	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
ANL	A, Rr	(A) ← (A) AND (Rr) r = 0–7	0	1	0	1	1	r	r	r	1	1							
ANL	A, @ Rr	(A) ← (A) AND ((Rr)) r = 0–1	0	1	0	1	0	0	0	r	1	1							
CPL	A	(A) ← NOT (A)	0	0	1	1	0	1	1	1	1	1							
CLR	A	(A) ← 0	0	0	1	0	0	1	1	1	1	1							
DA	A		0	1	0	1	0	1	1	1	1	1	•						
DEC	A	(A) ← (A) – 1	0	0	0	0	0	1	1	1	1	1							
INC	A	(A) ← (A) + 1	0	0	0	1	0	1	1	1	1	1							
ORL	A, # data	(A) ← (A) OR data	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
ORL	A, Rr	(A) ← (A) OR (Rr) r = 0–7	0	1	0	0	1	r	r	r	1	1							
ORL	A, @ Rr	(A) ← (A) OR ((Rr)) r = 0–1	0	1	0	0	0	0	0	r	1	1							
RL	A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (A_7)	1	1	1	0	0	1	1	1	1	1							

NEC

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1	$\overline{IBF}$	OBF	ST_4-ST_7
Accumulator (cont)																			
RLC	A	(AN + 1) ← (AN); N = 0–6 (A_0) ← (C) (C) ← (A_7)	1	1	1	1	0	1	1	1	1	1	•						
RR	A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (A_0)	0	1	1	1	0	1	1	1	1	1							
RRC	A	(AN) ← (AN + 1); N = 0–6 (A_7) ← (C) (C) ← (A_0)	0	1	1	0	0	1	1	1	1	1	•						
SWAP	A	(A_4–A_7) ↔ (A_0–A_3)	0	1	0	0	0	1	1	1	1	1							
XRL	A, # data	(A) ← (A) XOR data	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
XRL	A, Rr	(A) ← (A) XOR (Rr) r = 0–7	1	1	0	1	1	r	r	r	1	1							
XRL	A, @ Rr	(A) ← (A) XOR ((Rr)) r = 0–1	1	1	0	1	0	0	0	r	1	1							

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1	$\overline{IBF}$	OBF	ST_4-ST_7
Branch																			
DJNZ	Rr, addr	(Rr) ← (Rr) − 1; r = 0–7 If (Rr) ≠ 0; (PC_0–PC_7) ← addr	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2							
JB_b	addr	(PC_0–PC_7) ← addr if B_b = 1 (PC) ← (PC) + 2 if B_b = 0	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2							
JC	addr	(PC_0–PC_7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JF0	addr	(PC_0–PC_7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JF1	addr	(PC_0–PC_7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JMP	addr	(PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2							
JMPP	@A	(PC_0–PC_7) ← ((A))	1	0	1	1	0	0	1	1	2	1							
JNC	addr	(PC_0–PC_7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNIBF	addr	(PC_0–PC_7) ← addr if IBF = 0 (PC) ← (PC) + 2 if IBF = 1	1 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JOBF		(PC_0–PC_7) ← addr if OBF = 1 (PC) ← (PC) + 2 if OBF = 0	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNT0	addr	(PC_0–PC_7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNT1	addr	(PC_0–PC_7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JNZ	addr	(PC_0–PC_7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 1	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JTF	addr	(PC_0–PC_7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JT0	addr	(PC_0–PC_7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JT1	addr	(PC_0–PC_7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							
JZ	addr	(PC_0–PC_7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 1	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2							

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1	$\overline{IBF}$	OBF	ST_4-ST_7
Control																			
EN I	Enable the external interrupt input		0	0	0	0	0	1	0	1	1	1							
DIS I	Disable the external interrupt input		0	0	0	1	0	1	0	1	1	1							
SEL RB0	(BS) ← 0		1	1	0	0	0	1	0	1	1	1							
SEL RB	(BS) ← 1		1	1	0	1	0	1	0	1	1	1							
EN DMA	Enable DMA handshake		1	1	1	1	0	1	0	1	1	1							
EN FLAGS	Enable interrupt to master device		1	1	1	0	0	1	0	1	1	1							
Data Moves																			
MOV	A, # data	(A) ← data	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2							
MOV	A, Rr	(A) ← (Rr); r = 0–7	1	1	1	1	1	r	r	r	1	1							
MOV	A, @ Rr	(A) ← ((Rr)); r = 0–1	1	1	1	1	0	0	0	r	1	1							
MOV	A, PSW	(A) ← (PSW)	1	1	0	0	0	1	1	1	1	1							
MOV	Rr, # data	(Rr) ← data; r = 0–7	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2							
MOV	Rr, A	(Rr) ← (A); r = 0–7	1	0	1	0	1	r	r	r	1	1							
MOV	@ Rr, A	((Rr)) ← (A); r = 0–1	1	0	1	0	0	0	0	r	1	1							
MOV	@ Rr, # data	((Rr)) ← data; r = 0–1	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2							
MOV	PSW, A	(PSW) ← (A)	1	1	0	1	0	1	1	1	1	1							
MOVP	A, @ A	(PC_0–PC_7) ← (A) (A) ← ((PC))	1	0	1	0	0	0	1	1	2	1							
MOVP3	A, @ A	(PC_0–PC_7) ← (A) (PC_8–PC_{10}) ← 011 (A) ← ((PC))	1	1	1	0	0	0	1	1	2	1							
XCH	A, Rr	(A) ↔ (Rr); r = 0–7	0	0	1	0	1	r	r	r	1	1							
XCH	A, @ Rr	(A) ↔ ((Rr)); r = 0–1	0	0	1	0	0	0	0	r	1	1							
XCHD	A, @ Rr	(A_0–A_3) ↔ $((Rr))_0$–$((Rr))_3$; r = 0–1	0	0	1	1	0	0	0	r	1	1							

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1	$\overline{IBF}$	OBF	ST_4-ST_7
Flags																			
CPL C		(C) ← NOT (C)	1	0	1	0	0	1	1	1	1	1	•						
CPL F0		(F0) ← NOT (F0)	1	0	0	1	0	1	0	1	1	1			•				
CPL F1		(F1) ← NOT (F1)	1	0	1	1	0	1	0	1	1	1				•			
CLR C		(C) ← 0	1	0	0	1	0	1	1	1	1	1	•						
CLR F0		(F0) ← 0	1	0	0	0	0	1	0	1	1	1			•				
CLR F1		(F1) ← 0	1	0	1	0	0	1	0	1	1	1				•			
MOV STS, A		ST_4–ST_7 ← A_4–A_7	1	0	0	1	0	0	0	0	1	1							
Input / Output																			
ANL	Pp, # data	(Pp) ← (Pp) AND data p = 1–2	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2							
ANLD	Pp, A	(Pp) ← (Pp) AND (A_0–A_3); p = 4–7	1	0	0	1	1	1	p	p	2	1							
IN	A, Pp	(A) ← (Pp); p = 1–2	0	0	0	0	1	0	p	p	2	1							
IN	A, DBB	(A) ← (DBB)	0	0	1	0	0	0	1	0	1	1					•		
MOVD	A, Pp	(A_0–A_3) ← (Pp); p = 4–7 (A_4–A_7) ← 0	0	0	0	0	1	1	p	p	2	1							
MOVD	Pp, A	(Pp) ← (A_0–A_3); p = 4–7	0	0	1	1	1	1	p	p	1	1							
ORLD	Pp, A	(Pp) ← (Pp) OR (A_0–A_3); p = 4–7	1	0	0	0	1	1	p	p	1	1							
ORL	Pp, # data	(Pp) ← (Pp) OR data p = 1–2	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2							
OUT	DBB, A	(DBB) ← (A)	0	0	0	0	0	0	1	0	1	1							
OUTL	Pp, A	(Pp) ← (A); p = 1–2	0	0	1	1	1	0	p	p	1	1							
Registers																			
DEC	Rr (Rr)	(Rr) ← (Rr) – 1; r = 0–7	1	1	0	0	1	r	r	r	1	1							
INC	Rr	(Rr) ← (Rr) + 1; r = 0–7	0	0	0	1	1	r	r	r	1	1							
INC	@ Rr	((Rr)) ← ((Rr)) + 1; r = 0–1	0	0	0	1	0	0	0	r	1	1							

NEC

Instruction Set (cont)

Mnemonic	Operand	Operation	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1	$\overline{IBF}$	OBF	ST_4-ST_7
Subroutine																			
CALL	addr	((SP)) ← (PC), (PSW_4-PSW_7), (SP) ← (SP) + 1 (PC_8-PC_{10}) ← ($addr_8$-$addr_{10}$) (PC_0-PC_7) ← ($addr_0$-$addr_7$) (PC_{11}) ← DBF	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2							
RET		(SP) ← (SP) = 1 (PC) ← ((SP))	1	0	0	0	0	0	1	1	2	1							
RETR		(SP) ← (SP) = 1 (PC) ← ((SP)) (PSW_4-PSW_7) ← ((SP))	1	0	0	1	0	0	1	1	2	1							
Timer / Counter																			
EN TCNTI	Enable internal interrupt flag for timer / counter output.		0	0	1	0	0	1	0	1	1	1							
DIS TCNTI	Disable internal interrupt flag for timer / counter output.		0	0	1	1	0	1	0	1	1	1							
MOV A, T	(A) ← (T)		0	1	0	0	0	0	1	0	1	1							
MOV T, A	(T) ← (A)		0	1	1	0	0	0	1	0	1	1							
STOP TCNT	Stop count for event counter.		0	1	1	0	0	1	0	1	1	1							
STRT CNT	Start count for event counter.		0	1	0	0	0	1	0	1	1	1							
STRT T	Start count for timer.		0	1	0	1	0	1	0	1	1	1							
Miscellaneous																			
NOP		No operation performed.	0	0	0	0	0	0	0	0	1	1							

Note:

(1) Operation code designations r and p form the binary representation of the registers and ports involved.

(2) The dot under the appropriate flag bit indicates that its contents is subject to change by the instruction it appears in.

(3) References to the address and data are specified in bytes 2 and/or 1 of the instruction.

(4) Numerical subscripts appearing in the operation column reference the specific bits affected.

Instruction Set (cont)

Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program memory address (12 bits)
B_b	Bit designator (b = 0–7)
BS	Bank switch
BUS	Bus port
C	Carry flag
CLK	Clock signal
CNT	Event counter
D	Nibble designator (4 bits)
data	Number of expression (8 bits)
DBF	Memory bank flip-flop
F0, F1	Flags 0, 1
I	Interrupt
P	In-page operation designator
IBF	Input buffer full flag
Pp	Port designator (p = 1, 2 or 4–7)
PSW	Program status word

Symbol	Description
Rr	Register designator (r = 0, 1 or 0–7)
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Testable inputs 0, 1
X	External RAM
#	Prefix for immediate data
@	Prefix for indirect address
$	Current value of program counter
(x)	Contents of external RAM location
((x))	Contents of memory location addressed by the contents of external RAM location
←	Replaced by
OBF	Output buffer full flag
DBB	Data bus buffer
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
XOR	Exclusive-OR

NEC
NEC Electronics Inc.

μPD80C42
8-BIT, SINGLE-CHIP CMOS MICROCOMPUTER WITH UNIVERSAL PPI

Description

The μPD80C42 is a CMOS programmable peripheral interface controller which contains its own 8-bit microcomputer. It is well suited for use in master/slave configurations or as an intelligent peripheral device in applications requiring very low power consumption. The μPD80C42 has a CPU, 2K bytes of RAM, and 8-bit timer/counter, and I/O ports. I/O capability can be expanded by adding a μPD82C43, which interfaces directly to the μPD80C42. The external bus structure and associated control signals allow easy interfacing to 8048, 8085, and other microprocessor systems. The two standby modes allow even further reduction of power consumption in energy conscious systems.

With the exception of the $\overline{STOP}$ pin, the μPD80C42 is pin-for-pin compatible with the μPD8041A and the μPD8741A.

Features

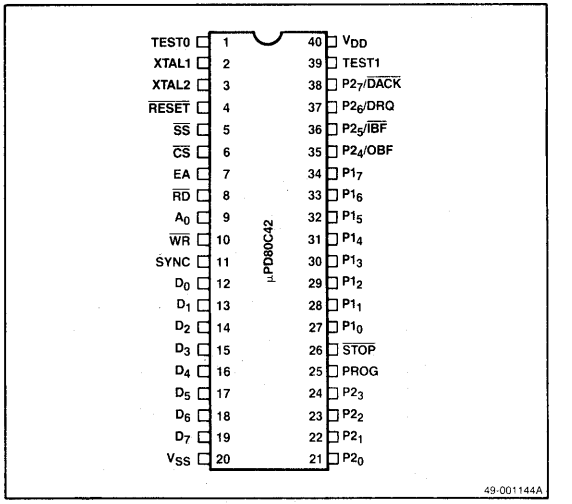
- ☐ CMOS technology
- ☐ Low power consumption
- ☐ 8048-, 8085A-, and 8086-bus compatible
- ☐ 8-bit CPU with 2K × 8 ROM and 128 × 8 RAM
- ☐ 8-bit timer/counter
- ☐ 18 I/O lines
- ☐ 8-bit status register
- ☐ Two data registers for asynchronous slave-to-master interface
- ☐ Interrupt, DMA, or polled operation
- ☐ Expandable I/O
- ☐ Two power down modes
- ☐ 8041A-, 8741A-pin compatible
- ☐ On-chip clock generator
- ☐ Single +5 V power supply

Ordering Information

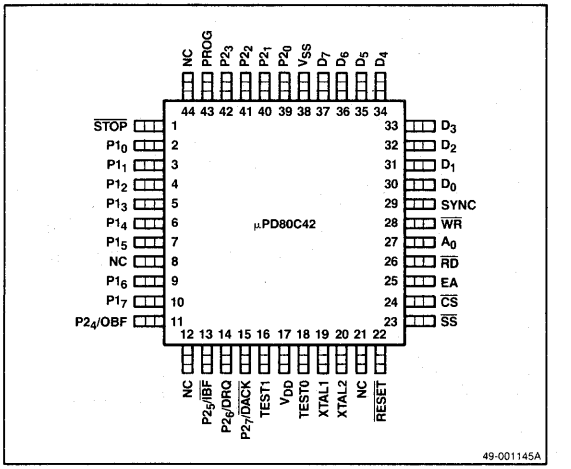
Part Number	Package Type	Max Frequency of Operation
μPD80C42C	40-pin plastic DIP	8 MHz
μPD80C42G-22	44-pin plastic miniflat	8 MHz

Pin Configurations

40-Pin Plastic DIP



44-Pin Plastic Miniflat



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Pin Identification

Plastic DIP

No.	Symbol	Function
1	TEST0	Test 0 input
2, 3	XTAL1, XTAL2	Crystal input
4	$\overline{RESET}$	Reset input
5	$\overline{SS}$	Single-step input
6	$\overline{CS}$	Chip select input
7	EA	External access input
8	$\overline{RD}$	Read input
9	A_0	Address input
10	$\overline{WR}$	Write input
11	SYNC	Synchronize output
12–19	D_0–D_7	Bidirectional port
20	V_{SS}	Ground
21–24	$P2_0$–$P2_3$	Quasi-bidirectional port 2
35–38	$P2_4$ / $\overline{OBF}$, $P2_5$ / $\overline{IBF}$, $P2_6$ / $\overline{DRQ}$, $P2_7$ / $\overline{DACK}$	Output buffer full, input buffer full, DMA request, DMA acknowledge
25	PROG	PROG output strobe
26	$\overline{STOP}$	$\overline{STOP}$ input
27–34	$P1_0$–$P1_7$	Quasi-bidirectional port 1
39	TEST1	Test 1 input
40	V_{DD}	Positive power supply
—	NC	No connection

Plastic Miniflat

No.	Symbol	Function
18	TEST0	Test 0 input
19, 20	XTAL1, XTAL2	Crystal input
22	$\overline{RESET}$	Reset input
23	$\overline{SS}$	Single-step input
24	$\overline{CS}$	Chip select input
25	EA	External access input
26	$\overline{RD}$	Read input
27	A_0	Address input
28	$\overline{WR}$	Write input
29	SYNC	Synchronize output
30–37	D_0–D_7	Bidirectional port
38	V_{SS}	Ground
39–42	$P2_0$–$P2_3$	Quasi-bidirectional port 2
11, 13–15	$P2_4$ / $\overline{OBF}$, $P2_5$ / $\overline{IBF}$, $P2_6$ / $\overline{DRQ}$, $P2_7$ / $\overline{DACK}$	Output buffer full, input buffer full, DMA request, DMA acknowledge
43	PROG	PROG output strobe
1	$\overline{STOP}$	$\overline{STOP}$ input
2–7, 9–10	$P1_0$–$P1_7$	Quasi-bidirectional port 1
16	TEST1	Test 1 input
17	V_{DD}	Positive power supply
8, 12, 21, 44	NC	No connection

Pin Functions

XTAL1, XTAL2 (Crystal)

XTAL1 and XTAL2 are the inputs for the crystal oscillator for the LC circuit generating internal clock signals. Use XTAL1 as the external clock input.

TEST0 (Test 0)

TEST0 is a testable input using conditional jump instructions JT0 and JNT0. TEST0 also resets the HALT mode.

TEST1 (Test 1)

TEST1 is a testable input using conditional jump instructions JT0 and JNT0. TEST1 is also an input to the event counter.

$\overline{RESET}$ (Reset)

$\overline{RESET}$ inputs a system reset, resets the HALT mode, and controls the STOP mode.

$\overline{SS}$ (Single-Step)

$\overline{SS}$ is an input used with SYNC to step the program through each instruction.

$\overline{CS}$ (Chip Select)

$\overline{CS}$ inputs the chip select signal. An active low enables the data bus.

EA (External Access)

EA is an input that inhibits internal program memory fetches. Use EA to check the ROM contents when debugging programs.

$\overline{WR}$ (Write)

$\overline{WR}$ is an input used by the master CPU to write data and commands into the data bus buffer in (DBBIN) register.

$\overline{RD}$ (Read)

$\overline{RD}$ is the input used by the master CPU to read data or

status words from the data bus buffer out (DBBOUT) or status registers.

A_0 (Address 0)

A_0 is an address input that the master CPU uses to determine the bus operation as follows:

Cycle	A_0	Operation
Read	0	Data
	1	Status
Write	0	Data
	1	Command

SYNC (Synchronization)

SYNC is an output that occurs once per instruction cycle. SYNC is used as a strobe for external circuitry or to synchronize the single-step operation.

PROG (PROG output)

When using the I/O expansion port (μPD82C43), PROG outputs a strobe that outputs data/addresses $P2_0$–$P2_3$.

$\overline{STOP}$ (Stop)

The $\overline{STOP}$ input controls the hardware STOP mode.

D_0–D_7 (Port)

D_0–D_7 is a bidirectional port that transfers data between the data bus buffer (DBBOUT, DBBIN) registers and the 8-bit master CPU data bus.

$P1_0$–$P1_7$ (Port 1)

$P1_0$–$P1_7$ is a quasi-bidirectional, 8-bit port.

$P2_0$–$P2_7$ (Port 2)

$P2_0$–$P2_7$ is a quasi-bidirectional, programmable 8-bit port. $P2_4$–$P2_7$ (high-order bits) are alternative pins for the following interrupt request and DMA handshaking functions:

$P2_4 = \overline{OBF}$ (Output buffer full)
$P2_5 = IBF$ (Input buffer full)
$P2_6 = \overline{DRQ}$ (DMA request)
$P2_7 = \overline{DACK}$ (DMA acknowledge)

V_{DD} (Power Supply)

V_{DD} is the positive power supply (+2.5 V to +6.0 V)

V_{SS} (Ground)

V_{SS} is the ground potential.

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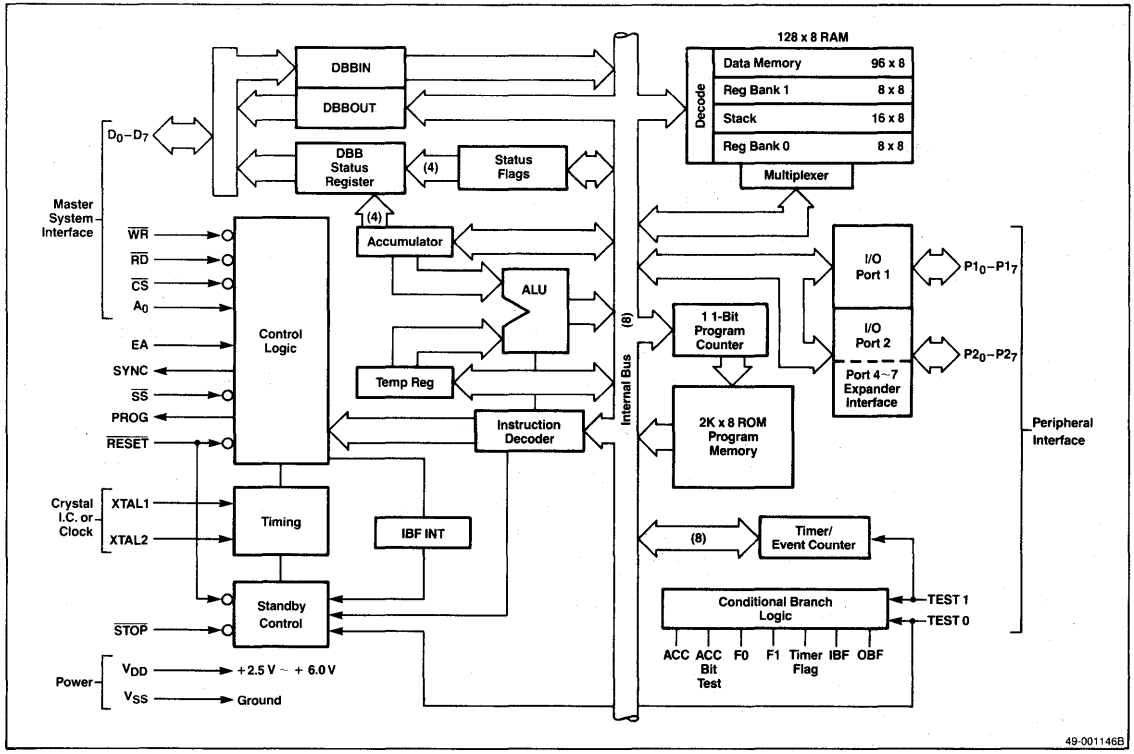
Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	−0.3 V to V_{DD} +0.3 V
Operating temperature, T_{OPT}	−40°C to +85°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Standard Voltage Range

$T_A = -40°C$ to +85°C, $V_{DD} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		+0.8	V	
Input voltage high	V_{IH}	2.2		V_{DD}	V	Except $\overline{RESET}$, XTAL1, XTAL2
	V_{IH1}	$V_{DD}-1$		V_{DD}	V	$\overline{RESET}$, XTAL1, XTAL2
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 2.0$ mA
Output voltage high	V_{OH}	2.4			V	D_0–D_7, SYNC, PROG; $I_{OH} = -400\,\mu A$
	V_{OH1}	2.4			V	Port 1, port 2; $I_{OH} = -50\,\mu A$
	V_{OH2}	$V_{DD}-0.5$			V	All outputs; $I_{OH} = -0.2\,\mu A$
Input current	I_{ILP}			−500	μA	Port 1, port 2; $V_I \leq V_{IL}$
	I_{ILC}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$
Input leakage current	I_{LI1}			±1	μA	T0, T1, $\overline{STOP}$, $\overline{CS}$, A_0, $\overline{RD}$, $\overline{WR}$; $V_{SS} \leq V_I \leq V_{DD}$
	I_{LI2}			±3	μA	EA; $V_{SS} \leq V_I \leq V_{DD}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} \leq V_O \leq V_{DD}$ High impedance, D_0–D_7, port
Standby current	I_{DD1}		1.5	3.0	mA	HALT mode; $t_{CY} = 1.25\,\mu s$
	I_{DD2}		2	20	μA	$\overline{STOP}$ mode (1)
Supply current	I_{DD}		10	20	mA	$t_{CY} = 1.25\,\mu s$
Data retention voltage	V_{DDDR}	2.0			V	$\overline{STOP}$ mode ($\overline{STOP}$, $\overline{RESET} \leq 0.4$ V) or $\overline{RESET}$ ($\overline{RESET} \leq 0.4$ V)

Note: (1) The input voltage pin is $V_I \leq V_{IL}$ or $V_I \geq V_{IH}$.

Extended Voltage Range

$T_A = -40°C$ to +85°C, $V_{DD} = +2.5\,V$ to $+6.0\,V$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		+0.6	V	$2.5\,V \leq V_{DD} \leq 4.5\,V$
		−0.3		+0.8	V	$4.5\,V \leq V_{DD} \leq 6.0\,V$
Input voltage high	V_{IH}	$0.7V_{DD}$		V_{DD}	V	Except $\overline{RESET}$, XTAL1, XTAL2
	V_{IH1}	$0.8V_{DD}$		V_{DD}	V	$\overline{RESET}$, XTAL1, XTAL2
Output voltage low	V_{OL}			+0.45	V	$I_{OL} = 1.0$ mA
Output voltage high	V_{OH}	$0.75V_{DD}$			V	D_0–D_7, SYNC, PROG; $I_{OH} = -100\,\mu A$
	V_{OH1}	$0.7V_{DD}$			V	Port 1, port 2; $I_{OH} = -10\,\mu A$
Input current	I_{ILP}			−500	μA	Port 1, port 2; $V_I \leq V_{IL}$
	I_{ILC}			−40	μA	$\overline{SS}$, $\overline{RESET}$; $V_I \leq V_{IL}$
Input leakage current	I_{LI1}			±1	μA	T0, T1, $\overline{STOP}$, $\overline{CS}$, A_0, $\overline{RD}$, $\overline{WR}$; $V_{SS} \leq V_I \leq V_{DD}$
	I_{LI2}			±5	μA	EA; $V_{SS} \leq V_I \leq V_{DD}$
Output leakage current	I_{LO}			±1	μA	$V_{SS} \leq V_O \leq V_{DD}$ High impedance, D_0–D_7, port
Standby current	I_{DD1}		300	600	μA	HALT mode; $V_{DD} = 3$ V; $t_{CY} = 5\,\mu s$
			2.0	4.0	mA	$V_{DD} = 6$ V $t_{CY} = 1.25\,\mu s$
	I_{DD2}		1	20	μA	STOP mode (1); $V_{DD} = 3$ V
			2	50	mA	$V_{DD} = 6$ V
Supply current	I_{DD}		2.0	5.5	mA	$V_{DD} = 3$ V; $t_{CY} = 5\,\mu s$
			16	30	mA	$V_{DD} = 6$ V; $t_{CY} = 1.25\,\mu s$
Data retention voltage	V_{DDDR}	2.0			V	$\overline{STOP}$ mode ($\overline{STOP}$, $\overline{RESET} \leq 0.4$ V) or $\overline{RESET}$ ($\overline{RESET} \leq 0.4$ V)

Note:
(1) The input voltage pin is $V_I \leq V_{IL}$ or $V_I \geq V_{IH}$.

AC Characteristics

Standard Voltage Range — DBB Read

$T_A = -0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{RD}$ low	t_{AR}	0			ns	
$\overline{CS}$, A_0 hold from $\overline{RD}$ high	t_{RA}	0			ns	
$\overline{RD}$ pulse width	t_{RR}	200			ns	
$\overline{CS}$, A_0 to data output delay	t_{AD}			150	ns	$C_L = 100$ pF
$\overline{RD}$ low to data output delay	t_{RD}			140	ns	$C_L = 100$ pF
$\overline{RD}$ high to data float delay	t_{DF}	0		85	ns	
Cycle time	t_{CY}	1.25		15	μs	

Standard Voltage Range — DBB Write

$T_A = -0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{WR}$ low	t_{AW}	0			ns	
$\overline{CS}$, A_0 hold from $\overline{WR}$ high	t_{WA}	0			ns	
$\overline{WR}$ pulse width	t_{WW}	200			ns	
data setup to $\overline{WR}$ high	t_{DW}	130			ns	
Data hold from $\overline{WR}$ high	t_{WD}	0			ns	

Extended Voltage Range — DBB Read

$T_A = -0°C$ to $+70°C$, $V_{DD} = +2.5V$ to $+6.0V$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{RD}$ low	t_{AR}	300			ns	
$\overline{CS}$, A_0 hold from $\overline{RD}$ high	t_{RA}	200			ns	
$\overline{RD}$ pulse width	t_{RR}	2000			ns	
$\overline{RD}$ low to data output delay	t_{RD}			1500	ns	$C_L = 100$ pF
$\overline{RD}$ high to data float delay	t_{DF}	0		400	ns	
Cycle time	t_{CY}	5		15	μs	

Extended Voltage Range — DBB Write

$T_A = -0°C$ to $+70°C$, $V_{DD} = +2.5V$ to $6.0V$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{CS}$, A_0 setup to $\overline{WR}$ low	t_{AW}	300			ns	
$\overline{CS}$, A_0 hold from $\overline{WR}$ high	t_{WA}	200			ns	
$\overline{WR}$ pulse width	t_{WW}	2000			ns	
data setup to $\overline{WR}$ high	t_{DW}	1500			ns	
Data hold from $\overline{WR}$ high	t_{WD}	200			ns	

Standard Voltage Range — Port 2

$V_{DD} = +5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port control setup to PROG low	t_{CP}	100			ns	$C_L = 80$ pF
Input port control hold from PROG low	t_{PC1}	0		80	ns	$C_L = 20$ pF
Output port control hold from PROG low	t_{PC2}	135			ns	$C_L = 20$ pF
Input data setup to PROG low	t_{PR}			650	ns	$C_L = 80$ pF
Input data hold from PROG high	t_{PF}	0		150	ns	$C_L = 20$ pF
Output data setup to PROG high	t_{DP}	200			ns	$C_L = 80$ pF
Output data hold from PROG high	t_{PD}	60			ns	$C_L = 20$ pF
PROG pulse width	t_{PP}	700			ns	

4

AC Characteristics (cont)

Extended Voltage Range — Port 2

V_{DD} = +2.5 V to +6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port control setup to PROG low	t_{CP}	460			ns	C_L = 80 pF
Input port control hold from PROG low	t_{PC1}	0		200	ns	C_L = 20 pF
Output port control hold from PROG low	t_{PC2}	1135			ns	C_L = 20 pF
Input data setup to PROG low	t_{PR}			2715	ns	C_L = 80 pF
Input data hold from PROG high	t_{PF}	0		500	ns	C_L = 20 pF
Output data setup to PROG high	t_{DP}	1850			ns	C_L = 80 pF
Output data hold from PROG high	t_{PD}	450			ns	C_L = 20 pF
PROG pulse width	t_{PP}	3250			ns	

Standard Voltage Range — DMA

V_{DD} = +5 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{DACK}$ setup to $\overline{RD}$, $\overline{WR}$	t_{ACC}	0			ns	
$\overline{DACK}$ hold from $\overline{RD}$, $\overline{WR}$	t_{CAC}	0			ns	
$\overline{DACK}$ to data output delay	t_{ACD}			140	ns	
$\overline{RD}$, $\overline{WR}$ to DRQ clear delay	t_{CRQ}			130	ns	C_L = 150 pF

Extended Voltage Range — DMA

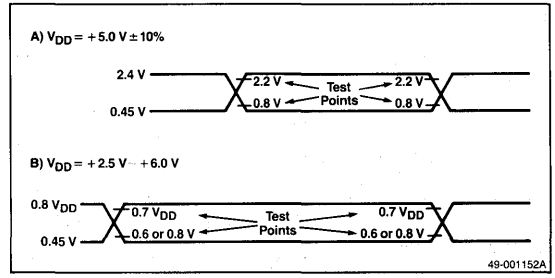
V_{DD} = +2.5 V to +6.0 V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{DACK}$ setup to $\overline{RD}$, $\overline{WR}$	t_{ACC}	200			ns	
$\overline{DACK}$ hold from $\overline{RD}$, $\overline{WR}$	t_{CAC}	200			ns	
$\overline{DACK}$ to data output delay	t_{ACD}			1500	ns	
$\overline{RD}$, $\overline{WR}$ to DRQ clear delay	t_{CRQ}			700	ns	C_L = 150 pF

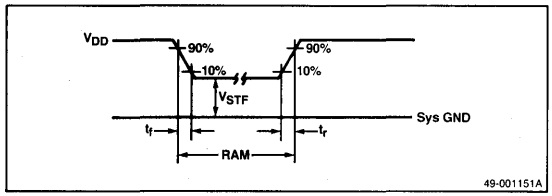
Standby Flag Retention Conditions

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Preservation of standby flag voltage fall time	t_f	100			μs	
Preservation of standby flag voltage rise time	t_r	100			μs	
Standby flag retention voltage	V_{STF}	2.0			V	

Input Waveforms for AC Test



Standby Flag Retention Timing

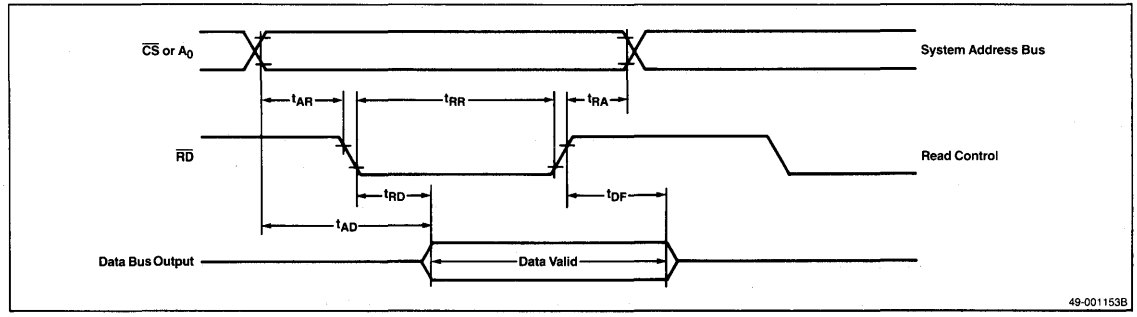


Bus Timing Requirements

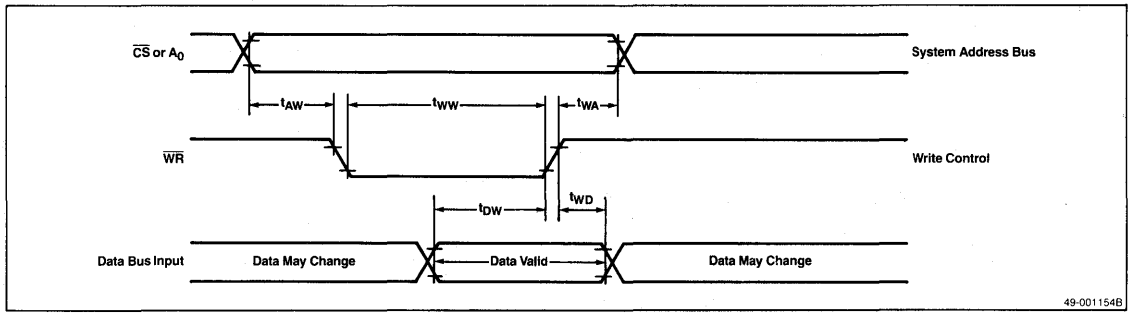
Symbol	Timing Formula	Min/Max	Unit
t_{CP}	$(1/10)\,t_{CY}-40$	Min	ns
t_{PC2}	$(4/15)\,t_{CY}-200$	Min	ns
t_{PR}	$(17/30)\,t_{CY}-120$	Max	ns
t_{PF}	$(1/10)\,t_{CY}$	Max	ns
t_{DP}	$(2/5)\,t_{CY}-150$	Min	ns
t_{PD}	$(1/10)\,t_{CY}-50$	Min	ns
t_{PP}	$(7/10)\,t_{CY}-250$	Min	ns
t_{CY}	$(1/f_{XTAL})\times 15$		μs

Timing Waveforms

Read Operation (DBBOUT Register)



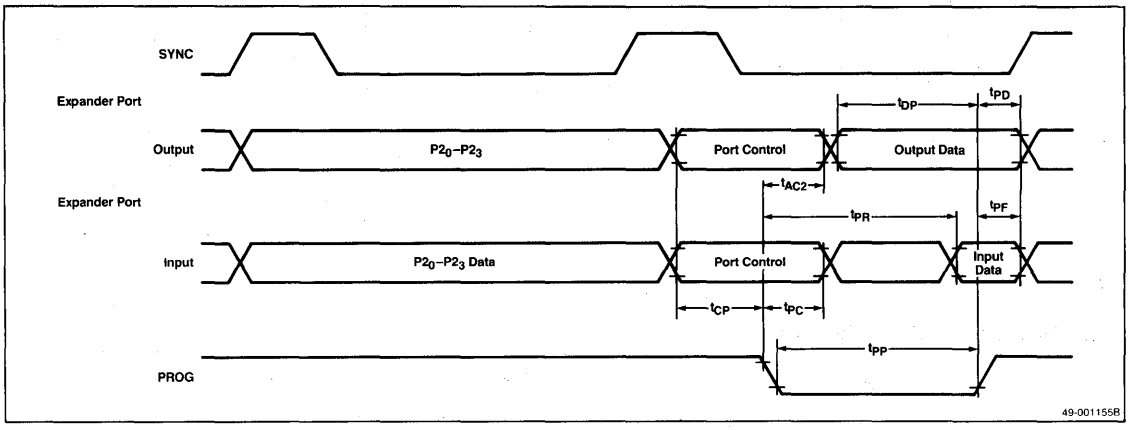
Write Operation (DBBIN Register)



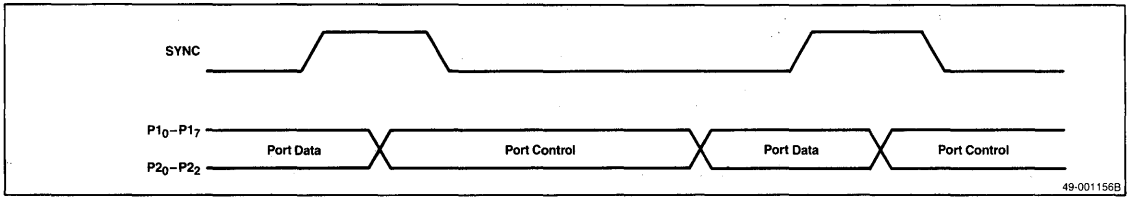
4

Timing Waveforms (cont)

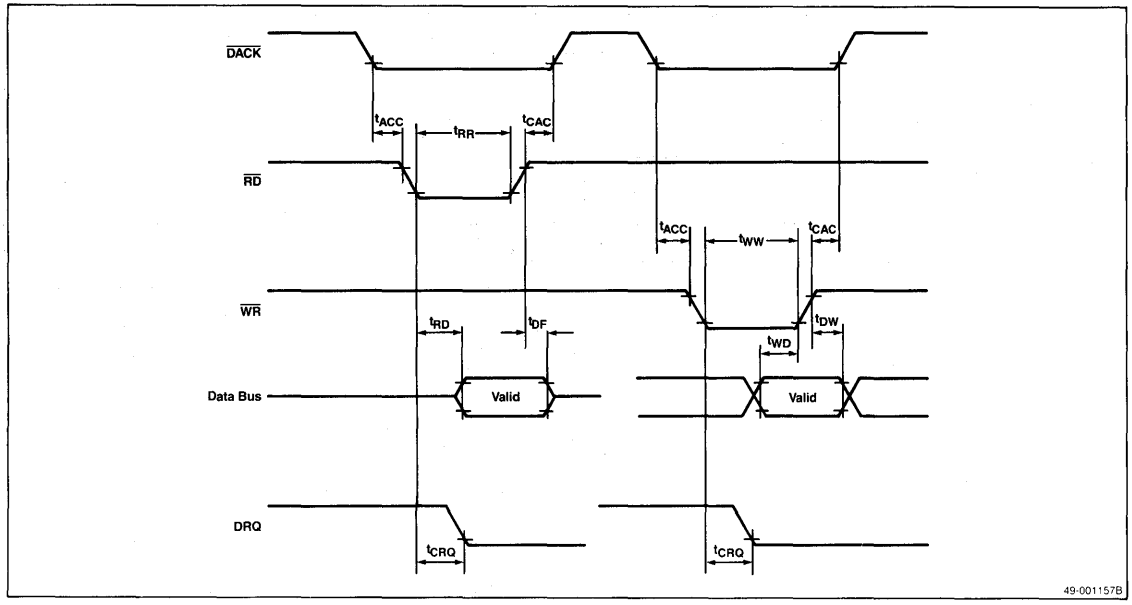
PORT2



PORT (EA = 1)



DMA

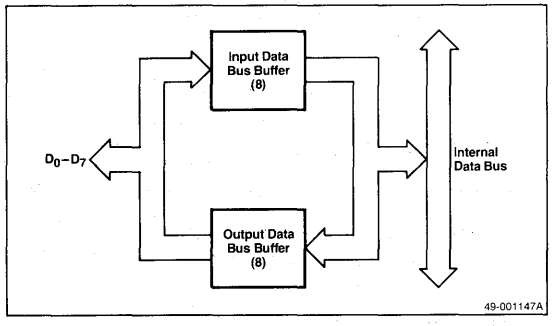


Functional Description

Data Bus Buffer In (DBBIN) and Data Bus Buffer Out (DBBOUT) Registers

As figure 1 shows, the DBBIN and DBBOUT registers transfer data to and from the master processors by way of the 8-bit external data bus (D_0-D_7) and the 8-bit internal data bus.

Figure 1. μPD80C42 Data Flow



Data Bus Buffer (DBB) Status Register

The μPD80C42 has an 8-bit status register (ST_0-ST_7) that contains information about the current status of the master or slave processor. The MOV STS, A instruction makes status bits ST_4-ST_7 user-definable by moving accumulator bits 4-1 to bits ST_4-ST_7 of the status register (ST_0-ST_3 are not affected). Bits ST_0-ST_3 give the status of the Output Buffer Full (OBF) and Input Buffer Full (IBF) bits, and flag bits (F0, F1). Figure 2 shows the status register format.

Figure 2. Status Register Format

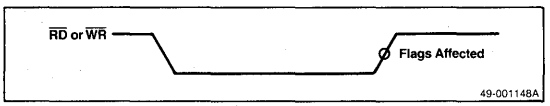
ST_7	ST_6	ST_5	ST_4	ST_3	ST_2	ST_1	ST_0
UD	UD	UD	UD	F1	F0	IBF	OBF

The MOV STS, A instruction is coded as follows:

1 0 0 1 0 0 0 0 90H

Figure 3 shows how ST_0-ST_3 change internally on the trailing-edge of $\overline{RD}$ or $\overline{WR}$ ($\overline{RD}$ and $\overline{WR}$ are edge-sensitive).

Figure 3. $\overline{RD}$ or $\overline{WR}$ Inputs



You can make ST_0 (OBF) and ST_1 (IBF) externally available in order to interrupt the master processor by executing the EN FLAGS instruction. When the EN FLAGS instruction is executed, $P2_4$ becomes the OBF pin. A 1 written to $P2_4$ enables OBF and outputs its status. A 0 written to $P2_4$ disables OBF by holding it low. Use OBF to indicate that valid data is available from the output data bus buffer register.

You can also use the EN FLAGS instruction to use $P2_5$ as the $\overline{IBF}$ pin. A 1 written to $P2_5$ enables $\overline{IBF}$ to output the inverse of the $\overline{IBF}$ status bit. A 0 written to $P2_5$ disables $\overline{IBF}$ by holding it low, making data at the data bus invalid.

The EN FLAGS instruction is coded as follows:

1 1 1 1 0 1 0 1 F5H

$P2_6$ and $P2_7$ are port pins or DMA handshake pins that allow a DMA interface. Use the EN DMA instruction to enable $P2_6$ and $P2_7$ as DRQ (DMA Request) and $\overline{DACK}$ (DMA Acknowledge), respectively. A 1 written to $P2_6$ activates DRQ, thus issuing a DMA request. Deactivate DRQ with the EN DMA instruction, $\overline{DACK}$ ANDed with $\overline{RD}$, or $\overline{DACK}$ ANDed with $\overline{WR}$. When EN DMA is executed, $P2_7$ ($\overline{DACK}$) functions as a chip select input for the data bus buffer registers during DMA transfers.

The EN DMA instruction is coded as follows:

1 1 1 0 0 1 0 1 E5H

HALT Mode

The HALT mode allows the μPD80C42 to conserve power during periods of inactivity. In the HALT mode, the oscillator remains active but the internal system clock stops. The HALT instruction allows the processor to enter the HALT mode.

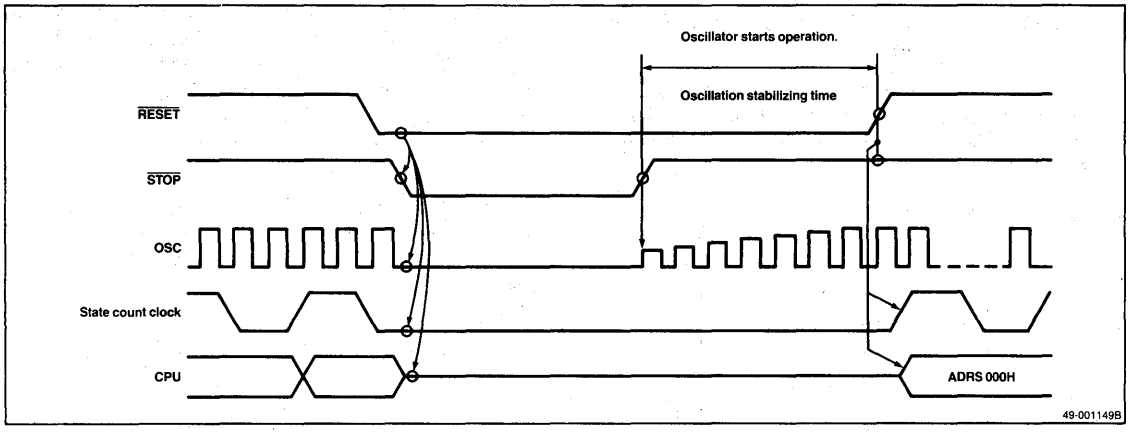
STOP Mode

The STOP mode disables the oscillator but maintains the contents of RAM. STOP mode conserves even more power than HALT mode. Enter STOP mode through software with the STOP instruction or through hardware with the $\overline{STOP}$ pin. In hardware STOP mode, the power supply voltage can drop as low as 2.0 V. In software STOP mode, it can drop as low as 2.5 V while still maintaining the RAM contents.

Control the STOP mode with hardware, with the $\overline{RESET}$ and $\overline{STOP}$ pins, as follows:

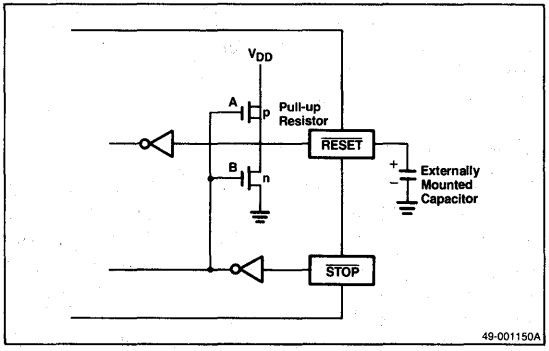
- Bring $\overline{RESET}$ low for at least six machine cycles, then bring $\overline{STOP}$ low. This assures proper termination of CPU operations. Figure 4 shows the timing for controlling STOP mode with hardware.

Figure 4. STOP Mode Control Timing



- Release hardware STOP mode by returning V_{CC} to +5 V ± 10%. After STOP goes high, hold RESET low long enough to allow the oscillator to stabilize. Figure 5 shows how to control oscillator settling time with the STOP pin by adding an external capacitor to the RESET line.
- Release the software STOP modes by applying a low level to the RESET pin to initiate oscillator operation. After sufficient oscillator stabilization time has passed, return RESET to a high level. Program execution will then begin at address 0.

Figure 5. STOP Mode Control Circuit



The following table shows the states of the output pins during both hardware and software STOP mode.

Table 1. Output Pins During STOP Mode

	State		
Output Pin	**STOPZ Instruction**	**STOPH Instruction**	**Hardware STOP**
$P1_0$–$P1_7$, $P2_0$–$P2_7$	High-Z	High level	High level
D_0–D_7	High-Z	High-Z	High-Z
PROG	High level	High level	High level
SYNC	Low level	Low level	Low level

Instruction Set

Mnemonic	Operation	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Accumulator												
ADD A, # data	(A), (C) ← (A) + data	Add immediate the specified data to the accumulator.(2)	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADD A, Rr	(A), (C) ← (A) + (Rr) r = 0–7	Add contents of designated register to the accumulator.(2)	0	1	1	0	1	r_2	r_1	r_0	1	1
ADD A, @ Rr	(A), (C) ← (A) + ((Rr)) r = 0–1	Add indirect the contents the data memory location to the accumulator.(2)	0	1	1	0	0	0	0	r_0	1	1
ADDC A, # data	(A), (C) ← (A) + (C) + data	Add immediate with carry the specified data to the accumulator.(2)	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ADDC A, Rr	(A), (C) ← (A) + (C) + (Rr) r = 0–7	Add with carry the contents of the designated register to the accumulator.(2)	0	1	1	1	1	r_2	r_1	r_0	1	1
ADDC A, @ Rr	(A), (C) ← (A) + (C) + ((Rr)) r = 0–1	Add indirect with carry the contents of data memory location to the accumulator.(2)	0	1	1	1	0	0	0	r_0	1	1
ANL A, # data	(A) ← (A) AND data	Logical AND specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ANL A, Rr	(A) ← (A) AND (Rr) r = 0–7	Logical AND contents of designated register with accumulator.	0	1	0	1	1	r_2	r_1	r_0	1	1
ANL A, @ Rr	(A) ← (A) AND ((Rr)) r = 0–1	Logical AND indirect the contents of data memory with accumulator.	0	1	0	1	0	0	0	r_0	1	1
CPL A	(A) ← NOT (A)	Complement the contents of the accumulator.	0	0	1	1	0	1	1	1	1	1
CLR A	(A) ← 0	Clear the contents of the accumulator.	0	0	1	0	0	1	1	1	1	1
DA A		Decimal adjust the contents of the accumulator.(2)	0	1	0	1	0	1	1	1	1	1
DEC A	(A) ← (A) – 1	Decrement by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
ORL A, Rr	(A) ← (A) OR (Rr); r = 0–7	Logical OR contents of designated register with accumulator.	0	1	0	0	1	r_2	r_1	r_0	1	1
ORL A, @ Rr	(A) ← (A) OR ((Rr)) r = 0–1	Logical OR indirect the contents of data memory location with accumulator.	0	1	0	0	0	0	0	r_0	1	1
RL A	$(A_{n+1}) \leftarrow (A_n)$, $(A_0) \leftarrow (A_7)$ n = 0–6	Rotate accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1
RLC A	$(A_{n+1}) \leftarrow (A_n)$, $(A_0) \leftarrow$ (C) (C) ← (A_7) n = 0–6	Rotate accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1
RR A	$(A_n) \leftarrow (A_{n+1})$, $(A_7) \leftarrow (A_0)$ n = 0–6	Rotate accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Accumulator (cont)												
RRC A	$(A_n) \leftarrow (A_{n+1})$, $(A_7) \leftarrow (C)$, $(C) \leftarrow (A_0)$ n = 0–6	Rotate accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1
SWAP A	$(A_7–A_4) \longleftrightarrow (A_3–A_0)$	Swap the 2 4-bit nibbles in the accumulator.	0	1	0	0	0	1	1	1	1	1
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
XRL A, Rr	(A) ← (A) XOR (Rr) r = 0–7	Logical XOR contents of designated register with accumulator.	1	1	0	1	1	r_2	r_1	r_0	1	1
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) r = 0–1	Logical XOR indirect the contents of data memory location with accumulator.	1	1	0	1	0	0	0	r_0	1	1
Branch												
DJNZ Rr, addr	(Rr) ← (Rr) – 1; If Rr ≠ 0; $(PC_7–PC_0) \leftarrow a_7–a_0$ r = 0–7	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r_2 a_2	r_1 a_1	r_0 a_0	2	2
JBb addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2
JC addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF0 addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JF1 addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JMP addr	$(PC_{10}–PC_8) \leftarrow (a_7–a_0)$	Direct jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
JMPP @ A	$(PC_7–PC_0) \leftarrow ((A))$	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1
JNC addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNIBF addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if IBF = 0 (PC) ← (PC) + 2 if IBF = 1	Jump to specified address if interrupt is low.	1 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT0 addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNT1 addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JNZ addr	$(PC_7–PC_0) \leftarrow a_7–a_0$ if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Branch (cont)												
JOBF addr	$(PC_7\text{-}PC_0) \leftarrow a_7\text{-}a_0$ if OBF = 1 $(PC) \leftarrow (PC) + 2$ if OBF = 0	Jump to specified address if output is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JTF addr	$(PC_7\text{-}PC_0) \leftarrow a_7\text{-}a_0$ if TF = 1 then reset TF $(PC) \leftarrow (PC) + 2$ if TF = 0	Jump to specified address if timer flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT0 addr	$(PC_7\text{-}PC_0) \leftarrow a_7\text{-}a_0$ if T0 = 1 $(PC) \leftarrow (PC) + 2$ if T0 = 0	Jump to specified address if test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JT1 addr	$(PC_7\text{-}PC_0) \leftarrow a_7\text{-}a_0$ if T1 = 1 $(PC) \leftarrow (PC) + 2$ if T1 = 0	Jump to specified address if test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
JZ addr	$(PC_7\text{-}PC_0) \leftarrow a_7\text{-}a_0$ if A = 0 $(PC) \leftarrow (PC) + 2$ if A = 1	Jump to specified address if accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2
Control												
EN I		Enable the interrupt.	0	0	0	0	0	1	0	1	1	1
DIS I		Disable the external interrupt input.	0	0	0	1	0	1	0	1	1	1
EN DMA		Enables DMA handshake lines.	1	1	1	0	0	1	0	1	1	1
EN Flags		Enables master interrupts.	1	1	1	1	0	1	0	1	1	1
SEL RB0	(BS) ← 0	Select bank 0 (locations 0–7) of data memory.	1	1	0	0	0	1	0	1	1	1
SEL RB1	(BS) ← 1	Select bank 1 (locations 24–31) of data memory.	1	1	0	1	0	1	0	1	1	1
HALT		Initiates halt mode.	0	0	0	0	0	0	0	1	1	1
STOP Z		Sets CPU to software stop mode. (Port output high impedance)	1	0	0	0	0	0	1	0	1	1
STOP H		Sets CPU to software stop mode. (Port output high level)	1	1	1	0	0	0	1	0	1	1
Data Moves												
MOV A, # data	(A) ← data	Move immediate the specified data into the accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2
MOV A, Rr	(A) ← (Rr); r = 0–7	Move the contents of the designated registers into the accumulator.	1	1	1	1	1	r_2	r_1	r_0	1	1
MOV A, @ Rr	(A) ← ((Rr)); r = 0–1	Move indirect the contents of data memory location into the accumulator.	1	1	1	1	0	0	0	r_0	1	1
MOV A, PSW	(A) ← (PSW)	Move contents of the program status word into the accumulator.	1	1	0	0	0	1	1	1	1	1
MOV Rr, # data	(Rr) ← data; r = 0–7	Move immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r_2 d_2	r_1 d_1	r_0 d_0	2	2
MOV Rr, A	(Rr) ← (A); r = 0–7	Move accumulator contents into the designated register.	1	0	1	0	1	r_2	r_1	r_0	1	1
MOV @ Rr, A	((Rr)) ← (A); r = 0–1	Move indirect accumulator contents into data memory location.	1	0	1	0	0	0	0	r_0	1	1
MOV @ Rr, # data	((Rr)) ← data; r = 0–1	Move immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r_0 d_0	2	2
MOV PSW, A	(PSW) ← (A)	Move contents of accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Data Moves (cont)												
MOVP A, @ A	A ← (PC_{10}–PC_8), (A))	Move data in the current page into the accumulator.	1	0	1	0	0	0	1	1	2	1
MOVP3 A, @ A	(A) ← ((011, A))	Move program data in page 3 into the accumulator.	1	1	1	0	0	0	1	1	2	1
XCH A, Rr	(A)←→ (Rr); r = 0–7	Exchange the accumulator and designated register's contents.	0	0	1	0	1	r_2	r_1	r_0	1	1
XCH A, @ Rr	(A)←→ ((Rr)); r = 0–1	Exchange indirect contents of accumulator and location in data memory.	0	0	1	0	0	0	0	r_0	1	1
XCHD A, @ Rr	(A_3–A_0)←→ (($Rr)_3$–$(Rr)_0$); r = 0–1	Exchange indirect 4-bit contents of accumulator and data memory.	0	0	1	1	0	0	0	r_0	1	1
Flags												
CPL C	(C) ← NOT (C)	Complement contents of carry bit.	1	0	1	0	0	1	1	1	1	1
CPL F0	(F0) ← NOT (F0)	Complement contents of flag F0.	1	0	0	1	0	1	0	1	1	1
CPL F1	(F1) ← NOT (F1)	Complement contents of flag F1.	1	0	1	1	0	1	0	1	1	1
CLR C	(C) ← 0	Clear contents of carry bit to 0.	1	0	0	1	0	1	1	1	1	1
CLR F0	(F0) ← 0	Clear contents of flag 0 to 0.	1	0	0	0	0	1	0	1	1	1
CLR F1	(F1) ← 0	Clear contents of flag 1 to 0.	1	0	1	0	0	1	0	1	1	1
Input / Output												
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1–2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p_1 d_1	p_0 d_0	2	2
ANLD Pp, A	(Pp) ← (Pp) AND (A_3–A_0); p = 4–7	Logical AND contents of accumulator with designated port (4–7).	1	0	0	1	1	1	p_1	p_0	2	1
IN A, DBB	(A) ← (DBBIN); IBF ← 0		0	0	1	0	0	0	1	0	1	1
IN A, Pp	(A) ← (Pp); p = 1–2	Input data from designated port (1–2) into accumulator.	0	0	0	0	1	0	p_1	p_2	2	1
MOVD A, Pp	(A_3–A_0) ← (Pp); (A_7–A_4) ← 0 p = 4–7	Move contents of designated port (4–7) into accumulator.	0	0	0	0	1	1	p_1	p_0	2	1
MOVD Pp, A	(Pp) ← (A_3–A_0); p = 4–7	Move contents of accumulator to designated port (4–7).	0	0	1	1	1	1	p_1	p_0	2	1
MOV STS, A	(ST_7–ST_4) ← (A_7–A_4)	Move contents of accumulator to designated port (4–7).	1	0	0	1	0	0	0	0	1	1

Instruction Set (cont)

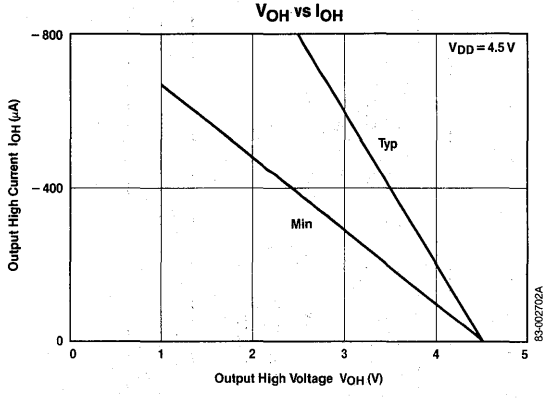
Mnemonic	Operation	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes
Input / Output (cont)												
ORLD Pp, A	(Pp) ← (Pp) OR (A_3–A_0); p = 4–7	Logical OR contents of accumulator with designated port (4–7).	1	0	0	0	1	1	p_1	p_0	2	1
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1–2	Logical OR immediate specified data with designated port (1–2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p_1 d_1	p_0 d_0	2	2
OUT DBB, A	(DBBOUT) ← (A), OBF ← 1		0	0	0	0	0	0	1	0	1	1
OUTL Pp, A	(Pp) ← (A); p = 1–2	Output contents of accumulator to designated port (1–2).	0	0	1	1	1	0	p_1	p_0	2	1
Registers												
DEC Rr	(Rr) ← (Rr) – 1; r = 0–7	Decrement by 1 contents of designated register.	1	1	0	0	1	r_2	r_1	r_0	1	1
INC Rr	(Rr) ← (Rr) + 1; r = 0–7	Increment by 1 contents of designated register.	0	0	0	1	1	r_2	r_1	r_0	1	1
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0–1	Increment indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r_0	1	1
Subroutine												
CALL addr	((SP)) ← (PC), (PSW_7–PSW_4) (SP) ← (SP) + 1 (PC_{10}–PC_0) ← a_{10}–a_0	Call designated subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from subroutine without restoring program status word.	1	0	0	0	0	0	1	1	2	1
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW_7–PSW_4) ← ((SP))	Return from subroutine restoring program status word.	1	0	0	1	0	0	1	1	2	1
Timer / Counter												
EN TCNTI		Enable internal interrupt flag for timer / counter output.	0	0	1	0	0	1	0	1	1	1
DIS TCNTI		Disable internal interrupt flag for timer / counter output.	0	0	1	1	0	1	0	1	1	1
MOV A, T	(A) ← (T)	Move contents of timer / counter into accumulator.	0	1	0	0	0	0	1	0	1	1
MOV T, A	(T) ← (A)	Move contents of accumulator into timer / counter.	0	1	1	0	0	0	1	0	1	1
STOP TCNT		Stop count for event counter.	0	1	1	0	0	1	0	1	1	1
STRT CNT		Start count for event counter.	0	1	0	0	0	1	0	1	1	1
STRT T		Start count for timer.	0	1	0	1	0	1	0	1	1	1
Miscellaneous												
NOP		No operation performed.	0	0	0	0	0	0	0	0	1	1

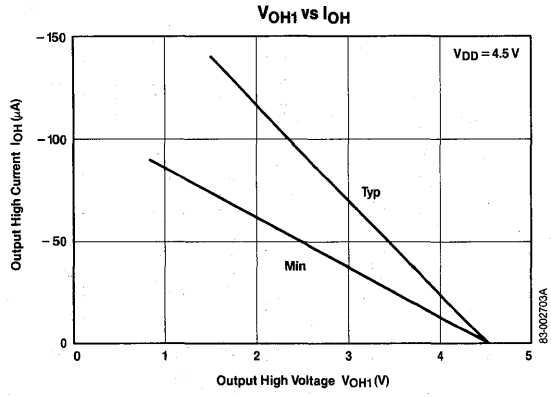
Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program memory address
b	Accumulator bit (b = 0–7)
C	Carry flag
CNT	Counter
data	8-bit data
DBB	Data bus buffer
F0, F1	Flags 0, 1 (C / D flag)
I	Interrupt
IBF	Input buffer full flag
OBF	Output buffer full flag
PC	Program counter
Pp	Port (p = 1–2 or 4–7)
PSW	Program status word
Rr	Register (r = 0–1 or r = 0–7)

Symbol	Description
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	TEST0, TEST1 pin
#	Immediate data
@	Indirect address
(x)	Contents of register X
((x))	Contents of memory addressed by X
←	Transfer direction, result
AND	Logical product (logical AND)
OR	Logical sum (logical OR)
XOR	Exclusive OR
———	Complement

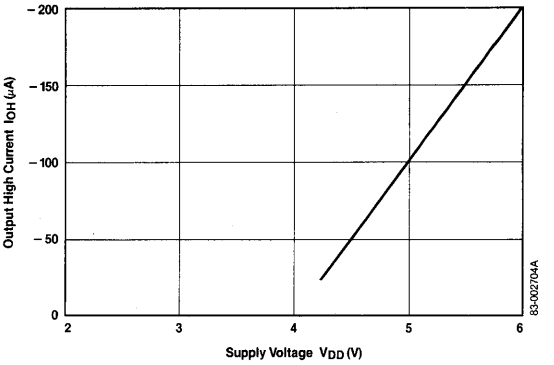
Operating Characteristics



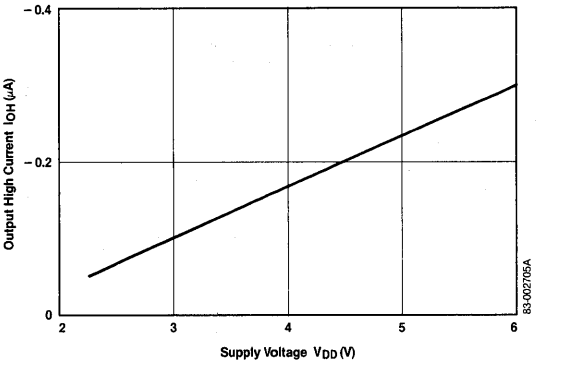


Operating Characteristics (cont)

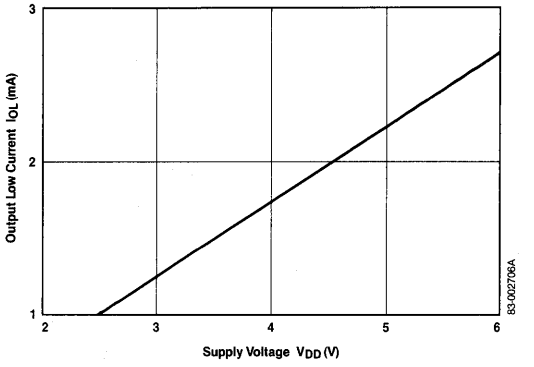
I_{OH} vs V_{DD} (V_{OH1} = 2.4 V)



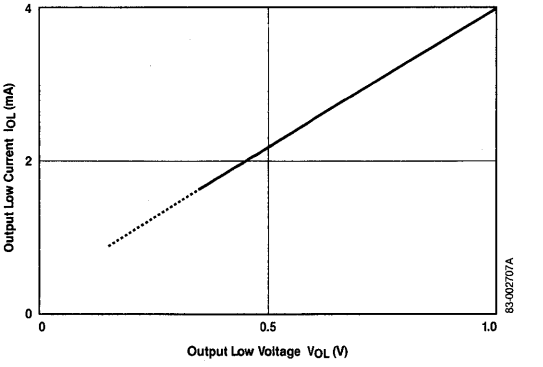
I_{OH} vs V_{DD} ($V_{OH2} = V_{DD} - 0.5$ V)



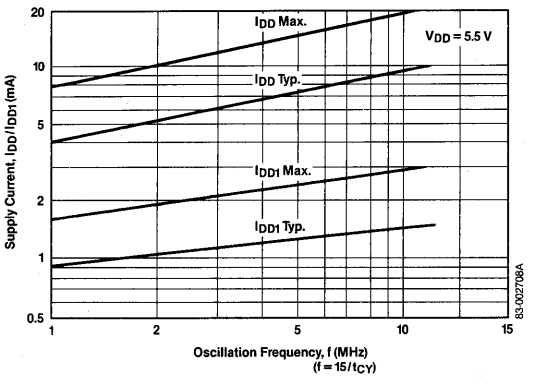
I_{OL} vs V_{DD} (V_{OL} = 0.45 V)



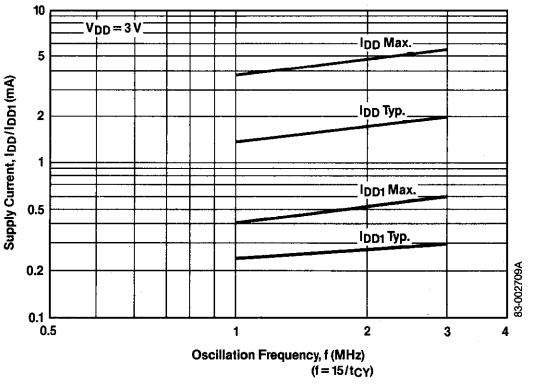
I_{OL} vs V_{DD} (V_{DD} = 4.5 V)



I_{DD}/I_{DD1} vs f(V_{DD} = 5.5 V)



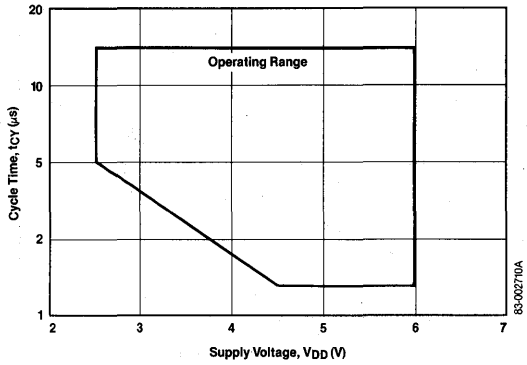
I_{DD}/I_{DD1} vs f(V_{DD} = 3 V)



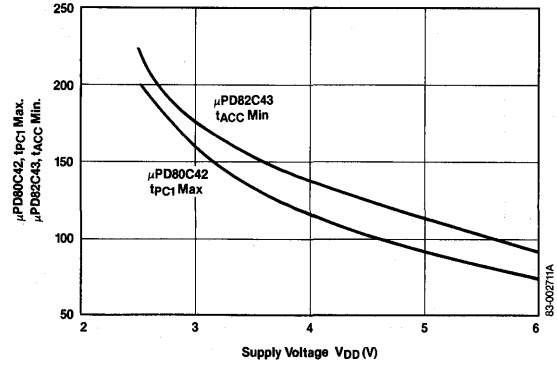
4

Operating Characteristics (cont)

t_{CY} vs V_{DD}



t_{PCI} Max (μPD80C42)/
t_{ACC} Min (μPD82C42) vs V_{DD}



NEC

NEC Electronics Inc.

μPD8748H
HIGH-SPEED, 8-BIT, SINGLE-CHIP NMOS MICROCOMPUTER WITH UV EPROM

Description

The μPD8748H is one of the μPD8048 family of single-chip 8-bit microcomputers. It is a high-speed NMOS processor that functions efficiently in control and arithmetic applications. The flexible instruction set allows you to directly set and reset individual data bits within the accumulator and the I/O ports. The variety of branch and table look-up instructions simplifies the implementation of standard logic functions.

The instruction set is made up of one- and two-byte instructions. Over 70% are single-byte instructions that require only one or two cycles. Over 50% require a single cycle.

The μPD8748H functions as a stand-alone microcomputer. You can expand its functions with standard 8080A/8085A peripherals and memories. It contains 1024 × 8 bits of ROM program memory, 64 × 8 bits of RAM data memory, 27 I/O lines, an 8-bit internal timer/event counter, oscillator, and clock circuitry.

The μPD8748H differs from the μPD8048 in that it has 1K of on-board EPROM. This is useful in preproduction or prototype applications where the software is not complete or in system designs in quantities that do not require a mask ROM. See the μPD8048H/8035HL data sheet for more information.

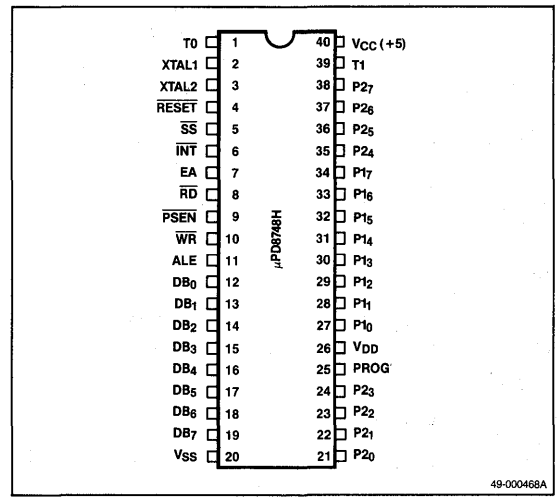
Features

- ☐ Low programming voltage
- ☐ Fully compatible with 8048/8748/8035
- ☐ NMOS silicon gate technology
- ☐ Single +5V supply
- ☐ 2.5μs cycle time
- ☐ 96 instructions; 70% single byte
- ☐ Internal timer/event counter
- ☐ 64 × 8 byte RAM data memory
- ☐ Single interrupt level
- ☐ 27 I/O lines
- ☐ Internal clock generator
- ☐ 8-level stack
- ☐ Compatible with 8080A/8085A peripherals
- ☐ Available in one-time-programmable plastic package

Ordering Information

Part Number	Package Type	Max Freq. of Operation
μPD8748HC	40-Pin plastic DIP	11 MHz
μPD8748HD	40-Pin cerdip with quartz window	11 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1, 39	T0, T1	Testable inputs 0 and 1
2, 3	XTAL1, XTAL2	Crystal inputs
4	$\overline{RESET}$	System reset input
5	$\overline{SS}$	Single step input
6	$\overline{INT}$	Interrupt input
7	EA	External access input
8	$\overline{RD}$	Read strobe output
9	$\overline{PSEN}$	Program store enable output
10	$\overline{WR}$	Write strobe output
11	ALE	Address latch enable output
12-19	D_0-D_7	8-bit bidirectional port
20	V_{SS}	Ground
21-24, 35-38	$P2_0$-$P2_7$	8-bit quasibidirectional port 2
25	PROG	Program pulse input
26	V_{DD}	Programming power supply
27-34	$P1_0$-$P1_7$	8-bit quasibidirectional port 1
40	V_{CC}	Primary power supply

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Pin Functions

T0, T1 (Testable inputs 0 and 1)

T0 uses the conditional transfer functions JT0 and JNT0; T1 uses JT1 and JNT1. The ENT0 CLK instruction allows T0 to use the internal state clock (CLK). Use the STRT CNT instruction to use T1 as the timer/counter. During programming, you can use T0 as a testable flag.

XTAL1, XTAL2 (Crystal inputs)

XTAL1 and XTAL2 are two sides of the crystal input for an external oscillator or frequency (non-TTL compatible V_{IH}).

$\overline{\text{RESET}}$ (Reset)

Active low input for processor initialization. $\overline{\text{RESET}}$ is also used for PROM programming verification and power down (non-TTL compatible V_{IH}).

$\overline{\text{SS}}$ (Single step)

Active low single step input. $\overline{\text{SS}}$ and ALE allow the processor to single step through each instruction in program memory.

$\overline{\text{INT}}$ (Interrupt)

Active low interrupt input. $\overline{\text{INT}}$ starts an interrupt if an enable interrupt instruction has been executed. $\overline{\text{RESET}}$ disables the interrupt. You can test $\overline{\text{INT}}$ with a conditional jump instruction.

EA (External access)

A logic 1 at the EA input tells the processor to perform all program memory fetches from external memory.

$\overline{\text{RD}}$ (Read strobe)

Active low read strobe output. $\overline{\text{RD}}$ pulses low when the processor performs a bus read. $\overline{\text{RD}}$ also enables data onto the processor bus from a peripheral device and functions as a read strobe for external data memory.

$\overline{\text{PSEN}}$ (Program store enable)

Active low program store enable output. $\overline{\text{PSEN}}$ becomes active only during external memory fetches.

$\overline{\text{WR}}$ (Write strobe)

Acitve low write strobe output. $\overline{\text{WR}}$ pulses low when the processor performs a bus write. $\overline{\text{WR}}$ also functions as a write strobe for external data memory.

ALE (Address latch enable)

Once each cycle, the falling edge of ALE latches the address for external memory or peripherals. You can also use ALE as a clock output.

D_0-D_7 (8-bit bidirectional bus)

The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ strobes allow you to perform synchronous reads and writes on this port. The contents of D_0-D_7 can be latched in static mode. During an external memory fetch, D_0-D_7 holds the LSBs of the program counter. $\overline{\text{PSEN}}$ controls the incoming addressed instruction. D_0-D_7 also holds address and data information for external RAM data store instruction (controlled by ALE, $\overline{\text{RD}}$, and $\overline{\text{WR}}$).

V_{SS} (Ground)

Ground.

$P2_0$-$P2_7$ (Port 2)

Port 2 is one of two 8-bit quasibidirectional ports. $P2_0$-$P2_3$ hold the four MSBs of the program counter for external data memory fetches; $P2_4$-$P2_7$ hold data. $P2_0$-$P2_3$ are also used as a 4-bit I/O bus for the μPD8243 I/O expander.

PROG (Program pulse)

Apply a +18 V pulse to the PROG input to program the μPD8748H. You can also use PROG as an output strobe for the μPD8243.

V_{DD} (Programming power supply)

V_{DD} must be +21 V to program the μPD8748H or +5 V for the ROM and PROM versions for normal operation.

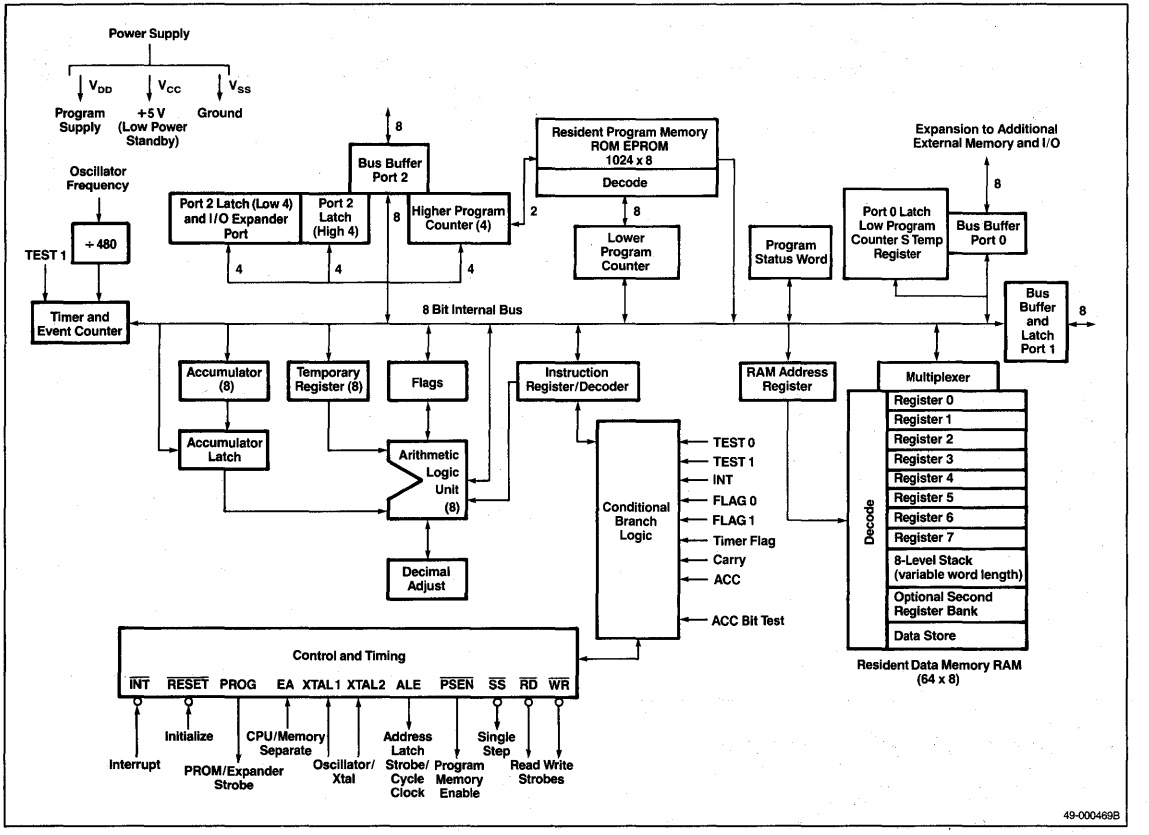
$P1_0$-$P1_7$ (Port 1)

Port 1 is one of two 8-bit quasibidirectional ports used for external data memory fetches.

V_{CC} (Power supply)

V_{CC} must be +5 V to program and operate the μPD8748H.

Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Operating temperature, T_{OP}	0°C to +70°C
Storage temperature, T_{ST}	−65°C to +150°C
Output voltage, V_O	−0.5 V to +7.0 V
Input voltage, V_I	−0.5 V to +7.0 V
Power supply voltages, V_{CC}, V_{DD}	−0.5 V to +7.0 V

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input low voltage (except XTAL1, XTAL2, RESET)	V_{IL}	−0.5		0.8	V	
Input low voltage (XTAL1, XTAL2, RESET)	V_{IL1}	−0.5		0.6	V	
Input high voltage (except XTAL1, XTAL2, RESET)	V_{IH}	2.0		V_{CC}	V	
Input high voltage (XTAL1, XTAL2, RESET)	V_{IH1}	3.8		V_{CC}	V	
Output low voltage (Bus)	V_{OL}			0.45	V	$I_{OL} = 2.0$ mA
Output low voltage (RD, WR, PSEN, ALE)	V_{OL1}			0.45	V	$I_{OL} = 1.8$ mA

DC Characteristics (cont)

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Output low voltage (PROG)	V_{OL2}			0.45	V	$I_{OL} = 1.0$ mA
Output low voltage (all other outputs)	V_{OL3}			0.45	V	$I_{OL} = 1.6$ mA
Output high voltage (Bus)	V_{OH}	2.4			V	$I_{OH} = -400\,\mu A$
Output high voltage ($\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH1}	2.4			V	$I_{OH} = -100\,\mu A$
Output high voltage (all other outputs)	V_{OH2}	2.4			V	$I_{OH} = -40\,\mu A$
Input leakage current (T1, $\overline{INT}$)	I_{LI}			±10	μA	$V_{SS} \leq V_I \leq V_{CC}$
Input leakage current ($P1_0$–$P1_7$, $P2_0$–$P2_7$, EA, $\overline{SS}$)	I_{LI1}			−500	μA	$V_{SS} + 0.45\,V \leq V_I \leq V_{CC}$
Output leakage current (Bus, T0, high impedance)	I_{LO}			±10	μA	$V_{SS} + 0.45\,V \leq V_I \leq V_{CC}$
Supply current (V_{DD})	I_{DD}	2		5	mA	
Total supply current	$I_{DD} + I_{CC}$	85		110	mA	

Programming DC Characteristics

$T_A = 25°C \pm 5°C$, $V_{CC} = +5V \pm 5\%$, $V_{DD} = +21V \pm 0.5V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
V_{DD} voltage high level	V_{DDH}	20.5		21.5	V	
V_{DD} voltage low level	V_{DDL}	4.75		5.25	V	
PROG voltage high level	V_{PH}	17.5		18.5	V	
PROG voltage low level	V_{PL}	4.0		V_{CC}	V	
EA program / verify voltage high level	V_{EAH}	17.5		18.5	V	
V_{DD} high voltage supply current	I_{DD}			20.0	mA	
PROG high voltage supply current	I_{PROG}			1.0	mA	
EA high voltage supply current	I_{EA}			1.0	mA	

AC Characteristics

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5V \pm 10\%$, $V_{SS} = 0V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Read, Write, and Instruction Fetch — External Data and Program Memory						
ALE pulse width	t_{LL}	150			ns	(1, 3)
Address setup before ALE	t_{AL}	70			ns	(1, 3)
Address hold after ALE	t_{LA}	50			ns	(1, 3)
Control pulse width ($\overline{RD}$, $\overline{WR}$)	t_{CC1}	480			ns	(1, 3)
Control pulse width ($\overline{PSEN}$)	t_{CC2}	350			ns	(1, 3)
Data setup before $\overline{WR}$	t_{DW}	390			ns	(1, 3)
Data hold after $\overline{WR}$	t_{WD}	40			ns	(1, 2, 3)
Cycle time	t_{CY}	1.36		15.0	μs	
Data hold after $\overline{RD}$, $\overline{PSEN}$	t_{DR}	0		110	ns	(1, 3)
$\overline{RD}$ to data in	t_{RD1}			330	ns	(1, 3)
$\overline{PSEN}$ to data in	t_{RD2}			190	ns	(1, 3)
Address setup before $\overline{WR}$	t_{AW}	300			ns	(1, 3)
Address setup before data in ($\overline{RD}$)	t_{AD1}			730	ns	(1, 3)
Address setup before data in ($\overline{PSEN}$)	t_{AD2}			460	ns	(1, 3)
Address float to $\overline{RD}$, $\overline{WR}$	t_{AFC1}	140			ns	(1, 3)
Address float to $\overline{PSEN}$	t_{AFC2}	10			ns	(1, 3)
ALE to $\overline{RD}$, $\overline{WR}$ delay time	t_{LAFC1}	200			ns	(1, 3)
ALE to $\overline{PSEN}$ delay time	t_{LAFC2}	60			ns	(1, 3)
$\overline{RD}$, $\overline{WR}$, PROG to ALE delay time	t_{CA1}	50			ns	(1, 3)
$\overline{PSEN}$ to ALE delay time	t_{CA2}	320			ns	(1, 3)

Note:
(1) Control Output: $C_L = 80$ pF, Bus Output: $C_L = 150$ pF
(2) Bus high impedance, load = 20 pF
(3) Clock oscillation frequency, $f_{OSC} = 11$ MHz

AC Characteristics (cont)

$T_A = 0°C$ to $+70°C$, $V_{CC} = V_{DD} = +5\,V \pm 10\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Port 2 Timing						
Port control setup before PROG	t_{CP}	100			ns	(1, 3)
Port control hold after PROG	t_{PC}	160			ns	(1, 3)
Input data setup before PROG	t_{PR}			650	ns	(1, 3)
Input data hold after PROG	t_{PF}	0		140	ns	(1, 3)
Output data setup before PROG	t_{DP}	400			ns	(1, 3)
Output data hold after PROG	t_{PD}	90			ns	(1, 3)
PROG pulse width	t_{PP}	700			ns	(1, 3)
Port 2 I/O data setup before ALE	t_{PL}	160			ns	(1, 3)
Port 2 I/O data setup after ALE	t_{LP}	15			ns	(1, 3)
ALE to port output time	t_{PV}			510	ns	(1, 3)
T0 output cycle time	t_{OPRR}	270			ns	(1, 3)

Note:
(1) Control output: $C_L = 80\,pF$, bus output: $C_L = 150\,pF$
(2) Bus high impedance, load = 20 pF
(3) Clock oscillation frequency, $f_{OSC} = 11\,MHz$

Programming AC Characteristics

$T_A = 25°C \pm 5°$, $V_{DD} = +21\,V \pm 0.5\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Address setup before $\overline{RESET}\uparrow$	t_{AW}	$4\,t_{CY}$				
Address hold after $\overline{RESET}\uparrow$	t_{WA}	$4\,t_{CY}$				
Data Input setup before PROG↓	t_{DW}	$4\,t_{CY}$				
Data input hold after PROG↓	t_{WD}	$4\,t_{CY}$				
$\overline{RESET}$ hold after verify	t_{PH}	$4\,t_{CY}$				
V_{DD} setup before PROG↑	t_{VDDW}	0		1.0	ms	
V_{DD} hold after PROG↓	t_{VDDH}	0		1.0	ms	
PROG pulse width	t_{PW}	50		60	ms	
TEST0 setup before program mode	t_{TW}	$4\,t_{CY}$				
TEST0 hold after program mode	t_{WT}	$4\,t_{CY}$				

Programming AC Characteristics (cont)

$T_A = 25°C \pm 5°$, $V_{DD} = +21\,V \pm 0.5\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
TEST0 to data output delay(1)	t_{DO}			$4\,t_{CY}$		
$\overline{RESET}$ pulse width to latch address	t_{WW}	$4\,t_{CY}$				
V_{DD} and PROG rise and fall times	t_r, t_f	0.5		100	μs	
CPU cycle time	t_{CY}	4.0		15	μs	4.0 μs / 3.7 MHz
$\overline{RESET}$ setup before EA↑	t_{RE}	$4\,t_{CY}$				

Note:
(1) If TEST0 is high, t_{DO} is triggered by $\overline{RESET}\uparrow$.

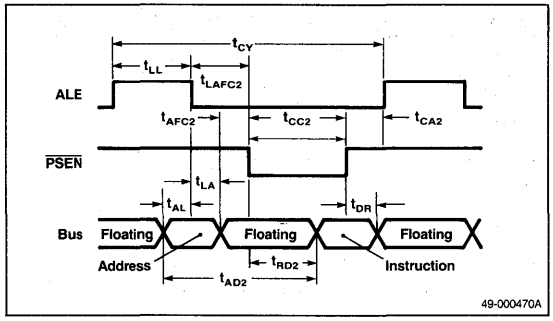
Bus Timing Requirements

Symbol	Timing Formula	Min/Max	Unit
t_{LL}	$(7/30)\,t_{CY} - 170$	Min	ns
t_{AL}	$(2/15)\,t_{CY} - 110$	Min	ns
t_{LA}	$(1/15)\,t_{CY} - 40$	Min	ns
t_{CC1}	$(1/2)\,t_{CY} - 200$	Min	ns
t_{CC2}	$(2/5)\,t_{CY} - 200$	Min	ns
t_{DW}	$(13/30)\,t_{CY} - 200$	Min	ns
t_{WD}	$(1/15)\,t_{CY} - 50$	Min	ns
t_{DR}	$(1/10)\,t_{CY} - 30$	Max	ns
t_{RD1}	$(11/13)\,t_{CY} - 170$	Max	ns
t_{RD2}	$(4/15)\,t_{CY} - 170$	Max	ns
t_{AW}	$(1/3)\,t_{CY} - 150$	Min	ns
t_{AD1}	$(7/10)\,t_{CY} - 220$	Max	ns
t_{AD2}	$(1/2)\,t_{CY} - 220$	Max	ns
t_{AFC1}	$(2/15)\,t_{CY} - 40$	Min	ns
t_{AFC2}	$(1/30)\,t_{CY} - 40$	Min	ns
t_{LAFC1}	$(1/5)\,t_{CY} - 75$	Min	ns
t_{LAFC2}	$(1/10)\,t_{CY} - 75$	Min	ns
t_{CA1}	$(1/15)\,t_{CY} - 40$	Min	ns
t_{CA2}	$(4/15)\,t_{CY} - 40$	Min	ns
t_{CP}	$(2/15)\,t_{CY} - 80$	Min	ns
t_{PC}	$(4/15)\,t_{CY} - 200$	Min	ns
t_{PR}	$(17/30)\,t_{CY} - 120$	Max	ns
t_{PF}	$(1/10)\,t_{CY}$	Max	ns
t_{DP}	$(2/5)\,t_{CY} - 150$	Min	ns
t_{PD}	$(1/10)\,t_{CY} - 50$	Min	ns
t_{PP}	$(7/10)\,t_{CY} - 250$	Min	ns
t_{PL}	$(4/15)\,t_{CY} - 200$	Min	ns
t_{LP}	$(1/30)\,t_{CY} - 30$	Min	ns
t_{PV}	$(3/10)\,t_{CY} + 100$	Max	ns
t_{OPRR}	$(1/5)\,t_{CY}$	Min	ns
t_{CY}	$(1/f_{OSC}) \times 15$		μs

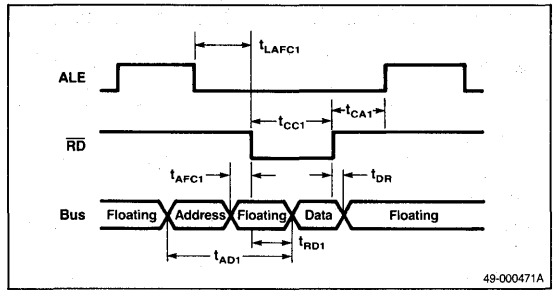
4

Timing Waveforms

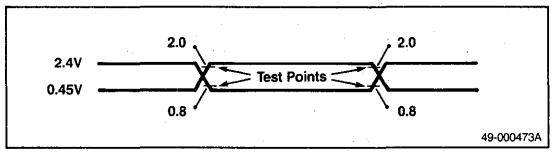
Instruction Fetch (External Program Memory)



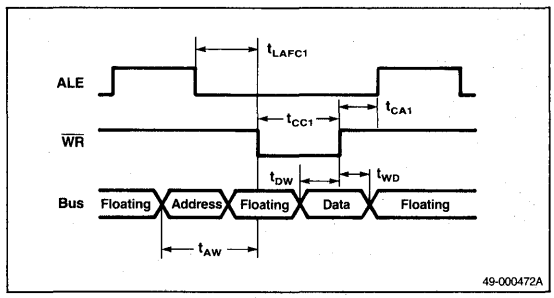
Read (External Data Memory)



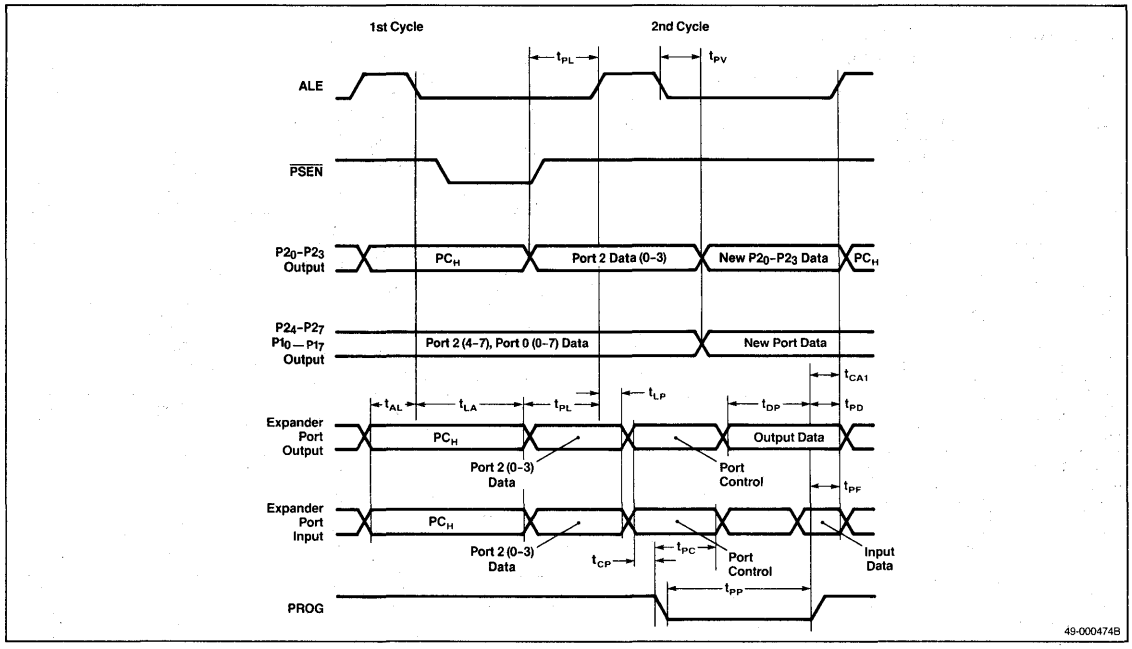
AC Test I/O Waveform



Write (External Data Memory)

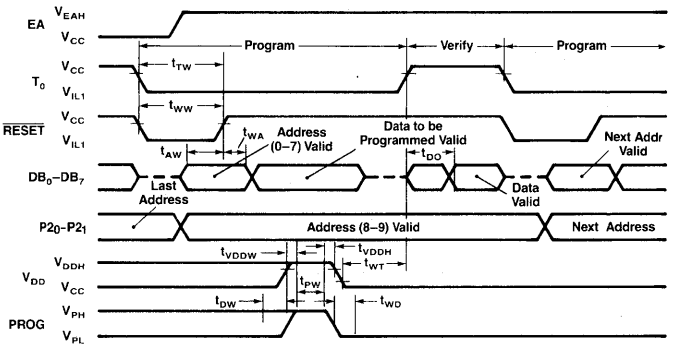


Port 1/Port 2



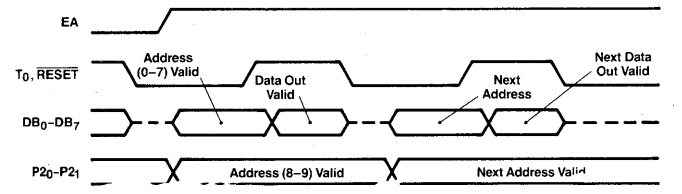
Timing Waveforms (cont)

Program/Verify



49-000475B

Verify



Note:

1. When EA is "low" or TO = 5 V, PROG should be in floating conditon [≠18 V].

2. t_{CY} 4 μs can be achieved using 3.7 MHz frequency at the XAL1 and XTAL2.

49-000476B

Instruction Set

Mnemonic	Operation	Description	Operation Code								Cycles	Bytes	Flags			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
Accumulator																
ADD A, # data	(A) ← (A) + data	Add immediate the specified data to the accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0–7	Add contents of designated register to the accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0–1	Add indirect the contents of the data memory location to the accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, # data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0–7	Add with carry the contents of the designated register to the accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0–1	Add indirect with carry the contents of data memory location to the accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, # data	(A) ← (A) AND data	Logical AND specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0–7	Logical AND contents of designated register with accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0–1	Logical AND indirect the contents of data memory with accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	Clear the contents of the accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		Decimal adjust the contents of the accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) – 1	Decrement by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, # data	(A) ← (A) OR data	Logical OR specified immediate data with accumulator.	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0–7	Logical OR contents of designated register with accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0–1	Logical OR indirect the contents of data memory location with accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	$(A_{N+1}) \leftarrow (A_N)$; N = 0–6 $(A_0) \leftarrow (A_7)$	Rotate accumulator left by 1 bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	$(A_{N+1}) \leftarrow (A_N)$; N = 0–6 $(A_0) \leftarrow$ (C) (C) ← (A_7)	Rotate accumulator left by 1 bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	$(A_N) \leftarrow (A_{N+1})$; N = 0–6 $(A_7) \leftarrow (A_0)$	Rotate accumulator right by 1 bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	$(A_N) \leftarrow (A_{N+1})$; N = 0–6 $(A_7) \leftarrow$ (C) (C) ← (A_0)	Rotate accumulator right by 1 bit through carry.	0	1	1	0	0	1	1	1	1	1	•			

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code								Cycles	Bytes	Flags			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
Accumulator (cont)																
SWAP A	$(A_4–A_7) \leftrightarrow (A_0–A_3)$	Swap the 2 4-bit nibbles in the accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, # data	(A) ← (A) XOR data	Logical XOR specified immediate data with accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0–7	Logical XOR contents of designated register with accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0–1	Logical XOR Indirect the contents of data memory location with accumulator.	1	1	0	1	0	0	0	r	1	1				
Branch																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0–7 If (Rr) ≠ 0; $(PC_0–PC_7)$ ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	$(PC_0–PC_7)$ ← addr if $B_b = 1$ (PC) ← (PC) + 2 if $B_b = 0$	Jump to specified address if accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	$(PC_0–PC_7)$ ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	$(PC_0–PC_7)$ ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	$(PC_0–PC_7)$ ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	$(PC_8–PC_{10}) \leftarrow (addr_8–addr_{10})$ $(PC_0–PC_7) \leftarrow (addr_0–addr_7)$ (PC_{11}) ← DBF	Direct jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	$(PC_0–PC_7)$ ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	$(PC_0–PC_7)$ ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	$(PC_0–PC_7)$ ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT0 addr	$(PC_0–PC_7)$ ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	$(PC_0–PC_7)$ ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	$(PC_0–PC_7)$ ← addr if A = 0 (PC) ← (PC) + 2 if A = 1	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	$(PC_0–PC_7)$ ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if timer flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	$(PC_0–PC_7)$ ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	$(PC_0–PC_7)$ ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code								Cycles	Bytes	Flags			
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0			C	AC	F0	F1
Branch (cont)																
JZ addr	(PC_0–PC_7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 1	Jump to specified address if accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
Control																
EN I		Enable the external interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the external interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the clock output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select bank 0 (locations 0–2047) of program memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select bank 1 (locations 2048–4095) of program memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select bank 0 (locations 0–7) of data memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select bank 1 (locations 24–31) of data memory.	1	1	0	1	0	1	0	1	1	1				
Data Moves																
MOV A, # data	(A) ← data	Move immediate the specified data into the accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0–7	Move the contents of the designated registers into the accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0–1	Move indirect the contents of data memory location into the accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the program status word into the accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, # data	(Rr) ← data; r = 0–7	Move immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0–7	Move accumulator contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0–1	Move indirect accumulator contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, # data	((Rr)) ← data; r = 0–1	Move immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	1 d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC_0–PC_7) ← (A) (A) ← ((PC))	Move data in the current page into the accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC_0–PC_7) ← (A) (PC_8–PC_{10}) ← 011 (A) ← ((PC))	Move program data in page 3 into the accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0–1	Move indirect the contents of external data memory into the accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0–1	Move indirect the contents of the accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ↔ (Rr); r = 0–7	Exchange the accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Data Moves (cont)																
XCH A, @ Rr	(A) ↔ ((Rr)); r = 0–1	Exchange indirect contents of accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	$(A_0–A_3)$ ↔ $((Rr))_0–((Rr))_3$; r = 0–1	Exchange indirect 4-bit contents of accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
Flags																
CPL C	(C) ← NOT (C)	Complement contents of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement contents of flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement contents of flag F1.	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear contents of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear contents of flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear contents of flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•
Input / Output																
ANL BUS, # data	(bus) ← (bus) AND data	Logical AND immediate specified data with contents of bus.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1–2	Logical AND immediate specified data with designated port (1 or 2).	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND $(A_0–A_3)$; p = 4–7	Logical AND contents of accumulator with designated port (4–7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1–2	Input data from designated port (1–2) into accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (bus)	Input strobed bus data into accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	$(A_0–A_3)$ ← (Pp); p = 4–7 $(A_4–A_7)$ ← 0	Move contents of designated port (4–7) into accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← $(A_0–A_3)$; p = 4–7	Move contents of accumulator to designated port (4–7).	0	0	1	1	1	1	p	p	2	1				
ORL BUS, # data	(bus) ← (bus) OR data	Logical OR immediate specified data with contents of bus.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR $(A_0–A_3)$; p = 4–7	Logical OR contents of accumulator with designated port (4–7).	1	0	0	0	1	1	p	p	2	1				
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1–2	Logical OR immediate specified data with designated port (1–2).	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(bus) ← (A)	Output contents of accumulator onto bus.	0	0	0	0	0	0	1	0	2	1				
OUTL Pp,A	(Pp) ← (A); p = 1–2	Output contents of accumulator to designated port (1–2).	0	0	1	1	1	0	p	p	2	1				
Registers																
DEC Rr (Rr)	(Rr) ← (Rr) + 1; r = 0–7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) = 1; r = 0–7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) = 1; r = 0–1	Increment indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				

Instruction Set (cont)

Mnemonic	Operation	Description	Operation Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Cycles	Bytes	Flags C	AC	F0	F1
Subroutine																
CALL addr	((SP)) ← (PC) (PSW_4–PSW_7), (SP) ← (SP) + 1 (PC_8–PC_{10}) ← ($addr_8$–$addr_{10}$) (PC_0–PC_7) ← ($addr_0$–$addr_7$) (PC_{11}) ← DBF	Call designated subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) = 1 (PC) ← ((SP))	Return from subroutine without restoring program status word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) = 1 (PC) ← ((SP)) (PSW_4–PSW_7) ← ((SP))	Return from subroutine restoring program status word.	1	0	0	1	0	0	1	1	2	1				
Timer / Counter																
EN TCNTI		Enable internal interrupt flag for timer / counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable internal interrupt flag for timer / counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of timer / counter into accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of accumulator into timer / counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop count for event counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start count for event counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start count for timer.	0	1	0	1	0	1	0	1	1	1				
Miscellaneous																
NOP		No operation performed.	0	0	0	0	0	0	0	0	1	1				

Note:

(1) Instruction code designations r and p form the binary representation of the registers and ports involved.

(2) The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

(3) References to the address and data are specified in bytes 2 and/or 1 of the instruction.

(4) Numerical subscripts appearing in the function column reference the specific bits affected.

Instruction Set Symbol Definitions

Symbol	Description
A	Accumulator
AC	Auxiliary carry flag
addr	Program memory address (12 bits)
B_b	Bit designator (b = 0–7)
BS	Bank switch
BUS	Bus port
C	Carry flag
CLK	Clock signal
CNT	Event counter
D	Nibble designator (4 bits)
data	Number or expression (8 bits)
DBF	Memory bank flip-flop
F0, F1	Flags 0, 1
I	Interrupt
P	"In-page" operation designator

Symbol	Description
Pp	Port designator (p = 1, 2 or 4–7)
PSW	Program status word
Rr	Register designator (r = 0, 1 or 0–7)
SP	Stack pointer
T	Timer
TF	Timer flag
T0, T1	Testable flags 0, 1
X	External RAM
#	Prefix for immediate data
@	Prefix for indirect address
$	Program counter's current value
(x)	Contents of external RAM location
((x))	Contents of memory location addressed by the contents of external RAM location
←	Replaced by

16-BIT, SINGLE-CHIP MICROCOMPUTERS

Section 5 — 16-Bit, Single-Chip Microcomputers

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NEC

NEC Electronics Inc.

μPD70320/322 (V25™) 16-BIT, SINGLE-CHIP CMOS MICROCOMPUTERS

PRELIMINARY INFORMATION

Description

The μPD70320 and μPD70322 (V25™) are high-performance, 16-bit, single-chip microcomputers with an 8-bit external data bus. They combine the instruction set of the μPD70108 (V20™) with many of the on-chip peripherals in NEC's 78000 series.

The μPD70320/322 processor has software compatibility with the V20 (and subsequently the 8086/8088), faster memory accessing, superior interrupt processing ability, and enhanced control of internal peripherals.

A variety of on-chip components, including 16K bytes of mask programmable ROM (μPD70322 only), 256 bytes of RAM, serial and parallel I/O, comparator port lines, timers, and a DMA controller make the μPD70320/322 a sophisticated microsystem.

Eight banks of registers are mapped into internal RAM below an additional 256-byte special function register (SFR) area that is used to control on-chip peripherals. Internal RAM and the SFR area are together relocatable to anywhere in the 1M-byte address space. This maintains compatibility with existing system memory maps.

The μPD70322 is the mask ROM version and the μPD70320 is the ROM-less version.

Features

- ☐ Complete single-chip microcomputer
  - — 16-bit ALU
  - — 16K bytes of ROM (μPD70322)
  - — 256 bytes of RAM
- ☐ Four-byte instruction prefetch queue
- ☐ 24 parallel I/O lines
- ☐ Eight analog comparator inputs with programmable threshold level
- ☐ Two independent DMA channels
- ☐ Two 16-bit timers
- ☐ Programmable time base counter
- ☐ Two full-duplex UARTs
- ☐ Programmable interrupt controller
  - — Eight priority levels
  - — Five external, 12 internal sources
  - — Register bank (eight) context switching
  - — Eight macro service function channels
- ☐ DRAM refresh pulse output
- ☐ Two standby modes
  - — HALT
  - — STOP
- ☐ Internal clock generator
  - — 5-MHz maximum frequency (0.4-μs instruction cycle time) (target specification: 8 MHz)
- ☐ Programmable wait state generation
- ☐ Separate address/data bus interface
- ☐ CMOS technology

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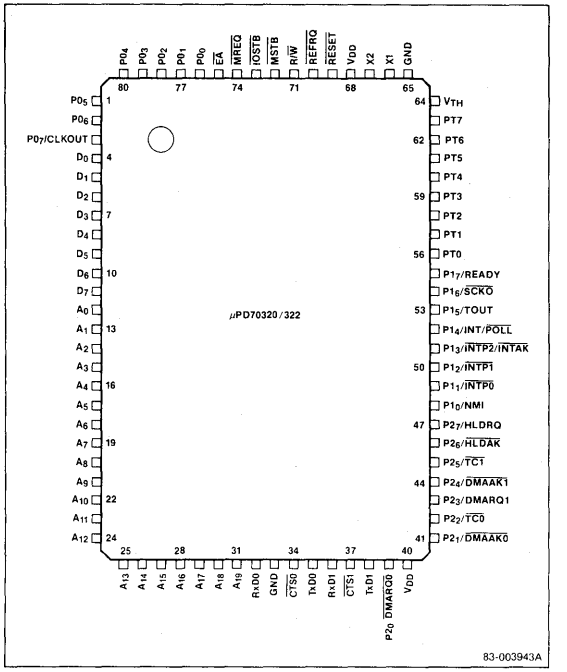
Ordering Information

Part Number	Package Type
μPD70320G-12	80-pin plastic miniflat
μPD70322G-12	80-pin plastic miniflat
μPD70320L	84-pin PLCC (plastic leadled chip carrier)
μPD70322L	84-pin PLCC (plastic leadled chip carrier)

Pin Configurations

80-Pin Plastic Miniflat



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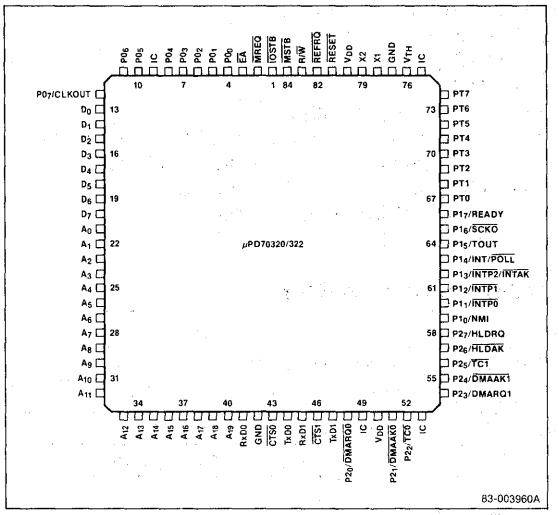
Pin Configurations (cont)

84-Pin PLCC



Pin Identification

Symbol	Function
A_0-A_{19}	Address bus outputs
D_0-D_7	Bidirectional data bus
X1, X2	Crystal connection terminals
$\overline{RESET}$	$\overline{Reset}$ input
V_{DD}	Positive power supply voltage
V_{SS}	Ground
V_{TH}	Threshold voltage input
PT0-PT7	Comparator port input lines
$\overline{EA}$	External access
$\overline{MREQ}$	Memory request output
$P0_0$-$P0_7$	I/O port 0
CLKOUT	System clock output
NMI	Nonmaskable interrupt input
$P1_1$-$P1_2$/ $\overline{INTP0}$-$\overline{INTP1}$	Parallel input port lines/ External interrupt input lines
$P1_3$/$\overline{INTP2}$/$\overline{INTAK}$	Parallel input port line/ External interrupt input line/ Interrupt acknowledge output
$P1_4$/INT/$\overline{POLL}$	I/O port 1/Interrupt request input/ I/O poll input
$P1_5$/TOUT	I/O port 1 bit/Timer out
$P1_6$/$\overline{SCK0}$	I/O port 1 bit/Serial clock out
$P1_7$/READY	I/O port 1 bit/Ready input
$P2_0$/$\overline{DMARQ0}$	I/O port 2 bit/DMA request 0
$P2_1$/DMAAR0	I/O port 2 bit/DMA acknowledge 0
$P2_2$/$\overline{TC0}$	I/O port 2 bit/DMA terminal count 0
$P2_3$/DMARQ1	I/O port 2/DMA request 1
$P2_4$/$\overline{DMAAK1}$	I/O port 2/DMA acknowledge 1
$P2_5$/$\overline{TC1}$	I/O port 2/DMA terminal count 1
$P2_6$/$\overline{HLDAK}$	I/O port 2/Hold acknowledge output
$P2_7$/HLDRQ	I/O port 2/Hold request input
$\overline{IOSTB}$	I/O strobe output
$\overline{MSTB}$	Memory strobe output
R/$\overline{W}$	Read/Write output
$\overline{REFRQ}$	Refresh pulse output
RxD0	Serial receive data 0 input
$\overline{CTS0}$	Clear to send 0 input
TxD0	Serial transmit data 0 output
RxD1	Serial receive data 1 input
$\overline{CTS1}$	Clear to send 1 input
TxD1	Serial transmit data 1 output

Pin Functions

A_0-A_{19} [Address Bus]

A_0-A_{19} is the 20-bit address bus used to access all external devices.

D_0-D_7 [Data Bus]

D_0-D_7 is the 8-bit external data bus.

$\overline{RESET}$ [Reset]

A low on $\overline{RESET}$ resets the CPU and all on-chip peripherals. $\overline{RESET}$ can also release the standby modes. After $\overline{RESET}$ returns high, program execution begins from address FFFF0H.

X1, X2 [Crystal Connections]

The internal clock generator requires an external crystal across these terminals.

V_{DD} [Power Supply]

Two positive power supply pins (V_{DD}) reduce internal noise.

V_{SS} [Ground]

Two ground connections (V_{SS}) reduce internal noise.

V_{TH} [Threshold Voltage]

The comparator port uses this pin to determine the analog reference point. The actual threshold to each comparator line can be V_{TH} or V_{TH} x n/16, where n = 1 to 15.

$\overline{EA}$ [External Access]

If this pin is low on reset, the μPD70322 will execute program code from external memory instead of from internal ROM.

$\overline{MREQ}$ [Memory Request]

$\overline{MREQ}$ (active low) informs external memory that the current bus cycle is a memory access bus cycle.

PT0-PT7 [Comparator Port]

PT0-PT7 are inputs to the analog comparator port.

$P0_0$-$P0_7$ [Port 0]

$P0_0$-$P0_7$ are the lines of port 0, an 8-bit bidirectional parallel I/O port.

$P1_0$-$P1_7$ [Port 1]

$P1_1$-$P1_3$ are the input only lines of parallel port 1. $P1_0$ and $P1_4$-$P1_7$ are the remaining lines of parallel port 1, each line individually programmable as either an input or output.

$P2_0$-$P2_7$ [Port 2]

$P2_0$-$P2_7$ are the lines of port 2, an 8-bit bidirectional I/O port. The lines can also be used as control signals for the on-chip DMA controller.

CLKOUT [System Clock]

This is the internal system clock. It can be used to synchronize external devices to the CPU.

NMI [Nonmaskable Interrupt]

NMI cannot be masked through software and is typically used for emergency processing. Upon execution, the interrupt starting address is obtained from interrupt vector number 2. NMI can release the standby modes and can be programmed to be either rising or falling edge triggered.

$\overline{INTP0}$-$\overline{INTP2}$ [External Interrupt]

$\overline{INTP0}$-$\overline{INTP2}$ allow external devices to generate I/O requests (interrupts). Each can be programmed to be rising or falling edge triggered.

$\overline{INTAK}$ [Interrupt Acknowledge]

After INT is asserted, the CPU will respond with $\overline{INTAK}$ (active low) to inform external devices that the interrupt request has been granted.

INT [Interrupt Request]

INT is a maskable, active-low, vectored interrupt request input. After assertion, external hardware must provide the interrupt vector number.

$\overline{POLL}$ [Poll]

Upon execution of the $\overline{POLL}$ intruction, the CPU checks the status of this pin and, if low, program execution continues. If high, the CPU will check the level of the line every five clock cycles until it is low. $\overline{POLL}$ can be used to synchronize program execution to external conditions.

TOUT [Timer Out]

TOUT is the square-wave output signal from the internal timer.

$\overline{SCKO}$, TxDn, $\overline{CTSn}$, RxDn [Serial Clock Out, Serial Transmit Data, Clear to Send, Serial Receive Data]

The two on-chip serial ports use these lines for data transmission, receiving, and handshaking.

READY [Ready]

After READY is asserted (active low), the CPU will synchronize and insert at least two wait states into a read or write cycle to memory or I/O. This allows the processor to accommodate devices whose access times are longer than normal execution allows.

DMARQn, DMAAKn, TCn [DMA Request, DMA Acknowledge, Terminal Count]

These are the control signals to and from the on-chip DMA controller.

HLDRQ [Hold Request]

The HLDRQ input (active low) is used by external devices to request the CPU to release the system bus to an external bus master. The following lines go into a high-impedance state with internal 4.7-kΩ pull-up resistors: A_0-A_{19}, D_0-D_7, $\overline{MREQ}$, R/$\overline{W}$, and $\overline{MSTB}$.

$\overline{HLDAK}$ [Hold Acknowledge]

An $\overline{HLDAK}$ output (active low) informs external devices that the CPU has released the system bus.

$\overline{IOSTB}$ [I/O Strobe]

$\overline{IOSTB}$ is asserted during read and write operations to external I/O.

$\overline{MSTB}$ [Memory Strobe]

$\overline{MSTB}$ (active low) is asserted during read and write operations to external memory.

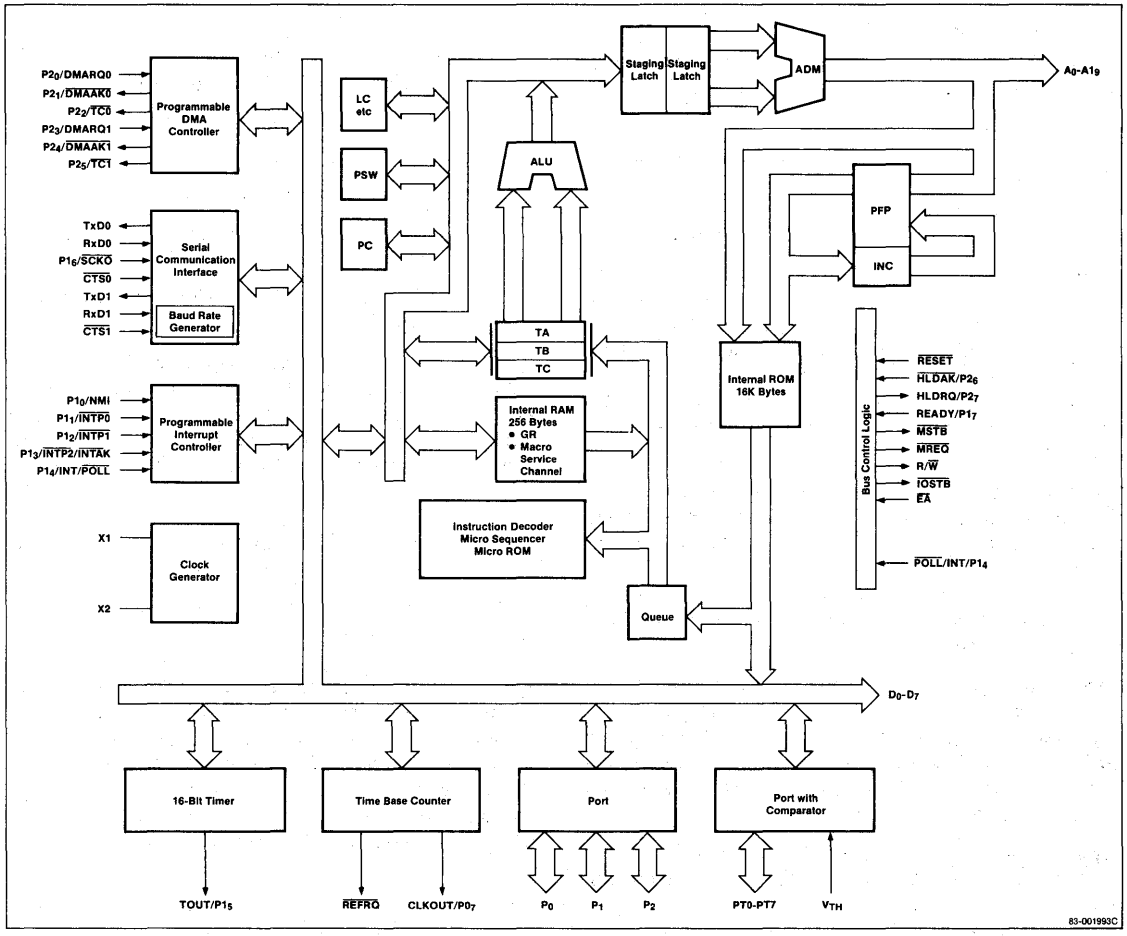
R/$\overline{W}$ [Read/Write]

An R/$\overline{W}$ output allows external hardware to determine if the current operation is a read or write cycle. It can also control the direction of bidirectional buffers.

$\overline{REFRQ}$ [Refresh]

This active-low output pulse can refresh nonstatic RAM. It can be programmed to meet system specifications and is internally synchronized so that refresh cycles do not interfere with normal CPU operation.

Block Diagram



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Functional Description

Architectural Enhancements

The following features enable the μPD70320/322 to perform high-speed execution of instructions:

- Dual data bus
- 16-/32-bit temporary registers/shifters (TA, TB, TA + TB)
- 16-bit loop counter (LC)
- Program counter (PC) and prefetch pointer (PFP)

Dual Data Bus. The μPD70320/322 has two internal 16-bit data buses: the main data bus and a subdata bus. This reduces the processing time required for addition/subtraction, and logical comparison instructions by one third over single bus systems. The dual data bus method allows two operands to be fetched simultaneously from the general purpose registers and transferred to the ALU.

16-/32-Bit Temporary Registers/Shifters. The 16-bit temporary registers/shifters (TA, TB) allow high-speed execution of multiplication/ division and shift/rotation instructions. By using the temporary registers/shifters, the μPD70320/322 can execute multiplication/division instructions about four times faster than with the microprogramming method.

Loop Counter [LC]. The dedicated hardware loop counter counts the number of loops for string operations and the number of shifts performed for multiple bit shift/rotation instructions. The loop counter works with internal dedicated shifters to speed the processing of multiplication/division instructions.

Program Counter and Prefetch Pointer [PC and PFP]. The hardware PC addresses the memory location of the instruction to be executed next. The hardware PFP addresses the program memory location to be accessed next. Several clocks are saved for branch, call, return, and break instructions compared with processors having only one instruction pointer.

Register Set

Figure 1 shows the μPD70320/322 has eight banks of registers functionally mapped into internal RAM. Each bank contains general purpose registers, pointer and index registers, segment registers, and save areas.

General Purpose Registers [AW, BW, CW, DW]. There are four 16-bit general purpose registers that can each serve as individual 16-bit registers or two independent 8-bit registers (AH, AL, BH, BL, CH, CL, DH, DL). The following instructions use the general purpose registers for default:

AW	Word multiplication/division, word I/O, data conversion
AL	Byte multiplication/division, byte I/O, BCD rotation, data conversion, translation
AH	Byte multiplication/division
BW	Translation
CW	Loop control branch, repeat prefix
CL	Shift instructions, rotation instructions, BCD operations
DW	Word multiplication/division, indirect addressing I/O

Pointers [SP, BP] and Index Registers [IX, IY]. These registers are used as 16-bit base pointers or index registers in based addressing, indexed addressing, and based indexed addressing. The registers are used as default registers under the following conditions:

SP	Stack operations
IX	Block transfer (source), BCD string operations
IY	Block transfer (destination), BCD string operations

Segment Registers. The segment registers divide the 1M-byte address space into 64K-byte blocks. Each segment register functions as a base address to a block; the effective address is an offset from that base. Physical addresses are generated by shifting the associated segment register left four binary digits and then adding the effective address. The segment registers are:

Segment Register	Default Offset
PS (Program segment)	PC
SS (Stack segment)	SP, Effective address
DS0 (Data segment-0)	IX, Effective address
DS1 (Data segment-1)	IY, Effective address

Save Registers. SAVE PC and SAVE PSW are used as save areas during register bank context switching. The VECTOR PC save location contains the effective address of the interrupt service routine when register bank switching is used to service interrupts.

Program Counter [PC]. The PC is a 16-bit binary counter that contains the offset address from the program segment of the next instruction to be executed. It is incremented every time an instruction is received from the queue. It is loaded with a new location whenever a branch, call, return, break, or interrupt is executed.

Processor Status Word [PSW]. The PSW contains the following status and control flags.

15 PSW 8

1	RB2	RB1	RB0	V	DIR	IE	BRK

7 0

S	Z	F1	AC	F0	P	BRKI	CY

Status Flags

- V Overflow bit
- S Sign
- Z Zero
- AC Auxiliary carry
- P Parity
- CY Carry

Control Flags

- DIR Direction of string processing
- IE Interrupt enable
- BRK Break (after every instruction)
- RBn Register bank select
- BRKI I/O trap enable (see software interrupts)
- F0, F1 General-purpose user flags (accessed through the flag special function register)

Memory Map

The μPD70320/322 has a 20-bit address bus that can directly access 1M bytes of memory. Figure 2 shows that the 16K bytes of internal ROM (μPD70322 only) are located at the top of the address space from FC000H to FFFFFH.

Internal Data Area. Figure 2 shows the internal data area (IDA) is a 256-byte internal RAM area followed consecutively by a 256-byte special function register (SFR) area. All the data and control registers for on-chip peripherals and I/O are mapped into the SFR area and accessed as RAM. The IDA is dynamically relocatable in 4K-byte increments by changing the value in the internal data base (IDB) register. Whatever value is in this register will be assigned as the uppermost eight bits of the IDA address.

On reset, the internal data base register is set to FFH which maps the IDA into the internal ROM space. However, since the μPD70322 has a separate bus to internal ROM, this does not present a problem. When these address spaces overlap, program code cannot be executed from the IDA and internal ROM locations cannot be accessed as data. You can select any of the eight possible register banks which occupy the entire internal RAM space. Multiple register bank selection allows faster interrupt processing and facilitates multitasking.

In larger-scale systems where internal RAM is not required for data memory, the internal RAM can be removed completely from the address space and dedicated entirely to registers and control functions such as macro service and DMA channels. Clearing the RAMEN bit in the processor control register achieves this. When the RAMEN bit is cleared, internal RAM can only be accessed by register addressing or internal control processes.

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Figure 1. Register Banks in Internal RAM

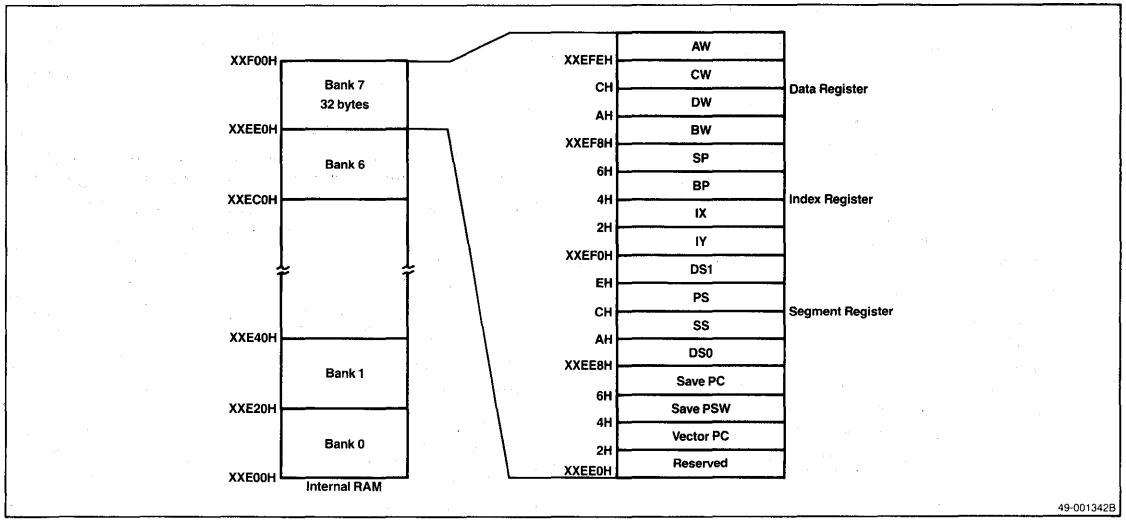
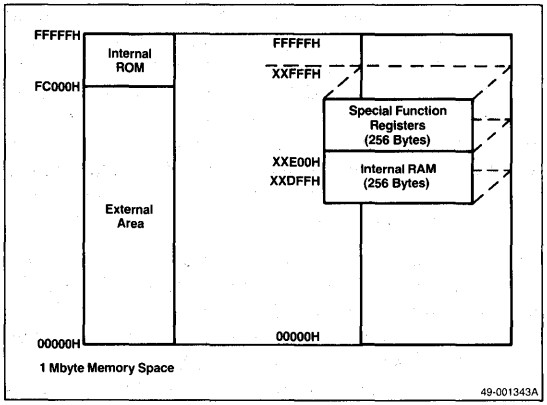


Figure 2. Memory Map



Instruction Set

The μPD70320/322 instruction set is fully compatible with the V20 native mode instruction set. The V20 instruction set is a superset of the μPD8086/8088 instruction set with different execution times and mnemonics.

The μPD70320/322 does not support the V20 8080 emulation mode. All of the instructions pertaining to this have been deleted from the μPD70320/322 instruction set.

Enhanced Instructions

In addition to the μPD8086/88 instructions, the μPD70320/322 has the following enhanced instructions.

Instruction	Function
PUSH imm	Pushes immediate data onto stack
PUSH R	Pushes eight general registers onto stack
POP R	Pops eight general registers from stack
MUL imm	Executes 16-bit multiply of register or memory contents by immediate data
SHL imm8 SHR imm8 SHRA imm8 ROL imm8 ROR imm8 ROLC imm8 RORC imm8	Shifts/rotates register or memory by immediate value
CHKIND	Checks array index against designated boundaries
INM	Moves a string from an I/O port to memory
OUTM	Moves a string from memory to an I/O port
PREPARE	Allocates an area for a stack frame and copies previous frame pointers
DISPOSE	Frees the current stack frame on a procedure exit

Unique Instructions

The μPD70320/322 has the following unique instructions.

Instruction	Function
INS	Inserts bit field
EXT	Extracts bit field
ADD4S	Performs packed BCD string addition
SUB4S	Performs packed BCD string subtraction
CMP4S	Performs packed BCD string comparison
ROL4	Rotates BCD digit left
ROR4	Rotates BCD digit right
TEST1	Tests bit
SET1	Sets bit
CLR1	Clears bit
NOT1	Complements bit
BTCLR	Tests bit; if true, clear and branch
REPC	Repeat while carry set
REPNC	Repeat while carry cleared

Variable Length Bit Field Operation Instructions

Bit fields are a variable length data structure that can range in length from 1 to 16 bits. The μPD70320/322 supports two separate operations on bit fields: insertion (INS) and extraction (EXT). There are no restrictions on the position of the bit field in memory. Separate segment, byte offset, and bit offset registers are used for insertion and extraction. Following the execution of these instructions, both the byte offset and bit offset are left pointing to the start of the next bit field, ready for the next operation. Bit field operation instructions are powerful and flexible and are therefore highly effective for graphics, high level languages, and packing/unpacking applications.

Insert bit field copies the bit field of specified length from the AW register to the bit field addressed by DS1:IY:reg8 (8-bit general purpose register). The bit field length can be located in any byte register or

supplied as immediate data. Following execution, both the IY and reg8 are updated to point to the start of the next bit field.

Bit field extraction copies the bit field of specified length from the bit field addressed by DS0:IX:reg8 to the AW register. If the length of the bit field is less than 16 bits, the bit field is right justified with a zero fill. The bit field length can be located in any byte register or supplied as immediate data. Following execution, both IX and reg8 are updated to point to the start of the next bit field.

Figures 3 and 4 show bit field insertion and bit field extraction.

Packed BCD

Packed BCD instructions process packed BCD data either as strings (ADD4S, SUB4S, CMP4S) or byte format operands (ROR4, ROL4). Packed BCD strings may be one to 254 digits in length. The two BCD rotation instructions perform rotation of a single BCD digit in the lower half of the AL register through the register or the memory operand.

Bit Manipulation Instructions

The μPD70320/322 has five unique bit manipulation instructions. The ability to test, set, clear, or complement a single bit in a register or memory operand increases code readability as well as performance over the logical operations traditionally used to manipulate bit data. This feature further enhances control over on-chip peripherals.

Repeat Prefixes

Two new repeat prefixes (REPC, REPNC) allow conditional block transfer instructions to use the state of the CY flag as the termination condition. This allows inequalities to be used when working on ordered data, thus increasing performance when searching and sorting algorithms.

Figure 3. Bit Field Insertion

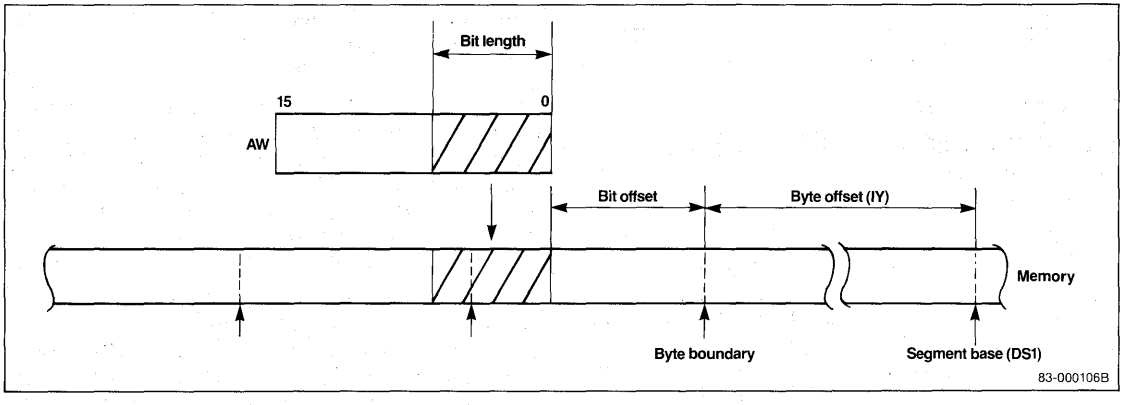
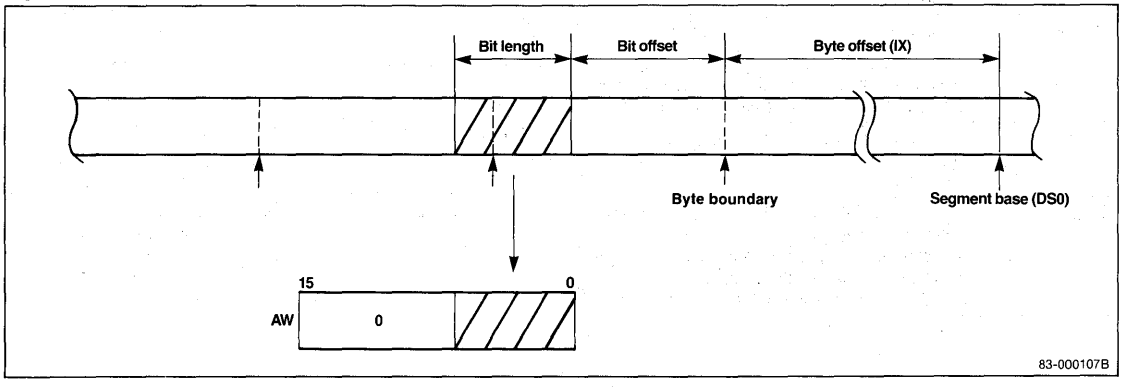


Figure 4. Bit Field Extraction



Besides the V20 instruction set, the μPD70320/322 has the four additional instructions described in table 1.

Table 1. Additional Instructions

Instruction	Function
BTCLR var,imm3, short label	Bit test and if true, clear and branch; otherwise, no operation
STOP (no operand)	Power down instruction, stops oscillator
RETRBI (no operand)	Return from register bank context switch interrupt
FINT (no operand)	Finished interrupt. After completion of a hardware interrupt or I/O request, this instruction must be used to reset the current priority bit in the in-service priority register (ISPR).

The ISPR is an 8-bit register; each of its bits, PR_0-PR_7, correspond to each of the eight possible I/O request priorities, respectively. The ISPR keeps track of the priority of the interrupt currently being serviced by setting the appropriate bit. The ISPR format is shown below.

PR_7	PR_6	PR_5	PR_4	PR_3	PR_2	PR_1	PR_0

Interrupt Structure

The μPD70320/322 can service interrupts generated through hardware and software. Table 2 shows the various software interrupts.

Table 2. Software Interrupts

Interrupt	Description
Divide error	The CPU will trap if a divide error occurs as the result of a DIV or DIVU instruction.
Single step	The interrupt is generated after every instruction if the BRK bit in the PSW is set.
Overflow	By using the BRKV instruction, an interrupt can be generated as the result of an overflow.
Interrupt instructions	The BRK 3 and BRK imm8 instructions can generate interrupts.
Array bounds	The CHKIND instruction will generate an interrupt if specified array bounds have been exceeded.
Escape trap	The CPU will trap on an FP01,2 instruction to allow software to emulate the floating point processor.
I/O trap	If the I/O trap bit in the PSW is set, a trap will be generated on every IN or OUT instruction. Software can then provide an updated peripheral address. This feature allows software interchangeabilty between different systems.

When executing software written for another system, it is better to implement I/O with on-chip peripherals to reduce external hardware requirements. However, since μPD70320/322 internal peripherals are memory mapped, software conversion could be difficult. The I/O trap feature allows easy conversion from external peripherals to on-chip peripherals.

Interrupt Vector Table. Table 3 shows the starting addresses of interrupt processing routines. The table begins at physical address 0H, which is outside the internal ROM space. Therefore, if utilizing an interrupt processing routine within the interrupt vector table, external memory will be required. By servicing interrupts via the macro service function or context switching, you can avoid the addition of external memory.

Each interrupt vector is four bytes. Upon execution of a vectored interrupt, the lower addressed word is transferred to the PC, and the upper word to the PS. However, the byte order within each word is reversed so that the low-order bytes of the vector address become the most significant bytes in the PC and PS.

Hardware Interrupt Configuration. There are two types of hardware interrupt requests: standard vectored interrupts and I/O requests.

After a vectored interrupt, the PC and PSW are saved on the stack and the program transfers to the location indicated by the interrupt vector contents. When an interrupt is triggered by NMI, the CPU automatically traps to vector number two. When an interrupt is triggered by INTR, external devices must provide the interrupt vector number.

I/O requests are a group of interrupts, generated externally or from on-chip peripherals. The internal interrupt controller controls I/O requests. I/O requests can be serviced (by the macro service function) without transferring program control to an interrupt routine. The following are the 14 possible I/O requests.

Group	Source
External interrupt request	INTP0, INTP1, INTP2
DMA controller	INTD0, INTD1
Timer	INTTU0, INTTU1, INTTU2
Serial interface	INTSER0, INTSR0, INTST0, INTSER1, INTSR1, INTST1

Table 3. Interrupt Vectors

Address (Hex)	Vector No.	Assigned Use
00	0	Divide error 04 1 Break flag
04	1	Break flag
08	2	NMI
0C	3	BRK3 instruction
10	4	BRKV instruction
14	5	CHKIND instruction
18	6	General purpose
1C	7	Escape trap
20	8	General purpose
24-3C	9-15	Reserved
40-4C	15-19	General purpose
50	20	I/O trap
54-5C	21-23	General purpose
60	24	Reserved
64-6C	25-27	General purpose
70	28	INTSER0
74	29	INTSR0
78	30	INTST0
7C	31	General purpose
80	32	INTSER1
84	33	INTSR1
88	34	INTST1
8C	35	General purpose
90	36	INTD0
94	37	INTD1
98-9C	38,39	General purpose
A0	40	$\overline{\text{INTP0}}$
A4	41	$\overline{\text{INTP1}}$
A8	42	$\overline{\text{INTP2}}$
AC	43	General purpose
B0	44	INTTU0
B4	45	INTTU1
B8	46	INTTU2
BC	47	INTTB
0C0-3FF	48-255	General purpose

Arbitration of I/O requests is resolved internally by the interrupt controller. The priority of each I/O request is individually programmable from 0 to 7 (0 is the highest priority). You can process these interrupts in one of three modes: standard vectored interrupt, register bank context switching, or macro service function. When standard vectored interrupt mode is selected, I/O requests are serviced as previously described vectored interrupts. The CPU automatically traps to the vector location shown in the interrupt vector table.

Register bank context switching allows I/O requests to be processed rapidly by switching register banks. After an interrupt, the new register bank selected is that which has the same register bank number (0-7) as the priority of the interrupt to be serviced. The PC and PSW are automatically stored in the save areas of the new register bank and the address of the interrupt routine is loaded from the vector PC storage location in the new register bank. After interrupt processing, execution of the RETRBI (return from register bank interrupt) returns control to the former register bank and restores the former PC and PSW. Figures 5 and 6 show register bank context switching and register bank return.

The macro service function (MSF) acts as an internal DMA controller between on-chip peripherals (special function registers) and memory. The MSF greatly reduces the software overhead and CPU time that other processors would require for register save processing, register returns, and other handling associated with interrupt processing.

If the MSF is selected for a particular I/O request, each time the request is received, a byte or word of data will be transferred between the SFR and memory without interrupting the CPU. Each time a request occurs, the macro service counter is decremented. When the counter reaches zero, an interrupt is generated. The MSF also has a character search option. When selected, every byte transferred will be compared to an 8-bit search character and an interrupt will be generated if a match occurs or if the macro service counter counts out.

There are eight eight-byte macro service channels mapped into internal RAM from XXE00H to XXE3FH. Figure 7 shows the components of each channel.

Figure 5. Register Bank Context Switching

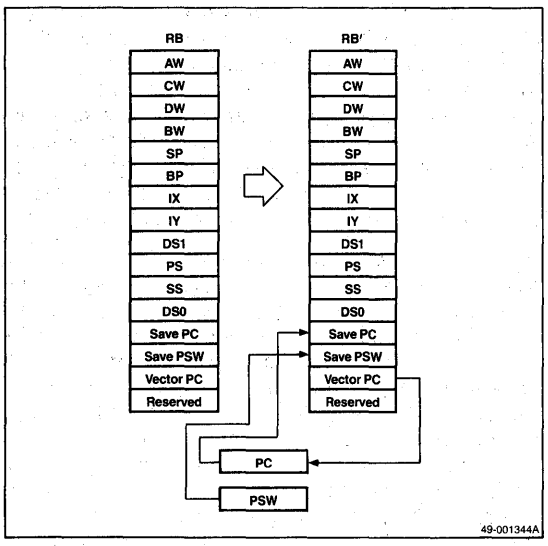


Figure 6. Register Bank Return

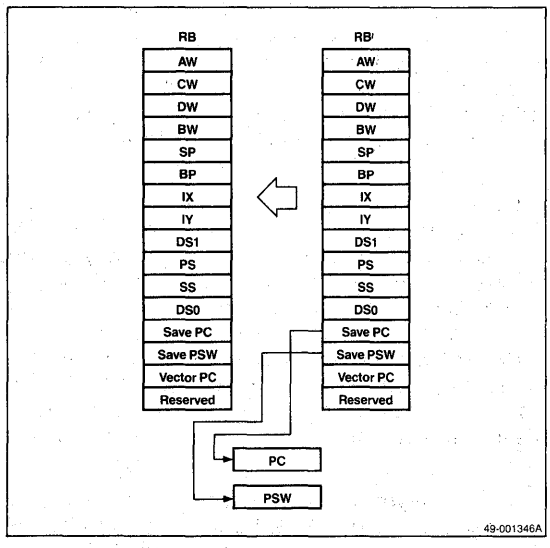
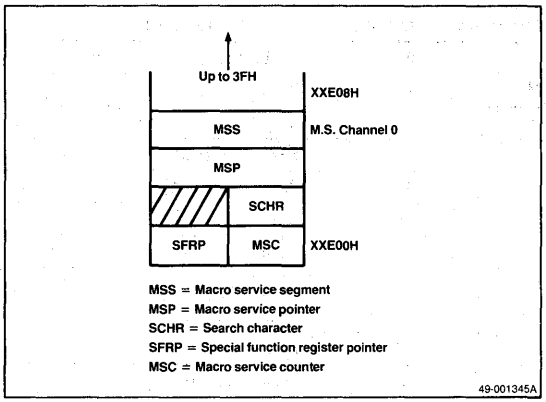


Figure 7. Macro Service Channels



On-Chip Peripherals

Timer Unit

The μPD70320/322 (figure 8) has two programmable 16-bit interval timers (TM0,TM1) with variable input clock frequencies on-chip. Each of the two 16-bit timer registers has an associated 16-bit modulus register (MD0, MD1). The timer operates in interval timer mode or one-shot mode.

Interval Timer Mode. In this mode, TM0/TM1 are decremented by the selected input clock and, after counting out, the registers are automatically reloaded from the modulus registers and counting continues. Each time TM1 counts out, I/O requests are generated through TF1 and TF2 (Timer Flags 1,2). When TM0 counts out, an I/O request is generated through TF0. The timer out signal can be used as a square wave output whose half-cycle is equal to the count time. There are two selectable input clocks (SCLK: system clock = fosc/2, fosc = 10 MHz).

Clock	Timer Resolution	Full Count
SCLK/6	1.2 μs	78.643 ms
SCLK/128	25.6 μs	1.678 s

One-Shot Mode. In the one-shot mode, TM0 and MD0 operate as independent one-shot timers. Starting with a preset value, each is decremented to zero. At zero, counting ceases and an I/O request is generated by TF0 or TF1. One-shot mode allows two selectable input clocks (fosc = 10 MHz).

Clock	Timer Resolution	Full Count
SCLK/12	2.4 μs	157.283 ms
SCLK/128	25.6 μs	1.678 s

Time Base Counter

The μPD70320/70322 has a free-running long base counter that can be used to generate periodic interrupts at lengthy intervals. The counter has three selectable input clocks: SCLK, SCLK/2, and SCLK/4. You can select one of the following four taps (outputs) from the counter as an interrupt source: i/1024, i/8192, i/64K, or i/1M ("i" is the selected input clock).

The TBC interrupt is unlike the other on-chip peripheral I/O requests in that it is preset as a level seven vectored interrupt. Macro service and register bank switching cannot be used to service this interrupt. Figure 9 is the time base counter block diagram.

Refresh Controller

The μPD70320/322 has an on-chip refresh controller for dynamic and pseudostatic RAM mass storage memories. The refresh controller generates refresh addresses and refresh pulses. It inserts refresh cycles between the normal CPU bus cycles according to refresh specifications.

The refresh controller outputs a 9-bit refresh address on address bits A_0-A_8 during the refresh bus cycle. Address bits A_8-A_{19} are all 1's. The 9-bit refresh address is automatically incremented at every refresh timing for 512 row addresses. The 8-bit refresh mode (RFM) register specifies the refresh operation and allows refresh during both CPU HALT and HOLD modes. Refresh cycles are automatically timed to $\overline{\text{REFRQ}}$ following read/write cycles to minimize the effect on system throughput.

The following shows the $\overline{\text{REFRQ}}$ pin level in relation to bits 4 (RFEN) and 7 (RELV) of the refresh mode register.

RFEN	RELV	$\overline{\text{REFRQ}}$ Level
0	0	0
0	1	1
1	0	0
1	1	Refresh pulse output

Figure 9. Time Base Counter Block Diagram

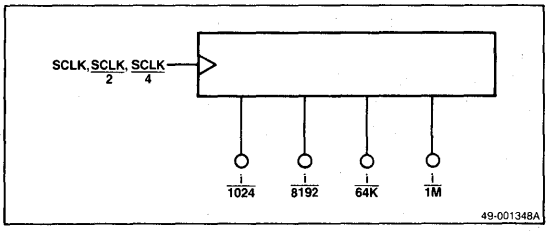
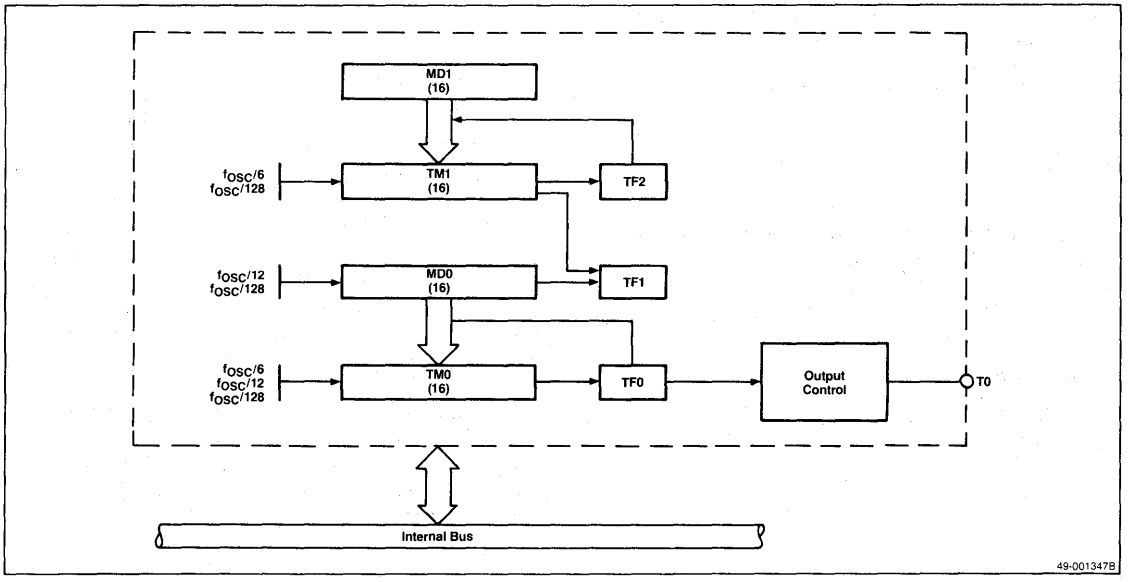


Figure 8. Timer Unit Block Diagram



Serial Interface

The μPD70320/322 has two full-duplex UARTs, channel 0 and channel 1. Each serial port channel has a transmit line (TxDn), a receive line (RxDn), and a clear to send (CTSn) input line for handshaking. Communication is synchronized by a start bit, and you can program the ports for even, odd, or no parity, character lengths of seven or eight bits, and one or two stop bits.

The μPD70320/322 has dedicated baud rate generators for each serial channel. This eliminates the need to obligate the on-chip timers. The baud rate generator allows a wide range of data transfer rates (up to 1 Mbps). This includes all of the standard baud rates without being restricted by the value of the particular external crystal. Each baud rate generator has an 8-bit baud rate generator (BRGn) data register which functions as a prescaler to a programmable input clock selected by the serial communication control (SCCn) register. Together these must be set to generate a frequency that is equivalent to the desired baud rate.

In addition to the asynchronous mode, channel 0 has a synchronous I/O interface mode. In this mode, each bit of data transferred is synchronized to a serial clock ($\overline{SCKO}$). This is the same as the NEC μCOM75 and μCOM87 series, and allows easy interfacing to these devices. Figure 10 shows the serial interface block diagram.

DMA Controller

The μPD70320/322 has a two-channel, on-chip DMA controller. This allows rapid data transfer between memory and auxiliary storage devices. The DMA controller supports four modes of operation, two for memory-to-memory transfers and two for transfers between I/O and memory.

Memory-to-Memory Transfers. In single-step mode, the falling edge of $\overline{DMARQ}$ causes DMA transfer cycles and CPU bus cycles to alternate as long as $\overline{DMARQ}$ is low or until the prescribed number of DMA transfers has occurred. Interrupts can be accepted while in this mode. In burst mode, DMA transfer cycles continue until the DMA terminal counter decrements to zero. Software can also initiate memory-to-memory transfers.

Transfers Between I/O and Memory. In single-transfer mode, one DMA transfer occurs after each falling edge of $\overline{DMARQ}$. After the transfer, the bus is returned to the CPU. In demand release mode, the falling edge of $\overline{DMARQ}$ enables DMA cycles, which continue as long as $\overline{DMARQ}$ is low.

In all modes, the $\overline{TC}$ (terminal count) output pin will pulse low and a DMA completion I/O request will be generated after the predetermined number of DMA cycles has been completed. Figure 11 shows the DMA channel area in memory.

The bottom of internal RAM contains all of the necessary address information for the designated DMA channels. The DMA channel mnemonics are as follows:

TC	Terminal counter
SAR	Source address register
SARH	Source address register high
DAR	Destination address register
DARH	Destination address register high

The DMA controller generates physical source addresses by offsetting SARH 12 bits to the left and then adding the SAR. The same procedure is also used to generate physical destination addresses. You can program the controller to increment or decrement source and/or destination addresses independently during DMA transfers.

Parallel Ports

The μPD70320/322 has three 8-bit parallel I/O ports: P0, P1, and P2. SFR locations can access these ports. The port lines are individually programmable as inputs or outputs. Many of the port lines have dual functions as port or control lines.

The analog comparator port (PT) compares each input line to a reference voltage. The reference voltage is programmable to be the V_{REF} input or V_{REF} x n/16, where n = 1 to 15.

Programmable Wait State Generation

You can generate wait states internally to further reduce the necessity for external hardware. Insertion of these wait states allows direct interface to devices whose access times cannot meet the CPU read/write timing requirements.

When using this function, the entire 1M-byte memory address space is divided into 128K-blocks. Each block, with the exception of the uppermost block, can be programmed for zero, one, or two wait states, or for external control (READY signal). The appropriate bits in the wait control word (WTC) control wait state generation. Programming the bits corresponding to the top 128K-byte block of memory, will actually set the wait state conditions for the entire I/O address space. Figure 12 shows the memory map for programmable wait state generation.

Figure 10. Serial Interface Block Diagram

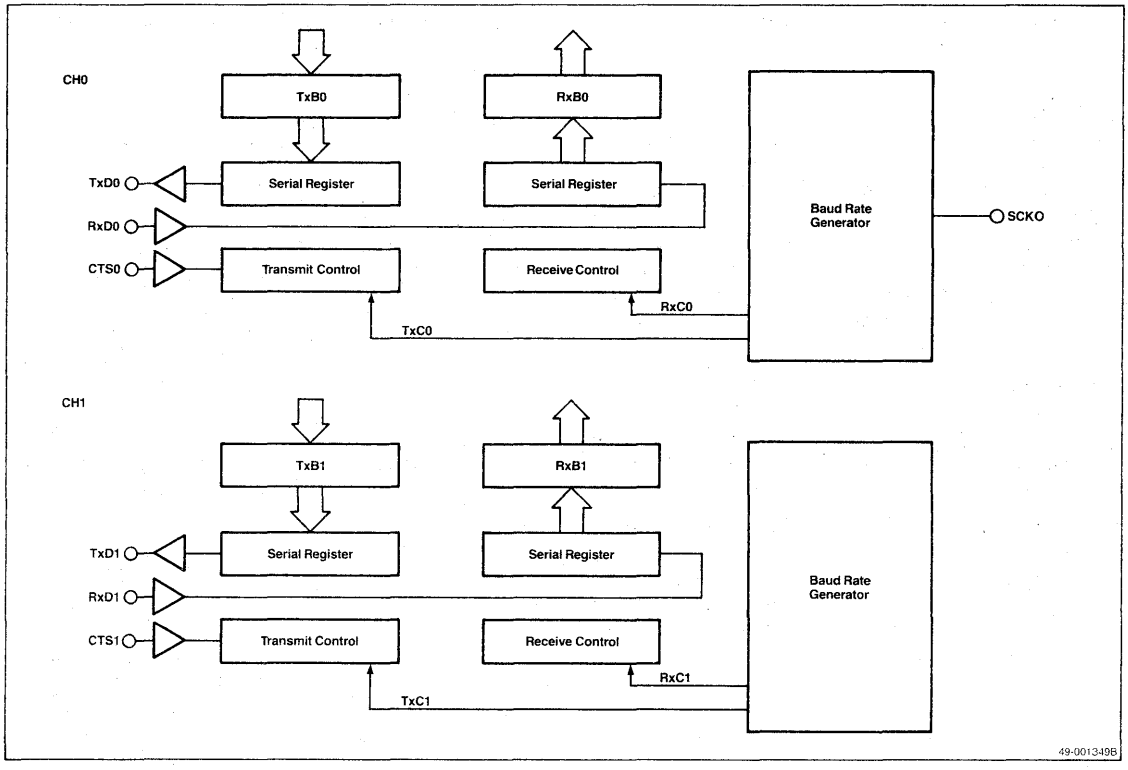


Figure 11. DMA Channels

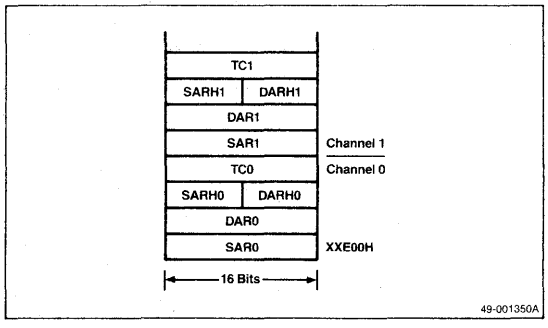
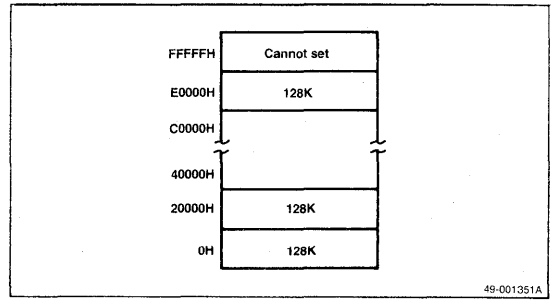


Figure 12. Programmable Wait State Generation



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Low-Power Standby

There are two low-power standby modes: HALT and STOP. Software causes the processor to enter either mode.

HALT Mode. In the HALT mode, the processor is inactive and the chip consumes much less power than when operational. The external oscillator remains functional and all peripherals are active. Internal status and output port line conditions are maintained. Any unmasked interrupt or I/O request can release this mode. In the EI state, I/O requests subsequently will be processed as vectored interrupts. In the DI state, program execution is restarted with the instruction following the HALT instruction.

STOP Mode. The STOP mode allows the largest power reduction while maintaining RAM. The oscillator is stopped, halting all internal peripherals. All internal status is maintained. Only a reset or NMI can release this mode.

A standby flag in the SFR area is set by rises in the supply voltage. The flag is reset when its status is read. Its status is maintained during normal operation and standby. Use the standby flag to determine whether program execution is returning from standby or from a cold start.

Special Function Registers

Table 4 shows the special function register mnemonic, type, address, reset value, and function. Figures 13 through 32 show the register formats.

Table 4. Special Function Registers

Name	Byte/ Word	Address	Reset Value	Function
P0	B	xxF00H		Port 0
PM0	B	xxF01H	FFH	Port mode 0
PMC0	B	xxF02H	00H	Port mode control 0
P1	B	xxF08H		Port 1
PM1	B	xxF09H	FFH	Port mode 1
PMC1	B	xxF0AH	00H	Port mode control 1
P2	B	xxF10H		Port 2
PM2	B	xxF11H	FFH	Port mode 2
PMC2	B	xxF12H	00H	Port mode control 2
PT	B	xxF38H		Port T
PMT	B	xxF3BH	00H	Port mode T
INTM	B	xxF40H	00H	Interrupt mode
EMS0	B	xxF44H		External interrupt macro service 0
EMS1	B	xxF45H		External interrupt macro service 1
EMS2	B	xxF46H		External interrupt macro service 2
EXIC0	B	xxF4CH	47H	External I/O request control 0
EXIC1	B	xxF4DH	47H	External I/O request control 1
EXIC2	B	xxF4EH	47H	External I/O request control 2

Table 4. Special Function Registers (cont)

Name	Byte/ Word	Address	Reset Value	Function
RXB0	B	xxF60H		Receive buffer 0
TXB0	B	xxF62H		Transfer buffer 0
SRMS0	B	xxF65H		Serial receive macro service 0
STMS1	B	xxF66H		Serial transmit macro service 1
SCM0	B	xxF68H	00H	Serial communication mode 0
SCC0	B	xxF69H	00H	Serial communication control 0
BRG0	B	xxF6AH	00H	Baud rate generator 0
SCE0	B	xxF6BH	00H	Serial communication error 0
SEIC0	B	xxF6CH	47H	Serial error I/O request control 0
SRIC0	B	xxF6DH	47H	Serial receive I/O request control 0
STIC0	B	xxF6EH	47H	Serial transmit I/O request control 0
RXB1	B	xxF70H		Receive buffer 1
TXB1	B	xxF72H		Transmit buffer 1
SRMS1	B	xxF75H		Serial receive macro service 1
STMS1	B	xxF76H		Serial transmit macro service 1
SCM1	B	xxF78H	00H	Serial communication mode 1
SCC1	B	xxF79H	00H	Serial communication control 1
BRG1	B	xxF7AH	00H	Baud rate generator register 1
SCE1	B	xxF7BH	00H	Serial communication error 0
SEIC1	B	xxF7CH	47H	Serial error I/O request control 1
SRIC1	B	xxF7DH	47H	Serial receive I/O request control 1
STIC1	B	xxF7EH	47H	Serial transmit I/O request control 1
TM0	W	xxF80H		Timer register 0
TM0L	B	xxF80H		Timer register 0 low
TM0H	B	xxF81H		Timer register 0 high
MD0	W	xxF82H		Modulo register 0
MD0L	B	xxF82H		Modulo register 0 low
MD0H	B	xxF83H		Modulo register 0 high
TM1	W	xxF88H		Timer register 1
TM1L	B	xxF88H		Timer register 1 low
TM1H	B	xxF89H		Timer register 1 high
MD1	W	xxF8AH		Modulo register 1
MD1L	B	xxF8AH		Modulo register 1 low
MD1H	B	xxF8BH		Modulo register 1 high
TMC0	B	xxF90H	00H	Timer control 0
TMC1	B	xxF91H	00H	Timer control 1
TMMS0	B	xxF94H		Timer macro service 0
TMMS1	B	xxF95H		Timer macro service 1
TMMS2	B	xxF96H		Timer macro service 2
TMIC0	B	xxF9CH	47H	Timer I/O request control 0
TMIC1	B	xxF9DH	47H	Timer I/O request control 1
TMIC2	B	xxF9EH	47H	Timer I/O request control 2
DMAC0	B	xxFA0H		DMA control 0
DMAM0	B	xxFA1H	00H	DMA mode 0
DMAC1	B	xxFA2H		DMA control 1
DMAM1	B	xxFA3H	00H	DMA mode 1
DIC0	B	xxFACH	47H	DMA I/O request control 0
DIC1	B	xxFADH	47H	DMA I/O request control 1
RFM	B	xxFE1H	10H	Refresh mode
TBIC	B	xxFECH	47H	Time base I/O request control
WTC	W	xxFE8H	FFH	Wait control
WTCL	B	xxFE8H	FFH	Wait control low
WTCH	B	xxFE9H	FFH	Wait control high
PSWL	B	xxFEAH	00H	Flag register
PRC	B	xxFEBH	4EH	Processor control
SB	B	xxFE0H		Standby control
IDB	B	FFFFFH	FFH	Internal data area base

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Figure 13. Port Mode Registers 0, 1, and 2.

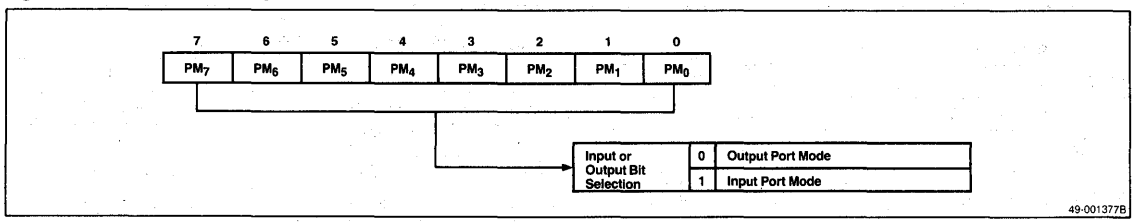


Figure 14. Port Mode Control 0 Register

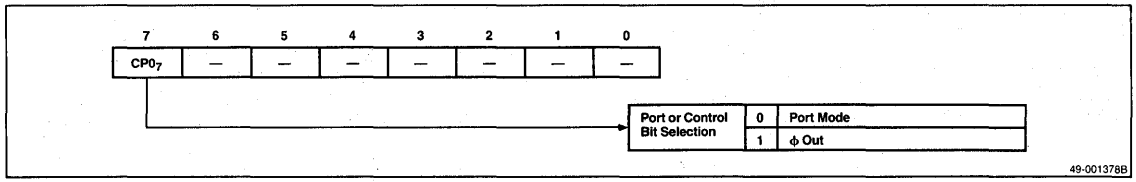


Figure 15. Port Mode Control 1 Register

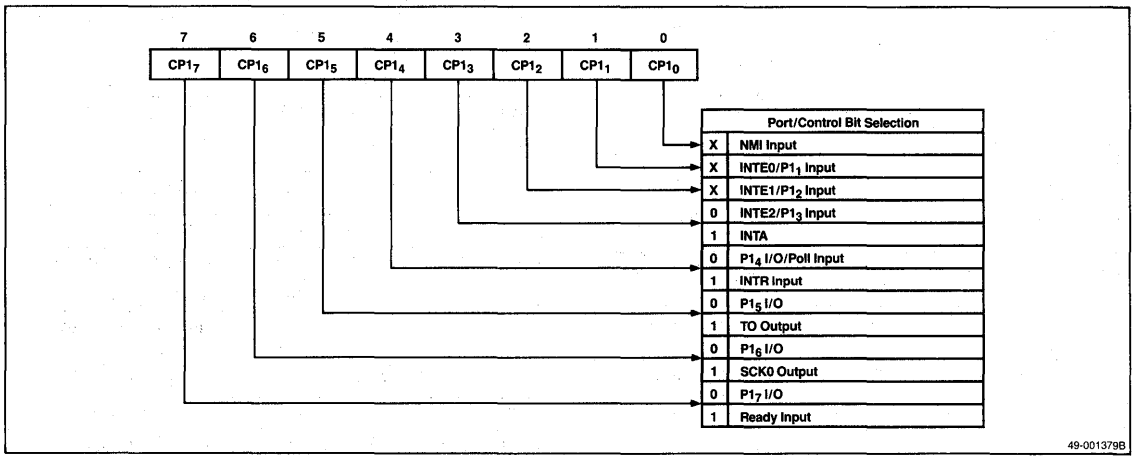


Figure 16. Port Mode Control 2 Register

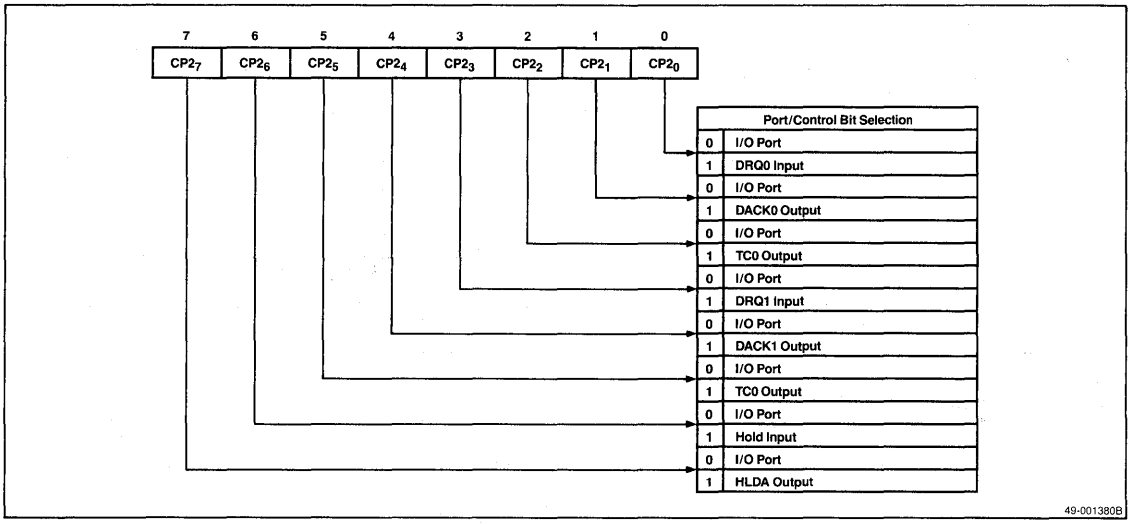
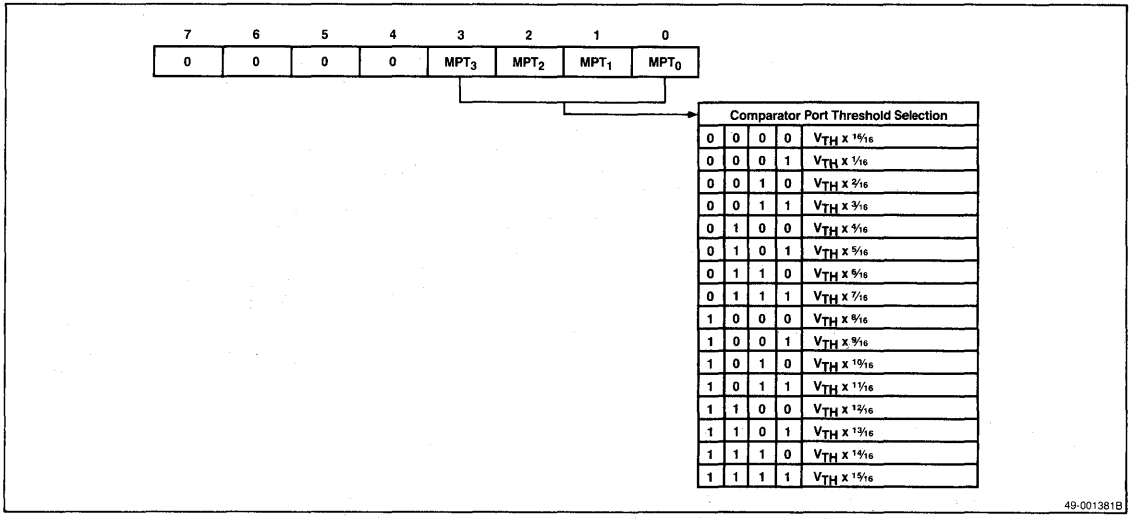


Figure 17. Port Mode T Register



5

Figure 18. Interrupt Mode Register

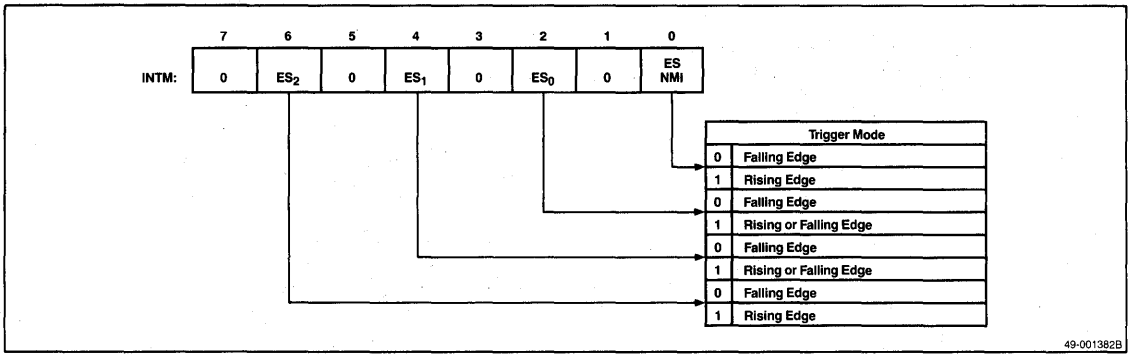


Figure 19. I/O Request Control Registers

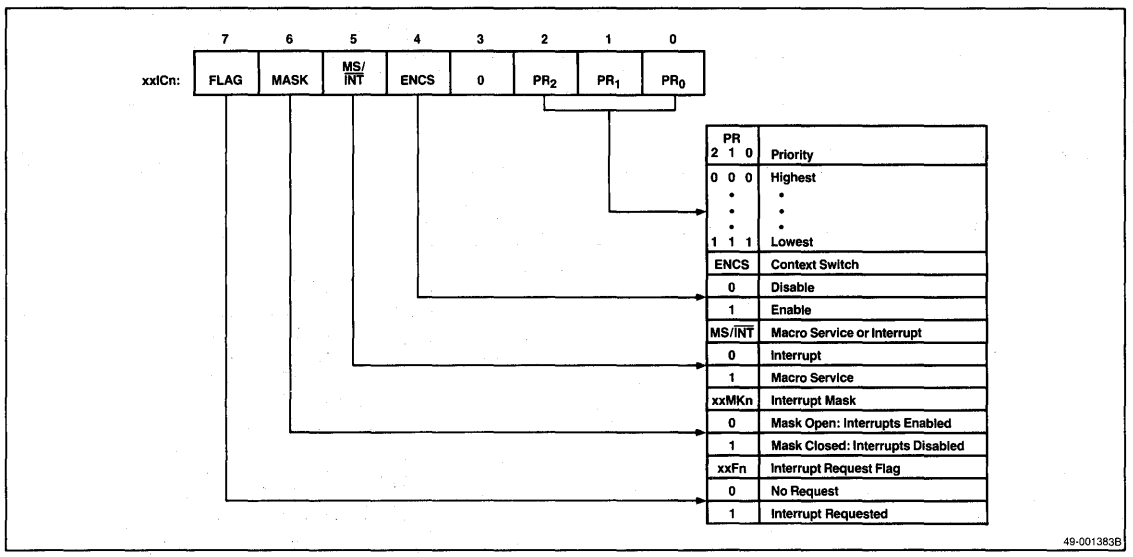


Figure 20. Macro Service Control Registers

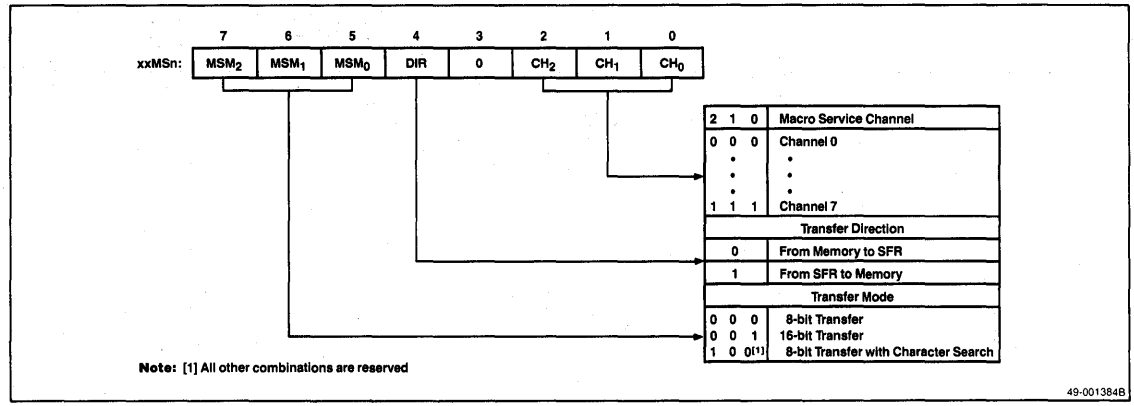


Figure 21. Serial Communication Mode Register

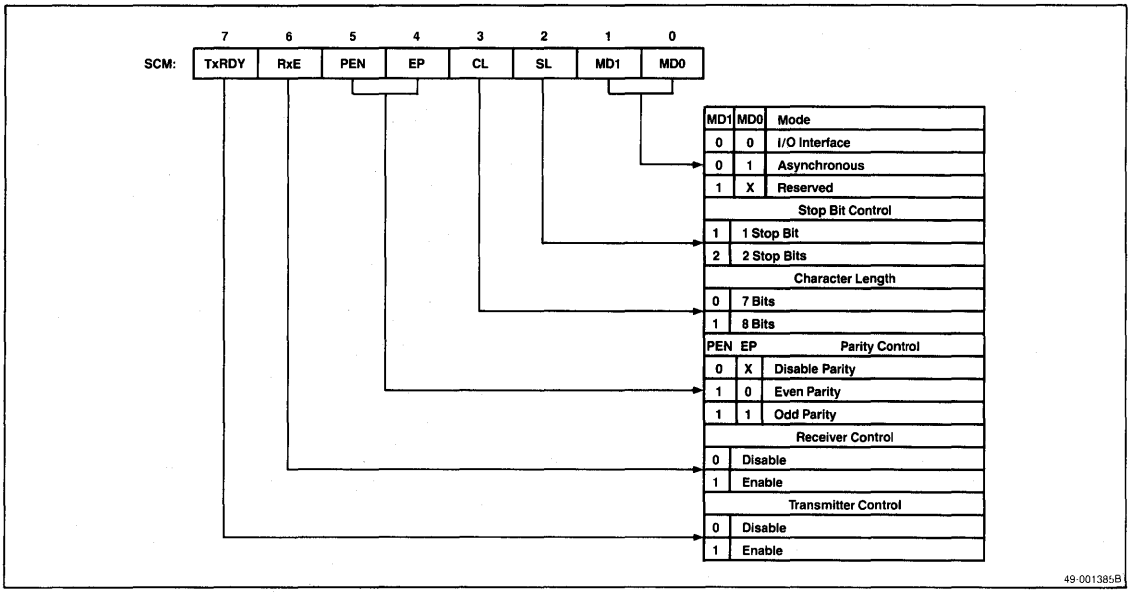
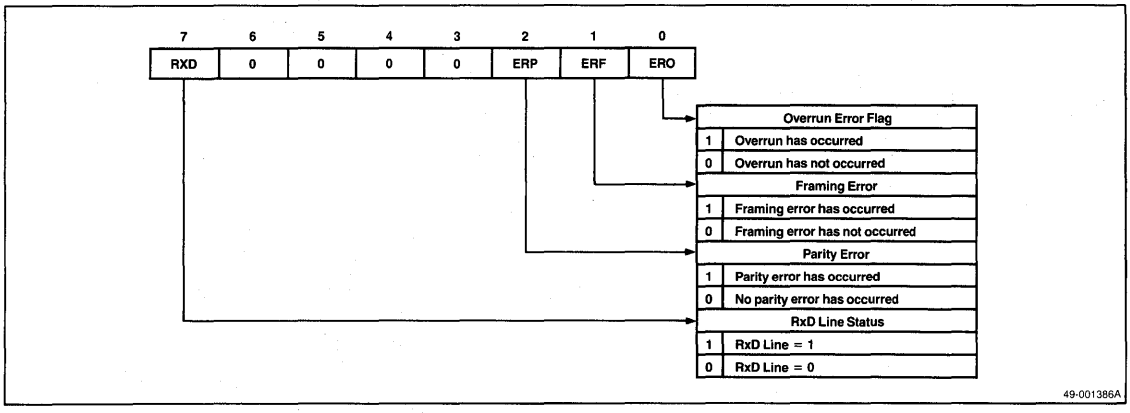
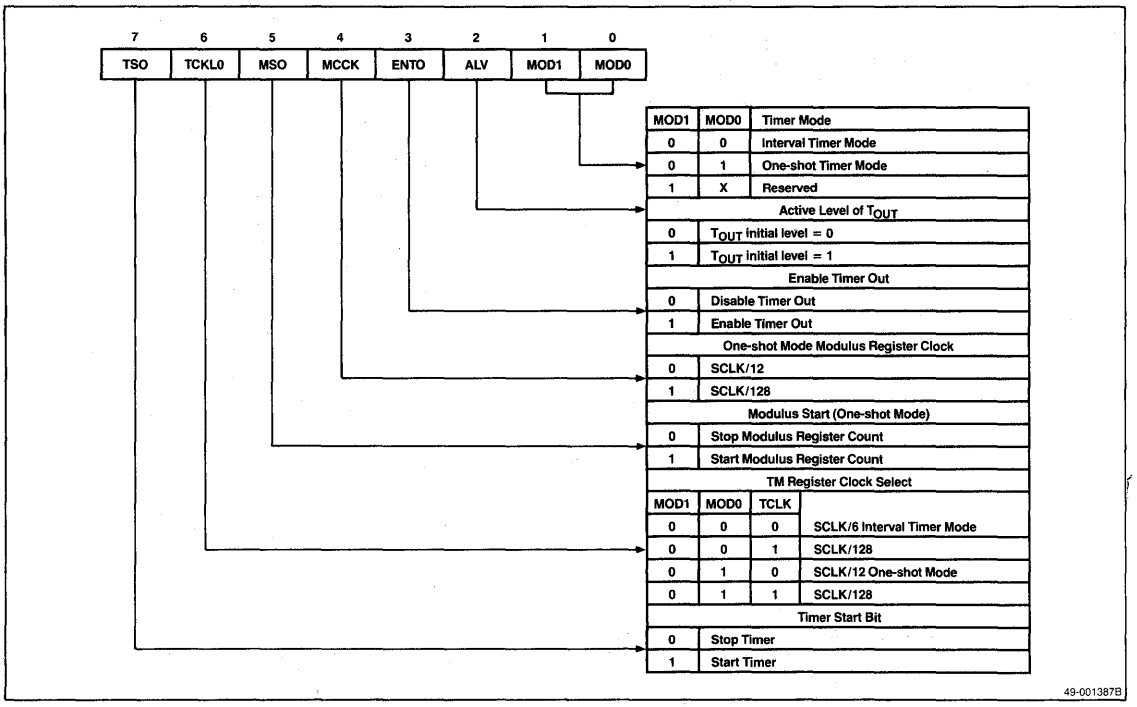


Figure 22. Serial Communication Error Registers



5

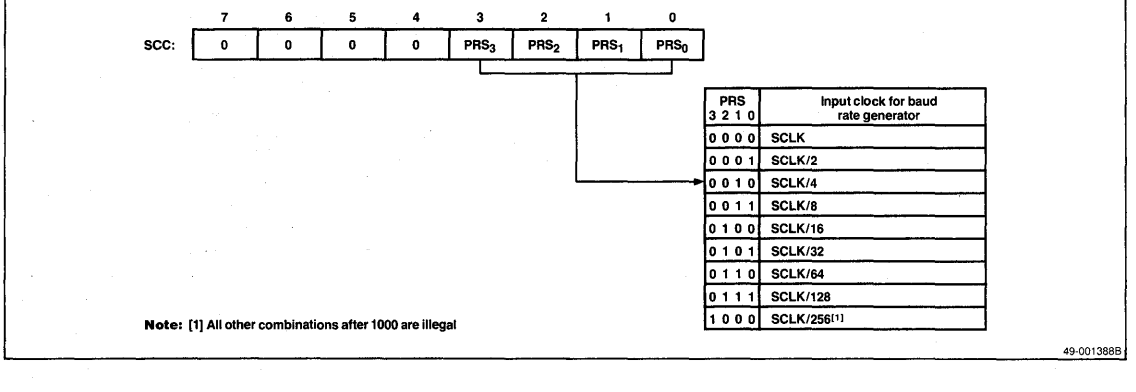
Figure 23. Timer Control 0 Register



MOD1	MOD0	Timer Mode
0	0	Interval Timer Mode
0	1	One-shot Timer Mode
1	X	Reserved
Active Level of T_{OUT}		
0	T_{OUT} initial level = 0	
1	T_{OUT} initial level = 1	
Enable Timer Out		
0	Disable Timer Out	
1	Enable Timer Out	
One-shot Mode Modulus Register Clock		
0	SCLK/12	
1	SCLK/128	
Modulus Start (One-shot Mode)		
0	Stop Modulus Register Count	
1	Start Modulus Register Count	
TM Register Clock Select		
MOD1	MOD0	TCLK
0	0	0 SCLK/6 Interval Timer Mode
0	0	1 SCLK/128
0	1	0 SCLK/12 One-shot Mode
0	1	1 SCLK/128
Timer Start Bit		
0	Stop Timer	
1	Start Timer	

49-001387B

Figure 24. Serial Communication Control Register



PRS 3 2 1 0	Input clock for baud rate generator
0 0 0 0	SCLK
0 0 0 1	SCLK/2
0 0 1 0	SCLK/4
0 0 1 1	SCLK/8
0 1 0 0	SCLK/16
0 1 0 1	SCLK/32
0 1 1 0	SCLK/64
0 1 1 1	SCLK/128
1 0 0 0	SCLK/256[1]

Note: [1] All other combinations after 1000 are illegal

49-001388B

Figure 25. Timer Control 1 Register

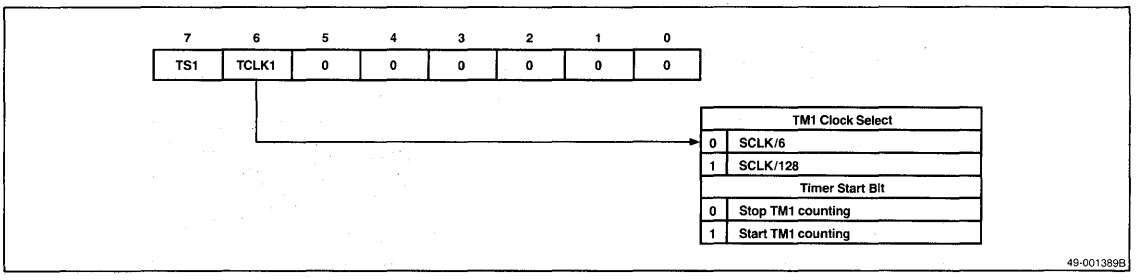


Figure 26. DMA Mode Registers

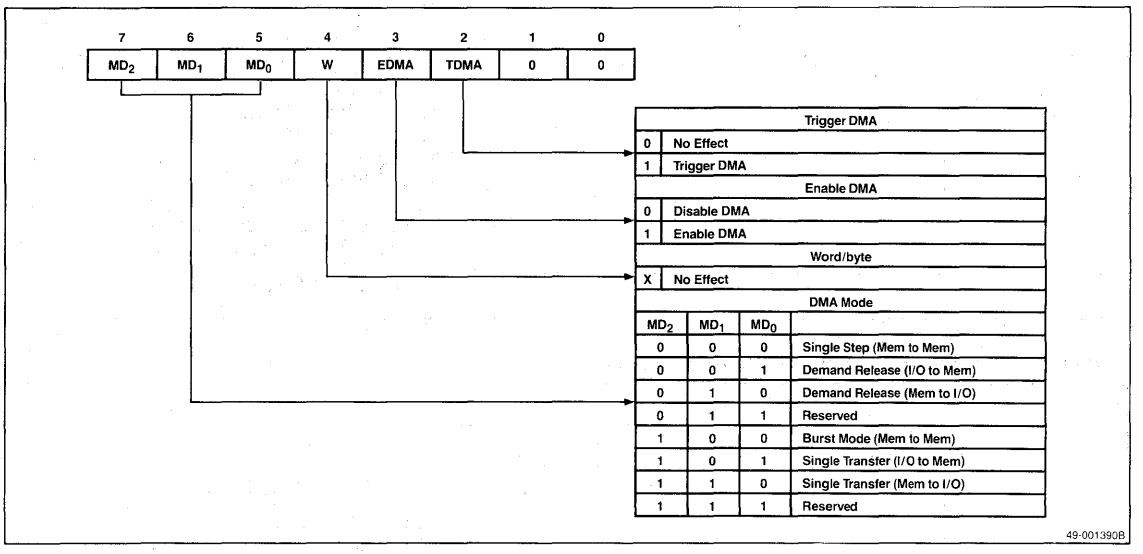


Figure 27. DMA Control Register

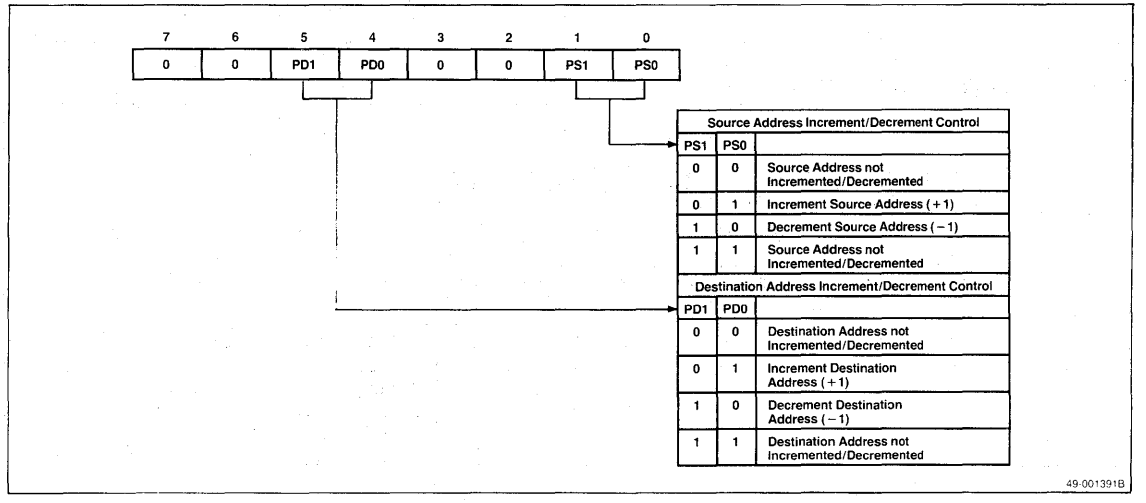


Figure 28. Refresh Mode Register

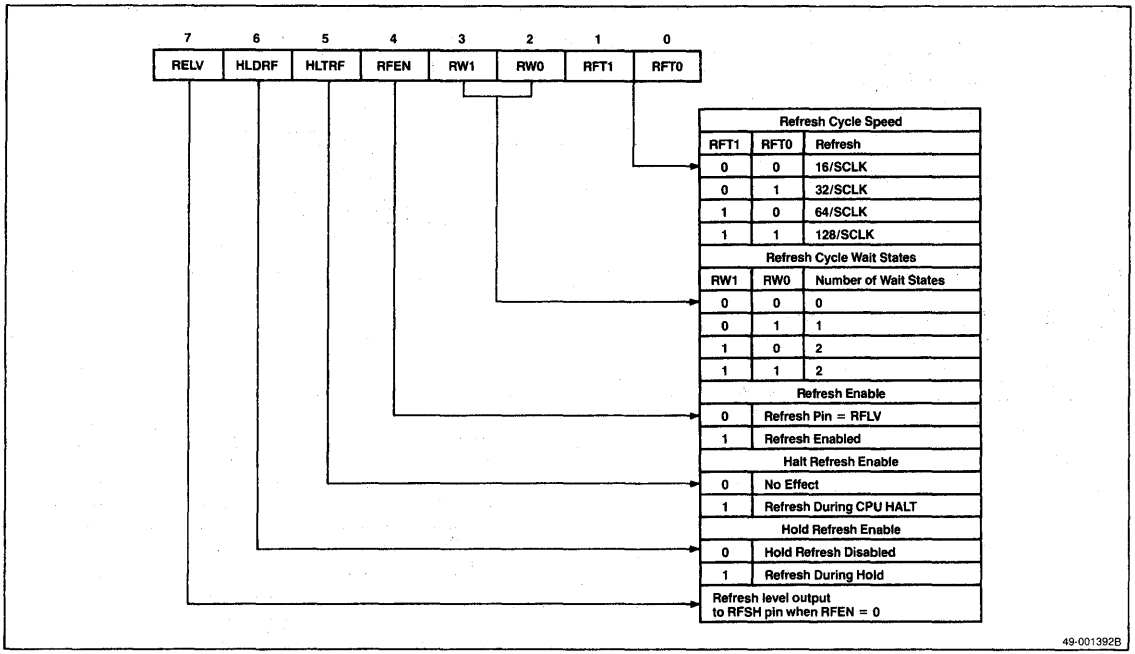


Figure 29. Time Base I/O Request Control Register

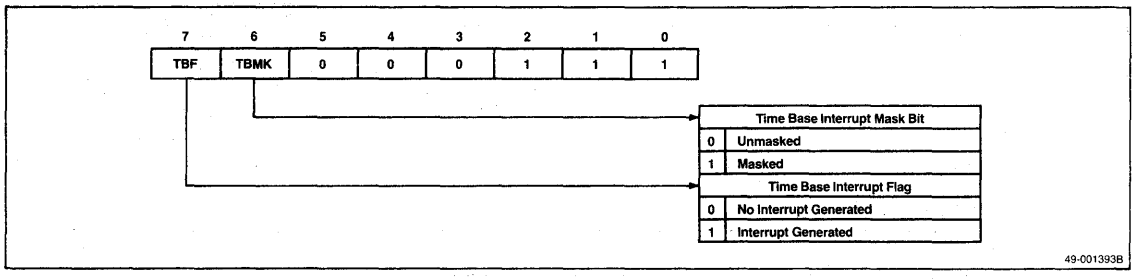


Figure 30. Wait Control Register

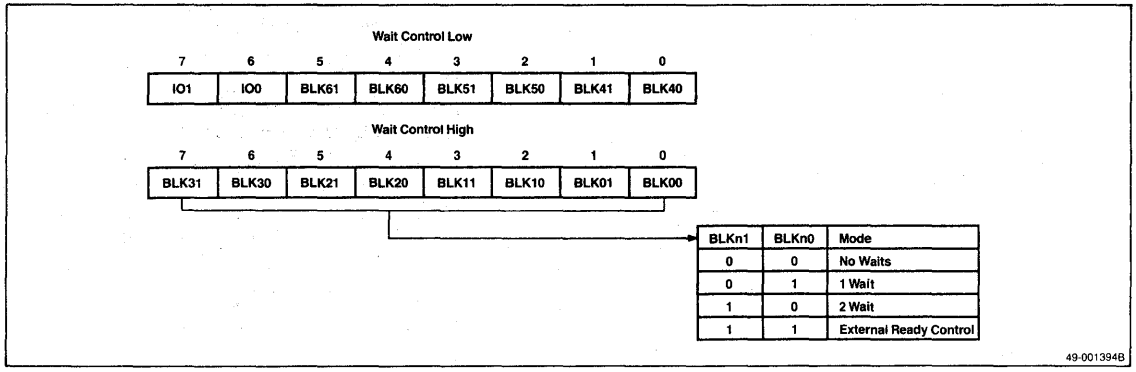


Figure 31. Processor Control Register

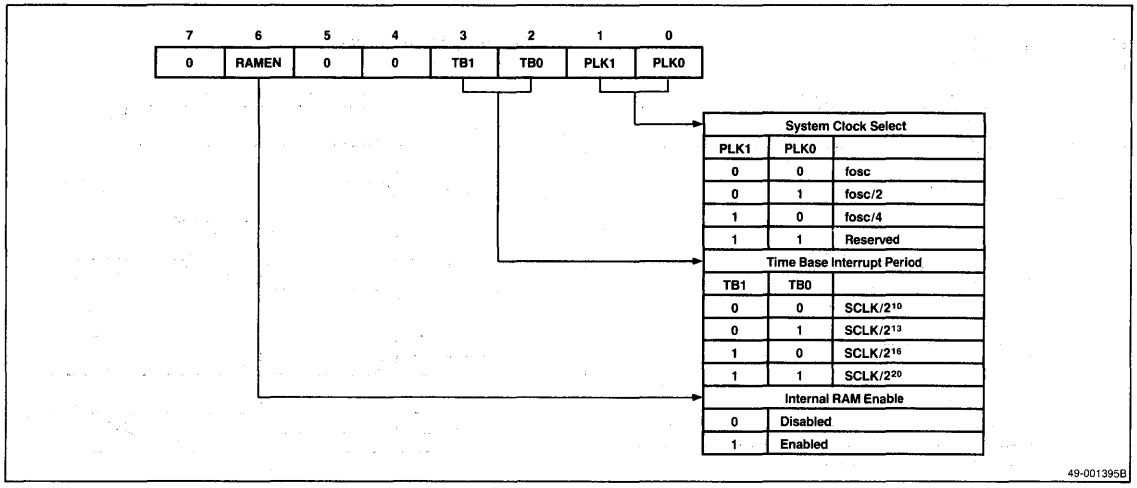
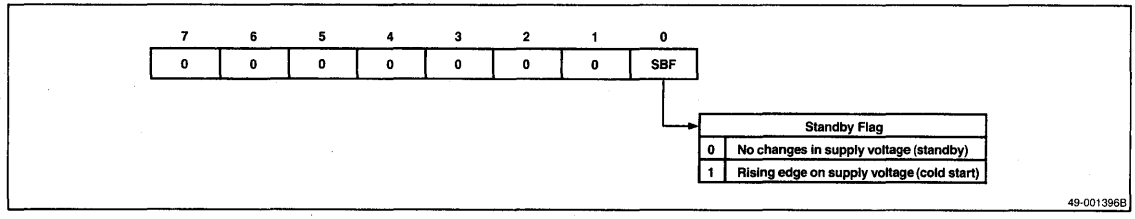


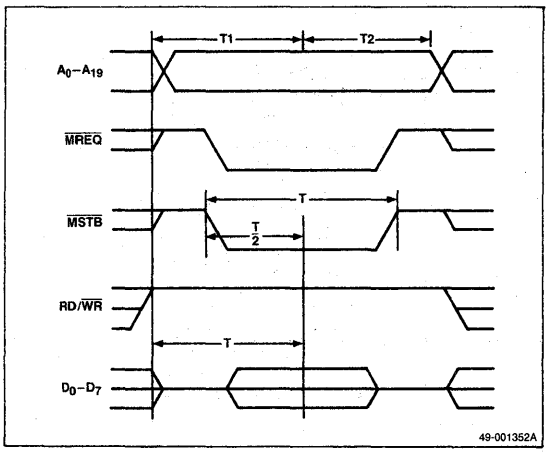
Figure 32. Standby Register



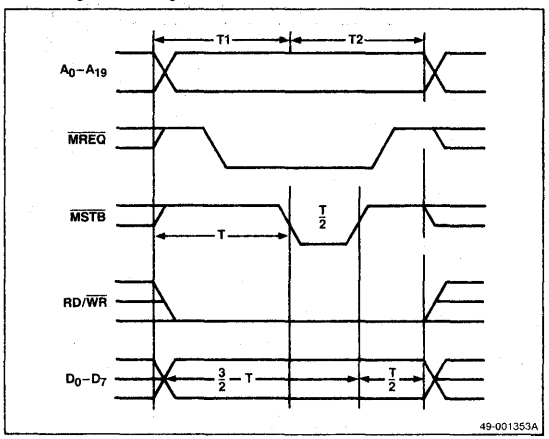
5

Timing Waveforms

Memory Read Cycle



Memory Write Cycle



LCD PERIPHERALS 6

Section 6 — LCD Peripherals

Description

The μPD6307 can directly drive any multiplexed LCD organized with up to 32 rows. It is easily cascaded to 128 rows.

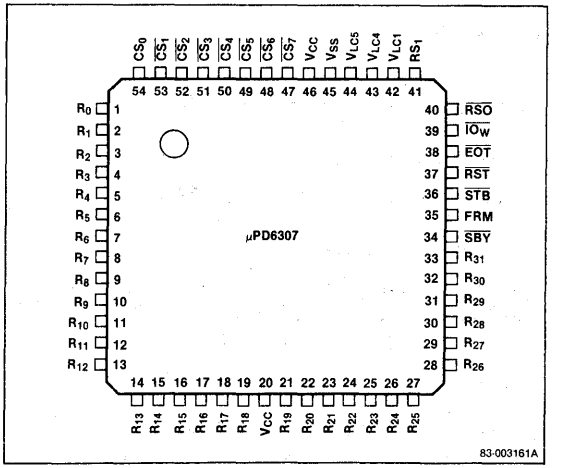
Features

- ☐ High voltage output 21 V maximum
- ☐ Directly controllable by the μPD72030
- ☐ CMOS technology
- ☐ Single 5 V ±10% power supply

Ordering Information

Part Number	Package Type
μPD6307G-F	54-pin plastic miniflat
μPD6307G-R	54-pin plastic miniflat (inverted leads)

Pin Configuration



Pin Identification

No.	Symbol	Function
1-19, 21-23	R_0-R_{31}	Row drive output
20	V_{CC}	Positive power supply
34	$\overline{SBY}$	Standby input
35	FRM	Frame input
36	STB	Strobe input
37	$\overline{RST}$	Reset input
38	$\overline{EOT}$	End of transfer input
39	$\overline{IOW}$	I/O write input
40, 41	RS_0, RS_1	Row select input
42-44	V_{LC1}, V_{LC4}, V_{LC5}	LCD drive supply
45	V_{SS}	Ground
46	V_{CC} (= V_{LC0})	Positive power supply and LCD drive supply
47-54	$\overline{CS_7}$-$\overline{CS_0}$	Chip select output

6

Pin Functions

R_0-R_{31} (Row Drive Output)

LCD row drive output.

$\overline{CS_0}$-$\overline{CS_7}$ (Chip Select)

Column driver chip select. These outputs are generated by the CS counter and RS_0-RS_1.

V_{LC1}, V_{LC4}, V_{LC5} (LCD Drive Supply)

Reference voltages used to drive R_0-R_{31}.

RS_0, RS_1 (Row Select)

This input selects the row driver cascade connection. It enables expansion to 128 row drive outputs and 32 $\overline{CS}$ outputs, as shown in table 1.

FRM (Frame)

A high level input to this pin displays a positive frame and a low level input displays a negative frame. At the falling or rising edge of the signal, the row counter is cleared and the row driver is started from R_0.

STB (Strobe)

Row drive strobe input. One STB pulse input at the timing interval causes the display of the next row.

$\overline{IOW}$ (I/O Write)

This input increments the CS counter signal following 10 low level $\overline{IOW}$ pulses.

$\overline{EOT}$ (End of Transfer)

This input clears the CS counter when it goes active low.

$\overline{RST}$ (Reset)

This is the row driver reset input. A low input clears the internal counter and row outputs R_0-R_{31}, and sets the CS_0-CS_7 outputs to a high level.

$\overline{SBY}$ (Standby)

This is the standby input. A low level input to this pin sets the row outputs R_0-R_{31} to V_{LC0}. Before entering standby mode, set all column driver display data to high level.

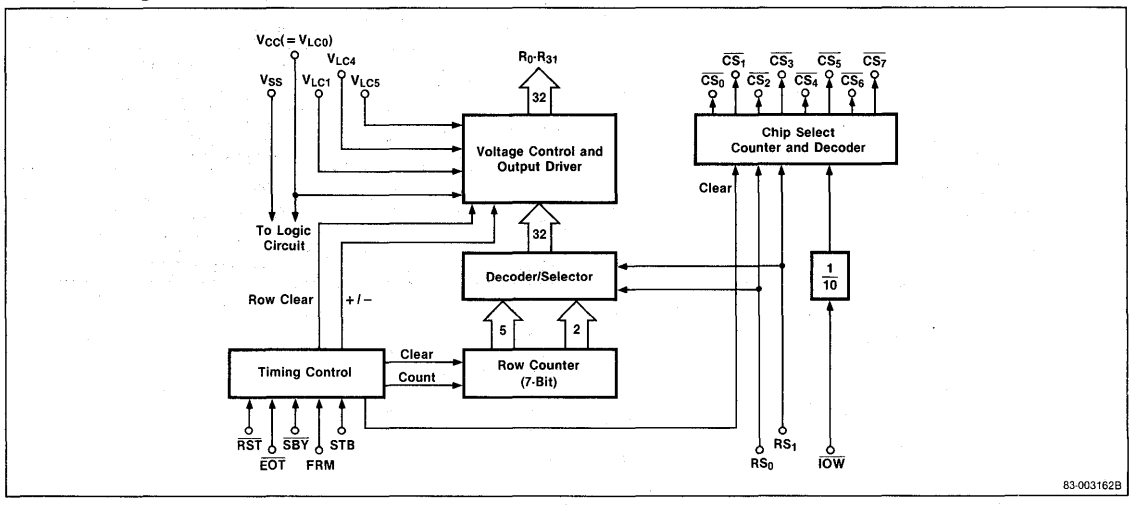
V_{CC} (= V_{LC0}) (Power Supply and LCD Drive Supply)

Connect the 5 V power supply between V_{CC} and V_{SS} for logic circuit operation. This pin is also used for the row drive voltage output.

V_{SS} (Ground)

Ground.

Block Diagram



Functional Description

Timing Control Circuit

This circuit controls the timing for each internal block. FRM, RS_0, RS_1, $\overline{RST}$, and $\overline{SBY}$ are sampled at the leading edge of STB, and then supplied to other internal circuits.

Row Counter Decoder/Select Circuit

As shown in figure 1, this circuit consists of a 7-bit counter, a comparator, and a 5 to 32 decoder. The 7-bit counter can accommodate 128 rows. The comparator acts to clear R_0-R_{31} if the upper two bits of the counter do not match RS_0 and RS_1. If they match, one of R_0-R_{31}, indicated by the lower five bits of the row counter, is selected and the rest are cleared. RS_0 and RS_1 allow for cascading as shown in table 1. Table 2 shows the row select logic.

Figure 1. Row Counter Decoder/Select Circuit

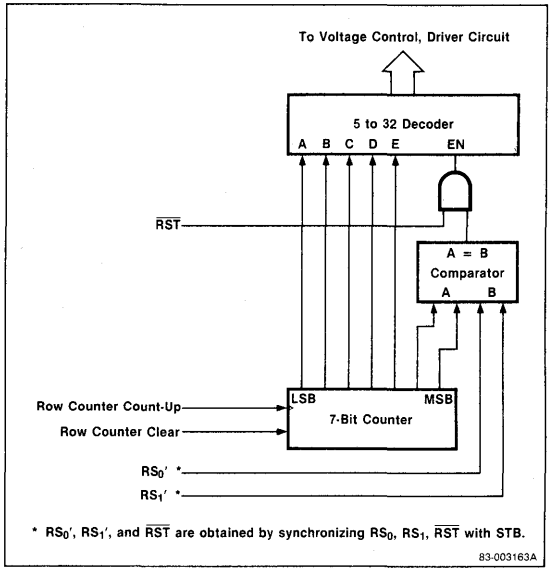


Table 1. RS_0 and RS_1 Row Cascading

RS_0	RS_1	Row Signal	Chip Select
0	0	R_0-R_{31}	$\overline{CS}_0$-$\overline{CS}_7$
0	1	R_{32}-R_{63}	$\overline{CS}_8$-$\overline{CS}_{15}$
1	0	R_{64}-R_{95}	$\overline{CS}_{16}$-$\overline{CS}_{23}$
1	1	R_{96}-R_{127}	$\overline{CS}_{24}$-$\overline{CS}_{31}$

Table 2. Row Select Logic

EN	E	D	C	B	A	Selected Row Signal
1	0	0	0	0	0	R_0
1	0	0	0	0	1	R_1
1	↓	↓	↓	↓	↓	R_n
1	1	1	1	1	0	R_{30}
1	1	1	1	1	1	R_{31}
0	X	X	X	X	X	None

Voltage Control Driver Circuit

This circuit generates the row signals for AC drive of the LCD panel. A low level $\overline{RST}$ clears the output. A low level $\overline{SBY}$ sets the output V_{LC0}. Table 2 shows the R_0-R_{31} output levels.

Table 2. R_0-R_{31} Outputs Levels

Function	+ (FRM = 1)	− (FRM = 0)
Select	V_{LC5}	V_{LC0}
Clear	V_{LC4}	V_{LC1}

Chip Select Counter/Decoder Circuit

This circuit, shown in figure 2, generates the column driver $\overline{CS}$ signal. This circuit has a 5-bit counter to generate up to 32 $\overline{CS}$ signals. The 5-bit counter is incremented once for every 10 $\overline{IOW}$ (active low) pulses. If the upper two bits of the chip select counter do not match RS_0 and RS_1, all the $\overline{CS}_0$-$\overline{CS}_7$ outputs are set to high level. If they match, one of $\overline{CS}_0$-$\overline{CS}_7$ (indicated by the lower three bits of the chip select counter) goes low. If $\overline{RST}$ is low, $\overline{CS}_0$-$\overline{CS}_7$ become high level. Table 3 shows the chip select logic.

6

Figure 2. Chip Select Counter/Decoder Circuit

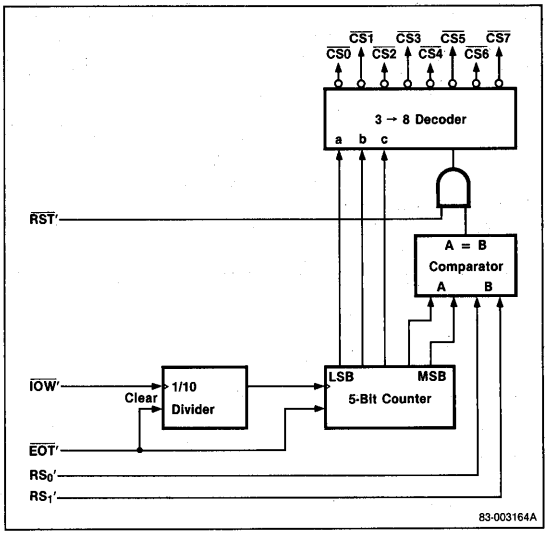


Table 3. Chip Select Logic

EN	c	b	a	Chip Select
1	0	0	0	$\overline{CS}_0$
1	0	0	1	$\overline{CS}_1$
1	0	1	0	$\overline{CS}_2$
1	0	1	1	$\overline{CS}_3$
1	1	0	0	$\overline{CS}_4$
1	1	0	1	$\overline{CS}_5$
1	1	1	0	$\overline{CS}_6$
1	1	1	1	$\overline{CS}_7$
0	X	X	X	Disabled

μPD6308
LCD COLUMN DRIVER

PRELIMINARY INFORMATION

Description

The μPD6308 can directly drive any multiplexed dot-matrix LCD organized with up to 40 columns. It is easily cascaded to fit the user's system.

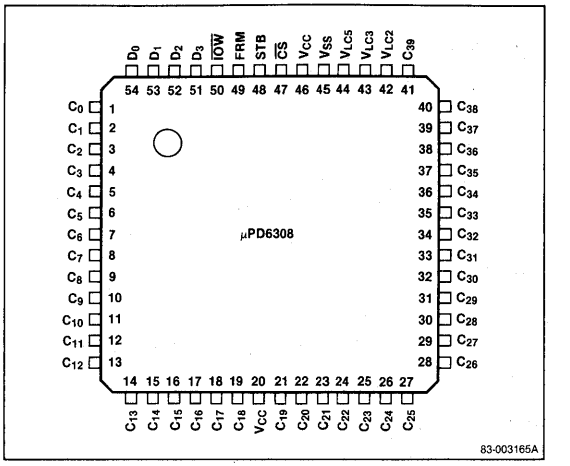
Features

- ☐ High voltage output 21 V maximum
- ☐ Directly controllable by the μPD72030
- ☐ CMOS technology
- ☐ Single 5 V ±10% power supply

Ordering Information

Part Number	Package Type
μPD6308G-F	54-pin plastic miniflat
μPD6308G-R	54-pin plastic miniflat (inverted leads)

Pin Configuration



Pin Identification

No.	Symbol	Function
1-19, 21-41	C_0-C_{39}	Column drive output
20	V_{CC}	Positive power supply
42-44	V_{LC2}, V_{LC3}, V_{LC5}	LCD drive supply
45	V_{SS}	Ground
46	V_{CC} (=V_{LC0})	Positive power supply and LCD drive supply
47	$\overline{CS}$	Chip select output
48	STB	Strobe input
49	FRM	Frame input
50	$\overline{IOW}$	I/O write input
51-54	D_3-D_0	Data input

6

Pin Functions

C_0-C_{39} (Column Drive Output)

LCD column drive output.

V_{LC2}, V_{LC3}, V_{LC5} (LCD Drive Supply)

Reference voltages used to drive C_0-C_{39}.

D_0-D_3 (Data Input)

This is the display data bus. Data in the 40-bit input latch is written via this bus four bits at a time, a total of 10 times.

FRM (Frame)

A high level input to this pin displays the positive frame and a low level input displays the negative frame.

STB (Strobe)

This is the column driver strobe input. At the leading edge of the STB input, the 40-bit display data in the input latch is transferred to the output latch to appear in the column drive output.

$\overline{IOW}$ (I/O Write)

This is the data write input. If $\overline{CS}$ is active and $\overline{IOW}$ goes low, data on D_0-D_3 is written to the input latch.

$\overline{CS}$ (Chip Select)

This input pin is connected to the chip select output of the row driver as the $\overline{IOW}$ enable. $\overline{CS}$ is active low.

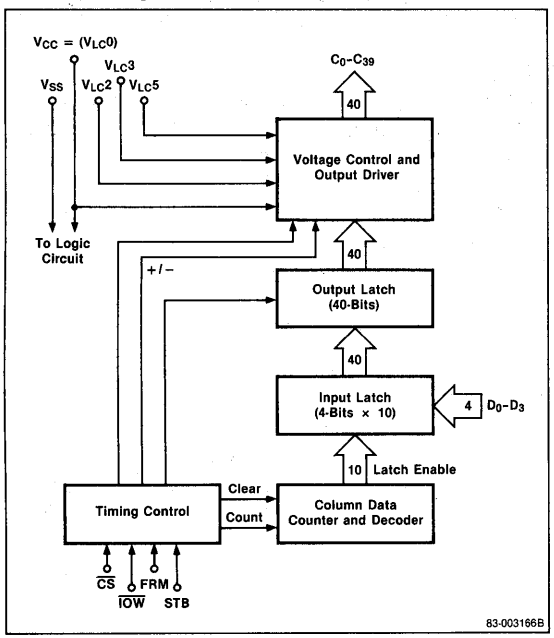
V_{CC} (= V_{LC0}) (Power Supply and LCD Drive Supply)

Connect the 5 V power supply between V_{CC} and V_{SS}. V_{CC} is also used for the column drive voltage.

V_{SS} (Ground)

Ground.

Block Diagram



Functional Description

Timing Control Circuit

This circuit controls the timing that operates each μPD6308 internal block.

Voltage Control Driver Circuit

This circuit generates the column signals for AC drive of the LCD panel. Table 1 lists C_0-C_{39} output levels. FRM' is obtained by internally synchronizing the FRM signal with the leading edge of the STB signal.

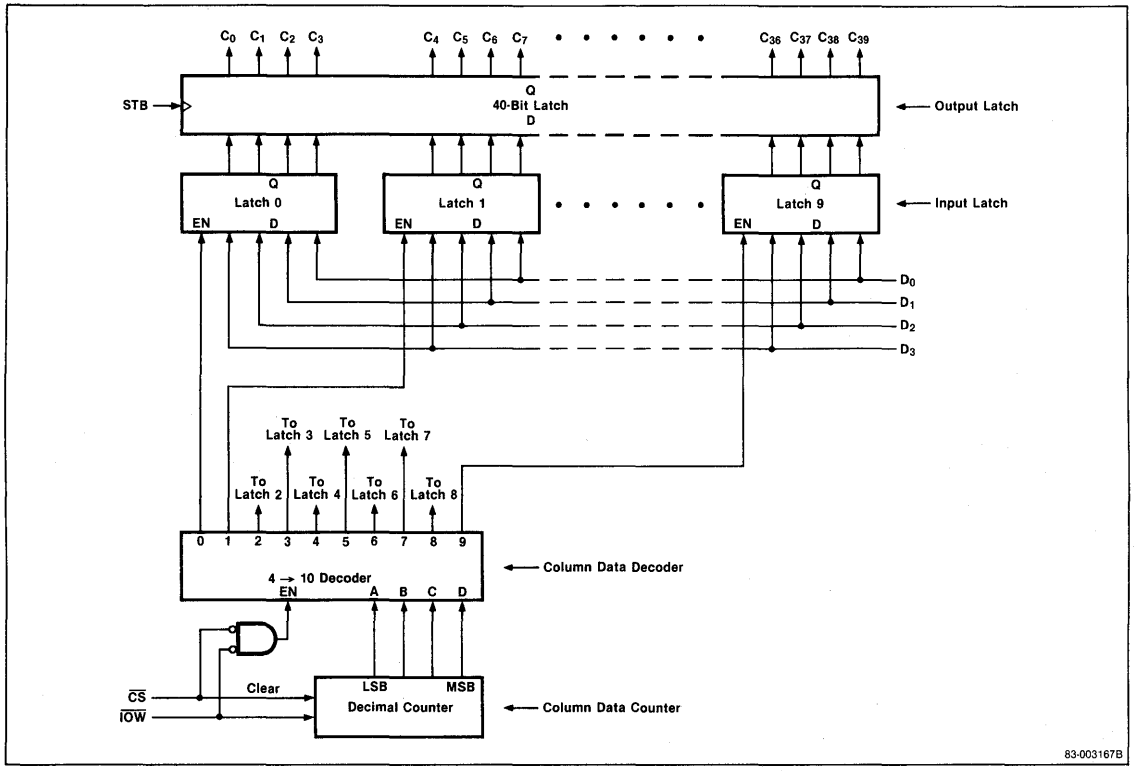
Table 1. C_0-C_{39} Output Levels

Function	+ (FRM' = 1)	− (FRM' = 0)
Select (Data = 1)	V_{LC5}	V_{LC0}
Clears (Data = 0)	V_{LC3}	V_{LC2}

Column Data Counter/Decoder Circuit

The column data counter/decoder circuit is shown in figure 1. This decimal circuit generates latch enable pulses to the input latches, which latch 40 bits of data (four bits at a time, a total of 10 times). The number of decoder outputs can be increased by cascading μPD6308s under the control of $\overline{CS}$. The counter value increments at the leading edge of $\overline{IOW}$, and clears when $\overline{CS}$ goes high.

Figure 1. Internal Block Diagram



Input Latch Circuit

The input latch circuit is shown in figure 1. The input latches display data four bits at a time until 40 bits are latched and displayed. When $\overline{CS}$ is active low, each $\overline{IOW}$ active low pulse input to the decimal counter causes 1 of 10 latch enable signals to be generated from the column data decoder. Latches 0 to 9 are enabled consecutively to load data D_0-D_3 until 40 bits are latched.

Output Latch Circuit

The output latch circuit is shown in figure 1. The 40 bits output from the input latch circuit are transferred to the output latch circuit at the leading edge of the STB signal and appear on the column drive outputs. Note that D_0 is output to C_3, D_1 to C_2, D_2, to C_1, and D_3 to C_0.

6

μPD7225
CMOS, INTELLIGENT, ALPHANUMERIC LCD CONTROLLER/DRIVER

Description

The μPD7225 is an intelligent peripheral device designed to interface most microprocessors with a wide variety of alphanumeric LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 32 segments and is easily cascaded for larger LCD applications. The μPD7225 communicates with a host microprocessor through an 8-bit serial interface. It includes a 7-segment numeric and a 14-segment alphanumeric segment decoder to reduce system software requirements. The μPD7225 is manufactured with a low power consumption CMOS process allowing use of a single power supply between 2.7 V and 5.5 V. It is available in a space-saving 52-pin plastic flat package.

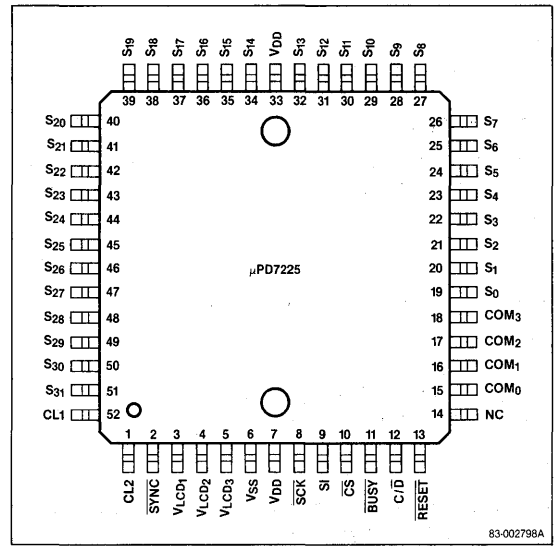
Features

- ☐ Single chip LCD controller with direct LCD drive
- ☐ Low cost serial interface to most microprocessors
- ☐ Compatible with
  - — 7-segment numeric LCD configurations up to 16 digits
  - — 14-segment alphanumeric LCD configurations up to 8 characters
- ☐ Selectable LCD drive configuration:
  - — Static, biplexed, triplexed, or quadruplexed
- ☐ 32-segment drivers
- ☐ Cascadable for larger LCD applications
- ☐ Selectable LCD bias voltage configuration:
  - — Static, 1/2 or 1/3
- ☐ Hardware logic blocks reduce system software requirements
  - — 8-bit serial interface
  - — Two 32 × 4-bit static RAMs for display data and blinking data storage
  - — Programmable segment decoding capability:
    - 16-character, 7-segment numeric decoder
    - 64-character, 14-segment USASCII alphanumeric decoder
  - — Programmable segment blinking capability
  - — Automatic synchronization of segment drivers with sequentially multiplexed backplane drivers
- ☐ Single power supply, variable from 2.7 V to 5.5 V
- ☐ Low power consumption CMOS technology
- ☐ Extended −40°C to +85°C temperature range available

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7225G-00	52-pin plastic miniflat	1 MHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	CL2	System clock output
2	$\overline{SYNC}$	Synchronization port
3–5	V_{LCD1}–V_{LCD3}	LCD bias voltage supply inputs
6	V_{SS}	Ground
7, 33	V_{DD}	Power
8	$\overline{SCK}$	Serial clock input
9	SI	Serial input
10	$\overline{CS}$	Chip select
11	$\overline{BUSY}$	Busy output
12	C/$\overline{D}$	Command or data select input
13	$\overline{RESET}$	Reset input
14	NC	No connection
15–18	COM_0–COM_3	LCD backplane driver outputs
19–32, 34–51	S_0–S_{31}	LCD segment driver outputs
52	CL1	System clock input

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Pin Functions

COM_0-COM_3

LCD backplane driver outputs.

S_0-S_{31}

LCD segment driver outputs.

V_{LCD1}-V_{LCD3}

LCD bias voltage supply inputs to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across V_{DD}.

SI

Serial input from the microprocessor.

$\overline{SCK}$

Serial clock input. Synchronizes 8-bit serial data transfer from the microprocessor to the μPD7225.

$\overline{BUSY}$

Handshake output indicates the μPD7225 is ready to receive the next data byte.

C/$\overline{D}$

Command/data select input. Distinguishes serially input data byte as a command or as display data.

$\overline{CS}$

Chip select input. Enables the μPD7225 for data input from the microprocessor. When $\overline{CS}$ is deselected, the display can be updated.

$\overline{SYNC}$

Synchronization port. For multichip operation, tie all $\overline{SYNC}$ lines together.

CL1

System clock input. Connect CL1 either to CL2 with a 180 kΩ resistor, or to an external clock source.

CL2

System clock output. Connect CL2 to CL1 with a 180 kΩ resistor, or leave open.

$\overline{RESET}$

Reset input. R/C circuit or pulse initializes the μPD7225 after power-up.

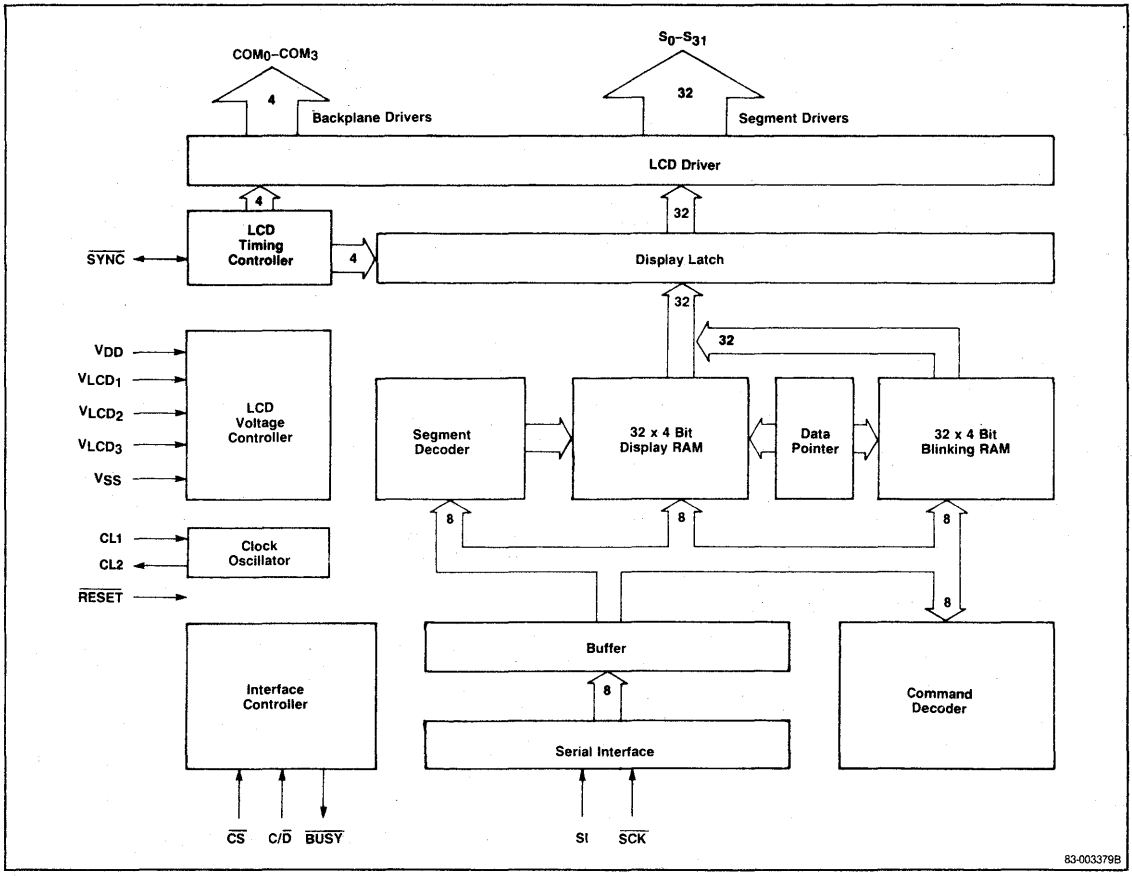
V_{DD}

Power supply positive. Apply single voltage ranging from 2.7 to 5.5 V for proper operation.

V_{SS}

Ground.

Block Diagram



6

Absolute Maximum Ratings

$T_A = 25°C$

Power supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	−0.3 V to V_{DD} +0.3 V
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	0		0.3 V_{DD}	V	
Input voltage high	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Output voltage low	V_{OL1}			0.5	V	$\overline{BUSY}$, $I_{OL} = 100\,\mu A$
	V_{OL2}			1.0	V	$I_{OL} = 900\,\mu A$, $\overline{SYNC}$
Output voltage high	V_{OH}	V_{DD} −0.5			V	$\overline{BUSY}$, $\overline{SYNC}$, $I_{OH} = -10\,\mu A$
Input leakage current low	I_{LIL}			−2	μA	$V_{IL} = 0\,V$
Input leakage current high	I_{LIH}			2	μA	$V_{IH} = V_{DD}$
Output leakage current	I_{LOL}			−2	μA	$V_{OL} = 0\,V$
	I_{LOH}			2	μA	$V_{OH} = V_{DD}$
Output short circuit current	I_{OS}			−300	μA	$\overline{SYNC}$, $V_{OS} = 1.0\,V$
Backplane driver output impedance	R_{COM}		5	7	kΩ	COM_0–COM_3, $V_{DD} \geq V_{LCD}$ (Note 1)
Segment driver output impedance	R_{SEG}		7	14	kΩ	S_0–S_{31}, $V_{DD} \geq V_{LCD}$ (Note 1)
Supply current	I_{DD}		100	250	μA	CL1 external clock, $f_\phi = 200$ kHz

Note:
(1) Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes.

DC Characteristics (cont)

$T_A = -0°C$ to $+70°C$, $V_{DD} = +2.7\,V$ to $5.5\,V$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL1}	0		0.3 V_{DD}	V	Except $\overline{SCK}$
	V_{IL2}	0		0.2 V_{DD}	V	$\overline{SCK}$
Input voltage high	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except $\overline{SCK}$
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{SCK}$
Output voltage low	V_{OL1}			0.5	V	$\overline{BUSY}$, $I_{OL} = 100\,\mu A$
	V_{OL2}			0.5	V	$I_{OL} = 400\,\mu A$, $\overline{SYNC}$
Output voltage high	V_{OH}	V_{DD} −0.75			V	$\overline{BUSY}$, $\overline{SYNC}$, $I_{OH} = -7\,\mu A$
Input leakage current low	I_{LIL}			−2	μA	$V_{IL} = 0\,V$
Input leakage current high	I_{LIH}			2	μA	$V_{IH} = V_{DD}$
Output leakage current	I_{LOL}			−2	μA	$V_{OL} = 0\,V$
	I_{LOH}			2	μA	$V_{OH} = V_{DD}$
Output short circuit current	I_{OS}			−200	μA	$\overline{SYNC}$, $V_{OS} = 0.5\,V$
Backplane driver output impedance	R_{COM}		6		kΩ	COM_0–COM_3, $V_{DD} \geq V_{LCD}$ (Note 1)
Segment driver output impedance	R_{SEG}		12		kΩ	S_0–S_{31}, $V_{DD} \geq V_{LCD}$ (Note 1)
Supply current	I_{DD}		30	100	μA	CL1 external clock, $V_{DD} = 3.0\,V \pm 10\%$, $f_\phi = 140$ kHz

Note:
(1) Applies to static-, 1/2-, and 1/3-LCD bias voltage schemes.

Capacitance

$T_A = 25°C$, $f_\phi = 1$ MHz

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions(1)
Input capacitance	C_I			10	pF	
Output capacitance	C_{O1}			20	pF	Except $\overline{BUSY}$
	C_{O2}			15	pF	$\overline{BUSY}$
I/O capacitance	C_{IO}			15	pF	$\overline{SYNC}$
Clock capacitance	C_ϕ			30	pF	CL1 input

Note:
(1) All unmeasured pins returned to 0 V.

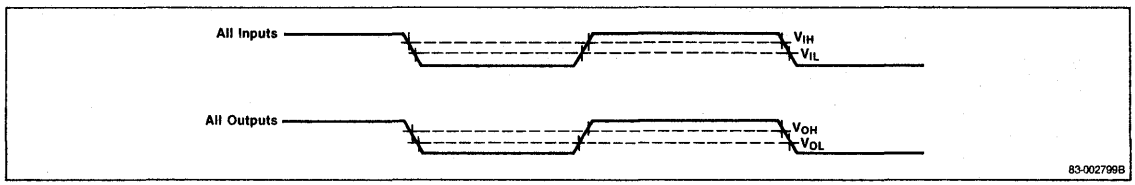
AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock frequency	f_ϕ	50		200	kHz	
	f_{OSC}	85	130	175	kHz	$R = 180\,k\Omega \pm 5\%$
Clock pulse width low	$t_{\phi WL}$	2		16	μs	CL1, external clock
Clock pulse width high	$t_{\phi WH}$	2		16	μs	CL1, external clock
$\overline{SCK}$ cycle	t_{CYK}	900			ns	
$\overline{SCK}$ pulse width low	t_{KWL}	400			ns	
$\overline{SCK}$ pulse width high	t_{KWH}	400			ns	
$\overline{BUSY}$ ↑ to $\overline{SCK}$ ↓ hold time	t_{BHK}	0			ns	
SI setup time to $\overline{SCK}$ ↑	t_{ISK}	100			ns	
SI hold time after $\overline{SCK}$ ↑	t_{IHK}	200			ns	
8th $\overline{SCK}$ ↑ to $\overline{BUSY}$ ↓ delay time	t_{KDB}			3	μs	$C_L = 50\,pF$
$\overline{CS}$ ↓ to $\overline{BUSY}$ ↓ delay time	t_{CDB}			1.5	μs	$C_L = 50\,pF$
C / $\overline{D}$ setup time to 8th $\overline{SCK}$ ↑	t_{DSK}	9			μs	
C / $\overline{D}$ hold time after 8th $\overline{SCK}$ ↑	t_{DHK}	1			μs	
$\overline{CS}$ hold time after 8th $\overline{SCK}$ ↑	t_{CHK}	1			μs	
$\overline{CS}$ pulse width low	t_{CWL}	$8/f_\phi$			μs	
$\overline{CS}$ pulse width high	t_{CWH}	$8/f_\phi$			μs	

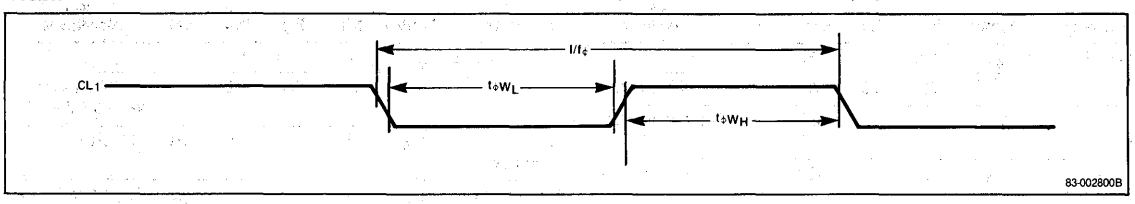
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock frequency	f_ϕ	50		140	kHz	
	f_{OSC}	50	100	140	kHz	$R = 180\,k\Omega + 5\%$, $V_{DD} = 3.0\,V \pm 10\%$
Clock pulse width low	$t_{\phi WL}$	3		16	μs	CL1, external clock
Clock pulse width high	$t_{\phi WH}$	3		16	μs	CL1, external clock
$\overline{SCK}$ cycle	t_{CYK}	4			μs	
$\overline{SCK}$ pulse width low	t_{KWL}	1.8			μs	
$\overline{SCK}$ pulse width high	t_{KWH}	1.8			μs	
$\overline{BUSY}$ ↑ to $\overline{SCK}$ ↓ hold time	t_{BHK}	0			ns	
SI setup time to $\overline{SCK}$ ↑	t_{ISK}	1			μs	
SI hold time after $\overline{SCK}$ ↑	t_{IHK}	1			μs	
8th $\overline{SCK}$ ↑ to $\overline{BUSY}$ ↓ delay time	t_{KDB}			5	μs	$C_L = 50\,pF$
$\overline{CS}$ ↓ to $\overline{BUSY}$ ↓ delay time	t_{CDB}			5	μs	$C_L = 50\,pF$
C / $\overline{D}$ setup time to 8th $\overline{SCK}$ ↑	t_{DSK}	18			μs	
C / $\overline{D}$ hold time after 8th $\overline{SCK}$ ↑	t_{DHK}	1			μs	
$\overline{CS}$ hold time after 8th $\overline{SCK}$ ↑	t_{CHK}	1			μs	
$\overline{CS}$ pulse width low	t_{CWL}	$8/f_\phi$			μs	
$\overline{CS}$ pulse width high	t_{CWH}	$8/f_\phi$			μs	
$\overline{SYNC}$ load capacitance	C_L			50	pF	$f_\phi = 200\,kHz$

AC Timing Characteristics

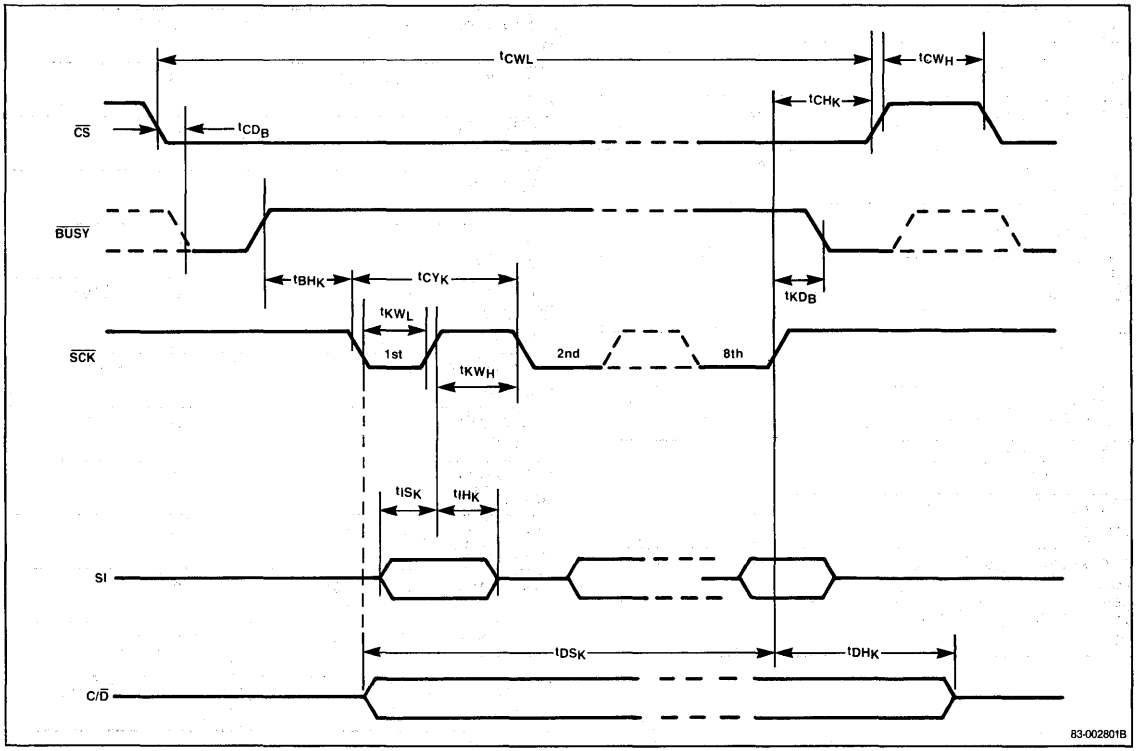


Timing Waveforms

Clock



Serial Interface



Instruction Set (Note 1)

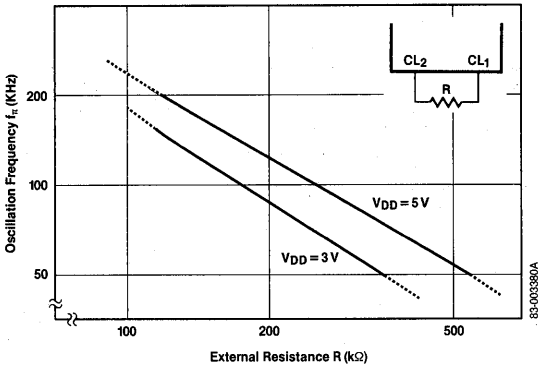
Command	Description	Hex Code	Operation Code							
			D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Mode Set	Initialize the μPD7225, including selection of: 1) LCD drive configuration 2) LCD bias voltage configuration 3) LCD frame frequency	40–5F	0	1	0	d_4	d_3	d_2	d_1	d_0
Unsynchronous Data Transfer	Synchronize display RAM data transfer to display latch with $\overline{CS}$	30	0	0	1	1	0	0	0	0
Synchronous Data Transfer	Synchronize display RAM data transfer to display latch with LCD drive cycle	31	0	0	1	1	0	0	0	1
Interrupt Data Transfer	Interrupt display RAM data transfer to display latch	38	0	0	1	1	1	0	0	0
Load Data Pointer	Load data pointer with 5 bits of immediate data	E0–FF	1	1	1	d_4	d_3	d_2	d_1	d_0
Clear Display RAM	Clear the display RAM and reset the data pointer	20	0	0	1	0	0	0	0	0
Write Display RAM	Write 4 bits of immediate data to the display RAM location addressed by the data pointer; increment data pointer	D0–DF	1	1	0	1	d_3	d_2	d_1	d_0
AND Display RAM	Perform a logical AND between the display RAM data addressed by the data pointer and 4 bits of immediate data; write result to same display RAM location. Increment data pointer	90–9F	1	0	0	1	d_3	d_2	d_1	d_0
OR Display RAM	Perform a logical OR between the display RAM data addressed by the data pointer and 4 bits of immediate data; write result to same display RAM location; increment data pointer	B0–BF	1	0	1	1	d_3	d_2	d_1	d_0
Enable Segment Decoder	Start use of the segment decoder	15	0	0	0	1	0	1	0	1
Disable Segment Decoder	Stop use of the segment decoder	14	0	0	0	1	0	1	0	0
Enable Display	Turn on the LCD	11	0	0	0	1	0	0	0	1
Disable Display	Turn off the LCD	10	0	0	0	1	0	0	0	0
Clear Blinking RAM	Clear the blinking RAM and reset the data pointer	00	0	0	0	0	0	0	0	0
Write Blinking RAM	Write 4 bits of immediate data to the blinking RAM location addressed by the data pointer; increment data pointer	C0–CF	1	1	0	0	d_3	d_2	d_1	d_0
AND Blinking RAM	Perform a logical AND between blinking RAM data addressed by the data pointer and 4 bits of immediate data; write result to same blinking location; increment data pointer	80–8F	1	0	0	0	d_3	d_2	d_1	d_0
OR Blinking RAM	Perform a logical OR between blinking RAM data addressed by the data pointer and 4 bits of immediate data; write result to same blinking location; increment data pointer	A0–AF	1	0	1	0	d_3	d_2	d_1	d_0
Enable Blinking	Start segment blinking at the frequency specified by 1 bit of immediate data	1A–1B	0	0	0	1	1	0	1	d_0
Disable Blinking	Stop segment blinking	18	0	0	0	1	1	0	0	0

Note:
(1) Details of operation and application examples can be found in the μPD7225 Intelligent Alphanumeric LCD Controller/Driver Technical Manual.

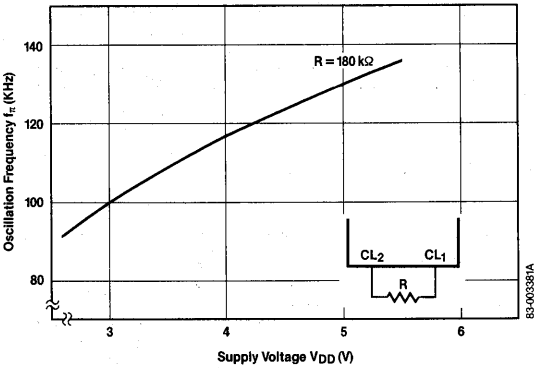
Operating Characteristics

$T_A = 25°C$

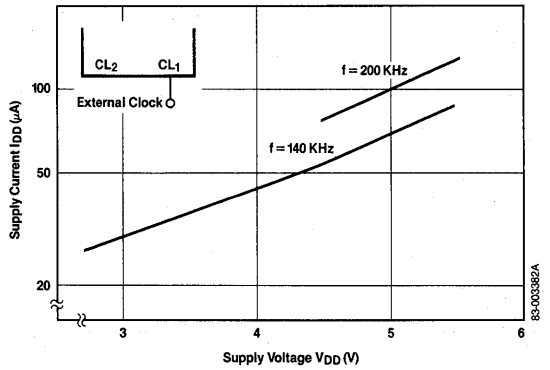
External Resistance vs Oscillation Frequency



Supply Voltage vs Oscillation Frequency



Supply Voltage vs Supply Current



7-Segment Numeric Data Decoder Character Set

Display Byte (HEX)	Character	Decoded Display RAM Data				
		Triplexed			Quadruplexed	
		Display RAM Address			Display RAM Address	
		n+2	n+1	n	n+1	n
00		3	5	3	D	7
01		0	0	3	0	6
02		2	7	1	E	3
03		0	7	3	A	7
04		1	2	3	3	6
05		1	7	2	B	5
06		3	7	2	F	5
07		0	1	3	0	7
08		3	7	3	F	7
09		1	7	3	B	7
0A		3	2	0	2	0
0B		3	7	0	F	1
0C		3	5	0	D	1
0D		0	6	0	A	0
0E		2	6	2	E	4
0F		0	0	0	0	0

14-Segment Alphanumeric Data Decoder Character Set

Display Byte (HEX)	Char.	Display RAM Address n+3	n+2	n+1	n	Display Byte (HEX)	Char.	Display RAM Address n+3	n+2	n+1	n	Display Byte (HEX)	Char.	Display RAM Address n+3	n+2	n+1	n	Display Byte (HEX)	Char.	Display RAM Address n+3	n+2	n+1	n
A0		0	0	0	0	B0		4	7	E	2	C0		A	7	C	0	D0		2	3	6	4
A1			Invalid			B1		0	6	0	0	C1		2	7	6	4	D1		0	7	E	8
A2			Invalid			B2		2	3	C	4	C2		8	7	8	5	D2		2	3	6	C
A3			Invalid			B3		2	7	8	4	C3		0	1	E	0	D3		1	5	8	4
A4			Invalid			B4		2	6	2	4	C4		8	7	8	1	D4		8	1	0	1
A5			Invalid			B5		2	5	A	4	C5		2	1	E	4	D5		0	6	E	0
A6			Invalid			B6		2	5	E	4	C6		2	1	6	4	D6		4	0	6	2
A7		0	0	0	2	B7		0	7	0	0	C7		0	5	E	4	D7		4	6	6	8
A8		0	0	0	A	B8		2	7	E	4	C8		2	6	6	4	D8		5	0	0	A
A9		5	0	0	0	B9		2	7	A	4	C9		8	1	8	1	D9		9	0	0	2
AA		F	0	0	F	BA			Invalid			CA		0	6	C	0	DA		4	1	8	2
AB		A	0	0	5	BB			Invalid			CB		2	0	6	A	DB			Invalid		
AC			Invalid			BC		4	0	8	2	CC		0	0	E	0	DC		1	0	0	8
AD		2	0	0	4	BD		2	0	8	4	CD		1	6	6	2	DD				Invalid	
AE			Invalid			BE		1	0	8	8	CE		1	6	6	8	DE			Invalid		
AF		4	0	0	2	BF			Invalid			CF		0	7	E	0	DF			Invalid		

μPD7227
CMOS, INTELLIGENT, DOT-MATRIX LCD CONTROLLER/DRIVER

Description

The μPD7227 intelligent dot-matrix LCD controller/driver is a peripheral device designed to interface most microprocessors with a wide variety of dot matrix LCDs. It can directly drive any multiplexed LCD organized as 8 rows by 40 columns, and is easily cascaded up to 16 rows and 280 columns. The μPD7227 is equipped with several hardware logic blocks, such as an 8-bit serial interface, ASCII character generator, 40 x 16 static RAM with full read/write capability, and an LCD timing controller; all of which reduce microprocessor system software requirements. The μPD7227 is manufactured with a single 5 V CMOS process, and is available in a space-saving 64-pin plastic flat package.

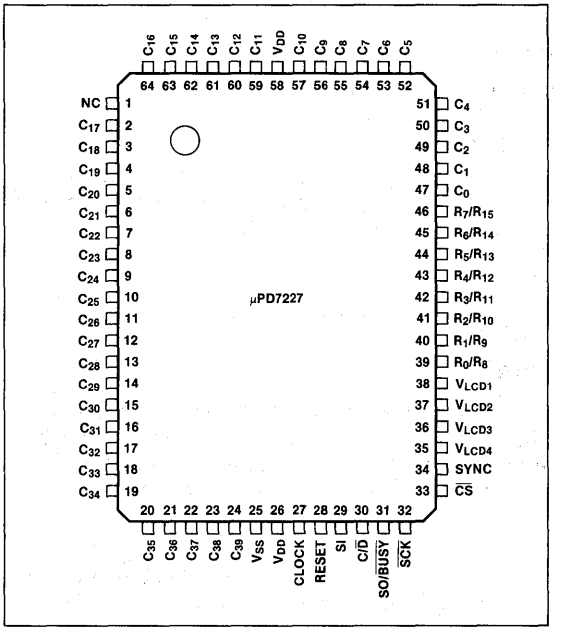
Features

- ☐ Single-chip LCD controller with direct LCD drive
- ☐ Compatible with most microprocessors
- ☐ Eight row drives
  - — Designed for dot-matrix LCD configurations up to 280 dots
  - — Designed for 5 x 7 dot-matrix character LCD configuration up to 8 characters
  - — Cascadable to 16 row drives
- ☐ 40 column drives
  - — Cascadable to 280 column drives
- ☐ Hardware logic blocks reduce system software requirements
  - — 8-bit serial interface for communication
  - — ASCII 5 x 7 dot-matrix character generator with 64-character vocabulary
  - — 40 x 16-bit static RAM for data storage, retrieval, and complete back-up memory capability.
  - — Voltage controller generates LCD bias voltages
  - — Timing controller synchronizes column drives with sequentially-multiplexed row drives
- ☐ Single +5 V power supply
- ☐ CMOS technology

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD7227G-12	64-pin plastic miniflat	1000 kHz

Pin Configuration



Pin Identification

No.	Symbol	Function
1	NC	No connection
2-24, 47-57, 59-64	C_0-C_{39}	LCD column driver outputs
25	V_{SS}	Ground
26, 58	V_{DD}	Power
27	CLOCK	System clock input
28	RESET	Reset input
29	SI	Serial input
30	C/$\overline{D}$	Command or data select input
31	SO/$\overline{BUSY}$	Serial output or busy output
32	$\overline{SCK}$	Serial clock input
33	$\overline{CS}$	Chip select input
34	SYNC	Synchronization port
35-38	V_{LCD1}-V_{LCD4}	LCD bias voltage supply inputs
39-46	R_0/R_8-R_7/R_{15}	LCD row driver outputs

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Pin Functions

C_0-C_{39}

LCD column driver outputs.

R0/8-R7/15

LCD row driver outputs.

V_{LCD1}-V_{LCD4}

LCD bias voltage supply inputs to the LCD voltage controller. Apply appropriate voltages from a voltage ladder connected across VDD.

SI

Serial input from the microprocessor.

SO/$\overline{BUSY}$

Serial output from the μPD7227 to the microprocessor when in read mode and C/$\overline{D}$ is low. When $\overline{BUSY}$ (active low), handshake output indicates the μPD7227 is ready to receive/send the next data byte.

$\overline{SCK}$

Serial clock input. Synchronizes 8-bit serial data transfer between the microprocessor and μPD7227.

C/$\overline{D}$

Command/data select input. Distinguishes serially input data byte as a command or as display data.

$\overline{CS}$

Chip select input. Enables the μPD7227 for communication with the microprocessor.

SYNC

Synchronization port. For multichip operation, tie all SYNC lines together and configure with the MODE SET command.

CLOCK

System clock input. Connect to external clock source.

RESET

Reset input. RC circuit or pulse initializes the μPD7227 after power-up.

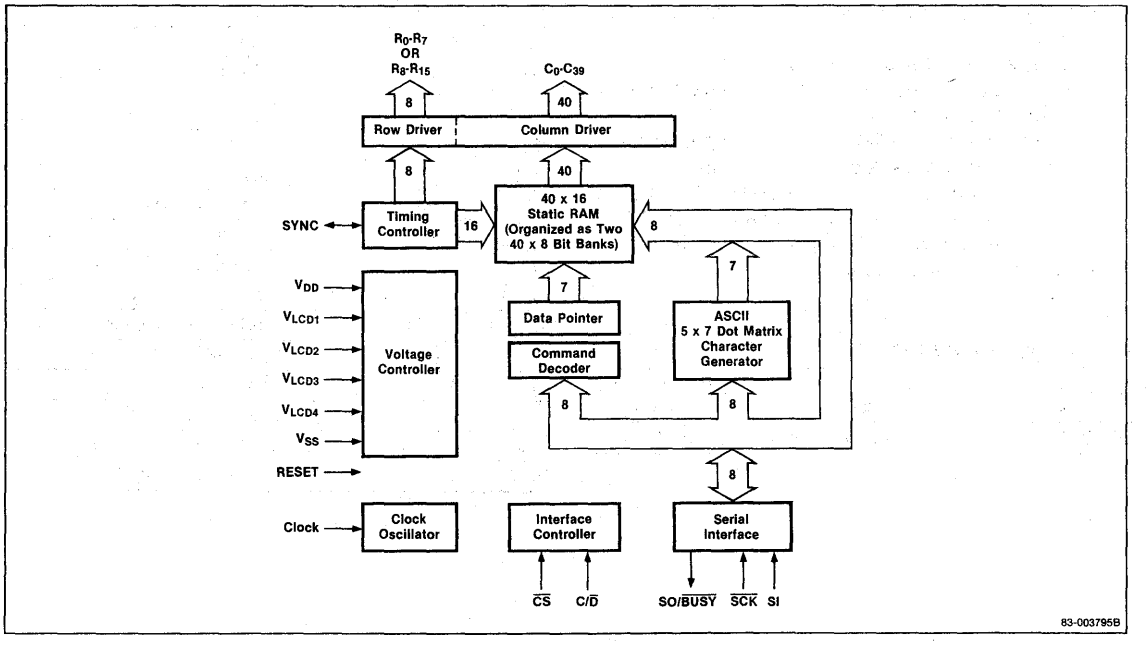
V_{DD}

Power supply positive. Apply single voltage 5 V ± 10% for proper operation.

V_{SS}

Ground.

Block Diagram



Absolute Maximum Ratings

T_A = 25°C

Power supply, V_{DD}	−0.3 V to +7.0 V
All inputs and outputs with respect to V_{CC}	−0.3 V to V_{DD} +0.3 V
Storage temperature, T_{STG}	−65°C to +150°C
Operating temperature, T_{OPT}	−10°C to +70°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, V_{DD} = 0V

Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Input capacitance	C_I		10	pF	fϕ = 1 MHz
Output capacitance	C_O		25	pF	Unmeasured pins returned to ground.
Input/output capacitance	C_{IO}		15	pF SYNC	

DC Characteristics

T_A = −10°C to +70°C, V_{DD} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
Input voltage, high	V_{IH}	0.7 V_{DD}		V_{DD}	V	
Input voltage, low	V_{IL}	0		0.3 V_{DD}	V	
Input leakage current, high	I_{LIH}			+10	μA	V_{IH} = V_{DD}
Input leakage current, low	I_{LIL}			−10	μA	V_{IH} = 0V
Output voltage, high	V_{OH1}	V_{DD}-0.5			V	SO/BUSY, I_{OH} = −400 μA
	V_{OH2}	V_{DD}-0.5			V	SYNC, I_{OH} = −100 μA
Output voltage, low	V_{OL1}			0.45	V	SO/BUSY, I_{OL} = +1.7 mA
				0.45	V	SYNC, I_{OL} = +100 μA
Output leakage current, high	I_{LOH}			+10	μA	V_{OH} = V_{DD}
Output leakage current, low	I_{LOL}			−10	μA	V_{OL} = 0V
LCD operating voltage	V_{LCD}	3.0		V_{DD}	V	8-row multiplexed LCD drive configuration
			V_{DD}		V	16-row multiplexed LCD drive configuration
Row drive output impedance	R_{ROW}		4	8	kΩ	
Column drive output impedance	R_{COLUMN}		10	15	kΩ	
Supply current	I_{DD}		200	400	μA	f0 = 400 KHz

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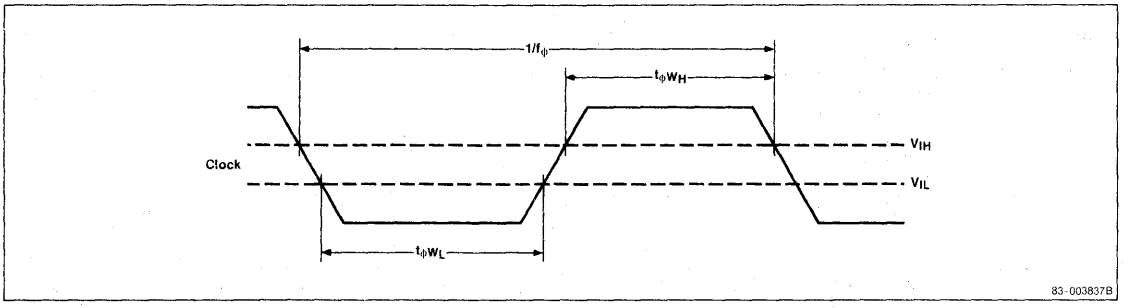
AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5.0V \pm 10\%$

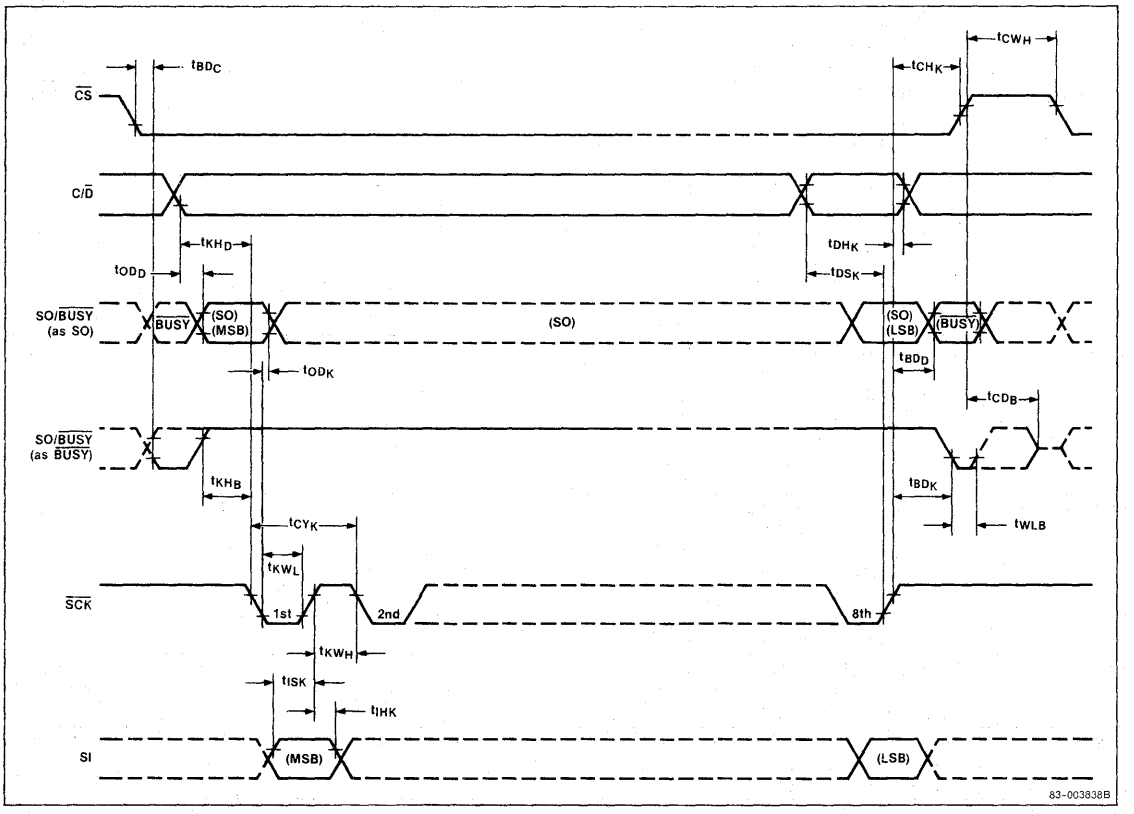
Parameter	Symbol	Limits Min	Limits Max	Unit	Test Conditions
Clock frequency	f_ϕ	100	1000	KHz	
Clock pulse width high	$t_{\phi WH}$	400		ns	
Clock pulse width low	$t_{\phi WL}$	400		ns	
$\overline{SCK}$ cycle	t_{CYK}	0.9		μs	
$\overline{SCK}$ pulse width high	t_{KWH}	400		ns	
$\overline{SCK}$ pulse width low	t_{KWL}	400		ns	
$\overline{SCK}$ hold time after $\overline{BUSY}$↑	t_{KHB}	0		ns	
SI setup time to $\overline{SCK}$↑	t_{ISK}	100		ns	
SI hold time after $\overline{SCK}$↑	t_{IHK}	250		ns	
SO delay time after $\overline{SCK}$↓	t_{ODK}		320	ns	C_{LOAD} = 50 pF
SO delay time after C/$\overline{D}$↓	t_{ODD}		2	μs	
$\overline{SCK}$ hold time after C/$\overline{D}$↓	t_{KHD}	2		μs	
$\overline{BUSY}$ delay time after 8th $\overline{SCK}$↑	t_{BDK}		3	μs	C_{LOAD} = 50 pF
$\overline{BUSY}$ delay time after C/$\overline{D}$↑	t_{BDD}		2	μs	
$\overline{BUSY}$ delay time after $\overline{CS}$↓	t_{BDC}		2	μs	
C/$\overline{D}$ setup time to 8th $\overline{SCK}$↑	t_{DSK}	2		μs	
C/$\overline{D}$ hold time after 8th $\overline{SCK}$↑	t_{DHK}	2		μs	
$\overline{CS}$ hold time after 8th $\overline{SCK}$↑	t_{CHK}	2		μs	
$\overline{CS}$ pulse width high	t_{CWH}	$2/f_\phi$		μs	
$\overline{CS}$↑ delay time to $\overline{BUSY}$ floating	t_{CDB}	2		μs	C_{LOAD} = 50 pF
SYNC load capacitance	C_{LOADS}		100	pF	
$\overline{BUSY}$ low level width	t_{WLB}	18	64	$1/f_\phi$	C_{LOAD} = 50 pF

Timing Waveforms

Clock Waveform



Serial Interface



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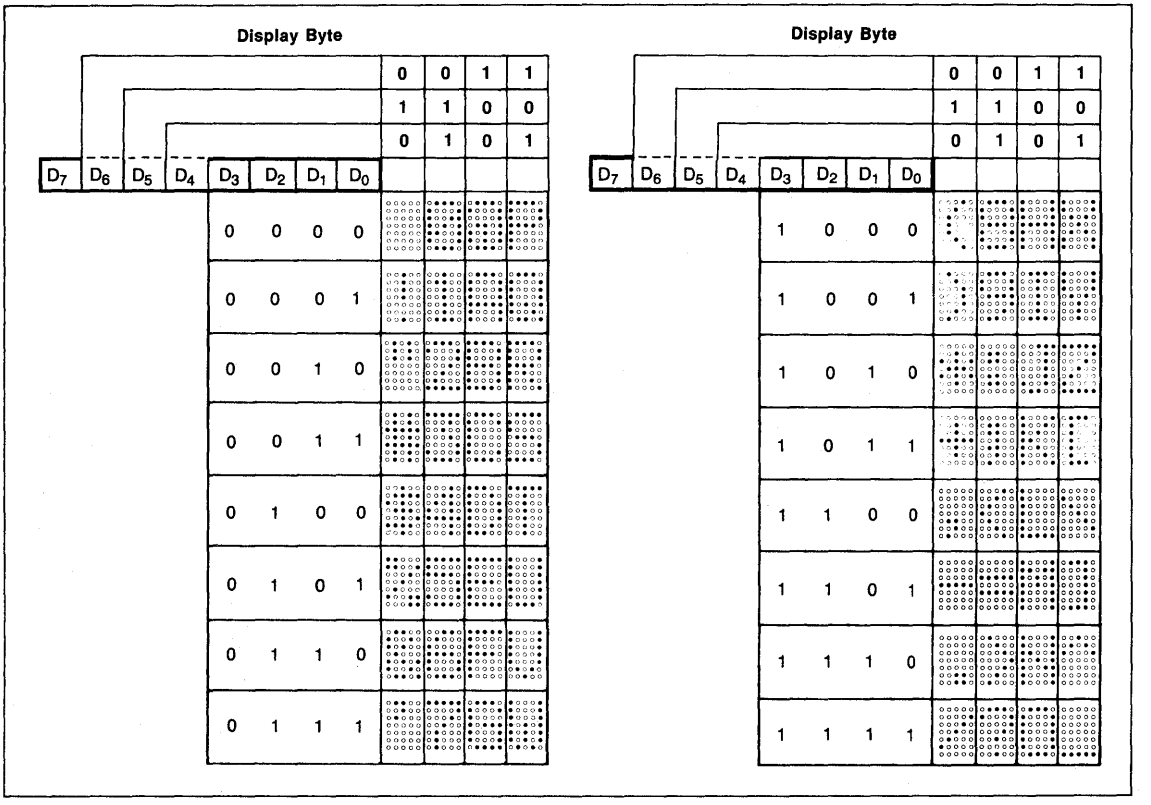
Command Summary

Command	Description	Instruction Code Binary D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HEX
Mode Set	Initialize the μPD7227, including selection of 1. LCD drive configuration 2. Row driver port function 3. RAM bank 4. SYNC port function	0	0	0	1	1	D_2	D_1	D_0	18-1F
Frame Frequency Set	Set LCD frame frequency	0	0	0	1	0	D_2	D_1	D_0	10-14
Load Data Pointer	Load data pointer with 7 bits of immediate data	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0	80-E7
Write Mode	Write display byte in serial register to RAM location addressed by data pointer; modify data pointer	0	1	1	0	0	1	D_1	D_0	64-67
Read Mode	Load RAM contents addressed by data pointer into serial register for output; modify data pointer	0	1	1	0	0	0	D_1	D_0	60-63
AND Mode	Perform a logical AND between the display byte in the serial register and the RAM contents addressed by data pointer; write result to same RAM location; modify data pointer	0	1	1	0	1	1	D_1	D_0	6C-6F
OR Mode	Perform a logical OR between the display byte in the serial register and the RAM contents addressed by data pointer; write result to same RAM location; modify data pointer	0	1	1	0	1	0	D_1	D_0	68-6B
Character Mode	Decode display byte in serial register into 5 x 7 character with character generator; write character to RAM location addressed by data pointer; increment data pointer by 5	0	1	1	1	0	0	1	0	72
Set Bit	Set single bit of RAM location addressed by data pointer; modify data pointer	0	1	0	D_4	D_3	D_2	D_1	D_0	40-5F
Reset Bit	Reset single bit of RAM location addressed by data pointer; modify data pointer	0	0	1	D_4	D_3	D_2	D_1	D_0	20-3F
Enable Display	Turn on the LCD	0	0	0	0	1	0	0	1	09
Disable Display	Turn off the ICD	0	0	0	0	1	0	0	0	08

Further details of operation can be found in the μPD7227 intelligent dot-matrix LCD controller/driver technical manual.

5 × 7 Character Set as Generated in μPD7227



D7	D6	D5	D4	D3	D2	D1	D0	0	0	1	1
								1	1	0	0
								0	1	0	1
				0	0	0	0				
				0	0	0	1				
				0	0	1	0				
				0	0	1	1				
				0	1	0	0				
				0	1	0	1				
				0	1	1	0				
				0	1	1	1				

D7	D6	D5	D4	D3	D2	D1	D0	0	0	1	1
								1	1	0	0
								0	1	0	1
				1	0	0	0				
				1	0	0	1				
				1	0	1	0				
				1	0	1	1				
				1	1	0	0				
				1	1	0	1				
				1	1	1	0				
				1	1	1	1				

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μPD7228
CMOS, INTELLIGENT, DOT-MATRIX LCD CONTROLLER/DRIVER

Description

The μPD7228 intelligent dot-matrix LCD controller/driver is a peripheral device designed to interface most microprocessors with a wide variety of dot-matrix LCDs. It can directly drive any multiplexed LCD organized as 8 rows by 50 columns or 16 rows by 42 columns. The μPD7228 has a standby function to conserve power. It is equipped with several logic blocks, such as an 8-bit serial interface, a 4-bit parallel interface, an ASCII upper/lower case, a Kana character generator, a 50 × 16 static RAM with full read/write capability, and an LCD timing controller, all of which reduce microprocessor system software requirements.

The μPD7228 is manufactured with a single 5 V CMOS process, and is available in an 80-pin space saving miniflat plastic package.

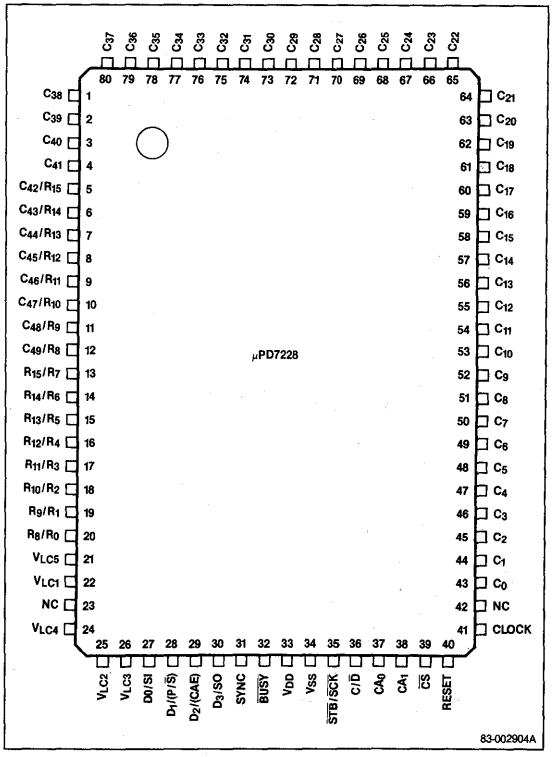
Features

- ☐ LCD direct drive
- ☐ 8- or 16-line multiplexing drive possible with single-chip
  - 8-line multiplexing: 400 (50 × 8) dots
  - 16-line multiplexing: 672 (42 × 16) dots
- ☐ 8-line or 16-line multiplexing drive with *n* chip configuration
  - 8-line multiplexing: *n* × 400 (*n* × 50 × 8) dots
  - 16-line multiplexing: *n* × 800 (*n* × 50 × 16) dots
- ☐ RAM: 2 × 50 × 8 bits for display data storage
- ☐ Programmer designated dot (graphics) display
- ☐ 5 × 7 dot-matrix display by on-chip character generator ASCII characters (alphanumerics, others): 64 characters; JIS characters (Kana and others): 96 characters
- ☐ Cursor operating command
- ☐ 8-bit serial interface compatible with μPD7500, μCOM-43N, μCOM-87/87LC
- ☐ 4-bit parallel interface compatible with μPD7500, μCOM-84/84C
- ☐ Standby function
- ☐ CMOS technology
- ☐ Single +5 V power supply
- ☐ Extended −40°C to +85°C temperature range available

Ordering Information

Part Number	Package Type
μPD7228G-12	80-pin plastic miniflat

Pin Configuration



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Pin Identification

No.	Symbol	Function
1–4, 43–80	C_0–C_{41}	LCD column drive outputs
5–12	C_{42} / R_{15}–C_{49} / R_8	LCD row / column drive outputs
13–20	R_0 / R_8–R_7 / R_{15}	LCD row drive outputs
21, 22, 24–26	V_{LC1}–V_{LC5}	LCD power supply
23, 42	NC	No connection
27	D_0 / SI	Data bus 0 / serial input
28	D_1(P/$\overline{S}$)	Data bus 1 (parallel / serial select)
29	D_2(CAE)	Data bus 2 (chip address enable)
30	D_3 / SO	Data bus 3 / serial output
31	SYNC	Synchronization signal input / output
32	$\overline{BUSY}$	Busy signal output
33	V_{DD}	Power supply
34	V_{SS}	Ground
35	$\overline{STB}$ / $\overline{SCK}$	Strobe / serial clock input
36	C / $\overline{D}$	Command / data select input
37, 38	CA_0, CA_1	Chip address select inputs
39	$\overline{CS}$	Chip select input
40	RESET	Reset signal input
41	CLOCK	System clock input

Pin Functions

D_0–D_3 (Data Bus)

In parallel interface mode, D_0–D_3 are input/output pins for 4-bit parallel data. Data on these lines is read at the rising edge of $\overline{STB}$. The four bits read on the first $\overline{STB}$ are loaded into the highest four bits of the serial/parallel register. The four bits read on the second $\overline{STB}$ are loaded into the lowest four bits of the register.

The contents of the serial/parallel register are output to these pins on the falling edge of $\overline{STB}$. As in the above case, the high-order four bits correspond to the first $\overline{STB}$, and the low-order four bits to the second $\overline{STB}$.

In serial interface mode, D_0 is a serial data input pin and D_3 is a serial data output pin. D_1 selects serial or parallel interface mode (P/$\overline{S}$), and D_2 is the chip address enable pin (CAE).

SI Serial Data-In (Input Common to D_0)

In serial interface mode, SI inputs serial data. Data on SI is loaded into the serial/parallel register at the rising edge of $\overline{SCK}$. The first data loaded is the most significant bit. To eliminate noise errors, SI uses the Schmitt-trigger input.

SO Serial Data-Out (Output Common to D_3)

In serial interface mode, SO is an output pin for serial data. The contents of the serial/parallel register are output to the SO pin, beginning with the most significant bit, on the falling edge of $\overline{SCK}$.

P/$\overline{S}$ Parallel/Serial Select (Input Common to D_1)

This pin sets parallel interface mode if it is high at the falling edge of RESET (at reset release). If it is low at the falling edge of RESET, it selects serial interface mode. The Schmitt-trigger prevents noise errors.

CAE Chip Address Enable (Input Common to D_2)

This pin is only used during serial interface mode, that is, when P/$\overline{S}$ is low at the falling edge of RESET. To enable chip addressing, the CAE line must be high at the falling edge of RESET. In parallel interface mode (when P/$\overline{S}$ is high at the falling edge of RESET), the chip addressing function is enabled regardless of the logic state of CAE at the falling edge of RESET. The Schmitt-trigger input prevents noise errors.

CA_0–CA_1 (Chip Address)

These input pins allow you to address the μPD7228 in a multi-chip configuration used for driving logic displays. During parallel interface mode, CA_0 and CA_1 are compared to chip address data sent from the CPU regardless of CAE status during a reset.

However, during serial interface mode, CA_0 and CA_1 are compared with chip address data from the CPU only when CAE enables chip addressing.

In multi-chip configurations, the device is selected if $\overline{CS} = 0$ and CA_0 and CA_1 match the chip address generated by the CPU. This address is the low two bits of the first 8-bit data input after $\overline{CS} = 0$.

In serial interface mode, if chip address selection is not used, connect CA_0 and CA_1 to ground.

$\overline{CS}$ (Chip Select)

$\overline{CS}$ is an active-low chip select input pin. When you are not using the chip address selection function, the $\overline{STB}$/$\overline{SCK}$ and C/$\overline{D}$ inputs are enabled if a low input is sent to $\overline{CS}$.

When you are using the chip address select function, if $\overline{CS}$ is brought low and the chip address data matches CA_0–CA_1, then $\overline{STB}$/$\overline{SCK}$ and C/$\overline{D}$ are enabled.

When $\overline{CS}$ is made high, D_3–D_0 and BUSY are placed in a high impedance state. The Schmitt-trigger input prevents noise errors.

STB/SCK (Strobe/Serial Clock)

In parallel interface mode, this is the strobe signal input pin ($\overline{STB}$) for 4-bit parallel input and output data. In serial interface mode, this is the serial clock input pin ($\overline{SCK}$) for serial input and output data.

C/$\overline{D}$ (Command/Data)

This pin specifies whether the parallel or serial input is a command or data. Bring C/$\overline{D}$ high to input a command, and low to input data.

In parallel interface mode, the contents of C/$\overline{D}$ are latched at the rising edge of the second $\overline{STB}$. Perform any changes to the C/$\overline{D}$ input before the falling edge of the first $\overline{STB}$. When outputting data, hold C/$\overline{D}$ low, whether serial or parallel.

In serial interface mode, the contents of C/$\overline{D}$ are latched at the rising edge of the eighth $\overline{SCK}$.

The Schmitt-trigger input prevents noise errors.

$\overline{BUSY}$ (Busy)

This pin outputs a busy signal to the CPU to warn that the μPD7228 is internally busy. When this signal is low, the CPU cannot read/write the μPD7228.

In the parallel interface mode, $\overline{BUSY}$ is forced low at the rising edge of the second $\overline{STB}$. In the serial interface mode, $\overline{BUSY}$ is forced low at the rising edge of the eighth $\overline{SCK}$.

If a chip is deselected ($\overline{CS}$ = high or chip address data does not match), the busy output is placed in the high impedance state.

SYNC (Synchronous)

In a multichip configuration, the SYNC signal synchronizes the phases of the LCD drive AC signals (row/column signals) among all the μPD7228's within the frame period. It uses the row drive signal as a common signal.

If one chip is designated master, its SYNC pin is in output mode and the remaining chips are made slaves. Their SYNC pins are put in input mode. The SMM command selects input or output mode. The master chip outputs a SYNC pulse in the last cycle of each frame. The slave chip reads the SYNC pulse from its own SYNC input for synchronization with the master chip.

In a single chip configuration, set the SYNC pin in the input or output mode. If you choose input mode, connect the SYNC pin to V_{SS}; conversely, if you choose output mode, the SYNC pin must be open.

Figures 1 and 2 show the output timing for the SYNC pulse in 8- and 16-line multiplexing.

Figure 1. SYNC Signal in 8-line Multiplexing

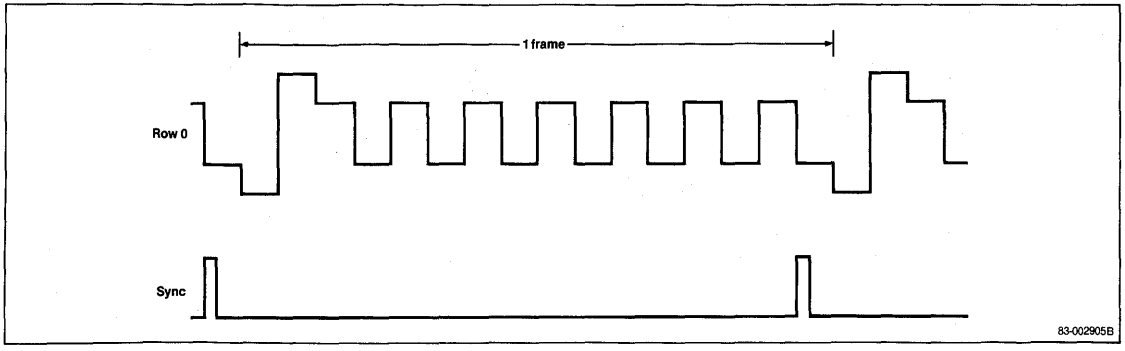
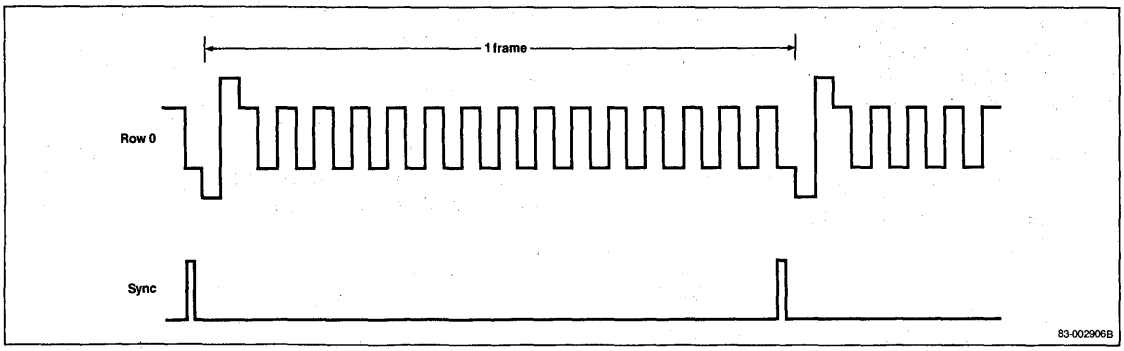


Figure 2. SYNC Signal in 16-line Multiplexing



C_0-C_{41} (Columns)

These pins output the column drive signal for the LCD.

R_8/C_{49}-R_{15}/C_{42} (Row/Column)

These pins are row drive outputs (R_8-R_{15}) or column drive outputs (C_{49}-C_{42}), depending on the SMM command.

R_0/R_8-R_7/R_{15} (Rows)

These pins are row drive outputs for rows R_0-R_7 or rows R_8-R_{15}, depending on the SMM command.

V_{LC1}-V_{LC5} (LCD Drive Voltage Supply)

These are reference voltage input pins for determining the voltage level of the LCD row/column drive signals.

CLOCK (Clock)

This is the external clock input pin.

RESET (Reset)

This is the active-high reset signal input pin. It has priority over all operations. You can also use it to release standby mode and begin low power data retention.

V_{DD} (Power Supply)

This is a positive power supply pin.

V_{SS} (Ground)

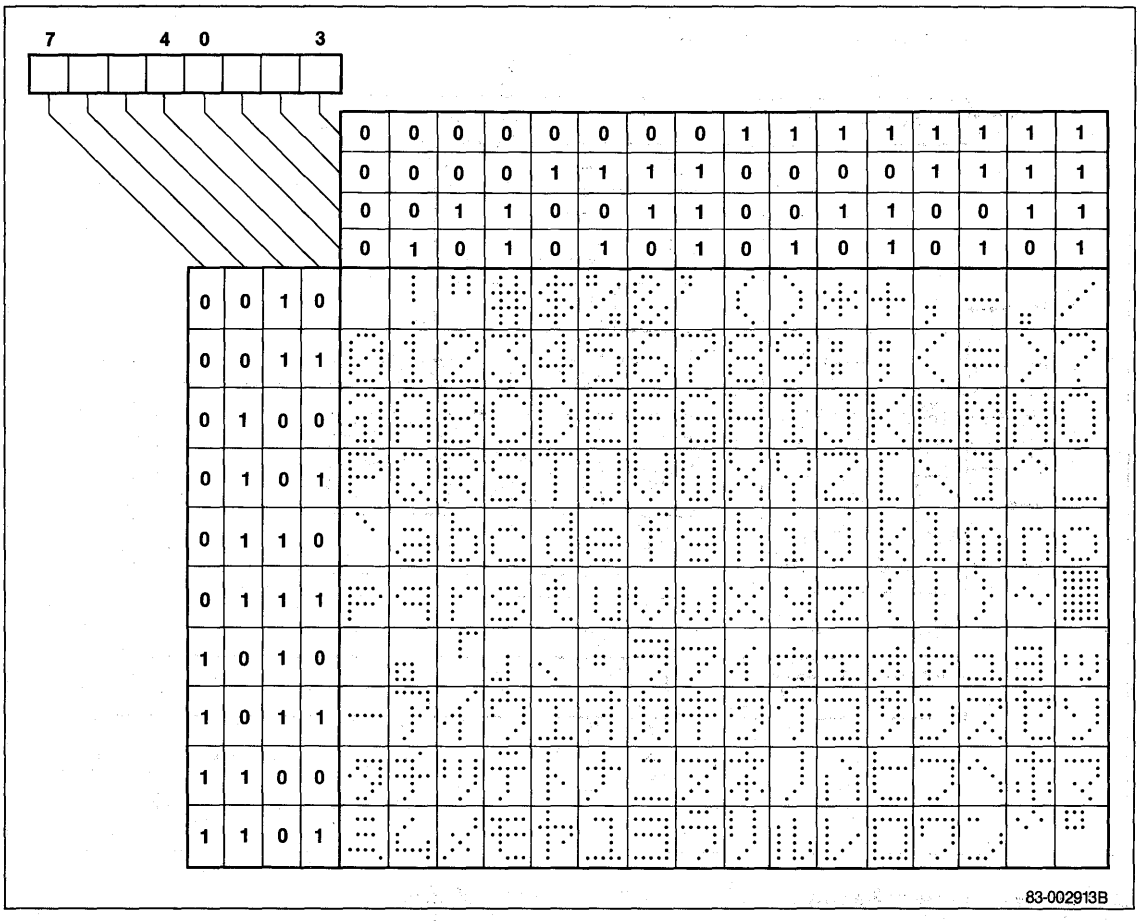
This is ground (GND).

Commands for μPD7228

The μPD7228 is provided with sixteen types of commands, each command consisting of one byte (8 bits).

Figure 3 shows the character codes and display patterns.

Figure 3. Character Codes and Display Patterns



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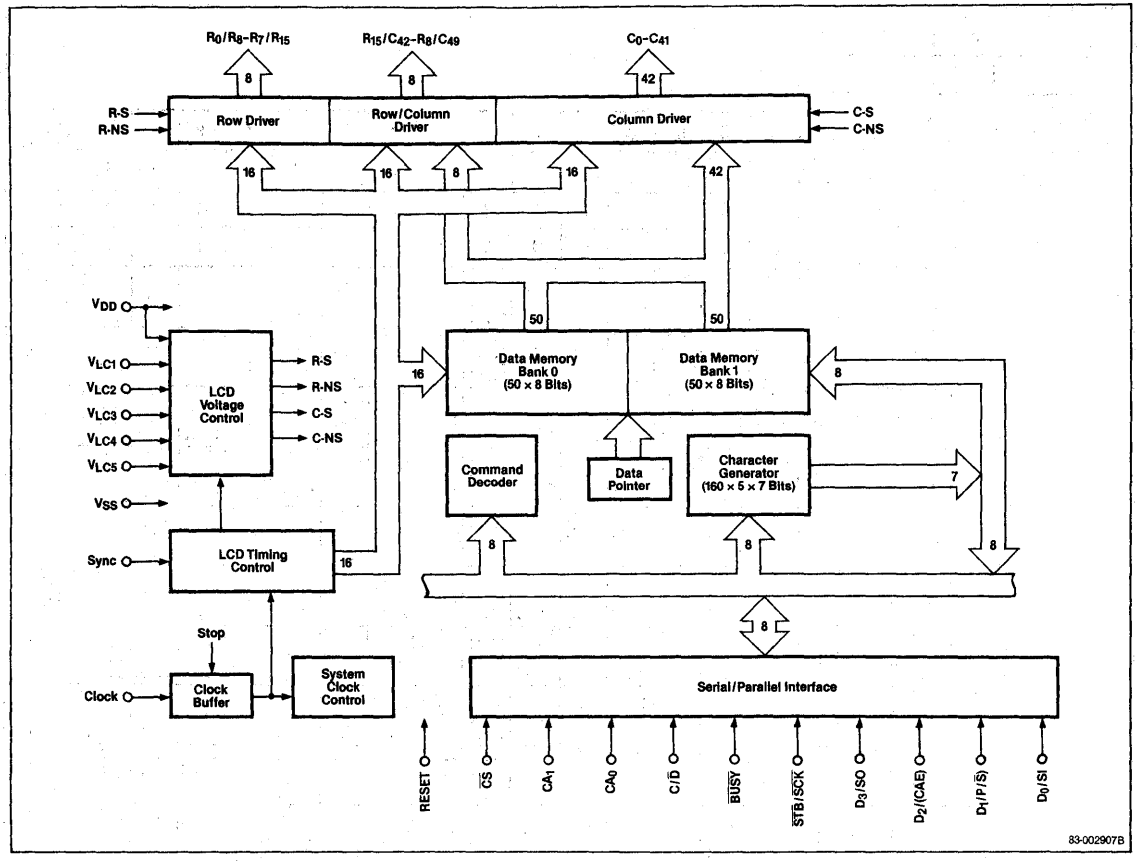
Block Diagram



Absolute Maximum Ratings

$T_A = 25°C$

Supply voltage, V_{DD}	−0.3 V to +7 V
Input voltage, V_I	−0.3 V to V_{DD} +0.3 V
Output voltage, V_O	−0.3 V to V_{DD} +0.3 V
Operating temperature, T_{OPT}	−10°C to +70°C
Storage temperature, T_{STG}	−65°C to +150°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

$T_A = 25°C$; $V_{DD} = 0$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I			10	pF	(Note 1)
Output capacitance	C_O			25	pF	(Note 1)
I/O capacitance	C_{IO}			15	pF	(Note 1)

Note:
(1) f = 1 MHz. Return unmeasured pins to 0 V.

DC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5\,V \pm 10\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage high	V_{IH1}	$0.7\,V_{DD}$		V_{DD}	V	Except $\overline{SCK}$
	V_{IH2}	$0.8\,V_{DD}$		V_{DD}	V	$\overline{SCK}$
Input voltage low	V_{IL}	0		$0.3\,V_{DD}$	V	
Output voltage high	V_{OH1}	$V_{DD}-0.5$			V	$\overline{BUSY}$, D_0–D_3, $I_{OH} = -400\,\mu A$
	V_{OH2}	$V_{DD}-0.5$			V	SYNC, $I_{OH} = -100\,\mu A$
Output voltage low	V_{OL1}			0.45	V	$\overline{BUSY}$, D_0–D_3, $I_{OL} = 1.7$ mA
	V_{OL2}			0.45	V	SYNC, $I_{OL} = 100\,\mu A$
Input leakage current high	I_{LIH}			10	μA	$V_I = V_{DD}$
Input leakage current low	I_{LIL}			−10	μA	$V_I = 0$ V
Output leakage current high	I_{LOH}			10	μA	$V_O = V_{DD}$
Output leakage current low	I_{LOL}			−10	μA	$V_I = 0$ V
LCD operating voltage	V_{LCD}	3.0		V_{DD}	V	
Row output impedance	R_{ROW}		4	8	kΩ	
Row / column output impedance	$R_{ROW/COL}$		5	10	kΩ	
Column output impedance	R_{COL}		10	15	kΩ	
Supply current	I_{DD1}		200	400	μA	Operating mode $f_C = 400$ kHz
	I_{DD2}			20	μA	Stop mode CLK = 0 V

AC Characteristics

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5\,V \pm 10\%$

Common Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Clock frequency	f_C	100		1100	kHz	
Clock pulse width high	t_{WHC}	350			ns	
Clock pulse width low	t_{WLC}	350			ns	
$\overline{RESET}$ pulse width high	t_{HRS}	4			μs	

Common Operation (cont)

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{BUSY}$ delay time from $\overline{CS}$ ↓	t_{DCSB}			2	μs	$C_L = 50$ pF
$\overline{CS}$ ↑ delay time to $\overline{BUSY}$ floating	t_{DCSBF}			4	μs	$C_L = 50$ pF
$\overline{CS}$ high level time	t_{WHCS}	4			μs	
SYNC load capacitance	C_{LSY}			100	pF	
Data set-up time to RESET ↓	t_{SDR}	0			μs	
Data hold time from RESET ↓	t_{HRD}	4			μs	

Serial Interface Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{SCK}$ cycle	t_{CYK}	0.9			μs	
$\overline{SCK}$ pulse width high	t_{WHK}	400			ns	
$\overline{SCK}$ pulse width low	t_{WLK}	400			ns	
$\overline{SCK}$ hold time from $\overline{BUSY}$ ↑	t_{HBK}	0			ns	
SI set-up time to $\overline{SCK}$ ↑	t_{SIK}	100			ns	
SI hold time from $\overline{SCK}$ ↑	t_{HKI}	250			ns	
SO delay time from $\overline{SCK}$ ↓	t_{DKO}			320	ns	$C_L = 50$ pF
$\overline{BUSY}$ delay time from eighth $\overline{SCK}$ ↑	t_{DKB}			3	μs	$C_L = 50$ pF
$\overline{BUSY}$ low-level time	t_{WLB}	18		64	$1/f_C$	$C_L = 50$ pF
C / $\overline{D}$ set-up time to first $\overline{SCK}$ ↓	t_{SDK}	0			μs	
C / $\overline{D}$ hold time from eighth $\overline{SCK}$ ↑	t_{HKD}	2			μs	
$\overline{CS}$ hold time from eighth $\overline{SCK}$ ↑	t_{HKCS}	2			μs	

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AC Characteristics (cont)

$T_A = -10°C$ to $+70°C$, $V_{DD} = +5\,V \pm 10\%$

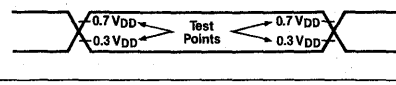
Parallel Interface Operation

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input command set-up time to $\overline{STB}$ ↓	t_A	100			ns	$C_L = 80\,pF$
Input command hold time from $\overline{STB}$ ↓	t_B	90			ns	$C_L = 20\,pF$
Input data set-up time to $\overline{STB}$ ↑	t_C	230			ns	$C_L = 80\,pF$
Input data hold time from $\overline{STB}$ ↑	t_D	50			ns	$C_L = 20\,pF$
Output data delay time	t_{ACC}	90		650	ns	$C_L = 80\,pF$
Output data hold time	t_H	0		150	ns	$C_L = 20\,pF$
$\overline{STB}$ pulse width low	t_{SL}	700			ns	
$\overline{STB}$ high level time	t_{SH}	1			μs	
$\overline{STB}$ hold time from $\overline{BUSY}$ ↑	t_{HBS}	0			μs	

Parallel Interface Operation (cont)

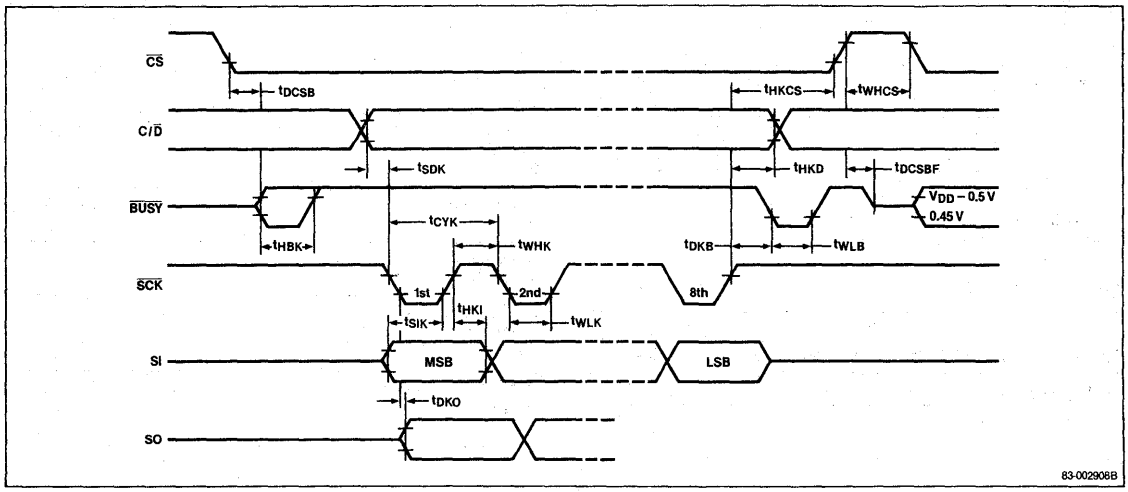
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{BUSY}$ delay time from second $\overline{STB}$ ↑	t_{DSB}			3	μs	
C/$\overline{D}$ set-up time to first $\overline{STB}$ ↓	t_{SDS}	0			μs	
C/$\overline{D}$ hold time froms econd $\overline{STB}$ ↑	t_{HSD}	2			μs	
$\overline{CS}$ hold time from second $\overline{STB}$ ↑	t_{HSCS}	2			μs	

AC Timing Test Points



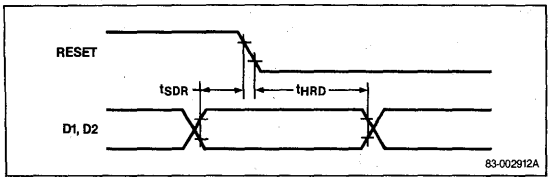
Timing Waveforms

Serial Interface

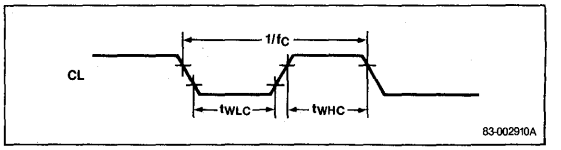


Timing Waveforms (cont)

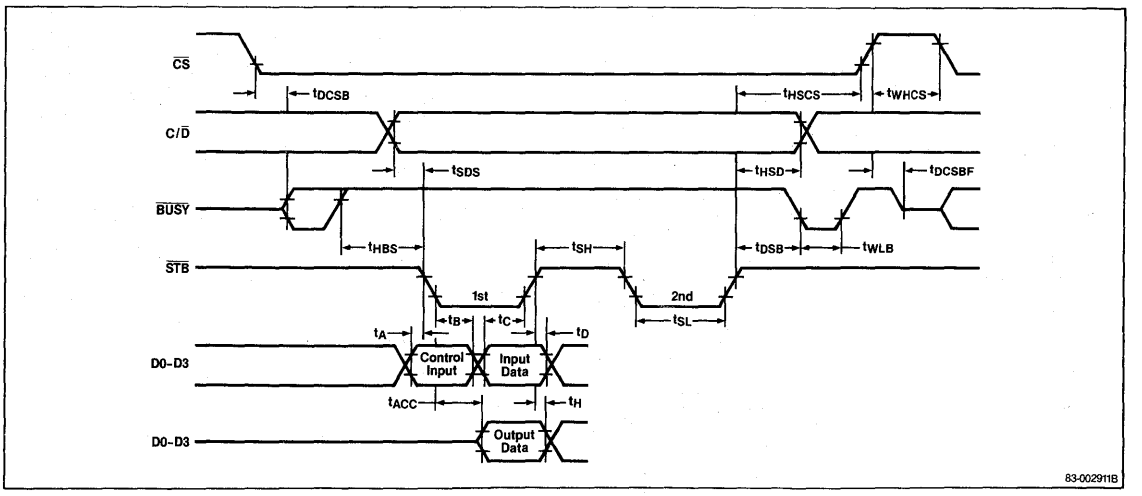
Interface



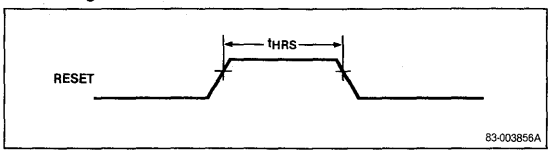
Clock Waveform



Parallel Interface



Reset Signal



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Command Summary

1. Set frame frequency	0	0	0	1	0	F2	F1	F0
2. Set multiplexing mode	0	0	0	1	1	M2	M1	M0
3. Display off	0	0	0	0	1	0	0	0
4. Display on	0	0	0	0	1	0	0	1
5. Set read mode	0	1	1	0	0	0	I1	I0
6. Set write mode	0	1	1	0	0	1	I1	I0
7. Set AND mode	0	1	1	0	1	1	I1	I0
8. Set OR mode	0	1	1	0	1	0	I1	I0
9. Set character mode with right entry	0	1	1	1	0	0	1	0
10. *Set character mode with left entry	0	1	1	1	0	0	0	1
11. Bit set	0	1	0	B2	B1	B0	J1	J0
12. Bit reset	0	0	1	B2	B1	B0	J1	J0
13. *Write cursor	0	1	1	1	1	1	0	1
14. *Clear cursor	0	1	1	1	1	1	0	0
15. Load immediate to data pointer	1	D6	D5	D4	D3	D2	D1	D0
16. *Set stop mode	0	0	0	0	0	0	0	1

Note:
* Newly added (compared to μPD7227).

Command Summary

		Instruction Code								
		Binary								
Mnemonic	**Operation**	**D_7**	**D_6**	**D_5**	**D_4**	**D_3**	**D_2**	**D_1**	**D_0**	**HEX**
SFF	Set frame frequency	0	0	0	1	0	D_2	D_1	D_0	10–14
SMM	Set multiplexing mode	0	0	0	1	1	D_2	D_1	D_0	18–1F
DISP OFF	Display off	0	0	0	0	0	0	0	0	08
DISP ON	Display on	0	0	0	0	1	0	0	1	09
LDPI	Load data pointer with immediate	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0	80–B1, C0–F1
SRM	Set read mode	0	1	1	0	0	0	D_1	D_0	60–63
SWM	Set write mode	0	1	1	0	0	1	D_1	D_0	64–67
SORM	Set OR mode	0	1	1	0	1	0	D_1	D_0	68–6B
SANDM	Set AND mode	0	1	1	0	1	1	D_1	D_0	6C–6F
SCML	Set character mode with left entry	0	1	1	1	0	0	0	1	71
SCMR	Set character mode with right entry	0	1	1	1	0	0	1	0	72
BSET	Bit set	0	1	0	D_4	D_3	D_2	D_1	D_0	40–5F
BRESET	Bit reset	0	0	1	D_4	D_3	D_2	D_1	D_0	20–3F
WRCURS	Write cursor	0	1	1	1	1	1	0	1	7D
CLCURS	Clear cursor	0	1	1	1	1	1	0	0	7C
STOP	Set stop mode	0	0	0	0	0	0	0	1	01

μPD72030
CMOS, INTELLIGENT LCD CONTROLLER

Description

The μPD72030 intelligent LCD controller manipulates dot-matrix characters and graphics by host CPU commands that are provided through an 8085-compatible bus interface. This frees the host to perform other tasks, and so increases overall system efficiency. The μPD72030 utilizes an 8-bit parallel bus that connects, without an additional interface, to such general-purpose microcomputers as the μPD8085AH or μPD8086. This bus permits high-speed data transfer to the LCD driver. A font character generator of up to 16 × 16 dots can be externally attached, permitting the generation of Kanji (Sino-Japanese) and other characters. A 5 × 7 dot character generator for alphanumeric characters and symbols totalling 64 characters is internally supported.

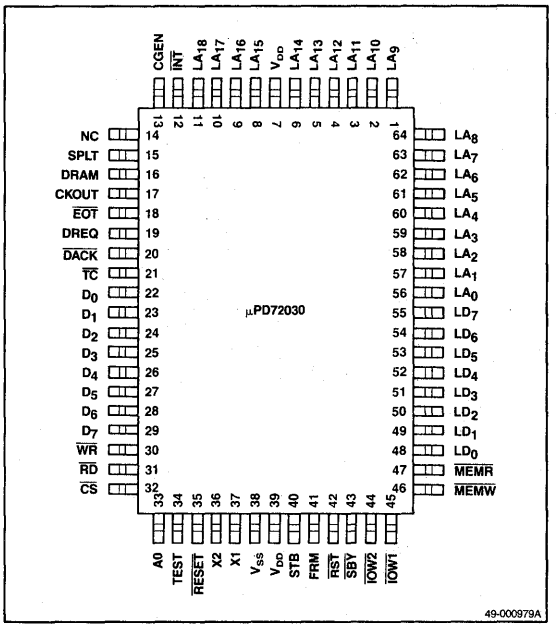
Features

- ☐ Display duty: 1/32 to 1/128
- ☐ Display control
  - — Cursor manipulation
    - — Vertical and horizontal movement
    - — Direct addressing
    - — Shift to home position
  - — Editing
  - — Scrolling
  - — Attribute functions
    - — Reverse display
    - — Underline
    - — Blinking display
- ☐ Directly connectable to LCD driver μPD6307/6308
- ☐ CMOS technology
- ☐ Single +5 V power supply

Ordering Information

Part Number	Package Type	Max Frequency of Operation
μPD72030G-12	64-pin plastic miniflat	6 MHz

Pin Configuration



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Pin Identification

No.	Symbol	Function
1-6,8-11, 56-64	LA_0-LA_{18}	Local address bus output
7,39	V_{DD}	Power supply input
12	$\overline{INT}$	Interrupt request output
13	CGEN	Character generator enable output
14	NC	No connection
15	SPLT	Split screen select output
16	DRAM	DRAM reset enable output
17	CKOUT	Clock output
18	$\overline{EOT}$	End of transfer output
19	DREQ	DMA request output
20	$\overline{DACK}$	DMA acknowledge input
21	$\overline{TC}$	Terminal count input
22-29	D_0-D_7	Data bus I/O
30	$\overline{WR}$	Write strobe input
31	$\overline{RD}$	Read strobe input
32	$\overline{CS}$	Chip select input
33	A0	Address 0; command and signal input for data bus function
34	TEST	Sets test mode input
35	$\overline{RESET}$	Reset input
36,37	X2,X1	Clock pins
38	V_{SS}	Ground
40	STB	Strobe output
41	FRM	Frame; AC converted signal output that drives the LCD
42	$\overline{RST}$	LCD driver reset output
43	$\overline{SBY}$	LCD standby mode output
44,45	$\overline{IOW2}$,$\overline{IOW1}$	LCD driver write strobe output
46	$\overline{MEMW}$	Local memory write output
47	$\overline{MEMR}$	Local memory read output
48-55	LD_0-LD_7	Data bus input to local memory

Pin Functions

Data Bus [D_0-D_7]

This I/O data bus interfaces with the host CPU. Writing of commands, parameters, and data, or reading of status and data are performed through this bus.

Address 0 [A0]

When input A0 is low, the data bus contains data or a parameter. When A0 is high, the data bus contains a command or status. A0 connects to the host CPU address bus.

Chip Select [$\overline{CS}$]

A low input to this pin enables the host CPU to read from or write to the data bus. $\overline{CS}$ connects to the host CPU address decode signal.

Read Strobe [$\overline{RD}$]

A low input to this pin while $\overline{CS}$ is active enables the μPD72030 to send status or data to the data bus. $\overline{RD}$ connects to the host CPU read strobe.

Write Strobe [$\overline{WR}$]

A low input to this pin while $\overline{CS}$ is active enables the μPD72030 to receive a command or parameter. $\overline{WR}$ connects to the host CPU write strobe.

DMA Request [DREQ]

This pin outputs a DMA service request for data block transfer. When a data block transfer is required between host CPU memory and μPD72030 local memory, if the transfer is possible, DREQ will be set high to request DMA service. DREQ connects to the service request input of the DMA controller. If the block transfer function is not used, this pin should be left open.

DMA Acknowledge [$\overline{DACK}$]

A low input to this pin acknowledges a DMA service request and internally sets $\overline{CS}$ and A0 low. $\overline{DACK}$ connects to the service acknowledge output of the DMA controller. If the block transfer function is not used, this pin should be pulled high.

Terminal Count [$\overline{TC}$]

A low input to this pin indicates data block transfer has terminated. $\overline{TC}$ connects to the DMA transfer termination output of the DMA controller. If the block transfer function is not used, $\overline{TC}$ should be pulled high.

Local Data Bus [LD_0-LD_7]

This data bus input provides communication between the μPD72030 and local memory, which consists of display memory and the character generator.

Local Address Bus [LA_0-LA_{18}]

This address bus output accesses local memory. LA_0-LA_{15} address display memory. LA_{16}-LA_{18} address the external character generator.

Character Generator Enable [CGEN]

This output enables the external character generator. When CGEN is high, the character address and scan address are output on LA_0-LA_{18}. When CGEN = 0, the address to display memory is output on LA_0-LA_{15}; LA_{16}-LA_{18} become don't care. When the external generator is not used, CGEN should be left open.

Split Screen Select [SPLT]

When the partitioned matrix display is used, this output pin selects which of two refresh memories will be available for access. When SPLT is low, refresh memory for the upper portion of the screen is accessed. When SPLT is high, refresh memory for the low portion of the screen is accessed.

DRAM Reset Enable [DRAM]

When dynamic RAM (DRAM) is connected to local memory, the logical AND of this output signal and the μPD72030 $\overline{RST}$ signal is input to the $\overline{RST}$ pin of the column driver. This prevents a loss of display memory contents while the display is off, without refreshing DRAM.

Local Memory Read [$\overline{MEMR}$]

This is the read strobe output to local memory. When $\overline{MEMR}$ goes low, the μPD72030 reads the contents of local memory. If $\overline{IOW1}$ and $\overline{IOW2}$ are also low level, the contents of display memory are directly written to the LCD driver.

Local Memory Write [$\overline{MEMW}$]

This is the write strobe output to local memory. When $\overline{MEMW}$ goes low, data is written to local memory.

LCD Driver Write Strobe [$\overline{IOW1}$, $\overline{IOW2}$]

These are the data write strobe outputs to the column driver. For each $\overline{MEMR}$ pulse, $\overline{IOW1}$ generates one pulse and $\overline{IOW2}$ generates two pulses. $\overline{IOW1}$ and $\overline{IOW2}$ are selected according to how the column driver is used.

Strobe [STB]

This is the row driver strobe. One STB pulse output at the timing interval causes the display of one row. The number of STB outputs during each frame interval determines the display duty.

Frame [FRM]

This output is an AC-converted signal that drives the LCD. A high-level output displays a positive frame (one screenful) and a low-level output displays a negative frame.

End of Transfer [$\overline{EOT}$]

When low, this output indicates one row of display data has transferred. $\overline{EOT}$ is a clear signal for the $\overline{CS}$ signal generator counter of the row driver.

LCD Driver Reset [$\overline{RST}$]

This output goes low when the LCD driver is being reset. For normal display, $\overline{RST}$ is high level.

LCD Standby [$\overline{SBY}$]

This output goes low when the LCD display stops and the LCD driver enters standby mode. For normal display, set $\overline{SBY}$ high level.

Clock Out [CKOUT]

This pin outputs a clock whose frequency is 1/15 that of the original oscillator.

XTAL1, XTAL2 [X1, X2]

These pins are used to connect an external crystal. Because the μPD72030 has a built-in high-gain amplifier, a functional clock can be generated by connecting a crystal or ceramic resonator and two capacitors to X1 and X2.

When an external clock is used, X1 inputs the clock and X2 is left open.

Reset [$\overline{RESET}$]

A low-level input to this pin initializes the μPD72030.

Interrupt Request [$\overline{INT}$]

This pin outputs an interrupt service request to the host CPU. If $\overline{INT}$ = 1, a command is being processed. If $\overline{INT}$ = 0, a command process is complete and the μPD72030 is ready to request a new command from the host CPU.

Test [TEST]

A high-level input to this pin sets the μPD72030 to test mode. For normal use, the input to the TEST pin should be fixed low by connecting TEST directly to V_{SS}.

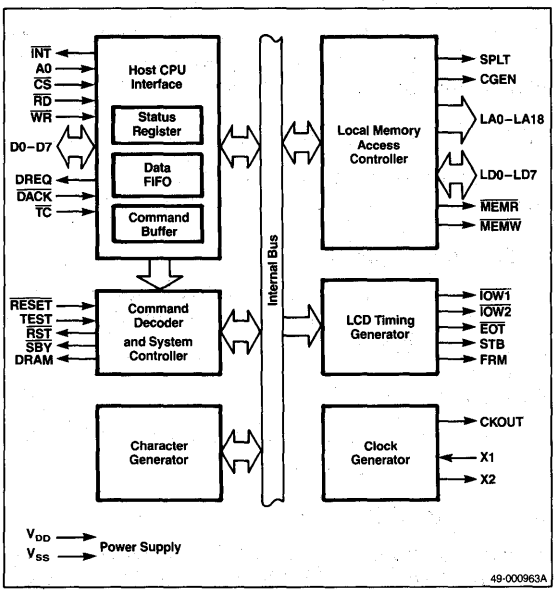
V_{SS}

Ground.

V_{DD}

Positive power supply.

Block Diagram



Functional Description

An LCD display system can be configured by connecting a row and column driver (a μPD6307 and μPD6308) and a general-purpose RAM as display memory to the μPD72030. An external character generator may be connected.

The μPD72030 performs both the display and command process. In the display process, the μPD72030 drives an LCD panel by sending display memory data to the column driver, and timing signals to the row and column drivers. At fixed intervals generated by the μPD72030, the display memory contents are transferred directly to the column driver via the local bus. When two or more column drivers are connected to the system, the row driver $\overline{CS}$ signal determines the column driver to which the data is to be written. After display data is stored in each column driver, the STB signal is output. One line of display data is then output to the LCD panel. The row signals are scanned, and the above sequence is repeated to drive the LCD panel using this time-division method.

In the command process, the μPD72030 manipulates the contents of display memory with host CPU commands. In order for the μPD72030 to process a command, the host CPU must read and check the status of the μPD72030. If the μPD72030 is processing a command, the host continues to read and check status until the μPD72030 is in the command wait state (no command is executing). When the μPD72030 is in the command wait state, the host sends a command to the μPD72030. (An interrupt may also be used.) The μPD72030 interprets the given command and executes it.

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	V_{SS} − 0.3 to +7 V
Input voltage, V_I	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Output voltage, V_O	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Operating temperature, T_{OPT}	−10 to +70°C
Storage temperature, T_{STG}	−65 to +125°C

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{DD1}	4.75	5.0	5.25	V	
Operating frequency	f_{OPT1}			6	MHz	T_A = −10 to +70°C
Supply voltage	V_{DD2}	4.5	5.0	5.5	V	
Operating frequency	f_{OPT2}			6	MHz	T_A = −10 to +50°C

DC Characteristics

T_A = −10 to +70°C, V_{DD} = 5 V ±5%
T_A = −10 to +50°C, V_{DD} = 5 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input voltage low	V_{IL}	−0.3		0.7	V	
Input voltage high	V_{IH1}	2.2		V_{DD} + 0.3	V	Other than $\overline{RESET}$, X1
	V_{IH2}	V_{DD} − 1		V_{DD} + 0.3	V	$\overline{RESET}$, X1
Output voltage low	V_{OL}	0		0.45	V	(1)
Output voltage high	V_{OH}	4.0			V	(2)
Input current	I_{I1}	−25		−3	μA	$\overline{RESET}$ $V_I \leq V_{IL}$
	I_{I2}			7.5	μA	X1: $V_I > V_{IH}$
		−7.5			μA	X1: $V_I < V_{IL}$
Input leakage current	I_{IL1}	−3		3	μA	TC, $\overline{DACK}$, $\overline{CS}$, A0, $\overline{RD}$, $\overline{WR}$ V_I = 0 V to V_{DD}
Output leakage current	I_{LO}	−3		3	μA	D_0-D_7, LD_0-LD_7 when high impedance
STOP current	I_{STP1}		1	12.0	μA	Xtal osc; No load
	I_{STP2}		3	10	mA	f_{OSC} = 6 MHz No load
Operating current	I_{SS}		5	14	mA	f_{OSC} = 6 MHz No load

Note:

(1) $\overline{IOW1}$, $\overline{IOW2}$, LD_0-LD_7, CKOUT, $\overline{MEMR}$, $\overline{MEMW}$, LA_0-LA_{18}, D_0-D_7, INT, CGEN, SPLT, DRAM, DREQ, FRM, STB, $\overline{RST}$, $\overline{EOT}$, $\overline{SBY}$. I_{OL} = 1.8 mA

(2) Same list as Note 1. I_{OH} = −0.4 mA

Capacitance

T_A = 25°C

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_I		7	12	pF	f_{OSC} = 1 MHz V_{OSC} = 0.1 V
Output capacitance	C_O		7	12	pF	

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AC Characteristics

T_A = −10 to +70°C, V_{DD} = 5 V ±5%
T_A = −10 to +50°C, V_{DD} = 5 V ±10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
$\overline{DACK}$, $\overline{CS}$, A0 setup to $\overline{RD}$↓	t_{AR}	0			ns	
$\overline{DACK}$, CS, A0 hold from $\overline{RD}$↑	t_{RA}	0			ns	
$\overline{RD}$ pulse width	t_{RR}	250			ns	
Data delay from $\overline{DACK}$, $\overline{CS}$, A0	t_{AD}			300	ns	C_L = 150 pF
Data delay from $\overline{RD}$↓	t_{RD}			250	ns	C_L = 150 pF
Data float from $\overline{RD}$↑	t_{DF}	10		120	ns	(1)
$\overline{DACK}$, $\overline{CS}$, A0 set-up to $\overline{WR}$↓	t_{AW}	0			ns	
$\overline{DACK}$, $\overline{CS}$, A0 hold from $\overline{WR}$↑	t_{WA}	0			ns	
$\overline{WR}$ pulse width	t_{WW}	160		15/ f_{OSC}	ns	
Data setup to $\overline{WR}$↑	t_{DW}	100			ns	
Data hold from $\overline{WR}$↑	t_{WD}	70			ns	
$\overline{TC}$ pulse width	t_{TC}	100			ns	
DREQ clear delay from $\overline{TC}$↓	t_{CDQ}			200	ns	C_L = 80 pF
$\overline{RD}$, $\overline{WR}$↓ to $\overline{TC}$↑	t_{RT}	100			ns	
$\overline{TC}$↓ to $\overline{RD}$, $\overline{WR}$↑	t_{TR}	100			ns	
DREQ↑ to $\overline{DACK}$↓	t_{DD}	0			ns	C_L = 80 pF
$\overline{DACK}$ pulse width	t_{DACK}	300			ns	
X1 cycle time	t_{CY}	166			ns	
X1 pulse width high	t_{CH}	50			ns	
X1 pulse width low	t_{CL}	80			ns	
X1 rise time	t_{CR}			20	ns	
X1 fall time	t_{CF}			20	ns	

Note:
(1) $V_{OH} = V_{DD} - 0.5$ V
$V_{OL} = 0.5$ V

Parameter	Symbol	Limits Min	Typ	Max	Unit
LA setup to $\overline{MEMR}$↓ (1)	t_{LMR}	60			ns
LA hold from $\overline{MEMR}$↑ (1)	t_{MRL}	100			ns
$\overline{MEMR}$ pulse width	t_{MRR}	660			ns
$\overline{MEMR}$ cycle time	t_{CYM}		1250		ns
$\overline{MEMR}$ high-level width	$t_{MR(H)}$	250			ns
LA to $\overline{IOW1}$↑	$t_{AD(1)}$	610			ns
$\overline{MEMR}$↓ to $\overline{IOW1}$↑	$t_{MRD(1)}$	400			ns
$\overline{IOW1}$↓ delay from $\overline{MEMR}$↓	t_{MRI1}	50			ns
$\overline{MEMR}$ hold from $\overline{IOW1}$↑	t_{IMR1}	160			ns
$\overline{IOW1}$ pulse width	t_{II1}	240			ns
$\overline{IOW1}$ cycle time	t_{CY1}	1100	1250		ns
$\overline{MEMR}$↓ to CKOUT↓	t_{MRF}	450			ns
CKOUT pulse width	t_{FF}	130			ns
CKOUT↑ to $\overline{MEMR}$↓	t_{FMR}	200			ns
CKOUT cycle time	t_{CY3}		2500		ns
DATA delay from $\overline{MEMR}$↓ (3)	t_{MRD}			430	ns
DATA hold from $\overline{MEMR}$↑ (3)	t_{MH}	0			ns
DATA delay from LA (1) (3)	t_{AD1}			500	ns
LA setup to $\overline{MEMW}$↓ (1)	t_{LMW}	200			ns
LA hold from $\overline{MEMW}$↑ (1)	t_{MWL}	190			ns
$\overline{MEMW}$ pulse width	t_{MWW}	400			ns
LA setup to DATA (1) (3)	t_{AD2}			270	ns
DATA setup to $\overline{MEMW}$↓ (3)	t_{DMW1}	10			ns
DATA setup to $\overline{MEMW}$↑ (2)	t_{DMW2}	580			ns
DATA hold from $\overline{MEMW}$↑ (2)	t_{MWD}	85			ns
STB pulse width (2)	t_{STB}	360			ns
STB↑ to $\overline{IOW1}$↓ (2)	t_{SW1}	530			ns
$\overline{IOW1}$↑ to $\overline{EOT}$↑ (2)	t_{WIE}	0			ns
$\overline{EOT}$ pulse width (2)	t_{EOT}	360			ns
FRM, $\overline{SBY}$, $\overline{RST}$ to STB↓ (2)	t_{FS}	720			ns
LA to $\overline{IOW2}$↑ (2)	$t_{AD(2)}$	400			ns
$\overline{MEMR}$↓ to $\overline{IOW2}$↑ (2)	$t_{MRD(2)}$	220			ns
$\overline{MEMR}$↓ to $\overline{IOW2}$↓ (2)	t_{MRI2}	0			ns

Note:

(1) Including CGEN and SPLT.

(2) Measuring points:
$V_{OH} = V_{DD} - 0.5$ V
$V_{OL} = 0.5$ V

(3) CLBUS = 200 pF

AC Characteristics (cont)

T_A = −10 to +70°C, V_{DD} = 5 V ±5%
T_A = −10 to +50°C, V_{DD} = 5 V ±10%
CL = 100 pF

Parameter	Symbol	Limits Min	Typ	Max	Unit
$\overline{IOW2}$↑ to $\overline{MEMR}$↓ (2)	t_{IMR2}	140			ns
$\overline{IOW2}$ pulse width (2)	t_{II2}	150			ns
$\overline{IOW2}$ cycle time (2)	t_{CY2}	500			ns
$\overline{IOW1}$↑ to $\overline{IOW2}$↓ (2)	T_{I12}	50			ns
$\overline{IOW2}$↑ to $\overline{IOW1}$↑ (2)	T_{I21}	70			ns
STB↑ to $\overline{IOW2}$↓ (2)	t_{SW2}	450			ns
LA setup to $\overline{MEMR}$↓ (1)	t_{LMR}	$1/f_{OSC}$ − 106			ns
LA hold from $\overline{MEMR}$↑ (1)	t_{MRL}	$1.5/f_{OSC}$ − 150			ns
$\overline{MEMR}$ pulse width	t_{MRR}	$5/f_{OSC}$ − 170			ns
$\overline{MEMR}$ cycle time	t_{CYM}		$7.5/f_{OSC}$		ns
$\overline{MEMR}$ high-level width	$t_{MR(H)}$	$2.5/f_{OSC}$ − 166			ns
LA to $\overline{IOW1}$↑	$t_{AD(1)}$	$5/f_{OSC}$ − 233			ns
$\overline{MEMR}$↓ to $\overline{IOW1}$↑	$t_{MRD(1)}$	$4/f_{OSC}$ − 266			ns
$\overline{IOW1}$↓ delay from $\overline{MEMR}$↓	t_{MRI1}	$1.5/f_{OSC}$ − 200			ns
$\overline{MEMR}$ hold from $\overline{IOW1}$↑	tIMR1	$1/f_{OSC}$ − 13			ns
$\overline{IOW1}$ pulse width	t_{II1}	$2.5/f_{OSC}$ − 176			ns
$\overline{IOW1}$ cycle time	t_{CY1}	$7.5/f_{OSC}$ − 150	$7.5/f_{OSC}$		ns
$\overline{MEMR}$↓ to CKOUT↓	t_{MRF}	$4.5/f_{OSC}$ − 300			ns
CKOUT pulse width	t_{FF}	$1.5/f_{OSC}$ − 120			ns
CKOUT↑ to $\overline{MEMR}$↓	t_{FMR}	$1.5/f_{OSC}$ − 50			ns
CKOUT cycle time	t_{CY3}		$15/f_{OSC}$		ns
DATA delay from $\overline{MEMR}$↓ (3)	t_{MRD}			$5/f_{OSC}$ − 400	ns
DATA hold from $\overline{MEMR}$↑ (3)	t_{MH}	0			ns
DATA delay from LA (1) (3)	t_{AD1}			$7/f_{OSC}$ − 666	ns
LA setup to $\overline{MEMW}$↓ (1)	t_{LMW}	$2.5/f_{OSC}$ − 216			ns
LA hold from $\overline{MEMW}$↑ (1)	t_{MWL}	$1.5/f_{OSC}$ − 60			ns
$\overline{MEMW}$ pulse width	t_{MWW}	$3.5/f_{OSC}$ − 183			ns
LA setup to DATA (1) (3)	t_{AD2}			$1.5/f_{OSC}$ + 20	ns

Parameter	Symbol	Limits Min	Typ	Max	Unit
DATA setup to $\overline{MEMW}$↓ (3)	t_{DMW1}	$1/f_{OSC}$ − 156			ns
DATA setup to $\overline{MEMW}$↑ (3)	t_{DMW2}	$4.5/f_{OSC}$ − 170			ns
DATA hold from $\overline{MEMW}$↑ (2)	t_{MWD}	$1/f_{OSC}$ − 81			ns
STB pulse width	t_{STB}	$3/f_{OSC}$ − 140			ns
STB↑ to $\overline{IOW1}$↓	t_{SW1}	$4/f_{OSC}$ − 136			ns
$\overline{IOW1}$↑ to EOT↓	t_{WIE}	$1/f_{OSC}$ − 166			ns
EOT pulse width	t_{EOT}	$3/f_{OSC}$ − 140			ns
FRM, $\overline{SBY}$, $\overline{RST}$ to STB↓	t_{FS}	$6/f_{OSC}$ − 280			ns
LA to $\overline{IOW2}$↑	$t_{AD\ (2)}$	$4/f_{OSC}$ − 266			ns
$\overline{MEMR}$↓ to $\overline{IOW2}$↑	$t_{MRD\ (2)}$	$3/f_{OSC}$ − 280			ns
$\overline{MEMR}$↓ to $\overline{IOW2}$↓	t_{MRI2}	$1.5/f_{OSC}$ − 250			ns
$\overline{IOW2}$↑ to $\overline{MEMR}$↓	t_{IMR2}	$1/f_{OSC}$ − 26			ns
$\overline{IOW2}$ pulse width	t_{II2}	$1.5/f_{OSC}$ − 100			ns
$\overline{IOW2}$ cycle time	t_{CY2}	$3.5/f_{OSC}$ − 83			ns
$\overline{IOW1}$↑ to $\overline{IOW2}$↓	t_{I12}	$1/f_{OSC}$ − 116			ns
$\overline{IOW2}$↑ to $\overline{IOW1}$↑	t_{I21}	$1/f_{OSC}$ − 96			ns
STB↑ to $\overline{IOW2}$↓	t_{SW2}	$4/f_{OSC}$ − 216			ns

Note:

(1) Including CGEN and SPLT.

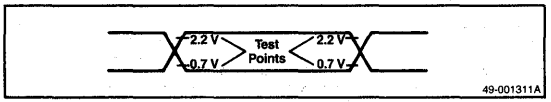
(2) Measuring points:
$V_{OH} = V_{DD} - 0.5$ V
$V_{OL} = 0.5$ V

(3) CLBUS = 200 pF
$f_{OSC} = f_{OPT1} = f_{OPT2}$

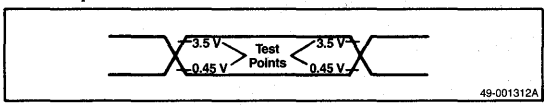
6

Timing Waveforms

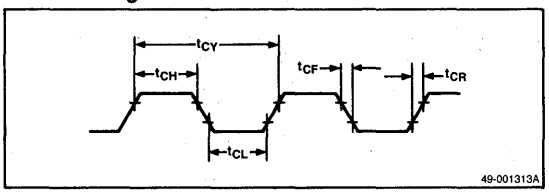
AC Input Test Points (except X1)



AC Output Test Points

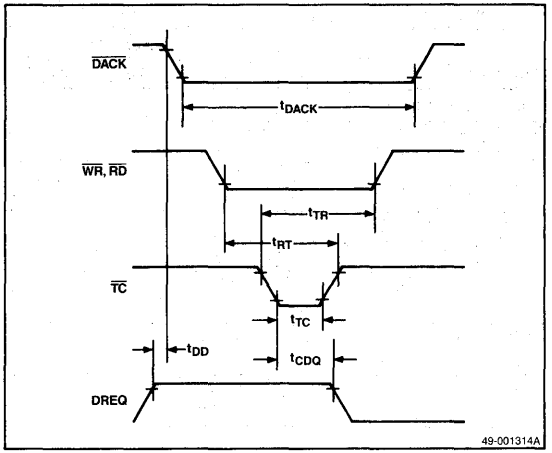


Clock Timing

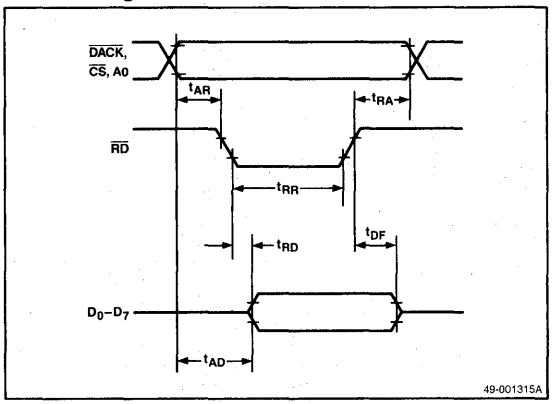


System Bus Timing

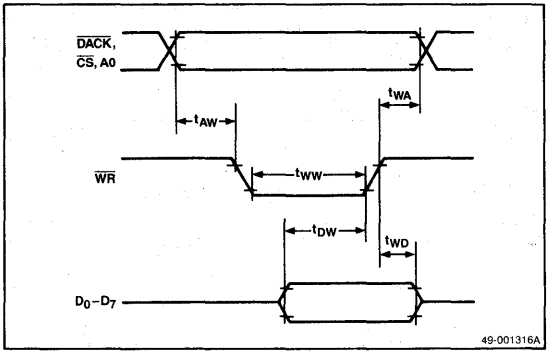
DMA Timing



Read Timing



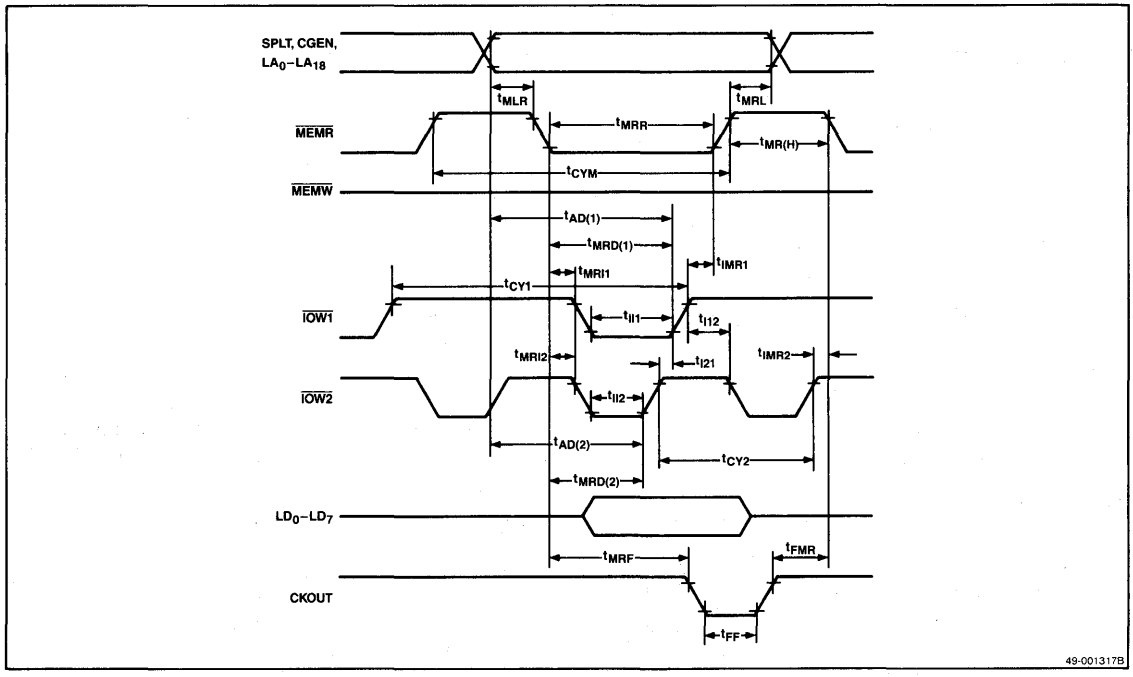
Write Timing



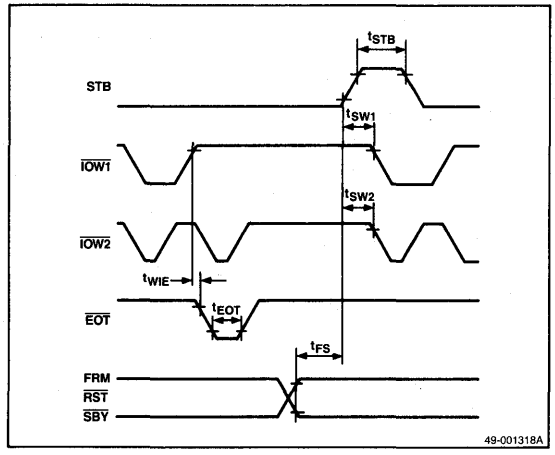
Timing Waveforms (cont)

Local Bus Timing

Display Timing



Display Timing



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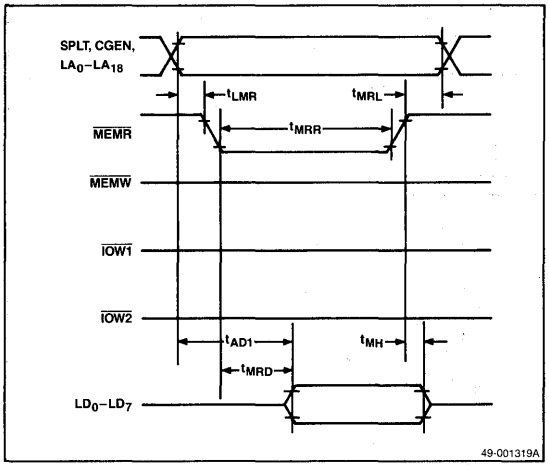
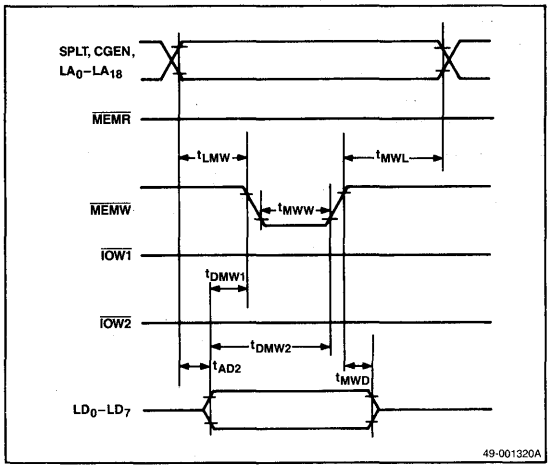
Timing Waveforms (cont)

Local Bus Timing (cont)

Read Timing



Write Timing



Commands

Paragraphs that follow explain the four initialization commands, nine function specifying commands, 21 display control commands, and 20 display data manipulation commands.

Initialization Commands

SYNC

1	0	0	1	0	1	1	0

Parameters

- Column direction (bytes)
  (L)
  (H)
- Time division
- 0 0 0 0 0 0 B1 B0
- STB cycle

Function. This command specifies the LCD panel size and the timing to generate control signals (FRM and STB) to the LCD driver. The total number of pixels in a row can be up to twice the number of time divisions.

B0 specifies whether the connection for expansion is used.

B0 = 0 Single matrix
= 1 Partitioned matrix
B1 = 0 DRAM not used
= 1 DRAM used

DSPDEF

1	0	0	1	0	1	1	1

Parameters

- Characters/line
- Character rows/screen
- Font size in column direction
- Font size in row direction
- Cell size in column direction
- Cell size in row direction
- 0 0 0 0 B3 B2 B1 B0

Function. Font and cell size are specified by a number of pixels. Cell size equals the character font size plus the size of the gap between each character, with the following limitations:

Cell column = 5 to 10, 12, or 16 pixels
Cell row = 7 to 17 pixels

B3 specifies the use of character code for the scan address. When B3 = 0, SA4 of the character code is used for the scan address. When B3 = 1, SA4 of the character code is used for the $\overline{CS}$ of the external character generator, in which case the following fonts are allowed:

Column Size	Row Size
1 to 8	1 to 16
9 to 16	1 to 8

B2 and B1 specify whether the external character generator is used. B0 specifies whether 2-byte codes are used.

B2	B1	Function
0	0	Internal character generator is used
0	1	External character generator is used
1	0	Internal and external character generators are used; if a code is given corresponding to characters in both, the internal character generator has priority.

B0 = 0 2-byte codes not used
= 1 2-byte codes used

MEMADR

1	1	1	1	0	0	0	1

Parameters

- Refresh memory starting address
  (L)
  (H)
- Character code memory starting address
  (L)
  (H)
- Character attribute memory starting address
  (L)
  (H)
- Graphics memory starting address
  (L)
  (H)

Function. This command specifies the start address of each display memory. If a memory is not required, set FFFFH.

MEMSIZ

1	1	1	1	0	0	1	0

Parameters

- Character code memory (lines)
- Character code memory (bytes)
  (L)
  (H)
- Character attribute memory (bytes)
  (L)
  (H)
- Graphics memory (bytes)
  (L)
  (H)

Function. This command specifies the size of each display memory. If a memory is not required, set 0.

To determine the required memory size for 1-byte codes, use the following formula:

MR = MB/R

where

MR is the number of character code memory rows

MB is the number of character code memory bytes

R is the number of characters per row.

For 2-byte codes, multiply the right side of the equation by 2.

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Function Specification Commands

START

1	0	0	0	0	0	0	0

This command releases the STOP mode when the display is OFF, interrupts command input, and clears the data bus.

STOP

1	0	0	0	0	0	0	1

This command turns the μPD72030 oscillator off. While the oscillator is off, data is retained with low power consumption. When a DRAM is used, STOP will destroy data in display memory.

The START command releases the STOP state. Once released, the oscillator requires an oscillation stabilizing time that has the same length as the blinking interval.

STOP2

1	0	0	0	1	0	0	1

This command functions like the STOP command except that the external clock is input.

DISPLY1

1	0	0	0	0	0	1	0

If the display is OFF, this command modifies refresh memory according to the contents of display memory and turns the display ON. If the display is ON, refresh memory is modified without turning the display off.

DISPLY2

1	0	0	0	0	1	0	0

Use this command after execution of BLANK, STOP, or STOP2 to return the display screen to the condition that existed before BLANK, STOP, or STOP2 was executed. DISPLY2 modifies refresh memory according to the contents of display memory and starts the display function.

DISPLY3

1	0	0	0	0	1	0	1

This command displays the contents of display memory unchanged.

DISPLY4

1	0	0	0	1	0	0	0

This command modifies the fixed row of refresh memory according to the contents of display memory. The fixed row is specified by the DIVIDU, DIVIDD, and DIVIDB commands. If DIVIDN is executed or the fixed row is modified to a different portion of display memory, DISPLY4 cannot be used. (Use DISPLY1.)

BLANK

1	0	0	0	0	0	1	1

This command stops display operation and turns the display off.

DISPL

1	1	1	1	0	1	0	0

This command updates the row where the cursor exists and moves the cursor to the leftmost position of the next row. If in graphics mode, the internal cursor position is moved.

Display Control Commands

MODEC, MODEG, MODEM

1	1	1	0	0	1	mode

These commands specify the display mode, as follows:

Command	Mode	Display Mode
MODEC	01	Character display mode (default)
MODEG	10	Graphics display mode
MODEM	11	Mixed (character/graphics) mode

If the display is ON, the display screen is changed to the specified mode. If MODEC is selected, refresh memory is cleared to 0 before refresh memory is updated. When the display mode is specified and display memory has not been specified, the contents of the addresses starting from FFFFH are displayed. (This proceeds from address FFFFH, to address 0, address 1, ...)

BLINK0-3

1	1	1	0	0	0	TS1	TS0

These commands specify four different blinking intervals, as follows:

Command	TS1	TS0	Interval Time
BLINK0	0	0	$2^{18} \times 15/f_{OSC}$ (default)
BLINK1	0	1	$2^{17} \times 15/f_{OSC}$
BLINK2	1	0	$2^{16} \times 15/f_{OSC}$
BLINK3	1	1	$2^{15} \times 15/f_{OSC}$

DSPPOS

1	1	1	1	0	0	0	0

Parameter

Display start position (row)

Function. This command specifies the row in character code memory where the display starts. The default is 0.

CURSOR

1	1	1	0	0	1	0	0

Parameter

0	0	0	0	0	0	P	B

Function. This command specifies the cursor type and whether blinking is to be used. These are specified as follows:

P = 0 Underline cursor
  = 1 Block cursor
B = 0 Blinking off
  = 1 Blinking on

The default is the underline cursor with blinking off. This cursor is one pixel thick, immediately below the character or space, its length that of the character plus the gap between the characters. The block cursor is the size of the character plus the gap. When the block cursor overlaps a character, the light and dark areas of the character are reversed.

CURON

1	0	0	1	0	0	0	0

This command sets the mode for cursor display on the screen. In display-ON character mode or display-ON mixed mode, CURON displays the cursor by writing to refresh memory. The default setting is for the cursor to be displayed.

CUROFF

1	0	0	1	0	0	0	1

This command sets the mode for no display of the cursor. In display-ON character mode or display-ON mixed mode, CUROFF turns the cursor off by modifying refresh memory.

CURUP, CURDN, CURRT, CURLT

1	0	0	0	1	1	B1	B0

This command shifts the cursor up, down, left, or right. The commands and their respective shift directions are as follows:

Command	B1	B0	Direction
CURUP	0	0	Up
CURDN	0	1	Down
CURRT	1	0	Right
CURLT	1	1	Left

When the cursor is displayed, these commands shift the cursor as specified. When the cursor is not displayed, it will be shifted and displayed in the next display mode. Table 1 describes what happens when the cursor is at the screen edge and one of these commands instructs the cursor to move outward.

CR

0	0	0	0	1	1	0	1

This command moves the cursor to leftmost edge.

LF

0	0	0	0	1	0	1	0

This command moves the cursor down one line.

BS

0	0	0	0	1	0	0	0

This command moves the cursor left one character.

Table 1. Cursor Movement at Screen Edge

Instruction	Function
CURUP at the highest row	Cursor does not move.
CURDN/LF at the lowest row	Screen scrolls and cursor moves down one row, remaining in the same column.
CURRT at rightmost edge in the highest row	Cursor moves to the leftmost edge in the next lower row.
CURRT at rightmost edge in the lowest line	Screen scrolls and cursor shifts to the leftmost edge of the next row.
CURLT/BS at the leftmost edge	Cursor moves to the rightmost edge in the preceding row.
CURLT/BS at leftmost edge in the highest row	Cursor does not move.

CURHM

1	0	0	0	1	0	1	1

When the cursor is displayed, this command moves the cursor to the home position (upper left corner of the screen). If the fixed row is set, the cursor will be at the upper left corner in the manipulating region, not on the fixed row. When the cursor is not displayed, it will be moved and displayed in the next display mode.

CURDR

1	0	0	1	0	1	0	0

Parameters

- Column position (X)
- Row position (Y)

Function. When the cursor is displayed, this command moves the cursor to a specified location (column X in row Y). When the cursor is not displayed, it will be moved and displayed in the next display mode.

When parameters exceeding the number of rows or columns are input, the address will be calculated assuming the specified location exists. The cursor will then be moved.

The default is home position (0, 0).

DIVIDU, DIVIDD

1	0	0	1	1	0	B1	B0

Parameters

- Character code memory fixed row
  (L)
  (H)
- Character attribute memory fixed row
  (L)
  (H)

Function. These commands specify the fixed row, which is a portion of refresh memory the user can allocate in order to modify parts of refresh memory without the whole display being updated. A fixed row corresponds to one line on the display screen.

B1 and B0 are specified as follows:

Command	B1	B0	Function
DIVIDU	0	1	Use upper fixed row (see DIVIDB)
DIVIDD	1	0	Use lower fixed row

If character attribute memory is not used, set FFFFH for the character attribute fixed row (L, H).

DIVIDB

1	0	0	1	1	0	1	1

Parameters

- Character code memory upper fixed row
  (L)
  (H)
- Character code memory lower fixed row
  (L)
  (H)
- Character attribute memory upper fixed row
  (L)
  (H)
- Character attribute memory lower fixed row
  (L)
  (H)

Function. This command is used when both upper and lower fixed rows are used, for the purpose of partitioning the screen. If character attribute memory is not used, set FFFFH for the character attribute memory upper and lower fixed rows (L, H).

The default is that upper and lower fixed rows are not set.

DIVIDN

1	0	0	1	1	0	0	0

This command invalidates the upper and lower fixed rows.

Display Data Manipulation Commands

CHRDSP

Parameter

- Character code
  (L)
- Character code (when in 2-byte code mode)
  (H)

Function. This command simultaneously displays a character (at the cursor location) and stores its display code in memory. The character code is input as a command, thus A0 = 1.

In 2-byte code mode, A0 must be 1 so that the lower byte of the character code will be sent to the command buffer and A0 = 0, when the higher byte of the character code is sent to the data buffer.

In display-ON graphics mode or display-OFF mode, only the code will be written to character code memory. When in display-ON character mode or mixed mode, the cursor will shift one character to the right when the display and writing are done. When the cursor is at the rightmost edge of a row, it will move to the leftmost edge of the next row. If the cursor is at the rightmost edge in the lowest row, the screen will scroll.

ESC

0	0	0	1	1	0	1	1

This command selects whether the input to the command buffer will be the command code or the external character generator code. The default is the command code, and the code selected toggles each time ESC is executed. Codes 1B, 08, 0A and 0D will not be accepted as character codes.

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ATTR

1	0	0	1	0	1	0	1

Parameter

0	S	C	0	0	U	R	B

S Space (when the character does not exist)
C Carriage return (logical row end)
U Underline
R Reverse
B Blink

Function. When a display character appears at the cursor location, ATTR specifies an attribute for the character and writes the attribute to attribute memory. Once specified, the attribute will apply to every subsequent character that is input, until another attribute is specified, or the ATTROF command is executed.

Any attribute can be specified by setting its bit to 1. Two or more attributes can be specified simultaneously.

The default is that all attributes are off.

ATTROF

1	0	0	0	1	0	1	0

This command releases any attributes specified for the character at the cursor location.

BLKTIN

1	0	0	1	1	1	1	0

Parameter

- Display memory address
  (L)
  (H)

Function. This command performs data block transfer from the data bus buffer to display memory. The address will increment each time a byte transfers. The DMA controller is used.

If the display is ON, executing BLKTIN to other than refresh memory causes no change in the display. To display the written contents of display memory, execute DISPLY1.

The μPD72030 does not enter the command wait state after the block transfer finishes.

BLKTOT

1	0	0	1	1	1	1	1

Parameters

- Display memory address
  (L)
  (H)

Function. This command performs data block transfer from display memory to the data bus buffer. The address will increment each time a byte transfers. The DMA controller is used.

The μPD72030 enters the command wait state after the block transfer finishes.

READ

1	1	1	0	1	0	0	0

Parameters

- Display memory address
  (L)
  (H)
- Number of transfer bytes

Function. This commands reads data from display memory and transfers the specified number of bytes via the data FIFO to the data bus buffer. The address increments each time a byte transfers.

If the host CPU does not accept all transfer data bytes, the μPD72030 cannot enter the command wait state.

WRITE

1	1	1	0	1	0	0	1

Parameters

- Display memory address
  (L)
  (H)
- Number of transfer bytes
- Write data
- Write data
  •
  •
  •
- Write data (max 256)

Function. This command writes data for the number of transfer bytes from the data bus buffer to display memory. The address increments each time a byte transfers. If 0 is input as the number of transfer bytes, 256 is assumed.

If the display is ON, executing WRITE to other than refresh memory causes no change in the display. Execute DISPLY1 to display the written contents.

If during WRITE execution the host CPU does not send the full number of transfer data bytes, the μPD72030 cannot enter the command wait state.

SELCT0, SELCT1

1	0	0	1	0	0	1	B0

When using a partitioned matrix, two refresh memories are required. When refresh memory is to be accessed, these commands specify refresh memory 0 or 1. The default is refresh memory 0. Once a refresh memory is specified, it remains valid until the next specification.

Command	B0	Selects
SELCT0	0	Refresh memory 0
SELCT1	1	Refresh memory 1

SELCTCG

1	1	1	1	0	0	1	1

Parameters

0	0	0	0	0	LA18	LA17	LA16

Function. This command will permit access to the external character generator memory. When a READ, WRITE, BLKTIN, or BLKTOT is executed, CGEN output goes high and the upper 3-bit address specified by the parameter is used.

CLRCHR

1	1	1	0	1	1	1	0

Parameters

- Data
- Data (for 2-byte code mode only)

Function. This command replaces character code memory with the specified data. If character attribute memory exists it is simultaneously cleared by 0.

In display-ON character mode or mixed mode, the display turns off, refresh memory is modified, and the display turns on again. The character display start position is initialized.

In display-ON graphics or display-OFF modes, only character code memory is altered. The boundaries of character code memory are initialized.

If character code memory is cleared by 20H or 2121H and attribute memory exists, attribute memory will be cleared by 40H (the space attribute is attached). The cursor will move to home position.

If character code memory is not specified, CLRCHR will not execute and the WARNING bit will be set.

CLRGRP

1	1	1	0	1	1	1	1

Parameter

- Data

Function. This command replaces graphics memory with the specified data.

In display-ON graphics mode or mixed mode, the display turns off, refresh memory is modified, and the display turns on. In character display-ON and -OFF modes, only graphics memory is modified.

If graphics memory is not specified, CLRGRP will not execute and the WARNING bit will be set.

TRANS

1	0	0	1	1	1	0	0

Parameters

Number of transfer characters

Function. This command sends the character code of each of the specified number of characters to the data bus buffer, beginning with the character at the cursor location. For each character, the character code and then the attribute code, if it exists, is sent. For 2-byte codes, the character code is sent from the lower to the higher bits. The number of characters to be transferred is specified as follows:

0 transfers up to the logical row end (up to the location where the CR attribute is set); 0 cannot be specified if attribute memory has not been specified

FFH transfers up to the physical row end (up to the right edge of the screen.)

1 to FEH transfers up to the specified number of characters.

In display-ON graphics or character display-OFF mode, the character code is transferred to the data bus buffer with an address that is calculated based on the cursor location and the character code start position stored in the controller.

If character code memory has not been specified, TRANS will not execute and the WARNING bit will be set.

CLRLN

1	0	0	0	0	1	1	0

This command clears character code memory from the cursor position to the right edge of the row. When character attribute memory exists, attribute memory will be cleared by 40H. The cursor does not move.

When 1-byte code is used, character code memory will be cleared by 20H. For 2-byte code, character code memory will be cleared by 2121H. Attribute memory should be set to the space attribute state (cleared by 40H).

In display-ON graphics and display-OFF mode, only character code memory is cleared depending on the cursor position and character code display start position stored in the controller.

When character code memory is omitted, the calculation of the character code memory address will be made assuming character code memory starts from address FFFFH.

CLRFRM

1	0	0	0	0	1	1	1

This command clears character code memory from the cursor location to the right edge of the last row. In display-ON mode, refresh memory is also cleared. If character attribute memory exists, it is cleared by 40H. The cursor does not move.

When 1-byte code is used, character code memory is cleared by 20H. For 2-byte code, character code memory is cleared by 2121H. Attribute memory should be set to the space attribute state, cleared by 40H.

In display-ON graphics and display-OFF mode, only character code memory is cleared, depending on the cursor position and character code display start position stored in the controller.

If character code memory has not been specified, character code memory will be cleared beginning from address FFFFH.

DRESET, DSET

1	1	1	0	1	0	1	B0

Parameter

- Pixel position in column direction
  (L)
  (H)
- Pixel position in row direction
  (L)
  (H)

Function. These commands reset or set a pixel at a specified coordinate on the screen. These commands manipulate only graphics memory.

Command	B0	Operation
DRESET	0	Reset
DSET	1	Set

The coordinate location is specified according to the number of pixels in the column and row positions. If the specified location is outside the screen, data in an unexpected location will be reset or set. DISPLY1 will display the updated contents of graphics memory.

If graphics memory has not been specified, DRESET or DSET will execute assuming graphics memory starts from address FFFFH.

GET

1	1	1	0	1	1	0	0

Parameters

- Pixel position in column direction
  (L)
  (H)
- Pixel position in row direction
  (L)
  (H)

Function. This command sends data that tells whether the pixel at the specified coordinate on the screen is set or reset in graphics memory. If the pixel is set, FFH is sent to the data bus buffer. If reset, 0 is sent to the data bus buffer.

If graphics memory has not been specified, GET will execute assuming graphics memory starts from address FFFFH.

COMP

1	1	1	0	1	1	0	1

Parameters

- Pixel position in column direction
  (L)
  (H)
- Pixel position in row direction
  (L)
  (H)

Function. This command reverses a pixel at a specified coordinate on the screen. COMP manipulates only graphics memory. If the specified location is outside the screen, data in an unexpected location will be reversed. DISPLY1 will display the updated contents of graphics memory.

If graphics memory has not been specified, COMP will execute assuming graphics memory starts from address FFFFH.

DEVELOPMENT TOOLS

7

Section 7 — Development Tools

Introduction

NEC has a comprehensive line of development hardware and software supporting our many families of single-chip microcomputers. NEC's software operates under CPM-86™ or MS-DOS™, and will run on a variety of hardware including IBM-PC™, NEC-APC, and the NEC MD-086 multiuser development system. Generally, an NEC cross-assembler will assemble all members of a series.

NEC hardware is divided into two types: Evakits and IE boards. Evakits are mother boards. They accept plug-in daughter boards that emulate specific microcomputers. IE boards are in-circuit emulators. They generally have more memory and more functionality than the specific device they emulate. Both types of hardware come with up/down load software that allows communication with the host computer over a serial line.

Following is an example of configuring a system for developing the μPD7533 single-chip microcomputer. The selection guide below shows that the μPD7533 requires a mother board, the EVAKIT-7500B, and a daughter board, the EV7533, which personalizes the mother board for the μPD7533.

For software development, you first select the host computer and operating system. Using the most popular module, the IBM-PC type running under MS-DOS, as an example, you would need ASM75-D52. This assembler works for all 7500 series members, and includes up/down loading software.

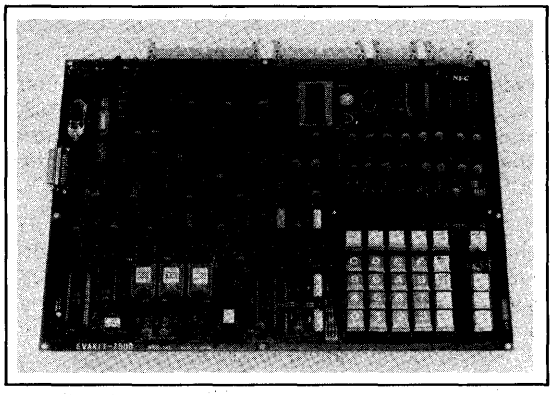
In addition to these development tools, you would need some μPD75CG33E piggyback prototyping chips. And voila, you have a low-cost development system that can be configured by adding daughter boards for other members of the family as new applications emerge.

μPD7500 Series Hardware Development Tool Selection Guide

Part Number	Emulator	Add-On Board (Required)	System Evaluation Board	EPROM Device
μPD7501	EVAKIT-7500B	EV7514	SE-7514A	—
μPD7502	EVAKIT-7500B	EV7514	SE-7514A	—
μPD7503	EVAKIT-7500B	EV7514	SE-7514A	—
μPD7506	EVAKIT-7500B	—	SE-7508	—
μPD7507	EVAKIT-7500B	—	—	μPD75CG08E
μPD7507H	EVAKIT-7500B	EV7508H	—	μPD75CG08HE
μPD7507S	EVAKIT-7500B	—	SE-7508	—
μPD7508	EVAKIT-7500B	—	—	μPD75CG08E
μPD7508A	EVAKIT-7500B	—	SE-7508	—
μPD7508H	EVAKIT-7500B	EV7508H	—	μPD75CG08HE
μPD7514	EVAKIT-7500B	EV7514	SE-7514A	—
μPD7516H	EVAKIT-7500B	EV7500FIP	—	μPD75CG16HE
μPD7519	EVAKIT-7500B	EV7500FIP	—	μPD75CG19E
μPD7519H	EVAKIT-7500B	EV7500FIP	—	μPD75CG19HE
μPD7527	EVAKIT-7500B	EV7528	—	μPD75CG28E
μPD7528	EVAKIT-7500B	EV7528	—	μPD75CG28E
μPD7533	EVAKIT-7500B	EV7533	—	μPD75CG33E
μPD7537	EVAKIT-7500B	EV7528	—	μPD75CG38E
μPD7538	EVAKIT-7500B	EV7528	—	μPD75CG38E
μPD7554	EVAKIT-7500B	EV7554A	SE-7554A	—
μPD7556	EVAKIT-7500B	EV7554A	SE-7554A	—
μPD7564	EVAKIT-7500B	EV7554A	SE-7554A	—
μPD7566	EVAKIT-7500B	EV7554A	SE-7554A	—

CP/M-86 is a trademark of Digital Research Corporation.
MS-DOS is a trademark of Microsoft Corporation.
IBM-PC is a trademark of International Business Machines Corporation.

EVAKIT-7500B



Description

The EVAKIT-7500B is a stand-alone Evakit for NEC's μPD7500 series of 4-bit, single-chip microcomputers. The EVAKIT-7500B provides complete hardware emulation and software debug capabilities for the μPD7506, μPD7507/7507S and the μPD7508/7508A microcomputers. With the addition of device specific add-on boards, the EVAKIT-7500B is easily tailored to support the remaining members of the family.

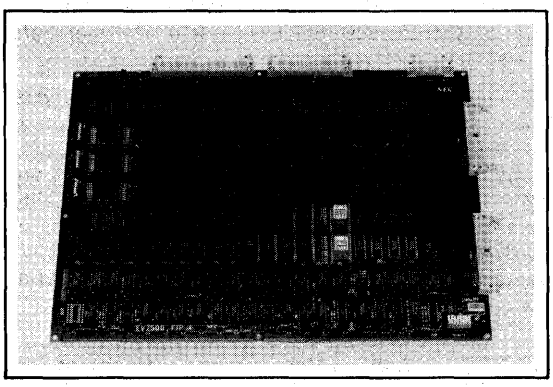
Real-time and single-step emulation capability, coupled with a powerful on-board system monitor and real-time trace capability create a powerful debug environment. The EVAKIT-7500B is controlled either from an on-board keypad or over a serial line from a terminal or host computer. User programs are downloaded through a serial line or read from a PROM. Existing programs may be modified or small programs may be created using the on-board hexadecimal keypad.

Features

- ☐ Real-time and single-step emulation capability
- ☐ 8K bytes of user program memory
- ☐ Powerful system monitor
  - — Display/modify/move program memory
  - — Display/modify data memory
  - — Load/verify/display PROM
  - — Examine/modify internal registers
  - — Full disassembler
- ☐ User-specified breakpoint conditions
  - — Program counter and number of passes
  - — Stack pointer
  - — Data address and value
- ☐ Real-time trace capability
  - — 2048 instruction cycle trace
  - — External trace probes
- ☐ Supports three operating modes
  - — On-board hexadecimal keypad controlled
  - — External terminal controlled
  - — Host computer system controlled
- ☐ Serial interface: RS-232C or TTL
- ☐ EPROM programming capability (2764 and 27128)

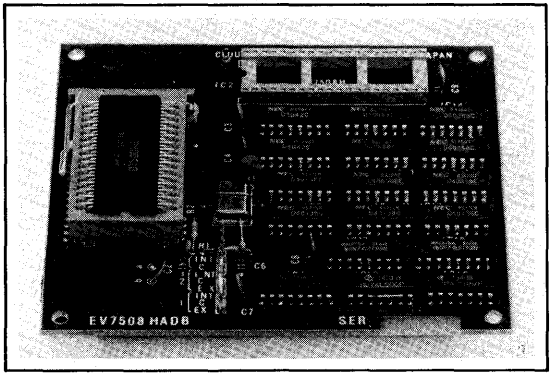
EV7500 Add-On Boards

EV7500FIP



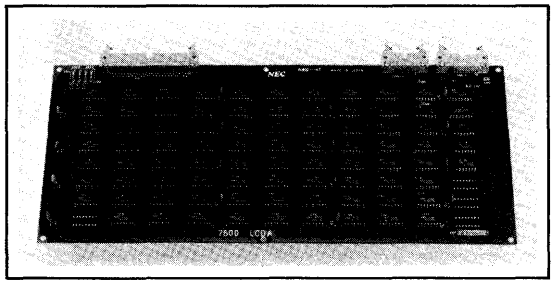
The EV7500FIP is an add-on board for the EVAKIT-7500B which is required for emulating the μPD7516H and the μPD7519/7519H microcomputers. This board is mounted under the EVAKIT-7500B, adding vacuum fluorescent display control and high voltage driver capability to the Evakit.

EV7508H



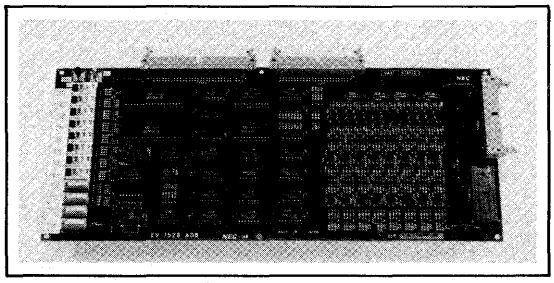
The EV7508H is an add-on board for the EVAKIT-7500B which is required for emulating the μPD7507H and the μPD7508H microcomputers. This board plugs directly into the μPD7500 socket on the EVAKIT-7500B, allowing the system to support these high speed versions of the μPD7500 series.

EV7514



The EV7514 is an add-on board for the EVAKIT-7500B which is required for emulating the μPD7501, μPD7502, μPD7503, and μPD7514 microcomputers. This board is mounted under the EVAKIT-7500B, adding LCD controller/driver capability to the Evakit.

EV7528



The EV7528 is an add-on board for the EVAKIT-7500B which is required for emulating the μPD7527, μPD7528, μPD7537, and μPD7538 microcomputers. This board is mounted under the EVAKIT-7500B, allowing the Evakit to support the additional features of these parts: I/O ports with high dielectric strength, optional pull-down resistors, and zero voltage detection circuits.

EV7533

The EV7533 is an add-on board for the EVAKIT-7500B which is required for emulating the μPD7533 microcomputer. This board plugs directly into the μPD7500 socket, allowing the Evakit to emulate the μPD7533's four analog inputs and its 8-bit A/D converter.

EV7554A

The EV7554A is an add-on board for the EVAKIT-7500B which is required for emulating the μPD7554, μPD7556, μPD7564, and μPD7566 microcomputers. This board mounts on top of EVAKIT-7500B, allowing the Evakit to emulate the additional features of these parts: optional pull-up/pull-down resistors for ports 0, 1, 10, and 11; comparator/CMOS inputs for port 1; high current/CMOS outputs for ports 8, 9, 10, and 11.

μPD7500 Series System Evaluation Boards

SE-7508

The SE-7508 is the system evaluation board for the μPD7506, μPD7507S, and μPD7508A microcomputers. The SE-7508 is functionally equivalent to the ROM-based microcomputers. With the user's program residing in either a μPD2716 or μPD2732 on board, the SE-7508 can be connected to the user's prototype allowing total system performance to be evaluated.

SE-7514A

The SE-7514A is the system evaluation board for the μPD7500 series microcomputers with LCD direct drive capabilities: μPD7501, μPD7502, μPD7503 and μPD7514. The SE-7514A is functionally equivalent to the ROM-based microcomputers. With the user's program residing in either an on-board μPD2764 or μPD27128, you can connect the SE-7514A to your prototype and evaluate total system performance.

SE-7554A

The SE-7554A is the system evaluation board for the μPD7500 series mini/microcomputers: μPD7554, μPD7556, μPD7564, and μPD7566. The SE-7554A is functionally equivalent to the ROM-based mini/microcomputer. With your program residing in the lower 4K bytes of an on-board μPD2764, you can connect the SE-7554A to your prototype and evaluate total system performance.

EVAKIT-75X

Description

The EVAKIT-75X is a stand-alone Evakit for NEC's μPD75000 series of 4-bit, single-chip microcomputers. With the addition of a device specific add-on board, the EVAKIT-75X is easily tailored to provide complete hardware emulation and software debug capabilities for the individual members of the family. Real-time and single step emulation capability, coupled with an on-board system monitor, create a powerful debug environment.

The EVAKIT-75X is controlled over a serial line from either a terminal or host computer. User programs can be downloaded through this serial line or read from PROM. The NEC PG1000 series PROM programmer with the PG1005 personality module can be connected for easy programming of the μPD75P105.

Features

- ☐ Real-time, real-time step, and single step emulation
- ☐ 16K bytes of program memory (72 hour backup)
- ☐ Powerful on-board system monitor
  - — Display/modify/move/exchange/search/verify program memory
  - — Display/modify/move/exchange/verify data memory
  - — Display/modify general and special registers
  - — Upload/download data
  - — Line-assembler and full disassembler
  - — Load/verify/display PROM
- ☐ User-specified breakpoints
  - — Logical OR of up to four break conditions
  - — Break loop counter
  - — Delayed break by machine cycle or instruction count
- ☐ Real-time trace capability
  - — 512 machine cycle or 2048 instruction cycle trace
  - — User-specified trace range
  - — Trace data search function
- ☐ Automatic command string execution
- ☐ Eight external sense probes
- ☐ Controlled from external terminal or host computer
- ☐ Two RS-232C serial ports
- ☐ On-board EPROM programmer (2764 and 27128)
- ☐ Upload/download program for PG1000/PG1005 PROM programmer

EVAKIT-75X Add-On Boards

EV75108

The EV75108 is an add-on board for the EVAKIT-75X required for emulating the μPD75104, μPD75106, and μPD75108 microcomputers. This board mounts on top of the EVAKIT-75X, allowing the Evakit to support the features specific to these parts. This includes switch selectable pull-up resistors on ports 12, 13, and 14.

EV75208

The EV75208 is an add-on board for the EVAKIT-75X which is required for emulating the μPD75204, μPD75206, and μPD75208 microcomputers. This board mounts on top of the EVAKIT-75X, allowing the Evakit to support the features specific to these parts including the FIP Controller/Driver.

PG1000 Personality Module

PG1005

The PG1005 is a plug-in personality module for the PG1000 PROM Programmer. This module is required to program the μPD75P108, the EPROM version for the μPD75104, μPD75106, and μPD75108 4-bit, single-chip microcomputers. Interchangeable socket adapters are provided with the PG1005 to allow programming both shrink dip and flat packages.

μPD7800 Series Hardware Development Tool Selection Guide

Part Number	Emulator	Real-time Trace Board	Add-on Board	System Evaluation Board	EPROM Device
μPD78C05A	EVAKIT-87LC [Note 1]	EV87LCRTT	EV78C06A	SE-78C06	—
μPD78C06A	EVAKIT-87LC	EV87LCRTT	EV78C06A	SE-78C06	—
μPD7807	IE-7809-M	—	—	—	μPD78P09R
μPD7808	IE-7809-M	—	—	—	μPD78P09R
μPD7809	IE-7809-M	—	—	—	μPD78P09R
μPD7810	EVAKIT-87AD [Note 1] IE-87AD-M	EV87ADRTT —	— —	— —	— —
μPD7810H	IE-7811H	—	—	—	—
μPD78C10	IE-78C11-M	—	—	—	—
μPD7811	EVAKIT-87AD [Note 1] IE-87AD-M	EV87ADRTT —	— —	— —	μPD78PG11E μPD78PG11E
μPD7811H	IE-7811H	—	—	—	μPD78PG11E [Note 2]
μPD78C11	IE-78C11-M	—	—	—	—
μPD78C14	IE-78C11-M	—	—	—	—

Notes:

(1) Addresses 0-0FFFH access memory on the Evakit only.

(2) Special selected parts.

EVAKIT-87AD

Description

The EVAKIT-87AD is one of the stand-alone Evakits for NEC's μPD7800 series of 8-bit, single-chip microcomputers. The EVAKIT-87AD provides complete hardware emulation and software debug capabilities for the μPD7811 microcomputer. Real-time and single-step emulation capability, coupled with an on-board system monitor, creates a powerful debug environment. An optional real-time trace board is also available to greatly increase your debugging capabilities.

An auxiliary hexadecimal keypad or a serial line from a terminal or host computer controls the EVAKIT-87AD. User programs are downloaded through a serial line or read from a PROM. Use the keyboard to modify existing programs or create small programs. An on-board programmer for 2716, 2732, 2732A, or 2764 EPROMs provides an easy means for submitting your final code for production.

Features

- ☐ Real-time and single-step emulation capability
- ☐ 8K bytes of on-board user program memory
  - — Expandable to 64K bytes using IEEE-796 bus
- ☐ Powerful system monitor
  - — Display/modify/move/search/verify/test Memory
  - — Display/modify internal registers
  - — Display input ports; write to output ports
  - — Load/verify/display PROM
  - — Full disassembler
- ☐ User-specified breakpoint
  - — One serial (logical AND of up to 4 conditions) or
  - — One parallel (logical OR of up to 15 conditions)
  - — Break delay and loop counter
  - — Break on: address and data values and CPU controls
- ☐ Supports three operating modes
  - — Auxiliary hexadecimal keypad controlled
  - — External terminal controlled
  - — Host computer system controlled
- ☐ Serial interface: RS-232C, TTL, or 20 mA current loop
- ☐ EPROM programming capability (2716, 2732, 2732A, 2764)

EVAKIT-87AD Add-On Board

EV87ADRTT

The EV87ADRTT is the real-time trace board for use with NEC's EVAKIT-87AD stand-alone Evakit. The EV87ADRTT communicates with the EVAKIT-87AD via the IEEE-796 bus, adding real-time trace and additional breakpoint capabilities to the Evakit. A 1K X 62-bit trace RAM is available for storing the status of the address bus, the data bus, the control signals, and the I/O ports as your program is executed in real-time. The trace data may be displayed in either the machine cycles or the instruction mode with the user controlling the content of the display. The addition of another address breakpoint, a timer breakpoint, and a trace step breakpoint greatly increase the power of the EVAKIT-87AD.

EVAKIT-87LC

Description

The EVAKIT-87LC is one of the stand-alone Evakits for NEC's μPD7800 series of 8-bit, single-chip microcomputers. The EVAKIT-87LC provides complete hardware emulation and software debug capabilities for the μPD78C06 microcomputer. With the addition of the EV78C06A add-on board, the EVAKIT-87LC supports the μPD78C06A. Real-time and single-step emulation capability, coupled with an on-board system monitor, create a powerful debug environment.

An auxiliary hexadecimal keypad or a serial line from a terminal or host computer controls the EVAKIT-87LC. User programs are downloaded through a serial line or read from a PROM. Existing programs may be modified or small programs may be created using the keypad. An on-board programmer for 2716 or 2732 EPROMs provides an easy means for submitting the user's final code for production. An optional real-time trace board is available to greatly increase your debugging capabilities.

Features

- ☐ Real-time and single-step emulation capability
- ☐ 4K bytes of on-board user program memory
  - — Expandable to 64K bytes using the IEEE-796 bus
- ☐ Powerful system monitor
  - — Display/modify/move/exchange/search/verify/test memory
  - — Display/modify internal registers
  - — Display input ports; write to output ports
  - — Load/verify/display PROM
  - — Full disassembler
- ☐ User-specified breakpoint
  - — One serial (logical AND of up to 4 conditions) or
  - — One parallel (logical OR of up to 15 conditions)
  - — Break delay and loop counter
  - — Break on: address, memory read/write, opcode fetch
- ☐ Three modes of operation
  - — Auxiliary hexadecimal keypad controlled
  - — External terminal controlled
  - — Host computer system controlled
- ☐ Serial interface: RS-232C, TTL, or 20 mA current loop
- ☐ EPROM programming capability (2716, 2732)

EVAKIT-87LC Add-On Boards

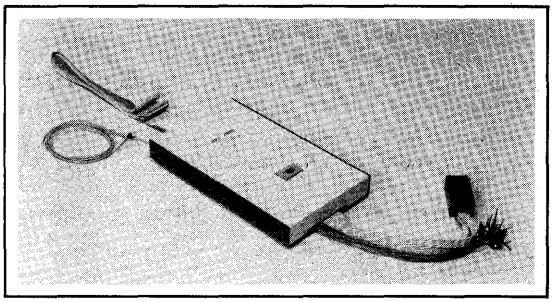
EV87LCRTT

The EV87LCRTT is the real-time trace board for use with NEC's EVAKIT-87LC stand-alone Evakit. The EV87LCRTT communicates with the EVAKIT-87LC via the IEEE-796 bus, adding real-time trace and additional breakpoint capabilities to the Evakit. A 1K X 59 bit trace RAM is available for storing the status of the address bus, data bus, control signals, I/O ports and ten external sense lines, as the user's program is executed in real-time. The trace data may be displayed in machine cycles or instruction mode with the user controlling the content of the display. The addition of another address breakpoint, a timer breakpoint, and a trace step breakpoint greatly increases the power of the EVAKIT-87LC.

EV78C06A

The EV78C06A is an add-on board for the EVAKIT-87LC which is required for emulating the μPD78C06A microcomputer. This board is connected between the Evakit and the target system, dividing the clock output of the Evakit by two. An emulation probe with a 64-pin QUIP header for plugging directly into the microcomputer socket of the target system is included with the EV76C06A.

IE-7809-M



Description

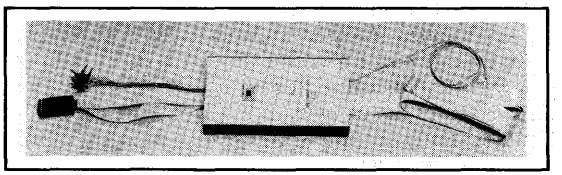
The IE-7809-M is one of the in-circuit emulators for NEC's μPD7800 series of 8-bit, single-chip microcomputers. The IE-7809-M provides complete hardware emulation and software debug capabilities for the μPD7807, μPD7808, and μPD7809 single-chip microcomputers. Real-time and single-step emulation capability, coupled with sophisticated memory mapping features, breakpoints and trace capabilities, create a powerful debug environment. A single-line assembler and disassembler, full register and memory control, and complete upload/download capabilities further simplify the task of debugging your hardware and software.

The IE-7809 can operate in two modes: as a stand-alone in-circuit emulator, controlled from either a user terminal or from a wide variety of host systems; or as an integral part of the MD-086 series microcomputer development system.

Features

- ☐ Real-time and single-step emulation
- ☐ User-designated breakpoints
- ☐ Sophisticated trace capabilities
  - — 1024 X 56-bit trace buffer
  - — Trace conditioning registers
  - — Instruction or machine cycle display
- ☐ Powerful memory mapping capability
  - — 64K bytes of RAM mappable in 256-byte blocks
- ☐ Line assembler/disassembler
- ☐ Eight external sense probes
- ☐ Self-diagnostic command
- ☐ Stand-alone configuration
  - — User terminal controlled
  - — Host computer system controlled
- ☐ MD-086 series development system bus-coupled configuration
  - — Symbolic debugging
  - — Macro command file capability
  - — Multiple IE-7809 operation
  - — Improved upload/download times

IE-87AD-M



Description

The IE-87AD-M is one of the in-circuit emulators for NEC's μPD7800 series of 8-bit, single-chip microcomputers. The IE-87AD-M provides complete hardware emulation and software debug capabilities for the μPD7810, and μPD7811 single-chip microcomputers. Real-time and single-step emulation capability, coupled with sophisticated memory mapping features, breakpoints, and trace capabilities create a powerful debug environment. A single-line assembler and disassembler, full register and memory control, and complete upload/download capabilities further simplify the task of debugging your hardware and software.

The IE-87AD-M can operate in two modes: as a stand-alone in-circuit emulator, controlled from either a user terminal or from a wide variety of host systems; or as an integral part of the MD-086 series microcomputer development system.

7

Features

- ☐ Real-time and single-step emulation
- ☐ User-designated breakpoints
- ☐ Sophisticated trace capabilities
  - — 1024 X 56-bit trace buffer
  - — Trace conditioning registers
  - — Instruction or machine cycle display
- ☐ Powerful memory mapping capability
  - — 64K bytes of RAM mappable in 256 byte blocks
- ☐ Line assembler/disassembler
- ☐ Eight external sense probes
- ☐ Self-diagnostic command
- ☐ Stand-alone configuration
  - — User terminal controlled
  - — Host computer system controlled
- ☐ MD-086 series development system bus-coupled configuration
  - — Symbolic debugging
  - — Macro command file capability
  - — Multiple IE-87AD-M Operation
  - — Improved upload/download times

IE-7811H-M

Description

The IE-7811H-M is one of the in-circuit emulators for NEC's μPD7800 series of 8-bit, single-chip microcomputers. The IE-7811H-M provides complete hardware emulation and software debug capabilities for the μPD7810H and μPD7811H single-chip microcomputers. Real-time and single-step emulation capability, coupled with sophisticated memory mapping features, breakpoints, and trace capabilities create a powerful debug environment. A single-line assembler, disassembler, full register, memory control, and complete upload/download capabilities further simplify the task of debugging your hardware and software.

The IE-7811H-M can operate in two modes: as a stand-alone in-circuit emulator, controlled from either a user terminal or from a wide variety of host systems; or as an integral part of the MD-086 series microcomputer development system.

Features

- ☐ Real-time and single-step emulation
- ☐ User-designated breakpoints
- ☐ Sophisticated trace capabilities
  - — 1024 X 56-bit trace buffer
  - — Trace conditioning registers
  - — Instruction or machine cycle display
- ☐ Powerful memory mapping capability
  - — 64K bytes of RAM mappable in 256-byte blocks
- ☐ Line assembler/disassembler
- ☐ Eight external sense probes
- ☐ Self-diagnostic command
- ☐ Stand-alone configuration
  - — User terminal controlled
  - — Host computer system controlled
- ☐ MD-086 series development system bus-coupled configuration
  - — Symbolic debugging
  - — Macro command file capability
  - — Multiple IE-87AD-M operation
  - — Improved upload/download times

IE-78C11-M

Description

The IE-78C11-M is one of the in-circuit emulators for NEC's μPD7800 series of 8-bit, single-chip microcomputers. The IE-78C11-M provides complete hardware emulation and software debug capabilities for the μPD78C10, μPD78C11 and μPD78C14 single-chip microcomputers. Real-time and single-step emulation capability, coupled with sophisticated memory mapping features, breakpoints and trace capabilities create a powerful debug environment. A single-line assembler, disassembler, full register, memory control, and complete upload/download capabilities further simplify the task of debugging your hardware and software.

The IE-78C11-M can operate in two modes: as a stand-alone in-circuit emulator, controlled from either a user terminal or from a wide variety of host systems; or as an integral part of the MD-086 series microcomputer development system.

Features

- ☐ Real-time and single-step emulation
- ☐ User-designated breakpoints
- ☐ Sophisticated trace capabilities
  - — 1024 X 56-bit trace buffer
  - — Trace conditioning registers
  - — Instruction or machine cycle display
- ☐ Powerful memory mapping capability
  - — 64K bytes of RAM mappable in 256 byte blocks
- ☐ Line assembler/disassembler
- ☐ Eight external sense probes
- ☐ Self-diagnostic command
- ☐ Stand-alone configuration
  - — User terminal controlled
  - — Host computer system controlled
- ☐ MD-086 series development system bus-coupled configuration
  - — Symbolic debugging
  - — Macro command file capability
  - — Multiple IE-78C11-M operation
  - — Improved upload/download times

μPD7800 Series System Evaluation Board

SE-78C06

The SE-78C06 is the system evaluation board for the μPD78C06 microcomputer. The SE-78C06 is functionally equivalent to the ROM-based microcomputer. With the user's program residing in a μPD2732 on-board, you can connect the SE-78C06 to your prototype, allowing total system performance evaluation.

PG1000 Personality Module

PG1003

The PG1003 is a plug-in personality module for the PG1000 PROM Programmer. This module is required to program the μPD78P09R, the EPROM version for the μPD7808 and μPD7809 8-bit, single-chip microcomputers. The PG1003 supports two programming modes: high-speed writing mode and normal writing mode.

IE-78310-R

Description

The IE-78310-R is the stand-alone in-circuit emulator for NEC's μPD78000 series of 8-bit, single-chip microcomputers. The IE-78310-R provides complete hardware emulation and software debug capabilities for the μPD78310 and μPD78312 single-chip microcomputers. Real-time and single-step emulation capability, coupled with sophisticated memory mapping features, breakpoints, and trace capabilities create a powerful debug environment.

A serial line from either a terminal or a host computer system controls the IE-78310-R. User programs can be uploaded or downloaded from the host system or from a PROM programmer connected to a second serial line.

Features

- ☐ Real-time and single-step emulation
  - — Up to 12 MHz external clock
  - — Software selectable internal or external clock
- ☐ Emulation memory
  - — 16K bytes of high-speed emulation memory for on-chip ROM
  - — 64K bytes of emulation memory for external memory mappable in 256-byte blocks
- ☐ Powerful system monitor
  - — Display/modify/move/exchange/search/verify/test memory
  - — Display/modify internal registers
  - — Upload/download capability
  - — Symbolic line assembler and disassembler
- ☐ User-specified breakpoints
  - — Logical OR of up to 4 conditions
  - — Logical AND of address, data, CPU status, loop count
  - — 8-bit external sense probe (bit-maskable)
  - — Emulation timer — 1 to 65,535 ms
  - — Program fetch count — 1 to 65,535 steps
- ☐ Real-time trace capability
  - — 2048 X 44-bit trace memory
  - — Traces: address, data, CPU status, ports 0-5, instruction queue status, macro service status, external sense probes
  - — User-specified trace qualifiers: address, data, CPU status, external sense probes
  - — Instruction/macro service/frame mode display
- ☐ Eight external sense probes for tracing user system signals
- ☐ Two RS-232C serial ports
- ☐ On-board self diagnostics

PRELIMINARY INFORMATION

IE-70322

Description

The IE-70322 is a portable stand-alone in-circuit emulator providing both hardware emulation and software debug capabilities for the NEC V25 (μPD70320/70322) 16-bit single-chip microcomputers. The standard IE-700K chassis integrates a 9.5 inch CRT display, two 5-1/4 inch 640 kilobyte floppy disk drives and an ASCII keyboard. Real-time and single-step emulation capability, coupled with sophisticated memory mapping features, breakpoints, and trace capabilities create a powerful debug environment. User programs can be uploaded and downloaded from a variety of host systems.

Features

- ☐ Portable stand-alone in-circuit emulator
  - — Integrated CRT, floppy disks, keyboard
  - — Can be upgraded to support V20/V30, V35, V40/V50, V60
- ☐ Precise real-time and single-step emulation
  - — Up to 8 MHz external clock
- ☐ User-specified mask ROM area of 0 KB, 8 KB, 16 KB or 32 KB
- ☐ 124 KB of high-speed emulation memory (expandable to 636 KB)
  - — Mappable in 4K blocks as user, internal or inhibited
- ☐ Seven user-specified breakpoints
  - — Selectable as execution or bus access cycle break
  - — Break loop counter
- ☐ Sophisticated real-time trace capability
  - — 2K trace buffer (sampling every machine cycle)
  - — Traces: IROM/memory address and data, CPU status, 16 external sense probes
  - — User-specified trace qualifiers
- ☐ Full symbolic debug capabilities
- ☐ Symbolic line assembler and disassembler
- ☐ Powerful communication software supporting:
  - — Digital Equipment Corporation VAX™ computers
  - — Intel Series II/III Development Systems
  - — IBM Personal Computers
  - — NEC MD-086 Series Development Systems
- ☐ Macro command file capability
- ☐ Full on-line help facility and screen editor
- ☐ EPROM programmer — 2732, 2764, 27128, 27256, 27512

VAX is a trademark of Digital Equipment Corporation.

EVAKIT-84C-1

Description

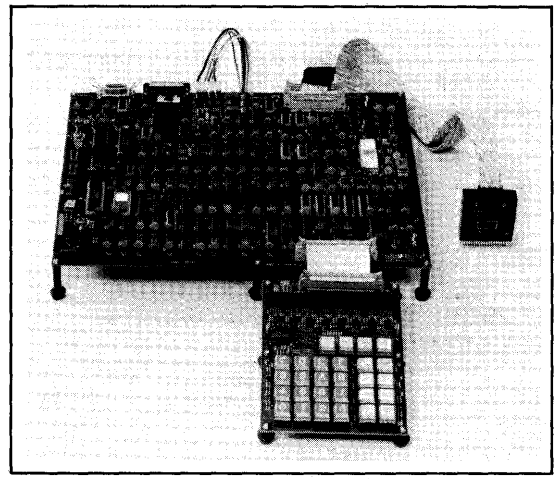
The EVAKIT-84C-1 is a stand-alone Evakit for NEC's μPD8048 series of 8-bit, single-chip microcomputers. The EVAKIT-84C-1 provides complete hardware emulation and software debug capabilities for the μPD8048H, μPD8049H, μPD80C48, μPD80C49H, and μPD80C50H microcomputers. Real-time and single-step emulation capability, coupled with a powerful on-board system monitor, and real-time trace capability create a powerful debug environment.

An on-board hexadecimal keypad or a serial line from a terminal or host computer controls the EVAKIT-84C-1. User programs are downloaded through the serial line or read from a PROM. Use the keypad to modify existing programs or create small programs. An on-board programmer for μPD2716, μPD8748, and μPD8749H EPROM devices provides an easy means for submitting your final code for production.

Features

- ☐ Real-time and single-step emulation capability
- ☐ 4K bytes on-board user program memory
- ☐ Powerful on-board system monitor
  - — Display/modify program memory
  - — Display/modify data memory
  - — Display/modify internal registers
  - — Display input ports; write to output ports
  - — Load/verify PROM
  - — Full disassembler
- ☐ Real-time trace capability — 256 steps
  - — Program counter; port 1, 2, or address/data on data bus
- ☐ User-specified breakpoints
  - — One serial (logical AND of up to 15 sequential addresses)
  - — Breakpoint loop counter: up to 16 counts
- ☐ Supports three operating modes
  - — On-board hexadecimal keypad controlled
  - — External terminal controlled
  - — Host computer system controlled
- ☐ Serial interface: RS-232C, TTL, 20 mA current loop
- ☐ EPROM programming capability (2716, 8748, 8749H)

EVAKIT-80C42



Description

The EVAKIT-80C42 is a stand-alone Evakit for NEC's μPD80C42 8-bit single-chip microcomputer that provides both complete hardware emulation and software debug capabilities. Real-time and single-step emulation capability, coupled with an on-board monitor create a powerful debug environment.

An auxiliary hexadecimal keypad or a serial line from a terminal or host computer controls the EVAKIT-80C42. User programs are downloaded through the serial line or read from a PROM. Use the keyboard to modify existing programs or create small programs. An on-board programmer for the μPD8741A EPROM device provides an easy means for submitting your final code for production.

Features

- ☐ Real-time and single-step emulation capability
- ☐ 2K bytes on-board user program memory
- ☐ Powerful on-board system monitor
  - — Display/modify/move/search/verify program memory
  - — Display/modify/move/search/verify data memory
  - — Display/modify internal registers
  - — Read/write to data bus buffer
  - — Display input ports; write to output ports
  - — Load/verify/display PROM
  - — Full disassembler

- ☐ Real-time trace capability — 256 steps
  - — Program counter; DBBIN, DBBOUT, and DBB status; OBF pin status
- ☐ User-specified breakpoints
  - — One serial (logical AND of up to 4 sequential addresses)
  - — One parallel (logical OR of up to 8 addresses)
  - — Breakpoint loop counter: up to 256 counts
- ☐ Supports three operating modes
  - — Auxiliary hexadecimal keypad controlled
  - — External terminal controlled
  - — Host computer system controlled
- ☐ Serial interface: RS-232C and TTL
- ☐ EPROM programming capability (μPD8741A)

μPD8048 Series Development Tool Selection Guide

Part Number	Emulator	System Evaluation Board	EPROM Device
μPD8035H	EVAKIT-84C-1	—	—
μPD8048H	EVAKIT-84C-1	—	μPD8748H*
μPD8039H	EVAKIT-84C-1	—	—
μPD8049H	EVAKIT-84C-1	—	μPD8749H*
μPD80C39H	EVAKIT-84C-1	—	—
μPD80C48	EVAKIT-84C-1	SE-80C50H	—
μPD80C35	EVAKIT-84C-1	—	—
μPD80C49H	EVAKIT-84C-1	SE-80C50H	—
μPD80C40H	EVAKIT-84C-1	—	—
μPD80C50H	EVAKIT-84C-1	SE-80C50H	—
μPD80C42	EVAKIT-80C42	—	μPD8741A

*μPD8748H and μPD8749H are both available in erasable windowed packages or in the economical one time programmable plastic package.

EV-9001/EV-9002

Description

The EV-9001 and EV-9002 shrink DIP conversion boards allow the standard in-circuit emulator and Evakit emulation cables to connect to shrink DIP sockets. The EV-9001-64 converts the emulation probe from a 64-pin QUIP to a 64-pin shrink DIP. The EV-9002-42/40/28 convert the emulation cables from 42-/40-/28-pin standard DIP to 42-/40-/28-pin shrink DIP respectively.

Ordering Information

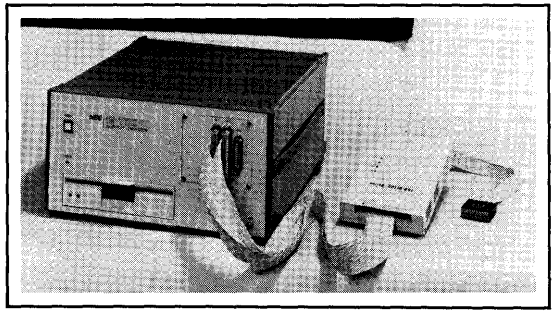
Conversion Board	Function
EV-9001-64	64-pin QUIP to 64-pin shrink DIP
EV-9002-42	42-pin standard DIP to 42-pin shrink DIP
EV-9002-40	40-pin standard DIP to 40-pin shrink DIP
EV-9002-28	28-pin standard DIP to 28-pin shrink DIP

SE-80C50H System Evaluation Board

The SE-80C50H is the system evaluation board for the following CMOS members of the μPD8048 series: μPD80C48H, μPD80C49H, and the μPD80C50H. The SE-80C50H is functionally equivalent to the ROM-based microcomputers. You can connect the SE-80C50H to your prototype with up to 4K of your program residing in an on-board μPD2716, μPD2732, μPD2732A, μPD2764, or a μPD27C64. This allows total system performance evaluation.

PRELIMINARY INFORMATION

IE-70108/70116



Description

The IE-70108 and IE-70116 are stand-alone in-circuit emulators that provide both hardware emulation and software debug capabilities for the NEC μPD70108 (V20) and μPD70116 (V30) respectively. Each system consists of a standard IE-70K chassis with interchangeable emulator pods for either the V20 or V30 microprocessor. The IE-70108/70116 provides real-time and single-step emulation in both native and 8080 emulation mode. User programs can be uploaded and downloaded from a variety of host systems via a serial link, or loaded directly from a CP/M-86® format 8" disk.

Features

- ☐ Stand-alone in-circuit emulator
  - — Interchangeable emulator pods for V20/V30
  - — Conversion kit available for IE-70208/70216-S008
- ☐ Precise real-time and single-step emulation
  - — 5/8 MHz internal clock
  - — Up to 8 MHz external clock
- ☐ Sophisticated memory mapping in 1K blocks of:
  - — 64K bytes of no wait state internal RAM
  - — 127K bytes of one wait state internal RAM (expandable to 610K bytes)
  - — Up to 1M byte of user system memory
- ☐ User programmable breakpoints and trace control
- ☐ 1K trace buffer — mnemonic and cyclic display
- ☐ Full symbolic debug capabilities
  - — 128K memory disk for rapid symbol search
- ☐ Symbolic line assembler and disassembler
- ☐ Full on-line help facility
- ☐ Macro command file capability
- ☐ External probes for tracing user system signals
- ☐ 1M byte 8" floppy disk drive

Ordering Information

Part Number	Description
IE-70108-S	In-circuit emulator for μPD70108 (with V20 pod)
IE-70116-S	In-circuit emulator for μPD70116 (with V30 pod)
IE-70108-001	Optional pod unit for μPD70108 emulation
IE-70116-001	Optional pod unit for μPD70116 emulation
IE-70116-1508	Converts IE-70208/216-S008 to IE-70108/70116-S

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V25/35 Series Selection Guide

Part Number	Emulator	EPROM Device
μPD70108 (V20)	IE-70108-S	—
μPD70116 (V30)	IE-70116-S	—
μPD70208 (V40)	IE-70208-S	—
μPD70216 (V50)	IE-70216-S	—
μPD70320 (V25)	IE-70322	—
μPD70322 (V25)	IE-70322	μPD70P322

ASM75

Description

The 7500 series absolute assembler (ASM75) converts symbolic source code for the entire 7500 series microcomputer family into executable absolute address object code. The assembler verifies that each instruction assembled is valid for the target microcomputer specified at assembly time. An object code file is produced in ASCII hexadecimal format and may be downloaded to a PROM programmer or hardware debugger.

The NEC ASM75 is available for use on all NEC development systems and many other manufacturers' microcomputer development systems, personal computers, minicomputers, and mainframes.

Features

- ☐ Absolute address object code output
- ☐ Macro definition capability
- ☐ Generic jump with optimization capability
- ☐ Conditional assembly options
  - — Up to eight levels of nesting
- ☐ User-selectable and directable output files
- ☐ Runs under a variety of operating systems
  - — CP/M-80®
  - — CP/M-86®
  - — MS-DOS®
  - — ISIS-II
- ☐ Fortran IV ANSI X3.9-1966 source program available

CP/M-80 and CP/M-86 are registered trademarks of Digital Research Corporation.

MS-DOS is a registered trademark of Microsoft Corporation.

Ordering Information

Part Number	Description
ASM75-C81	CP/M-80, 8" single-density floppy diskette
ASM75-D52	MS-DOS, 5-1/4" double-density floppy diskette
ASM75-I81	ISIS-II, 8" single-density floppy diskette
ASM75-I82	ISIS-II, 8" double-density floppy diskette
ASM75-M52	CP/M-86, 5-1/4" double-density floppy diskette
ASM75-M81	CP/M-86, 8" single-density floppy diskette
ASM75-F9T1	Fortran IV ANSI X3.9-1966 source program 9-track 1600 BPI magnetic tape

RA75X

Description

The RA75X relocatable assembler package converts symbolic source code for the μPD75104, μPD75106, and μPD75108 4-bit, single-chip microcomputers into an executable absolute address object code. This package consists of three separate programs: a relocatable assembler (RA75X), a linker (LK75X), and an object code converter (OC75X).

The RA75X translates a symbolic source module into a relocatable object module. The assembler verifies that each instruction assembled is valid for the target microcomputer specified at assembly time. LK75X combines multiple relocatable object modules into one absolute object module. OC75X produces an ASCII hexadecimal format object file.

The RA75X relocatable assembler package is available for use on all NEC development systems and many other manufacturers' development systems and personal computers.

Features

- ☐ Absolute address object code output
- ☐ User-selectable and directable output files
- ☐ Extensive error reporting
- ☐ Jump optimization
- ☐ Runs under a variety of operating systems
  - — CP/M-86®
  - — MS-DOS®

CP/M-86 is a registered trademark of Digital Research Corporation.

MS-DOS is a registered trademark of Microsoft Corporation.

Ordering Information

Part Number	Description
RA75X-D52	MS-DOS, 5-1/4" double-density floppy diskette
RA75X-M52	CP/M-86, 5-1/4" double-density floppy diskette
RA75X-M81	CP/M-86, 8" single-density floppy diskette

ASM87

Description

The 7800 series absolute assembler (ASM87) converts symbolic source code for the μPD7800, μPD7801, μPD7802, μPD78C05, μPD78C06, μPD7810, μPD7811, and μPD7816 microcomputers into executable absolute address object code. The assembler verifies that each instruction assembled is valid for the target microcomputer specified at assembly time. An object code file is produced in ASCII hexadecimal format and may be downloaded to a PROM programmer or hardware debugger.

The NEC ASM87 is available for use on all NEC development systems and many other manufacturers' microcomputer development systems, personal computers, minicomputers and mainframes.

Features

- ☐ Absolute address object code output
- ☐ Macro definition capability
- ☐ Generic jump with optimization capability
- ☐ Conditional assembly options
  - — Up to eight levels of nesting
- ☐ User-selectable and directable output files
- ☐ Runs under a variety of operating systems
  - — CP/M-80®
  - — CP/M-86®
  - — MS-DOS®
  - — ISIS-II
- ☐ Fortran IV ANSI X3.9-1966 source program available

CP/M-80 and CP/M-86 are registered trademarks of Digital Research Corporation.

MS-DOS is a registered trademark of Microsoft Corporation.

Ordering Information

Part Number	Description
ASM87-C81	CP/M-80, 8" single-density floppy diskette
ASM87-D52	MS-DOS, 5-1/4" double-density floppy diskette
ASM87-I81	ISIS-II, 8" single-density floppy diskette
ASM87-I82	ISIS-II, 8" double-density floppy diskette
ASM87-M52	CP/M-86, 5-1/4" double-density floppy diskette
ASM87-M81	CP/M-86, 8" single-density floppy diskette
ASM87-F9T1	Fortran IV ANSI X3.9-1966 source program 9-track 1600 BPI magnetic tape

RA87

Description

The RA87 relocatable assembler package converts symbolic source code for the entire 7800 family of 8-bit, single-chip microcomputers into executable absolute address object code. This package consists of three separate programs: a relocatable assembler (RA87), a linker (LK87), and an object converter (OC87).

The RA87 translates a symbolic source module into a relocatable object module. The assembler verifies that each instruction assembled is valid for the specified target microcomputer. LK87 combines multiple relocatable object modules into one absolute object module. OC87 produces an ASCII hexadecimal format object file.

The RA87 relocatable assembler package is available for use on all NEC development systems and many other manufacturers' microcomputer development systems and personal computers.

Features

- ☐ Absolute address object code output
- ☐ User-selectable and directable output files
- ☐ Extensive error reporting
- ☐ JMP/JRE optimization
- ☐ Runs under a variety of operating systems
  - — CP/M-86®
  - — MS-DOS®

CP/M-86 is a registered trademark of Digital Research Corporation.

MS-DOS is a registered trademark of Microsoft Corporation.

Ordering Information

Part Number	Description
RA87-D52	MS-DOS, 5-1/4" double-density floppy diskette
RA87-M52	CP/M-86, 5-1/4" double-density floppy diskette
RA87-M81	CP/M-86, 8" single-density floppy diskette

RA310

Description

The RA310 relocatable assembler package converts symbolic source code for the μPD78310 and μPD78312 8-bit, single-chip microcomputers into executable absolute address object code. This package consists of four separate programs: a relocatable assembler (RA310), a linker (LK310), a locator (LC310), and a librarian (LB310).

RA310 translates a symbolic source module into a relocatable object module. The assembler verifies that each instruction assembled is valid for the target microcomputer specified at assembly time. LK310 combines multiple relocatable object modules into one relocatable object module. LC310 assigns addresses to the relocatable object module and produces both an ASCII hexadecimal format object file and a symbol file for use by the 78000 series hardware emulators. LB310 creates and maintains files containing relocatable object modules. When the library file is included in the input to LK310, the linker only extracts those modules required to resolve external references and links them into the relocatable object module.

The RA310 relocatable assembler package is available for use on all NEC development systems and many other manufacturers' development systems, personal computers and minicomputers.

Features

- ☐ Macro definition capability
- ☐ Conditional assembly options
- ☐ Jump optimization
- ☐ Runs under a variety of operating systems
  - — CP/M-86®
  - — MS-DOS®
  - — VAX/VMS® and VAX/UNIX®

CP/M-86 is a registered trademark of Digital Research Corporation.

MS-DOS is a registered trademark of Microsoft Corporation.

VAX and VMS are registered trademarks of Digital Equipment Corporation.

UNIX is a trademark of AT&T.

Ordering Information

Part Number	Description
RA310-D52	MS-DOS, 5-1/4" double-density floppy diskette
RA310-M52	CP/M-86, 5-1/4" double-density floppy diskette
RA310-M81	CP/M-86, 8" single-density floppy diskette
RA310-VVT1	VAX/VMS, 9-track 1600 BPI magnetic tape
RA310-VXT1	VAX/UNIX, 9-track 1600 BPI magnetic tape

μPD70320/322 SOFTWARE RELOCATABLE ASSEMBLER DEVELOPMENT TOOLS

Description

The RA70320 Relocatable Assembler Package converts symbolic source code for the V25 (μPD70320/μPD70322) single-chip microcomputers into executable absolute address object code. The package consists of four separate programs: a relocatable assembler (RA70320), a linker (LK70320), a hexadecimal format object code converter (OC70320), and a librarian (LB70320).

RA70320 translates a symbolic source module into a relocatable object module. LK70320 combines relocatable object modules and absolute load modules and converts them into an absolute load module. OC70320 produces an ASCII hexadecimal format object file from either an absolute load or object module. LB70320 creates and maintains files containing relocatable object modules. When the library file is included as input to the LK70320, only those modules required to resolve external references are extracted from the library, relocated and linked into the absolute load module.

Features

- ☐ Absolute address object code output
- ☐ User-selectable and directable output files
- ☐ Extensive error reporting
- ☐ Powerful librarian
- ☐ Runs under a variety of operating systems
  - — CP/M-86®
  - — MS-DOS®
  - — ISIS/UDI
  - — VAX/VMS® and VAX/UNIX®

Ordering Information

Part Number	Description
RA70320-D52	MS-DOS, 5-1/4" double-density floppy diskette
RA70320-I81	ISIS-II, 8" single-density floppy diskette
RA70320-I82	ISIS-II, 8" double-density floppy diskette
RA70320-M52	CP/M-86, 5-1/4" double-density floppy diskette
RA70320-M81	CP/M-86, 8" single-density floppy diskette
RA70320-VVT1	VAX/VMS, 9 track 1600 BPI magnetic tape
RA70320-VXT1	VAX/UNIX, 9 track 1600 BPI magnetic tape

Description

The Evakit communication program (EVA) allows a variety of microcomputer development systems and personal computers to control NEC's Evakits and in-circuit emulators directly from the console of the host system. Once a particular emulator is selected from the EVA program's menu, EVA recognizes all legal commands for that emulator. In addition to the emulator standard commands, the EVA program provides commands to upload, download, and display disk files and directories, to save debug session on disk, to display command help files, and to exit from the program to the operating system.

You can download to the emulator object code program files produced by a cross assembler on the host system and upload patched copies of the program from the emulator to the disk for use in later debugging sessions. The disk display commands allow you to examine directories and files on the screen without having to exit the EVA program. This is extremely useful for checking a file before it is downloaded to the emulator or erased during an upload. The help command displays a complete list of all legal commands for the chosen emulator with their proper syntax. There is a command to exit from the EVA program and to return to the operating system. The emulator is not affected, and emulation can be continued by invoking the EVA program again.

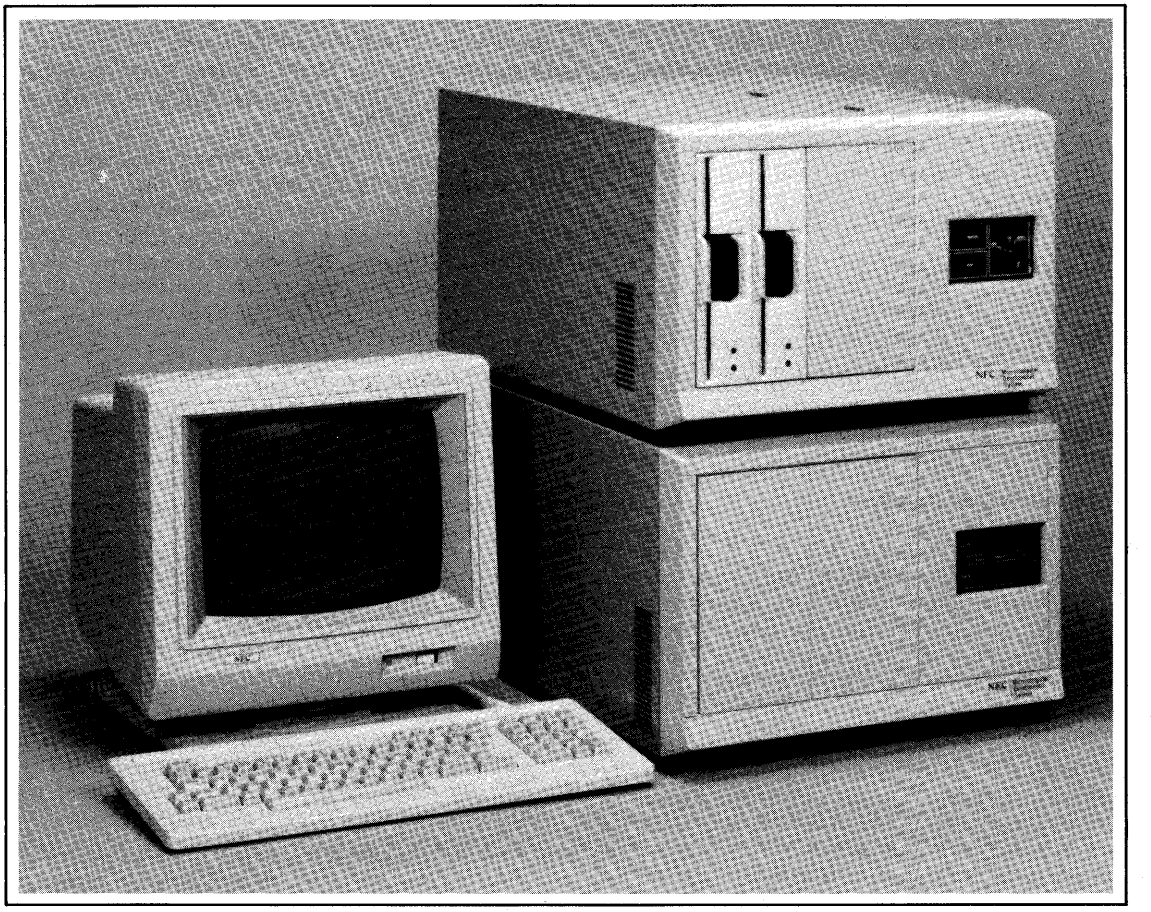
The EVA program is supplied in executable format and is included with each NEC assembler. Executable versions are available for the following host systems:

Intel MDS-220/330 under ISIS-II
NEC APC under CP/M-86®
IBM PC or PC/XT® under CP/M-86 or PC-DOS®
IBM PC/AT® under PC-DOS

Source code is available and may be modified to support other CP/M-80®, CP/M-86, MS-DOS®, and ISIS-II based systems.

The EVA program supports all current Evakits and in-circuit emulators and is periodically updated as new emulators are introduced.

MD-086 FLOPPY AND HARD DISK DRIVE SYSTEM



Description

The MD-086 series microcomputer development systems are a series of disk based, multi-user, multi-tasking systems supporting the development of products using NEC's microcomputers and microprocessors. Available in either a floppy disk-based or floppy/hard disk-based configuration, the MD-086 may be coupled with NEC's stand-alone evaluation kits (Evakits) or in-circuit emulators (IEs) to provide a complete integrated software and hardware development system.

Based on NEC's μPD8086 16-bit microprocessor, running Digital Research's MP/M-86® operating system, the MD-086 gives you access to all NEC's assemblers, simulators, high level language compilers, and all other CP/M-86® application software.

The MD-086FD-10 (floppy disk-based) consists of two units: the system chassis (housing all the electronics) and the system console (an ANSI standard X3.64 terminal.) The MD-086HD-10 (floppy/hard disk based) consists of three units: the system chassis, the hard disk chassis and the system console, and an ANSI standard terminal. Additional terminals may be added to the system as required, thereby lowering the system cost per user.

Features

- ☐ MP/M-86 multi-user/multi-tasking operating system
  - — Supports up to three users
  - — Supports multi-tasking at each user terminal
- ☐ 512K bytes of system memory
  - — Optional expansion to 1M byte total
- ☐ Two 1M byte 8" double-sided floppy disk drives
- ☐ Optional 35M byte hard disk
- ☐ 64K byte memory disk
- ☐ Two parallel printer ports
- ☐ IEEE-796 bus-based with 5 vacant slots for future expansion
- ☐ Separate ANSI standard X3.64 system console

Ordering Information

Part Number	Description
MD-086FD-10	MD-086 series, floppy disk-based system
MD-086HD-10	MD-086 series, floppy/hard disk-based system
MD-086DK	Hard disk upgrade for MD-086FD-10
MD-910TM	Character display terminal

Hardware Description

System Chassis

The system chassis of the MD-086 series houses a multiprocessor system, two 8" doubled-sided floppy disk drives, an IEEE-796 cardcage, power supply, and fans. Utilizing the industry standard IEEE-796 bus as its internal system bus, NEC's MD-086 series with several vacant slots, can easily be expanded to meet tommorrow's technological advances.

The multiprocessor architecture of the MD-086 series permits the master CPU to offload the time consuming tasks of data storage/retrieval and system I/O processing to its intelligent peripheral boards, significantly increasing the multi-user/ multi-tasking capabilities of the operating system. This multiprocessor system is composed of a μPD8086 master CPU board, a 512K-byte memory board, a μPD780-based intelligent floppy disk controller (FDC) board, a μPD8088-based intelligent system controller board (SCB), and an optional μPD780-based intelligent hard disk controller (HDC) board.

System Boards

The master CPU board is the heart of the system. Utilizing a μPD8086 microprocessor running at 5 MHz, it controls the operation of the multi-user/multi-programming operating system. The CPU board also contains the bootstrap loader PROM and the system work RAM, interrupt controller, and timer.

A single 512K-byte memory board provides the system memory and is accessed by either the master CPU board, the floppy disk controller board, or the optional hard disk controller board. System memory can be expanded to 1M byte by adding additional IEEE-796 bus memory boards.

The FDC board is an intelligent floppy disk controller board using NEC's μPD765A floppy disk controller chip to control up to four 8" double-sided floppy disk drives in either single or double-density format. Containing an NEC μPD780-1 microprocessor with 8K of PROM, 64K of RAM, and a DMA controller, the FDC board controls the transfer of data between the system memory and the floppy disk.

The HDC board is an intelligent hard disk controller board using NEC's μPD7261A hard disk controller chip to control up to two SMD interface hard disk drives. Containing an NEC μPD780-1 microprocessor with 8K PROM, 18K of RAM, and a DMA controller, the HDC board controls the transfer of data between the system memory and the hard disk.

The SCB is an intelligent I/O controller board using an NEC μPD8088 microprocessor with up to 16K bytes of PROM and 64K bytes of RAM to control the system console, the serial communication channels, the printer ports, and the paper tape interfaces.

The master CPU writes commands into the dual-ported memories on the FDC, HDC, and SCB boards. Each board executes its command with no further intervention by the master CPU. This increases the system performance of the MD-086 series.

The two 8" doubled-sided floppy disk drives provide approximately 2M bytes of data storage capacity. Single-sided diskettes are recorded in single-density to provide compatibility with other CP/M-86 and MP/M-86 systems. Double-sided diskettes are recorded in double-density providing a maximum storage capacity of 972K bytes per diskette.

Hard Disk Chassis

The optional hard disk chassis houses one 8" SMD interface hard disk drive capable of storing 32M bytes of formatted data, the power supply, and fans. A ready indicator, along with a write protect switch/indicator, and a fault switch/indicator are also provided.

System Console

The MD-910TM, an ANSI standard X3.64 CRT terminal, is provided as the system console for the MD-086 series microcomputer development systems. To take advantage of the multi-user features of the MD-086 series, additional ANSI standard terminals may be purchased separately from NEC Electronics Inc. or other manufacturers.

Software Description

The MD-086 series incorporates Digital Research's MP/M-86 operating system providing you a compact multi-user, multitasking operating system. Each user has complete access to all of the MP/M-86 facilities and may execute multiple programs simultaneously.

The powerful MP/M-86 file system manages all files and file directories, dynamically allocating, and releasing disk space as required. Designed for the multi-user environment, it enhances file integrity by permitting files to be opened in one of three modes: locked, unlocked, and read only modes. In locked mode, only one user may open a specific file at a given time, while in unlocked mode multiple users/programs may open the same file. Read only mode, permits a file to be opened by more than one process but it cannot be changed.

Optional password protection is available at both the file and disk level, providing protection for a particular user's files. MP/M-86's extended directories allow files to be dated and time stamped. Each file may have up to two date and time stamps: one reflects the date and time of the last update and the other the date of the last access or file creation.

All files generated on CP/M® 8" diskette systems may be read under MP/M-86, allowing you to easily transport existing software routines to the MD-086 series. Hardware-independent CP/M-86 application programs can be run, giving you access to a wide variety of third party software.

A 64K-byte memory disk residing in system memory is available for high speed file processing, significantly improving the overall performance of the MD-086 series microcomputer development systems.

The MD-086 series contains a PROM-resident monitor program which may be used for μPD8086 program development/debugging. This monitor program is entered automatically if there is no MP/M-86 system disk in drive A when the reset switch is pressed. Some of the main features of the MD-086 monitor are:

- ☐ Display, fill, substitute, compare, transmit, or test the contents of memory.
- ☐ Display and modify user registers.
- ☐ Read and write to the floppy disks and paper tape.
- ☐ Set breakpoints and execute user's program.
- ☐ Single-step and trace executing user's program.

Note:

CP/M is a registered trademark of Digital Research Corporation.

MD-086 Series Utilities

The following utility programs are supplied with the MD-086 series:

ABORT	Stops the specified process
ASM86	Absolute assembler for μPD8086/8088
ATTACH	Attaches program to its console
BACKUP	Makes a complete backup copy of a disk
CLEAR	Clears the system console screen
CONSOLE	Displays console number
DDT86	Dynamic debugging tool for μPD8086/8088
DIR	Displays disk directory of filenames
DSKRESET	Resets drives
ED	Line-oriented editor
ERA	Erases a file
ERAQ	Erases a file only after confirmation
FORMAT	Formats floppy disks
GENCMD	Converts H86 file to CMD file
GENSYS	Generates MP/M-86 operating system
HDBACKUP	Makes backup of hard disk logical drive
HDDUMP	Displays and changes contents of hard disk
HDFORMAT	Initializes hard disk logical drives
MPMSTAT	Displays MP/M-86 internal status
PHFORMAT	Physically formats hard disk
PIP	Copies files
PRINTER	Displays and sets the printer number
REN	Renames files
SDIR	Displays disk directory with options
SET	Sets disk and file protection levels, file attributes, and file time stamping
SHOW	Displays disk status and protection levels
SPOOL	Spools files to the list device
STAT	Displays, set files, and disk status
STOPSPLR	Stops the spooler
SUBMIT	Executes batch processing
SYSCPY	Copies system loader and MPM.SYS
TOD	Displays and sets time of day
TYPE	Displays ASCII file contents at console
USER	Displays and sets user number
YEAR	Sets the year

Five of these utilities have been incorporated into the operating system as resident system processes (RSPs) and reside in system memory. They can be executed without disk accesses, increasing the performance of the system. The RSPs in the MD-086 series include: ABORT, DSKRESET, MPMSTAT, PRINTER, and USER.

MD-086 Series Development Environment

The MD-086 series microcomputer development systems have been designed to provide a integrated software and hardware development environment for all NEC proprietary microcomputers, microprocessors, and digital signal and image processing components. For software development, a complete family of absolute and relocatable assemblers, high level language compilers, and digital signal and image processor simulators are available for the MD-086 Series. For software and hardware debug, NEC in-circuit emulators and Evakits can be controlled directly from the MD-086 series consoles.

Evakit communication programs are available for controlling all stand-alone Evakits via a serial link directly from any console of the development system. These programs provide program upload and download capability plus a full line assembler and disassembler.

Up to three in-circuit emulators can be plugged directly in the IEEE-796 backplane of the MD-086 series and controlled by the appropriate IE control program. In this bus-coupled configuration, your program debugging capabilities are greatly enhanced with the addition of symbolic debug, macro command file capability, and improved file upload/download times.

With the MD-086 series microcomputer development systems, you will always have access to development tools for NEC's newest components at the earliest possible time.

Documentation

The following documentation is supplied with the system. Additional copies may be obtained from NEC Electronics Inc.

- MD-086FD-10 Installation Manual
- MD-086FD-10 MP/M-86 Implementation Manual
- MD-910TM Terminal User Manual
- MP/M-86 Multi-Process Monitor User's Guide*
- MP/M-86 Operating System Guide*
- MP/M-86 Multi-Process Monitor Programmer's Guide*

*Additional copies may be obtained from Digital Research.

Equipment

The following equipment is supplied with the system:

MD-086FD-10

- 1 System chassis
- 2 RS-232C serial cables
- 1 Centronics printer cable
- 1 Line cord and ground adapter
- 1 Spare fuse
- 2 On-off keys
- 2 Male DB-25 solder type connectors/shells
- 1 Set of disk drive labels
- 2 8" floppy diskettes
  - — MP/M-86 system disk
  - — MP/M-86 gensys disk
- 1 MD-910TM system console
  - — 1 RS-232C cable
  - — 1 TTL level cable
  - — 1 Line cord and ground adapter
- 1 Set of documentation

MD-086HD-10

- 1 MD-086FD-10 system
- 1 MD-086DK

MD-086DK hard disk upgrade

- 1 Hard disk chassis
- 1 HDC board
- 1 Set of interconnecting cables
- 1 Line cord and ground adapter

Specifications

Processors

Main	μPD8086C, 5 MHz, CPU Board
Slave	μPD780C-1, 4 MHz, FDC Board
	μPD8088C-2, 6.5536 MHz, SCB Board
	μPD780C-1, 4 MHz, HDC Board

System Memory

512K-bytes of dynamic RAM (1M byte total — optional)

Operating system area	64K bytes
Memory Disk	64K bytes
User's Area	384K byte
	(896K bytes optional)

External Memory

Two double-sided 8" floppy disk drives
— 2M-byte maximum capacity

Optional SMD Interface 8" hard disk drive
— 32M-byte formatted capacity

Bus Structure

IEEE-796 Bus
— 5 spare slots in MD-086FD-10
— 4 spare slots in MD-086HD-10

Serial Interfaces

System console	RS-232C/TTL	1 channel
Serial interfaces	RS-232C	1 channel
	RS-232C/TTL	4 channel

Parallel Interfaces

Centronics printer interface 2 channel

Operating System

MP/M-86, version 2.0 with NEC proprietary enhancements.

Environmental Specifications

Temperature: −20 to +40°C, non-operating
+10 to +40°C, operating
Humidity: 10 to 90% relative humidity, non-operating
30 to 80% relative humidity, operating (without condensation)

Electrical Characteristics

FCC: Class A

AC Requirements:

System chassis: 90-132 V, 50/60 Hz ±2%, 5A
System console: 90-132 V, 50/60 Hz ±2%, 2A

Physical Characteristics

		System Console	
	System Chassis	CRT	Keyboard
Width	16.75 in (425 mm)	14.25 in (362 mm)	18.5 in (470 mm)
Height	11.77 in (299 mm)	14.29 in (363 mm)	1.50 in (38 mm)
Depth	24.21 in (615 mm)	13.46 in (342 mm)	7.44 in (189 mm)
Weight	59.40 lb (27 kg)	19.95 lb (9 kg)	4.41 lb (2 kg)

NEC
NEC Electronics Inc.

MD-910TM CHARACTER DISPLAY TERMINAL DEVELOPMENT TOOL

Description

The MD-910TM character display terminal is an ANSI standard CRT terminal used as the system console of the MD-086 series microcomputer development system. The MD-910TM can also be used as an additional console for this system, or as an external terminal for any stand-alone Evakit or in-circuit emulator.

Features

- ☐ Multiple emulation modes
  - — ANSI standard X3.64 (VT100 compatible)
  - — VT52 (Digital Equipment Corporation)
- ☐ Amber 12" nonglare screen
- ☐ Tilt/swivel display
- ☐ Detached low-profile keyboard conforming to DIN standard
  - — ASCII keys, numeric keypad, four function keys
- ☐ Total software set-up feature
- ☐ Smooth, jump, or partial scrolling
- ☐ 80/132 columns by 24-line display
- ☐ Standard, double width, or double height/width characters
- ☐ Blinking block, blinking underline, or invisible cursor
- ☐ Display attributes
  - — Normal, bold, blinking, reverse, underscore, overline, and vertical line
- ☐ Display status LEDs on keyboard
- ☐ Software selectable serial interface
  - — RS-232C, TTL, 20 mA current loop
  - — 7- or 8-bit character with odd, even, or no parity
  - — Full or half-duplex operation
  - — Transfer rate: 50 to 19200 BPS
- ☐ Power-on, self-diagnostic function and data analyzer mode
- ☐ Centronics printer port

Equipment

The following equipment is supplied with the MD-910TM terminal:

- 1 Display terminal
- 1 Keyboard with attached cable
- 1 RS-232C serial interface cable
- 1 TTL serial interface cable
- 1 AC power cord and ground adapter
- 1 Spare fuse
- 1 MD-910TM user's manual

Physical Characteristics

Dimension	Display	Keyboard
Width	14.25 in (362 mm)	18.05 in (470 mm)
Height	14.49 in (363 mm)	1.50 in (38 mm)
Depth	13.46 in (342 mm)	7.44 in (189 mm)
Weight	19.95 lb (9 Kg)	4.41 lb (2 Kg)

Environmental Specifications

Temperature: 0 to 40°C
Relative Humidity: 30 to 80% , non-condensing

Electrical Characteristics

FCC: Class A
Power: 90-132 V AC, 50/60 Hz ±2%, 2A

Ordering Information

Part Number	Description
MD-910TM	Character display terminal

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Description

The PG1000 is NEC's PROM Programmer for use with the MD-086 Series Development Systems and certain NEC Emulators. With the use of interchangeable personality modules, the user can tailor the PG1000 to support various NEC single-chip microcomputers. The user controls the PG1000 via the serial interface from either a host computer or an external terminal, or directly from the on-board keypad in stand-alone mode.

Features

- ☐ Interchangeable personality modules
- ☐ 16K of data RAM
- ☐ Address/data display and mode specification LEDs
- ☐ Flexible membrane keypad
- ☐ Three modes of operation
  - — Host computer controlled
  - — External terminal controlled
  - — Stand-alone operation
- ☐ Serial interface: RS-232C, TTL, or 20-mA current loop
- ☐ Parallel interface: TTL (two-wire handshake)

PG1000 Personality Modules

PG1003

The PG1003 is a plug-in personality module for the PG1000 PROM Programmer. This module is required to program the μPD78P09R, the EPROM version for the μPD7808 and μPD7809 8-bit, single-chip microcomputers. The PG1003 supports two programming modes: high-speed writing mode and normal writing mode.

PG1005

The PG1005 is a plug-in personality module for the PG1000 PROM Programmer. This module is required to program the μPD75P108, the EPROM version for the μPD75104, μPD75106, and μPD75108 4-bit, single-chip microcomputers. Interchangeable socket adapters are provided with the PG1005 to allow programming both shrink dip and flat packages.

PACKAGING INFORMATION

8

Section 8 — Packaging Information

Package/Device Cross Reference

Package	Device
20-Pin Plastic Shrink DIP (300 mil)	μPD7554CS μPD7564CS
20-Pin Plastic SO (Small Outline) (300 mil)	μPD7554G μPD7564G
24-Pin Plastic Shrink DIP (300 mil)	μPD7556CS μPD7566CS
24-Pin Plastic SO (Small Outline) (300 mil)	μPD7556G μPD7566G
28-Pin Plastic DIP (600 mil)	μPD7506C μPD7507SC
28-Pin Plastic Shrink DIP (400 mil)	μPD7506CT μPD7507SCT
40-Pin Plastic DIP (600 mil)	μPD7507C μPD7507HC μPD7508C μPD7508HC μPD7508AC μPD8035HLC μPD80C35C μPD8039HLC μPD80C39HC μPD80C40HC μPD8041AHC μPD80C42C μPD8048HC μPD80C48C μPD8049HC μPD80C49HC μPD80C50HC μPD8748HC μPD8749HC
40-Pin Plastic Shrink DIP (600 mil)	μPD7507CU μPD7507HCU μPD7508CU μPD7508HCU
40-Pin Ceramic Piggyback DIP (600 mil)	μPD75CG08E μPD75CG08HE
40-Pin Cerdip with Window (600 mil)	μPD8741AD μPD8748HD μPD8749HD
42-Pin Plastic DIP (600 mil)	μPD7527AC μPD7528AC μPD7533C μPD7537AC μPD7538AC
42-Pin Plastic Shrink DIP (600 mil)	μPD7527ACU μPD7528ACU μPD7533CU μPD7537ACU μPD7538ACU
42-Pin Ceramic Piggyback DIP	μPD75CG28E μPD75CG33E μPD75CG38E
44-Pin Plastic Miniflat	μPD48G-22 μPD49HG-22 μPD50HG-22 μPD7507HG-22 μPD7508HG-22 μPD7533G-22 μPD80C42G-22
52-Pin Plastic Miniflat	μPD7225G-00 μPD7506G-00 μPD7507G-00 μPD7508G-00 μPD80C48G-00 μPD80C49HG-00
54-Pin Plastic Miniflat	μPD6307G-F μPD6308G-F
54-Pin Plastic Miniflat (inverted leads)	μPD6307G-R μPD6308G-R
64-Pin Plastic Shrink DIP (750 mil)	μPD7516HCW μPD7519CW μPD7519HCW μPD7807CW μPD7808CW μPD7809CW μPD7810CW μPD78C10CW μPD7810HCW μPD7811CW μPD78C11CW μPD7811HCW μPD78C14CW μPD75104CW μPD75106CW μPD75108CW μPD75P108CW μPD78310CW μPD78312CW

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Package/Device Cross Reference

Package	Device
64-Pin Plastic Miniflat	μPD7227G-12 μPD7501G-12 μPD7502G-12 μPD7503G-12 μPD7516HG-12 μPD7519G-12 μPD7519HG-12 μPD78C06AG-12 μPD78C10G-1B μPD78C11G-1B μPD78C14G-1B μPD72030G-12 μPD75104G-1B μPD75106G-1B μPD75108G-1B μPD75P108G-1B μPD78310G-1B μPD78312G-1B
64-Pin Plastic QUIP	μPD7500HG-36 μPD7500HG-E-36 μPD7516HG-36 μPD7519G-36 μPD7519HG-36 μPD78C05AG-36 μPD7807G-36 μPD7808G-36 μPD7809G-36 μPD7810G-36
64-Pin Plastic QUIP (cont)	μPD78C10G-36 μPD7810HG-36 μPD7811G-36 μPD78C11G-36 μPD7811HG-36 μPD78C14G-36 μPD78310G-36 μPD78312G-36 μPD78P312G-36
64-Pin Shrink Cerdip with Window	μPD75P108DW
64-Pin Ceramic QUIP with Window	μPD78P09R
64-Pin Ceramic Piggyback QUIP	μPD75CG16HE μPD78PG11E μPD75CG19E μPD75CG19HE
68-Pin Plastic Leaded Chip Carrier (PLCC)	μPD78C10L μPD78C11L μPD78C14L μPD78310L μPD78312L
80-Pin Plastic Miniflat	μPD7228G-12 μPD7514G-12 μPD70320G-12 μPD70322G-12
84-Pin Plastic Leaded Chip Carrier (PLCC)	μPD70320L μPD70322L

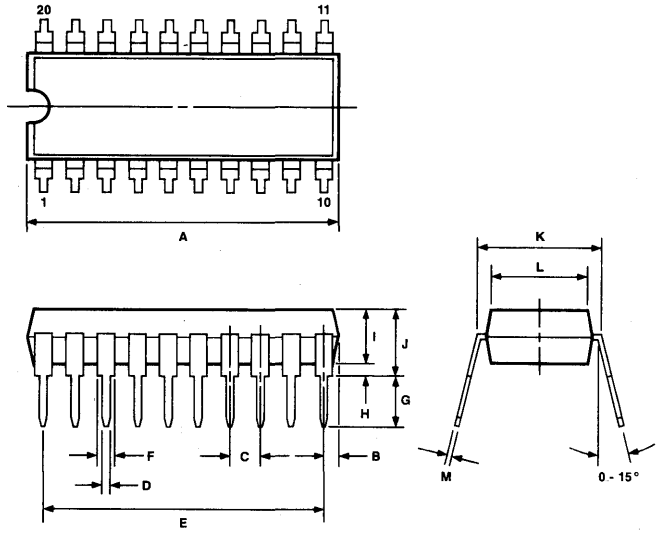
20-Pin Plastic Shrink DIP (300 mil)

Item	Millimeters	Inches
A	19.57 max	.771 max
B	1.78 max	.070 max
C	1.778 [TP]	.070 [TP]
D	.50 ±.10	.020 $^{+.004}_{-.005}$
E	16.0	.630
F	.85 min	.033 min
G	3.2 ±.3	.126 ±.012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.5	.256
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$

Note:

[1] Each lead centerline is located within .17 mm [.007 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



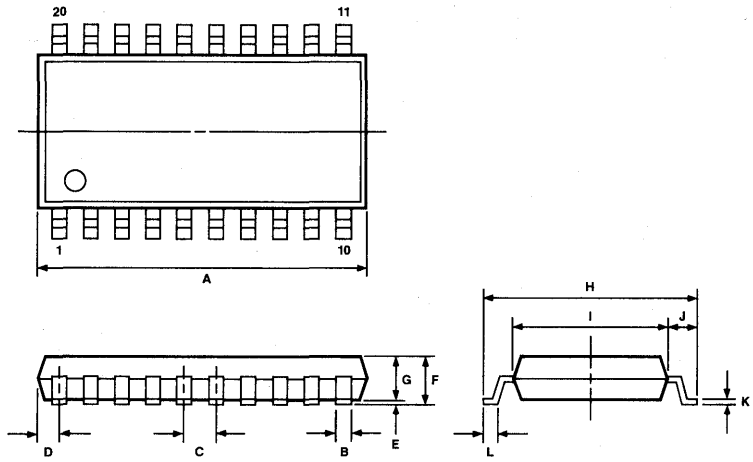
83-003609B

20-Pin Plastic SO (Small Outline) (300 mil)

Item	Millimeters	Inches
A	13.00 max	.512 max
B	.78 max	.031 max
C	1.27 [TP]	.050 [TP]
D	.40 $^{+.10}_{-.05}$	.016 $^{+.004}_{-.003}$
E	.1 ±.1	.004 ±.004
F	1.8 max	.071 max
G	1.55	.061
H	7.7 ±.3	.303 ±.012
I	5.6	.220
J	1.1	.043
K	.20 $^{+.10}_{-.05}$	.008 $^{+.004}_{-.002}$
L	.6 ±.2	.024 $^{+.008}_{-.009}$

Note:

[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.



83-003847B

8

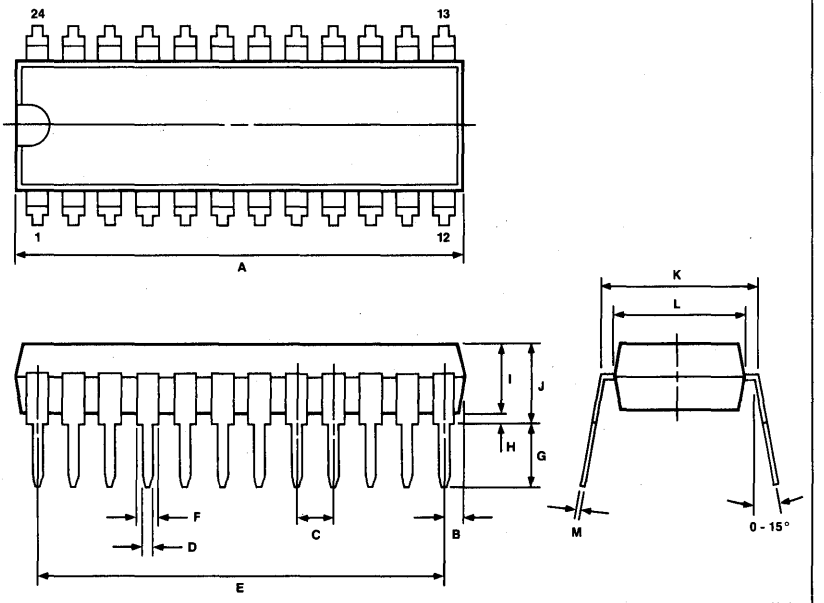
24-Pin Plastic Shrink DIP (300 mil)

Item	Millimeters	Inches
A	23.12 max	.911 max
B	1.78 max	.070 max
C	1.778 [TP]	.070 [TP]
D	.50 ±.10	.020 $^{+.004}_{-.005}$
E	19.558	.770
F	.85 min	.033 min
G	3.2 ±.3	.126 ±.012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	7.62 [TP]	.300 [TP]
L	6.5	.256
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$

Note:

[1] Each lead centerline is located within .17 mm [.007 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



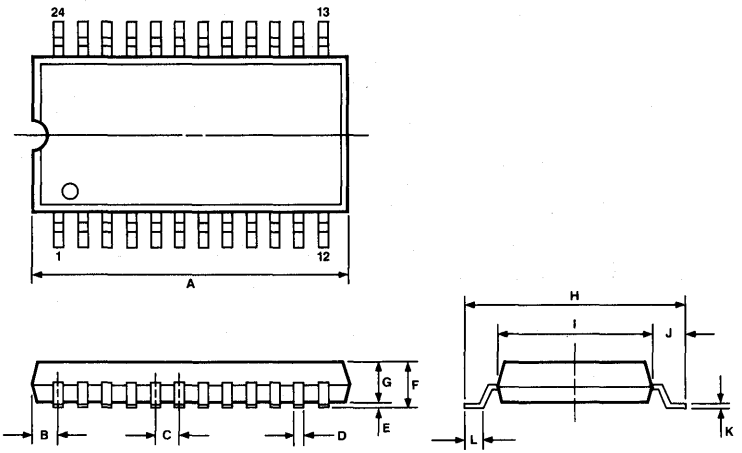
83-003783B

24-Pin Plastic SO (Small Outline) (300 mil)

Item	Millimeters	Inches
A	15.54 max	.612 max
B	.78 max	.031 max
C	1.27 [TP]	.050 [TP]
D	.40 $^{+.10}_{-.05}$	.016 $^{+.004}_{-.003}$
E	.1 ±.1	.004 ±.004
F	1.8 max	.071 max
G	1.55	.061
H	7.7 ±.3	.303 ±.012
I	5.6	.220
J	1.1	.043
K	.20 $^{+.10}_{-.05}$	.008 $^{+.004}_{-.002}$
L	.6 ±.2	.024 $^{+.008}_{-.009}$

Note:

[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.

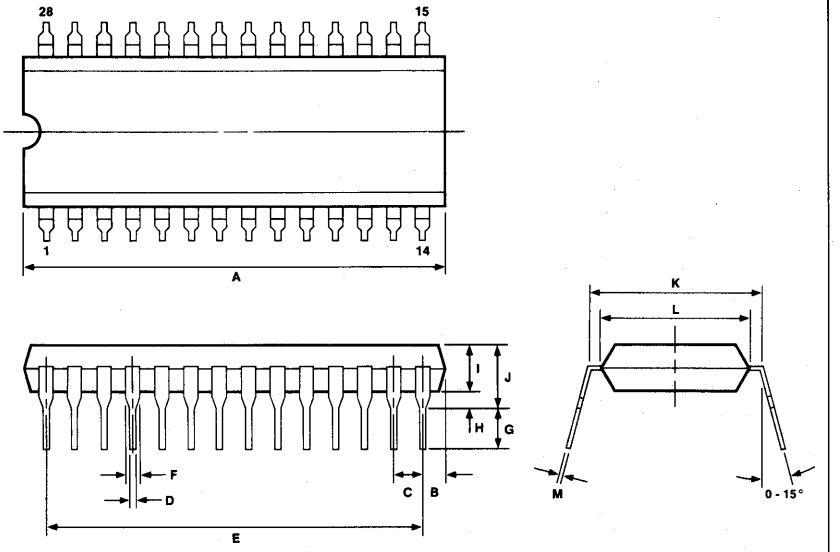


83-003857B

28-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	38.1 max	1.5 max
B	2.54 max	.10 max
C	2.54 [TP]	.10 [TP]
D	.5 ± .10	.02 $^{+.004}_{-.005}$
E	33.02	1.3
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.72 max	.226 max
K	15.24 [TP]	.60 [TP]
L	13.2	.52
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.

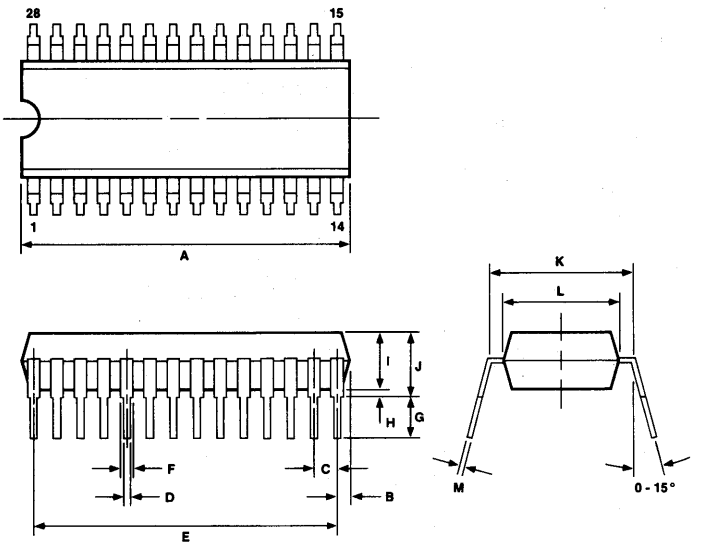


83-001407B

28-Pin Plastic Shrink DIP (400 mil)

Item	Millimeters	Inches
A	28.46 max	1.121 max
B	2.67 max	.106 max
C	1.778 [TP]	.070 [TP]
D	.50 ±.10	.02 $^{+.004}_{-.005}$
E	23.114	.91
F	.9 min	.035 min
G	3.2 ±0.3	.126 ±.012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	10.16 [TP]	.400 [TP]
L	8.6	.339
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:
1. Each lead centerline is located within .17 mm [.007 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



83-001519B

8

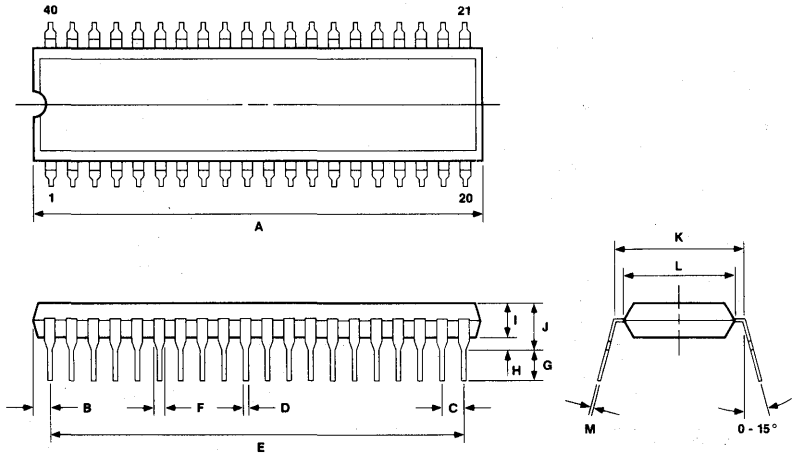
40-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ± .10	.020 $^{+.004}_{-.005}$
E	48.26	1.900
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.003}$

Notes:

[1] Each lead centerline is located within .25 mm [.010 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-001399B

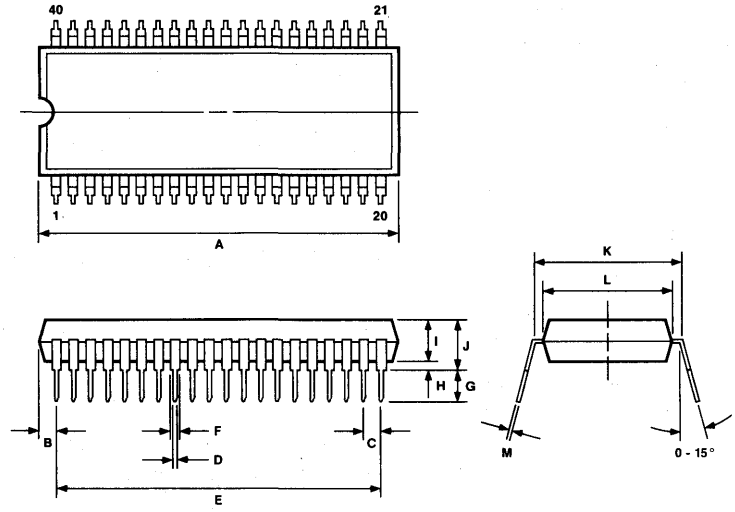
40-Pin Plastic Shrink DIP (600 mil)

Item	Millimeters	Inches
A	39.13 max	1.541 max
B	2.67 max	.106 max
C	1.778 [TP]	.070 [TP]
D	.50 ± .10	.020 ± .004
E	33.78	1.330
F	.9 min	.035 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.002}$

Note:

[1] Each lead centerline is located within .17 mm [.007 inch] of its true position [TP] at maximum material condition.

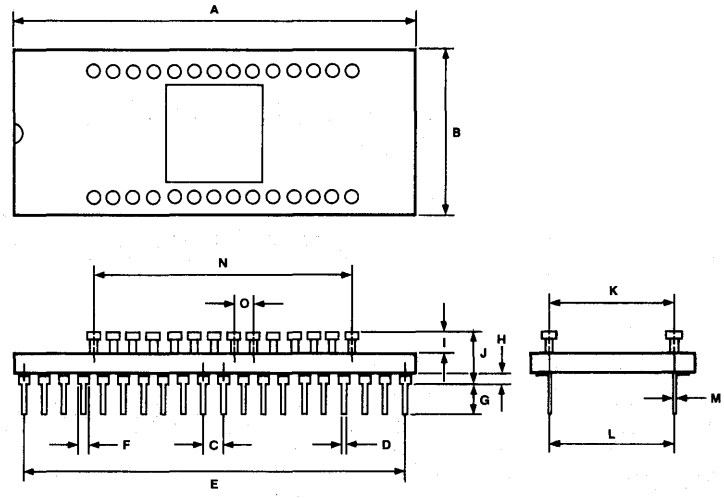
[2] Item "K" to center of leads when formed parallel.



83-003765B

40-Pin Ceramic Piggyback DIP (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.1 max
B	20.32	.8
C	2.54 ± .25	.1 ± .01
D	0.46 ± .05	.018 ± .002
E	48.26	1.9
F	1.02	.04
G	3.2 min	.126 min
H	1.02 min	.04 min
I	3.0 max	.118 max
J	4.32 max	.17 max
K	15.24	.6
L	15.24	.6
M	.25 ± .05	.01 ± .002
N	33.02	1.3
O	2.54 ± .25	.1 ± .01



83-003921B

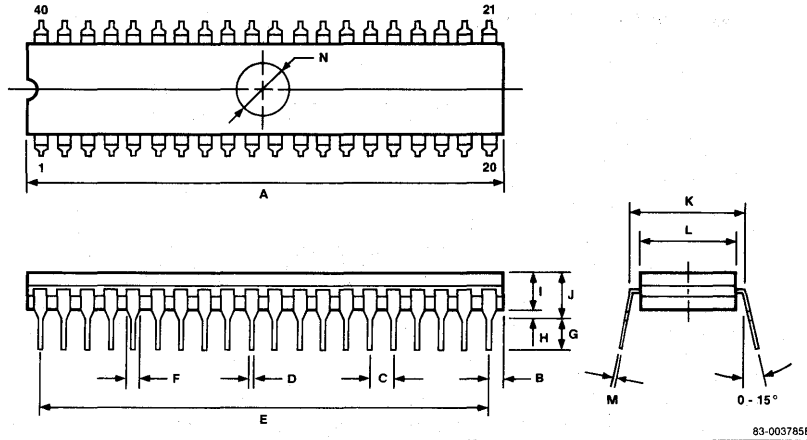
40-Pin Cerdip with Window (600 mil)

Item	Millimeters	Inches
A	53.34 max	2.100 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.50 ±.10	$.020^{+.004}_{-.005}$
E	48.26	1.900
F	1.2 min	.047 min
G	3.5 ±.3	.138 ±.012
H	.51 min	.020 min
I	3.80	.150
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.21	.520
M	.25 ±.05	$.010^{+.002}_{-.003}$
N	ϕ 7.62	ϕ .300

Note:

[1] Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003785B

8

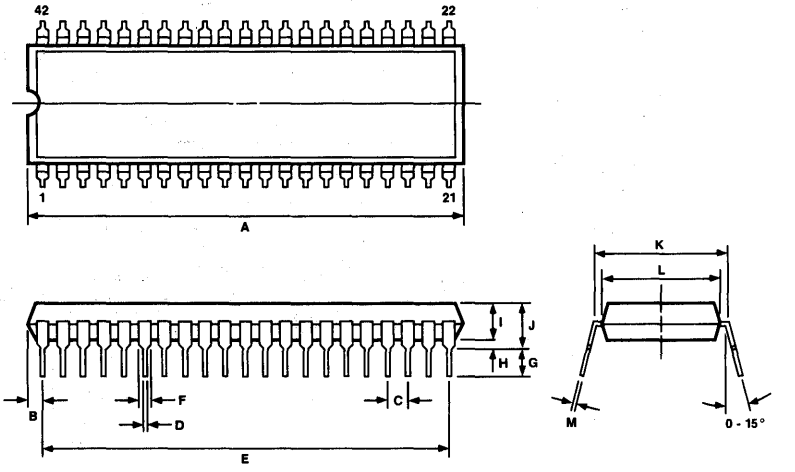
42-Pin Plastic DIP (600 mil)

Item	Millimeters	Inches
A	55.88 max	2.200 max
B	2.54 max	.100 max
C	2.54 [TP]	.100 [TP]
D	.5 ± .1	$.020^{+.004}_{-.005}$
E	50.8	2.000
F	1.2 min	.047 min
G	3.6 ± .3	.142 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.72 max	.226 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	$.25^{+.10}_{-.05}$	$.010^{+.004}_{-.003}$

Note:

[1] Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.

[2] Item "K" to center of leads when formed parallel.



83-003572B

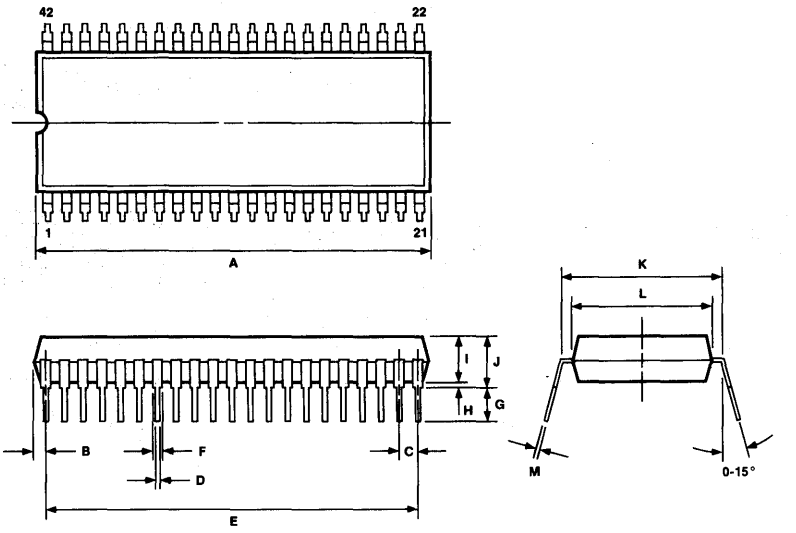
42-Pin Plastic Shrink DIP (600 mil)

Item	Millimeters	Inches
A	39.13 max	1.541 max
B	1.78 max	.070 max
C	1.778 [TP]	.070 [TP]
D	.50 ± .10	$.020^{+.004}_{-.005}$
E	35.57	1.400
F	.9 min	.035 min
G	3.2 ± .3	.126 ± .012
H	.51 min	.020 min
I	4.31 max	.170 max
J	5.08 max	.200 max
K	15.24 [TP]	.600 [TP]
L	13.2	.520
M	$.25^{+.10}_{-.05}$	$.10^{+.004}_{-.003}$

Note:

[1] Each lead centerline is located within .17 mm [.007 inch] of its true position [TP] at maximum material condition.

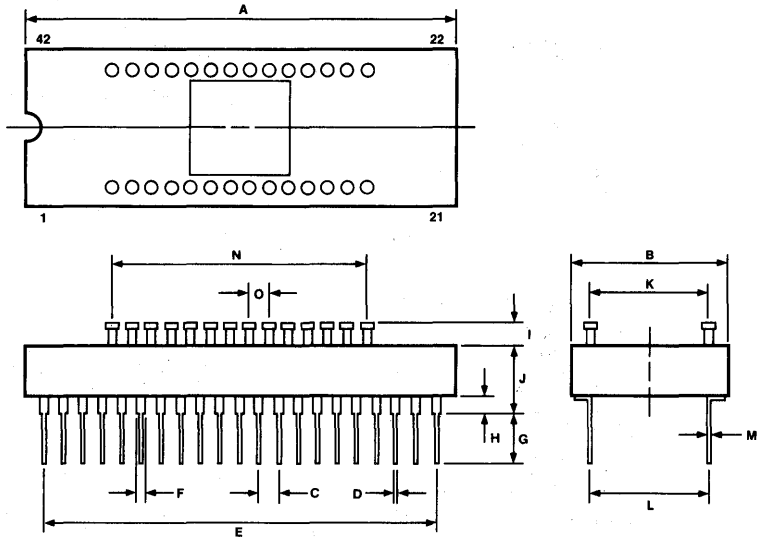
[2] Item "K" to center of leads when formed parallel.



83-003573B

42-Pin Ceramic Piggyback DIP

Item	Millimeters	Inches
A	55.88 max	2.200 max
B	20.32	.800
C	2.5 ± .25	.100 ± .010
D	0.46 ± .05	.018 ± .002
E	50.80	2.000
F	1.02	.040
G	3.2 min	.126 min
H	1.02 min	.040 min
I	3.0 max	.118 max
J	4.32 max	.170 max
K	15.24	.600
L	15.24	.600
M	.25 ± .05	.001 ± .010
N	33.02	1.300
O	2.54 ± .25	.100 ± .010



83-003574B

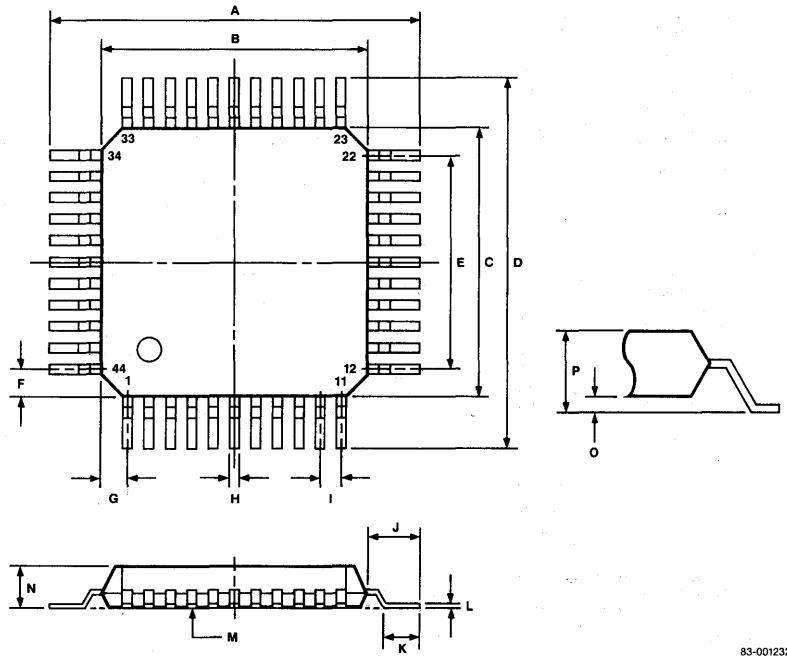
44-Pin Plastic Miniflat

Item	Millimeters	Inches
A	13.6 ±.4	.535 $^{+.017}_{-.016}$
B	10 ±.2	.394 $^{+.008}_{-.009}$
C	10 ±.2	.394 $^{+.008}_{-.009}$
D	13.6 ±.4	.535 $^{+.017}_{-.018}$
E	8.0	.315
F	1.0	.039
G	1.0	.039
H	.35 $^{+.20}_{-.10}$	.014 $^{+.006}_{-.005}$
I	.8 [TP] Note 1	.031 [TP]
J	1.8 ±.2	.071 $^{+.008}_{-.009}$
K	1.0 ±.2	.039 $^{+.009}_{-.008}$
L	.15 $^{+.10}_{-.05}$	.006 $^{+.004}_{-.003}$
M	.15 Note 2	.006
N	1.45 ±.1	.057 $^{+.005}_{-.004}$
O	0.0 ±.1	0.000 ±.004
P	1.65 max	.065 max

Note:

[1] Each lead centerline is located within .15 mm [.006 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



83-001232B

8

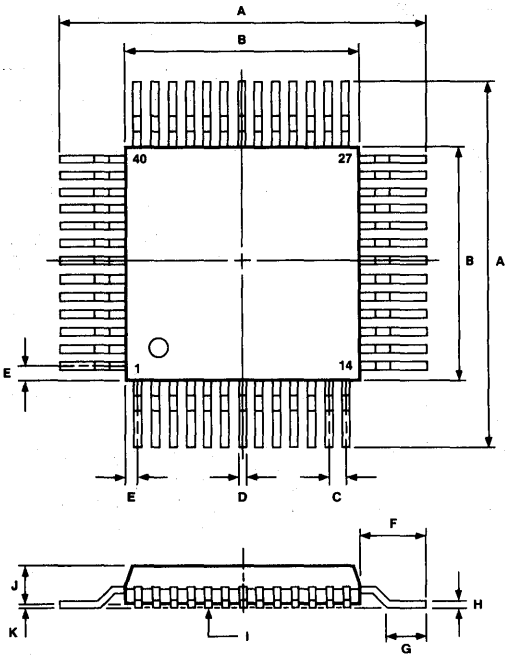
52-Pin Plastic Miniflat

Item	Millimeters	Inches
A	21.0 ±.4	.827 ±.016
B	14 ±.2	.551 $^{+.009}_{-.008}$
C	1.0 [TP] Note 1	.039 [TP]
D	.40 ±.10	.016 $^{+.004}_{-.005}$
E	1.0	.039
F	3.5 ±.2	.138 $^{+.008}_{-.009}$
G	2.2 ±.2	.087 $^{+.008}_{-.009}$
H	.15 $^{+.10}_{-.05}$	.006 $^{+.004}_{-.003}$
I	.15 Note 2	.006
J	2.6 $^{+.02}_{-.01}$	.102 $^{+.009}_{-.004}$
K	.1 ±.1	.004 ±.004

Note:

[1] Each lead centerline is located within .20 mm [.008 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



83-000932B

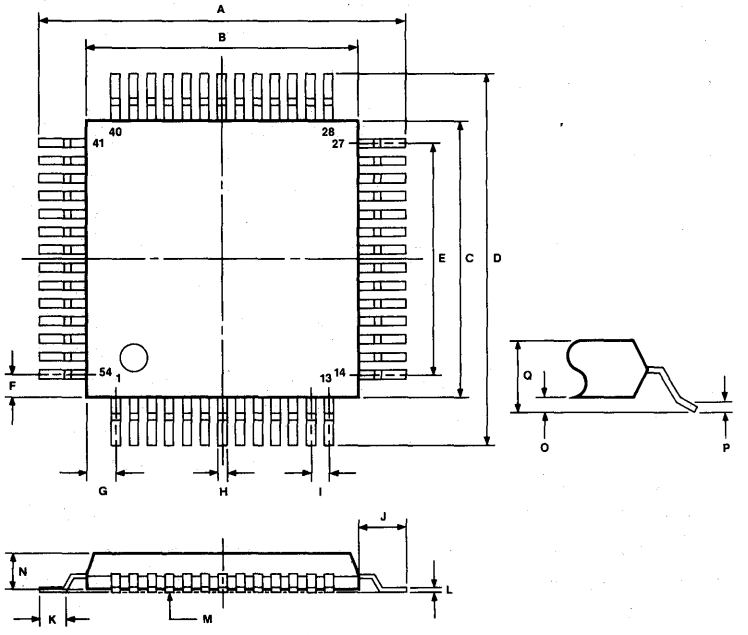
54-Pin Plastic Miniflat

Item	Millimeters	Inches
A	13.5 ±.4	.531 $^{+.017}_{-.016}$
B	9.5 ±.2	.374 ±.008
C	9.5 ±.2	.374 ±.008
D	13.5 ±.4	.531 $^{+.017}_{-.018}$
E	8.45	.333
F	.5	.020
G	.85	.033
H	.30 ±.10	.012 $^{+.004}_{-.005}$
I	.65 [TP] Note 1	.026 [TP]
J	2.0 ±.2	.079 $^{+.008}_{-.009}$
K	1.2 ±.2	.047 $^{+.009}_{-.008}$
L	.15 $^{+.10}_{-.05}$	.006 $^{+.004}_{-.003}$
M	.15 Note 2	.006
N	1.5 ±.1	.059 ±.004
O	0.1 ±.1	0.004 ±.004
P	0.1 ±.1	0.004 ±.004
Q	1.8 max	.071 max

Note:

[1] Each lead centerline is located within .15 mm [.006 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



83-003854B

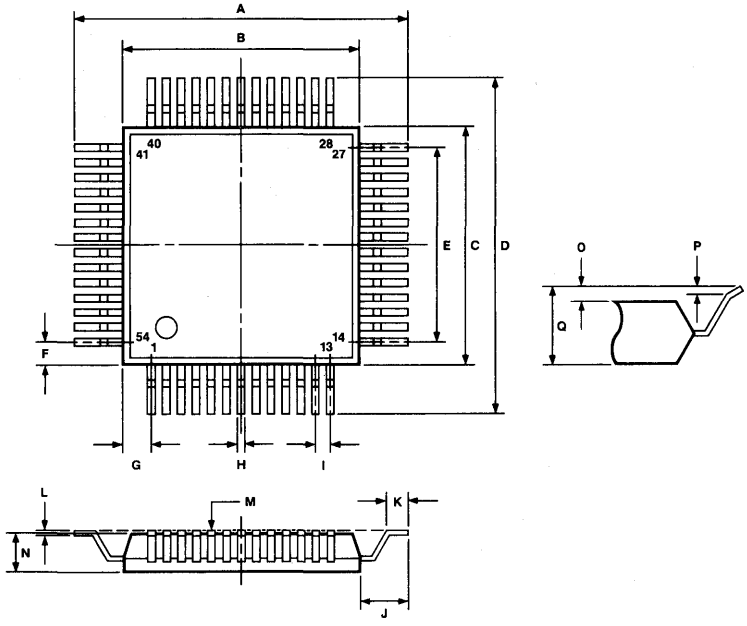
54-Pin Plastic Miniflat (inverted leads)

Item	Millimeters	Inches
A	13.9 ±.4	.547 ±.016
B	9.5 ±.2	.374 ±.008
C	9.5 ±.2	.374 ±.008
D	13.9 ±.4	.547 ±.016
E	8.45	.333
F	.5	.020
G	.85	.033
H	.30 ±.10	.012 $^{+.004}_{-.005}$
I	.65 [TP] Note 1	.026 [TP]
J	2.2 ±.2	.079 $^{+.008}_{-.009}$
K	.9 ±.2	.047 $^{+.009}_{-.008}$
L	.15 $^{+.10}_{-.05}$	.006 $^{+.004}_{-.003}$
M	.15 Note 2	.006
N	1.5 ±.1	.059 ±.004
O	0.1 ±.1	0.004 ±.004
P	0.1 ±.1	0.004 ±.004
Q	1.8 max	.071 max

Note:

[1] Each lead centerline is located within .15 mm [.006 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



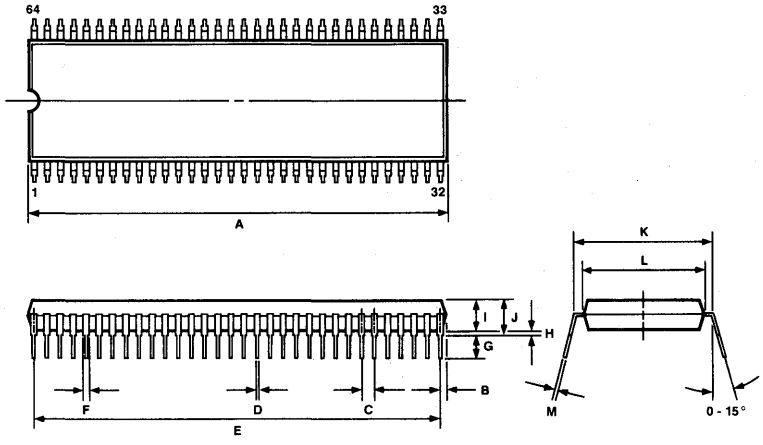
83-003855B

64-Pin Plastic Shrink DIP (750 mil)

Item	Millimeters	Inches
A	58.68 max	2.311 max
B	1.78 max	.07 max
C	1.778 [TP]	.07 [TP]
D	.5 ±.10	.02 $^{+.004}_{-.005}$
E	55.12	2.17
F	.9 min	.035 min
G	3.2 ±.3	.126 ±.012
H	.51 min	.02 min
I	4.31 max	.17 max
J	5.08 max	.2 max
K	19.05 [TP]	.75 [TP]
L	17	.669
M	.25 $^{+.10}_{-.05}$	.01 $^{+.004}_{-.003}$

Notes:

1. Each lead centerline is located within .17 mm [.0007 inch] of its true position [TP] at maximum material condition.
2. Item "K" to center of leads when formed parallel.



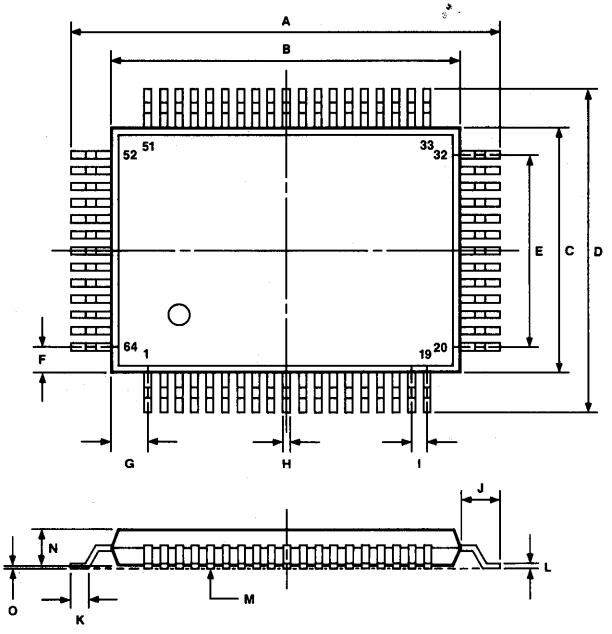
83-001494B

8

64-Pin Plastic Miniflat

Item	Millimeters	Inches
A	24.7 ±.4	.972 $^{+.017}_{-.016}$
B	20 ±.2	.795 $^{+.009}_{-.008}$
C	14 ±.2	.551 $^{+.009}_{-.008}$
D	18.7 ±.4	0.736 ±.016
E	12.0	.472
F	1.0	.039
G	1.0	.039
H	.40 ±.10	.016 $^{+.004}_{-.005}$
I	1.0 [TP] Note 1	.039 [TP]
J	2.35 ±.2	.093 $^{+.008}_{-.009}$
K	1.2 ±.2	.047 $^{+.009}_{-.008}$
L	.15 $^{+.10}_{-.05}$	.006 $^{+.004}_{-.003}$
M	.15 Note 2	.006
N	2.05 $^{+.2}_{-.1}$	.081 $^{+.008}_{-.005}$
O	0.1 ±.1	0.004 ±.004

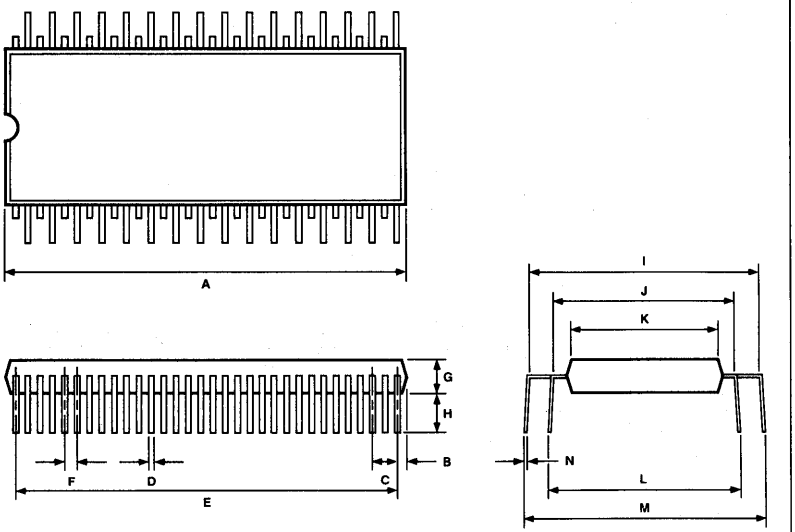
Note:
[1] Each lead centerline is located within .20 mm [.008 inch] of its true position [TP] at maximum material condition.
[2] Flat within .15 mm [.006 inch] total.



83-000933B

64-Pin Plastic QUIP

Item	Millimeters	Inches
A	41.8 max	1.65 max
C	2.54	.100
D	.5 ±.1	.020 ±.004
E	39.37	1.55
F	1.27 min	.050 min
G	3.6	.142
H	3.2 min	.126 min
I	24.13 ±1.05	.950 ±.041
J	19.05 ±1.05	.750 ±.041
K	16.5	.650
N	.25 $^{+.10}_{-.05}$	.010 $^{+.004}_{-.002}$



83-001508B

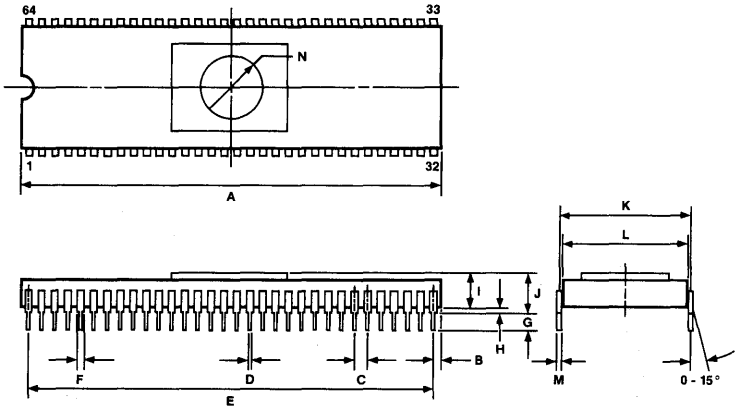
64-Pin Shrink Cerdip with Window

Item	Millimeters	Inches
A	58.68 max	2.311 max
B	1.78 max	.070 max
C	1.778 [TP]	.070 [TP]
D	.46 ±.05	.018 ±.002
E	55.11	2.17
F	.08 min	.003 min
G	3.5 ±.3	.138 ±.012
H	1.0 min	.093 min
I	3.0	.118
J	5.08 max	.200 max
K	19.05 [TP]	.750 [TP]
L	18.8	.740
M	.25 ±.05	.010 ±.002
N	7.62 dia	.300 dia

Note:

[1] Each lead centerline is located within .25 mm [.01 inch] of its true position [TP] at maximum material condition.

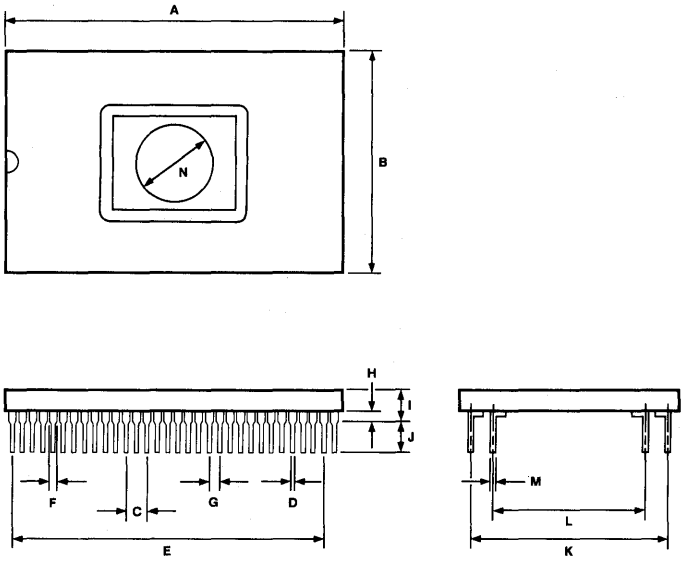
[2] Item "K" to center of leads when formed parallel.



83-003933B

64-Pin Ceramic QUIP with Window

Item	Millimeters	Inches
A	42.0 max	1.65 max
B	26.67	1.05
C	2.54 ±.25	.1 ±.01
D	.46 ±.05	.018 ±.002
E	38.10	1.5
F	1.02	.04
G	1.27 ±.25	.05 ±.01
H	1.02 min	.04 min
I	4.95 max	.194 max
J	3.2 min	.126 min
K	24.13	.95
L	19.05	.75
M	.25 ±.05	.01 ±.002
N	8.89 dia	.350 dia

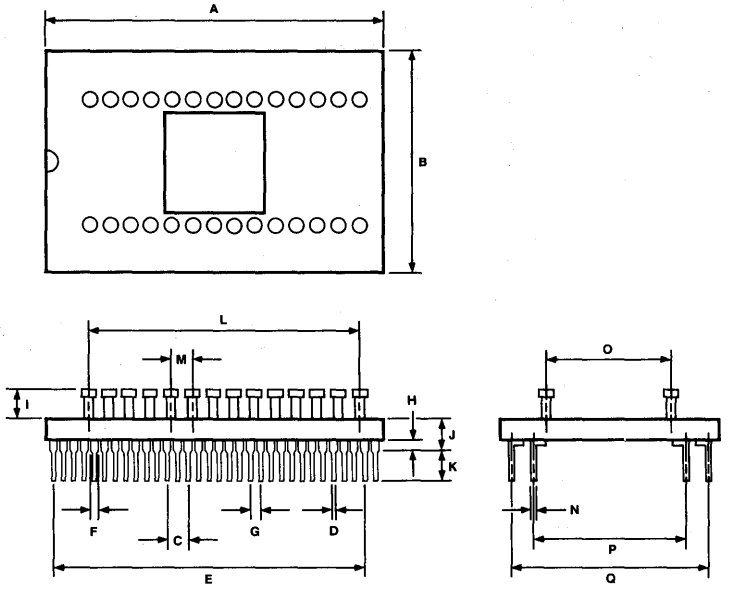


83-003929B

8

64-Pin Ceramic Piggyback QUIP

Item	Millimeters	Inches
A	42.0 max	1.65 max
B	26.67	1.050
C	2.54 ±.25	.100 ±.010
D	.46 ±.05	.018 ±.002
E	38.10	1.500
F	1.02	.040
G	1.27 ±.25	.050 ±.010
H	1.02 min	.040 min
I	3.9 max	.154 max
J	4.45 max	.175 max
K	3.2 min	.126 min
L	33.02	1.300
M	2.54 ±.25	.100 ±.010
N	.25 ±.05	.010 ±.002
O	15.24	.600
P	19.05	.750
Q	24.13	.950



83—003844B

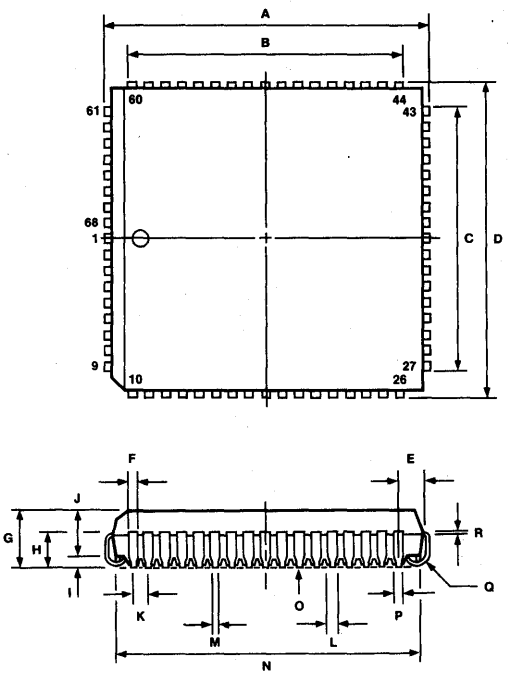
68-Pin Plastic Leaded Chip Carrier (PLCC)

Item	Millimeters	Inches
A	25.2 ±.2	.992 ±.008
B	24.20	.953
C	24.20	.953
D	25.2 ±.2	.992 ±.008
E	1.94 ±.15	.076 $^{+.007}_{-.006}$
F	.6	.024
G	4.4 ±.2	.173 $^{+.009}_{-.008}$
H	2.8 ±.2	.110 $^{+.009}_{-.008}$
I	.7 min	.028 min
J	3.6	.142
K	1.27 [TP] Note 1	.050 [TP]
L	.7	.028
M	.40 ±.10	.016 $^{+.004}_{-.005}$
N	23.12 ±.20	.910 $^{+.009}_{-.008}$
O	.15 Note 2	.006
P	1.0	.040
Q	R .8	R .031
R	.20 $^{+.10}_{-.06}$	.008 $^{+.004}_{-.002}$

Note:

[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



83-003792B

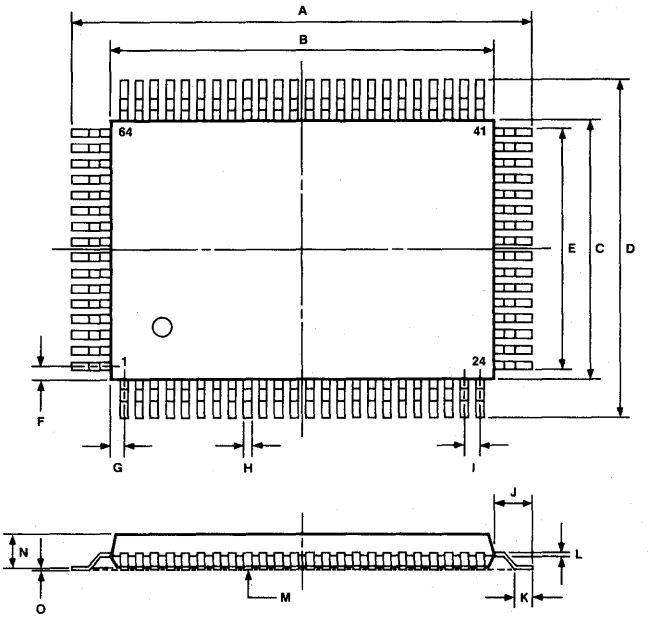
80-Pin Plastic Miniflat

Item	Millimeters	Inches
A	24.7 ±.4	.972 $^{+.017}_{-.016}$
B	20 ±.3	.795 $^{+.009}_{-.008}$
C	14 ±.2	.551 $^{+.009}_{-.008}$
D	18.7 ±.4	.736 ±.016
E	12	.472
F	1.0	.039
G	.8	.031
H	.35 ±.1	.014 $^{+.004}_{-.003}$
I	.8 [TP] Note 1	.031 [TP]
J	2.35 ±.3	.093 $^{+.006}_{-.009}$
K	1.2 ±.2	.047 $^{+.009}_{-.006}$
L	.15 $^{+.10}_{-.009}$	.006 $^{+.004}_{-.003}$
M	.15 Note 2	.006
N	2.05 $^{+.2}_{-.1}$	.081 $^{+.006}_{-.005}$
O	.1 ±.1	.004 ±.004

Note:

[1] Each lead centerline is located within .15 mm [.006 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



83-001230B

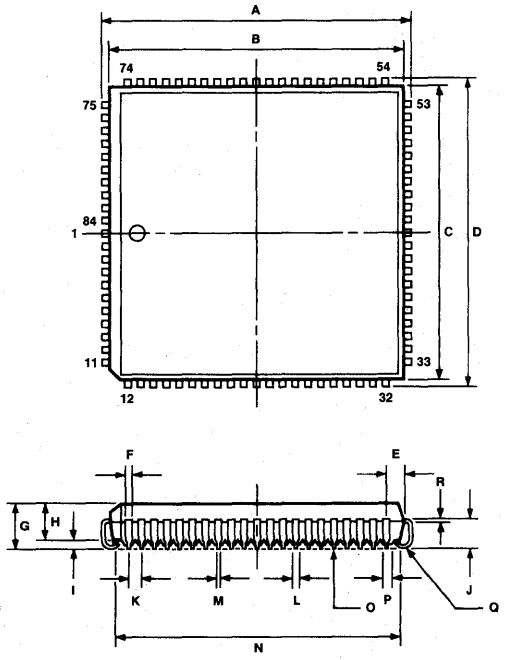
84-Pin Plastic Leaded Chip Carrier (PLCC)

Item	Millimeters	Inches
A	30.4 ±.2	1.197 ±.008
B	29.30	1.154
C	29.30	1.154
D	30.4 ±.2	1.197 ±.008
E	1.95 ±.15	.077 $^{+.006}_{-.007}$
F	.6	.024
G	4.4 ±.2	.173 $^{+.009}_{-.008}$
H	2.5 ±.2	.098 $^{+.009}_{-.008}$
I	.6 min	.024 min
J	3.7	.146
K	1.27 [TP] Note 1	.050 [TP]
L	.7	.028
M	.40 ±.10	.016 $^{+.004}_{-.005}$
N	28.51 ±.20	1.122 $^{+.009}_{-.008}$
O	.15 Note 2	.006
P	1.0	.040
Q	R .8	R .031
R	.20 $^{+.010}_{-.005}$	.008 $^{+.004}_{-.002}$

Note:

[1] Each lead centerline is located within .12 mm [.005 inch] of its true position [TP] at maximum material condition.

[2] Flat within .15 mm [.006 inch] total.



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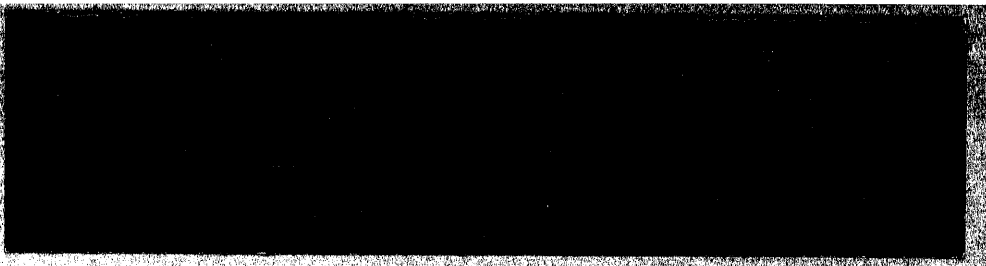

NEC

NEC Electronics Inc.

CORPORATE HEADQUARTERS

401 Ellis Street
P.O. Box 7241
Mountain View, CA 94039
TEL: 415-960-6000
TWX: 910-379-6985

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